HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

12845A

LINE PRINTER INTERFACE KIT

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Printed-Circuit Assembly:

12845-60001, Series 1214

Note

This manual should be retained with the Hewlett-Packard computer system documentation.

12845-90001

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SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the HP 12845A Line Printer Interface Kit (see figure 1-1).

1-3. GENERAL DESCRIPTION.

1-4. The HP 12845A Line Printer Interface Kit provides the necessary equipment to enable using the HP 2610A or the HP 2614A Line Printers with an HP 2100, 2114, 2115 or 2116 Computer. The kit contains the following items:

a. One line printer interface printed-circuit assembly (PCA), part no. 12845-60001.

b. One cable assembly, part no. 12845-60002.

c. One *Operating* and *Service Manual*, part no. 12845-90001.

1-5. The line printer interface kit uses a printed-circuit assembly (referred to in this manual as a PCA) which contains integrated circuits that transfer data and status information between the computer and the line printer. The interface PCA contains two groups of register circuits, one for output from the computer to the line printer and one for input from the line printer to the computer. Seven data bits are transferred from the computer through the output register to the line printer, and three status bits are transferred from the line printer through the input register to the computer. In addition to the register circuits, the interface PCA contains control and interrupt logic circuits that permit programming of the I/O functions.

1-6. The following information is transferred from the interface PCA to the line printer:

a. The Master Clear signal is derived from a CRS signal from the computer and restores the line printer circuits to the original state.

b. The Information Ready signal is derived from an STC signal from the computer and indicates when data is available for transfer to the line printer.

c. The Control Bit signal is derived from the logical state of bit 15 in the computer output word and informs the line printer if the character on the data lines is a data character or a format character.

d. Output register data bits 0 through 6 represent an ASCII (American Standard Code for Information Interchange) data character for printout or a format character for vertical line spacing.

1-7. The following information is transferred from the line printer to the interface PCA:

a. The Output Resume signal indicates when the line printer is able to accept a new character.

b. The Ready signal indicates the operational readiness of the line printer.

c. The Line Ready signal indicates that the line printer is ready to accept a line of data.

d. The Paper Out signal indicates an out-of-paper or paper-tear condition in the line printer.

1-8. IDENTIFICATION.

1-9. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code stamped on the PCA (e.g., A-1214-22). The letter code identifies the version of the etched trace pattern. The series code (four middle digits) refers to the electrical characteristics of the loaded PCA or the positions of the components on the PCA. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the PCA. If the series code stamped on the PCA does not agree with the series code shown on the title page of this manual, there are differences between your PCA and the PCA described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-10. SPECIFICATIONS.

1-11. Specifications for the line printer interface kit are listed in table 1-1.

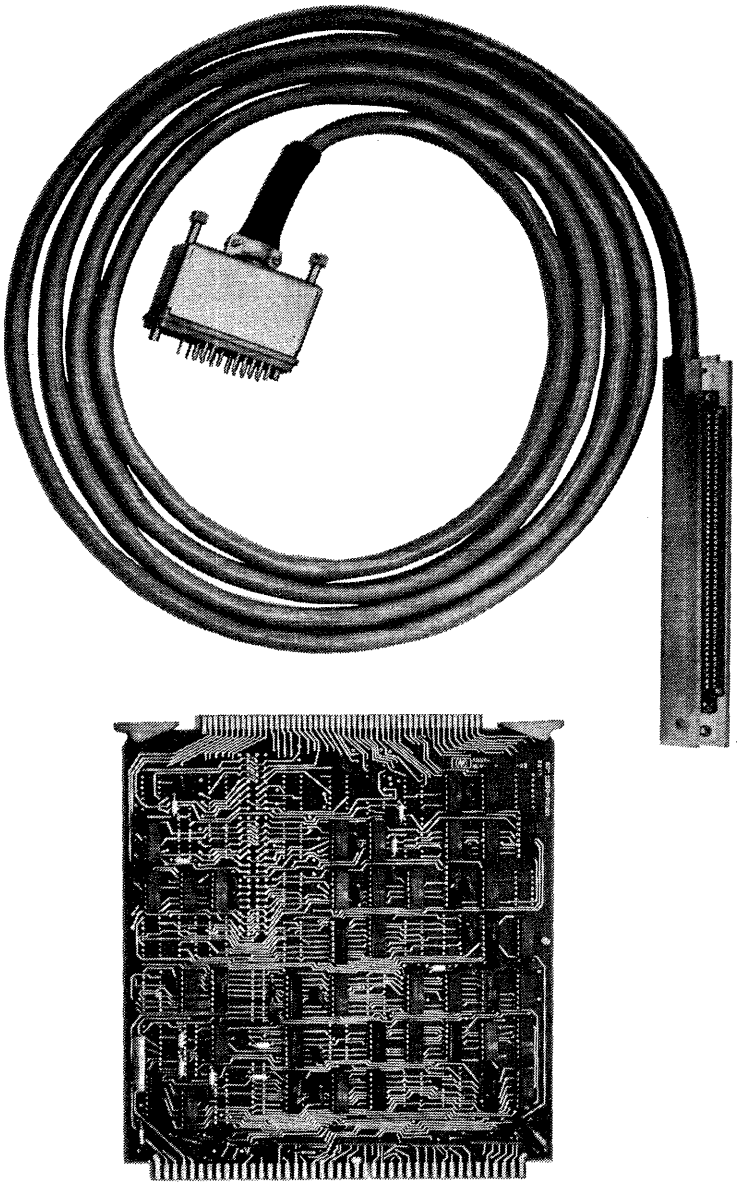

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Figure 1-1. HP 12845A Line Printer Interface Kit

Table 1-1. Interface Kit Specifications

CURRENT REQUIRED FROM COMPUTER:	
+4.5 Volt Supply	1.79 amperes
-2 Volt Supply	0.1 ampere
DATA TRANSFER RATE:	3.0 to 4.7 microseconds per character
TYPE OF CODE USED:	ASCII (7 bits per character)
LOGIC VOLTAGE LEVELS:	
Logic 1:	+2.4 volts dc (minimum)
Logic 0:	+0.4 volts dc (maximum)
CARD DIMENSIONS:	
Width:	7-3/4 inches (196.8 mm)
Height:	8-11/16 inches (220.7 mm)
WEIGHT:	
Net:	7 oz (198 gm)
Shipping:	2 lb (908 gm)

INSTALLATION AND PROGRAMMING

SECTION II

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspection, installation, reshipment, and programming for the HP 12845A Line Printer Interface Kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged kit without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. Before installing the interface PCA in the computer, determine that the additional power consumed by the PCA will not overload the computer power supply. Power requirements of the PCA are given in table 1-1; instructions for calculating available power are given in the applicable computer manual. If sufficient power is available, install the interface kit as follows:

a. Turn off power at the computer and at the line printer.

b. Gain access to the computer card cage and insert the interface PCA into the card slot corresponding to the desired I/O select code.

c. Connect the 100-pin connector (P1) of the interconnecting cable to the 100-pin edge connector of the interface PCA.

Note: In the following step, the cable is routed through the power cord access hole in the line printer. Connection is made to receptacle connector 4J100 on the HP 2614A Line Printer or to receptacle connector 4J109 on the HP 2610A Line Printer.

d. Connect the other end of the cable assembly to the mating connector at the rear of the line printer.

CAUTION

After connecting the cable to the HP 2610A Line Printer, be sure to position the cable to prevent contact with the flywheel of the paper drive motor.

e. Verify proper operation by performing the diagnostic test. Instructions for performing the diagnostic test are contained in Diagnostic Program Procedure, part no. 02100-90130 in the *Manual of Diagnostics*.

2-7. RESHIPMENT.

2-8. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the number of the kit.

2-9. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-10. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthrone, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to assure careful handling.

Note: In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

2-11. PROGRAMMING.

2-12. The following paragraphs provide general information for programming the line printer interface. The information consists of line printer characteristics, computer output, control signals to line printer, control and status signals from line printer, timing, and a sample flowchart. Additional programming information is available in the software manuals supplied with the computer.

2-13. LINE PRINTER CHARACTERISTICS.

2-14. The HP 2610A and HP 2614A Line Printers are similar in operation with the exception of the print rate and paper advance rate. Each of the line printers controls paper movement and printing of a 132-character line by receiving data characters, format characters, and control signals from

the interface PCA. Control and status signals are also sent from the line printer to the interface PCA.

2-15. The line printer accepts ASCII coded data over seven pairs of lines from the interface PCA. Each data character word contains the code for one printed character. The line printer character code set contains 64 characters. The character code set and printer characters are listed in table 2-1.

2-16. The same seven pairs of lines used to transfer data to the line printer are used to transfer a format-control word (seven bits) which controls vertical line spacing. Bits 0 through 6 of the computer output word are decoded by the line printer as an ASCII data character or as a vertical format control word, depending upon the logic state of the control bit (bit 15).

2-17. The format-control punched tape located inside the line printer is used for controlling the format of the line printer paper form and is provided with the line printer. The rectangular perforations in the tape are arranged in eight different patterns or tape levels (see figure 2-1), each causing the line printer paper form to advance a certain number of lines during the paper advance cycle of line printer operation. Format-control codes of $1XX100_8$ through $1XX107_8$ reference tape levels 1 through 8 of the format-control punched tape, respectively, as listed in table 2-2.

2-18. COMPUTER OUTPUT.

2-19. The computer output word is either a data character word or a format-control word as described in paragraphs 2-20 and 2-21.

Table 2-1. Line Printer Character Codes and Symbols

Character Code (Octal)	Character Symbol		Character Code (Octal)	Character Symbol
0 XX 100	@		0 XX 040	(BLANK)
0 XX 101	A		0 XX 041	!
0 XX 102	B		0 XX 042	"
0 XX 103	C		0 XX 043	#
0 XX 104	D		0 XX 044	$
0 XX 105	E		0 XX 045	%
0 XX 106	F		0 XX 046	&
0 XX 107	G		0 XX 047	'
0 XX 110	H		0 XX 050	(
0 XX 111	I		0 XX 051	)
0 XX 112	J		0 XX 052	*
0 XX 113	K		0 XX 053	+
0 XX 114	L		0 XX 054	,
0 XX 115	M		0 XX 055	—
0 XX 116	N		0 XX 056	.
0 XX 117	O		0 XX 057	/
0 XX 120	P		0 XX 060	Ø
0 XX 121	Q		0 XX 061	1
0 XX 122	R		0 XX 062	2
0 XX 123	S		0 XX 063	3
0 XX 124	T		0 XX 064	4
0 XX 125	U		0 XX 065	5
0 XX 126	V		0 XX 066	6
0 XX 127	W		0 XX 067	7
0 XX 130	X		0 XX 070	8
0 XX 131	Y		0 XX 071	9
0 XX 132	Z		0 XX 072	:
0 XX 133	[		0 XX 073	;
0 XX 134	\		0 XX 074	<
0 XX 135	]		0 XX 075	=
0 XX 136	↑		0 XX 076	>
0 XX 137	←		0 XX 077	?

Notes:
1. Bit 15 of the character word must always be a "0".
2. Character symbols shown above do not necessarily indicate line printer drum type-style.

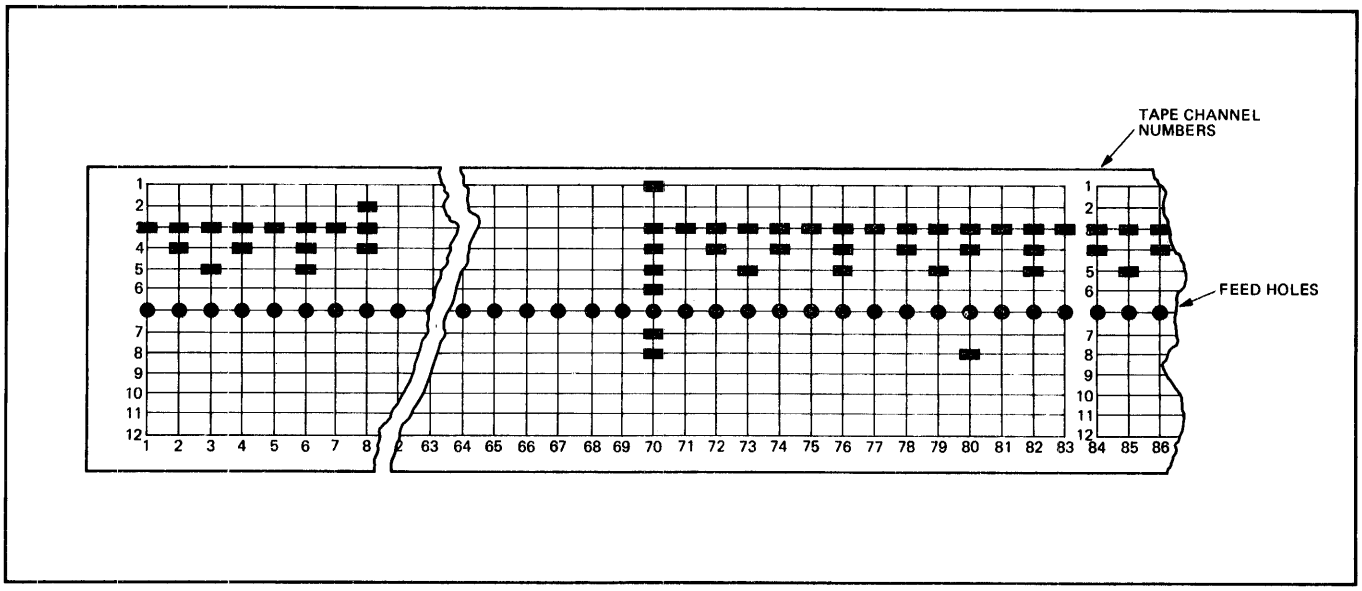

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Figure 2-1. Format-Control Punched Tape

Table 2-2. Format-Control Codes and Functions

Code (Octal)	Function
1XX000	Suppress line advance
1XX001	Advance 1 line
1XX002 thru 1XX077	Advance 2 lines thru Advance 63 lines
1XX100	Select tape channel 1 (skip to top of next form)
1XX101	Select tape channel 2 (skip to bottom of form)
1XX102	Select tape channel 3 (single space)
1XX103	Select tape channel 4 (skip to next double space line)
1XX104	Select tape channel 5 (skip to next triple space line)
1XX105	Select tape channel 6 (skip to next half page line)
1XX106	Select tape channel 7 (skip to next quarter page line)
1XX107	Select tape channel 8 (skip to next sixth page line)

NOTES:

1. Bit 15 of each format word must be a "1".
2. All tape levels have an automatic page-eject function.

2-20. DATA CHARACTER WORD. The data character word from the computer to the line printer is composed of seven data bits (bits 0 through 6) and one definition bit (bit 15). The data bits are programmed to form octal character codes as shown in table 2-1. Each of these codes causes a respective character symbol to be printed onto the line printer paper form during the print cycle of line printer operation. The definition bit (bit 15) defines these seven data bits as a data character code and must be a logic 0. A data character word must be transferred to the line printer for each character symbol in a line of print. The data character word bit format is as shown in figure 2-2.

2-21. FORMAT-CONTROL WORD. The format-control word from the computer to the line printer is composed of seven control bits (bits 0 through 6) and one definition bit (bit 15). The seven control bits are programmed to form octal format-control codes as shown in table 2-2. Format-control codes of 1XX000 through 1XX077 cause the line printer paper form to advance a specified number of lines during the paper advance cycle of line printer operation. Format-control codes of 1XX100 through 1XX107 refer to tape levels 1 through 8, respectively, of the format-control punched tape (refer to paragraph 2-17). Each level of the format-control punched tape causes the paper form to advance a specified number of lines during the paper advance cycle as shown in table 2-2. The definition bit (bit 15) defines the seven data bits of the format-control word as a format-control code and must be a logic 1. A format-control word must be transferred to the line printer following the last character word in each line of point. The bit format for the format-control word is as shown in figure 2-3.

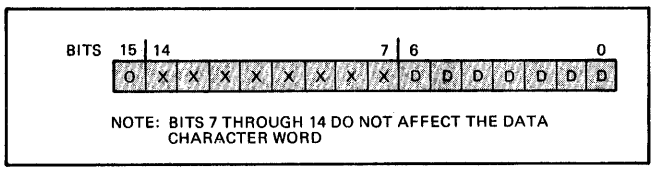

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Figure 2-2. Character Word Format

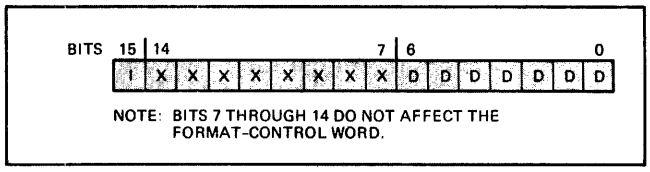

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Figure 2-3. Format-Control Word Format

2-22. CONTROL SIGNALS TO LINE PRINTER.

2-23. Control signals sent from the interface PCA to the line printer are as follows:

a. Information Ready signal.

b. Control Bit signal.

c. Master Clear signal.

2-24. INFORMATION READY SIGNAL. The Information Ready signal is a device command (or data strobe) type of signal. This signal strobes the data lines and Control Bit 15 into the line printer registers. The Information Ready signal occurs once for each data or format character word transferred from the interface PCA to the line printer.

2-25. CONTROL BIT SIGNAL. The Control Bit signal is obtained from bit 15 of the computer output word. A low Control Bit signal informs the line printer that a data character word is on the data lines. A high Control Bit signal informs the line printer that a format character word is on the data lines.

2-26. MASTER CLEAR SIGNAL. The Master Clear signal is triggered by a CRS signal from the computer to the interface PCA. The Master Clear signal restores the line printer circuits to the initial state. The Master Clear signal has a duration greater than 5 microseconds, so the line printer will not be ready for at least 5 microseconds after a CRS signal occurs.

2-27. CONTROL AND STATUS SIGNALS FROM LINE PRINTER.

2-28. Control and status signals sent from the line printer to the interface PCA are as follows:

a. Output Resume signal.

b. Ready signal.

c. Line Ready signal.

d. Paper Out signal.

2-29. OUTPUT RESUME SIGNAL. The Output Resume signal is a device flag type of signal that indicates to the interface PCA that the line printer has accepted the transfer of a data or format character word. This signal occurs in response to an Information Ready signal. The Output Resume signal also sets the Flag Buffer FF and clears the Information Ready FF to return the interface PCA to the initial condition. In addition, the Output Resume signal (in conjunction with the Line Ready signal) controls the logic state of bit 0 (Busy bit) in the input status word to the computer.

2-30. READY SIGNAL. The Ready signal indicates the operational readiness of the line printer to the interface PCA and controls the logic state of bit 15 in the input status word to the computer. The Ready signal is high when power is applied, the START switch is pressed, and no alarm conditions exist in the line printer. Alarm conditions are as follows:

a. Blown hammer driver fuse.

b. Drum gate open.

c. Format gate interlock open.

d. Paper fault condition exists.

e. Printhead voltage dropout.

f. Out of paper condition.

2-31. The paper fault condition is generated by the paper tear switches on the line printer or by a paper runaway. The paper runaway condition must be cleared by a Master Clear signal from the interface PCA or by pressing the START button on the line printer.

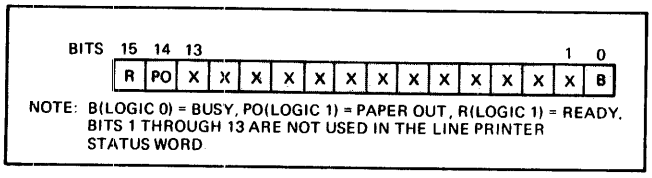
2-32. LINE READY SIGNAL. The Line Ready signal indicates to the interface PCA that the line printer is ready to accept a line of data. This signal initiates an interrupt request on the interface PCA and (in conjunction with the Output Resume signal) controls the logic state of bit 0 (Busy bit) in the input status word to the computer. The Line Ready signal goes low upon loading a format-control word in the line printer registers, and remains low until the conclusion of the print cycle and paper advance.

2-33. PAPER OUT SIGNAL. The Paper Out signal is a status signal which indicates an out of paper or paper tear condition in the line printer. The Paper Out signal controls the logic state of bit 14 in the input status word to the computer. This signal is asserted only when the format tape in the line printer has reached the bottom of form.

2-34. LINE PRINTER STATUS WORD. The bit format for the status word from the line printer to the computer is as shown in figure 2-4.

2-35. TIMING.

2-36. Line printer operation is synchronized through Output Resume and Information Ready signals. The Output Resume signal is initiated by the line printer when it is



2211-13

Figure 2-4. Line Printer Status Word Format

in Ready status and able to accept an input from the interface PCA. The Information Ready signal is initiated on the interface PCA by programming an STC,C instruction with the line printer select code. Information Ready signals are sent to the line printer to indicate when interface PCA outputs are ready to be transferred to the line printer. The interface signal timing diagram is shown in figure 2-5.

2-37. SAMPLE FLOWCHART.

2-38. The sample flowchart shown in figure 2-6 defines the software sequences required of I/O drivers written for the line printer.

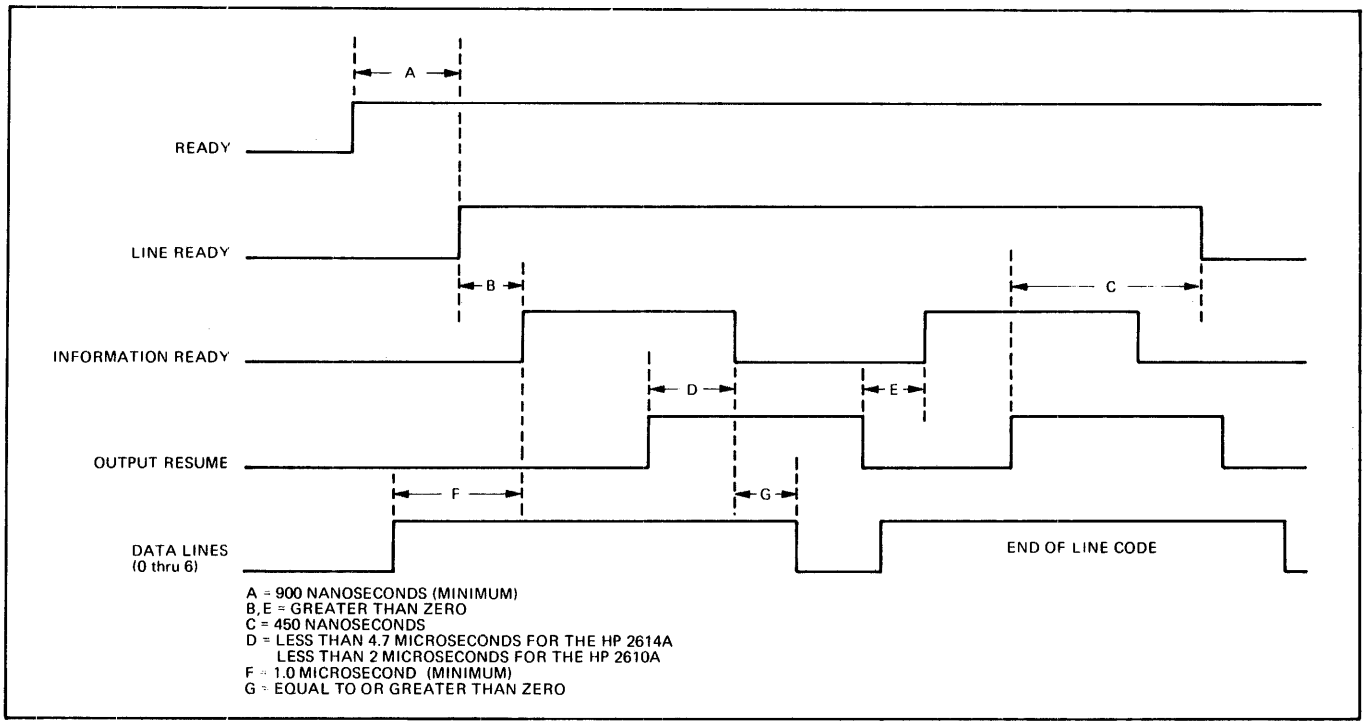


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Figure 2-5. Interface Signal Timing Diagram

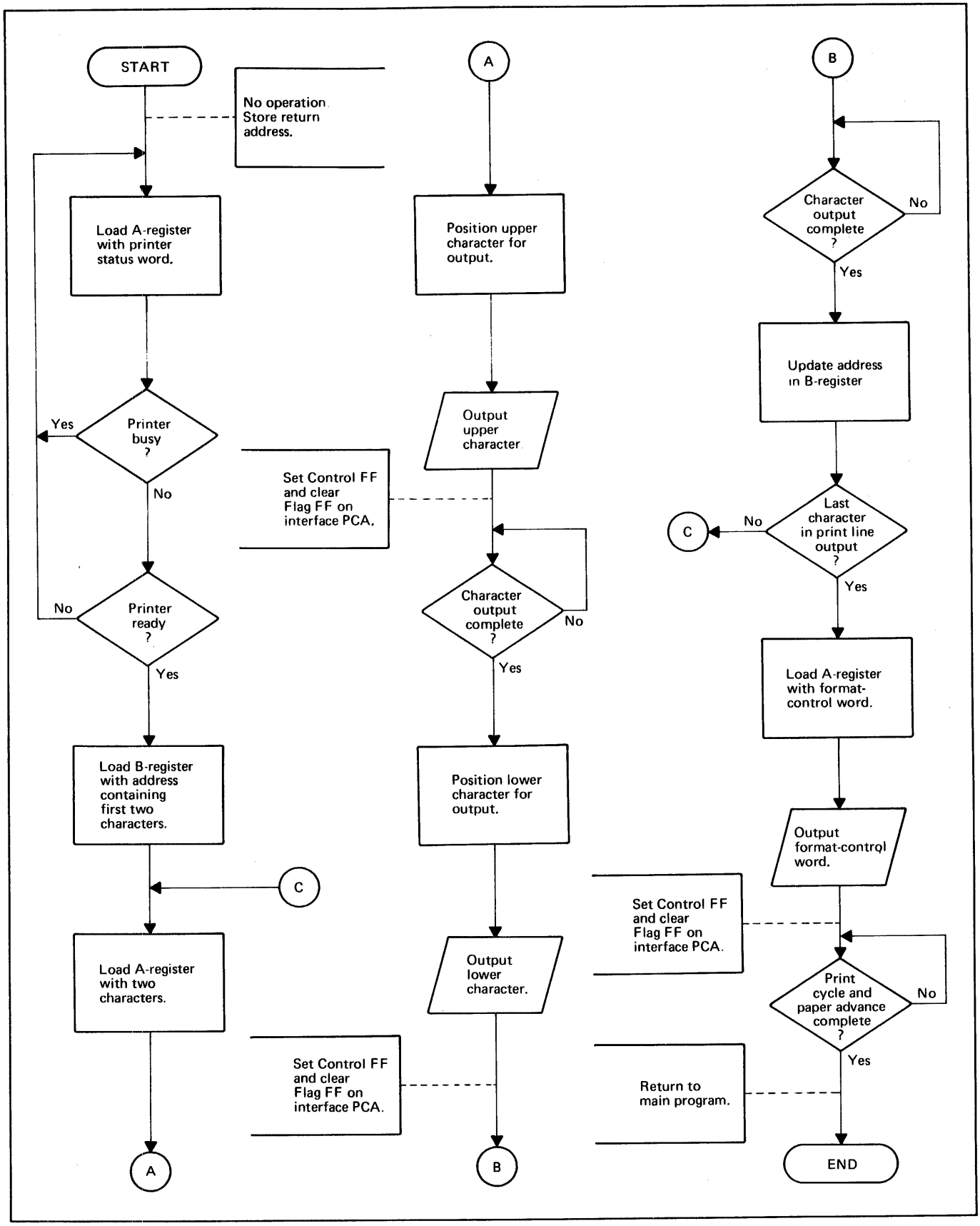

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Figure 2-6. Sample Program Flowchart

SECTION III THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section contains a functional description and a detailed circuit description of the line printer interface PCA. An operational flowchart of the interface PCA is shown in figure 3-2.

3-3. FUNCTIONAL DESCRIPTION.

3-4. The line printer interface PCA contains an output register and the necessary control circuits to transfer data from the computer to the line printer. The interface PCA also contains an input register used to transfer status information from the line printer to the computer. All functions are performed under programmed instructions and result in characters being printed by the line printer. Programmed instructions initiate the control signals that are sent from the computer to the interface PCA as shown in figure 3-1. These control signals enable the interface PCA output register so that data is transferred from the computer to the register. Control signals then initiate an Information Ready signal that is sent from the interface PCA to the line printer. When the line printer is on-line and ready to receive data, it responds to the Information Ready signal by printing.

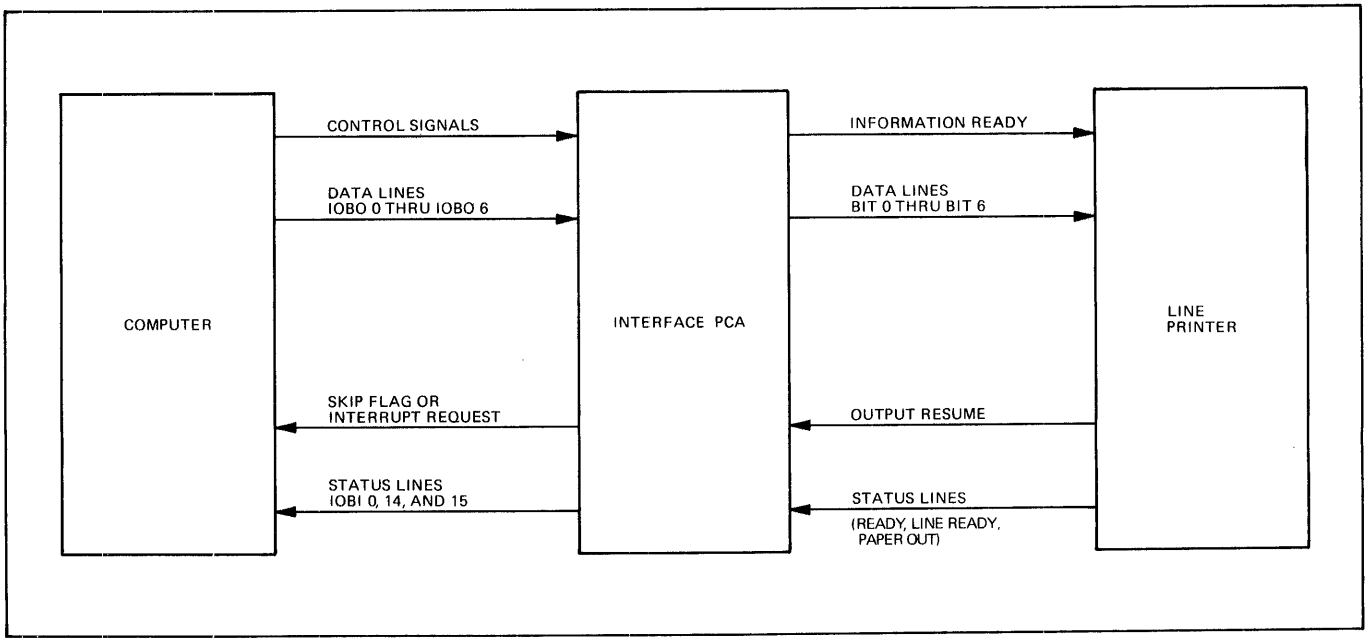
3-5. Data is transferred from the computer to the interface PCA and then to the line printer in seven-bit parallel ASCII. Each data transfer represents one character for printing or a format-control word. As the data or control character is received by the line printer, the line printer stores or processes the data as required and then returns an Output Resume signal to the interface PCA. The Output Resume signal indicates when the line printer is ready to receive more data.

3-6. On the interface PCA, the Output Resume signal initiates either a Skip Flag or Interrupt Request signal depending on the method programmed for data transfer. The initiated signal is then sent to the computer to start the next data transfer. Data transfer continues as long as the computer is programmed to transfer data to the line printer and the line printer remains on-line and ready.

3-7. Line printer status is indicated by three status signals that are sent from the line printer to the interface PCA input register. To read status indications, Control signals are used to enable the input register and send the information to the computer. The signals indicate the line printer ready, paper out, and busy status.

3-8. DETAILED CIRCUIT DESCRIPTION.

3-9. The line printer interface PCA uses circuits that were originally designed for use as a general purpose (universal) interface. These circuits were modified by the



2211-2

Figure 3-1. Interface Signal Flow, Block Diagram

installation of permanent jumpers and the connection of only those circuits required for the operation of the line printer. As a result, some of the circuits are not used in this configuration and are labeled as such in the schematic diagram shown in figure 4-4. The circuits that are used are divided into eight circuit groups, as follows:

a. Turn-on and preset circuit.

b. Select code detector circuit.

c. Flag circuit.

d. Control circuit.

e. Interrupt circuit.

f. Skip flag circuit.

g. Output register.

h. Input register.

3-10. TURN-ON AND PRESET CIRCUIT.

3-11. The turn-on and preset circuit establishes initial conditions for the interface PCA logic circuits. At computer power turn-on or when computer preset is enabled, the computer sends POPIO and CRS signals to the interface PCA. The POPIO signal is inverted to set the Flag Buffer FF which then enables the Flag FF at the next ENF signal (T2). The inverted POPIO signal is also supplied to the output register circuits U12, U24, and U33 to clear the registers. The CRS signal is inverted then processed by one-shot U75B and gate U53 to develop the Master Clear signal. The Master Clear signal is sent to the line printer to clear the controller circuits.

3-12. SELECT CODE DETECTOR CIRCUIT.

3-13. The select code detector circuit enables the line printer interface PCA to accept and perform the instructions intended for the line printer. When the line printer is addressed by programmed instructions, the LSCM and LSCL signal inputs to the interface PCA are both high. (The HSCM and HSCL circuits are not used.) The IOG signal goes high when any instruction is programmed for an I/O device. The LSCM, LSCL, and IOG signals are combined and distributed to the programmed instruction signal input gates, and are combined with the IOO and IOI signals to enable the output registers U12, U24 and U33, and status circuits U54, U65, and U105. Therefore, the LSCM, LSCL, and IOG signals must be high before the interface PCA will accept a programmed instruction, or transfer data or status to the computer.

3-14. FLAG CIRCUIT.

3-15. The flag circuit provides initial conditions that allow the computer to send data to the line printer by either the interrupt or skip flag method. This circuit contains the Flag and Flag Buffer FFs and associated logic circuits. One condition that is required to transfer data is that the Flag FF be set. The Flag FF is always set at the next available T2 of any machine cycle after the Flag Buffer FF is set. Setting the Flag Buffer FF is done by any one of three methods; during power turn-on and preset by the POPIO signal, by programming an STF instruction, and by the Operation Complete signal from one-shot U117A. The Flag and Flag Buffer FFs are both cleared by a CLF instruction and the Flag Buffer FF can also be cleared by an IAK signal from the computer.

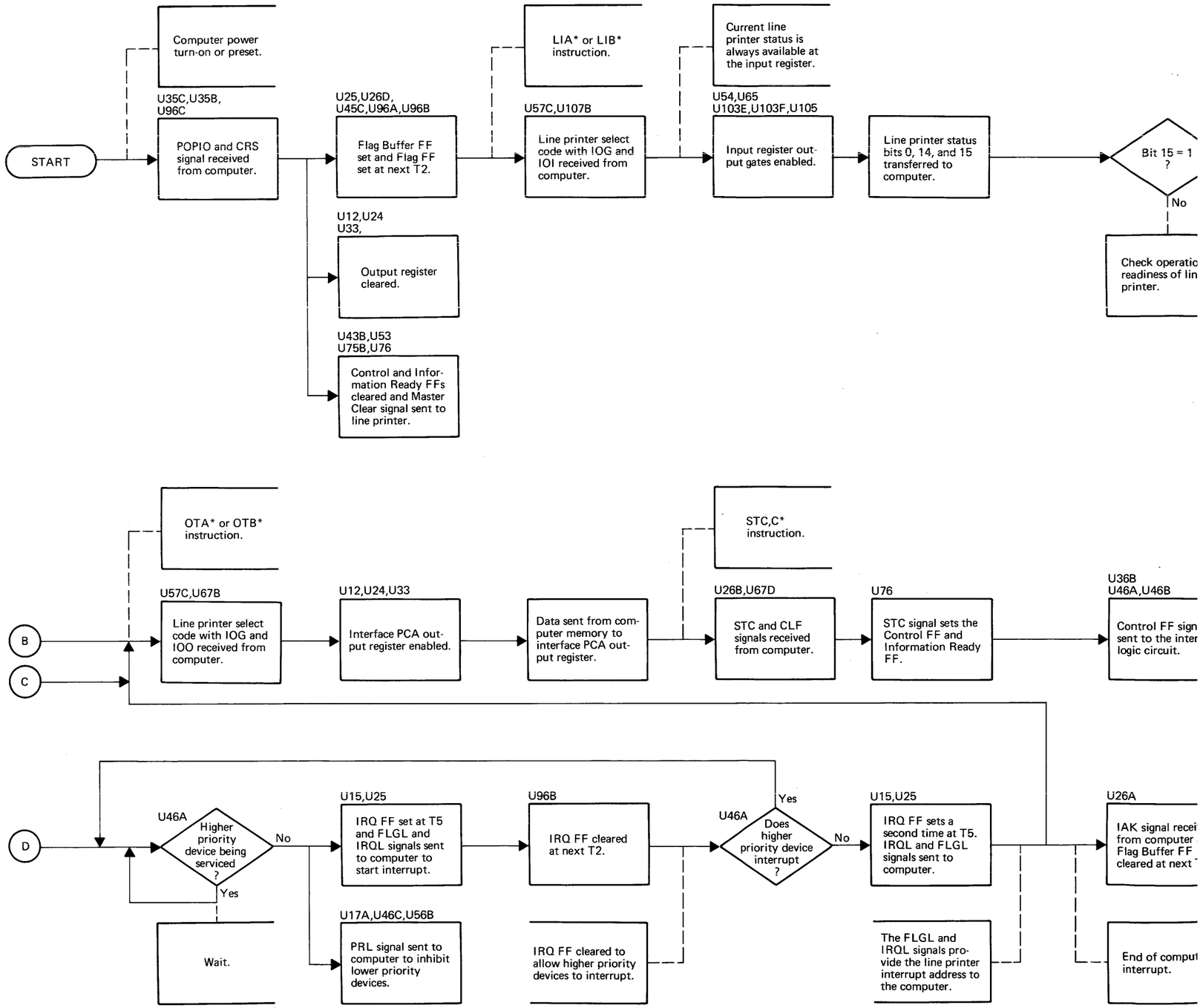
3-16. The line printer sends an Output Resume and a Line Ready signal to differential amplifier circuits on the interface PCA. The outputs of differential amplifiers U112B and U113B are "or-tied" by jumper W7 and supplied to one-shot circuits U117A and U117B. The Output Resume signal indicates when the line printer is ready to accept a data character and the Line Ready signal indicates when the line printer is ready to accept a line of data characters. When the Output Resume signal goes high or the Line Ready signal goes low, the leading edge of the pulse applied to one-shot U117B results in the Command Acknowledge signal which clears the Information Ready FF and the trailing edge applied to one-shot U117A results in the Operation Complete signal which sets the Flag Buffer FF to return the interface PCA to the initial condition.

3-17. CONTROL CIRCUIT.

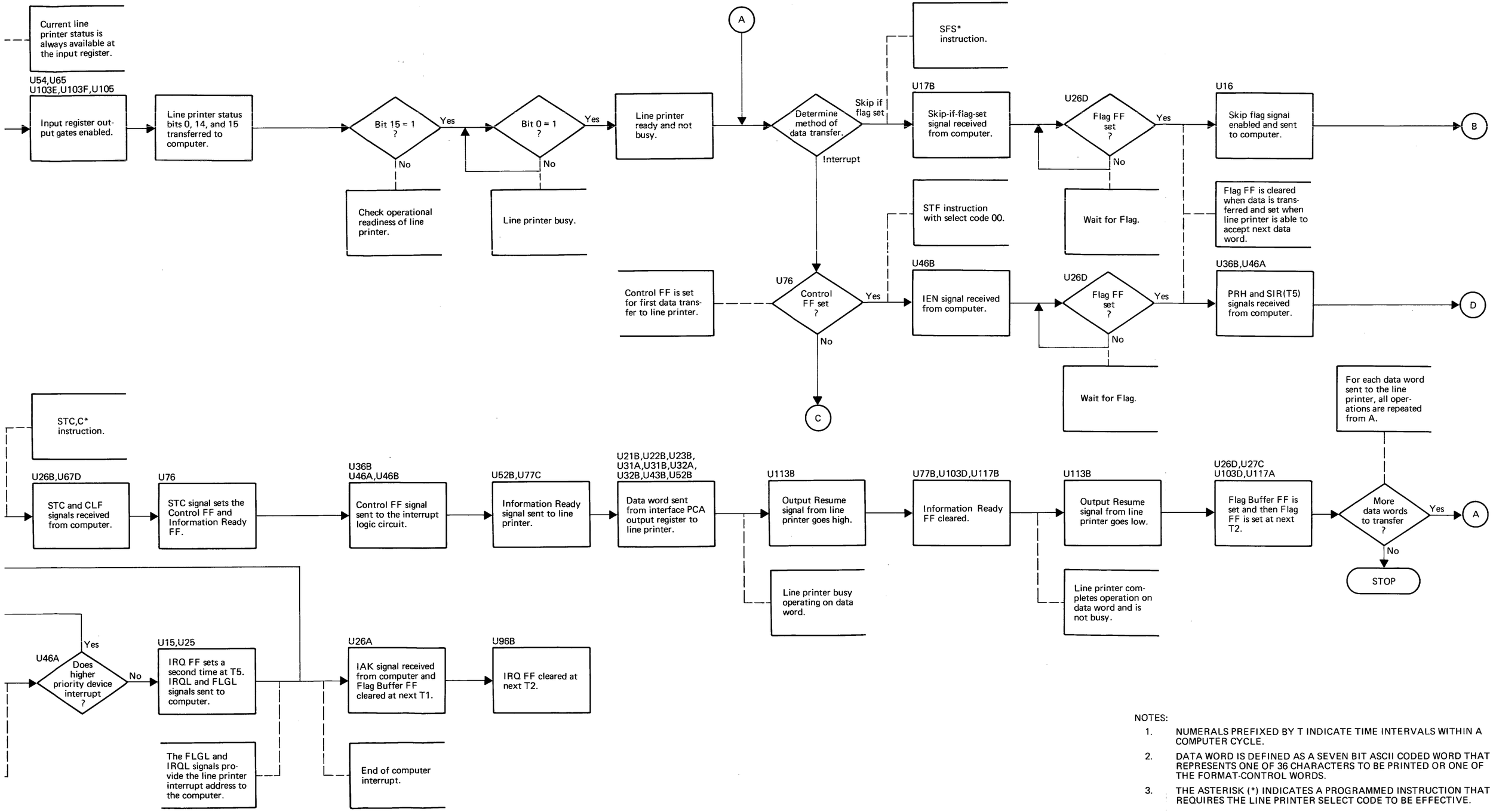
3-18. The control circuit is enabled to signal the line printer that data is available at the interface PCA output registers U12, U24, and U33. The control circuit contains the Control and Information Ready FFs in register U76. Both flip-flops are set by an STC instruction and cleared by a CRS signal or CLC instruction. Normally, the Control FF is set by the first STC instruction to the interface PCA and remains set until a CRS signal or CLC instruction is received. When set, the Control FF provides one condition for enabling the interrupt circuit. When the Information Ready FF is set, the output is sent through gate U77C and differential driver U52B to the line printer.

3-19. INTERRUPT CIRCUIT.

3-20. The interrupt circuit interrupts computer operation on a priority basis. During the interrupt, data is transferred from computer memory to the line printer. The interrupt circuit consists of the IRQ FF in register U25 and associated circuits. Initial conditions are established when the Flag and Control FFs are set and an IEN signal is received to enable gate U46B. An IEN signal is received when an STF instruction is programmed with select code 00. The low output of gate U46B combines with the inverted SIR signal (T5) in gate U36B to send a high signal to gate U46A. The output of gate U46B is also sent to gate U56B. If gate U56B also receives a high PRH signal, indicating that there are no higher priority devices requesting an interrupt, the gate output goes low, sending a PRL signal to all lower priority device interface PCAs. The PRL signal


Computer power turn-on or preset.
U35C,U35B, U96C
START
POPIO and CRS signal received from computer.
U25,U26D, U45C,U96A,U96B
Flag Buffer FF set and Flag FF set at next T2.
U12,U24 U33,
Output register cleared.
U43B,U53 U75B,U76
Control and Information Ready FFs cleared and Master Clear signal sent to line printer.
LIA* or LIB* instruction.
U57C,U107B
Line printer select code with IOG and IOI received from computer.
Current line printer status is always available at the input register.
U54,U65 U103E,U103F,U105
Input register output gates enabled.
Line printer status bits 0, 14, and 15 transferred to computer.
Bit 15 = 1 ?
No
Check operatic readiness of lin printer.
OTA* or OTB* instruction.
U57C,U67B
B
C
Line printer select code with IOG and IOO received from computer.
U12,U24,U33
Interface PCA output register enabled.
Data sent from computer memory to interface PCA output register.
STC,C* instruction.
U26B,U67D
STC and CLF signals received from computer.
U76
STC signal sets the Control FF and Information Ready FF.
U36B U46A,U46B
Control FF sign sent to the inter logic circuit.
D
U46A
Higher priority device being serviced ?
No
Yes
Wait.
U15,U25
IRQ FF set at T5 and FLGL and IRQL signals sent to computer to start interrupt.
U17A,U46C,U56B
PRL signal sent to computer to inhibit lower priority devices.
U96B
IRQ FF cleared at next T2.
IRQ FF cleared to allow higher priority devices to interrupt.
U46A
Does higher priority device interrupt ?
Yes
No
U15,U25
IRQ FF sets a second time at T5. IRQL and FLGL signals sent to computer.
The FLGL and IRQL signals provide the line printer interrupt address to the computer.
U26A
IAK signal recei from computer Flag Buffer FF cleared at next
End of comput interrupt.

2211-10



NOTES:

1. NUMERALS PREFIXED BY T INDICATE TIME INTERVALS WITHIN A COMPUTER CYCLE.
2. DATA WORD IS DEFINED AS A SEVEN BIT ASCII CODED WORD THAT REPRESENTS ONE OF 36 CHARACTERS TO BE PRINTED OR ONE OF THE FORMAT-CONTROL WORDS.
3. THE ASTERISK (*) INDICATES A PROGRAMMED INSTRUCTION THAT REQUIRES THE LINE PRINTER SELECT CODE TO BE EFFECTIVE.

Figure 3-2. Operational Flowchart

inhibits all lower priority interface PCAs from interrupting line printer operation. Gate U46A also receives the PRH signal, a signal from the set-side output of the Flag Buffer FF, and a signal from gate U36B. If all the inputs to gate U46A are high, the output goes low and sets the IRQ FF. Setting the IRQ FF provides FLGL and IRQL output signals. When the IRQ FF is first set, the high FLGL and IRQL signals are sent to the computer to initiate an interrupt.

3-21. At the next time T2, the ENF signal clears the IRQ FF to allow any higher priority device to request service during the interrupt. If no higher priority device requests service, the PRH signal remains high, as do the other inputs to gate U46A, and at time T5, the SIR signal sets the IRQ FF a second time. The FLGL and IRQL signals are then used to indicate the interrupt address.

3-22. The computer sends an IAK signal to the interface PCA to clear the Flag Buffer FF and executes the instruction contained in memory at the interrupt address. At time T2, the ENF signal clears the IRQ FF. Clearing the Flag Buffer FF prevents the IRQ FF from being set again after the requested interrupt is enabled. The Flag FF remains set, however, to maintain the low PRL signal to lower priority devices until processing of the requested interrupt is complete. To clear the Flag FF and enable lower priority devices, a CLF instruction must be programmed.

3-23. SKIP FLAG CIRCUIT.

3-24. The skip flag circuit is used to transfer data from computer memory to the line printer using a non-interrupt method. Before using the non-interrupt method, a CLF instruction is usually issued to select code 00 to disable the IEN signal and ensure that interrupt cannot occur. To enable the skip flag circuit, an SFS or SFC instruction is issued with the line printer select code. With the SFS instruction, the Flag FF must be set to provide a high SKF output signal to the computer. For the SFC instruction, the Flag FF must be cleared to provide a high SKF output signal. The high SKF signal tells the computer that the line printer is ready to receive data. With this method of transferring data, the computer is programmed to wait in a recycling loop before each data transfer until the SKF signal is true.

3-25. OUTPUT REGISTER.

3-26. The output register consists of two 6-bit registers (U12 and U24) and one 4-bit register (U33) as shown in figure 4-4. The output register contains 16 flip-flops, however, only seven (bits 0 through 6) are used for data transfer and one (bit 15) is used for control bit transfer. Data on the register input lines is stored at the low-to-high transition of the Clock line. A low signal on the Clear line will clear the register. Input signals to the registers are applied directly from the computer on the IOBO lines and are applied to the lines by an OTA or OTB instruction. The same instruction causes an IOO signal to be applied to gate U67B. Gate U67B is enabled if the OTA or OTB instruction was addressed with the line printer select code. The data on the IOBO lines is loaded into the output register and transferred through the differential drivers to the line printer. The differential driver type transmission circuits are used to provide high common-mode voltage rejection which prevents noise voltage interference. To read data from the output register, the line printer must receive an Information Ready signal from the interface PCA. Data sent to the line printer is in seven-bit parallel ASCII code with each seven-bit word representing a data character for printing or a format-control character of the format-control word.

3-27. INPUT REGISTER.

3-28. The input register consists of one 6-bit register (U54) and one 4-bit register (U95) as shown in figure 4-4. The input register contains 10 flip-flops, however, only three (bits 0, 14, and 15) are used (for status transfer to the computer). The logic 0 state of IOBI bit 0, and the logic 1 state of IOBI bits 14 and 15 indicates Busy, Paper Out, and Ready status, respectively. Status information is always available at the input register and can be read by the computer by an LIA or LIB instruction with the line printer select code. This instruction develops an IOI signal that is sent through gates U107B, U103E and U103F to enable gates U54A, U65A, and U105A.

3-29. The status signals are sent from the line printer to the input registers through differential amplifier circuits. The Ready and Paper Out status signals are sent through differential amplifiers U63A and U62A, respectively, to input register U64. When these signals are high, the output of the differential amplifiers is high and the IOBI 15 (Ready) and IOBI 14 (Paper Out) bits are in the logic 1 state. When the Line Ready status signal is low or the Output Resume signal is high, the "or-tied" output of differential amplifiers U112B and U113B goes low and the IOBI 0 (Busy) bit is in the logic 0 state. The bit format for the status word is described in paragraph 2-34.

4-1. INTRODUCTION.

4-2. This section contains troubleshooting and diagnostic information for the interface kit. An interconnecting cable diagram, integrated circuit diagrams, a schematic and parts location diagram, and a replaceable parts list are included.

4-3. PREVENTIVE MAINTENANCE.

4-4. Detailed preventive maintenance procedures and schedules are given in the computer system documentation. There are no separate preventive maintenance schedules for the interface kit; however, it is a good practice to remove dust and visually inspect the interface PCA whenever the PCA is removed from the computer.

4-5. DIAGNOSTICS.

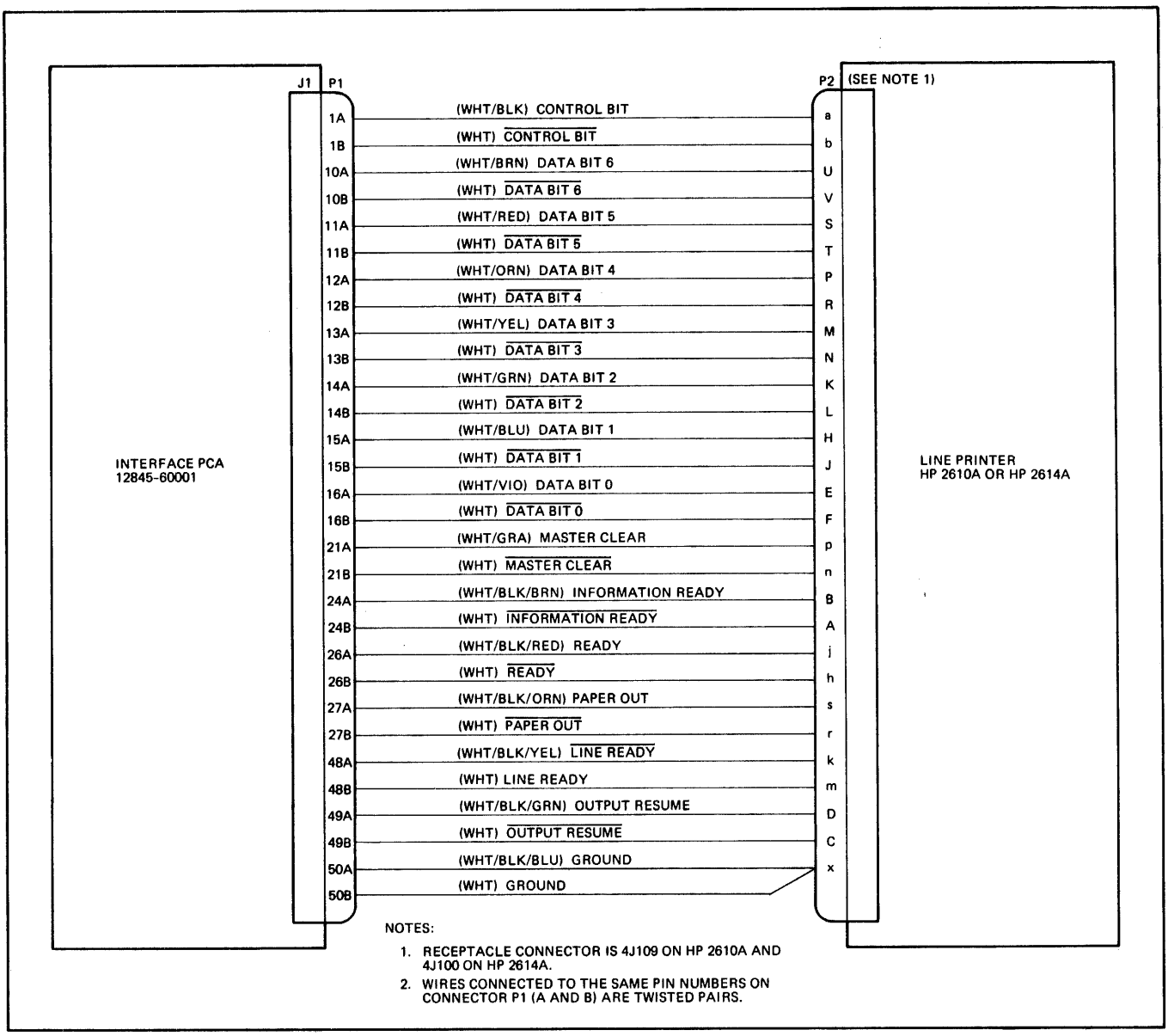
4-6. The interface PCA may be checked using the Diagnostic Operating Procedures, part no. 02100-90130 contained in the *Manual of Diagnostics*. The diagnostic will check the flag, control, and interrupt circuits, and the input and output buffer registers on the interface PCA.

4-7. TROUBLESHOOTING.

4-8. Troubleshooting for the interface PCA is accomplished by performing the tests in the diagnostic program and analyzing any error halts that occur as the test is being run. Continuity checks of the interconnecting cable may be performed by using figure 4-1. To further isolate troubles, refer to the integrated circuit diagrams in figures 4-2 and 4-3 and the parts location and schematic diagrams in figure 4-4. A replaceable parts list, in order of reference designations, is provided in table 4-1.

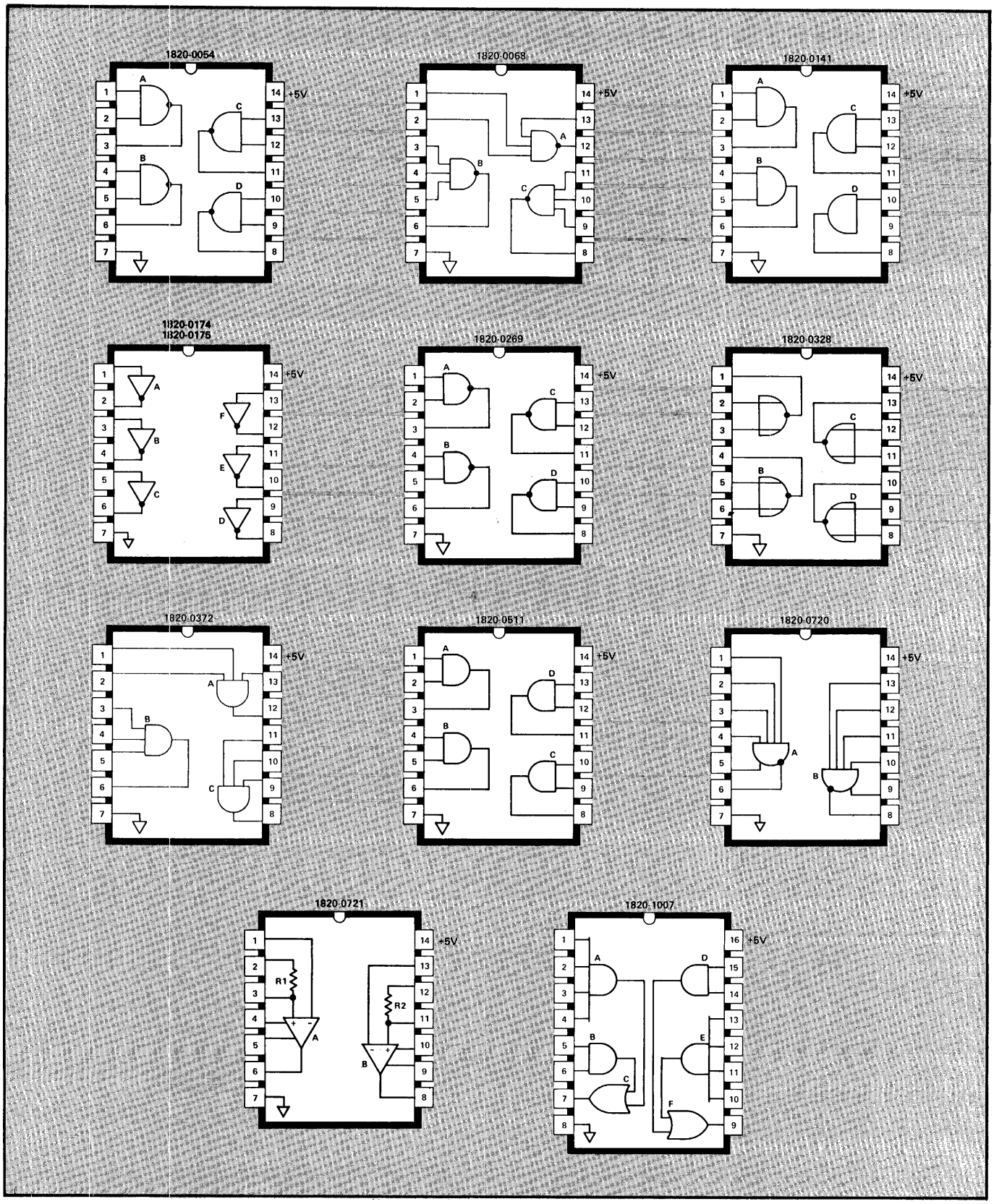
4-9. CABLE ASSEMBLY INTERCONNECTIONS.

4-10. Figure 4-1 shows the cable assembly interconnections between the interface PCA and the line printer. The cable assembly consists of 15 twisted-pair conductors. One of the pairs is a ground interconnection and 14 of the pairs are differential circuits (one signal line of positive polarity and the other of negative polarity). The purpose of the differential circuits is to prevent response to noise pulses that could trigger a single polarity circuit.



2211-7

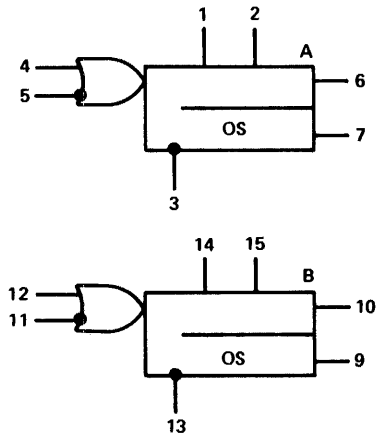
Figure 4-1. Cable Assembly Interconnecting Diagram



2211-8

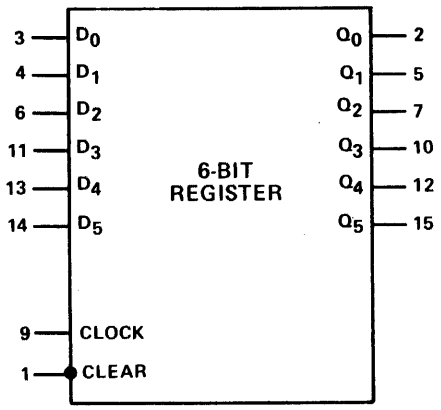
Figure 4-2. Integrated Circuit Logic Diagrams

1820-0515



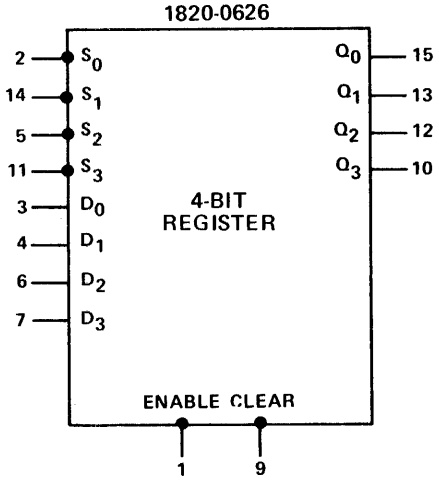
When either input condition is met the one-shot will generate an output pulse. The pulse width is determined by an external RC network. The circuit may be initialized by a low clear input.

1820-0788



Data on the input lines is entered into the register by a positive going transition of the CLOCK line. The register is cleared by a low input on the CLEAR line.

1820-0626

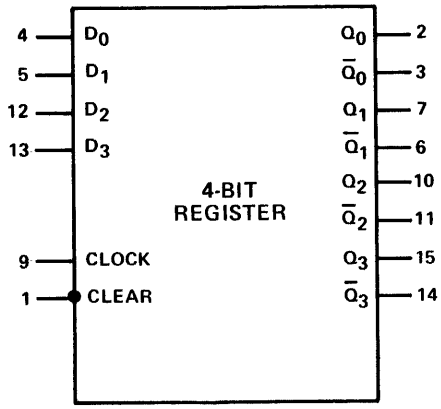


A low input on the ENABLE line allows data on the input lines to set the register. There are two modes of operation, one using the D input lines (most common) and the other using the S input lines.

If the D inputs are used the S inputs are held false. When the ENABLE line is low the register output lines will "follow" the D inputs. When the ENABLE line goes high the register will retain the last set of data inputs.

If the S inputs are used the D inputs are held true. When the ENABLE line is low, a false input on the S line will set the register bit. The register is then cleared by a low signal on the CLEAR line. The CLEAR line serves as a "master" register clear for both the D and S modes of operation.

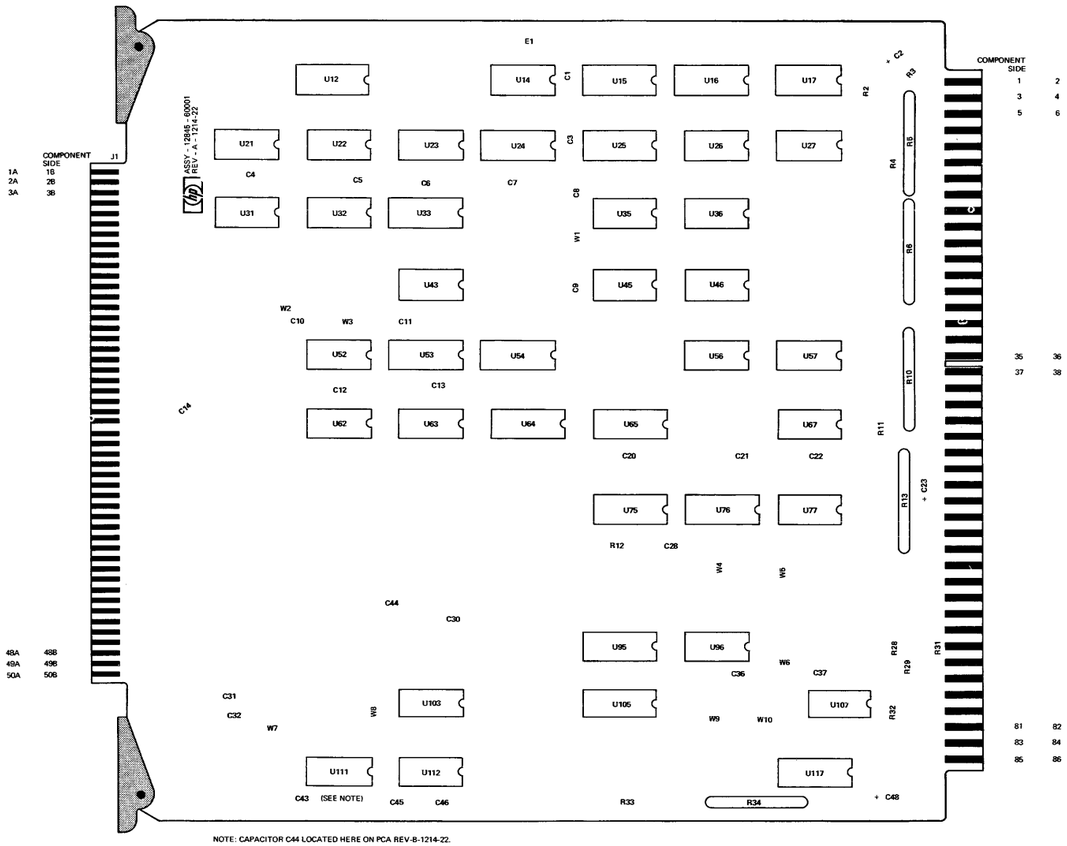
1820-0839



Data on the input lines (D_0 – D_3) is stored at the low-to-high transition of the CLOCK line. A low signal on the CLEAR line will clear the register.

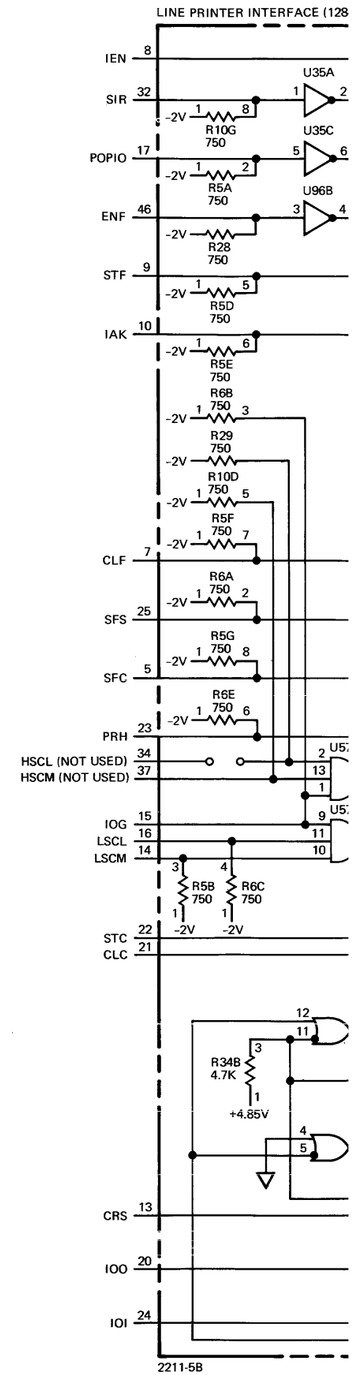
2211-9

Figure 4-3. Integrated Circuit Diagrams and Descriptions



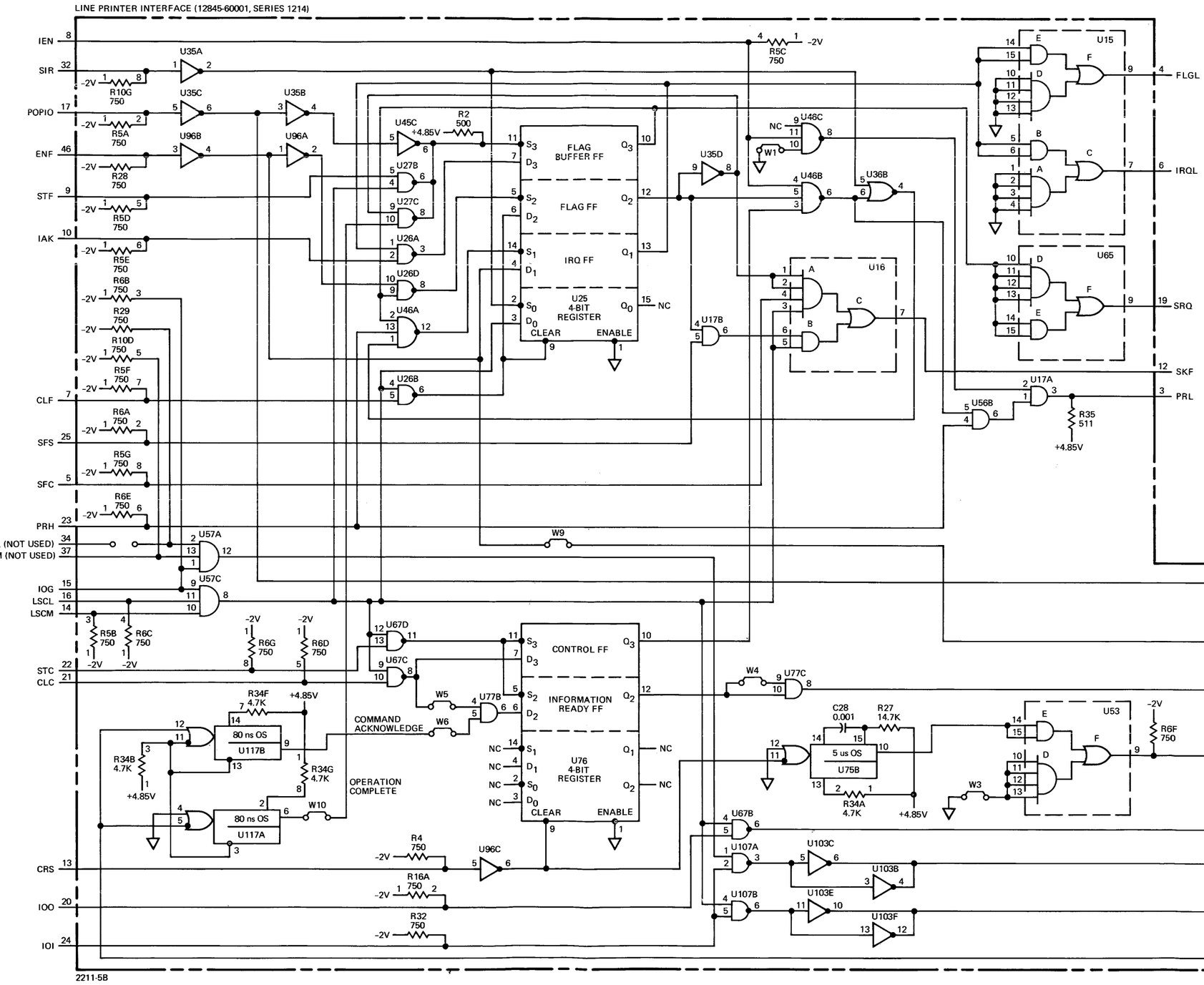
NOTE: CAPACITOR C44 LOCATED HERE ON PCA REV-8-1214-22.

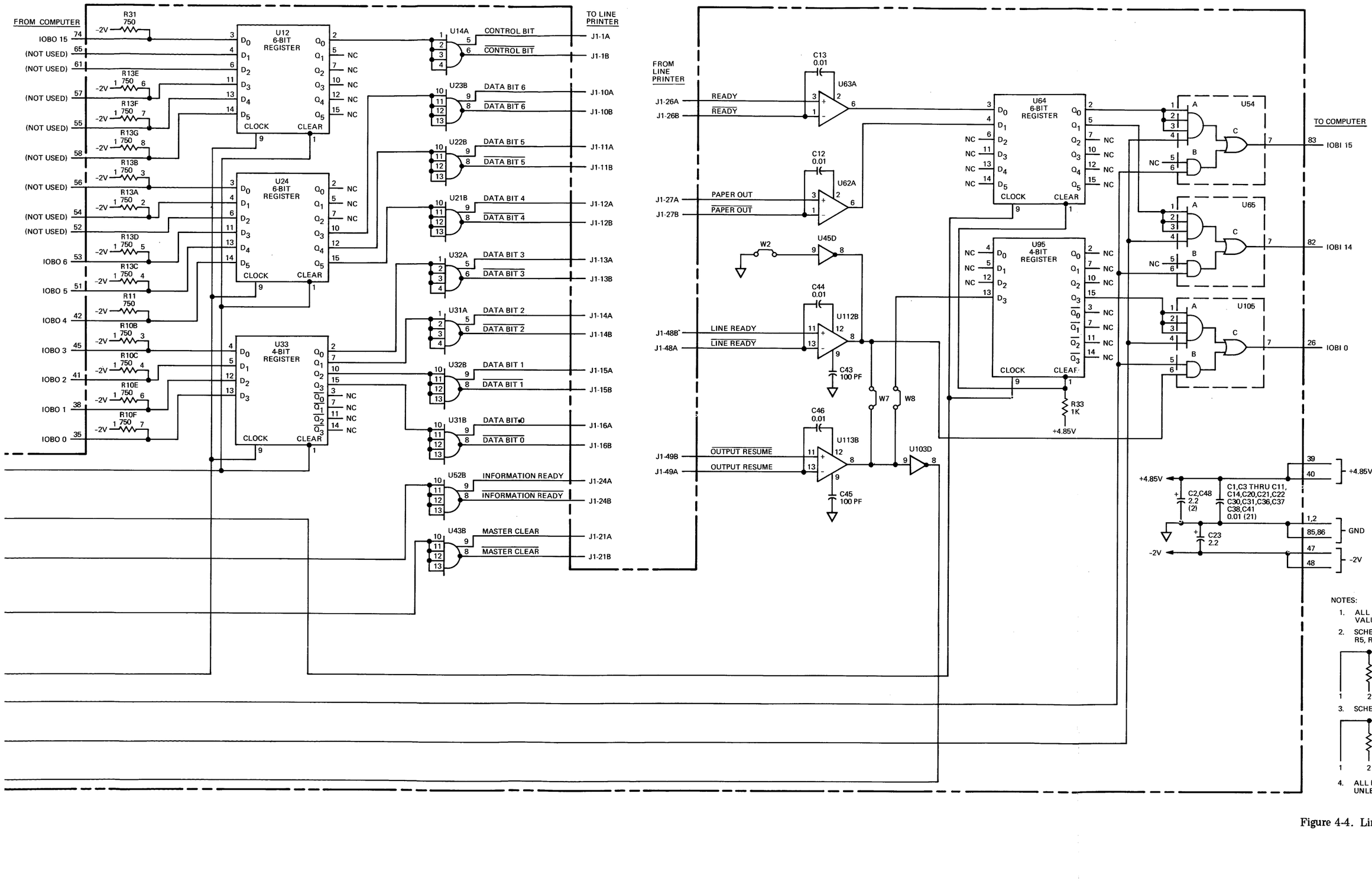
2211-6A



2211-5B

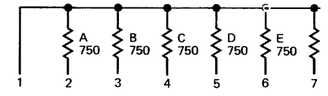
LINE PRINTER INTERFACE (12845-60001, SERIES 1214)



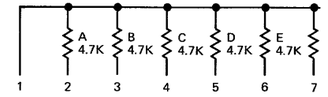


NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS AND VALUES ARE IN UF UNLESS OTHERWISE SPEC
2. SCHEMATIC DIAGRAM FOR RESISTOR NETWO R5, R6, R10, AND R13:

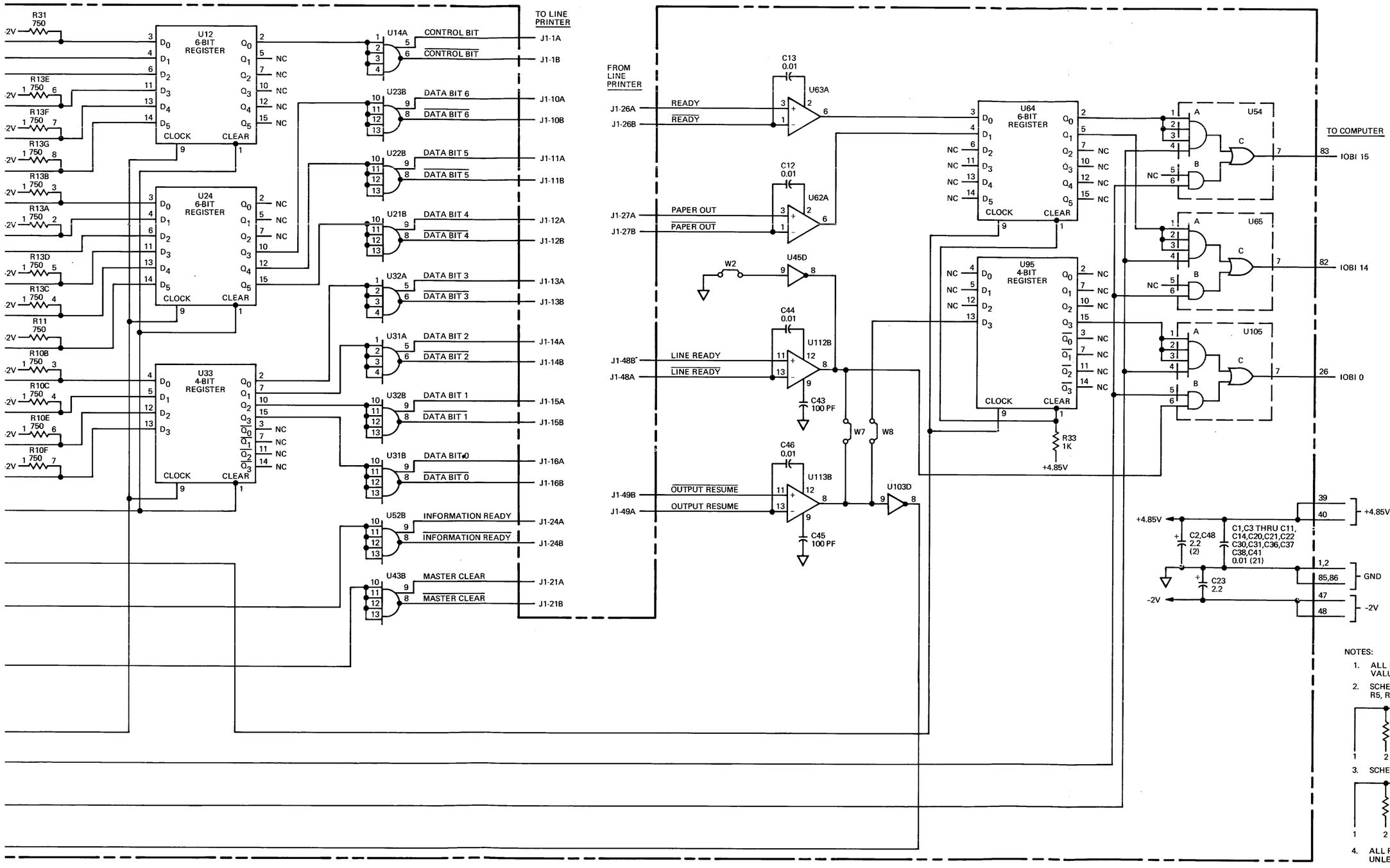


3. SCHEMATIC DIAGRAM FOR RESISTOR NETWO



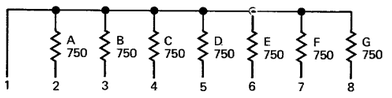
4. ALL PIN NUMBERS REFER TO 86-PIN CONNEC UNLESS OTHERWISE INDICATED.

Figure 4-4. Line Printer Interface PCA, Part and Schematic

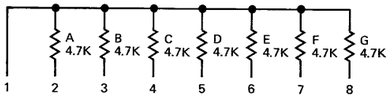


NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN UF UNLESS OTHERWISE SPECIFIED.
2. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R5, R6, R10, AND R13:



3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORK R34:



4. ALL PIN NUMBERS REFER TO 86-PIN CONNECTOR UNLESS OTHERWISE INDICATED.

Figure 4-4. Line Printer Interface PCA, Parts Location and Schematic Diagrams

Table 4-1. Line Printer Interface PCA (12845-60001), Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
	12845-60001	LINE PRINTER INTERFACE PCA	28480	12845-60001
C1,3 thru 14, 20 thru 22,30,31 36 thru 38,41,44,46	0160-2055	CAPACITOR, fxd, cer, 0.01 uF, +80 -20%, 100 Vdcw	56289	C023F101F103ZS22-CD
C2,23,48	0180-0197	CAPACITOR, fxd, elect, 2.2 uF, 10%, 20 Vdcw	56289	105D225X9020A2-DYS
C28	0180-3456	CAPACITOR, fxd, cer, 1000 pF, 10%, 250 Vdcw	56289	C067F251F102KS22-CD
C43,45	0160-0990	CAPACITOR, fxd, mica, 100 pF, 2%, 300 Vdcw	00853	RMD15F101G3S
R2,35	0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416
R4,11,28,29,31,32	0757-0420	RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W	28480	0757-0420
R5,6,10,13	1810-0075	RESISTOR, array, 7 x 750 ohms, 5%, 0.15W each	28480	1810-0075
R12	0698-3156	RESISTOR, fxd, flm, 14.7 ohms, 1%, 1/8W	28480	0698-3156
R33	0757-0280	RESISTOR, fxd, flm, 1k ohms, 1%, 1/8W	28480	0757-0280
R34	1810-0125	RESISTOR NETWORK, 4.7k ohms, 5% (7 resistors)	56289	200C-1858-CRR
U12,24,64	1820-0788	INTEGRATED CIRCUIT, TTL	01295	SN35431
U14,21 thru 23, 31,32,43,52	1820-0720	INTEGRATED CIRCUIT, TTL	27014	DM8830N
U15,16,53,54,65,105	1820-1007	INTEGRATED CIRCUIT, TTL	18324	N8T23B
U17,56	1820-0141	INTEGRATED CIRCUIT, TTL	28480	1820-0141
U25,76	1820-0626	INTEGRATED CIRCUIT, TTL	07263	U7B931459X
U26,67,107	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN74004
U27	1820-0269	INTEGRATED CIRCUIT, TTL	01295	SN7403N
U33,95	1820-0839	INTEGRATED CIRCUIT, TTL	01295	SN35872
U35,96,103	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U36	1820-0328	INTEGRATED CIRCUIT, TTL	04713	SN7402N
U45	1820-0175	INTEGRATED CIRCUIT, TTL	01295	SN7405N
U46	1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N
U57	1820-0372	INTEGRATED CIRCUIT, TTL	01295	SN74H11N
U62,63,112,113	1820-0721	INTEGRATED CIRCUIT, TTL	27014	SD14482
U75,117	1820-0515	INTEGRATED CIRCUIT, TTL	07263	U7B960259X
U77	1820-0511	INTEGRATED CIRCUIT, TTL	01295	SN7408N

REPLACEABLE PARTS

SECTION V

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the HP 12845A Line Printer Interface Kit. Table 5-1 lists parts in alphanumeric order by HP part number and lists the following information for each part.

a. Description of the part. (Refer to table 5-2 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to the list of manufacturers in table 5-3.

c. Manufacturer's part number.

d. Total quantity of each part used in the interface kit.

5-3. A separate parts list is provided along with the parts location view for the interface PCA in section IV of this manual. This parts list presents the parts in alphanumeric order by reference designation.

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Interface kit model number.
b. Printed-circuit assembly series number.
c. Hewlett-Packard part number for each part.
d. Description of each part.
e. Circuit reference designation (if applicable).

Table 5-1. Line Printer Interface Kit, Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0160-0990	CAPACITOR, fxd, mica, 100 pF, 2%, 300 Vdcw	00853	RDM15F101G3S	2
0160-2055	CAPACITOR, fxd, cer, 0.01 uF, +80 -20%, 100 Vdcw	56289	C023101F103ZS22-CD	24
0160-3456	CAPACITOR, fxd, cer, 1000 pF, 10%, 250 Vdcw	56289	C067F251F102KS22-CD	1
0180-0197	CAPACITOR, fxd, elect, 2.2 uF, 10%, 20 Vdcw	56289	150D225X9020A2-DYS	3
0698-3156	RESISTOR, fxd, flm, 14.7 ohms, 1%, 1/8W	28480	0698-3156	1
0757-0280	RESISTOR, fxd, flm, 1k ohms, 1%, 1/8W	28480	0757-0280	1
0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416	2
0757-0420	RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W	28480	0757-0420	6
1810-0075	RESISTOR, array, 7X750 ohms, 5%, 0.15W each	28480	1810-0075	4
1810-0125	RESISTOR NETWORK, 4.7k ohms, 5% (7 fxd resistors)	56289	200C-1858-CRR	1
1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN74004	3
1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N	1
1820-0141	INTEGRATED CIRCUIT, TTL	28480	1820-0141	2
1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N	3
1820-0175	INTEGRATED CIRCUIT, TTL	01295	SN7405N	1
1820-0269	INTEGRATED CIRCUIT, TTL	01295	SN7403N	1
1820-0328	INTEGRATED CIRCUIT, TTL	04713	SN7402N	1
1820-0372	INTEGRATED CIRCUIT, TTL	01295	SN74H11N	1
1820-0511	INTEGRATED CIRCUIT, TTL	01295	SN7408N	1
1820-0515	INTEGRATED CIRCUIT, TTL	07263	U7B960259X	2
1820-0626	INTEGRATED CIRCUIT, TTL	07263	U7B931459X	2
1820-0720	INTEGRATED CIRCUIT, TTL	12040	DM8830N	8
1820-0721	INTEGRATED CIRCUIT, TTL	12040	SD14482	4
1820-0788	INTEGRATED CIRCUIT, TTL	01295	SN35431	3
1820-0839	INTEGRATED CIRCUIT, TTL	01295	SN35872	2
1820-1007	INTEGRATED CIRCUIT, TTL	18324	N8T23B	6
12845-60001	LINE PRINTER INTERFACE PCA	28480	12845-60001	1
12845-60002	CABLE ASSEMBLY	28480	12845-60002	1
18245-90001	OPERATING AND SERVICE MANUAL	28480	12845-90001	1

Table 5-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	MC	= microcircuit	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	P	= plug connector	VR	= voltage regulator
CR	= diode	Q	= semiconductor device other than diode or microcircuit	W	= cable, jumper
DL	= delay line	R	= resistor	X	= socket
DS	= indicator	RT	= thermistor	Y	= crystal
E	= Misc electrical parts	S	= switch	Z	= tuned cavity, network
F	= fuse	T	= transformer		
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	ph	= Phillips head
ac	= alternating current	grn	= green	pk	= peak
ad	= anode			p-p	= peak-to-peak
Al	= aluminum	H	= henries	pt	= point
AR	= as required	Hg	= mercury	PIV	= peak inverse voltage
adj	= adjust	hr	= hour(s)	PNP	= positive-negative-positive
assy	= assembly	Hz	= hertz	PWV	= peak working voltage
		hdw	= hardware	porc	= porcelain
B	= base	hex	= hexagon, hexagonal	posn	= position(s)
bp	= bandpass			pozi	= pozidrive
blk	= black	ID	= inside diameter		
blu	= blue	IF	= intermediate frequency		
brn	= brown	in.	= inch, inches	rf	= radio frequency
brs	= brass	I/O	= input/output	rdh	= round head
Btu	= British thermal unit	int	= internal	rmo	= rack mount only
Be Cu	= beryllium copper	incl	= include(s)	rms	= root-mean-square
		insul	= insulation, insulated	RWV	= reverse working voltage
C	= collector	impgrg	= impregnated	rect	= rectifier
cw	= clockwise	incand	= incandescent	r/min	= revolutions per minute
ccw	= counterclockwise			RTL	= resistor-transistor logic
cer	= ceramic	k	= kilo (10^3), kilohm		
cmo	= cabinet mount only			s	= second
com	= common	lp	= low pass	SB	= slow blow
crt	= cathode-ray tube			Se	= selenium
CTL	= complementary-transistor logic	m	= milli (10^{-3})	Si	= silicon
		M	= mega (10^6), megohm	scr	= silicon controlled rectifier
cath	= cathode	My	= Mylar	sil	= silver
cd pl	= cadmium plate	mfr	= manufacturer	sst	= stainless steel
Comp	= composition	mom	= momentary	stl	= steel
conn	= connector	mtg	= mounting	spcl	= special
compl	= complete	misc	= miscellaneous	spdt	= single-pole, double-throw
		Met Ox	= metal oxide	spst	= single-pole, single-throw
dc	= direct current	mintr	= miniature	semicond	= semiconductor
dr	= drive				
DTL	= diode-transistor logic	n	= nano (10^{-9})	Ta	= tantalum
depc	= deposited carbon	n.c.	= normally closed or no connection	td	= time delay
dpdt	= double-pole, double-throw			Ti	= titanium
dpst	= double-pole, single-throw	Ne	= neon	tgl	= toggle
		no.	= number	thd	= thread
E	= emitter	n.o.	= normally open	tol	= tolerance
ECL	= emitter-coupled logic	np.	= nickel plated	TTL	= transistor transistor logic
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)		
elctlt	= electrolytic			U(μ)	= micro (10^{-6})
		NSR	= not separately replaceable		
F	= farads	NRFR	= not recommended for field replacement	V	= volt(s)
FF	= flip-flop			var	= variable
flh	= flat head			vio	= violet
Flm	= film	OD	= outside diameter	VDCW	= direct current working volts
Fxd	= fixed	OBD	= order by description		
filh	= fillister head	orn	= orange	W	= watts
		ovh	= oval head	WW	= wirewound
G	= giga (10^9)	oxd	= oxide	wht	= white
Ge	= germanium			WIV	= working inverse voltage
gl	= glass	p	= pico (10^{-12})		
gnd	= ground(ed)	PC	= printed circuit	yel	= yellow

Table 5-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their latest supplements.

Code No.	Manufacturers	Address
00853	Sangamo Electric Co., Pickens Div.	Pickens, S.C.
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas
04713	Motorola Inc. Semiconductor Prod. Div.	Phoenix, Arizona
07263	Fairchild Camera & Inst. Corp., Semiconductor Div.	Mountain View, Cal.
12040	National Semiconductor Corp.	Danbury, Conn.
18324	Signetics Corp.	Sunnyvale, Cal.
28480	Hewlett-Packard Co.	Palo Alto, Cal.
56289	Sprague Electric Co.	North Adams, Mass.

HEWLETT PACKARD

CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

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