64000

HP64000 Logic Development System

Model 64271A General Purpose Control Card

HEWLETT PACKARD

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Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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Service Manual
General Purpose Control Card
64271-90902, November 1983

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3. The information in this book is easy to find:

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SERVICE MANUAL

MODEL 64271A
GENERAL PURPOSE CONTROL CARD

REPAIR NUMBERS

This manual applies to **64271A Emulators** with a repair number prefix of **2124A**. For further information on repair numbers refer to "Instruments Covered by This Manual" in Section I.

Manual Part No. 64271-90902

PRINTED: NOVEMBER 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

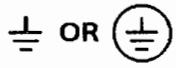
Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

General Definitions of Safety Symbols Used on Equipment or in Manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

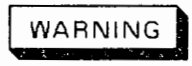
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).



The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

PRINTING HISTORY

Each new edition of this manual incorporates all material updated since the previous edition. Manual change sheets are issued between editions, allowing you to correct or insert information in the current edition.

The part number on the back cover changes only when each new edition is published. Minor corrections or additions may be made as the manual is reprinted between editions.

First Edition..... June 1981 (P/N 64271-90901)
Second Edition.....November 1983 (P/N 64271-90902)

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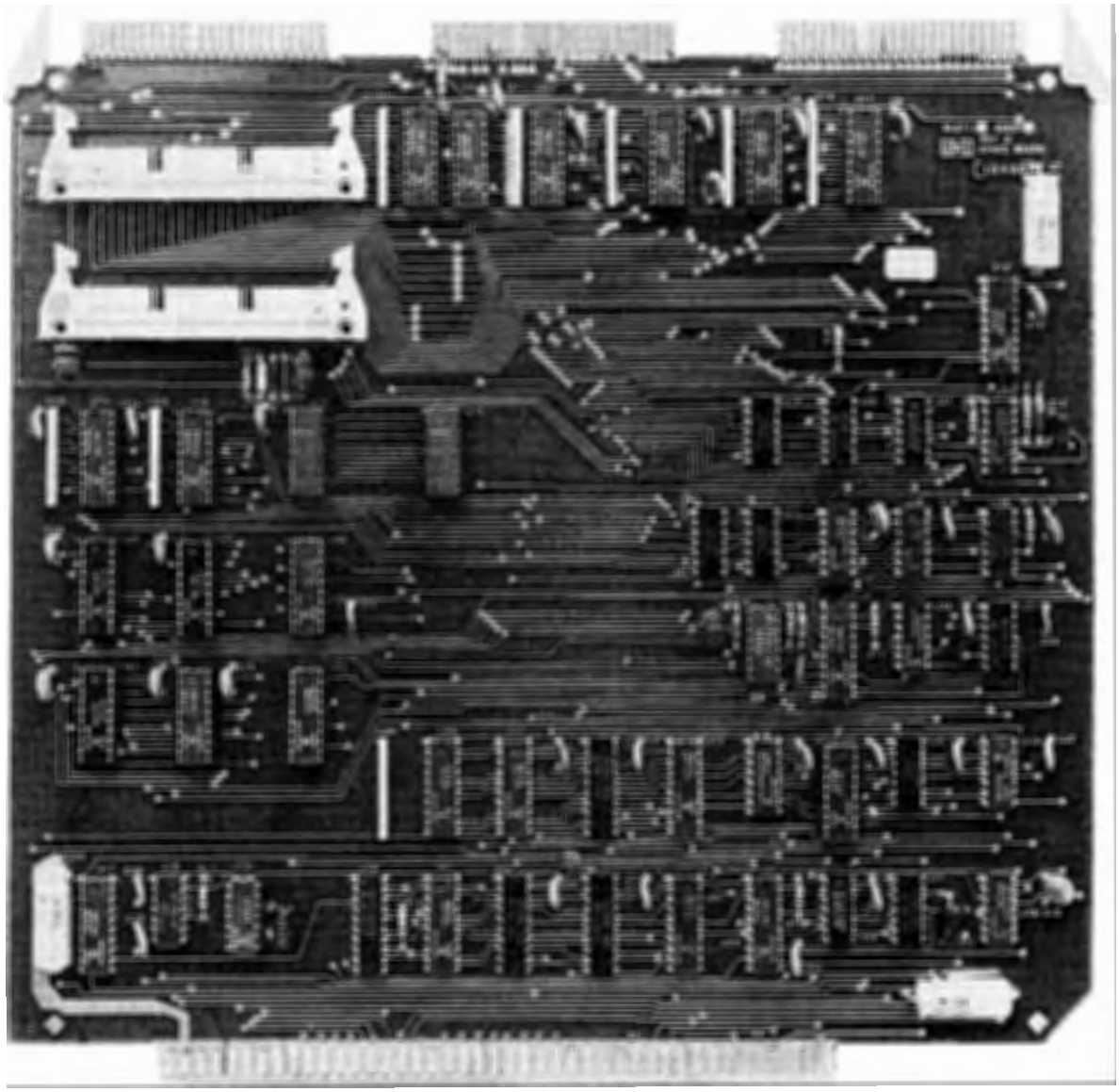


Figure 1-1. 64271A General Purpose Control Card

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Abbreviated Service Manual contains installation information, parts lists, component locators, and schematics for the 64271A General Purpose Control Card. It does not contain information for operating or servicing the 64271A. Refer to the applicable Emulation Subsystem manuals for information on operation and troubleshooting.

1-3. Shown on the title page is a microfiche part number. This number can be used to order 4X6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. ORGANIZATION.

1-5. This manual is organized into eight sections:

Section I, General Information, contains information regarding manual applicability, instrument usage, instrument characteristics, and equipment requirements.

Section II, Installation, explains how to unpack and install the Model 64271A; it also gives information on environmental limits of operation, and packing instructions should the 64271A ever need to be shipped.

Section III, Operation, refers the user to the proper manuals for operation of the 64271A in an emulation system.

Section IV, Performance Verification, describes how to run the option_test Performance Verification procedures for the 64271A board only; and indicates general methods for troubleshooting failures during these verification procedures.

Section V, Adjustments, normally contains calibration information; however, this section is blank since the 64271A requires no parametric adjustments.

Section VI, Replaceable Parts, contains information for ordering spare parts, along with parts lists for the 64271A board and diagrams showing the correspondence between the physical location of the part on the 64271A and the reference designator.

Section VII, Manual Changes, normally contains information required to modify the manual for other versions of the 64271A. However, no major electrical or functional changes have been made to the 64271A since its introduction; therefore, this section is blank.

Section VIII, Service, contains reference information for servicing a defective 64271A, including block diagrams, schematics, component locators, and theory of operation. A complete list of signal names (mnemonics) is also included here, with definitions of each signal's function provided.

1-6. INSTRUMENTS COVERED BY THIS MANUAL.

1-7. Attached to the 64271A is a repair number tag. The repair number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the prefix and the last five are the suffix. The prefix is the same for all identical General Purpose Control Cards; it only changes when a change is made to the card. The suffix is assigned sequentially and is different for each General Purpose Control Card. This manual applies to those 64271A's with repair number prefixes listed on the title page.

1-8. 64271A's manufactured after the printing of this manual may have a repair number not listed on the title page. The manual for the newer General Purpose Control Card will be accompanied by a yellow manual change supplement. The supplement explains how to adapt the manual to the newer 64271A.

1-9. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and as accurate as possible, Hewlett-Packard recommends that you periodically request the latest manual changes supplement. The supplement is identified by the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard Sales/Service office.

1-10. DESCRIPTION.

1-11. EMULATION OVERVIEW.

1-12. Refer to Figure 1-2, which is a basic block diagram of the emulation subsystem. The shaded portion is the area occupied by the Model 64271A General Purpose Control Board. The emulator may be used without a target system by developing software on the 64000 development stations via the editor and relocatable linker utilities; then this software may be uploaded into the emulation memory modules and executed by the emulation processor within the emulation pod. Analysis of software execution is also available. Note that the emulation processor transmits address information and transmits or receives data information to and from emulation memory and analysis via the emulation bus; this allows the processor to run at full speed without having to share the resources of the development station CPU bus.

1-13. The user probe of the emulator may also be inserted into the space which would be occupied by the microprocessor in a user's target system. The probe will then emulate the actions of that processor inserted into the system, with the added benefits of being able to access both the user's memory or emulation memory in any combination, plus allowing real-time analysis of software execution.

1-14. GP CONTROL BOARD.

1-15. The 64271A General Purpose Control Board performs the interface functions between the emulator pod, the emulation system, and the mainframe CPU. See Figure 1-3.

1-16. Last Address and Break Logic. Pod address HEA 0-23 is buffered to the emulation bus and the last address latches by address buffers. The last address latches are loaded on a low-to-high transition on the SETLAS line. If an emulation break (LBREAK) or a mainframe break (LBPCBRK) occurs, BRK is asserted. This causes an interrupt or break to be sent to the pod, and also allows the last address latches to hold the break address.

1-17. Ready Mapper. The ready mapper determines whether the current address on the pod bus (HEA 0-23) is within space mapped to user or emulation (mainframe) memory. Output from the mapper are two signals which are identical in logic function but have different uses. They are:

a. LUSER-- Output to the pod. When low, current address is within space mapped to user memory.

b. PREADY-- Internal use on control board. Used by the wait state generator and also used to enable the correct data buffers for a data transaction.

The mapper is programmed during the emulation defib (reset) mode.

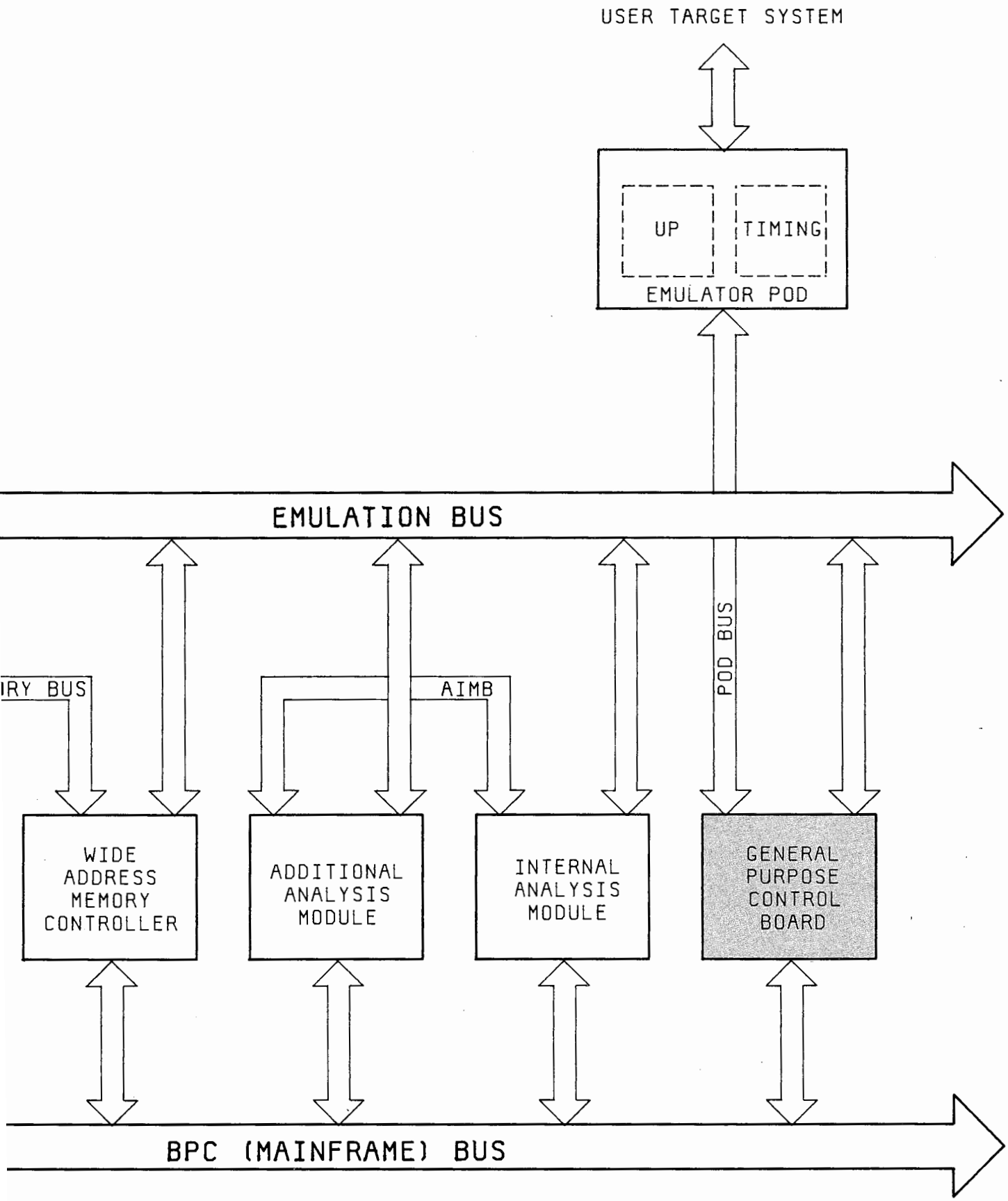
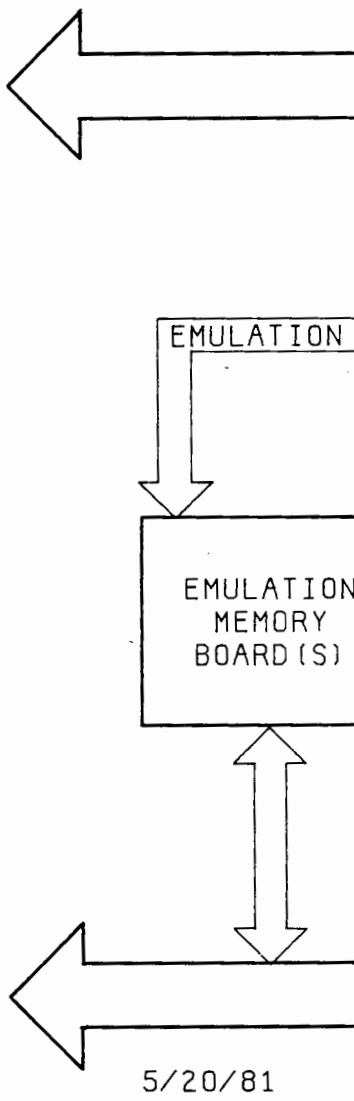
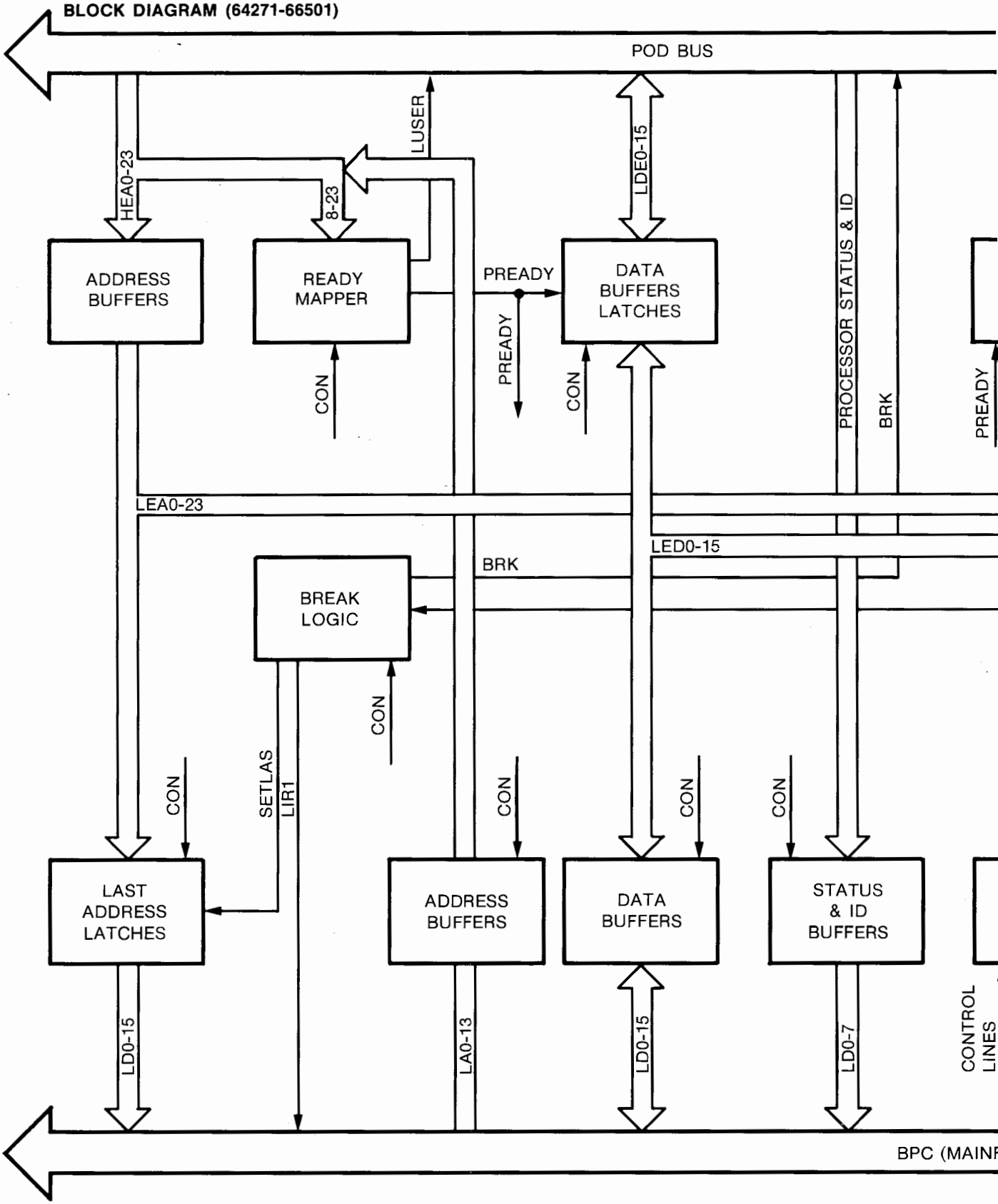


Figure 1-2.
Emulation Subsystem Block Diagram


EMULATION
EMULATION
MEMORY
BOARD(S)
5/20/81

BLOCK DIAGRAM (64271-66501)



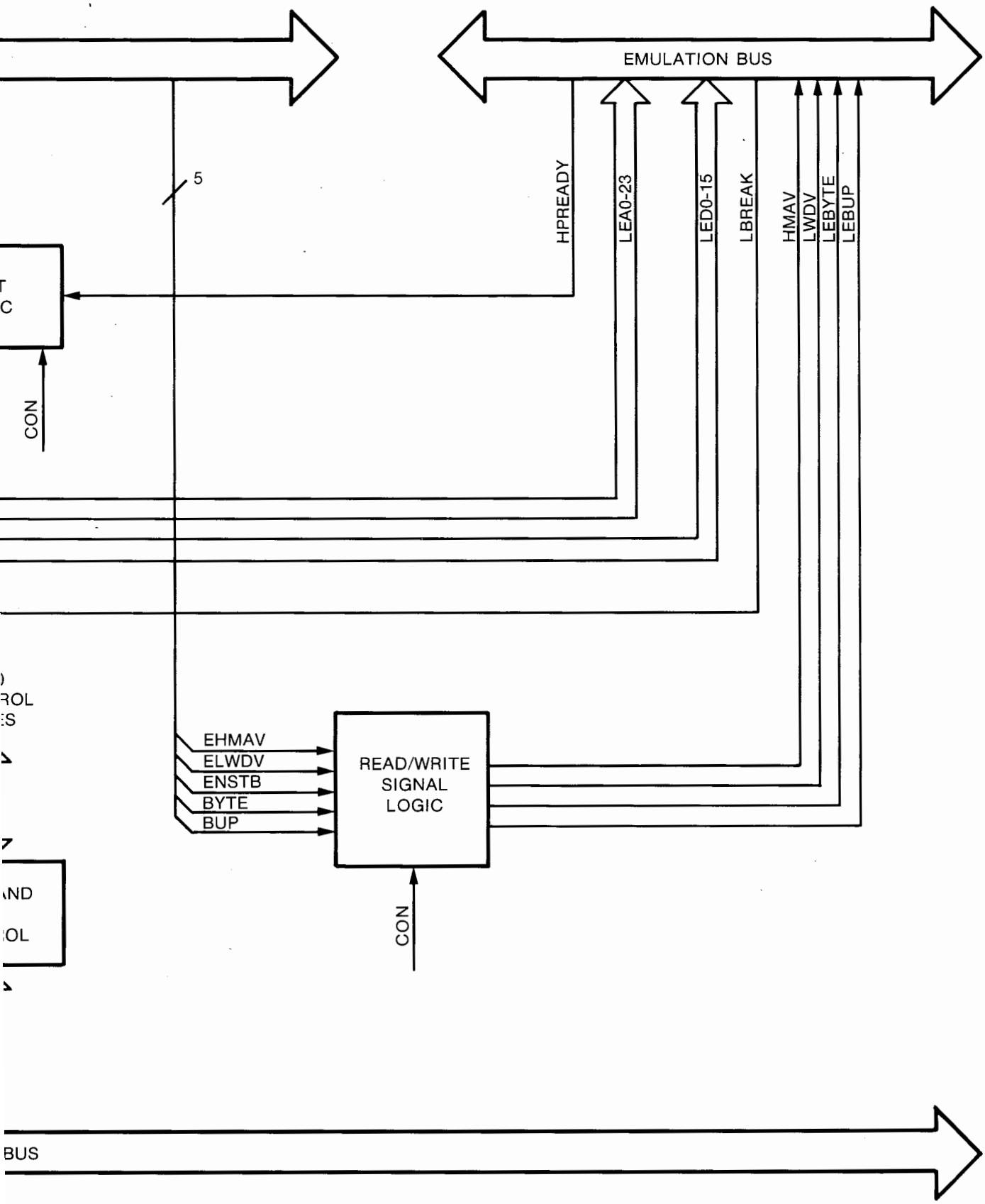


Figure 1-3. GP Control Board Block Diagram

1-18. Three Port Data Bus. Three separate data buses are used on the 64271A. They are:

a. Mainframe (mainframe CPU) data bus.

b. Pod data bus.

c. Emulation data bus.

The data bus enabling logic uses ready mapper signal PREADY and various signal lines from the command & control logic to determine which buffers to enable or disable for the data transaction.

1-19. Status and ID Buffers. The status buffer is used to gate emulation processor status onto the mainframe data bus. Also included is an ID (identification) buffer which, when enabled, tells the mainframe which emulator pod is connected to the control board, as well as identifying the control board itself.

1-20. Wait Logic. The wait logic functions as a programmable wait state generator, using PREADY (ready mapper), HPREADY (emulation memory controller), and various control lines to determine whether to insert wait states or acknowledges into the current memory cycle.

1-21. Command and Control. This section uses the mainframe data bus, address lines LA 12 & 13, and certain mainframe control lines to determine which functions are selected on the 64271A.

1-22. Read/Write Signal Logic. This section includes logic for:

a. Determining whether or not memory is being accessed (HMAV).

b. Inserting a delay into the ELWDV (Emulator Low Write Data Valid) line.

c. Determining polarity and function of the BYTE and BUP lines, which are used to enable lower and upper byte banks of memory.

1-23. ADDITIONAL EQUIPMENT REQUIRED.

1-24. The Model 64271A must be plugged into a 64000 mainframe to operate. It must also be connected to an in-circuit emulation pod and a wide address memory controller with at least 8K of memory to have a minimum emulation subsystem.

1-25. POWER SUPPLY LOADS.

1-26. Power supplies used by the 64271A and current draws are as follows:

+5 V -- Draws 3.1A
-5 V -- Routed to pods via the GP board, not used on board.
+12 V -- Routed to pods via the GP board, not used on board.
-12 V -- Not used.
+17 V -- Not used.
+40 V -- Not used.
-3 V -- Not used.

1-27. The current drawn by the selected Emulator Pod must be added to that of the 64271A to determine the current drawn by the combination.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information necessary to install the Model 64271A in the Model 64100A mainframe. Also included is information concerning initial inspection, damage claims, environmental considerations, storage and shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents have been checked for completeness and the 64271A has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the 64271A does not pass performance verification, notify the nearest Hewlett-Packard office. If the shipping container or cushioning material is damaged, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. INSTALLATION.

2-6. Figure 2-1 shows a top view of the 64100A mainframe card cage. The recommended card slot for the 64271A is the rearmost one, as this will maximize free cable length outside the mainframe to the in-circuit emulation pod.

WARNING

Read the Safety Summary at the front of this manual before installing the 64271A.

2-7. To install the 64271A, proceed as follows:

a. Turn off power to the 64100 station.

CAUTION

Power to the 64000 development station must be removed before installation or removal of option cards (emulation, etc.) to avoid damage to the option cards and the development station.

b. Loosen the two hold-down screws and remove the card cage access cover (64100A). (Refer to the 64110A Mainframe Service Manual for information on removing the card cage access cover of a 64110A.)

c. If you are installing the 64271A in a 64100A development station along with an emulator pod that uses a shielded cable assembly, verify that the RFI Ground Bracket (item 7 in Figure 2-3) has been installed in the mainframe as shown in Figure 2-4. If it has not been installed, go to the paragraphs entitled "RFI Ground Bracket Installation" in this section to install the bracket. After installation, proceed with step d.

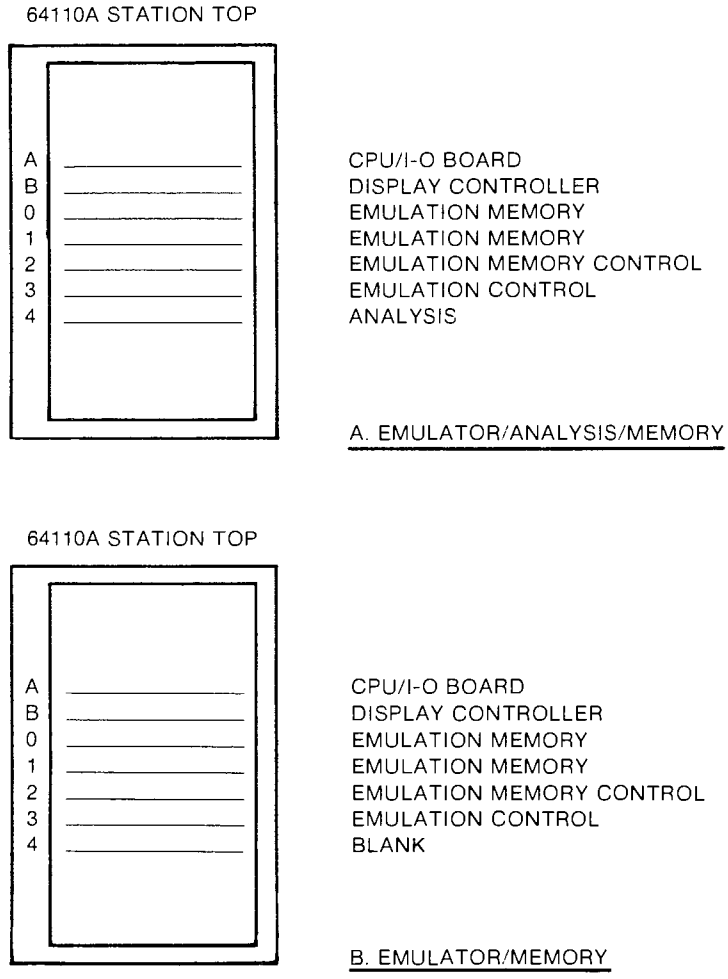


Figure 2-2. 64110A Card Cage Configuration

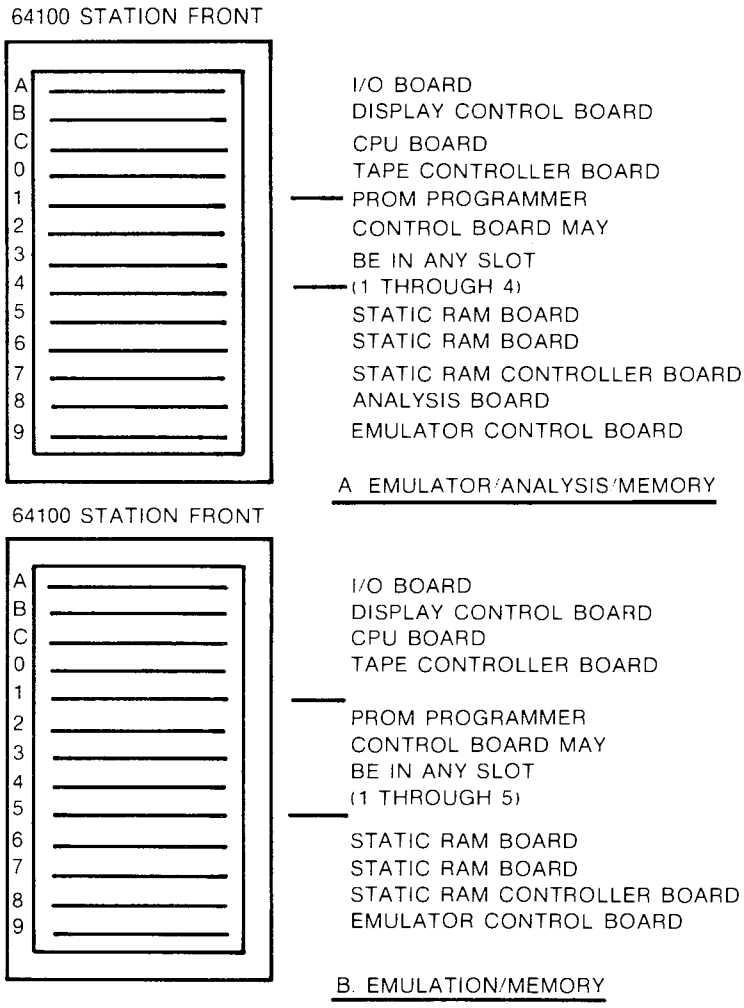


Figure 2-1. 64100A Card Cage Configuration

and on into the RFI ground bracket. Attach a nut (item 5) to the free end of the screw (inside the top cover of the development station at this point) and tighten firmly enough to hold the bar clamp in place but not so tight as to damage the emulator pod cables.

4. Tighten the nut placed on the stud in Step 2, being sure to observe the cautions given in Step 3.

5. Up to two sets of emulator pod cables can be grounded in this fashion, using the procedure described above.

64110A

1. Insert a screw (item 2) through the single hole end (NOT the slot end) of the ground bar clamp (item 1). Continue with the screw through the right most perforation of the emulator pod cable shield braid and the right most hole of the sheet metal in the rear of the mainframe. (Right most as viewed from the rear of the mainframe. Refer to Figure 2-6 for details.)

2. Repeat the procedure with another screw; this time, use the slot end of the bar clamp and the holes in the shield braid and sheet metal immediately left of the right most position (refer to Figure 2-6).

h. The emulation bus cables are next installed across the Control Card, the emulation memory controller, and the analysis options. (Refer to Table 2-1 for a list of available emulation bus cables.) The cables are keyed so that they will seat on the edge connector in only one position.

Table 2-1. Emulation Bus Cables

Cable	HP Part Number
Two Connector	8120-3351
Three Connector	8120-3352
Four Connector	8120-3353
Five Connector	8120-3345

i. Reinstall the card cage access cover and tighten the two screws (64100A). (Refer to the 64110A Mainframe Service Manual for information on replacing the card cage access cover of the 64110A.)

2-8. To remove the 64271A, reverse the installation procedure.

2-9. RFI GROUND BRACKET INSTALLATION.

2-10. An RFI Ground Bracket must be installed in the 64100A mainframe when installing the 64271A Control Board with any emulator pod that uses a shielded cable assembly for RFI suppression. The purpose of this ground bracket is to connect the emulator pod cable shield braid to earth ground. This effectively prevents the emission of radio frequency interference components from the pod cables.

2-11. No ground bracket is required on the 64110A development station, since the bar clamp holding the shield braid to the mainframe bolts into existing sheet metal which is at ground potential.

2-12. The RFI ground bracket parts are included with the emulator pod. For convenience, a photograph depicting all the parts is reproduced here; Table 2-2 gives a listing of the parts included in the ground bracket assembly.

d. If the Control Board has previously been installed in the development station, it must be removed to remove or install the emulator pod. To remove the 64271A, grasp both board extractor levers (at the top of the card) and pull up until the card disengages from the motherboard and clears the card guide rails.

e. Before installing the 64271A in the card cage, connect the selected Emulator Pod to the 64271A. Three multi-colored ribbon cables (within a shielded cable assembly) are used to connect the Emulator Pod to the Control Board. One cable is terminated in a female card-edge connector; the other two are terminated in female socket type connectors. Pin 1 is indicated by a triangle molded into each connector. The mating male connectors are at the top left corner of the 64271A (as you face the component side of the board). Pin 1 of the card-edge connector is indicated by a "1" etched on the board surface; Pin 1 of the two block connectors is indicated by a triangle molded into the connector block. The two block connectors and their female counterparts have matching colored dots on their surfaces. Also, the block connectors on the board are a latching type. Make sure the connectors are open (tips spread towards outside edges of board) before installing the emulator pod cables. Making sure to align Pin 1 of the male and female connectors, connect the pod to the control board by joining the three connector sets. When installing the block connectors, push down on the female connector until the latching tips snap over the top of the connector.

NOTE

To help prevent scuffing the pod cables when installing or removing the Control Board, try to keep the cables as flat and as close to the board as possible. When sliding the board into the development station, care should be used to prevent the cables from rubbing against the back side of the board installed in front of the Control Board.

f. Next install the 64271A in the 64100 card cage. To do this, grasp the control card by the extractor levers with the component side of the board towards the front of the develop- ment station and the card edge connector labeled "P1" towards the bottom of the card cage. Insert the card into the guide rails; making sure the connector "P1" and the edge connector socket on the Motherboard are aligned, push the card down until it seats firmly in the socket.

g. If the 64271A is installed with an emulator pod that uses a shielded cable assembly for RFI suppression, a ground bar clamp must now be installed to ground the shielded cable assembly to the mainframe sheet metal. Refer to Figure 2-3 for an illustration of the clamp (item 1); refer to either Figure 2-5 (64100A) or Figure 2-6 (64110A) as appropriate for details on how the clamp is installed while following the procedures given below.

64100A

1. The emulator pod cable shield braid has two perforations. Place the perforation nearest the RFI ground bracket stud over the stud and press down gently until the cable lays flat across the top rear of the mainframe.

2. Place the single hole end (NOT the slot end) of the ground bar clamp (item 1) over the RFI ground bracket stud in such a manner that the open end of the slot points in a clockwise direction as viewed from the top of the development station. Thread a single nut (item 5) onto the stud. Do not tighten the nut at this point.

3. Insert the long screw (item 4 in Figure 2-3) into the slot end of the ground bar clamp. Continue by inserting the screw through the free end of the ground shield braid

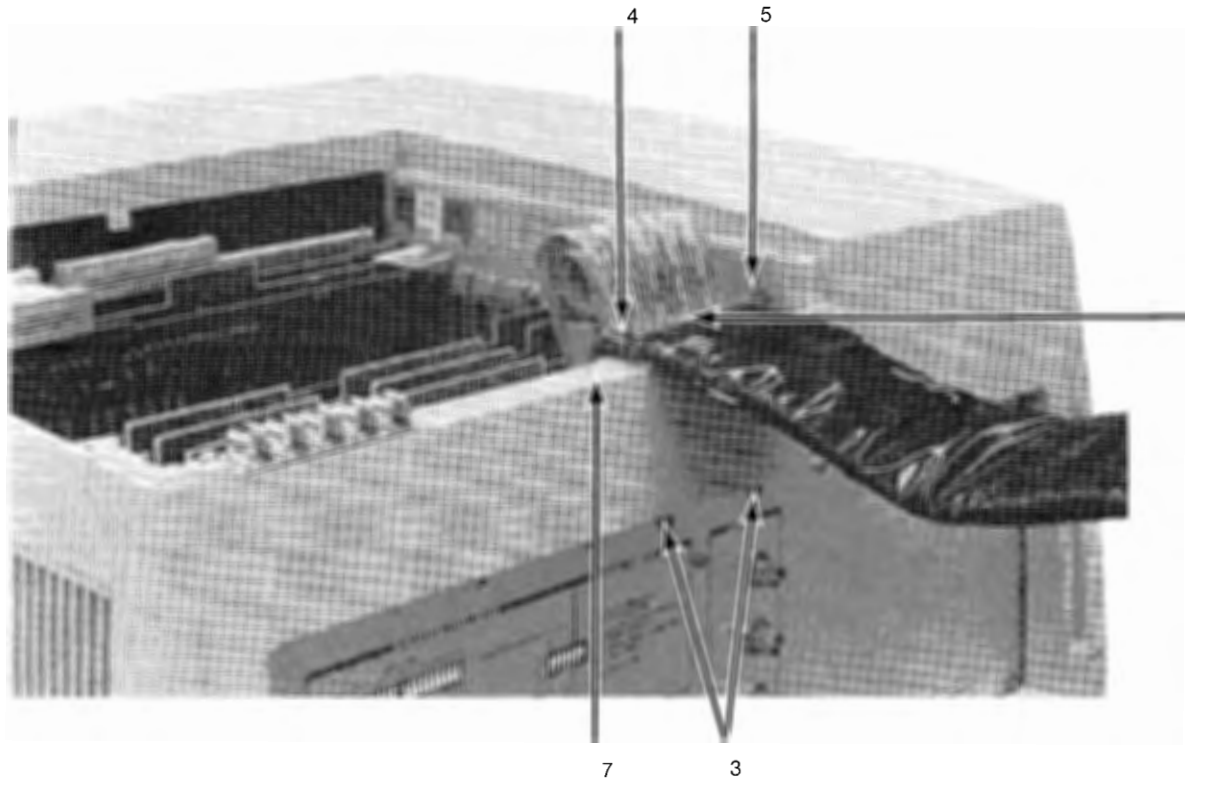


Figure 2-5. Ground Bar Clamp Installation (64100A)

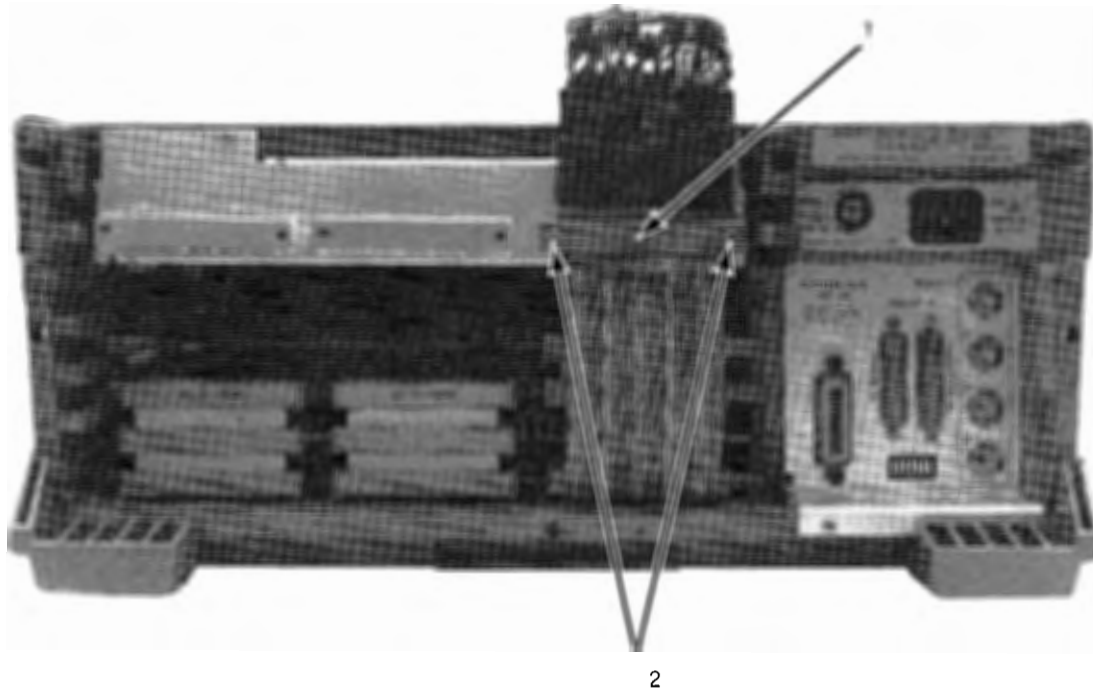


Figure 2-6. Ground Bar Clamp Installation (64110A)

Table 2-2. RFI Ground Bracket Assembly Parts

REF DES	DESCRIPTION	PART #
ITEM 0	GROUND BRACKET ASSY	64100-62102
ITEM 1	GROUND BAR CLAMP	1531-0273
ITEM 2	SCREW 4-40 3/4"	2200-0151
ITEM 3	SCREW 6-32 3/8"	2360-0117
ITEM 4	SCREW 6-32 1"	2360-0129
ITEM 5	NUT 6-32	2420-0001
ITEM 6	WASHER	3050-0235
ITEM 7	RFI GROUND BRACKET	64100-01207

2-13. To install the ground bracket on the 64100A development station, proceed as follows:

a. If no ground bracket is installed in the mainframe, then the old U-shaped cable strain relief bracket on the rightmost side of the mainframe top cover (as viewed from the rear) must be removed. Loosen the two screws; remove the bracket; discard the bracket and the screws (they will not be needed for the RFI bracket).

b. Place the RFI bracket on the top rear cover of the mainframe in the rightmost cable position (as viewed from the rear of the station) with the threaded stud on the bracket pointing upwards and the U-shaped portion of the bracket to the inside of the card cage. Refer to Figure 2-4 for details.

c. Refer to Figure 2-5. Thread two screws (item 3) into the RFI bracket from the outside of the development station rear panel sheet metal. Tighten the screws securely.

d. To remove the bracket, reverse the installation procedure.

2-14. OPERATING ENVIRONMENT.

2-15. The 64271A may be operated in environments within the following limits:

Temperature..... 0°to +55°C
Humidity.....Up to 95% relative humidity at +40°C
Altitude..... 4 600 m (15 000 ft)

It should be protected from temperature extremes which cause condensation within the instrument.

2-16. STORAGE AND SHIPMENT.

2-17. ENVIRONMENT.

2-18. The 64271A may be stored or shipped in environments within the following limits:

Temperature..... -40°C to +75°C
Humidity..... Up to 90% relative humidity
Altitude..... 15 000 m (50 000 ft)

2-19. ORIGINAL PACKAGING.

2-20. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard offices.

2-21. OTHER PACKAGING.

2-22. The following general instructions should be used for re-packing with commercially available materials:

a. Wrap the 64271A in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4- inch) thick around all sides of the 64271A to provide firm cushioning and prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

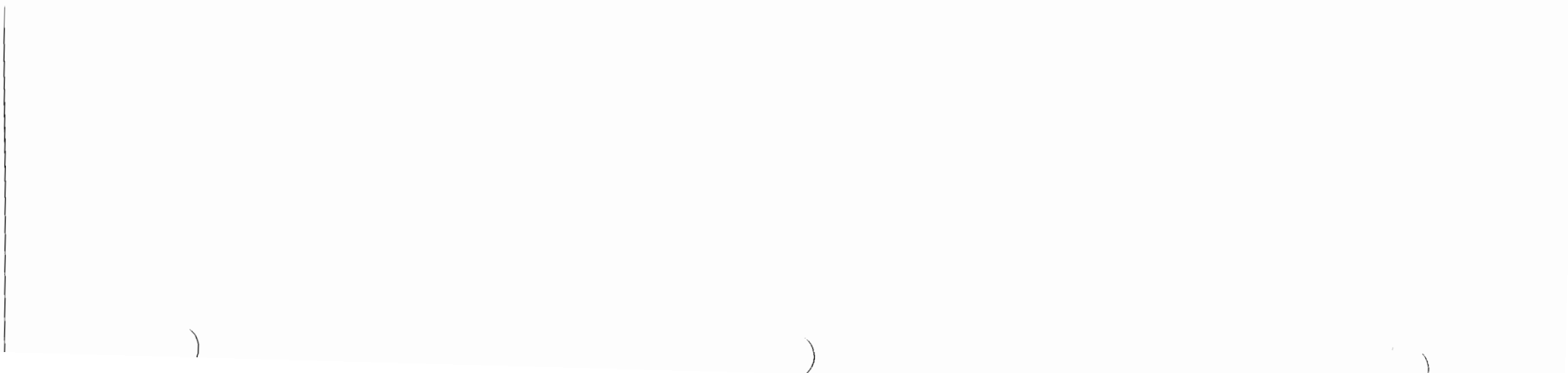
f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section contains no operating information. Refer to the applicable Emulation Subsystem Operator's Guide for information relating to the operation of the 64271A.



SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification for the General Purpose Emulation Control Card. The scope of the Performance Verification is to detect problems at the board level only. Board level troubleshooting is in support of the Blue Stripe Program.

4-3. For convenience, the figures for the Performance Verification are grouped together at the end of this section.

4-4. 64271A PERFORMANCE VERIFICATION.

4-5. The Performance Verification (P.V.) for the 64271A General Purpose Control Board is a subsection of the Option Test P.V. The Option Test P.V. tests all possible option modules that can be configured within the expansion slots of the Mainframe.

The option_test P.V. can either be run with a 64000 development station configured in a network arrangement (hard disk based); or it may be run from a 64000 station in a stand-alone configuration (mini disk based). When running the option_test performance verification on a Model 64271A Control board from a stand-alone 64000 configuration, the following modules must be present on the current local disk system:

FLOPPY_OP_SYS
OPTION_TEST
PV_EMUL_UDE

4-6. To test the 64271A, proceed as follows:

a. With the operating system initialized and awaiting a command, use the softkey (or manually type the lower case command):

option_test RETURN

Refer to Figure 4-1.

b. The P.V. will now display a directory of the installed option boards and their card slot number (Figure 4-2). Locate the General Purpose Controller - No Pod and enter the card slot number. For example, in Figure 4-2 the 64271A is in slot 9. Therefore, enter:

9 RETURN

c. A menu will now be displayed showing the test available to exercise the 64271A. This is the Mapper Control Test (refer to Figure 4-3). The following softkeys will appear at the bottom of the display:

<end>	Returns the user to the option test card slot listing.

<disp_test>	Advances the user to the detailed view of the mapper control test; that is, the test execution display.
<print>	Copies the display to the system line printer (if one is attached).

d. Press the <disp_test> softkey. This will advance the P.V. to the Control Board test execution display (refer to Figure 4-4). The following softkeys are listed at the bottom of the display:

<start>	Begins execution of the tests listed.
<exit_test>	Returns the user to the Mapper Control Test overview display described previously.
<print>	Copies the display to the system line printer (if one is attached).

e. To initiate testing of the General Purpose Control Card, press the <start> softkey. The key will be highlighted in inverse video on the display and test execution will proceed. If all tests pass, testing can be terminated as described in the next paragraph. However, if any failures occur, refer to the description of the Control Board Test in the following sections.

f. Termination of testing on the 64271A is possible in one of two ways:

1) The <start> softkey may be pressed. The test will terminate at the end of the current test cycle and the start softkey on the display will return to normal video. To completely exit the performance verification from this point, press the <exit_test> softkey. This returns the user to the Mapper Control Test display. Press the <end> softkey while in this display. This returns the user to the option_test card slot listing, at which point the <end> softkey can be pressed to exit the performance verification software.

2) The <exit_test> softkey may be pressed. The test will terminate at the end of the current test cycle and the display will be returned to the Mapper Control Test overview display. At this point, the user may press the <end> softkey, returning the display to the option_test card slot listing level. When the <end> softkey is pressed at this point, the option_test performance verification is completely exited and the display is returned to the "Awaiting command" status.

4-7. CONTROL BOARD TEST (Figure 4-4).

4-8. The Control Board Test consists of six tests. Each will be discussed in the order that they appear on the menu.

4-9. RAM OUTPUT SHORT TESTS (VCC/GND).

4-10. Purpose -- to make sure that the high speed ready mapper RAMs can output zeroes and ones throughout their address range.

4-11. What -- the mainframe CPU writes zeroes to all locations in the mapper RAMs and verifies that all locations can be read back correctly. The test is then repeated by writing ones to all locations and reading them back.

4-12. How -- the mainframe CPU address bus is translated through buffers U25 and U33 to the address bus HEA 8-23 of the mapper RAMs (U17,18). This is done by asserting LSEL from the mainframe bus and LDEFIB from control register U52. The mapper RAMs are selected in turn by the state of RESSEL. If RESSEL is high, U17 will be enabled; if low, U18 will be enabled. The write strobe for the RAMs is provided by LWPREADY from the function select decoder U43. LD0 from the mainframe CPU provides the data input for the RAMs. All locations in each RAM are written as a zero, and read back by negating LWPREADY and lowering U47 pin 1. This allows the mapper output to be passed through U35 and U47 out onto the mainframe data bus LD0. All other conditions remain the same for a read as they do for a write. The process is repeated by writing ones to all locations in the mapper RAMs and reading back the result.

4-13. Results -- If both RAMs fail at all locations, one of the following messages appears on the status line:

"Ram output stuck at VCC or defective (always on) write circuit"

"Ram output stuck at GND"

The test assumes that at least one RAM is good; it is also assumed that at least one RAM is present. If one of the RAMs has all failures it is assumed that the RAM is missing or defective.

4-14. Troubleshooting -- failures in this test are most likely caused by problems with the General Purpose Control Board; however, the emulator pod may be causing problems on the emulation address lines during the writes to the mapper RAM (if an emulator pod is left attached to the control board). To determine whether or not this is the case, disconnect the Emulator Pod from the Control Board and re-run the test. If the test still fails, the problem is with the Control Board; if the test passes, the problem is with the Emulator Pod. A probable reason for this failure is an improper DEFIB of the address buffers driving the bus to the 64271A.

4-15. MAPPER WRITE TEST.

4-16. Purpose -- to verify that the mapper RAM write circuitry is functional.

4-17. What -- the mainframe CPU writes zeroes to all locations in the mapper RAMs and then verifies that all locations were written correctly. The process is repeated by writing ones to all locations in the RAMs and verifying that correct data was written. If both write sequences show some failures, that is, the RAM will not write all zeroes and it also will not write all ones, another test is run which checks that writing a zero or one to each address returns the same result. If this test indicates that writing a zero or one to every location returns the same result, it is assumed that the write circuitry is defective.

4-18. How -- this test is performed in a similar manner to the preceding one. The mainframe CPU address bus is translated through buffers U25 and U33 to the address bus HEA 8-23 of the mapper RAMs (U17,18). This is done by asserting LSEL from the mainframe bus and LDEFIB from control register U52. The mapper RAMs are selected in turn by the state of RESSEL. If RESSEL is high, U17 will be enabled; if low, U18 will be enabled. The write strobe for the RAMs is provided by LWPREADY from the function select decoder U43. LD0 from the mainframe CPU provides the data input for the RAMs. All locations in each RAM are written as a zero, and read back by negating LWPREADY and lowering U47 pin 1. This allows the mapper output to be passed through U35 and U47 out onto the mainframe data bus LD0. All other conditions remain the same for a read as they do for a write. The process is repeated by writing ones to all locations in the mapper RAMs and reading back the result.

4-19. Results -- if an error is detected in either the first or second test then the status line will read:

"Defective (inactive) write circuitry"

4-20. Troubleshooting -- problems in this test are most likely to occur on the General Purpose Control Board; however, the emulator pod may be causing interference with the emulation address lines during the write sequences to the mapper RAMs (if an emulator pod is left attached to the control board). To determine whether or not this is the case, disconnect the Emulator Pod from the Control Board and re-run the test. If the test fails, the problem is with the Control Board; if the test passes, the problem is with the Emulator Pod. A probable reason for this failure is an improper DEFIB of the pod address buffers driving the bus to the 64271A.

4-21. INTERRUPT AND BREAK TESTS.

4-22. Purpose -- this test verifies that the mainframe CPU can cause an emulator break, and that the emulator control board can assert a mainframe CPU interrupt.

4-23. What -- in the first test, the mainframe CPU toggles the control register break line and reads it back. In the second test, the mainframe CPU enables interrupts and toggles the break line, then verifies that a mainframe interrupt is asserted.

4-24. How -- in the first test, the mainframe CPU sets the LBPCBRK line (output of control register U52) to a high and a low state in turn, and reads back the state of the line by enabling the output of status buffer U53. In the second test, the mainframe CPU sets the INTEN line (output of control register U41) to the high state and then toggles the LBPCBRK line to the low state. This propagates through U28 and U44 to force the output of U57 (LIR1) low, which will cause a mainframe interrupt to occur.

4-25. Results -- if the first test fails, one of the following messages will be displayed on the status line:

"Break appears to be stuck at ground"
"Break appears to be indeterminately failing"

The mainframe CPU assumes that the second test has failed if a jump to an interrupt service routine does not occur (this routine negates an error flag). If the test fails, the following message will be displayed on the status line:

"Break does not cause a mainframe CPU interrupt"

4-26. Troubleshooting -- Failures in this test are most likely to be caused by problems with the General Purpose Control Board, so it is recommended that this board be replaced first.

4-27. ADDRESS LINE SHORT TO GND TEST.

4-28. Purpose -- to make sure that address lines HEA 8-23 are not shorted to ground and can be read by the last address registers.

4-29. What -- the mainframe CPU performs a series of mapper RAM writes to appropriate addresses. The last address registers are clocked every time that a mapper write is done. The mainframe CPU then reads back the status of the last address registers and compares it with what was written.

4-30. How -- the mainframe CPU address bus is translated through buffers U25 and U33 to the address bus HEA 8-23 of the mapper RAMs (U17,18). This is done by asserting LSEL from the mainframe bus and LDEFIB from control register U52. The write strobe for the RAMs is provided by LWPREADY from the function select decoder U43. This signal is also input to AND gate U28C, which drives the reset input of flip-flop U22. When a mapper write is done (LWPREADY toggles low), U22 is cleared. The output of U22 is used to drive U45B, which provides the SETLAS signal to the last address registers. A low-to-high transition on this line clocks the mapper address into the last address registers (U39,U40). The mainframe CPU then reads the desired register by enabling it via function select decoder U43.

4-31. Results -- if an difference is detected between the address that was written and the address that was read, the following message will appear on the status line:

"Lines (HEA23 - HEA8)=XXXXH Appear to be fixed low"

This status information is decoded as follows:

HEX =	BINARY	SIGNAL
0000	0000 0000 0000 0000	
	---- ---- ---- ---1	HEA8
	---- ---- ---- --1-	HEA9
	---- ---- ---- -1--	HEA10
	---- ---- ---- 1---	HEA11
	---- ---- ---1 ----	HEA12
	---- ---- --1- ----	HEA13
	---- ---- -1-- ----	HEA14
	---- ---- 1--- ----	HEA15
	---- ---1 ---- ----	HEA16
	---- --1- ---- ----	HEA17
	---- -1-- ---- ----	HEA18
	---- 1--- ---- ----	HEA19
	---1 ---- ---- ----	HEA20
	--1- ---- ---- ----	HEA21
	-1-- ---- ---- ----	HEA22
	1--- ---- ---- ----	HEA23

For example, if the message reads (HEA23 - HEA8)=1248H, then HEA20, HEA17, HEA14, and HEA11 are bad.

4-32. Troubleshooting -- failures in this test are most likely caused by problems with the General Purpose Control Board; however, the emulator pod may be causing interference on the emulation address lines (if an emulator pod is left attached to the control board). To determine whether or not this is the case, disconnect the Emulator Pod from the Control Board and re-run the test. If the test fails, the problem is with the control board; if the test passes, the problem is with the Emulator Pod. The emulator pod address buffers which drive the 64271A should be checked to verify that they are tri-stated by the DEFIB signal from the Control Board.

4-33. ADDRESS LINE SHORT TO VCC TEST.

4-34. Purpose -- to make sure that address lines HEA 8-23 are not shorted to the +5 volt supply and can be read by the last address registers.

4-35. What -- the mainframe CPU performs a series of mapper RAM writes to appropriate addresses. The last address registers are clocked every time that a mapper write is done. The mainframe CPU then reads back the status of the last address registers and compares it with what was written.

4-36. How -- the mainframe CPU address bus is translated through buffers U25 and U33 to the address bus HEA 8-23 of the mapper RAMs (U17,18). This is done by asserting LSEL from the mainframe bus and LDEFIB from control register U52. The write strobe for the RAMs is provided by LWPREADY from the function select decoder U43. This signal is also input to AND gate U28C, which drives the reset input of flip-flop U22. When a mapper write is done (LWPREADY toggles low), U22 is cleared. The output of U22 is used to drive U45B, which provides the SETLAS signal to the last address registers. A low-to-high transition on this line clocks the mapper address into the last address registers (U39,U40). The mainframe CPU then reads the desired register by enabling it via function select decoder U43.

4-37. Results -- if an difference is detected between the address that was written and the address that was read, the following message will appear on the status line:

"Lines (HEA23 - HEA8)=XXXXH Appear to be fixed high or open"

This status information is decoded as follows:

HEX =	BINARY	SIGNAL
0000	0000 0000 0000 0000	
	---- ---- ---- ---1	HEA8
	---- ---- ---- --1-	HEA9
	---- ---- ---- -1--	HEA10
	---- ---- ---- 1---	HEA11
	---- ---- ---1 ----	HEA12
	---- ---- --1- ----	HEA13
	---- ---- -1-- ----	HEA14
	---- ---- 1--- ----	HEA15
	---- ---1 ---- ----	HEA16
	---- --1- ---- ----	HEA17
	---- -1-- ---- ----	HEA18
	---- 1--- ---- ----	HEA19
	---1 ---- ---- ----	HEA20
	--1- ---- ---- ----	HEA21
	-1-- ---- ---- ----	HEA22
	1--- ---- ---- ----	HEA23

For example, if the message reads (HEA23 - HEA8)=1248H, then HEA20, HEA17, HEA14, and HEA11 are bad.

4-38. Troubleshooting -- failures in this test are most likely to be caused by problems with the General Purpose Control Board; however, the emulator pod may be causing interference on the emulation address lines (if an emulator pod is left attached to the control board). To determine whether or not this is the case, disconnect the Emulator Pod from the Control Board and re-run the test. If the test fails, the problem is with the Control Board; if the test passes, the problem is with the Emulator Pod. The emulator pod address buffers which drive the 64271A should be checked to verify that they are being set to the high-impedance off state by the DEFIB signal from the Control Card.

4-39. ADDRESS LINE TO LINE SHORTS TEST.

4-40. Purpose -- to make sure that address lines HEA 8-23 are not shorted to each other and can be read by the last address registers.

4-41. What -- the mainframe CPU performs a series of mapper RAM writes to appropriate addresses. The last address registers are clocked every time that a mapper write is done. The mainframe CPU then reads back the status of the last address registers and compares it with what was written.

4-42. How -- the mainframe CPU address bus is translated through buffers U25 and U33 to the address bus HEA 8-23 of the mapper RAMs (U17,18). This is done by asserting LSEL from the mainframe bus and LDEFIB from control register U52. The write strobe for the RAMs is provided by LWPREADY from the function select decoder U43. This signal is also input to AND gate U28C, which drives the reset input of flip-flop U22. When a mapper write is done (LWPREADY toggles low), U22 is cleared. The output of U22 is used to drive U45B, which provides the SETLAS signal to the last address registers. A low-to-high transition on this line clocks the mapper address into the last address registers (U39,U40). The mainframe CPU then reads the desired register by enabling it via function select decoder U43.

4-43. Results -- if an difference is detected between the address that was written and the address that was read, the following message will appear on the status line:

"Lines (HEA23 - HEA8)=XXXXH Appear to have line to line shorts"

This status information is decoded as follows:

HEX =	BINARY	SIGNAL
0000	0000 0000 0000 0000	
	---- ---- ---- ---1	HEA8
	---- ---- ---- --1-	HEA9
	---- ---- ---- -1--	HEA10
	---- ---- ---- 1---	HEA11
	---- ---- ---1 ----	HEA12
	---- ---- --1- ----	HEA13
	---- ---- -1-- ----	HEA14
	---- ---- 1--- ----	HEA15
	---- ---1 ---- ----	HEA16
	---- --1- ---- ----	HEA17
	---- -1-- ---- ----	HEA18
	---- 1--- ---- ----	HEA19
	---1 ---- ---- ----	HEA20
	--1- ---- ---- ----	HEA21
	-1-- ---- ---- ----	HEA22
	1--- ---- ---- ----	HEA23

For example, if the message reads (HEA23 - HEA8)=1248H, then HEA20, HEA17, HEA14, and HEA11 are bad.

4-44. Troubleshooting -- failures in this test are most likely to be caused by problems with the General Purpose Control Board; however, the emulator pod may be causing interference on the emulation address lines which will cause the test to fail (if an emulator pod is left attached to the control board). To determine whether or not this is the case, disconnect the Emulator Pod from the Control Board and re-run the test. If the test fails, the problem is with the Control Board; if the test passes, the problem is with the Emulator Pod. The emulator pod address buffers which drive the bus to the 64271A should be checked to verify that they are being set to the high-impedance off state by the DEFIB signal from the Control Card.

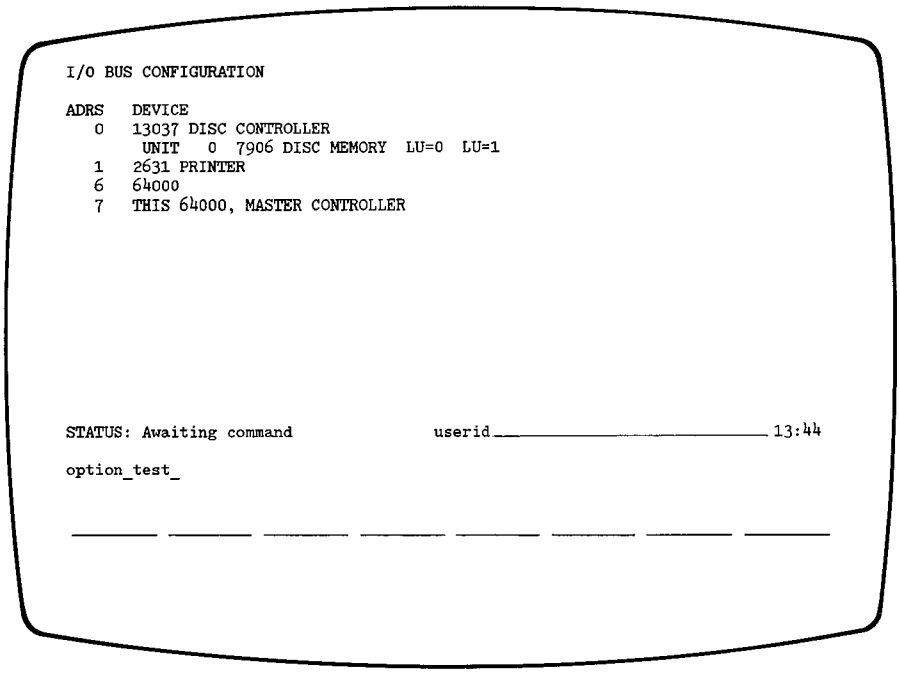


Figure 4-1. Awaiting Command Status

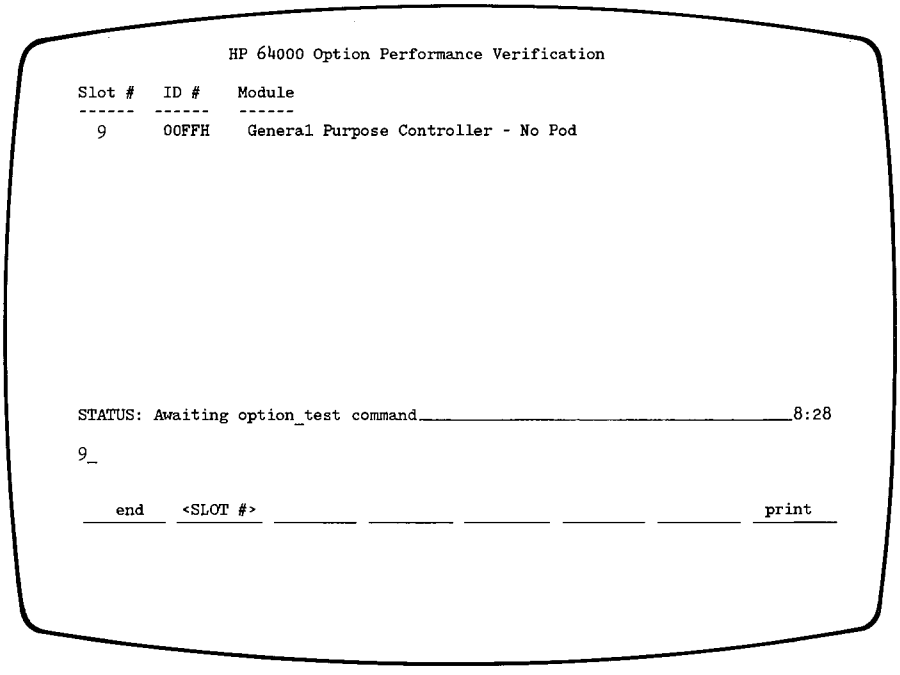


Figure 4-2. Option Test Card Slot Listing

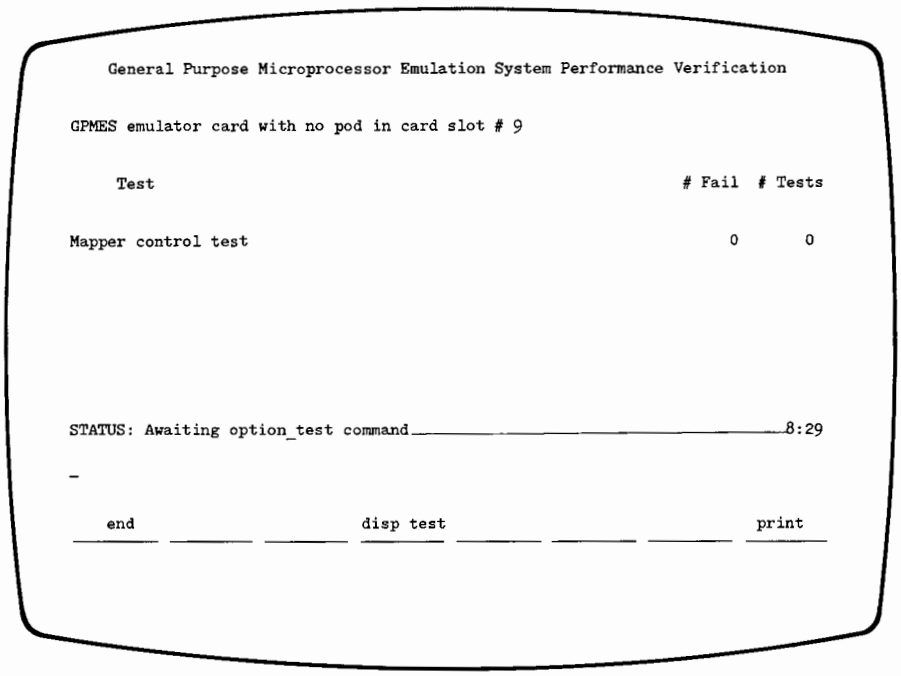


Figure 4-3. Mapper Control Test Overview

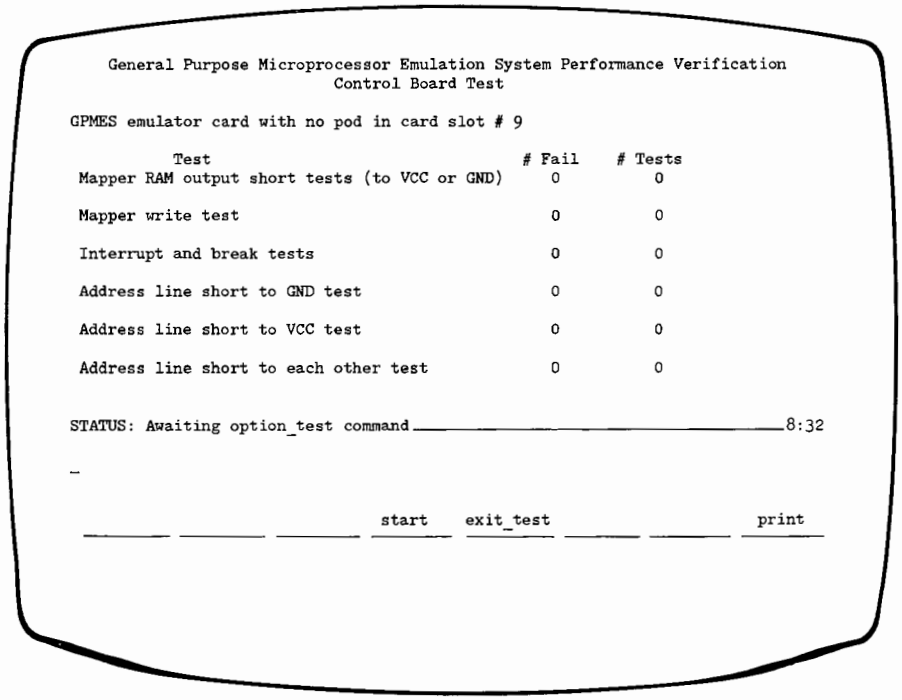


Figure 4-4. Control Board Test Display

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. The 64271A has no adjustments.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Section 6-3 lists exchange assemblies (Blue Stripe Program). Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains a list of manufacturer code numbers and corresponding names and addresses.

6-3. EXCHANGE ASSEMBLIES.

6-4. The Model 64271A is available through the Hewlett-Packard Corporate Parts Center by Blue Stripe Exchange. Exchange, factory repaired and tested assemblies are available only on a trade-in basis. Therefore, 64271A's required for spare parts stock must be ordered by the new assembly part number, found in Table 6-2, "Replaceable Parts". To order a Blue Stripe Exchange assembly, use Part Number 64271-69501.

6-5. ABBREVIATIONS.

6-6. Table 6-1 lists abbreviations used in the parts list, the schematics, and component locators.

6-7. REPLACEABLE PARTS.

6-8. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumeric order by reference designation.

b. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit (for HP internal use).

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A typical manufacturer of the part in a five-digit code.

e. The manufacturer's number for the part.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-9. ORDERING INFORMATION.

6-10. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service office.

6-11. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, description and function of the part and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/ Service office.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices- to provide these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

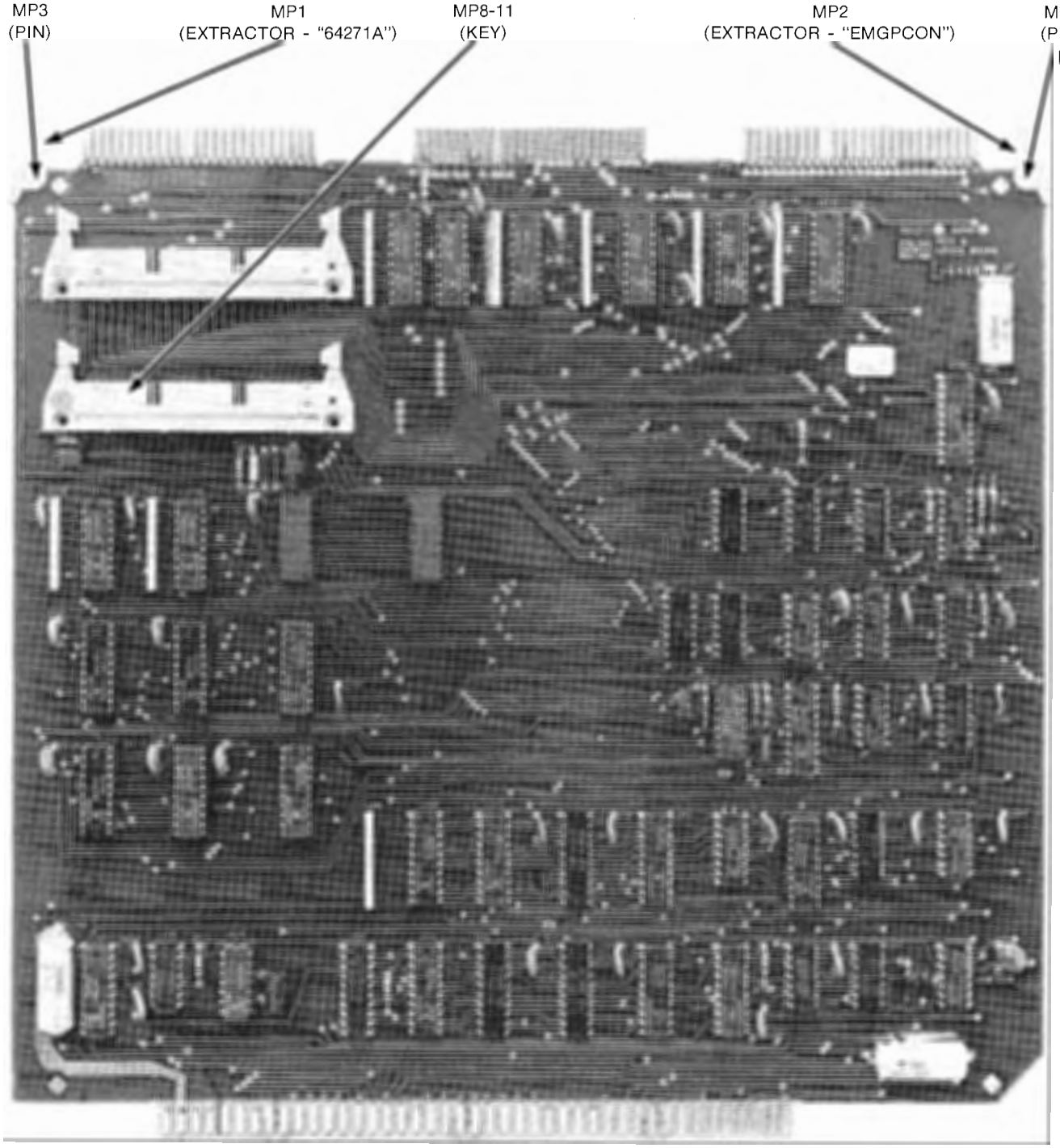


Figure 6-1. Illustrated Parts Breakdown (Sheet 1 of 2)

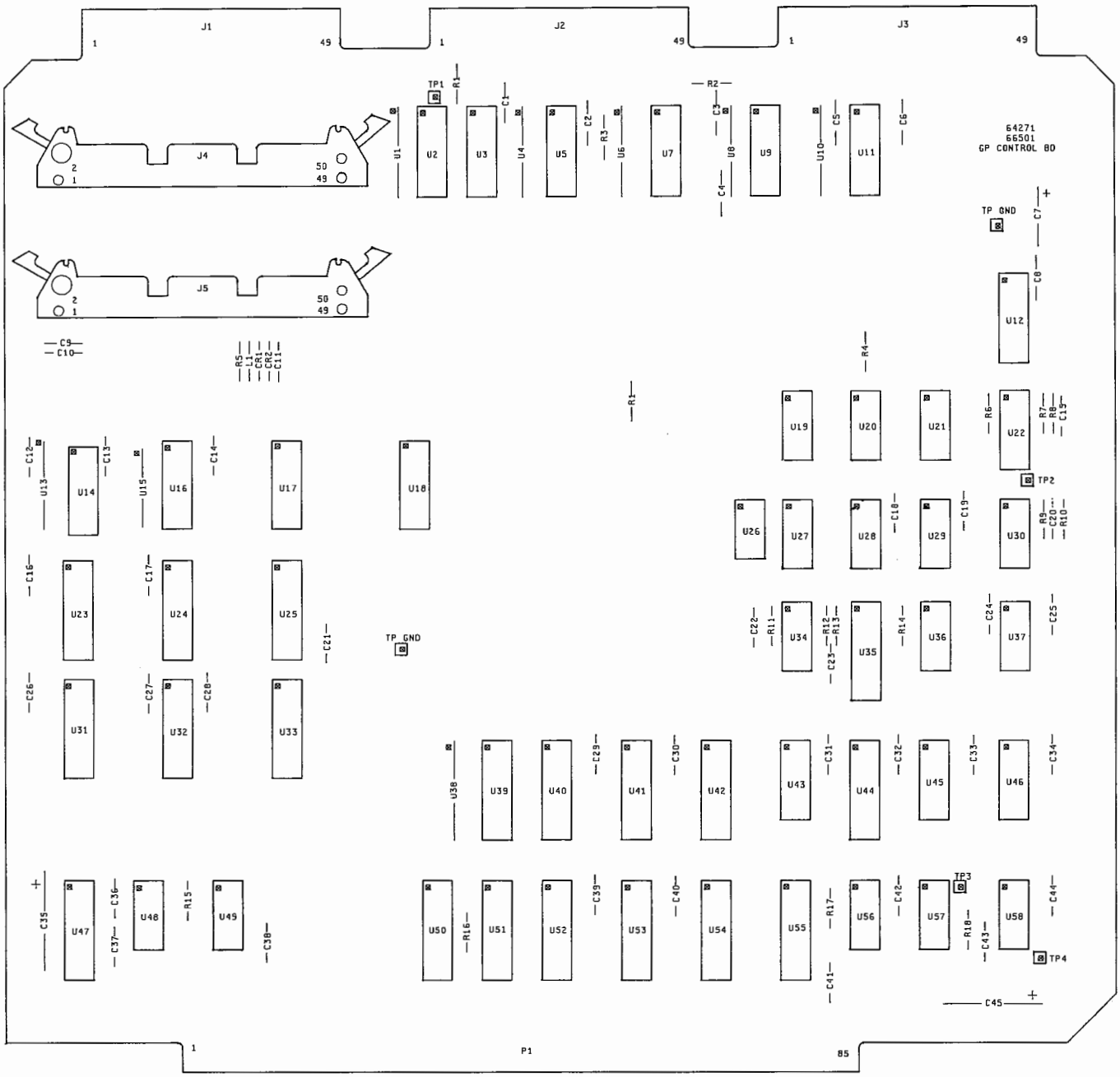


Figure 6-1. Illustrated Parts Breakdown (Sheet 2 of 2)

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	F	= fuse	MP	= mechanical part	U	= integrated circuit
B	= motor	FL	= filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	IC	= integrated circuit	Q	= transistor		
C	= capacitor	J	= jack	R	= resistor	VR	= voltage regulator
CP	= coupler	K	= relay	RT	= thermistor	W	= cable
CR	= diode	L	= inductor	S	= switch	X	= socket
DL	= delay line	LS	= loud speaker	T	= transformer	Y	= crystal
DS	= device signaling (lamp)	M	= meter	TB	= terminal board	Z	= tuned cavity network
E	= misc electronic part	MK	= microphone	TP	= test point		

ABBREVIATIONS

A	= amperes	H	= henries	N/O	= normally open	RMO	= rack mount only
AFC	= automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	= root-mean square
AMPL	= amplifier	HEX	= hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	HR	= hour(s)				
BE CU	= beryllium copper	HZ	= hertz	NPN	= negative-positive-negative	S-B	= slow-blow
BH	= binder head					SCR	= screw
BP	= bandpass			NRFR	= not recommended for field replacement	SE	= selenium
BRS	= brass	IF	= intermediate freq			SECT	= section(s)
BWO	= backward wave oscillator	IMPG	= impregnated	NSR	= not separately replaceable	SEMICON	= semiconductor
		INCD	= incandescent			SI	= silicon
CCW	= counter-clockwise	INCL	= include(s)			SIL	= silver
CER	= ceramic	INS	= insulation(ed)	OBD	= order by description	SL	= slide
CMO	= cabinet mount only	INT	= internal	OH	= oval head	SPG	= spring
COEF	= coeficient			OX	= oxide	SPL	= special
COM	= common	K	= kilo=1000			SST	= stainless steel
COMP	= composition					SR	= split ring
COMPL	= complete	LH	= left hand	P	= peak	STL	= steel
CONN	= connector	LIN	= linear taper	PC	= printed circuit		
CP	= cadmium plate	LK WASH	= lock washer	PF	= picofarads= 10^{-12} farads	TA	= tantalum
CRT	= cathode-ray tube	LOG	= logarithmic taper			TD	= time delay
CW	= clockwise	LPF	= low pass filter	PH BRZ	= phosphor bronze	TGL	= toggle
				PHL	= phillips	THD	= thread
DEPC	= deposited carbon	M	= milli=10^{-3}	PIV	= peak inverse voltage	TI	= titanium
DR	= drive	MEG	= meg=10^{6}	PNP	= positive-negative-positive	TOL	= tolerance
		MET FLM	= metal film			TRIM	= trimmer
ELECT	= electrolytic	MET OX	= metallic oxide	P/O	= part of	TWT	= traveling wave tube
ENCAP	= encapsulated	MFR	= manufacturer	POLY	= polystyrene		
EXT	= external	MHZ	= mega hertz	PORC	= porcelain	U	= micro=10^{-6}
		MINAT	= miniature	POS	= position(s)		
F	= farads	MOM	= momentary	POT	= potentiometer	VAR	= variable
FH	= flat head	MOS	= metal oxide substrate	PP	= peak-to-peak	VDCW	= dc working volts
FIL H	= fillister head	MTG	= mounting	PT	= point		
FXD	= fixed	MY	= "mylar"	PWV	= peak working voltage	W/	= with
						W	= watts
G	= giga (10^{9})	N	= nano (10^{-9})	RECT	= rectifier	WIV	= working inverse voltage
GE	= germanium	N/C	= normally closed	RF	= radio frequency		
GL	= glass	NE	= neon	RH	= round head or right hand	WW	= wirewound
GRD	= ground(ed)	NI PL	= nickel plate			W/O	= without

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64271-66501	1	1	GENERAL PURPOSE CONTROL BOARD ASSEMBLY	28480	64271-66501
C1	0160-2055	9	34	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C7	0180-0094	4	3	CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C9	0160-3622	8	3	CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C10	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C11	0140-0200	0	1	CAPACITOR-FXD 390PF +-5% 300VDC MICA	72136	DM15F391J0300WV1CR
C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0140-0207	7	2	CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22	0140-0202	2	1	CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR
C23	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C35	0180-0094	4		CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C38	0160-2201	7	1	CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C43	0140-0207	7		CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C45	0180-0094	4		CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
CR1	1901-0535	9	2	DIODE-SM SIG SCHOTTKY	28480	1901-0535
CR2	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
J4	1251-5653	3	2	CONNECTOR 50-PIN M POST TYPE	28480	1251-5653
J5	1251-5653	3		CONNECTOR 50-PIN M POST TYPE	28480	1251-5653
L1	9100-2264	5	1	INDUCTOR RF-CH-MLD 6.8UH 10% .105DX.26LG	28480	9100-2264
MP1	64271-85001	6	1	BOARD EXTRACTOR LEVER "64271A"	28480	64271-85001
MP2	64271-85002	7	1	BOARD EXTRACTOR LEVER "EMGPCON"	28480	64271-85002
MP3	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP5	7124-0267	2	1	LABEL-BROWN DOT	85480	QD25 TAPE B-810-BR
MP6	7124-0269	4	1	LABEL-RED DOT	85480	QD25 TAPE B-810-RD
MP7	7124-0270	7	1	LABEL-YELLOW DOT	85480	QD25 TAPE B-810-YL
MP8	1251-5595	2	4	POLARIZING KEY-POST CONN	28480	1251-5595
MP9	1251-5595	2		POLARIZING KEY-POST CONN	28480	1251-5595
MP10	1251-5595	2		POLARIZING KEY-POST CONN	28480	1251-5595
MP11	1251-5595	2		POLARIZING KEY-POST CONN	28480	1251-5595
R1	0757-0416	7	14	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R2	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R3	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R4	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R5	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R6	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R7	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R8	0757-0403	2	1	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R9	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R10	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R11	0757-0438	3	3	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R12	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R13	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R14	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R15	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R16	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R17	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R18	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
TP1	0360-0535	0	6	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TPGND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TPGND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1810-0430	0	7	NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
U2	1820-2699	8	7	IC-74F241	28480	1820-2699
U3	1820-1633	8	7	IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U4	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
U5	1820-2699	8		IC-74F241	28480	1820-2699
U6	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
U7	1820-1633	8		IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U8	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
U9	1820-1633	8		IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U10	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
U11	1820-1633	8		IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U12	1820-1633	8		IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U13	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
U14	1820-2699	8		IC-74F241	28480	1820-2699
U15	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
U16	1820-2699	8		IC-74F241	28480	1820-2699
U17	1818-3013	7	2	IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	28480	1818-3013
U18	1818-3013	7		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	28480	1818-3013
U19	1820-2684	1	3	IC-74F00	28480	1820-2684
U20	1820-2692	1	2	IC-74F86	28480	1820-2692
U21	1820-2685	2	2	IC-74F02	28480	1820-2685
U22	1820-0629	0	1	IC FF TTL S J-K NEG--EDGE-TRIG	01295	SN74S112
U23	1820-2700	2	3	IC-74F373	28480	1820-2700
U24	1820-2700	2		IC-74F373	28480	1820-2700
U25	1820-1917	1	3	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U26	1810-0568	2	1	DELAY LINE-30NS	28480	1810-0568
U27	1820-2684	1		IC-74F00	28480	1820-2684
U28	1820-2686	3	2	IC-74F08	28480	1820-2686
U29	1820-2690	9	1	IC-74F32	28480	1820-2690
U30	1820-2691	0	2	IC-74F74	28480	1820-2691
U31	1820-2700	2		IC-74F373	28480	1820-2700
U32	1820-2699	8		IC-74F241	28480	1820-2699
U33	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U34	1820-1782	8	1	IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
U35	1820-2699	8		IC-74F241	28480	1820-2699
U36	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U37	1820-2692	1		IC-74F86	28480	1820-2692
U38	1810-0275	1	1	NETWORK-RES 10-SIP 1.0K OHM X 9	01121	210A102
U39	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U40	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U41	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U42	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U43	1820-1240	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74S138N
U44	1820-1633	8		IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U45	1820-2684	1		IC-74F00	28480	1820-2684
U46	1820-2687	4	1	IC-74F10	28480	1820-2687
U47	1820-1633	8		IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U48	1820-2691	0		IC-74F74	28480	1820-2691
U49	1820-0261	6	1	IC MV TTL MONOSTBL	01295	SN74121N
U50	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U51	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U52	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U53	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U54	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U55	1820-2699	8		IC-74F241	28480	1820-2699
U56	1820-2685	2		IC-74F02	28480	1820-2685
U57	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	1820-1198
U58	1820-2686	3		IC-74F08	28480	1820-2686
XU2	1200-0639	8	14	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU3	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU5	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU7	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU9	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU11	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU14	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU16	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU17	1200-0539	7	2	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU18	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU23	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU24	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU25	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU31	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU32	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU33	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU34	1200-0607	0	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU49	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638

See introduction to this section for ordering information

Table 6-3. Manufacturer's Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
26654	VARADYNE INC	SANTA MONICA	CA	90404
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
85480	BRADY W H CO	MILWAUKEE	WI	53209

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section normally contains information for adapting this manual to assemblies to which the contents do not apply directly. Since this manual applies directly to serial prefixes listed on the title page, no change information is given. Refer to Section I for more information on repair numbers.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains information relating to the servicing and troubleshooting of the 64271A. Table 8-1 contains a listing of mnemonics (signal names), which are used in the schematics and theory of operation. Table 8-2 describes the basic symbols used on the schematics. Table 8-3 explains the symbology used to represent logic devices on the schematics. Figure 8-1 is a block diagram of the emulation subsystem; Figure 8-2 is a block diagram of the 64271A Control Board; and Figures 8-3 through 8-6 are the component locators and schematics for the 64271A. The material in this section is provided for reference purposes only. Refer to the applicable Emulation Subsystem service manual for information on troubleshooting procedures for the 64271A.

8-3. SAFETY.

8-4. Read the safety summary at the front of this manual before servicing this instrument.

8-5. THEORY OF OPERATION.

8-6. GENERAL.

8-7. The theory of operation information for the Model 64271A General Purpose Control Board is divided into four parts. The first part gives a basic overview of the emulation process. The second part introduces the block diagram of the emulation subsystem and describes the functions of each part of the subsystem. The third part introduces the block diagram of the 64271A Control Board and describes the board at the functional block level. The last part gives detailed theory of operation information broken down by schematics and the functional blocks appearing on each schematic.

While reading the theory of operation information, it may be helpful to refer to the paragraphs entitled "DESCRIPTION" in Section I of this manual in addition to the subsystem block diagram (Figure 8-1) and the GP Control Board block diagram (Figure 8-2).

8-8. EMULATION OVERVIEW.

8-9. "Emulate" means "to equal". In the HP64000 Logic Development System, the emulation implementation allows the user to replace the microprocessor in the target system breadboard with a plug from the emulator pod. The plug appears to act as much like the emulated microprocessor as is possible.

8-10. The user may develop programs using the assembler and compiler utilities of the 64000 system; store these on disk for later use; edit them as desired; and link them together while assigning absolute addresses (using the relocatable linker utility of the system). These programs may then be loaded into memory provided by the target system or by optional high-speed memory boards resident within the development station.

8-11. Once the programs are loaded into memory, the user may then release the emulator to run them so that an evaluation of the software or firmware can be made. When problems are found, the causes may be diagnosed by requesting the emulator to single-step through the program, display its registers, display a user or emulation memory location or locations, or perform other non-real time analysis functions. With the optional analysis module, real-time tracing of program state flow can be accomplished, providing a powerful tool for program analysis and debugging.

8-12. The emulation processor actually accomplishes the non-real time functions listed above. This is done by providing a monitor program within emulation memory space. The emulation system switches the processor between execution of the user program and the monitor program. For example, to single step the processor, the emulation system will release the processor to run the desired program. A break is then immediately asserted by the emulation software, forcing the emulator to begin executing the monitor program. (This is typically done via a non-maskable interrupt, although other emulation break implementations exist which do not use this resource). The program may cause the processor to store its registers into certain monitor memory locations. The mainframe can then request the processor to hold off memory accesses while it reads these monitor locations. The contents of each location can then be displayed on the development station screen with the appropriate register name. When the processor is finished executing the monitor program, it is directed to begin execution at the next address in the user program that would have been executed had a break not occurred. The sequence is then repeated.

8-13. EMULATION SUBSYSTEM BLOCK DIAGRAM.

8-14. Figure 8-1 is a block diagram of the emulation subsystem, which is used to emulate various microprocessors in the user's target system. Capabilities include software development and debugging, hardware emulation, and real-time program execution.

8-15. The emulator pod contains the specific microprocessor to be emulated. It may be used for software development with the user plug left unconnected; or its user plug may replace the microprocessor in the target system, allowing real-time execution of software developed on the 64000 system. It consists of two boards, one of which contains the microprocessor; the other contains logic to develop timing signals dedicated to that processor. The pod communicates with the rest of the emulation subsystem via the pod bus.

8-16. The General Purpose Control board performs the interface functions between the emulator pod, the emulation bus, and the mainframe bus. It buffers and controls data transactions between these three buses; performs a high-speed memory mapping function which is used to control buffers within the emulator pod, and also records various status information sent from the emulator pod.

8-17. The internal analysis module continuously stores data present on the emulation bus. It may be requested to store only certain sequences or types of data, and start or stop a store based upon the type of information present on the bus. The trace storage buffer is able to contain 256 different program states. A software disassembly function is provided for the analysis module. This converts binary data stored by the module into instruction mnemonics which are then displayed as requested on the 64000 system.

8-18. The wide address memory controller is used to control access to emulation memory and perform a mapping function, which allows various blocks of memory to appear to reside at user selected address ranges and respond as different types of memory (ROM, RAM, or illegal address range). The term "wide address" refers to the fact that this board is capable of responding to an address from the emulator pod which is 24 bits in width.

8-19. The emulation memory board(s) consist of banks of low-power high-speed static RAMs. Access to this memory is controlled by the wide address memory controller.

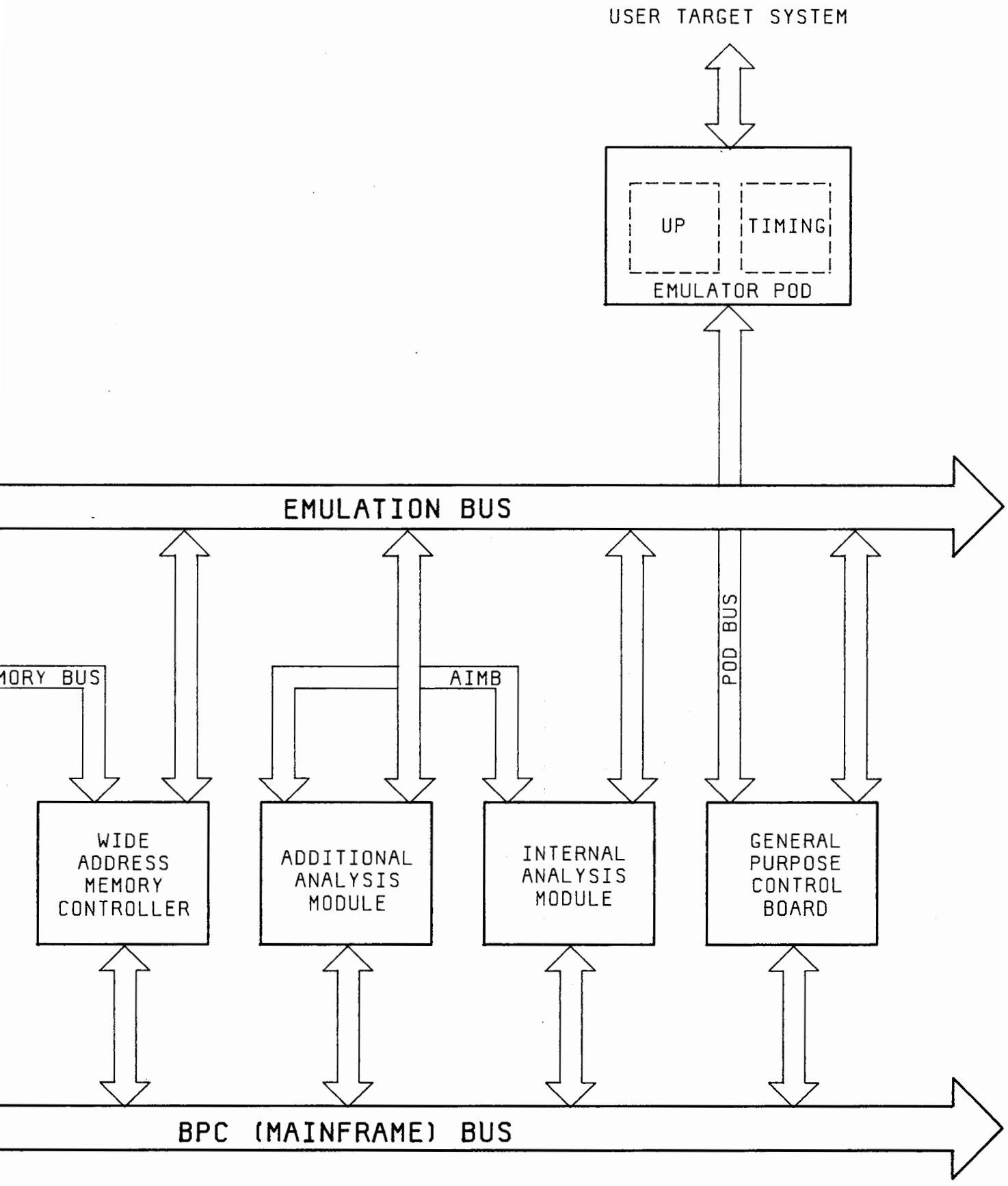
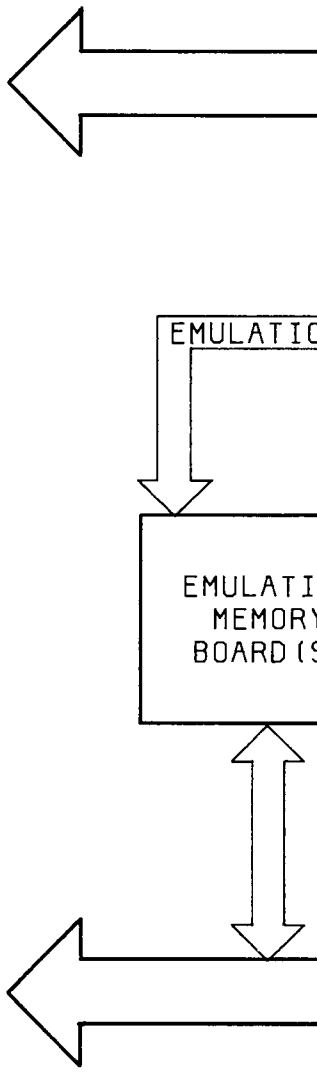


Figure 8-1.
Emulation Subsystem Block Diagram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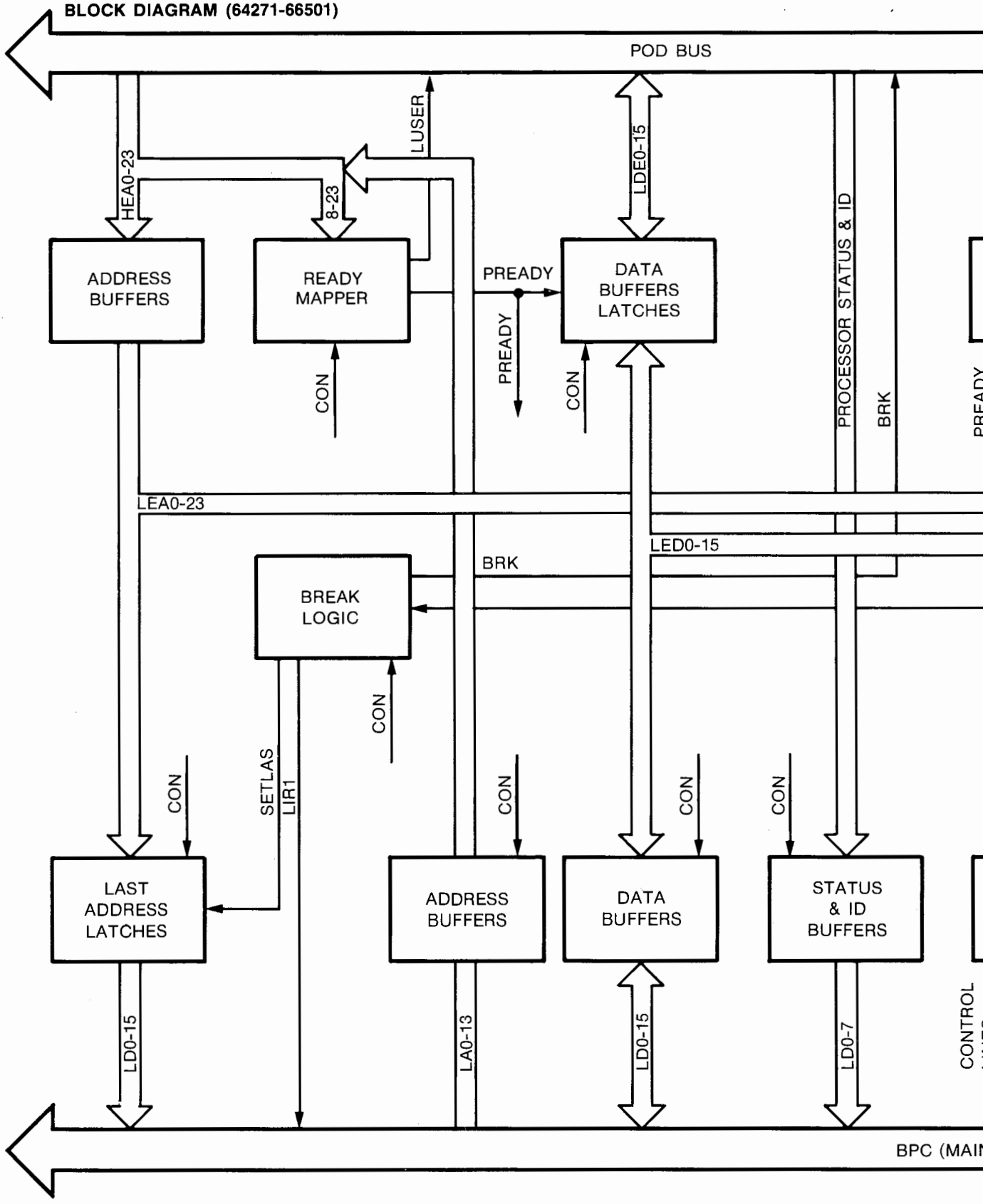
BLOCK DIAGRAM (64271-66501)



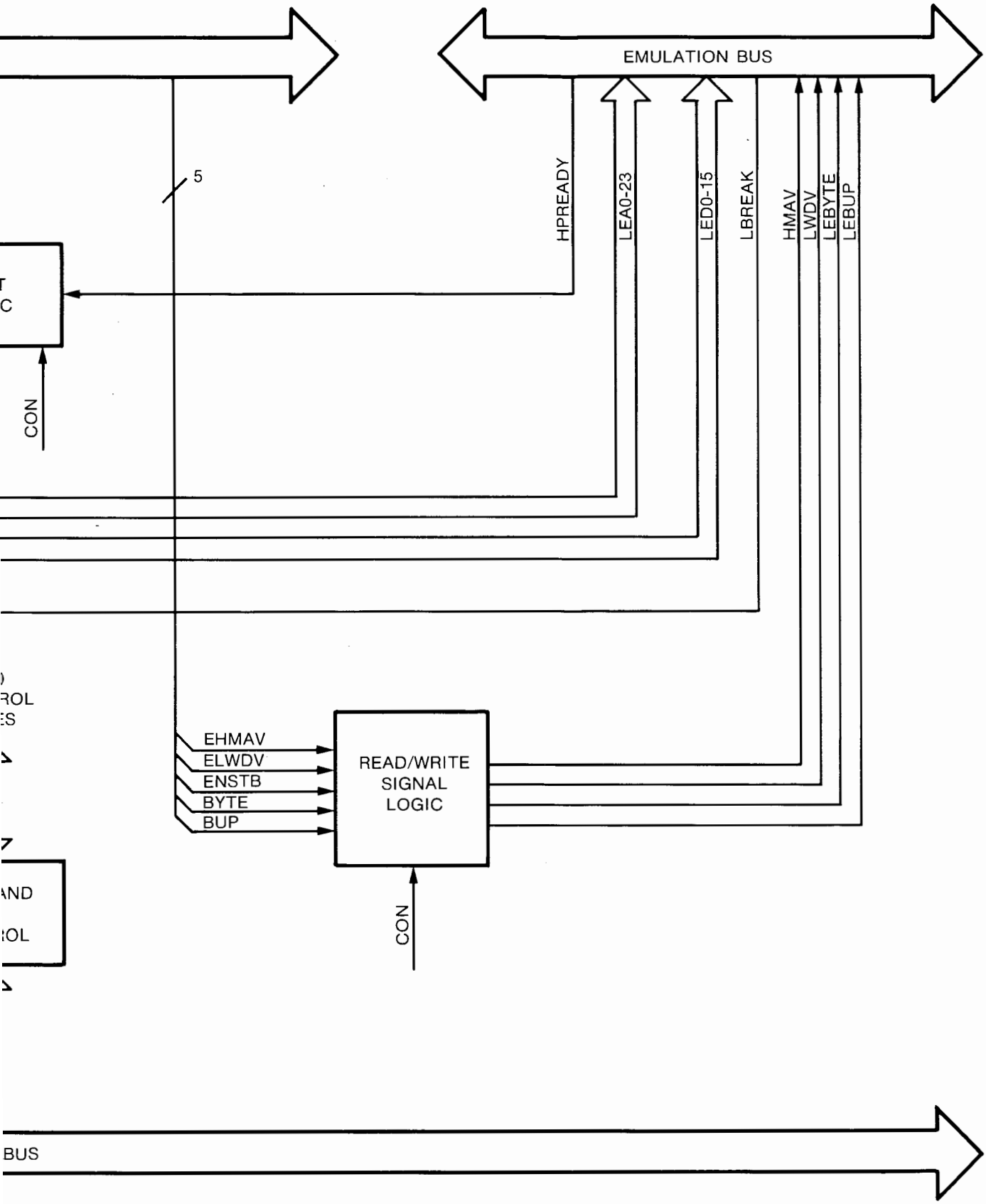


Figure 8-2. 64271A Block Diagram

8-20. GP CONTROLLER BLOCK DIAGRAM.

8-21. Figure 8-2 is a block diagram of the 64271A. The paragraphs below describe operation on the functional block level.

8-22. Last Address and Break Logic. Pod address HEA 0-23 is buffered to the emulation bus and the last address latches by address buffers. The last address latches are loaded on a low-to-high transition on the SETLAS line. If an emulation break (LBREAK) or a mainframe break (LBPCBRK) occurs, BRK is asserted. This causes an interrupt or break to be sent to the pod, and also allows the last address latches to hold the break address.

8-23. Ready Mapper. The ready mapper determines whether the current address on the pod bus (HEA 0-23) is within space mapped to user or emulation (mainframe) memory. Output from the mapper are two signals which are identical in logic function but have different uses. They are:

a. LUSER-- Output to the pod. When low, current address is within space mapped to user memory.

b. PREADY-- Internal use on control board. Used by the wait state generator and also used to enable the correct data buffers for a data transaction.

The mapper is programmed during the emulation defib (reset) mode.

8-24. Three Port Data Bus. Three separate data buses are used on the 64271A. They are:

a. Mainframe (mainframe CPU) data bus.

b. Pod data bus.

c. Emulation data bus.

The data bus enabling logic uses ready mapper signal PREADY and various signal lines from the command & control logic to determine which buffers to enable or disable for the data transaction.

8-25. Status and ID Buffers. The status buffer is used to gate emulation processor status onto the mainframe data bus. Also included is an ID (identification) buffer which, when enabled, tells the mainframe which emulator pod is connected to the control board, as well as identifying the control board itself.

8-26. Wait Logic. The wait logic functions as a programmable wait state generator, using PREADY (ready mapper), HPREADY (emulation memory controller), and various control lines to determine whether to insert wait states or acknowledges into the current memory cycle.

8-27. Command and Control. This section uses the mainframe data bus, address lines LA 12 & 13, and certain mainframe control lines to determine which functions are selected on the 64271A.

8-28. Read/Write Signal Logic. This section includes logic for:

a. Determining whether or not memory is being accessed (HMAV).

b. Inserting a delay into the ELWDV (Emulator Low Write Data Valid) line.

c. Determining polarity and function of the BYTE and BUP lines, which are used to enable lower and upper byte banks of memory.

8-29. SERVICE SHEET 1.

8-30. Service Sheet 1 (see Figure 8-3) depicts the circuitry used to interface the emulation control board and emulator pod to the mainframe CPU.

8-31. Address Buffers. During programming of the high-speed mapper RAMs (Service Sheet 2), the mainframe address bus must be applied to the address inputs of the RAMs. This is accomplished by three-state buffers U25 and U33; the outputs are enabled when the board is selected for an access while in the defib mode and LA12,13 are false. During all other conditions, the buffers are in the high-impedance off state, allowing the address lines from the emulator pod to be applied directly to the mapper RAMs without interference.

8-32. Data Buffers. Bidirectional transceivers U42 and U54 allow the mainframe CPU to communicate with the programmable registers within the emulator pod. Data is sent from the mainframe CPU bus to the emulator pod whenever the LWPOD signal is true. This occurs when the mainframe accesses the board during a write cycle within the address range 6XXX hex. Data is transferred from the emulator pod to the mainframe bus whenever the CPU reads from the address range 6XXX hex; this asserts the LRDPOD signal, which orients the transceivers properly for the transaction.

8-33. Last Address Latches. U39, U40 and U51 are octal registers with three-state outputs used to store the most recent state of the emulation processor's address bus. These latches are clocked by the SETLAS (Set Last Address Latches) signal from the timing logic. LEA0-23 from the emulation address bus drive the latch inputs. Reads of the latches are accomplished in a two step process, since the mainframe CPU can only handle 16 bits of data at a time. U39 and U51, which contain the lower 16 address bits, are read when the pin 11 output of mainframe command decoder U43 is true; this occurs when LWRT is false and LA12, 13 are true. The upper 8 address bits are stored in U40; this is read when LWRT is false, LA12 is true, and LA13 is false.

8-34. ID Buffer. U50 allows the mainframe to determine what type of emulator pod is attached to the GP Controller. The upper three bits of the inverting three-state buffer are hardwired to a logic high through R16; ID0-4 are provided by the emulation pod (if one is connected). To read the buffer, the mainframe CPU asserts LID while the board is selected and strobes the board (LSTB) to complete the transfer.

8-35. Status Buffer. U53 is an octal buffer with three-state outputs used by the emulation software through the mainframe CPU to determine the current status of the emulation pod and the control board. Five bits from the emulation pod drive the buffer; these are HWAITIN, HHALTIN, HRESETIN, HBUSGTIN and LICE. HWAITIN indicates whether or not the emulation processor is executing wait states; HHALTIN indicates that the processor is halted; HRESETIN indicates that the processor is being reset by the target system or by emulation; and HBUSGTIN indicates that the processor has released the bus to a requesting device. LICE indicates that the emulation pod is plugged into a powered on user target system.

LMBRKS drives bit 0 of the register; this line is asserted by the memory controller board to indicate that the break request originated on that board. LBPCBRK is driven directly by the control register, allowing verification of a break request generated by the mainframe. LOWSLOWCLOCK is driven by a monostable multivibrator; when low, it indicates that the processor has not performed any memory cycles for at least 150 nS.

To read the status buffer, the mainframe CPU asserts LA12 and negates LA13 during a read cycle from the board (LSEL, LSTB true, LID false).

8-36. Control Registers. U41 and U52 are octal D-type flip flops which allow the mainframe CPU to set up the state of the emulation system. Whenever the mainframe is powered up, the registers are cleared due to the low present at the pin 1 reset inputs (generated via mainframe LPOP). The registers are loaded

whenever the mainframe CPU writes to address range 4XXX hex (LSEL, LSTB asserted, LID negated); the data is latched on the rising edge of the pin 13 output of mainframe command decoder U43 as the cycle terminates.

8-37. LMSYNC Logic. U56A and open collector NAND gate U57A implement the LMSYNC drive logic. When the mainframe cycle starts, the LSEL and LSTM signals are asserted, driving the pin 1 output of U56A high. Since LSTB is high, LMSYNC is pulled low by U57A. The mainframe CPU then asserts LSTB to complete the transaction; this negates LMSYNC and allows the cycle to terminate.

8-38. LWPOD logic. Buffer U55, open-collector NAND gate U57D and gates U56C, U56D implement the logic used to generate a data write strobe for data transferred from the mainframe to the emulation pod. As the write cycle begins, the LSEL signal is asserted, LID is negated. This places a high on the pin 13 input of U57D through U56D. LSTM goes low, placing a low on the pin 8 input of U56C. When the pin 14 output of mainframe command decoder U43 is driven low (write to 6XXX hex, LSEL, LSTB true, LID false), then a high is applied to the pin 12 input of U57D, causing U57D's output to go low and subsequently asserting LWPOD through U55.

8-39. SERVICE SHEET 2.

8-40. Service Sheet 2 (Figure 8-4) shows the circuitry which interfaces the emulation pod address and data buses to the emulation system. Also shown is the high-speed mapper RAM, which controls buffer direction for user and emulation data transactions.

8-41. Data Latches (from Pod). U23, U24 and U31 are octal tri-state data latches used to selectively transfer data from the emulator pod to the emulation system.

For 16 bit emulators, the 8 BIT signal will be false, gating off latch U31. During emulator writes to emulation memory and all transactions with the user system, the LEMULRD and LWPOD signals will be high, enabling U23 through U27B and U24 through U27D and U58A. This allows data on the LDE0-15 bus to be seen on the LED0-15 bus.

Eight bit emulators use only the LDE0-7 bits on the emulator side; however, either the LED0-7 or LED8-15 lines may be used on the emulation system sided dependent on the state of the byte upper and lower strobes from the pod. When transferring data, the 8 BIT signal will be high; when LEMULRD and LWPOD are false for a write transaction or user transaction, the data on LDE0-7 will be seen by both LED0-7 and LED8-15 through U23 and U31, respectively.

8-42. Data Buffers (to Pod). U14, U16 and U32 are octal tri-state buffers used to transfer data from the emulation system to the emulator pod. These buffers are activated during emulation processor read memory cycles and during writes by the mainframe CPU to the emulation pod programmable registers.

Sixteen bit emulators use U14 and U16 for the transactions. U32 is gated to three-state off by the 8 BIT signal through NAND gate U46A. During a write to the pod by the mainframe CPU, LWPOD will be true; a read from emulation memory causes LEMULRD to be true. The assertion of either of these signals causes the pin 3 output of U58A to go low, enabling buffer U16; the pin 8 output of U27A is also low (derived from U27B) causing U14 to be enabled. This permits data from the LED0-15 bus to be transferred to the LDE0-15 bus.

Eight bit emulators use buffers U14 and U32. The 8 BIT signal from the emulation control register will be high, setting up U46A and U19A. A write to the emulation pod or a processor read from memory will then enable either U14 or U32, dependent on the state of address bit LEA0. If LEA0 is low, U32 is enabled; if high, U14 is enabled. This transfers data from the appropriate byte of emulation memory to the processor's eight bit data bus.

8-43. Address Buffers. U7, U9 and U11 are octal inverting transceivers which provide signal conditioning between the emulation pod address bus and the emulation system address bus. The buffer enable lines are hardwired to ground, thus gating the buffers permanently "on".

8-44. Ready Mapper. The high-speed mapper RAM consists of CMOS RAM devices U17 and U18. These RAMs are programmed before an emulation run such that an address applied to the RAM inputs will cause the data line to swing high or low, indicating whether that address lies within an address range assigned to user address space or emulation address space.

Different sized blocks of addresses can be defined by selecting either U17 or U18 via the RESSEL line from the control board control register. When RESSEL is low, U17 is selected, dividing a 16 megabyte address space into 4096 possible address blocks 4096 locations deep; a high on RESSEL selects U18, which divides a 1 megabyte address space into 4096 possible address blocks that are each 256 locations deep.

To program the mapper RAMs, the following steps occur: the mainframe CPU bus is translated through buffers U25 and U33 (schematic 1) to the address bus HEA8-23 of the mapper RAMs. This is done by asserting LSEL from the mainframe bus while LDEFIB from control register U52 is asserted. The mapper RAMs are selected in turn by the state of RESSEL; the write strobe for the RAMs is provided by LWPREADY from function select decoder U43. LD0 from the mainframe bus provides the data input to the RAMs.

When an address is applied to the RAMs in normal operation (LDEFIB false), the data output of the RAMs will swing high or low dependent upon the address range corresponding to the applied address. If low, the address lies within user address space, if high, it lies within emulation address space. Buffer U2 drives this signal to the emulation pod for use in buffer control there; U35 buffers the signal internally to the control board for use in the wait/acknowledge circuitry.

8-45. SERVICE SHEET 3A.

8-46. Service Sheet 3A (Figure 8-5) shows part of the circuitry used to generate the proper and control strobes for the emulation system from those supplied by the emulation pod.

8-47. Line Termination. U1 is a 220/270 pullup/pulldown pack used to lower the effective impedance of the line from the standpoint of the drivers at the emulation pod. This helps reduce signal reflections on the line and provides for cleaner signal transitions.

8-48. LWDV Circuitry. LWDV from the emulation pod provides timing for all writes to emulation memory by the emulation processor. The GP controller has provisions to select either normal timing for the LWDV strobe or a delayed timing.

When normal timing is selected, LWDV to emulation memory will follow the transitions of ELWDV from the pod. HWDSEL will be low; this resets monostable U34A and places a low on the pin 2 input of U29A. A low on ELWDV will place a high on the pin 1 input of U29A and release the reset input of U30B. Since U34A is reset, this places two highs on AND gate U28B, which causes a rising edge on the clock input of U30B, asserting the LWDV signal (the D input is tied high; LWDV is taken from the Q/ output). Returning ELWDV to the high state causes the pin 13 reset input of U30B to be asserted, negating LWDV and terminating the write transaction.

In some cases, the ELWDV strobe provided by the pod may need to be delayed to provide additional data set-up time for the memory boards. To accomplish this, the HWDSEL bit from the control register is set, allowing monostable U34A to function. When ELWDV swings low, a high is placed on the pin 4 trigger input of U34A and also on the pin 1 input of U29A. In addition, the reset input of U30B is released. Triggering U34A causes its pin 7 output to swing low for approximately 80 nanoseconds; when pin 7 returns high, a rising edge will appear on the output of U28B, clocking a high into U30B and asserting LWDV. When ELWDV returns high, U30B is reset, negating LWDV and terminating the cycle.

8-49. Upper and Lower Byte Strobes. The emulation system requires two strobes to indicate utilization of the 16 bit data bus by the current memory cycle. These strobes are LEBYTE and LEBUP from buffer U35 on the GP Control Card. If both strobes are high, the current cycle is a word transaction; if LEBYTE is low, the current cycle is a byte transaction, with LEBUP being used to indicate which byte (upper or lower) is active.

These strobes are generated by a gating network driven by the emulation pod BYTE and BUP signals. The signals enter the control board on J1 and are buffered by U2 before being input to exclusive OR gates U20C and U20D. These gates, along with the BUPPOL and BYPPOL signals from the emulation control registers, are used to program for the desired polarity of BYTE and BUP signals from the pod. If the strobes from the pod are active low, BUPPOL and BYPPOL will be set low and vice-versa.

When emulating a processor with an eight bit external bus, such as the 8088, the 8BIT signal from the emulation control register will be set. This effectively gates the LEBYTE signal permanently on and allows the LEA0 address bit to drive the LEBUP signal through U21A and U21D. When LEA0 is high, the lower byte is used; when low, the upper byte is used.

8BIT is negated for processors with 16 bit external data buses. For these processors, a choice of byte strobe modes is provided. Some processors use separate data strobes to indicate that either the upper or lower byte is to accessed in the current cycle (examples: 68000, 8086). Others use a byte/word strobe and the least significant address strobe, similar to the emulation bus scheme, to indicate which byte should be accessed (example: Z8000). To accomodate these differences, the SEPBYT signal from the pod control register is used.

When SEPBYT is low, a processor like the Z8000 with a byte/word select and upper/lower byte strobe is accomodated. The BYTE and BUP strobes from the pod are passed directly to LEBYTE and LEBUP; no further qualification is necessary.

When SEPBYT is high, processors like the 68000 and 8086 with upper and lower byte strobes are accomodated. If both BYTE and BUP are true, indicating a word transaction, then both inputs to U29C will be low, which places a low on the pin 9 input of U29C, negating LEBYTE. LEBUP is asserted; however, it is a don't care since a word transaction is indicated. If only BYTE is true, then LEBYTE is asserted by the pin 11 output of U58D. BUP is false, so the LEBUP signal is negated. If only BUP is true, then both LEBYTE and LEBUP are asserted.

8-50. HMAV Circuitry. The assertion of EHMAV from the emulation pod indicates that the emulation processor is not currently executing a memory cycle; thus, the mainframe CPU may be allowed to access emulation memory for the purpose of reading or modifying memory locations.

EHMAV enters the control board and is buffered and inverted by U3 to form LMAV before being applied to the pin 4 input of U19B. The pin 5 input of U19B is driven by a buffered and inverted version of the ENSTB signal, which is also provided by the emulation pod. When ENSTB is high, it indicates that the emulation processor is performing a bus cycle which does not reference a memory location; therefore, HMAV to the emulation bus should be asserted, regardless of the state of EHMAV. The pin 6 output of U19B drives the HMAV output to the emulation bus and becomes asserted whenever either EHMAV or ENSTB is asserted.

The emulation analysis strobe, LANAL, is also derived from the pod EHMAV signal through buffer/inverter U2. This line drives the emulation bus directly; it is also used to provide timing for the last address latches resident on the control board (Service Sheet 3B).

Monostable multivibrator U34B uses the LMAV signal to provide the LOWSLOWCLOCK indication to the status buffer. When no memory cycles occur for a 150 microsecond period, the circuit times out and asserts the LOWSLOWCLOCK signal.

R4, C11, and L1, along with buffers U5 and U3, forms the delayed memory cycle indication signal. This line (output from U3 pin 9) is an inverted version of EHMAV from the pod which has been delayed to allow the pod circuitry time to set up address and data lines. The delayed cycle indication is used to clock the last address register (Service Sheet 3B).

ENSTB is gated with the delayed memory cycle indication in U28D to form the LMAVD signal. LMAVD mirrors the transitions of HMAV to the emulation bus with a short delay in between transitions of HMAV and LMAVD. The signal is used to provide start of memory cycle indication to the wait state insertion circuitry.

LMAVD is ANDed with the PREADY signal from the mapper RAMs and the LEMWRT write status signal from the emulation pod to provide indication of emulation processor reads from an emulation memory location. That is, when LEMWRT is high (not write), PREADY is high (emulation space), and LMAVD is high (memory cycle in process), the pin 8 output of U46C will be driven low, asserting the LEMULRD signal and the HEMULRD signal to the pod through buffer/inverter U12. These signals are used to control the buffers both on the GP Control board and the emulator pod so that the data from the selected emulation memory location will be guided to the emulation processor.

U58B ORs together the LMAV and LDEFIB signals to set up the fast wait signal to the emulation pod (Service Sheet 3B).

8-51. Refresh Acknowledge. Gates U45C, U37A and buffer U3 implement the refresh acknowledge circuitry. On an emulation memory board that uses dynamic memory, the memory must be refreshed at regular intervals. The memory will request the refresh; the pod responds by driving the LDMACK line, which in turn drives the HREFAC line to the memory boards, indicating that refresh can proceed. Currently, none of the emulation memory boards use dynamic memory; therefore, this function is not implemented.

8-52. Analysis Status Buffer. The ESTAT3-7 lines from the emulation pod enter the GP Control Board on J5 and are terminated by pullup/pulldown resistors in U4, which lower the effective impedance of the signal line, providing signal conditioning. The lines then drive buffer U5, which passes the signals to the emulation bus as LES3-7. LES2 and LES1 are driven by delayed versions of the LEBUP and LEBYTE signals, respectively; the delay is necessary to provide additional hold time for the analysis modules. LES0 is driven by buffer U35, which passes the LEMWRT signal from the emulation pod to the status bus. LEMWRT is also driven by another segment of U35 to the emulation bus for use on the memory controller.

8-53. SERVICE SHEET 3B.

8-54. General. Service Sheet 3B (see Figure 8-6) shows the remainder of the timing circuitry on the GP Control Board, including the wait/acknowledge circuitry and the emulation break circuits.

8-55. Break Circuitry. A high-to-low transition on either the LBREAK signal from the emulation bus or the LBPCBRK signal from the emulation control register will clock a high into the Q output of J-K flip-flop U22A. The break signal to the pod will then be asserted through buffer U35 after being polarity selected via exclusive-OR gate U37D and the BRKPOL signal. The output of U28A, in addition to driving the clock line of U22A, also drives open-collector NAND gate U57C through buffer/inverter U44. If the INTEN signal from the control register is true, any activity on the LBPCBRK or LBREAK lines will assert the LIR1 interrupt line to the mainframe; this alerts the emulation software that an emulation break request has occurred.

8-56. Halt Requests. The emulation software may require that the emulation processor be halted so that inspection and modification of emulation memory locations under mainframe CPU control can be accomplished without interference from the emulation processor. Or, an emulation memory board

containing dynamic memory may wish to halt the processor so that refresh cycles can be performed without interference from memory access requests. (Note: this function is currently not used). In the former case, the HALT output from the control register is asserted, which asserts the HALT line to the emulation pod. If refresh is desired, the LREFREQ line will be asserted, asserting EHALT to the pod.

8-57. Last Address Latch Clock. A low-to-high transition on the SETLAS line, output from U45B, latches the address currently present on the inputs of the last address registers into those registers. The SETLAS line can be toggled from many sources.

During normal operation, the SETLAS line is activated by the combination of NAND gate U45D and flip-flop U30A. When a memory cycle starts, the delayed memory cycle indication (input to U45D pin 13) will go high, enabling U45D. At the end of the cycle, the LANAL strobe will rise, clocking a high into U30A, which propagates through U45D and U45B to assert the SETLAS line. If a break occurs, the LMBRKS status line will go low immediately after the cycle that caused the break. Any LANAL cycles which occur after this clock lows into U30A, which inhibits toggling of SETLAS and allows the mainframe CPU to determine the address which caused the invalid access and thus the memory break.

During writes to the mapper RAMs, the LWPREADY line will toggle low, thus asserting the pin 14 reset input of flip-flop U22B. This forces the Q output of U22B low, which asserts the SETLAS signal. The Q output feeds back to the pin 10 set input of U22B through the delay network formed by resistor R8 and capacitor C15. Now the Q output will be forced high; SETLAS is negated. Note that because of the OR function implemented by U28C, the PODADDL signal from the pod can also assert SETLAS in the manner described above.

Reading information from the emulation pod can also toggle the SETLAS line; in this mode, the LRDPOD signal sent to the pod clocks a low into U22B, asserting SETLAS; the SETLAS cycle terminates via the RC network explained previously.

8-58. Write Signals. Buffer U2 provides additional drive for the signals needed to write information into emulator pod registers; these are the LWRPCTR and LWPOD lines.

8-59. Wait/Acknowledge Circuitry. Various programmable configurations are available to send signals to the emulation pod indicating that emulation memory is ready to complete the requested transaction.

If the emulation processor operates with a wait signal, i.e. wait until memory is ready, then the WAITEN and HWAITEN/LACKEN signals from the control register will be programmed high, asserting the pins 5 and 6 inputs of AND-OR-INVERT gate U36. Assuming that the pod is looking for an active low wait signal, the pin 5 input of polarity selecting gate U37B will be programmed low by WAITPOL. Shortly after the memory cycle starts, the PREADY line will settle, indicating whether this cycle references emulation memory or user memory. If emulation memory is indicated, the line will be high, placing a high on the D input of U48B. The LMAVD cycle strobe will clock this high into U48B, asserting the LWAIT line to the pod through U36, U37B and buffer U55. When emulation memory is ready to complete the cycle, it will assert the HREADY line to the emulation bus. This fires monostable U49; the Q/ output of U49 clears U48B and negates the wait condition.

If the emulation processor operates with an acknowledge strobe; i.e. latch data from memory when the strobe occurs (example: 68000), then the WAITEN signal is high, the HWAITEN/LACKEN signal is low. This places two highs on the pin 11 and 12 inputs of U36 (LACKEN is inverted by U44). Assuming an active low acknowledge, WAITPOL will be programmed low as before. When the memory cycle starts, U48A has been cleared by the action of LMAV (refer to Service Sheet 3A). This holds off the acknowledge signal. If emulation memory is indicated by the PREADY line, then a high is applied to the pin 1 input of U36; a low is applied to the data input of U48A through inverter U44. This low is clocked into U48A by LMAVD, further holding off the acknowledge. When emulation memory becomes ready, the HREADY signal is asserted, firing U49 and forcing the pin 4 set input of U48A true. The Q output goes high, which completes

the enabling of U36 and sends the acknowledge strobe to the pod. When the memory cycle terminates, the strobe is terminated since LMAV clears U48A.

Some emulators, such as the Z8000, require additional setup time on their wait input; there is not time for the mapper RAM to determine the location of the memory reference. In these cases, a fast wait assertion is provided by U29D through buffer U55. For these pods, the LFASTWT signal from the control register will be programmed low. When the memory cycle starts, U48A has been cleared by the action of LMAV. This asserts the fast wait signal. If emulation memory is indicated by PREADY, a low is applied to the data input of U48A and clocked into the Q output by LMAVD. When emulation memory is ready, HREADY will be brought high, firing U49, which presets U48A and negates the fast wait condition.

8-60. LOGIC CONVENTION.

8-61. The circuits contained in the Model 64271A General Purpose Control Board use a combination of both positive and negative logic. The following definitions are necessary to properly understand positive and negative logic:

0-state -- the logic state which represents a false or negated logic condition.

1-state -- the logic state which represents a true or asserted logic condition.

Low level -- the more negative of two voltage levels chosen to represent logic states.

High level -- the more positive of two voltage levels chosen to represent logic states.

8-62. Given the above definitions, positive and negative logic are defined as follows:

```
Positive logic:  0-state = Low level voltage = negated
                 1-state = High level voltage = asserted

Negative logic:  0-state = High level voltage = negated
                 1-state = Low level voltage = asserted
```

8-63. The voltages representing the low and high levels within the Model 64271A are given as follows:

TTL Voltage levels

Level		Voltage
Input Low	(less than)	< 0.8 V
Input High	(greater than)	> 2.0 V
Output Low	(less than)	< 0.4 V
Output High	(greater than)	> 2.4 V

8-64. MNEMONICS.

8-65. Table 8-1 is a list of all mnemonics used on schematics for the 64271A. They are arranged in alphabetical order, with the mnemonic listed first, followed by the name of the signal and a description of its function and active state.

Table 8-1. Mnemonics

Mnemonic	Description
ACKPOL	Acknowledge Polarity -- Not used.
BRK	Break -- Output to pod from break circuitry requesting an interrupt of the emulation system. Active state polarity is software selectable via BRKPOL.
BRKPOL	Break Polarity -- output from control register U41 selecting active state polarity of the BRK signal. When high, the BRK output is active low; and vice- -versa.
BUP	Byte Upper -- Input from emulator pod which indicates that the upper byte bank of memory is to be used for the impending byte transaction. BUPPOL determines whether the byte enabling logic will respond to a high or low on this input.
BUPPOL	Byte Upper Polarity -- Output from U41 control register determining how the byte enabling logic responds to BUP. When low, BUP is seen as an active low signal, and vice-versa.
BYPPOL	Byte Polarity -- Output from U41 control register determining how the byte enabling logic responds to BYTE. When low, BYTE is seen as an active low signal, and vice-versa.
BYTE	Byte -- Input from the emulator pod which indicates that the impending data transfer is a byte operation rather than a word operation (Z8000); or that the the transaction involves the lower byte of memory (68000, 8086). BYPPOL determines whether this signal is seen as active high or active low.
EHALT	Emulator Halt -- Output to the pod requesting a halt of processing activity. May be an active high or active low signal, selectable by HALT.
EHMAV	Emulator High Memory Available -- Input from the emulator pod. When high, indicates that the pod is not accessing memory.
ELWDV	Emulator Low Write Data Valid -- Input from the pod. When low, the emulation processor has placed valid write data on the bus.
ENSTB	Enable Strobe -- Input from pod. The pod holds this line low during normal processor memory operations thus enabling HMAV to function normally. When high, the processor is doing an I/O or other form of operation, and HMAV is inhibited. LANAL, however, is not affected, causing I/O cycles to be stored on the analysis board.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
ESTAT 3-7	Emulator Status 3 through 7 -- Input from the pod indicating status.
HALT	Halt -- Output of control register U41. Requests emulator pod to halt processing. May be active high or active low, as determined by software.
HBUSGTIN	High Bus Grant Input -- Input from pod to status buffer U53. When high, the emulation processor has granted its bus for a DMA or coprocessor type of cycle.
HEA 0-23	High Emulator Address 0 through 23 -- Input from pod to address buffers U7,9,11. This address bus has the same polarity as the output from the emulation processor.
HEMULRD	High Emulation Read -- Output to pod from buffer gating logic. When high, indicates that the emulator pod will read emulation memory.
HHALTIN	High Halt Input -- Input from pod to U53 status buffer. When high, the emulation processor is in a halted state.
HPREADY	High Pre-Ready -- Input to wait state generator U36,48,49, from the emulation bus indicating that emulation memory is ready.
HREFAC	High Refresh Acknowledge -- Not used.
HRESETIN	High Reset Input -- Input from pod to U53 status buffer. When high, indicates that the emulation processor is in a reset state.
HWAITEN/LACKEN	High Wait Enable/Low Acknowledge Enable -- Output from control register U52 and input to the wait state generator. When low, and WAITEN is high, the wait generator functions in the acknowledge mode. When high, and WAITEN is high, the wait generator functions in the wait/ready mode.
HWAITIN	High Wait Input -- Input from pod to U53 status buffer. When high, indicates that the emulation processor is in a wait state.
HWDSEL	High Write Delay Select -- Output of control register U52. When high, the leading edge transition of LWDV is delayed approximately 100ns from the same transition of ELWDV.
ID 0-7	Identification 0 through 7 -- Input from pod to ID buffer U50. ID 0-4 indicate what type of emulator pod is connected to the control board; while ID 5-7 indicate that the control board is plugged into the mainframe.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
INTEN	Interrupt Enable -- Output of control register U41. Used in the break circuitry to enable an interrupt of the mainframe. LIR1 will be enabled when INTEN is high.
LA 0-13	Low Address 0 through 13 -- Mainframe (mainframe CPU) address bus. Input to address buffers U25,33 which translate this address into HEA 8-23 for use in programming the ready mapper. LA 12,13 are also used in mainframe command decoder U43.
LANAL	Low Analysis -- Output from memory available logic to the emulation bus. When a low-to-high transition occurs, the analysis board is instructed to record data present on the address, data, and status buses.
LBPCBRK	Low BPC Break -- Output of control register U52. Input to break logic. When a high-to-low transition occurs, the BPC is requesting an interrupt of the emulation system.
LBREAK	Low Break -- Input to the break logic from the emulation bus. When a high-to-low transition occurs, an emulation bus device is requesting an interrupt of the emulation system.
LD 0-15	Low Data 0 through 15 -- Mainframe (mainframe CPU) data bus. Used to program control registers U41,52; read status and ID buffers U50,53, last address latches U39,40,51; and transmit/receive data through bi-directional buffers U42 and 54.
LDE 0-15	Low Data Emulator 0 through 15 -- Bi-directional data bus between the emulator pod and control board. This bus is inverted from that of the emulation processor.
LDEFIB	Low Defibrillate -- Output of control register U52, used internal to the control board and buffered output to the pod. When low, used to reset appropriate devices on the control board and pod.
LDMACK	Low Direct Memory Access Acknowledge -- Not used.
LEA 0-23	Low Emulation Address 0 through 23 -- Output of address buffers (U7,9,11) to the last address latches (U39,40,51) and the emulation bus.
LEBUP	Low Enable Byte Upper -- output from the byte enabling logic to the emulation bus. When low, indicates that the upper byte of the data bus is to be used for the impending byte transfer operation.
LEBYTE	Low Emulation Byte -- output from the byte enabling logic to the emulation bus. When low, indicates that the impending data transfer is a byte operation rather than a word operation.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LED 0-15	Low Emulation Data 0 through 15 -- bidirectional data bus, connected to data buffers U14,16,23,24, 31,32,42,54 and to the emulation bus. This bus is primarily used for transferring data to and from emulation memory.
LEMULRD	Low Emulation Read -- Output to the control board circuitry from the buffer gating logic. When low, indicates that the emulation processor will be reading data from emulation memory.
LEMWRT	Low Emulator Write -- Input to control board from emulator pod. When low, indicates that the pod is doing a write cycle.
LES 0-7	Low Emulation Status 0 through 7 -- Output to the emulation bus from buffers U5,35 indicating status of the emulator pod; lower and upper byte enabling logic; and write cycle status.
LEWRT	Low Emulation Write -- Output to the emulation bus indicating that the emulator pod is in a write cycle.
LFASTWT	Low Fast Wait -- Output from control register U52 to the wait state generator. When low, the fast wait signal to the pod is enabled, allowing sufficient setup time on the emulation processor's wait line for accesses to emulation memory that require wait states.
LFWEN	Low Fast Wait Enable -- output to the emulation pod from buffer U55. When low, indicates that the wait line to the emulation processor should be asserted immediately.
LICE	Low In-Circuit Emulation -- Input to status buffer U53. When low, indicates that the emulator pod is plugged into a powered-on user target system.
LID	Low Identification -- Input to the mainframe command and control logic. When low, allows the control board to gate ID 0-7 onto the mainframe CPU data bus via U50 if both LSTB and LSEL are true (active low).
LIR1	Low Interrupt Request 1 -- Output of the break logic to the mainframe bus. When low, requests an interrupt of the mainframe.
LMAV	Low Memory Available -- Internal to the memory available logic. When low, indicates that the emulator pod is not using memory.
LMAVD	Low Memory Available Delayed -- Output of memory available logic, used to drive buffer enabling logic and the wait state generator. This is a delayed and inverted version of HMAV.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LMBRKS	Low Memory Break Status -- Input to status buffer U53 from the emulation bus. When low, indicates that the memory controller board has asserted a break.
LMSYNC	Low Memory Sync -- Output to the mainframe CPU (mainframe) bus. When low, the mainframe CPU must wait until the selected card can complete the read or write operation.
LOWSLOWCLOCK	Low Slow Clock -- Input to the status buffer U53 from the memory available logic. When low, indicates that the pod is not doing memory cycles.
LRDPOD	Low Read Pod -- Output to the emulator pod. When low, data is read from the pod.
LREFREQ	Low Refresh Request -- Not used.
LSEL	Low Select -- Input to the mainframe command and control logic from the mainframe CPU (mainframe) bus. When low, the card is being selected by the mainframe CPU.
LSTB	Low Strobe -- Input to the mainframe command and control logic from the mainframe CPU (mainframe) bus. When low, (mainframe CPU write), indicates that the data bus holds valid data. When low (mainframe CPU read), indicates that the mainframe CPU has freed the data bus for the addressed device to drive it.
LSTM	Low Start Memory -- Input to the mainframe command and control logic. When low, information on the mainframe address bus is valid.
LUSER	Low User -- Output of the high speed ready mapper to the pod. When low, indicates that the current address resides in space mapped to user memory.
LWDV	Low Write Data Valid -- Output to the emulation bus from the write delay generator. When low, indicates that valid information has been placed on the data bus by the emulation processor.
LWPCTR	Low Write Pod Control Register -- Output to pod from mainframe command and control. When low, information on the data bus to the pod is latched into the pod control register.
LWPOD	Low Write Pod -- Output from mainframe command and control. Used in data bus enable logic; also buffered to the pod as LWRTPOD. When low, data is transferred from the control board to the pod.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LWPREADY	Low Write Pre-Ready -- Output of mainframe command decoder U43 to high speed ready mapper. When low, data is written into the ready mapper.
LWRT	Low Write -- Input to mainframe command and control logic from the mainframe CPU (mainframe) bus. When low, the mainframe CPU will write to the addressed device.
LWRTPOD	Low Write Pod -- Buffered output to the pod of LWPOD. When low, data is transferred from the control board to the pod.
PODADDL	Pod Address Load -- Input from the pod to the last address logic. A low-to-high transition on this input causes information to be latched into the last address registers. Used only for performance verification.
PREADY	Pre-Ready -- Output of the high speed ready mapper to the wait state generator and the data buffer enable logic. When low, current address is in user memory space. When high, current address is in emulation memory space.
RESSEL	Resolution Select -- Output of U52 control register to the ready mapper. When high, ready mapper is selected for 256 byte block resolution. When low, ready mapper is selected for 4096 byte block resolution.
SEPBYT	Separate Byte -- Output of U41 control register, selecting mode for byte/word enabling logic. When low, BYTE and BUP function as upper and lower byte strobes (if both are activated, indicates a word transaction). When high, BYTE functions as a byte/word indicator; BUP functions as a byte upper/lower select line.
SETLAS	Set Last Address Latches -- Output of the last address control logic to the clock input of the last address registers (U39,40,51). A low-to-high transition on this line loads the current emulation address into the last address latches.
WAIT	Wait -- Output to the emulator pod from the wait state generator which tells the pod that emulation memory is not ready. Alternatively, this line may function as an acknowledge signaling that the data transfer is complete.
WAITEN	Wait Enable -- Output of U52 control register. When high, the wait state generator is enabled.
WAITPOL	Wait Polarity -- Input to wait state generator from U41 control register. Determines active state of the wait line. When low, WAIT is active high, and vice-versa.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
8 BIT	8 Bit -- Output of U52 control register and input to byte enabling logic and data buffer enable logic. When high, indicates 8 bit data bus mode.

Table 8-2. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

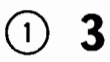
SCREWDRIVER ADJUSTMENT

ELECTRICAL TEST POINT
TP (WITH NUMBER)

NUMBERED WAVEFORM
NUMBER CORRESPONDS TO
ELECTRICAL TEST POINT NO.

LETTERED TEST POINT
NO MEASUREMENT AID
PROVIDED

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.



NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS

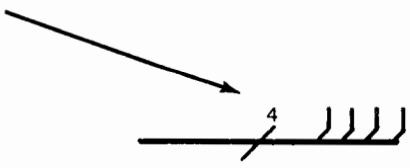


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Table 8-3. Logic Symbology

ENERAL

signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and puts on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

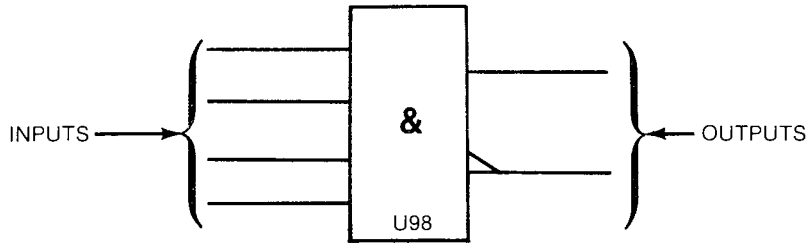
dependency notation is read from left to right (relative to the symbol's orientation).

external state is the state of an input or output outside the logic symbol.

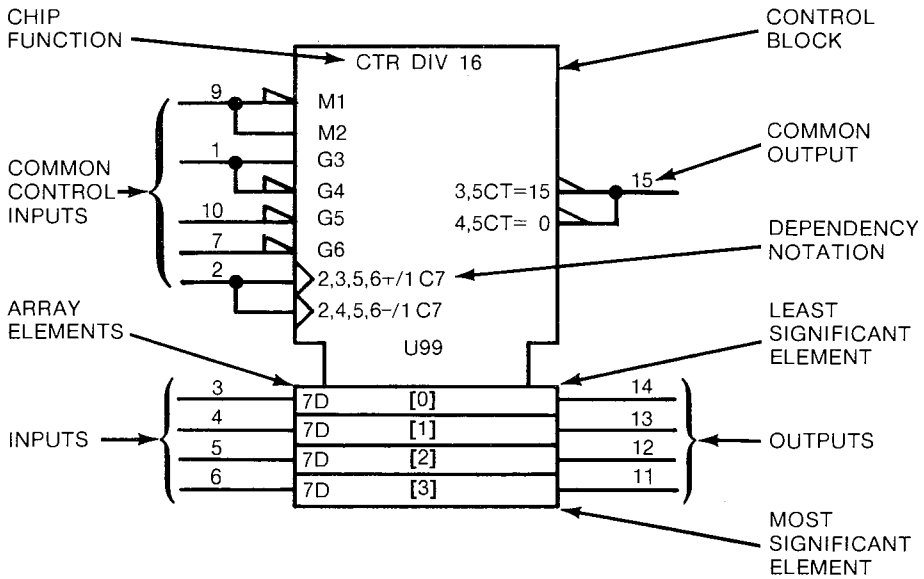
internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

MBOL CONSTRUCTION

me symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the resentation of input and output lines.



ne have a common Control Block with an array of elements:



NTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are ated in the control block. (Control blocks may be above or below the array elements.)

RAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. array element is independent of all other array elements. Unless indicated, the least significant element is always sest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers (shown in **[ ]**).

INPUTS - Inputs a

Common contr
according to th

Inputs to the ar
closest to the c

OUTPUTS - Outp

Common contr

Outputs of arra
the control bloc

CHIP FUNCTION

DEPENDENCY

Dependency nota

Dependency nota
common relations
2,3,5,6+/1,C7 is re
count....or (/) the i

The following type

a. AND (G
combina

b. Intercon

c. Control
controll

d. Set (S) a
input sta

e. Enable (
outputs

f. Mode (M
outputs

g. Address

h. Transmi
transmis

A Address (
C Control (
EN Enable (p
G AND (per
M Mode (se

Table 8-3. Logic Symbology (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

ir dependency notation.

outputs to the array elements

th the least significant element

y their dependency notation.

e least significant bit closest to

MUX - multiplexer.

ntation.

and outputs. Signals having a
rols D. Dependency notation
e counter to increment by one
D flip-flops.

en inputs and outputs in any

and indicates which inputs are

stable element when the R or S

uts are controlled by it (which

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complements state)
ut
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nection
ssion

Table 8-3. Logic Symbology (Cont'd)

OTHER SYMBOLS

∩	Analog Signal	⊾◿	Inversion	→	Shift Right (or down)
&	AND	○	Negation	/	Solidus (allows an input or more than one function)
} {	Bit Grouping	—✕—	Nonlogic Input/Output	▽	Three State
▷	Buffer	◇	Open Circuit (external resistor)	,	Causes notation and syn inputs/outputs in an AND rel occur in the order read from
!	Compare	◇	Open Circuit (external resistor)	( )	Used for factoring terms techniques.
▷	Dynamic	≥1	OR	[ ]	Information not defined.
=1	Exclusive OR	◇	Passive Pull Down (internal resistor)	Φ	Logic symbol not defined du
⊓	Hysteresis	◇	Passive Pull Up (internal resistor)		
?	Interrogation	⌐	Postponed		
—	Internal Connection	←	Shift Left (or up)		

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transiti
CG	Carry Generate	E	Extension (input or output)	+	Count U
CI	Carry Input	F	Function	–	Count D

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Ge
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Ac
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiv
BUF	Buffer	FF	Flip-Flop	ROM	Read Only
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Regist

DELAY and MULTIVIBRATORS

⊓⊓⊓	Astable	NV	Nonvolatile
100 ns	Delay	I	State of initial power
1⊓	Nonretriggerable Monostable	⊓_	Retriggerable Monosta

-3. Logic Symbology (Cont'd)

OTHER SYMBOLS

→	Shift Right (or down)
/	Solidus (allows an input or output to have more than one function)
▽	Three State
,	Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
( )	Used for factoring terms using algebraic techniques.
[ ]	Information not defined.
Φ	Logic symbol not defined due to complexity.

/Output
external resistor)
external resistor)
own (internal resistor)
p (internal resistor)
up)

LABELS

)	Carry Output	J	J Input
°	Carry Propagate	K	K Input
	Content	P	Operand
	Data Input	T	Transition
	Extension (input or output)	+	Count Up
	Function	–	Count Down

MATH FUNCTIONS

>	Greater Than
<	Less Than
CPG	Look Ahead Carry Generator
π	Multiplier
P-Q	Subtractor

CHIP FUNCTIONS

DIR	Directional	RAM	Random Access Memory
DMUX	Demultiplexer	RCVR	Line Receiver
FF	Flip-Flop	ROM	Read Only Memory
MUX	Multiplexer	SEG	Segment
OCT	Octal	SRG	Shift Register

ELAY and MULTIVIBRATORS

NV	Nonvolatile
I	State of initial power up
⎍⎍	Retriggerable Monostable

ole

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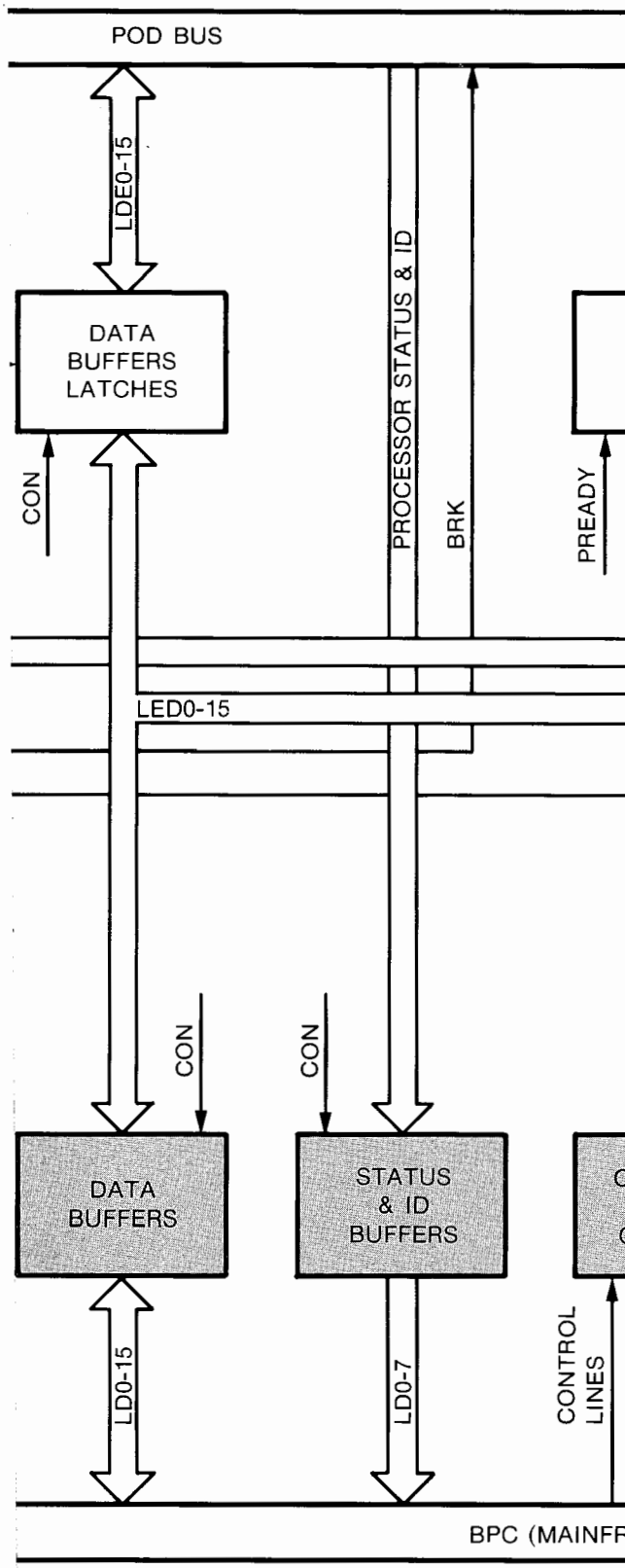
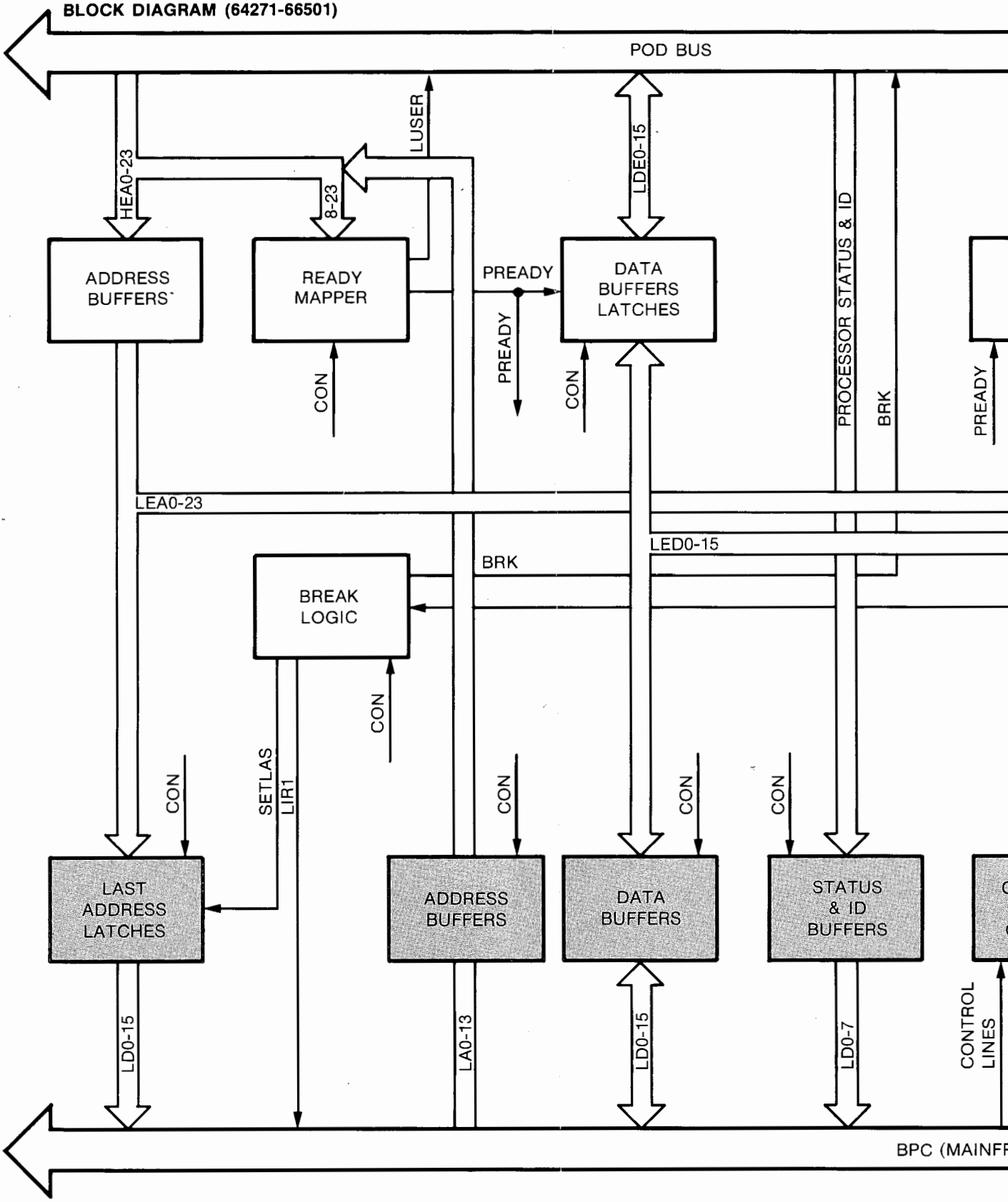
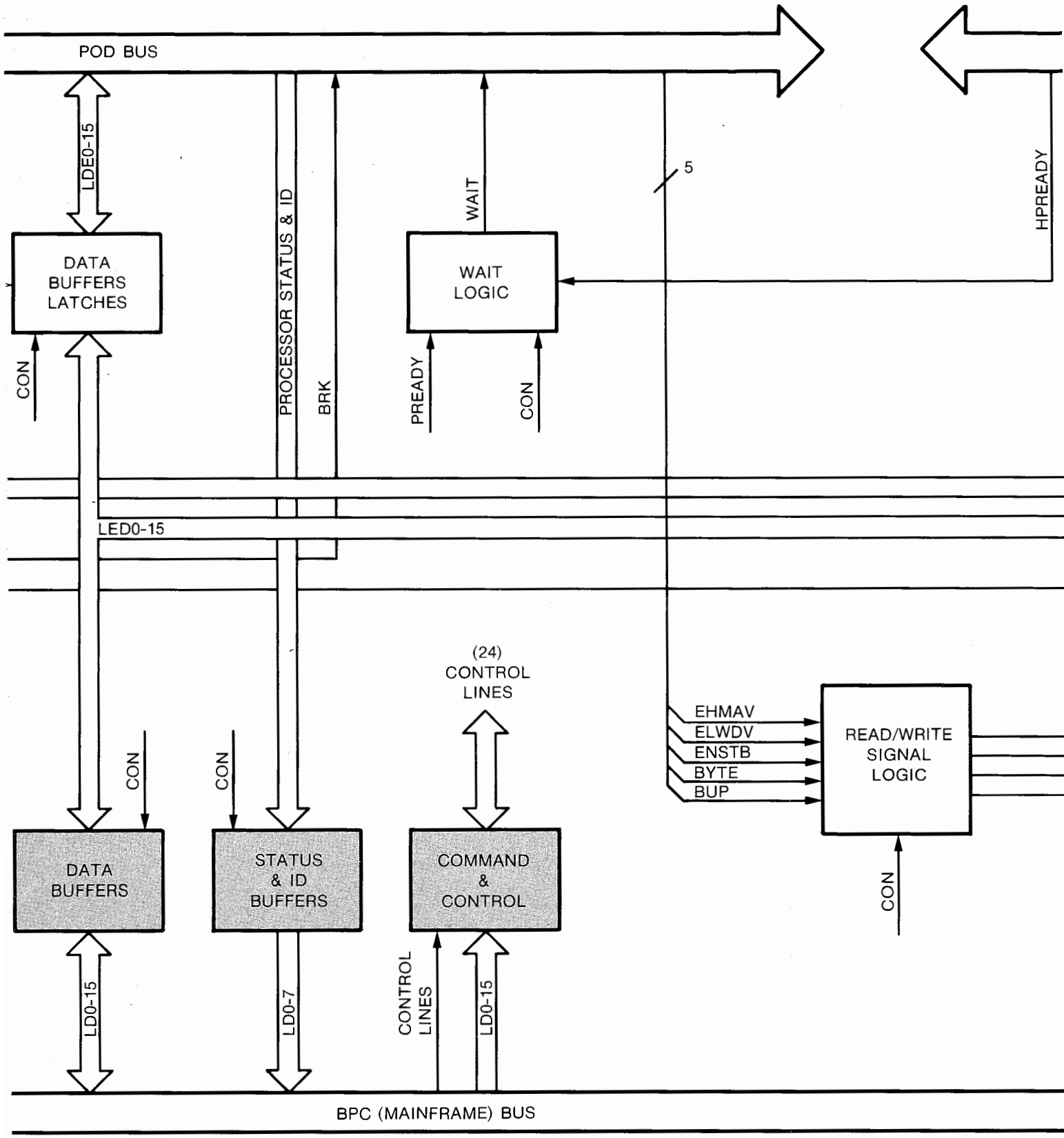
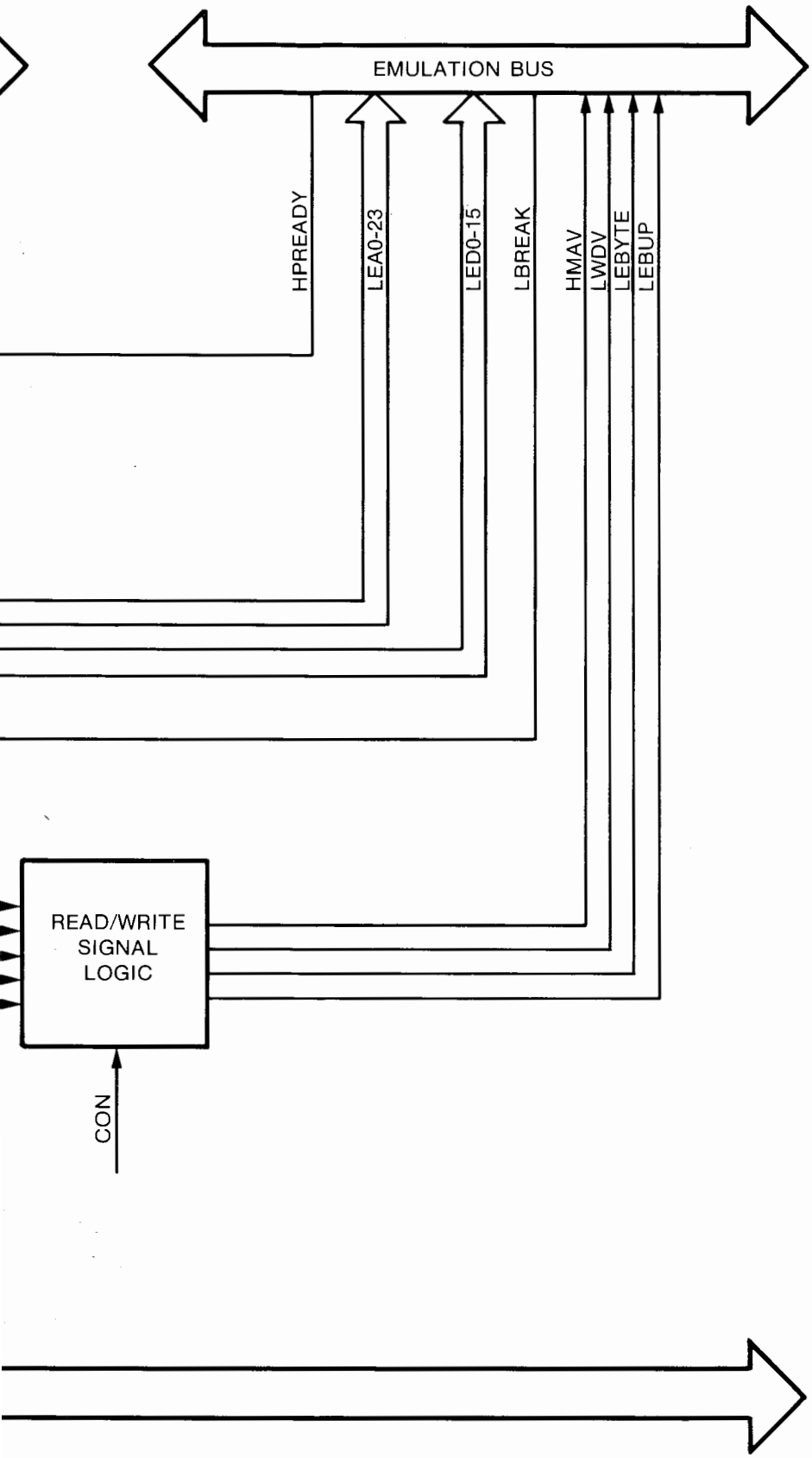


BLOCK DIAGRAM (64271-66501)




POD BUS
LDE0-15
DATA BUFFERS LATCHES
CON
PROCESSOR STATUS & ID
BRK
WAIT
WAIT LOGIC
PREADY
CON
5
HPREADY
LED0-15
(24) CONTROL LINES
EHMAV
ELWDV
ENSTB
BYTE
BUP
READ/WRITE SIGNAL LOGIC
CON
CON
CON
DATA BUFFERS
STATUS & ID BUFFERS
COMMAND & CONTROL
LD0-15
LD0-7
CONTROL LINES
LD0-15
BPC (MAINFRAME) BUS



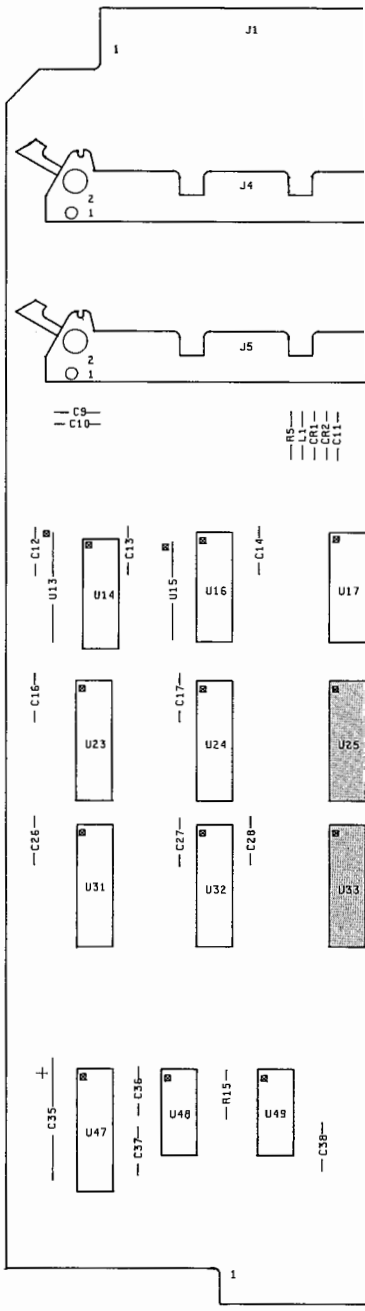


Figure 8-3.
Service Sheet 1, Mainframe

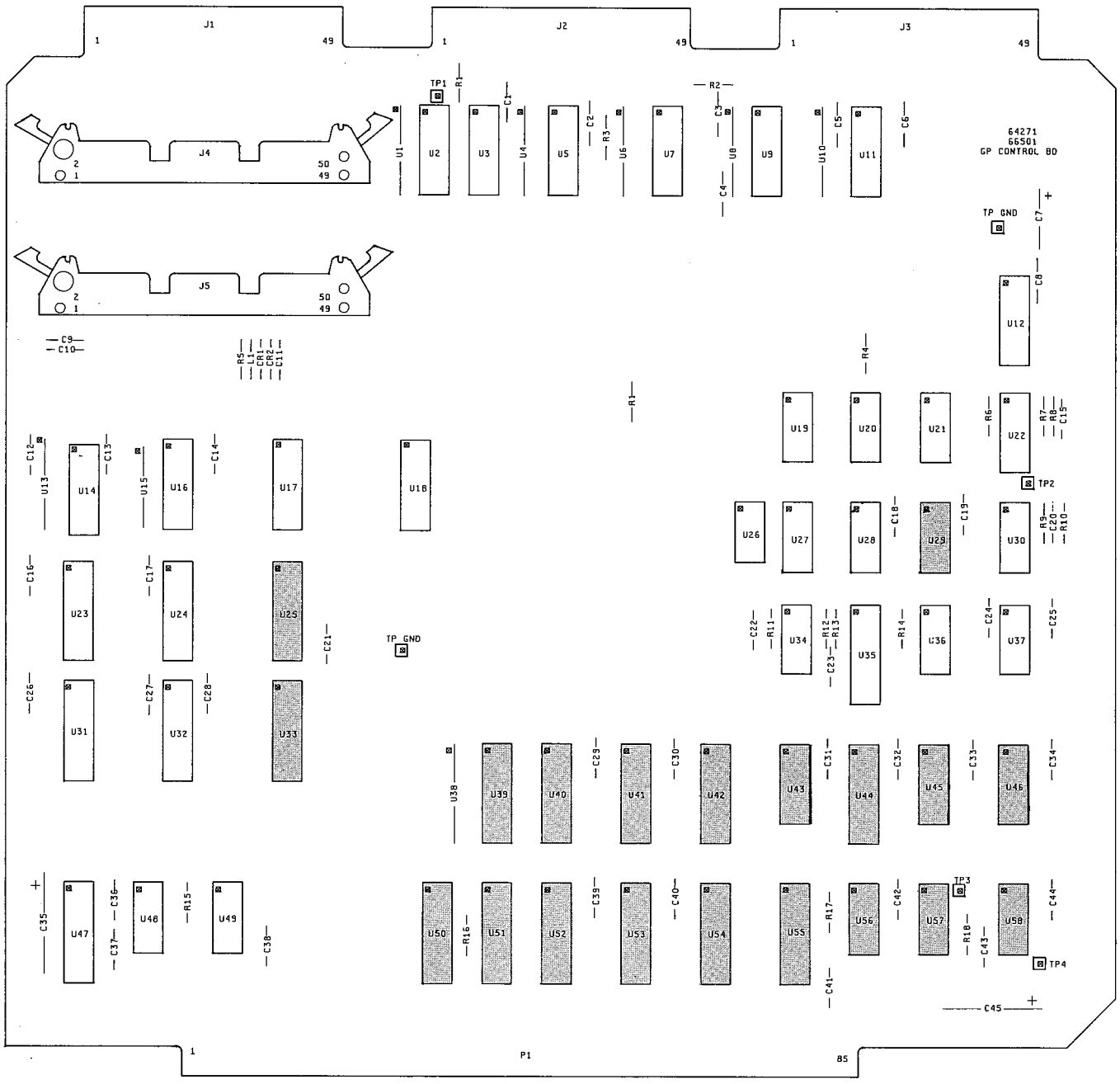
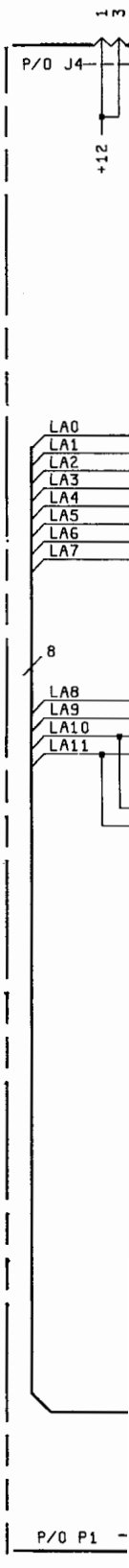
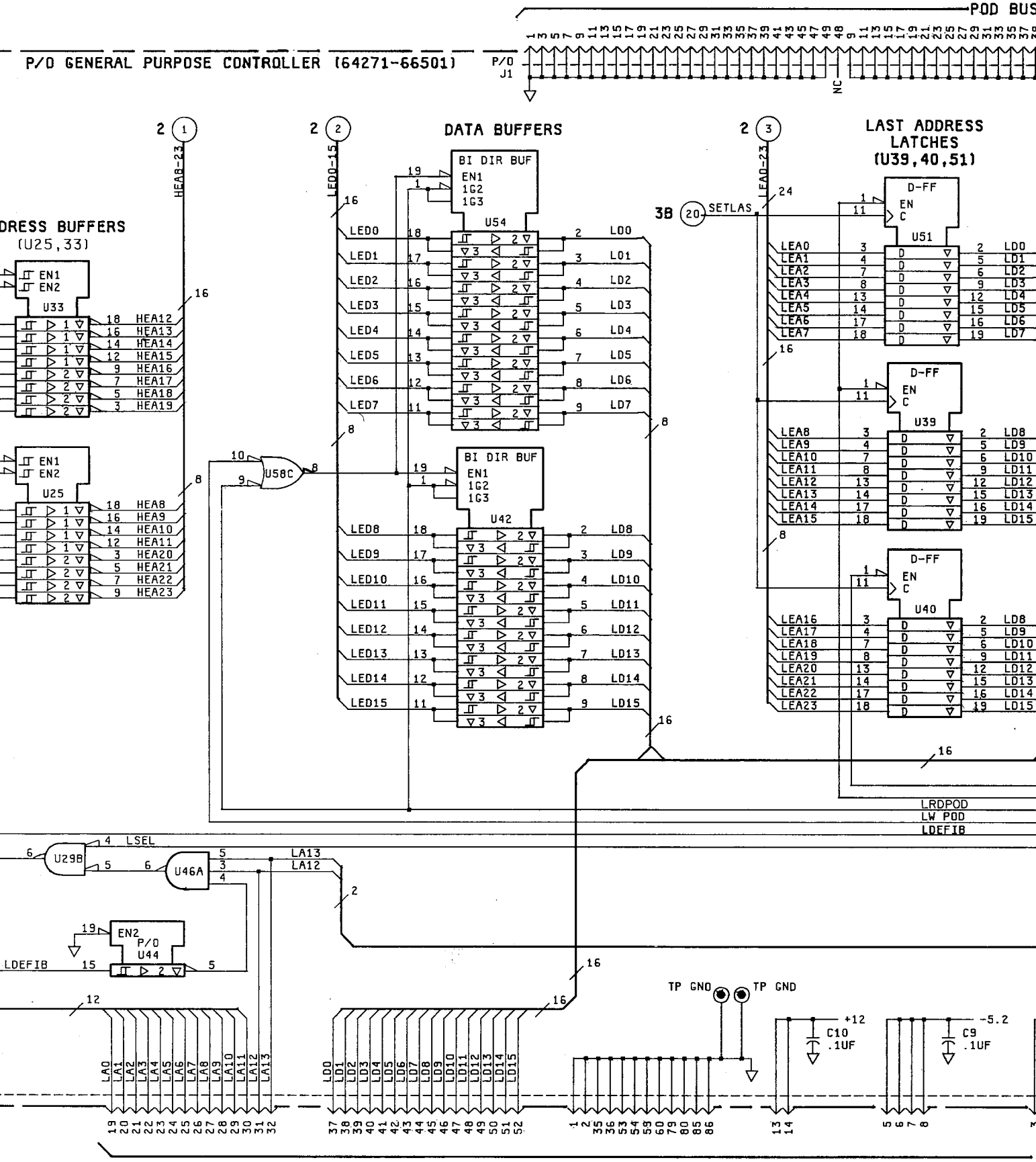
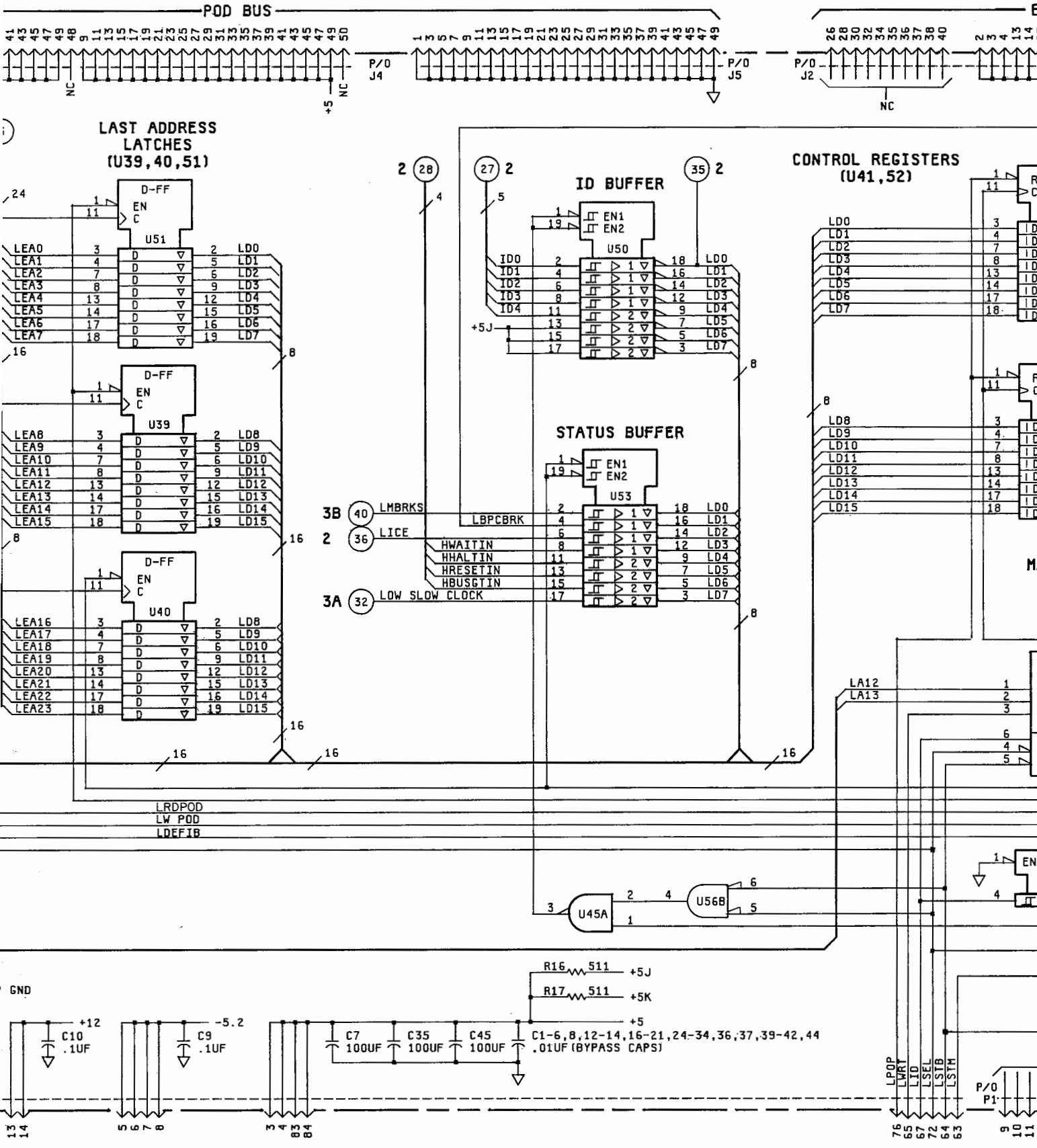
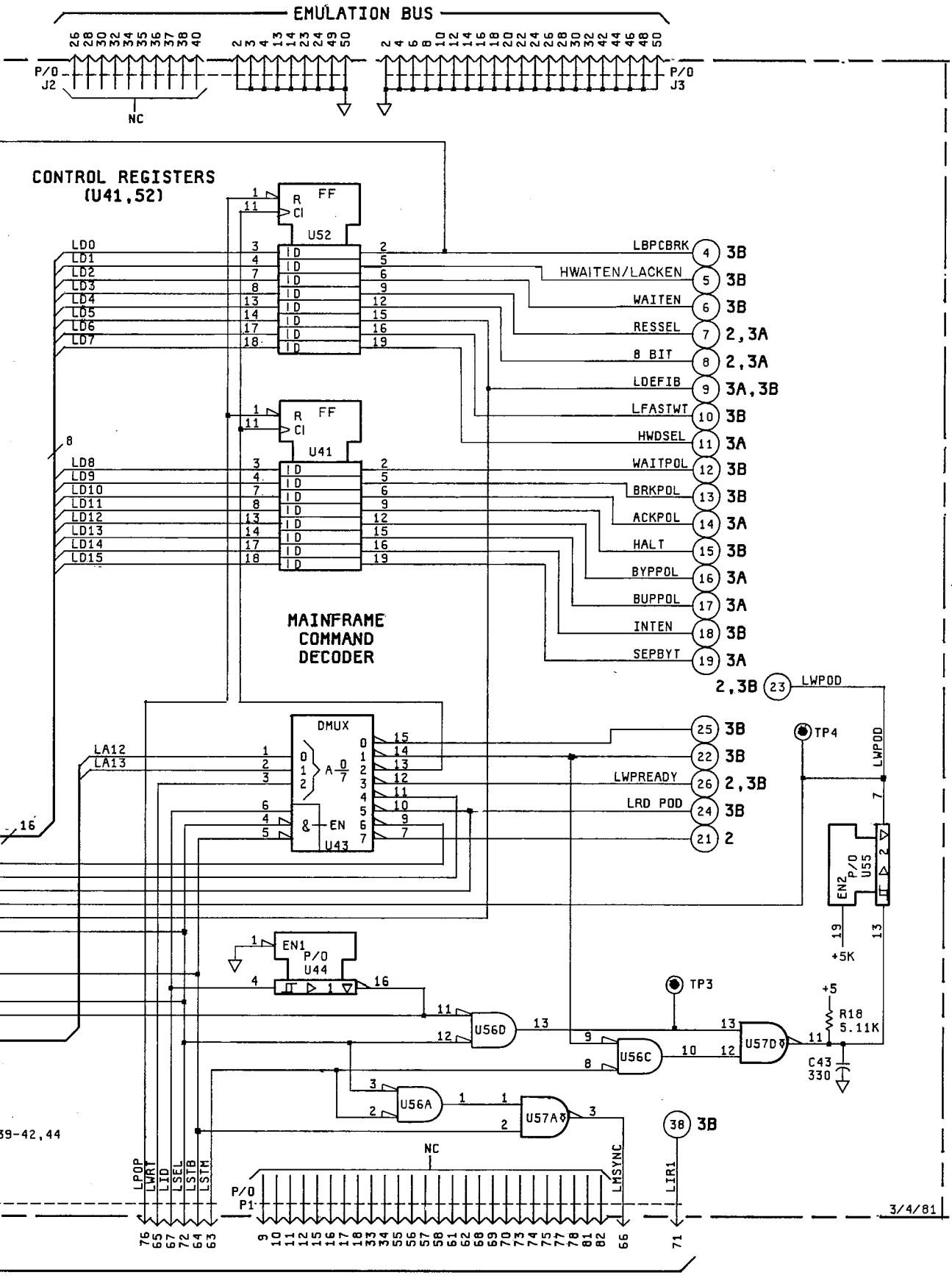


Figure 8-3.
Service Sheet 1, Mainframe CPU Interface (Sheet 1 of 2)


P/O J4
+12
LA0
LA1
LA2
LA3
LA4
LA5
LA6
LA7
8
LA8
LA9
LA10
LA11
P/O P1


P/O GENERAL PURPOSE CONTROLLER (64271-66501)
POD BUS
P/O J1
NC
DATA BUFFERS
LAST ADDRESS LATCHES (U39,40,51)
DRESS BUFFERS (U25,33)
BI DIR BUF
U54
U42
U58C
U51
U39
U40
D-FF
SETLAS
HEA8-23
LED0-15
LEA0-23
LSEL
LA13
LA12
LDEFIB
LRDPOD
LW POD
TP GND
+12
C10 .1UF
-5.2
C9 .1UF


POD BUS
P/O J4
P/O J5
P/O J2
NC
LAST ADDRESS LATCHES (U39,40,51)
U51
U39
U40
D-FF
LEA0
LEA1
LEA2
LEA3
LEA4
LEA5
LEA6
LEA7
LEA8
LEA9
LEA10
LEA11
LEA12
LEA13
LEA14
LEA15
LEA16
LEA17
LEA18
LEA19
LEA20
LEA21
LEA22
LEA23
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9
LD10
LD11
LD12
LD13
LD14
LD15
ID BUFFER
U50
ID0
ID1
ID2
ID3
ID4
+5J
STATUS BUFFER
U53
LMBRKS
LICE
LBPCBRK
HWAITIN
HHALTIN
HRESETIN
HBUSGTIN
LOW SLOW CLOCK
CONTROL REGISTERS (U41,52)
LRDPOD
LW POD
LDEFIB
U45A
U56B
LA12
LA13
GND
+12
-5.2
+5
+5K
C10 .1UF
C9 .1UF
C7 100UF
C35 100UF
C45 100UF
R16 511
R17 511
C1-6,8,12-14,16-21,24-34,36,37,39-42,44 .01UF (BYPASS CAPS)
LPOP
LWRT
LID
LSEL
LSTB
LSTM
P/O P1
BPC (MAINFRAME) BUS



ICS ON THIS

REF. DES.	HP PART NO
U25,33,50	1820-1917
U29	1820-2690
U39,40,51	1820-1997
U41,52	1820-1730
U42,54	1820-2075
U43	1820-1240
U44	1820-1633
U45	1820-2684
U46	1820-2687
U53	1820-2024
U55	1820-2699
U56	1820-2685
U57	1820-1198
U58	1820-2686

PARTS ON THIS

C1-10,12-14,16-21,2
R16-18
U25,29,33,39-46,50-

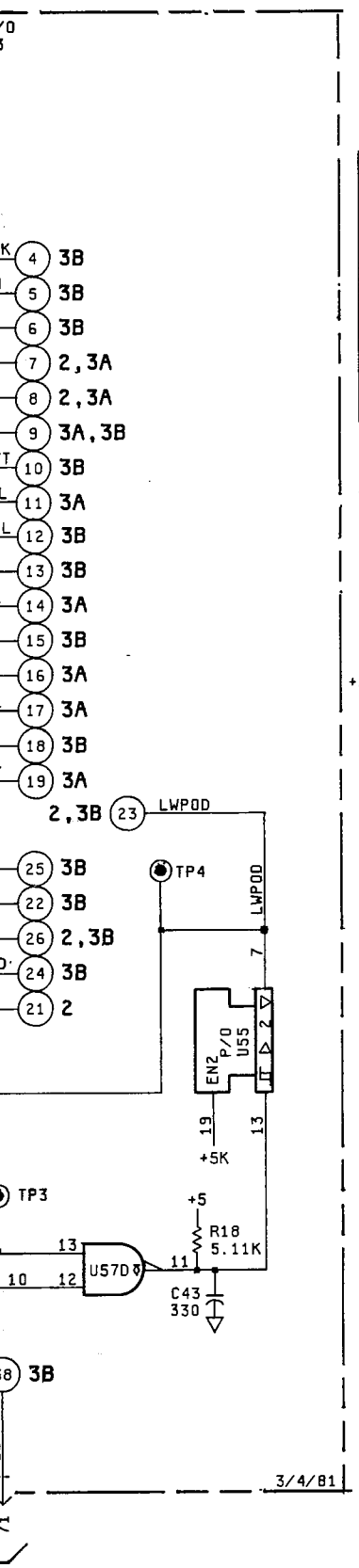
IC POWER
CONFIGURA

+5 20/10 U25,33, 39-42, 44,50-55

+5 16/8 U43

1

Service Sheet 1, Mainframe CPU Interfac



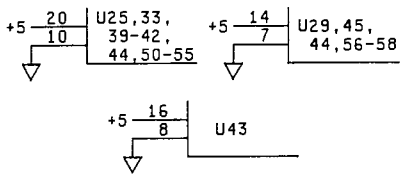
ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U25,33,50	1820-1917	SN74LS240N
U29	1820-2690	UA74F32
U39,40,51	1820-1997	SN74LS374
U41,52	1820-1730	SN74LS273
U42,54	1820-2075	SN74LS245
U43	1820-1240	74S138
U44	1820-1633	UA74S240
U45	1820-2684	UA74F00
U46	1820-2687	UA74F10
U53	1820-2024	SN74LS244
U55	1820-2699	UA74F241
U56	1820-2685	UA74F02
U57	1820-1198	1820-1198
U58	1820-2686	UA74F08

PARTS ON THIS SCHEMATIC

C1-10,12-14,16-21,24-37,39-45
R16-18
U25,29,33,39-46,50-58

IC POWER SUPPLY CONFIGURATIONS



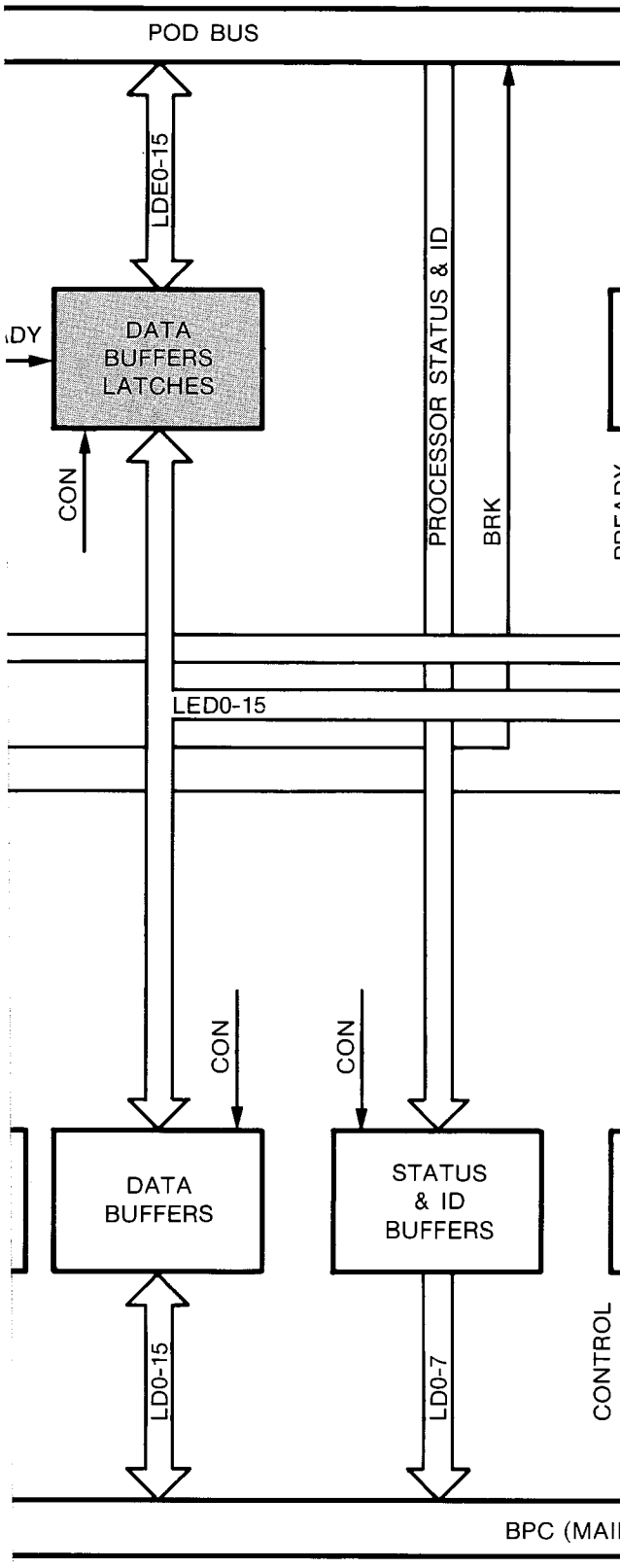


Figure 8-3.
Service Sheet 1, Mainframe CPU Interface (Sheet 2 of 2)

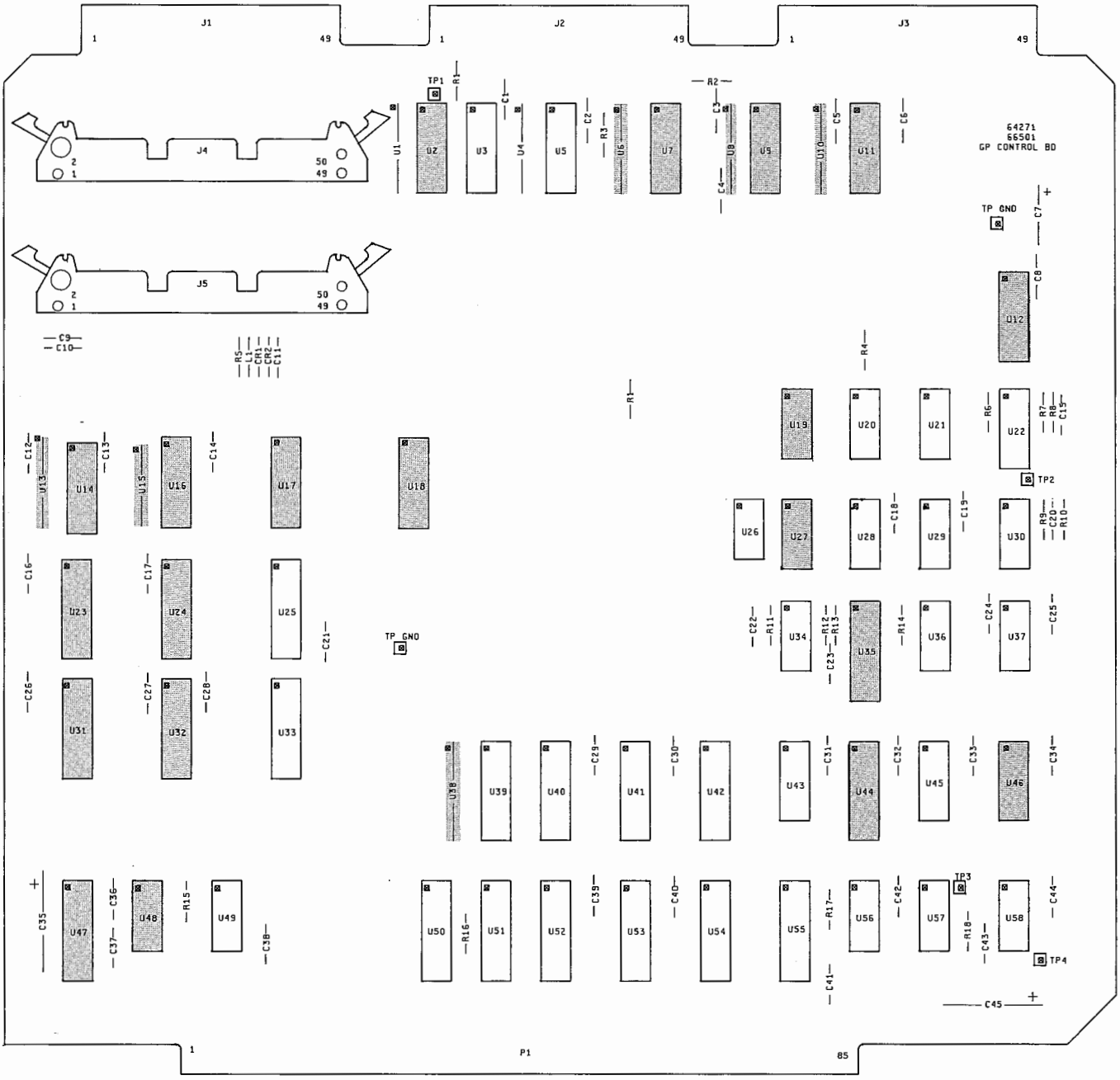
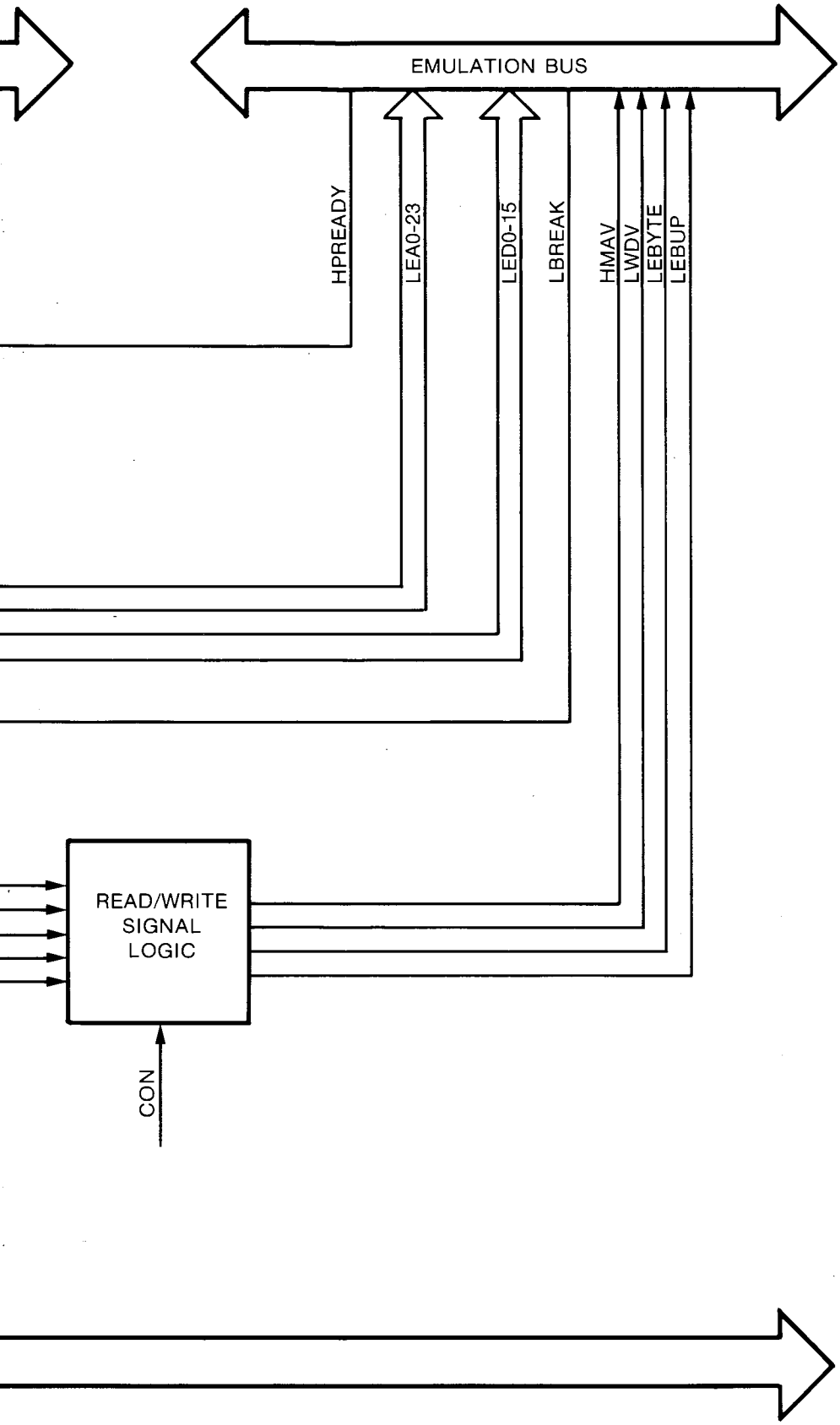


Figure 8-4.
Service Sheet 2, Emulation Pod Interface (Sheet 1 of 2)



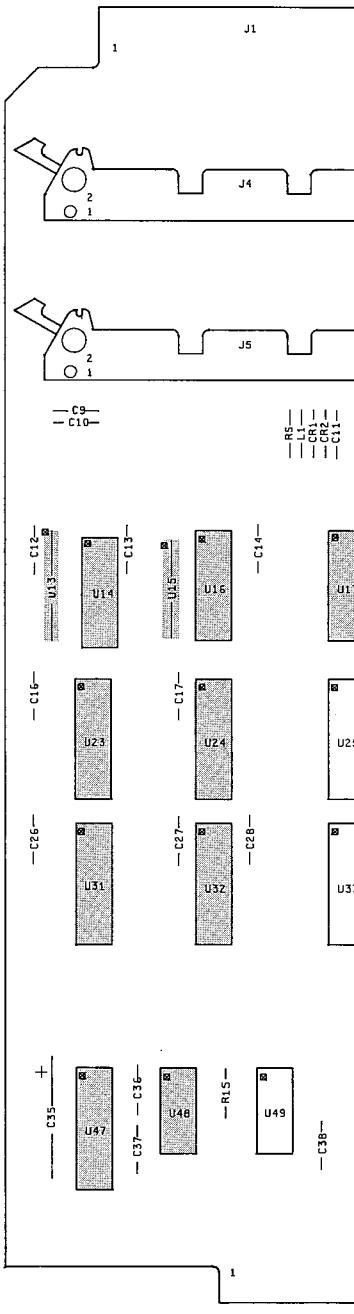
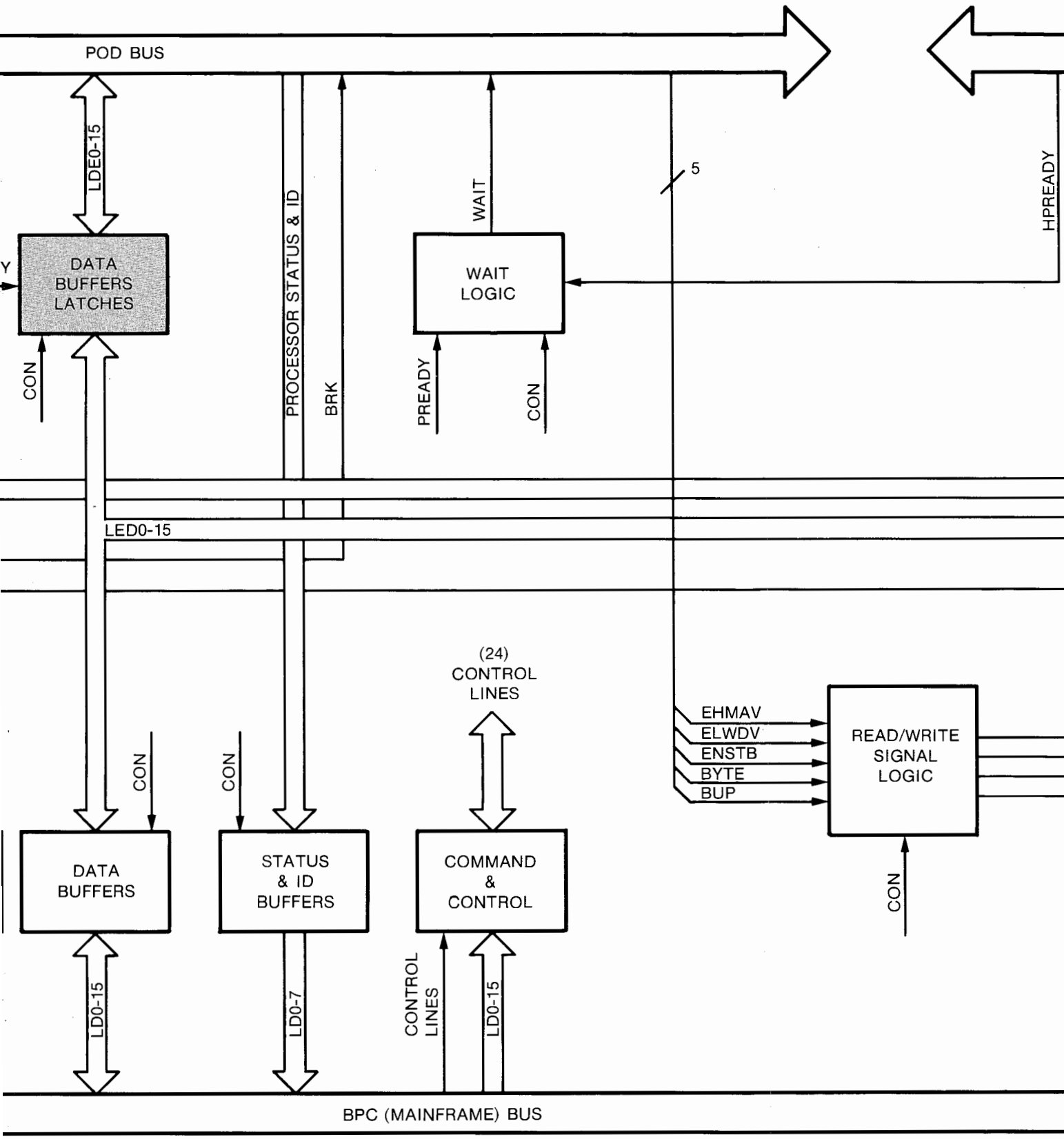
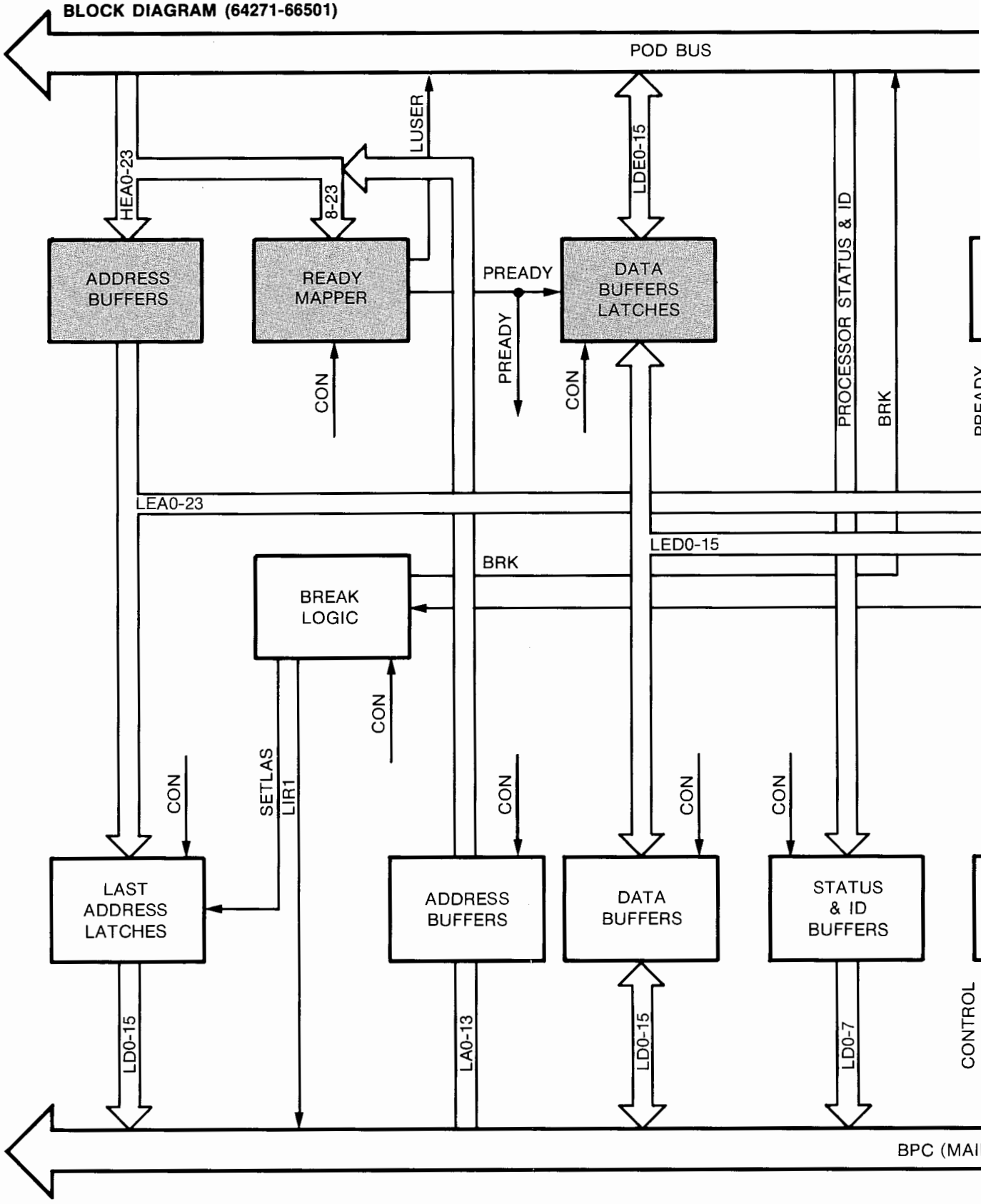
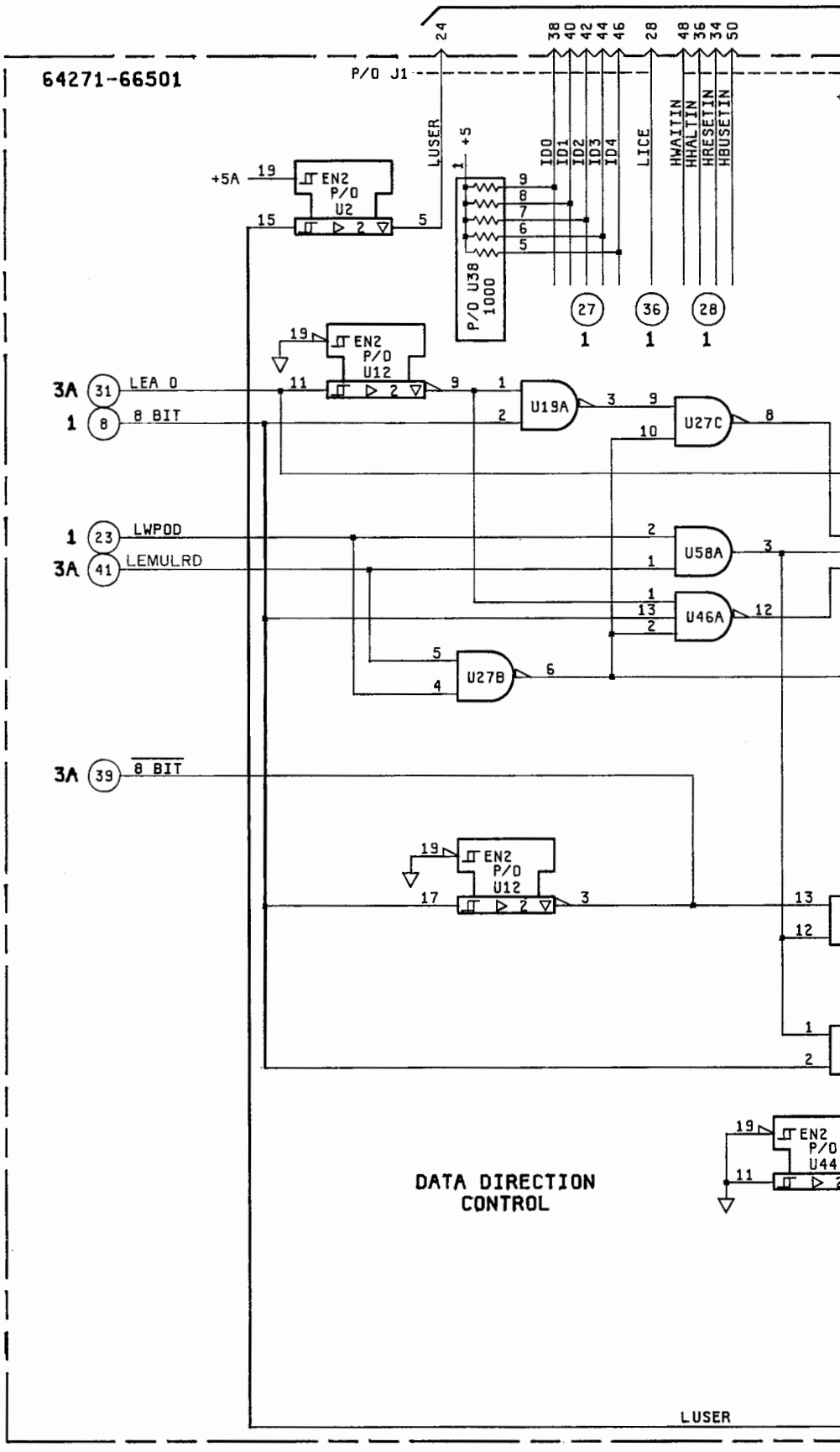


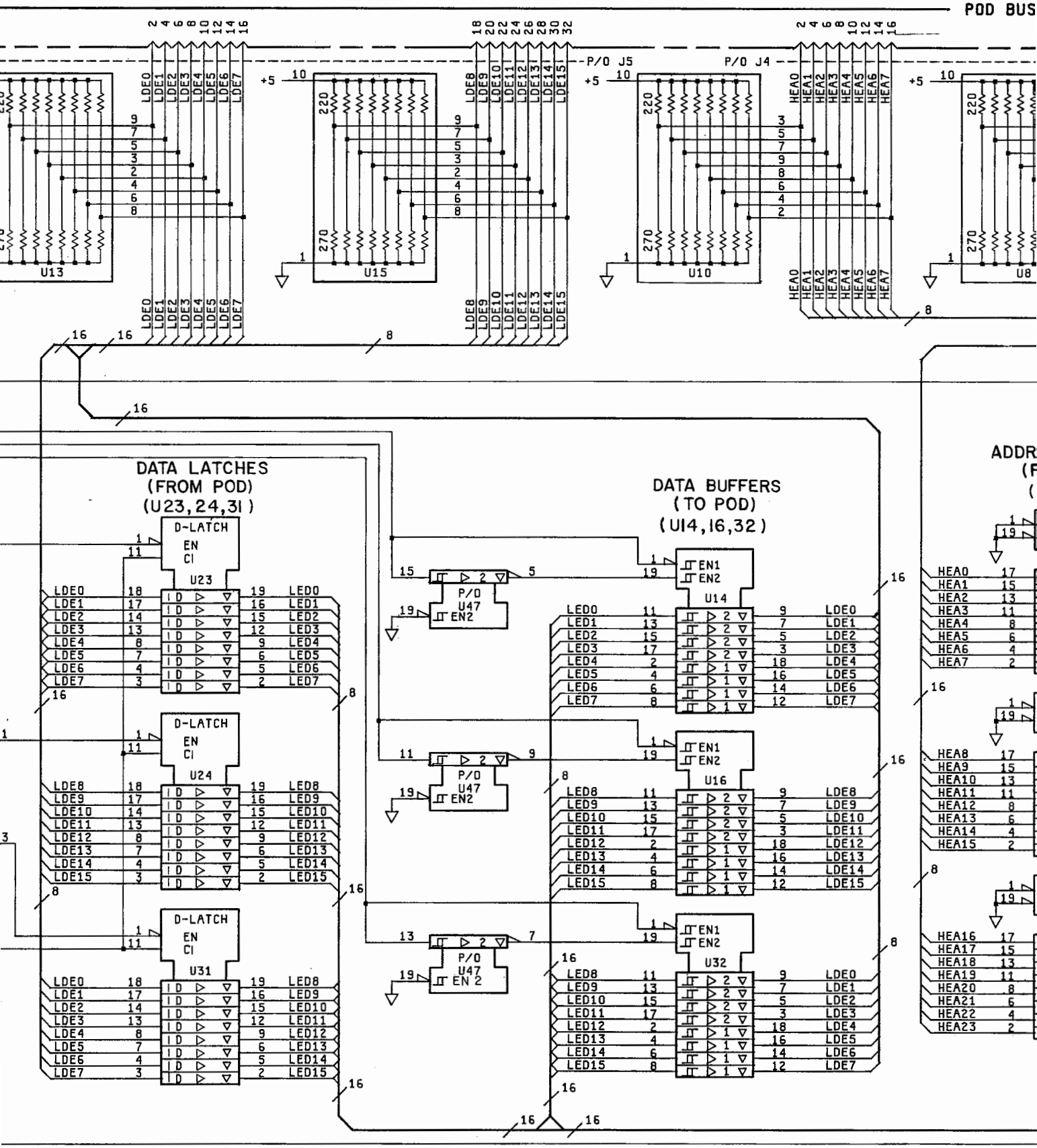
Figure 8-4.
Service Sheet 2, Emulation

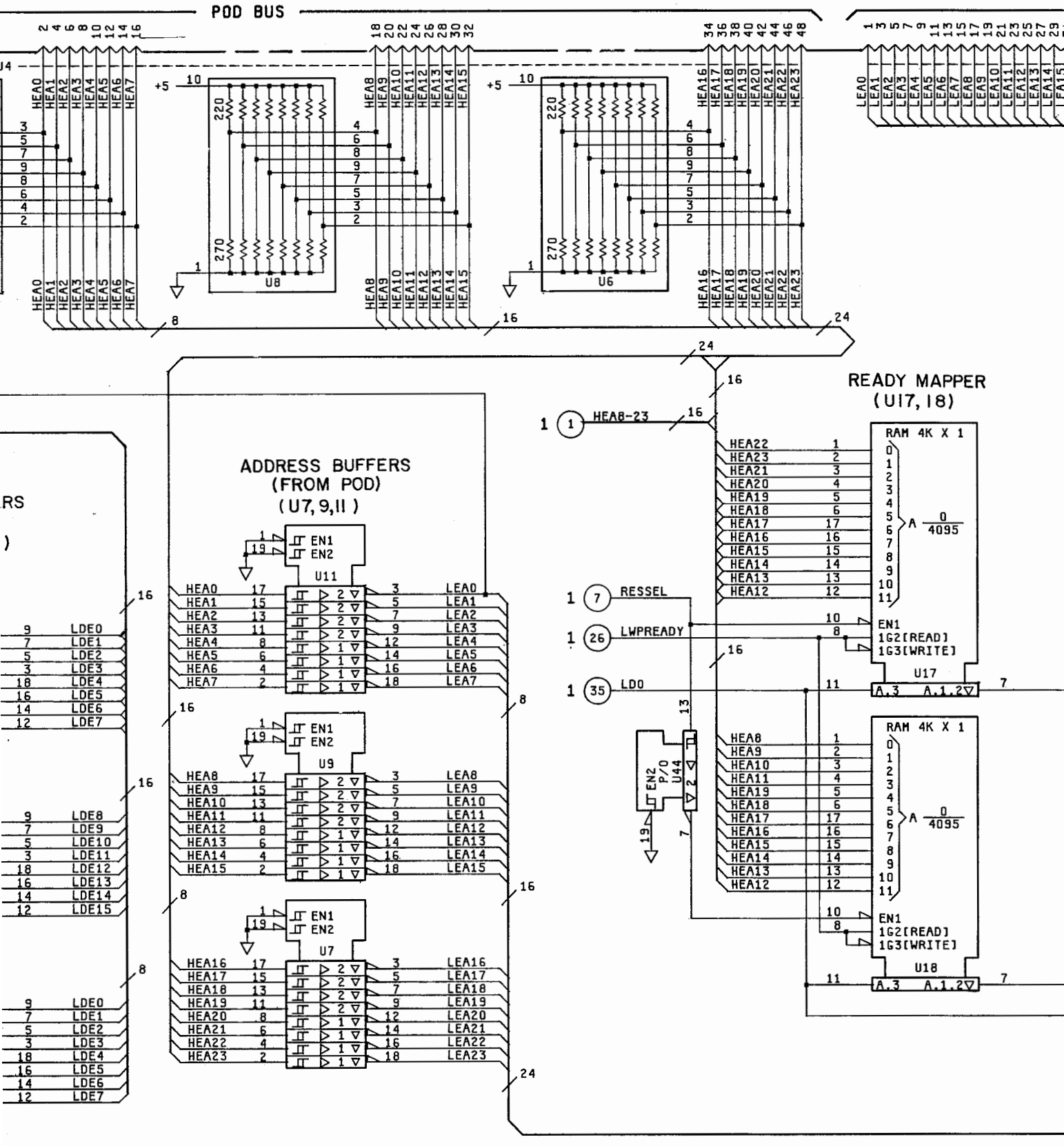

POD BUS
LDE0-15
DATA BUFFERS LATCHES
CON
PROCESSOR STATUS & ID
BRK
WAIT
WAIT LOGIC
PREADY
CON
5
HPREADY
LED0-15
(24) CONTROL LINES
EHMAV
ELWDV
ENSTB
BYTE
BUP
READ/WRITE SIGNAL LOGIC
CON
CON
CON
DATA BUFFERS
STATUS & ID BUFFERS
COMMAND & CONTROL
LD0-15
LD0-7
CONTROL LINES
LD0-15
BPC (MAINFRAME) BUS

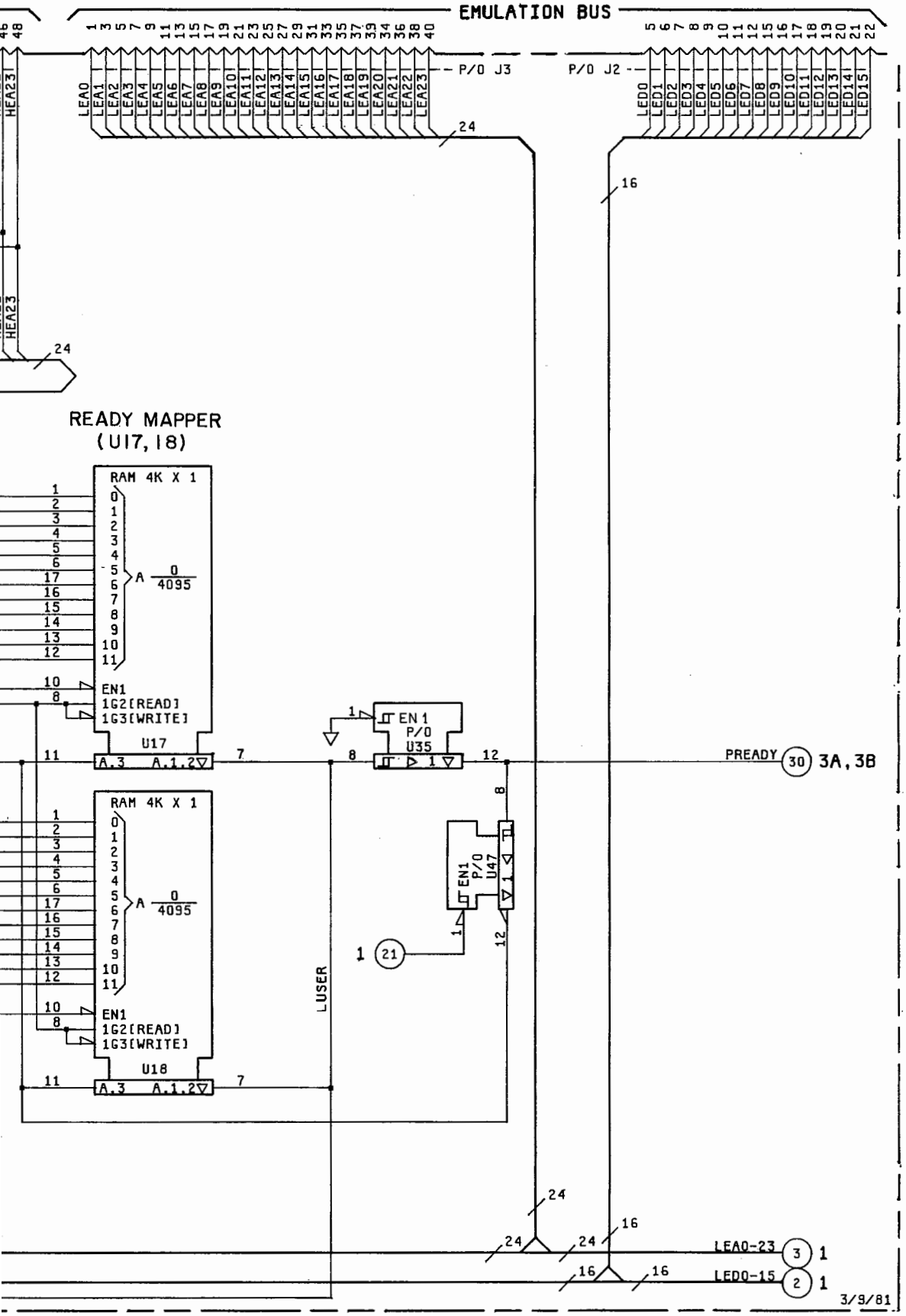
BLOCK DIAGRAM (64271-66501)




64271-66501
P/O J1
24
38
40
42
44
46
28
48
36
34
50
LUSER
+5
ID0
ID1
ID2
ID3
ID4
LICE
HWAITIN
HHALTIN
HRESETIN
HBUSETIN
+5A
EN2
P/O
U2
P/O U38
1000
27
36
28
U12
LEA 0
8 BIT
U19A
U27C
LWPOD
LEMULRD
U58A
U46A
U27B
8 BIT
U44
DATA DIRECTION
CONTROL
LUSER


POD BUS
P/O J5
P/O J4
U13
U15
U10
U8
DATA LATCHES
(FROM POD)
(U23,24,31)
DATA BUFFERS
(TO POD)
(U14,16,32)
D-LATCH
EN
CI
U23
U24
U31
U14
U16
U32
P/O
U47
EN2
EN1
ADDR


POD BUS
ADDRESS BUFFERS
(FROM POD)
(U7,9,11)
READY MAPPER
(U17,18)
RAM 4K X 1
RESSEL
LWPREADY
LDO
HEA8-23
U11
U9
U7
U8
U6
U17
U18
EN1
EN2
1G2[READ]
1G3[WRITE]



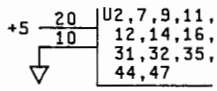
ICS ON THIS SCHEMA

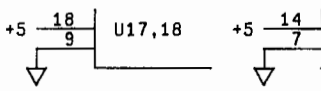
REF. DES.	HP PART NO.	MFG. P
U2,14,16, 32,35	1820-2699	UA7
U7,9,11, 12,44,47	1820-1633	UA74
U17,18	1818-1586	2147
U19,27	1820-2684	UA74
U23,24,31	1820-2700	UA74
U46	1820-2682	UA74
U58	1820-2686	UA74

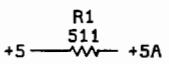
PARTS ON THIS SCHEMA

R1
U2,6-19,23,24,27,31,32,35,38,

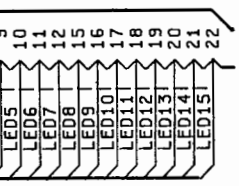
IC POWER SUPPLY CONFIGURATIONS







2



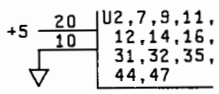
ICS ON THIS SCHEMATIC

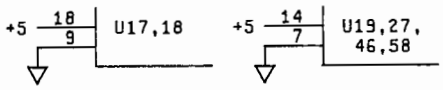
REF. DES.	HP PART NO.	MFG. PART NO.
U2,14,16, 32,35	1820-2699	UA74F241
U7,9,11, 12,44,47	1820-1633	UA74S240
U17,18	1818-1586	2147H-1
U19,27	1820-2684	UA74F00
U23,24,31	1820-2700	UA74F373
U46	1820-2682	UA74F10
U58	1820-2686	UA74F08

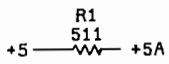
PARTS ON THIS SCHEMATIC

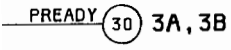
R1
U2,6-19,23,24,27,31,32,35,38,44,46,47,58

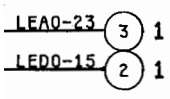
IC POWER SUPPLY CONFIGURATIONS











3/9/81

2

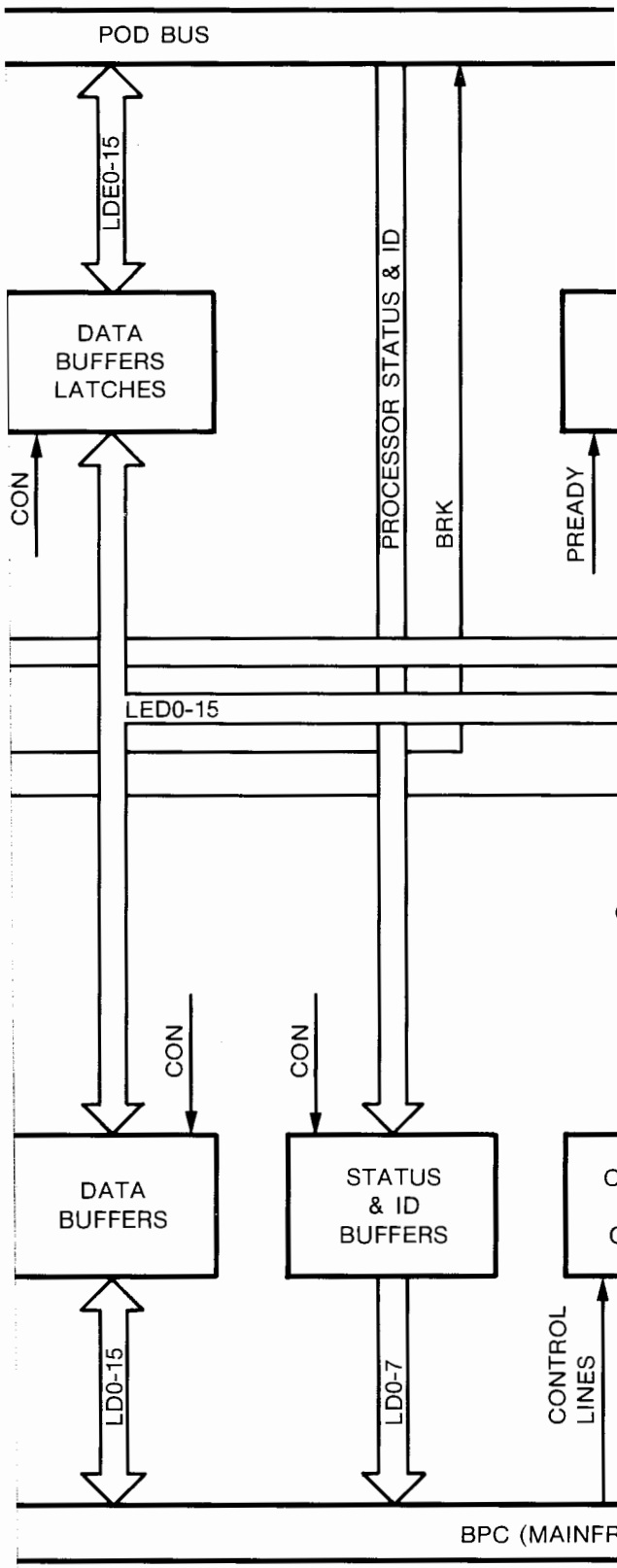


Figure 8-4.
Service Sheet 2, Emulation Pod Interface (Sheet 2 of 2)

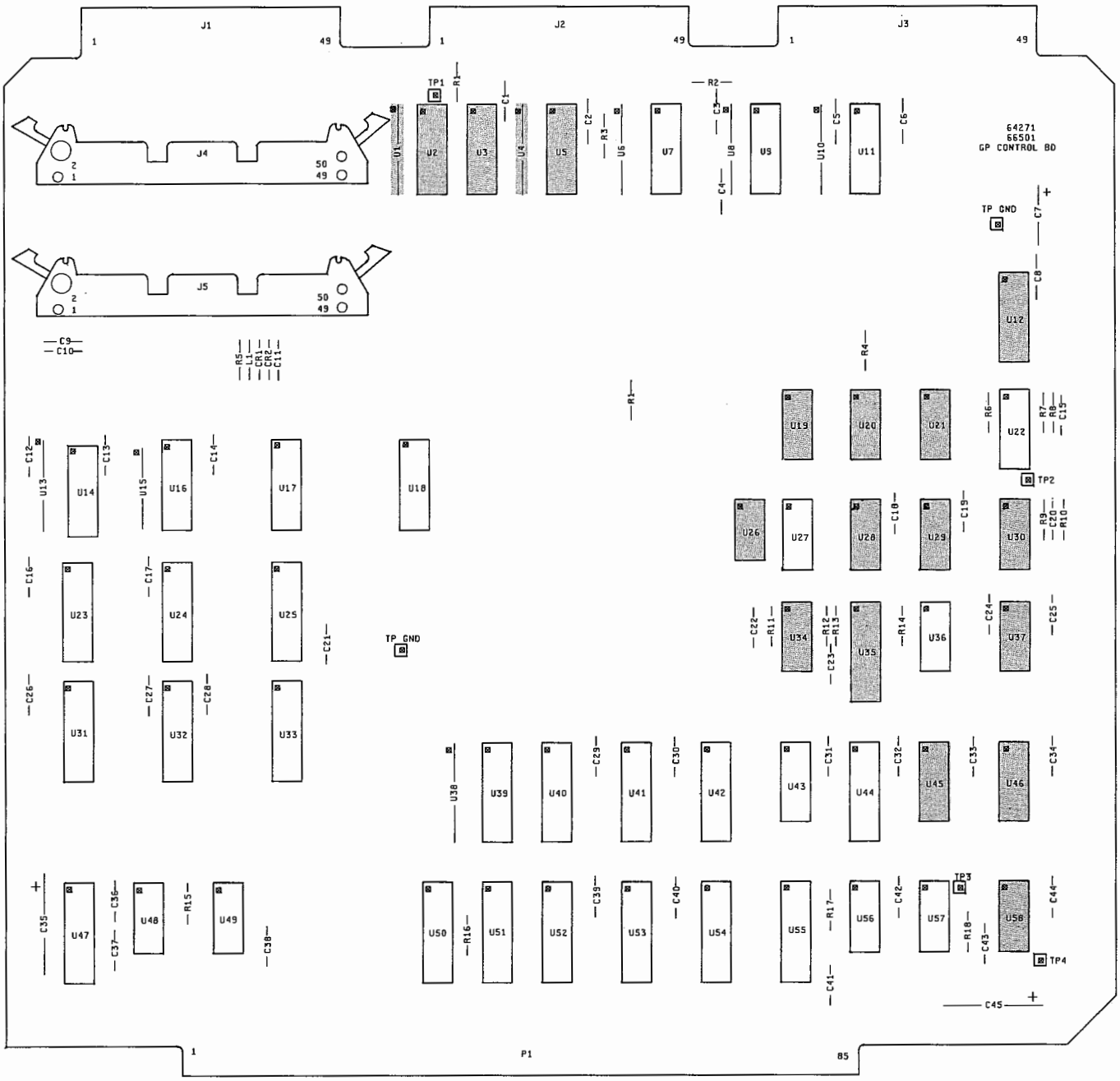
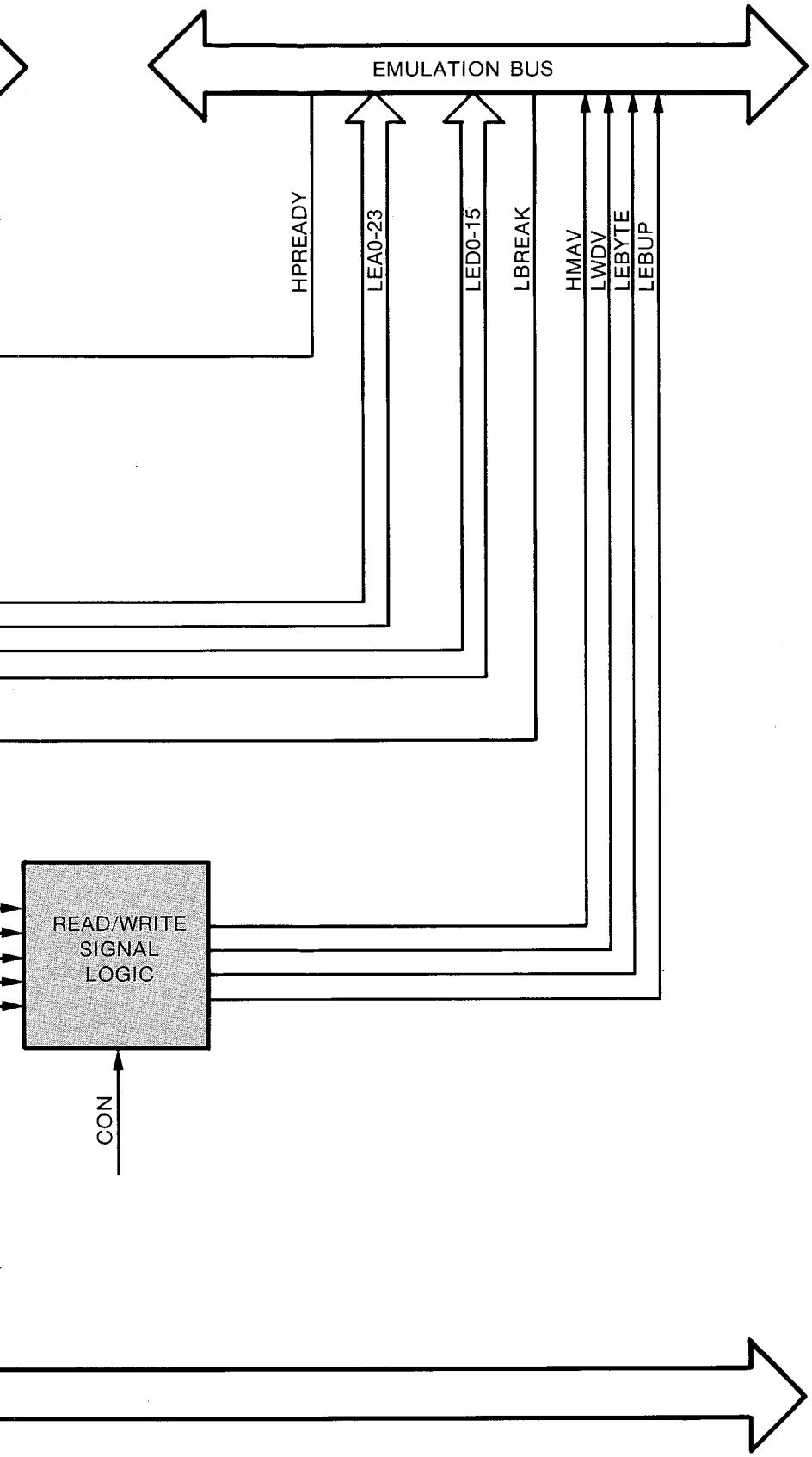


Figure 8-5.
Service Sheet 3A, Control Logic (Sheet 1 of 2)



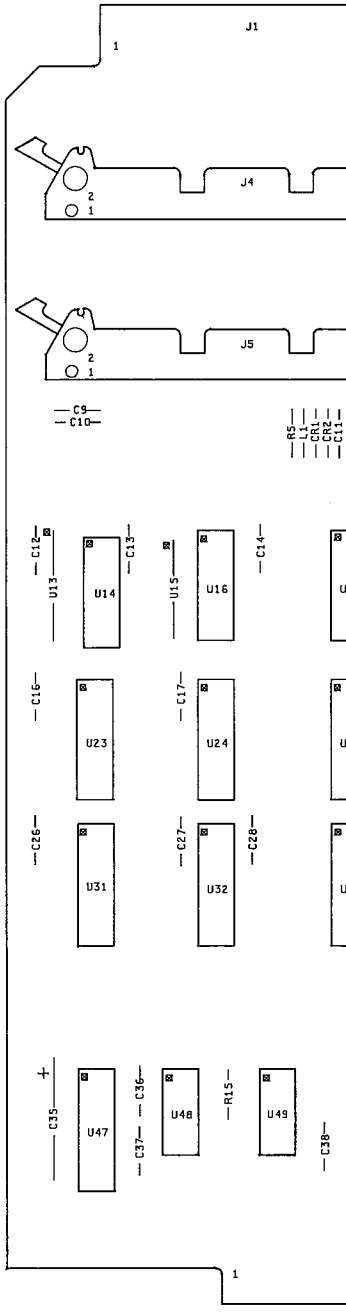
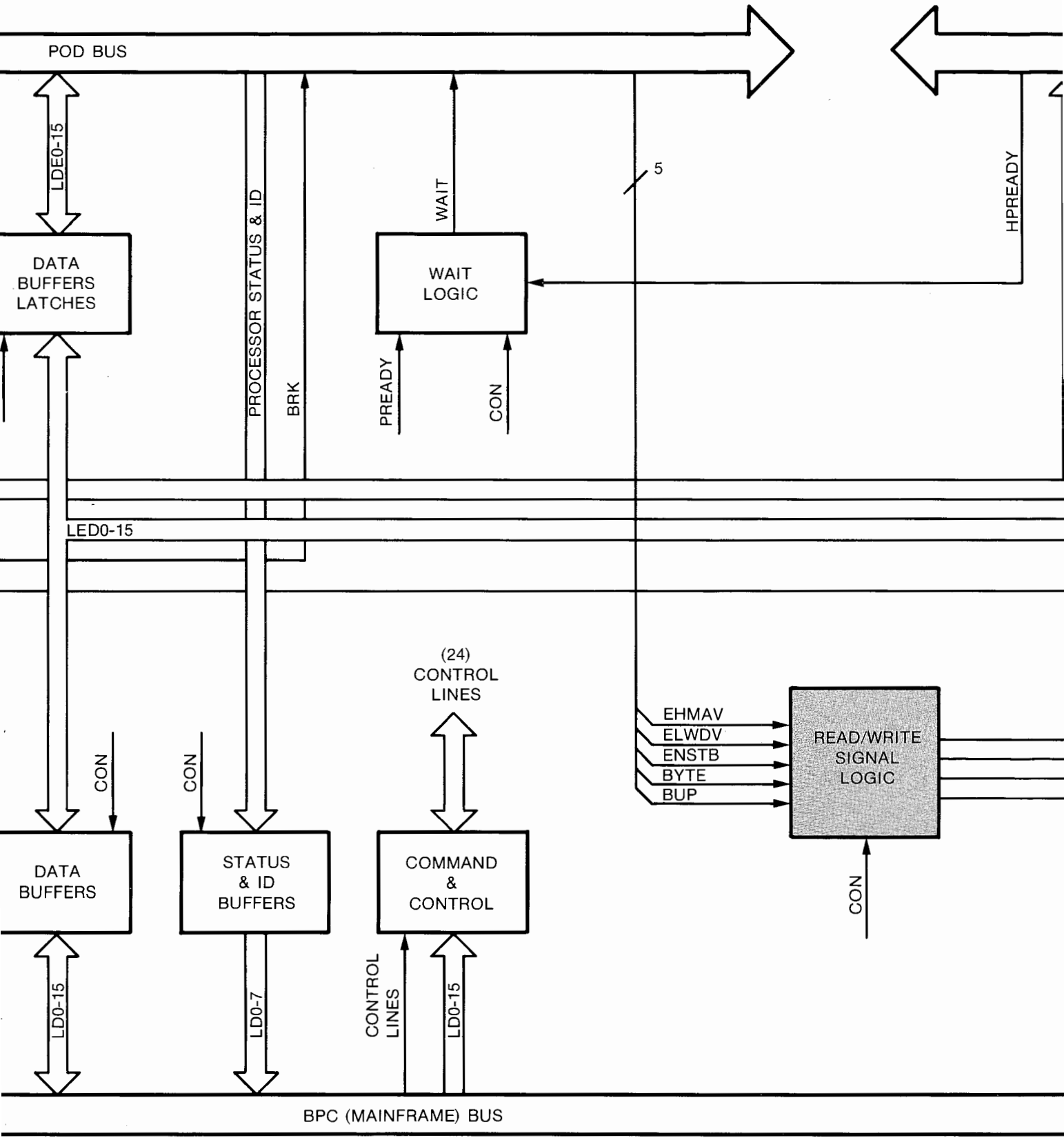
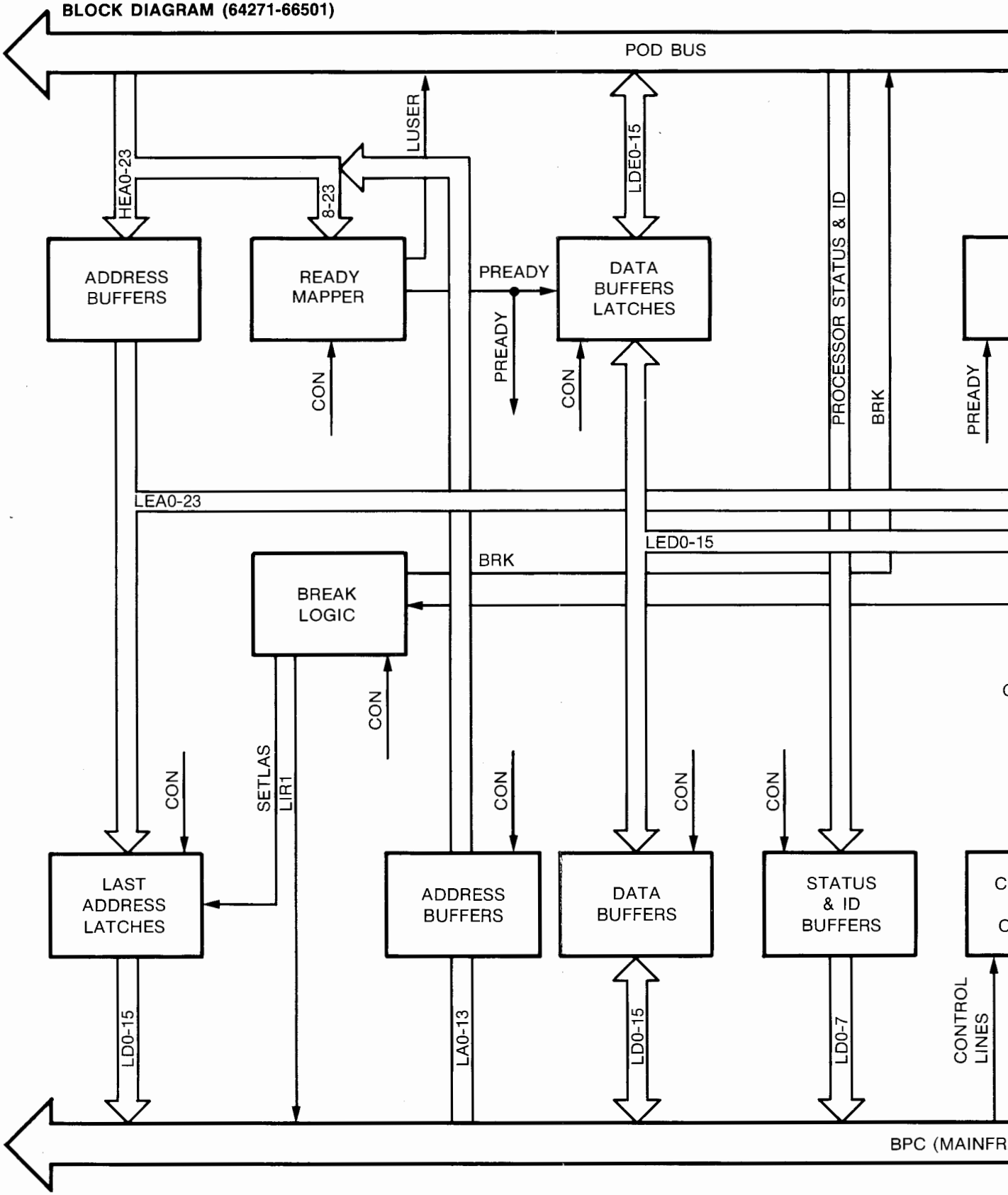
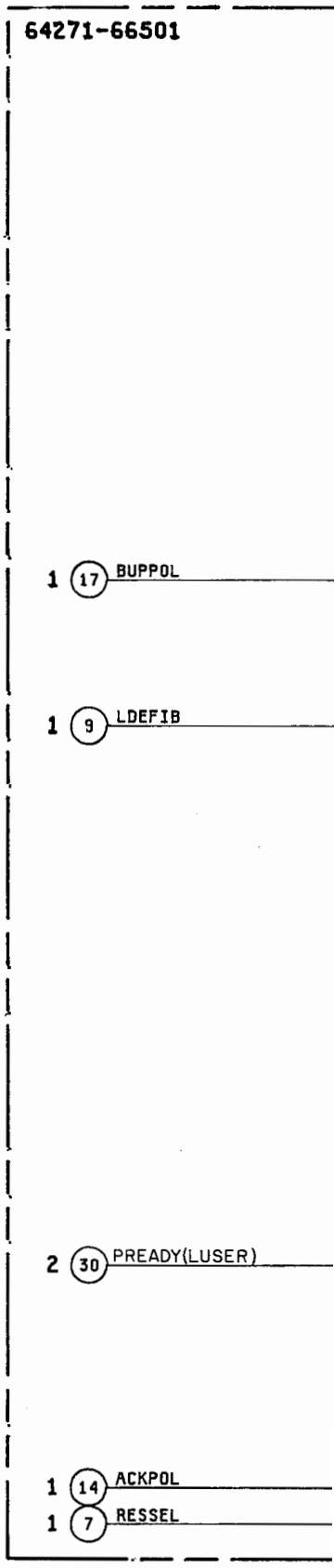


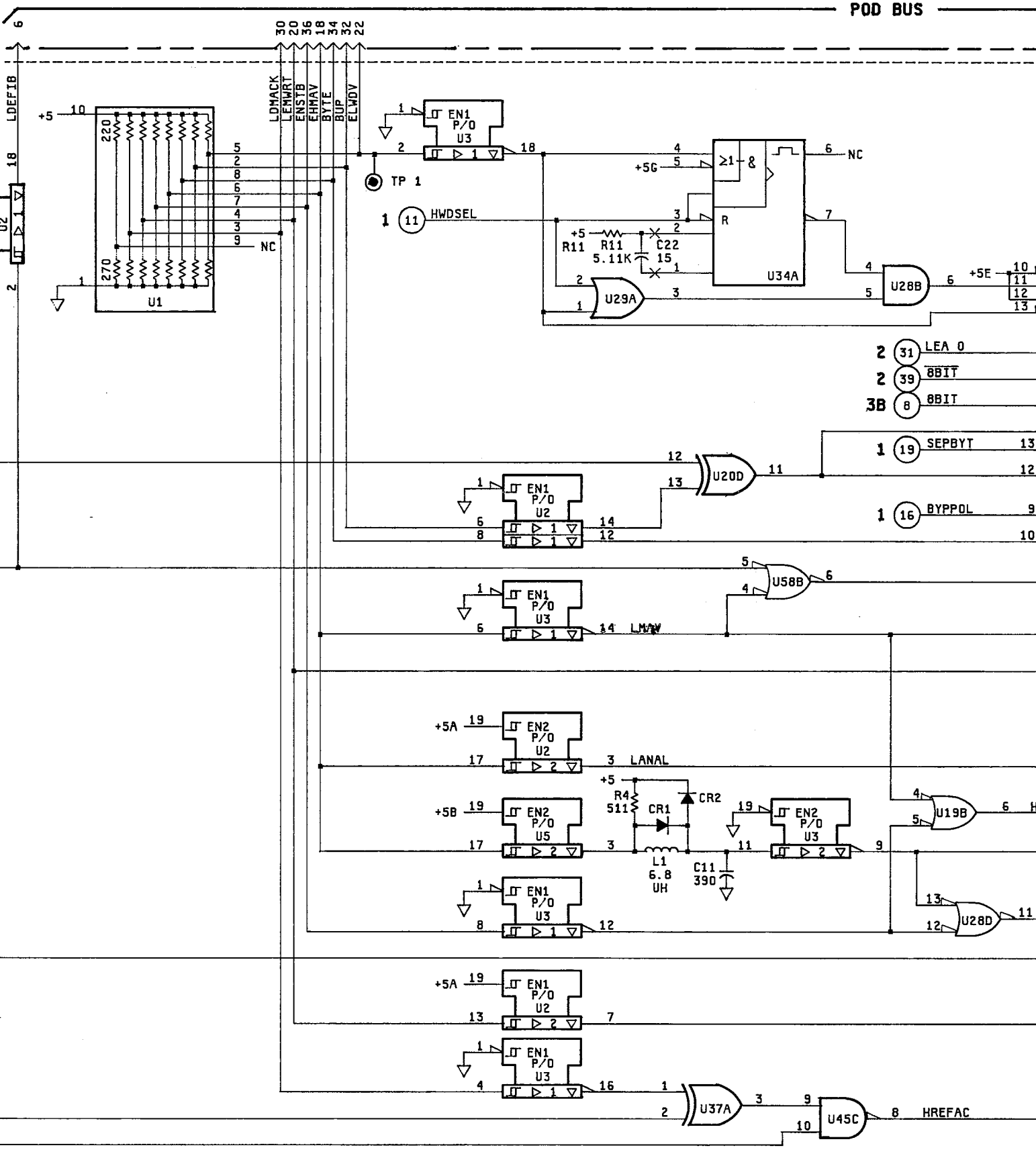
Figure 8-5.
Service Sheet 3A, Control L

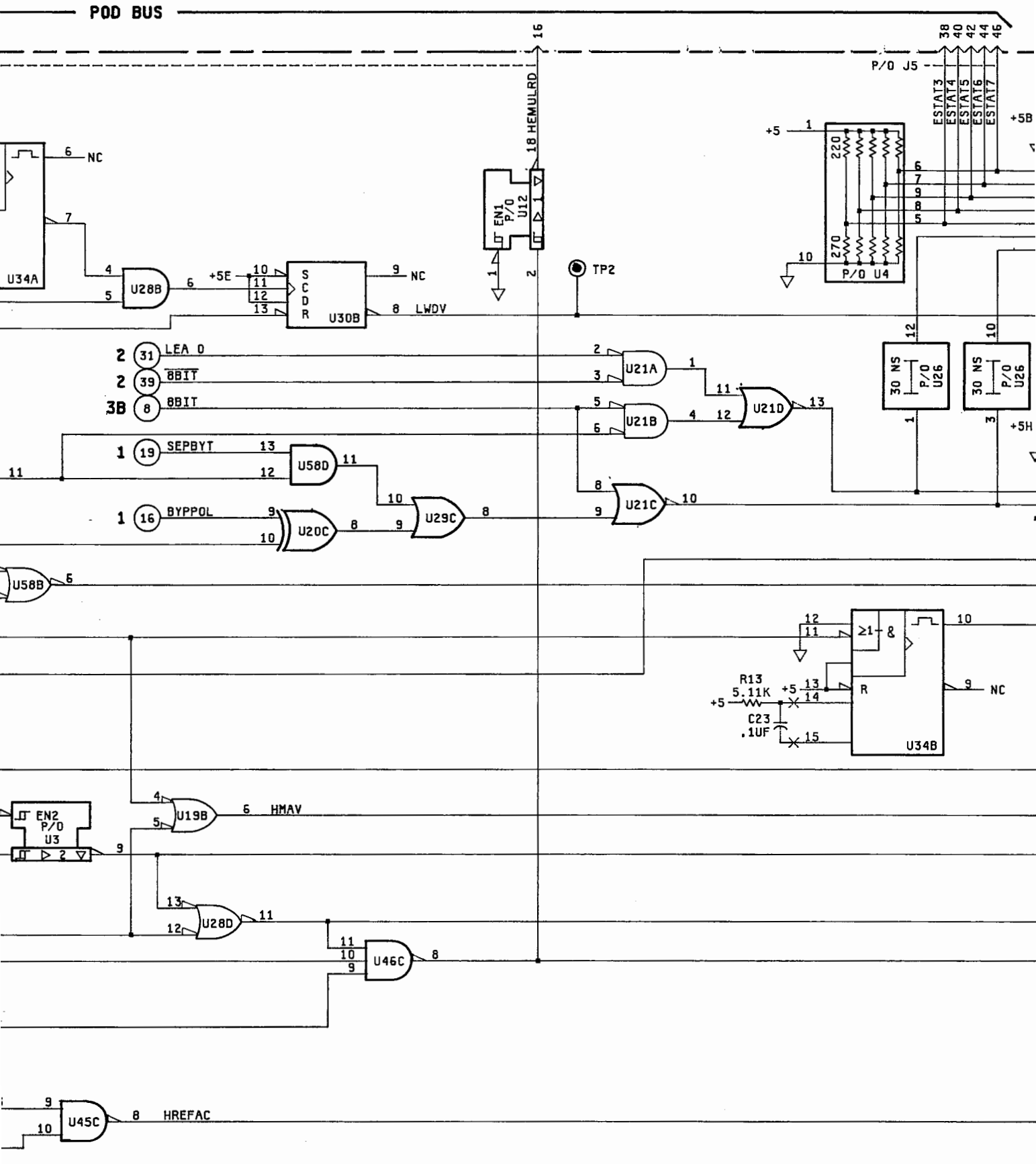

POD BUS
LDE0-15
DATA BUFFERS LATCHES
PROCESSOR STATUS & ID
BRK
WAIT
WAIT LOGIC
PREADY
CON
5
HPREADY
LED0-15
(24) CONTROL LINES
EHMAV
ELWDV
ENSTB
BYTE
BUP
READ/WRITE SIGNAL LOGIC
CON
CON
CON
DATA BUFFERS
STATUS & ID BUFFERS
COMMAND & CONTROL
LD0-15
LD0-7
CONTROL LINES
LD0-15
BPC (MAINFRAME) BUS

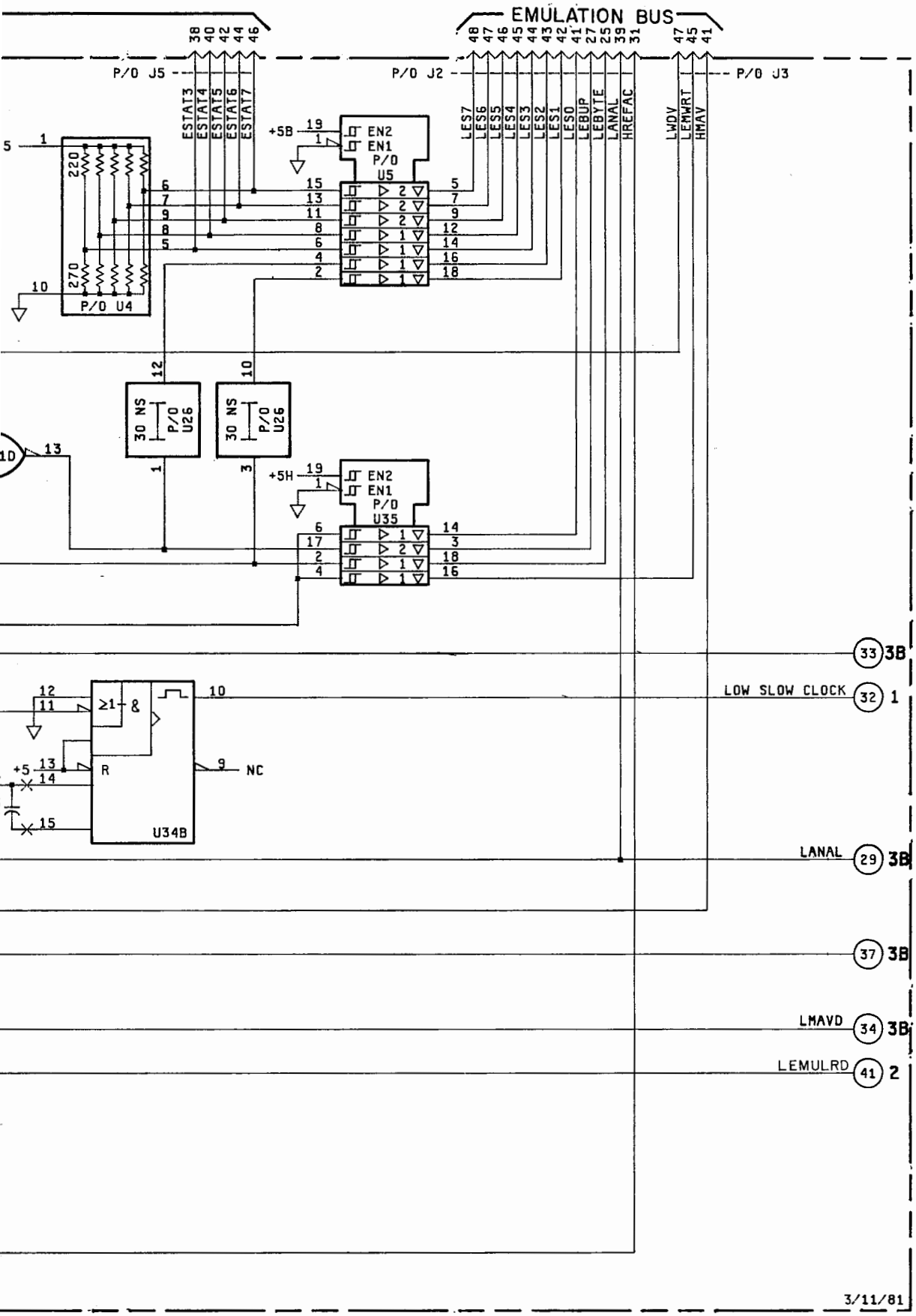
BLOCK DIAGRAM (64271-66501)




64271-66501
1 17 BUPPOL
1 9 LDEFIB
2 30 PREADY(LUSER)
1 14 ACKPOL
1 7 RESSEL


LDEF18
LDMACK
LEMWRT
ENSTB
EHMAV
BYTE
BUP
ELWDV
+5
220
270
U1
NC
TP 1
HWDSEL
EN1 P/O U3
EN1 P/O U2
EN2 P/O U2
EN2 P/O U5
EN2 P/O U3
+5G
≥1
&
R
U34A
U29A
U28B
+5E
R11
R11 5.11K
C22 15
U20D
U58B
U19B
U28D
U37A
U45C
LEA 0
8BIT
8BIT
SEPBYT
BYPPOL
LMAV
LANAL
+5A
+5B
R4 511
CR1
CR2
L1 6.8 UH
C11 390
HREFAC


POD BUS
16
18 HEMULRD
P/O J5
38
40
42
44
46
ESTAT3
ESTAT4
ESTAT5
ESTAT6
ESTAT7
+5B
+5
220
270
P/O U4
EN1
P/O
U12
TP2
U34A
NC
U28B
+5E
SCDR
U30B
LWDV
LEA 0
8BIT
SEPBYT
BYPPOL
U58D
U20C
U29C
U58B
U21A
U21B
U21C
U21D
30 NS
P/O
U26
+5H
R13
5.11K
C23
.1UF
U34B
EN2
P/O
U3
U19B
HMAV
U28D
U46C
U45C
HREFAC



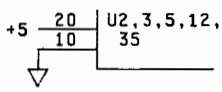
ICS ON THIS SCHE

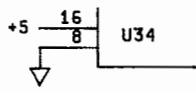
REF. DES.	HP PART NO.	MF
U2,5,35	1820-2699	
U3,12	1820-1633	
U19,45	1820-2684	
U20,37	1820-2692	
U21	1820-2685	
U26	1810-0568	
U28,58	1820-2686	
U29	1820-2690	
U30	1820-2691	
U34	1820-1782	
U46	1820-2682	

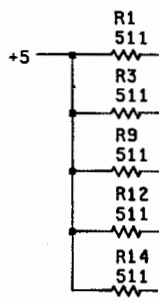
PARTS ON THIS SC

C11,22,23
CR1,2
L1
R1,3,5,9,11-14
U1-5,12,19,20,21,26,28-30,
58

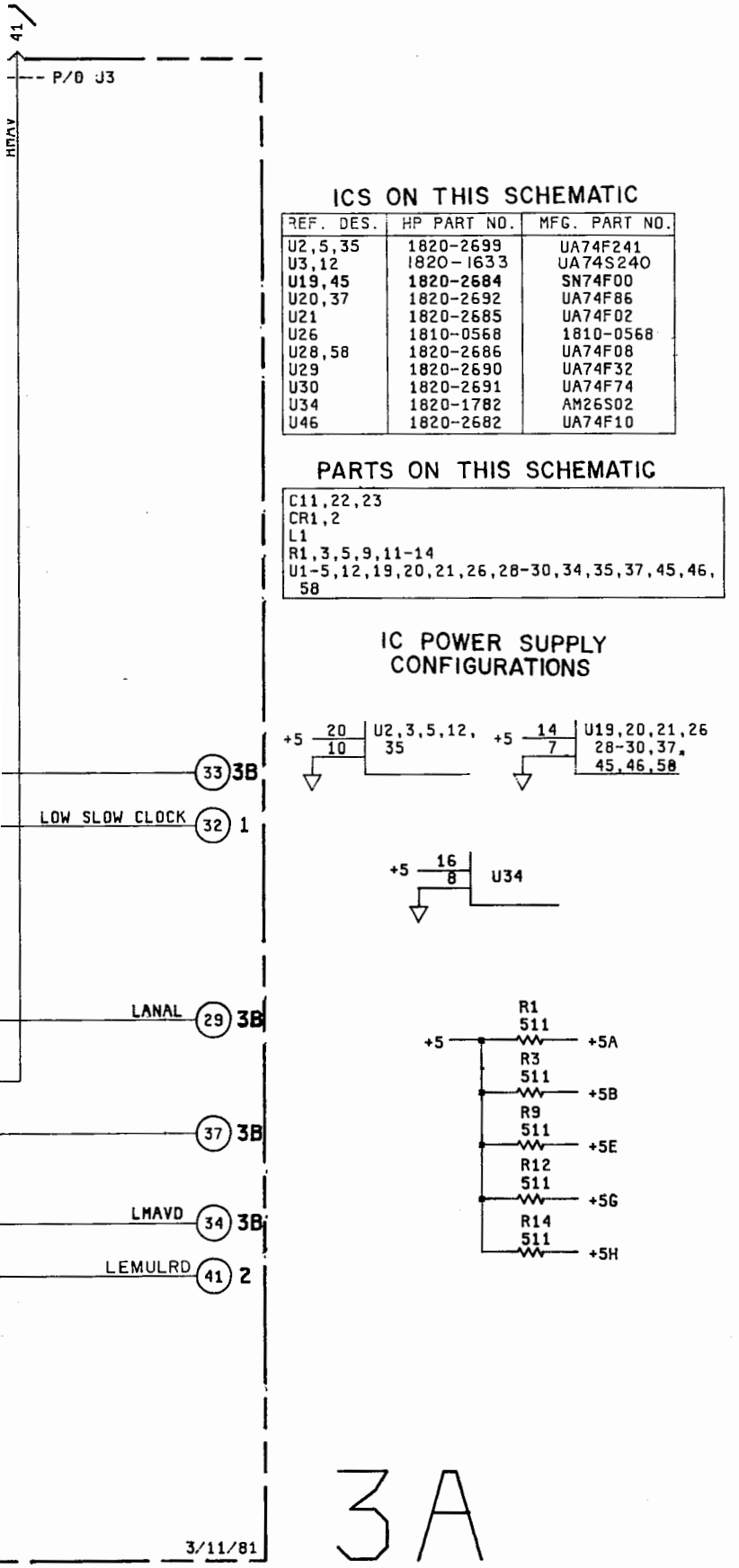
IC POWER SUP CONFIGURATIO







3A



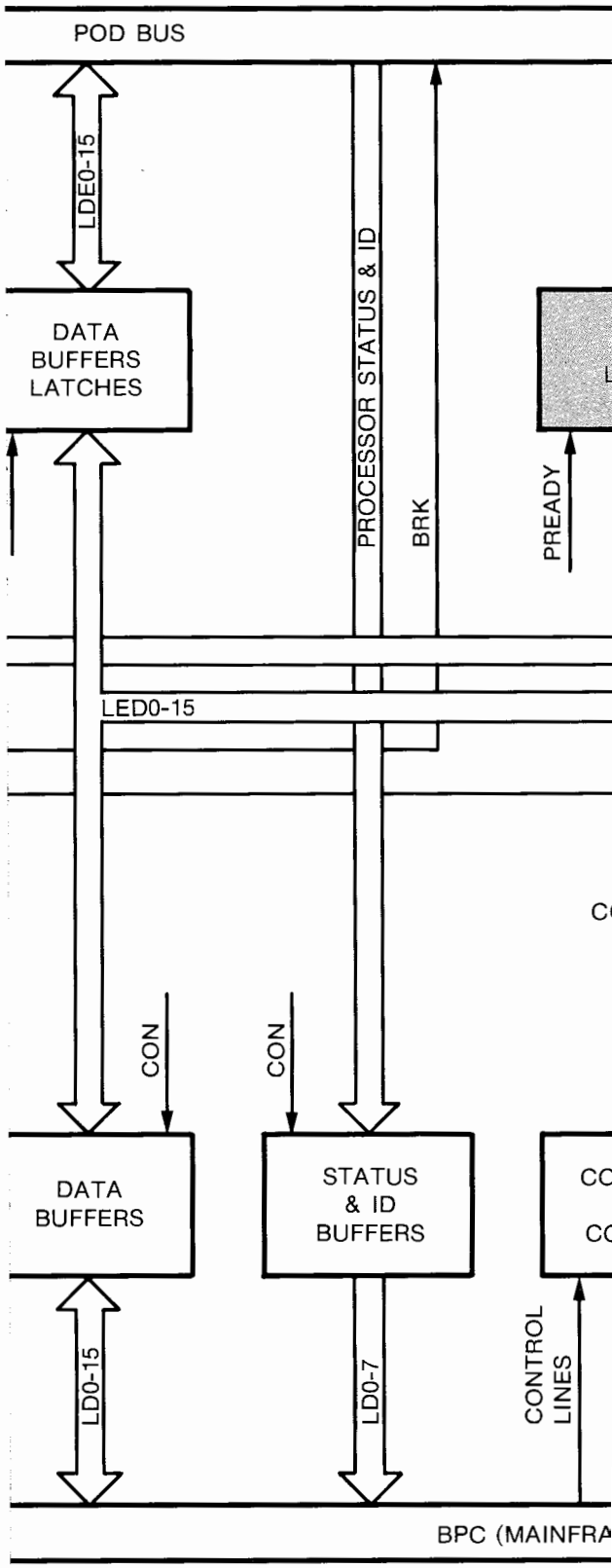
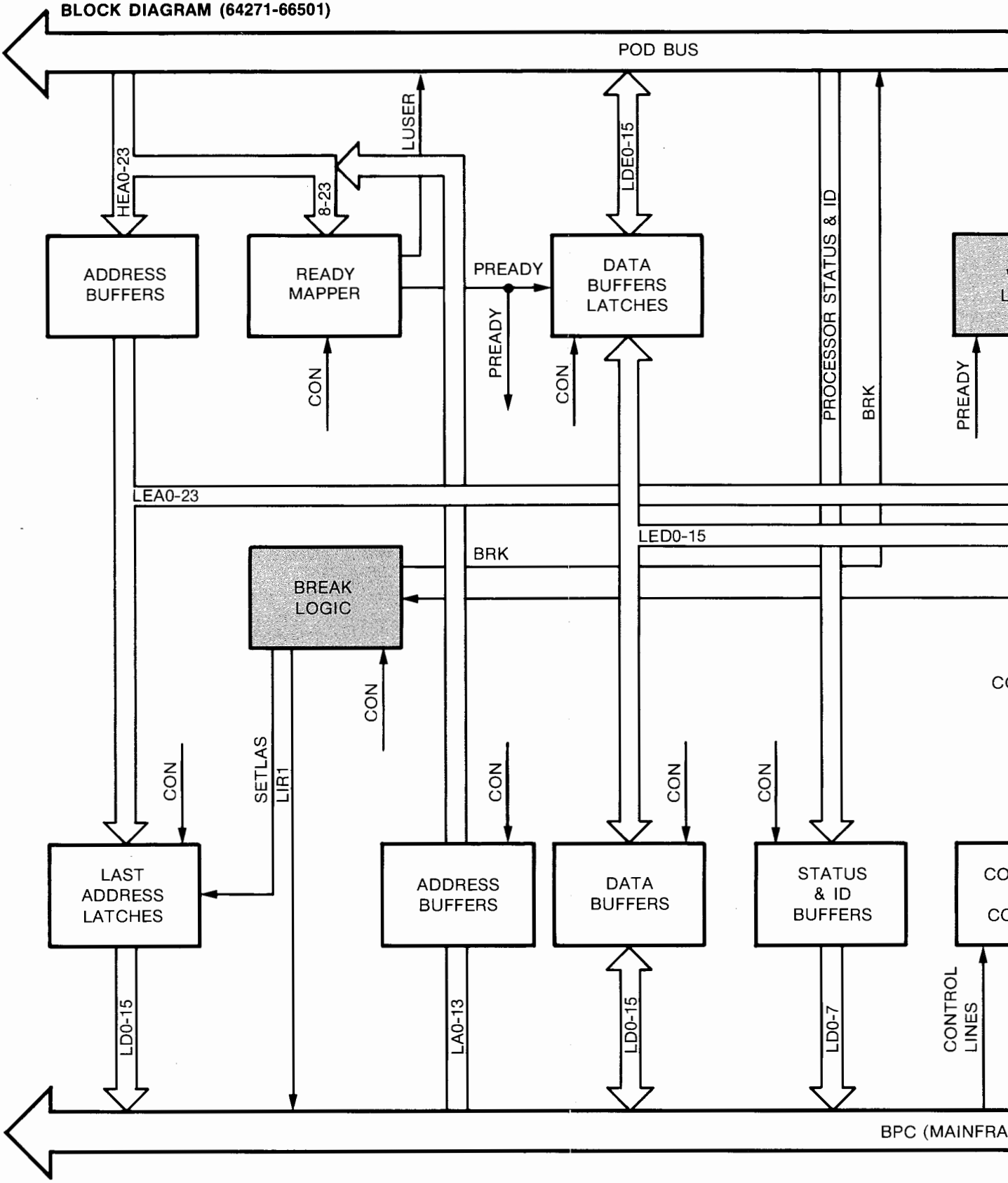
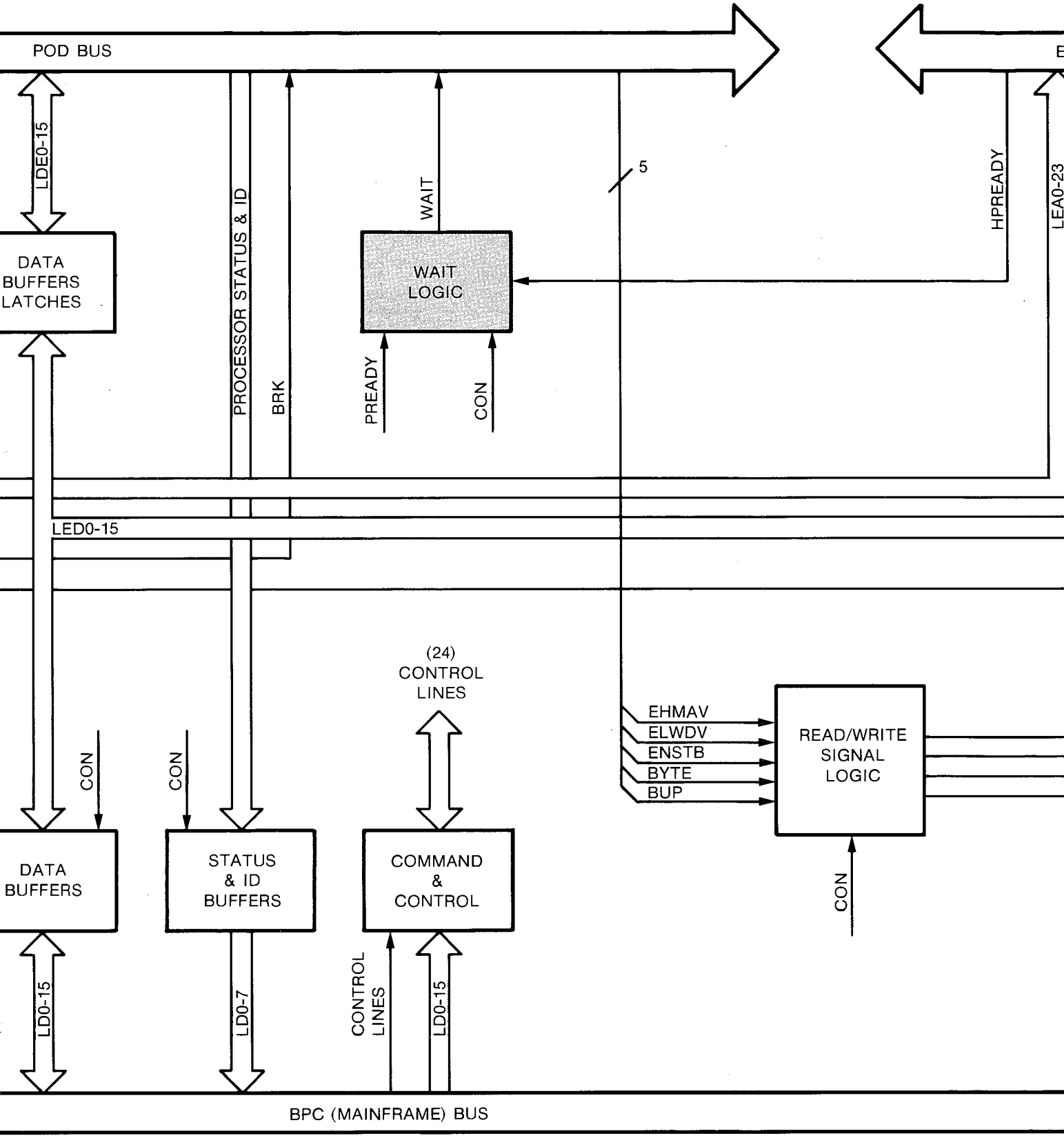
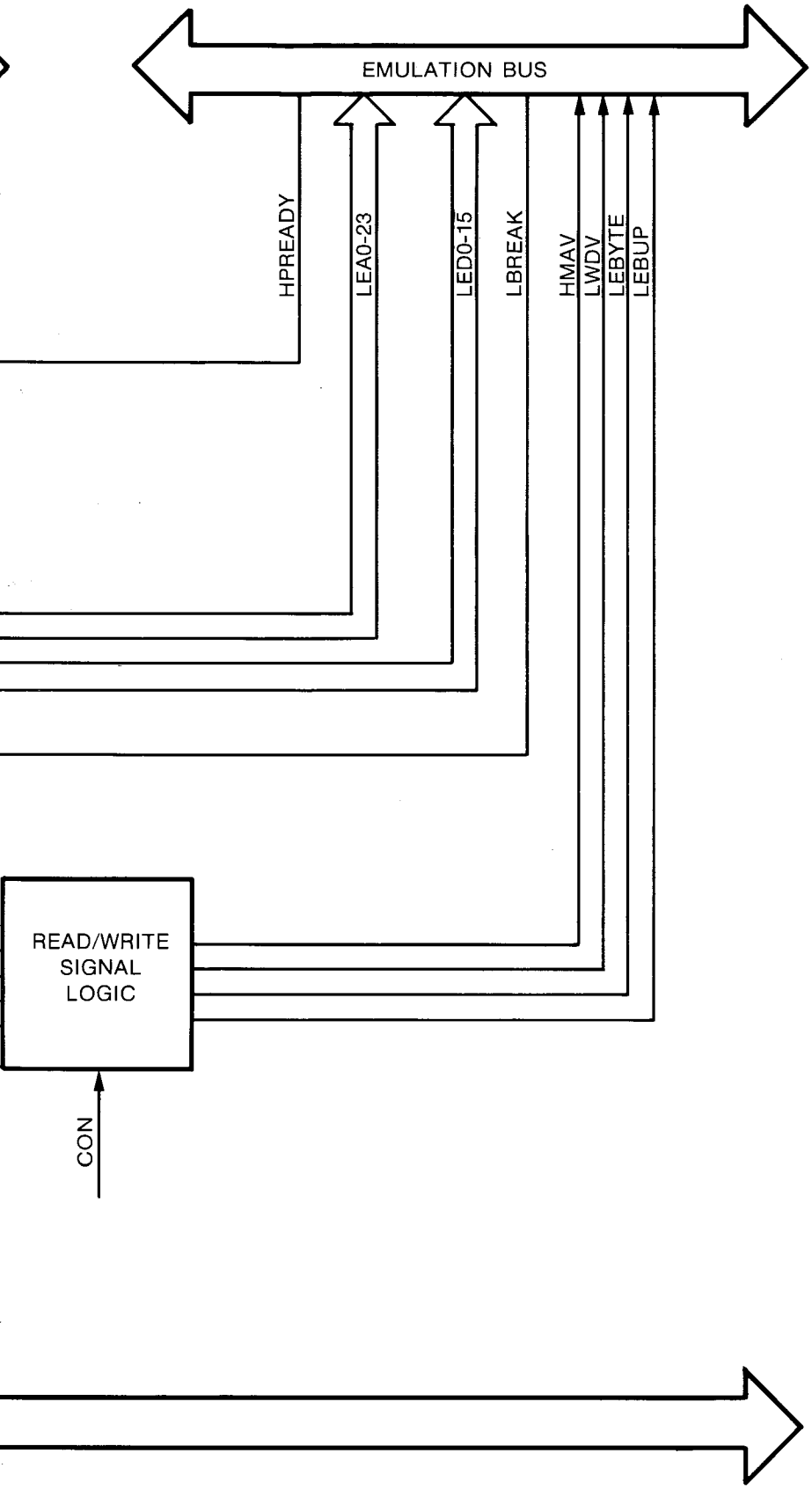


Figure 8-5.
Service Sheet 3A, Control Logic (Sheet 2 of 2)

BLOCK DIAGRAM (64271-66501)




POD BUS
LDE0-15
DATA BUFFERS LATCHES
PROCESSOR STATUS & ID
BRK
WAIT
WAIT LOGIC
PREADY
CON
5
HPREADY
LEA0-23
LED0-15
(24) CONTROL LINES
EHMAV
ELWDV
ENSTB
BYTE
BUP
READ/WRITE SIGNAL LOGIC
CON
CON
CON
DATA BUFFERS
STATUS & ID BUFFERS
COMMAND & CONTROL
LD0-15
LD0-7
CONTROL LINES
LD0-15
BPC (MAINFRAME) BUS



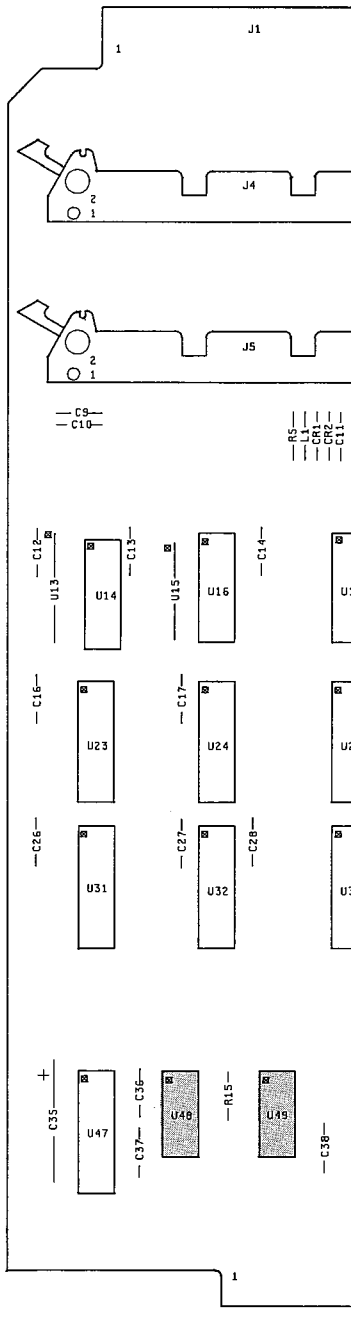


Figure 8-6.
Service Sheet 3B, Control L

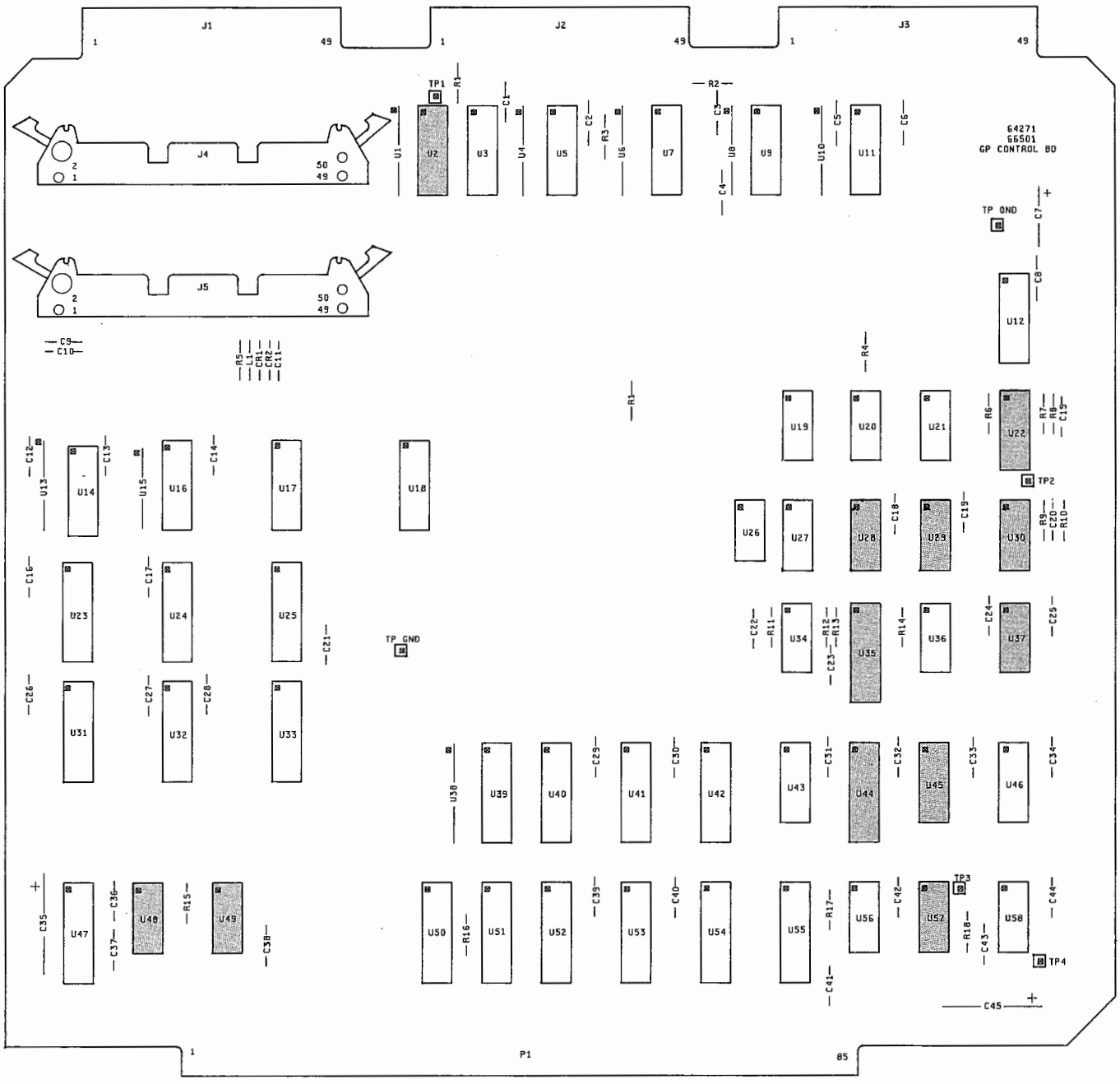
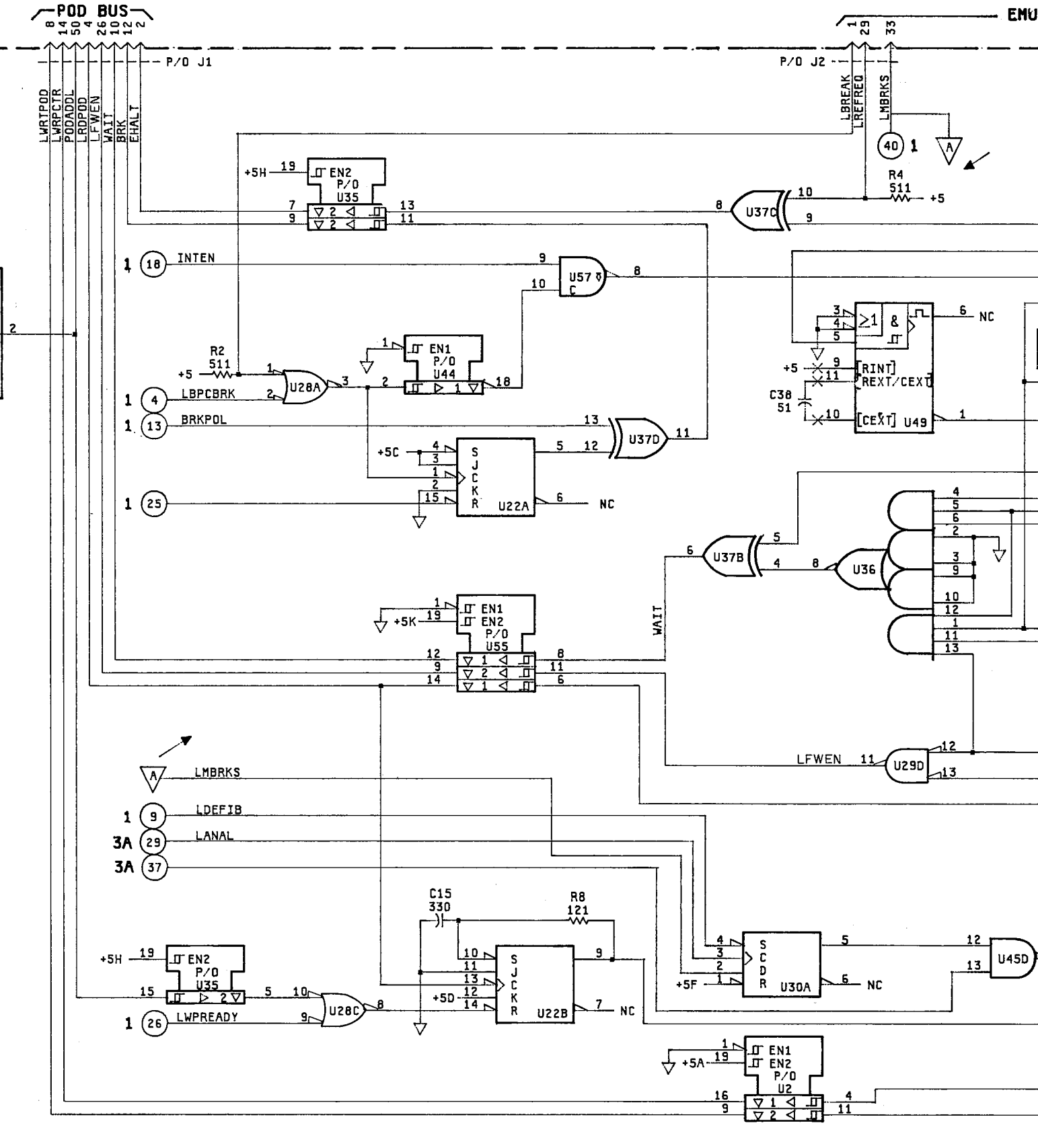
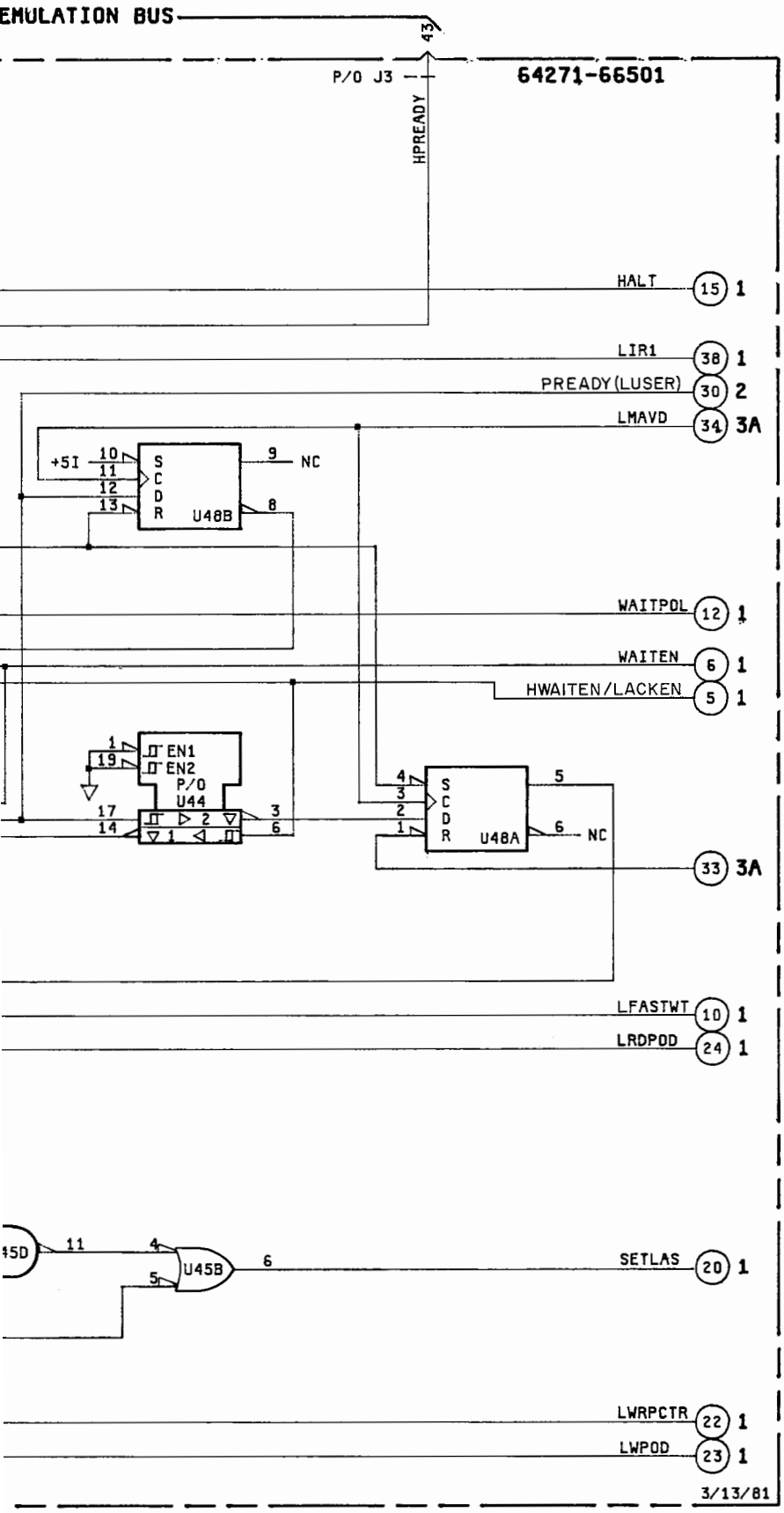


Figure 8-6.
Service Sheet 3B, Control Logic (Sheet 1 of 2)


POD BUS
8 14 50 4 26 10 12 2
P/O J1
LWRTPOD
LWRPCTR
PODADDL
LRDPOD
LFWEN
WAIT
BRK
EHALT
P/O J2
LBREAK
LREFREQ
LMBRKS
40 1
A
R4
511
+5
U37C
+5H
19
EN2
P/O
U35
7
9
13
11
1 18 INTEN
U57
R2
511
+5
U28A
LBPCBRK
BRKPOL
EN1
P/O
U44
18
U37D
+5C
SJCKR
U22A
NC
C38
51
[RINT]
REXT/CEXT
[CEXT]
U49
U37B
U36
+5K
EN1
EN2
P/O
U55
WAIT
LFWEN
U29D
LMBRKS
LDEFIB
LANAL
C15
330
R8
121
+5H
U28C
LWPREADY
+5D
U22B
SCDR
U30A
+5F
NC
U45D
+5A
EN1
EN2
P/O
U2



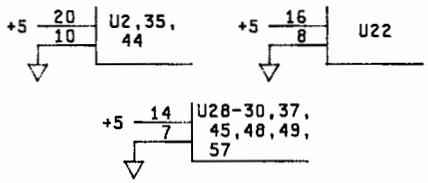
ICS ON THIS SCHEMATIC

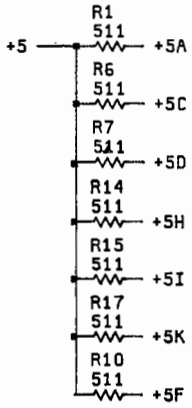
REF. DES.	HP PART NO.	MFG. PART NO.
U2,35	1820-2699	UA74F241
U22	1820-0629	SN74S112
U28	1820-2686	UA74F08
U29	1820-2690	UA74F32
U30,48	1820-2691	UA74F74
U36	1820-0691	SN74564
U37	1820-2692	UA74F86
U44	1820-1633	UA74S240
U45	1820-2684	UA74F00
U49	1820-0261	SN74121
U57	1820-1198	1820-1198

PARTS ON THIS SCHEMATIC

C15,38
R1,2,4,6-8,10,14,15,17
U2,22,28-30,35,37,44,45,48,49,57

IC POWER SUPPLY CONFIGURATIONS





3B

Figure 8-6.
Service Sheet 3B, Control Logic (Sheet 2 of 2)