IBM

Customer Engineering
Manual of Instruction

# 1405

## Disk Storage

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IBM

# Customer Engineering Manual of Instruction

## 1405 Disk Storage

# Contents

# Section 1 Description

The IBM 1405 Disk Storage unit, in combination with data processing systems like the 1401, offers the advantages and facility of large-capacity random access storage. This combination provides an efficient and economical in-line data processing system.

The in-line method of data processing continually maintains the records of a business in an up-to-date status. Any transaction affecting the business can be processed when it occurs, all records and accounts affected being updated immediately. Executives of the organization have available, at any time, information reflecting the status of accounts at that moment.

## Disk Storage General

Customer records in the IBM 1405 Disk Storage unit are magnetically recorded on the surfaces of disks, providing permanent record storage. The 1405 Model 1 has a storage capacity of 10 million alphameric characters utilizing 25 disks. Model 2 has a storage capacity of 20 million alphameric characters utilizing 50 disks.

The model 2 disk storage machine contains 100,000 fixed length records. Both sides of each disk have 200 tracks divided into 5 sectors. Each track within a sector can contain a 200 character record (Figure 1-1).

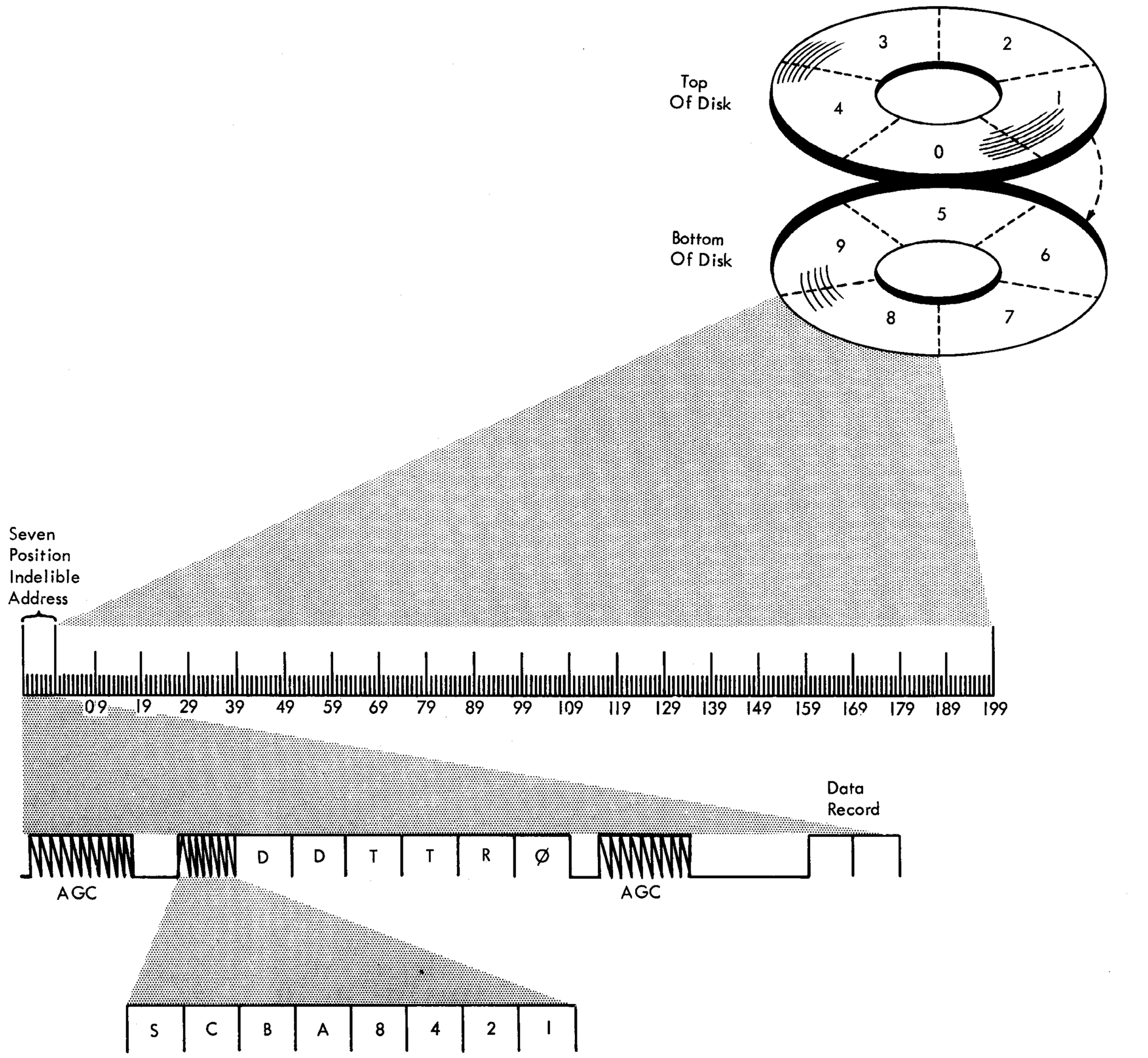



Figure 1-1. Disk Storage Record

Although there are only 50 actual disks (model 2), for the purpose of addressing, the disks are numbered by two's; the bottom disk is numbered 00, the next one above it is 02, then 04 etc., until the top disk (98) is reached. The disks, slightly separated from one another, are mounted on a vertical shaft. The tracks are numbered 00 through 199 beginning at the outside of the disk (Figure 1-2).

We now have a means of locating (addressing) any record on any one of the 50 actual disks. A 5-digit number can be used to identify any disk record; the high-order digit identifies the disk-tens address, the next digit identifies both the disk units and track 100's address, the next two digits identify the track units and tens address, and the low-order digit identifies the record (0-4 for the 5 records on the top side of the disk and 5-9 for the bottom side). For example, address 35439 will locate the record on disk 34, the 18th disk from the bottom, the 143rd track, and record 9 (bottom side of the disk). See Figure 1-3.

The read-write information is transferred to or read from the disks by two read-write heads. These heads are mounted on a fork-shaped access arm. One read-write head is for the top of a disk; the other is for the bottom of the same disk (Figure 1-4). The access arm is mounted on a carriage alongside the disk array. During a seek operation the access arm moves, under electronic control, vertically to seek a disk, and horizontally to seek a track.

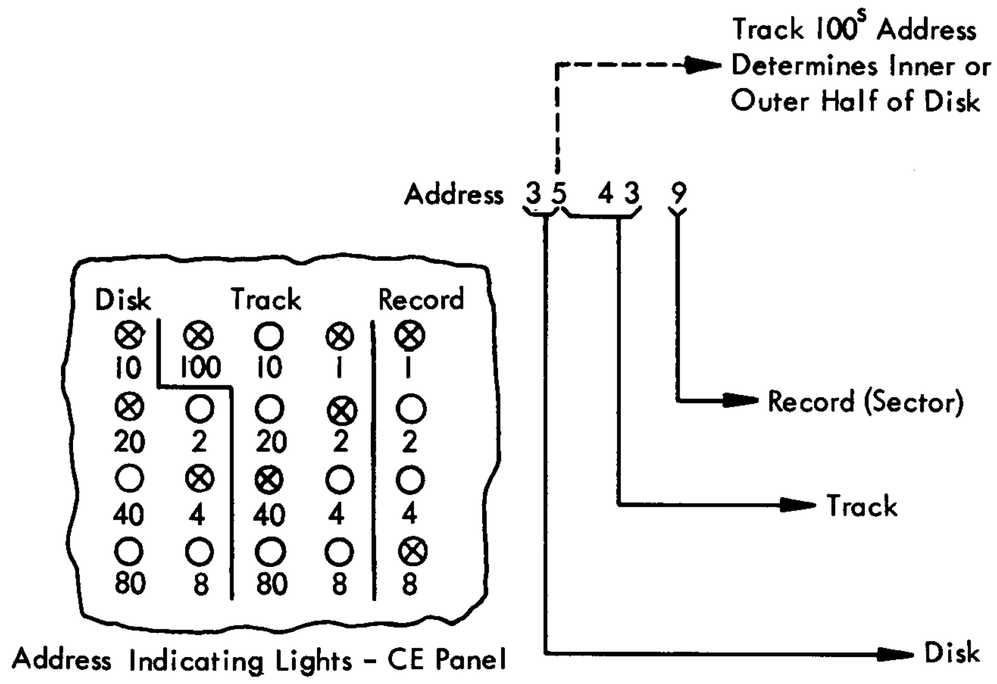



Figure 1-3. Five Digit Address

The 1405 may have as many as two access arms (three when used with a 1410 system), with additional arms installed on an optional basis. Each access arm has individual controls so its movement is completely independent.

The maximum access time for model 2 is 800 ms (700 for model 1). This is the time it takes the arm to move from the innermost track of the bottom disk to the innermost track of the top disk (or vice-versa). Maximum access time between adjacent tracks is 100 ms.

The disk array revolves at a speed of 1200 rpm. At this speed it takes about 10 ms to read or write a 200 character record, once the arm is properly located.

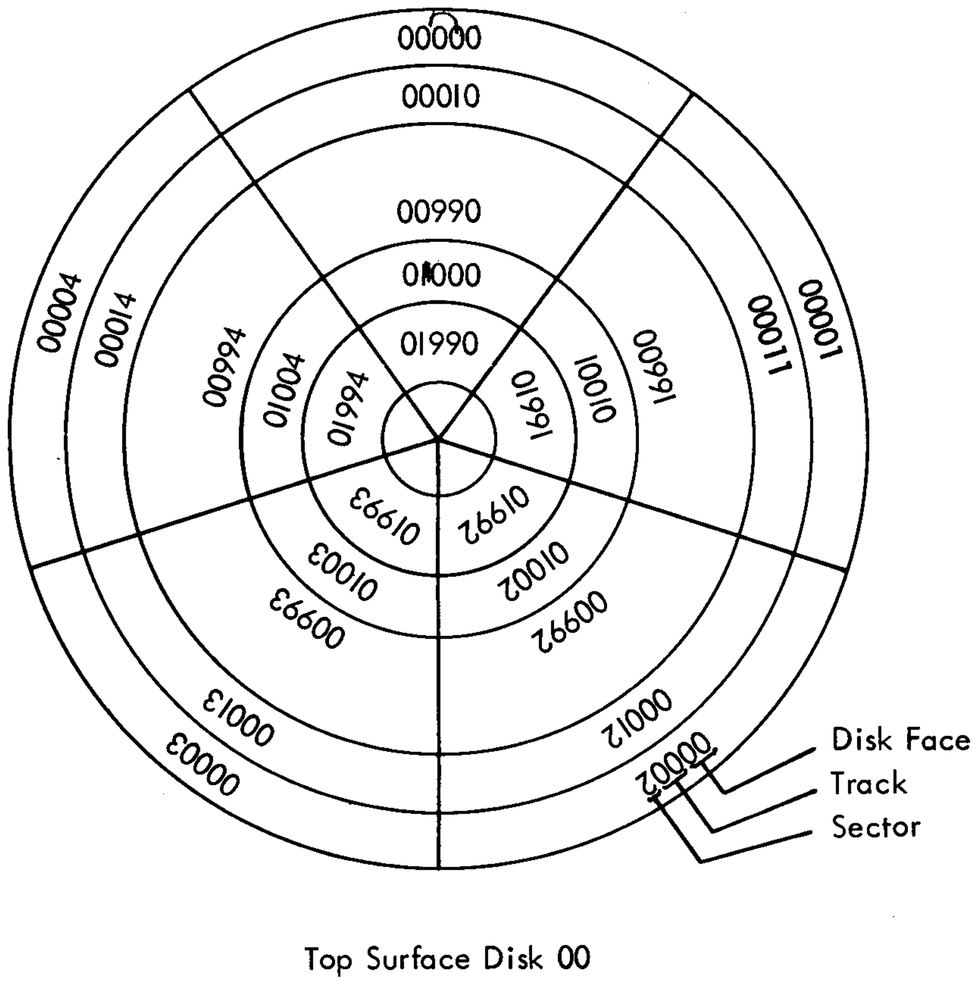



Figure 1-2. 1405 Disk

## Character Coding

Each character is recorded on the disk surfaces in the form of magnetized spots, serially-by-bit, serially-by-character, high order first. The IBM card code is converted to the 7-bit binary-coded-decimal (BCD) sys-

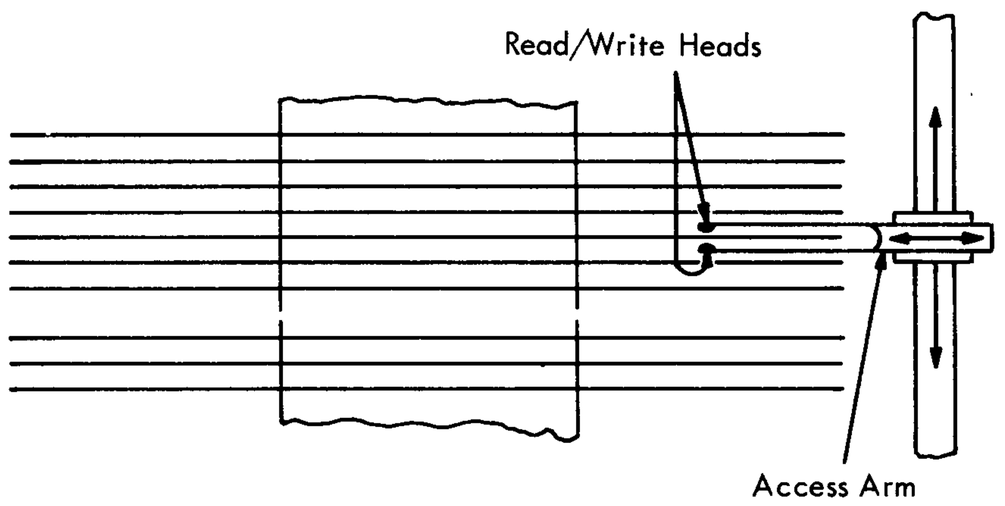



Figure 1-4. Access Arm

tem. A character is made from one or more bits of the 7 BCD code (CBA8421). Figure 1-5 contains a chart showing alphameric characters and BCD code equivalents. The recording sequence of the 7 BCD code is C-B-A-8-4-2-1, when using the move command. When using the load command, the recording sequence is W-C-B-A-8-4-2-1.

## *IBM 1405 Disk Storage Instructions*

Each disk sector has an indelible 7-digit address preceding the 200-character record. The indelible address provides a permanent address for each record in the file. It is recorded on each disk sector at the factory and can be altered only under Customer Engineering supervision.

The address in core storage of the Central Processing Unit (CPU) contains one more position than the indelible address. This is the high-order position and is used to identify the access arm (0-1-2). However, this position is automatically eliminated during the comparison as it has no significance to the record address. (See Figure 1-6).

| CHARACTER | BCD CODE | CHARACTER | BCD CODE |
|---|---|---|---|
| A | BA1 | 6 | C42 |
| B | BA2 | 7 | 421 |
| C | CBA21 | 8 | 8 |
| D | BA4 | 9 | C81 |
| E | CBA41 | * | B84 |
| F | CBA42 | % | A84 |
| G | BA421 | $ | CB821 |
| H | BA8 | & | CBA |
| I | CBA81 | ¤ | CBA84 |
| J | CB1 | . | BA821 |
| K | CB2 | ↑ | CA821 |
| L | B21 | # | 821 |
| M | CB4 | / | CA1 |
| N | B41 | – | B |
| O | B42 | @ | C84 |
| P | CB421 | ∓ | A |
| Q | CB8 | ? | CBA82 |
| R | B81 | ! | B82 |
| S | CA2 | ¢ | A82 |
| T | A21 | ∓ | CBA8421 |
| U | CA4 | Space | C |
| V | A41 | √ | C8421 |
| W | A42 | : | 841 |
| X | CA421 | > | 842 |
| Y | CA8 | = | CA841 |
| Z | A81 | ↓ | CA842 |
| 0 | C82 | " | A8421 |
| 1 | 1 | ) | CB841 |
| 2 | 2 | ; | CB842 |
| 3 | C21 | Δ | B8421 |
| 4 | 4 | ( | BA841 |
| 5 | C41 | < | BA842 |

Figure 1-5. BCD Coding

### Instruction Format

Disk storage operations are initiated by an instruction format that contains the following:

| | | | | |
|---|---|---|---|---|
| 1410 | Op Code<br>X | X-Control Field<br>XXX | B-Address<br>XXXXX | d-Character<br>X |
| 1401 | Op Code<br>X | A-Address<br>XXX | B-Address<br>XXX | d-Character<br>X |

OP CODE

The op code is represented by a single character that defines the basic operation to be performed. When this position in the instruction format contains an M, a move command is indicated. The data recorded on or read from the file will be in the 7-bit mode; each character being recorded as follows: S-C-B-A-8-4-2-1, where the S represents a space bit. Two hundred characters can be written on a disk sector when using the move command.

When the op code position of the instruction contains an L, a load command is indicated. This command permits instructions or data to be read or written on disk sectors similar to the move command. However, the load-write operation causes writing to occur in an 8-bit mode; each character being recorded as follows: S-W-C-B-A-8-4-2-1, where the W represents the bit position for the word mark. As a result of this 8-bit mode, only 176 characters are written or read per disk sector during a load-write or load-read command.

Because word marks are recorded on the disk during a load-write operation, the programmer should be certain that all records on a specific track are written in the same mode (all in load command or all in move command). If a record is read in a mode other than that used to write it, parity errors will occur. Abiding by this programming rule, the operator can cause the machine to perform a full track read operation successfully (five disk records are read sequentially using one instruction).

1401-A-ADDRESS OR 1410 X-CONTROL FIELD

The A portion of the CPU disk storage instruction always contains %FX. The %F signals that the disk storage unit is to be selected. The X represents the digit used to perform the following operations:

1. X = 0; seek a disk record.
2. X = 1; single record operation. One record is read or written (one 200 character record or 176 characters if in load op).
3. X = 2; full track operation. An entire track is read or written (5 records).
4. X = 3; write check operation. Data written on a disk in a preceding write operation is read from the disk and compared with the data in core storage.

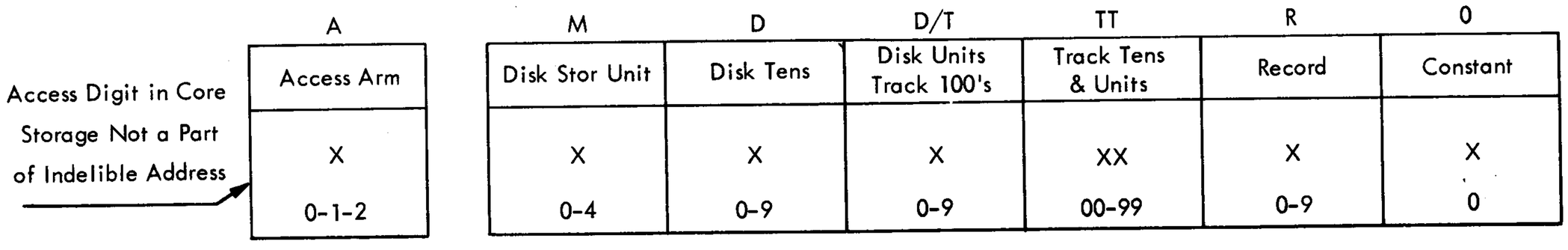



Figure 1-6. Record Address Format

5. X = 4; write address. This operation is performed only under CE supervision. It requires the use of the Write Address key-lock in addition to the instruction. The operation provides a means for rewriting the indelible address.

Branch if Indicator ON { BXXXN, BXXXV, BXXXW, BXXXX, BXXXY } XXX = I-address

B-ADDRESS

The B portion of the CPU disk storage instruction specifies the high-order position in core storage of the 8-digit record address.

d-CHARACTER

The d-character modifies an operation code as shown:

| Op Code | d-Character* | Operation |
|---|---|---|
| L/M | R (or S 1410) | Read |
| L/M | W (or X 1410) | Write |
| B | N | Test address invalid, access inoperative |
| B | W | Test wrong-length record indicator |
| B | X | Test unequal address compare indicator |
| B | Y | Test for any disk unit error condition |

*d-Character is not required on a seek or write check instruction.

### Assembled Disk Storage Instructions

The following list contains all of the valid disk storage instructions:

| OP | ASSEMBLED INSTRUCTION |
|---|---|
| Seek | M%F0XXX(XX) |
| Read Single Record | L/M%F1XXX(XX)R |
| Read Full Track | L/M%F2XXX(XX)R |
| Write Single Record | L/M%F1XXX(XX)W |
| Write Full Track | L/M%F2XXX(XX)W |
| Write Check | L/M%F3XXX(XX) |

*Seek Function.* When this function is initiated, the access arm servos to the disk and track specified by the disk record address. The CPU can continue processing while the access arm is in motion.

If the access arm is already at the disk to be used, a seek operation need not be given. The correct record is selected during the read or write instruction.

*Read Function.* A read operation causes data to be read from the file into the CPU core storage. Reading is stopped at the end of the 200th character (READ SINGLE RECORD OP) or at the end of the 1000th character (READ FULL TRACK).

A group mark with a word mark (GMWM) must be placed one position beyond the last position reserved in cores for the disk record(s). If the GMWM does not occur simultaneously with an end-of-record signal, the WRONG LENGTH RECORD indicator turns on and reading stops.

*Write Function.* A write operation causes CPU core storage data to be written on a disk in the file. Writing is stopped at the end of the 200th character (SINGLE RECORD OPERATION) or at the end of the 1000th character (FULL TRACK OPERATION).

A GMWM must be placed one position beyond the last position reserved in cores for the disk record(s). If the GMWM is sensed before the END-OF-RECORD signal is generated, the remainder of the disk record(s) fills with blanks and the WRONG LENGTH RECORD indicator is turned on.

*Write Check Function.* A write check operation must be performed following a write operation. No other file operation (on any file) can be performed until the data written, during the write operation, is checked.

This instruction causes a comparison to be made between the data in core storage and the data just written on the file. The system is programmed to read the last record that was addressed by the CPU program. Either a single record or a full track is checked depending on the type of write operation last performed. If any characters on the record(s) do not agree with the characters in core storage, the READ BACK CHECK ERROR indicator turns on (E or F channel indicator in 1410).

*Branch if Indicator ON Function.* After each file read or write operation, the CPU program must test for error indications to prevent the processing of unusable data. The program may then call for a stop, a repeat of the same program, or a continuation of the program.

The d-character specifies the indicator tested.

If the indicator tested is on, the next instruction is taken from the CPU I-Address. If the indicator is off, the next sequential instruction is taken.

INDICATORS

*Read-Write Parity Check or Read-Back-Check Error.* This indicator is turned on if an even bit parity is detected when reading or writing information to or from file. It will also be turned on if an unequal compare is detected during a write check operation.

*Wrong Length Record.* This indicator turns on if a GMWM does not occur simultaneously with an end-of-record signal from the file. If on, it indicates that the number of characters, read from, or written on the disk is not equal to 200 or 1000 characters (M Op Code) or 176 or 880 (L Op Code) Characters.

*Unequal Address Compare.* This indicator turns on if the disk record address in core storage does not agree with the indelible address on the disk record. This is an automatic comparison; it does not require programming. If an unequal address occurs, reading from or writing into the file is prevented; at the end-of-address compare time the processor proceeds to the next instruction.

*Any Disk Storage Error Condition.* This indicator turns on if any of the other indicators are on. The program may test this indicator and if off proceeds with the normal program. If on, the program should test the other indicators to determine the necessary corrective action.

## General Data Flow

The general data flow for the IBM 1405 is shown in Figure 1-7. The drawing shows the 1405 monitoring a CPU by means of an attachment unit (ATU).

The 1405 responds to seven different instructions. These seven instructions cause the 1405 to perform one, or more, of three basic functions; seek, read, and write. To accomplish these functions, the 1405 employs the following functional units:

1. Attachment Unit
2. File Control Unit
3. File Electronics Gate
4. Relay Gate.

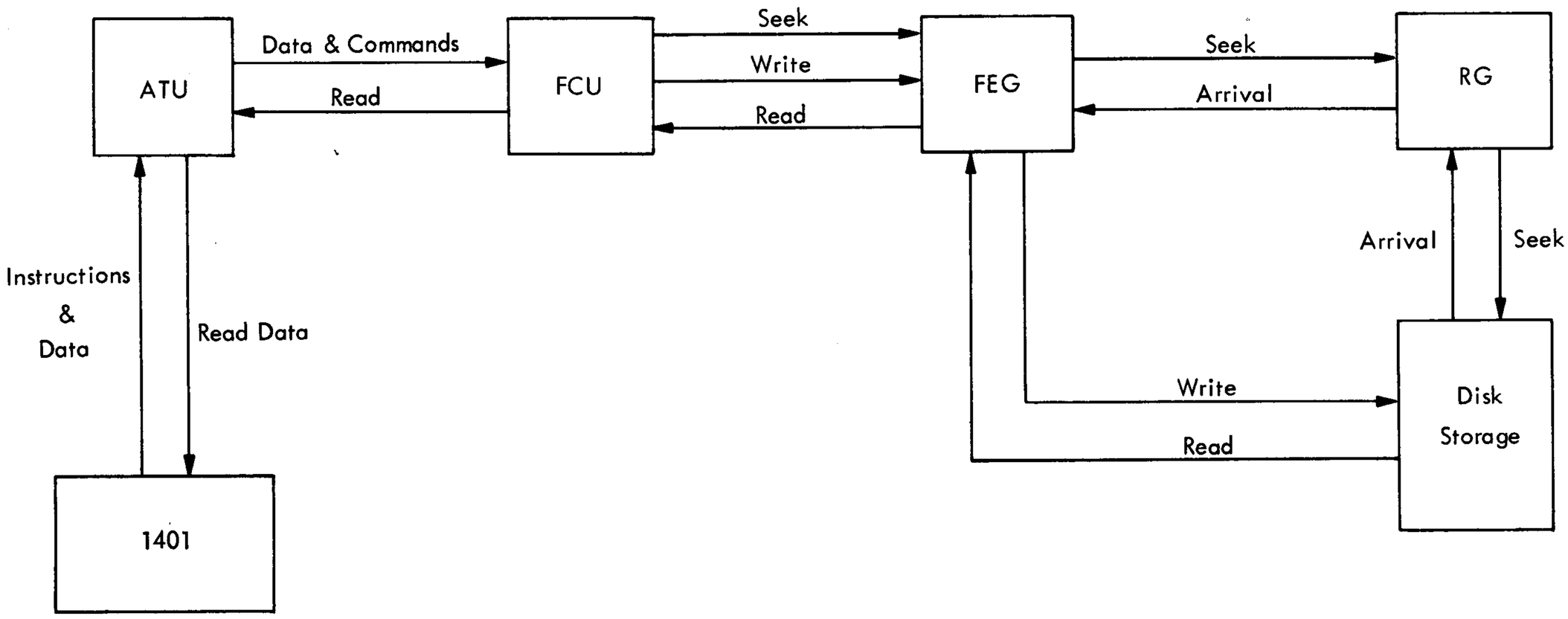



Figure 1-7. General Data Flow

### Attachment Unit (ATU) — 1401

The ATU continually monitors the output from the 1401 core storage unit. During I-cycles, when the 1401 reads out any disk storage instruction, the ATU decodes the instruction into the appropriate disk storage command. The command is then transmitted to the file control unit. Part of the ATU circuitry is actually located on gate 02A8 in the 1401.

The ATU also functions to power and level-set lines, control the 1401 clock (during file operations), and store 1405 errors until sensed by the 1401 at the completion of the disk storage operation.

### Attachment Unit (ATU) — 1410

The ATU continually monitors the data on the output channel. When the 1410 reads out a 1405 instruction, the necessary control lines are established between the 1410 and the 1405 through the ATU.

The ATU also contains the comparing circuits required for the indelible address and write check comparisons. In addition, it contains the error latches used to store 1405 errors until sensed by the 1410.

### File Control Unit (FCU)

The FCU comprises the greater part of the 1405 circuitry. The basic function of the FCU is to carry out the seven disk storage commands received from the ATU.

In addition, it checks the data to and from the disk storage unit for parity. It also "serializes" parallel-bit data from core storage and changes the serial-bit data read from the disk storage unit, to parallel-bit data for entry into core storage.

### File Electronic Gate and Relay Gate (FEG and RG)

Components in these two gates provide circuits required to execute the controls set up by the FCU.

The read-write circuits, null detectors, and head selection circuits are the basic components within the File Electronic Gate.

The Relay Gate, as the name implies, contains the relays required to perform the seek function.

### Disk Array

The arrangement of the disks in the file unit is shown in Figure 2-1. The file contains 52 disks (mod 2); however, only 50 of these are used for data storage. The top and bottom disks are dummy disks, used to aid in the regulation of stray air currents within the file. The recording disks are numbered consecutively from bottom to top, 00 to 98. The whole disk array is rotated at a speed of 1200 rpm.

Data is stored on both the top and bottom of each recording disk. There is one read-write head for addressing the top side of the disk and one for the bottom. Both of these heads are mounted in one access arm (Figure 2-2) which may be positioned to straddle any of the 50 disks.

When the access arm is addressed to any particular disk, it may be moved inward or outward to place the read-write heads at various radial distances from the center. The arm may be detented at 202 different positions. When the arm is detented at any one of its 202 positions, a circular path on the surface of the disk moves past the read-write heads. These circular paths are called tracks. Each track includes the paths on both the top and on the bottom of the disk.

The innermost track and the outermost track on each disk are reserved for use by the CE when servicing the file. The 200 remaining tracks are used for storage of accounting records.

With the disk rotating at 1200 rpm, each revolution requires 50 ms. Using a bit frequency of 186 kilobits/sec, two complete 200 character records can be stored in each $\frac{1}{5}$ of the track circumference; one on top side and one on bottom side. Thus, a total of 10 records can be stored on each disk storage track. Record positions 0, 1, 2, 3, and 4 are on the top side of each disk 5, 6, 7, 8, and 9 are on the bottom side.

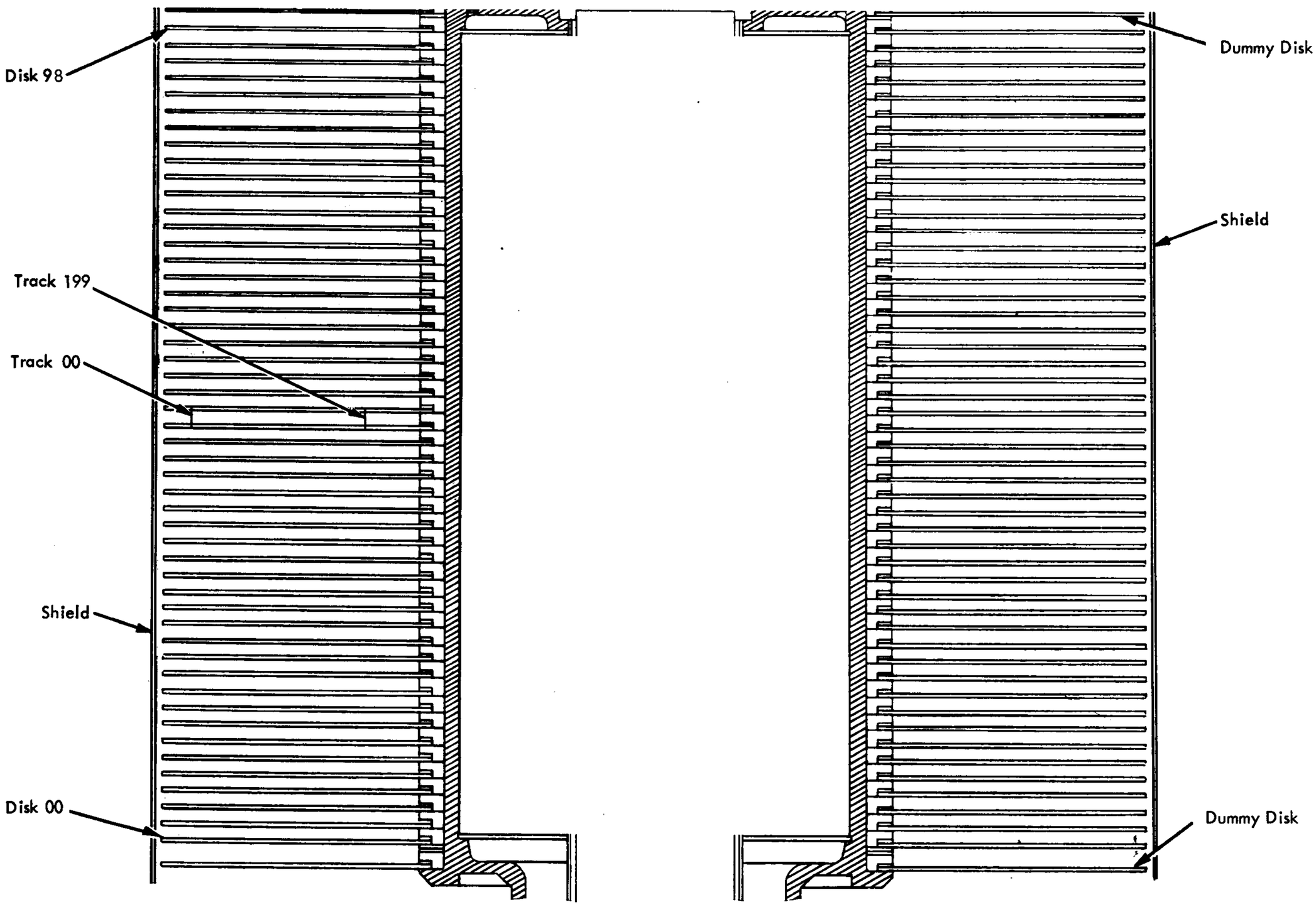



Figure 2-1. Disk Array

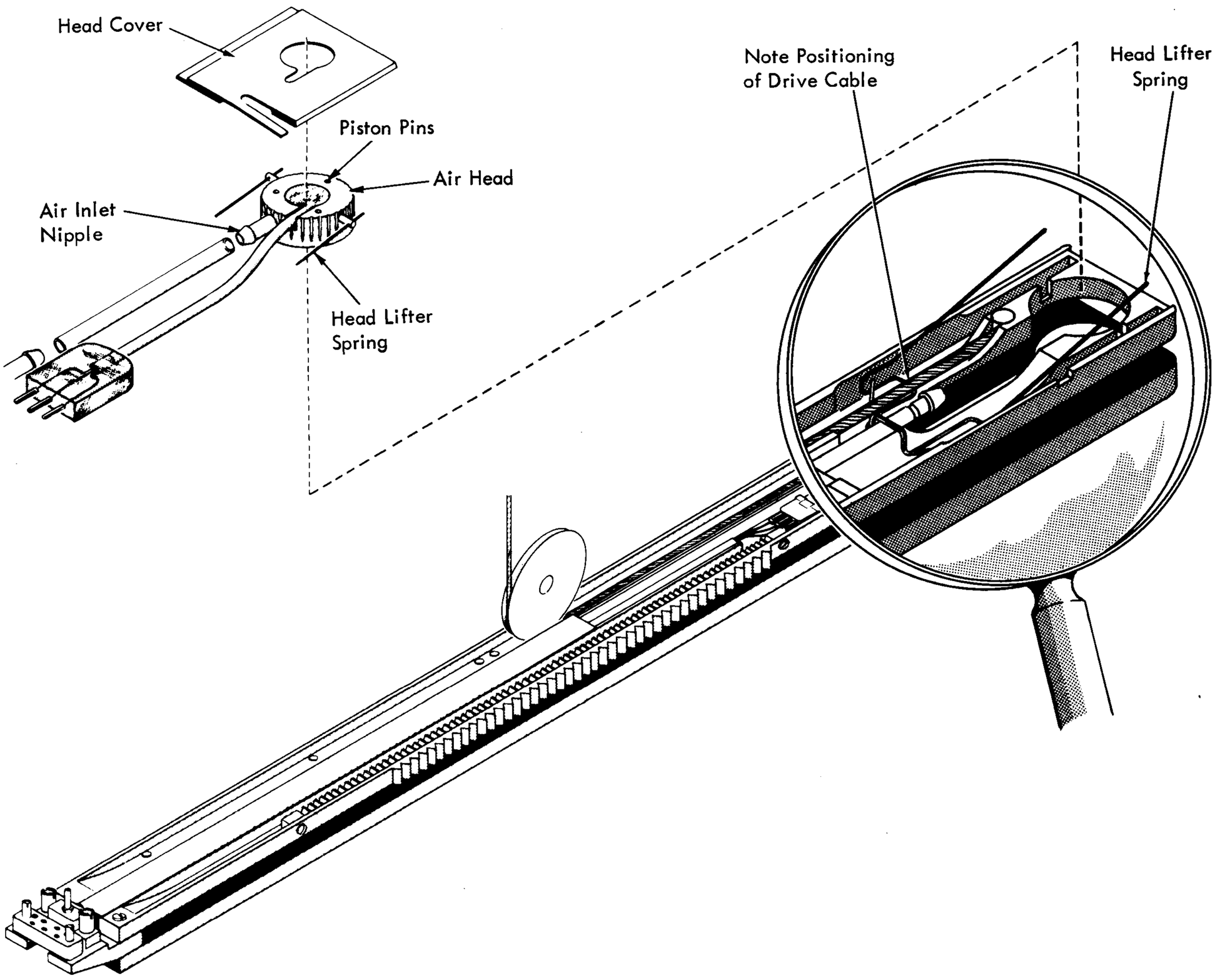



Figure 2-2. Access Arm Assembly

### *Disk and Track Selection*

In order to select a given track, the arm must be moved from its previous track location to the new track location. This involves one of three types of movement sequences:

1. To move to a numerically higher track address on the same disk, the access arm must move inward only.
2. To move the arm to a numerically lower track on the same disk, the arm must move outward only.
3. To move to an address on another disk; the arm must first be moved all the way out, then up or down to the new disk location, and inward to the selected track.

Since the third sequence includes the movements used in the other two, it is used as the example for an explanation of disk, track, and record selection.

### *Access Mechanism*

In order to accomplish the necessary movement of the arm, an access mechanism is provided. This consists basically of the following components (Figure 2-3):

1. A carriage on which the arm is mounted for horizontal movement.
2. A way on which the carriage is mounted for vertical movement.
3. Two access cables, a capstan, two clutches, and a motor to provide movement to the arm and carriage.
4. A disk detent to keep the carriage fixed in place while the arm moves into the disk array.
5. A track detent to fix the arm's position at the correct track.

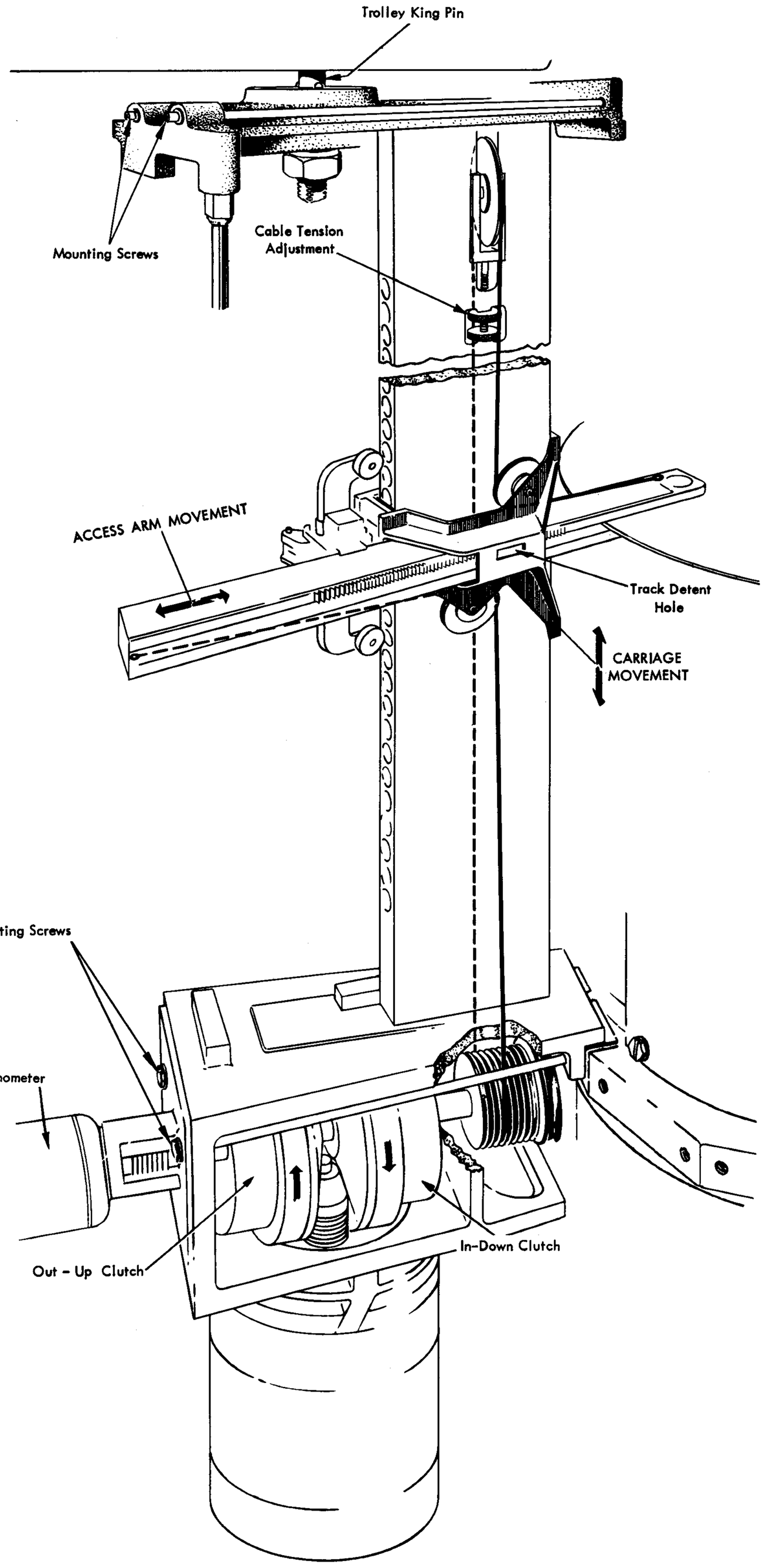



Figure 2-3. Access Mechanism

### Carriage and Disk Detent

In order to allow the arm to move vertically, it is held in a carriage that is free to move vertically on a specially constructed way (Figure 2-3). The arm itself is free to move horizontally within special guides on the carriage. However, the carriage cannot move vertically at the same time the arm is moving horizontally without damaging the disks. Therefore, the disk detent is provided to lock the carriage to the way while the arm is extended or retracted. The fail-safe bar is provided to lock the arm all the way out, in the home position, while the carriage moves vertically. The disk detent and the fail-safe bar are mechanically linked so that one or the other must be engaged at all times. This linkage (Figure 2-4) is called the fail-safe interlock.

When the arm is retracted to the home position, out-air pressure is applied to the disk detent piston to unlock the carriage so that it can move. When the correct disk has been located, in-air pressure is applied to the disk detent piston to lock the carriage to the way and unlock the arm.




Figure 2-4. Disk Detent Operation

### Capstan and Cables

The capstan and cables provide a method of applying power to move the arm and the carriage. The two cables are wrapped around the capstan in opposite directions (Figure 2-5). One of these cables goes up the far side of the way, over the tension adjusting pulley, down and through a pulley on the carriage and is fastened to the front end of the arm. The other cable goes up the near side of the way, through a pulley on the carriage and is fastened to the rear end of the arm.

If the disk detent locks the carriage to the way, rotating the capstan clockwise causes the arm to move in; rotating it counterclockwise causes the arm to move out.

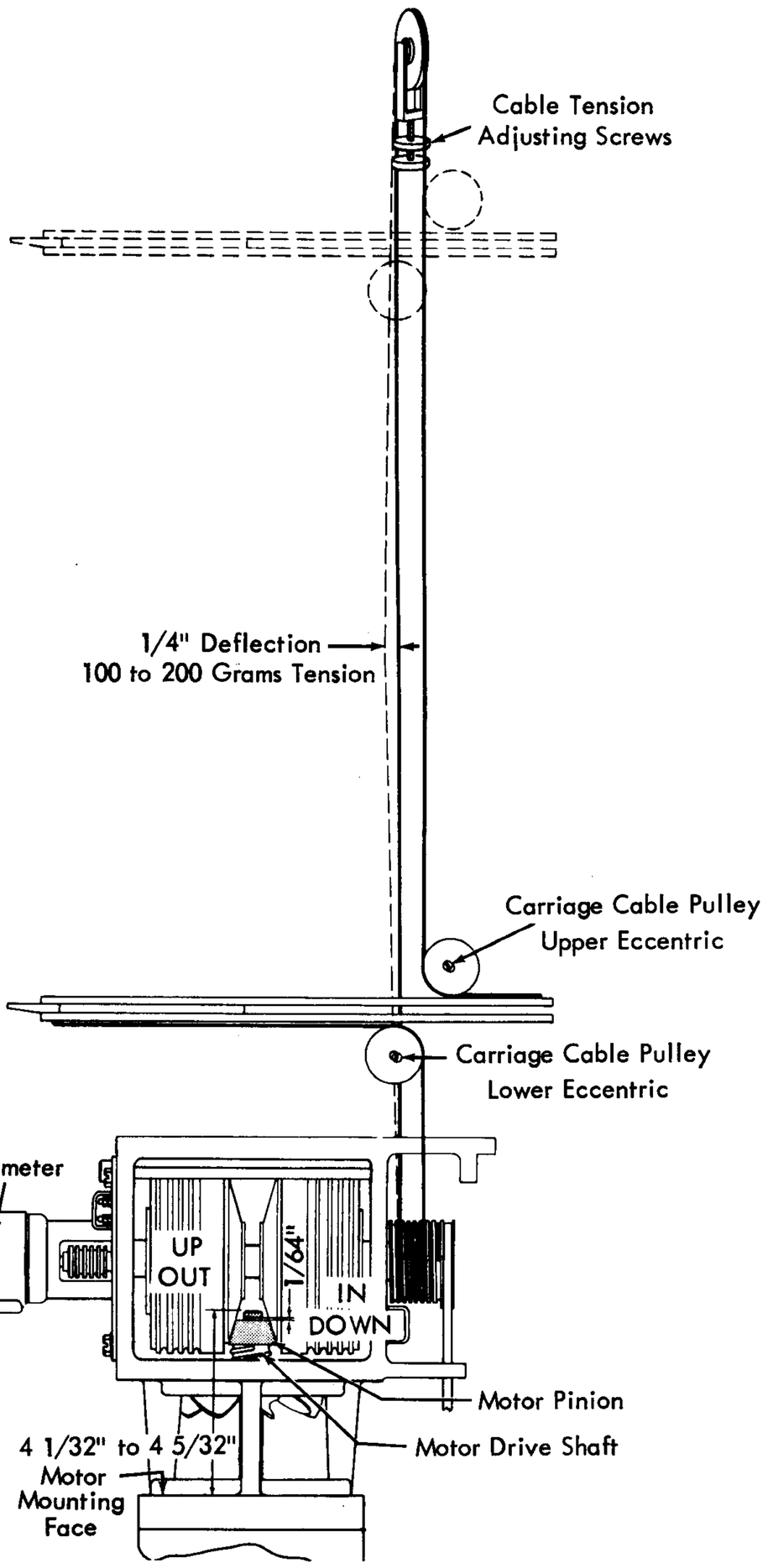



Figure 2-5. Drive Clutch and Cable

Clockwise capstan movement causes the carriage to move down if the disk detent is retracted; counterclockwise capstan movement causes the carriage to move up.

### Servo Clutches

The capstan can be caused to rotate in either direction by energizing one of two clutches attached to the capstan shaft. Figure 2-6 shows an exploded view of one of these clutches. The rotor is fastened to the capstan shaft, and the clutch housing is free to move about the shaft. The two clutch housings making up the pair of servo clutches are each positively driven in the opposite direction. A ⅓-hp motor operates a pinion drive to provide the rotational force (Figure 2-7).

The space between the rotor and the housing is filled with powdered iron and graphite. Application of a direct current to the magnet coil causes the powdered iron particles to align themselves and form a magnetic bond between the continuously running housing and the rotor.

The servo control circuits are designed so that only one clutch is energized at a time. If one of these clutches is energized to produce the desired movement of the arm or carriage, the other will be energized as the addressed position is reached to cause dynamic braking.

### Track Detent

Once the arm has been moved to the correct track, a track detent is driven by air pressure into a land in the rack on the side of the arm (Figure 2-8). In order to allow the rack to have teeth large enough to effectively hold the arm in place, four detents are provided. Thus, one arm-rack-tooth is used to hold the arm for one of four tracks, depending on which detent is used. The detents are air operated and spring returned.

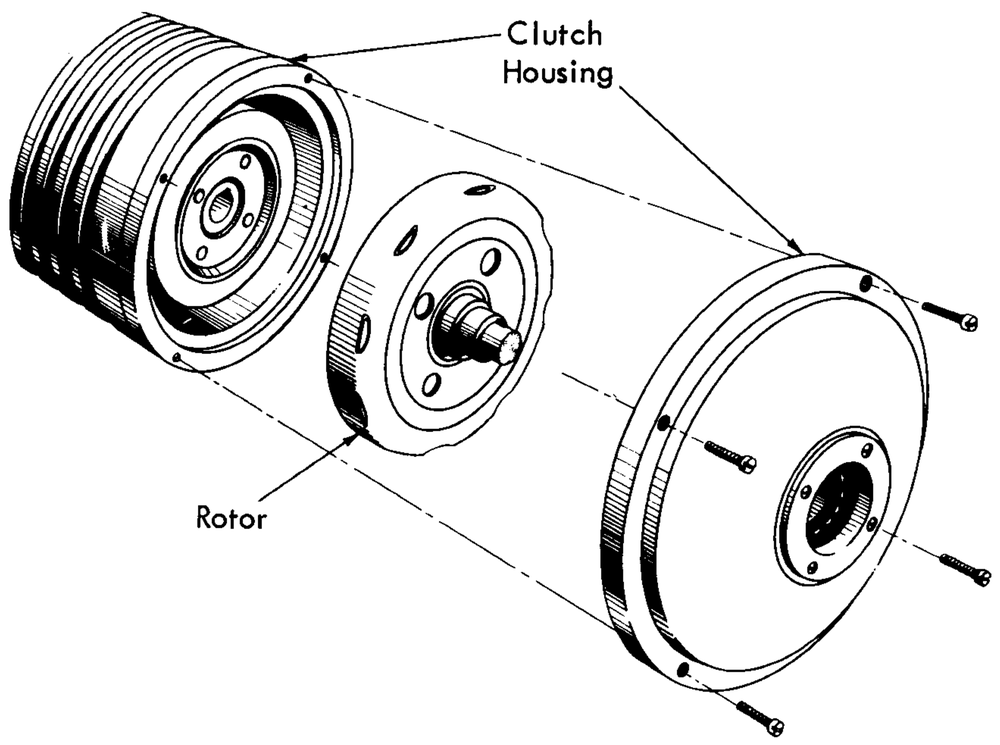



Figure 2-6. Exploded View of Magnetic Clutch

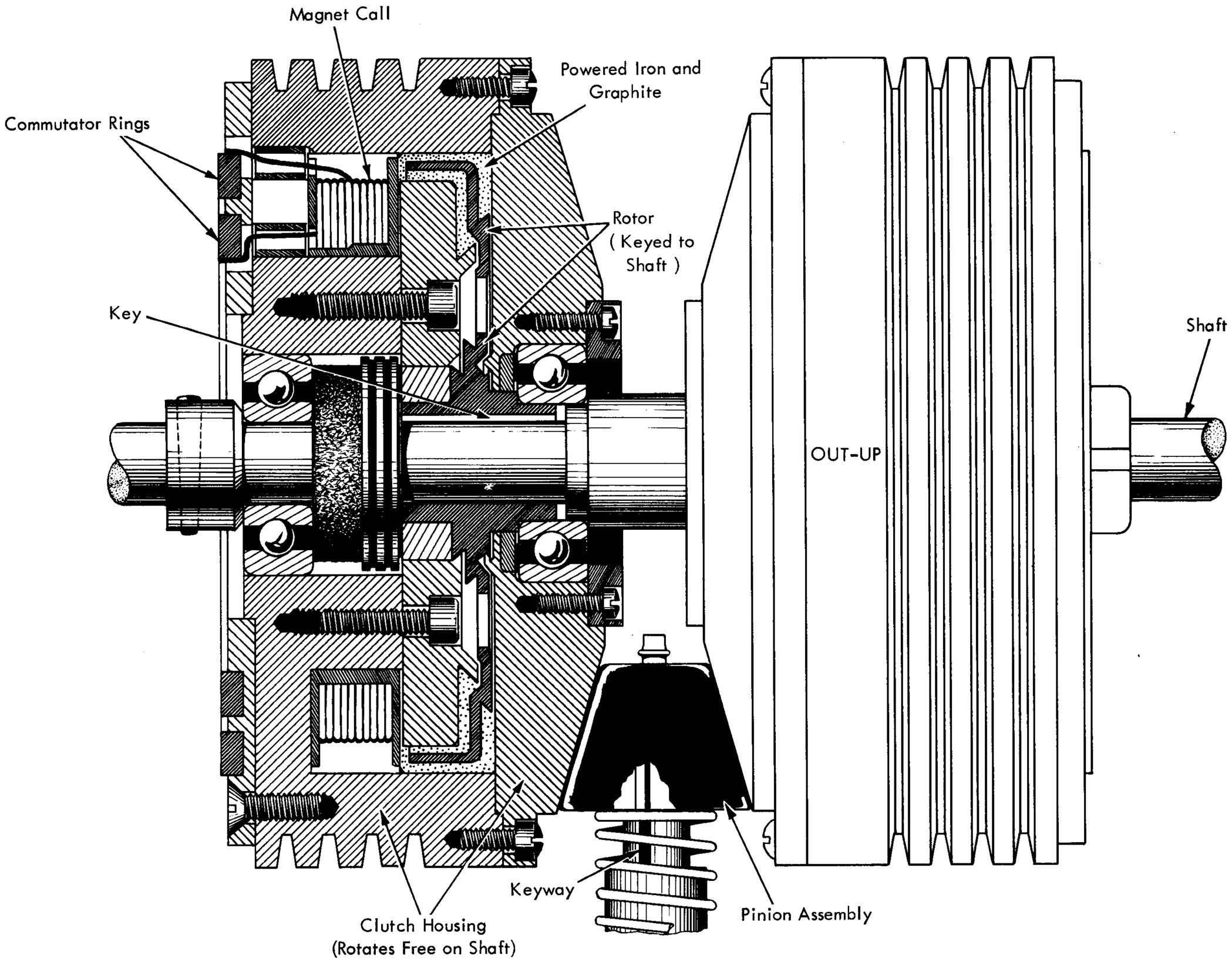



Figure 2-7. Magnetic Clutch Assembly

## Record Selection

When the access arm is detented so that its read-write heads are scanning a particular track, further selection is necessary to obtain one specific record.

The selection between the records on the top side of the disk and those on the bottom is accomplished by electronic switching determined by the address.

The selection of one of the five records on the selected side of the selected track is accomplished with the aid of the record heads. These heads are mounted on the top casting at intervals of 72 degrees (single access). A permanent magnet mounted on the top dummy disk moves past one record head every 10 ms. The record address causes the record selection circuit to select the proper head and provides a record start pulse at the correct time.

## Read-Write Heads

The actual reading and writing of a disk storage record is done by the read-write heads. Figure 2-9 shows the physical arrangement of the coils used for reading or writing on the disk. The read-write coils have a core consisting of 5 laminations, while the erase coil core has 11 laminations. The erasing of a broader path than is used for writing and reading helps minimize extraneous noise. The read-write head is cast in plastic and mounted in a larger mechanism called the air head.

Figure 2-2 shows the air heads as they are mounted in the access arm. The purpose of the air heads is to position the read-write head in relation to the disk. When the access arm is advanced from a position clear of a disk to a position straddling a disk, the read-write heads must be in a retracted position to avoid striking

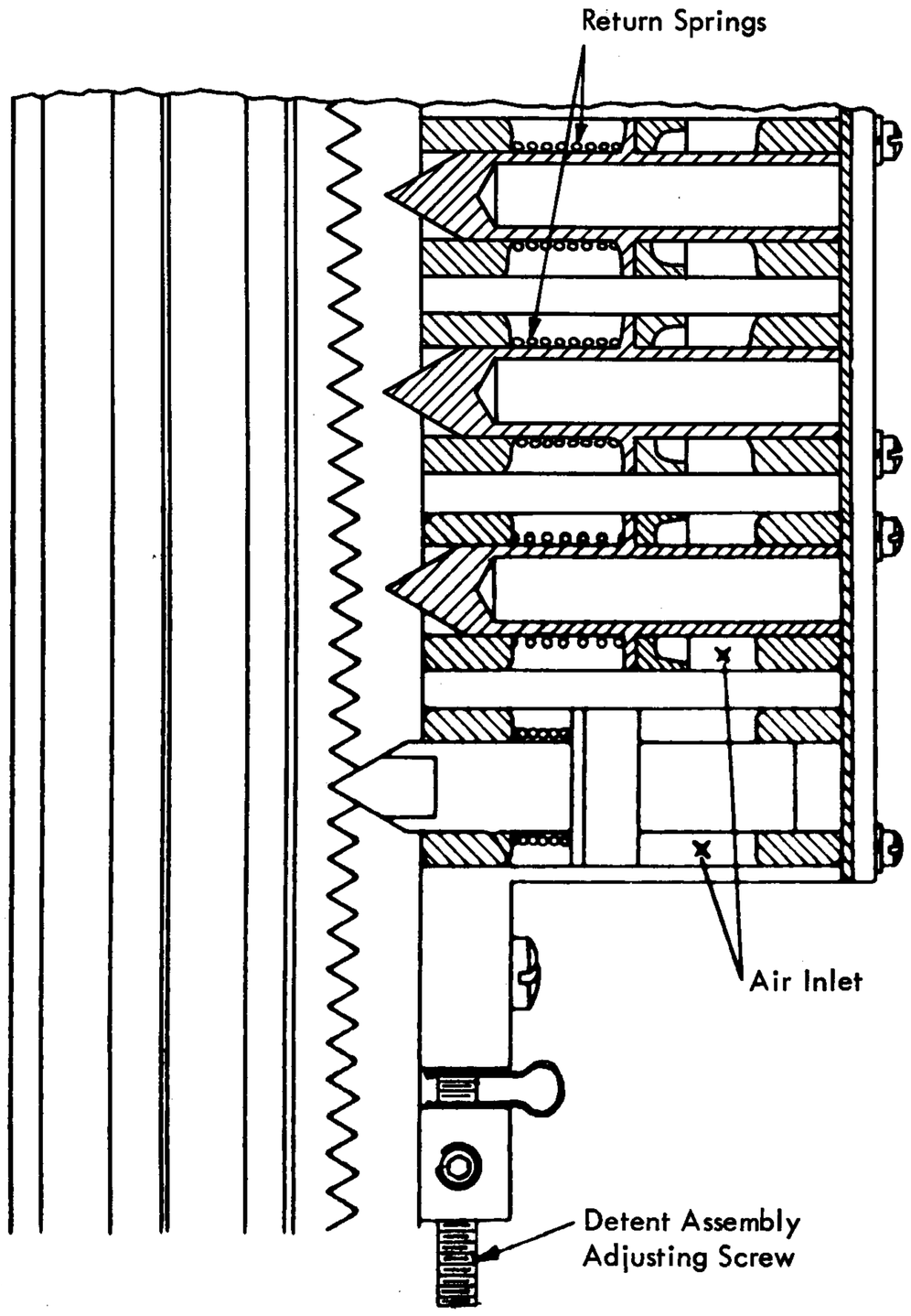



Figure 2-8. Track Detents

the edge of the disk. When the arm is detented at a track address, the read-write heads must be positioned close to the disk for reading and writing.

The positioning of the air head (and the read-write head which it contains) is controlled by the application or removal of air pressure. If no air pressure is applied to the head, the springs act against the gimbal pins to hold the head against the head cover. When air pressure is applied to the air head, the three pistons are forced to protrude from the head against the head cover. The stationary head cover limits the movement of the pistons, forcing the head away from the cover and toward the disk. To keep the head from scraping the disk, air is expelled against the disk from six small orifices in the head. The applied air pressure thus causes two distinct forces to impel the head in opposite directions. The point at which these forces balance allows the head to ride about .001" from the surface of the disk. When air is applied, the heads are said to be down, even though the bottom head is moved upward to reach its active position.

### Air Valve Solenoids

Seven air valve solenoids control the air used in the disk storage unit. Four of these solenoids control the air that is used to operate the four track detents (air operated spring returned). The head solenoid controls the air used to position the read-write heads. The two remaining solenoids control the operation of the disk detent; one controls the disk detent IN action, the other controls the disk detent OUT action.

### *Air Compressor*

The air compressor is housed in a remote cabinet. The compressor is designed to supply about 100 psi of air pressure to a maximum of 12 accesses. A 208-v or 230-v, 3-phase, 3-hp motor is used to drive the compressor. A three-position rotary switch, located on the disk storage starter box, controls the operating mode of the compressor and disk storage unit. The positions on the rotary switch provide for local-manual, local-automatic, and remote-automatic operation. In the local manual mode, the 1405 operates independently of the processing system and DC power can be controlled at the file starter box. In the local-automatic mode, DC power can be turned on or off at the file starter box. In the remote automatic mode, all functions of the 1405 are controlled by the processing unit (see POWER SEQUENCING, Section 11).

The compressor operates at a speed of 760 rpm and delivers 11 cfm of air at 90 psi. The air is delivered directly into an aftercooler (Figure 2-10) and then to a filter and water trap. It can then go to the unload valve for exhaust purposes or through the check valve to the air receiver tank in the file.

The check valve prevents the air in the receiver tank from exhausting back through the unload valve. The unload valve opens to the atmosphere when the pressure reaches approximately 93 psi. The water that has collected in the water trap will be expelled through the unload valve at this time. The unload valve closes to the atmosphere when the pressure reaches approximately 70 psi. A safety valve, set at 100 psi, is placed between the aftercooler and the water trap. If the unload valve fails to operate, the safety valve will prevent the system from overloading.

The air flowing down stream from the water trap is relatively free of condensed water. This air then flows through two cotton filters, where the oil carried over with the compressed air is removed. From the cotton filters, the air flows to the receiver tank located in the disk storage unit.

The receiver tank contains a valve on the bottom of

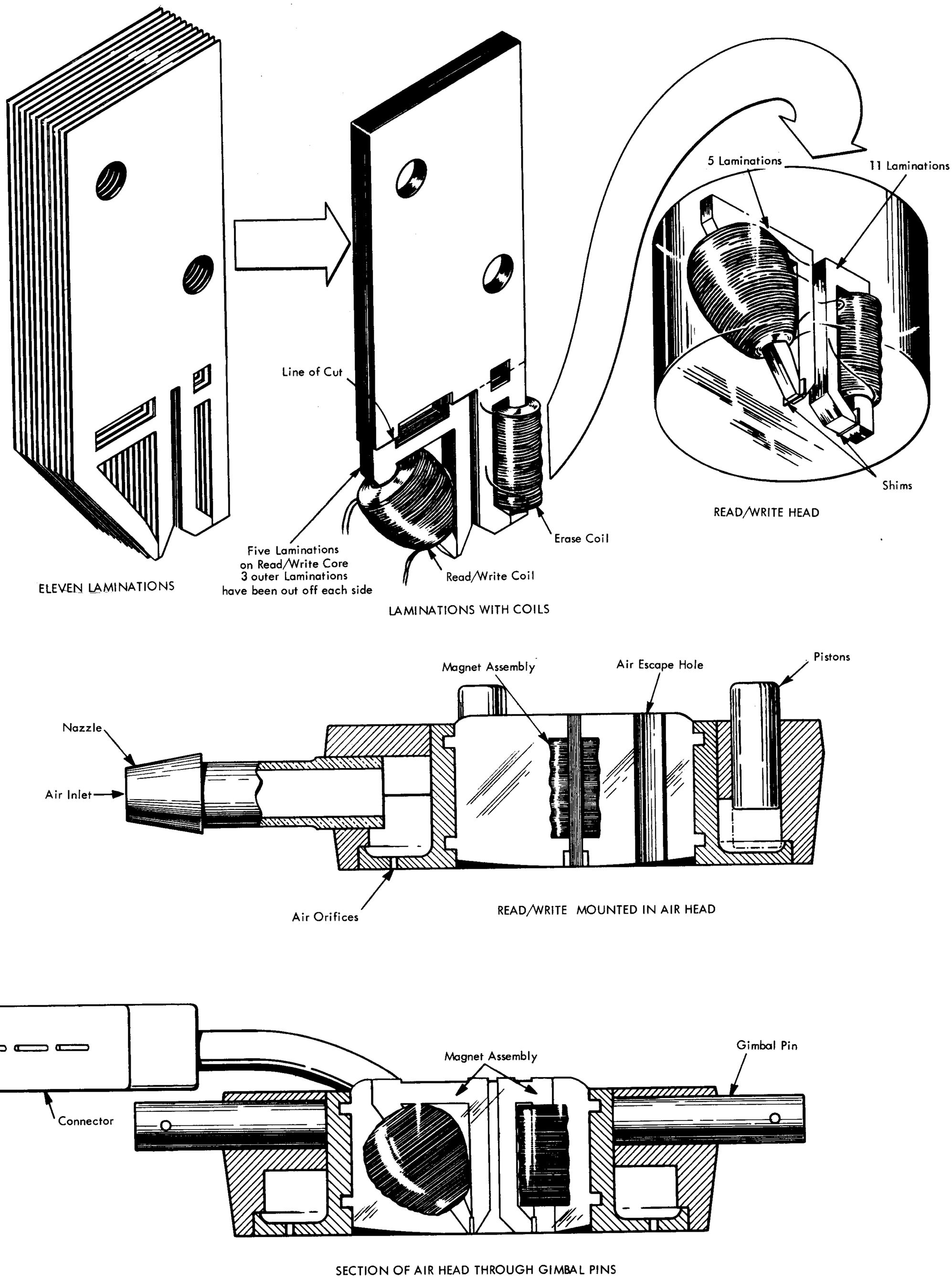



Figure 2-9. Read/Write Head and Air Head

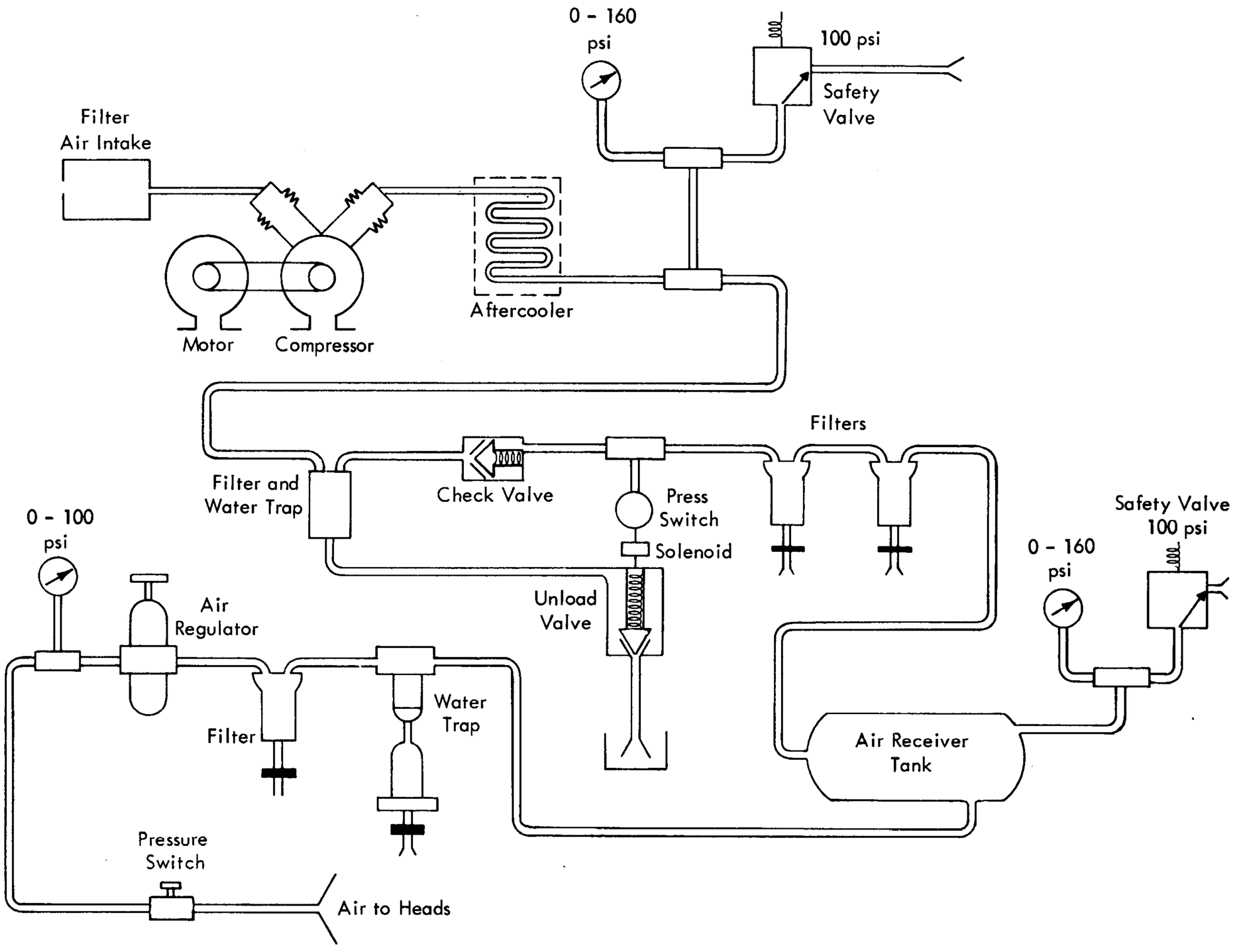



Figure 2-10. Air System Schematic

the tank for manual removal of any water that might collect. The receiver tank also contains a pressure gauge and a safety valve set at 100 psi. Air flows out of the tank to a water trap, filter, air regulator, and through a pressure switch to the read-write heads. The regulator is adjusted to supply a constant pressure of 55 psi. If the pressure falls below 45 psi, the pressure switch opens to prevent disk storage operation.

# Section 3 Basic Servo Circuits

In order to understand the circuits involved in a complete servo operation, it is first necessary to understand the logic of the servo control mechanism and the following servo circuits:

1. Logic and file safety
2. Track and disk null detectors
3. Detent
4. Driver
5. Clutch amplifier

## *Logic of Servo Control*

The preceding section dealing with mechanics explained the mechanisms required to move the read-write heads from one address to another. Since the various actions involved in a servo operation are controlled electronically, some means of translating the position of the access arm and carriage into electrical signals and controlling their movement is required.

### Track Potentiometer Logic

The track potentiometer provides a means of indicating electrically the distance and direction that the access arm must be moved to reach the addressed track. This potentiometer is mounted on the carriage as shown in Figure 3-1. The wiper is geared to the access arm. As the access arm is moved from its addressed position, the wiper moves from one end of the potentiometer resistor strip toward the other.

The upper part of Figure 3-2 shows the logic of the track potentiometer operation. A 150-v floating power supply is connected across the extremes of the potentiometer. The position on the potentiometer resistor strip corresponding to the newly addressed track is grounded. Since the track potentiometer is not physically large enough to permit a separate tap for each track position, taps are provided for track positions 00, 40, 80, 120, 160, and 200. Intermediate track positions are addressed by grounding a point on a voltage divider network connected between two adjacent taps. The selection of the grounding point is accomplished by the track address relay tree (75.70.91.1). Ground potential is provided through the disk null n/o points. (The disk null relay is picked when the carriage is detented at the addressed disk.)

If the wiper receives a positive signal, as is the case in Figure 3-2, the signal passes through the home relay n/c points (home relay is down when carriage is detented) to the clutch amplifier. A positive voltage applied to the clutch amplifier causes the out-and-up clutch to be energized.

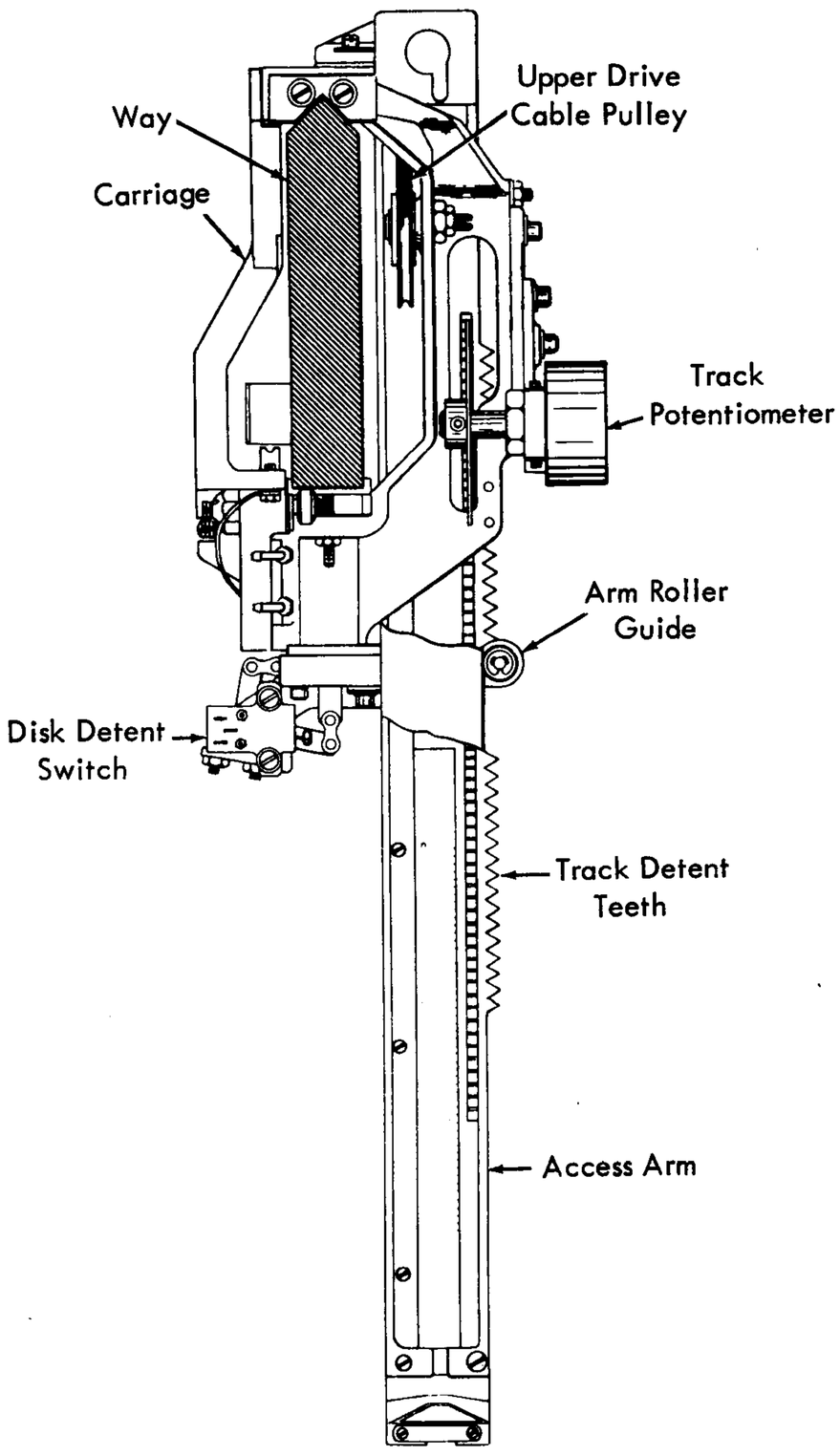



Figure 3-1. Access Arm

A negative wiper signal follows the same path to the clutch amplifier, but energizes the in-and-down clutch.

A zero wiper signal (indicating a null condition) prevents either clutch from being energized, but causes an output from the track null detector. This output energizes the track null relay which in turn energizes the track detent air solenoid.

### Disk Potentiometer Logic

The disk potentiometer provides a means of indicating electrically the direction and distance the carriage must be moved to reach the addressed track. It operates on the same principle as the track potentiometer, how-

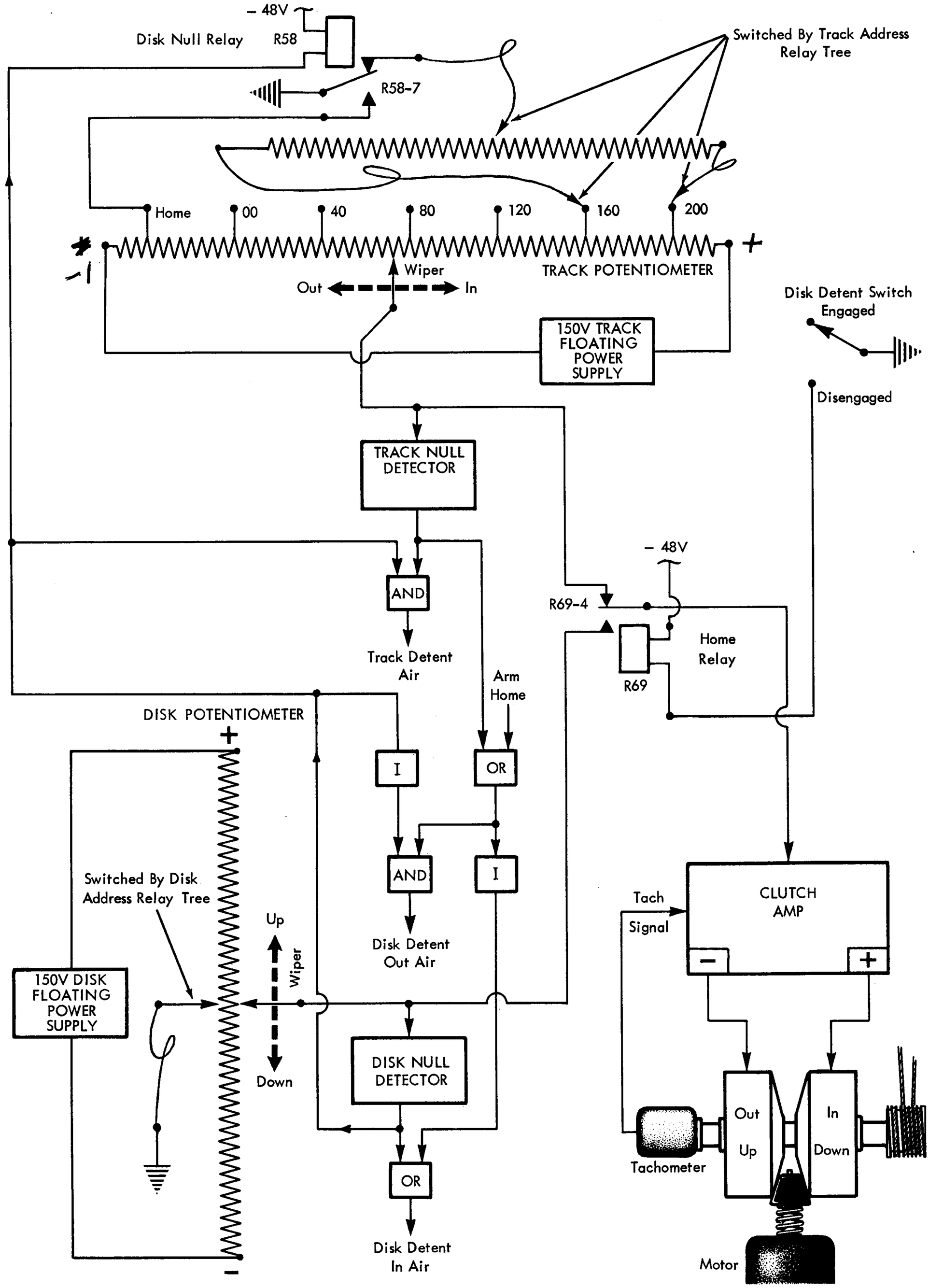



Figure 3-2. Logic of Access Servo System

ever, the disk potentiometer resistor strip is actually mounted on the side of the way. The spacing of the disks is sufficient to allow a separate tap on the disk potentiometer strip for each disk position. The disk potentiometer wiper is mounted on the carriage.

The output at the disk potentiometer wiper is fed to the disk null detector and a n/o point of the home relay. If the home relay is up (disk detent not engaged), the signal is fed to the clutch amplifier to control the movement of the carriage.

A zero wiper signal is recognized by the disk null detector as a disk null. When a disk null is detected, the detector provides an output to pick the disk null relay. The disk null relay controls the disk detent air by energizing the IN or the OUT air solenoids.

### Disk Detent Switch

When the disk detent is disengaged, the disk detent switch is transferred to pick the home relay (75.71.51.1). Therefore, when the home relay is picked, the carriage is free to move. The control over the clutches is then given to the disk potentiometer through a n/o point of the home relay (Figure 3-2).

### Tachometer Logic

The tachometer provides a means for controlling the speed of movement and deceleration of the arm or carriage during a servo operation. It is essentially a DC generator mounted on the clutch shaft (Figure 2-5).

As the clutch shaft gathers speed, the tachometer supplies a potential that builds up to an approximate maximum of 25 v. The tachometer signal is the same in polarity as the error signal and is referenced to the error signal (Figure 3-3). The voltage at the summing junction is the algebraic difference between the error signal and the tachometer signal.

As the carriage or arm approaches the addressed position, both signals approach ground. When the difference between the two signals reaches the crossover point, the opposite clutch is energized to provide dynamic braking. With the components properly adjusted, the carriage or arm will decelerate to a smooth stop without oscillation or overshoot (Figure 3-4).

## Logic and File Safety

### Logic Safety

The logic safety relay (R72 access 0) can be picked only by meeting the requirements of the interlock chain in series with the coil (75.71.51.2). If the interlocking conditions are fulfilled, the relay is picked when the file reset condition is developed on 75.38.11.1.

When the logic safety relay is picked, the following significant conditions exist:

1. The carriage is not at the extreme upper or lower limit of travel on the way. (The disk drive overtravel switches are closed.)
2. A number of critical relays are in the machine. (A normally-open and normally-closed point of each of these relays are paralleled, so that any one may be energized or de-energized and still complete the interlock.)
3. The 130°F thermal switch to the heater box is closed.

The logic safety relay can also be picked by the access inop switch located on the CE test panel. It provides a pick to the logic safety relay through the overtravel stop switches for test purposes.

### File Safe

This circuit (75.70.31.1) is available if the compressor is supplying at least 45 psi of air (minimum for proper head and detent operation) and the thermal switches in the heater box (temperature control for null and clutch amplifier circuits) are in their proper relationship (both closed between 100° and 130°F).

## Null Detectors

The disk and track null detectors are identical. The disk null detector receives the disk error signal from the disk wiper when the home relay is picked. The track null detector receives the track error signal when the home relay is down (Figure 3-3).

### Disk Null Detector

Servo logic requires that the disk null relay (R58 for access 0, 75.70.31.1) be energized only when the carriage is located at the disk to which it is addressed. The disk null relay is picked through a relay driver (Figure 3-3) when the disk wiper signal is within 0.4 v of ground (75.62.61.1 and 75.70.31.1).

The disk null detector is used to sense the absence of an error signal. Essentially, it is a high-input impedance DC amplifier.

Refer to the component circuit section in the ALDs for card type YES. The 5K level potentiometer is adjusted so that an error signal of ±0.4 v or less causes the disk null detector to drive the detent relay driver (APX) in such a manner that the disk null relay is picked (Figure 3-3). An error signal of ±0.5 v or greater causes the null detector to drive the detent driver in such a manner that the disk null relay is dropped.

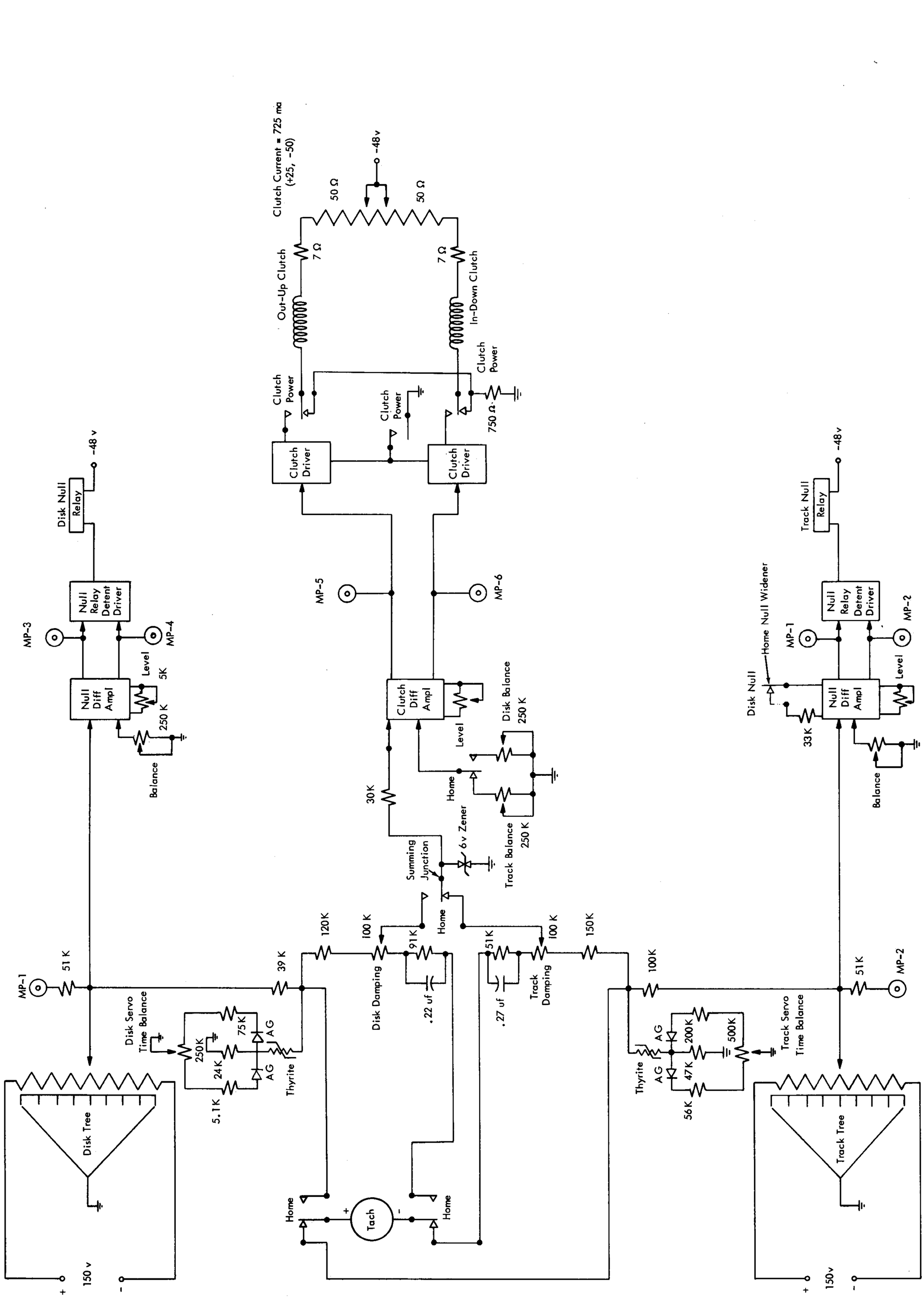



Figure 3-3. Servo Control Schematic

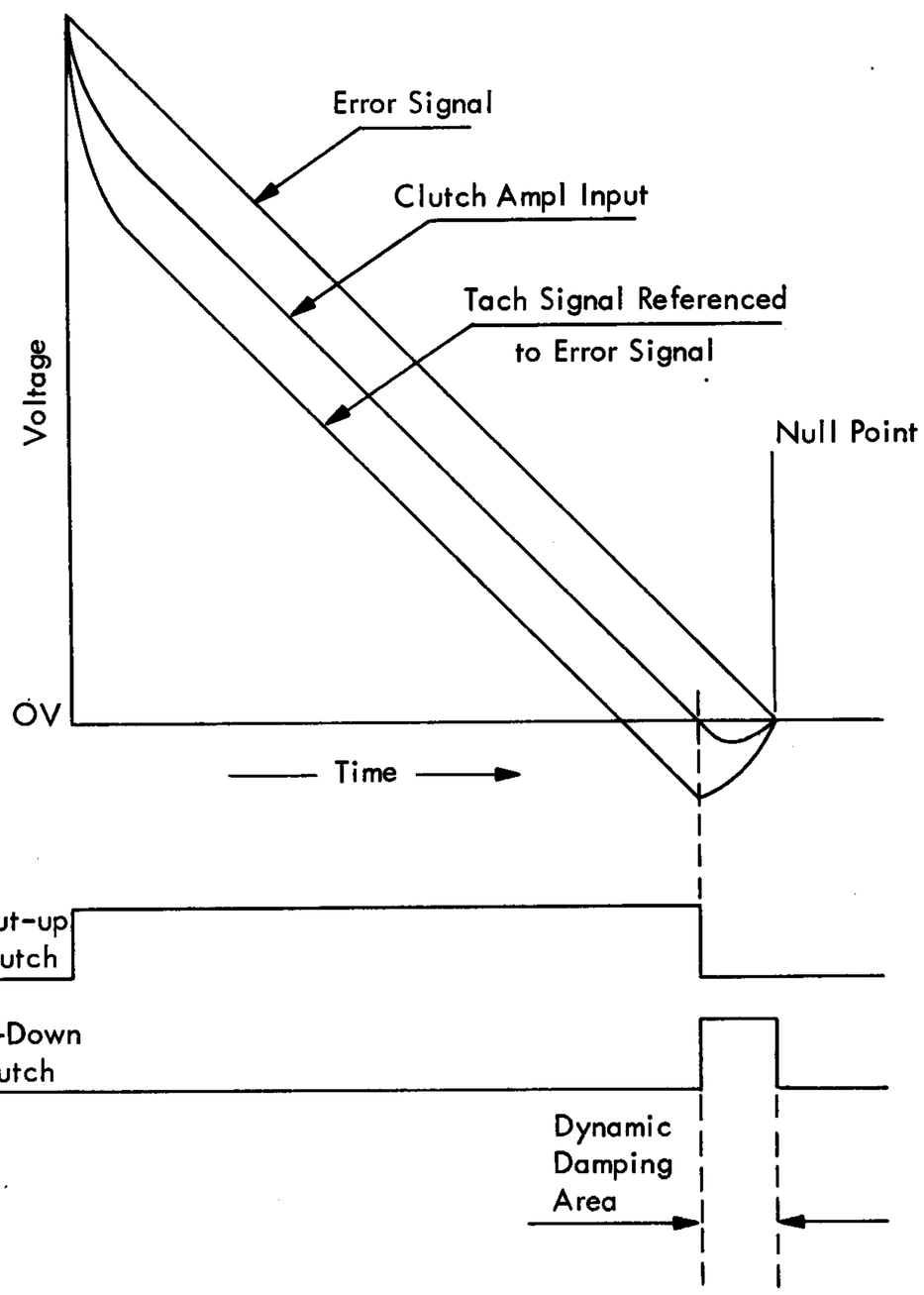



Figure 3-4. Idealized Servo Control

### Track Null Detector

Servo logic requires that the track null relay (R55 for access 0, 75.71.31.1) be energized only when the access arm is positioned at the track to which it is addressed or at the home position when there is no disk null. R55 is picked in a manner identical to the pick of R58 by the disk null detector. The operation of the track null detector when the arm is at the home position is covered later.

### *Detent Driver*

Refer to the component circuit diagrams in the ALDs for card type APX. The detent driver is a relay driving circuit capable of driving a –48-v relay that requires a maximum of 147 ma. The base of transistor T6 is referenced at approximately –1 v. A voltage applied to the base of T7 that is less than –1 v (approx.) causes T6 to conduct. T4 is then forward biased and the relay is picked. When the voltage on the base of T7 is greater than –1 v, T7 conducts to cause T6 and T4 to cut off and the relay to drop.

### *Clutch Amplifier*

Refer to card type YET in the component circuit section of the ALDs for the following description.

The clutch amplifier is designed to drive the servo clutch driver (card type AMK) which in turn energizes the clutch when the amplifier receives an error signal.

The amplifier is a direct coupled differential amplifier that amplifies the algebraic difference between the error signal and the tachometer signal (Figure 3-3). A negative input signal causes point C (Component Circuit Diagram) to go more negative which causes the clutch driver to energize the in-down clutch. A positive input signal causes point E to go more negative which causes the alternate clutch driver to energize the out-up clutch.

Power supply drift at the output is effectively cancelled by the orientation of the application points of the +30-v and –12-v supplies.

The amplifier requires an initial potentiometer adjustment to set the output levels. With the input grounded, the balance and level potentiometers are adjusted until points C and E are at a nominal no signal voltage of –1 v.

The Zener diodes at the input of the clutch amplifier clamp the amplifier inputs to the following limits:

Max = +6 (+0.30 –0.27)
Min = –6 (+0.27 –0.30)

As previously mentioned, the clutch amplifier drives one of two clutch drivers (type AMK). The driver is a linear amplifier capable of delivering an output current of approximately 700 ma. When one clutch driver is activated the other one is cut off.

# Section 4 Seek Operation (1405-1401)

In order to facilitate the explanation of the circuits involved in a seek operation, assume that a disk-to-disk servo, using access 0 in module (file) 0, from address 00195 (disk 00 track 19 record 5) to 94362, is called for by the instruction M%F0BBB.

## Objectives

1. Select the 1405 for a seek operation.
2. Place new address in file address register.
3. Start mechanical servo operation.
4. Retract R/W heads.
5. Disengage track detent.
6. Move arm out.
7. Disengage disk detent and lock arm out.
8. Move carriage up.
9. Engage the disk detent and release arm.
10. Move arm in.
11. Engage track detent.
12. Extend Read/Write heads.
13. Notify CPU that servo is complete with *access ready* signal.

### Select the 1405 for a Seek Operation

When the CPU encounters the instruction M%F0BBB, the % latch and the file op latch are set (75.01.04.2). The file op latch signals the 1405 that a disk storage operation is to be performed. The type of file operation to be performed is determined by the decode of the character following the F in the instruction (in this case 0 (zero)). When the 0 is decoded, the seek latch is set if the write check interlock latch is off (75.02.21.2). Not write check interlock gates the *file op* line to develop *gated file op* (75.01.42.2). The operation of the write check interlock latch is covered later. The write check interlock latch prevents any file operation except a write check following a write operation.

### Place New Address in File Address Register

Following the CPU instruction cycles, the CPU reads out the new address (parallel by bit and serially by character) to the 1405 character register (75.36.01.1). Each character of the address enters the character register under the control of *address strobe* (Figure 4-1).

*Address strobe* is generated on every process cycle during the time the address transfer latch is on. The address transfer latch is turned on at the beginning of the first process cycle following the instruction cycles (75.04.21.2).

The first character to enter the 1405 character register is the access digit. It is immediately strobed out of the character register to the select register by *address strobe delay* (the same strobe that allowed it to enter the register but delayed by 1.2 μsec) ANDed with digit 0 or digit 1 (75.23.01.1). The second character (module digit) is handled in the same way.

The 1405 digit ring is used to identify the address characters. It is reset with the digit 0 trigger on (75.21.11.1). It is advanced at the beginning of each process cycle during address transfer time except the first. The advancement during the first process cycle is prevented by the first address transfer latch. Thus, the first character transferred is identified as digit 0 (the access character). The second character transferred is identified as digit 1 (the module character), etc.

By the end of digit 1 time, during address transfer time, the access and module characters (00) are stored in the select register (Figure 4-1). *Access 0 select* and *mod 0 select* are then available from 75.23.01.1.

At digit 2 time, the disk tens character (9) is strobed out of the 1405 character register by *delayed address strobe* (75.24.01.1). The resultant bit-1 and bit-8 lines are then powered up and driven to 75.60.61.1 where they are ANDed with *access 0 seek select* (combination of access 0 select, mod 0 select and seek status 75.25.01.1), and digit 2 at the latching type drivers, 3A and 3D.

Each subsequent character of the address is handled in the same way at digit 3, 4, and 5 times, respectively. The record character (2) is not stored at this time. It is stored during the following read or write operation. Therefore, at the end of digit 5 time, during the address transfer portion of the operation, the disk and track address characters have been stored in the latching relay drivers (75.60.61.1).

As each relay driver is activated, a pick line is established to a corresponding address relay (75.70.01.1). The hold is maintained over the address relays from the previous seek instruction until the new pick lines are established. Thus, if the same address relay is used on a successive seek operation, it does not drop when the hold line is opened. The hold line is opened approximately 15 ms following the development of *servo start*.

### Start Mechanical Servo Operation

The initiation of the servo operation is controlled by the three start relays on 75.70.31.1. Start 1 is picked when *servo start* is developed by *address strobe* at digit

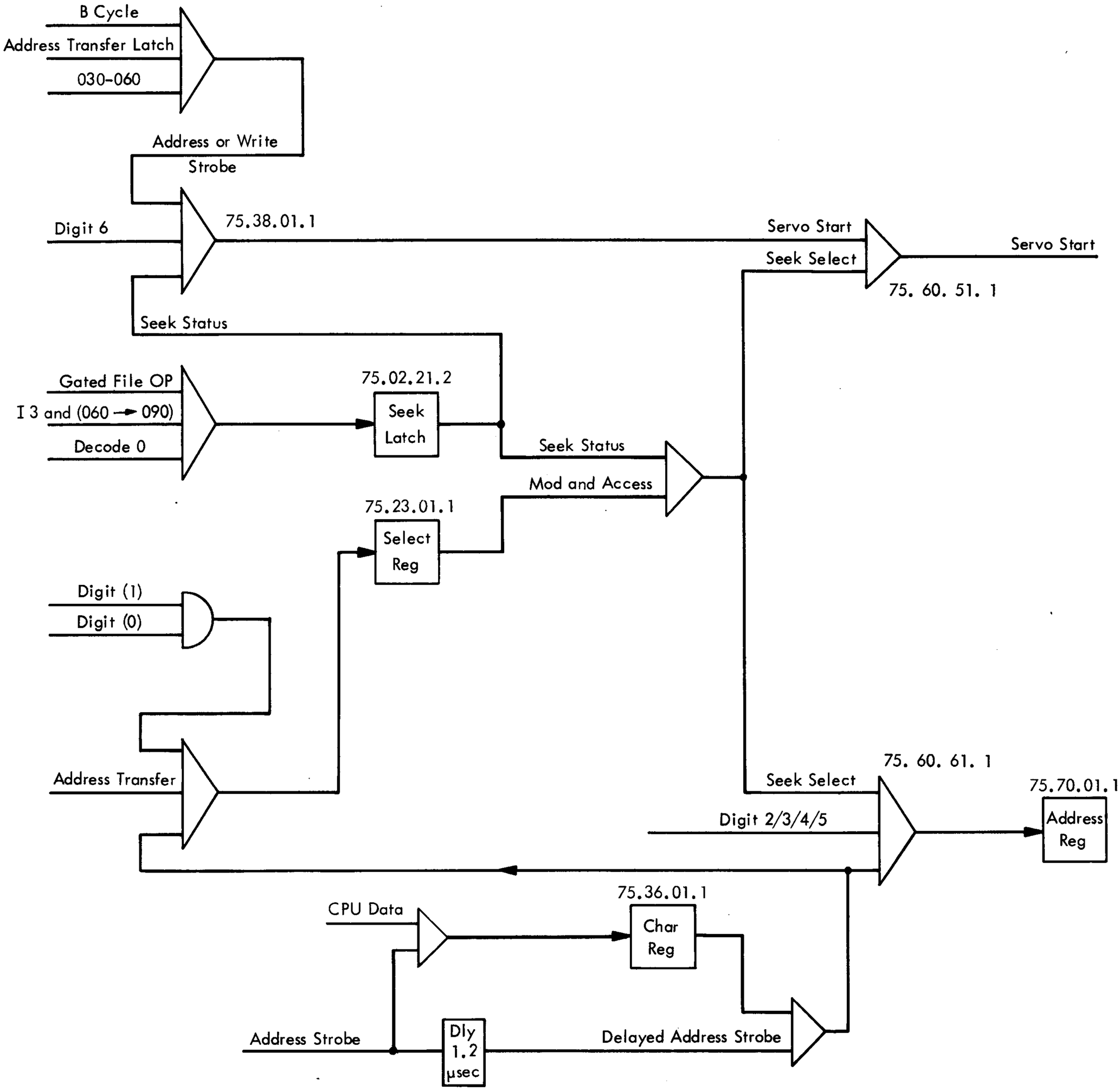



Figure 4-1. Development of Servo Start and Loading of Address Register

6 time (75.38.01.1) during the address transfer portion of the seek operation (Figure 4-1). *Servo start access 0* is then available from the latching driver at 6C (75.60.51.1).

### Retract R/W Heads

As seen in Figures 4-2 and 4-3, the R/W head solenoid (75.71.81.1) controls the air supplied to the heads. The solenoid is de-energized as soon as the head relay (R70) is dropped. Note, it is only necessary to drop the head relay if the disk address has been changed (disk-to-disk servo). The head relay dropped when start 1 picked to drop the disk null relay R58 (75.70.31.1). When air is removed from the heads, the return springs acting on the head gimbal pins, restore the heads to their recessed position.

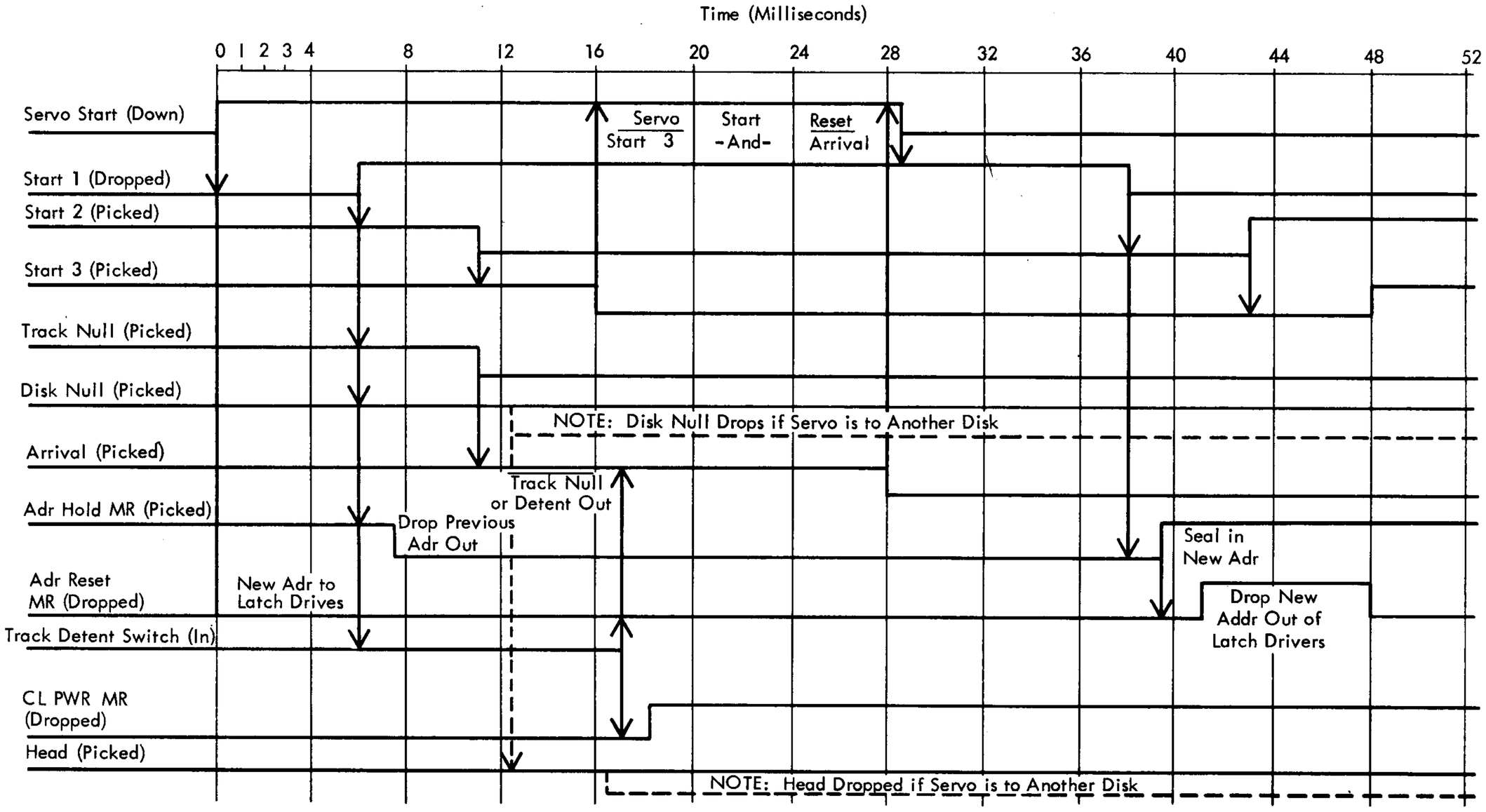



Figure 4-2. Relay Timing from Servo Start to Repick of Start 3

### Move Arm Out

To accomplish this objective, the carriage must be detented, the track detent must be released, and the out-up clutch must be energized (Figures 4-3 and 4-4).

The track detent solenoid was de-energized when start 1 picked (75.71.81.1). The disk detent in solenoid remains energized through the n/c points of the track null and home relay (75.71.81.1).

The out-up clutch (75.72.11.1) is energized by applying a positive track error signal to the clutch amplifier on 75.62.61.1 and by energizing the clutch power mercury relay (5C-75.61.51.1). *Clutch power 1, clutch power 2,* and *access 0 safe* are required to energize the clutch power relay. *Clutch power 1* is available when the track detent switch is transferred to the out position (75.71.51.1). *Clutch power 2* is available when the disk null relay drops (75.71.51.1). The latter circuit provides for a delayed energization of the clutch power relay if the R/W heads were previously located at one of the outer 40 tracks. This delay allows the R/W heads to be fully recessed by the time they reach the periphery of the disk. The positive track signal from the track potentiometer is supplied by grounding the home position through a n/c point of the disk null relay. The de-energized disk null relay indicates that the arm must be completely retracted; the n/c null relay points ground a position on the track potentiometer minus end, beyond track address 00 (75.70.91.1).

### Disengage Disk Detent and Lock Arm Out

When the arm is full retracted (Figures 4-3 and 4-4) a track null is developed and the track null relay (R55) is energized. The R55-2 n/o points (75.71.81.1) close to energize the disk detent out solenoid. At the same time the R55-3 n/o points open to de-energize the disk detent in solenoid. When the disk detent is disengaged, the fail-safe is engaged and the home relay (R69) is picked (75.71.51.1).

During a disk-to-disk servo, when the transfer from track drive-to-disk drive takes place, a considerable amount of time (with respect to ms) is required to transfer the disk detent and the fail-safe mechanism. In order to save some of this time, the home null region is widened to enable the track null relay to pick early. This widening effect is created when the disk null relay is down, by placing a 33K resistor in parallel with the clutch level potentiometer (Figure 3-3).

### Move Carriage Up

When the fail-safe mechanism is engaged, the arm is locked in the home position. Under this condition,

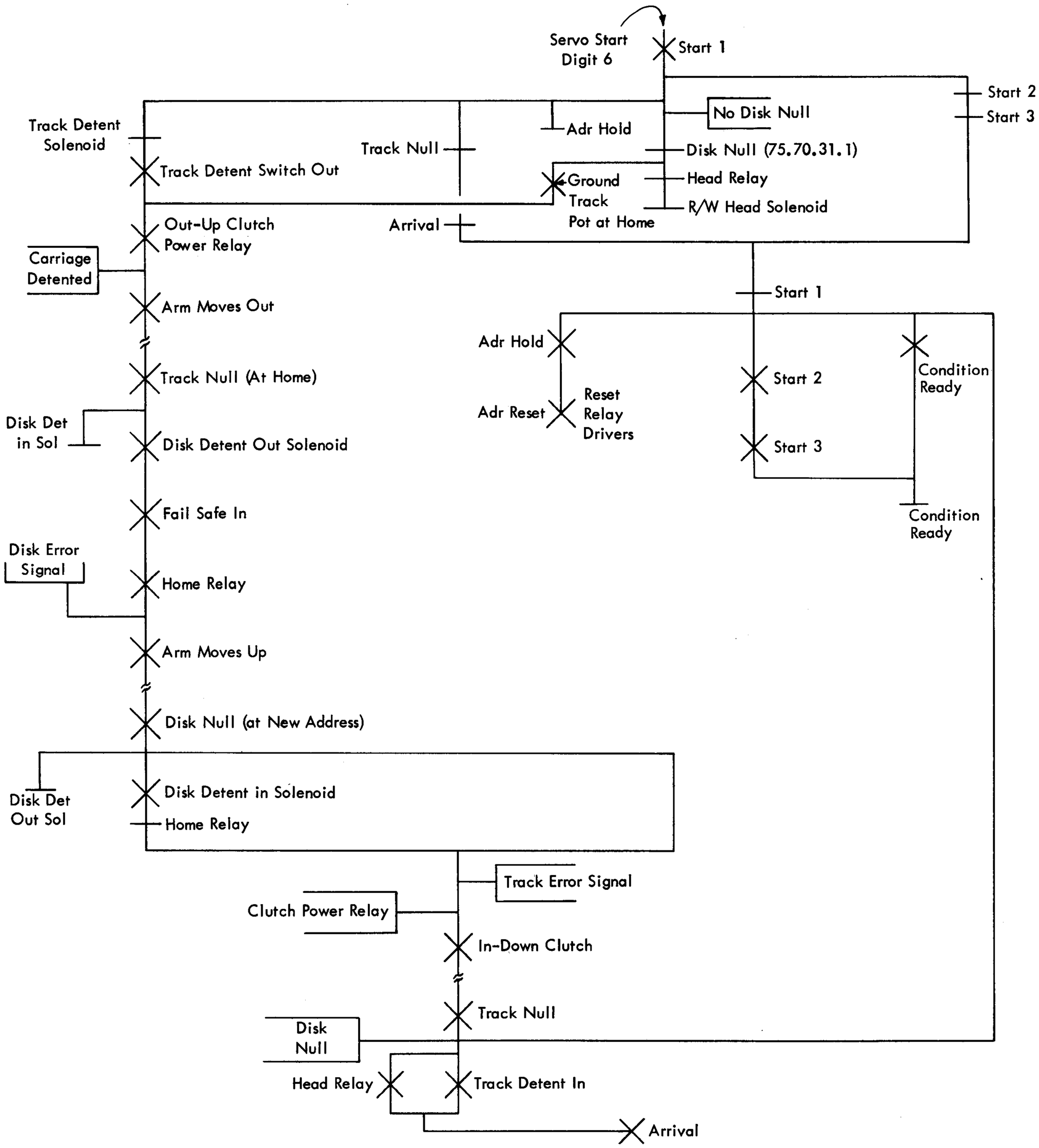



Figure 4-3. Disk-to-Disk Servo

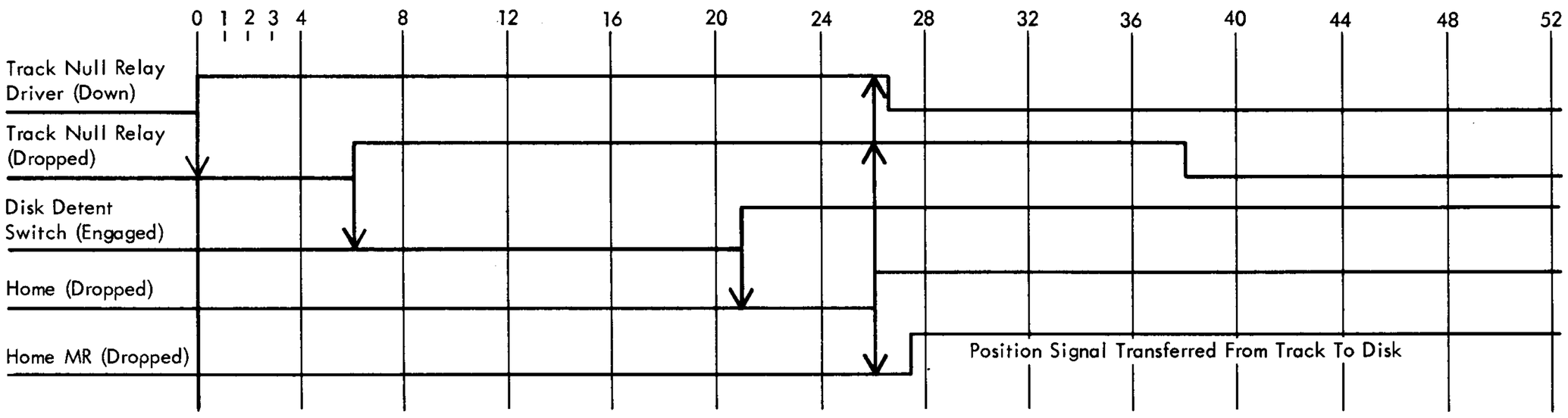



Figure 4-4. Relay Timing from Track Null to Pick of Home Relay

if the out-up clutch is energized, the carriage moves up. A positive disk error signal is applied to the clutch amplifier (Figure 3-3) through the transferred home relay points (75.62.01.1). In this example, the carriage is located at disk 00 while the disk potentiometer is grounded at location 94 through the address relay points on 75.71.61.1.

### Engage Disk Detent

When the disk null is detected (Figures 4-3 and 4-5), the disk detent in solenoid is energized through the n/o disk relay points (R58-5). At the same time the disk detent out solenoid is de-energized when the R58-3 n/c points open (75.71.81.1). When the disk detent is engaged, the fail-safe is disengaged and the home relay is dropped (75.71.51.1).

### Move Arm In

Energizing the in-down clutch, with the disk detent engaged, causes the arm to move in until a track null is detected. A negative track error signal is supplied to the clutch amplifier when the home relay is dropped (Figure 3-3). In this example, the track potentiometer is grounded at track position 36 by the points of the track address relays (75.71.91.1). The address relays place 40 units of resistance in parallel with the track potentiometer between positions 00 and 40. The ground is then established to provide 4 units of resistance down from track 40 or 36 units of resistance up from track 00, thereby, establishing the track null point at track 36.

### Engage Track Detent

When the track error signal reaches zero as shown in Figure 4-6, the track null relay (R55) is picked (75.70.31.1). With the disk and track null relays energized and the start 1 relay de-energized, one of the four track solenoids on 75.71.81.1 is energized. The selection of the correct solenoid is determined by the track address relays as shown in the chart on 75.71.81.1. In this example, track solenoid 0 is selected because the tens digit (3) of the track address is odd and the units digit of the address is 6.

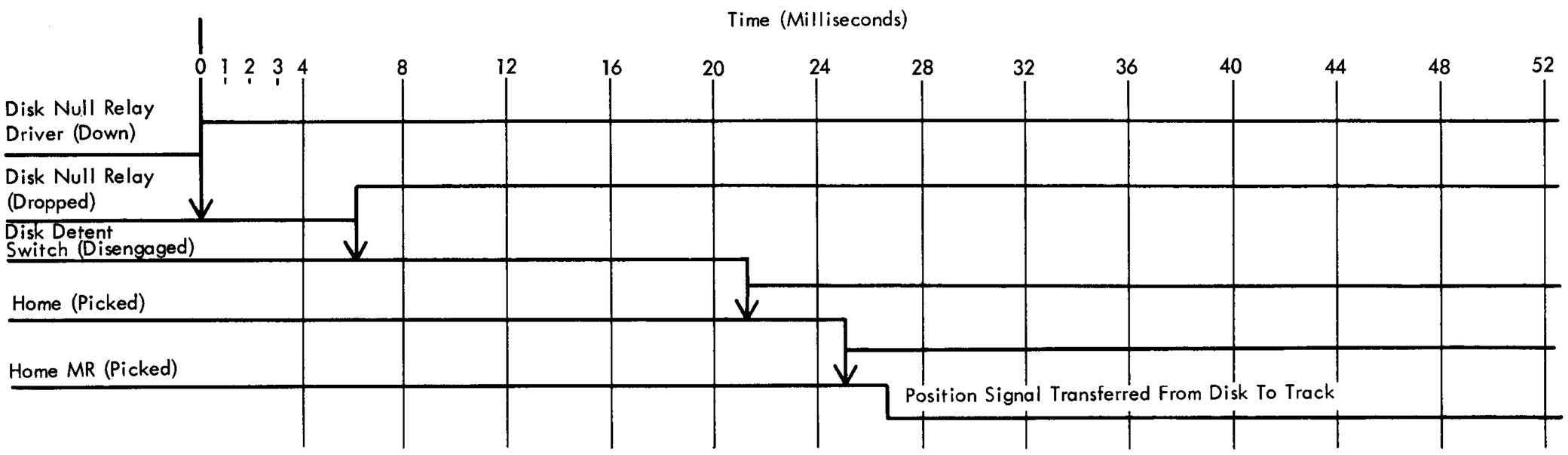



Figure 4-5. Relay Timing from Disk Null to Drop of Home Relay

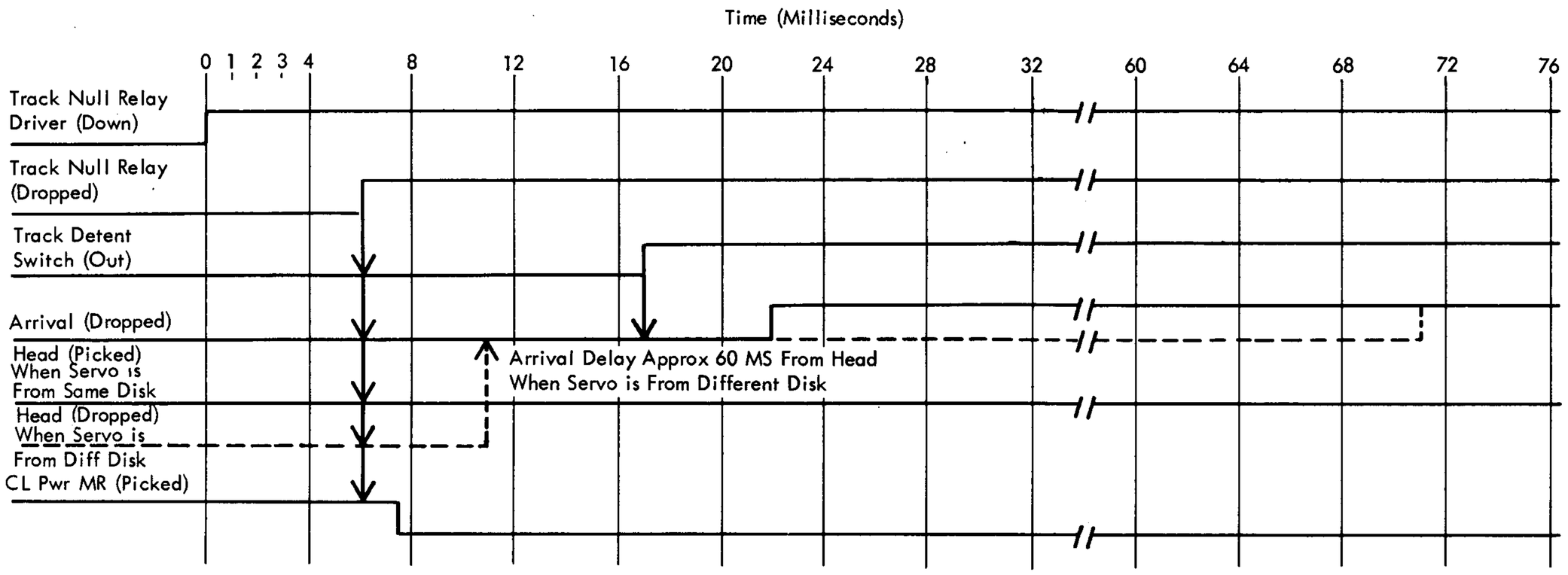



Figure 4-6. Relay Timing from Track Null to Pick of Arrival Relay

### Extend R/W Heads

The head relay (R70) is picked through the track null relay points (75.71.81.1). The R/W head solenoid is then energized through the n/o points of the head relay (75.71.81.1).

### Access Ready

This signal is developed to inform the CPU that the mechanical servo is complete. It results from the pick of the arrival relay (R62-75.70.30.1). The arrival relay is picked when the track detent switch transfers if a track null exists and the head relay is up (75.71.51.1). However, *access 0 ready* from 75.70.31.1 must find the condition-ready latch off before it is allowed to signal the CPU of the ready status (3A-75.61.81.1).

The condition-ready latch ascertains that the mechanical servo was initiated. The latch is turned on at digit 3 time of a seek operation and is turned off when both start 1 and start 3 are down (Figure 4-2). Start 1 and start 3 are both down for a short time after the initiation of the mechanical servo.

## *Customer Engineering Track Selection*

One of the two CE tracks (inner or outer) on an addressed disk is selected when the CE test lock switch is ON and a seek operation is called for. If the track units address is odd, the inner track is selected. If the track units address is even the outer track is selected.

The test relay (R30 for access 0) is energized on 75.70.31.1 from 75.39.01.1 when the test lock is ON. With the test relay up, the track pot is grounded one track out from 00 if the track units address is even, or one track in from track 200 if the track units address is odd (75.70.91.1).

Track solenoid 0 is selected through points of the test relay if the inner CE track is selected. Track solenoid 3 is selected if the outer CE track is selected (75.71.81.1).

The 1405 disk storage unit uses the NRZI (nonreturn to zero IBM) method of magnetic recording on the disk surface. This system recognizes a change in flux pattern to indicate a bit while no change represents a NO bit. Thus, each transition of magnetization from plus-to-minus or minus-to-plus polarity represents the storage of a bit. A binary coupled trigger (NRZI trigger) is flipped with each data bit. Thus, the direction of the recording current is reversed with each data bit (Figure 5-1). The corresponding read-back signal is voltage induced in the head winding as the changes in magnetic polarity in the disk surface cross the gap of the read-write head. Read back signals will range from 18 mv to 25 mv on the inside tracks to 35 mv to 50 mv on the outside tracks.

The physical configuration of the read-write head is shown in Figure 2-9. The head was designed to provide a recording bit rate of 186 kilobits per second. It is a 3-terminal device containing a read-write coil and an erase coil. The coils are connected to one another as shown on system diagram page 75.72.11.1. When reading or writing, the heads are positioned approximately .001″ from the surface of the disk.

## Disk Clock

The disk array revolves at a speed of 1200 rpm. At this speed, it takes approximately 50 ms to complete one revolution. Therefore, it takes about 10 ms for one of the 5 disk sectors to pass the read-write head. Within this length of time, the 1405 can read or write 200 data characters plus 8-indelible-address characters, the pre-indelible address AGC bits, and the pre-record AGC bits (Figure 5-2). To enable the 1405 to accomplish this, the recording bit rate must be equal to 5 $\mu$s per bit.

The disk clock is provided to control this bit rate and to identify each character and bit (or NO bit). If the read-write heads were permanently located at a fixed station, it would be possible to generate the clock by a clock track written on the disks. However, this is not feasible because of the inability to predict the exact position of the read-write head from one seek operation to the next. For this reason, a pair of external oscillators are used to generate a self-clocking system. Only one of these oscillators is used during a write operation. During a read operation, each read-data bit shifts the clock control from one oscillator to the other.

The basic 5 $\mu$s-bit pulse is divided into four working phases. Figure 5-3 contains a block diagram that describes the disk clock data flow and a timing chart showing the phase relationships.

### Disk Clock Circuit

The oscillators at 5A and 5C are controlled by the trigger at 3B (75.31.01.1). During a write operation the *+U not write gate* is down and the trigger is held OFF. The oscillator at 5A is then allowed to run. The oscillator at 5C is held OFF.

During a read operation the *+U not write gate* is up and the clock control trigger flips with each read data bit. If only one oscillator were used during a read operation, it might drift out of synchronism with the bits

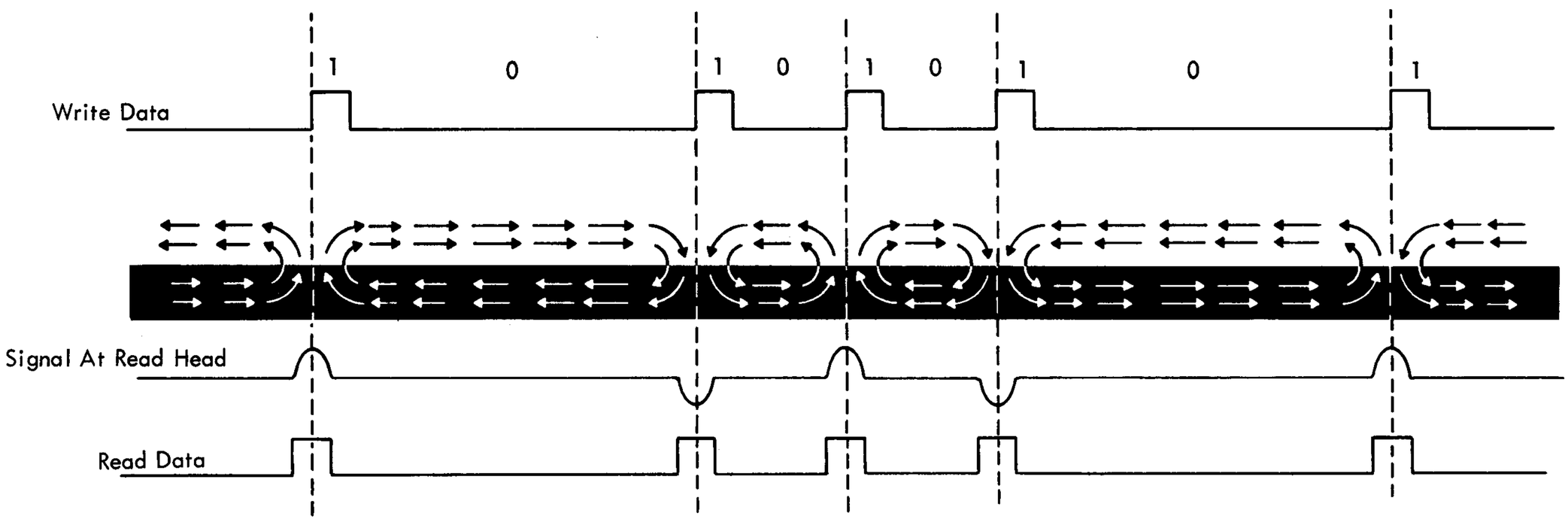



Figure 5-1. NRZI Recording

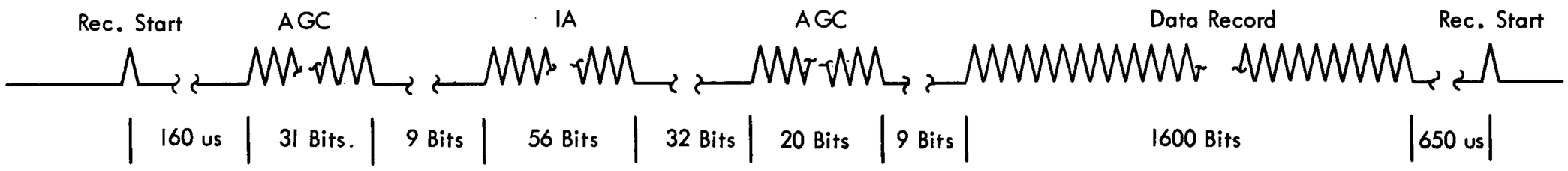



Figure 5-2. Record Layout

being read. By using two oscillators and alternating them with each data bit read, the chance of them drifting out of synchronism with the recorded bits is lessened. However, it is possible that a large gap could exit between characters on a track within one sector. This fact is taken care of by recording S bits for each character position; the S bit has no significance in the bit structure of any character. In this manner the oscillators are forced to alternate at least after every sixth bit time (seventh bit time in load Op).

The 2.5 $\mu$s phase-A pulse is developed as pin A at 6B goes PLUS. Phase B comes up 1 $\mu$s later by ANDing the output of the delay unit with phase A at 4H. When pin A of 6B goes MINUS (was PLUS for 2.5 $\mu$s), phase A and B fall. Delayed phase A remains available until the delay unit times out 1 $\mu$s later (Figure 5-3).

Phase C comes up as pin B at 6B goes PLUS. Phase C is then ANDed with the 1 $\mu$s delay from 2F to bring up phase D. The output from 2F also brings up the 1.5 $\mu$s phase-C delay pulse.

## *Write Driver Circuits*

The write driver circuits include the NRZI trigger, gate-buffer, voltage divider and write drivers (Figure 5-4). These units are required to develop and supply 85 ma to 120 ma of write current steadily through the erase winding and alternately to each half of the read-write winding. Idealized write circuit waveforms are shown in Figure 5-5.

### NRZI Trigger

The NRZI trigger is a high speed CTDL trigger with a binary connected input (4D-75.61.61.1). It accepts write-data pulses at a —T level. Each time the input signal goes to a —T level (representing a bit), the trigger flips. The output of the trigger, when gated with the write gate, functions through the gate-buffer (at 5C) to turn on one current driver and turn off the other.

### Gate-Buffer

The purpose of the gate-buffer (5C-75.61.61.1) is three fold; it provides an AND function for write data and the write gate, it isolates the current drivers from the NRZI trigger, and it converts the incoming signal level to that required by the current drivers.

Refer to card type AMJ in the component circuits section of the ALDs. The two outputs of the NRZI trigger drive the bases of T2 and T4. When T2 is ON, T4 is OFF.

When the input to T2 is —6 v, T2 will conduct, its base potential will be approximately —0.2 v, and diode D27 will rapidly cut off. The collector of T2 will be at a +U level. This condition holds the base of T7 at a +U level and prevents T7 from conducting. At the same time the input to T4 is at +6 v. T4 is cut off and its collector will be approximately —12 v.

If the write gate, applied to pin F, is at a —U level and T4 is cut off, the base of T6 will be at a —U level and T6 will conduct. Pin E will rise to approximately —6 v.

### Write Driver

The write driver produces a write current of 85 ma to 120 ma. This current passes through the head matrix and one leg of the read-write coil and the erase coil to the head select driver. A duplicate current driver is used to drive the other leg of the selected head. (6C, 6D-75.61.61.1)

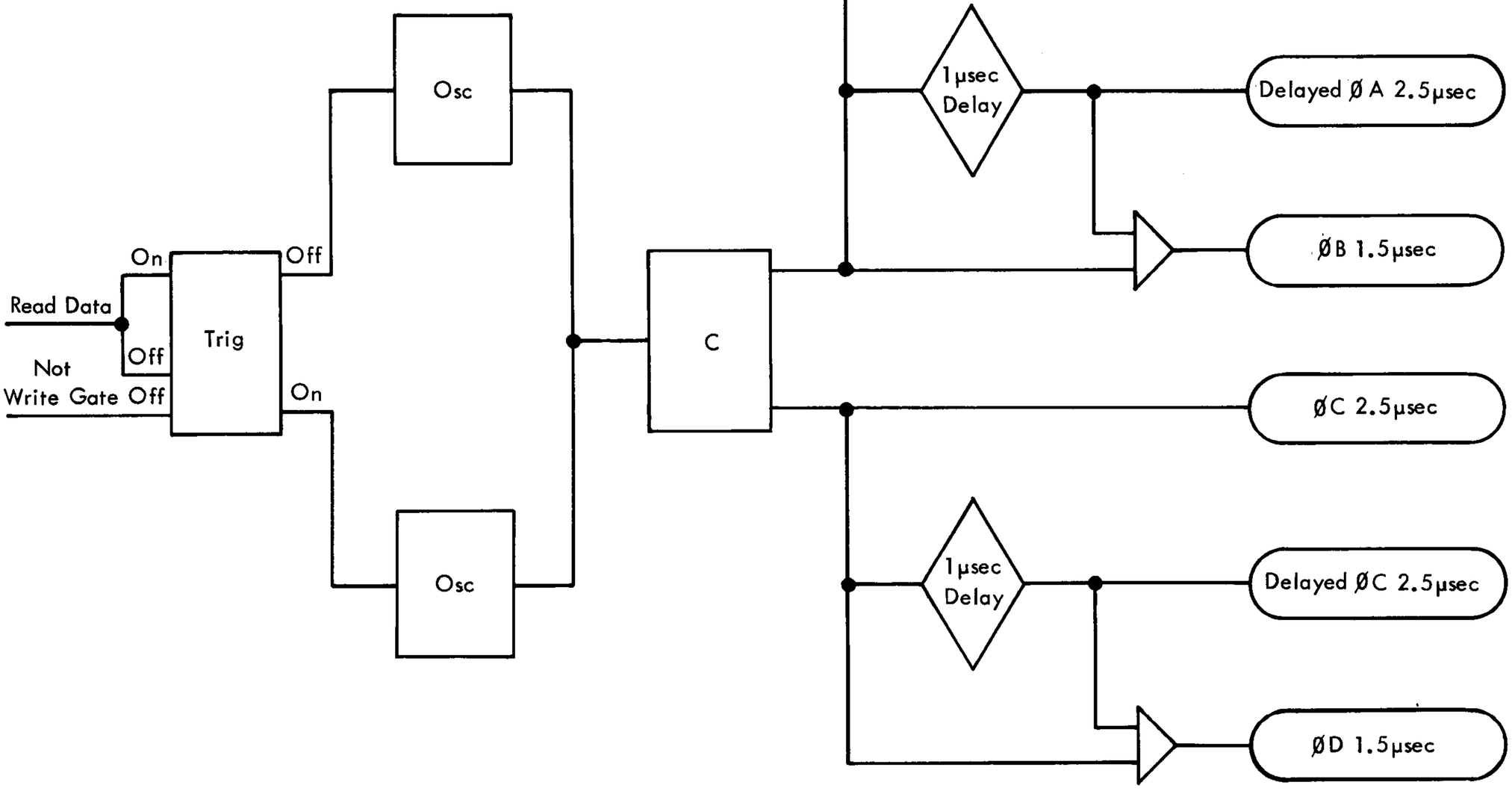
Refer to card type AMH in the component circuits section of the ALDs. In operation, pin D will be at —6 v when a data bit it to be written. T1 turns on and its collector approaches a —33 v. This forward biases T5 and it conducts to supply an emitter current return for T9. When T5 and T9 conduct, they allow 85 ma to 120 ma of write current to flow through one side of the read-write head. These two transistors are operated just into saturation to decrease the turn off time. The amplitude of the current is determined by R17 in the emitter circuit of T5.

When the current driver is turned off, T5 stops conducting. T9 is then starved off. The resulting inductive kick voltage will be clamped off at +30 v by D23, thus protecting T9.

Diode 44 protects the emitter-base junction of T9 from excessive reverse bias when the driver is off.

An additional 110-ohm, 2-watt resistor is located along the cable to the read/write heads approximately three feet away from the heads.

Data Flow




Timing

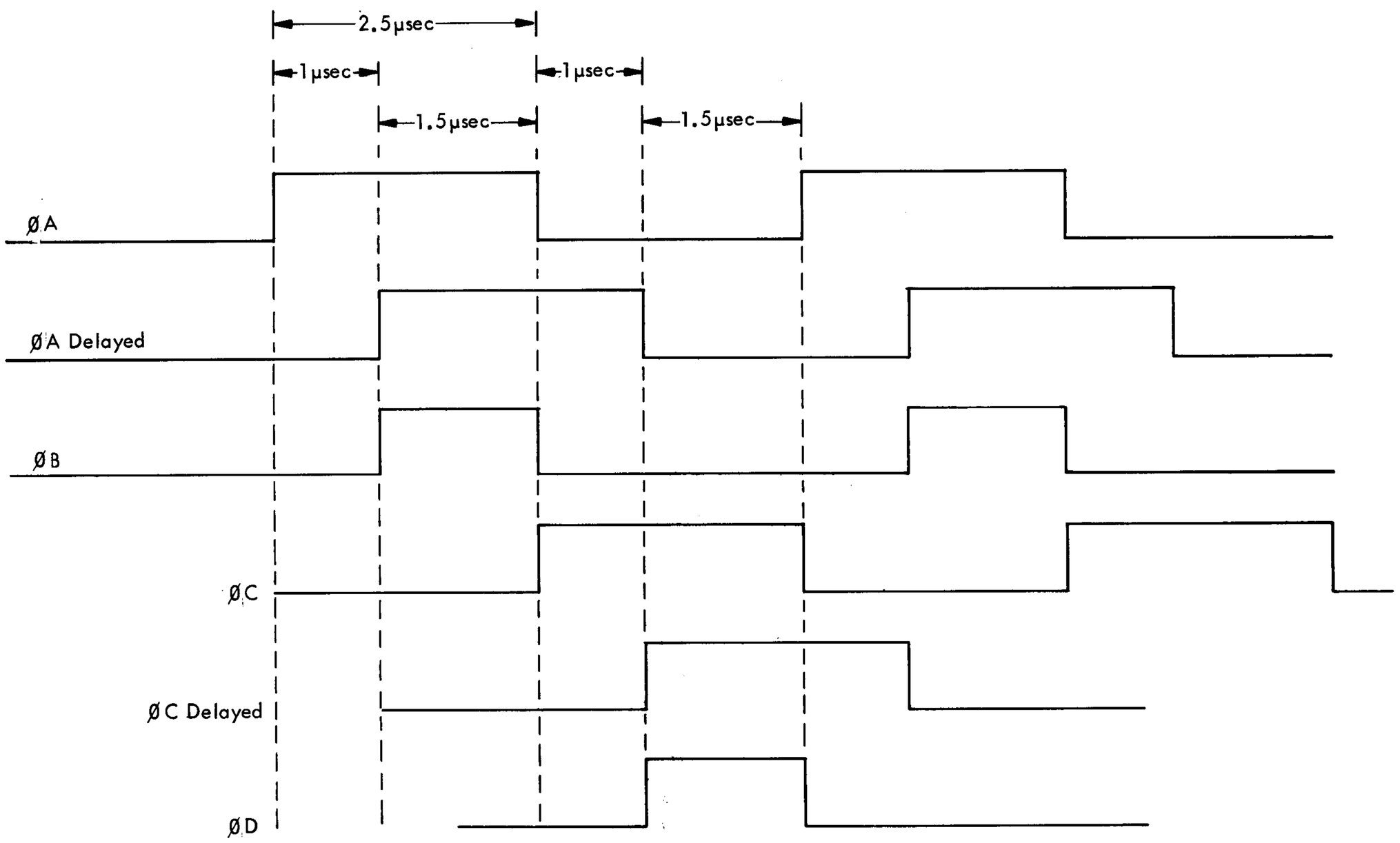



Figure 5-3. Disk Clock

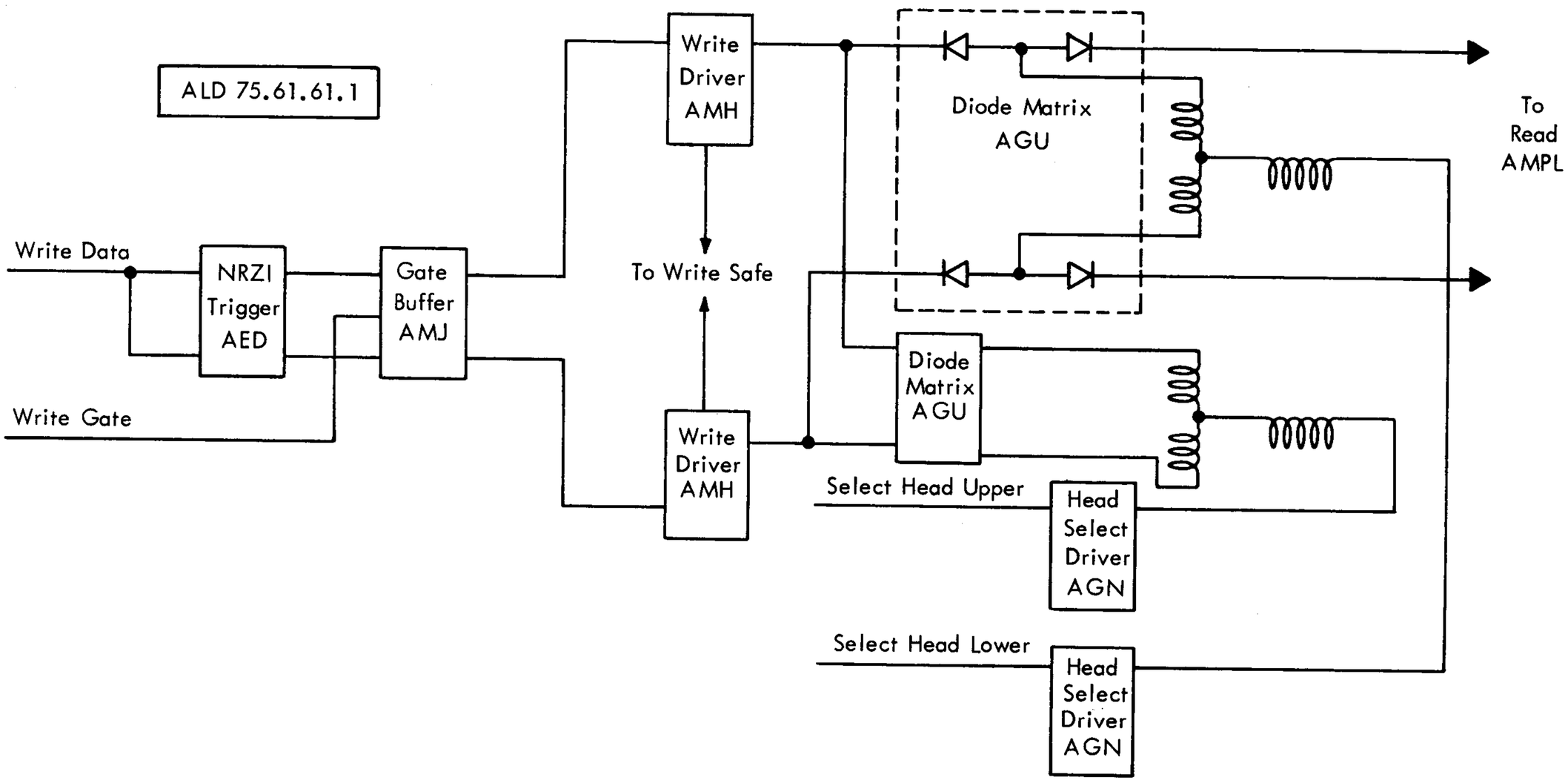



Figure 5-4. Write Circuit – Block Diagram

## *Head Selection*

The 1405 can have as many as three access arms. Each arm has a top and bottom read/write head. The head selection circuits must select and electronically connect one of the four heads to the write driver and read amplifier circuits. Selection is accomplished by switching the voltage applied to the erase coil of each head. The head select driver provides the switching voltage; +6 v for a selected condition, —20 v for a deselected condition (Figures 5-4 and 5-6).

### Head Select Driver

A head select driver is provided for each head (four for dual access, six for triple access). The proper driver is selected by ANDing the record address (which determines upper or lower head), the selected access (75.61.21.1), *write safe* and *access safe* (Figure 5-6). The development of *write safe* and *access safe* are covered later.

Refer to the component circuits section in the ALDs for card type AGN. A —T input forward biases T7. T7 conducts to lower its emitter voltage which forward biases T1. T1 conducts and pin E and H rise to approximately +6 v. The 2.5 mh choke is in series with the erase coil. The choke tends to minimize variations in erase current as the write drivers alternately conduct.

When the head select driver is deselected, pins E and H drop to —20 v.

### Head Matrix

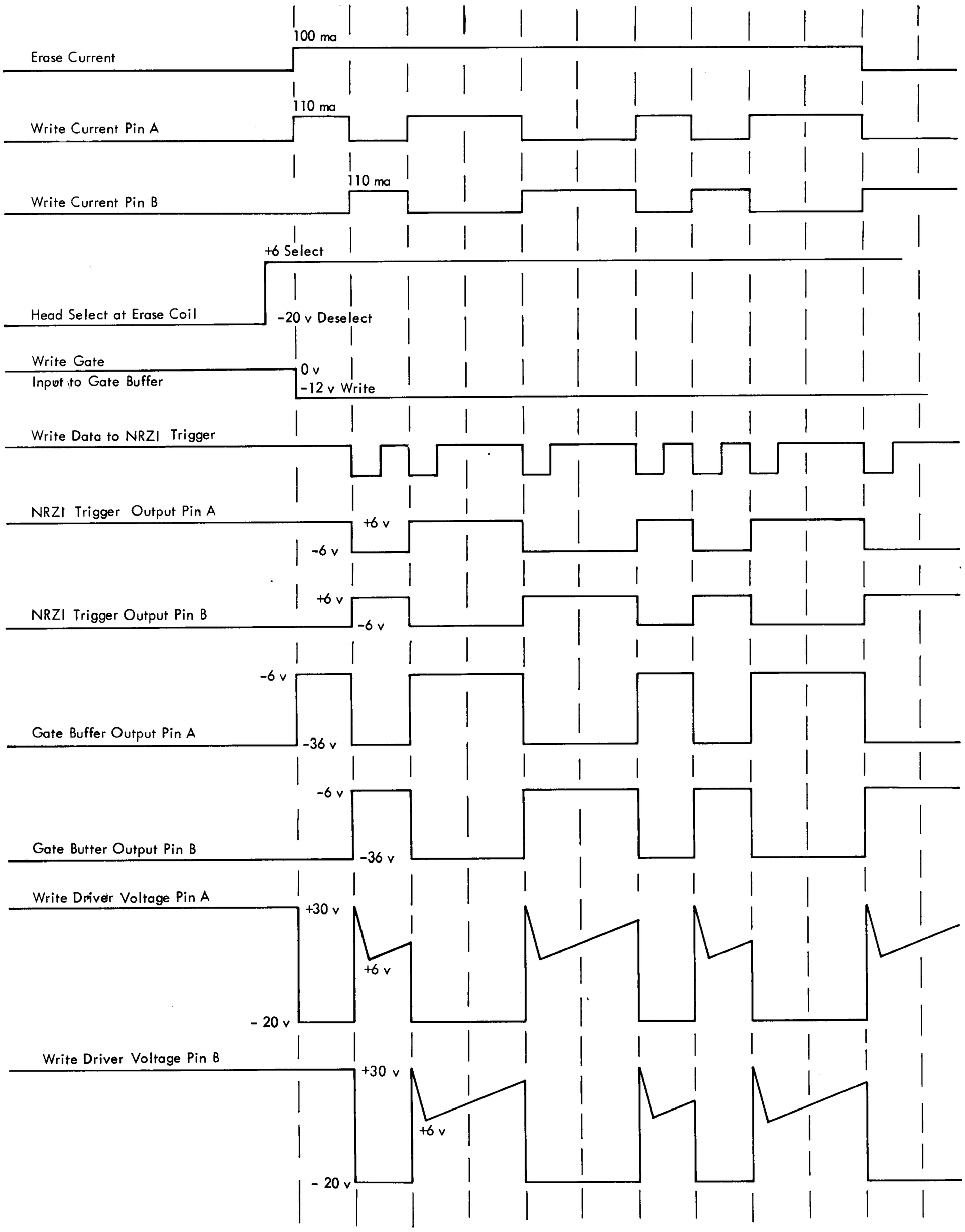
A type AGU card provides a diode network that allows either half of a selected head to be used for reading or writing. The card contains four diodes connected as shown in Figure 5-6.

If we assume that the upper head is selected and the *write gate* is up, head select driver A is supplying +6 v to point E. When the output of the write driver (connected to pin B) drops to —20 v, D43 is forward biased and the A side of the upper head draws write current. The next data bit causes point B to rise to +30 v and reverse biases D43. Point G (lower diode group) is then at —20 v (the write drivers alternate with each data bit). Diode D18 is now forward biased and write current is drawn through the B side of the upper head. In this manner, each data bit is recorded with opposing magnetic polarity.

If the *write gate* is down and the upper head is selected, points B and G are both at +30 v, D43 and D18 are both reverse biased and writing cannot take place. However, D21 and D40 are forward biased by the *not write gate* applied to pin C of the pre-amp (2A-75.62.11.1) therefore the upper head is selected for reading.

## *Safety Circuits*

The 1405 disk storage machine is used as a permanent




Idealized Voltage and Current Waveforms for Write Driver Circuit

Figure 5-5 Write Driver Circuit – Idealized Waveforms

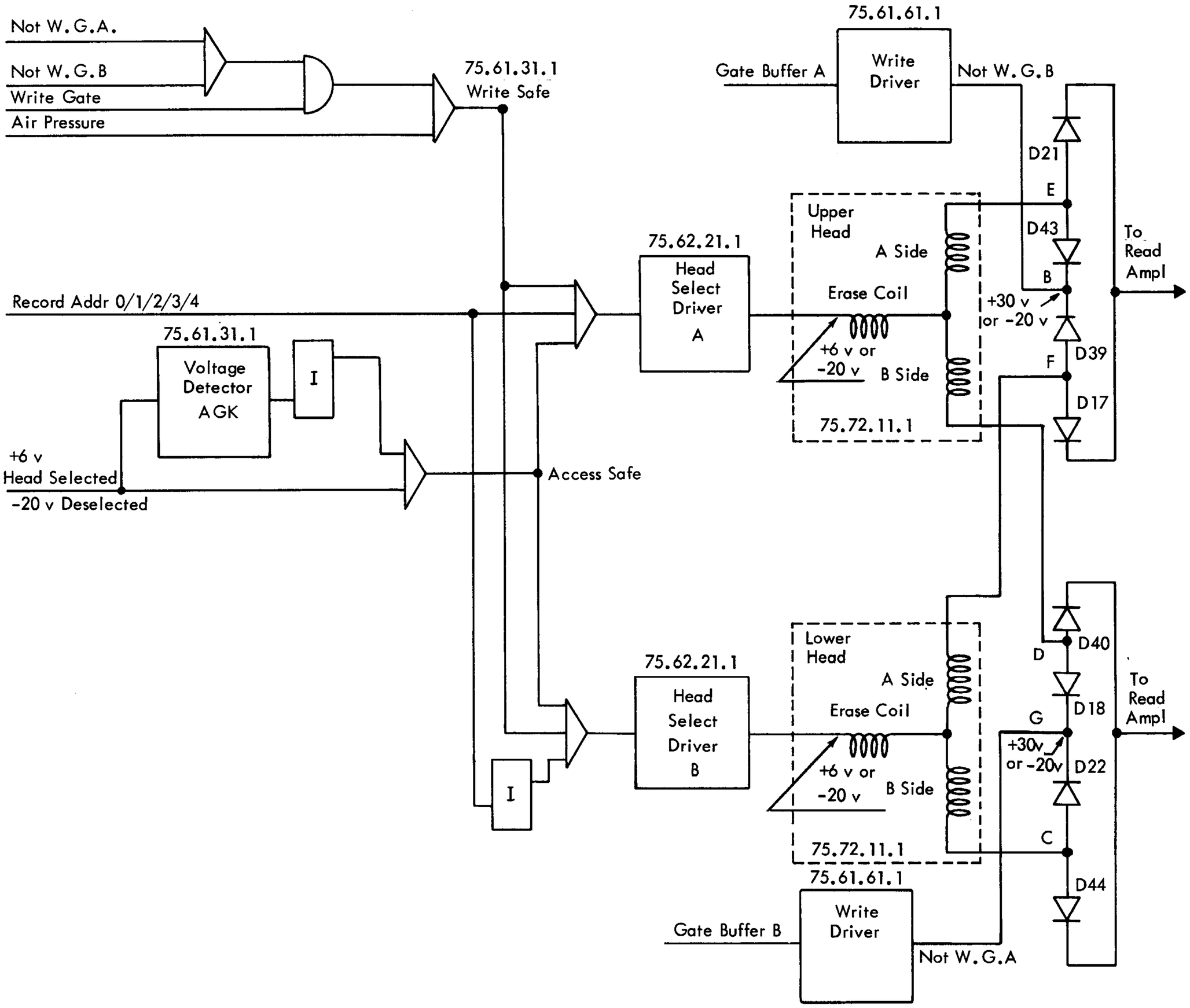



Figure 5-6. Head Selection

data storage device. Therefore, great care has been taken in the circuit design to protect the data stored on the disks. Several means are used to accomplish this objective.

The use of the indelible address associated with each record provides for a location check before new data is recorded. Two types of safety circuits are provided to deselect, or prevent selection of a head if improper voltage levels exit in the write driver, write gate or read-write head areas. The write safety circuit is used to deselect the head and generate a *file not safe* condition if a write driver turns on without a *write gate.* The head safety circuit detects failures in the read-write head or head cabling that cause an improper output voltage from head select driver. When the output from a head select driver is less than +5 v (when selected) or more positive than −5 v (when deselected), an *access not safe* condition results. The head is then deselected or not selected depending on its status.

### Write Safety

During a read operation, the write gate is down. Both write drivers are cut off and their output signal level is +30 v. Thus, the *write safe* line will be up to allow a head to be selected for reading purposes (Figure 5-6). Under these conditions, if either write driver conducts, *write safe* is dropped. This prevents any attempt to write while performing a read operation.

During a write operation, one write driver is cut off, the other is conducting, and the *write gate* is up. Again, the *write safe* line will be up. Note at this time,

whenever the *write gate* and *file safe* (air pressure) are up, a *write safe* condition exists. *File safe* is dot ORed at 6G (75.61.31.1) from 4E (75.61.91.1).

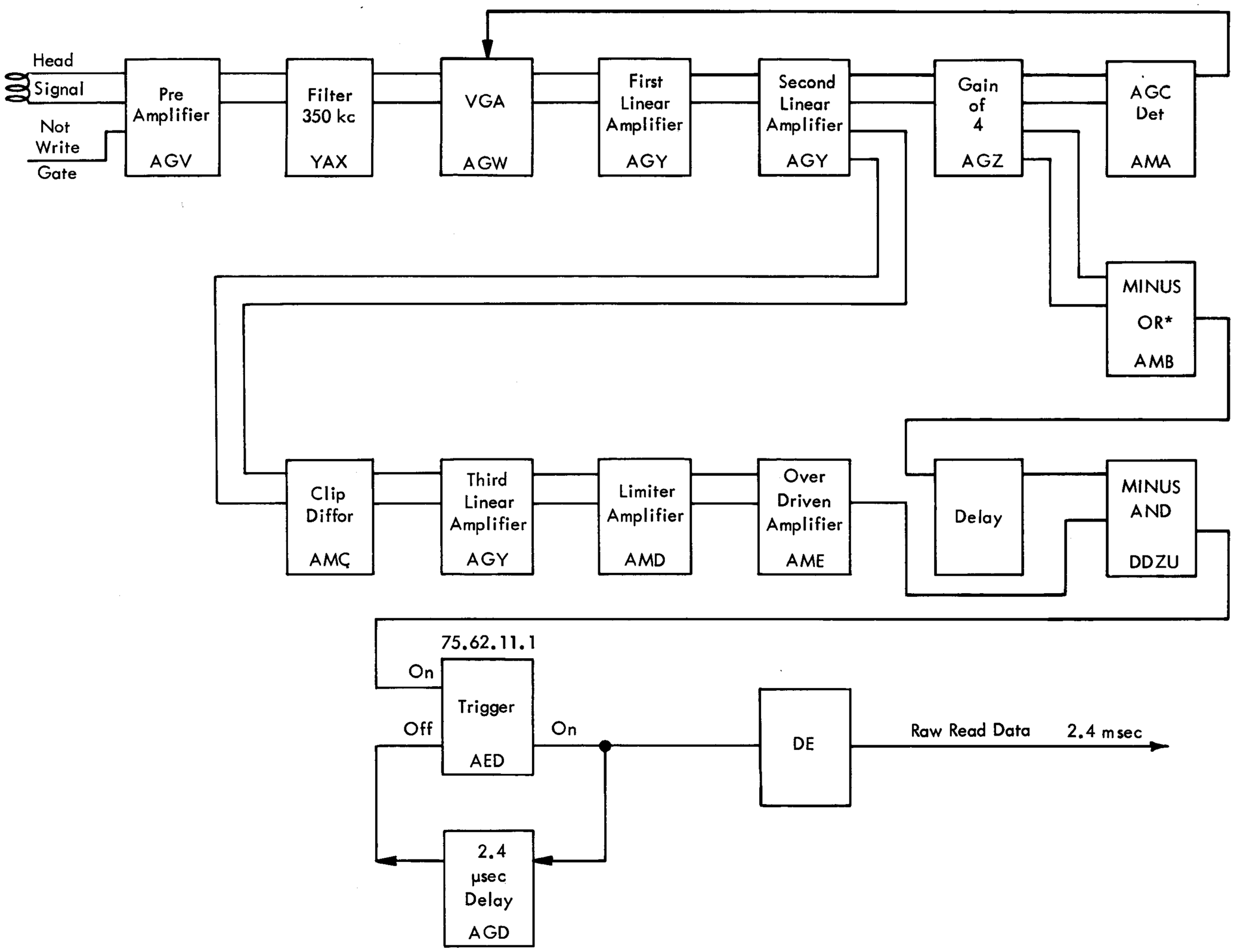
### Head Safety

Head safety is established when one of the *access safe* lines is brought up (75.61.31.1).

The head safety circuit detects failures in the read-write head or head cabling that could cause record erasure.

With power on, the head select drivers should always have an output of —20 v deselected, or +6 v selected (75.62.21.1). A significant deviation from these two voltage levels is recognized by a voltage detector (2A-75.61.31.1) as an access not-safe condition (Figure 5-6).

Refer to the component circuits section in the ALDs for card type AGK. One card contains three circuits; two circuits are required for each access. T3 is continually forward biased and conducting to provide a constant emitter voltage for T7. This voltage is such that an input of less than +5 v causes T7 to conduct and its output to become more positive. This output is one input to a two legged AND block (3A-75.61.31.1). The other leg is the direct output from the head select driver. When both inputs to A3 are satisfied, the *access safe* condition is dropped. For example, if a head cable becomes grounded, the output voltage of that head select driver will be more negative than +6 v while the head is selected, or more positive than —5 v if the head is deselected. Under these conditions, the inputs to 3A are satisfied and *access safe* is dropped.




*The OR circuit conducts with a signal that is at least 40 per cent, or greater, of maximum. Maximum signal at this point is 4.2 volts peak-to-peak when measured with a 310 oscilloscope.

Figure 5-7. Read Amplifier — Block Diagram

## *Read Amplifier Circuits*

The block diagram in Figure 5-7 shows the various components that constitute the read amplifier. The circuit is designed to accept a differential signal of 10 mv to 50 mv peak-to-peak from the read-write head. From this input it develops 2.4 $\mu$s raw read data pulses. (75.62.11.1)

An AGC detector is used to establish the gain to the linear amplifier stages. A group of AGC bits is recorded on the tracks ahead of the indelible address and ahead of the record information to permit setting the gain of the amplifier. The AGC level, 40% signal rejection, and the balance of the limiter and overdriven amplifier stages, are adjustable.

A slight amount of clipping is used to reduce the effect of overshoot. Overshoot may occur when the signals recur at the minimum bit rate of 30 kilobits per sec.

### Pre-Amp

Refer to the component circuits section in the ALDs for card type AGV. The pre-amp stage is a direct-coupled, linear-signal amplifier. Its function is to amplify (gain of 2) the incoming read signals. The differential input provides for noise rejection. In addition, T3 provides a constant current source that acts to reject common mode signals. The common mode rejection is approximately 300:1.

The *not write gate* applied to pin C provides —6 v during a read operation to forward bias the read diodes in the head matrix and diodes 38, 39 in the pre-amp. During a write operation, pin C is +20 v to adequately reverse bias the read diodes and diodes 38 and 39 in the pre-amp. D43 and D45 clamp the input at +8 v for large noise signals.

### Butterworth Filter

The Butterworth Filter card type YAX provides the AC load and DC biasing for the pre-amp. It is a lossless-ladder network acting as a low-pass filter. Its purpose is to reject high frequency noise signals that might appear in the output of the pre-amp.

### Variable Gain Amplifier

Refer to the component circuits section in the ALDs for card type AGW. This circuit working with the AGC current feed back provides a variable output to effectively set the input signal to the succeeding stages at a constant level. Thus, the variable gain control circuit compensates for the variation in input signal amplitude due to the change from inside to outside tracks, radial misalignment, or minor inherent differences between heads.

The gain of the VGA circuit varies from 0 to 3. T4 and T6 operate as a linear differential amplifier. The output is RC coupled to a variable impedance network consisting of R12, R13, D10, and D23 (D20 and D21 are used to suppress any negative switching spikes). D10 and D23 act as variable impedances because they are operated on the non-linear portion of their forward conductive curve. For example, the greater the current signal supplied to pin A by the AGC detector the higher the diode current becomes and the lower their impedance becomes. Consequently, a group of high amplitude signals develops a greater AGC current causing D10 and D23 to conduct more heavily reducing the output impedance and the gain of the VGA. The loop gain will then restore to its original value.

### Linear Amplifier

Refer to the component circuits section in the ALDs for card type AGY. The linear amplifier is a two-stage, direct-coupled, differential amplifier. Its gain and bandwidth are controlled by an RC negative feed back from T2 and T6.

The calculated gain of the amplifier is 15. The actual gain is approximately 12.5 with an overshoot on low frequency signals of about 15%.

### Clipper Amplifier

Refer to the component circuits section in the ALDs for card type AGZ. The clipper amplifier is a linear amplifier having a gain of four. The emitter-follower input stage feeds a common emitter amplifier stage. The amplifier has some negative feedback provided by the common emitter resistor R11. The emitter-follower output stage is designed to match the low impedance input and voltage level requirements of the OR circuit and the AGC detector.

The output stage provides an AC couple to the AGC detector and a direct couple to the special OR circuit. The output signal amplitude is approximately 24 v peak-to-peak.

### AGC Detector

Refer to the component circuits section in the ALDs for card type AMA. The AGC detector is used to detect the signal amplitude and control this amplitude by supplying a feed back signal to the VGA circuit. This feed back signal controls the load impedance of the VGA circuit; as the feed back signal increases, the output impedance of the VGA decreases to reduce the gain.

The bias on the common bases of the input transistors T7 and T8 is adjustable. This permits the establishment of a threshold that determines the amplitude of the negative signal required to turn T7 or T8 on.

If T7 or T8 conducts, charging current is supplied to C32. As the charge on C32 is increased, the base of T4 becomes more negative and its emitter approaches —6 v; T5 then conducts more heavily supplying more AGC current to the AGC stage, reducing the gain.

The loop gain will soon stabilize at the new gain level and the output of the second linear amplifier will be approximately 7 v peak-to-peak. The attack time of the AGC circuit is quite rapid. About 8 AGC bits are required to set the gain from no signal to a signal of 40 mv peak-to-peak.

It may be necessary to set the AGC rapidly when going from a group of high amplitude signals to a new group of low amplitude signals (i.e., indelible address to record AGC bits). This is accomplished by rapidly discharging C32 through T3. T3 is forward biased by *read amp reset* applied to pin D.

### Clipper Differentiate

The output of the second linear amplifier is capacitively coupled to the input of the clipper differentiate circuit. This differential input signal is normally 7 v peak-to-peak.

The input bias network will clip off the positive signal excursions. It also causes a small amount of base line clipping on the negative signal excursions. This negative clipping action is due to the slightly positive bias on the bases of T1 and T3. The negative signal input must exceed this reverse bias before it can turn T1 or T3 on.

The input to T5 and T6 is an RC differentiating network. The RC circuit has a time constant of approximately .2 $\mu$s. This circuit functions so that the peak of the negative input signal to T1 or T3 will be a zero voltage crossover at the base of T5 or T6.

### Limiter and Overdriven Amplifier

Refer to the component circuits section in the ALDs for card types AMD and AME. These two stages are used for shaping the output of the differentiated and amplified signal. They amplify and produce a steep sided pulse with a flat crown at the output of the overdriven stage. The leading edge of this pulse is gated through the minus AND circuit by the output from the OR circuit. The output signal of the clipper amplifier is approximately 23 v peak-to-peak.

### OR Circuit

Refer to the component circuits section in the ALDs for card type AMB. With no signal present, T5 and T7 are on, T4 and T6 are off, and T3 is on. The collector voltage at T4 and T6 is —5.2 v determined by the divider R44 and R36. P1 in the emitter circuit at T3 can be adjusted to vary the cut off bias on T4 and T6 from —9 v to —22 v.

Assume that P1 is adjusted to provide a cut off bias of —20 v. A positive input signal to pin E will cause T7 to conduct more heavily. Its emitter will follow toward —11 v and T5 will remain cut off. However, as the signal on pin E goes positive, the signal on pin F goes toward —25 v. When the emitter of T5 is approximately —20.5 v, T4 turns on and its collector voltage drops to about —7 v (Figure 5-8).

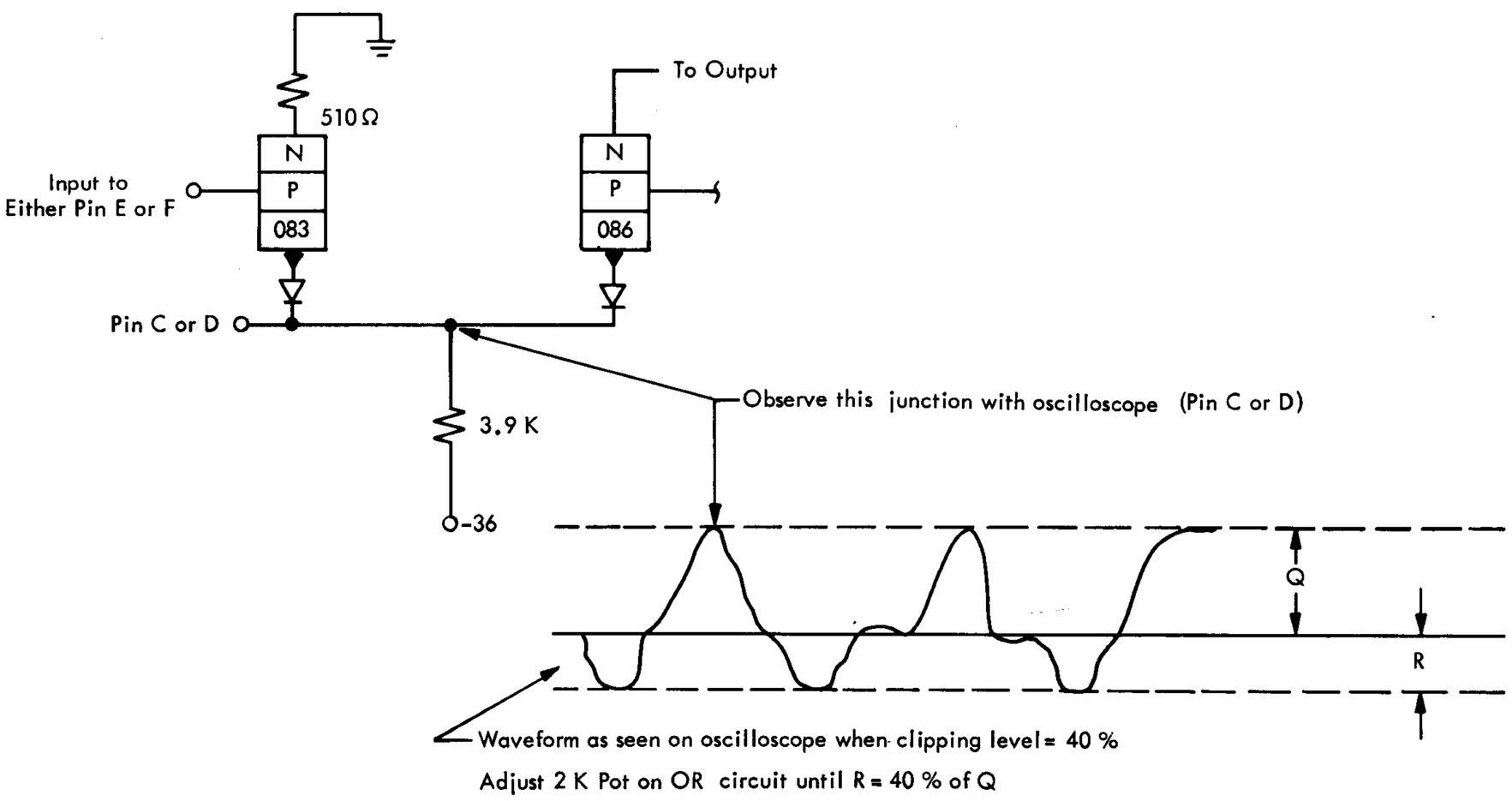



Figure 5-8. OR Circuit — Waveforms

The common emitter between T4 and T5 holds at approximately —20.5 v, T4 turns on and its collector voltage drops to about —8 v (Figure 5-8).

The common emitter between T4 and T5 holds at approximately —20.5 v while T4 is on. Therefore, T5 cuts off and remains off until the input voltage swings back to approximately —20 v. T5 then turns on, turning T4 off as the common emitter reaches approximately —20.2 v. The collector voltage of T5 then returns to —5.2 v.

**Read Data**

The output from the minus AND circuit (6E-75.62.11.1) goes through two stages of shaping and level setting. The leading edge of this signal is then used to turn on the data trigger (occurs at the peak-of-the-head signal).

The data trigger output is then fed through a special 2.4 $\mu$s delay card (AGD) to turn the data trigger off. Read data, at this point, is therefore a 2.4 $\mu$s pulse for each data bit read.

# Section 6 Read Single Record Operation (1405-1401)

A read single record operation is called for by the instruction M%F1BBBR. The operation is performed in the following sequential steps:

1. 1401 instruction cycles
2. Address transfer
3. Read pre-indelible address AGC bits
4. Read indelible address
5. Read pre-record AGC bits
6. Read data record

Figure 6-1 contains a block diagram showing the basic data flow during a read, write, or seek operation. This diagram, along with the sequence chart (Figures 6-2 and 6-3) and the data flow diagram (Figure 6-4), are provided to supplement the explanation of the read operation.

## *1401 Instruction Cycles*

During the 1401 instruction cycles, the 1405 monitors the output of the 1401 B register through the ATU. The basic objective during these cycles is to set latches in the ATU and the CPU to prepare the 1405 and the CPU for a file-read operation.

### Percent Latch

The percent latch is set in either a move or load status by the decode of percent (A84) at 060 to 090 time during I-ring 1 (75.02.11.1). This latch signifies that an input/output device is to be used with this instruction.

### File Op Latch

The file op latch is set by a decode of F if the percent latch is on at 060 to 090 time of I-ring 2 (75.02.11.1). This latch signals the 1405 that this is a disk storage unit operation.

### Single Record Latch

The single record latch is set by a decode of 1 at 060 to 090 time of I-ring 3 if the *+U gated file op* line is up (75.02.51.1). The *+U gated file op* is up when the file op latch is on and the write check interlock latch is off. The write check interlock latch, when ON, prevents any file operation except a write check. It turns on during a write operation and turns off when a write check is made.

The single record latch is used to gate the output of the read file (or write file) latch to the control unit.

### Read File Latch

The read file latch turns on if the write check interlock latch is off at 060 to 090 time of I-ring 7 if the instruction contains an R and the file op latch is on (75.02.31.1). Its output is gated by the single record latch and is subsequently used to turn on the read gate latch.

### First Address Transfer Latch

The first address transfer latch turns on at 105 to 000 time during I-ring 7 if the file op latch is on (75.04.21.2). It is used to gate the B address plus one into A STAR (1401). It also blocks the digit ring advance pulse during the first B cycle following the 1401 I cycles. It is reset during 090 to 105 time of this first B cycle.

### 400 μs Single Shot

The 400 μs single shot fires as soon as the read file latch turns on provided the 1405 is not in a CE test status (75.28.11.1).

The single shot prevents the start of the read operation until it times out. This circuit is necessary for two reasons. First, the 1405 is not ready to begin the read operation until after the address transfer step and it is impossible to predict when the correct record start pulse will occur. Second, during the address transfer step, the record head is selected. This selection causes noise to be fed into the read amplifier. The 400-μs delay provides a recovery time for the read amplifier. If the correct record pulse occurs during the address transfer step, it is blocked. The 400 μs single shot will have timed out by the time the disk array completes the next revolution allowing the read operation to continue.

## *Address Transfer*

The following basic objectives are accomplished during the address transfer step:

1. The B-address plus one is gated into A STAR.
2. The 1405 digit ring is advanced.
3. The access digit is transmitted from the 1401 B register to the 1405 select register.
4. The module digit (file No.) is transmitted from the 1401 B register to the 1405 select register. (Disk and track addresses are stored in the address relays from the previous seek operation.)
5. The record digit is transmitted from the B register to the 1405 record register.
6. A STAR (BBB+1) is gated to MAIN STAR (1401).
7. The 1401 clock is stopped.

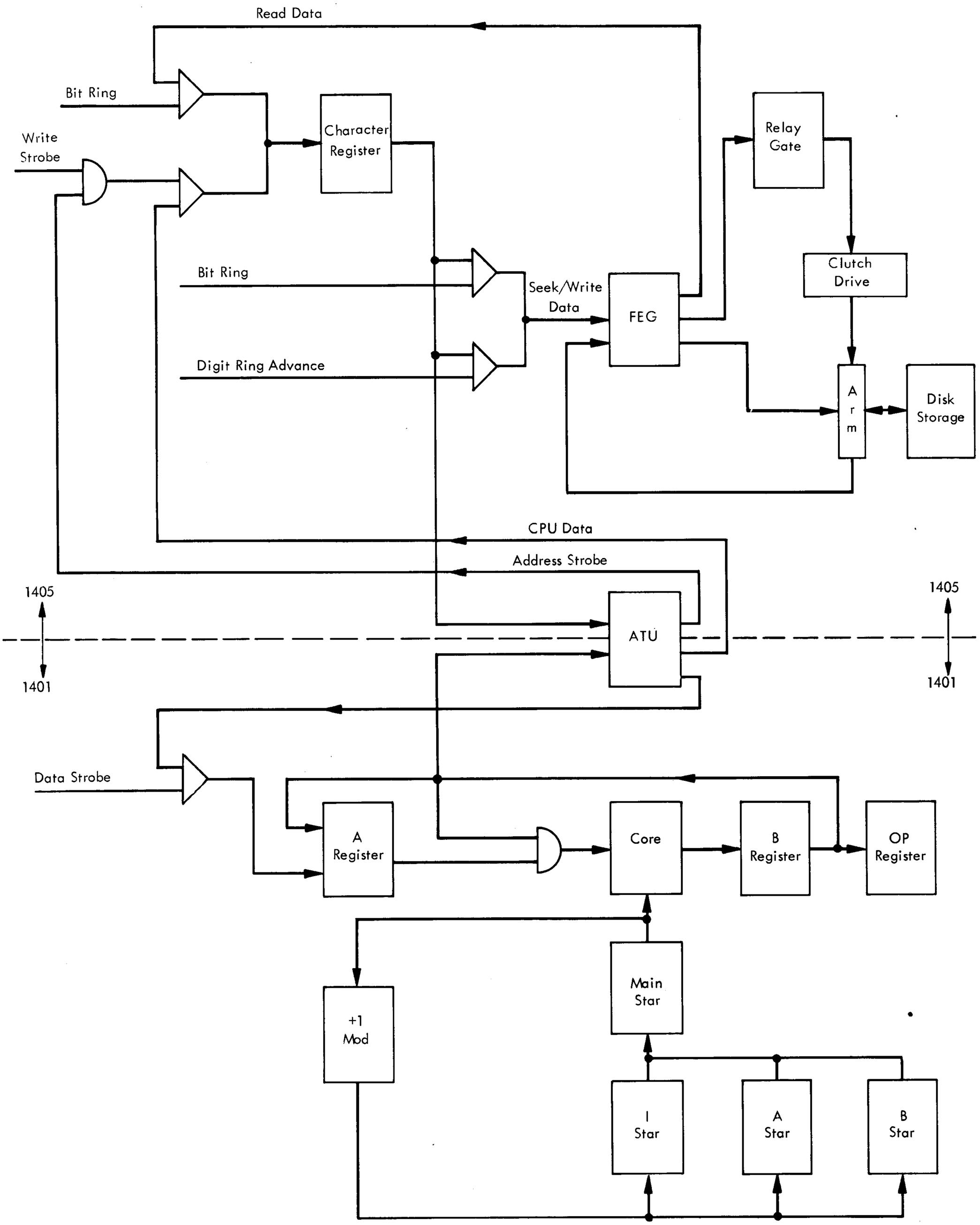



Figure 6-1. Basic Data Flow for Seek, Read, or Write

| SIG NAME<br>1405 BIT TIMES | ALD<br>Øa → | TEST POINT<br>01A: |
|---|---|---|
| −T START R/W TR. | 75.28.11.1 | 2J24N |
| −T RECORD PULSE | 75.28.01.1 | 2B02D |
| −T START R/W PULSE | 75.28.11.1 | 2G06G |
| −T A FOR B SUBSTITUTE | 75.04.21.2 | 1D17N |
| −T SECTOR GATE | 75.04.51.2 | 1D14P |
| −T ADDRESS GATE | 75.29.01.1 | 2F10H |
| −T AGC GATE (ØC) DEL | 75.29.01.1 | 2G14E |
| +U CTRL. CTR. ADV. (Øb) | 75.32.01.1 | 2F19F |
| −T STANDARD RD. DATA | 75.31.11.1 | 2C04F |
| −T READ GATE | 75.35.01.1 | 2G07E |
| −T NOT RD. DATA TR. | 75.32.01.1 | 2B22D |
| +U CTRL. CTR. 36 | 75.32.21.1 | 2H22H |
| −T COUNT 48 GATE | 75.32.21.1 | 2F18H |
| +U CTRL. CTR. 52 | 75.32.31.1 | 2H27H |
| −T DIGIT RING ADV | 75.04.51.2 | 1C28H |
| +T CHAR. REG. RESET | 75.36.01.1 | 2F10A |
| +T CTRL. CTR. RESET | 75.31.11.1 | 2C23A |
| −T COMPARE GATE | 75.04.31.2 | 1D23N |
| +U SET BIT S | 75.33.01.1 | 2C28A |
| −T BIT RING ADV. GATE | 75.33.01.1 | 2C25E |
| −T BIT RING ADV. PULSE | 75.33.01.1 | 2C07F |
| −T READ STROBE GATE | 75.31.11.1 | 2A26E |
| −T RESET A REG. | 75.01.71.2 | IN 1401<br>02A8 D11G |
| −T DATA STROBE | 75.31.11.1 | 2G10N |
| +U STORE A REG. | 75.04.51.2 | 1D24C |
| −T EXTRA CYCLE | 75.04.51.2 | 1D21P |
| −T 1401 CLOCK CONTROL | 75.04.11.2 | 1D22C |

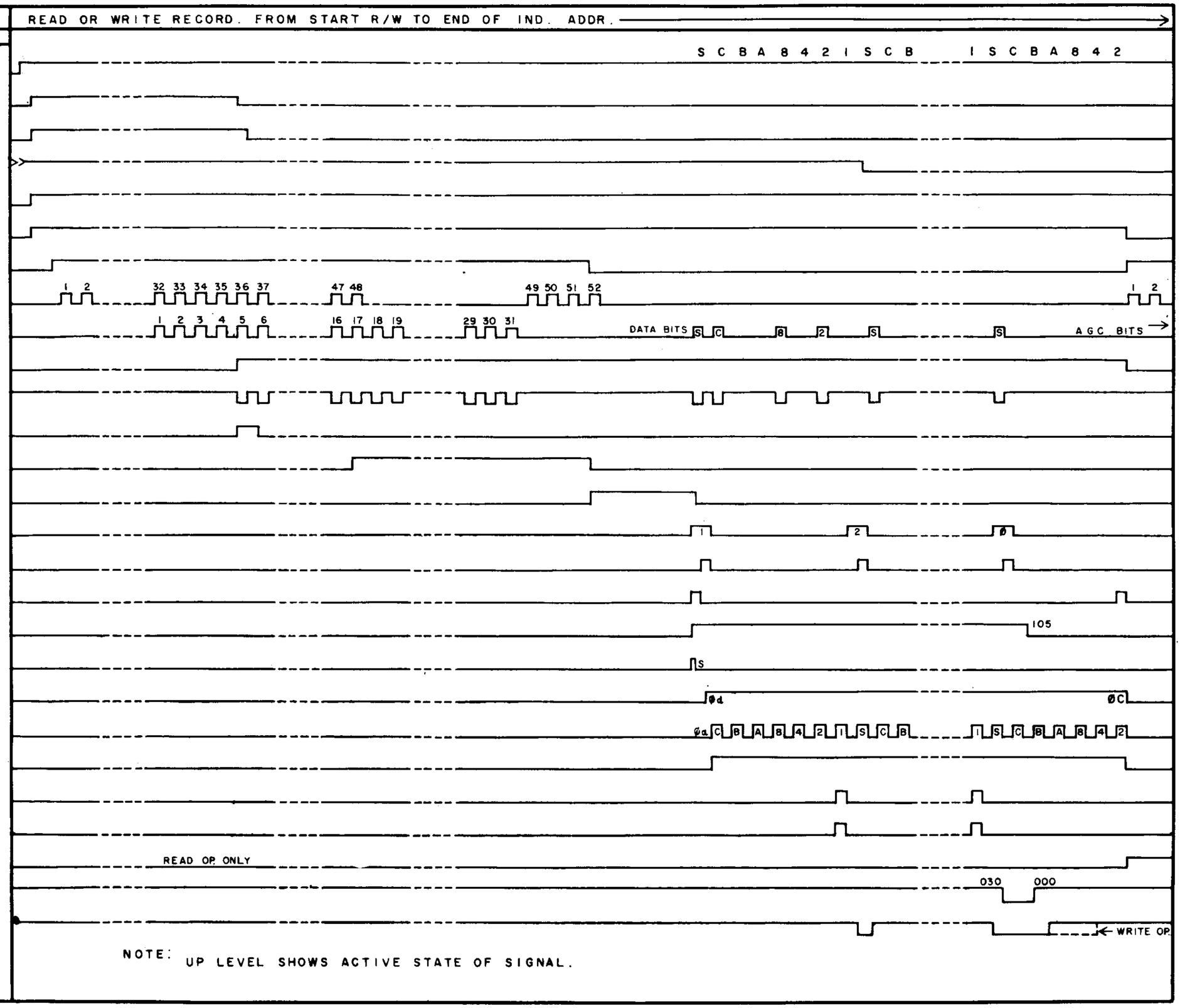
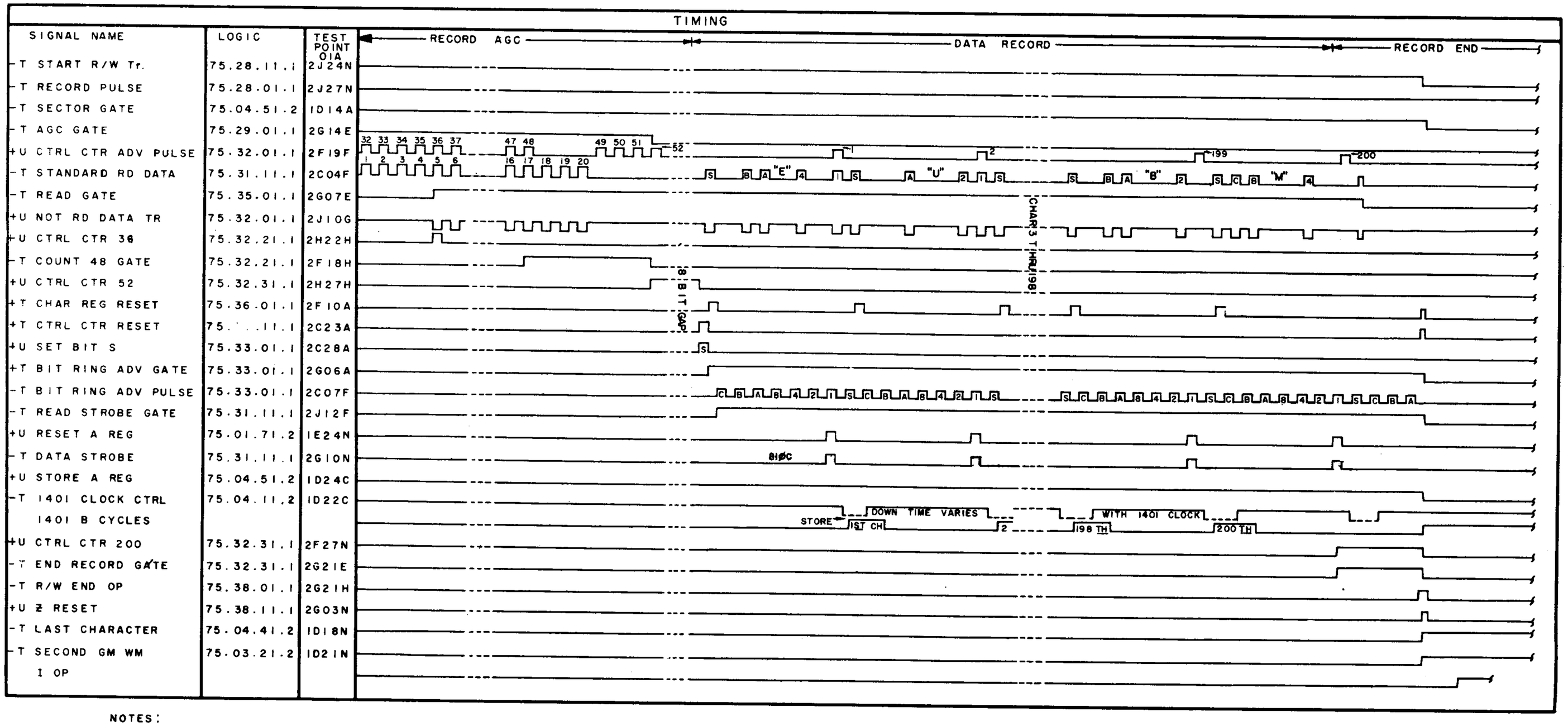



Figure 6-2. Read Indelible Address




NOTES:

1. THIS CHART SHOWS A MOVE OP. LOAD IS THE SAME EXCEPT:
   - (1) BIT RING INCLUDES A WM BETWEEN "S" AND "C" BIT.
   - (2) OPERATION ENDS WITH COUNT 176 INSTEAD OF COUNT 200
2. UP LEVEL SHOWS ACTIVE STATE OF SIGNAL.

Figure 6-3. Read Single Record — After Indelible Address Time

### Gate B-Address Plus One into A STAR

To enable the 1401 to compare the indelible address on the disk with the record address in core storage, the address of the module digit must be available to the 1401 during the first B cycle of the indelible address step. (The access digit is not a part of the indelible address).

During the first B cycle of the address transfer step, the first address transfer latch is ON. The output from this latch is powered up (75.01.71.2) and transmitted to the 1401 to gate the B-address plus one into A STAR.

The first address transfer latch is reset at the end of this first B cycle.

### Advance the 1405 Digit Ring

The digit ring (75.21.11.1) enables the 1405 to identify the address characters during address transfer and indelible address time.

When the digit ring is reset, the digit 0 trigger remains on; all others are turned off. The ring is reset initially with a *begin op reset* (75.38.11.1). The *begin op reset* line is activated 3 $\mu$s after the file op latch turns on.

During the address transfer step, the digit ring must advance at 1401 speed. This enables the digit ring to stay in step with each B cycle and thus identify the address characters. The ring is advanced at 000 to 015 during each *delta B cycle* if the *address transfer gate* is up and *first address transfer* is down. However, *first address transfer* is up during the first B cycle of the address transfer step to prevent the digit ring from advancing to digit one for the access character (access character is digit zero of the record address, Figure 6-2).

The *address transfer gate* is brought up on the first B cycle following the set of the first address transfer latch (75.04.21.1). It is reset at 105 to 000 during digit 7 time (eighth B cycle). See Figure 6-4.

The ring is reset to digit zero at the beginning of the pre-indelible address AGC step when *start read-write* comes up.

### Transmit Access and Module Characters

When the 1401 completes the instruction cycles, a normal I/E change occurs. *A cycle eliminate* is up as a result of the read file instruction therefore the 1401 begins a series of B cycles.

During the first B cycle, the access character (digit zero time) is strobed into the 1405 character register by the *address strobe* line (75.36.01.1). *Address strobe* (75.04.21.2) is available at 030 to 060 time during each B cycle that occurs while the address transfer latch is ON.

The access character, as an output from the character register, is immediately available to the select register (75.23.01.1). The requirements for entry into the select register are satisfied as *digit zero,* and *delayed address strobe* are both up. The module character is handled in the same way on the second B cycle at digit one time.

The disk and track address characters are not required by the 1405 at this time. They were stored in relays during the previous seek operation. Therefore, nothing significant occurs during the time between the beginning of the third B cycle and the end of the sixth B cycle (digit 2 through 5 time).

### Transmit the Record Digit

During the seventh B cycle (digit 6 time), the record character is transmitted to the 1405 character register (75.60.41.1). The character register output is then ANDed with *address strobe delay* (75.24.41.1). The resultant $+N$ *bit* line is powered up and converted to a $-T$ *bit* line. The record address register is then set during digit 6 time, if the address and module have been selected and the read file latch is ON.

The *address strobe delay,* used to strobe the record character into the record address register, provides a 1.2 $\mu$s delay from the normal address strobe.

### Gate A STAR to MAIN STAR

A STAR now contains the address of the module digit. To enable the proper comparison to be made during the I. A. step, A STAR is transferred to MAIN STAR during digit 7 time of the address transfer step.

The A for B substitute latch controls this transfer (75.04.21.2). The latch is turned on at 060 to 090 time during digit 7 of the eighth B cycle if *address transfer* is up (3D). The resultant *A for B substitute* line is interconnected to the 1401. *A STAR gate out* (BBB+1) takes place during 090 to 000 of this eighth B cycle. MAIN STAR modified by one (BBB+2) is gated to B STAR during the next B cycle.

### Stop the 1401 Clock

During the eighth B cycle (digit 7 time), the compatibility character is read into the 1401 B register. This character is not used when the 1405 is combined with the 1401 system, however, it is compared.

After the eighth B cycle, the 1401 clock is stopped when the clock control latch is turned off (Figure 6-5). The conditions required are *address transfer, not seek op, not write address,* and time 060 to 090 of digit 7 (6F-75.04.11.2). *Address transfer* is up until 105 to 000 of digit 7 time.

At the end of the address transfer step, the following significant conditions exit:

1. The 1401 B register contains the compatibility character (0).
2. The 1401 main storage address register contains the address of the module character (the original B address plus one).

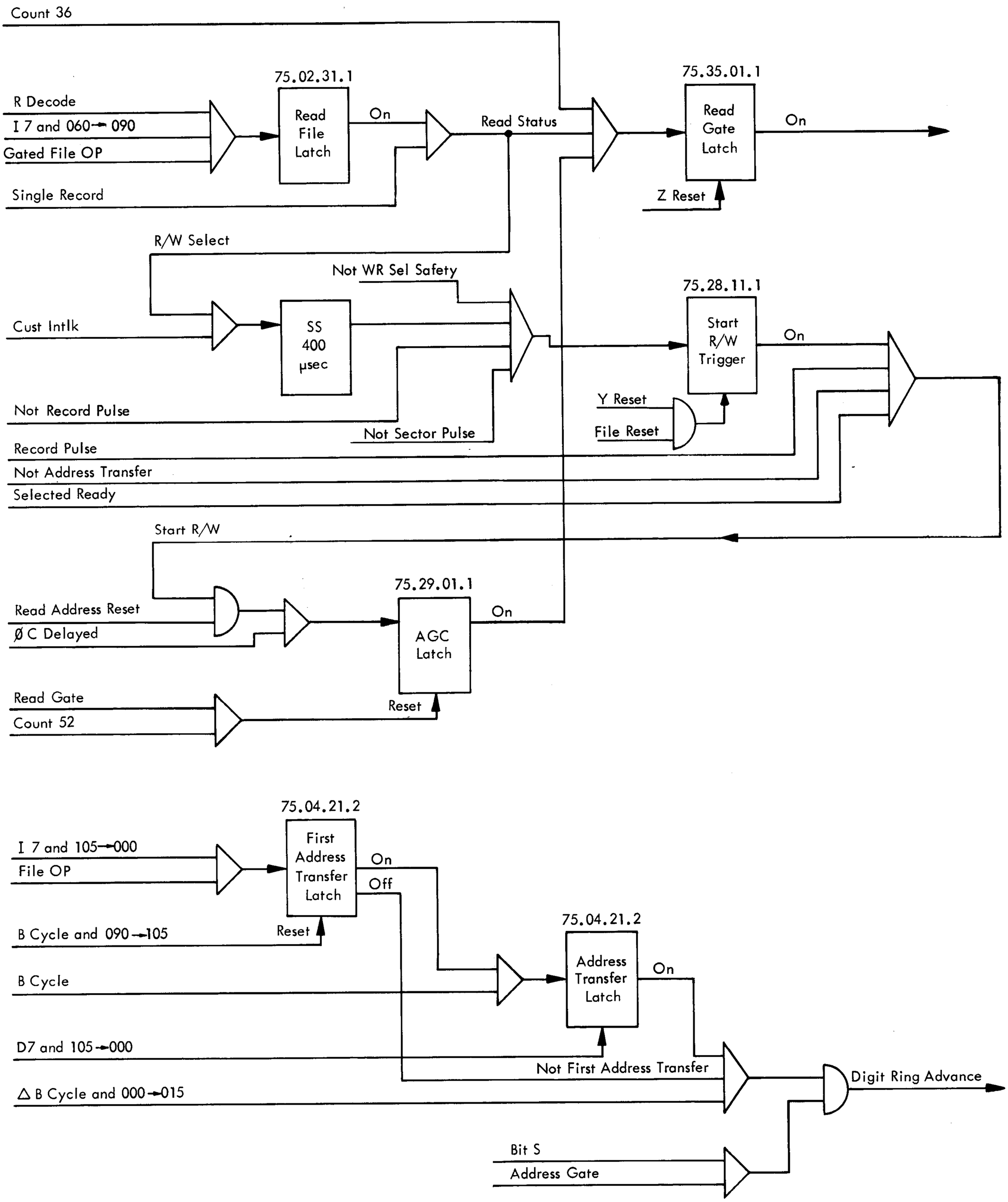



Figure 6-4. Read Single Record Operation

3. The 1401 B address register (B STAR) contains BBB + 8.
4. The 1405 digit ring is at digit 7.
5. The *address transfer gate* is down.
6. The correct read-write head has been selected for reading.
7. The A for B substitute latch is ON.

### *Read Pre-Indelible Address AGC Bits*

The basic objective of this step is to set the gain of the read amplifier. With the gain set, the indelible address can be properly read (see READ AMPLIFIER).

In addition to the objective, conditions are set up during this step to allow the indelible address to be read and transmitted to the 1401. The following pulses

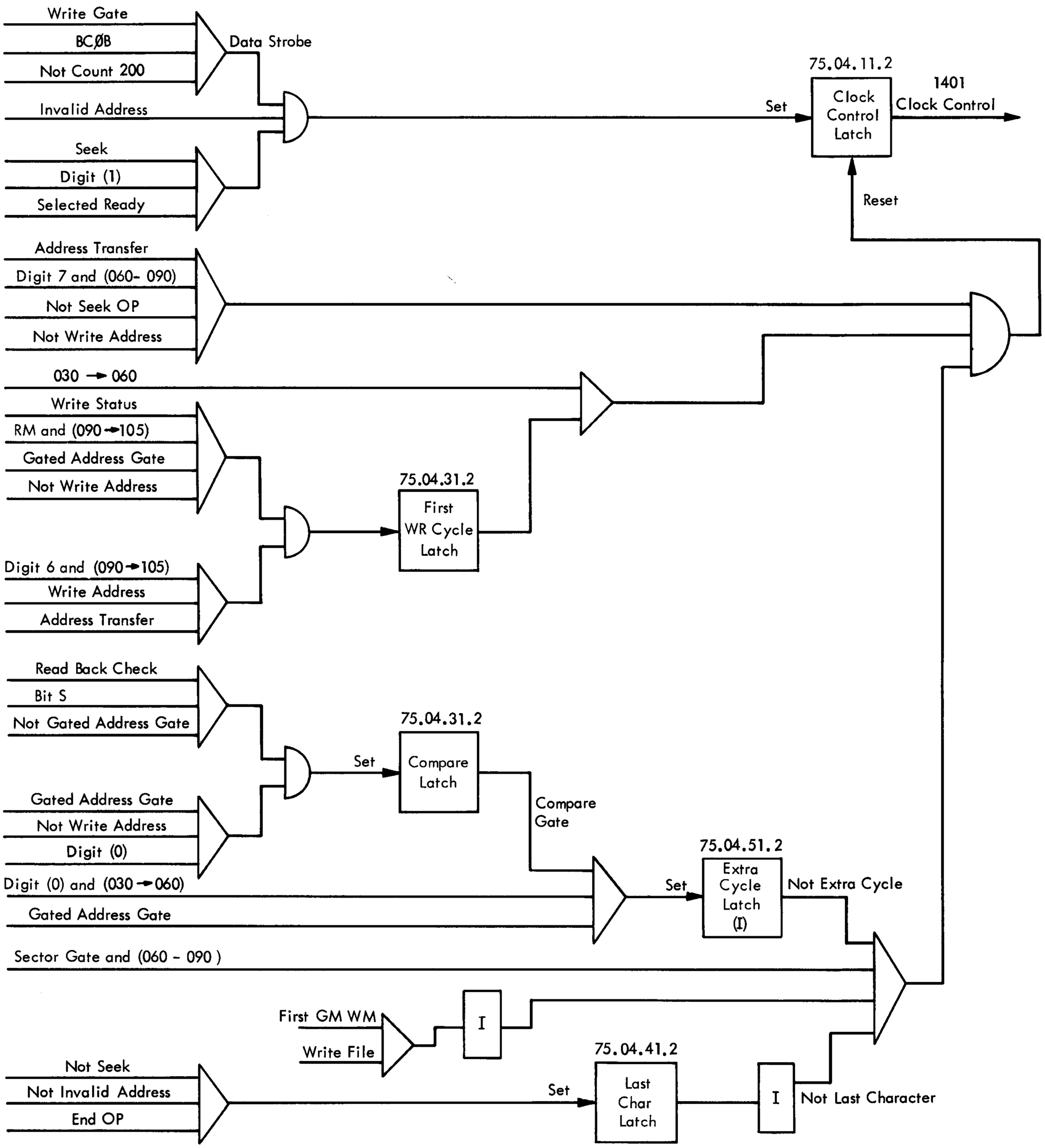



Figure 6-5. Clock Controls

and gates are therefore developed:

1. Start read/write pulse.
   a. sector gate
   b. address gate
   c. AGC gate
2. Record pulse
3. Selected ready
4. Control counter pulses

### Start Read/Write

When the 400 μs single shot times out, the start read/write trigger turns on provided a record or sector pulse is absent (5A, 5D-75.28.11.1). The trigger output is ANDed with *record pulse, selected ready,* and *not address transfer* to provide the start read/write impulse (Figure 6-4). *Start read/write* is then used to turn on the sector gate latch, the address gate latch AGC latch and to reset the digit ring.

The sector gate latch (75.04.51.2) provides a circuit during the data record portion to allow the 1401 A register to be gated into core storage during a read operation (not WRITE CHECK). The address gate latch (75.29.01.1) provides a gate that defines the address portion of the record. The AGC latch (75.29.01.1) provides a gate which functions with the control counter to define the portions of the sector that contain AGC bits.

### Record Pulse

Figure 6-6 shows the development of a *record pulse* for access 0 in module 0. This circuit employs three special cards.

The AGM card supplies the emitter bias for the five AGL circuits. The AGL card provides the selection of a single record head within the matrix. The AGJ card amplifies the induced signal from the selected head.

The selected access (0) and the selected module (0) are ANDed with *R/W select* to develop *access 0 R/W select* (75.30.01.1). This line is level set to —U and becomes the input to the AGM card (75.60.21.1) and forward biases T3. T3 conducts and supplies —6 v to the emitter circuits on the AGL cards. The base circuits for the AGL cards are supplied from the record address register. Thus, if the record address register contains 0/5, T7 is forward biased. As the permanent magnet (located on upper dummy disk) passes the 0/5 record head, a signal will be induced in the 0/5 record head coil. This signal is reflected by T7 and forward biases the pulse amplifier. The transistors in the AGL card circuits, for the unselected heads, are reverse biased (0 v on the base leg).

If both *access 0 R/W select* and *record address* are down, all of the AGL card transistors are reversed biased; —14 v on the emitters and 0 v on the bases. The induced signal amplitude is not great enough to overcome this reverse bias.

### Selected Ready

The *start R/W* impulse should not be developed unless the selected access arm has the read-write head positioned at the desired location. This fact is determined by the *selected ready* line in the following manner.

Assume access 0 is to be used in module 0 (file No. 1). The selected access is ANDed with the selected module (75.23.11.1). The resultant *00 select* line is then ANDed with *access 0 ready* to produce *selected ready* (75.27.01.1).

*00 select* verifies that access 0 in module 0 has been selected. *Access 0 ready* verifies two facts; (1) the preceding seek instruction was initiated, (2) the arm is located at the desired address.

Two latches are employed in the development of *access 0 ready* (75.61.81.1). The latch at 3A is turned on at digit 3 time of a seek operation. It must be turned off before the latch at 4B can be turned on. Initiation of the seek operation is verified by *condition ready. Condition ready* then turns the latch at 3A off. The latch at 4B can now turn on when the access arm reaches the desired location; determined by the pick of the arrival relay (Figure 6-7).

### Control Counter

The control counter provides the basic cycle control for all file operations (75.32.11.1). It divides and defines the portions of a record (sector), to be written or read, into the following groups:

1. From the beginning of the selected record to the beginning of the indelible address (pre-indelible address AGC bits).
2. From the end of the indelible address to the beginning of the data field (pre-record AGC bits).
3. The length of the data field.

#### CONTROL COUNTER ADVANCE

The control counter (75.32.11.1) is initially reset by a + *X reset.* This reset is generated by the *file op* line during the instruction cycles.

During the pre-indelible address AGC bit time (pre, I.A.), the file clock is running. The phase Bs generated by the clock are gated by *AGC gate, read status,* and *not read gate* (4D-75.32.01.1) to produce the counter control advance pulses. The counter is advanced in this manner until it contains 36.

When the counter contains 36, the read gate latch is turned on (75.35.01.1). This permits the *read gate* to be available in time for the first significant I.A. bit. When the *read gate* is available, *not read gate* is inactive. Thus, the counter advance pulses are blocked

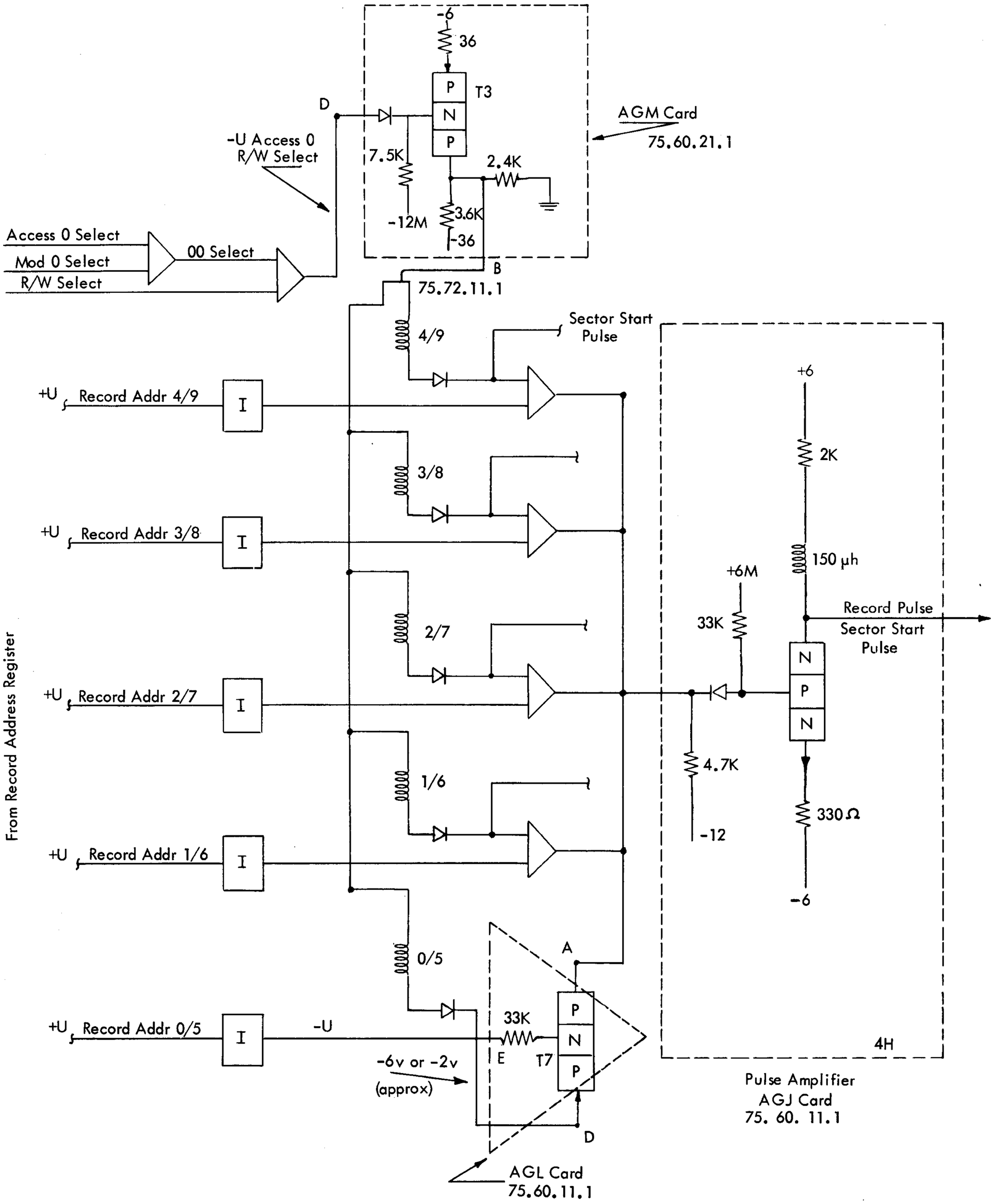



Figure 6-6. Record Head Selection and Record Pulse for Access 0, Module 0

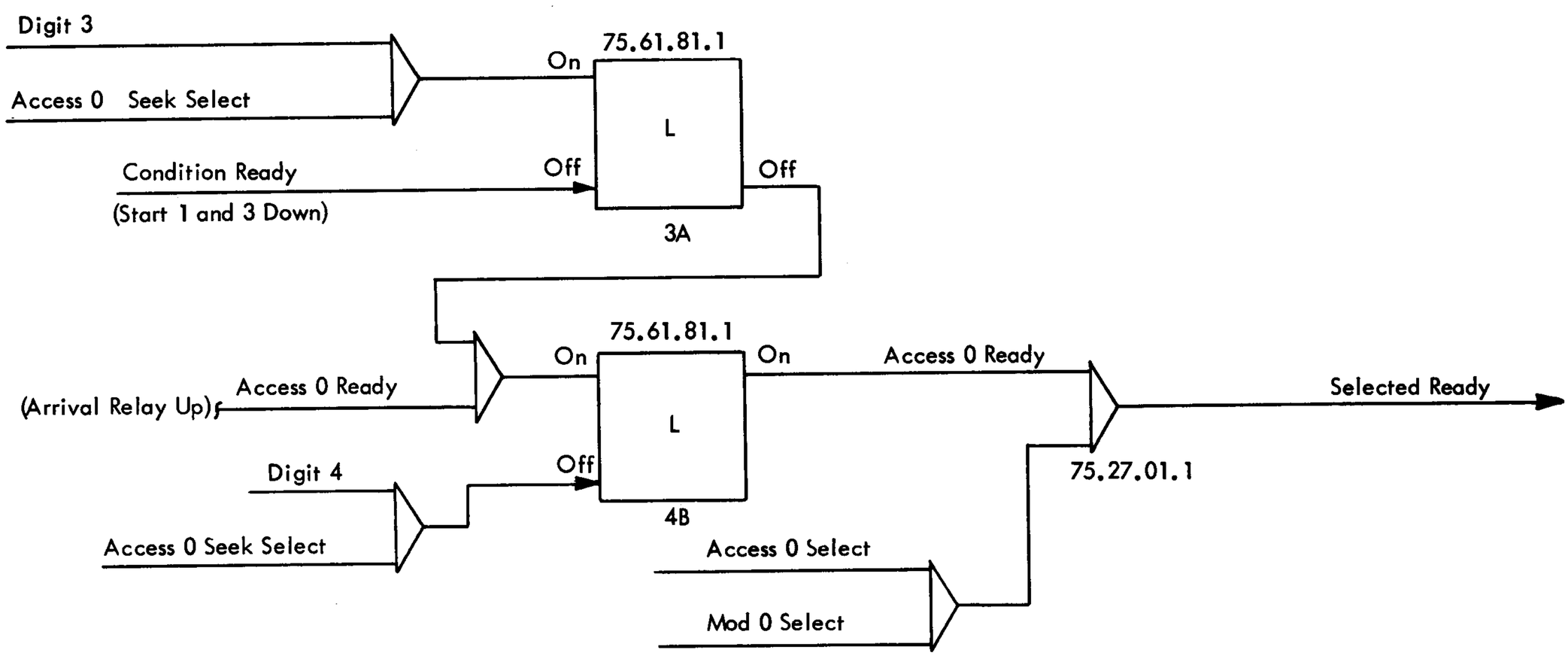



Figure 6-7. Selected Ready

by 4D. However, the counter must continue to count to provide the necessary controls during the remainder of this step. The phase B pulses are now gated by the output from 4F (75.32.01.1). The counter advances in this manner until it contains 48. The count 48 latch is then turned on (5G-75.32.21.1). When the count 48 latch is on, enough AGC bits have been read to properly set the gain of the read amp; the counter advance pulses are then blocked by 4F.

However, the counter must continue to advance until it contains 52. The absence of read data (AGC bits) provides these additional advance pulses (4H-75.32.21.1). When the counter contains 52, data has been absent for 4 bit times indicating that the read-write head is in the gap between the pre-I.A. AGC bits and the I.A. portion of the disk.

The *AGC gate* must now be dropped. *Count* 52 ANDS with *read gate* to turn the AGC gate latch off (4C-75.29.01.1). *Count* 52 is also used to turn the count 48 latch off (3H-75.32.21.1).

### *Read Indelible Address*

The basic objective of this step is to make a comparison between the IA characters recorded on the disk and the record address in core storage. If the two are not the same, the file operation is stopped and no address compare latch is turned on.

*Objectives:*

1. Advance bit ring.
2. Reset control counter.
3. Advance digit ring.
4. Establish compare gate.
5. Transfer IA characters to 1405 character register.
6. Transfer the IA characters to the 1401.
7. Drop compare gate.
8. End the IA step.

#### Bit Ring

The bit ring is used to define the bit times within a character time. It is an 8-position ring (SCBA8421) during a move operation and a 9-position ring (SWCBA8421) during a load operation. High speed CTDL negative input triggers make up the ring (75.33.11.1).

The ring is initially reset when the file op latch turns on, during the I-cycle step. The *not AGC gate* supplies another reset to ensure that the ring is reset just before it is used (75.38.11.1). The reset turns all triggers off.

The bit S trigger must be turned on at the very beginning of the I.A. step. It must then be advanced during the IA step to gate the I.A. characters into the 1405 character register.

The bit S trigger and the bit S latch are turned on by the leading edge ($\phi$A) of the first bit read from the disk after count 52; this will always be a bit S (4E-75.33.01.1). The ring is then advanced by each succeeding $\phi$A if the bit ring advance latch is ON (4B-75.33.01.1). The bit ring advance latch turns on with the first $\phi$D following the set of the bit S trigger (Figure 6-8).

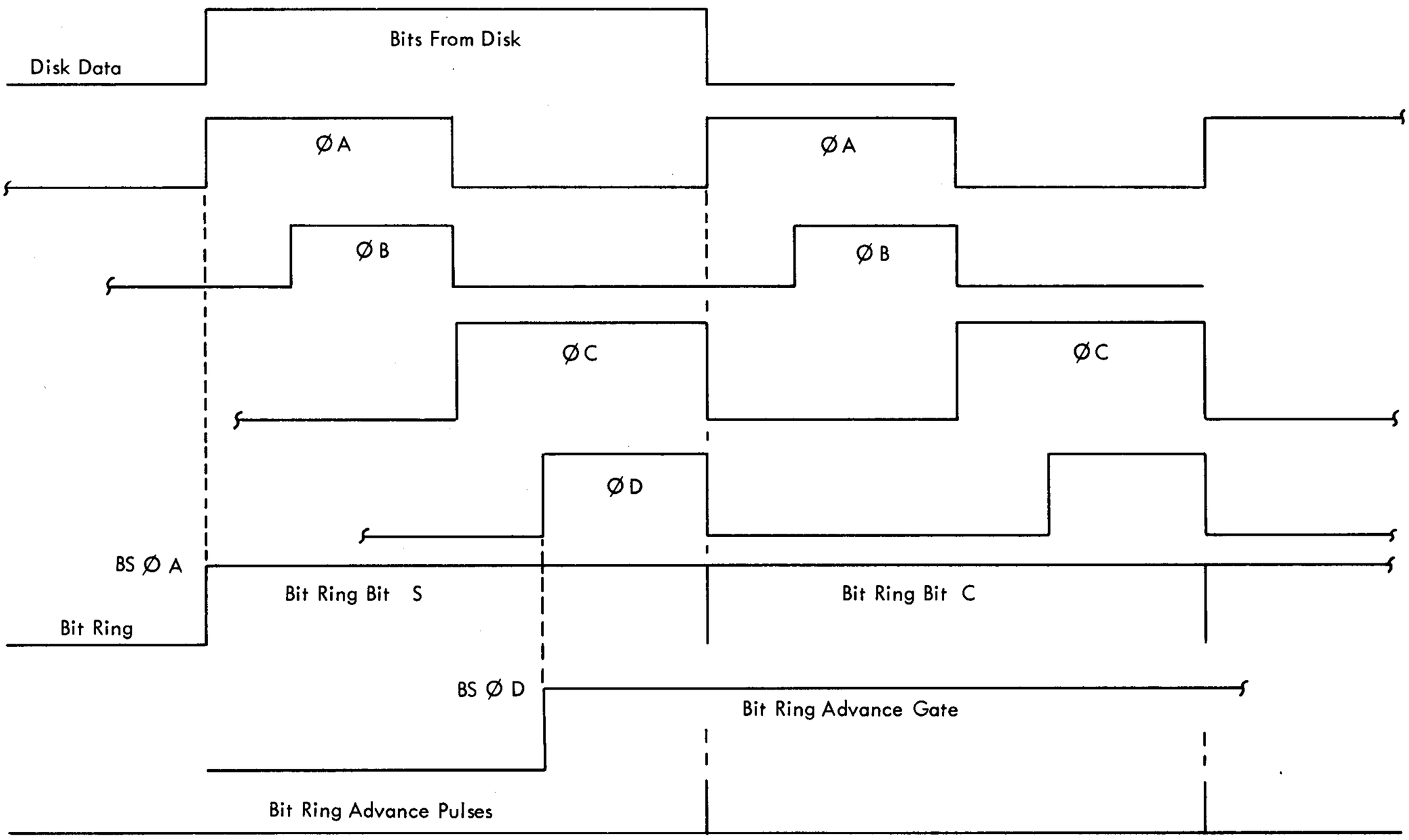



Figure 6-8. Bit Ring Advance

During the I.A. step, the WM bit trigger (4B-75.33.11.1) is never used. The set to 4B is blocked at 2B. The C bit trigger is set by the output from 2E during the I.A. step. Each succeeding trigger is then set when the preceding trigger goes off.

### Reset Control Counter

The control counter is not used during IA step. At the end of the pre-IA AGC step, the counter contained 52. It is reset with a bit S phase C delayed pulse if *not record gate* is high (4H-75.31.11.1).

It is important to remember that the bit ring was initially reset with all bit triggers off. Therefore, the control counter could not be reset until the bit S trigger turned on.

### Digit Ring Advance

The digit ring is again used to define the address characters. However, it must now be advanced at 1405 speed because the IA characters are being transmitted to the CPU.

The digit ring is advanced by each bit S that occurs while the *address gate* is up (2F-75.21.11.1).

The access character (digit 0) is not recorded on the disk as a part of the I.A. However, it does exist at the original BBB address in core storage so it must not be compared. Therefore, the first character compared is the module character (digit 1) found at address BBB plus one in core storage.

The first bit S that can occur to advance the digit ring is the bit S of the module character. The digit ring was reset to digit 0; it is therefore advanced to digit 1 by the bit S of the module character.

### Compare Gate

The compare gate latch is turned on at digit 1 time if not in a write address status and the *address gate* is up (4G-75.04.31.1). The *compare gate* remains up throughout the IA step. It provides for an automatic comparison between the contents of the A and B registers in the 1401.

### Transfer IA to Character Register

During digit 1 time, the module character bits are strobed into the character register by the bit ring (75.36.01.1). These arrive as *standard read data* from

75.31.11.1. The remaining IA characters enter the character register in a similar manner.

At the end of digit 1 time during the IA step, the following conditions exist:

1. The 1405 character register contains the module character.
2. The 1401 clock is stopped.
3. The compare gate is up.
4. The address of the module character is stored in the 1401 MAIN STAR.

### Transfer IA to 1401 A Register

START THE 1401 CLOCK

The 1401 clock must be started at digit 2 time to allow the module character to be compared. The 1401 clock turns on when the clock control latch is turned on (75.04.11.2). The latch is turned on by *+U data strobe.*

Data strobe for the I.A. step is developed on 75.31.11.1 at 4F. The requirements are *read data strobe gate* and B1$\phi$C. The read start gate latch turns on with the first bit C received after the *read gate* is up. The data strobe is, therefore, available at the end of digit 1 time (B1$\phi$C of the module character). A data strobe is then developed at each succeeding B1$\phi$C time.

The *data strobe* not only starts the 1401 clock but also gates the 1405 character register into the 1401 A register. Thus, during the first B cycle of the IA step, the module character from the IA enters the 1401 A register while the module character from cores enters the 1401 B register. The contents of the 1401 A and B registers are then compared.

The 1405 character register is reset at each BS$\phi$C during the time the read gate is up (75.36.01.1). The disk tens character is then strobed into the character register as the bit ring continues to advance.

STOP THE 1401 CLOCK

The 1401 clock must run at 1405 speed during the IA step. Therefore, only one B cycle is allowed per digit time.

The clock control latch is turned off at 060 to 090 time of each clock cycle if *extra cycle, sector gate,* and *not last character* are up (4D-75.04.11.2).In this manner, the clock is stopped each time after it is started throughout the IA step.

EXTRA CYCLE

An extra clock cycle is required by the 1401 after the compatibility character has been compared. This extra cycle reads the GMWM (stored in cores immediately following the compatibility character) to the 1401 B register and advances the B address to the first position reserved for the data record. This GMWM is not stored on the disk and therefore must not be compared.

The following objectives are required:

1. Turn extra cycle latch off.
2. Block reset of 1401 clock.
3. Drop compare gate.

*Turn Extra Cycle Latch Off.* The extra cycle latch (6E-75.04.51.2) is turned off when the inputs to the 4C are satisfied. The inputs required are *digit 0, compare gate, 030 to 060 time,* and *address gate.* All of these inputs are available at this time except *digit 0.*

The digit ring is advanced from digit 7 to digit 0 after the compatibility character has been strobed out to the 1401; the bit ring has not been reset and the *address gate* is up. Therefore, the extra cycle latch turns off at T030 to 060 during the B cycle used to compare the compatibility character. It turns on at T000 to 015 during the following B cycle.

*Block Reset of 1401 Clock.* The 1401 clock will continue running as long as the clock control latch is on (75.04.11.2). The extra cycle is provided by blocking the clock control reset from 4D. The output from 4D is blocked because the extra cycle latch turned off at T030 to 060.

### Drop Compare Gate

To prevent an attempt to compare the GMWM following the compatibility character, the compare gate must drop immediately following the comparison of the compatibility character. A circuit is available to reset the compare gate latch when the extra cycle latch turns off (75.04.31.2). The output from 3J resets the compare gate latch at 105 to 000 during the time the extra cycle latch is turned off.

### End of IA Step

The following objectives are required at the end of the IA step.

1. Reset the bit ring.
2. Turn off address latch.
3. Turn off read gate latch.
4. Bring up *Store A register.*

*Reset the Bit Ring.* The bit ring (75.33.11.1) is reset with all triggers OFF by *—U X reset* (75.38.11.1). This reset is developed from *read address reset* on 75.26.01.1 at 4D. The address reset latch (4D) is turned on at B4$\phi$C of digit 0 when the address gate is up resulting in a B4$\triangle\phi$C ($\triangle$=delayed) address reset pulse. The bit ring is therefore reset at B4$\triangle\phi$C time following the comparison of the compatibility character.

*Turn Off Address Latch.* The address latch (75.29.01.1) is turned off by the *—U X reset.* See objective one for the development of *—U X reset.*

*Turn Off Read Gate Latch.* The read gate latch (75.35.01.1) is turned off by *—U X reset* and *delayed phase C*. See objective one for *—U X reset* development.

*Store A Register. Store A register* is developed (4G-75.04.51.2) to allow the contents of the 1401 A register to be stored in cores. It brings up *transfer A register* within the 1401 and drops *transfer B register.*

The following conditions are required for this development: *Sector gate, read file, not gated address gate, not wrong length record, not write check, not 2nd GMWM.*

## Read Pre-Record AGC Bits

The basic objective of this step is to set the gain of the read amplifier. With the gain set, the data-record can be properly read (see READ AMPLIFIER). In addition to the basic objective, conditions are set up during this step to allow the data-record to be read and transmitted to the CPU.

The following circuit objectives are required:

1. Develop AGC gate.
2. Develop read gate.
3. Reset AGC gate latch.

### AGC Gate

The AGC gate latch (75.29.01.1) again functions with the control counter to define the portions of the sector that contain AGC bits; in this instance, the pre-record AGC bits.

The latch is turned on by *read address reset* (75.26.01.1) and *phase C delayed. Read address reset* (previously developed) is B4$\triangle\phi$C of digit 0 when the address gate is up. Therefore, the AGC latch turns on at B4 delayed $\phi$C of digit zero following the comparison of the compatibility character.

### Read Gate

The read gate latch (75.35.01.1) is turned on to allow the intake of data from the read amplifier. The conditions required are *read status, AGC gate,* and *count 36.* It remains on until the end of the read operation.

The control counter (75.32.21.01) is reset by *read address reset.* It is then advanced to 36 in the same manner as described under the pre-I.A. AGC step.

### Reset AGC Gate Latch

The control counter advances beyond 36 as described under the pre-I.A. AGC step. When the counter reaches 48 the count 48 latch is again turned on (5G-75.32.21.1). When the count 48 latch is ON, the counter is advanced by the absence of read data until it contains 52. At this point, data has been absent for 4 bit times indicating that the read-write head is located in the gap between the record AGC bits and the data record.

The AGC gate latch (75.29.01.1) is then turned off by *read gate,* and *count 52. Count 52* also turns the count 48 gate latch off.

## Data Record Step

The basic objective of this step is to read and transmit the data-record (200 characters) to the 1401. This step and the I.A. step are quite similar in operation.

To accomplish the data-record step, the following objectives are developed:

1. Advance the control counter.
2. Advance the bit ring.
3. Develop *record gate.*
4. Control the 1401 clock.
5. Transmit read data to 1401 A register and Store A register.
6. End the operation.

### Advance the Control Counter

The control counter is reset following the pre-record AGC step by *set bit ring* S, if not in a write address status (4J-75.31.11.1).

*Set bit ring* S is developed when the set bit S latch is turned on. The latch is turned on at the end of the pre-record AGC step when the counter contains 52 (75.33.01.1). Refer to the read I.A. step.

The counter is used, during this portion of the operation, to count the number of data-characters read. Therefore, it is advanced once at the end of each character time.

The counter advance pulses are generated on 75.32.01.1. The *bit ring advance gate* is sampled at bit one time at 3B. This output is then ANDed with $\phi$B to produce the counter advance pulses (B1$\phi$B).

The *bit ring advance gate* is turned on at BS$\phi$D time (75.33.01.1); the bit S from the first character position on the data-record portion of the disk.

### Advance the Bit Ring

The bit ring is advanced with each succeeding phase A once the bit ring advance latch is on and the bit S trigger has been set (75.33.11.1).

The bit ring gates the read data into the 1405 character register, serially by bit.

### Record Gate

The *record gate* is used to define the data-record portion of the disk (75.32.01.1). It is a combination of *bit ring advance gate* and *not address gate.* An examination of the bit ring advance latch (75.33.01.1), shows that, once on, it remains on until the end of the operation.

Therefore, the *record gate* is available for 200 characters during the data-record portion of the operation.

### Clock Control

During the data-record step the 1401 clock must run at 1405 speed; one B cycle per 1405 character time. The 1401 clock must not start until the entire character has entered the character register. Read data enters the character register serially by bit. Therefore, the 1401 clock is started at each B1$\phi$C time following the first character (75.04.11.2).

The *data strobe*, required to start the clock, is developed in the same way as described for the I.A. step. Again, the read start gate latch turns on with the first bit C received after the *read gate* is up. The first *data strobe* is then available during B1$\phi$C of the first character. A *data strobe* is then developed by each succeeding B1$\phi$C.

The clock control latch must be turned off before the next clock cycle begins. The output from 4D provides the reset as described in the I.A. step.

### Transmit Read Data

The output from the 1405 character register (75.36.01.1) is transmitted to the 1401 and is gated into the A register by the same B1$\phi$C *data strobes* that are used to turn the clock control latch on.

*Transfer A register*, within the 1401, is then developed by the interconnecting line, *store A register*. This allows the contents of the A register to enter the addressed position of core storage.

*Store A register* (4G-75.04.51.1) comes up when the *address gate* falls. The other conditioning factors at 4G prevent the storage of unusable data. *Store A register* normally remains up until the second GMWM is encountered in core storage.

### End the Read Operation

The end of the read operation is determined by the control counter. During the data-record step the counter advances one for each character time. When it contains 200 (B1$\phi$B of last character), the end record latch is turned on (6D-75.32.31.1).

The resultant end record gate line is ANDed with BS$\phi$C (4B-75.35.01.1) to turn the read gate latch off. This occurs at BS$\phi$C of the 201st character.

The *end record gate* also functions with BA$\phi$C to generate a 2.5 $\mu$s *R/W end op* impulse (4G-75.38.01.1). This 2.5 $\mu$s impulse then becomes the X and Z resets (75.38.11.1). *R/W end op* also develops *end op* on 75.38.01.1. *End op* then becomes the W resets on 75.02.41.1 and it also brings up *CPU end op*.

The *X and Z resets* reset the following latches and triggers: AGC, count 48, read gate, end of record, character register, write AGC, bit ring advance, control counter, bit ring, and read start gate.

The *W resets* reset the following latches: address transfer, A for B substitute, first address transfer cycle, clock control (reset on), sector gate, and first write cycle.

The *CPU end op* turns the last character latch on. This allows the end execute line to stay up until the next I op time.

## Read Single Record — Load Op (L%F1BBBR)

The purpose of this instruction is to allow the 1405 to read data from the file that contains WM's. The data flow is the same as the data flow during a move op. However, *end op* is generated after 176 characters instead of 200. This difference is due to the space required during a load op by the recording bit configuration of SWCBA8421.

The following two circuits require additional controls to allow the 1405 to accomplish this instruction:

1. Bit ring.
2. Control counter decode.

### Bit Ring Operation

The bit ring must provide a bit time for the WM (SWCBA8421) during the data-record step. However, it must not include this bit time during the I.A. step (I.A. is always recorded in an SCBA8421 configuration).

During the I.A. step, the *address gate* is up. When the bit ring advance pulse turns the bit S trigger off, (75.33.11.1) pin F (4A) goes to —T. This output is then gated through 2E and turns the C bit trigger on. The WM trigger is bypassed because the inputs at 2B are not satisfied when the *record gate* is down. Thus, the bit ring advances in the 8-bit mode (SCBA8421) during the I.A. step.

During the data-record step, the *address gate* is down and the *record gate* is up. When the bit S trigger turns off, pin F (4A) is gated through 2B and WM trigger is turned on. The next advance pulse turns the WM trigger off. The C bit trigger is then turned on through 2D. Thus, the ring advances in the 9-bit mode (SWCBA8421) during the data-record step.

### Control Counter Decode

The control counter advances as previously explained under READ SINGLE RECORD move op. However, the end-of-record latch must be set at count 176 instead of count 200.

A decode of count 176 is provided at 5B when the —T load op line is active. Thus the end-of-record latch is set at count 176 during a load op.

# Section 7 Write Single Record Operation (1405-1401)

A write single record operation is called for by the instruction M%F1BBBW. The operation is performed during the following sequential steps.

1. 1401 instruction cycles.
2. Address transfer.
3. Read pre-indelible address AGC bits.
4. Read indelible address.
5. Write pre-record AGC bits.
6. Write data record.

Figure 6-1 contains a block diagram showing the basic data flow during a read, write, or seek operation. This diagram along with the sequence charts (Figures 6-2 and 7-1) and the data flow diagram (Figure 7-2) are provided to supplement the explanation of the write operation.

A great deal of the write single record operation is identical to the READ SINGLE RECORD operation. Therefore, comparisons are made to the steps performed during the read operation; differences are then explained.

Address transfer, pre-I.A. AGC, and the read I.A. steps are identical for both the read and write operations. Refer to the READ SINGLE RECORD operation for an explanation of these steps.

## 1401 Instruction Cycles

The objectives during this step are identical to those of step one for READ SINGLE RECORD, with one exception. The write file latch must be turned on in place of the read file latch.

### Write File Latch

The write file latch turns on at T060 to 090 during I-ring 7 if the instruction contains a W and the *gated file op* line is up (75.02.31.2). Its output is gated by the single record latch (75.02.51.2) and is subsequently used to turn on the write gate latch. *Gated file op* is developed by ANDing *file op* and *not write check interlock* (75.01.42.2).

#### WRITE CHECK INTERLOCK LATCH

The purpose of this latch is to prevent any file operation, following a file write operation, except a write check operation. Therefore, data that is written on the disks must always be compared with the original data in core storage. The write check operation is not automatic; it must be programmed.

Assume that the write check interlock latch is off (start reset) and a write file instruction is initiated. The *gated file op* line is then developed and the write file latch (75.02.31.1) turns on. The write operation is then initiated.

During the write operation when the record gate comes up, the write check interlock latch is turned on (75.04.51.1). *Gated file op* is then dropped. As *gated file op* is required to initiate all file operations except write check, the write check interlock latch must be reset before the next file instruction can be executed. The *record gate* is used as a conditioning factor in the set of the write check interlock latch because it is necessary to prove that there was an address compare before the interlock is set.

The write check instruction (M%F3BBB) controls the reset of the write check interlock latch. A decode of three from the write check instruction is detected during I-ring-3 time and the write check latch is turned on (75.02.21.1). The output is ANDed with *start R/W* to reset the write check interlock latch. The next file instruction can now be executed.

## Write Pre-Record AGC Bits

During a write operation the pre-record AGC bits are always rewritten. The amplitude of the AGC bits and the data-record bits should then be the same; they are written with the same head and at approximately the same time.

The gain of the read amplifier is established by the AGC bits. Because the amplitude of the data-record bits is a reflection of the AGC bits, the gain of the read amplifier is properly set for reading during the data-record step.

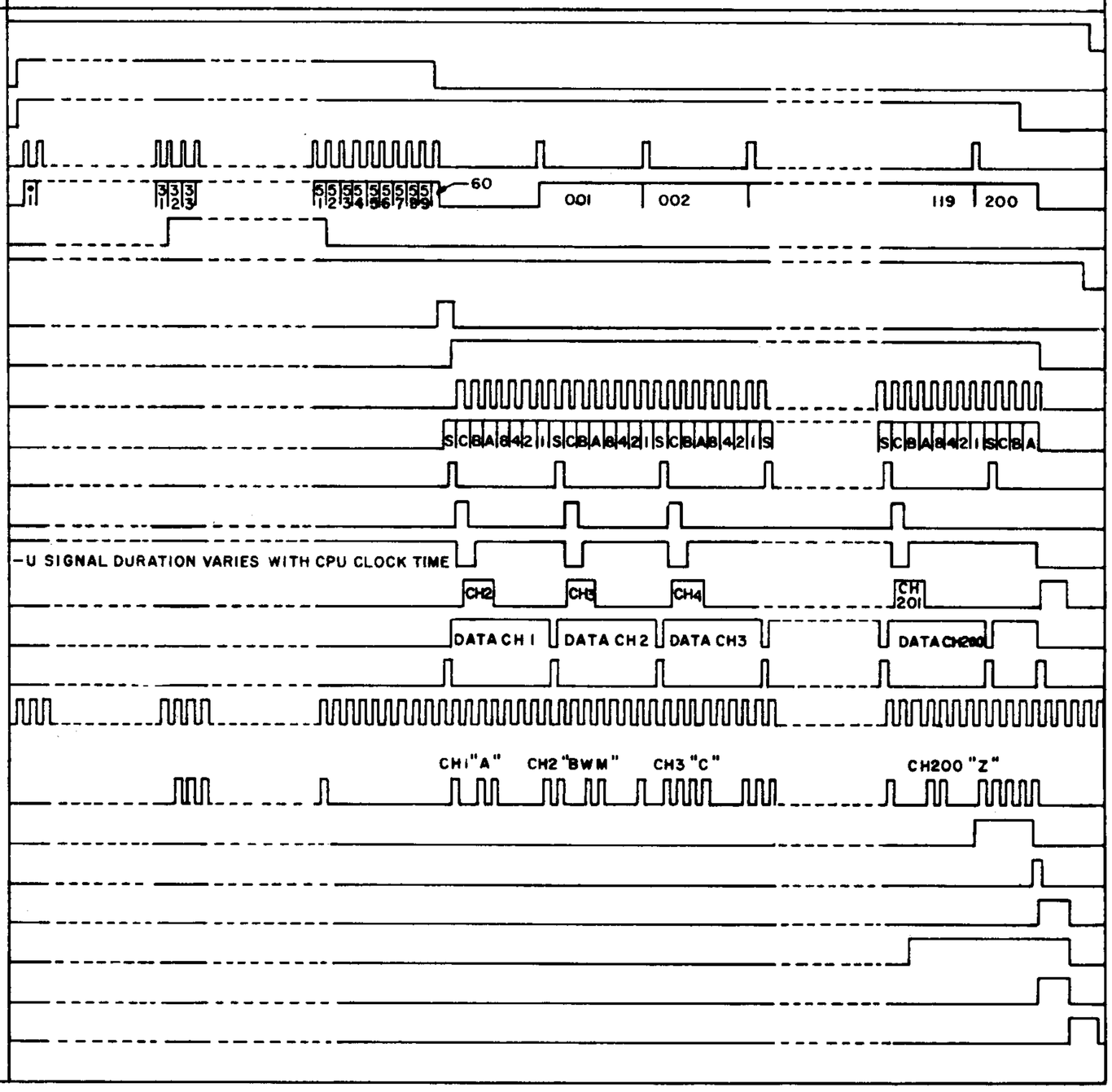
*Objectives*

1. Develop first write cycle.
2. Develop AGC gate.
3. Advance control counter.
4. Develop write gate.
5. Develop write AGC gate.

### First Write Cycle

At the end of the I.A. step, three B cycles are taken. The first compares the compatibility character, the second reads the GMWM out of cores (not compared), the third reads the first character to be written out of cores to the 1401 B register. The purpose of the first write cycle latch, is to provide a reset to the clock control latch during the third B cycle.

| LINE TITLE | LOGIC | TEST POINT |
|---|---|---|
| | (FROM 1401) | (1405) |
| –T MOVE OPR | 75.01.2 1.2 | 01A1E26C |
| –T AGC GATE | 75.29.01.1 | 01A2G14E |
| –T WRITE GATE | 75.34.01.1 | 01A2F10B |
| –U CTRL CNTR ADV PULSE | 75.32.01.1 | 01A2F19F |
| CONTROL COUNTER | 75.32.1 1.1 | ——— |
| –T WRITE AGC LT | 75.34.01.1 | 01A2H05E |
| +U WRITE RECORD | 75.02.512 | 01A1B25N |
| –T SET BS LATCH | 75.33.01.1 | 01A2C25H |
| –T BIT RING ADV GATE | 75.33.01.1 | 01A2C25E |
| –T BIT RING ADV PULSES | 75.33.01.1 | 01A2C07F |
| BIT RING | 75.33.1 1.1 | ——— |
| –T ADDR OR WR STROBE | 75.33.1 1.1 | 01A2B24A |
| –T DATA STROBE | 75.31.1 1.1 | 01A2G10N |
| +U NOT FILE CLOCK CONTROL | 75.04.1 1.2 | 01A1C04P |
| 1401 B CYCLES | ——— | ——— |
| CHARACTER REGISTER | 75.36.__ | ——— |
| +T CHAR REG RESET | 75.36.01.1 | 01A2F10A |
| –T PHASE C | 75.31.0 1.1 | 01A2A18G |
| (MOD Ø SELECT) | | |
| +U WRITE DATA | 75.34.1 1.1 | 01A2F06N |
| –T END RECORD GATE | 75.32.31.1 | 01A2G21E |
| –T R W END OP | 75.38.01.1 | 01A2G21H |
| –T LAST CHARACTER | 75.04.41.2 | 01A1C21N |
| –T SECOND GM WM | 75.03.21.2 | 01A1D21N |
| +U END EXECUTE | 75.04.41.2 | 01A1E22B |
| +U I RING OP | ——— | (1405) 01A1D02B |




NOTE:
ALL SIGNALS ARE SHOWN UP FOR THE ACTIVE STATE

Figure 7-1. Write Record — After Indelible Address Time

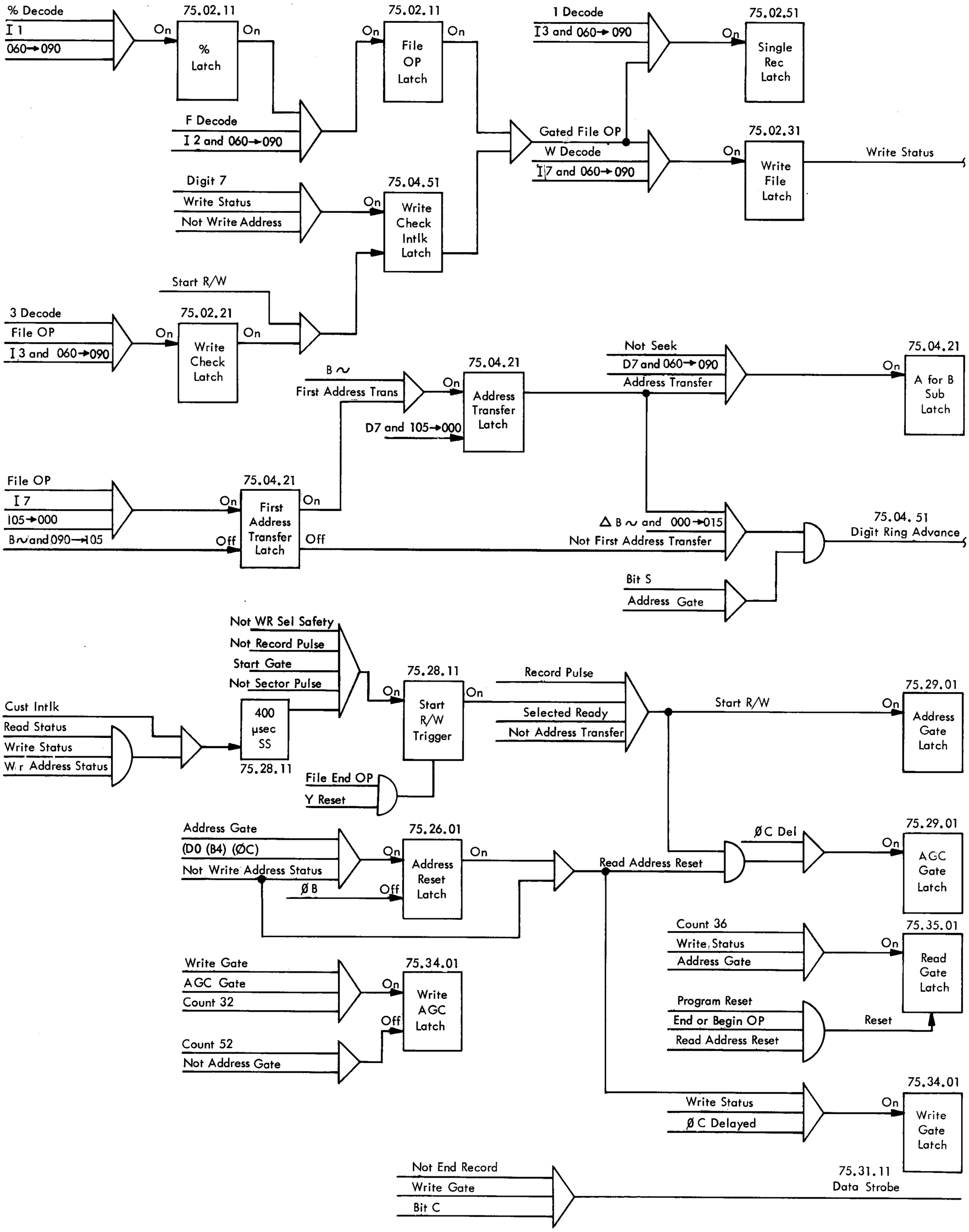



Figure 7-2. Write Single Record Operation

The latch is turned on at 090-105 during the second B cycle (end of I.A. step) if the *address gate* is up and the write file latch is on (75.04.31.2). It is reset at T060 to 090 during the third B cycle (Figure 7-3).

The reset to the clock control latch is blocked during the second B cycle by the first GMWM (2E-75.04.11.1). During the third B cycle, the reset is available at 030 to 060 time from 4H.

### AGC Gate

The *AGC gate* is used, at this time, to define the portion of the sector that is to be written with AGC bits. The AGC latch is turned on by *$\phi$C delayed* and *read address reset*. *Read address reset* (75.26.01.1) is up at B4$\triangle\phi$C ($\triangle$ = delayed) of digit zero during address gate time. *Read address reset* develops the *X reset* lines to reset the bit ring, address gate latch, control counter, and read gate latch.

### Control Counter

The control counter, at this time, operates in conjunction with the *AGC gate* to define the portion of the sector to be written with AGC bits.

With the *address gate* down, and the *AGC gate* up the counter advances with each $\phi$B impulse (4A, 6E-75.32.01.1). When it contains 60, the AGC latch is turned off (75.29.01.1) blocking any further counter advance pulses (4A-75.32.01.1). The counter is reset at the beginning of the data-record step when the set bit S latch turns on (4J-75.34.01.1).

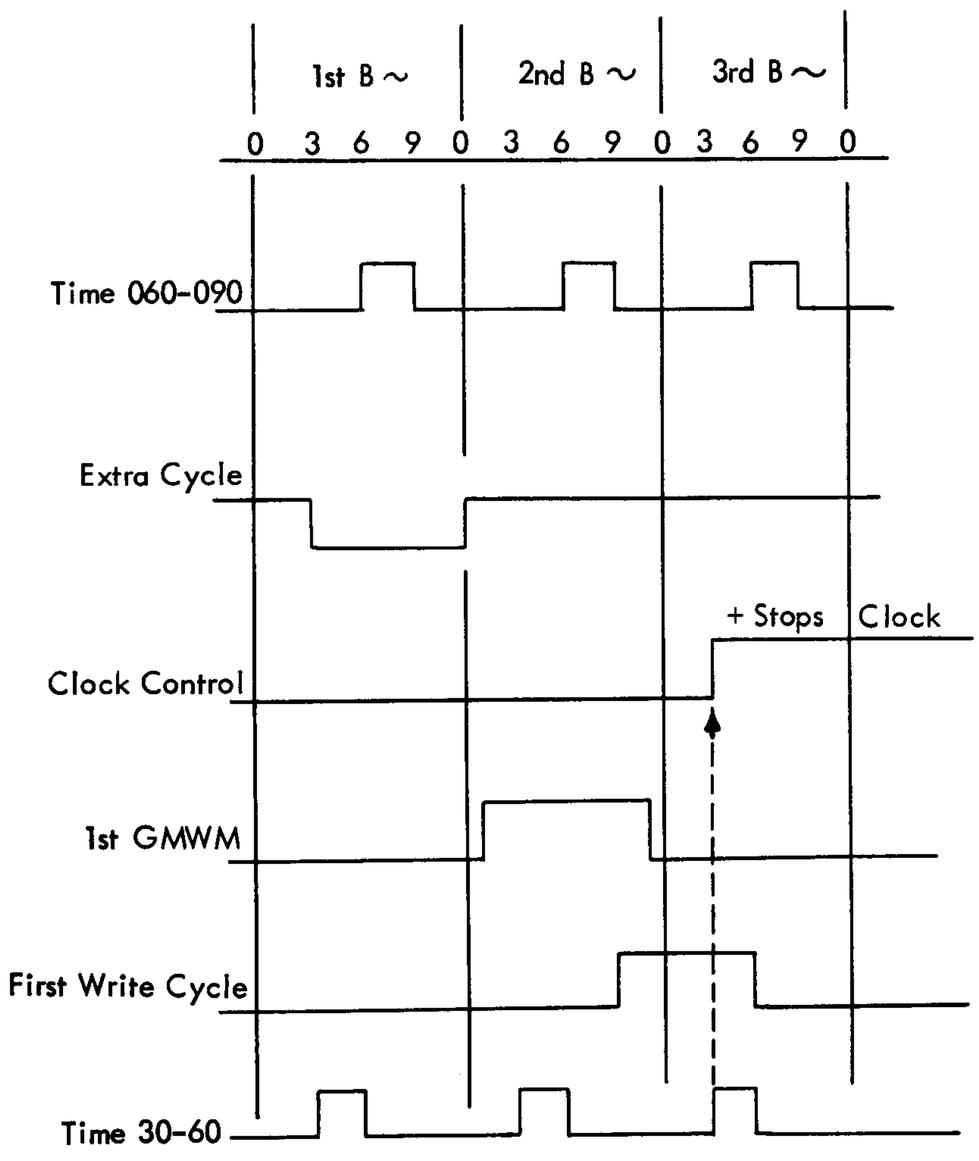



Figure 7-3. Clock Control – First Write Cycle

### Write Gate

The write gate (75.34.01.1) conditions the write amplifier (75.61.61.1) to allow the selected read-write head to draw write current (see BASIC READ WRITE CIRCUITS).

The write gate latch is turned on by *read address reset* and delayed $\phi$C. Therefore, the *write gate* is up at B4$\triangle\phi$C during the third B cycle. The latch remains on until the last character is written during the data-record step.

### Write AGC Latch

The write AGC latch (75.34.01.1) is used to bring up the *write data* line. The *write data line* then gates $\phi$C to the write amplifier (75.34.11.1). A series of $\phi$C impulses are then recorded on the disk during the time the write AGC latch is on.

The latch is turned on by *count* 32 if the *write gate* and the *AGC gate* are up (3C). It is turned off at count 52 (4A). Therefore, during the time the write AGC latch is on, 20 AGC bits are written.

## *Write Data Record*

The first character to be written on the data-record portion of the sector is stored in the 1401 B register. (Entered B register during the third B cycle of the pre-record AGC step.) This character must be transmitted to the 1405 character register where it is "serialized" by the bit ring to become write data.

The 1401 B cycles must be initiated at the beginning of each 1405 character time to enter the succeeding write character into the 1401 B register. This character must then be transmitted to the 1405 character register where it is "serialized" and becomes write data. Each succeeding character is handled in the same manner.

*Objectives*

1. Set and advance the bit ring.
2. Reset and advance the control counter.
3. Develop the record gate.
4. Develop write data.
5. Control the 1401 clock.
6. End the operation.

### Set and Advance the Bit Ring

The bit ring is used to "serialize" the 1405 character register output. The ring must, therefore, be allowed to run throughout the data-record step.

The set bit S latch is turned on at count 60 with *delayed $\phi$C* (2H-75.33.01.1). The bit ring advance gate then comes up at BS$\phi$D. Phase As are gated by the *bit ring advance gate* and become the *bit ring advance pulses*. Therefore, the first advance pulse occurs at BC$\phi$A and turns the bit C trigger on. The ring continues to advance with each succeeding $\phi$A.

### Reset and Advance the Control Counter

The control counter is reset when the set bit S latch turns on (4J-75.31.11.1). It is then advanced, once each character time (B1$\phi$B), to count the number of characters written (3B-75.32.01.1).

### Record Gate

The *record gate* identifies the portion of the sector reserved for the customer's record. It comes up with the *bit ring advance gate* (2B) and remains up until the bit ring advance latch is turned off by *end op* (2B-75.32.01.1).

### Write Data

The first character to be written enters the 1405 character register (75.36.01.1) from the CPU when a *write strobe* is developed at BS$\phi$C time (4C-75.31.11.1).

When the bit ring strobes the output from the character register, serial data is placed on the write-data line. Bit Ss are then inserted from 5H (75.34.01.1). The resultant write data line is then ANDed with the *write gate* (5E-75.34.01.1). *Write data,* as an output from 5D, is then ANDed with the selected module and is strobed by $\phi$Cs (3A-75.34.11.1). The resultant $\phi$C *write data* is then available as an input to the write amplifier (75.61.61.1).

### 1401 Clock Control

During the time the first character is being recorded on the disk, a B cycle must be initiated to enter the second write character into the 1401 B register.

The *data strobe*, used to turn the clock control trigger on, is developed at each bit-C time while the *write gate* is up (4D-75.31.11.1). The clock control latch is then reset at T060 to 090 during the B cycle. Thus, one B cycle is taken each character time.

In summary, each character to be written (except the first) enters the 1401 B register at 1405 bit-C time. It is then transmitted to the 1405 character register at BS$\phi$C time and is immediately "serialized" beginning at BC$\phi$A time.

### End the Operation

The write operation is ended in the same manner as the read operation. X, W, and Z resets are developed after the control counter reaches 200.

The write gate latch is turned off at BS$\phi$B time of the 201st character (5J-75.34.01.1). In case this circuit fails, a reset is also available when the write gate safety latch turns off. The latter circuit is available when a sector pulse indicates the beginning of the next disk sector. Thus, the risk of accidently erasing records is diminished.

The last character latch is turned on by *end op* thereby generating *end execute*. *End execute* ANDs with B cycle to cause a 1401 I.E. change.

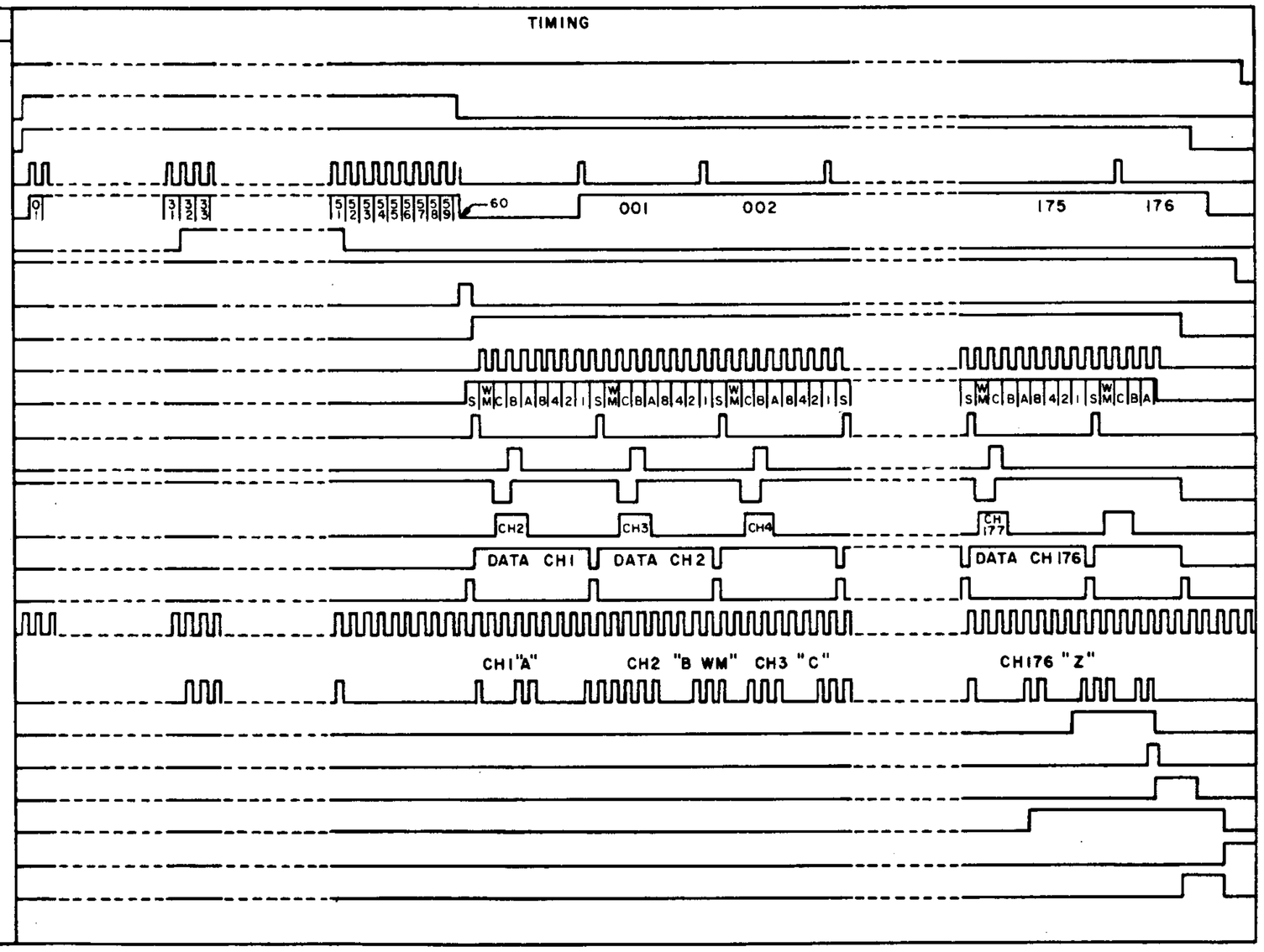
## Write Single Record — Load Op (L%F1BBBW)

The purpose of this instruction is to allow the 1405 to record WM's on the disks when WM's are encountered along with the write data. The functional objectives are the same as required for WRITE SINGLE RECORD MOVE OP. However, *end op* is generated after 176 characters have been written instead of 200. This difference is because of the space required by the recording bit configuration of SWCBA8421 during a load op.

Two circuits require additional controls to allow the 1405 to accomplish this objective. They are the bit ring and the control counter decode circuits.

These additional controls are discussed under READ SINGLE RECORD LOAD OPERATION in Section 6. (See Figure 7-4).

| LINE TITLE | LOGIC | TEST POINT |
|---|---|---|
| -T LOAD OPR | (FROM 1401) 75.01.42.2 | (1405) 01A1B28N |
| -T AGC GATE | 75.29.01.1 | 01A2G14E |
| -T WRITE GATE | 75.34.01.1 | 01A2F10B |
| +U CTRL CNTR ADV PULSE | 75.32.01.1 | 01A2F19F |
| CONTROL COUNTER | 75.32.11.1 | ——— |
| -T WRITE AGC LT | 75.34.01.1 | 01A2H05E |
| +U WRITE RECORD | 75.02.51.2 | 01A1B25N |
| -T SET BS LATCH | 75.33.01.1 | 01A2C25H |
| -T BIT RING ADV GATE | 75.33.01.1 | 01A2C25E |
| -T BIT RING ADV PULSES | 75.33.01.1 | 01A2C07F |
| BIT RING | 75.33.11.1 | ——— |
| -T ADDR OR WR STROBE | 75.31.11.1 | 01A2B24A |
| -T DATA STROBE | 75.31.11.1 | 01A2G10N |
| +U NOT FILE CLOCK CONTROL | 75.04.11.2 | 01A1C04P |
| 1401 B CYCLES | ——— | ——— |
| CHARACTER REGISTER | 75.36.--- | ——— |
| +T CHAR REG RESET | 75.36.01.1 | 01A2F10A |
| -T PHASE C | 75.31.01.1 | 01A2A18G |
| (MOD 0 SELECT) +U WRITE DATA | 75.34.11.1 | 01A2F06N |
| -T END RECORD GATE | 75.32.31.1 | 01A2G21E |
| -T RW END OP | 75.38.01.1 | 01A2G21H |
| -T LAST CHARACTER | 75.04.41.2 | 01A1C21N |
| -T SECOND GM WM | 75.03.21.2 | 01A1D21N |
| +U I RING OP | (FROM 1401) 75.01.41.2 | (1405) 01A1D02B |
| +U END EXECUTE | 75.04.41.2 | 01A1E22B |




NOTE: ALL SIGNALS ARE SHOWN UP FOR THE ACTIVE STATE.

Figure 7-4. Write Record, Load Operation — After Indelible Address Time

The functional objectives for read full track or write full track are the same. For this explanation, assume that a read full track operation is called for (M%F2-BBBR).

The instruction calls for 1000 characters to be read from five records on the same track. The five records must be read from the same side of the disk. Reading may begin at any one of the five records (0 through 4 or 5 through 9); the next four records are then read in order.

The data flow and basic objectives are the same as those required for a R/W single record operation. However, the indelible address of the first record (selected record) is the only one compared.

To accomplish a full track operation the following objectives are set forth.

1. Establish a full track operation.
2. Transfer only the first record address (AMDD-TTR0).
3. Develop start R/W for each of the five records.
4. End the operation after 200 characters of the fifth record.

### Establish Full Track Operation

A decode of 2 during I-ring 3 ANDs with *gated file op* and turns the full track latch on (75.02.51.1). *Write full track* is then available at 6E.

*Track status* is then available from 2G (75.20.01.1). *Track status* indicates that a five-record transfer has been called for by the instruction.

### Transfer Only First Record Address

The first record address is transferred and compared in the normal manner (see R/W SINGLE RECORD op).

When the last character of the first record has been read, *end op* is generated (75.38.01.1) and the X and Y reset lines are activated. *CPU end op,* however, is blocked at 4D preventing an I.E. change (75.01.61.2). The 1401 clock is therefore stopped after character 200 of the first record. The 1401 I-cycle steps and the address transfer steps are by-passed during the remainder of the operation (Figure 8-1).

### Develop Start R/W for Each of the Five Records

Start R/W for the first record is developed in the normal manner. That is, the start R/W trigger turns on from 5A (75.28.11.1) when the 400 μsec single shot times out. The first record pulse that occurs from the selected record is then gated through 6C to develop the first *start R/W* pulse. The first record is then handled in the manner described for SINGLE RECORD.

The second record is identified by the first sector pulse following the selected record pulse. As long as the start R/W trigger is on, each sector pulse in turn develops a start R/W pulse through 6C. The start R/W trigger remains on until *file end op* is generated for the fifth record. (The development of *file end op* is covered later.)

The record address of the first record remains in the select register throughout the operation. Therefore, the indelible address comparison must be suspended for each of the four records following the first record. This is accomplished by preventing the development of the compare gate during the IA portion of the last four records. In addition, the development of data strobes is prevented during the IA portion of the last four records. The latter condition prevents the initiation of 1401 B cycles during the IA portion of the last four records.

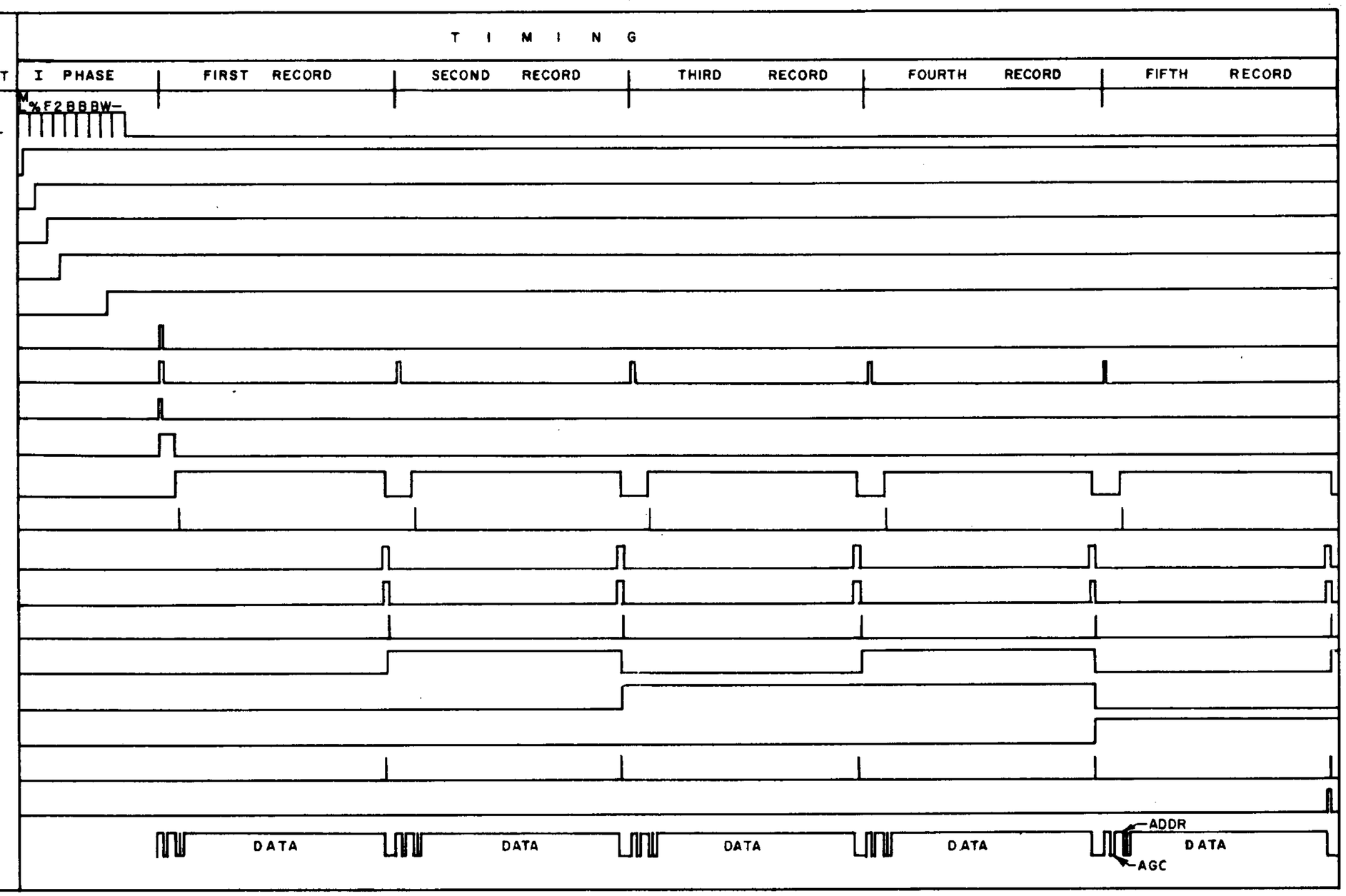
The set to the compare gate latch is blocked by *gated address gate* at 4G (75.04.31.2). *Gated address gate* is not developed for the last four records of a full track operation (3H-75.01.71.2); its development is prevented when the record counter contains one or more. Data strobes are also prevented when the record counter contains one or more (2H-75.31.11.1).

The record counter is a binary counter that is reset with all triggers off. At the end of each record, during a full track operation, the counter is advanced 2.4 μs after BAϕC of the 201st character by R/W end op delayed (2G-75.28.11.1).

### End the Operation

The *R/W end op* generated at the end of the fifth record (75.38.01.1) should bring up *CPU end op* to cause an I.E. change. This is accomplished indirectly at 4C (75.38.01.1) by *track end op*. When the R/W end op trigger is turned on, the *track end op gate* is immediately available to gate the outputs from counters one and four (6H-75.28.11.1). The counter is advanced, from four to five, 2.5 μs later by *R/W end op*. The resultant output, *track end op,* ANDs with *track* status to bring up *CPU end op* (4C-75.38.01.1).

| LINE TITLE | LOGIC | TEST POINT |
|---|---|---|
| I PHASE | | |
| -T LOAD OPR | (FROM 1401) 75.01.42.2 | (1405) 01A1B28N |
| -T FILE % LATCH | (1401) 75.01.04.2 | (1401) 02A8E09N |
| +U FILE OP | (1401) 75.01.04.2 | (1405) 01A1E23AP |
| -T FULL TRACK LATCH | 75.02.51.2 | 01A1B15A |
| -T WRITE FILE | 75.02.31.2 | 01A1B24B |
| -T RECORD PULSE | 75.28.01.1 | 01A2J27G |
| -T SECTOR PULSE | 75.28.01.1 | 01A2J04C |
| -T START RD WR | 75.28.11.1 | 01A2G06G |
| -T ADDR GATE | 75.29.01.1 | 01A2F10H |
| -T WRITE GATE | 75.34.01.1 | 01A2F10B |
| -T WR AGC LT | 75.34.01.1 | 01A2H05E |
| +U CONTROL COUNTER 176 LOAD OPERATION 200 MOVE OPERATION | 75.32.31.1 | 01A2J26N |
| -T END RECORD GATE | 75.32.31.1 | 01A2G21E |
| -T RW END OP | 75.38.01.1 | 01A2G21H |
| +U REC CNTR 1 | 75.28.11.1 | 01A2J05H |
| +U REC CNTR 2 | 75.28.11.1 | 01A2F09H |
| +U REC CNTR 4 | 75.28.11.1 | 01A2K02H |
| -T TRK END OP GATE | 75.38.01.1 | 01A2G21H |
| -T TRK END OP | 75.28.11.1 | 01A2J19G |
| TRACK LAYOUT | | |




NOTE: ALL SIGNALS ARE SHOWN UP FOR THE ACTIVE STATE

Figure 8-1. Write Full Track

# Section 9 Write Check Operation (1405-1401)

The basic objective of this operation is to cause the data-record portion of a sector to be compared, character by character, with the data in core storage from which it was written.

As previously explained, a write check operation must follow a write operation. No other file operation can be executed until the write check operation is performed. The operation is initiated by the instruction M%F3BBB, if the data was written in the move mode. If the data was written in the load mode, the operation is initiated by the instruction L%F3BBB. In either case, the BBB portion of the instruction must be the original core address of the recorded data.

The instruction is performed using the same steps as described for READ SINGLE RECORD OP. However, instead of storing the information read during the data-record step in cores, it is merely compared. Refer to Figure 9-1.

The following objectives modify the READ SINGLE RECORD operation to allow the execution of the write check instruction:

1. Turn on read file latch.
2. Provide compare gate during the data-record step.
3. Prevent storage of the 1401 A register.

### Read File Latch

As *gated file op* is not available following a write instruction, the read file latch is turned on by *write check* during a write check instruction (4D, 5D-75.02.31.2).

The write check latch is turned on by a decode of three during I-ring 3 (3F-75.02.21.1).

Note also, that *write check status* gates *start read write* to turn off the write check interlock latch (2F-75.04.51.2). This serves to release the file interlock condition so that succeeding file instructions may be executed.

### Compare Gate (75.04.31.2)

The compare gate latch is reset when the extra cycle latch is turned off at the end of the I.A. step (3J-75.04.31.2). The *compare gate* is re-established during the data-record step from 4F. The inputs to 4F are satisfied when the bit S trigger is turned on at the start of the first data-record character. The *address gate* was dropped at the end of the I.A. step and *write check status* was established during the I-cycles step.

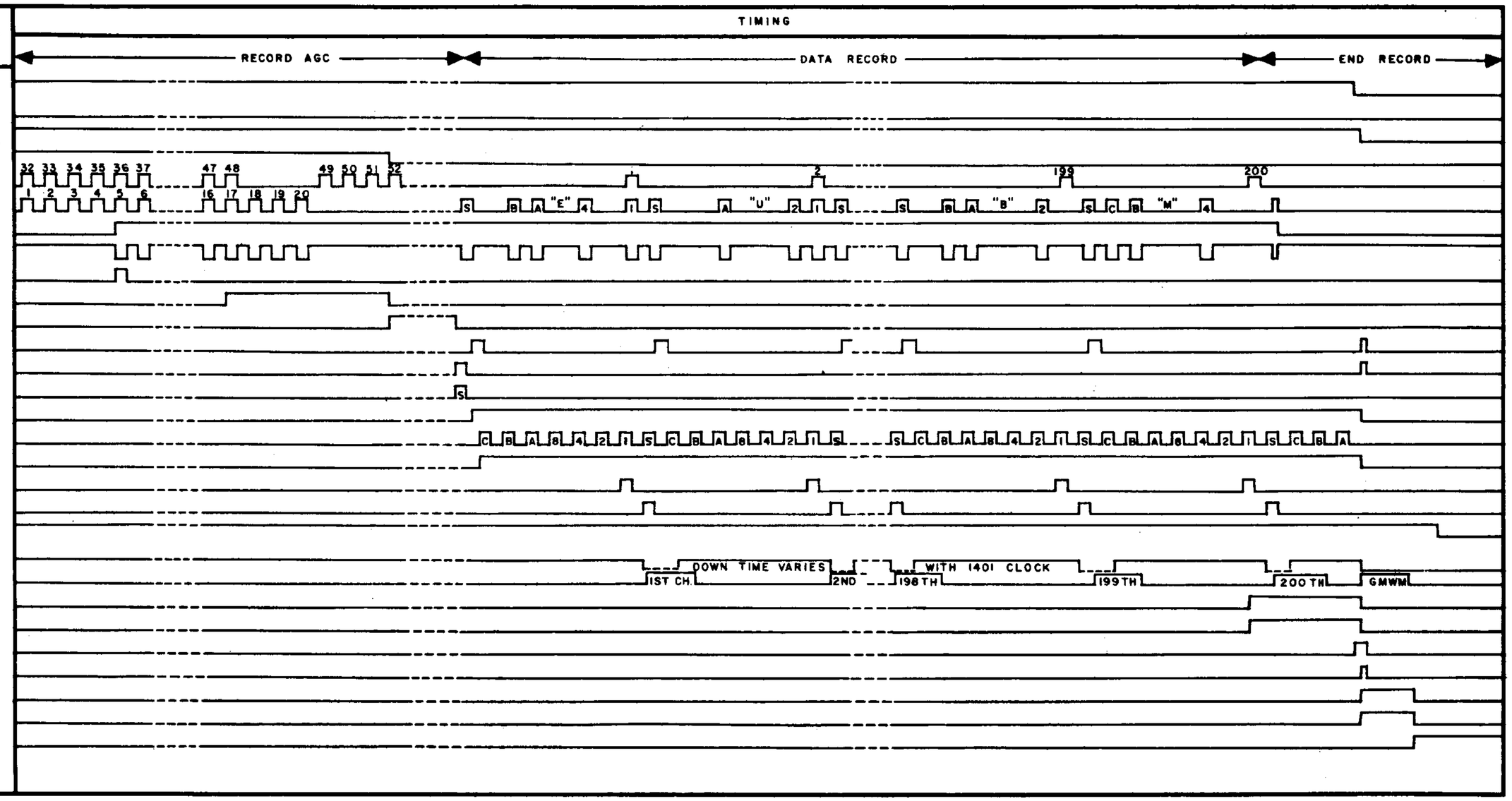
The *compare gate* remains up until reset at the end of the operation by *W reset*.

It is also significant to note the status of the single record and full track latches at the end of the previous write instruction (75.02.51.2). One or the other remains on because the write check interlock latch cannot be reset until *I op* time of the instruction following the execution of the write check instruction. Thus, the write check instruction is forced to check the same number of records written (one or five).

### Block Store A Register

To allow for the comparison and not the storage of the read data within the 1401, *store A register* must be blocked. When the write check latch is on, *not write check* is down. *Store A register* is therefore blocked at 3J (75.04.51.2).

| SIGNAL NAME | LOGIC | TEST POINT 01A: |
|---|---|---|
| -T START RLW. TR. | 75.28.11.1 | 2J24N |
| -T RECORD PULSE | 75.28.01.1 | 2J27N |
| -T SECTOR GATE | 75.04.51.2 | 1D14A |
| -T AGC GATE | 75.29.01.1 | 2G14E |
| +U CTRL. CTR ADV. PULSE | 75.32.01.1 | 2F19F |
| -T STANDARD RD. DATA | 75.31.11.1 | 2C04F |
| -T READ GATE | 75.35.01.1 | 2G07E |
| +U NOT RD. DATA TR. | 75.32.01.1 | 2J10G |
| +U CTRL. CTR 36 | 75.32.21.1 | 2H22H |
| -T COUNT 48 GATE | 75.32.21.1 | 2F18H |
| +U CTRL. CTR. 52 | 75.32.31.1 | 2H27H |
| +T CHAR. REG RESET | 75.36.01.1 | 2F10A |
| +T CTRL. CTR. RESET | 75.31.11.1 | 2C23A |
| +U SET BIT. S | 75.33.01.1 | 2C28A |
| +T BIT RING ADV. GATE | 75.33.01.1 | 2G06A |
| -T BIT RING ADV. PULSE | 75.33.01.1 | 2C07F |
| -T READ STROBE GATE | 75.31.11.1 | 2J12F |
| +U RESET A REG. | 75.01.71.2 | 1E24N |
| -T DATA STROBE | 75.31.11.1 | 2G10N |
| -T WRITE CHECK STATUS | 75.02.21.2 | 1E27H |
| -T 1401 CLOCK. CTRL. 1401 B CYCLES | 75.04.11.2 | 1D22C |
| +U CTRL. CTR. 200 | 75.32.31.1 | 2F27N |
| -T END RECORD GATE | 75.32.31.1 | 2G21E |
| -T R/W END OP. | 75.38.01.1 | 2G21H |
| +U Z RESET | 75.38.11.1 | 2G03N |
| -T LAST CHARACTER | 75.04.41.2 | 1D18N |
| -T SECOND GM WM | 75.03.21.2 | 1D21N |
| -T COMPARE GATE 1 OP. | 75.04.31.2 | 1D23N |




NOTE: THIS CHART SHOWS WRITE CHECK OF A MOVE OP.

LOAD OP IS THE SAME EXCEPT:
1. BIT RING INCLUDES A WM BETWEEN "S" AND "C" BIT.
2. OPERATION ENDS WITH COUNT 176 INSTEAD OF COUNT 200.

NOTE: UP LEVEL SHOWS ACTIVE STATE OF SIGNAL.

Figure 9-1. Write Check Operation

# Section 10 Write Address Operation (1405-1401)

The write address operation is performed only under CE supervision. The instruction M%F4BBB calls for a write address operation. However, a key lock switch, located on the CE test panel must be operated before the instruction can be executed. The indelible addresses are originally loaded onto the file at the factory. Therefore, the write address operation is used only if a particular address is destroyed.

A 7-character address is written on the previously selected record when the write address instruction is executed. The address of each disk is predetermined by the physical location of the disks on the disk array.

The operation is performed during the following sequential steps: Refer to Figure 10-1.

1. I-cycles.
2. Address transfer.
3. Write pre-I.A. AGC bits.
4. Write I.A. and end the operation.

## I-Cycles

The basic objectives during this step are to set the write address latch, the write file latch, and develop *write address status.*

Write address is set by a decode of four during I-ring 3. *Write file* and *write status* are then available from 75.02.31.2; they remain available until the next I-op time (75.02.41.2). *Write address* tests the status of the write address switch on 75.40.01.1. If the switch is on, *write address status* is available from 75.20.01.1 and the write address operation proceeds. If the switch is off, the operation is terminated at the beginning of the address transfer step (bit 4 of digit 0, 75.26.01.1).

## Address Transfer

The basic objectives to be accomplished during this step are the same as those for WRITE SINGLE RECORD, with one exception. The first write cycle must be taken at the end of this step. This will place the first I.A. character (module character) in the B register prior to the pre-I.A. AGC step; it is then ready to be transferred to the 1405 character register at the very beginning of the I.A. step.

*First write cycle* is turned on during digit 7 time when *address transfer* and *write address* are up (75.04.31.2). A for B substitute has placed the address of the module digit in MAIN STAR. The 1401 clock is allowed to run at the end of the address transfer step thereby placing the module digit in the 1401 B register. *First write cycle* then stops the clock (4H-75.04.11.2).

## Write Pre-I.A. AGC Bits

The basic objective of this step is to record the AGC bits with the same head used to write the I.A. characters. The amplitude of the AGC bits and the I.A. bits will then be approximately the same. This will allow the read amplifier gain to be properly set during succeeding operations.

The following objectives are developed in the normal manner:

| | |
|---|---|
| 1. Start-Read-Write | (75.28.11.1) |
| 2. Address Gate | (75.29.01.1) |
| 3. AGC Gate | (75.29.01.1) |

The following additional objectives are required:

| | |
|---|---|
| 1. Write gate | (75.34.01.1) |
| 2. Control Counter Advance | (75.34.01.1) |
| 3. Write AGC Latch | (75.34.01.1) |
| 4. Drop AGC Gate | (75.29.01.1) |

### Write Gate

The write gate latch is turned on from 3F (75.34.01.1) with $\phi$C delayed during the *Start R/W* pulse. It remains on until reset by *write address reset* which is generated at BS$\phi$C of digit 0 following the indelible address (3A, 4D-75.26.01.1). See BASIC READ WRITE CIRCUITS for the write amplifier operation.

### Control Counter Advance

The control counter is advanced following the development of the *start R/W* pulse to define the pre-IA AGC portion of the record and to count the number of AGC bits written.

During the pre-IA AGC bit time, the file clock is running. The phase Bs generated by the clock are gated by the output from 4E (75.32.01.1) to produce the counter advance pulses. The counter is advanced in this manner until it contains 72. When it contains 72, the bit S latch is set which sets the bit S trigger and in turn sets the bit ring advance gate. Further control counter advance pulses are then blocked by the absence of *not bit ring advance gate* at 4E.

### Write AGC Latch

The write AGC latch is used to bring up the *write data* line. *Write data* then gates $\phi$Cs to the write amplifier. A series of $\phi$Cs are then recorded on the disk during

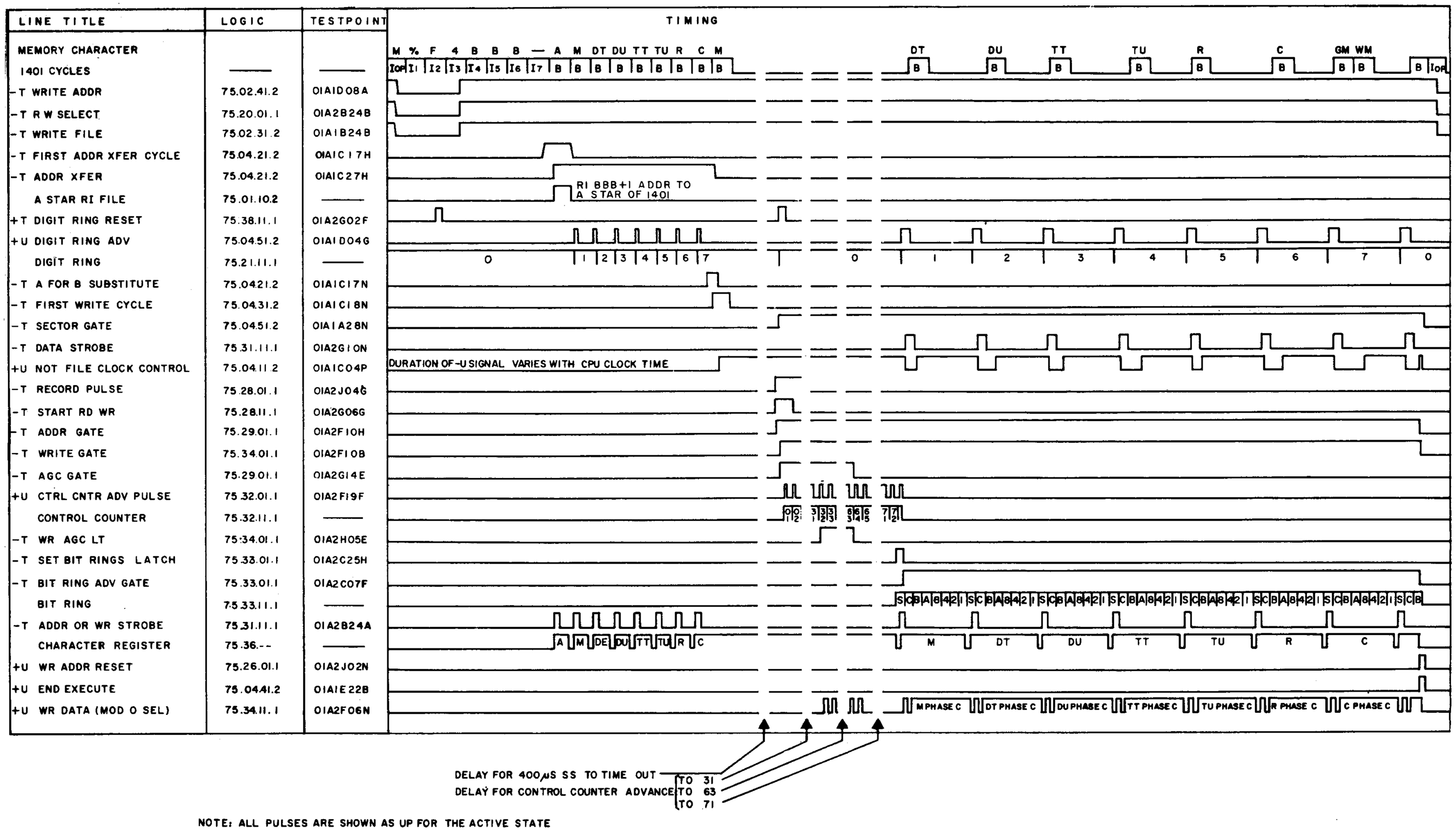



Figure 10-1. Write Address Operation

the time the write AGC latch is on. The latch is turned on by *count 32* if the *write gate* and the *AGC gate* are up (3C-75.34.01.1). It is turned off from 4B by count 64. Therefore, following the development of *start R/W*, the record contains a 32-bit gap, followed by 31 AGC bits, followed by a 9-bit gap.

#### Drop AGC Gate

The AGC latch is turned off by count 64 from 4H on 75.29.01.1.

## *Write IA and End the Operation*

Objectives

1. Set and advance the bit ring
2. Advance the digit ring
3. Develop write data
4. Control the 1401 clock
5. End the operation.

#### Set and Advance the Bit Ring

The bit ring is used to "serialize" the 1405 character register output. The ring must therefore be allowed to run through the IA step. The ring is set as described under WRITE PRE-IA AGC BITS. The bit ring advance gate is set at BS$\phi$D. Phase As are gated by the *bit ring advance gate* to become the *bit ring advance pulses.* Therefore, the first advance pulse occurs at BC$\phi$A to turn the bit-S trigger off and the bit-C trigger on. The ring continues to advance with each succeeding $\phi$A.

#### Advance the Digit Ring

The digit ring is advanced to identify the indelible address characters. It must therefore advance at 1405 speed to stay in step with the IA characters that are written. The advance pulses occur at bit-S time when the address gate is up (75.21.11.1). As previously described, the first bit S available is the bit S for the module character. This bit S then advances the digit ring to digit 1 to identify the module character.

#### Develop Write Data

During the address transfer step, the module character was placed in the 1401 B register. This character and each succeeding character of the IA must be transferred to the 1405 character register at the beginning of each digit time to enable them to be strobed from the character register by the bit ring during their respective digit time. The IA characters enter the character register when *write strobes* are developed at each BS$\phi$C time (4C-75.31.11.1). Write data is then developed in the normal manner as the bit ring strobes the character register output (75.36.01.1).

#### Control the 1401 Clock

See 1401 Clock Control under WRITE SINGLE RECORD operation.

#### End the Operation

The write address operation is ended when *write address reset* is developed at BS$\phi$C of digit 0 following the indelible address (3A, 4D-75.26.01.1). *Write address reset* serves to end the operation by developing *file end op, CPU end op,* and *end op* on 75.38.01.1. It also resets the write gate latch on 75.34.01.1.

# Section 11 Power Supply

The IBM 1405 requires a 3-phase 208/230-v source of power delivered to a 60-amp service. The main line voltage is fed through line CB2 and the emergency off contactor (K3) in the power distribution box. From the distribution box it is distributed to the following units as shown in Figure 11-1.

1. Access motor
2. 415-w ferroresonant regulator
3. 48-v power supply
4. File motor
5. Service transformer (step down)

The ferroresonant regulator distributes a regulated

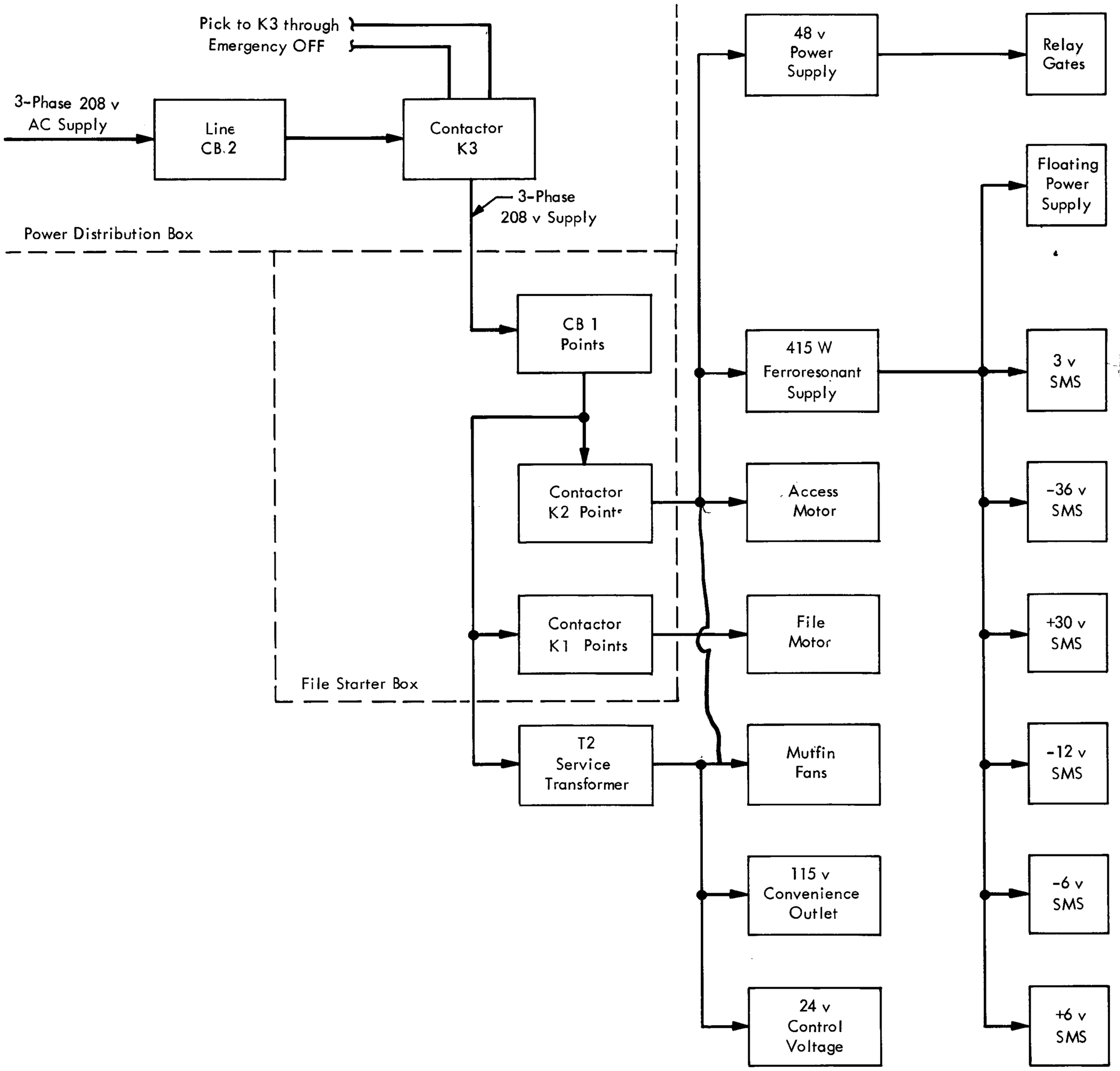



Figure 11-1. Ac and Dc Power Distribution

AC voltage to the standard series regulated SMS DC power supplies and to the 150-v floating power supply. The operation of the SMS power supplies and the ferroresonant regulator is explained in the CE Manual of Instruction on 60-cycle SMS power supplies (Form 225-6478).

## DC Voltages and Uses

The 1405 uses five standard series-regulated, 60-cycle SMS power supplies to develop –6, +6, –12, +30 and –36 v DC as shown in Figure 11-1. The 3-v SMS power supply (00.78.43.0) is used to develop the +6 M or –12 M voltage for the marginal checking circuits. This voltage is distributed through a switching assembly (75.58.31.1) to pins Q and R, respectively, of the SMS card sockets. By proper manipulation of the marginal control switches, the +6 M or –12 M voltage can be varied.

### Minus 6 Volts

The –6 v module is rated at 8 amps. It is distributed to terminal K on the SMS card sockets.

Minus 6 v is commonly used as the emitter voltage on NPN transistors in voltage mode circuits.

### Plus 6 Volts

The +6 v module is rated at 8 amps. It is distributed to terminal L of the SMS card sockets.

Plus 6 v is used as the collector voltage on NPN transistors used in voltage mode logic. In current mode switching, it serves a similar purpose.

Part of the output voltage from this supply is connected to the transistor circuitry through a switching assembly to develop the +6 M voltage previously mentioned.

### Minus 12 Volts

A standard series-regulated SMS power supply is used to develop the –12 v at 8 amps. It is distributed to pin M of the SMS card sockets.

Minus 12 v is referenced to –6 v and is used as the collector and base voltage for PNP transistors used in voltage mode logic. In current mode switching, it is used in a variety of ways.

Part of the output voltage of this supply is connected to transistor circuitry through a switching assembly to develop the –12 M voltage previously mentioned.

### Plus 30 Volts

The +30 v supply is rated at 2 amps. It is distributed to terminal N of those cards requiring +30 v.

It is used in the areas where large currents are required such as the clutch amplifier and clutch driver circuits.

### Minus 36 Volts

The –36 v power supply is a standard series-regulated SMS power supply. It is distributed to terminal P of the SMS card sockets that require –36 v.

The main application of this voltage is in current mode transistor logic.

## Power Sequence Unit

The power sequence unit is located in the file starter box (Figure 11-2). Its purpose is to control the distribution of the main line voltage to the various units shown in Figure 11-1.

The 1405, by means of the power sequence unit, can be operated in three different modes:

1. Remote automatic
2. Local automatic
3. Local manual.

## Remote Automatic Power ON Sequence

The 1405 is placed in the REMOTE AUTOMATIC mode when the rotary switch in the file starter box is turned to the remote automatic (RA) position. When the 1405 is in the RA mode, the compressor rotary switch must be placed in the REMOTE position. Power ON sequencing begins when the power ON key is pressed at the CPU (Figure 11-3).

### Objectives (Figure 11-4)

1. Energize start control relays.
2. Start file motor.
3. Start timer motor.
4. Start compressor motor.
5. Start access motor(s).
6. Activate 415-w ferroresonant DC supply.
7. Activate 48-v power supply.
8. Start muffin fan motors.
9. Establish a file ready condition.

#### ENERGIZE START CONTROL RELAYS

Relay R2 is energized (75.58.01.1) through the n/c K1 contact when the power ON key is pressed at the using system. R2 then holds through its own points as long as power is on at the using system. Remote power from the using system is then available from terminal C1-D through R2-1 n/o to energize R1. R1 holds through R3-1 n/c until the end of the power sequencing operation.

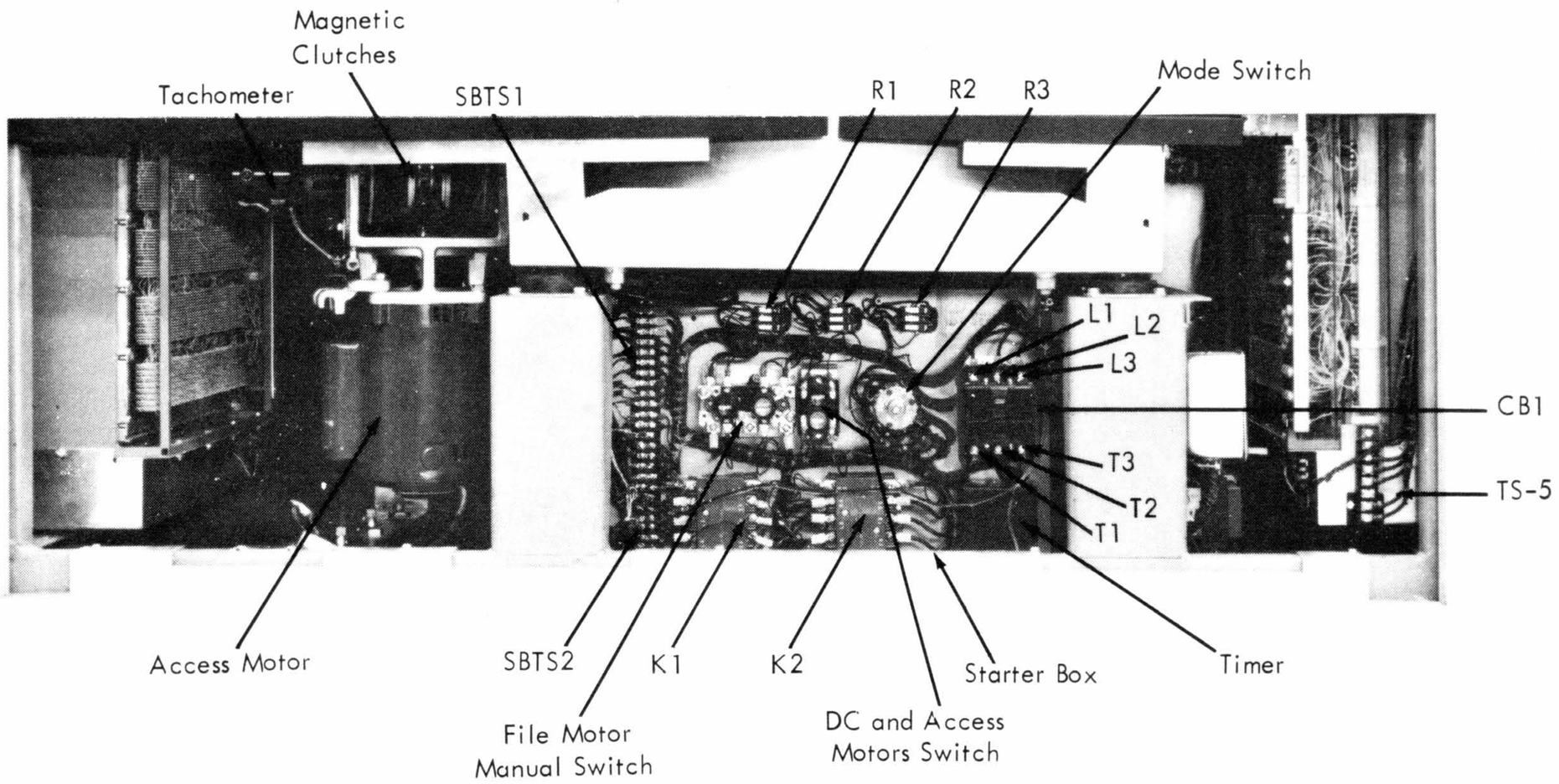



Figure 11-2. File Starter Box

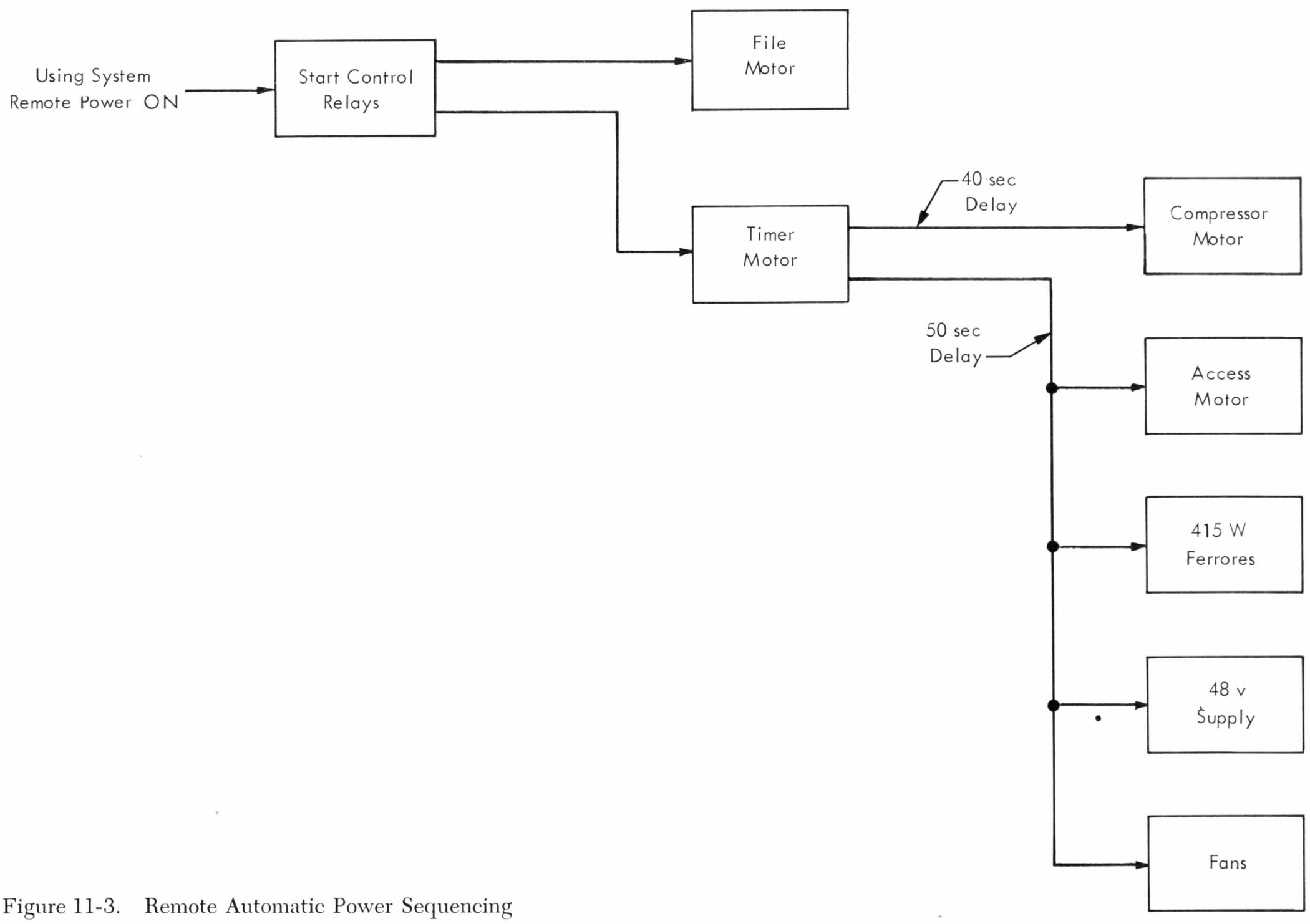



Figure 11-3. Remote Automatic Power Sequencing

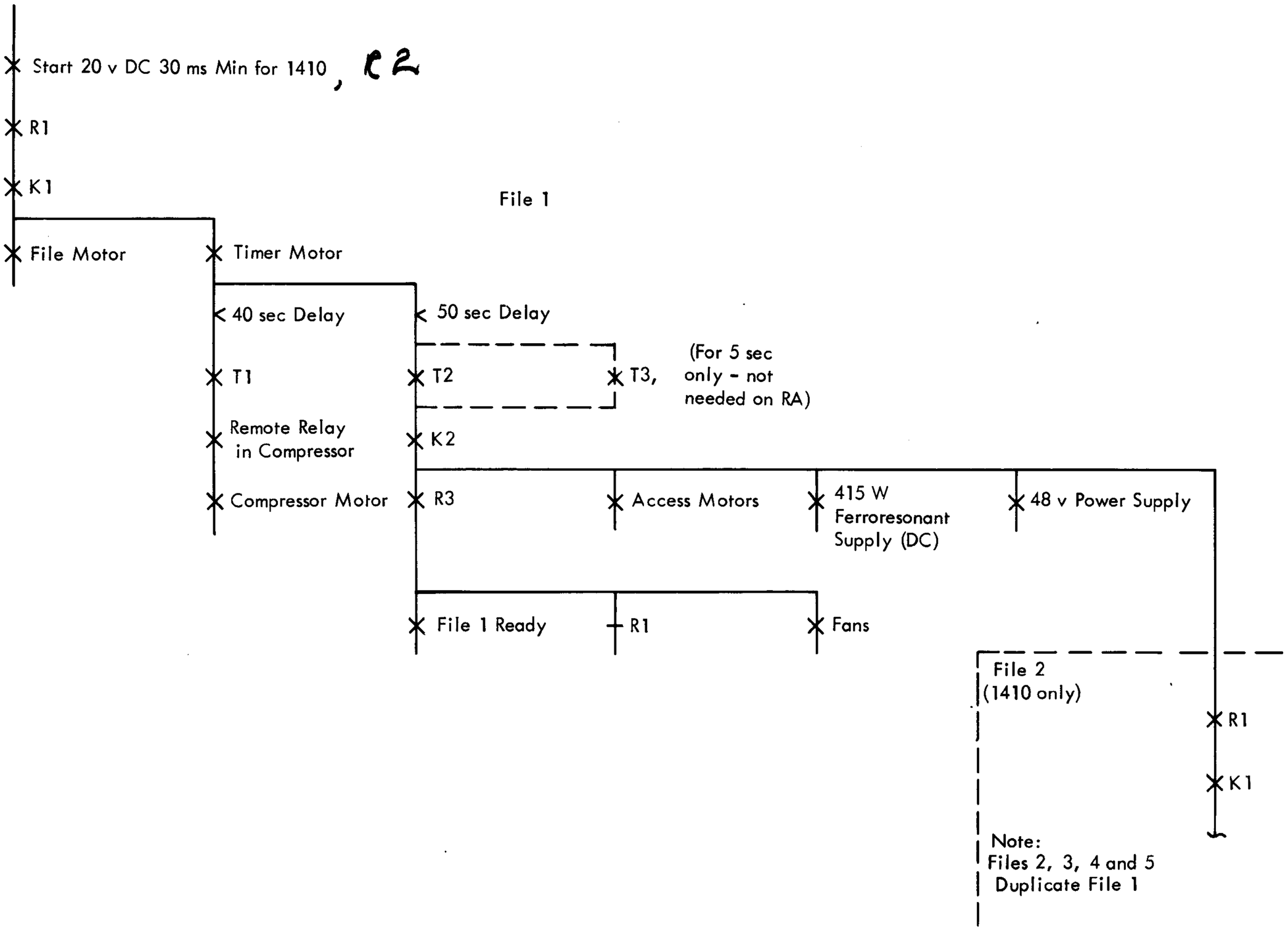



Figure 11-4. Remote Automatic Power Sequence

START FILE MOTOR

The file motor is energized through n/o points of contactor K1 (75.58.01.1). The circuit to pick K1 is through R1-2, the local auto stop switch to SBTS1-8 to the 24-v DC control voltage supply on 75.58.11.1.

K1 holds through one of its own n/o contactor points in parallel with R1-2 n/o.

It can be seen, from the foregoing, that there is no delay, except for relay pick time, in starting the file motor once power is brought up on the using system.

START TIMER MOTOR

When K1 is picked, the timer motor is energized through K1 n/o, the rotary switch terminals 46 and 47, the local auto stop switch, to the 24-v supply at SBTS1-8.

START COMPRESSOR MOTOR

The compressor motor (75.58.51.1) is energized 40 seconds after the timer motor is started through the T1 points on 75.58.01.1. When the T1 points close, the remote relay in the compressor is picked, from TS13 (75.58.51.1), to provide line voltage to the compressor motor.

START ACCESS MOTOR(S)

Fifty seconds after the timer motor is started, contactor K2 is energized through the timer T2 points (75.58.01.1). The circuit is traced as follows: from terminal C1 on K2 to terminal 1 of local DC ON switch, through R1-3 n/o to terminal 52 of rotary switch, through T2 to terminal 7 of K2, terminal 3 of local DC off, through the rotary switch terminals 37 and 36, to C1-H jumpered by the interconnecting cable to C1-N, through the rotary switch terminals 33 and 32, K1 terminals 1 and 2, rotary switch terminals 46 and 47, to terminal 45, local auto stop terminal 8, and SBTS1-8 to 24 v.

The ground side of this circuit depends on the SMS power supply circuit breaker interlock points being closed and R2-3 n/o transferred.

When K2 is energized, line voltage is supplied to the

access motor(s) through the points of K2 (75.58.01.1) and the access motor(s) toggle switch (75.58.11.1).

ACTIVATE 415-W FERRORESONANT DC SUPPLY

The ferroresonant supply transformer (T3-75.58.21.1) is energized when K2 is picked (see objective No. 5).

ACTIVATE 48-V POWER SUPPLY

The 48-v power supply (T1-75.58.21.1) is activated when K2 is picked (see objective No. 5).

START MUFFIN FANS

Power to start the muffin fans (75.58.21.1) is available from the service supply transformer (T2-75.58.11.1) when R3 is picked by K2 (75.58.01.1). The pick to K2 is described under objective No. 5.

When R3 is picked, R1 is dropped (75.58.01.1) to prevent it from drawing unnecessary power from the using system.

ESTABLISH A FILE-READY CONDITION

In a multifile system the file-ready signal is advanced to the succeeding file through R3-3 n/o (75.58.01.1). Each file, in the REMOTE mode, follows the same power sequencing as each preceding file develops the file ready signal.

## *Remote Automatic Power OFF Sequence*

This power-OFF sequence can be initiated by the using system or by the local auto stop or manual motor stop switch in the file starter box. In either case the sequence follows the same pattern with the following exception (Figure 11-5): when the power OFF sequence is initiated by the CPU, in a multifile system, all files go off in parallel (using system drops R2 in each file); activating the local auto stop or manual motor stop switch, drops only the file that contains the activated switch (K1 is dropped, R2 stays energized).

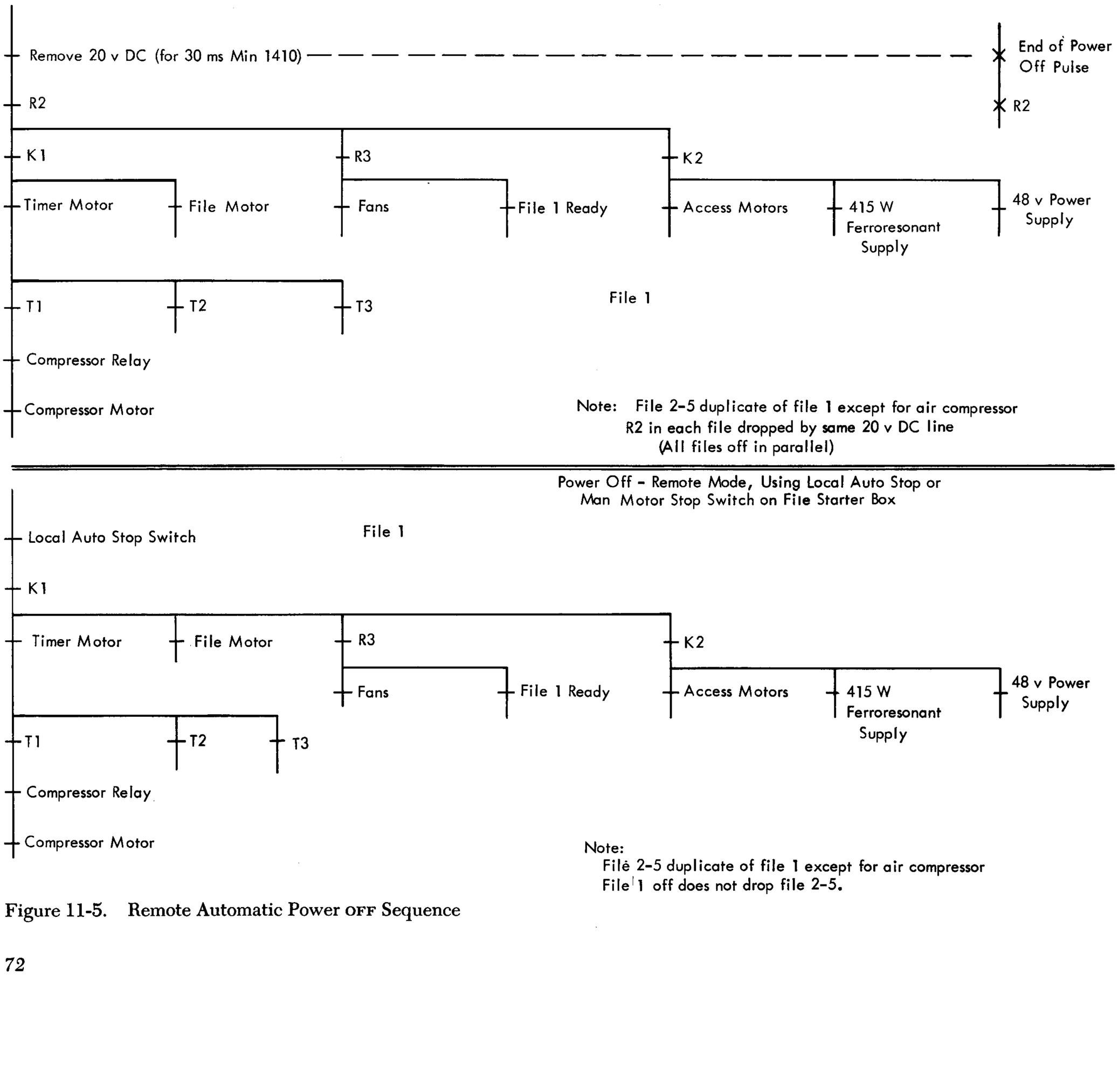



Figure 11-5. Remote Automatic Power OFF Sequence

### *Remote Automatic DC ON and OFF (1410 Only)*

When the DC OFF switch on the 1410 console is pressed, the circuit between terminals C1-H and C1-M is opened, thus dropping the hold to R3 and K2. When these two relays are down, the voltage supply to the fans, access motor(s), 415-w ferroresonant supply, and the 48-v power supply is interrupted (75.58.01.1 and 75.58.11.1). See Figure 11-6.

When the DC ON switch on the 1410 console is pressed, R1 is picked to provide a pick to K2 and R3 thus restoring power to the fans, access motor(s), and DC supplies.

### *Local Automatic Power ON and OFF*

The 1405 is placed in the local automatic mode when the rotary switch in the file starter box is turned to the Local Automatic (LA) position. When the 1405 is in the LA mode, the compressor rotary switch must be placed in the remote position. Power ON sequencing begins when the local auto start or manual motor start switch in the file starter box is pressed. The objectives for this mode are the same as those listed under REMOTE AUTOMATIC POWER ON SEQUENCE, excepting the first. The start control relays, previously defined as R1 and R2, are bypassed in this mode (Figure 11-7).

The file motor contactor, K1, is picked directly, when the local auto start or manual motor start switch is pressed (75.58.01.1) through terminals 42 and 48 of the rotary switch (LA position). K1 starts the timer motor. Fifty seconds later K2 is picked through T3 to supply power to the fans, access motor(s), and DC supplies. This circuit goes through terminals 31, 32 and 45, 46 of the rotary switch.

The power OFF sequence is initiated by pressing the local auto stop or manual motor stop switch in the file starter box (75.58.01.1). When this switch is pressed, K1 is dropped to initiate the sequence shown in Figure 11-7.

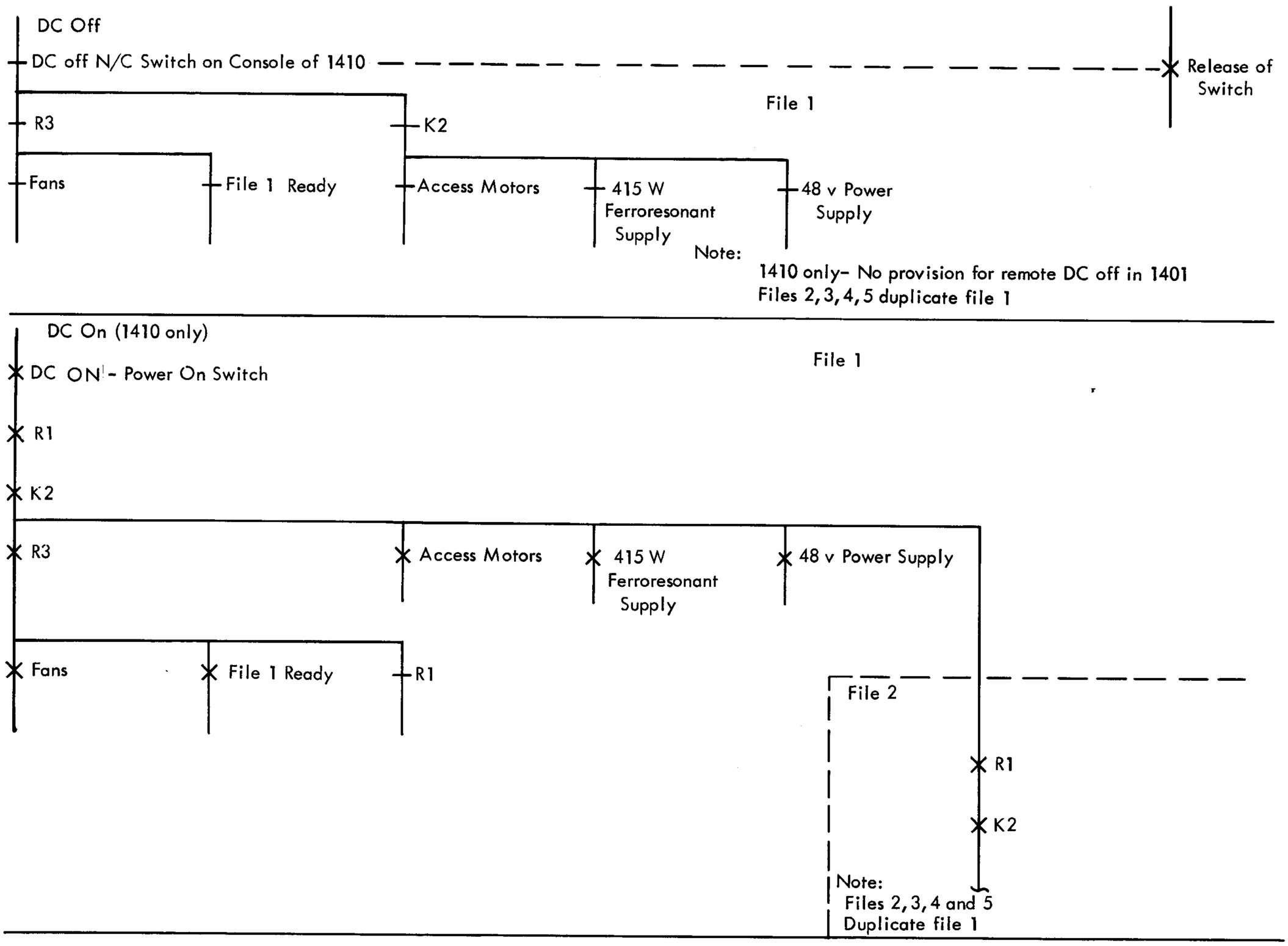
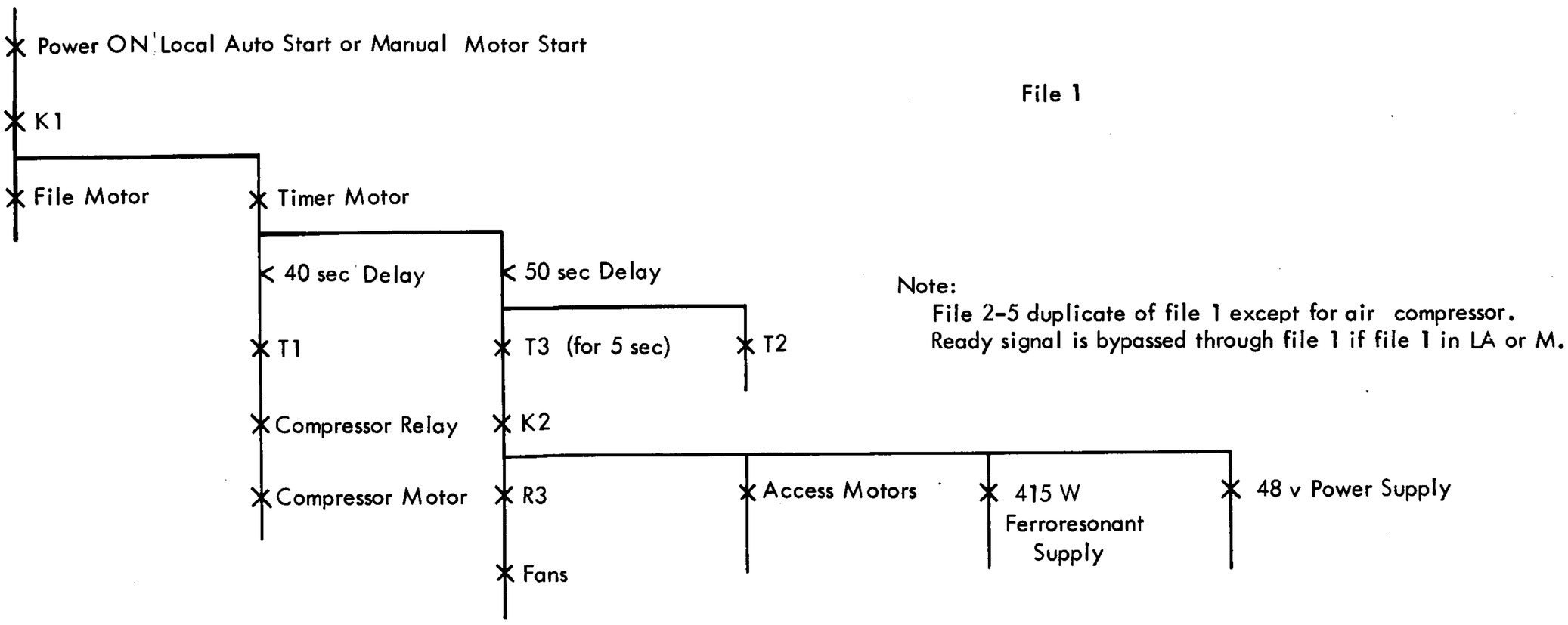



Figure 11-6. Remote Automatic DC OFF and DC ON.



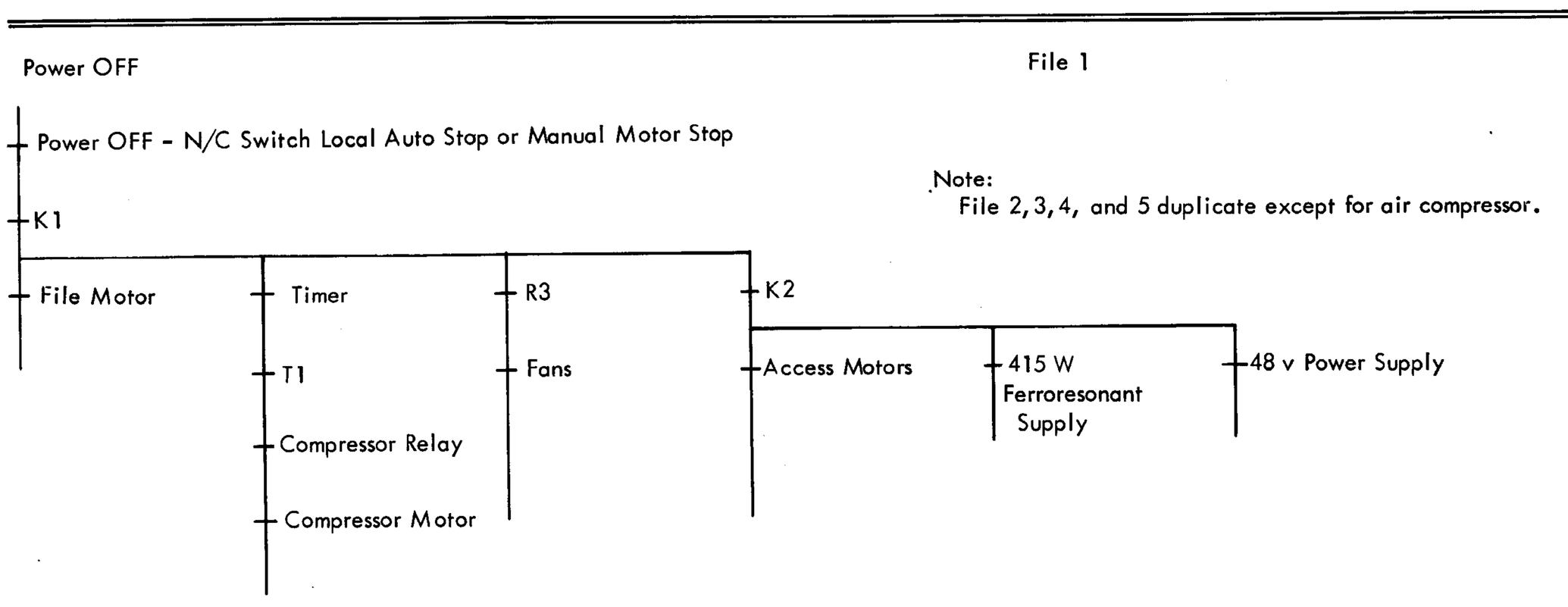




Figure 11-7. Local Automatic Power ON and OFF.

### *Local Automatic DC ON and OFF (Figure 11-8)*

Power is supplied to the fans, access motor(s), and DC supplies when the DC ON switch is pressed in the file starter box; the rotary switch is in the LA position. (75.58.01.1). This circuit uses terminals 51 and 52 on the rotary switch and T2 to supply the 24 v required to pick K2 and R3. K2 and R3 then hold through their own points, the DC OFF switch, and terminals 31, 32 and 45, 46 of the rotary switch.

DC OFF is initiated by pressing the DC OFF switch to open the hold circuit to K2 and R3.

### *Local Manual Power ON and OFF*

The 1405 is placed in the LOCAL MANUAL mode when the rotary switch in the file starter box is turned to the M (manual) position. The compressor rotary switch is set to LOCAL. In this mode the file motor, DC supply, and compressor are individually controlled.

#### File Motor ON and OFF (Figure 11-9)

In the manual mode, the file motor is started when K1 is picked by the local auto start or manual motor start switch. This circuit uses terminals 41 and 48 on the rotary switch.

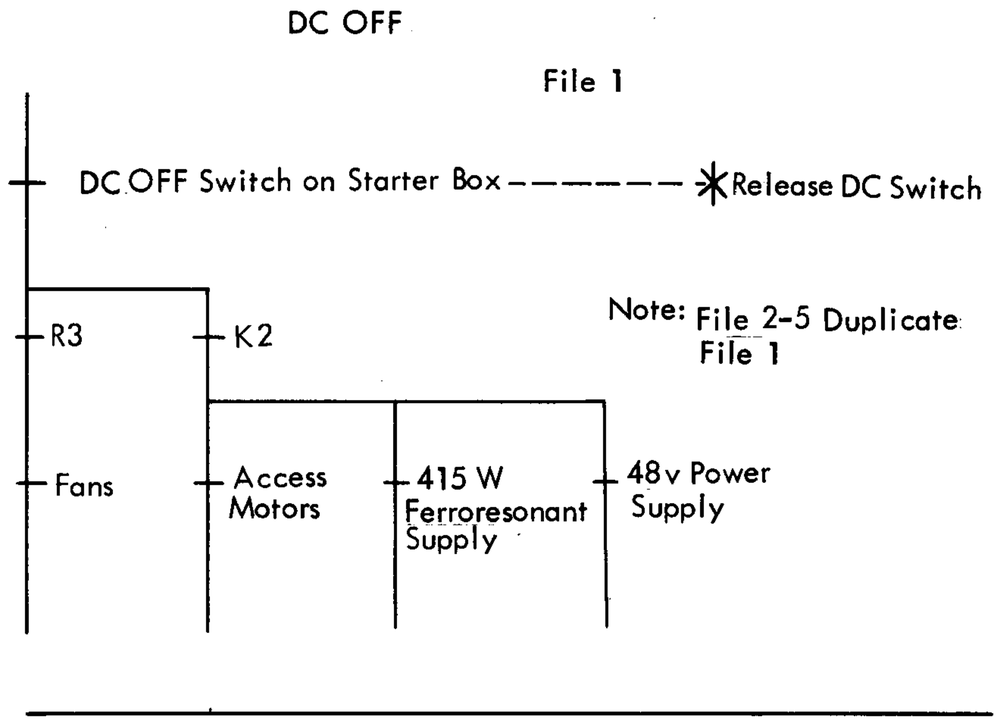



Figure 11-8. Local Automatic DC OFF and DC ON.

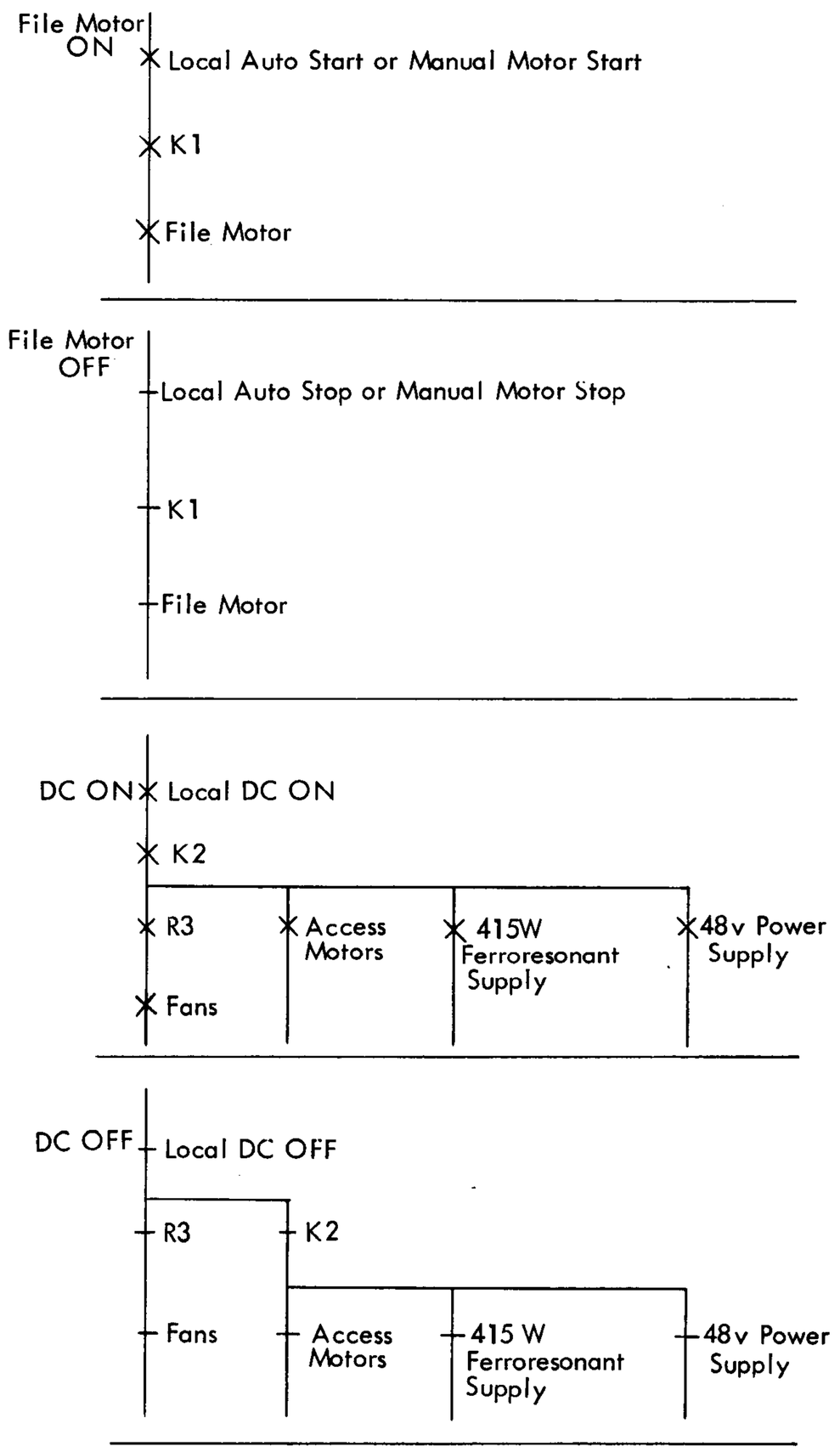



Figure 11-9. Local Manual Power Operation

K1 holds through its own points and the local auto stop or manual motor stop switch. To stop the file motor, the hold to K1 is opened by pressing the local auto stop or manual motor stop switch (75.58.01.1).

## DC ON

The DC supplies are supplied through the points of K2. K2 is picked when the local DC ON switch is pressed (75.58.01.1). This circuit uses terminals 51, 58 and 42, 48 of the rotary switch.

The hold for K2 is established through its own points, the local DC OFF switch, and terminals 44 and 45 of the rotary switch. DC OFF is initiated when this hold circuit is opened by pressing the local DC OFF switch.

# Section 12 1405-1410 File Operations

## Seek Operation

In order to facilitate the explanation of the circuits involved in a seek operation, assume that a disk-to-disk servo, using access 0 in module (file) 0, from address 00195 (disk 00 track 19 record 5) to address 94362 is called for by the instruction M%F0BBBBBR. Figure 12-1 and 12-2 contain logic flow diagrams showing 1410 operation during the execution of the seek instruction.

### Objectives

1. Select the 1405 for a seek operation.
2. Transfer new address to file (address transfer).
3. Test for file busy condition.
4. Start mechanical servo operation.
5. End seek address transfer.
6. Retrack R/W heads.
7. Disengage track detent.
8. Move arm out.
9. Disengage disk detent.
10. Move carriage up.
11. Engage the disk detent and release.
12. Move arm in.
13. Engage track detent.
14. Extend read/write heads.
15. Notify CPU that servo is complete with *access ready* signal.

#### Select the 1405 for a Seek Operation

When the CPU encounters the instruction M%F0BBBBB, the E channel is selected to send the 8-character record address to the file.

After the normal 1410 I/O interlock check the MOVE or LOAD condition is established in accordance with the instruction M/L. If the operation is to be performed in the LOAD mode, *CPU load* is sent to the FCU through the attachment unit (75.81.01.1). The file is normally conditioned to operate in the MOVE mode; therefore, the MOVE command is not transmitted to the file.

Once the M/L condition is established, the file is selected when the F in the instruction is decoded and the file op latch is set in the CPU. *File op* is then transmitted to the 1405 ATU to signal the 1405 that a disk storage operation is to be performed (75.81.01.1). The type of file operation to be performed is determined by the decode of the character following the F in the instruction; in this case 0 (zero). When the 0 is decoded, $-C$ *CPU seek* is generated and transmitted to the ATU to develop $+U$ *CPU seek* (75.81.11.1) if *file op* has been established and the write check interlock latch is off. The $+U$ *CPU seek* is used to select the file for a seek operation by generating $-T$ *seek status* in the FCU (75.20.01.1). The write check interlock latch is turned on at digit-7 time of a FILE WRITE operation. It remains on until reset by *master reset* or a CPU read-back-check operation. Its purpose is to prevent file seek operation following a WRITE operation (75.80.31.1).

If the write check interlock latch is on when a seek operation is called for, $+U$ *CPU seek* is blocked (4A-75.81.11.1) thus, preventing the development of $-T$ *seek status* in the FCU. It also prevents the resets to all latches in the ATU that normally arise from the development of *begin op reset* (75.81.91.1).

When the write check interlock is interrogated, as just described, the read back check latch in the CPU is interrogated. If a read back check has not been made since the last write operation, *master error stop* is generated in the CPU.

#### Transfer New Address to File

Following the set of the 1410 D-cycle latch, the *address transfer gate* is sent to the 1405 ATU (75.81.11.1) where it is powered up, level set, and sent to the FCU (75.20.01.1). The *address transfer gate* conditions the file for the address transfer step. The gate remains up until the last address character is transferred.

Once the *address transfer gate* is up, the CPU reads out the new address (parallel-by-bit and serially-by-character) to the 1405 character register (75.36.01.1). Each character of the address enters the character register under control of *address strobe* provided the CPU does not sense a B channel GMWM. If the CPU does sense the GMWM, the E channel wrong length record indicators in the CPU and in the 1405 are set (75.80.51.1). The E channel wrong length record indicator then provides a reset to the address transfer gate in the 1410 to terminate the file operation.

The absence of a B channel GMWM allows the CPU to send *first address strobe* to the file ATU (75.81.11.1) where it becomes *address strobe* and is then directed to the FCU (75.31.11.1).

The first character (access character) then enters the 1405 character register (75.36.01.1). It is immediately strobed out of the character register to the select register by *address strobe* delay (the same strobe that allowed it to enter the character register but delayed by 1.2 $\mu$s (75.31.11.1) ANDed with digit 0 (75.23.01.1). The second character (module digit) is handled in the same way at digit 1 time.

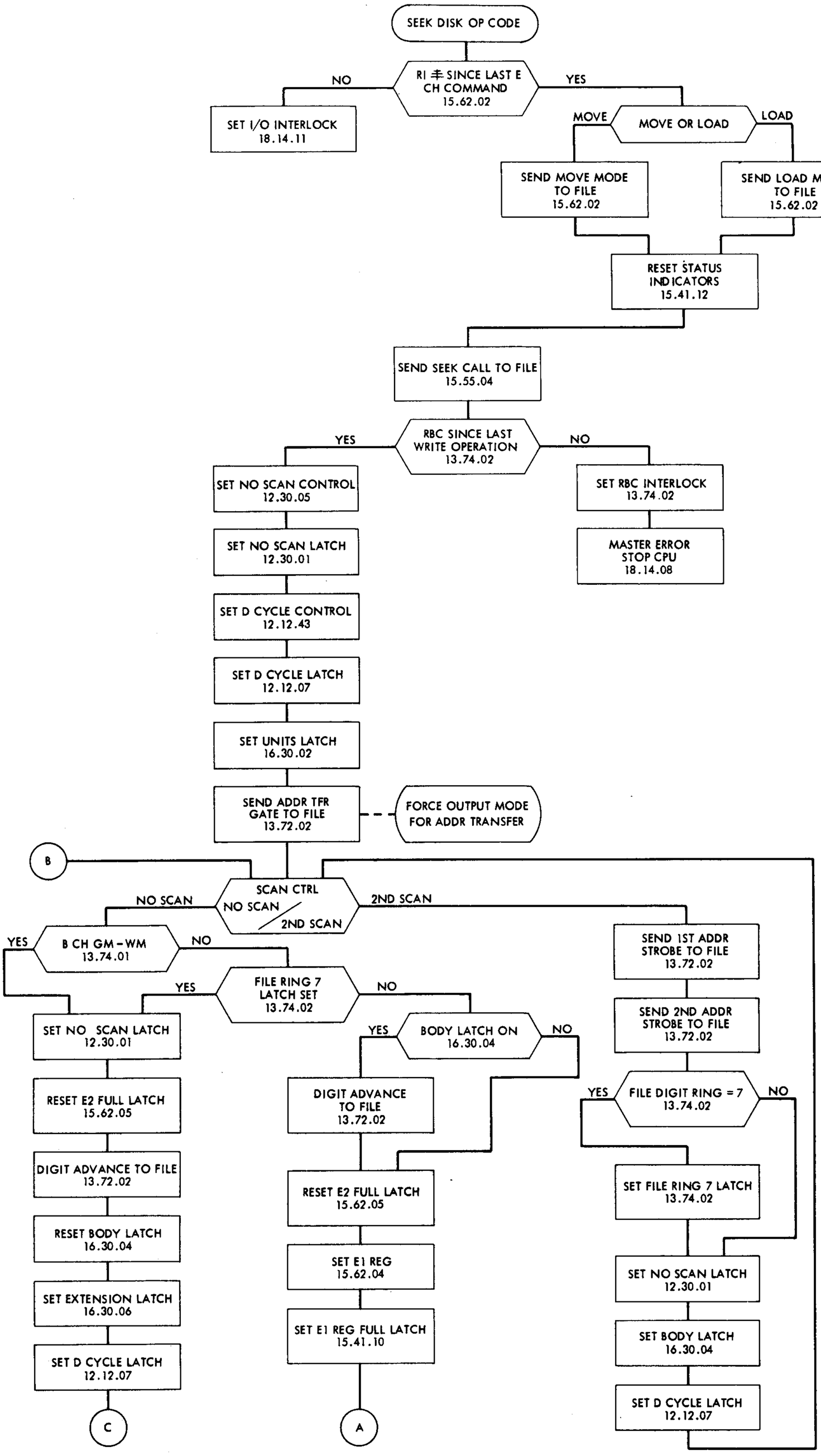



Figure 12-1. Seek Operation (1 of 2)

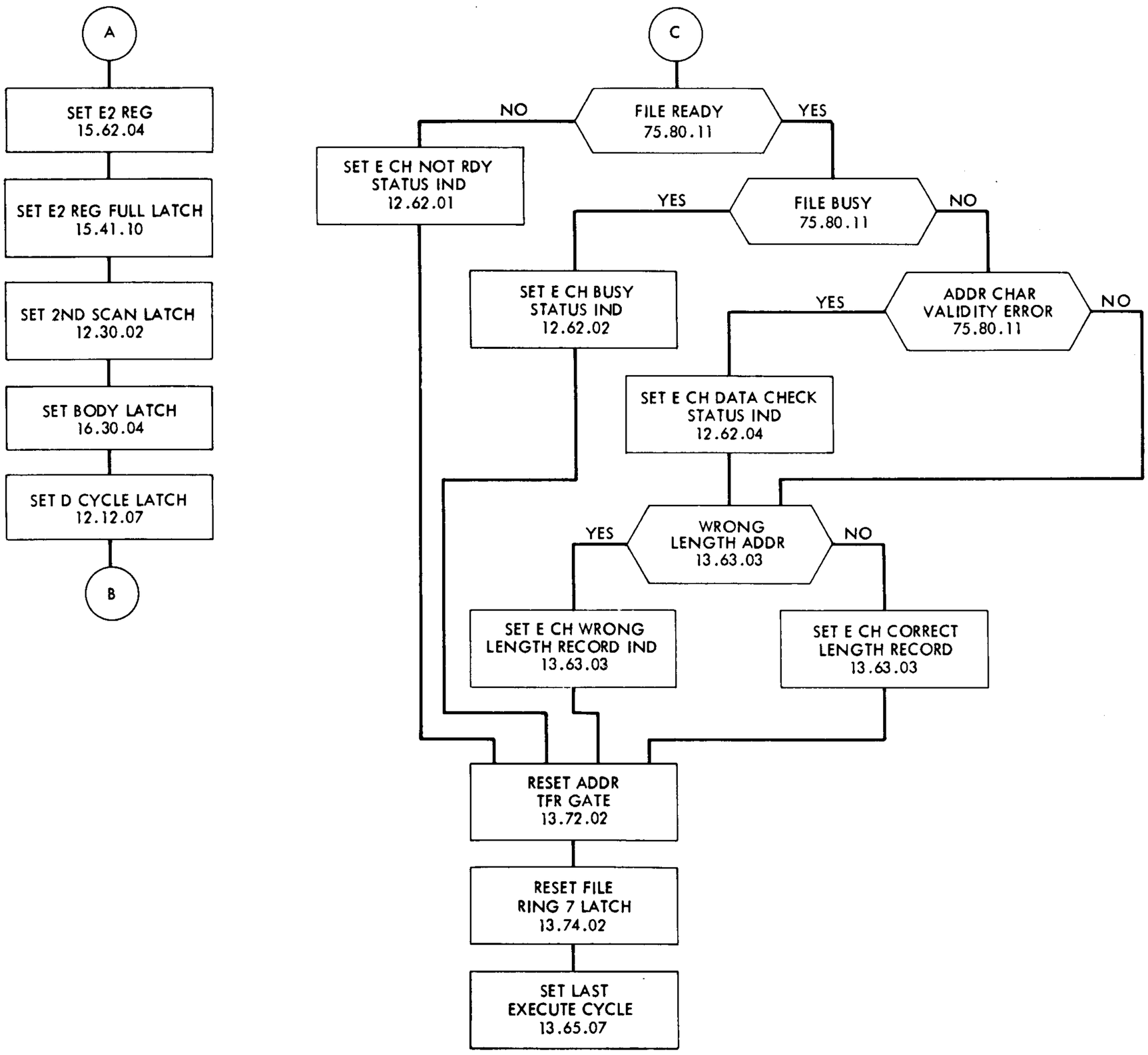



Figure 12-2. Seek Operation (2 of 2)

The 1405 digit ring is used to identify the address characters. It is reset with the digit 0 trigger on (75.21.11.1) The ring is advanced once during each *file op D cycle no scan* after the first by the digit ring advance pulse (75.81.11.1). The first advance is prevented because the body latch is off. Thus, the first character transferred is identified as digit 0 (the access character). The 1410 body latch is set following the transfer of the first character to the file, allowing the development of subsequent digit ring advance pulses for each character transferred. The second character transferred is then identified as digit 1 (module character), etc.

By the end of digit 1 time, the access and module characters (00) are stored in the select register. *Access 0 select* and *mod 0 select* are then available from 75.23.01.1.

At digit 2 time, the disk tens character (9) is strobed out of the 1405 character register by *delayed address strobe* (75.24.01.1). The resultant bit-1 and bit-8 lines are then powered up and driven to 75.60.61.1 where they are ANDed with *access 0 seek select* (combination of access 0 select, mod 0 select and seek status 75.25.01.1), and digit 2 at the latching type relay drivers, 3A and 3D.

Each subsequent character of the address is handled in the same way at digit 3, 4, and 5 time, respectively. The record character (2) is not stored at this time. It is stored during the following read or write operation. Therefore, at the end of digit 5 time, during the address transfer portion of the operation, the disk and track address characters have been stored in the latching relay drivers (75.60.61.1).

As each relay driver is activated, a pick line is estab-

lished to a corresponding address relay (75.70.01.1). The hold is maintained over the address relays from the previous seek instruction, until the new pick lines are established. Thus, if the same address relay is used on a successive seek operation, it does not drop when the hold line is opened. The hold line is opened approximately 15 ms following the development of *servo start*. *Servo start* is covered later.

### Test for File Busy Condition

By digit 2 time, during the address transfer step, *selected ready* is developed if the previous seek operation by the same arm in the same file, has been completed (75.27.01.1). If the previous SEEK has not been completed, then the access busy latch is set in the ATU at digit 2 time (75.81.31.1). The resultant output sets the E channel busy status indicator in the 1410 and also develops a *seek end op* to reset the 1405 (75.38.01.1).

### Start Mechanical Servo Operation

The initiation of the servo operation is controlled by the three start relays on 75.70.31.1. Start 1 is picked when *servo start* is developed by *address strobe* at digit 6 time (75.38.01.1) during the address transfer portion of the seek operation (Figure 4-1). *Servo start access 0* is then available from the latching driver at 6C (75.60.51.1).

### End Seek Address Transfer

The 1405 digit ring not only identifies the address characters but also serves as a counting device to ensure that the record address is the correct length. When the eighth and final address character is sent to the file, the 1405 digit ring is advanced to digit 7 and the file ring 7 latch is set in the 1410. The next character read from storage should be a GMWM. The two are then gated together; the presence of one without the other results in a wrong length address and the E channel wrong length record indicator is set.

When the file ring seven latch is set in the CPU, the CPU generates a digit ring advance pulse to advance the 1405 digit ring to digit 0 (resets the digit ring).

During the final D cycle, no scan is on. The E channel status indicators are tested, the address transfer gate and file ring 7 latch are reset and last execute cycle is set.

### Retract R/W Heads

Refer to Figures 4-2 and 4-3. The R/W head solenoid (75.71.81.1) controls the air supplied to the heads. The solenoid is de-energized as soon as the head relay (R70) is dropped. Note, it is only necessary to drop the head relay if the disk address has been changed (disk-to-disk servo). The head relay dropped when start 1 picked to drop the disk null relay, R58 (75.70.31.1). When air is removed from the heads, the return springs acting on the head gimbal pins restore the heads to their recessed position.

### Move Arm Out

Refer to Figures 4-3 and 4-4. To accomplish this objective the carriage must be detented, the track detent must be released, and the out-up clutch must be energized.

The track detent solenoid was de-energized when start 1 picked (75.71.81.1). The disk detent in solenoid remains energized through the n/c points of the track null and home relay (75.71.81.1).

The out-up clutch (75.72.11.1) is energized by applying a positive track error signal to the clutch amplifier on 75.62.61.1 and by energizing the clutch power mercury relay (5C-75.61.51.1). *Clutch power 1, clutch power 2* and *access 0 safe* are required to energize the clutch power relay. *Clutch power 1* is available when the track detent switch is transferred to the out position (75.71.51.1). *Clutch power 2* is available when the disk null relay drops (75.71.51.1). The latter circuit provides for a delayed energization of the clutch power relay if the R/W heads were previously located at one of the outer 40 tracks. This delay allows the R/W heads to be fully recessed by the time they reach the periphery of the disk. The positive track signal from the track potentiometer is supplied by grounding the home position through a n/c point of the disk null relay. The de-energized disk null relay indicates that the arm must be completely retracted; the n/c null relay points ground a position on the track potentiometer minus end, beyond track address 00 (75.70.91.1).

### Disengage Disk Detent and Lock Arm Out

Refer to Figures 4-3 and 4-4. When the arm is fully retracted, a track null is developed and the track null relay (R55) is energized. The R55-2 n/o points (75.71.81.1) close to energize the disk detent out solenoid. At the same time the R55-3 n/o points open to de-energize the disk detent in solenoid. When the disk detent is disengaged, the fail-safe is engaged and the home relay (R69) is picked (75.71.51.1).

During a disk-to-disk servo, when the transfer from track drive to disk drive takes place, a considerable amount of time (with respect to milliseconds) is required to transfer the disk detent and the fail-safe mechanism. In order to save some of this time, the home null region is widened to enable the track null relay to pick early. This widening effect is created, when the disk null relay is down, by placing a 33K resistor in parallel with the clutch amplifier level potentiometer (Figure 3-3).

### Move Carriage Up

When the fail-safe mechanism is engaged, the arm is locked in the home position. Under this condition, if the out-up clutch is energized, the carriage moves up. A positive disk error signal is applied to the clutch amplifier (Figure 3-3) through the transferred home relay points (75.62.01.1). In this example, the carriage is located at disk 00 while the disk potentiometer is grounded at location 94 through the address relay points on 75.71.61.1.

### Engage Disk Detent

Refer to Figures 4-3 and 4-5. When the disk null is detected, the disk detent in solenoid is energized through the n/o disk null relay points (R58-5). At the same time the disk detent out solenoid is de-energized when the R58-3 n/c points open (75.71.81.1). When the disk detent is engaged, the fail-safe is disengaged and the home relay is dropped (75.71.51.1).

### Move Arm In

Energizing the in-down clutch with the disk detent engaged causes the arm to move in until a track null is detected. A negative track error signal is supplied to the clutch amplifier when the home relay is dropped (Figure 3-3). In this example, the track potentiometer is grounded at track position 36 by the points of the track address relays (75.71.91.1). The address relays place 40 units of resistance in parallel with the track potentiometer between positions 00 and 40. The ground is then established to provide 4 units of resistance down from track 40 or 36 units of resistance up from track 00, thereby, establishing the track null point at track 36.

### Engage Track Detent

Refer to Figure 4-6. When the track error signal reaches zero, the track null relay (R55) is picked (75.70.31.1). With the disk and track null relays energized and the start 1 relay de-energized, one of the four track solenoids on 75.71.81.1 is energized. The selection of the correct solenoid is determined by the track address relays as shown in the chart on 75.71.81.1. In this example, track solenoid 0 is selected because the tens digit (3) of the track address is odd and the units digit of the address is 6.

### Extend R/W Heads

The head relay (R70) is picked through the track null relay points (75.71.81.1). The R/W head solenoid is then energized through the n/o points of the head relay (75.71.81.1).

### Access Ready

This signal is developed to inform the CPU that the mechanical servo is complete. It results from the pick of the arrival relay (R62-75.70.30.1). The arrival relay is picked when the track detent switch transfers if a track null exists and the head relay is up (75.71.51.1). However, *Access 0 Ready* from 75.70.31.1 must find the condition ready latch off before it is allowed to signal the CPU of the ready status (3A-75.61.81.1).

The condition ready latch ascertains that the mechanical servo operation was initiated. The latch is turned on at digit 3 time of a seek operation and is turned off when both start 1 and start 3 are down (Figure 4-2). Start 1 and start 3 are both down for a short time after the initiation of the mechanical servo.

## *Customer Engineering Track Selection*

One of the two CE tracks (inner or outer) on an addressed disk is selected when the CE test lock switch is on and a seek operation is called for. If the track units address is odd, the inner track is selected. If the track units address is even the outer track is selected.

The test relay (R30 for access 0) is energized on 75.70.31.1 from 75.39.01.1 when the test lock is on. With the test relay up, the track pot is grounded one track out from 00 if the track units address is even, or one track in from track 199 if the track units address is odd (75.79.91.1).

Track solenoid 0 is selected through points of the test relay if the inner CE track is selected. Track solenoid 3 is selected if the outer CE track is selected (75.71.81.1).

## Read Single Record Operation

A read single record operation is called for by the instruction M%F1BBBBBR. During instruction read out, the hundreds position character of the X-control field defines the type of operation (overlap or unoverlap) as well as the channel to be used (E or F). The tens position of the X-control field is always F to specify a 1405 operation. The units position of the X-control field is either a 1 or a 2 to specify a single record or full track operation. The d character must be an R to specify a read operation.

The operation is performed during the following sequential steps:

1. Instruction cycles
2. Address transfer
3. Read pre-indelible address AGC bits
4. Read indelible address (compare)
5. Read pre-record AGC bits
6. Read data record.

Figures 12-3, 12-4, 12-5, and 12-6 contain logic flow diagrams showing 1410 operation during the execution

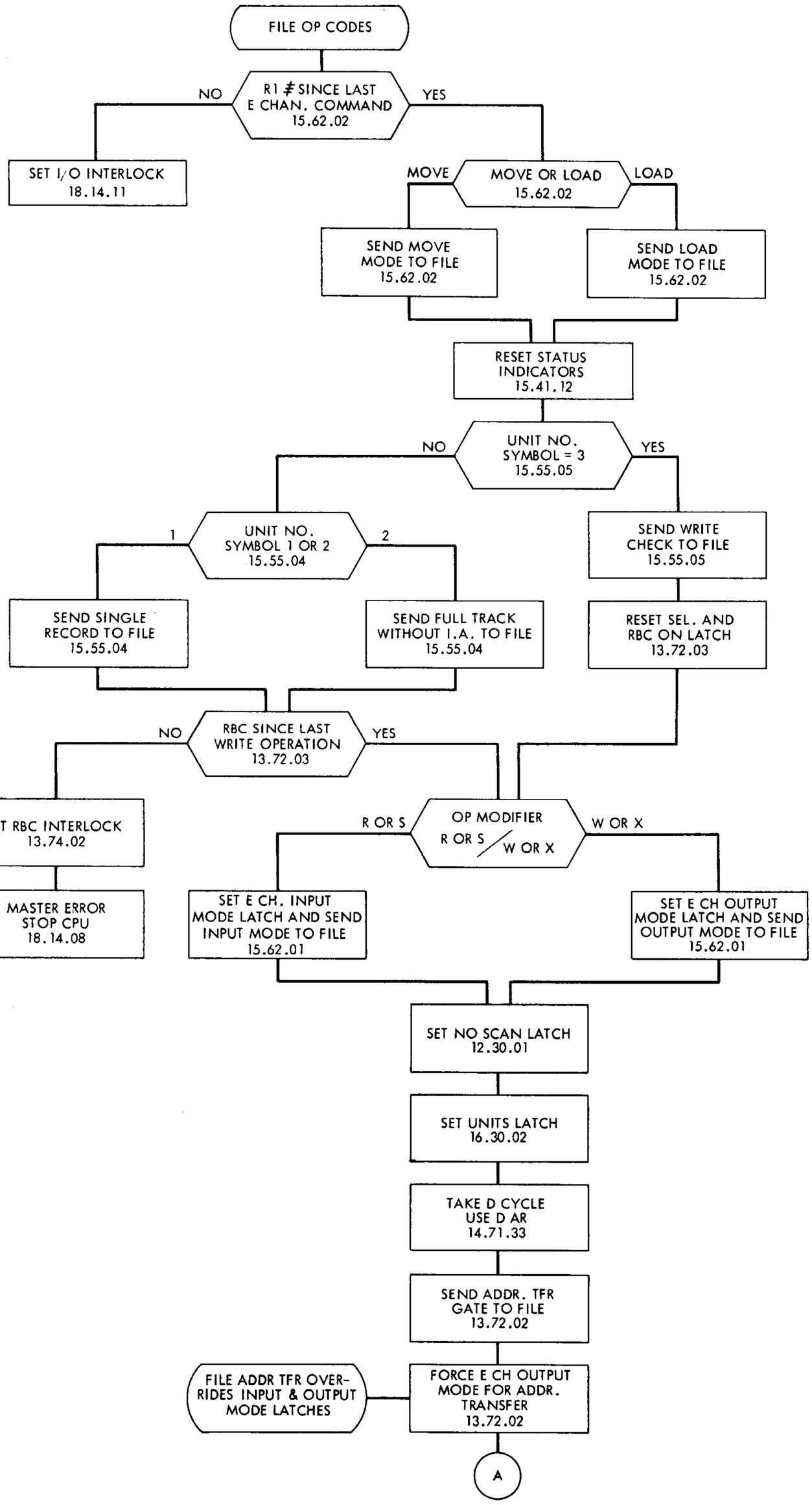



Figure 12-3. Address Transfer (1 of 4)

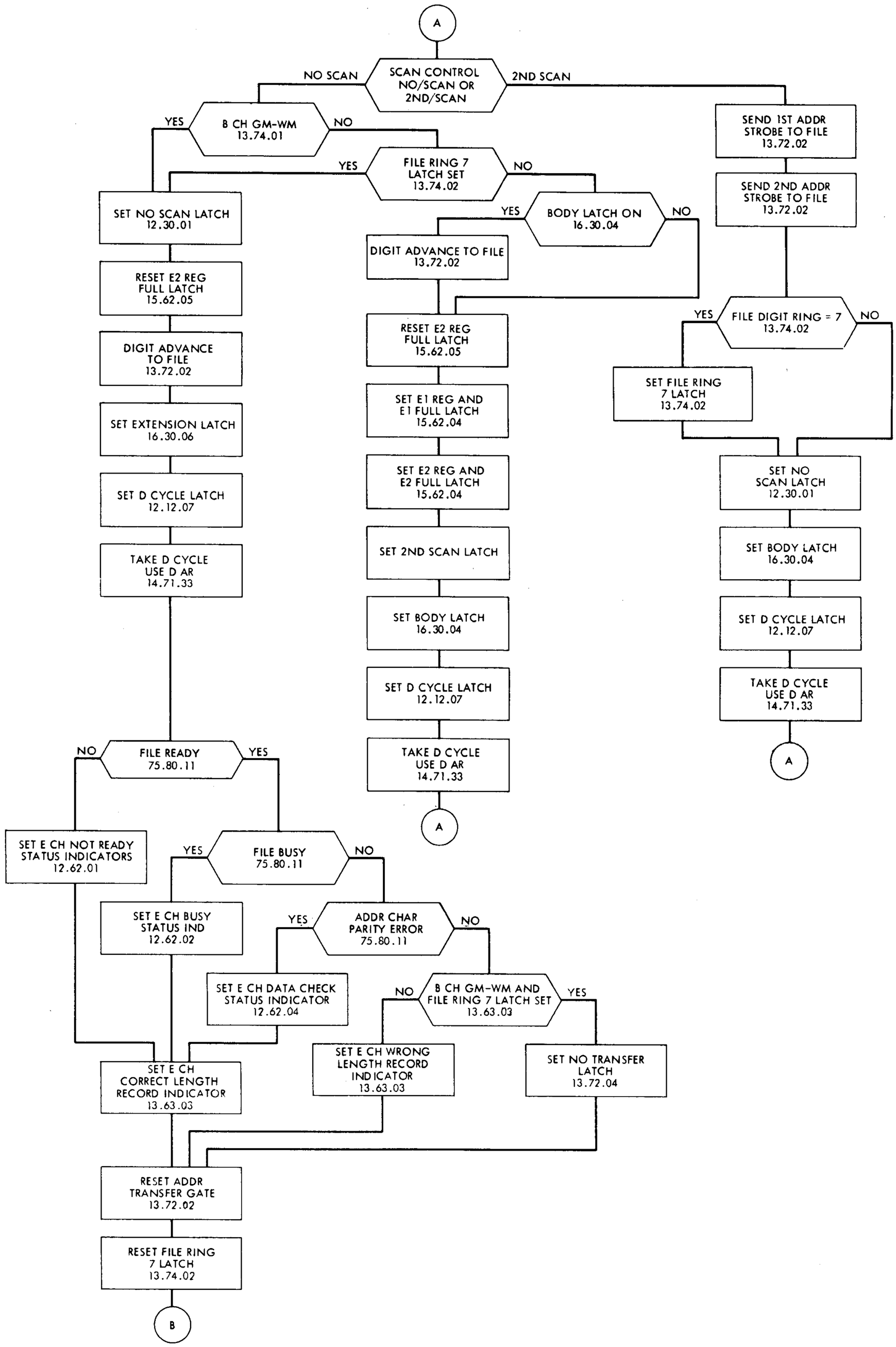



Figure 12-4. Address Transfer (2 of 4)

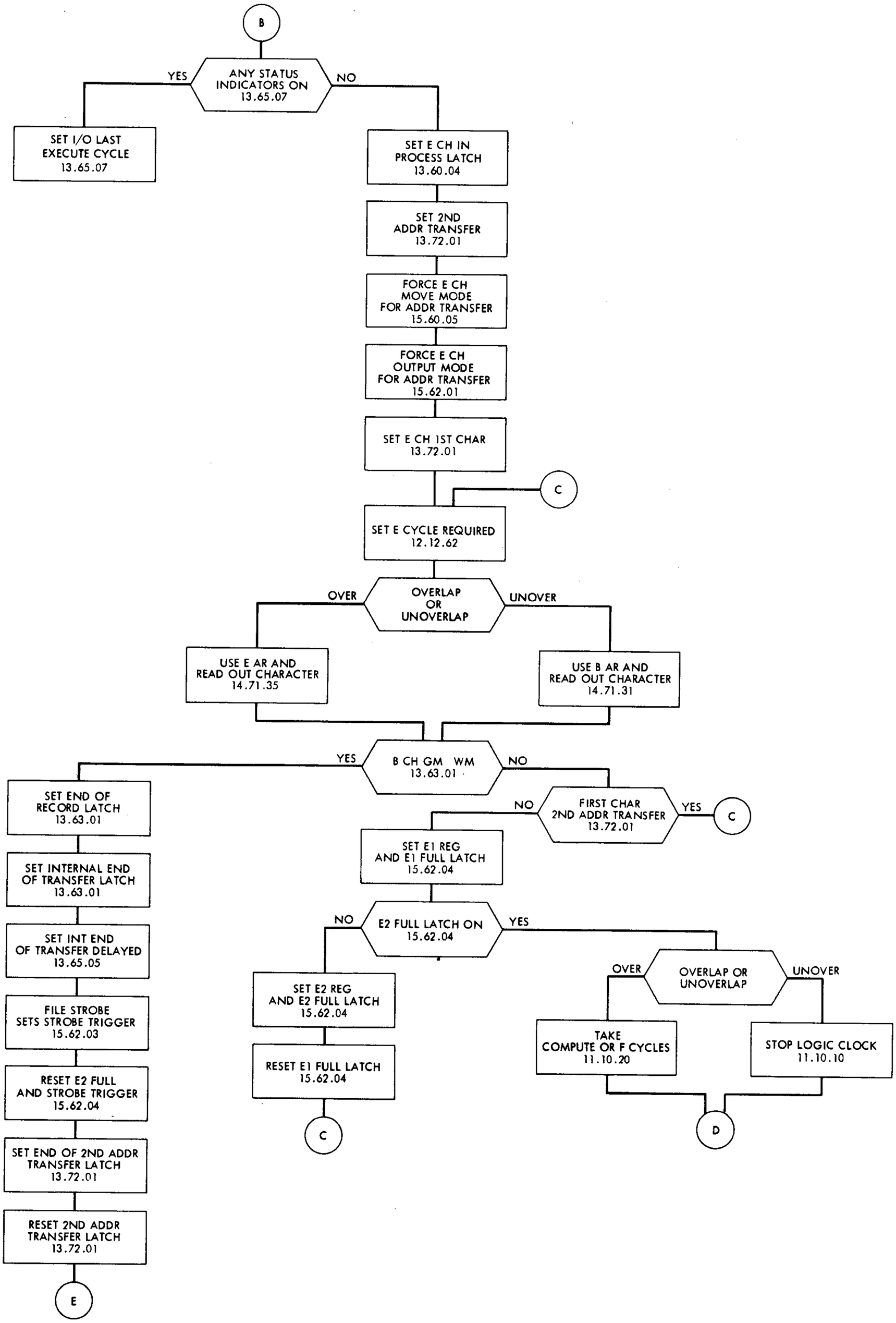



Figure 12-5. Address Transfer (3 of 4)

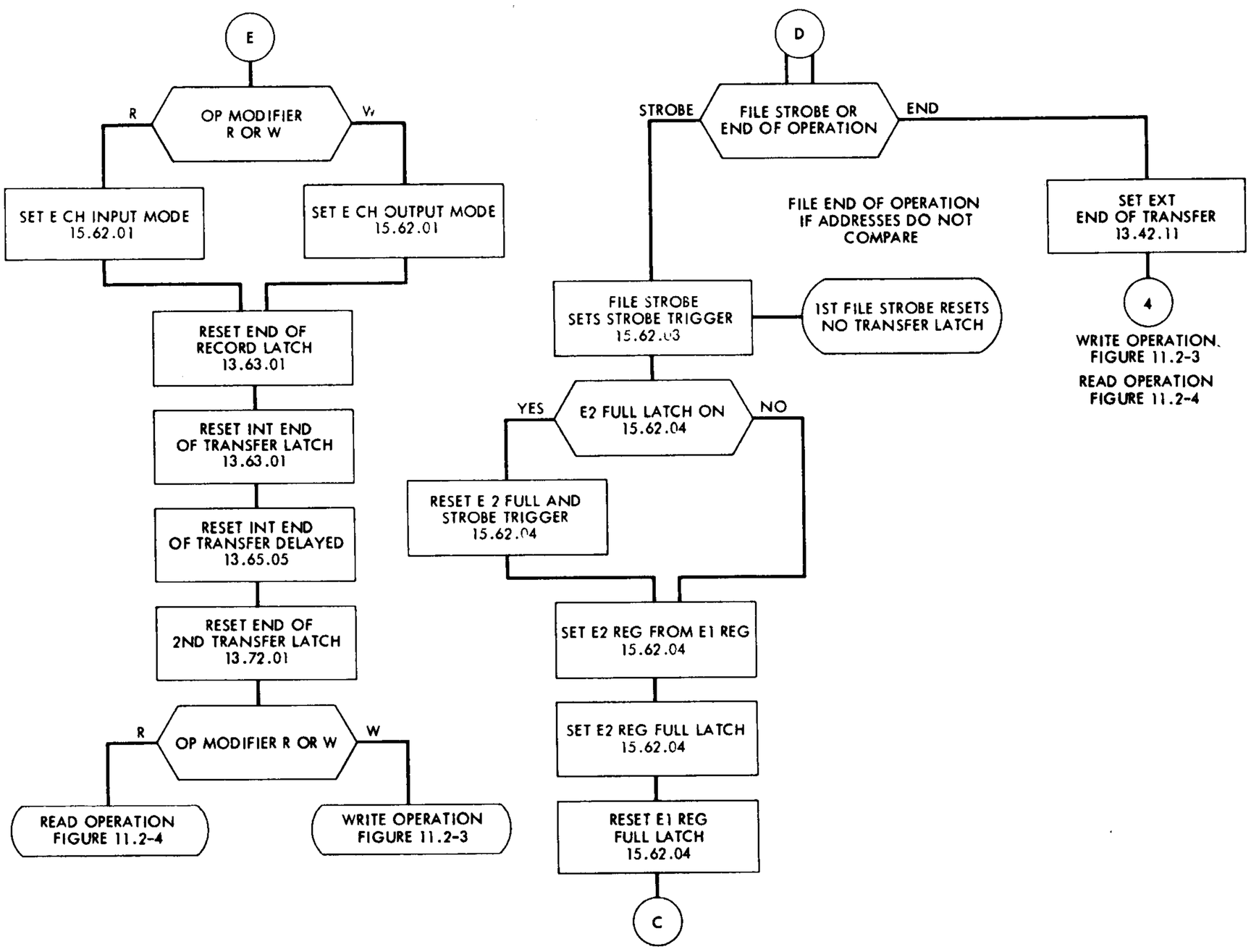



Figure 12-6. Address Transfer (4 of 4)

of the first four steps. These diagrams along with the sequence chart (Figure 12-7) are used to supplement the examination of this operation.

### *Instruction Cycles*

The basic objective during these cycles is to set latches in the 1410 and the file attachment unit to prepare for the 1405 read operation.

Following the 1410 I/O interlock check, move or load is sent to the file in accordance with the instruction M or L. The file is normally conditioned to operate in the MOVE mode; it therefore only samples the load line (75.81.01.1).

The E channel status indicators in the 1410 are then reset. The units position of the X-control field is then analyzed to determine the single record or full track requirement. In this case *single record* has been called for. *Single Record* is then ANDed with *file op* to set the single record latch in the ATU (75.81.81.1). The required *file op* line was previously established in the 1410 when the F in the instruction was analyzed.

If, at this point, a READ BACK CHECK has not been performed since the last write operation, the 1410 read back check indicator is set. The 1405 ATU is then reset by *RBCI reset* (75.81.91.1). *Master error stop* in the 1410 then stops the CPU. However, if a READ BACK CHECK has been made since the last write operation, the d-character is analyzed to determine read or write status. In this case read status is indicated; the 1410 input mode latch is set and *CPU read op* is sent to the 1405 ATU (75.81.01.1).

*CPU read op* is then gated by *CPU file op* (75.81.01.1). The resultant output (*CPU read op*) samples the single record and full track latches (75.81.81.1) to produce (in this case) *CPU read record.*

*CPU read record* is then transmitted to the 1405 FCU where it is powered and level set, and develops *read status* and *R/W select* (75.20.01.1).

The 1410 no scan and units latches are then set, the 1410 executes a d-cycle, and the *CPU address transfer gate* is sent to the 1405 ATU (75.80.21.0) and then to the FCU (75.20.01.1) to control the 1405 address transfer step.

## *Address Transfer*

The 1405 select and record registers (75.23.01.1 and 75.60.41.1) are reset at the end of every file operation. It is therefore necessary to transfer the record address from the 1410 to reselect the access, module, and record. The disk and track address relays are only reset during a SEEK operation and need not be reselected. However, the disk and track characters are read from 1410 storage during the address transfer step but nothing significant occurs in the 1405.

The address transfer step is described under objective No. 2 in Section 12 except for the transfer of the record character and the invalid address test.

### Record Character

When the 1410 reads out the record character the digit ring is advanced to digit 6 thus identifying the record character as digit 6. *Digit 6* then ANDS with *address transfer* (75.24.01.1). The character register is strobed by *address strobe delay;* the resultant output is then gated into the record address register by *digit 6* and *any access R/W select* (75.60.41.1).

### Invalid Address Test

An invalid address condition is established if either or both the selected access or the selected file are not safe at digit 1 time of the first address transfer step of a read or write operation. *Test valid address* (75.80.51.1) represents the access-unsafe and/or file-unsafe condition.

*Test valid address* is sampled by *address check strobe.* If the two concur, the invalid address latch is set. *Address check strobe* is *second address strobe* gated by *access not busy. Second address strobe* is developed immediately following *first address strobe.*

Therefore, the invalid address test is made immediately after the module character enters the 1405 select register.

## *Read Pre-Indelible Address AGC Bits*

The basic objective of this step is to set the gain of the read amplifier. With the gain set, the indelible address can be properly read. (See discussion of READ AMPLIFIER, Section 5.)

In addition to the basic objective, conditions are set up during this step to allow the indelible address to be read and transmitted to the ATU for comparison during the IA step. The following pulses and gates are therefore developed:

1. Start read/write pulse
   a. sector gate
   b. address gate
   c. AGC gate
2. Record pulse
3. Selected ready
4. Control counter pulses

### Start Read/Write

When *R/W select* was generated during the instruction cycles step, the 400 $\mu$s single shot was fired on 75.28.11.1.

The single shot prevents the start of the read operation until it times out. This circuit is necessary for two reasons. First, the 1405 is not ready to begin the read operation until after the address transfer step; it is impossible to predict when the correct record start pulse will occur. Second, during the address transfer step, the record head is selected. This selection causes noise to be fed into the read amplifier. The 400 $\mu$s delay provides a recovery time for the read amplifier. If the correct record pulse occurs during the address transfer step, it is blocked. The 400 $\mu$s single shot will have timed out by the time the disk array completes the next revolution allowing the read operation to continue.

When the 400 $\mu$s single shot times out, the start read/write trigger turns on provided a record or sector pulse is absent (5A, 5D-75.28.11.1). The trigger output is ANDed with *record pulse, selected ready,* and *not address transfer* to provide the start read/write impulse. *Start read/write* is then used to turn on the sector gate latch, the address gate latch AGC latch and to reset the digit ring.

The sector gate latch (75.04.51.2) provides a circuit during the data record portion to allow read data to be gated to the 1410. The address gate latch (75.29.01.1) provides a gate that defines the address portion of the record. The AGC latch (75.29.01.1) provides a gate that functions with the control counter to define the portions of the sector that contain AGC bits.

### Record Pulse

Figure 6-6 shows the development of a *record pulse* for access 0 in module 0. This circuit employs three special cards.

The AGM card supplies the emitter bias for the five AGL circuits. The AGL card provides the selection of a single-record head within the matrix. The AGJ card amplifies the induced signal from the selected head.

The selected access (0) and the selected module (0) are ANDed with *R/W select* to develop *access 0 R/W select* (75.30.01.1). This line is level set to –U and becomes the input to the AGM card (75.60.21.1) and forward biases T3. T3 conducts and supplies –6 v to the emitter circuits on the AGL cards. The base circuits for the AGL cards are supplied from the record address register. Thus, if the record address register contains 0/5, T7 is forward biased. As the permanent magnet

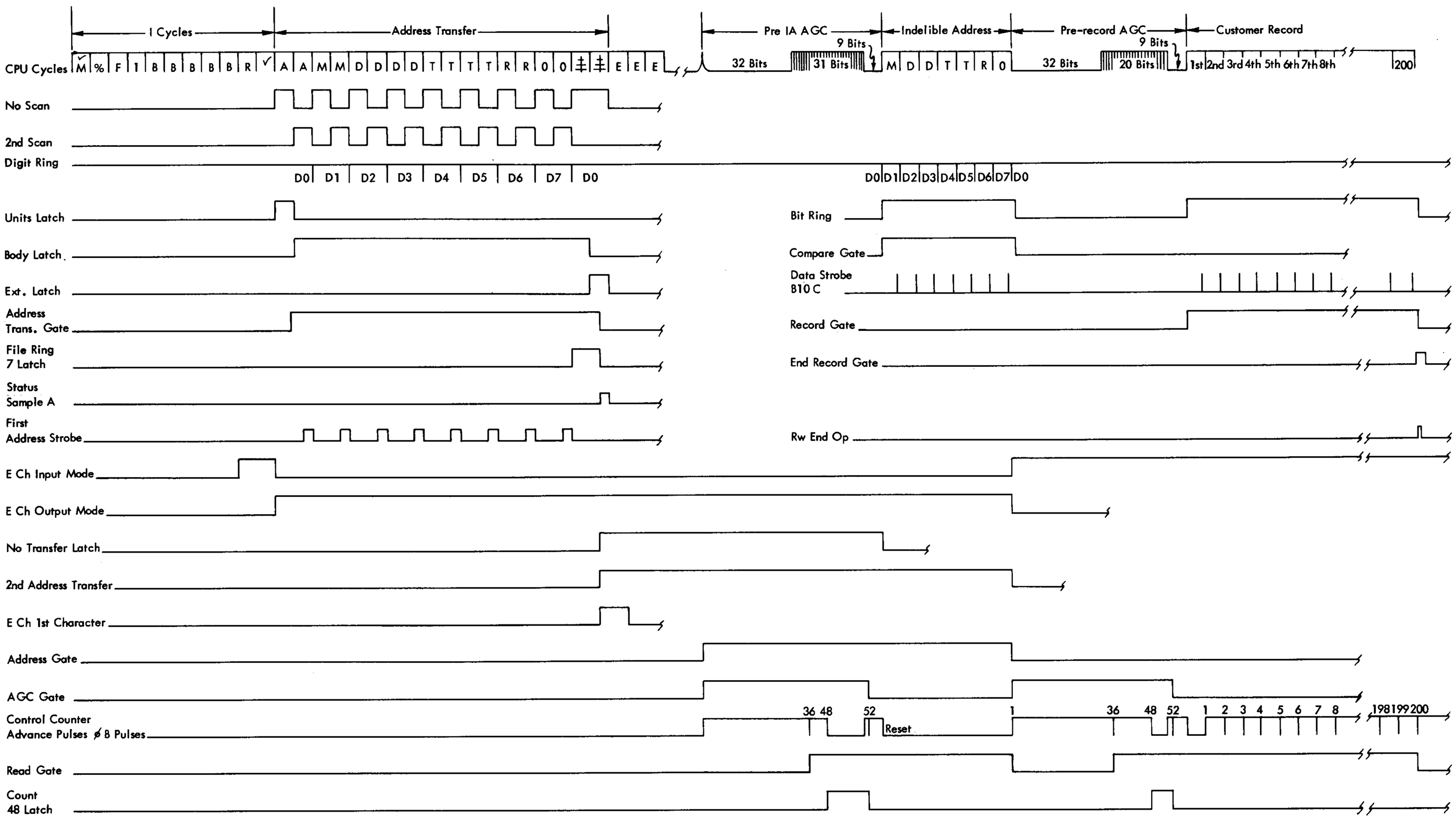



Figure 12-7. Read Operation – Sequence Chart

(located on upper dummy disk) passes the 0/5 record head, a signal will be induced in the 0/5 record head coil. This signal is reflected by T7 and forward biases the pulse amplifier. The transistors in the AGL card circuits, for the unselected heads, are reverse biased (0 v on the base leg).

If both *access 0 R/W select* and *record address* are down, all of the AGL card transistors are reverse biased; −14 v on the emitters and 0 v on the bases. The induced signal amplitude is not great enough to overcome this reverse bias.

### Selected Ready

The *start R/W* impulse should not be developed unless the selected access arm has the read-write head positioned at the desired location. This fact is determined by the *selected ready* line in the following manner.

Assume access 0 is to be used in module 0 (file No. 1). The selected access is ANDed with the selected module (75.23.11.1). The resultant *00 select* line is then ANDed with *access 0 ready* to produce selected ready (75.27.01.1).

Line *00 select* verifies that access 0 in module 0 has been selected. *Access ready* verifies two facts; (1) the preceding seek instruction was initiated, (2) the arm is located at the desired address.

Two latches are employed in the development of *access ready* (75.61.81.1). The latch at 3A is turned on at digit 3 time of a seek operation. It must be turned off before the latch at 4B can be turned on. Initiation of the seek operation is verified by *condition ready*. *Condition ready* then turns off. The latch at 4B can now turn on when the access arm reaches the desired location; determined by the pick of the arrival relay (Figure 6-7).

### Control Counter

The control counter provides the basic cycle control for all file operations (75.32.11.1). It divides and defines the portions of a record (sector), to be written or read, into the following groups:

1. From the beginning of the selected record to the beginning of the indelible address (pre-indelible address AGC bits).
2. From the end of the indelible address to the beginning of the data field (pre-record AGC bits).
3. The length of the data field.

#### CONTROL COUNTER ADVANCE

The control counter (75.32.11.1) is initially reset by a *+U X reset*. This reset is generated by the *file op* line during the instruction cycles.

During the pre-indelible address AGC bit time (pre-IA), the file clock is running. The phase Bs generated by the clock are gated by *AGC gate, read status,* and *not read gate* (4D-75.32.01.1) to produce the counter control advance pulses. The counter is advanced in this manner until it contains 36.

When the counter contains 36, the read gate latch is turned on (75.35.01.1). This permits the *read gate* to be available in time for the first significant I.A. bit. When the *read gate* is available, *not read gate* is inactive. Thus, the counter advance pulses are blocked by 4D. However, the counter must continue to count to provide the necessary controls during the remainder of this step. The phase B pulses are now gated by the output from 4F (75.32.01.1). The counter advances in this manner until it contains 48. The count 48 latch is then turned on (5G-75.32.21.1). When the count 48 latch is on, enough AGC bits have been read to properly set the gain of the read amp; the counter advance pulses are then blocked by 4F.

However, the counter must continue to advance until it contains 52. The absence of read data (AGC bits) provides these additional advance pulses (4H-75.32.21.1). When the counter contains 52, data has been absent for 4 bit times indicating that the read-write head is in the gap between the pre-I.A. AGC bits and the I.A. portion of the disk.

*The AGC gate* must now be dropped. *Count 52* ANDs with *read gate* to turn the AGC gate latch off (4C-75.29.01.1). *Count 52* is also used to turn the count 48 latch off (5H-75.32.21.1).

## Read Indelible Address (Second Address Transfer)

This step requires a second address transfer to compare the record address in cores to the indelible address read from the file. If the addresses do not compare, *file end op* is generated and no data is transferred.

Second address transfer begins after the CPU tests the status indicators following the first address transfer. If no status indicators are on, the CPU sets the second address transfer latch and *CPU address transfer gate* is again sent to the file (78.81.11.1).

Only seven address characters are transferred during the second address transfer. The first address character, access arm identification, is not transferred because it is not a part of the IA address and therefore must not be compared.

The GMWM following the address in cores is used to determine the end of the second address transfer. When the GMWM is sensed, conditions are established in the 1410 to set the end of second address transfer latch and to reset second address transfer.

The following 1405 circuit objectives are required:

1. Advance bit ring
2. Reset control counter

3. Advance digit ring
4. Establish compare gate
5. Compare the IA to the record address from storage
6. End the IA step (second address transfer)

### Advance Bit Ring

The bit ring is used to define the bit times within a character time. It is an 8-position ring (SCBA8421) during a move operation and a 9-position ring (SWCBA8421) during a load operation. High speed CTDL negative input triggers make up the ring (75.33.11.1).

The ring is initially reset when the file op latch turns on, during the 1401 I cycle step. The *not AGC gate* supplies another reset to ensure that the ring is reset just before it is used (75.38.11.1). The reset turns all triggers off.

The bit-S trigger must be turned on at the very beginning of the I.A. step. It must then be advanced during the I.A. step to gate the I.A. characters into the 1405 character register.

The bit S trigger and the bit S latch are turned on by the leading edge ($\phi$A) of the first bit read from the disk after count 52; this will always be a bit S (4E-75.33.01.1). The ring is then advanced by each succeeding $\phi$A if the bit ring advance latch is on (4B-75.33.01.1). The bit ring advance latch turns on with the first $\phi$D following the set of the bit S trigger (Figure 6-8).

During the I.A. step, the WM bit trigger (4B-75.33.11.1) is never used. The set to 4B is blocked at 2B. The C bit trigger is set by the output from 2E during the I.A. step. Each succeeding trigger is then set when the preceding trigger goes off.

### Reset Control Counter

The control counter is not used during I.A. step. At the end of the pre-I.A. AGC step, the counter contained 52. It is reset with a bit-S phase-C delayed pulse if *not record gate* is high (4H-75.31.11.1).

It is important to remember that the bit ring was initially reset with all bit triggers off. Therefore, the control counter could not be reset until the bit S trigger turned on.

### Advance Digit Ring

The digit ring is again used to define the address characters. However, it must now be advanced at 1405 speed because the I.A. characters are being transmitted to the CPU.

The digit ring is advanced by each bit S that occurs while the *address gate* is up (2F-75.21.11.1).

The access character (digit 0) is not recorded on the disk as a part of the I.A. However, it does exit at the original BBBBB address in core storage so it must not be compared. Therefore, the character compared is the module character (digit 1) found at address BBBBB plus one in core storage.

The first bit S that can occur to advance the digit ring is the bit S of the module character. The digit ring was reset to digit 0; it is therefore advanced to digit 1 by the bit S of the module character.

### Establish Compare Gate

The compare gate latch is turned on at bit 1 time of digit 1 if the file is not in a write address status and the *address gate* is up (75.81.71.1). The compare gate remains up throughout the IA step. It allows the comparison to be made in the ATU between the record address and the indelible address (75.81.41.1).

### Compare the IA to the Record Address from Storage

During digit 1 time the IA module character bits are strobed into the 1405 character register by the bit ring (75.36.01.1). They arrive as *standard read data* from 75.31.11.1. Each digit ring advance pulse resets the character register to allow each succeeding IA character to set up properly. See Figure 12-8.

When the bits enter the character register, the resultant character register bit lines and character register not bit lines condition one leg of each of the AND blocks on 75.81.41.1 and 75.81.51.1. The other leg of each AND block is conditioned by the CPU bit and CPU not bit lines from the E2 register. A double comparison is then made. If all bit lines logically compare, the resultant outputs from 75.81.41.1 and 75.81.51.1 AND with *comp spl 1* to turn the compare match 1 and compare match 2 latches on (75.81.61.1). *Comp spl 1* is a sample pulse developed at B1$\phi$C time if the compare gate is on (75.81.71.1). Note, the compare gate is turned on at bit 1 of digit 1 therefore the first *comp spl 1* available occurs at B1$\phi$C of digit 1.

Another sample pulse, *comp spl 2*, is generated at BS$\phi$C time (75.81.71.1) to test the status of the compare match 1 and 2 latches. If this pulse finds either one or both off, the no compare latch is set (75.81.61.1). Note, the first *comp spl 2* available occurs at BS$\phi$C of digit 2.

Compare match 1 and 2 are both reset at bit C time to allow each character to be compared as just described. However, the no compare latch can only be reset by a master reset.

If a comparing error does occur during the IA step, *no record found* and *not compare equal* are generated on 75.81.61.1. *No record found* sets the no address compare latch and sends a no record found indication to the 1410. *Not compare equal* halts the file operation by generating a 1405 end op signal (75.38.11.1).

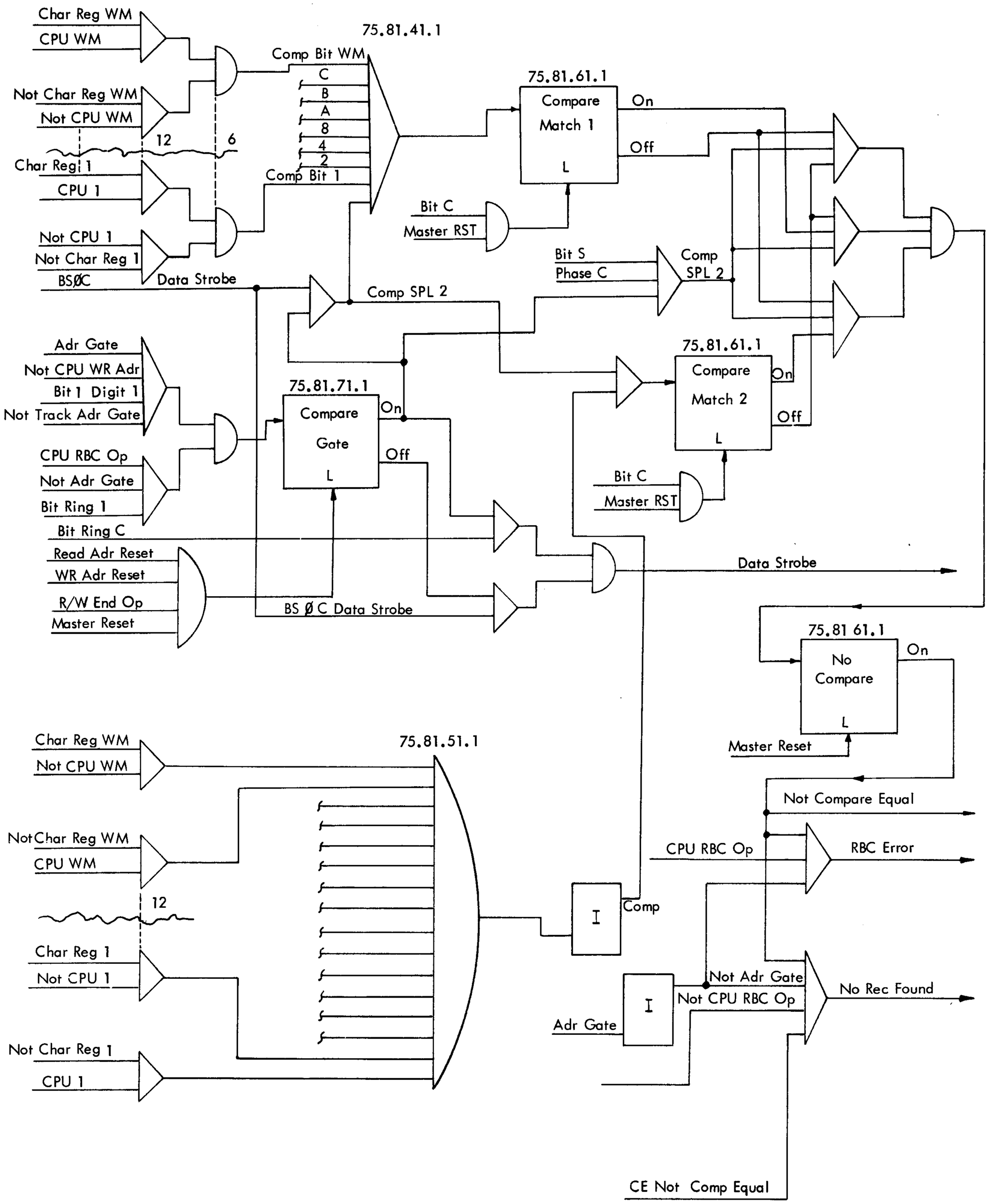



Figure 12-8. Compare Operation

### End the IA Step (Second Address Transfer)

The end of the 1410 second address transfer step is signalled when the 1410 senses the B channel GMWM following the last character of the record address.

The end of the 1405 IA step is signalled in the file by the development of *read address reset* (75.26.01.1). This pulse occurs at B4$\triangle\phi$C ($\triangle$ = delayed) time of digit 0 following the comparison of the compatibility character. It serves to develop the *—UX reset* lines (75.38.11.1) that in turn reset the bit ring (75.33.11.1) and the read gate latch (75.35.01.1).

*Read address reset* is also transmitted to the ATU to reset the compare gate (75.81.71.1).

## *Read Pre-Record AGC Bits*

The basic objective of this step is to set the gain of the read amplifier. With the gain set, the data-record can be properly read (see READ AMPLIFIER). In addition to the basic objective, conditions are set up during this step to allow the data-record to be read and transmitted to the CPU.

The following circuit objectives are required:

1. Develop AGC gate.
2. Develop read gate.
3. Reset AGC gate latch.

### AGC Gate

The AGC gate latch (75.29.01.1) again functions with the control counter to define the portions of the sector that contain AGC bits; in this instance, the pre-record AGC bits.

The latch is turned on by *read address reset* (75.26.01.1) and *phase C delayed. Read address reset* (previously developed) is B4$\triangle\phi$C of digit 0 when the address gate is up. Therefore, the AGC latch turns on at B4 delayed $\phi$C of digit zero following the comparison of the compatibility character.

### Read Gate

The read gate latch (75.35.01.1) is turned on to allow the intake of data from the read amplifier. The conditions required are *read status, AGC gate,* and *count 36.* It remains on until the end of the read operation.

The control counter (75.32.21.01) is reset by *read address reset.* It is then advanced to 36 in the same manner as described under the pre-I.A. AGC step.

### Reset AGC Gate Latch

The control counter advances beyond 36 as described under the pre-I.A. AGC step. When the counter reaches 48 the count 48 latch is again turned on (5G-75.32.21.1). When the count 48 latch is on, the counter is advanced by the absence of read data until it contains 52. At this point, data has been absent for 4 bit times indicating that the read-write head is located in the gap between the record AGC bits and the data record.

The AGC gate latch (75.29.01.1) is then turned off by *read gate* and *count 52. Count 52* also turns the count 48 gate latch off.

## *Read Data Record*

The basic objective of this step is to read and transmit the data record (200 characters) to the CPU. This step and the IA step are quite similar in operation.

To accomplish the data record step, the following objectives are developed:

1. Advance the control counter
2. Advance the bit ring
3. Develop record gate
4. Transmit read data to the CPU
5. End the operation.

Refer to Figures 12-9, 12-10, and 12-11 for 1410 operation during the examination of the following objectives.

### Advance the Control Counter

The control counter is reset following the pre-record AGC step by *set bit ring* S, if not in a write address status (4J-75.31.11.1).

*Set bit ring S* is developed when the set bit S latch is turned on. The latch is turned on at the end of the pre-record AGC step when the counter contains 52 (75.33.01.1). Refer to the READ I.A. step.

The counter is used, during this portion of the operation, to count the number of data-characters read. Therefore, it is advanced once at the end of each character time.

The counter advance pulses are generated on 75.32.01.1 .The *bit ring advance gate* is sampled at bit one time at 3B. This output is then ANDed with $\phi$B to produce the counter advance pulses (B1$\phi$B).

The *bit ring advance gate* is turned on at BS$\phi$D time (75.33.01.1); the bit S from the first character position on the data-record portion of the disk.

### Advance the Bit Ring

The bit ring is advanced with each succeeding phase A once the bit ring advance latch is on and the bit S trigger has been set (75.33.11.1).

The bit ring gates the read data into the 1405 character register, serially by bit.

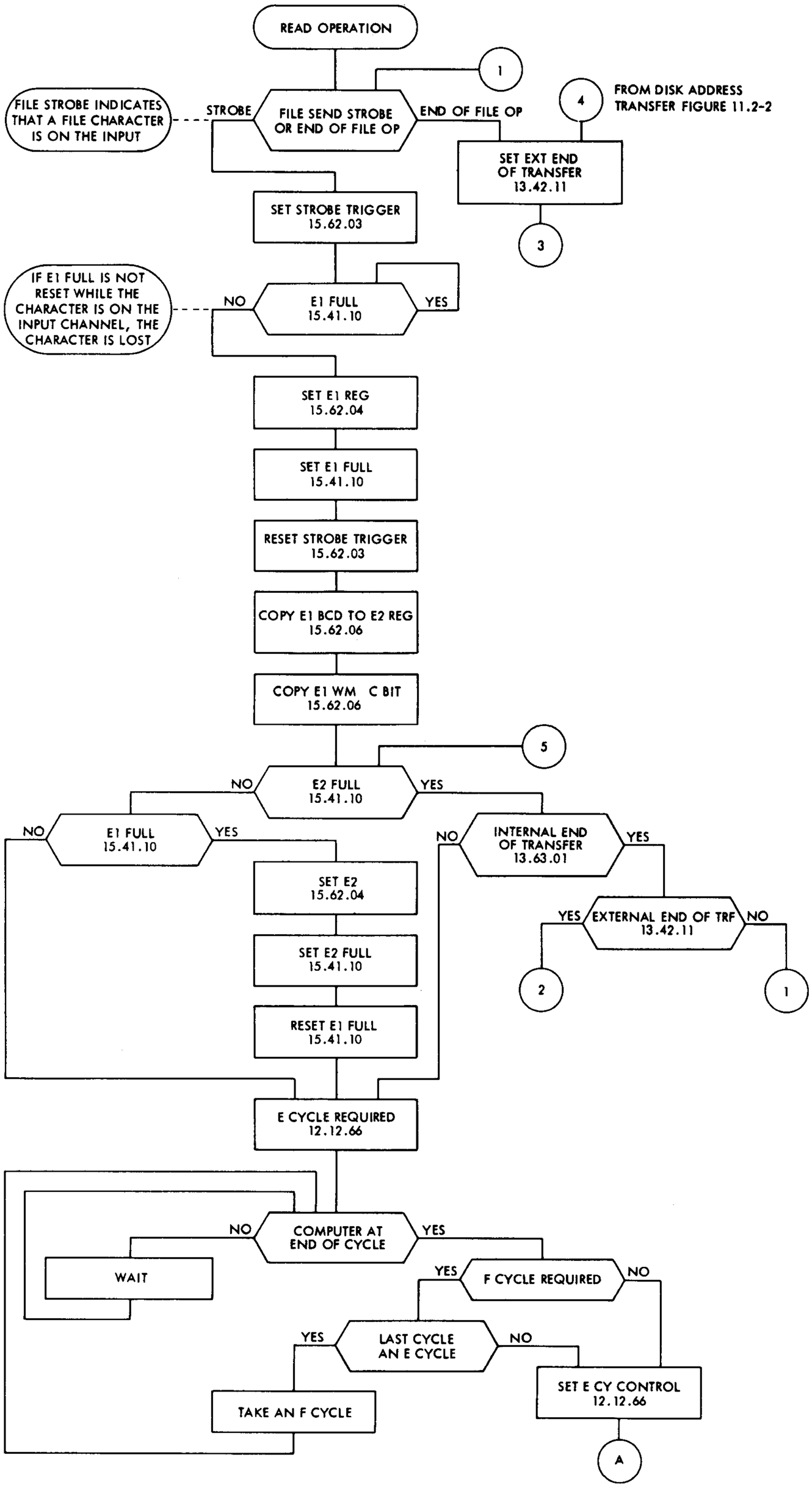



Figure 12-9. File Read Operation (1 of 3)

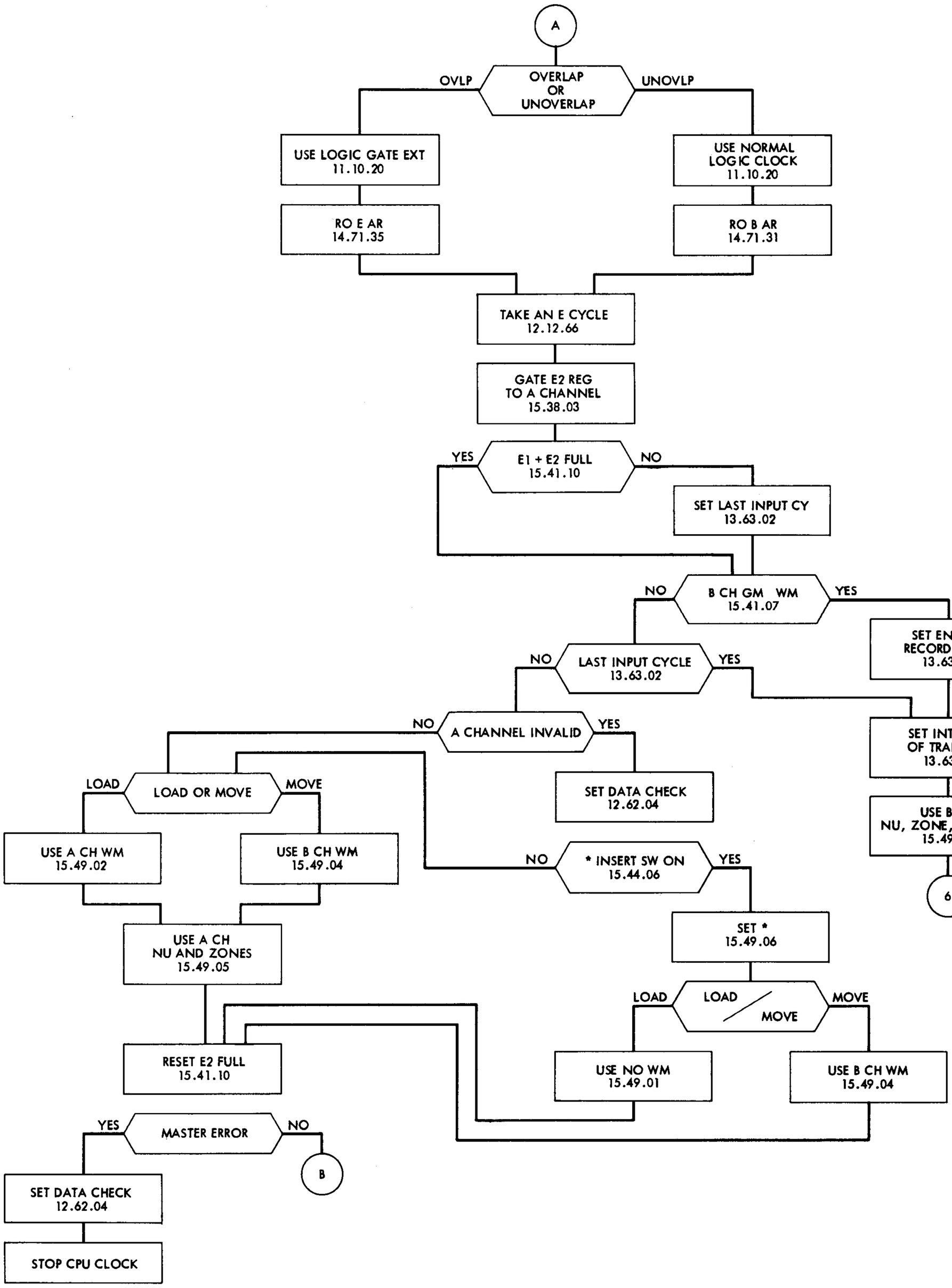



Figure 12-10. File Read Operation (2 of 3)

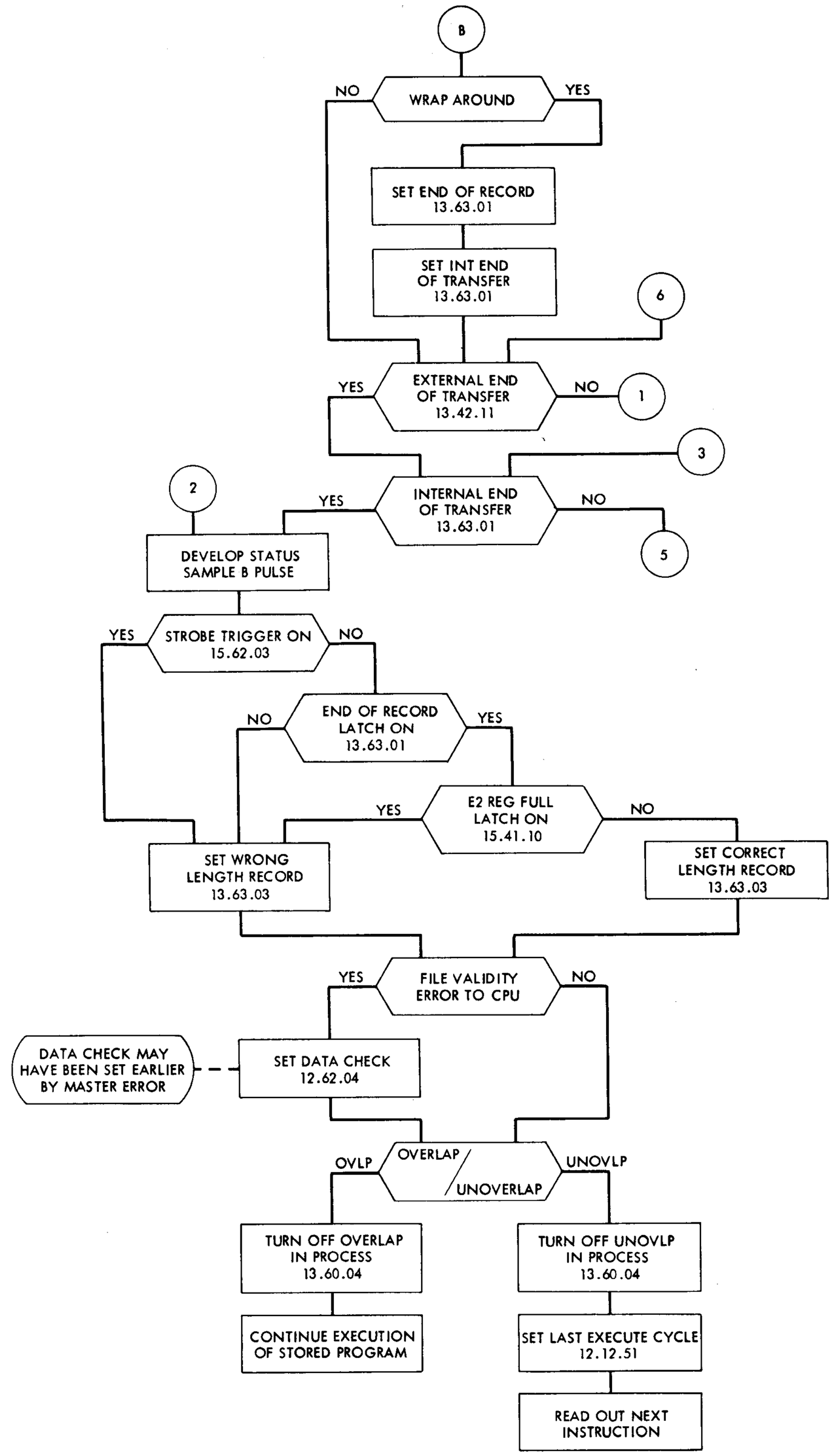



Figure 12-11. File Read Operation (3 of 3)

### Record Gate

The *record gate* is used to define the data-record portion of the disk (75.32.01.1). It is a combination of *bit ring advance gate* and *not address gate*. An examination of the bit ring advance latch (75.33.01.1), shows that, once on, it remains on until the end of the operation. Therefore, the *record gate* is available for 200 characters during the data-record portion of the operation.

### Transmit Read Data to the CPU

Read data enters the 1405 character register serially by bit and therefore cannot be transmitted to the CPU until the end of each 1405 character time. The end of a character is recognized at B1$\phi$C time; by this time the entire character is stored in the character register.

The transfer of data to the CPU is therefore controlled by *data strobe* developed at B1$\phi$C time from 75.31.11.1.

The $+U$ *data strobe* is gated by the OFF side of the compare gate latch in the 1405 ATU (75.81.71.1). The resultant $+U$ *data strobe* is then level set and sent to the CPU where it indicates that a file character is on the input channel. When the strobe is received, the character is placed in the proper data register. Each subsequent character is transferred in the same manner.

### End of Operation

The end of the 1405 read operation is determined by the control counter. During the data record step, the counter is advanced one position for each character time. When it contains 200 (B1$\phi$B of last character) the end-record latch is turned on (75.32.31.1). The resultant end record gate line is then ANDed with BS$\phi$C to turn the read gate latch off; this occurs at BS$\phi$C of the 201st character (75.35.01.1).

The *end record gate* also functions with BS$\phi$C to generate a 2.5 $\mu$s *R/W end op* pulse (75.38.01.1). This 2.5 $\mu$s pulse then becomes the X and Z resets (75.38.11.1) and it also develops *end op, file end op* and *CPU end op* on 75.38.01.1.

The *CPU end op* is sent to the 1410 through the ATU to signal the 1410 that the last file character has been transferred (75.81.21.1). This signal sets the external end of transfer latch in the CPU. The CPU stores the character from the data register and senses a GMWM. The GMWM indication causes the end of record and internal end of transfer latches to be set. If the GMWM is not sensed on this last cycle, only internal end of transfer is set and a wrong length record indication is established at status sample B time. The wrong length indicator in the file is also turned on (75.80.51.1). The operation is then terminated.

### *Read Single Record — Load Op (L%F1BBBBBR)*

The purpose of this instruction is to allow the 1405 to read data from the file that contains WM's. The data flow is the same as the data flow during a *move op*. However, *end op* is generated after 176 characters instead of 200. This difference is due to the space required during a load op by the recording bit configuration of SWCBA8421.

The following two circuits require additional controls to allow the 1405 to accomplish this instruction.

1. Bit Ring
2. Control Counter Decode

### Bit Ring Operation

The bit ring must provide a bit time for the WM (SWCBA8421) during the data-record step. However, it must not include this bit time during the I.A. step (I.A. is always recorded in an SCBA8421 configuration).

During the I.A. step, the *address gate* is up. When the bit ring advance pulse turns the bit S trigger off (75.33.11.1), pin F (4A) goes to $-$T. This output is then gated through 2E and turns the C bit trigger on. The WM trigger was bypassed because the inputs at 2B are not satisfied when the *record gate* is down. Thus, the bit ring advances in the 8-bit mode (SCBA8421) during the I.A. step.

During the data-record step, the *address gate* is down and the *record gate* is up. When the bit S trigger turns off, pin F (4A) is gated through 2B and the WM trigger is turned on. The next advance pulse turns the WM trigger off. The C bit trigger is then turned on through 2D. Thus, the ring advances in the 9-bit mode (SWCBA8421) during the data-record step.

### Control Counter Decode

The control counter advances as previously explained under READ SINGLE RECORD MOVE OP. However, the end-of-record latch must be set at count 176 instead of count 200.

A decode of count 176 is provided at 5B when the $-T$ *load op* line is active. Thus, the end-of-record latch is set at count 176 during a load op.

## Write Single Record Operation

A write single record operation is called for in the MOVE mode by the instruction M%F1BBBBBW. This instruction causes data to transfer from cores to the 1410 E1 register whenever the E1 register is empty. If the E2 register is empty the data is transferred from the E1 register to the E2 register.

The file samples the output lines from the E2 register and sends a strobe pulse to the CPU. The strobe pulse

indicates that the file has accepted the character from the E2 register the computer then transfers a new character from storage.

When the CPU senses the GMWM after the last character has been read out of storage, internal end-of-transfer is sent to the 1405 ATU to prevent the entry of any additional data into the 1405 character register (75.80.91.1).

The 1405 write operation is performed during the following sequential steps:

1. Instruction cycles
2. Address transfer (first)
3. Read pre-indelible address AGC bits
4. Read indelible address
5. Write pre-record AGC bits
6. Write data record

The logic flow diagrams (Figures 12-12 and 12-13) and the sequence chart (Figure 12-14) are used to supplement the examination of this operation.

A great deal of the WRITE SINGLE RECORD operation is identical to the READ SINGLE RECORD operation. Therefore, comparisons are made to the description of the steps performed during the read operation; differences are then explained.

Address transfer, pre-IA AGC, and the read IA steps are identical for both the read and write operations. Refer to the READ SINGLE RECORD operation for an explanation of these steps.

## *Instruction Cycles*

The objectives for this step are identical to those described under READ SINGLE RECORD with one exception; *write status* must be established instead of *read status.*

### Write Status

During the instruction cycles when the d-modifier is analyzed (Figure 13-1) —*C CPU write op* is sent to the 1405 ATU where it is gated by *CPU file op* to become —*U CPU* write op and —*T CPU write op* (75.81.01.1) —*T CPU write op* is then transmitted to 75.81.81.1 where it samples the record and track op latches. Single record has been called for by the instruction, therefore, *CPU write record* is developed and sent to the FCU where it develops *write status* and *R/W select* (75.20.01.1).

## *Write Pre-Record AGC Bits*

During a write operation the pre-record AGC bits are always rewritten. The amplitude of the AGC bits and the data-record bits should then be the same; they are written with the same head and at approximately the same time.

The gain of the read amplifier is established by the AGC bits. Because the amplitude of the data-record bits is a reflection of the AGC bits, the gain of the read amplifier is properly set for reading during the data-record step.

*Objectives*

1. Develop AGC gate.
2. Advance control counter.
3. Develop write gate.
4. Develop write AGC gate.

### AGC Gate

The *AGC gate* is used, at this time, to define the portion of the sector that is to be written with AGC bits (75.29.01.1). The AGC latch is turned on by $\phi C$ *delayed* and *read address reset. Read address reset* (75.26.01.1) is up at B4$\triangle\phi$C ($\triangle$ = delayed) of digit zero during address gate time. *Read address reset* develops the *X reset* lines to reset the bit ring, address gate latch, control counter, and read gate latch.

### Control Counter

The control counter, at this time, operates in conjunction with the *AGC gate* to define the portion of the sector to be written with AGC bits.

With the *address gate* down, and the *AGC gate* up the counter advances with each $\phi$B impulse (4A, 6E-75.32.01.1). When it contains 60, the AGC latch is turned off (75.29.01.1) blocking any further counter advance pulses (4A-75.32.01.1). The counter is reset at the beginning of the data-record step when the set-bit S latch turns on (4J-75.34.01.1).

### Write Gate

The write gate (75.34.01.1) conditions the write amplifier (75.61.61.1) to allow the selected read-write head to draw write current (see BASIC READ WRITE CIRCUITS).

The write gate latch is turned on by *read address reset* and delayed $\phi$C. Therefore, the *write gate* is up at B4$\triangle\phi$C at the end of address transfer time. The latch remains on until the last character is written during the data-record step.

### Write AGC Latch

The write AGC latch (75.34.01.1) is used to bring up the *write data* line. The *write data* line then gates $\phi$Cs to the write amplifier (75.34.11.1). A series of $\phi$C impulses are then recorded on the disk during the time the write AGC latch is on.

The latch is turned on by *count* 32 if the *write gate* and the *AGC gate* are up (3C). It is turned off at count 52 (4A). Therefore, during the time the write AGC latch is on, 20 AGC bits are written.

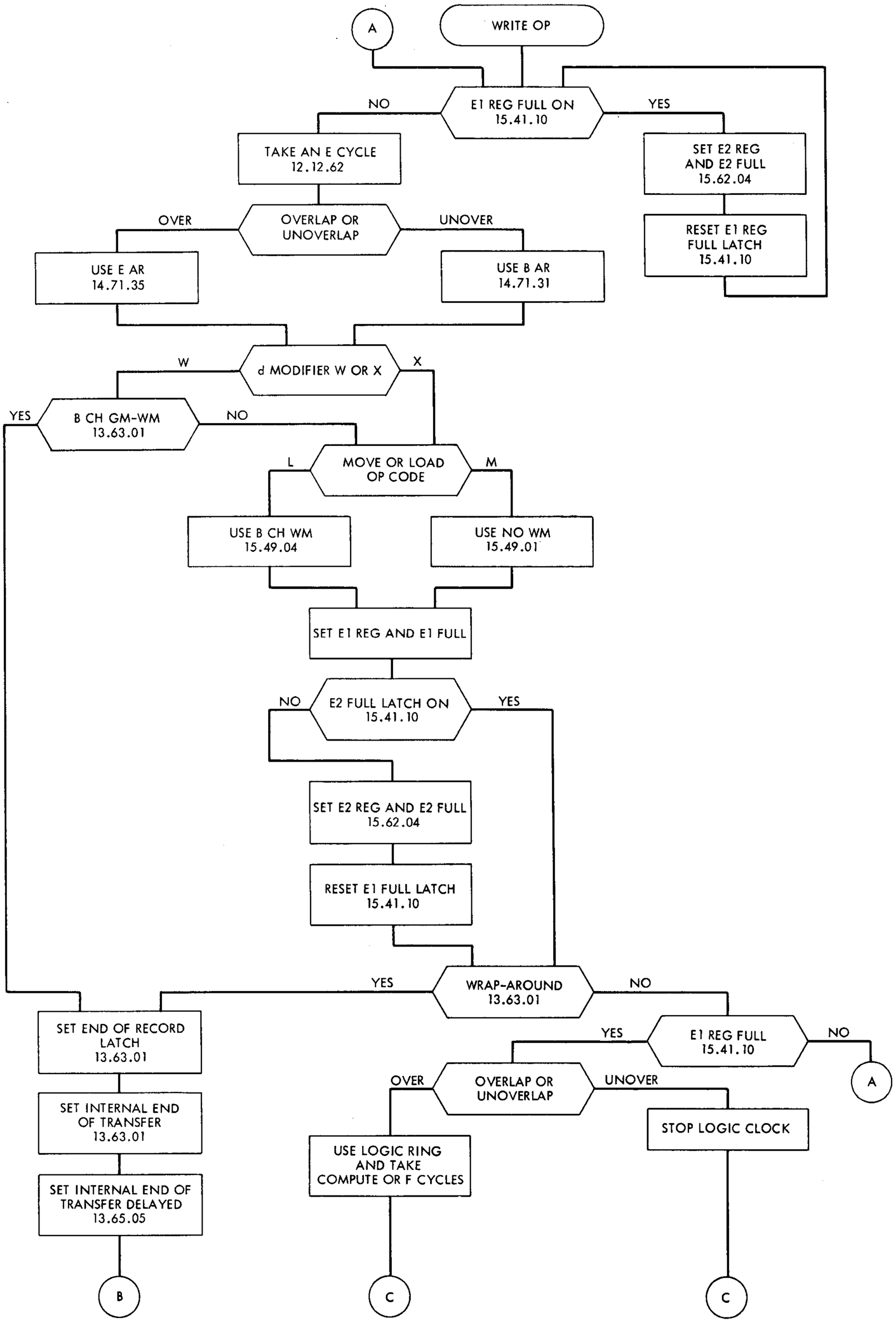



Figure 12-12. File Write Operation (1 of 2)

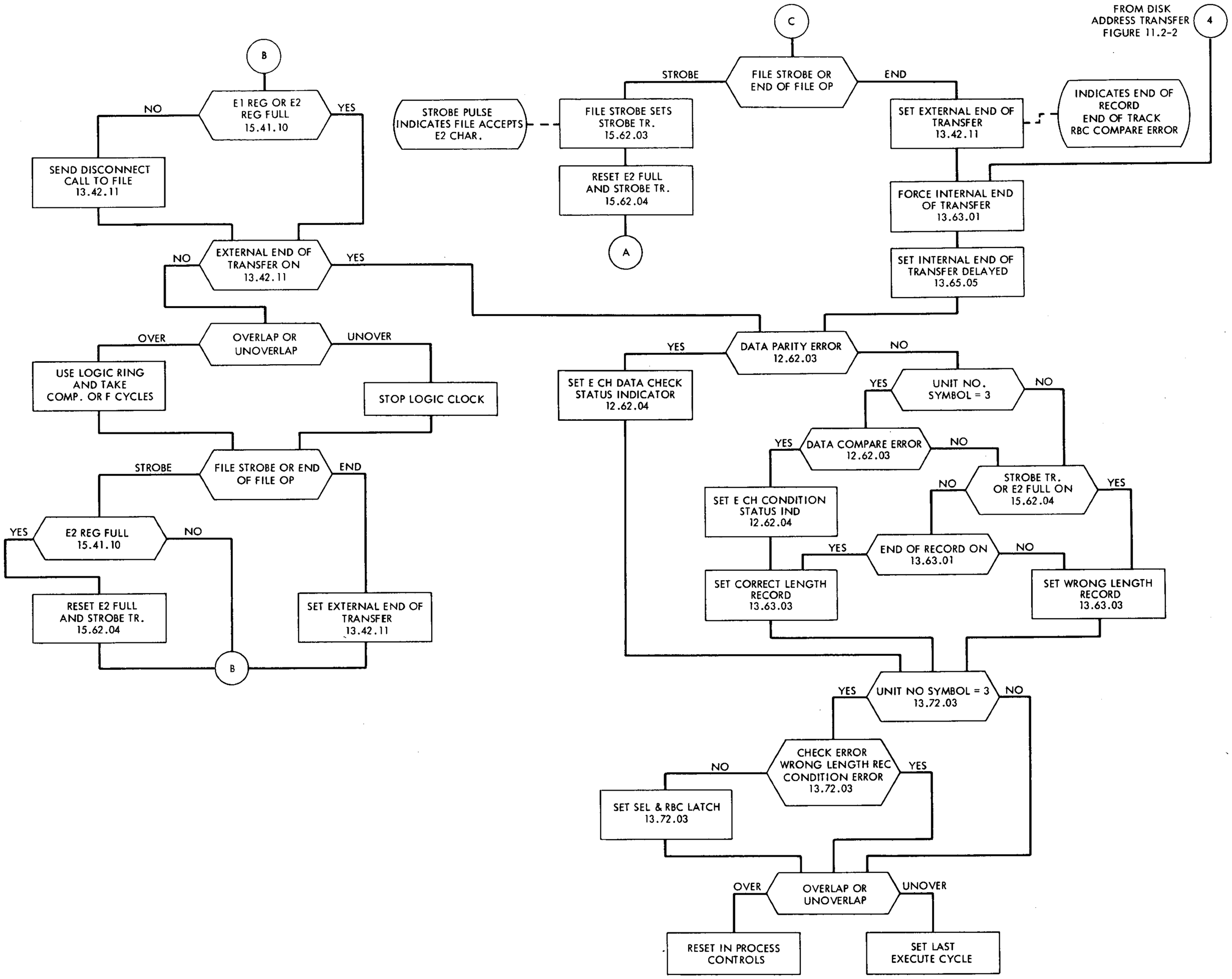



Figure 12-13. File Write Operation (2 of 2)

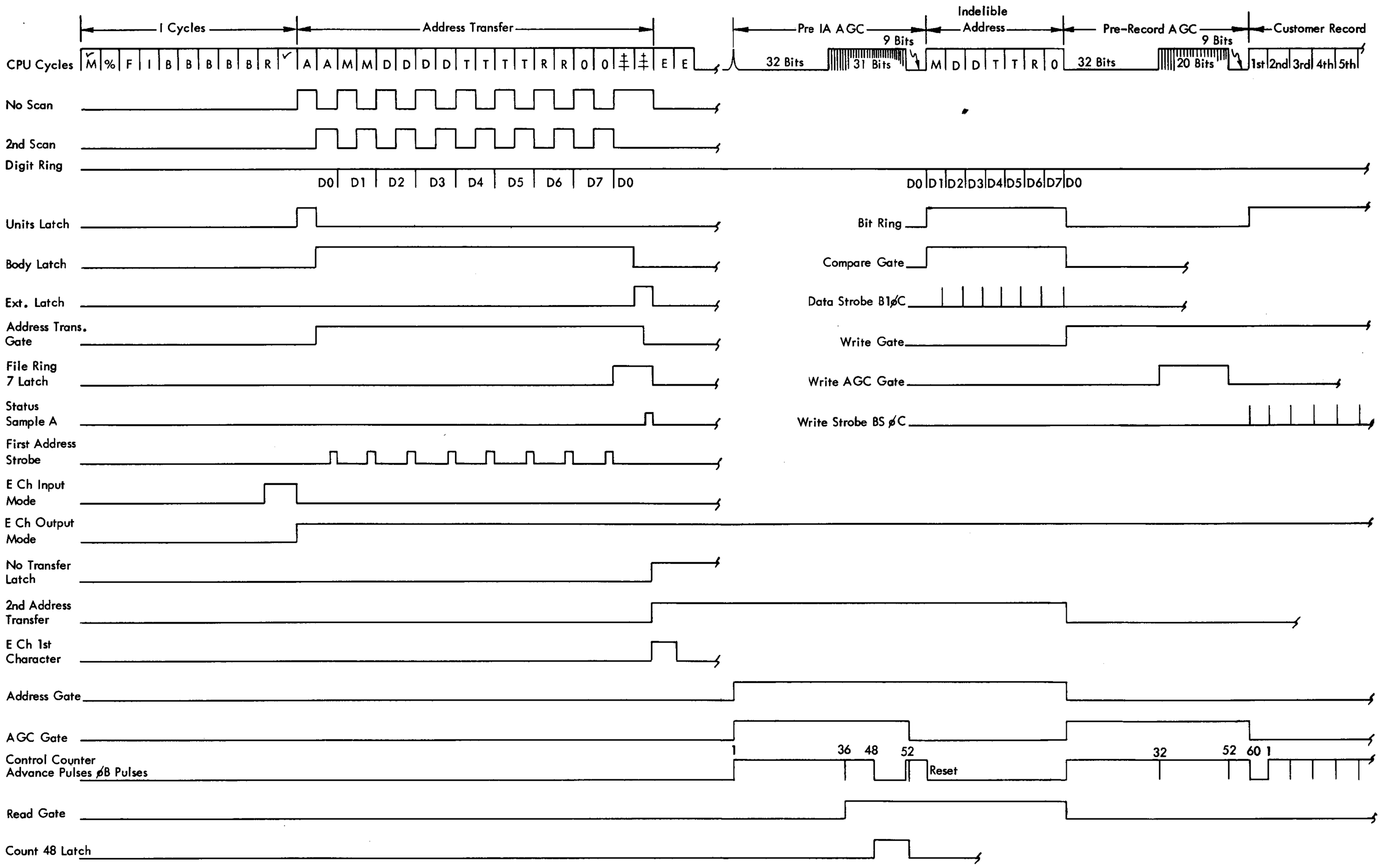



Figure 12-14. Write Operation – Sequence Chart

## *Write Data Record*

The first character to be written on the data record portion of the record is stored in the 1410 E2 register immediately following the IA comparison. This character and each subsequent character of the data record must be transmitted to the 1405 character register where they are "serialized" by the bit ring and become write data.

*Objectives*:

1. Set and advance the bit ring
2. Reset and advance the control counter
3. Develop the record gate
4. Develop write data
5. Send data strobe to 1410
6. End the operation.

### Set and Advance the Bit Ring

The bit ring is used to "serialize" the 1405 character register output. The ring must, therefore, be allowed to run throughout the data-record step.

The set-bit S latch is turned on at count 60 with *delayed $\phi C$* (2H-75.33.01.1). The bit ring advance gate then comes up at BS$\phi$D. Phase As are gated by the *bit ring advance gate* and become the *bit ring advance pulses*. Therefore, the first advance pulse occurs at BC$\phi$A and turns the bit C trigger on. The ring continues to advance with each succeeding $\phi$A.

### Reset and Advance the Control Counter

The control counter is reset when the set-bit S latch turns on (4J-75.31.11.1). It is then advanced, once each character time (B1$\phi$B), to count the number of characters written (3B-75.32.01.1).

### Record Gate

The *record gate* identifies the portion of the sector reserved for the customer's record. It comes up with the *bit ring advance gate* (2B) and remains up until the bit ring advance latch is turned off by *end op* (2B-75.32.01.1).

### Write Data

The first character to be written enters the 1405 character register (75.36.01.1), from the CUP when a *write strobe* is developed at BS$\phi$C time (4C-75.31.11.1).

When the bit ring strobes the output from the character register, serial data is placed on the write data line. Bit Ss are then inserted from 5H (75.34.01.1). The resultant write data line is then ANDed with the *write gate* (5E-75.34.01.1). *Write data,* as an output from 5D, is then ANDed with the selected module and is strobed by $\phi$Cs (3A-75.34.11.1). The resultant *$\phi C$ write data* is then available as an input to the write amplifier (75.61.61.1).

### Send Data Strobe to 1410

The 1405 generates *data strobes* at each bit C time during the time that the write gate is up to signal the 1410 that the previous character has been accepted. The 1410 then transfers the E1 register to the E2 register and reads the next character out of storage to the E1 register.

The bit C *data strobes* are generated on 75.31.11.1 and then transmitted to the ATU where they are gated by the OFF side of the compare gate latch (75.81.71.1). The resultant data strobe is then level set and transmitted to the 1410 (75.81.21.1).

In summary, each character to be written (except the first) enters the 1410 E2 register at 1405 bit C time. It then enters the 1405 character register at BS$\phi$C time and is immediately "serialized" beginning at BC$\phi$A time.

### End the Operation

The write operation is ended in the same manner as the read operation. Refer to objective No. 5 under READ DATA RECORD.

## *Write Single Record — Load Operation*

The purpose of this instruction is to allow the 1405 to record WM on the disks when WM's are encountered along with the write data. The functional objectives are the same as required for write single record move op. However, *end op* is generated after 176 characters have been written instead of 200. This difference is due to the space required by the recording bit configuration of SWCBA8421 during a load op.

Two circuits require additional controls to allow the 1405 to accomplish this objective. They are the bit ring and the control counter decode circuits.

These additional controls are discussed under READ SINGLE RECORD-LOAD OP.

## Read or Write Full Track

The functional objectives for read full track or write full track are the same. For this explanation, assume that a read full track operation is called for (M%F2BBBBBR).

The instruction calls for 1000 characters to be read from five records on the same track. The five records are read from the same side of the disk. Reading may begin at any one of the five records; the next four records are then read in order.

The data flow and basic objectives are the same as those required for a R/W single record operation. However, the indelible address of the first record (selected record) is the only one compared.

*Objectives*

1. Establish full track operation.
2. Transfer only the first record address.
3. Develop start R/W for each of the five records.
4. End the operation after 200 characters of the fifth record.

### Establish Full Track Operation

During instruction read out, the 2 in the units position of the X-control field is analyzed. *CPU track op* is generated and transmitted to the ATU where it is gated by *CPU file op* before it sets the track op latch (75.81.81.1). CPU read or write track is then determined by the d-modifier. In this case *CPU read track* is established allowing *track status, read status,* and *R/W select* to be developed on 75.20.01.1.

### Transfer Only First Record Address

The first record address is transferred in the normal manner (see R/W SINGLE RECORD operation.)

When the last character of the first record has been read, *end op* is generated and the X and Y reset lines are activated (75.38.01.1 and 75.38.11.1). However, *CPU end op* is blocked preventing an external end of transfer in the 1410.

### Develop Start R/W for Each of the Five Records

Start R/W for the first record is developed in the normal manner. That is, the start R/W trigger turns on from 5A (75.28.11.1) when the 400 $\mu$s single shot times out. The first record pulse that occurs from the selected record is then gated through 6C to develop the first *start R/W* pulse. The first record is then handled in the manner described under READ SINGLE RECORD.

The second record is identified by the first sector pulse following the selected record pulse. As long as the start R/W trigger is on, each sector pulse in turn develops a start R/W pulse through 6C. The start R/W trigger remains on until *file end op* is generated for the fifth record. (The development of *file end op* is covered later.)

The record address of the first record remains in the select register throughout the operation. Therefore, the indelible address comparison must be suspended for each of the four records following the first record. This is accomplished by preventing the development of the compare gate during the IA portion of the last four records. In addition, the development of data strobes is prevented during the IA portion of the last four records.

The set to the compare gate latch is blocked by the loss of *not track address gate* (75.81.71.1). *Not track address gate* is blocked when the record counter contains one or more (75.31.11.1). This condition also prevents the development of data strobes during address gate time.

The record counter is a binary counter; when reset, all of the triggers are off. During a full track operation the counter is advanced by *R/W end op delayed* (75.28.11.1). This pulse occurs 2.5 $\mu$s after BA$\phi$C of the 201st character (75.38.01.1).

### End the Operation

The *R/W end op* generated at the end of the fifth record (75.38.01.1) bring up *file end op* to cause an external end of transfer status to be set in the 1410. The development of *file end op* is accomplished by developing *track end op* in the following manner.

When the *R/W end op* trigger is turned on for the fifth record the record counter contains four. (The counter advance pulse for the fifth record occurs 2.5 $\mu$s after *R/W end op.*) *R/W end op* is then immediately gated through 6H (75.28.11.1) to develop *track end op.*

## Write Check Operation

The basic objective of this operation is to cause the data-record portion of a sector to be compared, character by character, with the data in core storage from which it was written.

As previously explained, a write-check operation must follow a write operation. No other file operation can be executed until the write-check operation is performed. The operation is initiated by the instruction M%F3BBBBBW, if the data was written in the MOVE mode. If the data was written in the LOAD mode, the operation is initiated by the instruction L%F3BBBBBW. In either case, the BBBBB portion of the instruction must be the original core address of the recorded data.

The instruction is performed using the same steps as described for READ SINGLE RECORD OPERATION. However, instead of storing the information read during the data-record step in cores, it is merely compared.

The following objectives are modifications to the READ SINGLE RECORD operation to allow the execution of the write check instruction:

*Objectives*

1. Establish read status.
2. Establish compare gate during the data-record step.

#### Establish Read Status

During 1410 instruction read out, the 3 in the X-control field is analyzed and *—C CPU RBC op* is sent to the 1405 ATU where it is level set to become *CPU write check.* When the d-modifier is analyzed, *CPU write op* is sent to the ATU where it gates *CPU write check* to develop *—T CPU RBC op.*

It must be determined at this point whether a single record or a full track is to be checked. The record op and track op latches are not reset following a write operation; therefore, whichever one was set, during the preceding write operation, gates *CPU RBC op* to develop either *CPU read record* or *CPU read track* (75.81.81.1). Note, *CPU write op* is prevented from developing *CPU write record or write track* by *—T not CPU RBC op.*

*CPU read record* or *CPU write check* develop *read status,* and *R/W select* on 75.20.01.1. Note, if a full track were to be checked, *CPU read track* would develop *track status.*

#### Establish Compare Gate During the Data-Record Step

When *—T CPU RBC op* is developed as previously explained, the following conditions are provided:

1. A reset to the write check interlock latch at digit 7 time of the first address transfer step (75.80.31.1).
2. A set to the compare gate latch after the second address transfer step (75.81.71.1).
3. A gate to allow a possible comparing error to be indicated as an RBC error, after the IA is compared (75.81.61.1).

## Write Address Operation

The write address operation is performed only under CE supervision. The instruction M%F4BBBBBW calls for a write address operation. However, a key-lock switch on the CE test panel must be operated before the instruction can be executed. The indelible addresses are originally loaded at the factory, therefore, the write address operation is only used if a particular address is destroyed.

A seven character address is written on the previously selected record when the write address instruction is executed. The disk addresses are predetermined by the physical location of the disks on the disk array.

The operation is performed during the following sequential steps:

1. I-cycles
2. Address transfer
3. Write pre-IA AGC bits
4. Write IA and end the operation.

### *I-Cycles*

The basic objective of this step is to condition the file for a write address operation by establishing *write address status* in the FCU.

During instruction read out when the 4 in the units position of the X-control field is analyzed, *CPU write address* is sent to the file ATU (75.81.01.1). *CPU file op* and *CPU write op* then gate *CPU write address* to the FCU where it tests the status of the CE write address switch (75.40.01.1). If the switch is in the write address position, *write address status* and *R/W select* are developed on 75.20.01.1. Note, *CPU write op* from 75.81.01.1 is not sent to the FCU because neither the record op or the track op latches are on (75.81.81.1). If the write address switch is off, the file operation is terminated at the beginning of the address-transfer step, B4 of digit 0 (75.26.01.1).

### *Address Transfer*

The basic objectives to be accomplished during this step are the same as those for the address transfer step described under READ SINGLE RECORD.

### *Write Pre-Indelible Address AGC Bits*

The basic objective of this step is to record the AGC bits with the same head used to write the I.A. characters. The amplitude of the AGC bits and the I.A. bits will then be approximately the same. This will allow the read amplifier gain to be properly set during succeeding operations.

The following objectives are developed in the normal manner:

| | |
|---|---|
| 1. Start/read write | (75.28.11.1) |
| 2. Address gate | (75.29.01.1) |
| 3. AGC gate | (75.29.01.1) |

The following additional objectives are required:

| | |
|---|---|
| 1. Write gate | (75.34.01.1) |
| 2. Control counter advance | (75.34.01.1) |
| 3. Write AGC latch | (75.34.01.1) |
| 4. Drop AGC gate | (75.29.01.1) |

#### Write Gate

The write gate latch is turned on from 3F (75.34.01.1) with $\phi$C delayed during the *start R/W* pulse. It remains on until reset by *write address reset* which is generated at BS$\phi$C of digit 0 following the indelible address (3A,4D-75.26.01.1). See, BASIC READ WRITE circuits for the write amplifier operation.

### Control Counter Advance

The control counter is advanced following the development of the *start R/W* pulse to define the pre-IA AGC portion of the record and to count the number of AGC bits written.

During the pre-IA AGC bit time, the file clock is running. The phase Bs generated by the clock are gated by the output from 4E (75.32.01.1) to produce the counter advance pulses. The counter is advanced in this manner until it contains 72. When it contains 72, the bit S latch is set which sets the bit S trigger which in turn sets the bit ring advance gate. Further control counter advance pulses are then blocked by the absence of *not bit ring advance gate* at 4E.

### Write AGC Latch

The write AGC latch is used to bring up the *write data* line. *Write data* then gates $\phi$Cs to the write amplifier. A series of $\phi$Cs are then recorded on the disk during the time the write AGC latch is on. The latch is turned on by *count 32* if the *write gate* and the *AGC gate* are up (3C-75.34.01.1). It is turned off from 4B by count 64. Therefore, following the development of *start R/W*, the record contains a 32 bit gap, followed by 31 AGC bits, followed by a 9 bit gap.

### Drop AGC Gate

The AGC latch is turned off by count 64 from 4A on 75.29.01.1.

## *Write Indelible Address and End the Operation*

Objectives:

1. Set and advance the bit ring
2. Advance the digit ring
3. Develop write data
4. End the operation.

### Set and Advance the Bit Ring

The bit ring is used to "serialize" the 1405 character register output. The ring must therefore be allowed to run through the IA step. The ring is set as described under WRITE PRE IA AGC BITS. The bit ring advance gate is set at BS$\phi$D. Phase As are gated by the *bit ring advance gate* to become the *bit ring advance* pulses. Therefore, the first advance pulse occurs at BC$\phi$A to turn the bit S trigger off and the bit C trigger on. The ring continues to advance with each succeeding $\phi$A.

### Advance the Digit Ring

The digit ring is advanced to identify the indelible address characters. It must therefore advance at 1405 speed to stay in step with the IA characters that are written. The advance pulses occur at bit S time when the address gate is up (75.21.11.1). As previously described, the first bit S available is the bit S for the module character. This bit S then advances the digit ring to digit 1 to identify the module character, etc.

### Develop Write Data

At the end of the address transfer step, the module character was placed in the E2 register. This character and each succeeding character of the IA must be transferred to the 1405 character register at the beginning of each digit time to enable them to be strobed from the character register by the bit ring during their respective digit time. The IA characters enter the character register when *write strobes* are developed at each BS$\phi$C time (4C-75.31.11.1). Write data is then developed in the normal manner as the bit ring strobes the character register output (75.36.01.1).

### End the Operation

The write address operation is ended when *write address reset* is developed at BS$\phi$C of digit 0 following the indelible address (3A, 4D-75.26.01.1). *Write address reset* serves to end the operation by developing *file end op, CPU end op,* and *end op* on 75.38.01.1. *Write address reset* also resets the write gate latch on 75.34.01.1.

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