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Program Logic

DOS Supervisor and Related Transients

Program Number 360N-CL-453

This reference publication describes the internal logic of the IBM Disk Operating System, Supervisor and Physical and Recovery Transient Programs. It is for persons involved in program maintenance and for system programmers altering the program design. Program logic information is not needed for normal operation of these programs. This publication is a supplement to the program listing.

Effective use of this manual requires an understanding of IBM System/360 or System/370 operation and of IBM Disk Operating System control and service programs, macro instructions, and operating procedures. Reference publications for this information are listed in the Preface of this manual.

Third Edition (June 1971)

This publication was formerly titled <u>IBM System/360 Disk</u> Operating System, Supervisor and Physical Transients Program <u>Logic Manual</u>. Although titles of some DOS publications (including this one) have been simplified, the change does not affect the contents of the publication.

This edition applies to Release 25 of IBM Disk Operating System and to all subsequent releases until otherwise indicated in new editions or Technical Newsletters. Changes are continually made to the specifications herein; before using this publication in connection with the operation of IBM systems, consult the latest System/360 and System/370 SRL Newsletter, GN20-0360, for the editions that are applicable and current.

This edition, GY24-5151-2, is a major revision of, and obsoletes, GY24-5151-1.

Summary of Amendments

This edition documents addition of, and changes to, the following information: PCIL (Private Core Image Library), JAI (Job Accounting Interface), System/370 RMS (Recovery Management Support), IDRA (Independent Directory Read-in Area), OLTEP (On-Line Test Executive Program), EREP (Environmental, Recording Editing, and Printing) enhancements, IBM 3211 Printer, System/360 Model 22, and certain maintenance enhancements.

Changes or additions to the text and illustrations are indicated by a vertical line to the left of the change.

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This Program Logic Manual (PLM) is a detailed quide to the IBM Disk Operating System supervisor and physical and recovery transient programs. It supplements the program listings by providing descriptive text and flowcharts.

The lists that follow give the titles of companion system control PLMs, prerequisite, and related publications.

Note: Although titles of some DOS publications have been simplified, the change does not affect the contents of the publications.

For overall system control logic description, this PLM is to be used with six other PLMs:

- Introduction to DOS Logic, GY24-5017
- DOS IPL and Job Control, GY24-5086
- DOS Librarian, GY24-5079
- DOS Linkage Editor, GY24-5080
- DOS Logical Transients, GY24-5152
- DOS System Service Programs, GY24-5153

Prerequisite to the effective use of the seven PLMs are the following publications:

- IBM System/360 Principles of Operation, GA22-6821
- DOS System Control and Service, GC24-5036
- IBM System/360 Disk and Tape Operating Systems, Assembler Language, GC24-3414

Publications related in subject matter to the seven system control PLMs are:

- DOS Supervisor and I/O Macros, GC24-5037
- DOS System Generation, GC24-5033
- DOS Operating Guide, GC24-5022
- DOS Messages, GC24-5074
- DOS Data Management Concepts, GC24-3427

Titles and abstracts of other related publications are listed in the IBM System/360 and System/370 Bibliography, GA22-6822.

This manual consists of seven major sections. The first section is an introduction to the supervisor and transient programs. The next section describes the generation and organization of the supervisor. The next five sections describe the detailed operation of the supervisor, physical IOCS, physical transients, and error logging and recovery. The last section of the manual, the appendixes, contains the label list, error messages, microfiche cross-reference index, and other references for use in analyzing program details.

The flowchart symbols used in this manual conform with the flowcharting standards of the American National Standards Institute, Inc. Numerals, such as 00, identify the program or general level flowcharts. The detailed flowcharts are identified by letters AA through ZZ. See Appendix F for an explanation of the flowchart symbols.

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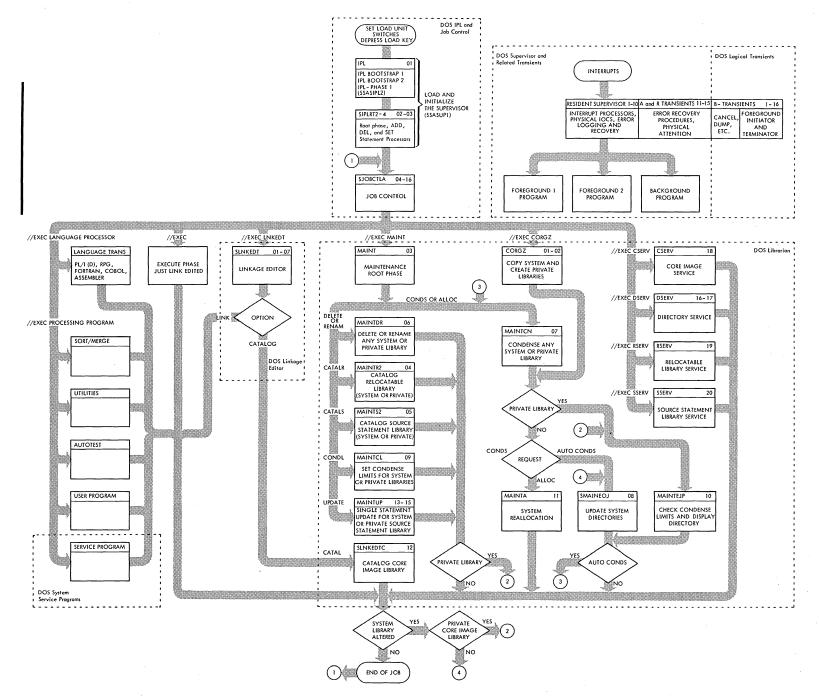
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ERP (Part 2 of 2)	

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Handler, Tape ERP (Part 2 of 2)	Writer



The resident version of the IBM System/360 Disk Operating System (DOS), System Control, provides disk operating system capabilities for 16K and larger System/360 configurations. At least one IBM 2311, 2314, or 2319 DASD device is required.

Systems larger than 16K can benefit from this 16K package if they do not require the expanded functions of the larger disk operating system packages offered by IBM. The system is disk resident, using the IBM 2311, 2314, or 2319 DASD device for on-line storage of all programs. Depending on the requirements of the particular application, the system can be expanded to include all processing programs used to perform the various jobs of a particular installation, or it can be tailored to a minimum system to control a single program.

The operating system includes the following components: CPU, input/output channels, input/output control units, input/output devices, microprogramming, system control programs, support programs, user programs, user data files, teleprocessing capability, and multiple programming capability. This PLM discusses the supervisor and the physical transients that are part of system control. supervisor and physical IOCS are specifically designed for a particular configuration by means of a one time assembly (generation time). They require reassembly only if the configuration changes.

The supervisor and physical IOCS provide the required interface between the program being executed and the other components of the operating system. The program currently being executed is identified to the operating system as the current program. The last program interrupted is identified as the problem program. problem program or the current program can be, at any given time, either a system control program, a support program, or a user program.

The supervisor operates with problem programs when job processing (problem program execution) occurs. The supervisor is divided into two parts:

The resident part, called the supervisor nucleus;

The nonresident part, called a supervisor transient.

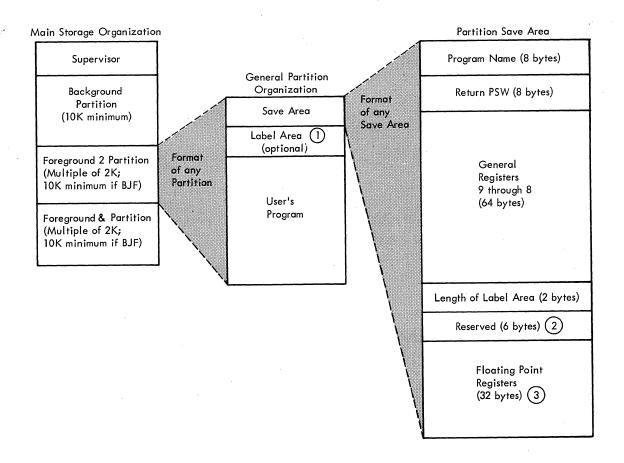
The nucleus is loaded into main storage at IPL time and remains there throughout job processing. Transients are loaded, as needed, from the core image library of SYSRES. When one transient has finished performing its service, it can be overlaid by another required transient. This technique makes maximum use of main storage allotted to the supervisor. The basic functions performed by the supervisor are:

- Storage protection (required for multiprogramming).
- · Interrupt handling.
- · Channel scheduling.
- Tape error statistics recording.
- Device error recovery.
- · Operator communications.
- Program retrieval (fetch or load).
- End-of-job processing.
- Timer services (optional).

Each installation must generate its own custom made supervisor by means of a one time assembly. Supervisor generation macros control the generation of the supervisor control program. The user must reassemble the supervisor if its functions are to be modified (for example, when an installation configuration changes).

MULTIPROGRAMMING

For systems with main storage equal to or greater than 24K, disk operating system offers multiprogramming support. This support is referred to as fixed partitioned multiprogramming, because the number and size of the partitions is defined during system generation. After system generation, the operator may redefine the size of the partition to meet the need of a specific program. Figure 1 shows the relationships among programs in a multiprogramming environment.



Notes:

- (1) Standard tape labels = 80 bytes; sequential DASD and DTFPH (MOUNTED = SINGLE) = 0 bytes; and DTFIS, DTFDA and DTFPH (MOUNTED = ALL) = 84 bytes + 20 bytes per extent statement.
- Job start time, for time stamp, is stored in last 4 bytes of this area (bytes 84–87) when BJF option is specified.
- Floating point register save area is required only when floating point feature is specified for supervisor generation.

Multiprogram Main Storage Organization Figure 1.

BACKGROUND VS FOREGROUND PROGRAMS

Foreground and background are the two types of problem programs in multiprogramming. Foreground programs may operate in either the batched-job mode or in the single-program mode. Background programs and batched-job foreground programs are initiated by job control from the batched-job input streams. Single-program foreground programs are initiated by the operator from the printer-keyboard. one completes, the operator must explicitly initiate the next program. Foreground and background programs initiate and terminate independently of each other.

The system can operate one background program and one or two foreground programs The supervisor controls simultaneously. priority for CPU processing, giving foreground programs priority over background programs. All programs operate with interrupts enabled. When an interrupt occurs, the supervisor gains control, processes the interrupt, and gives control to the highest priority program that is in a ready state.

Control is taken away from a high priority program when that program encounters a condition that prevents further processing until a specified event has occurred. Control is taken away from a lower priority program at the completion of an event for which a higher priority

program is waiting. When all programs in the system are simultaneously waiting (i.e., no program can process), the system is enabled for interruptions in the wait state.

The supervisor receives and processes interruptions. When an interruption satisfies a program's wait condition, that program becomes active and competes with other programs for CPU processing time.

In addition to at least 24K positions of main storage, multiprogramming support requires the storage protection feature.

If the batched-job foreground option is selected when the system is generated, all types of programs may be run as foreground programs. (Specifying the option causes the generation of individual communications regions for each partition.)

ASYNCHRONOUS PROCESSING

Asynchronous processing, also known as multitasking, provides a multiprogramming facility within any or all of the partitions of an MPS supervisor. An asynchronous program consists of two parts:

- The main program (maintask) that appears in the EXEC statement.
- One or more subprograms (subtasks) that must be in main storage in the same partition as the maintask.

The maintask initiates the subtask(s) via the ATTACH macro instruction. I/O overlap is facilitated because subtasks have higher priority than the maintask for CPU time within the partition. The subtasks are assigned priority in the order they are attached, the first attached subtask having the highest priority and the last attached subtask having the lowest priority. The partitions' priorities are unchanged.

Each subtask operates independently of the maintask and has its own registers and save area. Communication and synchronization between subtasks is accomplished by use of the POST and WAIT/WAITM macro instructions. Protection of shared data areas (resources) is accomplished by the ENQ macro and the corresponding DEQ macro.

Because only one set of symbolic I/O units exists for each partition, I/O assignments for all tasks must be made prior to the EXEC statement of the maintask.

A minimum of 24K bytes is required for multiprogramming, BTAM, 1412/1419/1255/1259 MICR document processing, and for assigning system I/O files to disk. The QTAM Message Control program requires a minimum of 32K bytes of main storage. The use of QTAM with two batched-job-foreground partitions requires a minimum of 64K bytes.

This section discusses:

- Techniques used in supervisor generation.
- Generation macros and their optional operands.
- The relationship between the outer generation macros and the inner macros that generate the bulk of the supervisor code.
- The organization of the supervisor, including the nucleus code, tables, and information blocks.

To understand macro definition language structure and usage, refer to the <u>DOS</u>
<u>Supervisor and I/O Macros</u> publication
listed in the front of this manual. With this information, an SSERV listing of the supervisor generation macros, and the PLM material, the reader can identify those sections of code that are generated for his own supervisor program. The basic instruction used in macro definition language is the AIF (ask if) statement. The following examples show how it is used:

- 1. AIF (&BG20).MP1
 This instruction asks if
 multiprogramming support is required.
 If BG20 is on, the next significant
 line in the SSERV listing is found at
 the label, .MP1, and any intervening
 code is rejected by the language
 translator. If BG20 is not on, the
 next sequential line on the SSERV
 listing is significant.
- 2. AIF (NOT &BG20).NO23
 This instruction tests the opposite status of the BG20 switch. In this case, the line at location .NO23 is the next significant line in the SSERV listing only when BG20 is not on; that is, only when multiprogramming support is not required.

A detailed description of the AIF instruction and the other instructions used in the SSERV listing is given in the Systems Reference Library publication, <u>IBM System/360 Disk and Tape Operating Systems, Assembler Specifications</u>, GC24-3414.

SUPERVISOR GENERATION

The supervisor is assembled with a series of macros that describe the installation's functional requirements and its configuration. At system generation time, a source deck containing the supervisor generation macros is assembled into an object deck. The job control program places the results of the assembly on SYSLNK (I/O device for the linkage editor program) and calls the linkage editor program. The deck is link-edited and cataloged to the core image library on SYSRES. A corresponding core image library directory entry is posted for the new supervisor, and the Program Information Department (PID) supervisor directory entry is deleted.

Normally, a condense maintenance program would then be executed to remove the PID supervisor from the core image library. The procedures and sequence of events used in system generation are described in the publication, DOS System Generation, GC24-5033.

Whenever a new supervisor generation is required, take these general steps:

- Punch the macro instructions and the selected optional operands into a card deck.
- Execute an assembly and put the object modules on SYSLNK (using an include control statement with no operand) via the job control program.
- 3. Link-edit the new supervisor, cataloging it to the core image library, deleting the old supervisor directory entry, and posting the new supervisor directory entry. System control programs must be cataloged in the same run as the supervisor.
- 4. Re-IPL with the new supervisor.
- Execute a maintenance program to condense the core image library, deleting the old supervisor program.

Figure 2 shows the allocation of storage for the generated supervisor.

) 4			Re	set to Zero	s after IPL				→ 13	\prod	
14 Comm Region Address	18 External Old PSW	20 SVC Old PSV	28 Program Old PSW	Program Ma		38 I/O Old PSW	40 CSW	48 CAW	4C BG Job Duration		
50 System Timer	54 System Ti of Day	mer	58 External New PSW	00 SVC 1 W29	New	68 Program Check New PSW	70 Machine (New PSW		78 I/O New PSW		
80 Diagnostic Sc	an-out Area (System/360	or Permanently	Allocated	Low Core (S)	ystem/3701				IJ	
· .			SI	JPERVISOF	NUCLEUS					1)	
Ge	neral Cancel	Routine			·		gisters (SVER	EG) Rout	ine	41	
					(Task Selec					$\frac{1}{1}$	
	TDD DAAC I!	. I A	Background Co	mmunicatio	ons Region ar		D 11 .			H	
	CRR or RMS Lir I Common Tab					General Entry SVC Interrupt				11	
	annel Schedul					Start I/O Rou				11	Nucleus
	O Interrupt					Machine Che		S/360 on	lv)	17	Code
	it Check					Error Recover		7	//	11	
At	tention Task					Error Recover	y Block			11	
. PC	,OC, AB, and	d IT Tables				PTA, IDRA,	and LTA Save	Areas		11	
Su	pervisor Const	ants				Fetch Subrout	ines]	
				SVC Interru	pt Routines					\prod	
Pro	gram Check R	outines				External Inter	rupt Routines			IJ	
			Resi	ident Devid	e Error Rout	ine				IJ	
Op	otion Routine				syslnk dib				41		
	CR Interrupt R		0.15.6	0.15		SYSCLB LUBs		<u> </u>	0.10.5	41	
2nd Part of All Bound PIB	2nd Par BG PIB		2nd Part of F2 PIB	2nd Po F1 PIE		2nd Part of Attn PIB	2nd Part of Quiesce I,		2nd Part of Supervisor PIB		
2nd Part of Subtask PIBs Note 2	1st Part All Bour		1st Part of BG PIB	1st Part of F2 PIB		1st Part of F1 PIB	1st Part Attn PIE	- 1	1st Part of Quiesce I/O PIB	1/0 0	
1st Part of Supervisor PIB	1st Part Subtask Note 2		Channel PUB Pointer Table	SVC In Table	terrupt	Channel Queue	LUBIC Table		REQID Table	$\ $	Informati Blocks
LUBDSP Table	TSKID Table)	FOCL	PUB Table		FAVP	JIB		Disk Information Blocks (with SYSFIL)	$\ $	
TEB/TEBV	Conso Buffer		FICL	NIC	L	LUB Table	Track Hold Note 3	l Table	CBF Patch Area		
PT	O Patch Area					JAI Partition	Tables, User	Save Are	ea, Label Area	V	
		(System/360 or				MCRR Patch Are				1	I/O Erroi
		(System/370	<u>'</u>	tor, RMS R	esident Routi	ines, RTA (R-tran				4}	Logging
SDR Communications Region				I/O Error Logging (OBR/SDR) Routines				K	Recovery		
Fo	reground 2 Cor	mmunicatio	ns Region				Communicati	ons Regio	on	41	Addition
F2 Comreg Extension				F1 Comreg Extension				43	Comm		
ASCII Translation Tables				SAB				41	Regions		
Pa	tch Area		1,		- /D	IDRA				*	Logical
					a (B-transier					Ŧŧ	and
	Table		rnysicai iro	CE A	a (A-transiei	1113) DAM	BG Progra	m Save	Area	11	Physical Transient
CL				roblem Prog			5 0 110g/c	5076		ピ	

Note 1: For PSW format see Figure 39. For CSW format see Figure 41. For CAW format see Figure 40. Note 2: Total of 9 subtasks PIBs generated.

Note 3: Maximum of 225 entries generated.

Figure 2. Supervisor Storage Allocation

SUPERVISOR GENERATION MACROS

The list of supervisor macros and optional operands in Figure 3 gives the reader:

- Supervisor generation macro names.
- Required macro sequence (as listed in Figure 3).
- Macro parameters. (Where there is an assumed value, that value is underlined.)
- A brief description of what the generated macro does.
- A brief description of what the individual parameter options do.

MACRO RELATIONSHIPS

The code generated by the assembler for any selected supervisor generation is a function of the generation macros described in Figure 4 and of a group of inner macros called by the generation macros. The primary purpose of the generation macros is to set global values, based on parameter options, that can be tested by the inner macros. These macros then generate the bulk of the supervisor code. The specific instructions assembled depend on the global settings. Some of the generation macros also generate code; however, these can be treated as exceptions and are identified in this subsection.

The most important global values used in supervisor generation are the B-globals. Therefore, this subsection emphasizes the generation macros that establish B-global values. However, some A-globals that are tested in the same manner as B-globals are also described in this subsection. C-globals are not described. Two figures in this subsection show macro relationships. Figure 5 shows the code generated, if any, and the globals set, if any. Figure 6 indicates the on-off conditions of the globals.

ORGANIZATION

The physical organization of the supervisor depends on the sequence of the supervisor generation macros. The sequence is

predetermined and cannot be changed by the user. The logical organization depends on the parameter options selected at generation time. Figure 2 is a main storage map of the assembled supervisor, which illustrates the supervisor physical organization in four major areas:

- Low Core
- Nucleus Code
- I/O Tables and Information Blocks
- Logical and Physical Transient Areas

The logical organization is not described in this manual because of the variety of options available. You must determine the logical organization for individual supervisor generations. By using the program level flowcharts to point to the detailed flowcharts, you may select the correct group of flowcharts for the desired generation.

LOW CORE

The first 128 bytes of main storage contain identical assignments for System/360 and System/370. The systems differ starting with byte 128. On System/360, DOS reserves a diagnostic scan-out area under conditions described in this section. On System/370, DOS allocates bytes 128-511 for specific hardware requirements. Low core assignments are made for both systems by DOS, and the user should not alter them.

The main storage locations that make up low core can be classified as PSWs, CSWs, CAWs, and main storage areas. PSWs, CAWs, and CSWs are described in the section Physical Input/Output Control System (PIOCS). The main storage areas include:

Byte (hex)	<u>Function</u>			
0-3	System/360: Contains SEREP error codes 00 and 01, or WAIT error codes 03-60 (Figure 3).			
0-3	System/370: Contains SEREP error codes A to I (X'C1' to X'C9'), or WAIT error codes 03-60 (Figure 3).			
0-4	Message area when SYSLOG is disabled.			

Byte 0	Byte 1	Byte 2	Byte 3	Explanation	
SYSTEM/360 SEREP Codes:					
X'00'	X' E2'	Not used	Not used	Machine check. Load SEREP. Re-IPL system.	
X'01'	X'E2'	Reserved	Reserved	Channel failure: interface or channel control check. Load SEREP. Re-IPL system.	
SYSTEM,	/370 SEREP (Codes:			
X'C1'	X'E2'	A, I, S*	Not used	Unrecoverable machine check.	
X' C2'	X' E2'	Not used	Not used	Unrecoverable channel failure during RMS fetch.	
X'C3'	X' E2'	A, I, S*	Not used	Channel failure on SYSLOG when RMS message scheduled.	
X'C4'	X'E2'	A, I, S*	Not used	Reserved (should not occur)	
X' C5'	X' E2'	A, I, S*	Not used	Channel failure; ERPIBs exhausted.	
X'C6'	X' E2'	A, I, S*	Not used	Channel failure; two channels damaged or a damaged channel situation occurred while RMS was executing an I/O operation.	
X'C7'	X' E2'	A, I, S*	Not used	Channel failure; system reset was presented by a channel.	
X'C8'	X' E2'	A, I, S*	Not used	Channel failure; system codes in ECSW are invalid.	
X'C9'	X' E2'	A, I, S*	Not used	Channel failure; channel address invalid.	
SYSTEM	/360 and SY	STEM/370 W	AIT Codes:		
X'03'	X' E6'	Channel	Unit	DOS unrecoverable disk error during program fetch. The first six sense bytes are placed in hex bytes 5-A. Re-IPL system.	
X'04'	X'E6'	Not used	Not used	Cancel condition has occurred while performing a Supervisor function (not a Supervisor detected problem–program error). Normally a Program Check while in Supervisor State. Re–IPL System.	
X'05'	X' E6'	Channel	Unit	I/O Error Queue has overflowed as the result of an I/O error on a program fetch channel program. Re–IPL system.	
X'06'	Not used	Not used	Not used	Reserved (should not occur).	
X'07'	X'E6'	Channel	Unit	IPL I/O error. Channel and unit indicate whether SYSRES or communication device. Re-IPL system.	
X'08' to X'60'		Channel	Unit	Error recovery messages. Refer to OP messages in <u>DOS Messages</u> , found in Preface.	

^{*}Note: A (X'C1') = SYSREC error recording unsuccessful.

I (X'C9') = SYSREC error recording imcomplete.

S (X'E2') = SYSREC error recording successful.

Figure 3. Low Core Error Bytes

14	When MPS=NO or YES: Contains address of background communications region.	54	Contains system time of day set by job control and IPL, updated by the supervisor timer routine (optional).
	When MPS=BJF: Contains address of communications region of the active partition.	80	Beginning of the System/360 diagnostic scan-out area or the System/370 permanently allocated low core.

Contains the system timer used with microprogramming. 50

System/360 Diagnostic Scan-Out Area

The DOS supervisor for the System/360 records machine check interrupts and channel inboard errors in the diagnostic scan-out area. The area is generated at SYSGEN and begins at byte 128 (X'80') of low core. The length of the area depends on the SYSGEN option MCRR (Machine Check Recording and Recovery).

When MCRR=NO, the diagnostic scan-out area is 12 bytes long. When MCRR=YES, the length of the area is model-dependent:

Model 30 area, 12 bytes Model 40 area, 196 bytes Model 50 area, 168 bytes

<u>Note</u>: System/370 does not generate a diagnostic scan-out area to diagnose interrupts and errors.

System/370 Permanently Allocated Low Core

Byte	Function
0-127	Identical to System/360
128-167	Reserved
168-172	Channel ID
173-175	ICEL pointer
176-181	Limited channel logout (ECSW)
182	Extended channel status
183-184	Validity
185-187	I/O address
188-231	Reserved
232-235	Machine check interruption code
236-247	Reserved
248-251	Failing-storage address
252-255	Region code
256-351	Fixed logout area
352-383	Floating-point register save area
384-447	General register save area
448-511	Control register save area

NUCLEUS CODE

The main storage map (Figure 2) illustrates the major routine and subroutine organization of the supervisor. Specific instructions are included or omitted depending on generation options. This manual describes the disk error recovery as the resident error recovery routine.

The background communications region does not change from generation to generation. Figure 8 illustrates the structure of the communications region. The starting address of the communications region is made available to a user in general register 1 through the COMRG macro. For certain options, extensions to the communications regions are generated at the end of the I/O Tables by the SEND macro. Figure 9 shows the contents of the communications region extensions.

I/O TABLES

The I/O tables (See Figure 7) that comprise this section of the supervisor establish the interface between a specific program and the hardware channels. For every device used on the system, there must be a PUB (Physical Unit Block). For every logical unit name (SYSXXX) used, there must be a LUB (Logical Unit Block). When an I/O request is made, an entry is made in CHANQ (the channel queue). The entry contains a CCB (Channel Command Block) address which, in turn, points to a CCB that contains a code (LUB table index) for the logical unit name.

The supervisor processes the request when possible on the device assigned to the logical unit. If the TEB option was selected at generation time, counts of tape errors by unit are kept in the TEBs (Tape Error Blocks). If the TEBV option was selected, counts of tape errors by volume are kept in TEBVs (Tape Error Blocks by Volume).

To understand the interaction among the various I/O tables, review the classification and sequence of the symbolic unit references (SYSXXX). The systems class (symbolic unit names reserved for system use) is made up of:

- 1. SYSRDR
- 2. SYSIPT
- 3. SYSPCH
- 4. SYSLST
- 5. SYSLOG
- 6. SYSLNK
- 7. SYSRES

- SYSSLB
- 9. SYSRLB
- SYSUSE 10.
- 11. SYSREC
- SYSCLB 12.

The programmer class (symbolic unit names reserved for programmer use) is made up of SYS000 to SYS221 with MPS or SYS000 to SYS243 with no MPS. This class is subdivided into these classifications:

- Background logical unit class (minimum of 10).
- Foreground two logical unit class (minimum of 5).
- Foreground one logical unit class (minimum of 5).

PUBs are built at system generation or IPL time. LUBs are built at system generation time. PUBs are assigned to LUBs at system generation or by the job control program, or by the single program initiator. CHANQ, TEBV, and TEB entries are built and processed by the supervisor program. Figure 7 shows the I/O table interrelationships

INFORMATION BLOCKS AND OTHER TABLES

To accomplish functions such as exit selection, DASD file protection, and record identification, the supervisor program requires pertinent information. At supervisor generation time certain main storage locations are set aside and, in some cases, initialized to supply the required information. The basic information blocks and their respective functions are:

PIB (Program Information Block): The first half of a PIB retains program status information for user and supervisor programs. It supplies routing information in a multiprogramming environment to allow selective program return and it contains pointers and switches used by the supervisor program (Figures 15 and 16). The second half contains the address of the area communications region and the system LUB Index, priority of the PIB address of the termination ECB, and the PIB displacement (Figure 14).

DIB (Disk Information Block): The DIB is built at generation time if the SYSFIL option was selected. It performs a record keeping function on system class units assigned to a DASD. The DIB contains the current seek address when the system is operating in a batched job environment.

The block is initialized by job control with extent information and updated by physical IOCS. When the PCIL option is used, the DIB is updated each time the PCIL is assigned. It is located in the IOTAB macro expansion. (See Figure 12.)

JIB (Job Information Block): The JIB contains one of the following:

- LUB entry of the standard assignment when a temporary LUB assignment is made.
- PUB pointer for an alternate LUB assignment.
- Extent information when DASD file protection is selected as a supervisor generation option.

Extent information is supplied by the program initiator and logical IOCS open transient routines. The supervisor can then perform the file protect function for the specified file limits. File protection does not include supervisor and transient originated I/O. (See Figure 19.)

SAB (Seek Address Block): Contains a four-byte address (BCCH) for each DASD when the seek separation feature is specified. It also has a fifth byte which contains a Track Hold Table pointer or X'FF' if both SKSEP and TRKHLD were generated, or X'00' if TRKHLD was not specified. The current address is maintained in the SAB for the particular device. Each SAB is referenced by its corresponding PUB.

Other Tables: Several optional tables are built at generation time within the supervisor:

- CE Table Generated in the SEND macro expansion. Contains 4-byte pointers, each of which points to a hook within the supervisor that accesses the CE serviceability routines. Provision is made for up to ten entries in the CE table. See Figure 28 for an illustration of this table, how it is accessed, and how the hooks are used.
- PC, OC, IT, and AB Tables Generated in the SGTCON macro expansion. These four tables (program check, operator communications, interval timer, and abnormal termination) contain addresses supplied by the user with a STXIT (See Figure 13.)
- CBF Table Generated in the LUBGEN macro expansion. This table holds the CCW, CCB, partition ID, and data for buffered I/O requests (SVC 0) to SYSLOG where SYSLOG is an IBM 1052. Figure 22.)

- DTF Address Generated in the SMICR macro expansion. These two tables (PDTABA and PDTABB) contain pointers, DTF addresses, and other information for handling external interrupts on magnetic ink character recognition (See Figure 10.) devices.
- ASCII-EBCDIC and EBCDIC-ASCII translation tables - Generated in the SEND macro expansion if the ASCII=YES optional parameter is specified. (See Figure 27.)

Additional Communications Region: communications regions for the two foreground partitions are located at the end of the I/O tables. Their format is identical to that of the background communications region. If generated, the background communications region extension immediately follows the BG communications region within the nucleus of the supervisor. Foreground extensions follow the F2 and F1 communications regions (see Figure 2). The extensions are generated if any of the following options are specified: CE, AP, AB, TRKHLD, MCRR, TEBV, EVA, ASCII, SPARM, or ERRLOG. The extensions are also generated if the MODEL option specifies a System/370 CPU. See Figure 9 for the format of the communications region extensions.

SDR Communications Region: Generated in the SEND macro expansion when the ERRLOG option is specified at system generation. This region provides an interface among job

control, the supervisor, and various A-transients when the OBR/SDR functions are in use. See Figure 26 for the SDR communications region format, and Figure 2 for the location of the region.

Transient, CE, and Save Areas: Main storage locations are reserved in the area preceding the problem program area for:

- Logical (\$\$B) transients 1200 bytes.
- Physical (\$\$A) transients 552 bytes.
- Recovery (\$\$R) transients 1000 bytes.
- CE area (only if CE=YES or n) 600 bytes minimum.
- Background save area 80 bytes (112 with floating point feature). The BG save area contains five subfields: PSW, general registers (9 through 8), label length, 6 reserved bytes, and optionally floating point registers (0,2,4,6). (See Figure 1.)

IDRA (Independent Directory Read-in Area): IDRA is a supervisor option that generates a 368 byte supplemental area to reduce contention for the physical transient area. IDRA reads core image library directories for all fetch and load operations. Thus, the PTA is left free to perform ERP.

Nan	Macro Description	Parameter = Option	Option Description
SUP	/R Describes system environment	SYSTEM = DISK	System residence (SYSRES) must be on a disk device.
		$MPS = \left\{ \frac{NO}{YES} \right\}$	Indicates multiprogramming support. If YES or BJF is specified, the system generated is capable of supporting two foreground programs. YES or BJF must be specified if TP = QTAM. If BJF is specified, the system generated will support batched mode for both foreground partitions. Multiple communications regions are generated only if MPS = BJF. MPS = YES is implied if MPS = BJF.
		$TP = \begin{cases} \frac{NO}{BTAM} \\ QTAM \\ QTAMn \end{cases}$	Specify if Basic or Queued Teleprocessing Access Method (BTAM or QTAM) is desired. When QTAM is specified, SVC support for BTAM is also included. To process QTAM in a system with asynchronous processing support, QTAMn must be specified where n is the maximum number of active QTAM message processing programs in the system. From 2 to 12 programs may be specified with a default value of 2.
		ERRLOG = (NO YES RDE n (YES, RDE) (n, RDE)	Specify if the Outboard Recorder (OBR) is to record data pertinent to an error that cannot be retried or corrected after a standard number or retries. Also, specify if the Statistical Data Recorder (SDR) is to record the cumulative error status of an I/O device. n defines the number of records required on the SDR partition of the Recorder File, where n is any number equal to, or greater than, the number of PUBs. YES indicates a number of SDR records equal to the number of PUBs. ERRLOG = RDE supports the Reliability Data Extractor for System/370 only. If RDE is specified without YES or n, YES is assumed. ERRLOG is assumed YES for all System/370 MODEL options if it is not specified.
		$MCRR = \left\{ \frac{NO}{YES} \right\}$	Specify if MCRR is to record pertinent data after a machine check, channel control check, interface control check, or channel data check. MCRR analyzes collected data and cancels the damaged partition(s). No attempt at error retry is made. This parameter is valid only for Models 30, 40, and 50.
		MICR = $\begin{pmatrix} \frac{NO}{1412} \\ 1419 \\ 1419D \end{pmatrix}$	Indicates whether the supervisor is to support magnetic ink character readers or optical reader/sorters. If both 1412s and 1419s are present, indicate 1419. 1419D/1275 indicates Dual Address Adapter 1419s. If 1412/1419/1255/1259/1270/1275s are attached to the multiplexor channel, the PIOCS parameter BMPX = YES is not supported.
		$AP = \left\{ \frac{NO}{YES} \right\}$	Indicates asynchronous processing support. This provides the user with the facility to write dependent programs to run concurrently within a partition and still maintain the partition independency of MPS. If YES is specified, global BG20 (MPS = YES or BJF) is forced on whether or not it was specified.
		$EU = \begin{cases} \frac{NO}{YES} \\ RELOC \end{cases}$	EU = YES specifies: IBM 1401/1440/1460 Emulator for Models 25, 30, or 40; IBM 1401/1440/1460 or 1410/7010 Emulator and mixed parity tape processing for System/370 CPUs. If foreground emulation is desired on any model, MPS = BJF is required. Foreground emulation on Model 40 requires EU = RELOC.
		$ASCII = \left\{ \frac{NO}{YES} \right\}$	Indicates whether the supervisor is to support the American National Standard Code for Information Interchange (ASCII). YES adds 512 bytes to supervisor size.
CON	PFG Describes hardware features	$MODEL = \left\{ \frac{30}{nn} \right\}$	nn defines the System/360 model number (Model 30, 40, or 50 must be entered if MCRR option is specified). nnn defines the System/370 model number. (A System/370 model causes generation of MCAR/CCH support. MCRR is not compatible with System/370.)
	-	$SP = \left\{ \frac{NO}{YES} \right\}$	Indicates the storage protection feature is desired. YES is assumed if MPS = YES or BJF in the SUPVR macro.
		$DEC = \left\{ \frac{NO}{YES} \right\}$	Decimal feature.
		$FP = \left\{ \frac{NO}{YES} \right\}$	Floating-point feature.
		TIMER = $\left\{ \frac{NO}{YES} \right\}$	Timer feature. If TIMER = YES the supervisor macro GETIME is supported.
		$PORT = \left\{ \frac{NO}{155} \right\}$	Causes Model 155 MCAR/CCH functions if MODEL = 145.

Figure 4. Supervisor Macros (Part 1 of 5)

Name	Macro Description	Parameter = Option	Option Description
STDJC	Sets standard values for job control variables.	$DECK = \left\{ \frac{YES}{NO} \right\}$	Output modules on SYSPCH.
		$LIST = \left\{ \frac{YES}{NO} \right\}$	Source modules listings from language translators on SYSLST.
		$XREF = \left\{ \frac{YES}{NO} \right\}$	Language translators output symbolic cross-reference lists on SYSLST.
		$ERRS = \left\{ \frac{YES}{NO} \right\}$	Compilers summarize all errors in source programs on SYSLST.
		$LOG = \left\{ \frac{YES}{NO} \right\}$	Listing of all control statements on SYSLST.
		$DUMP = \left\{ \frac{YES}{NO} \right\}$	Dump of registers and main storage on SYSLST.
		LINES = $\left\{\frac{56}{nn}\right\}$	Number of lines per page on SYSLST.
		$DATE = \left\{ \frac{MDY}{DMY} \right\}$	Format of date.
ŀ		$CHARSET = \left\{ \frac{48C}{60C} \right\}$	Specifies the 48 or 60 character set for language translator input on SYSIPT.
		LISTX = $\left\{\frac{NO}{YES}\right\}$	Hexadecimal object module listings from compilers on SYSLST.
		$SYM = \left\{ \frac{NO}{YES} \right\}$	Assembler output symbol tables on SYSPCH.
		$SPARM = \left\{ \frac{NO}{YES} \right\}$	Support of assembler variable symbol &SYSPARM
FOPT	Describes functional supervisory options	$OC = \left\{ \frac{NO}{YES} \right\}$	Operator initiated communications to problem programs. If OC = YES the facility is available to all programs in MPS. Must be YES if Emulator on System/370 is used.
		$PC = \left\{ \frac{NO}{YES} \right\}$	Problem program routine for program check. If PC = YES, the facility is available to all programs in MPS.
		$IT = \left\{ \begin{array}{c} \frac{NO}{BG} \\ F1 \\ F2 \end{array} \right\}$	Problem program ability to set timer intervals and specify a timer interrupt routine. BG, F1, or F2 indicates which program has the facility. When IT is specified for a partition, TIMER = YES is assumed in the CONFG macro. Timer support is available to only one program in MPS.
		$AB = \left\{ \frac{NO}{YES} \right\}$	Provides for valid use of the STXIT (AB) macro. If AB = YES, the facility is available to all programs in MPS.
		$TEB = \left\{ \frac{NO}{n} \right\}$	Tape error statistics are to be accumulated and logged, where n is the number of 2400-series tape units and tape cartridge readers (maximum of 225) attached to the system. **
	·	$TEBV = \left\{ \left(\begin{cases} \frac{NO}{DASD} \\ SYSLOG \end{cases} \right), n \right\}$	Tape Error Statistics by Volume are to be accumulated and logged on SYSLOG or a DASD device, where n is the number of 2400 series tape drives attached to the system. **
		$EVA = \left\{ \left(rth, \frac{NO}{wth}, n \right) \right\}$	Error Volume Analysis is supported where rth is the read error threshold, wth is the write error threshold, and n is the number of 2400 series tape drives attached to the system. **
11	9	** The n specified in TEB, TE are specified, and then TA	I BV, and EVA must be identical if two or more of these options PE=9 is assumed.

Figure 4. Supervisor Macros (Part 2 of 5)

Name	Macro Description	Parameter = Option	Option Description
FOPT (cont'd)		$SKSEP = \left\{ \frac{NO}{YES} \right\}$	Specifies if SEEKs are to be separated from the remainder of channel programs. Seek separation allows other devices on the channel to be accessed (including other seeks) during the seek. YES indicated support for all DASD types specified by the DVCGEN macro at system generation time, in is the number of DASD to be supported and cannot be less than the number of DASD specified at system generation. The maximum number is 254.
		$CE = \left\{ \frac{NO}{YES} \right\}$	Specifies the amount of core to be allocated to customer engineer serviceability routines or PDAIDs. When YES is specified, 600 bytes are allocated; when n bytes are specified, it must be for a minimum of 600 bytes. If PDAIDs or the QTAM or SVC in CEAIDs are used, specify a minimum of 800 bytes.
		$CCHAIN = \left\{ \frac{NO}{YES} \right\}$	Command chaining support for retry on I/O operations. When an error occurs and CCHAIN = YES, the user is allowed to retry at the last CCW executed instead of at the first CCW in the channel program as is the case in a normal retry. This option requires that the appropriate bit be set in the CCB.
		$PTO = \left\{ \frac{NO}{YES} \right\}$	Physical Transient Overlap allows tasks to be selected during the time of FETCH, LOAD, MVCOM, and ERP I/O. PTO is valid only when MPS = YES or MPS = BJF in the SUPVR macro.
	·	$CBF = \left\{\frac{NO}{n}\right\}$	Console Buffering provides immediate return to the caller when write I/O to SYSLOG is issued where SYSLOG is a 1052. n indicates the number of buffers to be generated. 1 to 50 buffers may be specified. 1 is assumed if the operand is invalid.
		$IDRA = \left\{ \frac{NO}{YES} \right\}$	Independent Directory Read-in Area feature. YES option causes generation of the IDRA area in supervisor. IDRA reduces contention for the PTA in fetch operations when ERP is active. Use of IDRA requires MPS = YES or BJF and PTO = YES.
		$TRKHLD = \left\{ \frac{NO}{n} \right\}$	If n is specified, coding to support the HOLD and FREE track macros. TRKHLD = n specifies the number of tracks to be held at any one time, and a Track Hold Table (See Figure 24) is generated for that number. If n is not in the range of 1 to 225, 10 is assumed.
		WAITM = $\left\{\frac{NO}{YES}\right\}$	Provides for valid use of the WAITM macro, waiting for one of a number of events to occur before continuing with task execution. Waits are performed on Event Control Blocks, which may be of the special form as in Figure 34. Other blocks that may be used as ECBs are CCBs, TECBs, and MICR CCBs since posting is done in bit 0 byte 2 of the block.
·		** RETAIN = $\left\{\frac{NO}{YES}\right\}$	Specifies if the data link to the Remote Analysis Center is to be supported. RETAIN = YES is valid only if a S/370 CPU was specified in the MODEL option. RETAIN = YES forces OC = YES.
		DASDFP = $\begin{cases} \frac{NO}{(n,n,2311)} \\ (n,n,2314) \\ (n,n,2321) \end{cases}$	Supervisory DASD file protection, where (n,n) indicates the range of channels to which DASDs may be attached. Specifying 2311 or 2314 indicates support for both. 2321 option indicates support for 2321 device as well as for 2311 and 2314. DASDFP prevents the user from writing outside the extents of his file in case of program error. Extents are protected to the nearest cylinder.
		*SYSFIL = $ \left\{ \begin{array}{c} NO \\ (2311 \ [,n1,n2]) \\ (2314 \ [,n1,n2]) \end{array} \right\} $	System input and system output (SYSRDR, SYSIPT, SYSLST, SYSPCH) files may be assigned to a 2311, 2314, or both. Specifying either indicates support for both. If MPS=BJF in the SUPVR macro, support is given for foreground logical units when running in batched mode.
			n1 = residual capacity (in records) for beginning of operator notification when SYSLST is assigned to a 2311 or 2314.
			100 ≤ n1 ≤ 65536 If n1 is omitted, 1000 is assumed.
			bytes of main storage are available. /370 CPU; YES is the default for a S/370 MODEL. NO is the default

Figure 4. Supervisor Macros (Part 3 of 5)

	Name	Macro Description	Parameter = Option	Option Description
	FOPT (cont'd)		*SYSFIL (cont'd)	n2=residual capacity (in records) for beginning of operator notification when SYSPCH is assigned to a 2311 or 2314.
				If n2 is omitted, 1000 is assumed.
			$PCIL = \left\{ \frac{NO}{YES} \right\}$	Provides supervisor support for private core image library.
			$JA = \left\{ \frac{NO}{YES}, \frac{1}{n1, n2, n3} \right\}$	NO defaults to no Job Accounting Interface support. YES specifies basic JA support. (n1,n2,n3) gives additional support to count SIOs issued to I/O devices by partition. n1,n2, and n3 refer to the number of devices in BG, F2, and F1 for which SIOs are to be counted. Choose values for each n from 0 to 255 to specify the number of devices accessed by partition; if any n value is omitted, it defaults to zero.
		,	$JALIOCS = \left\{ \frac{NO}{(n1, n2)} \right\}$	NO defaults to 16 bytes in the user save area and zero bytes for the alternate label area. Set n1 from 0 to 1024 bytes for the user save area; if omitted, it defaults to 16 bytes. Set n2 from 0 to 224 bytes for the alternate label area (usually=number specified by LBLTYP); if omitted, it defaults to zero bytes.
			OLTEP = $\left\{ \frac{NO}{YES} \right\}$	Specify if the on-line testing function is desired. If MODEL=a System/370 CPU, then OLTEP=YES is assumed.
	PIOCS -	Describes the system I/O configuration	$SELCH = \left\{ \frac{YES}{NO} \right\}$	Selector channels attached to the system.
			$BMPX = \left\{ \frac{NO}{YES} \right\}$	Burst Mode devices are supported on multiplexor channel. If 1412 – 1419s or 1287 – 1288s are attached to the multiplexor channel, BMPX =YES is not supported.
			$CHANSW = \left\{ \frac{NO}{TSWTCH} \right\}$ RWTAU	Channel switching tape control unit. RWTAU = 2404 or 2804, TSWTCH = 2816.
			$TAPE = \left\{ \frac{NO}{9} \right\}$	Indicates required tape PIOCS support. 9=nine track only, 7=seven or nine track, NO =No tape units attached. NO is the assumed value.
			$MRSLCH = \left\{ \frac{NO}{YES} \right\}$	MICR tape device assigned to a selector channel.
	ALLOC	Partitions storage for MPS (optional macro).	F1 =nK, F2 =nK	Specifies storage partitioning MPS, where n must be a multiple of 2. Must be at least 10K if MPS=BJF.
ľ	IOTAB	Describes installation requirements for I/O tables.	$IODEV = \left\{ \frac{10}{n} \right\}$	Number of I/O devices attached to the system.
		•	$BGPGR = \left\{\frac{10}{n}\right\}$	Number of symbolic units of the class SYSnnn for the background program.
			$F1PGR = \left\{ \frac{5}{n} \right\}$	Number of symbolic units of the class SYSnnn for F1. Valid only in MPS (minimum 5). Otherwise zero is assumed when MPS=NO.
			$F2PGR = \left\{ \frac{5}{n} \right\}$	Number of symbolic units of the class SYSnnn for F2. Valid only in MPS (minimum 5). Otherwise zero is assumed when MPS =NO.
			CHANQ= $\left\{\frac{6}{n}\right\}$	Number I/O requests in the channel queue. 6 is the minimum value generated. In a supervisor with CBF option specified, the minimum value is 6 plus the number of console buffers generated.
			$JIB = \left\{ \frac{5}{n} \right\}$	Number of Job Information Blocks (JIBs) for the system. Requirements are: 1. One JIB for each temporary logical unit assignment. 2. One JIB for each alternate logical unit assignment. 3. One JIB for each open 2311 or 2314 extent with the DASD file protect feature. 4. Two JIBs for each open 2321 extent with the DASD file protect feature.

*Valid when at least 24K bytes of main storage are available.

Figure 4. Supervisor Macros (Part 4 of 5)

Name	Macro Description	Parameter = Option	Option Description
DVCGEN	Specifies I/O devices. Each device type requires a separate DVCGEN macro. (See note 1 for DVCGEN rules. This is an optional macro.)	CHUN ={X'cuu'} DVCTYP = {xxxxxx} CHANSW = {NO YES} MODE ={X'ss'}	Specify the hexadecimal number of the channel and unit for the device. Specify the device type. See Figure 29. Specify if the device is attached to more than one selector channel. If it is, the device can be switched. 1. 2400T9. MODE specifies the tape mode. X'C0' is the default value. 2. 2400T7. MODE specifies the tape mode. X'90' is the default value. See Figure 30 for other values. 3. 2702. MODE designates the SADxxx command. X'00' is the default value. X'00' SAD0 X'01' SAD1 X'02' SAD2 X'03' SAD3 4. 2260 (Local). MODE is used to specify the 1053 printer when CHUN = X'cuu' refers to a 1053 attached to a 2848. The operand must be entered as MODE = X'01'. 5. 1412/1419. MODE designates the external interrupt bit associated with Magnetic Ink Character Readers. The modes X'01' through X'20' correspond to external interrupt PSW bits 31 through 26 respectively. For the dual address adapter 1419, this parameter is needed for both the 1419P and the 1419S device types. X'01' Device attached to external line 7. X'02' Device attached to external line 6. X'04' Device attached to external line 6. X'04' Device attached to external line 3. X'20' Device attached to external line 2. 6. 1018 Paper Tape Punch with 2826 Paper Tape Control Unit Model 1. This parameter specifies whether or not the Error Correction feature is present: X'00' feature not present X'01' feature present
ASSGN	Sets standard I/O assignments. A separate macro is required for each standard assignment desired. (Optional macro)	$\left\{ SYSxxx, X'cuu', \left\{ \frac{BG}{F1} \right\} \right\}$	SYSxxx is any symbolic logical unit (SYSIPT, SYSLOG, etc.) or programmer logical unit (SYS000, SYS001, etc.). X'cuu' is the hexadecimal number of the channel and unit to which the symbolic device is attached. $\left\{ \begin{array}{l} \underline{BG} \\ \overline{F1} \end{array} \right\} \ \text{indicates the specific partition to which the ASSGN is} \\ \left\{ \begin{array}{l} \underline{F2} \end{array} \right\} \ \text{being made} \ .$
SEND	Indicates end of supervisor generation .	[n]	Specifies the beginning address of the problem program area. An area should be reserved for supervision expansion and maintenance. The parameter is optional. If not specified, no area is reserved beyond the assembled last address of the supervisor.

Note 1: Rules for using DVCGEN

- 1. A separate DVCGEN macro instruction is required for each device.
- 2. The total number of DVCGEN macros must not exceed the total number of devices specified in the IODEV parameter of the IOTAB macro.
- 3. DVCGEN macros must be specified in ascending channel address sequence.
- 4. Switchable units (attached to more than one selector channel) must be defined once. They are defined on the lowest channel on which they are addressable.
- 5. The sequence of the DVCGEN cards determines the priority of the devices on their channel. Switchable units must be the last devices for each channel, and must be on consecutive channels.
- 6. The specifications of these macros may be altered by IPL ADD and DEL statements. See IPL PLM, GY24-5086.
- 7. Rules for SYSxxx:
 - a. The ASSGN macro allows SYSRDR, SYSLST, SYSPCH, and SYSIPT to be assigned to a tape or DASD. However, IPL unassigns any such
 - b. SYSLOG must also be assigned in BG, if assigned in foreground partition.
 - c. SYSLNK cannot be specified in either foreground partition.

Figure 4. Supervisor Macros (Part 5 of 5)

Macro	Туре	Code Generated	Critical Globals Set
SUPVR	generation	Defines low main storage	BG10 BG25 BG13 BG27 BG14 BG35 BG19 BG36 BG20 BG50 BG21 BG51 BG24 BG100 AG11
CONFG	generation	None	BG1 BG23 BG2 BG39 BG22 BG51 AG12
STDJC	generation	None	BG34 BG81
FOPT	generation	General cancel SVEREG routine General exit Background communication region and extension General entry SVC interrupt handler	BG0 BG60 BG2 BG61 BG4 BG62 BG5 BG71 BG6 BG72 BG7 BG73 BG8 AG2A BG14 AG7 BG15 AG10 BG16 AG13 BG18 AG21 BG26 AG22 BG30 AG23 BG32 AG28
			BG33 AG31 BG40 AG32 BG52 AG39
PIOCS	generation	None, directly calls inner macros.	BG3 BG11 BG9 BG12 BG10 BG31
SGTCHS	inner .	Channel scheduler Start I/O SIO accounting I/O interrupt	none
SGUNCK	inner	Unit check Error recovery exits	none
SGTCON	inner	VLDADR1 subroutine, ATNRTN routine, CCW chain, disk information blocks, error recovery block, SVC interrupt table, PC option table, and OC option table, physical transient save area, IDRA save area, logical transient save area.	none
SGDFCH	inner	Fetch subroutine	none
SGSVC	inner	Supervisor interrupts Program check interrupts External interrupts Console buffering routine	none
SGDSK	inner	Disk error recovery	none
SGTHAP	inner	Track hold, track free, set abnormal exit routine address, and asynchronous processing routines.	none
SMICR	inner	External interrupts for MICR type devices Program checks in stacker select routine Error recovery for test I/O and start I/O	none
ALLOC	generation	None	none

Figure 5. Macro Functions (Part 1 of 2)

Macro	Туре	Code Generated	Critical Globals Set
IOTAB	generation	Supervisor table expansions – SYSCLB LUB, PIBs, SVC Interrupt table, channel queue table (CHANQ), PUB, JIB, TEB, and TEBV.	AG2D
LUBGEN	inner	Generates NICL, FICL, and unassigned LUB tables, console buffers, and track hold table entries.	none
DVCGEN	generation	Overlays for PUB table entries.	AG8
ASSGN	generation	Overlays for LUB table entries.	none
SEND	generation	Generates console buffer and PTO patch areas; JAI partition tables, user save area, and label area; OBR/SDR routines. Calls inner macros COMMN for F1, F2, communications regions, COMMNEX for F1, F2, communications region extensions, TRTAB for ASCII translation tables, MCRAS for RMS resident coding and RTA. Defines end of supervisor nucleus, beginning of IDRA, A and B transient areas, start of problem program area, CE area, and BG save area.	none
SMCRR	inner	Machine check recording and recovery record builder.	none
COMMN	inner	Communications regions for all partitions.	none
COMMNEX	inner	Communications region extensions for all partitions.	none
TRTAB	inner	Generates ASCII translation tables.	none
MCRAS	inner	Generates RMS Monitor and RTA.	none
MAPLOWC	inner	Generates equates to address low core for RMS.	none

Figure 5. Macro Functions (Part 2 of 2)

<u>Global</u>	On Setting	<u>Purpose</u>
BG0	CE=YES Or n AP=YES AB=YES EU=YES TRKHLD=n ERRLOG=YES Or CLEAR MCRR=YES MICR=1412, 1419 or 1419D JA=YES JA=(n ₁ ,n ₂ ,n ₃) ASCII=YES MPS=YES OR BJF	Determines the length of the supervisor save area.
BG1	SP=YES	Determines whether the storage protect feature is used.
BG1QT	TP=QTAM	Determines QTAM support.
BG2	TIMER=YES JA=YES JA=(n ₁ ,n ₂ ,n ₃)	Determines whether the timer feature is used. Does not force BG0.
BG3	CHANSW=TSWTCH or RWTAU	Determines whether channel switching is supported (2816).
BG4	TEB=n	Determines if tape error statistics are to be accumulated and logged.
BG5	PTO=YES	Determines if physical transient overlap option is supported.
BG6	OC=YES	Determines if the asynchronous user interrupt key routine is supported. Does not force BGO.
BG 7	IT=F1, or F2, or BG	Determines whether the internal timer option is supported. Does not force BGO.
BG8	PC=YES	Determines if the user program check routine is supported.
BG9	CHANSW=RWTAU	Determines whether channel switching is supported (2404, 2804).
BG10	SELCH=YES	Determines whether selector channels are supported.
BG11	BMPX=YES	Determines whether burst mode devices will be supported on the multiplexor channel.
BG12	TAPE=7 or 9	Determines the type of tape support required.
BG13 *	AP=YES	Determines if asynchronous processing is supported. If yes, force on BG0, BG14, BG20.
BG14	WAITM=YES AP=YES	Determines if the wait multiple function is supported. Force on if AP is specified. Does not force on BG0.

Figure 6. Global Settings (Part 1 of 5)

Global	On Setting	Purpose
BG15 *	AB=YES	Determines if user abnormal termination routine is supported. Forces on BGO.
BG16 *	TRKHLD=n	Determines if the track hold function is supported. BG20 must be on (if it is not, it defaults to No).
BG18	CBF=n	Determines if console buffering option is supported.
BG19 *	MCRR=YES	Determines whether MCRR option is supported.
BG20	MPS=YES or BJF AP=YES	Determines whether multiprogramming support is required. Forces BGO.
BG21	TP=BTAM or QTAM	Determines whether teleprocessing support is required.
BG22	DEC=YES	Determines if the decimal feature is used. Does not force BGO.
BG23	FP=YES	Determines if the floating point feature is used. Does not force ${\tt BG0.}$
BG24	MPS=BJF	Determines if batched jobs will be run in foreground partitions. Forces BG0.
BG25	ERRLOG=any invalid setting	Indicates ERRLOG is set with an invalid option. Causes a message and terminates supervisor assembly.
BG26	PCIL=YES	Determines if PCIL is supported.
BG27	ERRLOG=RDE	Determines if RDE Support is required.
BG30	CCHAIN=YES	Determines if command chaining support for retry on I/O operation is used. Does not force BGO.
BG31	TAPE=9	Determines if 9 track tape support is required.
BG32	DASDFP=n,n	Determines whether the DASD file protect feature is supported. Does not force BGO.
BG33	SYSFIL=2311 or 2314	Determines if logical system I/O units are a disk device. Does not force ${\tt BGO}$.
BG34	DATE=MDY	Determines the type of date configuration to be supported.
BG35	MICR=1412, 1419, 1419D, 1270, 1275	Determines if any MICR type device is supported. Forces BG0.
BG36	MICR=1419D	Determines if 1419D (MICR type device with dual address adapter) only is supported. Forces BG0.

Figure 6. Global Settings (Part 2 of 5)

Global	On Setting	Purpose
BG38	OLTEP=YES	Indicates whether OLTEP is supported.
BG39	MODE= (a System/370 CPU)	Indicates RMS support for System/370.
BG40	RETAIN=YES	Indicates RETAIN/370 is Supported.
BG 41	DECK=YES	Job control options.
BG42	LIST=YES	Job control options.
BG43	LISTX=YES	Job control options.
BG44	SYM=YES	Job control options.
BG45	XREF=YES	Job control options.
BG46	ERRS=YES	Job control options.
BG47	CHARSET=48C	Job control options.
BG48	DUMP=YES	Job control options.
BG49	rog=AE2	Job control options.
BG50	EU=YES	Determines if emulator interface is generated. Forces on ${\tt BGO}$.
BG51	EU=RELOC	Determines if the relocatable version of CS/40 is used. Forces on BGO, BG50.
BG52	IDRA=YES	Indicates whether IDRA is supported.
BG60 *	TEBV=(device,n)	Determines if the Tape Error Statistics by Volume is supported. Does not force BGO.
BG61	TEBV=(DASD,n)	Determines if TEBV Device is DASD. Does not force BGO.
BG62 *	EVA=(rth,wth,n)	Determines if Error Volume Analysis is supported. Does not force BGO.
BG 71	JA=YES or JA=(n ₁ ,n ₂ ,n ₃)	Indicates whether JAI is supported.
BG72	JA=(n ₁ ,n ₂ ,n ₃)	Indicates whether count of SIOs is made.
BG73	JALIOCS=(n ₁ ,n ₂)	Indicates whether JAI label processing is supported.

Figure 6. Global Settings (Part 3 of 5)

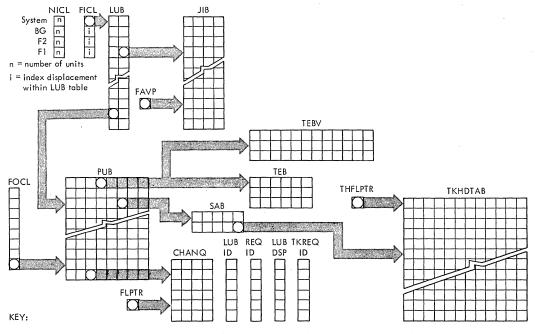
<u>Global</u>	On Setting	<u>Purpose</u>
BG81	SPARM=YES	Determines if SYSPARM is supported.
BG99	ALLOC F1=nK, F2=nK	Special sequence check for ALLOC macro within supervisor.
BG100*	ASCII=YES	Determines if ASCII translation tables are generated.
BG126	CHANSW=YES	Channel switching. Device can be attached to more than one selector channel.
BG127		Sequence check for DVCGEN macro.
AG1QT	TP=QTAM _n	Number of problem programs in QTAM system at one time.
AG1	IODEV=n	Number of entries for PUB Table.
AG2	Can be set by TEB, TEBV, EVA	Number of volume error blocks.
AG2A	TEB=n	Indicates number of Tape Error Blocks generated in FOPT macro.
AG3	CHUN=X'cuu'	Specifies number of channel (for example, X'cuu')
AG4	BGPGR=n	Number of BG programmer LUBs.
AG5	F2PGR=n	Number of F2 programmer LUBs.
AG6	F1PGR=n	Number of F1 programmer LUBs
AG7	SKSEP=YES or n	Determines that the seek separation option is desired. Does not force BGO.
AG8	SKSEP=YES or n	Sets count of direct access storage devices generated in DVCGEN.
AG9	$\begin{pmatrix} \text{CHANQ=} \\ \left(\frac{6 \text{ or } 6 + \text{CBF}}{n}\right) \end{pmatrix}$	Length of channel queue.
AG10 *	CE=YES or n	Indicates that an area is reserved for CE routines.
AG11 *	ERRLOG=YES, RDE, or n	Sets count of Statistical Data Records.
AG12	MODEL=nn or nnn PORT=155	Indicates model of CPU. Does not force BG0.
AG13	PCIL=YES	Number of system class LUBs.
AG15		Checks macro sequence of supervisor macros.

Figure 6. Global Settings (Part 4 of 5)

Global	On Setting	Purpose
AG16	DASDFP= $ \begin{pmatrix} n, n, & {2311 \\ 2314 \\ 2321 \end{pmatrix} $	First channel with DASD devices for file protect.
AG17	DASDFP= $\begin{pmatrix} n, n, & {2311 \\ 2314 \\ 2321 \end{pmatrix}$	Last channel with DASD devices for file protect.
AG18	SYSFIL= $ \begin{cases} 2311, & n_1, n_2 \\ 2314, & n_1, n_2 \end{cases} $	n ₁ Parameter of SYSFIL.
AG19	SYSFIL= {2311}, {n ₁ , n ₂ } {2314}, {n ₁ , n ₂ }	n ₂ Parameter of SYSFIL.
AG20	MCRR=YES	Set to value equal to number of PUBs when MCRR is supported.
AG21	IT=BG	Determines if a timer interrupt routine is for a BG program.
AG22	IT=F1	Determines if a timer interrupt routine is for an F1 program.
AG23	IT=F2	Determines if a timer interrupt routine is for an F2 program.
AG25	F1=nK	Number of blocks for F1 (must be in increments of 2K).
AG26	F2=nK	Number of blocks for F2 (must be in increments or 2K).
AG27	TRKHLD=n	Indicates number of tracks that can be held.
AG28	CBF=n	Indicates number of console buffers generated in LUBGEN. Does not force BGO.
AG31	EVA=(rth,wth,n)	Indicates the Read Error Threshold specified in EVA.
AG32	EVA=(rth,wth,n)	Indicates the Write Error Threshold specified in EVA.
AG39	JA=(n ₁ , n ₂ , n ₃) JALIOCS=(n ₁ , n ₂)	Indicates number of devices for which SIO counts are made. Indicates whether user save area and label processing are supported.
AG41	LINES=n	SYSLST line count.
AG53		Number of LUBs.
AG54	MRSLCH=YES	Indicates MICR type device is on a selector channel.

^{*}These globals determine if extension(s) to the communication region(s) are generated.

Figure 6. Global Settings (Part 5 of 5)



NICL (Number in Class)

: The first byte contains the number of system class units. The second, third, and fourth bytes contain the number of programmer class units (BG, F2, F1) (Figure 23).

FICL (First in Class)

: The first byte points to the first system class unit in the LUB table. (Always the first LUB table entry.) The second byte points to the first programmer class unit in the LUB table BG area. The third points to the first programmer class unit in the LUB table F2 area. The fourth points to the first programmer class unit in the LUB table F1 area (Figure 23).

LUB (Logical Unit Block) Table

: The first byte points to a PUB table entry (if the logical unit is assigned) or contains X'FF'. The second byte points to a JIB table entry or contains X'FF' (Figure 23).

PUB (Physical Unit Block) Table

: The first two bytes contain the channel and unit address of the physical device; the third a CHANQ pointer; the fourth a TEB pointer; the fifth device type codes; the sixth a device characteristic code or a SAB pointer; the seventh the channel scheduler flag; and the eighth has the job control flag (See Figure 18).

FOCL (First on Channel List)

: The first byte points to the first PUB (highest priority) on channel zero. The next byte points to the first PUB (highest priority) on channel one, etc. A hexadecimal FF indicates the associated channel is not supported.

TEB (Tape Error Block by Unit)

: One TEB is built for each tape unit at supervisor generation time if tape error statistics by unit are required (Figure 20).

TEBV (Tape Error Block by Volume)

: One TEBV is built for each tape unit at supervisor generation time if tape error statistics by volume are required (Figure 21).

FAVP (First Available Pointer)

: A one-byte pointer to the next available JIB entry.

JIB (Job Information Block)

: The first two bytes contain extent or LUB information. The third contains ownership and JIB flags. The fourth contains JIB chaining information (Figure 19).

CHANQ (Channel Queue) Table

: The first byte contains the chain field (a pointer to the next in queue). The last three bytes contain the CCB address (Figure 17).

LUBID (LUB Identification)

: A one-byte pointer to the LUB making the I/O request.

REQID (Requestor Identification)

: A one-byte pointer to the program containing the CCB (Figure 17).

LUBDSP (LUB Displacement)

: A one-byte value equal to the absolute LUB number (CCB byte 7).

FLPTR (Free List Pointer)

: A one-byte pointer to the next free entry in the channel queue (Figure 17).

SAB (Seek Address Block)

: A four-byte (BCCH) address that is the current disk address of the device plus a fifth byte that contains a Track Hold Table pointer or X'FF'. If the Track Hold function is not supported, the fifth byte contains X'00'.

TKHDTAB (Track Hold Table)

: The first byte contains a pointer to the next available entry (or X'FF'); bytes 2 - 4 have CCB address of the requesting task; bytes 5 – 10 have a disk address (BBCCHH) of track being held; byte 11 has key of owning track; and byte 12 has two uses: bit 0=1 means a task is waiting for the track, and bits 4 – 7 count the number of holds on the track. (Figure 24). Note: The number of holds is one more than the value of bits 4 - 7 of the last byte.

THFLPTR (Track Hold Free List Pointer)

: A one-byte pointer to the next free entry in the Track Hold Table.

TKREQID (Track Requestor Identification): A one-byte pointer to the PIB of the task requesting I/O.

Figure 7. I/O Table Interrelationship

COMREG*												···					-		
hexadecimal	0		8	OA			0C							20 24		28			2C
Displacement decimal	0 Date		Address o	f Ado	Address of		Problem Program Use			UPSI Byte	Job Name			Storage of L		Address ast Phas hed or led	Byte o with I		Label Area Length
	XXXXXXX		XX		XX		XXXXXXXX		⟨X	X Z		XXXXXXX		XXXX X				XXXX XX	
Displacement hexadecimal Displacement decimal	2E	30	34	35		36	1	37	- 1	38			3A	1	3B	3C		3E	
	PIK (PID)	Storag	End of Machine Storage Confg. Address Byte		Confg. La Byte I/		ndard guage nslator	Dump Log of ASCI Optio	o, and	Job Contro Byte	1	Linkage Control Byte	58 Language Translator Control Byte		Job Durati Indico Byte	itor Lal	dress of of		S
	XX	XXX	х х		Х		Х	Х		Х		Х		Х	Х		XX	XX	
						_			J	Job Con	trol	Switches							
Displacement hexadecimal Displacement decimal	40	42	44	46	48		4A	40		4E		4F			58	5.4		5C	
	64	66	68	70	72		74	76		78		79			88	90		92	
	Address of PUB	Addres of FAVP	f of		Address Add of EB FIC		of		ddres f UB	S Line Coun for SYSL			m D	Date LIOC Comm Bytes		n. 1st Part o		of of Last	
	XX	XX	XX	Х	X	XX	XX		XX	X		XXXX	XΧ	XXX	XX		XX		XX
Displacement hexadecimal Displacement decimal	5E 94		60	Į.	62 98		64		66			68 6A			6C		6E		
	Length of LUB ID Queue = No. of Channel		Address Disk Informa Block (I	of tion	Address of Error Recovery Block		+		Address		1	Address of Key OC Option Pro Table less wit		Key Prog	of Adgram the		Address of Logic the LUBID Transi Key		
	XX :		XX	X		X >		XX		XX	XX			XX		XX		XX	
Displacement hexadecimal Displacement decimal	70				7C		7E		80	30		84		86	87 8				
	112			+	124		+		128		132		\dashv	134	135 136		·	1	
	Supervisor Constants			2r Po	Address of 2nd Part of PIB Table		Address of MICR DTF Table (PDTABB)		QT. Ved	Address of QTAM Vector Table		Address of BG Comm. Region		tion Indi-	System Pointe Config- Comm uration Region Byte 2 Extens		m. on		
	XXXXXXXXXXX				XX		XX		>	XXXX		XX		X	х х		XXXX		

^{*} The address of the communications region is in fixed location X'14' - X'17'.

Displacement values illustrated can be used to access the listing and/or the key that follows the figure. The key offers more detailed information about each area when necessary.

Figure 8. Supervisor Communications Region (Part 1 of 5)

Key to Con	nmunications Region Disp	lacements:									
0		N/YY obtained from the job control date statement. Format controlled by COMREG + 53 Byte, date convention bit 0).									
8	Address of the problem	program area.									
10		g of the problem program area. Y (EOSSP)=Y (PPBEG) if the storage protection option has not SP) equals the first main storage location with a storage protection key of 1, if storage protection									
12	User area. If seek sepa address block.	User area. If seek separation option is specified, bytes 12 and 13 are used at IPL time for the address of the seek address block.									
23	User program switch inc	licator.									
24	Job name set by the jol	o control program from information found in the job statement.									
32	determines the address,	st byte of the problem program area as determined by the IPL program (Clear storage routine ENDRD routine of \$\$A\$IPL2 stores it.), or the address of the uppermost byte of the partition occessing of the ALLOC statement.									
36		st byte of the last phase of the problem program fetched or loaded. The initial value (as shown) fetch or load to the problem program area.									
40	operand on the EXEC st phases. The address va	orage address of the phase among all the phases having the same first four characters as the ratement. For the background partition only, job control builds a phase directory of these use may be incorrect if the program loads any of these phases above its link-edited origin atement has no operand, job control places in this location the ending address of the program									
44	Length of the problem	program label area.									
46	Program Interrupt Key start of the PIB table to	- PIK (if asynchronous processing is not supported): Value is equal to the displacement from the the PIB for the task. OR									
		D (if asynchronous processing is supported): Value is hex 10, 20, or 30 to identify the partition a subtask is running. (See the communications region extension, displacement 18, for the PIK									
		zero. rains the key of the program that was last enabled for interrupts, or the partition identifier in AP supervisor.									
	<u>Task</u>	PIK (PID) Value									
	*All Bound BG *F2 *F1 Attn Rtn Quiesce I/O Supervisor	X'00' X'10' X'20' X'30' X'40' X'50' X'60'									
	*These tasks do not	exist in a non-MPS supervisor.									
48	Logical end of main sta	rage address.									

Figure 8. Supervisor Communications Region (Part 2 of 5)

```
52
          Machine Configuration Byte (Values set at supervisor generation time.)
               Bit 0: 1 = Storage protect feature
                      0 = No storage protect feature
                  1: 1 = Decimal feature
                      0 = No decimal feature
                  2: 1 = Floating-point feature
                      0 = No floating-point feature
                     1 = Physical transient overlap option
                      0 = No physical transient overlap option
                     1 = Timer feature
                      0 = No timer feature
                  5: 1 = Channel switching device
                      0 = No channel switching device
                  6: 1 = Burst mode on multiplex channel support
                      0 = No burst mode on multiplex channel support
                  7: Reserved
53
          System Configuration Byte
              Bit 0: 1 = DDMMYY

0 = MMDDYY (Date convention bit set at generation time by STDJC)
                  1: 1 = Multiprogramming environment
                      0 = Batch job environment
                  2: 1 = DASD file-protect supported
                      0 = No file-protect support for DASD
                  3: 1 = DASD SYSIN - SYSOUT
                      0 = No DASD SYSIN - SYSOUT
                  4: 1 = Teleprocessing
                      0 = No teleprocessing
                     1 = Batch job in foreground
0 = No BJF
                  6: 1 = Asynchronous processing
                      0 = No AP
                     1 = Track Hold
                      0 = No Track Hold
54
          This byte contains the standard language translator I/O options (set by the STDJC macro).
              Bit 0: DECK option
                                         1 = yes, output object modules on SYSPCH
                  1: LIST option
                                         1 = yes, output source module listings and diagnostics on SYSLST
                  2: LISTX option
                                         1 = yes, output hexadecimal object module listings on SYSLST (compilers only)
                                         1 = yes, output symbol tables on SYSLST/SYSPCH
                  3: SYM option
                 4: XREF option
                                         1 = yes, output symbolic cross reference list on SYSLST
                 5: ERRS option
                                         1 = yes, output diagnostics on SYSLST (compilers only)
                      CHARSET option
                                         1 = 48, input on SYSIPT is 48 or 60 character set
                      Reserved
55
          This byte contains the standard supervisor options for abnormal EOJ and control statement display, and the indicator
          for the presence of the ASCII-EBCDIC and EBCDIC-ASCII translation tables.
              Bit 0: Always on
                  1: DUMP option
                                         1 = yes, dump registers and storage on SYSLST
                  2: Reserved
                                         1 = yes, list all control statements on SYSLST
                  3: LOG option
                4-6: Reserved
                 7: ASCII option
                                         1 = yes, ASCII supported
```

Figure 8. Supervisor Communications Region (Part 3 of 5)

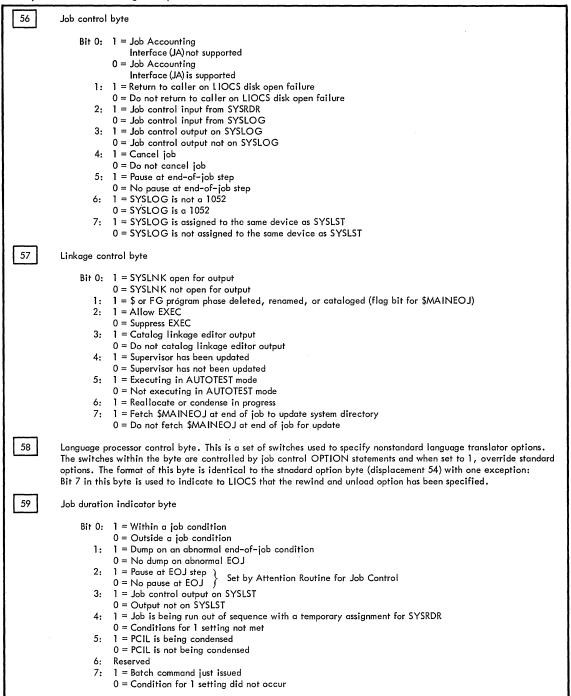


Figure 8. Supervisor Communications Region (Part 4 of 5)

Key to Communications Region Displacements: 60 Binary disk address of the volume label area (label cylinder). 62 76 As illustrated (Figures for information blocks, I/O tables, and pointers begin at Figure 7 which refers to more detailed Figures). 78 Set to the value nn specified in the LINES = nn parameter of the STDJC macro. 79 The format of the system date contained within this field is determined by the IPL program from information supplied in the date convention byte (displacement 53). Bytes 85 - 87 contain the day count. 88 Bytes reserved for use by LIOCS. Transient dump programs insert a key to indicate to the LIOCS end-of-volume routine, \$\$BCMT07, that it was called by a B-transient. 90 Address of the first part of the program information block (PIB) table. (See Figures 15, and 16.) 92 1D number of the last checkpoint. Temporary indicator of file protected DASD. Used at IPL time, when DASDFP is specified. 94 Length of the LUBID queue (in bytes). This equals the number of channel queue entries. It can also be used to access the REQID, LUBDSP, and TKREQID queues: (See Figure 17.) 96 Address of disk I/O position data. This is the starting address of the disk information block (DIB) table (See Figure 12). 98 Address of the beginning of the error recovery block. The error recovery block contains addresses of error recovery exits, error recovery queue information that can be used by physical transients routines, and defines storage for the error queue entries (See Figure 43). 100 104 As illustrated (See Figure 13). 106 Key of the program (BG, F2, or F1) that has timer support. 108 As illustrated (See Figure 17). 110 Logical Transient Key (LTK) contains the same value as the PIK (PID) (Displacement 46) when the logical transient is requested. When the transient area is not in use, LTK is equal to zero. The SVC 2 routine sets the LTK. The SVC 11 routine resets the LTK. 112 Supervisor constants: DOLLARBO (4 bytes) = C'\$\$BO' (5 bytes) = XL5'0' SSKADR (3 bytes) = Adcon of LTSVPT, logical transient save pointer ITARFA 124 Address of second part of program information block (PIB) table (See Figure 14). 126 Address of PDTABB, table of DTF addresses for MICR support (See Figure 10). 128 Address of QTAM vector table (IJLQTTAD). 132 Address of background communications region. 134 Option Indicator Byte Bit 0: 1 = MCRR indicated for OBR writer 0 = No MCRR indicated for OBR writer 1: 1 = EU interface active 0 = EU interface not active 2: 1 = Teleprocessing request 0 = No teleprocessing request 3: 1 = Supervisor support for only 9-track tape 0 = Supervisor does not support 9-track tape exclusively 4: Reserved 1 = RETAIN/370 support generated 0 = RETAIN/370 support not generated 6-7: Reserved 135 System Configuration Byte 2 Bit 0: 1 = PCIL supported 0 = PCIL not supported 1-7: Reserved

Figure 8. Supervisor Communications Region (Part 5 of 5)

Pointer to communications region extension (See Figure 9.)

136

	1	8	0C		10	12	14		18	1C	20
Displacement) (Decimal Displacement)		8	12		16	18	20		24	28	32
CE Table Address						ID of Task Running (PIK)	Task F queste Table (TKID	er ID Address	Address Used by QTAM (MVCFLD)	SDR Table Address (SDRTABLE)	TEBV Table Address (TEBVTAB)
xxxx	xxxx	xxxx	xxxx		XX	XX	XX	xx	xxxx	xxxx	XXXX
24 (Hexadecimal	28	2C	30	34		38		3C			
Displacement 36 (Decimal	40	44	48	52		56		60			
Displacement				ļ 					4		
OLTEP Linkage Address	RMS Linkage Address (RASLINK)	ASCII-EBCDIC Translation Table Address	(Reserved)	Tabl	Common e Address CTCOMN	1	ddress	&SYSPARM Field Address			
XXXX	xxxx	XXXX	XXXX		XXXX	XXXX	×.	xxxx			
B Difference between addresses of first part of PIB table and second part of PIB table (PIBDIFF). Abnormal Termination Table Address (minus 8) (ABPTR). Identification (LID) of the task owning the Logical Transient Area. Contains same value as PIK (displacement 18) when LTA is in use. Contains zero when LTA is not in use. Program Interrupt Key (PIK) if asynchronous processing is supported. Value is equal to the displacement of the start of the PIB table to the PIB of the main task or subtask being selected (running). First byte – zero Second byte – contains the displacement into the PIB table for a maintask or a subtask. Maintask – PIK value is hex 10, 20, or 30.											
16 Identificati Contains ze 18 Program Int to the PIB of First by Second Mair	on (LID) of the ero when LTA is errupt Key (PIK of the main task te – zero byte – contains ntask – PIK valu	task owning the s not in use. (if asynchronous or subtask being the displacement	Logical Transpressing selected (rule into the PII or 30.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB of First by Second Mair Subto	on (LID) of the ero when LTA is errupt Key (PIK) of the main task te – zero byte – contains nake – PIK valuesk – PIK value	task owning the s not in use. (1) if asynchronous or subtask being the displacement us is hex 10, 20,	Logical Transpropers of the PIF or 30.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB o First by Second I Mair Subto 20 Task Reques	on (LID) of the ero when LTA is errupt Key (PIK) of the main task te – zero byte – contains nake – PIK valuesk – PIK value	task owning the s not in use. (1) if asynchronous or subtask being the displacement us is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR)	Logical Transpropers of the PIF or 30.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB o First by: Second I Mair Subto 20 Task Reques 24 MVCFLD and	on (LID) of the ero when LTA is errupt Key (PIK) of the main task te – zero byte – contains task – PIK value ster ID Table Address used by (ddress used by (ddress used by (ddress weed by (dd	task owning the s not in use. (1) if asynchronous or subtask being the displacement us is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR)	Logical Trans processing selected (rut into the PII or 30.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB o First by Second I Mair Subto 20 Task Reques 24 MVCFLD at 28 Statistical I	on (LID) of the erro when LTA is errupt Key (PIK) of the main task te – zero byte – contains stask – PIK value ster ID Table Arddress used by (Data Recorder 1	task owning the s not in use. (3) if asynchronous or subtask being the displacement us is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR)	Logical Trans processing selected (rule into the Plicor 30.00, FO.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB o First by Second I Mair Subto 20 Task Reques 24 MVCFLD ac 28 Statistical I 32 Tape Error I	on (LID) of the erro when LTA is errupt Key (PIK) of the main task te – zero byte – contains stask – PIK value ster ID Table Arddress used by (Data Recorder 1	task owning the s not in use. (1) if asynchronous or subtask being the displacement us is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR) QTAM. Table Address (SD me Table Address	Logical Trans processing selected (rule into the Plicor 30.00, FO.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB of First by Second Mair Subto 20 Task Reque: 24 MVCFLD at 28 Statistical 32 Tape Error 36 Pointer to C	on (LID) of the erro when LTA is errupt Key (PIK of the main task te - zero byte - contains task - PIK value ster ID Table Address used by (Data Recorder 1)	task owning the s not in use. (c) if asynchronous or subtask being the displacement use is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR) QTAM. Table Address (SD me Table Address	Logical Trans processing selected (rule into the Plicor 30.00, FO.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB of First by Second I Mair Subto 20 Task Reques 24 MVCFLD at 28 Statistical II 32 Tape Error II 36 Pointer to C 40 RMS Linkage	on (LID) of the erro when LTA is errupt Key (PIK of the main task te - zero byte - contains stask - PIK value ster ID Table Address used by (Data Recorder Tellocks by Volur DLTEP Linkage pe Area Address	task owning the s not in use. (c) if asynchronous or subtask being the displacement use is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR) QTAM. Table Address (SD me Table Address	Logical Trans processing selected (rule into the Plicor 30.00, FO.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB of First by Second I Mair Subto 20 Task Reques 24 MVCFLD at 28 Statistical II 32 Tape Error II 36 Pointer to C 40 RMS Linkage	on (LID) of the erro when LTA is errupt Key (PIK of the main task te - zero byte - contains stask - PIK value ster ID Table Address used by (Data Recorder Tellocks by Volur DLTEP Linkage pe Area Address	task owning the soot in use. (c) if asynchronous or subtask being the displacementure is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR) QTAM. Table Address (SD me Table Address Addresses 6 (RASLINK)	Logical Trans processing selected (rule into the Plicor 30.00, FO.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB of First by Second Mair Subto 20 Task Reques 24 MVCFLD at 28 Statistical 32 Tape Error 36 Pointer to C 40 RMS Linkag 44 ASCII-EBCI 48 (Reserved)	on (LID) of the ero when LTA is errupt Key (PIK) of the main task te – zero byte – contains nitask – PIK value ster ID Table Address used by (Data Recorder TBlocks by Volur DLTEP Linkage pe Area Address	task owning the soot in use. (c) if asynchronous or subtask being the displacementure is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR) QTAM. Table Address (SD me Table Address Addresses 6 (RASLINK)	Logical Trans processing selected (rule into the Plicor 30.00, FO.	is sup unning B tabl	pported. \ g).	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB of First by: Second I Main Subto 20 Task Reques 24 MVCFLD at 28 Statistical I 32 Tape Error I 36 Pointer to C 40 RMS Linkag 44 ASCII-EBCI 48 (Reserved) 52 JAI Commo	on (LID) of the ero when LTA is errupt Key (PIK) of the main task te – zero byte – contains task – PIK value ster ID Table Address used by (Data Recorder 1 Blocks by Volur DLTEP Linkage pe Area Address DIC Translation in Table Address	task owning the s not in use. (c) if asynchronous or subtask being the displacement us is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR) QTAM. Table Address (SD me Table Address (RASLINK) Table Address.	Logical Transprocessing selected (runt into the Plicor 30.0, Fo	is supponing	oported. \alpha	/alue is eq	ual to t	he displacer			
16 Identificati Contains ze 18 Program Int to the PIB of First by Second Mair 20 Task Reques 24 MVCFLD at 28 Statistical I 32 Tape Error I 36 Pointer to 0 40 RMS Linkag 44 ASCII-EBCI 48 (Reserved) 52 JAI Commo 56 JAI Partition	on (LID) of the ero when LTA is errupt Key (PIK) of the main task te – zero byte – contains task – PIK value ster ID Table Address used by (Data Recorder 1 Blocks by Volur DLTEP Linkage pe Area Address DIC Translation in Table Address	task owning the s not in use. (c) if asynchronous or subtask being the displacement use is hex 10, 20, is hex 70, 80, 9 ddress (TKIDPTR) QTAM. Table Address (SD me Table Address (ARASLINK) Table Address.	Logical Transprocessing selected (runt into the Plicor 30.0, Fo	is supponing	oported. \alpha	/alue is eq	ual to t	he displacer			

Figure 9. Communications Region Extensions

The table of DTF addresses (PDTABB) contains six 8 - byte entries; one for each external line of the direct control feature on the system.

				PDT	<u>ABB</u>			
Byte —	 0	1 1 1	2	33	4	, 5	, 6 ,	7
. ↓		1				DTF ac	ddress for Mi	CR:
0	NI	PDSTAT+1,	Χ'	FE'	L	Device	on line 7	
8	NI	PDSTAT +1,	X'	FD'	i.	Device	on line 6	
16	NI	PDSTAT +1,	Χ'	FB'	wnership	Device	e on line 5	
24 _	NI	PDSTAT+1,	Χ¹	F7'		Device	e on line 4	
32 _	NI_	PDSTAT+1,	Χ'	EF'	T 0 E T	Device	on line 3	
40	NI	PDSTAT+1,	Χ'	DF'		Device	on line 2	
					+			
				Bacl	kground =	10		
				Fore	ground 2	= 20		
				Fore	ground 1	= 30		

● Bytes 0-3 -- Contain an 'AND' instruction that is executed in main line coding to turn off the external line status after its detection.

PDSTAT+1 will contain one or more of the following interrupt codes:

PSW Interrupt	Interrupt Code	External
Code Bit	(PSW Bits 26 - 31) *	Interrupt Cause
31	nnnnnnn l	External signal 7
30	nnnnnnln	External signal 6
29	nnnnn l nn	External signal 5
28	nnnnlnnn	External signal 4
27	nnnlnnnn	External signal 3
26	nnlnnnnn	External signal 2

- Byte 4 -- Contains the flag of the partition containing the DTF.
- Bytes 5-7--Contain the address of the DTF table.

Table of pointers (PDTABA) to DTF addresses associated with the external interrupt line. The table is set up to handle the status in descending order from Bit 31 to Bit 26 of the external old PSW.

DDTARA

			PDIA	<u>DA</u>			
- 0	1	2	3	4	5	6	7
00	08	00	10	00	08	00	18
00	80	00	10	00	80	00	20
00	08	00	10	00	08	00	18
00	80	00	10	00	08	00	28
00	- 08	00	10	00	08	00	18
00	08	00	10	00	08	00	20
00	08	00	10	00	08	00	18
00	08	00	10	00	08	00	
	00 00 00 00 00 00	00 08 00 08 00 08 00 08 00 08 00 08	00 08 00 00 08 00 00 08 00 00 08 00 00 08 00 00 08 00 00 08 00 00 08 00 00 08 00	00 08 00 10 00 08 00 10	00 08 00 10 00 00 08 00 10 00 00 08 00 10 00 00 08 00 10 00 00 08 00 10 00 00 08 00 10 00 00 08 00 10 00 00 08 00 10 00 00 08 00 10 00	00 08 00 10 00 08 00 08 00 10 00 08 00 08 00 10 00 08 00 08 00 10 00 08 00 08 00 10 00 08 00 08 00 10 00 08 00 08 00 10 00 08 00 08 00 10 00 08 00 08 00 10 00 08	00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00 00 08 00 10 00 08 00

^{*}n = other external - interrupt conditions.

Bytes 126 and 127 (X'7E'-'7F') of the communications region contain the address of these tables. Label PDTABB identifies the first byte of the first table. These tables are also used for optical reader/sorters.

Figure 10. Tables for MICR DTF Addresses and Pointers

Displacement	Label	Description
0-15	(ACCTCOMN) ACCTSVRG	Temporary register save area.
16-17	ACCTSVRX	Save area for remainder of overhead counter times distributed by partition on exit.
18-19	ACCTSVRE	Save area for remainder of all-bound counter times distributed by partition on entry.
20-23	ACCTPCNT	Count of partitions using JAI.
24	ACCTSAID	Owner of physical transient area*.
25	ACCTFAID	Interrupted program*.
26	ACCTRAID	Active program*.
27	ACCTSWCH	Accounting switches: if bit = 1, true; if bit = 0, not true.
		bit 0 – cancel accounting bit 1 – no active partitions bit 5 – \$JOBACCT in F1 bit 2 – catalog in process bit 6 – \$JOBACCT in F2 bit 3 – alternate label area bit 7 – \$JOBACCT in BG
28-31	ACCTIME	Start time of current accounting interval, in complement format.
32-33	ACCTRESC	Reserved.
34-35	ACCTUSEP	Address of user save area (ACCTUSER).
36-39	ACCTBLES	Address of BG Job Accounting Table.
40-43		Address of F2 Job Accounting Table if BJF; otherwise zero.
44-47		Address of F1 Job Accounting Table if BJF; otherwise zero.
48-53	ACCTSEAS	Seize blocks; serve as overlapped Event Control Blocks.
		TS Bit (reserved) Wait Bit 1 PIK 1 Wait Bit 2 PIK 2 TS Bit: X'00' = no \$JOBACCT running X'FF' = \$JOBACCT active
54-55	ACCTUSEL	Length of user save area, set with 4th operand of global AG39.
*Note: X'0	0' = all bound, X'10'	= BG, X'20' = F2, X'30' = F1, X'40' = overhead and FG if SPI.

Figure 11. Job Accounting Interface Common Table (ACCTCOMN)

		-																T						
				Cu	rrent	Addr	ess						End A	ddres	S		R	U.L.	L.L.		R.	.c.	Rese	rved
syslnk	В	В	С	С	Н	Н	R	Р	-			· · · · · · · · · · · · · · · · · · ·	- This	area	not u	used f	or SY	SLNK	DIB					
SYSIN	В	В	С	С	Н	Н	R	K	D	D	В	В	С	С	Н	Н	Х	Н	Н	*	xx	XX		
SYSPCH																				*				
SYSLST																				*				
Number of Bytes			-	- 7 - -			>		- 3 - -	>	-		— 6	, —		>	~ 1 >	←1 →	 →1 →	4]+	2	·	- -2	2 →

KEY: Current Address: The next address to be used (for both input and output).

End Address : The last address within the limits of the extent.

: Maximum number of records per track.

U.L.

: Upper head limit

L.L.

: Lower head limit

R.C.

: Record Count - residual capacity for beginning of operator notification. This is set at system generation time with the SYSFIL parameter, or after IPL with the SET statement (RCLST and/or RCPCH operands). A warning message is issued by job control after end-of-job step when the minimum number of remaining records has been reached or exceeded during the previous job.

Р

: Starting cylinder of Private Core Image Library, if PCIL is assigned.

KDD

: Key and data length for the symbolic device.

KDD for SYSIN = X'000050'KDD for SYSPCH = X'000051'

KDD for SYSLST = X'000079'

Bytes 96 and 97 (X'60' - '61') of the communications region contain the address of the SYSLNK entry. Label DSKPOS identifies the first byte of the table.

Figure 12. Disk Information Block (DIB) Table

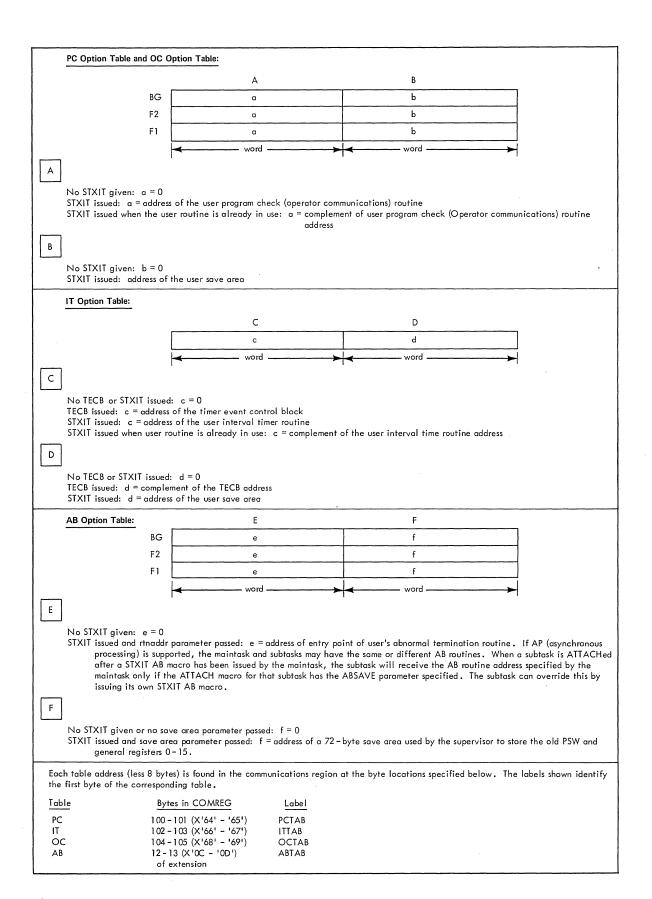


Figure 13. Option Tables

Byte Number		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	= 1 <i>6</i> B _{>}
All Bound PIB				Rese	rved			Priori All B Pl (Low	ity of ound IB		Rese	rved		H' All B PI Displa	ound	Rese	rved	L
Background PIB	•		ess of Comm.	Syst LUB I		Rese	rved	Priori BG (No				Termino		BG	010' PIB cement	Rese	rved	
FG2 PIB (Note 1)	Ò	Area C Reg		Syst LUB I		Rese	rved	Priori F2 (No				Terminony, or		F2	I 020' PIB cement	Reser	ved	
FG1 PIB (Note 1)		Area (Reg	ess of Comm. gion te 2)	Syst LUB I		Rese	erved	Priori F1 (No				Terminon ny, or		Fl	030' PIB cement	Reser	veď	
Attention PIB	Þ	BG (ess of Comm.	0	0	Rese	erved	H' Priori Atter P	ity of		F'	0' 	-	Attent	040' ion PIB cement	Reser	veď	
Quiesce I/O PIB	Þ			Rese	rved			H' Prior Quid I/O	ity of esce		F¹	0'		Quies	0050' ce PIB cement	Reser	ved	
Supervisor PIB	1			Rese	rved			Prior Super P	1' ity of rvisor IB jhest)		F	 		Supe	I 1060' rvisor IB cement	Reser	ved	
Subtask PIB (Note 3)	•	Area	ess of Comm. gion	Sys LUB I	tem ndex	Resi	ervēd	Sub	ity of task te 4)			dress fo , or F'(Displa	I PIB Icement aintask	Resei	ved	

Note 1. Generated only if MPS is specified.

Note 2. Always background communications region except when MPS = BJF.

Note 3. Total of nine subtasks generated, and only when AP is specified.

Note 4. Will be filled in with halfword indicating the relative priority of task in the system (range H'4' to H'15', the lower the number the higher the priority).

Bytes 124 and 125 (X'7C'-'7D') of the communications region contain the address of the second part of the PIB table. Label PIB2AD identifies the first byte of the table. The second part of PIB table comes before the first part in storage allocation. Refer to Figure 2.

Figure 14. Second Part of Program Information Block (PIB) Table

Byte Number		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AII Bound PIB		Flag Byte See A *	Reserved	SP P	refix		nch Instru All Bound						Ręsei	ved			
Problem Program PIB (Note 1)		Flag Byte See B *	Cancel Code (Fig. 36)	SYSLO (BG, F2	OG ID , or F1)	NOP Instruct- ion (CR)		ldress of ion Save		Number of Core Blocks (Note 2)	of t	ss of the he Partit		PIB Assign Flag See D	User LUB Index	Number of Program LUBs	Flag Byte See C *
Attention PIB	Ŷ	Flag Byte See E *	Cancel Code (Fig. 36)	SYSLO (AI		Branch Code (BC)		Address of Save Are ==Remain BC Ins	ea .	Switch Byte See F	(co	Transient ontains sa rea addre	ve	X'07' See D *	Reserved	Addre the Lo Trans	gical
Quiesce PIB	 	Flag Byte See A *	Cancel Code (Fig. 36)		/&' 		anch Inst			Scratch Byte X'00'	X'00'	Cho X'04'	unnel PUI	3 Table II	ndex Valı X'10'	ves X'14'	X'18'
Supervisor PIB	Þ	Flag Byte See A *	Cancel Code (Fig. 36)	SP Pr	refix		ranch Inst eneral Ex			Addre SYSRE		Length Queue	of Error Entry	Cor X'1F'	nstants to 2-5 of X'05'		tes X'00'
Subtask PIB for AP (Note 3)		Flag Byte See B *	Cancel Code (Fig. 36)	SYSLO (BG, F2	G ID 2, or F1)	NOP Instruc- tion	1	dress of to		Number of Core Blocks (Note 2)	Or Mc	dress of t igin of th iin Task		P1B Assign Flag See D	User LUB Index	Number of LUBs	Flag Byte See C

Note 1: Three problem program PIBs are built in this sequence when the MPS or BJF feature is selected as a generation option:

Background PIB Foreground 2 PIB Foreground 1 PIB 16 Byte Length

When a batch-only environment is established at generation time, the All Bound and Foreground PIBs are excluded from the table, and only one (BG) problem program PIB is built. However, the X'20' bytes that F2 and F1 PIBs normally occupy (between PIBBG and PIBAR) are filled with 32 bytes of DIBs data.

Note 2: Number is in multiples of 2K for F2 and F1. BG is always 10K (X' 0A').

Note 3: Total of nine subtask PIBs are generated, and only when AP is specified at generation time.

Bytes 90 and 91 (X'5A' – '5B') of the communications region contain the address of the first part of the PIB Table. Label PIBTAB identifies the first byte of the table.

Figure 15. First Part of Program Information Block (PIB) Table (See Figure 14 for Second Part)

^{*} See Figure 16 for flag byte expansions A, B, C, D, E and F.

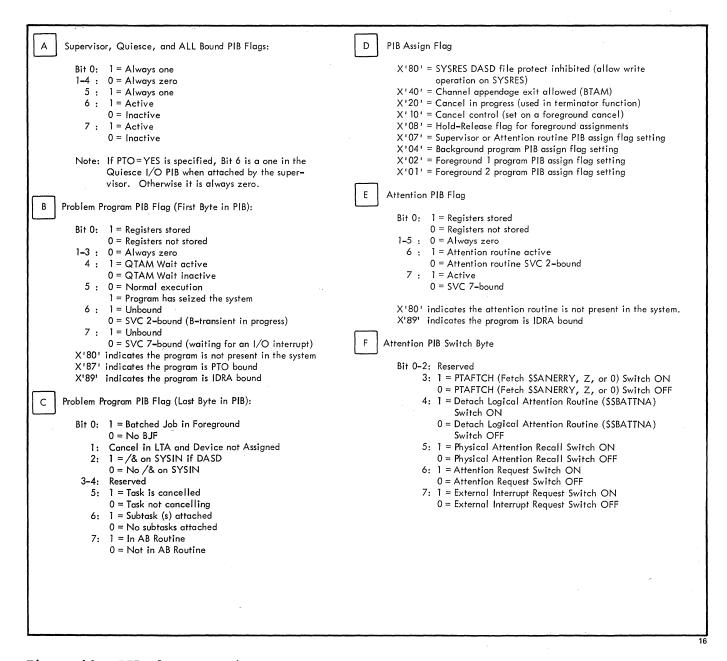


Figure 16. PIB Flag Expansions

FLPTR			CHAI	NQ			LUBID		REQID		LUBDSP		TKREQID
A		В		-c -			D		F	!	G		н
		Chain				1							
		Byte Chain							<u> </u>				
		Byte											
PUB		Chain											
Byte 2	T	Byte							ļ				
E	The length of the queue is	Chain Byte					1	1	ł				
	determined at supervisor gen –	Chain											
	eration time.	Byte Chain				 							-
		Byte	1								1		
		Chain											
		Byte				l	_						
		Chain Byte]		
L		Chain											
		Byte				<u></u> _							
	Byte	. 0	1	2	3								
	KEY												
	A Th	ne free list	t pointe	r contai	ns a di	isplaceme	ent index to	a free list o	entry wi	thin the cha	nnel que	ue.	
										nner as a de o more free			
		e availab		pointer (comun	is a nexu	decimal 11	, ii marcare	es mai n	o more free	1131 611111	es	
	B TH	ne first by	te of the	e channe	el que	Je entry (chain byte) contains a	pointer	(displaceme	nt index)	
	to	the next	channel	queue	entry f	or that d	evice. À h	exadecimal	FF indic	ates the las	t channel		
		ueue entry evice queu		t device	e. New	requests	on a giver	device are	queued	at the end	ot a give	n	
		CB addres:		snecifi	ed dev	ice							
	드			•						_			
								e identifyin :ement into		gical unit m LUB table.	aking the	•	
ı		•								for a specifi	a davisa		
		igure 18)		(urspiac	emem	muex) io	The this ci	idililei queu	ie emity	ioi a specifi	c device		
	F C	ontains a	code ide	entifying	a the p	roaram m	akina the l	/O request .	. The on	e– byte entr	v is calle	ed.	
	ه ت		estor Id	entifica						B belongs to			
	NI					,		2 1 52	0 51	2)			
								G = 1, F2 = where n =		3).			
		k = 1 for	superv	isor CC			hat bypass						
		k = 2 for $nk = FF$ for			hannel	queue er	ntries.						
			Ť.						.		L. S. L.		
	1 1	ontains X. artition LU					iss, or confo	ains the aisp	nacemei	nt index wit	iiin ine		
	Н С	ontains X'	'FF', or	the disp	olacem	ent into t	he PIB tabl	e for the PI	B of the	task request	ing I/O.		
										of the LUBIC			
										tables are i labels CH		ed	
		B, LUBDS					J		3		•		* •

Figure 17. CHANQ, LUBID, REQID, LUBDSP, and TKREQID Tables

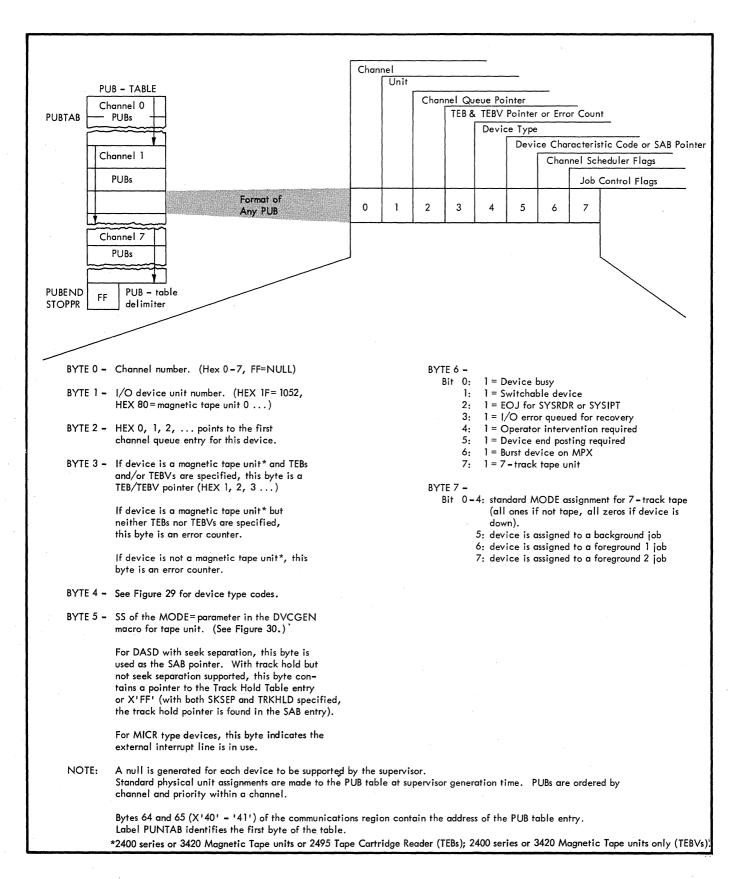


Figure 18. Physical Unit Block (PUB) Table

JIB Table	
JIB 1	
JIB 2	l
JIB 3	
JIB 4	ľ
JIB 5	
JIB 6	ı

Number (length of JIB table) determined at supervisor generation

Note: Two JIBs are required for a 2321 extent; one for lower limit and one for upper limit. The lower limit defining JIB must be chained to the upper limit defining JIB. Byte 1 of this type JIB contains the subcell number times 10 plus the strip number in binary.

0 1 2 3

Type of Entry

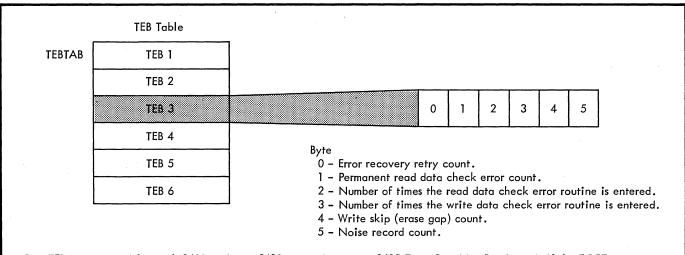
Stored standard assignment	LUB entry of stored standard assignment (PUB and JIB pointers)
Alternate assignment	PUB pointer of alternate X'00' assignment
1 2311 Extent	c _L c _L c _H c _H ②
1) 2321 Extent	or B _H B _H C _H C _H 3

Chain Byte.
Contains the displacement index of the next JIB.
A hexadecimal 'FF' defines the end of the chain.

- 1) Only when file-protect on DASD
- 2 Lower Cylinder Upper Cylinder
- (3) Cell or combined sub cell and strip

Bytes 68 - 69 (X'44' - '45') of the communications region contain the address of the JIB table entry. Label JIBTAB identifies the first byte of the table.

Figure 19. Job Information Block (JIB) Table



One TEB is generated for each 2400 series or 3420 magnetic tape or 2495 Tape Cartridge Reader unit if the FOPT macro contains the TEB = n parameter. Job control resets each TEB at normal or abnormal End-of-Job. An unused TEB contains HEX'FF0000000000'. A TEB is referenced from byte 3 of a magnetic tape unit PUB.

Bytes 70 and 71 (X'46'-'47') of the communications region contain the address of the TEB table entry. Label TEBTAB identifies the first byte of the table.

Figure 20. Tape Error Block (TEB) Table

Decimal Displace- ment		Byte Length	Description
(TEBV	Status Bloo	ck porti	on of TEBV Table, see <u>Note 1</u>)
0	TEBLEN	1	Length of TEBV Error Block (for each Error Block
1	TSBLEN	1	<pre>generated) Length of TEBV Status Block (4, 6, or 22 bytes, see Note 1)</pre>
2 3	EVARTH EVAWTH	1 1	EVA Read Error Threshold EVA Write Error Threshold
4	TEBSTAT	1 1	DASD ESTV File Status
5	TEBUDC	1	ESTVFLE Label Update Counter
•••		••••	
6	TEBDEV	1 1	Data Set Device Code
7	UPXTNT TEBRPT	1 1	Disk Address of Upper Extent of Data Set (cchh)
	NXTESR		Number of Records per Track Disk Address of Next Available Space for Data
1 12	NATESK		Record (cchhr)
17	ESTVLABL	5	Pointer to ESTVFLE Label in VTOC (cchhr)
!		•••	••• ••• ••• ••• •••
	Error Bloc	k portic	on of TEBV Table, see <u>Note 2</u>)
22	TEBV	1 1	Status Indicator (giving status of posting and writing error conditions)
23		1	<pre>Usage Indicator (X'00'=TEBV Error Block in use, X'FF'=Error Block generated but not serving any tape unit)</pre>
24		1 1	Retry Counter
25		1	Permanent Read Errors
26		1	Temporary Read Errors
27		1	Temporary Write Errors
28		1	Erase Gaps
29		1 1	Noise Blocks
30			Permanent Write Errors
31		1 1	Cleaner Actions
32			Number of Start I/Os
34		6	Volume Serial Number (volume ID)
	•••••	•••	••• ••• ••• ••• •••
40 (re	epeat bytes	22-39 f	or each TEBV Error Block)

Figure 21. TEBV Table Showing Status Block and Error Blocks (Part 1 of 2)

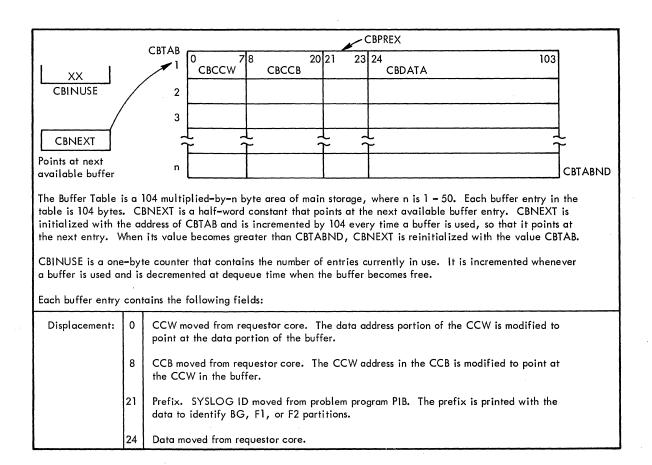
Note 1: The TEBV (Tape Error Block by Volume)
Table is composed of one Status Block and (n) Error
Blocks, and is addressed symbolically by label
TEBVTAB.

Supervisor generation options in the FOPT macro determine the size of the TEBV Status Block at generation time:

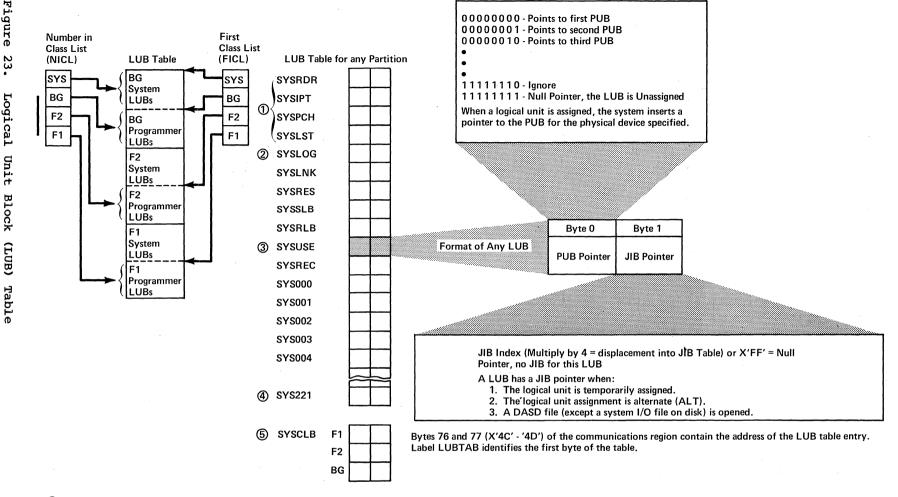
- When EVA is chosen without ESTV, the TEBV Status Block is four bytes long (bytes 0-3), followed by TEBV Error Blocks, so that bytes 4-21 are omitted.
- When ESTV output is to SYSLOG, the TEBV Status Block is six bytes long (bytes 0-5), followed by TEBV Error Blocks, so that bytes 6-21 are omitted.
- When ESTV output is to DASD, the TEBV Status Block is 22 bytes long (bytes 0-21, such as shown in this Figure), followed by TEBV Error Blocks.

Note 2: The number of TEBV Error Blocks generated corresponds to the (n) parameter of the FOPT macro for TEB, TEBV, or EVA options. A TEBV Error Block always contains 18 bytes, as shown in bytes 22-39 of this Figure. Therefore, the TEBV Table is composed of one TEBV Status Block (with its byte length dependent on supervisor generation options, as described in Note 1), followed by (n) number of 18-byte TEBV Error Blocks.

Figure 21. TEBV Table Showing Status Block and Error Blocks
(Part 2 of 2)



Console Buffering Table (CBTAB) and Work Areas Figure 22.



- When in Single Program Initiation mode (Foreground 1 or 2): Must be unit record device and can be referenced by the program.
- (2) When in Single Program Initiation mode (Foreground 1 or 2): Can be referenced by the program.
- 3 SYSUSE may be called SYSCTL in error recovery messages.
- The maximum number of programmer logical units in the system is 222 if MPS = BJF, or 244 if MPS = YES or NO.
- The SYSCLB (Private Core Image Library) LUB entry functions the same as other LUB entries, but is not part of the LUB Table. To locate the SYSCLB LUB in supervisor, perform the following steps:
 - 1. Divide the PIK by 8.
 - 2. Subtract the result in step 1 from the address of the PIB extension block.
 - 3. If option AP = YES, the result of step 2 is the location of SYSCLB LUB. If option AP = NO, add 16 (for the all-bound PIBX) to the result of step 2.

	X'FF' or Pointer	CCB Address	Address of Held Track (BBCCHH)	Key of Task	Flag and Counter
	Х	XXX	xxxxxx	Х	х
•	0	1	4	10	11

۲							
Byte	Explanation						
 0 	X'FF' or pointer to next available entry in the table. This is also placed in the PUB table, byte 5.						
1-3	Address of CCB associated with the task requesting the hold.						
4-9	Disk address of the track being held (in the form BBCCHH).						
10	Key of the task owning the track.						
11	Bit 0 on indicates a task is waiting for this track. 1-3 Unused 4-7 counter of number of holds on the track.						
l							

Figure 24. Track Hold (TKHDTAB) Table

Byte

Displacement	Label	Description
0-3	ACCTWK1* (ACCTABLE)*	Work area used in SIO update.
4 - 7	ACCTWK2	Work area used with ACCTWK1 in start/stop time routine
8-11	ACCTSVPT	Job card pointer; address of job card field following jobname.
12	ACCTPART	ID of partition in charge (partition switch name).
13	ACCTRES2	Reserved.
14 – 15	ACCTLEN	Length of SIO area = $6n + 1$, where n = number of devices for this partition in SYSGEN option JA = $(n1, n2, n3)$.
16-21	ACCTLOAD	Label area instruction; moves JAI label area address to OPEN/CLOSE transients.
22 - 23	ACCTRES3	Reserved.
24 – 27	ACCTLADD	Address of alternate label area.
28 – 31	ACCTCPUT	Counter for CPU time elapsed in a jobstep, counted in 300ths of a second.
32 - 35	ACCTOVHT	Counter for overhead time; time not charged to any partition.
36-39	ACCTBNDT	Counter for all – bound time; system wait state time divided between running partitions.
40 – 47	ACCTSVJN	Save area for job name during simulated EOJ.
		JOB ACCOUNTING TABLE (user's portion of Partition Table)
48 – 55	ACCTJBNM	Job name; taken from job card.
56 - 71	ACCTUSRS	User information; 16 bytes from Job card.
72 - 73	ACCTPTID	Partition ID; 'BG', 'F2', or 'F1' in EBCDIC format.
74	ACCTONOL	Cancel code; see Cancel Codes and Messages (Figure 32).
75	ACCTYPER	Type of record: 'S'=job step, 'L'=last step of job.
76 – 83	ACCTDATE	Date in format specified at SYSGEN (MM/DD/YY or DD/MM/YY).
84 – 87	ACCTSTRT	Start time of job, in packed decimal (OHHMMSSF; F=sign).
88 - 91	ACCTSTOP	Stop time of job, in same format as ACCTSTRT
92 – 95	ACCTRES	Reserved.
96-103	ACCTEXEC	Phase name; taken from execute card.
104 - 107	ACCTHICR	High core address of active program phase, from COMREG.
108 - 111	ACCTIMES	CPU time elapsed in a job step; counted in 300ths of a second.
112 - 115		Overhead time; elapsed time not charged to any partition, in 300ths of a second.
116-119		All-bound time; system wait state time divided between running partitions, in 300ths of a second.
120	ACCTSIOS	SIO tables: 6 bytes for each device specified by SYSGEN options, as follows: 2 bytes for device address (Ocuu), 4 bytes for count of SIOs in current jobstep.
		Overflow byte: normally X'20', but is X'30' if more devices are used within a partition than specified by SYSGEN options.
		ymbolically addresses the JAI Partition Tables with labels as shown. Each partition in which JAI is supported has a Table, labeled ACCTBG, ACCTF2, ACCTF1, for active partitions BG, F2, and F1 respectively.

Figure 25. Job Accounting Interface Partition Table (ACCTxx)

0	1	2	3	4			10) 11		17	18			24	25			31
SDR Flags (SDR – TABLE)	Parti- tion ID		Number of SDR Records		First SI BBCCH				First OBR ID BBCCHHR				rent OBR ID CHHR	a.		OBI Chh		·
SDR	ess of	35	36 Address SDR Un Switche	it	40 Re	served	43	44				List	Save Area					71
72		75	76		L		95	5 96	5 103	104		107	108	111	112	115	116	117
	1ask ytes			SDR1 V	Vork Are	ea			Test Under Mask Table		nporary rk Are		Test Unde Mask Instructio		F'65536	5'	SDR C	
118	S	DR2	2 Work Arec		135	136	Arec	э Мо	odified by A – Trans	ients:	155	1	5DR Error Message Save Area	Ві	163 ranch nstruction	F	BR/SI lag By Address	te
1 68	-					·						L						250
							Da	ta A	area for OBR/SDR R	lecords	i							
Key			nmunication	s Regio	n Displo	cement	S:											
0	SDR FI	ags	5:															
	Bi	1	: Key of O : RDE option	n					Bit 4: RF opt 5: RF opt 6: Error v	ion = \	Y E S							

2: Initial IPL time 6: Error while recording 7: Recorder file ready 3: RF option = NO, recording is suppressed Set and tested by Job Control. Set by EREP transient \$\$BSDRUP to identify the partition making the call for EREP recording. Settings: X'10' if EREP is running in BG. X'20' if EREP is running in F2. X'30' if EREP is running in F1. X'01' with one of the above if recorder file is ready. X'00' with one of the above if recorder file is not ready. Initial number of SDR records specified. If SDR record count is not specified, the file is formatted for OBR records only (\$JOBCTLM, see IPL and Job Control PLM, Y24-5086). Disk address of first SDR record. 11 Disk address of first OBR record. 18 Disk address of current OBR record. Disk address of last OBR record.

Figure 26. SDR Communications Region (SDRTABLE) (Part 1 of 2)

32 Address of SDR accumulator area which contains half - byte counters and accumulated error conditions. 36 Address of SDR unit switches. SDR switch byte (1 for each PUB): X'80' - Update operations complete X'40' - Counters on external file overflowed X'20' - I/O error during write X'08' - SDR update half - byte counters routine required X'04' - Update SDR record routine required Other - Reserved When entry contains X'01000000', indicates MCRR, no SDR supported. 40 Reserved. 44 SDR1 register save area. 72 Mask formats for interpretive error accumulator, SDR1: X'FF' - End of update X'FE' - Bypass counter X'FD' - Set up 'OR' condition to previous counter X'FC' - Ignore list item Other - Test bit in error queue 76 Used by the interpretive error accumulator routine to process list passed by OBR/SDR A-transient. 96 Used by the interpretive error accumulator routine. 104 Used by the interpretive error accumulator routine for address alignment. 108 Executed by the interpretive error accumulator routine. 112 Loop counter for the SDR counter update. 116 Save area for pointers to entries in the SDR error queue. 118 Work area where half byte error counters are unpacked and updated. 136 List of devices passed to the SDR processor from \$\$ANERAD. 156 Used by SDR/OBR recorder phases to pass error message displacements and disk error addresses in event of an error. 160 Entry point from OBR/SDR A - transients. Branches to label SDRMM. Pointer into the OBR/SDR unit switches. Status posted by recorder phases. (See byte 36). 168 OBR and SDR records formatted by the recorder phases.

Figure 26. SDR Communications Region (SDRTABLE) (Part 2 of 2)

ASCII to EBCDIC Correspondence (0/0 to 3/15)

		ASCII					EBCDIC		
Character	Col	Row	Bi		Col	Row		it	Comments
			Pat	tern	(in I	lex)	Pat	tern	
NUL	0	! 0	0000	0000	0	0	0000	0000	
SOH	0		0000	0001	0	1	0000	0001	
STX	0	2	0000	0010	0	2	0000	0010	
ETX	0	3	0000	0011	0	3	0000	0011	
EOT	0	4	0000	0100	3	7	0011	0111	
ENQ	0	5	0000	0101	2	D	0010	1101	
ACK	0	6 7	0000	0110	2	E	0010 0010	1110	
BEL BS	0	8	0000	0111 1000	2	6 F	0001	11111	
HT	0	9	0000	1000	1 0	5	0000	1 0100	
LF	0	10	0000	1 1010	2	5	0010	0101	
VT	0	1 11	0000	1011	0	I B	0000	1011	
FF	0	1 12	0000	1100	0	C	0000	1100	
CR	0	13	0000	1101	0	D	0000	1101	
SO	0	14	0000	1110	0	E	0000	1110	
SI	0	15	0000	1111	0	F	0000	1111	
DLE	1	0	0001	0000	1	0	0001	0000	
DC1	11		0001	0001	1	1	0001	0001	
DC2	1 1	2	0001	0010	1-!-	2	0001	0010	
DC3	 	3	0001	0011	1 1	3	0001	0011	
DC4	+ !-	4	0001	0100	3	C	0011	1 1100	
NAK		5	0001	0101	3	D	0011	1101	
SYN	 	1 6	0001	0110	3	2	0011	0010	
ETB CAN		7 8	0001	0111	2	6	0010 0001	1 1000	
EM	- - -	9	0001	1000	+	9	0001	1000	
SUB		10	0001	1010	3	F	0011	1111	
ESC	- 	1 11	0001	1011	2	7	0010	0111	
FS	l i	12	0001	1100	 	Ċ	0001	1100	
GS	1 1	13	0001	1101	-t-i-	l D	0001	1101	
RS	i	14	0001	1110	1 1	E	0001	1110	
US	1	15	0001	1111	1	F ,	0001	11111	
SP	2	0	0010	0000	4	0	0100	0000	
1	2	1	0010	0001	4	F	0100	1111	Logical OR
11	2	2	0010	0010	7	l F	0111	1111	
. #	2	3	0010	0011	7	В	0111	1011	
<u>\$</u>	2	4	0010	0100	5	В	0101	1011	
%	2	5	0010	0101	6	C	0110	1100	
<u>&</u>	2 2	6 7	0010	0110	5 7	0	0101 0111	0000	
	2	1 8	0010	1000	4	D D	0100	1101	
	$\frac{2}{2}$	9	0010	1000	5	t D	0100	1101	
*	2	10	0010	1010	5	C	0101	1100	1
+	2	1 11	0010	1011	4	E	0100	1110	
,	2	12	0010	1100	6	B	0110	1011	
_	2	13	0010	1101	6	0	0110	0000	Hyphen, Min
	2	14	0010	1110	4	В	0100	1011	
/	2	1 15	0010	1111	6		0110	0001	
0	3	0	0011	0000	F	0	1111	0000	1
1	3	1 1	0011	0001	F	1	1111	0001	
2	3	$\frac{2}{2}$	0011	0010	F	2	1111	0010	
3	3	3	0011	0011	F	3	1111	0011	
<u>4</u> 5	3 3	5	0011	0100	F	1 4	1111	0100 0101	
6	3	6	0011	0101	F F	<u>5</u>	1111	1 0101	
7	3	7	0011	0110	F	7	1111	1 0111	
8	3	8	0011	1000	F	8	1111	1 1000	
9	3	1 9	0011	1000	F	9	1111	1000	
:	3	10	0011	1010	7	Á	0111	1 1010	
;	3	11	0011	1 1011	5	E	0101	1 1110	
<	3	12	0011	1100	4	c	0100	1100	
=	3	13	0011	1101	7	E	0111	1110	
>	3	14	0011	1110	6	Е	0110	1110	
?	3	15	0011	1111	6	F	0110	1111	

Figure 27. ASCII Translation Tables (Part 1 of 4)

		ASCII					EBCDIC		1
Character	Col	Row		it	Col	Row		it	Comments
Character	001	1000	Pat	tern	(in l	Hex)	Pat	Pattern	
@	4	0	0100	0000	7	C	0111	1100	
Ā	4	. 1	0100	0001	С	1	1100	0001	
В .	4	2	0100	0010	С	2	1100	0010	
<u>C</u>	4	3	0100	0011	C	3	1100	0011	
<u>D</u>	4	4	0100	0100	C	4	1100	0100	<u> </u>
Ē	4	5	0100	0101	C C	5	1100	0101	
F G	4 4	6	0100 0100	0110 0111	C	l 6 l 7	1100 1100	0110	
Н	4	8	0100	1000	c	8	1100	1 1000	
1	4	9	0100	1001	1 c	9	1100	1 1001	·
j ·	4	10	0100	1010	D	1	1101	0001	
K	4	11	0100	1011	D	2	1101	0010	
L	4	12	0100	1100	D	3	1101	0011	
М	4	13	0100	1101	D	4	1101	0100	
N	4	14	0100	1110	D	5	1101	0101	
0	4	15	0100	1111	D	6	1101	0110	
P	5	0	0101	0000	D	7	1101	0111	
Q	5		0101	0001	<u> </u>	8	1101	1000	
R	5	2	0101	0010	D	9	1101	1001	
S	5	3	0101	0011 0100	E	2	1110	0010	
T U	5	5	0101 0101	0100	E	3 4	1110 1110	0011	
V	5	6	0101	0110	E E	1 5	1110	1 0100	
	5	7	0101	0110	E	6	1110	0110	
X	5	8	0101	1000	+ È	7	1110	0110	
Y	5	9	0101	1001	T E	8	1110	1000	
Ž	5	10	0101	1010	Ē	9	1110	1001	
Γ	5	11	0101	1011	4	A	0100	1010	
	5	12	0101	1100	E	0	1110	0000	Reverse Slar
]	5	13	0101	1101	5	A	0101	1010	
	5	14	0101	1110	5	F	0101	1111	Logical NO
	5	15	0101	1111	6	D	0110	1101	Underscore
	6	0	0110	0000	7	9	0111	1001	Grave Acce
a	6	1 1	0110	0001	8		1000	0001	
b	6	2	0110	0010	8	2	1000	0010	
c	6	3	0110	0011	8	3	1000	0011	
d	6	1 4	0110 0110	0100	8	4	1000	0100	
e f	6	5	0110	0101	8	5	1000	0101	
	6	7	0110	0110	8	° 7	1000	0110	
g h	6	8	0110	1000	8	1 8	1000	1000	
	6	9	0110	1000	8	9	1000	1 1000	1
i	6	10	0110	1010	9	1 1	1000	1 0001	
k	6	111	0110	1011	9	2	1001	0010	
	6	12	0110	1100	9	3	1001	0011	
m	6	13	0110	1101	9	4	1001	0100	
n	6	14	0110	1110	9	5	1001	0101	
0	6	15	0110	1111	9	6	1001	0110	
р	7	0	0111	0000	9	7	1001	0111	<u> </u>
q	7	<u> </u>	0111	0001	9	8	1001	1000	
r	7	2	0111 0111	0010	9	1 9	1001	1001	
<u> </u>	7	3	0111	0011	A	2	1010 1010	0010	+
U	7	5	0111	0100	A	4	1010	1 0100	
	7	6	0111	0110	. A	5	1010	0100	
w	7	7	0111	0111	T A	6	1010	0110	+
×	7	1 8	0111	1000	A	7 7	1010	1 0111	
У	7	9	0111	1001	A	8	1010	1000	
z	7	10	0111	1010	A	9	1010	1 1001	
{	7	11	0111	1011	c	0	1100	0000	
	7	12	0111	1100	6	A	0110	1010	Vertical Lin
}	7	13	0111	1101	D	0	1101	0000	
~	7	14	0111	1110	Α	1	1010	0001	Tilde
DEL	7	1 15	0111	1111	0	7	0000	0111	

Figure 27. ASCII Translation Tables (Part 2 of 4)

EBCDIC to ASCII Correspondence (X'00' to X'82')

EBCDIC TO THE PROPERTY OF THE						ASCII				
Character	Col	Row	B Pati	it ern	Col	Row	Bi Patt		Comments	
	(in h	Hex)				l				
NUL	. 0	0	0000	0000	0	1 0	0000	0000		
SOH	0	1	0000	0001	0	1	0000	0001		
STX	0	2	0000	0010	0	2	0000	0010		
ETX HT	0	5	0000	0011	0	3	0000	1001		
DEL	1 0	7	0000	0111	7	15	0111	1111	 	
VT	0	В	0000	1011	0	111	0000	1011		
FF	0	С	0000	1100	0	12	0000	1100		
CR	0	D	0000	1101	0	13	0000	1101		
SO	0	E	0000	1110	0	14	0000	1110		
SI	0	I F	0000	1111	0	15	0000 0001	1111 0000		
DLE DC1		0	0001	0000	 	1 1	0001	0000		
DC2	- - 	2	0001	0010	l i	2	0001	0010		
DC3	- 	3	0001	0011	 i	3	0001	0011		
BS	i	6	0001	0110	0	8	0000	1000		
CAN	1	8	0001	1000	1	8	0001	1000		
EM		9	0001	1001	1	9	0001	1001		
FS	1	C	0001	1100	1-!-	1 12	0001	1100		
GS	1-1-	D	0001	1101	1 1	13	0001	1101		
RS US	 	E F	0001	1110 1111	 	14	0001	1110 11111	- 	
LF	2	5	0010	0101	0	10	0000	1010		
ETB	2	6	0010	0110	 	1 7	0001	0111	<u> </u>	
ESC	2	7	0010	0111	 	11	0001	1011	<u> </u>	
ENQ	2	D	0010	1101	0	5	0000	0101		
ACK	2	E	0010	1110	0	6	0000	0110		
BEL	2	F	0010	1111	0	7	0000	0111		
SYN	3	2	0011	0010	1 1	6	0001	0110		
DC4	3 3	7 C	0011	0111	0	4 4	0000	0100 0100		
NAK	3	D	0011	1101	 	5	0001	0100		
SUB	3	1 F	0011	1111	l i	1 10	0001	1010		
SP	4	0	0100	0000	2	0	0010	0000		
[4	A	0100	1010	5	111	0101	1011		
- :	4	В	0100	1011	2	14	0010	1110		
<u> </u>	4	<u>C</u>	0100	1100	3	12	0011	1100		
	4 4	l D	0100 0100	1101	2 2	8 11	0010	1000		
-i	4	<u> I Б</u>	0100	1111	2	! ';	0010	0001	Logical OR	
&	5	. 0	0101	0000	2	6	0010	0110		
j	5	A	0101	1010	5	13	0101	1101		
\$	5	В	0101	1011	2	4	0010	0100		
*	5	С	0101	1100	2	10	0010	1010		
	5 5	<u>D</u>	0101	1101	2	9	0010	1001		
	5 5	E	0101 0101	1110 1111	5	11	0011 0101	1011 1110	Logical NO	
	6	1 0	0110	0000	2	1 13	0010	1110	Hyphen, Min	
	6	Ti	0110	0001	2	15	0010	1 1111	1.7511011, 7411	
	6	i A	0110	1010	7	12	0111	1100	Vertical Line	
	6	В	0110	1011	2	12	0010	1100		
%	6	C	0110	1100	2	5	0010	0101		
	6	D	0110	1101	5	15	0101	1111	Underscore	
?	6	F	0110 0110	1110 1111	3	14	0011	1110		
	7	1 9	0111	1001	6	0	0110	0000	Grave Accer	
•	7	i A	0111	1010	3	1 10	0011	1 1010	Oldve Accer	
#	7	1 B	0111	1011	2	3	0010	0011		
@	7	C	0111	1100	4	0	0100	0000		
1	7	D	0111	1101	2	7	0010	0111		
=	7	E	0111	1110	3	13	0011	1101		
	7	F	0111	1111	2	2	0010	0010		
a	8 8	1 2	1000	0001	6	1 2	0110 0110	0001		

Figure 27. ASCII Translation Tables (Part 3 of 4)

	EBC	DIC					ASCII		
Character	Col	Row Hex)		it tern	Col	Row		Bit ttern	Comments
	(in	l ex)		·	ļ			·	
С	8	3	1000	0011	6	3	0110	0011	
d	8	4	1000	0100	6	4	0110	0100	
e	8	5	1000	0101	6	5	0110	0101	
f	8	6	1000	0110	6	6	0110	0110	
g	8	7	1000	0111	6	7	0110	0111	
<u>h</u> i	8	8	1000 1000	1000	6	8 9	0110 0110	1000	
	9	1 1	1000	0001	6	10	0110	1 1010	
<u> </u> k	9	2	1001	0010	6	111	0110	1011	
	9	3	1001	0011	6	12	0110	1100	_
m	9	4	1001	0100	6	13	0110	1101	
n	9	5	1001	0101	6	14	0110	1110	
0	9	6	1001	0110	6	15	0110	1111	
р	9	7	1001	0111	7	0	0111	0000	
<u>q</u>	9	8	1001	1000	7	1	0111	0001	
r	9	9	1001	1001	7	2	0111	0010	<u> </u>
~	A	1	1010	0001	7	14	0111	1110	Tilde
<u>s</u>	A	2	1010	0010	7	3	0111	0011	_
t	A	3	1010 1010	0011 0100	7 7	5	0111 0111	0100	
V	A	5	1010	0100	7	6	0111	0110	-
	A	6	1010	0101	7	7	0111	0111	
×	A	7	1010	0111	7	8	0111	1 1000	+
у	A	8	1010	1000	7	9	0111	1 1001	
z	A	9	1010	1001	7	10	0111	1010	1
{	С	0	1100	0000	7	11	0111	1011	
Ä	С	1	1100	0001	4	1	0100	0001	
B	С	2	1100	0010	4	2	0100	0010	
C	С	3	1100	0011	4	3	0100	0011	
D	C	4	1100	0100	4	4	0100	0100	
E	C	5	1100	0101	4	5	0100	0101	
F	C	6	1100	0110	4	6	0100 0100	0110	
<u>G</u> H	C	7 8	1100 1100	1000	4	8	0100	1000	
	 c	9	. 1100	1000	4	9	0100	1000	
	 	1 0	1101	0000	7 7	13	0111	1 1101	
	D	1	1101	0001	4	10	0100	1 1010	
К	D	2	1101	0010	4	11	0100	1011	
L	D.	3	1101	0011	4	12	0100	1100	
М	D	4	1101	0100	4	13	0100	1101	
Ν	D	5	1101	0101	4	14	0100	1110	
0	D	1 6	1101	0110	4	15	0100	1111	
P	D	7	1101	0111	5	0	0101	0000	
Q R	D	8	1101 1101	1000	5	1 2	0101 0101	0001 0010	
	E	1 0	1110	0000		1 12	0101	1 1100	Reverse Sla
S	T E	2	1110	0010	5	3	0101	1 0011	We verse 310
<u></u>	Ē	3	1110	0011	5	4	0101	0100	
Ü	E	4	1110	0100	5	5	0101	1 0101	
V	E	5	1110	0101	5	6	0101	0110	
W ·	E	6	1110	0110	5	7	0101	0111	
X	E	7	1110	0111	5	8	0101	1000	
Y	E	8	1110	1000	5	9	0101	1001	
<u>Z</u>	- E	9	1110	1001	5	10	0101	1010	
0	F	0	1111	0000	3	1 0	0011	0000	
2	- F	1 2	1111	0001	3	1 2	0011	0001	
3	F F	3	1111	0010	3 3	1 3	0011	1 0010	
4	F	4	1111	0100	3	i 3 i 4	0011	1 0100	
5		1 5	1111	0100	3	5	0011	T 0100	+
6	F	6	1111	0110	3	6	0011	1 0110	
7	F	7	1111	0111	3	7	0011	0111	
. 8	 F	1 8	1111	1000	3	8	0011	1 1000	
9	F	9	1111	1001	3	9 .	0011	1001	

Figure 27. ASCII Translation Tables (Part 4 of 4)

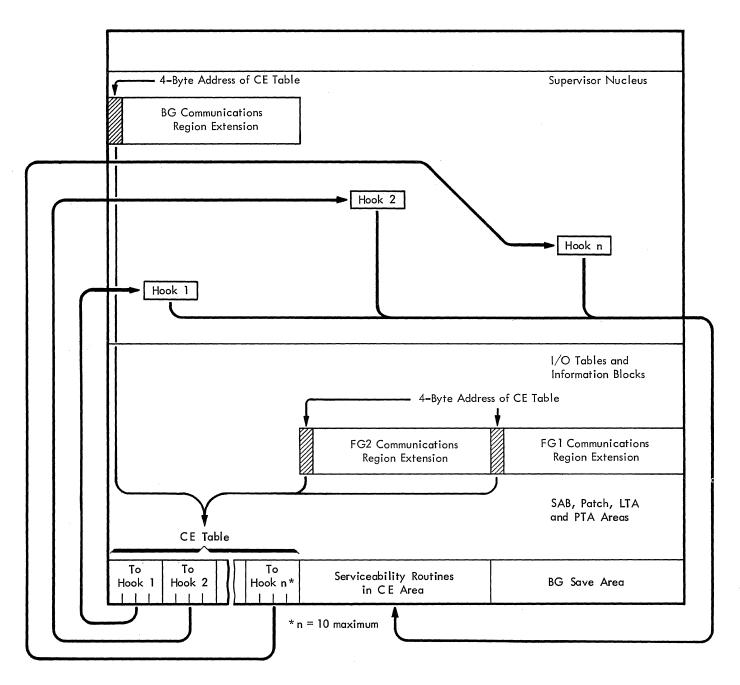


Figure 28. Accessing CE Serviceability and PDAID Routines

Card Code	Actual Device	Dev. Type X'nn'	Device Type
2400T9	9 – track 2400 Series Magnetic Tape Units 9 – track 3420 Magnetic Tape Units	50	Magnetic Tape Units
2400T7	7-track 2400 Series Magnetic Tape Units 7-track 3420 Magnetic Tape Units	-	Magnette rape offis
2495TC	2495 Tape Cartridge Reader	51	Tape Cartridge Reader
1442N1	1442N1 Card Read Punch	30	Card Readers – Punches
2520B1	2520B1 Card Read Punch	31	Cara Readers - Functies
2501	2501 Card Reader	10	Card Readers
2540R	2540 Card Reader	11	Cara Readers
2540P	2540 Card Punch	21	
2520B2	2520B2 Card Punch	20	Card Punches
1442N2	1442N2 Card Punch	22	Cara Punches
2520B3	2520B3 Card Punch	20	
1403	1403 Printer	40	
1403U	1403 Printer with UCS Feature	42	
3211	3211 Printer	43	
1404	1404 Printer	40	Printers
1443	1443 Printer	41	
1445	1445 Printer	41	1
1050A	1052, 3210, or 3215 Printer - Keyboard	00	1
UNSP	Unsupported Device	FF	Unsupported. No burst mode on multiplexor channel
UNSPB	Unsupported Device	FF	Unsupported with burst mode on multiplexor channel
2311	2311 Disk Storage Drive	60	Onsopported with borst mode of mornprexor channel
2314	2314 Direct Access Storage Facility		
2314	2319 Disk Storage Facility	62	DASD
2221		61	
2321	2321 Data Cell Drive	75	
1412**	1412 Magnetic Character Reader	//3	-
1419 ^ ^	1419 Magnetic Character Reader	- 70	·
	1255 Magnetic Character Reader	72	14160 14 .: 1 6 0
1419P**	1259 Magnetic Character Reader 1419 Dual Address Adapter Primary Control Unit	73	MICR - Magnetic Ink Character Recognition Devices and Optical Reader/Sorters
14195 **	1419 Dual Address Adapter Secondary Control Unit	74	
2701 *	2701 Data Adapter Unit	D0	
) A B	,	D1	Teleprocessing lines A = SADO command when enabling the line B = SAD1 command when enabling the line
2702 C C		DI	C = SAD2 command when enabling the line D = SAD3 command when enabling the line
2703	2703 Transmission Control	D2	
2955	2955 Data Adapter Unit	D7	Data link for RETAIN/370
2671	2671 Paper Tape Reader	70	Paper Tape Reader
1285	1285 Optical Reader	76	
1287	1287 Optical Reader	77	Optical Readers
1288	1288 Optical Page Reader	//	
1017	1017 Paper Tape Reader with 2826	78	Panar Tana Pandar
1017	Control Unit Model 1	/0	Paper Tape Reader
1018	1018 Paper Tape Punch with 2826 Control Unit Model 1	79	Paper Tape Punch
2260	2260 or 2265 Display Station	C0	Display Station
7770	7770 Audio Response Unit	D3	
7772	7772 Audio Response Unit	D4	Audio Response Units
101 <i>7</i> TP	1017 Paper Tape Reader with 2826 Control Unit Model 2	D5	Paper Tape Reader
1018TP	1018 Paper Tape Punch with 2826 Control Unit Model 2	D6	Poper Tape Punch

Note: The codes used in the DVCGEN macros are the same codes used in IPL statements.

Figure 29. Device Type Codes

 $^{^{*}}$ For other teleprocessing devices, see IBM System/360, DOS BTAM and QTAM PLMs, GY30 - 5001 and GY30 - 5002.

^{**} This device type code is also used for the 1270/1275 optical reader/sorters.

Density (Bytes per inch)	Parity	Convert Feature	Translate	SS Code*
200 200 200 200 200 200	odd odd odd even even	on off off off off	off off on off on	10 30 38 20 28
556 556 556 556 556	odd odd odd even even	on off off off off	off off on off on	50 70 78 60 68
800 800 800 800 800 800 1600		on off off off off density nine- density nine-		90 B0 B8 A0 A8 C8

Figure 30. Density Data

The supervisor is the storage resident portion of the Disk Operating System. It is loaded into storage at IPL time and remains there throughout system operations. Refer to the preceding section of this manual for information about generation of the resident supervisor. Refer to Figure 2 for information about the storage organization of the resident supervisor.

Infrequently-used supervisory functions are not included in the resident supervisor. They are in the form of transient programs (A and B) and are fetched or loaded from the core image library when needed.

BATCH JOB SUPPORT

Batch jobs may be run in any of the three partitions (BG, F2, F1). Batch job support is always provided in the background partition. To run in the foreground partitions, the MPS=BJF option must be specified.

MULTIPROGRAMMING SUPPORT (MPS)

General Entry and General Exit routines provide the mechanism for multiprogramming support. Refer to these areas on Chart 01 for additional descriptions for multiprogramming concepts. Figure 31 illustrates the task selection procedure associated with multiprogramming.

SUPERVISOR INTERRUPT PROCESSORS

This portion of the resident supervisor processes the following system interrupts:

- I/O interrupt.
- Program check interrupt.
- External interrupt.
- Machine check interrupt.
- Supervisor call interrupt.

	Priority Table	
Sample Status	PIB Tables	MVCFLD
X'84'	Supervisor task PIB	X'60'
X'84'	Quiesce I/O task PIB	X'50'
X'80'	Attention task PIB	X'40'
X'83'	† Foreground 1 program PIB	X,30,
X'82'	† Foreground 2 program PIB	X'20'
X'83'	Background program PIB	X'10'
X'85'	†All bound PIB	X'00'

 Test status flags in order specified by priority table.

2. Select 1st PIB for which the TRT function is not X'00'.

٠,				
	PIB Flags During Task Selection		Table of Selection Criteria	
	Meaning of Status	Flag	Label	TRT Function
	Detached	X'80'	TRTMSK	X'00'
	Waiting for B - transient area	X'81'	TRTLTK	X'00' or X'03' (Note 1)
	Waiting for CCB or TECB	X'82'		X,00,
	Ready to run	X'83'	TRTRUN	X'03' or X'00' (Note 2)
	Inactive SUPVR or Quiesce I/O	X'84'		X'00'
	Active SUPVR, Quiesce I/O, or All bound	X'85'		X'05'

Note 1: X'00' when the B-transient area is in use as indicated by the Logical Transient Key (LTK).

Note 2: X'00' when a task has seized the system. That task's status flag will equal X'84' or X'85'.

.† These PIBs are generated for MPS option only.

Figure 31. Task Selection Procedure

I/O INTERRUPT

Microprogramming detects an I/O interrupt and loads the I/O new PSW. Refer to the I/O Interrupt Processor on Chart 04.

PROGRAM CHECK INTERRUPT

Microprogramming detects a program check interrupt and loads the program check new PSW. Refer to Program Check Interrupt Processor on Chart 02.

EXTERNAL INTERRUPT

Microprogramming detects an external interrupt and loads the external new PSW. External interrupts can be caused by:

- Timer
- External interrupt key
- Signal

Refer to External Interrupt Processor on Chart 05.

MACHINE CHECK INTERRUPT

Microprogramming detects a machine check interrupt and loads the machine check new PSW. In a system without MCRR option, the SEREP action code (S) is stored in storage location 0001, and the system enters the wait state. If MCRR is present, system recovery is attempted. Refer to Chart 07.

SUPERVISOR CALL INTERRUPT (SVC)

SVC is detected by microprogramming, which loads the SVC new PSW. The SVC interrupt processor (Chart 03) analyzes the SVC code placed in the SVC old PSW by the calling program. Control is transferred to the appropriate processing routine. Some SVCs are optional and cause a cancel if the supervisor was generated without the option. (See Figure 33 for a list of supervisor calls.)

SVC 0: Execute the channel program (EXCP). The address of the user's command control block (CCB) must be supplied in general register 1 before this SVC is issued. Return may be either to the interrupted program or to the highest priority program ready to run.

Note: When an SVC 0 is issued by supervisor or A-Transient programs, the address of the CCB must be supplied in general register 15 before the SVC is issued.

SVC 1: Fetches a phase. A fetch loads a phase from the system core image library or a private core image library (see Note) and branches to the entry address in that phase. The load and entry addresses are obtained from the respective core image directory entry for the phase being fetched. The storage address of the phase name must be supplied in general register 1 before this SVC is issued. The user may override the linkage editor entry address

by supplying an entry address in general register 0. Return may be either to the interrupted program or to the highest priority program ready to run.

Note: If a PCIL (Private Core Image Library) is assigned, it is searched first for the proper phase. If the phase is not found, the system core image library is then searched. When the first character of the phase name is \$, the system core image library is searched first and the private core image library last.

SVC 2: Fetches a B-transient. Loads a B-transient program (phase name prefix equals \$\$B) from the system core image library, or a private core image library (see SVC 1 Note), to the B-transient area (refer to Figure 2), and enters the B-transient at its load address plus 8 bytes. The storage address of the B-transient phase name must be supplied in general register 1.

An address in general register 0 is ignored. The B-transient is loaded at the beginning address of the B-transient area. General register 15 is loaded with this address and may be used by B-transients as a base register. Return may be either to the interrupted program or to the highest priority program ready to run.

Only one program can use the B-transient area at a time. If the B-transient program is SVC 7 bound, another program is selected. This program becomes SVC 2 bound (waiting for the B-transient area) if it issues an SVC 2. Another program is then selected.

Note: Supervisor may branch directly to the SVC 2 routine when fetching a B-transient. If the transient is not in the library when referenced by the supervisor, the system enters the wait state.

SVC 3: Fetches or returns from an A-transient. Load an A-transient program (phase name prefix equals \$\$A) from the system core image library, or a private core image library (see SVC 1 Note), to the A-transient area (refer to Figure 2), and enters the A-transient at its load address plus 8 bytes. The storage address of the A-transient phase name is loaded in general register 1 before the fetch is made.

An address in general register 0 is ignored. The A-transient is loaded at the beginning address of the A-transient area. General register 11 is loaded with this address and is used by A-transients as a base register. Return is to the interrupted program.

Note: Supervisor may branch directly to the SVC 3 routine when fetching an A-transient. Only programs operating in the supervisor mode can issue an SVC 3. If the transient is not in the library, the system enters the wait state.

<u>Caution</u>: SVC 3 is also used as a return from an A-transient program. The last byte of the A-transient name field determines the usage.

- X'00' Returning from error recovery A-transients.
- X'01' Returning from physical attention transients (\$\$ANERRZ, Y, 0) or post cancel by any A-transient.
- Alphameric Fetch A-transient.

When returning from an A-transient, the branch address is in general register 15. The A-transient must load one of the exit addresses from the error recovery block (ERBLOC). Refer to Figure 43.

SVC 4: Loads a phase from the system core image library, or a private core image library (see SVC 1 Note), and returns to the user. (See the following Note.) The storage address of the phase name must be supplied in general register 1 before this SVC is issued. The user may override the link-edited load address by supplying a load address in general register 0. Upon return to the user, general register 1 contains the phase entry address adjusted for any changes in the phase's load address.

Note: Return may be either to the interrupted program or to the highest priority program ready to run.

SVC 5: Modifies the supervisor communications region. Supplies the supervisory support for the MVCOM macro. The sequence of events is:

- 1. MVCOM macro issues an SVC 5.
- SVC 5 fetches \$\$ANERR1 by branching to the SVC 3 routine.
- \$\$ANERR1 alters the supervisor communications region as specified by the MVCOM macro.

Return may be either to the interrupted program or to the highest priority program ready to run.

<u>SVC 6</u>: Cancels a program (task) or partition. If either a subtask or maintask (or only program in the partition) issues a CANCEL, cancel code X'23' is posted to the PIB for the task issuing the cancel. If a

maintask issues a CANCEL while subtasks are attached, cancel code X'17' is posted in the maintask PIB. If a CANCEL ALL is issued, cancel code X'1C' is posted. Cancel code X'23' does not cause a system dump even if the dump option has been specified.

A simple cancel issued by a subtask performs the same function as DETACH (see SVC 39), but also posts the ECB's byte 2, bits 0 and 1, and issues a subtask cancellation message. When CANCEL is issued by a maintask, the partition is canceled.

A CANCEL ALL macro issued by a subtask cancels the entire partition. In this case, the AB exits for all tasks that have them are taken, except for the subtask issuing the CANCEL ALL. (Refer to Figures 14-16 for the format of the PIB table, to Chart 03 for General Cancel Routine, and to Figure 36 for cancel codes.) The next time the canceled program is selected on general exit, the supervisor branches to the SVC 2 routine to fetch the cancel B-transient program \$\$BEOJ3 if teleprocessing is supported, or \$\$BEOJ4 if teleprocessing is not supported.

<u>SVC 7</u>: Waits for I/O to complete or a timer interrupt to occur. SVC 7 supplies the supervisory support for the WAIT macro.

With MPS option, returns directly to the interrupted program if the traffic bit has been posted in the CCB or TECB. See SVC 24 in this list for an explanation of the TECB. If traffic bit is not posted:

- Change the status of the interrupted program PIB to SVC 7 bound (not ready to run).
- Select the highest priority program that <u>is</u> ready to run.

When I/O is completed or a timer interrupt occurs:

- The traffic bit is posted in the CCB or TECB.
- 2. The PIB is restored to the ready-to-run status.
- When this program is again selected at general exit, the old PSW is loaded with the address of the second instruction of the WAIT macro expansion.

Without MPS option, returns directly to the interrupted program if the traffic bit has been posted in the CCB or TECB. (See SVC 24 in this list for an explanation of the TECB.) If the traffic bit is not

posted, the system enters the wait state with interrupts enabled.

SVC 8: Supplies the supervisory support to temporarily return from a B-transient program to the problem program. The B-transient area is not released. The task selection exit loads the problem program registers. An SVC 9 is used to return to the B-transient program.

SVC 9: Supplies the supervisory support for returning to the B-transient after an SVC 8 is issued. The task selection exit loads the B-transient registers.

SVC 10: Sets a timer interval. This SVC is optional, and the issuing program is canceled if supervisor is generated without the IT option. Only the timer supported program can issue an SVC 10. Others are canceled.

The time interval is specified in general register 1 by the user (SETIME macro). The system time of day (SYSTOD, X'54') is updated to the time that the next interrupt should occur (may change if another SVC 10 is issued). The system timer (SYSTIMER, X'50') is set to the specified time interval. The time interval in SYSTIMER immediately begins to lapse. Refer to IBM System/360 Principles of Operation, GA22-6821, for information concerning the operation of SYSTIMER.

Current system time of day can be obtained by shifting out the low order byte from the remaining time interval (SYSTIMER) and subtracting it from system time of day (SYSTOD). Time in SYSTOD is represented in the form, seconds x 300. Time in SYSTIMER is in the form, seconds $x 300 \times 256$.

An SVC 10 returns directly to the timer supported program. No task selection is performed.

SVC 11: Returns from a B-transient releasing the B-transient area. SVC 11 is invalid if issued by other than a B-transient. The logical transient area is released for use by other programs or tasks. Return is to the highest priority program ready to run.

SVC 12: Supplies the supervisory support to reset flags to 0 in the linkage control byte (displacement 57 in the supervisor communications region). The user loads the address of a mask (1 byte, hexadecimal) into general register 1. This mask is ANDed with the linkage control byte. An SVC 12 returns directly to the interrupted program. No task selection is performed.

SVC 13: Supplies the supervisory support to set flags to 1 in the linkage control byte (displacement 57 in the supervisor communications region). The user loads the address of a mask (1 byte, hexadecimal) into general register 1. This mask is ORed with the linkage control byte. An SVC 13 returns directly to the interrupted program. No task selection is performed.

This is the normal end of job (EOJ). Cancel code X'10' is posted to the PIB for the program issuing the SVC 14. Refer to Figures 14-16 for the format of the PIB tables and to Chart 03 for the General Cancel routine. The next time the canceled program is selected on general exit, a branch is made to the SVC 2 routine to fetch the cancel B-transient program \$\$BEOJ3 if teleprocessing is supported, or \$\$BEOJ4 if teleprocessing is not supported. Job control is loaded by \$\$BEOJ to perform the end-of-job-step.

SVC 15: This is the same as SVC 0 (EXCP), with this exception: when the CHANQ table is full, the SVC is ignored. Return is directly to the interrupted program in this case. If the CHANQ table is not full, general register 0 is zeroed and EXCP is issued (see \underline{SVC} 0 in this list).

The CHANQ table is full when the free list pointer (FLPTR) equals X'FF'. Refer to Figure 17 for the format of the CHANQ table and to Figure 32 for CHANQ operation.

SVCs 16 through 21 and SVC 37: These supervisor calls provide supervisory support for the STXIT and EXIT macros. They are optional, and the issuing program is canceled if supervisor was not generated with the applicable option.

- SVC 16 stores the address of the user's program check (PC) routine and save area address in the PC option table.
- SVC 17 provides a return from the user's PC routine to the program interrupted due to a program check.
- SVC 18 stores the address of the user's interval timer (IT) routine and save area address in the IT option table. Only the timer supported program can issue SVC 18. If multitasking, only the maintask can process the interruption.
- SVC 19 provides a return from the user's IT routine to the timer supported program. Only the timer supported program can issue SVC 19.
- SVC 20 stores the address of the user's operator communications (OC) routine

and save area address in the OC option table. If multitasking, only the maintask can process the interruption.

 SVC 21 provides a return from the user's OC routine to the program interrupted by the external interrupt key.

The address of the user routine is specified in general register 0, and the address of the user's save area is specified in general register 1 in all cases. Refer to Figure 13 for the format of the option tables.

SVCs 16, 18, and 20 return directly to the interrupted program. SVCs 17, 19, and 21 return either to the interrupted program or to the highest priority program ready to run.

SVC 22: Seizes the system and provides a release from such a seizure. The SVC 22 is ignored if supervisor was generated without the MPS option. The program issuing an SVC 22 is canceled if the PSW protection key field does not equal 0. (Only job control and B-transient programs can issue an SVC 22.)

The first SVC 22 issued seizes the system and the next one issued releases the system. The last byte of register 0 replaces the system mask. If register 0 is negative, the protection key is replaced by the protection key of the PIK.

The task selection mechanism is altered by the first SVC 22 so that only supervisor or quiesce I/O tasks and the program that issued the SVC 22 can be selected. The next SVC 22 issued restores the task selection mechanism. The contents of the last byte of general register 0 are again used as the system mask.

Return from each SVC 22 is directly to the interrupted program.

Note:

- There is no way to cancel a program that has seized the system.
- The program must have no pending I/O operations.
- The program cannot issue supervisor calls while the system is seized.

SVC 23: Loads phase header. Retrieves the load address for a specified phase from the system core image directory or a private core image directory. The program issuing an SVC 23 is canceled if supervisor was generated without the MPS option or if the PSW protection key does not equal 0. (Only

job control and B-transient programs can issue an SVC 23.)

The user must specify the address of the core image phase name in general register 1 and the address where the load address is to be stored in general register 0. The main fetch subroutine scans the core image directory and retrieves the load address. If the phase is found in the directory, the load address (3 bytes) is stored at the address specified by general register 0. If the phase is not found, the supervisor returns control to the interrupted program.

SVC 24: Stores the address of the user's timer event control block (TECB) and sets a timer interval. This SVC is optional, and the issuing program is canceled if supervisor is generated without IT option. Only the timer supported program can issue an SVC 24. Others are canceled.

The address of the user's TECB is specified in general register 0, and the time interval is specified in general register 1.

The traffic bit is reset in the TECB, and the TECB address is stored in the IT option table. Refer to Figure 13 for the format of the IT option table.

<u>Note</u>: The TECB has the same format as a command control block (CCB), but only the traffic bit is used. The traffic bit is set when a timer interrupt occurs. Refer to Figure 37 for the format of the CCB.

The time interval is set, and the system time of day is updated as for an SVC 10. (See SVC 10.) An SVC 24 returns directly to the timer supported program. No task selection is performed.

The user causes the program to wait for the timer interrupt to occur by issuing an SVC 7. (See SVC 7 in this list.)

SVC25: Halts I/O on a teleprocessing device, or halts I/O on any device if issued by OLTEP. If the supervisor is generated without teleprocessing and without OLTEP, any issuing program is canceled.

The address of any command control block (CCB) containing the symbolic address of the device to be halted must be supplied in register 1 before issuing the SVC 25. If the SVC 25 is used by a program other then OLTEP, an HIO instruction is issued to the device if:

- 1. It is a teleprocessing device, and
- An I/O interrupt is pending for the device.

If OLTEP is the issuing program, an HIO instruction is issued to the device if there is I/O pending for the device. That is the only restriction on OLTEP's use of SVC 25.

The supervisor returns to the highest priority program ready to run. The device busy flag is reset at this time. Unless SVC 25 is issued by OLTEP or a teleprocessing device, this SVC is ignored and results in cancelation. If OLTEP was a supervisor option and teleprocessing was not, issuing as SVC 25 by a program other than OLTEP results in cancelation.

SVC 26: Validate address limits. The program issuing an SVC 26 is canceled if the PSW protection key does not equal 0. (Only job control and B-transient programs can issue an SVC 26.)

The upper address must be specified in general register 2, and the lower address must be specified in general register 1. The upper address must be within main storage, and the lower address must be higher than the end of supervisor address, or the program is canceled (ERR25). Return is to the interrupted program. No task selection is performed.

With MPS option, the PIK of the program issuing the SVC 26 must equal the storage protection key for both addresses or the program is canceled (ERR25).

With batch operation, SVC 26 is ignored unless storage protection has been specified.

SVC 27: Same as SVC 25, except that SVC 27 cannot be used by OLTEP. It can be used only to halt I/O on a teleprocessing device. The CCB is not dequeued if the CSW has been stored after an HIO command.

SVC 28: Provides return from user's stacker select routine to the MICR external interrupt routine in the supervisor. This SVC is optional and causes a cancel if issued at any point other than in a stacker select routine with MICR devices.

SVC 29: Provides supervisory support for the WAITM macro (except for MICR type devices). If WAITM=YES has been specified in the FOPT macro, WAITM coding is generated to load general register 1 with the address of the ECB list name and to issue the SVC 29. However, when MICR type devices are used, SVC 47 is issued to identify the wait on the MICR CCB.

All interrupts are disabled and the CCBs are all checked for the traffic bit. When a CCB is found with the traffic bit posted, SVC 29 returns to the interrupted program.

If all CCBs are checked and no traffic bits are posted, one of two courses is taken:

- With MPs option Cause user to become I/O-bound, disable for I/O interrupts only, and return to task selection.
- Without MPS option Set wait bit in SVC old PSW, disable for I/O interrupts only, and return to interrupted program.

SVCs 30, 31, and 32: Reserved for QTAM. Refer to the QTAM PLM listed in the Preface.

SVCs 33 and 34: Reserved for internal macros COMRG and GETIME, respectively. Their use by other programs results in a branch to EXT01 (see Chart BG).

SVC 35: Protects a track from use by more than one task at a time. A X'FF' is moved to byte 2 of the SVC old PSW to indicate track hold. A requesting task not owning a held track is made inactive and must wait until the track is free. If more than sixteen holds on a track are attempted, the requesting task is canceled.

Exits are to EXCP3 to execute the I/O, or to RESVC if the track is already held. At RESVC, the problem program old PSW is set to execute the SVC 35 again, and a branch to EXT03 is taken for task selection. See Figure 24 for the Track Hold Table.

 $\underline{\mathtt{SVC}\ 36} \colon$ Frees a track that is held by the task issuing the FREE. An attempt to free a track not owned by the requestor results in cancellation of that task.

Exits on a successful FREE are to EXT03 for task selection, or to the DETACH routine if the FREE was issued by that routine.

SVC 37: Establishes linkage from the supervisor to a problem program abnormal termination (AB) routine. It stores the routine's entry point and save area address in the AB table. (The save area is a 72-byte area in which the old PSW and general registers 0-15 are stored.) Return is to the STXITing program.

SVC 38: Initializes a subtask. task's PIB and save area are copied to the subtask's PIB and save area. The subtask's PIB flag is set to X'83' to indicate 'ready-to-run.' Bit 0 of the maintask's R1 is set to 0 to indicate a successful attach, and absolute priority is established for the subtask. A subtask attempting to issue an ATTACH is canceled. Exit is to EXT03 for task selection.

SVC 39: Performs normal termination of a subtask. DETACH may be issued by either the subtask being terminated or by the main task.

The subtask's PIB is set inactive (byte 0 = X'80'), and its ECB (see Figure 34) is posted for termination. This routine calls the free routine to free any tracks held by this subtask, and a waiting task is removed from the wait state. Exit is to EXT03 for task selection.

SVC 40: Used for intertask communication. POST may be issued by either a maintask or a subtask. It is issued so that a task is aware of the termination of an event. Normal completion of the specified event is posted in the ECB (byte 2, bit 0 = 1). If the SAVE= parameter is present, only the "task waiting for this ECB is taken out of the wait state; otherwise, all waiting tasks are removed from the wait state. Exit from this routine is to EXT03 for task selection.

SVC 41: Informs the system that a resource (shared data area) is now available for use by another task. A task may issue the DEQ macro only to a resource that it currently owns. If it attempts to issue the DEQ macro to some other resource, the task is canceled.

If any other tasks are waiting for the resource, the highest priority task ready to run is removed from the wait state and gains control. If no other task is waiting for the resource, control returns to the task that issued the DEQ.

If a task terminates without DEQuing all of its ENQued resources, either in its normal coding or in its abnormal termination exit routine, any task subsequently attempting to ENQ the resource is canceled. See Figure 35 for the Resource Control Block (RCB).

Normal exits are to EXT01 or EXT03.

SVC 42: ENQ prevents tasks from simultaneous manipulation of a shared data area (resource). This is accomplished, using the TS instruction, by setting to ones all bits of byte 0 of the specified resource control block (RCB). Then the event control block (ECB) address is placed in bytes 4-7 of the RCB.

A task attempting to ENQ a resource that is already engueued by another task is placed in a queue and put in a waiting condition. The old PSW is set to reexecute the SVC 42 and task selection is performed.

A task is canceled if it attempts to nest ENQ(s) of a resource or if it attempts to ENQ a resource that is still owned by a terminated task.

When a task is finished with a resource, it should inform the system by issuing the DEQ macro. If it does not, tasks subsequently requesting that resource are canceled. See Figure 35 for the Resource Control Block.

SVC 43: Supplies supervisory support for the creation and updating of SDR records for devices not explicitly supported by the system. The address of the compressed SDR record area must be supplied in general register 1 before the SVC is issued. The SDR record area must be 22 bytes long: bytes reserved for the SDR processor, 1 byte initialized to zeroes, and a 19 byte SDR record with the 16 error counters compacted to 8 bytes. The SVC 43 causes a branch to the SDRSDR routine in the supervisor to complete processing of the record. Immediately following the SVC, the WAIT macro must be issued on the address in register 1.

Example:

LA 1,SDRAREA SVC 43 WAIT (1) or SDRAREA

This SVC is available only with the I/O Error Logging option (ERRLOG). See Chart 08 for the SDRSDR update routine.

SVC 44: Supplies supervisory support for external creation of OBR records for devices not explicitly supported by the system. The address of the OBR record area must be supplied in general register 1 before the SVC is issued. The OBR record area must be 83 bytes long: 2 bytes reserved for the OBR processor, 1 byte initialized to zeroes, and an 80 byte OBR record. The SVC 44 causes a branch to the SDROBR routine in the supervisor to write the OBR record. Immediately following the SVC, the WAIT macro must be issued on the address in register 1.

Example:

LA 1,0BRAREA SVC 44 WAIT (1) or OBRAREA

This SVC is available only with the I/O Error Logging option (ERRLOG). See Chart 08 for the SDROBR update routine.

SVC 45: Provides emulator interface for CPU Models 30 and 40, or System/370 models. On System/370, this SVC serves two purposes:

- When register 1 contains zero, SVC 45 sets communication region byte 134 to X'40', indicating that the emulator is active.
- When register 1 contains a PUB address, SVC 45 switches the parity bit in the PUB.

SVC 46: Provides OLTEP with the facility to operate in the supervisory state. In the initial issuing of the SVC, register 1 contains an entry point in OLTEP. The next time the SVC is issued, register 1 is zeroed out, forcing task selection.

SVC 47: Provides identification to the supervisor for MICR type device waits. The SVC results in exiting to task selection (EXT03) rather than reissuing the SVC (RESVC) as is done when SVC 29 is issued.

SVC 48: Reserved for future use.

SVC 49: Reserved for future use.

SVC 50: Reserved for LIOCS error recovery.

SVC 51: Provides OLTEP with the ability to find the length of a core image library without loading the phase. Registers 0 and 1 must be initialized before issuing

SVC 51. Register 0 must be pointed at a twelve-byte save area for the phase header, and register 1 must be pointed at the eight-byte phase name. The first 12 bytes of the phase header are moved to the save area. The save area is not altered if the phase is not in the core image library. If any program except OLTEP issues an SVC 51, that program is canceled.

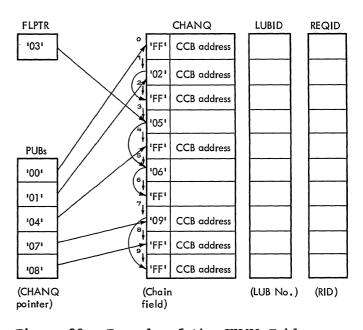


Figure 32. Example of the CHANQ Table Operation

Admin C	SV	/C	Function
Macro Supported Dec.		Hex.	FUNCTION
EXCP	0	0	Execute channel programs.
FETCH	1 2 3	1 2 3	Fetch any phase. Fetch a logical transient (B – transient). Fetch or return from a physical transient (A – transient).
LOAD	4	4	Load any phase.
MVCOM	5	5	Modify supervisor communications region.
CANCEL	6	6	Cancel a problem program or task.
WAIT	7	7	Wait for a CCB or TECB.
	8	8	Transfer control to the problem program from a logical transient (B – transient).
LBR ET	9	9	Return to a logical transient (B – transient) from the problem program after an SVC 8 .
SETIME	10*	А	Set timer interval.
	11 12	B C	Return from a logical transient (B – transient). Logical AND (Reset) to second job control byte (displacement 57 in communications region).
	13	D	Logical OR (Set) to second job control byte (displacement 57 in communications region).
EOJ	14	E	Cancel job and go to job control for end of job step.
	15	F	Same as SVC 0 except ignored if CHANQ table is full. (Primarily used by ERP).
STXIT (PC)	16*	10	Provide supervisor with linkage to user's PC routine for program check interrupts.
EXIT (PC)	17*	11	Return from user's PC routine.
STXIT (IT)	18*	12	Provide supervisor with linkage to user's IT routine for interval timer interrupts.
EXIT (IT)	19*	13	Return from user's IT routine.
STXIT (OC)	20*	14	Provide supervisor with linkage to user's OC routine for external or attention interrupts (operator communications).
EXIT (OC)	21*	15	Return from user's OC routine.
	22*	16	The first SVC 22 seizes the system for the issuing program by disabling multi- program operation. The second SVC 22 releases the system (enables multiprogram
	23*	17	operation). Load phase header. Phase load address is stored at user's address.
SETIME	24*	18	Provide supervisor with linkage to user's TECB and set timer interval.
	25*	19	Issue HALT I/O on a teleprocessing device, or HALT I/O on any device if issued by OLTEP.
	26* 27*	1A 1B	Validate address limits. Special HIO on teleprocessing devices.

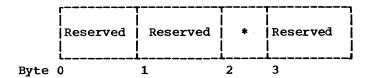
^{* =} optional

Figure 33. DOS Supervisor Calls (Part 1 of 2)

SVC		
Dec.	Hex.	Function
28*	1C	Return from user's stacker select routine (MICR type devices only).
29*	1D	Provide return from multiple wait macros WAITF and WAITM (except MICR type devices).
30*	1E	Wait for a QTAM element.
31*	1F	Post a QTAM element.
32 33 34	20 21 22	(Reserved). Reserved for internal macro COMRG. Reserved for internal macro GETIME.
35*	23	Hold a track for use by the requesting task only.
36*	24	Free a track held by the task issuing the FREE.
37*	25	Provide supervisor with linkage to user's AB routine for abnormal termination of a task.
38*	26	Initialize a subtask and establish its priority.
39*	27	Perform normal termination of a subtask. It includes calling the FREE routine to free any tracks held by the subtask.
40*	28	Inform the system of the termination of an event and ready any waiting tasks.
41*	29	Inform the system that a previously enqueued resource is now available.
42*	2A	Prevent tasks from simultaneous manipulation of a shared data area (resource).
43* 44* 45* 46* 47* 48 49 50	2B 2C 2D 2E 2F 30 31 32	Provide supervisor support for external creation and updating of SDR records. Provide supervisor support for external creation of OBR records. Provide emulator interface. Provide OLTEP with the facility to operate in supervisory state. Provide return from wait multiple WAITF for MICR type device. (Reserved) (Reserved) Reserved for LIOCS error recovery. Return phase length at OLTEP request.
	Dec. 28* 29* 30* 31* 32 33 34 35* 36* 37* 38* 40* 41* 42* 43* 44* 45* 46* 47* 48 49	Dec. Hex. 28* 1C 29* 1D 30* 1E 31* 1F 32 20 33 21 34 22 35* 23 36* 24 37* 25 38* 26 39* 27 40* 28 41* 29 42* 2A 43* 2B 44* 2C 45* 2D 46* 2E 47* 2F 48 30 49 31 50 32

^{* =} optional

Figure 33. DOS Supervisor Calls (Part 2 of 2)



*Byte 2

Bit 0: Turned on (X'80") at normal termination of subtask.

Bits 2-7: Reserved.

Note: Other blocks that may be used as ECBs are CCBs, TECBs, and MICR CCBs since posting is done in bit 0 of byte 2 of the block.

Figure 34. Event Control Block (ECB)

	*	Unused	**	ECB Address of Current Resource Owner		
1	х	ххх	X	xxx		
Byte	0	1 2 3	4	5 6 7		

*Byte 0: Availability byte - All ones when resource is in use. - All zeros when not in use.

**Byte 4: Flag byte: Bit 0 = 1, another task waiting for the resource.
= 0, no other task waiting for the resource.

<u>Note</u>: The address of the RCB is passed in register 1.

Figure 35. Resource Control Block (RCB)

	T	r	
Cancel Code (hex)	Message Code	Descriptive Part of Message (or Condition)	Label
10		Normal EOJ	ERR10
17	0S02I	(Same as 23 but causes dump	
i	i	because subtasks were attached	
İ		when maintask issued CANCEL	
Ì	ĺ	macro)	
18		(Eliminates cancel message	
ļ	1	when maintask issues DUMP	
1		macro with subtasks attached)	
19	0P74I	I/O Operator Option	
1A	0P73I	I/O Error	
1 B	0P82I	Channel Failure	ERRGO
1 1C	0S14I 0S12I	CANCEL ALL Macro Maintask Termination	ERR1C
1 1E	US121 US13I		ERR1D ERR1E
1 1E	05131 0P81I	Unknown ENQ Requestor CPU Failure	ERRIE
1 20	05011 08031 or	CPO FAITURE Program Check	ERRGO
1 20	05031 01 08111	Flogram Check	ERRZU
21	05111 05041 or	Illegal SVC	ERR21
1	08091	1110901 010	
22	0S05I or	Phase Not Found	ERR22
	0S06I		
23	05021	Program Request	ERR23
24	0S01I	Operator Intervention	ERR24
25	0P77I	Invalid address or insufficient	ERR25
ĺ	ĺ	core allocation to a partition.	
26**	0P71I	SYSXXX Not Assigned	ERR26
1	· .	(unassigned LUB code)	
27	0P70I	Undefined Logical Unit	ERR27
	•	(invalid LUB code in CCB)	
28	07707	(QTAM cancel in progress)	EXT02
30	0P72I	Reading Past /& Statement	ERR30
21	1 AD751	(on SYSRDR or SYSIPT)	EDD31
31	0P 7 5I	I/O Error Queue Overflow	ERR31
1		(error queue overflow	
		or no CHANQ entry avail-	
L	l	ante for EKL)	

Figure 36. Cancel Codes and Messages (Part 1 of 2)

Cancel Code (hex)	Message Code	Descriptive Part of Message (or Condition)	Label
32	0P 7 6I	Invalid DASD Address (disk) Irrecoverable I/O Error (tape)	ERR32
33	0P79I	No Long Seek (disk)	ERR33
34 	0P84I	I/O Error during fetch (unrecoverable I/O error during fetch of non\$ phase)	ERRGO
35	0P851	Job control open failure	
40		(load \$\$BEOJ)	EXT02
80		(cancel occurred in LTA)	EXT02
FF	0P78I	Unrecognized Cancel Code	
FF*	0P83x	Supervisor Catalog Failure	

All cancel-codes except in connection with DUMP-macro (code=X'00' is not a true cancel-condition) initially have a value X'40' higher than indicated above, but the X'40' bit is stripped by the SUPVR before fetching the Terminator. In addition to recognizing the cancel-codes above, the Terminator also recognizes the same codes with the X'80' bit on. The X'80' bit is tested for by \$\$BEOJ and subsequently reset.

*This cancel code is not significant in case of a supervisor catalog failure, because the system is placed in a wait state without any further processing by the Terminator. Thus, there is no conflict between this cancel code and the preceding X'FF' cancel code.

**If the CCB is unavailable, the logical unit is SYSxxx.

Figure 36. Cancel Codes and Messages (Part 2 of 2)

Physical IOCS is that portion of the resident supervisor that:

- Builds a schedule of I/O operations for all devices on the system (CHANQ table). Refer to Channel Scheduler on Chart 04 and to Figure 32 for CHANQ operation.
- Starts the actual I/O operations on a device (SIO). Refer to Actual I/O on Chart 04.
- Schedules the starting of all I/O operations and monitors all events associated with I/O. Refer to I/O Interrupt Processor on Chart 04.
- Performs error recovery procedures (ERP). Refer to Unit Check, Quiesce I/O, ERP Exits, and Resident Disk Error Recovery on Chart 06 and 07. Figures 37 through 41 illustrate: Command Control Block (CCB), Channel Command Word (CCW), Program Status Word (PSW), Channel Address Word (CAW), and Channel Status Word (CSW). See Figures 42 and 43 for CSW testing and error recovery block layout, respectively.

COMMAND CONTROL BLOCK

The CCB establishes communication between the problem program and physical IOCS. CCB is two double words in length with eight major fields, as shown in Figure 37. All data in the CCB is in the hexadecimal format. The eight fields of the CCB are listed and described as follows:

- Count Field (bytes 0, 1): Contains the residual count, which is stored in these two bytes by PIOCS when the CCB is removed from the queue.
- Transmission Information (bytes 2, 3): Used for communication between PIOCS and the problem program.

Note: Bytes 2 through 5 are ANDed off, by PIOCS, when the CCB is placed in the queue. However, the communication bits that were set on by the problem program are left on.

CSW Status Bits (bytes 4, 5): Contains the CSW status information, which is stored in these two bytes by PIOCS before control is returned to the problem program.

Note: The particular bits that are turned on in bytes 2 through 5 indicate the conditions that were detected by the problem program and PIOCS.

- 4. Symbolic Unit Address (bytes 6, 7): Contains the 2-byte hexadecimal representation of SYSnnn. This value represents the location of the logical unit in the LUB table (see Figure 23) and is placed in the CCB by the problem program.
- Byte 8: Is not used in EBCDIC files, and must then contain hexadecimal 0.

Contains the buffer offset (block prefix length) in ASCII files

Input (F, V, U) x'00' - x'63' Output (F, U) x'00' x'00' or x'04' Output (V)

- CCW Address (bytes 9-11): Contains the address of the CCW that is associated with this CCB. This address is placed in the CCB by the problem program.
- Byte 12: X'80'-CCB being used by ERP. X'40'-channel appendage routine for a teleprocessing device. X'20'-sense information desired. X'10'-message writer use. X'08'-EU tape error indicator. X'01'-seek separation or console buffering option specified.
- CCW Address in CSW (bytes 13-15): Contains the CCW address from the CSW. This address is stored by PIOCS before control is returned to the problem program. A CCB that has been queued, by PIOCS, to service a problem program I/O request cannot be used for a second problem program I/O request until the first request has been completed.

Note: Bytes 13-15 contain the address of the channel appendage routine when bit X'40' is set in byte 12.

9. Optional-Sense CCW (bytes 16-23): Bytes 16-23 are appended to the CCB by the CCB macro expansion when the user

desires sense information to be returned on unrecoverable I/O errors. The macro expansion also turns on bit 2 (X'20') in byte 12 of the CCB. User handles all error or exceptional conditions except program check, protection check, channel control check, and interface control check.

Bytes	Count 0 1	Transmission Information 2 3	CSW Status Bits			nbolic Unit Iress 7	Reserved for Logical IOCS 8	CCW Address	Reserved for Physical IOCS 12	CCW Address in CSW	Optional Sense CCW
Used for →	i		(Note 1) Byte 4 BIT DESIGNATION 32 Attention 33 Status modifier 34 Control unit enc 35 Busy 36 Channel end 37 Device end 38 Unit check 39 Unit exception	40 Program – cor interruption	Reproof Repr	SERNATION 1 1 1 1 1 1 1 1 1	ASCII Output Tapes Fixed:	Address of CCV Associated with this CCB	X'80'-CCB being	in the CSW Stored at Channel End, or Address of the Channel Appendage Routine for Teleprocessing Devices	8 Bytes Appended to th CCB when Sens I Information is Desired I I I I I I I I I I I I I I I I I I I
	! !			Byte	e 2				Console bottering	, 1	1
	Traffic Bit (Wait) (Note 5)	End - of - File (/* or /&) UCSB Parity Check (Line Complete) (Note 2)	Unrecoverable I/O Error	Accept Unrecoverable I/O	Return DASD Data Checks 2671 errors, or 1017/1018 errors to the user	Post at Device E	Data Checks Read or Veri Command, or	1018 2540 pment User Er D Routine on fy 3211 juested			
Bits		1	2	3	4	5	6	7	1		
Set On By—	PIOCS	PIOCS	PIOCS	Pr. Pr.	Pr. Pr.	Pr. Pr.	Pr. Pr.	Pr. F	r.		
		· ·		Byte	e 3						
	DASD – Data Check in Count Area MICR – SCU Not Operational 1285/1287/1288 Data Check	DASD - Track Overrun MICR - Intervention Required 1285/1287 - Keyboard Correction in Journal Tape	End of Cylinder MICR - (Note 4) 1287/1288 - Hopper Empty	2540, 2520 – Equipment Check Tape – Read Data Check DASD – Any Data Check 1285/1287 Equipment Check 1017/1018	Non – Recovery Questionable Condition: Card – Unusual Command Sequence DASD – No Record Foun.	No -Record Found Cond (Retry on 23 2314, or 23	ition Channel 9 311, Overflow o	the next to be exe	n CCW	·	
	Print Check/ Equipment Check	Mode 1017 – Broken Tape Print Quality/ Equipment Check		Data Check Print Check Data Check	1285/1287/1288 - Document Jam or Torn Tape UCSB Parity Chec (Command Retry)	-	1288 - End	*			
	l .										
Bits ———	0	1	2	3	4	5	6	7			

Note 1. Bytes 4 and 5 contain the status bytes of the Channel Status Word (Bits 32 – 47). If byte 2, bit 5 is on and device end results as a separate interrupt, device end will be ORed into CCB byte 4. Note 2. Indicates /* or /& statement encountered on SYSRDR or SYSIPT. Byte 4, bit 7 (unit exception) is also on.

Note 3. DASD data checks on count not returned.

Note 4. For 1255/1259/1270/1275/1419, disengage. For 1275/1419D, I/O Error in external interrupt routine (channel data check or busout check).

Note 5. The traffic bit (Byte 2, bit 0) is normally set on at channel end to signify that the I/O was completed. If byte 2, bit 5 has been set on, the traffic bit and bits 2 and 6 in byte 3 will be set on at device end. Also see Note 1.

Note 6. 1018 ERP does not support the Error Correction Function.

Note 7. This error occurs as an equipment check, data check, or FCB parity check.

Byte Bit Name Field

0	-1	2	3	4		5	
0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15	16 17 18 19 20 21 22 23	24 25 26 27 28 29 30 31	32 33 34 35 36	37 38 39	40 41 42 43 44 45 46 47	
Command Code		Flags	0 0 0	(Ignored)			
Α	·	В	С	D	E		

FIELD	NAME	DESCRIPTION
А	Command Code	Bits 0-7: Specify the operation to be performed. (See Part 2 of this Figure)
В	Data Address	Bits 8-31: Specify the location of a byte in main storage. It is the first location referred to in the area designated by the CCW.
C	Flags	Bits 32-36: Specify the flag bits used in conjunction with the CCW,
		Bit 32– Chain–Data (CD) causes the address portion of the next CCW to be used with the current CCW,†Note
		Bit 33- Chain-Command (CC) causes the command code and data address of the next CCW to be used. The chain data flag (bit 32) takes precedence over this flag.
		Bit 34– Suppress Length Indication (SLI) causes a possible incorrect length indication to be suppressed. The chain data flag (bit 32) takes precedence over this flag.
	:	Bit 35- Skip (SKIP) suppresses the transfer of information to main storage.
		Bit 36– Program Control Interruption (PCI) causes the channel to generate an interrupt when the CCW is fetched.
D	Reserved	Bits 37–39: (Must contain zeros)*
E	Ignored	Bits 40-47: Not checked
F	Count	Bits 48-63: Specify the number of bytes in the operation

Figure 38. Channel Command Word (CCW) (Part 1 of 2)

⁶ 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 Count F

^{*}The transfer in channel command (TIC) is the one exception to this statement.
†Note: Chain data cannot be done on 360/30 if a highspeed device is being used.

Example - 2311,2400 Model 3.

CHANNEL COMMAND CODES

Command Code assignments are listed in the following table. The symbol X indicates that the bit position is ignored; M identifies a modifier bit.

CODE	COMMAND		
MMMM 0 10 0	Sense		
XXX X 1 0 0 0 MMMM 1 1 0 0	Transfer in channel Read backward		
MMMM MM0 1	Write		
MMMM MM1 0	Read		
MMMM MM1 1	Control		

DASD, CHANNEL COMMAND CODES (see A26-5988)

			(M-T) Off	Multiple Track (M-T) Off				
Command 1	for CCW	Count	8-Bit Code 0123 4567	Hex Dec	Hex Dec			
Control	No Op Seek Seek Cylinder Seek Head Set File Mask Space Count Transfer in Channel Recalibrate (2311 only) Restore (2321 only) Sense I/O	X 6 6 6 1 1 X X	0000 0011 0000 0111 0000 1011 0001 1011 0001 1111 XXXX 1000 0001 0011 0001 0111 0000 0100	1B 27 1F 31 0F 15 X8 13 19 17 23				
Switching	Release Device Reserve Device	x x	1001 0100 1011 0100	94 148 B4 180				
Search †	Home Address EQ Identifier EQ Identifier HI Identifier EQ or HI Key EQ Key HI Key EQ or HI Key EQ or HI Key & Data EQ* Key A Data HI* Continue Scan EQ o' Continue Scan HI Continue Scan HI Continue Scan EQ or HI* Continue Scan EQ or Or HI Continue Scan EQ or HI Continue Scan Scan Scan HI Continue Scan Scan Scan Scan Scan Scan Scan Scan	4 (usually) 5 (usually) 5 (usually) 5 (usually) 1 (usually) 1 to 255 1 to 255 Note 1	0011 1001 0011 0001 0101 0001 0111 0001 0111 0001 0100 1001 0110 1001 0100 1101 0100 1101 0110 0101 0110 0101 0110 0101 0110 0101 0111 0101	71 113 29 41 49 73 69 105 2D 45 4D 77 6D 109 25 37 45 69 65 101	B9 185 B1 177 D1 209 F1 241 A9 169 C9 201 E9 233 AD 173 CD 205 ED 237			
Read †	Home Address Count Record R0 Data Key & Data Count, Key & Data Initial Program Load (IPL)	5 8 Number of bytes trans- ferred	0001 1010 0001 0010 0001 0110 0000 0110 0000 1110 0001 1110 0000 0010	12 18 16 22 06 06 0E 14 1E 30	9A 154 92 146 96 150 86 134 8E 142 9E 158			
Write	Home Address Record R0	5 (usually) 8+KL+DL of R0	0001 1001	19 25 15 21				
	Count, Key & Data Special Count, Key & Data* Data Key & Data	8+KL+DL 8+KL+DL DL KL & DL	0001 1101 0000 0001 0000 0101 0000 1101	1D 29 01 01 05 05 0D 13				

X = not significant; KL = Key Length DL = Data Length; EQ = Equal; HI = High

Desima	Command for CCW	8-Bit Code	Uav L
Device	Command for CCW	0 1 2 3 4 5 6 7	Hex De
1052	Read Inquiry BCD Read Reader 2 BCD Write BDC, Auto Carriage Return Write BDC, No Auto Carriage Return No Op Sense Alarm	0 0 0 0 1 0 1 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0	0A 10 02 02 09 09 01 01 03 03 04 04 0B 11
2540	Read, Feed, Select Stacker SS Type AA Read Feed (1400 compatability mode only) Feed, Select Stacker SS Type BA PFR Punch, Feed, Select Stacker SS Type BA Punch, Feed, Select Stacker SS Type BB SS Stacker D Data Mode 00 R1 0 EBCDIC 01 R2 1 Column Binary	S S D 0 0 0 0 1 0 1 1 D 0 0 0 1 0 1 1 D 1 0 0 1 0 5 S 1 0 0 0 1 1 S S D 0 1 0 0 1 S S D 0 1 0 0 1 S S D 0 1 0 0 1	
1442 N1	No Op RP3	MMM M 0 0 0 0 1 0 MMM M 0 0 0 0 0 1 1 0 MMM M 0 0 0 0	
1403 or 1443	Write, No Space Write, Space 1 After Print Write, Space 2 After Print Write, Space 3 After Print Write, Space 3 After Print Write, Skip To Channel N After Print Diagnostic Read (1403) Diagnostic Read (1443) Test 1/O Sense	0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 1 0 0 0 0	01 01 09 09 11 17 19 25 02 02 06 06 00 00 04 04
Carriage Control	Space Line Immediately	0 0 0 0 1 0 1 1 1 0 0 0 0 1 0 0 1 1 1 1	OB 11 13 19 1B 27 O3 O3
UCS	Allow buffer loading Load buffer (no folding) Load buffer (folding) Block data check latch Reset block data check latch	1 1 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	EB 23 FB 25 F3 24 73 12 7B 12
2400 Tape*	Read Backward (Overrides Data Converter On)	0 0 0 0 1 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0	0C 12 04 04 01 01 02 02
parit	C C C Codes Hex Dec D Density	ition X X X	Translator On Translator Off Request TIF

Figure 38. Channel Command Word (CCW) (Part 2 of 2)

86 DOS Supervisor and Related Transients

Byte Bit Name Field

0	1		2	3 .			4	5	6	7
0 1 2 3 4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19 20 21 22 23	24 25 26 27 28 29 30 31	32 33	34 35	36 37 38 39	40 41 42 43 44 45 46 47	48 49 50 51 52 53 54 55	56 57 58 59 60 61 62 63
System Mask	Key	CPU Mask	Interrupt	ion Code	ILC	СС	Prog. Mask		Instruction Address	
Α	В	С	. [)	Е	F	G		Н	

FIELD	NAME	DESCRIPTION
A	System Mask*	Bits 0-7: Are associated with the I/O channels and external signals as follows: Bit Interruption source 0 Multiplexor channel 1 Selector channel 1 2 Selector channel 2 3 Selector channel 3 4 Selector channel 4 5 Selector channel 5 6 Selector channel 6 7 Timer 7 Interrupt key External signal *A one-bit equals ON and permits an interrupt.
В	Protection Key	Bits 8–11: Form the CPU protection key. The key is matched with a storage key whenever a result is stored. If the protection feature is not implemented, bits 8–11 must be zero when loaded and are zero when stored.
С	CPU Mask (AMWP)	Bits 12–15: Form the CPU mask as follows: Bit Meaning [A] 12 If 1 - generate extended ASCII code [f 0 - generate EBCDIC (M) 13 If 1 - permits machine check interrupt [f 0 - prohibits machine check interrupt (W) 14 If 0 - the CPU is in the wait state [f 0 - the CPU is in the running state (P) 15 If 1 - the CPU is in the problem mode [f 0 - the CPU is in the supervisor mode
D	Interruption Code	Bits 16-31: Identify the cause of the interruption (See NOTE for specific interruption codes.)

FIELD	NAME	DESCRIPTION
E	Instruction Length Code	Bits 32 and 33: Indicate the length, in halfwords, of the instruction last executed, as follows:
-		00 (0) Not available (unpredictable) 01 (1) 1 halfword 10 (2) 2 halfwords 11 (3) 3 halfwords
F	Condition Code	Bits 34 and 35: Indicate the last condition code setting. All instructions do not set a condition code.
	·	00 Condition code 0 01 Condition code 1 10 Condition code 2 11 Condition code 3
G	Program Mask**	Bits 36–39: Form the program mask for the following program exceptions.
		Bit Exception
		36 Fixed-point overflow 37 Decimal overflow 38 Exponent underflow 39 Significance
		**A one-bit equals <u>ON</u> and permits a program check interrupt for a specific exception.
н	Instruction Address	Bits 40-63: Indicate the address of the leftmost byte of the next instruction to be executed.

SOURCE IDENTIFICATION	PSW BITS 16-31	MASK BITS		EXE- CUTION
Input/Output (old	l PSW 56, new PSW	120,	priority	4)
Multiplexor channel	00000000 aaaaaaaa	0	x	complete
Selector channel 1	00000001 aaaaaaaa	1	x	complete
Selector channel 2	00000010 aaaaaaaa	2	x	complete
Selector channel 3	00000011 aaaaaaaa	3	x	complete
Selector channel 4	00000100 aaaaaaaa	4	x	complete
Selector channel 5	00000101 aaaaaaaa	5	x	complet
Selector channel 6	00000110 аааааааа	6	x	complet
Program (old PSV	V 40, new PSW 104, 1	priori	y 2)	
Operation	0000000 00000001		1,2,3	suppres
Privileged operation	00000000 00000010		1,2	suppres
Execute	00000000 00000011		ź	suppres
Protection	00000000 00000100		0,2,3	suppress
				terminate
Addressing	00000000 00000101		0.1.2.3	suppress
				terminate
Specification	00000000 00000110		1,2,3	suppres
Data	00000000 00000111		2,3	terminat
Fixed-point overflow	00000000 00001000	36	1,2	complete
Fixed-point divide	00000000 00001001		1,2	suppress
				complete
Decimal overflow	00000000 00001010	37	3	complet
Decimal divide	00000000 00001011		3	suppress
Exponent overflow	00000000 00001100		1,2	terminat
Exponent underflow	00000000 00001101	38	1,2	complete
Significance	00000000 00001110	39	1,2	complete
Floating-point divide	00000000 00001111		1,2	suppress
Supervisor Call (o	ld PSW 32, new PSW	7 96, _I	oriority	2)
Instruction bits	00000000 rrrrrrr		1	complete
External (old PSW	24, new PSW 88, pr	riority	3)	
External signal 1	00000000 xxxxxx1	7	x -	complete
External signal 2	00000000 xxxxxx1x	7	x	complete
External signal 3	00000000 xxxxx1xx	7	. x	complete
External signal 4	00000000 xxxx1xxx	7	x	complete
External signal 5	00000000 xxx1xxxx	7	x	complete
External signal 6	00000000 xx1xxxxx	7	x	complete
Interrupt key	00000000 x1xxxxxx	7	x	complete
Timer	00000000 1xxxxxx	7	x	complete
Machine Check (o	ld PSW 48, new PSW	/ 112	priorit	y 1)
Machine malfunction	00000000 00000000	13	x	terminat
	. 1			
a Device addre				
r Bits of R ₁ and x Unpredictabl	l R ₂ field of superviso	OR CA	LL	

Mask bits 36 - 39 refer to the program mask.

Byte	0		1	2	3
Bit	0 1 2 3	4 5 6 7	8 9 10 11 12 13 14 15	16 17 18 1920 21 22 23	24 25 26 27 28 29 30 31
Name	Key	0000	4	— Command Address —	· · · · · · · · · · · · · · · · · · ·
Field	Α	В		С	

FIELD	NAME	DESCRIPTION
A	Protection Key	Bits 0 – 3 form the storage protection key for all commands associated with START I/O. This key is matched with a storage key whenever data is placed in storage. (Must contain zeros whenever storage protection is not implemented.)
В	Reserved	Bits 4 - 7 (Must contain zeros.)
С	Command Address	Bits 8-31 Designates the location of the first CCW in main storage associated with the START I/O. (The three low order bits, 29-31, must be zeros, specifying a CCW address on integral boundaries of a double word.)

Figure 40. Channel Address Word (CAW)

Channel Status Word (CSW)

Figure 41.

ſ	()	1	2	3	4	5	6	7
	0 1 2 3	4 5 6 7	8 9 10 11 12 13 14 15	16 17 18 19 20 21 22 23	24 25 26 27 28 29 30 31	32 33 34 35 36 37 38 39	40 41 42 43 44 45 46 47	48 49 50 51 52 53 54 55	56 57 58 59 60 61 62 63
	Key	0 0 0 0	-	 Command Address 		◄ ──── Sta	tus —	Cor	unt
	Α	В		C		[)		

IELD	NAME	DESCRIPTION				
Α	Protection Key	Bits 0-3 form the storage protection key used in the chain of operations at the subchannel.				
В	Reserved	Bits 4-7 (Must I	Bits 4-7 (Must be zeros.)			
С	Command Address	Bits 8-31 form	an address that is eight higher than t	the address of the last CC	W used. *	
D	Status	Bits 32 – 47 ident	ify the conditions in the device and	channel that caused the C	CSW to be stored.	
		Bits 32 – 39 are o	btained over the I/O Interface and i	indicate conditions detect	ed by the device or the control unit	
		Bits 40 – 47 are p	rovided by the channel and indicate	conditions associated wit	h the subchannel.	
		Each status bit re	presents one type of condition as fol	lows:		
		DEVI	CE OR CONTROL UNIT	CHA	CHANNEL/SUBCHANNEL	
		Bit Position	Designated Condition	Bit Position	Designated Condition	
Ì		32	Attention	40	Program - Controlled Interrupt	
		33	Status Modifier	41	Incorrect Length	
		34	Control Unit End	42	Program Check	
		35	Busy	43	43 Protection Check 44 Channel Data Check	
		36	Channel End	44		
		37	Device End	45	Channel Control Check	
1		38	Unit Check	46	Interface Control Check	
	1	L		L		

Bits 48-63 form the residual count for the last CCW used.

^{*} This address is not 8 higher on a command reject.

Status Bit	Status Condition	Action
45 46	Channel control check Interface control check	Enter wait state with all interrupts masked off. Note: System/370 CCH interrogates these bits for attempted recovery through the RMS function.
38 42 43 44 47	Unit check Program check Protection check Channel data check Channel chaining check	Exit to unit check on Chart 06 for error recovery.
32	Attention	For attention from a 1052, include attention task in task selection and take general exit (EXT03). Attention interrupts are ignored if: 1. System reallocation or condense is in operation. 2. Attention is not from a 1052.
35	Device busy	Skip channel end test.
36		See Charts CP and CQ for actions taken. Attempts to reschedule the channel (No attempt is made for the multiplex channel unless this is a burst-multiplex device).
37 34	Device end Control unit end	See Chart CL for actions taken. Attempts to reschedule the channel (If the multiplex channel is being rescheduled. If the device on the multiplex channel is a burst-multiplex device, both channel and device are rescheduled.)
33 and 35	Control unit busy	Reset device to available. The status is not tested unless neither channel end, device end, nor control unit end has occurred.

Figure 42. CSW Testing in I/O Interrupt Processor

Displacement from ERBLOC in Decimal	Length in Bytes	Label	Description
-2	2	ERRQ	Address of first error queue entry in table (ERQUE).
0	2	ERBLOC	Address of retry ERP exit (EXRTY).
2	2		Address of ignore ERP exit (EXIGN).
4	2		Address of DISWHY (retry) ERP exit (EXWHY).
6 .	2	YCHANQ	Address of the channel queue table (CHANQ).
8	2		Address of cancel ERP exit (EXCAN).
10	2	FULQUE	Address of last entry in error queue table.
12	2	ERQPTR	Address of last entry queued to table (initially ERQUE - 22).
14	2	RIK	Requestor I/O key (RIK).
16	2		Address of cancel attention exit (ATNCNL).
18	2		Address of attention dequeue exit (PUBDEQ).
20	2	ATNEXT	Address of attention exit (EXTO2).
22	8	SVC3NM	A – transient phase name field (\$\$ANERxx, where xx = any alphameric characters.
30	n x 22	ERQUE	n \times 22 bytes error queue entries, where n = 3 when SP = NO, and n = 5 when SP = YES.

Error Queue Entry (22 bytes)

Bytes	CSW 0-7	Pub Address of Device in Error 8-9	Flag Byte (see below)	Message Number 1	Sense Data ② 12-17	Disk Seek Address
	xxxxxxx	XX	X	Х	XXXXXX	xxxx

Flag Byte

Bit Designation O Unused		_
0 Unused	Bit	L
1 Intervention required 2 Passback	4 5	

Notes:

- See Figure 46 for Physical Transient error messages.
- See the following section, Physical Transient Programs, I/O Error Recovery Procedures and Sense Data.
- Put on by device ERP when user wants control returned on error.

Bytes 98 and 99 (X'62' - X'63') of the communications region contain the address of the error block. Label ERBLOC identifies the first byte of the table. The address of the first error queue entry is at ERBLOC - 2.

Figure 43. Error Recovery Block (ERBLOC) and Error Queue Entry

Physical transient programs are commonly referred to as A-transients. These infrequently-used sections of the supervisor reside in the core image library and are fetched by the resident supervisor (SVC 3) only when needed. Each program phase name begins with the prefix characters \$\$A. These phases are loaded singly into the A-transient area. Figure 2 for supervisor storage organization. The A-transient functions within DOS:

- Provide device-dependent Error Recovery Procedures (ERP).
- Issue messages associated with ERP operations, Message Writer.
- Process 1052 attention requests, Physical Attention Routines.
- Build and write OBR/SDR records.

The Physical Transient Overlap option allows user processing to continue during FETCH (SVCs 1, 2, and 3), LOAD (SVC 4), MVCOM (SVC 5), and ERP I/O operations. Otherwise, no task is selected while FETCH, LOAD, MVCOM, and ERP are processing.

Figure 44 illustrates each A-transient in terms of phase name, function, and program level chart identification.

ERP

To understand the error recovery procedures detailed in the flowcharts, you should be familiar with the sense information that corresponds to the individual I/O devices supported by this system.

Figure 45 illustrates the unit record equipment supported by ERP and also indicates the sense bits associated with each device. This figure is followed by ERP descriptions with their corresponding messages.

Note: Registers 1-8 cannot be used by error recovery phases. The contents of these registers may be destroyed should an interrupt cause a return to the supervisor.

Note: Although the disk error recovery procedure is not an A-transient, the sense data and action-taken information is included here to consolidate the sense data in this section of the manual. The disk ERP is part of the supervisor nucleus. See Chart 06.

MESSAGE WRITER

The message writer is a group of eight A-transients that build error messages, issue the message, analyze operator responses, and select the proper exit. Figure 46 for a listing of the error messages.

PHYSICAL ATTENTION ROUTINES

The physical attention routines are three A-transients fetched by the supervisor when an attention interrupt has been determined. The attention key signals operator communication with the system. If the operator chooses to initiate a foreground program or to use the nonresident attention routine facilities (other B-transients) the physical attention transients get the \$\$BATTNA root phase. If the operator is satisfying an operator intervention condition or canceling the job, the physical attention transients process the attention interrupt. When the physical attention routines are processing the interrupt, they perform parameter passing by using a common area called the interphase communications area. Figure 47 illustrates this area and its relationship to the entire A-transient area.

OBR/SDR A-TRANSIENTS

OBR/SDR Record Builder

The record builder routines are three A-transients that build and write on disk formatted OBR records, and update SDR disk counters. See Chart 12.

This A-transient passes a device to the SDR routine in the supervisor whenever an I/O error occurs. The list is a string of constants that map into some or all of the sixteen counters that are maintained by OBR/SDR support. See Figure 48 for examples of SDR device lists.

The OBR/SDR message writers are two A-transients that build and issue error messages in the event of an error while recording on the recorder file. These transients exit to the supervisor. See Figure 49 for a listing of the error messages.

Phase Name	Function	Program Level Chart ID
\$\$ANERRA \$\$ANERRB \$\$ANERRC	Error Recovery Monitor	11 11 11
\$\$ANERAK \$\$ANERAL \$\$ANERAM \$\$ANERAP \$\$ANERAQ \$\$ANERAR \$\$ANERAS \$\$ANERRD \$\$ANERRE \$\$ANERRE \$\$ANERRE	Tape (2400) Error Recovery	13 13 13 13 13 13 13 13 13 13 13 13
\$\$ANERRG \$\$ANERRH \$\$ANERRI \$\$ANERRJ \$\$ANERRK	Data Cell (2321) Error Recovery	11 11 11 11 11
\$\$ANERAE \$\$ANERAB \$\$ANERRN \$\$ANERRO \$\$ANERRP \$\$ANERRQ \$\$ANERRR \$\$ANERRS	Message Writer 	14 14 14 14 14 14 14
\$\$ANERAI \$\$ANERAJ	1017/1018 Paper Tape Error Recovery	12 12

Figure 44. A-Transient Programs (Part 1 of 2)

 Phase Name	 Function	Program Level
		Chart ID
\$\$ANERRT	MICR type devices (Single Address Adapter) Error Recovery	12
\$\$ANERRU \$\$ANERRV	Unit Record Error Recovery	11 11
\$\$ANERRW	1419/1275 (Dual Address Adapter) Error Recovery	12
\$\$ANERRX	Paper Tape Error Recovery	12
\$\$ANERR9	Optical Reader Error Recovery	11
\$\$ANERR6		11
\$\$ANERR7 \$\$ANERR8	Tape Cartridge Reader (2495) Error Recovery	11 11
\$\$ANERRZ		15
\$\$ANERRY \$\$ANERRO	Physical Attention	15 15
\$\$ANERR1	Modify Communications Region	None (See Chart TG)
*\$\$ANERRM		13
\$\$ANERAA \$\$ANERAC	OBR/SDR Record Builder	13 13
\$\$ANERAD	List Passer	11
\$\$ANERAF \$\$ANERAG	OBR/SDR Message Writer	13 13
\$\$ANERSA \$\$ANERSB	3211 Printer ERP	12 12
\$\$ANERSC	3211 Printer OBR Record Builder	12
*\$\$ANERRM is	also the initial message writer phas	se

Figure 44. A-Transient Programs (Part 2 of 2)

ERQUE	DASD	Tapes	Reader Punch	Print	ters	Printer Keyboard	Paper Tape Readers	Paper Tape Punch	Optical Reader	MICR	TCR
Device	2311, 2314, 2319, 2321	2400T7 2400T9 3420	1442, 2501, 2520, 2540	1403, 1404, 1443	3211	1052, 3210, 3215	2671 1017	1018	1285, 1287, 1288	1412, 1419, 1255, 1259, 1270, 1275	2495
Sense Bytes Byte 0 Bit 0	Command Reject									0	Cammand Reject
1	Intervention Required										
2	Busout Check										
3	Equipment Check										
4	Date Check						Data Check	8	Data Check		
5	Overrun		,	2	Buffer Parity Check				Overrun		
6	Track Condition Check		3		Load Check				Non- Recovery	Auto Select	Partition Check
. 7	Seek Check	Data Converter Check		Channel 9 Overflow			7		Keyboard Correction	0	
Byte 1 Bit 0	Data Check in Count				Command Retry				4		
1	Track Overrun				Print Check						
2	End - of - Cylinder				Print Quality						
3					Line Position						
4	No Record Found	At Load Point			Forms Check				Invalid Font		
5	File Protected				Command Suppress						
6	Missing Address Marker	File Protect Ring Present			Mechanical Motion						
7		Tape Not Compatible									

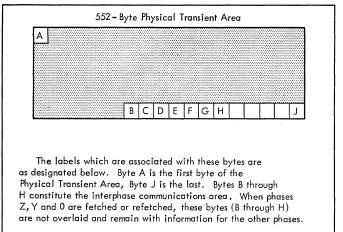
Notes: N/A = Not Applicable

- ① Command Reject or Disengage Failure (1412/1419); Command Reject or Control Command (1270/1275).
- 2 UCB Parity Check (1403 only).
- 3 Unusual Command Sequence (2540 read only).
- 4) Applies for 1287 to indicate tape (set to 1) or document (set to 0) mode.
- 5 Applies for 1287 in the document mode only.
- 6 SIO-Batch numbering switch off; TIO-Document Spacing Error (1287).
- 7 Applies for 1017 only; Broken Tape.
- (8) Only if Error Correction Feature present.

Figure 45. Sense Information for Devices Supported by Device Error Recovery

MESSAGE CODE (IN HEX)	10-CHARACTER MESSAGE	ERROR
08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31	C'INTERV REQ' C'BUSOUT CHK' C'EQUIP CHK' C'EQUIP CHK' C'OATA CHECK' C'VERIFY CHK' C'ADDR MRKER' C'OVERRUN C'SEEK CHECK' C'DTA CHK CT' C'FILE PROT' C'COMM REJCT' C'UNDETR ERR' C'ERR ON REC' C'NRF-MADDMK' C'BALST CELL' C'BLNK STRIP' C'PROG CHECK' C'PROT CHECK' C'INVAL SEEK' C'UNKNWN DEV' C'CHAN DTCHK' C'BK INTO LP' C'CONVRT CHK' C'DVC NOT OP'	OPERATOR INTERVENTION REQUIRED BUS OUT CHECK EQUIPMENT CHECK DATA CHECK VERIFY CHECK MISSING ADDRESS MARKER OVERRUN SEEK CHECK DATA CHECK IN COUNT FIELD VIOLATED FILE PROTECTION COMMAND REJECT UNDETERMINED ERROR ERROR DURING RECOVERY ATTEMPT NO RECORD FOUND & MISSING ADDRESS MARKER BALLAST CELL ACCESSED ON 2321 ACCESSED A PREVIOUSLY UNUSED STRIP I/O PROGRAM CHECK STORAGE PROTECTION CHECK SEEK ADDRESS NOT VALID DEVICE IN ERROR NOT RECOGNIZED CHANNEL DATA CHECK BACKSPACE INTO LOADPOINT TAPE CONVERT CHECK
32 33	C'NON COMPAT' C'BUF PARITY'	NONCOMPATIBLE TAPE ON DRIVE PARITY ERROR IN PRINTER BUFFER
34	C'BCH NM OFF'	BATCH NUMBERING SWITCH OFF ON MICR
35	C'NON RECOV '	NON-RECOVERY ON 1285
36	C'NO REC FND'	NO RECORD FOUND
37	C'DISEN FAIL'	DISENGAGE FAILURE ON MICR
38	C'INVLD FONT'	INVALID FONT ON 1287 IN DOCUMENT MODE
39	C'POSN CHECK'	POSITION CHECK ON 2495 TCR
40	C'BROKN TAPE'	BROKEN TAPE ON 1017
41	C'LOAD CHECK'	BUFFER LOAD CHECK ON 3211

Figure 46. Physical Transients Error Messages



Byte	<u>Label</u>	Phase	
Α	IJBPAR1 IJBPAR2	Z Y	Note: Bytes C, D and E
	IJBPAR3	Ö	are used to indicate the program(s) F1, F2 or BG, to be
В	PARLTK PARCOMM-1	Z	canceled. Bytes F, G and H indicate the programs
С	IJBPAR 1+504 PARCOMM IJBPAR2+504 PARCOMM2 PARCOMMC PARCOMMD	Z Y Z Y	which use devices which require operator intervention. Byte B indicates if a canceled program has fetched a logical transient.
F	PARCOMMI PARCOMMJ PARCOMMC+3 PARCOMMD+3	Z Y	
D,E, G,H	Addressed by incr	ementing	or decrementing one of these labels.

Figure 47. Interphase Communication Area (For A-Transients \$\$ANERRZ, Y, and 0)

XXXXX		жжжж	1	жжжж		жжжж
1	LIST FOR UNSUPPORTED DE	EVICE **	1	××	LIST FOR 2400 TAPE S	
жжжж		жжжж	1	XXXXX		жжжж
UNSUP	EQU " SDRMSK SENSE,0,2 SDRMSK SENSE,0,3 SDRMSK SENSE,0,5 SDRMSK END EOU "-UNSUP	BUS-OUT CHECK EQUIPMENT CHECK OVERRUN END OF LIST LENGTH OF LIST		TAPE	EQU ** SDRMSK SENSE,0,1 SDRMSK SENSE,0,2 SDRMSK SENSE,0,3 SDRMSK SENSE,0,5 SDRMSK SENSE,0,6	INTERVENTION REQUIRED BUS-OUT CHECK EQUIPMENT CHECK OVERRUN MASK WORD COUNT ZERO
ľ					SDRMSK SENSE,0,7	DATA CONVERTER CHECK
******	LIST FOR CHARACTER REAL	DER DEVICES 1285/1287/1412/1419	******		SDRMSK SENSE,3,0 SDRMSK SENSE,3,1 SDRMSK SENSE,3,2 SDRMSK SENSE,3,3	R/W VERTICAL REDUNDANCY CHECK LONGITUDINAL REDUNDANCY CHECK SKEW MASK CYCLIC REDUNDANCY CHECK
CHAR	EQU * SDRMSK SENSE,0,0 SDRMSK SENSE,0,2 SDRMSK SENSE,0,5 SDRMSK END	COMMAND REJECT BUS-OUT CHECK OVERRUN END OF LIST	1 1 1	LTAPE	SDRMSK SENSE,3,4 SDRMSK SENSE,1,0 SDRMSK END EQU "-TAPE	SKEW REGISTER VRC MASK NOISE MASK END OF LIST LENGTH OF LIST
LCHAR	EQU %-CHAR	LENGTH OF LIST	1	xxxxx		жжжж
жжжж		жжжж	!	**	LIST FOR DASD 2311/2	314/2321 ** ******
××	LIST FOR UNIT RECORD DI		1			
жжжж		xxxx	1	DASD	EQU *	
UNIT	EQU ** SDRMSK SENSE,0,1 SDRMSK SENSE,0,2 SDRMSK SENSE,0,3 SDRMSK END EQU **-UNIT	INTERVENTION REQUIRED BUS-OUT CHECK EQUIPMENT CHECK END OF LIST LENGTH OF LIST	1		SDRMSK SENSE,0,1 SDRMSK SENSE,0,2 SDRMSK SENSE,0,3 SDRMSK SENSE,0,5 SDRMSK SENSE,0,6 SDRMSK SENSE,0,7 SDRMSK SENSE,2,0	INTERVENTION REQUIRED BUS-OUT CHECK EQUIPMENT CHECK OVERRUN TRACK CONDITION SEEK CHECK UNSAFE
*****	LIST FOR 1052 CONSOLE	KKHKK KK KKKKK	1		SDRMSK BYPASS SDRMSK SENSE,2,2 SDRMSK SENSE,2,3 SDRMSK SENSE,2,4	BYPASS THIS COUNTER SERIALIZER/DESERILIZER CONTROL UNIT TAG LINE ALU CHECK
CONSL	EQU ** SDRMSK SENSE,0,1 SDRMSK SENSE,0,2 SDRMSK SENSE,0,3 SDRMSK SENSE,0,5 SDRMSK END EQU **-CONSL	INTERVENTION REQUIRED BUS-OUT CHECK EQUIPMENT CHECK OVERRUN END OF LIST LENGTH OF LIST	 	LDASD *** * *	SDRMSK BYPASS SDRMSK SENSE,1,6 SDRMSK END EQU "-DASD 2495 TAPE CARTRIDGE	BYPASS THIS COUNTER MISSING ADDRESS MARKER END OF LIST LENGTH OF LIST **** READER ** ****
*****	LIST FOR 2540 READER, PI	жжжж UNCH жж жжжж	! ! !	CARTAP	SDRMSK SENSE,0,1 SDRMSK SENSE,0,2	INTERVENTION REQUIRED BUS-OUT CHECK
RDPCH LRDPCH	EQU " SDRMSK SENSE,0,1 SDRMSK SENSE,0,2 SDRMSK SENSE,0,3 SDRMSK BYPASS SDRMSK SENSE,0,6 SDRMSK END EQU "-RDPCH	INTERVENTION REQUIRED BUS-OUT CHECK EQUIPMENT CHECK SKIP THIS COUNTER UNUSUAL COMMAND SEQUENCE END OF LIST LENGTH OF LIST	 	LCARTAF	SDRMSK SENSE,0,6 SDRMSK END EQU *-RDPCH	POSITION CHECK LENGTH OF LIST

PHASE		RECORDER FILE ERROR MESSAGE
\$\$ANERAF	0T01I	0CUUSDR RECORD OVERFLOWED
	0T02I	SDR AREA FULL OCUU
	0T03I	ERROR ON RECORDER FILE AT CCHHR
\$\$ANERAG 	0T00I 0T04I	LAST TRACK ON RECORDER FILE CHANNEL QUE FULL NO RECORD

Figure 49. Physical Transients Error Messages for OBR/SDR

ERROR LOGGING AND RECOVERY

Error logging and recovery procedures are done by the I/O Error Logging (ERRLOG), Machine Check Recording and Recovery (MCRR), and Machine Check Analysis and Recovery (MCAR) functions. These routines collect information about the reliability of the hardware. The environment records produced facilitate diagnosis and repair of a system and thus reduce interruptions due to hardware failure.

The system recovery portion of the MCRR function on System/360 reduces the number of conditions which cause the system to enter an uninterruptible wait state. System recovery is accomplished by canceling all affected tasks.

MCAR functions only when the MODEL option equals a System/370 CPU. If ERRLOG is not specified, MCAR forces the ERRLOG=YES option at system generation. MCAR gathers reliability information on SYSREC and contains error recovery procedures to minimize system hard waits.

If ERRLOG=RDE (Reliability Data Extractor) is specified, users of System/370 systems can gather additional data about hardware reliability. RDE writes IPL and EOD (End Of Day) records on SYSREC. These records indicate the reason for IPL and identify the RDE data on SYSREC.

For more information about MCAR, see the section Recovery Management Support for System/370.

I/O ERROR LOGGING (ERRLOG)

The Error Log function records two types of I/O errors. The Outboard Recorder (OBR) records pertinent data when a hard I/O error occurs. A hard I/O error is one which cannot be retried or cannot be corrected after a standard number of retries. The Statistical Data Recorder (SDR) records the cumulative error status of an I/O device. The data recorded by OBR and SDR may be processed and displayed by the Environment Record Editing and Printing (EREP) program. For the internal logic of the EREP program, refer to the System Service Program PLM, listed in the Preface.

Outboard Recorder (OBR)

OBR creates records when I/O errors occur which cannot be corrected by standard programmed error recovery procedures. The OBR records are built and written on the Recorder File (SYSREC) by two A-transients, \$\$ANERRM and \$\$ANERAA. Figure 49 shows the information contained in the OBR record. See Chart 12 for the OBR record builder and record writer A-transients.

Statistical Data Recorder (SDR)

SDR records the cumulative error status of each I/O device on the system. Sixteen half-byte counters are retained in core storage for each device. Each half-byte counter corresponds to one of the sixteen 2-byte error counters of the SDR record. These in-core counters are updated when an I/O error occurs. Figure 51 shows the SDR record format.

Whenever an OBR record is written onto the Recorder File, the SDR record for the device in error is also updated. When the SDR update routines are processing, they pass parameters in a common area, the SDR Communications Region. Figure 26 illustrates this region. SDR routines in the SEND macro expansion update internal counters and record information, and schedule Recorder File updates.

The counter update routine uses a device list passed by the A-transient \$\$ANERAD just before the ERP A-transient processing begins. Figure 48 display the SDRMSK device lists that are passed to the SDR processor whenever an error occurs on a given device. (SDRMSK is an internal macro that generates the device list entries used by the SDR processor. It is not documented in this manual.)

The first two in-core counters, which record, read, and write data check occurrences, are handled by the SDR processor itself and have no corresponding entry in the SDRMSK list. The SDR processor tests the CSW bit that corresponds to data check and examines the OP code of the CCW in question to determine if it is a read or write command.

The first entry in the SDRMSK list corresponds to the third in-core counter, second to the fourth, third to the fifth, and so on. SDRMSK Sense 0,1 means that this 1-byte generated entry corresponds to sense byte 0, bit=1 of the device associated with that list.

The updated SDR record is written on the Recorder File (SYSREC) by the A-transient \$\$ANERAC when thirteen errors have occured on a device. Chart 08 gives a description of the SDR update routines. See Charts 09 and 10 for \$\$ANERAD and \$\$ANERAC.

Writing OBR/SDR Records

It is possible to write or update SDR records and write OBR records for devices not explicitly supported by the system by using the SVCs 43 and 44.

The address of the compressed SDR record area must be supplied in general register 1 before the SVC 43 is issued. SVC 43 causes a branch to the SDRSDR routine in the supervisor to complete processing of the record. Immediately following the SVC, the WAIT macro must be issued on the address in register 1.

Example:

LA 1,SDRAREA SVC 43 WAIT (1) or SDRAREA

The SDR record area must be 22 bytes long and have three fields. The first field is reserved for the SDR processor. The second field must be initialized as zeros. During write, the SDR processor posts status, operation complete, or I/O error. The WAIT macro tests for operation complete. The third field is the updated SDR record. The counters field of the record must be in compacted format, meaning 16 half-byte error counters for a total of 8 bytes in length. Figure 51 shows the SDR record format with the 16 error counters in expanded form. The SDR processor expands the field to 16 two-byte areas on the disk.

FIELD SIZE 1	CONTENTS Reserved for SDR processor X'00' Initially
l Dyce	X'80' Posted for operation complete
	X'20' Posted for I/O error during write
10.7	issued with Recorder file off.*
3	SDR record with compacted error counters field - 16 half-byte counters.
AREA SIZ	E - 22 Byte Total
issuer of th	t be interrogated by the e SVC 43. If this bit is record was not written.

The address of the OBR record area must be supplied in general register 1 before the SVC 44 is issued. SVC 44 causes a branch to the SDROBR routine in the supervisor to write the OBR record. Immediately following the SVC, the WAIT macro must be issued on the address in register 1.

Example:

LA 1, OBRAREA SVC 44 WAIT (1) or OBRAREA

The OBR record area must be 83 bytes long and have 3 fields. The first field is reserved for the OBR processor. The second field must be initialzed as zeroes. During write, the OBR processor posts status, operation complete, or I/O error. The WAIT macro tests for operation complete. The third field is the OBR record. Figure 50 shows the OBR record format.

FIELD		CONTENTS
[1	2 Bytes	Reserved for OBR processor
12	1 Byte	X'00' Initially [
i	-	X'80' Posted for operation
i		complete
i		X'20' Posted for I/O error
ļ		during write.
ļ		
ļ.		X'10' Posted if SVC 44 is
l .		issued with Recorder file
1		off.*
[3	80 Bytes	OBR record.
İ	_	i
i	AREA STZ	E - 83 Byte Total
i		2 00 2700 20002
l I ★mhid	e hit muc	t be interrogated by the
		e SVC 44. If this bit is
		· · · · · · · · · · · · · · · · · · ·
on,	the OBR	record was not written.
L		

```
GENERAL FORMAT
                   SIZE
                             CONTENT/DESCRIPTION
Record Type
                   1 Byte
                             X'01' identifies OBR record.
                   4 Bytes
                             In packed decimal form:
Date
                                00YYDDDF = (Year, julian Date, Zone)
Time
                   4 Bytes
                              System time of day.
Program ID
                   8 Bytes
                              Name of JOB (in a Batched partition), or program name.
First CCW
                   8 Bytes
                             First CCW of failing chain.
Failing CCW
                   8 Bytes
                              CCW on which error occurred.
Channel & Unit
                   2 Bytes
CSW
                   8 Bytes
Sense
                   6 Bytes
                             Device sense bytes.
                   6 Bytes
                             Reserved for new sense.
Seek Address
                   6 Bytes
                              BBCCHH
Device Type
                   4 Bytes
                              Device type as stored in PUB table, mode setting, and
                              characteristics.
Poll Characters
                   4 Bytes
|Logical Unit
                   2 Bytes
Volume ID
                   6 Bytes
Reserved
                   2 Bytes
Guard Byte
                             X'FF'
                   1 Byte
                   RECORD CAPACITY - 80 Bytes Total
Note:
       Device Type
                         Records/Track
            2311
                               25
            2314
                               40
IBM 3211 FORMAT
                   SIZE
                              CONTENT/DESCRIPTION
                             X'01' identifies OBR record.
Record type
                   1 Byte
                   4 Bytes
                              Format is 00YYDDDZ (Year, julian Date, Zone in packed
Date
                              decimal).
                              System time of day.
Time
                   4 Bytes
                             Program name, or job in batched partition. First CCW in failing chain.
Job ID
                   8 Bytes
|First CCW
                   8 Bytes
|Failing CCW
                   8 Bytes
                              CCW on which error occurred.
|Channel & Unit
                   2 Bytes
                             Failing device address.
CSW
                   8 Bytes
Sense
                   6 Bytes
                              Six sense bytes produced by 3211.
                   6 Bytes
                              Reserved.
Device type
                   4 Bytes
                              First two bytes taken from bytes 4, 5 of 3211 PUB entry.
|Logical unit
                   2 Bytes
                   8 Bytes
Parity error
                              Up to 8 parity error locations in the print line buffer
 locations
                              (one byte per location, X'01' to X'96').
                   8 Bytes
Contents of
                              Contents of positions referenced in parity error locations.
 parity error
 locations
                   1 Byte
|Flag
                              Flag contains:
                               X'40' - 8 or fewer parity error locations.
                               X'41' - 8 or fewer parity error locations, but locations
                                       are unobtainable.
                               X'42' - Number and contents of parity error locations are
                                       unobtainable.
                               X'5C' - More than 8 parity error locations.
                               X'5D' - More than 8 parity error locations, but contents
                                       are unobtainable.
                              X'FF' = 3211 OBR record indicator.
Device ID
                   1 Byte
                              X'FF' designates end of record.
Guard byte
                   1 Byte
```

Figure 50. OBR Record Formats

KEY	FIELD Channel & Unit	SIZE 2 Bytes	DESCRIPTION Last Record X'FFFE' Available Record X'FFFF'
DATA	Poll Characters FIELD Type	4 Bytes SIZE 1 Byte	DESCRIPTION Device Type from PUB Table
	Characteristics	1 Byte	X'40' if Switchable Device X'02' if Burst on MPX Channel X'01' if 7 Track Tape
i I	Counters * Reserved	16x2 Bytes 2 Bytes	Error Counters
	Guard	1 Byte	X'FF'
<u> </u>	RECORD CAPACITY	- 43 Bytes T	otal

Note:	Device Type	Records/Track
	2311	29
	2314	38

*The SDR processor expands each of the sixteen half-byte in core counters into two byte counters on the disk. There can be thirteen errors on a device before updating the disk; the capacity of the 2 byte expansion is 32767 errors before overflow is reached.

Figure 51. SDR Record Format

MACHINE CHECK RECORDING AND RECOVERY (MCRR)

The SYSGEN option MCRR is valid for only System/360. The Disk Operating System provides System/370 a similar, but automatic, function. See the Recovery Management Support for System/370 section.

The MCRR function records system error information after a machine check, channel control check, interface control check, or channel data check occurs. MCRR then cancels the damaged task or tasks. No attempt is made to recover on any error involving the MCRR function. The recorded data can be processed and displayed by the Environment Record Editing and Printing (EREP) program. For information regarding the internal logic of the EREP program, refer to the System Service Program PLM, listed in the Preface of this manual.

The MCRR function builds two types of records on the Recorder File (SYSREC). Whenever a log-out occurs as a result of a channel failure, the routine builds model dependent Channel Inboard Error records and cancels the damaged task(s). The A-Transient \$\$ANERAA writes the CIE record. When a machine check occurs, the routine builds model dependent CPU Machine Check records, and cancels the damaged task(s). The A-Transient \$\$ANERAA writes the CPU record. Figure 53 shows the format of the two record types. See Chart 10 for a description of the MCRR routine.

If another MCRR condition occurs while the MCRR routine is in progress, the system enters a hard wait after posting the SEREP cancel code in low core.

MCRRPSW1 (See Note)							***************************************
			, .				1
	0 (Hexadecimal	Displacement)	8		10	14	
	0 (Decimal Dis	olacement)	8		16	20	
	MCRR	PSW Reentrant Address of	MCRR	PSW Address of	Address of Channel Failure	Address of Machine Check	
: 		MCRR Routine		MCRR Routine	Routine	Routine	
ı	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX]
Key to displacement:							
	< Recording and ant address (MC		Loaded to enable RR routine.	machine check	interrupts. Seco	nd word (displace	ement 4–7)
	k Recording and Laddress (MCRRI		Loaded to enable	machine check	interrupts. Seco	nd word (displace	ement 12-15)
16 Address of char	16 Address of channel failure routine (MACHEK1).						
20 Address of machine check routine (MACHEK).							
Note: MCRRPSW1 is t	Note: MCRRPSW1 is the label of the first byte of the MCRR Linkage Table.						
				,			

Figure 52. Machine Check Recording and Recovery (MCRR) Linkage Table

Record 1:		
ENTRY	SIZE	CONTENT/DESCRIPTION
Record ID	1 Byte	X'02' CIE Record ID X'nnNN' n of N records
Record Number	2 Bytes	X'nnNN' n of N records
	1 Byte	
Date	4 Bytes	In packed decimal form (00YYDDDF = (Year, julian Date, Zone)
 Time	4 Rytes	System time of day
		C'XXXXXXXX' Job name
10 Active Devices	20 Bytes	X'cuu' First 10 active devices on
1	20 27000	Channel
First CCW	8 Bytes	First CCW of failing chain
Failing CCW	8 Bytes	CCW on which error occurred
CSW	8 Bytes	
Failing Device		
Log-Out	12 Bytes	Mod 30 core bytes X'80'-X'8B'
ļ		Mod 40 core bytes X'80'-X'8B'
!		Mod 50 core bytes X'80'-X'8B'
 Indicator	1 Preto	or X'88'-X'93' X'01' OBR full log bit - Mod 50 only
Indicator	т русе	Unused Models 30 & 40
 End of Record	1 Byte	
i Ena of Record	I Dice	4. 1.
	RECORD CA	PACITY - 80 Bytes Total
Record 2: Models	40 & 50 on	ıly
 ENTRY	SIZE	CONTENT/DESCRIPTION
ENIKI	SIZE	CONTENT/ DESCRIPTION
Record ID	1 Bvte	X'02' CIE Record ID
Record Number	2 Bytes	X'nnNN' n of N records
Model Number	1 Byte	X'nnNN' n of N records X'40' or X'50'
Log-Out	75 Bytes	Mod 40 core bytes X'8C'-X'D6'
1	or	Mod 50 core bytes X'8c'-X'D6' or
l .	55 Bytes	Mod 50 core bytes X'95'-X'CB'
!	20 Bytes	Mod 50 only - Unused with short
	4.5.	record.
End of Record	1 Byte	X'FF.
l 	RECORD CA	PACITY - 80 Bytes Total

Figure 53. Machine Check Recording and Recovery (MCRR) Record Formats (Part 1 of 4)

Record 3: Models 40 & 50 only				
ENTRY	SIZE	CONTENT/DESCRIPTION		
Model Number	2 Bytes 1 Byte 75 Bytes	X'02' CIE Record ID X'nnNN' n of N records X'40' or X'50' Mod 40 core bytes X'D7'-X'121' Mod 50 core bytes X'D7'-X'121' Unused for Partition Log-Out X'FF'		
RECORD CAPACITY - 80 Bytes Total				
Record 4: Models 40 & 50 only				
ENTRY	SIZE	CONTENT/DESCRIPTION		
Record Number Model Number Log-Out	2 Bytes 1 Byte 34 Bytes	Mod 50		
RECORD CAPACITY - 80 Bytes Total				

Figure 53. Machine Check Recording and Recovery (MCRR) Record Formats (Part 2 of 4)

Record 1:			
ENTRY	SIZE	CONTENT/DESCRIPTION	
Record ID Record Number Model Number Date	1 Byte 4 Bytes	X'04' CPU Record ID X'nnNN' n of N records X'30', X'40', X'50' In packed decimal form 00YYDDDF = (Year, julian Date, Zone)	
•		System time of day C'XXXXXXXX' Job name X'cuu' First 10 active I/O units on channel	
PSW G.P. Registers Unused End of Record	8 Bytes 28 Bytes 3 Bytes	Machine check old PSW Registers 0-6	
<u> </u>	RECORD CAPACITY - 80 Byte Total		
Record 2:			
ENTRY	SIZE	CONTENT/DESCRIPTION	
F.P. Registers Unused	7 Bytes		
End of Record	1 Byte		
 Record 3:	RECORD CE	APACITY - 80 Byte Total	
Record 3: ENTRY	SIZE	CONTENT/DESCRIPTION	
Record ID Record Number Model Number Log-Out 	2 Bytes 1 Byte 12 Bytes 75 Bytes	X'04' CPU Record ID X'nnNN' n of N Records X'30', X'40', X'50' Mod 30 core bytes X'80'-X'8B' Mod 40 core bytes X'80'-X'CA' Mod 50 core bytes X'80'-X'CA'	
Unused End of Record	63 Bytes 1 Byte	(Model 30 only)	
RECORD CAPACITY - 80 Byte Total			

Figure 53. Machine Check Recording and Recovery (MCRR) Record Formats (Part 3 of 4)

Record 4: Models 40 & 50 only				
ENTRY	SIZE	CONTENT/DESCRIPTION		
Record Number Model Number	2 Bytes 1 Byte 75 Bytes	Mod 40 core bytes X'CB'-X'115' Mod 50 core bytes X'CB'-X'115'		
RECORD CAPACITY - 80 Byte Total				
Record 5: Models 40 & 50 only				
ENTRY	SIZE	CONTENT/DESCRIPTION		
Record Number Model Number Log-Out Parities	2 Bytes 1 Byte 46 Bytes 14 Bytes 12 Bytes 29 Bytes	X'04' CPU Record ID X'nnNN' n of N records X'40' or X'50' Mod 40 core bytes X'116'-X'143' Mod 50 core bytes X'116'-X'123' Registers parities (Mod 50 only) Mod 40		
 End of Record	49 Bytes 1 Byte	MOD 50 X'FF'		
RECORD CAPACITY - 80 Byte Total				

Figure 53. Machine Check Recording and Recovery (MCRR) Record Formats (Part 4 of 4)

I/O ERROR RECOVERY PROCEDURES AND SENSE DATA

2400 TAPE ERROR RECOVERY

Byte 0, Bit 3--Equipment Check

Action: Take equipment error exit
(cancel).

Message: OP10 EQUIP CHK.

Byte 0. Bit 2--Bus Out Check

Action: If at initial selection and command chaining, take equipment error exit (cancel); otherwise, retry.

Device End in Unit Status: If this condition occurs during a write, the tape is repositioned and the command is reissued. If this condition occurs during another type of command, the command is reissued. This procedure is followed until five retries have been attempted; if recovery is not sucessful, take equipment error exit (cancel).

Message: 0P09 BUSOUT CHK.

Byte 0, Bit 1--Intervention Required

Action: No Device End in Unit Status; TU Status B (sense byte 1, bit2) is tested. If TU Status B is off, the device is nonexistent. No retries are attempted. If TU Status B is on, an operator intervention required message is provided and, when the unit is made ready, the command is reissued.

Message: 0P08 INTERV REQ.

Action: Device End in Unit Status: If the command was a Rewind- Unload, processing continues; otherwise, take the equipment error exit (cancel).

Message: OP19 UNDETR ERR.

Byte 0, Bit 0--Command Reject

Action: If at load point and file protect, rewind and unload.

Message: OP17 FILE PROT.

Action: Take equipment error exit
(cancel).

Message: 0P18 COMM REJCT.

Byte 0, Bit 5--Overrun

Action: The tape is repositioned and the command is reissued. This procedure is followed until five retries have been attempted. If recovery is not sucessful, take equipment error exit (cancel).

Note that a data check during overrun suppresses the overrun condition.

Byte 1, Bit 4--Load Point

<u>Action</u>: If not caused by read backward operation, take equipment error exit (cancel).

Message: 0P29 BK INTO LP (Backspace
into Load Point Command).

Byte 0, Bit 4--Data Check

Action: If the operation is read or read backward, and if the noise bit (Byte 1, Bit 0) is on, or if more than 11 bytes were read, the tape is repositioned and the read or read backwards is retried. If the noise bit is off and the block size is less than 12 bytes, another block is read and operation continues. This procedure is followed until forty retries have been attempted. Every fifth retry is preceded by a tape cleaner action. A TIE (Track-in-Error) command is issued before every reread to send sense byte 2, which contains track-in-error information, to the tape control unit.

If the above procedure does not recover the error, the error routine tries to recover by reading in the opposite direction. If, however, any of the following conditions exists, the routine does <u>not</u> attempt opposite-direction recovery:

- Data chaining is being performed.
- Data conversion mode and 7-track tape are being used.
- The original CCW count is less than the physical block size on the tape.
- "Suppress data transfer" is specified in the original CCW.

In attempting opposite-direction recovery, the error routine first prepares to read without repositioning the tape. It issues a Track-in-Error command to send to the tape control unit the sense byte 2 obtained during the last original-direction retry. routine then issues a Read or Read Backwards command as its first retry. On subsequent retries, it repositions the tape, issues a Track-in-Error command, then a Read or Read Backwards command. Before every fifth retry, the routine causes a tape-cleaner action. The routine continues to retry until it either succeeds (i.e., no unit check occurs) or has made 40 unsucessful retries.

The read-opposite CCW has the "suppress data transfer" bit set until the first successful retry. The routine then alters the read-opposite CCW so that it can transfer data. The alteration consists of clearing the "suppress data transfer" bit and placing the "exact" count and the data address in the CCW. The "exact" count equals the block size to be read. If successful, the routine issues a Forward Space Record or

Backward Space Record command to reposition the tape past the block being read.

If all 40 read-opposite recovery attempts are unsuccessful, the routine makes one final retry, this time attempting to read in the original direction. Unlike previous attempts, it does not issue a Track-in-Error command before the Read or Read Backward command. Note that the routine avoids the final read attempt if either a permanent bus-out check occurs when the repositioning command is issued or an equipment check occurs. If the user will not accept the data check, take the cancel, ignore exit after the specified number of retries. If the user will accept the data check, return control to the user.

If the operation is a write or write tapemark, the tape is repositioned, an Erase Gap command is issued, and the Write or Write Tapemark command is reissued. This procedure is followed until fifteen retries have been attempted; then take equipment error exit (cancel).

If the operation is an erase gap, the command is reissued. This procedure is followed until three retries have been attempted; then take equipment error exit (cancel).

Message: 0P11 DATA CHECK.

•CSW Bit 44--Channel Data Check

Action: If this condition occurs during a read or write operation, the tape is repositioned and the command is reissued. If this condition occurs during a control command, the command is reissued. This procedure is followed until five retries have been attempted; then take equipment error exit (cancel).

Message: 0P28 CHAN DTCHK.

•Byte 0, Bit 7--Data Converter Check

Action: Take equipment error exit
(cancel).

Message: 0P30 CONVRT CHK.

•Byte 1, Bit 7--Not Capable

Action: Rewind and unload tape. Take equipment error exit.

Message: 0P32 NON COMPAT.

•No Previous Sense Bits On

Action: No retries are attempted.
Take equipment error exit.

Message: 0P19 UNDETR ERR.

•CSW Bit 47--Chaining Check

Action: The tape is repositioned and the command is reissued. This procedure is followed until five retries have been attempted; then take equipment error exit (cancel).

Message: 0P14 OVERRUN.

1052 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: One retry, take equipment
error exit (cancel, retry, ignore).

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: One retry, take equipment error exit (cancel, retry, ignore).

Message: OP10 EQUIP CHK.

• Byte 0, Bit 1--Intervention Required

Action: Execute audible alarm command and take operator intervention exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: One retry, take equipment
error exit (cancel, retry, ignore).

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: 0P18 COMM REJCT.

1403-1443 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one retry--take equipment error exit (initial selection: cancel, retry. Channel end: cancel, retry, ignore).

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Take equipment error exit
(cancel, ignore).

Message: OP10 EQUIP CHK.

 Byte 0, Bit 5--Code General Storage Parity Error (1403 only)

Action: Take equipment error exit (cancel). UCS buffer must be reloaded.

Message: 0P33 UCB PARITY.

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention

exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: If initial selection, one retry; otherwise, take equipment error exit (initial selection: cancel, retry. Channel end: cancel, retry, ignore).

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 7--Channel 9

Action: Post CCB, take continue exit.

<u>Note</u>: This test is main storage resident.

• Byte 0, Bit 0--Command Reject

Action: If command code is UCS enable or inhibit data check, take continue exit; otherwise, take program check exit. This procedure allows UCS-oriented programs to operate on non-UCS hardware.

Message: 0P18 COMM REJCT.

• Byte 0, Bit 4--Data Check (1403 Only)

Action: Take equipment error exit
(cancel, ignore).

Message: 0P11 DATA CHECK.

1442 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one retry; then take equipment error exit (cancel, retry). If data transfer, take operator intervention exit.

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Take operator intervention

exit.

Message: OP10 EQUIP CHK.

■ Byte 0, Bit 1--Intervention Required

Action: Take operator intervention

exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: If initial selection, do one retry; then take equipment error exit (cancel, retry). If data transfer, take operator intervention exit.

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 4--Data Check

Action: Take operator intervention

exit.

Message: 0P11 DATA CHECK.

• Byte 0, Bit 5--Overrun

Action: Take operator intervention

exit.

Message: 0P14 OVERRUN.

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: OP18 COMM REJCT.

• CSW Bit 47--Chaining Check

Action: Take operator intervention

exit.

Message: 0P14 OVERRUN.

2501, 2520, 2540 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one retry; then take equipment error exit (cancel, retry). If read data transfer, take operator intervention exit. If punch data transfer, one retry; then take equipment error exit (cancel, retry).

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Reader--Take operator intervention exit. Punch--CCB option. Take equipment error exit (cancel, ignore). For 2520, Byte 0, Bit 7 indicates punch check.

Message: OP10 EQUIP CHK.

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention

exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: One retry; then take equipment error exit (cancel, retry). If the device is a 2520, do not retry if this is not initial selection (cancel, retry).

Message: 0P09 BUSOUT CHK.

 Byte 0, Bit 4--Data Check (Cannot occur on a 2520 punch)

Action: Take operator intervention

exit.

Message: OP11 DATA CHECK.

 Byte 0, Bit 5--Overrun (Cannot occur on 2540 or 2520 punch)

Action: Take operator intervention

exit.

Message: 0P14 OVERRUN.

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: 0P18 COMM REJCT.

 Byte 0, Bit 6--Unusual Command Sequence (2540 read only)

Action: Post CCB--take continue exit.

• CSW Bit 47--Chaining Check (2501, 2520 read only)

Action: Take operator intervention

exit.

Message: 0P14 OVERRUN.

2671 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one
retry. Take equipment error exit
(cancel).

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Test CCB for ignore option (byte 2, bit 4) and if on, turn on byte 3, bit 1 of the CCB and take equipment error exit (cancel, ignore, retry). Otherwise, take operator intervention exit.

Message: OP10 EQUIP CHK.

Note: When an equipment check occurs, reposition the paper tape to the beginning of the record in error to perform the retry operation. The

device must not be readied until this repositioning has been performed. If the ignore option is available, exercise this option by repositioning the tape to the beginning of the next record on the tape and then responding ignore on the 1052 keyboard. The ignore option is available to the operator whenever the user specifies any of the DTFPT ERROPT entry options.

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention
exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: One retry; if error persists,
take equipment error exit (cancel,
retry).

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 4--Data Check

Action: Test CCB for ignore option (byte 2, bit 4) and if on, turn on byte 3, bit 3 of the CCB and take equipment error exit (cancel, ignore, retry). Otherwise, take operator intervention exit.

Message: OP11 DATA CHECK.

When a data check occurs, the Notes: user's CCW is modified by the error routine to allow rereading of the last character. The data address is the last character read (character in error), and the byte count is decreased by the number of valid characters read. If the CCB ignore option is chosen and the operator responds ignore, the I/O operation is dequeued and posted with the unrecoverable error bit on (CCB byte 2, bit 2) and 2671 data-check bit on (CCB byte 3, bit 3).

To read the rest of the record, the problem program (logical IOCS) should add one to the CCW data address and subtract one from the byte count to adjust for not rereading the bad character. It should then reissue the EXCP. The operator must backspace the tape two characters for retry (option retry or on the A-type message

when ignore is not allowed). If the operator chooses the ignore option (the character in error is not to be reread), he must backspace the tape one character if the load key was pressed to free the tape or if the character preceding the character under the read head is an EOR (End-of-Record). Otherwise, no manual intervention is required for the ignore option. The ignore option is available to the operator whenever the user specifies any of the DTFPT ERROPT entry options.

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: 0P18 COMM REJCT.

Note: A record may not be partly on one tape and partly on another.

2311-2314 DASD ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: One retry; then take equipment error exit (cancel, retry).

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3 - Equipment Check

Action: Take equipment error exit
(cancel, retry).

Message: OP10 EQUIP CHK.

• Byte 1, Bit 4 - No Record Found

Action: Test for byte 1, bit 6
(Missing Address Marker). If present, execute restore command and take retry exit. After ten retries, take equipment error exit (cancel, retry). If not present, read Home Address and compare to user's Seek Address. If equal, post No Record Found to the CCB and take continue exit. If not equal, treat as a Seek Check.

Messages: 0P21 NRF - MADDMK (No Record
Found/Missing Address Marker).
0P15 SEEK CHECK (Home Address unequal
to Seek Address).

Note: Home Address is read, and the track address is provided for the error

message. For other errors, the track address is obtained from the user seek address if error occurs during channel program execution.

• Byte 0, Bit 7--Seek Check

Action: If byte 0, bit 0 (command reject) is on, take program check exit. Otherwise, execute restore command and take retry exit. After ten retries, take equipment error exit (cancel, retry).

Messages: 0P26 INVAL SEEK (Seek Check/Command Reject)
0P15 SEEK CHECK.

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention
exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: If retry count is greater than nine, take equipment error exit (cancel, retry); otherwise, take retry exit.

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 4 - Data Check

Action: CCB options (all data checks, data check on read or verify). If retry count is greater than 256, take equipment error exit (cancel, retry); otherwise, take retry exit. After each 16 retries, a recalibrate is performed until the maximum of 256 retries is reached. After 256 retries, post data check on count to CCB, if present; otherwise, post data check. If command code is verify (implied), post verify error in CCB.

The verify command is implied under the following conditions:

- The CCW has a command code X'01' (Write - Special Count, Key and Data), and the skip and SILI flags are set on.
- The CCW has a command code X'1E'
 (Read Count, Key and Data), the
 skip and SILI flags are set on, and
 this CCW follows a CCW with a write
 command code X'1D'.

Messages: 0P12 VERIFY CHK (Data Check
on Verify Command).
0P11 DATA CHECK (Data Check/not Data
Check on Count or Verify).
0P16 DTA CHK CT (Data Check on Count).

Note: Home Address is read, and the track address is provided for the error message. For other errors, the track address is obtained from the user seek address if error occurs during channel program execution.

• Byte 0, Bit 5--Overrun

Action: If retry count is greater than
nine, take equipment error exit
(cancel, retry); otherwise, take retry
exit.

Message: 0P14 OVERRUN.

• Byte 1, Bit 6--Missing Address Markers

Action: If retry count is greater than nine, take equipment error exit (cancel, retry); otherwise, take retry exit.

Message: OP13 ADDR MRKER.

Note: Home Address is read, and the track address is provided for the error message. For other errors, the track address is obtained from the user seek address if error occurs during channel program execution.

• Byte 0, Bit 0 - Command Reject

Action: Check for Byte 1, Bit 5 (File Protect); in either case, take program check exit.

Messages: 0P18 COMM REJCT. 0P17 FILE PROT.

• Byte 0, Bit 6--Track Condition Check

Action:

- Read Home Address and R0 in the error recovery routine and move CCHH from R0 to Seek command executed below.
- If alternate track: update seek address to the next track address. If the track address equals ten, treat it as End of Cylinder; otherwise, proceed to step 3.
- Set up the channel program: Seek, Read Home Address (with skip bit on), TIC to CSW address minus eight. Execute this channel program in error recovery. At channel end, exit to channel scheduler CSW processing routine. If DASD file protection is present, set the appropriate file mask following Seek.
- Byte 1, Bit 1--Track Overrun

Action: Post track overrun to the CCB and take continue exit.

• Byte 1, Bit 2--End of Cylinder

Action: Post End of Cylinder to the CCB and take continue exit.

• Byte 1, Bit 5--File Protect

Action: Take program check exit.

Message: OP17 FILE PROT.

• CSW Bit 47--Chaining Check

Action: If retry count is greater than nine, take equipment error exit (cancel, retry); otherwise, take retry exit.

Message: OP14 OVERRUN.

Note: If the error routine gets an error while trying to execute a Restore command or Read Home Address or RO, equipment error exit is taken with retry and cancel options with the message: OP20 ERR ON REC (Error During Recovery).

2321 DASD ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: One retry; then take equipment error exit (cancel, retry).

Message: OP28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Take equipment error exit (cancel, retry).

Message: OP10 EQUIP CHK.

Byte 1, Bit 4--No Record Found

Action:

- If Byte 1, Bit 6 (missing Address Markers) is present, go to step 2. Otherwise, go to step 6.
- 2. If retry count is less than 3, issue a Restore command and go to step 5.
- If retry count is equal to 3, issue a Read Home Address to the first and last tracks of the cylinder. If neither is successful (unit checks), take equipment error exit (cancel, retry). Otherwise, go to step 4.
- If retry count is equal to 15, take equipment error exit (cancel, retry). Otherwise, go to step 5.
- 5. Increment retry count and take retry exit.
- Issue a Read RO and compare CCH to user's Seek Address. If equal, post No Record Found to the CCB and take continue exit. Otherwise, go to routine for Seek Check (alone).

Messages: OP15 SEEK CHECK (No Record Found/R0 unequal to Seek Address). OP23, BLNK STRIP (Step 3, cannot read Home Address). OP21 NRF - MADDMK (Step 4, 15 retries). • Byte 0, Bit 7--Seek Check

Action: If Byte 0, Bit 0 (command reject) is present, take program check exit. If Byte 1, Bit 6 (missing Address Markers) is present, take operator intervention exit. Otherwise, issue a Seek to BB1111, a Seek to BB2222, and take retry exit. After ten retries, take equipment error exit (cancel, retry).

Messages: 0P26 INVAL SEEK (Seek
Check/Command Reject).
0P22 BALST CELL (Seek Check/Missing
Address Markers).
0P15 SEEK CHECK (Seek Check alone).

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: Take retry exit. After 15, retries, take equipment error exit (cancel, retry).

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 4--Data Check

Action:

- 1. If retry count is less than eight, go to step 5.
- If retry count is equal to 226, take equipment error exit (cancel, retry).
- 3. If retry count is an even number, issue a Seek to X-X-X-4-19 (last track of strip) and a Seek to X-X-X-0-0 (first track of strip). Perform this operation eight times. Then proceed to step 4.
- 4. If retry count is any multiple of 32 (32, 64, 96, ...), issue a Seek to next lower strip. (If this is the lowest strip 00000 seek the next higher strip.) Proceed to step 5.
- Increment retry count and take retry exit.

Messages: 0P11 DATA CHECK (Data
Check/not Data Check on Count or
Verify).
0P12 VERIFY CHK (Data Check on Verify
Command).
0P16 DTA CHK CT (Data Check on Count).

Note: Home Address is read, and the track address is provided for the error message. For other conditions, the track address is obtained from the user's initial Seek Address if the error occurs during channel program execution.

• Byte 0, Bit 5--Overrun

Action: Take retry exit. After 15 retries, take equipment error exit (cancel, retry).

Message: 0P14 OVERRUN.

• Byte 1, Bit 6--Missing Address Markers

Action: Perform action indicated under Data Check just described.

Message: OP13 ADDR MRKER.

Note: Home Address is read, and the track address is provided for the error message. For other conditions, the track address is obtained from the user's initial Seek Address if the error occurs during channel program execution.

• Byte 0, Bit 0--Command Reject

Action: Check for byte 1, bit 5 (file protect); in either case, take program check exit.

Messages: 0P17 FILE PROT (Command
Reject/File Protect).
0P18 COMM REJCT (Command Reject alone).

• Byte 0, Bit 6--Track Condition Check

Action:

- 1. Read Home Address and R0 and move CCHH from R0 to Seek command executed below.
- 2. If alternate track: Update Seek Address to the next track address. If track address equals 20, treat it as End of Cylinder; otherwise, proceed to step 3.
- Read Home Address (with skip bit on), TIC to CSW command address minus eight (last CCW executed). Execute this channel program in error recovery. At channel end, exit to channel scheduler CSW processing routine. If DASD file protection is present, set file mask (inhibit long Seeks) following the seek.
- Byte 1, Bit 1--Track Overrun
 Action: Post track overrun to the CCB and take continue exit.
- Byte 1, Bit 2--End of Cylinder
 Action: Post End of Cylinder to the CCB and take continue exit.
- Byte 1, Bit 5--File Protect
 Action: Take program check exit.
 Message: 0P17 FILE PROT.
- CSW Bit 47--Chaining Check

Action: Take retry exit. After 15
retries, take equipment error exit
(cancel, retry).

Message: 0P14 OVERRUN.

Note: If the 2321 Error Routine gets an error while trying to execute a Restore command, a Seek command (data-check procedure), or a Read Home Address or a Read RO, equipment error exit is taken with retry and cancel options with the message: OP20 ERR ON REC (Error During Recovery).

1285-1287-1288 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

<u>Action</u>: One retry; then take equipment error exit (retry, cancel).

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Post byte 3 of CCB and then take continue exit.

Note: Data Check and Equipment Check, which indicate unreadable character and unreadable line, respectively, are retried by Logical IOCS in an attempt to correct the error.

• Byte 0, Bit 1--Intervention Required

Action: Test for byte 0, bit 6 (Nonrecovery)--if present, post byte 3, bit 4 of the CCB. This indicates that the error is passed back to the problem program. Exit via equipment error.

Message: 0P35 NON RECOV. If byte 0,
bit 6 is not present, take operator
intervention exit.
0P08 INTERV REQ.

• Byte 0, Bit 6--Nonrecovery

Action: Post byte 3, bit 4, of CCB and take continue exit.

• Byte 0, Bit 2--Busout Check

Action: One retry; then take equipment error exit (manual retry, cancel through ATTN routine).

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 4--Data Check

Action: Post byte 3, bit 0, of CCB and take continue exit.

Note: Data Check and Equipment Check, which indicate unreadable character and unreadable line, respectively, are retried by Logical IOCS in an attempt to correct the error.

• Byte 0, Bit 5--Overrun

Action: Four retries; then take equipment error exit (retry, cancel).

Message: OP14 OVERRUN.

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: OP18 COMM REJCT.

• CSW Bit 47--Chaining Check

Action: Four retries; then take equipment error exit (retry, cancel).

Message: 0P14 OVERRUN.

• Byte 0, Bit 7--Keyboard Correction

Action: Post byte 3, bit 1, of CCB and take continue exit.

• Byte 1, Bit 4--Invalid Font

Action: Take program check exit.

Message: 0P37 INVLD FONT.

Note: Byte 1, bit 4 applies only to the 1287 in document mode.

1412-1419 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: Post unrecoverable I/O error to CCB byte 2, bit 2. Turn on passback bit in error queue entry byte 10, bit 2 for return to user for error recovery.

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 0--Command Reject

Action: Check command code of CCW causing interrupt with X'E1' for 'Disengage Failed'. If 'Disengage Failed', post intervention required to CCB byte 3, bit 1; if not, post unrecoverable I/O error to CCB byte 2, bit 2. In either case, turn on passback in error queue entry of ERBLOC byte 10, bit 2, for return to user for error recovery.

Message: 0P18 COMM REJCT or 0P37 DISEN FAIL.

• Byte 0, Bit 1--Intervention Required

Action: Post "Intervention Required" to the CCB (byte 3, bit 1), and take IGNORE exit. No message is printed.

Message: 0P08 INTERV REQ.

Note: The problem program should process all documents in the input buffer, note the Intervention Required and perform any print out necessary for operator recovery, and issue an Engage-Read to the device to continue processing documents. If the Intervention Required is due to a batch numbering update failure, the operator must update the batch number as part of manual recovery.

• Byte 0, Bit 2--Bus Out Check

Action: Post unrecoverable I/O error to CCB byte 2, bit 2, and turn on passback bit in error queue entry of ERBLOC Byte 10, bit 2, for return to user for error recovery.

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 3--Should not occur

Action: Post Unrecoverable I/O error to the CCB and provide informational message to the operator.

Message: 0p19 UNDETR ERR

Note: CSW Bit 47 and Sense bits 4, 5, 6, and 7 will not cause an I/O Interrupt. If CSW bit 44 or sense bit 1, 2, or 3 is not present for an I/O interrupt, the action and message for sense bit 3 will be generated. LIOCS issues two informational messages through the MICR Message Writer:

- 1. 4MR1I EXTERNAL INTERRUPT I/O ERROR
- 2. 4MR2I SCU NOT OPERATIONAL
- Byte 0, Bit 7--Batch Numbering Switch Off

Action: Post document buffer byte 0, bits 0 and 1 and insert reject code X'CF' in byte 5. Turn off retry and turn on ignore bits in ERRFLG of error queue entry of ERBLOC.

Message: OP34 BCH NM OFF.

2495 ERROR RECOVERY

• CSW Bit 42--Program Check

Action: Take equipment error exit (cancel).

Message: 0P24 PROG CHECK

• CSW Bit 43--Protection Check

Action: Take equipment error exit
(cancel).

Message: 0P25 PROT CHECK

• CSW Bit 44--Channel Data Check

Action:

- Read Commands--backspace record, one retry, then take equipment error exit (cancel).
- All other commands—take equipment error exit (cancel).

Message: 0P28 CHAN DTCHK

- Byte 0, Bit 5--Should not occur
- Byte 0, Bit 7--Should not occur

Action: Take equipment error exit
(cancel).

Message: OP19 UNDETR ERR

• Byte 0, Bit 3--Equipment Check

Action: Take equipment error exit (cancel).

Message: OP10 EQUIP CHK

• Byte 0, Bit 2--Bus Out Check

Action: One retry, then take equipment error exit (cancel).

Message: 0P09 BUSOUT CHECK

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 6--Position Check

Action:

- 1. Read Commands--backspace one byte.
 Reread the remaining portion of
 the record. Repeat this sequence
 nine times for a total of ten
 rereads. On the eleventh try,
 take equipment error exit
 (cancel).
- All other commands—take equipment error exit (cancel).

Message: 0P39 POSN CHECK

• Byte 0, Bit 4--Data Check

Action: Backspace one byte. Reread the remaining portion of the record. Repeat this sequence nine times for a total of ten rereads. On the eleventh try, post data check error and set passback flag in ERBLOC if user requests return of data check errors, take equipment error exit (ignore, cancel).

Message: OP11 DATA CHECK

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: 0P18 COMM REJCT

1017/1018 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: For Read/Write Commands: If data transfer, no retry is performed. If initial selection, retry twice without repositioning. After specified number of retries has been reached, take equipment error exit (cancel).

Message: OP28 CHAN DTCHK

- CSW Bit 47--Chaining Check (Read/Write Commands).
- Byte 0, Bit 2--Bus-Out Check (Read Command during data transfer).
- Byte 0, Bit 3--Equipment Check (Read Command)
- Byte 0, Bit 4--Data-Check (Write Command if Error Correction feature not present)

- Byte 0, Bit 5--Overrun (Read/Write Commands)
- Byte 0, Bit 6--Lost Data (Read/Write Commands)
- Byte 0, Bit 7--Broken Tape (Write Command) This sense and status information is not used or may not occur for the indicated condition.

Action: Take equipment error exit
(cancel),

Message: OP19 UNDETR ERR

• Byte 0, Bit 0--Command Reject

Action: Take Program check exit.

Message: 0P18 COMM REJECT

• Byte 0, Bit 1--Intervention Required

Action: If initial selection (Read/Write Commands), take operator intervention exit. If data transfer (Write Command), update interrupted CCW and retry.

Message: 0P08 INTERV REQ

• Byte 0, Bit 2--Bus-Out Check

Action: If initial selection (Read/Write Commands), retry the operation twice. If data transfer (Write Command), update interrupted CCW and retry. If error persists, take equipment error exit (cancel).

Message: 0P09 BUSOUT CHK

 Byte 0, Bit 3--Equipment Check (Write Command)

Action: Take equipment error exit (cancel).

Message: OP10 EQUIP CHK

• Byte 0, Bit 4--Data Check

Action: If Read Command, update interrupted CCW, backspace one character and retry. If the error persists after four retries, test the CCB for the ignore option (byte 2, bit 4); if the bit is on, turn on byte 3, bit 3 of the CCB (1017/1018 data check) and take the equipment error exit (ignore, cancel). If the bit is not

on, take the equipment error exit (cancel). If Write Command, (Error Correction Feature Not Supported) byte 3, bit 3 in the CCB is set on, then if the user wants to process the data check himself (byte 2, bit 6 on in the CCB), control is returned to the user program. If the user does not want to process the data check, he must take the equipment error exit (ignore, cancel) if bit 4 of byte 2 in CCB is off.

Message: OP11 DATA CHECK

Note: When a data check occurs, the user's CCW is modified by the error routine to allow rereading or rewriting of the last character. The data address is the last character read or written (i.e., the character in error), and the byte count is decreased by the number of valid characters read or written. If the CCB ignore option is chosen and the operator responds ignore, the I/O operation is dequeued and posted with the unrecoverable error bit on (CCB byte 2, bit 2) and 1017/1018 data check bit on (CCB byte 3, bit 3). To read or write the rest of the record, the problem program (logical IOCS) adds 1 to the CCW data address and subtracts 1 from the byte count to adjust for not rereading or rewriting the bad character, and then reissues the EXCP. The ignore option is available to the operator whenever the user specifies any of the DTFPT ERROPT entry options.

 Byte 0, Bit 7--Broken Tape (Read Command)

Action: When this condition occurs, the last record has not been completely read. Turn on byte 3, bit 1 of the CCB (1017 broken tape) and take the equipment error exit (retry, ignore, cancel).

Message: 0P40 BROKEN TAPE

Note 1: When broken tape condition occurs, the operator must reposition the paper tape at the beginning of the record before responding. The 1017 must not be readied until this repositioning has been performed. If the ignore option is chosen, the I/O operation is dequeued and posted with the unrecoverable error bit on (CCB byte 2, bit 2) and the 1017 broken tape bit on (CCB byte 3, bit 1).

Note 2: A record may not be partly on one tape and partly on another.

The RMS (Recovery Mangement Support) is an automatic DOS feature for IBM System/370. RMS gathers information about hardware reliability and attempts certain error recovery operations. It is part of the entire RAS (reliability, availability, and serviceability) support for System/370.

RMS is supervisor generated and is composed of two functions:

- MCAR (Machine Check Analysis and Recovery) and
- CCH (Channel Check Handler).

However, RMS is not a supervisor option. It is generated automatically for System/370 at SYSGEN. The CONFG macro sets global BG39 when MODEL option shows a System/370 CPU. Figure 54 gives the overview of the RMS function in DOS.

MCAR FUNCTION

MCAR responds to machine check interrupts and attempts recovery. It logs error data on ERDS (Environmental Recording Data Set) on the Recorder File. It provides operator messages via SYSLOG.

When a machine check occurs, MCAR first logs the error, then retries the failure by CPU retry and ECC (Error Correction Code). If successful, a <u>soft MCI</u> (machine check interrupt) message occurs, signifying recovery from a machine check.

If hardware retry is unsuccessful, MCAR determines machine check severity through recovery transient analysis and records pertinent data on SYSREC. RMS controls the recording of data through the EFL (Error

Frequency Limit) feature of operating in Quiet or Recording mode. See the MODE Command section.

Hard MCI occurs when:

- CPU retry is unsuccessful, or
- Interrupted instruction cannot be retried, or
- Storage failure is permanent.

In event of a hard MCI, execution of the affected task stops. MCAR assesses damage and continues system operation when possible. It selectively terminates the affected partition. RMS records a full Damage Report on the Recorder File.

The system enters the hard wait state when a hard MCI:

- Interrupts supervisor coding
- Occurs while accessing critical information or phases from SYSRES, or
- Damages privileged coding through permanent storage error

MCAR attempts to notify the operator about:

- 1. Machine check type
- 2. Wait state, re-IPL
- Problem program termination
- 4. MODE operation change
- 5. Buffer deletion

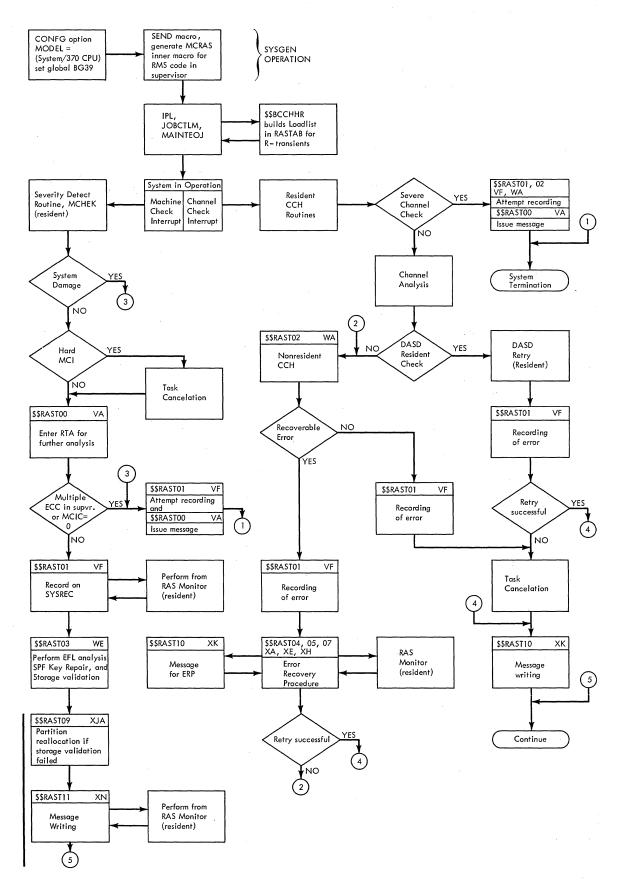


Figure 54. RMS Generation and Operation

CCH FUNCTION

The Channel Check Handler responds to channel error conditions. It first logs the error. Then, it evaluates the damage and attempts to decrease the impact on the entire system.

CCH assesses channel control checks and interface control checks to determine if the system can continue. Figure 55 shows the results of the Channel Check Severity Routine. Resident CCH performs severity analysis, records errors on SYSREC (see Figure 56 for the format of System/370 machine check records and Figure 57 for the format of System/370 channel check records), and builds an ERPIB (Error Recovery Procedure Interface Byte) entry.

Resident CCH coding performs no recovery action, but fetches the proper recovery transient to attempt restoration of system operation. Recovery transients operate under control of the RAS Monitor.

Figure 58 shows the devices supported with ERP by CCH routines and the action taken for each condition.

System termination results when:

- Hard channel error occurs on accessing critical information or phases from SYSRES
- System reset has occurred
- Channel address or reset codes are invalid
- Two channels are damaged simultaneously, or
- Four system ERPIBs are exhausted

RAS MONITOR AND R-TRANSIENTS

The RAS Monitor is a resident control program with which RMS (MCAR/CCH functions) controls the RTA. At DOS system generation for System/370, the RAS Monitor forms a portion of the resident supervisor. The RAS Monitor and RMS coding are generated

when the SYSGEN option MODEL=a System/370 CPU. That MODEL option turns on macro global BG39, generating RMS support.

The RAS Monitor:

- 1. Fetches R-transients into the RTA
- 2. Schedules I/O requests from the RTA
- Accepts RTA I/O request complete postings from CCH, and
- Provides exit interface from R-transients.

The R-transients (or recovery transients) are nonresident RMS ERPs (error recovery procedures). The transients are listed in order of descending priority in Figure 59 and in the load list portion (bytes 0-47) of the RMS table. Refer to Figure 60, RASTAB. The R-transient with the highest priority is activated wherever multiple transients are selected for the RTA.

R-transients perform channel check ERP and differ from A-transients, which still perform channel data check recovery.
R-transients operate on channel control checks and channel interface checks. They attempt to retry the operation, or terminate the affected partition, while trying to permit continued system activity. See Figure 61 for the recovery transient error messages.

MODE COMMAND

The MODE command gives the operator control of soft machine check interrupts. It permits the operator three options:

- Determine whether the system is in quiet or recording mode
- 2. Alter mode of operation
- 3. Change error threshold values

By the mode command, the operator can change machine check logging and can receive status reports about the system.

Channel Check Severity Detect Routine (Part 1):

Channel Address Valid	Reset Codes Valid	System Reset Code On	Start I/O Time	Unit Address Valid	RTA I/O Active	SYSRES Channel	Action Taken
No							1,2
Yes	No						1,2
Yes	Yes	Yes					1,2
Yes	Yes	No	Yes				5
Yes	Yes	No	No	No	No	No	1,3
Yes	Yes	No	No	No	Yes		1,2
Yes	Yes	No	No	No	No	Yes	1,3,4,5
Yes	Yes	No	No	Yes			5

ACTION CODES

- 1. Schedule recording.
- 2. Schedule system termination with proper message.
- 3. Set the damaged channel byte for non-resident channel check handler.
- 4. Assume the error is on SYSRES device.
- 5. Error can be isolated to a device, use Part 2.

Note: Every Channel Check that occurs in the system is passed through the Channel Check Severity Detect Routine. You can determine the disposition of the check by using part 1. When a Channel Check has been isolated to a device, use part 2 to determine the action taken.

Channel Check Device Isolation Results (Part 2):

No No 6 No Yes 7 Yes No No 8
Yes No No No 8
Yes No No Yes 6,9,10
Yes No Yes 6
Yes Yes No No 8
Yes Yes No Yes 8,9,10
Yes Yes Yes 11

ACTION CODES

- 6. Exit to supervisor I/O routine after other functions performed.
- 7. Find a free ERPIB in queue and fill with information for ERPs.
- 8. Exit to task selection after other functions performed.
- 9. Post ERPIB complete.
- 10. Dequeue the RAS CCB and requeue the users CCB.
- 11. Exit to DASD channel check handler.

Figure 55. Channel Check Severity Routine Results

Record 1	Machine Check ID (X'10')	1 – 2 Record Sequence Counter	3 CPU Model Number	Reserved	5 - 7 CPU Serial	8-9 CPU ID	10-11 MCEL Length	12 - 15 Date	16–19 Time of day in 300ths of a second Timer units	20 - 27 Reserved	28 - 35 Job ID	36 – 43 Machine Check Old PSW	1	7 erved	78 Damage Assessment	79 End of Record Indicator (X'FF')
Record 2	0 – 3 (Same as Ri	ecord 1)		4 Sub Class Codes	5 Tense Codes	6– 7 Error and Validity Codes	8-11 Extende Logout Length	12 – 19 Reserv		24 – 25 Region Co ECC Informatio	Cont	on Code rol Word	28 - 78	Reserve	d	79 (Same as Record 1)
Record 3	0 – 3 (Same as R	ecord 1)		4 - 48 Reserved								1	9-78 loating	Point Reg	ister Area	79 (Same as Record 1)
Record 4	0-3 (Same as R	ecord 1)		4–5 Floating F Area (Con		Save Ger	9 neral Regis	iters Save	e Area			L		70 – 78 Control Save A	Registers rea	79 (Same as Record 1)
Record 5	0-3 (Same as Re	ecord 1)		4-58 Control Re	egisters Sa	ve Area		÷			59 - 7 MCE	78 L (Machir	ne Checl	« Extende	d Logout)	79 (Same as Record 1)
Record 6-17	0 – 3 (Same as Re	ecord 1)		4-78 MCEL (Ma	ichine Che	eck Extend	ed Logout)								79 (Same as Record 1)
Record 18	0 – 3 (Same as Re	ecord 1)		4 - 75 MCEL (Ma	ichine Che	eck Extend	ed Logout)							76 – 78 Reserved X'000000')	79 (Same as Record 1)

* Note: The Model 155 uses Records 1 – 18, as shown. The Model 145 uses only Records 1 – 8. In Record 8 for the Model 145, Bytes 0 – 3 are the same as Record 1, Bytes 4 – 25 contain the remainder of the MCEL (Machine Check Extended Logout) area, and the remainder of the record is not used.

•	1		ł	1		1	1	ŀ	1	1	-
Label	CCKEY	CCNI	CCN2	CCMOD	CCCPUID	CCDATE	CCTIME	CCNAM	E CCAI	ou c	CFCCW
Record 1 *	Record ID	Record Number	Total Records	CPU Model Code	CPU ID Information	Date	Time of Day	Job Name	Activ 1/0 I		Failing CCW
,											
Displacement	52 - 59		60 - 63		64 - 65	66	67 - 69	70 - 73	74 - 77	78	79
Label	C	ccsw	CC	CECSW	CCDEVTYP	CCCHID	CCCUA	ССМРІ		CCSYSCO	CCGUAR
Record 1 (continued)		CSW	Ex CC	tended CW	Device Type	Channel ID	Control Unit	Multi – processing Information	Reserved	System Condition Byte	Guard Byte X'FF'
Displacement	0-3		4 - 78								79
Record 2	Same a	s Record				C	hannel Logout A	Area			Same as Record 1
											<u>.</u>
Displacement	0-3		4-24			25 - 78					79
Record 3	Same a	s Record		Channel	Logout Area			Unused			Same as Record 1
		essed sym	bolically		with the logout o	lata area,					

| 4- 11 | 12- 15 | 16- 19 | 20- 27 | 28- 43 | 44- 51

Figure 57. RMS Channel Check Record on SYSREC

Displacement

1403 AND 1443 Printers

	Sequence Code									
000	001	010	011	100	101	110	111			
2 2 2 2	5 5 5 5	5 3 5 3	3 3 5 3	5 5 5 5	3 3 5 3	2 2 2 2	3 3 5 3			
	2 2 2 2 2	000 001 2 5 2 5 2 5 2 5 2 5	000 001 010 2 5 5 2 5 3 2 5 5 2 5 3 2 5 3	000 001 010 011 2 5 5 3 2 5 3 3 2 5 5 5 2 5 3 3	000 001 010 011 100 2 5 5 3 5 2 5 3 3 5 2 5 5 5 5 2 5 3 3 5 2 5 3 3 5	000 001 010 011 100 101 2 5 5 3 5 3 2 5 3 3 5 3 2 5 5 5 5 5 2 5 3 3 5 3 2 5 3 3 5 3	000 001 010 011 100 101 110 2 5 5 3 5 3 2 2 5 3 3 5 3 2 2 5 5 5 5 5 2 2 5 3 3 5 3 2			

2520 Card Read Punch

Operation	Termination Code*				Sequence	e Code			
		000	001	010	011	100	101	110	111
Sense	00 01 10 11	2 2 2 2	5 2 5 5	5 5 5 5	5 5 5 5	5 2 5 5	5 5 5 5	2 2 2 2	5 5 5 5
Read/Control	00 01 10 11	2 2 2 2	5 2 5 5	4 4 4 4	4 4 4 4	5 2 5 5	4 4 4 4	2 2 2 2 2	4 4 4 4
Write/Control	00 01 10 11	2 2 2 2 2	5 2 5 5	4 4 5 5	4 4 5 5	5 2 5 5	4 4 5 5	2 2 2 2	4 4 5 5
Write, No Control	00 01 10 11	2 2 2 2	5 2 5 5	3 3 5 5	3 3 5 5	5 2 5 5	3 3 5 5	2 2 2 2 2	3 3 5 5
Immediate	00 01 10 11	2 2 2 2	5 2 5 5	2 2 2 2	2 2 2 2	5 2 5 5	2 2 2 2	2 2 2 2	5 2 5 5

1442 Card Read Punch

Operation	Termination Code*		Sequence Code										
		000	001	010	011	100	101	110	111				
Sense	00 01 10 11	2 2 2 2 2	5 2 5 5	5 5 3 3	5 5 3 3	5 2 5 5	5 5 3 3	2 2 2 2	5 5 3 3				
Read/Control	00 01 10 11	2 2 2 2 2	5 2 5 5	3 3 3 3	3 3 3 3	5 2 5 5	3 3 3 3	2 2 2 2 2	3 3 3 3				
Write/Control	00 01 10 11	2 2 2 2 2	5 2 5 5	3 3 3 3	3 3 3 3	5 2 5 5	3 3 3 3	2 2 2 2	3 3 3 3				

Note: This Figure shows individual errors for each device supported by CCH and the action taken for each condition. The Action Codes are explained at the end.

Figure 58. Error Recovery Procedures for CCH-Supported Devices (Part 1 of 2)

2501 Card Reader

Operation	Termination Code*	Sequence Code								
		000	001	010	011	100	101	110	111	
Read	00 01 10 11	2 2 . 2 . 2	5 2 5 5	4 4 4 4	4 2 4 4	5 2 5 5	4 4 4 4	2 2 2 2 2	4 4 4 4	
Sense	00 01 10 11	2 2 2 2 2	5 2 5 5	5 5 5 5	5 5 5 5	5 2 5 5	5 5 5 5	2 2 2 2	5 5 5 5	

2540 Card Read Punch

Operation	Termination Code*	Sequence Code									
		000	001	010	011	100	101	110	111		
Read-Feed-SS		2	5	3	4	5	3	2	3		
Read		2	4	4	4	4	4	2	4		
Feed-SS		2	4	3	2	4	2	2	3		
Punch-Feed-SS		2	5	3	4	5	3	2	3		

3210 and 3215 Console Printer-Keyboard

Operation	Termination Code*	Sequence Code										
		000	001	010	011	100	101	110	111			
Read Write, CR Write, No CR		2 2 2	5 5 5	5 5 5	3 3 3	5 5 5	3 3 3	2 2 2	3 3 3			
No Op Alarm	·	2 2	5 5	5 5	5 5	5 5	5 5	2 2	5 5			

DASD Devices 2311, 2314, 2319, 2321

These devices are retryable for all conditions of Retry Code and Termination Code by restarting the CCW list from the beginning (from the initial SEEK, SET FILE MASK, etc.). Ten attempts are made at retry of DASD Channel Errors.

Note: Recovery (\$\$R) transients are not invoked to act on all termination codes shown. Termination code 11 (system reset code) is handled by resident RMS routines. This termination code is shown primarily for reference purposes.

ACTION CODES

- Action 1. The channel is damaged and the channel user will be canceled unless he accepts unrecoverable I/O errors. If specified, control returns to the damaged channel user for further analysis. If the channel user is to be canceled due to a non-retryable or unrecoverable channel failure, the CCH ERP restores the Channel Queue Pointer and Channel Scheduler Flags in the PUB if required. It flags the ERPIB with a cancel code (X'FD'), saves CSW and CCW information for the user, and then returns to the CCH. The CCH then cancels the failing channel user.
- Action 2. Action 1 is taken followed by the CCH ERP.
- Action 3. This is a non-retryable condition. An operator message is issued by the CCH ERP, and Action 1 follows.
- Action 4. With this condition, retry is possible with manual repositioning by the operator. The CCH ERP issues an operator message and waits for a response to retry the operation (reoccurrence of this error during the retry causes Action 1).
- Action 5. This condition indicates the failing CCW can be retried. The CCH ERP identifies the failing CCW chain. If the failure reoccurs during the retry operation, an operator message is issued and Action 1 follows.

Figure 58. Error Recovery Procedures for CCH-Supported Devices (Part 2 of 2)

R-Transients	Charts	Function
\$\$RAST00	VA	MCAR analysis / CCH data gatherer
\$\$RAST01	VF	MCAR / CCH recording
\$\$RAST02	WA	CCH ERP scheduling
\$\$RAST03	WE	MCAR repair (error frequency unit)
\$\$RAST04	XA	Unit record CCH ERP
\$\$RAST05	XE	Unit record CCH ERP
\$\$RAST06		Reserved
\$\$RAST07	ХН	Tape CCH ERP
\$\$RAST08		Reserved
 \$\$RAST09 	ХJА	Partition reallocation
 \$\$RAST10 	XK	Message writer for ERPs.
\$\$RAST11	XN	Message writer

Figure 59. Load List of R-transients

0	4	8	12		16		20		24		28	32
LD00SLOT	LD01SLOT	LD02SLOT	LDO	3SLOT	LD04	SLOT	LD05SL	ОТ	LD06SLO	T	LD07SLOT	LD08SLOT
(\$\$RASTOO)	(\$\$RAST01)	(\$\$RAST02)	(\$\$F	RAST03)	(\$\$RA	ST04)	(\$\$RAS1	Γ05)	(\$\$RASTO	6)	(\$\$RAST07)	(\$\$RAST08)
1 2	3	5		5	(5	5			5		5	5
36	40	44	48		50		52		54		56	57
LD09SLOT	LD10SLOT	LD11SLOT	R.A	\SCCB	RASTI	В					RASCCBF	
(\$\$RAST09)	(\$\$RAST10)	(\$\$RAST11)	1	sidual			CCW Status		SYSRES LUB		RAS CCB	RAS Fetch
5	4	5				information		bytes			indicator	CCWs address
60	64	72	80	88 96 103		104	106					
	RASCCWS	RASRCG	RA	STIC	RASRE	READ RASEEK RTAOWN MCPIK		MCPIK	RTAID			
CCW stored address	RAS seek CCW	RAS search CCW	TIC	CCW	CCW f module RTA	o read e into	Seek Addres	ss	load list for in		PIK of task interrupted by machine chec	
107	108	112	116		120		124		128		132	136
ERPID	RASRETR	RASIOA	RASF	CHA	ERPIB4		RASDEC	AΩ	XCANRAS	A	CCENTADR	RASRES
WTOR request return load index	RTA return address after I/O operation	RAS I/O request address		est address address routine routine Check		Channel Check entry address	SYSRES I/O address					
138	140	142	L	144	<u> </u>	148	<u> </u>	156	I	160		164
RASREC	RASLOG	RASEMI	OA	RASCG	DSP	SUPF	RETR	SUF	РВВ	SI	UPBC	SUPBD
SYSREC I/O address	SYSLOG device address	Emergen SIO address	су	CCB lo routine address	•		area egisters 110	(X'	e address 1000') for ervisor	()	ase address K'2000') for opervisor	Base address (X'3000') for supervisor
168 (HIR - Hara	lware Instruction	Retry accumulator	·s)	<u> </u>		180 (EG	CMAIN -	Mains	storage error	accui	mulators)	
168	170	172		176		180		182		184		188
HIRACNT	HIRICNT	HIRITIME		HIRLTIM	Е	ECMA	CNT	EC	MLCNT	Е	CMITME	ECMLTME
HIR accumulated count	Count threshold value	Time of da first error of group	y for	Time throin clock		ECC o	nulated count for storage	thi	ount reshold lue	fo	ime of day or first error f count	Time threshold in clock units
192	194	196		197		198		199		200		201
RESTARTA	RESTARTP	MCMOD	E	BUFD	EL	RAS	MSG1	RA	SMSG2	E	OR	EOT
Disk restart address	PUB address of unit to be restarted	for mach		Count buffer delete	rs		byte 1	Mess	sage byte 2		ecords/track or SYSREC	Tracks/cylinder for SYSREC

Figure 60. RAS Monitor Table (RASTAB) (Part 1 of 2)

Notes: (1)Areas labeled LDxxSLOT (bytes 0 - 47) are called the Load List and each of the 12 entries are formatted as follows: BYTE 2 3 Flag Cylinder - Head Record (disk address of R-transient in the Byte core image directory) LD00SLOT flag byte: <u>Bi</u>t 0 Flag X'80' Description \$\$RAST00 module activated. X'40' Machine check analysis to be performed. 2 X'20 Channel check analysis to be performed. 3 X'10' Active I/O units are valid. X'08' System termination situation. 5 X'04 Reserved. X'02' 6 Reserved. X'01' Attempt made to record in system termination situation. LD01SLOT flag byte: <u>Bit</u> 0 Flag X'80' Description \$\$RAST01 module activated. X'40' Build and record channel check records. 1 2-7 Reserved. LD10SLOT flag byte: Flag Description \$\$RAST10 module activated. X'40' Refetch calling module after issuing message. Reserved. LDxxSLOT flag byte: Flag X'80' 0 \$\$RASTxx module activated; that is , should be fetched. 1-7 Reserved. RASMSG1: Flag Description <u>Bit</u> 0-3 Reserved. X'08' Timer damage. X'04' 5 ECC in Quiet mode. 6 7 X'02' Reserved. X'01' MCAR repair failed. RASMS G2: Description Check damage. Flag X'80' Bit 0 Last track on SYSREC. C40 buffer pages deleted. X'40'

Figure 60. RAS Monitor Table (RASTAB) (Part 2 of 2)

Soft machine checks disabled. ECC MCI disabled.

Error on SYSREC at BBCCHHR.

SYSREC full-run EREP.

Soft machine check.

2

5

X'20' X'10'

X'08'

X'04'

X'02'

X'01'

Message <u>Code</u>	Initiating <u>Phase</u> 	Error Message
01251	\$\$IPLRT2,4 (Note 3)	No RAS support for this model CPU.
0P13A	\$\$RAST10	Invalid response.
0P81I	\$\$BEOJ2A (Note 2)	Job XXXXXXXX canceled due to CPU failure.
0P82I	\$\$BEOJ2A (Note 2)	Job XXXXXXXX canceled due to channel failure.
0T001	\$\$RAST01,11	Last track on Recorder File.
0 T 03I	\$\$RAST01,11	Error on Recorder File at CCHHR.
0T05I	\$\$RAST01,11	Recorder File fullrun EREP.
0T06I	\$\$RAST03,11	ECC main storage MCI disabled.
0T07I	\$\$RAST03,11	All soft machine checks disabled.
180T0	\$\$RAST03,11	C40 buffer pages deleted = XXX.
0T09I	\$\$RAST03,11	Soft machine check.
0T10I	\$\$RAST04,5,7,10	Channel error recovery on cuu.
0T11I	\$\$RAST00,01	Hard wait, Code = X. (Note 1) Run EREP. Recording successful. Run EREP. Recording incomplete. Run SEREP. Recording unsuccessful.
0 T12 I	\$\$RAST04,5,7,10	Unrecoverable channel errors on cuu.
0 T13A	\$\$RAST04,5,7,10	Channel error on cuu.
OT14I	\$\$RAST03,11	Check damage. All modes quiet.
0 T15 I	\$\$RAST09	MCAR repair failed.
0 T16I	\$\$RAST03,11	EFL overflow.
0 T17 I	\$\$RAST03,11	Control storage ECC in quiet mode.
0T18I	\$\$RAST01	Timer damage.

Figure 61. RMS Error Messages (Part 1 of 2)

Message <u>Code</u>	Initiating <u>Phase</u> 	Error Message
0T19I	\$\$RAST09	(Lower, Upper) boundary of XX is DDDDDD, length is LLLK.
0T20I	\$\$RAST09	XX not usable.
11931	\$JOBCTLM (Note 3)	Recorder File is XXX% full. Run EREP.

Note 1: Hard wait has resulted due to system failure explained in the code X, where E ERPIB exhausted

X = A Unrecoverable machine check

B RAS fetch error

F Two channels damaged or RTA I/O active

C SYSLOG channel check while printing RMS message

G Reserved H Reserved

D No ECSW stored

I Invalid channel address on channel error

Note 2: For this phase, refer to the Logical Transients PLM, listed in Preface.

Note 3: For this phase, refer to the IPL and Job Control PLM, listed in Preface.

Figure 61. RMS Error Messages (Part 2 of 2)

RΑ	5	1	N	K

0 (Decimal Displacement)	8	9	10	11	12	16
CPUID	RASDMC	RASFLAGS	MCFLAGS	RASMODEL	RASTABA	RASBASE
CPU ID field	Damaged Channel byte	RAS flag byte	Machine Check flags	CPU Model	RAS Table (RASTAB) address	Base address for RAS Monitor
XXXXXXX	Х	Х	Х	Х	xxxx	xxxx

Key to RAS Linkage Area displacements:

itey io	Rey 10 10 to Emiliage 7 feet displacements.						
0	CPU ID field.						
8	Address of damaged channel, or X'FF' if no channel damaged.						
9	RAS Flag byte:	<u>bit</u>	flag	description			
		0 1 2 3 4 5 6 7	X'80' X'40' X'20' X'10' X'08' X'04' X'02' X'01'	RAS active RAS SIO flag RTA in control RAS I/O delayed Channel check on error SIO Reserved Channel check on SIO I/O active for SIO			
10	Machine Check Flags:	bit 0-4 5 6 7	<u>flag</u> X'04' X'02' X'01'	description Reserved Hard machine check All machine records built All channel check records built			
11 12 16	Largest CPU Model. Address of RAS Table (RASTAB). Address used for base register in RAS Monitor Program.						

Figure 62. RMS Linkage Area (RASLINK)

Chart 01. Supervisor General Entry, General Exit, and Processor Exit

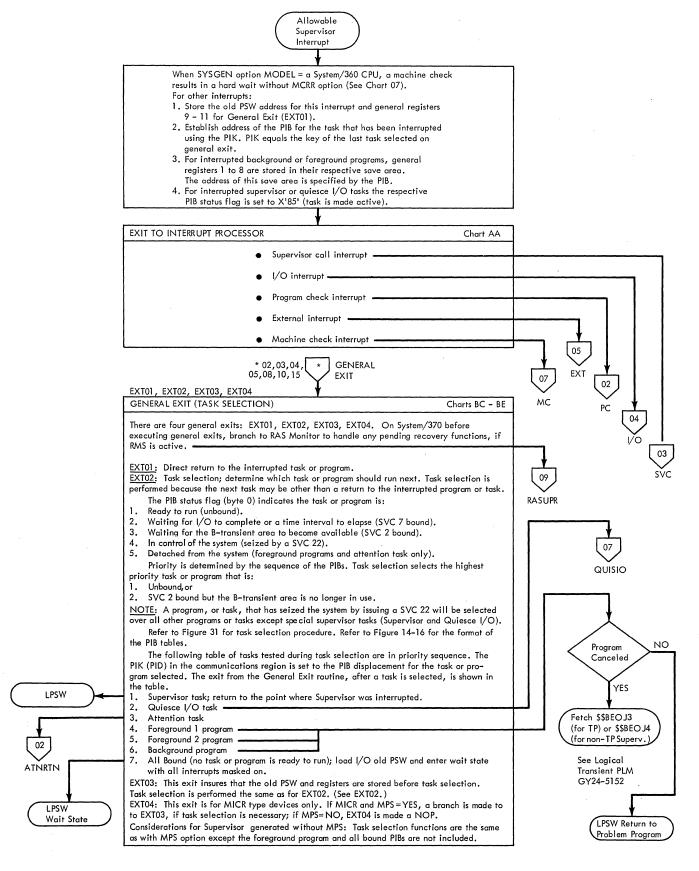
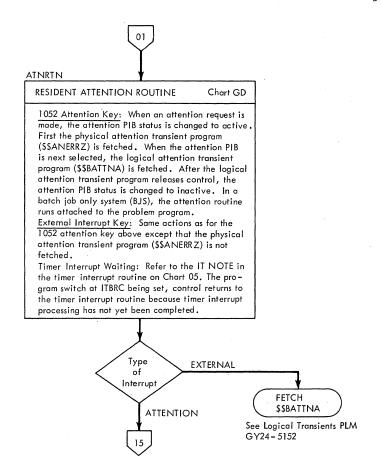
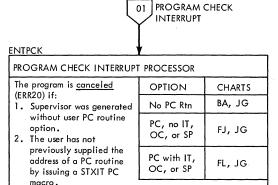


Chart 02. Resident Attention Routine and Program Check Interrupt Routine



\$\$ANERRZ



- 3. The user has specified an invalid save area.
- 4. The program check occurs while a B-Transient is in operation.
- The program check occurs while the user's PC routine is in operation (routine in use).

To exit to the user's PC routine:

- 1. Save the PC old PSW and problem program general registers in the user-supplied save area (72 bytes).
- 2. Store the address of the user PC routine in the PC old PSW.
- Branch to general exit EXT03 (EXT04 for MICR).
 The user's PC routine will be executed when this task is selected in the general exit routine. Return from the user's PC routine must be with an EXIT PC macro.

 See Figure 13 for PC option tables.

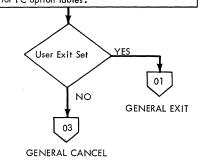


Chart 03. SVC Interrupt Processor, General Cancel, and Fetch

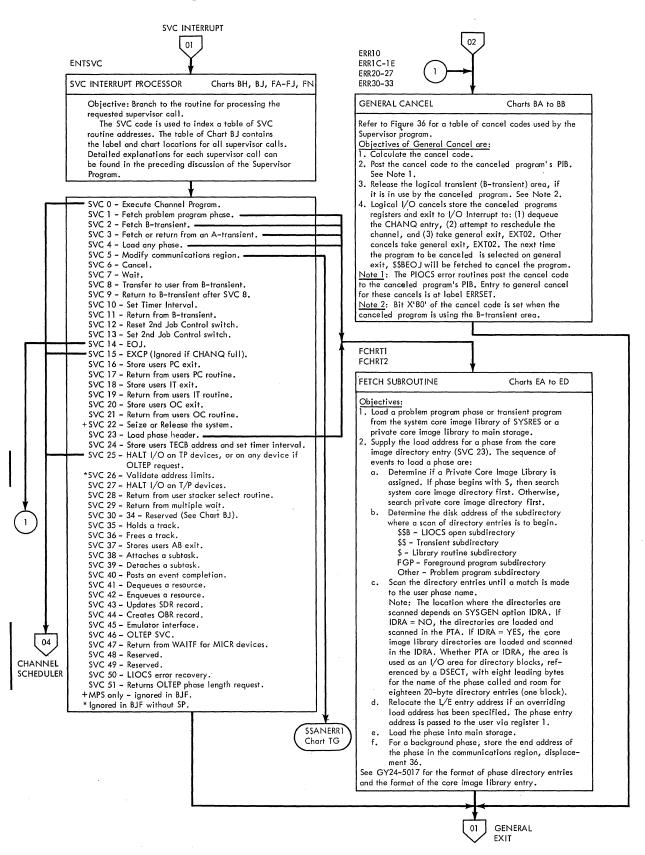


Chart 04. I/O Interrupt Processor and Channel Scheduler

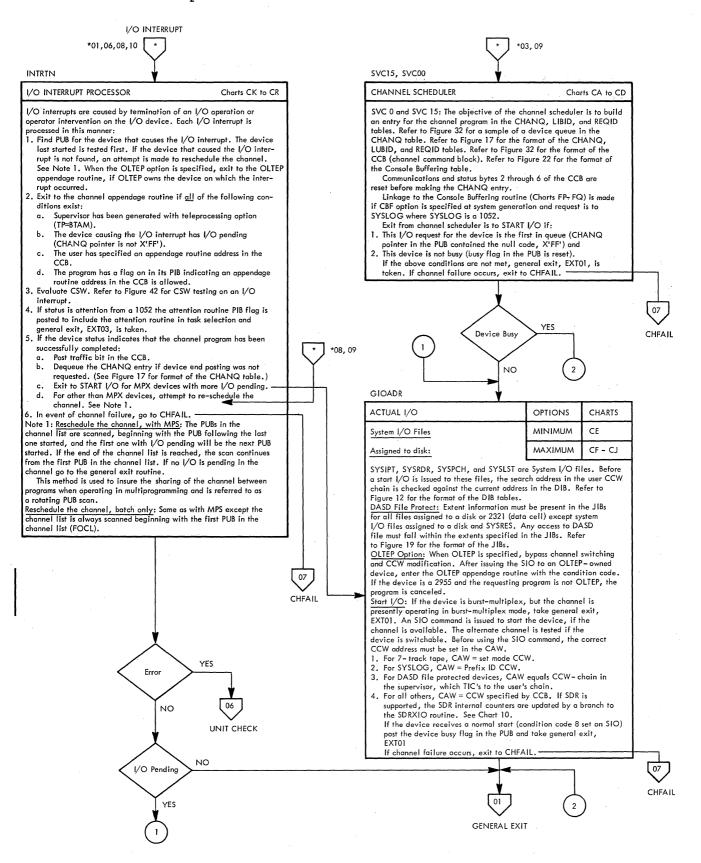


Chart 05. External Interrupt Routines

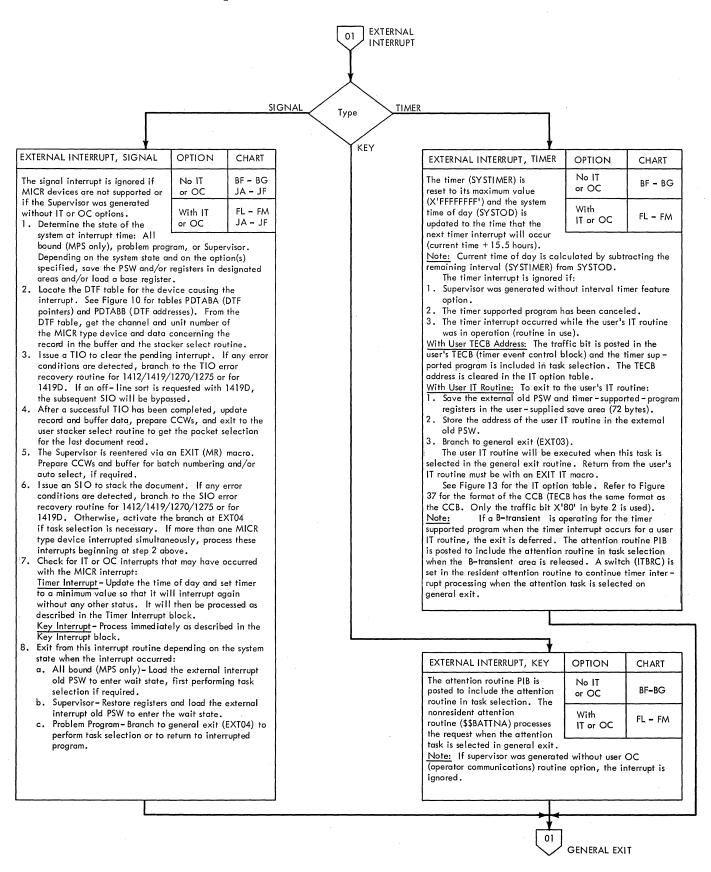


Chart 06. Unit Check and Resident ERP Routines

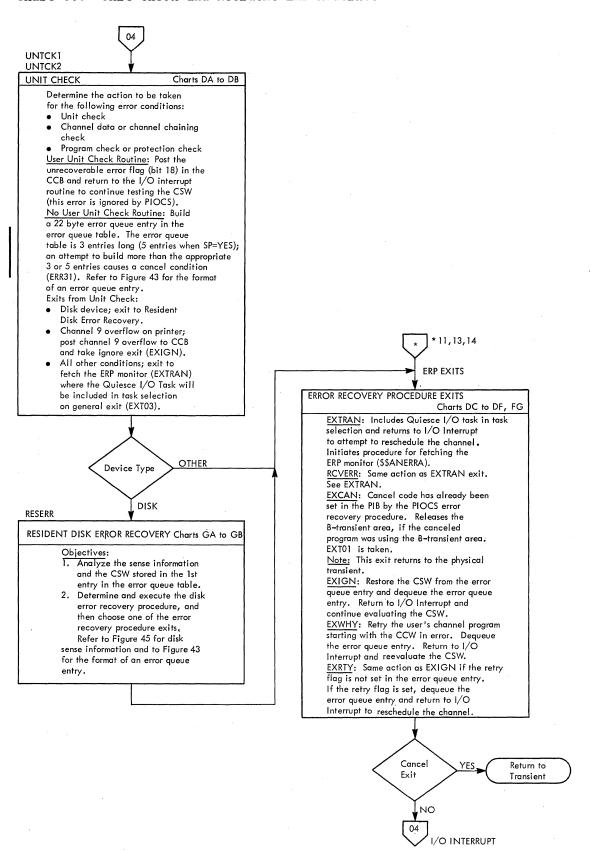


Chart 07. Quiesce I/O, Channel Failure, and Machine Check Interrupt Routines

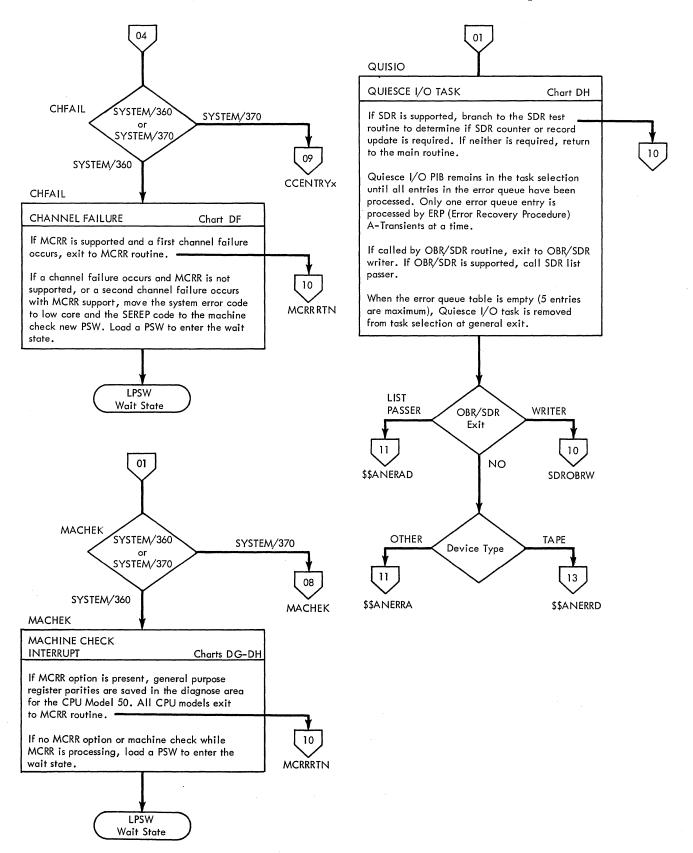


Chart 08. RMS Resident Machine Check Handler

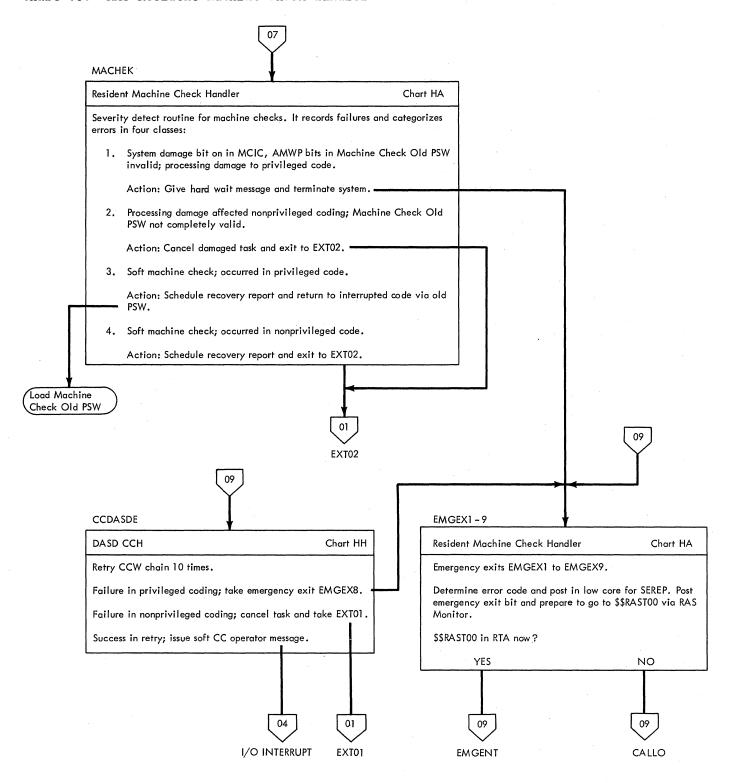


Chart 09. RMS Resident Channel Check Handler and RAS Monitor

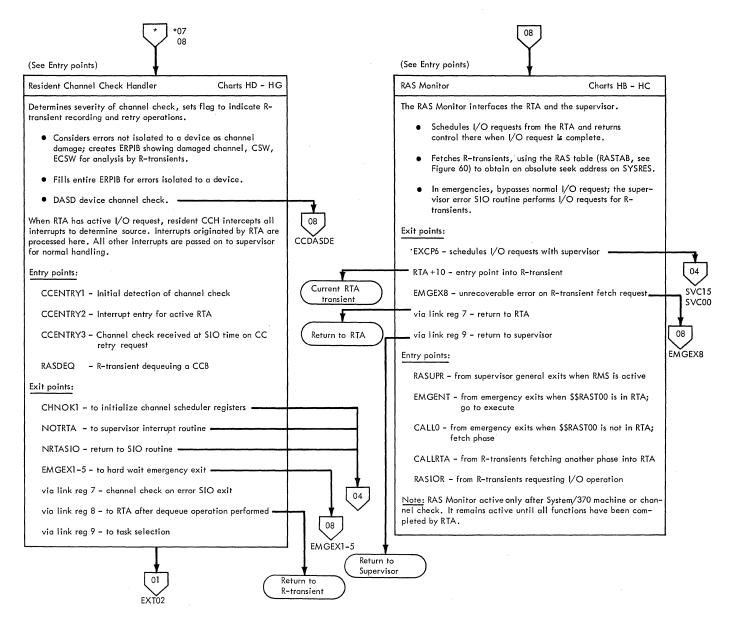
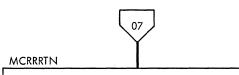


Chart 10. MCRR and OBR/SDR Routines



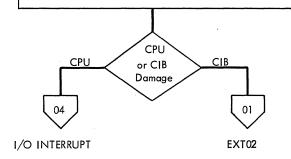
MCRR Routines

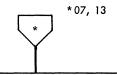
Charts KA to KJ

CHNERROR - Builds a model dependent channel inboard error record, cancels the damaged task and exits to the record writer routine.

MCREND02 - Writes the CIB record and exits to general cancel if the supervisor is the damaged task. MCRRCPU - Builds and writes the records for CPU failure and cancels the damaged tasks.

MCRECOVR - Readies the system for the next machine check interrupt and, of channel damage, goes to general exit. If CPU damage, exits to I/O interrupt.





OBR/SDR UPDATE ROUTINES

Charts LA to LG

SDRMM - Entered from OBR/SDR A - Transients as interface to system writer (\$\$ANERAB) TP transient (\$\$ANERAH), task selection or if MCRR write request, as return to MCRR routine.

SDRXIO - Schedules SDR update of internal counters after a start I/O sequence.

SDR2QT - Tests SDR error queue, exits to proper SDR update routine or returns to quiesce I/O routine. SDR2 - Updates SDR half - byte counters based upon accumulated error conditions and schedules recorder file update.

SDR23 - Gathers in a common area SDR record update information and calls SDR writer (\$\$ANERAC). SDR1 - Uses the SDR list passed by resident ERP to accumulate errors.

SDROBRW - Calls SDR writer (\$\$ANERAC) or OBR/ MCRR writer (\$\$ANERAA).

SDROBR, SDRSDR - A routine to gather in a common area information required to update an OBR/SDR record as a result of an SVC43 or SVC44. Exits to general exit. See Supervisor Call Interrupt (SVC) section.

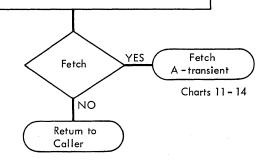


Chart 11. Physical Transients (Part 1 of 4)

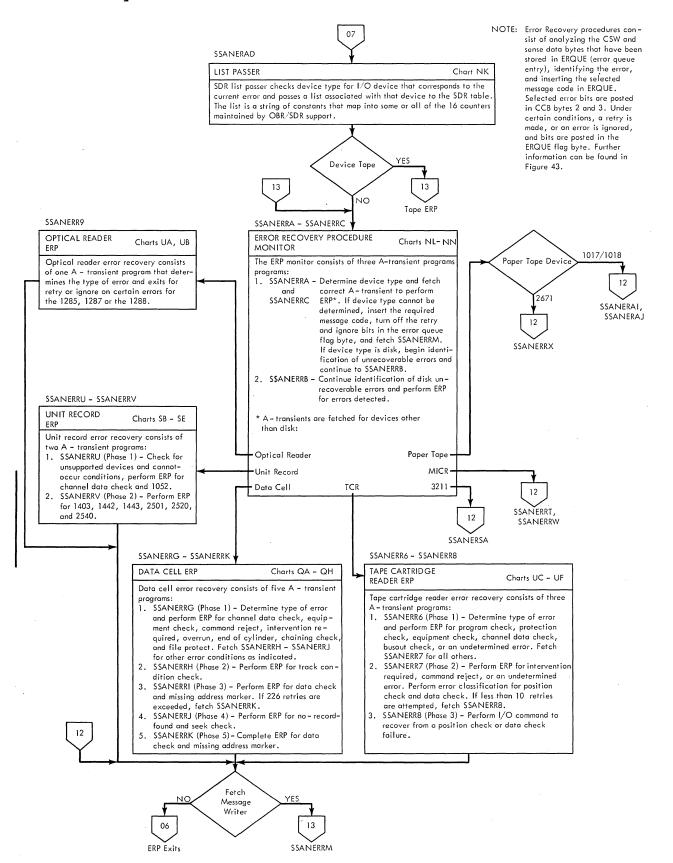


Chart 12. Physical Transients (Part 2 of 4)

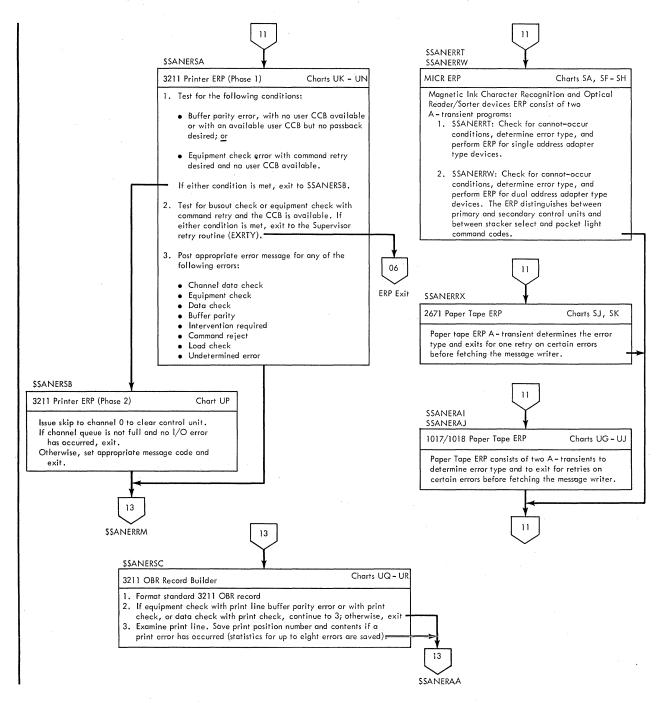
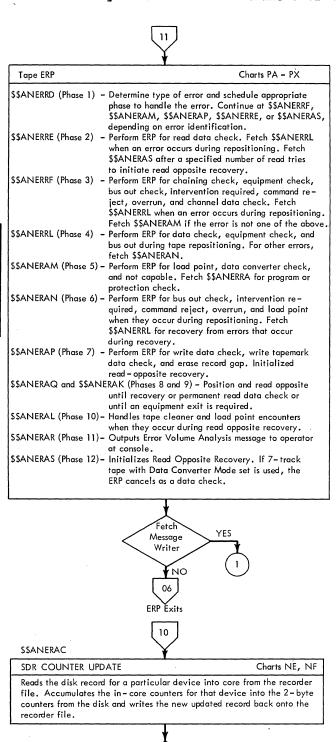


Chart 13. Physical Transients (Part 3 of 4)



Érror While Recording

10

SDRMM

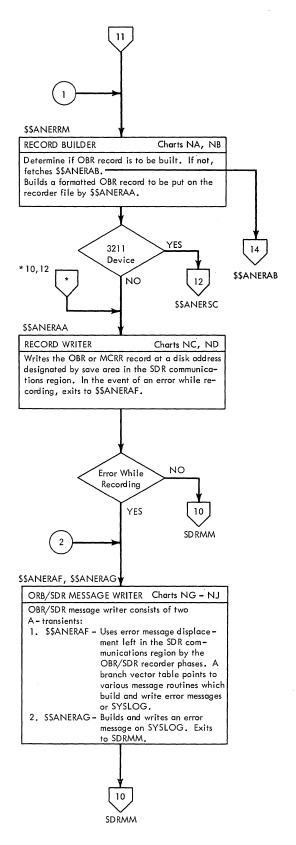


Chart 14. Physical Transients (Part 4 of 4)

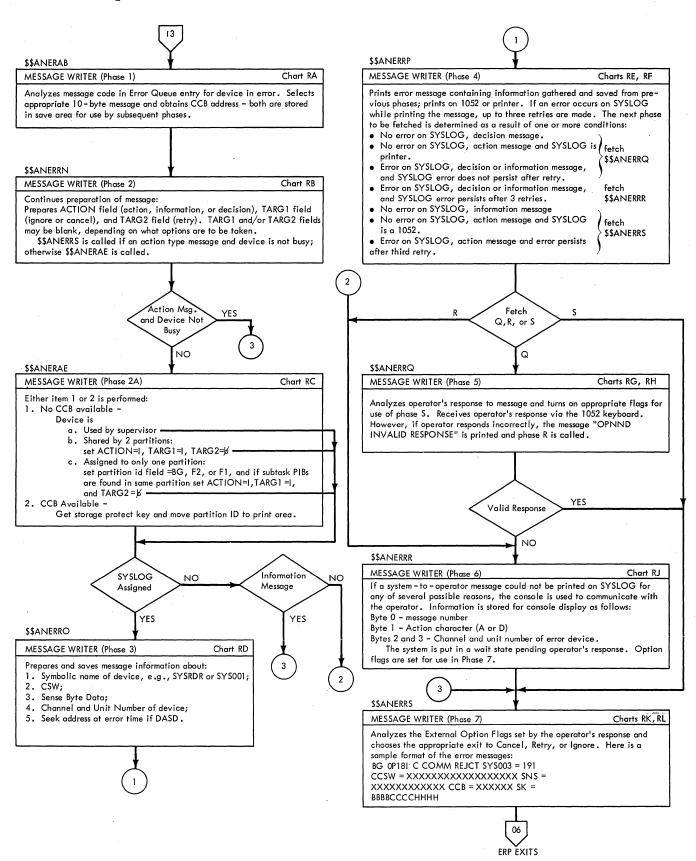


Chart 15. Physical Attention Transients

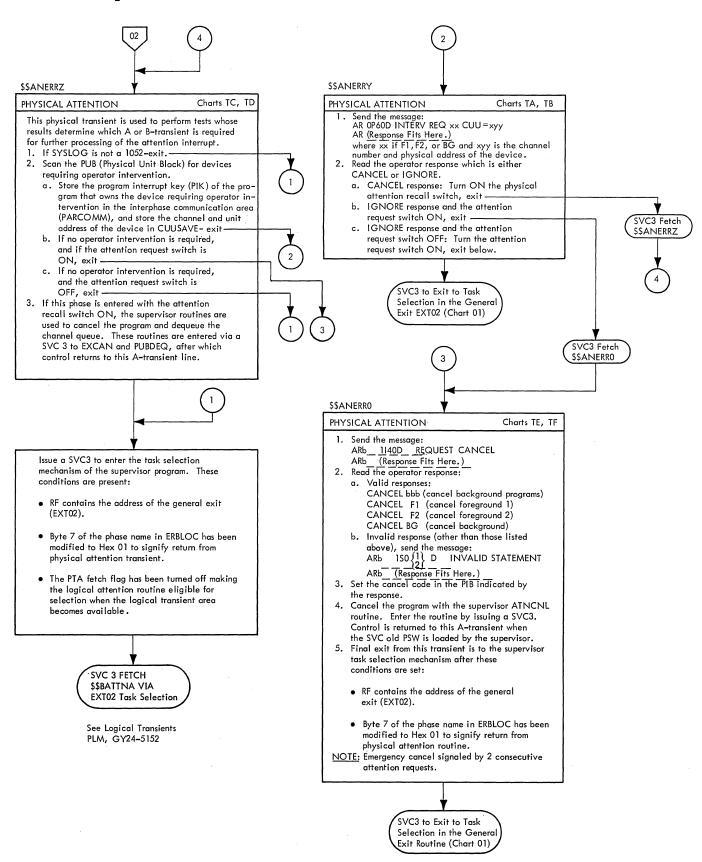


Chart AA. \$\$A\$SUP1 - SUPVR Macro, General Entry Refer to Chart 01.

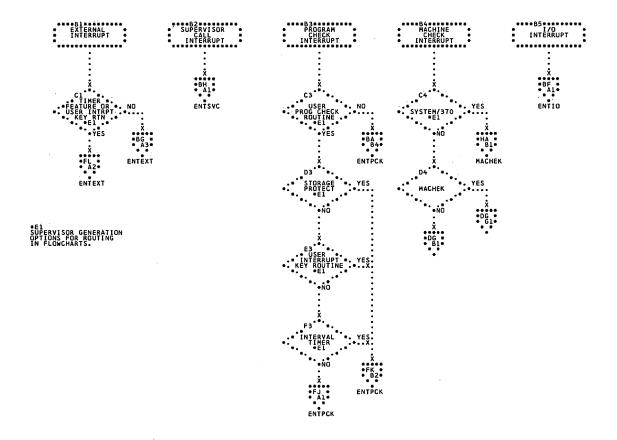
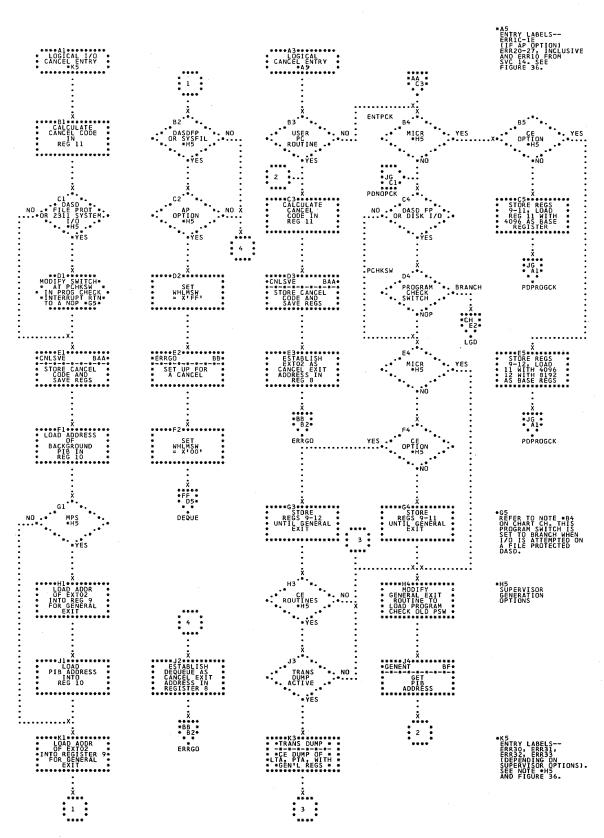


Chart BA. \$\$A\$SUP1 - FOPT Macro, General Cancels and Program Check without PC Routine Refer to Charts 02 and 03.



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Chart BAA. \$\$A\$SUP1 - FOPT Macro, CNLSVE and SVEREG Subroutines Refer to Charts 02 and 03.

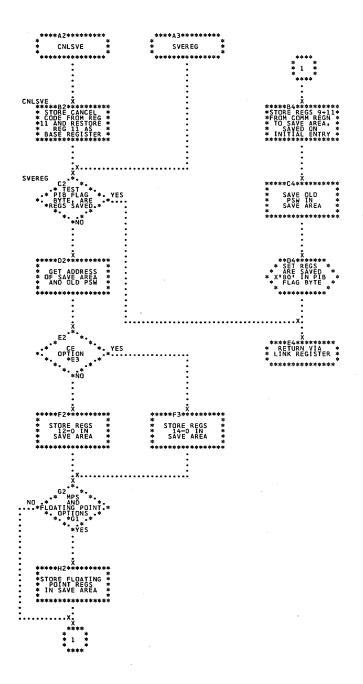


Chart BB. \$\$A\$SUP1 - FOPT Macro, General Cancel Subroutine Refer to Chart 03.

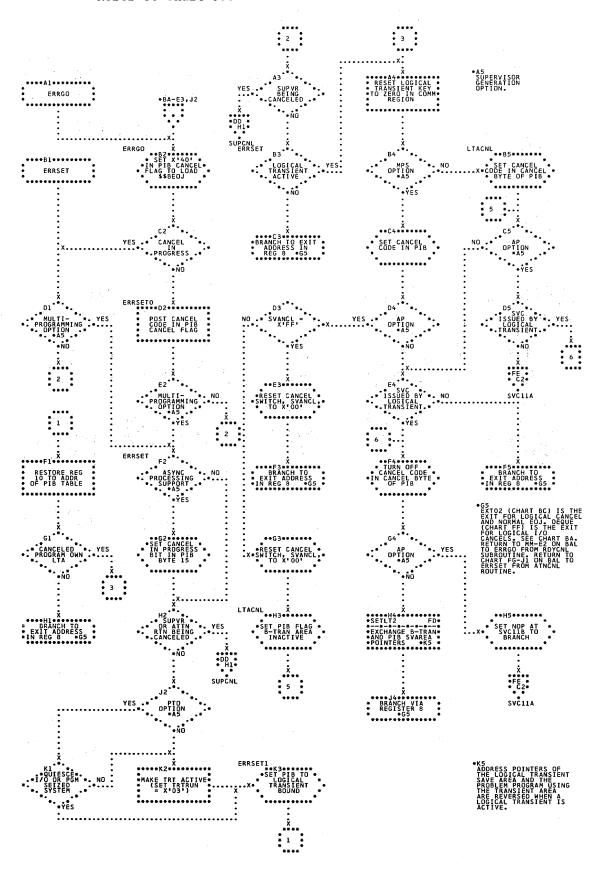


Chart BC. \$\$A\$SUP1 - FOPT Macro, General Exits (Part 1 of 4)
Refer to Chart 01.

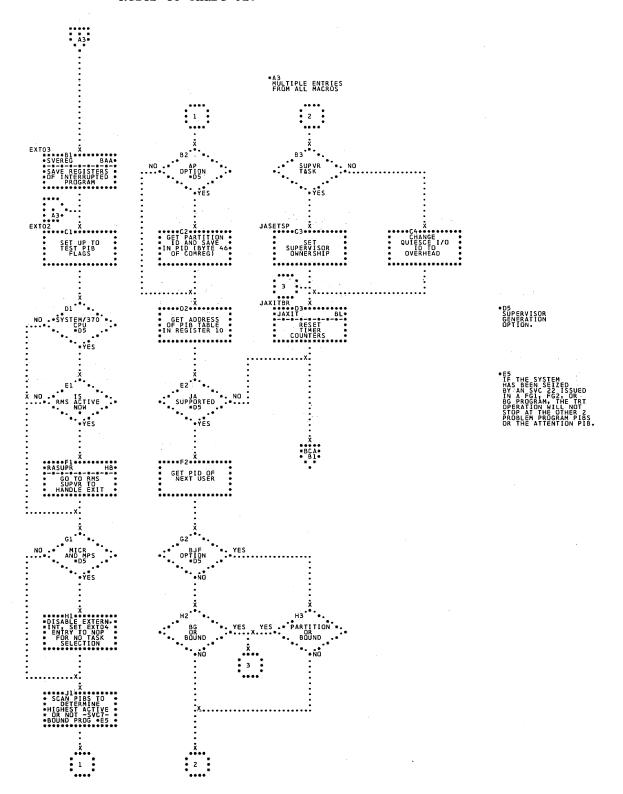


Chart BCA. \$\$A\$SUP1 - FOPT Macro, General Exits (Part 2 of 4) Refer to Chart 01.

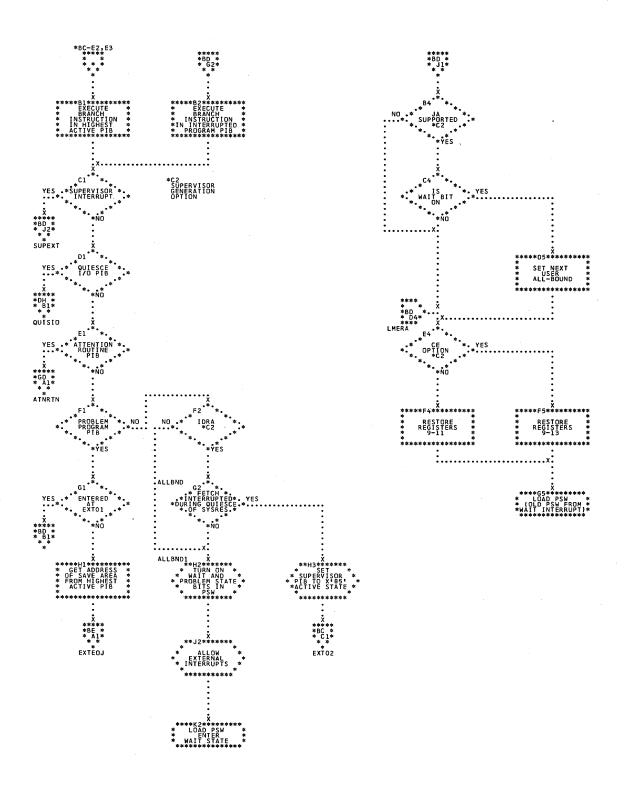


Chart BD. \$\$A\$SUP1 - FOPT Macro, General Exits (Part 3 of 4)
Refer to Chart 01.

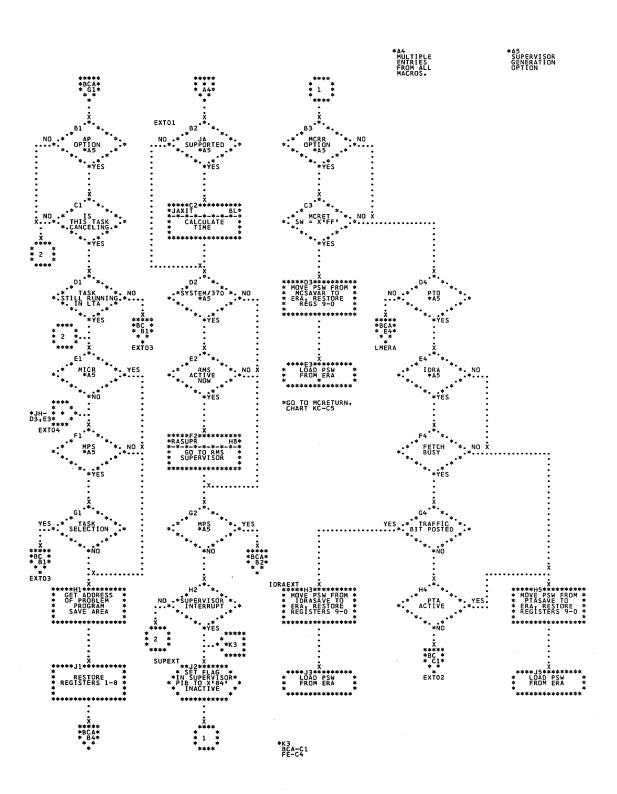
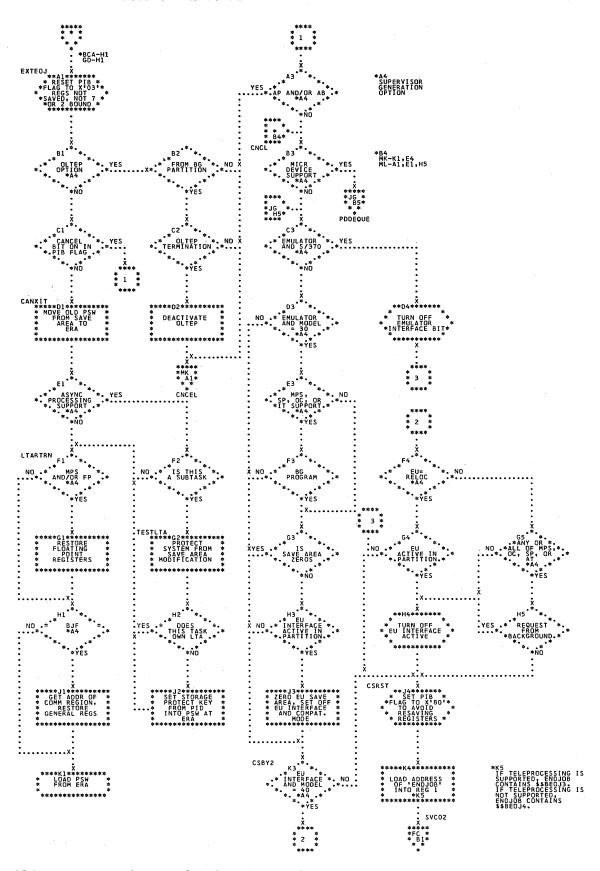


Chart BE. \$\$A\$SUP1 - FOPT Macro, General Exits (Part 4 of 4)
Refer to Chart 01.



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Chart BF. \$\$A\$SUP1 - FOPT Macro, General Entry (Part 1 of 2) Refer to Chart 05.

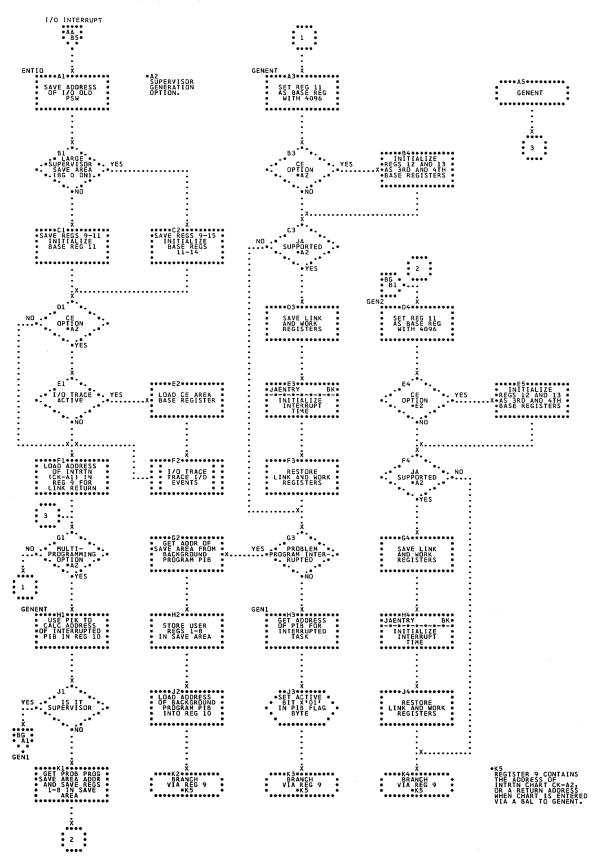
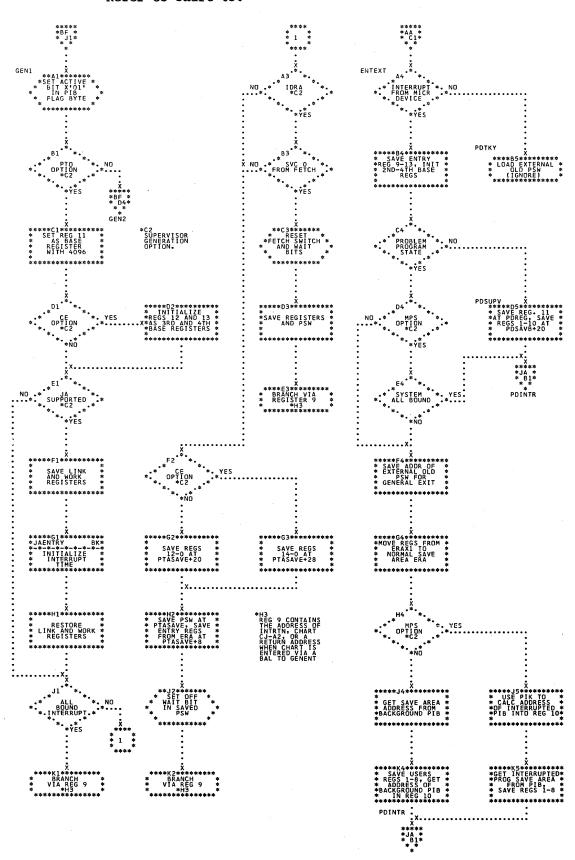


Chart BG. \$\$A\$SUP1 - FOPT Macro, General Entry (Part 2 of 2) Refer to Chart 05.



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Chart BH. \$\$A\$SUP1 - FOPT Macro, SVC Interrupt Handler Refer to Chart 03.

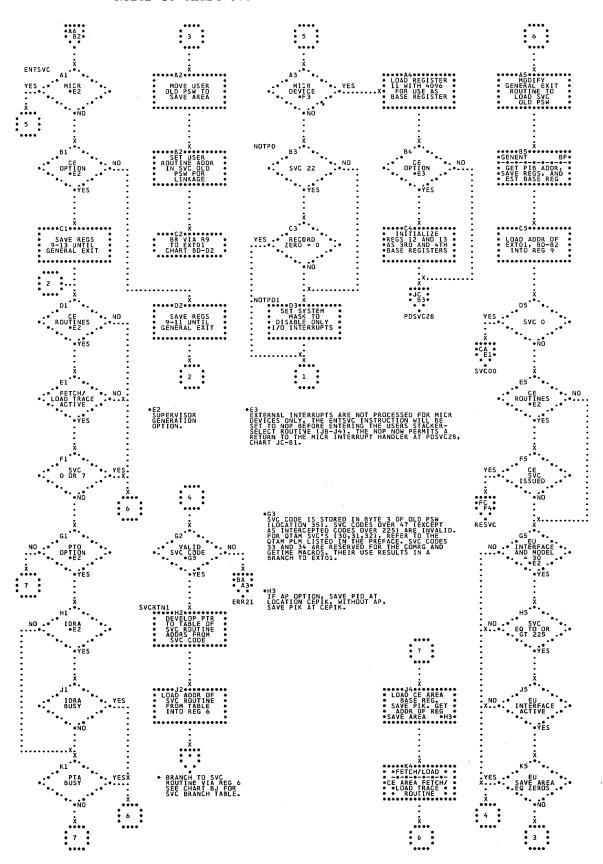
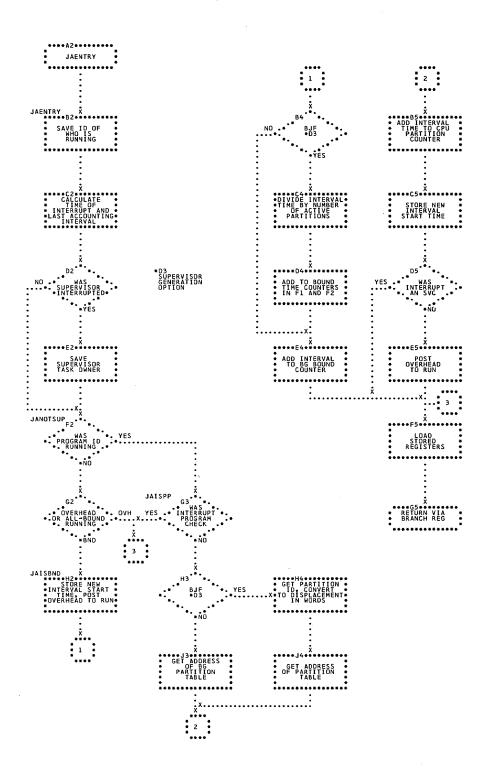


Chart BJ. \$\$A\$SUP1 - FOPT Macro, Supervisor Call Branch Table

SVC	OPTIONS	LABEL	CHART
0	ALL ·	SVC00	CA-F1
1	ALL	SVC01	FA-B1
2	ALL	SVC02	FC-B1
3	ALL	SVC03	FF-A1
4	ALL	SVC04	FF-B4
. 5	ALL	SVC05	FB-B2
. 6	ALL	SVC06	MM-B4
7	ALL	SVC07	FE-A3
8	ALL .	SVC08	FG-A1
9	ALL	SVC09	FG-A2
10	TIMER NO TIMER	SVC10 ERR21	FG-B5 BA-A3
11	ALL	SVC11	FE-B1
12	ALL	SVC12	FA-82
13	ALL	SVC13	FA-B4
14	ALL	ERR10	BA-A1
15	MPS NO MPS	SVC15	CA-B1 CB-B1
16	PC, NO IT OR OC PC AND IT OR OC NO PC	SXTRT1 SXTRT1 ERR21	FJ-85 FN-84 BA-A3
17	PC, NO IT OR OC PC AND IT OR OC NO PC	EXTRT1 EXTRT1 ERR21	FJ-B4 FN-B2 BA-A3
18	TIMER NO TIMER	SVC18 ERR21	FN-B5 BA-A3
19	TIMER NO TIMER	SVC19 ERR21	FN-B3 BA-A3
20	OC RTN NO OC TRN	SXTRT1 ERR21	FN-B4 BA-A3
21	OC RTN NO OC RTN	EXTRT1 ERR21	FN-B2 BA-A3
22	MPS NO MPS	SVC22 EXT01	FH-B1 BD-B2
23	MPS NO MPS	SVC23 ERR21	FH-B3 BA-A3
24	TIMER NO TIMER	SVC24 ERR21	FH-B5 BA-A3
25	BTAM OR OLTEP NO BTAM AND NO OLTEP	SVC25 ERR21	CA-F1 BA-A3

svc	OPTIONS	LABEL	CHART
26	STOR PROT	SVC26	FH-B4
	NO STOR PROT	EXT01	BD-B2
27	BTAM	SVC27	CA-F1
	NO BTAM	EXT01	BD-B2
28	MICR	PDSVC28	JC-B3
	NO MICR	ERR21	BA-A3
29	MICR	SVC29	FB-B3
	NO MICR	ERR21	BA-A3
30 TO 32	RESERVED FOR QTAM; REFER TO QTAM PLM LISTED IN PREFACE		
33,34	RESERVED FOR COMRG AND GETIME MACROS		
35	TRKHLD	SVC35	MA-A1
	NO TRKHLD	ERR21	BA-A3
36	TRKHLD	SVC36	MB-A1
	NO TRKHLD	ERR21	BA-A3
37	AB	SVC37	MC-A4
	NO AB	ERR21	BA-A3
38	AP	SVC38	MD-A1
	NO AP	ERR21	BA-A3
39	AP	SVC39	ME-A1
	NO AP	ERR21	BA-A3
40	AP	SVC40	MG-A1
	NO AP	ERR21	BA-A3
41	AP	SVC41	MH-A1
	NO AP	ERR21	BA-A3
42	AP	SVC42	MG-A4
	NO AP	ERR21	BA-A3
43	ERROR OR MCRR	SDRSDR	LF-C5
	NO ERRLOG AND NO MCRR	ERR21	BA-A3
44	ERRLOG OR MCRR	SDROBR	LF-C4
	NO ERRLOG AND MCRR	ERR21	BA-A3
45	EMULATOR INTERFACE	SVC45	FR-B1
	NO EMULATOR INTERFACE	ERR21	BA-A3
46	OLTEP INTERFACE	SVC46	FR-F4
	NO OLTEP INTERFACE	ERR21	BA-A3
47	WAITE FOR MICE DEVICES	SVC29	FB-B3
50	USED BY LIOCS FOR ERROR RECOVERY		
51	OLTEP	SVC51	FS-B2
	NO OLTEP	ERR21	BA-A3

Chart BK. \$\$A\$SUP1 - FOPT Macro, Job Accounting Timer Update Routine



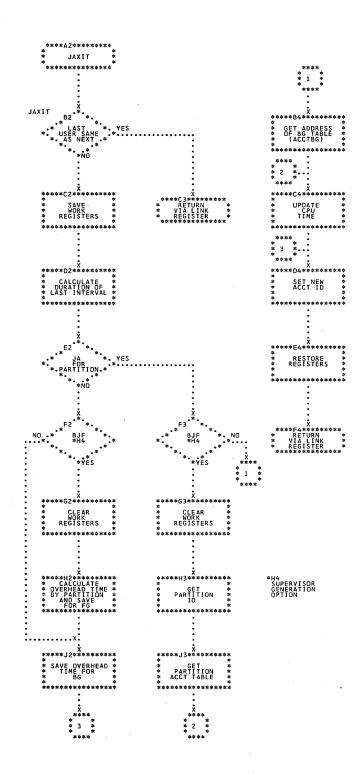


Chart CA. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler with MPS (Part 1 of 2) Refer to Chart 04.

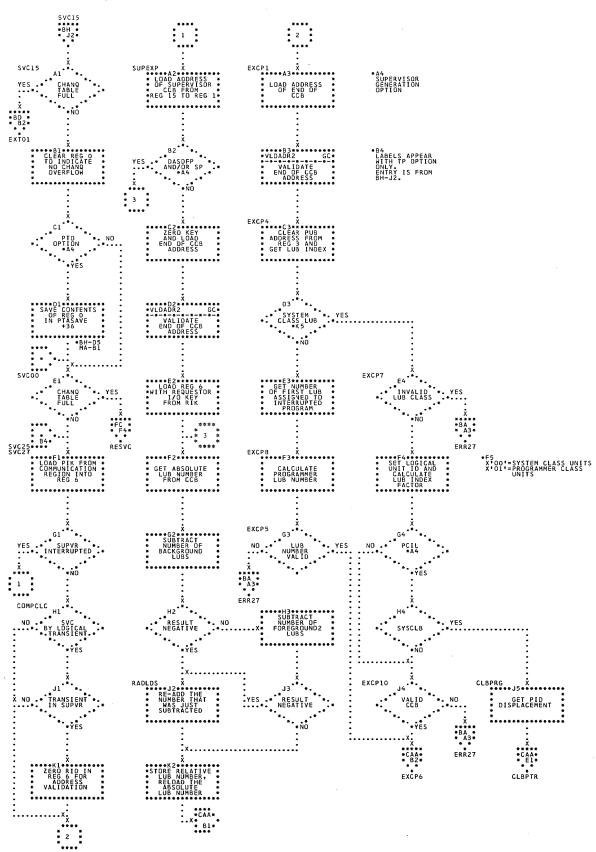


Chart CAA. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler with MPS (Part 2 of 2) Refer to Chart 04.

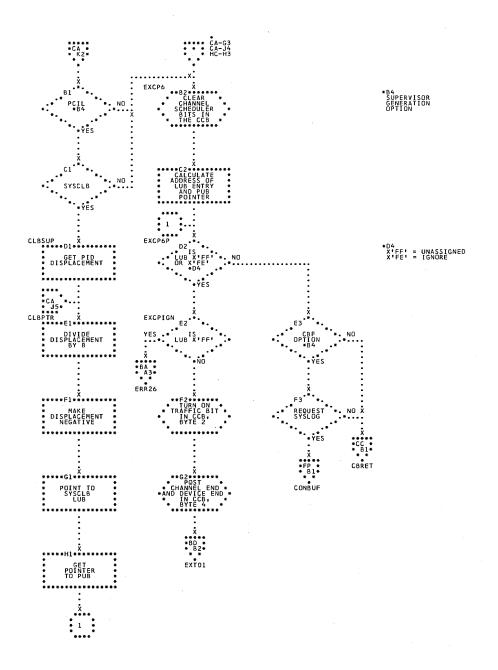


Chart CB. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler without MPS Refer to Chart 04.

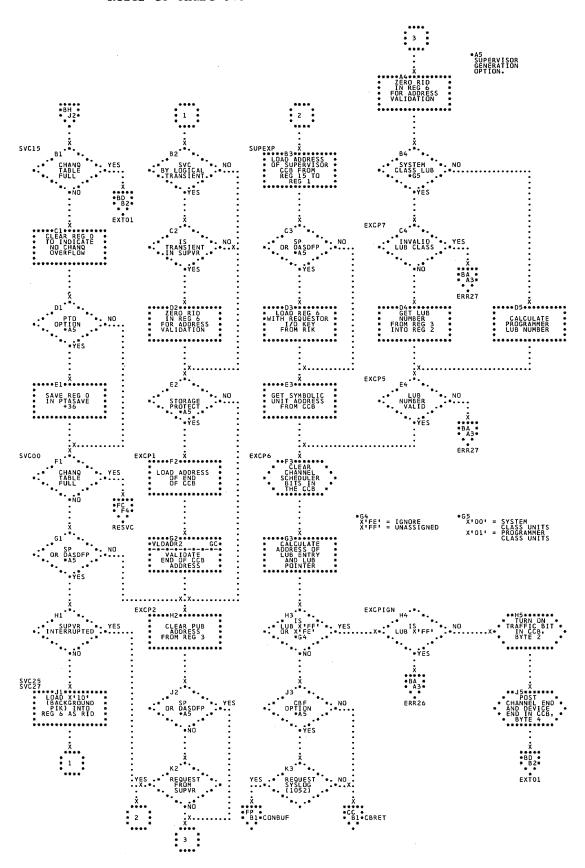


Chart CC. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler (Part 1 of 3) Refer to Chart 04.

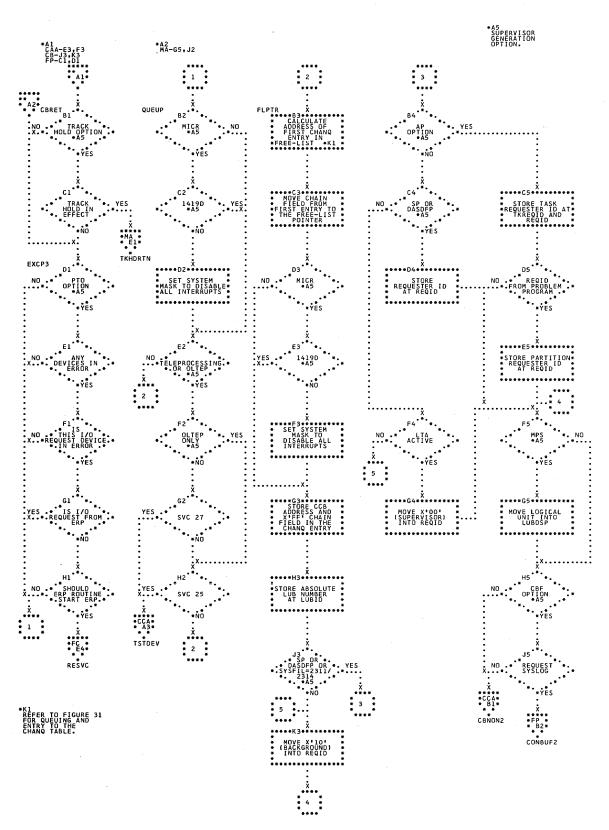


Chart CCA. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler (Part 2 of 3) Refer to Chart 04.

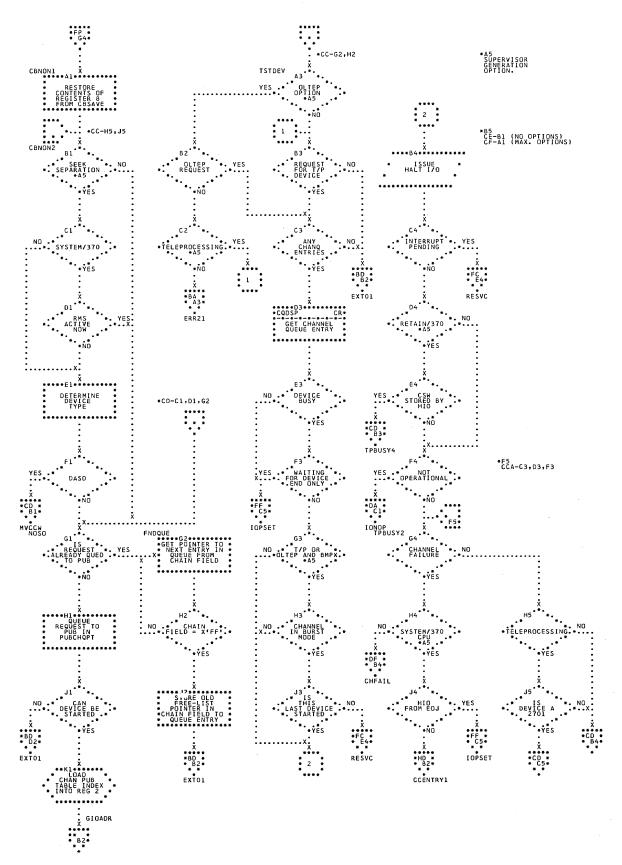


Chart CD. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler (Part 3 of 3) Refer to Chart 04.

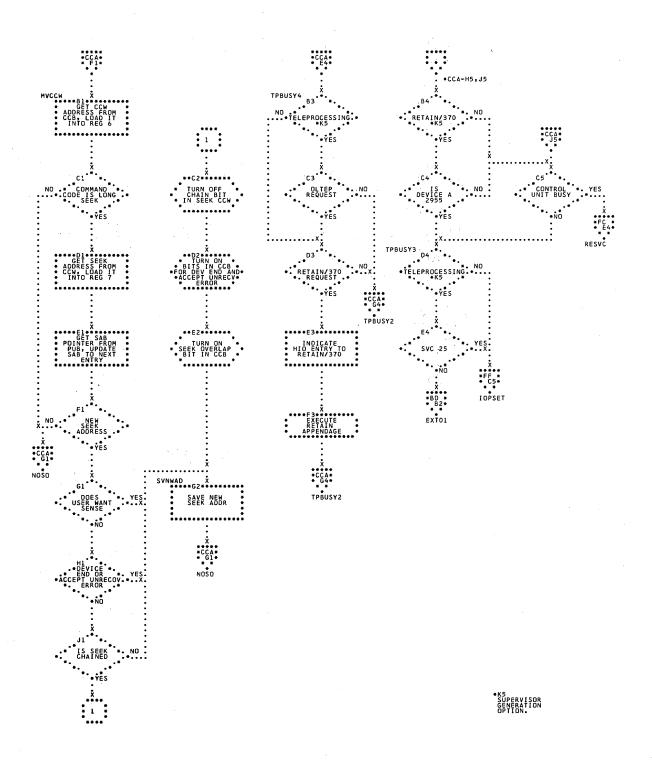


Chart CE. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- No Options, UNCOMMON Routine Refer to Chart 04.

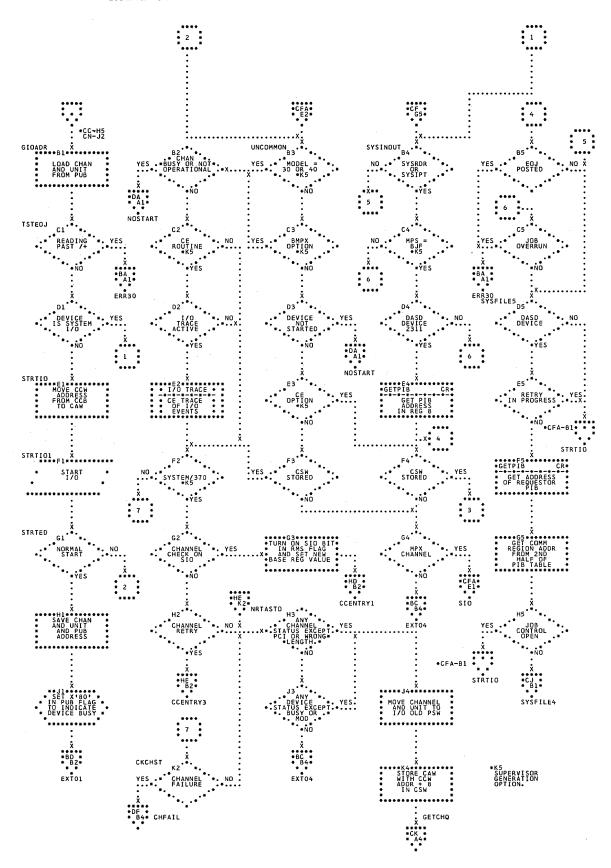


Chart CF. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- Maximum Options (Part 1 of 5) Refer to Chart 04.

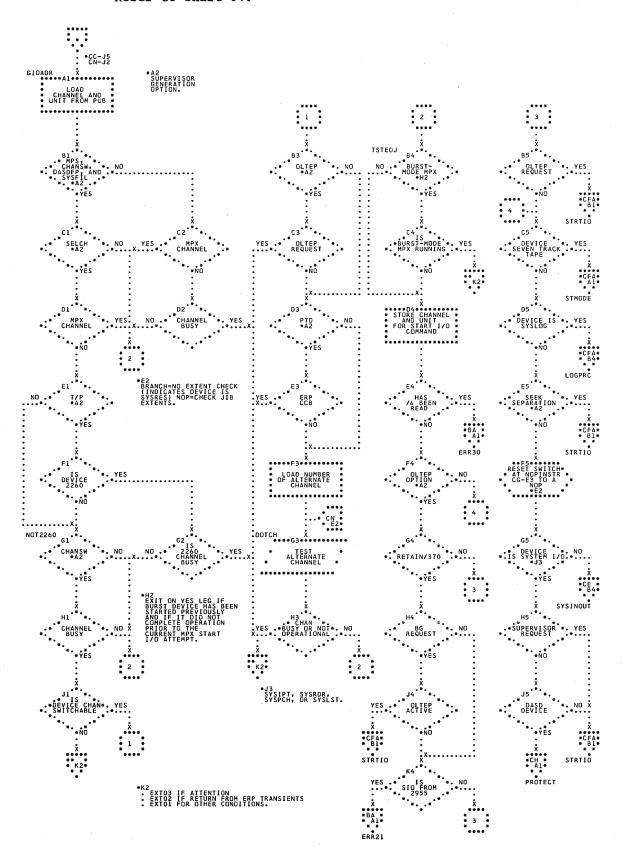


Chart CFA. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- Maximum Options (Part 2 of 5) Refer to Chart 04.

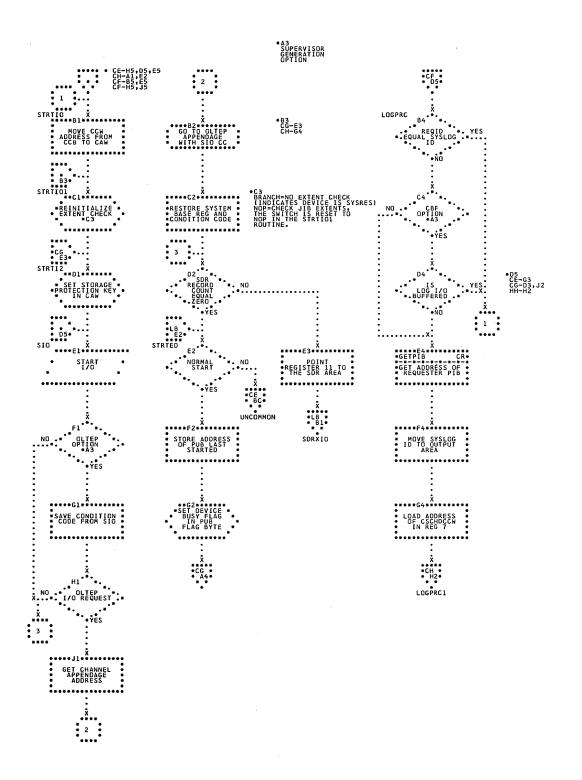
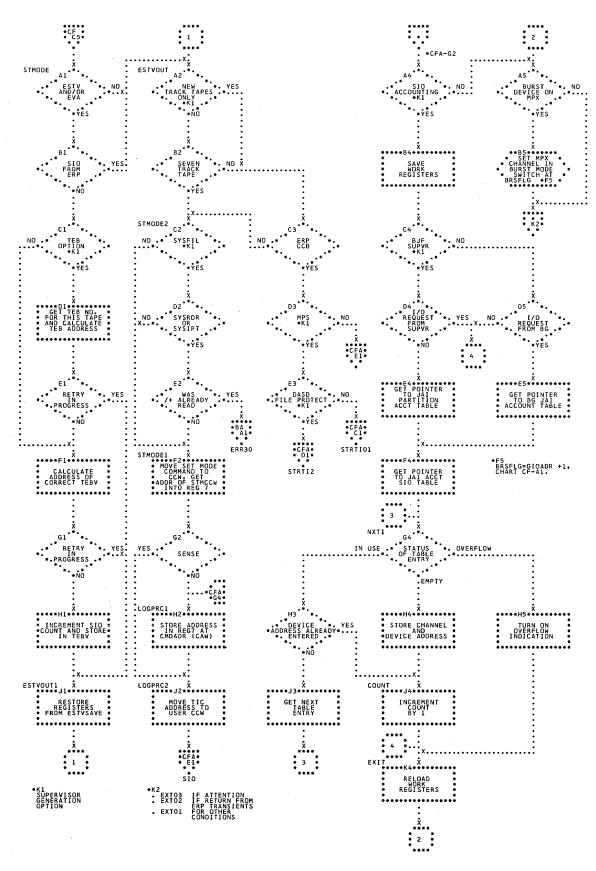


Chart CG. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- Maximum Options (Part 3 of 5) Refer to Chart 04.



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Chart CH. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- Maximum Options (Part 4 of 5)
Refer to Chart 04.

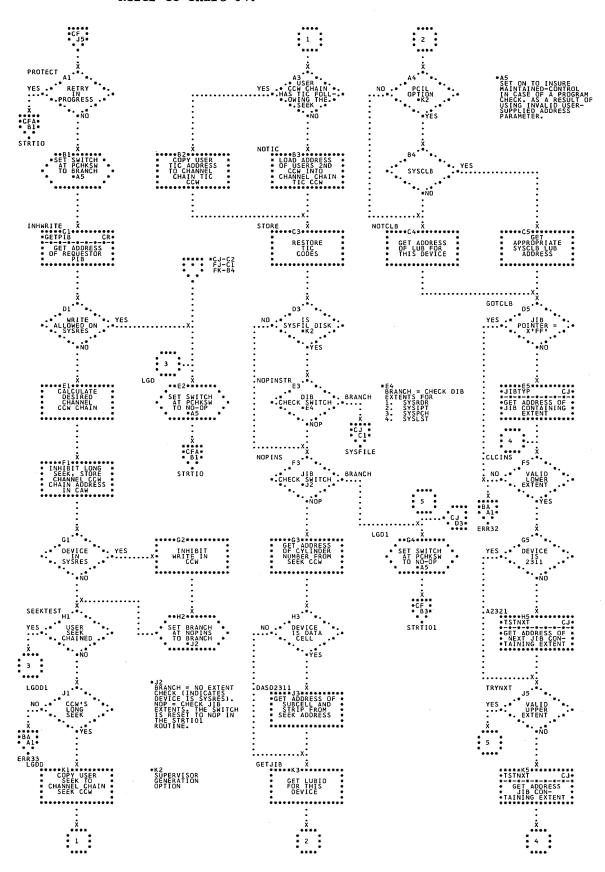


Chart CJ. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- Maximum Options (Part 5 of 5) Refer to Chart 04.

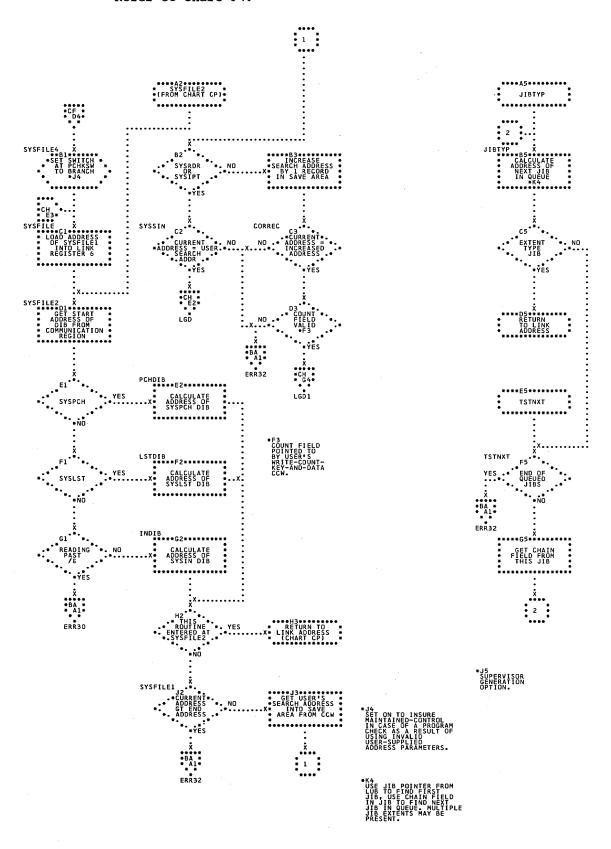


Chart CK. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt (Part 1 of 7)
Refer to Chart 04.

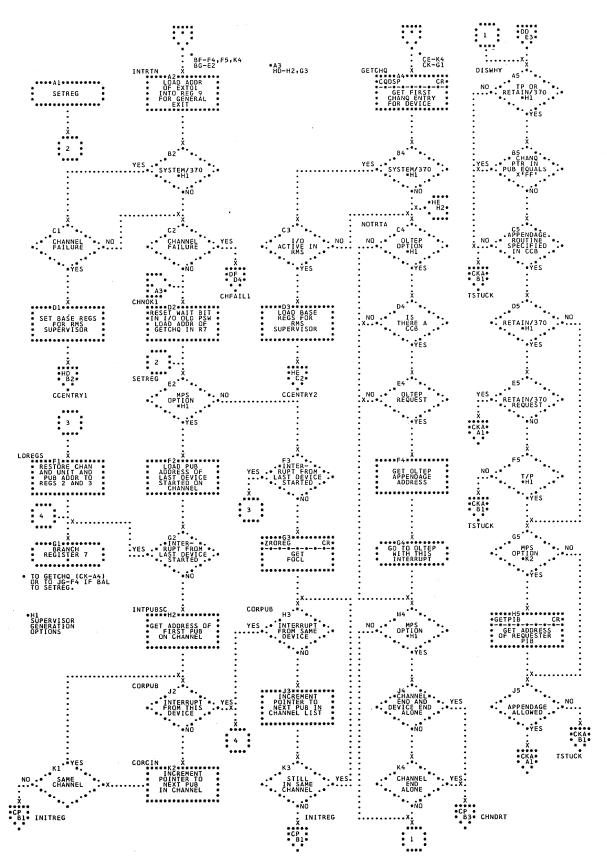


Chart CKA. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt (Part 2 of 7)
Refer to Chart 04.

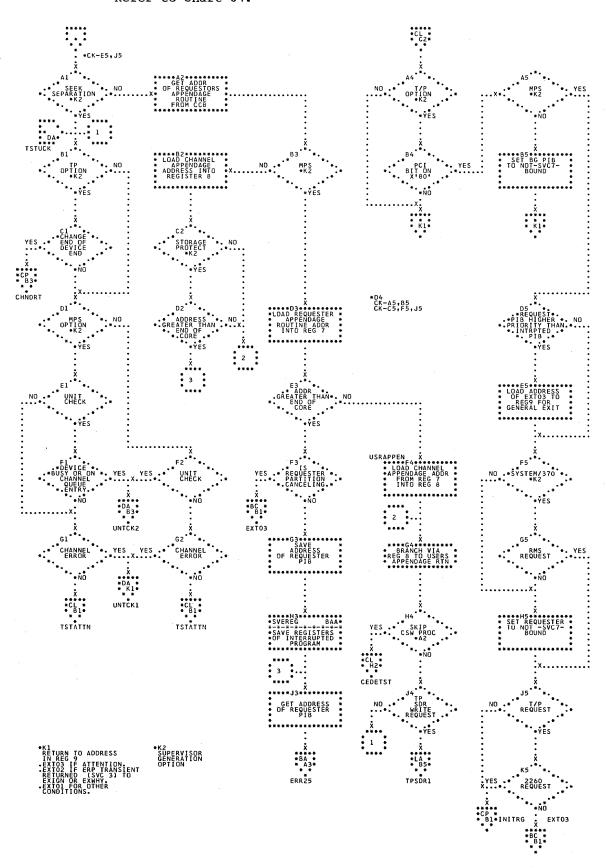


Chart CL. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt (Part 3 of 7) Refer to Chart 04.

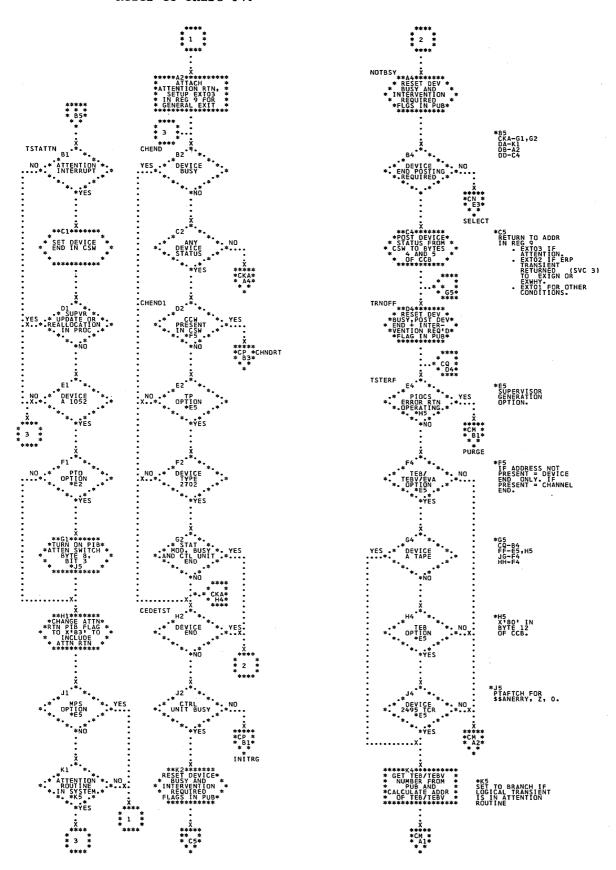
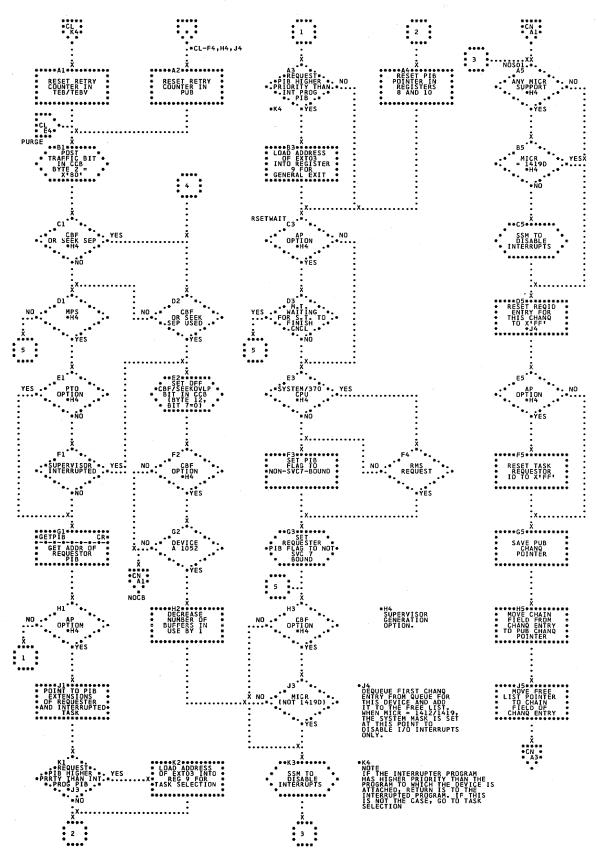


Chart CM. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt (Part 4 of 7)
Refer to Chart 04.



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Chart CN. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt (Part 5 of 7)
Refer to Chart 04.

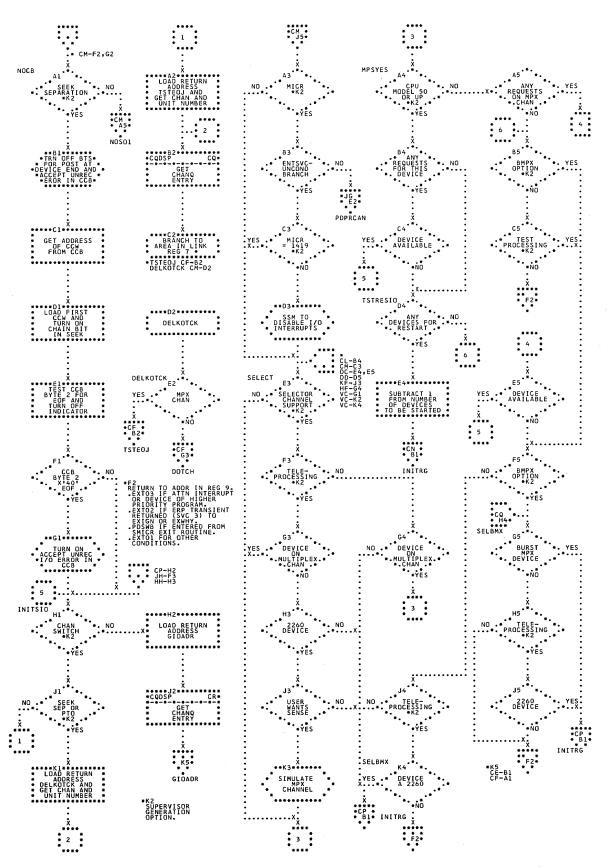


Chart CP. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt (Part 6 of 7)
Refer to Chart 04.

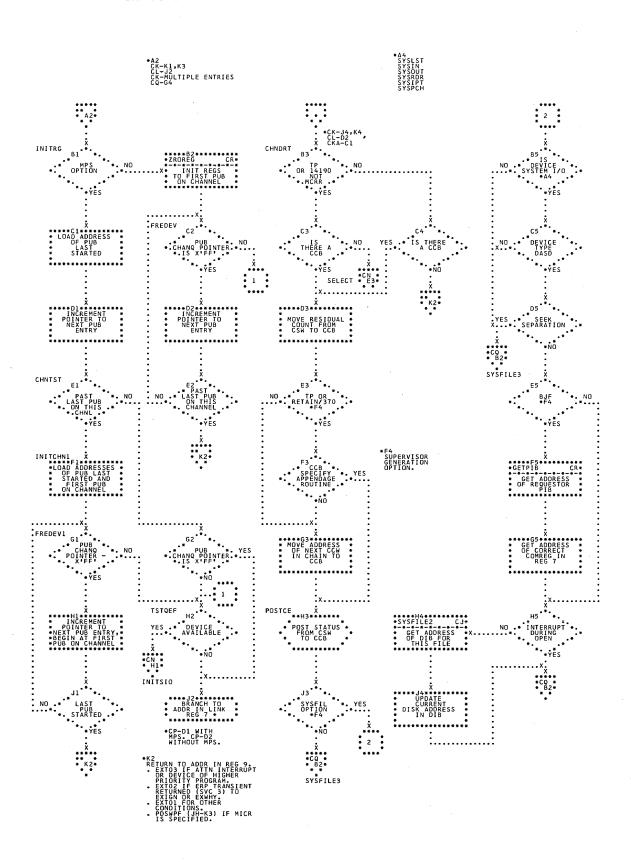


Chart CQ. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt (Part 7 of 7)
Refer to Chart 04.

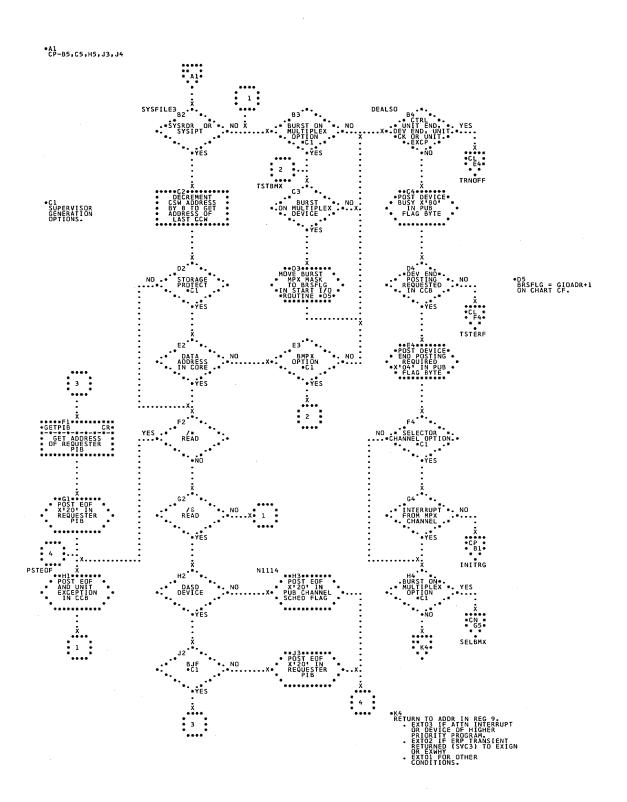


Chart CR. \$\$A\$SUP1 - SGTCHS Macro, I/O Interrupt Subroutines Refer to Chart 04.

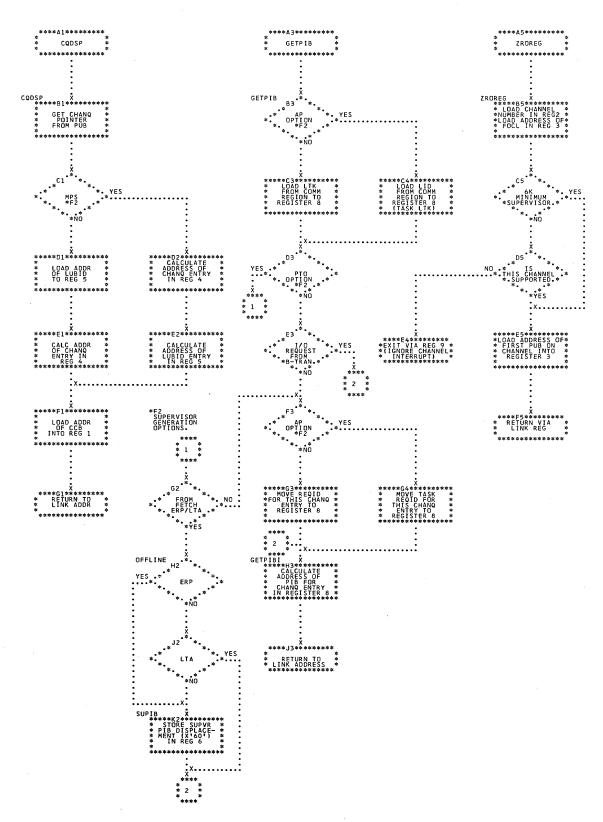


Chart DA. \$\$A\$SUP1 - SGUNCK Macro, Unit Check Entries (Part 1 of 2) Refer to Chart 06.

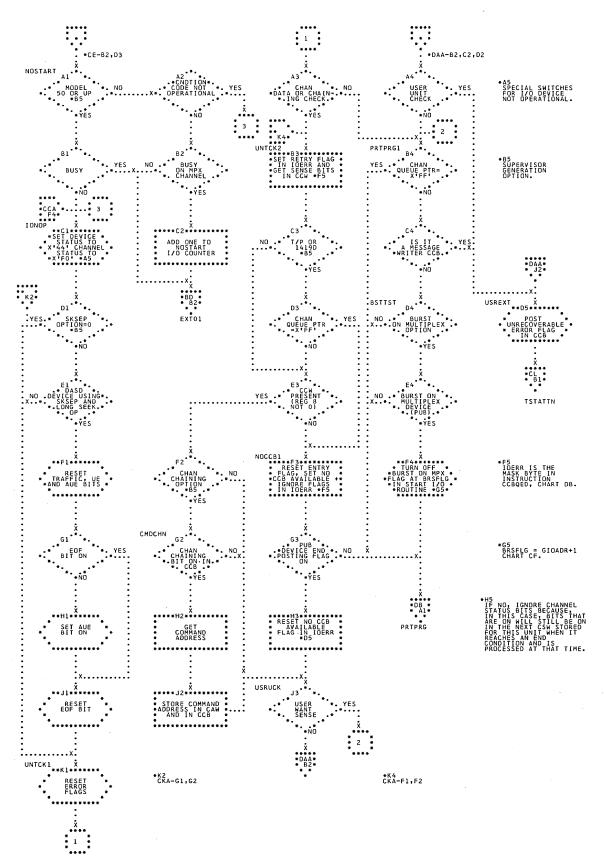


Chart DAA. \$\$A\$SUP1 - SGUNCK Macro, Unit Check Entries (Part 2 of 2) Refer to Chart 06.

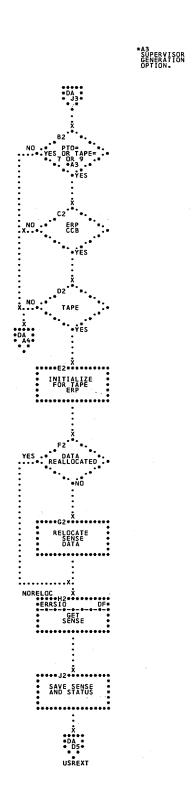


Chart DB. \$\$A\$SUP1 - SGUNCK Macro, Build Error Queue Entry Refer to Chart 06.

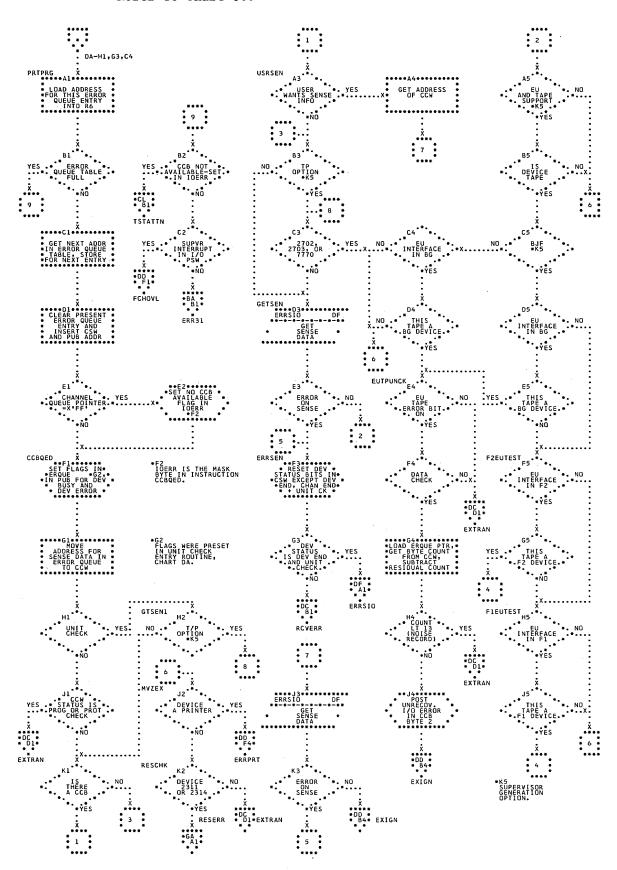
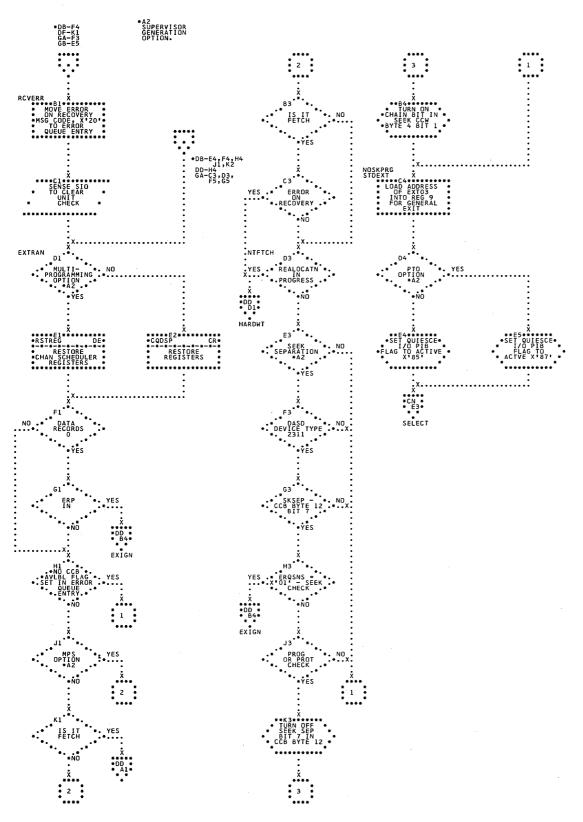


Chart DC. \$\$A\$SUP1 - SGUNCK Macro, Error Recovery Exits (Part 1 of 2) Refer to Chart 06.



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Chart DD. \$\$A\$SUP1 - SGUNCK Macro, Error Recovery Exits (Part 2 of 2)
Refer to Chart 06.

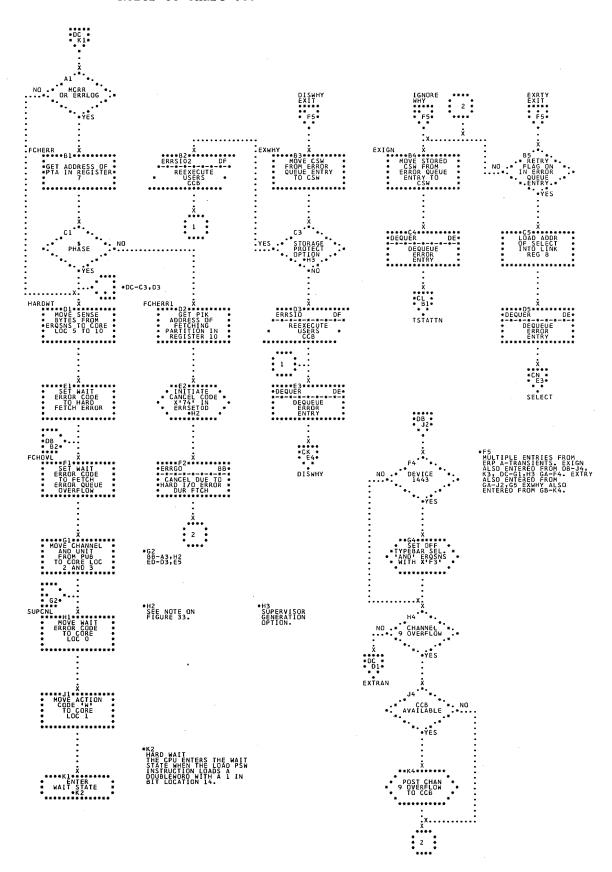


Chart DE. \$\$A\$SUP1 - SGUNCK Macro, DEQUER and RSTREG Subroutines Refer to Chart 06.

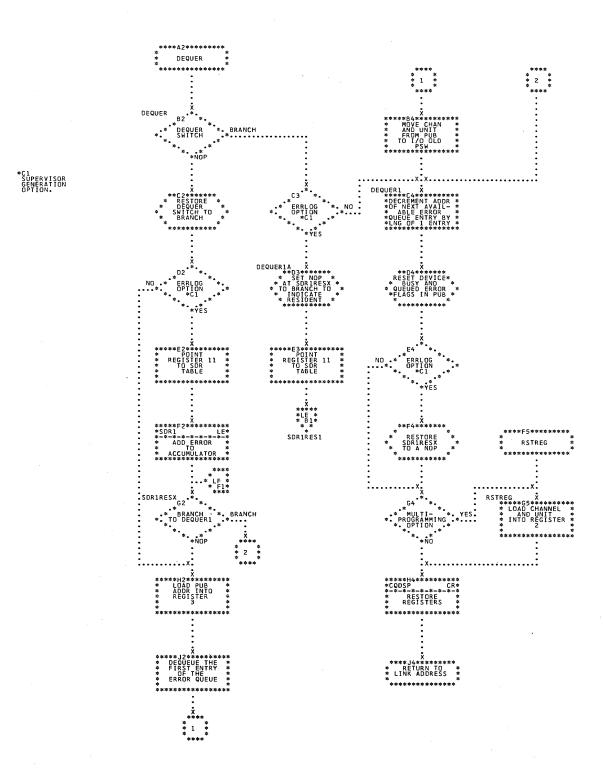


Chart DF. \$\$A\$SUP1 - SGUNCK Macro, Error Start I/O and Channel Failure Subroutines Refer to Charts 06 and 07.

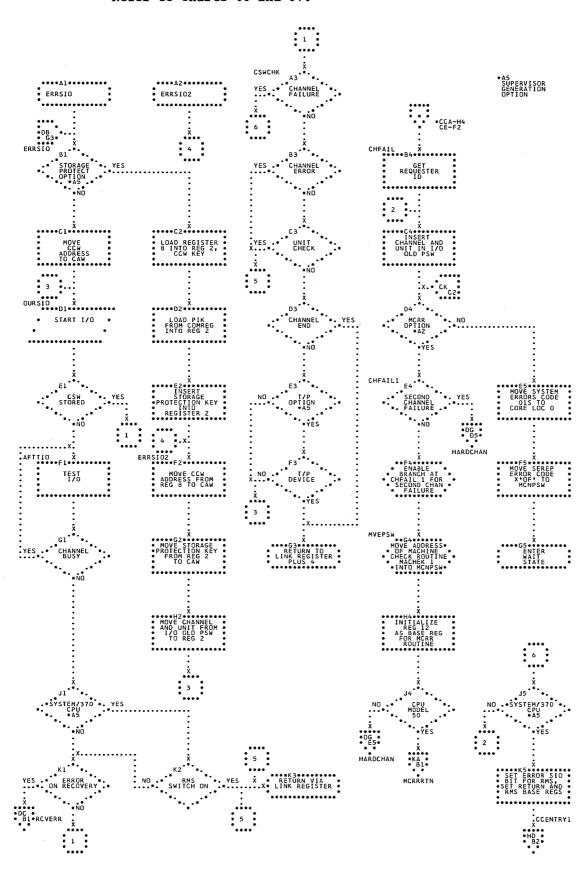
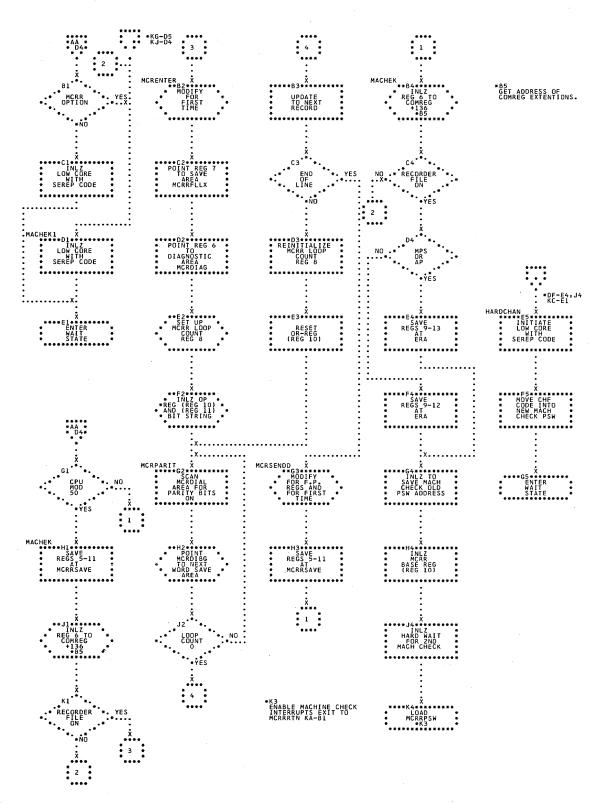


Chart DG. \$\$A\$SUP1 - SGUNCK Macro, Machine Check Interrupt Refer to Chart 07.



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Chart DH. \$\$A\$SUP1 - SGUNCK Macro, Quiesce I/O Task Refer to Chart 07

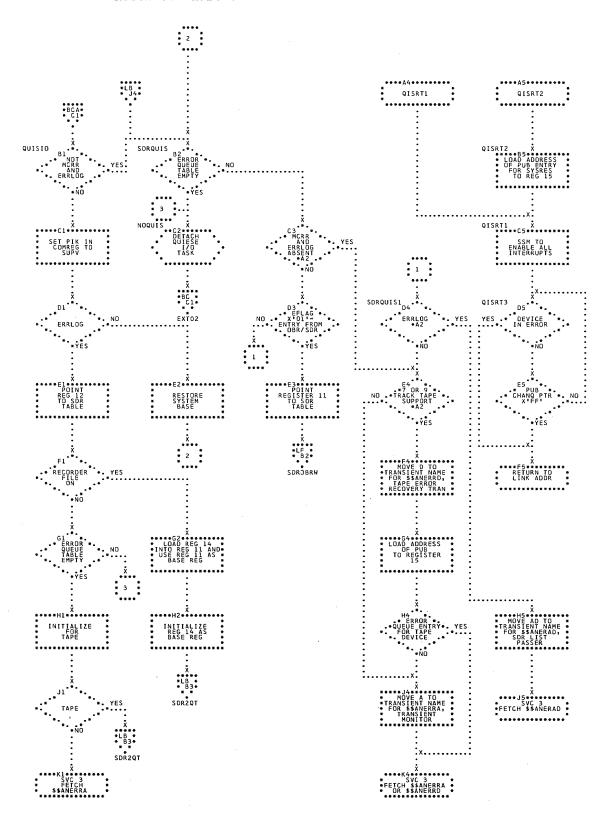


Chart EA. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 1 of 9) Refer to Chart 03.

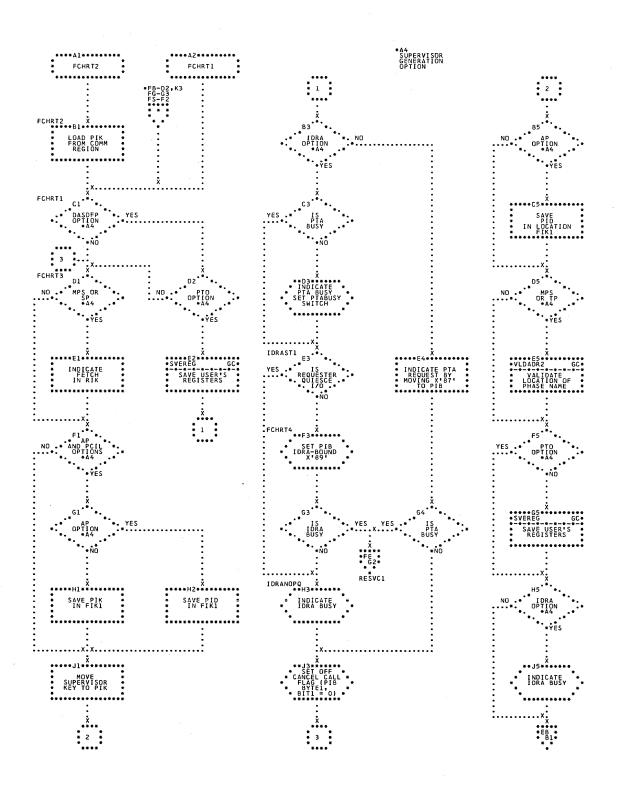


Chart EB. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 2 of 9) Refer to Chart 03.

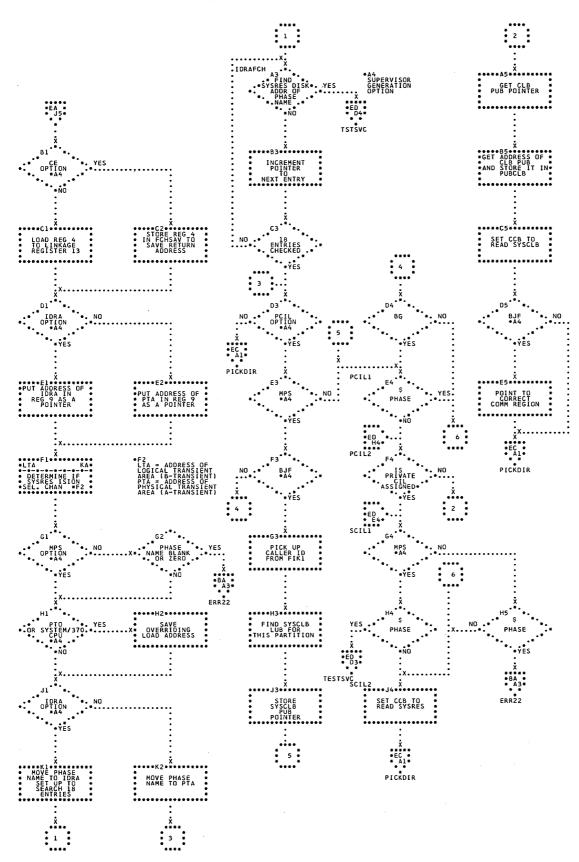
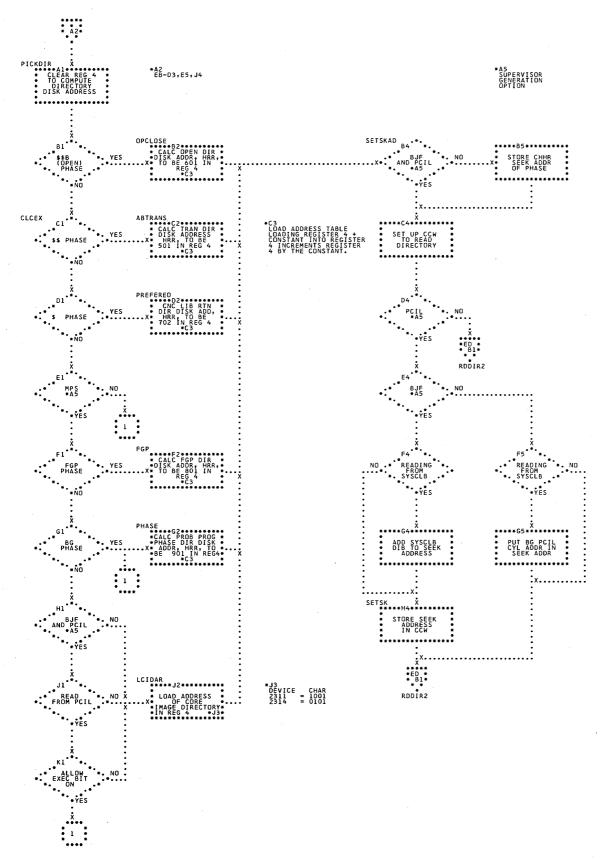


Chart EC. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 3 of 9) Refer to Chart 03.



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Chart ED. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 4 of 9) Refer to Chart 03.

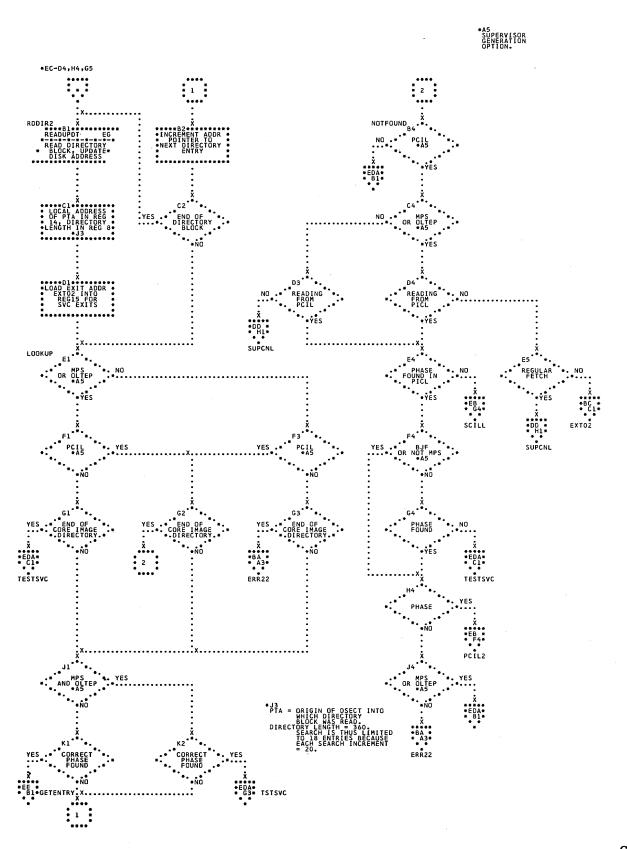
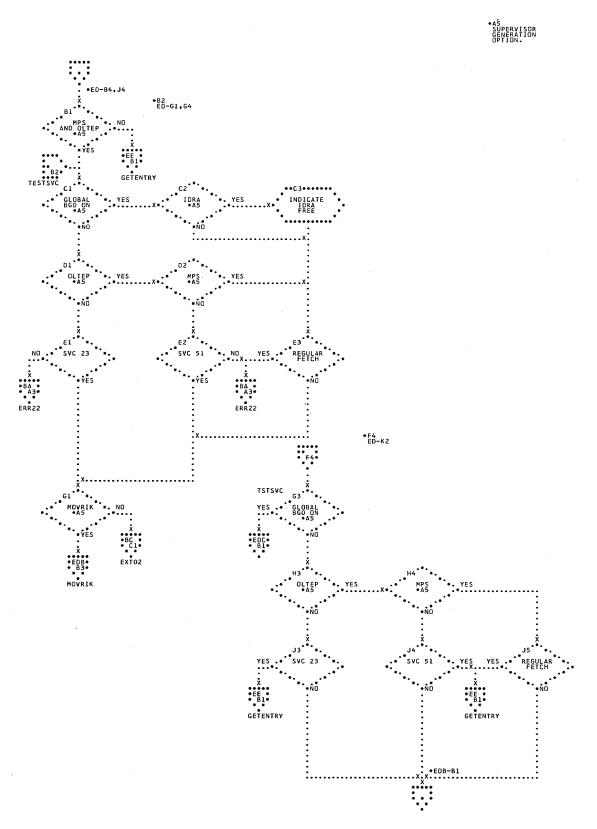


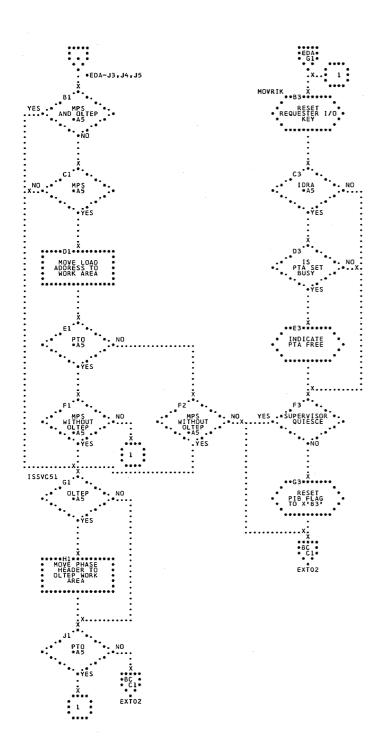
Chart EDA. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 5 of 9) Refer to Chart 03.

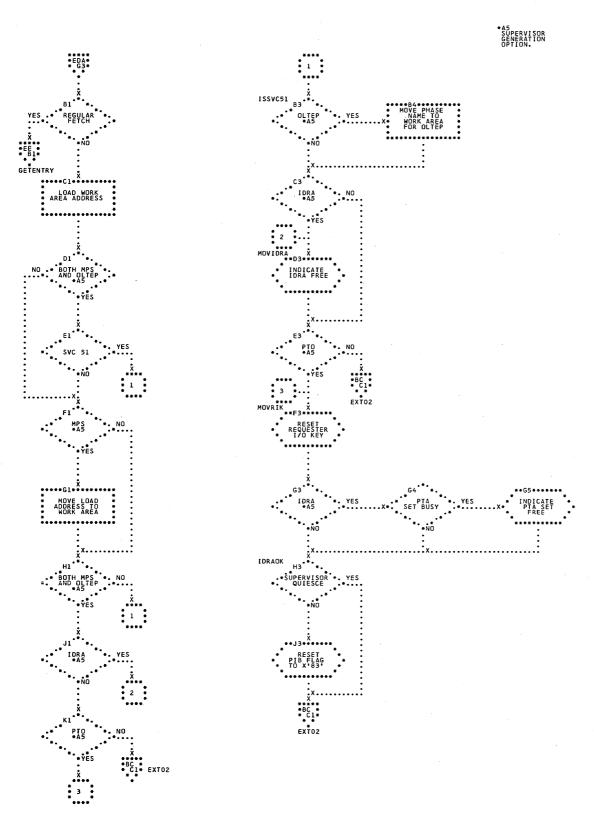


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Chart EDB. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 6 of 9) Refer to Chart 03.







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Chart EE. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 8 of 9) Refer to Chart 03.

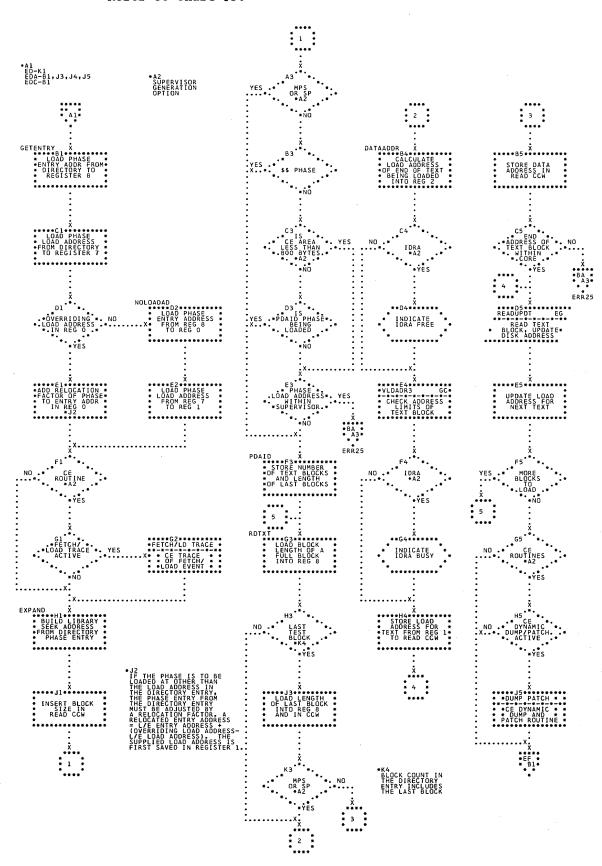


Chart EF. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 9 of 9) Refer to Chart 03.

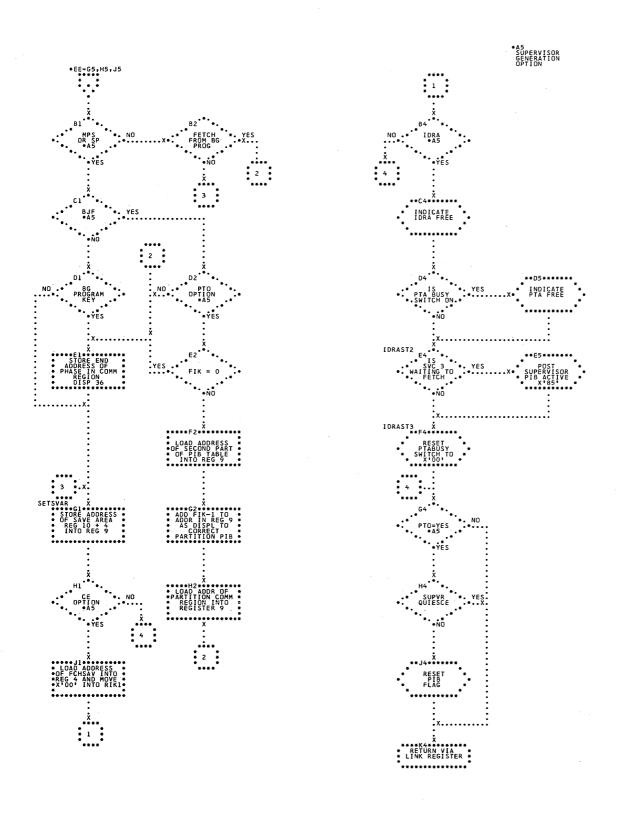


Chart EG. \$\$A\$SUP1 - SGDFCH Macro, Fetch Subroutine (Part 1 of 2) Refer to Chart 03.

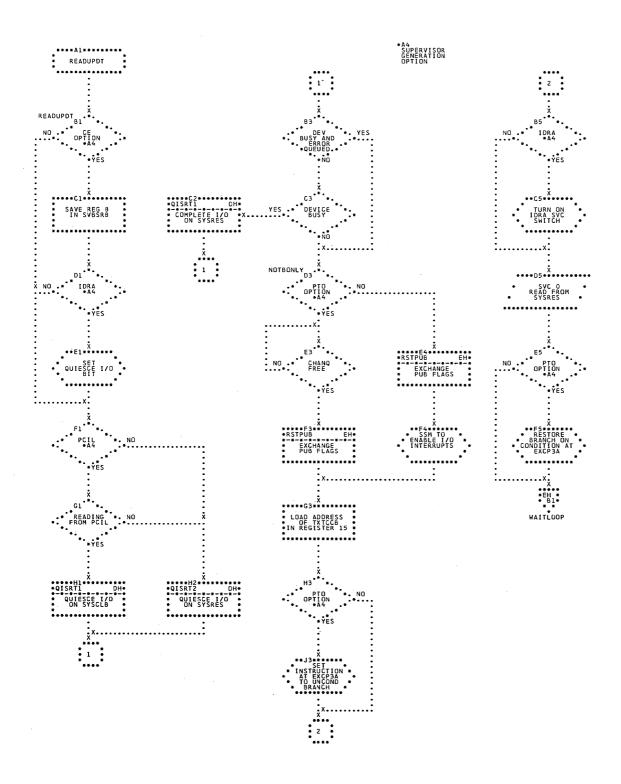


Chart EH. \$\$A\$SUP1 - SGDFCH Macro, Fetch Subroutine (Part 2 of 2) Refer to Chart 03.

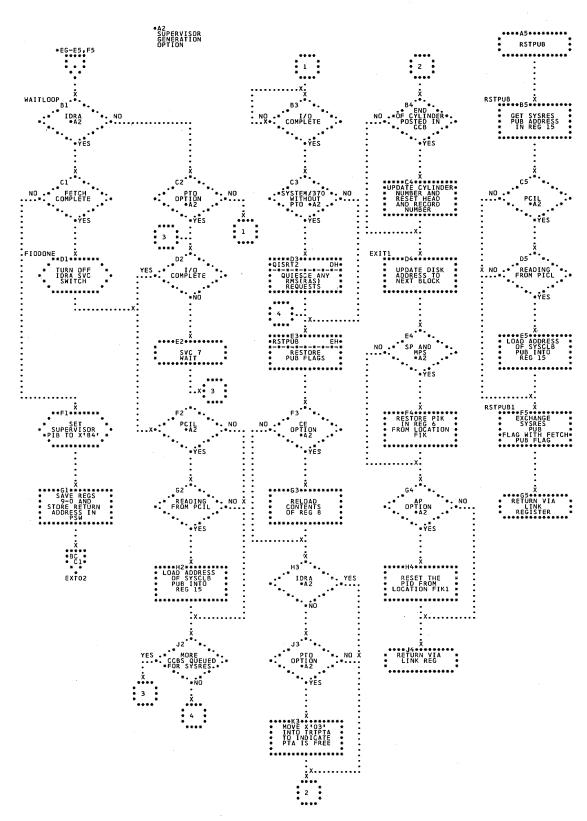


Chart FA. \$\$A\$SUP1 - SGSVC Macro, SVCs 1, 12, and 13 Refer to Chart 03.

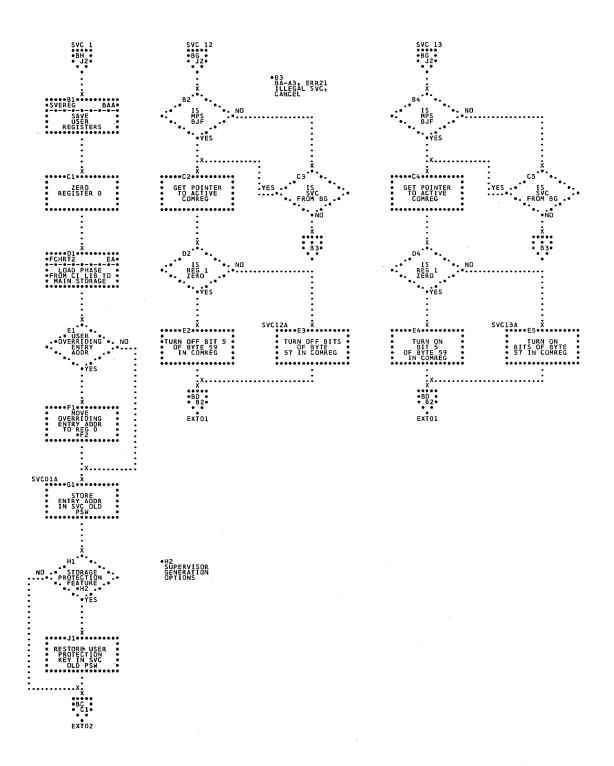


Chart FB. \$\$A\$SUP1 - SGSVC Macro, SVCs 5 and 29 Refer to Chart 03.

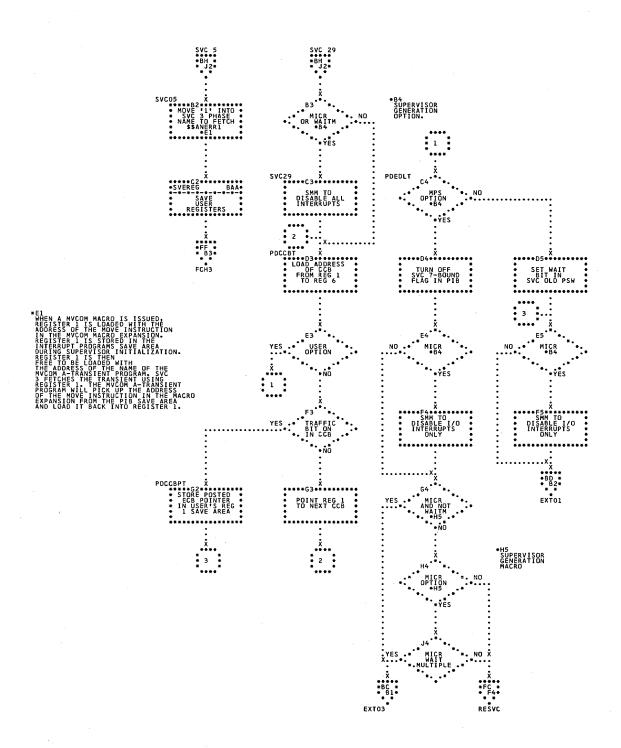


Chart FC. \$\$A\$SUP1 - SGSVC Macro, SVC 2 (Part 1 of 2) Refer to Chart 03.

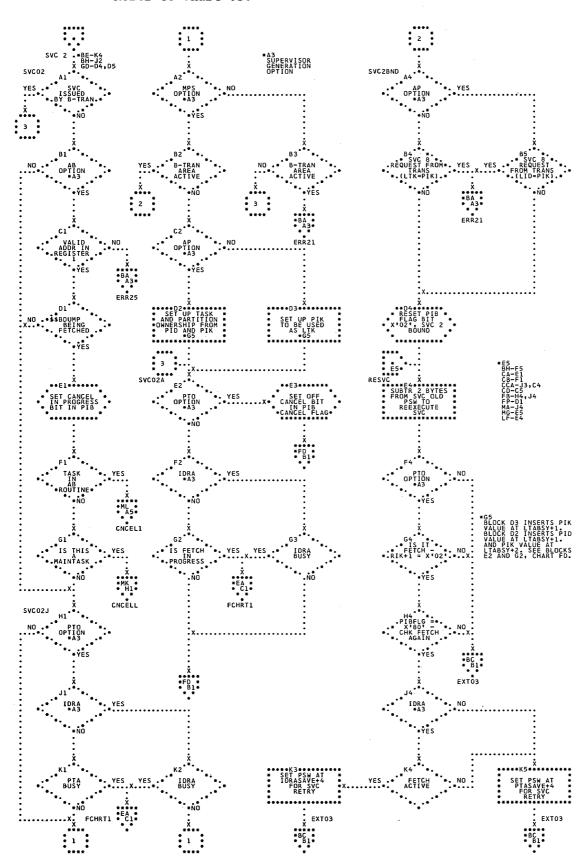
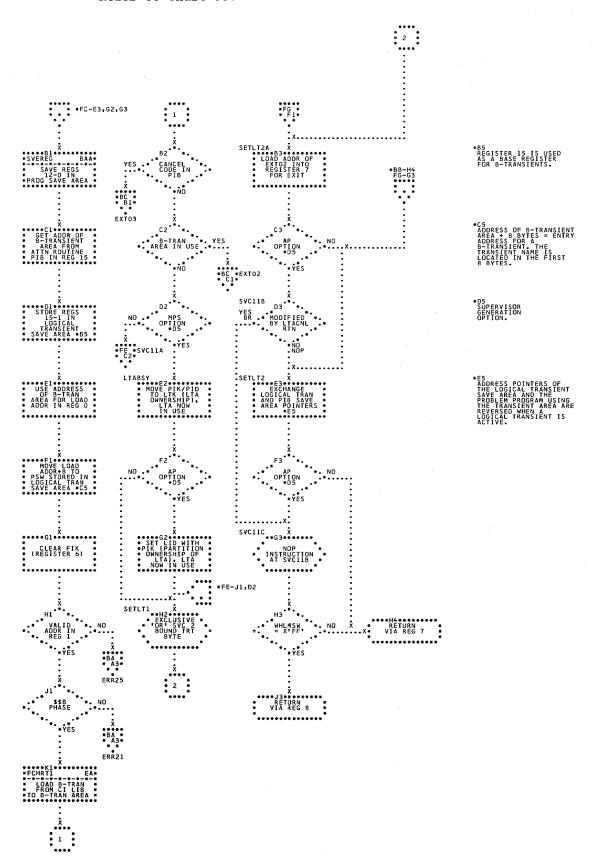


Chart FD. \$\$A\$SUP1 - SGSVC Macro, SVC 2 (Part 2 of 2), SETLT1 and SETLT2 Routines. Refer to Chart 03.



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Chart FE. \$\$A\$SUP1 - SGSVC Macro, SVCs 7 and 11 Refer to Chart 03.

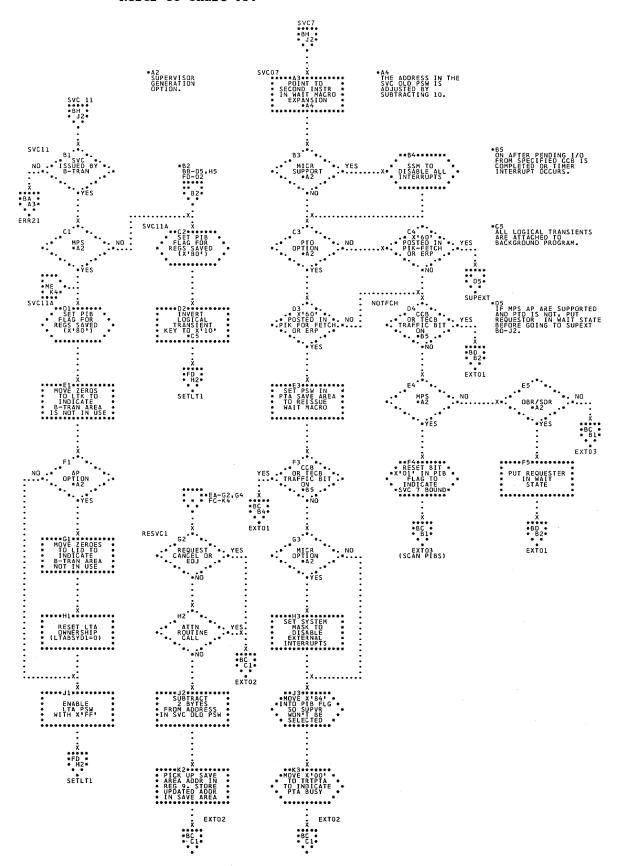
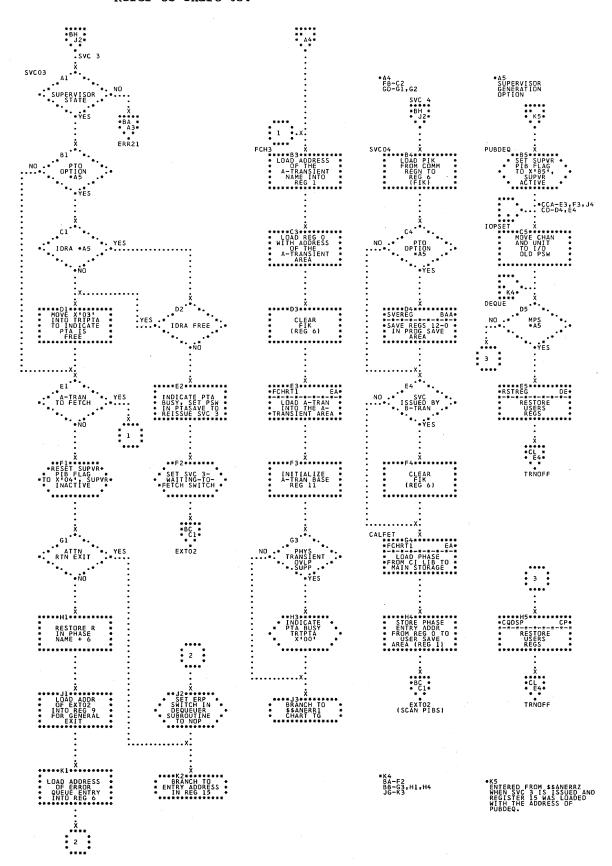


Chart FF. \$\$A\$SUP1 - SGSVC Macro, SVCs 3 and 4 Refer to Chart 03.



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Chart FG. \$\$A\$SUP1 - SGSVC Macro, SVCs 8, 9, and 10 Refer to Chart 03.

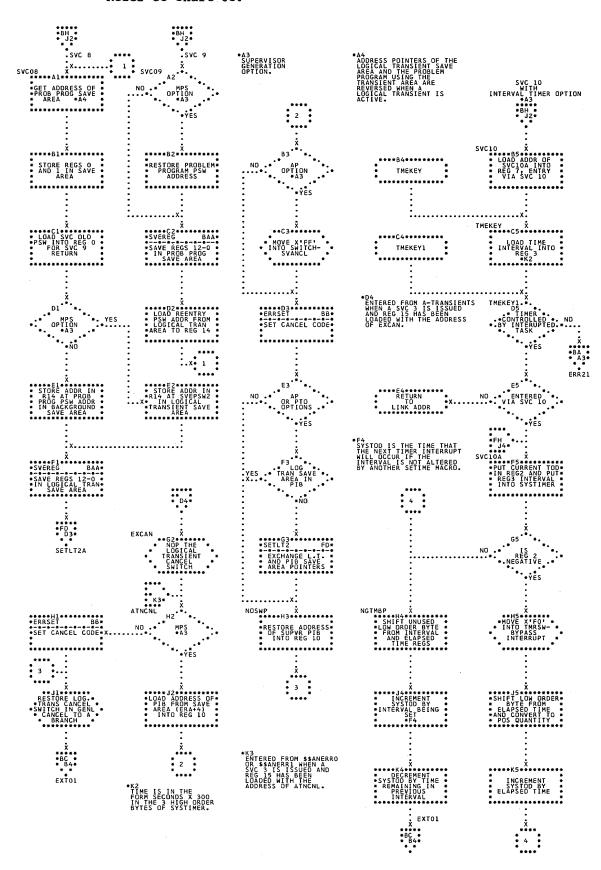


Chart FH. \$\$A\$SUP1 - SGSVC Macro, SVCs 22, 23, 24, and 26 Refer to Chart 03.

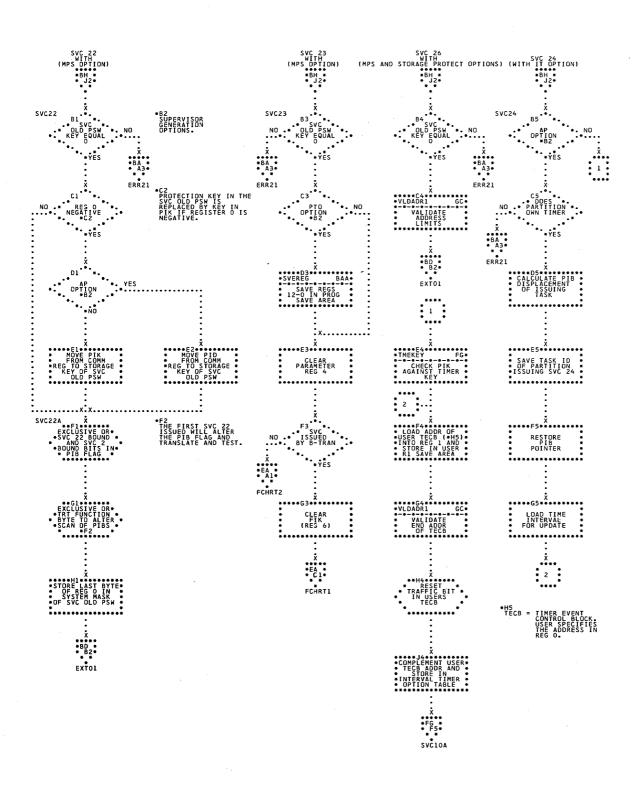


Chart FJ. \$\$A\$SUP1 - SGSVC Macro, Program Check Interrupt and SVCs 16 and 17 Refer to Charts 02 and 03.

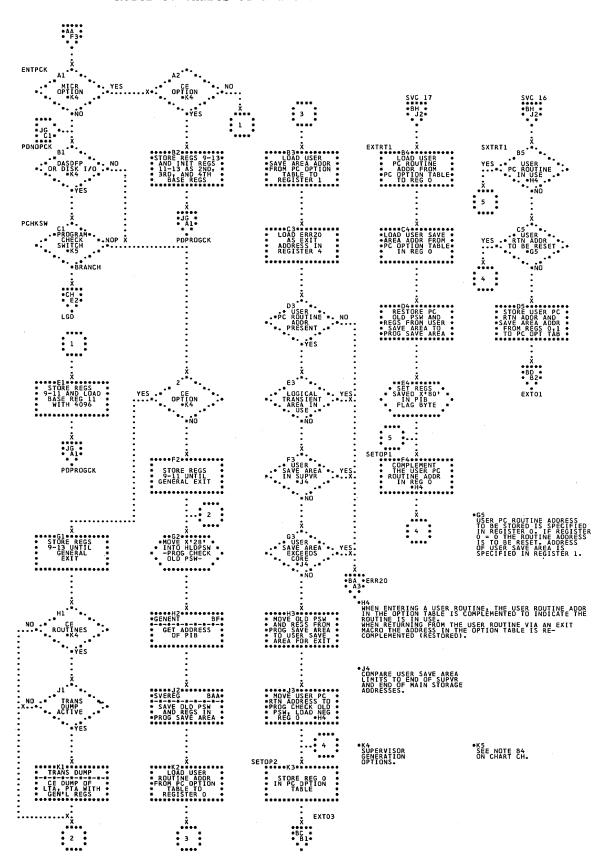


Chart FK. \$\$A\$SUP1 - SGSVC Macro, Program Check Interrupt Refer to Chart 02.

OPTIONS -- USER PC ROUTINE WITH (STORAGE PROTECT, INTERVAL TIMER, OR USER OC ROUTINE).

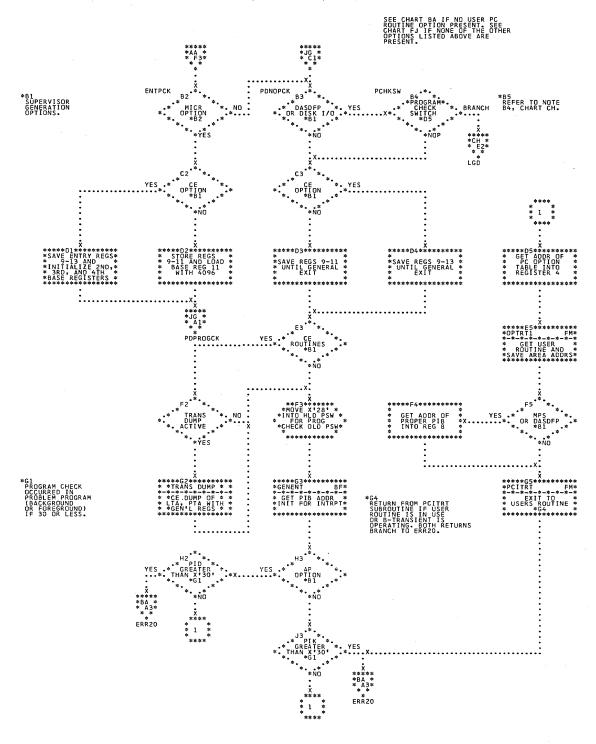


Chart FL. \$\$A\$SUP1 - SGSVC Macro, External Interrupt (Part 1 of 2) Refer to Chart 05.

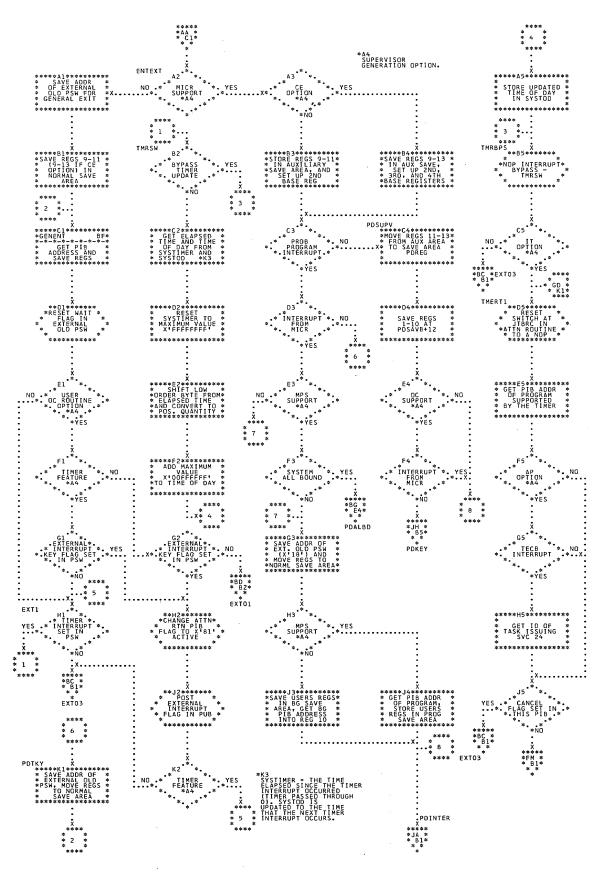
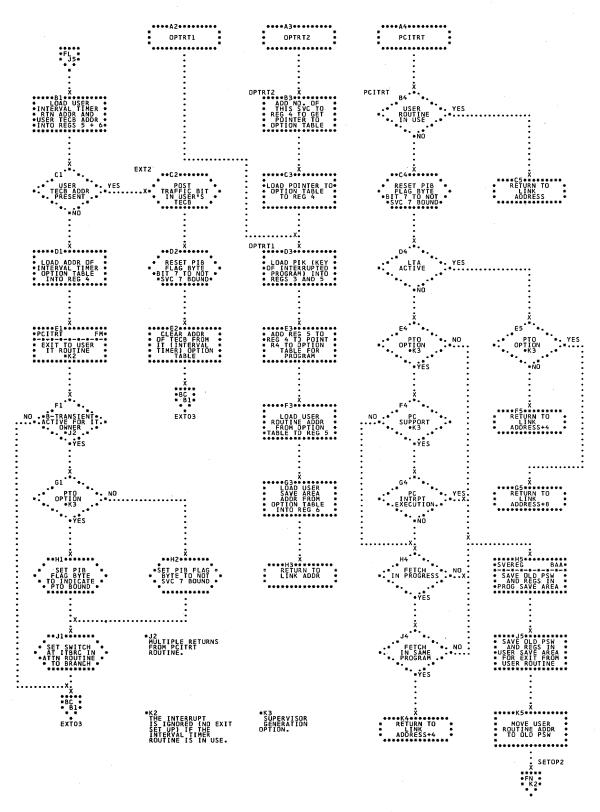


Chart FM. \$\$A\$SUP1 - SGSVC Macro, External Interrupt (Part 2 of 2) and External Interrupt Subroutines
Refer to Chart 05.



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Chart FN. \$\$A\$SUP1 - SGSVC Macro, Program Check Interrupt (SVCs 16 through 21 with Options)

Refer to Chart 03.

OPTIONS -- USER PC ROUTINE WITH (STORAGE PROTECT, INTERVAL TIMER, OR USER OC ROUTINE). *B1

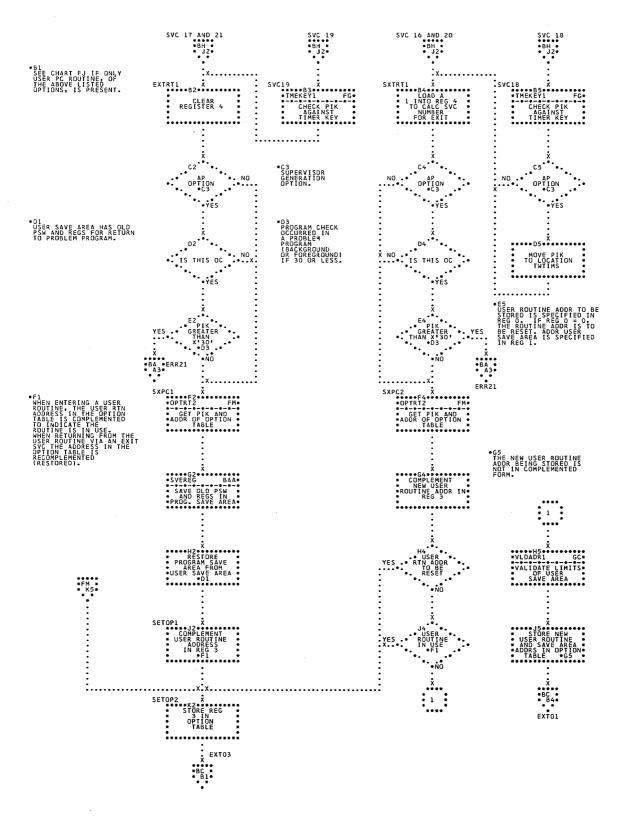
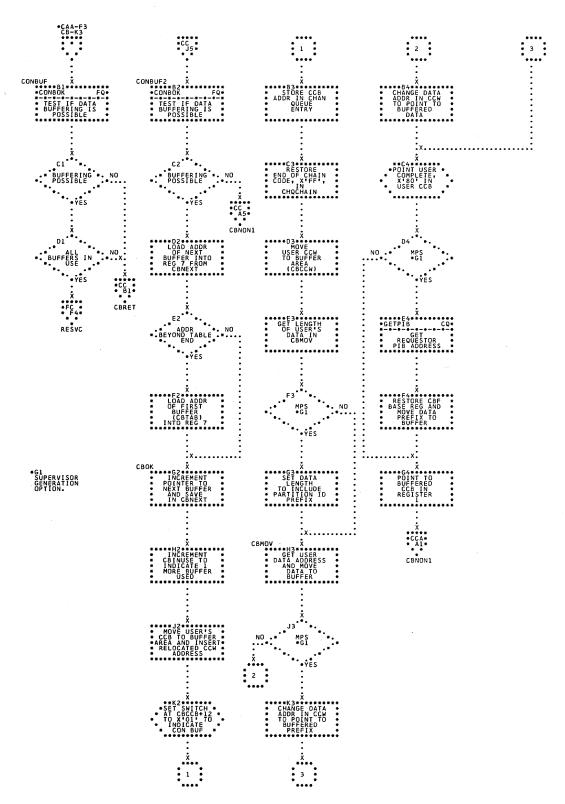


Chart FP. \$\$A\$SUP1 - SGSVC Macro, Console Buffering Routine (Part 1 of 2) Refer to Chart 04.



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Chart FQ. \$\$A\$SUP1 - SGSVC Macro, Console Buffering Routine (Part 2 of 2) Refer to Chart 04.

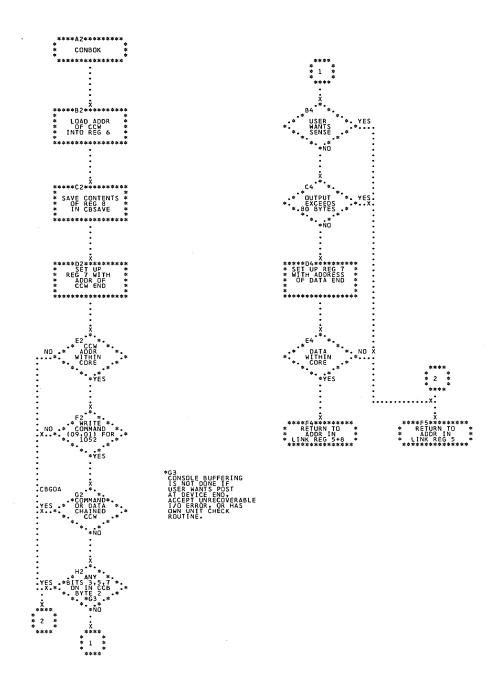


Chart FR. \$\$A\$SUP1 - SGSVC Macro, SVCs 43 and 45 Refer to Chart 03.

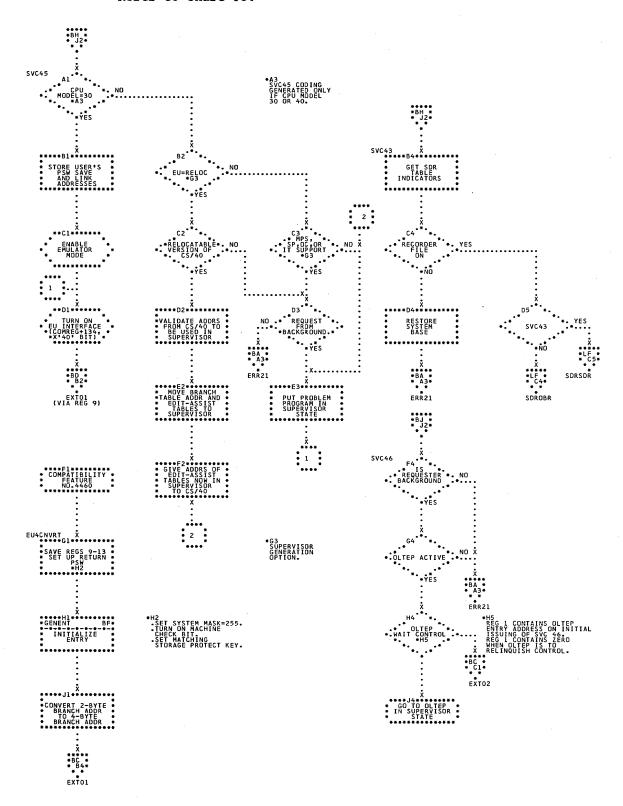
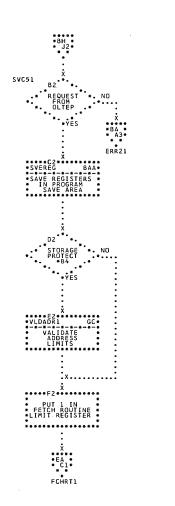
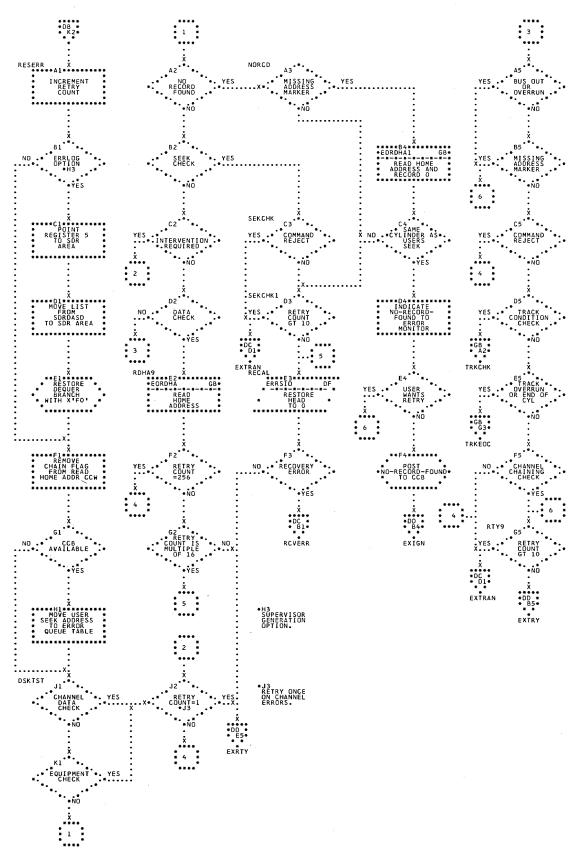


Chart FS. \$\$A\$SUP1 - SGSVC Macro, SVC 51 Refer to Chart 03.



*B4 SUPERVISOR GENERATION OPTION.

Chart GA. \$\$A\$SUP1 - SGDSK Macro, Disk Error Recovery (Part 1 of 2) Refer to Chart 06.



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Chart GB. \$\$A\$SUP1 - SGDSK Macro, Disk Error Recovery (Part 2 of 2) Refer to Chart 06.

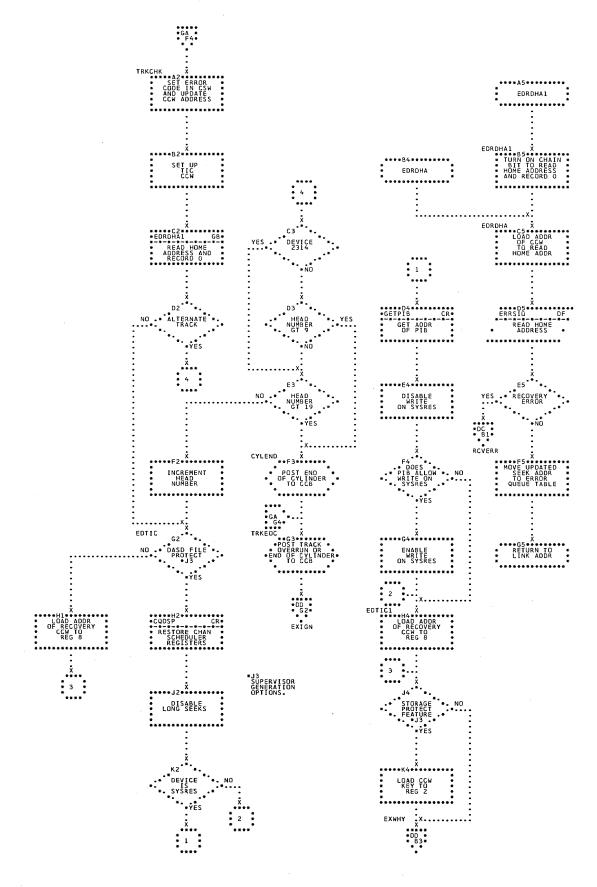


Chart GC. \$\$A\$SUP1 - SGTCON Macro, VLDADR Subroutine Refer to Chart 02.

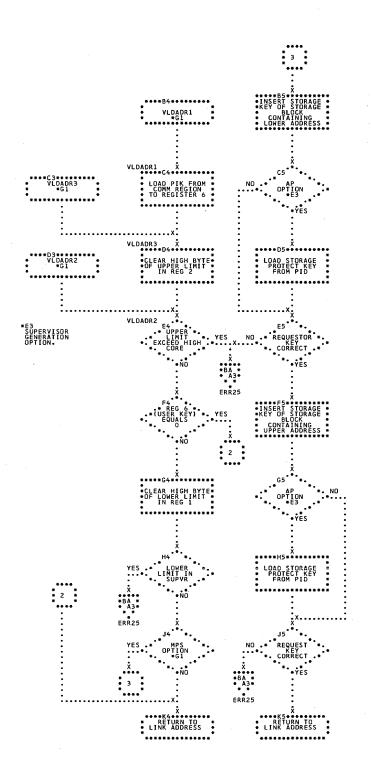


Chart GD. \$\$A\$SUP1 - SGTCON Macro, Resident Attention Subroutine Refer to Chart 02.

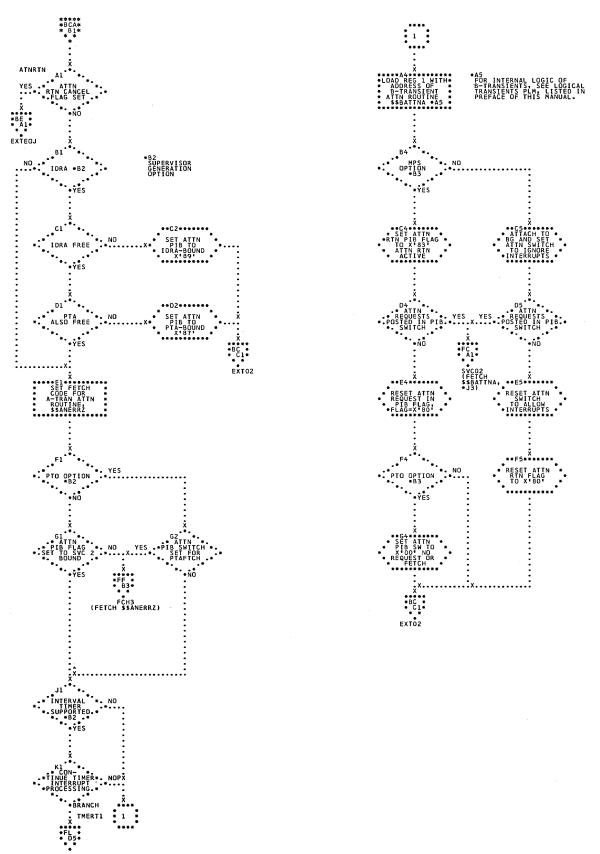


Chart HA. \$\$A\$SUP1 - MCRAS Macro, Resident Machine Check Handler Refer to Chart 08.

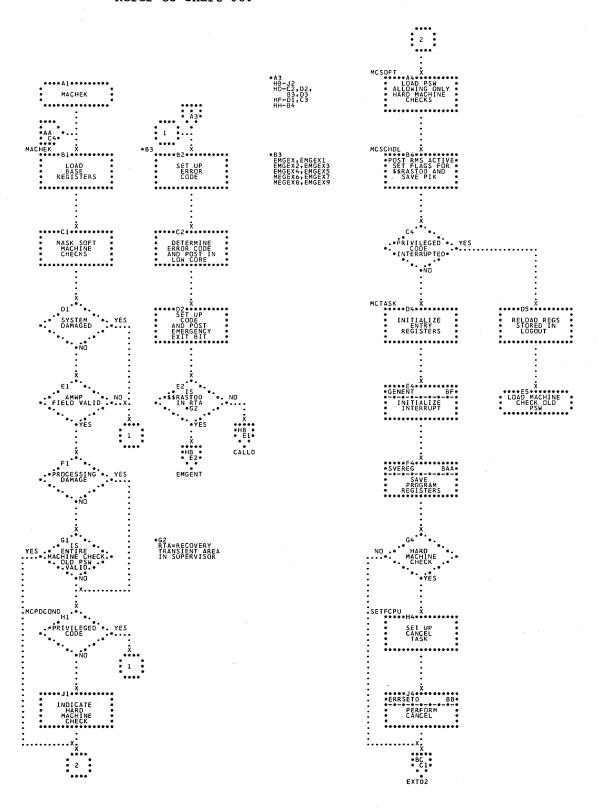


Chart HB. \$\$A\$SUP1 - MCRAS Macro, RAS Monitor (Part 1 of 2) Refer to Chart 09.

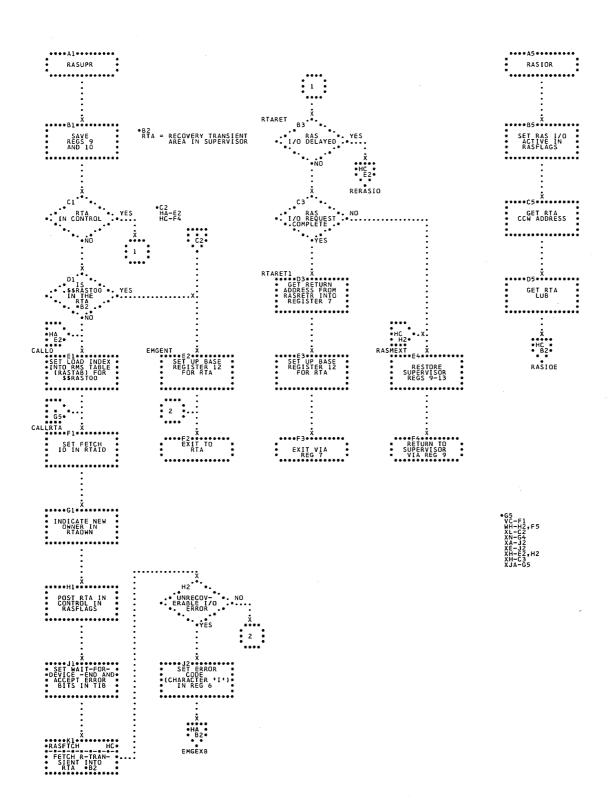
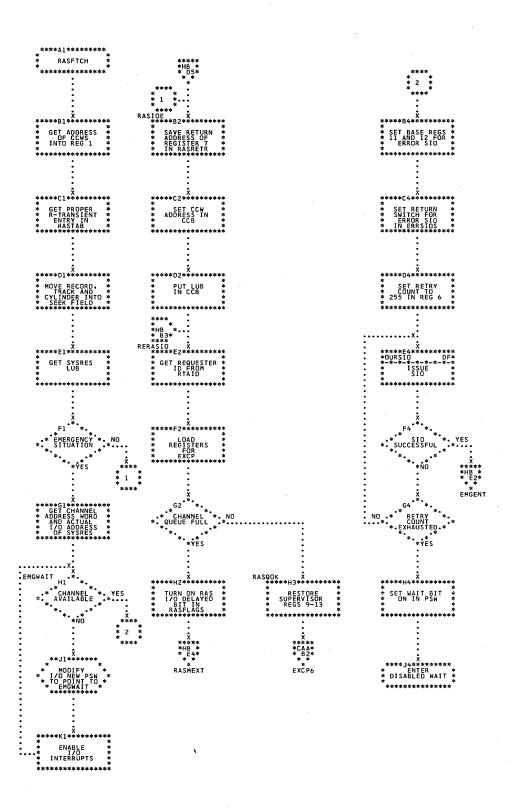


Chart HC. \$\$A\$SUP1 - MCRAS Macro, RAS Monitor (Part 2 of 2) Refer to Chart 09.



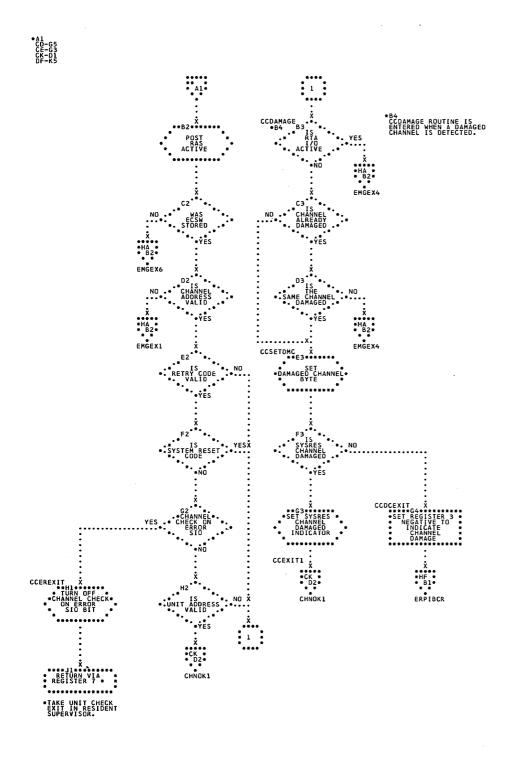


Chart HE. \$\$A\$SUP1 - MCRAS Macro, Resident Channel Check Handler (Part 2 of 4) Refer to Chart 09.

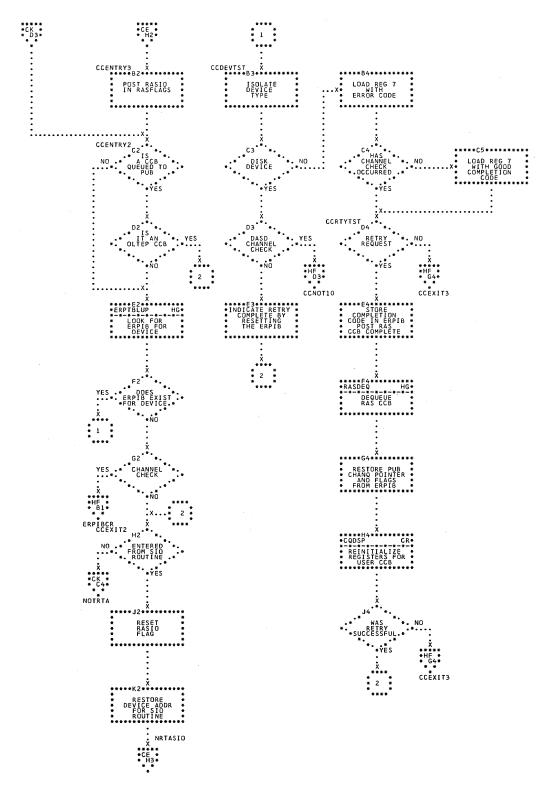


Chart HF. \$\$A\$SUP1 - MCRAS Macro, Resident Channel Check Handler (Part 3 of 4) Refer to Chart 09.

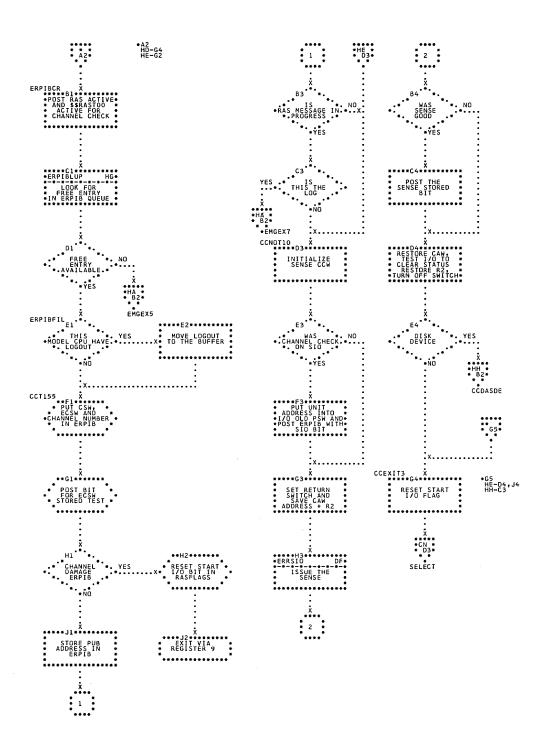


Chart HG. \$\$A\$SUP1 - MCRAS Macro, Resident Channel Check Handler (Part 4 of 4)
Refer to Chart 09.

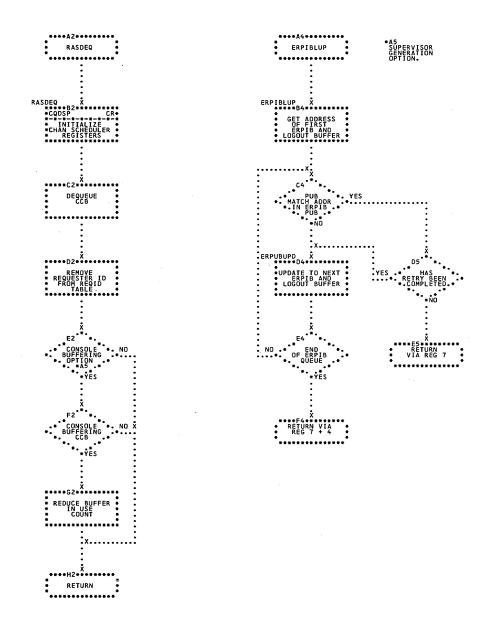


Chart HH. \$\$A\$SUP1 - MCRAS Macro, DASD Channel Check Handler Refer to Chart 08.

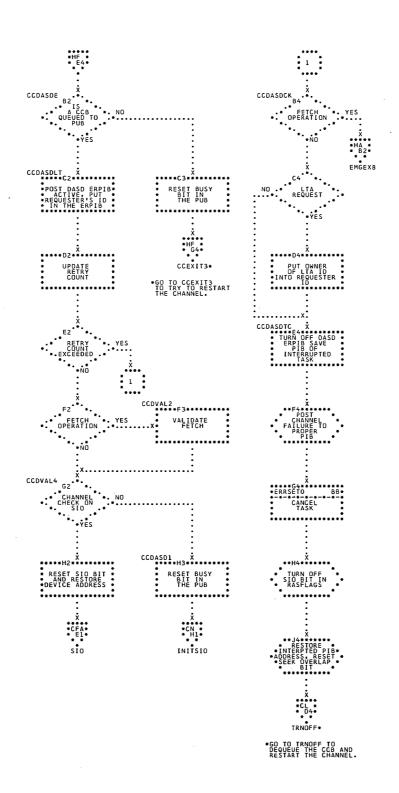
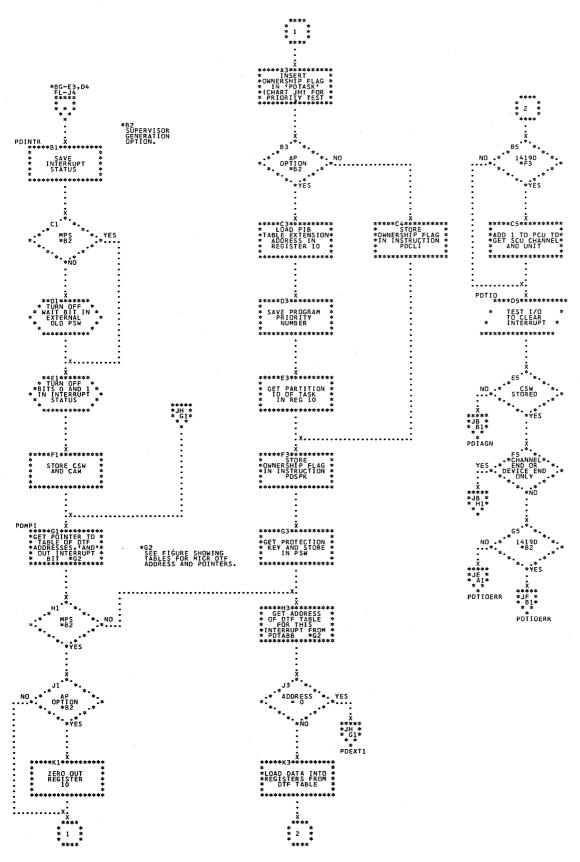


Chart JA. \$\$A\$SUP1 - SMICR Macro, External Interrupt (Part 1 of 3) Refer to Chart 05.



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Chart JB. \$\$A\$SUP1 - SMICR Macro, External Interrupt (Part 2 of 3) Refer to Chart 05.

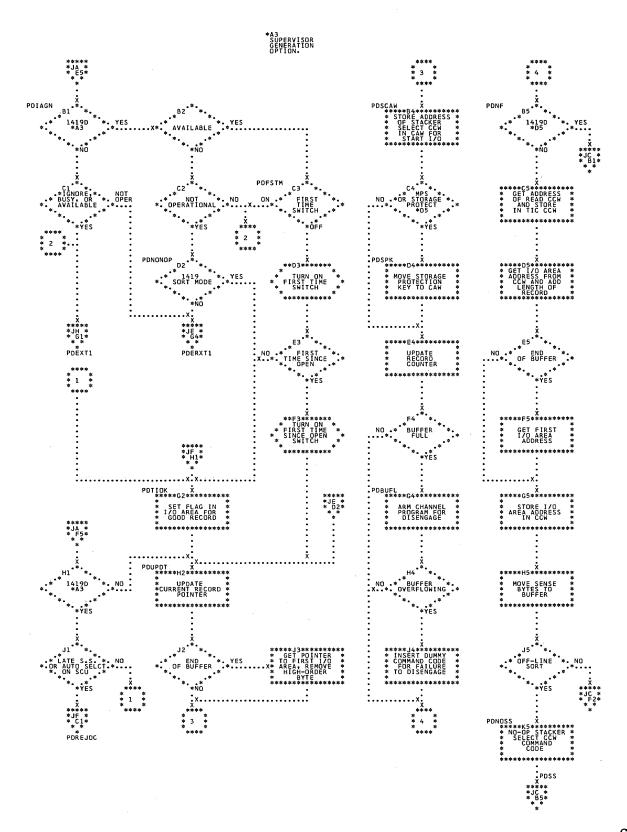
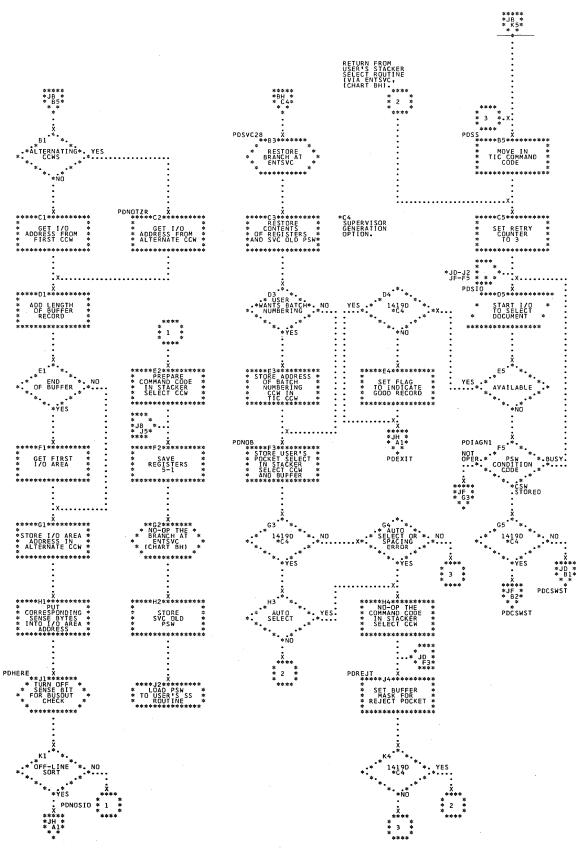


Chart JC. \$\$A\$SUP1 - SMICR Macro, External Interrupt (Part 3 of 3)
Refer to Chart 05.



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Chart JD. \$\$A\$SUP1 - SMICR Macro, ERP for 1412/1419 Start I/O Refer to Chart 05.

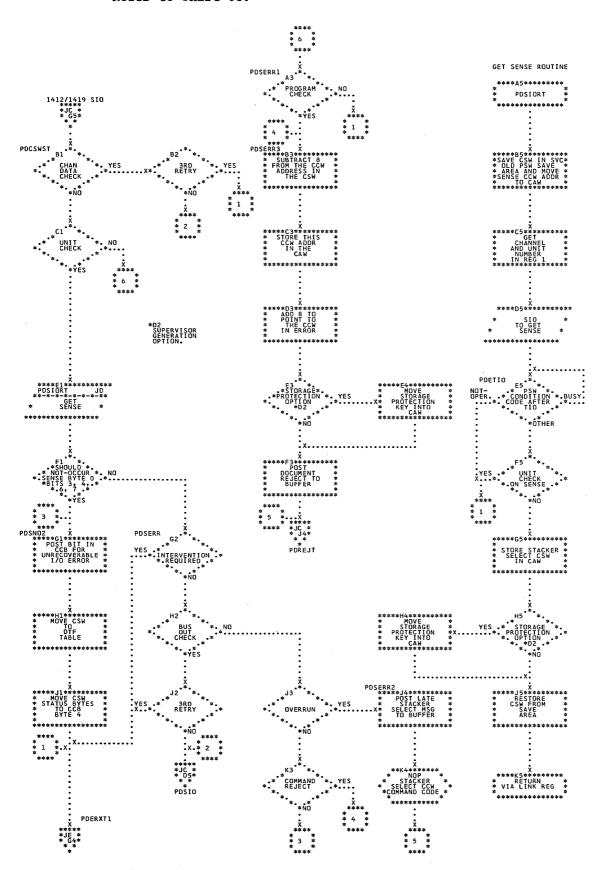
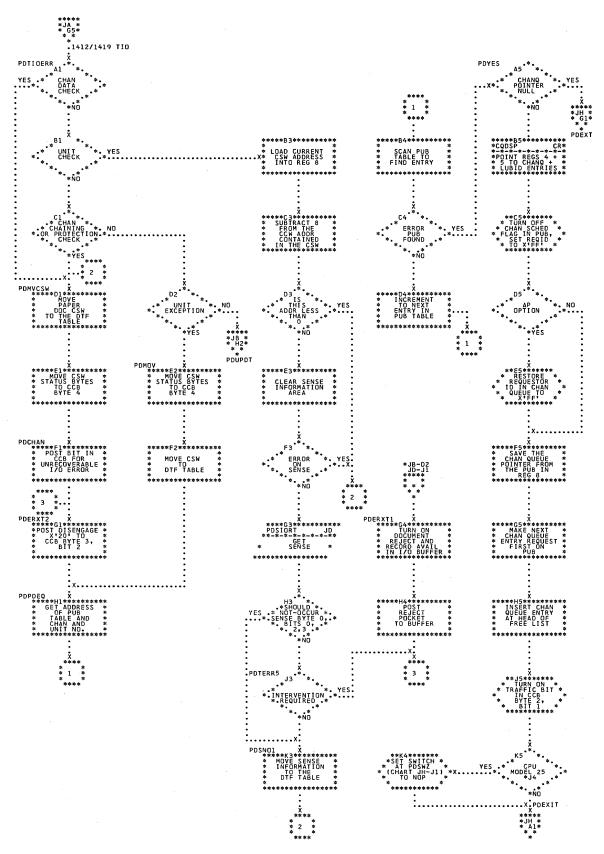


Chart JE. \$\$A\$SUP1 - SMICR Macro, ERP for 1412/1419 Test I/O Refer to Chart 05.



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Chart JF. \$\$A\$SUP1 - SMICR Macro, ERP for 1419D SIO and TIO Refer to Chart 05.

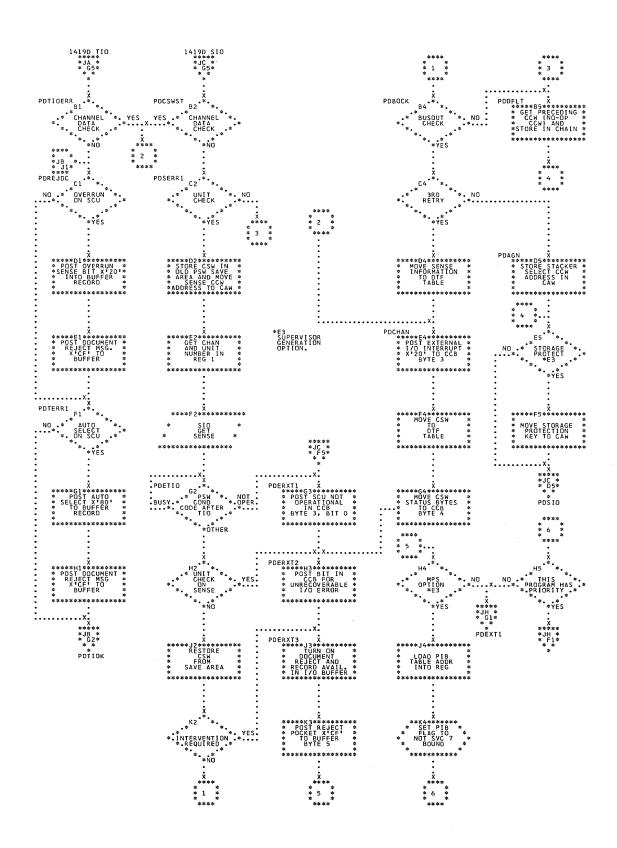


Chart JG. \$\$A\$SUP1 - SMICR Macro, Program Check Interrupt Refer to Chart 02.

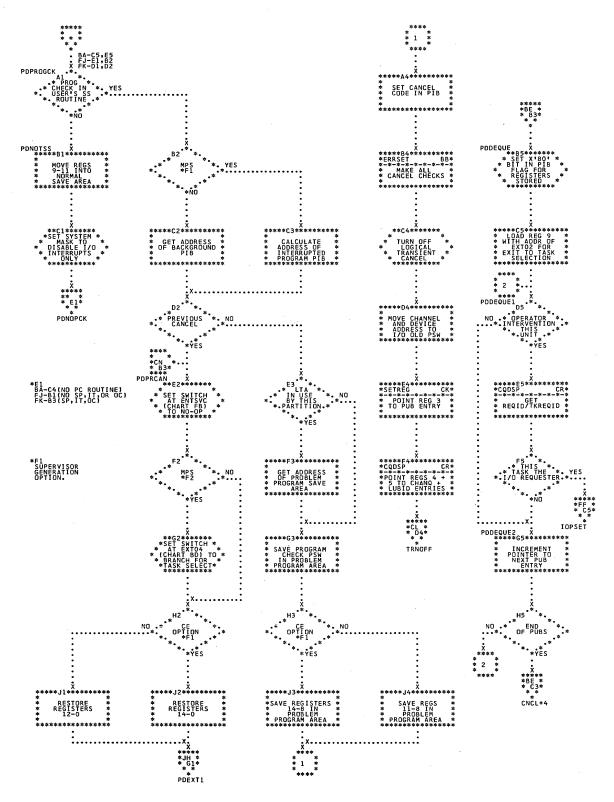


Chart JH. \$\$A\$SUP1 - SMICR Macro, Exit Routine Refer to Chart 02.

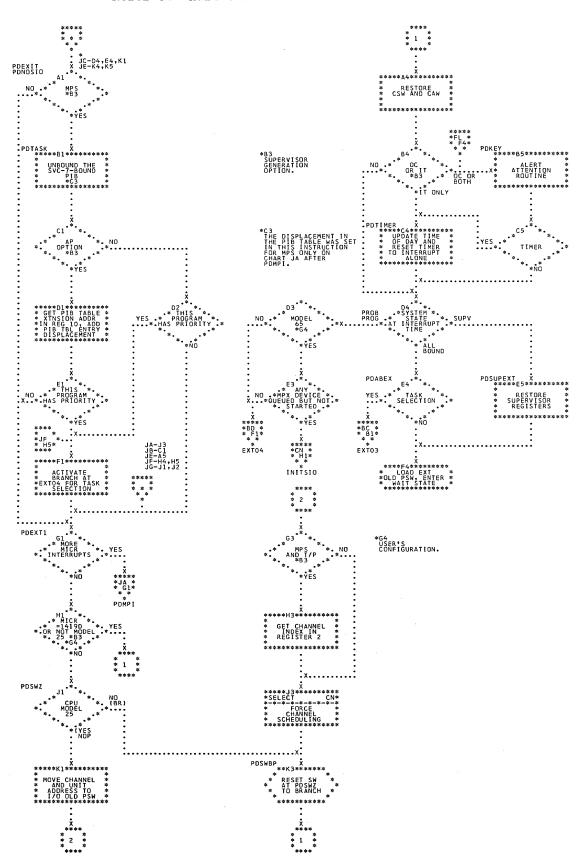


Chart KA. \$\$A\$SUP1 - SMCRR Macro, Channel Inboard Error Record Builder (Part 1 of 4)
Refer to Chart 10.

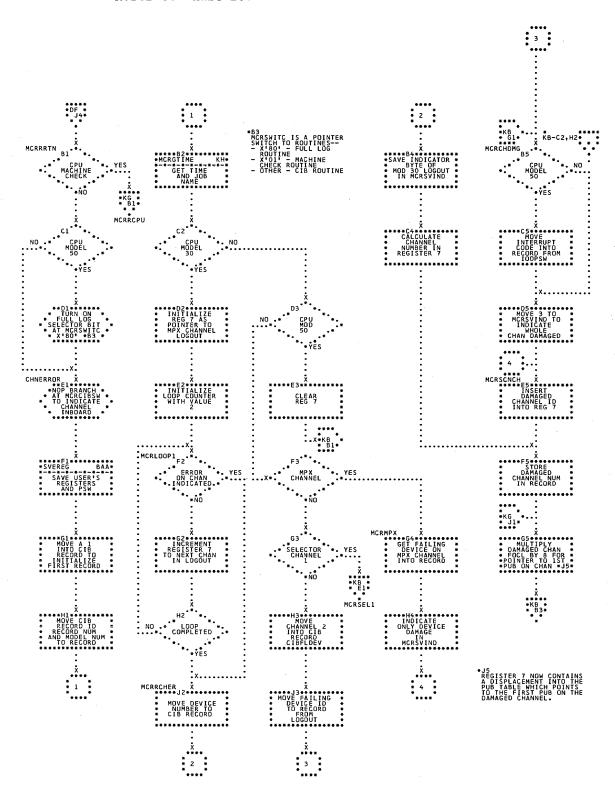


Chart KB. \$\$A\$SUP1 - SMCRR Macro, Channel Inboard Error Record Builder (Part 2 of 4)
Refer to Chart 10.

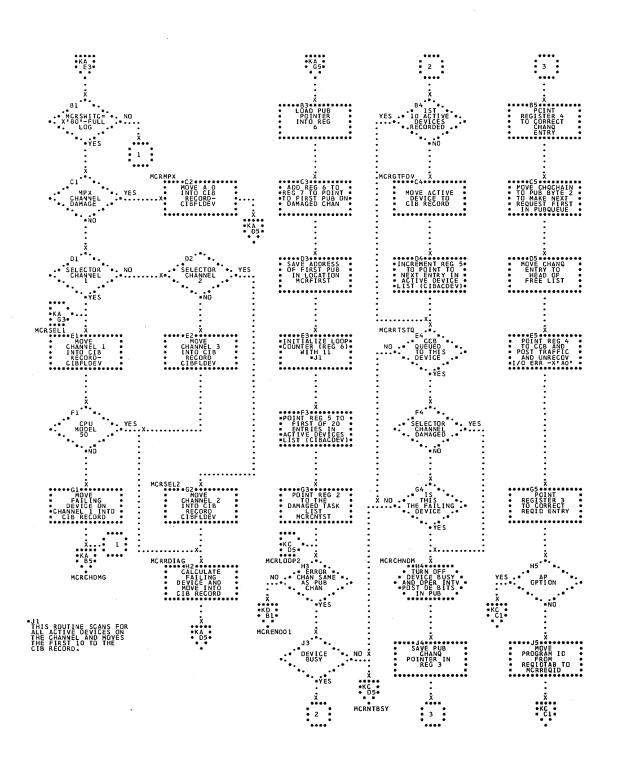
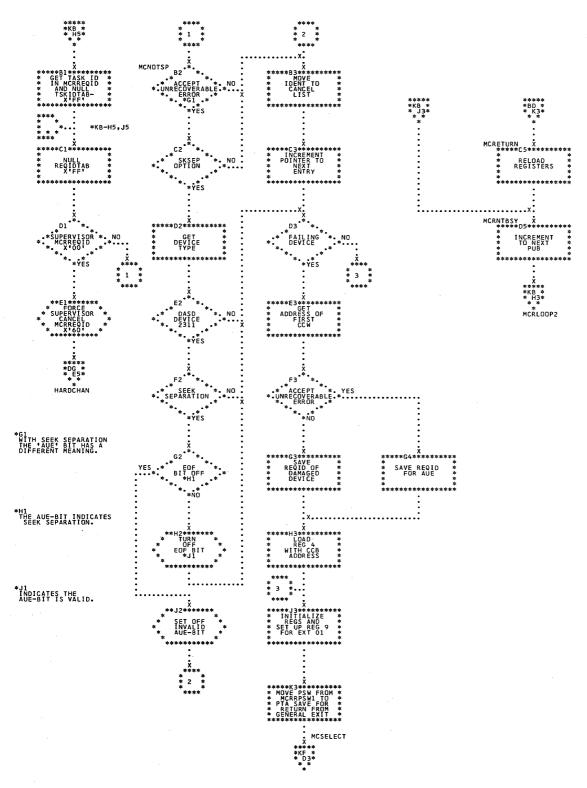


Chart KC. \$\$A\$SUP1 - SMCRR Macro, Channel Inboard Error Record Builder (Part 3 of 4)
Refer to Chart 10.



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Chart KD. \$\$A\$SUP1 - SMCRR Macro, Channel Inboard Error Record Builder (Part 4 of 4)
Refer to Chart 10.

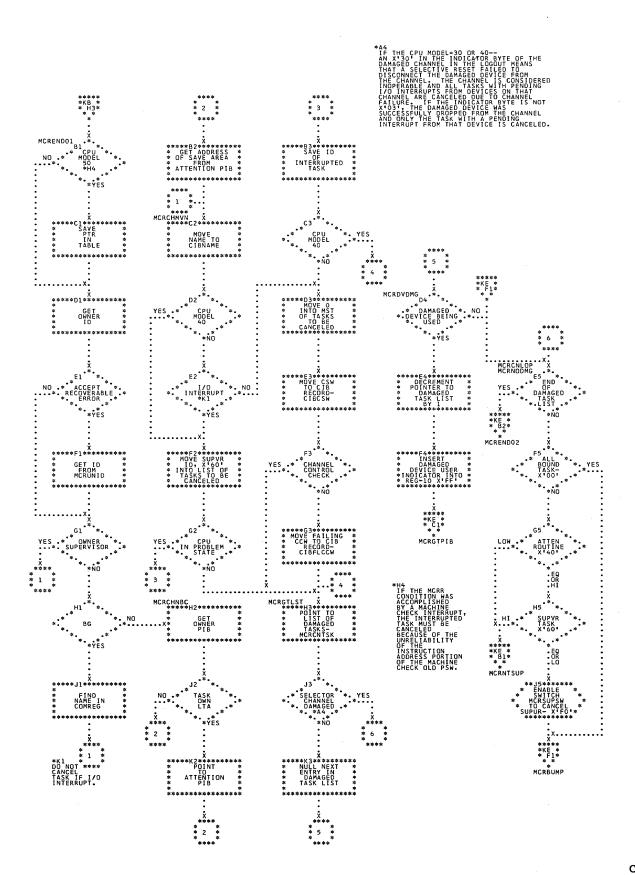
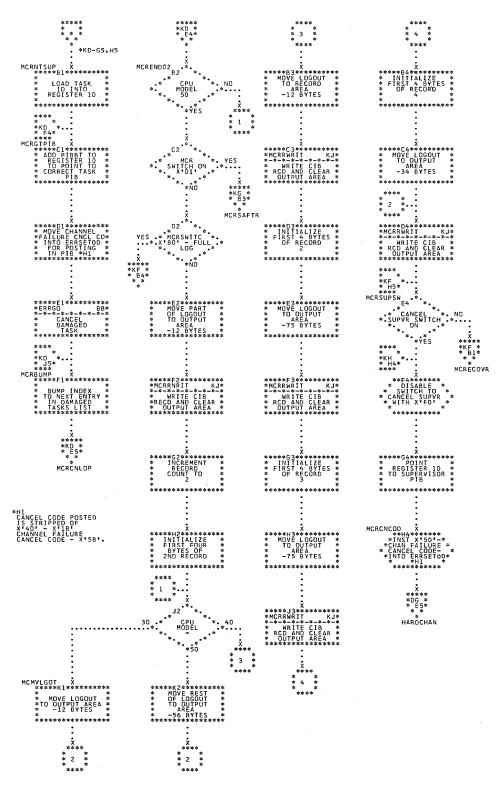


Chart KE. \$\$A\$SUP1 - SMCRR Macro, Write CIB Record Refer to Chart 10.



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Chart KF. \$\$A\$SUP1 - SMCRR Macro, MCRR Exit Routine Refer to Chart 10.

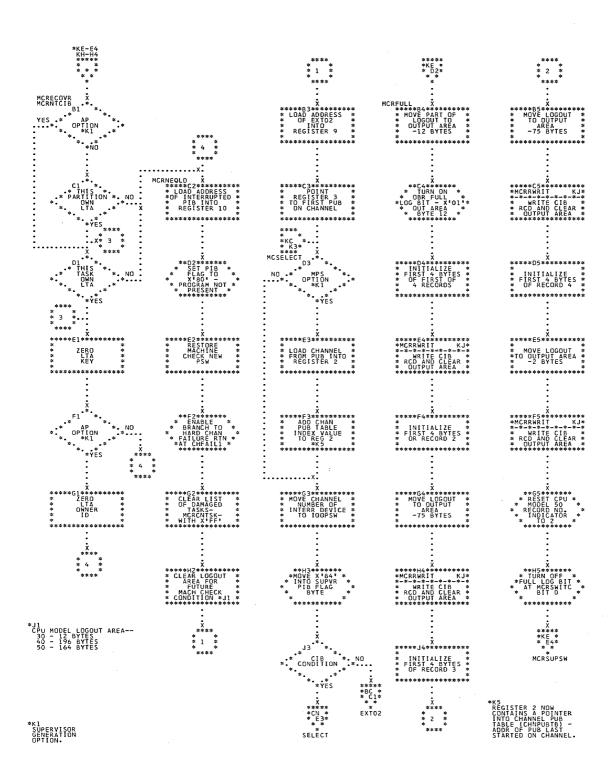
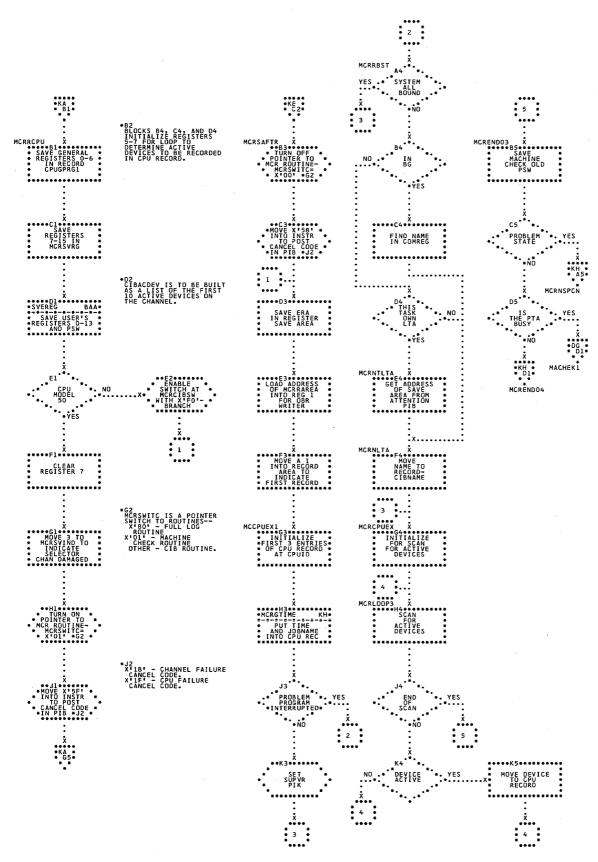


Chart KG. \$\$A\$SUP1 - SMCRR Macro, Machine Check Error Record Builder Refer to Chart 10.



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Chart KH. \$\$A\$SUP1 - SMCRR Macro, Write Machine Check Record Refer to Chart 10.

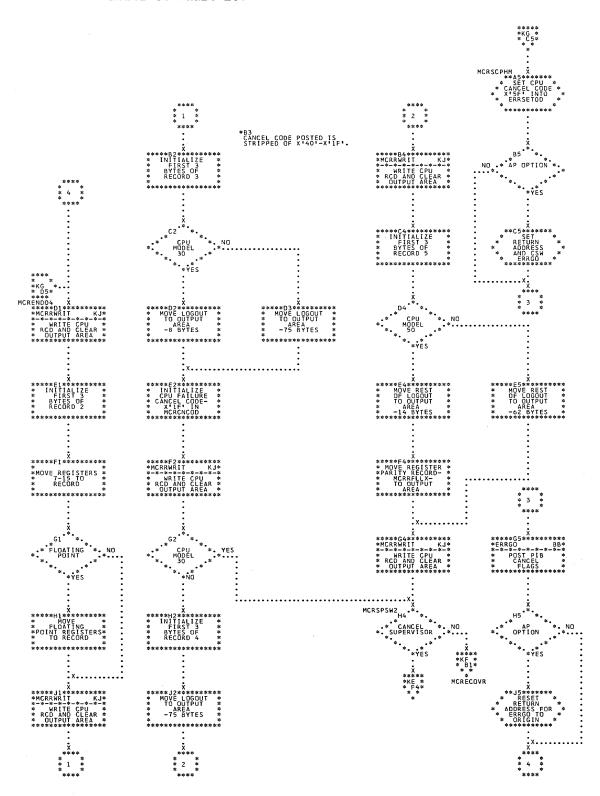


Chart KJ. \$A\$SUP1 - SMCRR Macro, MCRGTIME and MCRRWRIT Subroutines Refer to Chart 10.

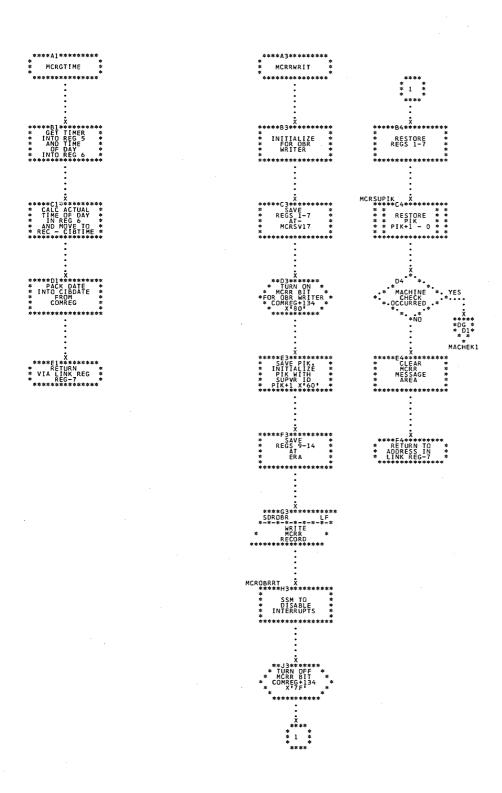


Chart LA. \$\$A\$SUP1 - SEND Macro, Exit to System Message Writer or Task Selection and TP Routines
Refer to Chart 10.

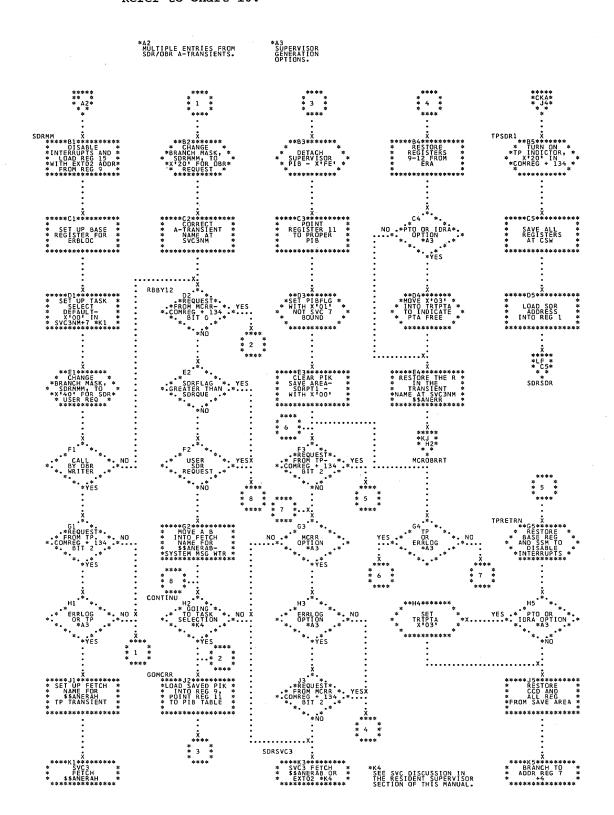


Chart LB. \$\$A\$SUP1 - SEND Macro, Routines to Test SDR Error Queue and to Schedule SDR Update of Internal Counters

Refer to Chart 10.

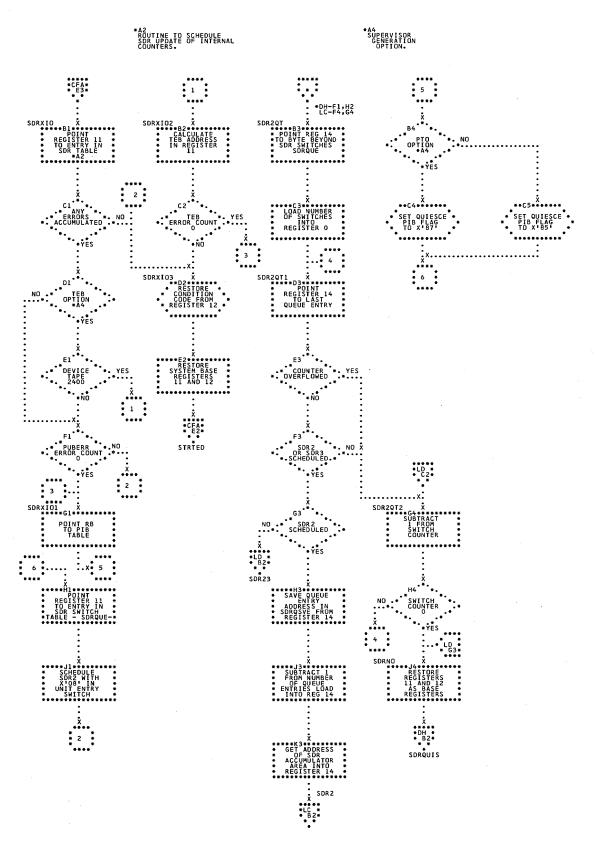


Chart LC. \$\$A\$SUP1 - SEND Macro, Update SDR Half-Byte Counters and Schedule Recorder File Update
Refer to Chart 10.

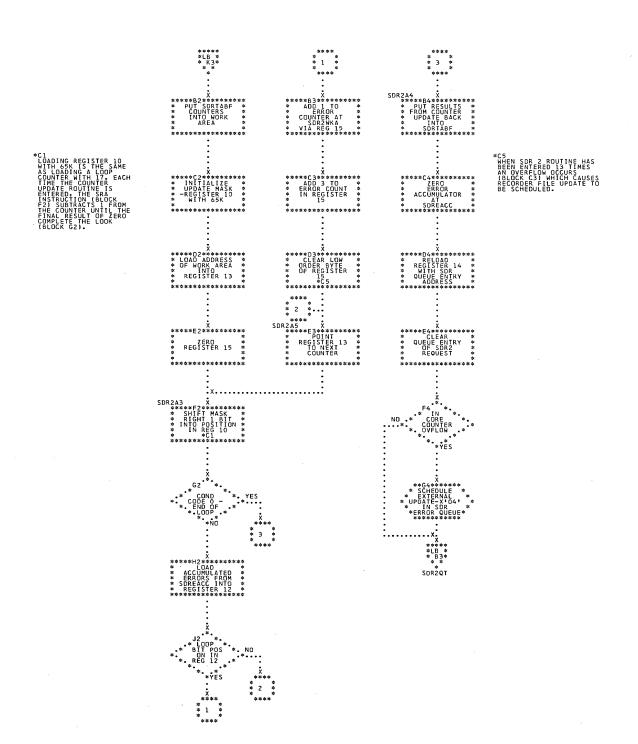


Chart LD. \$\$A\$SUP1 - SEND Macro, Gather Update Information and Fetch Writer Refer to Chart 10.

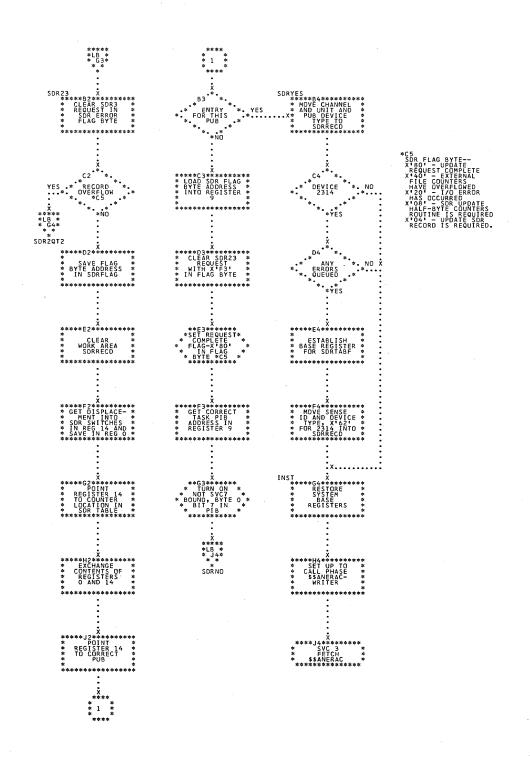


Chart LE. \$\$A\$SUP1 - SEND Macro, Interpretive Error Accumulator Refer to Chart 10.

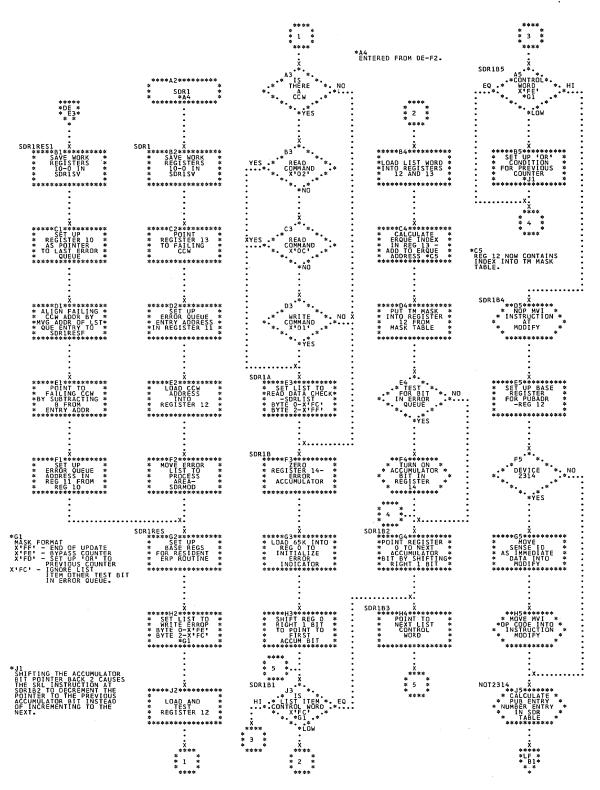


Chart LF. \$\$A\$SUP1 - SEND Macro, Call OBR/SDR Writers and Routines for OBR/SDR Requests (Part 1 of 2)
Refer to Chart 10.

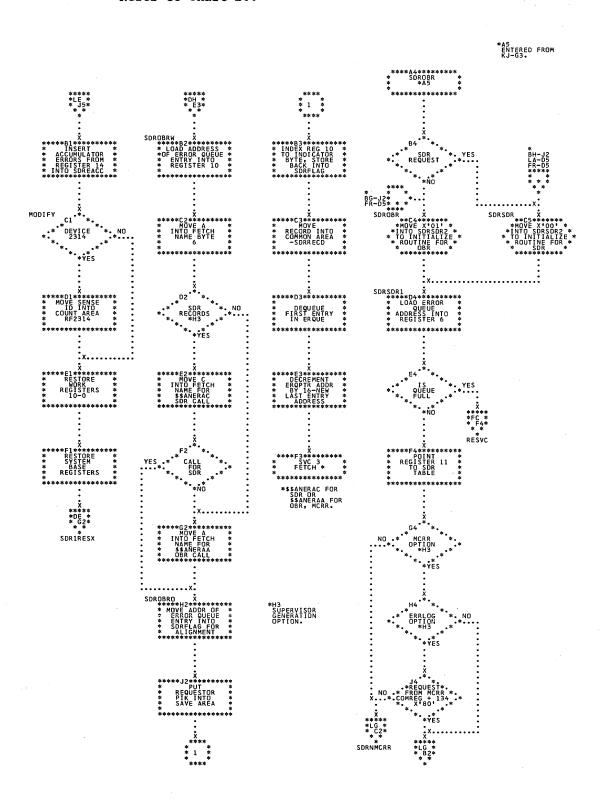


Chart LG. \$\$A\$SUP1 - SEND Macro, Routines for OBR/SDR Requests (Part 2 of 2) Refer to Chart 10.

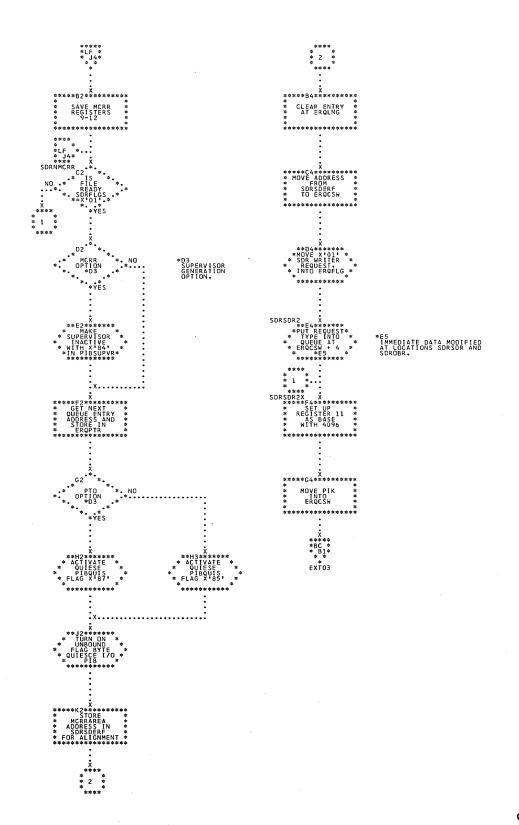


Chart LH. \$\$A\$SUP1 - SEND Macro, LTA Subroutine

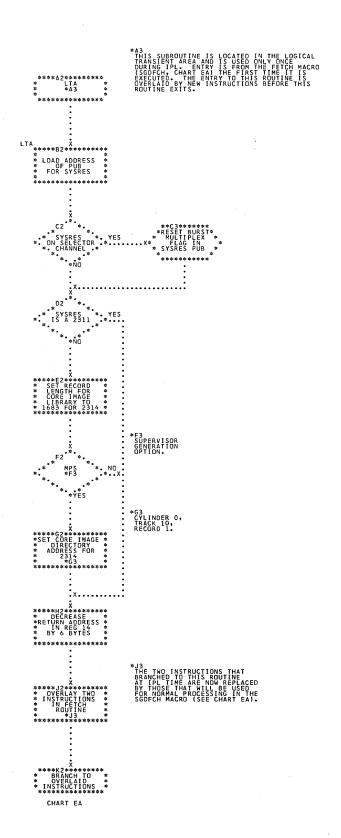


Chart MA. \$\$A\$SUP1 - SGTHAP Macro, Track HOLD Refer to Chart 03.

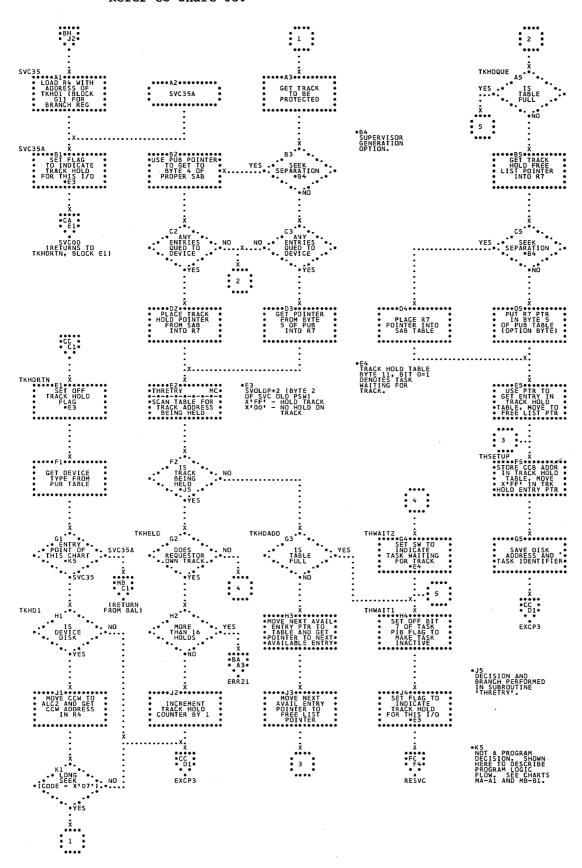
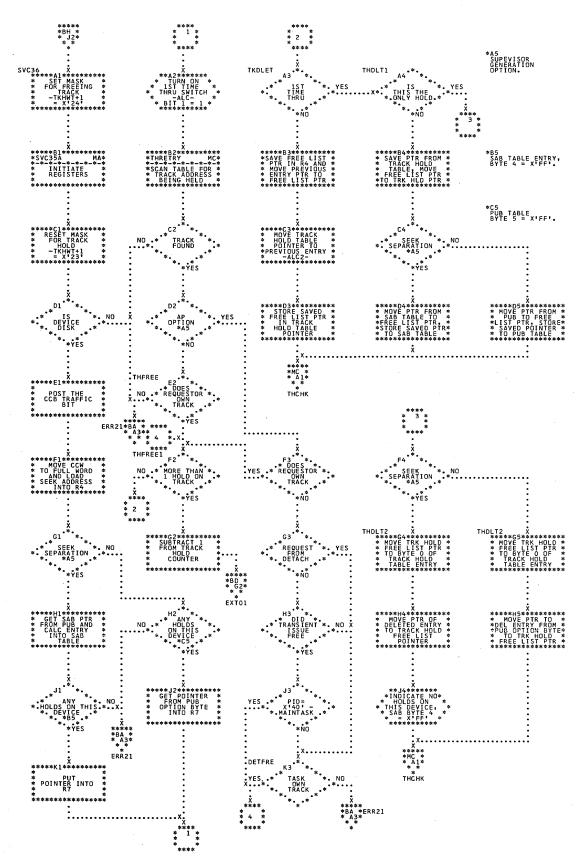


Chart MB. \$\$A\$SUP1 - SGTHAP Macro, FREE Track (Part 1 of 2) Refer to Chart 03.



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Chart MC. \$\$A\$SUP1 - SGTHAP Macro, FREE Track (Part 2 of 2), THRETRY Subroutine, and AB STXIT

Refer to Chart 03.

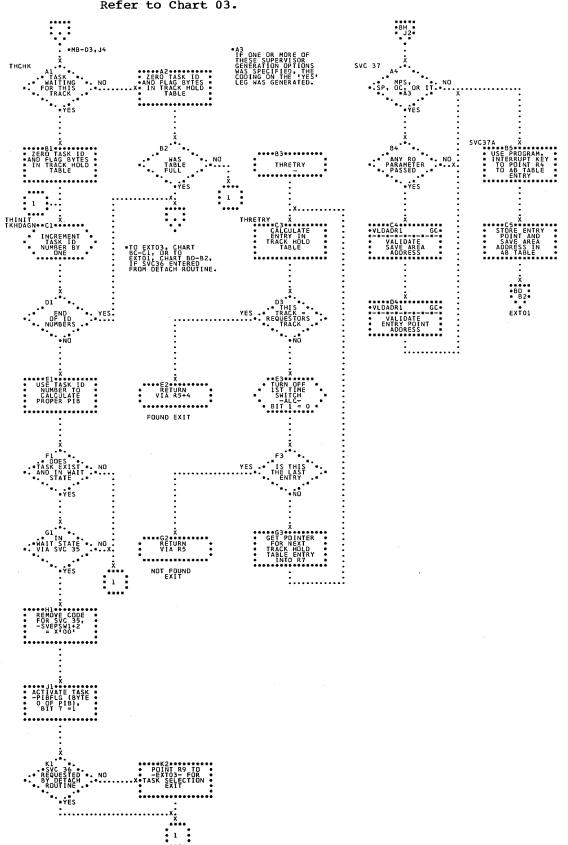
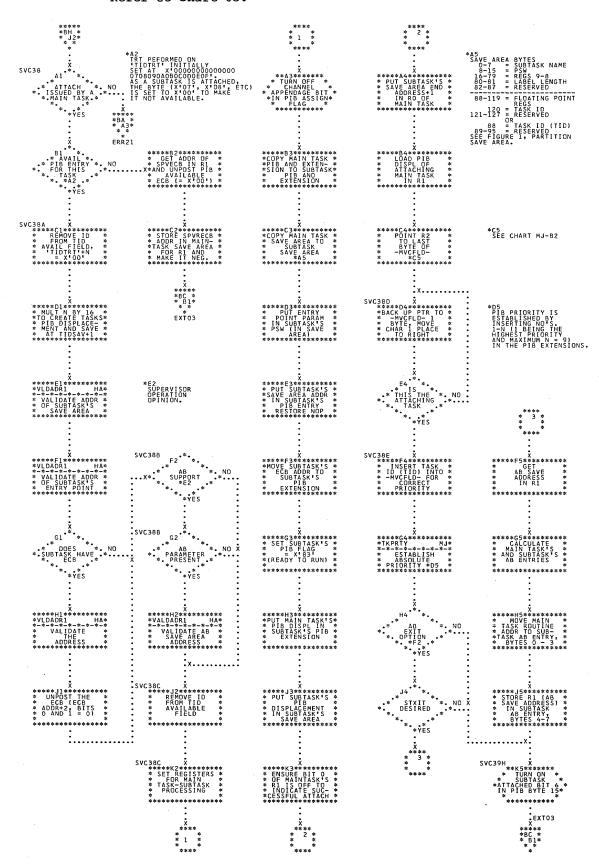


Chart MD. \$\$A\$SUP1 - SGTHAP Macro, ATTACH a Task Refer to Chart 03.



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Chart ME. \$\$A\$SUP1 - SGTHAP Macro, DETACH a Task (Part 1 of 2) Refer to Chart 03.

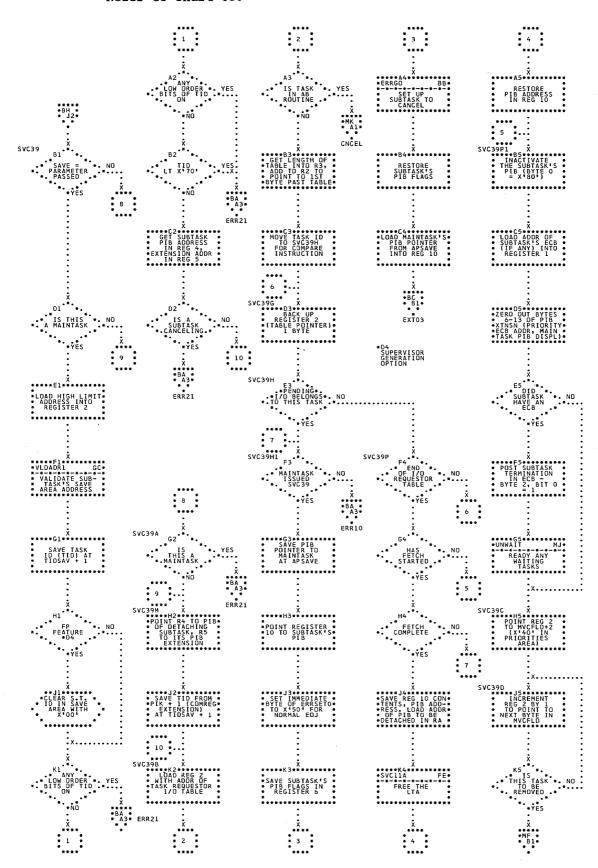
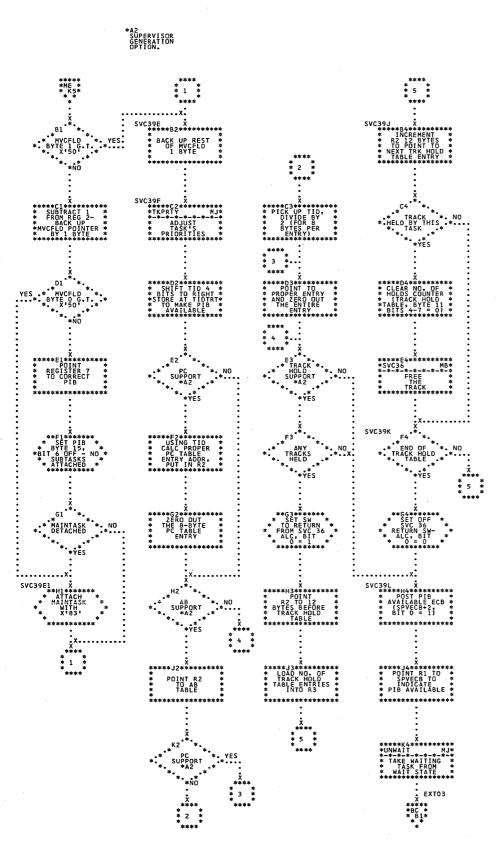


Chart MF. \$\$A\$SUP1 - SGTHAP Macro, DETACH a Task (Part 2 of 2) Refer to Chart 03.



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Chart MG. \$\$A\$SUP1 - SGTHAP Macro, POST a Completed Event and ENQ a Resource Refer to Chart 03.

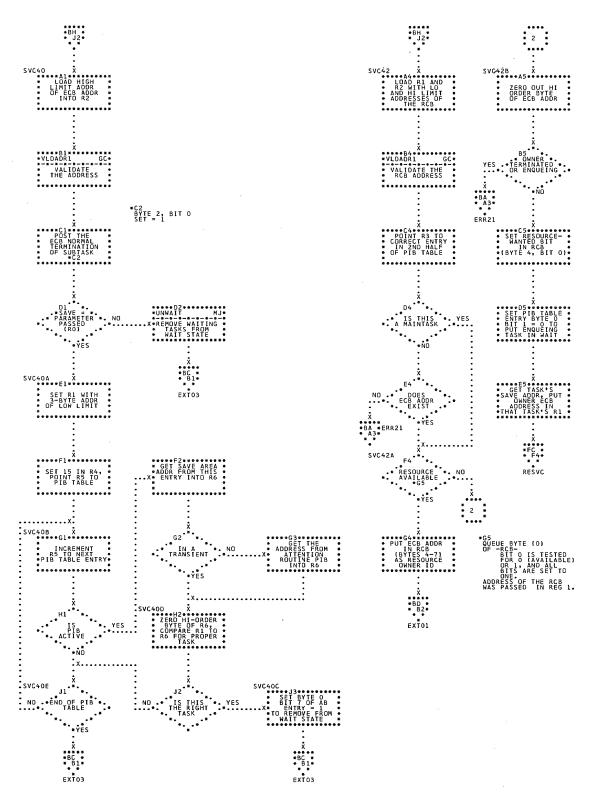
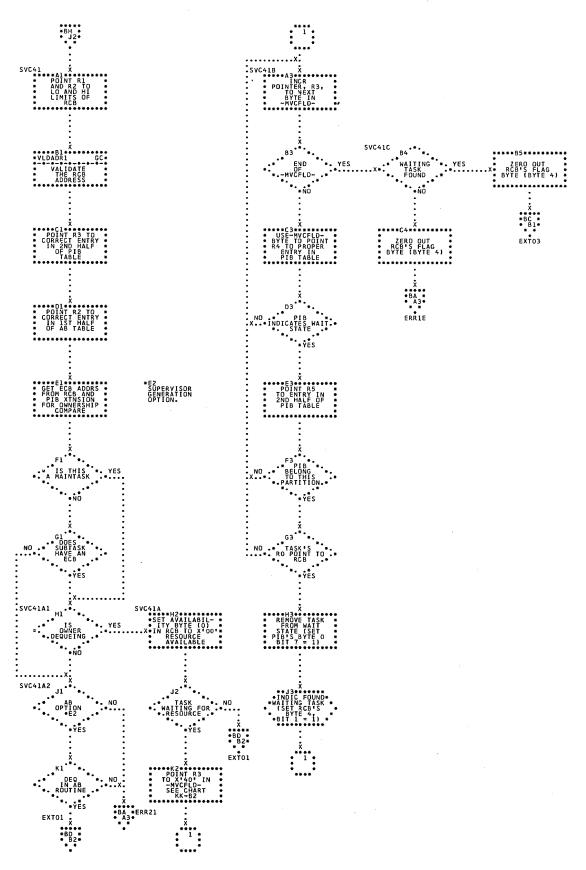


Chart MH. \$\$A\$SUP1 - SGTHAP Macro, DEQ a Resource Refer to Chart 03.



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Chart MJ. \$\$A\$SUP1 - SGTHAP Macro, Task Priority and UNWAIT Subroutines Refer to Chart 03.

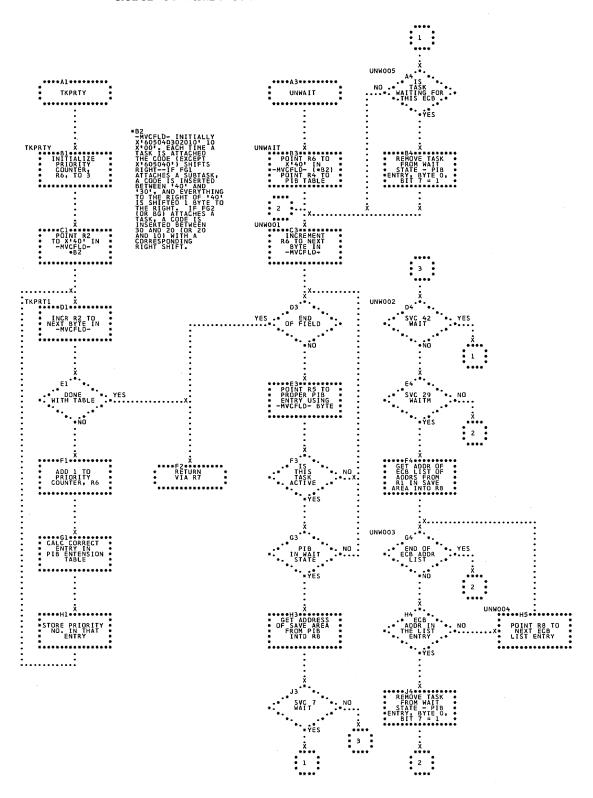
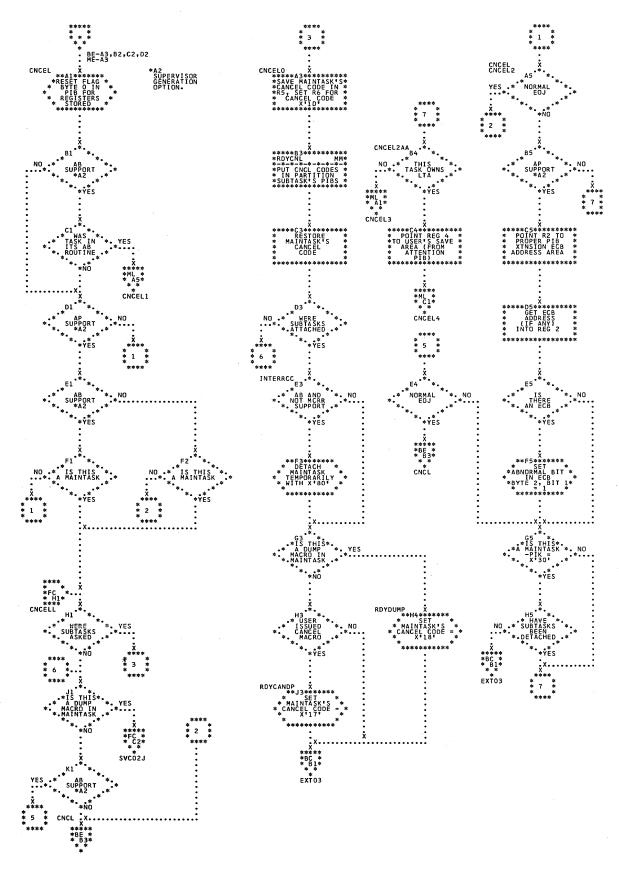


Chart MK. \$\$A\$SUP1 - SGTHAP Macro, Task Termination Handling (Part 1 of 2) Refer to Chart 01.



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Chart ML. \$\$A\$SUP1 - SGTHAP Macro, Task Termination Handling (Part 2 of 2) Refer to Chart 01.

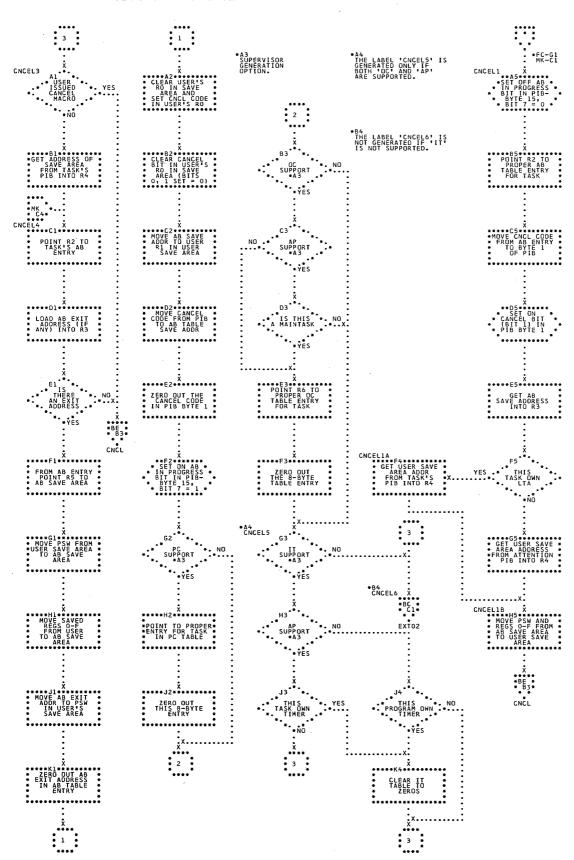
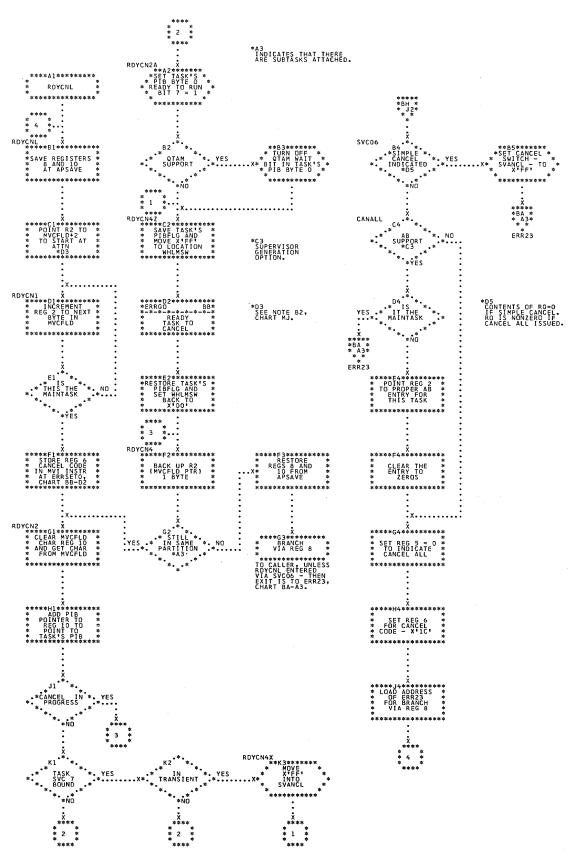
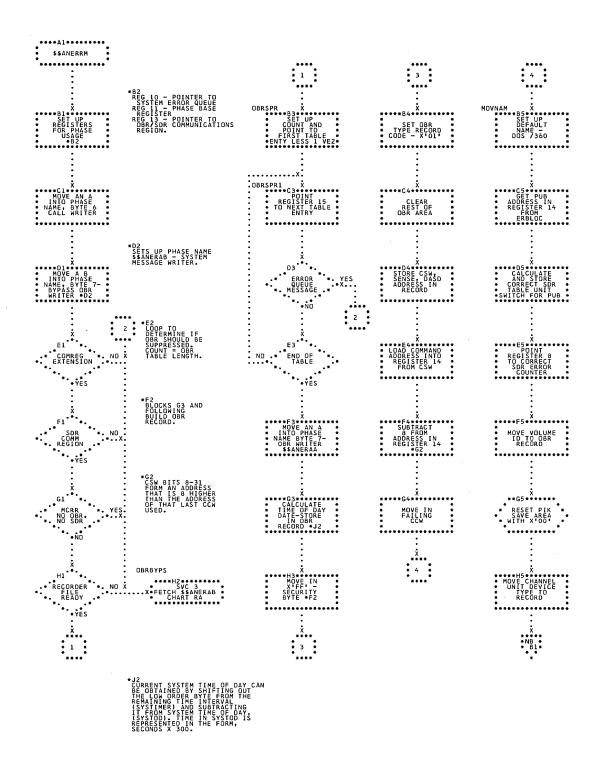


Chart MM. \$\$A\$SUP1 - SGTHAP Macro, RDYCNL Subroutine and CANCEL ALL Processing Refer to Chart 01.



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Chart NA. \$\$ANERRM - OBR Record Builder (Part 1 of 2) Refer to Chart 13.



\$\$ANERRM - OBR Record Builder (Part 2 of 2) Chart NB. Refer to Chart 13.

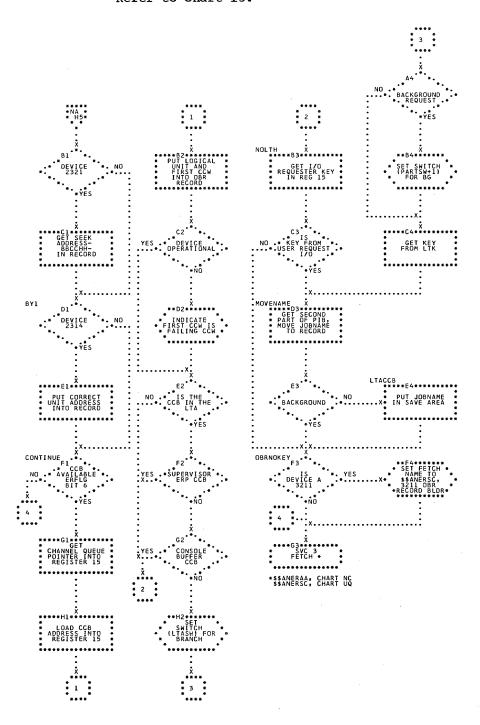
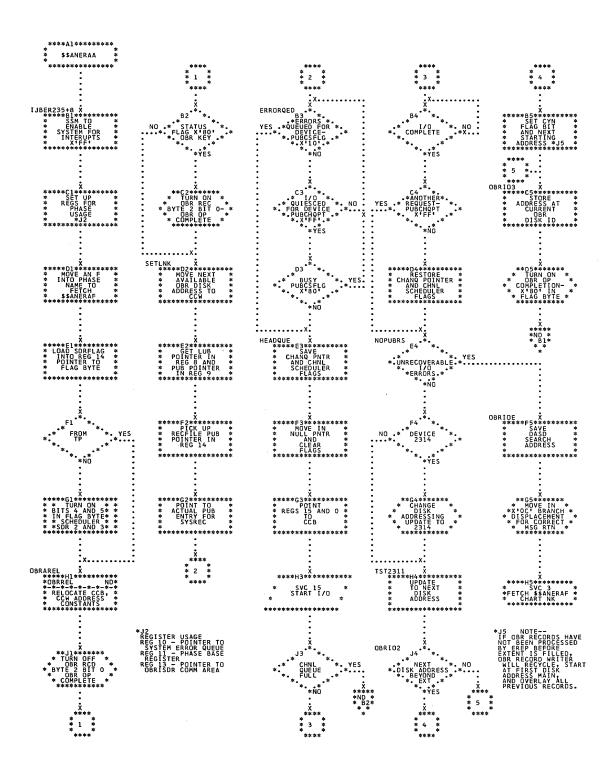


Chart NC. \$\$ANERAA - OBR/MCRR Record Writer (Part 1 of 2) Refer to Chart 13.



\$\$ANERAA - OBR/MCRR Record Writer (Part 2 of 2) Chart ND. Refer to Chart 13.

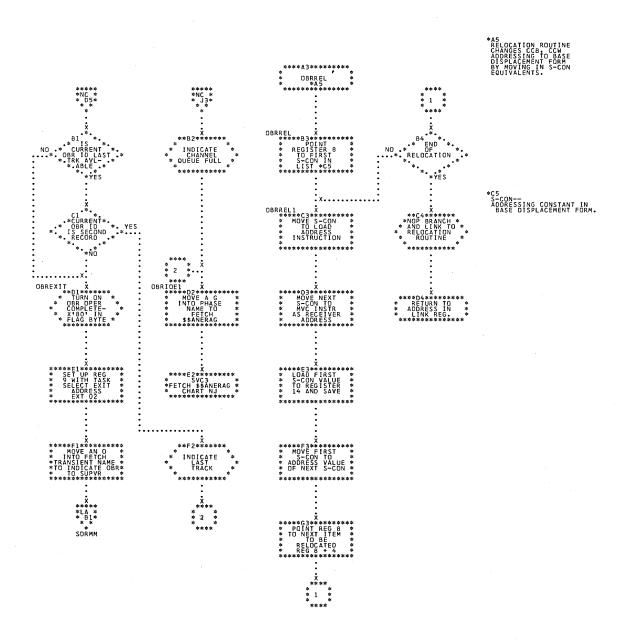


Chart NE. \$\$ANERAC - SDR External Update of Recorder File Records (Part 1 of 2) Refer to Chart 13.

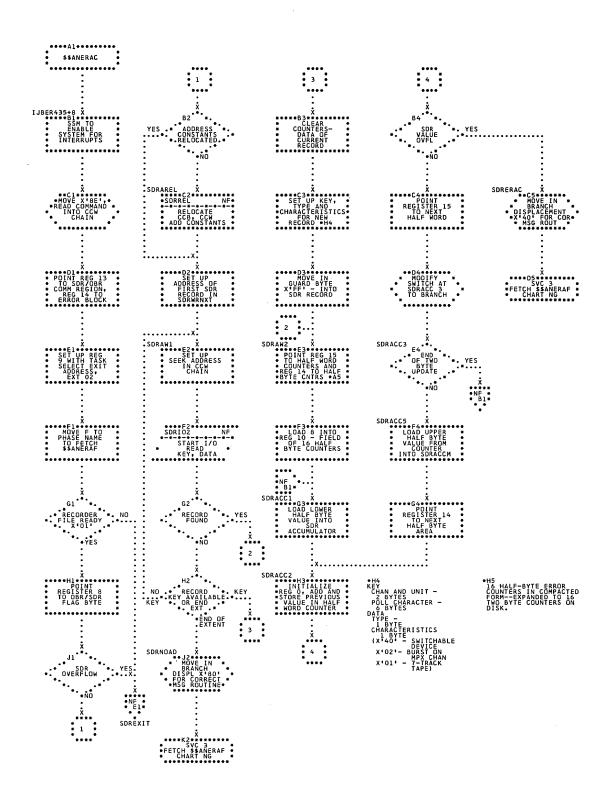
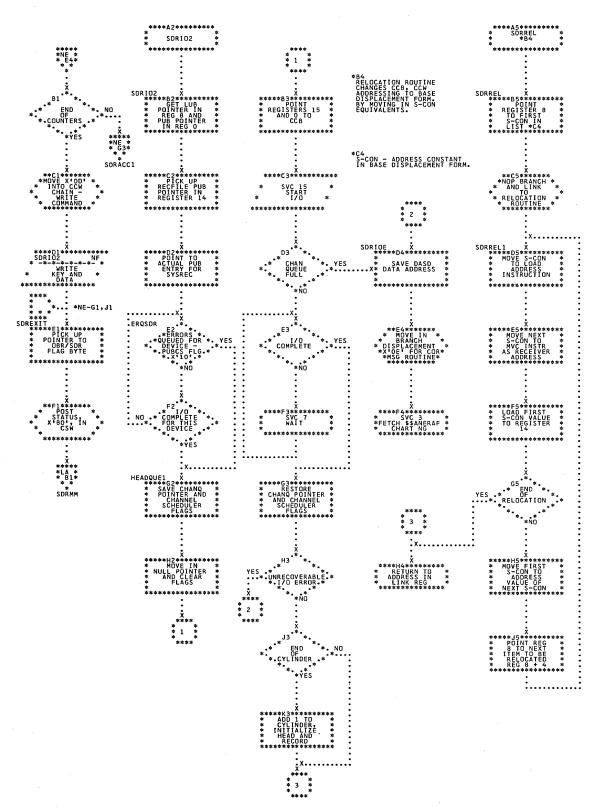


Chart NF. \$\$ANERAC - SDR External Update of Recorder File Records (Part 2 of 2) Refer to Chart 13.



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Chart NG. \$\$ANERAF - Recorder File Error Message Writer for OBR/SDR (Part 1 of 2) Refer to Chart 13.

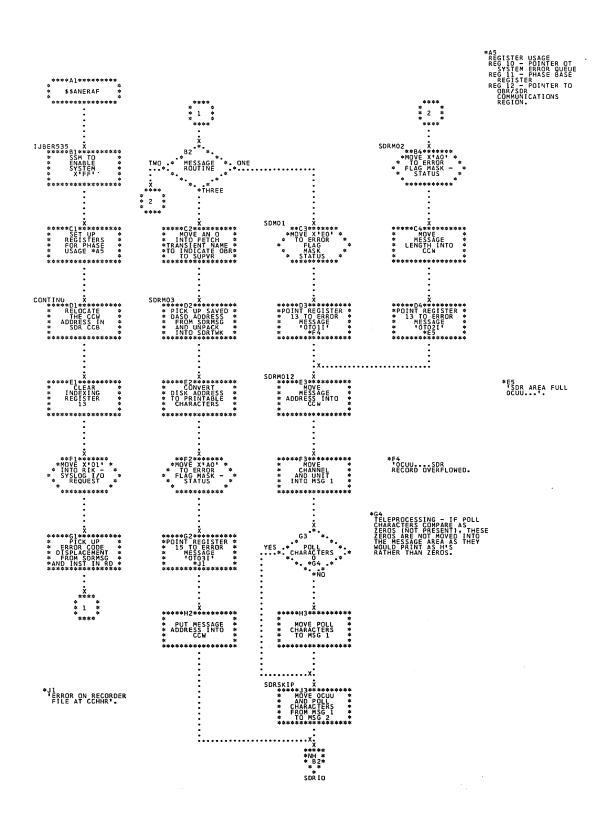


Chart NH. \$\$ANERAF - Recorder File Error Message Writer for OBR/SDR (Part 2 of 2) Refer to Chart 13.

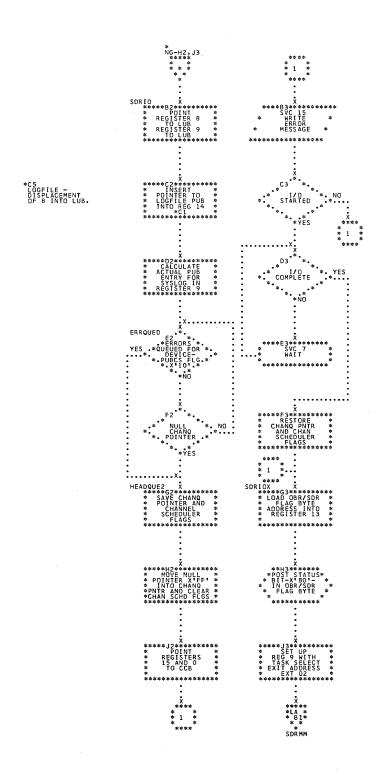


Chart NJ. \$\$ANERAG - Recorder File Last Track Error Message Writer for OBR/SDR Refer to Chart 13.

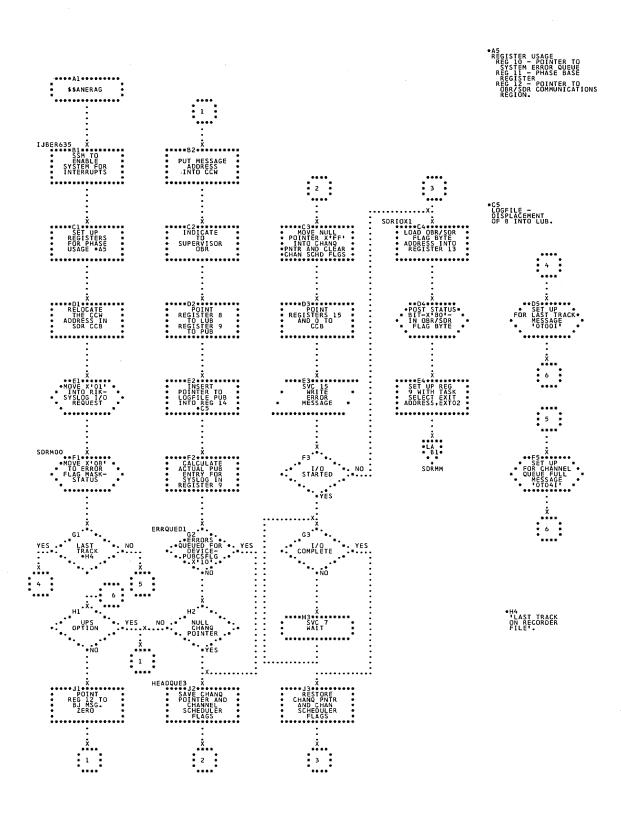


Chart NK. \$\$ANERAD - List Passer for SDR Processor Refer to Chart 11.

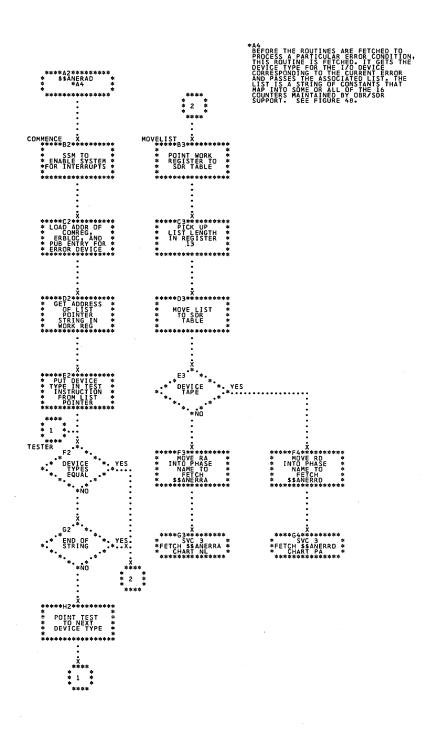


Chart NL. \$\$ANERRA - ERP Monitor (Part 1 of 2) Refer to Chart 11.

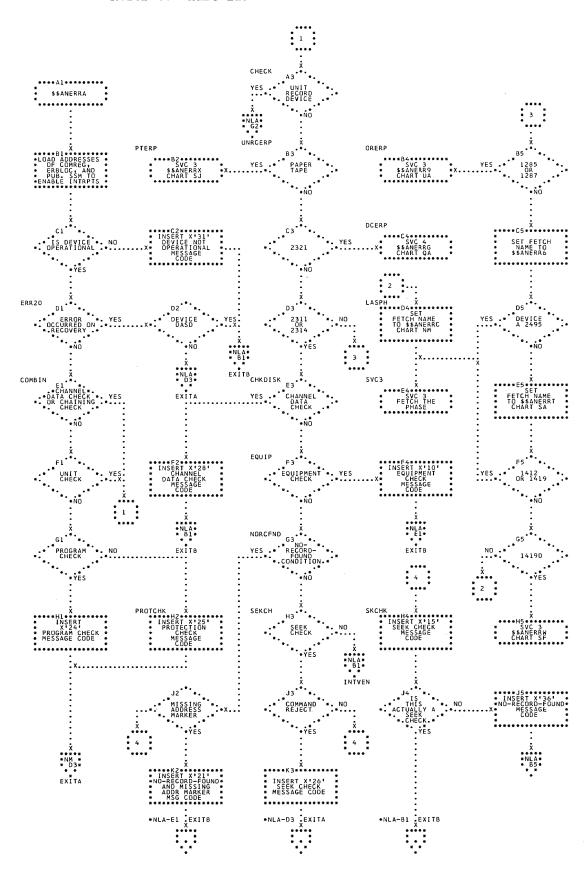
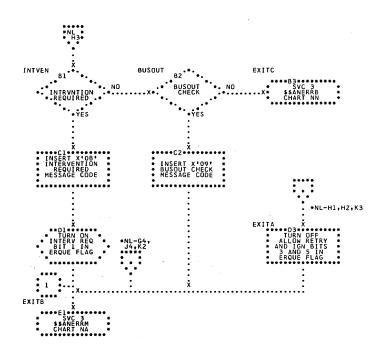
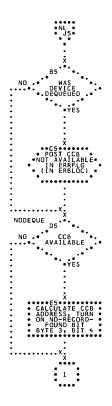


Chart NLA. \$\$ANERRA - ERP Monitor (Part 2 of 2) Refer to Chart 11.





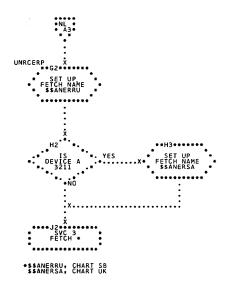


Chart NM. \$\$ANERRC - ERP Monitor Refer to Chart 11.

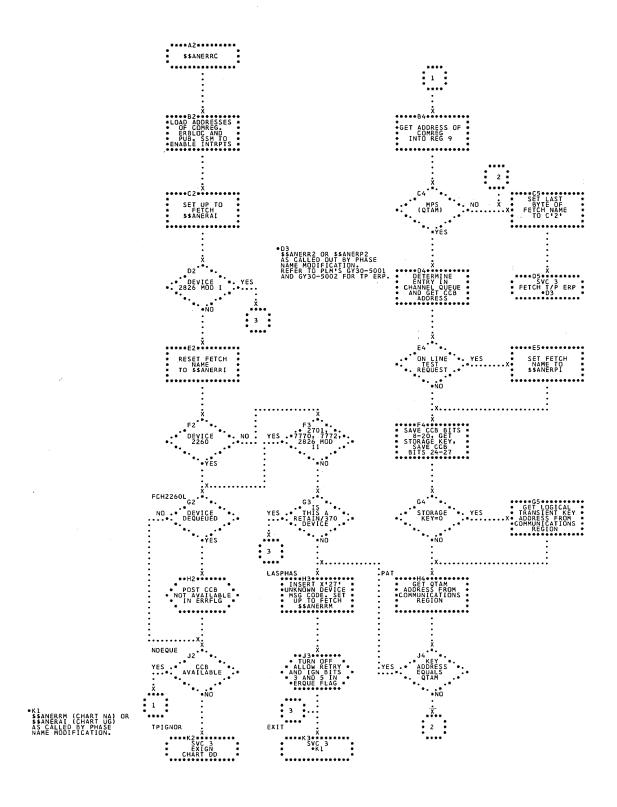


Chart NN. \$\$ANERRB - Disk ERP Refer to Chart 11.

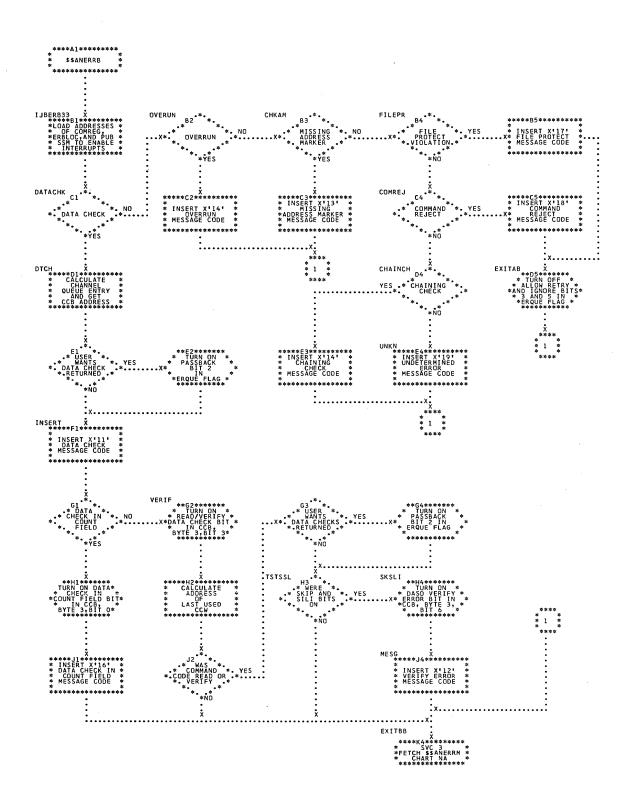


Chart PA. \$\$ANERRD - Phase 1 of Tape ERP (Part 1 of 2) Refer to Chart 13.

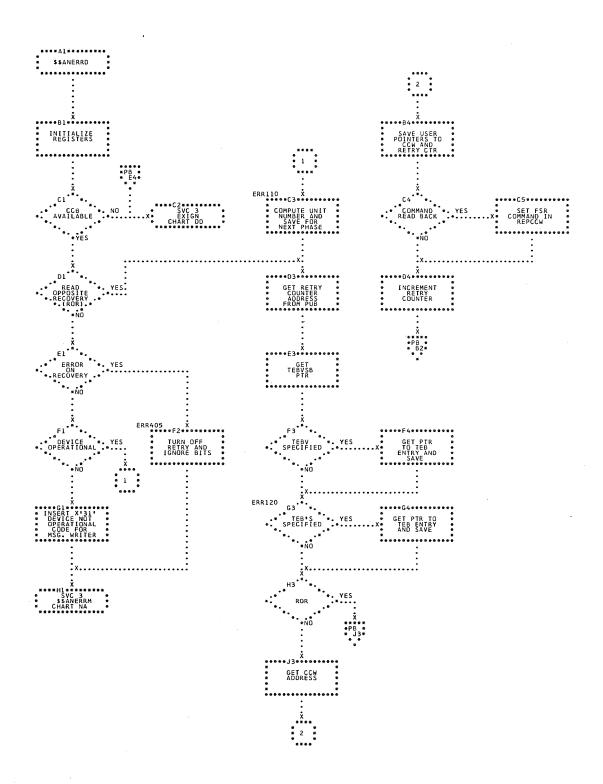


Chart PB. \$\$ANERRD - Phase 1 of Tape ERP (Part 2 of 2) Refer to Chart 13.

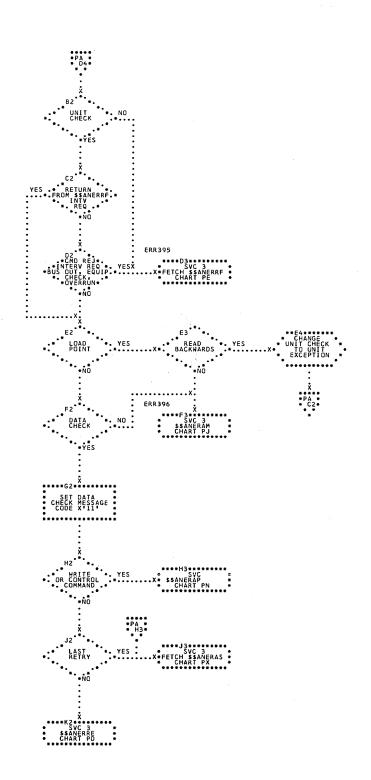


Chart PC. \$\$ANERRE - Phase 2 of Tape ERP (Part 1 of 2) Refer to Chart 13.

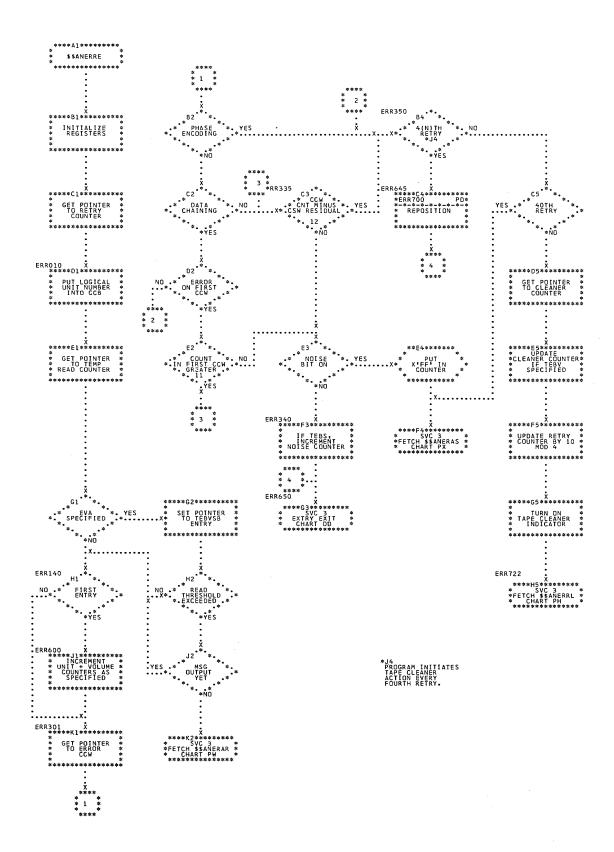


Chart PD. \$\$ANERRE - Phase 2 of Tape ERP (Part 2 of 2) Refer to Chart 13.

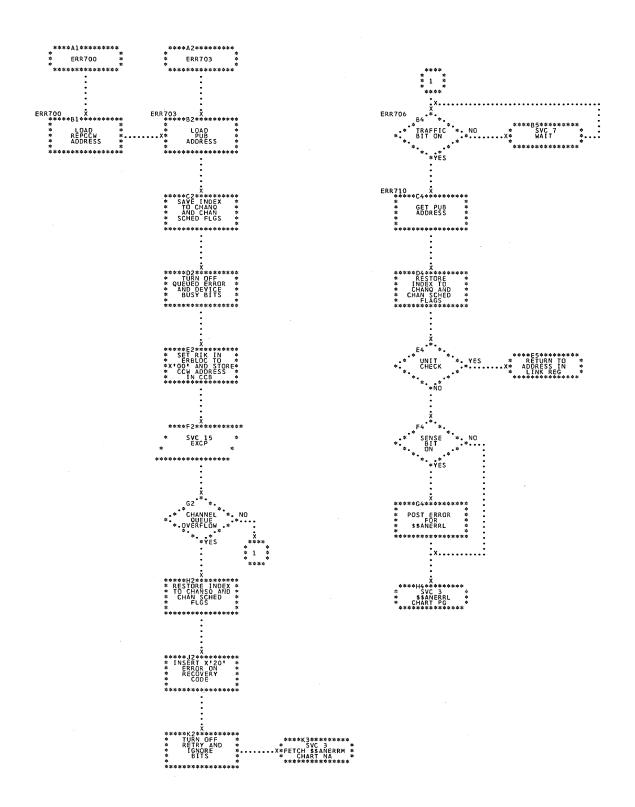


Chart PE. \$\$ANERRF - Phase 3 of Tape ERP (Part 1 of 2) Refer to Chart 13.

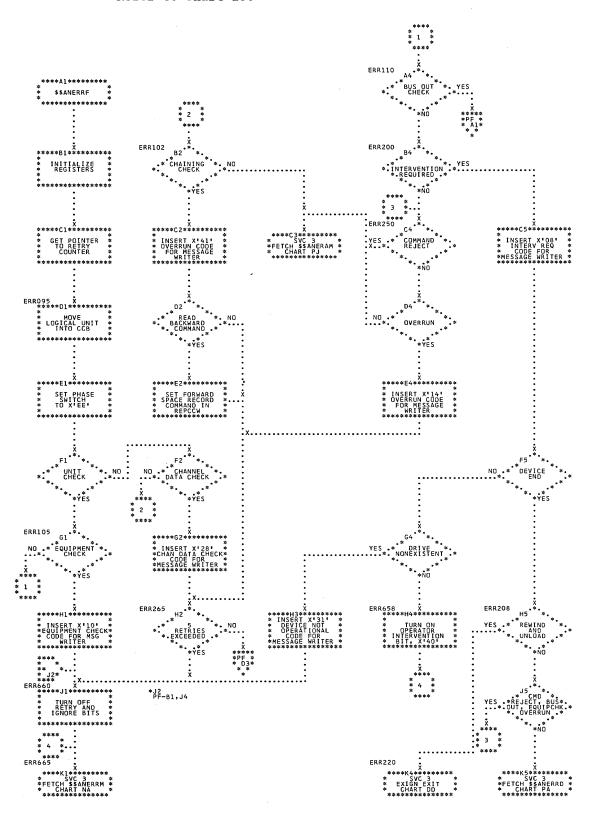


Chart PF. \$\$ANERRF - Phase 3 of Tape ERP (Part 2 of 2) Refer to Chart 13.

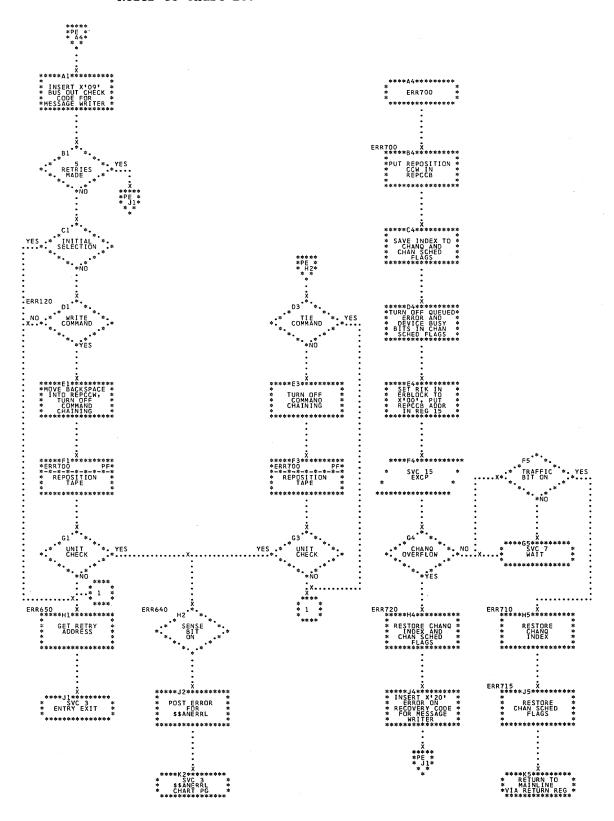


Chart PG. \$\$ANERRL - Phase 4 of Tape ERP (Part 1 of 2) Refer to Chart 13.

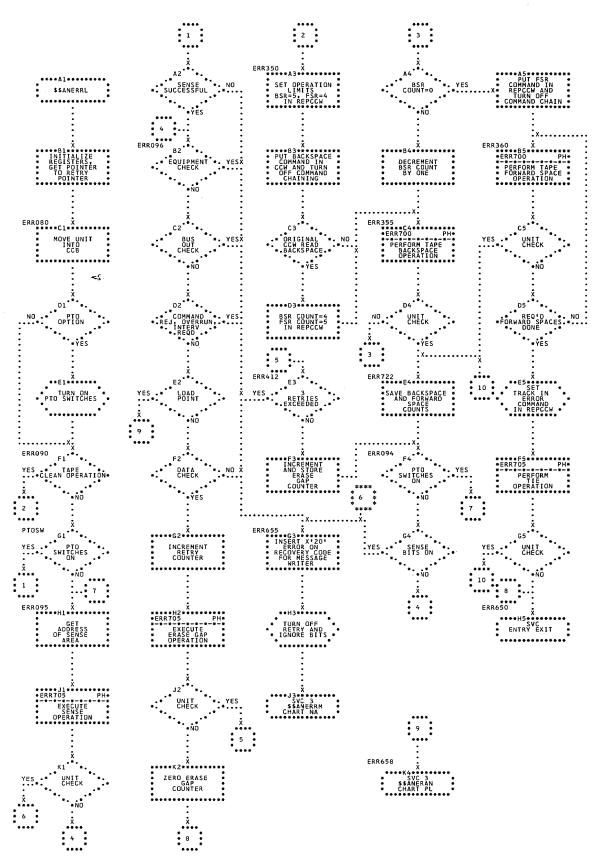


Chart PH. \$\$ANERRL - Phase 4 of Tape ERP (Part 2 of 2) Refer to Chart 13.

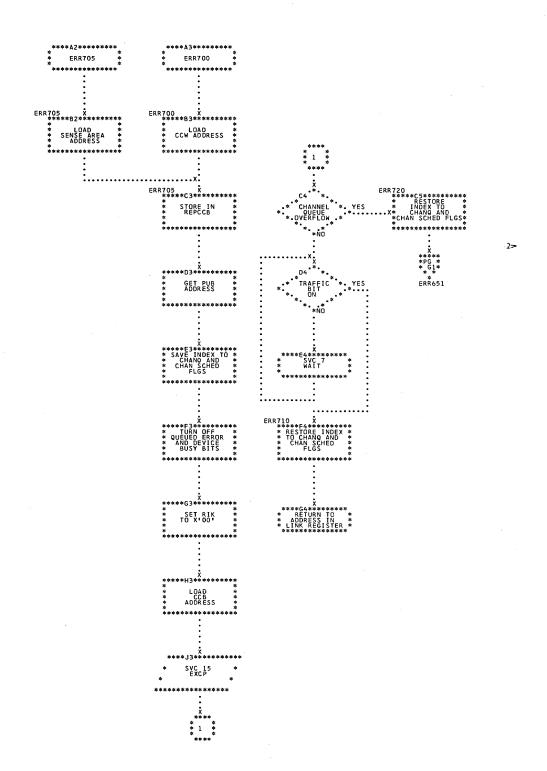


Chart PJ. \$\$ANERAM - Phase 5 of Tape ERP (Part 1 of 2) Refer to Chart 13.

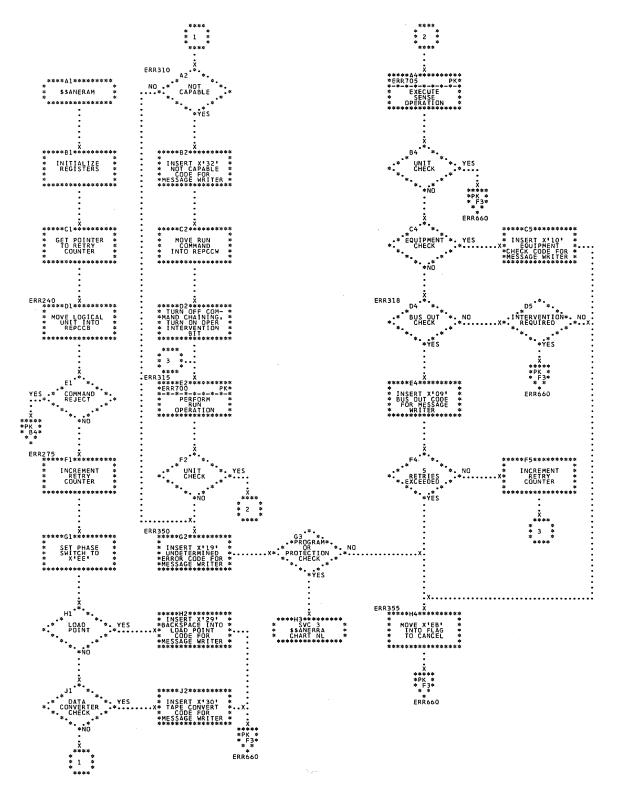


Chart PK. \$\$ANERAM - Phase 5 of Tape ERP (Part 2 of 2) Refer to Chart 13.

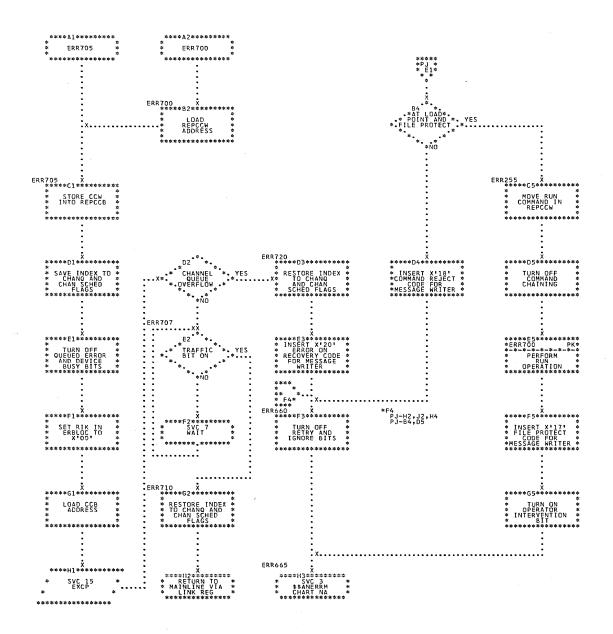


Chart PL. \$\$ANERAN - Phase 6 of Tape ERP (Part 1 of 2) Refer to Chart 13.

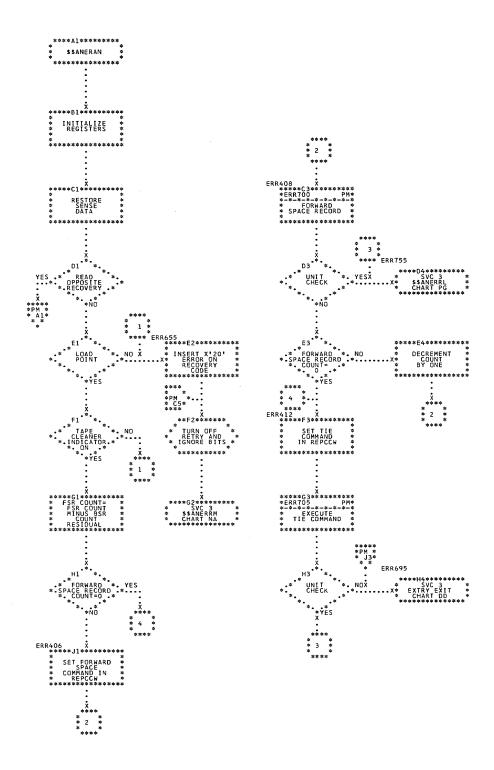


Chart PM. \$\$ANERAN - Phase 6 of Tape ERP (Part 2 of 2) Refer to Chart 13.

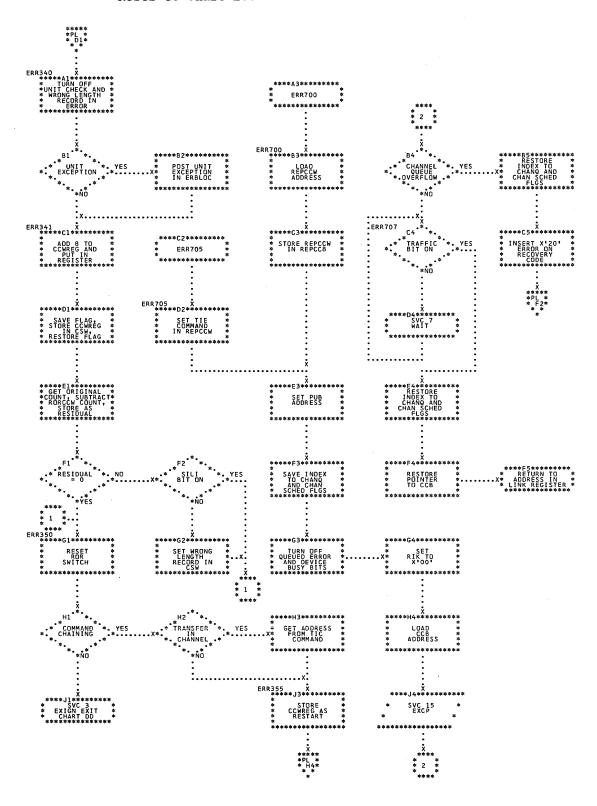


Chart PN. \$\$ANERAP - Phase 7 of Tape ERP (Part 1 of 2) Refer to Chart 13.

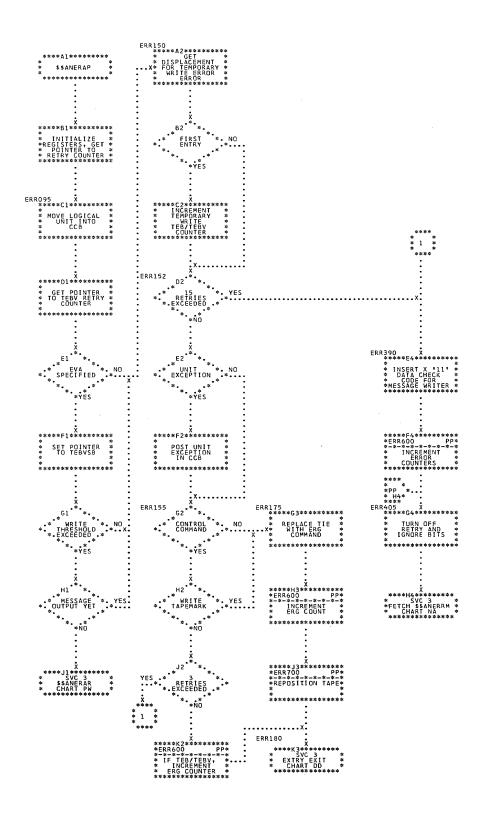


Chart PP. \$\$ANERAP - Phase 7 of Tape ERP (Part 2 of 2) Refer to Chart 13.

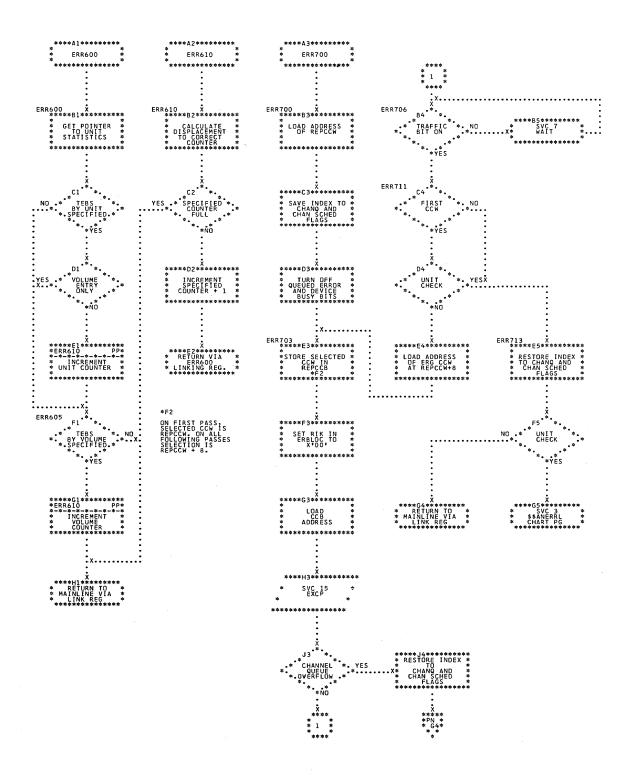


Chart PQ. \$\$ANERAQ - Phase 8 of Tape ERP (Part 1 of 2) Refer to Chart 13.

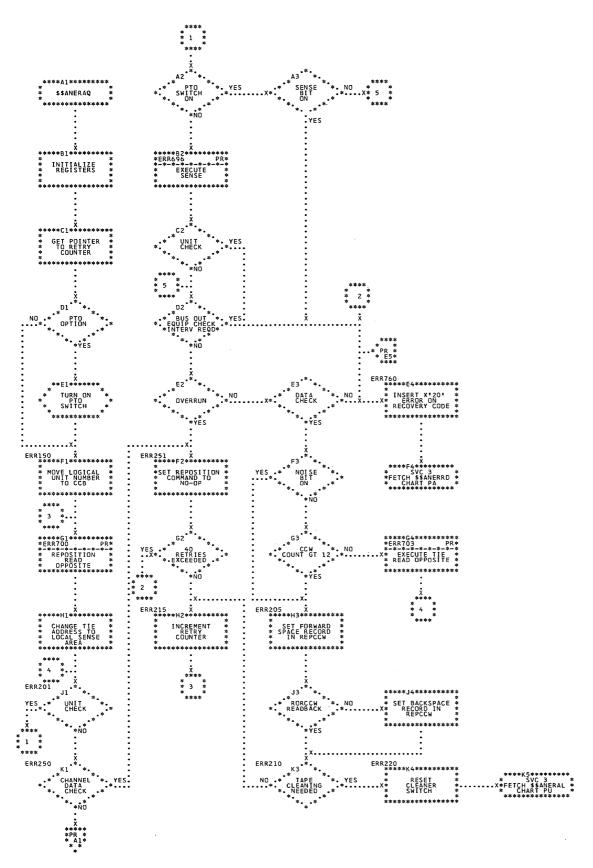


Chart PR. \$\$ANERAQ - Phase 8 of Tape ERP (Part 2 of 2) Refer to Chart 13.

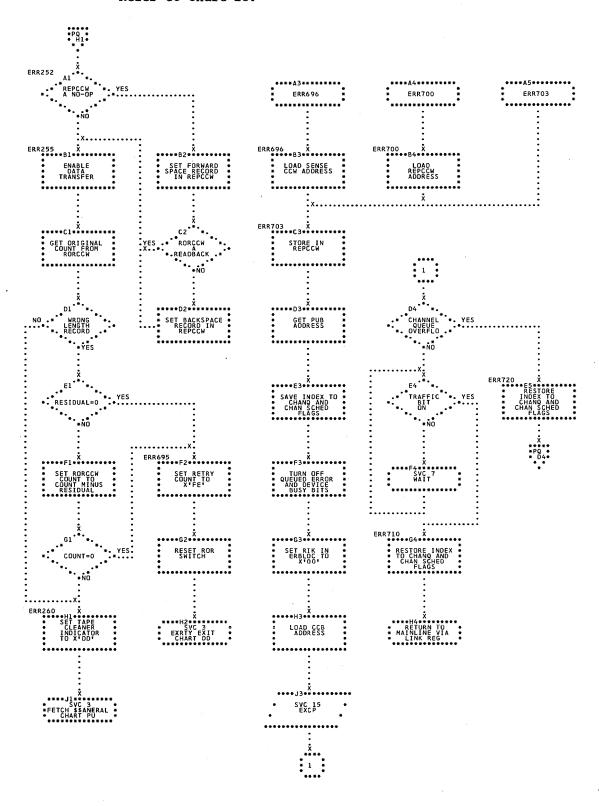


Chart PS. \$\$ANERAK - Phase 9 of Tape ERP (Part 1 of 2) Refer to Chart 13.

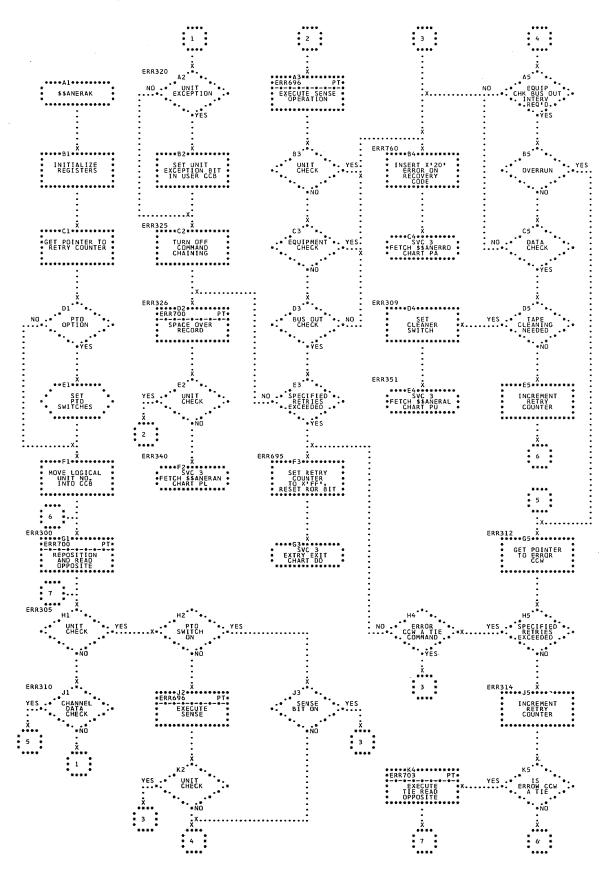


Chart PT. \$\$ANERAK - Phase 9 of Tape ERP (Part 2 of 2) Refer to Chart 13.

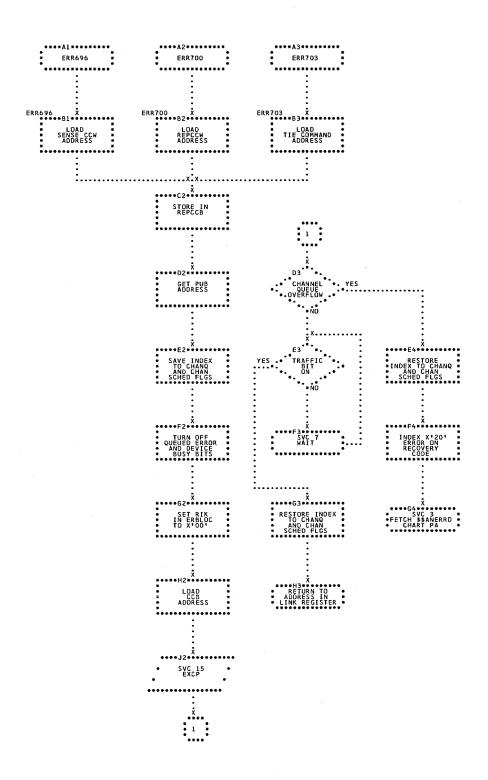


Chart PU. \$\$ANERAL - Phase 10 of Tape ERP (Part 1 of 2) Refer to Chart 13.

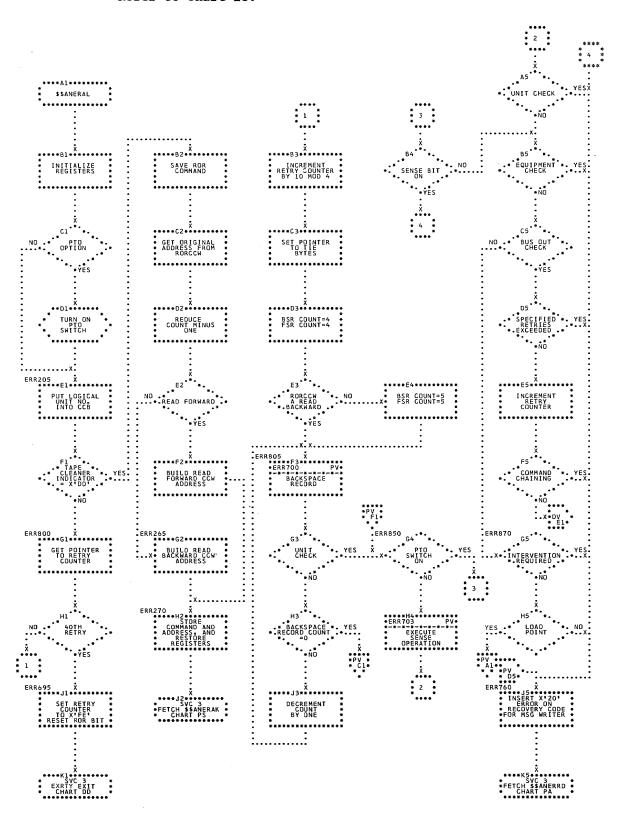


Chart PV. \$\$ANERAL - Phase 10 of Tape ERP (Part 2 of 2) Refer to Chart 13.

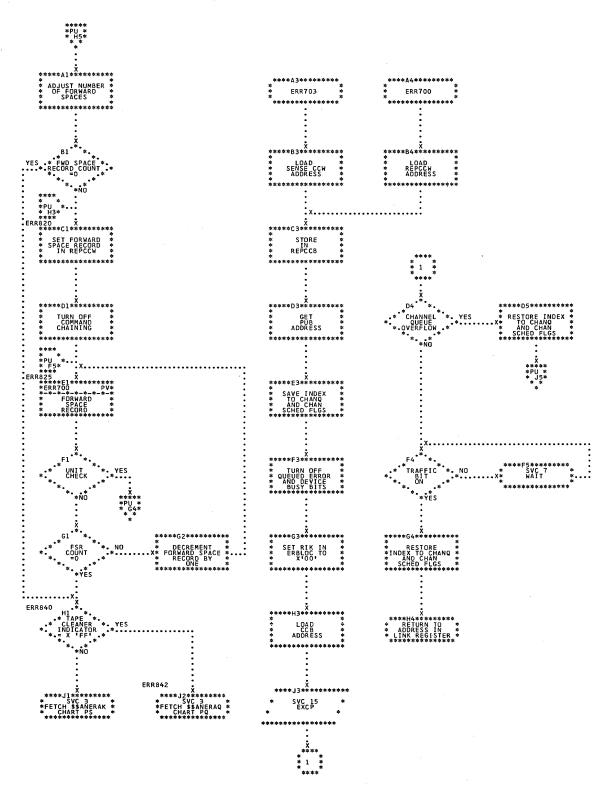


Chart PW. \$\$ANERAR - Phase 11 of Tape ERP Refer to Chart 13.

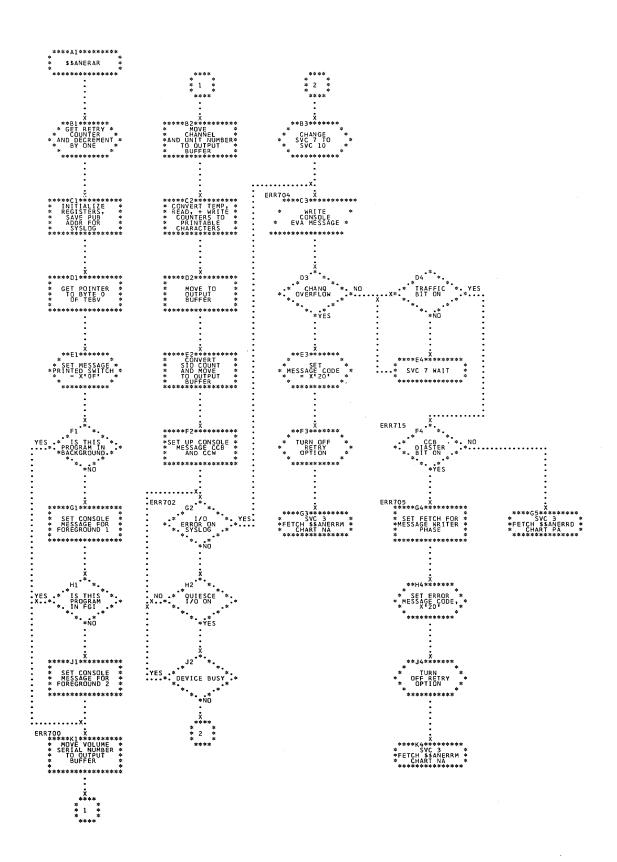
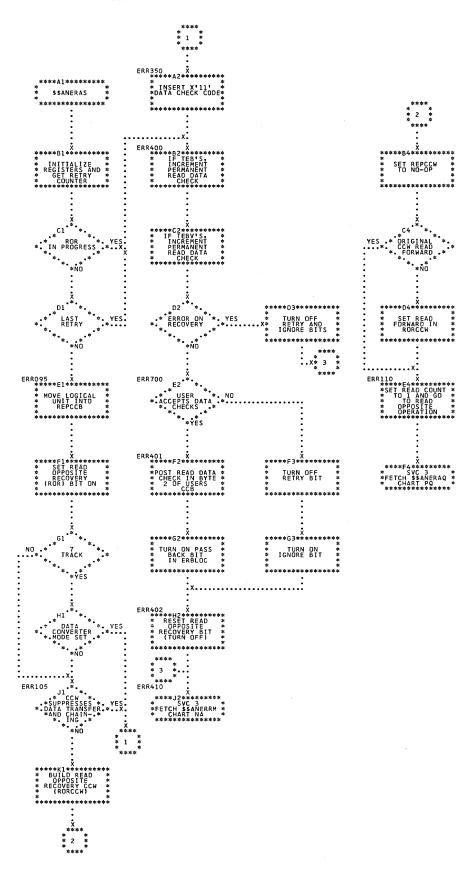


Chart PX. \$\$ANERAS - Phase 12 of Tape ERP Refer to Chart 13.



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Chart QA. \$\$ANERRG - Phase 1 of Data Cell ERP (Part 1 of 3) Refer to Chart 11.

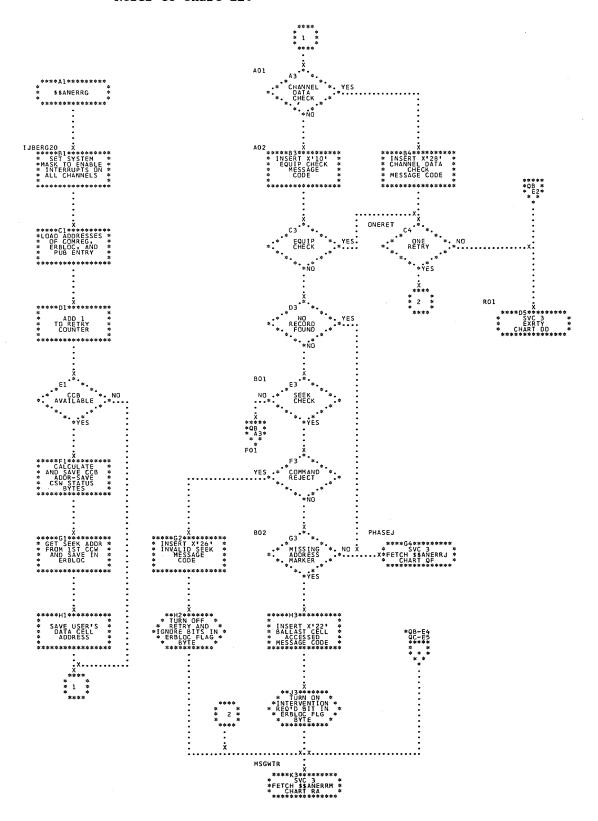


Chart QB. \$\$ANERRG - Phase 1 of Data Cell ERP (Part 2 of 3) Refer to Chart 11.

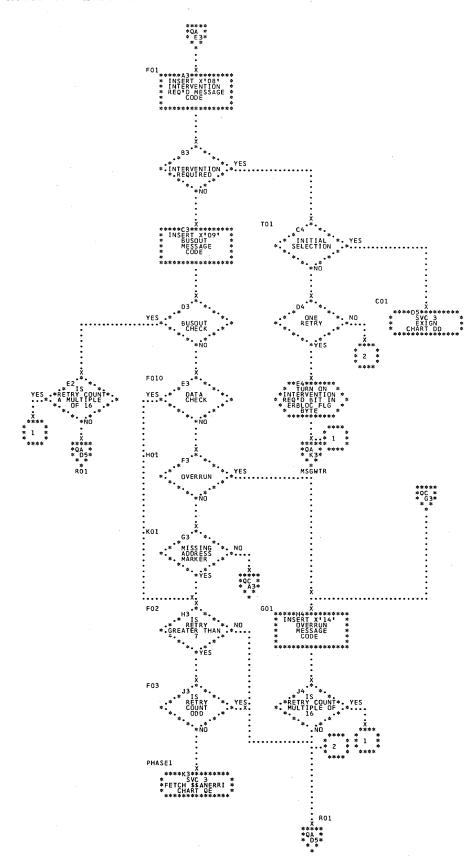


Chart QC. \$\$ANERRG - Phase 1 of Data Cell ERP (Part 3 of 3) Refer to Chart 11.

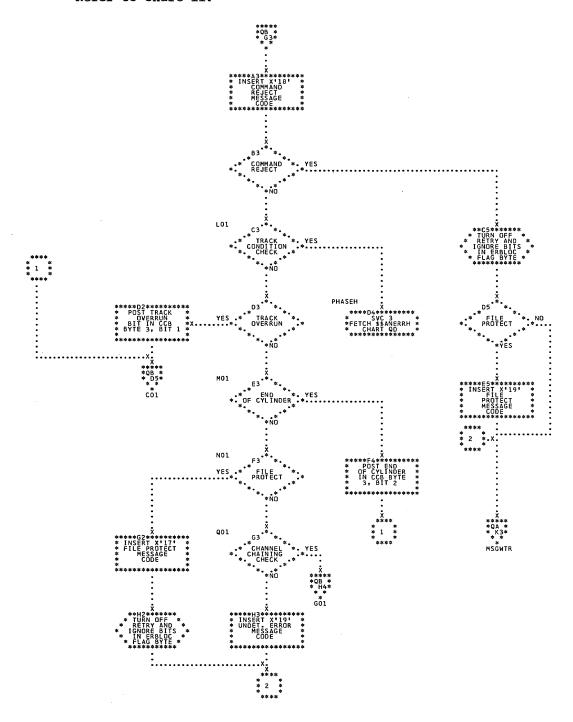
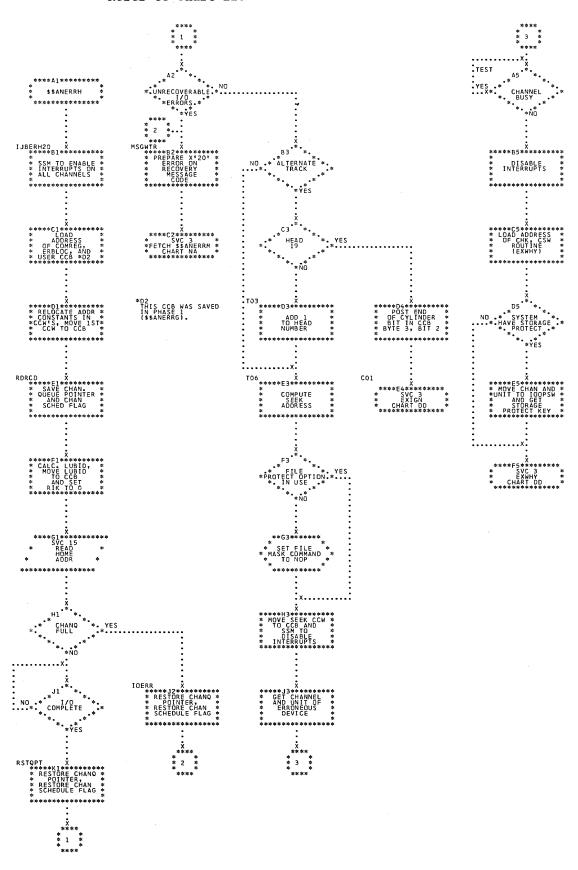


Chart QD. \$\$ANERRH - Phase 2 of Data Cell ERP Refer to Chart 11.



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Chart QE. \$\$ANERRI - Phase 3 of Data Cell ERP Refer to Chart 11.

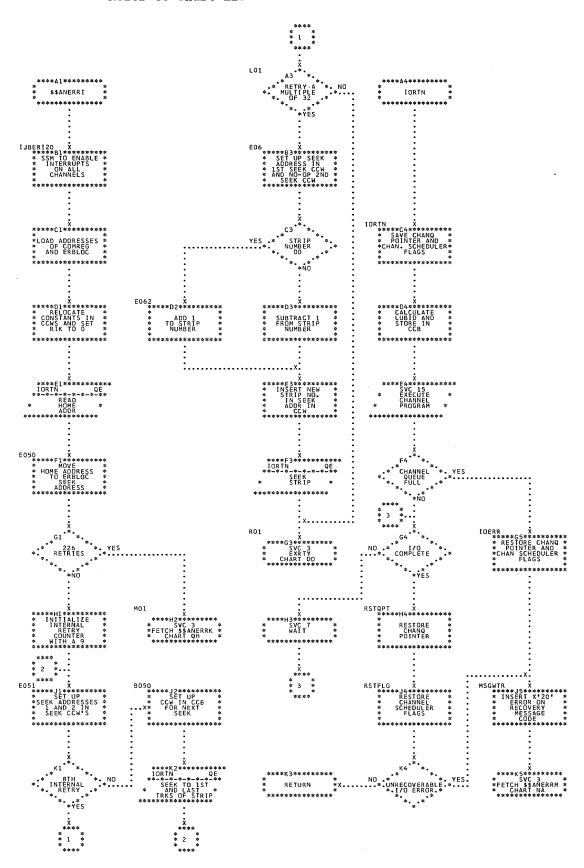
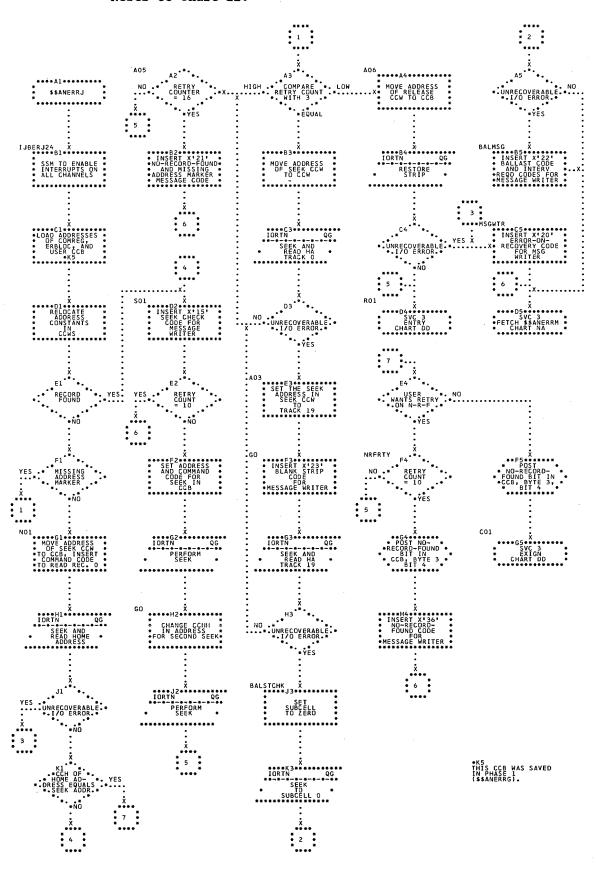


Chart QF. \$\$ANERRJ - Phase 4 of Data Cell ERP (Part 1 of 2) Refer to Chart 11.



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Chart QG. \$\$ANERRJ - Phase 4 of Data Cell ERP (Part 2 of 2) Refer to Chart 11.

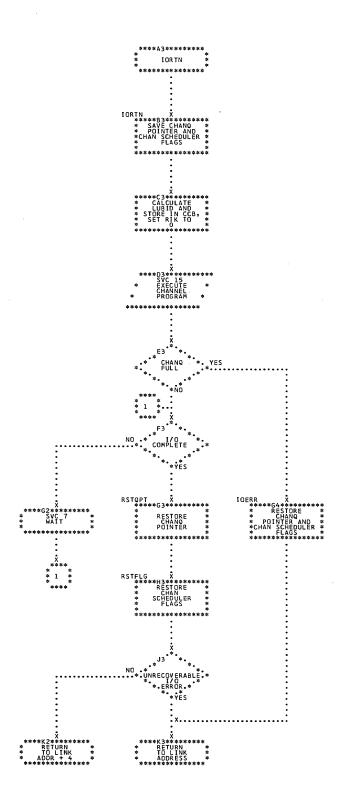


Chart QH. \$\$ANERRK - Phase 5 of Data Cell ERP Refer to Chart 11.

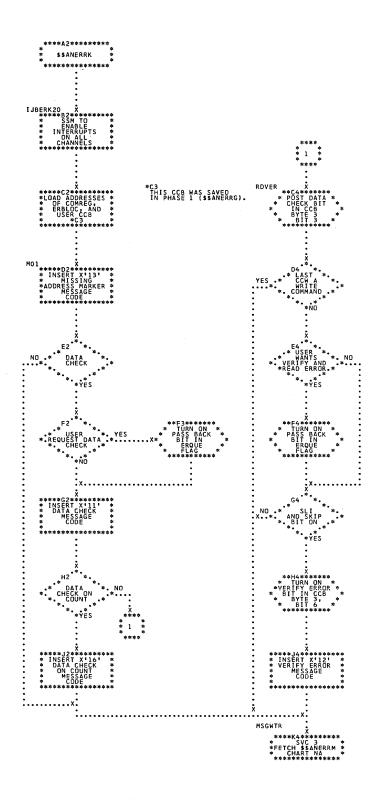


Chart RA. \$\$ANERAB - Phase 1 of ERP Message Writer Refer to Chart 14.

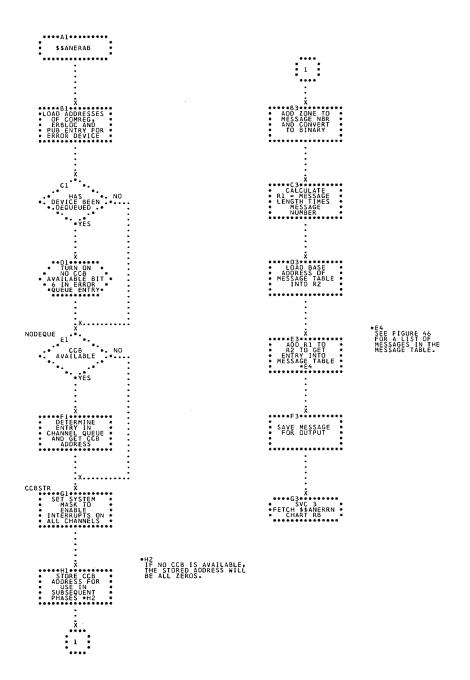
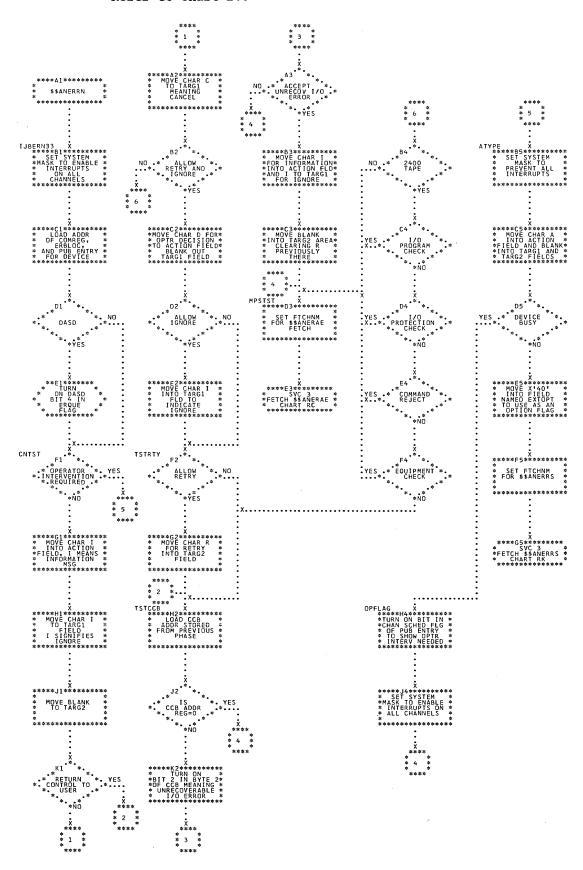


Chart RB. \$\$ANERRN - Phase 2 of ERP Message Writer Refer to Chart 14.



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Chart RC. \$\$ANERAE - Phase 2A of ERP Message Writer Refer to Chart 14.

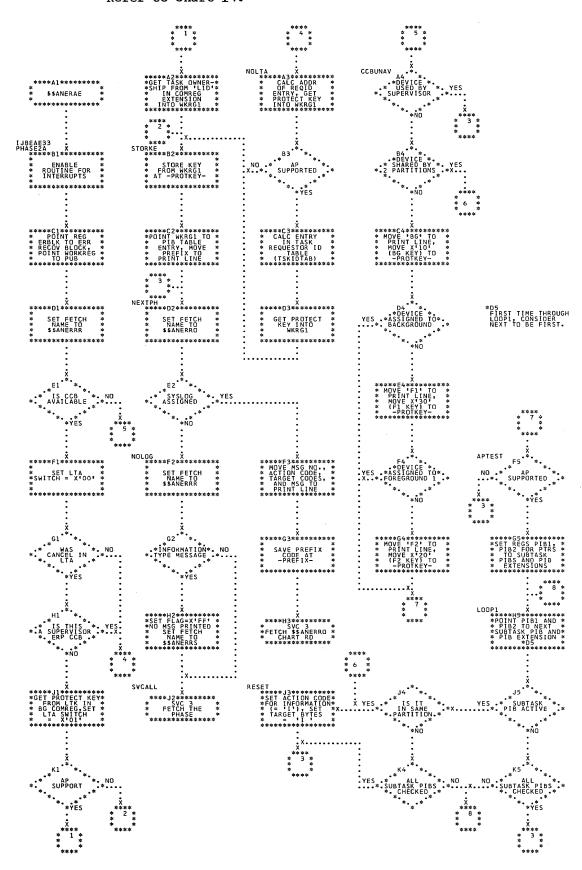
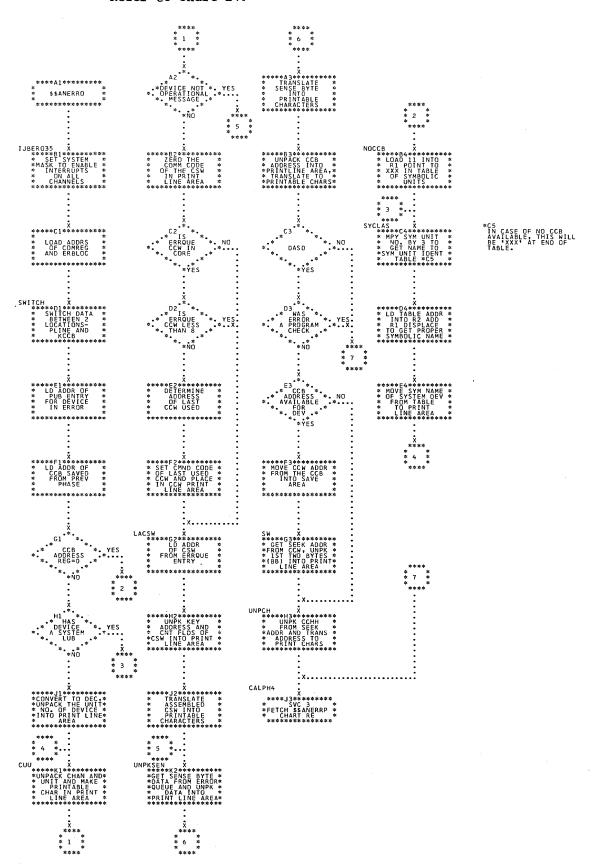


Chart RD. \$\$ANERRO - Phase 3 of ERP Message Writer Refer to Chart 14.



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Chart RE. \$\$ANERRP - Phase 4 of ERP Message Writer (Part 1 of 2) Refer to Chart 14.

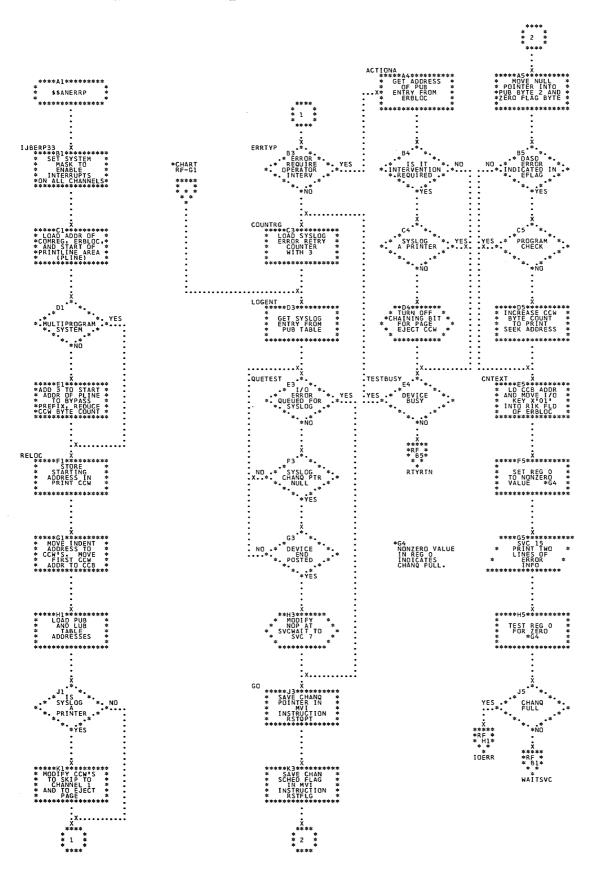


Chart RF. \$\$ANERRP - Phase 4 of ERP Message Writer (Part 2 of 2) Refer to Chart 14.

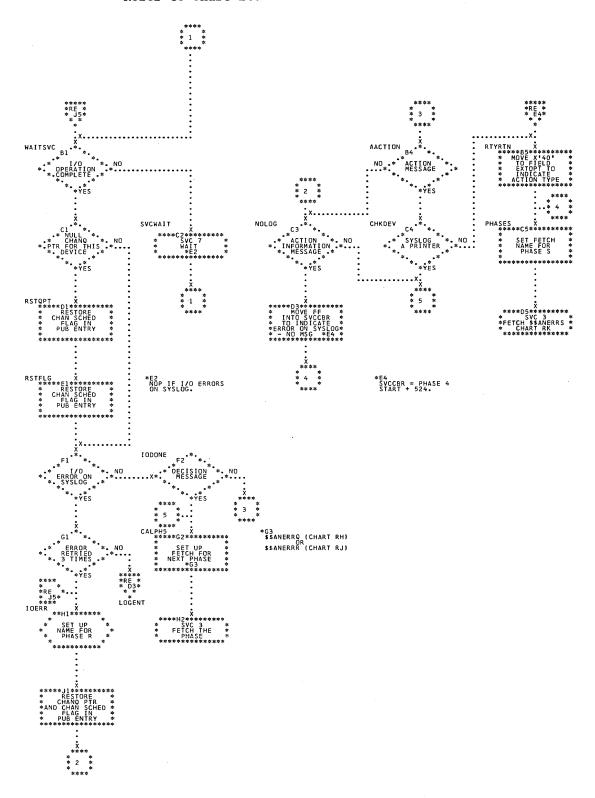


Chart RG. \$\$ANERRQ - Phase 5 of ERP Message Writer (Part 1 of 2) Refer to Chart 14.

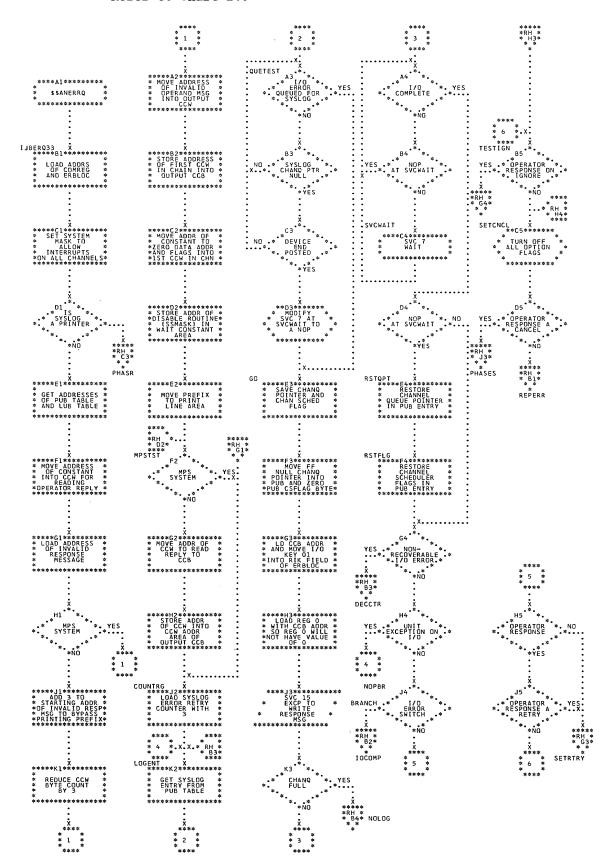


Chart RH. \$\$ANERRQ - Phase 5 of ERP Message Writer (Part 2 of 2) Refer to Chart 14.

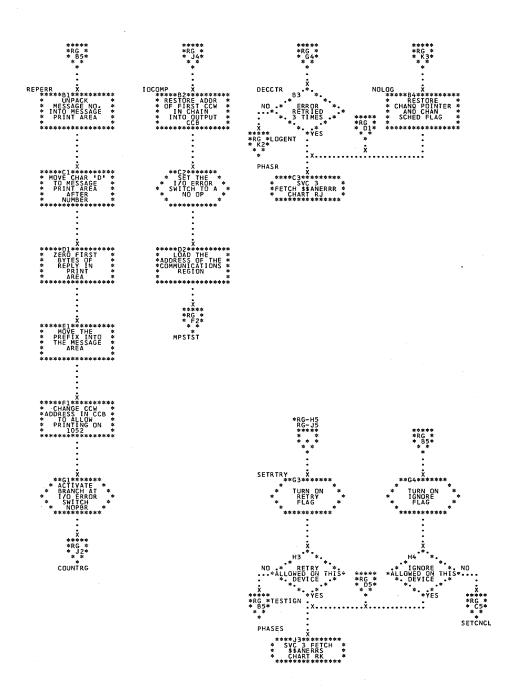


Chart RJ. \$\$ANERRR - Phase 6 of ERP Message Writer Refer to Chart 14.

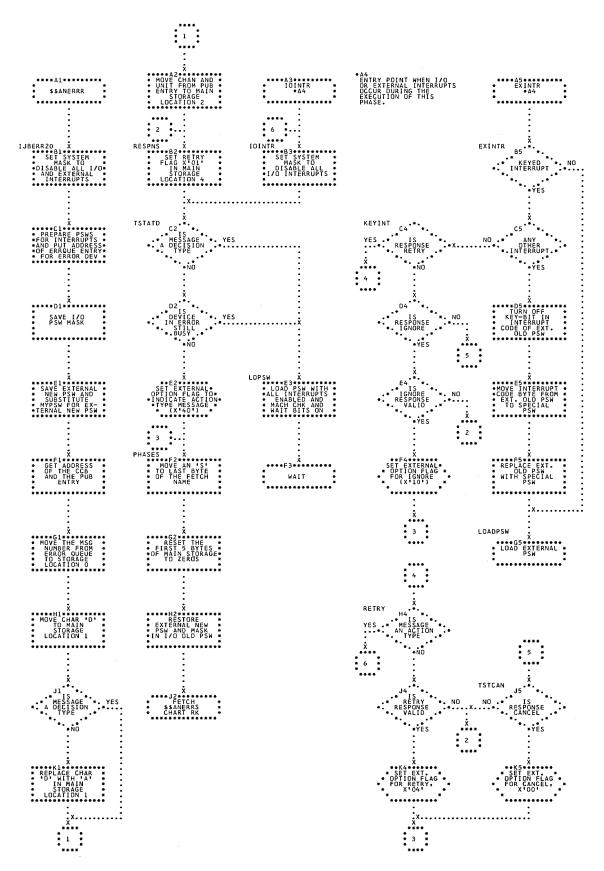


Chart RK. \$\$ANERRS - Phase 7 of ERP Message Writer (Part 1 of 2) Refer to Chart 14.

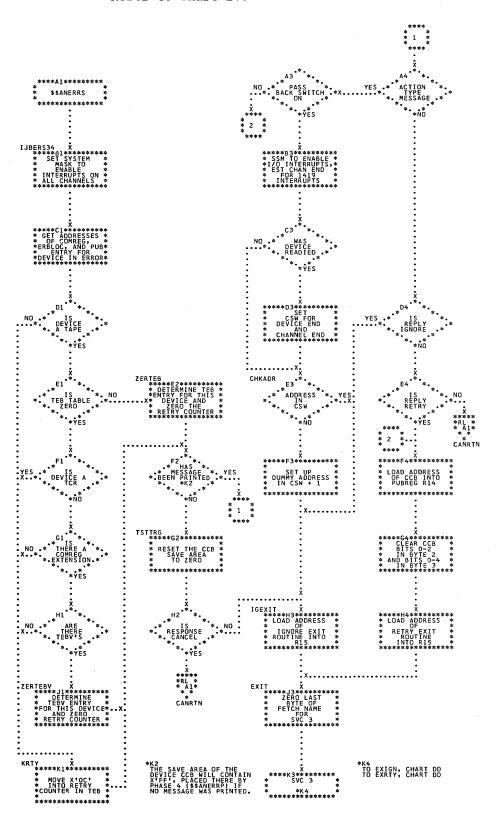


Chart RL. \$\$ANERRS - Phase 7 of ERP Message Writer (Part 2 of 2) Refer to Chart 14.

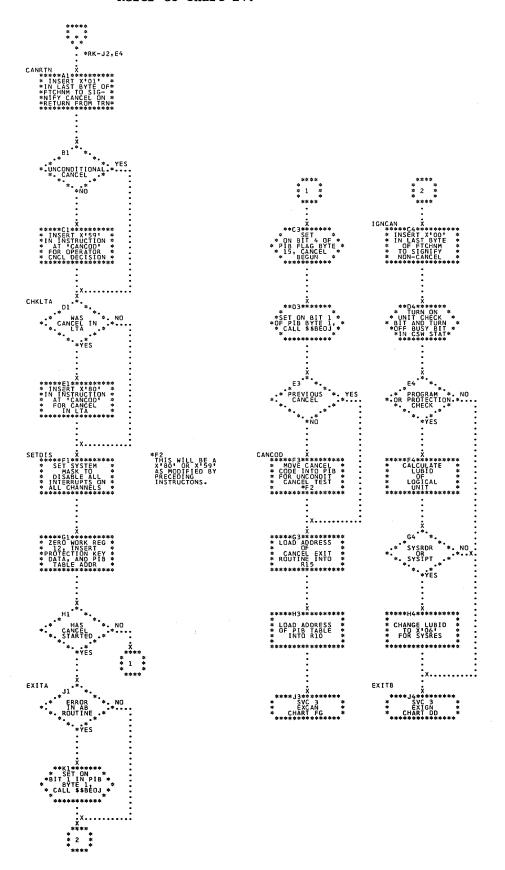
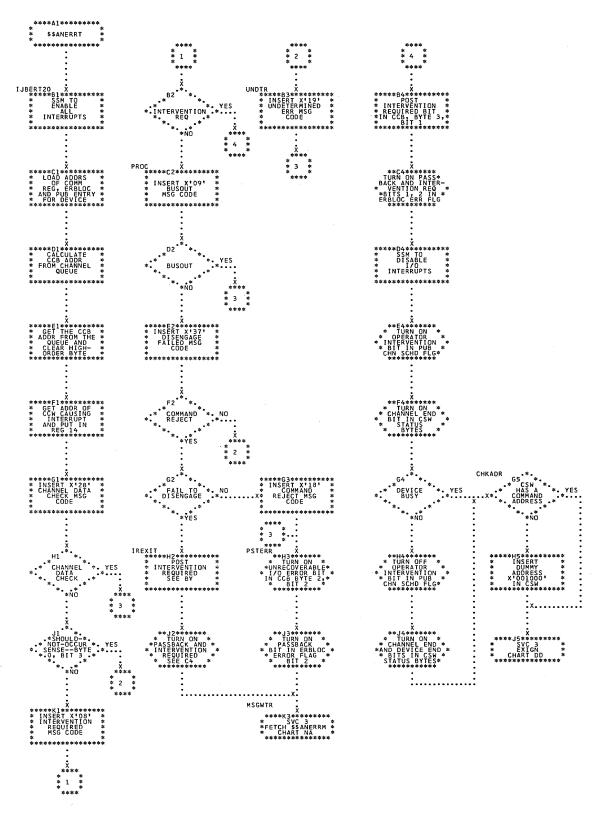


Chart SA. \$\$ANERRT - MICR (1412/1419) ERP Refer to Chart 12.



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Chart SB. \$\$ANERRU - Phase 1 of Unit Record ERP (Part 1 of 2) Refer to Chart 11.

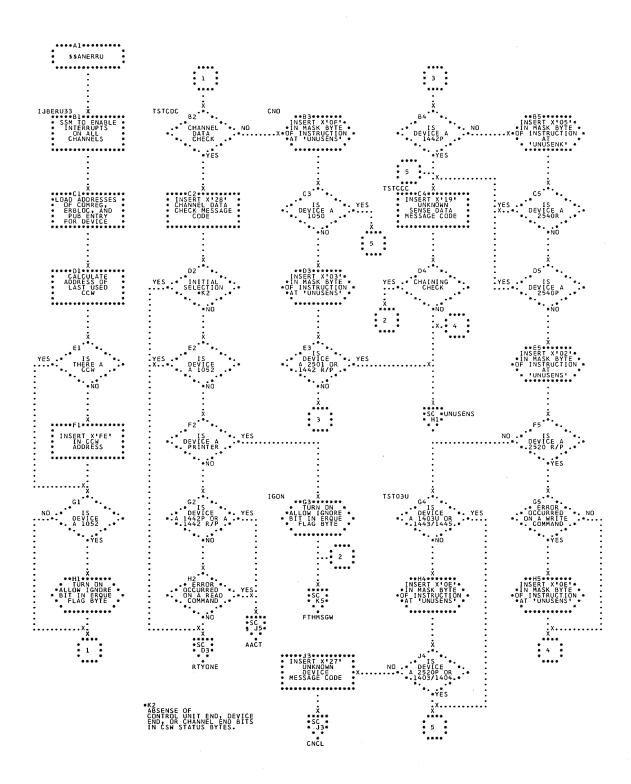


Chart SC. \$\$ANERRU - Phase 1 of Unit Record ERP (Part 2 of 2) Refer to Chart 11.

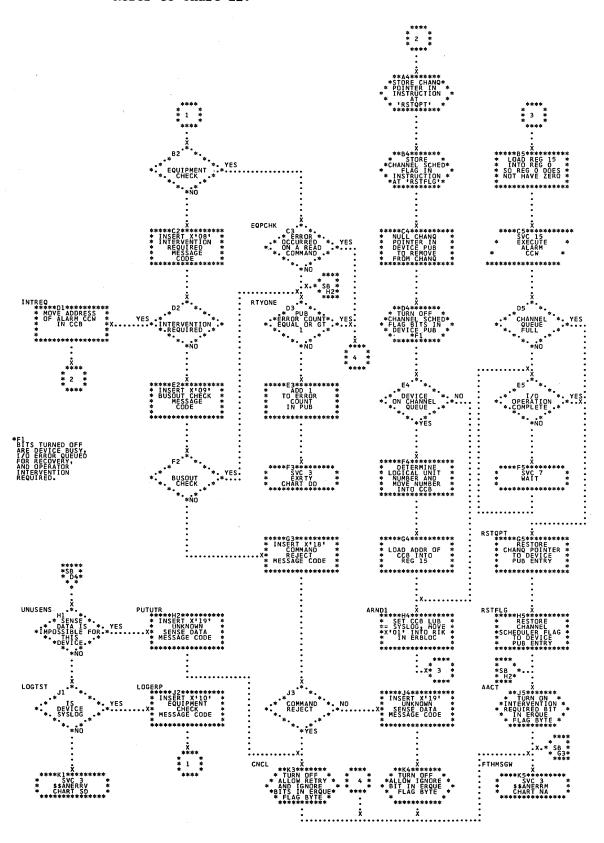


Chart SD. \$\$ANERRV - Phase 2 of Unit Record ERP (Part 1 of 2) Refer to Chart 11.

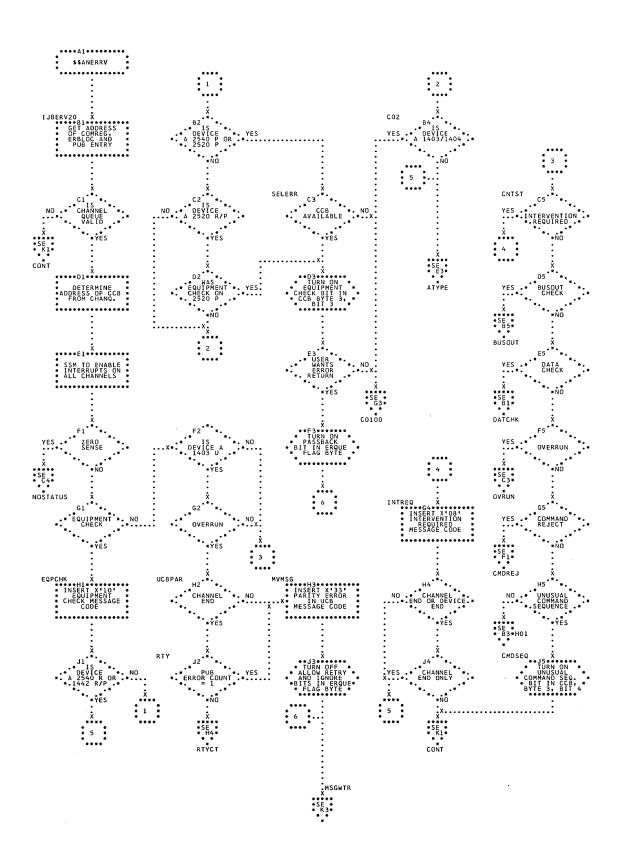


Chart SE. \$\$ANERRV - Phase 2 of Unit Record ERP (Part 2 of 2) Refer to Chart 11.

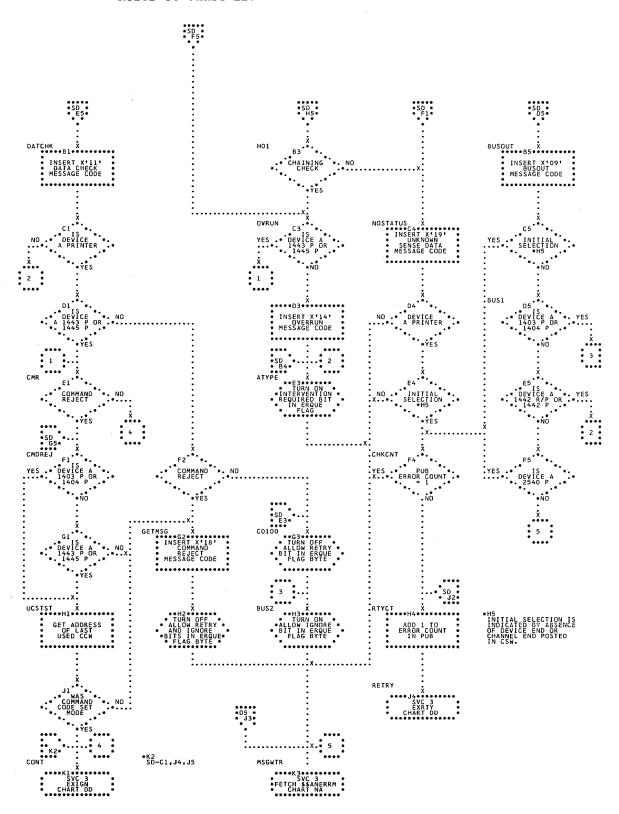


Chart SF. \$\$ANERRW - MICR (1419D) ERP (Part 1 of 3) Refer to Chart 12.

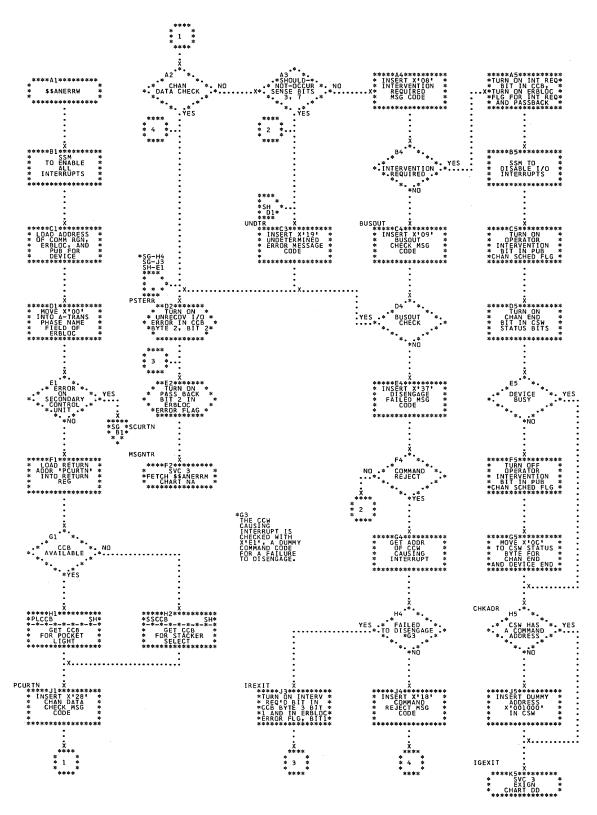


Chart SG. \$\$ANERRW - MICR (1419D) ERP (Part 2 of 3) Refer to Chart 12.

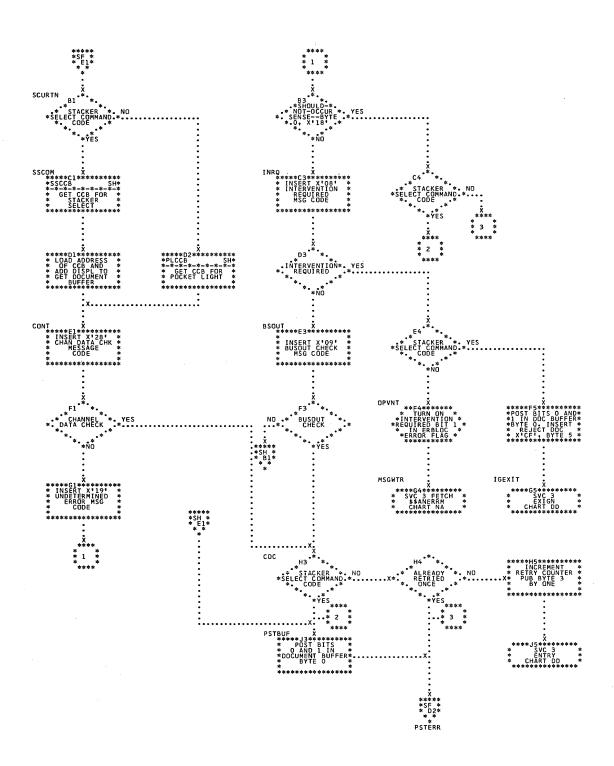


Chart SH. \$\$ANERRW - MICR (1419D) ERP (Part 3 of 3) Refer to Chart 12.

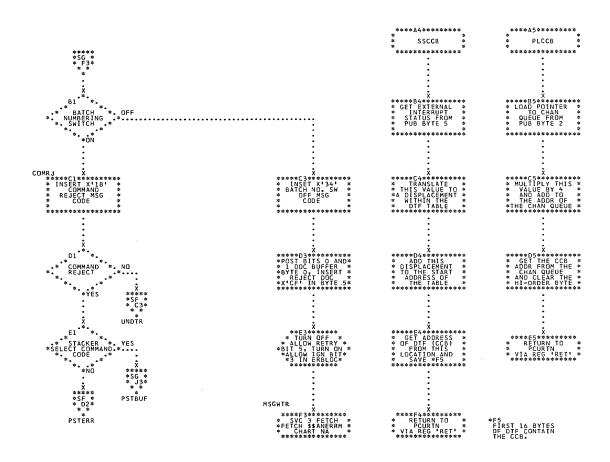


Chart SJ. \$\$ANERRX - 2671 Paper Tape ERP (Part 1 of 2) Refer to Chart 12.

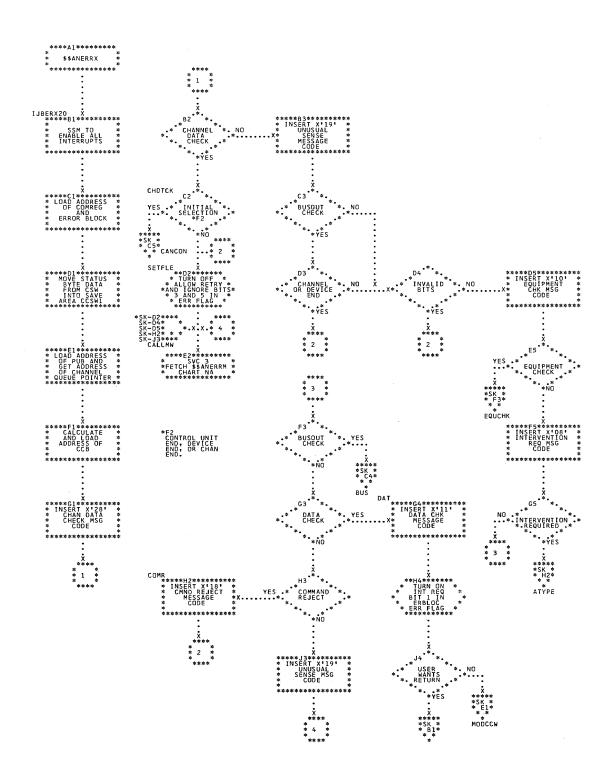


Chart SK. \$\$ANERRX - 2671 Paper Tape ERP (Part 2 of 2) Refer to Chart 12.

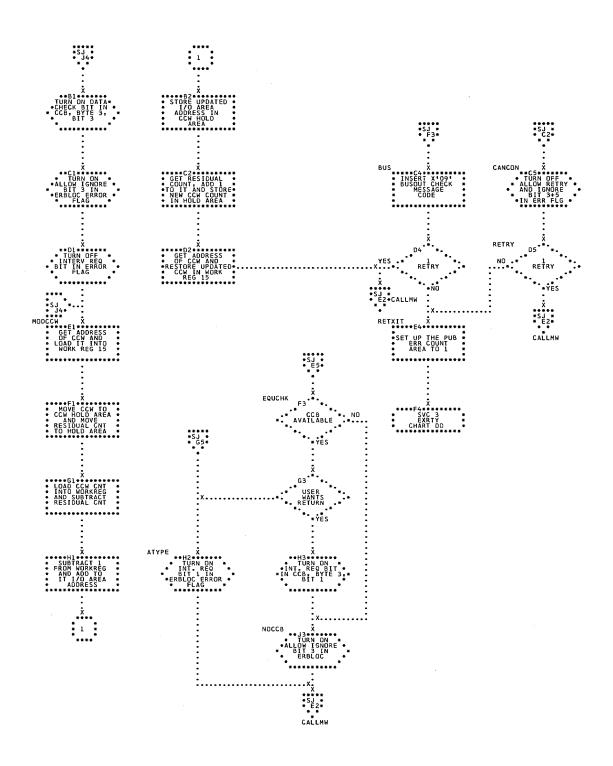


Chart TA. \$\$ANERRY - Physical Attention Routine: Send Message Refer to Chart 15.

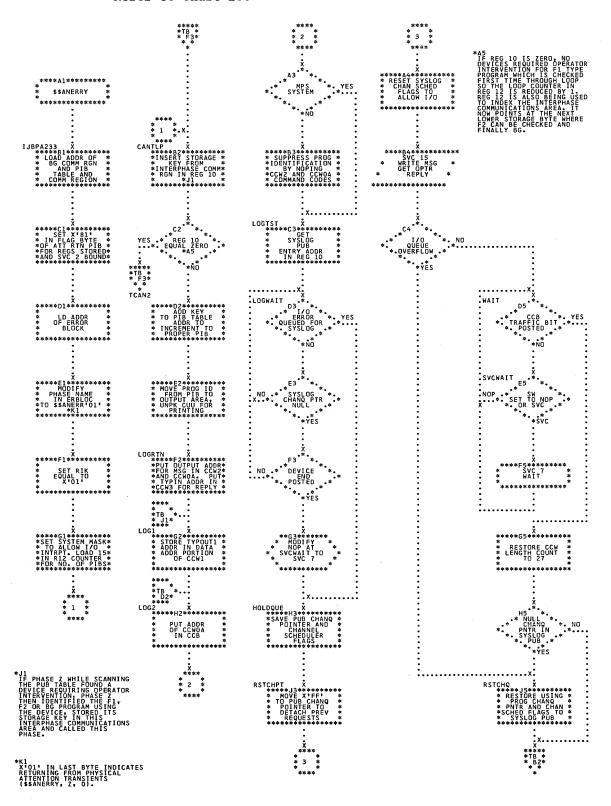


Chart TB. \$\$ANERRY - Physical Attention Routine: Read Operator Reply Refer to Chart 15.

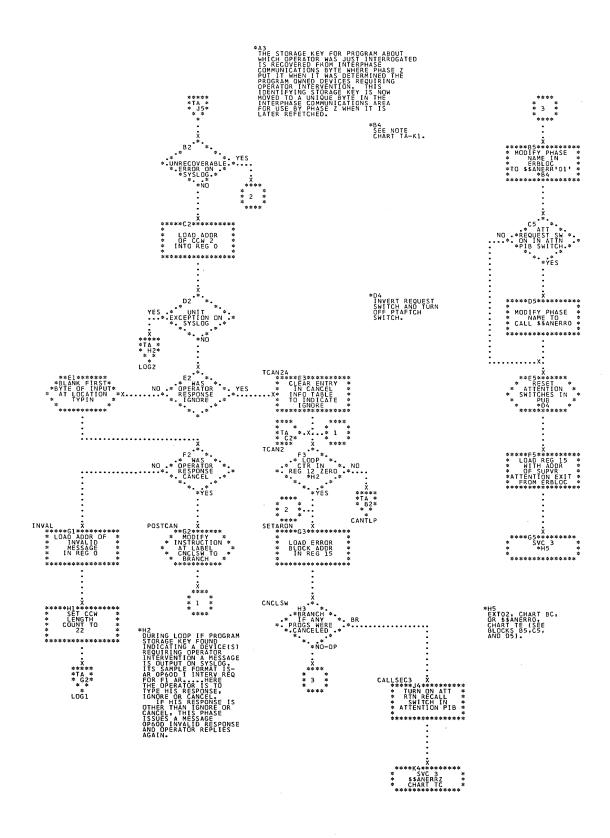
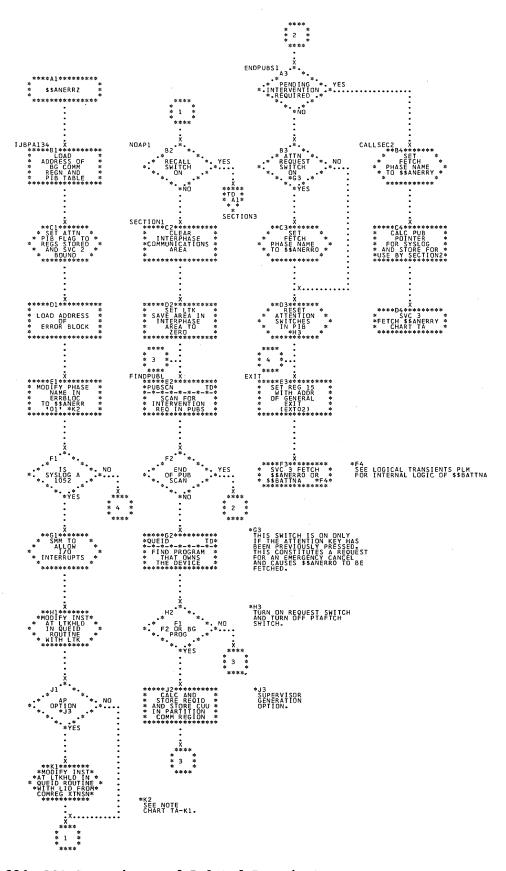


Chart TC. \$\$ANERRZ - Physical Attention Routine: Initial PUB Scan Refer to Chart 15.



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Chart TD. \$\$ANERRZ - Physical Attention Routine: Cancel Refer to Chart 15.

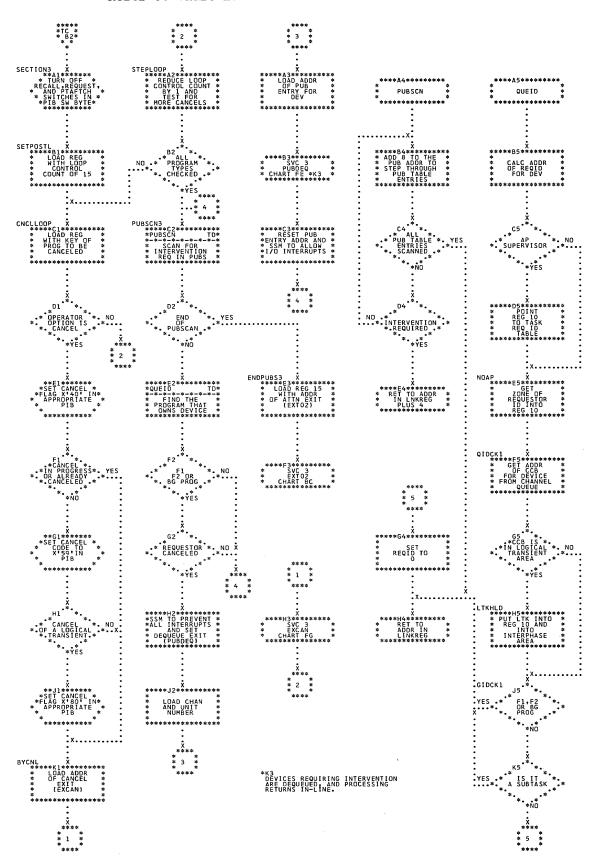
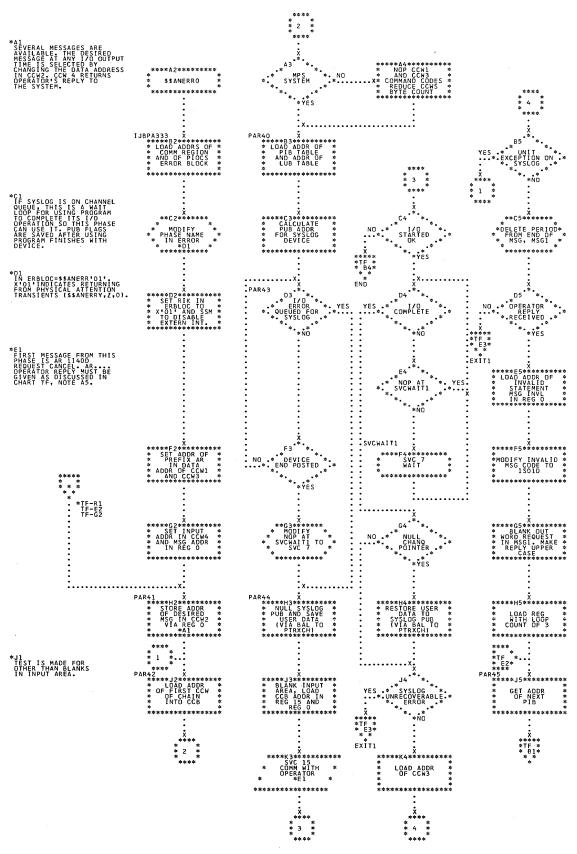


Chart TE. \$\$ANERRO - Physical Attention Routine: Request Cancel (Part 1 of 2)
Refer to Chart 15.



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Chart TF. \$\$ANERRO - Physical Attention Routine: Request Cancel (Part 2 of 2) Refer to Chart 15.

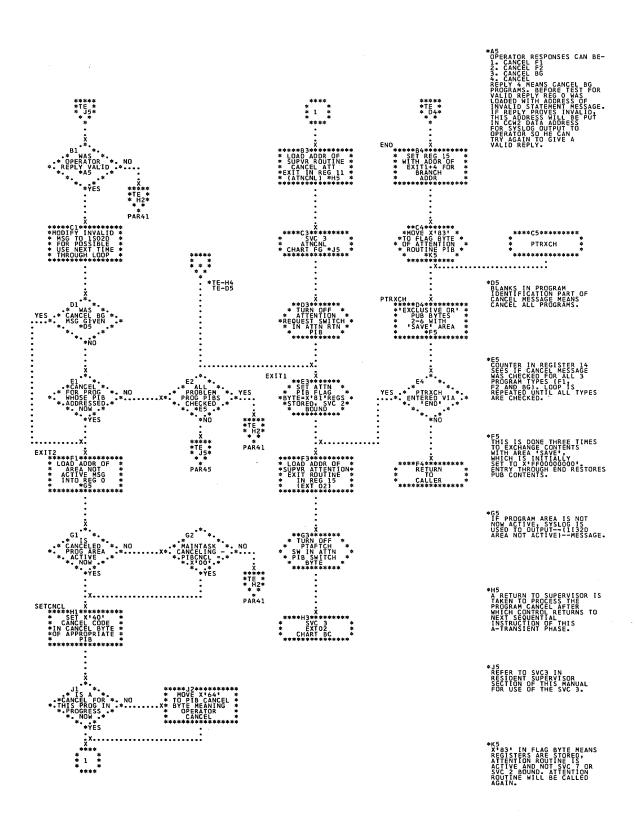
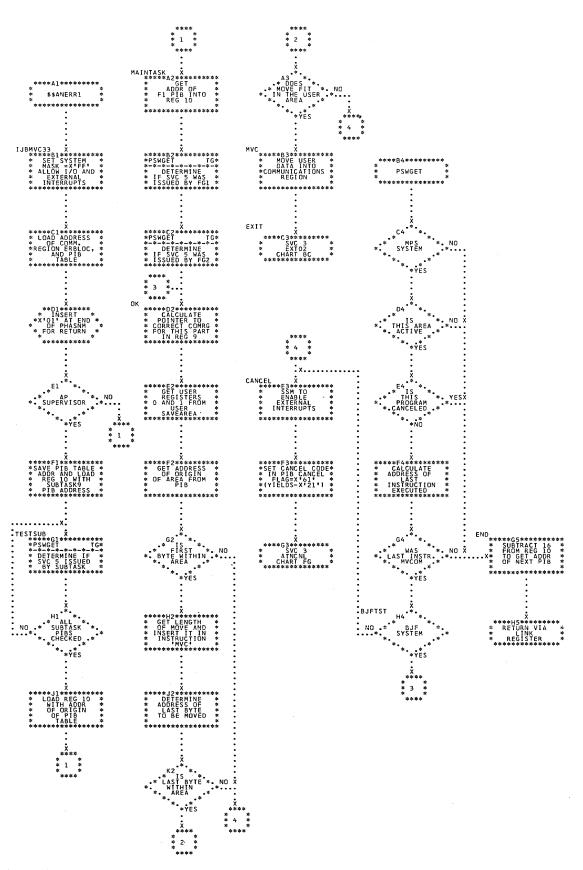


Chart TG. \$\$ANERR1 - Move Data to Communications Region



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Chart UA. \$\$ANERR9 - Optical Reader ERP (Part 1 of 2) Refer to Chart 11.

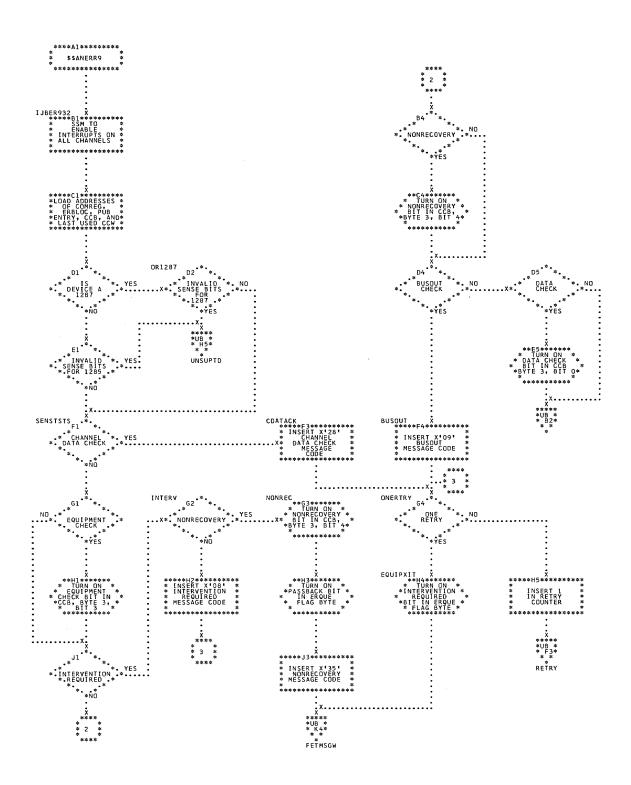
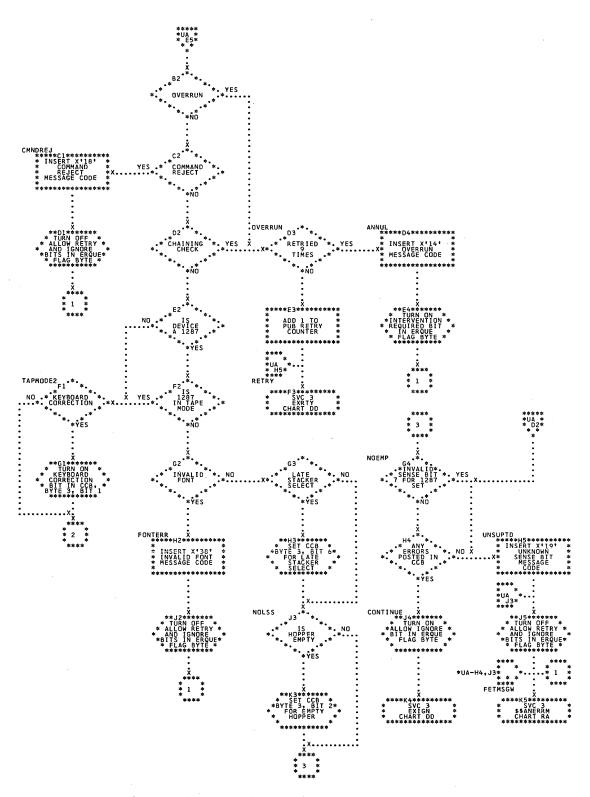


Chart UB. \$\$ANERR9 - Optical Reader ERP (Part 2 of 2) Refer to Chart 11



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Chart UC. \$\$ANERR6 - Phase 1 of 2495 ERP (Part 1 of 2) Refer to Chart 11.

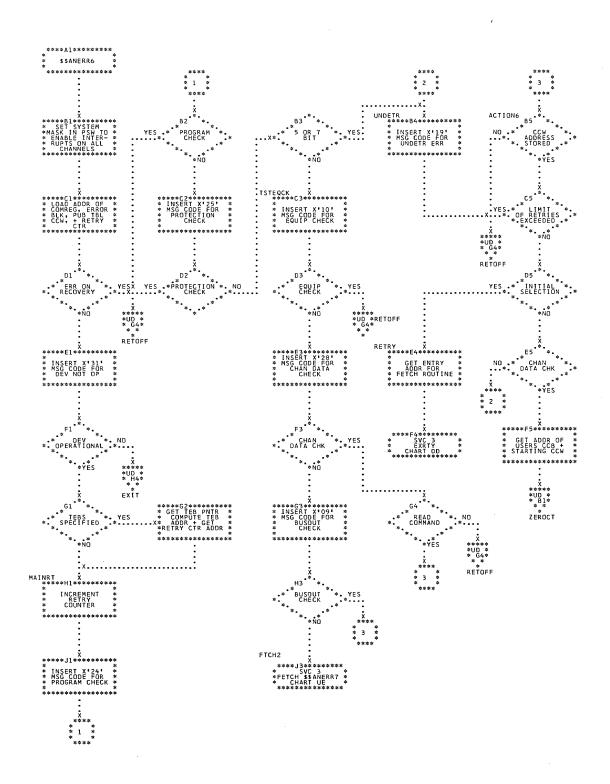
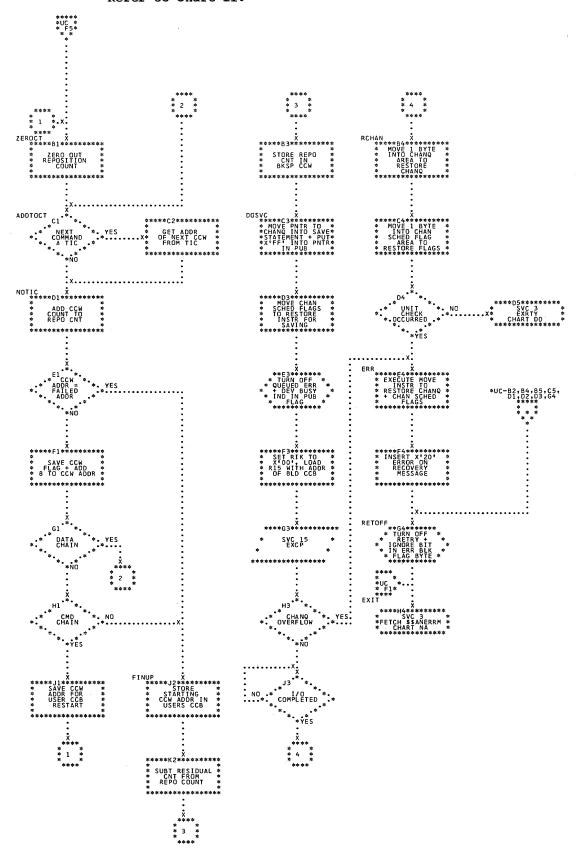


Chart UD. \$\$ANERR6 - Phase 1 of 2495 ERP (Part 2 of 2)
Refer to Chart 11.



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Chart UE. \$\$ANERR7 - Phase 2 of 2495 ERP Refer to Chart 11.

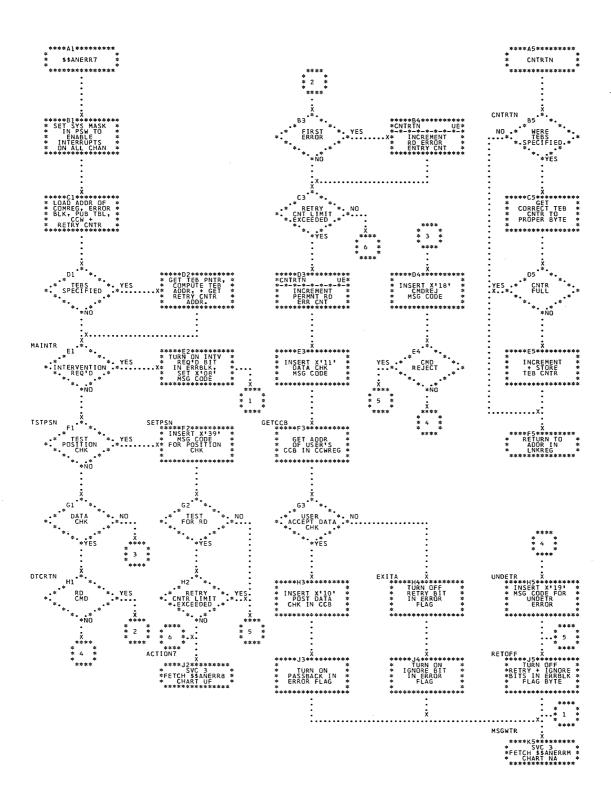
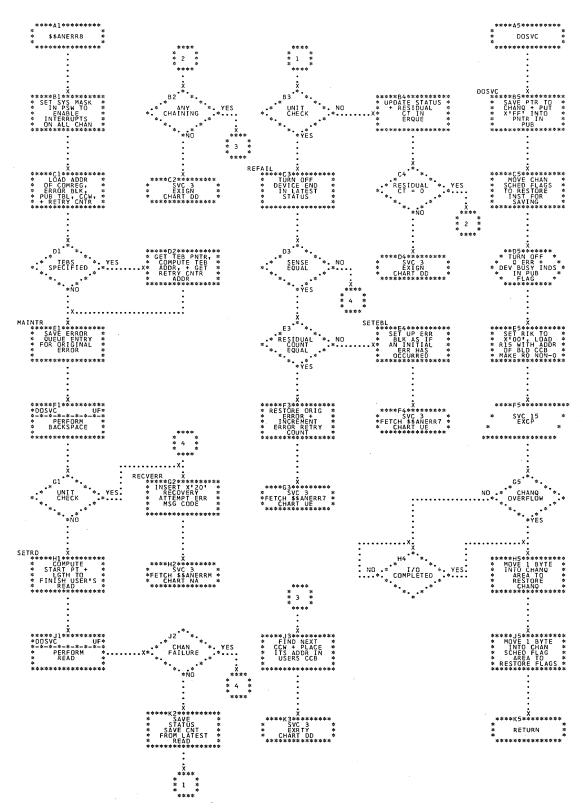


Chart UF. \$\$ANERR8 - Phase 3 of 2495 ERP Refer to Chart 11.



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Chart UG. \$\$ANERAI - Phase 1 of 1017/1018 Paper Tape ERP Refer to Chart 12.

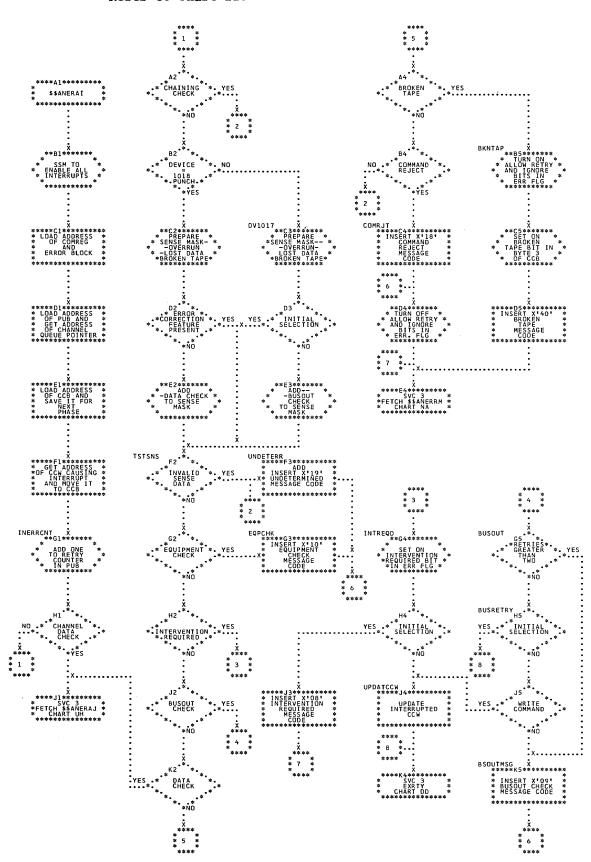


Chart UH. \$\$ANERAJ - Phase 2 of 1017/1018 Paper Tape ERP (Part 1 of 2) Refer to Chart 12.

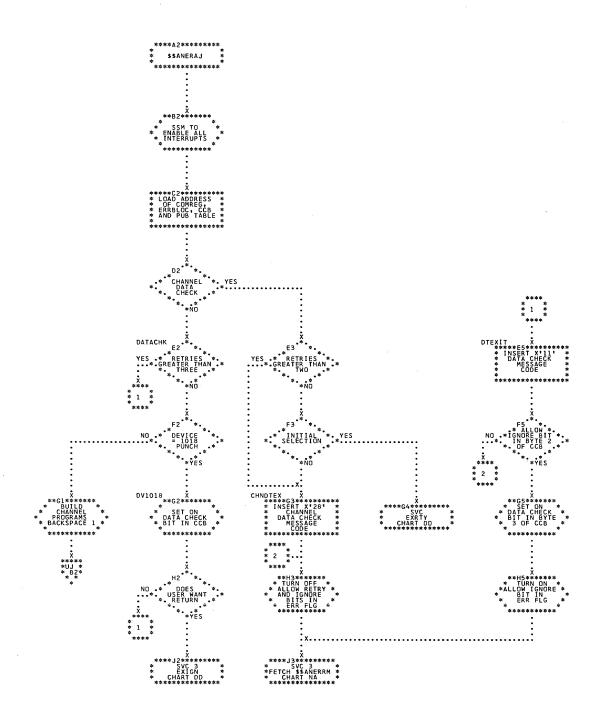


Chart UJ. \$\$ANERAJ - Phase 2 of 1017/1018 Paper Tape ERP (Part 2 of 2) Refer to Chart 12.

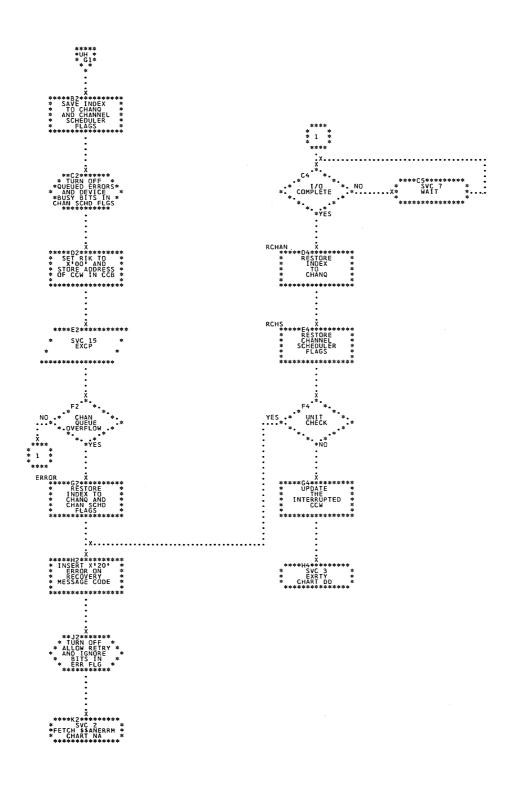


Chart UK. \$\$ANERSA - 3211 Printer ERP (Phase 1) (Part 1 of 4) Refer to Chart 12.

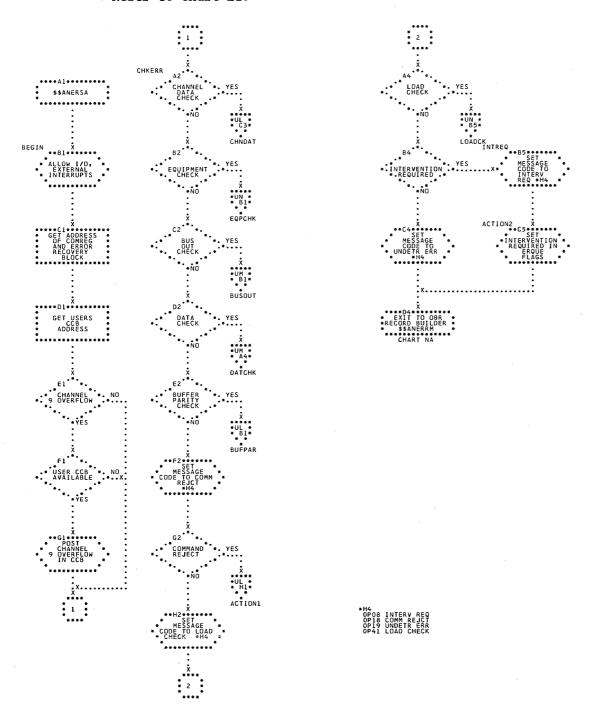


Chart UL. \$\$ANERSA - 3211 Printer ERP (Phase 1) (Part 2 of 4) Refer to Chart 12.

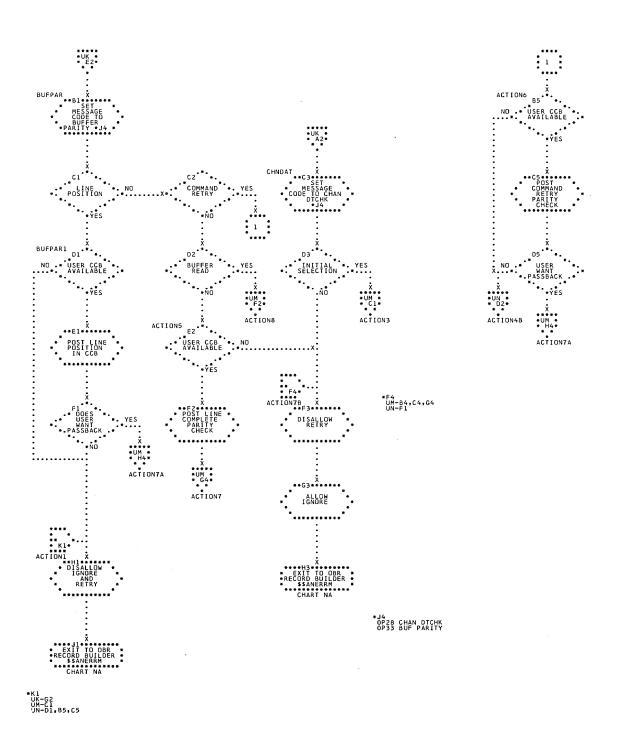


Chart UM. \$\$ANERSA - 3211 Printer ERP (Phase 1) (Part 3 of 4) Refer to Chart 12.

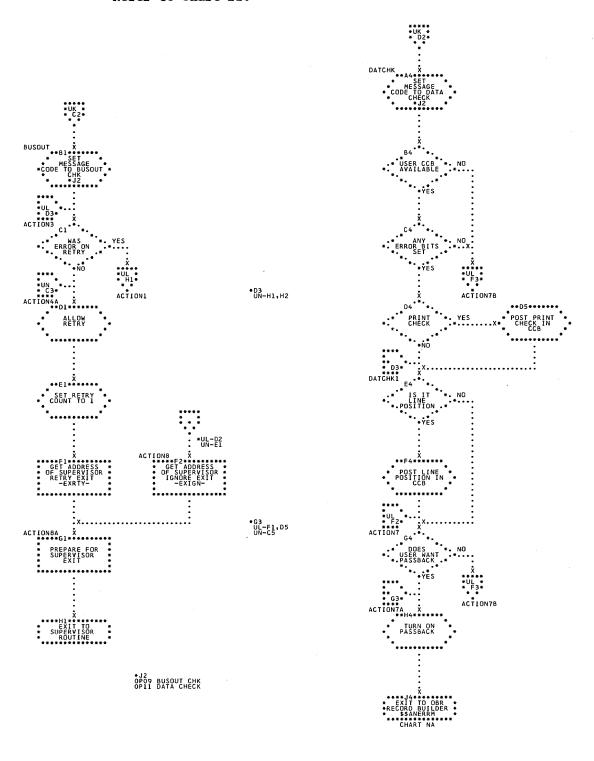


Chart UN. \$\$ANERSA - 3211 Printer ERP (Phase 1) (Part 4 of 4) Refer to Chart 12.

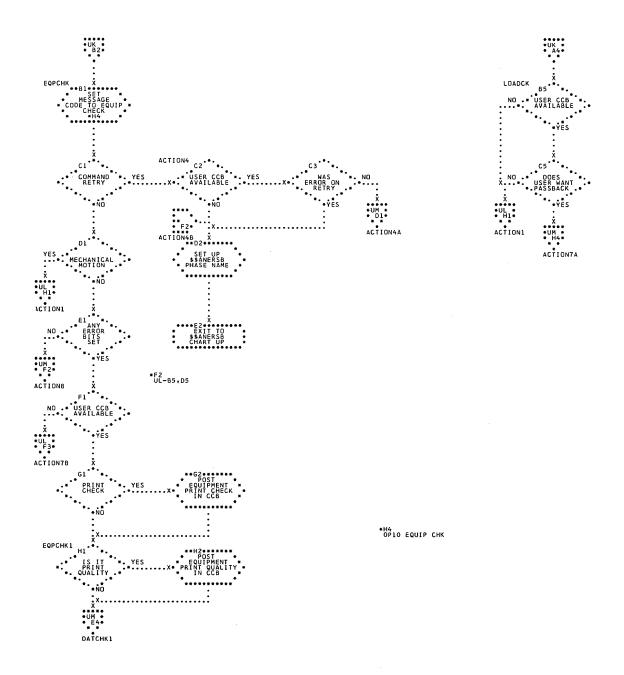
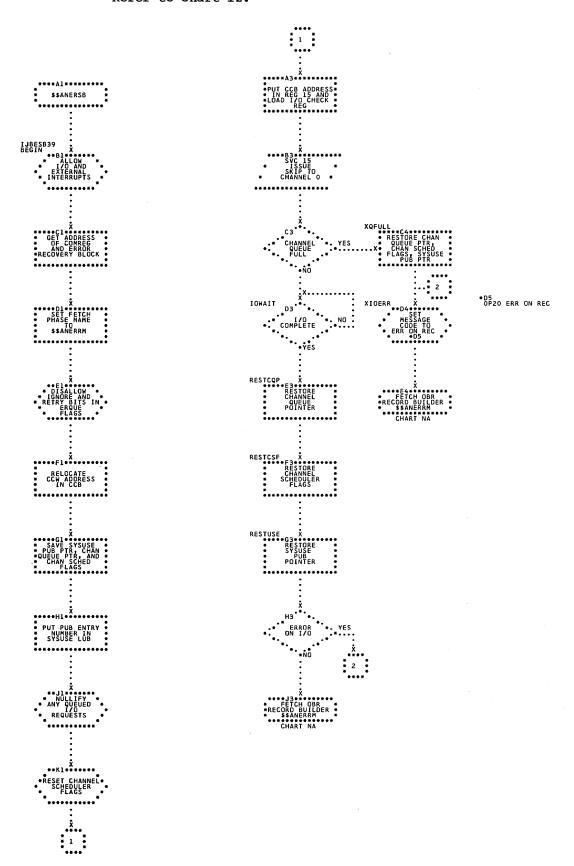


Chart UP. \$\$ANERSB - 3211 Printer ERP (Phase 2) Refer to Chart 12.



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Chart UQ. \$\$ANERSC - 3211 OBR Record Builder (Part 1 of 2) Refer to Chart 12.

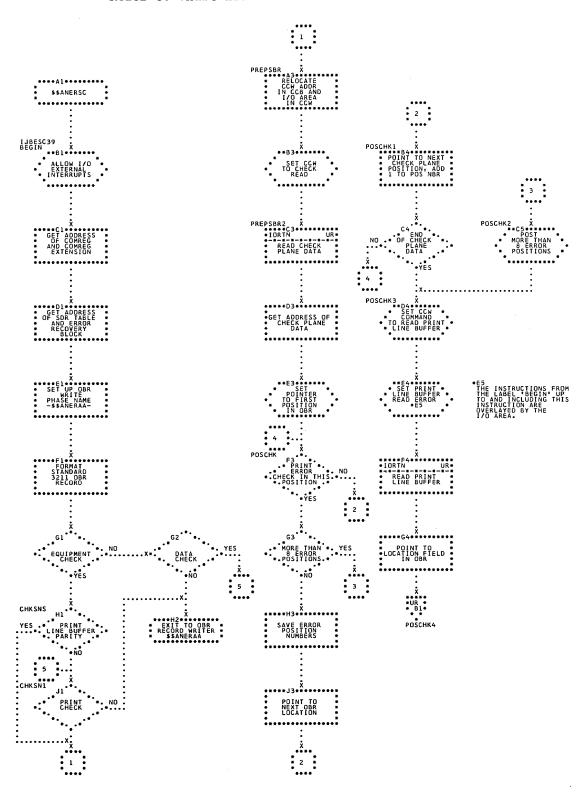


Chart UR. \$\$ANERSC - 3211 OBR Record Builder (Part 2 of 2) Refer to Chart 12.

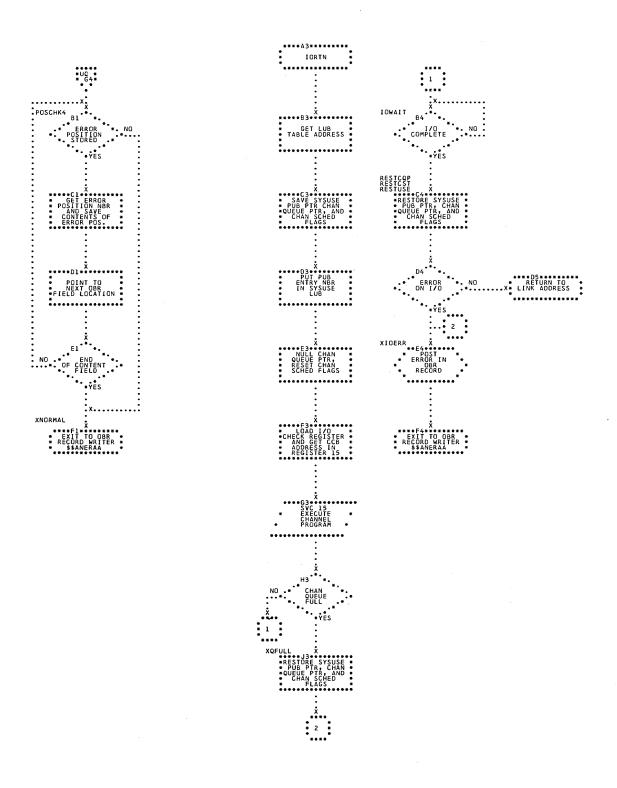


Chart VA. \$\$RAST00 - Initial MCAR/CCH Analysis (Part 1 of 4) Refer to Figure 54.

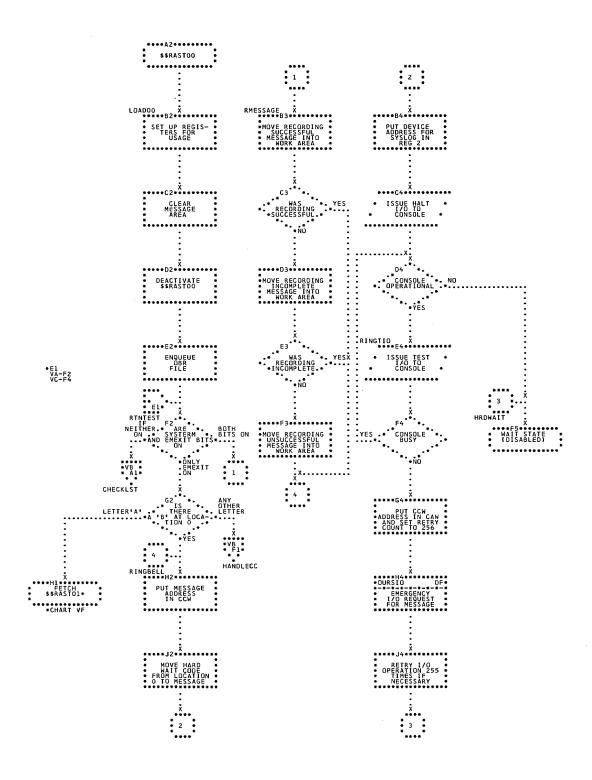


Chart VB. \$\$RAST00 - Initial MCAR/CCH Analysis (Part 2 of 4) Refer to Figure 54.

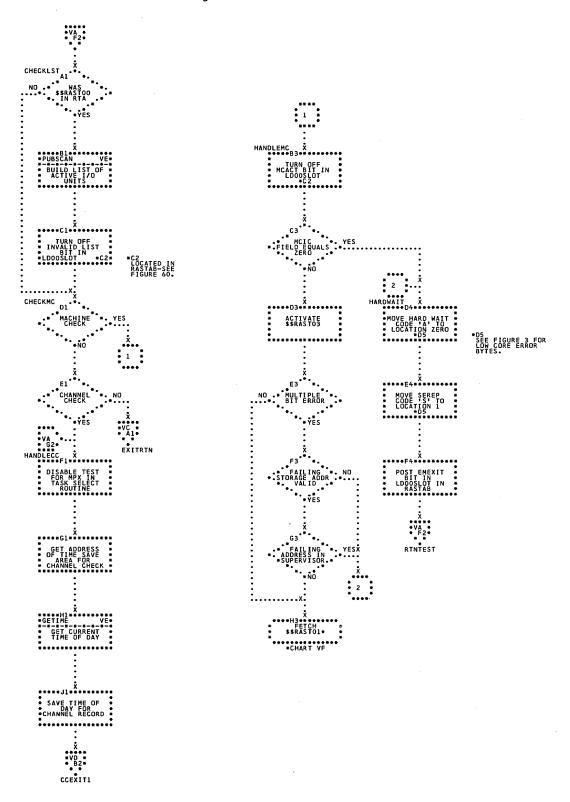


Chart VC. \$\$RAST00 - Initial MCAR/CCH Analysis (Part 3 of 4) Refer to Figure 54.

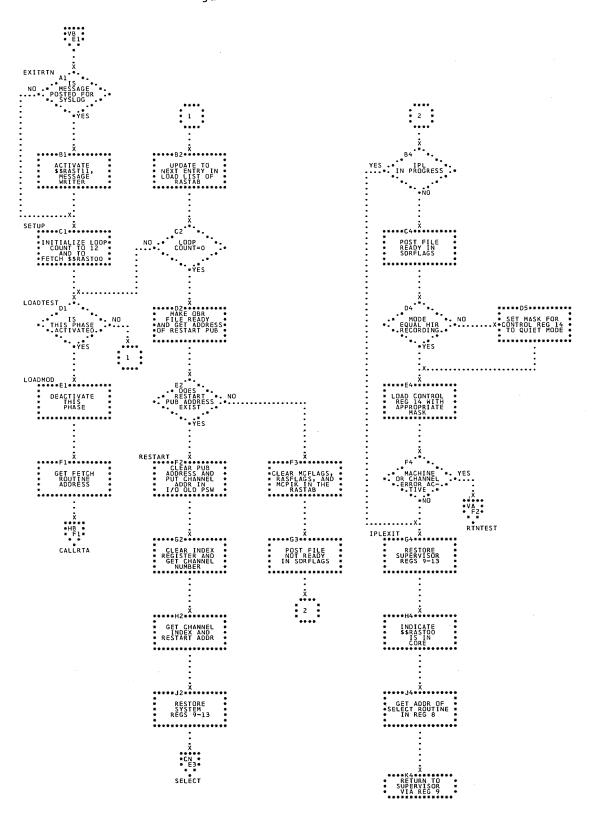


Chart VD. \$\$RAST00 - Initial MCAR/CCH Analysis (Part 4 of 4) Refer to Figure 54.

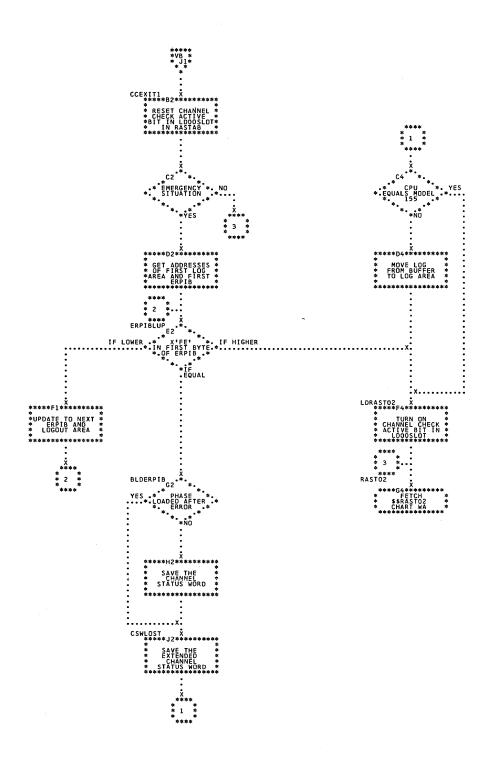


Chart VE. \$\$RAST00 - Subroutines Refer to Figure 54.

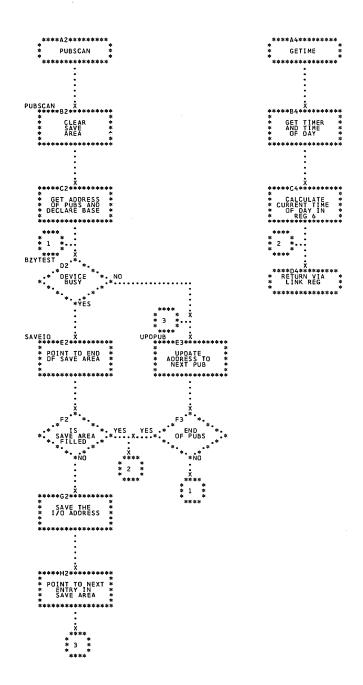


Chart VF. \$\$RAST01 - MCAR/CCH Record Builder (Part 1 of 5) Refer to Figure 54.

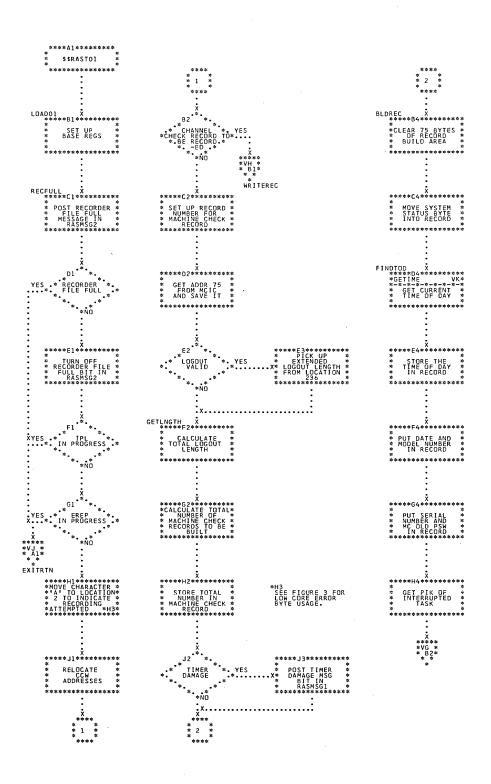


Chart VG. \$\$RAST01 - MCAR/CCH Record Builder (Part 2 of 5) Refer to Figure 54.

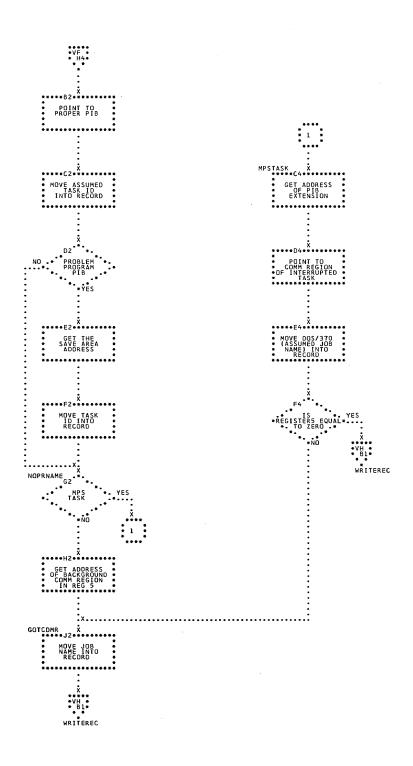


Chart VH. \$\$RAST01 - MCAR/CCH Record Builder (Part 3 of 5) Refer to Figure 54.

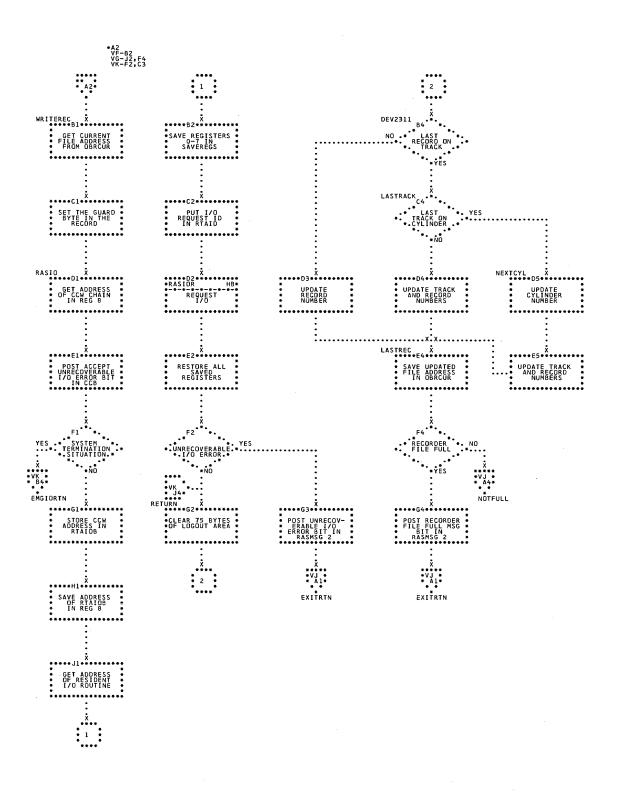
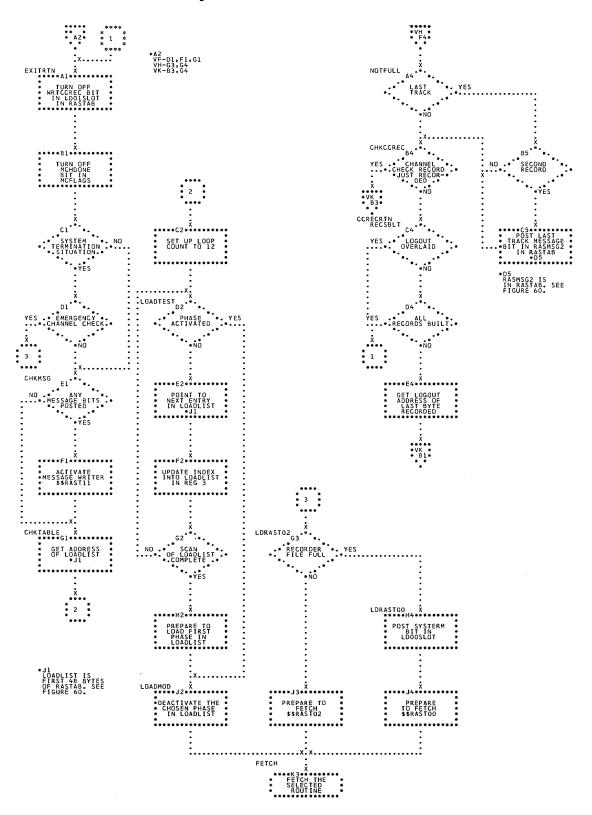


Chart VJ. \$\$RAST01 - MCAR/CCH Record Builder (Part 4 of 5)
Refer to Figure 54.



\$\$RAST01 - MCAR/CCH Record Builder (Part 5 of 5)
Refer to Figure 54. Chart VK.

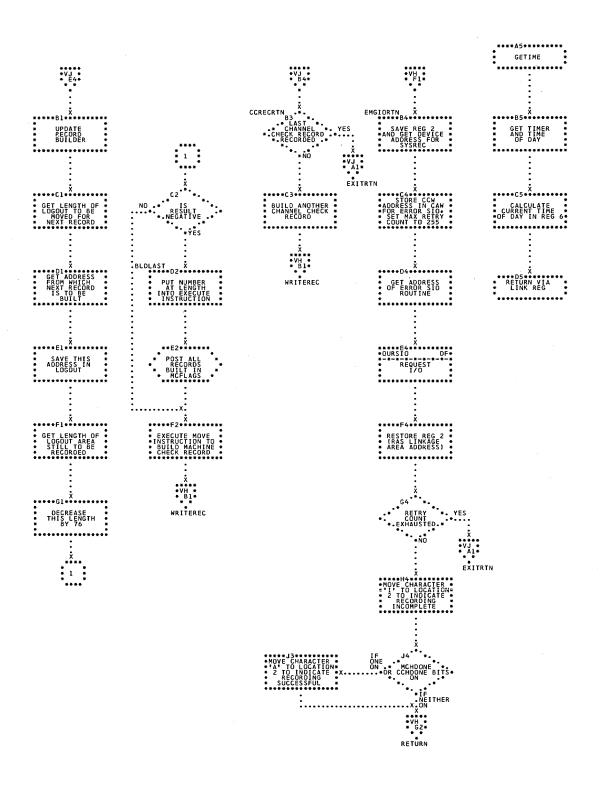


Chart WA. \$\$RAST02 - Nonresident Channel Check Handler (Part 1 of 3) Refer to Figure 54.

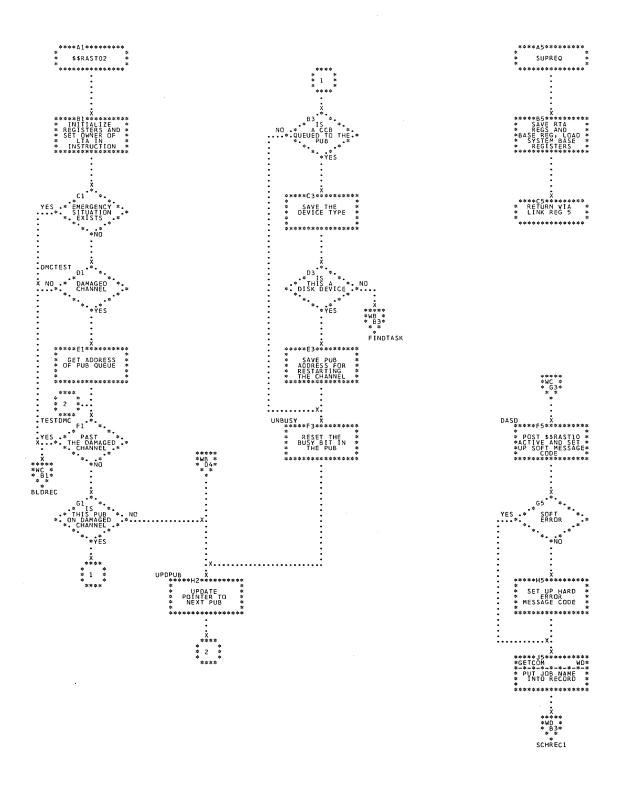


Chart WB. \$\$RAST02 - Nonresident Channel Check Handler (Part 2 of 3) Refer to Figure 54.

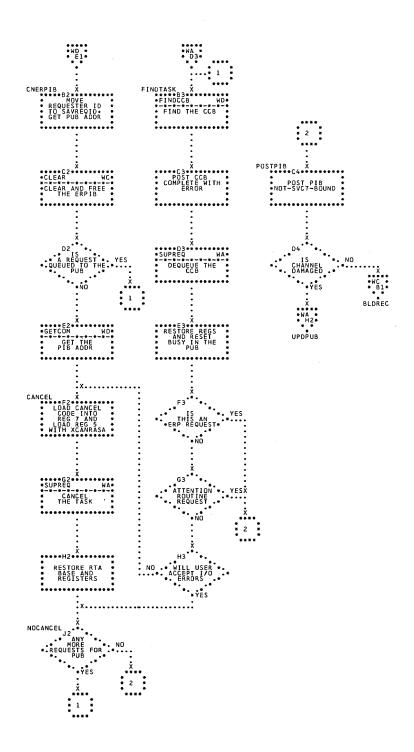


Chart WC. \$\$RAST02 - Nonresident Channel Check Handler (Part 3 of 3) Refer to Figure 54.

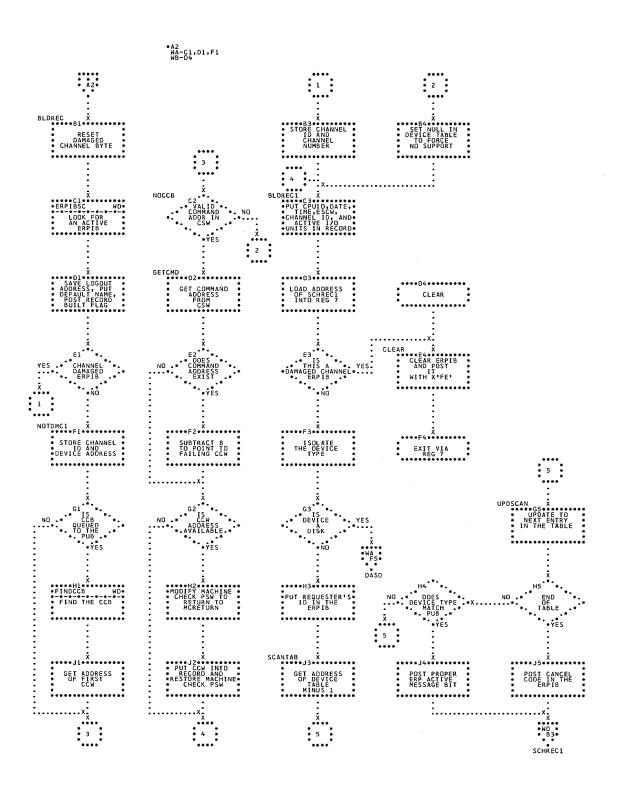
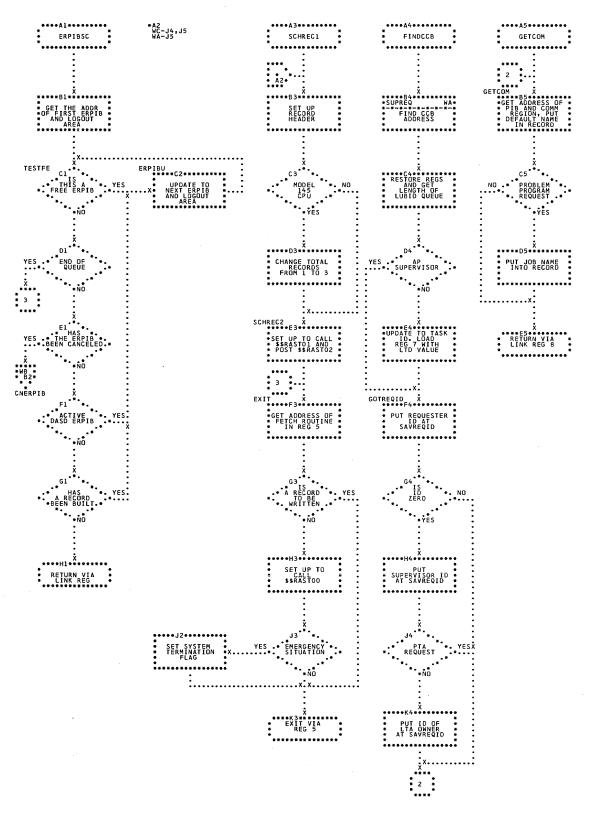


Chart WD. \$\$RAST02 - Subroutines Refer to Figure 54.



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Chart WE. \$\$RAST03 - Machine Check Repair / EFL Functions (Part 1 of 4) Refer to Figure 54.

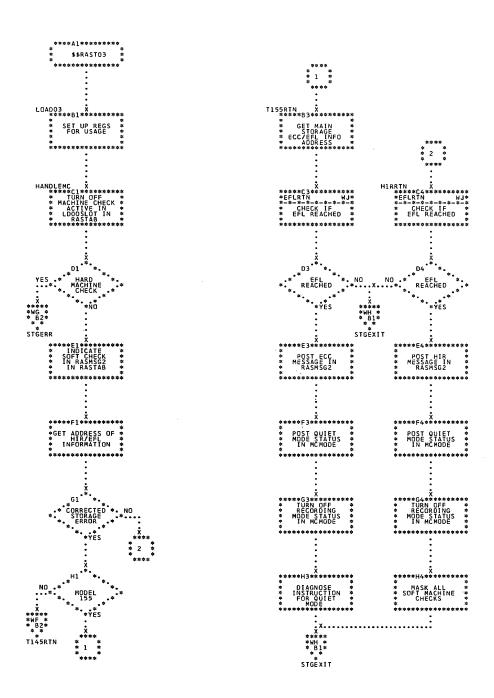


Chart WF. \$\$RAST03 - Machine Check Repair / EFL Functions (Part 2 of 4) Refer to Figure 54.

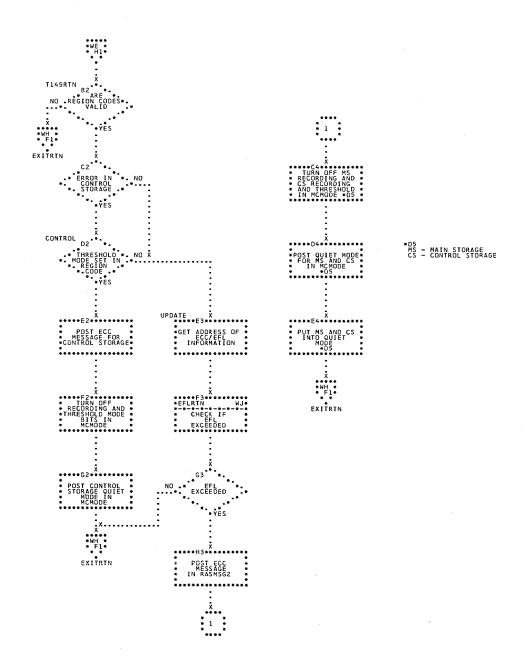


Chart WG. \$\$RAST03 - Machine Check Repair / EFL Functions (Part 3 of 4) Refer to Figure 54.

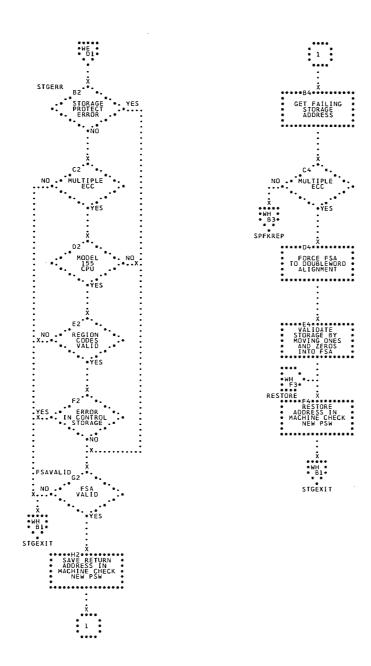
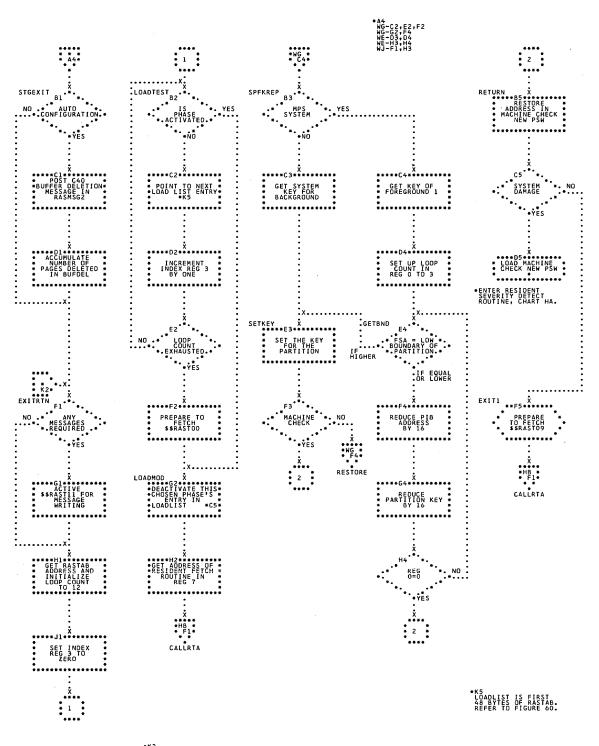


Chart WH. \$\$RAST03 - Machine Check Repair / EFL Functions (Part 4 of 4) Refer to Figure 54.



*K2 WF-B2,G2,E4

Chart WJ. \$\$RAST03 - Subroutines Refer to Figure 54.

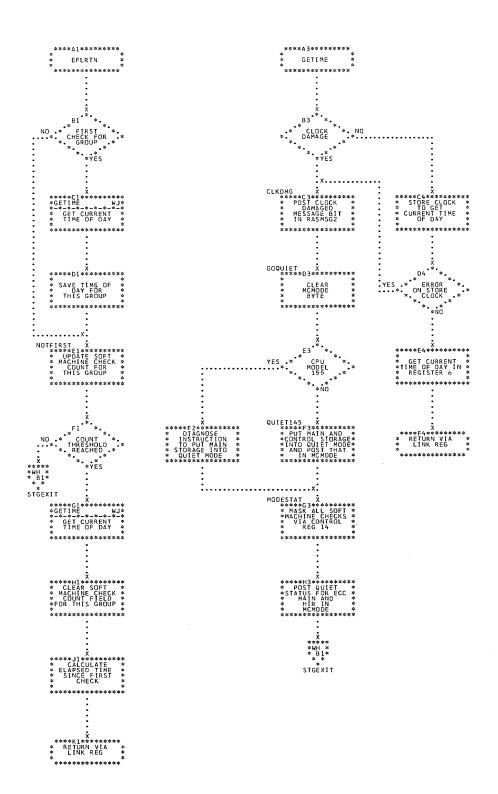
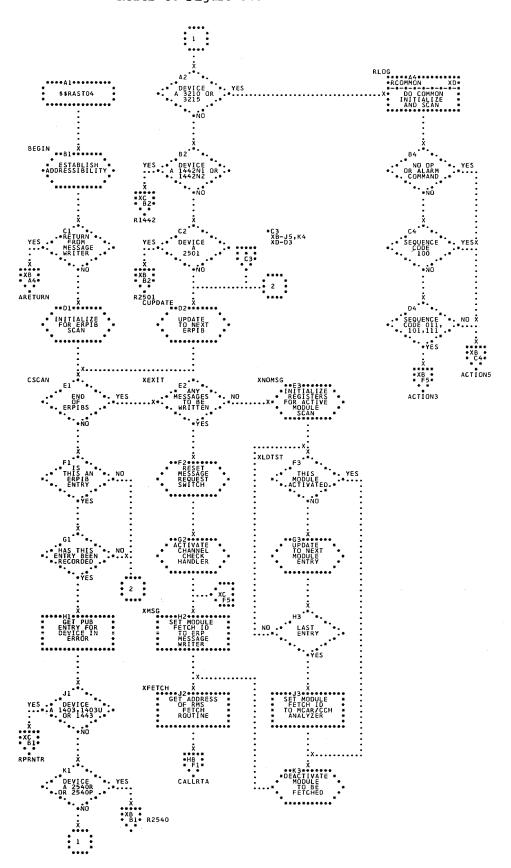


Chart XA. \$\$RAST04 - Unit Record Channel Check ERP (Part 1 of 4) Refer to Figure 54.



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Chart XB. \$\$RAST04 - Unit Record Channel Check ERP (Part 2 of 4) Refer to Figure 54.

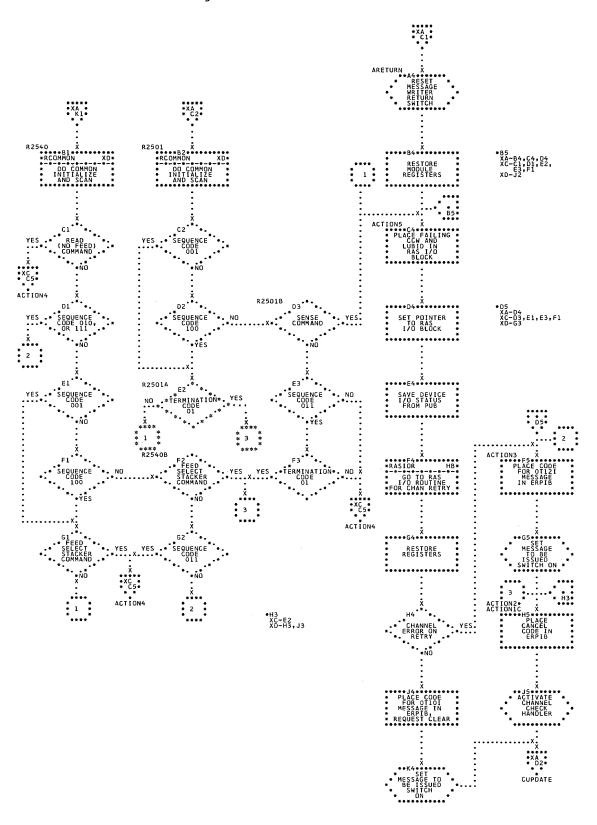


Chart XC. \$\$RAST04 - Unit Record Channel Check ERP (Part 3 of 4) Refer to Figure 54.

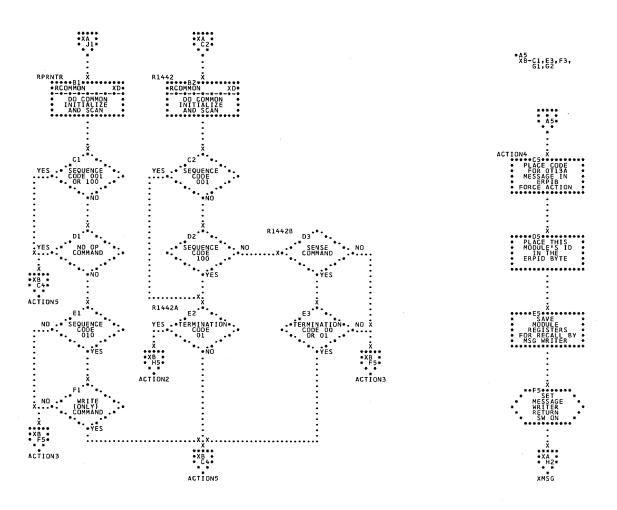


Chart XD. \$\$RAST04 - Unit Record Channel Check ERP (Part 4 of 4) Refer to Figure 54.

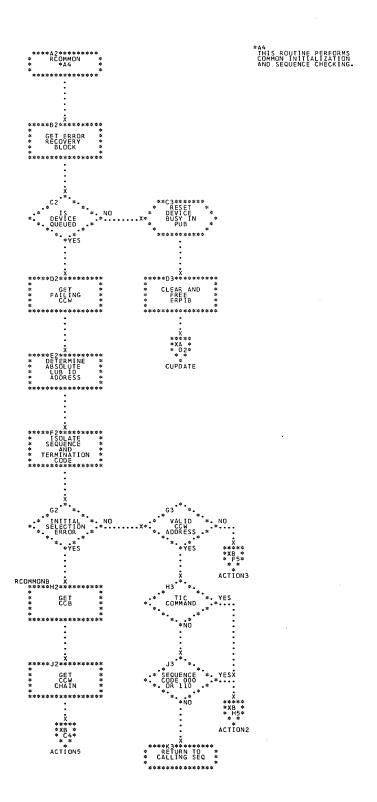
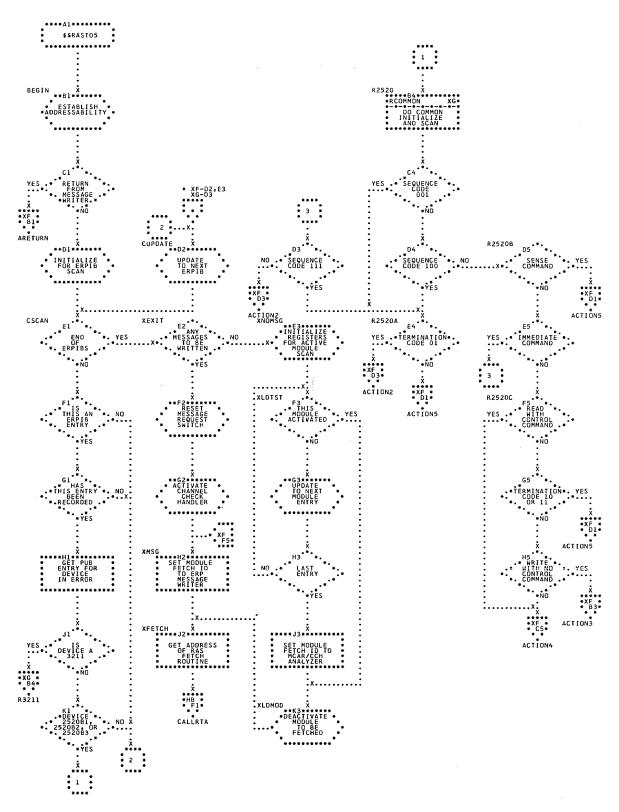
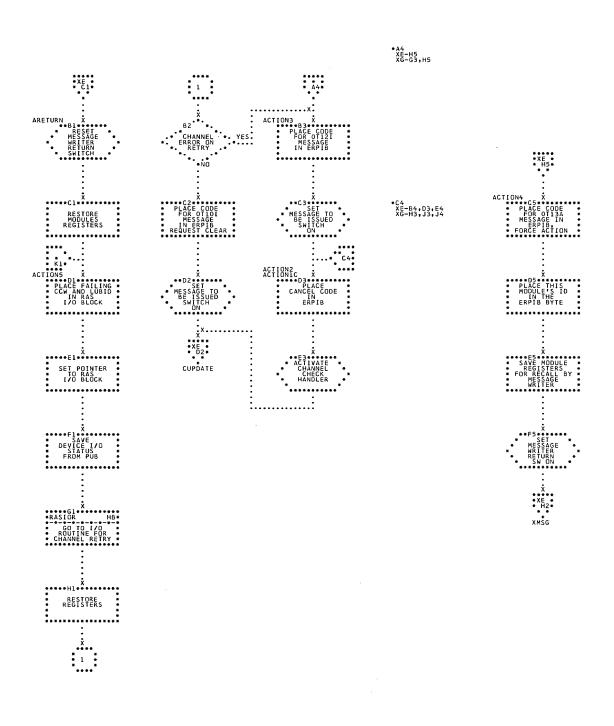


Chart XE. \$\$RAST05 - 2520 Channel Check ERP (Part 1 of 3) Refer to Figure 54.



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Chart XF. \$\$RAST05 - 2520 Channel Check ERP (Part 2 of 3) Refer to Figure 54.



*K1 XE-D5,E4,G5 XG-J2,C4,F4 XG-G4,H4,E5

Chart XG. \$\$RAST05 - 2520 Channel Check ERP (Part 3 of 3) Refer to Figure 54.

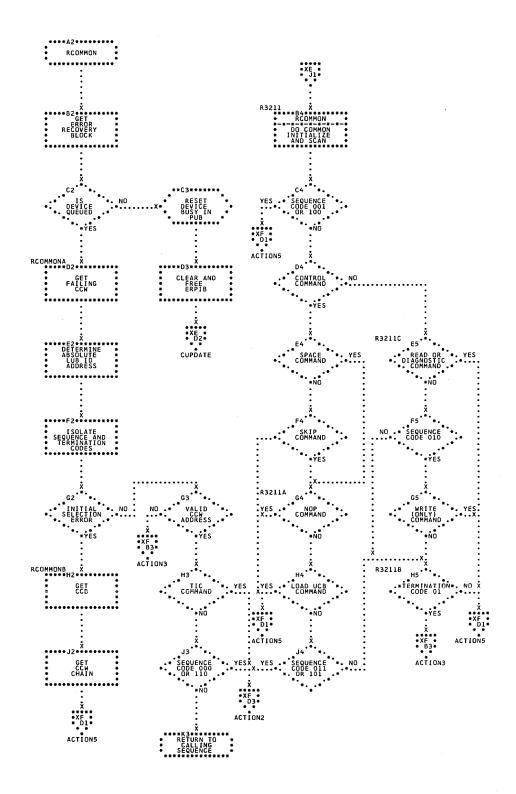


Chart XH. \$\$RAST07 - Channel Check Handler, Tape ERP (Part 1 of 2) Refer to Figure 54.

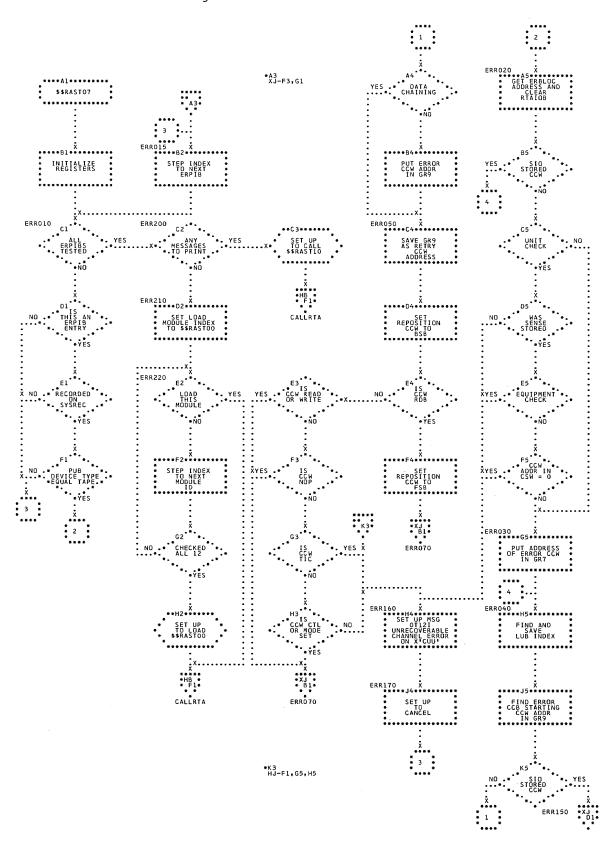


Chart XJ. \$\$RAST07 - Channel Check Handler, Tape ERP (Part 2 of 2) Refer to Figure 54.

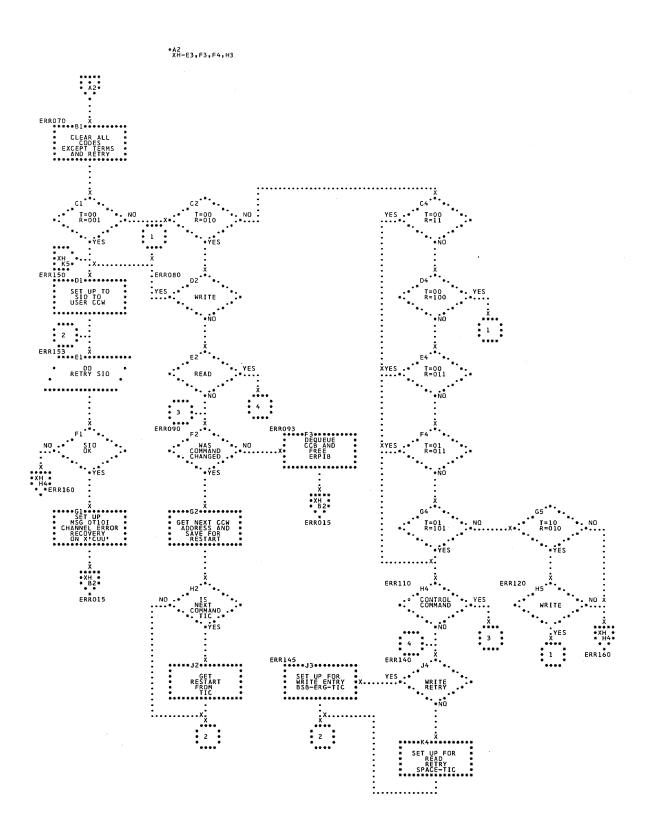


Chart XJA. \$\$RAST09 - Dynamic Reallocation of Partition (Part 1 of 2) Refer to Figure 54.

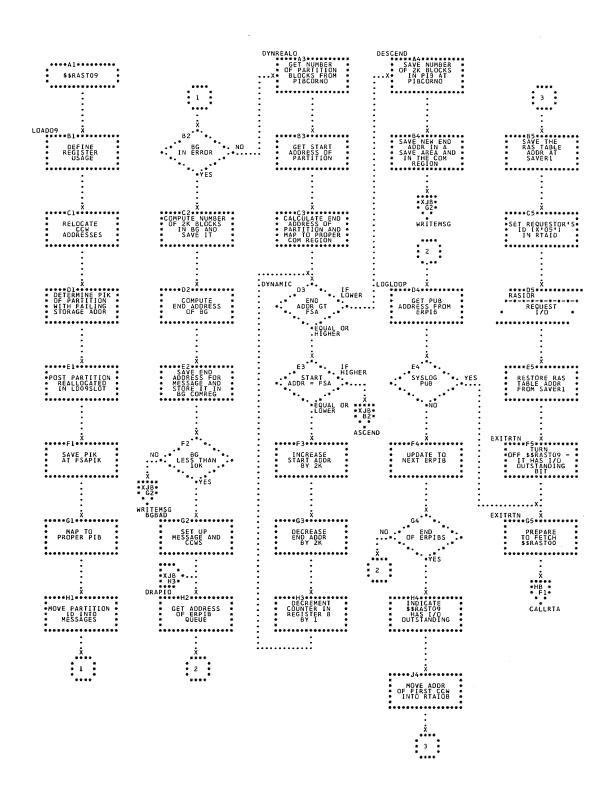
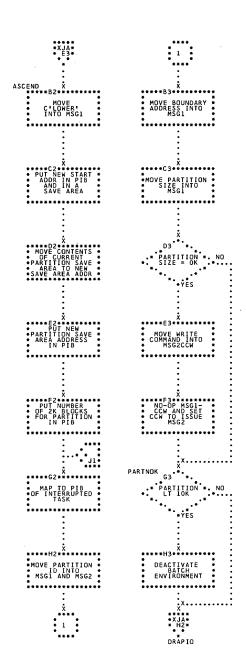


Chart XJB. \$\$RAST09 - Dynamic Reallocation of Partition (Part 2 of 2) Refer to Figure 54.



*J1 XJA-F2,B4

Chart XK. \$\$RAST10 - ERP Message Writer (Part 1 of 3) Refer to Figure 54.

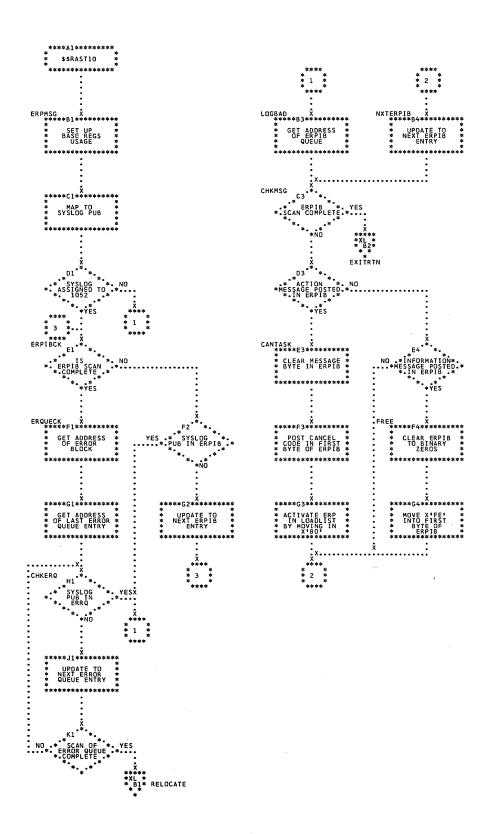


Chart XL. \$\$RAST10 - ERP Message Writer (Part 2 of 3) Refer to Figure 54.

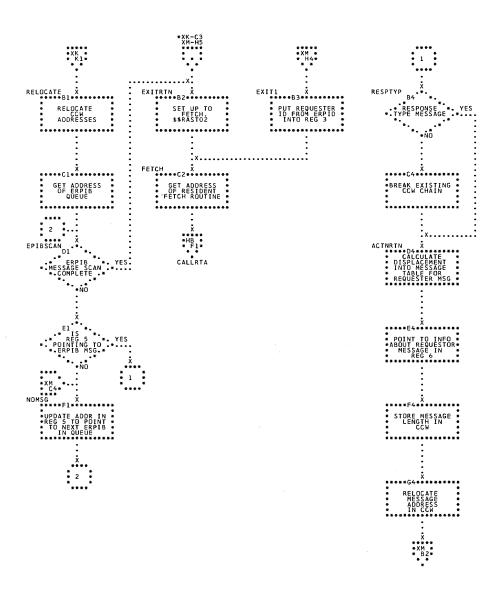


Chart XM. \$\$RAST10 - ERP Message Writer (Part 3 of 3) Refer to Figure 54.

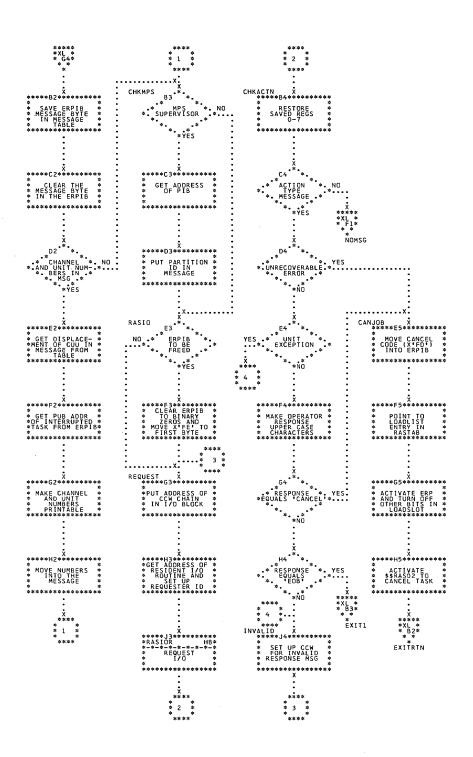
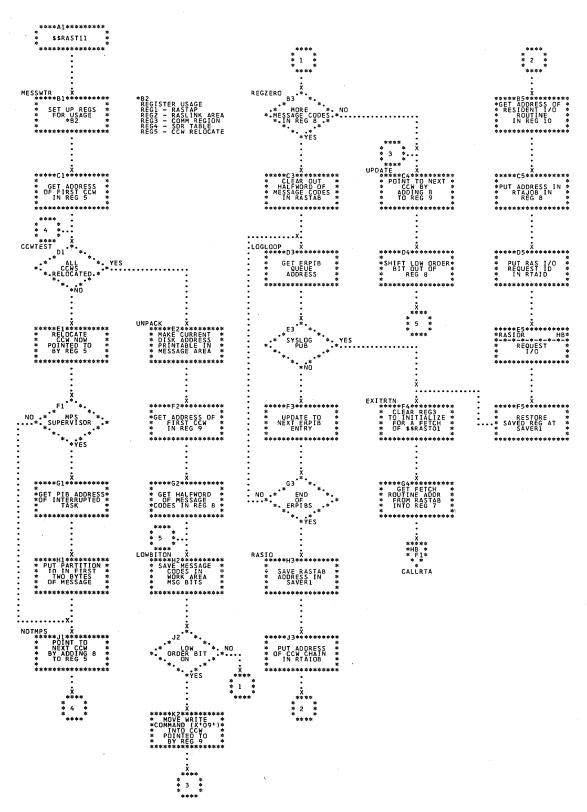


Chart XN. \$\$RAST11 - RTA Message Writer Refer to Figure 54.



390 DOS Supervisor and Related Transients

	Dhaga or		D TEMOM	<u> </u>	mc.
7-b-1	Phase or	Obasit	BJFTST	\$\$ANERR1	TG
<u>Label</u>	Macro	<u>Chart</u>	BKNTAP	\$\$ANERAI	UG
			BLDERPIB	\$\$RAST00	VD
AACT	\$\$ANERRU	SC	BLDLAST	\$\$RAST01	VK
AACTION	\$\$ANERRP	RF	BLDREC	\$\$RAST01	VF
ABTRANS	SGDFCH	EC	BLDREC	\$\$RAST02	WC
ACTIONA	\$\$ANERRP	RE	BLDREC1	\$\$RAST02	WC
ACTION1	\$\$ANERSA	UL	BSOUT	\$\$ANERRW	SG
ACTION1C	\$\$RAST04	XB	BSOUTMSG	\$\$ANERAI	UG
ACTION1C	\$\$RAST05	XF	BSTTST	SGUNCK	DA
ACTION2	\$\$ANERSA	UK	BTAM	\$\$ANERRC	NM
ACTION3	SSANERSA	UM	BUFPAR	SSANERSA	\mathbf{UL}
ACTION3	\$\$RAST04	XB	BUS	SSANERRX	SK
ACTION3	\$\$RAST05	XF	BUSOUT	\$\$ANERRA	NLA
ACTION4	\$\$ANERSA	UN	BUSOUT	\$\$ANERRV	SE
ACTION4	\$\$RAST04	XC	BUSOUT	\$\$ANERRW	SF
ACTION4	\$\$RAST05	XF	BUSOUT	\$\$ANERR9	UA
ACTION4A	\$\$ANERSA	UM	BUSOUT	\$\$ANERAI	UG
		UN			UM
ACTION4B	\$\$ANERSA		BUSOUT	\$\$ANERSA	
ACTION5	\$\$ANERSA	UL.	BUSRETRY	\$\$ANERAI	UG
ACTION5	\$\$RAST04	XB	BUS1	\$\$ANERRV	SE
ACTION5	\$\$RAST05	XF	BUS 2	\$\$ANERRV	SE
ACTION6	\$\$ANERSA	UL	BYCNL	\$\$ANERRZ	TD
ACTION6	\$\$ANERR6	UC	BY1	\$\$ANERRM	NB
ACTION7	\$\$ANERSA	UM	BZYTEST	\$\$RAST00	VE
ACTION7	\$\$ANERR7	UE	B01	\$\$ANERRG	QΑ
ACTION7A	\$\$ANERSA	UM	B02	\$\$ANERRG	QA
ACTION7B	\$\$ANERSA	UL		• •	
ACTION8	\$\$ANERSA	UM			
ACTION8A	\$\$ANERSA	UM	CALFET	SGSVC	FF
ACTNRTN	\$\$RAST10	XL	CALLMW	\$\$ANERRX	SJ
ADDTOCT	\$\$ANERR6	UD	CALLRTA	MCRAS	HB
AFTTIO	SGUNCK	DF	CALLSEC2	\$\$ANERRZ	TC
ALLBND	FOPT	BCA	CALLSEC3	\$\$ANERRY	TB
ALLBND1	FOPT	BCA	CALLO	MCRAS	HB
			CALPH4		RD
ANNUL	\$\$ANERR9	UB		\$\$ANERRO	
APTEST	\$\$ANERAE	RC	CALPH5	\$\$ANERRP	RF
ARETURN	\$\$RAST04	XB	CANALL	SGTHAP	MM
ARETURN	\$\$RAST05	XF	CANCEL	\$\$ANERR1	TG
ARND1	\$\$ANERRU	SC	CANCEL	\$\$RAST02	WB
ASCEND	\$\$RAST09	ХЈВ	CANCOD	\$\$ANERRS	RL
ATNCNL	SGSVC	FG	CANCON	\$\$ANERRX	SK
ATNRTN	SGTCON	GD	CANJOB	\$\$RAST10	MX
ATYPE	\$\$ANERRV	SE	CANRTN	\$\$ANERRS	\mathtt{RL}
ATYPE	\$\$ANERRX	SK	CANTASK	\$\$RAST10	XK
ATYPE	\$\$ANERRN	RB	CANTLP	\$\$ANERRY	TA
A01	\$\$ANERRG	Q A	CANXIT	FOPT	BE
A02	\$\$ANERRG	QA	CBGOA	SGSVC	FQ
A03	\$\$ANERRJ	QF	CBMOV	SGSVC	FP
A05	\$\$ANERRJ	QF	CBNON1	SGTCHS	CCA
A06	\$\$ANERRJ	QF	CBNON2	SGTCHS	CCA
A2321	SGTCHS	CH	CBOK	SGSVC	FP
	5010115		CBRET	SGTCHS	CC
			CCBOED	SGUNCK	DB
BALMSG	\$\$ANERRJ	QF	CCBSTR	\$\$ANERAB	RA
BALSTCHK	\$\$ANERRJ	QF	CCBUNAV	\$\$ANERAE	RC
BEGIN	\$\$ANERSA	UK	CCDADI	MCRAS	HH
BEGIN	\$\$ANERSA	UP	CCDAMAGE	MCRAS	HD
BEGIN	\$\$ANERSA	UQ	CCDASDCK	MCRAS	HH
BEGIN	\$\$RAST04	XA	CCDASDI	MCRAS	нн
BEGIN	\$\$RAST05	XE	CCDASDLT	MCRAS	HH
BGBAD	\$\$RAST09	ХJА	CCDASDTC	MCRAS	НН

CCDEVTST	MCRAS	HE	CNCEL	SGTHAP	MK
	MCRAS	HD	CNCELL	SGTHAP	MK
CCDEXIT					
CCENTRY1	MCRAS	HD	CNCEL0	SGTHAP	MK
CCENTRY2	MCRAS	HE	CNCEL1	SGTHAP	ML
CCENTRY3	MCRAS	HE	CNCEL1A	SGTHAP	ML
CCEREXIT	MCRAS	HD	CNCEL1B	SGTHAP	ML
CCEXIT1	MCRAS	HD	CNCEL2	SGTHAP	MK
CCEXIT1	\$\$RAST00	V D	CNCEL2AA	SGTHAP	MK
CCEXIT2	MCRAS	HE	CNCEL3	ŞGTHAP	ML
CCEXIT3	MCRAS	HF			
CCEXIT4	MCRAS	HF	CNCEL4	SGTHAP	ML
CCNOT10	MCRAS	HF	CNCEL5	SGTHAP	ML
CCRECRTN	\$\$RAST01	VK	CNCL	FOPT	\mathbf{BE}
CCRTYTST	MCRAS	HE	CNCL	\$\$ANERRU	SC
				7 1	
CCSETDMC	MCRAS	HD	CNCLLOOP	\$\$ANERRZ	TD
CCT155	MCRAS	HF	CNCLSW	\$\$ANERRY	TB
CCWTEST	\$\$RAST11	XN	CNERPIB	\$\$RAST02	WB
CDATACK	\$\$ANERR9	UA	CNLSVE	FOPT	BA
	• •				
CDC	\$\$ANERRW	SG	CNO	\$\$ANERRU	SB
CEDETST	SGTCHS	CL	CNTEXT	\$\$ANERRP	RE
			CNTRTN	\$\$ANERR7	UE
CHAINCH	\$\$ANERRB	NN	CNTST	\$\$ANERRV	SD
CHDTCK	\$\$ANERRX	SJ	CNTST	\$\$ANERRN	RB
	• •			• •	
CHECK	\$\$ANERRA	NL	COMBIN	\$\$ANERRA	NL
CHECKLST	\$\$RAST00	VB	COMMENCE	SSANERAD	NK
	: :				
CHECKMC	\$\$RAST00	VB	COMPCLC	SGTCHS	CA
CHEND	SGTCHS	CL	COMR	\$\$ANERRX	SJ
CHEND1	SGTCHS	CL	COMREJ	\$\$ANERRB	NN
CHFAIL	SGUNCK	DF	COMRJ	\$\$ANERRW	SH
CHFAIL1	SGUNCK	D F	COMRJT	\$\$ANERAI	ŪG
CHKACTN	\$\$RAST10	XM	CONBUF	SGSVC	\mathbf{FP}
CHKADR	\$\$ANERRT	SA	CONBUF2	SGSVC	\mathbf{FP}
CHKADR	\$\$ANERRW	SF	CONT	\$\$ANERRV	SE
				• •	SG
CHKADR	\$\$ANERRS	RK	CONT	\$\$ANERRW	
CHKAM	\$\$ANERRB	NN	CONTINU	SEND	LΑ
CHKCNT	\$\$ANERRV	SE	CONTINU	\$\$ANERAF	NG
				• •	
CHKDEV	\$\$ANERRP	RF	CONTINUE	\$\$ANERR9	UB
CHKDISK	\$\$ANERRA	NL	CONTINUE	SSANERRM	NB
	1 1			• •	
CHKERQ	\$\$RAST10	XK	CONTROL	\$\$RAST03	WF
CHKERR	SSANERSA	UK	CORCIN	SGTCHS	CK
	• •				
CHKLTA	\$\$ANERRS	RL	CORPUB	SGTCHS	CK
CHKMPS	\$\$RAST10	XM	CORPUB	SGTCHS	CK
CHKMSG	\$\$RAST01	VJ	CORREC	SGTCHS	CJ
CHKMSG	\$\$RAST10	XK	COUNT	SGTCHS	CG
	• •			SSANERRP	RE
CHKOCREC	\$\$RAST01	VJ	COUNTRG	1 1	
CHKSNS	\$\$ANERSC	ŪQ	COUNTRG	SSANERRQ	RG
CHKSN1	\$\$ANERSC	ŪQ	CQDSP	SGTCHS	CR
CHKTABLE	\$\$RAST01	VJ	CSBY2	FOPT	\mathbf{BE}
CHNDAT	ŚŚANERSA	UL	CSCAN	\$\$RAST04	XΑ
CHNDRT	SGTCHS	CP	CSCAN	\$\$RAST05	XΕ
CHNDTEX	\$\$ANERAJ	UH	CSRST	FOPT	\mathbf{BE}
	• •				
CHNERROR	SMCRR	KA	CSWCHK	SGUNCK	\mathbf{DF}
CHNOK1	SGTCHS	CK	CSWLOST	\$\$RAST00	VD
CIMMCIII		CP	CUPDATE	\$\$RAST04	XA
CHNTST	SGTCHS				
CKCHST	SGTCHS	CE	CUPDATE	\$\$RAST05	$\mathbf{x}\mathbf{E}$
CLBPRG	SGTCHS	CA	CUU	\$\$ANERRO	RD
				• •	
CLBPTR	SGTCHS	CAA	CYLEND	SGDSK	GB
CLBSUP	SGTCHS	CAA	C01	\$\$ANERRG	QB
CLCEX	SGDFCH	EC	C01	\$\$ANERRH	QD
CLCINS	SGTCHS	СН	C01	\$\$ANERRJ	QF
				: :	
CLEAR	\$\$RAST02	WC	C0100	\$\$ANERRV	SE
CLKDMG	\$\$RAST03	WJ	C02	\$\$ANERRV	SD
				* *	
CMDCHN	SGUNCK	DA			
CMDREJ	\$\$ANERRV	SE	DASD	\$\$RAST02	WA
				• •	
CMDSEQ	\$\$ANERRV	SD	DASD2311	SGTCHS	CH
CMNDREJ	\$\$ANERR9	UB	DAT	\$\$ANERRX	SJ
CMR	\$\$ANERRV	SE	DATAADDR	SGDFCH	EE
CMR	ANNTHUCC	ئدن	DWIWUDDK	DGDE CH	ظند

DATACHK	\$\$ANERRB	NN	EROSDR	\$\$ANERAC	NF
DATACHK	\$\$ANERAJ	UH	ERQUECK	\$\$RAST10	XK
	• •			• •	
DATACHK	\$\$ANERSA	UM	ERR	\$\$ANERR6	UD
DATACHK1	\$\$ANERSA	UM	ERRGO	FOPT	BB
DATCHK	\$\$ANERRV	SE	ERROR	\$\$ANERAJ	UJ
DCERP	\$\$ANERRA	NL	ERRORQED	\$\$ANERAA	NC
DEALSO	SGTCHS	CQ	ERRQUED	\$\$ANERAF	NH
DECCTR	\$\$ANERRQ	RH	ERRQUED1	\$\$ANERAG	NJ
DELKOTCK	SGTCHS	CN	ERRSEN	SGUNCK	DB
DEQUE	SGSVC	FF	ERRSET	FOPT	BB
~					
DEQUER	SGUNCK	DE	ERRSET	FOPT	$\mathbf{B}\mathbf{B}$
DEQUER1	SGUNCK	DE	ERRSET0	FOPT	BB
DEQUER1A	SGUNCK	DE	ERRSET1	FOPT	BB
DESCEND	\$\$RAST09	XJA	ERRSIO	SGUNCK	DF
DETFRE	SGTHAP	MB	ERRSIO2	SGUNCK	\mathbf{DF}
DEV2311	\$\$RAST01	VH	ERRTYP	\$\$ANERRP	RE
DISWHY	SGTCHS	CK	ERR010	\$\$ANERRE	PC
DMCTEST	\$\$RAST02	WA	ERR010	\$\$RAST07	XH
DOSVC	\$\$ANERR6	UD	ERR015	\$\$RAST07	XН
DOSVC	\$\$ANERR8	UF	ERR020	\$\$RAST07	$\mathbf{X}\mathbf{H}$
DOTCH	SGTCHS	CF	ERR030	\$\$RAST07	XH
DRAPIO	SSRAST09	ХJА	ERR040	\$\$RAST07	XН
DSKTST	T T	GA		• •	
	SGDSK		ERR050	\$\$RAST07	XH
DTCH	\$\$ANERRB	NN	ERR070	\$\$RAST07	ХJ
DTCRTN	\$\$ANERR7	UE			
DTEXIT	SSANERAJ	UH	ERR080	\$\$ANERRL	PG
DV1017	\$\$ANERAI	UG		• •	
			ERR080	\$\$RAST07	ХJ
DV1018	\$\$ANERAJ	UH	ERR090	\$\$ANERRL	PG
DYNAMIC	\$\$RAST09	XJA	ERR090	\$\$RAST07	ХJ
DYNREALO	\$\$RAST09	XJA	ERR093	\$\$RAST07	ХJ
	771415205		ERRO94	: :	PG
				\$\$ANERRL	
			ERR095	\$\$ANERRF	PE
EDRDHA	SGDSK	GB	ERR095	\$\$ANERRL	PG
EDRDHA1	SGDSK	GB	ERR095	\$\$ANERAP	PN
EDTIC	SGDSK	GB	ERRO95	\$\$ANERAS	PX
				1 1	
EDTIC1	SGDSK	GB	ERR096	\$\$ANERRL	PG
EMGENT	MCRAS	HB	ERR102	\$\$ANERRF	PE
EMGIORTN	\$\$RAST01	VK	ERR105	SSANERRF	PE
EMGWAIT	MCRAS	НС	ERR105	\$\$ANERAS	PX
END	\$\$ANERRO	TF	ERR110	\$\$ANERRD	PA
END	\$\$ANERR1	TG	ERR110	\$\$ANERRF	\mathbf{PE}
ENDPUBS1	\$\$ANERRZ	TC	ERR110	\$\$RAST07	ХJ
ENDPUBS3	\$\$ANERRZ	TD	ERR110	\$\$ANERAS	PX
ENTEXT	FOPT	BG	ERR120	• •	PA
				\$\$ANERRD	
ENTEXT	SGSVC	FL	ERR1 20	\$\$ANERRF	\mathbf{PF}
ENTIO	FOPT	BF	ERR120	\$\$RAST07	ХJ
ENTPCK	FOPT	BA	ERR1 40	\$\$ANERRE	PC
ENTPCK	SGSVC	FJ	ERR145	\$\$RAST07	ХJ
ENTPCK	SGSVC	FK	ERR150	\$\$RAST07	ХJ
ENTSVC	FOPT	BH	ERR150	\$\$ANERAP	PN
EPIBSCAN	\$\$RAST10	XL	ERR1 50	\$\$ANERAQ	PQ
EQPCHK	\$\$ANERRU	sc	ERR152	SSANERAP	PÑ
				• •	
EQPCHK	\$\$ANERRV	SD	ERR153	\$\$RAST07	ХJ
EQPCHK	\$\$ANERAI	UG	ERR155	\$\$ANERAP	PN
EQUCHK	\$\$ANERRX	SK	ERR160	\$\$RAST07	XH
EQPCHK	\$\$ANERSA	UN	ERR170	\$\$RAST07	XН
EOPCHK1	\$\$ANERSA	UN	ERR 17 5	\$\$ANERAP	PN
~					
EQUIP	\$\$ANERRA	NL	ERR180	\$\$ANERAP	PN
EQUIPXIT	\$\$ANERR9	UA	ERR20	\$\$ANERRA	NL
ERPIBCER	MCRAS	HF	ERR 200	\$\$ANERRF	\mathbf{PE}
ERPIBCK	\$\$RAST10	XK	ERR201	\$\$ANERAQ	
					PQ
ERPIBFIL	MCRAS	HF	ERR 205	\$\$ANERAQ	PQ
ERPIBLUP	MCRAS	HG	ERR205	\$\$ANERAL	PU
ERPIBLUP	\$\$RAST00	VD	ERR 208	\$\$ANERRF	PE
ERPIBU	\$\$RAST02	WD	ERR210	\$\$RAST07	хH
ERPMSG	\$\$RAST10	XK	ERR 210	\$\$ANERAQ	PQ
ERPUBUPD	MCRAS	HG			

ERR215	SSANERAO	PQ	ERR658	\$\$ANERRL	PG
ERR220	\$\$ANERRF	PĒ	ERR660	\$\$ANERRF	PE
	• •			• •	
ERR220	\$\$ANERAQ	PQ	ERR660	\$\$ANERAM	PK
ERR240	\$\$ANERAM	PJ	ERR665	\$\$ANERRF	PE
ERR250	\$\$ANERRF	PE	ERR665	\$\$ANERAM	PK
	1 1				
ERR250	\$\$ANERAQ	PQ	ERR695	\$\$ANERAN	PL
ERR251	\$\$ANERAQ	PQ	ERR695	\$\$ANERAQ	PR
ERR252	\$\$ANERAQ	PR	ERR695	\$\$ANERAK	PS
ERR255	\$\$ANERAM	PK	ERR695	\$\$ANERAL	PÜ
ERR255	\$\$ANERAQ	PR	ERR696	\$\$ANERAQ	PR
ERR260	\$\$ANERAQ	PR	ERR696	\$\$ANERAK	PT
ERR265	SSANERRF	PE		• •	
	• •		EDD 700	4433777777	-
ERR265	\$\$ANERAL	PU	ERR 7 00	\$\$ANERRE	PD
ERR270	\$\$ANERAL	PU	ERR700	\$\$ANERRF	\mathbf{PF}
ERR 275	\$\$ANERAM	PJ	ERR700	\$\$ANERRL	PH
	7 7		ERR700	\$\$ANERAM	PK
ERR300	\$\$ANERAK	PS	ERR 7 00	\$\$ANERAN	PM
ERR301	\$\$ANERRE	PC	ERR700	\$\$ANERAP	\mathbf{PP}
ERR305	\$\$ANERAK	PS	ERR700	\$\$ANERAQ	PR
				• •	
ERR309	\$\$ANERAK	PS	ERR700	\$\$ANERAK	PT
ERR310	\$\$ANERAM	PJ	ERR 700	\$\$ANERAR	PW
ERR310	SSANERAK	PS	ERR700	\$\$ANERAS	PX
ERR312	\$\$ANERAK	PS	ERR702	\$\$ANERAR	PW
	· ·				
ERR314	\$\$ANERAK	PS	ERR703	\$\$ANERRE	PD
ERR315	\$\$ANERAM	PJ	ERR703	\$\$ANERAP	PP
ERR318	SSANERAM	Р J	ERR703	SSANERAQ	PR
	• •				
ERR320	\$\$ANERAK	PS	ERR 7 03	\$\$ANERAK	\mathbf{PT}
ERR325	\$\$ANERAK	PS	ERR704	\$\$ANERAR	PW
ERR326	\$\$ANERAK	PS	ERR705	\$\$ANERRL	PH
			ERR705		
ERR335	\$\$ANERRE	PC		\$\$ANERRL	PH
ERR340	\$\$ANERRE	PC	ERR 7 05	\$\$ANERAM	PK
ERR340	\$\$ANERAN	PM	ERR705	\$\$ANERAN	PM
ERR340	\$\$ANERAK	PS	ERR705	\$\$ANERAR	PW
	1 1				
ERR341	\$\$ANERAN	PM	ERR 7 06	\$\$ANERRE	PD
ERR350	\$\$ANERRE	PC	ERR706	\$\$ANERAP	\mathbf{PP}
ERR350	\$\$ANERRL	PG	ERR 7 07	\$\$ANERAN	PM
ERR350	• •	PJ	ERR 71 0		
	\$\$ANERAM			\$\$ANERRE	PD
ERR350	\$\$ANERAN	PM	ERR 71 0	\$\$ANERRF	\mathbf{PF}
ERR350	\$\$ANERAS	PX	ERR 71 0	\$\$ANERRL	PH
ERR351	\$\$ANERAK	PS	ERR710	\$\$ANERAM	PK
				: :	
ERR355	\$\$ANERRL	PG	ERR 71 0	\$\$ANERAQ	PR
ERR355	\$\$ANERAM	PJ	ERR 711	\$\$ANERAP	\mathbf{PP}
ERR355	\$\$ANERAN	PM	ERR 71 3	\$\$ANERAP	PP
ERR360	1 1	PG	ERR715	: :	PF
	\$\$ANERRL			\$\$ANERRF	
ERR390	\$\$ANERAP	PN	ERR 71 5	\$\$ANERAR	PW
ERR395	\$\$ANERRD	PB	ERR720	\$\$ANERRF	PF
ERR396	\$\$ANERRD	PB	ERR720	\$\$ANERRL	PH
ERR400	\$\$ANERAS	PX	ERR720	\$\$ANERAM	PK
ERR401	\$\$ANERAS	PX	ERR 7 20	\$\$ANERAQ	PR
ERR402	\$\$ANERAS	PX	ERR722	SSANERRE	PC .
ERR405	SSANERRD	PA	ERR722	\$\$ANERRL	PG
	: :				
ERR405	\$\$ANERAP	PN	ERR755	\$\$ANERAN	\mathbf{PL}
ERR406	\$\$ANERAN	PL	ERR760	\$\$ANERAQ	PQ
ERR408	\$\$ANERAN	PL	ERR760	\$\$ANERAK	PS
		PX		• •	
ERR410	\$\$ANERAS		ERR760	\$\$ANERAL	PU
ERR412	\$\$ANERRL	PG	ERR805	\$\$ANERAL	PU
ERR412	\$\$ANERAN	PL	ERR820	\$\$ANERAL	PV
ERR600	\$\$ANERRE	PC	ERR825	\$\$ANERAL	PV
ERR600	\$\$ANERAP	PP	ERR840	\$\$ANERAL	PV
ERR605	\$\$ANERAP	PP	ERR842	\$\$ANERAL	PV
ERR610	\$\$ANERAP	PP	ERR870	\$\$ANERAL	PU
				• •	
ERR640	\$\$ANERRF	PF	ESTVOUT	SGTCHS	CG
ERR650	\$\$ANERRE	PC	ESTVOUT1	SGTCHS	CG
ERR650	\$\$ANERRF	PF	EXCPIGN	SGTCHS	CAA
ERR650	\$\$ANERRL	PG	EXCPIGN	SGTCHS	CB
ERR655	\$\$ANERRL	PG	EXCP10	SGTCHS	CA
ERR655	\$\$ANERAN	PL	EXCP2	SGTCHS	CB
ERR658	\$\$ANERRF	PE	EXCP3	SGTCHS	,CC
-		•			• -

EXCP5	SGTCHS	CA	FREDEV	SGTCHS	CP
EXCP5	SGTCHS	СВ	FREDEV1	SGTCHS	CP
EXCP6P	SGTCHS	CAA	FREE	\$\$RAST10	XK
EXCP7	SGTCHS	CA	FSAVALID	\$\$RAST03	WG
EXINTR	\$\$ANERRR	R J	FTCH2	\$\$ANERR6	UC
EXIT	SGTCHS	CG	FTHMSGW	\$\$ANERRU	SC
EXIT	\$\$ANERRC	NM	F01	\$\$ANERRG	QΒ
EXIT	\$\$ANERRS	RK	F010	\$\$ANERRG	QB
EXIT	\$\$ANERRZ	TC	F02	\$\$ANERRG	QB
EXIT	\$\$ANERR1	TG	F03	\$\$ANERRG	QВ
	SANERRI				
EXIT	\$\$ANERR6	UD	F1EUTEST	SGUNCK	DB
EXIT	\$\$RAST02	WD	F2EUTEST	SGUNCK	DB
EXITA	\$\$ANERRA	NLA			
EXITA	SSANERRS	RL			
			CEI NOMI	44D3 0001	****
EXITA	\$\$ANERR7	UE	GELNGTH	\$\$RAST01	VF
EXITAB	\$\$ANERRB	NN	GENENT	FOPT	\mathbf{BF}
EXITB	\$\$ANERRA	NLA	GENENT	FOPT	BF
EXITB	\$\$ANERRS	RL	GEN1	FOPT	\mathbf{BF}
		NN	GEN1	FOPT	BG
EXITBB	\$\$ANERRB				
EXITC	\$\$ANERRA	NLA	GETBND	\$\$RAST03	WH
EXITRTN	\$\$RAST09	XJA	GETCCB	\$\$ANERR7	UE
EXITRTN	\$\$RAST10	XL	GETCHO	SGTCHS	CK
EXITRTN	\$\$RAST00	VC .	GETCMD	\$\$RAST02	WC
EXITRTN	\$\$RAST01	VJ	GETCOM	\$\$RAST02	WD
EXITRTN	\$\$RAST03	WH ·	GETENTRY	SGDFCH	EE
EXITRTN	\$\$RAST11	XN	GETJIB	SGTCHS	CH
EXIT1	SGDFCH	EH	GETMSG	\$\$ANERRV	SE
EXIT1	\$\$ANERRO	TF	GETPIB	SGTCHS	CR
EXIT1	\$\$RAST03	WH	GETPIB1	SGTCHS	CR
EXIT1	\$\$RAST10	XL	GETSEN	SGUNCK	DB
EXIT2	\$\$ANERRO	TF	GIDCK1	\$\$ANERRZ	TD
				• •	
EXPAND	SGDFCH	EE	GIOADR	SGTCHS	CE
EXTEOJ	FOPT	BE	GIOADR	SGTCHS	CF
EXTRAN	SGUNCK	DC	GO	\$\$ANERRJ	QF
EXTRT1	SGSVC	FJ	GO	\$\$ANERRJ	QF
				• •	
EXTRT1	SGSVC	FN	GO	\$\$ANERRP	RE
EXT01	FOPT	BD	GO	\$\$ANERRQ	RG
EXT02	FOPT	BC	GOMCRR	SEND	LA
EXT03	FOPT	BC	GOQUIET	\$\$RAST03	WJ
EXTO4	FOPT	BD	GOTCDMR	\$\$RAST01	VG
EXT1	SGSVC	FL	GOTCLB	SGTCHS	CH
EXT2	SGSVC	FM	GOTREQID	\$\$RAST02	WD
E050	\$\$ANERRI	QE	GTSEN1	SGUNCK	DB
E051	\$\$ANERRI	QE	G01	\$\$ANERRG	QB
			GOT	SAMERING	Δp
E06	\$\$ANERRI	QE			
E062	\$\$ANERRI	QE			
			HALT	SGTCHS	CD
			HANDLECC	\$\$RAST00	VB
FCHRT1	SGDFCH	EA	HANDLEMC	\$\$RAST00	VB
_					
FCHRT2	SGDFCH	EA	HANDLEMC	\$\$RAST03	WE
FCHRT3	SGDFCH	EA	HARDCHAN	SGUNCK	DG
FCHRT4	SGDFCH	EA	HARDWAIT	\$\$RAST00	VB
FCH2260L	\$\$ANERRC	NM	HEADQUE	\$\$ANERAA	NC
	• •				
FCH3	SGSVC	FF	HEADQUE1	\$\$ANERAC	NF
FETCH	\$\$RAST01	VJ	HEADQUE 2	\$\$ANERAF	NH
FETCH	\$\$RAST10	XL	HEADQUE3	\$\$ANERAG	NJ .
FETMSGW	SSANERR9	UB	HOLDQUE	\$\$ANERRY	TA
FGP		EC	HRDWAIT	\$\$RAST00	VA
	SGDFCH				
FILEPR	\$\$ANERRB	NN	H01	\$\$ANERRV	SE
FINDPUBL	\$\$ANERRZ	TC	H01	\$\$ANERRG	QB
FINDTASK	\$\$RAST02	WB	H1RRTN	\$\$RAST03	ÑΕ
FINDTOD	\$\$RAST01	VF		7 7	
FINUP	\$\$ANERR6	UD			
FIODONE	SGDFCH	EH	IDRAEXT	FOPT	BD
FLPTR	SGTCHS	CC	IDRAFCH	SGDFCH	EB
FNDQUE	SGTCHS	CCA	IDRAOK	SGDFCH	EDC
			-		
FNDQUE1	SGTCHS	CD	IDRANOPQ	SGDFCH	EA
FONTERR	\$\$ANERR9	UB	IDRAST1	SGDFCH	EA

IDRAST2	SGDFCH	EF	IREXIT	\$\$ANERRT	SA
IDRAST3	SGDFCH	EF	IREXIT	SSANERRW	SF
IGEXIT	\$\$ANERRS	RK	ISSVC51	SGDFCH	EDB
IGEXIT	\$\$ANERRW	SF	ISSVC51	SGDFCH	EDC
IGEXIT	\$\$ANERRW	SG			
IGNCAN	\$\$ANERRS	RL			
IGON	\$\$ANERRU	SB	JAENTRY	FOPT	BK
	• •	NL	JAISBND	FOPT	BK
IJBERA35	\$\$ANERRA				
IJBERB33	\$\$ANERRB	NN	JAISPP	FOPT	BK
IJBERB35	\$\$ANERAB	RA .	JANOTSUP	FOPT	BK
IJBERC35	\$\$ANERRC	NM	JASETSP	FOPT	BC
IJBERG20	SSANERRG	QA	JAXIT	FOPT	\mathbf{BL}
					BC
IJBERH20	\$\$ANERRH	QD	JAXITBR	FOPT	
IJBERI20	\$\$ANERRI	QE	JIBTYP	SGTCHS	CJ
IJBERJ24	\$\$ANERRJ	QF			
IJBERK20	\$\$ANERRK	QH			
IJBERN33	\$\$ANERRN	RB	KEYINT	\$\$ANERRR	RJ
	• •				
IJBERO35	\$\$ANERRO	RD	KRTY	\$\$ANERRS	RK
IJBERP33	\$\$ANERRP	RE	K01	\$\$ANERRG	QB
IJBERQ33	\$\$ANERRQ	RG			
IJBERR 20	\$\$ANERRR	RJ			
IJBERS34	SSANERRS	RK	LACSW	\$\$ANERRO	RD
	• •				
IJBERT20	\$\$ANERRT	SA	LASPH	\$\$ANERRA	NL
IJBERU33	\$\$ANERRU	SB	LASPHAS	\$\$ANERRC	NM
IJBERV20	\$\$ANERRV	SD	LASTRACK	\$\$RAST01	VH
IJBERX20	\$\$ANERRX	SJ	LASTREC	\$\$RAST01	VH
	\$\$ANERAF			SGDFCH	EC
IJBER535	1 4	NG	LCIDAR		
IJBER635	\$\$ANERAG	NJ	LDPSW	\$\$ANERRR	RJ
IJBER932	\$\$ANERR9	UA	LDRAST00	\$\$RAST01	VJ
IJBMVC33	\$\$ANERR1	TG	LDRAST02	\$\$RAST00	VD
IJBPA134	\$\$ANERRZ	TC	LDRAST02	\$\$RAST01	٧J
				• •	
IJBPA233	\$\$ANERRY	TA	LDREGS	SGTCHS	CK
IJBPA333	\$\$ANERRO	TE	LGD	SGTCHS	CH
INDIB	SGTCHS	CJ	LGDD	SGTCHS	CH
INERRCNT	\$\$ANERAI	UG	LGDD1	SGTCHS	CH
INHWRITE	SGTCHS	CH	LGD1	SGTCHS	CH
INITCHN1	SGTCHS	CP	LMERA	FOPT	BCA
INITRG	SGTCHS	CP	LOADCK	\$\$ANERSA	UN
INITSIO	SGTCHS	CN	LOADMOD	\$\$RAST00	VC
INRO	\$\$ANERRW	SG	LOADMOD	\$\$RAST01	VJ
INSERT	\$\$ANERRB	NN	LOADMOD	\$\$RAST03	WH
INST	SEND	LD	LOADPSW	\$\$ANERRR	RJ
INTERRCC	SGTHAP	MK	LOADTEST	\$\$RAST00	VC
INTERV	\$\$ANERR9	UA	LOADTEST	\$\$RAST01	VJ
INTPUBSC	SGTCHS	CK .	LOADTEST	\$\$RAST03	WH
INTREQ	\$\$ANERRU	SC	LOAD00	\$\$RAST00	VA
	i i			i i	
INTREQ	ŞŞANERRV	SD	LOAD01	\$\$RAST01	VF.
INTREQ	\$\$ANERSA	UK	LOAD03	\$\$RAST03	WE
INTREQD	\$\$ANERAI	UG	LOAD09	\$\$RAST09	XJA
INTRTN	SGTCHS	CK	LOGBAD	\$\$RAST10	XK
INTVEN	\$\$ANERRA	NLA	LOGENT	SSANERRP	RE
	: :			1 1	
INVAL	\$\$ANERRY	TB	LOGENT	\$\$ANERRQ	RG
INVALID	\$\$RAST10	XM	LOGERP	\$\$ANERRU	SC
IOCOMP	\$\$ANERRQ	RH	LOGLOOP	\$\$RAST09	XJA
IODONE	\$\$ANERRP	RF	LOGLOOP	\$\$RAST11	XN
IOERR	\$\$ANERRH	QD	LOGPRC	SGTCHS	CFA
	• •				
IOERR	\$\$ANERRI	QE	LOGPRC1	SGTCHS	CG
IOERR	\$\$ANERRJ	QG	LOGPRC2	SGTCHS	CG
IOERR	\$\$ANERRP	RF	LOGRTN	\$\$ANERRY	TA
IOINTR	\$\$ANERRR	RJ	LOGTST	\$\$ANERRU	sc
	• •			* *	TA
IONOP	SGUNCK	DA	LOGIST	\$\$ANERRY	
IOPSET	SGSVC	FF	LOGWAIT	\$\$ANERRY	TA
IORTN	\$\$ANERRI	QE	LOG1	\$\$ANERRY	TA
IORTN	\$\$ANERRJ	QG	LOG2	\$\$ANERRY	TA
IOWAIT	\$\$ANERSB	UP	LOOKUP	SGDFCH	ED
IOWAIT	\$\$ANERSC	UR	LOOP1	\$\$ANERAE	RC
IPLEXIT	\$\$RAST00	VC	LOWBITON	\$\$RAST11	XN

LSTDIB	SGTCHS	CJ	MCRSENDD	SGUNCK	DG
LTA		LH			
	SEND		MCRSPSW2	SMCRR	KH
LTABSY	SGSVC	FD	MCRSUPIK	SMCRR	ĸJ
LTACCB	\$\$ANERRM	NB	MCRSUPSW	SMCRR	KE
LTACNL	FOPT	BB	MCSCHDL	MCRAS	HA
LTARTRN	FOPT	BE	MCSELECT	SMCRR	\mathbf{KF}
LTKHLD	\$\$ANERRZ	TD	MCSOFT	MCRAS	HA
L01	\$\$ANERRG	QC	MCTASK	MCRAS	HA
L01	\$\$ANERRI	QE	MESG	\$\$ANERRB	NN
			MESSWTR	\$\$RAST11	XN
			MODCCW	\$\$ANERRX	SK
MACHER	SGUNCK	DG			
MACHEK			MODESTAT	\$\$RAST03	WJ
MACHEK	SGUNCK	DG	MODIFY	SEND	LF
MACHEK	SGUNCK	DG	MOVELIST	\$\$ANERAD	NK
MACHEK1	SGUNCK	DG	MOVENAME	\$\$ANERRM	NB
MAINRT	\$\$ANERR6	UC	MOVIDRA	SGDFCH	EDC
MAINTASK	\$\$ANERR1	TG	MOVNAM	\$\$ANERRM	NA
MAINTR	\$\$ANERR7	UE	MOVRIK	SGDFCH	EDB
MAINTR	\$\$ANERR8	UF	MOVRIK	SGDFCH	EDC
MCCPUEX1	SMCRR	KG	MPSTASK	\$\$RAST01	VG
MCMVLGOT	SMCRR	KE	MPSTST	\$\$ANERRN	RB
MCNOTSP	SMCRR	KC	MPSTST	SSANERRO	RG
				~	
MCPDCOND	MCRAS	HA	MPSYES	SGTCHS	CN
MCRBUMP	SMCRR	KE	MSGNTR	\$\$ANERRW	SF
MCRCHDMG	SMCRR	KA	MSGWTR	\$\$ANERRT	SA
MCRCHMVN	SMCRR	KD	MSGWTR	\$\$ANERRV	SE
MCRCHNBC	SMCRR	KD	MSGWTR	\$\$ANERRW	SG
MCRCHNDM	\$\$A\$SUP1	KB	MSGWTR	\$\$ANERRW	SH
	• • •	KE		\$\$ANERR7	UE
MCRCNCOD	SMCRR		MSGWTR		
MCRCPUEX	SMCRR	KG	MSGWTR	\$\$ANERRG	QΑ
MCRDVDMG	SMCRR	KD	MSGWTR	\$\$ANERRH	QD
MCREND01	SMCRR	KD	MSGWTR	\$\$ANERRI	QΕ
				• •	
MCREND02	SMCRR	KE	MSGWTR	\$\$ANERRJ	\mathbf{QF}
MCREND03	SMCRR	KG	MSGWTR	\$\$ANERRK	QH
MCREND04	SMCRR	KH	MSG2	\$\$ANERAB	RA
MCRENTER	SGUNCK	DG	MSG3	\$\$ANERAB	RA
				1 1	
MCRETURN	SMCRR	KC	MSG4	\$\$ANERAB	RA
MCRFULL	SMCRR	KF	MVC	\$\$ANERR1	TG
MCRGTFDV	\$\$A\$SUP1	KB	MVCCW	SGTCHS	CD
		KD			
MCRGTLST	SMCRR		MVEPSW	SGUNCK	\mathbf{DF}
MCRGTPIB	SMCRR	KE	MVMSG	\$\$ANERRV	SD
MCRLOOP1	SMCRR	KA	MVZEX	SGUNCK	DB
MCRLOOP2	\$\$A\$SUP1	KB	M01	\$\$ANERRG	QC
				• •	
MCRLOOP3	SMCRR	KG	M01	\$\$ANERRI	QΕ
MCRMPX	SMCRR	KA	M01	\$\$ANERRK	QH
MCRMPXST	\$\$A\$SUP1	KB .			
MCRNEQLD	SMCRR	KF			
MCRNLTA	SMCRR	KG	NDEQUE	\$\$ANERRC	NM
MCRNODMG	SMCRR	KD	NEXTCYL	\$\$RAST01	VH
MCRNTBSY	SMCRR	KC .	NEXTPH	SSANERAE	RC
				• •	
MCRNTCIB	SMCRR	KF	NGTMBP	SGSVC	FG
MCRNTLTA	SMCRR	KG	NOAP	\$\$ANERR Z	$\mathbf{T}\mathbf{D}$
MCRNTSUP	SMCRR	KE	NOAP1	\$\$ANERRZ	TC
MCROBRRT	SMCRR	KJ	NOCANCEL	\$\$RAST02	WB
				• •	
MCRPARIT	SGUNCK	DG	NOCB	SGTCHS	CN
MCRRBST	SMCRR	KG	NOCCB	\$\$ANERRX	SK
MCRRCHER	SMCRR	KA	NOCCB	\$\$RAST02	WC
MCRRCPU	SMCRR	KG	NOCCB	\$\$ANERRO	RD
MCRRDIAG	\$\$A\$SUP1	KB	NOCCB1	SGUNCK	DA
MCRRRTN	SMCRR	KA	NODEQUE	\$\$ANERRC	NM
MCRRTSTQ	\$\$A\$SUP1	KB	NODEQUE	\$\$ANERAB	RA
	• • •				
MCRSAFTR	SMCRR	KG	NOEMP	\$\$ANERR9	UB
MCRSCNCH	SMCRR	KA	NOLOADAD	SGDFCH	$\mathbf{E}\mathbf{E}$
MCRSCPHM	SMCRR	KH	NOLOG	\$\$ANERAE	RC.
			NOLOG	\$\$ANERRP	RF
Manager 4	AAR AGEEDA	WD.		• •	
MCRSEL1	\$\$A\$SUP1	KB	NOLOG	\$\$ANERRQ	RH
MCRSEL2	\$\$A\$SUP1	KB	NOLSS	\$\$ANERR9	UB
				•	

NOLTA	\$\$ANERAE	RC	OURSIO	SGUNCK	\mathbf{DF}
	• •				
NOLTH	\$\$ANERRM	NB	OVERRUN	\$\$ANERR9	UB
NOMSG	\$\$RAST10	XL	OVERUN	\$\$ANERRB	NN
NONREC	\$\$ANERR9	AU	OVRUN	\$\$ANERRV	SE
			OVION	\$\$MINDINI V	ОH
NOPBR	\$\$ANERRQ	RG			
NOPINS	SGTCHS	CH			
NOPINSTR	SGTCHS	СН			
			Danmar	44D3.0000	37.75
NOPRNAME	\$\$RAST01	VG	PARTNOK	\$\$RAST09	XJB
NOPUBRS	SSANERAA	NC	PAR40	\$\$ANERRO	TE
NORELOC	SGUNCK	DAA	PAR41	\$\$ANERRO	TE
				· ·	
NOQUIS	SGUNCK	DH	PAR42	\$\$ANERRO	TE
			PAR43	\$\$ANERRO	TE
NORCD	SGDSK	GA	PAR44	\$\$ANERRO	TE
NORCFND	\$\$ANERRA	NL	PAR45	\$\$ANERRO	TE
NOSO	SGTCHS	CCA	PAT	\$\$ANERRC	NM
NOSTART	SGUNCK	DA	PCHDIB	SGTCHS	CJ
NOSTATUS	\$\$ANERRV	SE	PCHKSW	FOPT	BA
NOSWP	SGSVC	FG	PCHKSW	SGSVC	FJ
NOS01	SGTCHS	CM			FK
			PCHKSW	SGSVC	
NOTBONLY	SGDFCH	EG	PCIL1	SGDFCH	$\mathbf{E}\mathbf{B}$
NOTBSY	SGTCHS	CL	PCIL2	SGDFCH	EB
NOTCLB		CH		SGSVC	
	SGTCHS		PCITRT		FM
NOTDMC1	\$\$RAST02	WC	PCURTN	\$\$ANERRW	SF
NOTFCH	SGSVC	FE	PDABEX	SMICR	JН
NOTFIRST	\$\$RAST03	WJ	PDAGN	SMICR	JF
NOTFOUND	SGDFCH	ED	PDAID	SGDFCH	EE
NOTFULL	\$\$RAST01	VJ	PDBOCK	SMICR	JF
	• •				
NOTIC	SGTCHS	CH	${ t PDBUFL}$	SMICR	JВ
NOTIC	\$\$ANERR6	UD	PDCCBPT	SGSVC	FB
NOTMPS	SSRAST11	XN	PDCCBT	SGSVC	FB
	• •				
NOTPD	FOPT	BH	PDCHAN	SMICR	JΕ
NOTPD1	FOPT	BH	PDCHAN	SMICR	JF
NOTRIA	SGTCHS	CK	PDCOMP	SMICR	JE
NOT2314	SEND	LE	PDCSWST	SMICR	JD
NRFRTY	\$\$ANERRJ	QF	PDCSWST	SMICR	JF
NRTASTO	SGTCHS	ĈE	PDDEQUE	SMICR	JG
NTFTCH	SGUNCK	DC	PDDEQUE1	SMICR	JG
NXTERPIB	\$\$RAST10	XK	PDDEQUE2	SMICR	JG
NXT1	SGTCHS	CG			
			PDDFLT	SMICR	JF
N01	\$\$ANERRG	QC	t PDEDLT	SGSVC	$\mathbf{F}\mathbf{B}$
N01	\$\$ANERRJ	QF	PDERXT1	SMICR	JΕ
N1114	SGTCHS		PDERXT1	SMICR	JF
NTTT4	SGICES	CQ			
		•	PDERXT2	SMICR	JΕ
	*		PDERXT2	SMICR	JF
OBRAREL	\$\$ANERAA	NC			JF
	· •		PDERXT3	SMICR	
OBRBYPS	\$\$ANERRM	NA	PDETIO	SMICR	JD
OBREXIT	\$\$ANERAA	ND	PDET IO	SMICR	JF
OBRICE	SSANERAA	NC			JН
			PDEXT1	SMICR	
OBRIOE1	\$\$ANERAA	ND	PDFSTM	SMICR	JВ
OBRIO2	\$\$ANERAA	NC .	PDHERE	SMICR	JC
OBRIO3	• •	NC			
	\$\$ANERAA		PDIAGN	SMICR	JB
OBRNOCCB	\$\$ANERRM	NB	PDIAGN1	SMICR	JC
OBRNOKEY	\$\$ANERRM	NB	PDINTR	SMICR	JA
OBRREL					
	\$\$ANERAA	ND	PDKEY	SMICR	JH
OBRREL1	\$\$ANERAA	ND	PDMOV	SMICR	JE
OBRSPR	\$\$ANERRM	NA	PDMPI	SMICR	JA
OBRSPR1	· •				
	\$\$ANERRM	NA	PDMVCSW	SMICR	JE
OFFLINE	SGTCHS	CR			
OK .	\$\$ANERR1	TG	PDNF	SMICR	JB
	• •				
ONERET	\$\$ANERRG	QA	PDNOB	SMICR	JC
ONERTRY	\$\$ANERR9	UA	PDNONOP	SMICR	JΒ
OPCLOSE	SGDFCH	EC	PDNOPCK	FOPT	BA
OPFLAG	\$\$ANERRN	RB	PDNOPCK	SGSVC	FJ
OPTRT1	SGSVC	FM	PDNOPCK	SGSVC	FK
OPTRT2	SGSVC	FM	PDNOSS	SMICR	JB
OPVNT	\$\$ANERRW	SG	PDNOTSS	SMICR	JG
ORERP	\$\$ANERRA	NL	PDNOTZR	SMICR	JC
OR1287	SSANERR9	UA	PDPDEQ	SMICR	JE
	T T		 .		

PDPRCAN	SMICR	JG	PUBSCN3	\$\$ANERRZ	TD
PDPROGCK	SMICR	JG	PURGE	SGTCHS	CM
PDREJDC	SMICR	JF	PUTUTR	\$\$ANERRU	SC
		JC	FOIGIK	\$\$MININO	50
PDREJT	SMICR				
PDSCAW	SMICR	JB			
PDSERR	SMICR	JD	QIDCK1	\$\$ANERRZ	$\mathbf{T}\mathbf{D}$
PDSERR1	SMICR	JD	QISRT1	SGUNCK	DH
PDSERR1	SMICR	JF	QISRT2	SGUNCK	DH
PDSERR2	SMICR	JD	QISRT3	SGUNCK	DH
PDSERR3	SMICR	JD	QUETEST	SSANERRP	RE
PDSIO	SMICR	JC	QUETEST	\$\$ANERRQ	RG
PDSNO1	SMICR	JE	QUEUP	SGTCHS	CC
PDSNO2	SMICR	JD	QUIET145	\$\$RAST03	WJ
PDSPK	SMICR	JВ	QUISIO	SGUNCK	DH
PDSS	SMICR	JC	Q01	\$\$ANERRG	QC
PDSUPEXT	SMICR	JH			
PDSUPV	FOPT	BG			
PDSUPV	SGSVC	FL	RADLDS	SGTCHS	CA
PDSVC28	SMICR	JC	RASDEO	MCRAS	HG
PDSWBP	SMICR	JH	RASIO	\$\$RAST01	VH
PDSWZ	SMICR	JH	RASIO	SSRAST10	XM
PDTASK	SMICR	JH	RASIO	\$\$RAST11	XN
				• •	
PDTERR1	SMICR	JE	RASIOE	MCRAS	HC
PDTERR1	SMICR	JF	RASMEXT	MCRAS	HB
PDTERR2	SMICR	JE	RASQOK	MCRAS	HC .
PDTERR5	SMICR	JE	RAST02	\$\$RAST00	VD
PDTIMER	SMICR	JH	RBBY12	SEND	LA
PDTIO	SMICR	JA	RCHAN	\$\$ANERR6	UD
PDTIOERR	SMICR	JE	RCHAN	\$\$ANERAJ	υJ
PDTIOERR	SMICR	JF	RCHS	\$\$ANERAJ	UJ
		JB			
PDTIOK	SMICR		RCOMMONA	\$\$RAST05	XG
PDTKY	FOPT	BG	RCOMMONB	\$\$RAST04	ХD
PDTKY	SGSVC	FL	RCOMMONB	\$\$RAST05	ΧG
PDUPDT	SMICR	JВ	RCVERR	SGUNCK	DC
PDYES	SMICR	JЕ	RDDIR2	SGDFCH	ED
PHASE	SGDFCH	EC	RDHA9	SGDSK	GA
PHASEH	\$\$ANERRG	QC	RDRCD	\$\$ANERRH	QD
PHASEJ	SSANERRG	QA	RDTXT	SGDFCH	ĒE
PHASES	\$\$ANERRP	RF	RDVER	\$\$ANERRK	QH
PHASES	• •	RH	RDYCANDP	SGTHAP	MK
	\$\$ANERRQ				
PHASES	\$\$ANERRR	RJ	RDYCNL	SGTHAP	MM
PHASE1	\$\$ANERRG	QB	RDYCN1	SGTHAP	MM
PHASE2A	\$\$ANERAE	RC	RDYCN2	SGTHAP	MM
PHASR	\$\$ANERRQ	RH	RDYCN2A	SGTHAP	MM
PICKDIR	SGDFCH	EC	RDYCN4	SGTHAP	MM
POSCHK	\$\$ANERSC	UQ	RDYCN4X	SGTHAP	MM
POSCHK3	\$\$ANERSC	ŪQ	RDYCN4Z	SGTHAP	MM
POSCHK4	SSANERSC	UR	RDYDUMP	SGTHAP	MK
POSTCAN	\$\$ANERRY	TB	READUPDT	SGDFCH	EG
POSTCE	SGTCHS	CP	RECAL	SGDSK	GA
		WB		SSRAST01	VF
POSTPIB	\$\$RAST02		RECFULL		
PREFERED	SGDFCH	EC	RECSBLT	\$\$RAST01	VJ
PREPSBR	\$\$ANERSC	ŪQ	RECVERR	\$\$ANERR8	UF
PROC	\$\$ANERRT	SA	REFAIL	\$\$ANERR8	UF
PROTCHK	\$\$ANERRA	NL	REGZERO	\$\$RAST11	XN
PROTECT	SGTCHS	CH	RELOC	\$\$ANERRP	RE
PRTPRG	SGUNCK	DB	RELOCATE	\$\$RAST10	\mathbf{XL}
PRTPRG1	SGUNCK	DA	REPERR	\$\$ANERRQ	RH
PSTBUF	\$\$ANERRW	SG	REQUEST	\$\$RAST10	XM
PSTEOF	SGTCHS		RERASIO	MCRAS	HC
		CQ			
PSTERR	\$\$ANERRT	SA	RESCHK	SGUNCK	DB
PSTERR	\$\$ANERRW	SF	RESERR	SGDSK	GA
PTERP	\$\$ANERRA	NL	RESET	\$\$ANERAE	RC
PTOSW	\$\$ANERRL '	PG	RESPNS	\$\$ANERRR	RJ
PTRXCH	\$\$ANERRO	TF	RESPTYP	\$\$RAST10	ХL
PUBDEQ	SGSVC	FF	RESTART	\$\$RAST00	VC
PUBSCAN	\$\$RAST00	VE	RESTCOP	\$\$ANERSC	UR
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RESTORE	\$\$RAST03	WG	SDRACC5	\$\$ANERAC	NE
RESTUSE	\$\$ANERSB	UP	SDRAREL	\$\$ANERAC	NE
RESVC	SGSVC	FC	SDRAW1	SSANERAC	NE
	SGSVC	FE			
RESVC1	SGSVC	rŁ	SDRAW2	\$\$ANERAC	NE
			SDRERAC	\$\$ANERAC	NE
RETOFF	\$\$ANERR6	UD	SDREXIT	\$\$ANERAC	NF
RETOFF	\$\$ANERR7	UE	SDRIO	\$\$ANERAF	NH
RETRY	\$\$ANERRV	SE	SDRIOE	\$\$ANERAC	NF
	: :				
RETRY	\$\$ANERRX	SK	SDRIOX	\$\$ANERAF	NH
RETRY	\$\$ANERR9	UB	SDRIOX1	\$\$ANERAG	ŊJ
RETRY	\$\$ANERR6	UC	SDRIO2	\$\$ANERAC	NF
RETRY	\$\$ANERRR	R J	SDRMM	SEND	LA
RETURN	\$\$RAST01	VH	SDRM00	\$\$ANERAG	ŊJ
RETURN	\$\$RAST03	WH	SDRM012	\$\$ANERAF	NG
RETXIT	\$\$ANERRX	SK	SDRM02	\$\$ANERAF	NG
RINGBELL	\$\$RAST00	VA	SDRM03	\$\$ANERAF	NG
RINGTIO	\$\$RAST00	VA	SDRNMCRR	SEND	LG
RLOG	\$\$RAST04	XA	SDRNO	SEND	LB
RMESSAGE	\$\$RAST00	VA			NE
	• •		SDRNOAD	\$\$ANERAC	
RPRNTR	\$\$RAST04	XC	SDROBR	SEND	\mathbf{LF}
RSETWAIT	SGTCHS	CM	SDROBRO	SEND	\mathbf{LF}
RSTCHPT	\$\$ANERRY	TA	SDROBRW	SEND	LF
RSTCHO	SSANERRY	TA	SDRQUIS	SGUNCK	DH
-	• •			SGUNCK	
RSTFLG	\$\$ANERRU	SC	SDRQUIS1		DH
RSTFLG	\$\$ANERRI	QE	SDRREL	\$\$ANERAC	NF
RSTFLG	\$\$ANERRJ	QG	SDRREL1	\$\$ANERAC	NF
RSTFLG	SSANERRP	RF	SDRSDR	SEND	LF
RSTFLG	SSANERRO	RG	SDRSDR1	SEND	LF
RSTPUB	SGDFCH	EH	SDRSDR2	SEND	LG
RSTPUB1	SGDFCH	EH	SDRSDR2X	SEND	$\mathbf{L}\mathbf{G}$
RSTQPT	\$\$ANERRU	SC	SDRSKIP	\$\$ANERAF	NG
RSTQPT	SSANERRH	QD ·	SDRSVC3	SEND	LA
RSTOPT	\$\$ANERRI	QE	SDRXIO	SEND	LB
	• •		SDRXIO1		
RSTQPT	\$\$ANERRJ	QG		SEND	LB
RSTQPT	\$\$ANERRP	RF	SDRXIO2	SEND	$\mathbf{L}\mathbf{B}$
RSTQPT	\$\$ANERRQ	RG	SDRXIO3	SEND	$_{ m LB}$
RSTREG	SGUNCK	DE	SDRYES	SEND	$\mathbf{L}\mathbf{D}$
RTARET	MCRAS	НВ	SDR1	SEND	LE
RTARET1	MCRAS	HB	SDR1A	SEND	LE
RTNTEST	\$\$RAST00	VA	SDR1B	SEND	LE
RTY	\$\$ANERRV	SD	SDR1B1	SEND	LE
RTYCT	\$\$ANERRV	SE	SDR1B2	SEND	LE
RTYONE	\$\$ANERRU	sc	SDR1B3	SEND	LE
RTYRTN	SSANERRP	RF	SDR1B4	SEND	LE
R01	\$\$ANERRG	QA	SDR1B5	SEND	LE
R01	\$\$ANERRI	QE	SDR1RES	SEND	$\mathbf{L}\mathbf{E}$
R01	\$\$ANERRJ	QF	SDR1RESX	SGUNCK	DE
R1442	\$\$RAST04	XC	SDR1RES1	SEND	$\mathbf{L}\mathbf{E}$
R1442A	SSRAST04	XC	SDR 2A3	SEND	LC
R1442B	• •	XC			LC
	\$\$RAST04		SDR2A4	SEND	
R2501	\$\$RAST04	XB	SDR2A5	SEND	LC
R2501A	\$\$RAST04	XB	SDR2QT	SEND	LB
R2501B	\$\$RAST04	XB	SDR 2QT1	SEND	LB
R2520	SSRAST05	XE	SDR2QT2	SEND	LB
R2520B	\$\$RAST05	XE	SDR23		LD
			SDR23	SEND	מת
R2540	\$\$RAST04	XB			
			SECTION1	\$\$ANERRZ	TC
			SECTION3	\$\$ANERRZ	$\mathbf{T}\mathbf{D}$
SAVEIO	\$\$RAST00	VE	SEEKTEST	SGTCHS	CH
SCANTAB	\$\$RAST02	WC	SEKCH	\$\$ANERRA	NL
SCHREC2	\$\$RAST02	WD	SEKCHK	SGDSK	GA
SCIL1	SGDFCH	EB	SEKCHK1	SGDSK	GA
SCIL2	SGDFCH	EB	SELBMX	SGTCHS	CN
SCURTN	\$\$ANERRW	SG	SELBMX	SGTCHS	CN
SDM01	\$\$ANERAF	NG	SELECT	SGTCHS	CN
SDRACC1	\$\$ANERAC	NE	SELERR	\$\$ANERRV	SD
SDRACC2	\$\$ANERAC	NE	SENSTSTS	\$\$ANERR9	UA
SDRACC3	\$\$ANERAC	NE			

SETARON	\$\$ANERRY	TB	SVC05	SGSVC	FB
SETCNCL	SSANERRO	TF	SVC06	SGTHAP	MM
		RG	SVC07		
SETCNCL	\$\$ANERRQ			SGSVC	FE
SETDIS	\$\$ANERRS	RL	SVC08	SGSVC	FG
SETEBL	\$\$ANERR8	UF	SVC10.	SGSVC	FG
SETFCPU	MCRAS	HA	SVC10A	SGSVC	FG
SETFLE	\$\$ANERRX	SJ	SVC11	SGSVC	FE
SETKEY	\$\$RAST03	WH	SVC11A	SGSVC	\mathbf{FE}
SETLNK	\$\$ANERAA	NC	SVC11A	SGSVC	FE
SETLT1	SGSVC	FD	SVC11B	SGS V C	FD
SETLT2	SGSVC	FD	SVC11C	SGSVC	FD
SETLT2A	SGSVC	FD	SVC12A	SGSVC	
					FA
SETOP1	SGSVC	FJ	SVC13A	SGSVC	FA
SETOP1	SGSVC	FN	SVC15	SGTCHS	CA
SETOP2	SGSVC	FJ	SVC15	SGTCHS	CB
SETOP2	SGSVC	FN	SVC18	SGSVC	FN
	\$\$ANERRZ	TD	SVC19	SGSVC	
SETPOSTL					FN
SETPSN	\$\$ANERR7	UE	SVC2BND	SGSVC	FC
SETRD	\$\$ANERR8	UF	SVC22	SGSVC	\mathbf{FH}
SETRTRY	\$\$ANERRQ	RH	SVC22A	SGSVC	FH
SETSK	SGDFCH	EC	SVC23	SGSVC	FH
SETSKAD	SGDFCH	EC	SVC24	SGSVC	FH
SETSVAR	SGDFCH	EF	SVC27	SGTCHS	CB
SETUP	\$\$RAST00	VC .	SVC29	SGSVC	$\mathbf{F}\mathbf{B}$
SIO	SGTCHS	CFA	SVC3	\$\$ANERRA	NL
SKCHK	\$\$ANERRA	NL	SVC35	SGTHAP	
	• •				MΑ
SKSLI	\$\$ANERRB	NN	SVC35A	SGTHAP	MΑ
SPFKREP	\$\$RAST03	WH	SVC36	SGTHAP	MB
SSCOM	SSANERRW	SG	SVC37A	SGTHAP	MC
STDEXT	SGUNCK	DC	SVC38	SGTHAP	MD
STEPLOOP	\$\$ANERRZ	TD	SVC38A	SGTHAP	MD
STGERR	\$\$RAST03	WG	SVC38B	SGTHAP	MD
STGEXIT	\$\$RAST03	WH	SVC38B	SGTHAP	MD
STMODE	SGTCHS	CG	SVC38C	SGTHAP	MD
STMODE1	SGTCHS	CG	SVC38C	SGTHAP	
					MD
STMODE2	SGTCHS	CG	SVC38D	SGTHAP	MD
STORE	SGTCHS	СН	SVC38E	SGTHAP	MD
STORKE	\$\$ANERAE	RC	SVC39	SGTHAP	ME
			SVC39A	SGTHAP	ME
CMDMED	COMOTIC	O.F.			
STRTED	SGTCHS	CE	SVC39B	SGTHAP	ME
STRTED	SGTCHS	CFA	svc39c	SGTHAP	ME
STRTIO	SGTCHS	CE	SVC39D	SGTHAP	ME
STRTIO	SGTCHS	CFA	SVC39E	SGTHAP	MF
STRTIO1	SGTCHS	CE	SVC39E1	SGTHAP	MF
STRTIO1	SGTCHS	CFA	SVC39F	SGTHAP	MF
STRTI2	SGTCHS	CFA	SVC39G	SGTHAP	ME
SUPEXP	SGTCHS	CA	SVC39H	SGTHAP	MD
SUPEXP	SGTCHS	СВ	SVC39H	SGTHAP	ME
SUPEXT	FOPT	BD	SVC39H1	SGTHAP	ME
SUPIB	SGTCHS	CR	SVC39J	SGTHAP	MF
svc 37	SGTHAP	MC	SVC39K	SGTHAP	MF
SVCALL	\$\$ANERAE	RC	SVC39L	SGTHAP	MF
SVCA6	SGSVC	FR	SVC39M	SGTHAP	ME
		BH	SVC39P		
SVCRTN1	FOPT			SGTHAP	ME
SVCWAIT	\$\$ANERRY	TA	SVC39P1	SGTHAP	ME
SVCWAIT	\$\$ANERRP	RF	SVC39Q	SGTHAP	MF
SVCWAIT	SSANERRO	RG ·	SVC40	SGTHAP	MG
SVCWAIT1	\$\$ANERRO	TE	SVC40A	SGTHAP	MG
	• •				
SVC00	SGTCHS	CA	SVC40B	SGTHAP	MG
SVC00	SGTCHS	CB	SVC40C	SGTHAP	MG
SVC01A	SGSVC	FA	SVC40D	SGTHAP	MG
SVC02	SGSVC	FC	SVC40E	SGTHAP	MG
SVC02A		FC	SVC40L		
	SGSVC			SGTHAP	MH
SVC02J	SGSVC	FC	SVC41A	SGTHAP	MH
SVC03	SGSVC	FF	SVC41A1	SGTHAP	MH
SVC03	SGSVC	FF	SVC41A2	SGTHAP	ΜH
SVC04	SGSVC	FF	SVC41B	SGTHAP	MH
			- · · · ·		

SVC41C	SGTHAP	MH	TPIGNOR	\$\$ANERRC	NM
SVC42	SGTHAP	MG	TPRETRN	SEND	LA
		MG	TPSDR1	SEND	LA
SVC42A	SGTHAP				
SVC42B	SGTHAP	MG	TRKCHK	SGDSK	GB
SVC43	SGSVC	FR	TRKEOC	SGDSK	GB
SVC45	SGSVC	$\mathbf{F}\mathbf{R}$	TRNOFF	SGTCHS	\mathbf{CL}
SVC51	SGSVC	FS	TRYNXT	SGTCHS	CH
			TSTATD	\$\$ANERRR	RJ
SVEREG	FOPT	BAA	TSTATTN	SGTCHS	CL
SVEREG	SGTCON	GC	TSTBMX	SGTCHS	
					CQ
SVNWAD	SGTCHS	CD	TSTCAN	\$\$ANERRR	RJ
SWITCH	\$\$ANERRO	RD	TSTCCB	\$\$ANERRN	RB
SXPC1	SGSVC	FN	TSTCCC	\$\$ANERRU	SB
SXPC2	SGSVC	FN	TSTCDC	\$\$ANERRU	SB
SXTRT1	SGSVC	FJ	TSTDEV	SGTCHS	CCA
SXTRT1	SGSVC	FN	TSTEOJ	SGTCHS	CE
		RD		7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	UC
SYCLAS	\$\$ANERRO		TSTEQCK	\$\$ANERR6	
SYSFILE	SGTCHS	СJ	TSTERF	SGTCHS	CL
SYSFILE1	SGTCHS	СJ	TSTNXT	SGTCHS	CJ
SYSFILE2	SGTCHS	CJ	TSTPSN	\$\$ANERR7	UE
SYSFILE3	SGTCHS	CQ	TSTQEF	SGTCHS	CP
SYSFILE4	SGTCHS	СĴ	TSTRESIO	SGTCHS	CN
SYSFILE5	SGTCHS	CE	TSTRTY	\$\$ANERRN	RB
SYSINOUT	SGTCHS	CE	TSTSNS	\$\$ANERAI	ÜG
SYSSIN	SGTCHS	CJ	TSTSSL	\$\$ANERRB	NN
S01	\$\$ANERRJ	QF	TSTSVC	SGDFCH	EDA
			TSTTRG	\$\$ANERRS	RK
			TSTUCK	SGTCHS	CKA
TAPMODE2	\$\$ANERR9	UB ·	TST03U	\$\$ANERRU	SB
TCAN2	SSANERRY	TB	TST2311	\$\$ANERAA	NC
TCAN2A	\$\$ANERRY	TB	T01	1 1	QB
	• •			\$\$ANERRG	-
TEST	\$\$ANERRH	QD	T03	\$\$ANERRH	QD
TESTBUSY	\$\$ANERRP	RE	T06	\$\$ANERRH	QD
TESTDMC	\$\$RAST02	WA	T145RTN	\$\$RAST03	WF
TESTEOJ	SGTCHS	CF	T155RTN	\$\$RAST03	WE
TESTER	\$\$ANERAD	NK			
TESTFE	\$\$RAST02	WD			
TESTIGN	\$\$ANERRQ	RG	UCBPAR	\$\$ANERRV	SD
TESTLTA	FOPT	BE	UCSTST	\$\$ANERRV	SE
TESTEIR	\$\$ANERR1	TG	UNBUSY	\$\$RAST02	WA
	• •			• •	CE
TESTSVC	SGDFCH	EDA	UNCOMMON	SGTCHS	
THCHK	SGTHAP	MC	UNDETERR	\$\$ANERAI	UG
THDLT1	SGTHAP	MB	UNDETR	\$\$ANERR6	UC
THDLT 2	SGTHAP	MB	UNDETR	\$\$ANERR7	UE
THDLT 2	SGTHAP	MB	UNDTR	\$\$ANERRT	SA
THFREE	SGTHAP	MB	UNDTR	SSANERRW	SF
THFREE1	SGTHAP	MB	UNKN	\$\$ANERRB	NN
THRETRY	SGTHAP	MC	UNPACK	\$\$RAST11	XN
			UNPCH		
THSETUP	SGTHAP	MA		\$\$ANERRO	RD
THWAIT1	SGTHAP	MA	UNPKSEN	\$\$ANERRO	RD
THWAIT2	SGTHAP	MA	UNRCERP	\$\$ANERRA	NL
TKDLET	SGTHAP	MB	UNSUPTD	\$\$ANERR9	UB
TKHDADD	SGTHAP	MA	UNTCK1	SGUNCK	DA
TKHDQUE	SGTHAP	MA	UNTCK2	SGUNCK	DA
TKHDRTN	SGTHAP	MA	UNUSENS	\$\$ANERRU	SC
TKHD1	SGTHAP	MA	TIAWUU	SGTHAP	MJ
TKHELD	SGTHAP	MA	UNW001	SGTHAP	MJ
TKPRTY	SGTHAP	MJ	UNW002	SGTHAP	МJ
TKPRT1	SGTHAP	MJ	UNW003	SGTHAP	MJ
TMEKEY	SGSVC	FG	UNW004	SGTHAP	MJ
TMERT1	SGSVC	FL	UNW005	SGTHAP	MJ
TMRBPS	SGSVC	FL	UPDATCCW	\$\$ANERAI	UG
		FL		\$\$RAST03	WF
TMRSW	SGSVC		UPDATE		
TPBUSY	SGTCHS	CD	UPDATE	\$\$RAST11	XN
TPBUSY1	SGTCHS	CD	UPDPUB	\$\$RAST00	VE
TPBUSY2	SGTCHS	CCA	UPDPUB	\$\$RAST02	WA
TPBUSY3	SGTCHS	CC	UPDSCAN	\$\$RAST02	WC
TPBUSY4	SGTCHS	CC	USRAPPEN	SGTCHS	CKA
				the state of the s	-

USREXT	SGUNCK	DA	XFETCH	\$\$RAST04	XA
USRSEN	SGUNCK	DB	XFETCH	\$\$RAST05	XE
USRUCK	SGUNCK	D A	XIOERR	\$\$ANERSB	UP
			XLDMOD	\$\$RAST05	ΧE
			XLDTST	\$\$RAST04	XA
VERIF	\$\$ANERRB	NN	XLDTST	\$\$RAST05	XE
VLDADR1	SGTCON	GC	XMSG	\$\$RAST04	XA
VLDADR2	SGTCON	GC	XMSG	\$\$RAST05	ΧE
VLDADR3	SGTCON	GC	XNOMSG	\$\$RAST04	XA
			XNOMSG	\$\$RAST05	ΧE
			XNORMAL	\$\$ANERSC	UR
WAIT	\$\$ANERRY	TA	XQFULL	\$\$ANERSB	UP
WAITLOOP	SGDFCH	EH	XTOERR	\$\$ANERSC	UR
WAITSVC	\$\$ANERRP	RF			
WRITEREC	\$\$RAST01	VH			
			ZEROCT	\$\$ANERR6	UD
			ZERTEB	\$\$ANERRS	RK
XEXIT	\$\$RAST04	XΑ	ZERTEBV	\$\$ANERRS	RK
XEXIT	\$\$RAST05	XE	ZROREG	SGTCHS	CR

APPENDIX B: ERROR MESSAGE CROSS REFERENCE

Messag	e Phase	2	Chart			(Data Cell) (Unit Record)	QH SE
0P08	\$\$A\$SUP1 \$\$ANERAI \$\$ANERRA	(Paper Tape)	GA UG NM		\$\$ANERRX	(Paper Tape) (Tape Cartridge Reader)	SJ UE
	\$\$ANERRF \$\$ANERRG \$\$ANERRT \$\$ANERRU \$\$ANERRV	(Tape) (Data Cell) (MICR Type) (Unit Record) (Unit Record)	PF QB SA SC SD			(3211 Printer)	UK
	\$\$ANERRX \$\$ANERR7	(MICR Type) (Paper Tape) (Tape Cartridge Reader)	SF,SG SJ UE	0P12	\$\$ANERRB \$\$ANERRK	(Disk) (Data Cell)	NN QH
		(Optical Reader) (3211 Printer)	UA UK				
				0P13	\$\$ANERRB \$\$ANERRK \$\$RAST10	(Disk) (Data Cell)	NN QH XL
0P09	\$\$ANERAM	(Paper Tape) (Tape)	GA UG PJ				
	\$\$ANERRA \$\$ANERRF		NM PF	0P14	\$\$A\$SUP1 \$\$ANERRB		GA NN
		(Data Cell)	QB		\$\$ANERRF	(Tape)	PE, PF
	* *	(MICR Type) (Unit Record)	SA SC			(Data Cell) (Unit Record)	QB SE
	\$\$ANERRV	(Unit Record)	SE			(Optical Reader)	UB
		(MICR Type)	SF,SG				
		(Paper Tape) (Tape Cartridge	SJ UC,UD				
	PAMERINO	Reader)	OC , OD	0P15	\$\$A\$SUP1	(Disk)	GA
		(Tape Cartridge Reader)	UE		\$\$ANERRA		NL QF
		(Optical Reader) (3211 Printer)	UA UK				
0010	AAS AANDA	(mi-la)	62	0P16	\$\$ANERRB \$\$ANERRK	(Disk) (Data Cell)	NN QH
0P10		(Paper Tape)	GA UG				
	\$\$ANERAM \$\$ANERRA		PJ NL	0P17	\$\$ANERAM	(Tane)	PK
	\$\$ANERRF		PE	OF I	\$\$ANERRB		NN
	\$\$ANERRG	(Data Cell)	Q A		• •	(Data Cell)	Q C
		(Unit Record)	SC				
		(Unit Record) (Paper Tape)	SD SJ				
		(Tape Cartridge Reader)	ÜC	0P18	\$\$A\$SUP1 \$\$ANERAI	(Disk) (Paper Tape)	GA UG
		(Tape Cartridge Reader)	UE		\$\$ANERAM \$\$ANERRB		PK NN
	\$\$ANERSA	(3211 Printer)	UK		\$\$ANERRT \$\$ANERRU	(Data Cell) (MICR Type) (Unit Record) (Unit Record)	QC SA SC SE
0P11	\$\$A\$SUP1		GA			(MICR Type)	SF,SH
	\$\$ANERAJ \$\$ANERAP	(Paper Tape)	ÜH PN		• •	(Paper Tape) (Tape Cartridge	SJ UE
	\$\$ANERAS		PX		/ Manaçç	Reader)	OE
	\$\$ANERRB	(Disk)	NN			(Optical Reader)	UB
	\$\$ANERRD	(Tape)	PA		\$\$ANERSA	(3211 Printer)	UK

0P19	SSANERAI	(Paper Tape)	UG	0P28	\$\$A\$SUP1	(Disk)	G A
	\$\$ANERAM		PJ			(Paper Tape)	UH
	\$\$ANERRB		NN		\$\$ANERRA		NL
		(Data Cell)	QC		\$\$ANERRF		PE
		(MICR Type)	SA			(Data Cell)	QA
		(Unit Record)	SB,SC		φγιιιωιαιο	(Data CCLL)	×
		(Unit Record)	SE SE				
		(MICR Type)	SF,SG		¢¢ANEPPT	(MICR type)	SA
		(Paper Tape)	SJ SJ			(Unit Record)	SB
		(Tape Cartridge	UC			(MICR type)	SF,SG
	PARIETINO	Reader)	00			(Paper Tape)	SJ , SG
	¢¢aniedd7	(Tape Cartridge	UE			(Tape Cartridge	AC 20
	/ ANDINAÇÇ	Reader)	OE		SAMERKO	Reader)	UC
	¢¢ a niedd o	(Optical Reader)	UB		CCANFDDQ	(Optical Reader)	UA
		(3211 Printer)	UK			(3211 Printer)	UK
	ACMUNAÇÇ	(SZII FIINCEI)	UK		ACMINAÇÇ	(3211 FIInter)	ΟĽ
0P20	\$\$A\$SUP1	(Disk)	DB, DF, GA,				
			GB				
	\$\$ANERAJ	(Paper Tape)	U J	0P29	\$\$ANERAM	(Tape)	PJ
	\$\$ANERAK		PS,PT		• •	-	
	\$\$ANERAL		PV				
	\$\$ANERAM	(Tape)	PK				
	\$\$ANERAN		PL,PM	0P30	\$\$ANERAM	(Tape)	РJ
	\$\$ANERAQ		PQ		• •	-	
	\$\$ANERAR		PW				
	\$\$ANERRE		PD				
	\$\$ANERRF	-	PE	0P31	\$\$ANERRA	(Disk)	NL
	\$\$ANERRL		PG		\$\$ANERRD		PA
		(Data Cell)	QD		\$\$ANERRF		PF
		(Data Cell)	QE			(Tape Cartridge	UC
		(Data Cell)	Q F		+ +	Reader)	•
		(Tape Cartridge	UD			noudez,	
	φφιιιωτικο	Reader)	OB				
	\$\$ANERR8	(Tape Cartridge	UF				
	φφιιιισιαιο	Reader)	01	0P32	\$\$ANERAM	(Tane)	РJ
	SSANERSB	(3211 Printer)	UP	0101	φφιτιωταπι	(1upo)	- 0
	77	,	-				
				0P33		(Unit Record)	SD
					\$\$ANERSA	(3211 Printer)	UK
0P21	\$\$A\$SUP1		GA				
	\$\$ANERRA		NL				
	\$\$ANERRJ	(Data Cell)	$Q\mathbf{F}$	0P34	\$\$ANERRW	(MICR type)	SH
0P 22	¢ ¢ a NEDDC	(Data Cell)	07	0P35	¢¢a NEDDO	(Optical Reader)	TT3
UF ZZ	SAMERING	(Data Cell)	QA	0233	SAMEKKS	(Optical Reader)	UA
0P23	SSANERRJ	(Data Cell)	QF	0P36	\$\$A\$SUP1	(Disk)	GA.
0.1.1.0	~~~~~~~	13404 0011,	x -	0	\$\$ANERRA		NL
						(Data Cell)	QF
0P24	\$\$ANERRA	(Disk)	NL		ффинис	(baca ccii)	21
01 24		(Tape Cartridge	UC				
	SAMERKO	Reader)	00	0P37	¢¢x M PDDm	(MICR type)	SA
		Readel		UF 3 /		(MICR type)	SF
					SAMEKKW	(MICK Cype)	3r
0P 25	\$\$ANERRA	(Disk)	NL				
01 23		(Tape Cartridge	UC	0P38	¢¢ anerp q	(Optical Reader)	UB
	\$\$III.DICCO	Reader)	00	0130	φφιπιμικ.	(opereur Reduct)	OB
		TOUGET /					
				0P39	SSANERR7	(Tape Cartridge	UE
0P26	\$\$ANERRA	(Disk)	NL		T T	Reader)	
		(Data Cell)	QA				
	4411101010		×**				
				0P40	SSANERAT	(Paper Tape)	ŪG
0P27	\$\$ANERRA	(Disk)	NL	•	T-T		
	\$\$ANERRC		NM				
		(Unit Record)	SB	0P41	SSANERSA	(3211 Printer)	UK
	TT				77		

0P60D	\$\$ANERRY	TB	0 T11I	\$\$RAST00	VA
0T00I	\$\$ANERAG	ŊJ	0 T 12I	\$\$RAST04	хв
	\$\$RAST11	XN		\$\$RAST05	XF
	\$\$RAST01	VF		\$\$RAST07	XH
		,		\$\$RAST10	XL
0T01I	\$\$ANERAF	NG	0 T13A	\$\$RAST04	хс
01011	SAMMENTE	110	ULLUM	\$\$RAST05	XF
				\$\$RAST10	XL
0T02I	\$\$ANERAF	NG		SOMBILO	ил
			0 T14I	\$\$RAST11	XN
0T03I	\$\$ANERAF	NG		\$\$RAST03	WE
	\$\$RAST11	XN		* *	
	\$\$RAST01	VF			
	•••		0 T15I	\$\$RAST09	XJA
OTO4I	\$\$ANERAG	NH			
			0T16I	\$\$RAST03	WE
				\$\$RAST11	XN
0T05I	\$\$RAST11	XN			
	\$\$RAST01	VF			
			0 T17I	\$\$RAST11	XN
0T06I	\$\$RAST11	XN			
	\$\$RAST03	WE	0T18I	\$\$RAST11	XN
	• •			\$\$RAST01	VF
0T07I	\$\$RAST11	XN			
	\$\$RAST03	WE	0T19I	\$\$RAST09	ХЈВ
180TO	\$\$RAST11	XN	OT20I	\$\$RAST09	XJB
	\$\$RAST03	WE			
			1I32D	\$\$ANERRO	TF
0T09I	\$\$RAST11	XN			
	\$\$RAST03	WE ·			
			1140D	\$\$ANERRO	TE
0T10I	\$\$RAST04	хв			
	\$\$RAST05	XF	1S02D	\$\$ANERRO	TF
	\$\$RAST07	ХJ			
	\$\$RAST10	XL			
			1 s 10D	\$\$ANERRO	TE

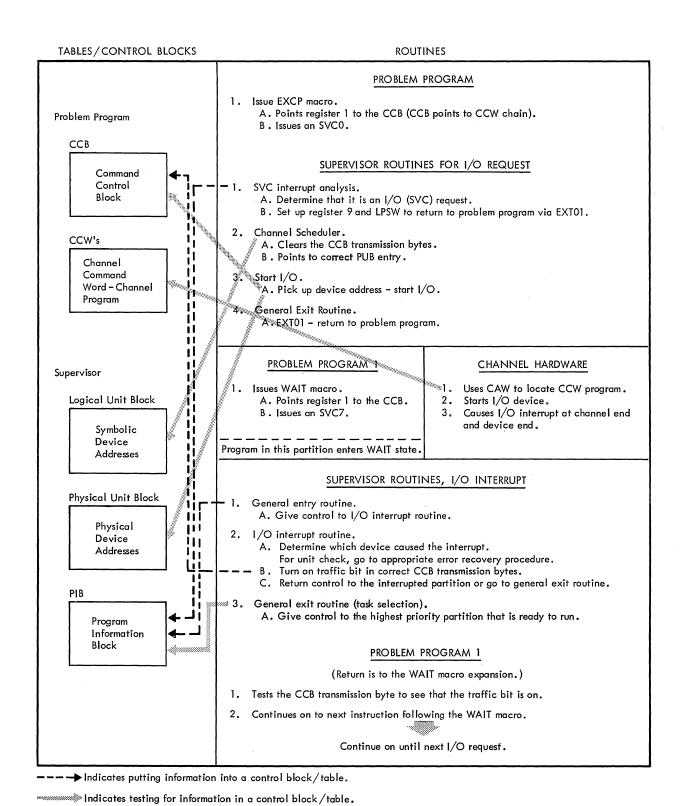


Figure 63. I/O Request-I/O Interrupt Sequence

APPENDIX D: LABEL INFORMATION FORMAT ON SYSRES

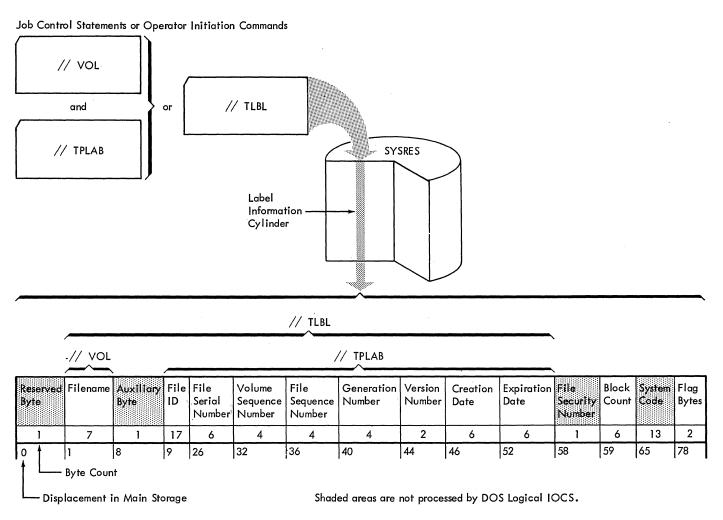


Figure 64. Format of SYSRES Tape Label Information

1	2	3		4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	Field
DLBL- EXTENT Indicator	Filename	DA/IS Switch	File ID		Format 1D	File Serial Number	Volume Seq. No.	Creation Date	Expiration Date	Reserved	Open Code	System Code	Volume Serial Number	EXTENT Type	EXTENT Seq. No.	Extent Lower Limit	Extent Upper Limit		2321 Lower Cell 2321 Upper Cell	Another Extent if DA or ISFMS
1	7	1	44		1	6	2	3	3	2	1	13	6	1	1	4	4	2	1 1	Bytes
0	-	ω	6		53	54	09	62	65	89	70	17	84	06	91	92	%	901	103	Displacement

Field	Name	Description	Field	Name	Description
1.	DLBL-EXTENT	SD Bit 0: 1 = Next extent on a new pack. Bit 1: 1 = Last extent.	12. 	System Code	Initialized to contain DOS/360 VER 3. This field is not processed by DOS.
		Bit 2: 1 = Last extent. Bit 2: 1 = Bypass extent. Bit 3: 1 = New volume on same unit.	1 1 1 1	Volume Serial No.	Volume serial number for extent.
		Bit 4: 1 = Extent limits omitted. Bit 5: 1 = Extent converted to DASD address. Bit 6: 1 = No EXTENT/XTENT card. Bit 7: 1 = Unused. DA or ISFMS Number of extents.	14. 	Extent Type	Same codes as in Format - 1 label: X'00' = Next three fields do not indicate any extent. X'01' = Prime data area (ISFMS) or consecutive area, etc., (that is the extent containing the user's data records).
2.	Filename		! !		X'02' = Overflow area of an ISFMS file. X'04' = Cylinder index or master index of an ISFMS file.
3.	DA/IS Switch	Bits 0-3: Unused. Bit 4: 1 = Extent limits omitted. Bit 5: 1 = Extent converted to DASD address.	! 		X'40' = User label track area. X'8n' = Shared cylinder indicator, where n = 1, 2, or 4.
		Bit 6 & 7: Unused.	15. 	Extent Seq. No.	Number of extent as determined by the extent card sequence.
4.	File ID	File identifier including generation and version numbers. If field is missing on DLBL card, Filename padded with blanks is inserted.	i 16. & 17.	Extent Lower and Upper Limits	Before the OPEN, DLBL/EXTENT information is in the relative track form of HHNNT followed by three bytes of binary
5.	Format ID	Numeric 1 is inserted.	! !		zeros. HH = Relative (to 0) start address in tracks. NN = Number of tracks.
6.	File Serial No.	Volume serial number from first extent.	: 		T = 0 or upper track number for split cylinder in SD files.
7.	Volume Seq. No.	Always initialized to X'0001'.	! !		Following an OPEN on DLBL/EXTENT cards, or whenever DLAB/XTENT cards are used,
8.	Creation Date	Initialized with 3 bytes of X'00'.	! !		the extent lower and upper limits are each in the CCHH format.
9.	Expiration Date	If date is in the form YYDDD, it is converted to YDD. If date is in retention period form, I to 4 characters, the field is padded with binary zeros.	 18. 	Logical (Symbolic) Unit Address	This 2-byte field identifies the logical unit with the same code as that used in a CCB. The first byte identifies the unit class:
10.	Reserved	The retention period, if specified is converted to a 2-byte number and inserted in this field.	; ! ! ! !		X'00' = System Logical Unit X'01' = Programmer Logical Unit The second byte identifies the logical unit within its class.
11.	Open Code	DLBL type: S = Sequential D= Direct Access	 19.		Thus X'0003' denotes SYSLST and X'0103' denotes SYS003.
		C or E = Indexed sequential File Management System where: C = Load create function E = Load extend function		2321 Lower Cell 2321 Upper Cell	2321 extent lower and upper cell limit. This 2-byte field contains zeros for 2311/2314/2319 disk.

Note: For Sequential Disk files, a complete 104-byte block is repeated for each new EXTENT. For Direct Access and ISFMS files, only fields 13 through 18 are repeated for each EXTENT.

Figure 65. Format of SYSRES DASD Label Information

APPENDIX E: PROGRAM KEY DEFINITIONS

PID (Partition Identifier)

The PID is a halfword long, consisting of a zero value in the high-order byte and the key value in the low-order byte. The key value is the key of the partition that was last enabled for interrupts. Key values are X'00', X'10', X'20',...X'60' for All Bound, BG, F2, F1, Attention, Quiesce I/O and Supervisor, respectively.

PID is defined in an AP (asynchronous processing) supervisor only and is found at byte-displacement 46 in the communications region. (This halfword is named PIK in a non-AP supervisor. See PIK below.)

PIK (Program Interrupt Key)

The PIK is a halfword long, consisting of a zero value in the high-order byte and the key value in the low-order byte. The key value is the key of the program that was last enabled for interrupts.

When an interrupt occurs, the value of the PIK indicates to the supervisor which program (task) was interrupted. It can also be used by transient programs and problem programs to determine if they are running as BG, F1, or F2, or, in the AP supervisor, if the last interrupted task was a maintask or a subtask.

The value of the PIK equals the displacement from the beginning of the PIB table to the PIB entry for the program (task). For BG, F2, and F1 tasks, this value equals the storage protect key multiplied by sixteen.

In a non-AP supervisor, PIK is found at displacement 46 in the communications region. In an AP supervisor PIK is found at displacement 18 in the communication region extension. (Also see PID.)

<u>Task</u>	PIK Value	
All Bound*	X 00	
BG	X'10'	
F2*	x'20'	
F1*	x'30'	
AR	X'40'	
Quiesce I/O	x"50"	
Supervisor	X'60'	
Subtask**	x'70' - x'	FO "

- *Multiprogramming generation option only.
- **Asynchronous processing generation option only. A total of nine subtask PIBs is generated, thus the displacement hex 70-F0 indicates the maximum range.

The PIK is set by task selection within the general exit routine. The fetch routine sets the PIK to X'60', because it enables itself for interrupts and because it gets control directly from the SVC interrupt routines. Like other completely disabled supervisor routines, the SVC interrupt routines do not change the PIK from the value it had when the interrupt occurred that transferred control.

LID (Logical Transient Identification)

The LID contains the same value as the PIK when the logical transient area is in use (i.e., the LID identifies ownership of the logical transient area). When this transient area is free, the halfword LID contains zeros. The SVC 2 routine sets the LID, and the SVC 11 routine resets it to zero. LID is defined only in an AP supervisor. See also LTK, PIK, and PID.

LTK (Logical Transient Key)

The LTK has the same value as the PIK when the logical transient area is in use. When the transient area is free, the LTK equals zero. The SVC 2 routine sets the LTK, and the SVC 11 routine resets it to zero.

RID (Requestor Identification)

See Figure 17, REQID (Item F).

RIK (Requestor I/O Key)

When a supervisor routine (fetch or physical transient) issues an SVC 0 or SVC 15, the routine puts the value to be used in the CAW storage protect key into the high-order digit of the second byte of the RIK halfword. When this value is zero, the low order digit has these special meanings:

Physical transients put a X'01' into the RIK when they are doing a SYSLOG I/O. The PIK for physical transients has a value of X'06', therefore the channel scheduler would type "SP" (supervisor ID) as the SYSLOG ID. The physical transients put the ID of the program referred to by the message into the message.

RIK	<u>Meaning</u>
X'01'	This is a SYSLOG I/O request.
	The channel scheduler is not to
	type a SYSLOG ID prefix.

type a SYSLOG ID prefix.

X'02'. This has been a fetch I/O request. This special code is required by ERP to recognize fetch requests.

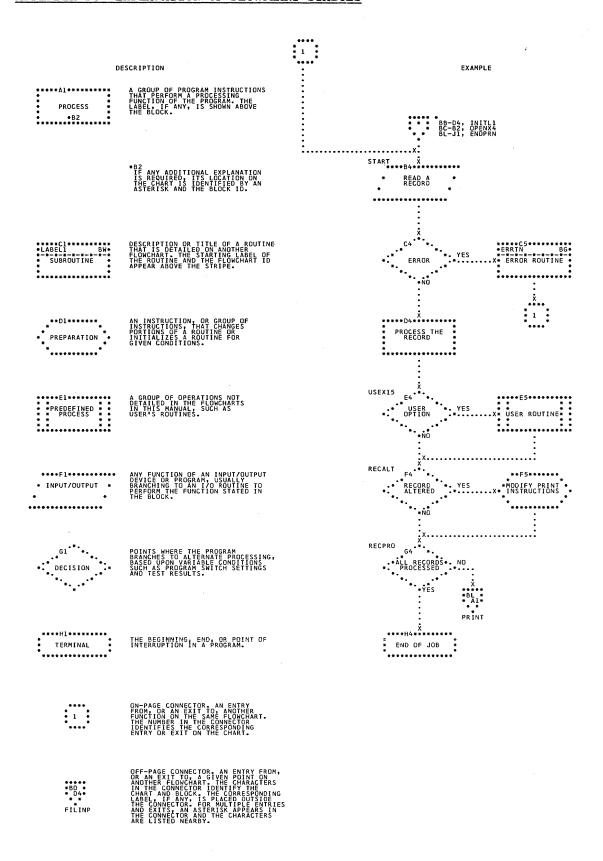
Fetch always sets a X'02' in the RIK. ERP transients put the key of the program requiring ERP into the RIK, when the ERP is a retry of a user EXCP and the ERP transient requires control to return to itself.

FIK (Fetch I/O Key)

Used by the fetch to validate the phase name address and load address. FIK has the following values:

ey of the problem equestor.	program		
-			
ey of the problem			
	equestor if the transient	if the transient issued the ey of the problem program if	if the transient issued the SVC ey of the problem program if not

APPENDIX F: EXPLANATION OF FLOWCHART SYMBOLS



m1					
	gives the rela		\$\$ANERRB	None	CTL.019.00
		ocatable module	(\$\$ANERRA)		
	iche labels, a	and microfiche	\$\$ANERRC	None	CTL.019.00
identification	n numbers.		(\$\$ANERRA)		
	k indicates th				
	e microfiche l		\$\$ANERRD*	None	CTL. 020.00
		e module name, it	\$\$ANERRE*	None	CTL. 021.00
is so indicat	ed in parenthe	eses.	\$\$ANERRF*	None	CTL.022.00
			\$\$ANERRG*	None	CTL.023.00
	se or module t		\$\$ANERRH*	None	CTL.024.00
	ofiche card, t		\$\$ANERRI*	None	CTL.025.00
	n number of or	aly the first	\$\$ANERRJ*	None	CTL.026.00
card is shown	l•		\$\$ANERRK*	None	CTL.027.00
			\$\$ANERRL*	None	CTL.028.00
The index	includes all t	he macro names	\$\$ANERRM*	None	CTL.029.00
	ation numbers.				
	on the microf				
further ident	ified by rows	A to E. The	\$\$ANERRN*	None	CTL.030.00
		macros that use	\$\$ANERRO*	None	CTL.031.00
more than one	microfiche ca	ard.	\$\$ANERRP*	None	CTL.032.00
			\$\$ANERRQ*	None	CTL.033.00
For the co	mplete microfi	che	\$\$ANERRR*	None	CTL.034.00
cross-referen	ce index, see	Introduction to	\$\$ANERRS*	None	CTL. 035.00
DOS Logic, li	sted in the Pr	eface.	\$\$ANERRT*	None	IOM.001.00
			\$\$ANERRU*	None	CTL. 036.00
			\$\$ANERRV*	None	CTL.037.00
			\$\$ANERRW*	None	IOM.002.00
			• •		
Core Image	Relocatable		\$\$ANERRX*	None	CTL.038.00
Core Image Phase Name	Relocatable Module Name	Card ID	\$\$ANERRX* \$\$ANERRY*	None	CTL.039.00
Phase Name	Module Name		\$\$ANERRY* \$\$ANERRZ		
Phase Name	Module Name	Card ID	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY)	None None	CTL.039.00 CTL.039.00
Phase Name	Module Name		\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERR0	None	CTL.039.00
Phase Name	Module Name		\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY)	None None	CTL.039.00 CTL.039.00
Phase Name \$\$A\$SUP1 (see \$\$ANERAA*	Module Name individual ma	cro phase names)	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERR0	None None	CTL.039.00 CTL.039.00
Phase Name \$\$A\$SUP1 (see	Module Name	CTL.002.00 CTL.003.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY)	None None	CTL.039.00 CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00
Phase Name \$\$A\$SUP1 (see \$\$ANERAA*	Module Name individual ma	cro phase names)	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY) \$\$ANERRY)	None None None	CTL.039.00 CTL.039.00 CTL.039.00
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB*	Module Name individual ma	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY) \$\$ANERR1* \$\$ANERR6*	None None None None	CTL.039.00 CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC*	Module Name individual ma None None None None	CTL.002.00 CTL.003.00 CTL.004.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR7*	None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00
Phase Name \$\$A\$\$UP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAC*	Module Name individual ma None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR7* \$\$ANERR8*	None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00
Phase Name \$\$A\$\$UP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAC* \$\$ANERAD* \$\$ANERAE*	Module Name individual ma None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR7* \$\$ANERR8* \$\$ANERR8* \$\$ANERR9*	None None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00 IOR.001.00
Phase Name \$\$A\$\$UP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAC* \$\$ANERAD* \$\$ANERAE* \$\$ANERAE*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR7* \$\$ANERR7* \$\$ANERR8* \$\$ANERR9*	None None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00 IOR.001.00 CTL.043.50
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAC* \$\$ANERAD* \$\$ANERAE* \$\$ANERAE* \$\$ANERAE* \$\$ANERAE*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.008.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR7* \$\$ANERR8* \$\$ANERR8* \$\$ANERR9*	None None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00 IOR.001.00 CTL.043.50 CTL.043.60
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAD* \$\$ANERAE* \$\$ANERAE* \$\$ANERAF* \$\$ANERAG* \$\$ANERAG*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.007.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR7* \$\$ANERR8* \$\$ANERR9* \$\$ANERSA* \$\$ANERSB* \$\$ANERSC*	None None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00 IOR.001.00 CTL.043.50 CTL.043.50 CTL.043.70
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAD* \$\$ANERAE* \$\$ANERAE* \$\$ANERAE* \$\$ANERAE* \$\$ANERAE* \$\$ANERAG* \$\$ANERAI*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.009.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR8* \$\$ANERR8* \$\$ANERS8* \$\$ANERSB* \$\$ANERSC*	None None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00 IOR.001.00 CTL.043.50 CTL.043.50 CTL.043.70
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAC* \$\$ANERAE* \$\$ANERAE* \$\$ANERAF* \$\$ANERAG* \$\$ANERAI* \$\$ANERAJ* \$\$ANERAK*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.009.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR8* \$\$ANERR8* \$\$ANERS8* \$\$ANERSB* \$\$ANERSC*	None None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00 IOR.001.00 CTL.043.50 CTL.043.60 CTL.043.70
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAE* \$\$ANERAE* \$\$ANERAF* \$\$ANERAF* \$\$ANERAI* \$\$ANERAJ* \$\$ANERAK* \$\$ANERAL*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.008.00 CTL.009.00 CTL.010.00 CTL.011.00 CTL.011.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR8* \$\$ANERR8* \$\$ANERS8* \$\$ANERSB* \$\$ANERSC*	None None None None None None None None	CTL. 039.00 CTL. 039.00 CTL. 040.00 CTL. 041.00 CTL. 042.00 CTL. 043.00 IOR. 001.00 CTL. 043.50 CTL. 043.60 CTL. 043.70 CTL. 257.00 CTL. 257.00 CTL. 259.00
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAE* \$\$ANERAE* \$\$ANERAF* \$\$ANERAF* \$\$ANERAI* \$\$ANERAJ* \$\$ANERAK* \$\$ANERAL* \$\$ANERAL*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.008.00 CTL.009.00 CTL.010.00 CTL.011.00 CTL.011.00 CTL.012.00 CTL.013.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR8* \$\$ANERR8* \$\$ANERSB* \$\$ANERSB* \$\$ANERSC* \$\$RAST00* \$\$RAST01* \$\$RAST02* \$\$RAST03*	None None None None None None None None	CTL.039.00 CTL.039.00 CTL.040.00 CTL.041.00 CTL.042.00 CTL.043.00 IOR.001.00 CTL.043.50 CTL.043.60 CTL.043.70 CTL.257.00 CTL.258.00 CTL.259.00 CTL.259.00
Phase Name \$\$A\$\$UP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAC* \$\$ANERAE* \$\$ANERAF* \$\$ANERAF* \$\$ANERAI* \$\$ANERAJ* \$\$ANERAK* \$\$ANERAK* \$\$ANERAK* \$\$ANERAK* \$\$ANERAL* \$\$ANERAM* \$\$ANERAM*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.009.00 CTL.010.00 CTL.010.00 CTL.011.00 CTL.011.00 CTL.012.00 CTL.013.00 CTL.014.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRY) \$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR8* \$\$ANERR8* \$\$ANERSB* \$\$ANERSB* \$\$ANERSC* \$\$RAST00* \$\$RAST01* \$\$RAST02* \$\$RAST04*	None None None None None None None None	CTL. 039.00 CTL. 039.00 CTL. 040.00 CTL. 041.00 CTL. 042.00 CTL. 043.00 IOR. 001.00 CTL. 043.50 CTL. 043.60 CTL. 043.70 CTL. 257.00 CTL. 258.00 CTL. 259.00 CTL. 260.00 CTL. 261.00
Phase Name \$\$A\$SUP1 (see \$\$ANERAA* \$\$ANERAB* \$\$ANERAC* \$\$ANERAC* \$\$ANERAF* \$\$ANERAF* \$\$ANERAF* \$\$ANERAJ* \$\$ANERAJ* \$\$ANERAJ* \$\$ANERAL* \$\$ANERAL* \$\$ANERAL* \$\$ANERAN* \$\$ANERAN*	Module Name individual ma None None None None None None None None	CTL.002.00 CTL.003.00 CTL.004.00 CTL.005.00 CTL.006.00 CTL.007.00 CTL.009.00 CTL.010.00 CTL.010.00 CTL.011.00 CTL.011.00 CTL.012.00 CTL.013.00 CTL.014.00 CTL.015.00	\$\$ANERRY* \$\$ANERRZ (\$\$ANERRY) \$\$ANERRO (\$\$ANERRY) \$\$ANERR1* \$\$ANERR6* \$\$ANERR6* \$\$ANERR8* \$\$ANERS8* \$\$ANERSB* \$\$ANERSC* \$\$RAST00* \$\$RAST01* \$\$RAST02* \$\$RAST04* \$\$RAST04*	None None None None None None None None	CTL. 039.00 CTL. 039.00 CTL. 040.00 CTL. 041.00 CTL. 042.00 CTL. 043.00 IOR. 001.00 CTL. 043.50 CTL. 043.60 CTL. 043.70 CTL. 257.00 CTL. 258.00 CTL. 259.00 CTL. 260.00 CTL. 261.00 CTL. 262.00
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Macro Name	Card ID	Row	SEND	453.012.50	A-D
•			SGDFCH	453.013.00	A
ALLOC	453.001.00	A	SGDSK	453.013.00	В
ASSGN	453.001.00	В	SGSVC	453.013.00	C-E
COMMN	453.003.00	D	SGTCHS	453.014.00	A-D
COMMNEX	453.003.50	A	SGTCON	453.014.01	A
CONFG	453.004.00	A	SGTHAP	453.014.01	C-E
DVCGEN	453.006.00	В	SGUNCK	453.014.50	A,B
FOPT	453.007.00	C,D	SMCRR	453.012.00	B,C
IOTAB	453.008.50	A,B	SMICR	477.002.00	A,B
LUBGEN	453.008.00	E	STDJC	453.015.00	В
MAPLOWC	453.008.50	D	SUPVR	453.015.00	D
MCRAS	453.008.50	E	TRTAB	453.014.01	В
PIOCS	453.010.00	A			

For a more complete list of data processing terms, refer to <u>IBM Data Processing</u>
<u>Techniques</u>, A Data Processing Glossary, GC20-1699.

ASCII (American National Standard Code for Information Interchange): A 128-character, 7-bit code. The high-order bit in the System/360 8-bit environment is zero.

buffer:

- 1. A storage device in which data is assembled temporarily during data transfer. An example is the IBM 2821 Control Unit, a control and buffer storage unit for card readers, card punches, and printers.
- punches, and printers.2. During I/O operations, a portion of main storage into which data is read or from which data is written.

<u>CCH (channel check handler)</u>: A feature that assesses System/370 channel errors to determine if the system can continue operations.

channel inboard error: An error that
occurs between one I/O device and the
central processing unit.

chronological area of the recorder file:
The area of the recorder file (IJSYSRC)
where error records are printed as they
occur. The record types included are:
OBR, MCRR, MCAR, CCH, BTAM, QTAM, and 2715
error records. This area is present on
both the System/360 and System/370 recorder
files and differs from the SDR area where
cumulative errors are recorded by device
type.

core image library: A SYSRES area (or a
device of the same type as SYSRES) that
stores programs processed by the linkage
editor. Each program is in a form that can
be executed in main storage.

core wrap mode: The method of operation that records the events of a trace in main storage. It is the default process when no output device for the trace has been specified. The contents can be displayed by either a dump program or manually from the console.

<u>data set security</u>: A feature that provides protection for disk files. A data secured file cannot be accidentally accessed by a problem program.

<u>Disk Operating System</u>: A disk resident system that provides operating system capabilities for 16K and larger IBM System/360 and System/370 systems.

DOS Volume Statistics: A facility that monitors and records the number of temporary read and write errors on currently accessed tape volumes. This facility has two options, Error Statistics by Tape Volume (ESTV) and Error Volume Analysis (EVA).

EREP (environmental recording, editing and printing): A program that processes the data contained on the system recorder file.

ESTV (Error Statistics by Tape Volume):
One of the two options of the DOS Volume
Statistics. With ESTV support, the system
collects data on tape errors by volume for
any tape volumes used by the system.

EVA (Error Volume Analysis): One of the two options of the DOS Volume Statistics. With this option, the system issues a message to the operator when a number of temporary read or write errors (specified by the user at system generation time) has been exceeded on a currently accessed tape volume.

F/L Trace (Fetch/Load Trace): A program that records information about phases and transients as they are called from a core image library.

fetch

- To bring a program phase into main storage from a core image library for immediate execution.
- 2. The routine that retrieves requested phases and loads them into main storage.
- 3. The name of a macro instruction (FETCH) used to transfer control to the system loader.
- To transfer control to the system loader.

GSVC Trace (Generalized Supervisor Calls Trace): A program that records SVC interrupts as they occur. All or a selected group of SVCs can be traced.

I/O (input/output) error logging: The
process of recording OBR and SDR records on
the system recorder file.

IDRA (independent directory read-in area):
A resident area, created by a supervisor option into which the system reads core

image library directories for fetch and load operations. Using IDRA frees the physical transient area to perform error recovery procedures.

IOCS (input/output control system): group of macro instruction routines provided by IBM for handling the transfer of data between main storage and external storage devices.

I/O Trace (Input/Output) Trace): A program that records I/O device activity for all or a selected group of I/O devices.

job accounting interface: A function that accumulates accounting information for each job step to: charge usage of the system, help plan new applications, and help supervise system operation more efficiently.

MCAR (machine check analysis and recording): A feature that records System/370 machine check interrupt error information on the system recorder file and then attempts to recover from the interrupt.

MCRR (machine check recording and recovery): The recording of pertinent data
on the system recorder file after either a machine check interrupt or a channel inboard error occurred on System/360 Model 30, Model 40, or Model 50.

MCI (machine check interrupt): The interrupt that occurs if the central processing unit fails to operate.

object module: One or more control sections in relocatable, nonexecutable form. An object module must be processed by the linkage editor before it can be executed in the system.

OBR (outboard recorder): A feature that records pertinent data on the system recorder file when an unrecoverable I/O error occurs.

overlay: A program segment (phase) that is loaded into main storage. It replaces all or part of a previously retrieved section.

PCIL (private core image library): A file referenced in the same manner and for the same purposes as the system core image library, but distinct from the system core image library. PCIL increases available core image library space to enable

compiling, linkage editing, and executing in the foreground partition, when a private core image library is assigned to that foreground partition.

PDAID (Problem Determination Aids): Programs that trace a specified event when it occurs during the operation of a program. The traces provided are QTAM Trace, I/O Trace, F/L Trace, and GSVC Trace.

private library: A relocatable, core image, or source statement library that is separate and distinct from the system library.

problem determination: A procedure or process (provided by IBM) that the user can follow after an error message to determine the cause of that error. (See PDAID)

QTAM Trace: A routine that records certain supervisor and I/O activities on tape or in main storage.

RDE (Reliability Data Extractor): A function that provides hardware reliability data that is analyzed by IBM.

RMS (recovery management support): A feature for System/370 that consists of the MCAR (machine check analysis and recording) and CCH (channel check handler) functions. RMS gathers information about System/370 hardward reliability and attempts certain error recovery operations. RMS is a part of the entire reliability, availability, and serviceability support for System/370.

SDR (statistical data recorder): A feature that records the cumulative error status of an I/O device on the system recorder file.

stand-alone dump: A program that displays the contents of main storage from a minimum of 8K bytes to a maximum of 16384K bytes. It helps to determine the cause of an

system recorder file: The file that is used to record hardware reliability data.

track hold: A function for protecting DASD tracks that are currently being processed. When track hold is specified in the DTF, a track that is being modified by a task on one partition cannot be concurrently accessed by a task or subtask in another partition.

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DOS SUPERVISOR AND RELATED TRANSIENTS PROGRAM LOGIC MANUAL

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This Technical Newsletter, a part of Release 26 of the IBM Disk Operating System, provides replacement pages for your publication. These replacement pages remain in effect for subsequent DOS releases unless specifically altered. Pages to be inserted an and/or removed are:

Cover-2		159,160	277,278	
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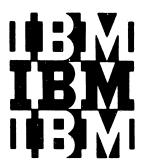
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Summary of Amendments

This TNL contains documentation changes for:

Enhancements to OLTEP
IBM 3211 Printer Error Recovery Procedures
RMS generation and operation
Maintenance changes and technical correction.

Note: Please insert this page in your publication to provide a record of changes.



Program Logic

DOS Supervisor and Related Transients

Program Number 360N-CL-453

This reference publication describes the internal logic of the IBM Disk Operating System, Supervisor and Physical and Recovery Transient Programs. It is for persons involved in program maintenance and for system programmers altering the program design. Program logic information is not needed for normal operation of these programs. This publication is a supplement to the program listing.

Effective use of this manual requires an understanding of IBM System/360 or System/370 operation and of IBM Disk Operating System control and service programs, macro instructions, and operating procedures. Reference publications for this information are listed in the Preface of this manual.

Third Edition (June, 1971)

This publication was formerly titled <u>IBM System/360 Disk</u> Operating System, Supervisor and Physical Transients Program <u>Logic Manual</u>. Although titles of some DOS publications (including this one) have been simplified, the change does not affect the contents of the publication.

This edition, with Technical Newsletter GN33-8692, applies to Release 26 of the IBM Disk Operating System and to all subsequent releases until otherwise indicated in new editions or Technical Newsletters. Changes are continually made to the specifications herein; before using this publication in connection with the operation of IBM systems, consult the latest System/360 and System/370 SRL Newsletter, GN20-0360, for the editions that are applicable and current.

This edition, GY24-5151-2, is a major revision of, and obsoletes, GY24-5151-1.

Summary of Amendments

This edition documents addition of, and changes to, the following information: PCIL (Private Core Image Library), JAI (Job Accounting Interface), System/370 RMS (Recovery Management Support), IDRA (Independent Directory Read-in Area), OLTEP (On-Line Test Executive Program), EREP (Environmental Recording, Editing, and Printing) enhancements, IBM 3211 Printer, System/360 Model 22, and certain maintenance enhancements.

Technical Newsletter GN33-8692 contains documentation changes for:

- Enhancements to OLTEP
- IBM 3211 Printer Error Recovery Procedures
- RMS generation and operation
- An interface has been provided for the 2596 Card Read Punch support, which will be released at a future date
- Maintenance changes and technical corrections

Changes or additions to the text and illustrations are indicated by a vertical line to the left of the change.

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Name	Macro Description	Parameter Option	Option Description
SUPVR	Describes system environment	SYSTEM DISK	System residence (SYSRES) must be on a disk device.
		$MPS = \left\{ \frac{NO}{YES} \right\}$	Indicates multiprogramming support. If YES or BJF is specified, the system generated is capable of supporting two foreground programs. YES or BJF must be specified if TP = QTAM. If BJF is specified, the system generated will support batched mode for both foreground partitions. Multiple communications regions are generated only if MPS = BJF. MPS = YES is implied if MPS = BJF.
		$TP = \begin{pmatrix} \frac{NO}{BTAM} \\ QTAM \\ QTAMn \end{pmatrix}$	Specify if Basic or Queued Teleprocessing Access Method (BTAM or QTAM) is desired. When QTAM is specified, SVC support for BTAM is also included. To process QTAM in a system with asynchronous processing support, QTAMn must be specified where n is the maximum number of active QTAM message processing programs in the system. From 2 to 12 programs may be specified with a default value of 2.
		$ERRLOG = \begin{cases} \frac{NO}{YES} \\ RDE \\ n \\ (YES, RDE) \\ (n, RDE) \end{cases}$	Specify if the Outboard Recorder (OBR) is to record data pertinent to an error that cannot be retried or corrected after a standard number or retries. Also, specify if the Statistical Data Recorder (SDR) is to record the cumulative error status of an I/O device. n defines the number of records required on the SDR partition of the Recorder File, where n is any number equal to, or greater than, the number of PUBs. YES indicates a number of SDR records equal to the number of PUBs. ERRLOG = RDE supports the Reliability Data Extractor for System/370 only. If RDE is specified without YES or n, YES is assumed. ERRLOG is assumed YES for all System/370 MODEL options if it is not specified.
		$MCRR = \left\{ \frac{NO}{YES} \right\}$	Specify if MCRR is to record pertinent data after a machine check, channel control check, interface control check, or channel data check. MCRR analyzes collected data and cancels the damaged partition(s). No attempt at error retry is made. This parameter is valid only for Models 30, 40, and 50.
		MICR = $\begin{pmatrix} \frac{NO}{1412} \\ 1419 \\ 1419D \end{pmatrix}$	Indicates whether the supervisor is to support magnetic ink character readers or optical reader/sorters. If both 1412s and 1419s are present, indicate 1419. 1419D/1275 indicates Dual Address Adapter 1419s. If 1412/1419/1255/1259/1270/1275s are attached to the multiplexor channel, the PIOCS parameter BMPX = YES is not supported.
		$AP = \left\{ \frac{NO}{YES} \right\}$	Indicates asynchronous processing support. This provides the user with the facility to write dependent programs to run concurrently within a partition and still maintain the partition independency of MPS. If YES is specified, global BG20 (MPS = YES or BJF) is forced on whether or not it was specified.
		$EU = \begin{cases} \frac{NO}{YES} \\ RELOC \end{cases}$	EU = YES specifies: IBM 1401/1440/1460 Emulator for Models 25, 30, or 40; IBM 1401/1440/1460 or 1410/7010 Emulator and mixed parity tape processing for System/370 CPUs. If foreground emulation is desired on any model, MPS = BJF is required. Foreground emulation on Model 40 requires EU = RELOC.
		$ASCII = \left\{ \frac{NO}{YES} \right\}$	Indicates whether the supervisor is to support the American National Standard Code for Information Interchange (ASCII). YES adds 512 bytes to supervisor size.
CONFG	Describes hardware features	$MODEL = \left\{ \frac{30}{nn} \right\}$	nn defines the System/360 model number (Model 30, 40, or 50 must be entered if MCRR option is specified). nnn defines the System/370 model number. (A System/370 model causes generation of MCAR/CCH support. MCRR is not compatible with System/370.)
		$SP = \left\{ \frac{NO}{YES} \right\}$	Indicates the storage protection feature is desired. YES is assumed if MPS = YES or BJF in the SUPVR macro.
		$DEC \left\{ \frac{NO}{YES} \right\}$	Decimal feature.
		$FP = \left\{ \frac{NO}{YES} \right\}$	Floating-point feature.
		TIMER = $\left\{ \frac{NQ}{YES} \right\}$	Timer feature. If TIMER = YES the supervisor macro GETIME is supported.
		PORT = $\left\{\frac{NO}{155}\right\}$	Causes Model 155 MCAR/CCH functions if MODEL = 145.

Figure 4. Supervisor Macros (Part 1 of 5)

Name	Macro Description	Parameter = Option	Option Description
STD JC	Sets standard values for job control variables.	$DECK = \left\{ \frac{YES}{NO} \right\}$	Output modules on SYSPCH.
		LIST = $\left\{\frac{\text{YES}}{\text{NO}}\right\}$	Source modules listings from language translators on SYSLST.
		$XREF = \left\{ \frac{YES}{NO} \right\}$	Language translators output symbolic cross-reference lists on SYSLST.
		$ERRS = \left\{ \frac{YES}{NO} \right\}$	Compilers summarize all errors in source programs on SYSLST.
		$LOG = \left\{ \frac{YES}{NO} \right\}$	Listing of all control statements on SYSLST.
		$DUMP = \left\{ \frac{YES}{NO} \right\}$	Dump of registers and main storage on SYSLST.
		LINES = $\left\{\frac{56}{nn}\right\}$	Number of lines per page on SYSLST.
		$DATE = \left\{ \frac{MDY}{DMY} \right\}$	Format of date.
		$CHARSET = \left\{ \frac{48C}{60C} \right\}$	Specifies the 48 or 60 character set for language translator input on SYSIPT.
		LISTX = $\left\{ \frac{NO}{YES} \right\}$	Hexadecimal object module listings from compilers on SYSLST.
		$SYM = \left\{ \frac{NO}{YES} \right\}$	Assembler output symbol tables on SYSPCH.
		$SPARM = \left\{ \frac{NO}{YES} \right\}$	Support of assembler variable symbol &SYSPARM
FOPT	Describes functional supervisory options	$OC = \left\{ \frac{NO}{YES} \right\}$	Operator initiated communications to problem programs. If OC=YES, the facility is available to all programs in MPS. Must be YES if Emulator on System/370 is used. OLTEP=YES forces OC=YES.
		$PC = \left\{ \frac{NO}{YES} \right\}$	Problem program routine for program check. If PC = YES, the facility is available to all programs in MPS.
		$IT = \left\{ \begin{array}{l} \frac{NO}{BG} \\ F1 \\ F2 \end{array} \right\}$	Problem program ability to set timer intervals and specify a timer interrupt routine. BG, F1, or F2 indicates which program has the facility. When IT is specified for a partition, TIMER = YES is assumed in the CONFG macro. Timer support is available to only one program in MPS.
		$AB = \left\{ \frac{NO}{YES} \right\}$	Provides for valid use of the STXIT (AB) macro. If AB = YES, the facility is available to all programs in MPS.
		$TEB = \left\{ \frac{NO}{n} \right\}$	Tape error statistics are to be accumulated and logged, where n is the number of 2400-series tape units and tape cartridge readers (maximum of 225) attached to the system. **
		$TEBV = \begin{cases} \begin{cases} \frac{NO}{DASD} \\ (syslog) \end{cases}, n \end{cases}$	Tape Error Statistics by Volume are to be accumulated and logged on SYSLOG or a DASD device, where n is the number of 2400 series tape drives attached to the system. **
		$EVA = \left\{ \left(rth, \frac{NO}{wth}, n \right) \right\}$	Error Volume Analysis is supported where rth is the read error threshold, wth is the write error threshold, and n is the number of 2400 series tape drives attached to the system. **
		** The n specified in TEB, TE are specified, and then TA	I BV, and EVA must be identical if two or more of these options PE=9 is assumed.

Figure 4. Supervisor Macros (Part 2 of 5)

Name	Macro Description	Parameter Option	Option Description
FOPT (cont'd)		$SKSEP = \begin{cases} \frac{NO}{YES} \\ n \end{cases}$	Specifies if SEEKs are to be separated from the remainder of channel programs. Seek separation allows other devices on the channel to be accessed (including other seeks) during the seek. YES indicated support for all DASD types specified by the DVCGEN macro at system generation time. n is the number of DASD to be supported and cannot be less than the number of DASD specified at system generation. The maximum number is 254.
		$CE = \left\{ \frac{NO}{YES} \right\}$	Specify the number of bytes to be aalocated to the problem determination programs. 800 is the minimum number of bytes that can be specified. For the actual number of bytes allocated, see Figure 1–6.
		$CCHAIN = \left\{ \frac{NO}{YES} \right\}$	Command chaining support for retry on I/O operations. When an error occurs and CCHAIN = YES, the user is allowed to retry at the last CCW executed instead of at the first CCW in the channel program as is the case in a normal retry. This option requires that the appropriate bit be set in the CCB.
		$PTO = \left\{ \frac{NO}{YES} \right\}$	Physical Transient Overlap allows tasks to be selected during the time of FETCH, LOAD, MVCOM, and ERP I/O. PTO is valid only when MPS = YES or MPS = BJF in the SUPVR macro.
		$CBF = \left\{ \frac{NO}{n} \right\}$	Console Buffering provides immediate return to the caller when write I/O to SYSLOG is issued where SYSLOG is a 1052. n indicates the number of buffers to be generated. 1 to 50 buffers may be specified. 1 is assumed if the operand is invalid.
		$IDRA = \left\{ \frac{NO}{YES} \right\}$	Independent Directory Read-in Area feature. YES option causes generation of the IDRA area in supervisor. IDRA reduces contention for the PTA in fetch operations when ERP is active. Use of IDRA requires MPS = YES or BJF and PTO = YES.
		$TRKHLD = \left\{ \frac{NO}{n} \right\}$	If n is specified, coding to support the HOLD and FREE track macros. TRKHLD = n specifies the number of tracks to be held at any one time, and a Track Hold Table (See Figure 24) is generated for that number. If n is not in the range of 1 to 225, 10 is assumed.
		$WAITM = \left\{ \frac{NO}{YES} \right\}$	Provides for valid use of the WAITM macro, waiting for one of a number of events to occur before continuing with task execution. Waits are performed on Event Control Blocks, which may be of the special form as in Figure 34. Other blocks that may be used as ECBs are CCBs, TECBs, and MICR CCBs since posting is done in bit 0 byte 2 of the block.
	·	** RETAIN = $\left\{ \frac{NO}{YES} \right\}$	Specifies if the data link to the Remote Analysis Center is to be supported. RETAIN = YES is valid only if a S/370 CPU was specified in the MODEL option.
		DASDFP = $\begin{cases} \frac{NO}{(n,n,2311)} \\ (n,n,2314) \\ (n,n,2321) \end{cases}$	Supervisory DASD file protection, where (n,n) indicates the range of channels to which DASDs may be attached. Specifying 2311 or 2314 indicates support for both. 2321 option indicates support for 2321 device as well as for 2311 and 2314. DASDFP prevents the user from writing outside the extents of his file in case of program error. Extents are protected to the nearest cylinder.
		*SYSFIL = \{ \left(2311 \bigcircle{\capacite	System input and system output (SYSRDR, SYSIPT, SYSLST, SYSPCH) files may be assigned to a 2311, 2314, or both. Specifying either indicates support for both. If MPS=BJF in the SUPVR macro, support is given for foreground logical units when running in batched mode.
			n1 = residual capacity (in records) for beginning of operator notification when SYSLST is assigned to a 2311 or 2314.
			100 ≤ n1 ≤ 65536 If n1 is omitted, 1000 is assumed.
		* Valid when at least 24K ** YES is valid only on a S/ for a S/360 MODEL.	bytes of main storage are available. /370 CPU; YES is the default for a S/370 MODEL. NO is the default

Figure 4. Supervisor Macros (Part 3 of 5)

Name	Macro Description	Parameter = Option	Option Description
FOPT (cont'd)		*SYSFIL (cont'd)	n2 = residual capacity (in records) for beginning of operator notification when SYSPCH is assigned to a 2311 or 2314. 100≤ n2≤65536 If n2 is omitted, 1000 is assumed.
		$ PCIL = \left\{ \frac{NO}{YES} \right\}$	Provides supervisor support for private core image library.
		$JA = \left\{ \frac{NO}{YES} \atop n1, n2, n3 \right\}$	NO defaults to no Job Accounting Interface support. YES specifies basic JA support. (n1,n2,n3) gives additional support to count SIOs issued to I/O devices by partition. n1,n2, and n3 refer to the number of devices in BG, F2, and F1 for which SIOs are to be counted. Choose values for each n from 0 to 255 to specify the number of devices accessed by partition; if any n value is omitted, it defaults to zero.
		$JALIOCS = \left\{ \frac{NO}{(n1, n2)} \right\}$	NO defaults to 16 bytes in the user save area and zero bytes for the alternate label area. Set n1 from 0 to 1024 bytes for the user save area; if omitted, it defaults to 16 bytes. Set n2 from 0 to 224 bytes for the alternate label area (usually =number specified by LBLTYP); if omitted, it defaults to zero bytes.
		OLTEP = $\left\{\frac{NO}{YES}\right\}$	Specify if the on-line testing function is desired. If MODEL= a System/370 CPU, then OLTEP=YES is assumed. OLTEP=YES forces OC=YES.
PIOCS	Describes the system I/O configuration	$SELCH = \left\{ \frac{YES}{NO} \right\}$	Selector channels attached to the system.
		$BMPX = \left\{ \frac{NO}{YES} \right\}$	Burst Mode devices are supported on multiplexor channel. If 1412 – 1419s or 1287 – 1288s are attached to the multiplexor channel, BMPX =YES is not supported.
			Channel switching tape control unit. RWTAU = 2404 or 2804, TSWTCH = 2816.
		TAPE = $\left\{ \frac{NO}{9} \right\}$	Indicates required tape PIOCS support. 9=nine track only, 7=seven or nine track, NO=No tape units attached. NO is the assumed value.
		$MRSLCH = \left\{ \frac{NO}{YES} \right\}$	MICR tape device assigned to a selector channel.
ALLOC	Partitions storage for MPS (optional macro).	F1 =nK, F2 =nK	Specifies storage partitioning MPS, where n must be a multiple of 2. Must be at least 10K if MPS=BJF.
IOTAB	Describes installation requirements for I/O tables.	IODEV = $\left\{\frac{10}{n}\right\}$	Number of I/O devices attached to the system.
		$BGPGR = \left\{\frac{10}{n}\right\}$	Number of symbolic units of the class SYSnnn for the background program.
		$F1PGR = \left\{ \frac{5}{n} \right\}$	Number of symbolic units of the class SYSnnn for F1. Valid only in MPS (minimum 5). Otherwise zero is assumed when MPS=NO.
		$F2PGR = \left\{ \frac{5}{n} \right\}$	Number of symbolic units of the class SYSnnn for F2. Valid only in MPS (minimum 5). Otherwise zero is assumed when MPS=NO.
		CHANQ = $\left\{\frac{6}{n}\right\}$	Number I/O requests in the channel queue. 6 is the minimum value generated. In a supervisor with CBF option specified, the minimum value is 6 plus the number of console buffers generated.
		JIB = $\left\{\frac{5}{n}\right\}$	Number of Job Information Blocks (JIBs) for the system. Requirements are: 1. One JIB for each temporary logical unit assignment. 2. One JIB for each alternate logical unit assignment. 3. One JIB for each open 2311 or 2314 extent with the DASD file protect feature. 4. Two JIBs for each open 2321 extent with the DASD file protect feature.

*Valid when at least 24K bytes of main storage are available .

Figure 4. Supervisor Macros (Part 4 of 5)

Name	Macro Description	Parameter = Option	Option Description
DVCGEN	Specifies I/O devices. Each device type requires a separate DVCGEN macro. (See note 1 forr DVCGEN rules. This is an optional macro.)	CHUN - {X'cuu'} DVCTYP - {xxxxxx} CHANSW = {NO / YES} MODE = {X'ss'}	Specify the hexadecimal number of the channel and unit for the device. Specify the device type. See Figure 29. Specify if the device is attached to more than one selector channel. If it is, the device can be switched. 1. 2400T9. MODE specifies the tape mode. X'C0' is the default value. 2. 2400T7. MODE specifies the tape mode. X'90' is the default value. See Figure 30 for other values. 3. 2702. MODE designates the SADxxx command. X'00' is the default value, X'00' SAD0 X'01' SAD1 X'02' SAD2 X'03' SAD3 4. 2260 (Local). MODE is used to specify the 1053 printer when CHUN = X'cuu' refers to a 1053 attached to a 2848. The operand must be entered as MODE = X'01' 5. 1412/1419. MODE designates the external interrupt bit associated with Magnetic Ink Character Readers. The modes X'01' through X'20' correspond to external interrupt PSW bits 31 through 26 respectively. For the dual address adapter 1419, this parameter is needed for both the 1419P and the 1419S device types. X'01' Device attached to external line 6. X'04' Device attached to external line 6. X'04' Device attached to external line 4. X'10' Device attached to external line 3. X'20' Device attached to external line 2. 6. 1018 Paper Tape Punch with 2826 Paper Tape Control Unit Model 1. This parameter specifies whether or not the Error Correction feature is present: X'00' feature not present X'01' feature present
ASSGN	Sets standard I/O assignments. A separate macro is required for each standard assignment desired. (Optional macro)	$\left\{ SYSxxx,X'cuu',\left\{ \frac{BG}{F1}\right\} \right\}$	SYSxxx is any symbolic logical unit (SYSIPT, SYSLOG, etc.) or programmer logical unit (SYS000, SYS001, etc.). X'cuu' is the hexadecimal number of the channel and unit to which the symbolic device is attached. $\left\{ \begin{array}{l} \underline{BG} \\ \overline{F1} \end{array} \right\} \ \ \text{indicates the specific partition to which the ASSGN is} \\ \left\{ \begin{array}{l} \underline{F2} \end{array} \right\} \ \ \ \text{being made} \ .$
SEND	Indicates end of supervisor generation .	[n]	Specifies the beginning address of the problem program area. An area should be reserved for supervision expansion and maintenance. The parameter is optional. If not specified, no area is reserved beyond the assembled last address of the supervisor.

Note 1: Rules for using DVCGEN

- 1. A separate DVCGEN macro instruction is required for each device.
- 2. The total number of DVCGEN macros must not exceed the total number of devices specified in the IODEV parameter of the IOTAB macro.
- 3. DVCGEN macros must be specified in ascending channel address sequence.
- 4. Switchable units (attached to more than one selector channel) must be defined once. They are defined on the lowest channel on which they are addressable.
- 5. The sequence of the DVCGEN cards determines the priority of the devices on their channel. Switchable units must be the last devices for each channel, and must be on consecutive channels.
- 6. The specifications of these macros may be altered by IPL ADD and DEL statements. See IPL PLM, GY24-5086.
- 7. Rules for SYSxxx:
 - a. The ASSGN macro allows SYSRDR, SYSLST, SYSPCH, and SYSIPT to be assigned to a tape or DASD. However, IPL unassignes any such assignments.
 - b. SYSLOG must also be assigned in BG, if assigned in foreground partition.
 - c. SYSLNK cannot be specified in either foreground partition.

Figure 4. Supervisor Macros (Part 5 of 5)

Macro	Туре	Code Generated	Critical Globals Set
SUPVR	generation	Defines low main storage	BG10 BG25 BG13 BG27 BG14 BG35 BG19 BG36 BG20 BG50 BG21 BG51 BG24 BG100 AG11
CONFG	generation	None	BG1 BG23 BG2 BG39 BG22 BG51 AG12
STDJC	generation	None	BG34 BG81
FOPT	generation	General cancel SVEREG routine General exit Background communication region and extension General entry SVC interrupt handler	BG0 BG60 BG2 BG61 BG4 BG62 BG5 BG71 BG6 BG72 BG7 BG73 BG8 AG2A BG14 AG7 BG15 AG10 BG16 AG13 BG18 AG21 BG26 AG22 BG30 AG23 BG32 AG28 BG33 AG31 BG38 AG32 BG38 AG32 BG40 AG39
PIOCS	generation	None, directly calls inner macros.	BG3 BG11 BG9 BG12 BG10 BG31
SGTCHS	inner	Channel scheduler Start I/O SIO accounting I/O interrupt	none
SGUNCK	inner	Unit check Error recovery exits	none
SGTCON	inner	VLDADR1 subroutine, ATNRTN routine, CCW chain, disk information blocks. error recovery block, SVC interrupt table, PC option table, and OC option table, physical transient save area, IDRA save area, logical transient save area.	none
SGDFCH	inner	Fetch subroutine	none
sgsvc	inner	Supervisor interrupts Program check interrupts External interrupts Console buffering routine	none
SGDSK	inner	Disk error recovery	none
SGTHAP	inner	Track hold, track free, set abnormal exit routine address, and asynchronous processing routines.	none
SMICR	inner	External interrupts for MICR type devices Program checks in stacker select routine Error recovery for test I/O and start I/O	none
ALLOC	generation	None	none

Figure 5. Macro Functions (Part 1 of 2)

Масго	Туре	Code Generated	Critical Globals Set
IOTAB	generation Supervisor table expansions – SYSCLB LUB, PIBs, SVC Interrupt table, channel queue table (CHANQ), PUB, JIB, TEB, and TEBV.		AG2D
LUBGEN	inner	Generates NICL, FICL, and unassigned LUB tables, console buffers, and track hold table entries.	none
DVCGEN	generation	Overlays for PUB table entries.	AG8
ASSGN	generation	Overlays for LUB table entries.	none
SEND	generation	Generates console buffer and PTO patch areas; JAI partition tables, user save area, and label area; OBR/SDR routines. Calls inner macros COMMN for F1, F2, communications regions, COMMNEX for F1, F2, communications region extensions, TRTAB for ASCII translation tables, MCRAS for RMS resident coding and RTA. Defines end of supervisor nucleus, beginning of IDRA, A and B transient areas, start of problem program area, CE area, and BG save area.	none
SMCRR	inner	Machine check recording and recovery record builder.	none
COMMN	inner	Communications regions for all partitions.	none
COMMNEX	inner	Communications region extensions for all partitions.	none
TRTAB	inner	Generates ASCII translation tables.	none
MCRAS	inner	Generates RMS Monitor and RTA.	none
MAPLOWC	inner	Generates equates to address low core for RMS.	

Figure 5. Macro Functions (Part 2 of 2)

<u> Global</u>	On Setting	<u>Purpose</u>
BG O	CE=YES Or n AP=YES AB=YES EU=YES TRKHLD=n ERRLOG=YES Or CLEAR MCRR=YES MICR=1412, 1419 or 1419D JA=YES JA=(n ₁ , n ₂ , n ₃) ASCII=YES MPS=YES OR BJF	Determines the length of the supervisor save area.
BG1	SP=YES	Determines whether the storage protect feature is used.
BG1QT	TP=QTAM	Determines QTAM support.
BG2	TIMER=YES JA=YES JA=(n _{1"} n _{2"} n ₃)	Determines whether the timer feature is used. Does not force BGO.
BG3	CHANSW=TSWTCH or RWTAU	Determines whether channel switching is supported (2816).
BG4	TEB=n	Determines if tape error statistics are to be accumulated and logged.
BG5	PTO=YES	Determines if physical transient overlap option is supported.
BG6	OC=YES OLTEP=YES	Determines if the asynchronous user interrupt key routine is supported. Does not force BGO.
BG7	IT=F1, or F2, or BG	Determines whether the internal timer option is supported. Does not force BGO.
BG8	PC=YES	Determines if the user program check routine is supported.
BG9	CHANSW=RWTAU	Determines whether channel switching is supported (2404, 2804).
BG10	SELCH=YES	Determines whether selector channels are supported.
BG11	BMPX=YES	Determines whether burst mode devices will be supported on the multiplexor channel.
BG12	TAPE=7 or 9	Determines the type of tape support required.
BG13 *	AP=YES	Determines if asynchronous processing is supported. If yes, force on BG0, BG14, BG20.
BG14	WAITM=YES AP=YES	Determines if the wait multiple function is supported. Force on if AP is specified. Does not force on BGO.

Figure 6. Global Settings (Part 1 of 5)

<u>Global</u>	On Setting	<u>Purpose</u>
BG15 *	AB=YES	Determines if user abnormal termination routine is supported. Forces on BG0.
BG16 *	TRKHLD=n	Determines if the track hold function is supported. BG20 must be on (if it is not, it defaults to NO).
BG18	CBF=n	Determines if console buffering option is supported.
BG19 *	MCRR=YES	Determines whether MCRR option is supported.
BG20	MPS=YES or BJF AP=YES	Determines whether multiprogramming support is required. Forces BG0.
BG21	TP=BTAM or QTAM	Determines whether teleprocessing support is required.
BG 22	DEC=YES	Determines if the decimal feature is used. Does not force $\ensuremath{BG0}\xspace$.
BG23	FP=YES	Determines if the floating point feature is used. Does not force ${\tt BG0.}$
BG 24	MPS=BJF	Determines if batched jobs will be run in foreground partitions. Forces BG0.
BG25	ERRLOG=any invalid setting	Indicates ERRLOG is set with an invalid option. Causes a message and terminates supervisor assembly.
BG 26	PCIL=YES	Determines if PCIL is supported.
BG 27	ERRLOG=RDE	Determines if RDE Support is required.
BG30	CCHAIN=YES	Determines if command chaining support for retry on I/O operation is used. Does not force BGO.
BG31	TAPE=9	Determines if 9 track tape support is required.
BG32	DASDFP=n,n	Determines whether the DASD file protect feature is supported. Does not force BGO.
BG33	SYSFIL=2311 or 2314	Determines if logical system I/O units are a disk device. Does not force BGO.
BG34	DATE=MDY	Determines the type of date configuration to be supported.
BG35	MICR=1412, 1419, 1419D, 1270, 1275	Determines if any MICR type device is supported. Forces BGO.
BG36	MICR=1419D	Determines if 1419D (MICR type device with dual address adapter) only is supported. Forces BG0.

Figure 6. Global Settings (Part 2 of 5)

<u>Global</u>	On Setting	<u>Purpose</u>
BG38	OLTEP=YES	Indicates whether OLTEP is supported; forces BG6.
BG39	MODEL=a S/370 CPU	Indicates RMS support for System/370.
BG 40	RETAIN=YES	Indicates RETAIN/370 is Supported.
BG 41	DECK=YES	Job control options.
BG 42	LIST=YES	Job control options.
BG 43	LISTX=YES	Job control options.
BG 44	SYM=YES	Job control options.
BG45	XREF=YES	Job control options.
BG46	ERRS=YES	Job control options.
BG 47	CHARSET=48C	Job control options.
BG 48	DUMP=YES	Job control options.
BG 4 9	LOG=YES	Job control options.
BG 50	EU=YES	Determines if emulator interface is generated. Forces on $\ensuremath{BG0}\xspace$.
BG51	EU=RELOC	Determines if the relocatable version of CS/40 is used. Forces on BG0, BG50.
BG52	IDRA=YES	Indicates whether IDRA is supported.
BG60 *	TEBV=(device,n)	Determines if the Tape Error Statistics by Volume is supported. Does not force BGO.
BG61	TEBV= (DASD, n)	Determines if TEBV Device is DASD. Does not force BGO.
BG62 *	EVA=(rth,wth,n)	Determines if Error Volume Analysis is supported. Does not force ${\tt BG0.}$
BG 7 1	JA=YES or JA=(n _{1"} n _{2"} n ₃)	Indicates whether JAI is supported.
BG 7 2	JA=(n _{1"} n _{2"} n ₃)	Indicates whether count of SIOs is made.
в с7 3	JALIOCS=(n ₁ , n ₂)	Indicates whether JAI label processing is supported.

Figure 6. Global Settings (Part 3 of 5)

If OLTEP is the issuing program, an HIO instruction is issued to the device if there is I/O pending for the device. If MPS=YES was specified during system generation, OLTEP uses SVC 25 to dequeue an unstarted I/O operation to a shared device. The channel queue entry is removed from the channel queue, and in this case an HIO instruction is not executed.

The supervisor returns to the highest priority program ready to run. The device busy flag is reset at this time. Unless SVC 25 is issued by OLTEP or a teleprocessing device, this SVC is ignored and results in cancelation. If OLTEP was a supervisor option and teleprocessing was not, issuing as SVC 25 by a program other than OLTEP results in cancelation.

SVC 26: Validate address limits. The program issuing an SVC 26 is canceled if the PSW protection key does not equal 0. (Only job control and B-transient programs can issue an SVC 26.)

The upper address must be specified in general register 2, and the lower address must be specified in general register 1. The upper address must be within main storage, and the lower address must be higher than the end of supervisor address, or the program is canceled (ERR25). Return is to the interrupted program. No task selection is performed.

With MPS option, the PIK of the program issuing the SVC 26 must equal the storage protection key for both addresses or the program is canceled (ERR25).

With batch operation, SVC 26 is ignored unless storage protection has been specified.

SVC 27: Same as SVC 25, except that SVC 27 cannot be used by OLTEP. It can be used only to halt I/O on a teleprocessing device. The CCB is not dequeued if the CSW has been stored after an HIO command.

SVC 28: Provides return from user's stacker select routine to the MICR external interrupt routine in the supervisor. SVC is optional and causes a cancel if issued at any point other than in a stacker select routine with MICR devices.

SVC 29: Provides supervisory support for the WAITM macro (except for MICR type If WAITM=YES has been specified devices). in the FOPT macro, WAITM coding is generated to load general register 1 with the address of the ECB list name and to issue the SVC 29. However, when MICR type devices are used, SVC 47 is issued to identify the wait on the MICR CCB.

All interrupts are disabled and the CCBs are all checked for the traffic bit. When a CCB is found with the traffic bit posted, SVC 29 returns to the interrupted program.

If all CCBs are checked and no traffic bits are posted, one of two courses is taken:

- With MPS option Cause user to become I/O-bound, disable for I/O interrupts only, and return to task selection.
- Without MPS option Set wait bit in SVC old PSW, disable for I/O interrupts only, and return to interrupted program.

SVCs 30, 31, and 32: Reserved for QTAM. Refer to the QTAM PLM listed in the Preface.

SVCs 33 and 34: Reserved for internal macros COMRG and GETIME, respectively. Their use by other programs results in a branch to EXT01 (see Chart BG).

SVC 35: Protects a track from use by more than one task at a time. A X'FF' is moved to byte 2 of the SVC old PSW to indicate track hold. A requesting task not owning a held track is made inactive and must wait until the track is free. If more than sixteen holds on a track are attempted, the requesting task is canceled.

Exits are to EXCP3 to execute the I/O, or to RESVC if the track is already held. At RESVC, the problem program old PSW is set to execute the SVC 35 again, and a branch to EXT03 is taken for task selection. See Figure 24 for the Track Hold Table.

SVC 36: Frees a track that is held by the task issuing the FREE. An attempt to free a track not owned by the requestor results in cancellation of that task.

Exits on a successful FREE are to EXT03 for task selection, or to the DETACH routine if the FREE was issued by that routine.

SVC 37: Establishes linkage from the supervisor to a problem program abnormal termination (AB) routine. It stores the routine's entry point and save area address in the AB table. (The save area is a 72-byte area in which the old PSW and general registers 0-15 are stored.) Return is to the STXITing program.

SVC 38: Initializes a subtask. The main task's PIB and save area are copied to the subtask's PIB and save area. The subtask's PIB flag is set to X'83' to indicate 'ready-to-run.' Bit 0 of the maintask's R1

is set to 0 to indicate a successful attach, and absolute priority is established for the subtask. A subtask attempting to issue an ATTACH is canceled. Exit is to EXT03 for task selection.

<u>SVC 39</u>: Performs normal termination of a subtask. DETACH may be issued by either the subtask being terminated or by the main task.

The subtask's PIB is set inactive (byte 0 = X'80'), and its ECB (see Figure 34) is posted for termination. This routine calls the free routine to free any tracks held by this subtask, and a waiting task is removed from the wait state. Exit is to EXT03 for task selection.

SVC 40: Used for intertask communication. POST may be issued by either a maintask or a subtask. It is issued so that a task is aware of the termination of an event. Normal completion of the specified event is posted in the ECB (byte 2, bit 0 = 1). If the SAVE= parameter is present, only the task waiting for this ECB is taken out of the wait state; otherwise, all waiting tasks are removed from the wait state. Exit from this routine is to EXTO3 for task selection.

SVC 41: Informs the system that a resource (shared data area) is now available for use by another task. A task may issue the DEQ macro only to a resource that it currently owns. If it attempts to issue the DEQ macro to some other resource, the task is canceled.

If any other tasks are waiting for the resource, the highest priority task ready to run is removed from the wait state and gains control. If no other task is waiting for the resource, control returns to the task that issued the DEQ.

If a task terminates without DEQuing all of its ENQued resources, either in its normal coding or in its abnormal termination exit routine, any task subsequently attempting to ENQ the resource is canceled. See Figure 35 for the Resource Control Block (RCB).

Normal exits are to EXT01 or EXT03.

SVC 42: ENQ prevents tasks from simultaneous manipulation of a shared data area (resource). This is accomplished, using the TS instruction, by setting to ones all bits of byte 0 of the specified resource control block (RCB). Then the event control block (ECB) address is placed in bytes 4-7 of the RCB.

A task attempting to ENQ a resource that is already engueued by another task is

placed in a queue and put in a waiting condition. The old PSW is set to reexecute the SVC 42 and task selection is performed.

A task is canceled if it attempts to nest ENQ(s) of a resource or if it attempts to ENQ a resource that is still owned by a terminated task.

When a task is finished with a resource, it should inform the system by issuing the DEQ macro. If it does not, tasks subsequently requesting that resource are canceled. See Figure 35 for the Resource Control Block.

SVC 43: Supplies supervisory support for the creation and updating of SDR records for devices not explicitly supported by the The address of the compressed SDR record area must be supplied in general register 1 before the SVC is issued. The SDR record area must be 22 bytes long: 2 bytes reserved for the SDR processor, 1 byte initialized to zeroes, and a 19 byte SDR record with the 16 error counters compacted to 8 bytes. The SVC 43 causes a branch to the SDRSDR routine in the supervisor to complete processing of the record. Immediately following the SVC, the WAIT macro must be issued on the address in register 1.

Example:

LA 1,SDRAREA SVC 43 WAIT (1) or SDRAREA

This SVC is available only with the I/O Error Logging option (ERRLOG). See Chart 08 for the SDRSDR update routine.

SVC 44: Supplies supervisory support for external creation of OBR records for devices not explicitly supported by the system. The address of the OBR record area must be supplied in general register 1 before the SVC is issued. The OBR record area must be 83 bytes long: 2 bytes reserved for the OBR processor, 1 byte initialized to zeroes, and an 80 byte OBR record. The SVC 44 causes a branch to the SDROBR routine in the supervisor to write the OBR record. Immediately following the SVC, the WAIT macro must be issued on the address in register 1.

Example:

LA 1, OBRAREA SVC 44 WAIT (1) or OBRAREA

This SVC is available only with the I/O Error Logging option (ERRLOG). See Chart 08 for the SDROBR update routine.

SVC 45: Provides emulator interface for CPU Models 30 and 40, or System/370 models. On System/370, this SVC serves two purposes:

- 1. When register 1 contains zero, SVC 45 sets communication region byte 134, bit 1 on, indicating that the emulator is active.
- When register 1 contains a PUB address, SVC 45 switches the parity bit in the PUB.

SVC 46: Provides OLTEP with the facility to operate in the supervisory state. In the initial issuing of the SVC, register 1 contains an entry point in OLTEP. The next time the SVC is issued, register 1 is zeroed out, forcing task selection.

SVC_47: Provides identification to the supervisor for MICR type device waits. The SVC results in exiting to task selection (EXT03) rather than reissuing the SVC (RESVC) as is done when SVC 29 is issued.

SVC 48: Reserved for future use.

SVC 49: Reserved for future use.

SVC 50: Reserved for LIOCS error recovery.

SVC 51: Provides OLTEP with the ability to find the length of a core image library without loading the phase. Registers 0 and 1 must be initialized before issuing SVC 51. Register 0 must be pointed at a twelve-byte save area for the phase header, and register 1 must be pointed at the

The first 12 bytes eight-byte phase name. of the phase header are moved to the save area. The save area is not altered if the phase is not in the core image library. If any program except OLTEP issues an SVC 51, that program is canceled.

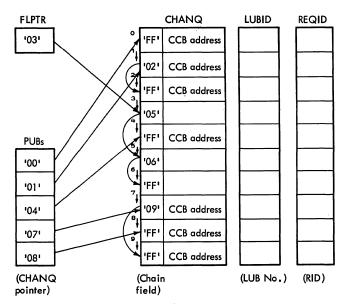


Figure 32. Example of the CHANQ Table Operation

SVC 52: Provides an interface between the supervisor and \$\$BEOJ4. SVC 52 allows the forced dequeuing of channel queue entries that belong to devices assigned to the partition or task that is being canceled or has reached end-of-job.

	SVC		Emphis	
Macro Supported	Dec.	Hex.	Function	
EXCP	0	0	Execute channel programs.	
FETCH	1 2 3	1 2 3	Fetch any phase. Fetch a logical transient (B – transient). Fetch or return from a physical transient (A – transient).	
LOAD	4	4	Load any phase.	
MVCOM	5	5	Modify supervisor communications region.	
CANCEL	6	6	Cancel a problem program or task.	
WAIT	7	7	Wait for a CCB or TECB.	
	- 8	8	Transfer control to the problem program from a logical transient (B-transient).	
LBRET	9	9	Return to a logical transient (B – transient) from the problem program after an SVC 8 .	
SETIME	10*	Α	Set timer interval.	
	11 12	B C	Return from a logical transient (B – transient). Logical AND (Reset) to second job control byte (displacement 57 in communi-	
	13	D	cations region). Logical OR (Set) to second job control byte (displacement 57 in communications region).	
EOJ	14	E	Cancel job and go to job control for end of job step.	
	15	F	Same as SVC 0 except ignored if CHANQ table is full. (Primarily used by ERP).	
STXIT (PC)	16*	10	Provide supervisor with linkage to user's PC routine for program check interrupts.	
EXIT (PC)	1 <i>7</i> *	11	Return from user's PC routine.	
STXIT (IT)	18*	12	Provide supervisor with linkage to user's IT routine for interval timer interrupts.	
EXIT (IT)	19*	13	Return from user's IT routine.	
STXIT (OC)	20*	14	Provide supervisor with linkage to user's OC routine for external or attention interrupts (operator communications).	
EXIT (OC)	21*	15	Return from user's OC routine.	
	22*	16	The first SVC 22 seizes the system for the issuing program by disabling multi- program operation. The second SVC 22 releases the system (enables multiprogram operation).	
	23*	17	Load phase header. Phase load address is stored at user's address.	
SETIME	24*	18	Provide supervisor with linkage to user's TECB and set timer interval.	
	25*	19	Issue HALT I/O on a teleprocessing device, or HALT I/O on any device if issued by OLTEP. For a MPS=YES system, dequeue an unstarted OLTEP I/O request to a shared device.	
	26* 27*	1A 1B	Validate address limits. Special HIO on teleprocessing devices.	

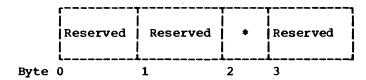
^{*=}Optional

Figure 33. DOS Supervisor Calls (Part 1 of 2)

Macro Supported	SVC		<u> </u>
	Dec.	Hex.	Function
EXIT (MR)	28*	1C	Return from user's stacker select routine (MICR type devices only).
	29*	1D	Provide return from multiple wait macros WAITF and WAITM (except MICR type devices).
QWAIT	30*	1E	Wait for a QTAM element.
QPOST	31*	1F	Post a QTAM element.
	32 33 34	20 21 22	(Reserved). Reserved for internal macro COMRG. Reserved for internal macro GETIME.
HOLD	35*	23	Hold a track for use by the requesting task only.
FREE	36*	24	Free a track held by the task issuing the FREE.
STXIT (AB)	37*	25	Provide supervisor with linkage to user's AB routine for abnormal termination of a task.
ATTACH	38*	26	Initialize a subtask and establish its priority .
DETACH	39*	27	Perform normal termination of a subtask. It includes calling the FREE routine to free any tracks held by the subtask.
POST	40*	28	Inform the system of the termination of an event and ready any waiting tasks.
DEQ	41*	29	Inform the system that a previously enqueued resource is now available.
ENQ	42*	2A	Prevent tasks from simultaneous manipulation of a shared data area (resource).
	43* 44* 45* 46* 47* 48 49 50	2B 2C 2D 2E 2F 30 31 32 33	Provide supervisor support for external creation and updating of SDR records. Provide supervisor support for external creation of OBR records. Provide emulator interface. Provide OLTEP with the facility to operate in supervisory state. Provide return from wait multiple WAITF for MICR type device. (Reserved) (Reserved) Reserved for LIOCS error recovery. Return phase length at OLTEP request.
	52*	34	Provide an interface between supervisor and end-of-job routines.

^{* =} optional

Figure 33. DOS Supervisor Calls (Part 2 of 2)



*Byte 2

Bit 0: Turned on (X'80') at normal termination of subtask.

Bits 0 and 1: Turned on (X°c0°) if the subtask is abnormally terminated.

Bits 2-7: Reserved.

Note: Other blocks that may be used as ECBs are CCBs, TECBs, and MICR CCBs since posting is done in bit 0 of byte 2 of the block.

Figure 34. Event Control Block (ECB)

İ	*	Unused	**	ECB Address of Current Resource Owner
	х	ххх	Х	xxx
Byte	0	1 2 3	4	5 6 7

*Byte 0: Availability byte - All ones when resource is in use.
- All zeros when not in use.

**Byte 4: Flag byte: Bit 0 = 1, another task waiting for the resource.
= 0, no other task waiting for the resource.

Note: The address of the RCB is passed in register 1.

Figure 35. Resource Control Block (RCB)

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by TNL GN33-8692

	lytes ——	Count	Transmission Information	CSW Status Bits		Sym Add		leserved for logical IOCS	CCW Address	Reserved for Physical IOCS 12	CCW Address in CSW	Optional Sense CCW
	Jsed for ———————————————————————————————————	Residual Count	Transmitting Information Between Physical IOCS and Problem Program	(Note 1) Byte 4 BIT DESIGNATIO 32 Attention 33 Status modifier 34 Control unit er 35 Busy 36 Channel end 37 Device end 38 Unit check 39 Unit exception	40 Program - con interruption and 41 Incorrect ler 42 Program chee 43 Protection cl 44 Channel date 45 Channel con	Repre-	Becimal Butter offer Offset: SCII Input Tapes 100'-X'63' SCII Output 1pes Fixed: 100' ariable: X'00' or X'04'	Address of CCW Associated with this CCB	X'80'-CCB being	Address of CCW in the CSW Stored of Channel End, or Address of the Channel Appendoge Routine for Teleprocessing Devices	8 Bytes Appended to the CCB when Sense Information is Desired	
		Traffic Bit (Wait)	End - of - File (/* or /&) 3211- UCSB Parity Check (Line Complete) (Note 2)	Unrecoverable I/O Error	Accept Unrecoverable I/O	Return DASD Data Checks 2671 errors, or 1017/1018 errors to the user	Post at Device End (Note 5)	Return Tape R Data Check, Data Check, or 2520 Equip Check, DASI Data Checks Read or Verif Command, or Passback Req (Notes 3 &	1018 2540 User Err On Routine on fy 3211 uested 6)			
	Bits Bet On By	PIOCS	l PIOCS	PIOCS	3 Pr. Pr.	Pr. Pr.	5 Pr. Pr.	Pr. Pr.	7 Pr. P			
					Byte					•		
		DASD – Data Check in Count Area MICR – SCU Not Operational 1285/1287/1288 Data Check 3211– Print Check/ Equipment Check	DASD - Track Overrun MICR - Intervention Required 1285/1287 - Keyboard Correction in Journal Tape Mode 1017 - Broken Tape 3211 - Print Quality/ Equipment Check	DASD - End of Cylinder MICR - (Note 4) 1287/1288 - Hopper Empty in Document Mode 3211 - Line Position Error (Note 7)	2540, 2520 - Equipment Check Tape - Read Data Check DASD - Any Data Check 1285/1287 Equipment Check 1017/1018 Data Check 3211 - Print Check/ Data Check	Non - Recovery Questionable Condition: Card - Unusual Command Sequence DASD - No Record Found 1285/1287/1288 - Document Jam or Torn Tape 3211 - UCSB Parity Check (Command Retry)	No -Record - Found Conditi (Retry on 2311 2314, or 2319	, Overflow or	the next (to be executed)	ccw		
	Bits —	0	1 1	2	3	4	5	6	7	!		
5	Set On By—	PIOCS PIOCS = Physical		PIOCS	PIOCS	PIOCS	Pr. Pr.	PIOCS	Pr. Pr	• 1 .		

Pr. Pr. = Problem Program

Note 1. Bytes 4 and 5 contain the status bytes of the Channel Status Word (Bits 32 - 47). If byte 2, bit 5 is on and device end results as a separate interrupt, device end will be ORed into CCB byte 4.

Note 2. Indicates /* or /& statement encountered on SYSRDR or SYSIPT. Byte 4, bit 7 (unit exception) is also on.

Note 3. DASD data checks on count not returned.

Note 4. For 1255/1259/1270/1275/1412/1419, disengage. For 1275/1419D, I/O Error in external interrupt routine (channel data check or busout check).

Note 5. The traffic bit (Byte 2, bit 0) is normally set on at channel end to signify that the I/O was completed. If byte 2, bit 5 has been set on, the traffic bit and bits 2 and 6 in byte 3 will be set on at device end. Also see Note 1.

Note 6. 1018 ERP does not support the Error Correction Function.

Note 7. This error occurs as an equipment check, data check, or FCB parity check.

Byte Bit Name Field

0	1	2	3	4		5	
0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15	16 17 18 19 20 21 22 23	24 25 26 27 28 29 30 31	32 33 34 35 36	37 38 39	40 41 42 43 44 45 46 47	
Command Code		—— Data Address ——		Flags	0 0 0	(Ignored)	
Α		В	С	D	E		

FIELD	NAME	DESCRIPTION
A	Command Code	Bits 0-7: Specify the operation to be performed. (See Part 2 of this Figure)
В	Data Address	Bits 8-31: Specify the location of a byte in main storage. It is the first location referred to in the area designated by the CCW.
С	Flags	Bits 32–36: Specify the flag bits used in conjunction with the CCW,
		Bit 32- Chain-Data (CD) causes the address portion of the next CCW to be used with the current CCW.†Note
		Bit 33- Chain-Command (CC) causes the command code and data address of the next CCW to be used. The chain data flag (bit 32) takes precedence over this flag.
		Bit 34– Suppress Length Indication (SLI) causes a possible incorrect length indication to be suppressed. The chain data flog (bit 32) takes precedence over this flog.
		Bit 35- Skip (SKIP) suppresses the transfer of information to main storage.
		Bit 36– Program Control Interruption (PCI) causes the channel to generate an interrupt when the CCW is fetched.
D	Reserved	Bits 37-39: (Must contain zeros)*
Ē	Ignored	Bits 40–47: Not checked
F	Count	Bits 48-63: Specify the number of bytes in the operation

^{*}The transfer in channel command (TIC) is the one exception to this statement. †Note: Chain data cannot be done on 360/30 if a highspeed device is being used. Example - 2311,2400 Model 3.

Figure 38. Channel Command Word (CCW) (Part 1 of 2)

	6						7								
48	48 49 50 51 52 53 54 55						55	56	57	58	59	80	61	62	63
•	Count —								•						
	F														

•	10-CHARACTER				
(IN HEX)	MESSAGE	ERROR			
08	C'INTERV REQ'	OPERATOR INTERVENTION REQUIRED			
j 09	C'BUSOUT CHK'	BUS OUT CHECK			
10	C'EQUIP CHK '	EQUIPMENT CHECK			
j 11	C'DATA CHECK'	DATA CHECK			
12	C'VERIFY CHK'	VERIFY CHECK			
13	C'ADDR MRKER'	MISSING ADDRESS MARKER			
	C'OVERRUN '	OVERRUN			
15	C'SEEK CHECK'	SEEK CHECK DATA CHECK IN COUNT FIELD			
16	C'DTA CHK CT'				
17	C'FILE PROT '	VIOLATED FILE PROTECTION			
	C'COMM REJCT				
		UNDETERMINED ERROR			
		ERROR DURING RECOVERY ATTEMPT			
	C'NRF-MADDMK'				
		BALLAST CELL ACCESSED ON 2321			
	C'BLNK STRIP'				
		I/O PROGRAM CHECK			
	C'PROT CHECK'				
		SEEK ADDRESS NOT VALID			
		DEVICE IN ERROR NOT RECOGNIZED			
		CHANNEL DATA CHECK			
		BACKSPACE INTO LOADPOINT			
	C'CONVRT CHK'				
		DEVICE NOT OPERATIONAL			
		NONCOMPATIBLE TAPE ON DRIVE			
		PARITY ERROR IN PRINTER BUFFER			
	C'BCH NM OFF'				
	C'NON RECOV	NON-RECOVERY ON 1285			
1 36	C'NO REC FND	NO RECORD FOUND			
37	C'DISEN FAIL	DISENGAGE FAILURE ON MICR			
38	C'INVLD FONT'	INVALID FONT ON 1287 IN DOCUMENT MODE			
		POSITION CHECK ON 2495 TCR			
		BROKEN TAPE ON 1017 BUFFER LOAD CHECK ON 3211			
41	C'LOAD CHECK'	BUFFER LOAD CHECK ON SZII			

Figure 46. Physical Transients Error Messages

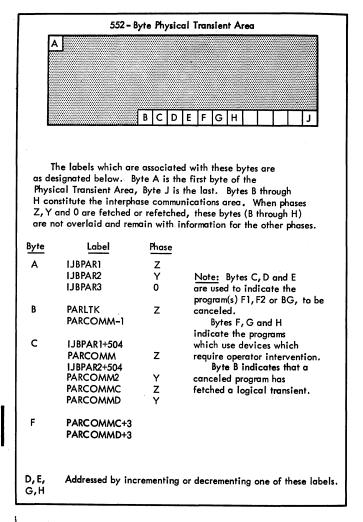


Figure 47. Interphase Communication Area (For A-Transients \$\$ANERRZ, Y, and 0)

1403-1443 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one retry--take equipment error exit (initial selection: cancel, retry. Channel end: cancel, retry, ignore).

Message: OP28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Take equipment error exit
(cancel, ignore).

Message: OP10 EQUIP CHK.

• Byte 0, Bit 5--Code General Storage Parity Error (1403 only)

Action: Take equipment error exit (cancel). UCS buffer must be reloaded.

Message: OP33 UCB PARITY.

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention exit.

Message: OPO8 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: If initial selection, one retry; otherwise, take equipment error exit (initial selection: cancel, retry. Channel end: cancel, retry, ignore).

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 7--Channel 9

Action: Post CCB, take continue exit.

Note: This test is main storage resident.

• Byte 0, Bit 0--Command Reject

Action: If command code is UCS enable or inhibit data check, take continue exit; otherwise, take program check exit. This procedure allows UCS-oriented programs to operate on non-UCS hardware.

Message: OP18 COMM REJCT.

Byte 0, Bit 4--Data Check (1403 Only)

Action: Take equipment error exit (cancel, ignore).

Message: OP11 DATA CHECK.

3211 PRINTER ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one retry--take equipment error exit (initial selection: cancel, retry. Channel end: cancel, retry, ignore).

Message: OP28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Check the following bits of sense byte 1 in the order indicated; if a bit is on when tested, the system takes the action indicated in the discussion of these bits.

Bit 0, Command retry Bit 1, Print check Bit 2, Print quality Bit 3, Line position

Bit 6, Mechanical motion

If none of the preceding conditions occurred, then a transparent sync check or a train overload condition occurred.

Action: Provide information type message and continue processing.

Message: OP10 EQUIP CHK.

• Byte 0, Bit 2--Bus Out Check

Action: Provide an intervention required message. The operator should then make the device ready to continue processing.

Message: 0P09 BUSOUT CHK.

• Byte 0, Bit 4--Data Check

Action: Check the following bits of sense byte 1 in the order indicated; if a bit is on when tested, the system takes the action indicated in the discussion of these bits.

Bit 1, Print check Bit 3, Line position If neither of the preceding conditions has occurred, take the following action:

Action: Provide information, type message, and take cancel exit. (Permanent error.)

Message: OP11 DATA CHK.

• Byte 0, Bit 5--Buffer Parity Check

Action: First, check the following bits of sense byte 1 in the order indicated; if a bit is on when tested, the system takes the action indicated in the discussion of these bits.

Bit 1, Print check Bit 3, Line position

If neither of the preceding conditions has occurred, the system attempts to read the contents of the 3211 buffers. If the attempt is successful, take the following action:

Action: Provide an information message. If a user routine is available, then go to it; otherwise, continue processing.

If the attempt to read the contents of the 3211 buffers is not successful, take the following action:

Action: Provide a message that allows the operator to respond IGNORE or CANCEL.

For equipment checks, the operator must examine the sense information for the intervention required bit along with the equipment check. If intervention is required, the operator must make the device ready.

Message: OP33 BUF PARITY.

• Byte 0, Bit 0--Command Reject

Action: Provide information, type message, and take cancel exit. (Permanent error.)

Message: OP18 COMMREJCT.

• Byte 0, Bit 6--Load Check

Action: An error condition occurred when either the UCSB or the FCB was loaded. Provide information, type message, and take cancel exit. (Permanent error.)

Message: 0P41 LOAD CHECK.

• Byte 0, Bit 1--Intervention Required

Action: First, sense byte 1, bit 4 is tested for a forms check; if the bit is on, the action indicated in the discussion for this bit is taken. Otherwise, an interlock condition has occurred on the 3211. The probable causes are:

Gate not latched Train not positioned Stop key active Vacuum low Train overload

Action: Provide an intervention required message. The operator should then make the device ready to continue processing.

Message: 0P08 INTERV REQ.

• Byte 1, Bit 0--Command Retry

Action:

- For message OP10, a print line buffer parity check occurred. The recovery procedure depends upon the user's error option for Command Retry (CCB byte 2, bit 5).
 - If the Command Retry option is specified, reissue the failing CCW. If the retry is unsuccessful, the error is considered uncorrectable. Provide information, type message, and take cancel exit. (Permanent error.)
 - b. If the Command Retry option is not specified, issue a "Skip to channel 0" (X'38') command to allow the carriage to perform the suppressed command. Provide information, type message, and take cancel exit. (Permanent error.)
- For message OP33, a UCSB parity check occurred.

Action: This action depends upon the user's error routine to reload the

UCSB. After the UCSB is reloaded, reissue the failing CCW. If the retry is unsuccessful, the error is considered uncorrectable. Provide information, type message, and take cancel exit. (Permanent error.)

• Byte 1, Bit 1--Print Check

<u>Action</u>: For message 0P10, a print check occurred for one or more of the following reasons:

Hammer fire check Sync check Coil protection

For message OP11, a print check occurred because of an unprintable character. In response to either message, do the following:

Provide a message that allows the operator to respond IGNORE or CANCEL. If the response is CANCEL, go to the user's error routine if available.

For equipment checks, the operator must examine the sense information for the intervention required bit along with the equipment check. If intervention is required, the operator must make the device ready.

• Byte 1, Bit 2--Print Quality

Action: A print quality check occurred because the platen failed to advance or retract, or excessive ribbon motion and/or ribbon skew was detected. Provide a message that allows the operator to respond IGNORE or CANCEL. If the response is CANCEL, go to the user's error routine if available.

For equipment checks, the operator must examine the sense information for the intervention required bit along with the equipment check. If intervention is required, the operator must make the device ready.

• Byte 1, Bit 4--Forms Check

<u>Action</u>: A forms check occurred for one of the following reasons:

The Carriage Detent Switch is off.
The paper is jammed or the forms are
torn.

The 3211 is out of paper. The stacker is full.

Provide an intervention required message. The operator should then make the device ready to continue processing.

• Byte 1, Bit 6--Mechanical Motion

Action: Provide information, type
message, and take cancel exit.
(Permanent error.)

Note: When certain 3211 errors occur, additional information is provided to the user by turning on bits in the user's CCB. These errors and bit settings are indicated in Figure 37.

1442 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one retry; then take equipment error exit (cancel, retry). If data transfer, take operator intervention exit.

Message: OP28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Take operator intervention

exit.

Message: OP10 EQUIP CHK.

• Byte 0, Bit 1--Intervention Required

<u>Action</u>: Take operator intervention exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: If initial selection, do one retry; then take equipment error exit (cancel, retry). If data transfer, take operator intervention exit.

Message: OP09 BUSOUT CHK.

• Byte 0, Bit 4--Data Check

Action: Take operator intervention
exit.

Message: OP11 DATA CHECK.

• Byte 0, Bit 5--Overrun

Action: Take operator intervention
exit.

Message: 0P14 OVERRUN.

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: 0P18 COMM REJCT.

• CSW Bit 47--Chaining Check

Action: Take operator intervention

exit.

Message: OP14 OVERRUN.

2501, 2520, 2540 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

Action: If initial selection, one retry; then take equipment error exit (cancel, retry). If read data transfer, take operator intervention exit. If punch data transfer, one retry; then take equipment error exit (cancel, retry).

Message: 0P28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Reader--Take operator intervention exit. Punch--CCB option. Take equipment error exit (cancel, ignore). For 2520, Byte 0, Bit 7 indicates punch check.

Message: OP10 EQUIP CHK.

• Byte 0, Bit 1--Intervention Required

Action: Take operator intervention

exit.

Message: 0P08 INTERV REQ.

• Byte 0, Bit 2--Bus Out Check

Action: One retry; then take equipment error exit (cancel, retry). If the device is a 2520, do not retry if this is not initial selection (cancel, retry).

Message: 0P09 BUSOUT CHK.

 Byte 0, Bit 4--Data Check (Cannot occur on a 2520 punch)

 $\underline{\underline{Action}}$: Take operator intervention exit.

Message: OP11 DATA CHECK.

 Byte 0, Bit 5--Overrun (Cannot occur on 2540 or 2520 punch)

Action: Take operator intervention

exit.

Message: 0P14 OVERRUN.

• Byte 0, Bit 0--Command Reject

Action: Take program check exit.

Message: 0P18 COMM REJCT.

• Byte 0, Bit 6--Unusual Command Sequence (2540 read only)

Action: Post CCB--take continue exit.

• CSW Bit 47--Chaining Check (2501, 2520 read only)

<u>Action</u>: Take operator intervention exit.

Message: OP14 OVERRUN.

2671 ERROR RECOVERY

• CSW Bit 44--Channel Data Check

<u>Action</u>: If initial selection, one retry. Take equipment error exit (cancel).

Message: OP28 CHAN DTCHK.

• Byte 0, Bit 3--Equipment Check

Action: Test CCB for ignore option (byte 2, bit 4) and if on, turn on byte 3, bit 1 of the CCB and take equipment error exit (cancel, ignore, retry). Otherwise, take operator intervention exit.

Message: OP10 EQUIP CHK.

Note: When an equipment check occurs, reposition the paper tape to the beginning of the record in error to perform the retry operation. The

The RMS (Recovery Mangement Support) is an automatic DOS feature for IBM System/370. RMS gathers information about hardware reliability and attempts certain error recovery operations. It is part of the entire RAS (reliability, availability, and serviceability) support for System/370.

RMS is supervisor generated and is composed of two functions:

- MCAR (Machine Check Analysis and Recovery) and
- CCH (Channel Check Handler).

However, RMS is not a supervisor option. It is generated automatically for System/370 at SYSGEN. The CONFG macro sets global BG39 when MODEL option shows a System/370 CPU. Figure 54 gives the overview of the RMS function in DOS.

MCAR FUNCTION

MCAR responds to machine check interrupts and attempts recovery. It logs error data on ERDS (Environmental Recording Data Set) on the Recorder File. It provides operator messages via SYSLOG.

When a machine check occurs, MCAR first logs the error, then retries the failure by CPU retry and ECC (Error Correction Code). If successful, a <u>soft MCI</u> (machine check interrupt) message occurs, signifying recovery from a machine check.

If hardware retry is unsuccessful, MCAR determines machine check severity through recovery transient analysis and records pertinent data on SYSREC. RMS controls the recording of data through the EFL (Error

Frequency Limit) feature of operating in Quiet or Recording mode. See the MODE Command section.

Hard MCI occurs when:

- CPU retry is unsuccessful, or
- Interrupted instruction cannot be retried, or
- Storage failure is permanent.

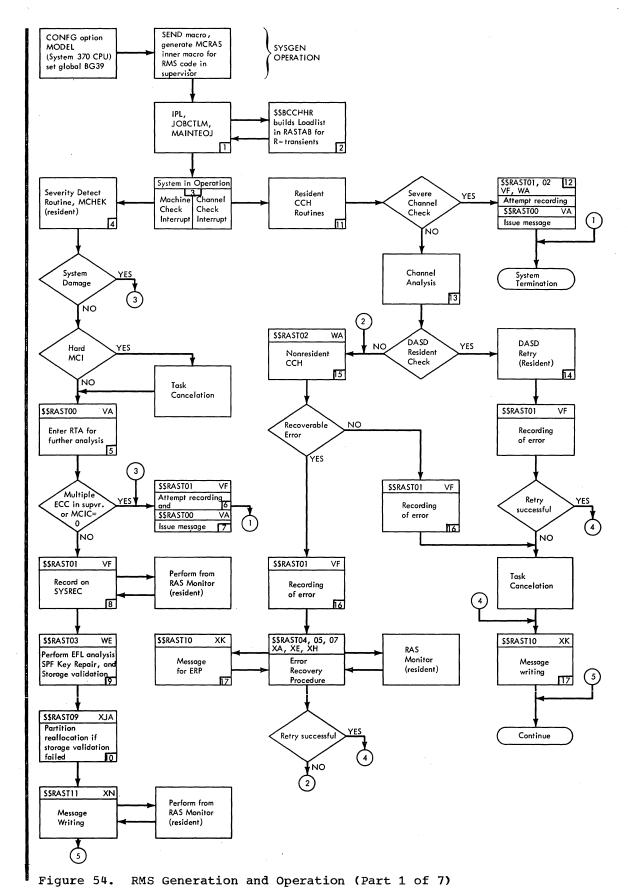
In event of a hard MCI, execution of the affected task stops. MCAR assesses damage and continues system operation when possible. It selectively terminates the affected partition. RMS records a full Damage Report on the Recorder File.

The system enters the hard wait state when a hard MCI:

- Interrupts supervisor coding
- Occurs while accessing critical information or phases from SYSRES, or
- Damages privileged coding through permanent storage error

MCAR attempts to notify the operator about:

- Machine check type
- 2. Wait state, re-IPL
- 3. Problem program termination
- 4. MODE operation change
- 5. Buffer deletion



,

1 A test is made during IPL to determine if RMS support has been included in the supervisor. If RMS support has been generated, a test is made to determine if the CPU is a S/360 or S/370 model.

If the system has been IPLed from a $S/360_w$ code to simulate the actions of a S/360 is moved into the machine check and channel check routines. A message is issued to notify the operator that no RMS support exists.

If the CPU is a S/370 model, \$\$BCCHHR is called.

The primary function of the transient \$\$BCCHHR is to scan the core image directory for all transients whose names begin with '\$\$RAST' and build a directory in storage for these transients. This directory (Load List) is located in the RAS table where a fullword is reserved for the CHR (Channel, Head, Record) of each RAS phase. The low-order three bytes of each fullword contains the CHR while the high order byte is reserved for switches and flags. Currently twelve fullword entries exist and occupy the first 48 bytes in the RAS table.

All RAS transients have the following format for their names:

\$\$RASTnn, where nn is a decimal number from 00 to 11. The last two digits in each phase name are used as the index to the RAS table load list. Multiplying this number by four and adding the product to the RAS table address produces the address for the particular entry.

Another function of \$\$BCCHHR is to determine whether the recorder file is a 2311 or 2314 disk and place the number of records per track and tracks per cylinder in the RAS table at EOR and EOT, respectively. This information is needed by \$\$RAST01 for the disk (SYSREC) address updating procedure. The channel addresses of the devices to which SYSRES and SYSREC are assigned are placed in the RAS table at RASRES and RASLOG, respectively.

3 When a hardware failure occurs, CPU Retry hardware attempts to re-execute the operation.

If the outcome of the retry is successful, a recoverable machine check is indicated, a logout is made to the CPU logout area, and a machine check interrupt is taken.

If the outcome of the retry is unsuccessful, an unrecoverable machine check is indicated, a logout is made to the CPU logout area, and a machine check interrupt is taken.

A channel error is detected when a CSW is stored with either the interface control check or channel control check bit on. Thus, the logging is done both at I/O interruption time and CC1 time to an I/O instruction under control of CR14 bit 2. A channel error does not cause a machine check interrupt on the Model 145 but does cause a machine check interrupt on the Model 155.

Figure 54. RMS Generation and Operation (Part 2 of 7)

- 4 The severity detect routine for machine checks categorizes errors into four classes:
 - System damage bit on in MCIC, AMWP bits in machine check old PSW invalid; processing damage to privileged code.

Action: Give hard wait message and terminate system.

Processing damage affected nonprivileged coding; machine check old PSW not completely valid.

Action: Cancel damaged task and exit to EXT02.

3. Recoverable machine check occurred in privileged code.

<u>Action</u>: Schedule recovery report and return to interrupted code via old PSW.

4. Recoverable machine check occurred in nonprivileged code.

Action: Schedule recovery report, and exit to EXT02.

- Class 1 The C'A' is posted in location LOWCORE, C'S' is posted in location LOWCORE+1, and RAS ACTIVE and EMEXIT bits are posted in location LD00SLOT.
- Class 2 The task is canceled and the MCACT and RAS ACTIVE bits are posted in location LD00SLOT.
- Class 3 The RAS ACTIVE and MCACT bits are posted in LD00SLOT.
- Class 4 The RAS ACTIVE and MCACT bits are posted in location LD00SLOT.
- 5 Transient \$\$RAST00 analyzes the codes stored at locations LD00SLOT and LOWCORE.

If the EMEXIT bit is on, the system will eventually be terminated. If a C'A" is posted at LOWCORE, \$\$RAST01 is fetched to build and record machine check records and post the SYSTERM bit in LD00SLOT. \$\$RAST00 is then fetched again to log an appropriate message regarding the recording status and terminate the system. If a C"B" is posted at location LOWCORE, no recording is attempted and the system is terminated.

When neither the EMEXIT or SYSTERM bits are on in LD00SLOT, a further test is made to determine if multiple ECC errors have occurred in the supervisor.

Multiple ECC errors in the supervisor cause a Hard Wait condition. A C'A' is posted in location LOWCORE, SEREP code C'S' is posted in LOWCORE+1, the EMEXIT bit is posted in LD00SLOT, and \$\$RAST01 is fetched.

Figure 54. RMS Generation and Operation (Part 3 of 7)

6 Transient \$\$RAST01 attempts to build the machine check records and record them on SYSREC. A code is posted in LOWCORE+2 to indicate the status of the recording effort.

C'A'=recording was attempted but failure occurred on first record.

C'I'=recording was incomplete but at least one record was successfully written on SYSREC.

C"S'=recording of all records was successful.

The SYSTERM bit is posted in LD00SLOT, and \$\$RAST00 is fetched again.

- 7 \$\$RAST00 tests LD00SLOT, finding both the SYSTERM and EMEXIT bits on, it attempts to issue an OT11I Hard Wait message regarding the recording status and then to terminate the system.
- 8 If multiple ECC errors are found in the Problem Program or no ECC errors are found, \$\$RAST01 is fetched.

Other codes stored by \$\$RAST01 at LOWCORE indicate a channel error.

<u>Code</u>	<u>Meaning</u>
В	Irrecoverable channel check on fetch
С	Channel check on log with RASMSG
D	ECSW not stored
E	ERPIB queue has been exhausted
F	2 channels damaged at some time
G	System reset code in ECSW
Н	Retry/reset codes invalid
I	Channel address invalid
\$\$RAST01 bu	ilds machine check records and records them on SYSREC.

Figure 54. RMS Generation and Operation (Part 4 of 7)

9 For the Model 155, ECC/EFL analysis is done by simply checking if a specified error count has been reached within a specified time limit, whereupon a diagnose instruction is used to place the machine in quiet mode. 155 HIR/EFL analysis is done in a similar manner to that of ECC/EFL, but instead of using a diagnose command to switch from full recording to quiet, control register 14 is loaded with bit 4 off.

145 HIR/EFL analysis is identical to that of the Model 155. 145 ECC/EFL analysis differs from the Model 155 to the extent that control storage analysis is necessary, and the EFL is initially set to 16 single bit errors in eight hours rather than eight errors in eight hours. On the occurrence of a single bit error while in control storage threshold mode, a message is issued, via the hardware facility, to indicate that control storage is in quiet mode.

In all Model 155 and 145 analyses, the mode status is posted in a one byte location in the RAS table called MCMODE. The eight bit configuration of the byte is as follows:

Bit	Λ	нтр	recording mode
DIC	o .		
	1		quiet mode
	2	ECC	recording mode in main storage
	3	ECC	quiet mode in main storage
	4	ECC	recording mode in control storage
	5	ECC	quiet mode in control storage
	6	ECC	threshold mode in control storage
	7	Not	used

The following tests are made before storage validation (moving a doubleword of ones and zeros into the failing storage address) is attempted.

- 1 Test if failing storage valid
- 2 Test to see that the FSA was not in the UCW (Unit Control Storage---Model 155 only)
- 3 Check for multiple ECC errors

Only if the preceding conditions exist is storage validation attempted.

In an MPS environment an attempt to set the storage protect key is made in situations where there was a protection error. A rotary scan is initiated to determine which partition owns the failing storage address. Once this is determined, an attempt is made to set the storage protect key for that partition.

If a machine check, other than system damage, is encountered while validating storage or repairing the SPF key, the MCAR REPAIR FAILED message is scheduled for the message writer. If system damage was encountered, the resident severity detect routine is entered by loading the machine check new PSW.

For the Model 155, if auto-configuration has occurred, a message code is posted in RASMSG2 and an information message is issued by \$\$RASTI1. Also, a total of the buffers deleted is kept in a one byte area in the RAS table called BUFDEL.

Possible messages issued at this time:

```
0T09I SOFT MACHINE CHECK
0T06I ECC MCI DISABLED
0T07I ALL SOFT MCI DISABLED
0T14I CLOCK DAMAGE. ALL MODES QUIET
0T08I C40 BUFFER PAGES DELETED=XXX
0T17I CONTROL STORAGE ECC IN QUIET MODE
0T16I EFL OVERFLOW
```

Figure 54. RMS Generation and Operation (Part 5 of 7)

10 \$\$RAST09 reallocates partition sizes whenever a machine check interrupt, other than system damage, occurs while storage validation or SPF key repair is being performed for multiple bit failures. It also issues messages regarding the size and status of the partition.

Dynamic reallocation for the background partition is as follows:

- If the size of BG from its starting address to the failing storage address is greater than 10K, BG is still considered usable and a new upper boundary address is moved into the communication region.
- If BG is less than 10K a message, BG NOT USABLE, is issued.

Dynamic reallocation for foreground partitions is as follows:

- If the upper half of a partition contains the failing storage address (FSA), the upper boundary address in the communications region is changed to the next integral boundary below the FSA. The beginning address of the partition remains unchanged. If the partition size is reduced below 10K, the batch environment is deactivated.
- If the lower half of a foreground partition contains the FSA, the beginning address in the PIB is changed to the next integral 2K boundary above the FSA. The upper boundary address remains unchanged. Again, if the foreground partition is reduced below 10K, the batch environment is deactivated.

\$\$RAST00 is fetched to determine if any more errors are pending before continuing. Normally, no more errors are pending and the system continues.

- 11 This routine gains control from either the SIO or I/O Interrupt routines when a channel check occurs. The ECSW is inspected to determine if enough information is valid to isolate the damage to either a channel or device.
- 12 When enough valid information cannot be found in the ECSW, a severe damage condition exists and an exit is taken to the resident machine check handler routine.

The EMEXIT bit is posted in location LD00SLOT and the system is terminated. For the various types of errors, see item 8.

LOWCORE is tested and contains something other than C'A" to indicate a channel error.

When an emergency situation exists, an attempt to build the first channel check record is made.

\$\$RAST01 attempts to build all remaining channel check records and records them on the ERDS. A code is posted indicating the status of the recording effort (see item 6). The SYSTERM bit is posted in LD00SLOT, and \$\$RAST00 is fetched.

With the EMEXIT and SYSTERM bits on, \$\$RAST01 attempts to issue an 0T11I Hard Wait message regarding the recording status and then to terminate the system. See item 8.

Figure 54. RMS Generation and Operation (Part 6 of 7)

- 13 If the damage cannot be isolated to a device, the entire channel is considered damaged. An ERPIB is created, with the PUB field of the ERPIB containing the address of the damaged channel. The CSW and ECSW are saved in the ERPIB for the nonresident channel check handler. If the damage can be isolated to a device the entire ERPIB is filled for the nonresident channel check handler.
- 14 This routine gains control from the channel check handler when the damaged device is a DASD unit. The operation is retried by restarting the chain of CCWs.

The channel queue pointer byte of the ERPIB is used as an error counter. If the retry count has not been reached and the channel check occurred on an SIO instruction, a branch to the SIO instruction is taken. If the channel check occurred at interrupt time, a branch to restart the operation is taken.

If ten retry attempts fail, the task is canceled. If channel check occurred in the supervisor, the system is terminated.

If retry is successful, a message is issued regarding the error and a recoverable channel check is recorded on SYSREC.

15 \$\$RAST02 builds the first channel check record. The appropriate ERP is activated.

\$\$RAST04 Unit record ERP

\$\$RAST05 Unit record ERP

\$\$RAST06 Not used

\$\$RAST07 Tape ERP

\$\$RAST01 builds all but the first channel check records and stores them on the ERDS. All machine check record building is bypassed.

The recording status is posted in LOWCORE+2 on system termination. See item 6 for the status codes.

The ERPs take appropriate action to handle the error depending on the data stored in the ERPIB.

17 \$\$RAST10 issues all messages pertinent to the ERPs and clears the ERPIBs.

The following messages are possible:

OT101 CHANNEL ERROR RECOVERY ON CUU

OT12I IRRECOVERABLE CHANNEL ERROR ON CUU

OT13A CHANNEL ERROR ON CUU

\$\$RAST00 is fetched to determine if any more errors are pending before continuing.

Figure 54. RMS Generation and Operation (Part 7 of 7)

Chart BH. \$\$A\$SUP1 - FOPT Macro, SVC Interrupt Handler Refer to Chart 03.

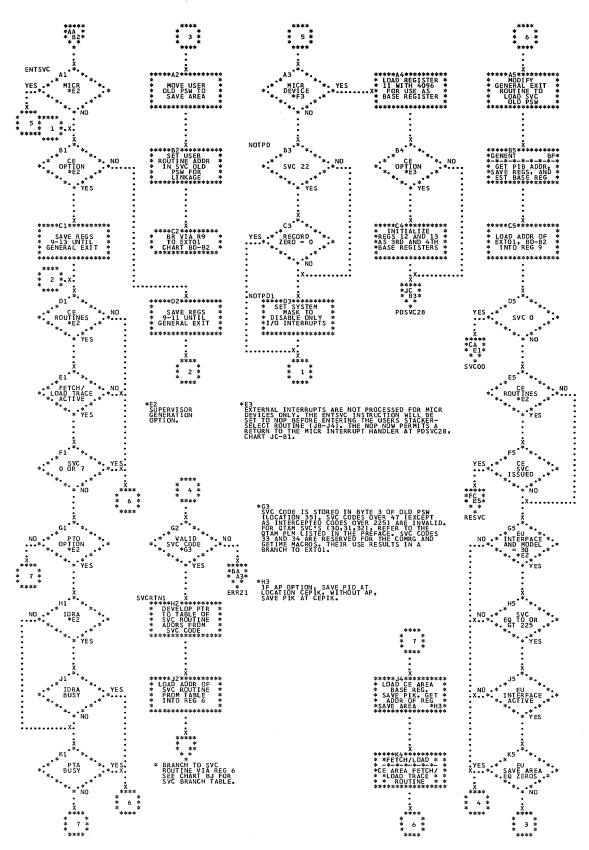


Chart BJ. \$\$A\$SUP1 - FOPT Macro, Supervisor Call Branch Table

svc	OPTIONS	LABEL	CHART
0	ALL	SVC00	CA-F1
1	ALL	SVC01	FA-B1
2	ALL	SVC02	FC-B1
3	ALL	SVC03	FF-A1
4	ALL	SVC04	FF-B4
5	ALL	SVC05	FB-B2
6	ALL	SVC06	MM-B4
7	ALL	SVC07	FE-A3
8	ALL	SVC08	FG-A1
9	ALL	SVC09	FG-A2
10	TIMER NO TIMER	SVC10 ERR21	FG-B5 BA-A3
11	ALL	SVC11	FE-B1
12	ALL	SVC12	FA-B2
13	ALL	SVC13	FA-B4
14	ALL	ERR10	BA-A1
15	MPS NO MPS	SVC15	CA-B1 CB-B1
16	PC, NO IT OR OC PC AND IT OR OC NO PC	SXTRTI SXTRTI ERR21	FJ-B5 FN-B4 BA-A3
17	PC, NO IT OR OC PC AND IT OR OC NO PC	EXTRT1 EXTRT1 ERR21	FJ-B4 FN-B2 BA-A3
18	TIMER NO TIMER	SVC18 ERR21	FN-B5 BA-A3
19	TIMER NO TIMER	SVC19 ERR21	FN-B3 BA-A3
20	OC RTN NO OC RTN	SXTRT1 ERR21	FN-B4 BA-A3
21	OC RTN NO OC RTN	EXTRT1 ERR21	FN-B2 BA-A3
22	MPS NO MPS	SVC22 EXT01	FH-B1 BD-B2
23	MPS NO MPS	SVC23 ERR21	FH-B3 BA-A3
24	TIMER NO TIMER	SVC24 ERR21	FH-B5 BA-A3
25	BTAM OR OLTEP NO BTAM AND NO OLTEP	SVC25 ERR21	CA-F1 BA-A3

svc	OPTIONS	LABEL	CHART
26	STOR PROT	SVC26	FH-B4
	NO STOR PROT	EXT01	BD-B2
27	BTAM	SVC27	CA-F1
	NO BTAM	EXT01	BD -B 2
28	MICR	PDSVC28	JC-B3
	NO MICR	ERR21	BA-A3
29	MICR	SVC29	FB-B3
	NO MICR	ERR21	BA-A3
30 TO 32	RESERVED FOR QTAM: REFER TO QTAM PLM LISTED IN PREFACE		-
33, 34	RESERVED FOR COMRG AND GETIME MACROS)	
35	TRKHLD	SVC35	MA-A1
	NO TRKHLD	ERR21	BA-A3
36	TRKHLD	SVC36	MB-A1
	NO TRKHLD	ERR21	BA-A3
37	AB	SVC37	MC-A4
	NO AB	ERR21	BA-A3
38	AP	SVC38	MD-A1
	NO AP	ERR21	BA-A3
39	AP	SVC39	ME-A1
	NO AP	ERR21	BA-A3
40	AP	SVC40	MG-A1
	NO AP	ERR21	BA-A3
41	AP	SVC41	MH-A1
	NO AP	ERR21	BA-A3
42	AP	SVC42	MG-A4
	NO AP	ERR21	BA-A3
43	ERROR OR MCRR	SDRSDR	LF-C5
	NO ERRLOG AND NO MCRR	ERR21	BA-A3
44	ERRLOG OR MCRR	SDROBR	LF-C4
	NO ERRLOG AND MCRR	ERR21	BA-A3
45	EMULATOR INTERFACE	SVC45	FR-B1
	NO EMULATOR INTERFACE	ERR21	BA-A3
46	OLTEP INTERFACE	SVC46	FR-F4
	NO OLTEP INTERFACE	ERR21	BA-A3
47	WAITF FOR MICR DEVICES	SVC29	FB-B3
50	USED BY LIOCS FOR ERROR RECOVERY		
51	OLTEP	SVC51	FS-B2
	NO OLTEP	ERR21	BA-A3
52	MPS NO MPS	SVC52 ERR21	BA-A3

Chart CB. \$A\$SUP1 - SGTCHS Macro, Channel Scheduler without MPS Refer to Chart 04.

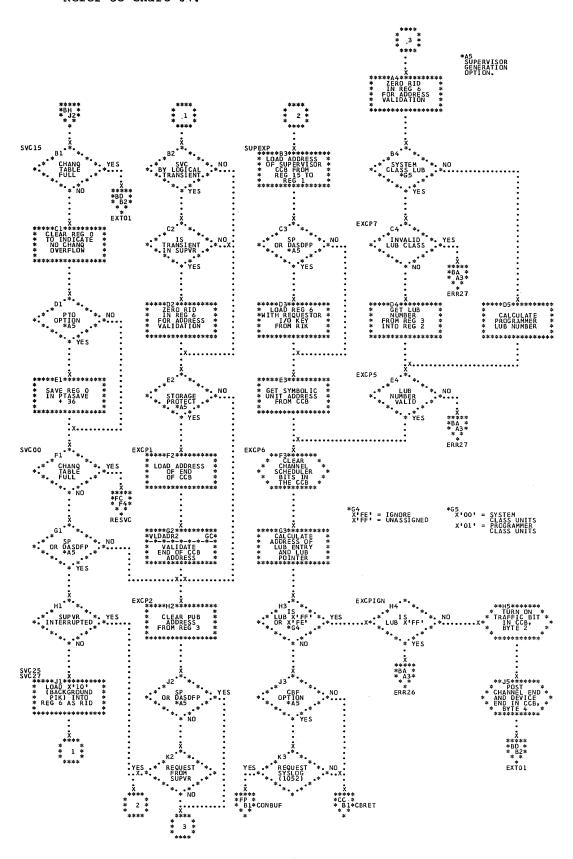


Chart CC. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler (Part 1 of 3)
Refer to Chart 04:

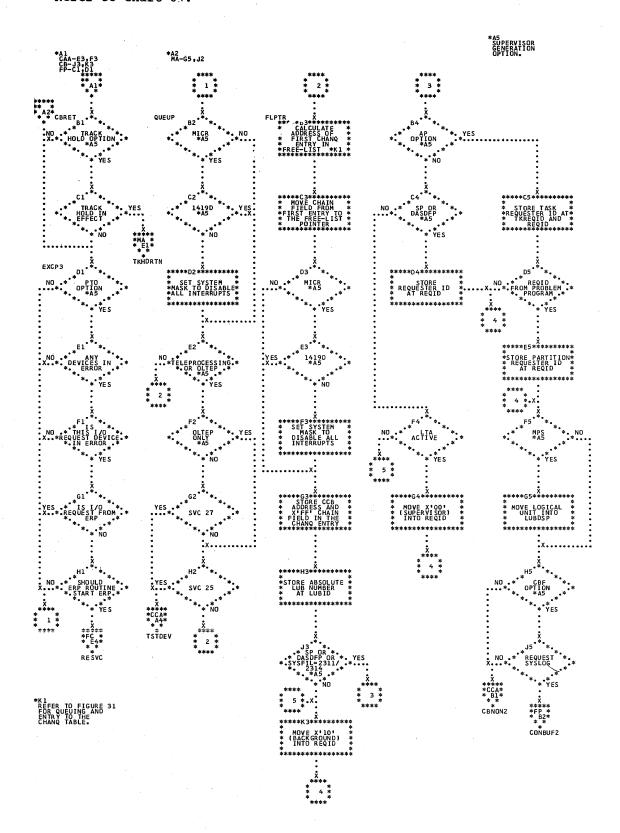


Chart CCA. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler (Part 2 of 3) Refer to Chart 04.

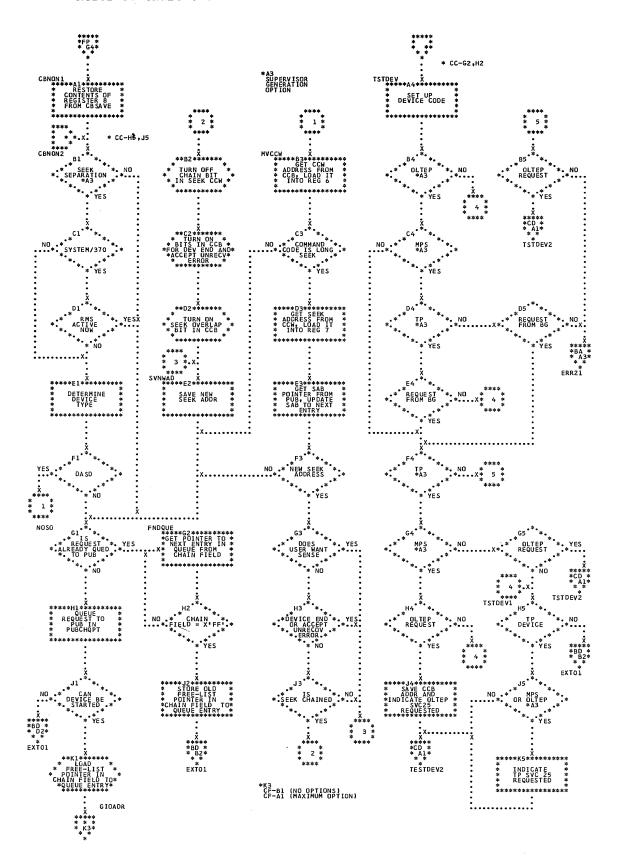


Chart CD. \$\$A\$SUP1 - SGTCHS Macro, Channel Scheduler (Part 3 of 3) Refer to Chart 04.

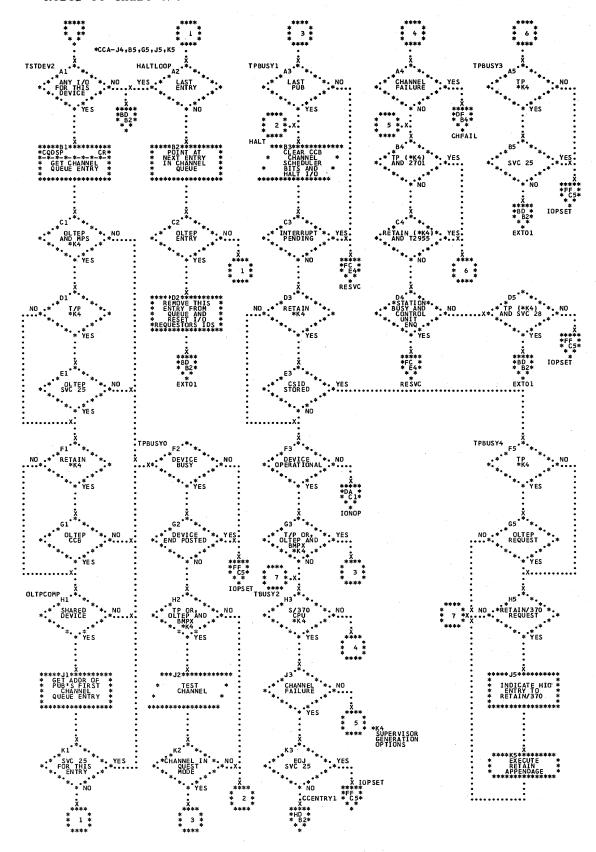


Chart CE. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- No Options, UNCOMMON Routine Refer to Chart 04.

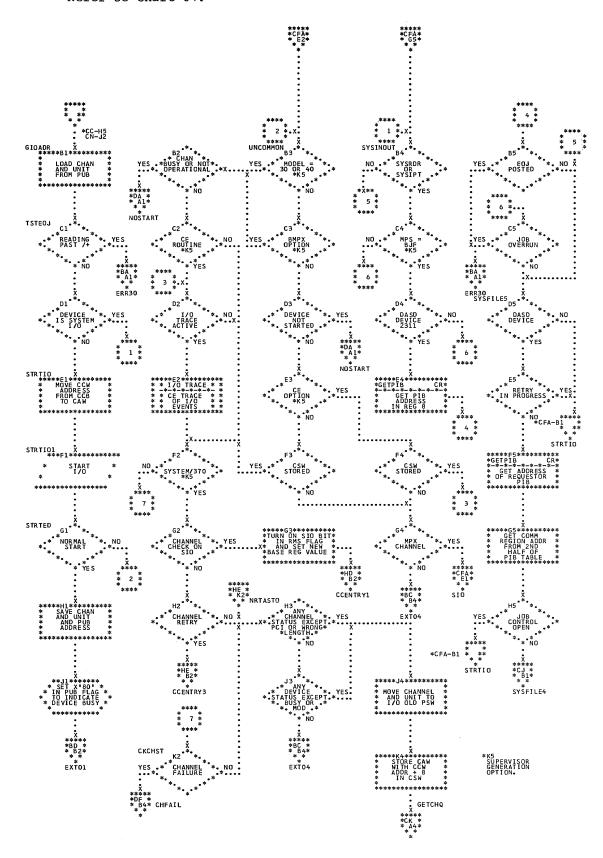


Chart CF. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- Maximum Options (Part 1 of 5) Refer to Chart 04.

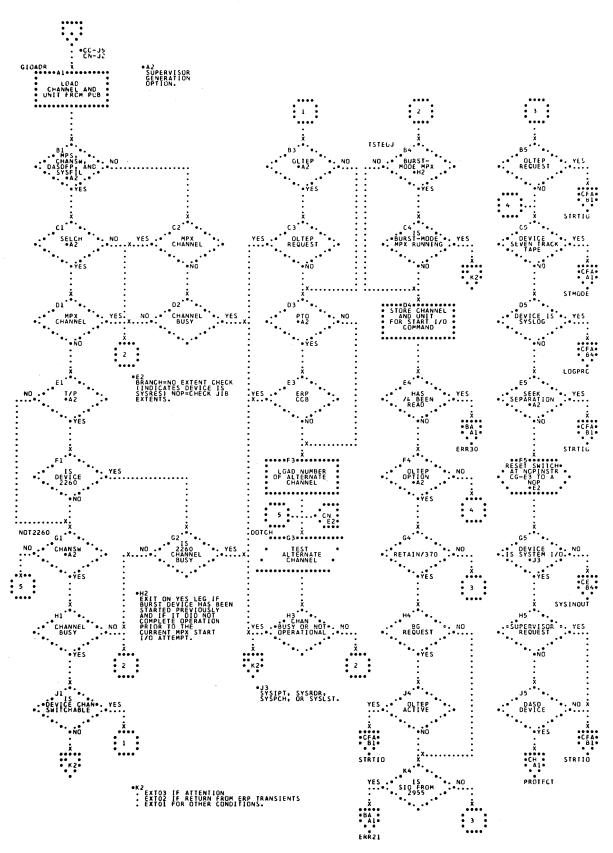


Chart CFA. \$\$A\$SUP1 - SGTCHS Macro, Start I/O -- Maximum Options (Part 2 of 5) Refer to Chart 04.

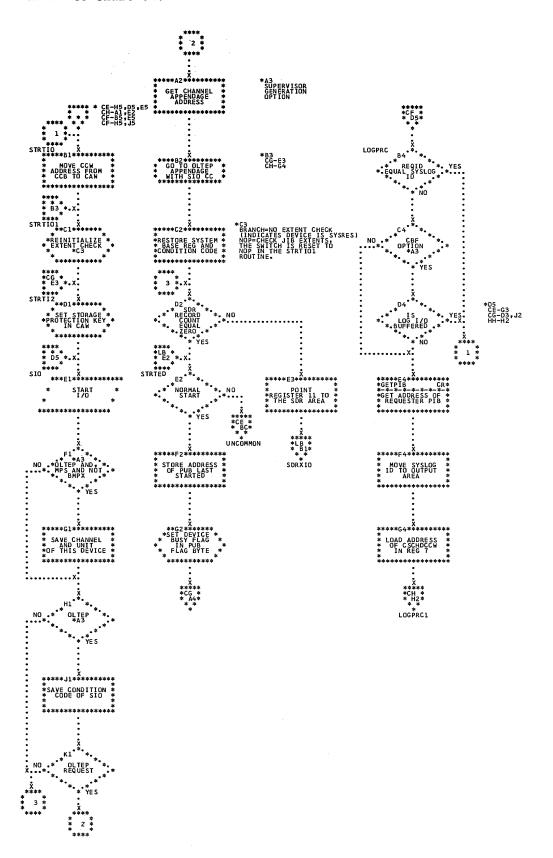


Chart CG. \$\$A\$SUPl - SGTCHS Macro, Start I/O -- Maximum Options (Part 3 of 5) Refer to Chart 04.

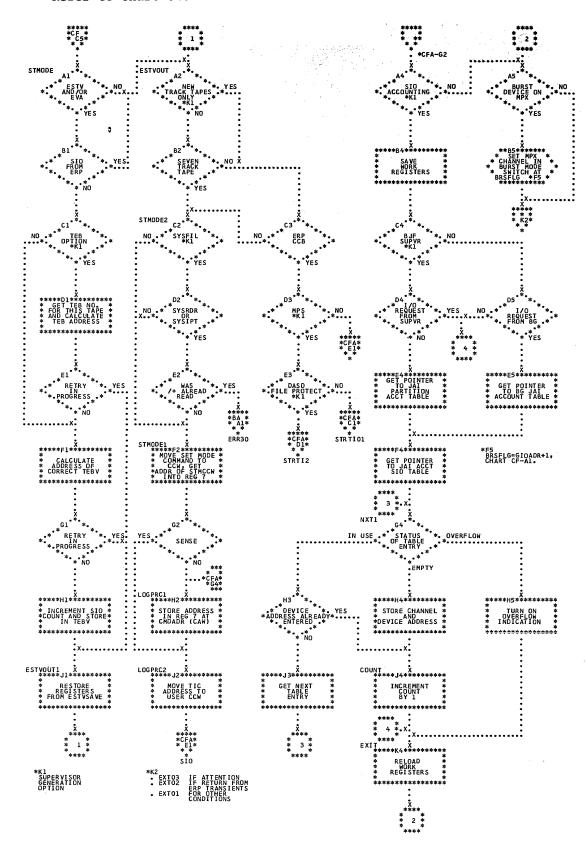
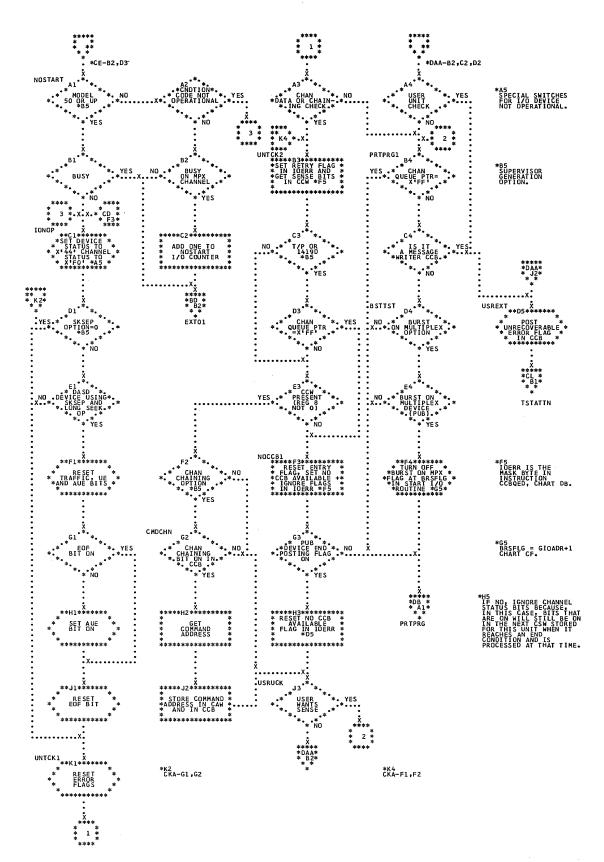


Chart DA. \$\$A\$SUP1 - SGUNCK Macro, Unit Check Entries (Part 1 of 2)
Refer to Chart 06.



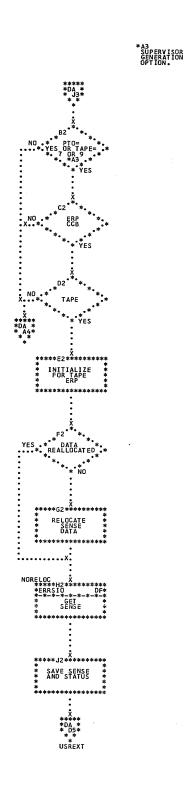


Chart DB. \$\$A\$SUP1 - SGUNCK Macro, Build Error Queue Entry Refer to Chart 06.

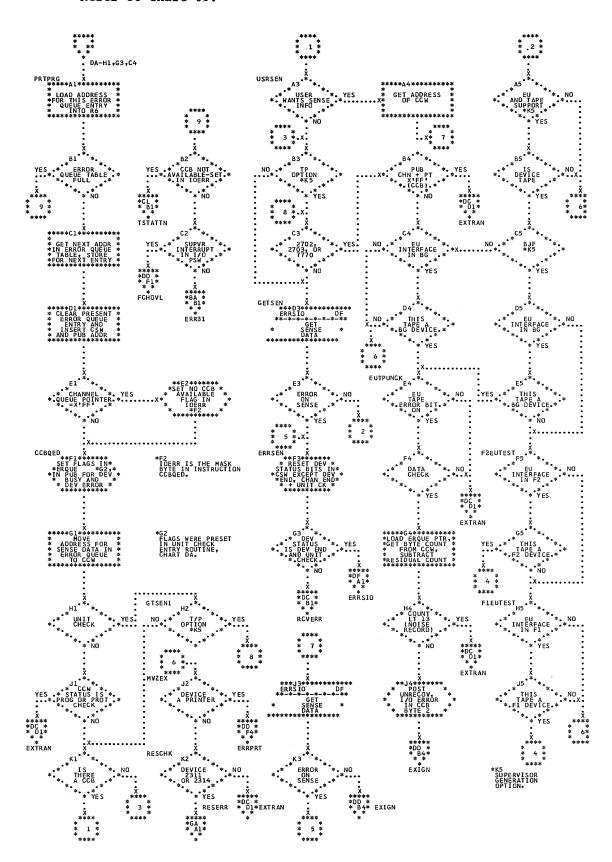


Chart DC. \$\$A\$SUP1 - SGUNCK Macro, Error Recovery Exits (Part 1 of 2) Refer to Chart 06.

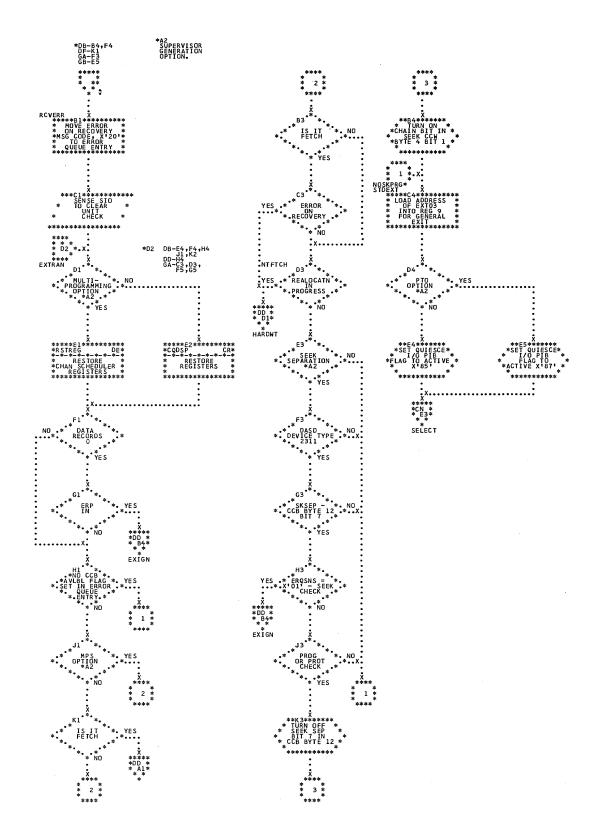


Chart DF. \$\$A\$SUPl - SGUNCK Macro, Error Start I/O and Channel Failure Subroutines Refer to Charts 06 and 07.

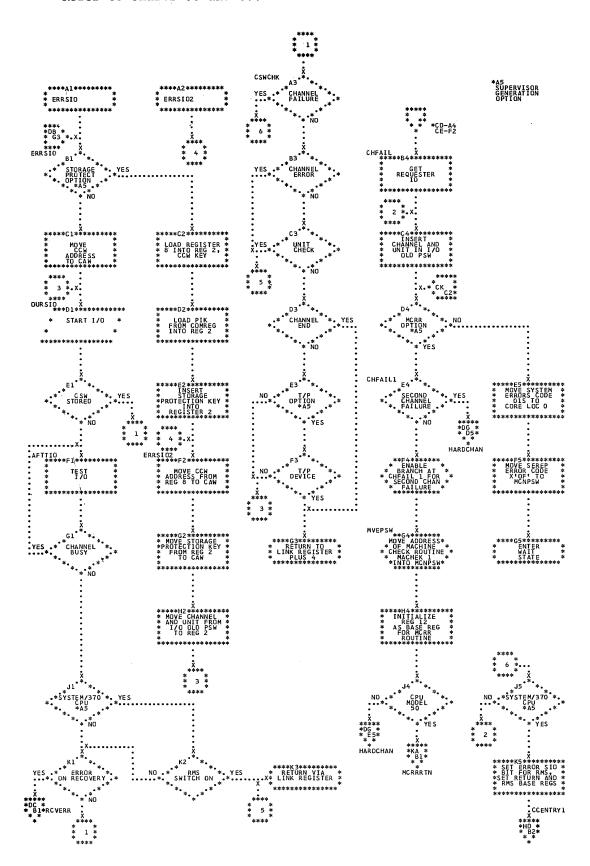


Chart DG. \$\$A\$SUPl - SGUNCK Macro, Machine Check Interrupt Refer to Chart 07.

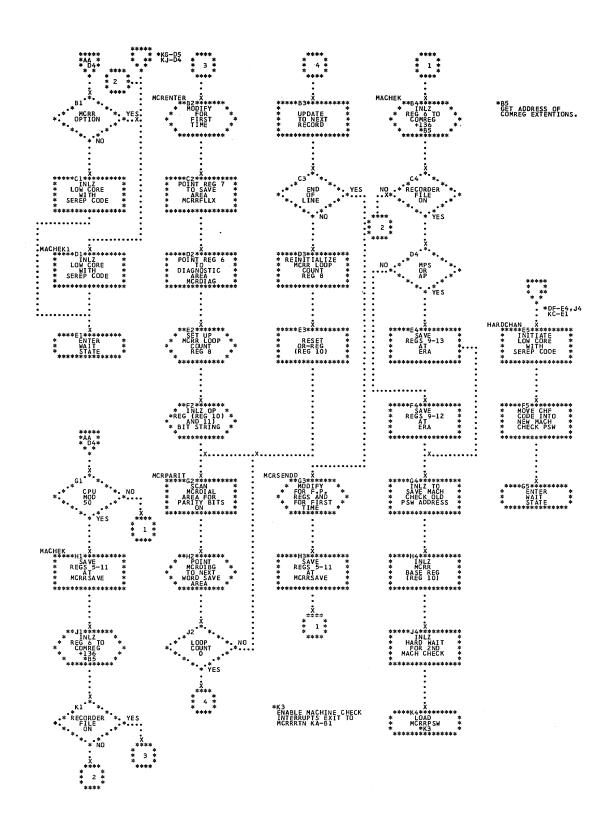


Chart EB. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 2 of 9) Refer to Chart 03.

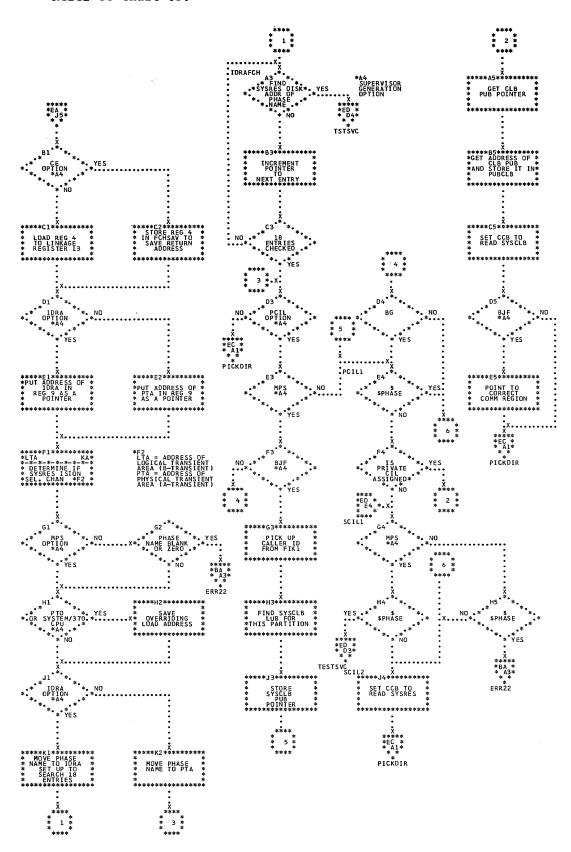


Chart EC. \$\$A\$SUP1 - SGDFCH Macro, Fetch (Part 3 of 9) Refer to Chart 03.

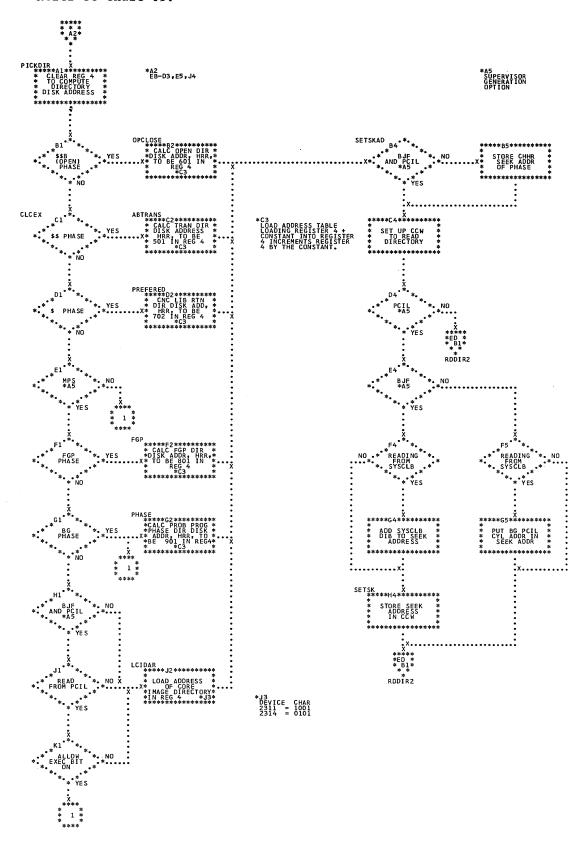


Chart FA. \$\$A\$SUP1 - SGSVC Macro, SVCs 1, 12, and 13 Refer to Chart 03.

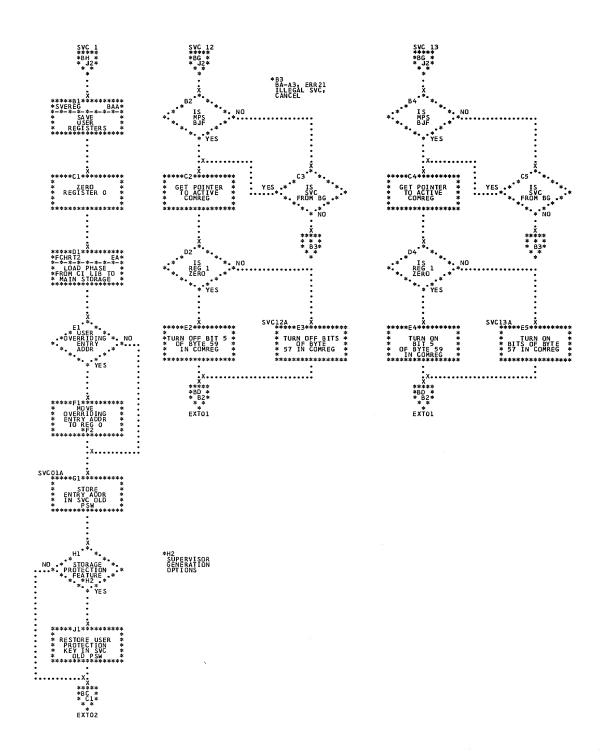


Chart FB. \$\$A\$SUP1 - SGSVC Macro, SVCs 5, 26, and 29 Refer to Chart 03.

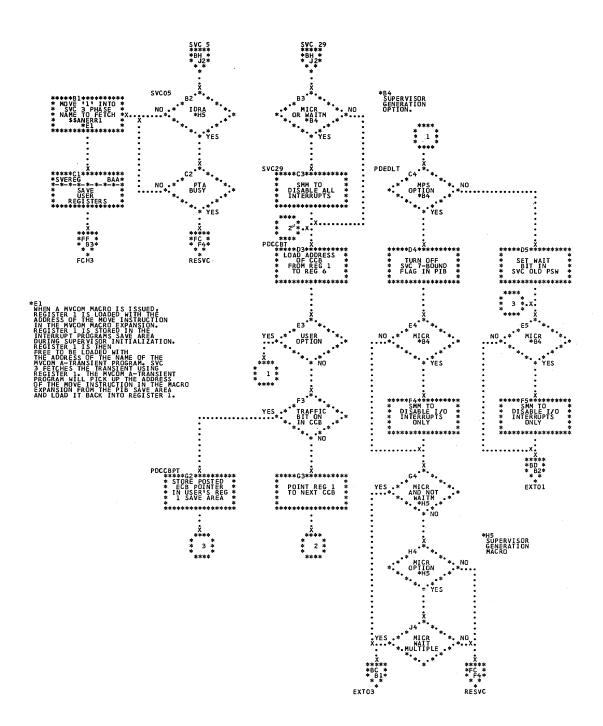


Chart FC. \$\$A\$SUP1 - SGSVC Macro, SVC 2 (Part 1 of 2) Refer to Chart 03.

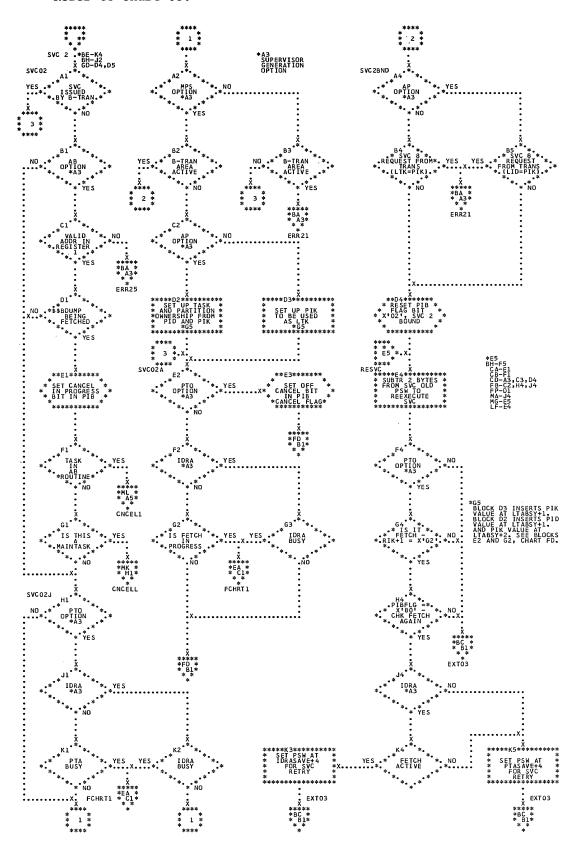


Chart FD. \$\$A\$SUP1 - SGSVC Macro, SVC 2 (Part 2 of 2), SETLT1 and SETLT2 Routines. Refer to Chart 03.

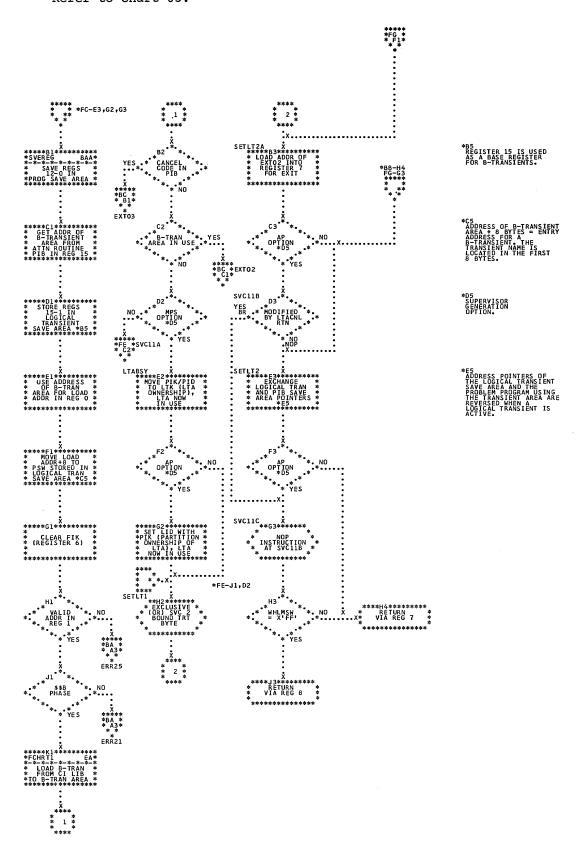


Chart FE. \$\$A\$SUP1 - SGSVC Macro, SVCs 7 and 11 Refer to Chart 03.

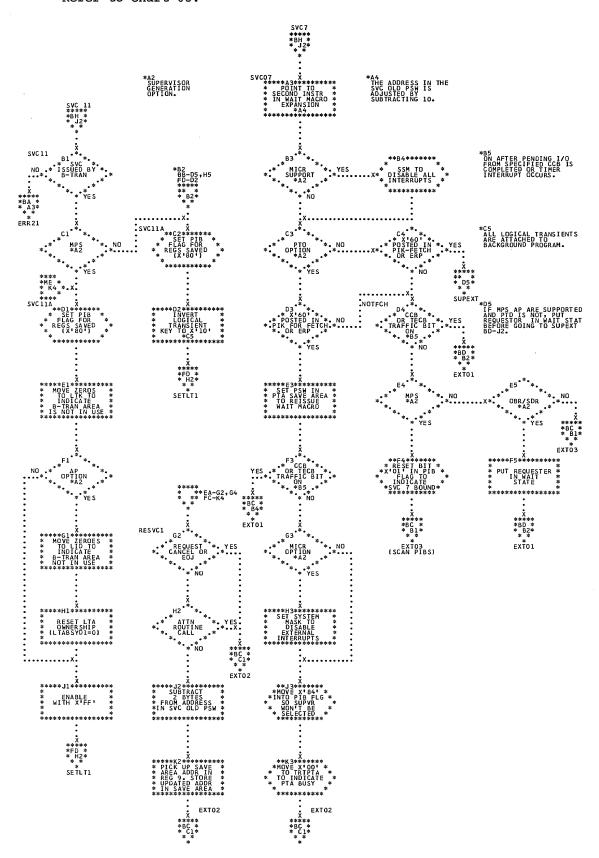


Chart FF. \$\$A\$SUP1 - SGSVC Macro, SVCs 3 and 4 Refer to Chart 03.

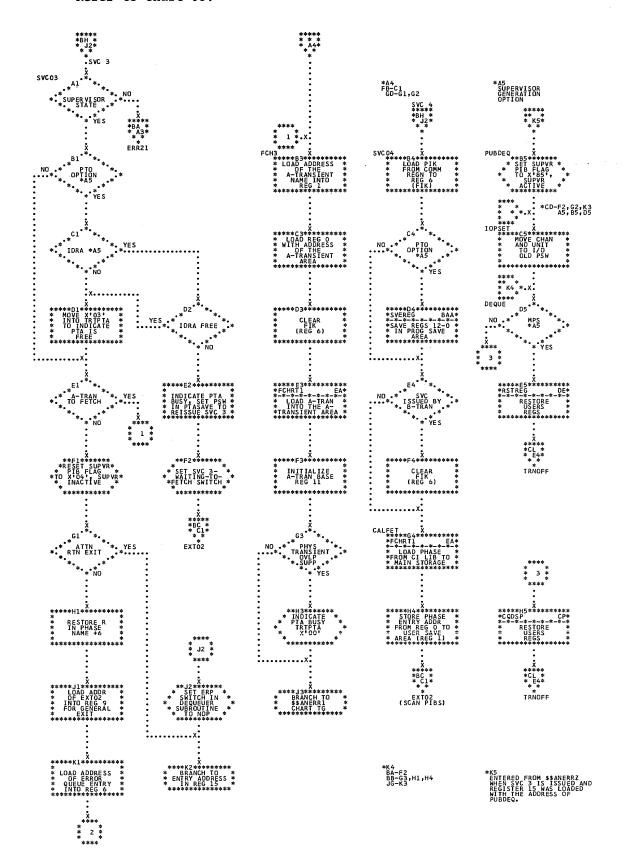


Chart FQ. \$\$A\$SUP1 - SGSVC Macro, Console Buffering Routine (Part 2 of 2) Refer to Chart 04.

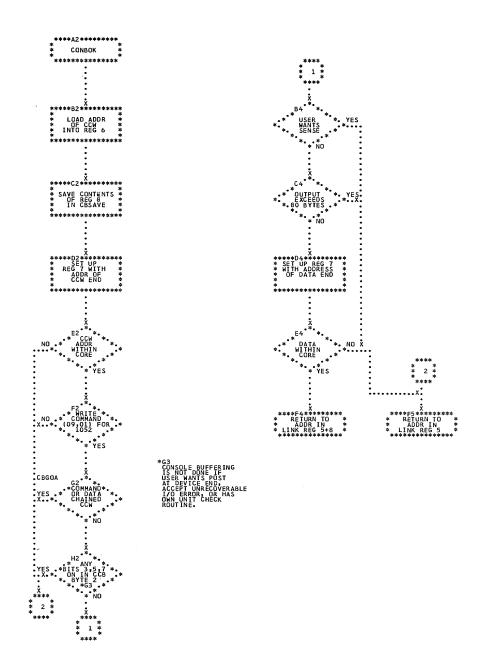


Chart FR. \$\$A\$SUP1 - SGSVC Macro, SVCs 43, 45, and 46 Refer to Chart 03.

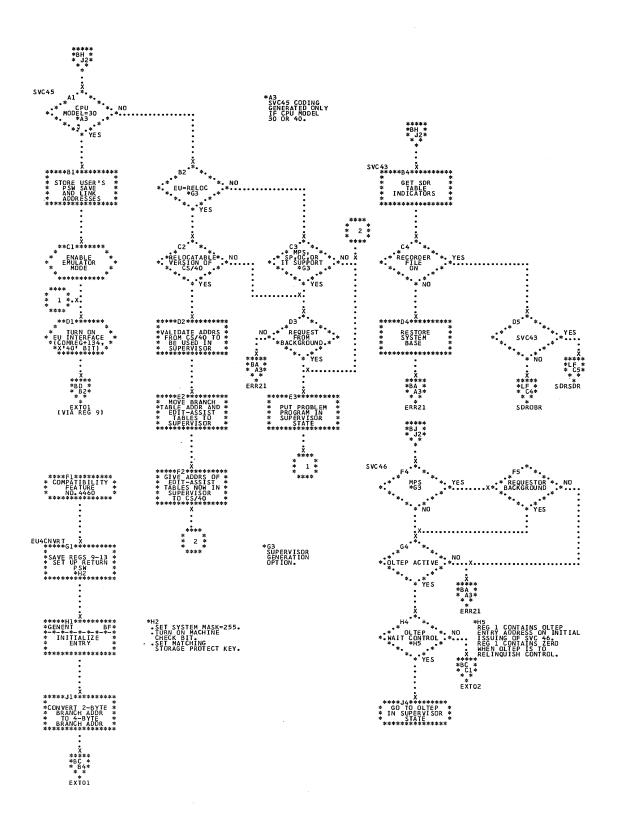


Chart FS. \$\$A\$SUPl - SGSVC Macro, SVC 51 Refer to Chart 03.

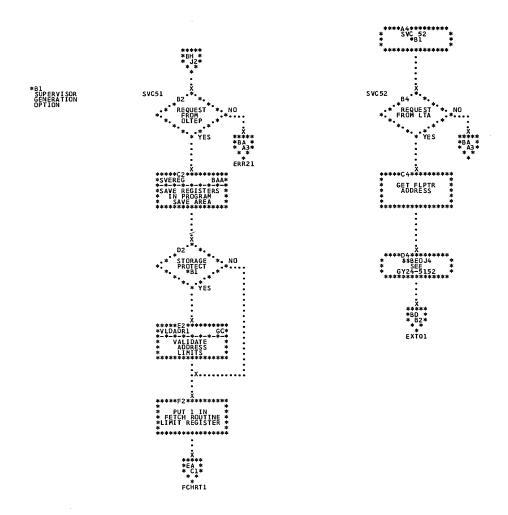


Chart GA. \$\$A\$SUPl - SGDSK Macro, Disk Error Recovery (Part 1 of 2) Refer to Chart 06.

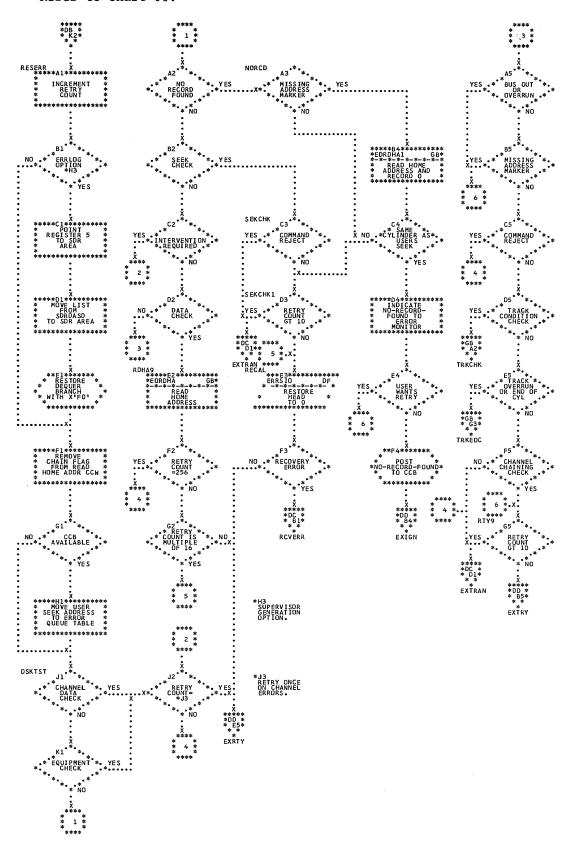
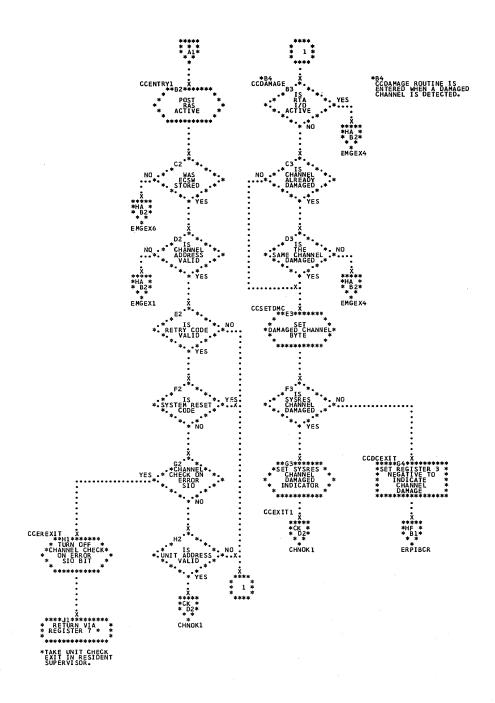


Chart HD. \$\$A\$SUPl - MCRAS Macro, Resident Channel Check Handler (Part 1 of 4) Refer to Chart 09.



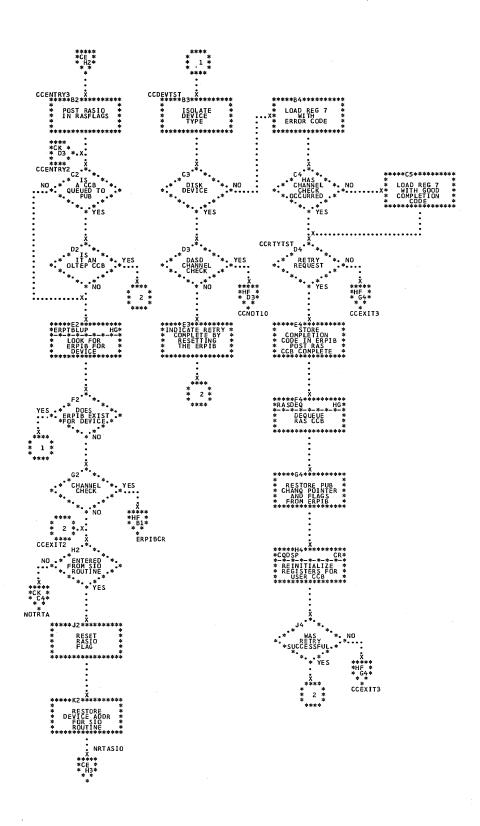


Chart JH. \$\$A\$SUP1 - SMICR Macro, Exit Routine Refer to Chart 02.

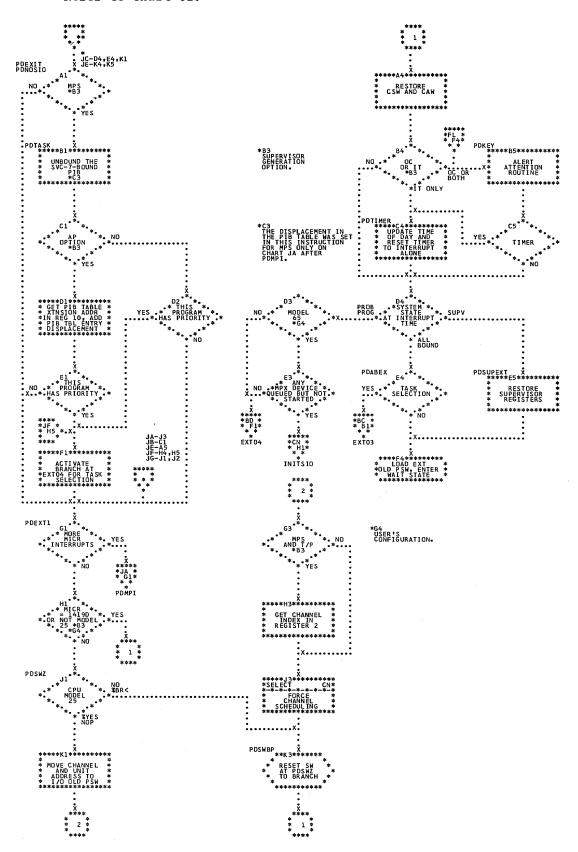


Chart KA. \$\$A\$SUP1 - SMCRR Macro, Channel Inboard Error Record Builder (Part 1 of 4)
Refer to Chart 10.

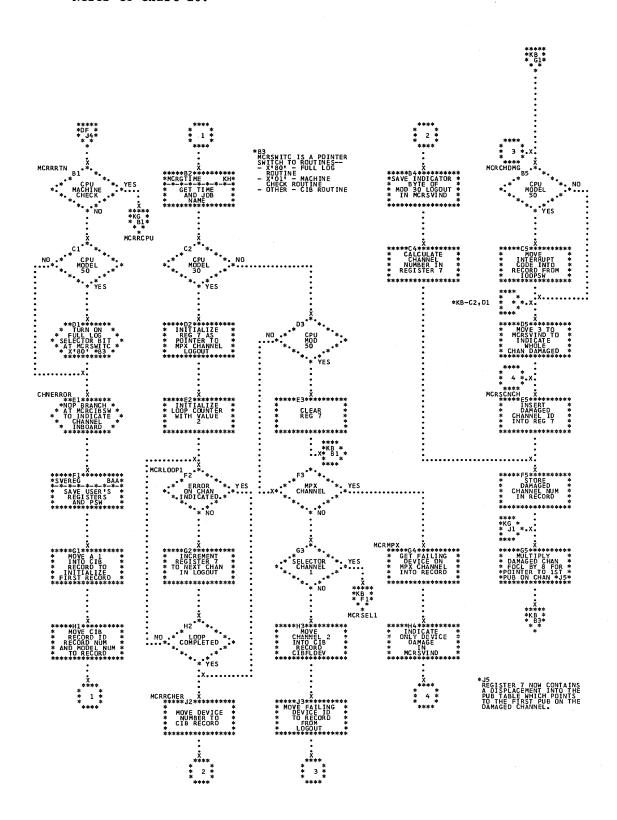


Chart KB. \$\$A\$SUP1 - SMCRR Macro, Channel Inboard Error Record Builder (Part 2 of 4) Refer to Chart 10.

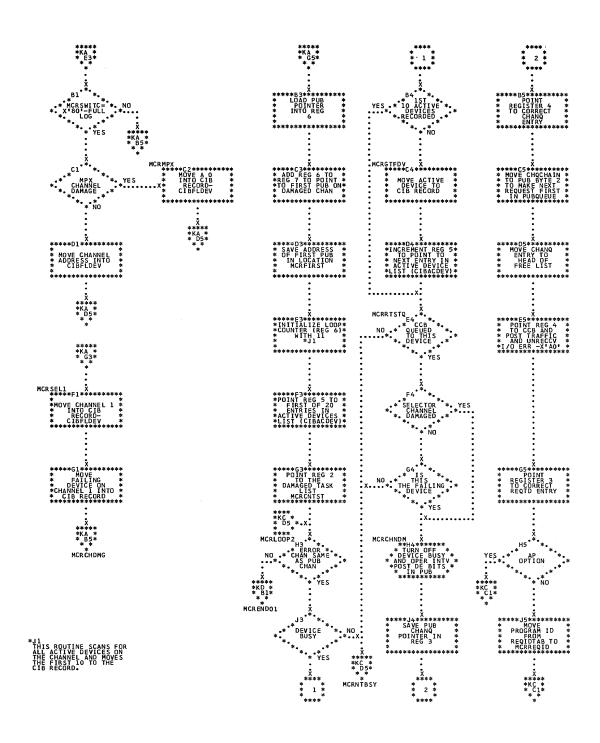


Chart KC. \$\$A\$SUP1 - SMCRR Macro, Channel Inboard Error Record Builder (Part 3 of 4) Refer to Chart 10.

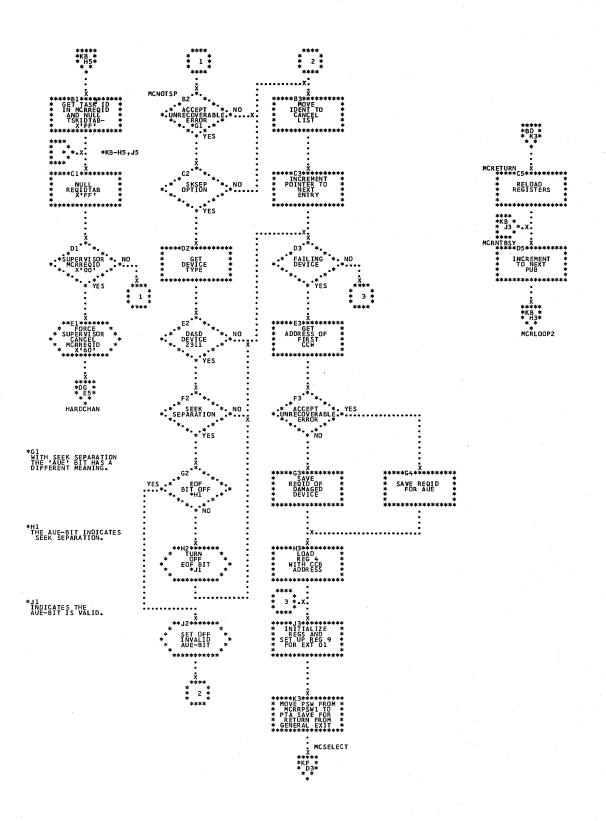


Chart ME. \$\$A\$SUPl - SCTHAP Macro, DETACH a Task (Part 1 of 2) Refer to Chart 03.

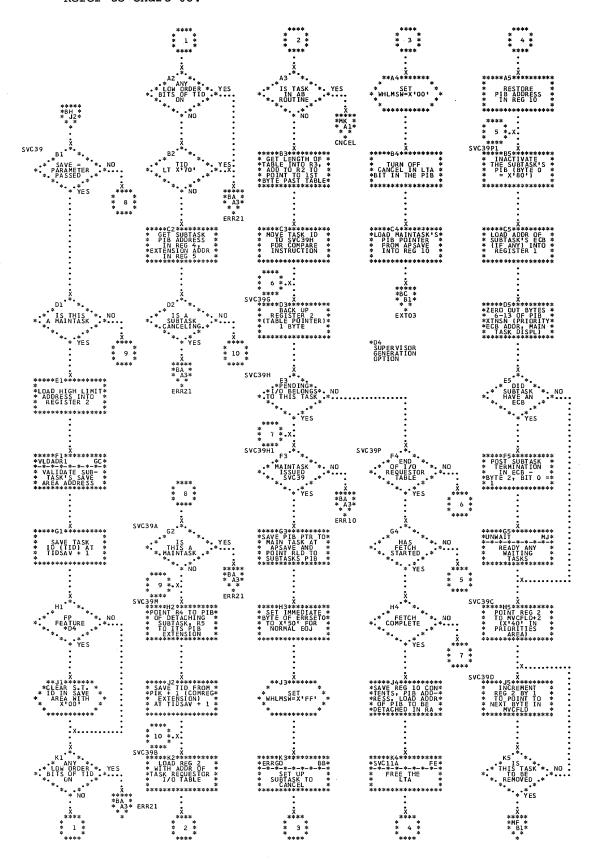


Chart MF. \$\$A\$SUPl - SGTHAP Macro, DETACH a Task (Part 2 of 2) Refer to Chart 03.

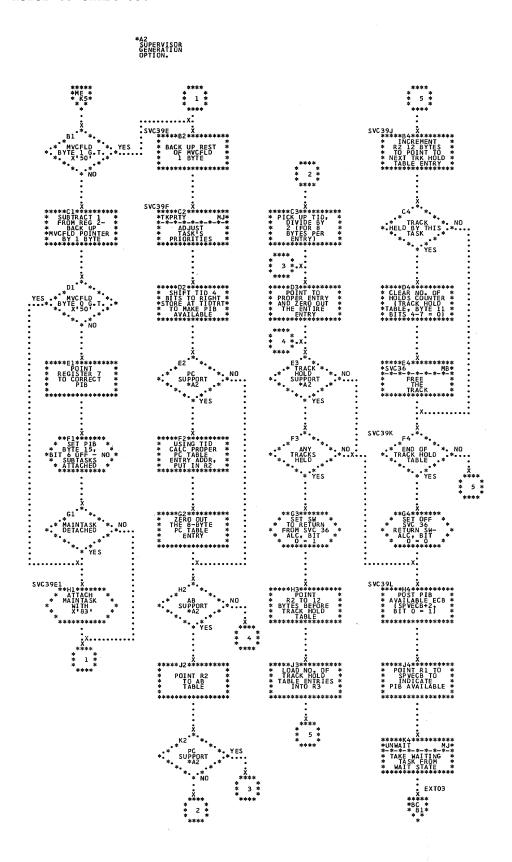


Chart NJ. \$\$ANERAG - Recorder File Last Track Error Message Writer for OBR/SDR Refer to Chart 13.

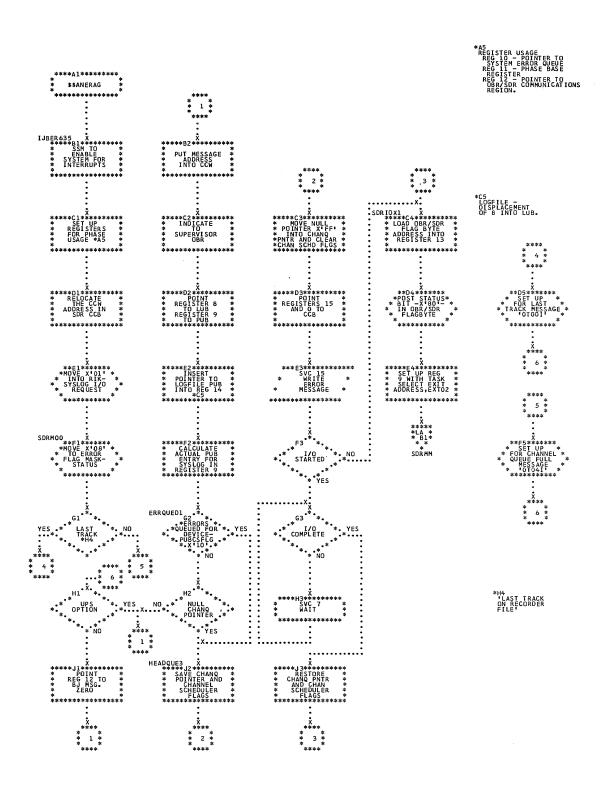
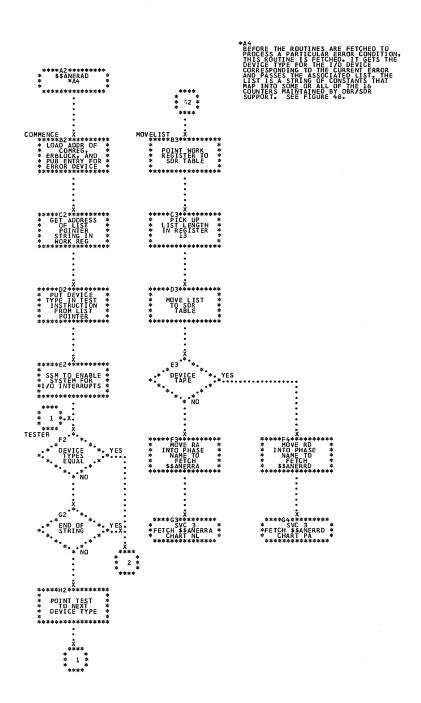


Chart NK. \$\$ANERAD - List Passer for SDR Processor Refer to Chart 11.



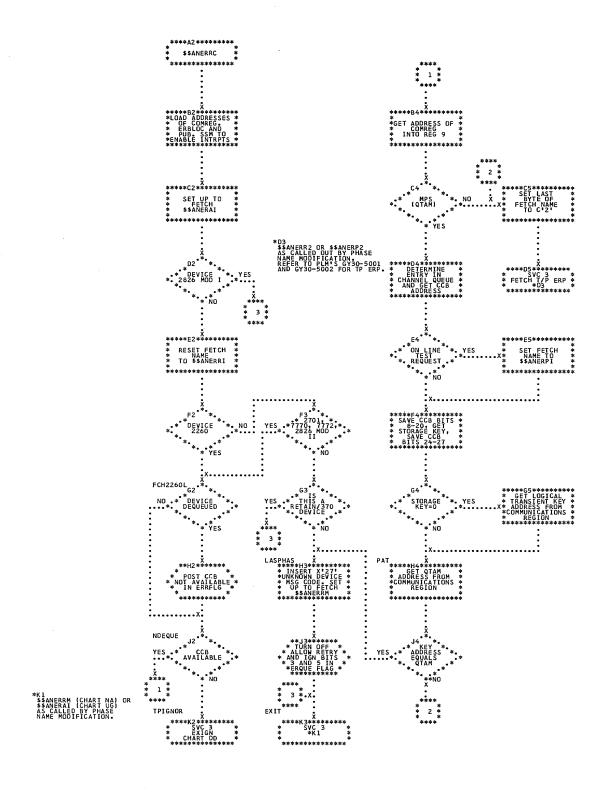


Chart NN. \$\$ANERRB - Disk ERP Refer to Chart 11.

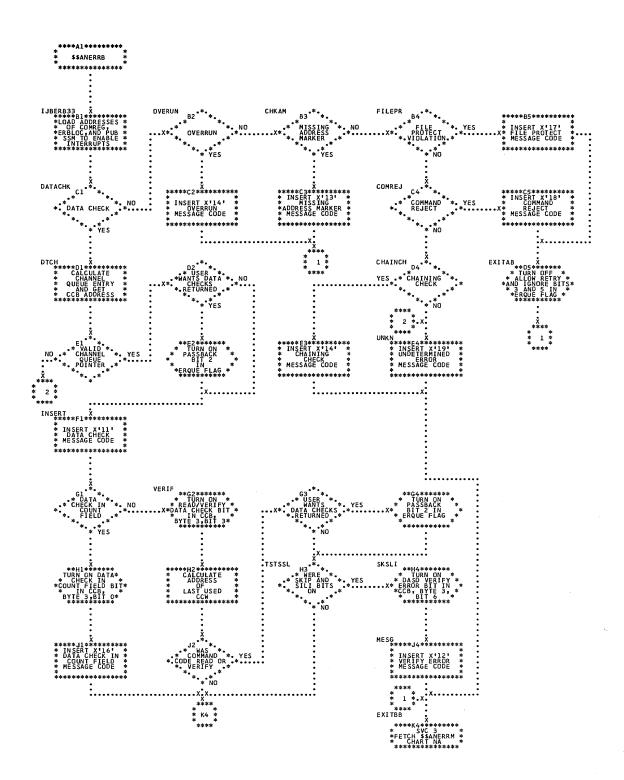
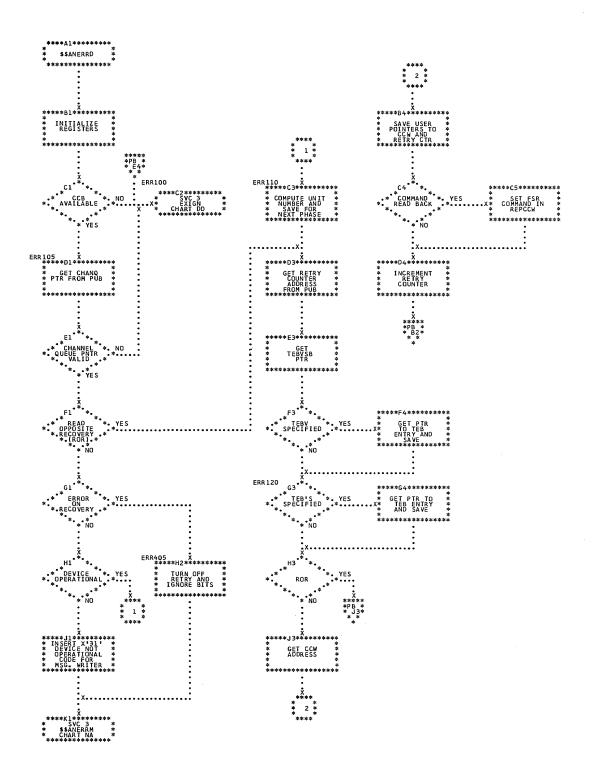


Chart PA. \$\$ANERRD - Phase 1 of Tape ERP (Part 1 of 2) Refer to Chart 13.



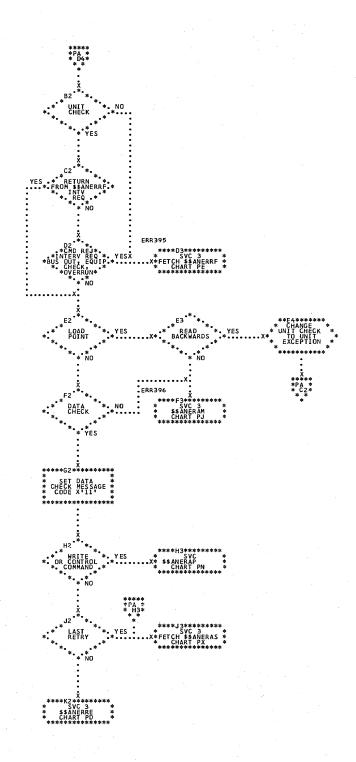


Chart QA. \$\$ANERRG - Phase 1 of Data Cell ERP (Part 1 of 3) Refer to Chart 11.

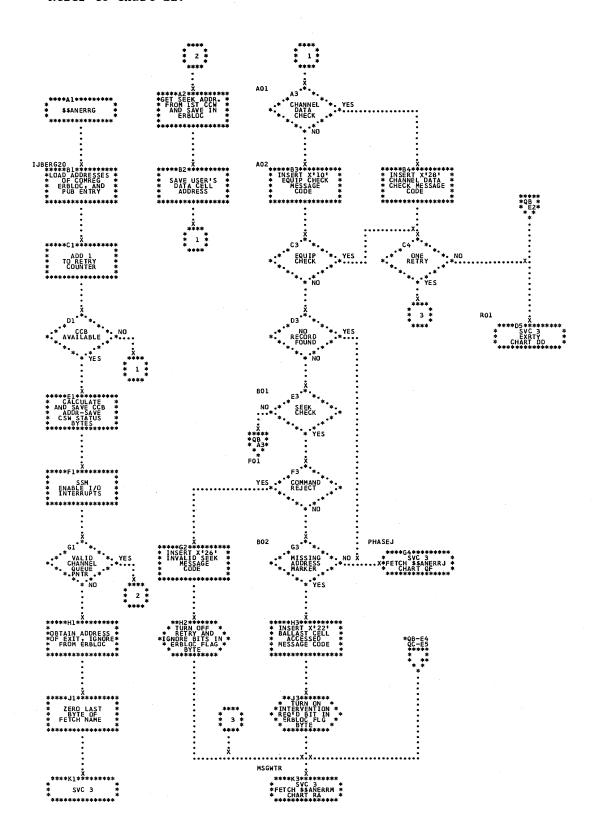


Chart QB. \$\$ANERRG - Phase 1 of Data Cell ERP (Part 2 of 3) Refer to Chart 11.

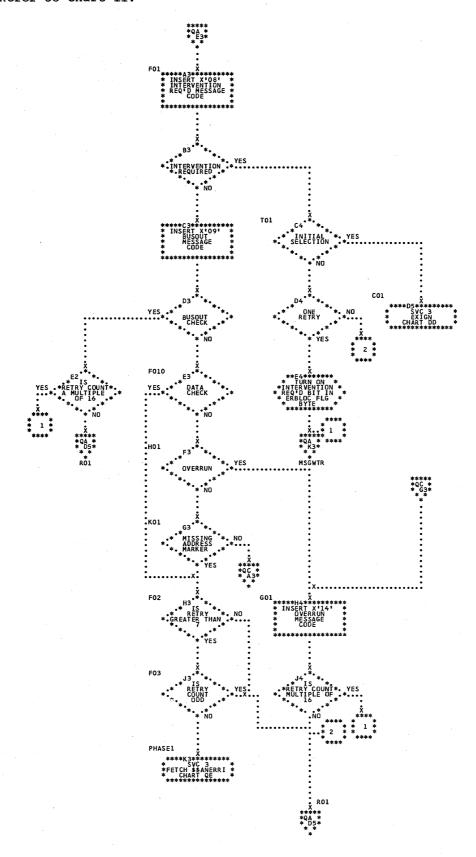


Chart QC. \$\$ANERRG - Phase 1 of Data Cell ERP (Part 3 of 3) Refer to Chart 11.

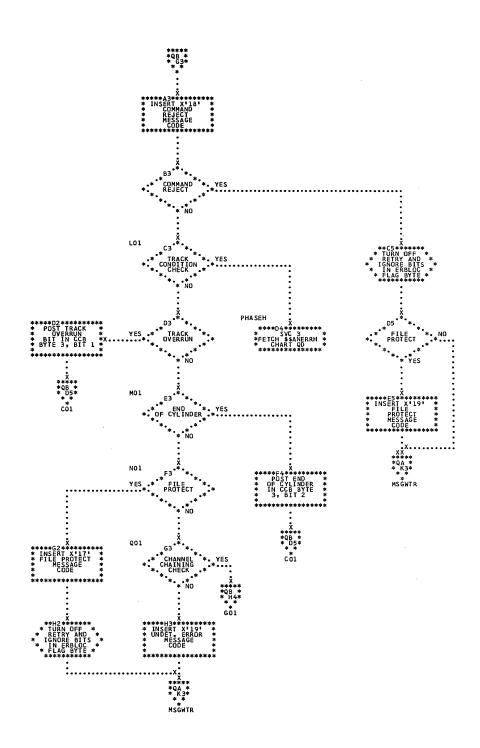


Chart QD. \$\$ANERRH - Phase 2 of Data Cell ERP Refer to Chart 11.

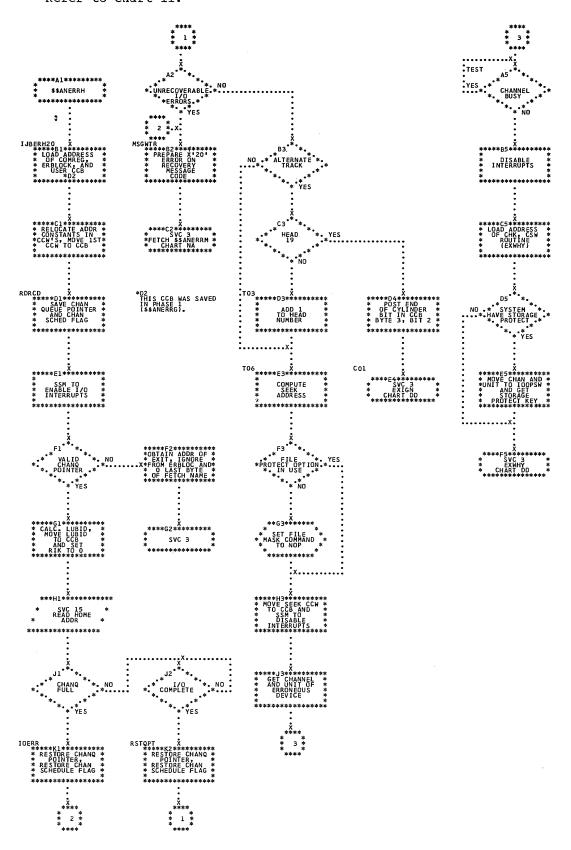


Chart QE. \$\$ANERRI - Phase 3 of Data Cell ERP Refer to Chart 11.

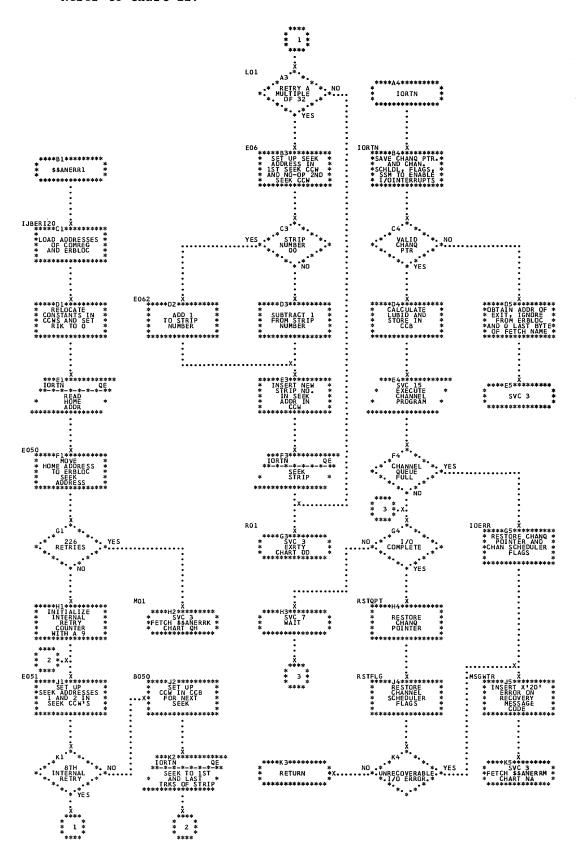


Chart QF. \$\$ANERRJ - Phase 4 of Data Cell ERP (Part 1 of 2) Refer to Chart 11.

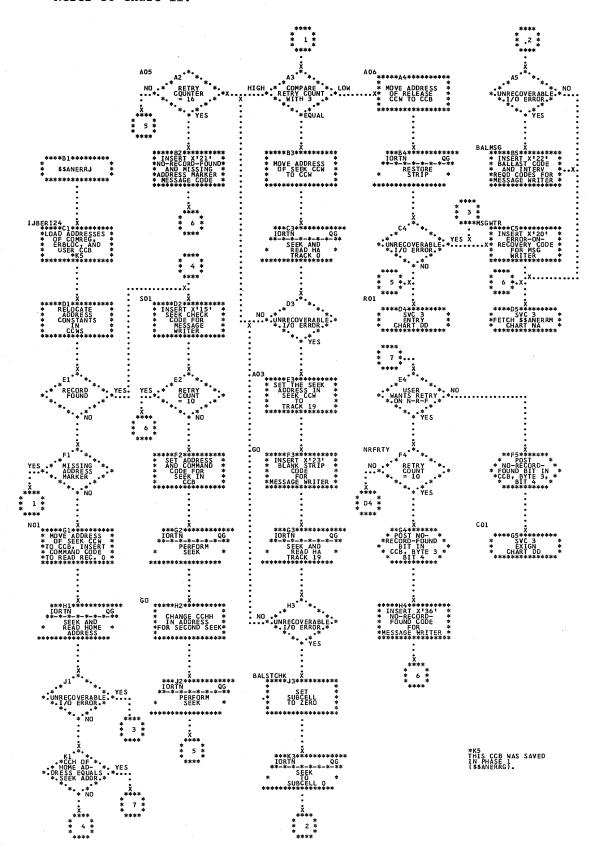


Chart QG. \$\$ANERRJ - Phase 4 of Data Cell ERP (Part 2 of 2) Refer to Chart 11.

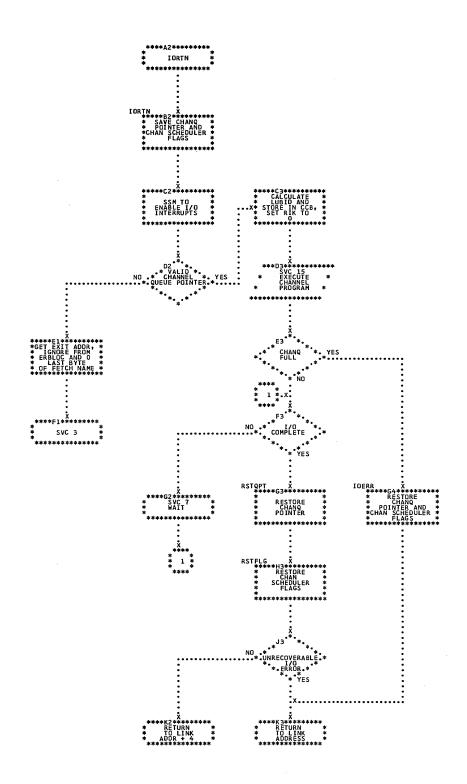


Chart QH. \$\$ANERRK - Phase 5 of Data Cell ERP Refer to Chart 11.

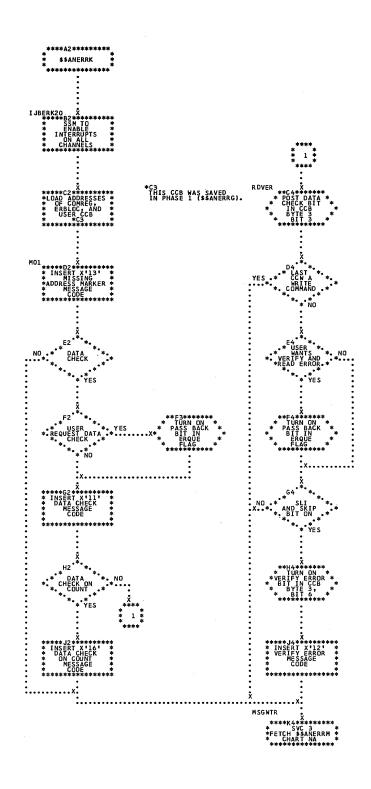


Chart RL. \$\$ANERRS - Phase 7 of ERP Message Writer (Part 2 of 2) Refer to Chart 14.

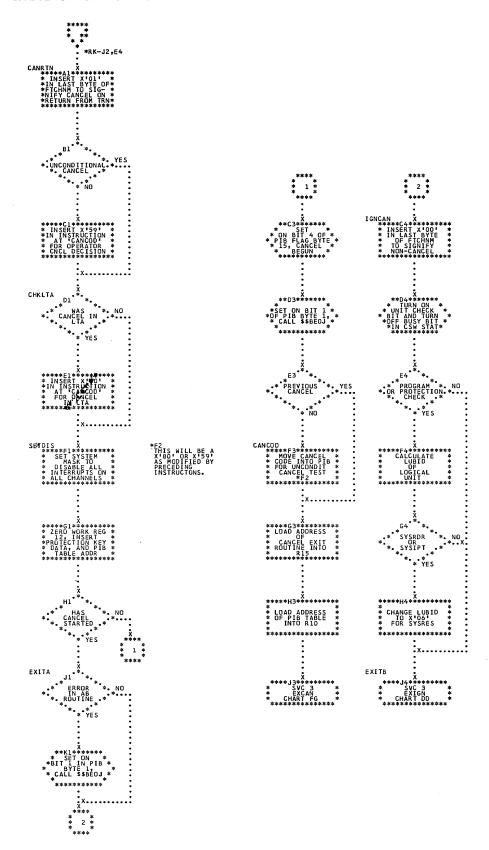


Chart SA. \$\$ANERRT - MICR (1412/1419) ERP Refer to Chart 12.

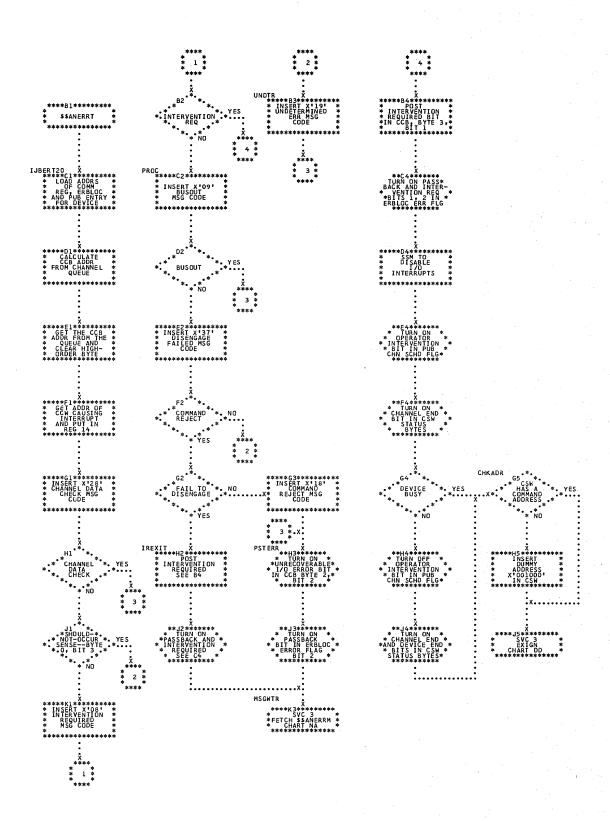


Chart SF. \$\$ANERRW - MICR (1419D) ERP (Part 1 of 3) Refer to Chart 12.

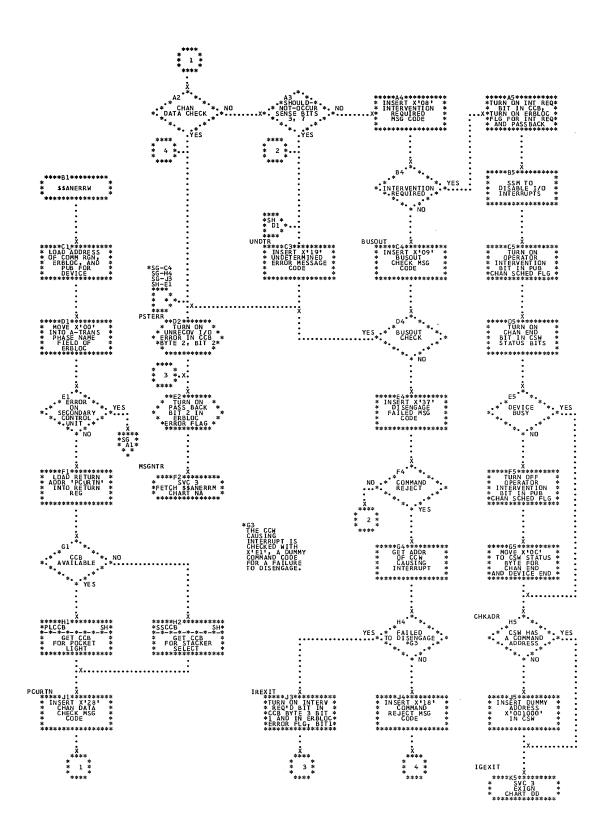


Chart SG. \$\$ANERRW - MICR (1419D) ERP (Part 2 of 3) Refer to Chart 12.

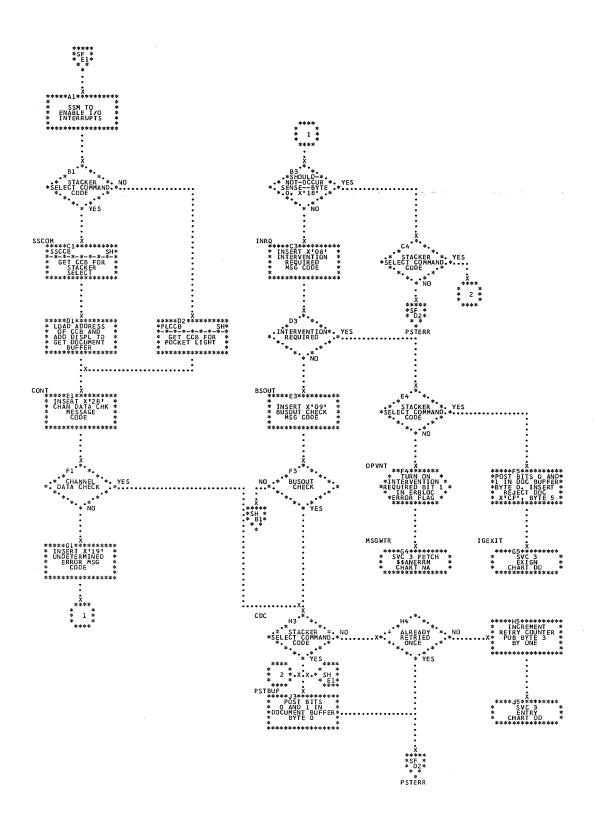


Chart SH. \$\$ANERRW - MICR (1419D) ERP (Part 3 of 3) Refer to Chart 12.

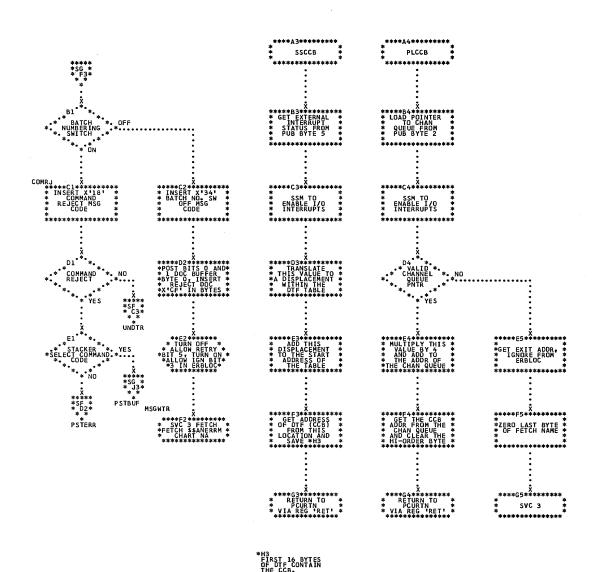


Chart SJ. \$\$ANERRX - 2671 Paper Tape ERP (Part 1 of 2) Refer to Chart 12.

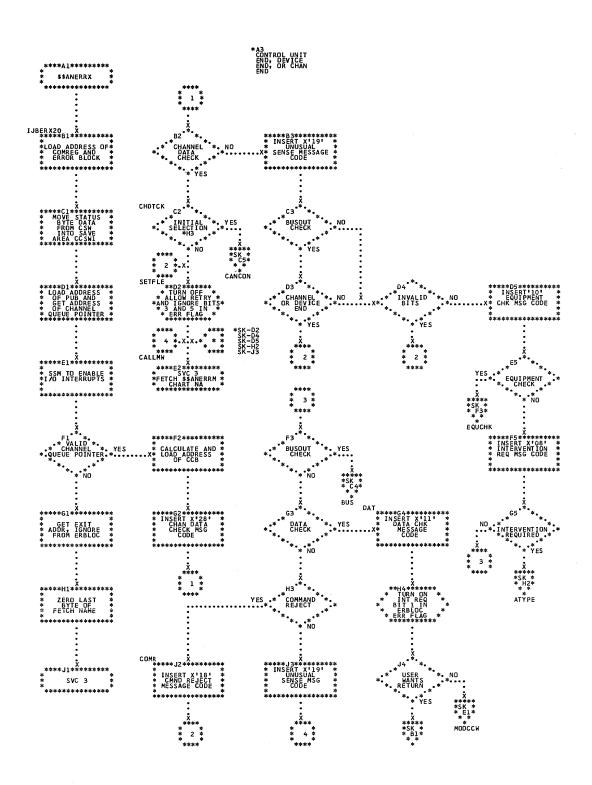


Chart UA. \$\$ANERR9 - Optical Reader ERP (Part 1 of 2) Refer to Chart 11.

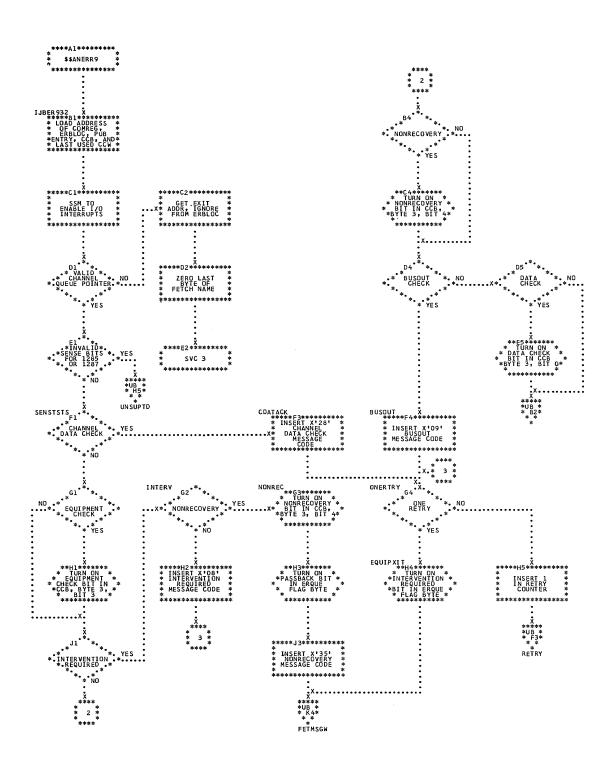


Chart UB. \$\$ANERR9 - Optical Reader ERP (Part 2 of 2) Refer to Chart 11.

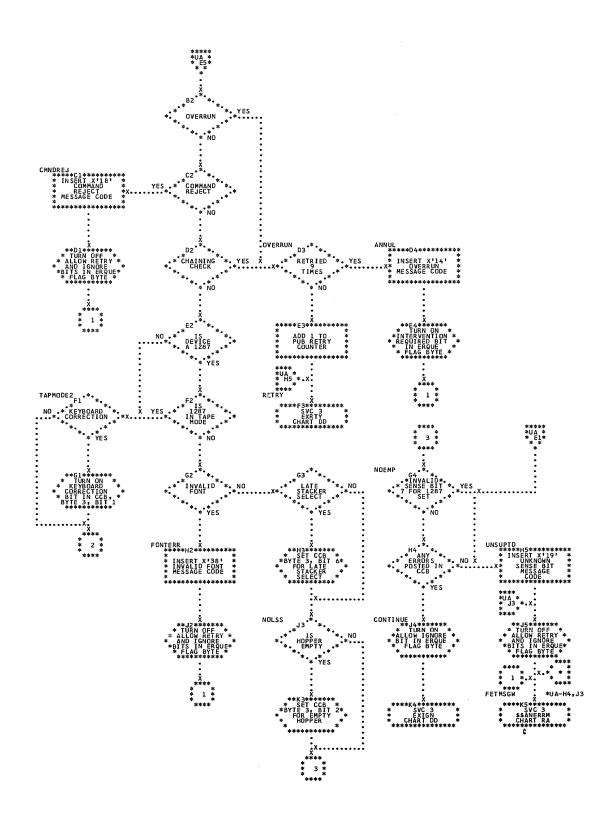


Chart UC. \$\$ANERR6 - Phase 1 of 2495 ERP (Part 1 of 2) Refer to Chart 11.

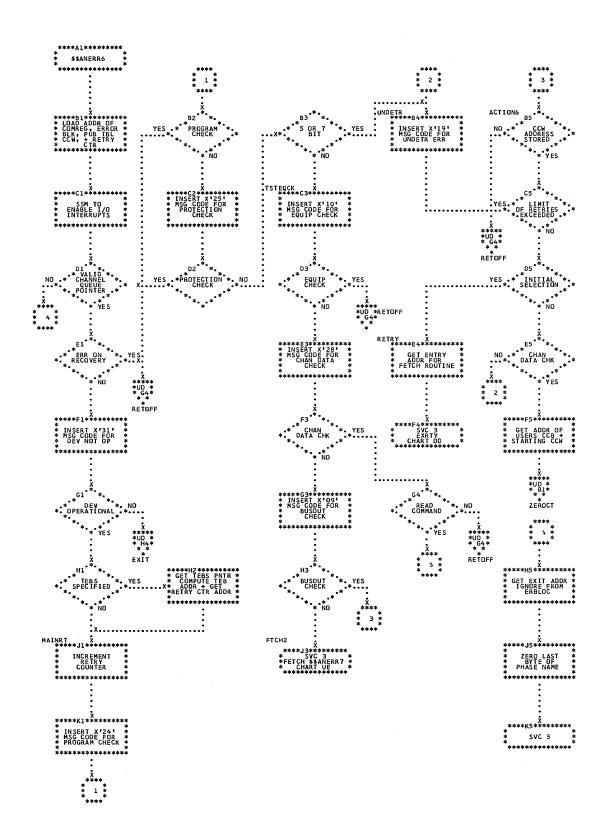


Chart UD. \$\$ANERR6 - Phase 1 of 2495 ERP (Part 2 of 2) Refer to Chart 11.

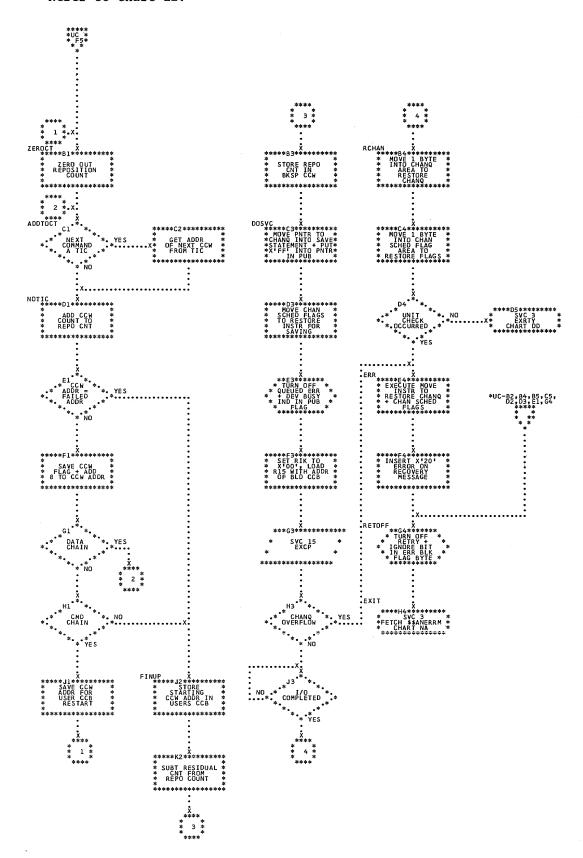


Chart UE. \$\$ANERR7 - Phase 2 of 2495 ERP Refer to Chart 11.

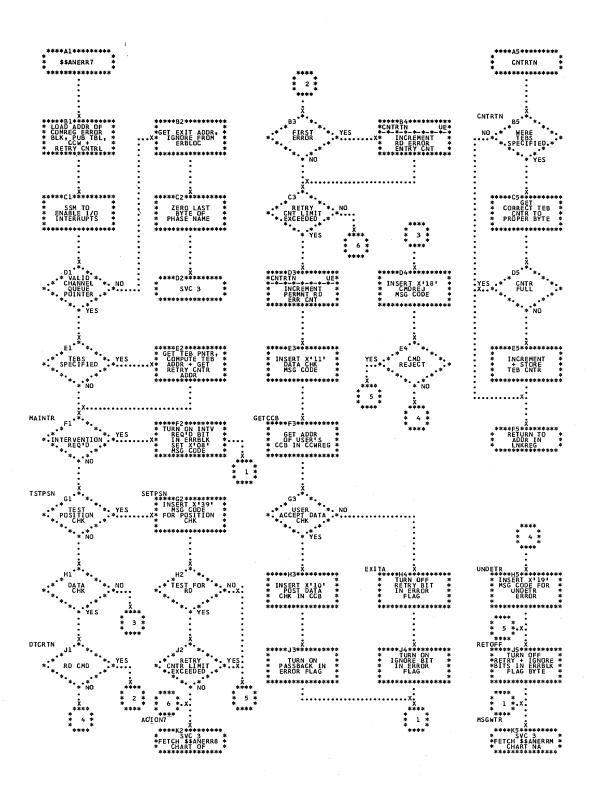


Chart UF. \$\$ANERR8 - Phase 3 of 2495 ERP Refer to Chart 11.

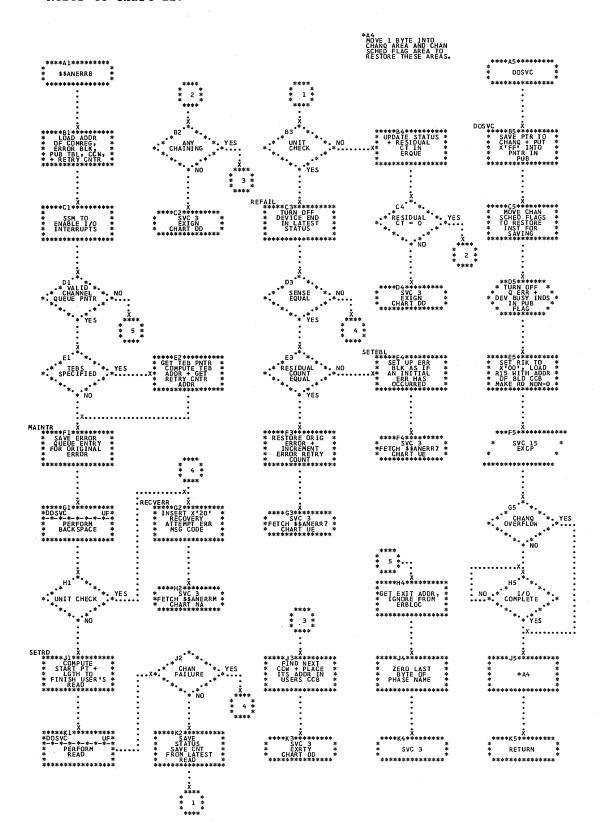


Chart UG. \$\$ANERAI - Phase 1 of 1017/1018 Paper Tape ERP Refer to Chart 12.

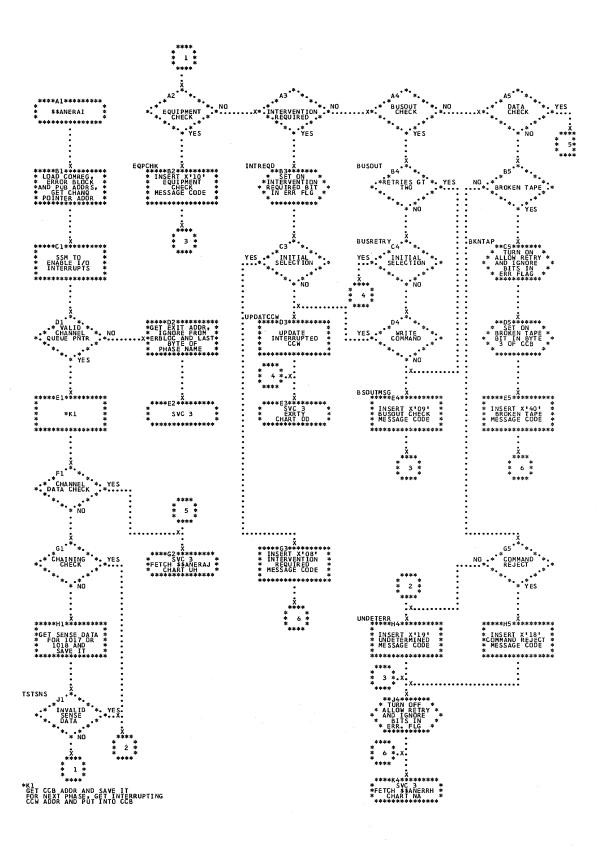


Chart UH. \$\$ANERAJ - Phase 2 of 1017/1018 Paper Tape ERP (Part 1 of 2) Refer to Chart 12.

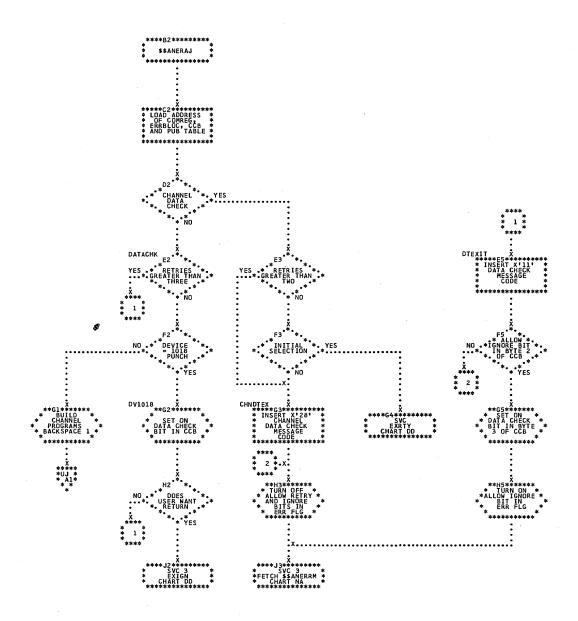


Chart UJ. \$\$ANERAJ - Phase 2 of 1017/1018 Paper Tape ERP (Part 2 of 2) Refer to Chart 12.

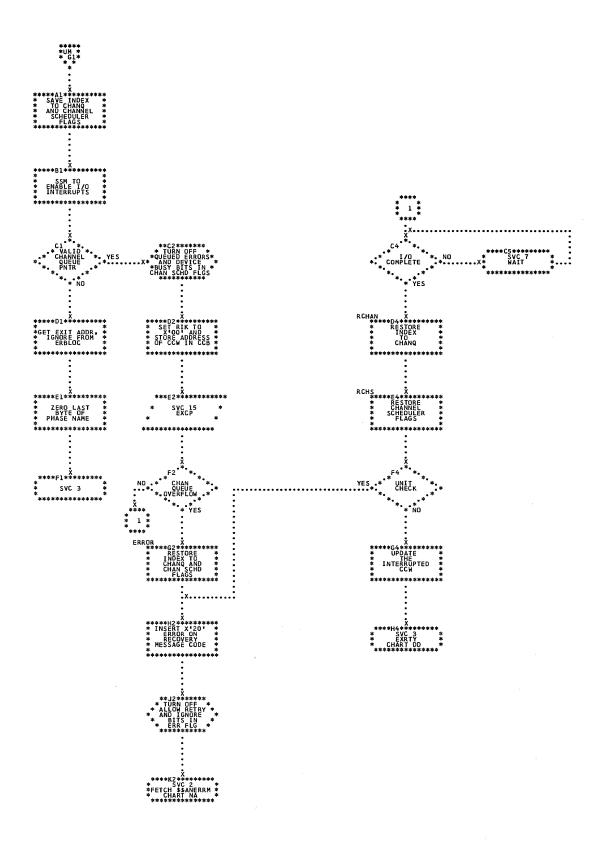
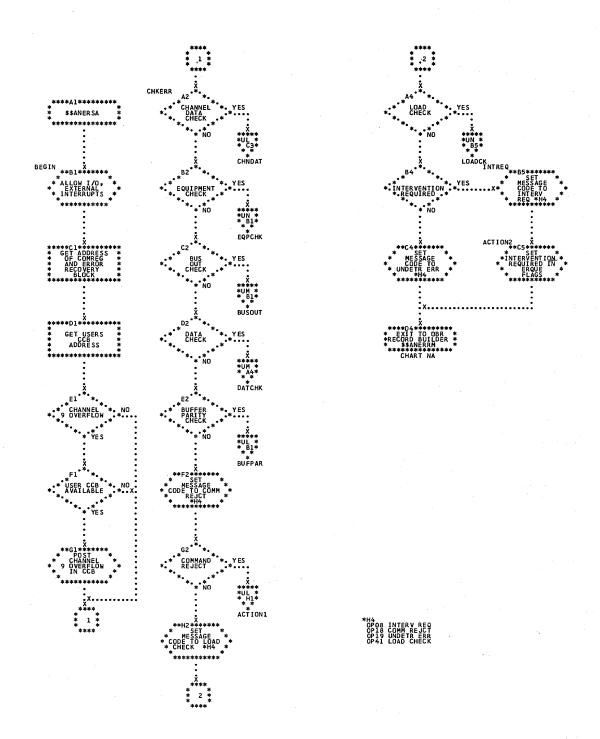


Chart UK. \$\$ANERSA - 3211 Printer ERP (Phase 1) (Part 1 of 4) Refer to Chart 12.



APPENDIX A: LABEL LIST

	Phase or		BJFTST	\$\$ANERR1	TG
<u>Label</u>	<u>Macro</u>	<u>Chart</u>	BKNTAP	\$\$ANERAI	UG
			BLDERPIB	\$\$RAST00	V D
AACT	\$\$ANERRU	SC	BLDLAST	\$\$RAST01	VK
AACTION	\$\$ANERRP	RF	BLDREC	\$\$RAST01	VF
ABTRANS	SGDFCH	EC	BLDREC	\$\$RAST02	WC
ACTIONA	\$\$ANERRP	RE	BLDREC1	\$\$RAST02	WС
ACTION1	\$\$ANERSA	UL	BSOUT	\$\$ANERRW	SG
ACTION1C	\$\$RAST04	XB	BSOUTMSG	\$\$ANERAI	ŬĠ
ACTION1C	\$\$RAST05	XF	BSTTST	SGUNCK	DA
ACTION2	\$\$ANERSA	UK	BTAM	\$\$ANERRC	MM
ACTION3	\$\$ANERSA	UM	BUFPAR	\$\$ANERSA	\mathtt{UL}
ACTION3	\$\$RAST04	XB	BUS	\$\$ANERRX	SK
ACTION3	\$\$RAST05	XF	BUSOUT	\$\$ANERRA	NLA
ACTION4	\$\$ANERSA	UN	BUSOUT	\$\$ANERRV	SE
ACTION4	\$\$RAST04	XC	BUSOUT	\$\$ANERRW	SF
ACTION4	\$\$RAST05	XF	BUSOUT	\$\$ANERR9	UΑ
ACTION4A	\$\$ANERSA	UM	BUSOUT	\$\$ANERAI	UG
ACTION4B	\$\$ANERSA	UN	BUSOUT	\$\$ANERSA	UM
ACTION5	\$\$ANERSA	UL	BUSRETRY	\$\$ANERAI	UG
ACTION5	\$\$RAST04	XB	BUS1	\$\$ANERRV	SE
ACTION5	\$\$RAST 05	XF	BUS2	\$\$ANERRV	SE
ACTION6	\$\$ANERSA	UL	BYCNL	\$\$ANERRZ	TD
ACTION6	\$\$ANERR6	UC .	BY1	\$\$ANERRM	NВ
ACTION7	\$\$ANERSA	UM	BZYTEST	\$\$RAST00	ΔE
ACTION7	\$\$ANERR7	UE	B 01	\$\$ANERRG	QΑ
ACTION7A	\$\$ANERSA	UM	B02	\$\$ANERRG	AQ
ACTION 7B	\$\$ANERSA	$\Omega \Gamma$			
ACTION8	\$\$ANERSA	UM			
ACTION8A	\$\$ANERSA	UM	CALFET	SGSVC	FF
ACTNRTN	\$\$RAST10	XL	CALLMW	\$\$ANERRX	SJ
ADDTOCT	\$\$ANERR6	UD	CALLRTA	MCRAS	HB
AFTTIO	SGUNCK	DF	CALLSEC2	\$\$ANERRZ	TC
ALLBND	FOPT	BCA	CALLSEC3	\$\$ANERRY	TB
ALLBND1	FOPT	BCA	CALLO	MCRAS	HB
ANNUL	\$\$ANERR9	UB	CALPH4	\$\$ANERRO	RD
APTEST	\$\$ANERAE	RC	CALPH5	\$\$ANERRP	RF
ARETURN	\$\$RAST04	XB	CANALL	SGTHAP	MM
ARETURN	\$\$RAST05	XF	CANCEL	\$\$ANERR1	TG
ARND1	\$\$ANERRU	SC	CANCEL	\$\$RAST02	WB
ASCEND	\$\$RAST 09	ХJВ	CANCOD	\$\$ANERRS	RL
ATNCNL	SGSVC	FG	CANCON	\$\$ANERRX	SK
ATNRTN	SGTCON	GD	CANJOB	\$\$RAST10	XM
ATYPE	\$\$ANERRV	SE	CANRTN	\$\$ANERRS	RL
ATYPE	\$\$ANERRX	SK	CANTASK	\$\$RAST10	XK
ATYPE	\$\$ANERRN	RB	CANTLP	\$\$ANERRY	TA
A01	\$\$ANERRG	QA	CANXIT	FOPT	BE
A02	\$\$ANERRG	QA	CBGOA	SGSVC	FQ
A03	\$\$ANERRJ	QF	CBMOV	SGSVC	FP
A05	\$\$ANERRJ	QF	CBNON1	SGTCHS	CCA
A06	\$\$ANERRJ	QF	CBNON2	SGTCHS	CCA
A2321	SGTCHS	CH	CBOK	SGSVC	FP
			CBRET	SGTCHS	CC
DATHOO	443 Mmn = =	0.77	CCBQED	SGUNCK	DB
BALMSG	\$\$ANERRJ	QF	CCBSTR	\$\$ANERAB	RA
BALSTCHK	\$\$ANERRJ	QF	CCBUNAV	\$\$ANERAE	RC
BEGIN	\$\$ANERSA	UK	CCDADI	MCRAS	HH
BEGIN	\$\$ANERSA	UP	CCDAMAGE	MCRAS	HD
BEGIN	\$\$ANERSA	UQ	CCDASDCK	MCRAS	НН
BEGIN	\$\$RAST04	XA	CCDASDI	MCRAS	HH
BEGIN	\$\$RAST05	XE	CCDASDLT	MCRAS	НН
BGBAD	\$\$RAST09	XJA	CCDASDTC	MCRAS	HH

CCDEVTST	MCRAS	HE	CMNDREJ	\$\$ANERR9	UB
CCDEXIT	MCRAS	HD	CMR	\$\$ANERRV	SE
CCENTRY1	MCRAS	HD	CNCEL	SGTHAP	MK
CCENTRY2	MCRAS	HE	CNCELL		MK
CCENTRY3	MCRAS	HE	CNCEL0		
					MK
CCEREXIT	MCRAS	HD	CNCEL1		ML
CCEXIT1	MCRAS	HD .	CNCEL1A	SGTHAP	ML
CCEXIT1	\$\$RAST00	VD	CNCEL1B	SGTHAP	ML
CCEXIT2	MCRAS	HE	CNCEL2	SGTHAP	MK
CCEXIT3	MCRAS	HF	CNCEL2AA		MK
CCEXIT4	MCRAS	HF	CNCEL3		ML
CCNOT10	MCRAS	HF	CNCEL4		ML
CCRECRTN	\$\$RAST 01	ΛK	CNCEL5		\mathtt{ML}
CCRTYTST	MCRAS	HE	CNCL	FOPT	BE
CCSETDMC	MCRAS	HD	CNCL	\$\$ANERRU	SC
CCT155	MCRAS	HF	CNCLLOOP		TD
CCWTEST	\$\$RAST11	XN	CNCLSW		TB
				• •	
CDATACK	\$\$ANERR9	UA	CNERPIB	\$\$RAST02	WB
CDC	\$\$ANERRW	SG	CNLSVE		BA
CEDETST	SGTCHS	CL	CNO	\$\$ANERRU	SB
CHAINCH	\$\$ANERRB	NN	CNTEXT	SSANERRP	RE
CHDTCK	\$\$ANERRX	SJ	CNTRTN	\$\$ANERR7	UE
CHECK	\$\$ANERRA	NL	CNTST		SD
				• •	
CHECKLST	\$\$RAST00	VB	CNTST		RB
CHECKMC	\$\$RAST00	٧B	COMBIN	\$\$ANERRA	NL
CHEND	SGTCHS	CL.	COMMENCE	\$\$ANERAD	NK
CHEND1	SGTCHS	\mathtt{CL}	COMPCLC	SGTCHS	CA
CHFAIL	SGUNCK	DF	COMR	\$\$ANERRX	SJ
CHFAIL1	SGUNCK	DF	COMREJ		NN
CHKACTN	\$\$RAST10	XM			SH
	• •		COMRJ	1.1	
CHKADR	\$\$ANERRT	SA	COMRJT	• •	UG
CHKADR	\$\$ANERRW	SF	CONBUF		$_{ m FP}$
CHKADR	\$\$ANERRS	RK	CONBUF 2	SGSVC	\mathbf{FP}
CHKAM	\$\$ANERRB	NN	CONT	\$\$ANERRV	SE
CHKCNT	\$\$ANERRV	SE	CONT		SG
CHKDEV	\$\$ANERRP	RF	CONTINU		LA
	• •				
CHKDISK	\$\$ANERRA	NL	CONTINU	7.7	NG
CHKERQ	\$\$RAST10	XK	CONTINUE	\$\$ANERR9	UΒ
CHKERR	\$\$ANERSA	UK	CONTINUE	\$\$ANERRM	NB
CHKLTA	\$\$ANERRS	RL	CONTROL	\$\$RAST03	WF
CHKMPS	\$\$RAST10	XM	CORCIN	SGTCHS	CK
CHKMSG	\$\$RAST01	VJ ·	CORPUB		CK
CHKMSG	\$\$RAST10	XK	CORPUB	SGTCHS	CK
CHKOCREC	\$\$RAST01	VJ	CORREC		CJ
CHKSNS	\$\$ANERSC	ŪQ	COUNT	SGTCHS	CG
CHKSN1	\$\$ANERSC	UQ	COUNTRG	\$\$ANERRP	RE
CHKTABLE	\$\$RAST01	٧J	COUNTRG	\$\$ANERRQ	RG
CHNDAT	SSANERSA	UL	CQDSP	SGTCHS	CR
CHNDRT	SGTCHS	CP	CSBY2	FOPT	BE
CHNDTEX	\$\$ANERAJ	UH	CSCAN	\$\$RAST04	XA
	• •				
CHNERROR	SMCRR	KA	CSCAN	\$\$RAST05	ΧE
CHNOK1	SGTCHS	CK	CSRST	FOPT	BE
CHNTST	SGTCHS	CP	CSWCHK	SGUNCK	DF
CKCHST	SGTCHS	CE	CSWLOST	\$\$RAST00	VD
CLBPRG	SGTCHS	CA	CUPDATE	\$\$RAST04	ΧA
CLBPTR	SGTCHS	CAA	CUPDATE	\$\$RAST05	XE
CLBSUP	SGTCHS	CAA	CUU	\$\$ANERRO	RD
CLCEX	SGDFCH	EC	CYLEND	SGDSK	GB
CLCINS	SGTCHS	CH	C01	\$\$ANERRG	QΒ
CLEAR	\$\$RAST02	WC	C01	\$\$ANERRH	QD
CLKDMG	\$\$RAST03	WJ	C01	\$\$ANERRJ	QГ
CMDCHN	SGUNCK	DA	C0100	\$\$ANERRV	ŜE
CMDREJ	\$\$ANERRV	SE	C02	\$\$ANERRV	SD
	\$\$ANERRV	SD	-02	A ATTITUTE A	עט
CMDSEQ	ANNTHUCK	UD.			

DASD	ራ <mark>ል</mark> በ እ ርመለን	C.T.N.	ERPIBLUP	MCRAS	HG
	\$\$RAST02	WA			
DASD2311	SGTCHS	CH	ERPIBLUP	\$\$RAST00	\mathbf{v}_{D}
DAT	\$\$ANERRX	SJ	ERPIBU	\$\$RAŞT02	WD
DATAADDR	SGDFCH	EE	ERPMSG	\$\$RAST10	XK
				MCRAS	HG
DATACHK	\$\$ANERRB	NN	ERPUBUPD		
DATACHK	\$\$ANERAJ	UH	ERQSDR	\$\$ANERAC	NF
DATACHK	\$\$ANERSA	UM	ERQUECK	\$\$RAST10	XK
DATACHK1	SSANERSA	UM	ERR	SSANERR6	UD
			ERRGO	FOPT	BB
DATCHK	\$\$ANERRV	SE			
DCERP	\$\$ANERRA	NL	ERROR	\$\$ANERAJ	UJ
DEALSO	SGTCHS	CQ	ERRORQED	\$\$ANERAA	NC
DECCTR	\$\$ANERRQ	RH	ERRQUED	\$\$ANERAF	ИН
DELKOTCK		CN	ERRQUED1	SSANERAG	NJ
	SGTCHS		~		
DEQUE	SGSVC	FF	ERRSEN	SGUNCK	DB
DEQUER	SGUNCK	DE	ERRSET	FOPT	BB
DEQUER1	SGUNCK	DE	ERRSET	FOPT	BB
DEQUER1A	SGUNCK	DE	ERRSET 0	FOPT	ВВ
DESCEND	\$\$RAST09	XJA	ERRSET1	FOPT	BB
DETFRE	SGTHAP	MB	ERRSIO	SGUNCK	DF
DEV2311	\$\$RAST01	VH	ERRSIO2	SGUNCK	\mathtt{DF}
DISWHY	SGTCHS	CK	ERRTYP	\$\$ANERRP	RE
				\$\$ANERRE	PC
DMCTEST	\$\$RAST02	WA	ERR010		
DOSVC	\$\$ANERR6	ŨD	ERR010	\$\$RAST0 7	XН
DOSVC	\$\$ANERR8	UF	ERRO15	\$\$RAST07	XΗ
DOTCH	SGTCHS	CF	ERR020	\$\$RAST07	XН
			ERR030	• •	XH
DRAPIO	\$\$RAST09	XJA		\$\$RAST07	
DSKTST	SGDSK	GA	ERR040	\$\$RAST0 7	XH
DTCH	\$\$ANERRB	NN	ERR050	\$\$RAST07	XН
DTCRTN	SSANERR7	UE	ERR070	SSRAST07	ХJ
	• •			QQIIII O I	
DTEXIT	\$\$ANERAJ	UH		1.1	
D V1017	\$\$ANERAI	UG	ERR080	\$\$ANERRL	PG
DV1018	\$\$ANERAJ	UH	ERR080	\$\$RAST0 7	ХJ
DYNAMIC	\$\$RAST09	XJA	ERR090	SSANERRL	PG
			ERRO90	\$\$RAST07	XJ
DYNREALO	\$\$RAST09	XJA			
			ERR093	\$\$RAST0 7	ХJ
			ERRO94	\$\$ANERRL	PG
EDRDHA	SGDSK	GB	ERR095	\$\$ANERRF	PE
EDRDHA1	SGDSK	GB	ERR095	\$\$ANERRL	PG
				• •	
EDTIC	SGDSK	GB	ERR095	\$\$ANERAP	PN
EDTIC1	SGDSK	GB	ERR095	\$\$ANERAS	PX
EMGENT	MCRAS	HB	ERR096	\$\$ANERRL	PG
EMGIORTN	\$\$RAST01	VK	ERR100	\$\$ANERRB	NN
				• •	
EMGWAIT	MCRAS	HC	ERR102	\$\$ANERRF	PE
END	\$\$ANERRO	TF	ERR1 05	\$\$ANERRB	NN
END	\$\$ANERR1	TG .	ERR105	\$\$ANERRF	PE
ENDPUBS1	\$\$ANERRZ	TC	ERR1 05	\$\$ANERAS	PΧ
			ERR110	\$\$ANERRD	PA
ENDPUBS3	\$\$ANERRZ	TD			
ENTEXT	FOPT	BG	ERR110	\$\$ANERRF	PE
ENTEXT	SGSVC	FL	ERR110	\$\$RAST07	ХJ
ENTIO	FOPT	BF	ERR110	\$\$ANERAS	PX
ENTPCK	FOPT	BA	ERR120	\$\$ANERRD	PA
ENTPCK	SGSVC	FJ	ERR120	\$\$ANERRF	PF
ENTPCK	SGSVC	FK	ERR120	\$\$RAST07	ХJ
ENTSVC	FOPT	BH	ERR140	\$\$ANERRE	PC
EPIBSCAN	\$\$RAST10	XL	ERR145	SSRAST07	ХJ
		•	ERR150	• •	
EQPCHK	\$\$ANERRU	SC		\$\$RAST07	ХJ
EQPCHK	\$\$ANERRV	SD	ERR150	\$\$ANERAP	PN
EQPCHK	\$\$ANERAI	UĞ	ERR150	\$\$ANERAQ	PQ
EQUCHK	\$\$ANERRX	SK	ERR152	\$\$ANERAP	\tilde{PN}
	• •		ERR153	\$\$RAST07	
EQPCHK	\$\$ANERSA	UN			ΧJ
EQPCHK1	\$\$ANERSA	UN	ERR155	\$\$ANERAP	PN
EQUIP	\$\$ANERRA	NL	ERR160	\$\$RAST0 7	XH
EQUIPXIT	\$\$ANERR9	UA	ERR170	\$\$RAST07	XH
	• •		ERR175	\$\$ANERAP	PN
ERPIBCER	MCRAS	HF			
ERPIBCK	\$\$RAST10	XK	ERR180	\$\$ANERAP	PN .
ERPIBFIL	MCRAS	HF	ERR20	\$\$ANERRA	NL

ERR200	\$\$ANERRF	\mathbf{PE}		ERR6 05	SSANERAP	PP
ERR201	SSANERAO	PQ		ERR610	SSANERAP	PP
ERR205	\$\$ANERAQ	PQ		ERR640	\$ \$ ANERR F	PF
ERR205	\$\$ANERAL	PÜ		ERR650	\$\$ANERRE	PC
ERR208	\$\$ANERRF	PE		ERR650	SSANERRF	PF
ERR210	\$\$RAST07	XH		ERR650	\$\$ANERRL	PG
ERR210	\$\$ANERAQ	PQ		ERR655	\$\$ANERRL	PG
ERR215	\$\$ANERAQ	PQ		ERR655	\$\$ANERAN	PL
ERR220	\$\$ANERRF	PE		ERR658	\$ \$ ANERRF	PE
ERR220	\$\$ANERAQ	PQ		ERR658	\$\$ANERRL	PG
ERR240	\$\$ANERAM	$\tilde{\mathrm{PJ}}$		ERR660	\$\$ANERRF	PE
ERR250	\$\$ANERRF	PE		ERR660	\$\$ANERAM	PK
ERR250	\$ \$ ANERAQ	PQ		ERR665	\$\$ANERRF	$_{ m PE}$
ERR251	\$\$ANERAQ	PQ		ERR665	SSANERAM	PK
ERR252				ERR695		PL
	\$\$ANERAQ	PR			\$\$ANERAN	
ERR255	\$\$ANERAM	PK		ERR695	\$\$ANERAQ	PR
ERR255	\$\$ANERAQ	PR		ERR695	\$\$ANERAK	PS
				ERR6 95		PÜ
ERR260	\$\$ANERAQ	PR			\$\$ANERAL	
ERR265	\$\$ANERRF	PE		ERR696	\$ \$ ANERAQ	PR
ERR265	\$\$ANERAL	PU		ERR6 96	\$\$ANERAK	PT
ERR270	\$\$ANERAL	PU			* * * * * * * * * * * * * * * * * * * *	
ERR2 7 5	\$\$ANERAM	РJ		ERR 7 00	\$\$ANERRE	PD
				ERR 7 00	\$\$ANERRF	PF
ERR300	SSANERAK	PS		ERR700	SSANERRL	PH
					· •	
ERR301	\$\$ANERRE	PC		ERR 7 00	\$\$ANERAM	PK
ERR305	\$\$ANERAK	PS		ERR 7 00	\$\$ANERAN	PM
ERR309	SSANERAK	PS		ERR700	\$\$ANERAP	PP
	• •					
ERR310	\$\$ANERAM	РJ		ERR 7 00	\$\$ANERAQ	PR
ERR310	\$ \$ ANERAK	PS		ERR700	\$\$ANERAK	\mathbf{PT}
ERR312	\$\$ANERAK	PS		ERR700	SSANERAR	PW
	AAANEDAK				\$\$ANERAS	PX
ERR314	\$\$ANERAK	PS		ERR 7 00		
ERR315	\$\$ANERAM	PJ		ERR 7 02	\$\$ANERAR	PW
ERR318	\$\$ANERAM	$_{ m PJ}$		ERR 7 03	\$\$ANERRE	PD
ERR320	SSANERAK	PS		ERR703	\$\$ANERAP	PP
	• •				* *	
ERR325	\$\$ANERAK	PS		ERR 7 03	\$\$ANERAQ	PR
ERR326	\$\$ANERAK	PS		ERR 703	\$\$ANERAK	PT
ERR335	SSANERRE	PC		ERR704	SSANERAR	PW
					• •	
ERR340	\$\$ANERRE	PC		ERR 7 05	\$\$ANERRL	PH
ERR340	\$\$ANERAN	PM	•	ERR 7 05	\$\$ANERRL	PH
ERR340	\$\$ANERAK	PS		ERR705	\$\$ANERAM	PK
	JANEKAK Linnari					
ERR341	\$\$ANERAN	PM		ERR705	\$\$ANERAN	PM
ERR350	\$\$ANERRE	PC		ERR 7 05	\$\$ANERAR	PW
ERR350	SSANERRL	PG		ERR 7 06	\$\$ANERRE	PD
				ERR 7 06	SSANERAP	PP
ERR350	\$\$ANERAM	PJ				
ERR350	\$\$ANERAN	PM		ERR707	\$\$ANERAN	PM
ERR350	\$\$ANERAS	PX		ERR 71 0	\$\$ANERRE	PD.
051	\$\$ANERAK			ERR 7 10	\$\$ANERRF	PF
ERR351		PS				
ERR355	\$\$ANERRL	PG		ERR 71 0	\$\$ANERRL	PH
ERR355	\$\$ANERAM	PJ		ERR 7 10	\$\$ANERAM	PK
ERR355	\$\$ANERAN	PM		ERR 71 0	\$\$ANERAQ	PR
					\$\$ANERAP	
ERR360	\$\$ANERRL	PG		ERR711		PP
ERR390	\$\$ANERAP	PN		ERR 71 3	\$\$ANERAP	$_{ m PP}$
ERR395	\$\$ANERRD	PB		ERR 7 15	\$\$ANERRF	PF
				ERR 7 15	\$\$ANERAR	
ERR396	\$\$ANERRD	PB				PW
ERR400	\$\$ANERAS	PX		ERR 7 20	\$\$ANERRF	\mathbf{PF}
ERR401	\$\$ANERAS	PΧ		ERR 7 20	\$\$ANERRL	PH
ERR402	\$\$ANERAS	PX		ERR 7 20	\$\$ANERAM	PK
ERR405	\$\$ANERRD	PA		ERR 7 20	\$\$ANERAQ	PR
ERR405	\$\$ANERAP	PN		ERR722	\$\$ANERRE	PC
ERR406	\$\$ANERAN	PL		ERR722	\$\$ANERRL	PG
ERR408	\$\$ANERAN	$_{ m PL}$		ERR 7 55	\$\$ANERAN	PL
ERR410	\$\$ANERAS	PΧ		ERR 760	\$\$ANERAQ	PQ
ERR412	\$\$ANERRL	PG		ERR760	\$\$ANERAK	PS
	1 1	PL		ERR760	\$\$ANERAL	PU
ERR412	\$\$ANERAN					
ERR600	\$\$ANERRE	PC		ERR805	\$\$ANERAL	ÞΩ
ERR600	\$\$ANERAP	PP		ERR820	\$\$ANERAL	PV
	T T	- -				

ERR825 ERR840 ERR842 ERR870 ESTVOUT ESTVOUT1 EXCPIGN EXCP1GN EXCP10 EXCP2 EXCP3 EXCP5 EXCP5	\$\$ANERAL \$\$ANERAL \$\$ANERAL \$\$ANERAL SGTCHS SGTCHS SGTCHS SGTCHS SGTCHS SGTCHS SGTCHS SGTCHS SGTCHS	PV PV PU CG CG CAA CB CA CB CA CB CCA CB	FETCH FETMSGW FGP FILEPR FINDPUBL FINDTASK FINDTOD FINUP FIODONE FLPTR FNDQUE FNDQUE1 FONTERR	\$\$RAST10 \$\$ANERR9 SGDFCH \$\$ANERRB \$\$ANERRZ \$\$RAST02 \$\$RAST01 \$\$ANERR6 SGDFCH SGTCHS SGTCHS SGTCHS \$GTCHS	XL UB EC NN TC WB VF UD EH CC CCA CD UB
EXCP 6P	SGTCHS	CAA	FREDEV	SGTCHS	CP
EXCP7	SGTCHS	CA	FREDEV1	SGTCHS	CP
EXINTR	\$\$ANERRR	RJ	FREE	\$\$RAST10	XK
EXIT EXIT	SGTCHS SSANERRC	CG NM	FSAVALID FTCH2	\$\$RAST03 \$\$ANERR6	WG UC
EXIT	\$\$ANERRS	RK	FTHMSGW	\$\$ANERRU	SC
EXIT	\$\$ANERRZ	TC	F01	\$\$ANERRG	QB .
EXIT	\$\$ANERR1	TG	F010	\$\$ANERRG	QB
EXIT	\$\$ANERR6	UD	F02	\$\$ANERRG	QB
EXIT	\$\$RAST02	WD	F03	\$\$ANERRG	QB
EXITA EXITA	\$\$ANERRA \$\$ANERRS	NLA RL	F1EUTEST F2EUTEST	SGUNCK SGUNCK	DB DB
EXITA	\$\$ANERR7	UE	121011101	booner	טט
EXITAB	\$\$ANERRB	NN			
EXITB	\$\$ANERRA	NLA	GELNGTH	\$\$RAST01	VF
EXITB	\$\$ANERRS	RL	GENENT	FOPT	BF
EXITBB EXITC	\$\$ANERRB \$\$ANERRA	NN NLA	GENENT GEN1	FOPT FOPT	BF BF
EXITRTN	\$\$RAST09	XJA	GEN1	FOPT	BG
EXITRTN	\$\$RAST10	XL	GETBND	\$\$RAST03	HW
EXITRTN	\$\$RAST00	ΛC	GETCCB	\$\$ANERR7	UE
EXITRTN	\$\$RAST01	VJ	GETCHQ	SGTCHS	CK WC
EXITRTN EXITRTN	\$\$RAST03 \$\$RAST11	WH XN	GETCMD GETCOM	\$\$RAST02 \$\$RAST02	WD
EXIT1	SGDFCH	EH	GETENTRY	SGDFCH	EE
EXIT1	\$\$ANERRO	TF	GETJIB	SGTCHS	CH
EXIT1	\$\$RAST03	WH	GETMSG	\$\$ANERRV	SE
EXIT1 EXIT2	\$\$RAST10	XL TF	GETPIB GETPIB1	SGTCHS	CR CR
EXPAND	\$\$ANERRO SGDFCH	EE	GETSEN	SGTCHS SGUNCK	DB
EXTEOJ	FOPT	BE	GIDCK1	\$\$ANERRZ	TD
EXTRAN	SGUNCK	DC	GIOADR	SGTCHS	CE
EXTRT1	SGSVC	FJ	GIOADR	SGTCHS	CF
EXTRT1 EXT01	SGSVC FOPT	FN BD	GO GO	\$\$ANERRJ \$\$ANERRJ	QF QF
EXTO2	FOPT	BC	GO	\$\$ANERRP	RE
EXT03	FOPT	BC	GO	\$\$ANERRQ	RG
EXT04	FOPT	BD	GOMCRR	SEND	LA
EXT1	SGSVC	FL	GOQUIET	\$\$RAST03	WJ
EXT2 E050	SGSVC \$\$ANERRI	FM QE	GOTCDMR GOTCLB	\$\$RAST01 SGTCHS	VG CH
E051	\$\$ANERRI	QE	GOTREQID	\$\$RAST02	WD
E06	\$\$ANERRI	QE	GTSEN1	SGUNCK	DB
E062	\$\$ANERRI	QE	G01	\$\$ANERRG	QB
FCHRT1	SGDFCH	EA	HALT	SGTCHS	CD
FCHRT2 FCHRT3	SGDFCH SGDFCH	EA EA	HALTLOOP HANDLECC	SGTCHS \$\$RAST00	CD VB
FCHRT4	SGDFCH	EA	HANDLEMC	\$\$RAST00	VB
FCH2260L	\$\$ANERRC	NM	HANDLEMC	\$\$RAST03	WE
FCH3	SGSVC	FF	HARDCHAN	SGUNCK	DG
FETCH	\$\$RAST01	VJ	HARDWAIT	\$\$RAST00	VВ

HEADQUE	ŚŚANERAA	NC	INVAL	\$\$ANERRY	\mathbf{T} B
HEADQUE1	\$\$ANERAC	NF	INVALID	\$\$RAST10	MX
HEADQUE2	\$\$ANERAF	NH	IOCOMP	\$\$ANERRQ	RH
HEADQUE 3	\$\$ANERAG	NJ	IODONE	\$\$ANERRP	RF
HOLDQUE	\$ \$ ANERRY	TA	IOERR	\$\$ANERRH	QD
HRDWAIT	\$\$RAST00	٧A	IOERR	\$\$ANERRI	QE ·
H01	\$\$ANERRV	SE	IOERR	\$\$ANERRJ	QG
H01	\$\$ANERRG	QB	IOERR	\$\$ANERRP	RF
H1RRTN	\$\$RAST03	WE	IOINTR	\$\$ANERRR	RJ
			IONOP	SGUNCK	DA
				SGSVC	FF
			IOPSET		
IDRAEXT	FOPT	BD	IORTN	\$ \$ ANERRI	QE
IDRAFCH	SGDFCH	EB	IORTN	\$\$ANERRJ	QG
IDRAOK	SGDFCH	EDC	TIAWOI	\$\$ANERSB	UP
IDRANOPQ	SGDFCH	EA	TIAWOI	\$\$ANERSC	UR
IDRAST1		EA	IPLEXIT	• •	VC
	SGDFCH			\$\$RAST00	
IDRAST2	SGDFCH	EF	IREXIT	\$\$ANERRT	SA
IDRAST3	SGDFCH	EF	IREXIT	\$\$ANERRW	SF
				• •	
IGEXIT	\$\$ANERRS	RK	ISSVC51	SGDFCH	EDB
IGEXIT	\$\$ANERRW	SF	ISSVC51	SGDFCH	EDC
IGEXIT	SSANERRW	SG			
	• •				
IGNCAN	\$\$ANERRS	\mathtt{RL}			
IGON	\$\$ANERRU	SB			
	• •		73 F17 F 17	70.D#	D. 7.7
IJBERA35	\$\$ANERRA	NL	JAENTRY	FOPT	BK
IJBERB33	\$\$ANERRB	NN	JAISBND	FOPT	BK
IJBERB35	\$\$ANERAB	RA	JAISPP	FOPT	BK
· ·					
IJBERC35	\$\$ANERRC	NM	JANOTSUP	FOPT	BK
IJBERG 20	SSANERRG	QΆ	JASETSP	FOPT	BC
	, , ,				
IJBERH20	\$\$ANERRH	QD	JAXIT	FOPT	\mathtt{BL}
IJBERI 20	\$\$ANERRI	QE	JAXITBR	FOPT	BC
IJBERJ24	\$\$ANERRJ	QF	JIBTYP	SGTCHS	CJ
IJBERK20	\$\$ANERRK	QH			
IJBERN33	\$\$ANERRN	RB			
	• •				
IJBERO35	\$\$ANERRO	RD	KEYINT	\$\$ANERRR	RJ
IJBERP33	\$\$ANERRP	RE	KR TY	\$\$ANERRS	RK
	• •	RG	K01	• •	
IJBERQ33	\$ \$ANERRQ		VOI	\$\$ANERRG	QB
IJBERR20	\$\$ANERRR	RĴ			
IJBERS34	\$\$ANERRS	RK			
	• •				
IJBERT20	\$\$ANERRT	SA	LACSW	\$\$ANERRO	RD
IJBERU33	\$\$ANERRU	SB	LASPH	\$\$ANERRA	NL
IJBERV20	\$\$ANERRV	SD	LASPHAS	SSANERRC	NM
				• •	
IJBERX20	\$\$ANERRX	SJ	LASTRACK	\$\$RAST01	VH
IJBER535	SSANERAF	NG	LASTREC	\$\$RAST01	VH
	* *				
IJBER635	\$\$ANERAG	ŊĴ	LCIDAR	SGDFCH	EC
IJBER932	\$\$ANERR9	UA	LDPSW	\$\$ANERRR	RJ
IJBMVC33	\$\$ANERR1	TG	LDRAST00	SSRAST01	۷J
IJBPA134	\$\$ANERRZ	TC	LDRAST02	\$\$RAST00	ΔD
IJBPA233	\$\$ANERRY	TA	LDRAST02	\$\$RAST01	VJ.
IJBPA333	\$\$ANERRO	TE	LDREGS	SGTCHS	CK
	• • •				
INDIB	SGTCHS	CJ	$_{ m LGD}$	SGTCHS	CH
INÉRRCNT	\$\$ANERAI	UG	LGDD	SGTCHS	CH
	• •				
INHWRITE	SGTCHS	CH	LGDD1	SGTCHS	CH
INITCHN1	SGTCHS	CP	LGD1	SGTCHS	CH
INITRG	SGTCHS	CP	LMERA	FOPT	BCA
INITSIO	SGTCHS	CN	LOADCK	\$\$ANERSA	UN
INRQ	\$\$ANERRW	SG	LOADMOD	\$\$RAST00	۷C
				11	
INSERT	\$\$ANERRB	NN	LOADMOD	\$\$RAST01	٧J
INST	SEND	${f L}{f D}$	LOADMOD	\$\$RAST03	WH
INTERRCC		MK	LOADPSW	\$\$ANERRR	RJ
	SGTHAD	1.777			
INTERV	SGTHAP	FT 70			
INTPUBSC	SGTHAP \$\$ANERR9	ΑU	LOADTEST	\$\$RAST00	VC
	\$\$ANERR9		,	• •	
TNIMDEA	\$\$ANERR9 SGTCHS	CK	LOADTEST	\$\$RAST01	۷J
INTREQ	\$\$ANERR9 SGTCHS \$\$ANERRU	CK SC	LOADTEST LOADTEST	\$\$RAST01 \$\$RAST03	VJ WH
INTREQ INTREQ	\$\$ANERR9 SGTCHS	CK	LOADTEST	\$\$RAST01	۷J
INTREQ	\$\$ANERR9 SGTCHS \$\$ANERRU \$\$ANERRV	CK SC SD	LOADTEST LOADTEST LOAD00	\$\$RAST01 \$\$RAST03 \$\$RAST00	VJ WH VA
INTREQ INTREQ	\$\$ANERR9 SGTCHS \$\$ANERRU \$\$ANERRV \$\$ANERSA	CK SC SD UK	LOADTEST LOADTEST LOAD00 LOAD01	\$\$RAST01 \$\$RAST03 \$\$RAST00 \$\$RAST01	VJ WH VA VF
INTREQ	\$\$ANERR9 SGTCHS \$\$ANERRU \$\$ANERRV	CK SC SD UK UG	LOADTEST LOADTEST LOAD00	\$\$RAST01 \$\$RAST03 \$\$RAST00 \$\$RAST01 \$\$RAST03	VJ WH VA
INTREQ INTREQ INTREQD	\$\$ANERR9 SGTCHS \$\$ANERRU \$\$ANERRV \$\$ANERSA \$\$ANERAI	CK SC SD UK UG	LOADTEST LOADTEST LOAD00 LOAD01 LOAD03	\$\$RAST01 \$\$RAST03 \$\$RAST00 \$\$RAST01 \$\$RAST03	VJ WH VA VF WE
INTREQ INTREQ INTREQD INTRTN	\$\$ANERR9 SGTCHS \$\$ANERRU \$\$ANERRV \$\$ANERSA \$\$ANERAI SGTCHS	CK SC SD UK UG CK	LOADTEST LOADTEST LOAD00 LOAD01 LOAD03 LOAD09	\$\$RAST01 \$\$RAST03 \$\$RAST00 \$\$RAST01 \$\$RAST03 \$\$RAST09	VJ WH VA VF WE XJA
INTREQ INTREQ INTREQD	\$\$ANERR9 SGTCHS \$\$ANERRU \$\$ANERRV \$\$ANERSA \$\$ANERAI	CK SC SD UK UG	LOADTEST LOADTEST LOAD00 LOAD01 LOAD03	\$\$RAST01 \$\$RAST03 \$\$RAST00 \$\$RAST01 \$\$RAST03	VJ WH VA VF WE

LOGENT	\$\$ANERRP	RE	MCRNTBSY	SMCRR	KC
LOGENT	\$\$ANERRQ	RG	MCRNTCIB	SMCRR	KF
		SC			
LOGERP	\$\$ANERRU		MCRNTLTA	SMCRR	KG
LOGLOOP	\$\$RAST09	ХJА	MCRNTSUP	SMCRR	KE
LOGLOOP	\$\$RAST11	XN	MCROBRRT	SMCRR	КJ
LOGPRC	SGTCHS	CFA	MCRPARIT	SGUNCK	DG
LOGPRC1	SGTCHS	CG	MCRRBST	SMCRR	KG
LOGPRC 2	SGTCHS	CG	MCRRCHER	SMCRR	KA
LOGRTN	\$\$ANERRY	TA	MCRRCPU	SMCRR	KG
LOGTST	\$\$ANERRU	SC	MCRRDIAG	\$\$A\$SUP1	KB
LOGTST	\$\$ANERRY	TA	MCRRRTN	SMCRR	ΚA
LOGWAIT	\$\$ANERRY	TA	MCRRTSTO	\$\$A\$SUP1	KB
LOG1	\$\$ANERRY	TA	MCRSAFTR	SMCRR	KG
LOG2	\$\$ANERRY	TA	MCRSCNCH	SMCRR	KA
LOOKUP	SGDFCH	ED	MCRSCPHM	SMCRR	KH
LOOP1			MCKSCFIIM	SMCKK	KII
	\$\$ANERAE	RC	MODORI 1	443 40IID1	TT TO
LOWBITON	\$\$RAST11	XN	MCRSEL1	\$\$A\$SUP1	KB
LSTDIB	SGTCHS	CJ	MCRSEL2	\$\$A\$SUP1	KB
LTA	SEND	LH	MCRSENDD	SGUNCK	DG
LTABSY	SGSVC	FD	MCRSPSW2	SMCRR	KH
LTACCB	\$\$ANERRM	NB	MCRSUPIK	SMCRR	ΚJ
LTACNL	FOPT	BB	MCRSUPSW	SMCRR	KE
LTARTRN	FOPT	BE	MCSCHDL	MCRAS	HA
LTKHLD	\$\$ANERRZ	TD	MCSELECT	SMCRR	KF
L01	\$\$ANERRG	QC	MCSOFT	MCRAS	HA
L01	\$\$ANERRI	QE	MCTASK	MCRAS	HA
201	φφιιινατικά	51	MESG	\$\$ANERRB	NN
			MESSWTR	\$\$RAST11	XN
MAGUER	COUNCE	D.G.			
MACHEK	SGUNCK	DG	MODCCW	\$\$ANERRX	SK
MACHEK	SGUNCK	DG	MODESTAT	\$\$RAST03	WJ
MACHEK	SGUNCK	DG	MODIFY	SEND	\mathbf{LF}
MACHEK1	SGUNCK	DG	MOVELIST	\$\$ANERAD	NK
MAINRT	\$\$ANERR6	UC	MOVENAME	\$\$ANERRM	NB
MAINTASK	\$\$ANERR1	TG	MOVIDRA	SGDFCH	EDC
MAINTR	\$\$ANERR7	UE	MOVNAM	\$\$ANERRM	NA
MAINTR	\$\$ANERR8	UF	MOVRIK	SGDFCH	EDB
MCCPUEX1	SMCRR	KG	MOVRIK	SGDFCH	EDC
MCMVLGOT	SMCRR	KE	MPSTASK	\$\$RAST01	VG
MCNOTSP	SMCRR	KC	MPSTST	\$\$ANERRN	RB
MCPDCOND	MCRAS	HA	MPSTST	\$\$ANERRQ	RG
MCRBUMP	SMCRR	KE	MPSYES	SGTCHS	CN
MCRCHDMG	SMCRR	KA	MSGNTR	\$\$ANERRW	SF
MCRCHMVN	SMCRR	KD		\$\$ANERRT	SA
			MSGWTR		
MCRCHNBC	SMCRR	KD	MSGWTR	\$\$ANERRV	SE
MCRCHNDM	\$\$A\$SUP1	KB	MSGWTR	\$\$ANERRW	SG
MCRCNCOD	SMCRR	KE	MSGWTR	\$\$ANERRW	SH
MCRCPUEX	SMCRR	KG	MSGWTR	\$\$ANERR7	UE
MCRDVDMG	SMCRR	KD	MSGWTR	\$\$ANERRG	QΑ
MCREND01	SMCRR	KD	MSGWTR	\$\$ANERRH	QD
MCREND 02	SMCRR	KE	MSGWTR	\$\$ANERRI	QΕ
MCREND03	SMCRR	KG	MSGWTR	\$\$ANERRJ	\mathbf{QF}
MCREND 04	SMCRR	KH	MSGWTR	\$\$ANERRK	QH
MCRENTER	SGUNCK	DG	MSG2	\$\$ANERAB	RA
MCRETURN	SMCRR	KC	MSG3	\$\$ANERAB	RA
MCRFULL	SMCRR	KF	MSG4	\$\$ANERAB	RA
MCRGTFDV	\$\$A\$SUP1	KB	MVC	\$\$ANERR1	TG
MCRGTLST	SMCRR	KD	MVCCW	SGTCHS	CCA
MCRGTPIB	SMCRR	KE	MVEPSW	SGUNCK	DF
MCRLOOP1	SMCRR	KA	MVMSG	\$\$ANERRV	SD
MCRLOOP2	\$\$A\$SUP1	KB	MVZEX	SGUNCK	DB
MCRLOOP3	SMCRR	KG	M01	\$\$ANERRG	QC
MCRMPX	SMCRR	KA	M01	\$\$ANERRI	QΕ
MCRMPXST	\$\$A\$SUP1	KB	M01	\$\$ANERRK	QН
MCRNEQLD	SMCRR	KF			
MCRNLTA	SMCRR	KG			
MCRNODMG	SMCRR	KD			

MADOLIA						
MITTER CHIEF	\$\$ANERRC	NM		OBRBYPS	\$\$ANERRM	NA
NDEQUE					3.3	
NEXTCYL	\$\$RAST01	VH		OBREXIT	\$\$ANERAA	ND
NEXTPH	\$\$ANERAE	RC		OBRICE	\$\$ANERAA	NC
NGTMBP	SGSVC	FG		OBRIOE1	\$\$ANERAA	ND
NOAP	\$\$ANERRZ	${f T}{f D}$		OBRIO2	\$\$ANERAA	NC
NOAP1	SSANERRZ	TC		OBRIO3	SSANERAA	NC
NOCANCEL	\$\$RAST02	WB		OBRNOCCB	\$\$ANERRM	NB
NOCB	SGTCHS	CN		OBRNOKEY	\$\$ANERRM	NB
NOCCB	\$\$ANERRX	SK		OBRREL	\$\$ANERAA	ND
NOCCB	\$\$RAST02	WC		OBRREL1	\$ \$ ANERAA	ND
NOCCB		RD				
	\$\$ANERRO			OBRSPR	\$\$ANERRM	NA
NOCCB1	SGUNCK	DA		OBRSPR1	\$\$ANERRM	NA
NODEQUE	\$\$ANERRC	NM	•	OFFLINE	SGTCHS	CR
-						
NODEQUE	\$\$ANERAB	RA		OK	\$\$ANERR1	\mathbf{TG}
NOEMP	\$\$ANERR9	UB		OLTPCOMP	SGTCHS	CD
NOLOADAD	SGDFCH	EE		ONERET	\$\$ANERRG	QΑ
NOLOG	\$\$ANERAE	RC ·		ONERTRY	\$\$ANERR9	UA
	• •	RF				EC
NOLOG	\$\$ANERRP			OPCLOSE	SGDFCH	
NOLOG	\$\$ANERRQ	RH		OPFLAG	\$\$ANERRN	RB
NOLSS	\$\$ANERR9	UB		OPTRT1	SGSVC	FM
NOLTA	\$\$ANERAE	RC		OPTRT2	SGS V C	FM
NOLTH	SSANERRM	NB		OPVNT	\$\$ANERRW	SG
NOMSG	\$\$RAST10	\mathtt{XL}		ORERP	\$\$ANERRA	NL
NONREC	\$\$ANERR9	UA		OURSIO	SGUNCK	DF
	• •					
NOPBR	\$\$ANERRQ	RG		OVERRUN	\$\$ANERR9	UB
NOPINS	SGTCHS	CH		OVERUN	\$\$ANERRB	· NN
NOPINSTR	SGTCHS	CH		OVRUN	SSANERRV	SE
				OAKON	SOURTING	313
NOPRNAME	\$\$RAST01	۷G				
NOPUBRS	\$\$ANERAA	NC	*			
				77 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	++77 0700	
NORELOC	SGUNCK	DAA		PARTNOK	\$\$RAST09	XJB
NOQUIS	SGUNCK	DH		PAR40	\$\$ANERRO	\mathbf{TE}
				PAR41	\$\$ANERRO	\mathbf{TE}
NORCD	SGDSK	GA		PAR42	\$\$ANERRO	\mathbf{TE}
NORCFND	\$\$ANERRA	NL		PAR43	\$\$ANERRO	TE
	• •					
NOSO	SGTCHS	CCA		PAR44	\$\$ANERRO	${f TE}$
MOOMADM	001717077					
NOSTART	SGUNCK	DA			SSANERRO	TE
NOSTART	SGUNCK	DA		PAR45	\$\$ANERRO	TE
NOSTART	\$\$ANERRV	SE		PAR45 PAT	\$\$ANERRC	NM
				PAR45		
NOSTATUS NOSWP	\$\$ANERRV SGSVC	SE FG		PAR45 PAT PCHDIB	\$\$ANERRC SGTCHS	NM CJ
NOSTATUS NOSWP NOS01	\$\$ANERRV SGSVC SGTCHS	SE FG CM		PAR45 PAT PCHDIB PCHKSW	\$\$ANERRC SGTCHS FOPT	NM CJ BA
NOSTATUS NOSWP	\$\$ANERRV SGSVC	SE FG		PAR45 PAT PCHDIB	\$\$ANERRC SGTCHS	NM CJ
NOSTATUS NOSWP NOSO1 NOTBONLY	\$\$ANERRV SGSVC SGTCHS SGDFCH	SE FG CM EG		PAR45 PAT PCHDIB PCHKSW PCHKSW	\$\$ANERRC SGTCHS FOPT SGSVC	NM CJ BA FJ
NOSTATUS NOSWP NOSO1 NOTBONLY NOTBSY	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS	SE FG CM EG CL		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC	NM CJ BA FJ FK
NOSTATUS NOSWP NOSO1 NOTBONLY	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS	SE FG CM EG CL CH		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCHKSW	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH	NM CJ BA FJ FK EB
NOSTATUS NOSWP NOSO1 NOTBONLY NOTBSY NOTCLB	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS	SE FG CM EG CL		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC	NM CJ BA FJ FK
NOSTATUS NOSWP NOSO1 NOTBONLY NOTBSY NOTCLB NOTDMC1	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS \$\$RAST02	SE FG CM EG CL CH WC		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCHKSW PCIL1 PCIL2	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH	NM CJ BA FJ FK EB EB
NOSTATUS NOSWP NOSO1 NOTBONLY NOTBSY NOTCLB NOTDMC1 NOTFCH	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS \$\$RAST02 SGSVC	SE FG CM EG CL CH WC FE		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCHLSW PCIL1 PCIL2 PCITRT	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC	NM CJ BA FJ FK EB EB
NOSTATUS NOSWP NOSO1 NOTBONLY NOTBSY NOTCLB NOTDMC1	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS \$\$RAST02	SE FG CM EG CL CH WC		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCHKSW PCIL1 PCIL2	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH	NM CJA FJ FK EB EM SF
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTDMC1 NOTFCH NOTFIRST	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS \$\$RAST02 SGSVC \$\$RAST03	SE FG CM EG CH WC FE WJ		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW	NM CJA FJ FK EB EM SF
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTDMC1 NOTFCH NOTFIRST NOTFOUND	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH	SE FG CM EG CL WC FE WJ ED		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR	NM CJ BA FJ FK EB EB FM SF JH
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTCLB NOTFCH NOTFCH NOTFIRST NOTFOUND NOTFULL	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH \$\$RAST01	SE FG CM EG CH WC FE WJ ED VJ		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAGN	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR SMICR	NM CJ BA FK EB EM SF JH JF
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTDMC1 NOTFCH NOTFIRST NOTFOUND	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS SGTCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH	SE FG CM EG CL WC FE WJ ED		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR	NM CJ BA FJ FK EB EB FM SF JH
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTCLB NOTFCH NOTFCH NOTFIRST NOTFOUND NOTFULL NOTIC	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$TCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH \$\$RAST01 SGTCHS	SE FG CM EG CH WC FE WJ ED VJ CH		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAID	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR SMICR SGDFCH	NM CJ BJ FK EB EM SH JF EE
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTCLB NOTFCH NOTFCH NOTFIRST NOTFOUND NOTFULL NOTIC	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH \$\$RAST01 SGTCHS \$\$ANERR6	SE FG CM EG CH WC FE WJ ED CH UD		PAR45 PAT PCHDIB PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAGN PDAID PDBOCK	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR SMICR SGDFCH SMICR	NM CJA FJKBB EMFHFEF JJEF
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTCLB NOTFCH NOTFCH NOTFIRST NOTFOUND NOTFULL NOTIC	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$TCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH \$\$RAST01 SGTCHS	SE FG CM EG CH WC FE WJ ED VJ CH		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAID	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR SMICR SGDFCH	NM CJ BJ FK EB EM SH JF EE
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NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTCLB NOTFCH NOTFCH NOTFIRST NOTFOUND NOTFULL NOTIC NOTIC NOTIC NOTIC NOTMPS NOTPD	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$TCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH \$\$RAST01 \$\$TCHS \$\$ANERR6 \$\$RAST11 FOPT	SE FG CM EG CH WC FE WD CH UD XN BH		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAGN PDAID PDBOCK PDBUFL PDCCBPT	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR SMICR SGDFCH SMICR SMICR SMICR SMICR SMICR SMICR SMICR SMICR SMICR SMICR SMICR SMICR	NM CJA FFEEEE SJJEEFB FB
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NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTDMC1 NOTFCH NOTFIRST NOTFOUND NOTFULL NOTIC NOTIC NOTIC NOTMPS NOTPD NOTPD1 NOTPD1 NOTRIA NOT2314 NRFRTY NRTASTO NTFTCH NXTERPIB NXT1 N01 N01	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$TCHS \$\$RAST 02 SGSVC \$\$RAST 03 SGDFCH \$\$RAST 01 SGTCHS \$\$ANERR6 \$\$RAST11 FOPT FOPT SGTCHS SEND \$\$ANERRJ SGTCHS SGUNCK \$\$RAST10 SGTCHS \$\$ANERRJ SGTCHS \$\$ANERRJ \$\$RAST10 \$\$ANERRJ \$\$RAST10 \$\$ANERRJ	SE FM CCCWFWDJHDNHHKEFECKGC QF		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAGN PDAID PDBOCK PDBUFL PDCCBPT PDCCBT PDCHAN PDCHAN PDCHAN PDCHAN PDCSWST PDCSWST PDCSWST PDDEQUE PDDEQUE1 PDDEQUE2 PDDFLT	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR SMIC	NO A J K B B M F H F E F B B B E F E D F G G G F F D J J J J J J J J J J J J J J J J J
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTDMC1 NOTFCH NOTFIRST NOTFOUND NOTFULL NOTIC NOTIC NOTIC NOTMPS NOTPD NOTPD1 NOTPD1 NOTRIA NOT2314 NRFRTY NRTASTO NTFTCH NXTERPIB NXT1 N01 N01	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$TCHS \$\$RAST 02 SGSVC \$\$RAST 03 SGDFCH \$\$RAST 01 SGTCHS \$\$ANERR6 \$\$RAST11 FOPT FOPT SGTCHS SEND \$\$ANERRJ SGTCHS SGUNCK \$\$RAST10 SGTCHS \$\$ANERRJ SGTCHS \$\$ANERRJ \$\$RAST10 \$\$ANERRJ \$\$RAST10 \$\$ANERRJ	SE FM CCCWFWDJHDNHHKEFECKGC QF		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAGN PDAID PDBOCK PDBUFL PDCCBPT PDCCBT PDCHAN PDCOMP PDCSWST PDCSWST PDCSWST PDDEQUE PDDEQUE2 PDDFLT PDEDLT PDERXT1	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$MICR S	M J A J K B B M F H F E F B B B E F E D F G G G F B E J D J J J J J J J J J F J
NOSTATUS NOSWP NOSO1 NOTBONLY NOTBSY NOTCLB NOTCLB NOTFCH NOTFIRST NOTFOUND NOTFILL NOTIC NOTIC NOTIC NOTHPS NOTPD NOTPD1 NOTPD1 NOTRIA NOT2314 NRFRTY NRTASTO NTFTCH NXTERPIB NXT1 N01 N01 N01 N01 N1114	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$TCHS \$\$RAST02 SGSVC \$\$RAST03 SGDFCH \$\$RAST01 SGTCHS \$\$ANERR6 \$\$RAST11 FOPT FOPT SGTCHS SEND \$\$ANERRJ SGTCHS SGUNCK \$\$RAST10 SGTCHS SGUNCK \$\$RAST10 SGTCHS SGUNCK \$\$RAST10 SGTCHS	SE FM GLHCEJDJHDNHHKEFECKGCFQ		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAGN PDAID PDBOCK PDBUFL PDCCBPT PDCCBT PDCHAN PDCHAN PDCOMP PDCSWST PDCSWST PDCSWST PDCSWST PDCSWST PDDEQUE1 PDDEQUE2 PDDFLT PDERXT1 PDERXT1	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$\$ANERRW SMICR SMIC	M J A J K B B M F H F E F B B B E F E D F G G G F B E F D J D J J J J J J J J J J J J J J J J J
NOSTATUS NOSWP NOS01 NOTBONLY NOTBSY NOTCLB NOTDMC1 NOTFCH NOTFIRST NOTFOUND NOTFULL NOTIC NOTIC NOTIC NOTMPS NOTPD NOTPD1 NOTPD1 NOTRIA NOT2314 NRFRTY NRTASTO NTFTCH NXTERPIB NXT1 N01 N01	\$\$ANERRV SGSVC SGTCHS SGDFCH SGTCHS \$\$TCHS \$\$RAST 02 SGSVC \$\$RAST 03 SGDFCH \$\$RAST 01 SGTCHS \$\$ANERR6 \$\$RAST11 FOPT FOPT SGTCHS SEND \$\$ANERRJ SGTCHS SGUNCK \$\$RAST10 SGTCHS \$\$ANERRJ SGTCHS \$\$ANERRJ \$\$RAST10 \$\$ANERRJ \$\$RAST10 \$\$ANERRJ	SE FM CCCWFWDJHDNHHKEFECKGC QF		PAR45 PAT PCHDIB PCHKSW PCHKSW PCHKSW PCIL1 PCIL2 PCITRT PCURTN PDABEX PDAGN PDAID PDBOCK PDBUFL PDCCBPT PDCCBT PDCHAN PDCOMP PDCSWST PDCSWST PDCSWST PDDEQUE PDDEQUE2 PDDFLT PDEDLT PDERXT1	\$\$ANERRC SGTCHS FOPT SGSVC SGSVC SGDFCH SGDFCH SGSVC \$MICR S	M J A J K B B M F H F E F B B B E F E D F G G G F B E J D J J J J J J J J J F J

PDERXT2	SMICR	JF	PDHERE	SMICR	JC
PDERXT3	SMICR	JF	PDIAGN	SMICR	JВ
PDETIO	SMICR	JD	PDIAGN1	SMICR	JC
PDETIO	SMICR	JF	PDINTR	SMICR	JA
PDEXT1	SMICR	JH	PDKEY	SMICR	JН
PDFSTM	SMTCR	.TR			

PDMOV	SMICR	JE	PREPSBR	\$\$ANERSC	ŪQ
PDMPI	SMICR	JA	PROC	\$\$ANERRT	SA
PDMVCSW	SMICR	JE	PROTCHK	\$\$ANERRA	NL
			PROTECT	SGTCHS	CH
PDNF	SMICR	JB ·	PRTPRG	SGUNCK	DB
		JC			
PDNOB	SMICR		PRTPRG1	SGUNCK	DA
PDNONOP	SMICR	JB	PSTBUF	\$\$ANERRW	SG
PDNOPCK	FOPT	BA	PSTEOF	SGTCHS	CQ
PDNOPCK	SGSVC	FJ	PSTERR	\$\$ANERRT	SA
PDNOPCK	SGSVC	FK	PSTERR	\$\$ANERRW	sf
PDNOSS	SMICR	JВ	PTERP	\$\$ANERRA	NL
PDNOTSS	SMICR	JG	PTOSW	\$\$ANERRL	PG
PDNOTZR	SMICR	JC	PTRXCH	\$\$ANERRO	TF
PDPDEQ	SMICR	JЕ	PUBDEQ	SGSVC	FF
PDPRCAN	SMICR	JG	PUBSCAN	\$\$RAST00	VE
PDPROGCK		JG	PUBSCN3	• •	TD
	SMICR			\$\$ANERRZ	
PDREJDC	SMICR	JF	PURGE	SGTCHS	CM
PDREJT	SMICR	JC	PUTUTR	\$\$ANERRU	SC
PDSCAW	SMICR	JB			
PDSERR	SMICR	JD			
PDSERR1	SMICR	JD	QIDCK1	\$\$ANERRZ	\mathtt{TD}
PDSERR1	SMICR	JF	QISRT1	SGUNCK	DH
PDSERR2	SMICR	JD	QISRT2	SGUNCK	DH
PDSERR3	SMICR	JD	QISRT3	SGUNCK	DH
PDSIO	SMICR	JC	QUETEST	\$\$ANERRP	RE
PDSNO1	SMICR	JE	QUETEST	\$\$ANERRQ	RG
PDSNO2	SMICR	JD		SGTCHS	CC
			QUEUP OUIET145		
PDSPK	SMICR	JB	~	\$\$RAST03	WJ
PDSS	SMICR	JC	QUISIO	SGUNCK	DH
PDSUPEXT	SMICR	JH	Q 01	\$\$ANERRG	QC
PDSUPV	FOPT	BG	•		
PDSUPV	SGSVC	FL			
PDSVC28	SMICR	JC	RADLDS	SGTCHS	CA
PDSWBP	SMICR	JH	RASDEO	MCRAS	HG
PDSWZ	SMICR	ЈН	RASIO	\$\$RAST01	VН
PDTASK	SMICR	JH	RASIO	\$\$RAST10	ΧM
PDTERR1	SMICR	JE	RASIO	\$\$RAST11	XN
PDTERR1	SMICR	JF	RASIOE	MCRAS	HC
PDTERR2	SMICR	JE	RASMEXT	MCRAS	HB
PDTERR5	SMICR	JE	RASQOK	MCRAS	HC
PDTIMER	SMICR	JH	RAST02	\$\$RAST00	۷D
PDTIO	SMICR	JA	RBBY12	SEND	LA
PDTIOERR	SMICR	JE	RCHAN	\$\$ANERR6	UD
PDTIOERR	SMICR	JF	RCHAN	\$\$ANERAJ	IJ
PDTIOK	SMICR	JB	RCHS	\$\$ANERAJ	UJ
PDTKY	FOPT	BG	RCOMMONA	\$\$RAST05	XG
PDTKY	SGSVC	FL	RCOMMONB	\$\$RAST04	XD
PDUPDT	SMICR	JB	RCOMMONB	\$\$RAST05	XG
PDYES	SMICR	JE	RCVERR	SGUNCK	DC
PHASE	SGDFCH	EC	RDDIR2	SGDFCH	ED
PHASEH	\$\$ANERRG	QC	RDHA9	SGDSK	GA
	• •	-			
PHASEJ	\$\$ANERRG	QA	RDRCD	\$\$ANERRH	QD
PHASES	\$\$ANERRP	RF	RDTXT	SGDFCH	EE
PHASES	\$\$ANERRQ	RH	RDVER	\$\$ANERRK	QН
PHASES	\$\$ANERRR	RJ	RDYCANDP	SGTHAP	MK
PHASE1	\$\$ANERRG	QB	RDYCNL	SGTHAP	MM
PHASE2A	\$\$ANERAE	RC	RDYCN1	SGTHAP	MM
PHASR	\$\$ANERRQ	RH	RDYCN2	SGTHAP	MM
PICKDIR	SGDFCH	EC	RDYCN2A	SGTHAP	MM
POSCHK	\$\$ANERSC	ŪQ	RDYCN4	SGTHAP	MM
POSCHK3	\$\$ANERSC	ΩŎ	RDYCN4X	SGTHAP	MM
POSCHK4	\$\$ANERSC	UR	RDYCN4Z	SGTHAP	MM
POSTCAN	\$\$ANERRY	TB			
	• •		RDYDUMP	SGTHAP	MK
POSTCE	SGTCHS	CP	READUPDT	SGDFCH	EG
POSTPIB	\$\$RAST02	WB	RECAL	SGDSK	GA
PREFERED	SGDFCH	EC	RECFULL	\$\$RAST01	VF

RECSBLT	\$\$RAST01	٧J	R2501A	\$\$RAST04	XB
RECVERR		UF	R2501B	\$\$RAST04	XВ
	\$\$ANERR8		R2520		
REFAIL	\$\$ANERR8	UF		\$\$RAST05	XE
REGZ ERO	\$\$RAST11	XN	R2520B	\$\$RAST05	$\mathbf{x}\mathbf{E}$
RELOC	SSANERRP	RE	R2540	\$\$RAST04	XB
				• •	
RELOCATE	\$\$RAST10	XL			
REPERR	\$\$ANERRQ	RH			
REQUEST	\$\$RAST10	XM			
RERASIO	MCRAS	HC	SAVEIO	\$\$RAST00	VE
RESCHK	SGUNCK	DB	SCANTAB	\$\$RAST02	WC
RESERR	SGDSK	GA	SCHREC2	\$\$RAST02	WD
RESET	\$\$ANERAE	RC	SCIL1	SGDFCH	EB
RESPNS	SSANERRR	RJ	SCIL2	SGDFCH	EB
RESPTYP	\$\$RAST10	XL	SDM01	\$\$ANERAF	NG
RESTART	\$\$RAST00	۷C	SDRACC1	\$\$ANERAC	NE
RESTCQP	\$\$ANERSC	UR	SDRACC2	\$\$ANERAC	NE
RESTORE		WG			
	\$\$RAST03		SDRACC3	\$\$ANERAC	NE
RESTUSE	\$\$ANERSB	UP	SDRACC5	\$\$ANERAC	NE
RESVC	SGSVC	FC	SDRAREL	\$\$ANERAC	NE
RESVC1	SGSVC	FE	SDRAW1	\$\$ANERAC	NE
KEDVCI	babve	111			
			SDRAW2	\$\$ANERAC	NE
RETOFF	\$\$ANERR6	UD	SDRERAC	\$\$ANERAC	NE
RETOFF	SSANERR7	UE	SDREXIT	\$\$ANERAC	NF
RĚTRY	\$\$ANERRV	SE			
			SDRIO	\$\$ANERAF	NH
RETRY	\$\$ANERRX	SK	SDRIOE	\$\$ANERAC	NF
RETRY	\$\$ANERR9	UB	SDRIOX	\$\$ANERAF	NH
RETRY	\$\$ANERR6	UC	SDRIOX1	\$\$ANERAG	NJ
RETRY	\$\$ANERRR	RJ	SDRIO2		
	• •			\$\$ANERAC	NF
RETURN	\$\$RAST01	VН	SDRMM	SEND	LA
RETURN	\$\$RAST03	WH	SDRM00	\$\$ANERAG	NJ
RETXIT	\$\$ANERRX	SK	SDRM012	SSANERAF	NG
RINGBELL	\$\$RAST00	VA		• •	
			SDRM02	\$\$ANERAF	NG
RINGTIO	\$\$RAST00	ΑV	SDRM03	\$\$ANERAF	NG
RLOG	\$\$RAST04	XA	SDRNMCRR	SEND	LG
RMESSAGE	\$\$RAST00	VΑ	SDRNO	SEND	LB
RPRNTR	\$\$RAST04	XC			
	• •		SDRNOAD	\$\$ANERAC	NE
RSETWAIT	SGTCHS	CM	SDROBR	SEND	$_{ m LF}$
RSTCHPT	\$\$ANERRY	TA	SDROBRO	SEND	$_{ m LF}$
RSTCHO	\$\$ANERRY	TA	SDROBRW	SEND	\mathbf{LF}
RSTFLG	\$\$ANERRU	SC			
			SDRQUIS	SGUNCK	DH
RSTFLG	\$\$ANERRI	QE	SDRQUIS1	SGUNCK	DH
RSTFLG	\$\$ANERRJ	QG	SDRREL	\$\$ANERAC	NF
RSTFLG	SSANERRP	RF	SDRREL1	\$\$ANERAC	NF
RSTFLG	• •	RG		• •	LF
	\$\$ANERRQ		SDRSDR	SEND	
RSTPUB	SGDFCH	EH	SDRSDR1	SEND	\mathbf{LF}
RSTPUB1	SGDFCH	EH	SDRSDR2	SEND	LG
RSTQPT	\$\$ANERRU	SC	SDRSDR2X	SEND	LG
RSTOPT	\$\$ANERRH	QD			NG
			SDRSKIP	\$\$ANERAF	
RSTQPT	\$\$ANERRI	QE	SDRSVC3	SEND	LA
RSTQPT	\$\$ANERRJ	QG	SDRXIO	SEND	${f LB}$
RSTQPT	\$\$ANERRP	RF	SDRXIO1	SEND	LB
RSTOPT	SSANERRO	RG			
	• •		SDRXIO2	SEND	$\mathbf{L}\mathbf{B}$
RSTREG	SGUNCK	DE	SDRXIO3	SEND	$_{ m LB}$
RTARET	MCRAS	HB	SDRYES	SEND	LD
RTARET1	MCRAS	HB	SDR1	SEND	$_{ m LE}$
RTNTEST	\$\$RAST00	VA	SDR1A	SEND	LE
	• •				
RTY	\$\$ANERRV	SD	SDR1B	SEND	$_{ m LE}$
RTYCT	\$\$ANERRV	SE	SDR1B1	SEND	\mathbf{LE}
RTYONE	\$\$ANERRU	SC	SDR1B2	SEND	$_{ m LE}$
RTYRTN	\$\$ANERRP	RF	SDR1B3	SEND	LE
R01	\$\$ANERRG	QA	SDR1B4	SEND	LE
R01	\$\$ANERRI	QE	SDR1B5	SEND	$_{ m LE}$
R01	\$\$ANERRJ	QF	SDR1RES	SEND	$_{ m LE}$
R1442	\$\$RAST04	ХС	SDR1RESX	SGUNCK	DE
R1442A	\$\$RAST04	XC	SDR1RES1	SEND	LE
R1442B	\$\$RAST04	XC	SDR2A3	SEND	LC
R2501	\$\$RAST04	XВ	SDR2A4	SEND	LC

SDR2A5	SEND	LC	SUPEXT	FOPT	BD
SDR2QT	SEND	LB	SUPIB	SGTCHS	CR
SDR2QT1	SEND	LB	SVC 37	SGTHAP	MC
SDR2QT2	SEND	LB	SVCALL	\$\$ANERAE	RC
SDR23	SEND	LD	SVCA6	SGSVC	FR
			SVCRTN1	FOPT	BH
GEOTTON1	AANUTED DE	mo.			TA
SECTION1	\$\$ANERRZ	TC	SVCWAIT	\$\$ANERRY	
SECTION3	\$\$ANERRZ	TD	SVCWAIT	\$\$ANERRP	RF
SEEKTEST	SGTCHS	CH	SVCWAIT	\$\$ANERRQ	RG
SEKCH	\$\$ANERRA	NL	SVCWAIT1	\$\$ANERRO	TE
	, ,	GA	SVC00	SGTCHS	CA
SEKCHK	SGDSK				
SEKCHK1	SGDSK	GA	SVC00	SGTCHS	CB
SELBMX	SGTCHS	CN	SVC01A	SGSVC	FΑ
SELBMX	SGTCHS	CN	SVC02	SGSVC	FC
SELECT	SGTCHS	CN	SVC02A	SGSVC	FC
SELERR	\$\$ANERRV	SD	SVC02J	SGSVC	FC
SENSTSTS	\$\$ANERR9	AU	SVC03	SGSVC	$\mathbf{F}\mathbf{F}$
SETARON	\$\$ANERRY	TB	SVC03	SGSVC	$\mathbf{F}\mathbf{F}$
SETCNCL	\$\$ANERRO	TF	SVC04	SGSVC	$\mathbf{F}\mathbf{F}$
	• •				
SETCNCL	\$\$ANERRQ	RG	SVC05	SGSVC	$\mathbf{F}\mathbf{B}$
SETDIS	\$\$ANERRS	RL	SVC06	SGTHAP	MM
SETEBL	\$\$ANERR8	UF	SVC07	SGSVC	FE
SETFCPU	MCRAS	HA	SVC08	SGSVC	FG
SETFLE	\$\$ANERRX	SJ	SVC09	SGSVC	FG
SETKEY	\$\$RAST03	WH	SVC10	SGSVC	FG
SETLNK	\$\$ANERAA	NC	SVC10A	SGSVC	FG
SETLT1	SGSVC	FD	SVC11	SGSVC	FE
					FE
SETLT2	SGSVC	FD	SVC11A	SGSVC	
SETLT2A	SGSVC	FD	SVC11A	SGSVC	FE
SETOP1	SGSVC	FJ	SVC11B	SGSVC	FD
SETOP1	SGSVC	FN	SVC11C	SGSVC	FD
SETOP2	SGSVC	FJ	SVC12A	SGSVC	FA
SETOP2	SGSVC	FN	SVC13A	SGSVC	FA
SETPOSTL	\$\$ANERRZ	TD	SVC15	SGTCHS	CA
SETPSN	\$\$ANERR7	UE	SVC15	SGTCHS	CB
SETRD	\$\$ANERR8	UF	SVC18	SGSVC	FN
	• •				
SETRTRY	\$\$ANERRQ	RH	SVC19	SGSVC	FN
SETSK	SGDFCH	EC	SVC2BND	SGSVC	FC
SETSKAD	SGDFCH	EC	SVC22	SGSVC	FH
SETSVAR	SGDFCH	EF	SVC22A	SGSVC	FH
		VC	SVC23	SGSVC	FH
SETUP	\$\$RAST00				
SIO	SGTCHS	CFA	SVC24	SGSVC	FΗ
SKCHK	\$\$ANERRA	NL	SVC25	SGTCHS	CB
SKSLI	\$\$ANERRB	NN	SVC26	SGSVC	FB
SPFKREP	\$\$RAST03	WH	SVC27	SGTCHS	СВ
					FB
SSCOM	\$\$ANERRW	SG	SVC29	SGSVC	
STDEXT	SGUNCK	DC	SVC3	\$\$ANERRA	NL
STEPLOOP	\$\$ANERRZ	TD	SVC35	SGTHAP	MA
STGERR	\$\$RAST03	WG	SVC35A	SGTHAP	$\mathbf{A}\mathbf{M}$
STGEXIT	\$\$RAST03	WH	SVC36	SGTHAP	MB
	• •				
STMODE	SGTCHS	CG	SVC37A	SGTHAP	MC
STMODE1	SGTCHS	CG	SVC38	SGTHAP	MD
STMODE2	SGTCHS	CG	SVC38A	SGTHAP	MD
STORE	SGTCHS	CH	SVC38B	SGTHAP	MD
STORKE	\$\$ANERAE	RC	SVC38B	SGTHAP	MD
			SVC38C	SGTHAP	MD
STRTED	SGTCHS	CE	SVC38C	SGTHAP	MD
STRTED	SGTCHS	CFA	SVC38D	SGTHAP	MD
		CE	SVC38E	SGTHAP	MD
STRTIO	SGTCHS				
STRTIO	SGTCHS	CFA	SVC39	SGTHAP	ME
STRTIO1	SGTCHS	CE.	SVC39A	SGTHAP	ME
STRTIO1	SGTCHS	CFA	SVC39B	SGTHAP	ME
STRTI2	SGTCHS	CFA	SVC39C	SGTHAP	ME
SUPEXP	SGTCHS	CA	SVE39D	SGTHAP	ME
SUPEXP	SGTCHS	CB			

•					
SVC39E	SGTHAP	MF	TESTLTA	FOPT	\mathbf{BE}
SVC39E1	SGTHAP	MF	TESTSUB	\$\$ANERR1	TG
			and the second s		
SVC39F	SGTHAP	MF	TESTSVC	SGDFCH	EDA
SVC39G	SGTHAP	ME	THCHK	SGTHAP	MC
SVC39H	SGTHAP	MD	THDLT1	SGTHAP	MB
SVC39H	SGTHAP	ME	THDLT2	SGTHAP	MB
SVC39H1	SGTHAP	ME	THDLT2	SGTHAP	MB
SVC39J	SGTHAP	MF	THFREE	SGTHAP	MB
SVC39K	SGTHAP	MF	THFREE1	SGTHAP	MB
SVC39L	SGTHAP	MF	THRETRY	SGTHAP	MC
SVC39M	SGTHAP	ME	THSETUP	SGTHAP	MA
SVC39P	SGTHAP	ME	THWAIT1	SGTHAP	MA
SVC39P1	SGTHAP	ME	THWAIT2	SGTHAP	MA
SVC390	SGTHAP	MF	TKDLET	SGTHAP	MB
SVC40	SGTHAP	MG	TKHDADD	SGTHAP	MΑ
SVC40A	SGTHAP	MG	TKHDQUE	SGTHAP	MA
SVC40B	SGTHAP	MG	TKHDRTN	SGTHAP	MΑ
SVC40C	SGTHAP	MG	TKHD1	SGTHAP	MΑ
SVC40D	SGTHAP	MG	TKHELD	SGTHAP	MA
SVC40E	SGTHAP	MG	TKPRTY	SGTHAP	MJ
SVC41					
	SGTHAP	MH	TKPRT1	SGTHAP	MJ
SVC41A	SGTHAP	MH	TMEKEY	SGSVC	FG
SVC41A1	SGTHAP	MH	TMERT1	SGSVC	FL
SVC41A2	SGTHAP	MH	TMRBPS	SGSVC	FL
SVC41B	SGTHAP	MH	TMRSW	SGSVC	${ t FL}$
SVC41C	SGTHAP	MH	TPBUSY 0	SGTCHS	CD
SVC42	SGTHAP	MG	TPBUSY1	SGTCHS	CD
the state of the s					
SVC42A	SGTHAP	MG	TPBUSY2	SGTCHS	CD
SVC42B	SGTHAP	MG	TPBUSY3	SGTCHS	CD
SVC43	SGSVC	FR	TPBUSY4	SGTCHS	CD
SVC45	SGSVC	FR	TPIGNOR	\$\$ANERRC	NM
SVC46	SGSVC	FR	TPRETRN	SEND	LA
SVC51	SGSVC	FS	TPSDR1	SEND	LA
SVC52	SGSVC	FS	TRKCHK	SGDSK	$_{\mathtt{GB}}$
SVEREG	FOPT	BAA	TRKEOC	SGDSK	GB
SVEREG	SGTCON	GC	TRNOFF	SGTCHS	\mathtt{CL}
SVNWAD	SGTCHS	CCA	TRYNXT	SGTCHS	CH
SWITCH	\$\$ANERRO	RD	TSTATD	\$ \$ ANERRR	RJ
SXPC1	SGSVC	FN	TSTATTN	SGTCHS	\mathtt{CL}
SXPC2	SGSVC	FN	TSTBMX	SGTCHS	CQ
SXTRT1	SGSVC	FJ	TSTCAN	\$\$ANERRR	RJ
SXTRT1	SGSVC	FN	TSTCCB	\$\$ANERRN	RB
SYCLAS	\$\$ANERRO	RD .	TSTCCC	\$\$ANERRU	SB
SYSFILE	SGTCHS	CJ	TSTCDC	\$\$ANERRU	SB
SYSFILE1	SGTCHS	CJ	TSTDEV	SGTCHS	CCA
SYSFILE2	SGTCHS	CJ	TSTDEV1	SGTCHS	CCA
SYSFILE3	SGTCHS	CQ	TSTDEV2	SGTCHS	CD
SYSFILE4	SGTCHS	CJ	TSTEOJ	SGTCHS	CE
SYSFILE5	SGTCHS	CE	TSTEQCK	\$\$ANERR6	UC
			-		
SYSINOUT	SGTCHS	CE	TSTERF	SGTCHS	\mathtt{CL}
SYSSIN	SGTCHS	CJ	TSTNXT	SGTCHS	CJ
S01	\$\$ANERRJ	QF	TSTPSN	\$\$ANERR7	UE
201	JARRENNO	Δī		• •	
			TSTQEF	SGTCHS	CP
		1	TSTRESIO	SGTCHS	CN
TAPMODE2	\$\$ANERR9	UB	TSTRTY	\$\$ANERRN	RB
TCAN2	\$\$ANERRY	TB	TSTSNS	\$\$ANERAI	UG
TCAN2A	\$\$ANERRY	${f T}{f B}$	TSTSSL	\$\$ANERRB	NN
TEST	\$\$ANERRH	QD	TSTSVC	SGDFCH	EDA
TESTBUSY	\$\$ANERRP	RE	TSTTRG	\$\$ANERRS	RK
TESTDMC	\$\$RAST02	WA	TSTUCK	SGTCHS	CKA
TESTEOJ	SGTCHS	CF	TST03U	\$\$ANERRU	SB
			TST2311		
TESTER	\$\$ANERAD	NK		\$\$ANERAA	NC
TESTFE	\$\$RAST02	WD	T01	\$\$ANERRG	QΒ
TESTIGN	\$\$ANERRQ	RG	T03	\$\$ANERRH	QD
		•		•.•	-

\$\$ANERRH	QD	USRSEN	SGUNCK	DB
	WF	USRUCK	SGUNCK	DA
SSRAST03	WE			
• • • • • • • • • • • • • • • • • • • •				
		VERIF	\$\$ANERRB	NN
ŚŚANERRV	SD	VLDADR1	SGTCON	GC
	SE	VLDADR2	SGTCON	GC
\$\$RAST02	AW	VLDADR3	SGTCON	GC
SGTCHS	CE			
\$\$ANERAI	ŪG			
\$\$ANERR6	UC	WAIT	\$\$ANERRY	TA
\$\$ANERR7	UE	WAITLOOP	SGDFCH	EH
\$\$ANERRT	SA	WAITSVC	\$\$ANERRP	RF
\$\$ANERRW	SF	WRITEREC	\$\$RAST01	VH
\$\$ANERRB	NN		• •	
\$\$RAST11	XN			
\$\$ANERRO	RD	XEXIT	\$\$RAST04	XΑ
\$\$ANERRO	RD	XEXIT	\$\$RAST05	XE
\$\$ANERRA	NL	XFETCH	\$\$RAST04	XA
\$\$ANERR9	UB	XFETCH	\$\$RAST05	XE
SGUNCK	DA	XIOERR	\$\$ANERSB	UΡ
SGUNCK	DA	XLDMOD	\$\$RAST05	XE
\$\$ANERRU	SC	XLDTST	\$\$RAST04	XΑ
SGTHAP	MJ	XLDTST	\$\$RAST05	XE
SGTHAP	MJ	XMSG	\$\$RAST04	XΑ
SGTHAP	MJ	XMSG	\$\$RAST05	XE
SGTHAP	MJ	XNOMSG	\$\$RAST04	XΑ
SGTHAP	MJ	XNOMSG	\$\$RAST05	XΕ
SGTHAP	MJ	XNORMAL	\$\$ANERSC	UR
\$\$ANERAI	UG	XQFULL	\$\$ANERSB	UP
\$\$RAST 03	WF	XTOERR	\$\$ANERSC	UR
\$\$RAST11	XN			
\$\$RAST00	٧E			
\$\$RAST02	WA	ZEROCT	\$\$ANERR6	UD
\$\$RAST02	WC	ZERTEB	\$\$ANERRS	RK
SGTCHS	CKA	ZERTEBV	\$\$ANERRS	RK
SGUNCK	DA	ZROREG	SGTCHS	CR
	SGTCHS \$\$ANERAI \$\$\$ANERR6 \$\$ANERR7 \$\$\$ANERRT \$\$\$ANERRW \$\$\$ANERRB \$\$\$ANERRO \$\$\$THAP \$\$THAP \$\$\$THAP \$\$\$T	\$\$RAST03 WE \$\$RAST03 WE \$\$RAST03 WE \$\$RAST03 WE \$\$RAST03 WE \$\$ANERRV SE \$\$ANERRV SE \$\$ANERRV SE \$\$ANERAI UG \$\$ANERAI UG \$\$ANERR6 UC \$\$ANERR7 UE \$\$ANERRT SA \$\$ANERRW SF \$\$ANERRW SF \$\$ANERRB NN \$\$RAST11 XN \$\$ANERRO RD \$	\$\$RAST03 WF \$\$RAST03 WE VERIF \$\$ANERRV SD VLDADR1 \$\$ANERRV SE VLDADR2 \$\$ANERRV SE VLDADR3 SGTCHS CE \$\$ANERAI UG \$\$ANERAI UG \$\$ANERR6 UC WAIT \$\$ANERR7 UE WAITLOOP \$\$ANERRW SF WRITEREC \$\$ANERRW SF WRITEREC \$\$ANERRW SF WRITEREC \$\$ANERRW SF WRITEREC \$\$ANERRO RD XEXIT \$\$ANERRO RD XEXIT \$\$ANERRO RD XEXIT \$\$ANERRO RD XEXIT \$\$ANERRA NL XFETCH \$\$ANERRA NL XFETCH \$\$ANERRA NL XFETCH \$\$ANERRP UB XFETCH \$\$ANERRP UB XFETCH \$\$ANERRP UB XFETCH \$\$ANERRP UB XFETCH \$\$GUNCK DA XIOERR SGUNCK DA XIDERR SGUNCK DA XIDERR SGUNCK DA XIDTST SGTHAP MJ XMSG SGTHAP MJ XMSG SGTHAP MJ XMSG SGTHAP MJ XMSG SGTHAP MJ XNOMSG SG	S\$RAST03 WF

APPENDIX B: ERROR MESSAGE CROSS REFERENCE

Messag	<u>e</u> <u>Phase</u>	2	<u>Chart</u>		\$\$ANERRD	(Tape) (Data Cell)	PA QH
0P08	\$\$ANERRA \$\$ANERRF	(Paper Tape) (Disk) (Tape)	GA UG NM PF		\$\$ANERRV \$\$ANERRX	(Unit Record) (Paper Tape) (Tape Cartridge Reader)	SE SJ UE
	\$\$ANERRT \$\$ANERRU	(Data Cell) (MICR Type) (Unit Record) (Unit Record)	QB SA SC SD			(3211 Printer)	ÜK
	\$\$ANERRX \$\$ANERR7	(MICR Type) (Paper Tape) (Tape Cartridge Reader)	SF,SG SJ UE	0P12	\$\$ANERRB \$\$ANERRK	(Disk) (Data Cell)	ОН Ии
		(Optical Reader) (3211 Printer)	UA UK	0P13	\$\$ANERRB \$\$ANERRK \$\$RAST10	(Disk) (Data Cell)	NN QH XL
0P09	\$\$A\$SUP1	(Disk) (Paper Tape)	GA UG				
	\$\$ANERAM \$\$ANERRA \$\$ANERRA	(Tape) (Disk)	PJ NM PF	0P14	\$\$A\$SUP1 \$\$ANERRB \$\$ANERRF	(Disk) (Tape)	GA NN PE,PF
		(Data Cell) (MICR Type)	QB SA			(Data Cell) (Unit Record)	QB SE
	\$\$ANERRU \$\$ANERRV \$\$ANERRW	(Unit Record) (Unit Record) (MICR Type)	SC SE SF,SG			(Optical Reader)	ÜB
		(Paper Tape) (Tape Cartridge	sj UC,UD	0P15	\$\$A\$SUP1		GA
	\$\$ANERR7	Reader) (Tape Cartridge Reader)	UE		\$\$ANERRA \$\$ANERRJ	(Disk) (Data Cell)	NL QF
		(Optical Reader) (3211 Printer)	UA UK				
	••			0P16	\$\$ANERRB \$\$ANERRK	(Disk) (Data Cell)	NN QH
0P10	\$\$A\$SUP1	(Disk) (Paper Tape)	GA				
	\$\$ANERAM	(Tape)	UG PJ	0P17	\$\$ANERAM	•	PK
	\$\$ANERRA \$\$ANERRF		NL PE		\$\$ANERRB \$\$ANERRG	(Disk) (Data Cell)	nn QC
	\$\$ANERRG	(Data Cell)	QA .		• • • • • • • • • • • • • • • • • • • •		~
		(Unit Record) (Unit Record)	SC SD				
	\$\$ANERRX	(Paper Tape)	SJ	0P18	\$\$A\$SUP1		GA
	\$\$ANERR6	(Tape Cartridge Reader)	UC		\$\$ANERAI \$\$ANERAM	(Paper Tape)	UG PK
	\$\$ANERR7	(Tape Cartridge Reader)	UE		\$\$ANERRB		NN
	\$\$ANERSA	(3211 Printer)	UK		\$\$ANERRT \$\$ANERRU \$\$ANERRV	(MICR Type) (Unit Record) (Unit Record) (MICR Type)	QC SA SC SE SF,SH
0P11	\$\$A\$SUP1		GA		\$\$ANERRX	(Paper Tape)	SJ
	\$\$ANERAJ \$\$ANERAP	(Paper Tape)	UH PN		\$\$ANERR7	(Tape Cartridge Reader)	UE
	\$\$ANERAS		PX			(Optical Reader)	UB
	\$\$ANERRB		NN		\$\$ANERSA	(3211 Printer)	UK

RIK (Requestor I/O Key)

When a supervisor routine (fetch or physical transient) issues an SVC 0 or SVC 15, the routine puts the value to be used in the CAW storage protect key into the high-order digit of the second byte of the RIK halfword. When this value is zero, the low order digit has these special meanings:

Physical transients put a X'01' into the RIK when they are doing a SYSLOG I/O. The PIK for physical transients has a value of X'60', therefore the channel scheduler would type "SP" (supervisor ID) as the SYSLOG ID. The physical transients put the ID of the program referred to by the message into the message.

RIK	<u>Meaning</u>						
X'01'	This is a SYSLOG I/O request.						
	The channel scheduler is not to						
	type a SYSLOG ID prefix.						

X'02' This has been a fetch I/O request. This special code is required by ERP to recognize fetch requests.

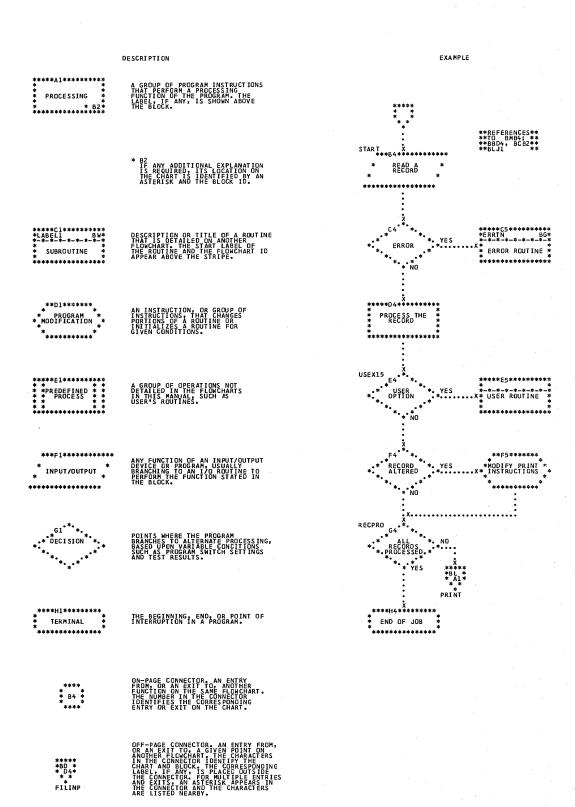
Fetch always sets a X'02' in the RIK. ERP transients put the key of the program requiring ERP into the RIK, when the ERP is a retry of a user EXCP and the ERP transient requires control to return to itself.

FIK (Fetch I/O Key)

Used by the fetch to validate the phase name address and load address. FIK has the following values:

- 1 Key of the problem program requestor.
- 2 0 0
- 4 0 if the transient issued the SVC 4. Key of the problem program if not a transient.

APPENDIX F: EXPLANATION OF FLOWCHART SYMBOLS



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