IBM Field Engineering

Maintenance Diagrams

2020 Processing Unit

System/360 Model 20

(Machines with serial no. 50,000 and above)

Volume 1

SY33-1024-0

Preface

This publication (Volume 1) and its companion publication (Volume 2, Order No. SY33-1042) constitute the Field Engineering Maintenance Diagrams manual for the IBM 2020 Processing Unit (machines with serial number 50,000 and above) in the IBM System/360 Model 20. Volume 1 contains information on the following:

Diagnostic techniques (Section 1)
Error conditions (Section 2)
Data flow (Section 3)
Functional units (Section 4)
Power (Section 6)
Microprograms (Appendix B)

Volume 2 contains operations information (Section 5), including microinstruction charts, MANOP charts, and cycle-stealing charts.

Both volumes are used for maintenance, instruction, and recall.

The material in these volumes supplements the information contained in the following manuals:

1. Field Engineering Theory of Operation, *2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1021.
2. Field Engineering Maintenance Manual, *2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1035.

Associated Publications

The following Field Engineering Maintenance Diagrams manuals contain information on the features which may be installed on the 2020 Processing Unit:

1. *1403 Printer Models 2, 7, N1 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1018.
2. *2152 Printer-Keyboard Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1026.
3. *2203 Printer Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1022.
4. *2520 Card Read Punch Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1028.
5. *2560 Multi-Function Card Machine Attachment Feature, 2501 Card Reader Attachment Feature, 1442 Card Punch Model 5 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1033.
6. *Binary Synchronous Communications Adapter, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1039.
7. *Input/Output Channel Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1017.
8. *Storage Control Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1037.

Information on the serial I/O channel feature is contained in Field Engineering Theory of Operation, Maintenance Diagrams, *Serial I/O Channel Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1040.

The associated Field Engineering Theory of Operations manuals for the features are:

1. *1403 Printer Models 2, 7, N1 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1020.
2. *2152 Printer-Keyboard Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1025.
3. *2203 Printer Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1027.
4. *2520 Card Read Punch Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1029.
5. *2560 Multi-Function Card Machine Attachment Feature, 2501 Card Reader Attachment Feature, 1442 Card Punch Model 5 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1034.
6. *Binary Synchronous Communications Adapter, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1038.
7. *Input/Output Channel Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1019.
8. *Storage Control Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Order No. SY33-1036.

Second Edition (April 1969)

This volume is a major revision of, and obsoletes, all information (except Section 5) in ZZ33-1024-0 and FE Supplement ZZ33-1041; the companion publication, Volume 2, obsoletes Section 5.

Changes are continually made to the specifications herein; any such changes will be reported in subsequent revisions or FE Supplements.

A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Laboratories, Product Publications, Dept 3179, 703 Boeblingen/Wuertt, P.O. Box 210, Germany.

Form Y33-1024-0
FES Y33-1049

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Note: The diagrams in this manual have a code number to the right of the caption. This is a publishing control number and is unrelated to the subject matter.

Legends

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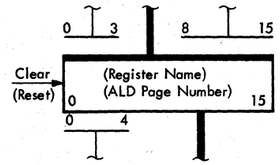
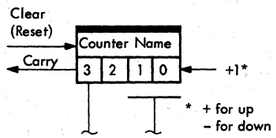
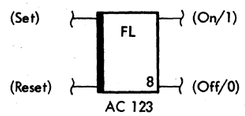


Register, Counter

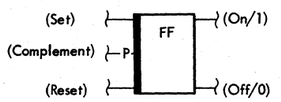
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.





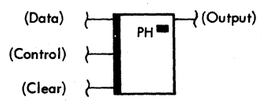
Flip Latch

Input side is denoted by thick line. Circuit multiples shown by numeral in lower right corner. ALD reference page may be shown beneath.



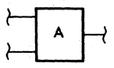
Flip-Flop

Input side is denoted by thick line. Shift signal is shown by a P or N.

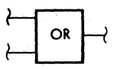


Polarity Hold

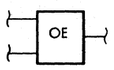
Input side is denoted by thick line.



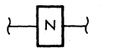
AND



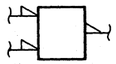
OR



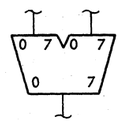
Exclusive OR



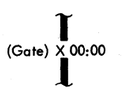
Negator (Inverter)



Negative Polarity wedge

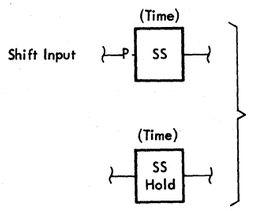


Adder

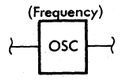


Gate

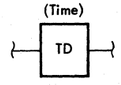
Numerals against gate symbol give page or diagram number of gating circuit.



Singleshot

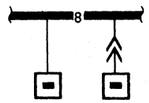


Oscillator



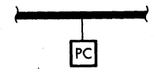
Time Delay

Indicator lamp

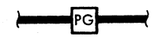


Identifies indicatable bus, register, latch, ect. such as: Indicatable bus with number of bus lines indicated

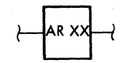
Indicatable flip latch



Parity Check data bus

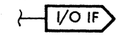


Parity Generate data bus



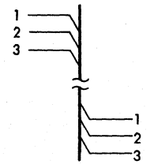
Amplifier

XX Abbreviations:
CD = Core Driver
CR = Current
DF = Differential
HD = Head Driver
ID = Indicator Driver
LD = Line Driver
LS = Line Sense
LT = Line Terminator
MD = Magnet Driver
V = Voltage Amplifier



Interface

Denotes interface between two units.



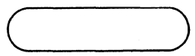
Multiple Line Transfer

2. Timing Charts

Active State

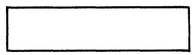
Numerals at beginning and end of the bar identify the signal(s)(also on the same chart) that activate and deactivate this line "Not" with the number indicates that lack of the signal conditions the line.

3. Flowcharts



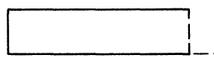
Terminal

Indicates beginning or end of event



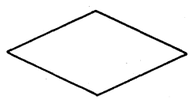
Process

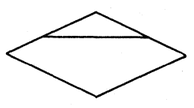
Indicates a major function or event. The upper portion of a divided block specifies where a detailed flowchart of the process is located.



Annotation

Gives descriptive comment or explanatory note.





Decision

Indicates a point in a flowchart where a branch to alternate paths is possible. The upper portion of a divided block specifies where a detailed flowchart is located.

4. General

On-Page Connector

Indicates connection between two parts of the same diagram. Arrow leaving symbol points (line-of-sight) to correspondingly-numbered symbol.

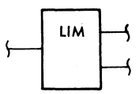
On-Page Connector

Indicates connection between two parts of the same diagram. Alphameric grid coordinate of complementary connector shown beneath.

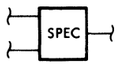
Off-Page Connector

Indicates connection between diagrams located on separate pages. Location of correspondingly-lettered symbol shown adjacent.

5. Additional Symbols

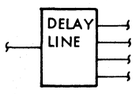


Limiter

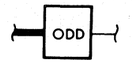


SPECIAL. Function of block described by appended name

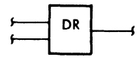
Test Point. Refer to ALD page CE101 or CE102 for appropriate signals



Delay Line. Provides outputs of differing delays



ODD. Output is active only when an odd number of inputs is active



Current Driver

Functional Logic Blocks

A functional logic block (FLB), which is a comprehensive representation of a number of AND and/or OR logic blocks, consists of two sections separated by a neck; the upper section is defined as *control* and collects signals common to all or some logic combinations contained in the FLB, while the lower section is defined as *data*. Input lines to the data section activate output lines under control (gating) of the control section.

The required input levels or the provided output levels of the FLB signals are identified by a wedge if negative; if no wedge is present, the level is positive.

Where input signals to the FLB are generated by a single AND or OR switch, the switch blocks are directly attached to the FLB input (control or data).

The basic function performed by an FLB is stated at the top of the control section.

In the 2020 CPU FEMDM, the following FLB types are used:

1. Selector (Example 1).
2. Decode (Example 2).
3. ALU (special) (Example 3).

A decode FLB consists of the data section only.

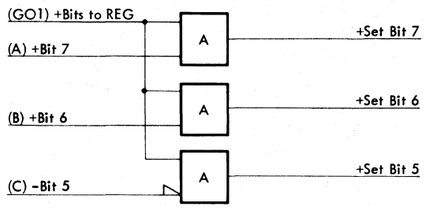
FLB input lines are specified by alphabetic or numeric characters. However, within one FLB, control and data inputs are specified differently; that is, if control inputs are specified numerically, the data inputs are specified alphabetically and vice versa.

The control inputs are additionally marked "GO" to indicate an output gate or "G" to indicate an input gate.

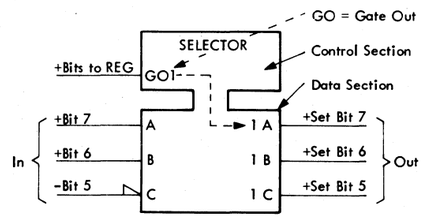
The size of an FLB depends upon the number of input or output signals and the function performed.

Example 1: SELECTOR

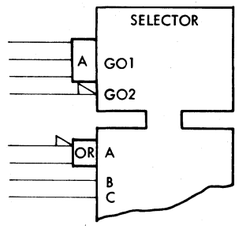
Normal Logic Representation

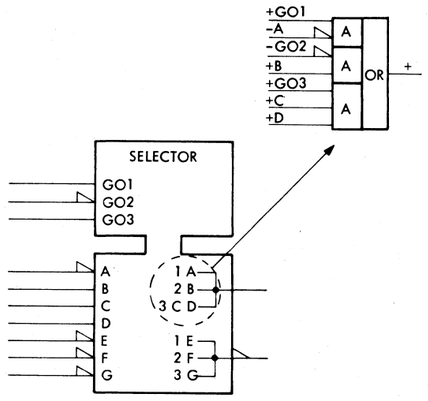


Equivalent FLB



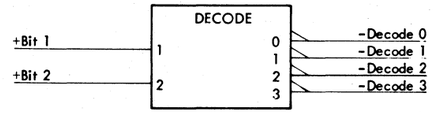
Variations

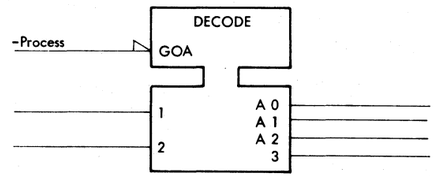




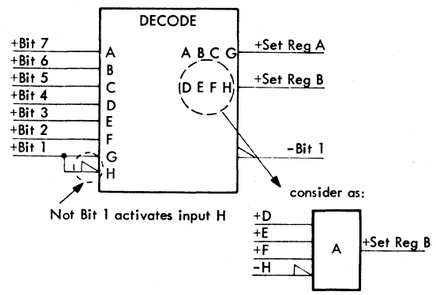
Example 2: DECODE

Decoding is performed in binary mode. The inputs are specified by their binary value. Other decodes (instead of binary) are possible



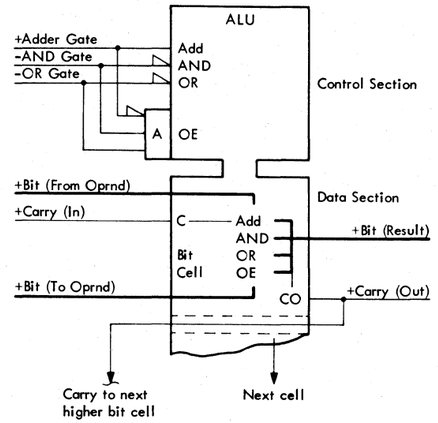


Note: Decode output 3 is independent of output gate GOA



Example 3: ALU

The data section is divided into bit cells. Every bit cell performs the arithmetic or logical function for one bit position. The function to be performed is specified in the control section. The carry input (C) is used for add only. The carry output (CO) can be activated during every ALU function (for parity correction)



Abbreviations

ac	Alternating Current
Addr	Address
ALD	Automated Logic Diagram
Alt	Alter
ALU	Arithmetic and Logical Unit
Amp*, Amplf*	Amplifier
ASCII	The American National Standard Code for Information Interchange
Att*	Attention
Auto	Automatic
Aux	Auxiliary
Bin	Binary
BOM	Basic Operating Module
BSCA	Binary Synchronous Communications Adapter
CC	Condition Code
Chk	Check
Comp	Compare
Cond*	Condition
Conn	Connection
Cont*	Continuously
Corr*	Correction
CPL	Control Program Load
CPU	Central Processing Unit
CS	Cycle Steal
CSR	Cycle Steal Request
CTRL	Control (microinstruction)
Ctrl	Control
CY	Delta Cycle
Cy	Cycle
DA	Device Address
DASF	Display, Alter, Scan, or Fill (signal)
Dec*	Decode
Decr	Decrement
Del*	Delayed
Det*	Detailed
Dev	Device
Disalt	Display or Alter (signal)
Disp, Displ	Display
DL	Detailed Log
Dr*, Driv*	Driver
EBCDIC	Extended Binary-Coded-Decimal Interchange Code
E-Phase	Execution Phase
Ext*	Extension
Fd	Feed
FDR	From-Data Register
FS	Function Specification
Gnd	Ground
GPR	General Purpose Register
Hw	Halfword
Hz	Hertz
I-Addr	Instruction Address
IAR	Instruction Address Register
ICPL	Initial Control Program Load
Imm	Immediate
Incr	Increment
Ind*	Indicator
Indir	Indirect
Inh	Inhibit (signal)
Inlk	Interlock
Insn, Instr*	Instruction
Int	Integrator (signal)
Intern*	Internal
Interr*, Intr	Interrupt
Inv	Invert
I/O	Input/Output
IOC	Input/Output Channel
I-Phase	Instruction Phase
IPT	Interrupt Priority Table
LC	Length Count
Lft*	Left
LS	Local Store
LSA	Local Store Addressing (check)
Lw*	Lower
MAR	Modify Address Register
Mem	Memory
MFCM	Multi-Function Card Machine (2560)
MHz	Megahertz
Microinstr, M-Instr	Microinstruction
Mod	Modify
Mom	Momentary (switch)
N/C	Normally Closed
N/O	Normally Open
Norm	Normal
ns	Nanosecond
NSI	Next Sequential Instruction
Op	Operation
OPR	Op Register (signal)
Oprd	Operand
Overr*	Overrun
Par*	Parity
Pb	Pushbutton
PL	Program Load
Pos	Position
Proc	Process
Prog*	Program
PS	Power Supply
PSW	Program Status Word
Rd	Read
Reg	Register
Regen	Regenerate
Rem	Remote
Req	Request
Res	Reset
Rht	Right
Rot	Rotary (switch)
RY	Relay (signal)
SA	Sense Amplifier
SAR	Storage Address Register
SCR	Silicon Controlled Rectifier
SCRID	Silicon Controlled Rectifier Indicator Driver
SDR	Storage Data Register
SENS	Sense (Microinstruction)
SIOC	Serial I/O Channel
SLD	Solid Logic Design
SNG	Single
ST*	Storage
St	Start
ST DASF	Storage Display, Alter, Scan, or Fill
Stor	Storage
Strb	Strobe
SU	Shift Unit
Suppr*	Suppress
Sw	Switch
Sync	Synchronization
TDR	To-Data Register
Tog	Toggle (switch)
Tw	Typewriter
TXT	Text
Uncond	Unconditional
Up	Upper
us	Microsecond
USASCII	*See* ASCII
V	Volts
V_{REF}	Voltage Reference
w-o	Without
Wr	Write

Note: References CC101, PA211, etc in this manual are ALD page numbers.

* Nonstandard, ALD abbreviation

2 3 4 5 6 7 8

A

2-4C9 +Inhibit Check FL
2-4D9 +SAR Check FL
2-4E9 +Modifier Check FL
2-6C9 +ALU Zero Test FL
2-6C9 +Bus Check FL
2-6D9 +Shift Unit Check FL
A
-All Checks
CC101

4-10E5 +Storage Use
+T1
4-4A9 +Delta Process not CS Reg
4-4B4 -Reset Pulse
A
A
OR
Stor Use Del
FL
+ Stor Use Delayed FL
- Stor Use Delayed FL
CC122

-All Checks
4-24C9 +Invert Parity FL
A
CC121

4-48B9 +ALU Zero
4-20B8 +ST DASF
4-20C8 +ST Test
A
A
A
OR
CC121

ALU Test
FL
+ALU Test FL
CC121

LS Write Control for TMS/TMSZ 4-36B5

4-18C3 +Set OPR Gate
+T3
4-54A3 +CLC
A
CC121

+CY0 or CY1
A
+T8
4-4A9 +Process
A
CC121

Fossils, subject to deletion

B

4-20D8 + MANOP Set ALU Zero
+CY3
4-4A9 +Delta Process
+CY1
4-20B8 +ST DASF
A
A
OR
CC122

-ALU Test FL
+T3
A
CC122

A
+T3
+T1
A
A
OR
CC122

4-62D5 -SENS 11
+T8
4-4A9 +Process not Cycle Steal
4-4D4 -Power On FL active
A
OR

The Missing Phase Detection feature is installed in 50 Hz power supplies only

(from PS, WC221) +3V Missing Phase
+ Process Check
Missing Phase
A
FL
-Missing Phase FL
I/O Common Bus In (CPU SENS) 4-62C4
CC122

CE Console
4-57A2

MANOP ALU not Zero
FL
+MANOP ALU not Zero
4-57E8 -Proc Check Overr Sw INT
OR
CC122

4-24D9 -STOR Test Load

Attention Indicator Customer Console 4-1A6

Process Check
FL
DOT
+Process Check FL
Run Control 4-4A5
-Process Check FL
LSA Check 2-2C7
4-4B4 -Reset Pulse
2-2D9
-System or Check Reset
OR
CC122

C

2-2C9 -LSA Check FL
2-4E9 -Modifier Check FL
2-4D9 -SAR Check FL
2-4C9 -Inhibit Check FL
2-6C9 -Bus Check FL
2-6C9 -ALU Zero Test FL
2-6D9 -Shift Unit Check FL
OR
Freeze Reg 4-59E2
Reset/Set Current PL 4-32D4
-Any Check
+Any Check
+LSA or MOD Check
OR
+LSA or MOD Check
LOG Control 4-22B5

4-4A9 +Delta Process
4-22A6 -LOG
A
4-24C9 +Invert Parity FL
CC122

AR CR
+Invert Parity
Change Parity Sum Bit 15 and 7 4-48E4,E6
Run Control 4-4C8
Invert Switch Parity 4-46E6
CC122

N
-Invert Parity
SU Parity Correction 4-52A3, C3, C7, E7
SDR Set 4-16B3
Terminate ST Test 4-4B6
Inhibit Check 2-4C7
Bus Check 2-6C8
Modifier Check 2-4D6
Eight Shift Parity 4-40E6
Prevent Cycle Advance 4-24E5

D

OR
+ALU or Bus or SU Check
Inhibit Check 2-4C7
Reset/Set OCU1 Monitoring Reg 4-22E2
Prevent Cycle Advance 4-24E5
CC101

System or Check Reset:

1. CE CPU Check Reset Sw
2. CE CPU Reset Sw
3. Power On
4. System Reset
5. Load Key operated for: ICPL, CPL, Cust Prgm Load

} LOG Reset CY3, T6

Reset Pulse:

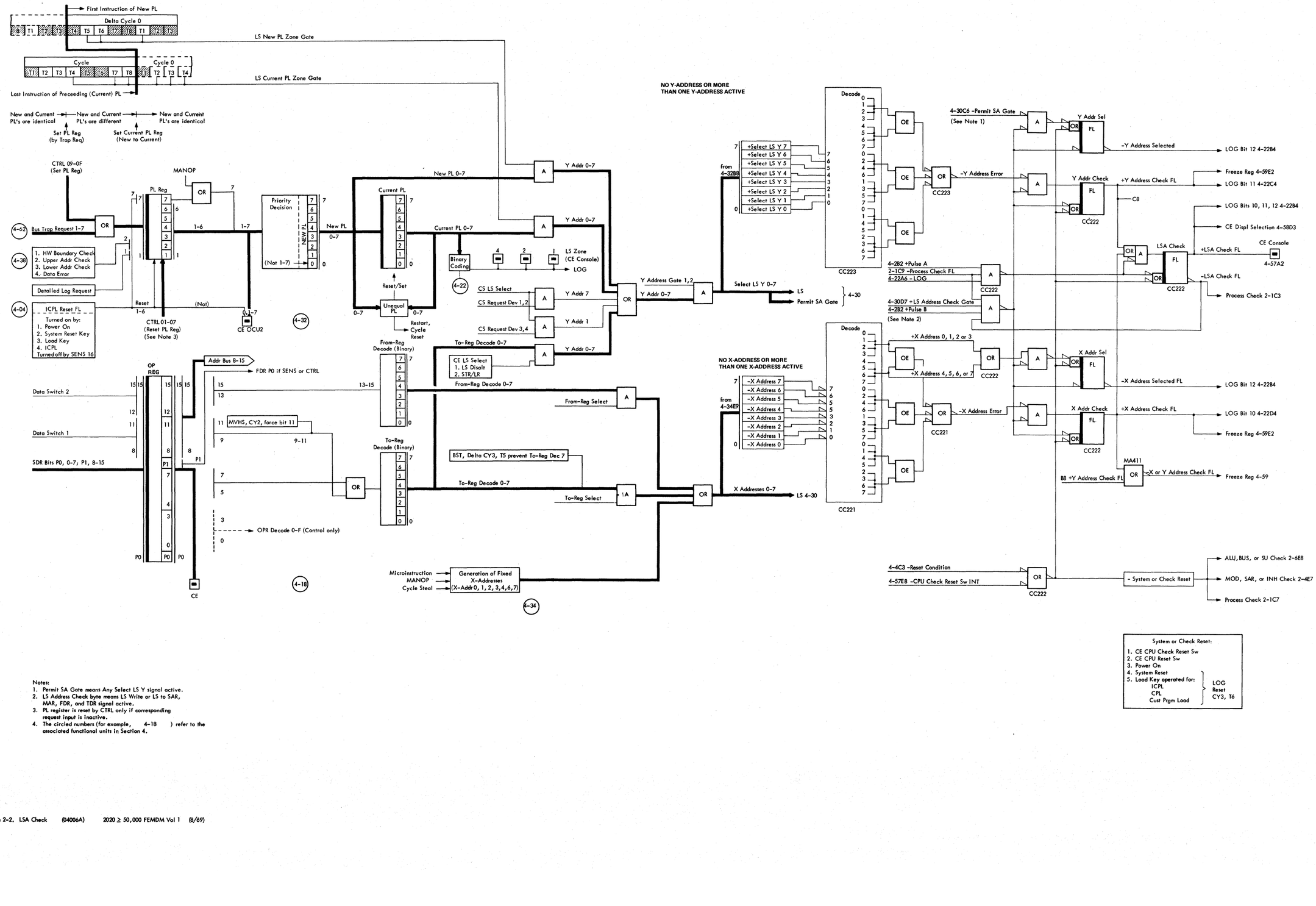
1. Power On
2. System Reset key or,
3. Load Key operated.

Origin of Frequently Occurring Signals

Signal	Origin
CYO, 1, 2, and 3	4-24E9
T1, 2, 3, 4, 5, 6, 7, and 8	4-2B9

E

● Diagram 2-1. Process Check, ALU Test/MANOP ALU not Zero, and Missing Phase (04005A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)

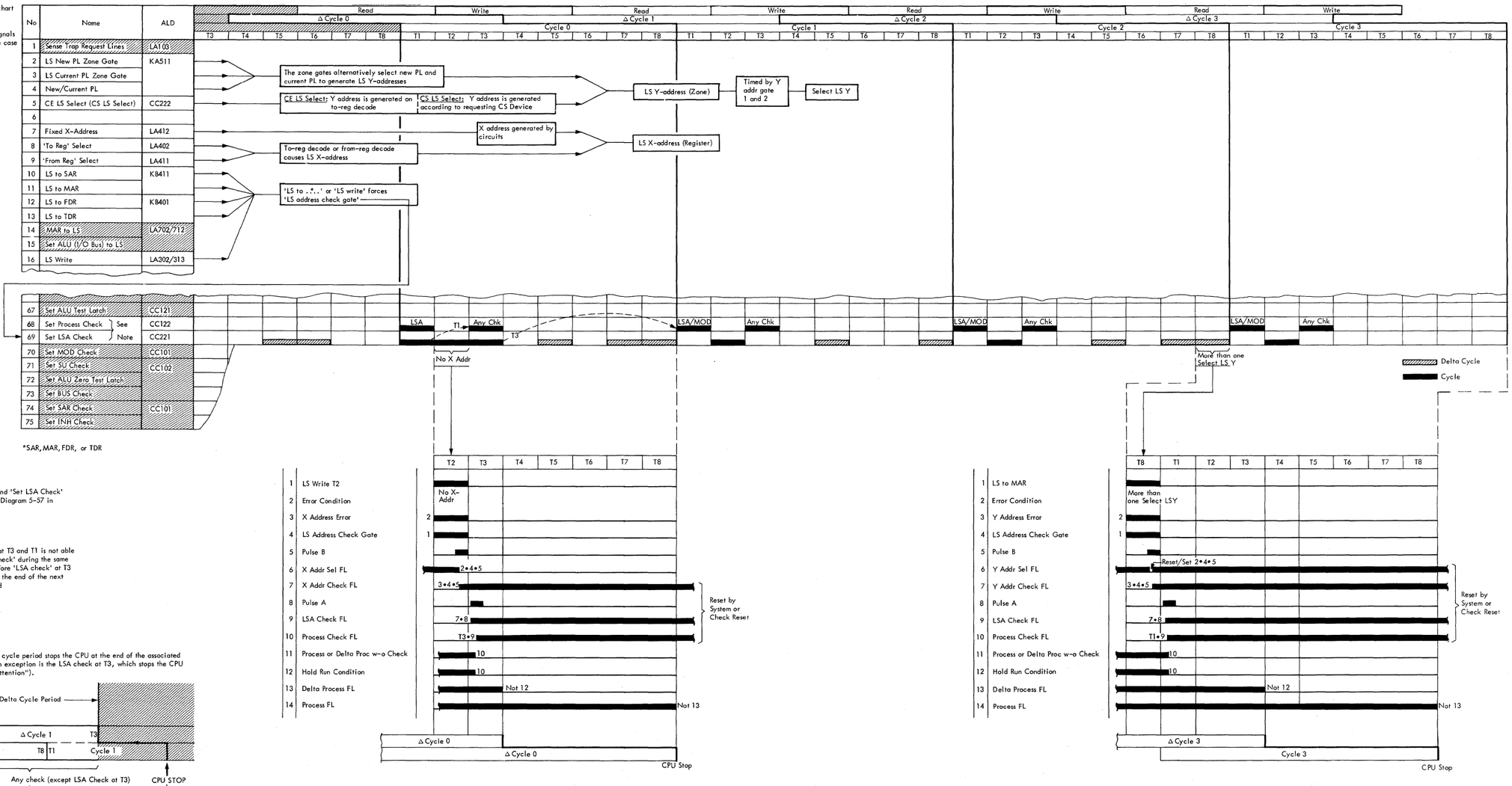


Notes:
1. Permit SA Gate means Any Select LS Y signal active.
2. LS Address Check byte means LS Write or LS to SAR, MAR, FDR, and TDR signal active.
3. PL register is reset by CTRL only if corresponding request input is inactive.
4. The circled numbers (for example, 4-18) refer to the associated functional units in Section 4.

Part of the standard timing chart used to represent CPU basic operations (see Section 5 in Volume 2). The unshaded signals have to be considered in the case of an LSA check.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select (CS LS Select)	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702/712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
67	Set ALU Test Latch	CC121
68	Set Process Check (See Note)	CC122
69	Set LSA Check (See Note)	CC221
70	Set MOD Check	CC101
71	Set SU Check	CC102
72	Set ALU Zero Test Latch	
73	Set BUS Check	
74	Set SAR Check	CC101
75	Set INH Check	

*SAR, MAR, FDR, or TDR

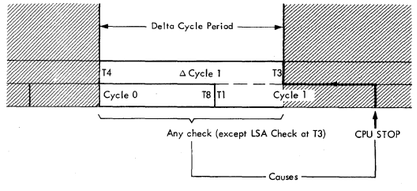


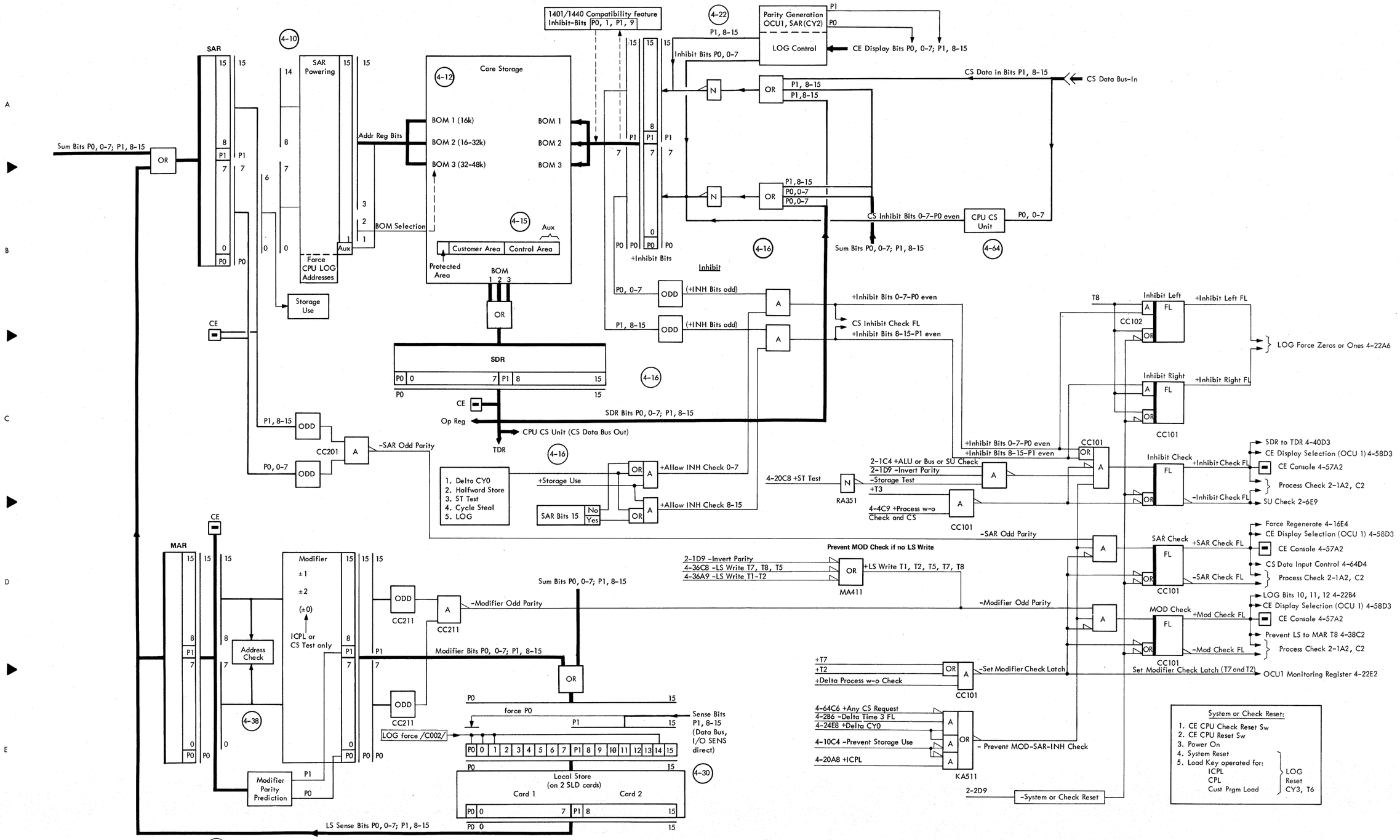
NOTE: 'Set Process Check' and 'Set LSA Check' timing is taken from Diagram 5-57 in Volume 2

Attention: 'Set LSA check' at T3 and T1 is not able to set 'process check' during the same T-period. Therefore 'LSA check' at T3 stops the CPU at the end of the next processing period

CPU Check Stop Timing

A CPU check during a delta cycle period stops the CPU at the end of the associated cycle (processing period); an exception is the LSA check at T3, which stops the CPU after the next cycle (see "Attention").

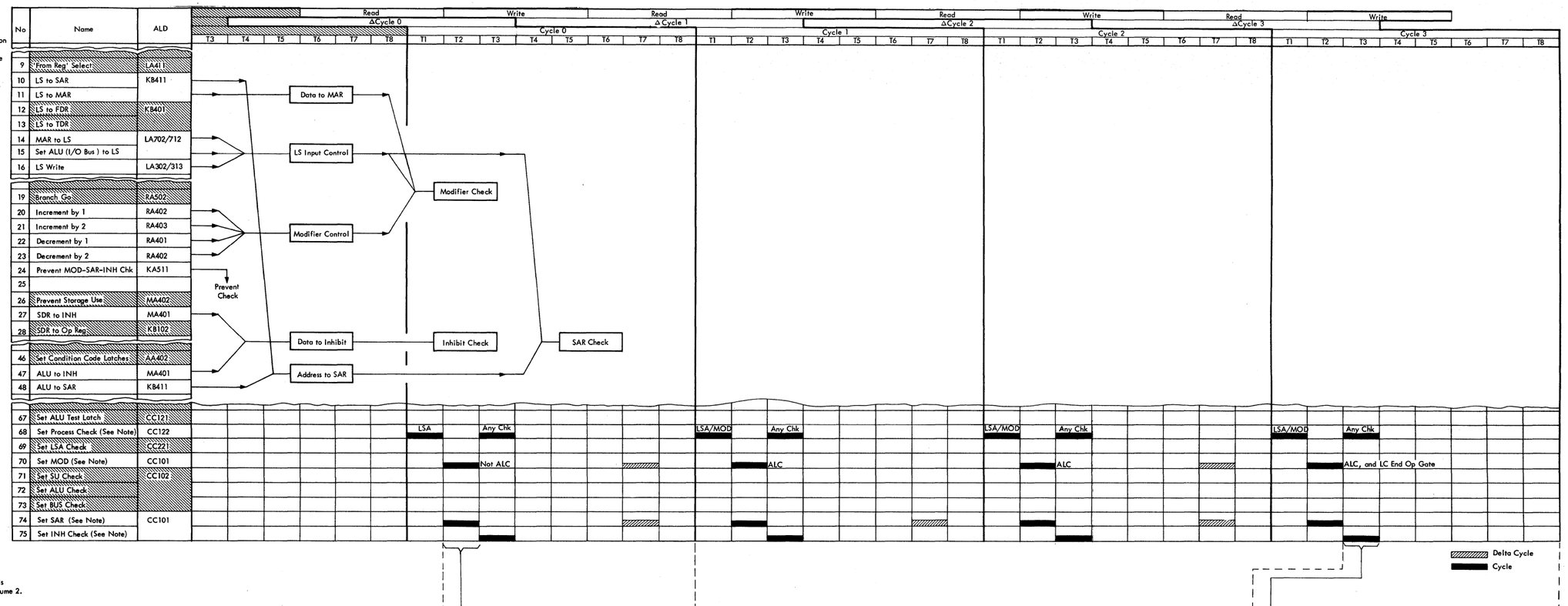




Note: The circled numbers (for example, (4-30)) refer to the associated functional units in Section 4

Part of standard timing chart used to represent CPU basic operations (see Section 5 in Volume 2). The unshaded signals have to be considered in the case of:
Modifier Check.
SAR Check
Inhibit Check.

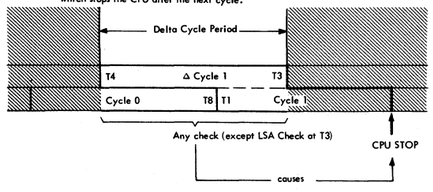
No	Name	ALD
9	From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702/712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent MOD-SAR-INH Chk	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to INH	MA401
28	SDR to Op Reg	KB102
46	Set Condition Code Latches	AA402
47	ALU to INH	MA401
48	ALU to SAR	KB411
67	Set ALU Test Latch	CC121
68	Set Process Check (See Note)	CC122
69	Set LSA Check	CC221
70	Set MOD (See Note)	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set BUS Check	
74	Set SAR (See Note)	CC101
75	Set INH Check (See Note)	

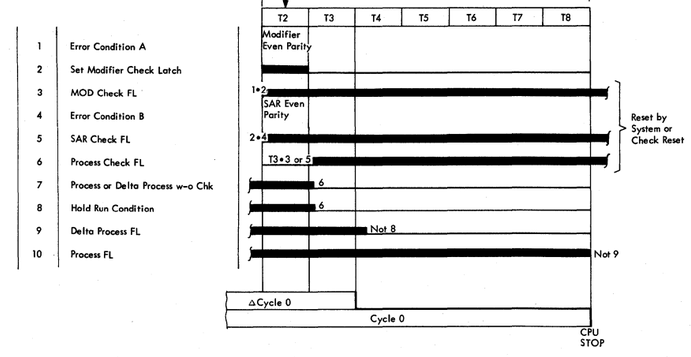


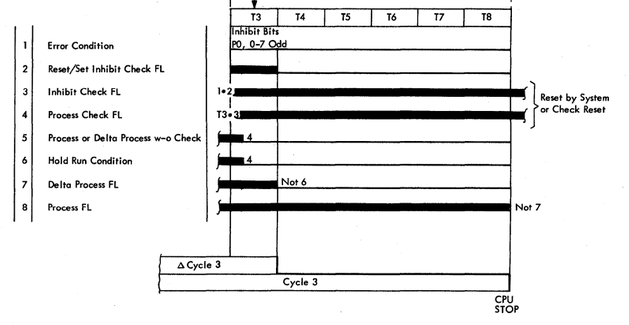
Note: Timing of the set check signals is taken from Diagram 5-57 in Volume 2.

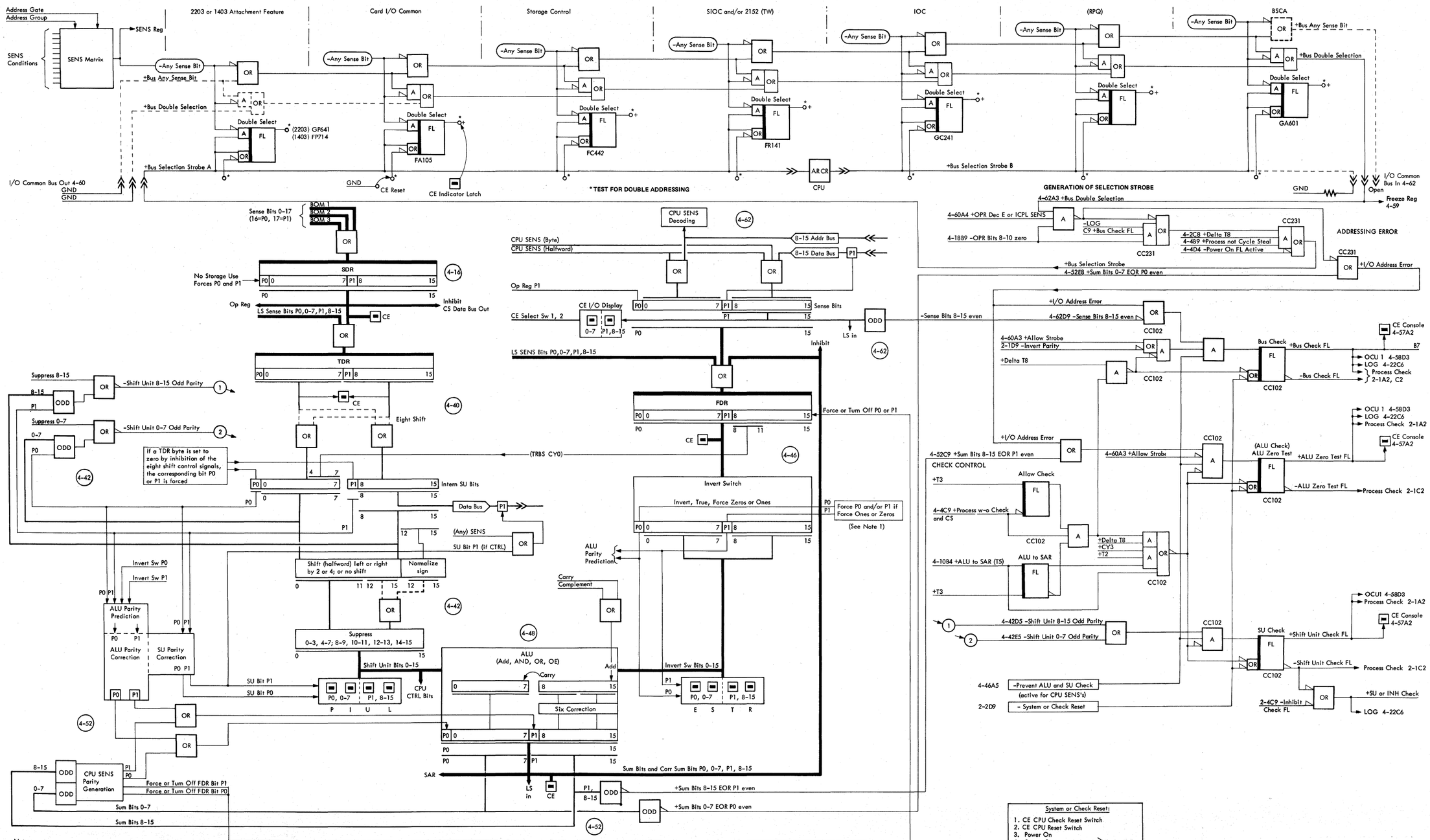
CPU Check Stop Timing

A CPU check during a delta cycle period stops the CPU at the end of the associated cycle (processing period); and exception is the LSA check at T3, which stops the CPU after the next cycle.









System or Check Reset:
1. CE CPU Check Reset Switch
2. CE CPU Reset Switch
3. Power On
4. System Reset
5. Load Key operated for: ICPL, CPL, Cust Prgm Load

LOG Reset CY3, T6

Notes:
1. Except for TRBS, all CPU operations perform invert switch functions on byte format. During TRBS CY0, bits 8-11 are forced to zero (half byte). The parity of T, R display can be wrong. To obtain correct parity at ALU output, FDR bits 8-11 are moved to SU, where they cause a change of the predicted parity bit P1. A change is necessary if an odd number of turned-on bits is forced to zero
2. The circled numbers (for example, (4-42)) refer to the associated functional units in Section 4

Part of standard timing chart used to represent CPU basic operations (see Section 5 in Volume 2). The unshaded signals have to be considered in the case of:
ALU Check
SU Check
BUS Check

No	Name	ALD
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to INH	HA401
48	ALU to SAR	KB411
49		
50	Data Switch to OP REG	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
67	Set ALU Zero Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set MOD Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set BUS Check	
74	Set SAR Check	CC101
75	Set INH Check	

SU Check
ALU Check
BUS Check
ALU and SU Check at T5 and T2. T2 only when CY3
Prevent Checks for CPU SENS's

Read / Write
Cycle 0 / Cycle 1 / Cycle 3
T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8

CPU STOP

ALU to SAR

1	Error Condition
2	ALU to SAR
3	ALU to SAR FL
4	CY3
5	Reset/Set SU and ALU Check FL
6	SU Check FL
7	Process Check FL
8	Process or Delta Proc w-o Check
9	Hold Run Condition
10	Delta Process FL
11	Process FL

Shift Unit 0-7 even parity
2 — T3
T2•3•4
5•1
1•5
T3•6
6
7
Not 9
Not 10

Reset by System or Check Reset

LSA | Any Chk | LSA/MOD | Any Chk | LSA/MOD | Any Chk | LSA | Any Chk

T8 | Set Process Check | Set SU Check | Set Bus Check | ΔT8

ALU to LS or INH

1	Error Condition A
2	Error Condition B
3	Allow Check FL
4	ALU to SAR FL
5	Delta T8
6	Allow Strobe
8	SU Check FL
9	ALU Zero Test FL
10	Process Check FL
11	Process or Delta Proc w-o Check
12	Hold Run Condition
13	Delta Process FL
14	Process FL

T7 T8 T1 T2 T3 T4 T5 T6 T7 T8
Shift Unit 8-15 even parity
Sum Bits 8-15 FOR P1 even
Not 11
1•3• Not 4•5
2•3• Not 4•5• Not 6
T3•8 or 9
8 or 9
10
Not 12
Not 13
Reset by System or Check Reset
Δ Cycle 1
Cycle 0 — Repeat Cycle 0
CPU STOP

Bus Check – Double Addressing

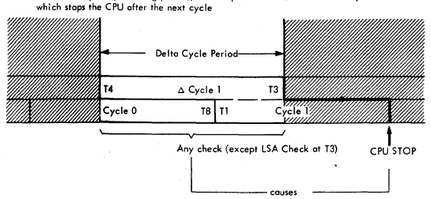
1	Bus Double Selection
2	OPR Dec E or ICPL SENS
3	Bus Selection Strobe A/B
4	Double Select FL's
5	I/O Address Error
6	Allow Check FL
7	Allow Strobe
8	Delta T8
9	Bus Check FL
10	Process Check FL
11	Process or Delta Proc w-o Check
12	Hold Run Condition
13	Delta Process FL
14	Process FL

T7 T8 T1 T2 3 4 5 6 7 8
ΔT8 •1•2
See Note
Not 2
Not 11
2 — Not 2
5•8
T3•9
9
10
No 12
Not 13
Reset by System or Check Reset
Δ Cycle 0
Cycle — Repeat Cycle
CPU STOP

Delta Cycle
Cycle

CPU Check Stop Timing

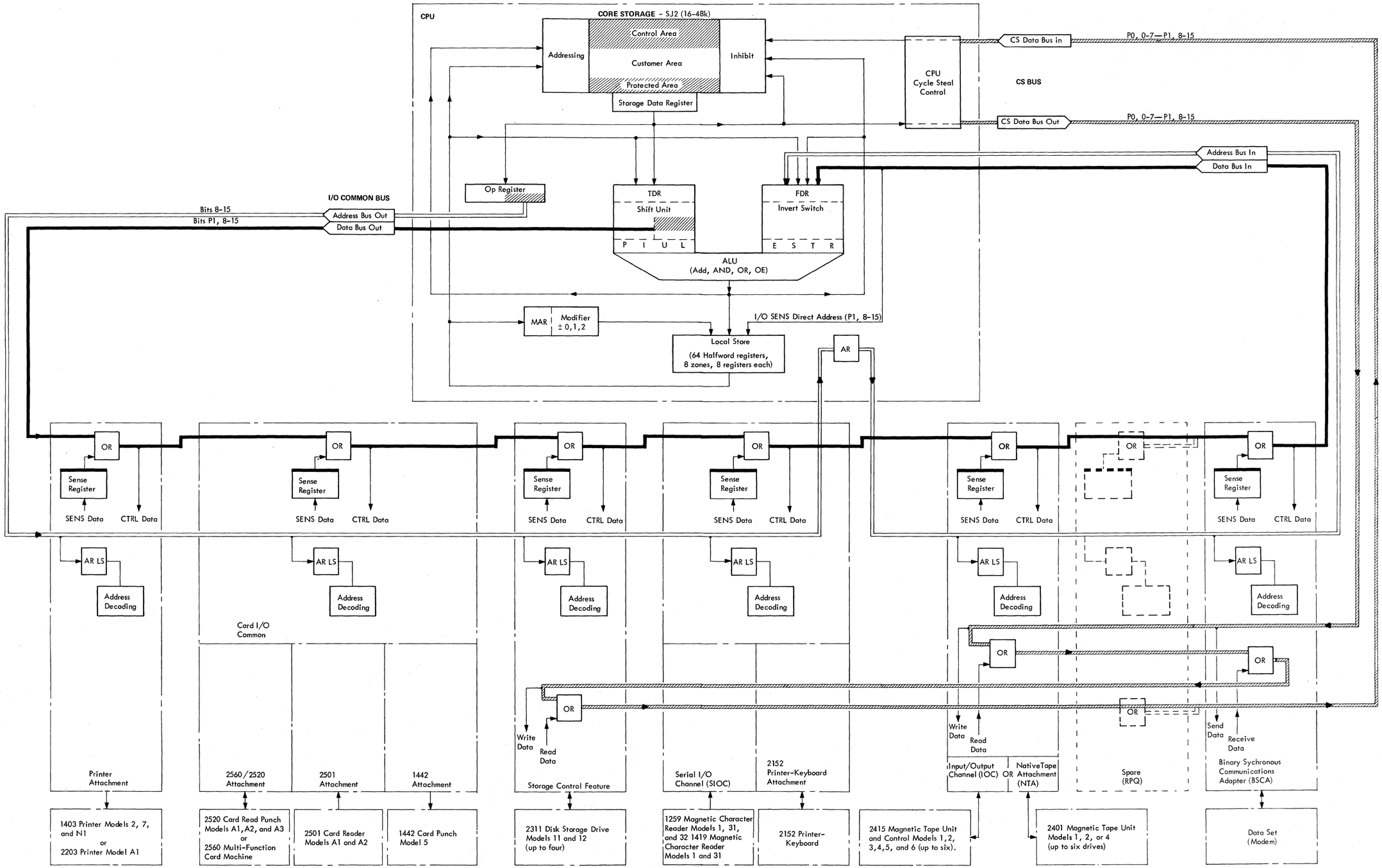
A CPU check during a delta cycle period stops the CPU at the end of the associated cycle (processing period); an exception is the LSA check at T3, which stops the CPU after the next cycle



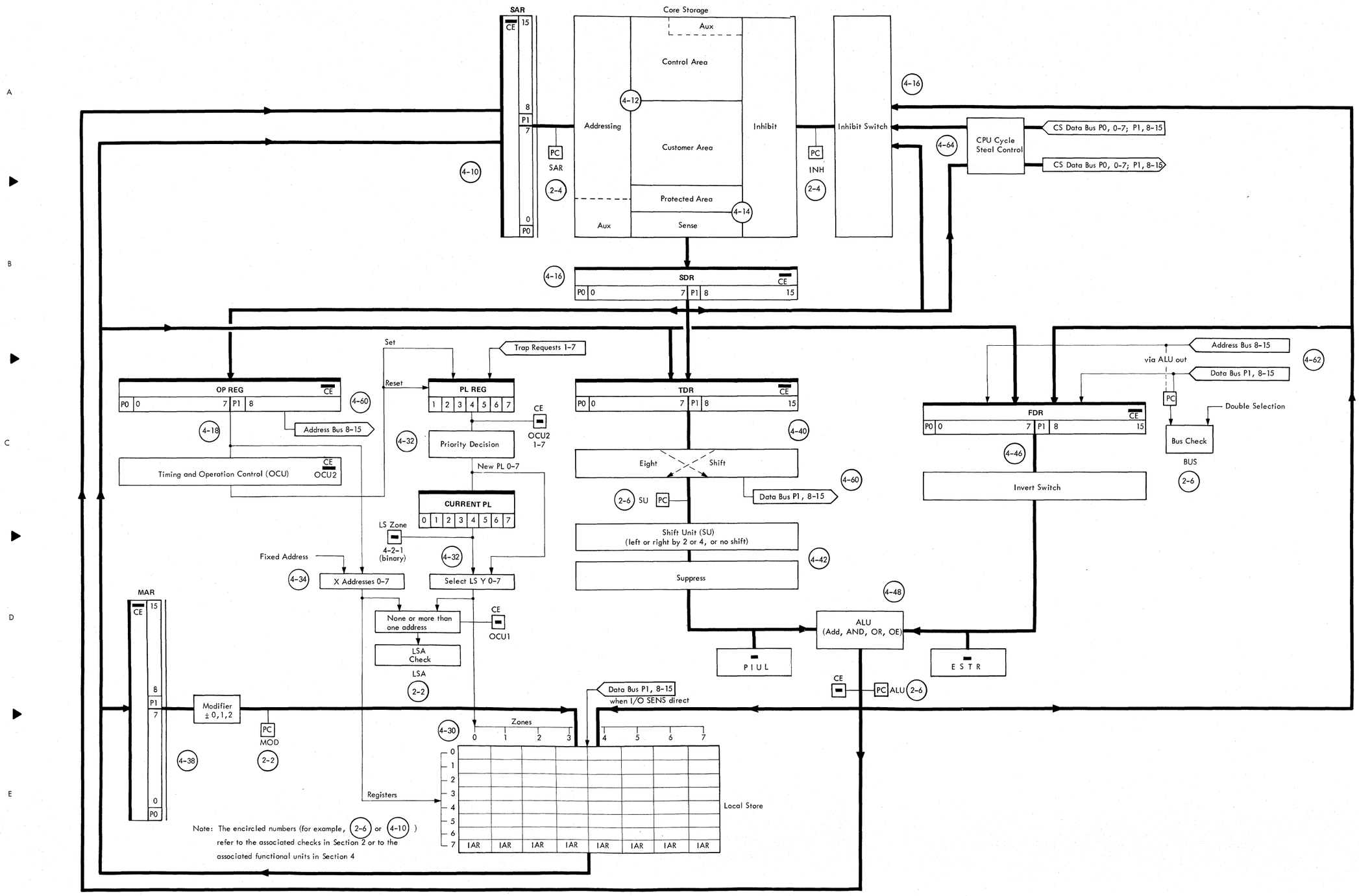
Note: The Double Select FL's are reset as follows:

1. During power-on
2. When the CE connects reset input to ground
3. When the next Selection Strobe comes up

● Diagram 2-7. Timing of ALU, MOD, and SU Check (04011A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)



• Diagram 3-1. System Data Flow (04012B) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)



Note: The encircled numbers (for example, (2-6) or (4-10)) refer to the associated checks in Section 2 or to the associated functional units in Section 4

Diagram 3-2. CPU Data Flow (04013A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)

2 3 4 5 6 7 8 9

A B C D E

C9 +Bus Lamp Test Switch

15 +Invert Sw Bit 15
+Invert Sw Bit 14
+Invert Sw Bit 13
+Invert Sw Bit 12
+Invert Sw Bit 11
+Invert Sw Bit 10
+Invert Sw Bit 9
+Invert Sw Bit 8
46D9 +Invert Sw Bit P1
+Invert Sw Bit 7
+Invert Sw Bit 6
+Invert Sw Bit 5
+Invert Sw Bit 4
+Invert Sw Bit 3
+Invert Sw Bit 2
+Invert Sw Bit 1
+Invert Sw Bit 0
P0 +Invert Sw Bit P0

15 +Shift Unit Bit 15
+Shift Unit Bit 14
+Shift Unit Bit 13
42C/D9 +Shift Unit Bit 12
+Shift Unit Bit 11
+Shift Unit Bit 10
+Shift Unit Bit 9
8 +Shift Unit Bit 8
52B6 +SU Bit P1
7 +Shift Unit Bit 7
+Shift Unit Bit 6
+Shift Unit Bit 5
+Shift Unit Bit 4
+Shift Unit Bit 3
+Shift Unit Bit 2
+Shift Unit Bit 1
0 +Shift Unit Bit 0
52D6 +SU Bit P0
4D9 +Turn On Stop Light

+20V Switch Common from Laminar Bus (PS)

SCRID* OR PA221 PA211 PA231 PA241 PA271

C9 +Bus Lamp Test Switch
WC361 +2520 or 2560 Indicator
WC361 +2501 Indicator
2-02 +Process Check FL
SCRID* OR PA261

62A2 +Bus Printer Indicator
62A2 +Bus Tw Indicator
WC361 +1442 Indicator
SCRID* OR PA261

WC541 +IOC Indicator
62A2 +Bus SIOC Indicator
WC541 +File Indicator
SCRID* OR PA261

P1 11 12 15 | P0 3 4 7 | P1 11 12 15

U L P I — P 8 4 2 1 / 8 4 2 1
E S T R — P 8 4 2 1 / 8 4 2 1

ATTENTION
PROCESS LINE FAILURE POWER THERMAL PRINTER SIOC
CARD I/O 1 | CARD I/O 2 | CARD I/O 3 | 2152 | STOR CTRL | IOC

DATA 1 2
REGISTER DATA (or) ADDRESS 1 2 3 4

START STOP LOAD SYSTEM RESET I/O CHECK RESET

PROCESS
INSN STEP ADR STOP
STOR DPLY DPLY REG
STOR ALTER ALTER REG
STOR SCAN STOR FILL
CPL

POWER ON POWER OFF
See Note

PULL (Emergency Power Off) See Note
CE Meter
(CPU Serial No.) 50,000 and above
Off On TIME SHARING LAMP TEST
Customer Meter
CE (CE Key Sw)

*SCRID PRINCIPLES
7.25V ac from PS
7.25V ac for indicators
SCRID Common (Gnd)
SCR
+Bit
+Lamp Test Sw
OR

CUSTOMER ADDRESS SWITCHES
+20V Switch Common
Data 1 Data 2 Addr 1 Addr 2 Addr 3 Addr 4
Sw Rot N
PA131 PA141 PA151 PA161 PA171 PA181

CUSTOMER DATA SWITCHES
+Data Sw 1 Bit 1 INT
+Data Sw 1 Bit 2 INT
+Data Sw 1 Bit 4 INT
+Data Sw 1 Bit 8 INT
+Data Sw 2 Bit 1 INT
+Data Sw 2 Bit 2 INT
+Data Sw 2 Bit 4 INT
+Data Sw 2 Bit 8 INT
+Addr Sw 1 Bit 1 INT
+Addr Sw 1 Bit 2 INT
+Addr Sw 1 Bit 4 INT
+Addr Sw 1 Bit 8 INT
+Addr Sw 2 Bit 1 INT
+Addr Sw 2 Bit 2 INT
+Addr Sw 2 Bit 4 INT
+Addr Sw 2 Bit 8 INT
+Addr Sw 3 Bit 1 INT
+Addr Sw 3 Bit 2 INT
+Addr Sw 3 Bit 4 INT
+Addr Sw 3 Bit 8 INT
+Addr Sw 4 Bit 1 INT
+Addr Sw 4 Bit 2 INT
+Addr Sw 4 Bit 4 INT
+Addr Sw 4 Bit 8 INT

+20V Switch Common
OP REG 18A3
I/O Common Bus In 62C7/9

CUSTOMER MODE SWITCH
Mode Sw Rot PA111
-Single Instruction Mode INT
-Address Stop Mode INT
-Display Register Mode INT
-Alter Register Mode INT
-Storage Fill Mode INT
-Storage Scan Mode INT
-Storage Alter Mode INT
-Storage Display Mode INT
-Initial Ctrl Prog Load INT
LS Write 36E4
I/O Common Bus In B2B7, B9, C4
MANOP 20A2

Lamp Test Gnd NC Sw Mom NO +3V Op +Bus Lamp Test Sw → CE Console 57E3, I/O Common Bus Out 60E9, A2, A5
Time Sharing Sw Tog PA126 Op -Time Sharing Sw INT → I/O Common Bus In 62A8

CE Key Sw Op NO NC
-CE Key Sw INT
+20V CE Key Sw N/O
+20V CE Key Sw N/C
→ I/O Common Bus In 62A8, MANOP 20A2, Inhibit Control 16E4, CE Console 57D2

WC221 41V ac 1
RR1
I/O Common Bus In 62, E7/C7/C9 WC221 41V ac 2
PA111
Meter CE Meter CUST
PA191
+20V Switch Common

+Sw Bit 1 INT
+Sw Bit 2 INT
+Sw Bit 4 INT
+Sw Bit 8 INT
Integrators
Bit 1 Bit 2 Bit 4 Bit 8

Switch Abbreviations:
PB = Push Button
Rot = Rotary
Tog = Toggle
Mom = Momentary

NOTE: For wiring of Power On/Off keys, Emergency Power Off switch, and the attention indicators 'Line Failure', 'Power', and 'Thermal', refer to ALD YB045 (50Hz) or ALD YB145 (60Hz)

CONSOLE KEYS
Start Sw PB NC NO N Op
Stop Sw PB NC NO N Op
PA121
57C9 +20V Rem Stop Key N/O
57C9 +20V Rem Reset Key N/O

Load Sw PB NC NO N Op
System Reset Sw PB NC NO N Op
I/O Check Res Sw PB NC NO N Op
PA121

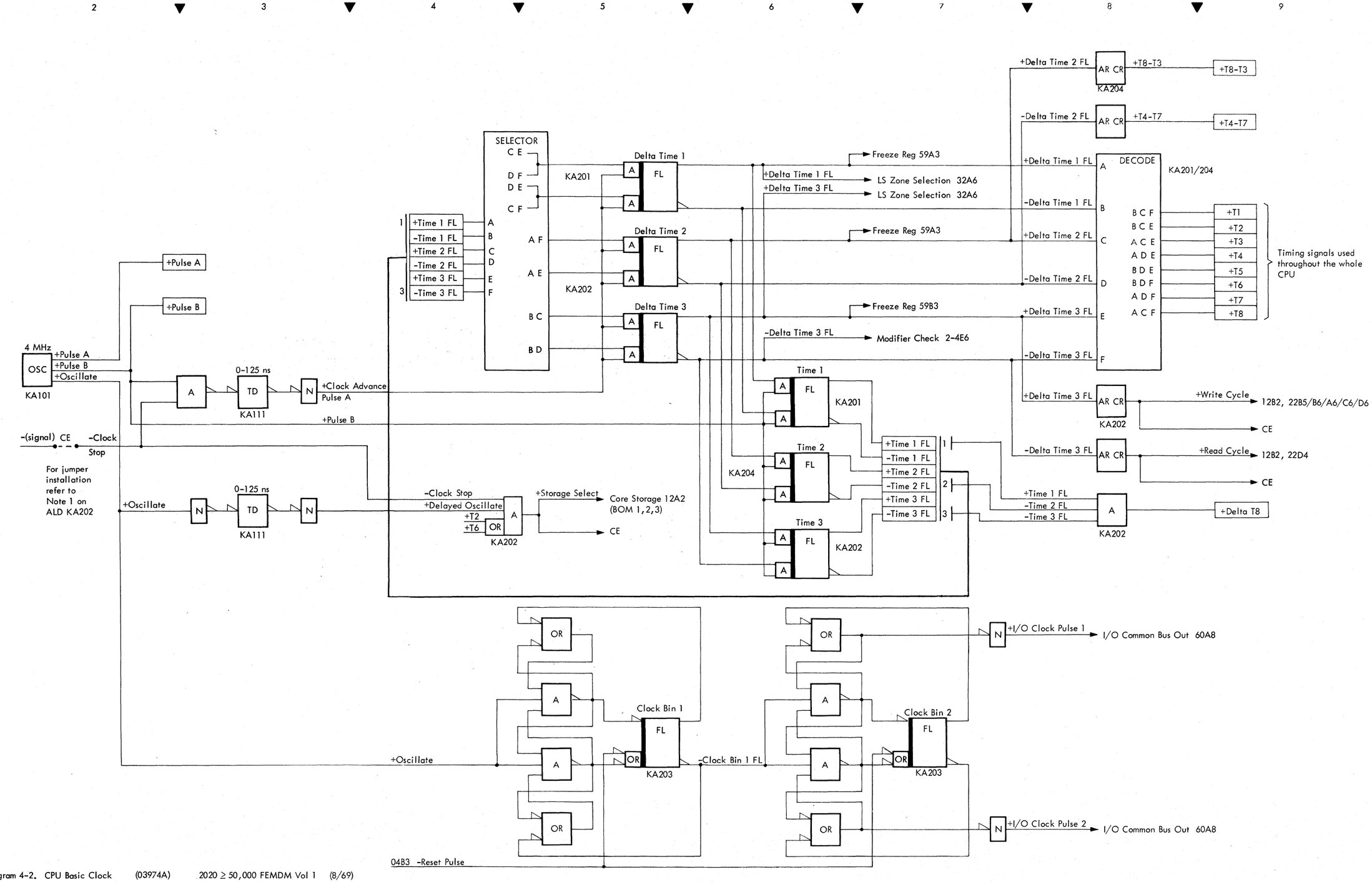
+Load Key INT
-Load Key INT
+System Reset Key INT
-System Reset Key INT
+I/O Check Reset Key INT
+Start Key INT
-Start Key INT
-Stop Key INT
→ Run Control 4-4
→ I/O Common Bus Out 60D7

USEMETER CONTROL
4A9 +Process
62A2 -Bus BSCA Wait
62B5 -Set Process Meter
A KA502 OR PA301 OR SS OR
-Process Meter Ctrl
H RR1 P RR1 PA191 +3V
-CE Key Sw INT
A -Process Meter Go → I/O Common Bus Out 60E7

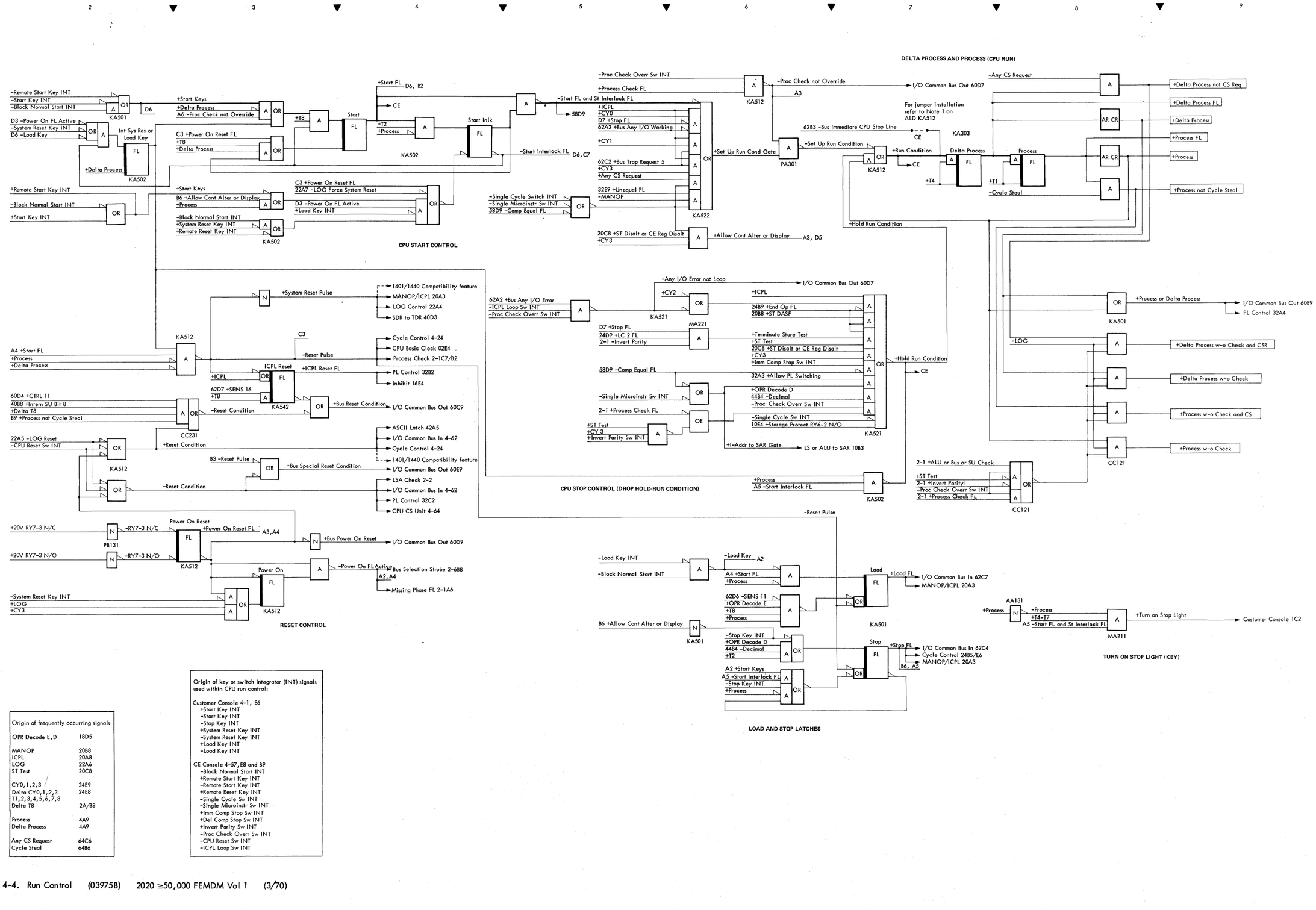
12880

Data and Address Switch Principles

● Diagram 4-1. Customer Console (03973A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)



● Diagram 4-2. CPU Basic Clock (03974A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)



Origin of frequently occurring signals:

OPR Decode E,D	18D5
MANOP	20B8
ICPL	20A8
LOG	22A6
ST Test	20C8
CY0,1,2,3	24E9
Delta CY0,1,2,3	24E8
T1,2,3,4,5,6,7,8	
Delta T8	2A/B8
Process	4A9
Delta Process	4A9
Any CS Request	64C6
Cycle Steal	64B6

Origin of key or switch integrator (INT) signals used within CPU run control:

Customer Console 4-1, E6
- +Start Key INT
- -Start Key INT
- -Stop Key INT
- +System Reset Key INT
- -System Reset Key INT
- +Load Key INT
- -Load Key INT

CE Console 4-57, E8 and B9
- -Block Normal Start INT
- +Remote Start Key INT
- -Remote Start Key INT
- +Remote Reset Key INT
- -Single Cycle Sw INT
- -Single Microinstr Sw INT
- +Imm Comp Stop Sw INT
- +Del Comp Stop Sw INT
- +Invert Parity Sw INT
- -Proc Check Overr Sw INT
- -CPU Reset Sw INT
- -ICPL Loop Sw INT

• Figure 4-4. Run Control (03975B) 2020 ≥50,000 FEMDM Vol 1 (3/70)

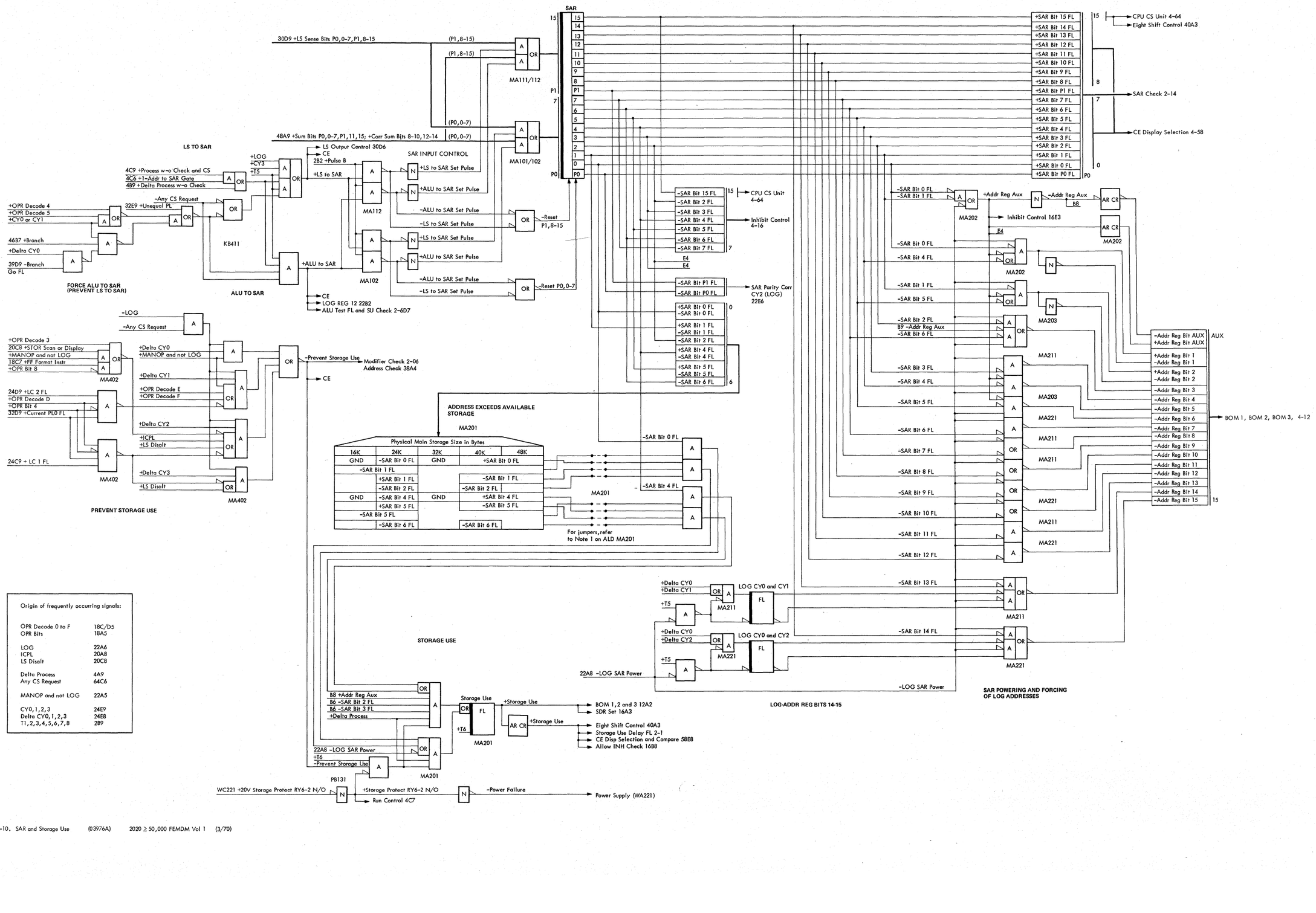


Diagram 4-10. SAR and Storage Use (03976A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)

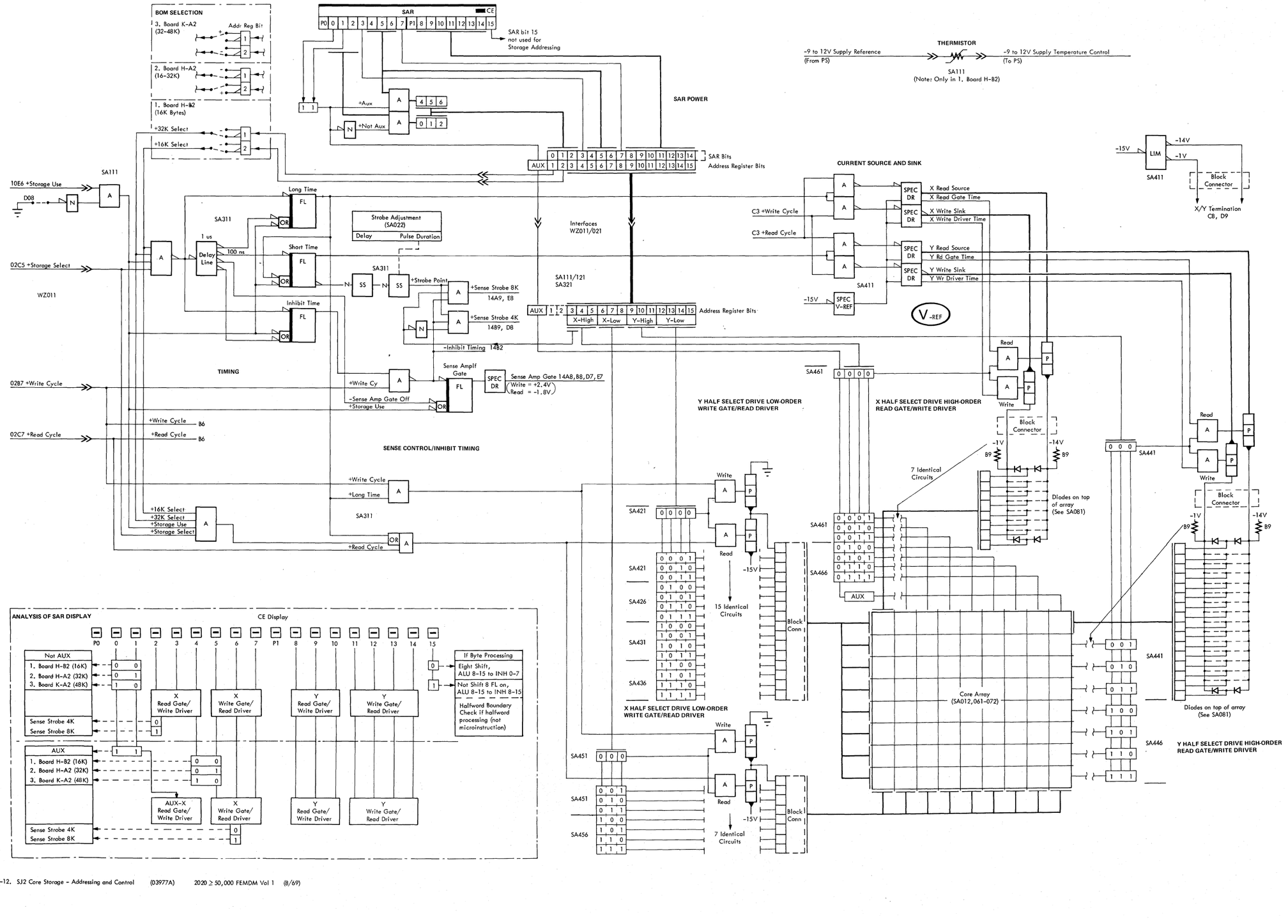


Diagram 4-12. SJ2 Core Storage - Addressing and Control (03977A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)

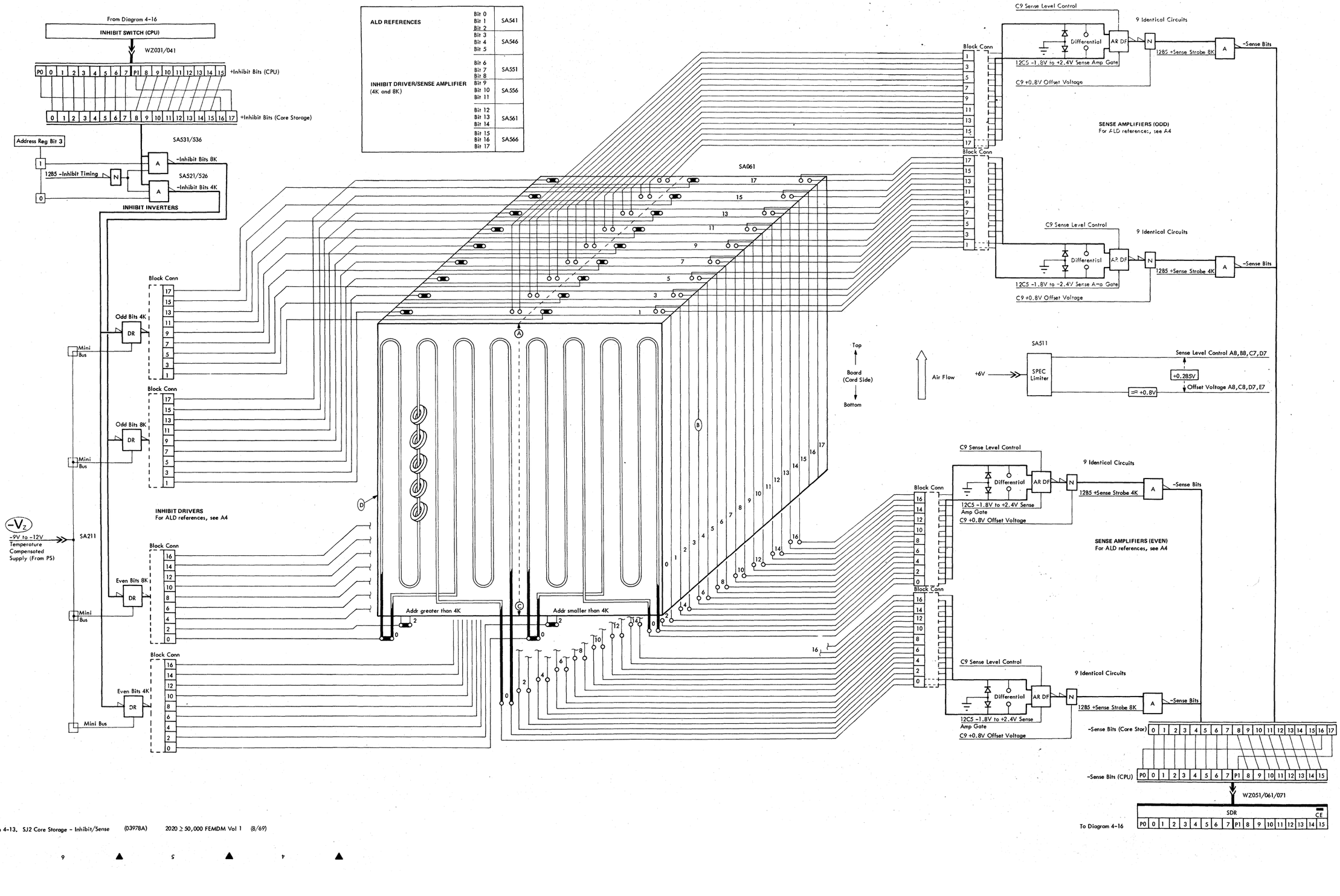
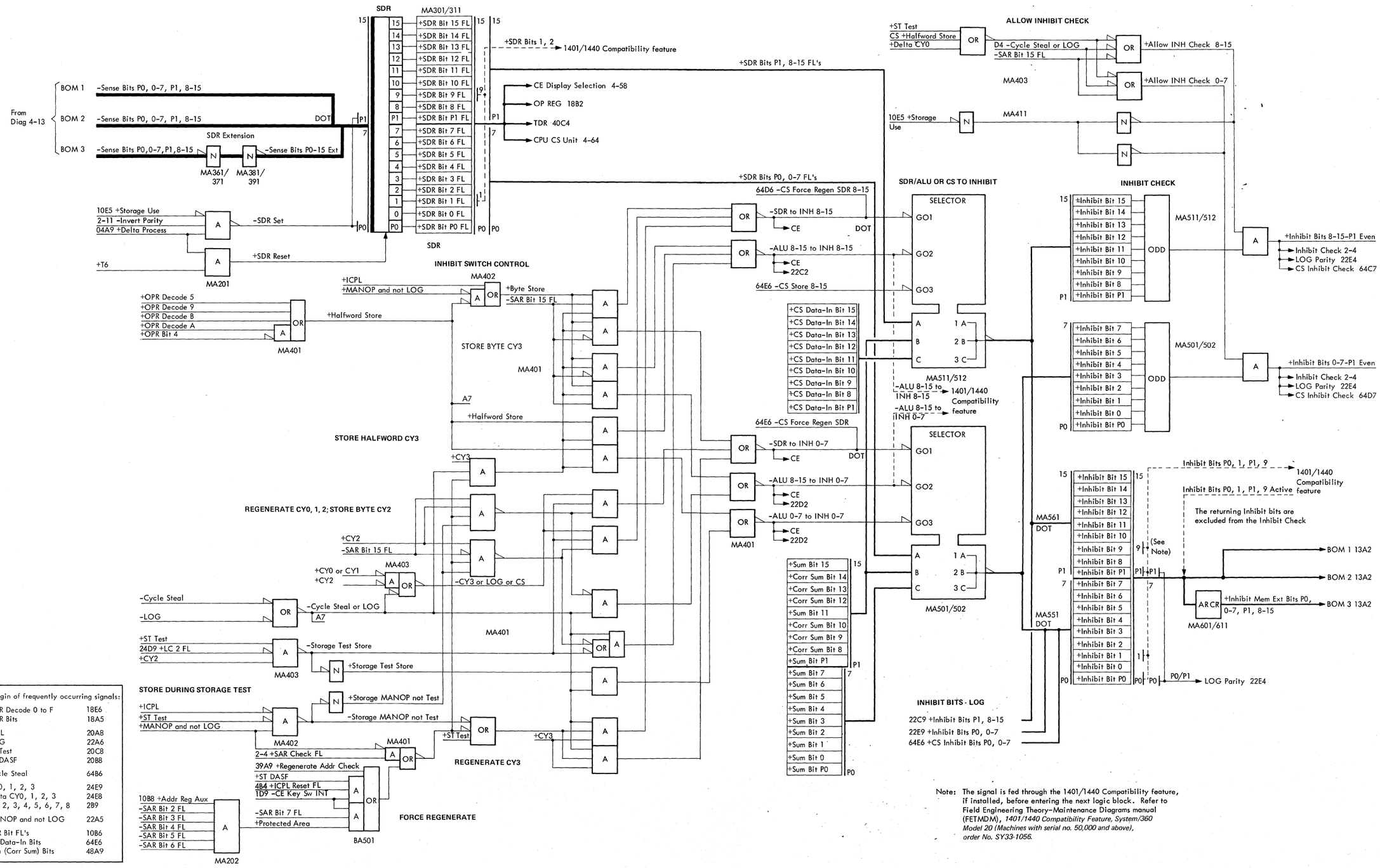
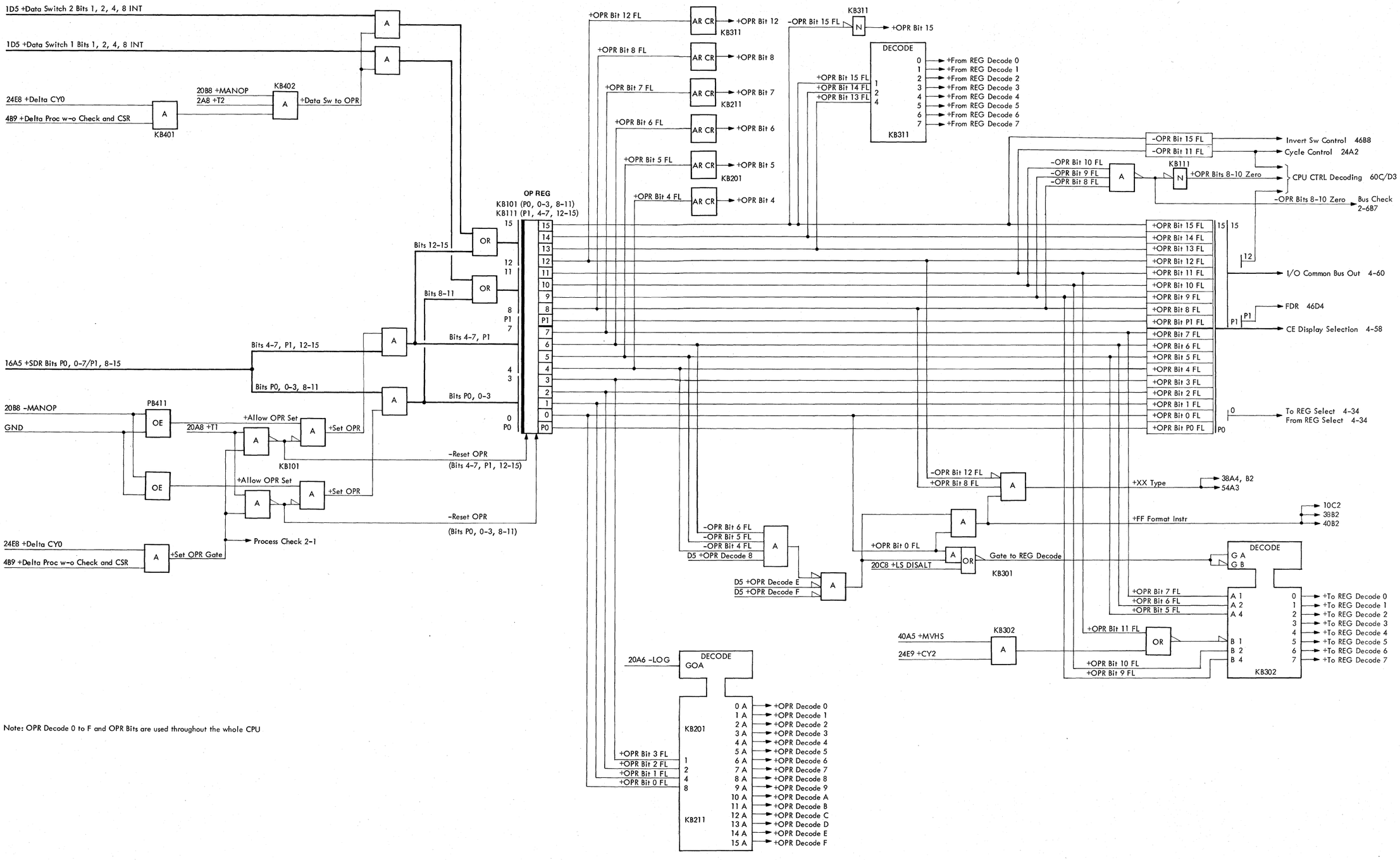


Diagram 4-13. SJ2 Core Storage - Inhibit/Sense (03978A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)



Origin of frequently occurring signals:	
OPR Decode 0 to F	18E6
OPR Bits	18A5
ICPL	20A8
LOG	22A6
ST Test	20C8
ST DASF	20B8
Cycle Steal	64B6
CY0, 1, 2, 3	24E9
Delta CY0, 1, 2, 3	24E8
T1, 2, 3, 4, 5, 6, 7, 8	2B9
MANOP and not LOG	22A5
SAR Bit FL's	10B6
CS Data-In Bits	64E6
Sum (Corr Sum) Bits	48A9

Note: The signal is fed through the 1401/1440 Compatibility feature, if installed, before entering the next logic block. Refer to Field Engineering Theory-Maintenance Diagrams manual (FETMDM), *1401/1440 Compatibility Feature, System/360 Model 20 (Machines with serial no. 50,000 and above), order No. SY33-1056.*



Note: OPR Decode 0 to F and OPR Bits are used throughout the whole CPU

Diagram 4-18. Op Register and Op Register Decoding (03980A) 2020 ≥ 50,000 FEMDM Vol (3/70)

2 3 4 5 6 7 8 9

A B C D E

Switch Integrator Signals from Customer Console 4-01(D7) and CE Console (CE) 4-57(E8)

CE -Initial Ctrl Prog Load INT
CE +CE Mode Sw INT
CE -CE Key Sw INT
CE -ICPL Loop Sw INT
CE -Storage Alter Mode INT
CE -Storage Display Mode INT
CE -Storage Fill Mode INT
CE -Storage Scan Mode INT
CE -Storage Test Sw INT

4D7 +Load FL
-Log
+ Allow ICPL
+CY3
+T6
ICPL FL
KA532
04B4 +System Reset Pulse
OR
KA531
+ICPL
24B9 +End Op FL
+T6
4D7 +Stop FL
Do Not Care
KA531

-Alter
-Displ
-Fill
-Scan
OR
KA531
+Intern ST DASF

-Display Reg Mode INT
-Alter Reg Mode INT
-Displ Reg
-Alt Reg
+CE Mode
OR
KA532
-Intern LS Disalt

-CE Key
N
+CE Key Sw On

-Fill
-ST Test Sw
KA531
+Intern ST Test
N
-Intern ST Test

+Intern ST DASF
-Intern LS Disalt
OR
KA531
+Process
+Delta CY0
+T6
-Log
MANOP FL
+MANOP FL
-Intern MANOP FL

-ICPL FL
-LOG
OR
-MANOP
+MANOP
N
-Bus MANOP
I/O Common Bus Out 60E9
DOT
D5, D6
1401/1440 Compatibility feature
-Prev CS Addr Check 2

-Intern ST Test
+Intern ST DASF
+CE Key Sw On
+CE Mode Sw INT
KA531
KA532
+ST DASF
-ST Fill or Alter not CE Mode
Address Check 39A8/B6

-Storage Alter Mode INT
-Storage Display Mode INT
-Storage Scan Mode INT
-Stor Scan or Fill
+Stor Scan or Display
Cycle Control 24A8, B6, B8
Prevent Storage Use 10C2

+CE Key Sw On
+Intern ST Test
-Intern CE Key and CE Mode Sw
KA531
KA532
+ST Test
+LS Disalt
+LS DISALT
+LS Disalt or LOG
+LS Disalt or Log
LS Write 4-36
X Address 0 34A2
-LOG

-Intern LS Disalt
+Intern ST DASF
-Storage Fill Mode INT
-Storage Scan Mode INT
-Intern LS Disalt
+ST Disalt or CE Reg Disalt
Run Control 4B6

-Intern LS Disalt
-Alter Reg Mode INT
+Intern ST Test
+LC2 FL
+MANOP Set ALU Zero
Process Check 2-1

B6 +MANOP
+CY0
-LOG
-Intern ST Test
-MANOP Inbus to FDR
I/O Bus to FDR 46A4
I/O Common Bus In 62D4

-ICPL FL
+Intern ST DASF
+CY0 or CY1
+Intern ICPL or ST Mode
B6 +MANOP
-MANOP Suppr 0-7
-MANOP Suppr 8-15
Suppress Control 44A6, C6
Suppress Control 44A6, C6
Shift by 2 or 4 42B3
Shift by 2 or 4 42B3

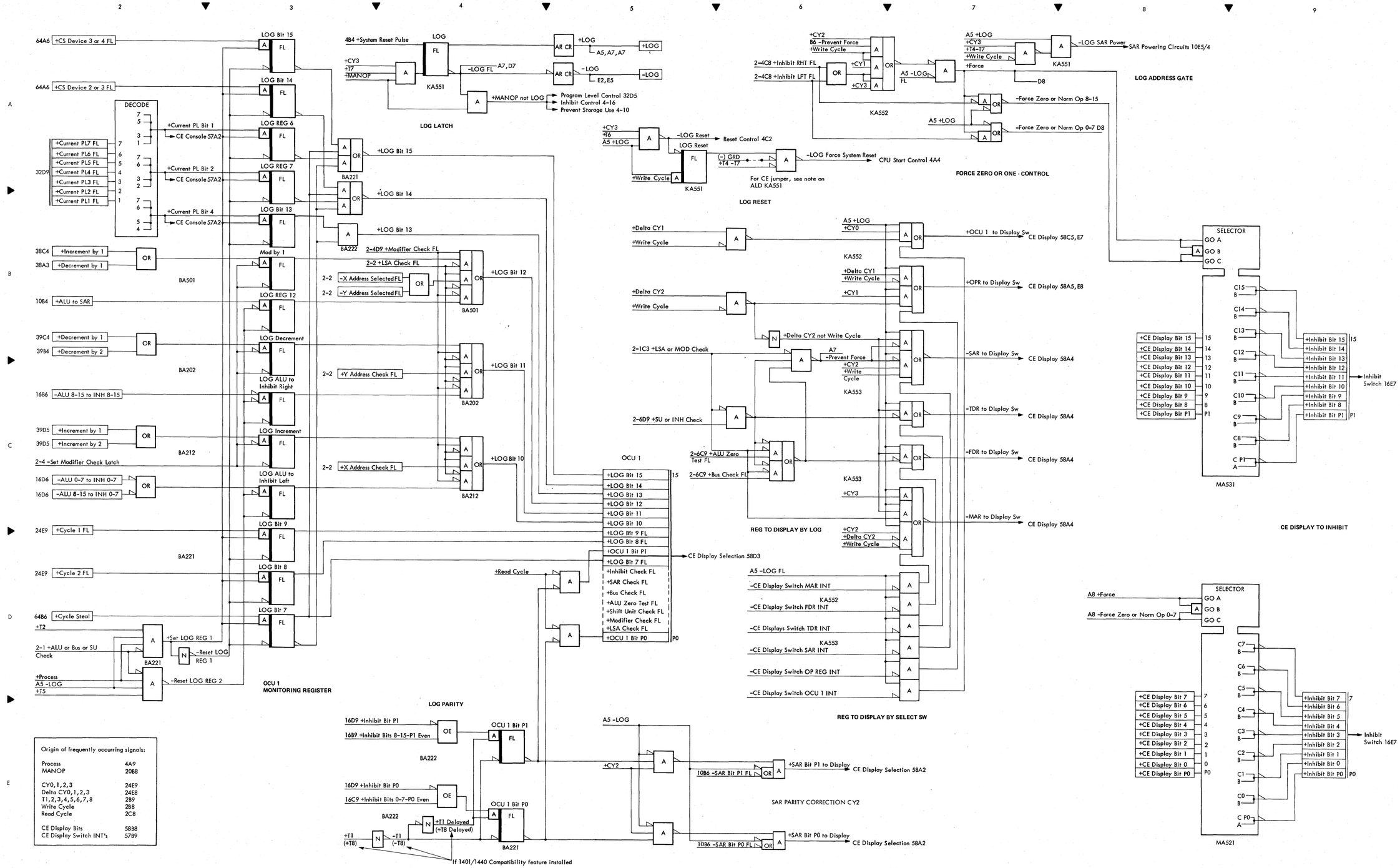
-Intern LS Disalt
+CY0 or CY1
+LC2 FL
+Intern ST Test
+CY3
+Intern ST DASF

Origin of frequently occurring signals:	
Log	22A6
CY0,1,2,3	24E9
Delta CY0,1,2,3	24E8
T1,2,3,4,5,6,7,8	2B9
Process	4A9
LC2 FL	24D9

Note: ICPL, MANOP, ST DASF, ST TEST, and LS DISALT are main control signals used throughout the whole CPU

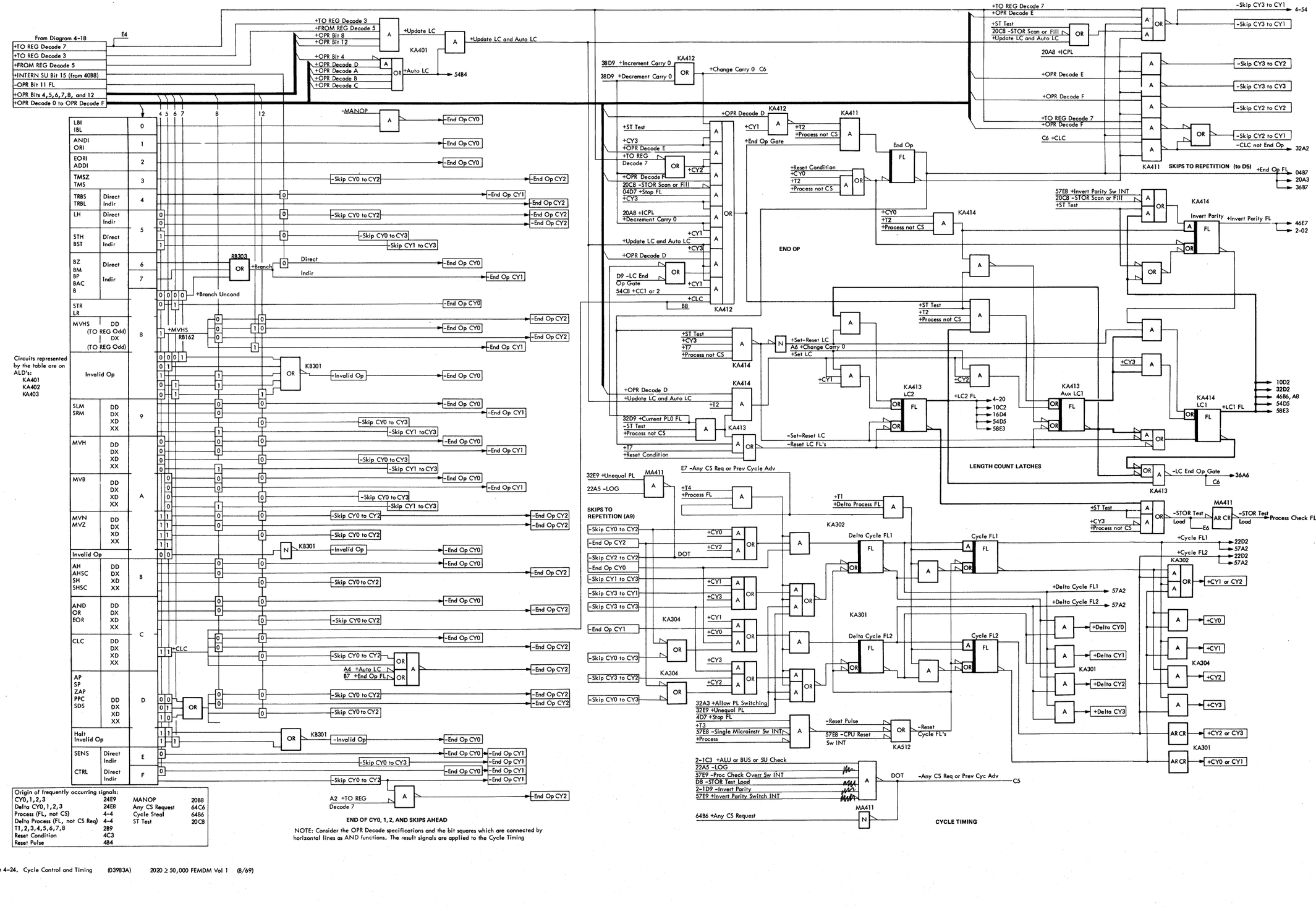
ST DASF = Storage Display, Alter, Scan, or Fill
DISALT = Display or Alter

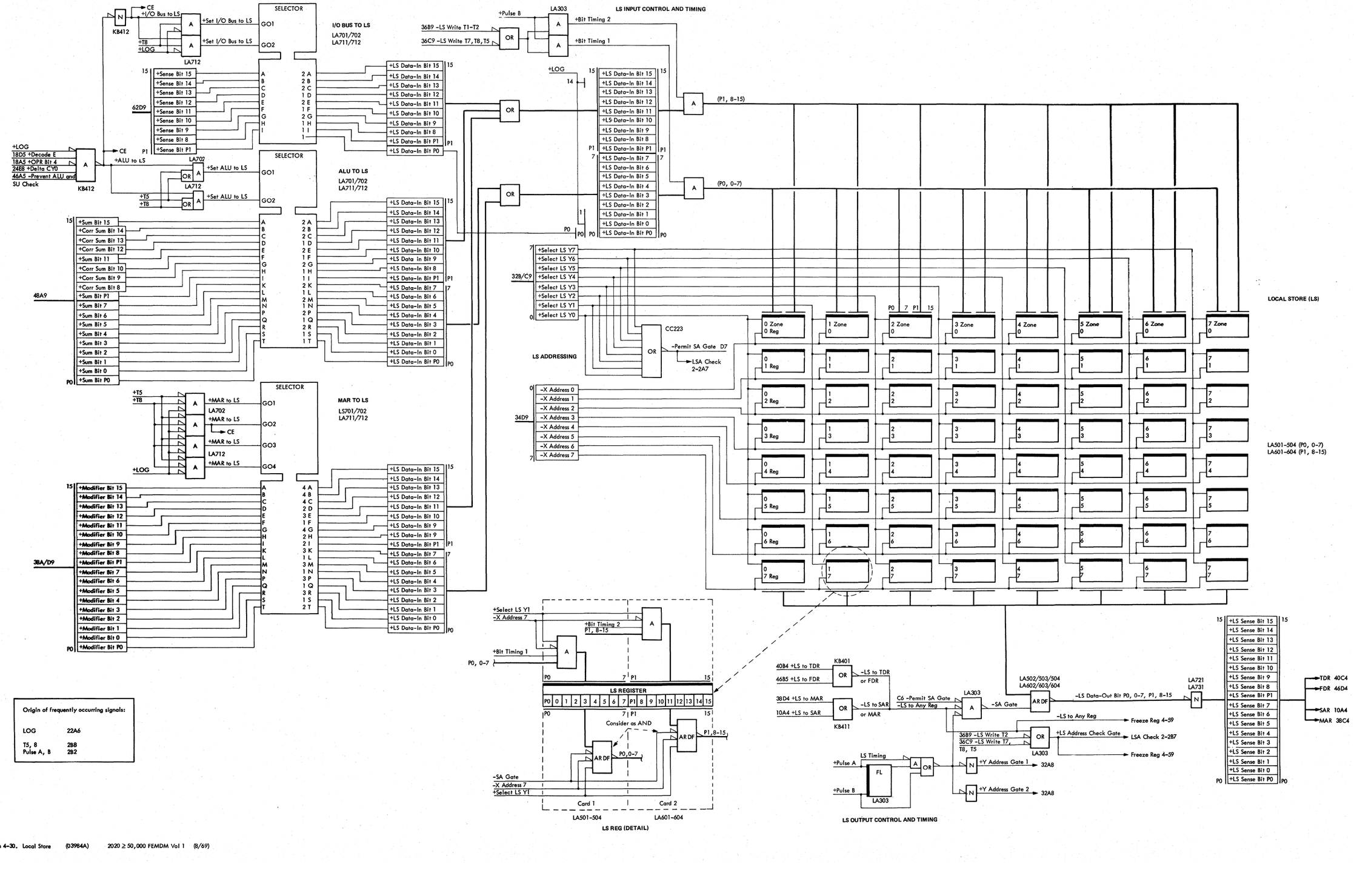
● Diagram 4-20. MANOP and ICPL (03981B) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)

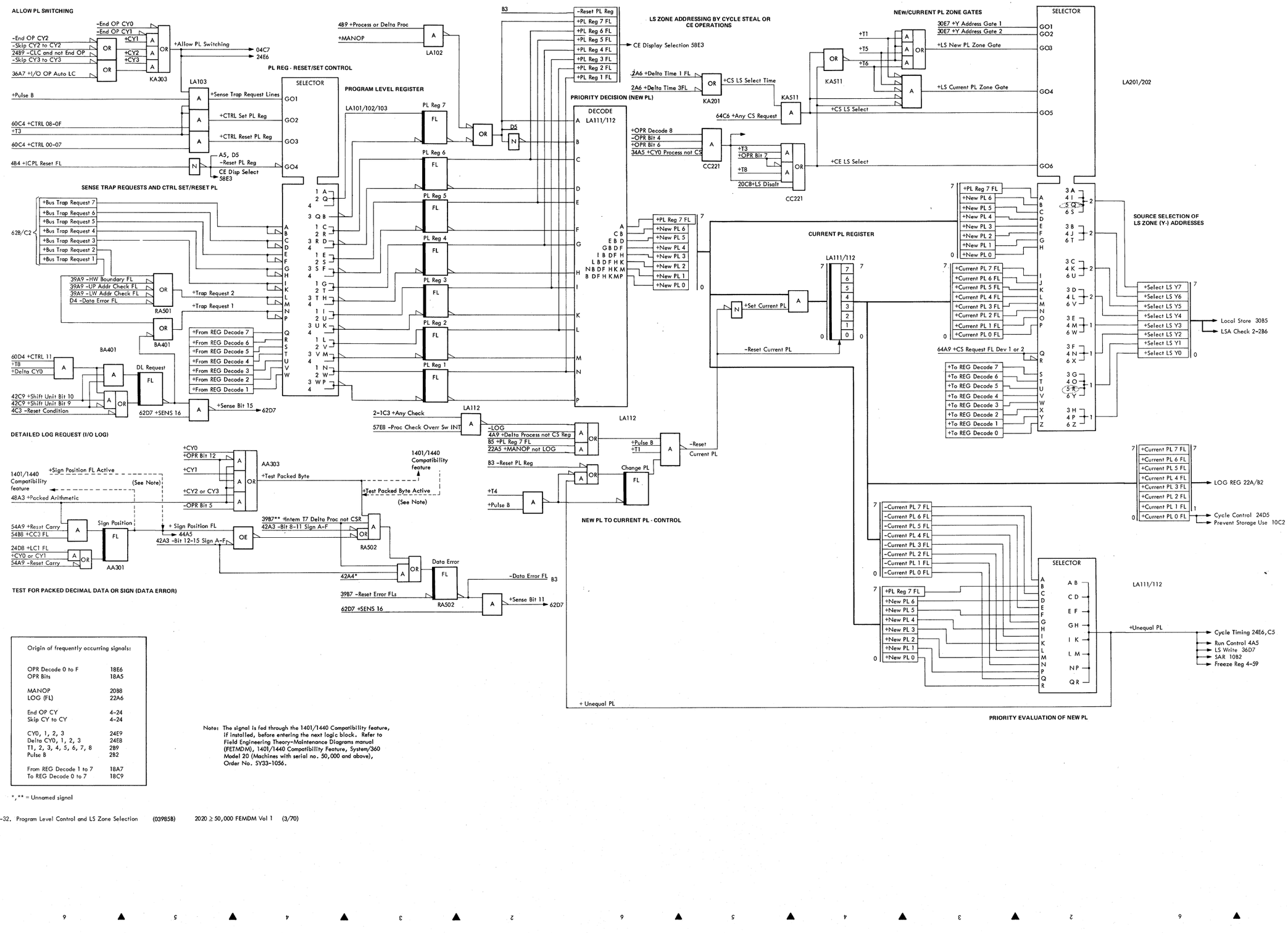


Origin of frequently occurring signals:

Process	4A9
MANOP	20B8
CY0,1,2,3	24E9
Delta CY0,1,2,3	24E8
T1,2,3,4,5,6,7,8	28F9
Write Cycle	28B
Read Cycle	2C8
CE Display Bits	58B8
CE Display Switch INT's	57B9


From Diagram 4-18
+TO REG Decode 7
+TO REG Decode 3
+FROM REG Decode 5
+INTERN SU Bit 15 (from 4088)
-OPR Bit 11 FL
+OPR Bits 4,5,6,7,8, and 12
+OPR Decode 0 to OPR Decode F
E4
+TO REG Decode 3
+FROM REG Decode 5
+OPR Bit 8
+OPR Bit 12
+Update LC
KA401
+Update LC and Auto LC
+OPR Bit 4
+OPR Decode D
+OPR Decode A
+OPR Decode B
+OPR Decode C
+Auto LC
54B4
-MANOP
-End Op CY0
-Skip CY0 to CY2
-End Op CY2
-End Op CY1
-Skip CY0 to CY3
-Skip CY1 to CY3
RB303
+Branch
Direct
Indir
+Branch Uncond
+MVHS
RB162
KB301
-Invalid Op
+CLC
A4 +Auto LC
B7 +End Op FL
A2 +TO REG Decode 7
LBI
IBL
ANDI
ORI
EORI
ADDI
TMSZ
TMS
TRBS
TRBL
LH
STH
BST
BZ
BM
BP
BAC
B
STR
LR
MVHS
DD
(TO REG Odd)
DX
(TO REG Odd)
Invalid Op
SLM
SRM
MVH
MVB
MVN
MVZ
AH
AHSC
SH
SHSC
AND
OR
EOR
CLC
AP
SP
ZAP
PPC
SDS
Halt
Invalid Op
SENS
CTRL
Circuits represented by the table are on ALD's:
KA401
KA402
KA403
Origin of frequently occurring signals:
CY0,1,2,3 24E9
Delta CY0,1,2,3 24E8
Process (FL, not CS) 4-4
Delta Process (FL, not CS Req) 4-4
T1,2,3,4,5,6,7,8 2B9
Reset Condition 4C3
Reset Pulse 4B4
MANOP 2088
Any CS Request 64C6
Cycle Steal 6486
ST Test 20C8
END OF CY0, 1, 2, AND SKIPS AHEAD
NOTE: Consider the OPR Decode specifications and the bit squares which are connected by horizontal lines as AND functions. The result signals are applied to the Cycle Timing
38D9 +Increment Carry 0
38D9 +Decrement Carry 0
KA412
+Change Carry 0 C6
+OPR Decode D
+ST Test
+CY3
+OPR Decode E
+TO REG Decode 7
+OPR Decode F
20C8 -STOR Scan or Fill
04D7 +Stop FL
20A8 +ICPL
+Decrement Carry 0
+Update LC and Auto LC
+OPR Decode D
D9 -LC End Op Gate
54C8 +CC1 or 2
+CLC
B8
+CY1
+T2
+Process not CS
+End Op Gate
KA411
+Reset Condition
+CY0
End Op
FL
END OP
KA414
+ST Test
+CY3
+T7
+Process not CS
+Set-Reset LC
A6 +Change Carry 0
+Set LC
+OPR Decode D
+Update LC and Auto LC
32D9 +Current PL0 FL
-ST Test
+Process not CS
+T7
+Reset Condition
KA413
LC2
Aux LC1
LC1
+LC2 FL
4-20
10C2
16D4
54D5
58E3
-Set-Reset LC
-Reset LC FL's
LENGTH COUNT LATCHES
-LC End Op Gate
C6
36A6
+TO REG Decode 7
+OPR Decode E
+ST Test
20C8 -STOR Scan or Fill
+Update LC and Auto LC
20A8 +ICPL
+OPR Decode E
+OPR Decode F
+TO REG Decode 7
+OPR Decode F
C6 +CLC
-Skip CY3 to CY1
4-54
-Skip CY3 to CY2
-Skip CY2 to CY2
-Skip CY2 to CY1
-CLC not End Op
32A2
SKIPS TO REPETITION (to D5)
+End Op FL
04B7
20A3
36B7
57E8 +Invert Parity Sw INT
20C8 -STOR Scan or Fill
+ST Test
Invert Parity
+Invert Parity FL
46E7
2-02
10D2
32D2
46B6, A8
54D5
58E3
+LC1 FL
SKIPS TO REPETITION (A9)
32E9 +Unequal PL
22A5 -LOG
MA411
+T4
+Process FL
+T1
+Delta Process FL
KA302
DOT
-End Op CY2
-Skip CY2 to CY2
-End Op CY0
-Skip CY1 to CY3
-Skip CY3 to CY1
-Skip CY3 to CY3
-End Op CY1
-Skip CY0 to CY3
KA304
KA301
32A3 +Allow PL Switching
32E9 +Unequal PL
4D7 +Stop FL
+T3
57E8 -Single Microinstr Sw INT
+Process
Delta Cycle FL1
Delta Cycle FL2
Cycle FL1
Cycle FL2
+Delta Cycle FL1
+Delta Cycle FL2
57A2
+Delta CY0
+Delta CY1
+Delta CY2
+Delta CY3
-Reset Pulse
57E8 -CPU Reset Sw INT
KA512
-Reset Cycle FL's
2-1C3 +ALU or BUS or SU Check
22A5 -LOG
57E9 -Proc Check Overr Sw INT
D8 -STOR Test Load
2-1D9 -Invert Parity
57E9 +Invert Parity Switch INT
64B6 +Any CS Request
-Any CS Req or Prev Cyc Adv
C5
CYCLE TIMING
E7 -Any CS Req or Prev Cycle Adv
-STOR Test Load
E6
-STOR Test Load
Process Check FL 2-187
+Cycle FL1
+Cycle FL2
22D2
57A2
22D2
57A2
+CY1 or CY2
+CY0
+CY1
+CY2
+CY3
+CY2 or CY3
+CY0 or CY1

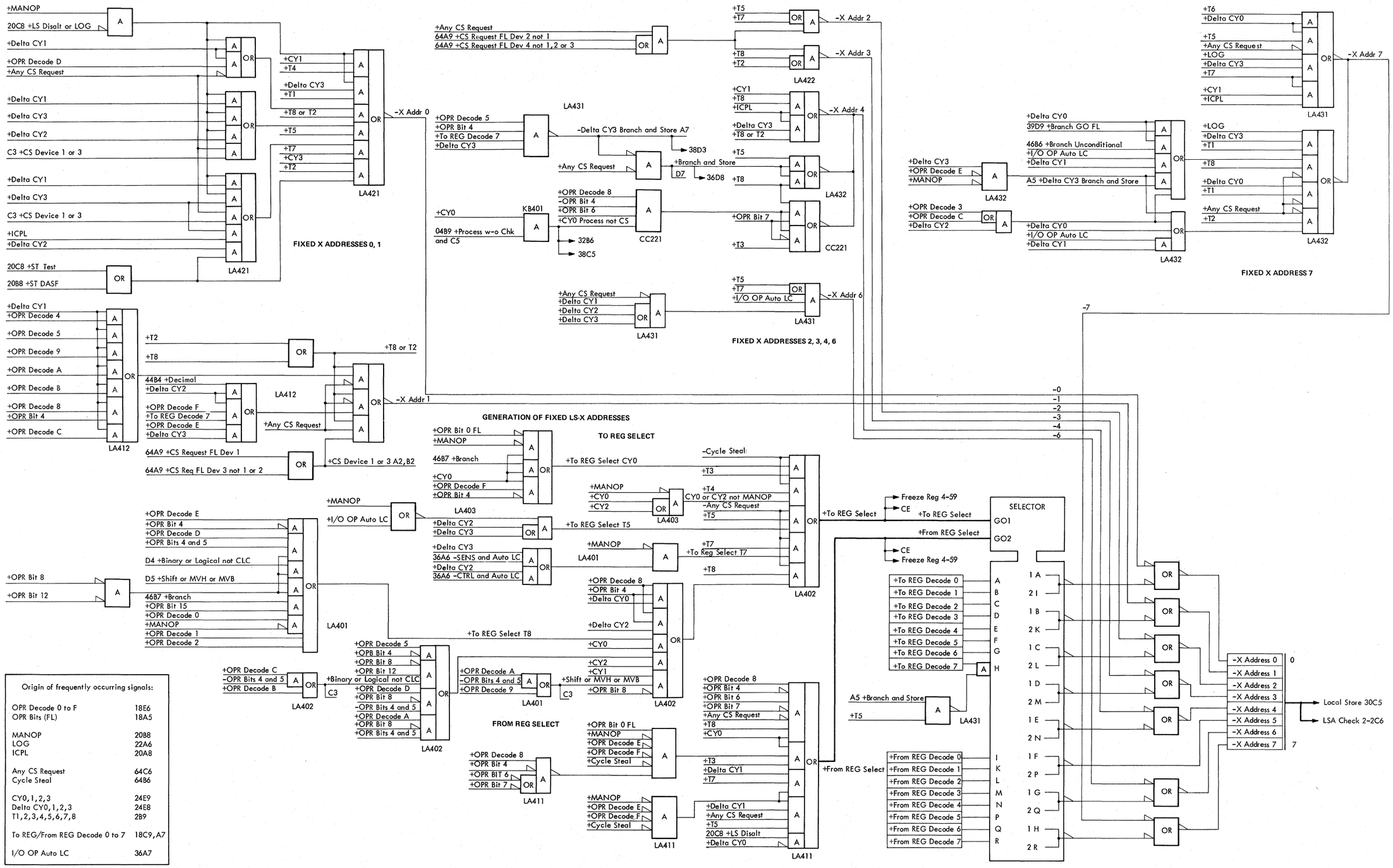

I/O BUS TO LS
LA701/702
LA711/712
ALU TO LS
LA701/702
LA711/712
MAR TO LS
LS701/702
LA711/712
LS INPUT CONTROL AND TIMING
LOCAL STORE (LS)
LS ADDRESSING
LA501-504 (P0, 0-7)
LA601-604 (P1, 8-15)
LS REGISTER
LS REG (DETAIL)
LS OUTPUT CONTROL AND TIMING
Origin of frequently occurring signals:
LOG 22A6
T5, 8 2B8
Pulse A, B 2B2



Origin of frequently occurring signals:	
OPR Decode 0 to F	18E6
OPR Bits	18A5
MANOP	20B8
LOG (FL)	22A6
End OP CY	4-24
Skip CY to CY	4-24
CY0, 1, 2, 3	24E9
Delta CY0, 1, 2, 3	24E8
T1, 2, 3, 4, 5, 6, 7, 8	2B9
Pulse B	2B2
From REG Decode 1 to 7	18A7
To REG Decode 0 to 7	18C9

Note: The signal is fed through the 1401/1440 Compatibility feature, if installed, before entering the next logic block. Refer to Field Engineering Theory-Maintenance Diagrams manual (FETMDM), 1401/1440 Compatibility Feature, System/360 Model 20 (Machines with serial no. 50,000 and above), Order No. SY33-1056.

*,** = Unnamed signal



Origin of frequently occurring signals:

OPR Decode 0 to F	18E6
OPR Bits (FL)	18A5
MANOP	20B8
LOG	22A6
ICPL	20A8
Any CS Request	64C6
Cycle Steal	64B6
CY0,1,2,3	24E9
Delta CY0,1,2,3	24E8
T1,2,3,4,5,6,7,8	2B9
To REG/From REG Decode 0 to 7	18C9,A7
I/O OP Auto LC	36A7

Diagram 4-34. To Reg/From Reg Select and LS X-Addresses (03986A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)

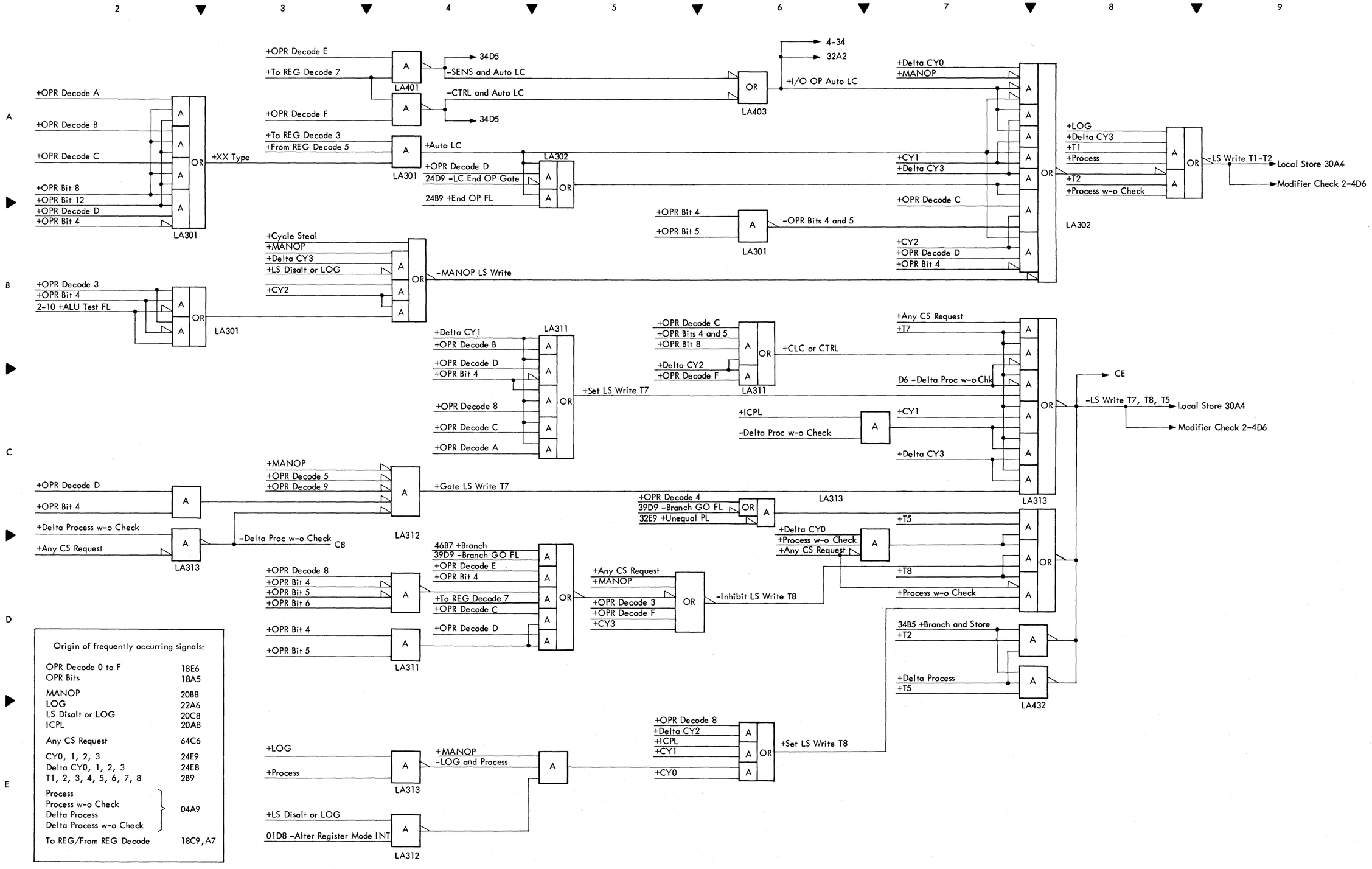
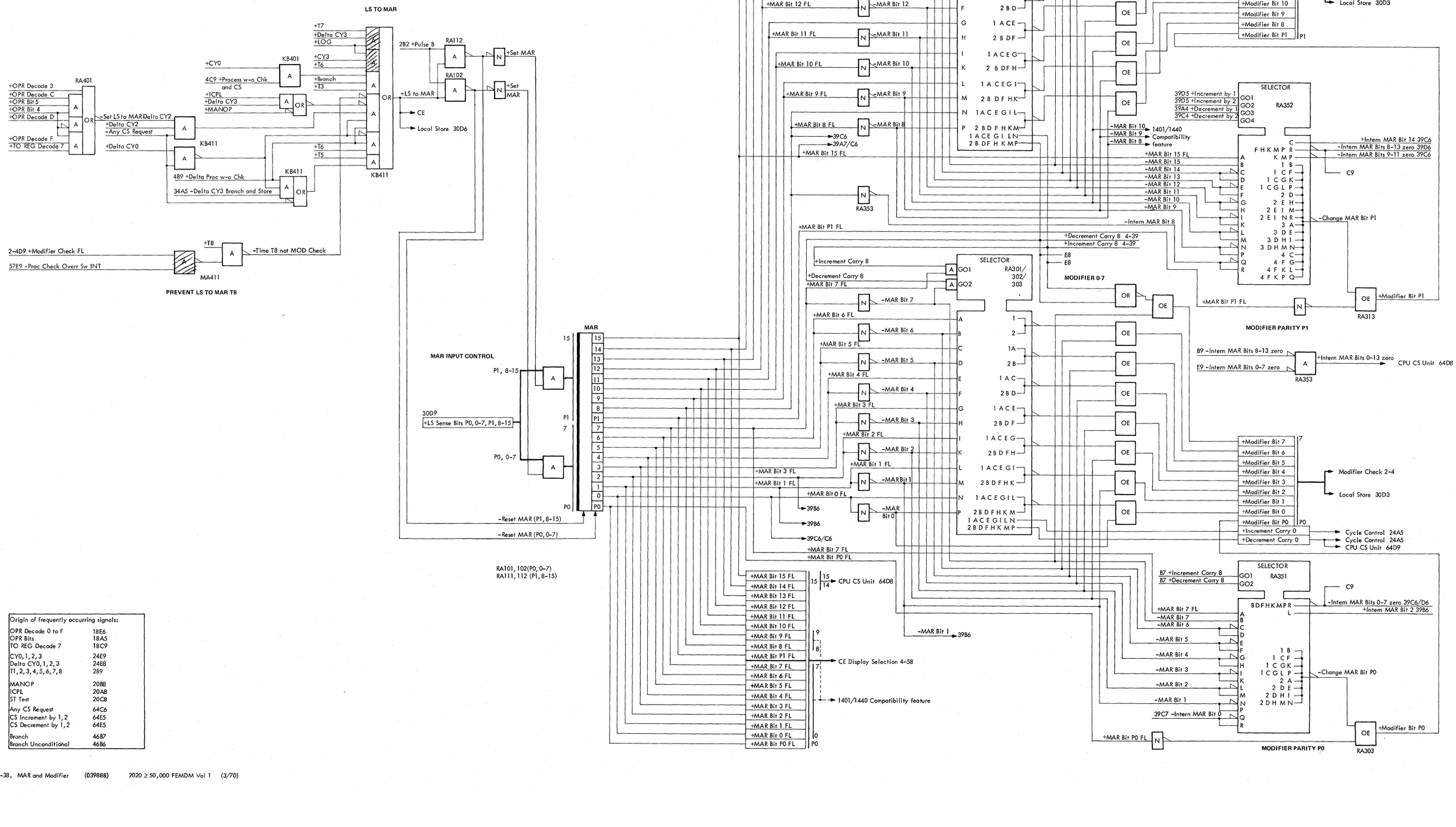
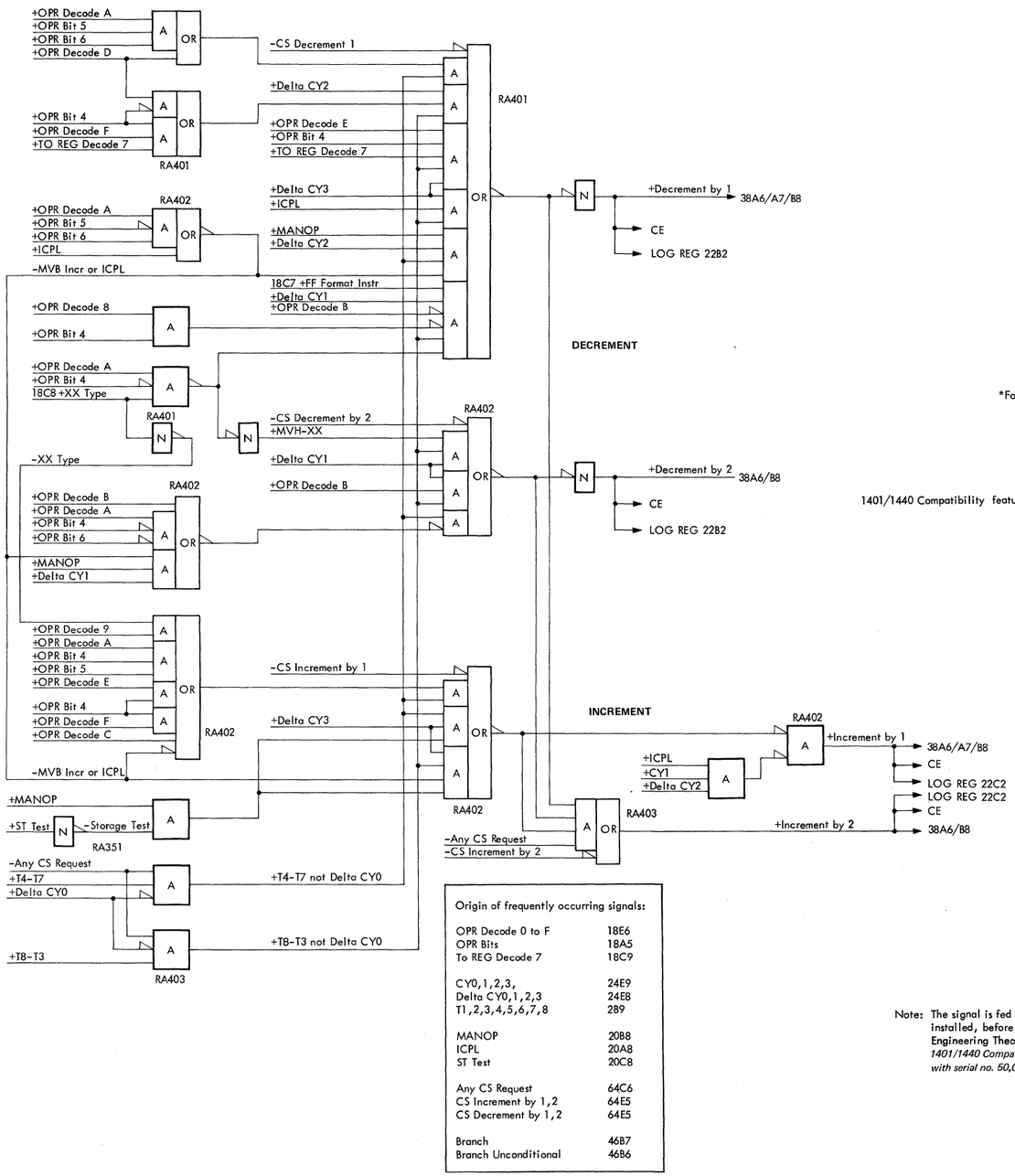


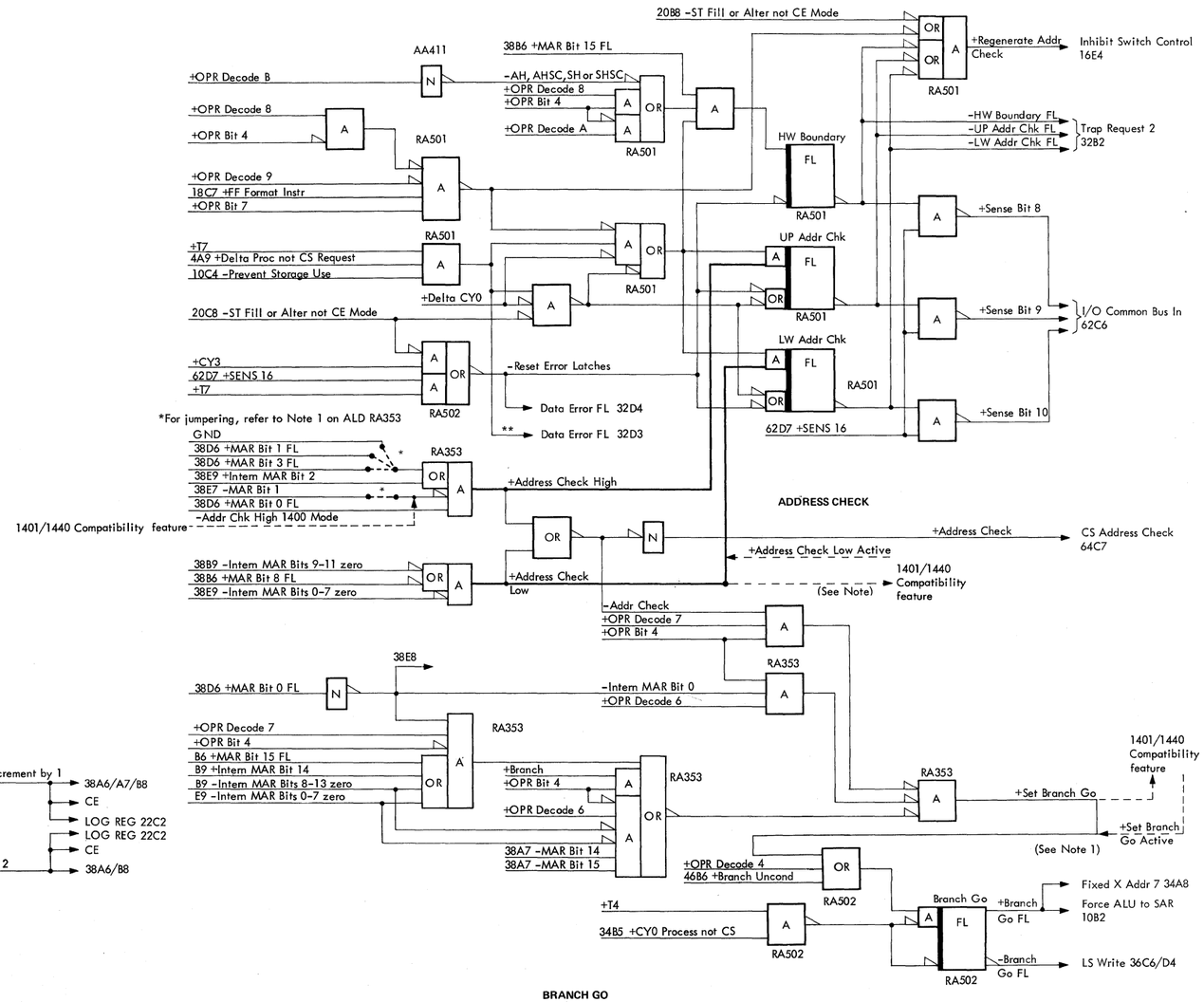
Diagram 4-36. LS Write (03987A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)



Origin of frequently occurring signals:	
OPR Decode 0 to F	18E6
OPR Bits	18A5
TO REG Decode 7	18C9
CY0, 1, 2, 3	24E9
Delta CY0, 1, 2, 3	24E8
T1, 2, 3, 4, 5, 6, 7, 8	28J
MANOP	20B8
ICPL	20A8
ST Test	20C8
Any CS Request	64C6
CS Increment by 1, 2	64E5
CS Decrement by 1, 2	64E5
Branch	46B7
Branch Unconditional	46B6



Origin of frequently occurring signals:	
OPR Decode 0 to F	18E6
OPR Bits	18A5
To REG Decode 7	18C9
CY0,1,2,3,	24E9
Delta CY0,1,2,3	24E8
T1,2,3,4,5,6,7,8	2B9
MANOP	20B8
ICPL	20A8
ST Test	20C8
Any CS Request	64C6
CS Increment by 1,2	64E5
CS Decrement by 1,2	64E5
Branch	46B7
Branch Unconditional	46B6



Note: The signal is fed through the 1401/1440 Compatibility feature, if installed, before entering the next logic block. Refer to Field Engineering Theory-Maintenance Diagrams manual (FETMDM), *1401/1440 Compatibility Feature, System/360 Model 20 (Machines with serial no. 50,000 and above), order No. SY33-1056.*

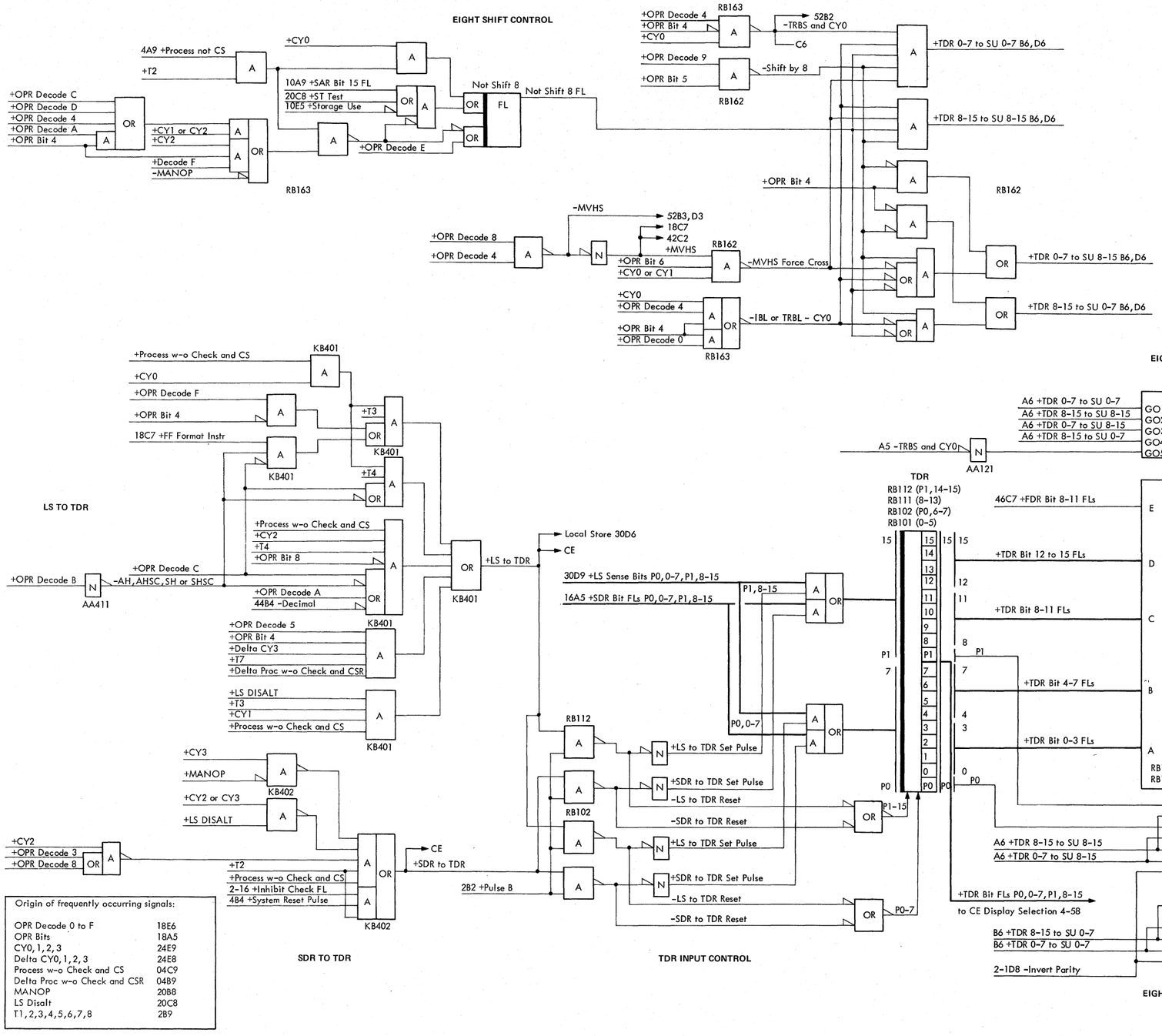
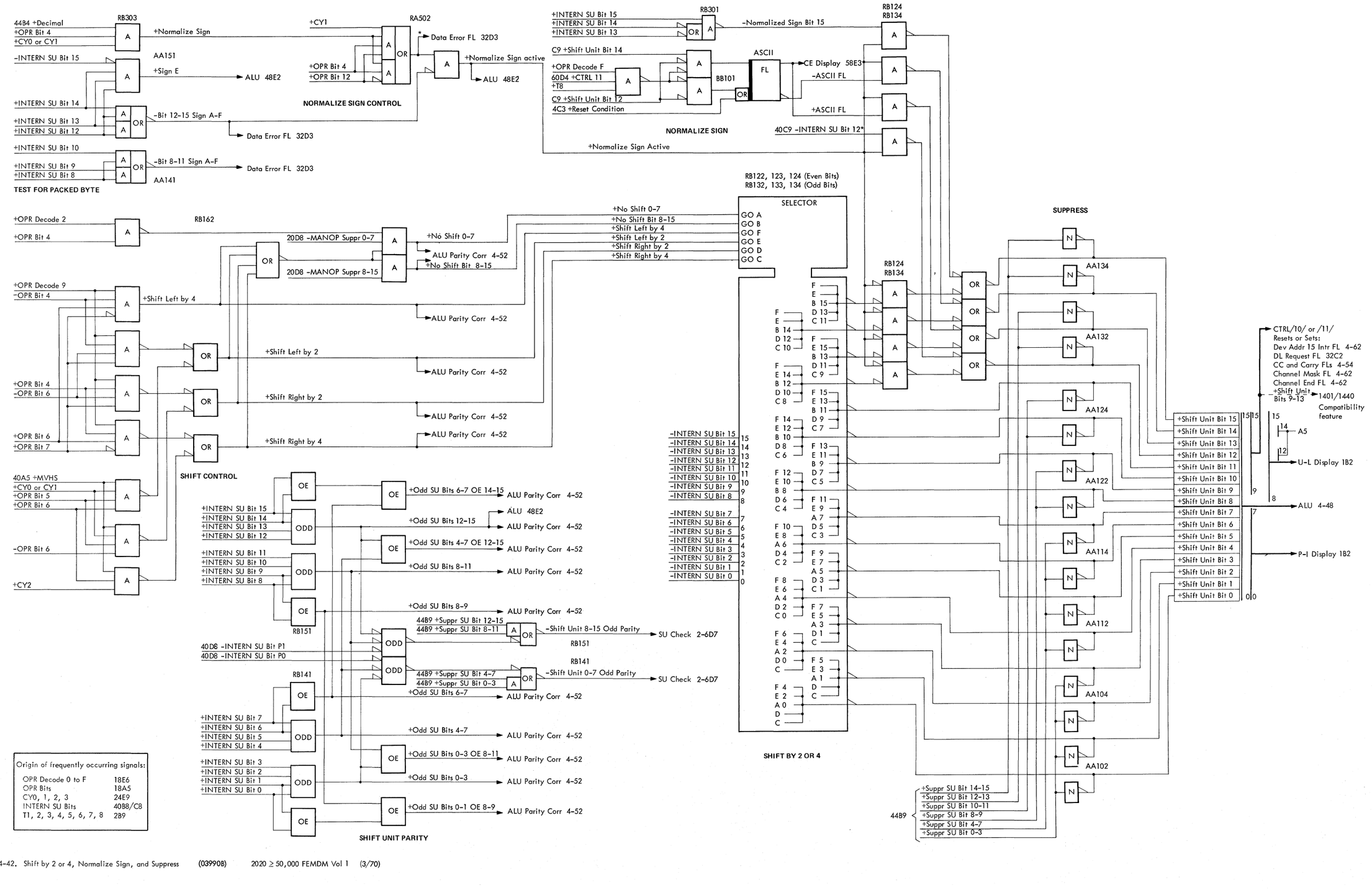
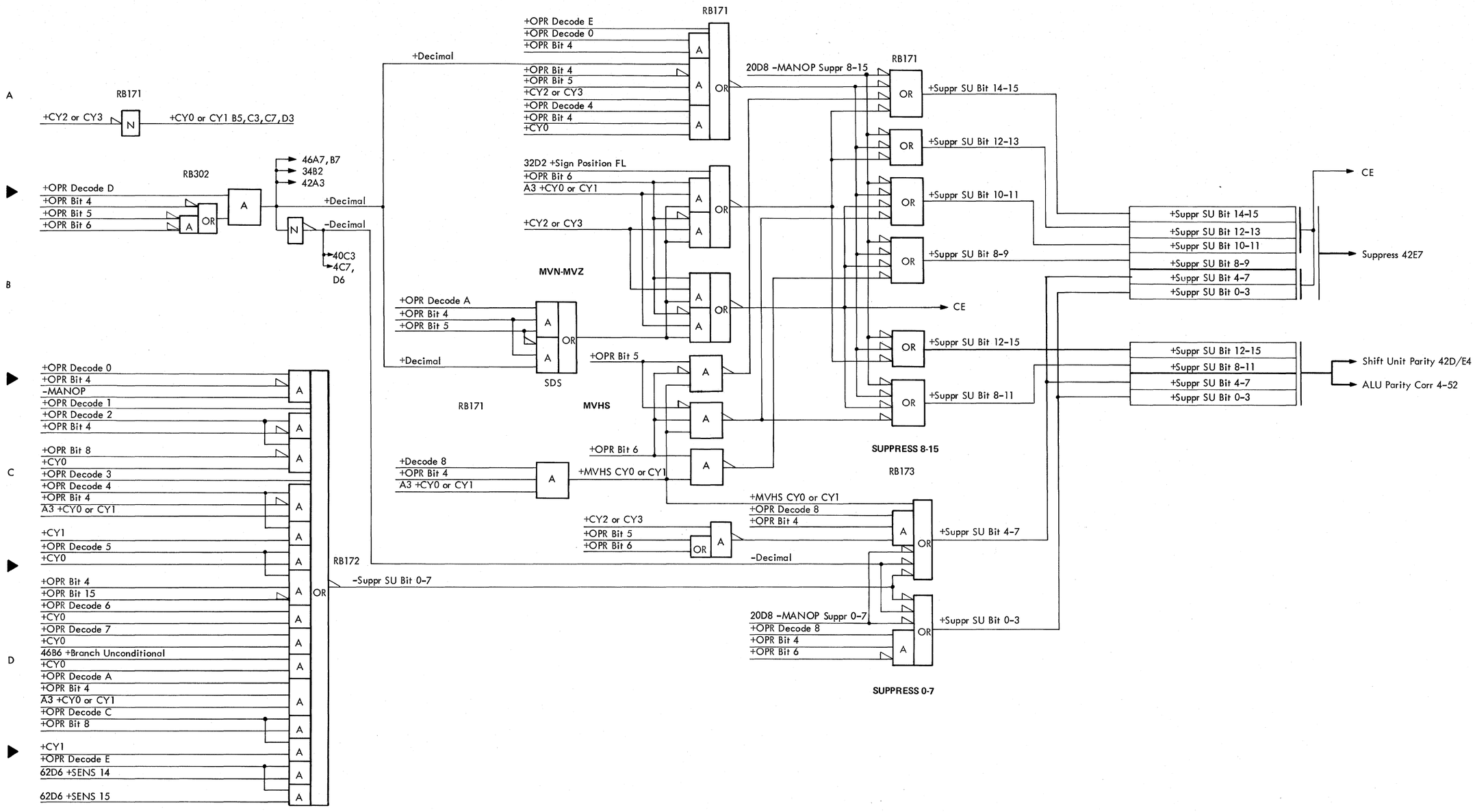


Diagram 4-40. TDR and Eight Shift (03989A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)



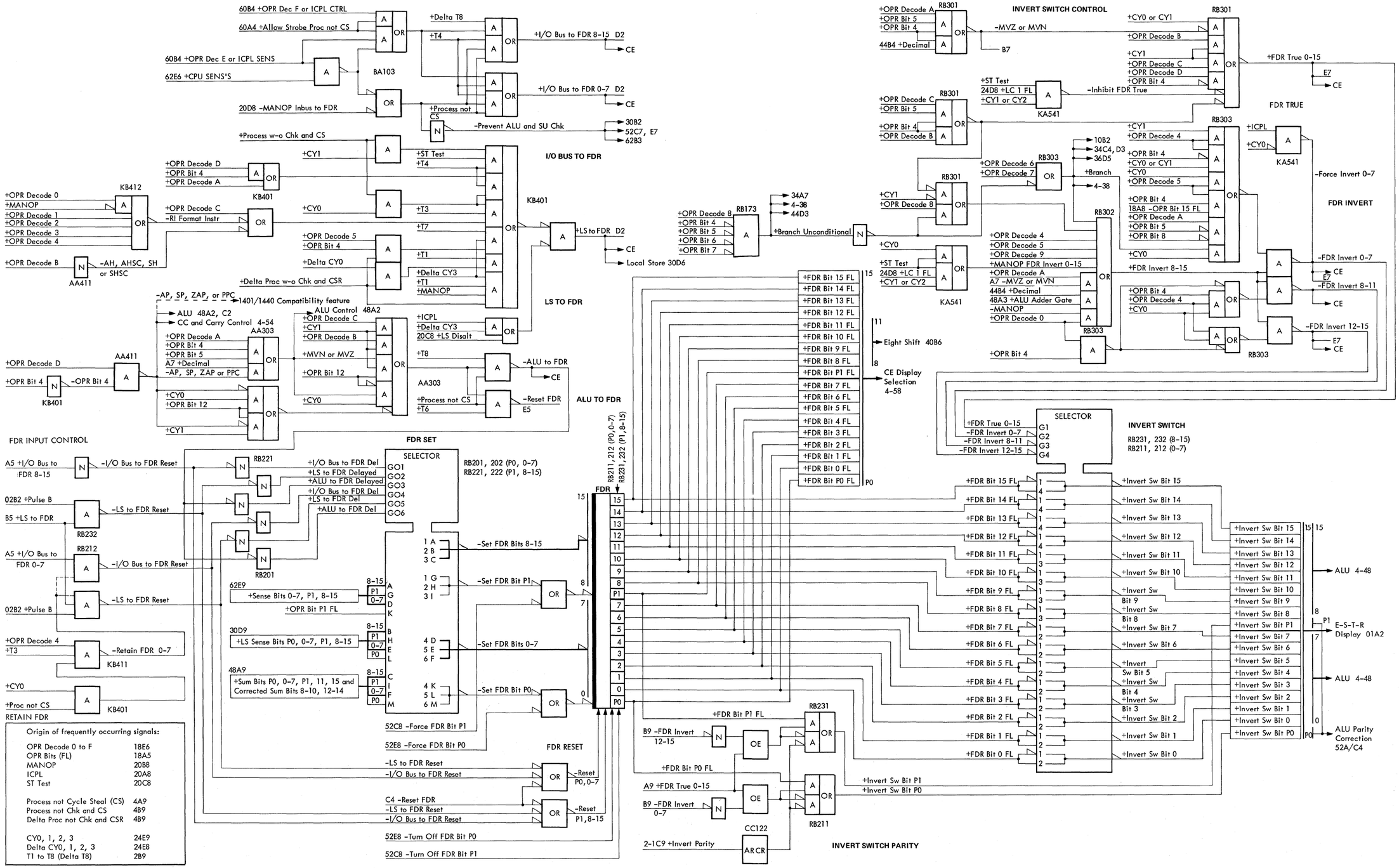
● Diagram 4-42. Shift by 2 or 4, Normalize Sign, and Suppress (03990B) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)



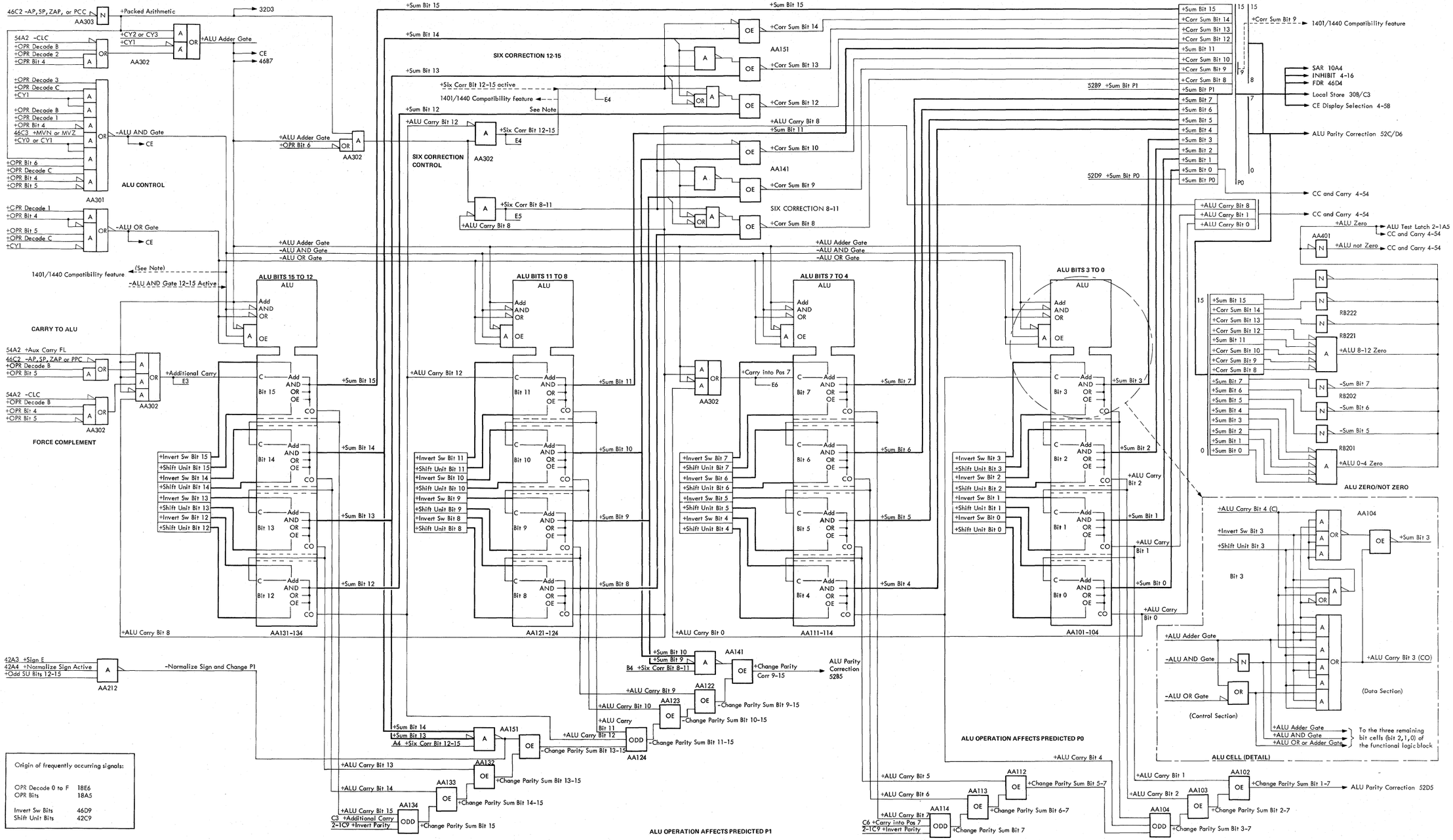
Origin of frequently occurring signals:

OPR Decode 0 to F	18E6
OPR Bits	18A5
CY0,1,2,3	24E9

Diagram 4-44. Suppress Control (03991A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)



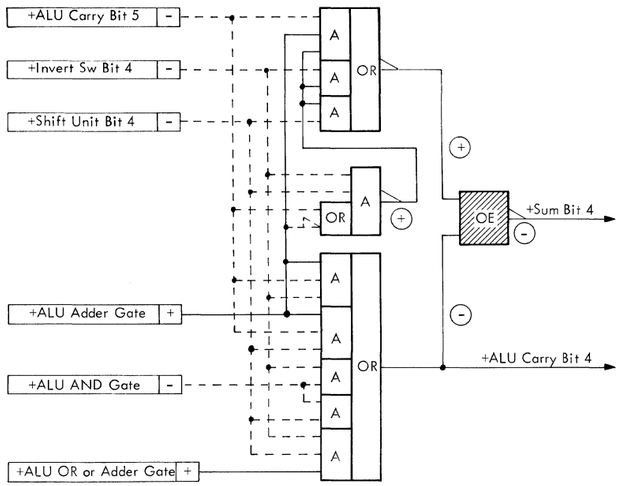
● Diagram 4-46. FDR and Invert Switch (03992B) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)



Note: The signal is fed through the 1401/1440 Compatibility feature, if installed, before entering the next logic block. Refer to Field Engineering Theory-Maintenance Diagrams manual (FETMDM), *1401/1440 Compatibility Feature, System/360 Model 20 (Machines with serial no. 50,000 and above), order No. SY33-1056.*

2 3 4 5 6 7 8 9

A

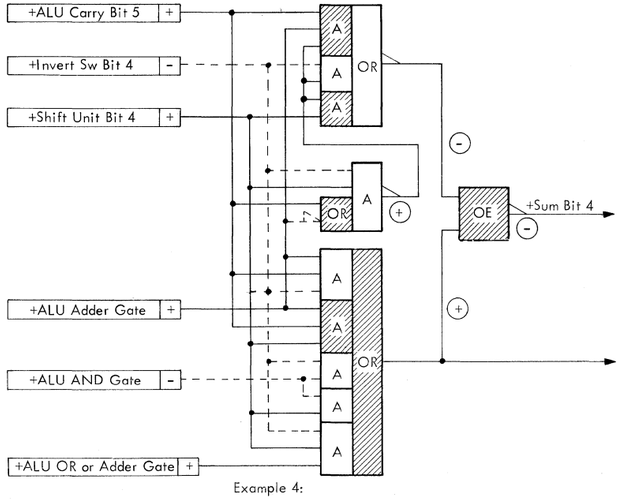


Example 1:

Add	Shift Unit Bit 4	=	0	(-)
	Invert Sw Bit 4	=	0	(-)
	ALU Carry Bit 5	=	0	(-)
Result	Sum Bit 4	=	0	(-)
	ALU Carry Bit 4	=	0	(-)

B

C

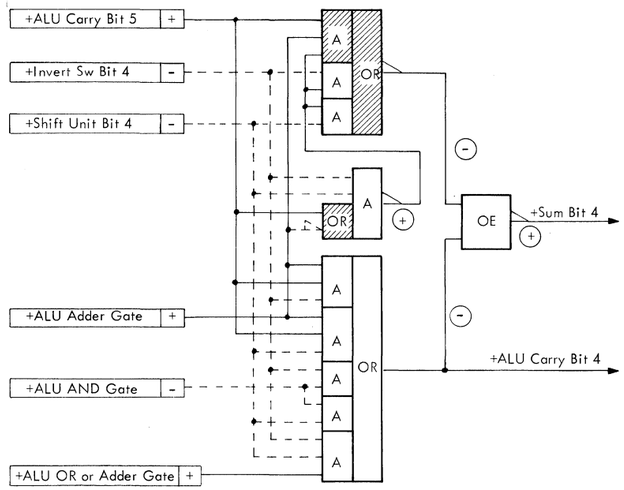


Example 4:

Add	Shift Unit Bit 4	=	1	(+)
	Invert Sw Bit 4	=	0	(-)
	ALU Carry Bit 5	=	1	(+)
Result	Sum Bit 4	=	0	(-)
	ALU Carry Bit 4	=	1	(+)

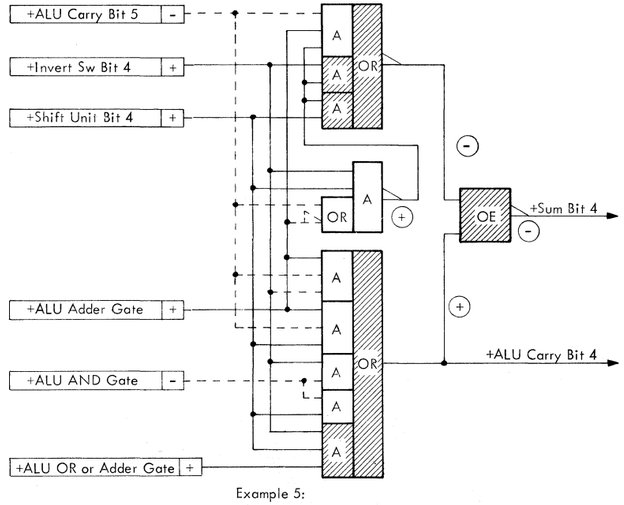
D

E



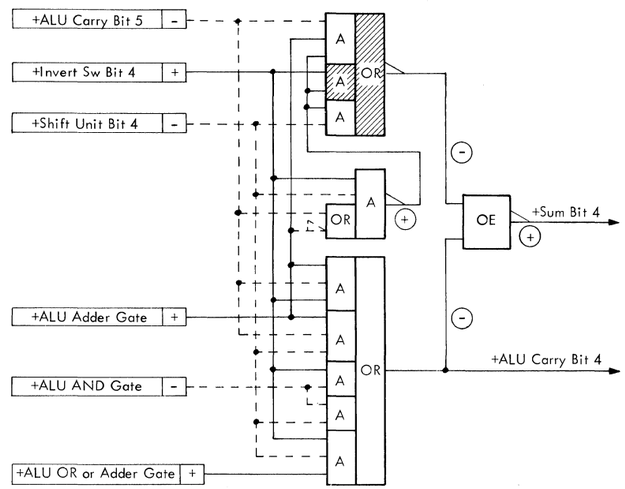
Example 2:

Add	Shift Unit Bit 4	=	0	(-)
	Invert Sw Bit 4	=	0	(-)
	ALU Carry Bit 5	=	1	(+)
Result	Sum Bit 4	=	1	(+)
	ALU Carry Bit 4	=	0	(-)



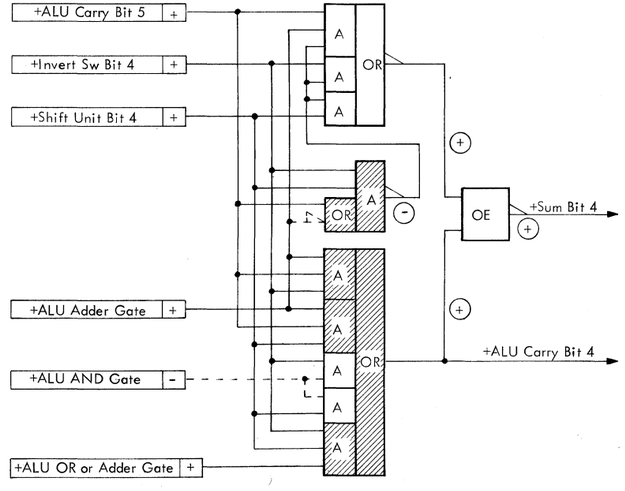
Example 5:

Add	Shift Unit Bit 4	=	1	(+)
	Invert Sw Bit 4	=	1	(+)
	ALU Carry Bit 5	=	0	(-)
Result	Sum Bit 4	=	0	(-)
	ALU Carry Bit 4	=	1	(+)



Example 3:

Add	Shift Unit Bit 4	=	0	(-)
	Invert Sw Bit 4	=	1	(+)
	ALU Carry Bit 5	=	0	(-)
Result	Sum Bit 4	=	1	(+)
	ALU Carry Bit 4	=	0	(-)

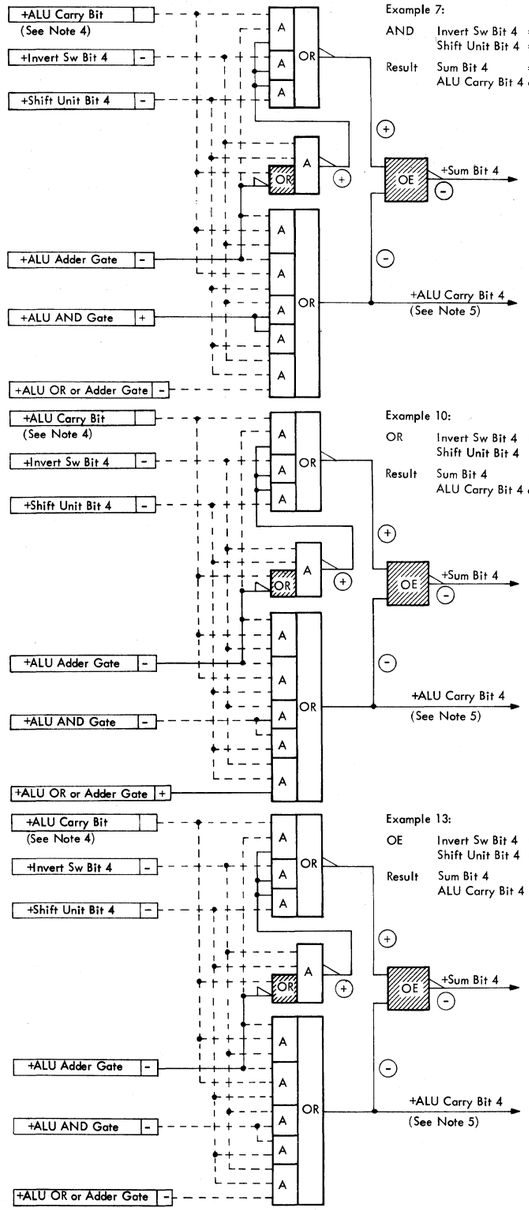


Example 6:

Add	Shift Unit Bit 4	=	1	(+)
	Invert Sw Bit 4	=	1	(+)
	ALU Carry Bit 5	=	1	(+)
Result	Sum Bit 4	=	1	(+)
	ALU Carry Bit 4	=	1	(+)

Notes:
1. Inactive input lines are dotted
2. Active AND/OR blocks are shaded
3. The encircled positive and negative signs (⊕ / ⊖) define the level at the corresponding output line
4. The ALU carry bit output provides the carry to the next high-order bit all, and is used to recognize when a parity change is required

Diagram 4-49. ALU Cell Operating Principles - Add (03994) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)



Example 7:

AND Invert Sw Bit 4 = 0 (-)
Shift Unit Bit 4 = 0 (-)

Result Sum Bit 4 = 0 (-)
ALU Carry Bit 4 output not active (-)

Example 10:

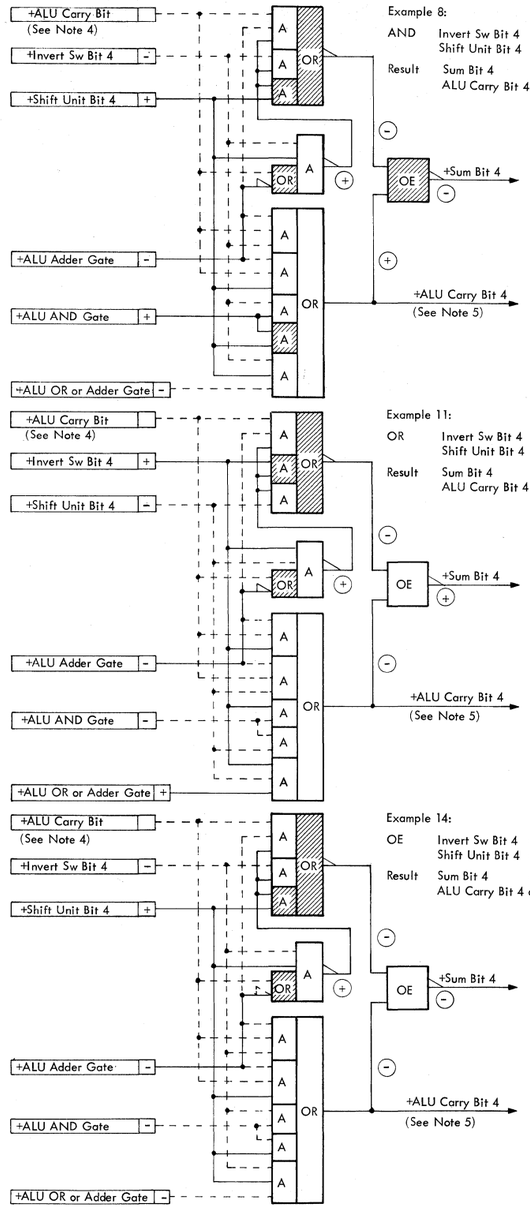
OR Invert Sw Bit 4 = 0 (-)
Shift Unit Bit 4 = 0 (-)

Result Sum Bit 4 = 0 (-)
ALU Carry Bit 4 output not active (-)

Example 13:

OE Invert Sw Bit 4 = 0 (-)
Shift Unit Bit 4 = 0 (-)

Result Sum Bit 4 = 0 (-)
ALU Carry Bit 4 output not active (-)



Example 8:

AND Invert Sw Bit 4 = 0 (-)
Shift Unit Bit 4 = 1 (+)

Result Sum Bit 4 = 1 (+)
ALU Carry Bit 4 output active (+)

Example 11:

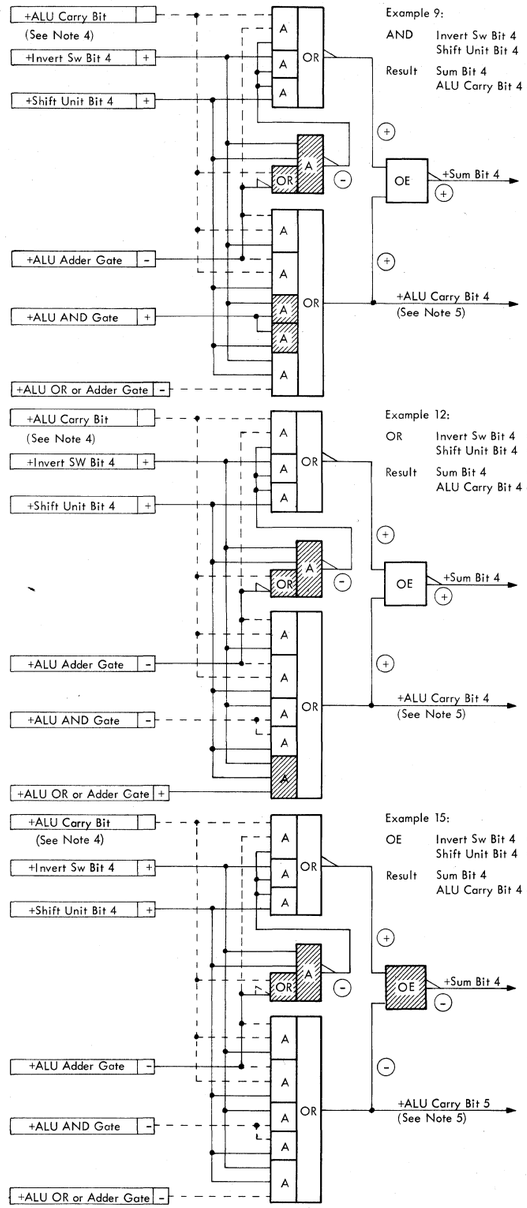
OR Invert Sw Bit 4 = 1 (+)
Shift Unit Bit 4 = 0 (-)

Result Sum Bit 4 = 1 (+)
ALU Carry Bit 4 output not active (-)

Example 14:

OE Invert Sw Bit 4 = 0 (-)
Shift Unit Bit 4 = 1 (+)

Result Sum Bit 4 = 1 (+)
ALU Carry Bit 4 output not active (-)



Example 9:

AND Invert Sw Bit 4 = 1 (+)
Shift Unit Bit 4 = 1 (+)

Result Sum Bit 4 = 1 (+)
ALU Carry Bit 4 output active (+)

Example 12:

OR Invert Sw Bit 4 = 1 (+)
Shift Unit Bit 4 = 1 (+)

Result Sum Bit 4 = 1 (+)
ALU Carry Bit 4 output active (+)

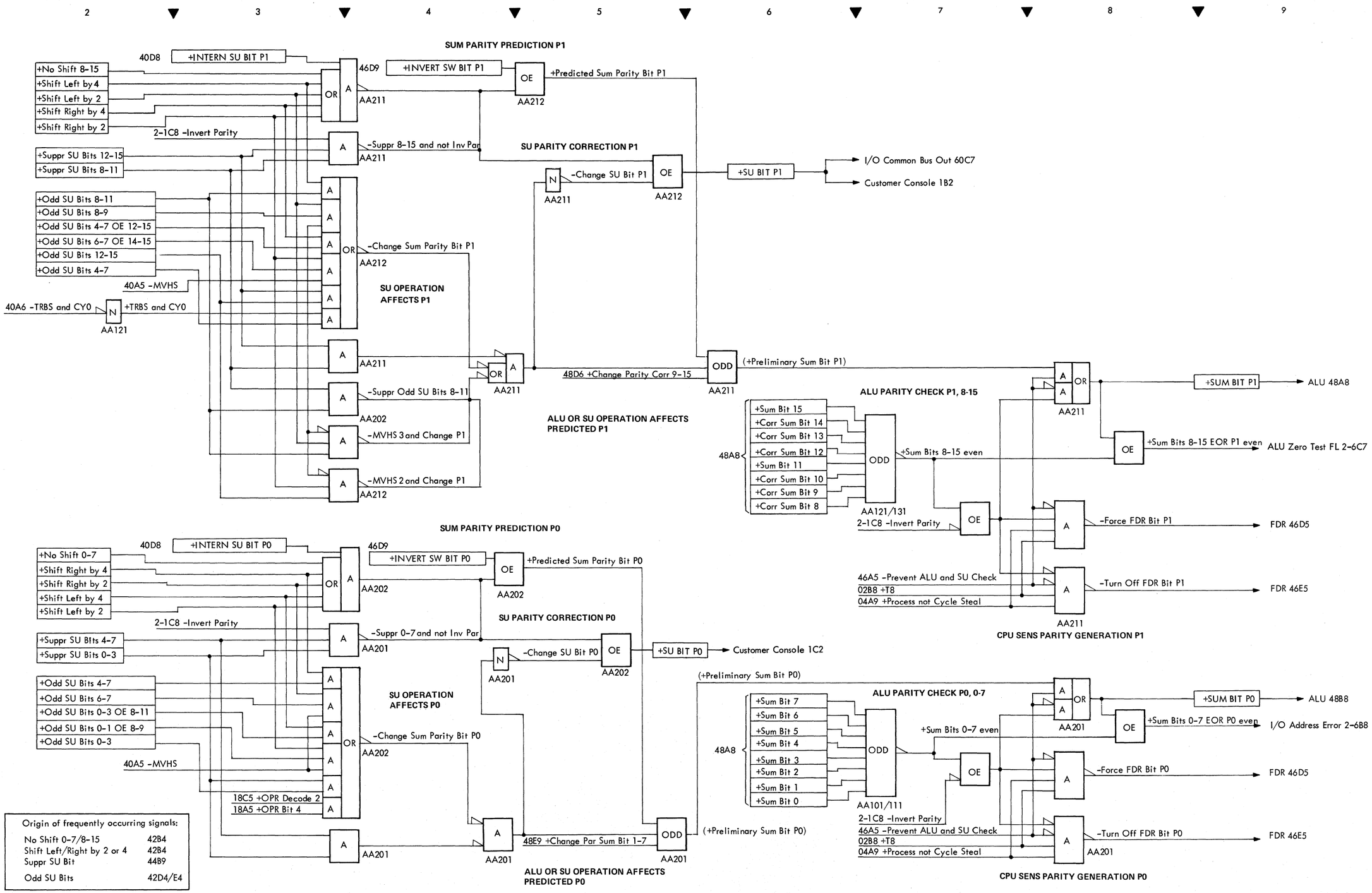
Example 15:

OE Invert Sw Bit 4 = 1 (+)
Shift Unit Bit 4 = 1 (+)

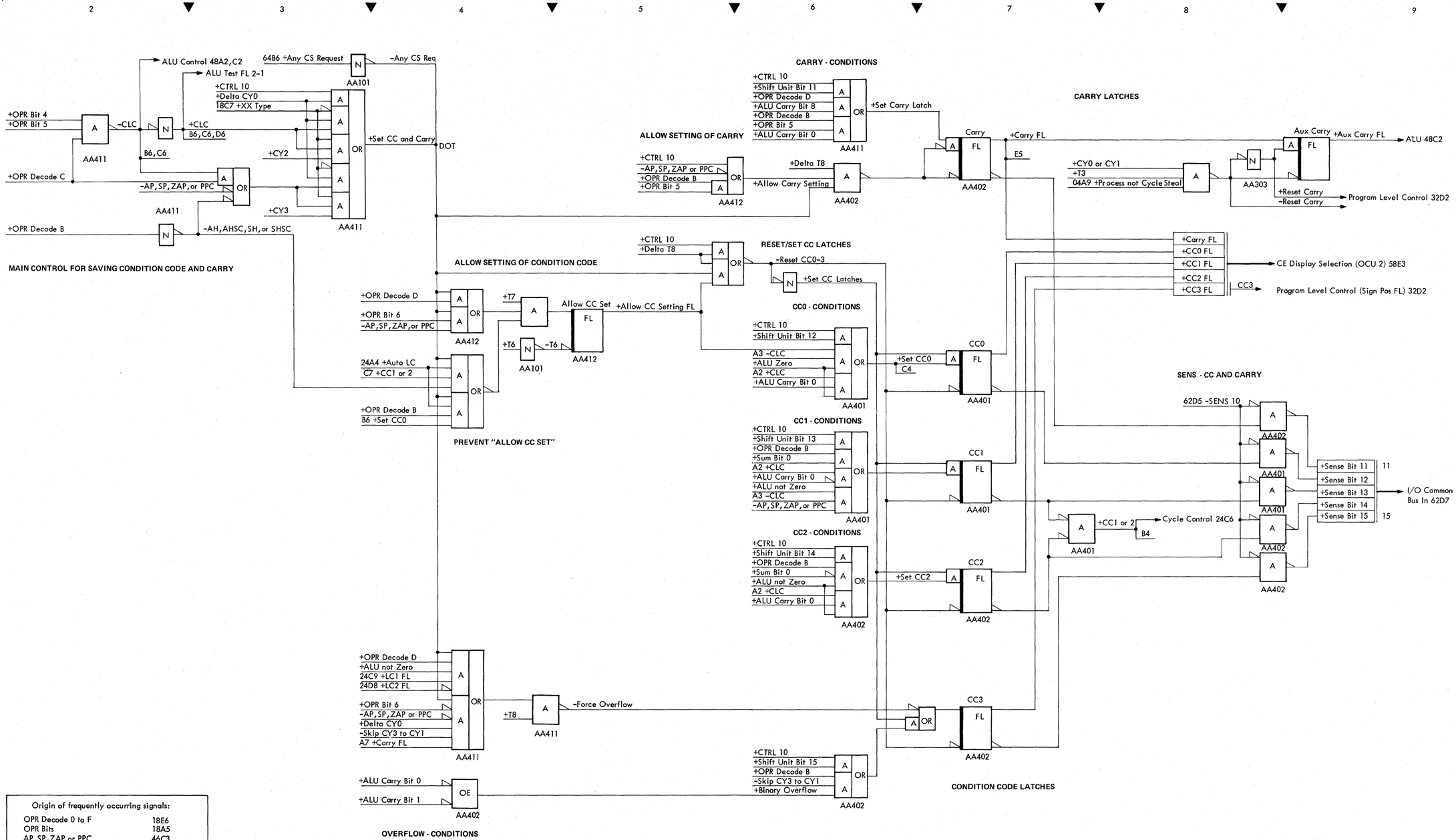
Result Sum Bit 4 = 0 (-)
ALU Carry Bit 4 output not active (-)

Notes:
1. Inactive inputs are dotted
2. Active AND/OR blocks are shaded
3. The encircled positive and negative signs (⊕/⊖) define the level at the corresponding output line
4. The ALU carry bit input is not used by the ALU circuits for the logical operations AND/OR/OE
5. The ALU carry bit output is used for parity correction only in the logical operations AND/OR/OE. The active ALU carry bit is not accepted by the next high-order bit call

Diagram 4-50. ALU Cell Operating Principles - AND/OR/OE (03995) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

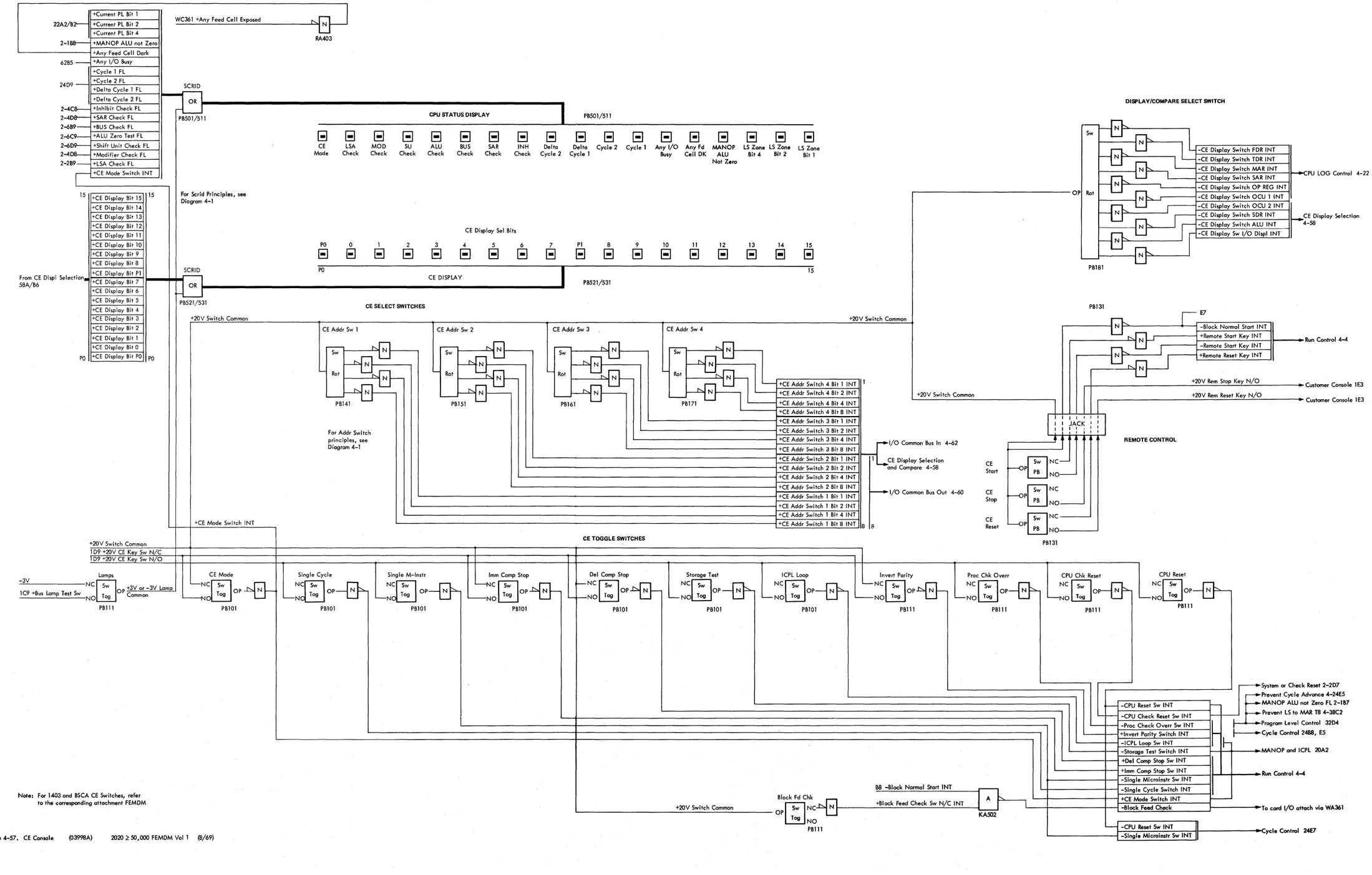


● Diagram 4-52. Shift Unit Parity Correction/ALU Parity Prediction and Correction (03996A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)



Origin of frequently occurring signals:	
OPR Decode 0 to F	18E6
OPR Bits	18A5
AP,SP,ZAP or PPC	46C3
CTRL 10	60C4
CY0,1,2,3	24E9
Delta CY0,1,2,3	24E8
T1,2,3,4,5,6,7,8,Delta T8	2B9
Skip CY3 to CY1	24A9
Shift Unit Bits	42C9
Sum Bit 0	48B8
ALU Carry Bit 0,1,8	48B9
ALU Zero/not Zero	48B9

● Diagram 4-54. Condition Code and Carry (03997A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)


+Current PL Bit 1
+Current PL Bit 2
+Current PL Bit 4
+MANOP ALU not Zero
+Any Feed Cell Dark
+Any I/O Busy
+Cycle 1 FL
+Cycle 2 FL
+Delta Cycle 1 FL
+Delta Cycle 2 FL
+Inhibit Check FL
+SAR Check FL
+BUS Check FL
+ALU Zero Test FL
+Shift Unit Check FL
+Modifier Check FL
+LSA Check FL
+CE Mode Switch INT
22A2/B2
2-1B8
6285
24D9
2-4C8
2-4D8
2-6B9
2-6C9
2-6D9
2-4D8
2-2B9
WC361 +Any Feed Cell Exposed
RA403
SCRID
OR
PB501/511
CPU STATUS DISPLAY
CE Mode
LSA Check
MOD Check
SU Check
ALU Check
BUS Check
SAR Check
INH Check
Delta Cycle 2
Delta Cycle 1
Cycle 2
Cycle 1
Any I/O Busy
Any Fd Cell DK
MANOP ALU Not Zero
LS Zone Bit 4
LS Zone Bit 2
LS Zone Bit 1
For Scrid Principles, see Diagram 4-1
+CE Display Bit 15
+CE Display Bit 14
+CE Display Bit 13
+CE Display Bit 12
+CE Display Bit 11
+CE Display Bit 10
+CE Display Bit 9
+CE Display Bit 8
+CE Display Bit P1
+CE Display Bit 7
+CE Display Bit 6
+CE Display Bit 5
+CE Display Bit 4
+CE Display Bit 3
+CE Display Bit 2
+CE Display Bit 1
+CE Display Bit 0
+CE Display Bit P0
From CE Displ Selection 58A/B6
CE Display Sel Bits
CE DISPLAY
PB521/531
CE SELECT SWITCHES
+20V Switch Common
CE Addr Sw 1
CE Addr Sw 2
CE Addr Sw 3
CE Addr Sw 4
PB141
PB151
PB161
PB171
+CE Addr Switch 4 Bit 1 INT
+CE Addr Switch 4 Bit 2 INT
+CE Addr Switch 4 Bit 4 INT
+CE Addr Switch 4 Bit 8 INT
+CE Addr Switch 3 Bit 1 INT
+CE Addr Switch 3 Bit 2 INT
+CE Addr Switch 3 Bit 4 INT
+CE Addr Switch 3 Bit 8 INT
+CE Addr Switch 2 Bit 1 INT
+CE Addr Switch 2 Bit 2 INT
+CE Addr Switch 2 Bit 4 INT
+CE Addr Switch 2 Bit 8 INT
+CE Addr Switch 1 Bit 1 INT
+CE Addr Switch 1 Bit 2 INT
+CE Addr Switch 1 Bit 4 INT
+CE Addr Switch 1 Bit 8 INT
For Addr Switch principles, see Diagram 4-1
I/O Common Bus In 4-62
CE Display Selection and Compare 4-58
I/O Common Bus Out 4-60
DISPLAY/COMPARE SELECT SWITCH
PB181
-CE Display Switch FDR INT
-CE Display Switch TDR INT
-CE Display Switch MAR INT
-CE Display Switch SAR INT
-CE Display Switch OP REG INT
-CE Display Switch OCU 1 INT
-CE Display Switch OCU 2 INT
-CE Display Switch SDR INT
-CE Display Switch ALU INT
-CE Display Sw I/O Displ INT
CPU LOG Control 4-22
CE Display Selection 4-58
PB131
E7
-Block Normal Start INT
+Remote Start Key INT
-Remote Start Key INT
+Remote Reset Key INT
Run Control 4-4
+20V Rem Stop Key N/O
+20V Rem Reset Key N/O
Customer Console 1E3
JACK
REMOTE CONTROL
CE Start
CE Stop
CE Reset
+CE Mode Switch INT
CE TOGGLE SWITCHES
+20V Switch Common
1D9 +20V CE Key Sw N/C
1D9 +20V CE Key Sw N/O
-3V
1C9 +Bus Lamp Test Sw
+3V or -3V Lamp Common
Lamps
CE Mode
Single Cycle
Single M-Instr
Imm Comp Stop
Del Comp Stop
Storage Test
ICPL Loop
Invert Parity
Proc Chk Overr
CPU Chk Reset
CPU Reset
PB111
PB101
-CPU Reset Sw INT
-CPU Check Reset Sw INT
-Proc Check Overr Sw INT
+Invert Parity Switch INT
-ICPL Loop Sw INT
-Storage Test Switch INT
+Del Comp Stop Sw INT
+Imm Comp Stop Sw INT
-Single Microinstr Sw INT
-Single Cycle Switch INT
+CE Mode Switch INT
-Block Feed Check
System or Check Reset 2-2D7
Prevent Cycle Advance 4-24E5
MANOP ALU not Zero FL 2-1B7
Prevent LS to MAR T8 4-38C2
Program Level Control 32D4
Cycle Control 24B8, E5
MANOP and ICPL 20A2
Run Control 4-4
To card I/O attach via WA361
Cycle Control 24E7
Block Fd Chk
B8 -Block Normal Start INT
+Block Feed Check Sw N/C INT
KA502
Note: For 1403 and BSCA CE Switches, refer to the corresponding attachment FEMDM

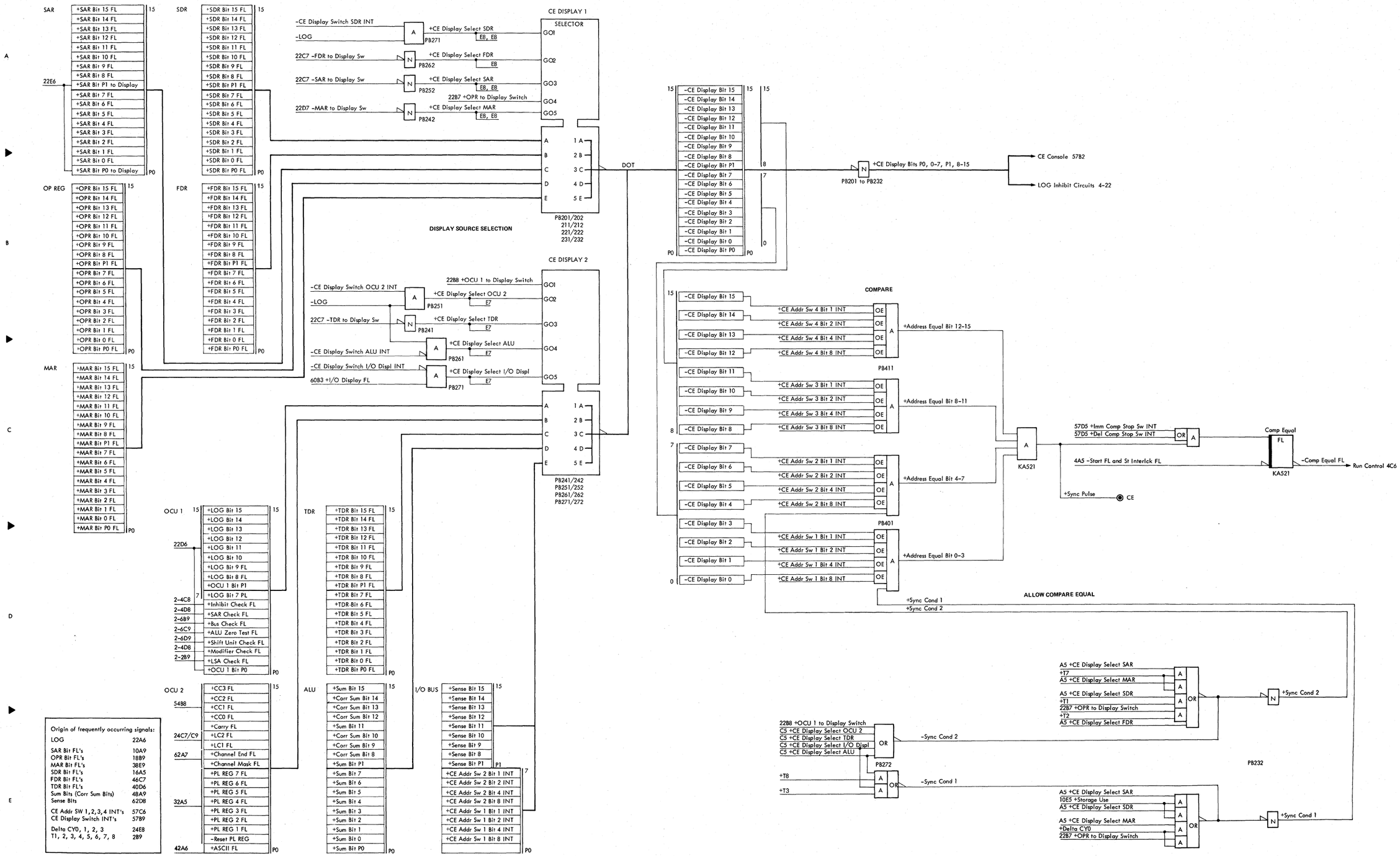


Diagram 4-58. CE Display Selection and Compare (03999A) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)

2 3 4 5 6 7 8 9

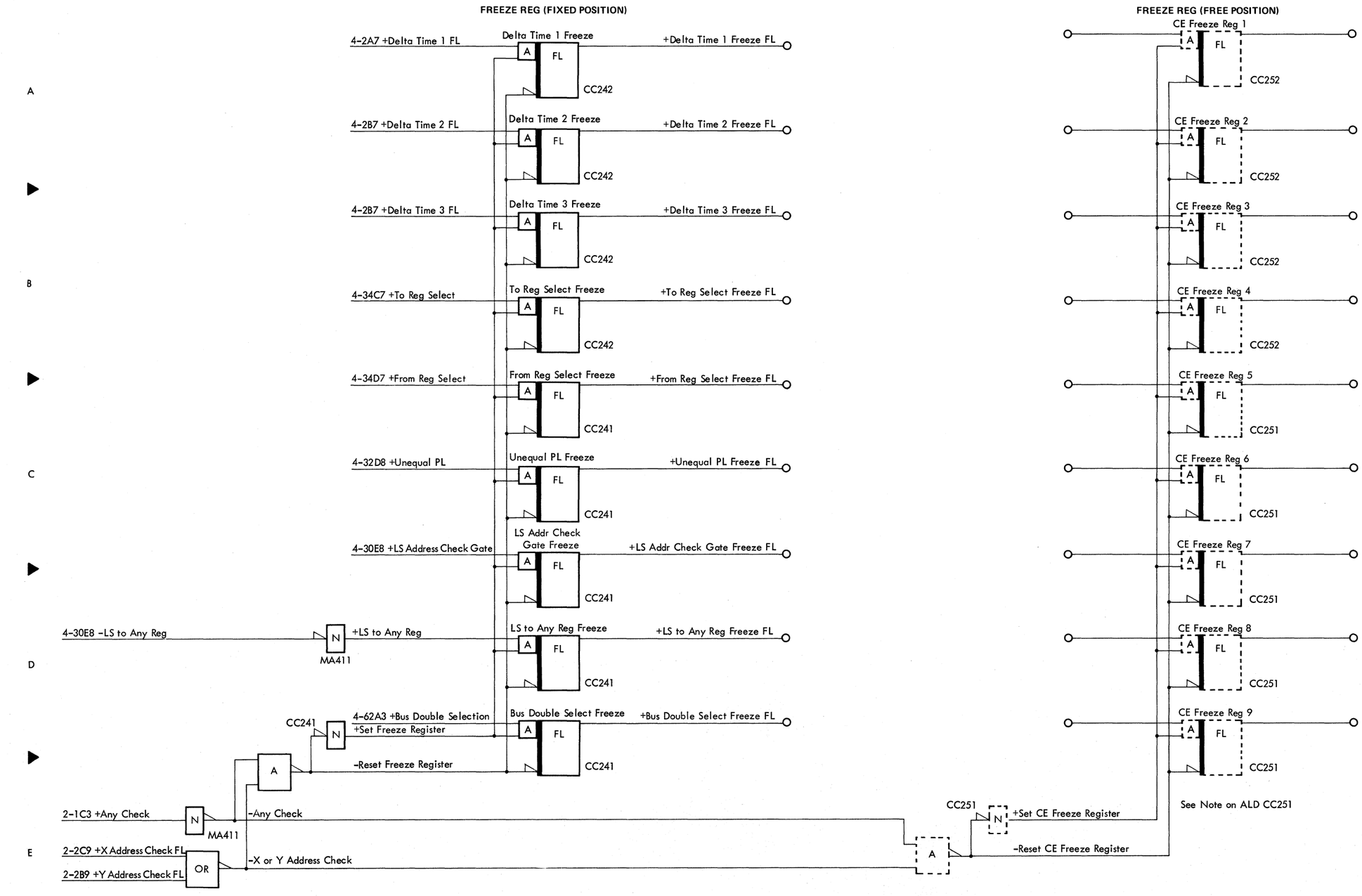
A

B

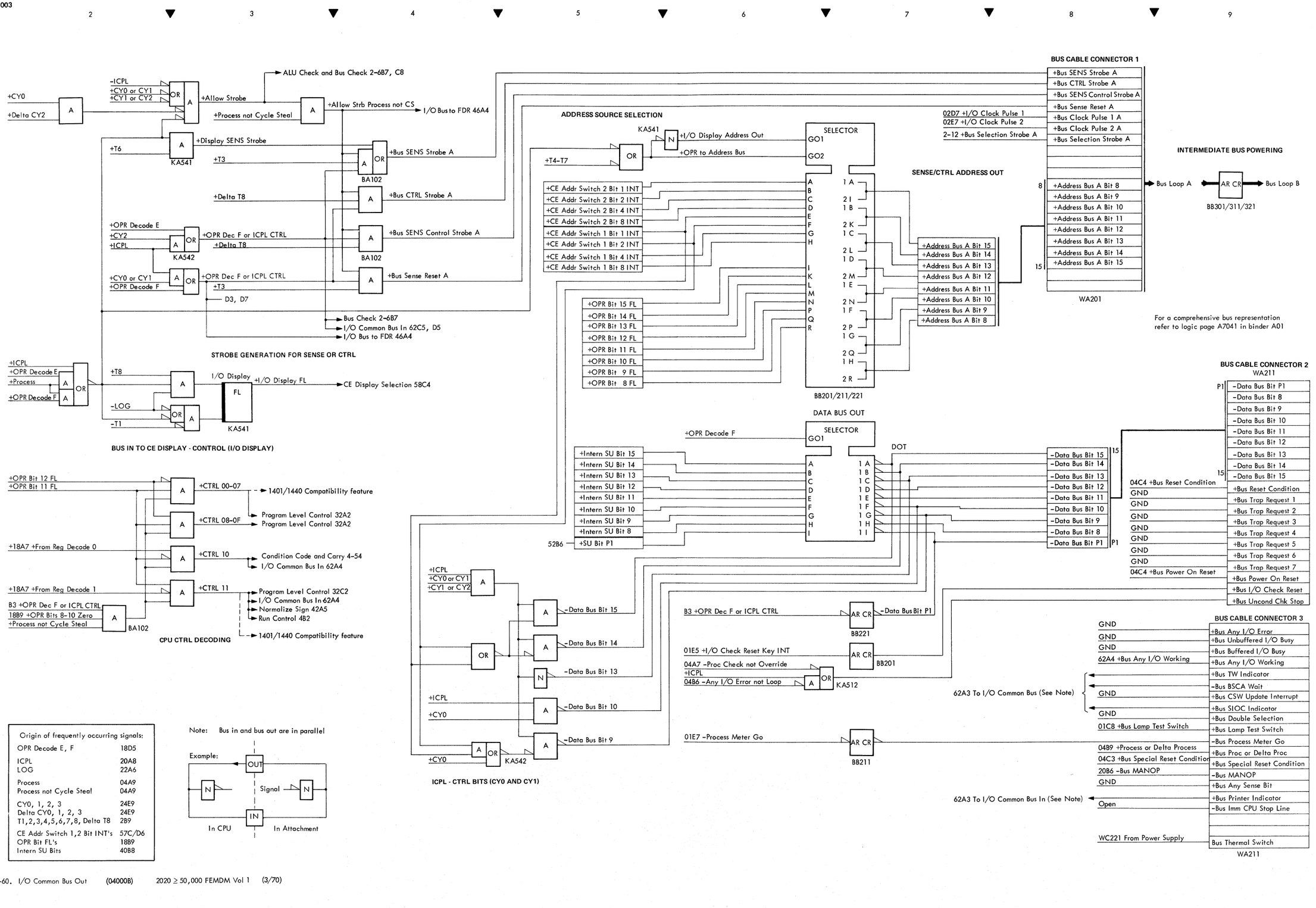
C

D

E



● Diagram 4-59. CE Freeze Register (04338) 2020 ≥ 50,000 FEMDM Vol 1 (8/69)



● Diagram 4-60. I/O Common Bus Out (04000B) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)

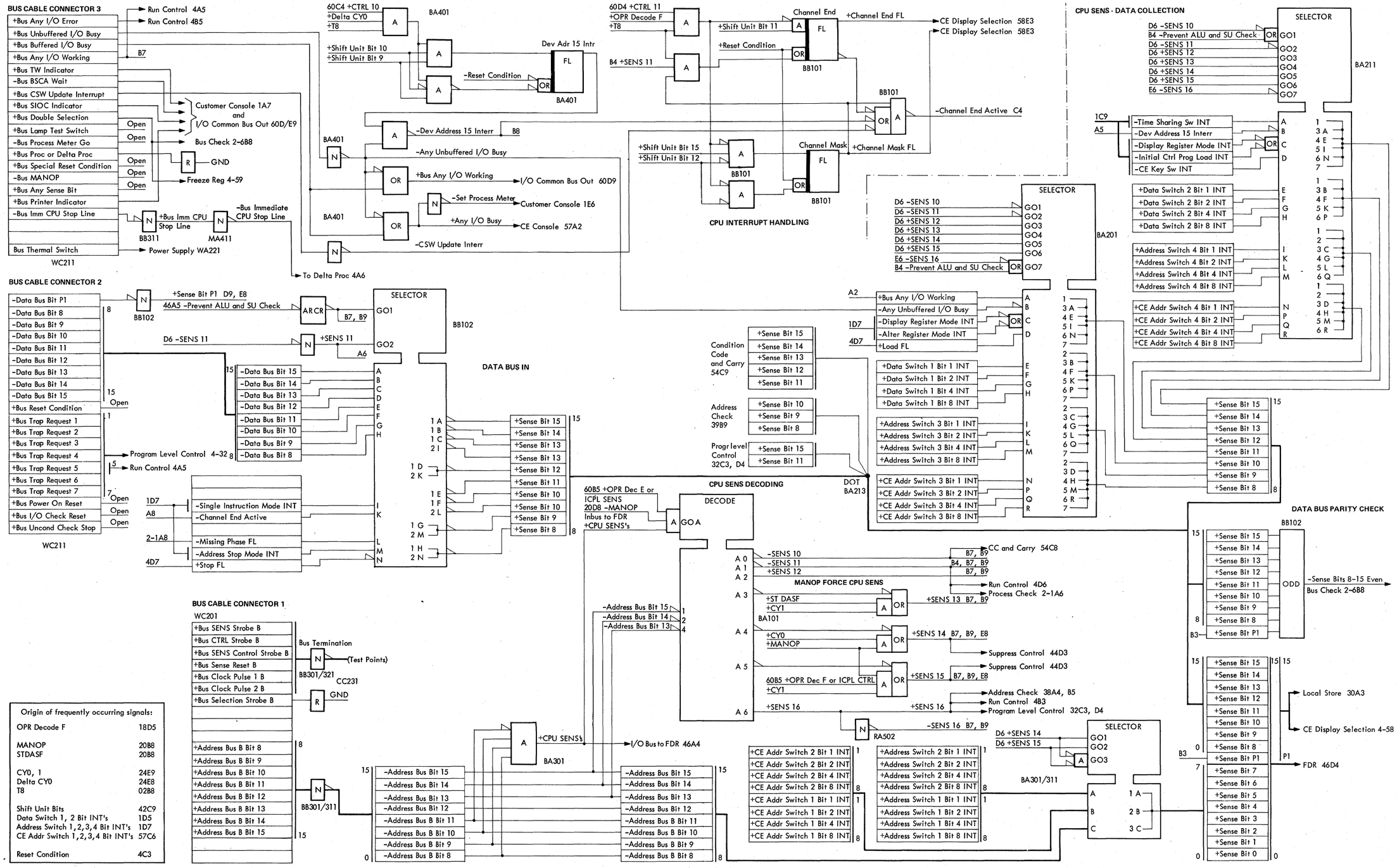
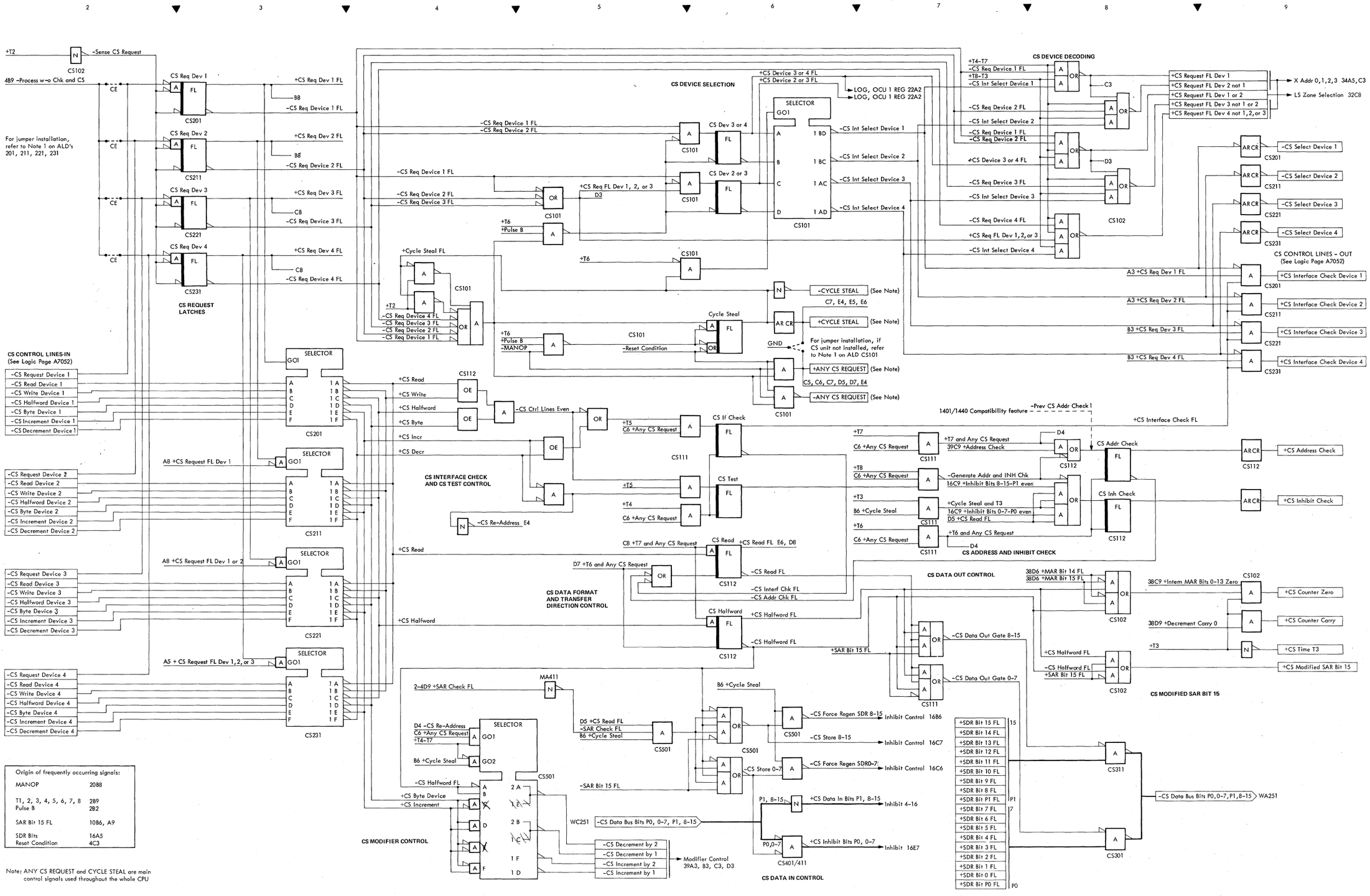


Diagram 4-62. I/O Common Bus In (04001A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)



● Diagram 4-64. CPU Cycle Steal Control Unit (04002A) 2020 ≥ 50,000 FEMDM Vol 1 (3/70)

	2		3		4		5		6		7		8		9	
	+Additional Carry	4-48 C2	−Address Bus Bit 11	4-62 E4	ALU to SAR FL	2-06 D7	+Bus CTRL Strobe B	4-62 D3	+CE Addr Switch 2 Bit 2 INT	4-57 C6
	+Addr Check High	4-39 C7	−Address Bus Bit 12	4-62 E4	+ALU Zero	4-48 B9	+Bus Double Select Freeze FL	4-59 D5	+CE Addr Switch 2 Bit 4 INT	4-57 C6
	+Addr Check Low	4-39 C7	−Address Bus Bit 13	4-62 E4	+ALU Zero Test FL	2-06 C9	+Bus Double Selection	2-06 A9	+CE Addr Switch 2 Bit 8 INT	4-57 C6
	+Addr Reg Bit AUX	4-10 C9	−Address Bus Bit 14	4-62 E4	−ALU Zero Test FL	2-06 C9		4-62 B2	+CE Addr Switch 3 Bit 1 INT	4-57 C6
	−Addr Reg Bit AUX	4-10 C9	−Address Bus Bit 15	4-62 E4	+ALU 0-4 Zero	4-48 C9		4-60 D9	+CE Addr Switch 3 Bit 2 INT	4-57 C6
	+Addr Reg Bit 1	4-10 C9	+Address Check	4-39 C9	−ALU 0-7 to INH 0-7	4-16 D6	+Bus I/O Check Reset	4-60 D9	+CE Addr Switch 3 Bit 4 INT	4-57 C6
A	−Addr Reg Bit 1	4-10 C9	+Address Equal Bit 0-3	4-58 D7	+ALU 8-12 Zero	4-48 C9	+Bus I/O Working	4-62 B4	+CE Addr Switch 3 Bit 8 INT	4-57 C6
	−Addr Reg Bit 2	4-10 C9	+Address Equal Bit 4-7	4-58 C7	−ALU 8-15 to INH 0-7	4-16 C6	−Bus Immediate CPU Stop Line	4-60 E9	+CE Addr Switch 4 Bit 1 INT	4-57 C6
	+Addr Reg Bit 2	4-10 C9	+Address Equal Bit 8-11	4-58 C7	−ALU 8-15 to INH 8-15	4-16 B6		4-62 B2	+CE Addr Switch 4 Bit 2 INT	4-57 C6
	−Addr Reg Bit 3	4-10 C9	+Address Equal Bit 12-15	4-58 C7	+Any Check	2-01 C3	+Bus Lamp Test Sw	4-01 C8	+CE Addr Switch 4 Bit 4 INT	4-57 C6
	−Addr Reg Bit 4	4-10 C9	Address Reg	4-10 C9	+Any CS Request	4-64 B6	+Bus Lamp Test Switch	4-62 B2	+CE Addr Switch 4 Bit 8 INT	4-57 C6
	−Addr Reg Bit 5	4-10 C9	Address Source Selection	4-34 D7	−Any CS Request	4-64 C6		4-60 E9	CE Display	4-57 B4
▶	−Addr Reg Bit 6	4-10 C9	−Address Stop Mode INT	4-01 C8	+Any Feed Cell Dark	4-57 A2	−Bus MANOP	4-20 B7	+CE Display Select ALU	4-58 C4
	−Addr Reg Bit 7	4-10 C9	−AH, AHSC, SH, or SHSC	4-39 A7	+Any Feed Cell Exposed*	4-57 A3		4-60 E9	+CE Display Select FDR	4-58 A4
	−Addr Reg Bit 8	4-10 C9		4-40 C2	+Any I/O Busy	4-62 B4		4-62 B2	+CE Display Select I/O Displ	4-58 C4
	−Addr Reg Bit 9	4-10 C9		4-46 B2	−Any I/O Error Not Loop	4-04 B6	+Bus Printer Indicator	4-60 E9	+CE Display Select MAR	4-58 A4
	−Addr Reg Bit 10	4-10 C9		4-54 A3	−Any Unbuffered I/O Busy	4-62 A4		4-62 B2	+CE Display Select OCU2	4-58 B4
	−Addr Reg Bit 11	4-10 C9	−All Checks	2-01 A3	−AP, SP, ZAP, or PPC	4-46 C3	−Bus Process Meter Go	4-60 E9	+CE Display Select SAR	4-58 A4
	−Addr Reg Bit 12	4-10 C9	+Allow Carry Setting	4-54 A6	−ASCII FL	4-42 A6		4-62 B2	+CE Display Select SDR	4-58 A4
B	−Addr Reg Bit 13	4-10 D9	+Allow CC Setting FL	4-54 B5	+ASCII FL	4-42 A6	+Bus Process or Delta Process	4-60 E9	+CE Display Select TDR	4-58 B4
	−Addr Reg Bit 14	4-10 D9	Allow Check FL	2-06 D7	+Auto LC	4-24 A4		4-62 B2	−CE Display Bit 0	4-58 B5
	−Addr Reg Bit 15	4-10 D9	+Allow Cont Alter or Display	4-04 B6		4-36 A4	+Bus Reset Condition	4-04 C4	−CE Display Bit 1	4-58 B5
	+Addr Sw 1 Bit 1 INT	4-01 D4	+Allow ICPL	4-20 A3	+Aux Carry FL	4-54 A9	+Bus Selection Strobe	2-06 B8	−CE Display Bit 2	4-58 B5
	+Addr Sw 1 Bit 2 INT	4-01 D4	+Allow INH Check 0-7	2-04 D5	Aux LC1 FL	4-24 C8	+Bus Selection Strobe A	4-60 B8	−CE Display Bit 3	4-58 B5
	+Addr Sw 1 Bit 4 INT	4-01 D4		4-16 A8			+Bus Selection Strobe B	4-62 D3	−CE Display Bit 4	4-58 B5
▶	+Addr Sw 1 Bit 8 INT	4-01 D4	+Allow INH Check 8-15	2-04 D5			+Bus SENS Control Strobe A	4-60 A8	−CE Display Bit 5	4-58 B5
	+Addr Sw 2 Bit 1 INT	4-01 D5		4-16 A8	+Binary or Logical not CLC	4-34 D4	+Bus SENS Control Strobe B	4-62 D3	−CE Display Bit 6	4-58 B5
	+Addr Sw 2 Bit 2 INT	4-01 D5	+Allow OPR Set	4-18 C3	+Binary Overflow	4-54 E6	+Bus SENS CTRL Strobe A	4-60 B4	−CE Display Bit 7	4-58 B5
	+Addr Sw 2 Bit 4 INT	4-01 D5	+Allow PL Switching	4-32 A3	+Bit Timing 1	4-30 A5	+Bus SENS Strobe A	4-60 A4	−CE Display Bit 8	4-58 B5
	+Addr Sw 2 Bit 8 INT	4-01 D5	+Allow Strb Process not CS	4-60 A4	+Bit Timing 2	4-30 A5		4-60 A8	−CE Display Bit 9	4-58 A5
	+Addr Sw 3 Bit 1 INT	4-01 D6	+Allow Strobe	4-60 A3	−Bit 12-15 Sign A-F	4-42 A2	+Bus SENS Strobe B	4-62 D3	−CE Display Bit 10	4-58 A5
C	+Addr Sw 3 Bit 2 INT	4-01 D6	−Alter Register Mode INT	4-01 C8	−Bit 8-11 Sign A-F	4-42 A2	+Bus Sense Reset A	4-60 A8	−CE Display Bit 11	4-58 A5
	+Addr Sw 3 Bit 4 INT	4-01 D6	+ALU Adder Gate	4-48 A3	+Block Feed Check Sw N/C INT	4-57 E8		4-60 B4	−CE Display Bit 12	4-58 A5
	+Addr Sw 3 Bit 8 INT	4-01 D6	ALU Bits 3 to 0	4-48 B7	−Block Normal Start INT	4-57 C9	+Bus Sense Reset B	4-62 D3	−CE Display Bit 13	4-58 A5
	+Addr Sw 4 Bit 1 INT	4-01 D7	ALU Bits 7 to 4	4-48 B6	+Branch	4-46 B8	+Bus SIOC Indicator	4-01 A8	−CE Display Bit 14	4-58 A5
	+Addr Sw 4 Bit 2 INT	4-01 D7	ALU Bits 11 to 8	4-48 B4		4-24 B3		4-62 B2	−CE Display Bit 15	4-58 A5
	+Addr Sw 4 Bit 4 INT	4-01 D7	ALU Bits 15 to 12	4-48 B3	+Branch and Store	4-34 B5	+Bus Special Reset Condition	4-04 C3	−CE Display Bit P0	4-58 B5
	+Addr Sw 4 Bit 8 INT	4-01 D7	+ALU Carry Bit 0	4-48 D8	−Branch Go FL	4-39 D9		4-60 E9	−CE Display Bit P1	4-58 B5
▶	+Address Bus A Bit 8	4-60 B8	+ALU Carry Bit 1	4-48 D8	+Branch Go FL	4-39 D9		4-62 B2	CE Display Bits P0, 0-7, P1, 8-15	2-04 A6
	+Address Bus A Bit 9	4-60 B8	+ALU Carry Bit 2	4-48 C8	+Branch Unconditional	4-46 B6	Bus Thermal Switch	4-60 E9	+CE Display Bits P0, 0-7, P1, 8-15	4-58 B7
	+Address Bus A Bit 10	4-60 B8	+ALU Carry Bit 3	4-48 C8	+Branch Uncond	4-24 B3		4-62 B2	−CE Display Switch ALU INT	4-57 B9
	+Address Bus A Bit 11	4-60 B8	+ALU Carry Bit 4	4-48 D6	+Bus Any I/O Error	4-60 D9	+Bus TW Indicator	4-60 D9	−CE Display Switch FDR INT	4-57 B9
	+Address Bus A Bit 12	4-60 B8	+ALU Carry Bit 5	4-48 D6		4-62 A2		4-62 A2	−CE Display Switch I/O Displ INT	4-57 B9
	+Address Bus A Bit 13	4-60 B8	+ALU Carry Bit 6	4-48 C6	+Bus Any I/O Working	4-60 D9	+Bus Unbuffered I/O Busy	4-60 D9	−CE Display Switch MAR INT	4-57 B9
	+Address Bus A Bit 14	4-60 B8	+ALU Carry Bit 7	4-48 C6		4-62 A2		4-62 A2	−CE Display Switch OCU1 INT	4-57 B9
	+Address Bus A Bit 15	4-60 B8	+ALU Carry Bit 8	4-48 D5	+Bus Any Sense Bit	2-06 A9	+Bus Uncond Check Stop	4-60 D9	−CE Display Switch OCU2 INT	4-57 B9
D	+Address Bus B Bit 8	4-62 E3	+ALU Carry Bit 9	4-48 D5		4-60 E9	+Byte Store	4-16 B5	−CE Display Switch OP REG INT	4-57 B9
	+Address Bus B Bit 9	4-62 E3	+ALU Carry Bit 10	4-48 C5		4-62 B2			−CE Display Switch SAR INT	4-57 B9
	+Address Bus B Bit 10	4-62 E3	+ALU Carry Bit 11	4-48 C5	−Bus BSCA Wait	4-60 D9			−CE Display Switch SDR INT	4-57 B9
	+Address Bus B Bit 11	4-62 E3	+ALU Carry Bit 12	4-48 D3		4-62 B2	+Carry FL	4-54 A7	−CE Display Switch TDR INT	4-57 B9
	+Address Bus B Bit 12	4-62 E3	+ALU Carry Bit 13	4-48 D3	+Bus Buffered I/O Busy	4-60 D9	+Carry Into Pos 7	4-48 C6	CE Display to Inhibit	4-22 B9
	+Address Bus B Bit 13	4-62 E3	+ALU Carry Bit 14	4-48 C3		4-62 A2	CC0 FL	4-54 B7	CE Display 1	4-58 A5
▶	+Address Bus B Bit 14	4-62 E3	+ALU Carry Bit 15	4-48 C3	Bus Cable Connector 1	4-60 A8	CC1 FL	4-54 C7	CE Display 2	4-58 B5
	+Address Bus B Bit 15	4-62 E3	−ALU End Gate	4-48 A2	Bus Cable Connector 2	4-60 C9	+CC1 or 2	4-54 C8	CE Key	4-01 D8
	−Address Bus Bit 8	4-62 E4	+ALU not Zero	4-48 B9	Bus Cable Connector 3	4-60 D9	CC2 FL	4-54 C7	−CE Key Sw INT	4-01 D7
	−Address Bus Bit 9	4-62 E4	+ALU or Bus or SU Check	2-01 C3	−Bus Check FL	2-06 C9	CC3 FL	4-54 D7	+CE Key Sw On	4-20 B4
	−Address Bus Bit 10	4-62 E4	−ALU OR Gate	4-48 B2	+Bus Check FL	2-06 C9	+CC0 FL	4-54 B8	+CE Mode Sw INT	4-57 E8
			+ALU Test FL	2-01 A6	+Bus Clock Pulse 1A	4-60 A8	+CC1 FL	4-54 B8	+CE Mode Switch INT	4-57 D3
E			−ALU Test FL	2-01 B6	+Bus Clock Pulse 1B	4-62 D3	+CC2 FL	4-54 B8	+Change Carry 0	4-24 A6
	* From WC361		−ALU to FDR	4-46 C5	+Bus Clock Pulse 2A	4-60 A8	+CC3 FL	4-54 B8	−Change MAR Bit P0	4-38 E9
	** Logic Page A7052		+ALU to FDR Del	4-46 C3	+Bus Clock Pulse 2B	4-62 D3	+CE Addr Switch 1 Bit 1 INT	4-57 D6	−Change MAR Bit P1	4-38 C9
	*** From WC251		+ALU to FDR Delayed	4-46 C3	+Bus CSW Update Interrupt	4-62 B2	+CE Addr Switch 1 Bit 2 INT	4-57 D6	+Change Parity Sum Bit 1-7	4-48 E9
	† From WC541		+ALU to LS	4-30 A2		4-60 D9	+CE Addr Switch 1 Bit 4 INT	4-57 D6	+Change Parity Sum Bit 2-7	4-48 E8
	†† From WC21		ALU to LS	4-30 B4	+Bus CTRL Strobe A	4-60 A4	+CE Addr Switch 1 Bit 8 INT	4-57 D6	+Change Parity Sum Bit 3-7	4-48 E8
	††† From PSWC221		+ALU to SAR	4-10 B3		4-60 A8	+CE Addr Switch 2 Bit 1 INT	4-57 C6	+Change Parity Sum Bit 5-7	4-48 E8

	2	3	4	5	6	7	8	9
	+Change Parity Sum Bit 6-7	4-48 E7	+CS Data in Bits P1, 8-15	4-62 E6	+CS Request 3 FL	4-64 B3	+CY0 or CY2 not MANOP	4-34 C5	−Delta Time 3 FL	4-02 B5
	+Change Parity Sum Bit 7	4-48 E7	+CS Decrement	4-62 C4	−CS Request 4 FL	4-64 B3	+CY0 Process not CS	4-34 B5	+Delta Time 3 FL	4-02 B5
	+Change Parity Sum Bit 9-15	4-48 D5	−CS Decrement by 1	4-62 E5	+CS Request 4 FL	4-64 B3			+Delta Time 1 Freeze FL	4-59 A5
	−Change Parity Sum Bit 9-15	4-48 E6	−CS Decrement by 2	4-62 E5	−CS Select Device 1	4-64 A9			+Delta Time 2 Freeze FL	4-59 A5
	−Change Parity Sum Bit 10-15	4-48 E6	−CS Decrement Device 1**	4-62 C2	−CS Select Device 2	4-64 A9	−Data Bus Bit 8	4-60 C8	+Delta Time 3 Freeze FL	4-59 B5
	−Change Parity Sum Bit 11-15	4-48 E5	−CS Decrement Device 2**	4-62 C2	−CS Select Device 3	4-64 B9		4-62 B2	+Delta T8	4-02 C9
A	+Change Parity Sum Bit 13-15	4-48 E7	−CS Decrement Device 3**	4-62 D2	−CS Select Device 4	4-64 B9	−Data Bus Bit 9	4-60 C8	−Dev Address 15 Intrr	4-62 A4
	−Change Parity Sum Bit 13-15	4-48 E5	−CS Decrement Device 4**	4-62 D2	−CS Store 8-15	4-64 E6		4-60 E5	+Dev Adr 15 Intr FL	4-62 A5
	+Change Parity Sum Bit 15	4-48 E4	+CS Device 1 or 3 A2, B2	4-34 C4	−CS Store 0-7	4-64 E6		4-62 B2	−Display Register Mode INT	4-01 C8
	Change PL FL	4-32 C5	+CS Device 2 or 3 FL	4-62 A6	+CS Test FL	4-64 C6	−Data Bus Bit P1	4-60 C8	+Display Sense Strobe	4-60 A3
	−Change SU Bit P0	4-52 D5	−CS Device 2 or 3 FL	4-62 B6	+CS Time T3	4-64 D9		4-62 B2	DL Request FL	4-32 C2
	−Change SU Bit P1	4-52 A5	−CS Device 3 or 4 FL	4-62 A6	+CS Write	4-64 C4	−Data Bus Bit 10	4-60 E5		
▶	−Change Sum Parity Bit P0	4-52 E4	+CS Device 3 or 4 FL	4-62 A6	−CS Write Device 1**	4-64 C2		4-60 C8		
	−Change Sum Parity Bit P1	4-52 B4	−CS Force Regen SDR 0-7	4-64 E6	−CS Write Device 2**	4-64 C2		4-62 B2	Eight Shift	4-40 D7
	−Channel End Active	4-62 A7	−CS Force Regen SDR 8-15	4-64 E6	−CS Write Device 3**	4-64 D2	−Data Bus Bit 11	4-60 C8	−End Op CY0	4-24 B4
	+Channel End FL	4-62 A6	+CS Halfword	4-62 C4	−CS Write Device 4**	4-64 D2		4-62 C2	−End Op CY1	4-24 B4
	+Channel Mask FL	4-62 B6	−CS Halfword Device 1**	4-62 C2	−CSW Update Interr	4-62 B4	−Data Bus Bit 12	4-60 C8	−End Op CY2	4-24 B5
	−CLC	4-54 A2	−CS Halfword Device 2**	4-62 C2	−CTRL and Auto LC	4-36 A4		4-62 C2	+End Op FL	4-24 B7
	+CLC	4-54 A2	−CS Halfword Device 3**	4-62 D2	+CTRL Reset PL Reg	4-32 A3	−Data Bus Bit 13	4-60 D5	+End Op Gate	4-24 B6
B	−CLC not End Op	4-24 A9	−CS Halfword Device 4**	4-62 D2	+CTRL Set PL Reg	4-32 A3		4-60 C8		
	+CLC or CTRL	4-36 B6	−CS Halfword FL	4-62 D6	+CTRL 00-07	4-60 C3		4-62 C2		
	+Clock Advance Pulse A	4-02 C3	+CS Halfword FL	4-62 D6	+CTRL 08-0F	4-60 C3	−Data Bus Bit 14	4-60 D5		
	−Clock Bin 1 FL	4-02 E6	+CS Increment	4-62 C4	+CTRL 10	4-60 D3		4-60 C8	FDR	4-46 D5
	+Clock Bin 2 FL	4-02 E7	−CS Increment by 1	4-62 E5	+CTRL 11	4-60 D3		4-62 C2	+FDR Bit 0 FL	4-46 C6
	−Clock Bin 2 FL	4-02 E7	−CS Increment by 2	4-62 E5	+Current PL Bit 1	4-22 A2	−Data Bus Bit 15	4-60 D5	+FDR Bit 1 FL	4-46 C6
▶	−Comp Equal FL	4-58 C9	−CS Increment Device 1**	4-62 C2	+Current PL Bit 2	4-22 A2		4-60 C8	+FDR Bit 2 FL	4-46 C6
	Console Keys	4-01 E4	−CS Increment Device 2**	4-62 C2	+Current PL Bit 4	4-22 B2		4-62 C2	+FDR Bit 3 FL	4-46 C6
	Core Storage-Inhibit/Sense	4-13	−CS Increment Device 3**	4-62 D2	Current PL Register	4-32 B6	Data Bus In	4-62 C4	+FDR Bit 4 FL	4-46 C6
	+Corr Sum Bit 8	4-48 B6	−CS Increment Device 4**	4-62 E2	+Current PL0 FL	4-32 B7	Data Bus Parity Check	4-62 D9	+FDR Bit 5 FL	4-46 C6
	+Corr Sum Bit 9	4-48 B6	+CS Inhibit Bits P0, 0-7	4-62 E6		4-32 D8	−Data Error FL	4-32 D4	+FDR Bit 6 FL	4-46 C6
	+Corr Sum Bit 10	4-48 A6	+CS Inhibit Check	4-64 D9	+Current PL1 FL	4-32 B7	+Data Sw to OPR	4-18 A3	+FDR Bit 7 FL	4-46 C6
	+Corr Sum Bit 11	4-48 A6	+CS Inhibit Check FL	4-62 C8		4-32 D8	+Data Sw 1 Bit 1 INT	4-01 D3	+FDR Bit 8 FL	4-46 C6
C	+Corr Sum Bit 12	4-48 A6	−CS INT Select Device 1	4-62 A7	+Current PL2 FL	4-32 B7	+Data Sw 1 Bit 2 INT	4-01 D3	+FDR Bit 9 FL	4-46 C6
	+Corr Sum Bit 13	4-48 A6	−CS INT Select Device 2	4-62 A7		4-32 D8	+Data Sw 1 Bit 4 INT	4-01 D3	+FDR Bit 10 FL	4-46 C6
	+Corr Sum Bit 14	4-48 A6	−CS INT Select Device 3	4-62 B7	+Current PL3 FL	4-32 B7	+Data Sw 1 Bit 8 INT	4-01 D3	+FDR Bit 11 FL	4-46 C6
	−CPU Check Reset Sw INT	4-57 E8	−CS INT Select Device 4	4-62 B7		4-32 C8	+Data Sw 2 Bit 1 INT	4-01 D3	+FDR Bit 12 FL	4-46 B6
	−CPU Reset Sw INT	4-57 E8	+CS Interface Check FL	4-62 C6	+Current PL4 FL	4-32 B7	+Data Sw 2 Bit 2 INT	4-01 D3	+FDR Bit 13 FL	4-46 B6
	CPU SENS Decoding	4-62 D6	−CS Interface Check FL	4-62 C6		4-32 C8	+Data Sw 2 Bit 4 INT	4-01 D3	+FDR Bit 14 FL	4-46 B6
▶	+CPU SENS's	4-62 E5	+CS LS Select	4-32 A6	+Current PL5 FL	4-32 B7	+Data Sw 2 Bit 8 INT	4-01 D3	+FDR Bit 15 FL	4-46 B6
	CPU SENS-DATA Selection	4-62 A8	+CS LS Select Time	4-32 A6		4-32 C8	+Decimal	4-44 B3	+FDR Bit P0 FL	4-46 C6
	CPU Status Display	4-57 A4	+CS Modified SAR Bit 15	4-62 D9	+Current PL6 FL	4-32 B7	−Decimal	4-44 B3	+FDR Bit P1 FL	4-46 C6
	−CS Addr Check FL	4-62 C8		4-64 D9		4-32 C8	+Decrement by 1	4-39 A4	−FDR Invert 0-7	4-46 B9
	+CS Addr Check FL	4-62 C8	−CS Re-Address	4-62 C4	+Current PL7 FL	4-32 B7	+Decrement by 2	4-39 B4	−FDR Invert 12-15	4-46 C9
	+CS Address Check	4-64 D9	+CS Read	4-62 C4		4-32 C8	+Decrement Carry 0	4-38 D8	−FDR Invert 8-11	4-46 B9
	+CS Byte	4-62 C4	−CS Read Device 1**	4-62 C2	Customer Address Switches	4-01 C5	+Decrement Carry 8	4-38 C6	+FDR Invert 8-15	4-46 B8
D	+CS Byte Device	4-64 E4	−CS Read Device 2**	4-62 C2	Customer Data Switches	4-01 D2	+Del Comp Stop Sw INT	4-57 E8	FDR Set	4-46 C4
	−CS Byte Device 1**	4-62 C2	−CS Read Device 3**	4-62 D2	Customer Mode Switches	4-01 C7	+Delayed Oscillate	4-02 C4	−FDR to Display Sw	4-22 C7
	−CS Byte Device 2**	4-62 C2	−CS Read Device 4**	4-62 D2	+CY2 or CY1	4-44 A2	+Delta Cycle FL1	4-24 D8	+FDR True 0-15	4-46 A9
	−CS Byte Device 3**	4-62 D2	+CS Read FL	4-62 C6	+CY2 or CY3	4-44 A2	+Delta Cycle FL2	4-24 D8	+FF Format Instr	4-18 C8
	−CS Byte Device 4**	4-62 E2	−CS Read FL	4-62 D6	+Cycle FL1	4-24 D8	+Delta CY0	4-24 D8	+File Indicatort	4-01 A8
	+CS Counter Carry	4-62 D9	−CS Request Device 1**	4-62 B2	+Cycle FL2	4-24 D8	+Delta CY1	4-24 D8	+Force	4-22 A7
▶	+CS Counter Zero	4-62 D9	−CS Request Device 2**	4-62 C2	Cycle FL1	4-24 D7	+Delta CY2	4-24 E8	−Force FDR Bit P0	4-52 E8
	−CS CTRL Lines Even	4-62 C6	−CS Request Device 3**	4-62 D2	Cycle FL2	4-24 D7	+Delta CY2 not Write Cycle	4-22 B6	−Force FDR Bit P1	4-52 C8
	−CS Data Out Gate 0-7	4-62 D7	−CS Request Device 4**	4-62 D2	+Cycle Steal and T3	4-62 C7	+Delta CY3	4-24 E8	−Force Invert 0-7	4-46 A9
	−CS Data Out Gate 8-15	4-62 D7	+CS Request FL Device 1	4-62 A8	+Cycle Steal FL	4-62 B6	−Delta CY3 Branch and Store A7	4-34 A5	−Force Overflow	4-54 D5
	−CS Data Bus Bits P0, 0-7, P1, 8-15	4-64 E8	+CS Request FL Device 1 or 2	4-62 A8	−Cycle Steal FL	4-62 B6	−Delta Proc w-o Check	4-36 D3	−Force Zero or Norm Op 0-7	4-22 A7
	−CS Data Bus Bits P0, 0-7, P1, 8-15***	4-64 E5	+CS Request FL Device 1, 2, or 3	4-62 A5	−Cycle Steal or LOG	4-16 D3	+Delta Process	4-04 A9	−Force Zero or Norm Op 8-15	4-22 A7
			+CS Request FL Device 2 not 1	4-62 A8	+Cycle 0	4-24 D9	+Delta Process FL	4-04 A9	+From REG Decode 0	4-18 A7
			+CS Request FL Device 3 not 1 or 2	4-62 A8	+Cycle 0 or Cycle 1	4-24 E9	+Delta Process not CS Reg	4-04 A9	+From REG Decode 1	4-18 A7
E			+CS Request FL Device 4 not 1, 2, or 3	4-62 A8	+Cycle 1	4-24 D9	+Delta Process w-o Check	4-04 C9	+From REG Decode 2	4-18 A7
			−CS Request 1 FL	4-64 A3	+Cycle 1 or Cycle 2	4-24 D9	+Delta Process w-o Check and CSR	4-04 B9	+From REG Decode 3	4-18 A7
			+CS Request 1 FL	4-64 A3	+Cycle 2	4-24 E9	+Delta Time 1 FL	4-02 A5	+From REG Decode 4	4-18 A7
			+CS Request 2 FL	4-64 A3	+Cycle 2 or Cycle 3	4-24 E9	−Delta Time 1 FL	4-02 B5	+From REG Decode 5	4-18 A7
			−CS Request 2 FL	4-64 A3	+Cycle 3	4-24 E9	−Delta Time 2 FL	4-02 B5	+From REG Decode 6	4-18 A7
			−CS Request 3 FL	4-64 B3	−Cycle 3 or LOG or CS	4-16 D4	+Delta Time 2 FL	4-02 B5	+From REG Decode 7	4-18 A7

* From WC361
** Logic Page A7052
*** From WC251
† From WC541
†† From WC21
††† From PSWC221

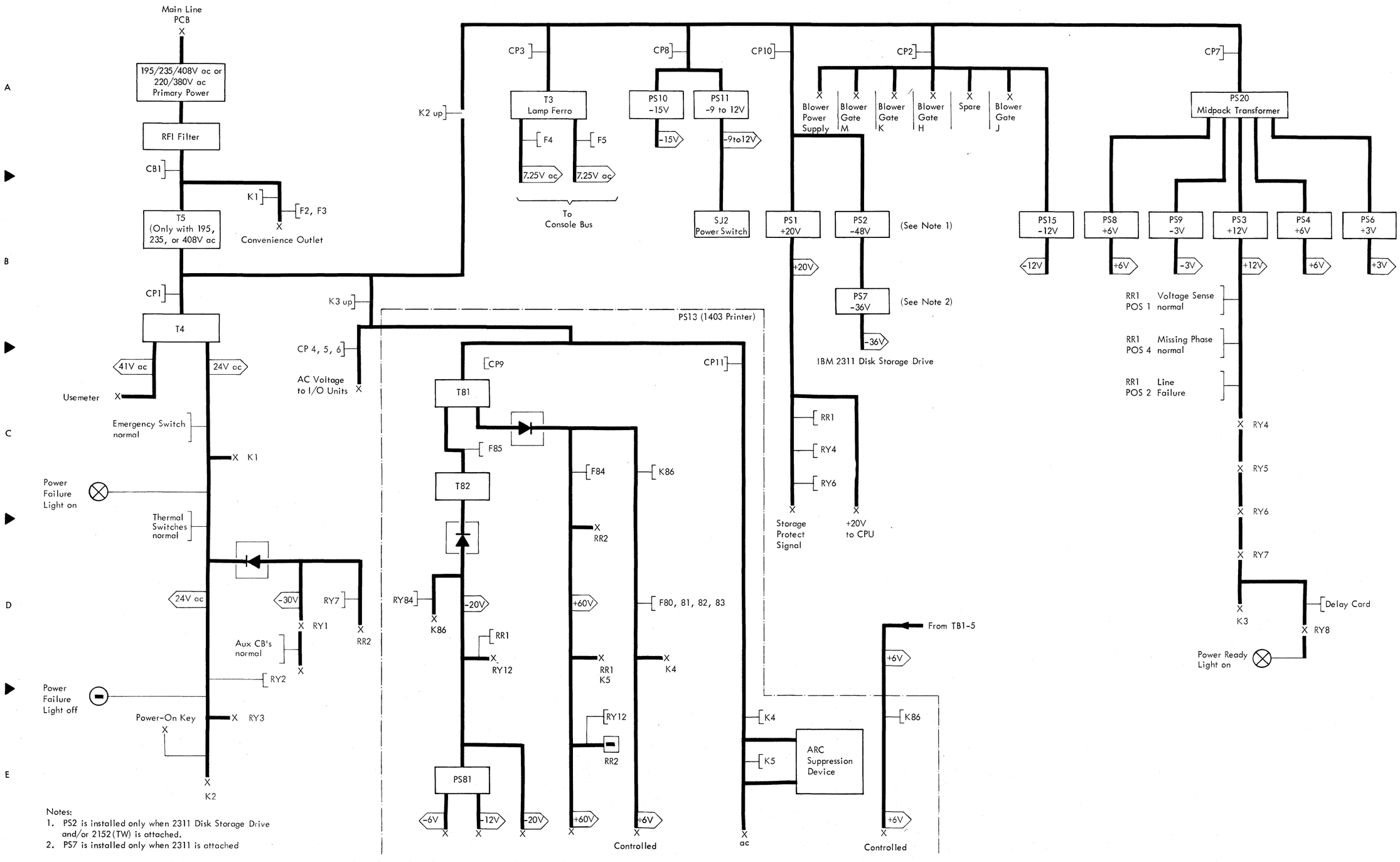
Diagram 4-99. Signal Reference List (Part 2 of 5) (04344) 2020 ⩾ 50,000 FEMDM Vol 1 (8/69)

2		3		4		5		6		7		8		9	
	+From REG Select Freeze FL	4-59 C5	+Inhibit Bit 10	4-16 D8		−Intern SU Bit 7	4-40 D8	+LOG Bit 10	4-22 C4	+LS Sense Bit P1	4-30 E9
	+From Register Select	4-34 E6		4-22 C9		+Intern SU Bit 8	4-40 D8	+LOG Bit 11	4-22 B4	−LS to Any Reg	4-30 E7
			+Inhibit Bit 11	4-16 D8		−Intern SU Bit 8	4-40 D8	+LOG Bit 12	4-22 B4	+LS to FDR	4-46 B5
				4-22 C9		+Intern SU Bit 9	4-40 D8	+LOG Bit 13	4-22 B4	+LS to FDR Delayed	4-46 C3
	+Gate LS Write T7	4-36 C4	+Inhibit Bit 12	4-16 D8		−Intern SU Bit 9	4-40 D8	+LOG Bit 14	4-22 B4	−LS to FDR Reset	4-46 D2
	Gate to REG Decode	4-18 D7		4-22 B9		+Intern SU Bit 10	4-40 D8	+LOG Bit 15	4-22 A4	+LS to MAR	4-38 B4
A	−Generate Addr and Inhib Chk	4-62 C7	+Inhibit Bit 13	4-16 D8		−Intern SU Bit 10	4-40 C8	+LOG Bit 7 FL	4-22 D3	+LS to SAR	4-10 B3
				4-22 B9		+Intern SU Bit 11	4-40 D8	+LOG Bit 8 FL	4-22 D3	−LS to SAR or MAR	4-30 E7
			+Inhibit Bit 14	4-16 D8		−Intern SU Bit 11	4-40 C8	+LOG Bit 9 FL	4-22 D3	+LS to TDR	4-40 C4
	+Halfword Store	4-16 B4		4-22 B9		+Intern SU Bit 12	4-40 D8	LOG CY0 and CY1 FL	4-10 D6	−LS to TDR or FDR	4-30 E7
	+Hold Run Condition	4-04 C7	+Inhibit Bit 15	4-16 D8		−Intern SU Bit 12	4-40 C8	LOG CY0 and CY2 FL	4-10 D6	−LS to TDR Reset	4-40 E5
	−HW Boundary FL	4-39 A9		4-22 B9		−Intern SU Bit 12*	4-40 C9	+LOG Decrement FL	4-22 B3	+LS to TDR Set Pulse	4-40 D5
▶			+Inhibit Bit P0	4-16 E8		+Intern SU Bit 13	4-40 D8	−LOG FL	4-22 A4	−LS Write T2	4-36 A9
				4-22 E9		−Intern SU Bit 13	4-40 C8	−LOG Force System Reset	4-22 A6	−LS Write T7, T8, T5	4-36 C8
	+I-Addr to SAR Gate	4-04 C6	+Inhibit Bit P1	4-16 D8		+Intern SU Bit 14	4-40 D8	+LOG Increment FL	4-22 C3	+LSA Check FL	2-02 B9
	+I/O Bus to FDR Del	4-46 C3		4-22 E9		−Intern SU Bit 14	4-40 C8	−LOG REG 6 FL	4-22 A3	−LSA Check FL	2-02 B9
	−I/O Bus to FDR Reset	4-46 D2	+Inhibit Bits 0-7-P1 Even	4-16 C9		+Intern SU Bit 15	4-40 D8	−LOG REG 7 FL	4-22 A3	+LSA or MOD Check	2-01 C3
		4-46 C2		2-04 B6		−Intern SU Bit 15	4-40 C8	+LOG REG 12 FL	4-22 B3	−LW Addr Chk FL	4-39 A9
	+I/O Bus to FDR 0-7	4-46 A5	−Inhibit Bits 4K	4-13 B3		−Intern SU Bit P0	4-40 E8	−LOG Reset	4-22 A5		
B	+I/O Bus to FDR 8-15	4-46 A5	+Inhibit Bits 8-15-P1 Even	2-04 B6		+Intern SU Bit P0	4-40 E8	LOG Reset FL	4-22 A5		
	+I/O Bus to LS	4-30 A2		4-16 B9		+Intern SU Bit P1	4-40 E8	−LOG SAR Power	4-22 A8	−MANOP	4-20 B6
	+I/O Check Reset Key INT	4-01 E5	−Inhibit Bits 4K	4-13 B3		−Intern SU Bit P1	4-40 E8	Long Time FL	4-12 B3	+MANOP	4-20 B6
	+I/O Clock Pulse 1	4-02 D8	+Inhibit Bits 8-15-P1 Even	2-04 B6		−Invalid Op	4-24 C4	+LS Addr Check Gate	4-30 E8	+MANOP ALU not Zero	2-01 B8
	+I/O Clock Pulse 2	4-02 E8		4-16 B9		+Invert Parity	2-01 C8	+LS Addr Check Gate Freeze FL	4-59 D5	+MANOP FDR Invert 0-15	4-46 B7
	+I/O Display Address Out	4-60 A6	−Inhibit Check FL	2-04 C8		−Invert Parity	2-01 C8	+LS to Any Reg Freeze FL	4-59 D5	−MANOP FL	4-20 B6
▶	+I/O Display FL	4-60 B3	−Inhibit FDR True	4-46 A8		+Invert Parity FL	4-24 B9	+LS Data-In Bit 0	4-30 B5	+MANOP FL	4-20 B6
	+I/O Op Auto LC	4-36 A6	+Inhibit Left FL	2-04 C8		+Invert Parity Sw INT	4-57 E8	+LS Data-In Bit 1	4-30 B5	−MANOP Inbus to FDR	4-20 E7
	+I/O Address Error	2-06 B9	−Inhibit LS Write T8	4-36 D6		Invert Sw	4-46 C8	+LS Data-In Bit 2	4-30 B5	−MANOP LS Write	4-36 B4
	−IBL or TRBL-CY0	4-40 B5	+Inhibit Mem Ext Bits P0	4-16 D9		+Invert Sw Bit 0	4-46 E9	+LS Data-In Bit 3	4-30 B5	+MANOP not LOG	4-22 A4
	+ICPL	4-20 A5	+Inhibit Right FL	2-04 C8		+Invert Sw Bit 1	4-46 E9	+LS Data-In Bit 4	4-30 B5	+MANOP Set ALU Zero	4-20 D7
	−ICPL FL	4-20 A5	Inhibit Time FL	4-12 B3		+Invert Sw Bit 2	4-46 E9	+LS Data-In Bit 5	4-30 B5	−MANOP Suppr 0-7	4-20 E7
	−ICPL Loop Sw INT	4-57 E8	−Inhibit Timing	4-12 C4		+Invert Sw Bit 3	4-46 D9	+LS Data-In Bit 6	4-30 A5	−MANOP Suppr 8-15	4-20 E7
C	+ICPL Reset FL	4-04 C3	−Initial CTRL Prog Load INT	4-01 D8		+Invert Sw Bit 4	4-46 D9	+LS Data-In Bit 7	4-30 A5	MAR	4-38 D5
	+Imm Comp Stop Sw INT	4-57 E8	+Interface Check Device 1	4-62 B9		+Invert Sw Bit 5	4-46 D9	+LS Data-In Bit 8	4-30 A5	+MAR Bit 0 FL	4-38
	+Increment by 1	4-39 D4	+Interface Check Device 2	4-62 B9		+Invert Sw Bit 6	4-46 D9	+LS Data-In Bit 9	4-30 A5	−MAR Bit 1	4-38 D6
	+Increment by 2	4-39 D4	+Interface Check Device 3	4-62 B9		+Invert Sw Bit 7	4-46 D9	+LS Data-In Bit 10	4-30 A5	+MAR Bit 1 FL	4-38 D6
	+Increment Carry 0	4-38 D8	+Interface Check Device 4	4-62 B9		+Invert Sw Bit 8	4-46 D9	+LS Data-In Bit 11	4-30 A5	+MAR Bit 2 FL	4-38 D6
	+Increment Carry 8	4-38 C6	+Intern ICPL or ST Mode	4-20 E6		+Invert Sw Bit 9	4-46 D9	+LS Data-In Bit 12	4-30 A5	+MAR Bit 3 FL	4-38 D6
▶	+Inhibit Bit 0	4-16 E8	−Intern LS Disalt	4-20 B4		+Invert Sw Bit 10	4-46 D9	+LS Data-In Bit 13	4-30 A5	+MAR Bit 4 FL	4-38 D6
		4-22 E9	−Intern MAR Bit 0	4-39 C7		+Invert Sw Bit 11	4-46 D9	+LS Data-In Bit 14	4-30 A5	+MAR Bit 5 FL	4-38 C6
	+Inhibit Bit 1	4-16 D8	+Intern MAR Bit 2	4-38 E9		+Invert Sw Bit 12	4-46 D9	+LS Data-In Bit 15	4-30 A5	+MAR Bit 6 FL	4-38 C6
		4-22 E9	−Intern MAR Bit 8	4-38 C8		+Invert Sw Bit 13	4-46 D9	+LS Data-In Bit P0	4-30 B5	+MAR Bit 7 FL	4-38 C6
	+Inhibit Bit 2	4-16 D8	+Intern MAR Bit 14	4-38 B9		+Invert Sw Bit 14	4-46 D9	+LS Data-In Bit P1	4-30 A5	−MAR Bit 8	4-38 B6
		4-22 E9	+Intern MAR Bits 0-13 Zero	4-38 D9		+Invert Sw Bit 15	4-46 D9	−LS Data-Out Bit P0, 0-7, P1, 8-15	4-30 E8	+MAR Bit 8 FL	4-38 B6
	+Inhibit Bit 3	4-16 D8	−Intern MAR Bits 0-7 Zero	4-38 E9		+Invert Sw Bit P0	4-46 E7	+LS Disalt	4-20 D7	−MAR Bit 9	4-38 B6
		4-22 E9	−Intern MAR Bits 8-13 Zero	4-38 B9			4-46 E9	+LS Disalt or LOG	4-20 D7	+MAR Bit 9 FL	4-38 B6
D	+Inhibit Bit 4	4-16 D8	−Intern MAR Bits 9-11 Zero	4-38 B9		+Invert Sw Bit P1	4-46 E7	+LS New PL Zone Gate	4-32 A7	−MAR Bit 10	4-38 B6
		4-22 E9	+Intern ST DASF	4-20 B4			4-46 D9	LS Register	4-30 E5	+MAR Bit 10 FL	4-38 B6
	+Inhibit Bit 5	4-16 D8	+Intern ST Test	4-20 B4		+IOC Indicator †	4-01 A8	+LS Sense Bit 0	4-30 E9	−MAR Bit 11	4-38 B6
		4-22 E9	−Intern ST Test	4-20 B4				+LS Sense Bit 1	4-30 E9	+MAR Bit 11 FL	4-38 B6
	+Inhibit Bit 6	4-16 D8	−Intern SU Bit 0	4-40 D8				+LS Sense Bit 2	4-30 E9	−MAR Bit 12	4-38 A6
		4-22 E9	+Intern SU Bit 0	4-40 C8		Lamp Test Sw	4-01 C8	+LS Sense Bit 3	4-30 E9	+MAR Bit 12 FL	4-38 A6
▶	+Inhibit Bit 7	4-16 D8	+Intern SU Bit 1	4-40 C8		−LC End Op Gate	4-24 C9	+LS Sense Bit 4	4-30 E9	−MAR Bit 13	4-38 A6
		4-22 E9	−Intern SU Bit 1	4-40 D8		+LC1 FL	4-24 C9	+LS Sense Bit 5	4-30 E9	+MAR Bit 13 FL	4-38 A6
	+Inhibit Bit 8	4-16 D8	−Intern SU Bit 2	4-40 D8		+LC2 FL	4-24 C7	+LS Sense Bit 6	4-30 E9	−MAR Bit 14	4-38 A6
		4-22 C9	+Intern SU Bit 2	4-40 C8		+Load FL	4-04 D7	+LS Sense Bit 7	4-30 E9	+MAR Bit 14 FL	4-38 A6
	+Inhibit Bit 9	4-16 D8	−Intern SU Bit 3	4-40 D8		−Load Key	4-04 D6	+LS Sense Bit 8	4-30 E9	−MAR Bit 15	4-38 A6
		4-22 C9	+Intern SU Bit 3	4-40 C8		+Load Key INT	4-01 E5	+LS Sense Bit 9	4-30 D9	+MAR Bit 15 FL	4-38 A6
			−Intern SU Bit 4	4-40 D8		−Load Key INT	4-01 E5	+LS Sense Bit 10	4-30 D9	+MAR Bit P0 FL	4-38 D6
E			+Intern SU Bit 4	4-40 C8		Local Store	4-30 C7	+LS Sense Bit 11	4-30 D9	+MAR Bit P1 FL	4-38 C6
			+Intern SU Bit 5	4-40 C8		−LOG	4-22 A5	+LS Sense Bit 12	4-30 D9	−MAR Bit 2	4-38 D6
			−Intern SU Bit 5	4-40 D8		+LOG	4-22 A5	+LS Sense Bit 13	4-30 D9	−MAR Bit 3	4-38 D6
			+Intern SU Bit 6	4-40 C8		+LOG ALU to Inhibit Left FL	4-22 C3	+LS Sense Bit 14	4-30 D9	−MAR Bit 4	4-38 D6
			−Intern SU Bit 6	4-40 D8		+LOG ALU to Inhibit Right FL	4-22 C3	+LS Sense Bit 15	4-30 D9	−MAR Bit 5	4-38 C6
			+Intern SU Bit 7	4-40 D8		−LOG and Process	4-36 E4	+LS Sense Bit P0	4-30 E9	−MAR Bit 6	4-38 C6

* From WC361
** Logic Page A7052
*** From WC251
† From WC541
†† From WC21
††† From PSWC221

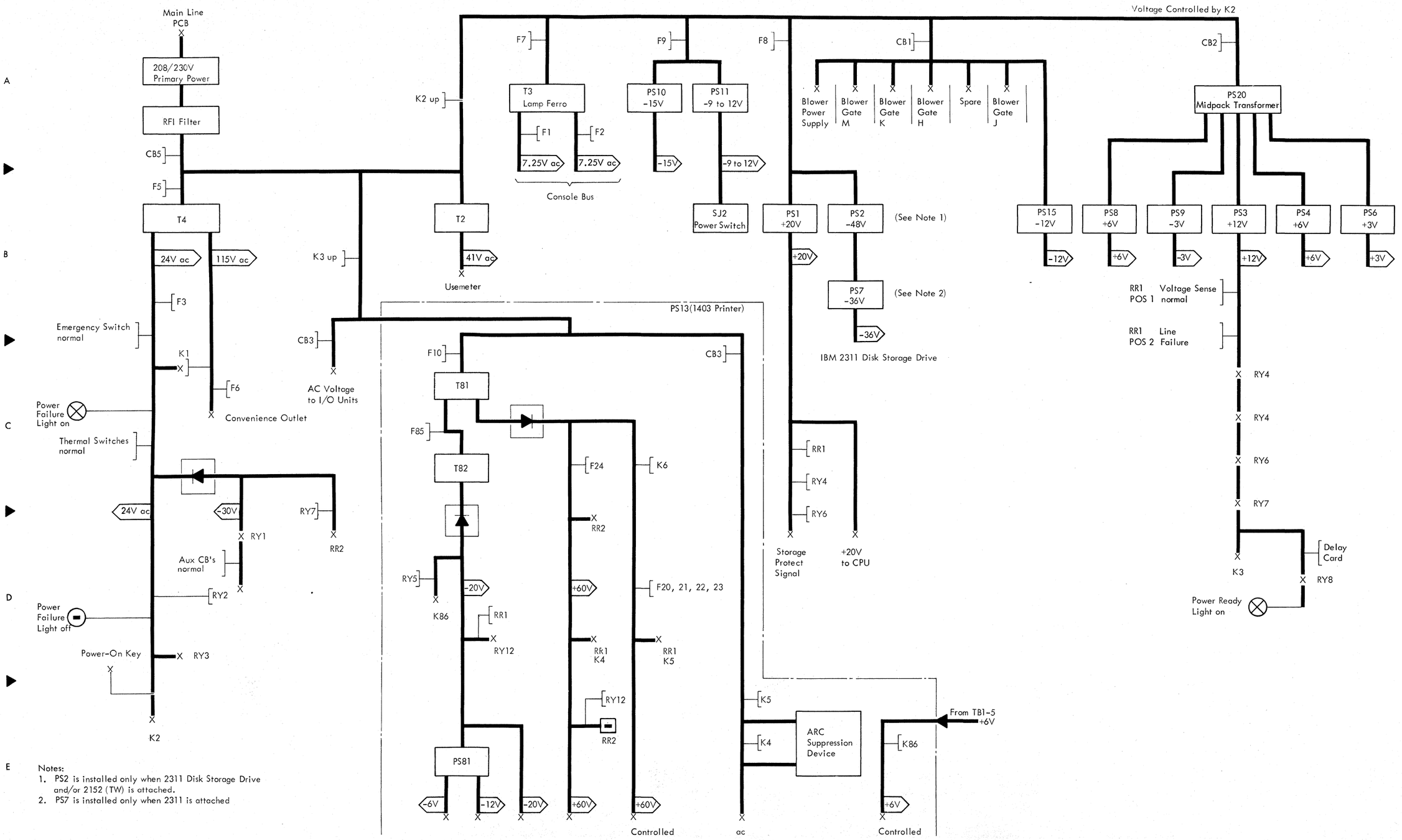
2	3	4	5	6	7	8	9
—MAR Bit 7	4-38 C6	+OCU 1 Bit P0	4-22 D5	+OPR Decode 5	4-18 E6	—Reset LOG REG 1	4-22 D2	+SDR Bit 14 FL	4-16 A4
—MAR to Display Sw	4-22 C7	—OCU 1 Bit P0 FL	4-22 E4	+OPR Decode 6	4-18 E6	—Reset LOG REG 2	4-22 D2	+SDR Bit 15 FL	4-16 A4
+MAR to LS	4-30 C3	+OCU 1 Bit P1	4-22 D5	+OPR Decode 7	4-18 E6	—Reset MAR	4-38 B4	+SDR Bit P0 FL	4-16 B4
—Missing Phase FL	2-01 A8	—OCU 1 Bit P1 FL	4-22 E4	+OPR Decode 8	4-18 E6	—Reset OPR	4-18 C4	+SDR Bit P1 FL	4-16 A4
+MOD by 1 FL	4-22 B3	+OCU 1 to Display Sw	4-22 B7	+OPR Decode 9	4-18 E6	—Reset PL Reg	4-32 A3	—SDR Reset	4-16 B3
—MOD Check FL	2-04 D8	+Odd SU Bits	4-42 D4	+OPR to Address Bus	4-60 A6	—Reset Pulse	4-04 B3	—SDR Set	4-16 B3
A +MOD Check FL	2-04 D8	+Odd SU Bits 0-1 OE 8-9	4-42 E4	+OPR to Display Sw	4-22 B7	—Retain FDR 0-7	4-46 D2	—SDR to INH 0-7	4-16 C6
+Modifier Bit 0	4-38 D8	+Odd SU Bits 0-3	4-42 E4	+Oscillate	4-02 B2	—RI Format Instr	4-46 B3	—SDR to INH 8-15	4-16 B6
+Modifier Bit 1	4-38 D8	+Odd SU Bits 0-3 OE 8-11	4-42 E4			+Run Condition	4-04 A7	+SDR to TDR	4-40 E4
+Modifier Bit 2	4-38 D8	+Odd SU Bits 12-15	4-42 D4			—RY7-3 N—C	4-04 D2	—SDR to TDR Reset	4-40 E5
+Modifier Bit 3	4-38 D8	+Odd SU Bits 4-7	4-42 E4	+Packed Arithmetic	4-48 A2	—RY7-3 N—O	4-04 D2	+SDR to TDR Set Pulse	4-40 D5
+Modifier Bit 4	4-38 D8	+Odd SU Bits 4-7 OE 12-15	4-42 D4	—Permit SA Gate	2-02 A7			+Select LS Y0	4-32 C8
▶ +Modifier Bit 5	4-38 D8	+Odd SU Bits 6-7	4-42 E4		4-30 C6			+Select LS Y1	4-32 C8
+Modifier Bit 6	4-38 D8	+Odd SU Bits 6-7 OE 14-15	4-42 D4	+PL Register 1 FL	4-32 A5	—SA Gate	4-30 E7	+Select LS Y2	4-32 C8
+Modifier Bit 7	4-38 D8	+Odd SU Bits 6-7 OE 14-15	4-42 C4	+PL Register 2 FL	4-32 A5	SAR	4-10 A5	+Select LS Y3	4-32 C8
+Modifier Bit 8	4-38 B8	+Odd SU Bits 8-11	4-42 D4	+PL Register 3 FL	4-32 A5	—SAR Bit P0 FL	4-10 B6	+Select LS Y4	4-32 B8
+Modifier Bit 9	4-38 B8	+Odd SU Bits 8-9	4-42 D4	+PL Register 4 FL	4-32 A5	+SAR Bit P0 FL	4-10 A8	+Select LS Y5	4-32 B8
+Modifier Bit 10	4-38 B8	OP REG	4-18 B5	+PL Register 5 FL	4-32 A5	+SAR Bit P0 to Display	4-22 E6	+Select LS Y6	4-32 B8
+Modifier Bit 11	4-38 B8	+OPR Bit 0 FL	4-18 C8	+PL Register 6 FL	4-32 AE	—SAR Bit P1 FL	4-10 B6	+Select LS Y7	4-32 B8
B +Modifier Bit 12	4-38 B8	+OPR Bit 1 FL	4-18 C8	+PL Register 7 FL	4-32 B5	+SAR Bit P1 FL	4-10 A8	—SENS 10	4-62 D6
+Modifier Bit 13	4-38 A8	+OPR Bit 2 FL	4-18 C8		4-32 A5	+SAR Bit P1 to Display	4-22 E6	—SENS 11	4-62 D6
+Modifier Bit 14	4-38 A8	+OPR Bit 3 FL	4-18 C8	—Power Failure	4-10 E5	+SAR Bit 0 FL	4-10 C6	+SENS 11	4-62 B3
+Modifier Bit 15	4-38 A8	+OPR Bit 4	4-18 B6	—Power On FL Active	4-04 D4	—SAR Bit 0 FL	4-10 C6	—SENS 12	4-62 D6
+Modifier Bit P0	4-38 E9	—OPR Bit 4	4-46 C2	+Power On Reset FL	4-04 D3	+SAR Bit 1 FL	4-10 C6	+SENS 13	4-62 D7
	4-38 D8	—OPR Bits 4 and 5	4-36 B6		4-04 D4	—SAR Bit 1 FL	4-10 C6	+SENS 14	4-62 D7
▶ +Modifier Bit P1	4-38 C9	+OPR Bit 4 FL	4-18 C8	+Predicted Sum Parity Bit P0	4-52 D5	+SAR Bit 2 FL	4-10 A8	+SENS 15	4-62 D7
	4-38 B8	+OPR Bit 5	4-18 B6	+Predicted Sum Parity Bit P1	4-52 A5	—SAR Bit 2 FL	4-10 B6	—SENS 16	4-62 E7
—Modifier Odd Parity	2-04 D4	+OPR Bit 5 FL	4-18 B8	—Prevent ALU and SU Check	4-46 A5	+SAR Bit 3 FL	4-10 A8	+SENS 16	4-62 E7
Modifier Parity P0	4-38 E9	+OPR Bit 6 FL	4-18 A6	—Prevent Force	4-22 B6	—SAR Bit 3 FL	4-10 B6	—SENS and Auto LC	4-36 A4
Modifier Parity P1	4-38 B9		4-18 B8	—Prevent MOD-SAR-INH Check	2-04 E7	+SAR Bit 4 FL	4-10 C6	SENS/CTRL Address Out	4-60 A7
Modifier 0-7	4-38 C7	+OPR Bit 7 FL	4-18 A6	—Prevent Storage Use	4-10 C3	—SAR Bit 4 FL	4-10 B6	Sense Amp Gate	4-12 C5
Modifier 8-15	4-38 A7		4-18 B8	—Proc Check not Override	4-04 A6	+SAR Bit 5 FL	4-10 C6	—Sense Amp Gate Off	4-12 C4
C —MVB Incr or ICPL	4-39 D2	—OPR Bit 8 FL	4-18 A8	—Proc Check Overr Sw INT	4-57 E8	—SAR Bit 5 FL	4-10 B6	+Sense Bit 0	4-62 E8
+MVH-XX	4-39 B3	+OPR Bit 8 FL	4-18 A6	+Process	4-04 A9	+SAR Bit 6 FL	4-10 A8	+Sense Bit 1	4-62 E8
—MVHS	4-40 B4		4-18 B8	—Process	4-04 D8	—SAR Bit 6 FL	4-10 B6	+Sense Bit 2	4-62 E8
+MVHS	4-40 B5	—OPR Bit 9 FL	4-18 A8	+Process Check FL	2-01 C8	+SAR Bit 7 FL	4-10 A8	+Sense Bit 3	4-62 E8
+MVHS CY0 or CY1	4-44 C5	+OPR Bit 9 FL	4-18 B8	—Process Check FL	2-01 C8	—SAR Bit 7 FL	4-10 B6	+Sense Bit 4	4-62 E8
—MVHS Force Cross	4-40 B5	+OPR Bit P0 FL	4-18 C8	+Process FL	4-04 A9	+SAR Bit 8 FL	4-10 A8	+Sense Bit 5	4-62 E8
▶ —MVHS 2 and Change P1	4-52 C4	+OPR Bit P1 FL	4-18 B8	—Process Meter CTRL	4-01 E7	+SAR Bit 9 FL	4-10 A8	+Sense Bit 6	4-62 E8
—MVHS 3 and Change P1	4-52 C4	—OPR Bit 10 FL	4-18 A8	—Process Meter Go	4-01 E7	+SAR Bit 10 FL	4-10 A8	+Sense Bit 7	4-62 E8
+MVN or MVZ	4-46 C3	+OPR Bit 10 FL	4-18 B8	+Process not Cycle Steal	4-04 A9	+SAR Bit 11 FL	4-10 A8	+Sense Bit 8	4-62 C8
—MVZ or MVN	4-46 A7	+OPR Bit 11 FL	4-18 B8	+Process w-o Check	4-04 C9	+SAR Bit 12 FL	4-10 A8		4-62 D4
		—OPR Bit 11 FL	4-18 A8	+Process w-o Check and CS	4-04 C9	+SAR Bit 13 FL	4-10 A8		4-62 E8
+New PL0	4-32 B5	+OPR Bit 12	4-18 A6	Program Level Register	4-32 A4	+SAR Bit 14 FL	4-10 A8		4-39 B9
+New PL1	4-32 B5	+OPR Bit 12 FL	4-18 B8	+Protected Area	4-16 E3	—SAR Bit 15 FL	4-10 B6	+Sense Bit 9	4-62 D4
D +New PL2	4-32 B5	+OPR Bit 13 FL	4-18 B8	+Pulse A	4-02 B2	+SAR Bit 15 FL	4-10 A8		4-62 C8
+New PL3	4-32 B5	+OPR Bit 14 FL	4-18 B8	+Pulse B	4-02 B2	—SAR Check FL	2-04 D8		4-62 E8
+New PL4	4-32 B5	+OPR Bit 15 FL	4-18 B8			+SAR Check FL	2-04 D8		4-39 B9
+New PL5	4-32 B5	—OPR Bit 15 FL	4-18 A8			—SAR Odd Parity	2-04 C4	+Sense Bit P1	4-62 B3
+New PL6	4-32 B5	+OPR Bit 15 FL	4-18 A6	+Read Cycle	4-02 C9	—SAR to Display Sw	4-22 B7		4-62 E8
+No Shift 0-7	4-42 B4	—OPR Bit 15 FL	4-18 A6	REG Decode	4-18 A7	SDR	4-16 A4	+Sense Bit 10	4-39 B9
▶ +No Shift 8-15	4-42 B4	+OPR Dec E or ICPL SENS	4-60 B3	+Regenerate Addr Check	4-39 A9	+SDR Bit 0 FL	4-16 B4		4-62 C4
+Normalize Sign	4-42 A2	+OPR Dec F or ICPL CTRL	4-60 B3	+Remote Reset Key INT	4-57 C9	+SDR Bit 1 FL	4-16 B4		4-62 C8
+Normalize Sign Active	4-24 A4	OPR Decode	4-18 D6	+Remote Start Key INT	4-57 C9	+SDR Bit 2 FL	4-16 B4		4-62 E8
—Normalize Sign and Change P1	4-48 D2	+OPR Decode A	4-18 E6	—Remote Start Key INT	4-57 C9	+SDR Bit 3 FL	4-16 B4	+Sense Bit 11	4-32 D4
—Normalized Sign Bit 15	4-42 A6	+OPR Decode B	4-18 E6	+Reset Carry	4-54 A8	+SDR Bit 4 FL	4-16 B4		4-54 C9
Not Shift 8 FL	4-40 A4	+OPR Decode C	4-18 E6	—Reset Carry	4-54 A8	+SDR Bit 5 FL	4-16 A4		4-62 C8
		+OPR Decode D	4-18 E6	—Reset CC 0-3	4-54 B6	+SDR Bit 6 FL	4-16 A4		4-62 C4
E		+OPR Decode E	4-18 E6	—Reset Condition	4-04 C3	+SDR Bit 7 FL	4-16 A4		4-62 E8
* From WC361		+OPR Decode F	4-18 E6	+Reset Condition	4-04 C3	+SDR Bit 8 FL	4-16 A4	+Sense Bit 12	4-54 C9
** Logic Page A7052		+OPR Decode 0	4-18 E6	—Reset Current PL	4-32 C6	+SDR Bit 9 FL	4-16 A4		4-62 C8
*** From WC251		+OPR Decode 1	4-18 E6	—Reset Cycle FL's	4-24 E7	+SDR Bit 10 FL	4-16 A4		4-62 D8
† From WC541		+OPR Decode 2	4-18 E6	—Reset Error Latches	4-39 B7	+SDR Bit 11 FL	4-16 A4		4-62 C4
†† From WC21		+OPR Decode 3	4-18 E6	—Reset FDR	4-46 C5	+SDR Bit 12 FL	4-16 A4		
††† From PSWC221		+OPR Decode 4	4-18 E6	—Reset LC FL's	4-24 C6	+SDR Bit 13 FL	4-16 A4		

2		3		4		5		6		7		8		9	
	+Sense Bit 13	4-54 C9	+Shift Unit Bit 4	4-42 D9	—Storage Test	4-39 D2	+TDR 0-7 to SU 8-15	4-40 B6	—X Addr 2	4-34 A6
		4-62 D8	+Shift Unit Bit 5	4-42 D9	+Storage Test Store	4-16 D3	+TDR 8-15 to SU 0-7	4-40 B6	—X Addr 3	4-34 A6
		4-62 C4	+Shift Unit Bit 6	4-42 D9	—Storage Test Store	4-16 D3	+TDR 8-15 to SU 8-15	4-40 A6	—X Addr 4	4-34 A6
		4-62 C8	+Shift Unit Bit 7	4-42 D9	—Storage Test Sw INT	4-57 E8	+Terminate Store Test	4-04 B6	—X Addr 6	4-34 B6
	+Sense Bit 14	4-54 C9	+Shift Unit Bit 8	4-42 D9	+Storage Use	4-10 E5	+Test Packet Byte	4-32 C3	—X Addr 7	4-34 A9
		4-62 C8	+Shift Unit Bit 9	4-42 D9	+Storage Use FL	4-10 E5	Time Sharing Sw	4-01 C8	+X Address Check FL	2-02 C8
A		4-62 D8	+Shift Unit Bit 10	4-42 C9	+SU Bit P0	4-52 D6	+Time 1 FL	4-02 C6	—X Address Error	2-02 C7
		4-62 C4	+Shift Unit Bit 11	4-42 C9	+SU Bit P1	4-52 A6	—Time 1 FL	4-02 C6	—X Address Selected FL	2-02 C8
	+Sense Bit 15	4-32 C3	+Shift Unit Bit 12	4-42 C9	+SU or INH Check	2-06 E9	+Time 2 FL	4-02 C6	—X Address 0	4-34 D9
		4-54 C9	+Shift Unit Bit 13	4-42 C9	+Sum Bit 0	4-48 D8	—Time 2 FL	4-02 C6	+X Address 0, 1, 2 or 3	2-02 C7
		4-62 C4	+Shift Unit Bit 14	4-42 C9	+Sum Bit 1	4-48 C8	+Time 3 FL	4-02 D6	—X Address 2	4-34 D9
		4-62 D8	+Shift Unit Bit 15	4-42 C9	+Sum Bit 2	4-48 C8	—Time 3 FL	4-02 D6	—X Address 3	4-34 E9
▶		4-62 C8	—Shift Unit Check FL	2-06 D9	+Sum Bit 3	4-48 C8	—Time T8 not Mod Check	4-38 C3	—X Address 4	4-34 E9
	—Sense Bit 8-15 Even	4-62 D9	+Shift Unit Check FL	2-06 D9	+Sum Bit 4	4-48 D6	+To REG Decode 0	4-18 D9	+X Address 4, 5, 6, or 7	2-02 C7
	—Sense Bits P0-15 Ext	4-16 A3	—Shift Unit 0-7 Odd Parity	2-06 C2	+Sum Bit 5	4-48 C6	+To REG Decode 1	4-18 D9	—X Address 5	4-34 E9
	—Sense Bits 8-15 Even	2-06 B7	—Shift	4-42 E5	—Sum Bit 5	4-48 C9	+To REG Decode 2	4-18 D9	—X Address 6	4-34 E9
	—Sense CS Request	4-64 A2	—Shift Unit 8-15 Odd Parity	2-06 C2	+Sum Bit 6	4-48 C6	+To REG Decode 3	4-18 D9	—X Address 7	4-34 E9
	+Sense Strobe 4K	4-12 B4		4-42 D5	—Sum Bit 6	4-48 C9	+To REG Decode 4	4-18 D9	X Read Gate Time	4-12 B7
	+Sense Strobe 8K	4-12 B4	Short Time FL	4-12 B3	+Sum Bit 7	4-48 C6	+To REG Decode 5	4-18 D9	X Read Source	4-12 B7
B	+Sense Trap Request Lines	4-32 A3	+Sign E	4-42 A2	—Sum Bit 7	4-48 C9	+To REG Decode 6	4-18 D9	X Write Driver Time	4-12 B7
	+Set ALU to LS	4-30 B3	+Sign Position FL	4-32 D2	+Sum Bit 8	4-48 D6	+To REG Decode 7	4-18 D9	X Write Sink	4-12 B7
	+Set Carry Latch	4-54 A6	—Single Cycle Sw INT	4-57 E8	+Sum Bit 9	4-48 C6	+To REG Select CY0	4-34 C5	+XX Type	4-18 C8
	+Set CC and Carry	4-54 A4	—Single Instruction Mode INT	4-01 C8	+Sum Bit 10	4-48 C6	+To REG Select T5	4-34 D5		4-36 A3
	+Set CC Latches	4-54 B6	—Single Microinstr Sw INT	4-57 E8	+Sum Bit 11	4-48 C6	+To REG Select T7	4-34 D5	—XX Type	4-39 B2
	+Set CC0	4-54 B6	+SIOC Indicator	4-60 D9	+Sum Bit 12	4-48 D5	+To REG Select T8	4-34 D4		
▶	+Set CC2	4-54 D6	+Six Corr Bit 8-11	4-48 B4	+Sum Bit 13	4-48 C5	+To REG Select	4-34 D6		
	+Set Current PL	4-32 B6	+Six Corr Bit 12-15	4-48 A4	+Sum Bit 14	4-48 C5	+To REG Select Freeze FL	4-59 B5	+Y Address Check FL	2-02 B8
	—Set FDR Bit P0	4-46 D4	—Skip CY2 to CY1	4-24 A9	+Sum Bit 15	4-48 C5	+Trap Request 1	4-32 B3	—Y Address Error	2-02 B7
	—Set FDR Bit P1	4-46 D4	—Skip CY2 to CY2	4-24 A9	+Sum Bit P0	4-52 D8	+Trap Request 2	4-32 B3	+Y Address Gate 1	4-30 E7
	—Set FDR Bits 0-7	4-46 D4	—Skip CY3 to CY1	4-24 A9	+Sum Bit P1	4-52 C8	+TRBS and CY0	4-52 B2	+Y Address Gate 2	4-30 E7
	—Set FDR Bits 8-15	4-46 D4	—Skip CY3 to CY3	4-24 A9	+Sum Bits 0-7 EOR P0	4-52 D8	—TRBS and CY0	4-40 A5	—Y Address Selected	2-02 A8
	+Set I/O Bus to LS	4-30 A3	—Skip CY0 to CY2	4-24 B4	+Sum Bits 0-7 Even	4-52 E7	—Turn Off FDR Bit P0	4-52 E8	Y Read Gate Time	4-12 B7
C	+Set LC	4-24 C6	—Skip CY0 to CY3	4-24 B4	+Sum Bits 8-15 EOR P1 Even	4-52 C8	—Turn Off FDR Bit P1	4-52 D8	Y Read Source	4-12 B7
	—Set LOG REG 1	4-22 D2	—Skip CY1 to CY3	4-24 B4	+Sum Bits 8-15 Even	4-52 C7	+Turn On Stop Light	4-04 D9	Y Write Driver Time	4-12 B7
	—Set LS to MAR Delta CY2	4-38 B2	—Skip CY3 to CY1	4-24 A9	—Suppr Odd SU Bits 8-11	4-52 C4	+T1	4-02 B9	Y Write Sink	4-12 B7
	+Set LS Write T7	4-36 C5	Source Selection of LS Zone (Y—)		+Suppr SU Bit 0-3	4-44 D6	—T1	4-22 E4		
	+Set LS Write T8	4-36 E6	Addresses	4-32 C5	—Suppr SU Bit 0-7	4-44 D4	+T1 Delayed	4-22 E4		
	+Set MAR	4-38 B4	+ST DASF	4-20 B7	+Suppr SU Bit 4-7	4-44 C6	+T2	4-02 B9	+1442 Indicator*	4-01 A7
▶	—Set Modifier Check Latch	2-04 E7		4-20 C7	+Suppr SU Bit 8-11	4-44 C6	+T3	4-02 B9	+20V Rem Reset Key N/O	4-57 C9
	+Set OPR	4-18 C3		4-20 D7	+Suppr SU Bit 8-9	4-44 B6	+T4	4-02 B9	+20V Rem Stop Key N/O	4-57 C9
	+Set OPR Gate	4-18 C3	—ST Fill or Alter not CE Mode	4-20 C7	+Suppr SU Bit 10-11	4-44 B6	+T4-T7	4-02 A9	+20V Storage Protect RY6-2 N/O††	4-10 E3
	—Set Process Meter	4-62 B4	+ST Disalt or CE Reg Disalt	4-20 D7	+Suppr SU Bit 12-13	4-44 A6	+T4-T7 not Delta CY0	4-39 D3	+2501 Indicator*	4-01 A6
	+Set Reset LC	4-24 C6	+ST Test	4-20 C7	+Suppr SU Bit 12-15	4-44 C6	+T5	4-02 B9	+2520 or 2560 Indicator*	4-01 A6
	—Set Reset LC	4-24 C6	+Start FL	4-04 A4	+Suppr SU Bit 14-15	4-44 A6	+T6	4-02 B9	+3V Missing Phase†††	2-01 A7
	—Set Up Run Condition	4-04 A6	—Start FL and ST Interlock FL	4-04 A5	—Suppr 0-7 and not Inv Par	4-52 D4	—T6	4-54 B4	+3V or —3V Lamp Common	4-57 D2
D	+Set Up Run Condition Gate	4-04 A6	—Start Interlock FL	4-04 A5	—Suppr 8-15 and not Inv Par	4-52 A4	+T6 and Any CS Request	4-62 C7		
	Shift by 2 or 4	4-42 B6	—Start Key INT	4-01 E5	+Sync Cond 1	4-58 E9	+T7	4-02 B9		
	—Shift By 8	4-40 A5	+Start Key INT	4-01 E5	—Sync Cond 1	4-58 E7	+T7 and Any CS Request	4-62 C7		
	+Shift Left by 2	4-42 C3	+Start Keys	4-04 A3	+Sync Cond 2	4-58 E9	+T8	4-02 B9		
	+Shift Left by 4	4-42 B2	+Stop FL	4-04 D7	—Sync Cond 2	4-58 E7	+T8 or T2	4-34 C4		
	+Shift or MVH or MVB	4-34 D5	—Stop Key INT	4-01 E5	+Sync Pulse	4-58 C8	+T8-T3	4-02 A9		
	+Shift Right by 2	4-42 C3	+Stor Scan or Display	4-20 C7	—System or Check Reset	2- 2 D9	+T8-T3 not Delta CY0	4-39 D3		
▶	+Shift Right by 4	4-42 C3	—Stor Scan or Fill	4-20 C7	+System Reset Key INT	4-01 E5				
	+Shift Unit Bit 0	4-42 D9	—Store Test Load	4-24 D9	—System Reset Key INT					
	+Shift Unit Bit 1	4-42 D9	+Stor Use Delayed FL	2-01 A3	+System Reset Pulse	4- 4 B3	+Unequal PL	4-32 E8		
	+Shift Unit Bit 2	4-42 D9	—Stor Use Delayed FL	2-01 B3			+Unequal PL Freeze FL	4-59 C5		
	+Shift Unit Bit 3	4-42 D9	—Storage Alter Mode INT	4-01 D8			—Up Addr Check FL	4-39 A9		
			—Storage Display Mode INT	4-01 D8	TDR	4-40 D6	+Update LC	4-24 A4		
E			—Storage Fill Mode INT	4-01 D8	+TDR Bit 0 to 3 FLs	4-40 D6	+Update LC and Auto LC	4-24 A4		
	* From WC361		—Storage MANOP not Test	4-16 E3	+TDR Bit 4 to 7 FLs	4-40 D6				
	** Logic Page A7052		+Storage MANOP not Test	4-16 E3	+TDR Bit 8 to 11 FLs	4-40 C6	+Write Cycle	4-02 C9		
	*** From WC251		+Storage Protect RY6-2 N/O	4-10 E4	+TDR Bit FLs P0, 0-7, P1, 8-15	4-40 E6				
	† From WC541		—Storage Scan Mode INT	4-01 D8	+TDR Bit 12 to 15 FLs	4-40 C6				
	†† From WC21		+Storage Select	4-02 C5	—TDR to Display Sw	4-22 C7	—X Addr 0	4-34 A4		
	††† From PSWC221		—Storage Test	2-04 C6	+TDR 0-7 to SU 0-7	4-40 A6	—X Addr 1	4-34 C4		



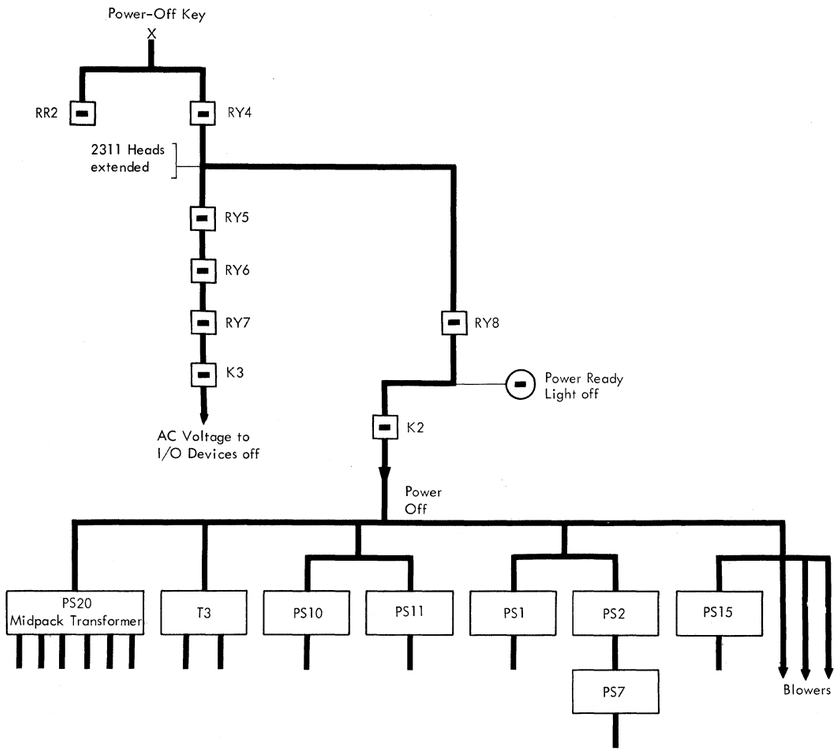
Notes:
1. PS2 is installed only when 2311 Disk Storage Drive and/or 2152(TW) is attached.
2. PS7 is installed only when 2311 is attached

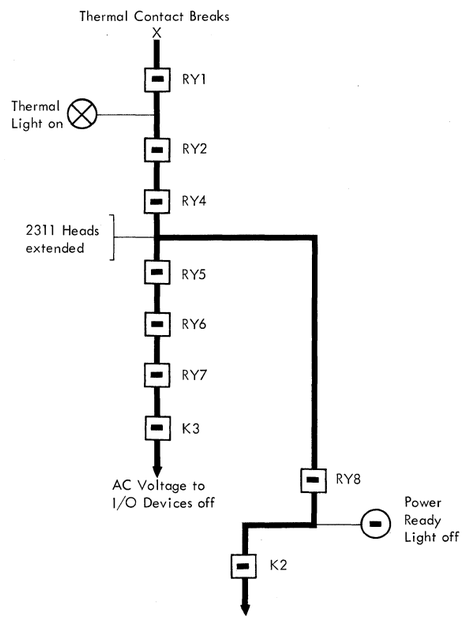
Diagram 6-1. Power-On Sequence, 50 Hz Power Supply (04014) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

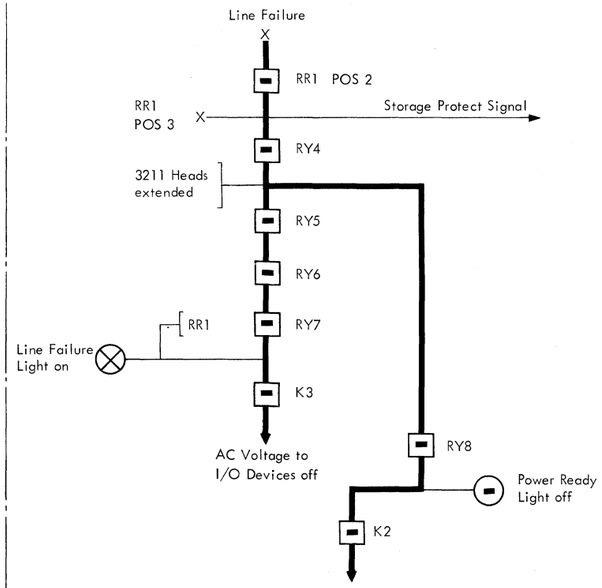


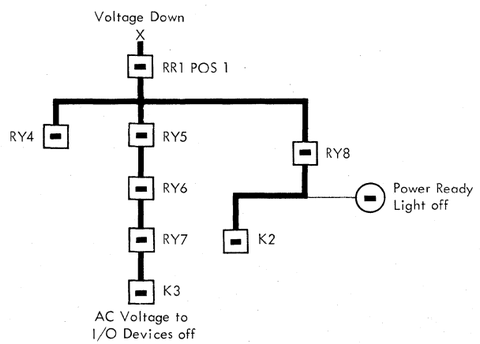
Notes:
1. PS2 is installed only when 2311 Disk Storage Drive and/or 2152 (TW) is attached.
2. PS7 is installed only when 2311 is attached

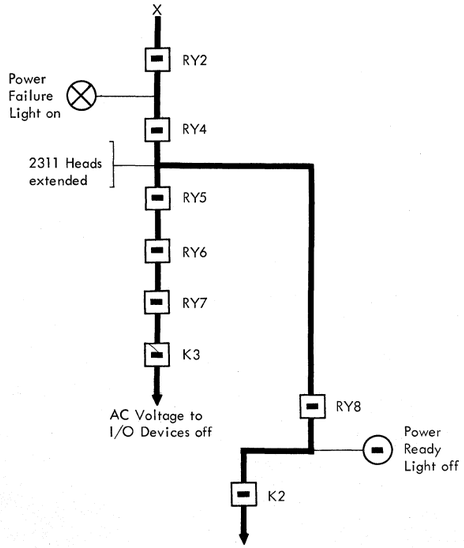
Diagram 6-5. Power-On Sequence, 60 Hz Power Supply (04015) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

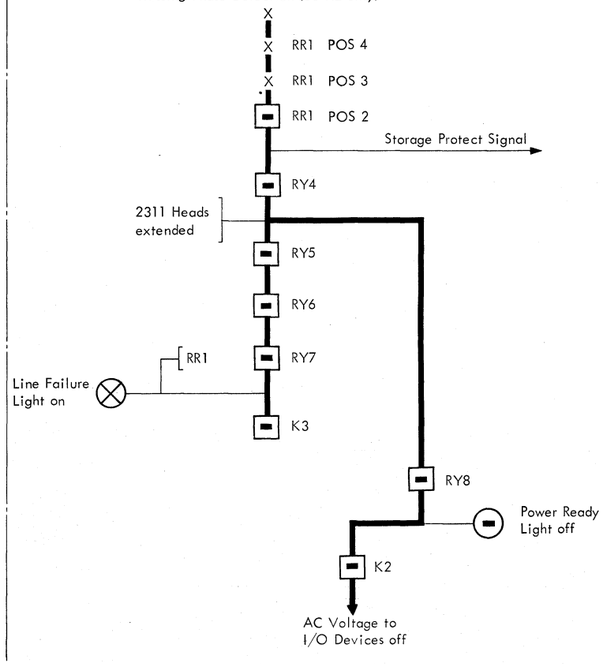












Legend

X Activated Relay

Deactivated Relay

Activated Light

Deactivated Light

Diagram 6-10. Power-Off Sequences, 50 and 60 Hz Power Supplies (04016) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

Label	Reference Diag	Reference Co-ord	Remarks
AASPCR	-	-	See QJH 030
ABADR	-	-	Constant in storage
ABSCR	-	-	See QUH 020
ACBIN	-	-	See BINPH
ACDP 60	-	-	See QVW 010
ACELG	-	-	See DLPROG
ACHKS	-	-	Address of check sum
ACLFL 1	-	-	See QYH 020
ACLFL 2	-	-	See QRH 010
ACLFL 3	-	-	See QYK 020
ACNORM	-	-	See NORMPH
ACT 0	B-49	B2	
ACT 2	B-49	B3	
ACT 3	B-49	C4	
ACT 4	B-49	B5	
ACT 6	B-49	B6	
ADCH	B-37	B2	
ADDRSW	-	-	Address 0014
ADP	B-33	B4	
ADR	-	-	Constant in storage
ADRESS	-	-	Constant in storage
AD2F0	B-37	D4	
AEND 01	-	-	See QYH 030
AEND 20	-	-	See QRH 060
AEND 42	-	-	See QYK 040
AENTRY	-	-	See ENTRY
AFIL 1	-	-	See QMH 020
AFIL 2	-	-	See RETPL 1
AHAR	B-25	C2	
AHARP 2	B-25	D3	
AINTB	-	-	See RPQINB
AINTE	-	-	See QWH 020
AINTP	-	-	See QYP 060
AINTRD	-	-	See QHN 070
AINTX	-	-	Constant in storage
AINT 0	-	-	See RPQIN 0
AINT 7	-	-	See QPH 020
AINT 8	-	-	See QMH 030
AIOCR 1	-	-	See QPH 030
AIPH	-	-	See IP
AIPHAS	-	-	See IPHASE
AIPHS	-	-	See IP
AIRPT	-	-	See INTRPT
AIST	-	-	See IST
AKEY	-	-	See TOTCHK
ALENG	-	-	Text length field
ALGHD	-	-	See LOGHND
ALOAD	-	-	Load address (Col 7)
ALOG	-	-	Address /C1E0/
ALTER	B-13	D4	
AMACS	-	-	See QHK 010
ANDIF 0	B-43	C7	
ANDIOF	B-41	B6	
AND 42	B-23	C3	
ANOTOP	-	-	See QJH 100
AOVERR	-	-	Address /0054/
AP	B-33	B5	
APCH 20	-	-	See QRH 041
APCH 42	-	-	See QYP 070
APL 1	-	-	See RETPL 1
APRCHK	-	-	See PRGCHK
AREAD	-	-	See RDAREA
ARECAL	-	-	See IRECAL
ARESET	-	-	See CLRLS
ARPQL 2	-	-	See RPQL 2
ASCAN	-	-	See QSH 040
ASENS	-	-	Constant in storage
ASPCER	-	-	See SPECER
ASPSW	-	-	See SPSW 1
ASR	B-25	B5	
ATYPE	-	-	Card type (Col 3)

Label	Reference Diag	Reference Co-ord	Remarks
ATYPRQ	-	-	See QWH 030
AUNPK 3	-	-	See UNPK 3
AUXL	-	-	See BUFFER
AVAIL	-	-	See QJH 070
AVL	B-35	D8	
AXCC	-	-	See IPHASE
AXCC 1	-	-	See IPHASE
AXL	-	-	See BUFFER
AXL 2	-	-	See BUFFER
BAS	B-25	C4	
BASP 2	B-25	C4	
BEGIN	B- 7	B3	
BINPH	-	-	See 2560,2501,1442 Atch FEMDM*
BRADR	-	-	Constant in storage
BRTOL 1	-	-	Branch table in storage
BUFFER	-	-	16 bytes in storage
BUSCHK	B-35	B6	
BZ0P	B-45	A6	
CCDE	-	-	Constant in storage
CCLOOP	B-15	D2	
CCODE	-	-	Address /0010/
CCOVFL	B-33	B9	
CCSET	B-39	D3	
CCTAB	-	-	CC translation table
CD	-	-	See CCDE
CDFAST	-	-	See 2560,2501,1442 Atch FEMDM*
CH	B-25	C7	
CHSTAT	-	-	Address /0011/
CHKSUM	-	-	Hash total field
CIO	B-35	A6	
CIOI	-	-	See CIO
CLC	B-31	B4	
CLRLS	B- 7	A3	
CNT	-	-	Constant in storage
COLOG 2	B-51	A5	
COUNT	-	-	Constant in storage
COUNT 7	B-51	C2	
CP	B-33	A6	
CT1	B-55	B6	
DATAD 1	-	-	Two bytes in storage
DATASW	-	-	Address /0013/
DATERR	B-37	B6	
DBUF	-	-	Address of auxiliary area
DECCNT	B-39	B3	
DECODE	B-29	D3	
DEL 1	B-51	A8	
DEL 2	B-51	C8	
DEL 3	B-51	D8	
DEPINS	-	-	See 2560,2501,1442 Atch FEMDM*
DIAGTB	-	-	See ACT 0
DIGSEL	B-29	A6	
DIVCHK	B-39	B2	
DLPROG	-	-	See QJH 220
DLPR 2	-	-	See APL 1
DLPR 9	B-51	B2	
DLPR 11	-	-	See QRH 100
DLPR 14	B-51	B3	
DP	B-39	A3	
DPI	-	-	See DP
DPLOOP	B-39	D3	
DSPM	B-33	A8	
DSZ	B-33	A8	
DVFLW	B-33	A9	
ED	B-29	A3	
ENDCD	B-59	B6	
ENDEDT	B-29	D5	
ENDTST	B-37	D5	

Label	Reference Diag	Reference Co-ord	Remarks
ENTRY	-	-	Address /0108/
ER	-	-	See PROGER
ERROR	-	-	See PROGER
ERROR 1	B-59	A3	
EXECT	B-7	B3	
EXCEPT	B-15	A2	
EXC 0	B-15	B2	
EXC 1	B-15	B2	
FCP	B-33	C9	
FETCH	B-17	B2	
FILL	B-29	A4	
FRD	B-37	E5	
FRDI	-	-	See FRD
GETBYT	B-37	C5	
HPR	B-15	C2	
HPRI	-	-	See HPR
IAR	-	-	See MPIAR
INTRPT	B-17	A2	
INT 6	B-17	D5	
INT 15	B-17	D5	
INVOP	B-15	A7	
INVOPI	-	-	See INVOP
INVRG	B-25	B9	
INVRG 1	-	-	See INVRG
INVX	B-23	B8	
IOTRB	-	-	Branch table in storage
IP	B-19	B3	
IPACKI	-	-	See IPPACK
IPASR	B-25	A9	
IPBASR	B-23	A3	
IPBC	B-23	A7	
IPBCR	B-23	A5	
IPCLI	B-31	B6	
IPDC11	-	-	See IPZCAS
IPDIAG	B-49	A4	
IPDIAI	-	-	See IPDIAG
IPHASE	-	-	See QJH 020
IPMDI	-	-	See IPMPDP
IPMPDP	B-37	A3	
IPMVO	B-41	A3	
IPMVOI	-	-	See IPMVO
IPPACK	B-45	A4	
IPRX	B-25	A5	
IPSI	B-35	A4	
IPSPSI	-	-	See IPSPSW
IPSPSW	B-47	A2	
IPSS	B-27	A3	
IPSSI	-	-	See IPSS
IPT	-	-	Address /0060/
IPTM	B-31	B2	
IPUNPI	-	-	See IPUNPK
IPUNPK	B-43	A3	
IPZCAS	B-33	A3	
IRECAL	-	-	Constant in storage
IST	-	-	Sense table in storage
KD2	B-51	B2	
KEY 1	-	-	Two bytes in storage
KEY 2	-	-	Two bytes in storage
L	-	-	Constant in storage
L2	-	-	Constant in storage
LACHAR	-	-	See 2560,2501,1442 Atch FEMDM*
LBIZON	B-43	B5	
LGEND	-	-	Address /C27F/
LEVEL 0	-	-	See QJH 060
LEVEL 1	-	-	See QJH 140

Label	Reference Diag	Reference Co-ord	Remarks
LEVEL 2	-	-	See QJH 160
LEVEL 5	-	-	See 2560,2501,1442 Atch FEMDM*
LH	B-25	C5	
LMVO	B-41	B4	
LOGAR	-	-	Log area in storage
LOGHND	B-9	A2	
LOOPST	B-29	B4	
LPACK	B-45	A7	
LPTR	B-27	B5	
LUNPK	B-43	C5	
LVLADR	-	-	See QMH 050 STCL Atch FEMDM*
MACIAR	-	-	Two bytes in storage
MANRT	B-13	A2	
MIAR	-	-	Constant in storage
MODESW	-	-	Address /0012/
MOVELP	B-37	B5	
MPIAR	-	-	Constant in storage
MPLP	B-37	D4	
MV	B-33	B6	
MVB45I	B-41	D3	
MVC	B-27	A8	
MVI	B-35	C3	
MVLP	B-39	A3	
MVN	B-27	C2	
MVN2T6	B-33	C8	
MVZ	B-27	C3	
NEWADR	B-39	B4	
NEW 1	B-51	B2	
NEW 2	B-51	C2	
NEW 3	-	-	See QJH 230
NI	B-35	B2	
NOLACH	-	-	See 2560,2501,1442 Atch FEMDM*
NORMPH	-	-	See 2560,2501,1442 Atch FEMDM*
NORUN	-	-	Address /0011/
NOSIGN	B-37	C5	
NOSPER	B-37	A5	
NOTOP	-	-	See QJH 100
NS	B-39	D3	
OI	B-35	C4	
OPTB	B-19	C2	
OR 14	B-29	C7	
OUT	B-29	D5	
OUT 7	-	-	See QJH 150
OFLOW	-	-	See 2560,2501,1442 Atch FEMDM*
OVRUN	-	-	See 2560,2501,1442 Atch FEMDM*
PACK 1	B-45	A5	
PL2TAB	-	-	Branch table in storage
PL2TB2	-	-	Branch table in storage
PL3	-	-	See QSH 020
PL4	-	-	See QUH 030
PL6	-	-	See QMH 050
PL7TRB	-	-	Branch table in storage
PLRST	-	-	See 2560,2501,1442 Atch FEMDM*
PRGCHK	B-15	A6	
PRGCL 1	-	-	See QJH 180
PRGERR	-	-	See PROGER
PROGER	-	-	See QJH 040
PRSEL 1	-	-	See DLPR 2
PRTRAP	B-11	B2	
QHK 010	-	-	Constant in storage
QHN 020	-	-	Two bytes in storage
QHN 050	-	-	Constant in storage
QHN 070	-	-	One byte in storage
QHSA	-	-	128 bytes in storage
QHS 000	-	-	See LEVEL 5 start address
QHS 010	-	-	See DATAD 1

*See Preface for appropriate Form Number

Label	Reference Diag	Reference Co-ord	Remarks
QHS 020	B-57	B3	
QHS 030	-	-	See SPHADX
QHS 040	-	-	See SRREAD
QHS 050	-	-	See SIOC FETMDM*
QHS 060	-	-	See SIOC FETMDM*
QHS 070	-	-	Two bytes in storage
QJHA	-	-	See OPTB
QJH 010	B-19	A3	
QJH 020	B-19	B3	
QJH 030	B-15	D6	
QJH 040	B-15	D6	
QJH 050	B-15	A4	
QJH 060	B-21	A2	
QJH 070	B-35	A8	
QJH 080	B-35	E6	
QJH 090	B-35	D6	
QJH 100	B-35	D5	
QJH 110	B-47	B2	
QJH 120	-	-	See TYPI
QJH 130	B-55	C4	
QJH 140	B-55	A4	
QJH 150	B-11	C4	
QJH 160	B-11	A2	
QJH 180	B-51	A8	
QJH 190	B-51	A8	
QJH 200	B-51	B8	
QJH 220	B-51	A3	
QJH 230	B-51	C2	
QJH 240	-	-	Address /C102/
QJH 250	-	-	Translate table in storage
QJH 260	-	-	Address /C12C/
QJH 270	-	-	Address /C13E/
QJH 280	-	-	Address /C118/
QJH 290	-	-	Two bytes in storage
QJH 300	-	-	Two bytes in storage
QJH 310	B-51	A4	
QJH 320	B-51	A5	
QJH 330	B-51	A6	
QJH 340	B-51	A6	
QJH 350	-	-	Address /C122/
QJH 360	-	-	Two bytes in storage
QJH 370	-	-	Two bytes in storage
QMH 020	B-55	B2	
QMH 030	-	-	See STCL FEMDM*
QMH 050	-	-	See STCL FEMDM*
QPH 020	-	-	See IOC FEMDM*
QPH 030	-	-	See IOC FEMDM*
QRH 010	-	-	See 2560,2501,1442 Atch FEMDM*
QRH 041	B-11	B3	
QRH 060	B-11	B4	
QRH 100	B-51	B3	
QSH 020	-	-	See 1403 Atch FEMDM*
QSH 030	-	-	See 1403 Atch FEMDM*
QSH 040	-	-	See 1403 Atch FEMDM*
QUH 020	B-55	C6	
QUH 030	-	-	See BSCA FEMDM*
QVW 010	B-11	B2	
QWH 020	-	-	See 2152 Atch FEMDM*
QWH 030	B-11	B5	
QYH 020	-	-	See 2560,2501,1442 Atch FEMDM*
QYH 030	B-11	B4	
QYK 020	-	-	See 2560,2501,1442 Atch FEMDM*
QYK 040	B-11	B5	
QYP 060	-	-	See 2560,2501,1442 Atch FEMDM*
QYP 070	B-11	B3	
RCOLBN	-	-	See 2560,2501,1442 Atch FEMDM*
RDAREA	-	-	Address /00A0/
RDCHK	-	-	See 2560,2501,1442 Atch FEMDM*
READ	B-59	B3	
READ 1	B-59	C2	

Label	Reference Diag	Reference Co-ord	Remarks
REPEAT	-	-	See QJH 010
RESCNT	-	-	See SIOC FETMDM*
RETPL 1	-	-	See QJH 130
RETPL 2	-	-	See QJH 150
RETPL 7	-	-	See QHS 020
RPQINB	-	-	Reserved for RPQ
RPQIN 0	-	-	Reserved for RPQ
RPQL 2	B-11	B6	
RREAD 1	-	-	See 2560,2501,1442 Atch FEMDM*
RSET	B-9	A5	
RXTB	-	-	Op code table in storage
SCAN	B-17	A3	
SCAN 1	B-17	B3	
SCHEQ 1	B-57	B4	
SCNDGT	B-29	A7	
SDSAC	B-33	C3	
SENSE	B-17	D2	
SENS 3	B-11	A2	
SETCC	-	-	See QJH 080
SETPT	B-59	D2	
SETSGN	B-37	E5	
SGN	B-39	D4	
SHSR	B-25	C3	
SIGN	-	-	Constant in storage
SIGNQ	-	-	Constant in storage
SIGNR	-	-	Constant in storage
SIGNST	B-29	A8	
SLM 444	B-41	A4	
SNSREQ	-	-	See 2560,2501,1442 Atch FEMDM*
SP	B-33	A5	
SPCERR	B-37	D3	
SPECER	-	-	See QJH 030
SPES	-	-	See SPECER
SPHADD	-	-	Constant in storage
SPHADX	-	-	Constant in storage
SPHAD 4	-	-	Constant in storage
SPHAD 6	-	-	Constant in storage
SPSW	-	-	See QJH 110
SPSW 1	B-47	C2	
SRREAD	-	-	Constant in storage
SSTB	-	-	SS and SI op code table
START	B-29	A4	
STH	B-25	C6	
STOP	-	-	See QJH 050
STOP 1	B-59	C6	
STORE	B-29	B4	
STPSW	B-17	A5	
STRGR	B-29	C8	
SUBR	-	-	See QJH 200
SUBR 1	-	-	See QJH 190
SUBR 3	B-51	C8	
TABLE	-	-	CC and op code table
TESTFL	-	-	See 2560,2501,1442 Atch FEMDM*
TEXCPT	B-59	A6	
TIOB	B-35	B6	
TIOBI	-	-	See TIOB
TMODE	B-13	D3	
TOADR	-	-	Address /0178/
TOTCHK	-	-	Two bytes in storage
TR	B-27	A5	
TSTDGT	B-29	B7	
TSTZON	B-7	C3	
TXTCD	B-59	B5	
TYPI	-	-	Constant in storage
UNPK 1	B-43	B7	
UNPK 2	B-43	C7	
UNPK 3	B-43	D7	

Label	Reference Diag	Reference Co-ord	Remarks
WAIT	B-35	B8	
WORKIN	-	-	See QJH 090
WRKLP	B-59	C2	
XCC	-	-	See EXCEPT
XCCA	-	-	See IPHASE
XCCB	-	-	See IPHASE
XCCBA	B-41	C6	
XCCBAA	-	-	See XCCC
XCCC	-	-	See IPHASE
XCCD	-	-	See IPHASE
XCCI	-	-	See EXCEPT
XIO	B-35	A6	
XIOI	-	-	See XIO
YENTR	-	-	See QSH 030
ZAP	B-33	A7	

*See Preface for appropriate Form Number

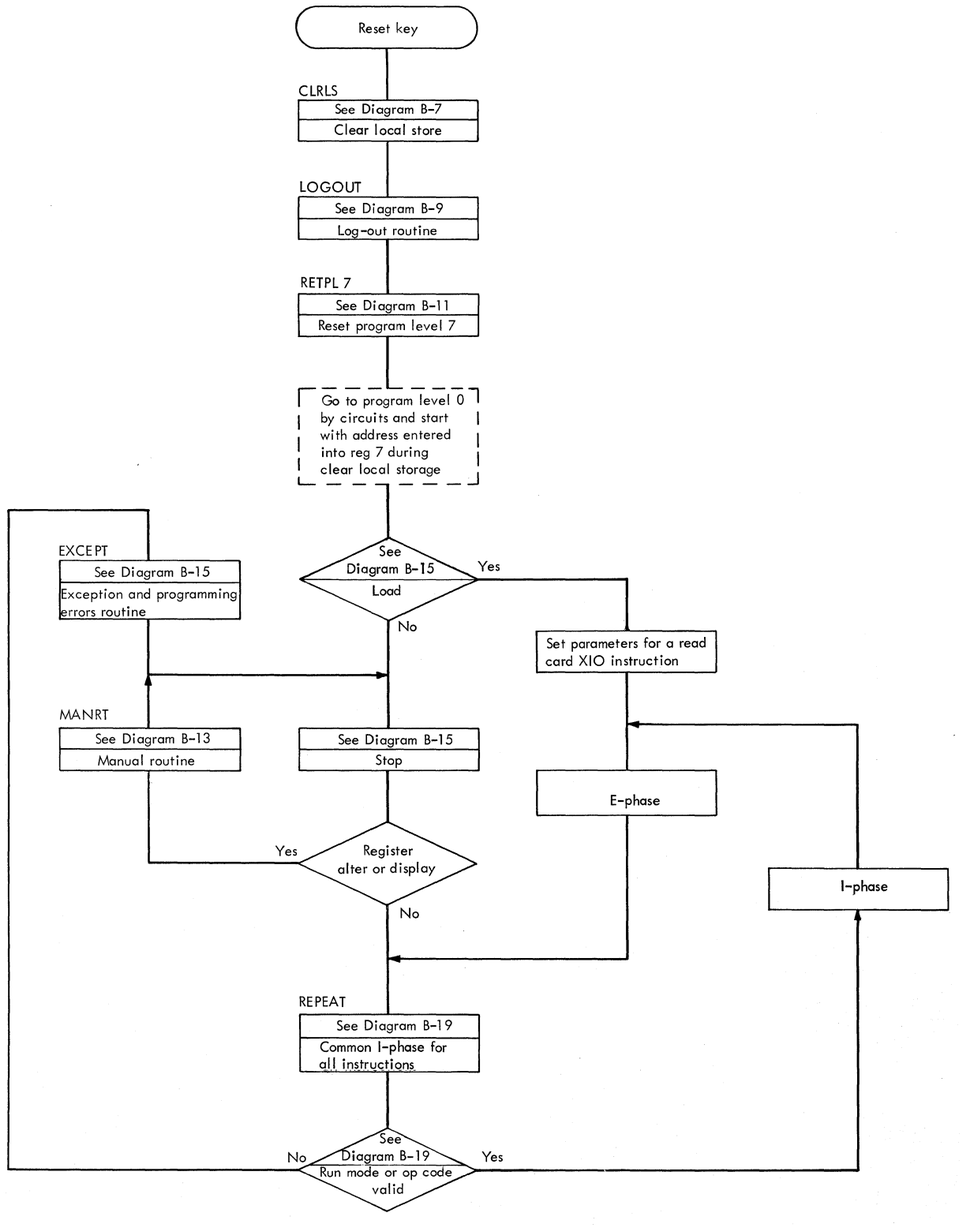
A

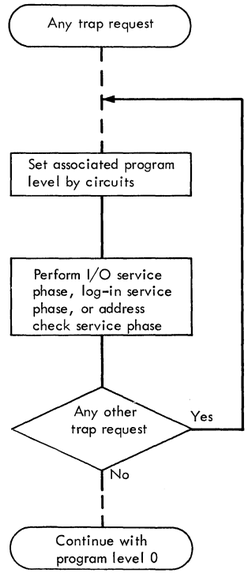
B

C

D

E


Reset key
CLRLS
See Diagram B-7
Clear local store
LOGOUT
See Diagram B-9
Log-out routine
RETPL 7
See Diagram B-11
Reset program level 7
Go to program level 0 by circuits and start with address entered into reg 7 during clear local storage
See Diagram B-15 Load
Yes
No
EXCEPT
See Diagram B-15
Exception and programming errors routine
Set parameters for a read card XIO instruction
MANRT
See Diagram B-13
Manual routine
See Diagram B-15
Stop
E-phase
Yes
Register alter or display
No
I-phase
REPEAT
See Diagram B-19
Common I-phase for all instructions
See Diagram B-19 Run mode or op code valid
No
Yes


Any trap request
Set associated program level by circuits
Perform I/O service phase, log-in service phase, or address check service phase
Any other trap request
Yes
No
Continue with program level 0

/00XY/

	0 1	2 3	4 5	6 7	8 9	A B	C D	E F
0	GPR 0 /0000/	Special Engineering RPQ DA0 *	GPR 1 /1000/	Address of 2501 QYH 010 If not attached /0088/	GPR 2 /2000/	Address of 2520/2560 QRH 020 *	GPR 3 /3000/	Address of 1442 QYK 010 *
1	GPR 4 /4000/	Address of 1403/2203 QSH 010 *	GPR 5 /5000/	Address of BSCA QUH 010	GPR 6 /6000/	Address Serial I/O Channel QXH 010 *	GPR 7 /7000/	Address of I/O Channel QPH 010 *
2	GPR 8	Address of Storage Control QMH 010 *	GPR 9	Address to Common I-Phase QJH 020	GPR A	Address to Common I-Phase QJH 030 *	GPR B	Special Engineering RPQ DAB *
3	GPR C	Address to Common I-Phase QJH 020	GPR D	Address to Common I-Phase QJH 020	GPR E	Address of 2152 QWH 010 *	GPR F	Test Overlap Mode TIOB /008A/
4	IOC Work Area							
5	Interference Number	Special Engineering	Overrun Indicator for Card Read	Print Head Select Parameter	2520 Auxiliary Last Card Indicator	Carriage Control Field	2501 Auxiliary Last Card Indicator	Detailed Log Switch
6	Interrupt Priority Table: SIOC Read; 2501 Read; 2520 2560 Read; 1403 2203 Print; BSCA; 2560 Punch; 1442 Punch; 2560 Card Print; 2560 Punch; Special Engineering; I/O Channel; Storage Control							
7	Interrupt Priority Table: Special Engineering; 2152 Read Write; 2152 Inquiry; /FF/ End of IPT; Intermediate Read Area for Log: /F0/ EBCDIC ASCII; Read Buffer; Equal Compare; Field Length							
8	1st Halfword of Instruction Op-Code	Instruction Recall-Address	Current PSW 0-15	Current PSW 16-31	Switch DA 1 to 2 Branch to address shown in pos: /000B/	Program Portion: Test, if TIOB /3080/	If yes, move Branch Address /A463/	Branch to address shown in pos: /0037/

General Purpose Registers 1 through 7 must not be used by customer.

If I/O is attached symbolic address points to entry of appropriate micro-program section. For an I/O which is not attached, the contents of halfword is 008E.

For additional information see section "QHNA" C01 Binder, Pages 13-15

Cycle Steal	Priority Table
Device One	STCL
Device Two	RPQ
Device Three	IOC
Device Four	BSCA

• Figure B-5. Protected Area and Control and Sense Tables (Part 1 of 2) (04782)

CTRL and SENS TABLES

CTRL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
10	-	-	-	-	-	-	-	-	-	Dev addr 15 inter-rupt FL	Set/reset bit 9	Carry FL	CC0 FL	CC1 FL	CC2 FL	CC3 FL
11	-	-	-	-	-	-	-	-	-	Det log request FL	Set/reset bit 9	Set channel end	Not set/ not reset bits 14-15	-	USASCII FL	Channel Mask FL

SENS	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
10	-	-	-	-	-	-	-	-	-	-	-	Carry FL	CC0 FL	CC1 FL	CC2 FL	CC3 FL
11	-	-	-	-	-	-	-	-	Stop key FL	Address Stop	Missing power phase	-	Any interrupt	Instruction step	-	-
12	-	-	-	-	-	-	-	-	Load key FL	Register alter	Any unbuffered I/O busy	Any I/O busy	CE key switch off	Register display	Dev addr 15 inter-rupt	Time-sharing sw off
13	← 2 Data switches (byte) →															
14	← 4 Customer address switches →															
15	← 4 CE select switches →															
16	-	-	-	-	-	-	-	-	Halfword boundary check	Upper Stor address check	Lower stor address check	Decimal data check				Det log request FL

Data Independent Set/Reset Conditions

CTRL 00-07: Reset program level 0-7
CTRL 08-0F: Set program level 0-7
CTRL 10: Reset ICPL reset FL
SENS 11: Reset load FL
SENS 11 and channel mask or system reset:
Reset channel end FL
SENS 16 or not process: reset program check FL's

System Reset

When the system reset key is pressed, a trap request in program level 7 occurs with the difference that the start address of the level 7 routine is not taken from the IAR of level 7. The absolute instruction address /C002/ is forced by hardware.

If a process check has occurred, the system reset routine starts with testing, the logout area is saved, and the process check counter is increased by one.

The second step is to clear the complete local store. The IAR's (register 7 of every program level) are set to the starting addresses of the different program level routines; all other registers, except those used by the system reset routine itself, are cleared to zero.

Then the low-order core storage area containing indicators and the interrupt priority table, as well as the first halfword of the current PSW (location /84/), are reset to zero.

The last step in program level 7 is to reset the ICPL latch and the program check latches; program level 7 is reset and the machine comes to the stop in PL0.

Load

With the exception that the 'load' latch is also set, depression of the load key causes the same action as that produced by the system reset key. The 'load' latch is tested when the system reset routine enters program level 0. If the 'load' latch is off, the CPU stops. If it is on, the CPU reads a card and branches to the first position of the read area. This is done by providing the appropriate parameters for the card read I/O microprogram and loading the macro IAR with the data from the address switches.

Stop, Instruction Step, and Address Stop

When the stop key is pressed, the 'stop' latch is turned on. INSTRUCTION STEP and ADDRESS STOP are positions of the mode switch. These three conditions are tested by SENS /11/ at the beginning of an I-cycle (no run conditions). In the case of stop-latch-on or instruction-step-mode the machine comes to an unconditional stop. In the case of address-stop-mode or the instruction address not matching with the position of the address switches, the CPU proceeds with the next instruction. Only one 'halt' instruction exists in the microprogram.

Register Display and Alter

The test for 'register display' or 'alter' is located behind the 'halt' instruction. The display and alter function is performed according to the rules of the Model 20 console specifications. The address of the halfword to be displayed or altered is derived from the register number selected by data switch 1:

Reg No	*Displayed*	*Altered*
0-3	0080-0087	0080-0087
4-7	ZEROES	NOTHING
8-F	4 n	4 n

n = Register number

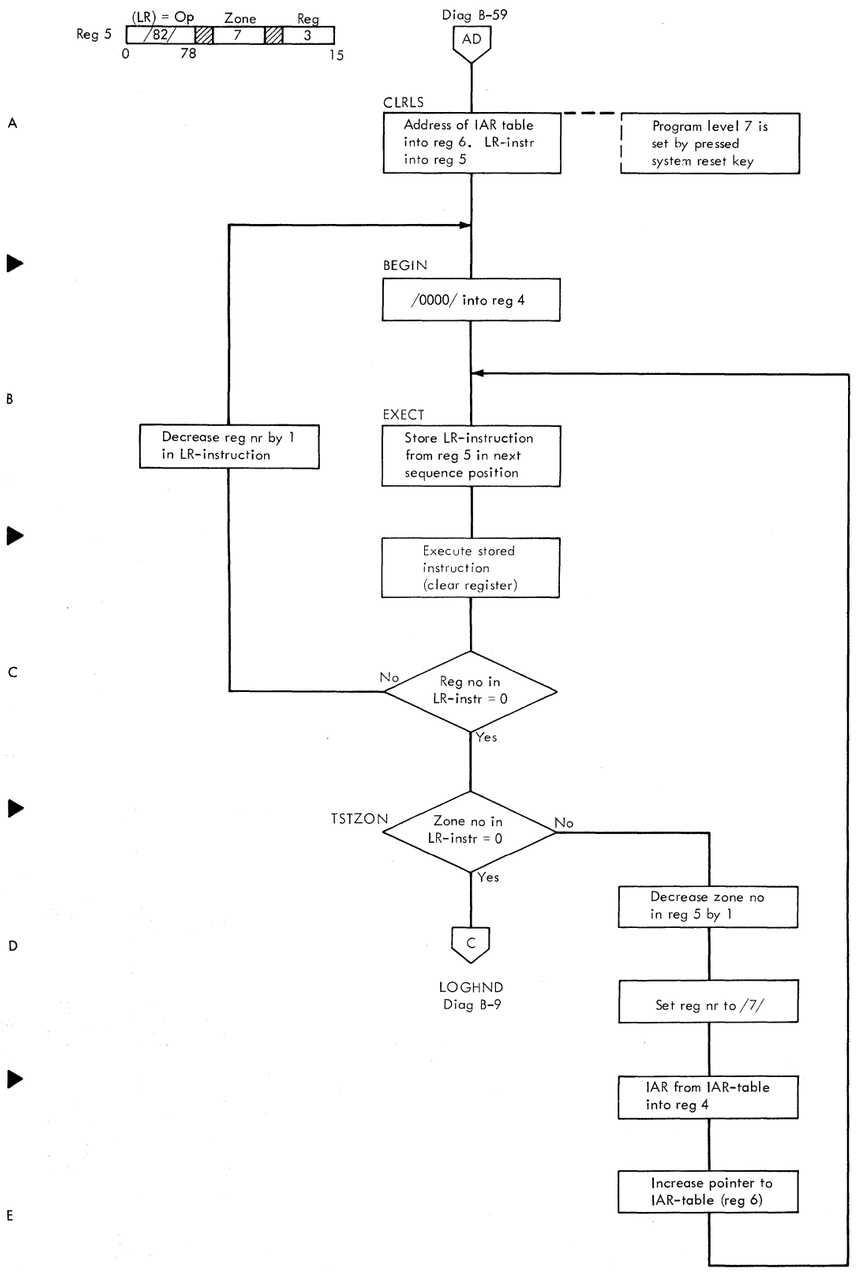
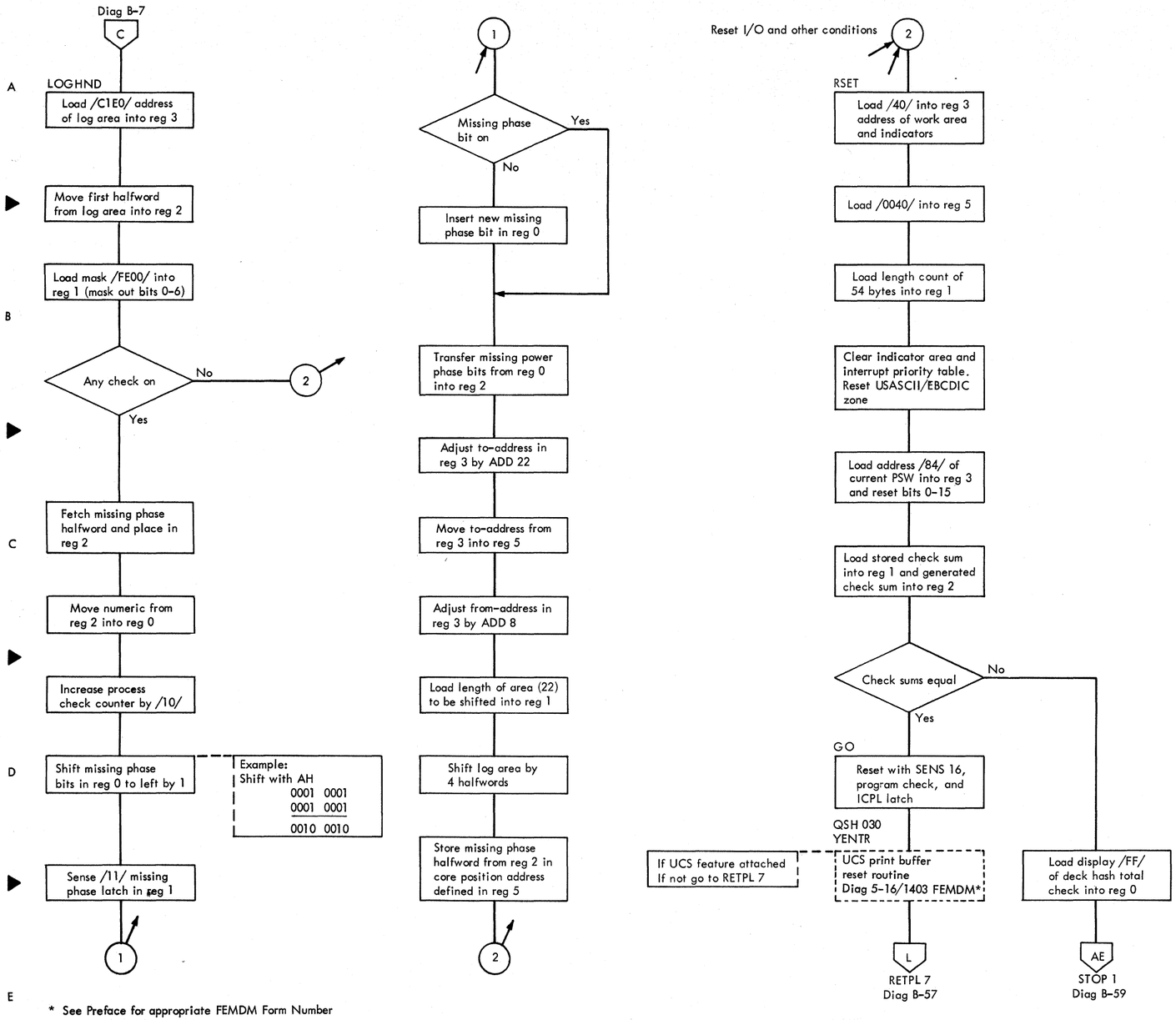


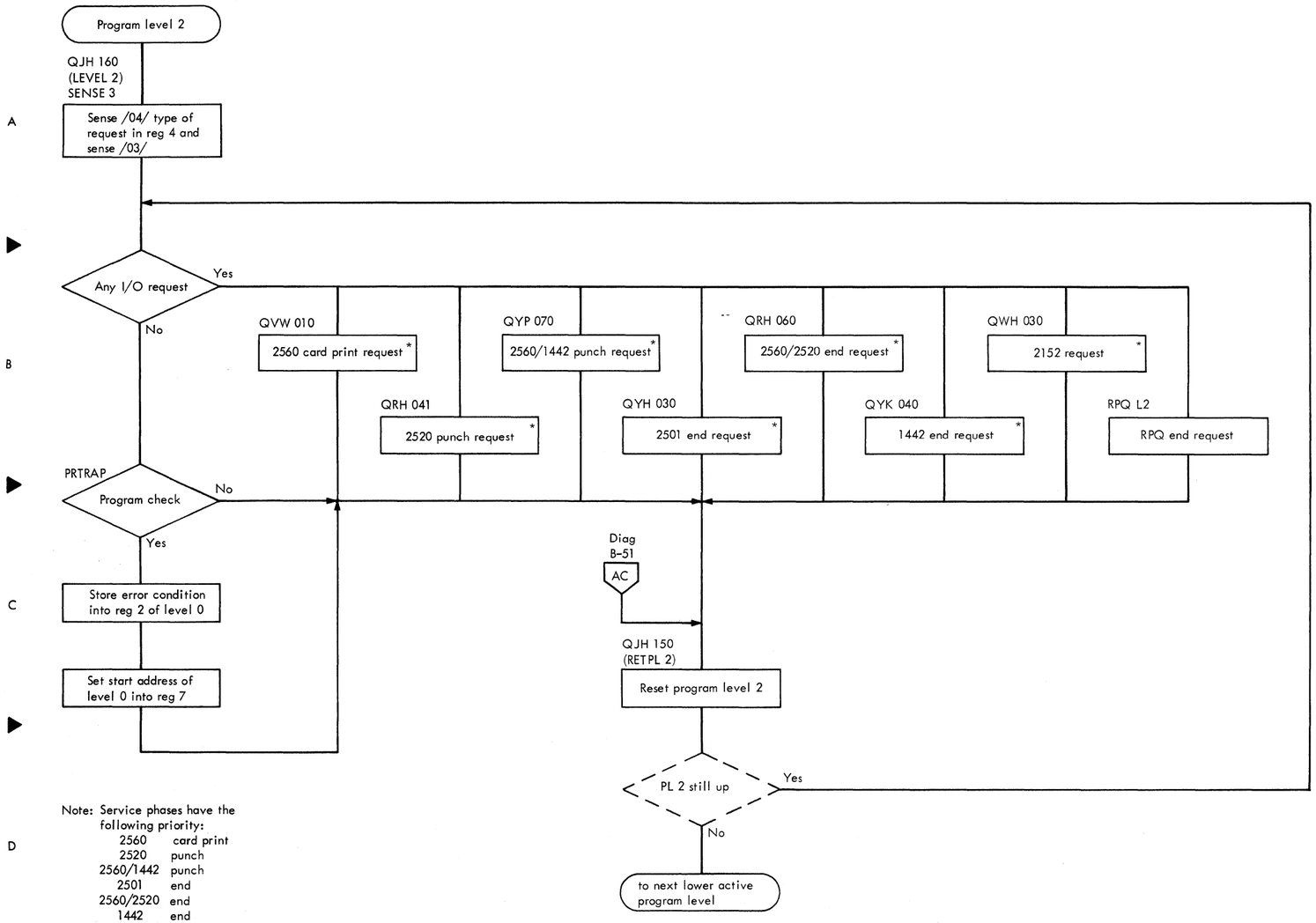
Diagram B-7. Clear Local Store (03929) 2020 ≃ 50,000 FEMDM Vol 1 (2/69)

CPU LOG HANDLING



* See Preface for appropriate FEMDM Form Number

Diagram B-9. CPU Log Handling (03930) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)



Note: Service phases have the following priority:

2560	card print
2520	punch
2560/1442	punch
2501	end
2560/2520	end
1442	end
2152	request

* See Preface for appropriate FEMDM Form Number

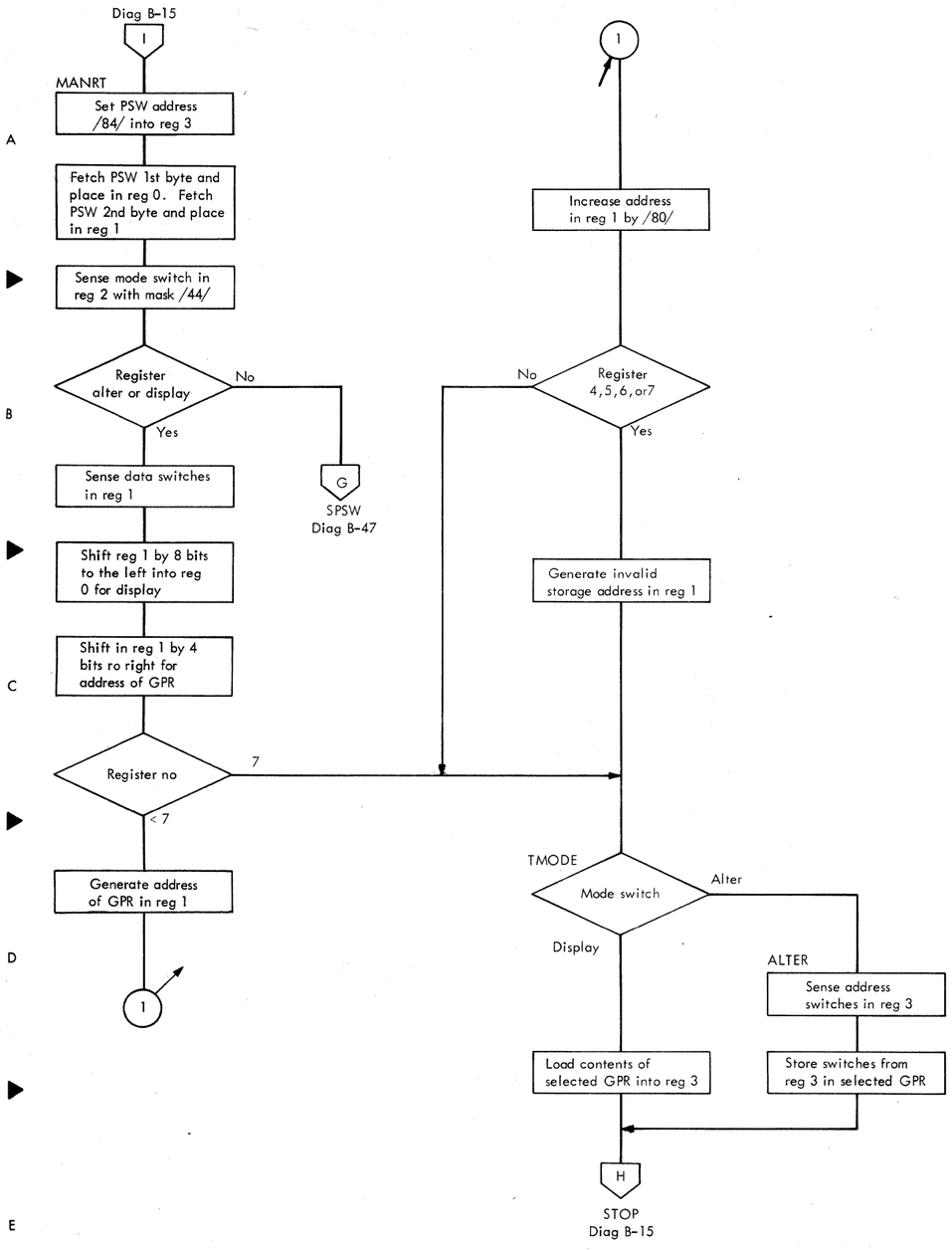


Diagram B-13. Manual Routine (03932) 2020 ≃ 50,000 FEMDM Vol 1 (2/69)

Programming Error Handling

Seven program error conditions exist for the Model 20. Each condition is identified by a code displayed in the I-register on the console:

Error Condition	*Display*
1. Invalid Op Code	1
2. Address Lower than 144	4
3. Address Exceeds Storage	5
4. Specification Check	6
5. Decimal Data Check	7
6. Binary Overflow	8
7. Decimal Divide Check	B

Error Conditions 2 through 5 are detected by hardware, while conditions 1, 6, and 7 are detected by microprogram. If the microprogram detects a program error, it loads the appropriate display code into the left-hand byte of LS register 0 and branches to the exception routine, which stores the PSW and performs the stop. The difference from the normal stop is that in an error stop the IAR (6) is loaded with the I-recall address (address of the instruction in which the error occurred). In a normal stop, the IAR (6) contains the address of the next sequential instruction.

A hardware-detected program error causes a trap in program level 2. Which of the four possible error conditions exists is determined by SENS /16/. This information is transferred to level 0, where the appropriate display code is set. The rest of the action is the same as for the micro-program-detected program error.

Stop Conditions and Related Displays

Normal Stops

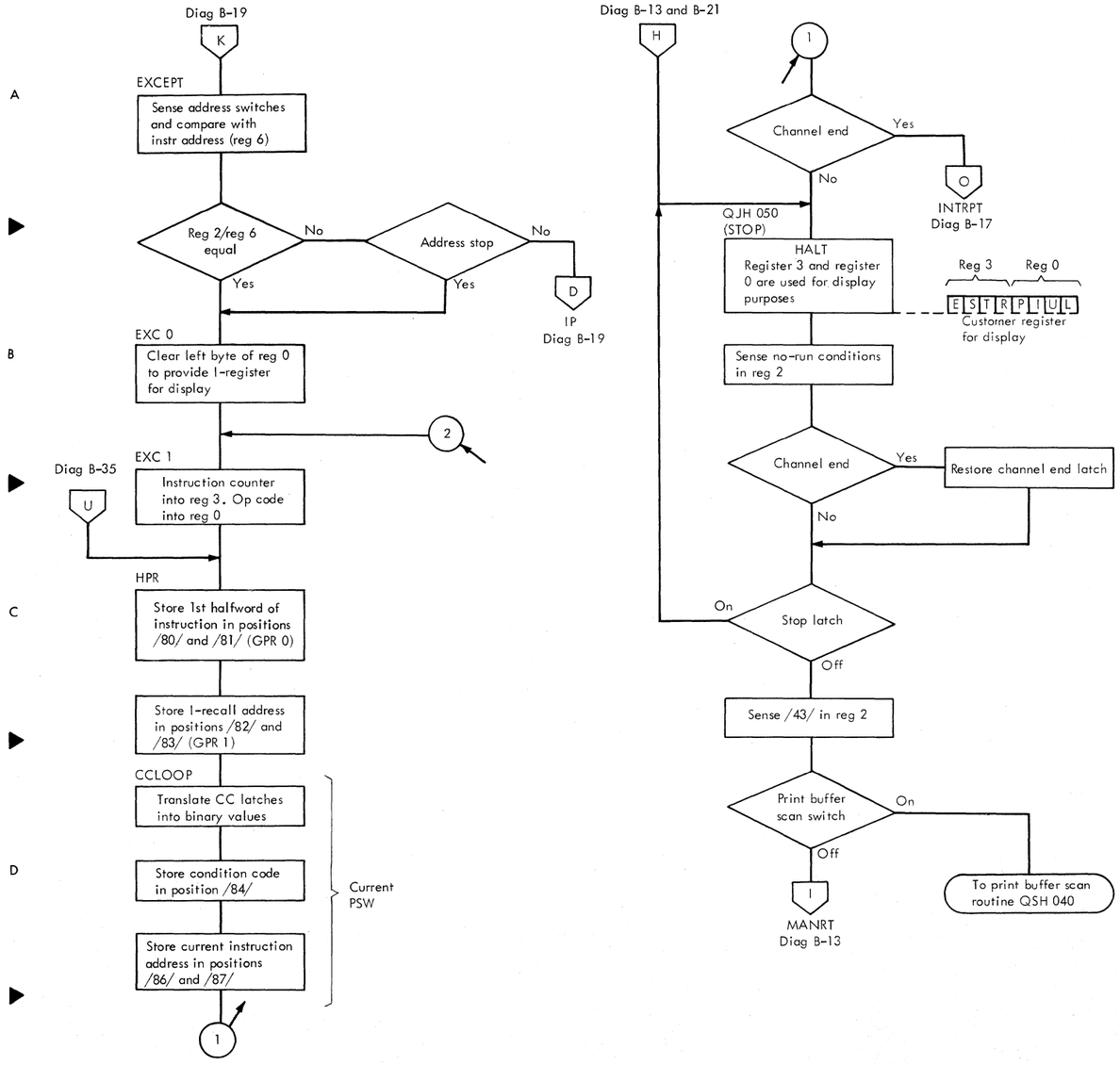
	P	I	U	L	E	S	T	R
SYSTEM RESET	0	0	0	0	0	0	0	0
HPR - INSTRUCTION			9	9	HALT Identifier (D1-B1)			
STOP KEY			Machine Instruction Op Code		Instruction Address			
ADDRESS STOP								
INSTRUCTION STEP								
REGISTER ALTER	No of selected reg		0	0	Register Data			
REGISTER DISPLAY								

Program Error Stops

INVALID OPCODE	0	1	Machine Instruction Op Code	Instruction Address
ADDRESS LOWER 144		4		
ADDR EXCEEDS STOR		5		
SPECIFICATION CHECK		6		
DEC DATA CHECK		7		
BIN OVERFLOW		8		
DEC DIVIDE CHECK		B		

[03849]

EXCEPTION ROUTINE



PROGRAMMING ERRORS

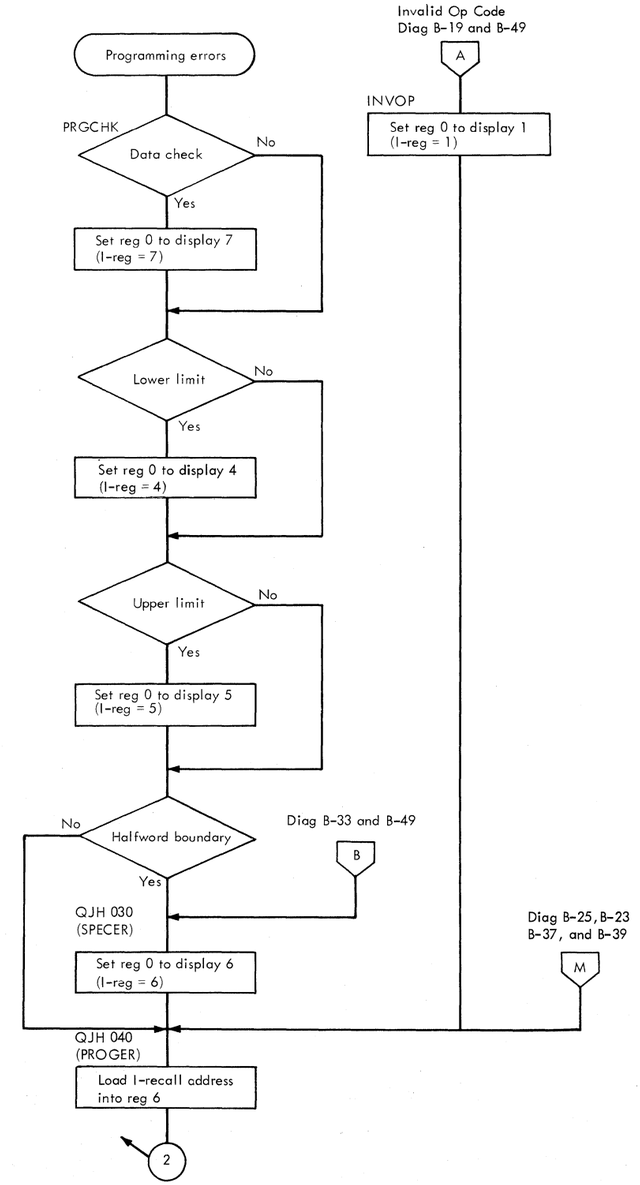
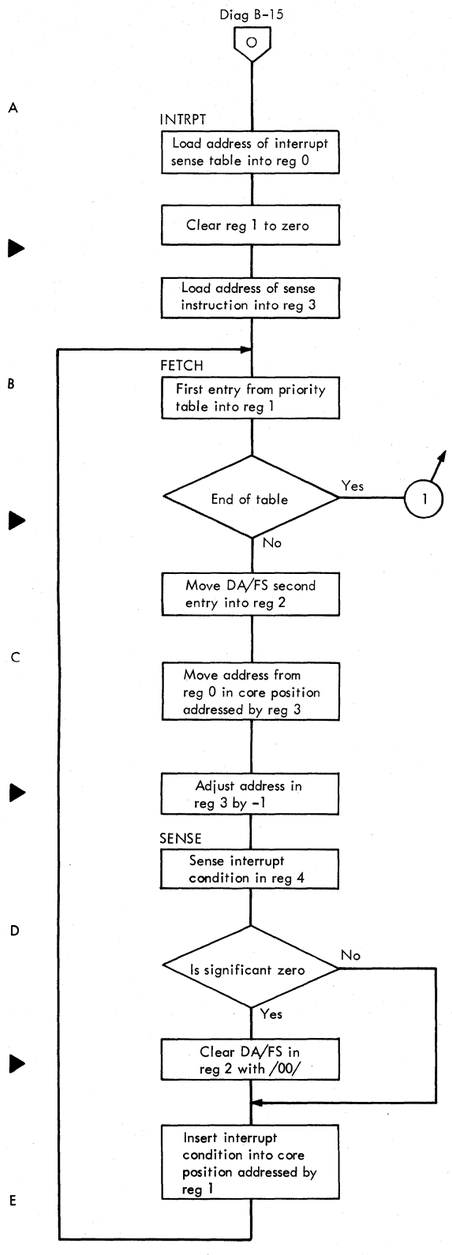


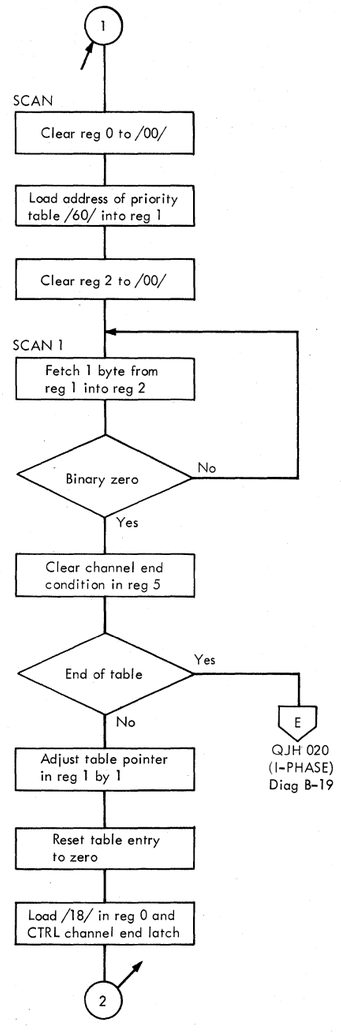
Diagram B-15. Exception Routine and Programming Errors (03934) 2020 ≃ 50,000 FEMDM Vol 1 (2/69)

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

TEST AND STORE HARDWARE INTERRUPT CONDITIONS



SCAN INTERRUPT PRIORITY TABLE



STORE OLD PSW AND BRANCH TO SPECIAL I/O ROUTINE

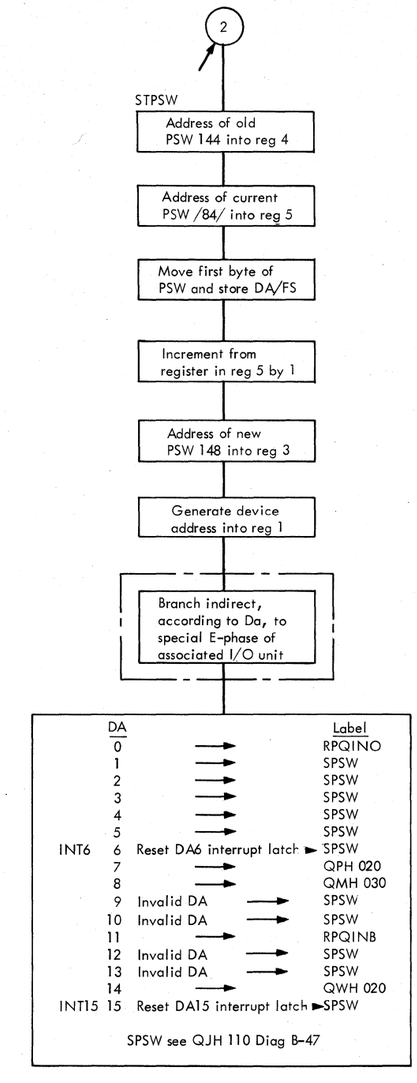
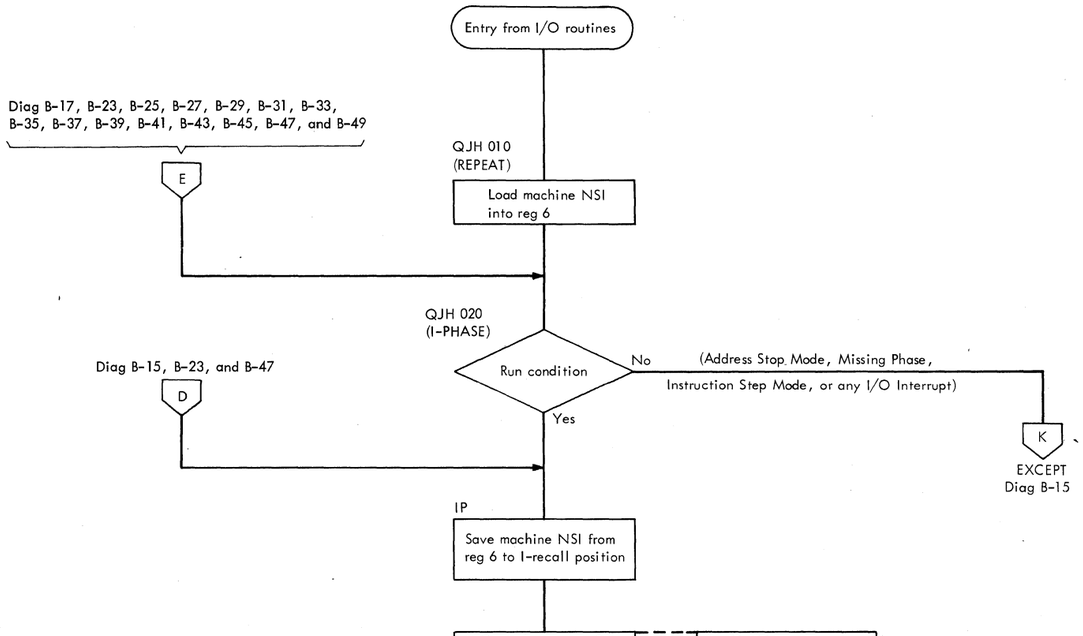


Diagram B-17. Interrupt Handling (03935) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

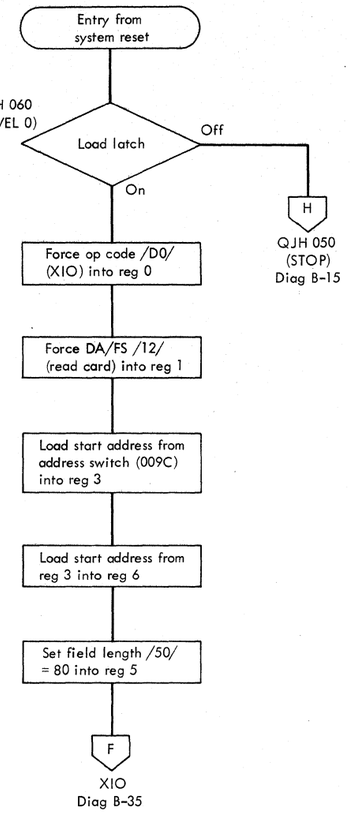


OPTB

Op Code	Mnemonic	Diagram	Op Code	Mnemonic	Diagram
/07/	BCR	B-23	/9B/	CIO	B-35
/0D/	BASR	B-23	/D0/	XIO	B-27
/1A/	AR	B-25	/D1/	MVN	B-27
/1B/	SR	B-25	/D2/	MVC	B-27
/40/	STH	B-25	/D3/	MVZ	B-27
/47/	BC	B-23	/D5/	CLC	B-31
/48/	LH	B-25	/DC/	TR	B-27
/49/	CH	B-25	/DE/	ED	B-27
/4A/	AH	B-25	/F1/	MVO	B-41
/4B/	SH	B-25	/F2/	PACK	B-45
/4D/	BAS	B-25	/F3/	UNPK	B-43
/81/	SPSW	B-47	/F8/	ZAP	B-33
/83/	~~DIAGN~~	B-49	/F9/	CP	B-33
/91/	TM	B-31	/FA/	AP	B-33
/92/	MVI	B-35	/FB/	SP	B-33
/94/	NI	B-35	/FC/	MP	B-37
/95/	CLI	B-31	/FD/	DP	B-37
/96/	OI	B-35			
/99/	~~HPR~~	B-35			
/9A/	TIOB	B-35	all other codes are invalid op		B-15 (off-page connector A)

Diagram B-19. Common I-Phase for all Instructions (03936)

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9



A

B

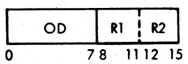
C

D

E

Diagram B-21. Load Routine (03937) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

Branch and Store (BASR), Branch, RR Format

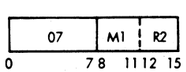


- **Objective: the rightmost 16 bits of the PSW (the updated instruction address) are stored as link information in the GPR specified by R1. Subsequently, the instruction address is replaced by the branch address.**
- **R1 is the address of a GPR into which the NSI address is stored.**
- **R2 is the address of a GPR which contains the branch address.**

The branch address is determined before the link information is stored.

When the R2 field contains zero, the link information is stored without branching.

Branch On Condition (BCR), Branch, RR Format



- **Objective: the updated instruction address is replaced by the branch address if the state of the condition code is as specified by M1; otherwise, normal instruction sequencing proceeds with the updated instruction address (0000 0111).**
- **M1 is a four-bit field, used as a mask.**
- **R2 is the address of a GPR which contains the branch address.**

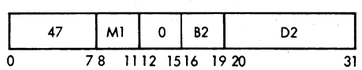
The M1 field is used as a four-bit mask. The four bits of the mask correspond, left to right, with the four condition codes shown in the following:

Condition Code	*Instruction Bits*
0 0	8
0 1	9
1 0	10
1 1	11

The branch is successful (that is, occurs) whenever the condition code has a corresponding mask bit of one.

When all four mask bits are ones, the branch is unconditional. When all four mask bits are zero or when the R2 field contains zero, the branch instruction is equivalent to a no operation.

Branch On Condition (BC), Branch, RX Format



- **The updated instruction address (NSI address) is replaced by the branch address if the state of the condition code is as specified by M1; otherwise, normal instruction sequencing proceeds with the NSI address.**
- **M1 is a four-bit field used as a mask.**
- **The /0/ four-bit field is not used and must be /0/ (0000).**
- **B2 and D2 are the direct or effective main storage address which is used as a branch address.**

The M1 field is used as a four-bit mask. The four bits of the mask correspond, left to right, with the four condition codes, 0, 1, 2, 3, as shown in the following table:

Condition Code	*Instruction Bits*
0 0	8
0 1	9
1 0	10
1 1	11

The branch is successful whenever the condition code has a corresponding mask bit of one.

When all four mask bits are ones, the branch is unconditional. When all four mask bits are zero, the branch instruction is equivalent to a no operation.

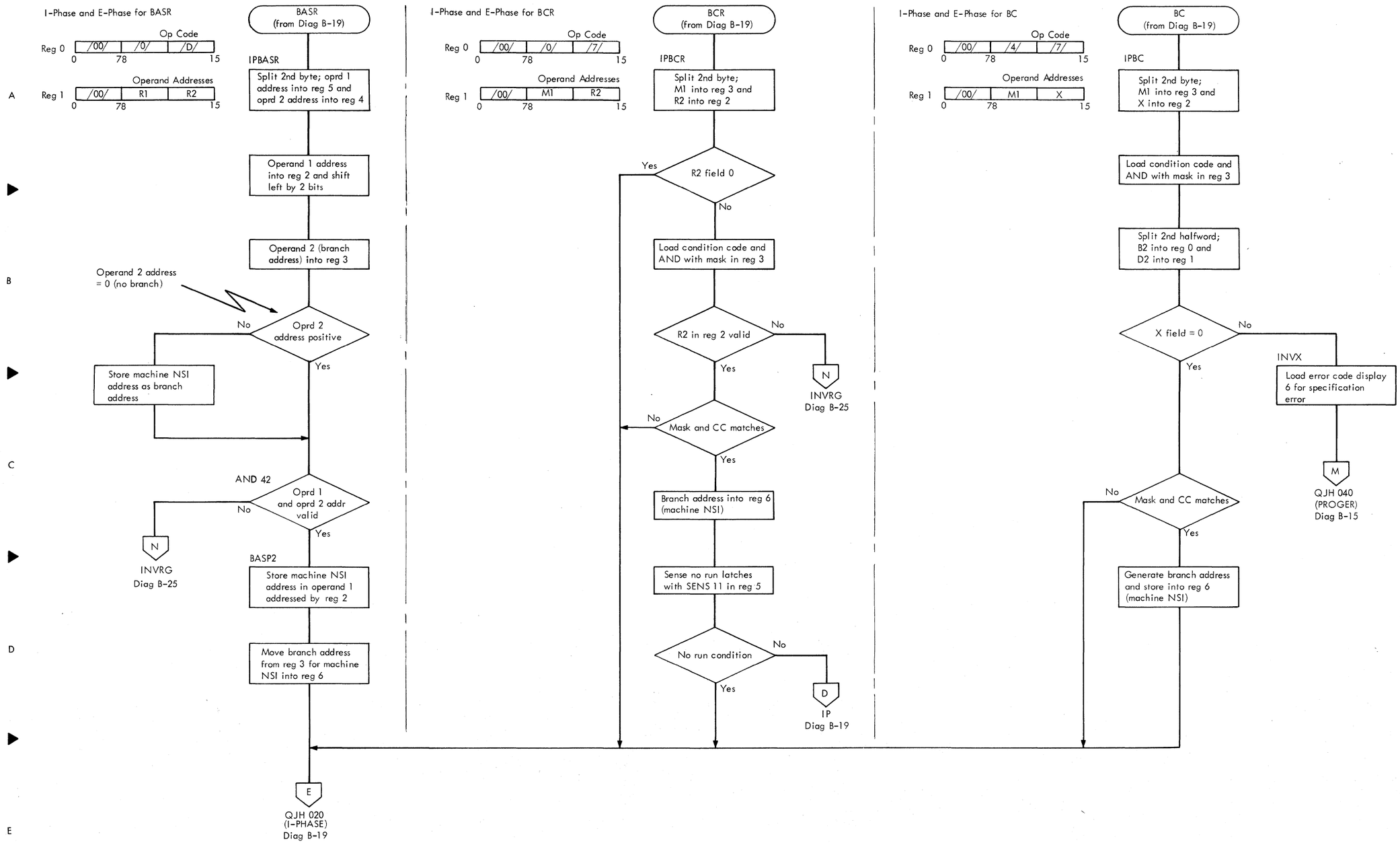
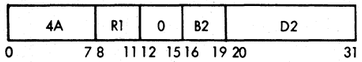


Diagram B-23. BASR, BCR, and BC I-Phase and E-Phase (03939)

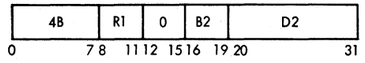
Add Halfword (AH), Fixed-Point, RX Format



- **The second operand is added to the first operand.**
- **The sum is placed in the first operand location.**
- **R1 is the address of a GPR which contains operand 1.**
- **The /0/ four-bit field is not used and must be /0/ (0000).**
- **B2 and D2 are the direct or effective main storage address and must be even (boundary).**

Operands and sums are treated as 15-bit integers with signs. The operation is performed by adding all 16 bits of both operands. If the carries out of the sign bit position and the high-order numeric bit position agree, the sum is satisfactory. If they disagree, an overflow has occurred. The sign bit is not changed after the overflow. A positive overflow yields a negative final sum and a negative overflow results in a positive sum. An overflow results in a binary overflow error condition; the CPU stops and DR-I contains an /8/ to indicate binary overflow.

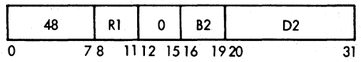
Subtract Halfword (SH), Fixed-Point, RX-Format



- **The second operand is subtracted from the first operand and the difference is placed in the first operand location.**
- **R1 is the address of a GPR which contains operand 1.**
- **The /0/ four-bit field is not used and must be /0/ (0000).**
- **R2 and D2 are the direct or effective main storage address of operand 1 and must be even (boundary).**

Operands and differences are treated as 15-bit integers with a sign. Subtraction is performed by adding the twos complement of the second operand to the first operand. All 16 bits of both operands participate as in the add instruction. If the carries out of the sign bit position and the high-order numeric bit position agree, the difference is satisfactory. If they disagree, an overflow has occurred, resulting in a binary overflow error condition; the CPU stops and DR-I contains an /8/ to indicate binary overflow. Subtracting a maximum negative number from another maximum negative number gives a zero result and no overflow.

Load Halfword (LH), Fixed-Point, RX Format

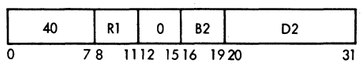


- **The halfword second operand is placed in the first operand location.**
- **R1 is the address of a GPR which contains the operand 1.**
- **The /0/ four-bit field is not used and must be /0/ (0000).**
- **B2 and D2 are the direct of effective main storage address of operand 2.**

If the four-bit field (12-15) is not /0/, the CPU stops with a /6/ in DR-I to indicate a program (specification) error.

The operand 2 address must be even (boundary). If it is not even, the CPU stops. DR-I contains a /6/ to indicate a program (specification) error.

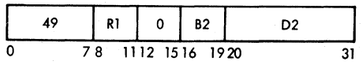
Store Halfword (STH), Fixed-Point, RX Format



- **Objective: store the first operand at the halfword second operand location.**
- **R1 is the address of a GPR which contains operand 1.**
- **The four-bit field is not used and must be /0/ (0000).**
- **B2 and D2 are the direct or effective main storage address of operand 2.**

In this operation, operand 2 and not operand 1 is replaced (destroyed). If the four-bit field (12-15) is not /0/, the CPU stops with a /6/ in DR-I to indicate a program (specification) error.

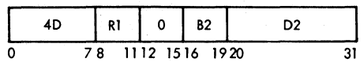
Compare Halfword (CH), Fixed-Point, RX-Format



- **The first operand is compared with the second operand.**
- **The result of the comparison is saved in the condition code latches.**
- **R1 is the address of a GPR which contains operand 1.**
- **The /0/ four-bit field is not used and must be /0/ (0000).**
- **B2 and D2 are the direct or effective main storage address of operand 2.**

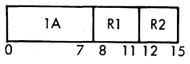
Comparison is algebraic. Both operands are treated as 15-bit integers with signs. Operands in registers or storage are not changed as a result of the operation. If the four-bit field (12-15) is not /0/, the CPU stops with a /6/ in DR-I to indicate a program (specification) error.

Branch and Store (BAS), Branch, RX Format



- **The rightmost 16 bits of the PSW (the updated instruction address) are stored as link information in the GPR specified by R1.**
- **Subsequently, the instruction address is replaced by the branch address.**
- **R1 is the address of a GPR which receives the NSI address.**
- **The four-bit field is not used and must be /0/ (0000).**
- **B2 and D2 are the direct or effective main storage address which is used as branch address.**

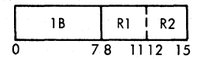
Add (AR), Fixed-Point, RR Format



- **Objective: add the second operand to the first operand.**
- **The sum is placed in the first operand location.**
- **R1 is the address of a GPR which contains operand 1.**
- **R2 is the address of a GPR which contains operand 2.**

Operands and sums are treated as 15-bit integers with sign. Addition is performed by adding all 16 bits of both operands. If the carry out of the sign-bit position and the high-order numeric bit agree, the sum is satisfactory. If they disagree, an overflow has occurred. A positive overflow yields a negative final sum, and a negative overflow results in a positive sum. An overflow results in a binary overflow error condition. The CPU stops and DR-I contains a /8/ to indicate the binary overflow.

Subtract (SR), Fixed-Point, RR Format

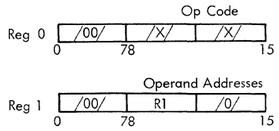


- **Objective: subtract the second operand from the first operand.**
- **The difference is placed in the first operand location.**
- **R1 is the address of a GPR which contains operand 1.**
- **R2 is the address of a GPR which contains operand 2.**

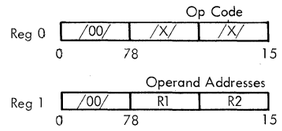
Operands and differences are treated as 15-bit integers with sign. Subtraction is performed by adding the twos complement of the second operand to the first operand. All 16 bits of both operands participate as in the add instruction. If the carry out of the sign bit position and the high-order numeric bit position agree, the difference is satisfactory. If they disagree, an overflow has occurred, resulting in a binary overflow error condition; the CPU stops and DR-I contains an /8/ to indicate binary overflow.

I-Phase and E-Phase for AH, SH, LH, STH, CH, BAS

E-Phase for AR and SR



I-Phase for AR and SR



AH, SH, LH, STH, CH, and BAS (from Diag B-19)

IPRX

Read out B2 and store in reg 2. Read out D2 and store in reg 3

If address check, branch to trap 2

Generate operand 2 address out of B2-D2. Result into reg 3

Shift operand 1 address by 2 into reg 2

Operand 2 into reg 4

If address check, branch to trap 2

ASR

GPR addr specified by R1 valid

No

Load error code display 6 if specified reg = 0-7, or display 5 if programmed bits 12-15 are not 0

Yes

1

Which Op code

AH/AR

AHAR

Add operands and store result into core position addressed by reg 2 and set CC

SH/SR

SHSR

Subtract operands and store result into core position addressed by reg 2 and set CC

AHARP 2

Sense condition code and store into reg 0

BAS

Adjust branch address in reg 3 by -2

BASP 2

Store machine NSI in operand 1 (addressed by reg 2)

Move branch address from reg 3 for machine NSI address into reg 6

LH

Move halfword from reg 4 and store into GPR defined by reg 2

STH

Adjust data address in reg by -2

Store halfword addressed by reg 2 into core position addressed by reg 3

CH

Operand 1 into reg 2

Subtract oprd 2 from oprd 1 (reg 4 from reg 2). Result in reg 2

Sense condition code and store into reg 1

Overflow bit set

No

Yes

Load error code display 8 for overflow error into reg 0

Overflow bit set

No

Yes

Indicating negative result of subtraction

Remove overflow bit from CC and reverse bits 2 and 4 since result of SH was negative. Set new condition code

M

QJH 040
(PROGER)
Diag B-15

E

QJH 020
(I-PHASE)
Diag B-19

AR and SR (from Diag B-19)

IPASR

Oprd 2 addr into reg 3 and shift left by 2. Oprd 1 addr into reg 2 and shift right by 2

Load operand 2 addressed by reg 3 into reg 4

GPR addr specified by R1 and R2 valid

Yes

1

No

Diag B-23

N

INVRG

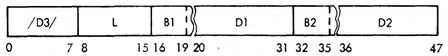
Load error code display 5 for addressing error into reg 0

M

QJH 040
(PROGER)
Diag B-15

Diagram B-25. AH, SH, LH, STH, CH, BAS, AR, and SR I-Phase and E-Phase (03941) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

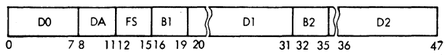
Move Zones (MVZ), Logical, SS Format



- **Objective: the four high-order bits of each byte in the second operand field (the zones) are placed in the corresponding bit positions of the first operand field. The four low-order bits of each byte (the numerics) remain unchanged in both operand fields.**
- **L is the field length of both operands.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

The instruction has the SS format and, therefore, is a storage-to-storage move. Movement is left to right through each field and the same overlapping field conditions may arise as in the preceding move instruction.

Transfer I/O (XIO), Logical, SS Format



The device address (DA) specifies the I/O device to which output data is to be transmitted, or from which input data is to be received.

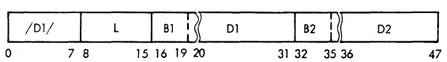
The function specification (FS) specifies the input or output function to be performed on the I/O device addressed and the particular component of the addressed device (when required).

The main-storage location of the first byte in the input or output data field is derived from the contents of the B1-D1 fields according to the rules for direct or effective address generation.

The field or record length of the input or output data in main storage is derived from the contents of the B2-D2 fields.

The field length specification for input or output data fields in main storage is the actual number of bytes in the field. Whereas for variable field length processing operations, the field length specification is the number of bytes extending beyond the first byte.

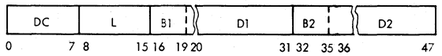
Move Numerics (MVN), Logical, SS Format



- **Objective: the four low-order bits of each byte in the second operand field (the numerics) are placed in the low-order bit positions of the bytes in the first operand field. The four high-order bits of each byte (the zones) remain unchanged in both operand fields.**
- **L is the field length of both operands.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

The instruction has the SS format and, therefore, is a storage-to-storage move. Movement is left to right through each field. The fields may overlap in any desired way.

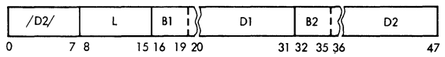
Translate (TR), Logical, SS Format



- **Objective: the second operand address designates the beginning of a translate list. The binary value of each byte of the first operand selects a position within this list. The contents of this position replace the selecting byte in the first operand.**
- **L is the field length of both operands.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

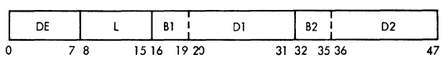
The bytes of the first operand are selected one-by-one for translation. Each argument byte is added to the entire initial address, the second operand address, in the low-order bit positions. The sum is used as the address of the function byte which then replaces the original argument byte. The operation proceeds until the first operand field is exhausted. It is permissible for the list and the first operand field to overlap.

Move Characters (MVC), Logical, SS Format



- **Objective: the second operand is placed in the first operand location.**
- **The SS format is used for storage-to-storage move.**
- **In the storage-to-storage move, the fields may overlap in any desired way. Movement is left to right through each field, one byte at a time.**
- **The bytes to be moved are not changed or inspected. The condition code is not changed.**
- **L is the field length of both operands.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

Edit (ED), Logical, SS Format



- **The format of the source (the second operand) is changed from packed to zoned, and is edited under control of the pattern (the first operand).**
- **The edited result replaces the pattern.**
- **Editing includes sign and punctuation control, and the suppression and protection of leading zeros.**
- **Editing facilitates programmed blanking of all-zero fields.**
- **Several numbers may be edited in one operation, and numeric information may be combined with text.**
- **The op code is DE (1101 1111).**
- **L is the field length of the pattern (first operand).**
- **B1 and D1 are the main storage address of the pattern.**
- **B2 and D2 are the main storage address of operand 2.**

The field length applies to the pattern (the first operand). The pattern has the unpacked format and may contain any character. The source (the second operand) has the packed format and must contain valid digit and sign codes. The four left bits of a byte must be 0000-1001, otherwise a data error occurs. The right four bits are recognized as either a sign or a digit.

Both operands are processed left to right, one character at a time. Overlapping pattern and source fields give unpredictable results.

The character to be stored in the first operand field is determined by three items; the digit obtained from the source field, the pattern character, and the state of a trigger, called the S trigger. One of three actions may be taken as follows:

1. The source digit may be stored.
2. The pattern character may be left unchanged.
3. A fill character may be stored.

Programming Notes

As a rule, the source operand is shorter than the pattern since it yields two digits (or a digit and a sign) for each source number.

When a single instruction is used to edit several numbers, the zero-field identification is provided only for the last field.

The following table gives the details of an editing operation. The leftmost columns give the pattern character and its code. The next columns show the states of the digit and the S trigger used to determine the resulting action. The rightmost column shows the new setting of the S trigger.

Character Code	*Name and Purpose*	*Examine Digit*	*Trigger Status*	*Digit Status*	*Result Char*	*Trigger Set*
0010 0000	Digit select	Yes	s = 1		Digit	
			s = 0	d not 0	Digit	s = 1
			s = 0	d = 0	Fill	
0010 0001	Significance start		s = 1		Digit	
		Yes	s = 0	d not 0	Digit	
			s = 0	d = 0	Fill	s = 1
0010 0010	Field separator	No			Fill	s = 0
Other	Message insertion		s = 1		Leave	
		No	s = 0		Fill	

Legend:
d - Source digit
s - S trigger 1: minus sign; digits or pattern used
0: plus sign; fill used
Digit - A source digit replaces the pattern character
Fill - The fill character replaces the pattern character
Leave - The pattern character remains unchanged

S Trigger

The S trigger is used to control the storing or replacing of source digit and pattern characters. Source digits are replaced when zero suppression or protection is desired. Digits to be stored in the result, whether zero or not, are termed *significant*. Pattern characters are replaced or stored when they are significance-dependent or sign-dependent, such as punctuation or credit symbols. The S trigger is also used to record the sign of the source and set the condition code accordingly.

The S trigger is set to the zero state at the start of the operation and is subsequently changed, depending upon the source number and the pattern characters.

Pattern Character

Three pattern characters (digit-select character, significance-start character, and field-separator character) have a special use in editing as follows:

Note: The three characters are replaced either by a source digit or by a fill character; their encoding is shown in the table under "Programming Notes".

1. The digit-select character causes either a source digit or the fill character to be inserted in the result field.
2. The significance-start character has the same function as the digit-select character. It also indicates that the following digits are significant.
3. The field-separator character identifies individual fields in a multiple-field editing operation. The character is replaced by the fill character. The S trigger is set to zero and testing for a zero-field is re-initiated.
4. All other pattern characters are treated in a common way. If the S trigger is one, the pattern character is left unchanged; if the S trigger is zero, the pattern character is replaced by the fill character.

If the pattern character is either a digit-select or a significance-start character, the source digit is examined. The source digit replaces either of these pattern characters if the S trigger is one or if the source digit is non-zero. A non-zero digit inserted when the S trigger is zero causes the S trigger to be set to one to indicate that the following digits are significant. If the S trigger and the source digit are both zero, the fill character is substituted for either the digit-select or significance-start character.

Source Digit

When the source digit is stored in the result, it is expanded from the packed to the zoned format by attaching a zone. The zone code is 1111 in the binary coded decimal mode and 0101 in the USASCII mode.

The source digits are examined only once during an editing operation. They are selected eight bits at a time from the second operand field. The four leftmost bits are examined first. The four rightmost bits remain available for the next pattern character which calls for a digit examination. However, the four rightmost bits are inspected for a sign code immediately after the four leftmost bits are examined.

Any of the plus-sign codes (1010, 1100, 1110, or 1111) set the S trigger to zero after the digit is inspected, whereas the minus-sign codes (1011 and 1101) leave the S trigger unchanged. When one of these sign codes is encountered in the four rightmost bits, these bits no longer are treated as a digit, and a new character is fetched from storage for the next digit to be examined.

A plus sign sets the S trigger to zero, even if the trigger was set to one for a non-zero digit in the same source byte (or by a significance-start character for that digit).

Fill Character

The fill character is obtained from the pattern as part of the editing operation. The first character of the pattern is used as the fill character and is left unchanged in the result field, except when it is the digit-select or significance-start character. In the latter cases, a digit is examined and, when non-zero, inserted.

Result Condition

To facilitate the blanking of all-zero fields, the condition code is used to indicate the sign and zero status of the last field edited. All digits examined are tested for the code 0000. The presence or absence of an all-zero source field is recorded in the condition code at the termination of the editing operation. The use of the condition code is as follows:

1. The condition code is made 0 for a zero source field, regardless of the state of the S trigger.
2. For a non-zero source field and an S trigger of one, the code is made 1 to indicate less than zero.
3. For a non-zero source field and an S trigger of zero, the code is made 2 to indicate greater than zero.

The condition-code setting pertains to fields as specified by the field-separator characters, regardless of the number of signs encountered.

For the multiple-field editing operations, the condition-code setting reflects only the field following the last field-separator character. When the last character of the pattern is a field-separator character, the condition code is made 0.

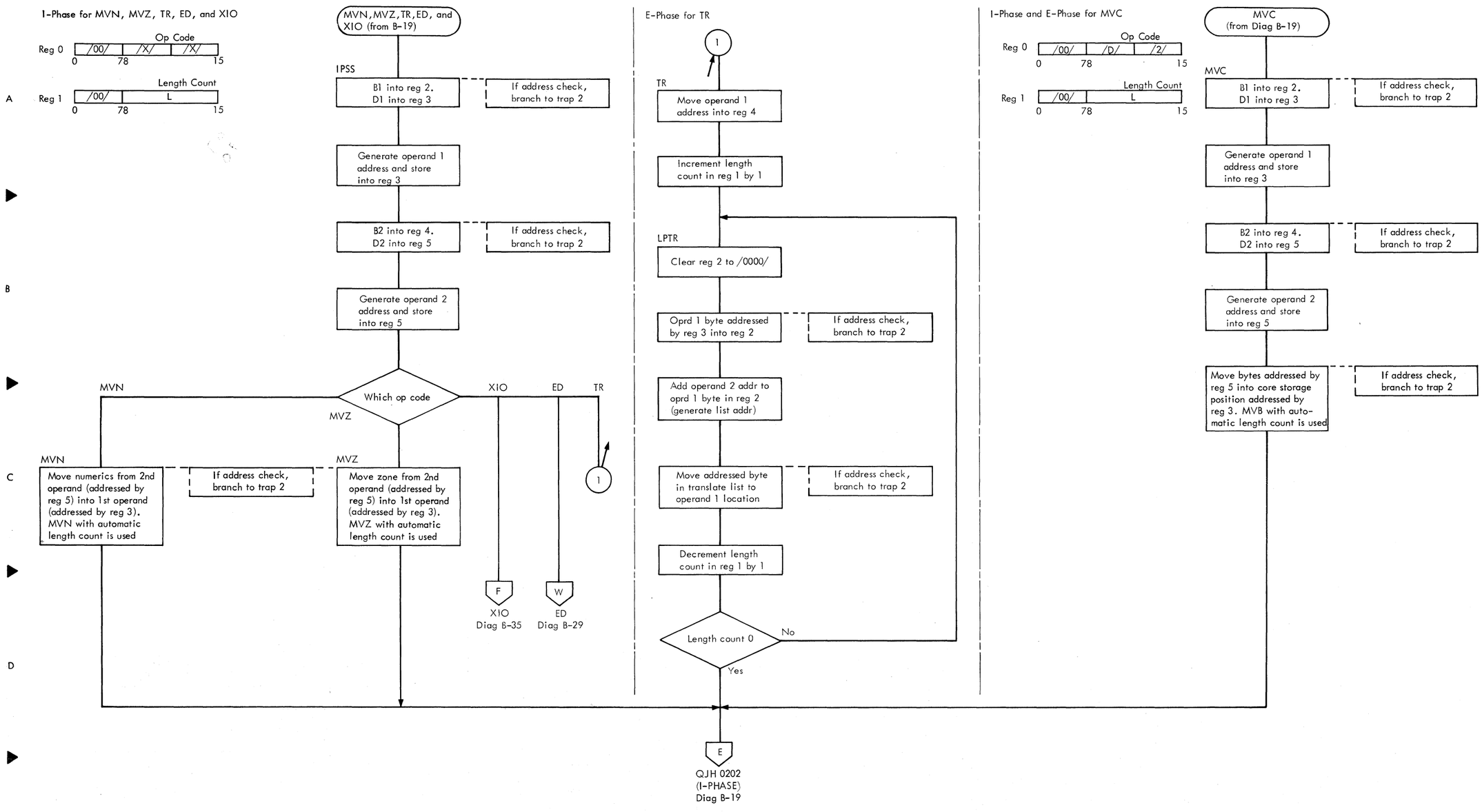


Diagram B-27. MVN, MVZ, TR, ED, XIO, and MVC I-Phase and MVN, MVZ, TR, and MVC E-Phase (03943) 2020 ≃ 50,000 FEMDM Vol 1 (2/69)

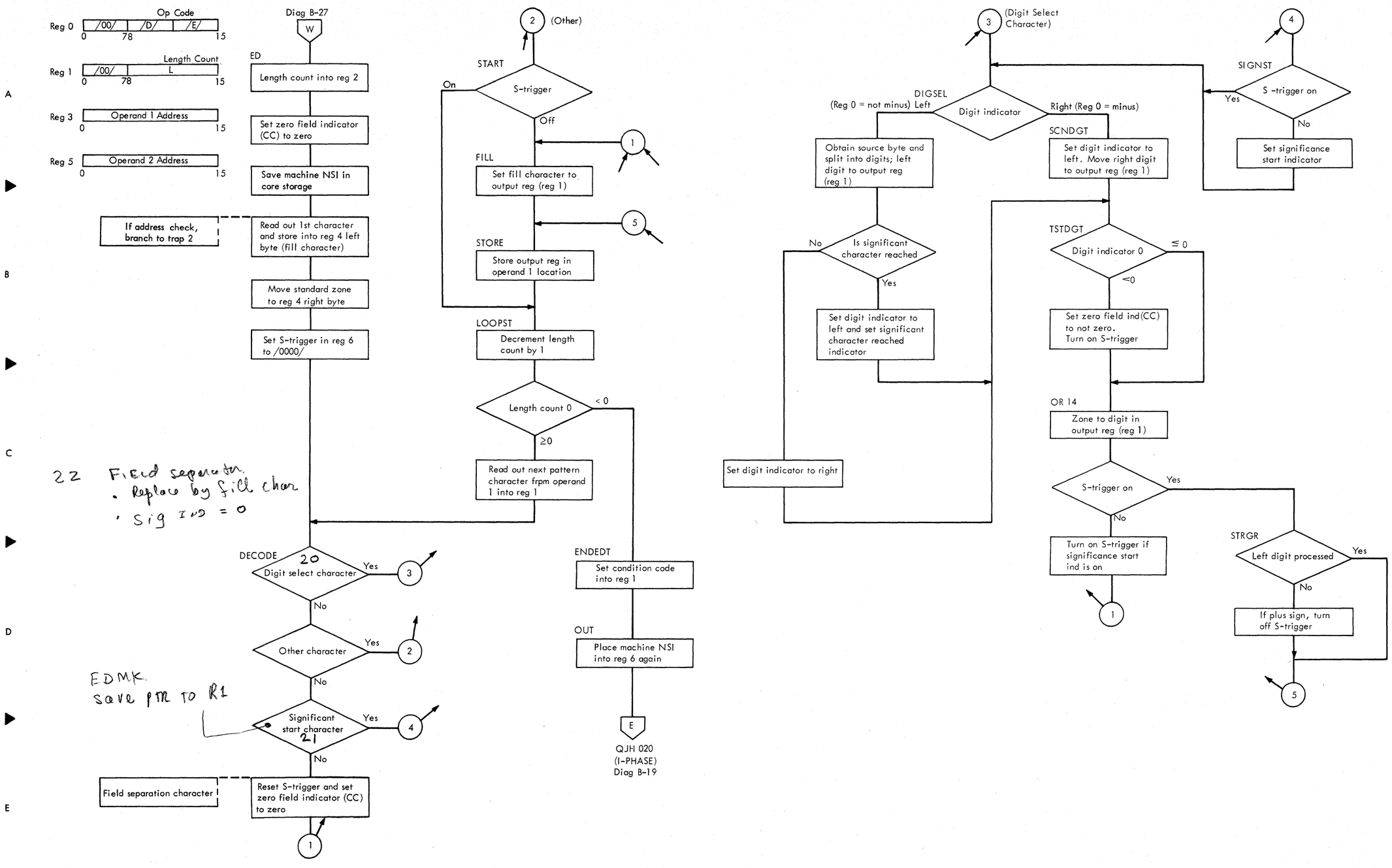
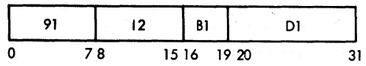


Diagram B-29. EDIT E-Phase (03944) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

Test Under Mask (TM), Logical Data, SI Format



- **The first operand one byte is ANDed with the second operand (one byte) to set the condition code.**
- **I2 is the operand 2 and is called mask.**
- **B1 and D1 are the direct or effective main storage address of operand 1.**

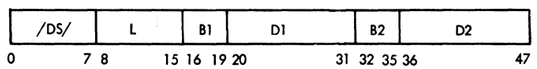
The condition code is set to:

00 (Zero): If operand 1 and operand 2 (mask) have no corresponding bits.

11 (All ones): If operand 1 has bits (1) in all corresponding positions where the operand 2 (mask) has bits (1).

01 (Mixed): For all other bit patterns in operand 1 or operand 2.

Compare Logical (CLC), Logical Data, SS Format



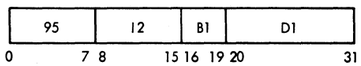
- **Objective: the first operand is compared with the second operand and the result is indicated in the condition code.**
- **L is the field length of both operands.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

The SS format is used for storage-to-storage comparison. The operation proceeds left to right.

In the compare logical operation, all bits are treated alike as part of an unsigned binary quantity. In the variable length storage-to-storage operation, comparison is left to right and may extend to field lengths of 256 bytes. The operation may be used for alphameric comparison.

The condition code is made 00 if the operands are equal, 01 if the first operand is low compared with the second operand, and 10 if the first operand is high compared with the second operand.

Compare Logical (CLI), Logical Data, SI Format

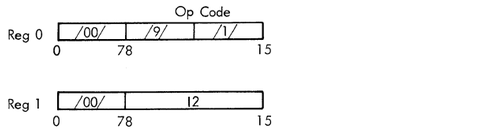


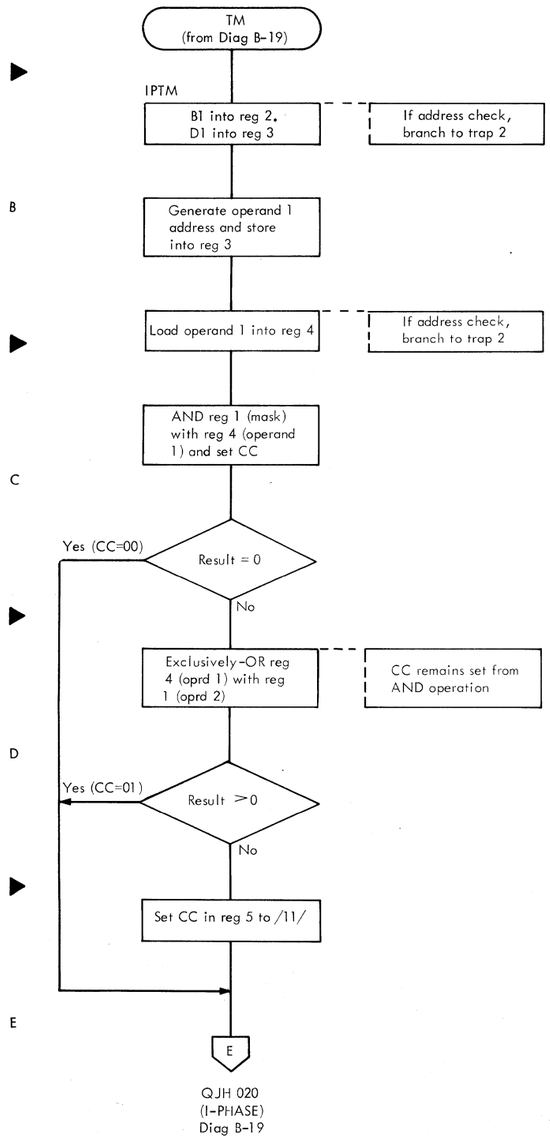
- **The first operand is compared with the second operand.**
- **The result is indicated in the condition code.**
- **I2 is the operand 2.**
- **B1 and D1 are the direct or effective main storage address of operand 1.**

The comparison is made with both operands in binary form.

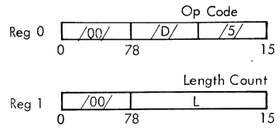
The condition code is made 00 if the operands are equal, 01 if the first operand is low compared with the second operand, and 10 if the first operand is high compared with the second operand.

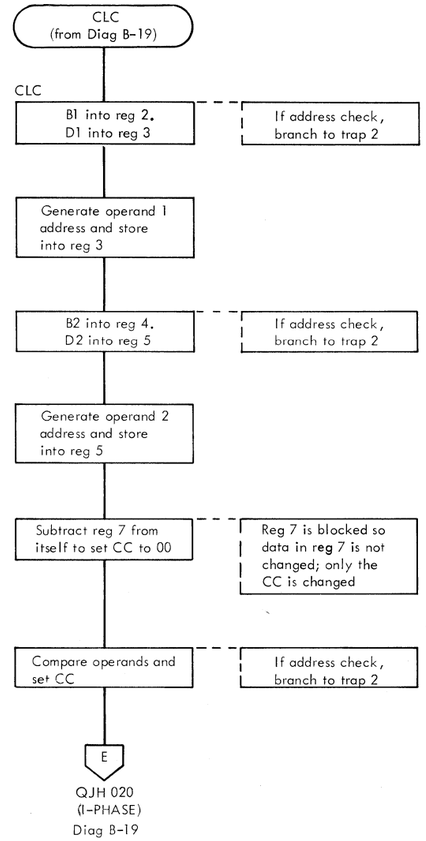
I-Phase and E-Phase for TM



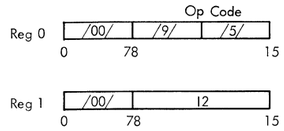


I-Phase and E-Phase for CLC





I-Phase and E-Phase for CLI



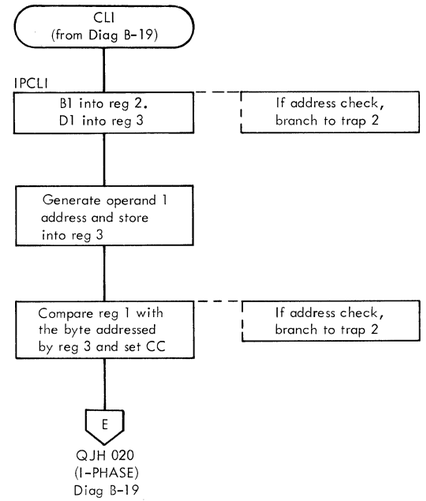
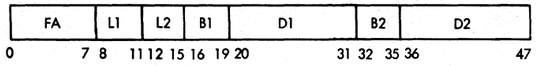


Diagram B-31. TM, CLC, and CLI I-Phase and E-Phase (03946) 2020 ≥ 50,000 EEMDM Vol 1 (2/69)

Add Decimal (AP), Decimal, SS Format



- **Objective: the second operand is added to the first operand and the sum is placed in the first operand location. Addition is algebraic, taking into account the sign and all digits of both operands.**
- **The sign of the result is determined by the rules of algebra. A zero sum is always positive.**
- **When high-order digits are lost because of overflow, a zero result has the sign of the correct sum.**
- **The first and second operand fields may overlap when their low-order bytes coincide. It, therefore, is possible to add a number to itself.**
- **L1 is the field length of operand 1.**
- **L2 is the field length of operand 2.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

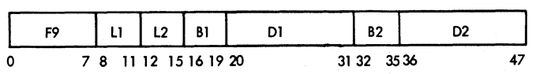
When the length of the second operand (L2) is greater than the length of the first operand (L1), a specification error stop occurs. The instruction is not executed.

All signs and digits are checked for validity. If necessary, high-order zeros are supplied for the second operand.

The condition code is set according to the result of the add decimal operation:

Result	*Condition Code*
Zero	0 0
Less than zero	0 1
Greater than zero	1 0
Overflow	1 1

Compare Decimal (CP), Decimal, SS Format



- **Objective: the first operand is compared with the second operand and the condition code indicates the comparison result.**
- **Comparison is right to left, taking into account the sign and all digits of both operands.**
- **L1 is the field length of operand 1.**
- **L2 is the field length of operand 2.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

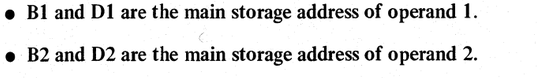
If the second operand field is shorter than the first operand field, the second operand field is extended with high-order zeros. A positive zero compares equally with a negative zero. Neither operand is changed as a result of the operation and overflow cannot occur. The first and second field may overlap when their low-order bytes coincide. It is, therefore, possible to compare a number with itself.

The compare decimal operation differs in several respects from compare logical. The compare decimal operation is processed right to left. Signs, zeros, and invalid characters are taken into account and fields are extended when unequal in length. Also, the field length is restricted to 16 eight-bit bytes, whereas the compare logical operation permits fields up to 256 bytes. When the length of the second operand (L2) is greater than the length of the first operand (L1), a specification error stop occurs. The instruction is not executed. All signs and digits are checked for validity.

The condition code is made 00 if the operands are equal, 01 if the first operand is low, and 10 if the first operand is high.

Note: Comparison is performed by subtracting operand 2 from operand 1. Since the operand 1 field must remain unchanged an auxiliary field in control storage is used for subtraction.

Zero and Add (ZAP), Decimal, SS Format

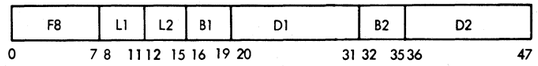


- **The second operand is placed in the first operand location.**
- **The operand is equivalent to an addition to zero.**
- **The sign code is made 1100 for positive results and 1101 for negative results in the binary coded decimal mode, and 1010 for positive results and 1011 for negative results in the USASCII mode.**
- **A zero result is always positive.**
- **L1 is the field length of operand 1.**
- **L2 is the field length of operand 2.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

Extra high-order zeros are supplied if needed. The first and second operand field may overlap when the rightmost byte of the first operand field is coincident with, or to the right of, the rightmost byte of the second operand.

When the length of the second operand (L2) is greater than the length of the first operand (L1), a specification error stop occurs. The instruction is not executed. The second operand is checked for valid sign and digit codes.

Subtract Decimal (SP), Decimal, SS Format



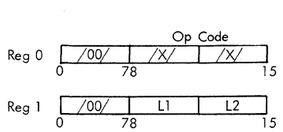
- **Objective: the second operand is subtracted from the first operand and the difference is placed in the first operand location.**
- **Subtraction is algebraic, taking into account the sign and all digits of both operands.**
- **L1 is the field length of operand 1.**
- **L2 is the field length of operand 2.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

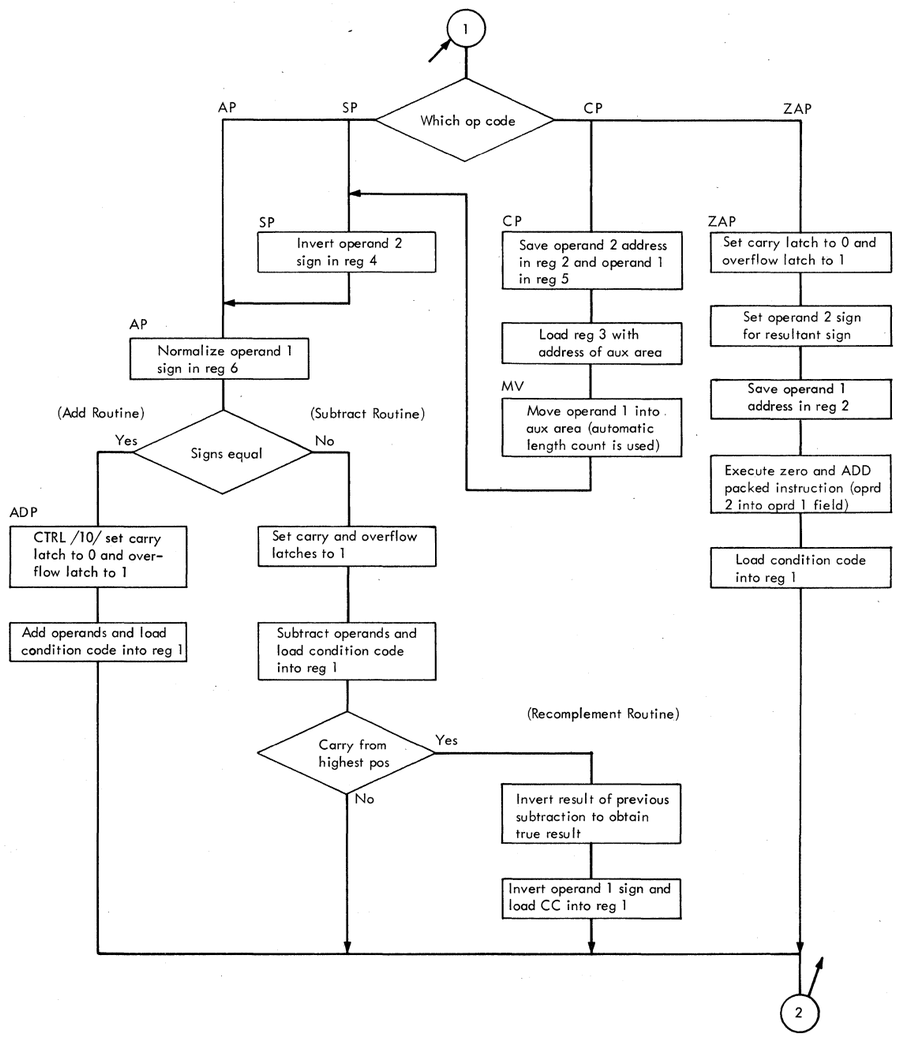
With the exception that the sign of the second operand is inverted prior to addition, the subtract instruction is identical to the add instruction. The sign of the result is determined by the rules of algebra. A zero difference is always positive. When high-order digits are lost because of overflow, a zero result has the sign of the correct difference.

The operands of a subtract operation may overlap when their low-order bytes coincide, even when their lengths are unequal. This property may be used to make an entire field or the low-order part of a field zero.

The condition code is set according to the result of the subtract decimal operation:

Result	*Condition Code*
Zero	0 0
Less than zero	0 1
Greater than zero	1 0
Overflow	1 1





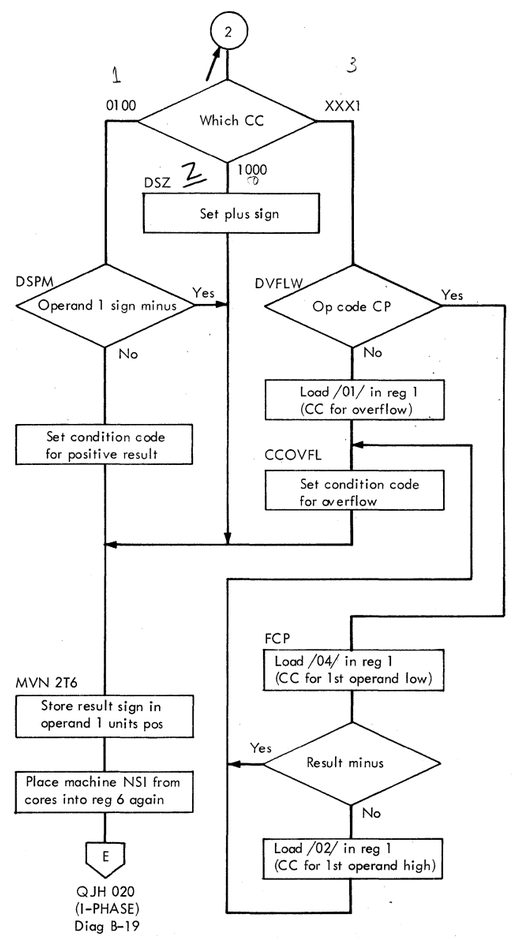
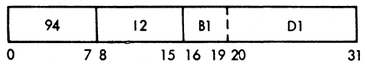


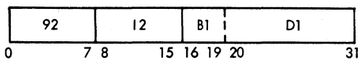
Diagram B-33. AP, SP, ZAP, and CP I-Phase and E-Phase (03948) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

AND (NI), Logical Data, SI Format



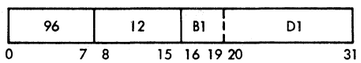
- **The logical product (AND) of the first and second operand bits is placed in the first operand location.**
- **I2 is an eight-bit pattern which is ANDed with the byte addressed by the operand 1 address.**
- **B1 and D1 are the direct or effective main storage address of operand 1.**

Move (MVI), Logical Data, SI Format



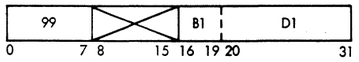
- **The second operand is placed in the first operand location.**
- **I2 is the operand 2.**
- **B1 and D1 are the direct or effective main storage address of operand 1.**

OR (OI), Logical Data, SI Format



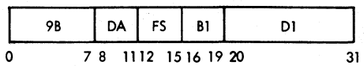
- **The logical sum (OR) of the first and second operand bits is placed in the first operand location.**
- **I2 is an eight-bit pattern which ORed with the byte addressed by the operand 1 address.**
- **B1 and D1 are the direct or effective main storage address of operand 1.**

Halt and Proceed (HPR), Logical Data, SI Format



- **Stops the CPU for customer control purposes.**
- **Bits 8 through 15 are ignored.**
- **B1 and D1 are the direct or effective address and are located in DR-A, S, T, R when the CPU stops.**

Control I/O (CIO), Logical Data, SI Format

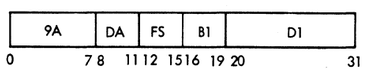


The DA specifies the I/O device in which a control function is to be performed.

The FS specifies the particular component (it may also specify the primary function of that component) in the I/O device addressed.

A detailed specification of the control function to be performed is derived from the contents of the B1-D1 fields according to the rules for direct or effective address generation. If the detailed specification derived from the B1-D1 field is all zero, a no-operation occurs.

Test I/O and Branch (TIOB), Logical Data, SI Format



The DA specifies the I/O device in which a condition is to be tested.

The FS specifies the particular condition or indicator to be tested in the I/O device addressed.

If the condition tested in the addressed I/O device is on, the updated instruction address is replaced by the branch address derived from the B1-D1 fields; otherwise, normal instruction sequencing continues with the updated instruction address.

Note 1: When branching to the special I/O E-Phase, the contents of the local store are as follows:

Reg	XIO	CIO	TIOB
0	/0035/ (53)	/0000/ (0)	/FFFF/ (-1)
1	DA/FS*	DA/FS*	DA/FS*
2	-	-	-
3	D1 + (B1)	D1 + (B1)	D1 + (B1)
4	Address checked	Not checked	Address checked
5	D2 + (B2) checked for positive	-	-
6	Macro IAR	Mdcro IAR	Macro IAR

* The DA/FS is right aligned, the high-order byte being zero (bits 8-11: DA; bits 12-15: FS)

Note 2: Return from Special I/O E-Phase

The following entry points are provided:

IPHASE — Proceeds with next I-phase taking the contents of register 6 as instruction address. In the case of CIO and TIOB, no branch, register 6 has to be left unchanged. In the case of TIOB, branch, the contents of register 3 or 4 have to be moved into register 6.

MVH 6, 3

REPEAT — The previous macro instruction is repeated (that is, the I-phase is entered with the contents of IRECAL in register 6). To be used for CPU interlock in the case of an I/O-busy condition.

AVAIL — Tests time-sharing switch, sets condition code to 0 and proceeds with next I-phase. Register 6 must be unchanged. Return of XIO, available.

WORKIN — Sets condition code to 1 and proceeds with next I-phase. Register 6 must be unchanged. Return of XIO, working.

NOTOP — Sets condition code to 3 and proceeds with next I-phase. Register 6 must be unchanged. Return of XIO, not operational.

SETCC — May be used to set the condition code with a value preloaded in register 0. Next I-phase is entered. Register 6 must be unchanged.

SPECER — Sets I-register on CPU console to 6 (specification error) and performs an error stop.

PROGER — Displays the value of bits 4-7 of register 0 in the I-register on the CPU console and performs an error stop. Register 0 has to be previously loaded by means of an

IBL 0, display

with the appropriate error code (see B-14). This entry is used for any program check condition other than 6.
than 6.

PRGCL 1 — 2501 'log' routine

PRGCL 2 — 2560/2520 'log' routine

PRGCL 3 — 1442 'log' routine

PRGCL 4 — 2203/1403 'log' routine

The 'log' routine requires register 0, containing the modified op code, to be left unchanged, and assumes the address of the next macro instruction being always in register 6. In the case of a successful TIOB instruction, the exchange of the instruction address (MVH 6, 3) is determined by special I/O E-phase. At its end, the 'log' routine branches either to IPHASE (no setting of condition code, in case of TIOB) or to NOTOP (condition code 3, in the case of XIO).

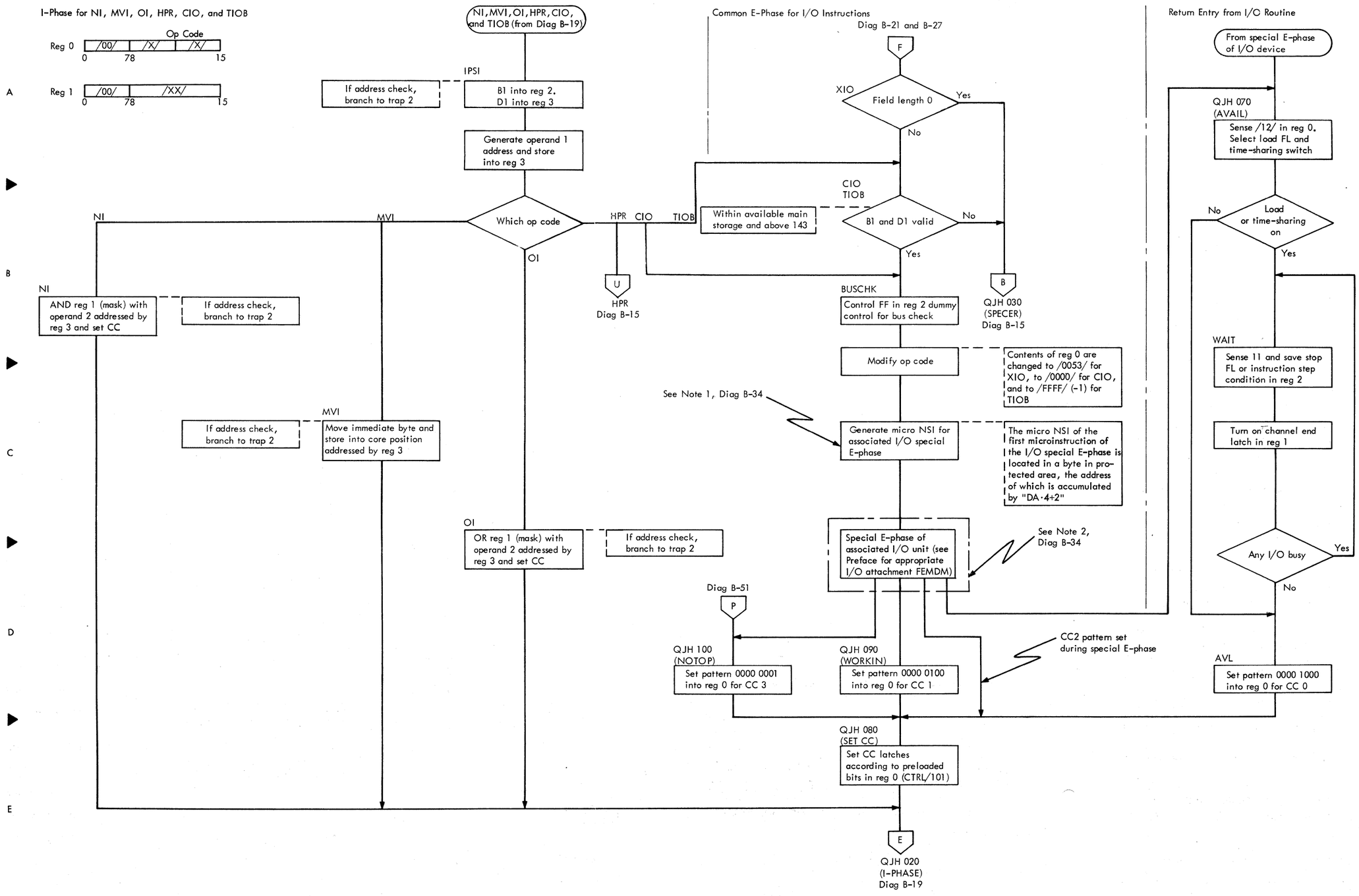
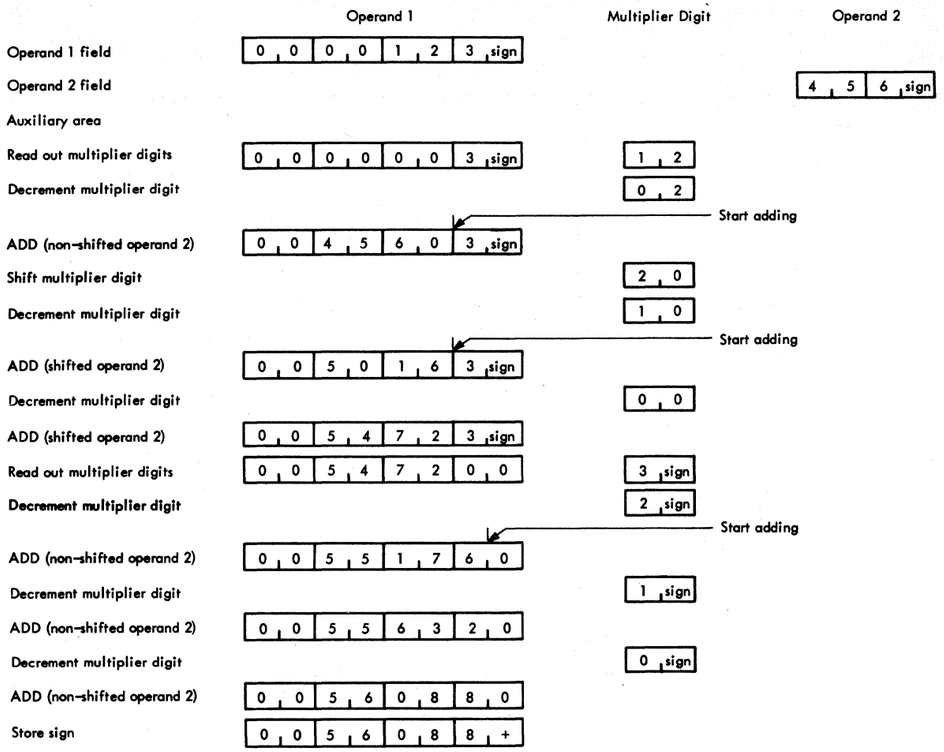


Diagram B-35. NI, MVI, OI, HPR, CIO, and TIOB I-Phase, Common E-Phase for I/O Instructions, and Return Entry from I/O Routine (03950)

MULTIPLICATION EXAMPLE: 123+●456+



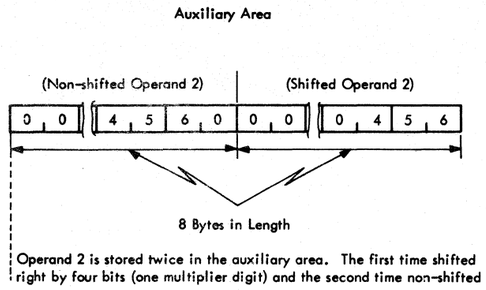
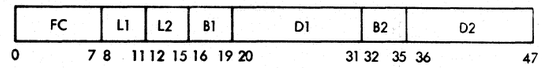


Diagram B-36. Multiplication Example (03951) 2020≥50,000 FEMDM Vol 1 (2/69)

Multiply Decimal (MP), Decimal, SS Format



- **Objective: the product of the multiplier (second operand) and the multiplicand (first operand) replaces the multiplicand.**
- **L1 is the field length of operand 1.**
- **L2 is the field length of operand 2.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**
- **All operands and results are treated as signed integers, right-aligned in their field.**
- **The sign of the product is determined by the rules of algebra from the multiplier and multiplicand signs, even if one or both operands are zero.**

Since the number of digits in the product will be the sum of the number of digits in the operands, the multiplicand must have high-order zero digits for at least a field size which equals the multiplier size, otherwise a data error occurs. This definition of the multiplicand field ensures that no product overflow can occur. The maximum product size is 30 digits. At least one high-order digit of the product field will be zero. The multiplier and product fields may overlap when their low-order bytes coincide.

When the multiplicand does not have the desired number of leading zeros, multiplication may be preceded by a zero-and-add operation into a larger field.

Program Error Checking

The multiplier size is limited to 15 digits and a sign, and must be less than the multiplicand size. If the length code L2 is larger than seven, or larger than or equal to the length code L1, the operation is not executed and a specification error stop occurs.

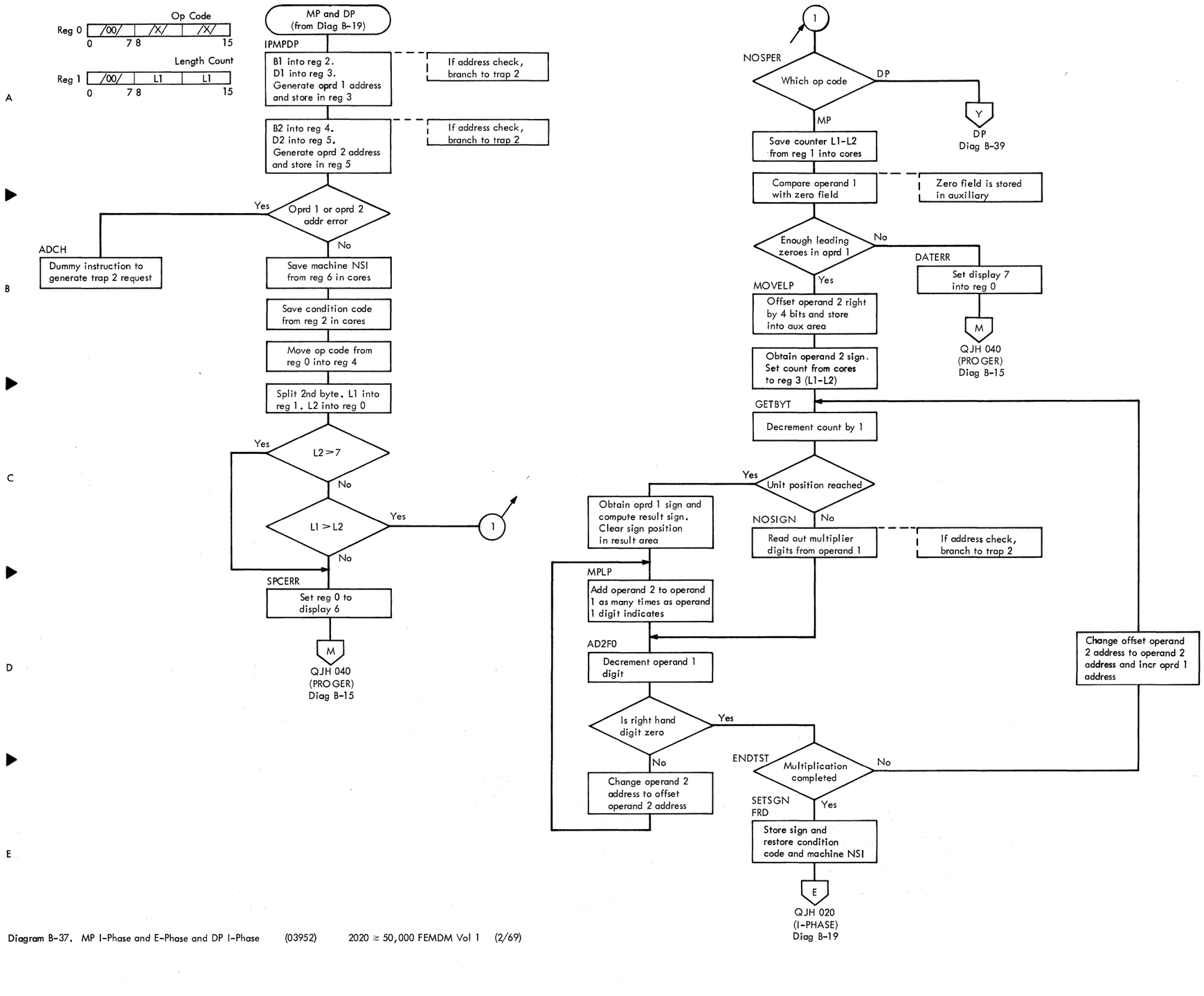


Diagram B-37. MP I-Phase and E-Phase and DP I-Phase (03952) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

DIVIDE EXAMPLE: 1 2 3 4 5 6: 5 8 2

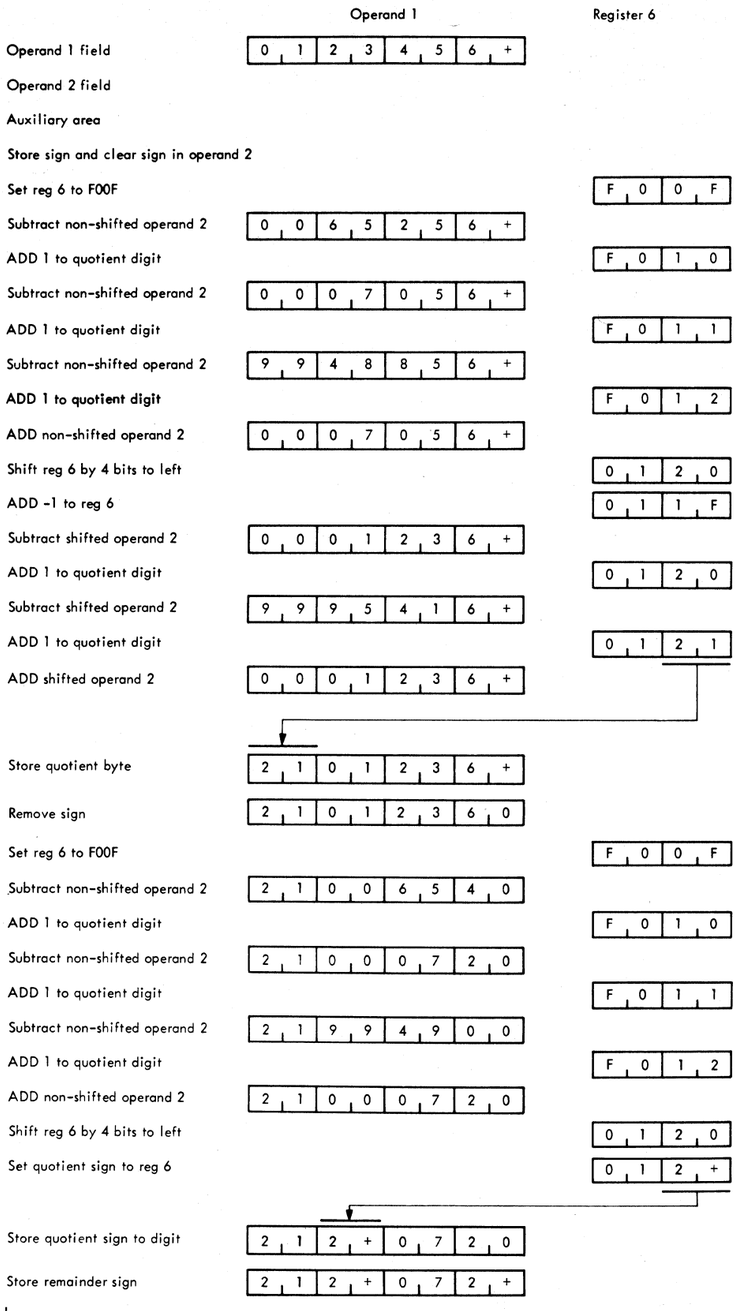
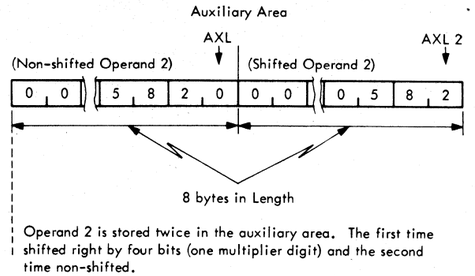
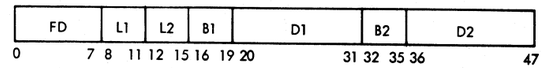


Diagram B-38. Divide Example (03953) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)



Operand 2 is stored twice in the auxiliary area. The first time shifted right by four bits (one multiplier digit) and the second time non-shifted.

Divide Decimal (DP), Decimal, SS Format



- **Objective: the dividend (first operand) is divided by the divisor (second operand) and replaced by the quotient and remainder.**
- **The dividend, divisor, quotient, and remainder are signed integers, right-aligned in their fields.**
- **The sign of the quotient is determined by the rules of algebra from dividend and divisor signs.**
- **The remainder has the same sign as the dividend.**
- **The foregoing rules are true even when quotient or remainder is zero.**
- **L1 is the field length of operand 1.**
- **L2 is the field length of operand 2.**
- **B1 and D1 are the main storage address of operand 1.**
- **B2 and D2 are the main storage address of operand 2.**

The quotient field is placed leftmost in the first operand. The remainder field is placed rightmost in the first operand field and has a size equal to the divisor size. Together, the quotient and remainder occupy the entire dividend field. Therefore, the address of the quotient field is the address of the first operand. The size of the quotient field in eight-bit bytes is L1 less L2, and the length code for this field is one less (L1 − L2 − 1). The divisor and dividend fields may overlap only if their low-order bytes coincide.

The maximum dividend size is 30 digits and a sign. Since the smallest remainder size is one digit and a sign, the maximum quotient size is 29 digits and a sign.

The condition for a divide check can be determined by a trial subtraction. The leftmost digit of the divisor field is aligned with the leftmost-but-one digit of the dividend field. When the divisor, so aligned, is less than or equal to the dividend, a quotient overflow is indicated.

Program Error Checking

The operation is not executed and a specification error stop occurs, when the divisor length code is larger than seven, or larger than or equal to the dividend length code.

A divide check occurs if the quotient is larger than the allowable number of digits or if the dividend does not have at least one leading zero. In that case, the operation is not executed and a decimal divide error stop occurs. Divisor and dividend remain unchanged in their storage locations.

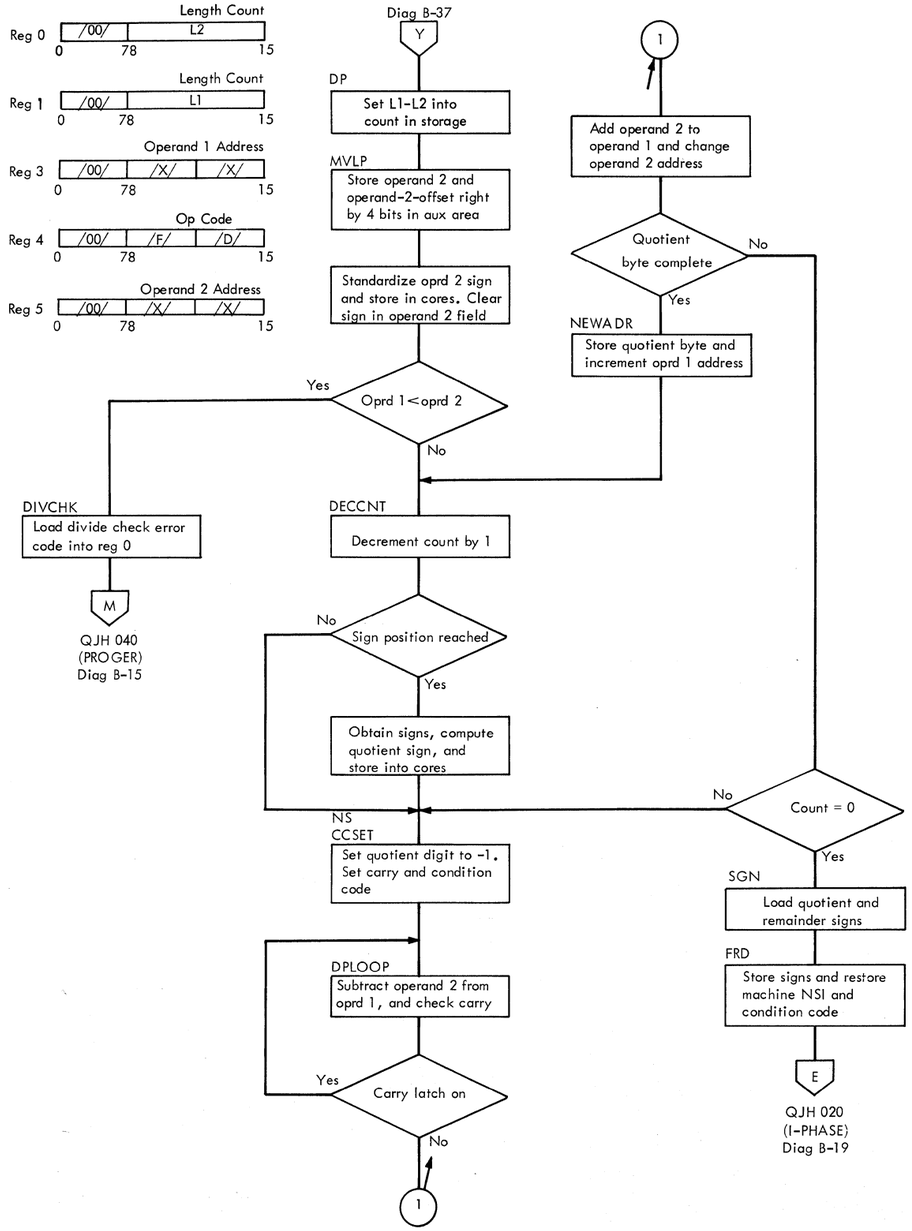
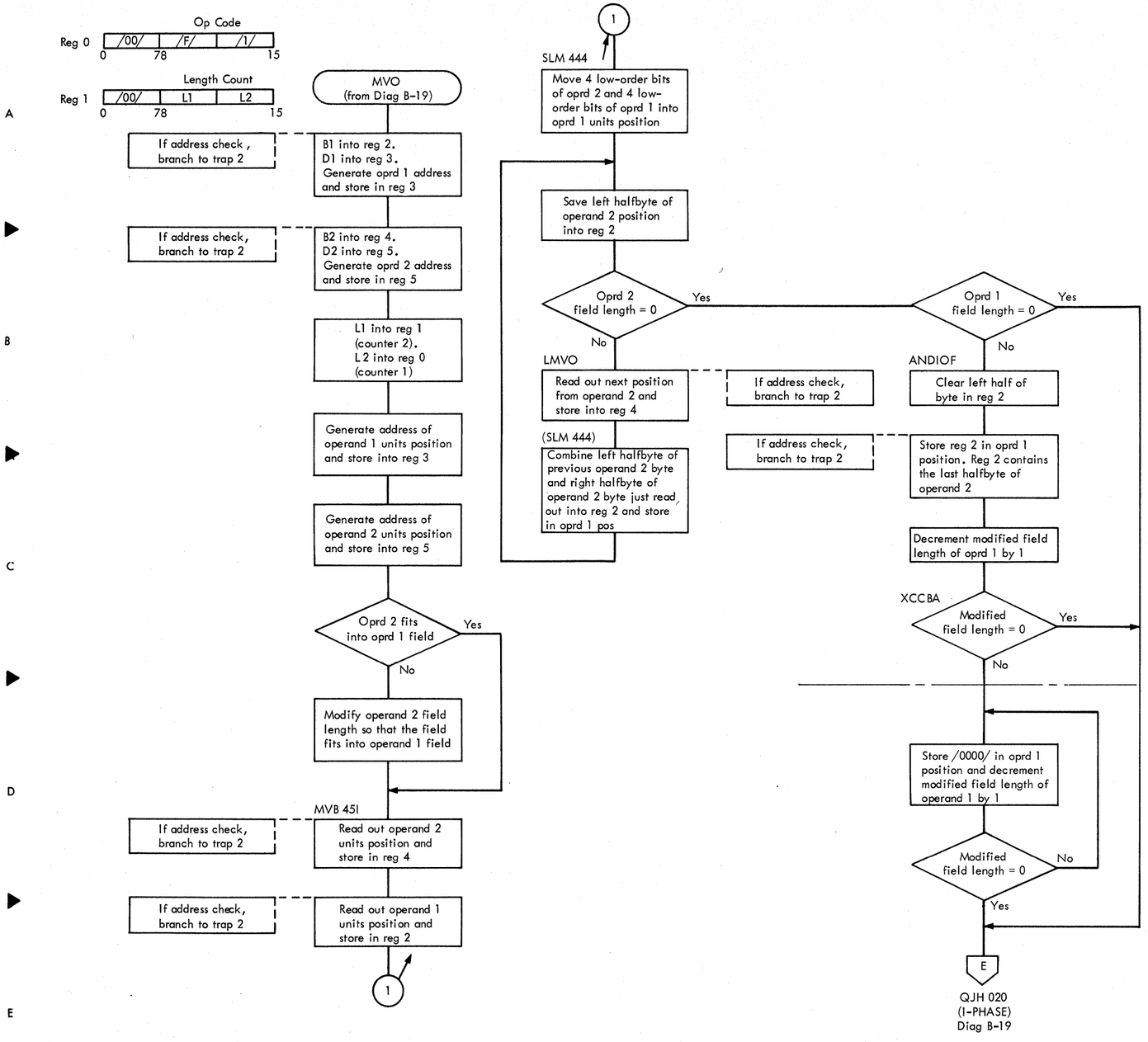
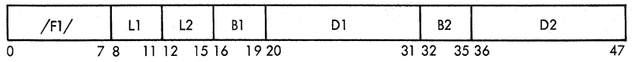


Diagram B-39. DP E-Phase (03954) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)



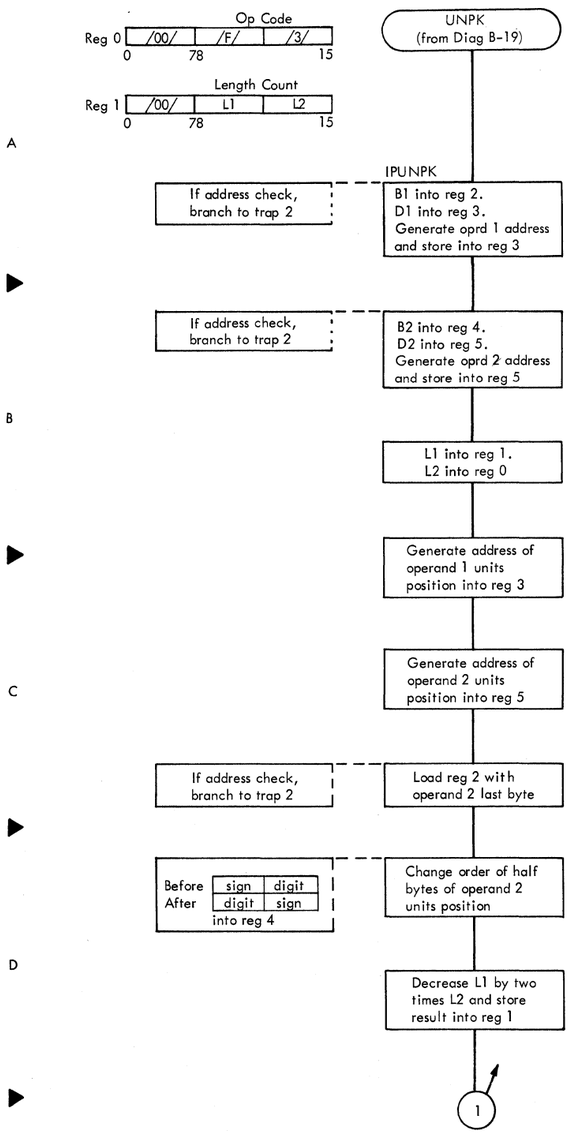
Move with Offset (MVO), Decimal, SS Format

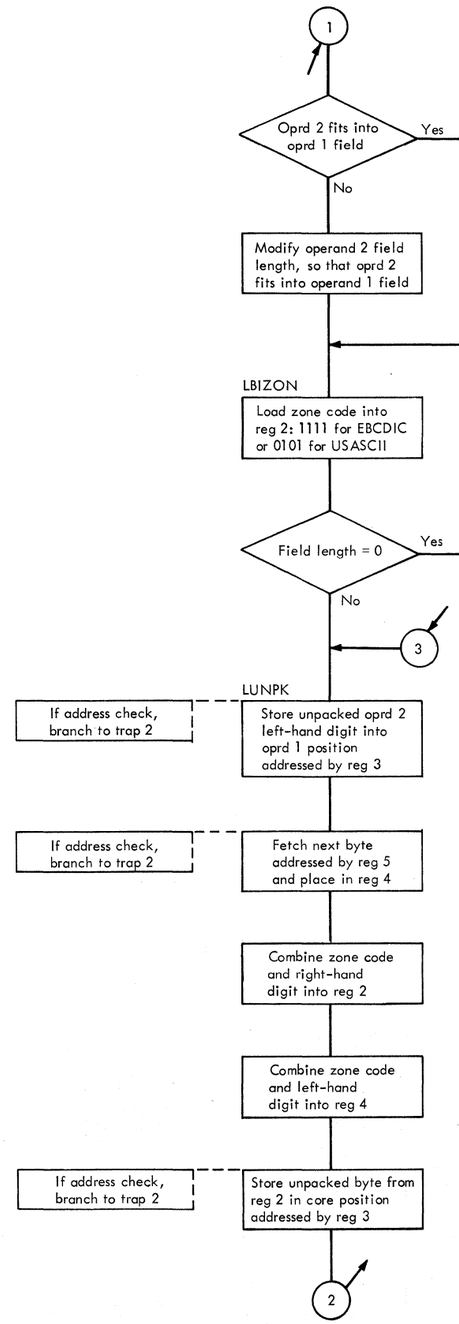


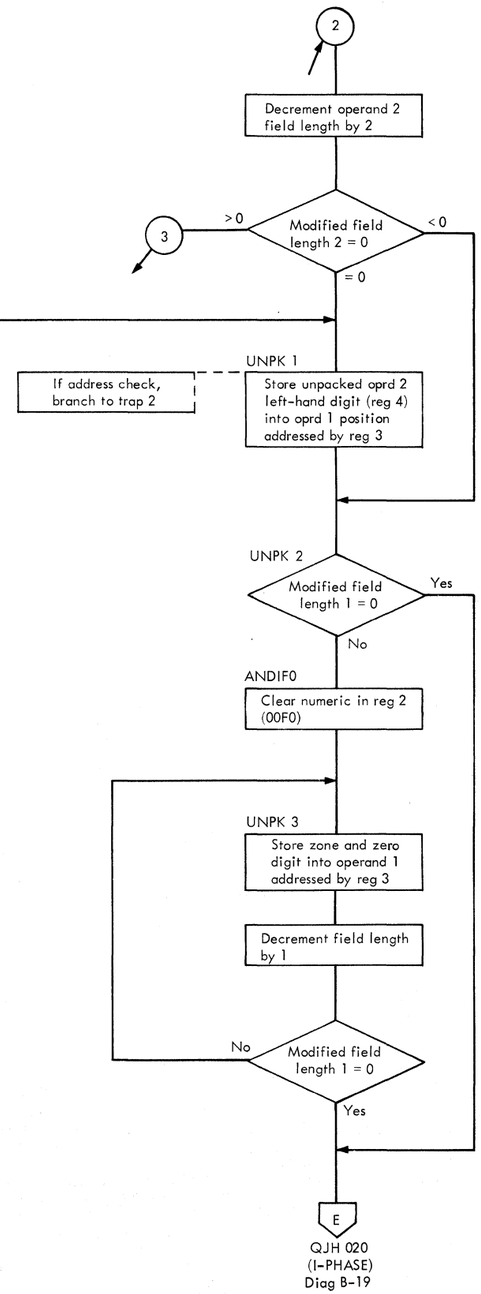
- Objective: the four low-order bits of the first operand are attached as low-order bits to the second operand, the second operand bits are offset by four bit positions, and the result is placed in the first operand location.
- L1 is the field length of operand 1.
- L2 is the field length of operand 2.
- B1 and D1 are the main storage address of operand 1.
- B2 and D2 are the main storage address of operand 2.

The move operation consists of placing the second operand to the left of, and adjacent to, the four low-order bits of the first operand. The fields are processed right to left. If necessary, the second operand is extended with high-order zeros. If the first operand field is too short to contain all bytes of the second operand, the remaining information is ignored. Overlapping fields may occur and are processed by storing a result byte as soon as the necessary operand bytes are fetched.

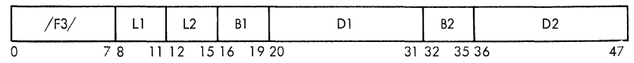
Diagram B-41. MVO I-Phase and E-Phase (03955) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)







Unpack (UNPK), Decimal, SS Format

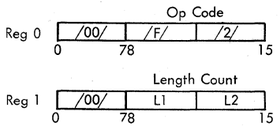


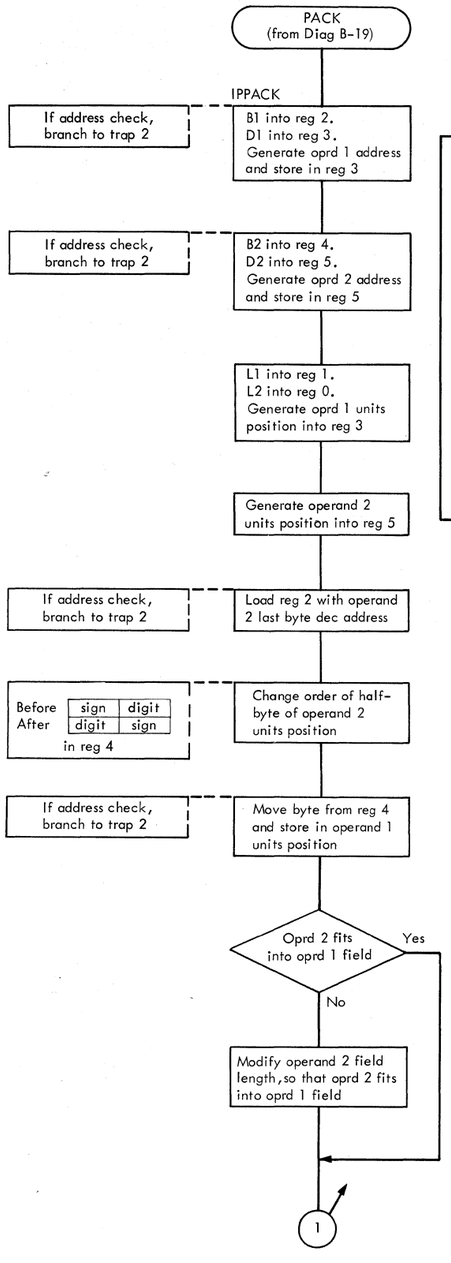
- Objective: the format of the second operand is changed from packed to zoned, and the result is placed in the first operand location.
- L1 is the field length of operand 1.
- L2 is the field length of operand 2.
- B1 and D1 are the main storage address of operand 1.
- B2 and D2 are the main storage address of operand 2.

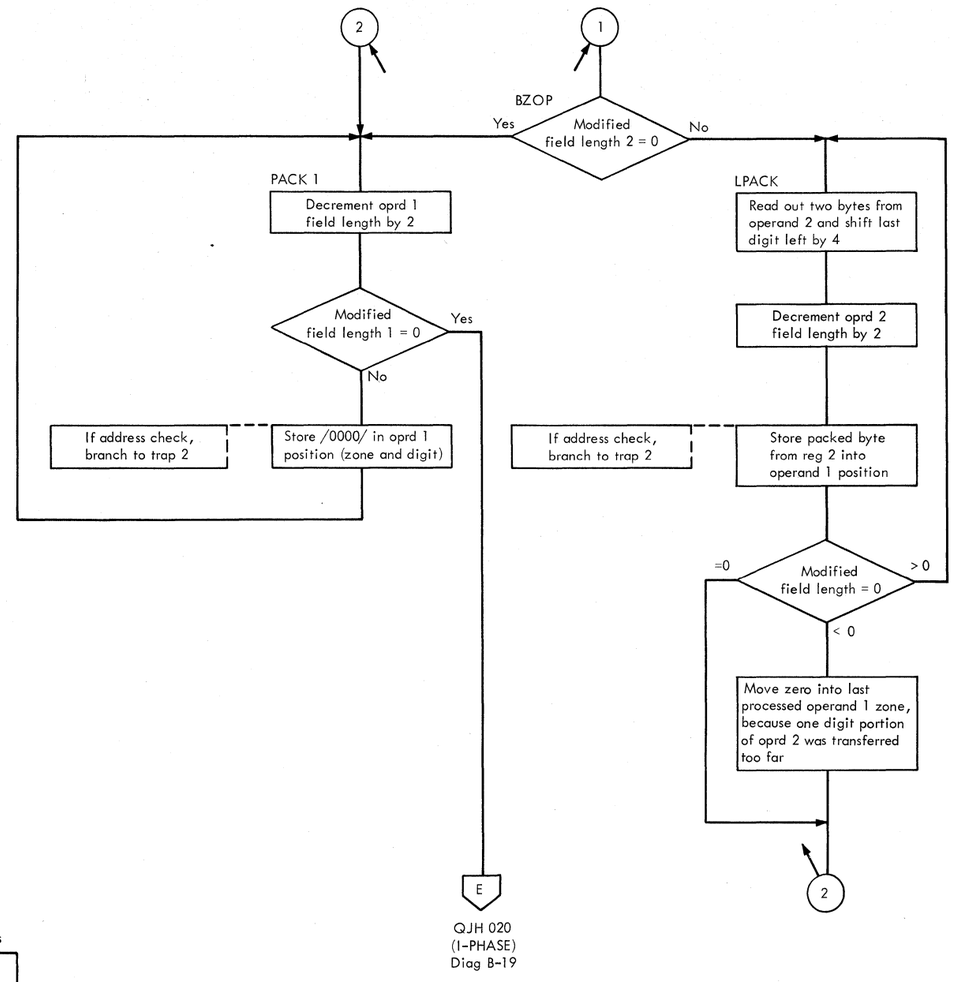
The digits and sign of the packed operand are placed unchanged in the first operand location, using the zoned format. Zones with coding 1111 in the binary coded mode and coding 0101 in the USASCII mode are supplied for all bytes except the low-order byte, which receives the sign of the packed operand.

The fields are processed right to left. High-order zero characters are supplied if the second operand needs extension. If the first operand field is too short to contain all significant digits of the second operand, the remaining digits are ignored. The first and second operand fields may overlap and are processed by storing a result byte immediately after the necessary operand byte is fetched.

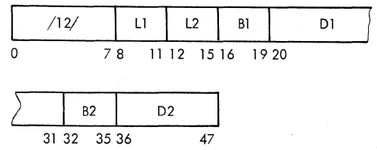
Diagram B-43. UNPK I-Phase and E-Phase (03956)







Pack (PACK), Decimal, SS Format

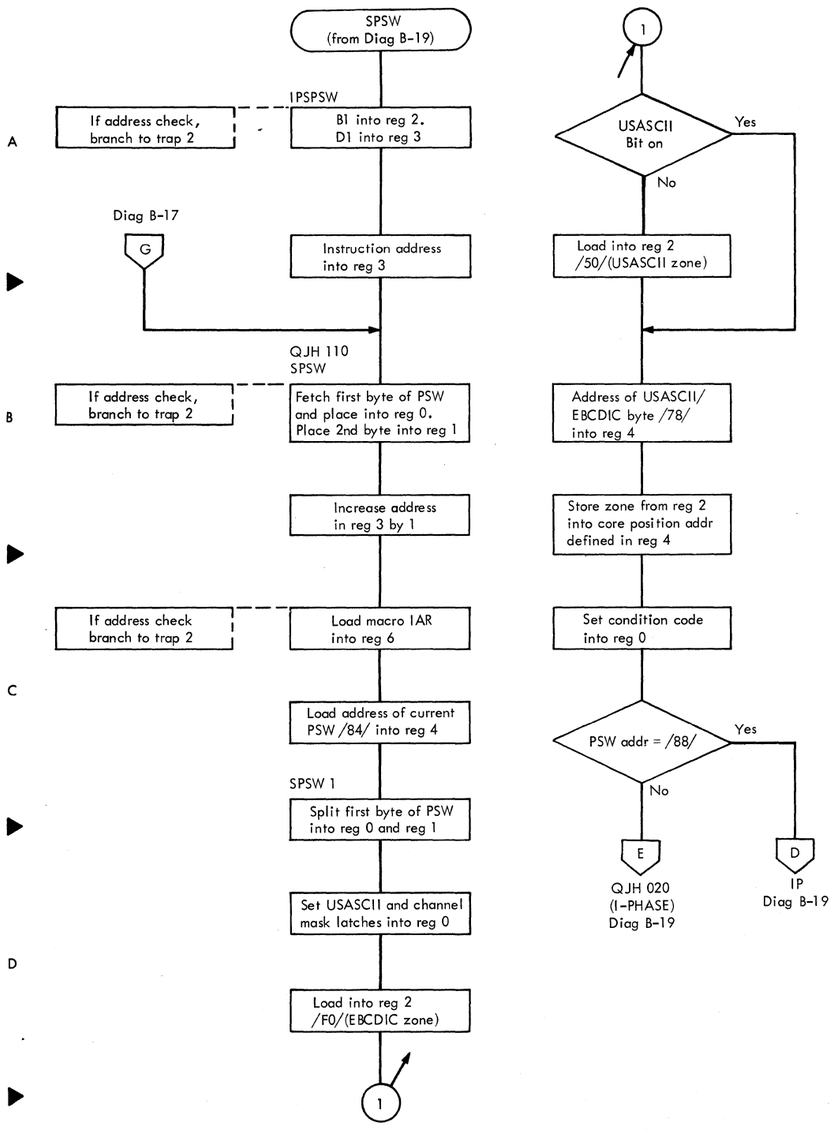


- Objective: the format of the second operand is changed from zoned to packed, and the result is placed in the first operand location.
- L1 is the field length of operand 1.
- L2 is the field length of operand 2.
- B1 and D1 are the main storage address of operand 1.
- B2 and D2 are the main storage address of operand 2.

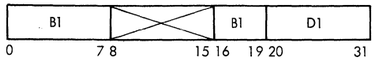
The second operand is assumed to have the zoned format. All zones are ignored except the zone over the low-order digit, which is assumed to represent a sign. The sign is placed in the four rightmost bits of the low-order byte, and the digits are placed adjacent to the sign and to each other in the remainder of the result field.

The fields are processed right to left. If necessary, the second operand is extended with high-order zeros. If the first operand field is too short to contain all significant digits of the second operand field, the remaining digits are ignored. Overlapping fields may occur and are processed by storing each result byte immediately after the necessary operand bytes are fetched.

Diagram B-45. PACK I-Phase and E-Phase (03957) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)



Set PSW (SPSW), Branch, SI Format



- The 32-bit word (four eight-bit bytes), located in main storage with the leftmost byte at the first operand address, replaces the PSW.
- The op code is /81/ (1000 0001).
- Bits 8 through 15 are ignored.
- B1 and D1 are the direct or effective main storage address of the leftmost byte of a located PSW.

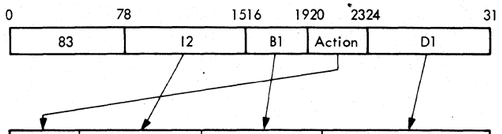
The set-PSW instruction is equivalent to a branch operation.

When an input/output interrupt occurs, the PSW is stored in main storage locations 144/147 and a new PSW is obtained from main storage locations 148-151.

The PSW has a fixed-length format of one word. It is located in an unaddressable (by machine program) register in the CPU (auxiliary storage positions 20, 21, 30, and 31) and is employed as an internal control.

Diagram B-47. SPSW I-Phase and E-Phase (03958) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

Diagnostic Operation Format



Action	I2 (8 Bits)	B1 (4 Bits)	D1 (8 Bits)
0	May be used as parameter	Number of GPR containing branch address to microprogram	May be used as parameter
2	Value of increment	Not used	Address of counter (displacement in block C1)
3	Not used	Not used	Not used
4,5	Length of area to be fetched -1 (max 64 bytes)	Not used	Address of area to be fetched (displacement in block C1 or C2)
6,7	Length of area to be cleared -1 (max 256 bytes)	Not used	Address of area to be cleared (displacement in block C1 or C2)

Action 0: Provides a branch to a special microprogram routine. This routine (E-phase) is not in the control program but has to be coded individually for the various diagnostic programs in the customer storage area. The diagnostic operation, action 0, only provides the parameters for the linkage to the microprogram and the return to the macro (Model 20) program. This action only works with the usemeter switch in CE mode otherwise it is treated as invalid op code.

Action 1: Is not used (no operation).

Action 2: Increments a counter inside the log area (that is, in block C1). The counter is one halfword wide and has to be located on a halfword boundary.

Action 3: Stores the value of the customer console switches to a fixed location in main storage. It will be a no operation if the mode switch is at ADDRESS STOP.

Action 4: Moves a desired part of the 'log' area in block C1 into the fixed storage location /0178/. This action is used for log-out editing.

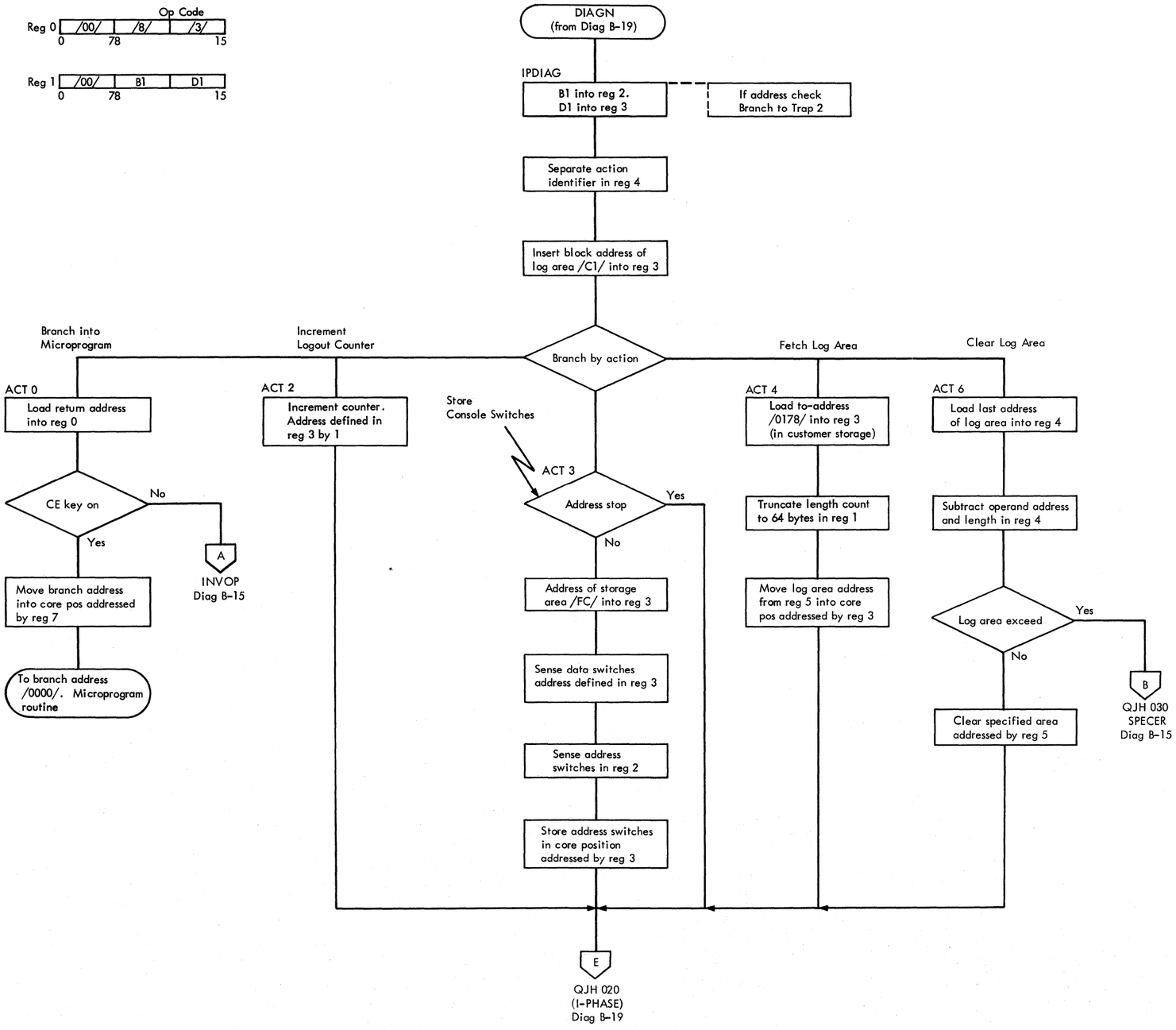
Action 5: Does the same with the 'log' area portion in block C2 as action 5 does with the 'log' area in block C1.

Action 6: Clears a desired part of the 'log' area in block C1.

Action 7: Clears a desired part of 'log' area in block C2.

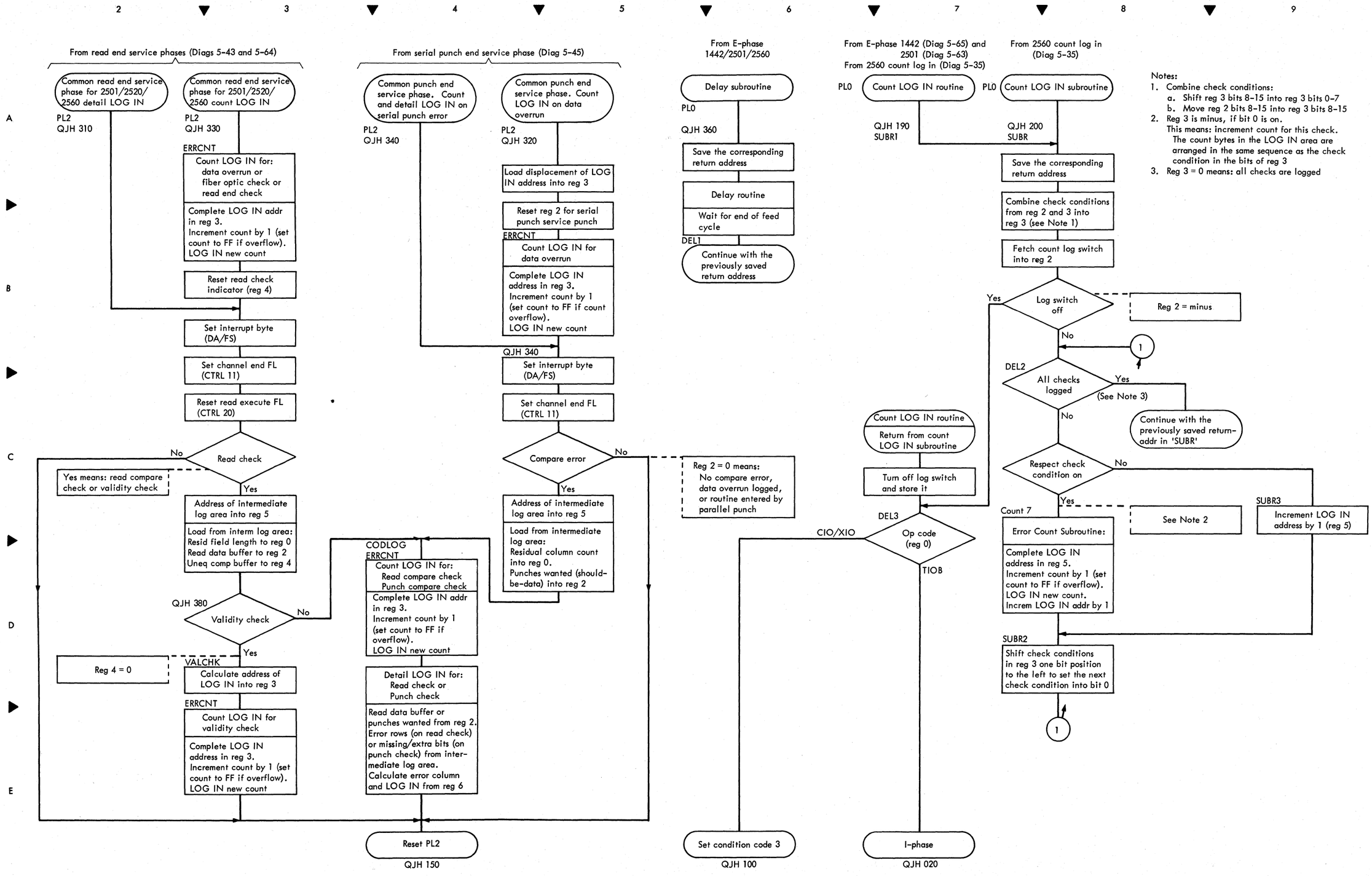
Note: In actions 4 through 7 any displacement within block C1 or C2 may be addressed with a maximum length of 256 bytes. In actions 6 and 7 the area to be cleared is checked to determine that it does not exceed the 'log' area. If it does, nothing is cleared and a specification check occurs.

2 3 4 5 6 7 8 9



A B C D E

Diagram B-49. DIAGN 1-Phase and E-Phase (03960)



● Diagram B-51. Flowchart: Common Read/Punch End Service Phase with LOG IN, Delay Subroutine for E-Phases, and Cont LOG IN Routine and Subroutine (04341)

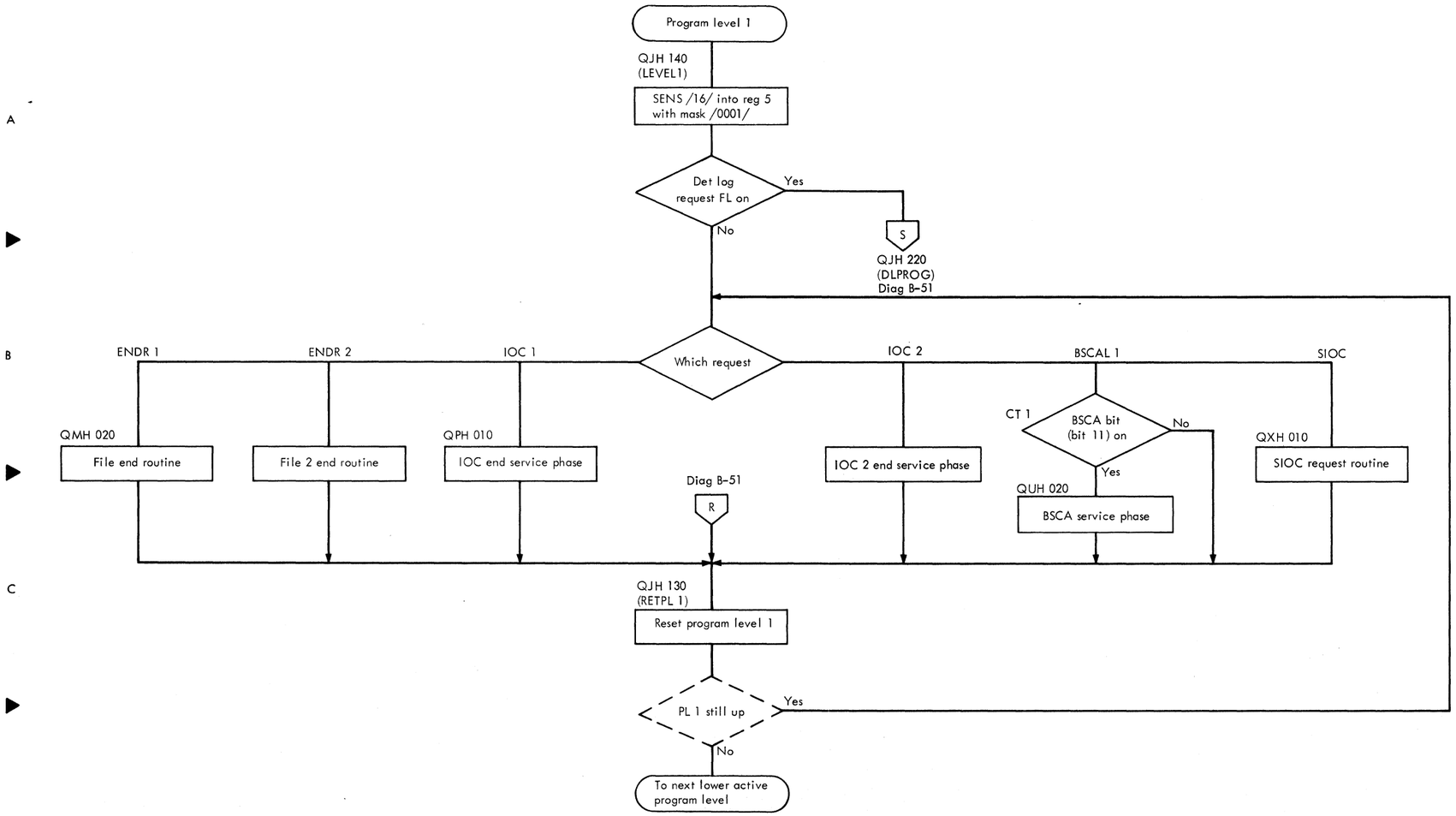
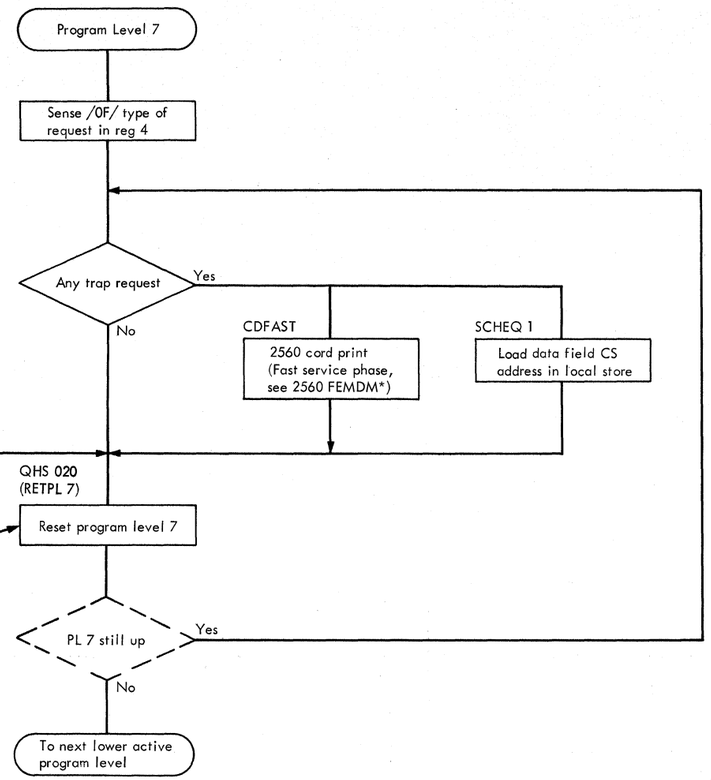


Diagram B-55. Program Level 1 Common Trap Routine (03962) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)



* See Preface for appropriate FEMDM Form Number

Diagram B-57. Program Level 7 Common Trap Routine (03963) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

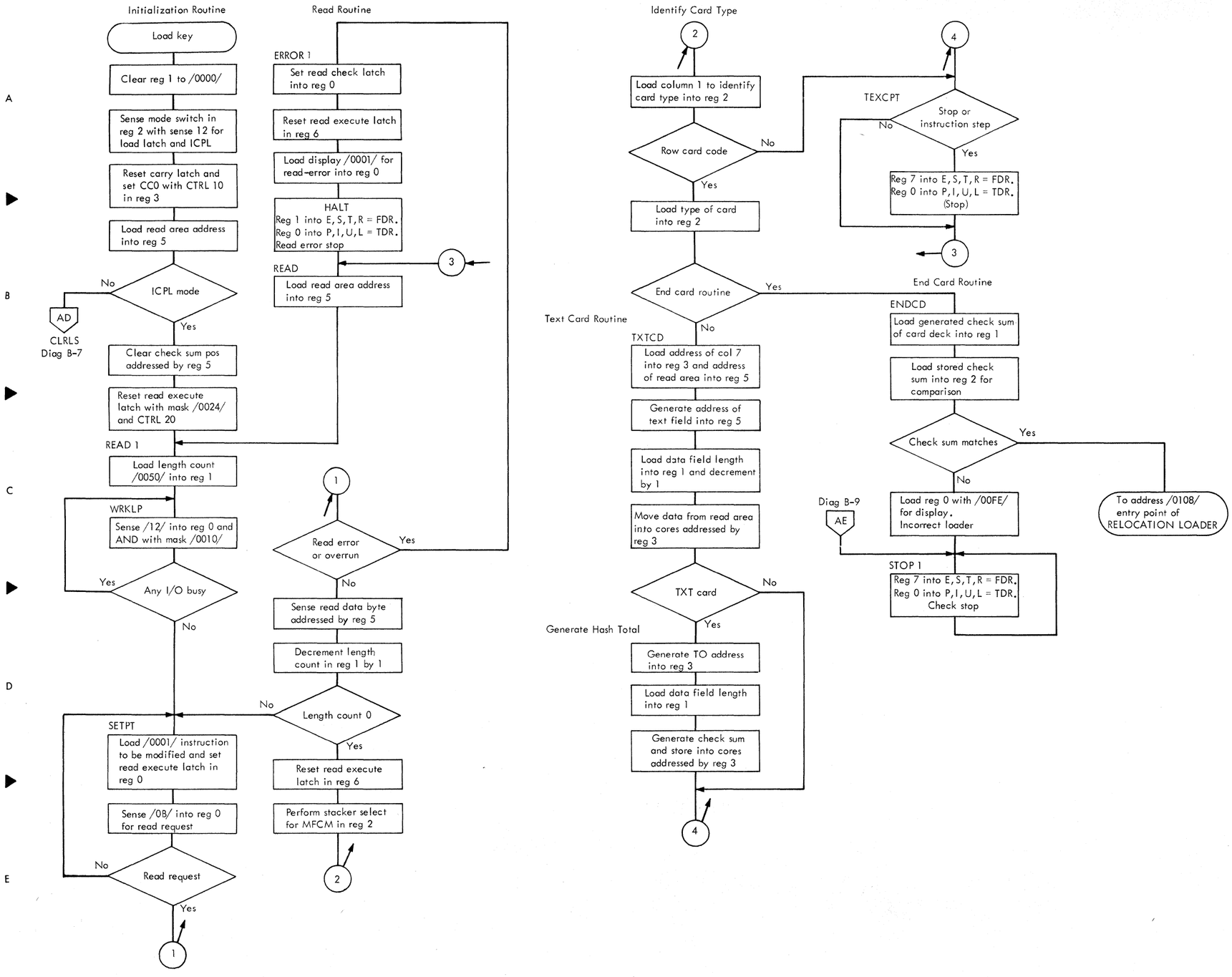


Diagram B-59. Absolute Loader (03964) 2020 ≥ 50,000 FEMDM Vol 1 (2/69)

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2020 Processing Unit System/360 Model 20 (Machines with serial no. 50,000 and above)

This supplement provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

Front Cover	4-39, 4-40
Title page, ii	4-42, 4-44
iii, iv	4-46, 4-48
vii	4-52, 4-54
2-3, 2-4	4-60, 4-62
3-1, 3-2	4-64
4-4, 4-10	B-1 (Part 2)
4-16, 4-18	B-3, B-5 (Part 1)
4-20, 4-22	B-5 (Part 2), B-6
4-32, 4-34	Reader's Comment, Business Reply
4-36, 4-38	Back Cover

A change to the text or a small change to a diagram is indicated by a vertical line to the left of the change; a changed or added diagram is denoted by the symbol • to the left of the caption.

Summary of Amendments

1. Implementation of interconnecting signals of 2020 Processing Unit and 1401/1440 Compatibility feature.
2. Extension of system data flow by the Native Tape Attachment feature (NTA).
3. Re-organization of the protected area layout.
4. Form numbers are re-coded.

Note: Please file this cover letter at the back of the manual to provide a record of changes.

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iii, iv
2-1 through 2-7
3-1, -2
4-1 through 4-48
4-52 - 4-64
4-99
B-49, -51

Changed Diagrams are denoted by the symbol • to the left of the caption. In some instances, Diagrams have been reissued which contain only editorial (i.e. non-technical) changes; these diagrams are not indicated by the symbol.

Summary of Amendments: Changes reflect latest engineering change level.

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