IBM Field Engineering

Maintenance Diagrams

2025 Processing Unit

Y24-3529-0

Form Y24-3529-0
FES Y24-0094

Preface

The IBM System/360 Model 25 FEMDM is intended as a quick-recall document for use in the field. The manual consists of the following sections.

1. Diagnostic Technique Diagrams
   These diagrams give a generalized approach to troubleshooting problems on the System/360 Model 25.
3. Data Flow Diagrams
   These diagrams show the system data flow and identify the major components of the system.
4. Functional Units Diagrams
   The functional units diagrams are positive logic diagrams of the CPU, Integrated Units, File, and Channel circuits. These diagrams show logical operation of circuits without regard to signal level, although actual ALD line names are used.
5. Operational Diagrams
   The operational diagrams describe some of the basic operations performed by the System/360 Model 25 and its integrated attachments.

Immediately following the table of contents is a reference list of lights, switches, and latches used in the System/360 Model 25.

References to the System/360 Model 25 FEMDM are made from the following manuals.

System/360 Model 25 Processing Unit FETOM, Form Y24-3527.

System/360 Model 25 Processing Unit Integrated 2540 Attachment FETOM, Form Y24-3532.

System/360 Model 25 Processing Unit Integrated 1403 Attachment FETOM, Form Y24-3533.

System/360 Model 25 Processing Unit Integrated 2311 Attachment FETOM, Form Y24-3534.

System/360 Model 25 Processing Unit Channel FETOM, Form Y24-3531.

System/360 Model 25 Processing Unit FE Maintenance Manual, Form Y24-3528.

First Edition (October, 1968)

Significant changes or additions to the specifications contained in this publication are continually being made. Any such changes will be reported in subsequent revisions or FE Supplements.

This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. 171, P.O. Box 6, Endicott, N.Y. 13760. A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be sent to the above-mentioned address.

Form Y24-3529-0
FES Y24-0506

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Operational Diagrams

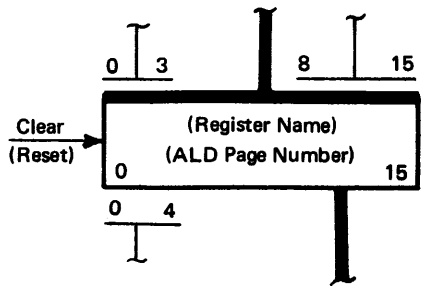
1400 MODE

LOCATION OF LIGHTS AND SWITCHES

LOCATION OF LATCHES AND TRIGGERS

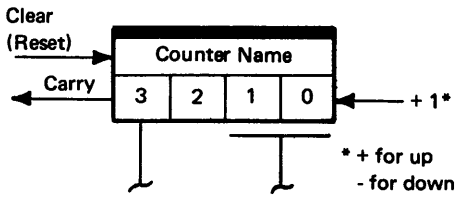
LEGEND

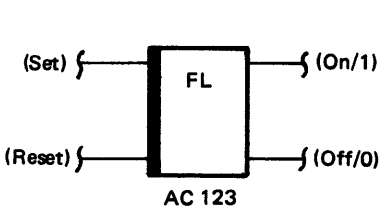
1. LOGIC DIAGRAMS



Register, Counter

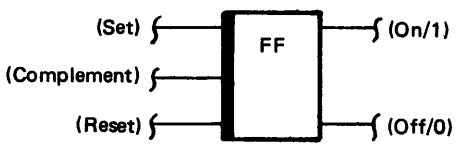
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.





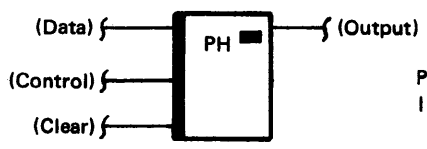
Flip Latch

Input side is denoted by thick line. Circuit multiples shown by numeral in lower right corner. ALD reference page may be shown beneath.

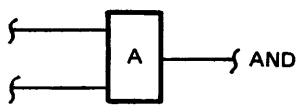


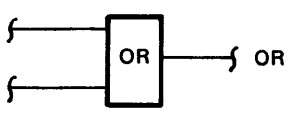
Flip-Flop

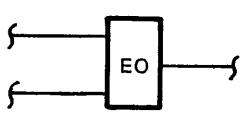
Input side is denoted by thick line. Shift signal is shown by a P or N.



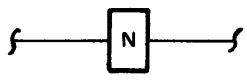
Polarity Hold
Input side is denoted by thick line.



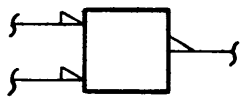




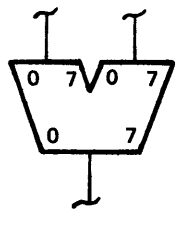
Exclusive OR



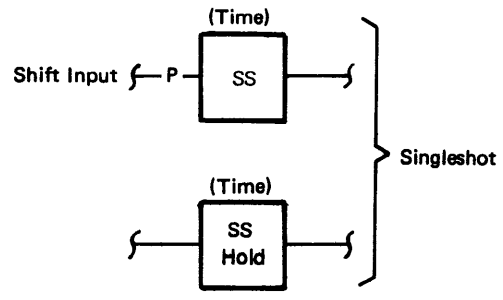
Negator (Inverter)

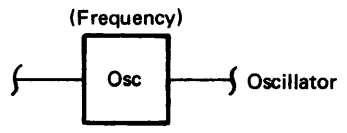


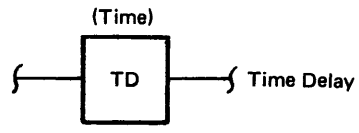
Negative Polarity Wedge



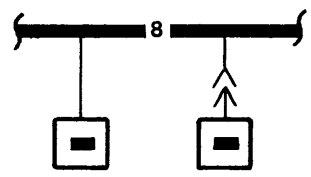
Adder





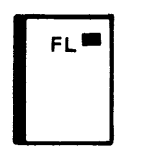


Indicator Lamp

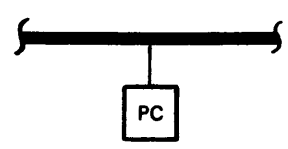


Identifies indicatable bus, register, latch, etc. such as:

Indicatable bus with number of bus lines indicated.

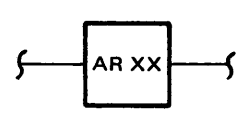


Indicatable Flip Latch

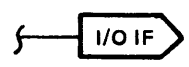


Parity Check Data Bus

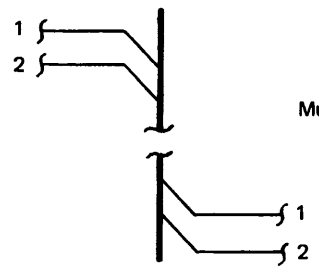
Parity Generate Data Bus



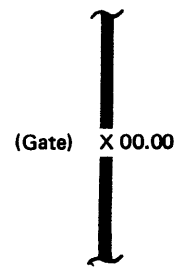
Amplifier
XX Abbreviations
CD = Core Driver
HD = Head Driver
ID = Indicator Driver
LD = Line Driver
LT = Line Terminator
MD = Magnet Driver
V = Voltage Amplifier



Interface
Denotes interface between two units.



Multiple Line Transfer



Gate

Numerals against gate symbol give page or diagram number of gating circuit.

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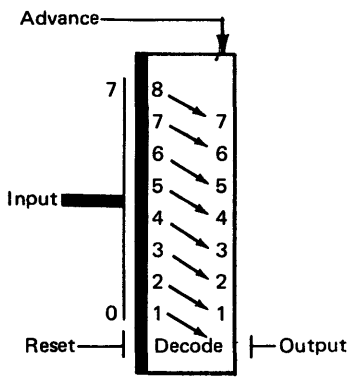
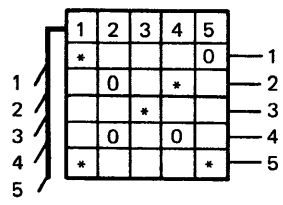
LEGEND

1. LOGIC DIAGRAMS



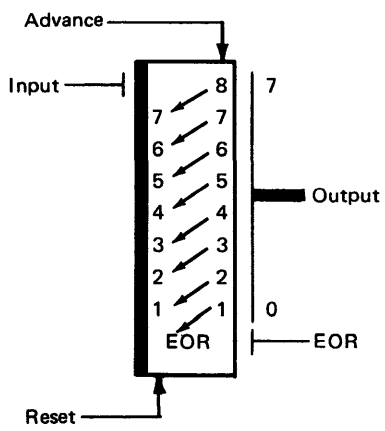
Shift Registers

The Shift Registers are commonly used to serialize and deserialize data information. Input side is denoted by the thick line. A partial transfer of contents is shown by numbered input/output lines.



Multiple Line
Input/Output Block

* Indicates active level
0 Indicates inactive level

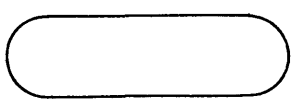


2. TIMING CHARTS

Active State

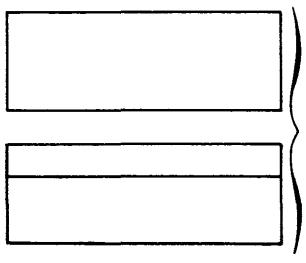
Numerals at beginning and end of the bar identify the signal(s) (also on the same chart) that activate and deactivate this line. "(Not)" with the number indicates that lack of the signal conditions the line

3.FLOWCHARTS



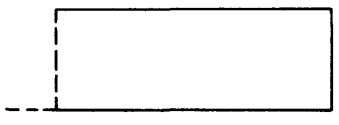
Terminal

Indicates beginning or end of event.



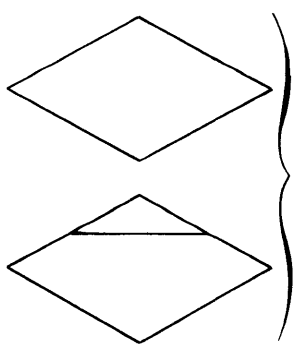
Process

Indicates a major function or event. The upper portion of a divided block specifies where a detailed flowchart of the process is located.



Annotation

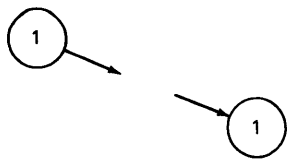
Gives descriptive comment or explanatory note.



Decision

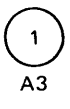
Indicates a point in a flowchart where a branch to alternate paths is possible. The upper portion of a divided block specifies where a detailed flowchart is located.

4. GENERAL



On-Page Connector

Indicates connection between two parts of the same diagram. Arrow leaving symbol points (line-of-sight) to correspondingly-numbered symbol.

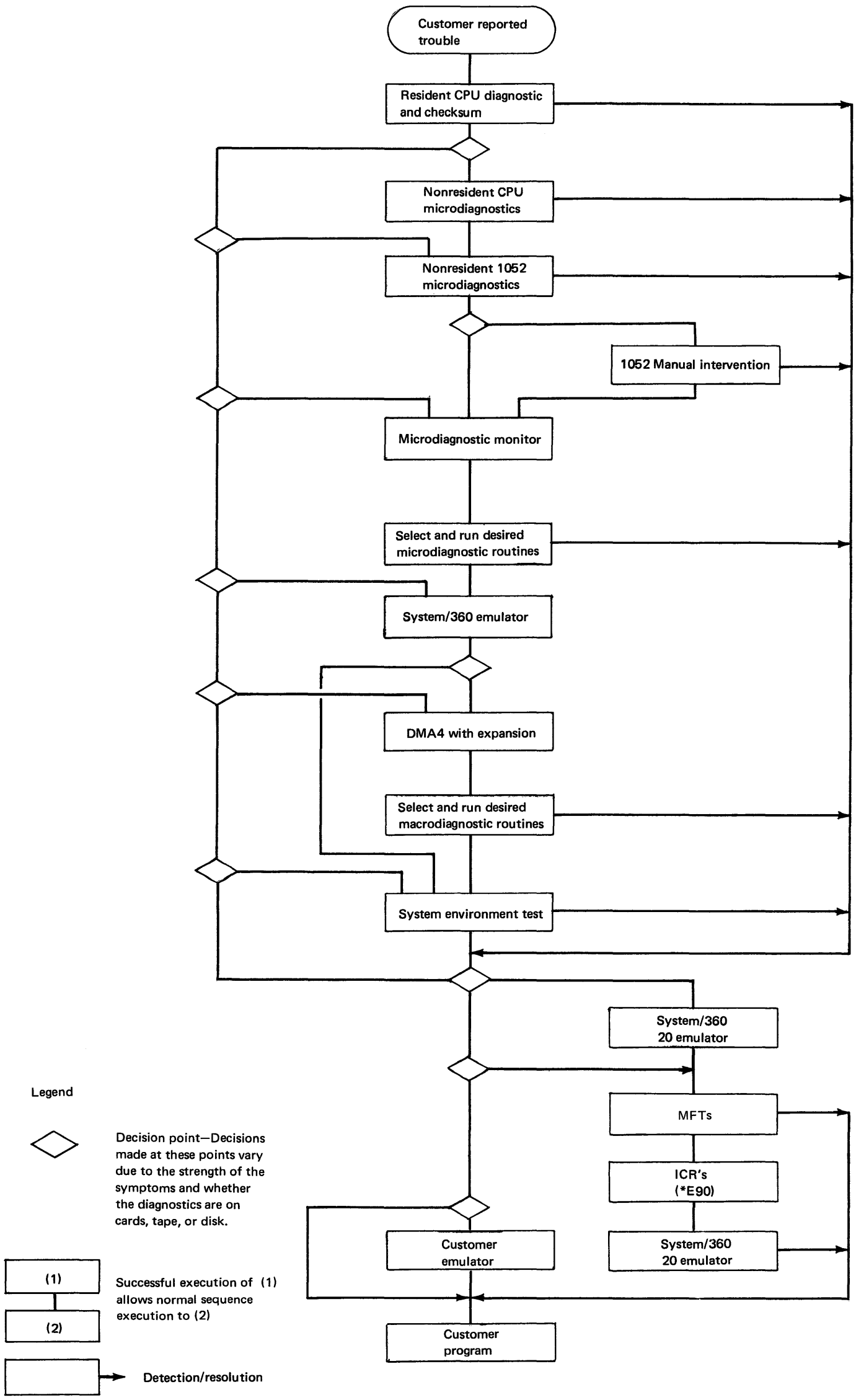


On-Page Connector

Indicates connection between two parts of the same diagram. Alphameric grid coordinate of complementary connector shown beneath.

Off-Page Connector

Indicates connection between diagrams located on separate pages. Location of correspondingly-lettered symbol shown adjacent.



General Diagnostic Strategy Diagrams

These diagrams describe the elements of the System/360 Model 25 basic maintenance strategy and how these elements should be most effectively used by FE. A majority of failures are expected to respond to this diagnostic package, which features comprehensive high-resolution card-fault-locating microdiagnostics.

The above diagram presents a general overview of the diagnostics and is not intended to be complete in itself.

Descriptive text sections of the following diagrams are written to the minimum detail level necessary for understanding and executing the maintenance strategy. For example, the microdiagnostic descriptions are at a summary detail level. The detailed microdiagnostic description consists of the Microprogram Automation System (MAS) list and comments.

For all categories of microdiagnostics, card replacement based on card-fault-location information is the primary approach to fault correction.

Card-fault-location information is provided for all microdiagnostic routines except those that are I/O unit oriented. Tests run under the microdiagnostic monitor use the 1052 to print card-fault-location error messages. Card-fault-location for the nonmonitor microdiagnostics are contained in the MAS listing. For all categories of microdiagnostics, the MAS listing for these routines is provided for additional failure analysis assistance.

Additional resident maintenance facilities are provided as part of every emulator microprogram to assist in failure analysis. These are:

1. FE trap (64 bytes starting at CS address 280)
2. Machine-check trap and 1052 logout
3. 1052 alter/display.

Diagram 1-1. Using the Diagnostic Program Package (Part 1 of 9)

The minor additional circuitry required for 1400-mode operation of 2311 and 2540 devices is tested using the microdiagnostics for these attachment features. Consequently, no special 1400 compatibility diagnostic or function tests are provided with this feature.

Similarly, the System/360 Model 20 Mode feature is implemented almost entirely by microprograms. Therefore special diagnostics are required only when a 2560 MFCM is included with this feature.

Diagnostic coverage for this feature configuration System/360 Model 20 Mode with 2560 MFCM is:

1. Microdiagnostics to test the 2560 attachment logic in the CPU.
2. 2020 Machine Function Tests (macrodiagnostics) executed in the System/360 Model 20 Mode to exercize and diagnose the 2560.
3. Impulse Check Routines (coreload *E90) for measuring the timing impulses from the 2560 and comparing them against a tolerance table.

The diagnostic strategy diagrams are the vehicle used to describe the general approach for executing the diagnostic package. The summary strategy diagram on this page provides a general conceptual perspective of the diagnostic strategy. The detailed strategy diagrams are not intended to cover all failure circumstances nor will they for a specific problem define which diagnostic execution path is most effective. For example, if the failure symptoms point strongly to a tape unit problem, then the microdiagnostics should be bypassed and DMA4 plus the tape macrodiagnostic sections should be loaded and executed.

The 2025 diagnostic program package and diagnostic strategy diagrams do not preclude the FE using common sense and his ability to recognize and interpret customer or machine indicated failure symptoms. The diagnostic package is most effective when its execution is based on the above ingredients.

Note: Where alternate input devices are available, the complete Diagnostic Program Package (DPP) should be kept in appropriate form to use these devices for Control Storage Load (CSL).

The recommended order for using the alternate CSL capability is :

(a) disk
(b) tape
(c) cards

The general diagnostic strategy is based on comprehensive, high-resolution card-fault-locating microdiagnostic programs. These maintenance facilities are sectionalized into the following categories.

RESIDENT MICRODIAGNOSTICS

- **The resident CPU microdiagnostic (BDIA) is initiated automatically by system reset CSL, or IPL to test the basic CPU logic necessary for a control storage load operation.**

- **The checksum routine is always initiated following the resident CPU microdiagnostic to ensure that control-storage contents are correct for all emulator core loads.**

- **When the card reader is the only input device, the microdiagnostic tests the attachment circuitry and the I/O read function necessary to load control storage from the card reader.**

- **The channel microdiagnostic is provided on systems having neither Integrated 2311 Attachment nor Integrated 2540 Card Read Punch. It tests the circuitry necessary for the channel to be functional.**

The resident CPU microdiagnostic routines test the CPU circuits necessary for a control storage load (CSL) operation. No I/O device or attachment circuitry is checked.

For all operating modes (System/360 or other emulator), the resident CPU microdiagnostic is loaded into fixed locations of control storage beginning at address 0240 (system reset trap address).

Generally, errors are indicated either by a stop word, a stop loop, or a branch-test stop. If the CPU stops because of a stop word, the clock is stopped. The clock-off light on the CPU console is turned on. The M-register contents are displayed (the M-register contains the address of the next control word).

A stop loop is a single-word loop. The clock runs, but the microprogram does not progress. This type of error indication is identified when the system light is on, the manual light and clock-off light are off. The branch test stop method of error detection is used to indicate that a branch was executed incorrectly. This diagnostic function uses special hardware (DR-register bit 7) to detect the failure to branch correctly. The console indication is the same as for a stop word (system light off and manual light on) with the additional indication of the DR-register bit 7 remaining on. Similar to the stop word, the clock is stopped and the M-register contents are displayed (address of next control word).

These stop indications, together with a list of possible failing-card locations, provide a comprehensive diagnostic tool. This microdiagnostic is entered automatically when the:

1. system reset key is released,
2. CSL bootstrap and control-storage loading routines are completed, or
3. load key (IPL) is released.

These routines include a branching test, an ALU function test, a mode-register test, a storage word test, an LS X-line addressing test, an LS set/reset test, a dynamic condition register set/reset test, an ALU error-detection and A/B-register error-detection facilities.

The checksum routine is always initiated upon completion of the resident CPU diagnostic. This routine performs an exclusive OR function of the contents of control storage (with the exception of EC information located at 0002 through 000C and the 64-byte CE trap area starting at location 0280 hex). A special checksum number, created by the microprogram and included with every CSL, causes the exclusive OR function result to be zero. Executing the checksum routine ensures that the control store load was complete and correct, and that the control storage contents have remained complete and correct. This provides protection against a missing CSL card, an inadvertent change to some control storage data, or a machine failure that prevents proper control store loading. A CSL check indicator on the console panel is turned on when a checksum error occurs.

A message confirming the EC level of the core load is printed on the console printer (see example on Diag 1-1 Part 7) when the program is executed as part of the resident microdiagnostic program initiated at the completion of a CSL.

If the CPU is in CE mode (CE key is inserted), a correction factor is automatically entered into control storage. This correction factor permits future execution of the checksum routine without error. This correction factor remains until the next control store load. Upon completion of the checksum routine the system-reset routine is entered and executed.

On systems where the card reader is the only input device, a resident diagnostic is used to test the card reader circuits needed to CSL. The diagnostic uses the portion of control storage usually apportioned for file microprograms.

If used for the Integrated 2540, this microdiagnostic tests the circuits used for manual operation, for card-feed path handling, and reader status and checking circuits.

If used for a card reader attached to the channel, this microdiagnostic tests much of the logic necessary for a CSL operation from a card reader attached through the channel.

For systems having neither 2311 Attachment or Integrated 2540, a resident microdiagnostic is provided to test the channel circuitry. Due to these restrictions, only a low percentage of the systems will have this resident program.

Nonresident, Nonmonitor-Oriented Microdiagnostics

- ***100**
  The nonresident CPU microdiagnostic is intended to provide extensive coverage and high failing-card resolution for the basic CPU logic. It provides expanded detection and failing-card resolution as compared to the resident CPU microdiagnostic. It also contains the resident microdiagnostics for the 2540 and the channel.

- ***110**
  The nonresident 1052 microdiagnostic comprises two parts: the attachment-circuitry routines, and the device exercising routines. This microdiagnostic ensures that the 1052 is capable of performing the I/O functions required by the microdiagnostic monitor.

- ***130**
  The nonresident memory microdiagnostic is designed for use if a CPU has two storage modules under the failure conditions described in the following.

The nonresident CPU microdiagnostic routines provide a complete, high-resolution test of basic CPU logic hardware. The routines are normally executed as the second logical step (after BDIA and checksum routines) of the primary diagnostic strategy. They can also be executed before and after any EC activity to verify CPU operation.

All systems will be shipped with the *100 residing in control storage. Once the basic CPU has been tested, the CSL device (Integrated 2540 or any reader attached to the channel) may be tested by using the resident diagnostic.

The nonresident CPU microdiagnostic can be loaded from cards, tape, or disk, using the CSL procedure for the appropriate input device. The routines are then executed automatically in a given sequence. If these tests are already loaded, the system-reset key initiates execution of the routines in the correct sequence. The system stops after the last test.

These routines should be loaded and executed (although this is not significant) before attempting to run the 1052 diagnostics or any of the tests executed under the microdiagnostic monitor. The nonresident CPU microdiagnostic is executed at computer speed and gives maximum assurance that the basic CPU data paths are error free.

Any errors encountered (such as a stop word or a branch-test stop) are indicated on the system control panel. If an error is detected, the CE checks the fault-location list of possible failing-card locations for this error indication. Some of the functions tested are:

Access and branch facilities
Basic ALU
Arithmetic modifier

Diagram 1-1. Using the Diagnostic Program Package (Part 2 of 9)

Diagnostic register
Status register set and reset
Local storage Y-axis line-address decode and read/write controls
Local storage controls and cycle-control (storage word)
Local storage X-axis line-address decode and set/reset
Local storage addressing and data storage
System mask register
ALU-check circuits
Comprehensive arithmetic facilities
Storage word
Priority Control
Trap priority.

The 1052 microdiagnostic program is a standalone program designed to test the console printer and attachment circuits. An error causes a microprogram stop. Error messages are contained following the stop-word location in the microprogram listings. If the CE performs the suggested repair procedure and the same error occurs again, the scope loop facility allows a tight loop on the error. Logic page references are included in the second error-stop error messages. This test is usually placed in the card reader hopper with the nonresident nonmonitor-controlled CPU microdiagnostic. It is then normally executed as the next test after the CPU microdiagnostic has been completed without error. The nonresident 1052 microdiagnostic can also be loaded separately and run separately from the CPU nonresident microdiagnostic. This is useful for verifying correct operation after making mechanical adjustments in the console printer.

The first part of the test is concerned with the attachment and control circuitry, because confidence in the control circuit must be established before the mechanical units can be checked. Some of the functions tested are:

TU- and TT-registers (basic operation and status storage)
System reset
Basic interface control
Upper case and lower case character decode circuits
Space, carrier return, and end of line, when applicable

The following message is printed on the 1052 when the first part of the test is completed.

```
1==1 0123456789 WRITE. FOR 12.5 INCH
PLATEN DEPRESS START KEY. FOR 13 1/8
PLATEN AND EOL TEST DEP REQ THEN START
KEY-1234567

ROUTINES TYA1, TYA2, TYDB, TYDC, HAVE
BEEN COMPLETED WITHOUT AN ERROR.

TO RUN ROUTINES TYDD AND TYDE WHICH WILL
REQUIRE MANUAL INTERVENTION DEPRESS
START THEN THE REQUEST KEY, AND FOLLOW
INSTRUCTIONS AT EACH STOP WORD.  STOP
WORD ADDRESS IS ADDRESS IN CONSOLE
LIGHTS MINUS 2.
*** NOTE ***TO BYPASS MANUAL ROUTINES
DEPRESS THE LOAD KEY.  THIS
WILL CSL MICRO MONITOR IF AVAILABLE.
```

With confidence established in the control circuitry, the second part of the microdiagnostic is started. This part includes manual intervention routines, and checks for correct printing from the keyboard as well as the set and reset of the various external facilities. Also included are facilities for adjusting singleshots, for continuous printing of a selected character, and for unlocking the keyboard to allow characters to be typed. The latter function facilitates mechanical adjustments. During this second part of the test, instructions in the MAS listing provide direction to the CE.

The nonresident memory microdiagnostic is provided for systems with two storage modules to isolate hardware failures within a module. It is intended for use when a memory failure is occurring in only one of the modules. The microdiagnostic isolates SLT failures to a failing card and array failures to the defective section of the array.

The microdiagnostic loads various bit patterns into the failing storage module, reads the data back out and retains the addresses of failing locations. The failing addresses are then analyzed and a decision is made as to the card location of the failing component. The card location is then indicated via a 1052 printout. If a card location can not be determined, a message is printed describing the problem causing the failure.

Loading of this microdiagnostic is restricted to the Integrated 2540 or a channel reader. Output messages are printed on the 1052 Printer. A special set of bootstrap cards is required for loading *130; these are provided with the system.

Nonresident, Monitor-Oriented Microdiagnostics

The descriptions in the following sections are used to test for, and diagnose, failures associated with the various input/output attachment features (except 1052) the I/O channel, and certain CPU features. The microdiagnostic monitor (*1C0) provides the capability for loading microdiagnostic sections, printing messages required by the sections and the monitor, handling all interrupts, handling all traps, looping of a section, and looping of a routine within a section.

The low-half of control storage (addresses 0000 to 1FFE) is reserved for the monitor. The section to be executed is loaded into the high-half of control storage (addresses 2000 to 3FFE).

The micromonitor should be configurated for the individual system by adding a maximum of two cards to the monitor deck immediately preceding the end card. For detailed information, refer to routine WW8A in the micromonitor (*1C0) microlisting.

(1) CPU FEATURES (*200)

The CPU features microdiagnostic operates under monitor control to provide a comprehensive check of hardware and logic peculiar to Storage Protection and/or Interval Timer; optional features on the 2025.

The first part of the section is comprised of routines designed to provide resolution for Storage Protection. Some of the functions performed are:

Setting and resetting of the associated registers (Q, FQ, GQ, HQ).

Verification that the data paths between the registers and CPU are operational.

Writing and reading capabilities of the 64-byte monolithic local storage memory. This routine also permits scoping of local storage timings.

Parity checking of the monolithic stack and verification of the parity checking circuitry.

Interaction test of the monolithic stack.

A check of each tag and key position by first setting 00 and then FF in each position.

Capability to detect key and tag mismatch or a bad parity tag in file mode.

The second part of the CPU features section is designed to check logic and hardware (T register triggers and latches, etc.) associated with the Interval Timer. Error and fault locating messages are printed on the 1052 under monitor control for both parts of the CPU feature microdiagnostic.

(2) INTEGRATED 2311 ATTACHMENT MICRODIAGNOSTIC (*300, *310, *320)

This microdiagnostic program operates in the microdiagnostic monitor environment to exercise and test the Integrated 2311 Attachment circuits.

Initially, the diagnostic mode is turned on in the attachment circuitry. The purpose of this is to prevent any activity in the 2311 itself, and then to allow the attachment circuitry to be tested without the 2311. This permits a thorough evaluation of the attachment circuits without manipulating any actual data on the 2311. A failure in any basic test causes a branch to the error check and message subroutine which provides the general housekeeping needed (within the Integrated 2311 attachment microdiagnostics), such as control of the looping facilities, routing the program to the proper error messages, and interface with the microdiagnostic monitor. The microdiagnostic monitor contains the necessary CPU general housekeeping routines, as well as the console printer-keyboard subroutine so the error messages can be printed.

The basic function tests progress from the simpler hardware functions to more complex overall functions. The test sequence is as follows:

- A general hardware reset test for some of the attachment circuits.
- Op-register and op-register decode.
- Bit ring advance via write phase A and read clock simulation. Both checked for write clock gate and read gate.
- Exercise the compare logic, cyclic code register and associated circuits and read buffer and write buffer shift circuits. Sync detect character and sync detect along with bit ring inhibit is checked.
- A read home address and R0 operation are simulated.
- Flag bits 6 and 7 and track condition are checked.
- A write home address command, write R0 command, a write-count, key and data command are simulated. The write count key data command simulates through write address mark time because after this point the operation is the same as the write R0 command.

- The 1400 circuits are tested if the option is on the file control. See the micromonitor sense switches for definition of Integrated 2311 1400 hardware.
- The data check, data check in count, and track overrun are checked.
- A search equal home address operation is simulated.
- Wrong length record and CCW count 0 circuits are checked.
- Some of the file trap gate, trap conditions, clock through key and data, data overrun, and head compare are checked.
- A search equal count command is simulated.

A routine is provided to aid in adjusting some of the file control singleshots. Routine 06 (X06A) of *300 contains instructions for the adjustment procedure. This routine is normally not run unless the appropriate section sense switch is on. The singleshots that can be adjusted via this routine are:

1. Head condition
2. 400 ns index and delta 400 ns index
3. Control tag
4. Upper and lower 16 ms singleshots for recalibrate timeout.

Diagram 1-1. Using the Diagnostic Program Package (Part 3 of 9)

(3) INTEGRATED 1403 ATTACHMENT MICRODIAGNOSTIC (*400, *410, *420)

The printer attachment microdiagnostic exercises and tests the 1403 attachment and control circuits. The test is designed to check the hardware logic used for printing and performing carriage operations. Mechanical functions are also exercised.

The microdiagnostic program consists of three groups of routines:

The first two groups include the dynamic, non-printing, fault-locating tests. The CE transfers the current limit switch (a CE aid) so printing is suspended. This prevents the possibility of print magnet coil damage due to an existing defect. These groups check all the basic attachment and control circuits such as status generation, timing circuits, buffer and buffer control, PCC and subscan control, and checking circuits.

The third group of routines is executed for a more rigorous exercising of the mechanical and electronic units. In these routines, printing and carriage operations are allowed to occur to exercise all printer functions. This group includes carriage exercising routines and a print routine.

The error message scheme for these routines consists of basic error information printed via the 1052, with reference to the microlisting for more extensive fault locating and troubleshooting messages. In some cases, oscilloscope sync point information is included in the error messages to facilitate trouble analysis with an oscilloscope.

(4) INTEGRATED 2540 CARD READ PUNCH MICRODIAGNOSTIC (*500, *510)

The 2540 microdiagnostic operates under control of the microdiagnostic monitor to perform comprehensive tests of logic circuitry for the Integrated 2540 attachment as well as much of the device circuitry. The first part of the test (*500) includes various dynamic routines designed to exercise and test control and attachment circuits at computer speed. This allows a rapid checkout of the majority of reader-punch circuits. Some of the functions tested are:

Basic data flow and branch registers (RS, DS, RPS, RPD1, RPD2, RP1, and RP2)
Circuitry for manual operations and card feed path handling
Status and error-checking circuits
Basic data handling ability of attachment (includes shift and address registers for all cycles for both reading and punching).

The second part of the test (*510) includes routines that exercise the mechanical functions as well as the attachment and control circuits. This part of the test identifies brush failures by row and column. Punch feed read is also exercised. Also, card punch data-oriented problems are detected and identified.

(5) SYSTEM/360 CHANNEL MICRODIAGNOSTIC (*600)

This microdiagnostic program is executed in the monitor environment to test the System/360 channel. These routines are designed to test the channel circuitry to ensure that it can generate and respond to all standard I/O interface signals. Failures cause a branch to the microdiagnostic monitor for error message printout and looping facilities:

The first routine tests that all channel registers (GD, GS, GI and GT) can be reset correctly. The microlisting describes the correct reset of these latches, and includes a summary of the register position functions. Also tested are the channel diagnostic latch for correct set and reset, the CPU-to-external line for correct function, and the channel mode circuit for correct operation.

The second routine checks the bus-out and bus-in lines (all bits), and the tags-in lines (request-in, operational-in, status-in, service-in, select-in, and address-in).

The third routine checks the tags-out latches for correct set and reset. This includes the operational-out, the select-out, the service-out, the command-out, and the address-out latches. This routine simulates failure conditions that could erroneously raise a tags-out line to determine correct circuit operation.

The fourth routine checks for correct operation of the service-in and status-in circuits. The microdiagnostic program checks that these lines fall in correct response to the service-out and command-out lines being raised. In addition, the correct operation of the channel 1 interrupt latch is determined.

The fifth routine checks the suppress-out data chain, channel ID, and buffered-device latches for correct operation. Direct set and reset responses are checked, as well as the function of these latches in response to other circuit functions.

The sixth routine checks the burst latch, the initial selection latch, and the low and high priority trap circuits. Correct trap requests are simulated and the circuit responses checked. An incorrect trap request causes a branch to the monitor so an error message can be printed.

The seventh routine checks for correct function of the channel parity circuits.

Additional routines are provided to facilitate diagnosing interface and I/O device failures. These include:

a) Check Sel-Out wrap around to Sel-In.
b) ADDRESS response test
c) TEST I/O, complete initial selection of all possible device addresses.
d) Single cycle routine - command to a particular address and looping capabilities

(6) INTEGRATED COMMUNICATIONS ATTACHMENT MICRODIAGNOSTICS (*700, *710, *720, *730)

*700 This microdiagnostic operates under control of the microdiagnostic monitor to test extensively the ICA base hardware. The test performs microprogram trapping, line adapter addressing, and extensive checkout of the CPU to ICA interface.

*710 This microdiagnostic operates under control of the microdiagnostic monitor to test the start/stop EIA and telegraph line adapters. The test performs an extensive checkout of line adapter addressing and trapping. Transmit and receive trapping and clocking are checked on all adapters.

*720 This microdiagnostic operates under control of the microdiagnostic monitor to test the binary synchronous line adapter. Some of the functions tested are the 1- and 3-second time delays, TRCR ring controls, transmit and receive, A-serdes and B-serdes register advancing, SYN character encode and decode, and SYN character count insert.

*730 This microdiagnostic operates under control of the microdiagnostic monitor to test the automatic calling feature. The diagnostic checks to determine that the external autocall unit has power on. If it has power on, an extensive checkout of the base ICA to autocall feature interface is performed.

The ICA microdiagnostics require a line adapter definition table that is stored in program storage location starting at 25C0. The format of the LDT table is explained in detail in routine ZA01, which is contained in coreloads *700, *710, *720, and *730.

(7) INTEGRATED 2560 MICRODIAGNOSTIC (*800, *810, *820)

This microdiagnostic is provided with the Model 20 Mode feature when a 2560 MFCM is included in the configuration. It is executed under monitor control and tests the 2560 attachment logic in the 2025 without exercising the 2560.

The first part of the test, *800 and *810, includes various dynamic routines that exercise the attachment circuits at computer speed. The routines use print latches, diagnostic hardware, and an internal diagnostic configuration to allow a rapid checkout of the majority of the attachment circuits.

Some of the functions tested are feed CB lines, motor ready, data buffer read controls, and data buffer punch controls. Read compare is checked by forcing read checks.

Other tests check the data buffer by exercising various punchbit combinations with external bus-out bits. Punch compare is tested by forcing read checks.

Feed cell inputs are checked by exercising punch feed select lines. Secondary select controls, feed cell dark latches, punch push controls, feed check latches, and attachment controls are also tested.

If the print feature is installed, the print control circuitry is tested. The print feature tests are bypassed automatically if the feature is not installed.

Singleshot adjustment routines, motor ready time delay testing, and manual intervention routines are included in *820.

Generally, the four sections should be executed sequentially although the capability exists under monitor for separate execution.

(8) INTEGRATED 2560 ICR MICRODIAGNOSTICS (*E90)

This is a nonmonitor microdiagnostic that provides 2560 tests corresponding to the following System/360 Model 20 ICR tests:

Speed calibration
Feed CB's and feed clutch
Magnet control and feed CB flip latches - primary
Magnet control and feed CB flip latches - secondary
Primary feed (print and non-print)
Secondary feed (print and non-print)
Feed flip latches (print and non-print feature)
Punch pusher - primary
Punch pusher - secondary
Punch and print CB's (modified for geneva drive machines)
Feed check diagnostic - Note 1

The above routines check for proper operation of the 2560 by measuring timing impulses and comparing them against a tolerance table. Test results are printed out on the 1403 printer with provisions for printing out on the 1052 printer keyboard when the 1403 is not available.

Note 1: This is macro test ICR125 run under *E90 diagnostic coreload. It includes the cycle delay feature.

Diagram 1-1. Using the Diagnostic Program Package (Part 4 of 9)

CARD-FAULT LOCATION

All of the microdiagnostic programs are designed to find a failing card by cross-referencing an address to a listing of suspect card locations. This listing is provided as a separate document for resident and nonresident nonmonitor-controlled programs. For monitor-controlled microdiagnostics, the suspect card location or locations are printed on the 1052 console printer for each error. However, the integrity of the card-fault-location information can be assured only if:

1. All microdiagnostics are executed in the sequence shown in the Diagnostic Strategy Diagrams
2. All parts of multiple part programs are executed in sequential order (example for 1403 Printer; *400 must be executed, followed by *410 and then *420).
3. The first error encountered is corrected before proceeding to subsequent routines or sections of the microdiagnostics.

As an assurance against inadvertent failures caused during a repair, it is considered good CE practice to re-execute all parts of multiple-part programs before the system is returned to the customer.

MICRODIAGNOSTIC PROGRAM AND HARDWARE CONCURRENCY

The resolution and fault-locating capabilities of the microdiagnostic programs can be assured only when they are concurrent to the system hardware. Therefore, it is considered good CE practice to verify the EC level of each program before execution.

ALD logic pages AA000 through AAnnn provide the cross-reference information for each program and the associated system hardware. Refer the EC level of each program to these charts for each of the Diagnostic Program Package modes as follows:

1) Cards

EC level is punched in columns 36-41 of the first card of each section.

2) Tape or Disk

Nonmonitor-controlled sections (*100, *110, *1C0).
EC level (last four digits in hex form) is stored in control-storage location 0EC0.
Monitor-controlled sections.
EC level (last four digits in decimal form) is printed on the console printer as part of the operator message when each section is loaded (refer to Diag 1-1 P3 for example).

LOADING AND USING THE DIAGNOSTIC PROGRAM PACKAGE

Set the console switches ABCD as follows (switches A and B must be set the same):

Switches AB = CC CSL from channel
Switches AB = EE CSL from Integrated 2540
Switches AB = FF CSL from Integrated 2311
Switches AB = DD CSL from Integrated 2560
Switches CD = actual unit address (when using a device on the channel (AB=CC) for file (AB=FF))

a. DPP (Diagnostic Program Package) on cards
   1. Place the microdiagnostic program decks in the reader in the following sequence:
      Note: For bootstrap listing, refer to Vol. 1 of ALD's.

      Bootstrap
      Nonresident CPU
      1052 Nonresident
      Micro Monitor
      Micro Monitor Sections

   2. Use the Diagnostic Strategy Diagrams and execute the microdiagnostic programs in the sequence indicated; setup and execution instructions are provided on the diagrams.

Note: Once the monitor has been loaded, the 1052 prints system configuration information. When this printout is complete, set switches ABCD to 0000 and press the CPU Load button. This initiates loading the next section. When the next section is loaded, the card reader stops. Press SYSTEM RESET and START to execute the section. If the section executes without error, the console printer prints T and, if monitor sense switch 5 is on, the next section loads automatically. Refer to the procedure for using Monitor Sense Switches (Diag 1-1 P5).
The next section can be loaded at any time by pressing STOP, setting switches ABCD to 0000, and pressing the CPU load key.
All microdiagnostic card decks have a core load index number punched in columns 73-76. The sequence number within the deck is punched in columns 77-80.

It is possible to load the entire microdiagnostic package sequentially. Refer to the Diagnostic Strategy Diagrams for specific instructions on how to perform a sequential microdiagnostic load and run. When executing microdiagnostic program sections under monitor, it may be desirable to remove sections already executed and stacked in the 2540 or 2560, and to load additional sections. This can be implemented by setting console switches ABCD to FFFF and pressing the console load key. Then follow the instructions printed on the console printer.

Note: The same message will print when the reader is out of cards and the load key is pressed with console switches ABCD set to 0000.

b. DPP on Magnetic Tape
   1. File protect the DPP tape and mount on tape drive.
   2. Set CPU Console switches CD to tape drive address.
   3. Press CSL key to load the CPU Non-Resident Microprogram. Follow the test sequence in the strategy diagrams at the successful completion of the CPU nonresident microprogram, press START to load the 1052 microprogram.
   4. At the successful completion of the 1052 NONRESIDENT MICROPROGRAM, press the load key to load the Monitor.
   5. The following options are now available.
      (a) Execute all sections in sequence as shown below:

      *200 - CPU Features (Storage Protect & Interval Timer)
      *300 - 2311 Part 1
      *310 - 2311 Part 2
      *320 - 2311 Part 3
      *400 - 1403 Part 1
      *410 - 1403 Part 2
      *420 - 1403 Part 3
      *500 - 2540 Part 1
      *510 - 2540 Part 2
      *600 - Channel
      *800 - 2560 Part 1
      *810 - 2560 Part 2
      *820 - 2560 Part 3

      Set the CPU console switches ABCD to 0000. Press CPU load key. The first program will load and this message will be S(XXXX) where XXXX is the program number;
      0200 STOR PROT DIAG

      Press START to execute the program. (At the successful execution of the program, the console printer will print a T and the next program will load automatically if monitor sense switch 5 is on.)
      The preceding sequence is repeated through all programs.

      (b) Execute selected programs in (a). Set the CPU console switches ABCD to 0XXX, where XXX is the number of the program; 300, 310, 400, 500 and 600. Press the CPU load key. The program will load and the message as in (a) above will be printed. Press the start key to execute the program.

      Note: Read backward operations are not possible with 7-track tape, therefore rewind to the load point. Set switches ABCD to 0100 and rewind tape. Press start key to execute the program.

      (c) Load System/360 Emulator
      Set the CPU console switches ABCD to 0E60. Press the CPU load key; then load the customer program.

      (d) Load System/360 Model 20 Emulator
      Set the CPU console switches ABCD to 0E20. Press the CPU load key; then load the customer program.

c. DPP on the 2311 Disk File
   1. Mount the disk pack on the 2311 disk drive.
   2. Set CPU console switches CD to the 2311 disk drive address.
   3. Repeat instructions 3 through 5 under DPP on Magnetic Tape.

Monitor Sense Switches

To set any of the monitor sense switches (excepting 8 or 9, see note 1), place the CPU into process mode and press the alter/display key. Enter SC X,X,X, X,X,X,.....on the 1052 printer Keyboard, where X is the representative character on the keyboard to cause setting of the corresponding sense switch. The keys identifying the sense switches may be pressed in any order. Press the EOB key on the 1052 at the end of the SC message entry. Press the start key on the CPU to get out of alter/display function.

To reset any of the microdiagnostic monitor sense switches, place the CPU into process mode and press the alter/display key. Enter RC X,X,X,X, ...on the 1052 printer Keyboard, where each X represents the corresponding sense switch. The keys identifying the sense switches may be pressed in any order. Press the EOB key on the 1052 at the end of the RC message entry. Press the start key on the CPU to get out of the alter/display function.

Following is a summary of the microdiagnostic monitor sense switch positions and their meanings. All switches are off following a monitor load, monitor initialize function, or if reset by a reset instruction. Pressing SYSTEM RESET, or loading a new section does not affect the setting of the monitor sense switches. The monitor sense switches are located at control storage address 03BE.

Diagram 1-1. Using the Diagnostic Program Package (Part 5 of 9)

Monitor Sense Switch No.	State	Meaning
0	Off	Normal mode
	On	Suppress all messages
1	Off	Normal mode
	On	Print only error messages
2	Off	Halt on error
	On	Continue after error
3	Off	Normal mode
	On	Print only section 1D, routine number, and BAL address
4	Off	Print full error message
	On	Print only * on error message
5 (See Note 1)	Off	Manual Mode All routines are initiated. Monitor halts after loading each section. Monitor halts after executing each section. (If start button is pressed, section is executed again.) Sections halt after issuing setup instructions (See Note 1).
	On	Dynamic Mode Sections are loaded and executed sequentially under monitor control. Tests requiring manual intervention (*420 - routine 70, *510 - all routines, *600 - routine 11) are not run. Sections do not halt after issuing setup instructions (See Note 1).
7	Off	Normal Mode
	On	80-80 card to tape from card reader used to load monitor to tape address XX (hex) specified in auxiliary storage 008D. Set switches ABCD to FFFF,press LOAD and the 1052 prints a message to load the card reader.
8, 9 (Note 2)	Off	Normal mode
	On	Loop section
9	Off	Normal mode
	On	Loop routine
6,A,B,C,D,E,F		Not used

Note 1: The setup necessary is as follows: Interval Timer Test: Toggle switch on. Printer tests: CE carriage tape on, T-casting closed, no forms check, 6-line neutral, and current limit switch in limit position.

Note 2: Monitor Sense Switches 8 or 9 should not be set on by using alter/display or erroneous looping can result. These switches must be set as described under the following headings:
Section Sense Switches
Select and Loop a Routine

Section Sense Switches

The section sense switches do not have fixed meanings, but instead the meanings are defined according to section need. If these switches require manual setup, the console printer will print the sense switch definition for this section.

To set any of the section sense switches, place the CPU in process mode and press the alter/display key. Enter SS X,X,X,X,.....on the 1052, where X is the representative character on the keyboard to cause setting the corresponding sense switch. Press the EOB key on the 1052 at the end of the SS message entry. Press START on the CPU to get out of the alter/display function.

To reset any of the section sense switches, place the CPU in process mode and press the alter/display key. Enter RS X,X,X,X,.....on the 1052 printer Keyboard where X is the representative character on the keyboard to cause setting the corresponding sense switch. Press the EOB key on the 1052 at the end of the RS message entry. Press CPU start key to get out of alter/display function.

Alter/Display Function

The alter/display function works the same as that on the System/360 Emulator. Press start key once to get out of the alter/display mode when finished.

System Reset-Start

Once a microdiagnostic section is loaded, press the system reset key and then the start key on the CPU console to initiate execution of the section from its starting point.

Select and Loop a Routine

This method of initiating the loop routine function sets microdiagnostic monitor sense switch 9 on automatically, and also allows selection of the routine to be looped. Dial 01XX into the CPU ABCD switches, where XX is the routine number to be looped. Press SET IC and the message "Looping Routine XX" will be printed on the 1052. Press START on the CPU to start the looping function.

To exit a loop routine, press STOP on the CPU. To progress to subsequent routines, reset monitor sense switch 9 as previously described. To select another routine looping, dial another routine number and press SET IC and START as before.

Select and Loop a Section

The capability is provided under monitor, to loop a selected section of the microdiagnostic programs (*300, *310, *320, *400, *410, *420, *500, *600) by setting monitor sense switch 8 on as follows:

1. Set console switches ABCD to 01FF (after the section has been loaded, with monitor sense switch 5 off, or after an error stop).
2. Press SET IC.

To exit from a looping section, press the stop key and set monitor sense switch 8 off.

Initialize Microdiagnostic Monitor Function

To initialize the microdiagnostic monitor, press the alter/display key and type an "I" on the 1052. This restores all microdiagnostic monitor sense switches to the normal state (all off).

Microdiagnostic Monitor Message Codes

The messages printed by the 1052 are identified by a code that prints to the left of the message. These are defined as follows:

* = Section error message
$ = Monitor operator message (for your information)
/ = Operator procedural error
¤ or < = Unanticipated trap

When the microdiagnostic monitor has been loaded, the 1052 prints out an operator message that identifies the features present on this particular system. The 1052 prints a list of features and identifies with a 'Y' those features included with this system, and with an 'N' those features not included with the system. Following are sample messages printed by the 1052.

```
$ MONITOR SYSTEM FEAT EVALUATION
     *-MONITOR ASSUMPTION

2581 4 MEM-48K
2582 Y STGPROT
2583 Y TIMER
2584*Y  60 CYCLE
2590 Y NTV 2540
2591*Y  PFR
2592*N  51 COL
2593*N  1400
2595 Y NTV 2311
2596*N  1400
259A Y NTV 1403
259B*2  MOD 2
259C*N   MCS
25A4 Y CHNL
25A9 Y NTV 2560
25AE Y NTV COMM

TO ALTER SYSTEM CONFIG MODIFY
ASSOCIATED FLAG BYTES IN PROG STOR.
REFER TO WW8A IN MAS LISTING FOR
INSTRUCTIONS
 NTV COMM CONFIG INFORMATION IS
CONTAINED IN PROG STOR BEGINNING AT
25C0
```

Message at completion of microdiagnostic
Monitor CSL with system configuration not defined by input card.

Diagram 1-1. Using the Diagnostic Program Package (Part 6 of 9)

```
$ MOD 25 SYSTEM CONFIGURATION

2581 3 MEM-32K
2582 Y STGPROT
2583 Y TIMER
2584 Y  GO CYCLE
2590 Y NTV 2540
2591 Y  PFR
2592 N  51 COL
2593 N  1400
2595 Y NTV 2311
2596 N  1400
259A Y NTV 1403
259B 2  MOD 2
259C N  MCS
25A4 Y CHNL
25A9 Y NTV 2560
25AE Y NTV COMM

TO ALTER SYSTEM CONFIG MODIFY ASSOCIATED
FLAG BYTES IN PROG STOR. REFER TO WW8A IN MAS
LISTING FOR INSTRUCTIONS
 NTV COMM CONFIG INFORMATION IS CONTAINED
IN PROG STOR BEGINNING AT 25C0
```

Message at completion of microdiagnostic.
Monitor CSL with system configuration defined by input card.

```
S 0600 CHANNEL DIAG
```

Operator message at start of each section.

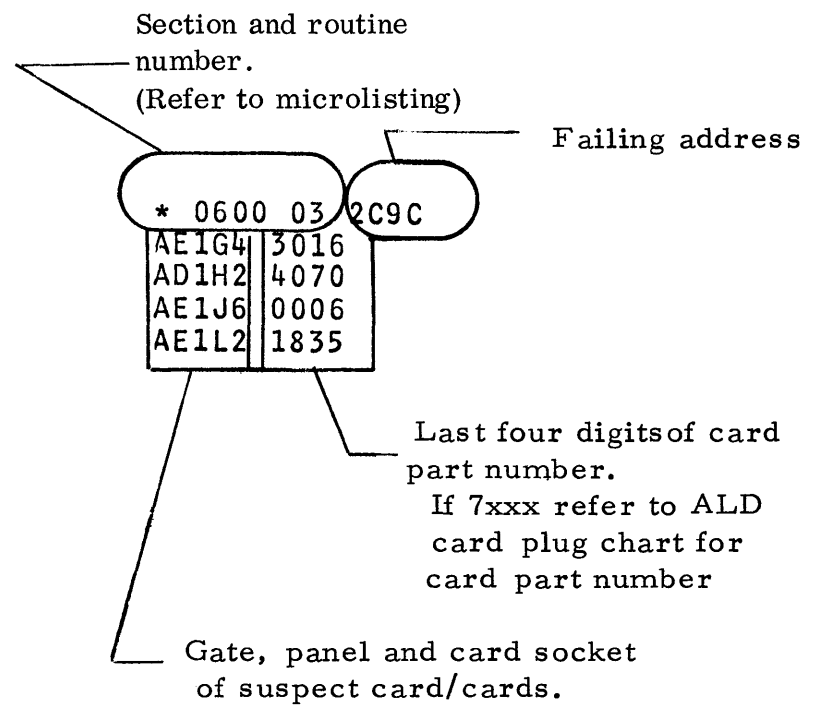
```
S
0200 20 25F8
TURN INTERVAL TIMER SWITCH TO ON AND DEPRESS
START BUTTON.  WHEN DIAGNOSTIC IS COMPLETE TURN
INTERVAL TIMER SWITCH TO OFF.  THIS IS A ONE
TIME MESSAGE.
T

/ DO NOT HIT START-ROUTINE NOT IN SECTION

/ INV A,B SWITCHES
```

```
$ TO LOOP ROUTINE 03 PRESS CPU START



$ TO LOOP ROUTINE 05 PRESS CPU START
```

```
$ TO LOOP SECTION PRESS CPU START
```

```
$ TO LOOP NEW SECTION FROM NATIVE 2540,
DO NPRO AND MAKE READY WITH ADDITIONAL
SECTION(S).
```

General operator messages.



Message for failure under Monitor.

Valid CSL and check sum

```
8229 0E60 4C14 0000
```

Check sum value in control storage (cs 0002 for E060)

Emulator(360) core load

E C level of core load

Invalid CSL and check sum

(Indicator on CPU turned on)

```
8229 0E60 0C14 0000
8229 0E60 0C14 4000
```

Second line prints only if C. E. key is on.

Result of Exclusive OR function.

Diagram 1-1. Using the Diagnostic Program Package (Part 7 of 9)

Creating the Diagnostic Program Package

The entire DPP is shipped in card form for all System/360 Model 25 systems. However, execution of the DPP can be enhanced by using the disk file or magnetic tape capability where the system configuration permits. These mediums not only simplify loading of microdiagnostic programs and the System/360 emulator but also expand their effectiveness by providing an alternate means of CSL.

During installation of the system, the card decks should be transcribed to disk or tape (obtained locally) as follows:

a. Disk DPP

Use FOFE (Revision level 3) to convert the DPP card file to the CE Disk Pack (Both MACROS and MICROS). Refer to FOFE Users Guide.

Note 1: If the CE disk pack to be used was built with a previous level of FOFE, it must be rebuilt completely.

Note 2: The diagnostic microcode chains from the file bootstrap to *100 to *110 to the micromonitor. All four must be on the CE pack.

Note 3: If it is necessary to put two emulators (or diagnostics) on the CE disk pack having the same I.D. (i.e., *E60), this can be accomplished by changing columns 75 and 76 of the first card of one of the decks to another hex value (i.e., *E61).

Note 4: Do not include *130 (Memory Diagnostic) or *E90 (2560 ICRs) in either the Disk DPP or the Tape DPP.

Note 5: Prior to building a DPP on a disk pack, program FFF0 must be run against that disk pack.

b. Magnetic Tape DPP

Either DEBE (if available) or the 80-80 card to tape function of the micromonitor (*1C0) should be used to create the DPP tape from the card decks. The System/360 Model 25 macrodiagnostics can be placed on another tape by the standard procedure used for generating a diagnostic tape.

Example: FOFF as defined in FOFF description in the maintenance diagnostic programs manual for tapes, Vol. 01.

The procedure for using DEBE is as follows.

1. Mount reel of tape (obtain locally) and make drive ready.
2. Load the decks in the card reader in the following sequence.

   DEBE or *1C0
   Channel Bootstrap Card
   *100 CPU Nonresident
   *110 - 1052 Nonresident
   *1C0 - Diagnostic Monitor
   *200 - Storage Protect
   *300 - 2311 Part 1
   *310 - 2311 Part 2
   *320 - 2311 Part 3
   *400 - 1403 Part 1
   *410 - 1403 Part 2
   *420 - 1403 Part 3
   *500 - 2540 Part 1
   *510 - 2540 Part 2
   *600 - Channel
   *800 - 2560 Part 1
   *810 - 2560 Part 2
   *820 - 2560 Part 3
   Channel Bootstrap Card
   *E60 - System/360
   Channel Bootstrap Card
   *E20 - System/360 Model 20
3. Make reader ready; press END OF FILE
4. Select reader address on CPU console.
5. Press CPU load key.
   The reader will stop about midway through DEBE. At this point press the interrupt key to complete loading DEBE.
6. The console printer will then print this message:

   ENT PROG ID - XX

   Enter CT EOB from console printer keyboard.
7. This message will then be printed:

   ENT ADDR OF OUTPT TAPE - MMAAA

   Enter tape drive address EOB
   Example 00181
8. At completion of card to tape operation, identify the reel of magnetic tape as the DPP.

The procedure for using the 80-80 card to tape function of the micromonitor is as follows.

1. CSL the micromonitor (*1C0)
2. Set monitor sense switch 7 and store the tape address in auxiliary storage 008D.
   Example: (Tape Address = 80)
   a) Press the alter/display key.
   b) Enter from the 1052, SC7 EOB.
   c) Enter from the 1052, AA 008D 80 EOB.
3. Set FFFF in the console switches and press CPU load key.
4. A message will be printed on the console printer describing the action to be taken.

   ```
   $ TO LOAD NEW SECTION FROM NATIVE 2540.
   DO NPRO AND MAKE READY WITH ADDITIONAL
   SECTION(S). EOF ON.
   ```

   Example:
5. NPRO the reader used initially to load the micromonitor.
6. Load the decks in the card reader. The sequence of cards is the same as described in step 2 under the DEBE procedure with the exception of the DEBE deck.
7. Make reader ready; press END OF FILE.
8. Column 36 through 80 of the first card of each microprogram deck will be printed on the console printer as that card is written on tape. This printout can be retained as a record of the contents of the tape.

   Example: `128500 DIAG---BASIC CPU 0EC0*1000-01`
9. When the card-to-tape operation is complete, the same message as in step 4 will be printed on the console printer.
10. Identify the reel of magnetic tape as the DPP.

Note: If an I/O error is encountered with DEBE or the 80-80 card to tape micromonitor function, the error will be indicated via a 1052 console printout. The respective procedure for generating the DPP tape must be restarted at its beginning.

Macrodiagnostics

The following macrodiagnostics are included in the System/360 Model 25 field maintenance package. Descriptions and listings are provided in volume 40 of the logic binders. Those released previously and in common use on other systems are indicated by an asterisk (*). Descriptions are not provided for diagnostics released previously.

MONITOR

*1. DMA4 - 3020
*2. Message Editor - 310A
3. Expansion section - E10B

This allows DMA4 to adjust itself and become more flexible if core storage is available. The areas of increased capabilities are:

a. The number of UDT entries is expanded from 28 to 100.
b. A typewriter input language compatible with DMA8 has been incorporated.
c. System configuration can be set up by English language statements in TXT cards.
d. UDT table can be set up via DMA4 or DMA8 UDT cards.
e. Diagnostic information is available via console printer.

The expansion section adjusts itself with DMA4 according to the following rules:

a. The expansion section is aborted if the proper level of DMA4 is not loaded.
b. Typewriter input is activated only on systems having DM input device identified as a 90.
c. The expansion routines are placed in 3000 - 3FFF on 16K systems not having the DM editor (310A) loaded.
d. On 16K systems having the editor loaded, an option is given to the user to maintain the editor and abort the expansion section or vice versa.
e. The expansion section and tables will be located in 4000 to 4FFF (thus preserving the DM editor if it is loaded) on systems greater than 16K. New diagnostic sections have been released for the integrated attached I/O device. These sections require unique UDT entries:

1043 Printer	8F
2311 File	67
2540 Reader/Punch	8B

The program listing for DMA4 expansion provides explanation of the status messages, instructions to operator, etc., that are pertinent to the section.

Diagram 1-1; Using the Diagnostic Program Package (Part 8 of 9)

*EXTERNAL INTERRUPT/DIRECT CONTROL - 34E1

2311 Microdiagnostics

C675 File Function
C676 File Function
C677 File Function
C678 File Function
C679 File Function
C67A File Function
C67B File Scan
C67C 2311 Diagnostic Test
C67D 2311 Diagnostic Test

SYSTEM/360 MODEL 20 MODE (2560)

The following System/360 Model 20 MFT macrodiagnostics are available for execution in the System/360 Model 20 Mode to ascertain proper operation of the 2560 MFCM.

MFT 2041 Ripple Read
MFT 2042 Ripple Punch
MFT 2043 Ripple Card Print
MFT 2045 Ripple Read (Column binary)
MFT 2061 Stacker Select
MFT 2062 Print Head Select
MFT 2072 I/O Short Program
MFT 2073 Read Error Last Card
MFT 2080 Speed Test
MFT 2090 Read Adjustment

The following MFT test decks consist of data cards for use with the MFT tests indicated:

MFT 2031 Ripple Data Cards (for MFT 2041)
MFT 2032 Column Binary Data Cards (for MFT 2045)
MFT 2033 Read Error Last Card Data Cards (for MFT 2073)
MFT 2034 Read Adjustment Data Cards (for MFT 2090).

ICR 125 test deck is designed to run under *E90 microdiagnostic coreload.

**MFT2072 should be used only for 2560 problems. The least number of commands that will bring on a failure should be generated. A unique sequence of commands may be generated to simulate the I/O program conditions that are causing machine failure. Other devices (1403, 2501, 1442, etc.) may be operated simultaneously with the 2560, if needed, to develop the failure.

SYSTEM ENVIRONMENT TEST

The SYST-M30-B system environment test is used by the customer engineer to exercise and test the system. This program is designed to allow the customer engineer to operate the System/360 Model 25 in a manner similar to worst case customer operation. The vigorous random internal and I/O exercising done by the program assures that intermittent, timing sensitive, or program-oriented troubles will be detected. The results of this test are logged internally and are printed out automatically at frequent break points as well as being available at any time they are requested.

The I/O units that this test can exercise are 2540, 1403, 1442N1, 1443, 1050, 2400 series tape units, and 2311 files.

INTEGRATED COMMUNICATIONS ATTACHMENT

Physical Wrap Test

To run the macrodiagnostic physical wrap tests (C4F1, C4F2, C4F3, C4F4) a wrap connector (P/N 2543186) must be utilized.

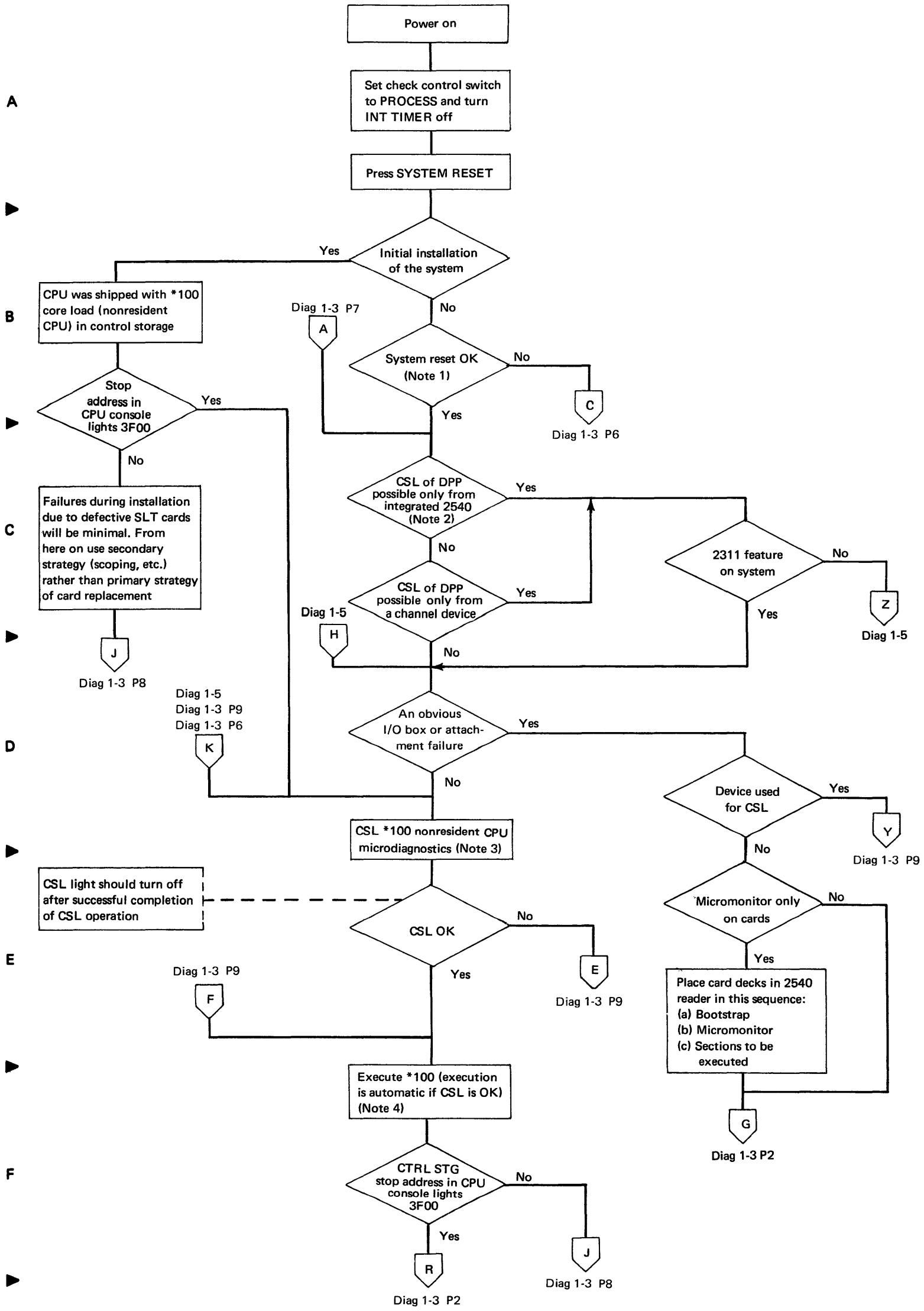
This connector is to be installed on the I/O Gate (01E) in the location of the lines to be tested prior to loading the macrodiagnostics. Each connector has the capability to wrap two pairs of lines or just a single pair depending on the system configuration.

Note of Caution: This wrap connector *cannot* be used with a terminal control Type I telegraph board.

Macrodiagnostics

ID Number	
CBB0	Binary Synchronous Function
CBB1	Binary Synchronous Function
CBB2	Binary Synchronous Function
CBB3	Binary Synchronous Function
CBB4	Binary Synchronous Function
CBB5	Binary Synchronous Function
CBB6	Binary Synchronous Function
CBB7	Binary Synchronous Function
CBB8	Binary Synchronous Function
CBB9	Binary Synchronous Function
CBBA	Binary Synchronous Function
CBBB	Binary Synchronous Function
CBBC	Binary Synchronous Multipoint Function
ED60	Binary Synchronous diagnostics can request test message from central BTAM control.
CBE1	IBM 1 Line Adapter Test
CBE2	IBM 1 Line Adapter Test
CBE3	IBM 1 Line Adapter Test
CBE4	IBM 1 Line Adapter Test
CBE5	IBM 2 Line Adapter Test
CBE6	IBM 2 Line Adapter Test
CBE7	IBM 2 Line Adapter Test
CBE8	TLG1 Line Adapter Test
CBE9	TLG1 Line Adapter Test
CBEA	TTY Line Adapter Test
CBEE	Autodial Test
C4EE	Multicom Configurator
C4EF	Multicom 16K
C4F0	Multicom 32K
C4F1	IBM 1 Physical Wrap
C4F2	IBM 2 Physical Wrap
C4F3	TLG Physical Wrap
C4F4	TTY Physical Wrap
C4F5	1050 Terminal Exerciser
C4F6	2740 Terminal Exerciser
C4F7	1060 Terminal Exerciser
C4F8	1030 Terminal Exerciser
C4F9	TLG Terminal Exerciser
C4FA	TTY Terminal Exerciser
C4FB	2780 Terminal Exerciser
C4FC	IBM 1 Autowrap
C4FD	IBM 2 Autowrap
C4FE	TLG Autowrap
C4FF	TTY Autowrap

Diagram 1-1 Using the Diagnostic Program Package (Part 9 of 9)



Notes:

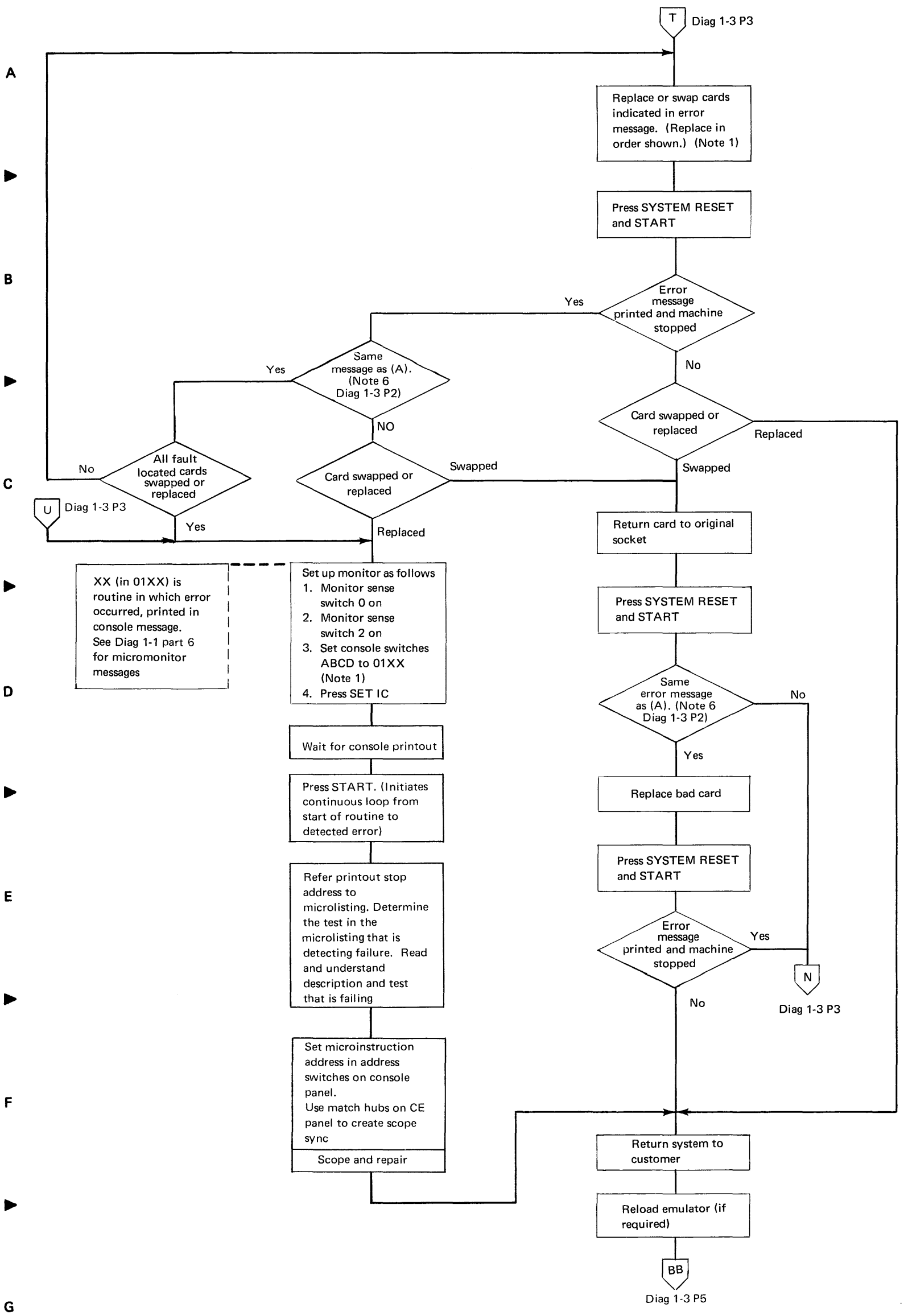
(1) An OK system reset is indicated by all of the following.
- (a) No check lights
- (b) Manual light off then on
- (c) System light on then off
- (d) CPU console lights for byte 0 is 00000000 and parity bit is off.
- (e) No checksum error.

(2) DPP (Diagnostic Program Package)
Where alternate input devices are available, the complete diagnostic program package should be kept in appropriate form to use these devices for CSL.
The recommended order for using the alternate CSL capability is:
- (a) Disk
- (b) Tape
- (c) Card

(3) For CSL of nonresident microdiagnostics from cards, place decks in hopper of reader at this point, in sequence indicated:
- (a) Bootstrap
- (b) Nonresident CPU
- (c) 1052
- (d) Micromonitor
- (e) Section(s) to be executed.

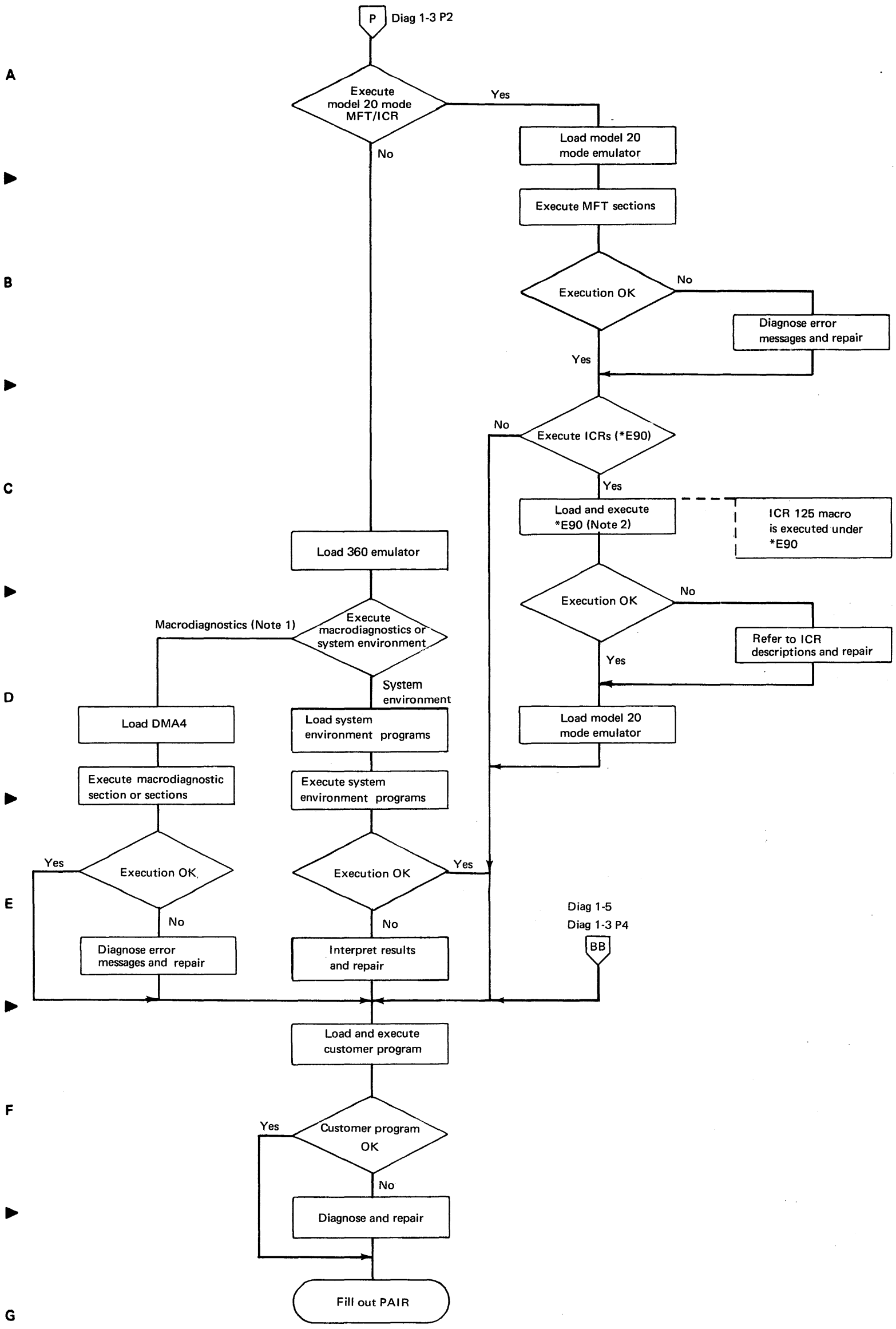
(4) *100 can be looped by setting console switches A,B to 00 and pressing SYSTEM RESET.

Diagram 1-3. Diagnosis Techniques Diagrams (Part 1 of 10)



Notes:
(1) Use these guidelines with the card fault list:
  (a) If number of suspect cards is 12 or less, replace all cards in order shown.
  (b) If number of suspect cards is more than 12, replace the first 12 in order shown, then go to secondary strategy.

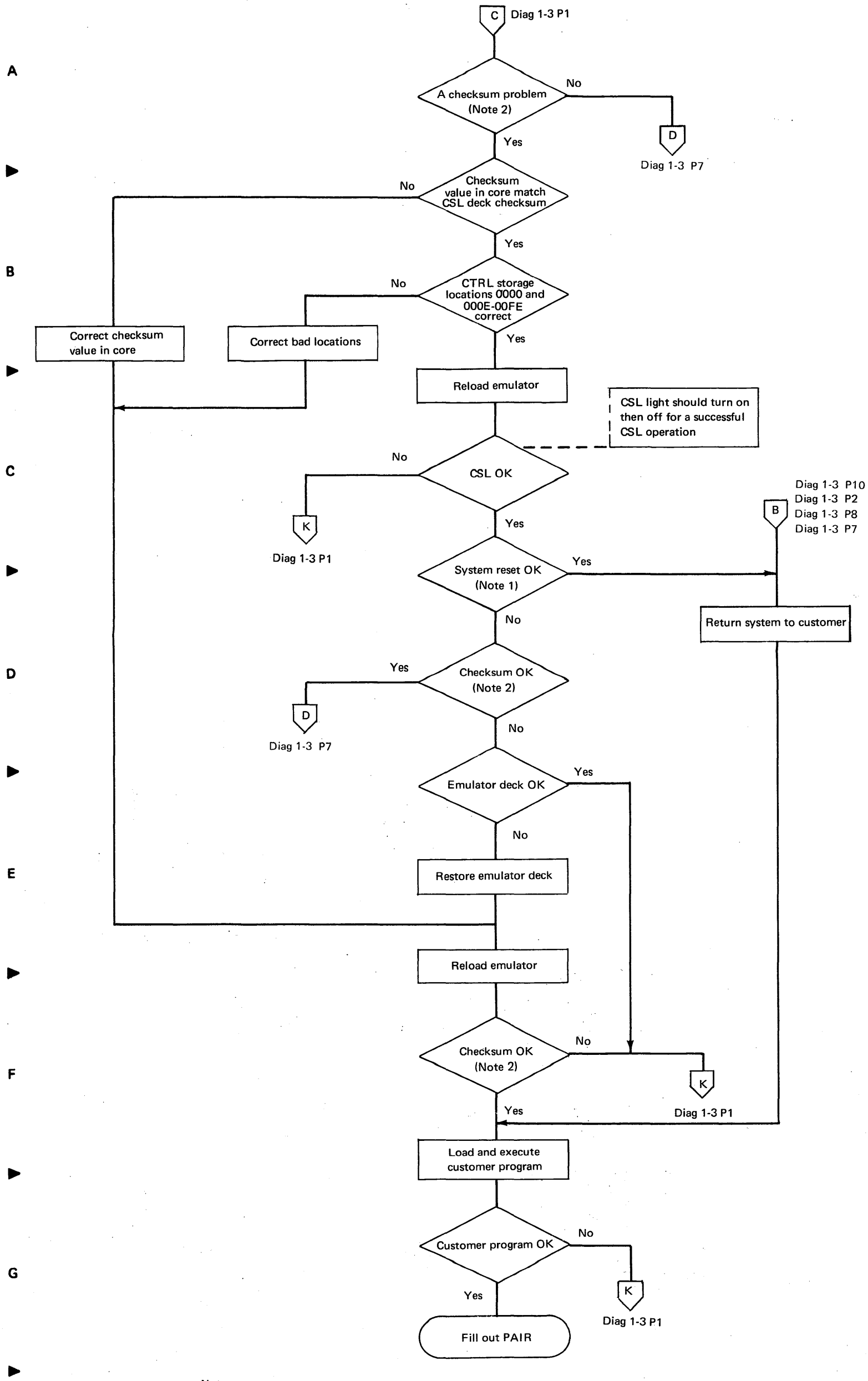
● Diagram 1-3. Diagnosis Techniques Diagrams (Part 4 of 10)



Notes:
(1) Macrodiagnostic programs are provided only for 2311 and channel attached I/O devices under 360 emulator.

(2) Microlisting for routine NAAB provides instructions for executing *E90

● Diagram 1-3. Diagnosis Techniques Diagrams (Part 5 of 10)



Notes:

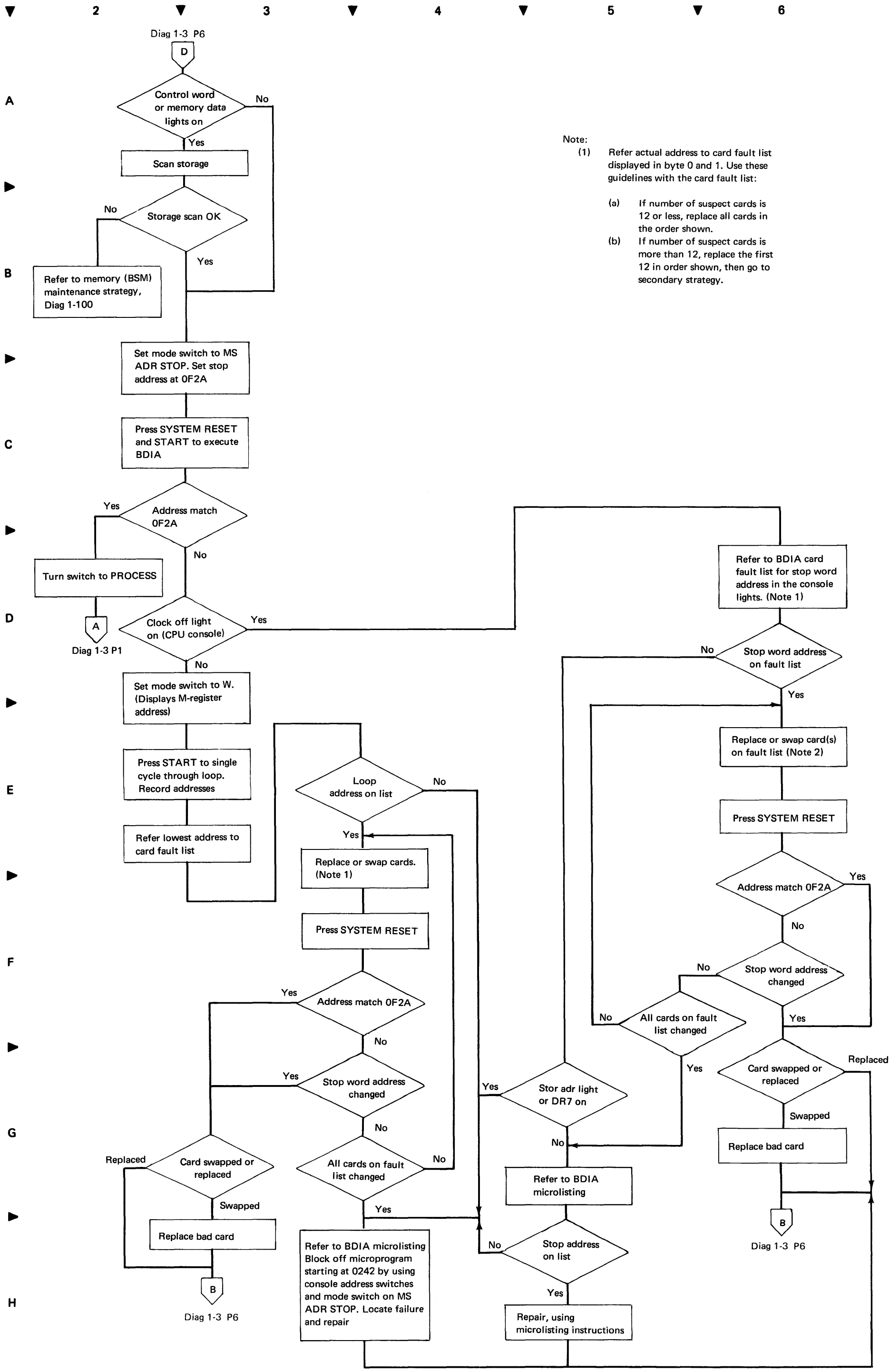
(1) An OK system reset is indicated by all of the following.
- (a) No check lights
- (b) Manual light off then on
- (c) System light on then off
- (d) Byte 0 in console lights is 00000000 with parity bit off.
- (e) No checksum error.

(2) A bad checksum is indicated as follows.

CE key off - Stop with console checksum light on

CE key on - Two line printout on console printer. (Refer to example on Diagram 1-1 P7.)

● Diagram 1-3. Diagnosis Techniques Diagrams (Part 6 of 10)



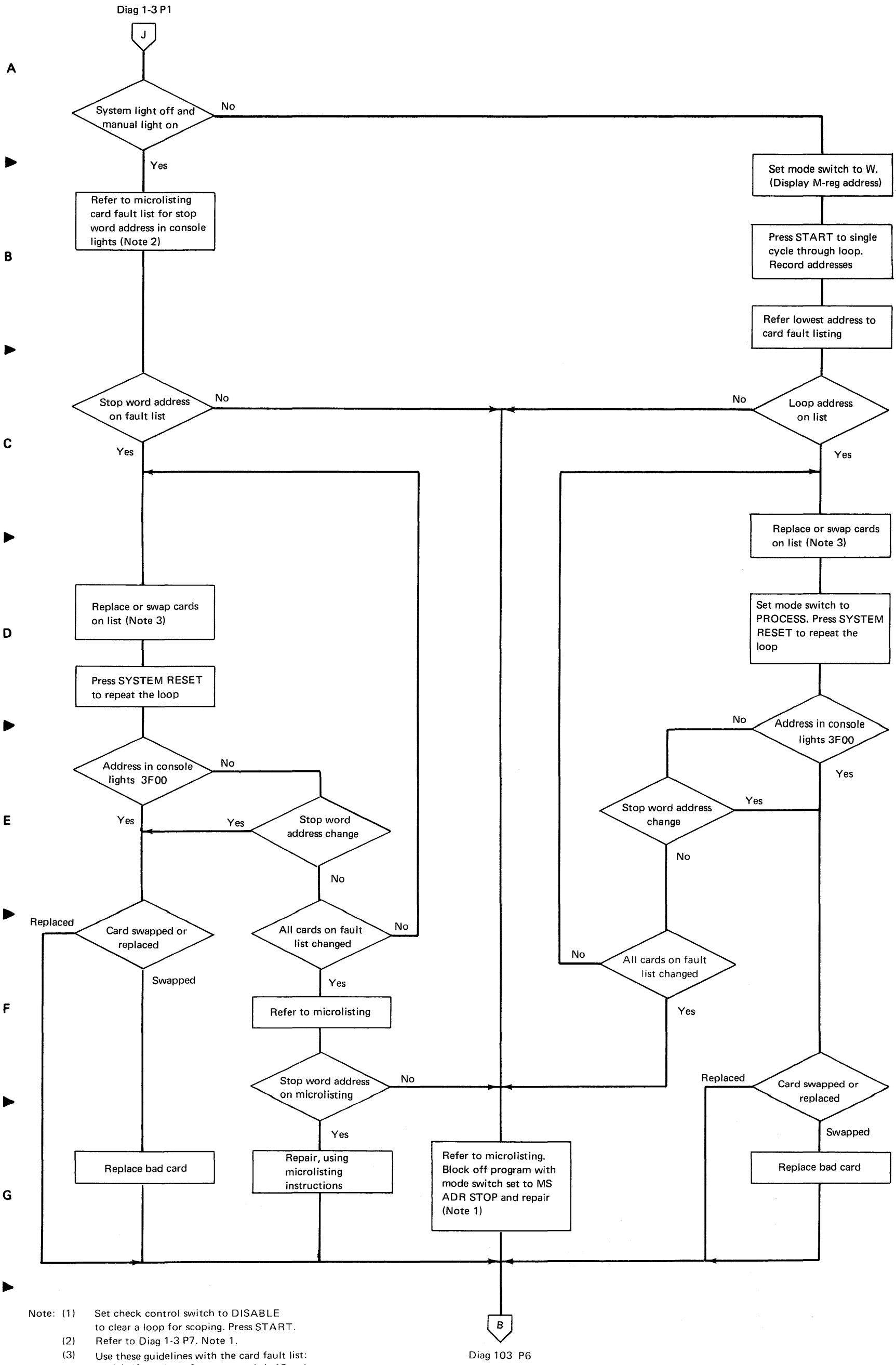
Note:

(1) Refer actual address to card fault list displayed in byte 0 and 1. Use these guidelines with the card fault list:

(a) If number of suspect cards is 12 or less, replace all cards in the order shown.

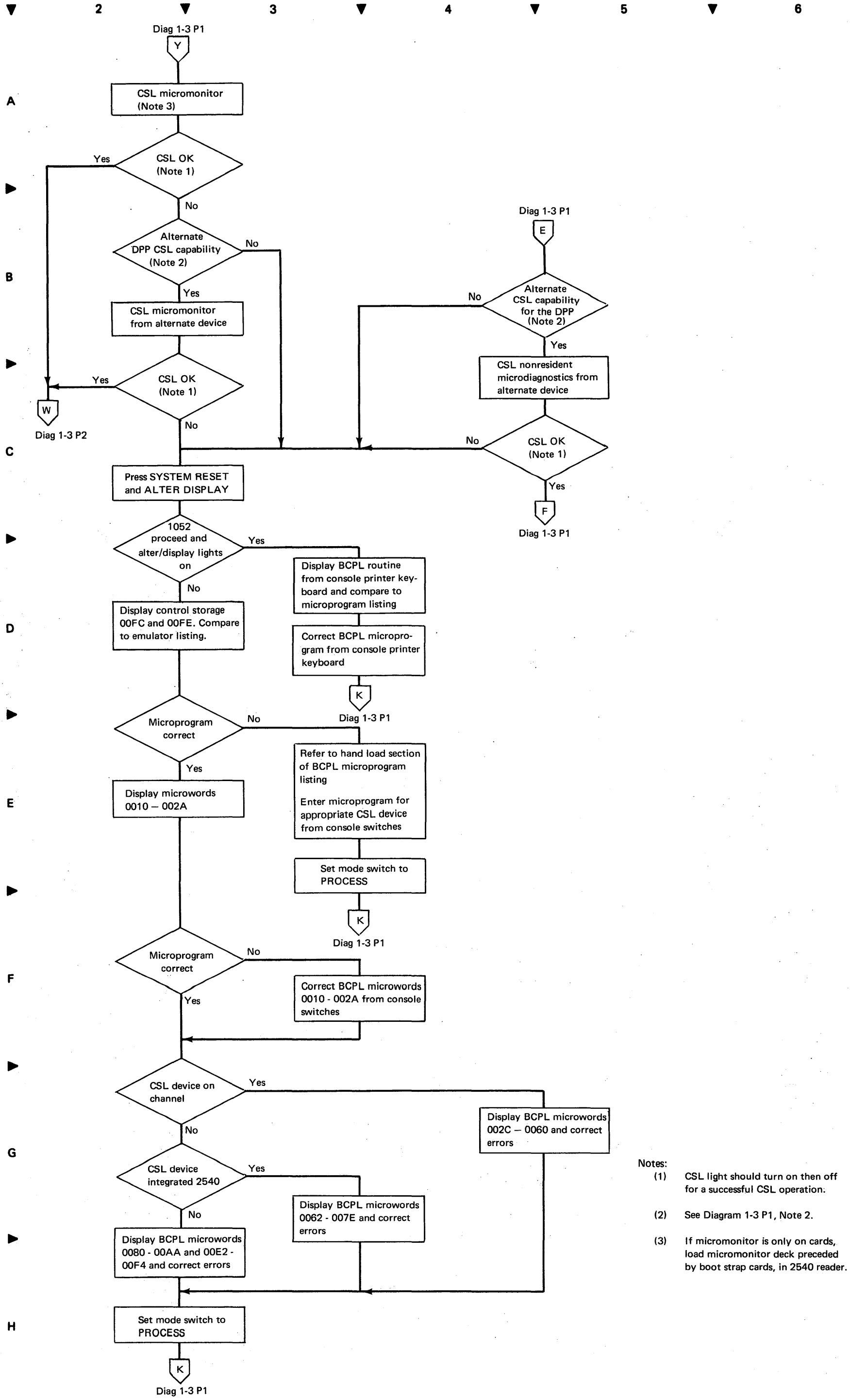
(b) If number of suspect cards is more than 12, replace the first 12 in order shown, then go to secondary strategy.

● Diagram 1-3. Diagnosis Techniques Diagrams (Part 7 of 10)



Note: (1) Set check control switch to DISABLE to clear a loop for scoping. Press START.
(2) Refer to Diag 1-3 P7. Note 1.
(3) Use these guidelines with the card fault list:
(a) If number of suspect cards is 12 or less, replace all cards in the order shown.
(b) If number of suspect cards is more than 12 replace the first 12 in order shown, then go to secondary strategy.

● Diagram 1-3. Diagnosis Techniques Diagrams (Part 8 of 10)



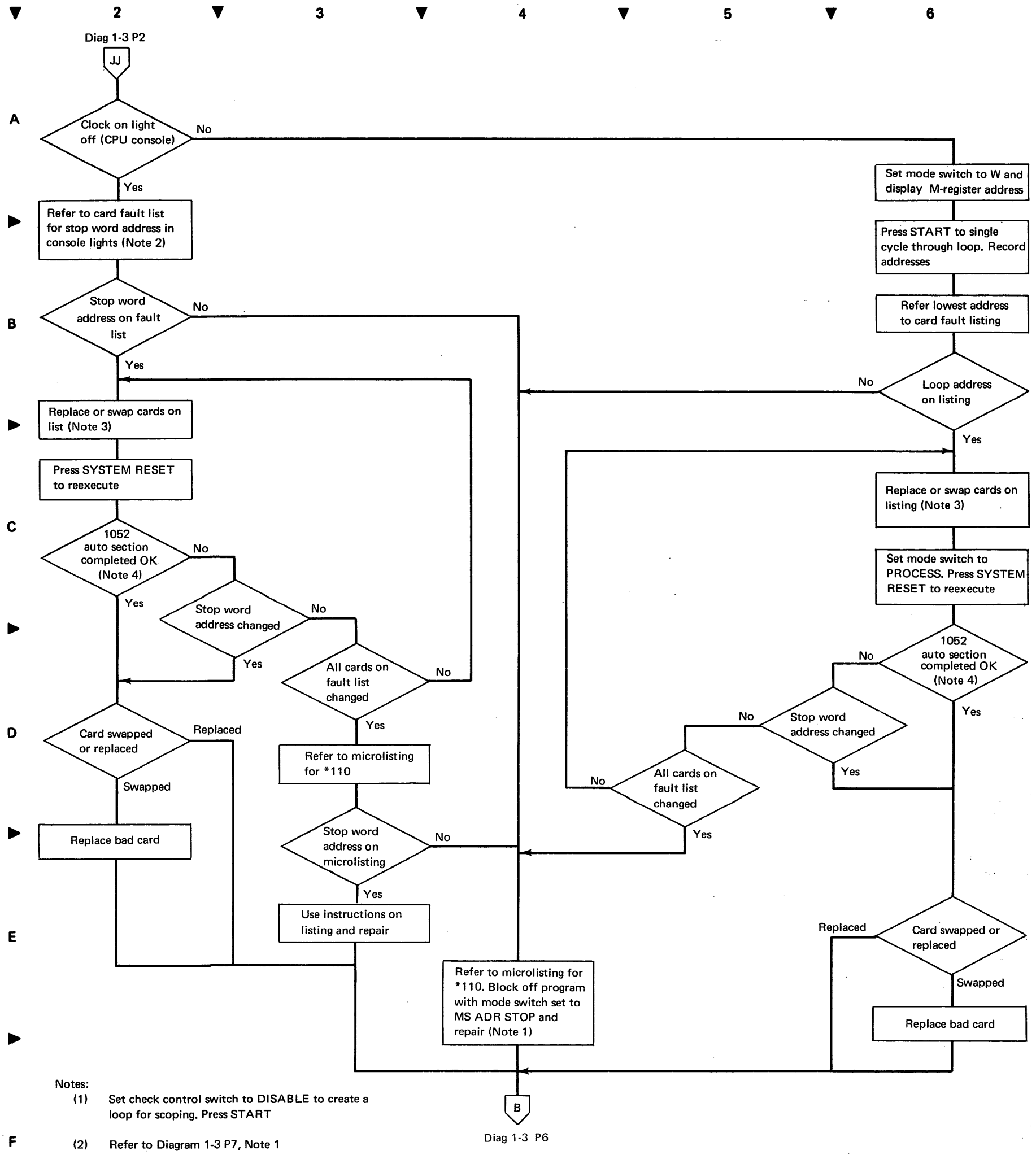
Notes:

(1) CSL light should turn on then off for a successful CSL operation.

(2) See Diagram 1-3 P1, Note 2.

(3) If micromonitor is only on cards, load micromonitor deck preceded by boot strap cards, in 2540 reader.

● Diagram 1-3. Diagnosis Techniques Diagrams (Part 9 of 10)



Notes:

(1) Set check control switch to DISABLE to create a loop for scoping. Press START

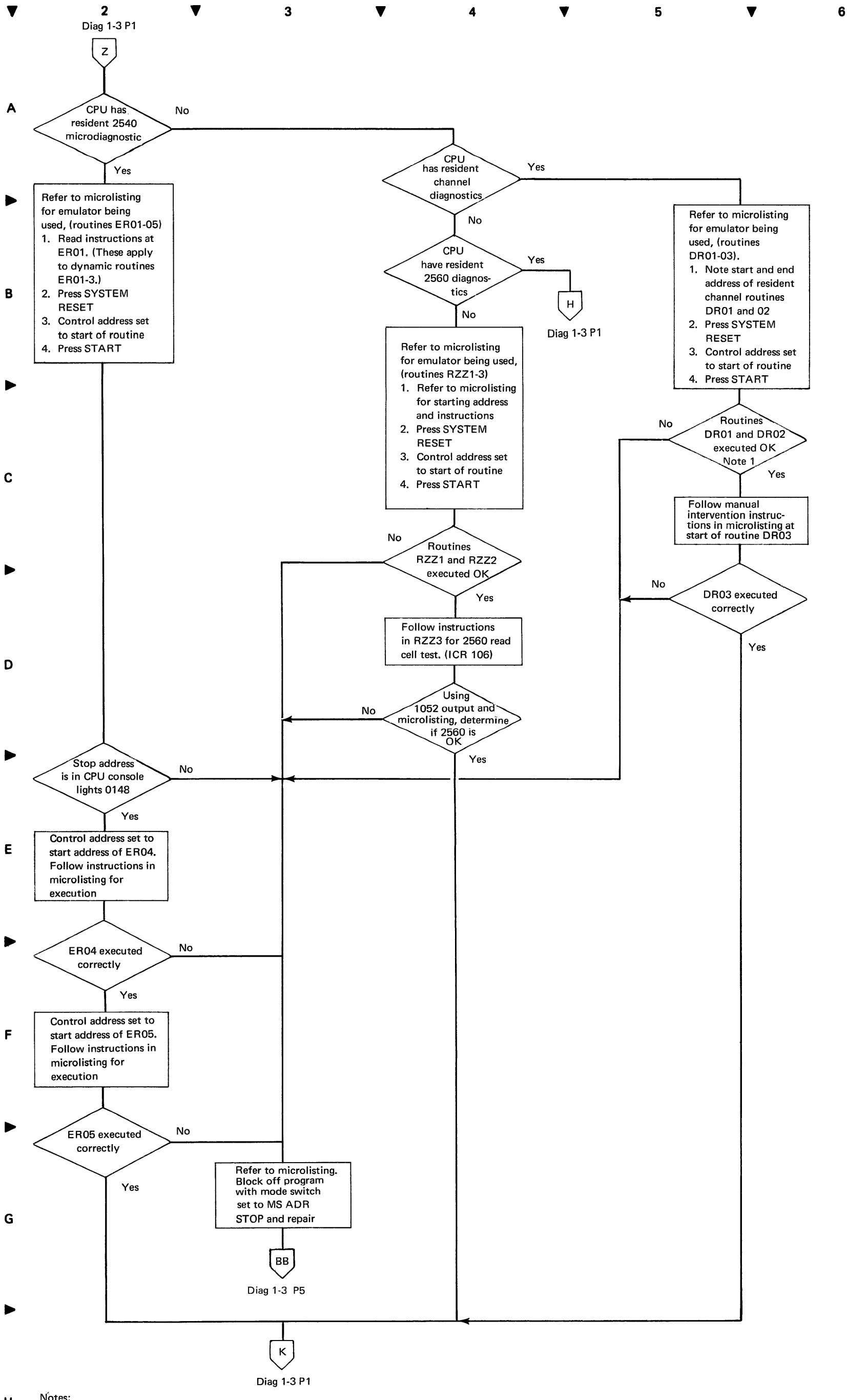
(2) Refer to Diagram 1-3 P7, Note 1

(3) Use these guidelines with the card fault list:

(a) If number of suspect cards is 12 or less, replace all cards in the order shown.
(b) If number of suspect cards is more than 12, replace the first 12 in order shown, then go to secondary strategy.

(4) Refer to Diagram 1-3 P2, Note 5.

● Diagram 1-3. Diagnosis Techniques Diagrams (Part 10 of 10)



Notes:

(1) DR01 and DR02 execute automatically; DR03 requires manual intervention. If DR01 and DR02 execute correctly, the CPU will stop at the point manual intervention is required in DR03; follow the instructions in the DR03 microlisting.

● Diagram 1-5. Resident 2540, 2560 Channel Microdiagnostics

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Memory Diagnostic Technique Diagrams

A

The following diagnostic strategy diagrams should be used when troubleshooting a memory failure. Used with the operator's console, these diagrams provide a comprehensive diagnostic tool for locating and correcting memory failures.

Use *130 Memory Microdiagnostic on systems with two memory modules (more than 16K of program storage) when the failure is occurring in only one of the modules. The microlisting for *130 provides the necessary instructions for setup and execution of this microdiagnostic.

B

C

D

E

F

G

H

● Diagram 1-100. Memory Diagnostic Technique Diagrams

SCAN STORAGE

1. Mode switch to single cycle position
2. Diagnostic control switch to scan stor
3. Mode switch to process
4. Check control switch to stop (unless specified otherwise)
5. System reset
6. Start

LOAD PROG STORAGE

1. Mode switch to single cycle position
2. ABCD switches to data to be stored [$X_1X_2X_2X_2$ (Hex)]
3. Diagnostic control switch to load prgm stor
4. Mode switch to process
5. Check control switch to stop (unless specified otherwise)
6. System reset
7. Start

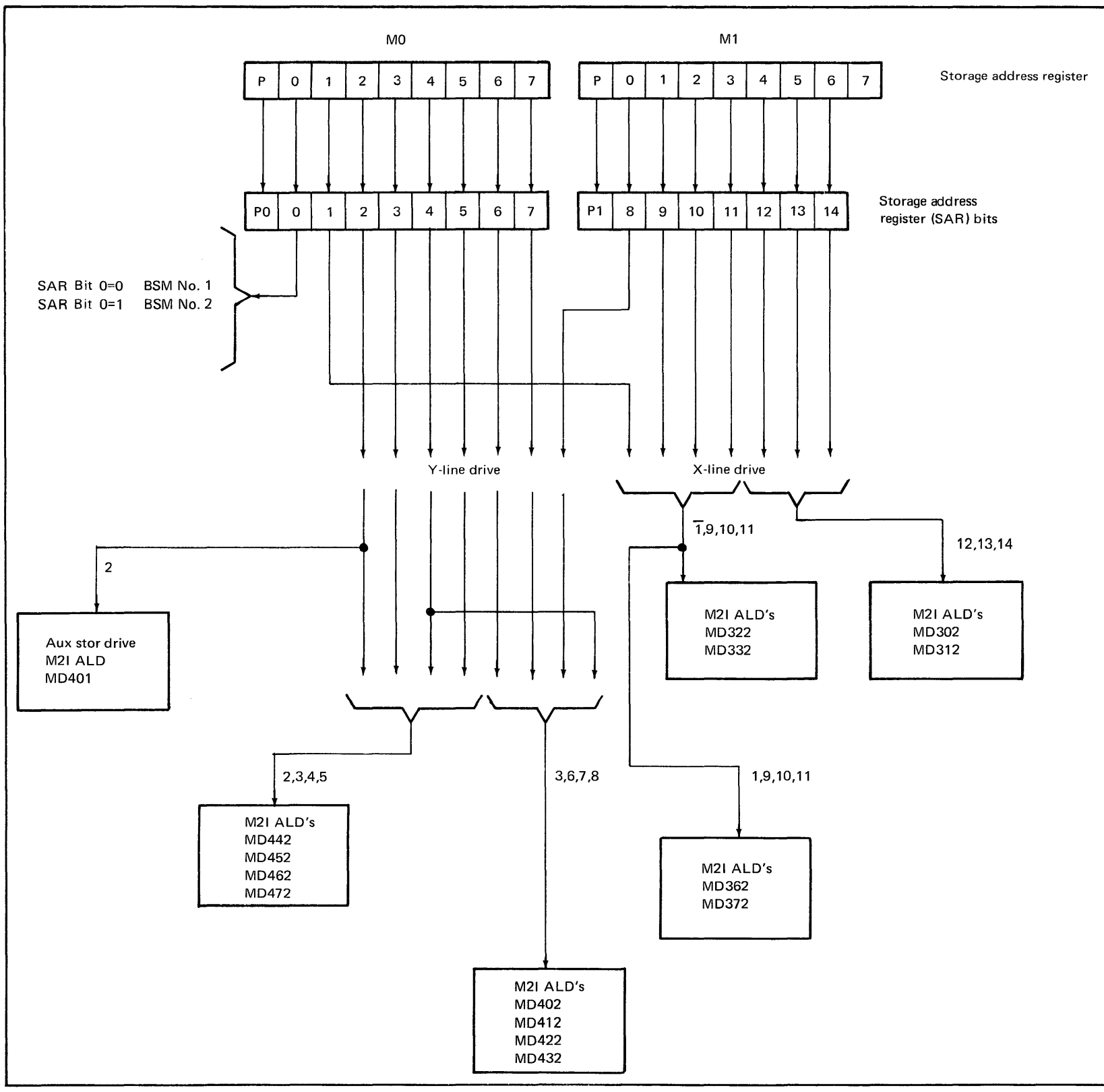
SINGLE ADDRESS SCAN (At Address 0000)

1. Mode switch to single cycle position
2. Diagnostic control switch to single adr ms
3. Mode switch to process
4. Check control switch to stop (unless specified otherwise)
5. Set switches ABCD to address to be scanned
6. System reset
7. Control address set and start

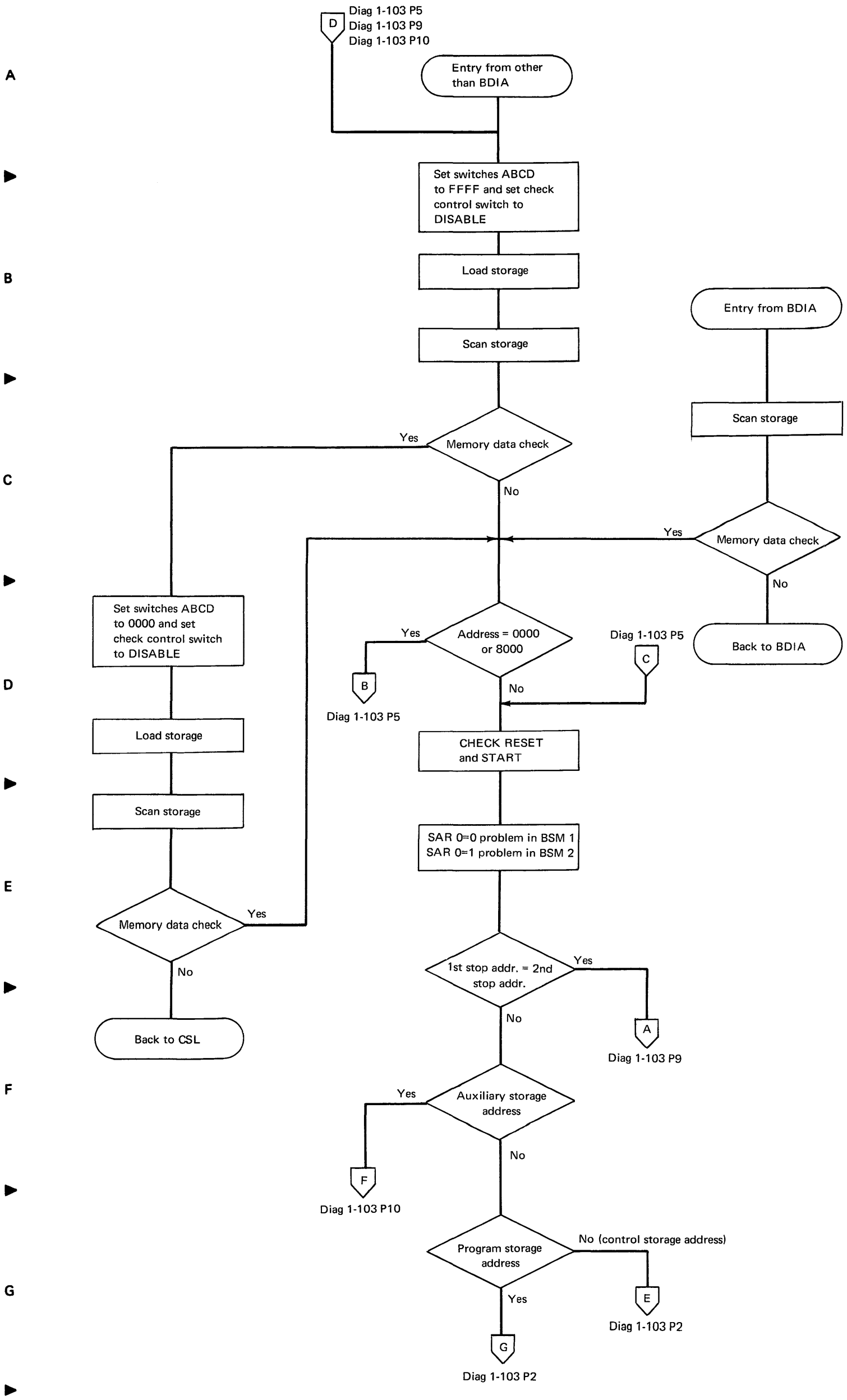
LOAD STORAGE (Control storage addresses 0000-00FE are accessed but contents remain unchanged)

1. Mode switch to single cycle position
2. ABCD switches to data to be stored
3. Diagnostic control switch to load stor
4. Mode switch to process
5. Check control switch to stop (unless specified otherwise)
6. System reset
7. Start

Memory Diagnostic Technique Console Scan Procedure



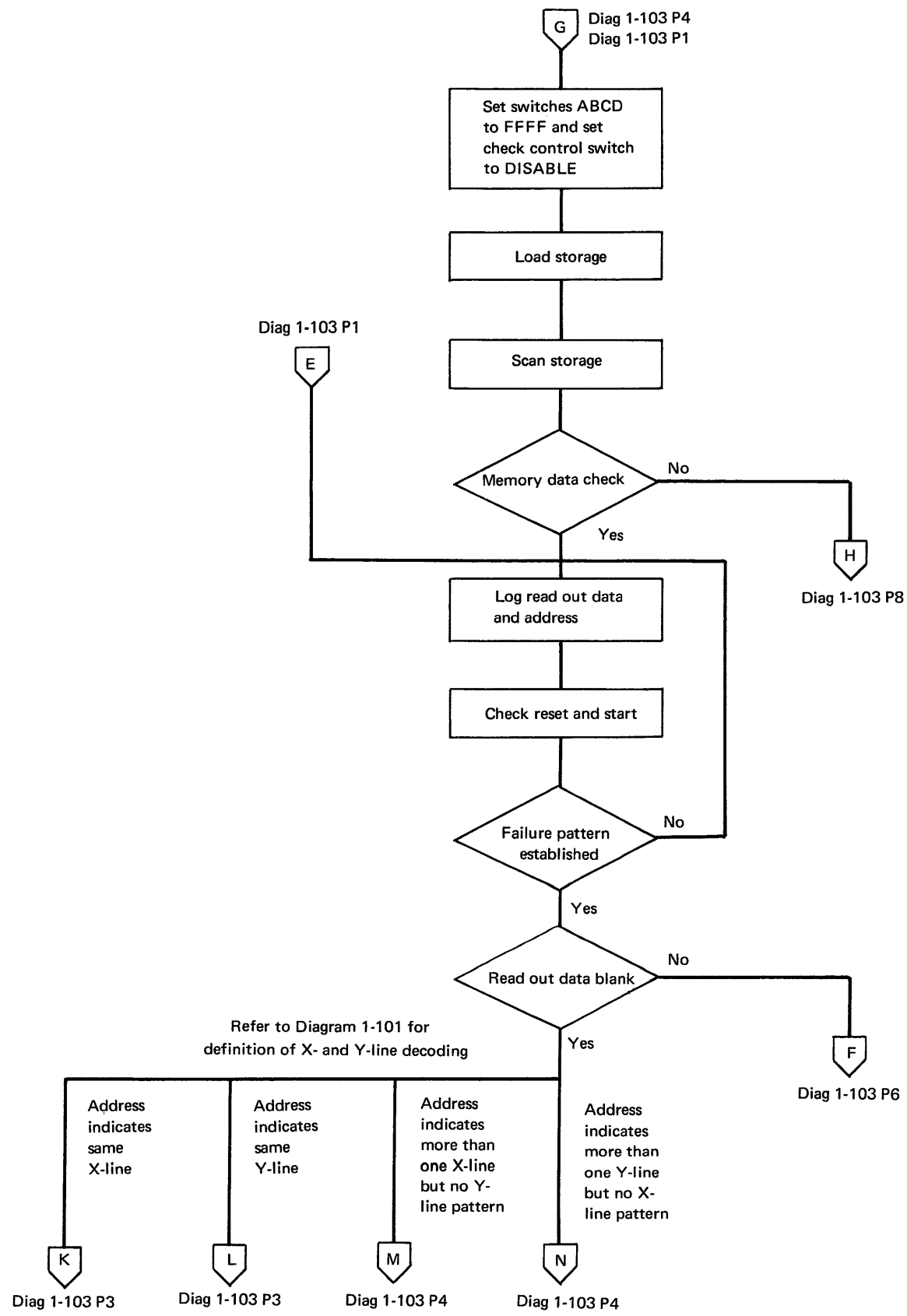
● Diagram 1-101. X-Line, Y-Line Decode Source and Memory Diagnostic Technique Console Scan Procedure



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 1 of 10)

2 3 4 5 6

A B C D E F G H



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 2 of 10)

2 3 4 5 6

A

Read out data blank for single X- or Y-line.

Diag 1-103 P2

K

SAR bit 1 = 0

No

Yes

Display a failing address + 4000 (hex)

B

Data blank

Yes

No

X-line drivers

Refer to M2I ALD's
MD 302
MD 312
MD 322
MD 332

Note 2

X-line drivers

Refer to M2I ALD's
MD 322
MD 332

Note 2

X-line drivers

Refer to M2I ALD's
MD 362
MD 372

Note 2

Diag 1-103 P2

L

Y-line drivers

Refer to M2I ALD's
MD 402
MD 412
MD 422
MD 432
MD 442
MD 452
MD 462
MD 472

Note 2

C

Notes:

(1) These include:
- (a) Array solder connections
- (b) Driver to array pin continuity
- (c) Contact and spring tension on array connector.

(2) Refer to Chapter 1 of 2025 FEMM for X-line and Y-line card locations.

Swap cards

For program storage, repeat procedure beginning at Diag 1-103 P2 G. For control storage, repeat procedure beginning at Diag 1-103 P5 B

D

Yes

Change in failure pattern

No

Replace bad card.

Diag 1-103 P10

P

More cards to swap

Yes

No

E

Check for open drive line or diode

Yes

Open drive line or diode

No

F

Attempt to repair

Check drive line physical connections (Note 1)

2 BSMs

No

Yes

G

Swap arrays and try again

Problem switches to other BSM

No

Repaired

No

Yes

Yes

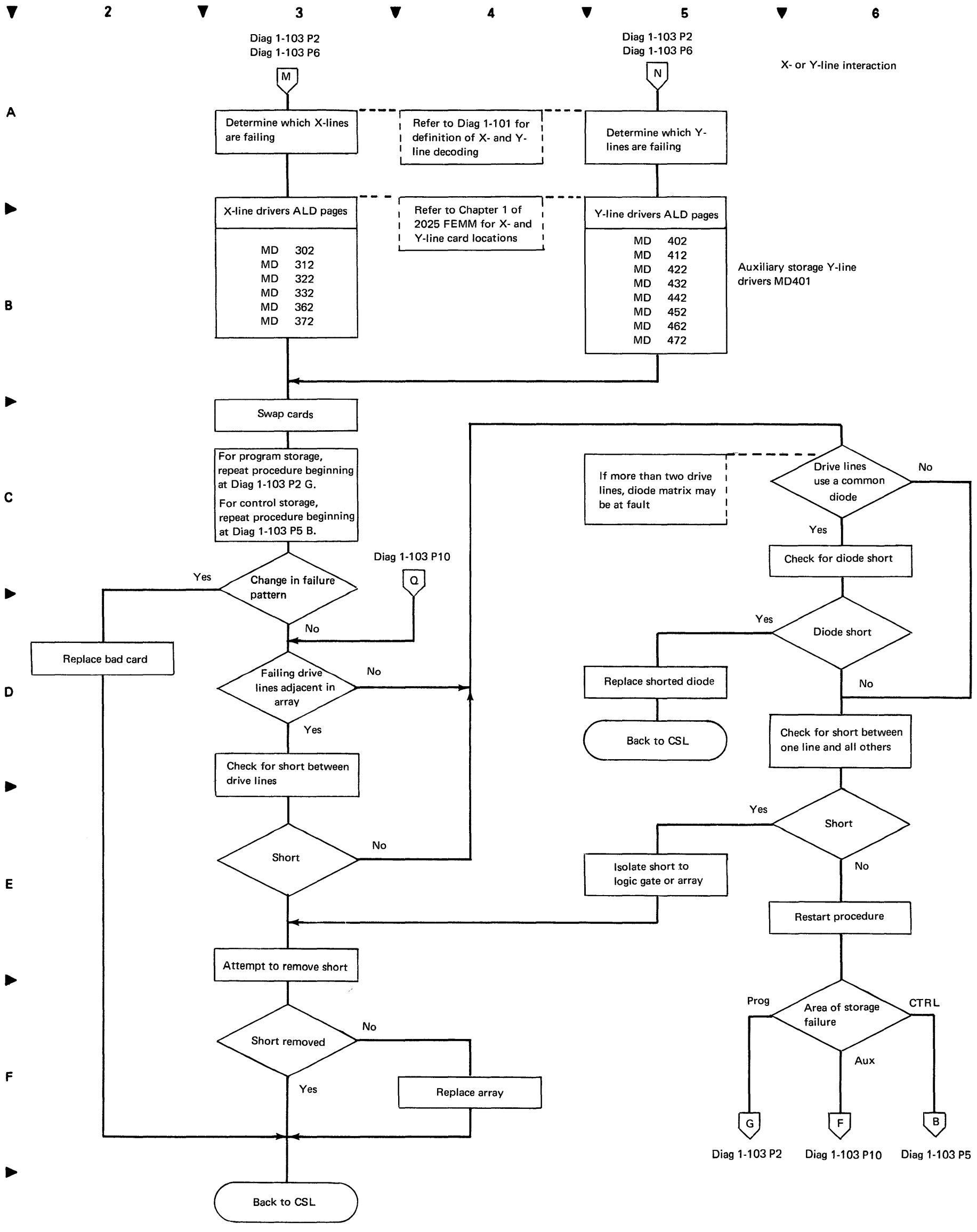
Replace array

Replace array and gate

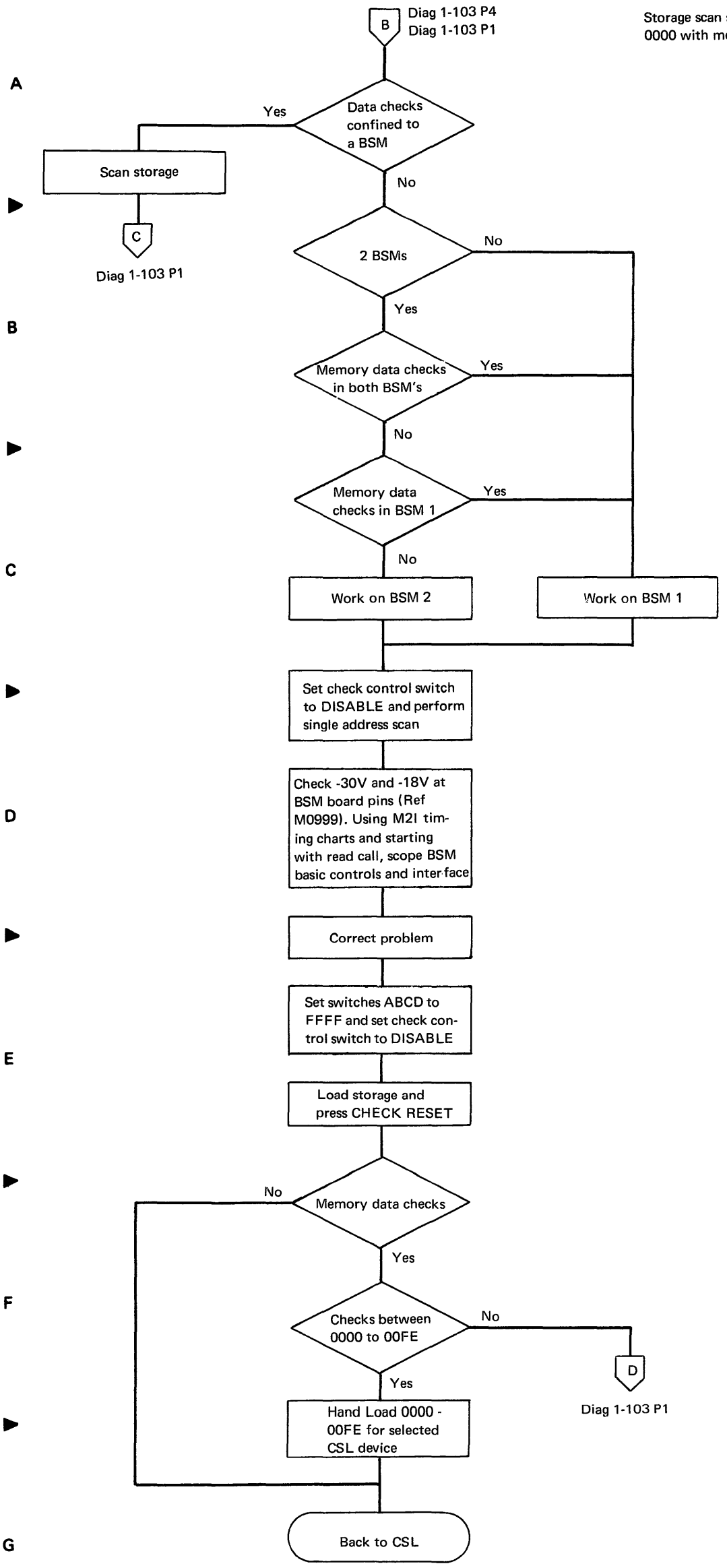
H

Back to CSL

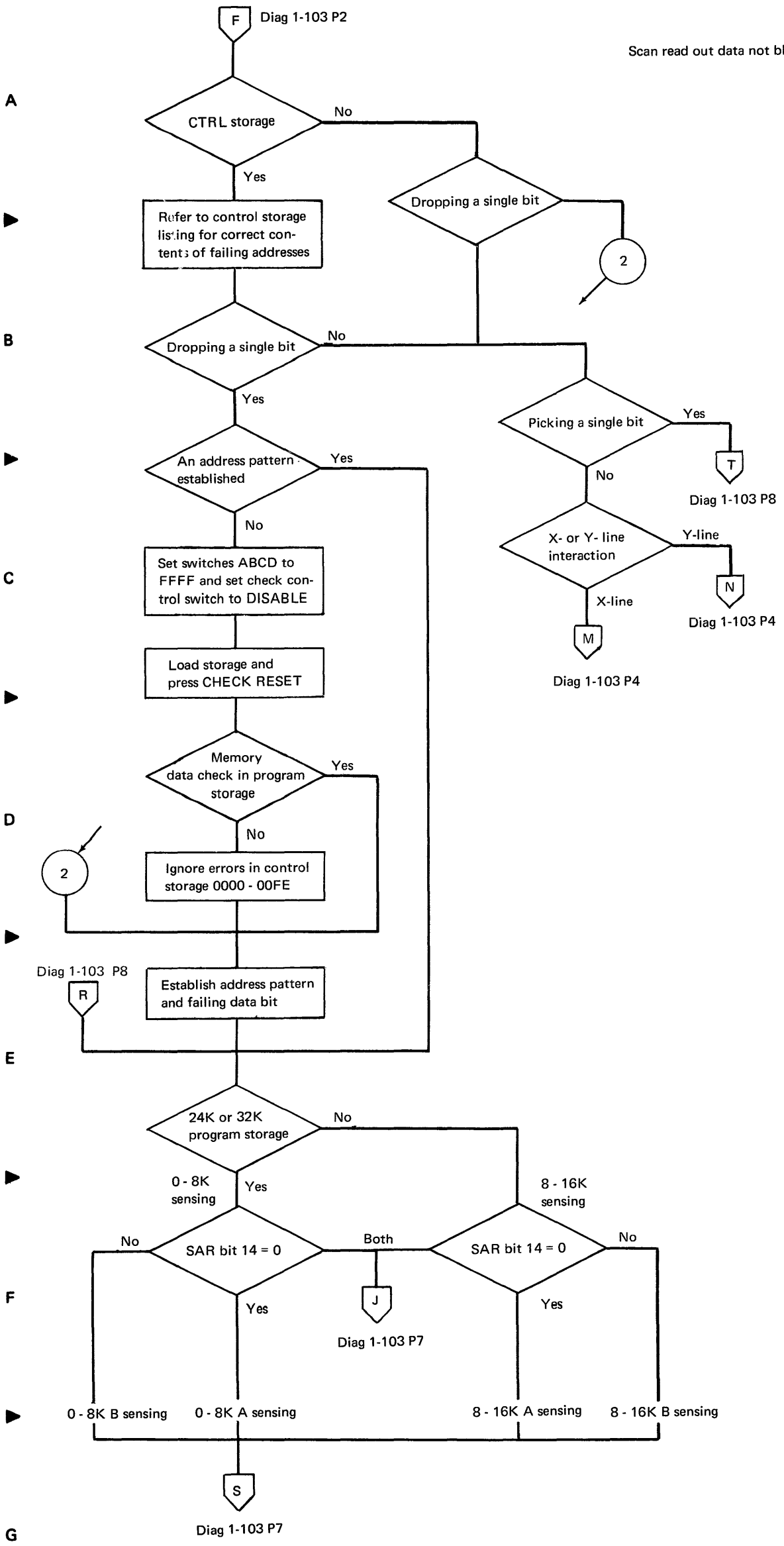
● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 3 of 10)



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 4 of 10)



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 5 of 10)



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 6 of 10)

2 3 4 5 6

Notes:

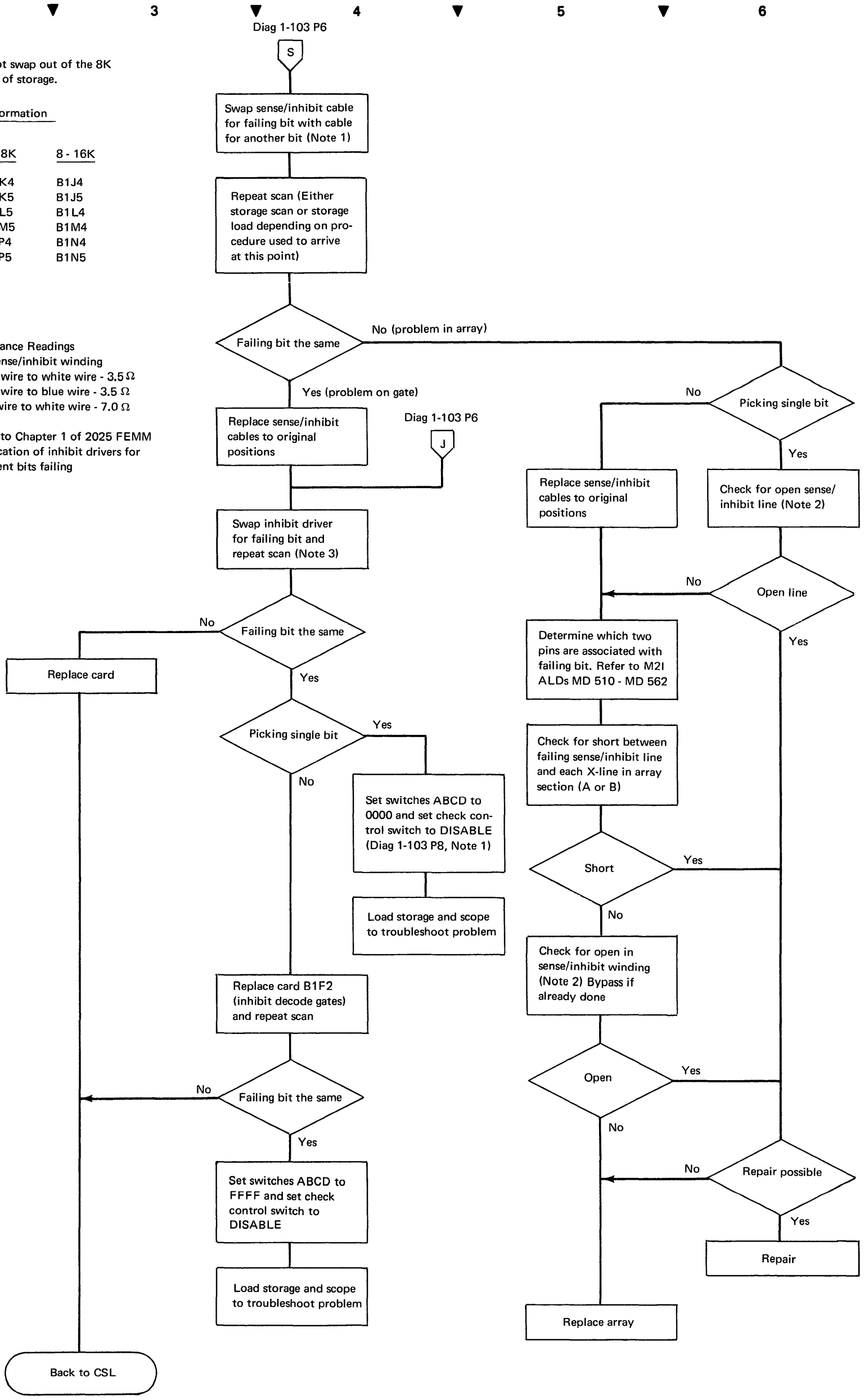
(1) Do not swap out of the 8K block of storage.

Cable information

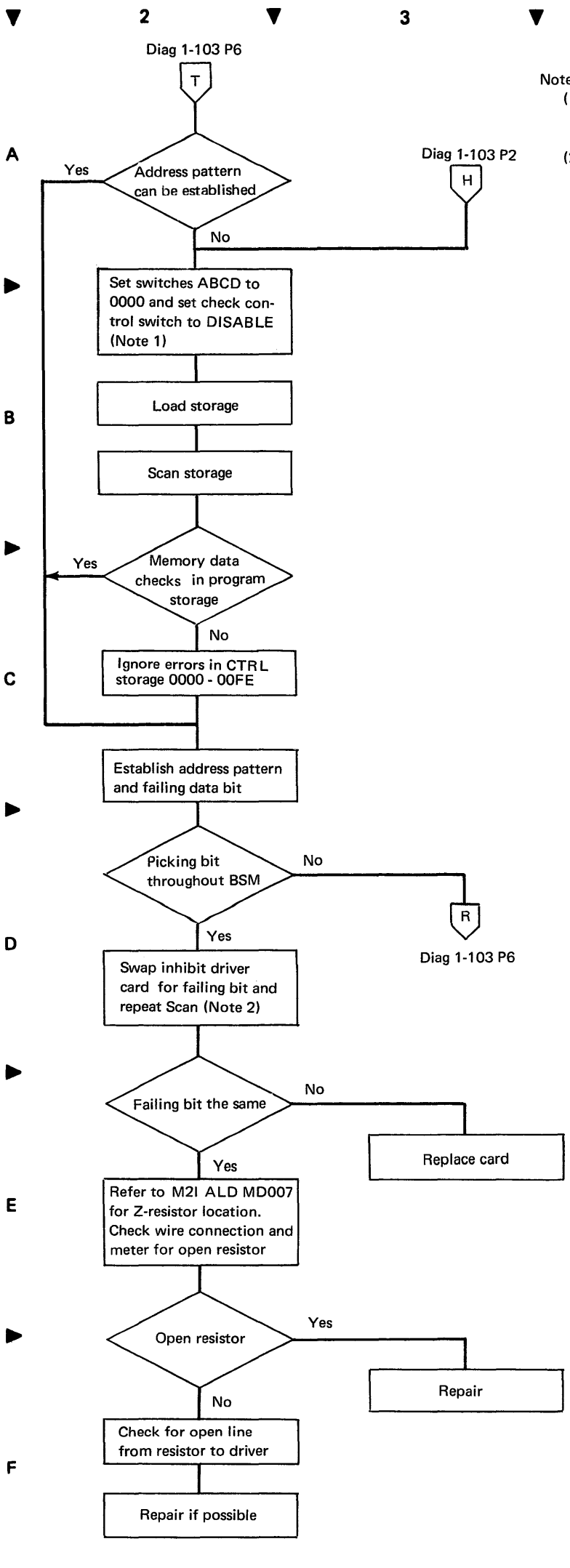
Date bits	0 - 8K	8 - 16K
0,1,2	B1K4	B1J4
3,4,5	B1K5	B1J5
6,7,P0	B1L5	B1L4
8,9,10	B1M5	B1M4
11,12,13	B1P4	B1N4
14,15,P1	B1P5	B1N5

(2) Resistance Readings
For sense/inhibit winding
Black wire to white wire - 3.5 Ω
Black wire to blue wire - 3.5 Ω
Blue wire to white wire - 7.0 Ω

(3) Refer to Chapter 1 of 2025 FEMM for location of inhibit drivers for different bits failing



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 7 of 10)



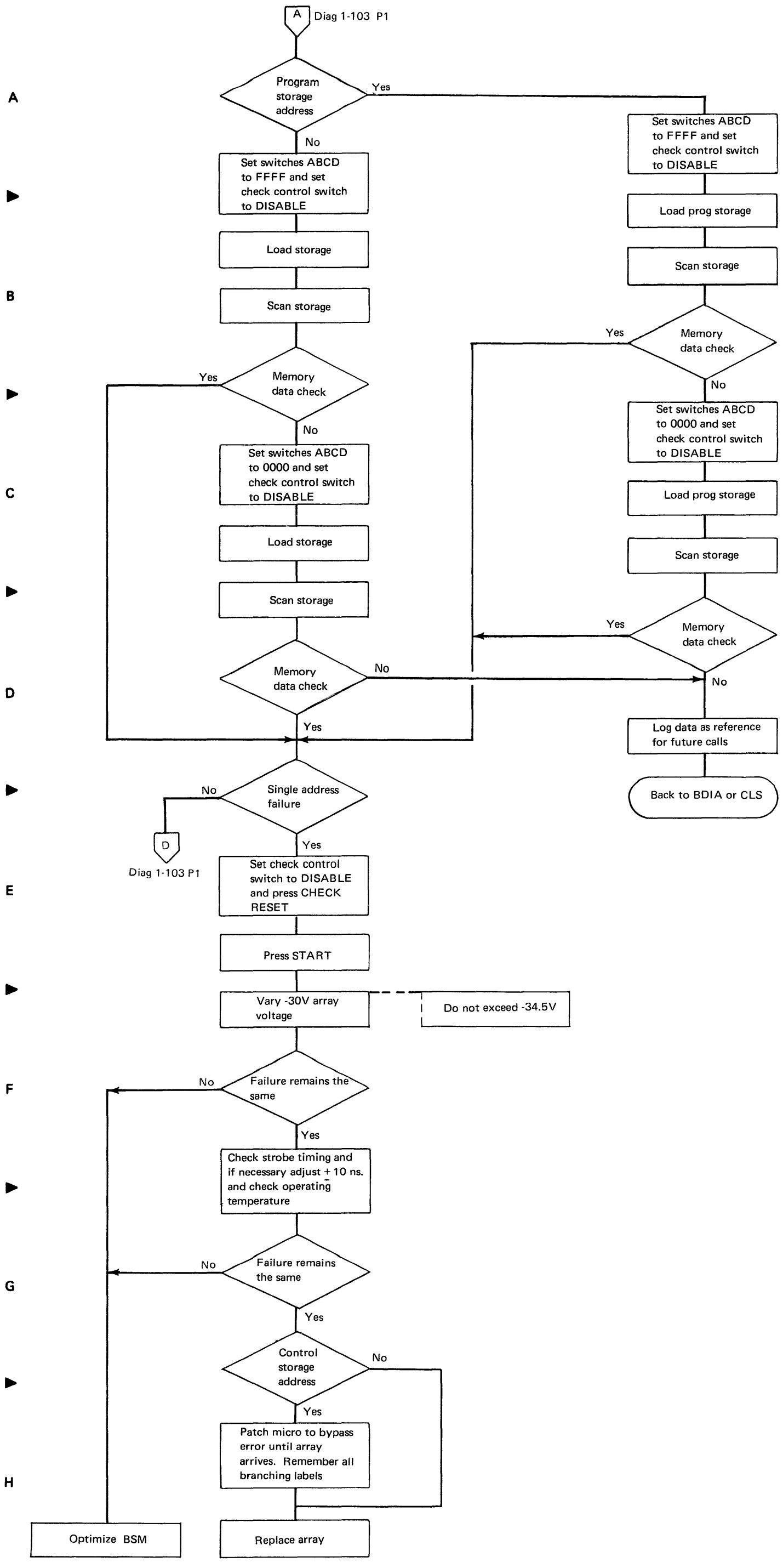
Notes:

(1) If P0 or P1 are being picked, set switches ABCD to 0101

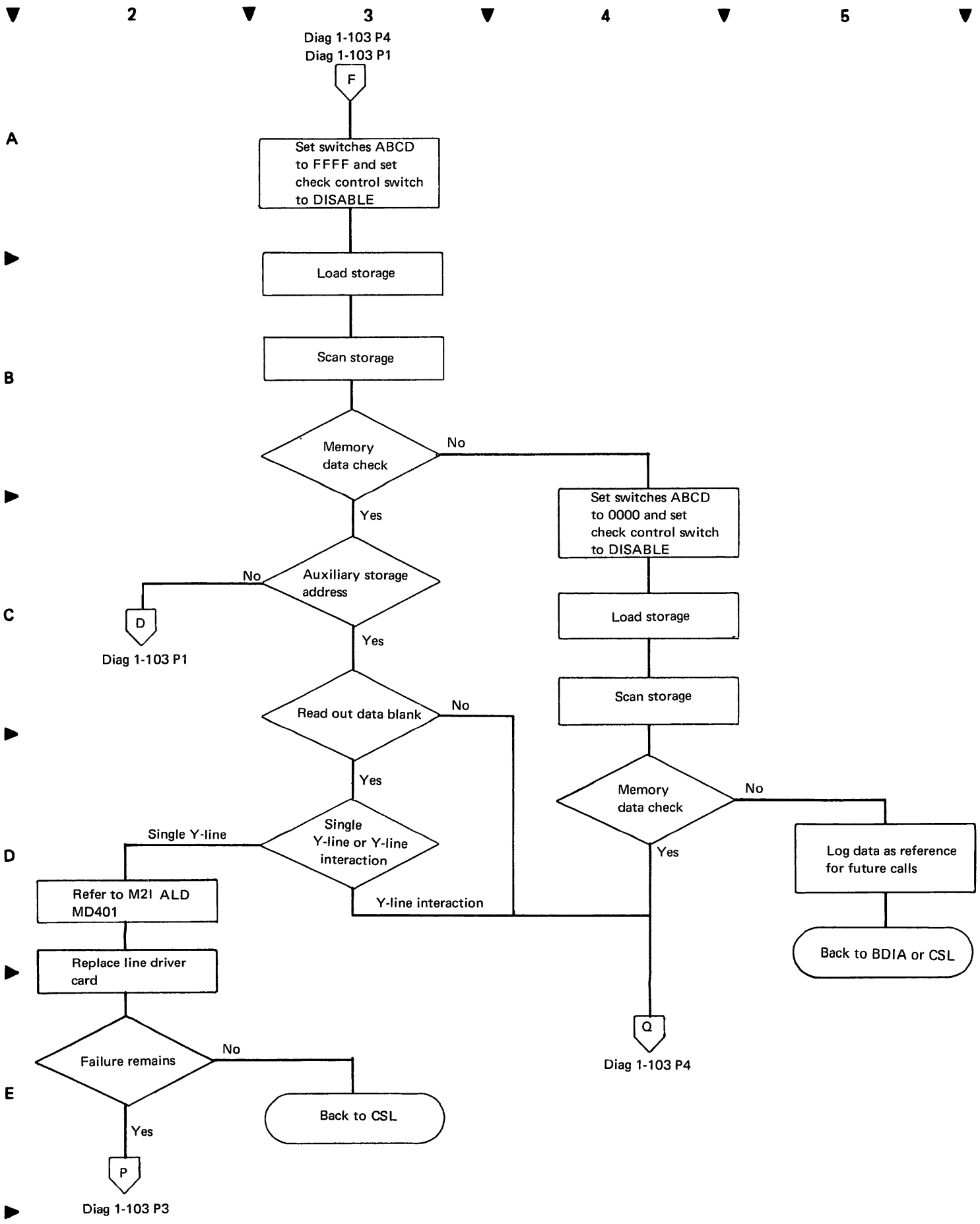
(2) Refer to Chapter 1 of 2025 FEMM for location of inhibit drivers for different bits failing

PICKING A SINGLE BIT

● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 8 of 10)



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 9 of 10)



● Diagram 1-103. Memory Diagnostic Technique Diagrams (Part 10 of 10)

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Power System Diagnostic Technique

A

▶

B

▶

C

▶

D

▶

E

▶

F

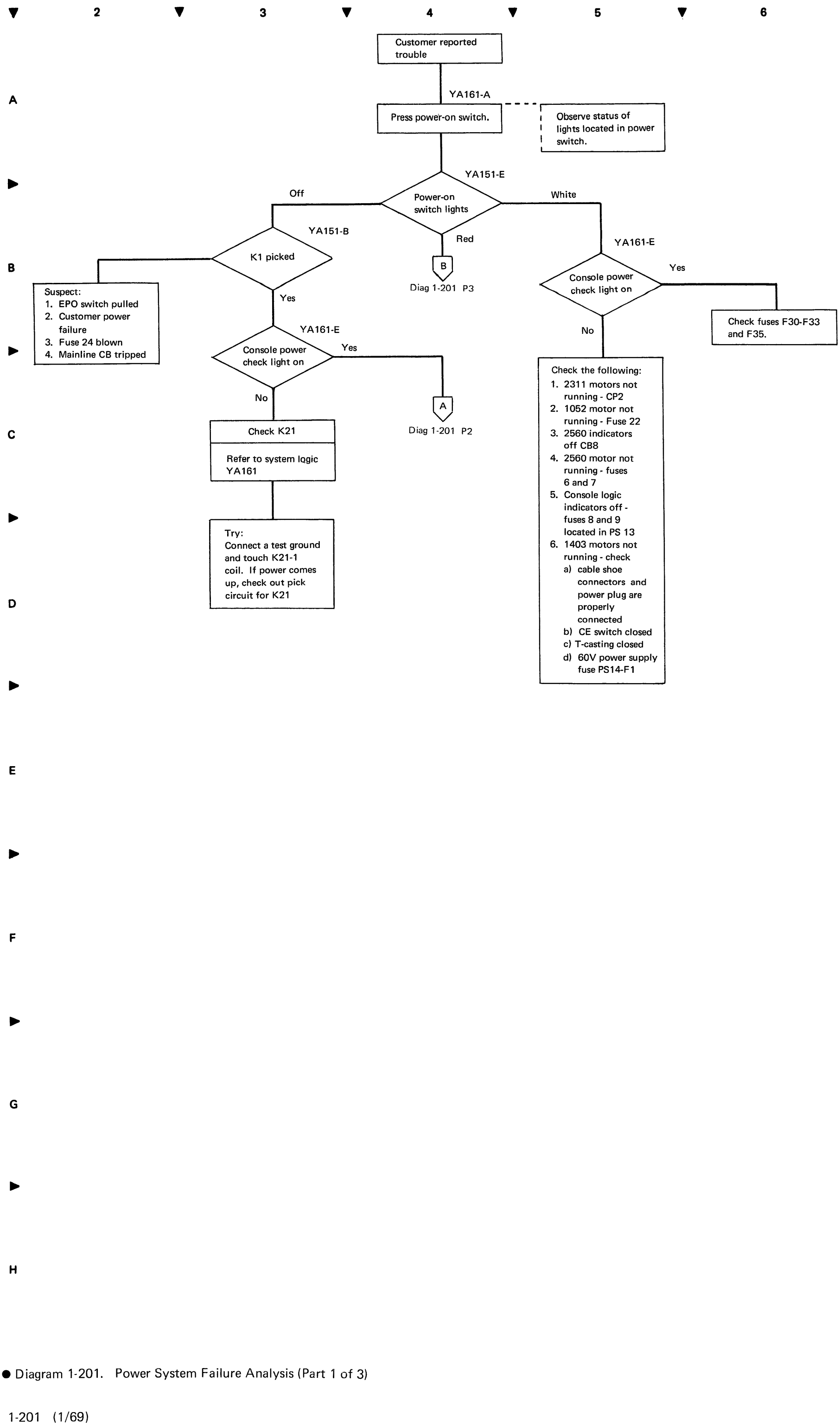
▶

G

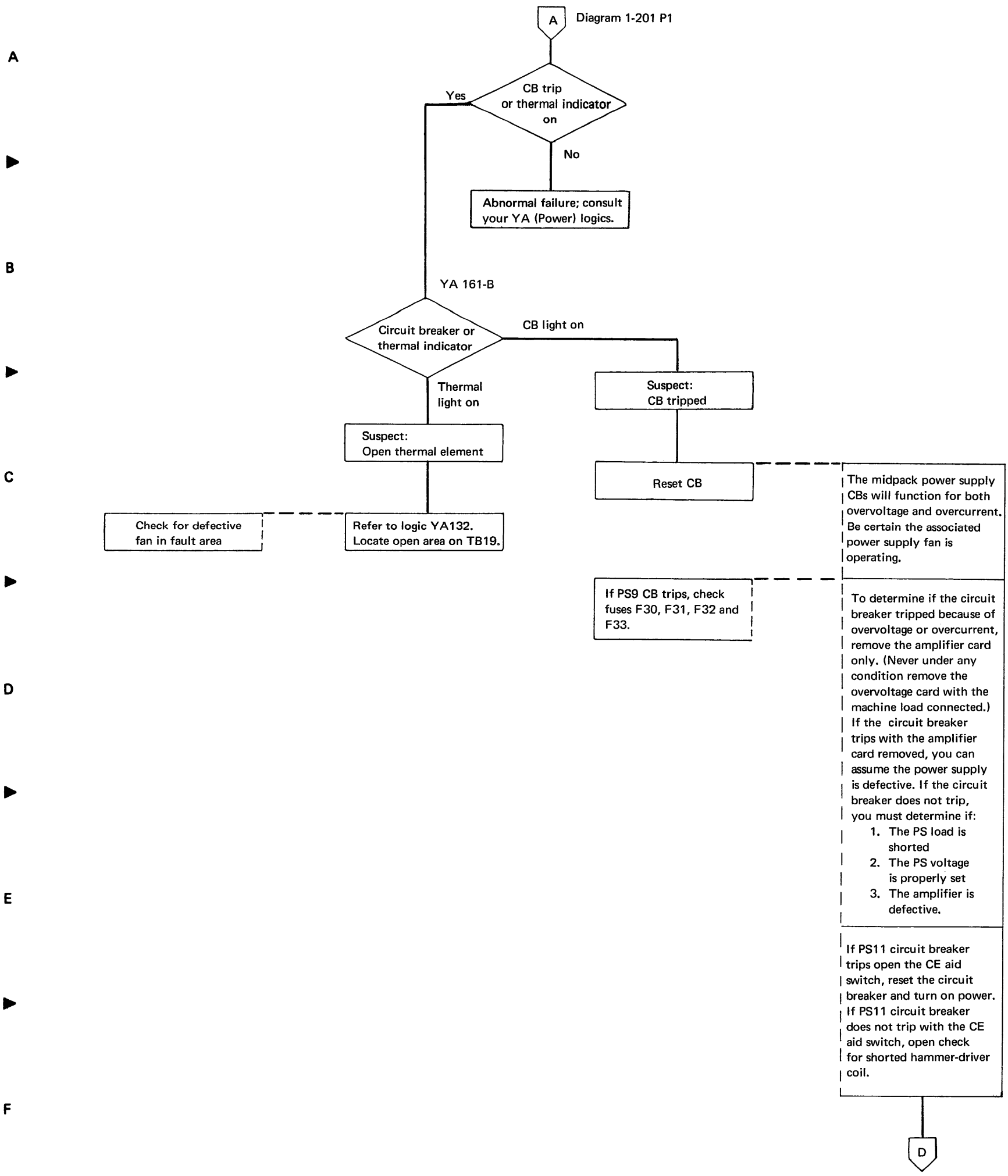
▶

H

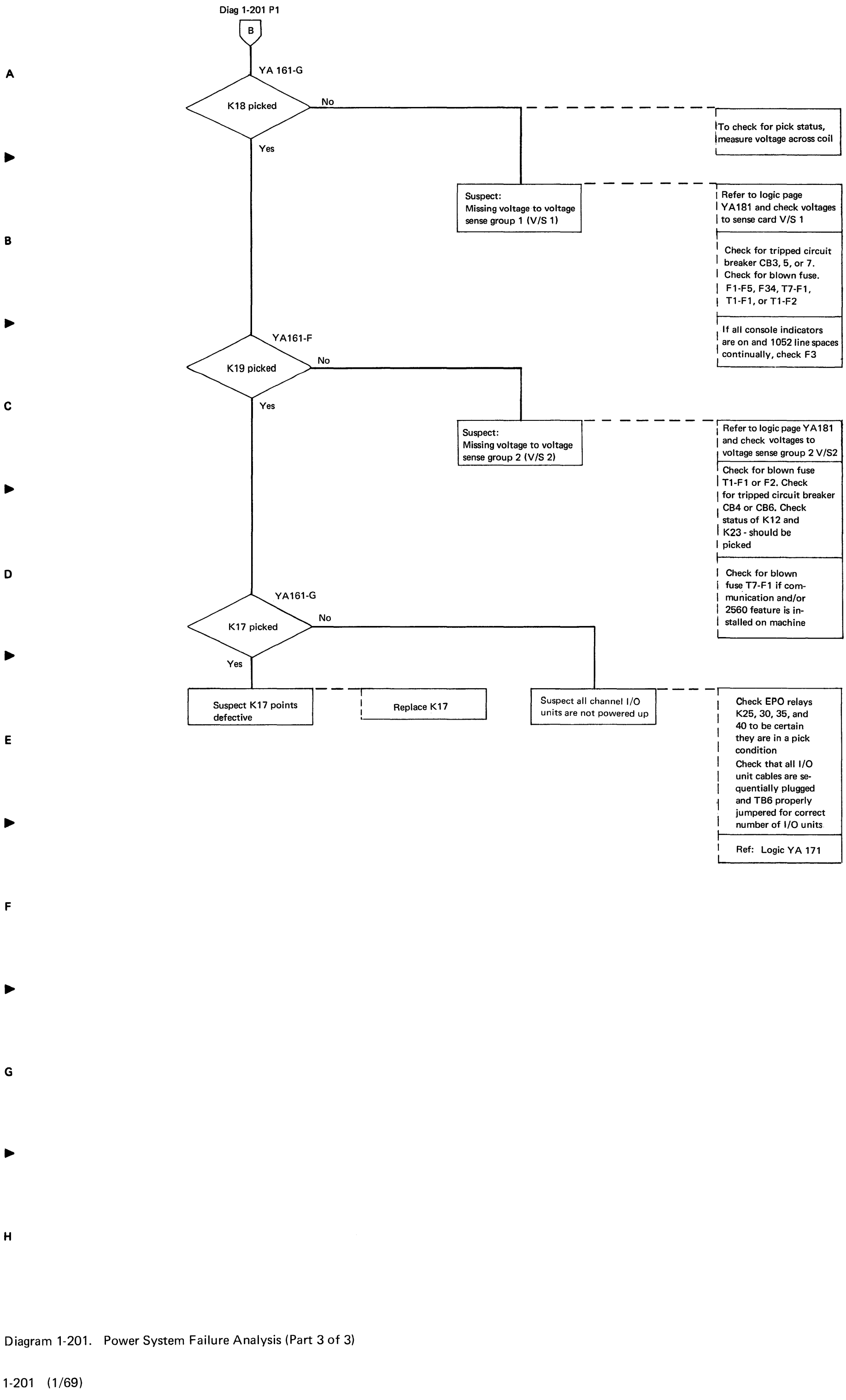
Diagram 1-200 Power System Diagnostic Technique



● Diagram 1-201. Power System Failure Analysis (Part 1 of 3)



● Diagram 1-201. Power System Failure Analysis (Part 2 of 3)



● Diagram 1-201. Power System Failure Analysis (Part 3 of 3)

2 3 4 5 6

A print check with print ready off can indicate a coil protect check. If the chain motor is not running, this is an indication of a coil protect check because this error would drop the +60V.

Caution
A bad hammer driver card that is always on may have been due to a shorted hammer coil. Swapping cards may result in damaging additional hammer driver cards. The problem causing position should be positively identified and checked for a shorted coil before full current printing is attempted.

Diagram 1-201 P2

D

This indicates that one or more hammer driver is on and cannot be reset. Two methods can be used to identify the error print positions:
1. Observe which positions printed on the form when the error was reset.
2. Open the current limit switch, open the T-casting, remove the paper and observe which hammers are protruding.

Error position indicated

Yes

Determine why the hammer driver is on. The problem can be due to a failure on the hammer driver card or due to an improper input signal to the hammer driver. With the current limit switch open, the output of the hammer driver will be at 0V if it is on. If it is not on, but another driver is on, the output will be at approximately +6V. If no drivers are on, the output will be at +40V. If the hammer driver latch is on, the test point will be at 0V. If the latch is off, the test point will be at approximately +6V.

No

No HD compare inputs should be on. No addressed HD reset should be on. HD reset should be at 0V to reset the HD. If power has just been turned on, or system reset given, the PLBAR is 00 so that the address lines on are X0 and Y0. If a print line has just been completed, the PLBAR is 132 so that the address lines on are X4 and Y16. No other address combination should be on

Printing occurs after the error is reset

Yes

This indicates a solid coil protect check. Operate the check reset key and try to print again

Error occurs immediately after reset

Yes

A print check with print ready off may indicate a coil protect check. Reset the error and print

No

Reset the print check, make the printer ready and try to print again

Print check

Yes

A

Diagram 1-300 P2

No

No additional errors occur. Problem is intermittent and may be due to a faulty current sense reed relay. The relay is occasionally failing to pick

No

Open the current limit switch to limit HD current and attempt to turn off the print check light on the printer with the check reset key

Check reset

No

It should not be possible to reset the print check because of one of two conditions
1. The current sense reed relay has failed and is always closed even though the current should be below the pick level due to the current limiting resistor.
2. One of the circuits in the coil protect check has failed keeping the check latch on erroneously

Yes

The coil in the error position is shorted and cannot operate the hammer. It will be necessary to identify the shorted position. Fuses F30 and F31 control the odd hammers and fuses F32 and F33 control the even hammers. Remove the fuses and observe which will allow +60V to remain on with the current limit switch in the normal (ON) position. See WP 221 and WP 222 for the HD positions controlled by each fuse

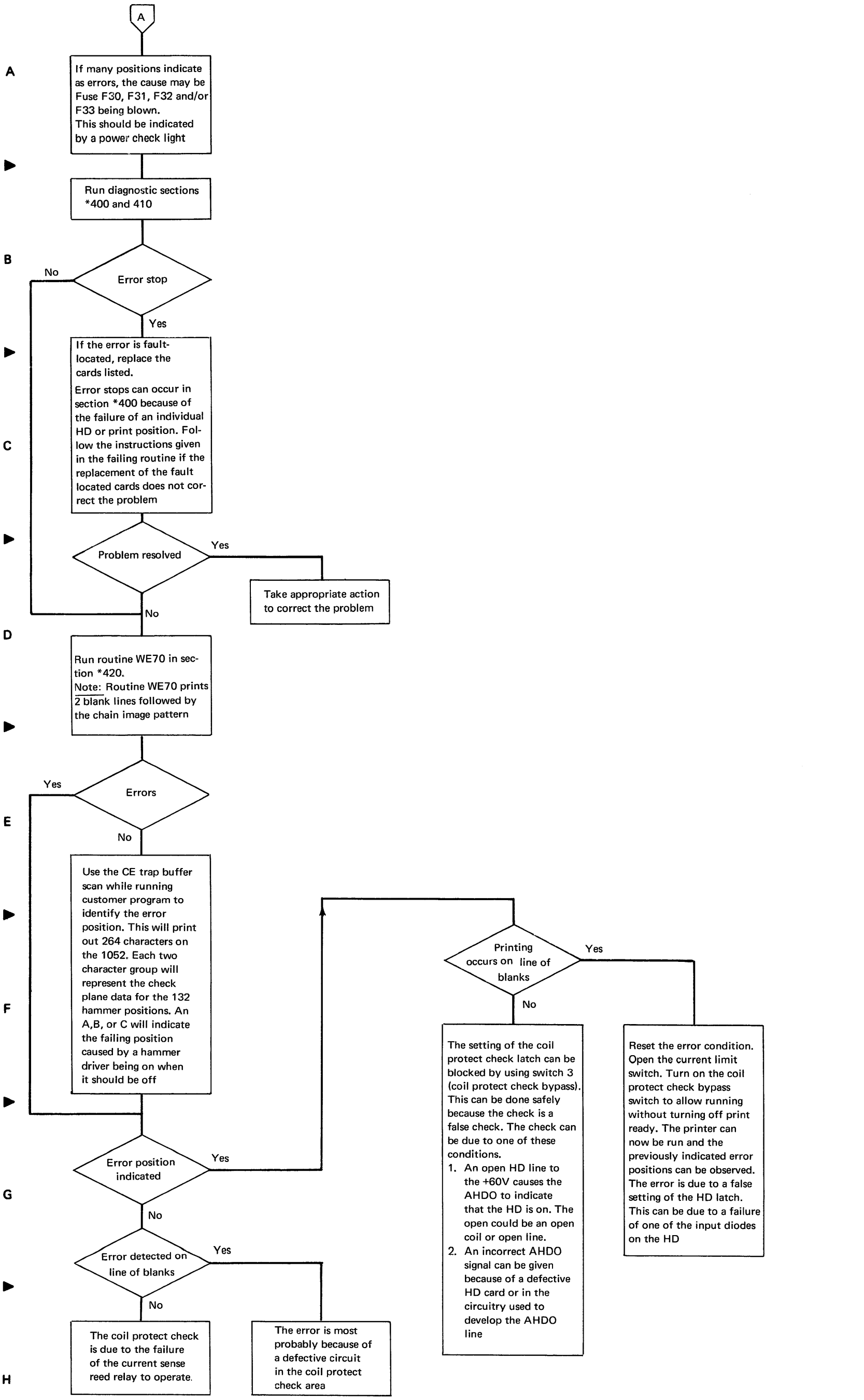
The HD cards for the indicated positions can now be removed. To determine the failing card remove cards only with power off. Once the failing card has been defined, the current limit switch can be opened, and the output of the HD observed to determine the bad circuit. The coil in the failing position must be checked and replaced if shorted, because the shorted coil can damage another HD the next time printing is attempted.

The alternate method of determining which is the shorted coil is by measuring the resistance from the output of the HD to the +60V return. A resistance of approximately 12 ohms is expected. A resistance of less than 10 ohms is probably a shorted coil

A B C D E F G H

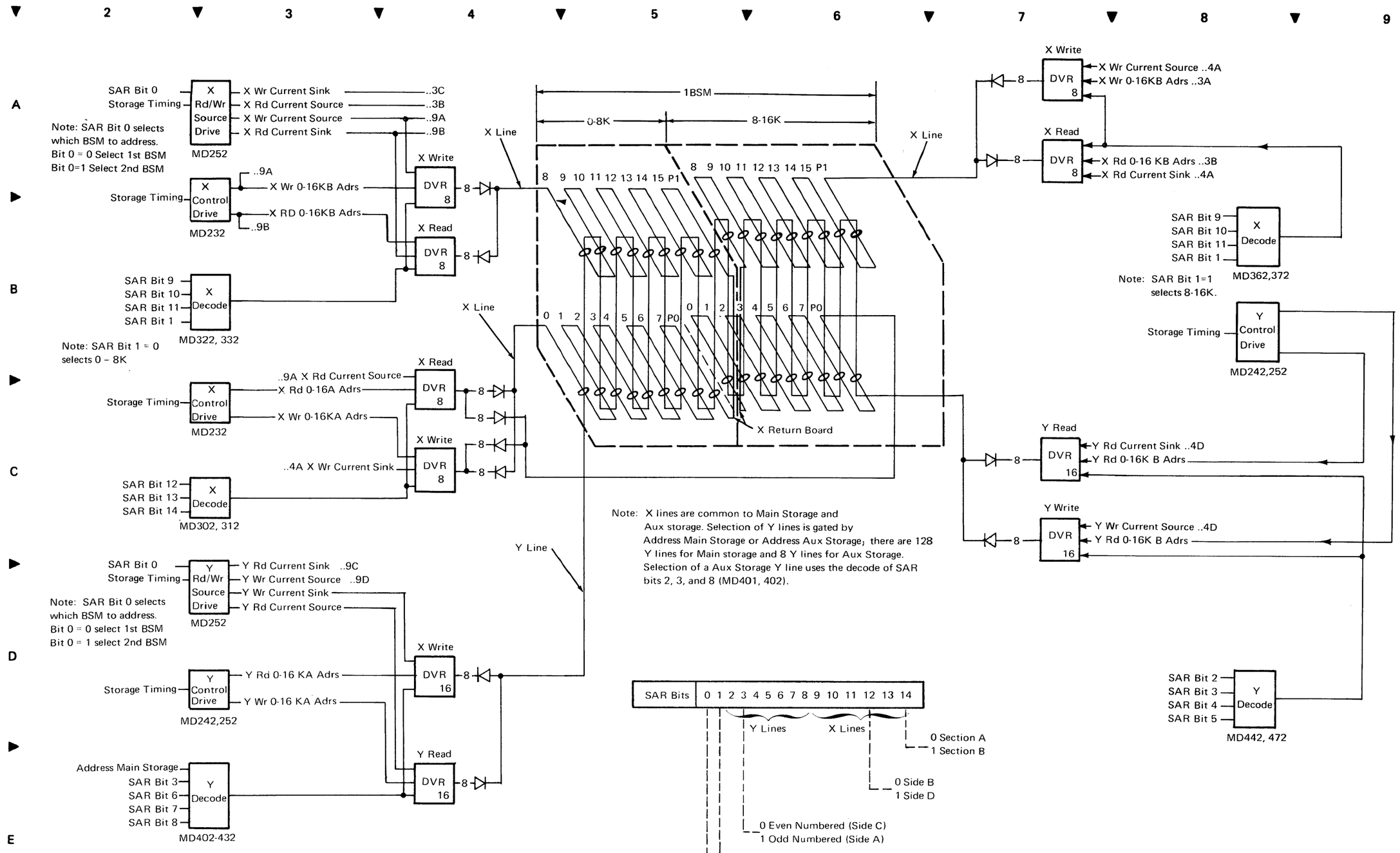
● Diagram 1-300. Coil Protect Diagnostic Technique (Part 1 of 2)

Diagram 1-300 P1



● Diagram 1-300. Coil Protect Diagnostic Technique (Part 2 of 2)

Diagram 4-26. Core Storage Driver



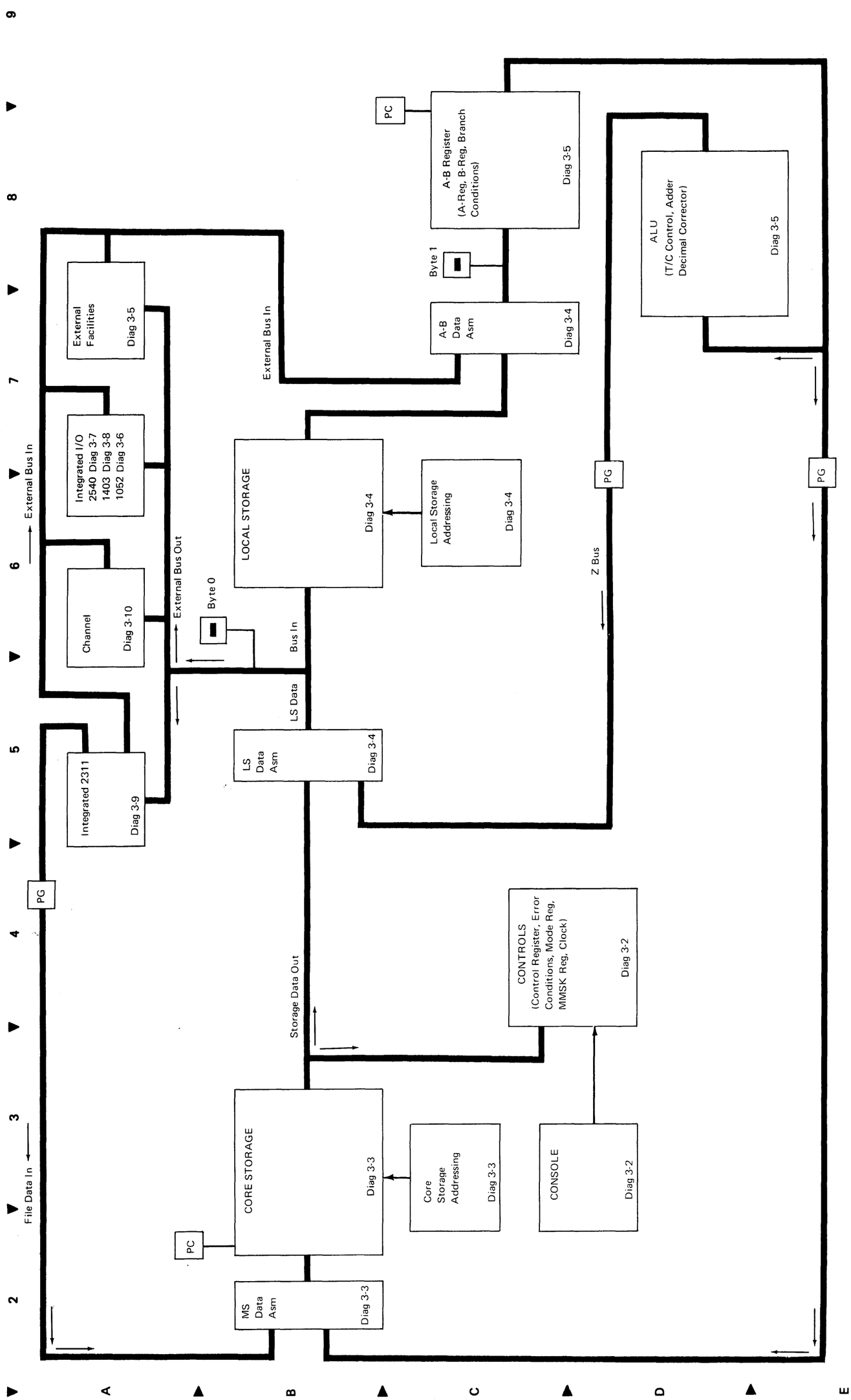
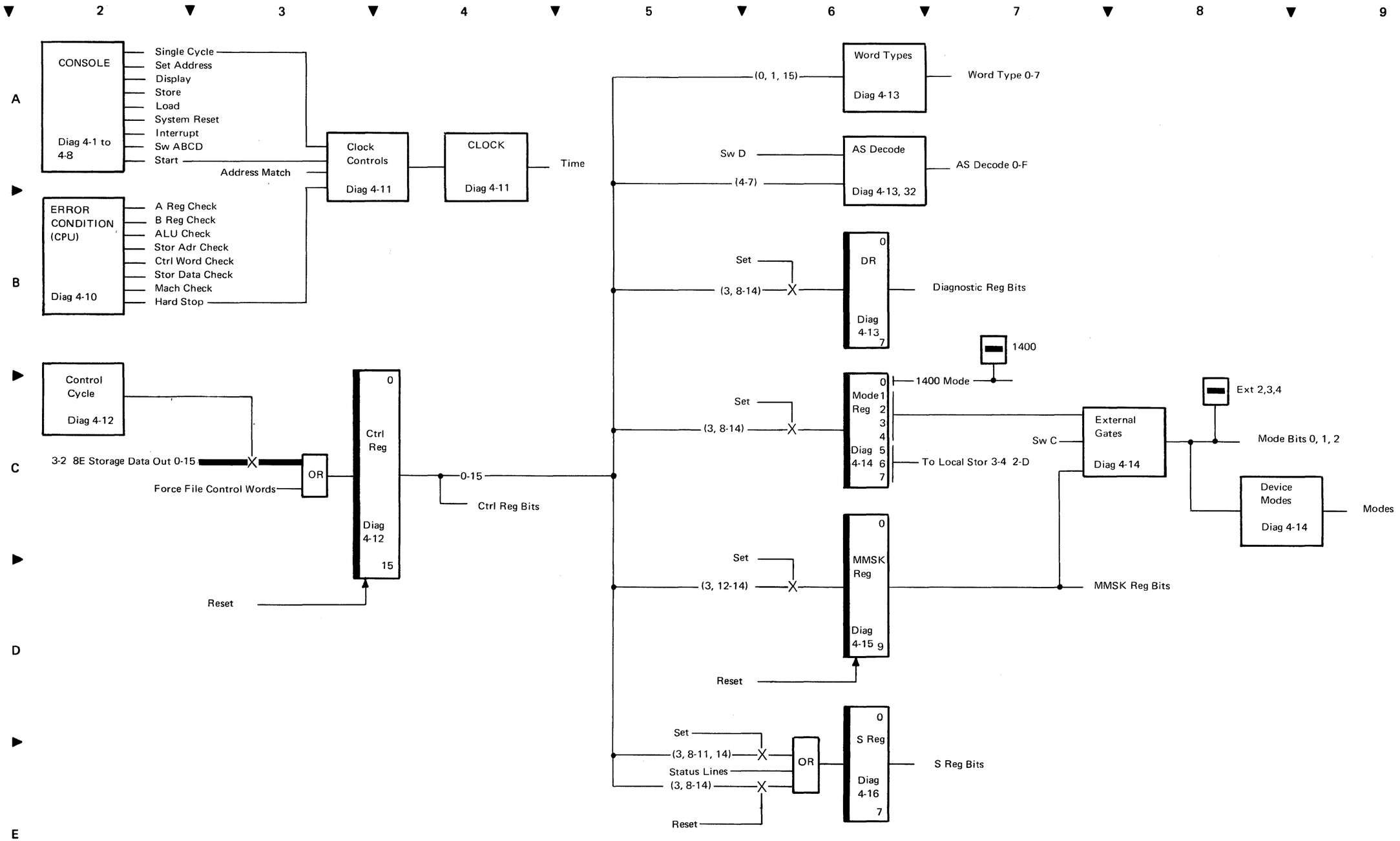


Diagram 3-1. 2025 System Data Flow

Diagram 3-2. Control Circuits Data Flow



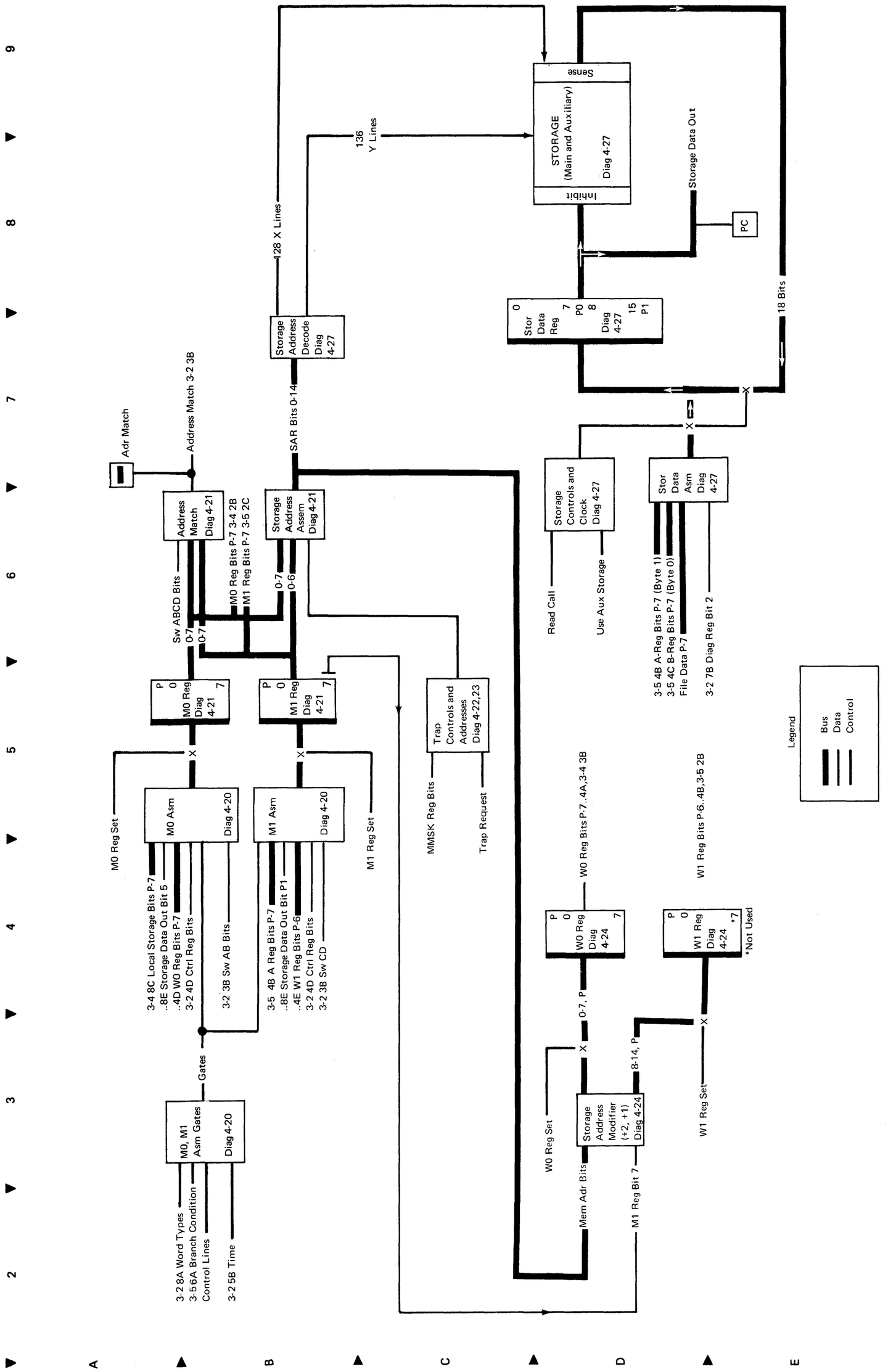
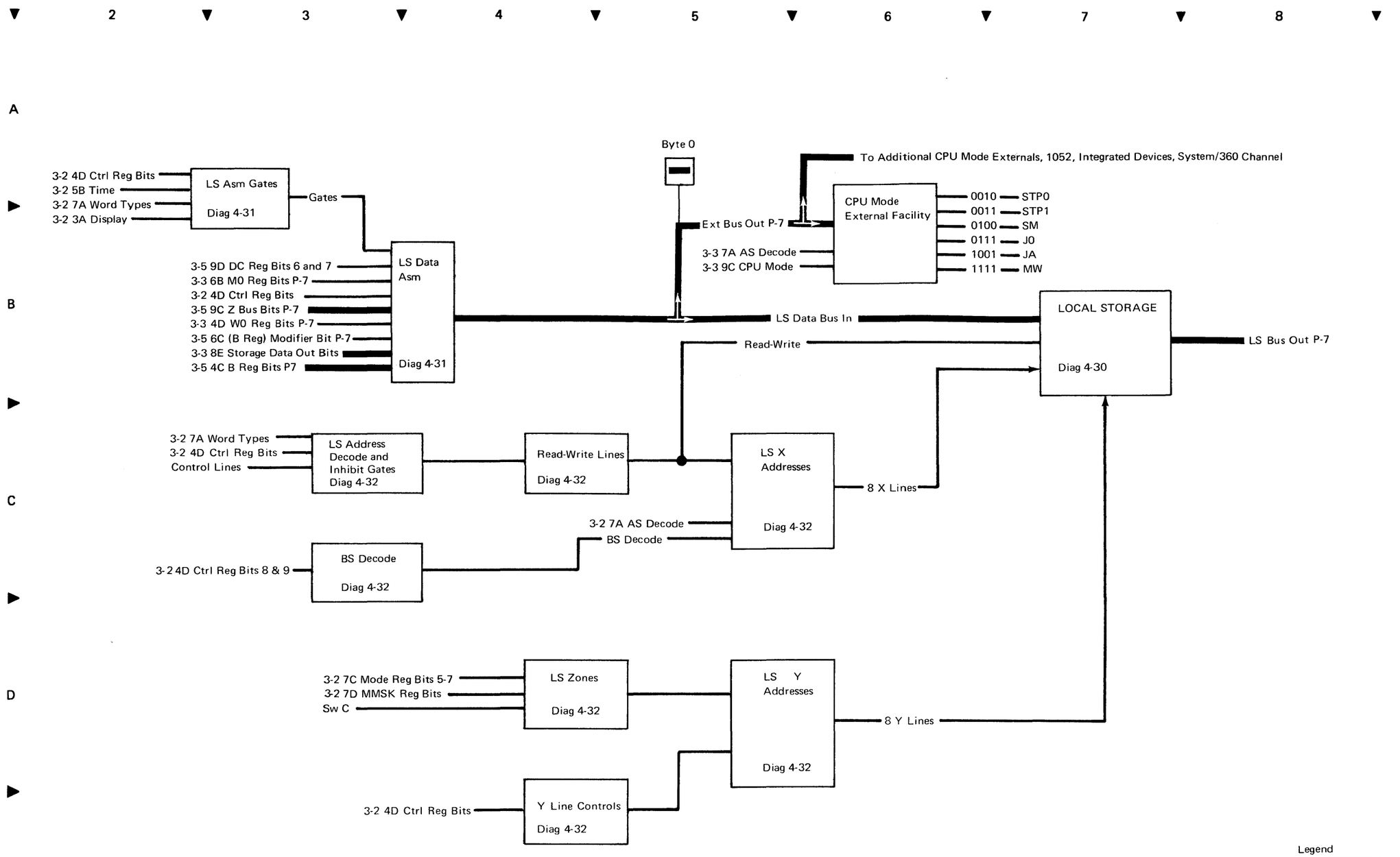


Diagram 3-3. Core Storage and Addressing Data Flow

Diagram 3-4. Local Storage Data Flow



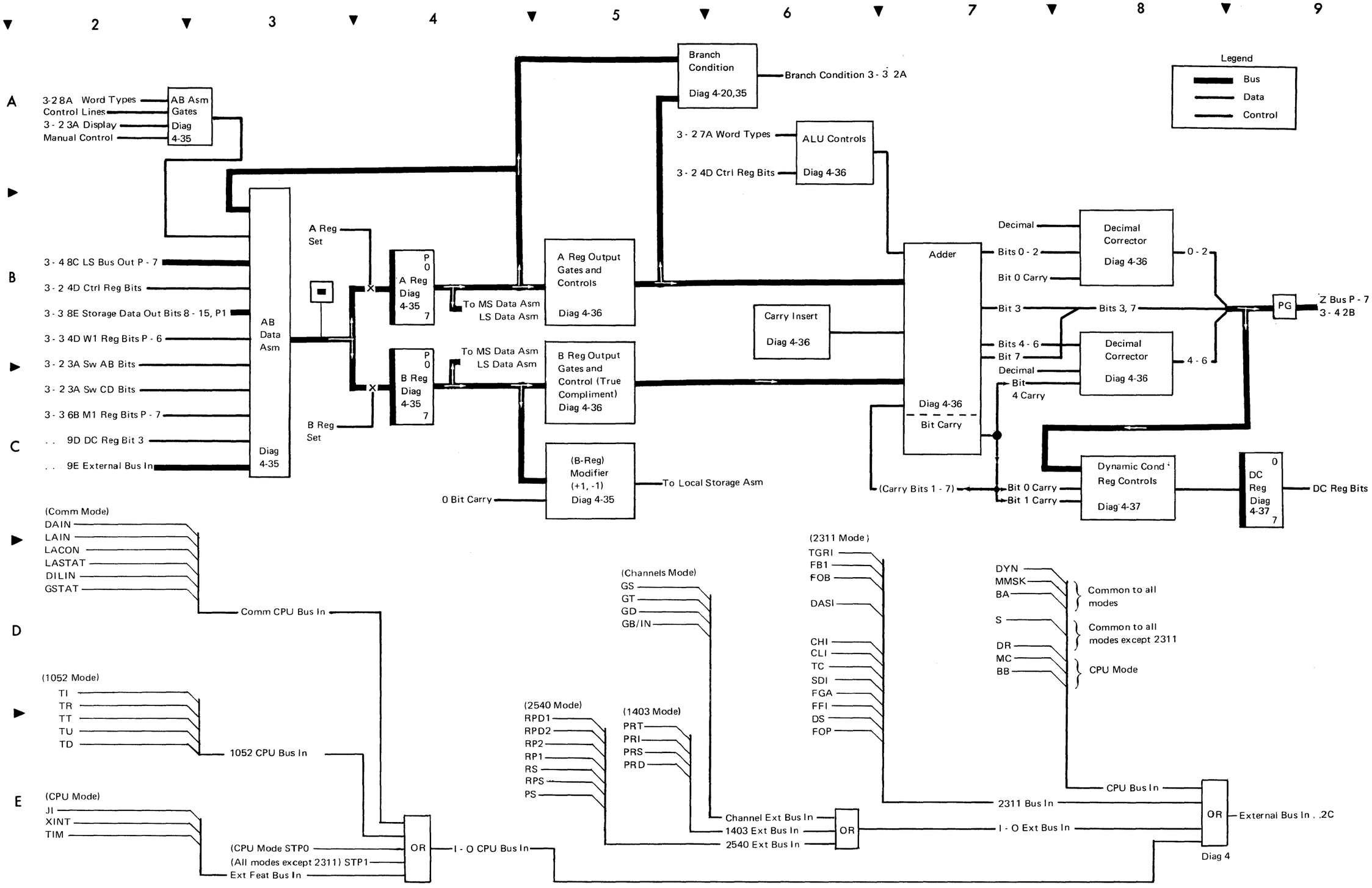
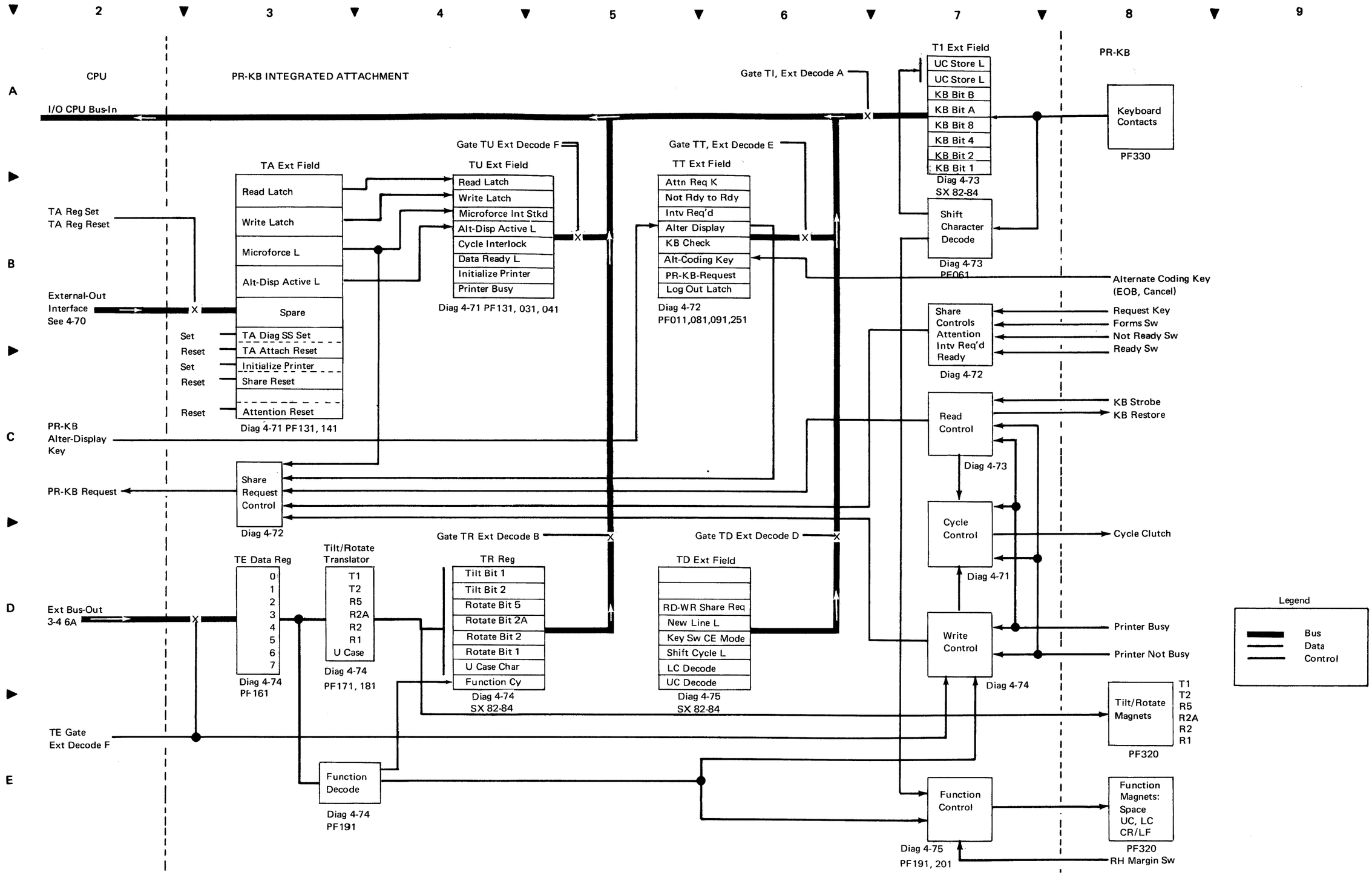

2
3
4
5
6
7
8
9
A
B
C
D
E
Legend
Bus
Data
Control
3-28A Word Types
Control Lines
3 - 2 3A Display
Manual Control
AB Asm Gates Diag 4-35
3 - 4 8C LS Bus Out P - 7
3 - 2 4D Ctrl Reg Bits
3 - 3 8E Storage Data Out Bits 8 - 15, P1
3 - 3 4D W1 Reg Bits P - 6
3 - 2 3A Sw AB Bits
3 - 2 3A Sw CD Bits
3 - 3 6B M1 Reg Bits P - 7
. . 9D DC Reg Bit 3
. . 9E External Bus In
AB Data Asm
Diag 4-35
A Reg Set
B Reg Set
P 0 A Reg Diag 4-35 7
P 0 B Reg Diag 4-35 7
To MS Data Asm LS Data Asm
To MS Data Asm LS Data Asm
A Reg Output Gates and Controls Diag 4-36
B Reg Output Gates and Control (True Compliment) Diag 4-36
(B-Reg) Modifier (+1, -1) Diag 4-35
0 Bit Carry
To Local Storage Asm
Branch Condition Diag 4-20,35
Branch Condition 3 - 3 2A
3 - 2 7A Word Types
3 - 2 4D Ctrl Reg Bits
ALU Controls Diag 4-36
Carry Insert Diag 4-36
Adder
Diag 4-36
Bit Carry
(Carry Bits 1 - 7)
Decimal
Bits 0 - 2
Bit 0 Carry
Bit 3
Bits 4 - 6
Bit 7
Decimal
Bit 4 Carry
Decimal Corrector Diag 4-36
Decimal Corrector Diag 4-36
Bits 3, 7
0 - 2
4 - 6
PG
Z Bus P - 7
3 - 4 2B
Bit 0 Carry
Bit 1 Carry
Dynamic Cond Reg Controls Diag 4-37
0 DC Reg Diag 4-37 7
DC Reg Bits
(Comm Mode)
DAIN
LAIN
LACON
LASTAT
DILIN
GSTAT
Comm CPU Bus In
(1052 Mode)
TI
TR
TT
TU
TD
1052 CPU Bus In
(CPU Mode)
JI
XINT
TIM
(CPU Mode STP0
(All modes except 2311) STP1
Ext Feat Bus In
OR
I - O CPU Bus In
(Channels Mode)
GS
GT
GD
GB/IN
(2540 Mode)
RPD1
RPD2
RP2
RP1
RS
RPS
PS
(1403 Mode)
PRT
PRI
PRS
PRD
Channel Ext Bus In
1403 Ext Bus In
2540 Ext Bus In
OR
(2311 Mode)
TGRI
FB1
FOB
DASI
CHI
CLI
TC
SDI
FGA
FFI
DS
FOP
2311 Bus In
I - O Ext Bus In
DYN
MMSK
BA
Common to all modes
S
Common to all modes except 2311
DR
MC
BB
CPU Mode
CPU Bus In
OR
External Bus In . .2C
Diag 4

Diagram 3-6. Console Printer-Keyboard Data Flow



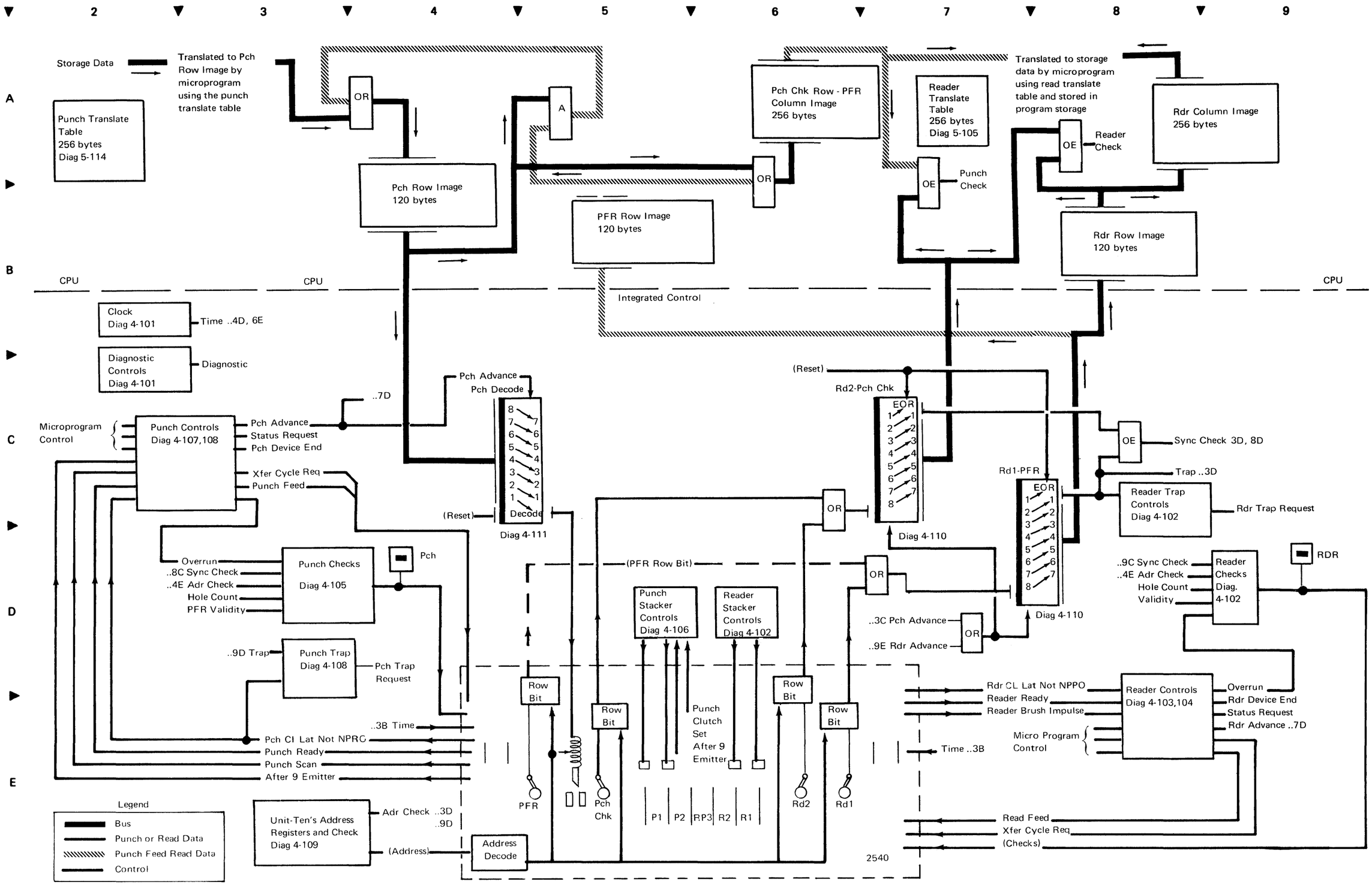

2
3
4
5
6
7
8
9
A
B
C
D
E
Storage Data
Translated to Pch Row Image by microprogram using the punch translate table
Punch Translate Table 256 bytes Diag 5-114
OR
A
Pch Row Image 120 bytes
Pch Chk Row - PFR Column Image 256 bytes
Reader Translate Table 256 bytes Diag 5-105
Translated to storage data by microprogram using read translate table and stored in program storage
Rdr Column Image 256 bytes
OE
Reader Check
OR
OE
Punch Check
PFR Row Image 120 bytes
Rdr Row Image 120 bytes
CPU
CPU
CPU
Integrated Control
Clock Diag 4-101
Time ..4D, 6E
Diagnostic Controls Diag 4-101
Diagnostic
..7D
Pch Advance
Pch Decode
(Reset)
Decode
Diag 4-111
(Reset)
Rd2-Pch Chk
EOR
Diag 4-110
OR
OE
Sync Check 3D, 8D
Trap ..3D
Rd1-PFR
EOR
Diag 4-110
Reader Trap Controls Diag 4-102
Rdr Trap Request
Microprogram Control
Punch Controls Diag 4-107,108
Pch Advance
Status Request
Pch Device End
Xfer Cycle Req
Punch Feed
Overrun
..8C Sync Check
..4E Adr Check
Hole Count
PFR Validity
Punch Checks Diag 4-105
Pch
(PFR Row Bit)
OR
..9C Sync Check
..4E Adr Check
Hole Count
Validity
Reader Checks Diag. 4-102
RDR
Punch Stacker Controls Diag 4-106
Reader Stacker Controls Diag 4-102
..3C Pch Advance
..9E Rdr Advance
OR
..9D Trap
Punch Trap Diag 4-108
Pch Trap Request
Row Bit
Row Bit
Row Bit
Row Bit
Punch Clutch Set After 9 Emitter
..3B Time
Pch Cl Lat Not NPRO
Punch Ready
Punch Scan
After 9 Emitter
Rdr CL Lat Not NPPO
Reader Ready
Reader Brush Impulse
Time ..3B
Micro Program Control
Reader Controls Diag 4-103,104
Overrun
Rdr Device End
Status Request
Rdr Advance ..7D
PFR
Pch Chk
P1
P2
RP3
R2
R1
Rd2
Rd1
Read Feed
Xfer Cycle Req
(Checks)
2540
Unit-Ten's Address Registers and Check Diag 4-109
Adr Check ..3D ..9D
(Address)
Address Decode
Legend
Bus
Punch or Read Data
Punch Feed Read Data
Control

Diagram 3-8. Printer Data Flow

2 3 4 5 6 7 8 9

A

Hammers
1
Drum
AMP
1403
Stop Brushes
Slow Brushes
E1
AMP
A Set
A Reset
A Set
A Reset
Slow Brush Latches 4-212 1 12
Stop Brush Latches 4-212 1 2 4 8
Carr Brush Reg 4-212 1 2 4 8
Slow Speed Compare 4-212
Slow Speed Latch 4-212
Skip Compare 4-212
Carriage Drive Reset 4-2
PSS Gate 4-204
SS Ring 4-204
Adv +1
MCS Advance
Adv +2
Adv +8
OR 4-205

B

Print Scan
A
Clock 4-203
A
Clock Control
PCC Reset 4-206
PCC Count 1 2 4 8 16 4-205 32 64 128
Compare 4-209
HD Matrix 4-210
1
Carriage Control Reg Set
X
Carr Ctrl Reg 4-212 1 2 4 8
Chan 9 and 12 Latches 4-212

C

Ext Bus Out (From CPU)
PLB Bus Out Sample
X
Time Write
Inhibit 4-208 1 2 4 8 16 32 64 128 P PLC C1 C2 C3
Print Line Buffer 4-208 1 2 4 8 16 32 64 128 P PLC C1 C2 C3
SA 4-208
Strobe
X
PLB Data Reg 4-208 1 2 4 8 16 32 64 128 P PLC C1 C2 C3
PC
A
Carriage Go
Space 1 XX
Space 2 SS
Space 3 SS
Space Latch 4-213
Carriage Drive 4-213

D

Hammer Check 4-211
Gate 1403 PRS External
X
PLB Bus In Sample
X
Legend
Bus
Data
Control

PLBAR Bus Out Sample
X
PLBAR 1 2 4 8 16 32 64 128 4-207
PLBAR Bus In Sample
X
Ext Bus In (To CPU)

E

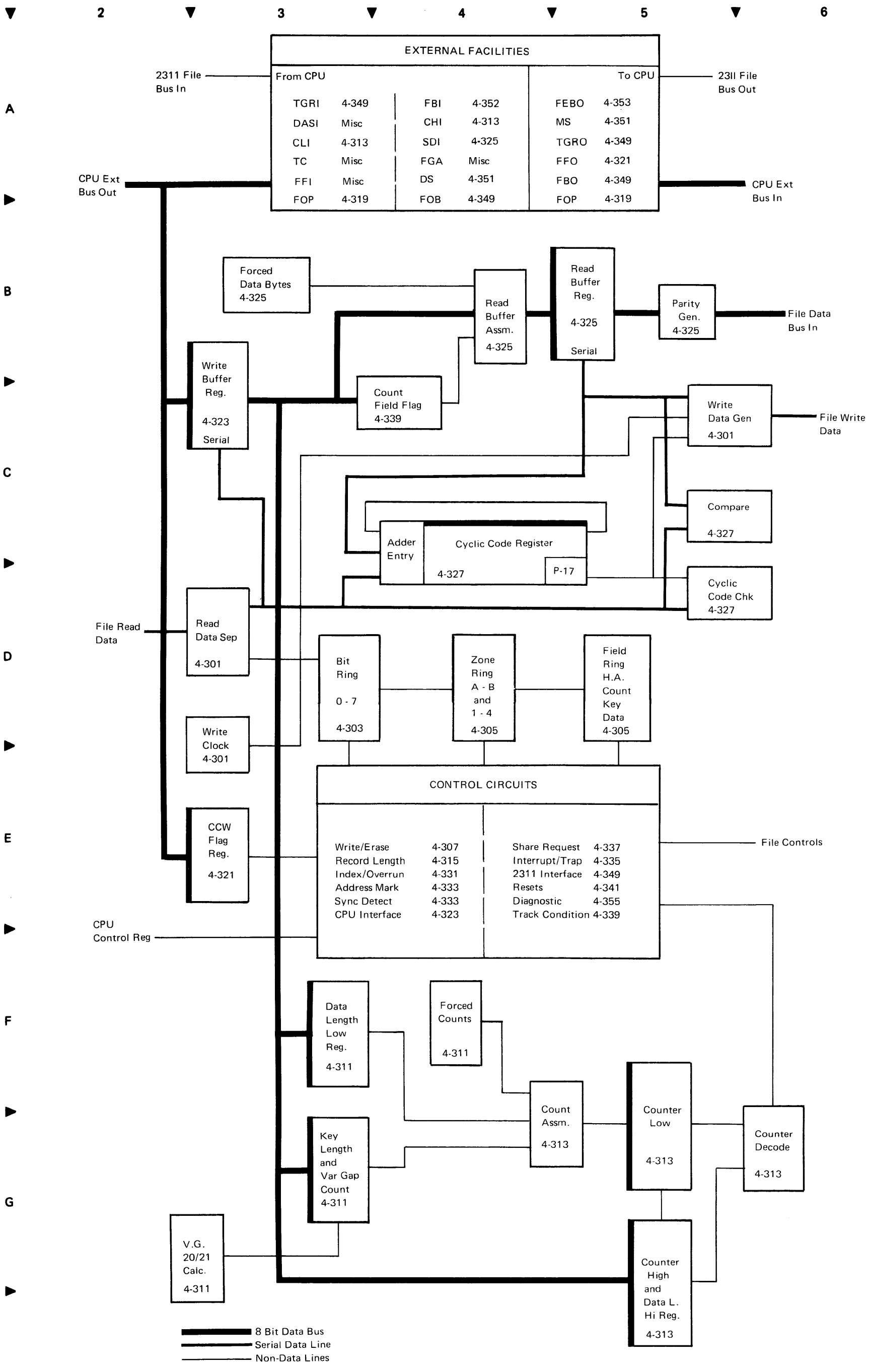
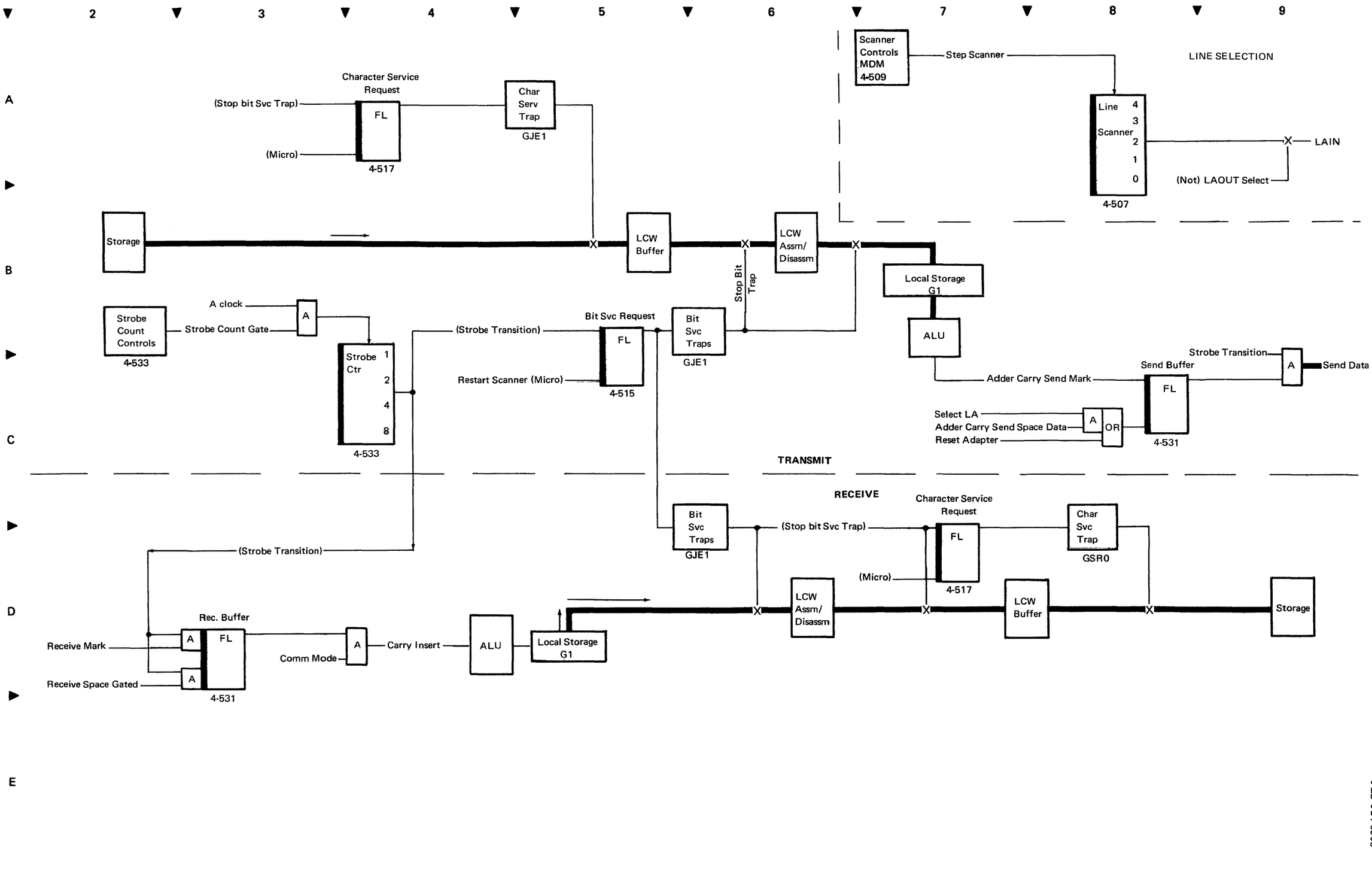
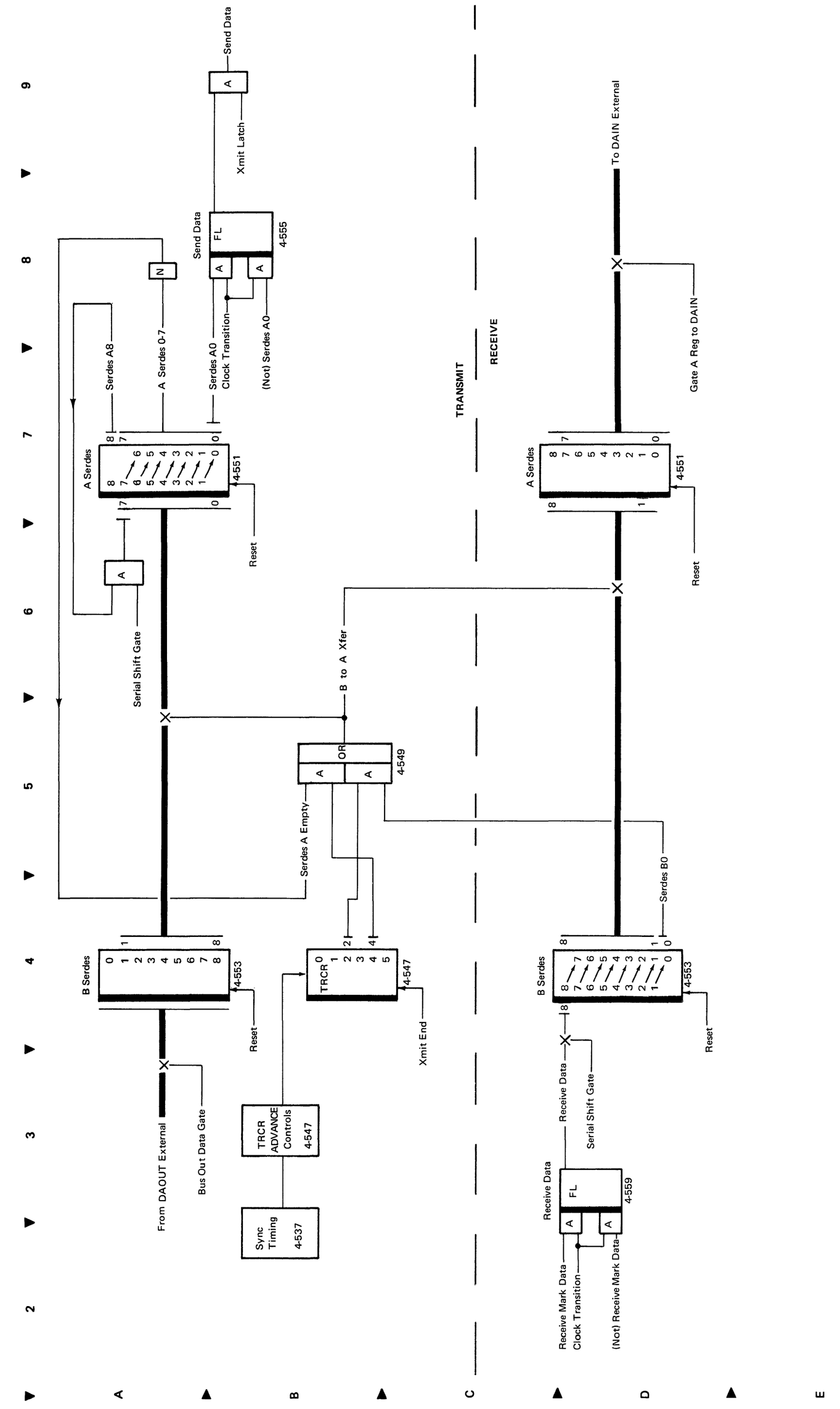


Diagram 3-9. File Control Data Flow

Diagram 3-10. Gating of External Facilities in Channel Operation



Form Y24-3529-0
FES Y24-0506



● Diagram 3-12. Communications Synchronous Data Flow

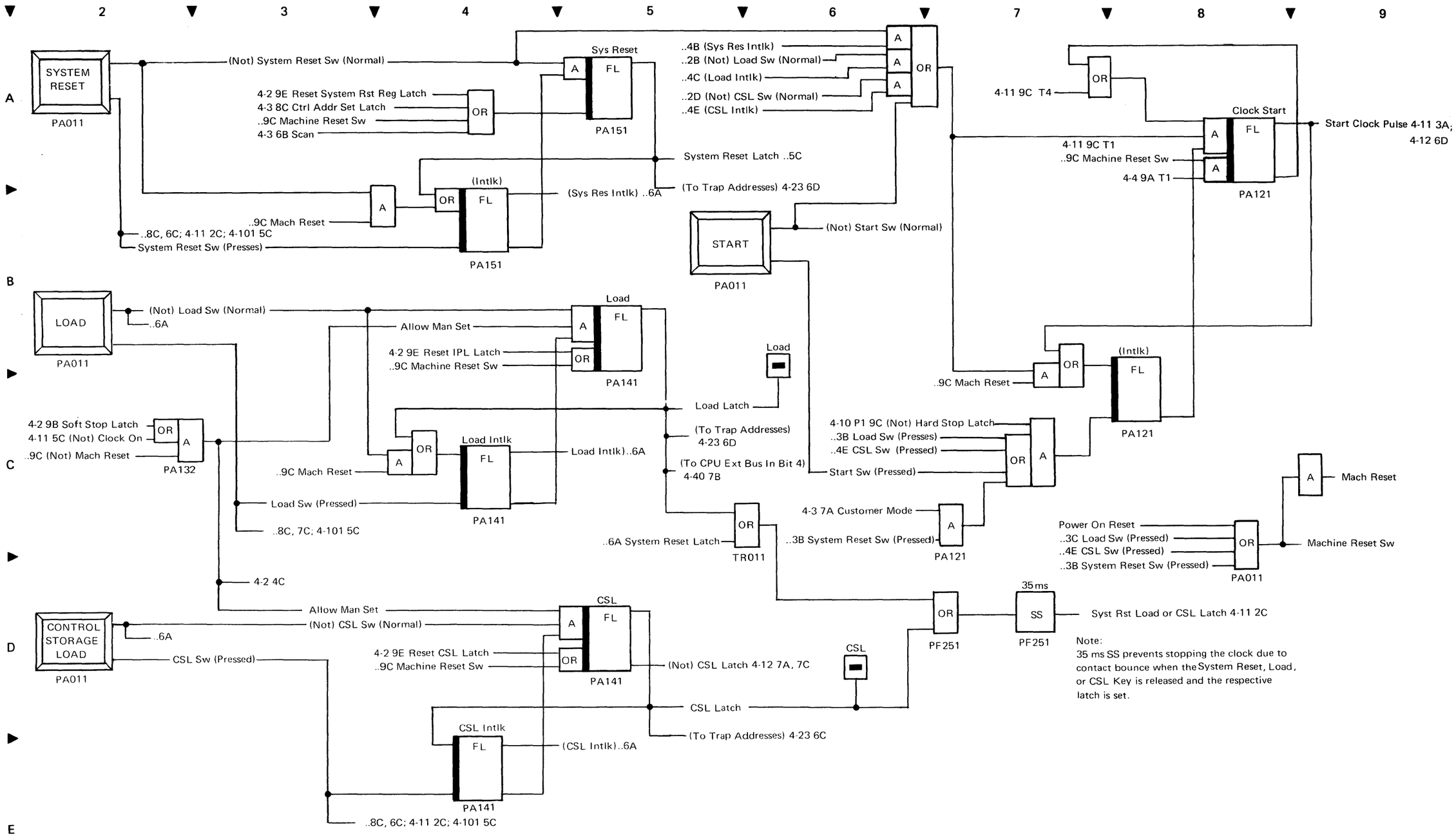
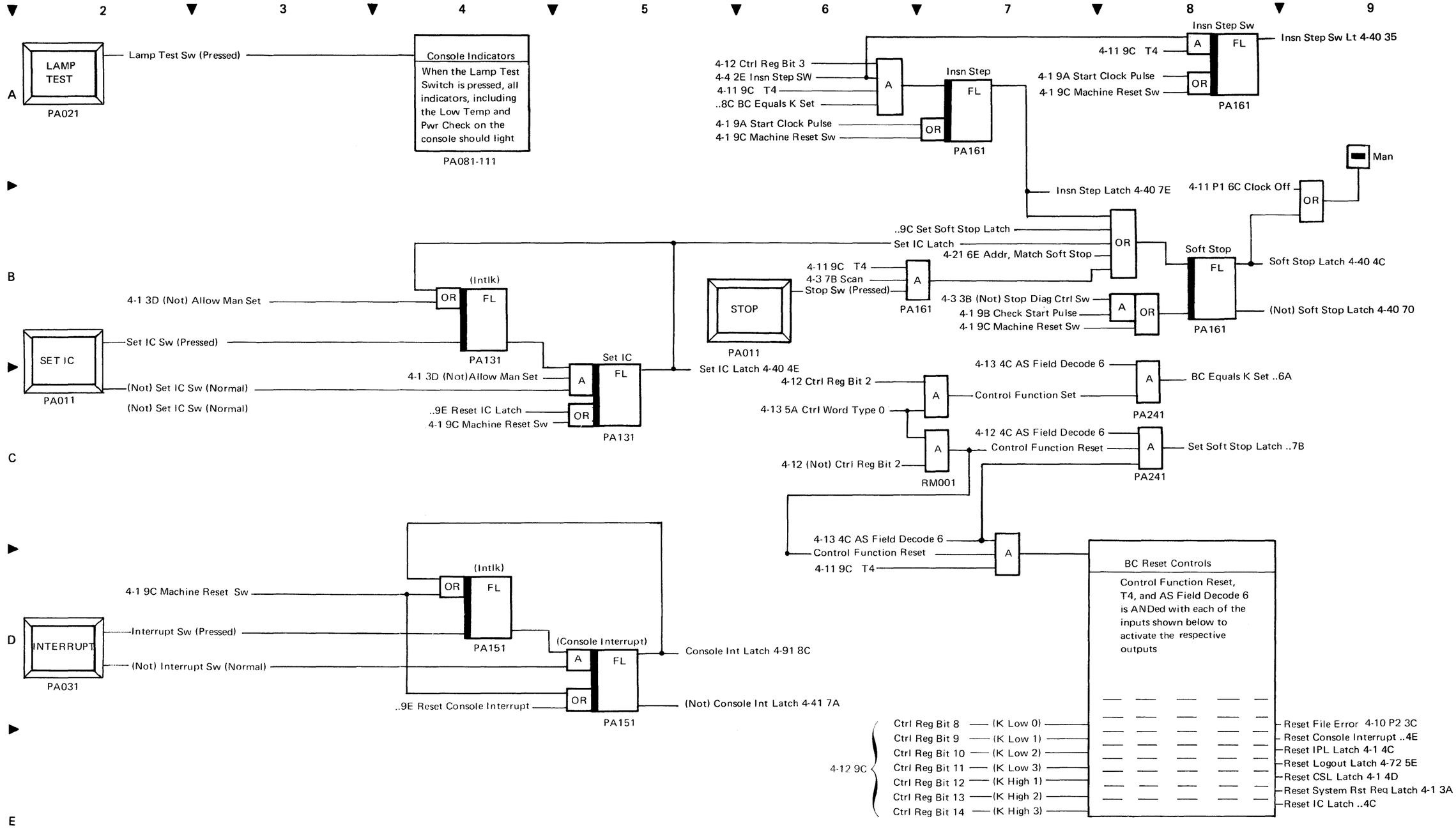

2
3
4
5
6
7
8
9
A
B
C
D
E
SYSTEM RESET
PA011
(Not) System Reset Sw (Normal)
4-2 9E Reset System Rst Reg Latch
4-3 8C Ctrl Addr Set Latch
..9C Machine Reset Sw
4-3 6B Scan
OR
Sys Reset
A
FL
PA151
..4B (Sys Res Intlk)
..2B (Not) Load Sw (Normal)
..4C (Load Intlk)
..2D (Not) CSL Sw (Normal)
..4E (CSL Intlk)
A
A
A
OR
4-11 9C T4
OR
Clock Start
A
FL
Start Clock Pulse 4-11 3A; 4-12 6D
4-11 9C T1
..9C Machine Reset Sw
4-4 9A T1
A
PA121
System Reset Latch ..5C
(To Trap Addresses) 4-23 6D
(Intlk)
OR
FL
(Sys Res Intlk) ..6A
A
..9C Mach Reset
..8C, 6C; 4-11 2C; 4-101 5C
System Reset Sw (Presses)
PA151
START
PA011
(Not) Start Sw (Normal)
LOAD
PA011
(Not) Load Sw (Normal)
..6A
Load
A
FL
Allow Man Set
4-2 9E Reset IPL Latch
..9C Machine Reset Sw
OR
PA141
Load
Load Latch
(To Trap Addresses) 4-23 6D
(To CPU Ext Bus In Bit 4) 4-40 7B
..9C Mach Reset
A
OR
(Intlk)
FL
PA121
4-2 9B Soft Stop Latch
4-11 5C (Not) Clock On
..9C (Not) Mach Reset
OR
A
PA132
..9C Mach Reset
A
OR
Load Intlk
FL
Load Intlk)..6A
Load Sw (Pressed)
..8C, 7C; 4-101 5C
PA141
4-10 P1 9C (Not) Hard Stop Latch
..3B Load Sw (Presses)
..4E CSL Sw (Pressed)
Start Sw (Pressed)
OR
A
4-3 7A Customer Mode
..3B System Reset Sw (Pressed)
A
PA121
..6A System Reset Latch
OR
TR011
A
Mach Reset
Power On Reset
..3C Load Sw (Pressed)
..4E CSL Sw (Pressed)
..3B System Reset Sw (Pressed)
OR
PA011
Machine Reset Sw
4-2 4C
Allow Man Set
CONTROL STORAGE LOAD
PA011
(Not) CSL Sw (Normal)
..6A
CSL Sw (Pressed)
CSL
A
FL
4-2 9E Reset CSL Latch
..9C Machine Reset Sw
OR
PA141
(Not) CSL Latch 4-12 7A, 7C
CSL
CSL Latch
(To Trap Addresses) 4-23 6C
CSL Intlk
FL
(CSL Intlk)..6A
PA141
..8C, 6C; 4-11 2C; 4-101 5C
OR
PF251
35 ms
SS
PF251
Syst Rst Load or CSL Latch 4-11 2C
Note:
35 ms SS prevents stopping the clock due to contact bounce when the System Reset, Load, or CSL Key is released and the respective latch is set.

Diagram 4-2. Manual Switches Lamp Test, Set IC, Interrupt, Stop



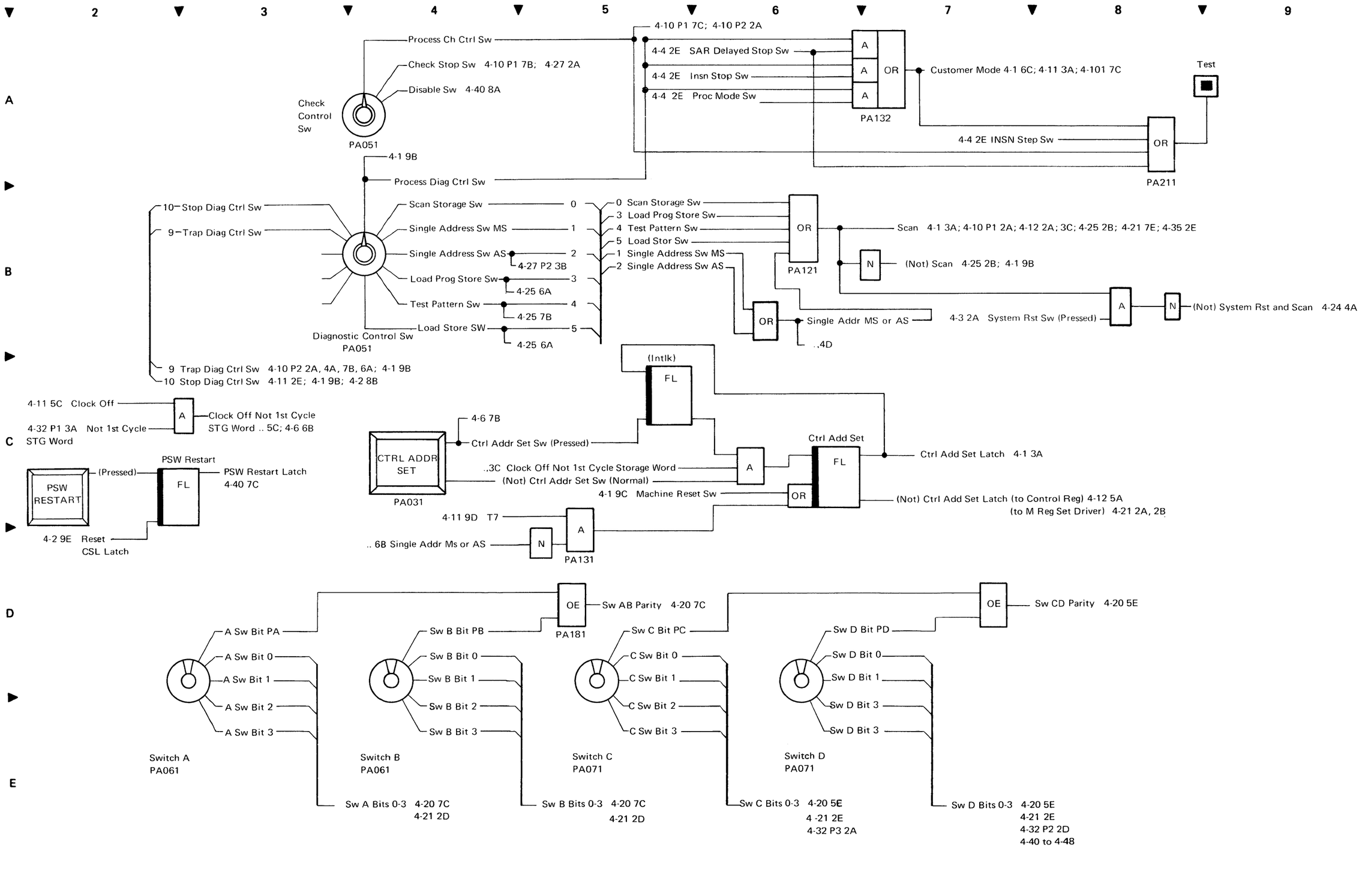
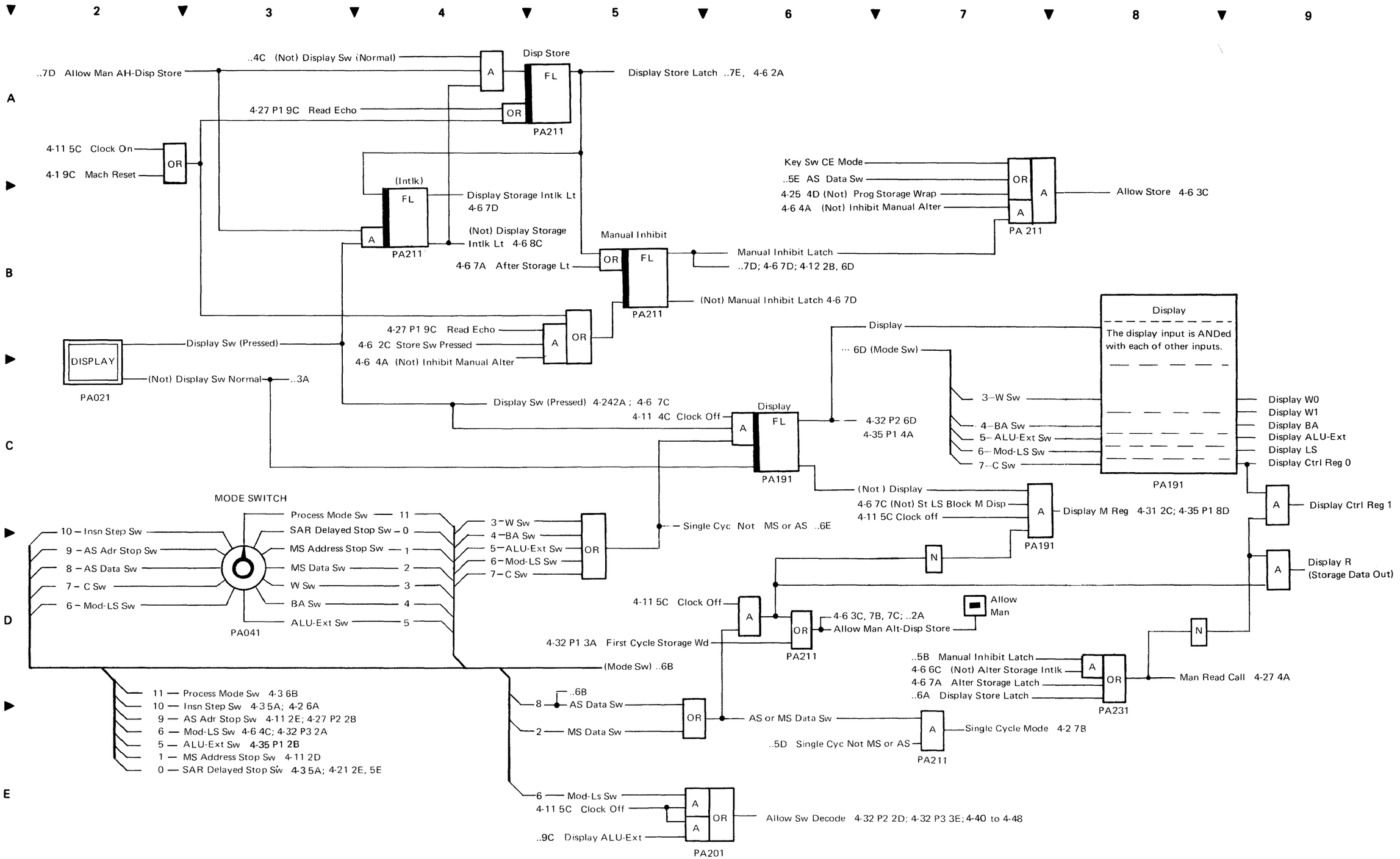

2
3
4
5
6
7
8
9
A
B
C
D
E
Process Ch Ctrl Sw
Check Stop Sw 4-10 P1 7B; 4-27 2A
Disable Sw 4-40 8A
Check Control Sw
PA051
4-10 P1 7C; 4-10 P2 2A
4-4 2E SAR Delayed Stop Sw
4-4 2E Insn Stop Sw
4-4 2E Proc Mode Sw
A
A
A
OR
PA132
Customer Mode 4-1 6C; 4-11 3A; 4-101 7C
Test
4-4 2E INSN Step Sw
OR
PA211
4-1 9B
Process Diag Ctrl Sw
10 Stop Diag Ctrl Sw
9 Trap Diag Ctrl Sw
Scan Storage Sw 0
Single Address Sw MS 1
Single Address Sw AS 2
4-27 P2 3B
Load Prog Store Sw 3
4-25 6A
Test Pattern Sw 4
4-25 7B
Load Store SW 5
4-25 6A
Diagnostic Control Sw
PA051
0 Scan Storage Sw
3 Load Prog Store Sw
4 Test Pattern Sw
5 Load Stor Sw
1 Single Address Sw MS
2 Single Address Sw AS
OR
PA121
Scan 4-1 3A; 4-10 P1 2A; 4-12 2A; 3C; 4-25 2B; 4-21 7E; 4-35 2E
N
(Not) Scan 4-25 2B; 4-1 9B
OR
Single Addr MS or AS
..4D
4-3 2A System Rst Sw (Pressed)
A
N
(Not) System Rst and Scan 4-24 4A
9 Trap Diag Ctrl Sw 4-10 P2 2A, 4A, 7B, 6A; 4-1 9B
10 Stop Diag Ctrl Sw 4-11 2E; 4-1 9B; 4-2 8B
4-11 5C Clock Off
4-32 P1 3A Not 1st Cycle
A
Clock Off Not 1st Cycle STG Word .. 5C; 4-6 6B
STG Word
PSW Restart
PSW RESTART
(Pressed)
FL
PSW Restart Latch 4-40 7C
4-2 9E Reset CSL Latch
(Intlk)
FL
4-6 7B
CTRL ADDR SET
Ctrl Addr Set Sw (Pressed)
PA031
..3C Clock Off Not 1st Cycle Storage Word
(Not) Ctrl Addr Set Sw (Normal)
A
Ctrl Add Set
FL
Ctrl Add Set Latch 4-1 3A
4-1 9C Machine Reset Sw
OR
(Not) Ctrl Add Set Latch (to Control Reg) 4-12 5A
(to M Reg Set Driver) 4-21 2A, 2B
4-11 9D T7
.. 6B Single Addr Ms or AS
N
A
PA131
OE
Sw AB Parity 4-20 7C
PA181
A Sw Bit PA
A Sw Bit 0
A Sw Bit 1
A Sw Bit 2
A Sw Bit 3
Switch A
PA061
Sw A Bits 0-3 4-20 7C
4-21 2D
Sw B Bit PB
Sw B Bit 0
Sw B Bit 1
Sw B Bit 2
Sw B Bit 3
Switch B
PA061
Sw B Bits 0-3 4-20 7C
4-21 2D
Sw C Bit PC
C Sw Bit 0
C Sw Bit 1
C Sw Bit 2
C Sw Bit 3
Switch C
PA071
Sw C Bits 0-3 4-20 5E
4 -21 2E
4-32 P3 2A
OE
Sw CD Parity 4-20 5E
Sw D Bit PD
Sw D Bit 0
Sw D Bit 1
Sw D Bit 3
Sw D Bit 3
Switch D
PA071
Sw D Bits 0-3 4-20 5E
4-21 2E
4-32 P2 2D
4-40 to 4-48

Diagram 4-4. Manual Switches (Display)



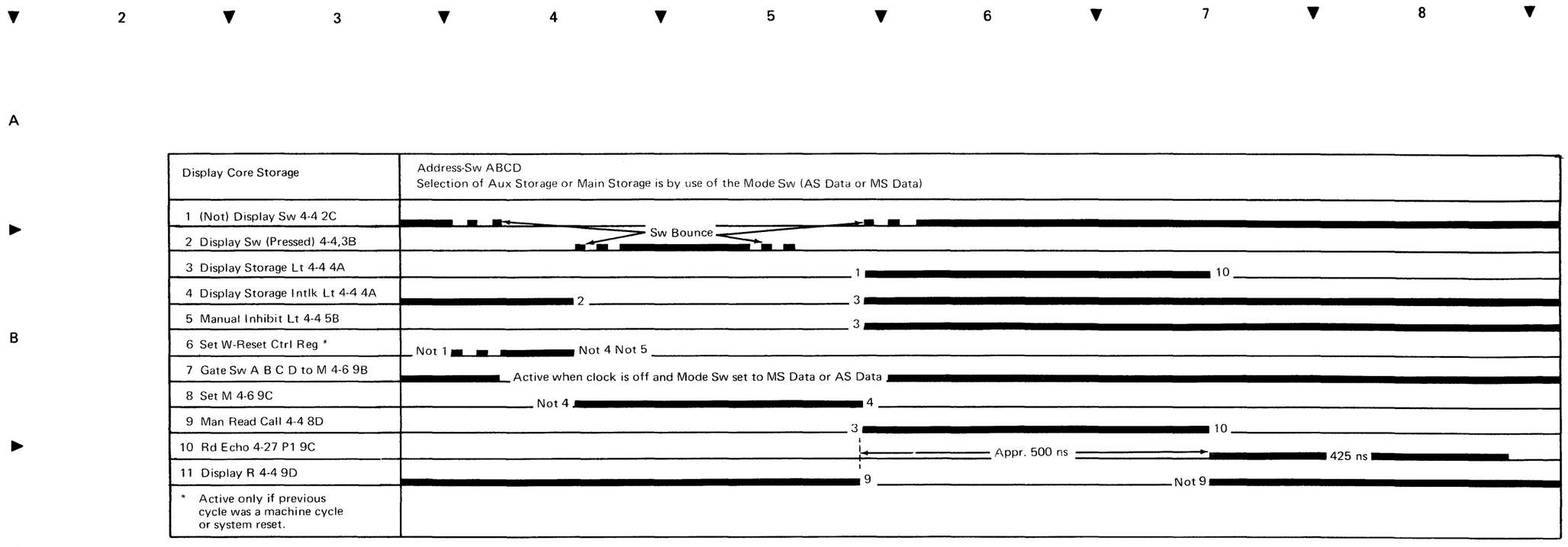
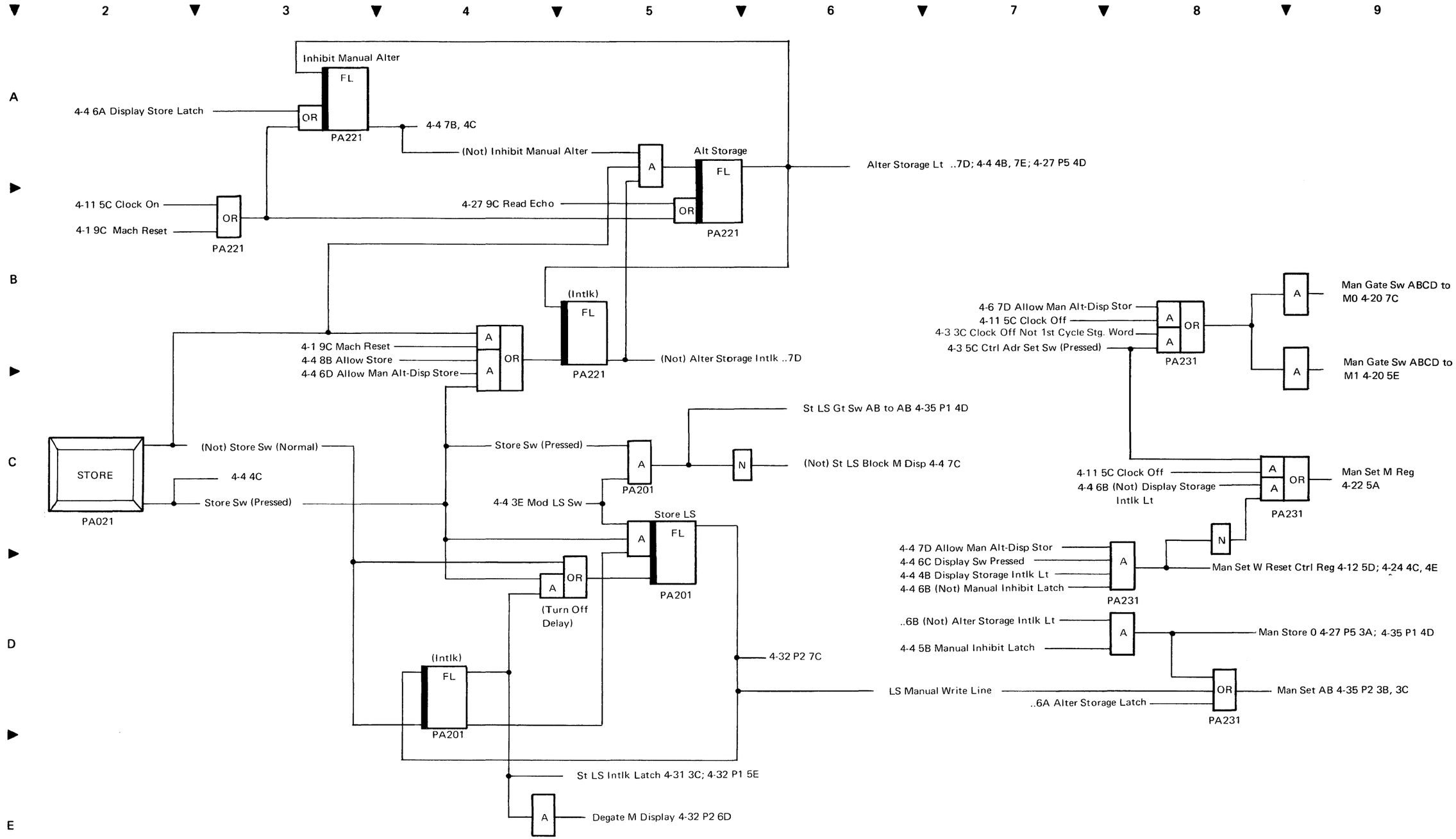

2
3
4
5
6
7
8
9
A
B
C
D
E
Display Core Storage
Address-Sw ABCD
Selection of Aux Storage or Main Storage is by use of the Mode Sw (AS Data or MS Data)
1 (Not) Display Sw 4-4 2C
2 Display Sw (Pressed) 4-4,3B
3 Display Storage Lt 4-4 4A
4 Display Storage Intlk Lt 4-4 4A
5 Manual Inhibit Lt 4-4 5B
6 Set W-Reset Ctrl Reg *
7 Gate Sw A B C D to M 4-6 9B
8 Set M 4-6 9C
9 Man Read Call 4-4 8D
10 Rd Echo 4-27 P1 9C
11 Display R 4-4 9D
* Active only if previous cycle was a machine cycle or system reset.
Sw Bounce
1
10
2
3
3
Not 1
Not 4 Not 5
Active when clock is off and Mode Sw set to MS Data or AS Data
Not 4
4
3
10
Appr. 500 ns
425 ns
9
Not 9

Diagram 4-6. Manual Switch (Store)



2 3 4 5 6 7 8 9

Store Local Storage Data-Sw AB Address-Sw CD (No Time Base)

1	(Not) Store Sw	4-6 2C	Sw Bounce
2	Store Sw (Pressed)	4-6 2C	
3	Store LS Latch	4-6 5D	2 10
4	Store LS Intlk Lt	4-6 4D	3 1
5	Allow Sw Decode	4-4 6E	
6	Display M	4-4 8C	2 (Not) 2
7	Man Set AB	4-6 9B	2 2
8	Gate Sw AB to AB	4-6 6C	
9	Gate B to LS Asm	4-31 7C	
10	LS Latch (Turn Off Delay)	4-6 4D	1 2·4 2 1

Alter Core Storage: Display halfword must be done first.
Alter Aux Storage if Mode Sw to AS Data
Alter program storage if Mode Sw to MS Data; To Alter control storage CE key must be On.

After alter is completed the data set into core storage is displayed in byte 0 and byte 1 indicators.

1	(Not) Store Sw	4-6 2C	Switch Bounce
2	Store Sw (Pressed)	4-6 2C	Switch Bounce
3	Alter Storage Lt	4-6 2C	1 9
4	Alter Storage Intlk Lt	4-6 5B	2 3
5	Man Inhibit Lt	4-4 5B	9 3
6	Gate Sw AB to AB	4-6 6C	
7	Man Read Call	4-4 8D	(Not) 4 (Not)5 3 (Not)3
8	Man Store 0	4-6 9D	(Not)4 (Not)5
9	Rd Echo	4-27 P1 9C	Appr. 500 ns after 7 425 ns Appr. 500 ns after 7 425ns
10	Man Set AB	4-6 9E	(Not)4 (Not)5
11	Inhibit Manual Alter Lt	4-6 3A	3
12	Display R (Storage Data)	4-4 9D	7 (Not)7 7 (Not)7
13	Store Byte 0	4-27 P5 4A	8 (Not)8
14	Store Byte 1	4-27 P5 5D	3 (Not)3
15	Gate Sw CD to AB	4-35 P1 6E	

Diagram 4-10. Error Latches (Part 1 of 3)

2 3 4 5 6 7 8 9

A

4-11 9D T7 — (Allow PC) FL — Allow PC — 1

..6B Check Reset Sw (Pressed)
4-11 5C Clock Off
4-1 9C Machine Reset Sw
A OR
PA121

4-10 P3 8B, 8C, 8D
4-12 5D; 4-75 2E

B

Storage Data Parity Check

Check Storage Data Out Bits P0, 0-7. If Even, Parity Error Exists.

Check Storage Data Out Bits P1, 8-15. If Even, Parity Error Exists.

RC071

4-12 5B Prog Mem Word Cycle
(Even Parity)
(Not) Check R1
(Not) Check R0
(Even Parity)
4-3 5B Scan
A A A OR — 3
RC071

OR

4-337 9D (Not) Share Cycle
4-12 5A (Ctrl Cycle AB)
4-12 5B (Not) PMWC
A — 4
RC071

C

4-21 4D (Not) M1 Reg Bit 7
4-12 5B PMWC
OR
4-21 4D M1 Reg Bit 7
OR
MC181

D

Mem Addr Parity Check

Mem Addr Bits 0-14, M1 Reg Bits P and 7, and M0 P Bit Corrected are Checked for Even Parity. If Even, Parity Error Exists

MP071

4-20 4C (Not) Gate Br Mask to M — A — M-Reg Even — 5
MP071

E

..6C Mach Or Chk Rst — OR — (Reset) — 2
4-10 P3 8B,C,D

4-15 6C KH Decode 9
4-15 6C MMSK Reset Pulse
A — Reset Error Reg — 4-10 P2 7C
RM041

CHECK RESET
PR021

Check Reset Sw (Pressed) ..2A; 4-10 P2 2B; 4-12 2B

4-13 8D Check Sum Latch
..9D Error Pulse
4-3 8A Check Stop Switch
4-13 8D (Not) DR-0 Disable CPU Error Stop
Chnl Parity Check Latch GS3
4-3 4A Process Ch Ctrl Switch
..9D Error Pulse
A A A OR

4-15 8C MMSK Reg Bit 8
4-15 8C MMSK Reg Bit 9
OR

Hard Stop
FL
Hard Stop 4-11 3B
(Not) Hard Stop 4-11 2C; 4-1 7B
KC051

4-1 9C Machine Reset Sw
OR
Mach Or Chk Rst
..3D
KC051

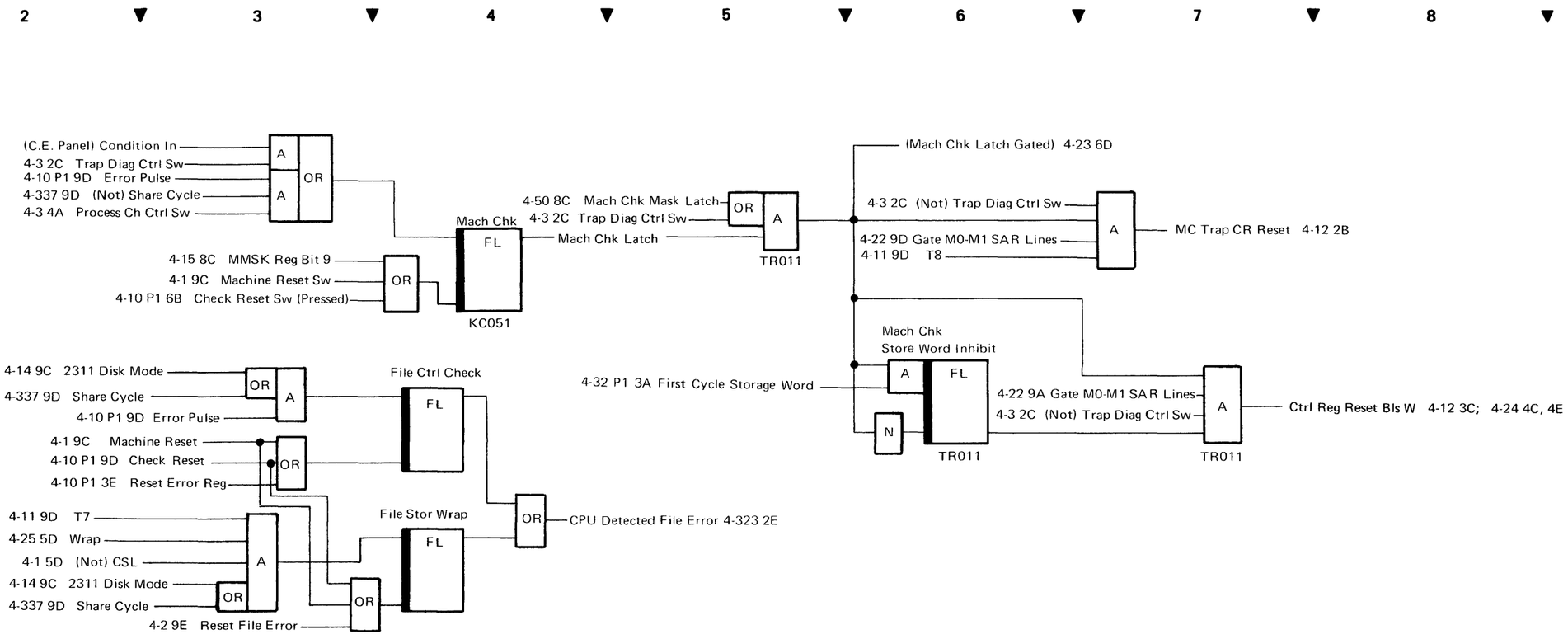
1 — Allow PC
4 — 4-11 9B T3
3 — Storage Data Check
A
Storage Data Check
FL
Storage Data Parity Latch — 4-21 2A; 4-40 7C
Mem Data
2 — (Reset)
KC062

4-13 8D (Not) DR-0 Disable CPU Error Stop
4-90 P2 9D Set STP Parity Error
OR A
4-10 P2 2A
Error Pulse ..7B, 7C
KC062

1 — Allow PC
4-11 9B T3
4 — Ctrl Word Parity Error
A
Ctrl Word Check
FL
Ctrl Word Parity Latch — 4-27 2A; 4-40 7C
Ctrl Word
2 — (Reset)
KC062

4-10 P3 9C Error Pulse 1

1 — Allow PC
4-11 9E T8
5 — M Reg Even
A
Stor Addr Check
FL
Storage Address Check Latch — 4-40 7C
Stor Addr
2 — (Reset)
KC062



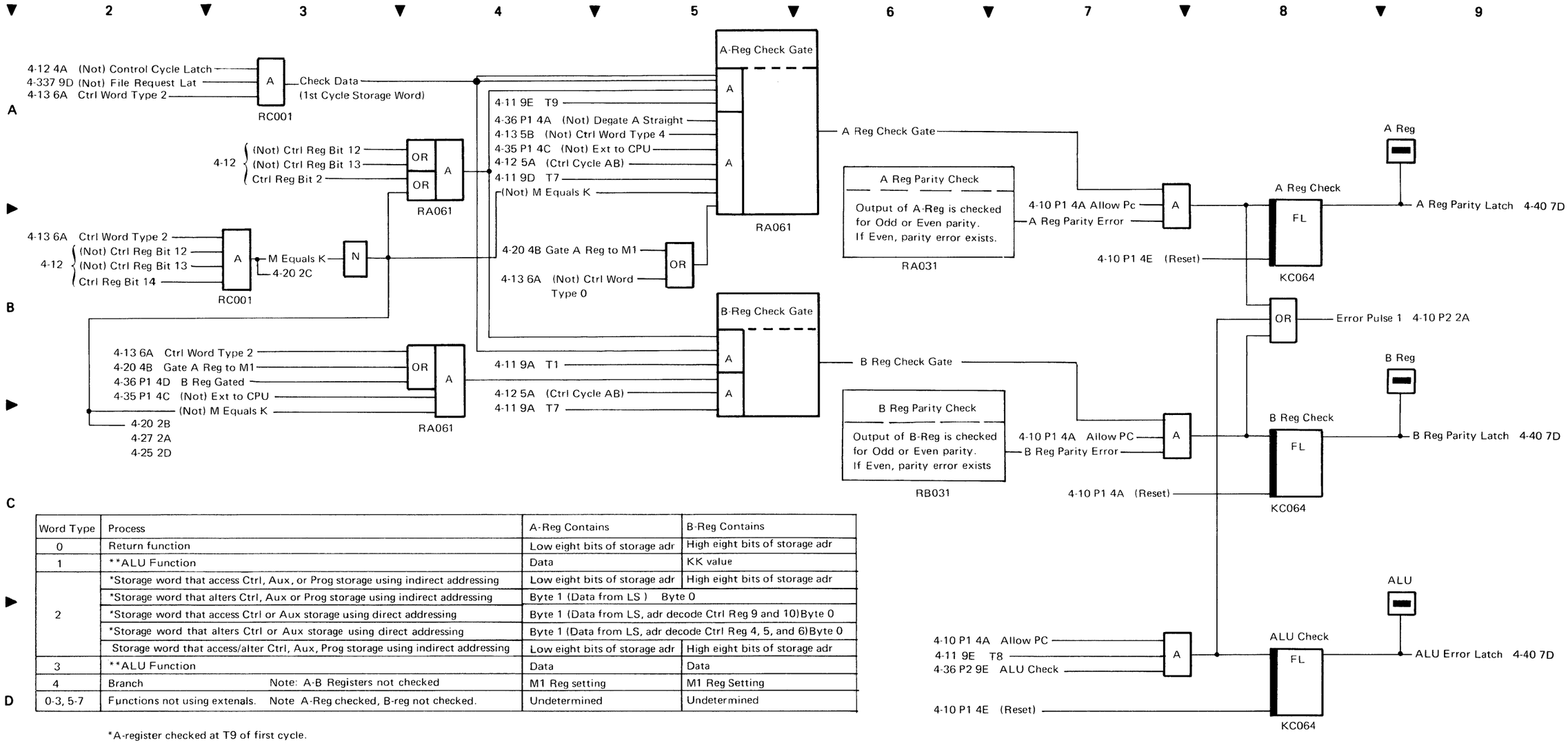
Mach Chk Trap with Trap Diag Ctrl Sw Off	During Storage Word (Word Type 2)			During Word Types 0, 1, 3-7		
	T0		T0	T0		T0
	1st Cycle Stor Wd	2nd Cycle Stor Wd	1st Wd of Trap	Ctrl Word X	* No Operation	1st Wd of Trap
1 Mach Chk Latch 4-10 4A						
2 Mch Chk Stor Word Inh Lt 4-10 6B						
3 Gate M0-M1 to SAR Lines 4-22 9A						
4 Ctrl Cycle Lt 4-12 4A					5	
5 MC Trap CR Reset 4-10 7A		Note 1			Note 1	
6 Ctrl Reg Reset Bls W 4-10 8B		Note 2			Blocks W Reg Set	Note 1
7 Ctrl Reg Reset 4-12 6D						
8 Mach Chk Mask Latch 4-50 8D						

Note 1: Reset does not occur when the Trap Diag Ctrl Sw is on.

Note 2: Second cycle of storage word normally blocks set C-register and set W-register.

* No operation occurs during this cycle; cycle is required to save the address + 2 where the error occurred. Ctrl reg is reset at T0 of the no operation cycle and is not set.

Diagram 4-10. Error Latches (Part 3 of 3)



Word Type	Process	A-Reg Contains	B-Reg Contains
0	Return function	Low eight bits of storage adr	High eight bits of storage adr
1	**ALU Function	Data	KK value
2	*Storage word that access Ctrl, Aux, or Prog storage using indirect addressing	Low eight bits of storage adr	High eight bits of storage adr
	*Storage word that alters Ctrl, Aux or Prog storage using indirect addressing	Byte 1 (Data from LS)	Byte 0
	*Storage word that access Ctrl or Aux storage using direct addressing	Byte 1 (Data from LS, adr decode Ctrl Reg 9 and 10)	Byte 0
	*Storage word that alters Ctrl or Aux storage using direct addressing	Byte 1 (Data from LS, adr decode Ctrl Reg 4, 5, and 6)	Byte 0
	Storage word that access/alter Ctrl, Aux, Prog storage using indirect addressing	Low eight bits of storage adr	High eight bits of storage adr
3	**ALU Function	Data	Data
4	Branch Note: A-B Registers not checked	M1 Reg setting	M1 Reg Setting
0-3, 5-7	Functions not using extenals. Note A-Reg checked, B-reg not checked.	Undetermined	Undetermined

*A-register checked at T9 of first cycle.
B-register checked at T1 of second cycle.

**A-register and/or B-register checked if gated.

Diagram 4-11. Clock Logic (Part 1 of 2)

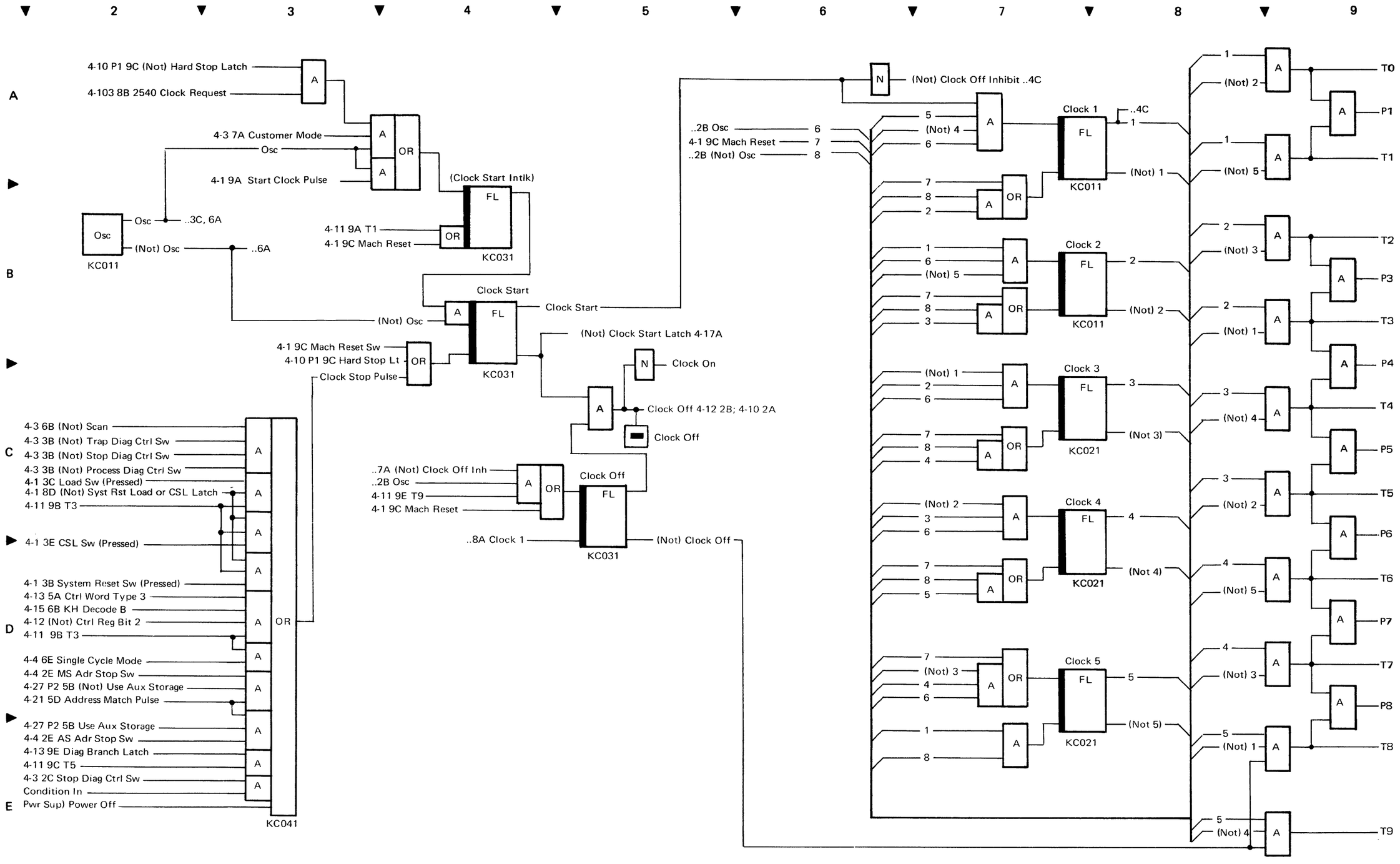
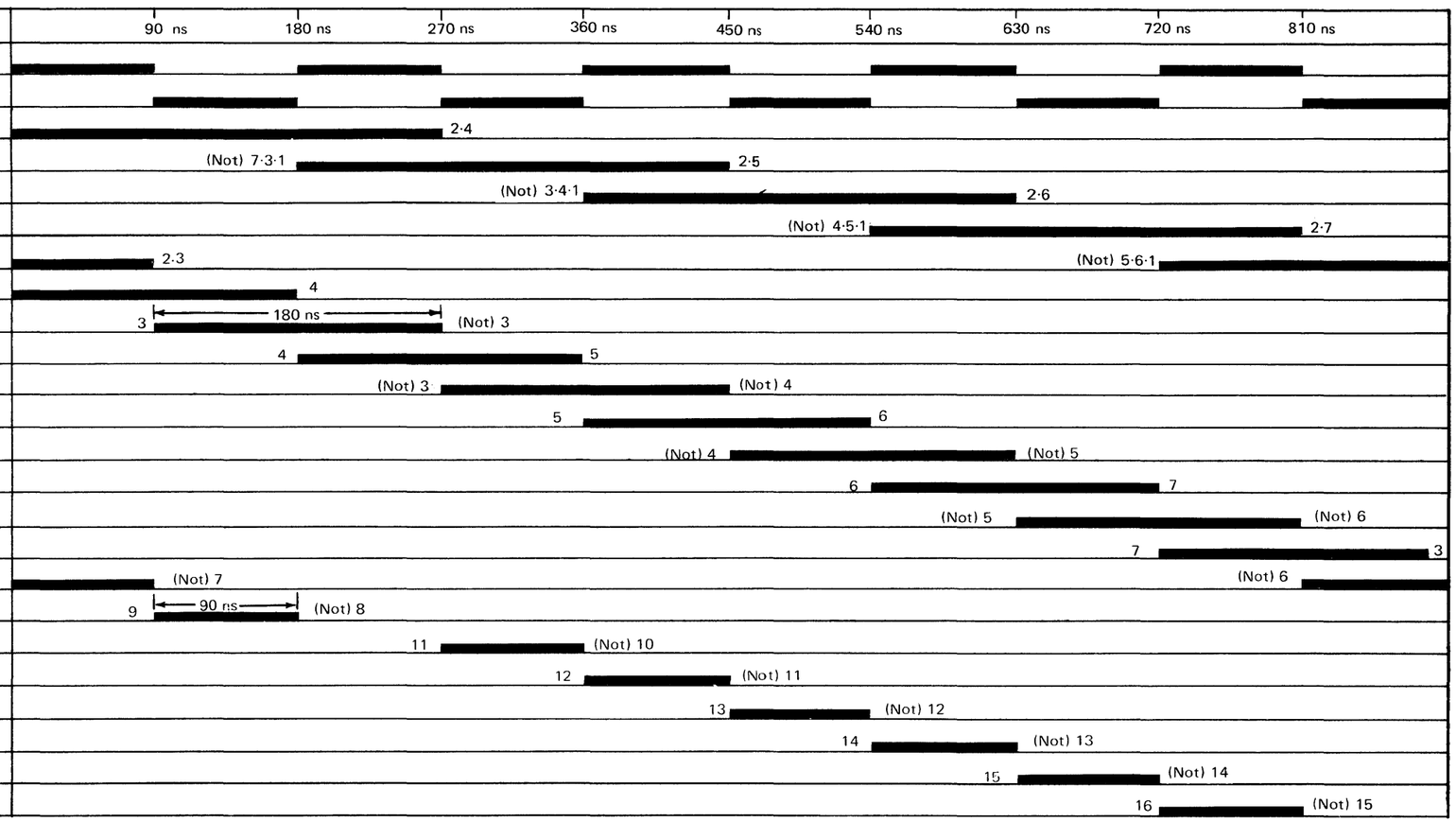


Diagram 4-11. Clock Timing (Part 2 of 2)

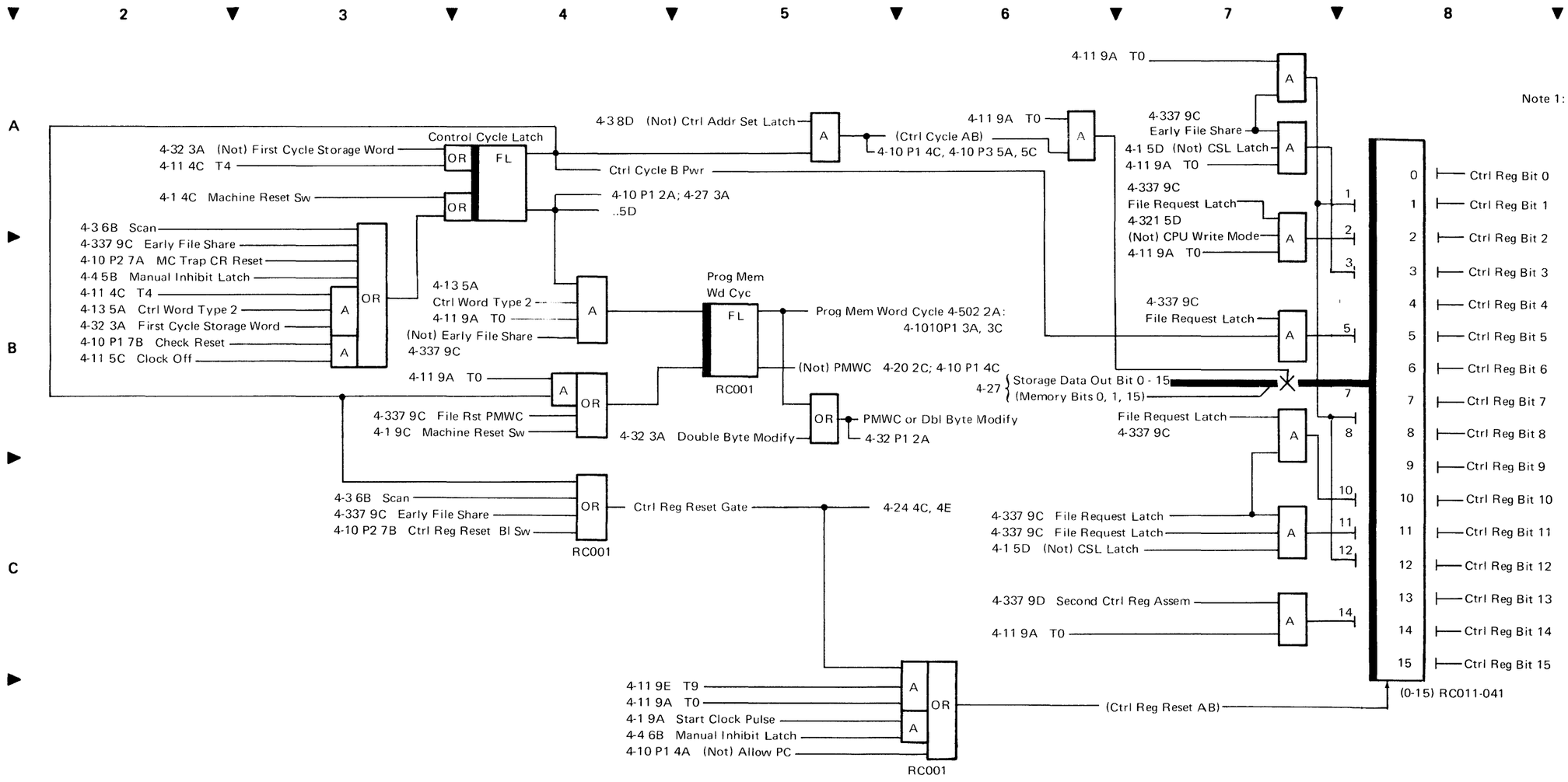
1	OSC	4-11	2A	
2	(Not) OSC	4-11	2A	
3	Clock 1	4-11	8A*	
4	Clock 2	4-11	8B*	
5	Clock 3	4-11	8C*	
6	Clock 4	4-11	8D*	
7	Clock 5	4-11	8D*	
8	Clock T0	4-11	9A	
9	Clock T1	4-11	9A	
10	Clock T2	4-11	9B	
11	Clock T3	4-11	9B	
12	Clock T4	4-11	9C	
13	Clock T5	4-11	9C	
14	Clock T6	4-11	9C	
15	Clock T7	4-11	9D	
16	Clock T8	4-11	9D**	
17	Clock T9	4-11	9C**	
18	Clock P1	4-11	9A	
19	Clock P3	4-11	9B	
20	Clock P4	4-11	9B	
21	Clock P5	4-11	9C	
22	Clock P6	4-11	9C	
23	Clock P7	4-11	9D	
24	Clock P8	4-11	9D	



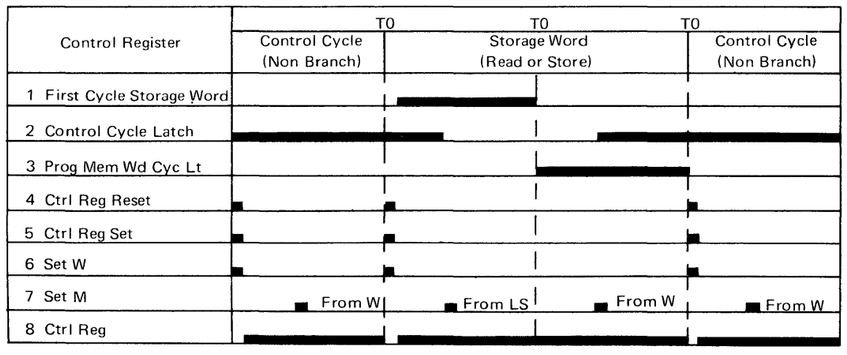
*Machine reset turns Clock 1, 2, 3, and 4 off and turns Clock 5 on.

**When clock is off these lines are blocked.

Diagram 4-12. Control Register



Note 1: For control word typess 4, 5, 6, and 7 Ctrl Reg Bit 5 is set to a 1 (limits register addressing) Storage Data Out Bit 5 is used as a replacement bit for word type 4 and for testing A-Reg gates on word type 5, 6, and 7.



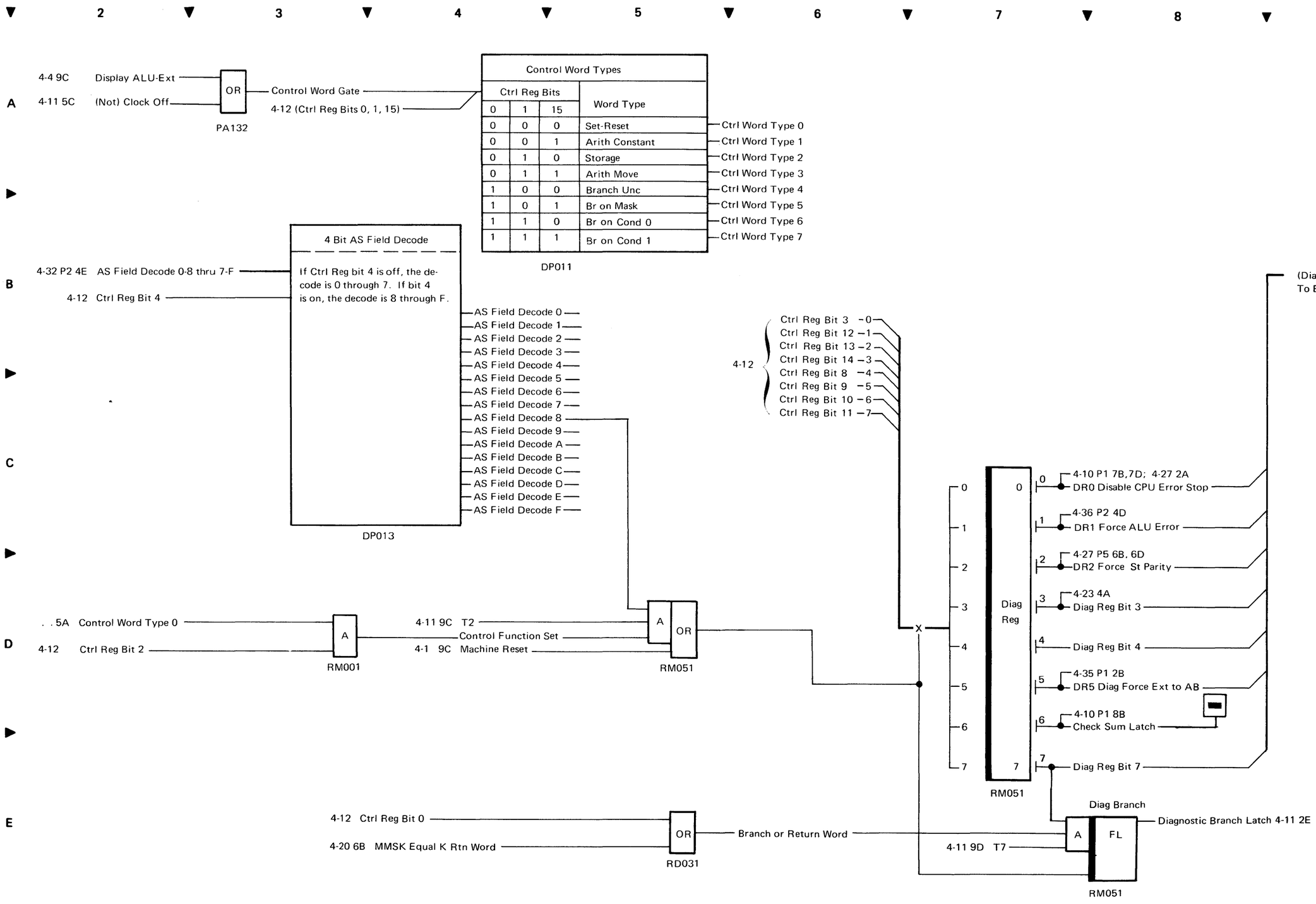
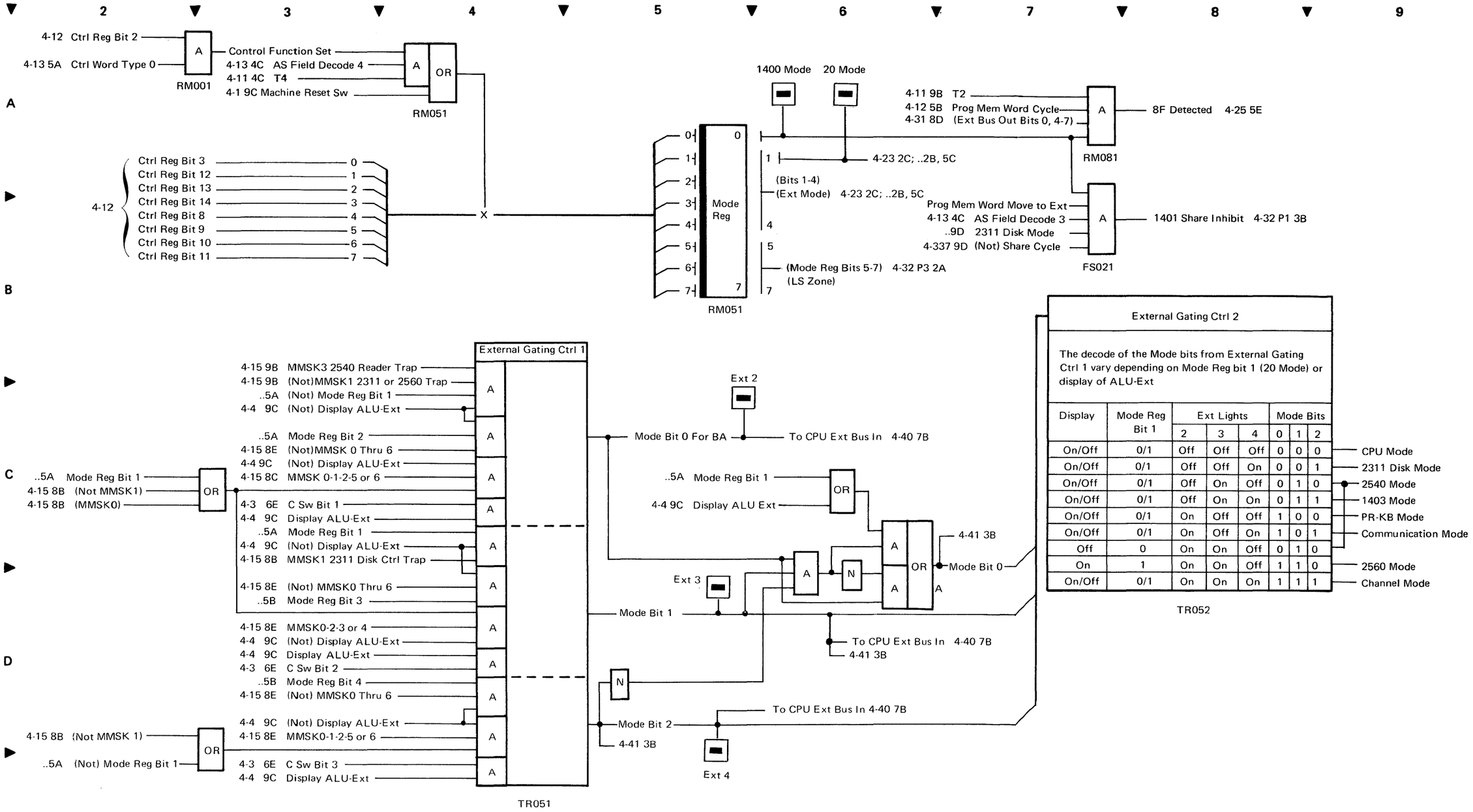

2
3
4
5
6
7
8
9
A
B
C
D
E
4-4 9C Display ALU-Ext
4-11 5C (Not) Clock Off
OR
PA132
Control Word Gate
4-12 (Ctrl Reg Bits 0, 1, 15)
Control Word Types
Ctrl Reg Bits
Word Type
0 1 15
0 0 0 Set-Reset
0 0 1 Arith Constant
0 1 0 Storage
0 1 1 Arith Move
1 0 0 Branch Unc
1 0 1 Br on Mask
1 1 0 Br on Cond 0
1 1 1 Br on Cond 1
Ctrl Word Type 0
Ctrl Word Type 1
Ctrl Word Type 2
Ctrl Word Type 3
Ctrl Word Type 4
Ctrl Word Type 5
Ctrl Word Type 6
Ctrl Word Type 7
DP011
4-32 P2 4E AS Field Decode 0-8 thru 7-F
4-12 Ctrl Reg Bit 4
4 Bit AS Field Decode
If Ctrl Reg bit 4 is off, the decode is 0 through 7. If bit 4 is on, the decode is 8 through F.
AS Field Decode 0
AS Field Decode 1
AS Field Decode 2
AS Field Decode 3
AS Field Decode 4
AS Field Decode 5
AS Field Decode 6
AS Field Decode 7
AS Field Decode 8
AS Field Decode 9
AS Field Decode A
AS Field Decode B
AS Field Decode C
AS Field Decode D
AS Field Decode E
AS Field Decode F
DP013
4-12
Ctrl Reg Bit 3 – 0
Ctrl Reg Bit 12 – 1
Ctrl Reg Bit 13 – 2
Ctrl Reg Bit 14 – 3
Ctrl Reg Bit 8 – 4
Ctrl Reg Bit 9 – 5
Ctrl Reg Bit 10 – 6
Ctrl Reg Bit 11 – 7
(Diag Reg Bits 0-5, 7)
To Ext Bus In 4-40 7C
. . 5A Control Word Type 0
4-12 Ctrl Reg Bit 2
A
RM001
4-11 9C T2
Control Function Set
4-1 9C Machine Reset
A
OR
RM051
X
0
1
2
3
4
5
6
7
Diag Reg
0
7
RM051
0 4-10 P1 7B,7D; 4-27 2A
DR0 Disable CPU Error Stop
1 4-36 P2 4D
DR1 Force ALU Error
2 4-27 P5 6B, 6D
DR2 Force St Parity
3 4-23 4A
Diag Reg Bit 3
4 Diag Reg Bit 4
5 4-35 P1 2B
DR5 Diag Force Ext to AB
6 4-10 P1 8B
Check Sum Latch
7 Diag Reg Bit 7
4-12 Ctrl Reg Bit 0
4-20 6B MMSK Equal K Rtn Word
OR
RD031
Branch or Return Word
Diag Branch
A
FL
RM051
4-11 9D T7
Diagnostic Branch Latch 4-11 2E

Diagram 4-14. Mode Register and Mode Decode

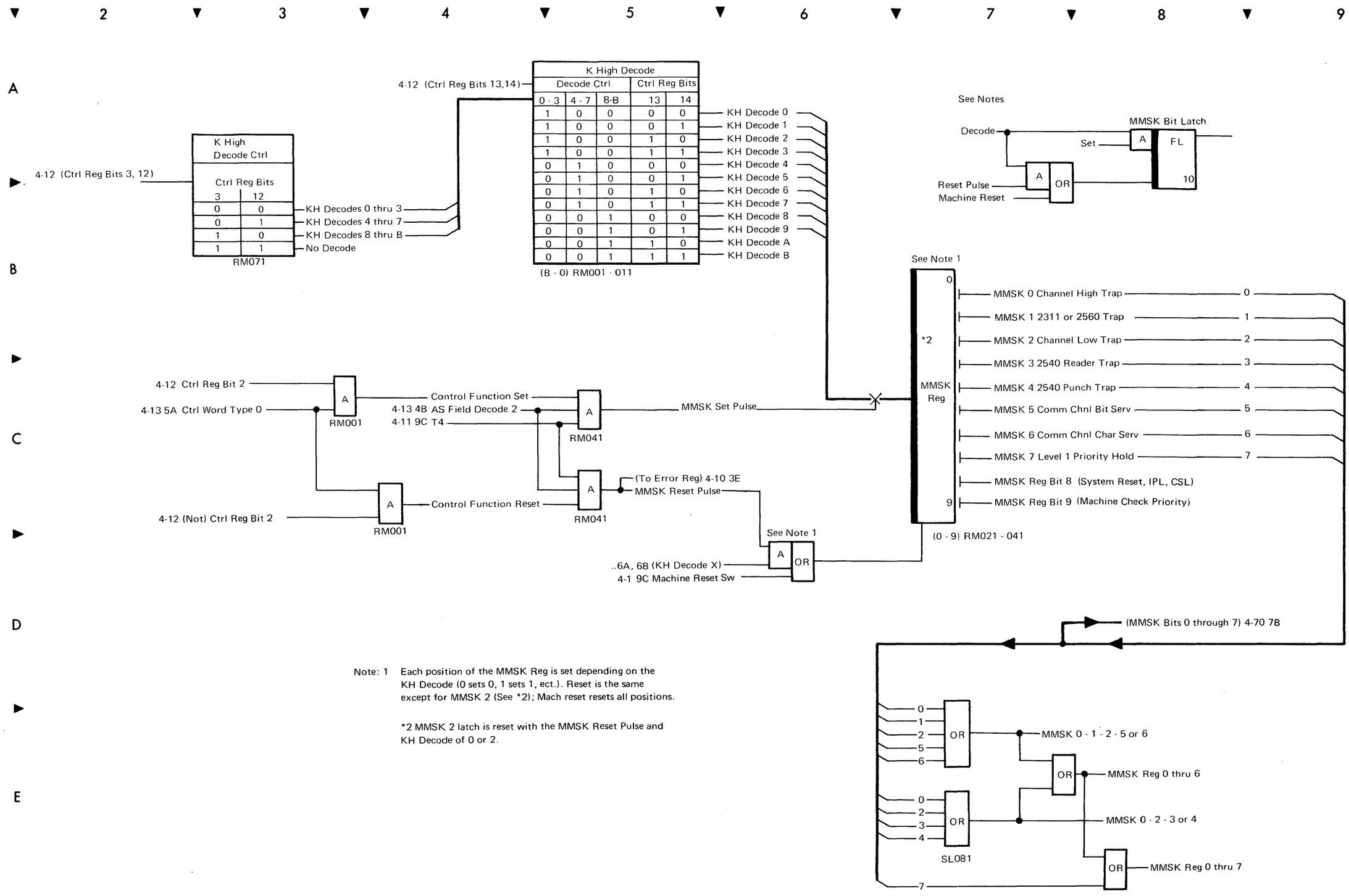


External Gating Ctrl 2

The decode of the Mode bits from External Gating Ctrl 1 vary depending on Mode Reg bit 1 (20 Mode) or display of ALU-Ext

Display	Mode Reg Bit 1	Ext Lights			Mode Bits			
		2	3	4	0	1	2	
On/Off	0/1	Off	Off	Off	0	0	0	CPU Mode
On/Off	0/1	Off	Off	On	0	0	1	2311 Disk Mode
On/Off	0/1	Off	On	Off	0	1	0	2540 Mode
On/Off	0/1	Off	On	On	0	1	1	1403 Mode
On/Off	0/1	On	Off	Off	1	0	0	PR-KB Mode
On/Off	0/1	On	Off	On	1	0	1	Communication Mode
Off	0	On	On	Off	0	1	0	
On	1	On	On	Off	1	1	0	2560 Mode
On/Off	0/1	On	On	On	1	1	1	Channel Mode

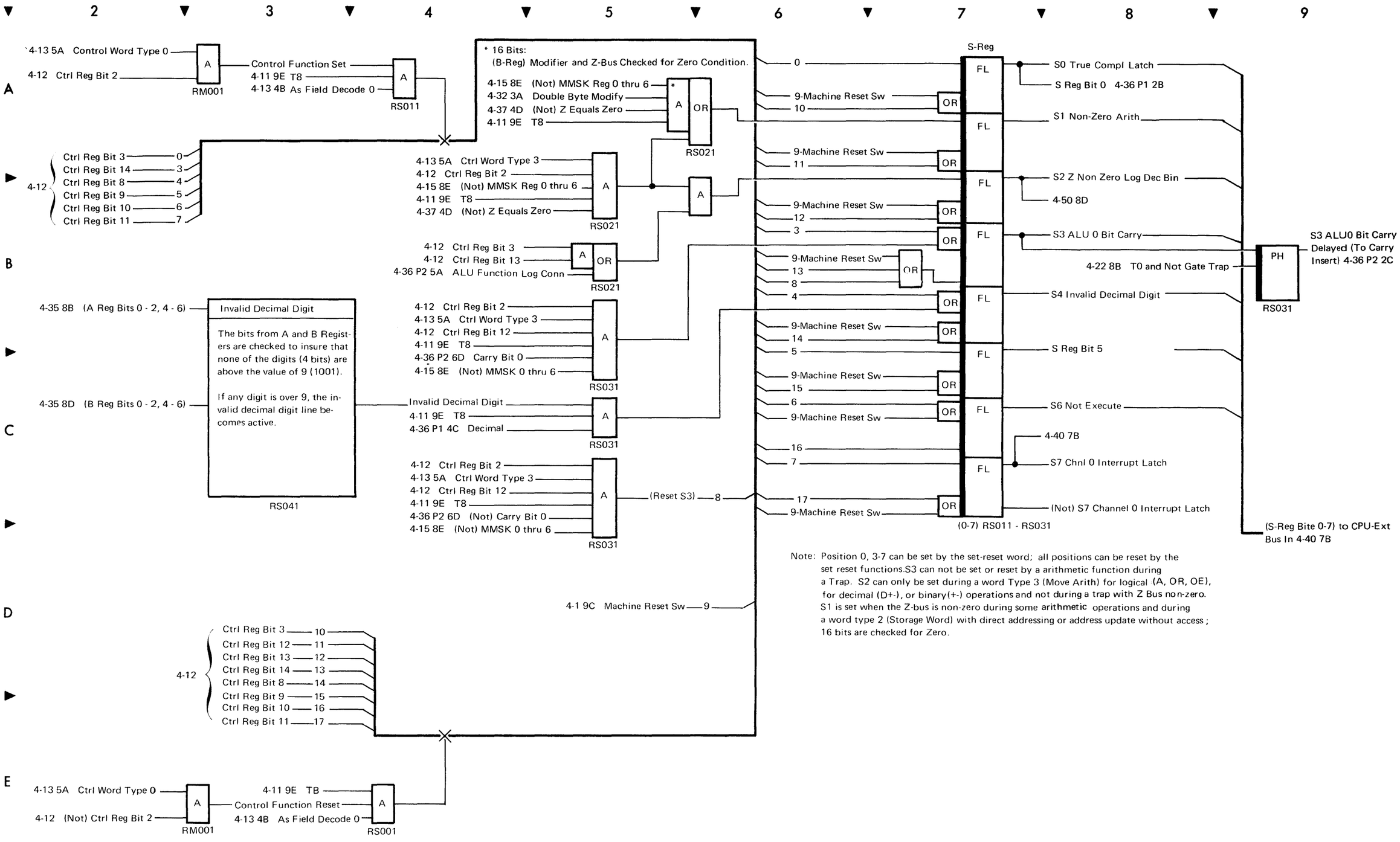
TR052



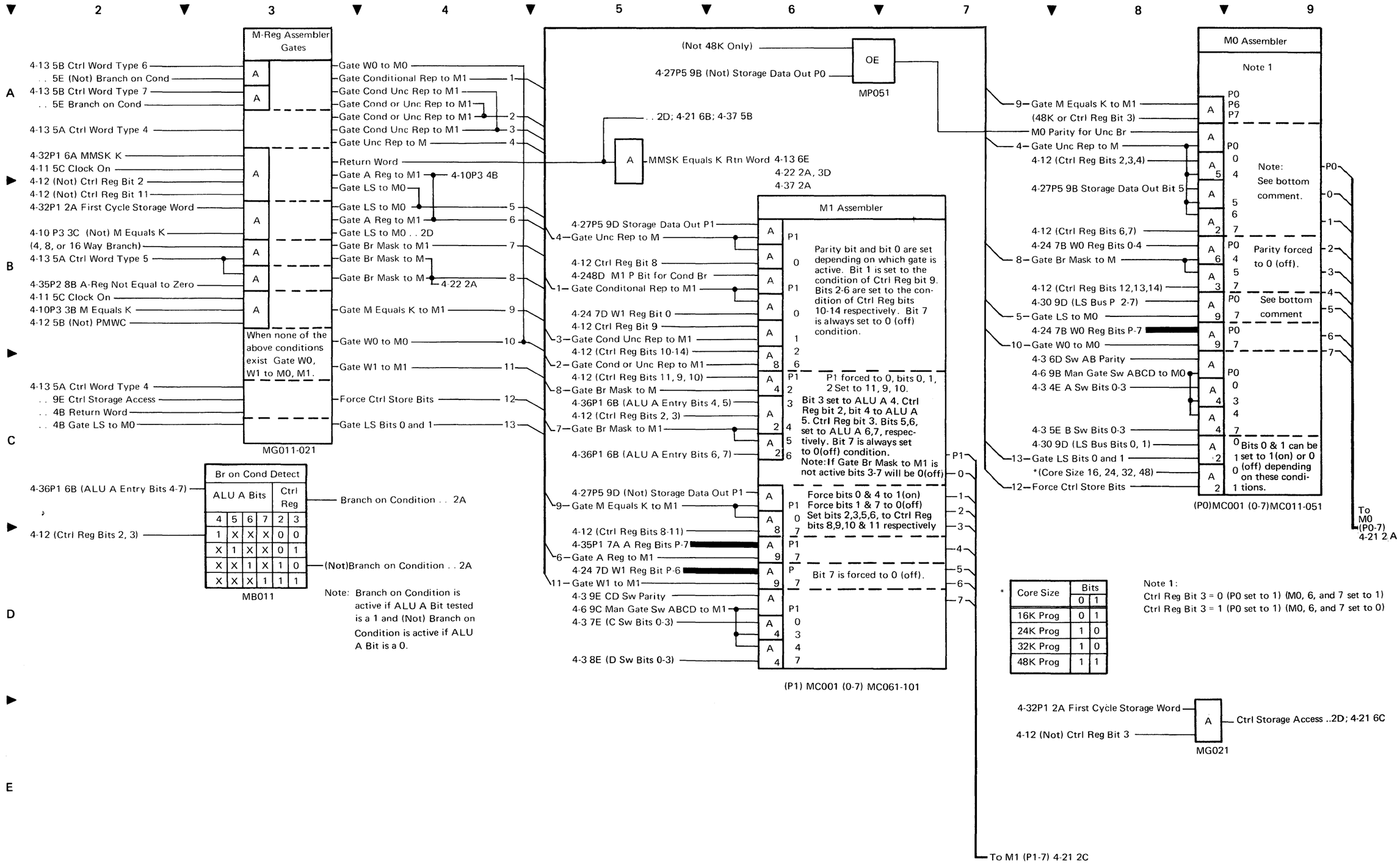
Note: 1 Each position of the MMSK Reg is set depending on the KH Decode (0 sets 0, 1 sets 1, ect.). Reset is the same except for MMSK 2 (See *2); Mach reset resets all positions.

*2 MMSK 2 latch is reset with the MMSK Reset Pulse and KH Decode of 0 or 2.

Diagram 4-16. S Register



Note: Position 0, 3-7 can be set by the set-reset word; all positions can be reset by the set reset functions.S3 can not be set or reset by a arithmetic function during a Trap. S2 can only be set during a word Type 3 (Move Arith) for logical (A, OR, OE), for decimal (D+-), or binary(+-) operations and not during a trap with Z Bus non-zero. S1 is set when the Z-bus is non-zero during some arithmetic operations and during a word type 2 (Storage Word) with direct addressing or address update without access ; 16 bits are checked for Zero.


2
3
4
5
6
7
8
9
A
B
C
D
E
M-Reg Assembler Gates
4-13 5B Ctrl Word Type 6
5E (Not) Branch on Cond
4-13 5B Ctrl Word Type 7
5E Branch on Cond
4-13 5A Ctrl Word Type 4
4-32P1 6A MMSK K
4-11 5C Clock On
4-12 (Not) Ctrl Reg Bit 2
4-12 (Not) Ctrl Reg Bit 11
4-32P1 2A First Cycle Storage Word
4-10 P3 3C (Not) M Equals K (4, 8, or 16 Way Branch)
4-13 5A Ctrl Word Type 5
4-35P2 8B A-Reg Not Equal to Zero
4-11 5C Clock On
4-10P3 3B M Equals K
4-12 5B (Not) PMWC
Gate W0 to M0
Gate Conditional Rep to M1 1
Gate Cond Unc Rep to M1
Gate Cond or Unc Rep to M1
Gate Cond or Unc Rep to M1 2
Gate Cond Unc Rep to M1 3
Gate Unc Rep to M 4
Return Word
Gate A Reg to M1
4-10P3 4B
Gate LS to M0
Gate LS to M0 5
Gate A Reg to M1 6
Gate LS to M0 . . 2D
Gate Br Mask to M1 7
Gate Br Mask to M
Gate Br Mask to M 8
4-22 2A
Gate M Equals K to M1 9
When none of the above conditions exist Gate W0, W1 to M0, M1.
Gate W0 to M0 10
Gate W1 to M1 11
4-13 5A Ctrl Word Type 4
9E Ctrl Storage Access
4B Return Word
4B Gate LS to M0
Force Ctrl Store Bits 12
Gate LS Bits 0 and 1 13
MG011-021
Br on Cond Detect
ALU A Bits
Ctrl Reg
4-36P1 6B (ALU A Entry Bits 4-7)
4-12 (Ctrl Reg Bits 2, 3)
Branch on Condition . . 2A
(Not)Branch on Condition . . 2A
MB011
Note: Branch on Condition is active if ALU A Bit tested is a 1 and (Not) Branch on Condition is active if ALU A Bit is a 0.
(Not 48K Only)
4-27P5 9B (Not) Storage Data Out P0
OE
MP051
. . 2D; 4-21 6B; 4-37 5B
MMSK Equals K Rtn Word 4-13 6E
4-22 2A, 3D
4-37 2A
M1 Assembler
4-27P5 9D Storage Data Out P1
4-Gate Unc Rep to M
4-12 Ctrl Reg Bit 8
4-248D M1 P Bit for Cond Br
1-Gate Conditonal Rep to M1
4-24 7D W1 Reg Bit 0
4-12 Ctrl Reg Bit 9
3-Gate Cond Unc Rep to M1
4-12 (Ctrl Reg Bits 10-14)
2-Gate Cond or Unc Rep to M1
4-12 (Ctrl Reg Bits 11, 9, 10)
8-Gate Br Mask to M
4-36P1 6B (ALU A Entry Bits 4, 5)
4-12 (Ctrl Reg Bits 2, 3)
7-Gate Br Mask to M1
4-36P1 6B (ALU A Entry Bits 6, 7)
4-27P5 9D (Not) Storage Data Out P1
9-Gate M Equals K to M1
4-12 (Ctrl Reg Bits 8-11)
4-35P1 7A A Reg Bits P-7
6-Gate A Reg to M1
4-24 7D W1 Reg Bit P-6
11-Gate W1 to M1
4-3 9E CD Sw Parity
4-6 9C Man Gate Sw ABCD to M1
4-3 7E (C Sw Bits 0-3)
4-3 8E (D Sw Bits 0-3)
Parity bit and bit 0 are set depending on which gate is active. Bit 1 is set to the condition of Ctrl Reg bit 9. Bits 2-6 are set to the condition of Ctrl Reg bits 10-14 respectively. Bit 7 is always set to 0 (off) condition.
P1 forced to 0, bits 0, 1, 2 Set to 11, 9, 10.
Bit 3 set to ALU A 4. Ctrl Reg bit 2, bit 4 to ALU A 5. Ctrl Reg bit 3. Bits 5,6, set to ALU A 6,7, respectively. Bit 7 is always set to 0(off) condition.
Note: If Gate Br Mask to M1 is not active bits 3-7 will be 0(off)
Force bits 0 & 4 to 1(on)
Force bits 1 & 7 to 0(off)
Set bits 2,3,5,6, to Ctrl Reg bits 8,9,10 & 11 respectively
Bit 7 is forced to 0 (off).
(P1) MC001 (0-7) MC061-101
M0 Assembler
Note 1
9-Gate M Equals K to M1
(48K or Ctrl Reg Bit 3)
M0 Parity for Unc Br
4-Gate Unc Rep to M
4-12 (Ctrl Reg Bits 2,3,4)
4-27P5 9B Storage Data Out Bit 5
4-12 (Ctrl Reg Bits 6,7)
4-24 7B W0 Reg Bits 0-4
8-Gate Br Mask to M
4-12 (Ctrl Reg Bits 12,13,14)
4-30 9D (LS Bus P 2-7)
5-Gate LS to M0
4-24 7B W0 Reg Bits P-7
10-Gate W0 to M0
4-3 6D Sw AB Parity
4-6 9B Man Gate Sw ABCD to M0
4-3 4E A Sw Bits 0-3
4-3 5E B Sw Bits 0-3
4-30 9D (LS Bus Bits 0, 1)
13-Gate LS Bits 0 and 1
*(Core Size 16, 24, 32, 48)
12-Force Ctrl Store Bits
Note: See bottom comment.
Parity forced to 0 (off).
See bottom comment
Bits 0 & 1 can be set to 1(on) or 0 (off) depending on these conditions.
(P0)MC001 (0-7)MC011-051
To M0 (P0-7) 4-21 2A
Core Size
Bits
16K Prog 0 1
24K Prog 1 0
32K Prog 1 0
48K Prog 1 1
Note 1:
Ctrl Reg Bit 3 = 0 (P0 set to 1) (M0, 6, and 7 set to 1)
Ctrl Reg Bit 3 = 1 (P0 set to 1) (M0, 6, and 7 set to 0)
4-32P1 2A First Cycle Storage Word
4-12 (Not) Ctrl Reg Bit 3
Ctrl Storage Access ..2D; 4-21 6C
MG021
To M1 (P1-7) 4-21 2C

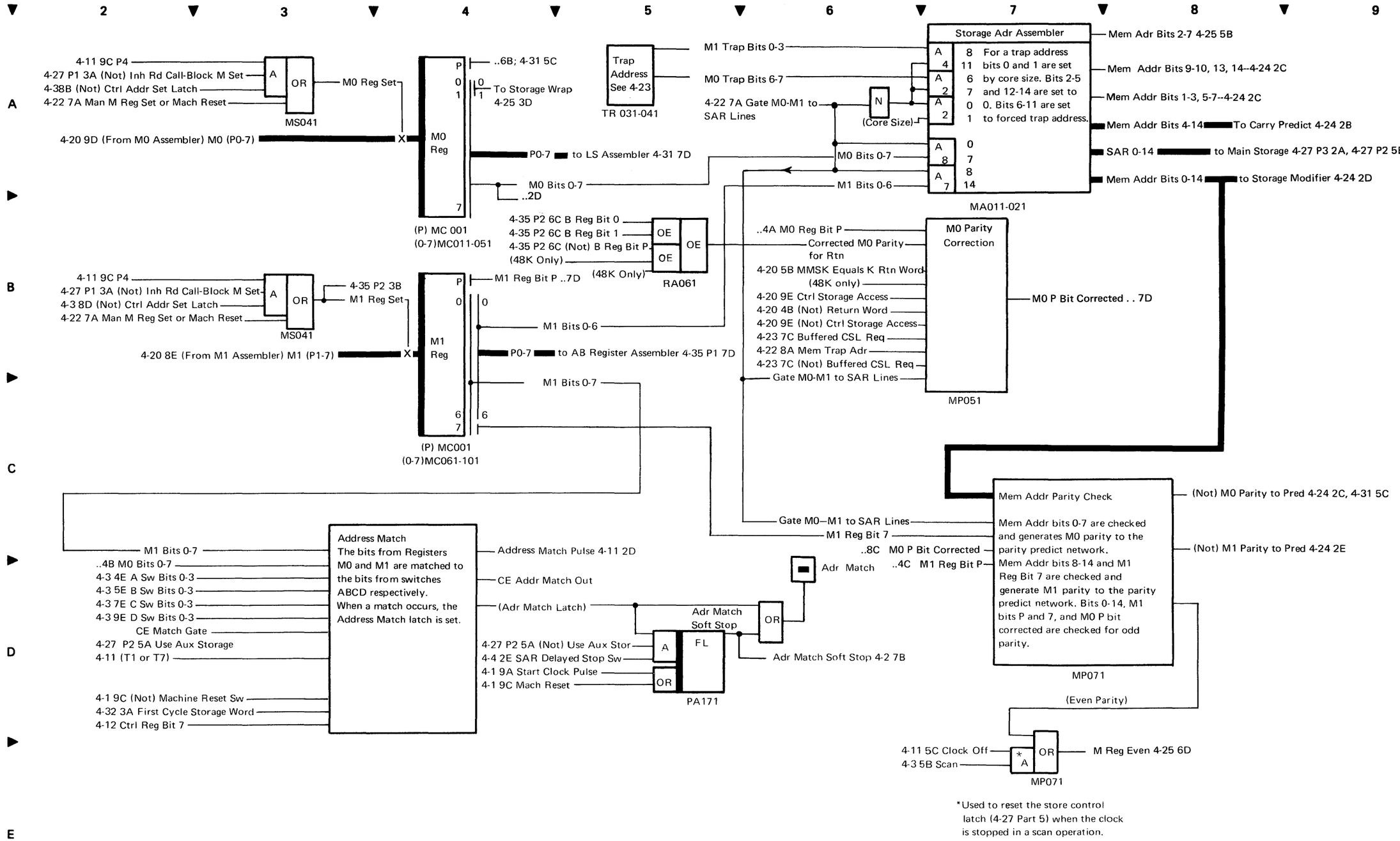
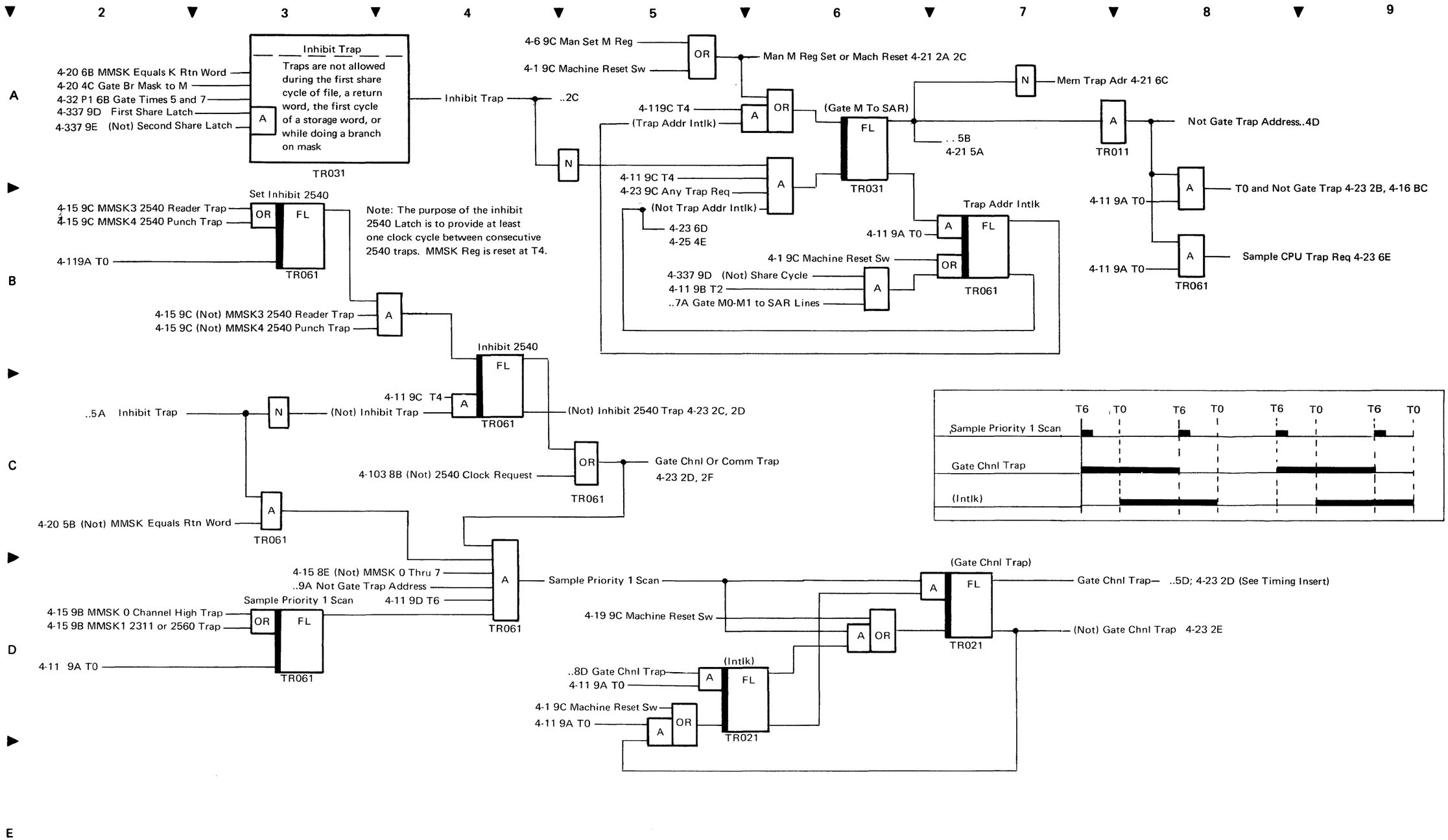

2
3
4
5
6
7
8
9
A
B
C
D
E
4-11 9C P4
4-27 P1 3A (Not) Inh Rd Call-Block M Set
4-38B (Not) Ctrl Addr Set Latch
4-22 7A Man M Reg Set or Mach Reset
A
OR
MS041
M0 Reg Set
4-20 9D (From M0 Assembler) M0 (P0-7)
X
P
0
1
7
M0 Reg
(P) MC 001
(0-7)MC011-051
..6B; 4-31 5C
0
1
To Storage Wrap 4-25 3D
P0-7 to LS Assembler 4-31 7D
M0 Bits 0-7
..2D
Trap Address See 4-23
TR 031-041
M1 Trap Bits 0-3
M0 Trap Bits 6-7
4-22 7A Gate M0-M1 to SAR Lines
N
(Core Size)
Storage Adr Assembler
A 4
A 2
A 2
A 8
A 7
8
11
6
7
0
1
0
7
8
14
For a trap address bits 0 and 1 are set by core size. Bits 2-5 and 12-14 are set to 0. Bits 6-11 are set to forced trap address.
M0 Bits 0-7
M1 Bits 0-6
MA011-021
Mem Adr Bits 2-7 4-25 5B
Mem Addr Bits 9-10, 13, 14--4-24 2C
Mem Addr Bits 1-3, 5-7--4-24 2C
Mem Addr Bits 4-14
To Carry Predict 4-24 2B
SAR 0-14
to Main Storage 4-27 P3 2A, 4-27 P2 5B
Mem Addr Bits 0-14
to Storage Modifier 4-24 2D
4-35 P2 6C B Reg Bit 0
4-35 P2 6C B Reg Bit 1
4-35 P2 6C (Not) B Reg Bit P
(48K Only)
OE
OE
(48K Only)
RA061
..4A M0 Reg Bit P
Corrected M0 Parity for Rtn
4-20 5B MMSK Equals K Rtn Word (48K only)
4-20 9E Ctrl Storage Access
4-20 4B (Not) Return Word
4-20 9E (Not) Ctrl Storage Access
4-23 7C Buffered CSL Req
4-22 8A Mem Trap Adr
4-23 7C (Not) Buffered CSL Req
Gate M0-M1 to SAR Lines
M0 Parity Correction
M0 P Bit Corrected . . 7D
MP051
4-11 9C P4
4-27 P1 3A (Not) Inh Rd Call-Block M Set
4-3 8D (Not) Ctrl Addr Set Latch
4-22 7A Man M Reg Set or Mach Reset
A
OR
MS041
4-35 P2 3B
M1 Reg Set
4-20 8E (From M1 Assembler) M1 (P1-7)
X
P
0
6
7
M1 Reg
(P) MC001
(0-7)MC061-101
M1 Reg Bit P ..7D
0
6
M1 Bits 0-6
P0-7 to AB Register Assembler 4-35 P1 7D
M1 Bits 0-7
Mem Addr Parity Check
Mem Addr bits 0-7 are checked and generates M0 parity to the parity predict network. Mem Addr bits 8-14 and M1 Reg Bit 7 are checked and generate M1 parity to the parity predict network. Bits 0-14, M1 bits P and 7, and M0 P bit corrected are checked for odd parity.
MP071
(Not) M0 Parity to Pred 4-24 2C, 4-31 5C
(Not) M1 Parity to Pred 4-24 2E
Gate M0—M1 to SAR Lines
M1 Reg Bit 7
..8C M0 P Bit Corrected
..4C M1 Reg Bit P
Address Match
The bits from Registers M0 and M1 are matched to the bits from switches ABCD respectively. When a match occurs, the Address Match latch is set.
M1 Bits 0-7
..4B M0 Bits 0-7
4-3 4E A Sw Bits 0-3
4-3 5E B Sw Bits 0-3
4-3 7E C Sw Bits 0-3
4-3 9E D Sw Bits 0-3
CE Match Gate
4-27 P2 5A Use Aux Storage
4-11 (T1 or T7)
4-1 9C (Not) Machine Reset Sw
4-32 3A First Cycle Storage Word
4-12 Ctrl Reg Bit 7
Address Match Pulse 4-11 2D
CE Addr Match Out
(Adr Match Latch)
Adr Match
Adr Match Soft Stop
OR
A
FL
OR
PA171
4-27 P2 5A (Not) Use Aux Stor
4-4 2E SAR Delayed Stop Sw
4-1 9A Start Clock Pulse
4-1 9C Mach Reset
Adr Match Soft Stop 4-2 7B
(Even Parity)
4-11 5C Clock Off
4-3 5B Scan
*
A
OR
MP071
M Reg Even 4-25 6D
*Used to reset the store control latch (4-27 Part 5) when the clock is stopped in a scan operation.

Diagram 4-22. Trap Controls



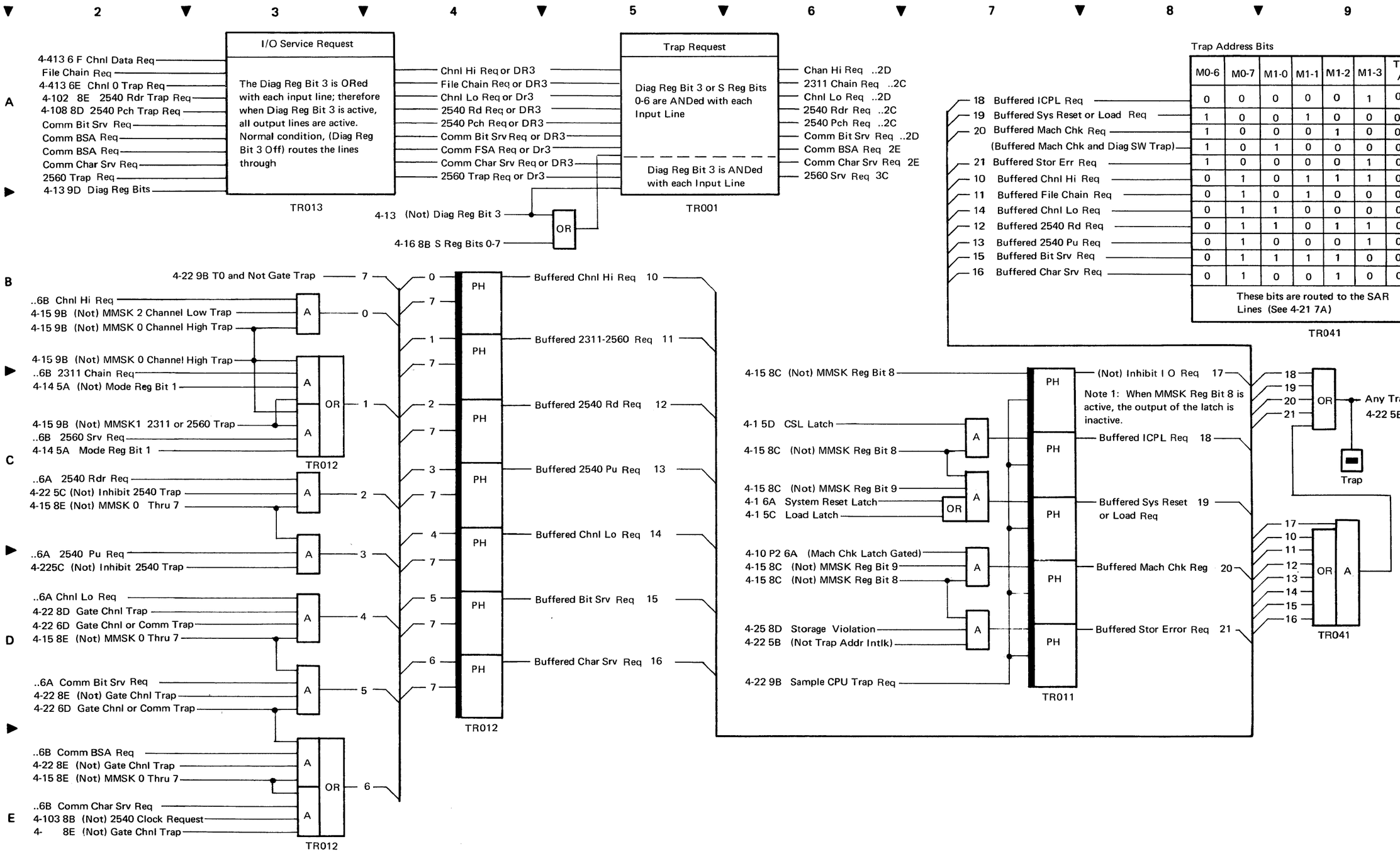
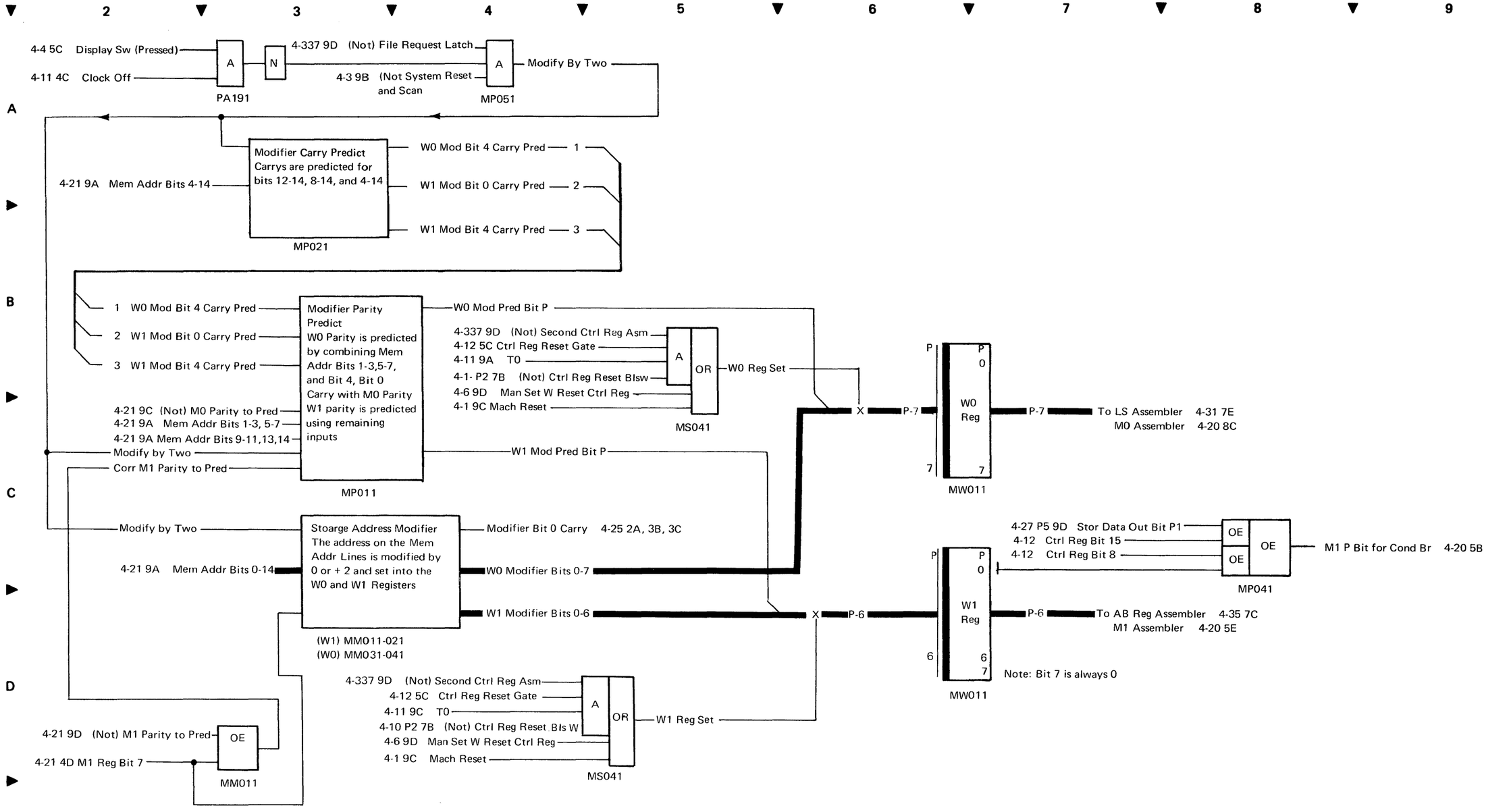
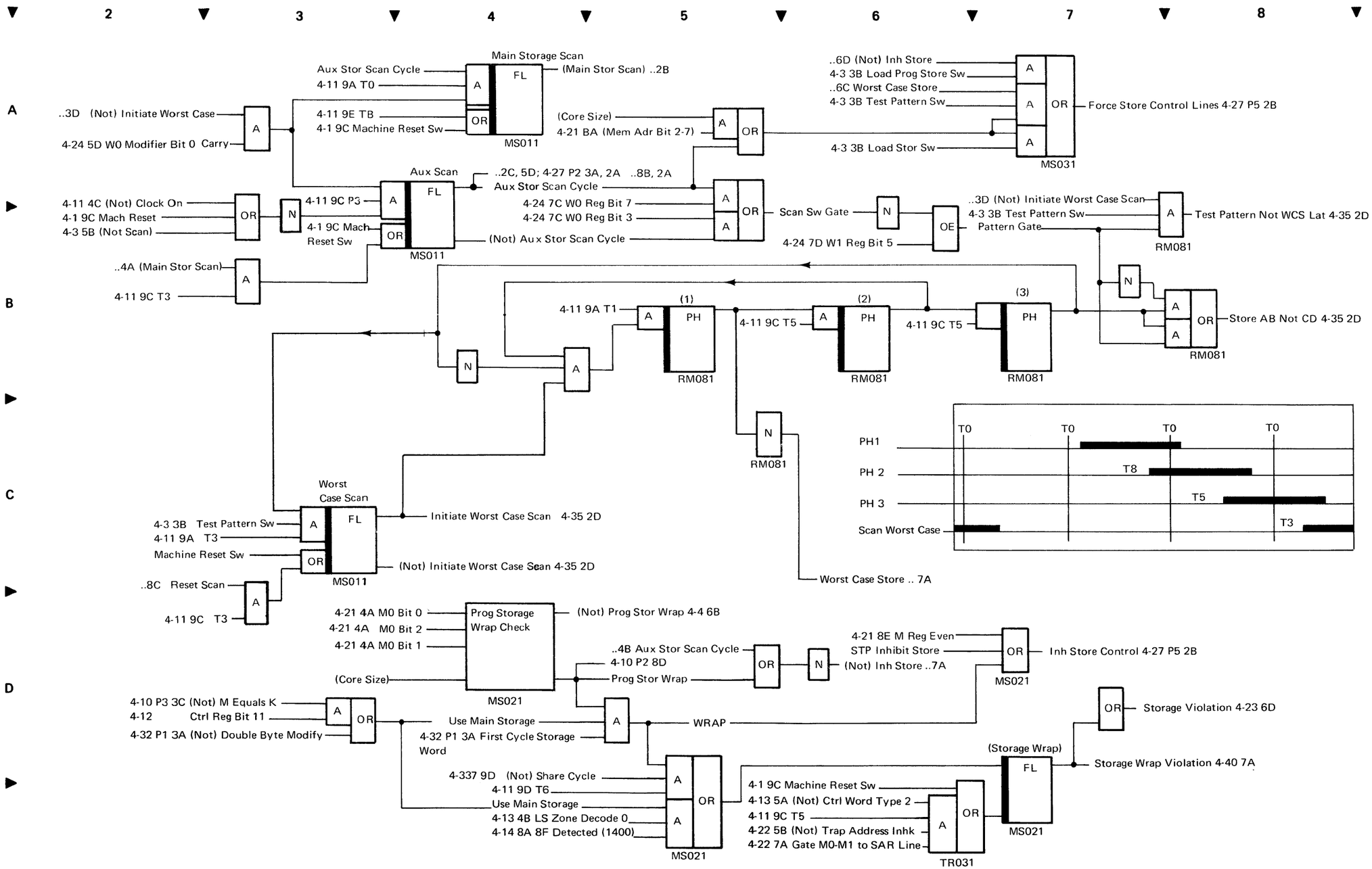
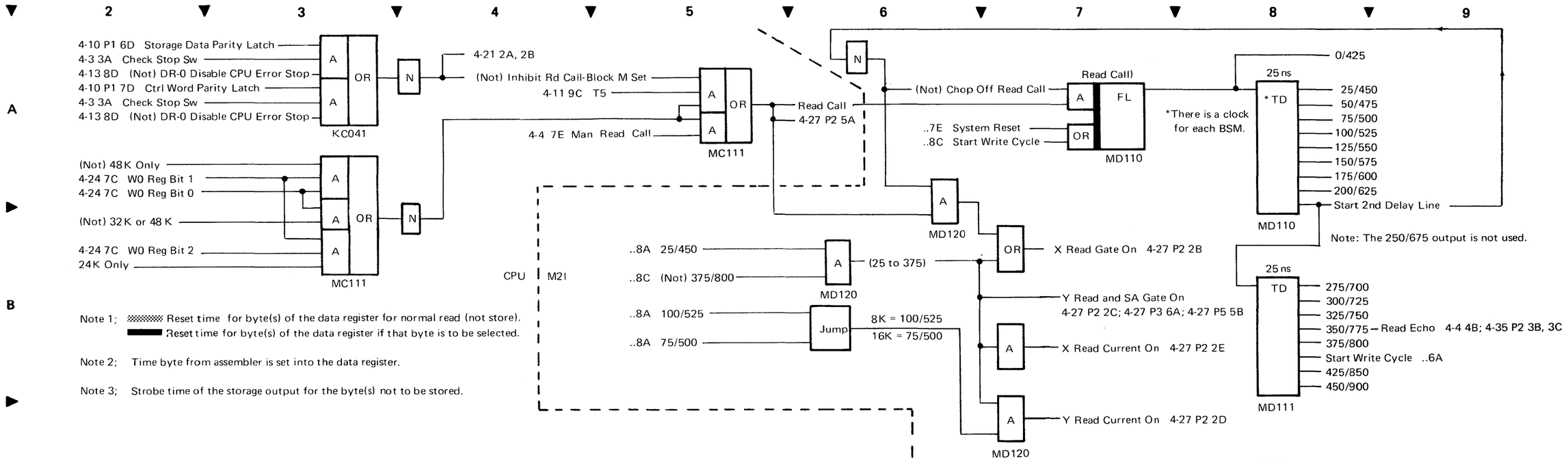
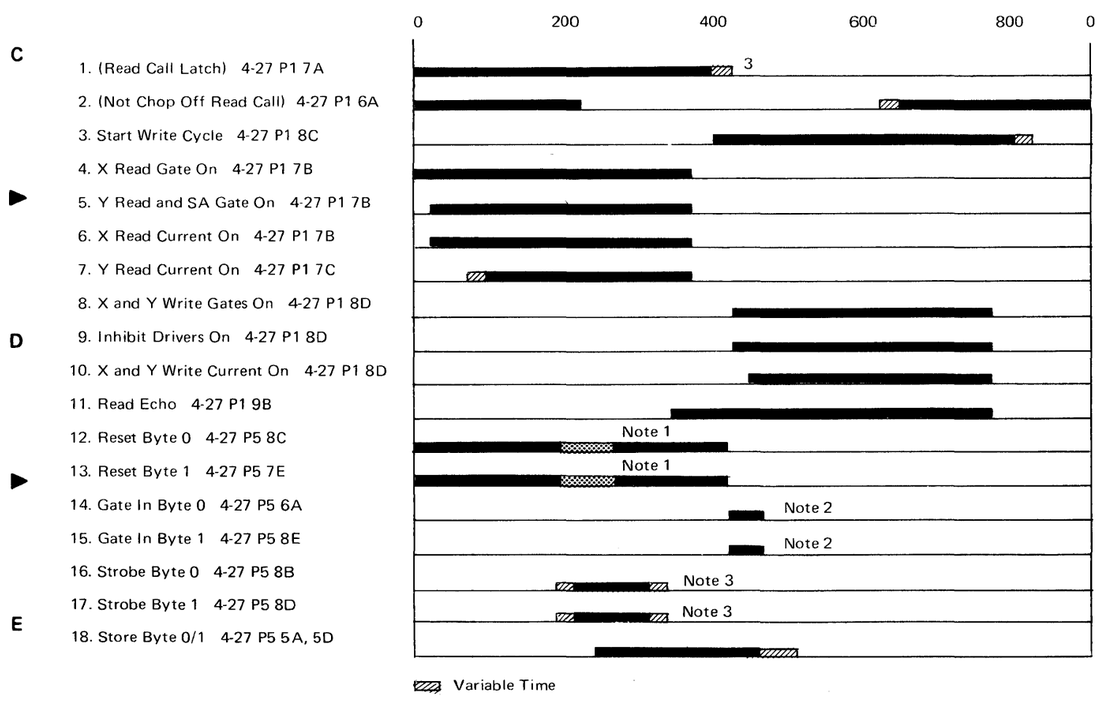

2
3
4
5
6
7
8
9
A
B
C
D
E
I/O Service Request
4-413 6 F Chnl Data Req
File Chain Req
4-413 6E Chnl 0 Trap Req
4-102 8E 2540 Rdr Trap Req
4-108 8D 2540 Pch Trap Req
Comm Bit Srv Req
Comm BSA Req
Comm BSA Req
Comm Char Srv Req
2560 Trap Req
4-13 9D Diag Reg Bits
The Diag Reg Bit 3 is ORed with each input line; therefore when Diag Reg Bit 3 is active, all output lines are active. Normal condition, (Diag Reg Bit 3 Off) routes the lines through
TR013
Chnl Hi Req or DR3
File Chain Req or DR3
Chnl Lo Req or Dr3
2540 Rd Req or DR3
2540 Pch Req or DR3
Comm Bit Srv Req or DR3
Comm FSA Req or Dr3
Comm Char Srv Req or DR3
2560 Trap Req or Dr3
4-13 (Not) Diag Reg Bit 3
4-16 8B S Reg Bits 0-7
OR
Trap Request
Diag Reg Bit 3 or S Reg Bits 0-6 are ANDed with each Input Line
Diag Reg Bit 3 is ANDed with each Input Line
TR001
Chan Hi Req ..2D
2311 Chain Req ..2C
Chnl Lo Req ..2D
2540 Rdr Req ..2C
2540 Pch Req ..2C
Comm Bit Srv Req ..2D
Comm BSA Req 2E
Comm Char Srv Req 2E
2560 Srv Req 3C
Trap Address Bits
M0-6 M0-7 M1-0 M1-1 M1-2 M1-3 Trap Adr
18 Buffered ICPL Req 0 0 0 0 0 1 0010
19 Buffered Sys Reset or Load Req 1 0 0 1 0 0 0240
20 Buffered Mach Chk Req 1 0 0 0 1 0 0220
(Buffered Mach Chk and Diag SW Trap) 1 0 1 0 0 0 0280
21 Buffered Stor Err Req 1 0 0 0 0 1 0210
10 Buffered Chnl Hi Req 0 1 0 1 1 1 0170
11 Buffered File Chain Req 0 1 0 1 0 0 0140
14 Buffered Chnl Lo Req 0 1 1 0 0 0 0180
12 Buffered 2540 Rd Req 0 1 1 0 1 1 01B0
13 Buffered 2540 Pu Req 0 1 0 0 0 1 0110
15 Buffered Bit Srv Req 0 1 1 1 1 0 01E0
16 Buffered Char Srv Req 0 1 0 0 1 0 0120
These bits are routed to the SAR Lines (See 4-21 7A)
TR041
4-22 9B T0 and Not Gate Trap
..6B Chnl Hi Req
4-15 9B (Not) MMSK 2 Channel Low Trap
4-15 9B (Not) MMSK 0 Channel High Trap
4-15 9B (Not) MMSK 0 Channel High Trap
..6B 2311 Chain Req
4-14 5A (Not) Mode Reg Bit 1
4-15 9B (Not) MMSK1 2311 or 2560 Trap
..6B 2560 Srv Req
4-14 5A Mode Reg Bit 1
TR012
..6A 2540 Rdr Req
4-22 5C (Not) Inhibit 2540 Trap
4-15 8E (Not) MMSK 0 Thru 7
..6A 2540 Pu Req
4-225C (Not) Inhibit 2540 Trap
..6A Chnl Lo Req
4-22 8D Gate Chnl Trap
4-22 6D Gate Chnl or Comm Trap
4-15 8E (Not) MMSK 0 Thru 7
..6A Comm Bit Srv Req
4-22 8E (Not) Gate Chnl Trap
4-22 6D Gate Chnl or Comm Trap
..6B Comm BSA Req
4-22 8E (Not) Gate Chnl Trap
4-15 8E (Not) MMSK 0 Thru 7
..6B Comm Char Srv Req
4-103 8B (Not) 2540 Clock Request
4- 8E (Not) Gate Chnl Trap
TR012
PH
Buffered Chnl Hi Req 10
Buffered 2311-2560 Req 11
Buffered 2540 Rd Req 12
Buffered 2540 Pu Req 13
Buffered Chnl Lo Req 14
Buffered Bit Srv Req 15
Buffered Char Srv Req 16
TR012
4-15 8C (Not) MMSK Reg Bit 8
4-1 5D CSL Latch
4-15 8C (Not) MMSK Reg Bit 8
4-15 8C (Not) MMSK Reg Bit 9
4-1 6A System Reset Latch
4-1 5C Load Latch
4-10 P2 6A (Mach Chk Latch Gated)
4-15 8C (Not) MMSK Reg Bit 9
4-15 8C (Not) MMSK Reg Bit 8
4-25 8D Storage Violation
4-22 5B (Not Trap Addr Intlk)
4-22 9B Sample CPU Trap Req
(Not) Inhibit I O Req 17
Note 1: When MMSK Reg Bit 8 is active, the output of the latch is inactive.
Buffered ICPL Req 18
Buffered Sys Reset or Load Req 19
Buffered Mach Chk Reg 20
Buffered Stor Error Req 21
TR011
Any Trap Req 4-22 5B
Trap
TR041

Diagram 4-24. Storage Address Modifier, W0, W1 Register




2
3
4
5
6
7
8
9
A
B
C
D
E
Main Storage Scan
Aux Stor Scan Cycle
4-11 9A T0
4-11 9E TB
4-1 9C Machine Reset Sw
(Main Stor Scan) ..2B
MS011
..3D (Not) Initiate Worst Case
4-24 5D W0 Modifier Bit 0 Carry
Aux Scan
..2C, 5D; 4-27 P2 3A, 2A ..8B, 2A
Aux Stor Scan Cycle
4-11 4C (Not) Clock On
4-1 9C Mach Reset
4-3 5B (Not Scan)
4-11 9C P3
4-1 9C Mach Reset Sw
(Not) Aux Stor Scan Cycle
..4A (Main Stor Scan)
4-11 9C T3
(Core Size)
4-21 BA (Mem Adr Bit 2-7)
4-24 7C W0 Reg Bit 7
4-24 7C W0 Reg Bit 3
..6D (Not) Inh Store
4-3 3B Load Prog Store Sw
..6C Worst Case Store
4-3 3B Test Pattern Sw
4-3 3B Load Stor Sw
MS031
Force Store Control Lines 4-27 P5 2B
Scan Sw Gate
4-24 7D W1 Reg Bit 5
OE
..3D (Not) Initiate Worst Case Scan
4-3 3B Test Pattern Sw
Pattern Gate
RM081
Test Pattern Not WCS Lat 4-35 2D
4-11 9A T1
4-11 9C T5
4-11 9C T5
(1)
(2)
(3)
PH
Store AB Not CD 4-35 2D
Worst Case Scan
4-3 3B Test Pattern Sw
4-11 9A T3
Machine Reset Sw
..8C Reset Scan
4-11 9C T3
Initiate Worst Case Scan 4-35 2D
(Not) Initiate Worst Case Scan 4-35 2D
Worst Case Store .. 7A
PH1
PH 2
PH 3
Scan Worst Case
T0
T8
T5
T3
4-21 4A M0 Bit 0
4-21 4A M0 Bit 2
4-21 4A M0 Bit 1
(Core Size)
Prog Storage Wrap Check
(Not) Prog Stor Wrap 4-4 6B
MS021
..4B Aux Stor Scan Cycle
4-10 P2 8D
Prog Stor Wrap
(Not) Inh Store ..7A
4-21 8E M Reg Even
STP Inhibit Store
Inh Store Control 4-27 P5 2B
4-10 P3 3C (Not) M Equals K
4-12 Ctrl Reg Bit 11
4-32 P1 3A (Not) Double Byte Modify
Use Main Storage
4-32 P1 3A First Cycle Storage Word
WRAP
4-337 9D (Not) Share Cycle
4-11 9D T6
Use Main Storage
4-13 4B LS Zone Decode 0
4-14 8A 8F Detected (1400)
4-1 9C Machine Reset Sw
4-13 5A (Not) Ctrl Word Type 2
4-11 9C T5
4-22 5B (Not) Trap Address Inhk
4-22 7A Gate M0-M1 to SAR Line
TR031
(Storage Wrap)
Storage Violation 4-23 6D
Storage Wrap Violation 4-40 7A


2
3
4
5
6
7
8
9
A
B
4-10 P1 6D Storage Data Parity Latch
4-3 3A Check Stop Sw
4-13 8D (Not) DR-0 Disable CPU Error Stop
4-10 P1 7D Ctrl Word Parity Latch
4-3 3A Check Stop Sw
4-13 8D (Not) DR-0 Disable CPU Error Stop
KC041
4-21 2A, 2B
(Not) Inhibit Rd Call-Block M Set
4-11 9C T5
4-4 7E Man Read Call
MC111
Read Call
4-27 P2 5A
(Not) 48K Only
4-24 7C W0 Reg Bit 1
4-24 7C W0 Reg Bit 0
(Not) 32K or 48 K
4-24 7C W0 Reg Bit 2
24K Only
MC111
(Not) Chop Off Read Call
..7E System Reset
..8C Start Write Cycle
Read Call)
MD110
*There is a clock for each BSM.
0/425
25 ns
*TD
25/450
50/475
75/500
100/525
125/550
150/575
175/600
200/625
Start 2nd Delay Line
MD110
Note: The 250/675 output is not used.
MD120
..8A 25/450
..8C (Not) 375/800
(25 to 375)
MD120
..8A 100/525
..8A 75/500
Jump
8K = 100/525
16K = 75/500
CPU M2I
X Read Gate On 4-27 P2 2B
Y Read and SA Gate On
4-27 P2 2C; 4-27 P3 6A; 4-27 P5 5B
X Read Current On 4-27 P2 2E
Y Read Current On 4-27 P2 2D
MD120
25 ns
TD
275/700
300/725
325/750
350/775 – Read Echo 4-4 4B; 4-35 P2 3B, 3C
375/800
Start Write Cycle ..6A
425/850
450/900
MD111
Note 1; Reset time for byte(s) of the data register for normal read (not store).
Reset time for byte(s) of the data register if that byte is to be selected.
Note 2; Time byte from assembler is set into the data register.
Note 3; Strobe time of the storage output for the byte(s) not to be stored.


C
D
E
0
200
400
600
800
0
1. (Read Call Latch) 4-27 P1 7A
2. (Not Chop Off Read Call) 4-27 P1 6A
3. Start Write Cycle 4-27 P1 8C
4. X Read Gate On 4-27 P1 7B
5. Y Read and SA Gate On 4-27 P1 7B
6. X Read Current On 4-27 P1 7B
7. Y Read Current On 4-27 P1 7C
8. X and Y Write Gates On 4-27 P1 8D
9. Inhibit Drivers On 4-27 P1 8D
10. X and Y Write Current On 4-27 P1 8D
11. Read Echo 4-27 P1 9B
12. Reset Byte 0 4-27 P5 8C
13. Reset Byte 1 4-27 P5 7E
14. Gate In Byte 0 4-27 P5 6A
15. Gate In Byte 1 4-27 P5 8E
16. Strobe Byte 0 4-27 P5 8B
17. Strobe Byte 1 4-27 P5 8D
18. Store Byte 0/1 4-27 P5 5A, 5D
3
Note 1
Note 1
Note 2
Note 2
Note 3
Note 3
Variable Time

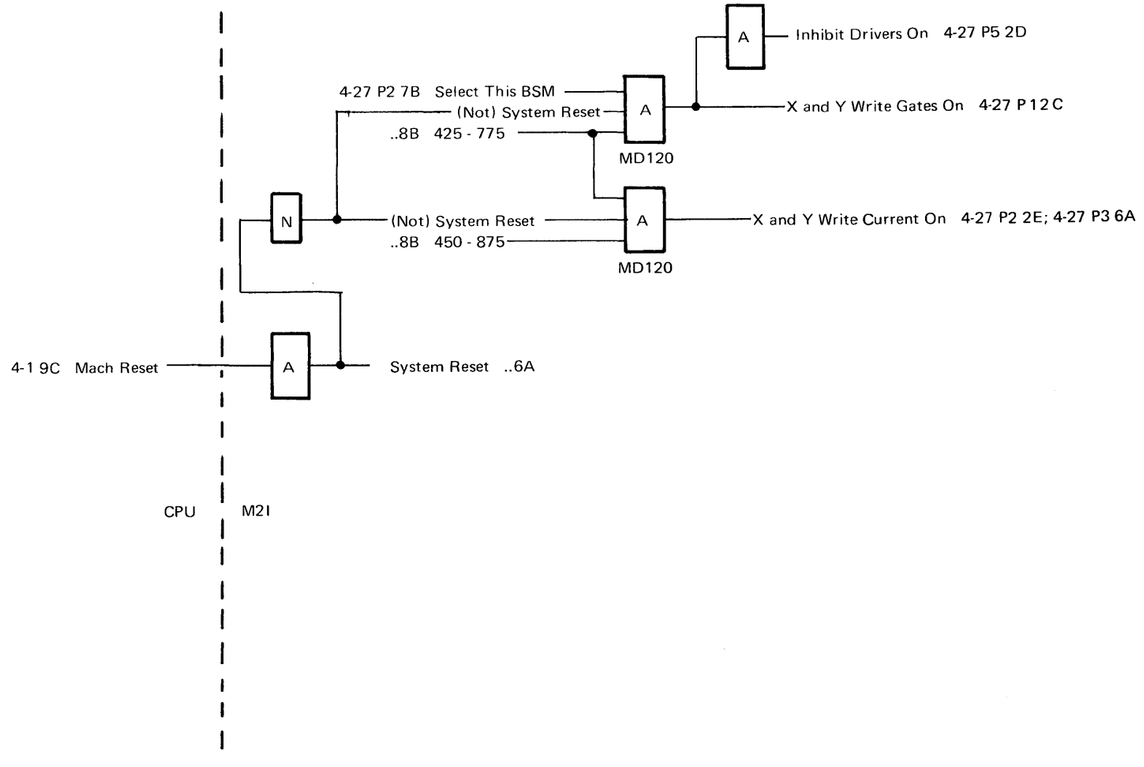
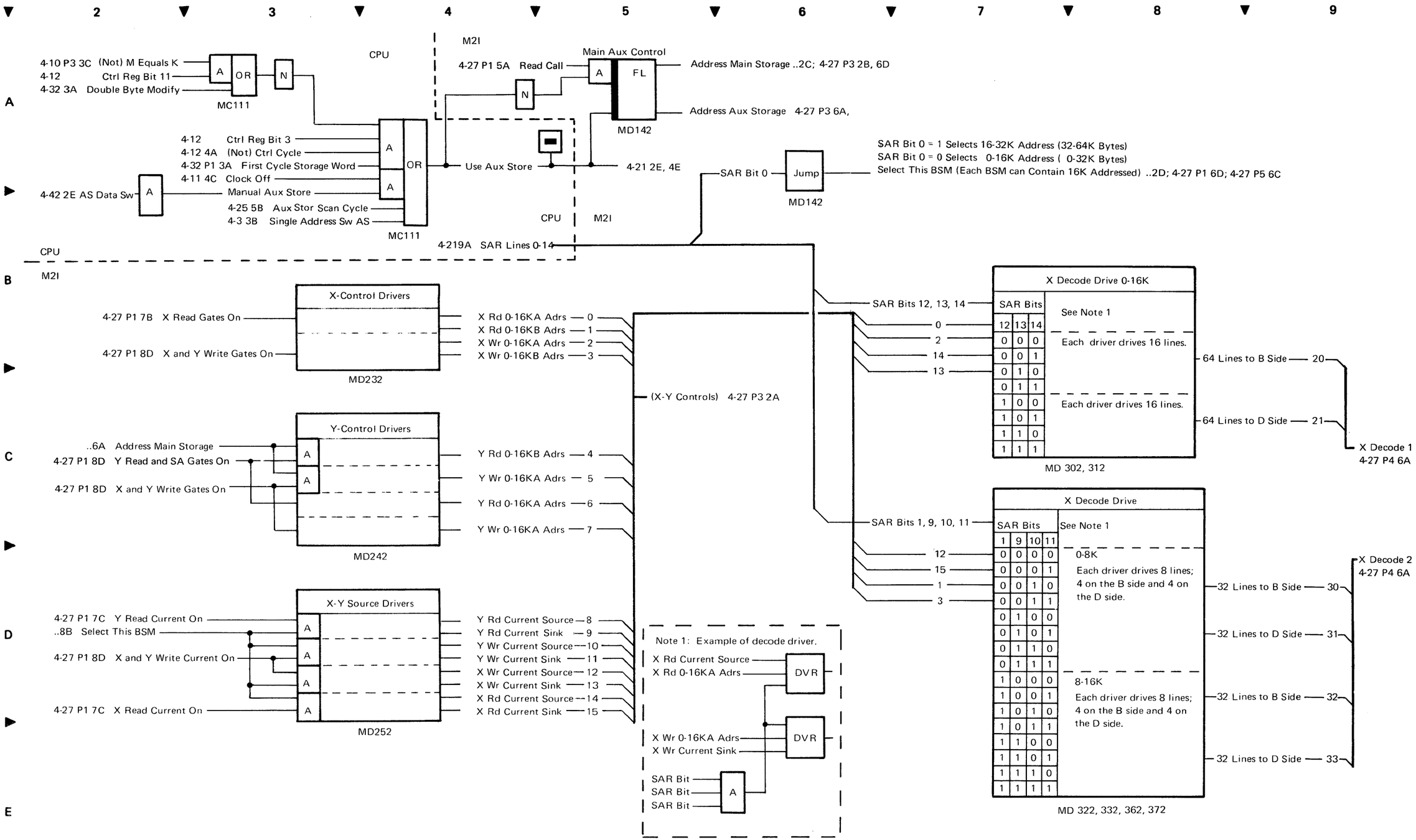

A
Inhibit Drivers On 4-27 P5 2D
4-27 P2 7B Select This BSM
(Not) System Reset
..8B 425 - 775
A
X and Y Write Gates On 4-27 P12C
MD120
N
(Not) System Reset
..8B 450 - 875
A
X and Y Write Current On 4-27 P2 2E; 4-27 P3 6A
MD120
4-1 9C Mach Reset
A
System Reset ..6A
CPU M2I

Diagram 4-27. Main and Aux Storage (X Decode) (Part 2 of 5)



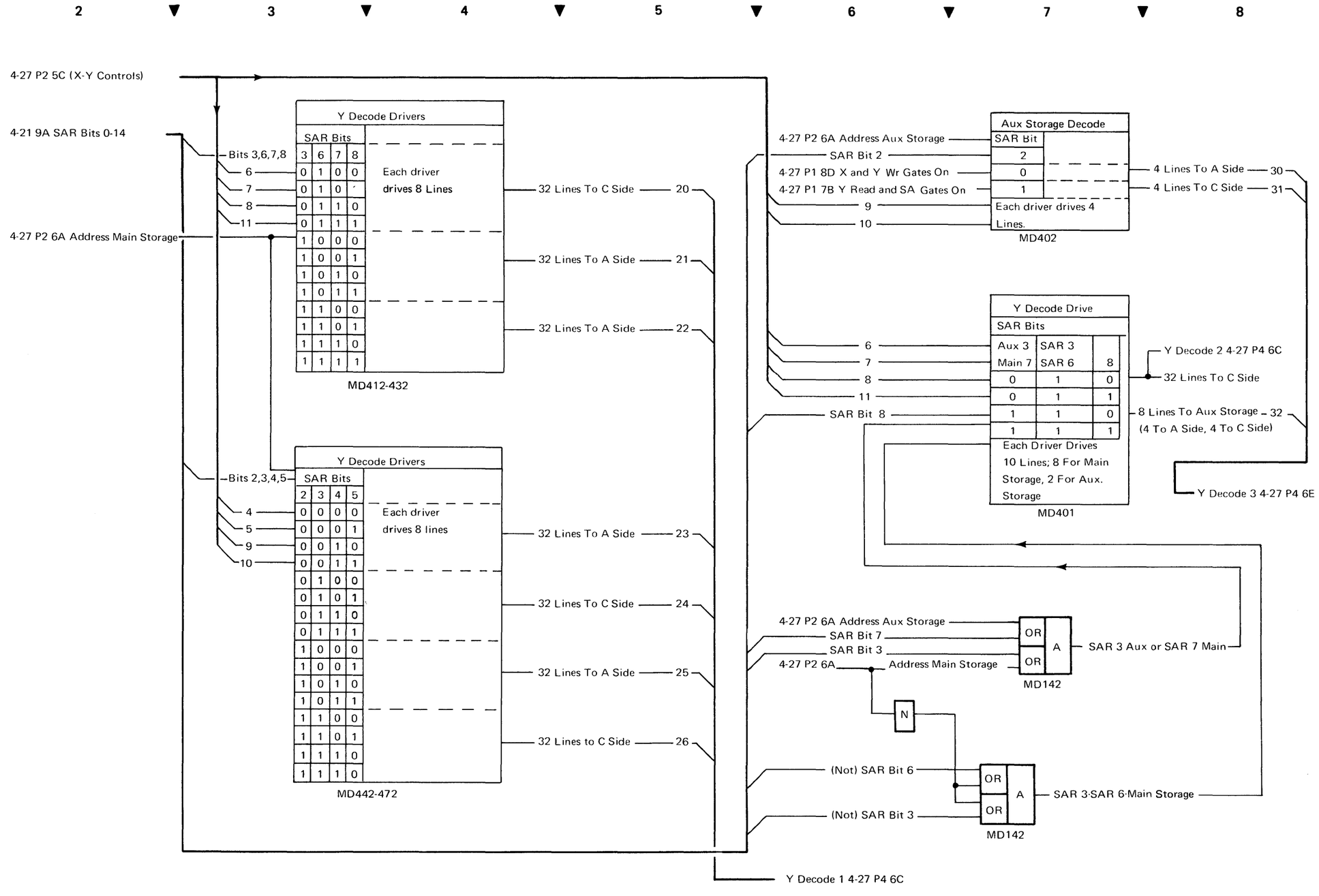
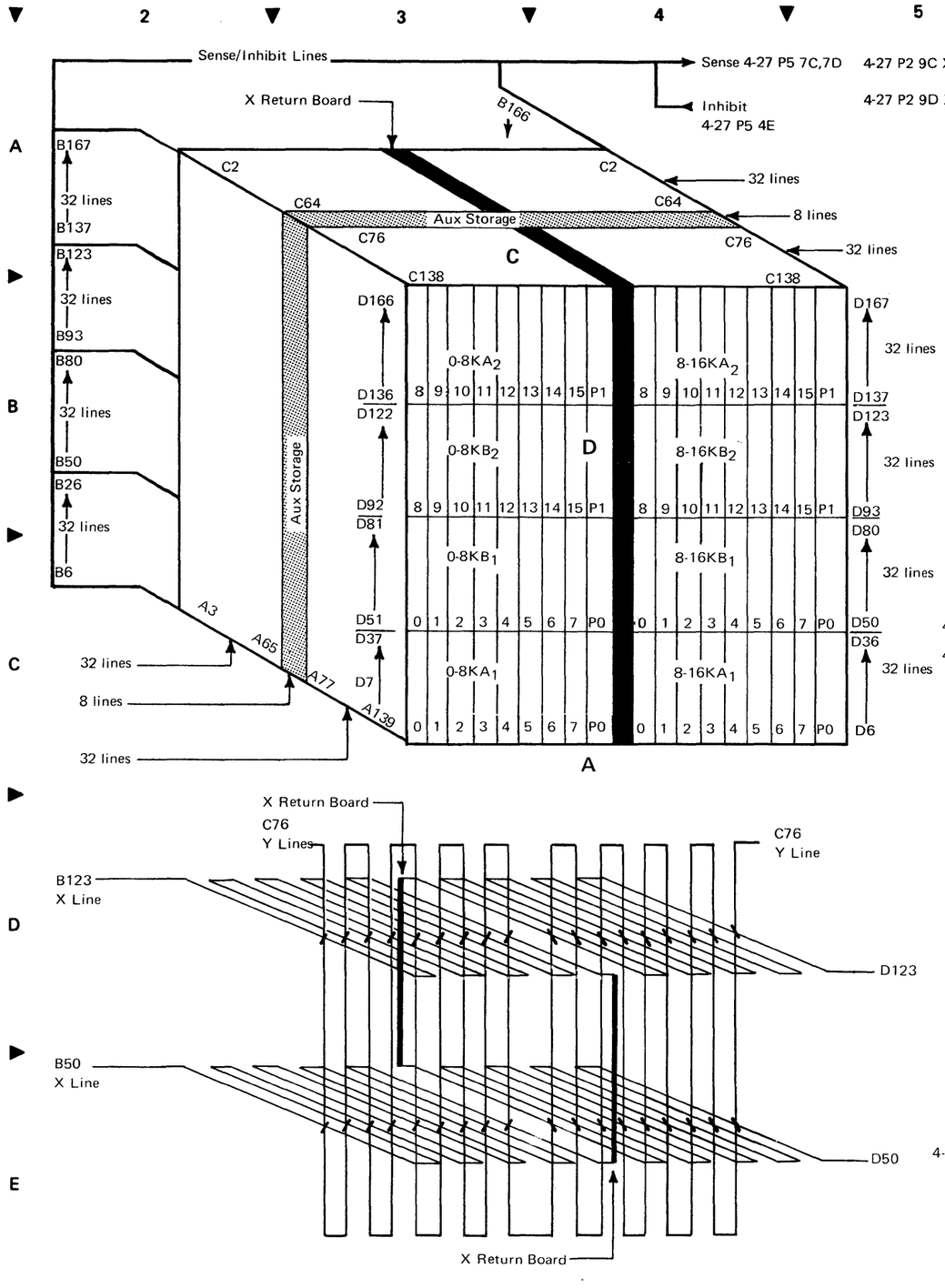

2
3
4
5
6
7
8
9
A
B
C
D
E
4-27 P2 5C (X-Y Controls)
4-21 9A SAR Bits 0-14
4-27 P2 6A Address Main Storage
Y Decode Drivers
SAR Bits
3 6 7 8
Bits 3,6,7,8
6
7
8
11
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1
Each driver drives 8 Lines
32 Lines To C Side 20
32 Lines To A Side 21
32 Lines To A Side 22
MD412-432
Y Decode Drivers
SAR Bits
2 3 4 5
Bits 2,3,4,5
4
5
9
10
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 0
Each driver drives 8 lines
32 Lines To A Side 23
32 Lines To C Side 24
32 Lines To A Side 25
32 Lines to C Side 26
MD442-472
4-27 P2 6A Address Aux Storage
SAR Bit 2
4-27 P1 8D X and Y Wr Gates On
4-27 P1 7B Y Read and SA Gates On
9
10
Aux Storage Decode
SAR Bit
2
0
1
Each driver drives 4 Lines.
4 Lines To A Side 30
4 Lines To C Side 31
MD402
6
7
8
11
SAR Bit 8
Y Decode Drive
SAR Bits
Aux 3 Main 7
SAR 3 SAR 6
8
0 1 0
0 1 1
1 1 0
1 1 1
Each Driver Drives 10 Lines; 8 For Main Storage, 2 For Aux. Storage
Y Decode 2 4-27 P4 6C
32 Lines To C Side
8 Lines To Aux Storage 32
(4 To A Side, 4 To C Side)
Y Decode 3 4-27 P4 6E
MD401
4-27 P2 6A Address Aux Storage
SAR Bit 7
SAR Bit 3
4-27 P2 6A
Address Main Storage
OR
OR
A
SAR 3 Aux or SAR 7 Main
MD142
N
(Not) SAR Bit 6
(Not) SAR Bit 3
OR
OR
A
SAR 3·SAR 6·Main Storage
MD142
Y Decode 1 4-27 P4 6C

Diagram 4-27. Main and Aux Storage (Core) (Part 4 of 5)



Main And Aux. Storage	X Lines Decode Pin Entry and Exit							
SAR Bits	SAR Bit 12 13 14							
1 9 10 11	000	001	010	011	100	101	110	111
0 0 0 0	6-167	50-123	8-165	52-121	7-166	51-122	9-164	53-120
0 0 0 1	10-163	54-119	12-161	56-117	11-162	55-118	13-160	57-116
0 0 1 0	14-159	58-115	16-157	60-113	15-158	59-114	17-156	61-112
0 0 1 1	18-155	62-111	20-153	64-109	19-154	63-110	21-152	65-108
0 1 0 0	22-151	66-107	24-149	68-105	23-150	67-106	25-148	69-104
0 1 0 1	26-147	70-103	28-145	72-101	27-146	71-102	29-144	73-100
0 1 1 0	30-143	74- 99	32-141	76- 97	31-142	75- 98	34-140	77- 96
0 1 1 1	34-139	78- 95	36-137	80- 93	35-138	79- 94	37-136	81- 92
1 0 0 0	7-166	51-122	9-164	53-120	6-167	50-123	8-165	52-121
1 0 0 1	11-162	55-118	13-160	57-116	10-163	54-119	12-161	56-117
1 0 1 0	15-158	59-114	17-156	61-112	14-159	58-115	16-157	60-113
1 0 1 1	19-154	63-110	21-152	65-108	18-155	62-111	20-153	64-109
1 1 0 0	23-150	67-106	25-148	69-104	22-151	66-107	24-149	68-105
1 1 0 1	27-146	71-102	29-144	73-100	26-147	70-103	28-145	72-101
1 1 1 0	31-142	75- 98	34-140	77- 96	30-143	74- 99	32-141	76- 97
1 1 1 1	35-138	79- 94	37-136	81- 92	34-139	78- 95	36-137	80- 93
	Side B				Side D			

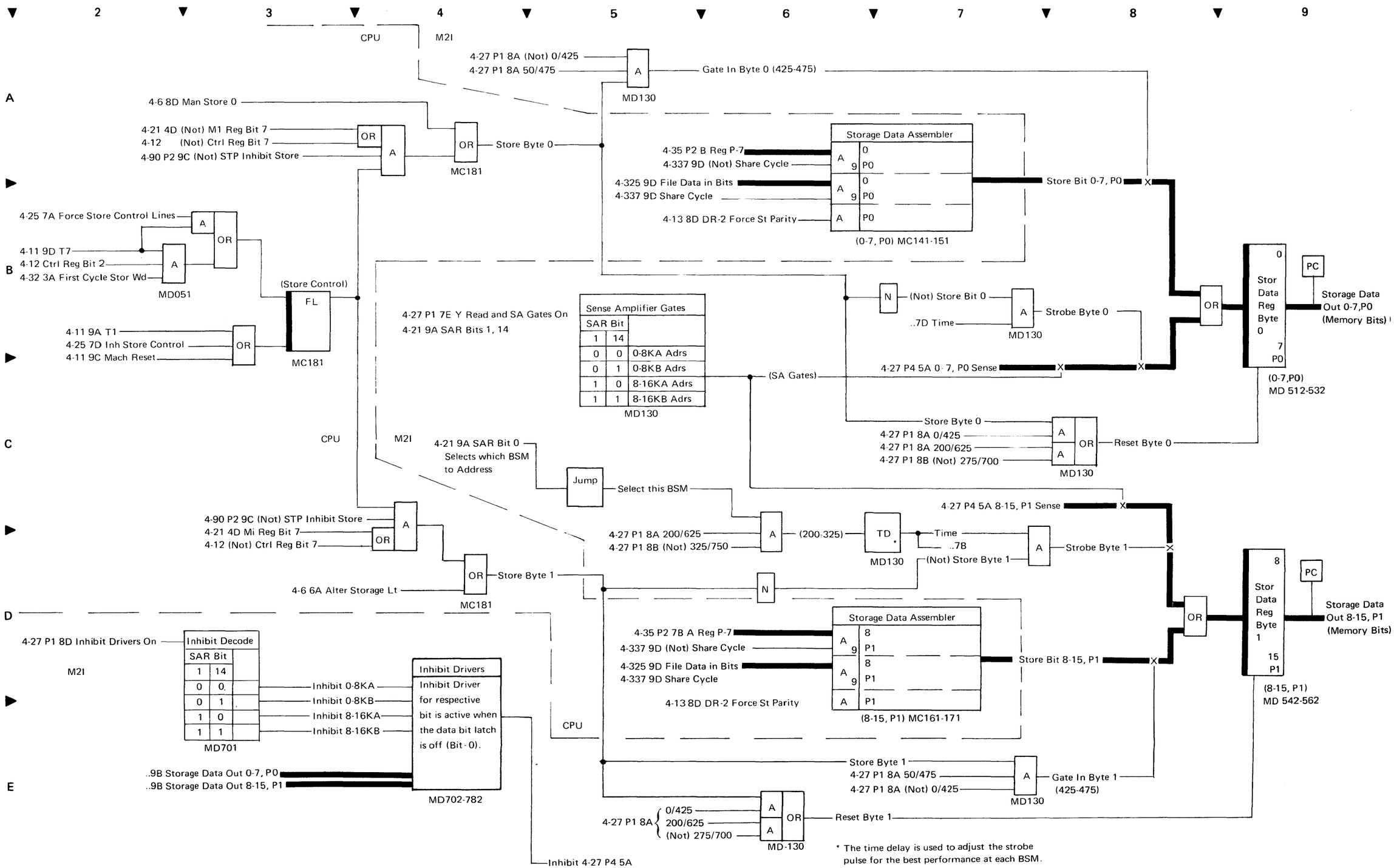
4-27 P3 6E Y Decode 1
4-27 P3 8B Y Decode 2

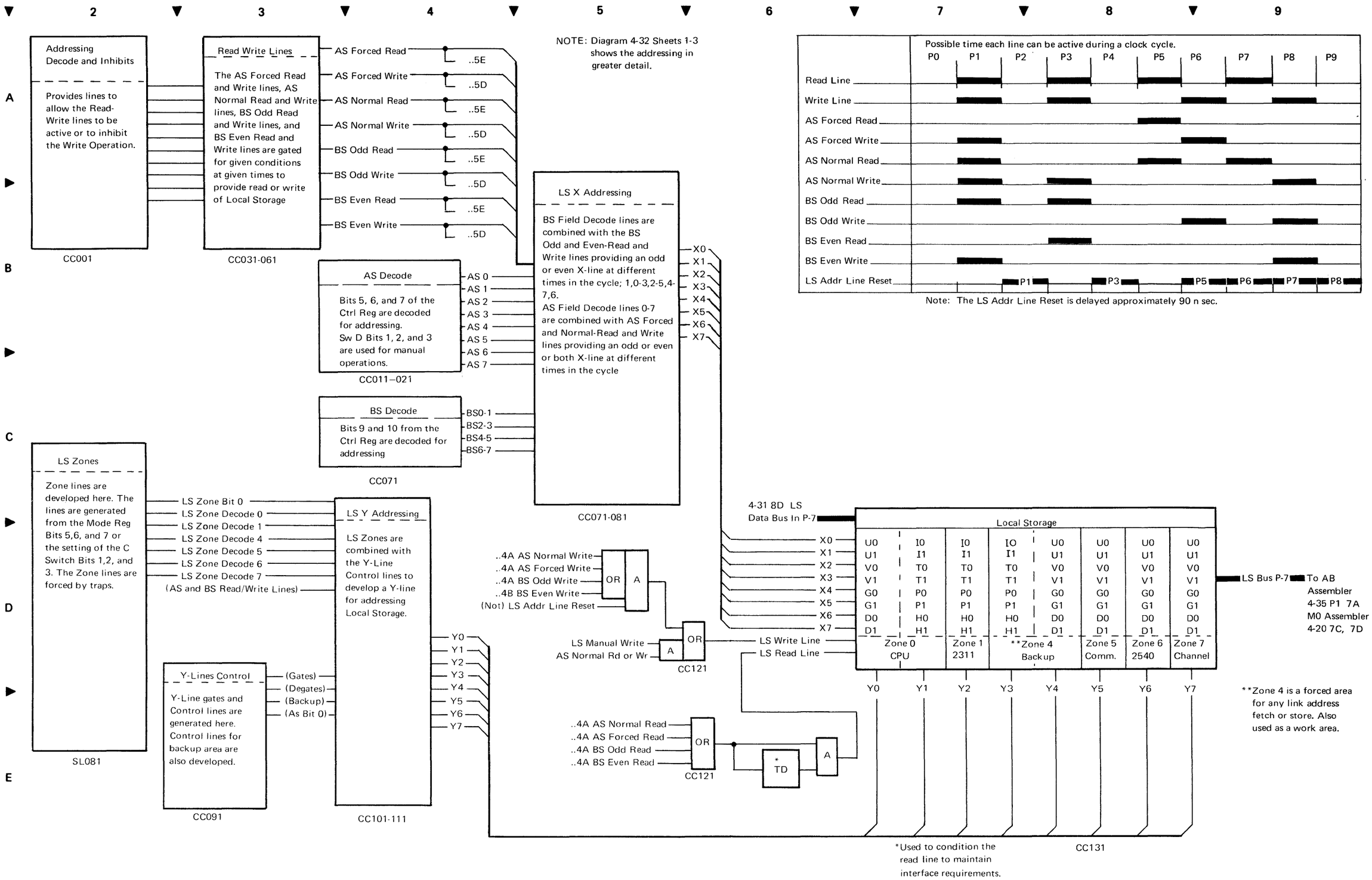
Main Storage	Y Lines Decode Pin Entry and Exit								
SAR Bits	SAR Bits 6, 7, 8								
2 3 4 5	000	001	010	011	100	101	110	111	Side
0 0 0 0	2	34	76	108	4	36	78	110	
0 0 0 1	6	38	80	112	8	40	82	114	C
0 0 1 0	10	42	84	116	12	44	86	118	
0 0 1 1	14	46	88	120	16	48	90	122	
0 1 0 0	3	35	77	109	5	37	79	111	
0 1 0 1	7	39	81	113	9	41	33	115	
0 1 1 0	11	43	85	117	13	45	87	119	A
0 1 1 1	15	47	89	121	17	49	91	123	
1 0 0 0	18	50	92	124	20	52	94	126	
1 0 0 1	22	54	96	128	24	56	98	130	
1 0 1 0	26	58	100	132	28	60	102	134	C
1 0 1 1	30	62	104	136	32	64	106	138	
1 1 0 0	19	51	93	125	21	53	95	127	
1 1 0 1	23	55	97	129	25	57	99	131	
1 1 1 0	27	59	101	133	29	61	103	135	A
1 1 1 1	31	63	105	137	33	65	107	139	

4-27 P3 9B Y Decode 3

Aux Storage Y Lines Decode Pin Entry and Exit					
SAR Bit	SAR Bit 3,8				Side
2	00	01	10	11	
0	66	68	72	74	C
1	67	69	73	75	A

Note: Shown on this page is the layout for one 16K half word BSM. 8K of addresses (16K bytes) for program storage require 1 BSM; any thing greater up to 48K (bytes) require a second BSM which has the same layout.


2
3
4
5
6
7
8
9
A
B
C
D
E
CPU
M2I
4-27 P1 8A (Not) 0/425
4-27 P1 8A 50/475
A
MD130
Gate In Byte 0 (425-475)
4-6 8D Man Store 0
4-21 4D (Not) M1 Reg Bit 7
4-12 (Not) Ctrl Reg Bit 7
4-90 P2 9C (Not) STP Inhibit Store
OR
A
OR
MC181
Store Byte 0
Storage Data Assembler
4-35 P2 B Reg P-7
4-337 9D (Not) Share Cycle
4-325 9D File Data in Bits
4-337 9D Share Cycle
4-13 8D DR-2 Force St Parity
A 9 0 P0
A P0
(0-7, P0) MC141-151
Store Bit 0-7, P0
X
4-25 7A Force Store Control Lines
4-11 9D T7
4-12 Ctrl Reg Bit 2
4-32 3A First Cycle Stor Wd
MD051
(Store Control)
FL
MC181
4-11 9A T1
4-25 7D Inh Store Control
4-11 9C Mach Reset
4-27 P1 7E Y Read and SA Gates On
4-21 9A SAR Bits 1, 14
Sense Amplifier Gates
SAR Bit
1 14
0 0 0-8KA Adrs
0 1 0-8KB Adrs
1 0 8-16KA Adrs
1 1 8-16KB Adrs
MD130
(SA Gates)
N
(Not) Store Bit 0
..7D Time
Strobe Byte 0
4-27 P4 5A 0-7, P0 Sense
OR
0
Stor Data Reg Byte 0
7 P0
PC
Storage Data Out 0-7,P0 (Memory Bits)
(0-7,P0) MD 512-532
Store Byte 0
4-27 P1 8A 0/425
4-27 P1 8A 200/625
4-27 P1 8B (Not) 275/700
Reset Byte 0
4-21 9A SAR Bit 0 Selects which BSM to Address
Jump
Select this BSM
4-90 P2 9C (Not) STP Inhibit Store
4-21 4D Mi Reg Bit 7
4-12 (Not) Ctrl Reg Bit 7
4-6 6A Alter Storage Lt
Store Byte 1
4-27 P1 8A 200/625
4-27 P1 8B (Not) 325/750
(200-325)
TD *
MD130
Time
..7B
(Not) Store Byte 1
Strobe Byte 1
4-27 P4 5A 8-15, P1 Sense
8
Stor Data Reg Byte 1
15 P1
(8-15, P1)
MD 542-562
Storage Data Out 8-15, P1 (Memory Bits)
4-27 P1 8D Inhibit Drivers On
M2I
Inhibit Decode
SAR Bit
1 14
0 0
0 1
1 0
1 1
MD701
Inhibit 0-8KA
Inhibit 0-8KB
Inhibit 8-16KA
Inhibit 8-16KB
Inhibit Drivers
Inhibit Driver for respective bit is active when the data bit latch is off (Bit-0).
..9B Storage Data Out 0-7, P0
..9B Storage Data Out 8-15, P1
MD702-782
4-35 P2 7B A Reg P-7
4-337 9D (Not) Share Cycle
4-325 9D File Data in Bits
4-337 9D Share Cycle
4-13 8D DR-2 Force St Parity
A 9 8 P1
A P1
(8-15, P1) MC161-171
Store Bit 8-15, P1
Store Byte 1
4-27 P1 8A 50/475
4-27 P1 8A (Not) 0/425
Gate In Byte 1 (425-475)
4-27 P1 8A 0/425
200/625
(Not) 275/700
MD-130
Reset Byte 1
Inhibit 4-27 P4 5A
* The time delay is used to adjust the strobe pulse for the best performance at each BSM.



Note: The LS Addr Line Reset is delayed approximately 90 n sec.

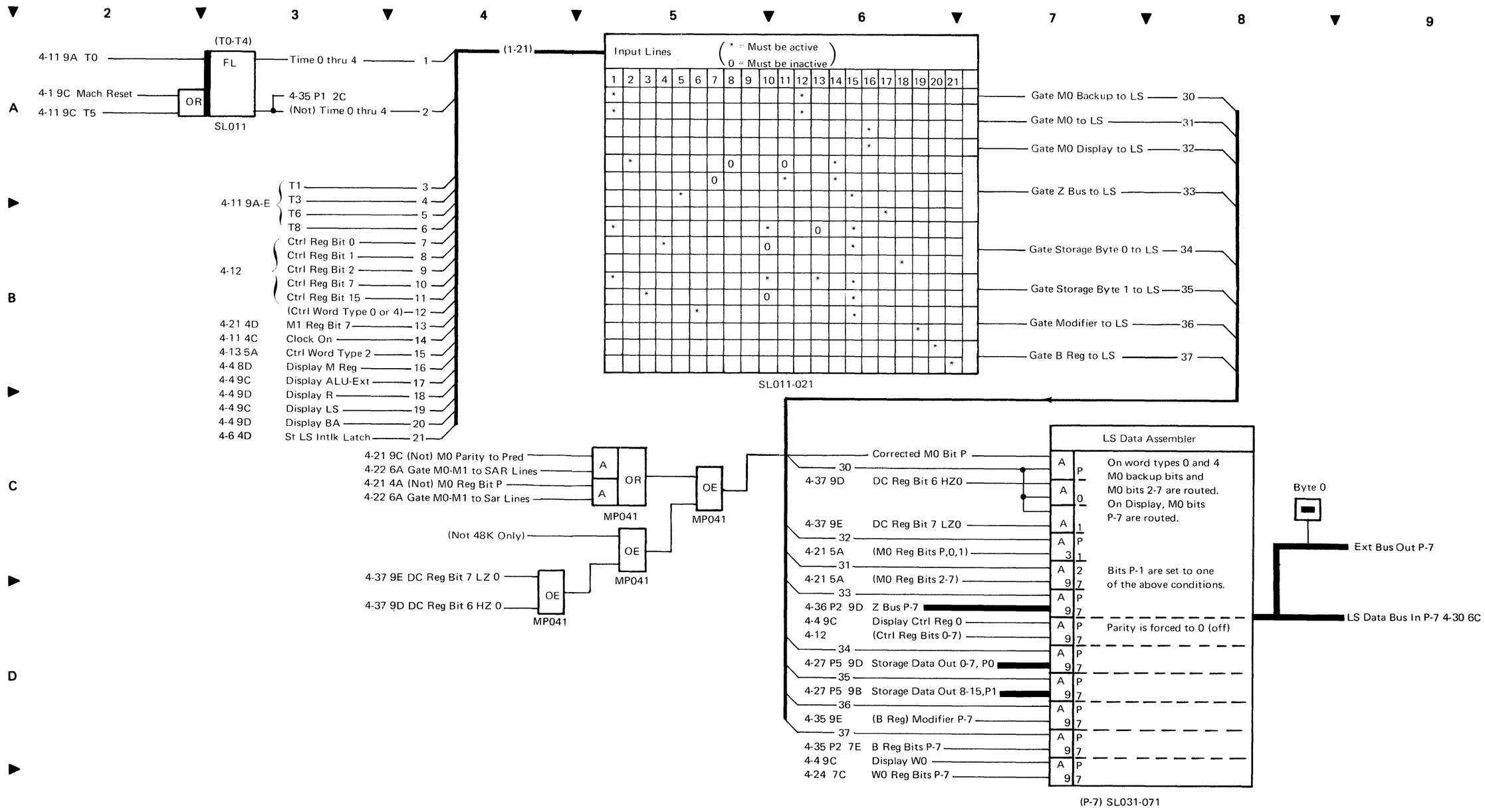
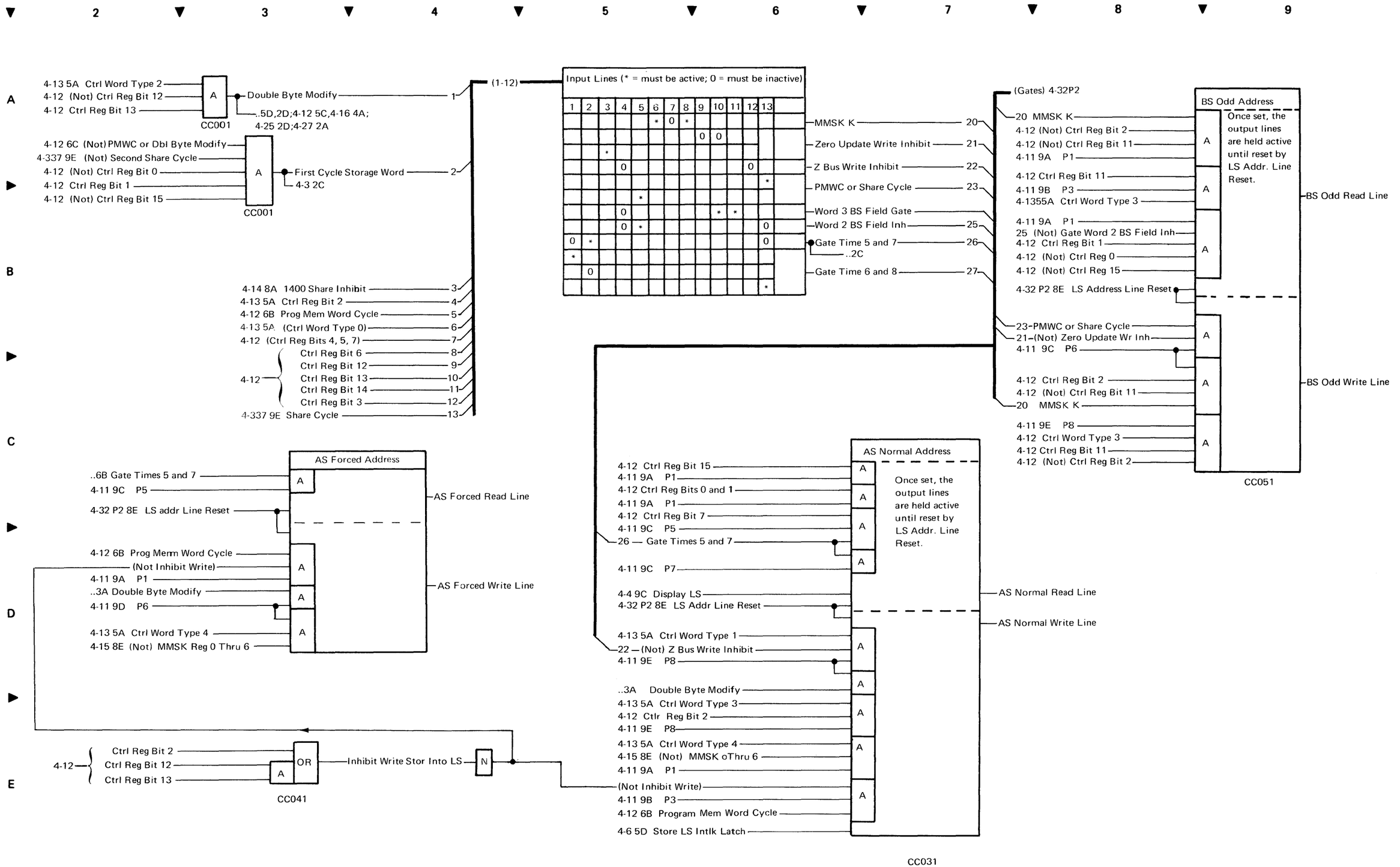
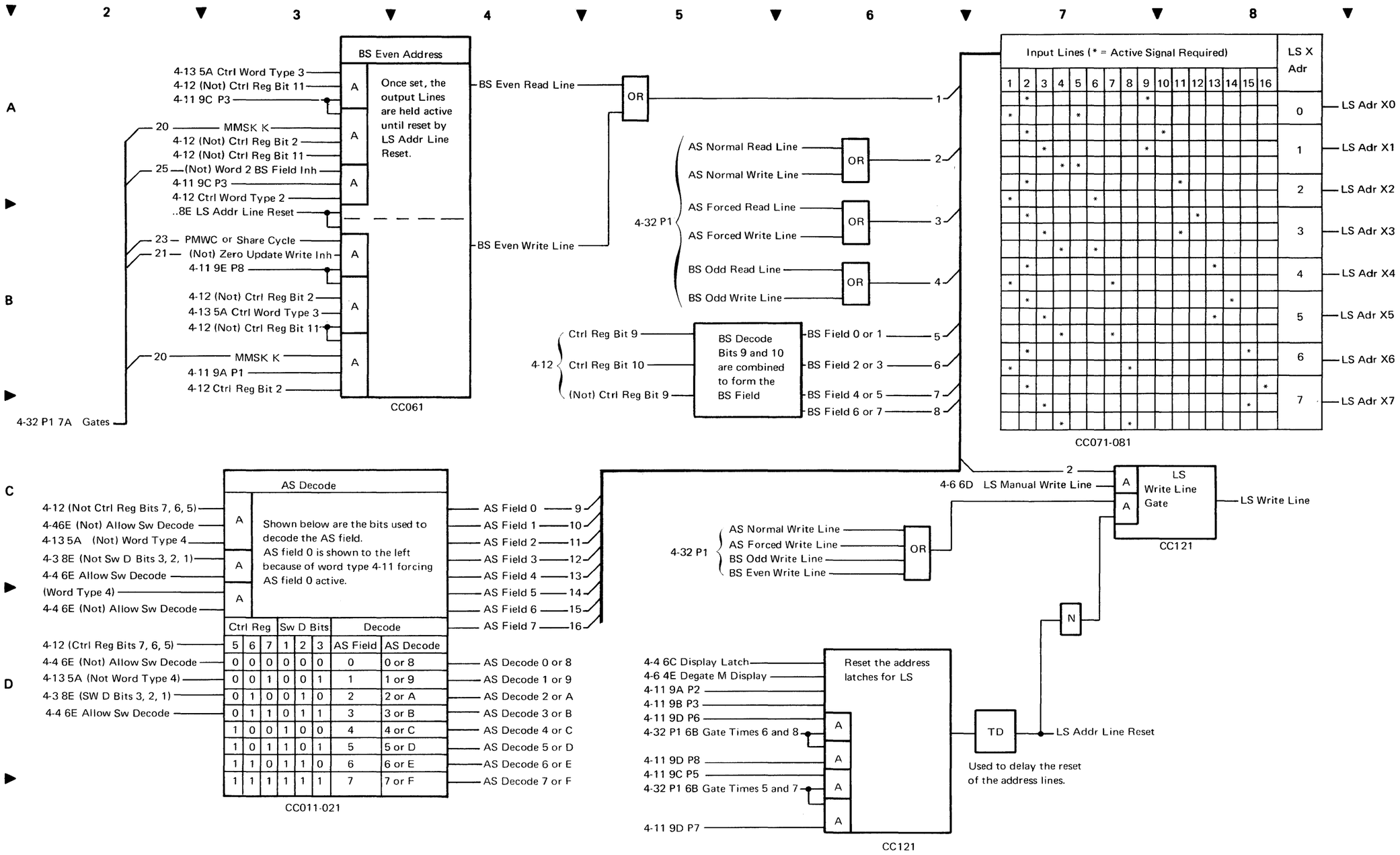

2
3
4
5
6
7
8
9
A
B
C
D
E
(T0-T4)
4-11 9A T0
4-1 9C Mach Reset
4-11 9C T5
FL
OR
SL011
Time 0 thru 4 — 1
4-35 P1 2C
(Not) Time 0 thru 4 — 2
(1-21)
4-11 9A-E
T1 — 3
T3 — 4
T6 — 5
T8 — 6
4-12
Ctrl Reg Bit 0 — 7
Ctrl Reg Bit 1 — 8
Ctrl Reg Bit 2 — 9
Ctrl Reg Bit 7 — 10
Ctrl Reg Bit 15 — 11
(Ctrl Word Type 0 or 4) — 12
4-21 4D M1 Reg Bit 7 — 13
4-11 4C Clock On — 14
4-13 5A Ctrl Word Type 2 — 15
4-4 8D Display M Reg — 16
4-4 9C Display ALU-Ext — 17
4-4 9D Display R — 18
4-4 9C Display LS — 19
4-4 9D Display BA — 20
4-6 4D St LS Intlk Latch — 21
Input Lines
(* = Must be active
0 = Must be inactive)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
SL011-021
Gate M0 Backup to LS — 30
Gate M0 to LS — 31
Gate M0 Display to LS — 32
Gate Z Bus to LS — 33
Gate Storage Byte 0 to LS — 34
Gate Storage Byte 1 to LS — 35
Gate Modifier to LS — 36
Gate B Reg to LS — 37
4-21 9C (Not) M0 Parity to Pred
4-22 6A Gate M0-M1 to SAR Lines
4-21 4A (Not) M0 Reg Bit P
4-22 6A Gate M0-M1 to Sar Lines
A
A
OR
MP041
OE
MP041
(Not 48K Only)
OE
MP041
4-37 9E DC Reg Bit 7 LZ 0
4-37 9D DC Reg Bit 6 HZ 0
OE
MP041
Corrected M0 Bit P
30
4-37 9D DC Reg Bit 6 HZ0
4-37 9E DC Reg Bit 7 LZ0
32
4-21 5A (M0 Reg Bits P,0,1)
31
4-21 5A (M0 Reg Bits 2-7)
33
4-36 P2 9D Z Bus P-7
4-4 9C Display Ctrl Reg 0
4-12 (Ctrl Reg Bits 0-7)
34
4-27 P5 9D Storage Data Out 0-7, P0
35
4-27 P5 9B Storage Data Out 8-15,P1
36
4-35 9E (B Reg) Modifier P-7
37
4-35 P2 7E B Reg Bits P-7
4-4 9C Display W0
4-24 7C W0 Reg Bits P-7
LS Data Assembler
On word types 0 and 4
M0 backup bits and
M0 bits 2-7 are routed.
On Display, M0 bits
P-7 are routed.
Bits P-1 are set to one
of the above conditions.
Parity is forced to 0 (off)
Byte 0
Ext Bus Out P-7
LS Data Bus In P-7 4-30 6C
(P-7) SL031-071

Diagram 4-32. LS Addressing (Part 1 of 3)





Ctrl Reg			Sw D Bits			Decode	
5	6	7	1	2	3	AS Field	AS Decode
0	0	0	0	0	0	0	0 or 8
0	0	1	0	0	1	1	1 or 9
0	1	0	0	1	0	2	2 or A
0	1	1	0	1	1	3	3 or B
1	0	0	1	0	0	4	4 or C
1	0	1	1	0	1	5	5 or D
1	1	0	1	1	0	6	6 or E
1	1	1	1	1	1	7	7 or F

Diagram 4-32. LS Addressing (Part 3 of 3)

2 3 4 5 6 7 8 9

4-11 4C Clock Off
4-4 2E Mod-LS Sw
A

A
4-3 6E C Sw Bits 1-3
4-15 8E (MMSK0-6)
4-14 5B Mode Reg Bits 5-7

Normal Decode (Mode Reg)			Manual Decode (C Sw Bits)			Forced Decode (Bypass Mode Reg)	LS Zone Bit	LS Zone Decode
5	6	7	1	2	3			
0	0	0	0	0	0		–	0
0	0	1	0	0	1	MMSK1 2311 Disk Ctrl Trap	2	1
0	1	0	0	1	0		1	–
0	1	1	0	1	1		1, 2	–
1	0	0	1	0	0		0	4
1	0	1	1	0	1	MMSK5 Comm Chnl Bit Serv MMSK6 Comm Chnl Char Serv	0, 2	5
1	1	0	1	1	0	MMSK3 2540 Reader Trap MMSK4 2540 Punch Trap	0, 1	6
1	1	1	1	1	1	MMSK0 Channel High Trap MMSK2 Channel Low Trap	0, 1, 2	7

Any trap degates the Mode reg decode. The C sw decode occurs when the Mode switch is at Mod-LS and the clock is off; all other decodes (Mode and Traps) are degated. Two MMSK bits active at same time, highest priority decodes.

SL081

LS5 LS6 LS7

LS Zone Bit 2 4-40 7C
LS Zone Bit 1 4-40 7C
LS Zone Bit 0 — 1 — 4-40 7C

LS Zone Decode 0 — 2
LS Zone Decode 1 — 3
LS Zone Decode 4 — 4
LS Zone Decode 5 — 5
LS Zone Decode 6 — 6
LS Zone Decode 7 — 7

4-12 Ctrl Reg Bit 0 — 14
4-12 Ctrl Reg Bit 8 — 15
4-32 P1 6A MMSK K — 16
4-337 9D Share Cycle — 18

B

C

4-32 P1
- AS Normal Read Line
- AS Forced Read Line
- AS Normal Write Line
- AS Forced Write Line

OR — AS Y Line Gate — 8

4-32 P1
- BS Odd Read Line
- BS Even Read Line

4-32 P2
- BS Odd Write Line
- BS Even Write Line

OR — BS Y Line Gate — 9

D

Y Line Ctrl

4-12 (Not) Ctrl Reg Bit 1
4-12 (Not) Ctrl Reg Bit 15
4-11 4C Clock On
4-337 9D Share Cycle

A — Word Type 4 or 0 — Degate Y Lines 0-3 — 10
Force Backup Area — 11
A — File — Degate Y Line 4-7 — 12

E

4-12 Ctrl Reg Bit 4
4-4 6E (Not) Allow Sw Decode
4-3 8E Sw D Bit 0
4-4 6E Allow Sw Decode

A
A
OR — AS Adder Field Bit 0 — 13

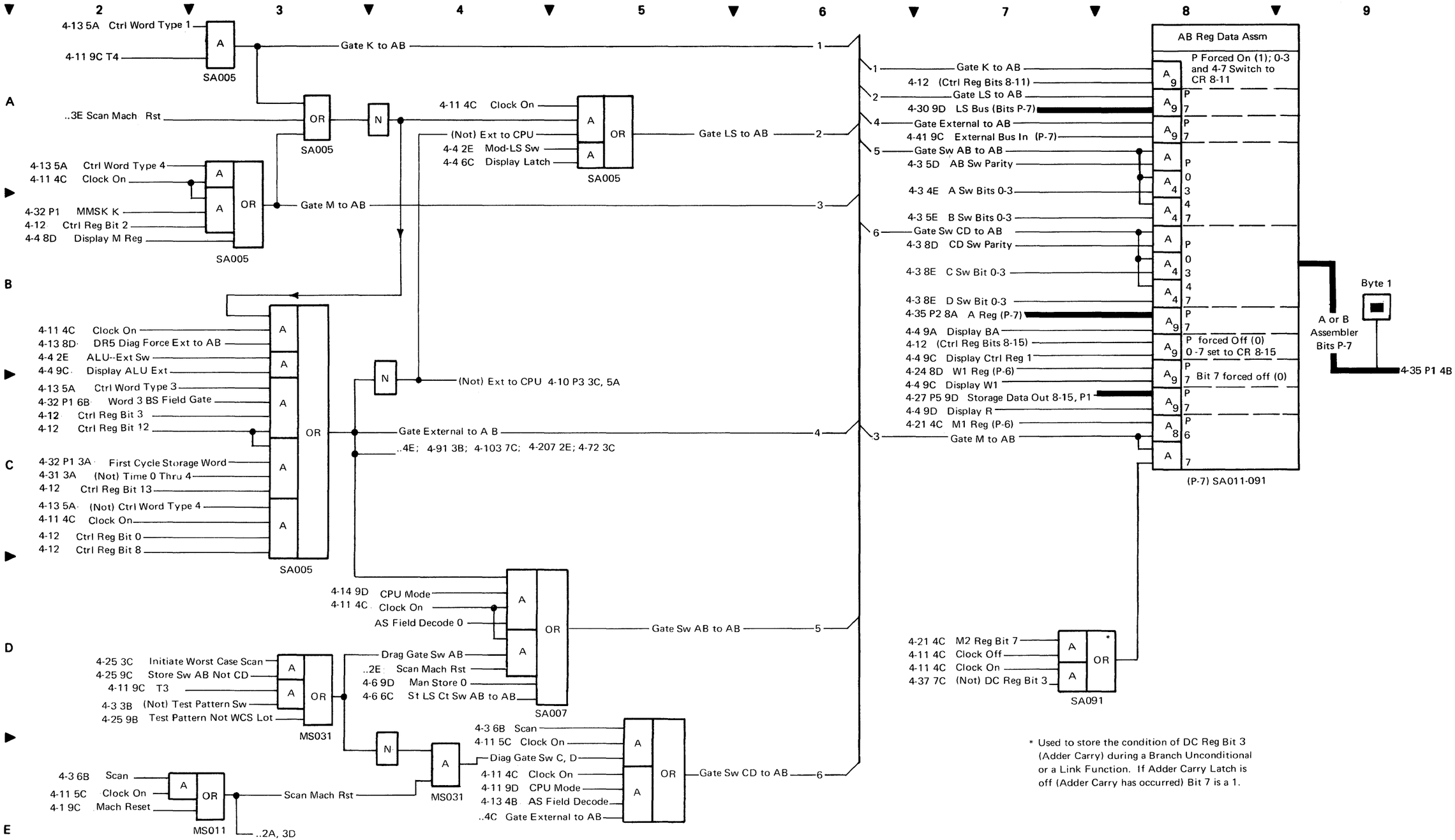
Input Lines (*=Active signal required, 0=Non-active signal required)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	LS Y Adr
	*							*	0					0				0
	*						*		0			0						
	*							*	0					*				1
	*						*		0			*						
								*									*	2
		*						*	0									
		*					*		0									
							*			*			*				0	3
*							*		0			*						
*								*	0					*				
								*						*	*		0	
								*						0	*		0	4
		*						*			0			0				
		*					*				0	0						
				*			*				0	0						5
				*				*			0			0				
					*		*				0	0						6
					*			*			0			0				
						*					0	0						7
						*					0			0				

(Y0-Y3)CC101 (Y4-Y7)CC111

LS Adr Y0
LS Adr Y1
LS Adr Y2
LS Adr Y3
LS Adr Y4
LS Adr Y5
LS Adr Y6
LS Adr Y7

Diagram 4-35. A-B Assembler, Registers, and Modifier (Part 1 of 2)



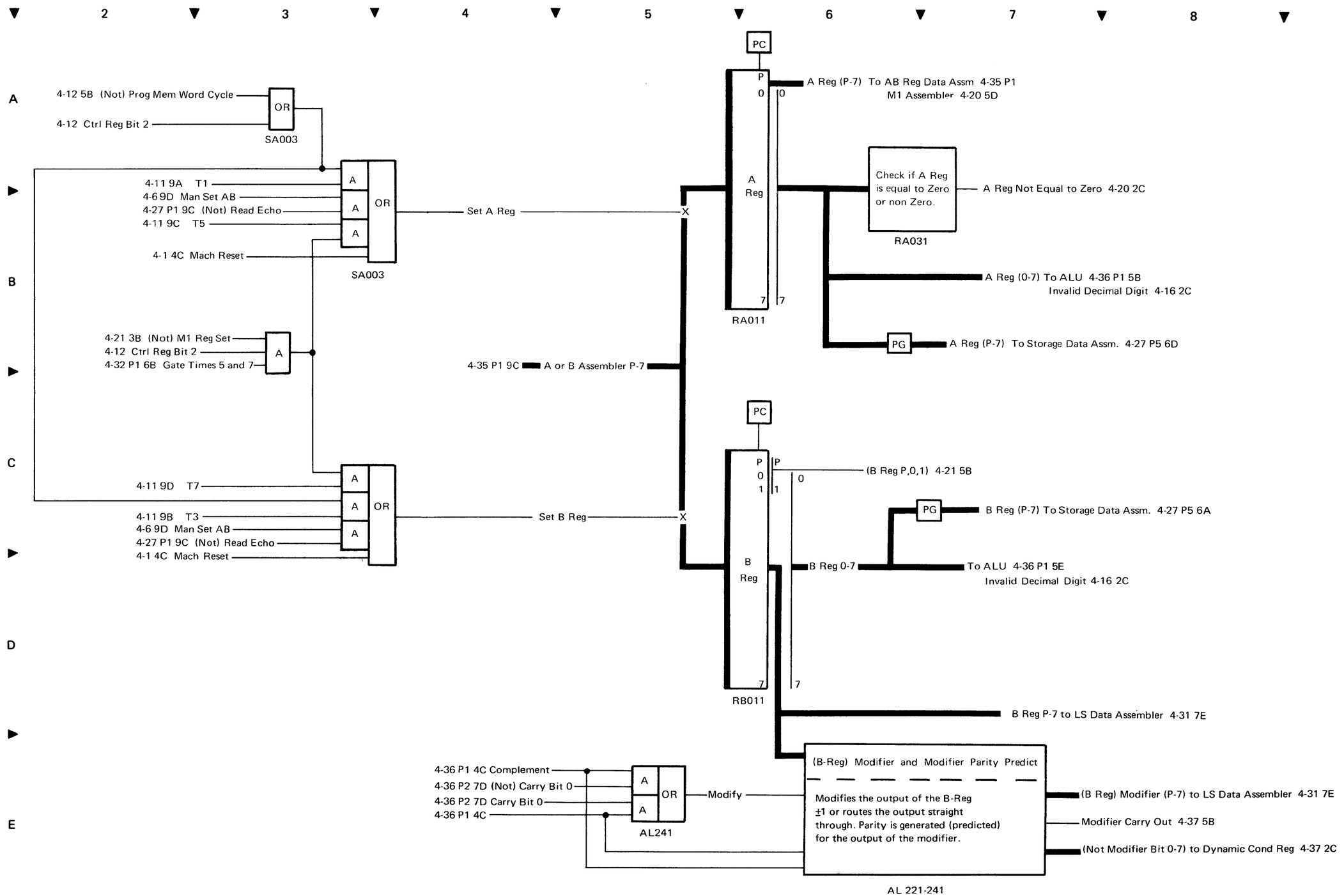
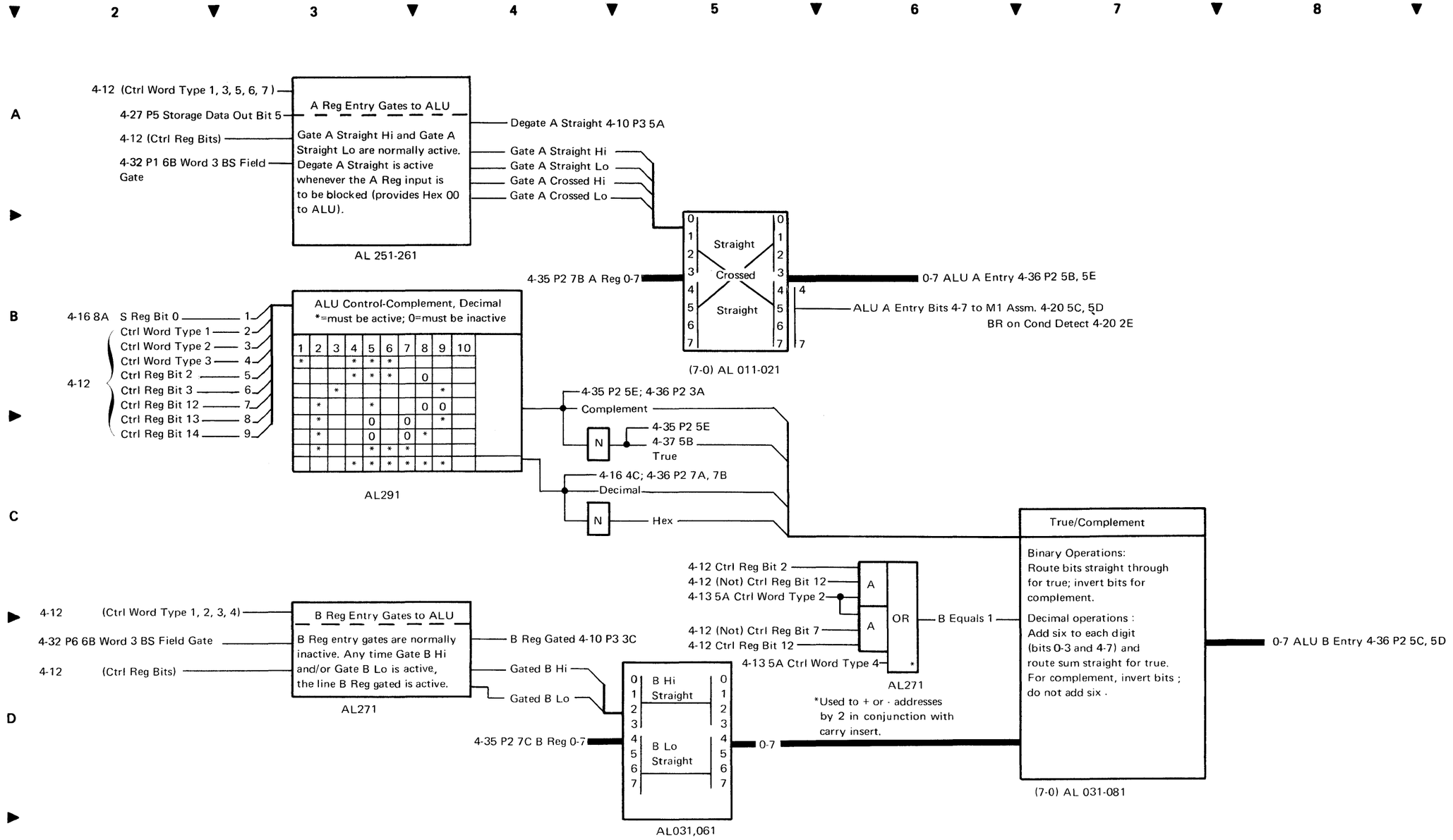

2
3
4
5
6
7
8
9
A
B
C
D
E
4-12 5B (Not) Prog Mem Word Cycle
4-12 Ctrl Reg Bit 2
OR
SA003
4-11 9A T1
4-6 9D Man Set AB
4-27 P1 9C (Not) Read Echo
4-11 9C T5
4-1 4C Mach Reset
A
OR
SA003
Set A Reg
4-21 3B (Not) M1 Reg Set
4-12 Ctrl Reg Bit 2
4-32 P1 6B Gate Times 5 and 7
4-35 P1 9C A or B Assembler P-7
4-11 9D T7
4-11 9B T3
4-6 9D Man Set AB
4-27 P1 9C (Not) Read Echo
4-1 4C Mach Reset
Set B Reg
X
PC
P
0
7
A Reg
RA011
A Reg (P-7) To AB Reg Data Assm 4-35 P1
M1 Assembler 4-20 5D
Check if A Reg is equal to Zero or non Zero.
RA031
A Reg Not Equal to Zero 4-20 2C
A Reg (0-7) To ALU 4-36 P1 5B
Invalid Decimal Digit 4-16 2C
PG
A Reg (P-7) To Storage Data Assm. 4-27 P5 6D
PC
P
0
1
B
Reg
RB011
(B Reg P,0,1) 4-21 5B
PG
B Reg (P-7) To Storage Data Assm. 4-27 P5 6A
B Reg 0-7
To ALU 4-36 P1 5E
Invalid Decimal Digit 4-16 2C
B Reg P-7 to LS Data Assembler 4-31 7E
4-36 P1 4C Complement
4-36 P2 7D (Not) Carry Bit 0
4-36 P2 7D Carry Bit 0
4-36 P1 4C
OR
AL241
Modify
(B-Reg) Modifier and Modifier Parity Predict
Modifies the output of the B-Reg ±1 or routes the output straight through. Parity is generated (predicted) for the output of the modifier.
(B Reg) Modifier (P-7) to LS Data Assembler 4-31 7E
Modifier Carry Out 4-37 5B
(Not Modifier Bit 0-7) to Dynamic Cond Reg 4-37 2C
AL 221-241

Diagram 4-36. ALU (Part 1 of 2)



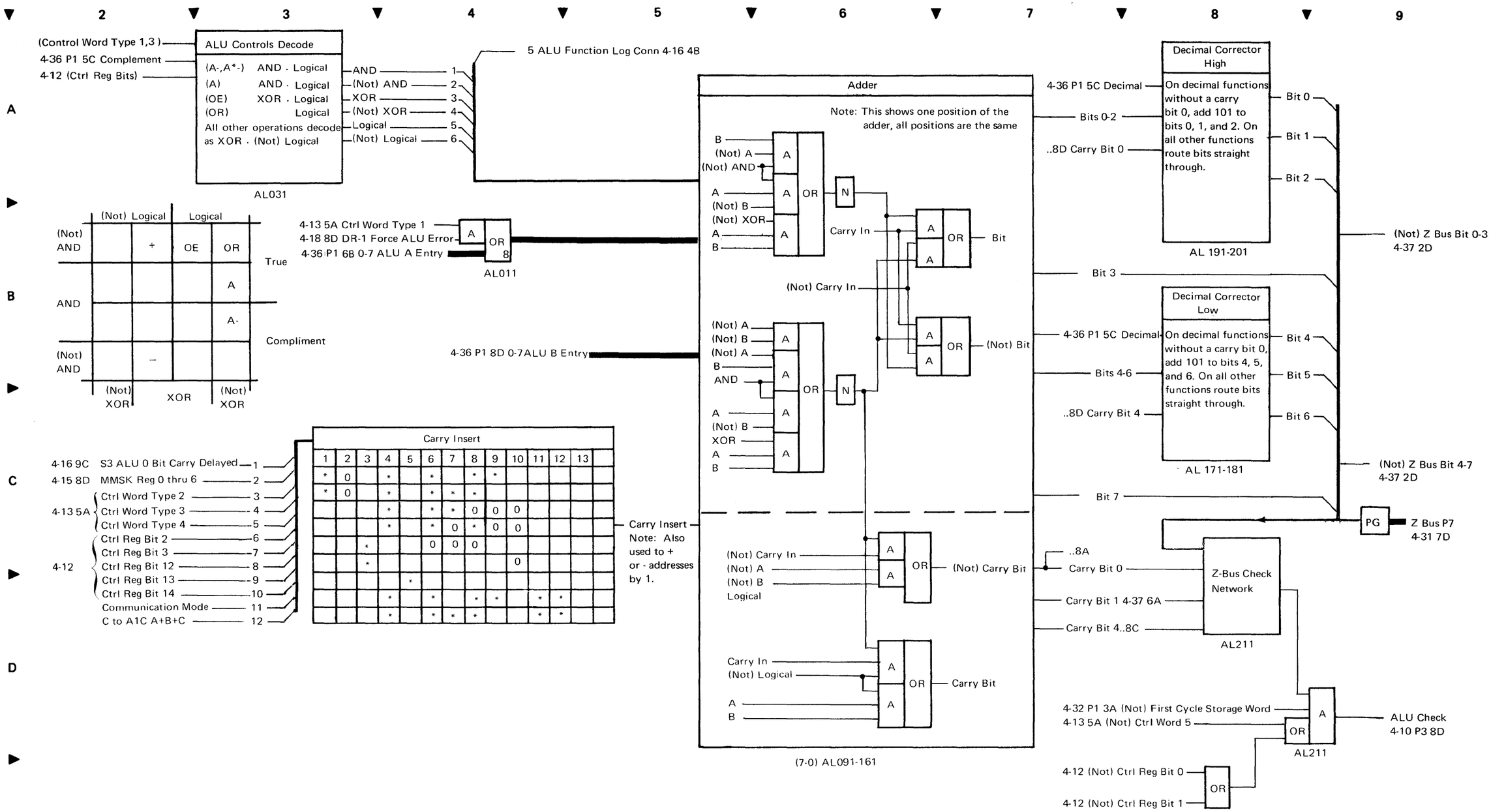

2
3
4
5
6
7
8
9
A
B
C
D
E
(Control Word Type 1,3)
4-36 P1 5C Complement
4-12 (Ctrl Reg Bits)
ALU Controls Decode
(A-,A*-) AND · Logical
(A) AND · Logical
(OE) XOR · Logical
(OR) Logical
All other operations decode as XOR · (Not) Logical
AND — 1
(Not) AND — 2
XOR — 3
(Not) XOR — 4
Logical — 5
(Not) Logical — 6
AL031
5 ALU Function Log Conn 4-16 4B
(Not) Logical
Logical
(Not) AND
+
OE
OR
True
A
AND
A-
Compliment
(Not) AND
–
(Not) XOR
XOR
(Not) XOR
4-13 5A Ctrl Word Type 1
4-18 8D DR-1 Force ALU Error
4-36 P1 6B 0-7 ALU A Entry
A
OR
8
AL011
4-36 P1 8D 0-7 ALU B Entry
Carry Insert
1 2 3 4 5 6 7 8 9 10 11 12 13
4-16 9C S3 ALU 0 Bit Carry Delayed — 1
4-15 8D MMSK Reg 0 thru 6 — 2
4-13 5A Ctrl Word Type 2 — 3
Ctrl Word Type 3 — 4
Ctrl Word Type 4 — 5
4-12 Ctrl Reg Bit 2 — 6
Ctrl Reg Bit 3 — 7
Ctrl Reg Bit 12 — 8
Ctrl Reg Bit 13 — 9
Ctrl Reg Bit 14 — 10
Communication Mode — 11
C to A1C A+B+C — 12
Carry Insert
Note: Also used to + or - addresses by 1.
Adder
Note: This shows one position of the adder, all positions are the same
B
(Not) A
(Not) AND
A
(Not) B
(Not) XOR
A
B
A
OR
N
Carry In
Bit
(Not) Carry In
(Not) A
(Not) B
AND
A
(Not) B
XOR
A
B
(Not) Bit
(Not) Carry In
(Not) A
(Not) B
Logical
(Not) Carry Bit
Carry In
(Not) Logical
A
B
Carry Bit
(7-0) AL091-161
4-36 P1 5C Decimal
Bits 0-2
..8D Carry Bit 0
Decimal Corrector High
On decimal functions without a carry bit 0, add 101 to bits 0, 1, and 2. On all other functions route bits straight through.
Bit 0
Bit 1
Bit 2
AL 191-201
Bit 3
4-36 P1 5C Decimal
Bits 4-6
..8D Carry Bit 4
Decimal Corrector Low
On decimal functions without a carry bit 0, add 101 to bits 4, 5, and 6. On all other functions route bits straight through.
Bit 4
Bit 5
Bit 6
AL 171-181
(Not) Z Bus Bit 0-3
4-37 2D
(Not) Z Bus Bit 4-7
4-37 2D
Bit 7
PG
Z Bus P7
4-31 7D
..8A
Carry Bit 0
Carry Bit 1 4-37 6A
Carry Bit 4..8C
Z-Bus Check Network
AL211
4-32 P1 3A (Not) First Cycle Storage Word
4-13 5A (Not) Ctrl Word 5
OR
A
ALU Check
4-10 P3 8D
AL211
4-12 (Not) Ctrl Reg Bit 0
4-12 (Not) Ctrl Reg Bit 1
OR

Diagram 4-37. D C Register

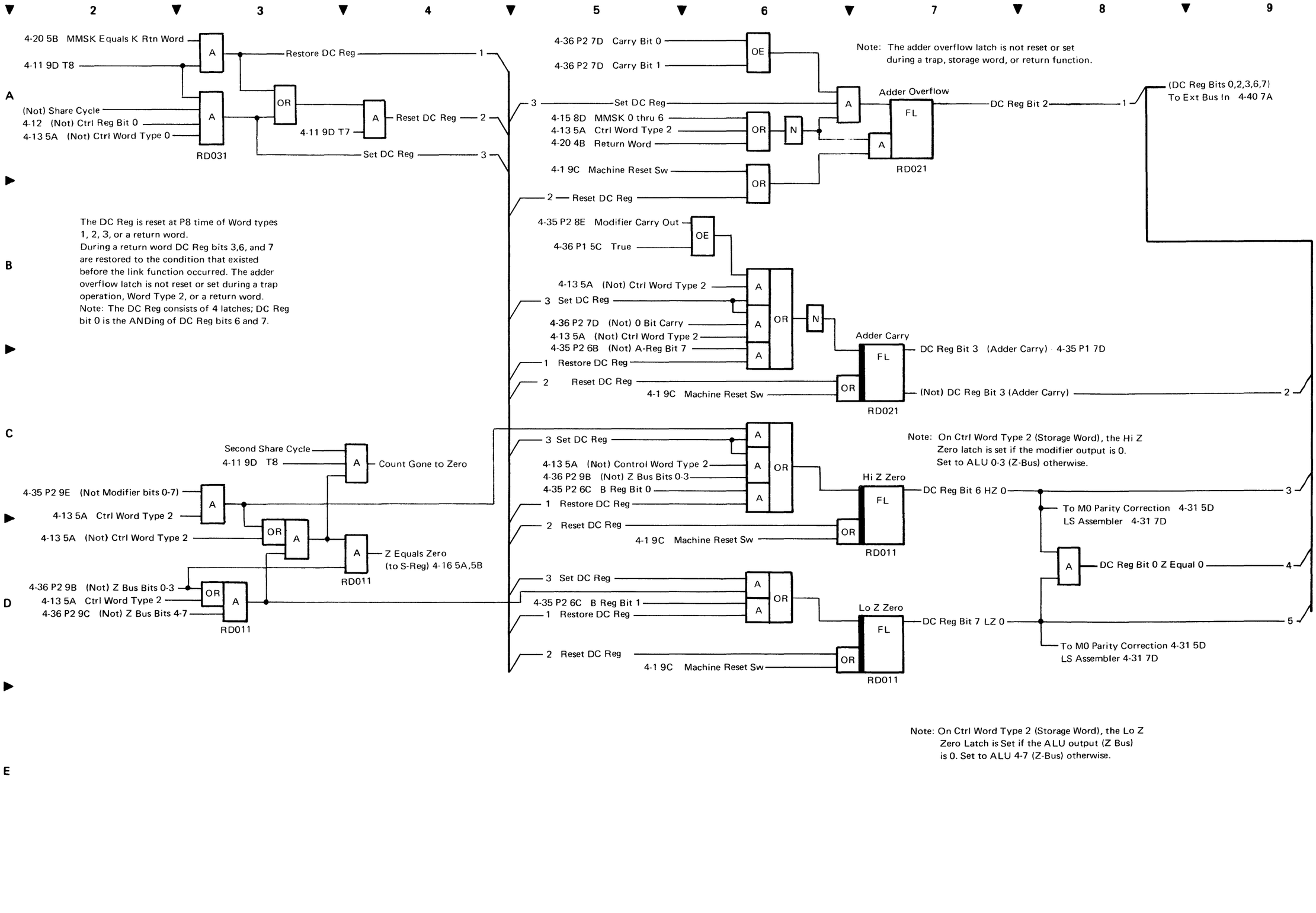
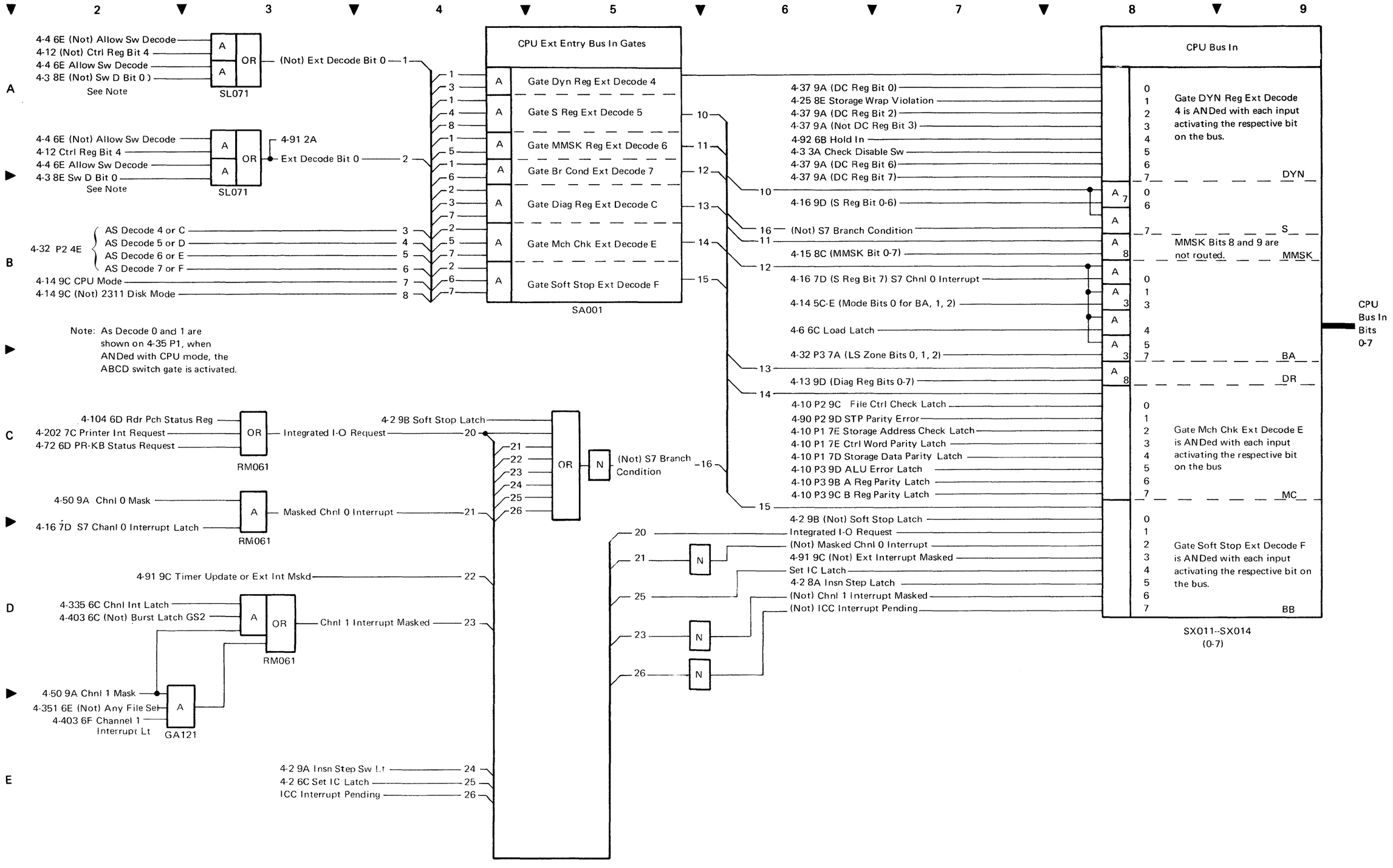
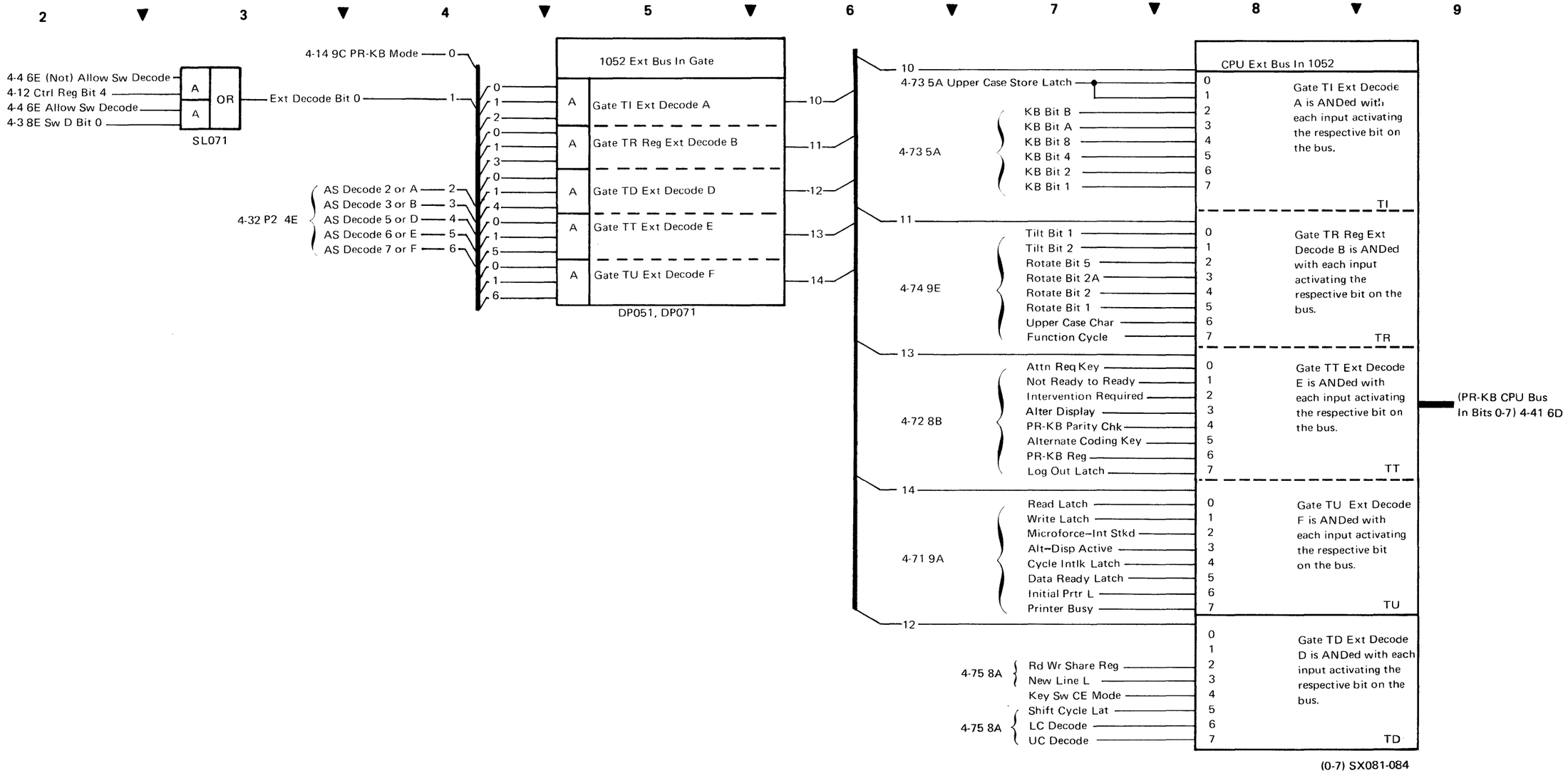


Diagram 4-40. External Facility (CPU Mode and Common) CPU Bus In



2
3
4
5
6
7
8
9
A
B
C
D
E
4-4 6E (Not) Allow Sw Decode
4-12 Ctrl Reg Bit 4
4-4 6E Allow Sw Decode
4-3 8E Sw D Bit 0
A
A
OR
SL071
Ext Decode Bit 0
1
4-14 9C CPU Mode–0
0
4-32 P2 4E
AS Decode 0 or 8—2
AS Decode 1 or 9—3
AS Decode 2 or A—4
0
1
3
4-4 6E (Not) Allow Sw Decode
4-12 (Not) Ctrl Reg Bit 4
4-4 6E Allow Sw Decode
4-3 8E (Not) Sw D Bit 0
SL071
(Not) Ext Decode Bit 0
5
0
1
4
4-14 9C (Not) 2311 Mode
6
7
5
3
5
6
(Not) 2560 Mode
CPU Ext Bus In Gates
Gate Dir-Ctrl Ext Decode 8
Gate Ext Int Decode 9
Gate Timer Count Decode 4
Gate STP0 Ext Decode 2
Gate STP1 Ext Decode 3
(2,3) DP041
(8,9,A) DP061
10
11
12
13
14
Ext Feat Bus In
10
4-92 8A (Not) Dir Ctrl Bit 0-7
11
4-91 6D (Not) Timer Ext Int Bit 0
4-2 5D (Not) Console Int Latch
4-91 6D (Not Ext Int Bits 2-7)
12
4-91 7B (Not Timer Reg 4-7)
JI
Note: The external and timer interrupt latches are reset on, therefore to recognize an interrupt the latch must be off.
XINT
Bits 0-3 are forced to 1's
TIM
Ext Feat Bus In Bits 0-7 ..6D
(0-7) Sx071-072
CPU Ext Bus In
13
4-90 P2 5B (STP0 Bits 0-3)
4-90 P2 5E (Q Reg Bits 4-7)
14
4-90 P2 9E (STP1 Bits 0-7)
STP0
STP1
CPU Ext Bus In Bit 0-7 ..6D
(0-7) SX081-084
4-45 Channel Ext (0-7)
4-44 1403 Ext (0-7)
4-43 2540 Ext (0-7)
OR
SX032-041
IO Ext Bus In (0-7)
4-40 CPU Bus In (0-7)
4-46 P2 2311 Ext Bus In (0-7)
OR
SA101
Ext Bus In P-7 4-35 P1 7A
4-42 PR-KB CPU Bus In (0-7)
4-47 Comm Ext Bus In (0-7)
..9C CPU Ext Bus In (0-7)
..9A Ext Feat Bus In
OR
IO CPU Bus In (0-7)
4-73 3B KB Bit C
4-42 Gate TI Ext Decode A
4-405 6A Chnl Bus In Bit P
4-45 Gate 6-B In Ext Decode F
4-90 P2 6C STP1 Bit P
..6B Gate STP1 External Decode 3
OR
SX031
Ext Bus In Bit P

Diagram 4-42. External Facility (1052 Mode) 1052 CPU Bus In



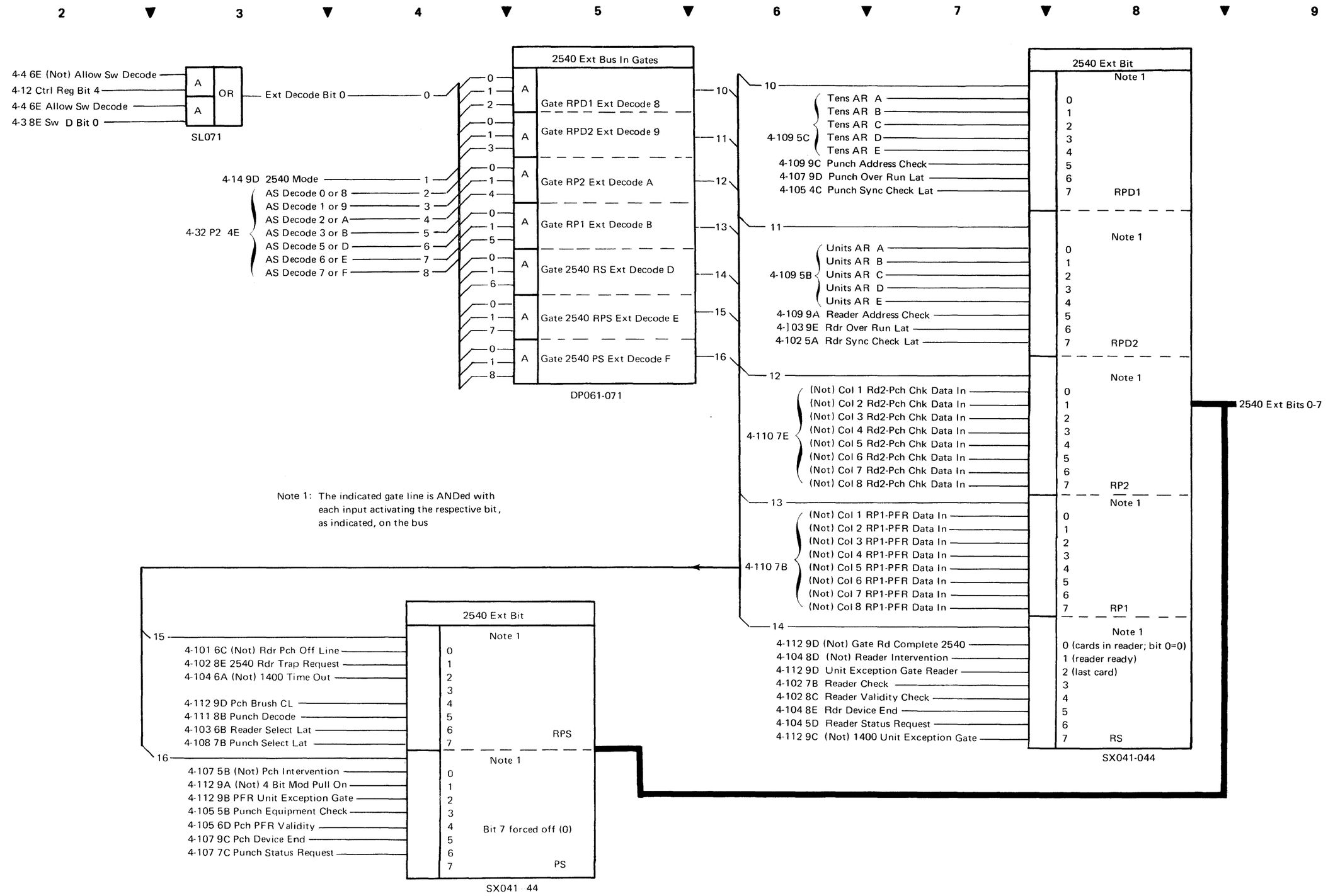
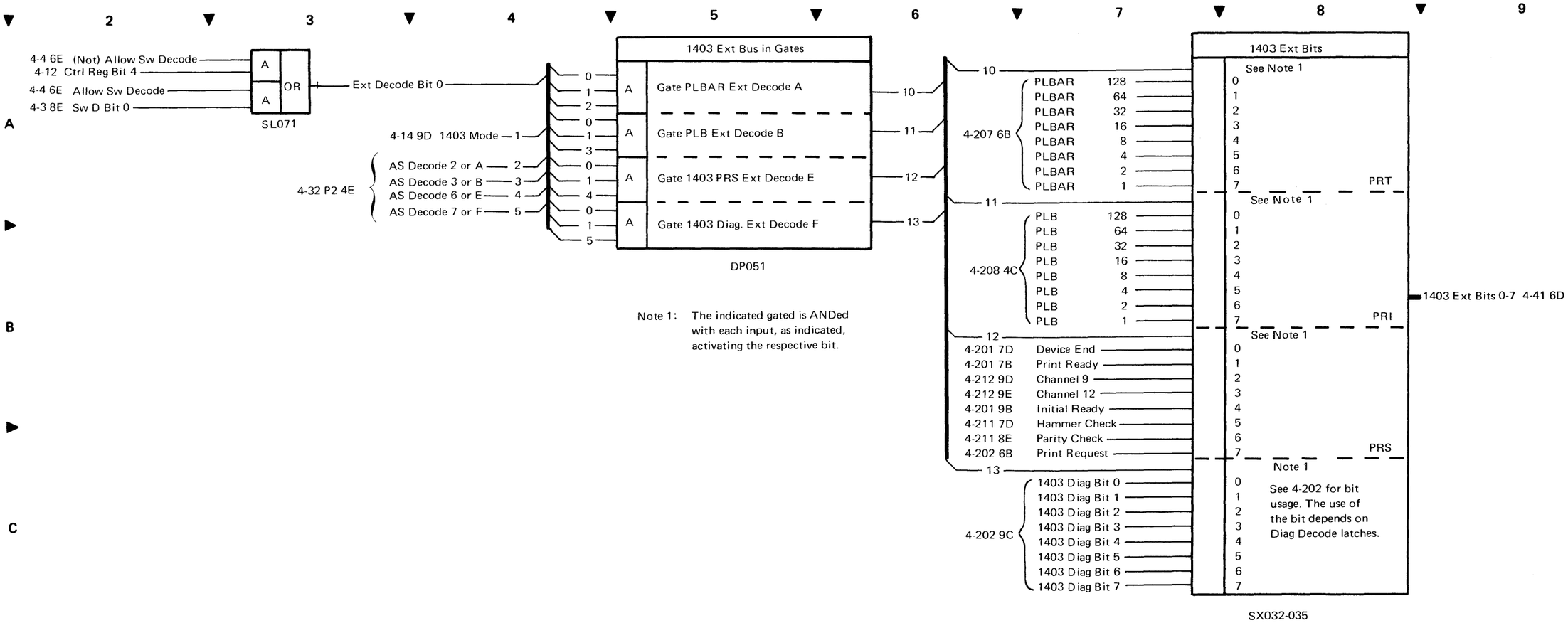

2 3 4 5 6 7 8 9
A B C D E
4-4 6E (Not) Allow Sw Decode
4-12 Ctrl Reg Bit 4
4-4 6E Allow Sw Decode
4-3 8E Sw D Bit 0
A
A
OR
Ext Decode Bit 0
SL071
4-14 9D 2540 Mode
4-32 P2 4E
AS Decode 0 or 8
AS Decode 1 or 9
AS Decode 2 or A
AS Decode 3 or B
AS Decode 5 or D
AS Decode 6 or E
AS Decode 7 or F
2540 Ext Bus In Gates
Gate RPD1 Ext Decode 8
Gate RPD2 Ext Decode 9
Gate RP2 Ext Decode A
Gate RP1 Ext Decode B
Gate 2540 RS Ext Decode D
Gate 2540 RPS Ext Decode E
Gate 2540 PS Ext Decode F
DP061-071
2540 Ext Bit
Note 1
4-109 5C Tens AR A/B/C/D/E
4-109 9C Punch Address Check
4-107 9D Punch Over Run Lat
4-105 4C Punch Sync Check Lat
RPD1
4-109 5B Units AR A/B/C/D/E
4-109 9A Reader Address Check
4-103 9E Rdr Over Run Lat
4-102 5A Rdr Sync Check Lat
RPD2
4-110 7E (Not) Col 1-8 Rd2-Pch Chk Data In
RP2
4-110 7B (Not) Col 1-8 RP1-PFR Data In
RP1
4-112 9D (Not) Gate Rd Complete 2540
4-104 8D (Not) Reader Intervention
4-112 9D Unit Exception Gate Reader
4-102 7B Reader Check
4-102 8C Reader Validity Check
4-104 8E Rdr Device End
4-104 5D Reader Status Request
4-112 9C (Not) 1400 Unit Exception Gate
0 (cards in reader; bit 0=0)
1 (reader ready)
2 (last card)
RS
SX041-044
2540 Ext Bits 0-7
Note 1: The indicated gate line is ANDed with each input activating the respective bit, as indicated, on the bus
2540 Ext Bit
4-101 6C (Not) Rdr Pch Off Line
4-102 8E 2540 Rdr Trap Request
4-104 6A (Not) 1400 Time Out
4-112 9D Pch Brush CL
4-111 8B Punch Decode
4-103 6B Reader Select Lat
4-108 7B Punch Select Lat
RPS
4-107 5B (Not) Pch Intervention
4-112 9A (Not) 4 Bit Mod Pull On
4-112 9B PFR Unit Exception Gate
4-105 5B Punch Equipment Check
4-105 6D Pch PFR Validity
4-107 9C Pch Device End
4-107 7C Punch Status Request
Bit 7 forced off (0)
PS
SX041-44

Diagram 4-44. External Facility (1403 Mode) 1403 External Bits



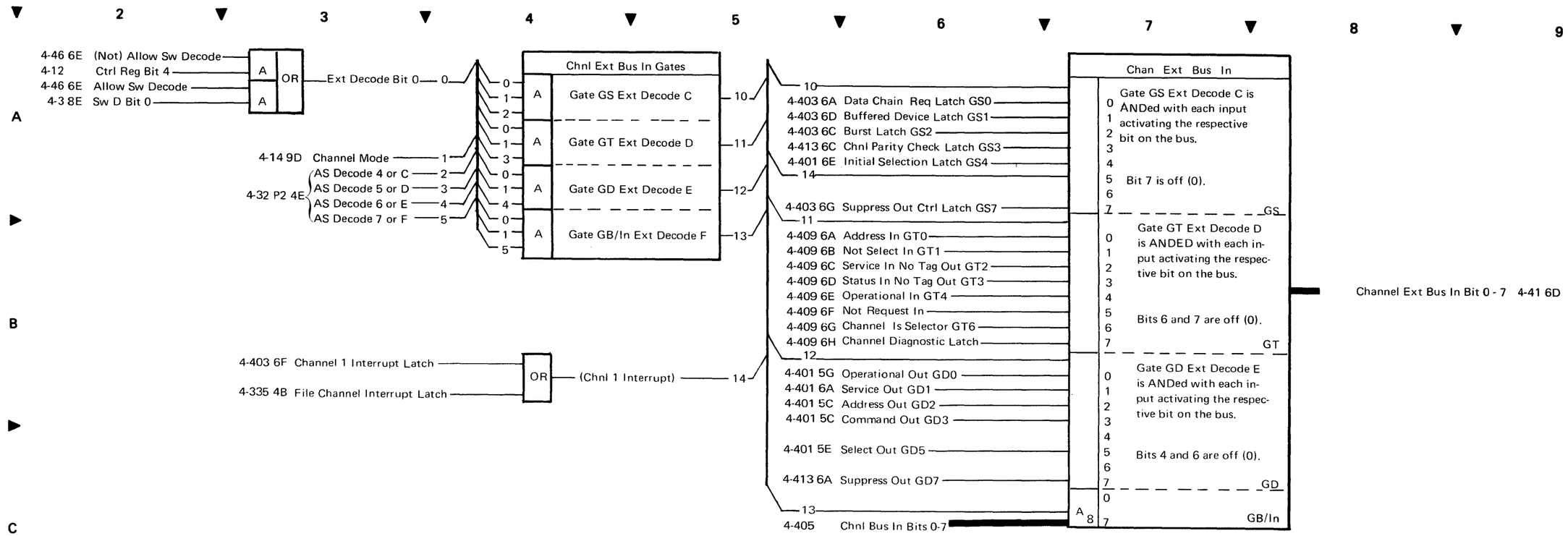
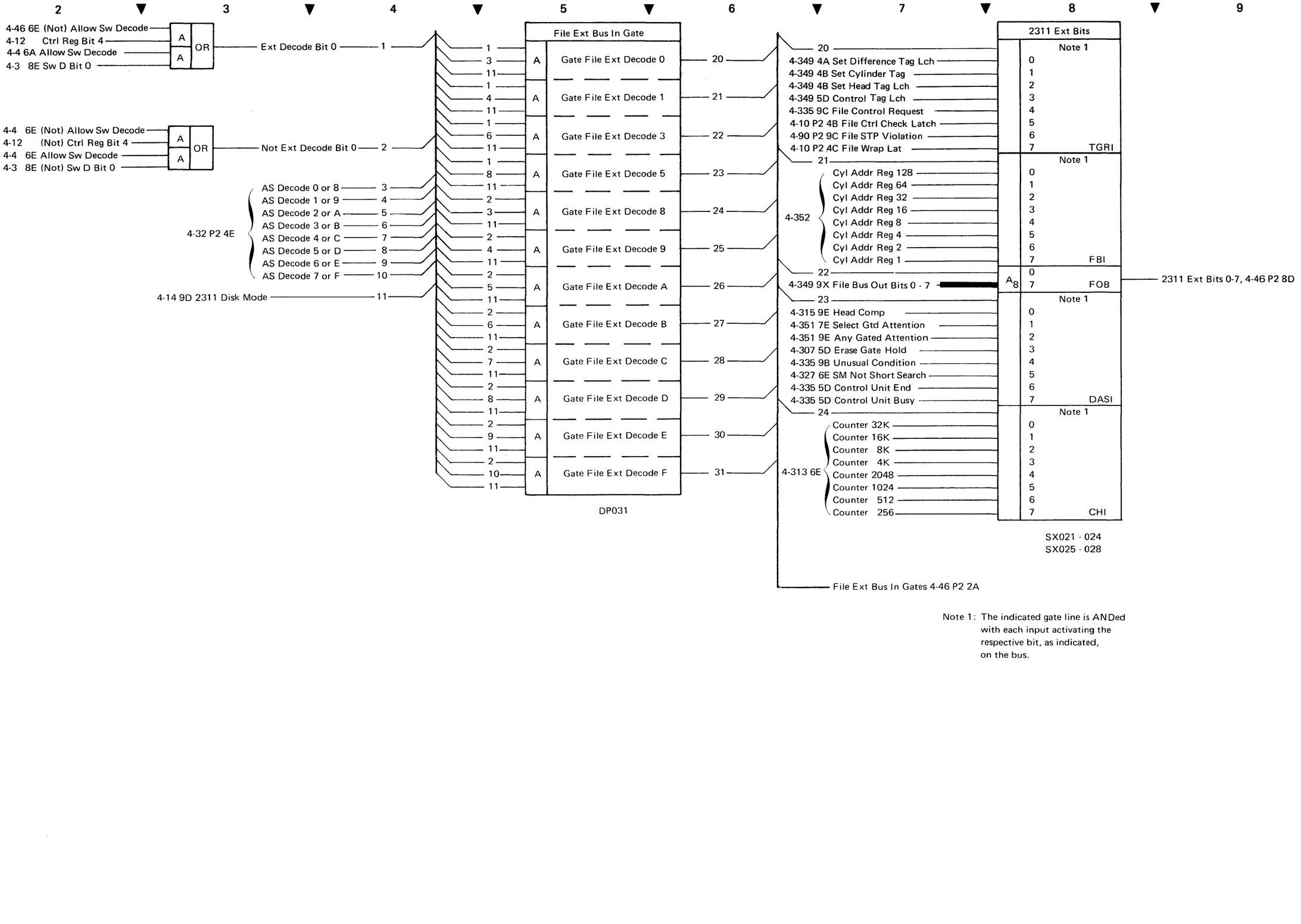
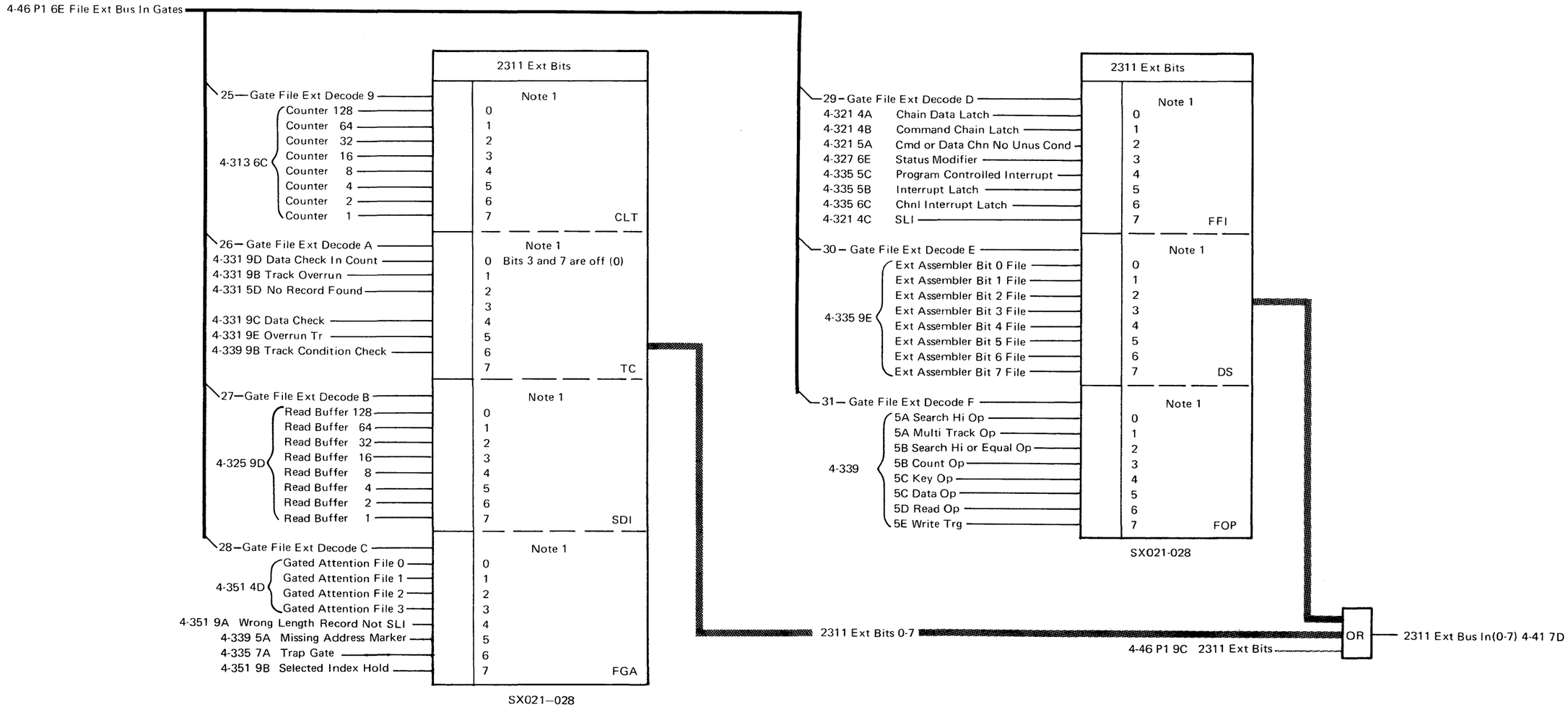

2
3
4
5
6
7
8
9
A
B
C
D
E
4-46 6E (Not) Allow Sw Decode
4-12 Ctrl Reg Bit 4
4-46 6E Allow Sw Decode
4-3 8E Sw D Bit 0
A
OR
Ext Decode Bit 0
0
4-14 9D Channel Mode
4-32 P2 4E
AS Decode 4 or C
AS Decode 5 or D
AS Decode 6 or E
AS Decode 7 or F
1
2
3
4
5
Chnl Ext Bus In Gates
Gate GS Ext Decode C
Gate GT Ext Decode D
Gate GD Ext Decode E
Gate GB/In Ext Decode F
10
11
12
13
4-403 6F Channel 1 Interrupt Latch
4-335 4B File Channel Interrupt Latch
OR
(Chnl 1 Interrupt)
14
4-403 6A Data Chain Req Latch GS0
4-403 6D Buffered Device Latch GS1
4-403 6C Burst Latch GS2
4-413 6C Chnl Parity Check Latch GS3
4-401 6E Initial Selection Latch GS4
4-403 6G Suppress Out Ctrl Latch GS7
4-409 6A Address In GT0
4-409 6B Not Select In GT1
4-409 6C Service In No Tag Out GT2
4-409 6D Status In No Tag Out GT3
4-409 6E Operational In GT4
4-409 6F Not Request In
4-409 6G Channel Is Selector GT6
4-409 6H Channel Diagnostic Latch
4-401 5G Operational Out GD0
4-401 6A Service Out GD1
4-401 5C Address Out GD2
4-401 5C Command Out GD3
4-401 5E Select Out GD5
4-413 6A Suppress Out GD7
4-405 Chnl Bus In Bits 0-7
Chan Ext Bus In
Gate GS Ext Decode C is ANDed with each input activating the respective bit on the bus.
Bit 7 is off (0).
GS
Gate GT Ext Decode D is ANDED with each input activating the respective bit on the bus.
Bits 6 and 7 are off (0).
GT
Gate GD Ext Decode E is ANDed with each input activating the respective bit on the bus.
Bits 4 and 6 are off (0).
GD
A 8
GB/In
Channel Ext Bus In Bit 0 - 7 4-41 6D

Diagram 4-46. External Facility (2311 Mode) 2311 Ext Bits (Part 1 of 2)

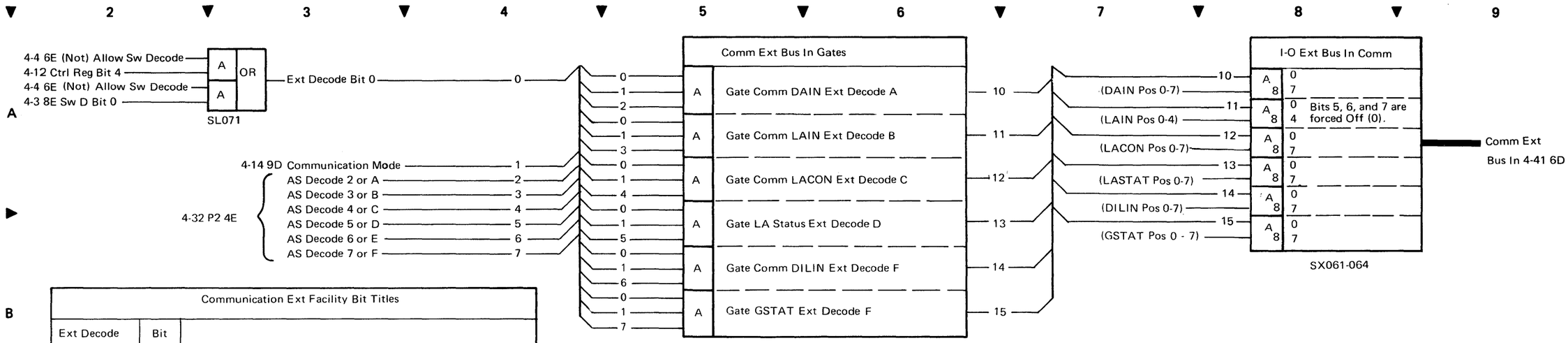


Note 1: The indicated gate line is ANDed with each input activating the respective bit, as indicated, on the bus.



Note 1: The indicated gate line is ANDed with each input activating the respective bit, as indicated, on the bus.

Diagram 4-47. External Facility (Communication Mode) Comm Ext Bus In



Communication Ext Facility Bit Titles

Ext Decode	Bit	
1010 (A) DAIN= Data In	0	Sync Data In Bit 0
	1	Sync Data In Bit 1
	2	Sync Data In Bit 2
	3	Sync Data In Bit 3
	4	Sync Data In Bit 4
	5	Sync Data In Bit 5
	6	Sync Data In Bit 6
	7	Sync Data In Bit 7
1011 (B) LAIN= Line Address In	0	Comm Line Address In Bit 0
	1	Comm Line Address In Bit 1
	2	Comm Line Address In Bit 2
	3	Comm Line Address In Bit 3
	4	Comm Line Address In Bit 4
	5	Forced Off (0)
	6	
	7	

Ext Decode	Bit	Sync Mode	Start/Stop Mode
1100 (C) LACON= Line Adapter Conditions	0	LA Enabled	Line Adrs Enabled
	1	Int/Ext Clock	
	2	Even/Odd Parity	Even/Odd Parity
	3	Leased/Switched	Leased/Switched Network
	4	Interface AB	Bit Overflow
	5		Rcv Bit Buffer
	6		
	7		

Ext Decode	Bit	Sync Mode	Start/Stop Mode
1101 (D) LASTAT= Line Adapter Status	0	Clr to Send Off	Clear to Send Off
	1	Data Set Rdy On	Data Set Rdy On
	2	1 Second Time Out Trap	IBM I/II or TTY1/11
	3	3 Second Time Out Trap	TC1 IBM/TTY
	4	Char Phase	Transmit Mode
	5	Sync Char Serv Trap	Transmit Line Trigger (mrk/sp)
	6	Overflow	Line Quiet; Rcv Line (mark/space)
	7	Sync Chain Serv	Telegraph In Adapter

Ext Decode	Bit	
1110 (E) DILIN= Dial In	0	Power Indicator On(PWI)
	1	Abandon Call and Retry (ACR)
	2	Present Next Digit (PND)
	3	Digit Present (DPR)
	4	Call Reqst (CRQ); or Dial NBR8(Diag)
	5	Dial NBR4(Diag)
	6	Dial NBR2 (Diag)
	7	Valid Address; Dial NBR1(Diag)

Ext Decode	Bit	
1111(F) GSTAT= General Status	0	Sync Service Trap
	1	General Chain Service Trap
	2	Data Set Ready Trap
	3	Dial Service Trap
	4	Start/Stop Char Serv Trap
	5	Time-Out Update Trap
	6	
	7	Time-Out Remember

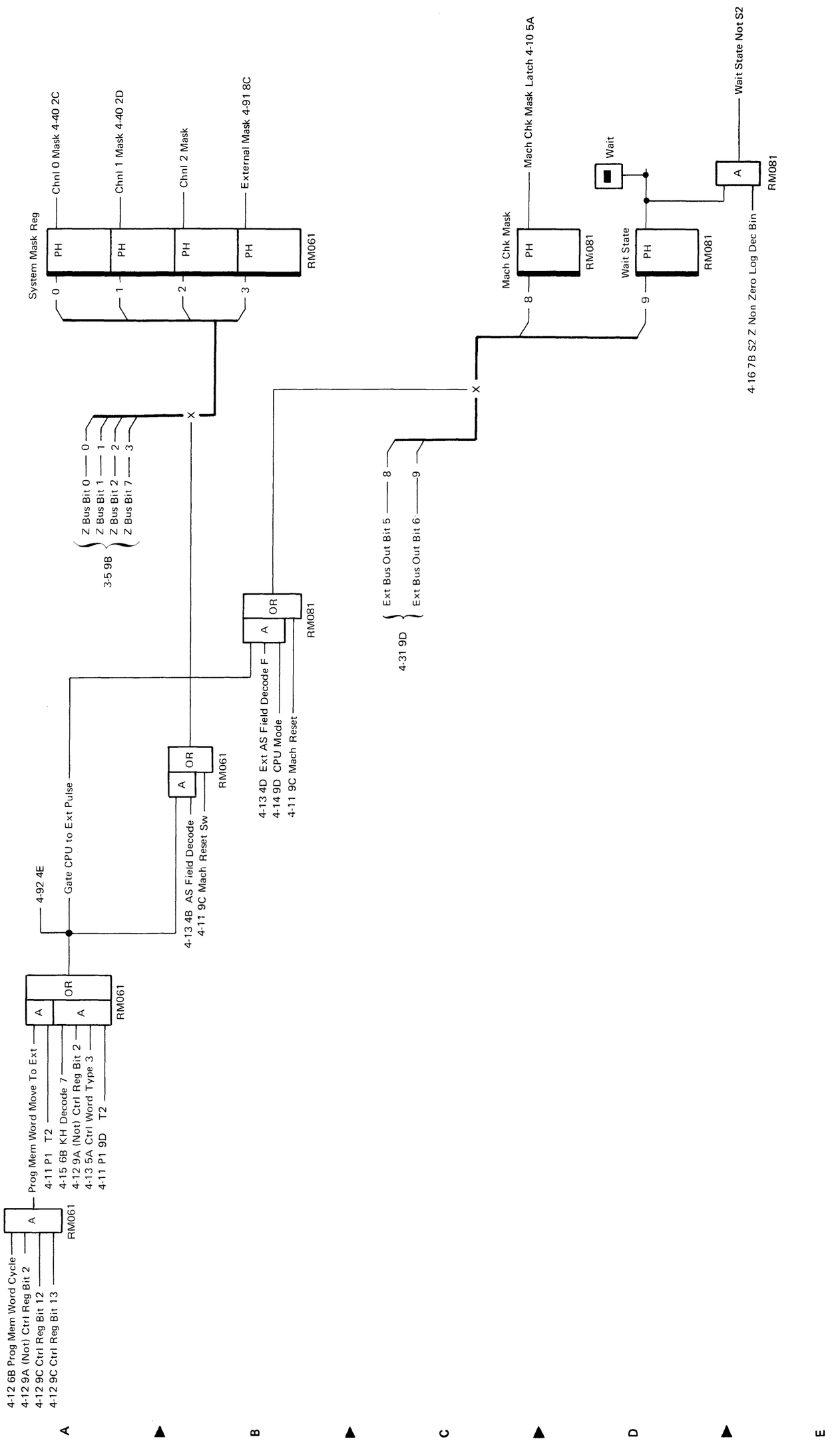
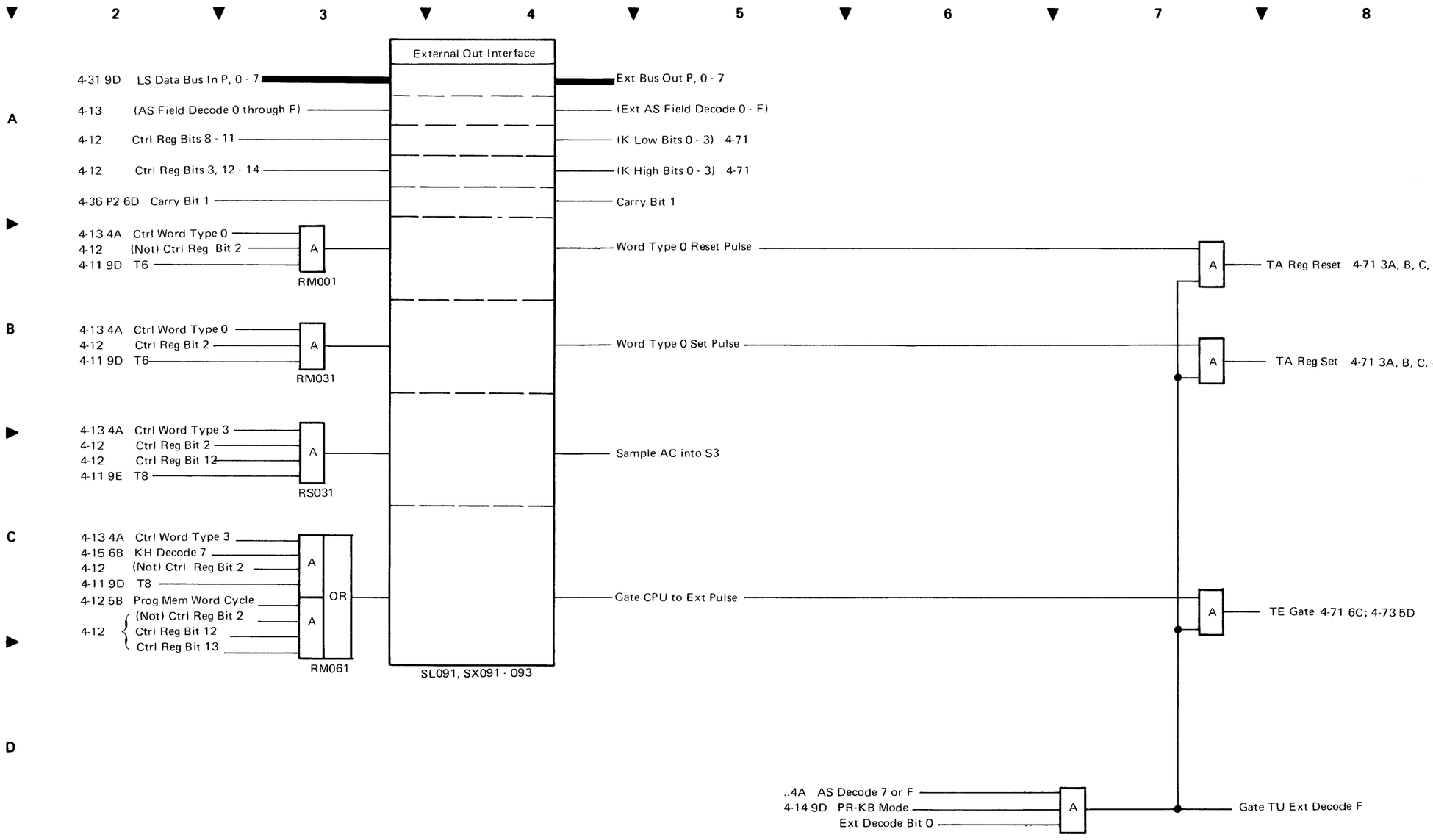


Diagram 4-50. System Mask, Mach Chk Mask, Wait State

Diagram 4-70. External Out Interface (PR-KB)



TA External Field
AS Decode=F

KH 0	Read Latch	Set / Rst
1	Write Latch	Set / Rst
2	Microforce Latch	Set / Rst
3	Alter-Display Active Latch	Set / Rst
KL 0	Spare	
1	TA Diag SS Set	Set
	TA Attach Rst	Rst
2	Initialize Prtr	Set
	Share Reset	Rst
3	Spare	Set
	Attention Rst	Rst

Kybd Read
4-70 8B TA Reg Set
4-70 4A K High 0
4-70 8B TA Reg Reset
4-75 4E Attach Rst
PF 131
Read L 4-75 6C, 4-73 4D, 4-73 5D,
(Not) Read Latch 4-72 3E; 4-73 8D

Prtr Write
4-70 8B TA Reg Set
4-70 4A K High 1
4-70 8B TA Reg Reset
4-75 4E Attach Rst
PF 131
Write L ..6C, 4-74 4D , 4-75 6B ..6D
(Not) Write Latch 4-72 3E

Microforce
4-70 8B TA Reg Set
4-70 4A K High 2
4-70 8B TA Reg Reset
4-75 4E Attach Rst
PF 131
(Not) Run Mode 4-72 3D, 5B
Microforce Int Stkd
Alt - Disp Active

PR-KB Alter Dplay
(On CPU Console)

Alt - Disp Act
4-70 8B TA Reg Set
4-70 4A K High 3
4-70 8B TA Reg Reset
4-75 4E Attach Rst
PF 131
Alt Disp Act L
4-72 5C

4-16 8D (Not) S7 Chnl 0 Interrupt Latch
Int Stkd Share
4-72 4D

Cycle Intlk
. . 8D (Not) Printer Busy
. . 8E (Not) RD-WR Share
. . 8D Printer Busy
. . 8C (Not) Data Ready L
4-75 4E Attach Rst
PF 031
Cycle Intlk L
. . 6C, 6D
4-72 5C
4-75 6B, 8B 7B
4-75 7D, 7C
(Not) Cycle Intlk L
4-75 5C

Data Ready
4-73 8C SS2
4-75 8B Shift Cycle L
. . 5A Write L
. . 8D (Not) Printer Busy
. . 8C Initil Prtr L
4-70 8D TE Gate
. . 8D Printer Busy
. . 8B Cycle Intlk L
4-75 4E Attach Rst
PF 031
Data Ready L
(Not) Data Ready L
. . 6B, . . 6E
. . 6D
4-75 3C

Initialize Prtr
4-75 5D T2 and Rst
. . 8D Printer Busy
. . 8B Cycle Intlk L
4-1 9C Machine Rst Sw
PF 031
Initil Prtr L
. . 6C, 4-73 6B, 4-75 3C
4-75 7C, 4-74 3E
(Not) Initil Prtr

Printer Busy
4-73 3B
Printer Busy Sw
4-73 3B
(Not) Printer Busy Sw
PF 041
Printer Busy
. . 6B, . . 6C, . . 6D,
4-73 7E, 4-75 3D
(Not) Printer Busy . . 6B, 4-75 5B
. . 6C

RD-WR Share
4-75 4E Attach Rst
PF 081
RD-WR Share Reg
4-72 3D
4-75 8A
(Not) RD-WR Share
4-75 6B
4-73 8D
. . 6B

TA Diag SS Set 4-73 4C
4-70 4A K LOW 1
4-70 8B TA Reg Set
4-70 8B TA Reg Reset
TA Attach Rst 4-75 3E

4-70 4A K LOW 2
Initil
4-75 5C U Case Store Latch
4-70 8B TA Reg Set
PF 141
Share
TA Share Rst 4-72 3A

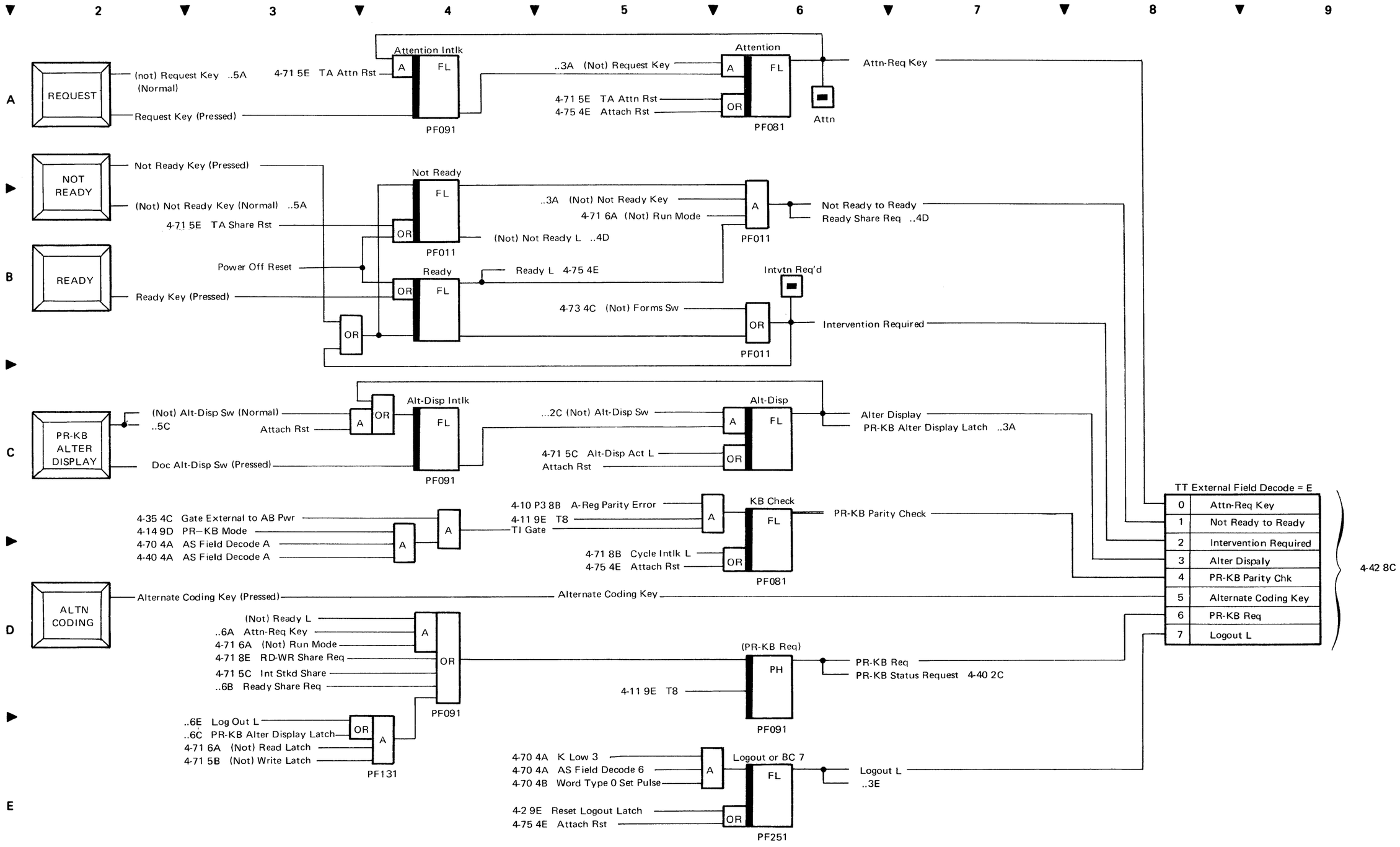
Attn
4-70 8B TA Reg Reset
4-70 4A K LOW 3
TA Attn Rst 4-72 4A, 5A

TU External Field
Decode = F

0	Read L
1	Write L
2	Microforce Int Stkd
3	Alt-Disp Active
4	Cycle Intlk L
5	Data Ready L
6	Initil Prtr L
7	Printer Busy

4-42 8D

Diagram 4-72. TT External Field (Branch Conditions)



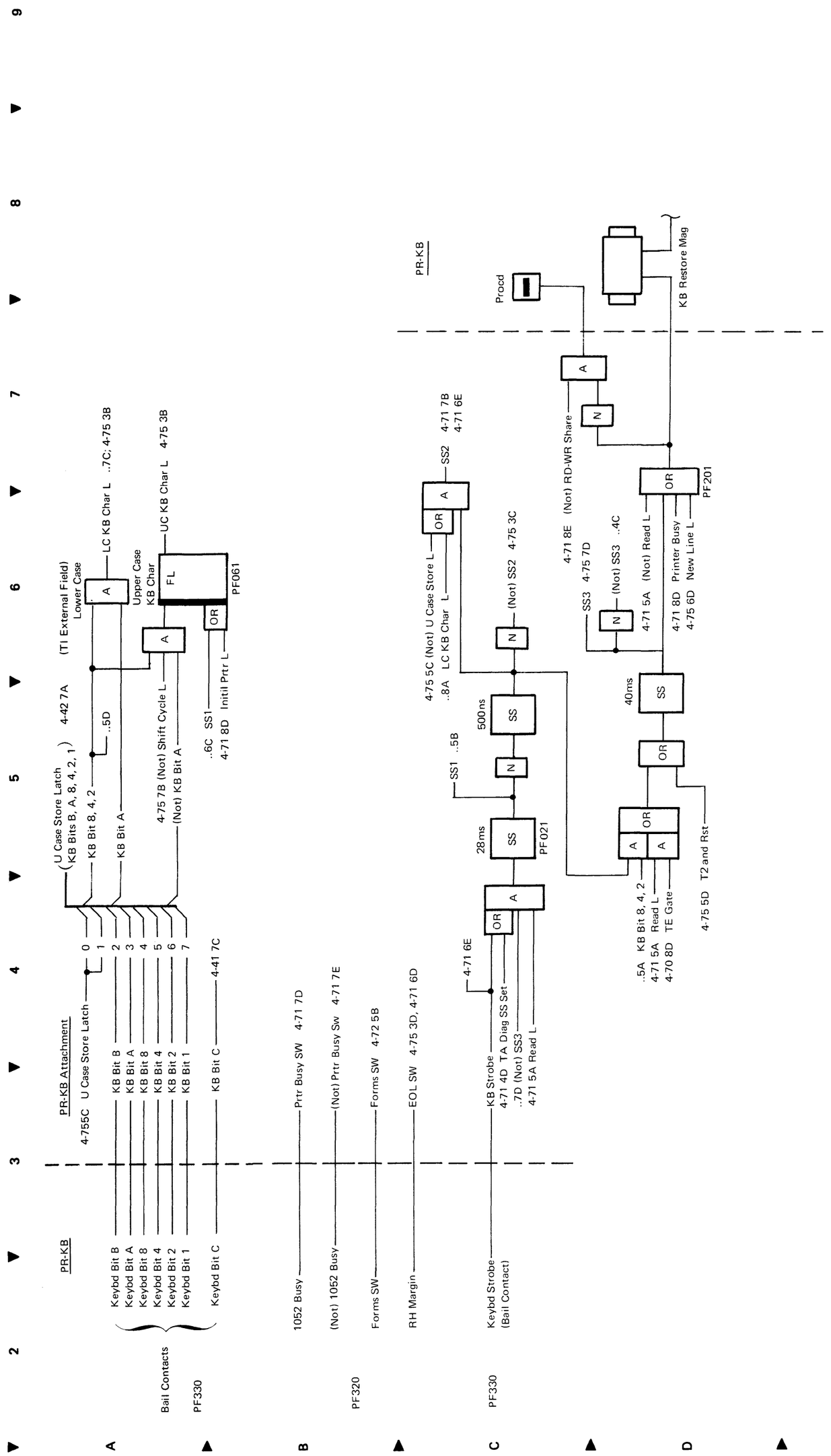
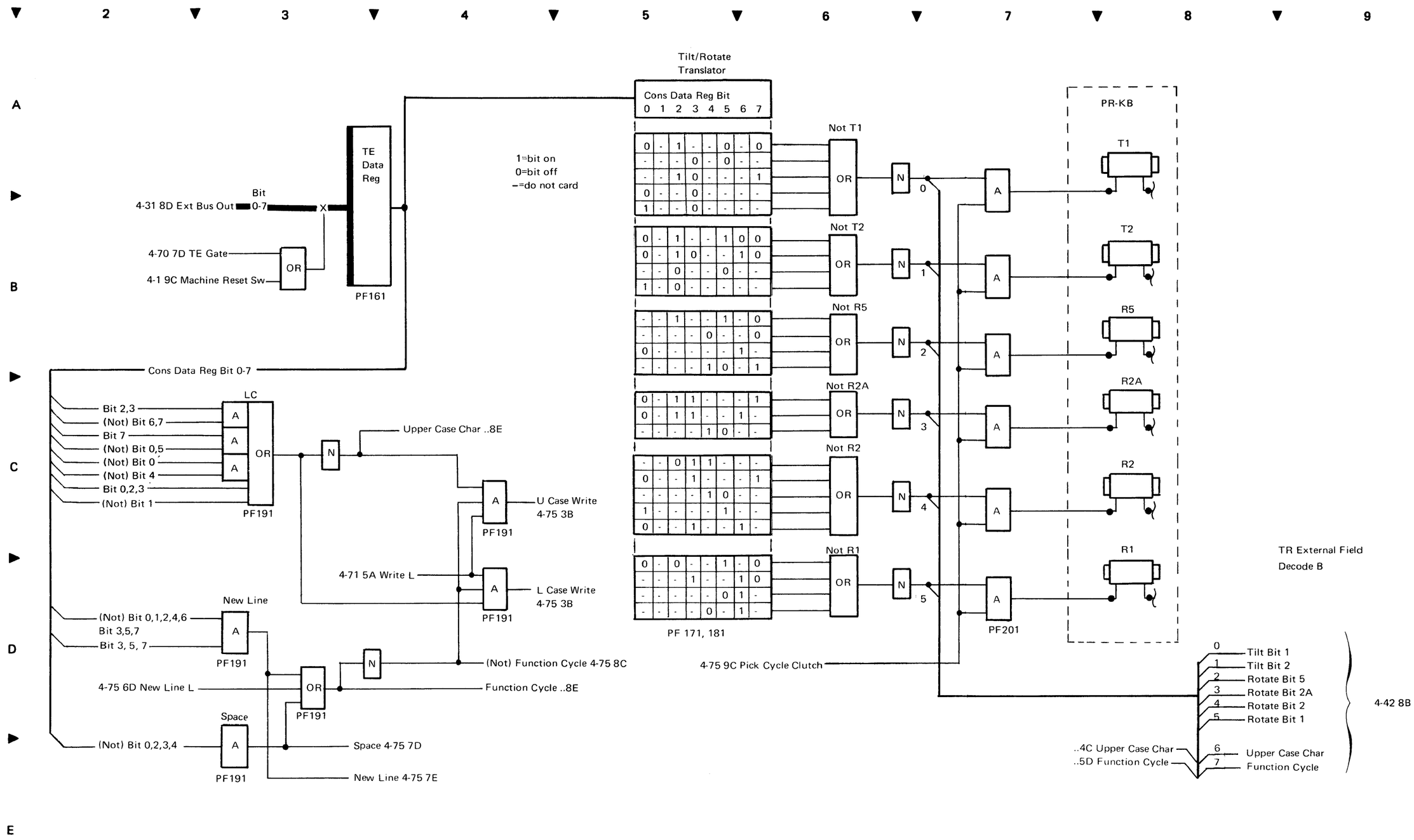


Diagram 4-73. TI External Field and Single Shots

Diagram 4-74. TE Data Reg, Tilt Rotate Translator, Function/Decode and TR External



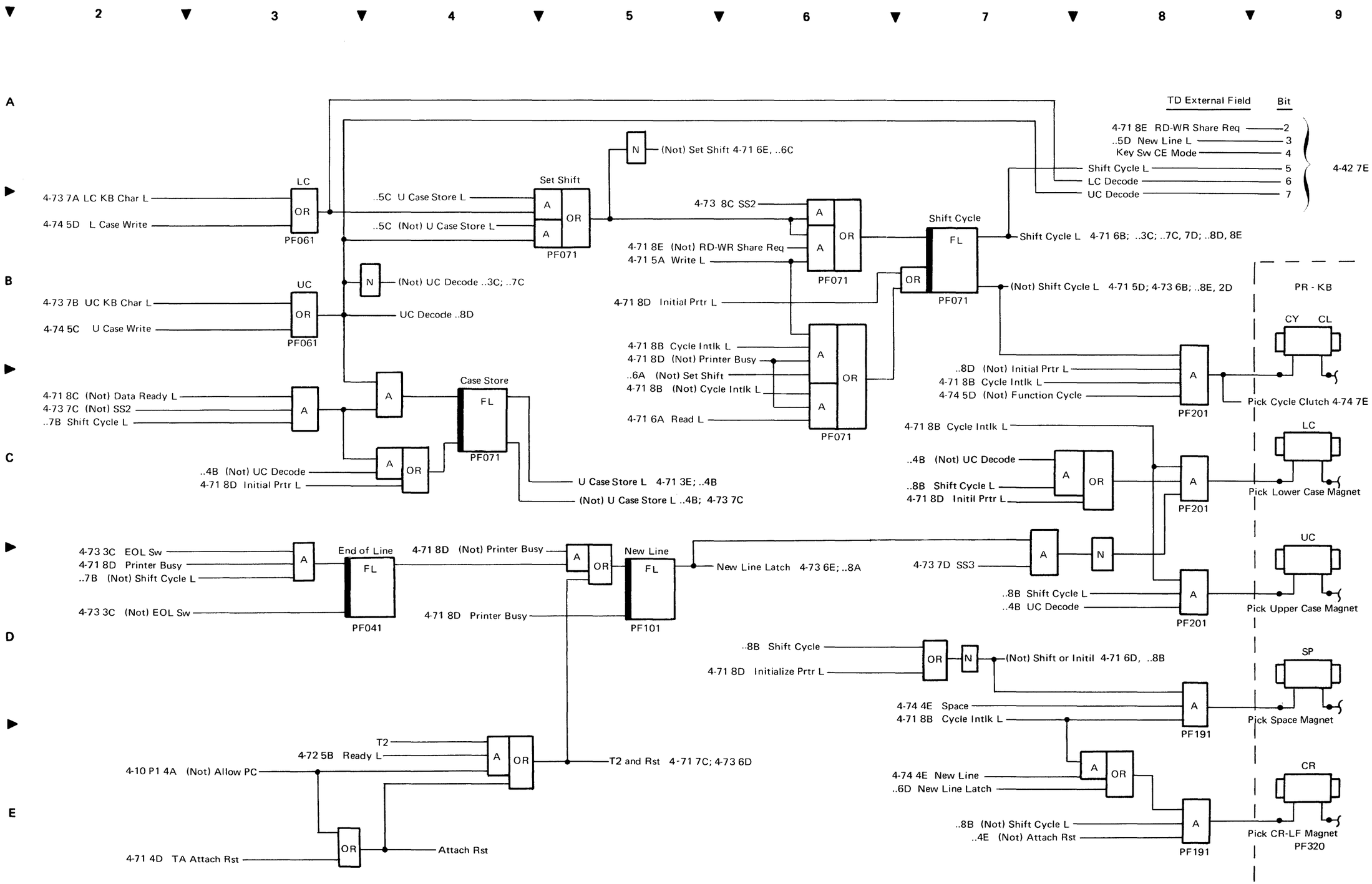
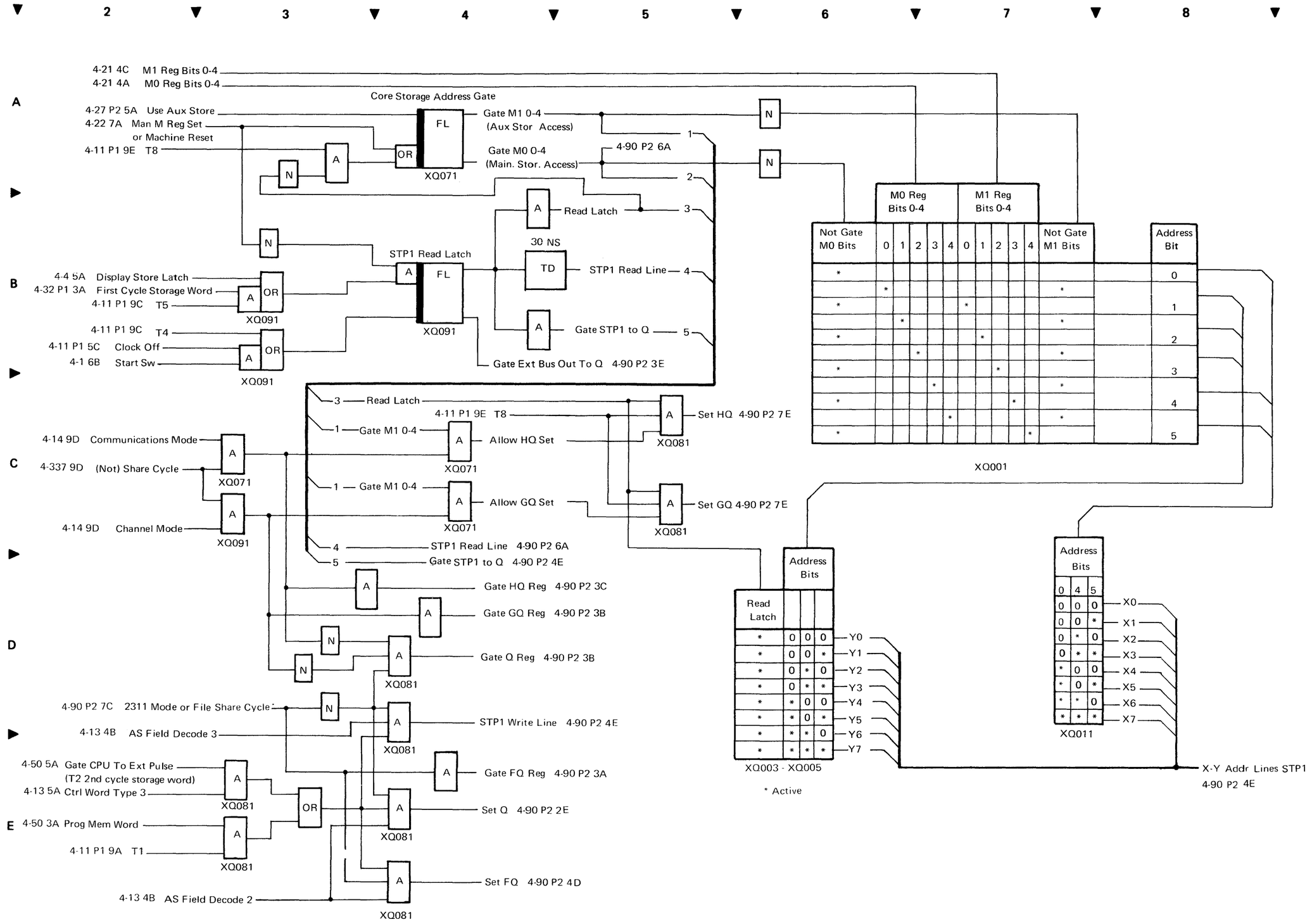

2
3
4
5
6
7
8
9
A
B
C
D
E
TD External Field
Bit
4-71 8E RD-WR Share Req
2
..5D New Line L
3
Key Sw CE Mode
4
Shift Cycle L
5
LC Decode
6
UC Decode
7
4-42 7E
4-73 7A LC KB Char L
4-74 5D L Case Write
LC
OR
PF061
..5C U Case Store L
..5C (Not) U Case Store L
Set Shift
A
OR
PF071
N
(Not) Set Shift 4-71 6E, ..6C
4-73 8C SS2
4-71 8E (Not) RD-WR Share Req
4-71 5A Write L
Shift Cycle
FL
PF071
Shift Cycle L 4-71 6B; ..3C; ..7C, 7D; ..8D, 8E
(Not) Shift Cycle L 4-71 5D; 4-73 6B; ..8E, 2D
4-73 7B UC KB Char L
4-74 5C U Case Write
UC
(Not) UC Decode ..3C; ..7C
UC Decode ..8D
4-71 8D Initial Prtr L
4-71 8B Cycle Intlk L
4-71 8D (Not) Printer Busy
..6A (Not) Set Shift
4-71 8B (Not) Cycle Intlk L
4-71 6A Read L
PR - KB
CY
CL
..8D (Not) Initial Prtr L
4-71 8B Cycle Intlk L
4-74 5D (Not) Function Cycle
PF201
Pick Cycle Clutch 4-74 7E
4-71 8C (Not) Data Ready L
4-73 7C (Not) SS2
..7B Shift Cycle L
Case Store
PF071
..4B (Not) UC Decode
4-71 8D Initial Prtr L
U Case Store L 4-71 3E; ..4B
(Not) U Case Store L ..4B; 4-73 7C
4-71 8B Cycle Intlk L
..4B (Not) UC Decode
..8B Shift Cycle L
4-71 8D Initil Prtr L
LC
Pick Lower Case Magnet
4-73 3C EOL Sw
4-71 8D Printer Busy
..7B (Not) Shift Cycle L
4-73 3C (Not) EOL Sw
End of Line
PF041
4-71 8D (Not) Printer Busy
New Line
PF101
New Line Latch 4-73 6E; ..8A
4-73 7D SS3
..8B Shift Cycle L
..4B UC Decode
UC
Pick Upper Case Magnet
..8B Shift Cycle
4-71 8D Initialize Prtr L
(Not) Shift or Initil 4-71 6D, ..8B
SP
4-74 4E Space
4-71 8B Cycle Intlk L
PF191
Pick Space Magnet
T2
4-72 5B Ready L
4-10 P1 4A (Not) Allow PC
T2 and Rst 4-71 7C; 4-73 6D
4-74 4E New Line
..6D New Line Latch
CR
..8B (Not) Shift Cycle L
..4E (Not) Attach Rst
Pick CR-LF Magnet
PF320
4-71 4D TA Attach Rst
Attach Rst

Diagram 4-90. Storage Protection (Part 1 of 2)



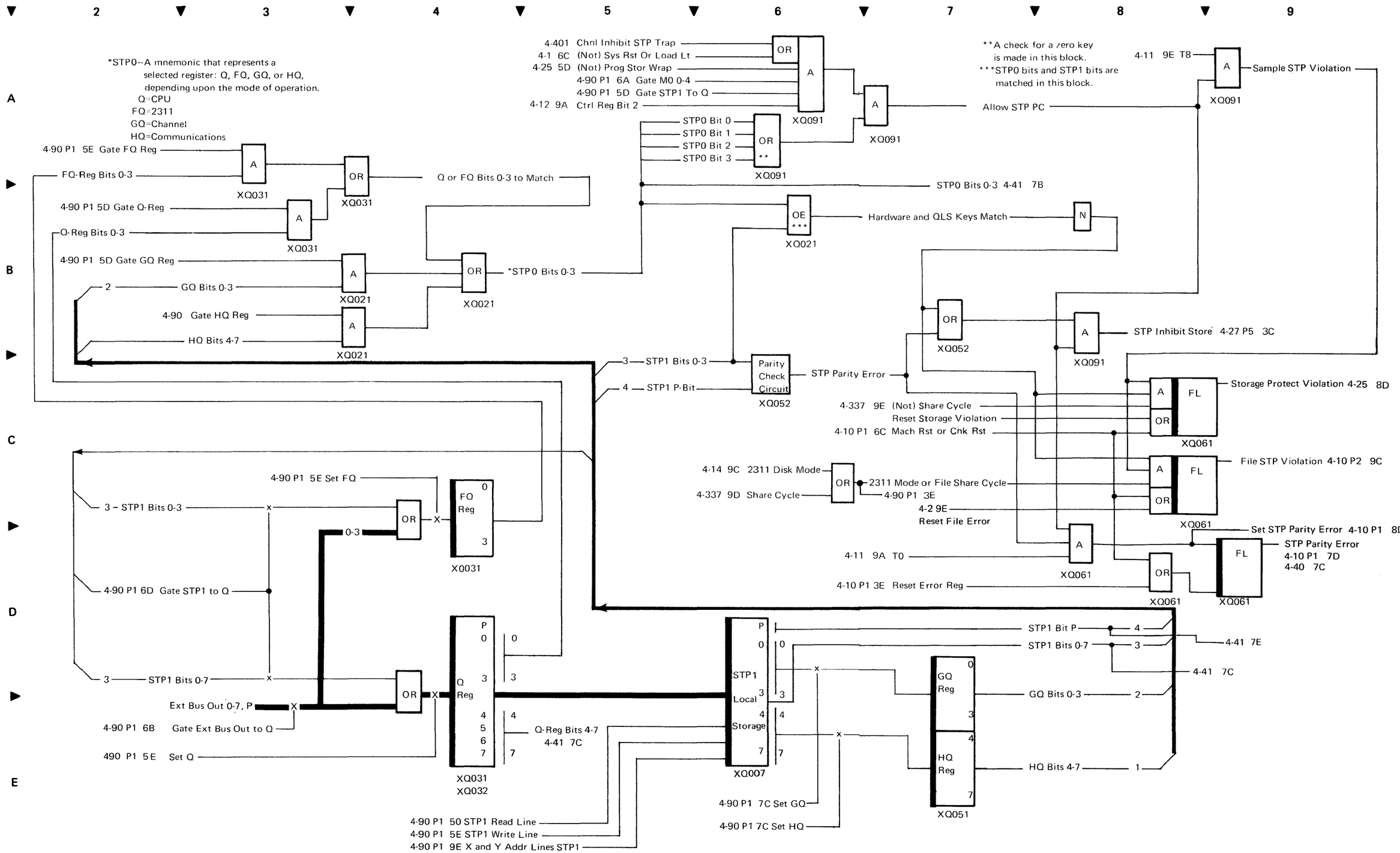
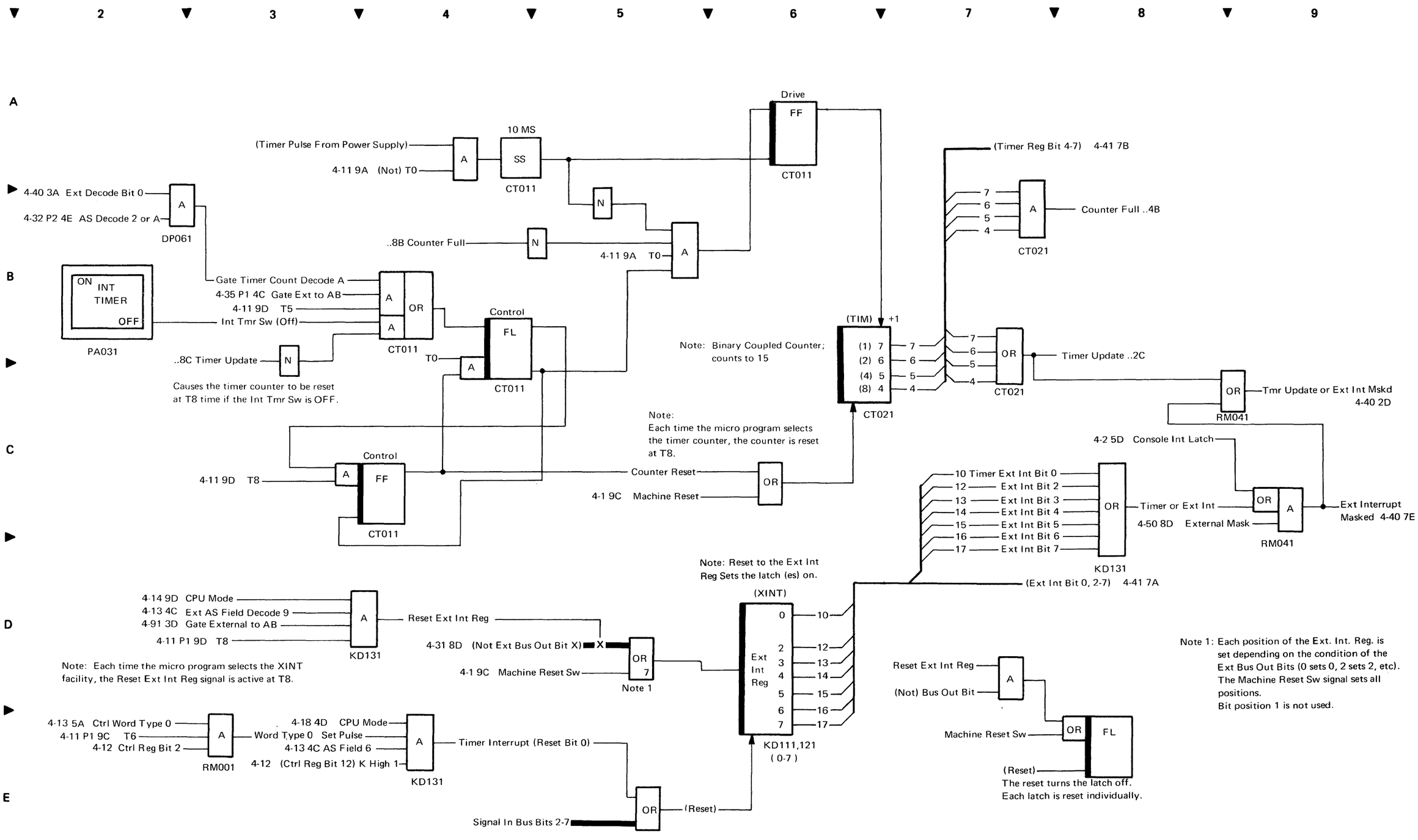

2
3
4
5
6
7
8
9
A
B
C
D
E
*STP0--A mnemonic that represents a selected register: Q, FQ, GQ, or HQ, depending upon the mode of operation.
Q=CPU
FQ=2311
GQ=Channel
HQ=Communications
**A check for a zero key is made in this block.
***STP0 bits and STP1 bits are matched in this block.
4-90 P1 5E Gate FQ Reg
FQ-Reg Bits 0-3
A
XQ031
OR
XQ031
Q or FQ Bits 0-3 to Match
4-90 P1 5D Gate Q-Reg
Q-Reg Bits 0-3
A
XQ031
4-90 P1 5D Gate GQ Reg
2
GQ Bits 0-3
A
XQ021
4-90 Gate HQ Reg
HQ Bits 4-7
A
XQ021
OR
XQ021
*STP0 Bits 0-3
4-401 Chnl Inhibit STP Trap
4-1 6C (Not) Sys Rst Or Load Lt
4-25 5D (Not) Prog Stor Wrap
4-90 P1 6A Gate M0 0-4
4-90 P1 5D Gate STP1 To Q
4-12 9A Ctrl Reg Bit 2
OR
A
XQ091
A
XQ091
Allow STP PC
STP0 Bit 0
STP0 Bit 1
STP0 Bit 2
STP0 Bit 3
OR
**
XQ091
STP0 Bits 0-3 4-41 7B
OE
***
XQ021
Hardware and QLS Keys Match
N
4-11 9E T8
A
XQ091
Sample STP Violation
3
STP1 Bits 0-3
4
STP1 P-Bit
Parity Check Circuit
XQ052
STP Parity Error
OR
XQ052
A
XQ091
STP Inhibit Store 4-27 P5 3C
4-337 9E (Not) Share Cycle
Reset Storage Violation
4-10 P1 6C Mach Rst or Chk Rst
A
OR
FL
XQ061
Storage Protect Violation 4-25 8D
4-14 9C 2311 Disk Mode
4-337 9D Share Cycle
OR
2311 Mode or File Share Cycle
4-90 P1 3E
4-2 9E
Reset File Error
A
OR
FL
XQ061
File STP Violation 4-10 P2 9C
4-11 9A T0
A
XQ061
Set STP Parity Error 4-10 P1 8D
STP Parity Error
4-10 P1 7D
4-40 7C
4-10 P1 3E Reset Error Reg
OR
XQ061
FL
XQ061
4-90 P1 5E Set FQ
3 - STP1 Bits 0-3
OR
0-3
FQ Reg
XQ0031
4-90 P1 6D Gate STP1 to Q
3
STP1 Bits 0-7
Ext Bus Out 0-7, P
4-90 P1 6B Gate Ext Bus Out to Q
490 P1 5E Set Q
OR
Q Reg
XQ031
XQ032
Q-Reg Bits 4-7
4-41 7C
STP1 Local Storage
XQ007
STP1 Bit P
STP1 Bits 0-7
4-41 7E
4-41 7C
GQ Reg
GQ Bits 0-3
HQ Reg
HQ Bits 4-7
XQ051
4-90 P1 7C Set GQ
4-90 P1 7C Set HQ
4-90 P1 50 STP1 Read Line
4-90 P1 5E STP1 Write Line
4-90 P1 9E X and Y Addr Lines STP1

Diagram 4-91. Interval Timer, External Interrupt Register



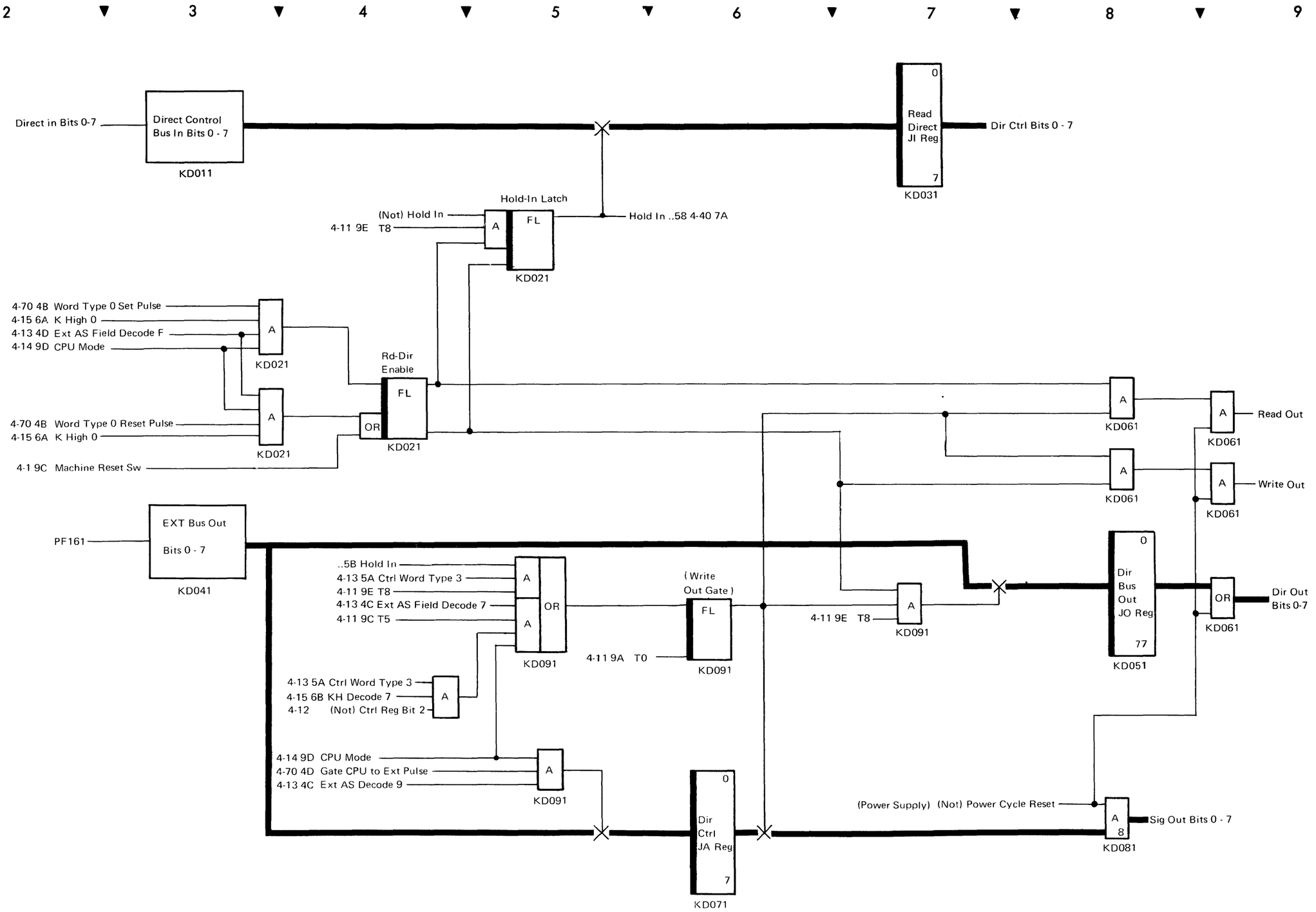
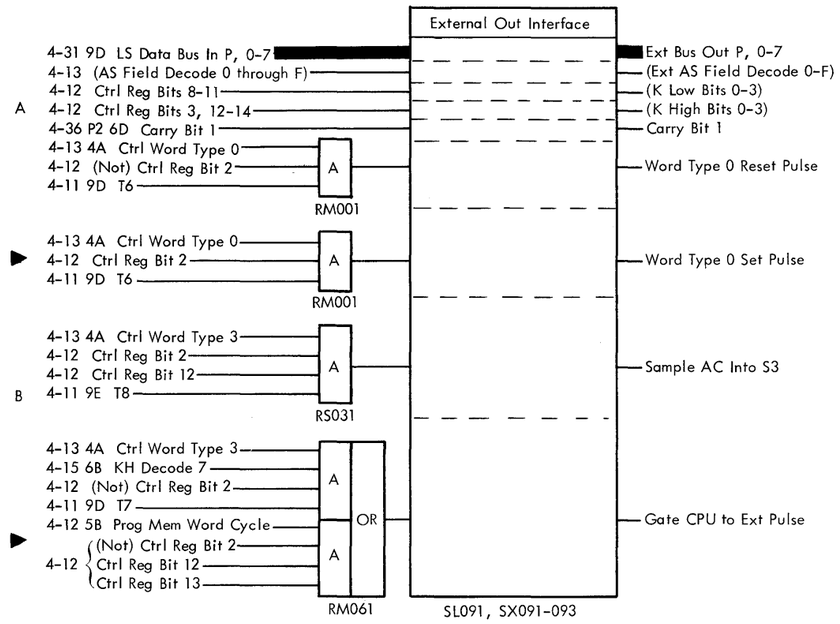

2
3
4
5
6
7
8
9
A
B
C
D
E
Direct in Bits 0-7
Direct Control Bus In Bits 0 - 7
KD011
0
Read Direct JI Reg
7
KD031
Dir Ctrl Bits 0 - 7
Hold-In Latch
(Not) Hold In
4-11 9E T8
A
FL
KD021
Hold In ..58 4-40 7A
4-70 4B Word Type 0 Set Pulse
4-15 6A K High 0
4-13 4D Ext AS Field Decode F
4-14 9D CPU Mode
A
KD021
Rd-Dir Enable
FL
4-70 4B Word Type 0 Reset Pulse
4-15 6A K High 0
A
KD021
OR
KD021
4-1 9C Machine Reset Sw
A
KD061
A
Read Out
KD061
A
KD061
A
Write Out
KD061
PF161
EXT Bus Out
Bits 0 - 7
KD041
..5B Hold In
4-13 5A Ctrl Word Type 3
4-11 9E T8
4-13 4C Ext AS Field Decode 7
4-11 9C T5
A
A
OR
KD091
(Write Out Gate)
FL
4-11 9A T0
KD091
4-11 9E T8
A
KD091
0
Dir Bus Out JO Reg
77
KD051
OR
Dir Out Bits 0-7
KD061
4-13 5A Ctrl Word Type 3
4-15 6B KH Decode 7
4-12 (Not) Ctrl Reg Bit 2
A
4-14 9D CPU Mode
4-70 4D Gate CPU to Ext Pulse
4-13 4C Ext AS Decode 9
A
KD091
0
Dir Ctrl JA Reg
7
KD071
(Power Supply) (Not) Power Cycle Reset
A
8
KD081
Sig Out Bits 0 - 7

Diagram 4-100. External Out Interface (2540)



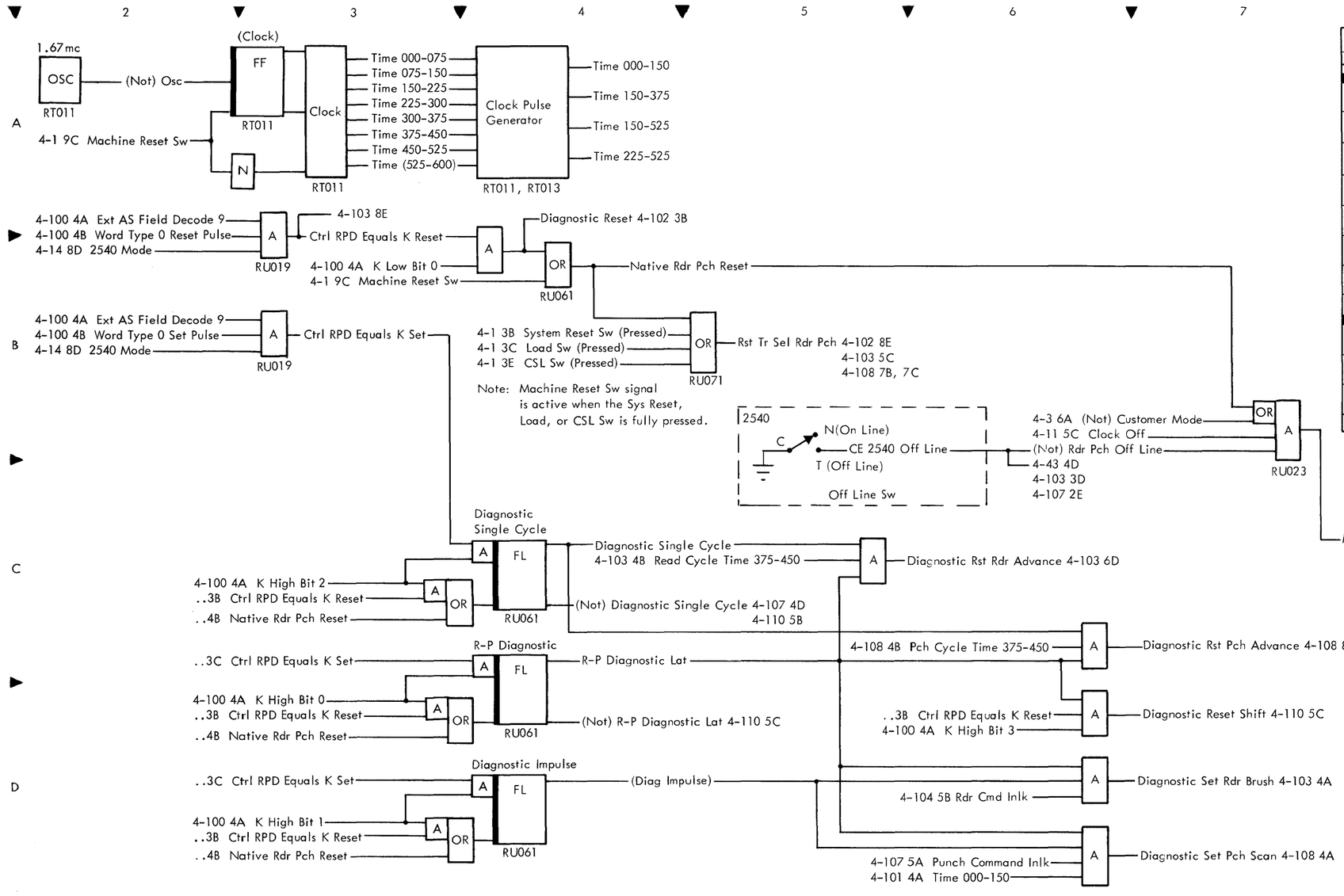
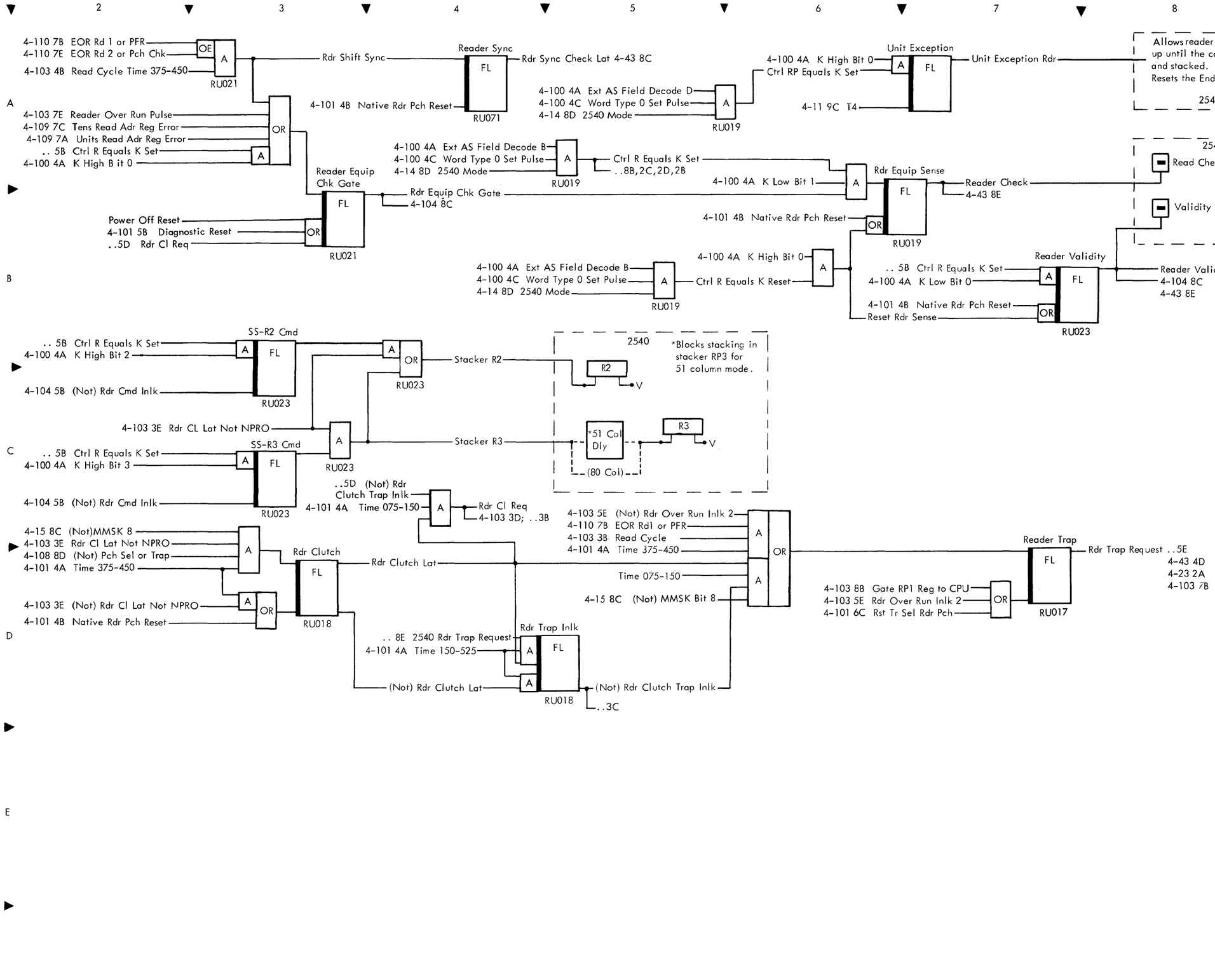
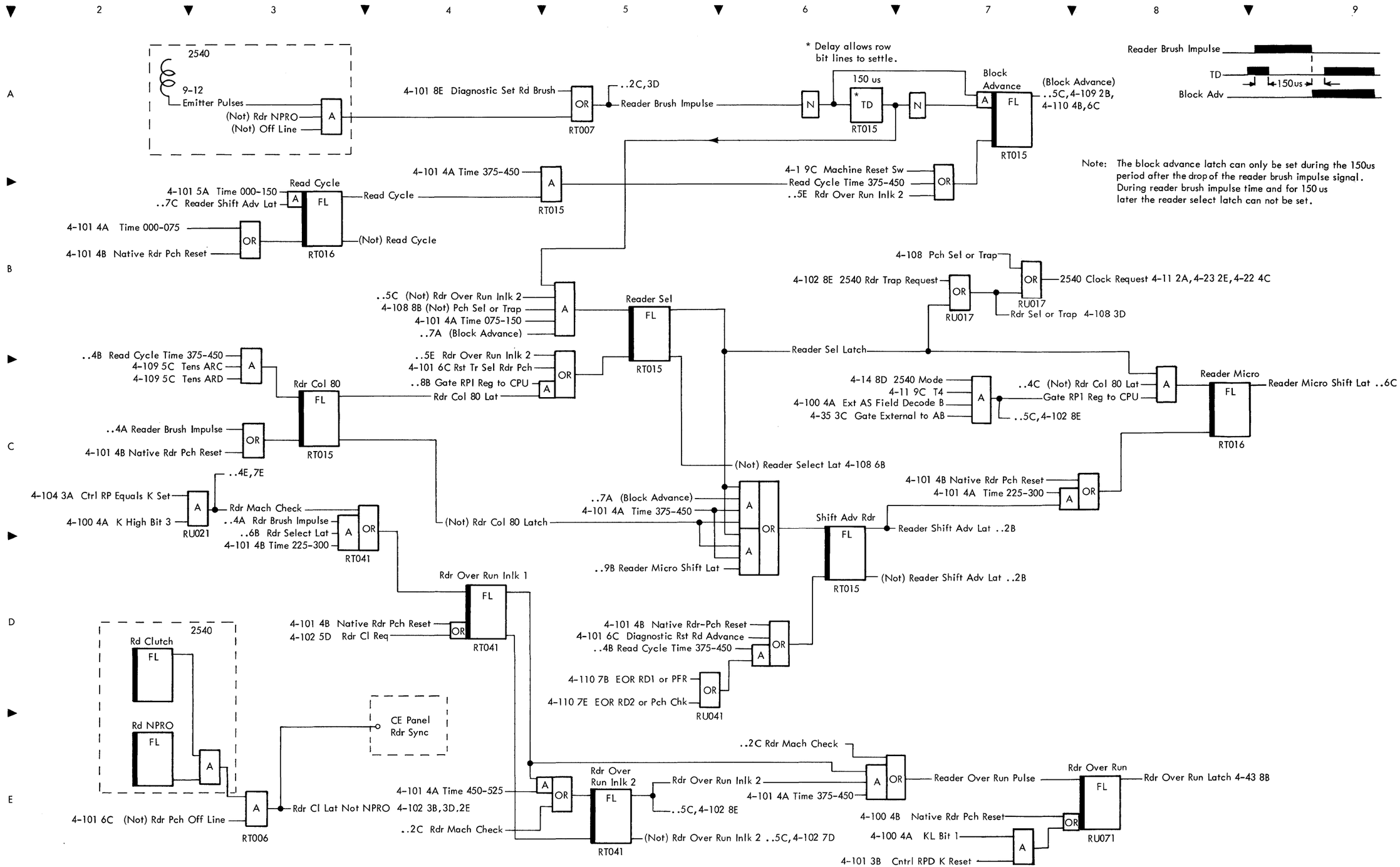
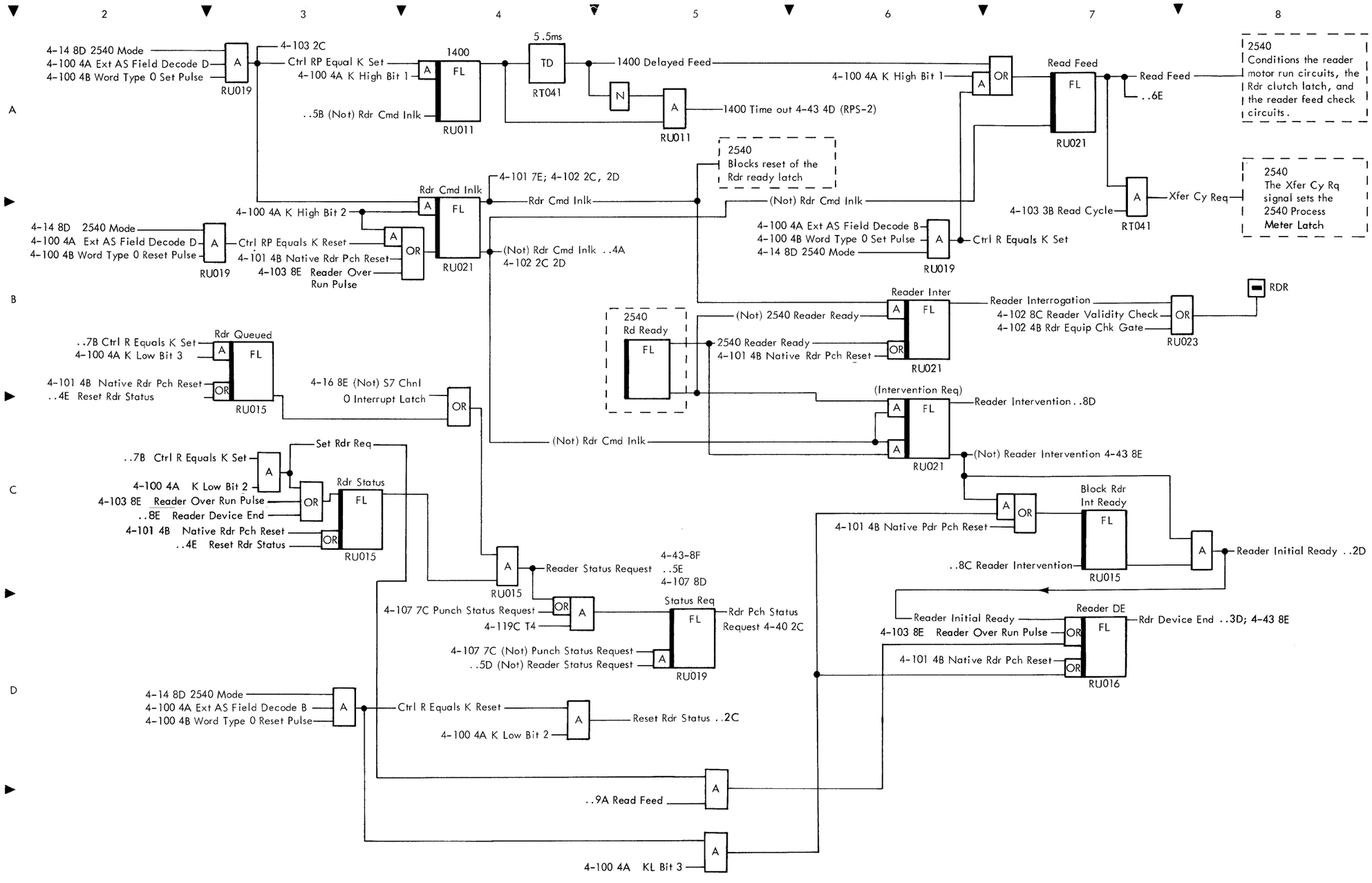

2
3
4
5
6
7
8
9
A
B
C
D
E
1.67mc
OSC
RT011
(Not) Osc
(Clock)
FF
RT011
Clock
RT011
Time 000-075
Time 075-150
Time 150-225
Time 225-300
Time 300-375
Time 375-450
Time 450-525
Time (525-600)
Clock Pulse Generator
RT011, RT013
Time 000-150
Time 150-375
Time 150-525
Time 225-525
4-1 9C Machine Reset Sw
N
4-100 4A Ext AS Field Decode 9
4-100 4B Word Type 0 Reset Pulse
4-14 8D 2540 Mode
A
RU019
4-103 8E
Ctrl RPD Equals K Reset
4-100 4A K Low Bit 0
4-1 9C Machine Reset Sw
A
Diagnostic Reset 4-102 3B
OR
RU061
Native Rdr Pch Reset
4-100 4A Ext AS Field Decode 9
4-100 4B Word Type 0 Set Pulse
4-14 8D 2540 Mode
A
RU019
Ctrl RPD Equals K Set
4-1 3B System Reset Sw (Pressed)
4-1 3C Load Sw (Pressed)
4-1 3E CSL Sw (Pressed)
OR
RU071
Rst Tr Sel Rdr Pch 4-102 8E
4-103 5C
4-108 7B, 7C
Note: Machine Reset Sw signal is active when the Sys Reset, Load, or CSL Sw is fully pressed.
2540
C
N(On Line)
CE 2540 Off Line
T (Off Line)
Off Line Sw
4-3 6A (Not) Customer Mode
4-11 5C Clock Off
(Not) Rdr Pch Off Line
4-43 4D
4-103 3D
4-107 2E
OR
A
RU023
Mach Reset Rdr Pch
2540
Mach Reset Rdr
Mach Reset Pch
Power On Reset
Power On Reset
0
75
150
225
300
375
450
525
0
4.8us.
.6us.
Clock is operating as long as power is on. The first position to turn on, after machine reset, is 000-075.
Diagnostic Single Cycle
A
FL
RU061
Diagnostic Single Cycle
4-103 4B Read Cycle Time 375-450
A
Diagnostic Rst Rdr Advance 4-103 6D
4-100 4A K High Bit 2
..3B Ctrl RPD Equals K Reset
..4B Native Rdr Pch Reset
A
OR
(Not) Diagnostic Single Cycle 4-107 4D
4-110 5B
R-P Diagnostic
..3C Ctrl RPD Equals K Set
A
FL
RU061
R-P Diagnostic Lat
4-108 4B Pch Cycle Time 375-450
A
Diagnostic Rst Pch Advance 4-108 8D
4-100 4A K High Bit 0
..3B Ctrl RPD Equals K Reset
..4B Native Rdr Pch Reset
A
OR
(Not) R-P Diagnostic Lat 4-110 5C
..3B Ctrl RPD Equals K Reset
4-100 4A K High Bit 3
A
Diagnostic Reset Shift 4-110 5C
Diagnostic Impulse
..3C Ctrl RPD Equals K Set
A
FL
RU061
(Diag Impulse)
4-104 5B Rdr Cmd Inlk
A
Diagnostic Set Rdr Brush 4-103 4A
4-100 4A K High Bit 1
..3B Ctrl RPD Equals K Reset
..4B Native Rdr Pch Reset
A
OR
4-107 5A Punch Command Inlk
4-101 4A Time 000-150
A
Diagnostic Set Pch Scan 4-108 4A

Diagram 4-102. Reader Checks, Stacker Select and Reader Traps




2 3 4 5 6 7 8 9
A B C D E
2540
9-12
Emitter Pulses
(Not) Rdr NPRO
(Not) Off Line
A
4-101 8E Diagnostic Set Rd Brush
OR
RT007
..2C,3D
Reader Brush Impulse
* Delay allows row bit lines to settle.
N
150 us
* TD
RT015
N
Block Advance
A
FL
RT015
(Block Advance) ..5C,4-109 2B, 4-110 4B,6C
Reader Brush Impulse
TD
150us
Block Adv
Note: The block advance latch can only be set during the 150us period after the drop of the reader brush impulse signal. During reader brush impulse time and for 150 us later the reader select latch can not be set.
4-101 4A Time 375-450
A
RT015
4-1 9C Machine Reset Sw
Read Cycle Time 375-450
..5E Rdr Over Run Inlk 2
OR
Read Cycle
4-101 5A Time 000-150
..7C Reader Shift Adv Lat
A
FL
RT016
(Not) Read Cycle
4-101 4A Time 000-075
4-101 4B Native Rdr Pch Reset
OR
..5C (Not) Rdr Over Run Inlk 2
4-108 8B (Not) Pch Sel or Trap
4-101 4A Time 075-150
..7A (Block Advance)
A
Reader Sel
FL
RT015
4-108 Pch Sel or Trap
4-102 8E 2540 Rdr Trap Request
OR
RU017
OR
RU017
2540 Clock Request 4-11 2A,4-23 2E,4-22 4C
Rdr Sel or Trap 4-108 3D
..4B Read Cycle Time 375-450
4-109 5C Tens ARC
4-109 5C Tens ARD
A
..5E Rdr Over Run Inlk 2
4-101 6C Rst Tr Sel Rdr Pch
..8B Gate RPI Reg to CPU
A
OR
Rdr Col 80
FL
RT015
Rdr Col 80 Lat
Reader Sel Latch
4-14 8D 2540 Mode
4-11 9C T4
4-100 4A Ext AS Field Decode B
4-35 3C Gate External to AB
A
..4C (Not) Rdr Col 80 Lat
Gate RP1 Reg to CPU
..5C,4-102 8E
A
Reader Micro
FL
RT016
Reader Micro Shift Lat ..6C
..4A Reader Brush Impulse
4-101 4B Native Rdr Pch Reset
OR
RT015
..4E,7E
(Not) Reader Select Lat 4-108 6B
4-104 3A Ctrl RP Equals K Set
4-100 4A K High Bit 3
A
RU021
Rdr Mach Check
..4A Rdr Brush Impulse
..6B Rdr Select Lat
4-101 4B Time 225-300
A
OR
RT041
(Not) Rdr Col 80 Latch
..7A (Block Advance)
4-101 4A Time 375-450
A
A
OR
..9B Reader Micro Shift Lat
Shift Adv Rdr
FL
RT015
Reader Shift Adv Lat ..2B
(Not) Reader Shift Adv Lat ..2B
4-101 4B Native Rdr Pch Reset
4-101 4A Time 225-300
A
OR
Rdr Over Run Inlk 1
FL
RT041
4-101 4B Native Rdr Pch Reset
4-102 5D Rdr Cl Req
OR
4-101 4B Native Rdr-Pch Reset
4-101 6C Diagnostic Rst Rd Advance
..4B Read Cycle Time 375-450
A
OR
4-110 7B EOR RD1 or PFR
4-110 7E EOR RD2 or Pch Chk
OR
RU041
2540
Rd Clutch
FL
Rd NPRO
FL
A
CE Panel
Rdr Sync
..2C Rdr Mach Check
Rdr Over Run Inlk 2
4-101 4A Time 450-525
A
OR
FL
RT041
Rdr Over Run Inlk 2
4-101 4A Time 375-450
A
OR
Reader Over Run Pulse
Rdr Over Run
FL
RU071
Rdr Over Run Latch 4-43 8B
..5C,4-102 8E
4-100 4B Native Rdr Pch Reset
OR
4-100 4A KL Bit 1
4-101 3B Cntrl RPD K Reset
A
4-101 6C (Not) Rdr Pch Off Line
A
RT006
Rdr Cl Lat Not NPRO 4-102 3B,3D,2E
..2C Rdr Mach Check
(Not) Rdr Over Run Inlk 2 ..5C,4-102 7D


2
3
4
5
6
7
8
A
B
C
D
E
4-14 8D 2540 Mode
4-100 4A Ext AS Field Decode D
4-100 4B Word Type 0 Set Pulse
RU019
4-103 2C
Ctrl RP Equal K Set
4-100 4A K High Bit 1
1400
FL
RU011
..5B (Not) Rdr Cmd Inlk
5.5ms
TD
RT041
1400 Delayed Feed
N
1400 Time out 4-43 4D (RPS-2)
4-100 4A K High Bit 1
OR
Read Feed
RU021
Read Feed
..6E
2540
Conditions the reader motor run circuits, the Rdr clutch latch, and the reader feed check circuits.
2540
Blocks reset of the Rdr ready latch
4-101 7E; 4-102 2C, 2D
Rdr Cmd Inlk
4-100 4A K High Bit 2
4-14 8D 2540 Mode
4-100 4A Ext AS Field Decode D
4-100 4B Word Type 0 Reset Pulse
Ctrl RP Equals K Reset
4-101 4B Native Rdr Pch Reset
4-103 8E Reader Over Run Pulse
(Not) Rdr Cmd Inlk ..4A
4-102 2C 2D
(Not) Rdr Cmd Inlk
4-100 4A Ext AS Field Decode B
4-100 4B Word Type 0 Set Pulse
4-14 8D 2540 Mode
Ctrl R Equals K Set
4-103 3B Read Cycle
Xfer Cy Req
RT041
2540
The Xfer Cy Rq signal sets the 2540 Process Meter Latch
Reader Inter
Reader Interrogation
4-102 8C Reader Validity Check
4-102 4B Rdr Equip Chk Gate
RU023
RDR
2540
Rd Ready
(Not) 2540 Reader Ready
2540 Reader Ready
4-101 4B Native Rdr Pch Reset
..7B Ctrl R Equals K Set
4-100 4A K Low Bit 3
Rdr Queued
4-101 4B Native Rdr Pch Reset
..4E Reset Rdr Status
RU015
4-16 8E (Not) S7 Chnl 0 Interrupt Latch
(Intervention Req)
Reader Intervention ..8D
(Not) Reader Intervention 4-43 8E
..7B Ctrl R Equals K Set
4-100 4A K Low Bit 2
4-103 8E Reader Over Run Pulse
..8E Reader Device End
4-101 4B Native Rdr Pch Reset
..4E Reset Rdr Status
Set Rdr Req
Rdr Status
RU015
Block Rdr Int Ready
4-101 4B Native Pdr Pch Reset
..8C Reader Intervention
Reader Initial Ready ..2D
Reader Initial Ready
4-103 8E Reader Over Run Pulse
4-101 4B Native Rdr Pch Reset
Reader DE
Rdr Device End ..3D; 4-43 8E
RU016
Reader Status Request
4-43-8F ..5E 4-107 8D
4-107 7C Punch Status Request
4-119C T4
Status Req
Rdr Pch Status Request 4-40 2C
4-107 7C (Not) Punch Status Request
..5D (Not) Reader Status Request
RU019
4-14 8D 2540 Mode
4-100 4A Ext AS Field Decode B
4-100 4B Word Type 0 Reset Pulse
Ctrl R Equals K Reset
4-100 4A K Low Bit 2
Reset Rdr Status ..2C
..9A Read Feed
4-100 4A KL Bit 3

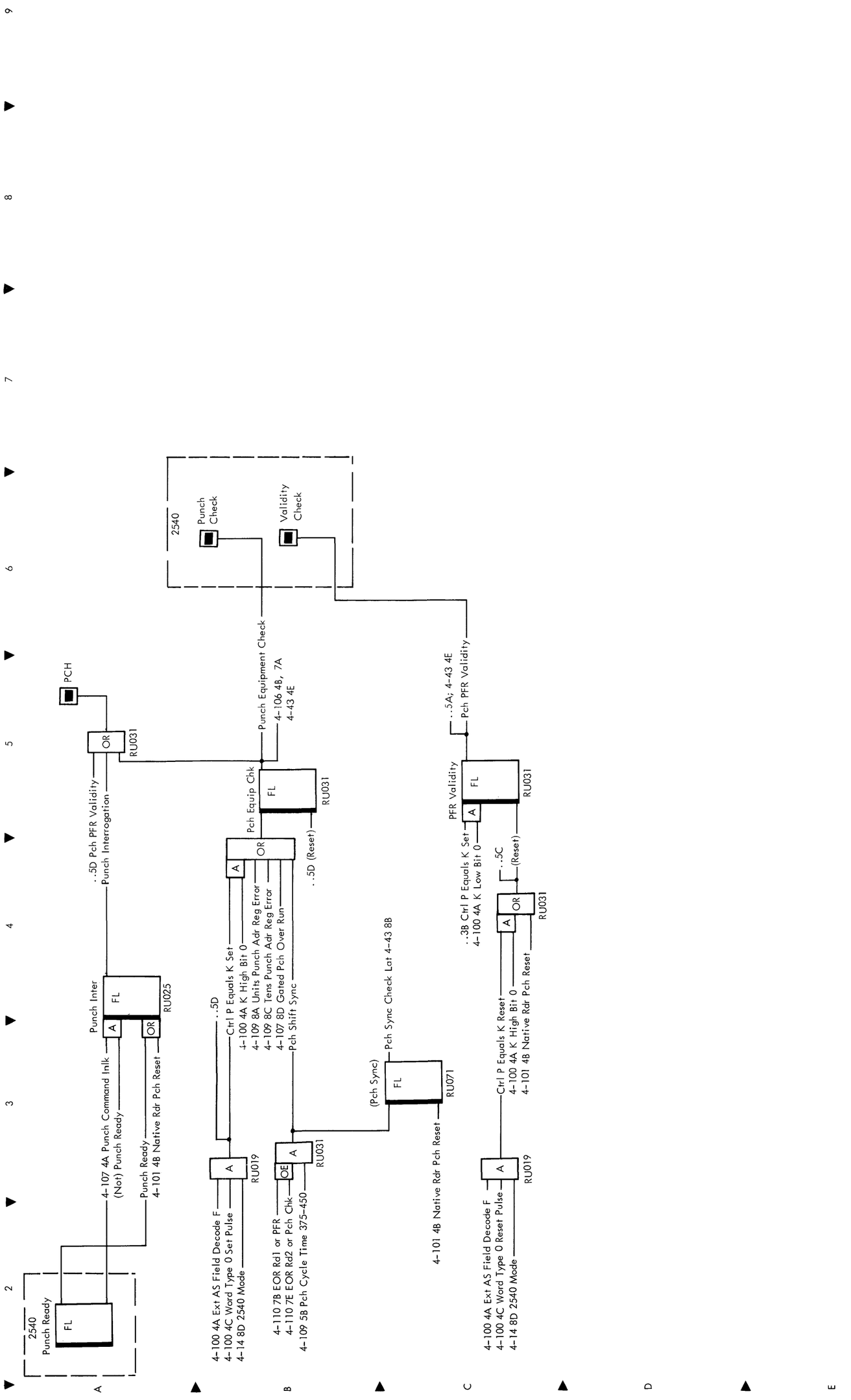
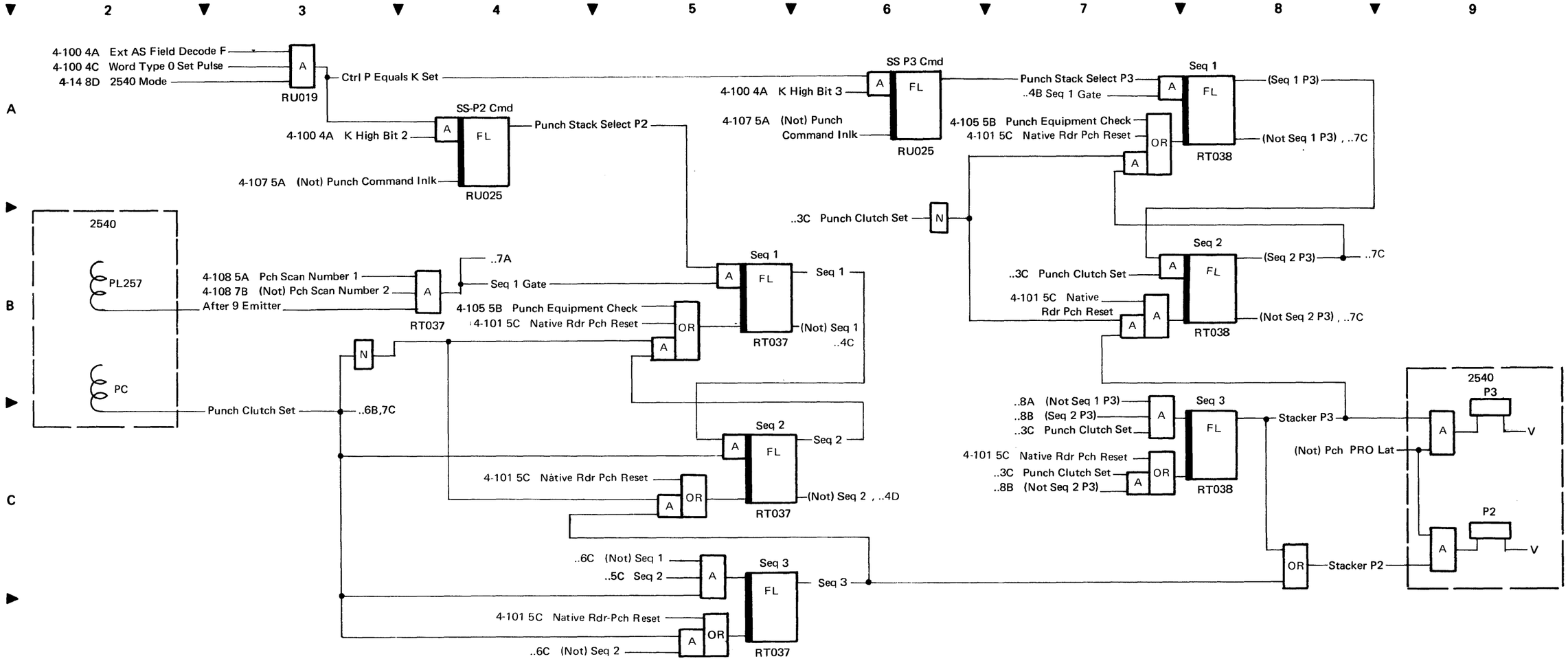


Diagram 4-105. Punch Checks

Diagram 4-106. Punch Stacker Selector



Cycle		Punch				Check				Stack			
Punch Timing		9	117	226	315	9	117	226	315	9	117	226	
1	Punch Clutch Set	22	112	202	292	22	112	202	292	22	112	202	292
2	After 9 Emitter			257				257				257	
3	Sequence 1 Lat							2					
4	Sequence 2 Lat												
5	Sequence 3 Lat												
6	Stacker Magnet												
7	Stacker Px Cmd												

Punch Cmd — (Stacker info held one cycle by micro)

Reset by next Pch Cmd — 52° Card at chute blade

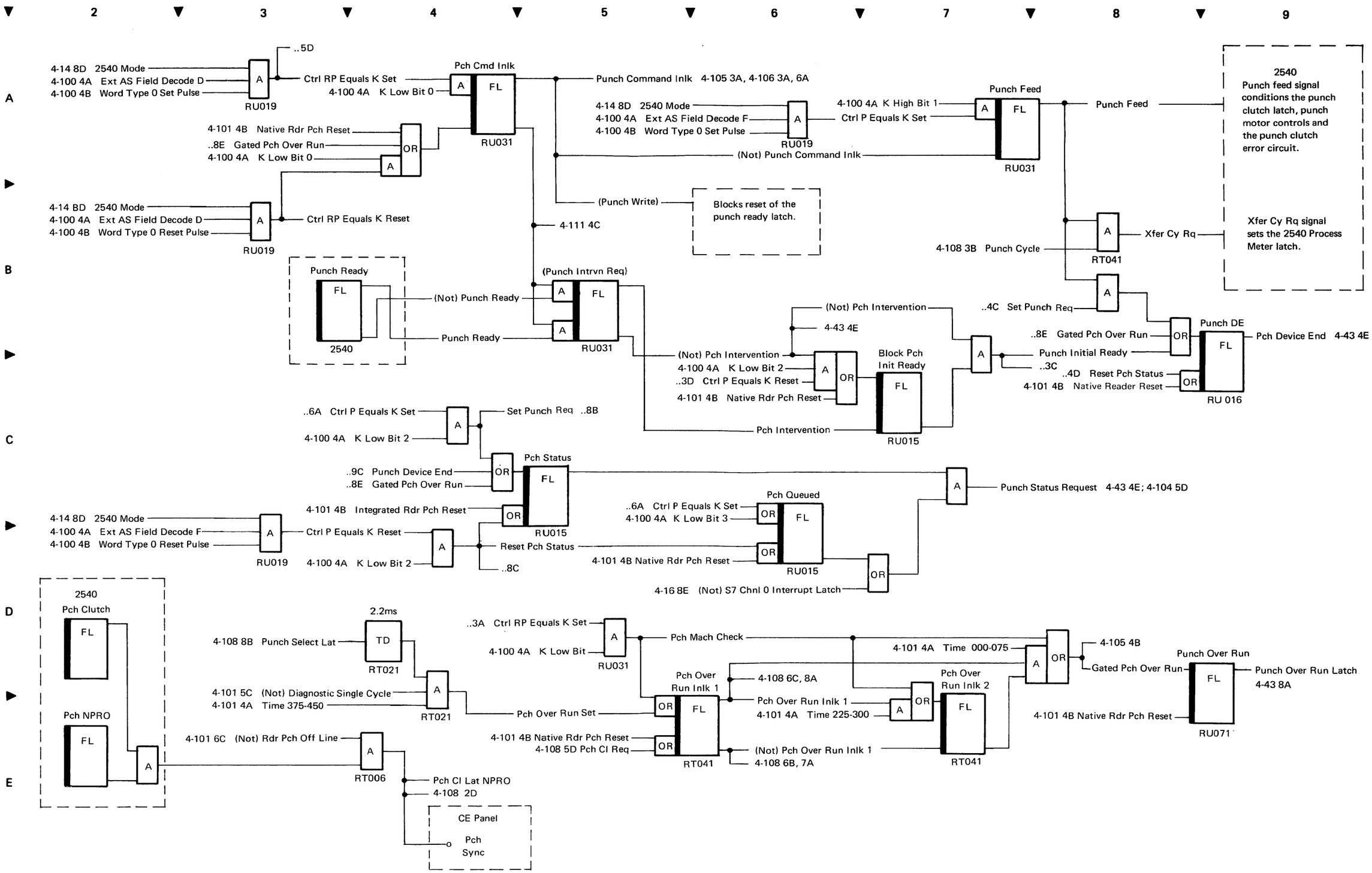

2
3
4
5
6
7
8
9
A
B
C
D
E
4-14 8D 2540 Mode
4-100 4A Ext AS Field Decode D
4-100 4B Word Type 0 Set Pulse
A
RU019
..5D
Ctrl RP Equals K Set
4-100 4A K Low Bit 0
Pch Cmd Inlk
A
FL
RU031
Punch Command Inlk 4-105 3A, 4-106 3A, 6A
4-101 4B Native Rdr Pch Reset
..8E Gated Pch Over Run
4-100 4A K Low Bit 0
OR
A
4-14 8D 2540 Mode
4-100 4A Ext AS Field Decode F
4-100 4B Word Type 0 Set Pulse
A
RU019
4-100 4A K High Bit 1
Ctrl P Equals K Set
Punch Feed
A
FL
RU031
Punch Feed
2540
Punch feed signal conditions the punch clutch latch, punch motor controls and the punch clutch error circuit.
(Not) Punch Command Inlk
4-14 BD 2540 Mode
4-100 4A Ext AS Field Decode D
4-100 4B Word Type 0 Reset Pulse
A
RU019
Ctrl RP Equals K Reset
(Punch Write)
Blocks reset of the punch ready latch.
4-111 4C
Punch Ready
FL
2540
(Not) Punch Ready
Punch Ready
(Punch Intrvn Req)
A
A
FL
RU031
4-108 3B Punch Cycle
A
RT041
Xfer Cy Rq
Xfer Cy Rq signal sets the 2540 Process Meter latch.
..4C Set Punch Req
A
(Not) Pch Intervention
4-43 4E
(Not) Pch Intervention
4-100 4A K Low Bit 2
..3D Ctrl P Equals K Reset
4-101 4B Native Rdr Pch Reset
A
OR
Block Pch Init Ready
FL
RU015
Pch Intervention
A
..8E Gated Pch Over Run
Punch Initial Ready
..3C
..4D Reset Pch Status
4-101 4B Native Reader Reset
OR
OR
Punch DE
FL
RU 016
Pch Device End 4-43 4E
..6A Ctrl P Equals K Set
4-100 4A K Low Bit 2
A
Set Punch Req ..8B
Pch Status
..9C Punch Device End
..8E Gated Pch Over Run
OR
FL
RU015
4-101 4B Integrated Rdr Pch Reset
OR
4-14 8D 2540 Mode
4-100 4A Ext AS Field Decode F
4-100 4B Word Type 0 Reset Pulse
A
RU019
Ctrl P Equals K Reset
A
4-100 4A K Low Bit 2
Reset Pch Status
..8C
Pch Queued
..6A Ctrl P Equals K Set
4-100 4A K Low Bit 3
OR
FL
RU015
4-101 4B Native Rdr Pch Reset
OR
OR
4-16 8E (Not) S7 Chnl 0 Interrupt Latch
A
Punch Status Request 4-43 4E; 4-104 5D
2540
Pch Clutch
FL
Pch NPRO
FL
A
2.2ms
4-108 8B Punch Select Lat
TD
RT021
4-101 5C (Not) Diagnostic Single Cycle
4-101 4A Time 375-450
A
RT021
Pch Over Run Set
4-101 6C (Not) Rdr Pch Off Line
A
RT006
Pch Cl Lat NPRO
4-108 2D
CE Panel
Pch Sync
..3A Ctrl RP Equals K Set
4-100 4A K Low Bit
A
RU031
Pch Mach Check
Pch Over Run Inlk 1
OR
FL
RT041
4-108 6C, 8A
Pch Over Run Inlk 1
4-101 4A Time 225-300
A
OR
Pch Over Run Inlk 2
FL
RT041
4-101 4B Native Rdr Pch Reset
4-108 5D Pch Cl Req
OR
(Not) Pch Over Run Inlk 1
4-108 6B, 7A
4-101 4A Time 000-075
A
OR
4-105 4B
Gated Pch Over Run
Punch Over Run
FL
RU071
Punch Over Run Latch
4-43 8A
4-101 4B Native Rdr Pch Reset

Diagram 4-108. Punch Controls, Trap

2 3 4 5 6 7 8 9

A B C D E

2540

(Not) Pch NPRO Latch
Pch Scan Pulse
Brush Gate Latch
(Not) Off Line
A

After 9Emitter
(Not) Off Line
(Not) Pch NPRO Latch
OR
A
After 9 Emitter

4-101 8E Diagnostic Sel Pch Scan
Punch Scan
4-101 4A Time 000-150
A
A
OR

4-101 4A Time 375-450
A
Pch Cycle Time 375-450

4-101 4A Time 000-150
..9C Shift Advance Pch Lat
A
Pch Cycle
FL
RT018
Punch Cycle
..6D, 8D

4-101 4B Native Rdr Pch Reset
..9C (Not) Shift Advance Pch Lat
4-101 4A Time 000-075
A
OR

4-101 4A Time 000-075
4-101 4B Native Rdr Pch Reset
OR
Pch Scan No. 1
FL
RT018
4-106 3B
Pch Scan Number 1

4-101 4A Time 150-225
4-100 4B Native Rdr Pch Reset
A
OR

4-100 4A Time 150-225
4-107 6E (Not) Pch Overrun Inlk 1
A
Pch Scan No. 2
A
FL
(Not) Pch Scan Number 2 4-106 3B

Delta Pch Scan
FL
RT018
Delta Pch Scan Lat ..6B
4-100 4B Native Rdr Pch Reset
..4B Pch Cycle Time 375-450
4-107 6E Pch Overrun Inlk 1
OR

4-101 4A Time 300-375
..9A Delta Pch Scan Lat
4-103 7B (Not) Rdr Sel or Trap
4-108 6E (Not) Pch Overrun Inlk 1
A

Pch Sel
FL
Punch Select Lat ..8D; 4-109 2B; 4-110 4C
(Not) Punch Select Lat 4-103 5B

4-101 4A Time 375-450
4-109 5C Tens ARC
4-109 5C Tens ARD
A
Pch Col 80
FL
RT021

..9A Delta Pch Scan Lat
4-101 4B Integrated Rdr Pch Reset
OR

..5C Decode Enter
4-107 5E Pch Overrun Inlk 1
4-101 6C Rst Tr Sel Rdr Pch
A
OR

..9A Dlta Pch Scan Lat
4-101 4A Time 300-375
A
A
OR

Punch Micro
FL
Punch Micro Lat

4-101 4D Gate CPU to Ext Pulse
4-14 8D 2540 Mode
4-100 4A Ext AS Field Decode F
A
..7E
Decode Enter

..8B Punch Select Lat
4-101 4B Native Rdr Pch Reset
..4B Pch Cycle Time 375-450
A
OR

Punch Shift Adv
FL
RT021
Shift Advance Pch Lat
(Not) Shift Advance Pch Lat ..2B

4-101 4B Native Pdr Pch Reset
4-101 7D Diagnostic Rst Pch Advance
..3B Punch Cycle
4-101 4A Time 375-450
End of Byte Record
A
OR
OR

..6E (Not) Pch Clutch Tap Inlk
4-101 4A Time 300-375
Pch Clutch Lat
A
4-107 5E
Pch Cl Req

4-110 7E EOR Rd 2 or Pch Chk
4-110 7B EOR Rd 1 or PFR
OR

..3B Punch Cycle
4-101 4A Time 375-450
A
OR

..7B Punch Select Lat
OR
Pch Sel or Trap 4-102 3E

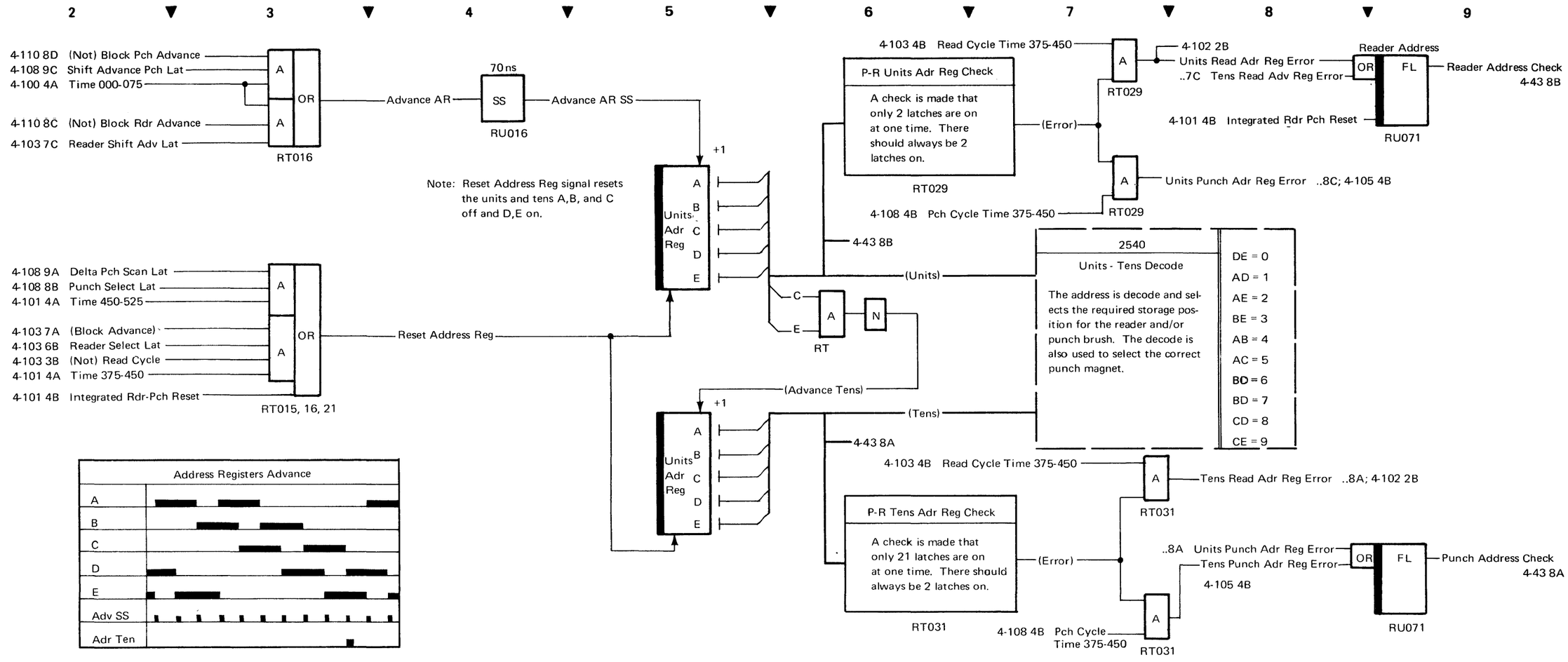
Pch Clutch
4-107 2E Pch Cl Lst Not NPRO
4-103 7B (Not) Rdr Sel or Trap
4-101 4A Time 150-225
A
FL
RU018

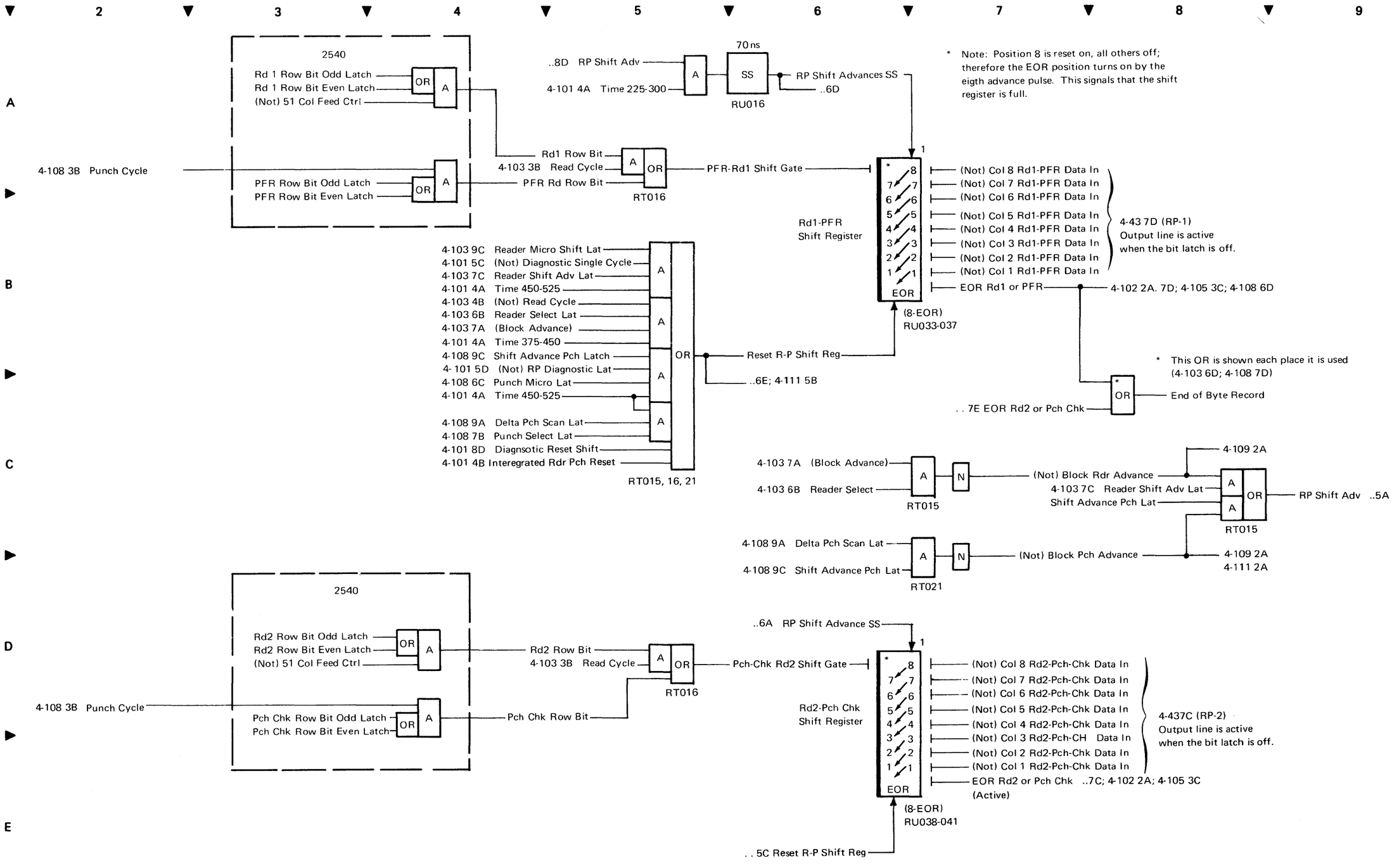
4-107 (Not) Pch Cl Lat Not NPRO
4-101 4B Native Rdr Pch Reset
A
OR

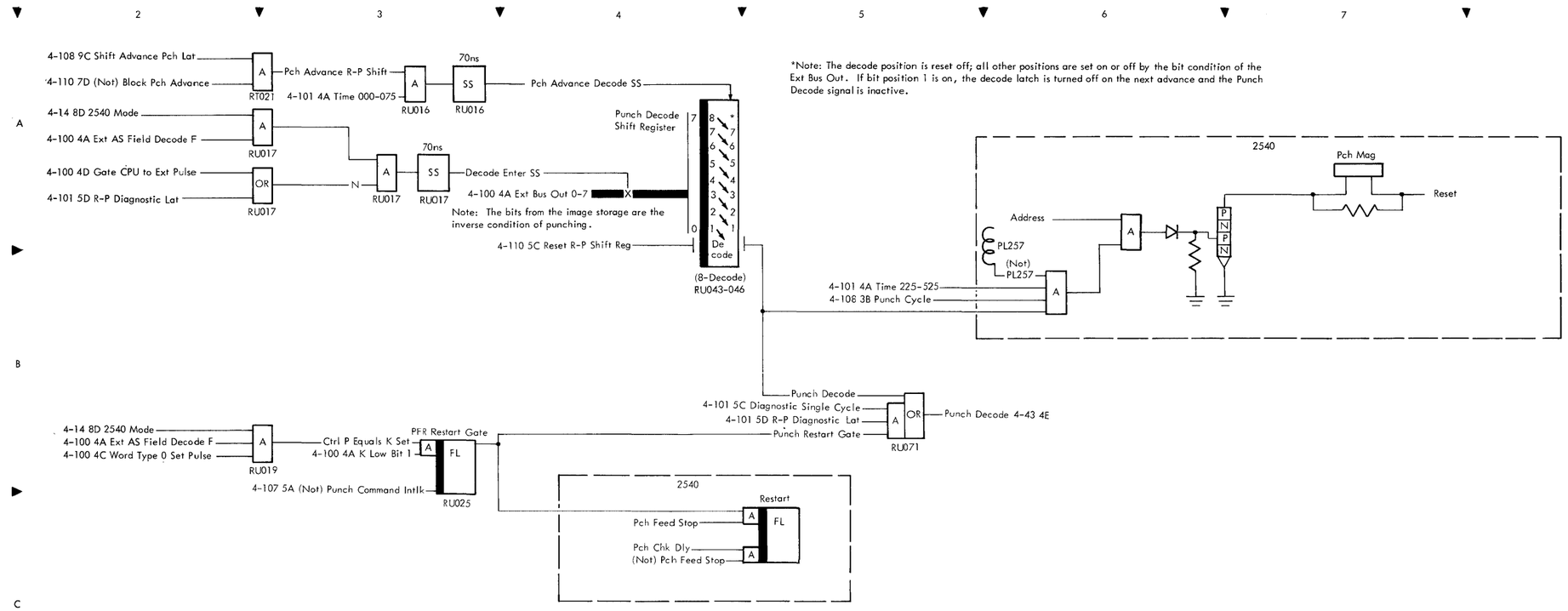
Pch Trap Inlk
2540 Pch Trap Request
4-101 4A Time 375-450
4-101 4A Time 375-450
A
FL
RU018
(Not) Pch Clutch Trap Inlk, ..4D

Punch Trap
FL
2540 Pch Trap Request 4-23 2A

..5C Deocde Enter
4-101 6C Rst Tr Sel Rdr Pch
OR


2
3
4
5
6
7
8
9
A
B
C
D
E
4-110 8D (Not) Block Pch Advance
4-108 9C Shift Advance Pch Lat
4-100 4A Time 000-075
4-110 8C (Not) Block Rdr Advance
4-103 7C Reader Shift Adv Lat
A
OR
RT016
Advance AR
70ns
SS
RU016
Advance AR SS
+1
Units Adr Reg
A
B
C
D
E
Note: Reset Address Reg signal resets the units and tens A,B, and C off and D,E on.
4-103 4B Read Cycle Time 375-450
P-R Units Adr Reg Check
A check is made that only 2 latches are on at one time. There should always be 2 latches on.
RT029
(Error)
A
RT029
4-102 2B
Units Read Adr Reg Error
..7C Tens Read Adv Reg Error
Reader Address
OR
FL
RU071
Reader Address Check
4-43 8B
4-101 4B Integrated Rdr Pch Reset
A
Units Punch Adr Reg Error ..8C; 4-105 4B
RT029
4-108 4B Pch Cycle Time 375-450
4-43 8B
(Units)
2540
Units - Tens Decode
The address is decode and selects the required storage position for the reader and/or punch brush. The decode is also used to select the correct punch magnet.
DE = 0
AD = 1
AE = 2
BE = 3
AB = 4
AC = 5
BD = 6
BD = 7
CD = 8
CE = 9
4-108 9A Delta Pch Scan Lat
4-108 8B Punch Select Lat
4-101 4A Time 450-525
4-103 7A (Block Advance)
4-103 6B Reader Select Lat
4-103 3B (Not) Read Cycle
4-101 4A Time 375-450
4-101 4B Integrated Rdr-Pch Reset
A
OR
RT015, 16, 21
Reset Address Reg
C
E
A
N
RT
(Advance Tens)
+1
Units Adr Reg
A
B
C
D
E
(Tens)
4-43 8A
4-103 4B Read Cycle Time 375-450
A
RT031
Tens Read Adr Reg Error ..8A; 4-102 2B
P-R Tens Adr Reg Check
A check is made that only 21 latches are on at one time. There should always be 2 latches on.
RT031
(Error)
..8A Units Punch Adr Reg Error
Tens Punch Adr Reg Error
4-105 4B
OR
FL
RU071
Punch Address Check
4-43 8A
4-108 4B Pch Cycle Time 375-450
A
RT031
Address Registers Advance
A
B
C
D
E
Adv SS
Adr Ten


2 3 4 5 6 7 8 9
A B C D E
2540
Rd 1 Row Bit Odd Latch
Rd 1 Row Bit Even Latch
(Not) 51 Col Feed Ctrl
OR
A
4-108 3B Punch Cycle
PFR Row Bit Odd Latch
PFR Row Bit Even Latch
PFR Rd Row Bit
Rd1 Row Bit
4-103 3B Read Cycle
PFR-Rd1 Shift Gate
RT016
..8D RP Shift Adv
4-101 4A Time 225-300
70 ns
SS
RU016
RP Shift Advances SS
..6D
* Note: Position 8 is reset on, all others off; therefore the EOR position turns on by the eigth advance pulse. This signals that the shift register is full.
Rd1-PFR Shift Register
(Not) Col 8 Rd1-PFR Data In
(Not) Col 7 Rd1-PFR Data In
(Not) Col 6 Rd1-PFR Data In
(Not) Col 5 Rd1-PFR Data In
(Not) Col 4 Rd1-PFR Data In
(Not) Col 3 Rd1-PFR Data In
(Not) Col 2 Rd1-PFR Data In
(Not) Col 1 Rd1-PFR Data In
EOR
(8-EOR)
RU033-037
4-43 7D (RP-1)
Output line is active when the bit latch is off.
EOR Rd1 or PFR
4-102 2A. 7D; 4-105 3C; 4-108 6D
4-103 9C Reader Micro Shift Lat
4-101 5C (Not) Diagnostic Single Cycle
4-103 7C Reader Shift Adv Lat
4-101 4A Time 450-525
4-103 4B (Not) Read Cycle
4-103 6B Reader Select Lat
4-103 7A (Block Advance)
4-101 4A Time 375-450
4-108 9C Shift Advance Pch Latch
4-101 5D (Not) RP Diagnostic Lat
4-108 6C Punch Micro Lat
4-101 4A Time 450-525
4-108 9A Delta Pch Scan Lat
4-108 7B Punch Select Lat
4-101 8D Diagnsotic Reset Shift
4-101 4B Interegrated Rdr Pch Reset
RT015, 16, 21
Reset R-P Shift Reg
..6E; 4-111 5B
* This OR is shown each place it is used (4-103 6D; 4-108 7D)
End of Byte Record
. . 7E EOR Rd2 or Pch Chk
4-103 7A (Block Advance)
4-103 6B Reader Select
RT015
(Not) Block Rdr Advance
4-103 7C Reader Shift Adv Lat
Shift Advance Pch Lat
RP Shift Adv ..5A
4-109 2A
4-108 9A Delta Pch Scan Lat
4-108 9C Shift Advance Pch Lat
RT021
(Not) Block Pch Advance
4-109 2A
4-111 2A
2540
Rd2 Row Bit Odd Latch
Rd2 Row Bit Even Latch
(Not) 51 Col Feed Ctrl
4-108 3B Punch Cycle
Pch Chk Row Bit Odd Latch
Pch Chk Row Bit Even Latch
Pch Chk Row Bit
Rd2 Row Bit
4-103 3B Read Cycle
Pch-Chk Rd2 Shift Gate
RT016
..6A RP Shift Advance SS
Rd2-Pch Chk Shift Register
(Not) Col 8 Rd2-Pch-Chk Data In
(Not) Col 7 Rd2-Pch-Chk Data In
(Not) Col 6 Rd2-Pch-Chk Data In
(Not) Col 5 Rd2-Pch-Chk Data In
(Not) Col 4 Rd2-Pch-Chk Data In
(Not) Col 3 Rd2-Pch-CH Data In
(Not) Col 2 Rd2-Pch-Chk Data In
(Not) Col 1 Rd2-Pch-Chk Data In
EOR
(8-EOR)
RU038-041
4-437C (RP-2)
Output line is active when the bit latch is off.
EOR Rd2 or Pch Chk ..7C; 4-102 2A; 4-105 3C
(Active)
. . 5C Reset R-P Shift Reg



	Reader Transfer		Advance	1	2	3	7	8	Trap	1
	Name	MDM Page	000	000	000	000	000	000	000	000	000
1	Reader Brush Impulse	4-103 3A	500 us							
2	(Rdr Brush Imp TD)	4-103 6A	← 150 us							
3	(Block Advance)	4-103 7A	375							
4	Reader Select	4-103 6C								
5	Reader Shift Adv Lat	4-103 7C						375 · 10		375·12
6	Reset Address Reg	4-109 3B	375 450							
7	Read Cycle Latch	4-103 3B	000							
8	Advance AR	4-109 4A	5·000							
9	RP Shift Adv	4-110 6A	225							
10	End of Byte Record	4-110 8C								450·5
11	Reader Trap Latch	4-102 9D								
12	Reader Micro Lat	4-103 9C								225
13	Reset R-P Shift Reg	4-110 5B	375 450							12·450

This shows the Shift Register being loaded with 8 bits and recognizing when the register is full (End of Byte Record). Also the trap latch and the time for the trap; all 8 bits are transferred in parallel. When trap is taken the Reader Micro Latch turns on, setting conditions for the next 8 bits to be loaded into the registers.

	Punch Transfer		Advance	1	2	3	7	8	Trap	1	2
	Name	MDM Page	000	000	000	000	000	000	000	000	000
1	Punch Scan	4-108 3A									
2	Punch Scan #1 Lat	4-108 5A									
3	Punch Scan #2 Lat	4-108 7A									
4	Delta Pch Scan Lat	4-108 9A									
5	Punch Select Lat	4-108 7B									
6	Punch Shift Adv Lat	4-108 9C									
7	Punch Cycle	4-108 3B	000								
8	Reset Address Reg	4-109 3B	450 525								
9	Reset RP Shift Reg	4-110 5B	450 525							15·450	
10	Advance AR	4-109 4A	6·000								
11	RP Shift Adv	4-110 6A	225								
12	Pch Advance Decode	4-111 5A	6·000								
13	End of Byte Record	4-110 8C									
14	Punch Trap Lat	4-108 7D									
15	Punch Micro Lat	4-108 6C									

Punch Decode Shift Register Loaded

The first 8 bits have been loaded into the Punch Decode Shift Register prior to receiving the punch scan pulse. One bit is shifted out for each Pch Advance Decode pulse. End of byte record signals the end of 8 bits.

Diagram 4-112. Timing to 2540, 2540 Signal to External Facility

2 3 4 5 6 7 8 9

A B C D E

2540

(Not) Rem Stop
Punch Run In
A
FL
4 Bit Modify Pull On 4-43 4E

Die Sta Dly
PL 347
Throat Dly
A
PRF EOF
FL
FL
OR
PFR Unit Exception Gate 4-43 4E
Power On Reset
Pch Clutch Latch

4-108 3B Punch Cycle
(Even Address)
4-101 4A Time 150-525
(150-450)
A
Pch Read Out Drive
A
Rd Read Out Drive
4-103 3B Read Cycle

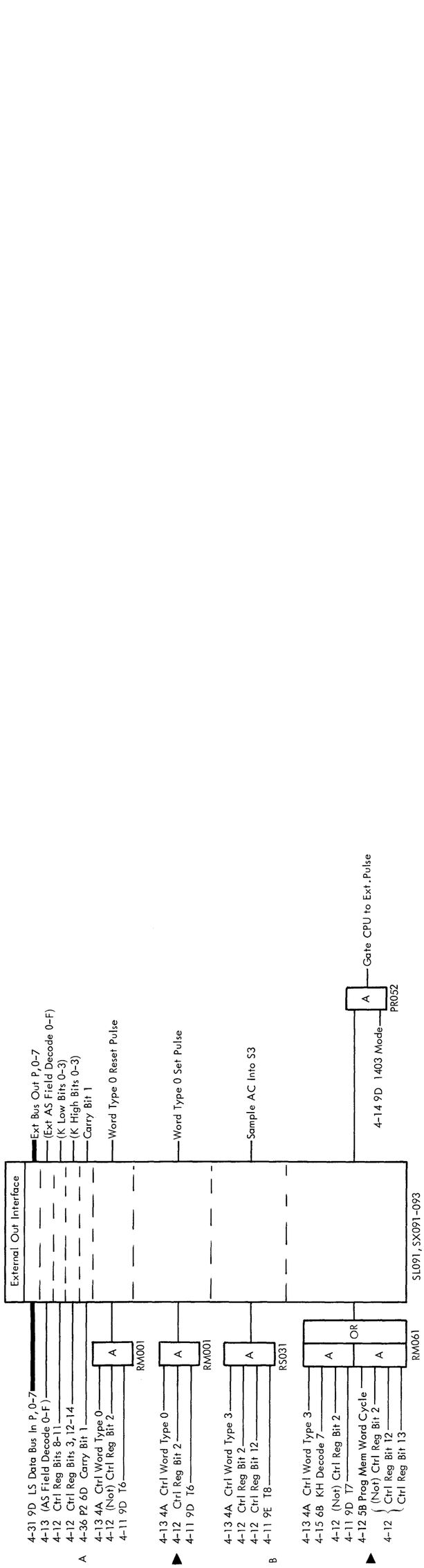
No 2 Br Dly
(Not) No 1 Br Dly
(Not) No 1 Br Sta
(Reader)
End of File
A
FL
1400 Unit Exception Gate 4-43 8E

A
Unit Exception Gate Reader 4-43 8E
Rdr Runout Reset

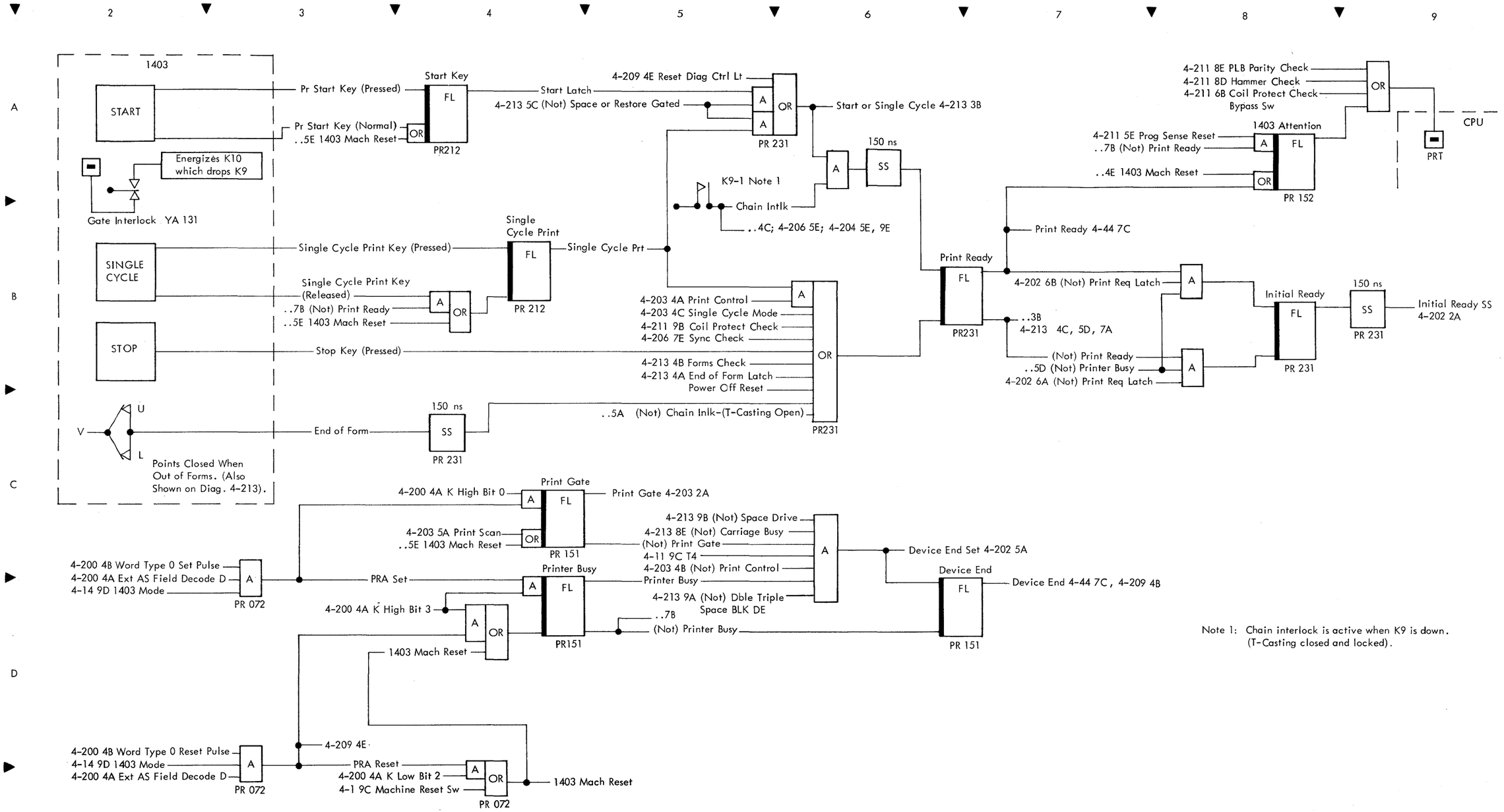
4-101 4A Time 075-150
Row Bit Reset Even Aux Latch

Rd Feed Stop Latch
No 2 Br Dly or Runout
OR
Gate Rd Complete 2540 4-43 8E

Pch Brush CL Delay
Pch Brush CL 4-43 4D



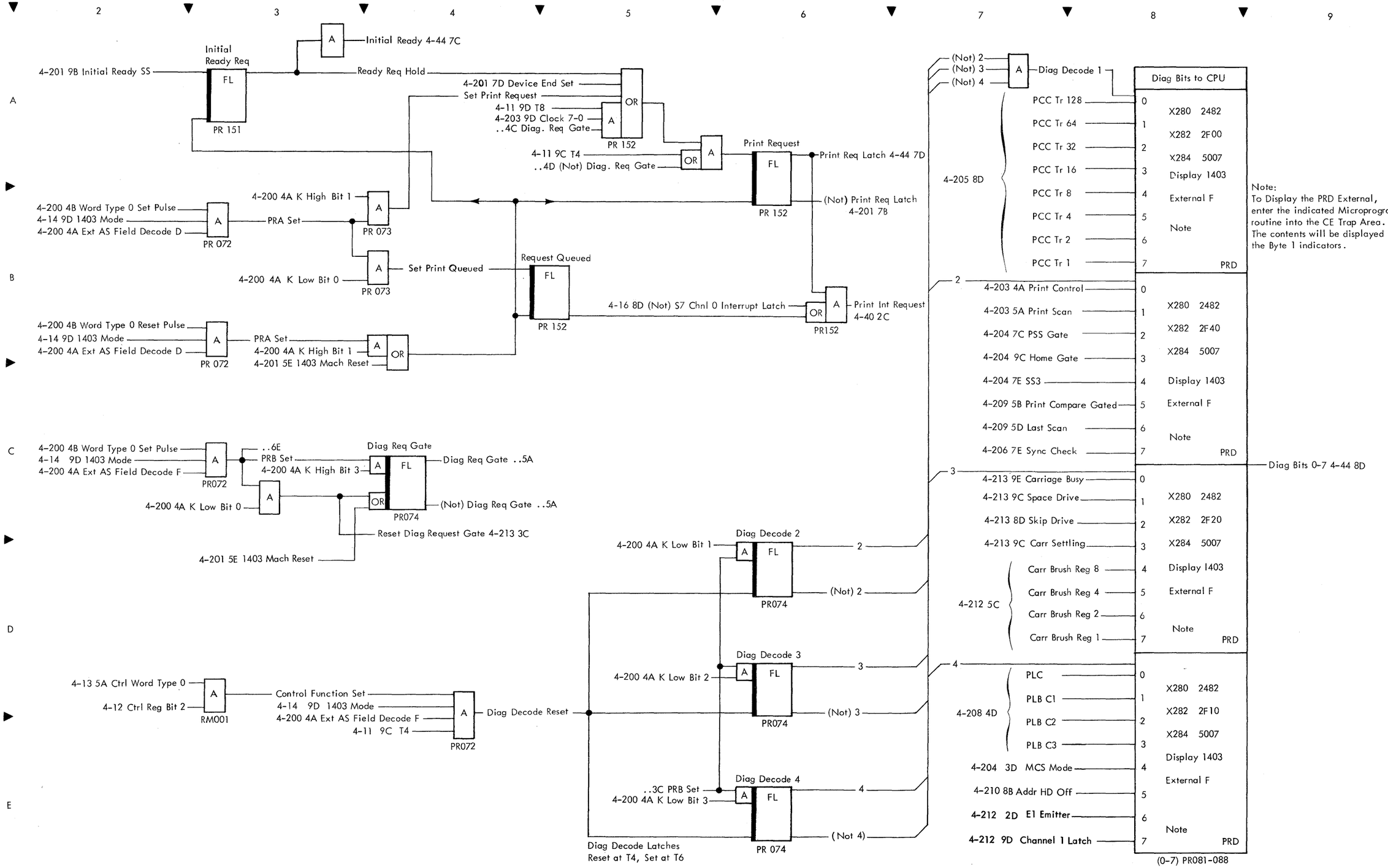
● Diagram 4-200. External-Out Interface (Printer)



Note 1: Chain interlock is active when K9 is down. (T-Casting closed and locked).

Form Y24-3529-0
FES Y24-0094

● Diagram 4-202. Printer Controls, Status, and Diagnostic Bits to CPU



2 3 4 5 6 7 8 9

A B C D E

* The input is a CE aid. If home gate is jumpered (back panel), the Print Control Latch can only turn on at home gate time. Printing will then always start with the PCC at a value of 01.

4-204 6E Printer in Sync
4-213 9C (Not) Carr Settling
4-201 4C Print Gate
4-204 9C Home Gate (Jumper)*
4-204 9C Advance PCC
4-204 7E SS3
4-204 6E (Not) Printer In Sync
...9D Clock 6-7
...5B (Not) Print Scan
4-209 5D Last Scan
4-211 6C Coil Protect Gated
A
OR
Print Control Set 4-209 2C
Print Control
FL
PR261
..7D
Print Control
4-204 9D Reset Home Gate
4-201 5C
(Not) Print Control
..7A Clock Control
..9D Clock 0-1
CE Panel PR Sync
Print Scan
4-201 4C
4-206 2C, 6C, 7C
Print Scan
..9D Clock 5-6
4-210 4A Adr 44,88 or 132
Clock Control
PR412
Scan Clock Run ..5C
Clock Control ..4B; 4-205 2B, 5E; 4-209 4C
(Not) Print Scan
..8C (Not) Osc
..9D Clock 7-0
(Not) Clock Control 4-204 4B; 4-207 2A; 4-208 3D
4-205 2A, 4D; 4-206 2C
..2B; 4-206 6C

4-200 4B Word Type 0 Set Pulse
4-200 4A Ext AS Field Decode F
4-14 8D 1403 Mode
PRB Set
4-200 4A K High Bit 0
4-200 4A K High Bit 1
4-1 9C Machine Reset Sw
Single Cycle
Single Cycle Mode 4-201 5B
4-209 5B
4-210 8C
4-204 3D
4-204 4B, 3D
(Not) Single Cycle Mode
PR073

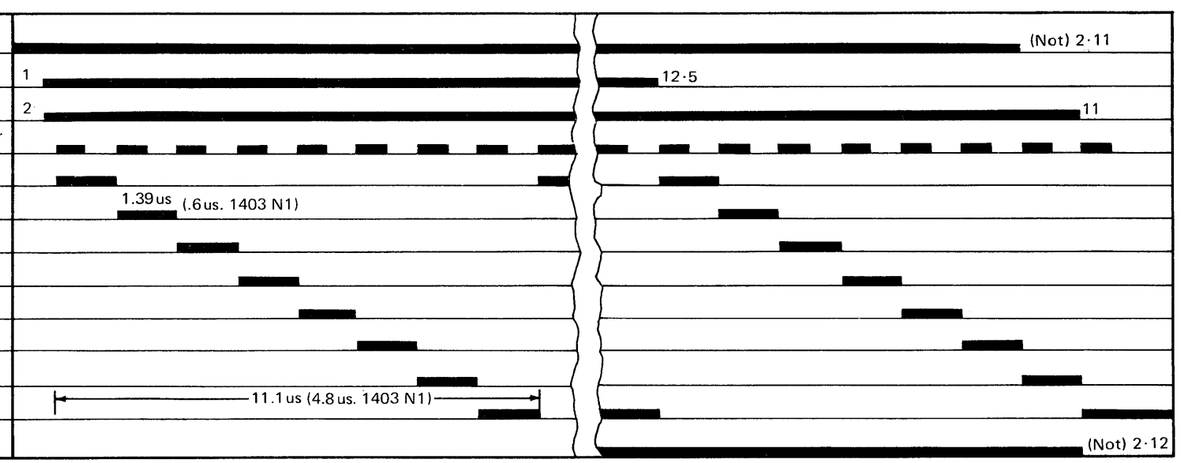
4-200 4B Word Type 0 Reset Pulse
4-200 4A Ext AS Field Decode F
4-14 8D 1403 Mode
PR B Reset
4-200 4A K High Bit 1
..9D Clock 1-2
4-201 5E 1403 Mach Rst
Single Cycle Clock Run
PR073

..7A Scan Clock Run
..9D Clock 7-0
Clock Run
PR073
Osc Trigger
PR411
Clock 11.1 us
Clock 0-1
Clock 1-2
Clock 2-3
Clock 3-4
Clock 4-5
Clock 5-6
Clock 6-7
Clock 7-0

720 KC (1403 Model 2 or 7)
OSC
PR411
1667 KC (1403 N1)
OSC
PR411
OSC
N
(Not) OSC ..6B

Block Resync
..4A Print Control
4-206 8E Sync Check
...4B Not Print Ctrl
4-204 6D Set Pr In Sync
PR261
(Not) Block Res Sync
4-204 4D MCS Gate Home
4-204 9C Home Gate SS
4-204 4C Set PSS B
Resync PCC 4-204 5E

1	Print Control
2	Print Scan
3	Clock Run
4	Oscillator Trigger
5	Clock 0—1
6	Clock 1—2
7	Clock 2—3
8	Clock 3—4
9	Clock 4—5
10	Clock 5—6
11	Clock 6—7
12	Clock 7—0
13	Clock Control



Form Y24-3529-0
FES Y24-0094

Form Y24-3529-0
FES Y24-0094

2 3 4 5 6 7 8 9

A B C D E

1403 Drum — Diff Amp — Diff Amp — CV PR262 — N — 15us. SS PR262

Note: The SS extends the drum pulse to cover noise which occurs when the drum pulse turns off.

N — OR — A

4-203 4C (Not) Single Cycle Mode
4-203 7A (Not) Clock Control

4-200 4B Word Type 0 Reset Pulse
4-200 4A Ext AS Field Decode F
4-14 8D 1403 Mode
A PR072
PRB Reset
K Low Bit 0 — A — FL — Diag PSS Pulse — OR PR251
4-200 4A K Low Bit 1
4-201 5E 1403 Mach Reset
A OR PR074

1	Oscillator	555us (243us. 1403 N1)
2	Drum or Single Cycle	144 — 90us — Home — 180us — 1
3	PSS A	
4	PSS B	
5	PSS C	
6	PSS Gate Latch	(Not) 2 — (Not) 2
7	Set Home Gate SS	(Not) 5
8	Advance PCC	
9	Home Gate SS	7 — 350us (160us. 1403 N1) — 7
10	Home Gate	5 — 5
11	Set Pr In Sync	10 — (Not) 10
12	Print Control	8 (See Diag 4-203 4A)
13	SS1	7
14	SS2	7
15	SS3	

4-203 9E, ..9C

Drum or Single Cycle — N — A — Set PSS B — N — A — Set PSS C
..7C (Not) PSS Gate
4-203 8D Osc
..4C (Not) PSS B
A — PSS A FL PR251 — (Not) PSS A — A — PSS B FL PR251 — PSS B — ..2C; 4-206 6E
4-207 3B; 4-209 3C
..2C, 4

N — OR
..4C PSS B
4-203 8D Osc
A

N — N

Drum or Single Cycle — N — PSS Gate FL PR252 — 4-202 7B
..9D (Not) Home Gate
PSS Gate
(Not) PSS Gate ..2C

PSS C FL PR251 — 4-206 6E
(Not) PSS B
4-203 8D Osc
A
(Not) PSS C

..4C Set PSS B — A — Advance PCC 4-203 2A; 4-205 2A; 4-209 4C PR252
(160us. 1403 N1) 340us — N
A — SS PR252 — Home Gate SS 4-207 4B, ..8D; 4-203 8E
Home Gate
(Not) PSS B — A — FL PR252 — Home Gate 4-203 2A; 4-202 9C ..5D
PSS C
(Not) Home Gate ..8C ..3E

4-203 5C (Not) Single Cycle Mode
1403
Inactive — MCS Mode — Closed when using a MCS chain
MCS Emitter — 1 pulse per chain revolution
(1403 N1 6pulses per train revolution)

MCS
A — 4-205 2B, 4-202 8E
MCS Mode — OR PR372 — 4-203 8E
MCS Emitter
MCS Emitter — A FL PR372
..9C (Not) Home Gate

4-206 7E Sync Check
4-213 5C Chk Rst or Diag Rst
A — 150 ns SS PR252 — Set Pr In Sync — 4-209 2D, 3C; 4-203 8E
MCS Gate Home
..9C Home Gate

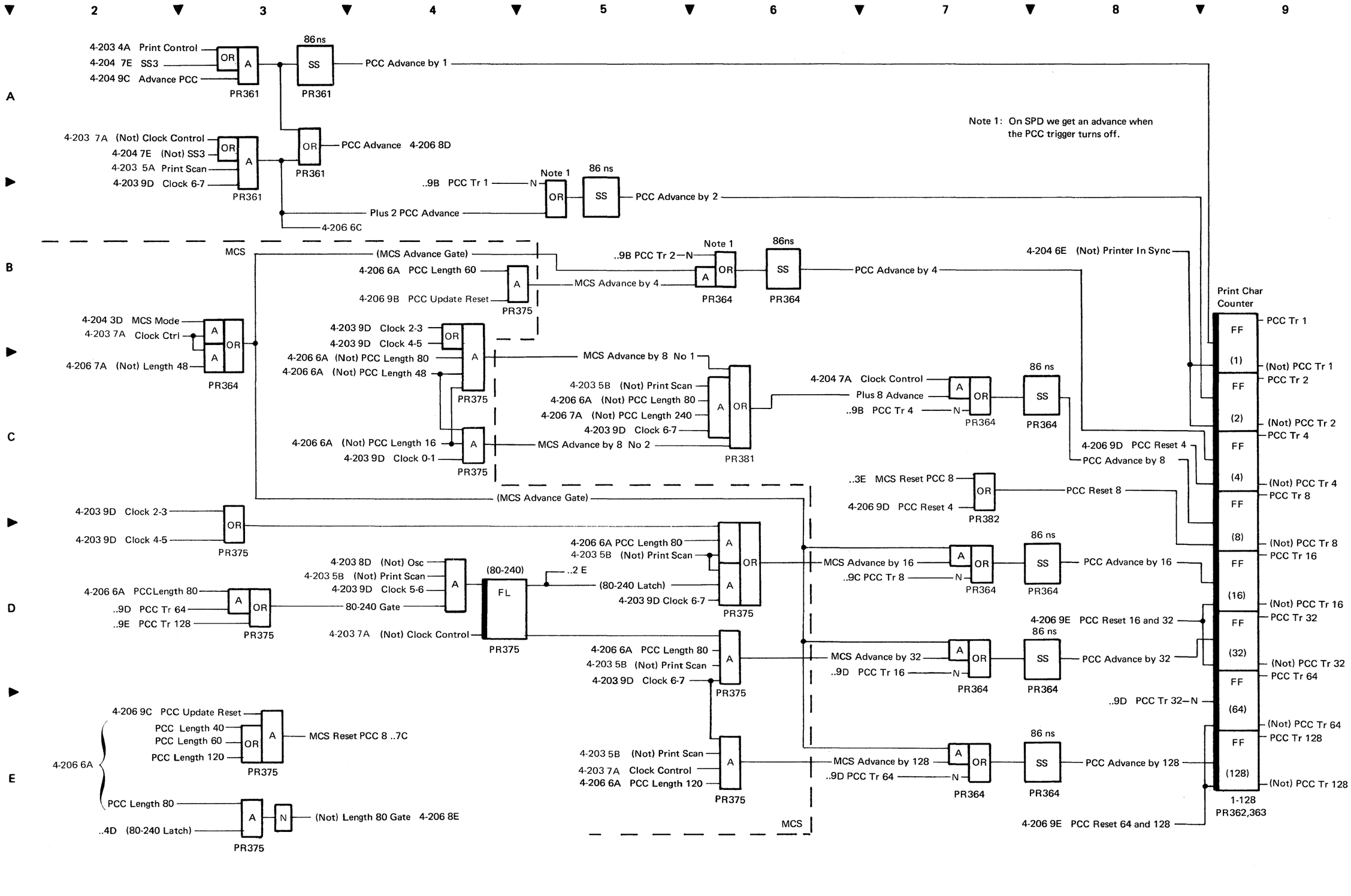
Printer In Sync
4-201 5A (Not) Chain Inlk
4-201 4E 1403 Mach Reset
4-206 4A PCCL Reset
4-203 9E Resync PCC
OR — FL PR252 — Printer In Sync 4-203 2A
(Not) Printer In Sync
4-203 2B; 4-205 8B; 4-206 6E, 7D

Set Home Gate SS
86 ns SS PR361 — SS Ring Advance
+1
SS Ring 1 2 * 3 PR365 — SS1 SS2 SS3

..9C (Not) Home Gate SS — A — Reset Home Gate 4-203 5B; 4-209 2C; 4-206 2C, 6D
4-201 5E 1403 Mach Reset
4-201 5A (Not) Chain Inlk
OR

* Note: Postion 3 is labeled (Not) SS3 and is reset off. When position 3 is off, SS3 lines are active.

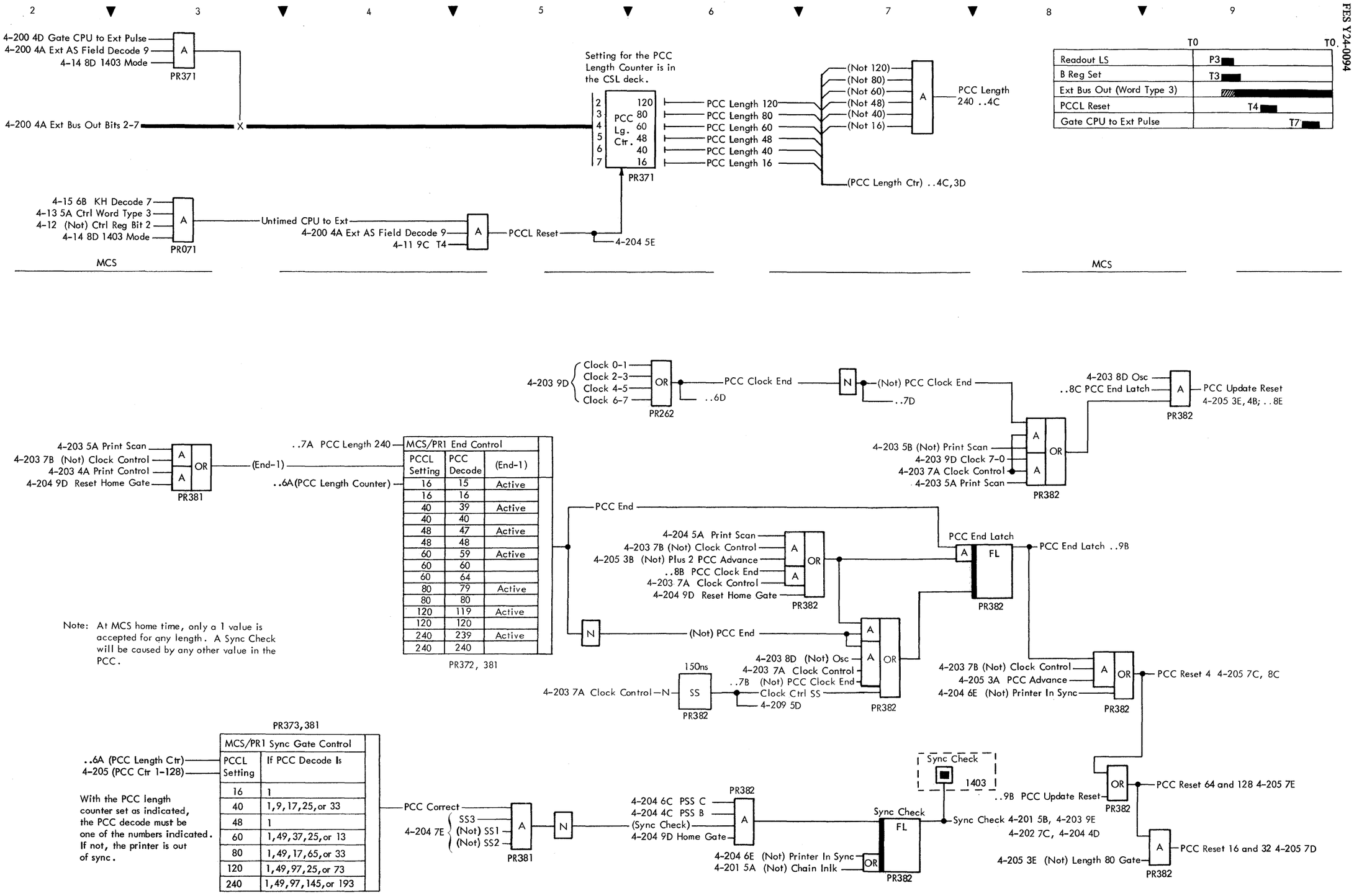
SS Ring Adv
SS1
SS2
SS3

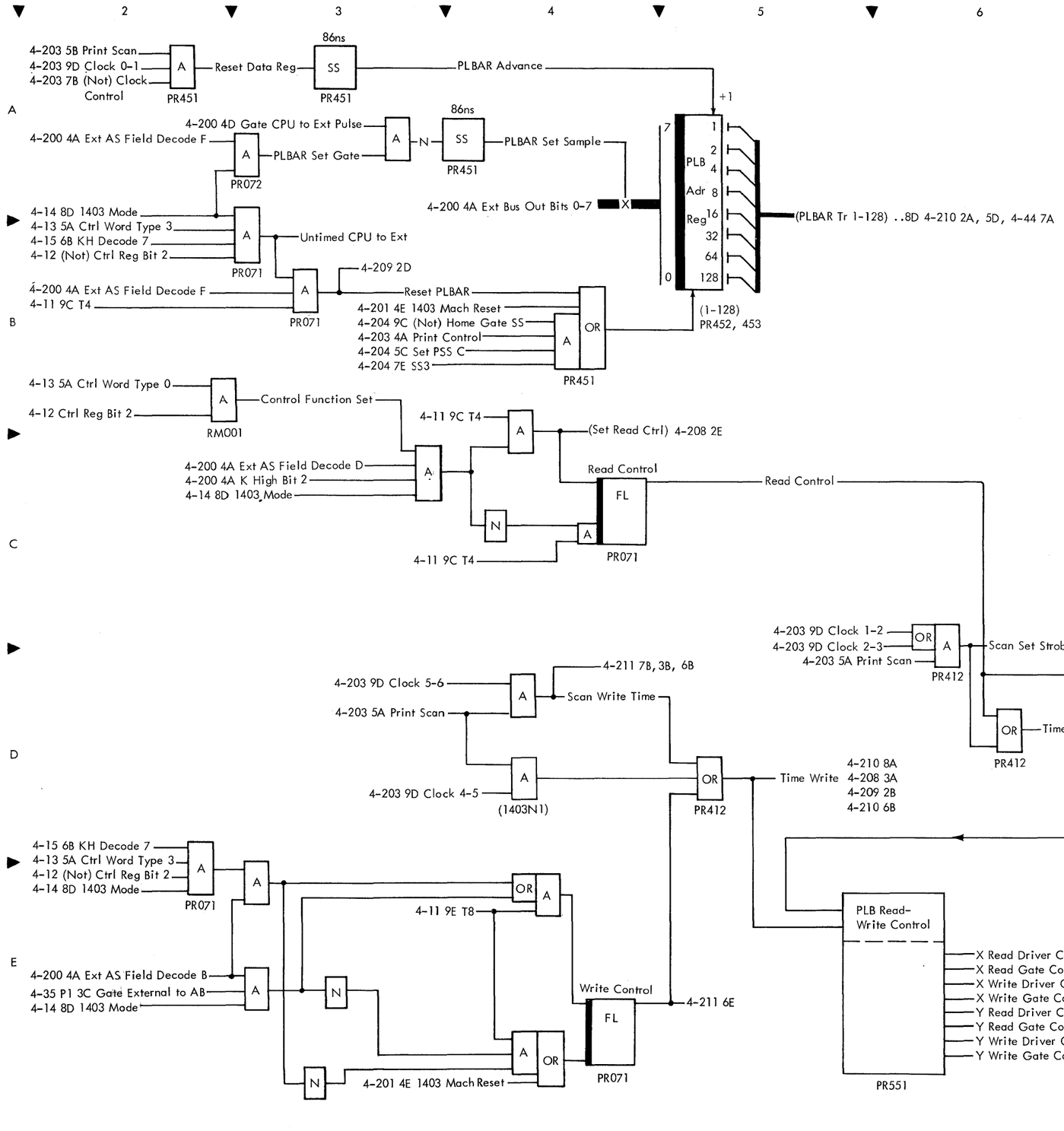


Form Y24-3529-0
FES Y24-0094

● Diagram 4-206. PCC Length Counter and PCC Resets

Form Y24-3529-0
FES Y24-0094





Read Data to CPU/Write Data from CPU ■=Read or Write ▨=Write Only

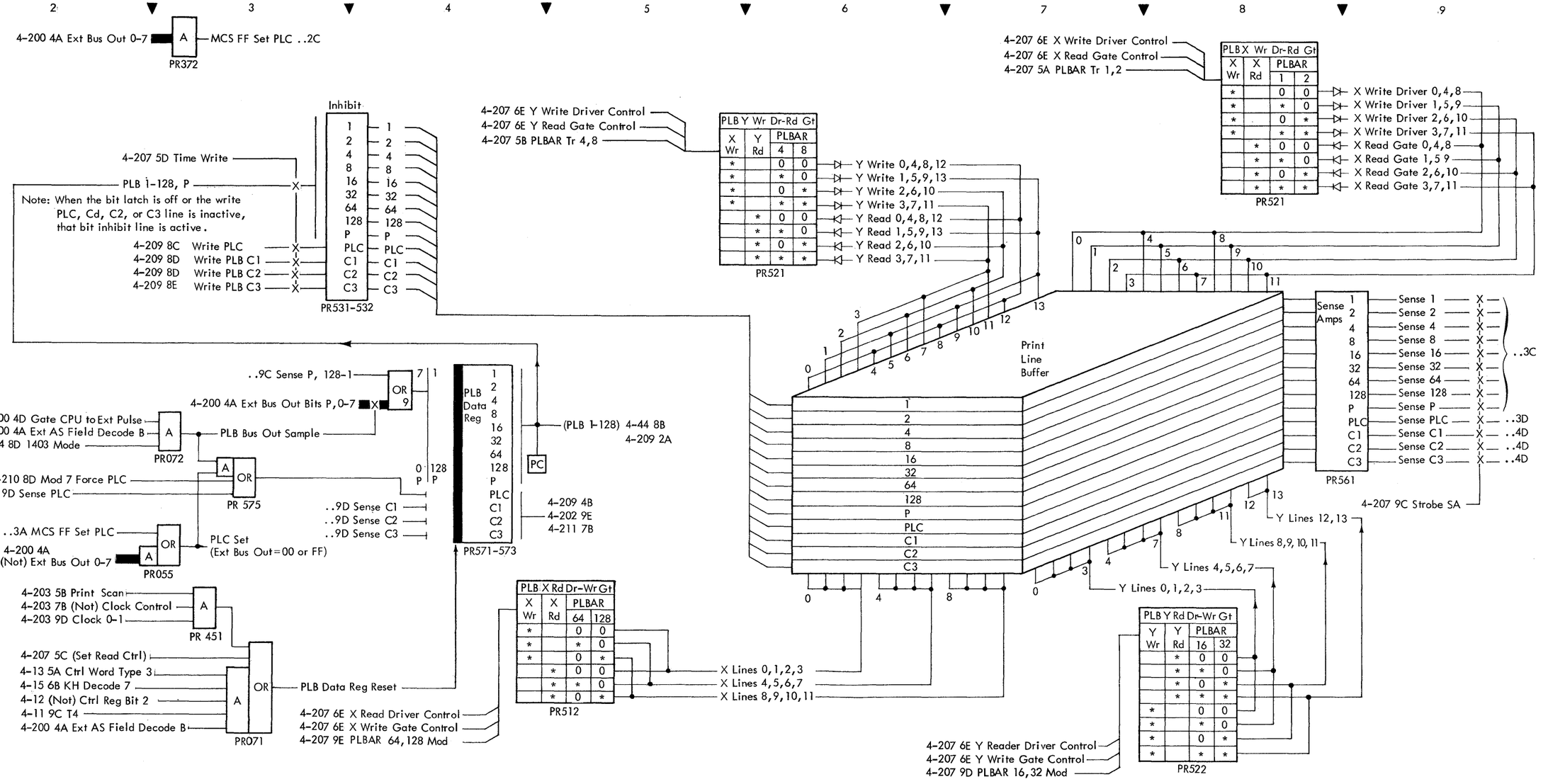
Cycle	Write PLBAR	Set Read Ctrl	Dummy	Read/Write Data	Dummy
Time P	0 2 4 6 8	1 3 5 7 9	0 2 4 6 8	1 3 5 7 9	0 2 4 6 8
PLBAR Reset	■				
PLBAR Set	■				
Data Reg Reset		■		▨	
Data Reg Set				▨	
Read Control		■	■		
Write Control					■
Parity Sample					▨
	Word Type 3	Word Type 0	Word Type X	Word Type 3	Word Type X

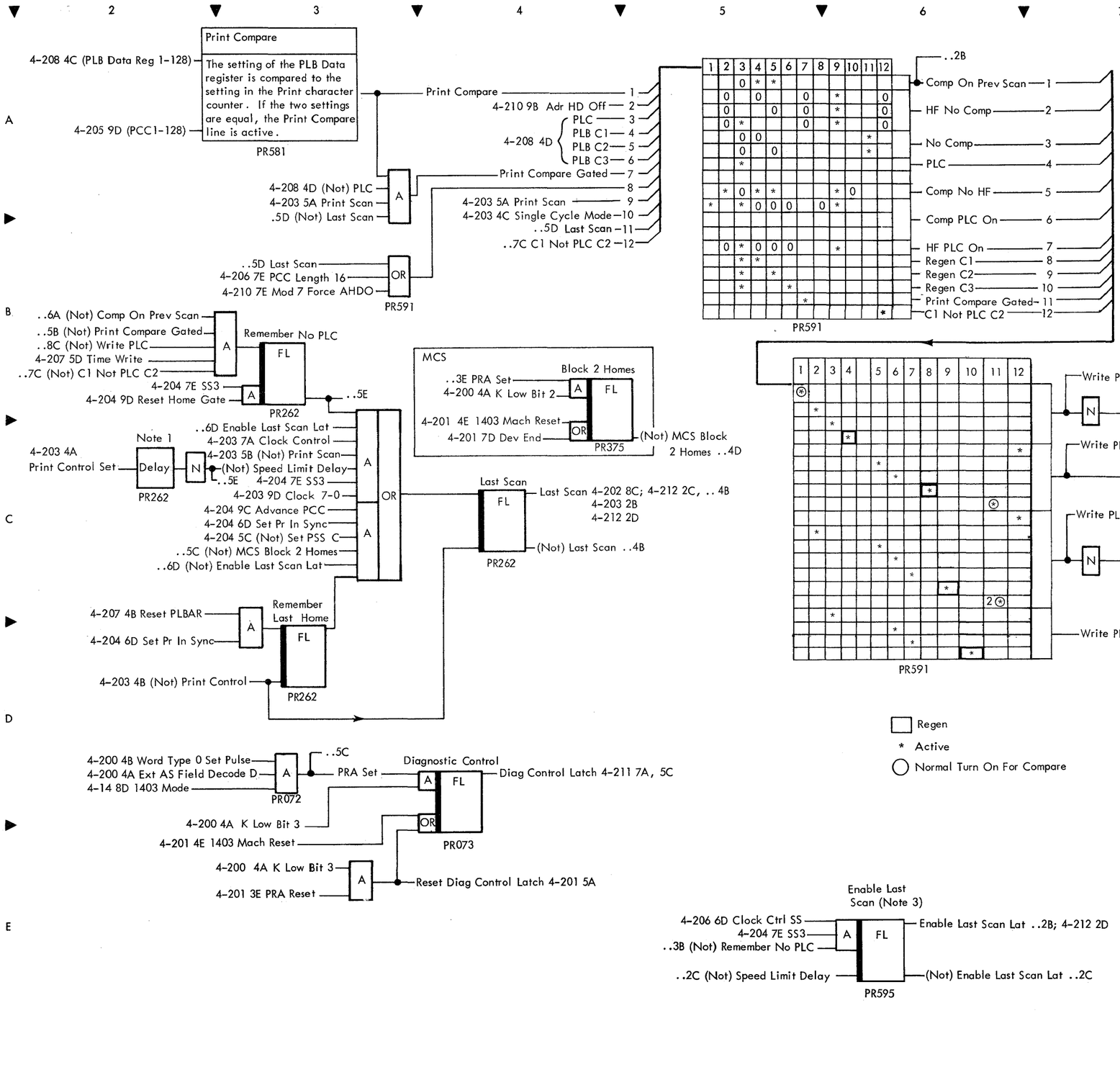
Note: The PLBAR is set during PLB loading so print line character 1 is in buffer position 1, character 2 in position 45, character 3 in position 89, character 4 in position 2. This allows the PLBAR advance by +1 during printing. PLBAR 1, hammer 1; PLBAR 2, hammer 4; PLBAR 3, hammer 7; etc.

Form Y24-3529-0
FES Y24-0094

● Diagram 4-208. PLB Data Register and Print Line Buffer

Form Y24-3529-0
FES Y24-0094





Check Plane Operation (1403 Models 2 or 7)

NO ERROR
- PLBC1, PLBC2

Set with Print Compare Gated (11)
Not Regenerated (8 and 9)
PLC
- Set On Next Scan (1)
- Regenerated (4)

ERROR CONDITIONS
- Set PLBC1, PLBC2, PLBC3 (Lines 2, 3, 5, 6 or 7)
- Regenerate (Lines 8, 9, 10)
- PLC will slso be set for all errors. The PLC, in addition to some check plane bit, indicates an error.

Check Plane Operation (1403 Model N1)

Print compare gated sets only C1. The next time the position is addressed, C1 Not PLC C2 sets C1 and C2. When the position is addressed for the third time, C1 Not PLC C2 (compare on previous) sets PLC and clears C1 and C2.

Note 1: The microdiagnostics are used to adjust the delay to give a maximum speed of 750 LPM for 1403 Model 2 and 1419 LPM for the 1403 Model N1.

Note 2: Turned on only for 1403 Models 2 or 7.

Note 3: The enable last scan latch is used for the 1403 Model N1 to delay the last scan for one additional scan after the last position has compared. This allows the hammer driver to stay on for two scans for 1403 Model N1 operation.

Form Y24-3529-0
FES Y24-0094

● Diagram 4-210. Hammer Driver Matrix

Form Y24-3529-0
FES Y24-0094

4-207 6B PLBAR 1-128

1	2	4	8	16	32	64	128	
0	0	*	*	0	*	0		
0	0	0	*	*	0	*		
0	0	*					*	

PR456

Adr 44, 88, or 132 4-203 6A

Hammer Addressing

1	2	4	8	16	32	64	128	
0	0	0						X Address 0
*	0	0						X Address 1
0	*	0						X Address 2
*	*	0						X Address 3
0	0	*						X Address 4
*	0	*						X Address 5
0	*	*						X Address 6
*	*	*						X Address 7
			0	0	0	0	0	Y Address 0
			*	0	0	0	0	Y Address 1
			0	*	0	0	0	Y Address 2
			*	*	0	0	0	Y Address 3
			0	0	*	0	0	Y Address 4
			*	0	*	0	0	Y Address 5
			0	*	*	0	0	Y Address 6
			*	*	*	0	0	Y Address 7
			0	0	0	*	0	Y Address 8
			*	0	0	*	0	Y Address 9
			0	*	0	*	0	Y Address 10
			*	*	0	*	0	Y Address 11
			0	0	*	*	0	Y Address 12
			*	0	*	*	0	Y Address 13
			0	*	*	*	0	Y Address 14
			*	*	*	*	0	Y Address 15
			0	0	0	0	*	Y Address 16

(X0-X7) PR 6U, 612
(Y0-Y16) PR621, 622

Hammer Driver Selection Matrix

Y ↓ / X →	0	1	2	3	4	5	6	7	Sub Scan Used
0		1	4	7	10	13	16	19	Sub Scan 1
1	22	25	28	31	34	37	40	43	
2	46	49	52	55	58	61	64	67	
3	70	73	76	79	82	85	88	91	
4	94	97	100	103	106	109	112	115	
5	118	121	124	127	130	2	5	8	Sub Scan 2
6	11	14	17	20	23	26	29	32	
7	35	38	41	44	47	50	53	56	
8	59	62	65	68	71	74	77	80	
9	83	86	89	92	95	98	101	104	
10	107	110	113	116	119	122	125	128	
11	131	3	6	9	12	15	18	21	Sub Scan 3
12	24	27	30	33	36	39	42	45	
13	48	51	54	57	60	63	66	69	
14	72	75	78	81	84	87	90	93	
15	96	99	102	105	108	111	114	117	
16	120	123	126	129	132				

PR 651-672

(Select HDX)

4-209 5B Print Compare Gated
4-207 5D Time Write
A
HD Compare
PR625

Note: HD Compare has several lines-
1 - Odd HD 1-55
2 - Even HD 2-56
3 - Odd HD 57-111
4 - Even HD 58-112
5 - Odd/Even HD 113-132

HD X (Note 1)
A
FL
PR651-672

1403
+60
Hammer Magnet

A
OR
(Addr HD X Off)
4-209 5A
4-211 7B
...8D Mod 7 Force AHDO

Reset

Resets Selected HD
4-207 5D Time Write
4-209 5B (Not) Print Compare Gated
4-209 7C (Not) C1 Not PLC C2
A
(Adr HDX Reset)
OR

Resets All HD
4-203 4B (Not) Print Control
4-211 9B Coil Protect Check
4-203 5C Single Cycle Mode
OR
PR625
HD Reset

Note: Reset has several Lines-
1 - Odd HD 1-55
2 - Even HD 2-56
3 - Odd HD 57-111
4 - Even HD 58-112
5 - Odd/Even HD 113-132

Note 1:
For 1403 models 2 or 7, the hammer driver is on for one print scan.
For 1403 N1, the Hammer driver is on for two print scans.

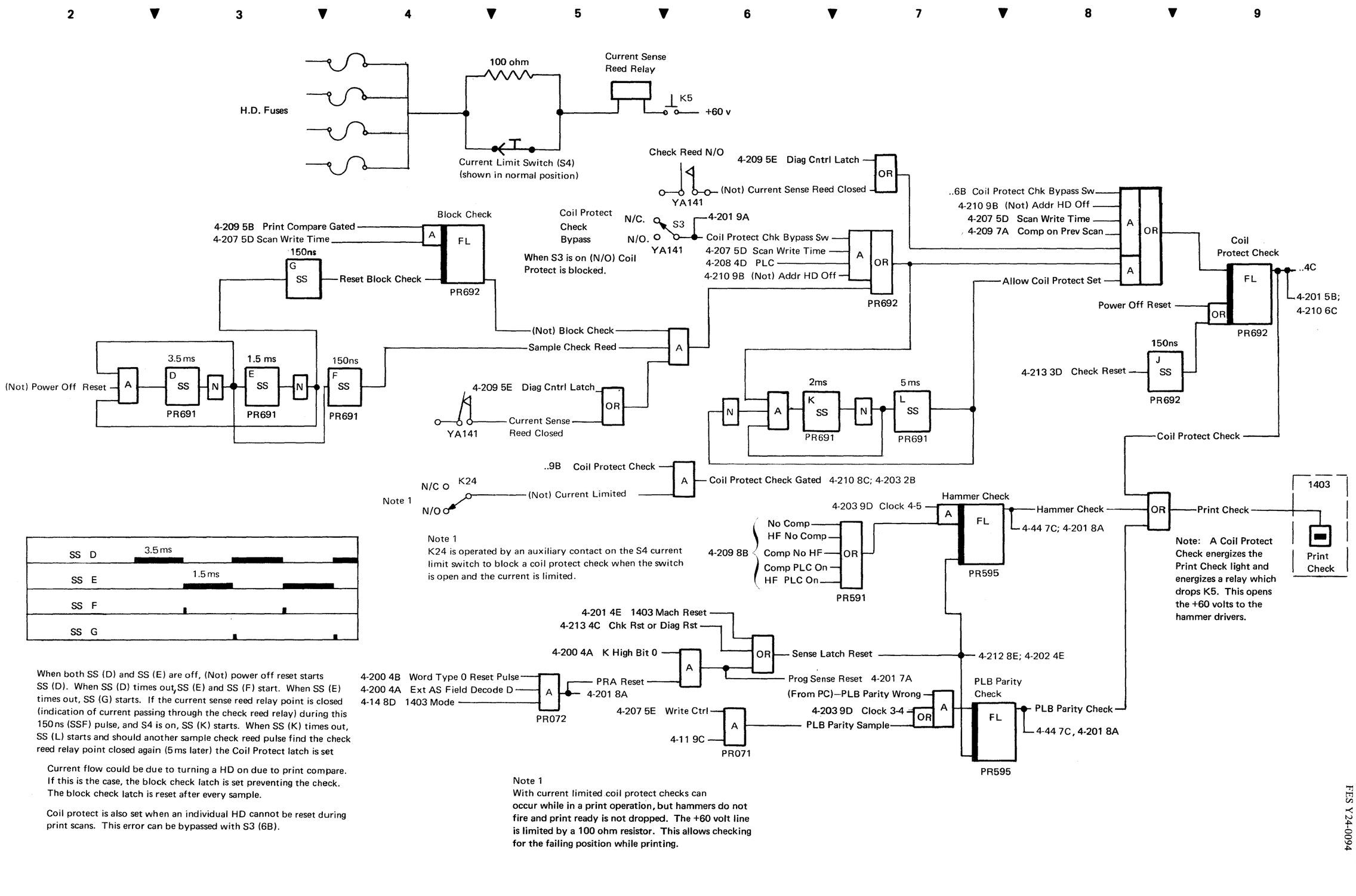
Model 7

4-207 6B
PLBAR 1 — 1
PLBAR 2 — 2
PLBAR 4 — 3
PLBAR 8 — 4
PLBAR 16 — 5
PLBAR 32 — 6
PLBAR 64 — 7
PLBAR 128 — 8
4-204 8E
SS1 — 9
SS2 — 10

1	2	3	4	5	6	7	8	9	10
*			*		*			*	
	*		*		*			*	
		*	*		*			*	
*		*		*		*			*
	*	*		*		*			*
*							*		
	*						*		
		*					*		
			*	*		*			*

Moo Mod 7 Force AHDO ..8B, 4-209 3B

A
Mod 7 Force PLC ..8B; 4-208 2D
Clock 1-2



Note 1
K24 is operated by an auxiliary contact on the S4 current limit switch to block a coil protect check when the switch is open and the current is limited.

When both SS (D) and SS (E) are off, (Not) power off reset starts SS (D). When SS (D) times out, SS (E) and SS (F) start. When SS (E) times out, SS (G) starts. If the current sense reed relay point is closed (indication of current passing through the check reed relay) during this 150 ns (SSF) pulse, and S4 is on, SS (K) starts. When SS (K) times out, SS (L) starts and should another sample check reed pulse find the check reed relay point closed again (5 ms later) the Coil Protect latch is set

Current flow could be due to turning a HD on due to print compare. If this is the case, the block check latch is set preventing the check. The block check latch is reset after every sample.

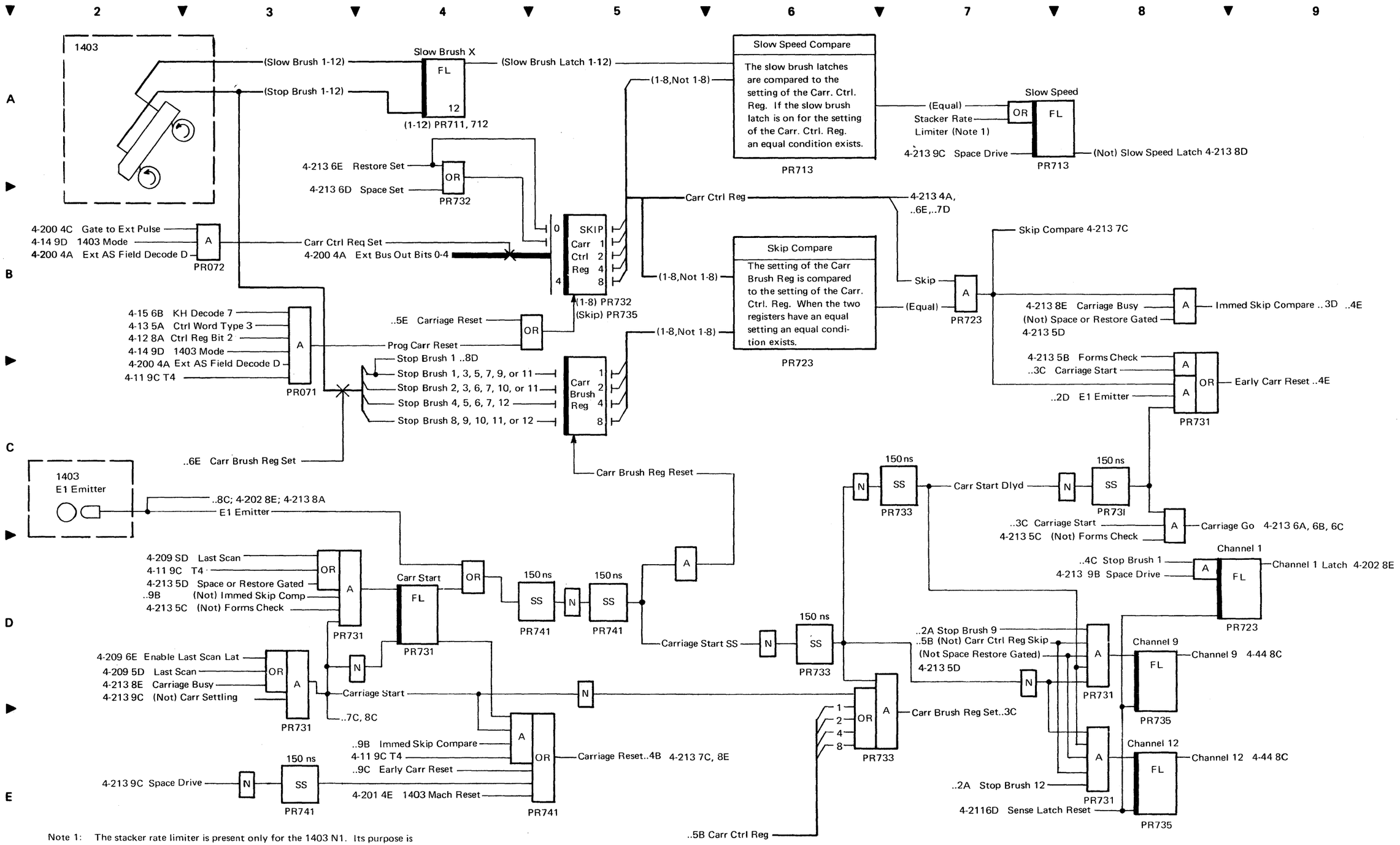
Coil protect is also set when an individual HD cannot be reset during print scans. This error can be bypassed with S3 (6B).

Note 1
With current limited coil protect checks can occur while in a print operation, but hammers do not fire and print ready is not dropped. The +60 volt line is limited by a 100 ohm resistor. This allows checking for the failing position while printing.

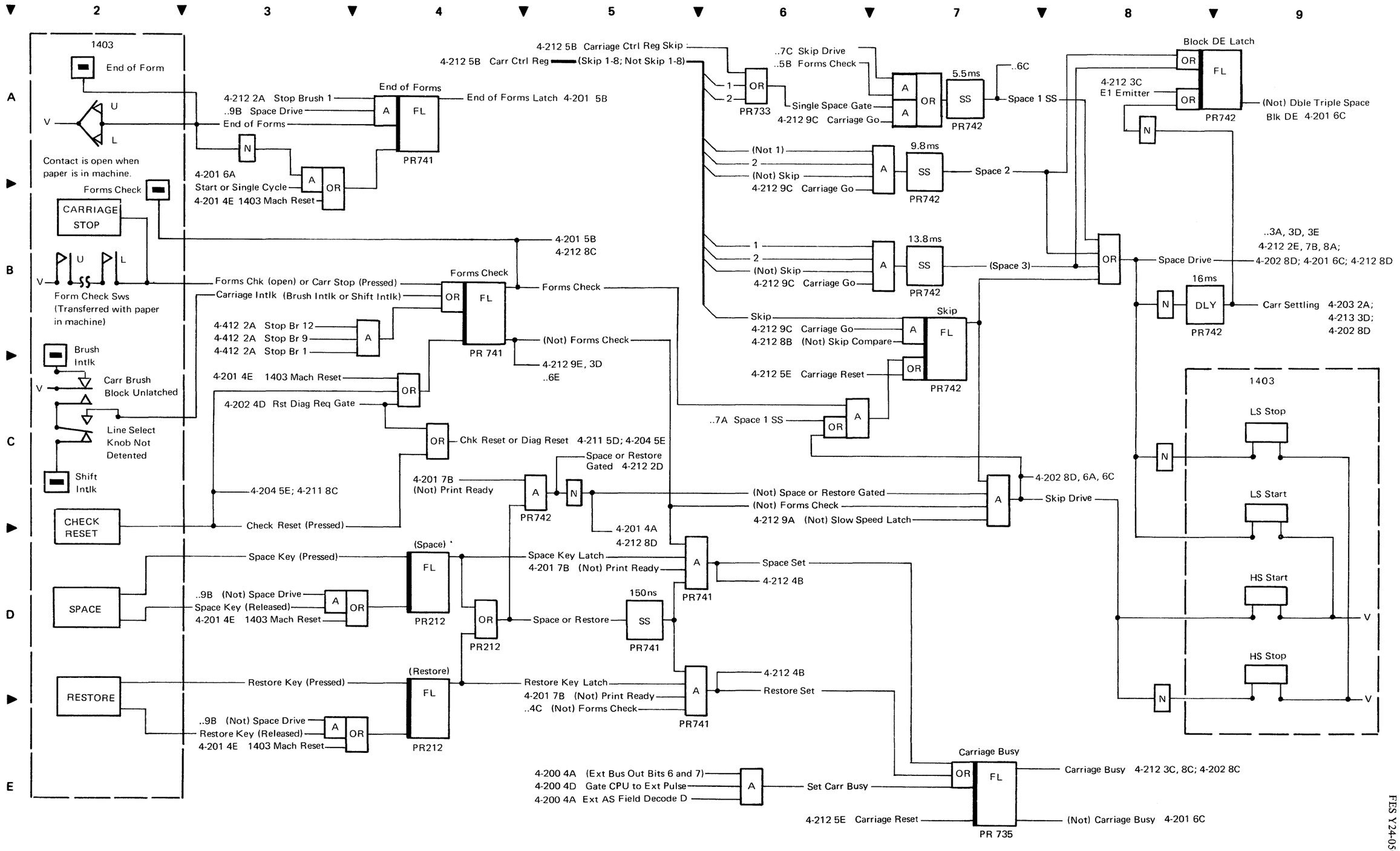
Form Y24-3529-0
FES Y24-0094

● Diagram 4-212. Carriage Compare and Channel Latches 1, 9, and 12

Form Y24-3529-0
FES Y24-0094

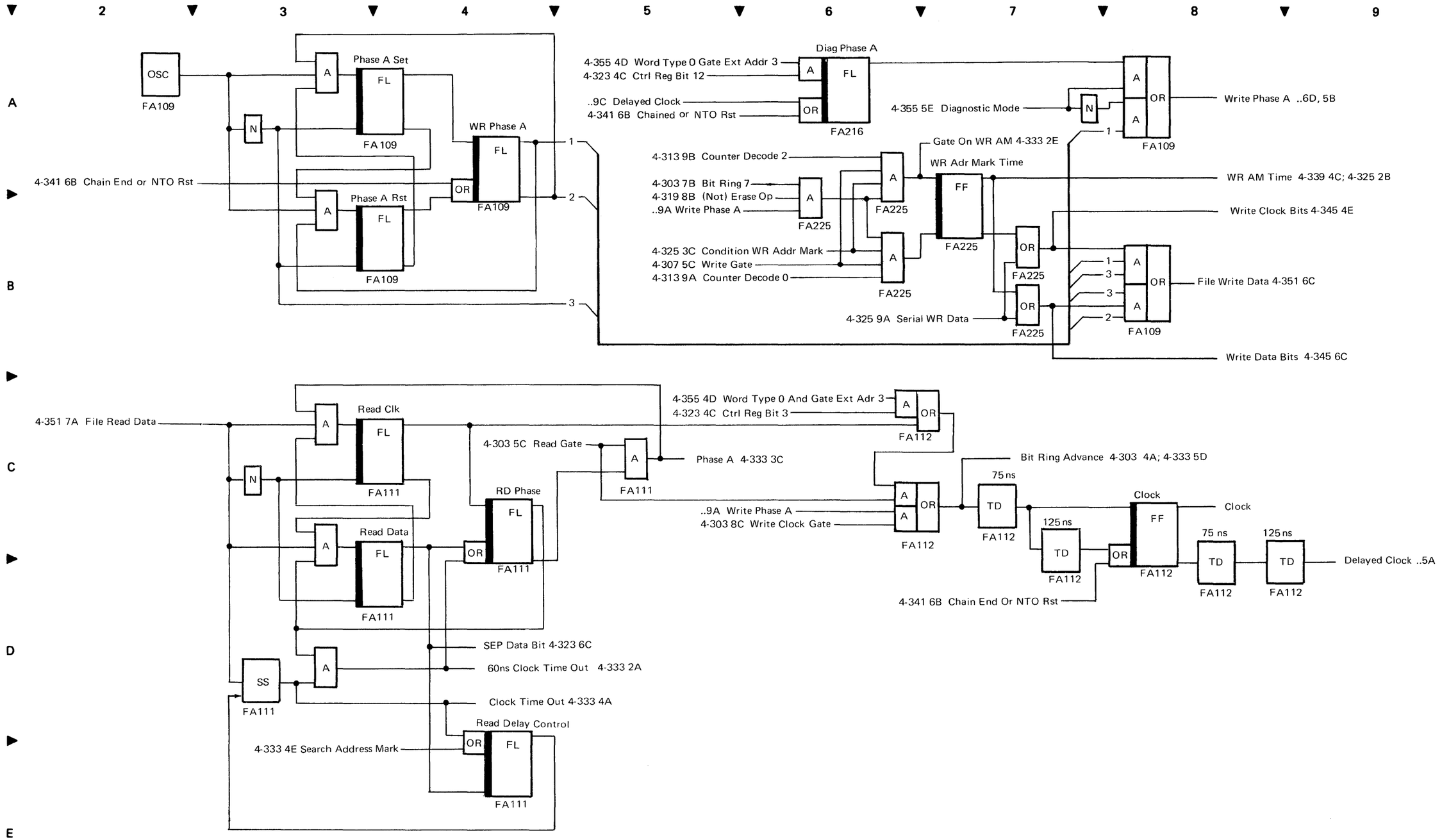


Note 1: The stacker rate limiter is present only for the 1403 N1. Its purpose is to determine that the carriage has been in high speed for such a length of time that 8 inches of paper has accumulated ahead of the stacker drive. The slow speed latch is set and the remainder of the skip is done in slow speed allowing the accumulated paper to be stacked.



Form Y24-3529-0
FES Y24-0503

Diagram 4-301. Read and Write Data/Clock Pulse Controls



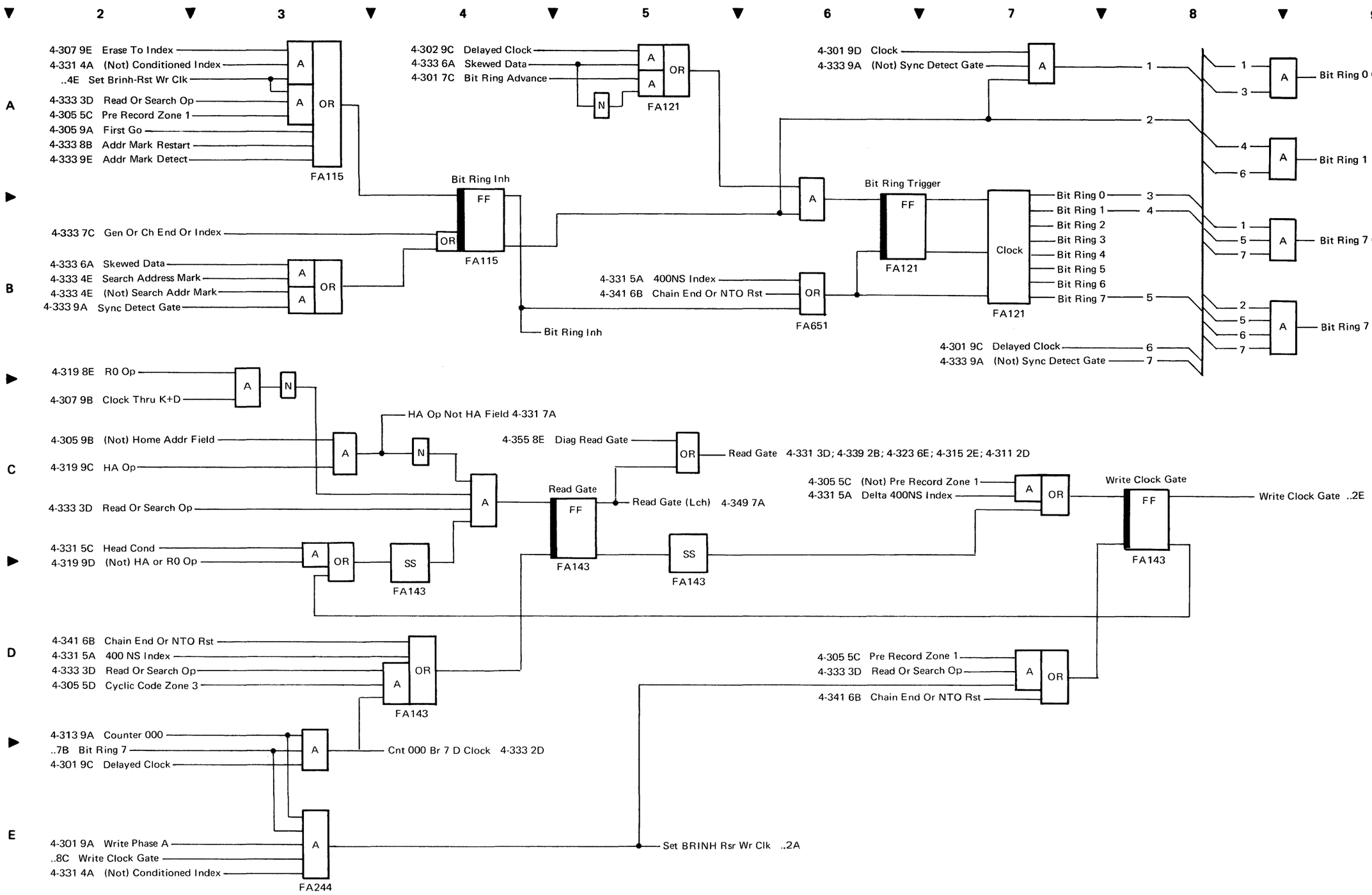
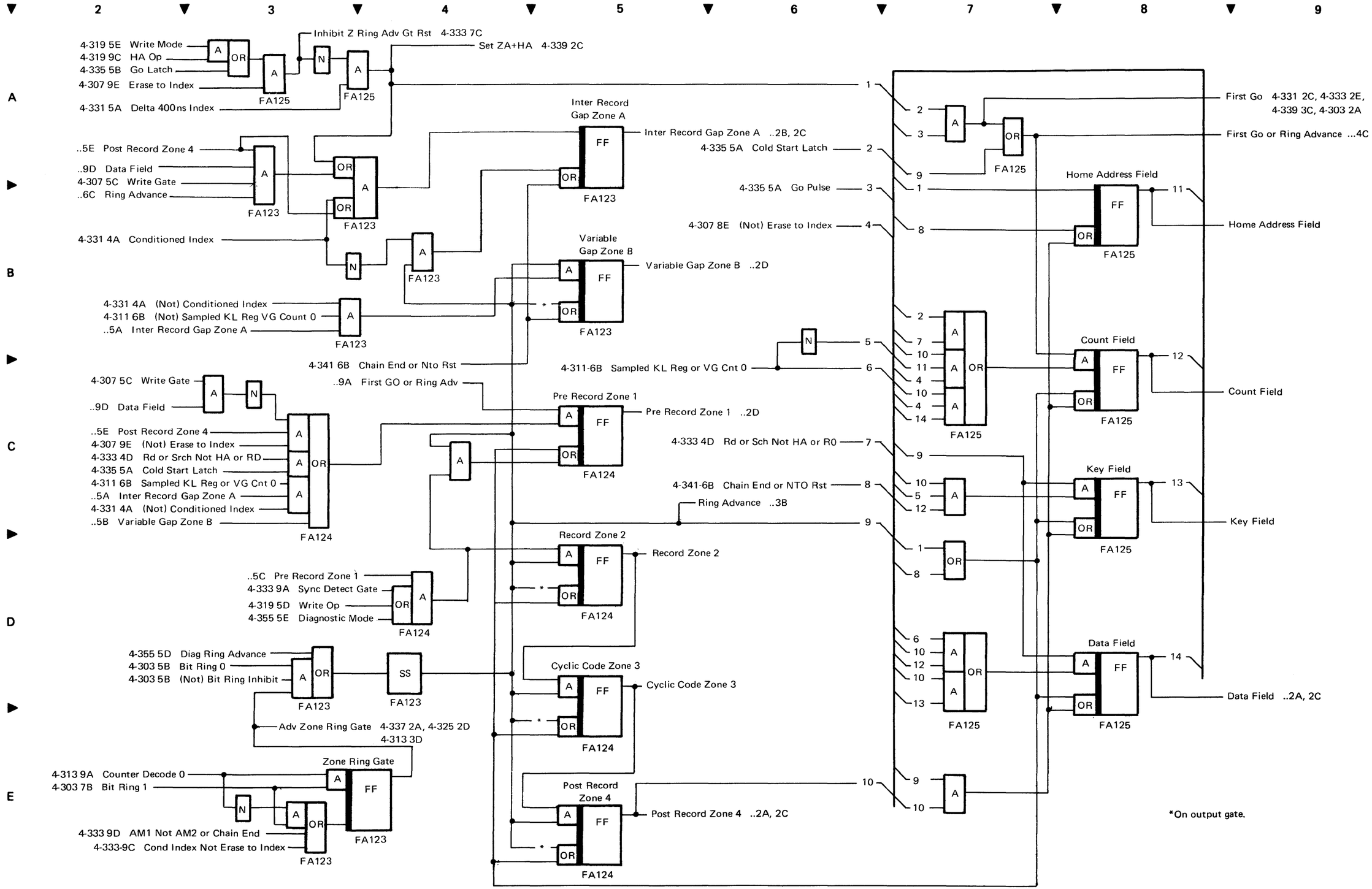

2
3
4
5
6
7
8
9
A
B
C
D
E
4-307 9E Erase To Index
4-331 4A (Not) Conditioned Index
..4E Set Brinh-Rst Wr Clk
4-333 3D Read Or Search Op
4-305 5C Pre Record Zone 1
4-305 9A First Go
4-333 8B Addr Mark Restart
4-333 9E Addr Mark Detect
A
A
OR
FA115
4-302 9C Delayed Clock
4-333 6A Skewed Data
4-301 7C Bit Ring Advance
A
A
OR
N
FA121
4-301 9D Clock
4-333 9A (Not) Sync Detect Gate
A
1
2
Bit Ring Inh
FF
OR
FA115
4-333 7C Gen Or Ch End Or Index
4-333 6A Skewed Data
4-333 4E Search Address Mark
4-333 4E (Not) Search Addr Mark
4-333 9A Sync Detect Gate
A
A
OR
Bit Ring Inh
A
Bit Ring Trigger
FF
FA121
4-331 5A 400NS Index
4-341 6B Chain End Or NTO Rst
OR
FA651
Clock
Bit Ring 0
Bit Ring 1
Bit Ring 2
Bit Ring 3
Bit Ring 4
Bit Ring 5
Bit Ring 6
Bit Ring 7
FA121
3
4
5
4-301 9C Delayed Clock
4-333 9A (Not) Sync Detect Gate
6
7
1
3
A
Bit Ring 0 Clock
4
6
A
Bit Ring 1 Delta Clk
1
5
7
A
Bit Ring 7 Clock
2
5
6
7
A
Bit Ring 7 Delta Clk
4-319 8E R0 Op
4-307 9B Clock Thru K+D
A
N
HA Op Not HA Field 4-331 7A
4-305 9B (Not) Home Addr Field
4-319 9C HA Op
A
N
4-355 8E Diag Read Gate
OR
Read Gate 4-331 3D; 4-339 2B; 4-323 6E; 4-315 2E; 4-311 2D
4-333 3D Read Or Search Op
A
Read Gate
FF
Read Gate (Lch) 4-349 7A
4-305 5C (Not) Pre Record Zone 1
4-331 5A Delta 400NS Index
A
OR
Write Clock Gate
FF
Write Clock Gate ..2E
FA143
4-331 5C Head Cond
4-319 9D (Not) HA or R0 Op
A
OR
SS
FA143
SS
FA143
FA143
4-341 6B Chain End Or NTO Rst
4-331 5A 400 NS Index
4-333 3D Read Or Search Op
4-305 5D Cyclic Code Zone 3
A
OR
FA143
4-305 5C Pre Record Zone 1
4-333 3D Read Or Search Op
4-341 6B Chain End Or NTO Rst
A
OR
4-313 9A Counter 000
..7B Bit Ring 7
4-301 9C Delayed Clock
A
Cnt 000 Br 7 D Clock 4-333 2D
4-301 9A Write Phase A
..8C Write Clock Gate
4-331 4A (Not) Conditioned Index
A
FA244
Set BRINH Rsr Wr Clk ..2A

Diagram 4-305. Field and Zone Rings



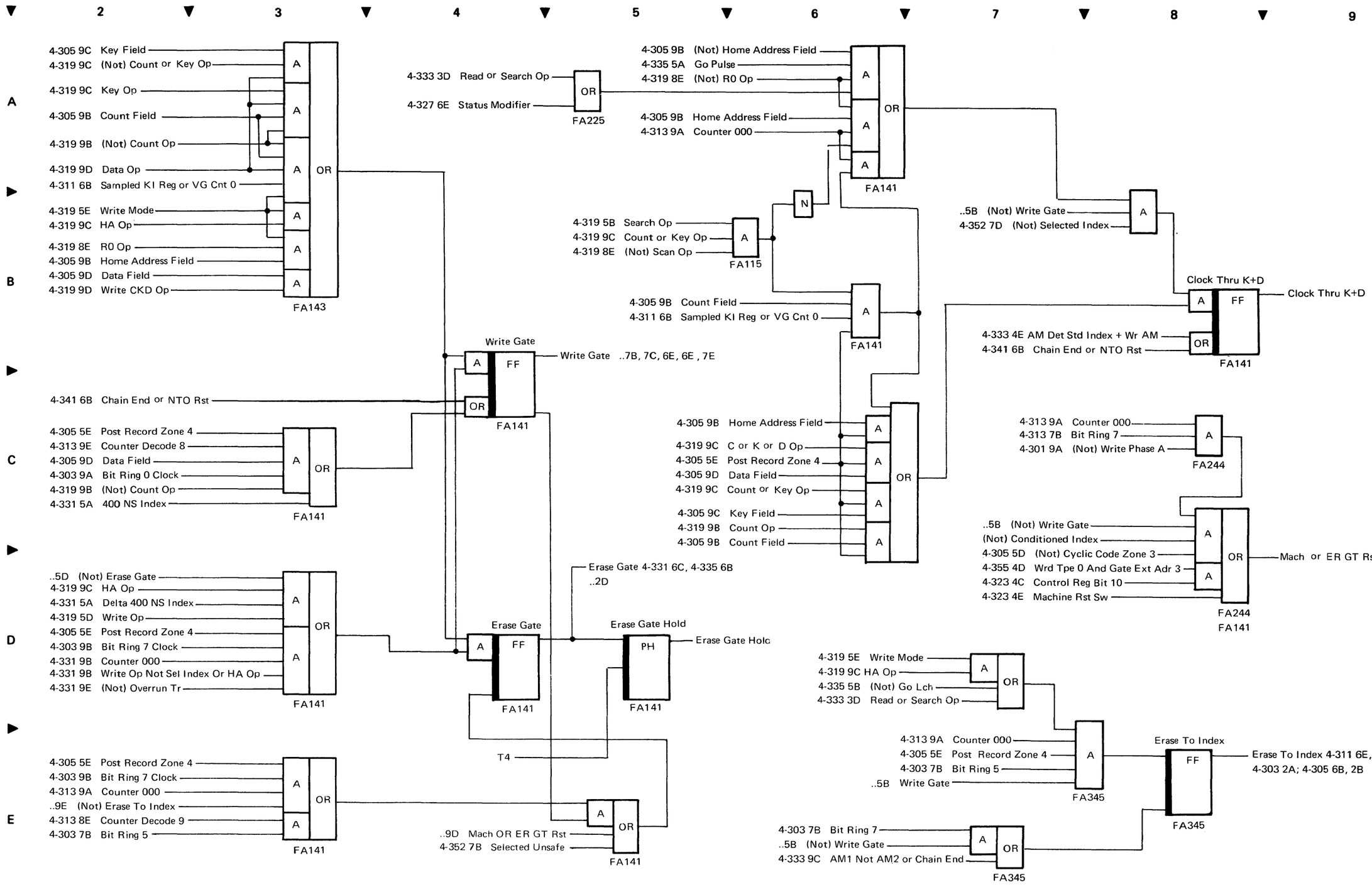
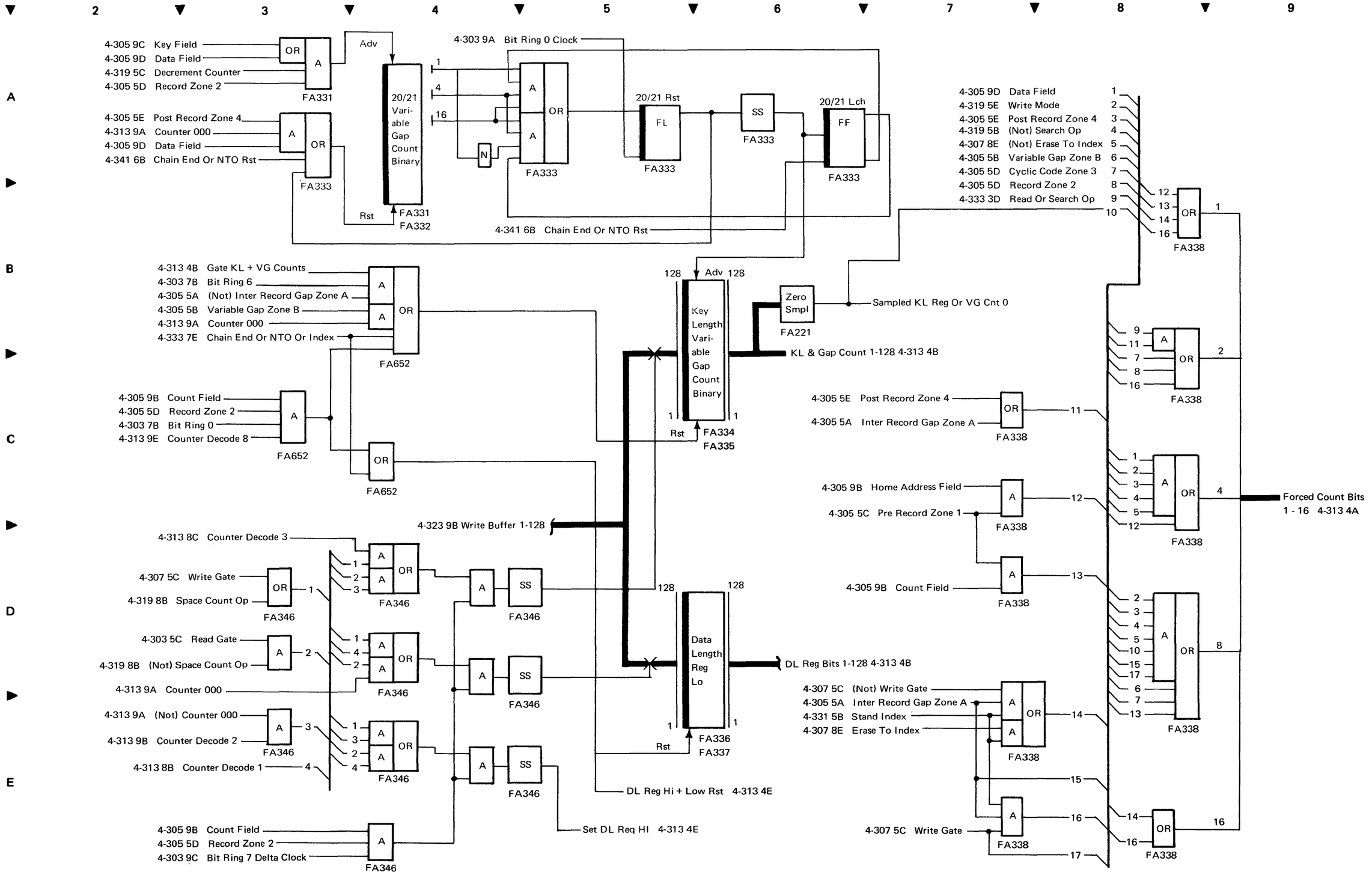
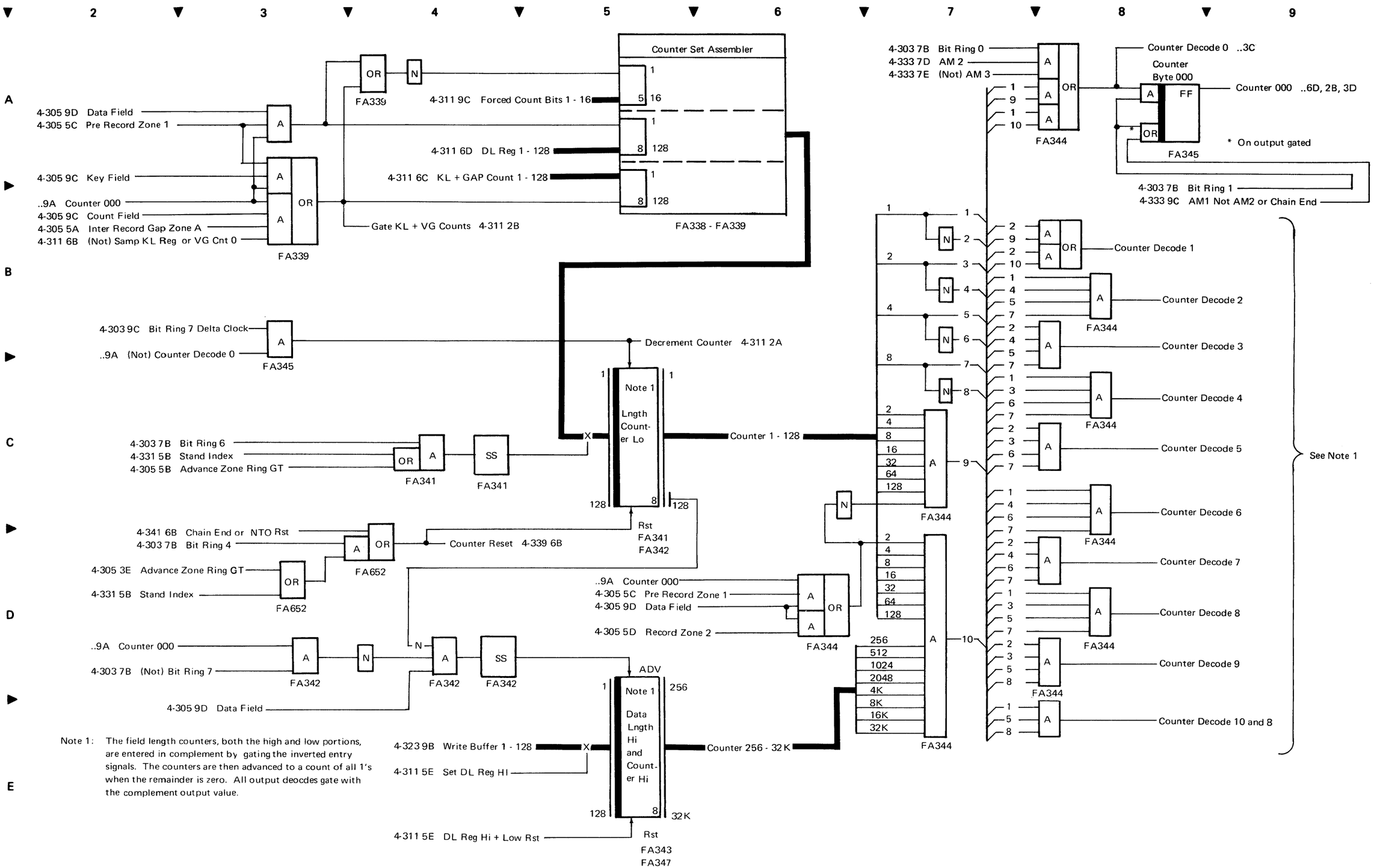

2
3
4
5
6
7
8
9
A
B
C
D
E
4-305 9C Key Field
4-319 9C (Not) Count or Key Op
4-319 9C Key Op
4-305 9B Count Field
4-319 9B (Not) Count Op
4-319 9D Data Op
4-311 6B Sampled KI Reg or VG Cnt 0
4-319 5E Write Mode
4-319 9C HA Op
4-319 8E R0 Op
4-305 9B Home Address Field
4-305 9D Data Field
4-319 9D Write CKD Op
A
OR
FA143
4-333 3D Read or Search Op
4-327 6E Status Modifier
OR
FA225
4-305 9B (Not) Home Address Field
4-335 5A Go Pulse
4-319 8E (Not) R0 Op
4-305 9B Home Address Field
4-313 9A Counter 000
A
OR
FA141
N
4-319 5B Search Op
4-319 9C Count or Key Op
4-319 8E (Not) Scan Op
A
FA115
..5B (Not) Write Gate
4-352 7D (Not) Selected Index
A
Clock Thru K+D
A
FF
Clock Thru K+D
4-333 4E AM Det Std Index + Wr AM
4-341 6B Chain End or NTO Rst
OR
FA141
4-305 9B Count Field
4-311 6B Sampled KI Reg or VG Cnt 0
A
FA141
Write Gate
A
FF
Write Gate ..7B, 7C, 6E, 6E , 7E
4-341 6B Chain End or NTO Rst
OR
FA141
4-305 9B Home Address Field
4-319 9C C or K or D Op
4-305 5E Post Record Zone 4
4-305 9D Data Field
4-319 9C Count or Key Op
4-305 9C Key Field
4-319 9B Count Op
4-305 9B Count Field
A
A
A
OR
4-313 9A Counter 000
4-313 7B Bit Ring 7
4-301 9A (Not) Write Phase A
A
FA244
4-305 5E Post Record Zone 4
4-313 9E Counter Decode 8
4-305 9D Data Field
4-303 9A Bit Ring 0 Clock
4-319 9B (Not) Count Op
4-331 5A 400 NS Index
A
OR
FA141
..5B (Not) Write Gate
(Not) Conditioned Index
4-305 5D (Not) Cyclic Code Zone 3
4-355 4D Wrd Tpe 0 And Gate Ext Adr 3
4-323 4C Control Reg Bit 10
4-323 4E Machine Rst Sw
A
A
OR
Mach or ER GT Rst ..4E
FA244
FA141
Erase Gate 4-331 6C, 4-335 6B
..2D
..5D (Not) Erase Gate
4-319 9C HA Op
4-331 5A Delta 400 NS Index
4-319 5D Write Op
4-305 5E Post Record Zone 4
4-303 9B Bit Ring 7 Clock
4-331 9B Counter 000
4-331 9B Write Op Not Sel Index Or HA Op
4-331 9E (Not) Overrun Tr
A
A
OR
FA141
Erase Gate
A
FF
FA141
Erase Gate Hold
PH
FA141
Erase Gate Hold
4-319 5E Write Mode
4-319 9C HA Op
4-335 5B (Not) Go Lch
4-333 3D Read or Search Op
A
OR
4-313 9A Counter 000
4-305 5E Post Record Zone 4
4-303 7B Bit Ring 5
..5B Write Gate
A
FA345
Erase To Index
FF
FA345
Erase To Index 4-311 6E, 7B, ..2E
4-303 2A; 4-305 6B, 2B
T4
4-305 5E Post Record Zone 4
4-303 9B Bit Ring 7 Clock
4-313 9A Counter 000
..9E (Not) Erase To Index
4-313 8E Counter Decode 9
4-303 7B Bit Ring 5
A
A
OR
FA141
A
OR
..9D Mach OR ER GT Rst
4-352 7B Selected Unsafe
FA141
4-303 7B Bit Ring 7
..5B (Not) Write Gate
4-333 9C AM1 Not AM2 or Chain End
A
OR
FA345

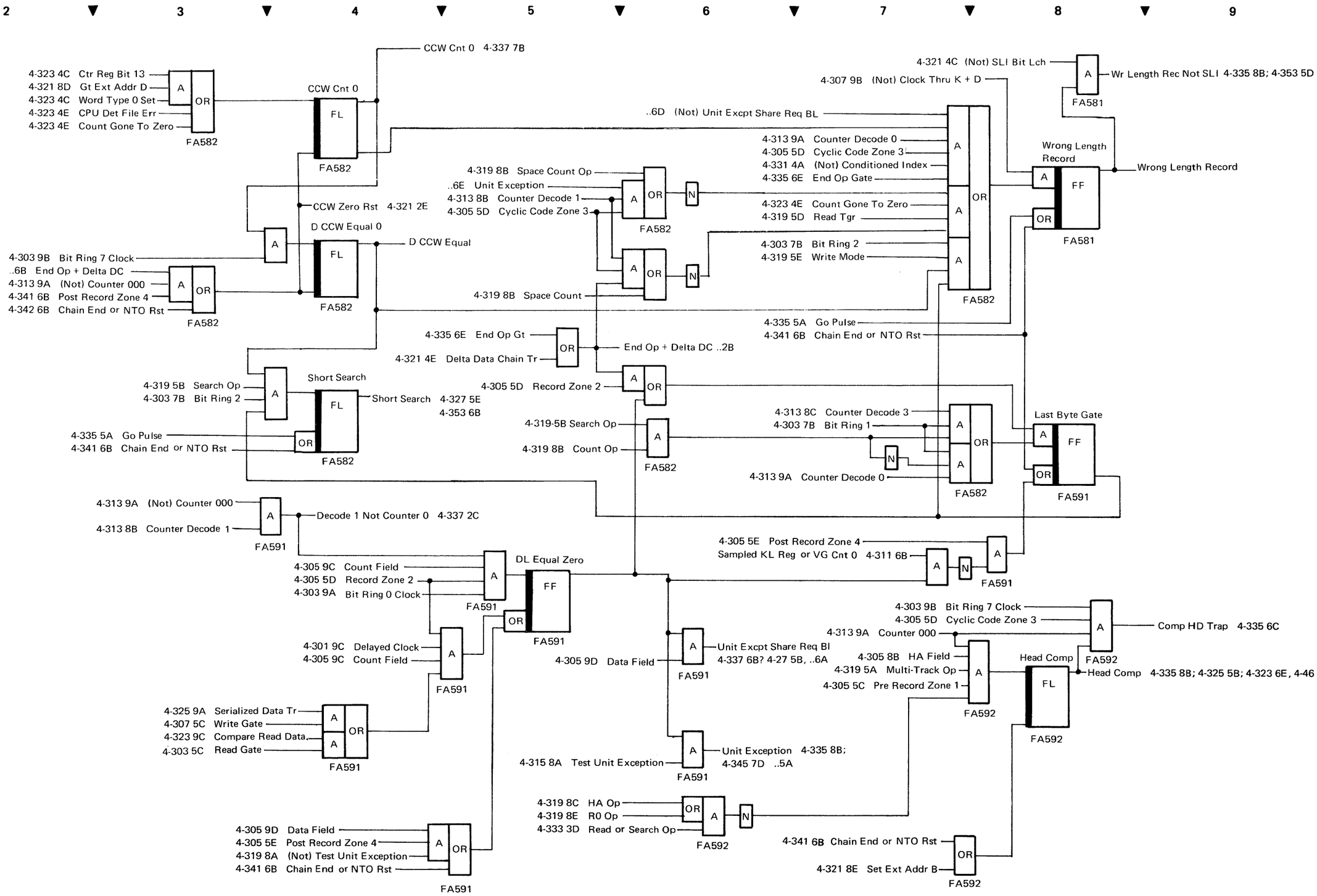
Diagram 4-311. Field Length Registers and Gap Controls





Note 1: The field length counters, both the high and low portions, are entered in complement by gating the inverted entry signals. The counters are then advanced to a count of all 1's when the remainder is zero. All output deocdes gate with the complement output value.

Diagram 4-315. Record Length Controls



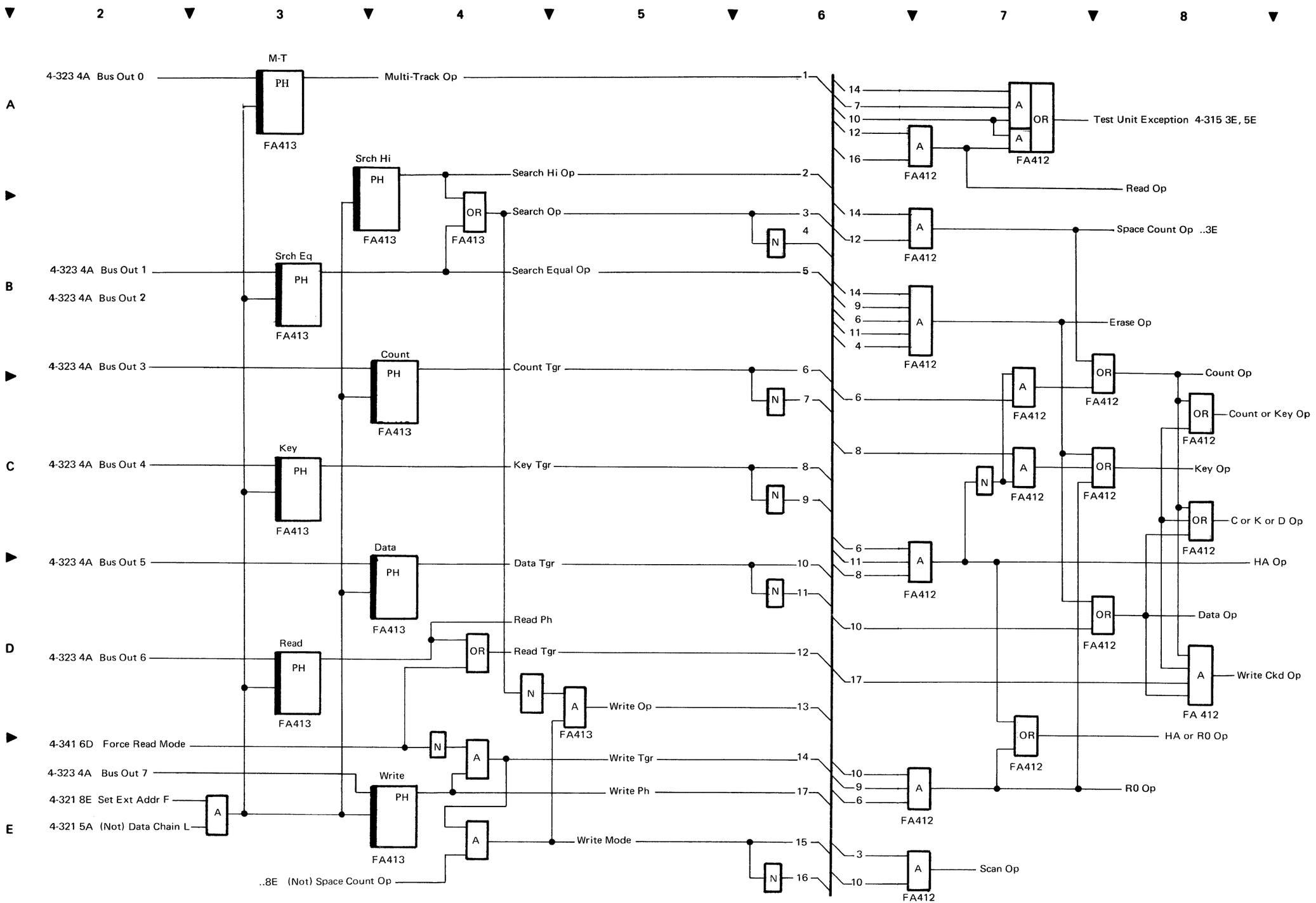
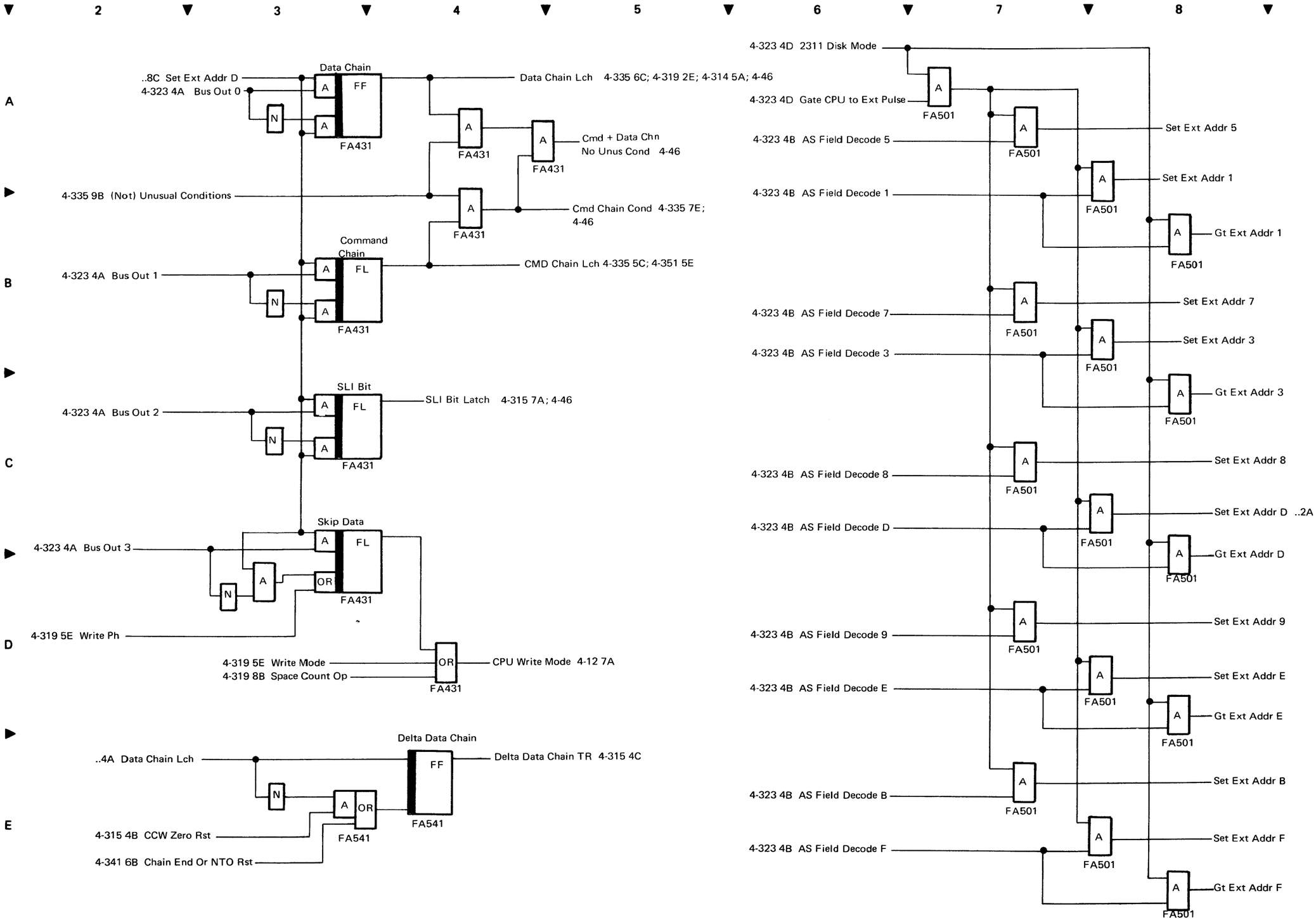
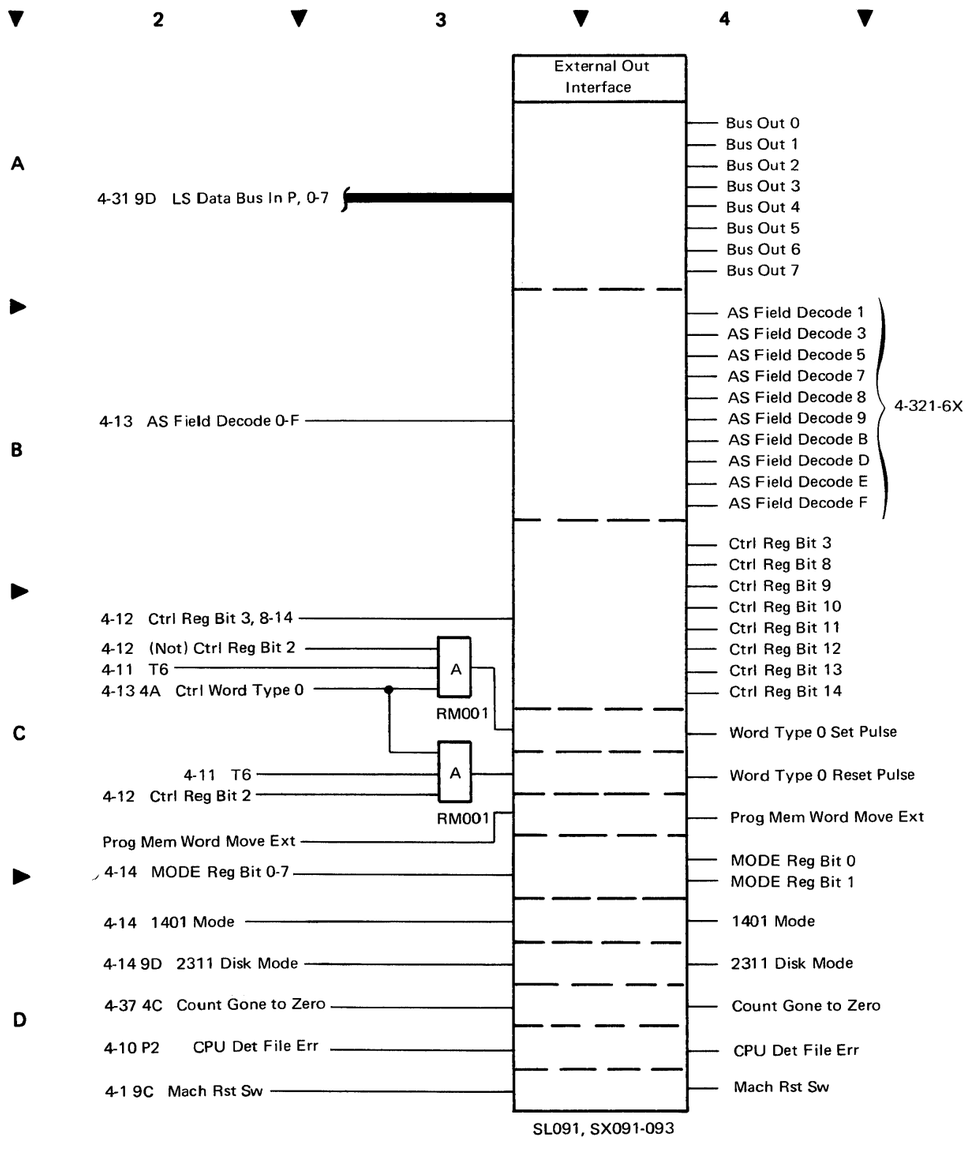

2
3
4
5
6
7
8
9
A
B
C
D
E
4-323 4A Bus Out 0
M-T
PH
FA413
Multi-Track Op
Srch Hi
Search Hi Op
OR
Search Op
4-323 4A Bus Out 1
4-323 4A Bus Out 2
Srch Eq
Search Equal Op
4-323 4A Bus Out 3
Count
Count Tgr
Key
4-323 4A Bus Out 4
Key Tgr
4-323 4A Bus Out 5
Data
Data Tgr
Read Ph
4-323 4A Bus Out 6
Read
Read Tgr
N
A
Write Op
FA413
4-341 6D Force Read Mode
4-323 4A Bus Out 7
Write
Write Tgr
Write Ph
4-321 8E Set Ext Addr F
4-321 5A (Not) Data Chain L
..8E (Not) Space Count Op
Write Mode
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
FA412
Test Unit Exception 4-315 3E, 5E
Read Op
Space Count Op ..3E
Erase Op
Count Op
Count or Key Op
Key Op
C or K or D Op
HA Op
Data Op
Write Ckd Op
HA or R0 Op
R0 Op
Scan Op

Diagram 4-321. CCW Flag Register and External Decodes




2
3
4
5
External Out Interface
4-31 9D LS Data Bus In P, 0-7
Bus Out 0
Bus Out 1
Bus Out 2
Bus Out 3
Bus Out 4
Bus Out 5
Bus Out 6
Bus Out 7
AS Field Decode 1
AS Field Decode 3
AS Field Decode 5
AS Field Decode 7
AS Field Decode 8
AS Field Decode 9
AS Field Decode B
AS Field Decode D
AS Field Decode E
AS Field Decode F
4-321-6X
4-13 AS Field Decode 0-F
Ctrl Reg Bit 3
Ctrl Reg Bit 8
Ctrl Reg Bit 9
Ctrl Reg Bit 10
Ctrl Reg Bit 11
Ctrl Reg Bit 12
Ctrl Reg Bit 13
Ctrl Reg Bit 14
4-12 Ctrl Reg Bit 3, 8-14
4-12 (Not) Ctrl Reg Bit 2
4-11 T6
4-13 4A Ctrl Word Type 0
A
RM001
4-11 T6
4-12 Ctrl Reg Bit 2
A
RM001
Word Type 0 Set Pulse
Word Type 0 Reset Pulse
Prog Mem Word Move Ext
Prog Mem Word Move Ext
4-14 MODE Reg Bit 0-7
MODE Reg Bit 0
MODE Reg Bit 1
4-14 1401 Mode
1401 Mode
4-14 9D 2311 Disk Mode
2311 Disk Mode
4-37 4C Count Gone to Zero
Count Gone to Zero
4-10 P2 CPU Det File Err
CPU Det File Err
4-1 9C Mach Rst Sw
Mach Rst Sw
SL091, SX091-093
A
B
C
D
E

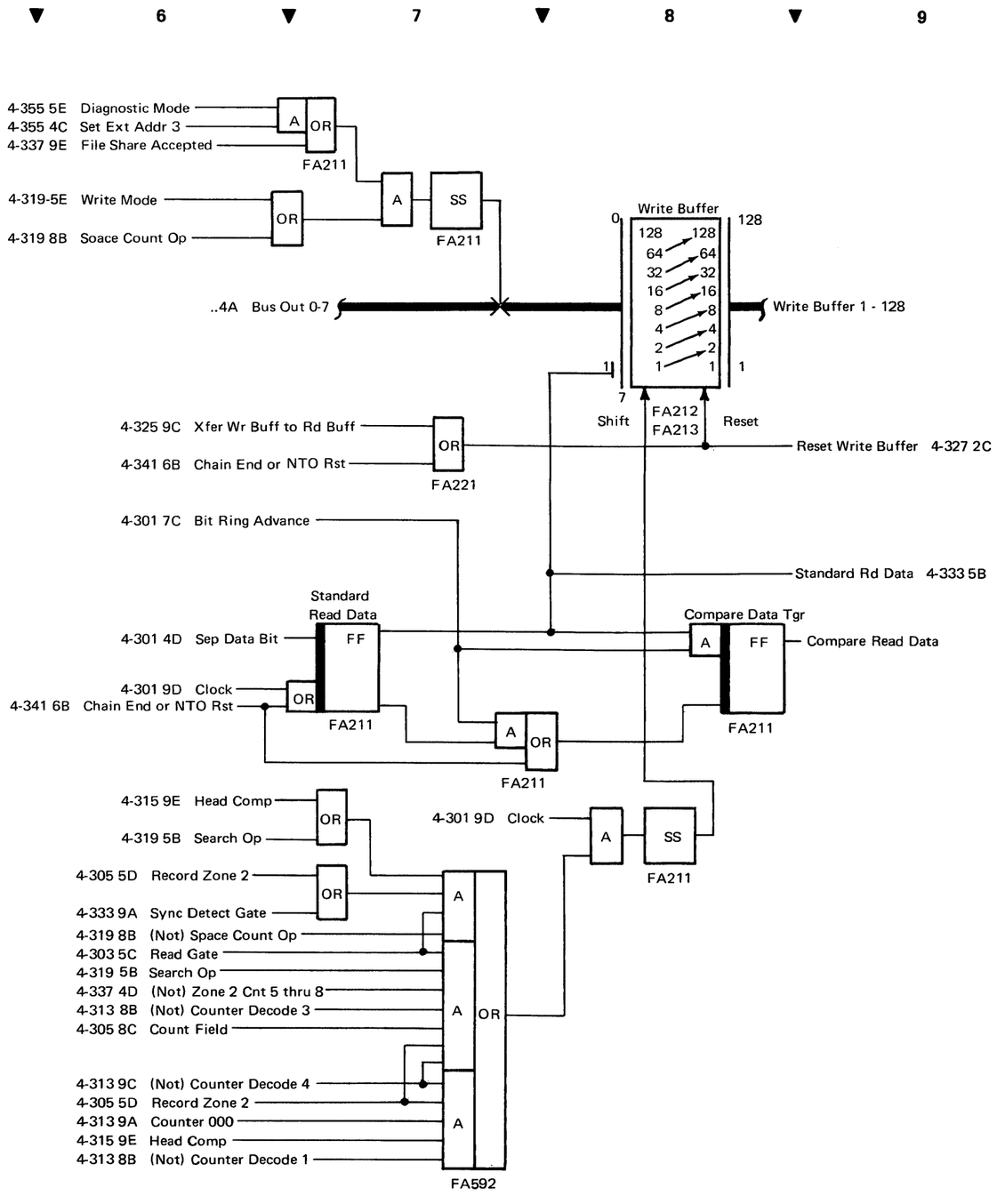
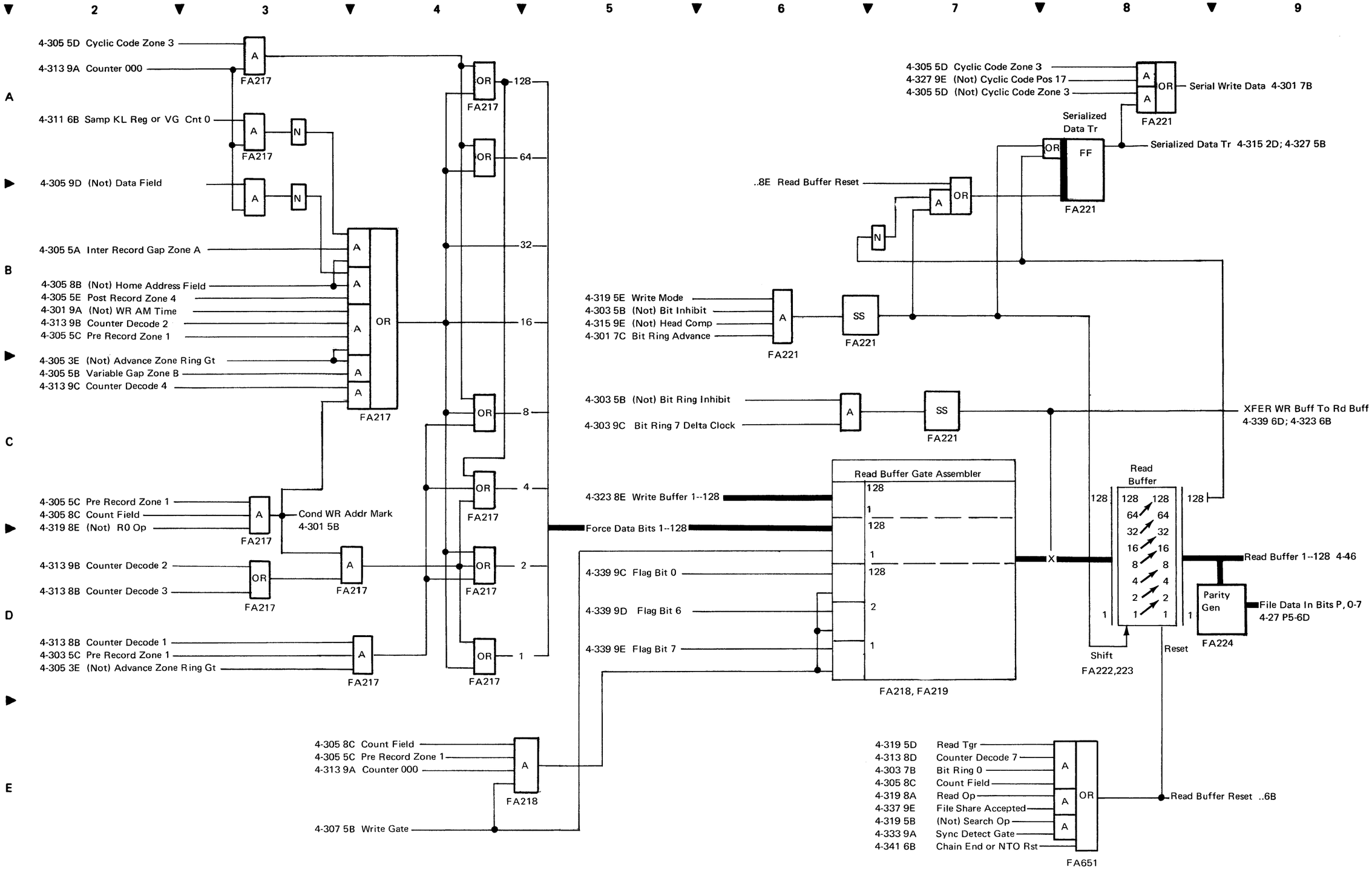

6
7
8
9
4-355 5E Diagnostic Mode
4-355 4C Set Ext Addr 3
4-337 9E File Share Accepted
A
OR
FA211
4-319-5E Write Mode
4-319 8B Soace Count Op
OR
A
SS
FA211
Write Buffer
0
128
128
64
32
16
8
4
2
1
128
64
32
16
8
4
2
1
1
7
1
..4A Bus Out 0-7
Write Buffer 1 - 128
Shift
FA212
FA213
Reset
4-325 9C Xfer Wr Buff to Rd Buff
4-341 6B Chain End or NTO Rst
OR
FA221
Reset Write Buffer 4-327 2C
4-301 7C Bit Ring Advance
Standard Rd Data 4-333 5B
Standard Read Data
4-301 4D Sep Data Bit
FF
4-301 9D Clock
4-341 6B Chain End or NTO Rst
OR
FA211
Compare Data Tgr
A
FF
FA211
Compare Read Data
A
OR
FA211
4-315 9E Head Comp
4-319 5B Search Op
OR
4-301 9D Clock
A
SS
FA211
4-305 5D Record Zone 2
4-333 9A Sync Detect Gate
4-319 8B (Not) Space Count Op
4-303 5C Read Gate
4-319 5B Search Op
4-337 4D (Not) Zone 2 Cnt 5 thru 8
4-313 8B (Not) Counter Decode 3
4-305 8C Count Field
A
A
OR
4-313 9C (Not) Counter Decode 4
4-305 5D Record Zone 2
4-313 9A Counter 000
4-315 9E Head Comp
4-313 8B (Not) Counter Decode 1
A
FA592

Diagram 4-325. Read Buffer and Assembler



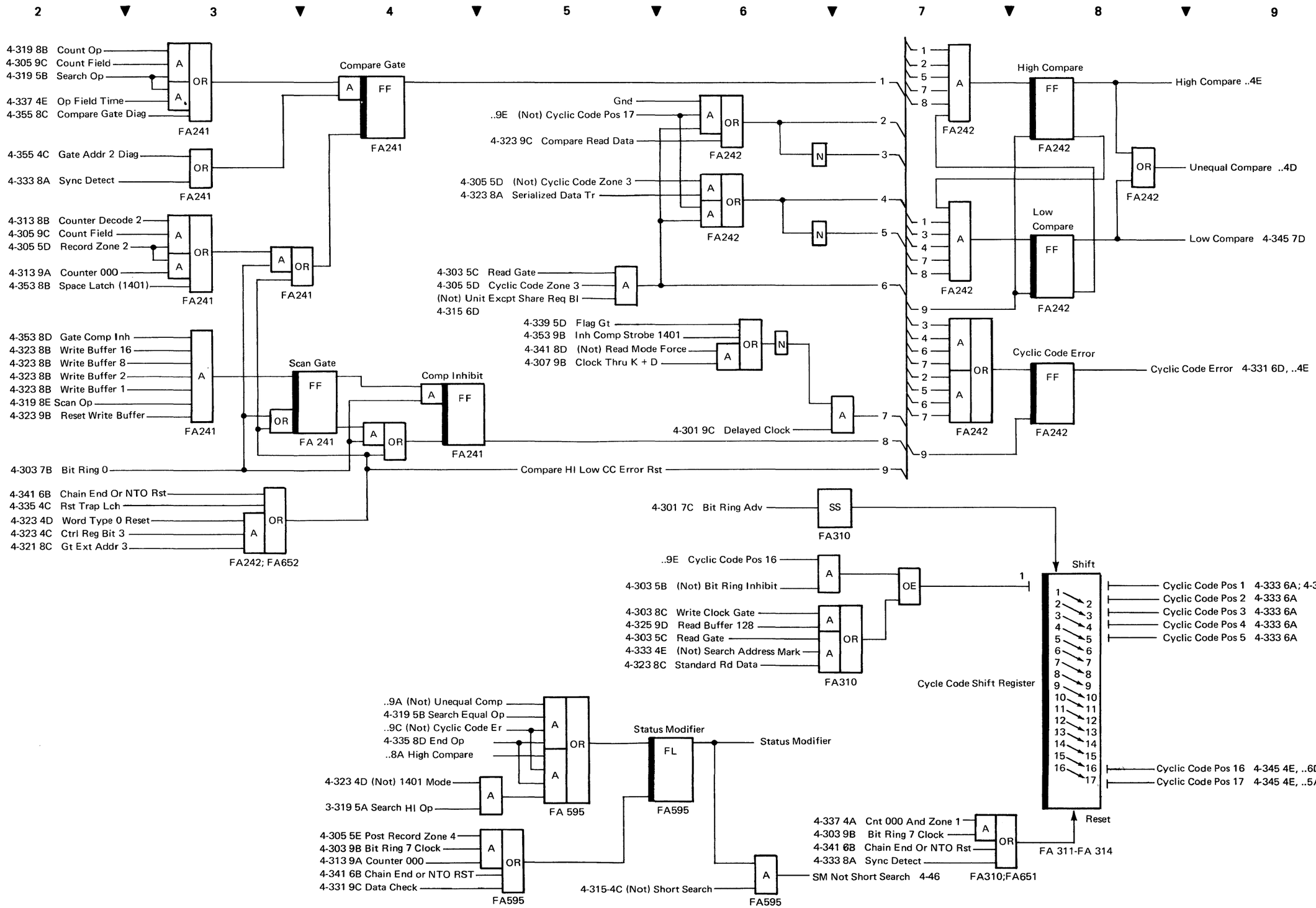
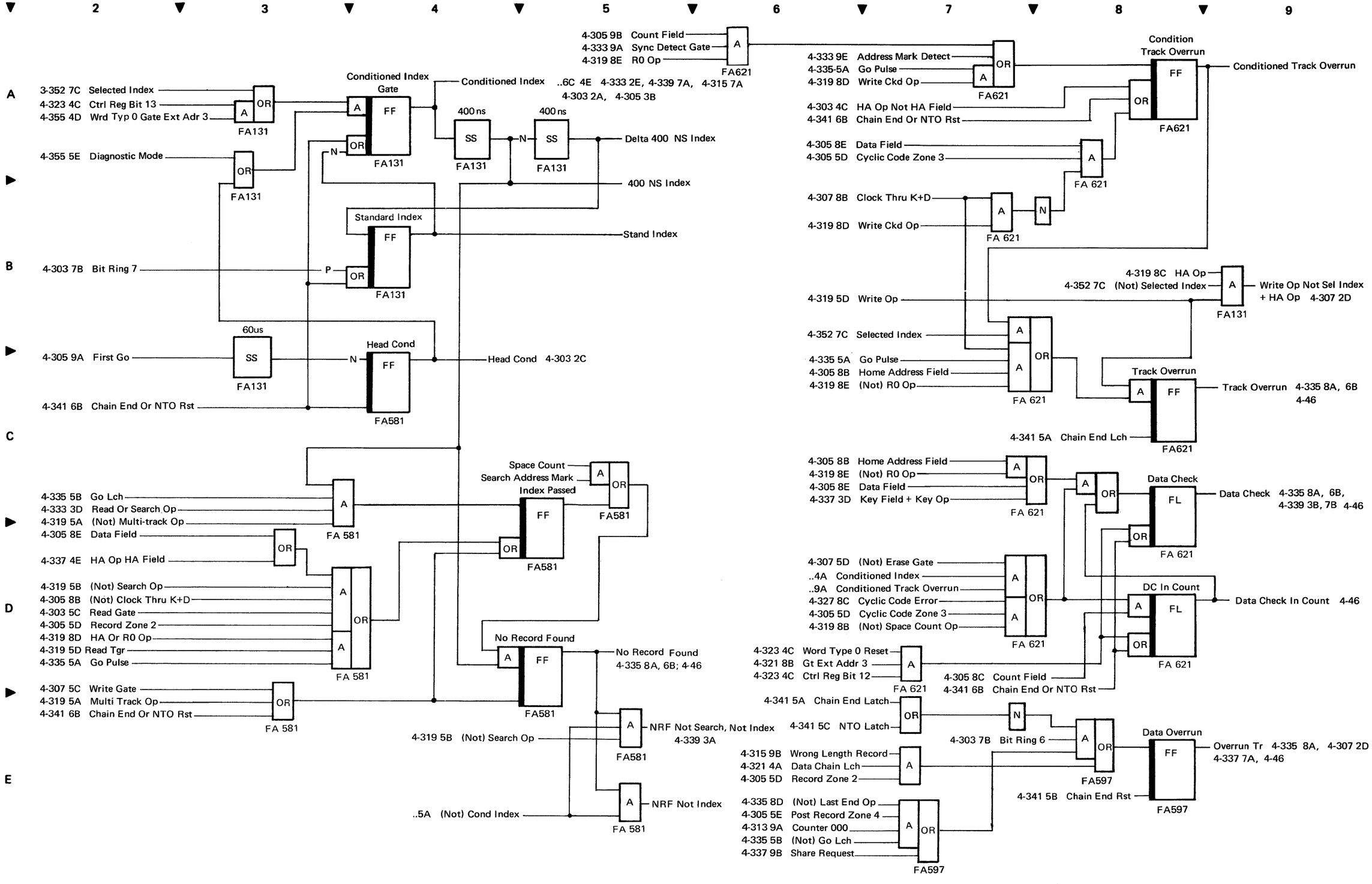

2
3
4
5
6
7
8
9
A
B
C
D
E
4-319 8B Count Op
4-305 9C Count Field
4-319 5B Search Op
4-337 4E Op Field Time
4-355 8C Compare Gate Diag
FA241
4-355 4C Gate Addr 2 Diag
4-333 8A Sync Detect
FA241
4-313 8B Counter Decode 2
4-305 9C Count Field
4-305 5D Record Zone 2
4-313 9A Counter 000
4-353 8B Space Latch (1401)
FA241
Compare Gate
FA241
FA241
4-353 8D Gate Comp Inh
4-323 8B Write Buffer 16
4-323 8B Write Buffer 8
4-323 8B Write Buffer 2
4-323 8B Write Buffer 1
4-319 8E Scan Op
4-323 9B Reset Write Buffer
FA241
Scan Gate
FA 241
Comp Inhibit
FA241
4-303 7B Bit Ring 0
Compare HI Low CC Error Rst
4-341 6B Chain End Or NTO Rst
4-335 4C Rst Trap Lch
4-323 4D Word Type 0 Reset
4-323 4C Ctrl Reg Bit 3
4-321 8C Gt Ext Addr 3
FA242; FA652
Gnd
..9E (Not) Cyclic Code Pos 17
4-323 9C Compare Read Data
FA242
4-305 5D (Not) Cyclic Code Zone 3
4-323 8A Serialized Data Tr
FA242
4-303 5C Read Gate
4-305 5D Cyclic Code Zone 3
(Not) Unit Excpt Share Req BI
4-315 6D
4-339 5D Flag Gt
4-353 9B Inh Comp Strobe 1401
4-341 8D (Not) Read Mode Force
4-307 9B Clock Thru K + D
4-301 9C Delayed Clock
1 2 5 7 8
1 3 4 7 8
3 4 6 7 2 5 6 7
9
FA242
High Compare
FA242
High Compare ..4E
OR
Unequal Compare ..4D
FA242
Low Compare
FA242
Low Compare 4-345 7D
Cyclic Code Error
FA242
Cyclic Code Error 4-331 6D, ..4E
4-301 7C Bit Ring Adv
SS
FA310
..9E Cyclic Code Pos 16
4-303 5B (Not) Bit Ring Inhibit
OE
1
4-303 8C Write Clock Gate
4-325 9D Read Buffer 128
4-303 5C Read Gate
4-333 4E (Not) Search Address Mark
4-323 8C Standard Rd Data
FA310
Shift
Cycle Code Shift Register
Cyclic Code Pos 1 4-333 6A; 4-345 4E
Cyclic Code Pos 2 4-333 6A
Cyclic Code Pos 3 4-333 6A
Cyclic Code Pos 4 4-333 6A
Cyclic Code Pos 5 4-333 6A
Cyclic Code Pos 16 4-345 4E, ..6D
Cyclic Code Pos 17 4-345 4E, ..5A
Reset
..9A (Not) Unequal Comp
4-319 5B Search Equal Op
..9C (Not) Cyclic Code Er
4-335 8D End Op
..8A High Compare
4-323 4D (Not) 1401 Mode
3-319 5A Search HI Op
FA 595
Status Modifier
FL
FA595
Status Modifier
4-305 5E Post Record Zone 4
4-303 9B Bit Ring 7 Clock
4-313 9A Counter 000
4-341 6B Chain End or NTO RST
4-331 9C Data Check
FA595
4-315-4C (Not) Short Search
FA595
4-337 4A Cnt 000 And Zone 1
4-303 9B Bit Ring 7 Clock
4-341 6B Chain End Or NTO Rst
4-333 8A Sync Detect
SM Not Short Search 4-46
FA310;FA651
FA 311-FA 314

Diagram 4-331. Index Controls and Overrun Detection



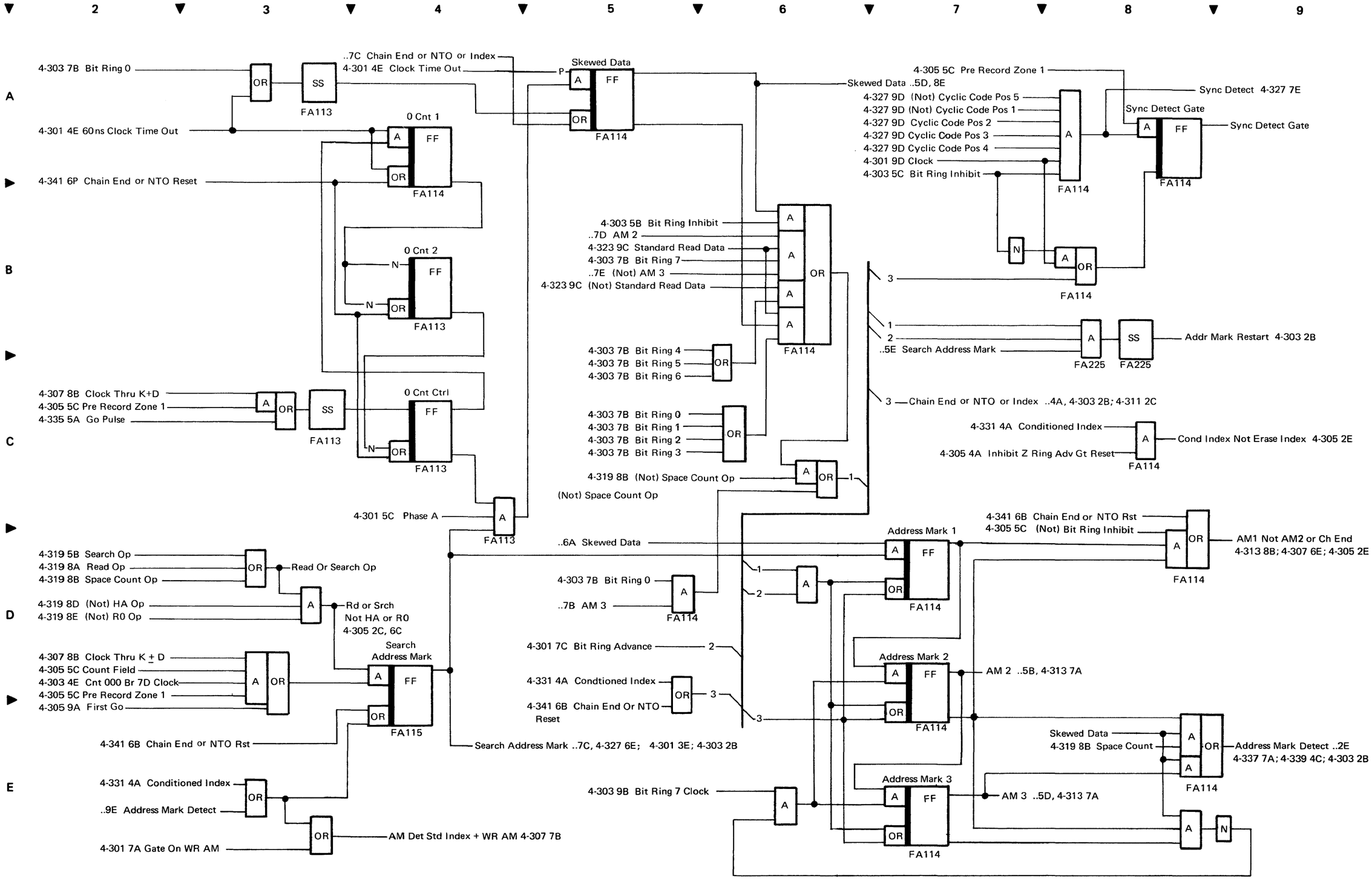
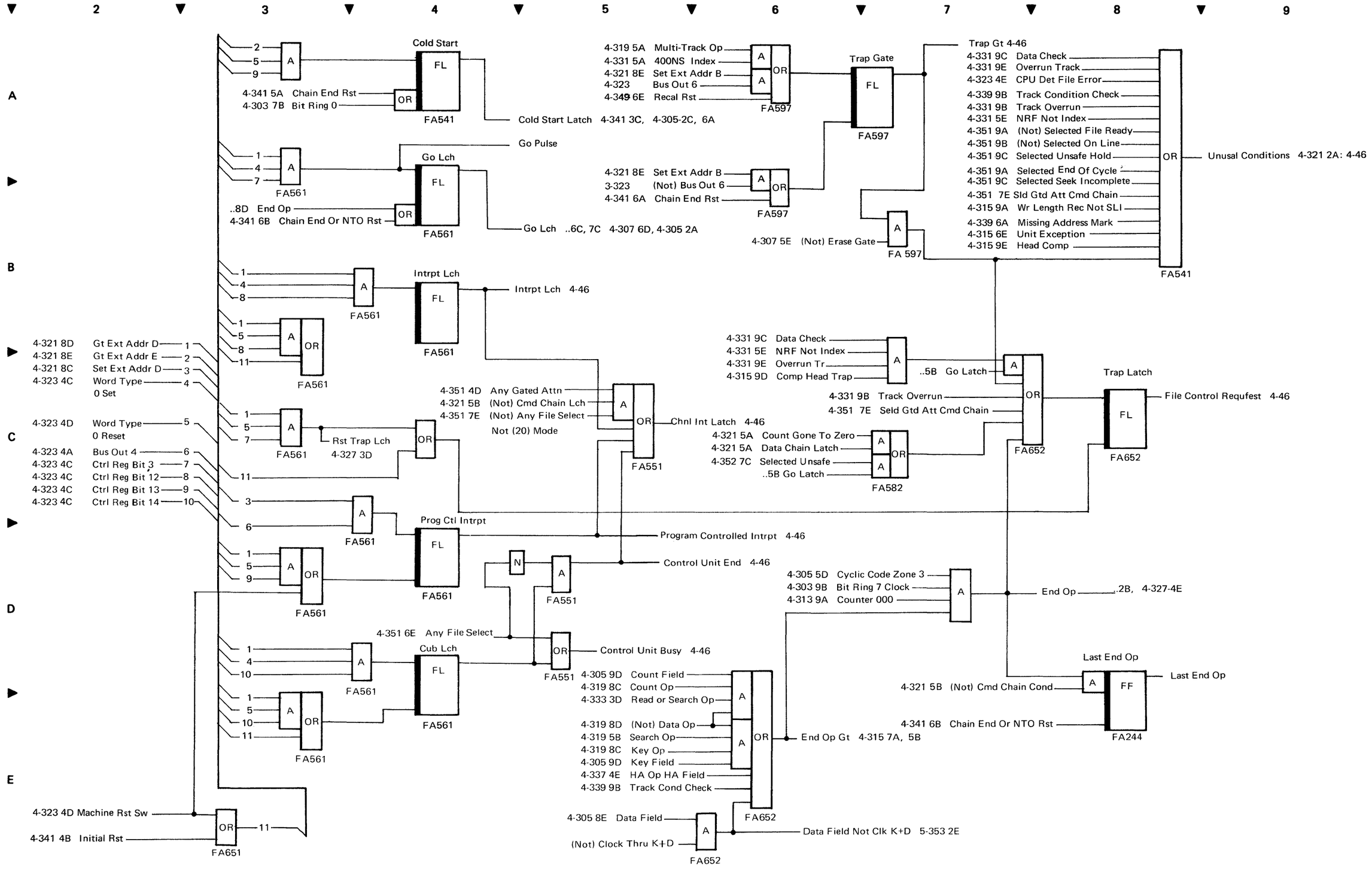

2
3
4
5
6
7
8
9
A
B
C
D
E
4-303 7B Bit Ring 0
OR
SS
FA113
..7C Chain End or NTO or Index
4-301 4E Clock Time Out
Skewed Data
P
A
FF
OR
FA114
4-305 5C Pre Record Zone 1
Skewed Data ..5D, 8E
4-327 9D (Not) Cyclic Code Pos 5
4-327 9D (Not) Cyclic Code Pos 1
4-327 9D Cyclic Code Pos 2
4-327 9D Cyclic Code Pos 3
4-327 9D Cyclic Code Pos 4
4-301 9D Clock
4-303 5C Bit Ring Inhibit
Sync Detect 4-327 7E
Sync Detect Gate
Sync Detect Gate
4-301 4E 60ns Clock Time Out
0 Cnt 1
4-341 6P Chain End or NTO Reset
0 Cnt 2
N
0 Cnt Ctrl
4-307 8B Clock Thru K+D
4-305 5C Pre Record Zone 1
4-335 5A Go Pulse
4-303 5B Bit Ring Inhibit
..7D AM 2
4-323 9C Standard Read Data
4-303 7B Bit Ring 7
..7E (Not) AM 3
4-323 9C (Not) Standard Read Data
4-303 7B Bit Ring 4
4-303 7B Bit Ring 5
4-303 7B Bit Ring 6
4-303 7B Bit Ring 0
4-303 7B Bit Ring 1
4-303 7B Bit Ring 2
4-303 7B Bit Ring 3
4-319 8B (Not) Space Count Op
(Not) Space Count Op
3
1
2
..5E Search Address Mark
Addr Mark Restart 4-303 2B
FA225
3 — Chain End or NTO or Index ..4A, 4-303 2B; 4-311 2C
4-331 4A Conditioned Index
4-305 4A Inhibit Z Ring Adv Gt Reset
Cond Index Not Erase Index 4-305 2E
4-301 5C Phase A
..6A Skewed Data
4-319 5B Search Op
4-319 8A Read Op
4-319 8B Space Count Op
Read Or Search Op
4-319 8D (Not) HA Op
4-319 8E (Not) R0 Op
Rd or Srch
Not HA or R0
4-305 2C, 6C
4-303 7B Bit Ring 0
..7B AM 3
Address Mark 1
4-341 6B Chain End or NTO Rst
4-305 5C (Not) Bit Ring Inhibit
AM1 Not AM2 or Ch End
4-313 8B; 4-307 6E; 4-305 2E
4-301 7C Bit Ring Advance
4-331 4A Condtioned Index
4-341 6B Chain End Or NTO Reset
Address Mark 2
AM 2 ..5B, 4-313 7A
4-307 8B Clock Thru K ± D
4-305 5C Count Field
4-303 4E Cnt 000 Br 7D Clock
4-305 5C Pre Record Zone 1
4-305 9A First Go
Search Address Mark
4-341 6B Chain End or NTO Rst
Search Address Mark ..7C, 4-327 6E; 4-301 3E; 4-303 2B
Skewed Data
4-319 8B Space Count
Address Mark Detect ..2E
4-337 7A; 4-339 4C; 4-303 2B
Address Mark 3
4-303 9B Bit Ring 7 Clock
AM 3 ..5D, 4-313 7A
4-331 4A Conditioned Index
..9E Address Mark Detect
4-301 7A Gate On WR AM
AM Det Std Index + WR AM 4-307 7B

Diagram 4-335. Interrupt and Trap Controls



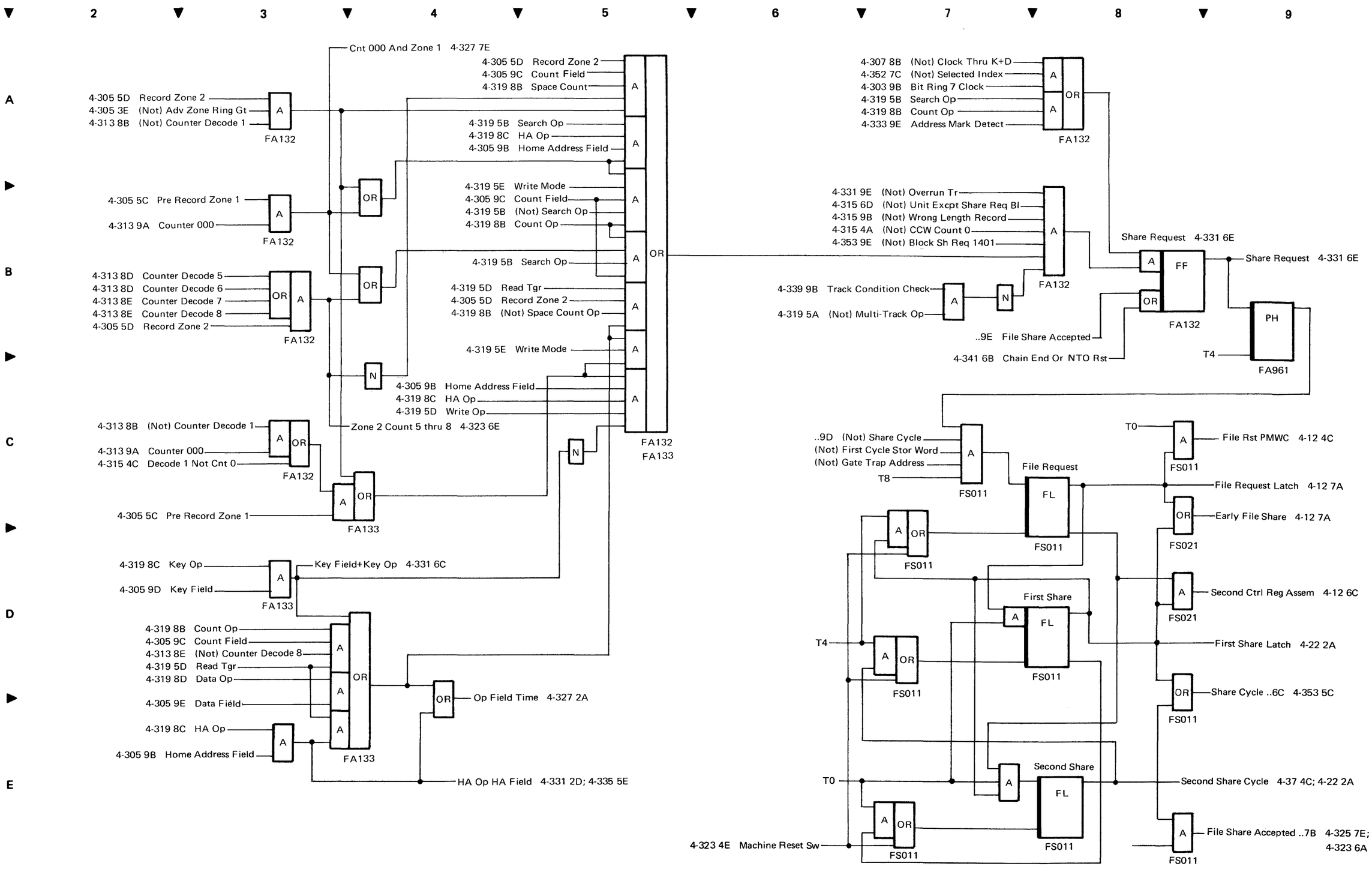
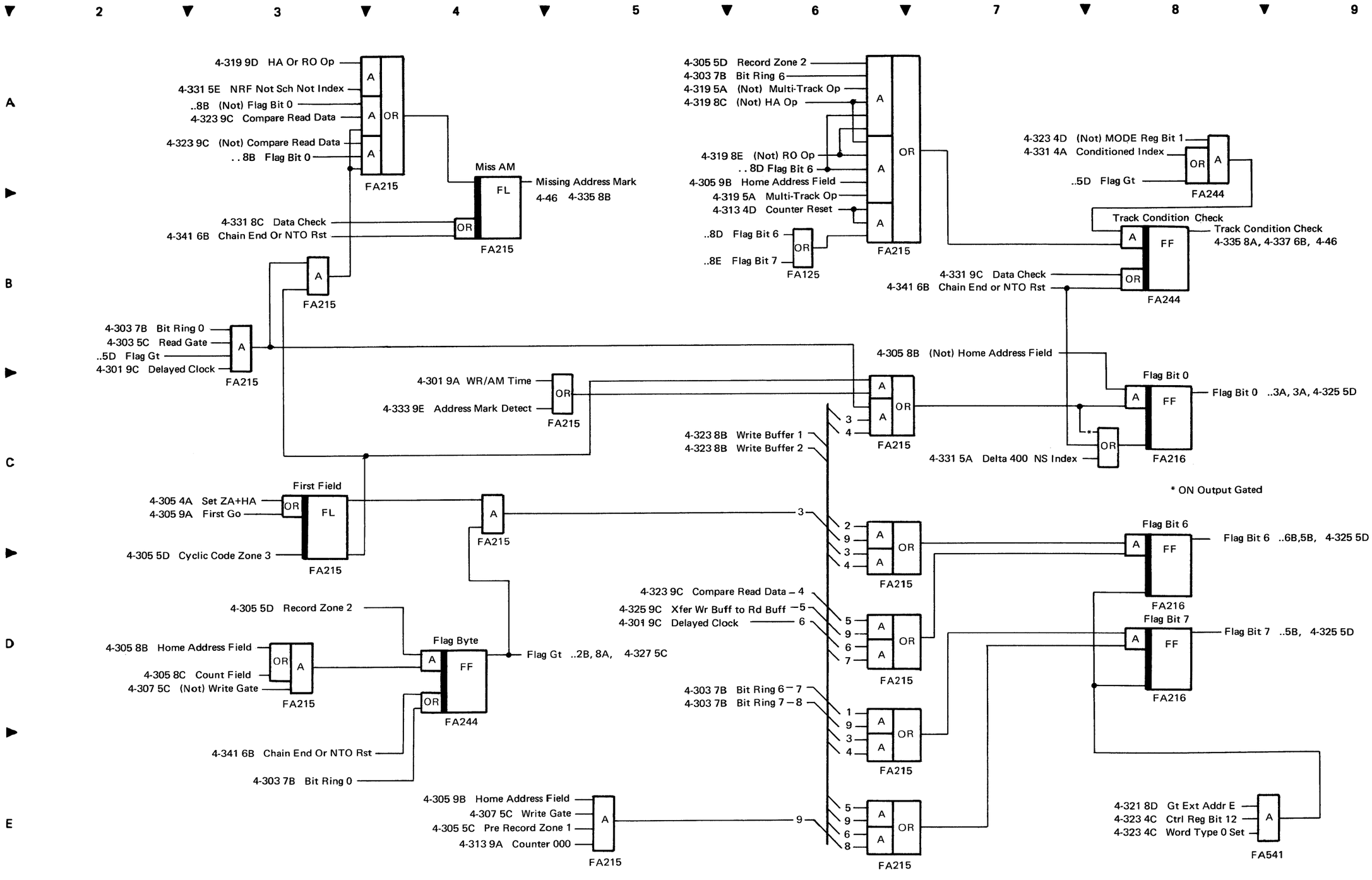

2
3
4
5
6
7
8
9
A
B
C
D
E
Cnt 000 And Zone 1 4-327 7E
4-305 5D Record Zone 2
4-305 3E (Not) Adv Zone Ring Gt
4-313 8B (Not) Counter Decode 1
A
FA132
4-305 5C Pre Record Zone 1
4-313 9A Counter 000
A
FA132
OR
4-313 8D Counter Decode 5
4-313 8D Counter Decode 6
4-313 8E Counter Decode 7
4-313 8E Counter Decode 8
4-305 5D Record Zone 2
OR
A
FA132
OR
N
4-313 8B (Not) Counter Decode 1
4-313 9A Counter 000
4-315 4C Decode 1 Not Cnt 0
A
OR
FA132
4-305 5C Pre Record Zone 1
A
OR
FA133
Zone 2 Count 5 thru 8 4-323 6E
4-305 5D Record Zone 2
4-305 9C Count Field
4-319 8B Space Count
A
4-319 5B Search Op
4-319 8C HA Op
4-305 9B Home Address Field
A
4-319 5E Write Mode
4-305 9C Count Field
4-319 5B (Not) Search Op
4-319 8B Count Op
A
4-319 5B Search Op
A
OR
4-319 5D Read Tgr
4-305 5D Record Zone 2
4-319 8B (Not) Space Count Op
A
4-319 5E Write Mode
A
4-305 9B Home Address Field
4-319 8C HA Op
4-319 5D Write Op
A
FA132
FA133
N
4-319 8C Key Op
4-305 9D Key Field
A
FA133
Key Field+Key Op 4-331 6C
4-319 8B Count Op
4-305 9C Count Field
4-313 8E (Not) Counter Decode 8
4-319 5D Read Tgr
4-319 8D Data Op
4-305 9E Data Field
4-319 8C HA Op
4-305 9B Home Address Field
A
A
A
OR
FA133
OR
Op Field Time 4-327 2A
HA Op HA Field 4-331 2D; 4-335 5E
4-307 8B (Not) Clock Thru K+D
4-352 7C (Not) Selected Index
4-303 9B Bit Ring 7 Clock
4-319 5B Search Op
4-319 8B Count Op
4-333 9E Address Mark Detect
A
A
OR
FA132
4-331 9E (Not) Overrun Tr
4-315 6D (Not) Unit Excpt Share Req Bl
4-315 9B (Not) Wrong Length Record
4-315 4A (Not) CCW Count 0
4-353 9E (Not) Block Sh Req 1401
A
FA132
4-339 9B Track Condition Check
4-319 5A (Not) Multi-Track Op
A
N
Share Request 4-331 6E
A
FF
OR
FA132
Share Request 4-331 6E
..9E File Share Accepted
4-341 6B Chain End Or NTO Rst
PH
T4
FA961
..9D (Not) Share Cycle
(Not) First Cycle Stor Word
(Not) Gate Trap Address
T8
A
FS011
File Request
FL
FS011
T0
A
FS011
File Rst PMWC 4-12 4C
File Request Latch 4-12 7A
A
OR
FS011
FS011
OR
FS021
Early File Share 4-12 7A
First Share
A
FL
FS011
T4
A
OR
FS011
A
FS021
Second Ctrl Reg Assem 4-12 6C
First Share Latch 4-22 2A
OR
FS011
Share Cycle ..6C 4-353 5C
Second Share
T0
A
FL
FS011
Second Share Cycle 4-37 4C; 4-22 2A
4-323 4E Machine Reset Sw
A
OR
FS011
A
FS011
File Share Accepted ..7B 4-325 7E;
4-323 6A

Diagram 4-339. Track Condition Flag Controls



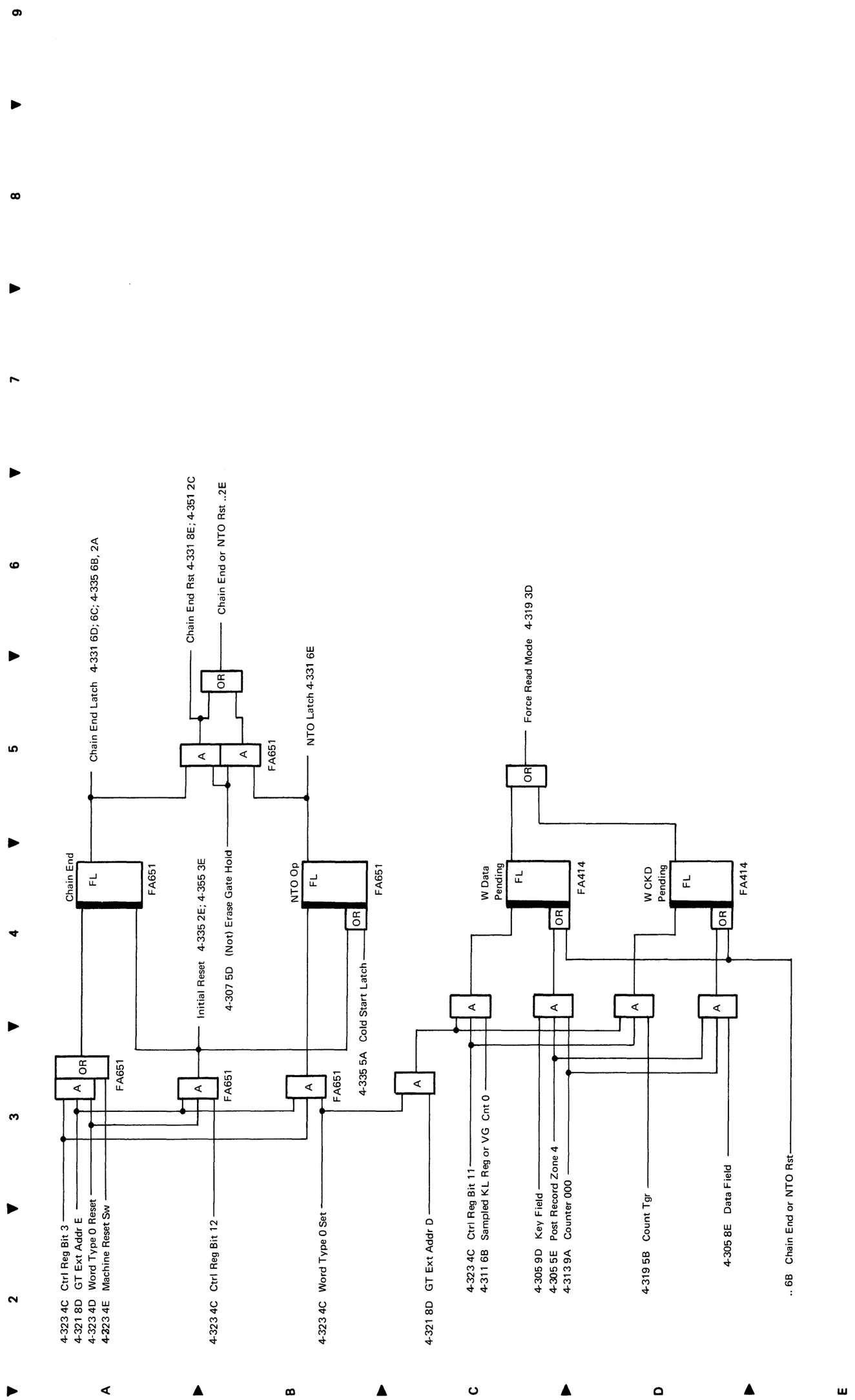
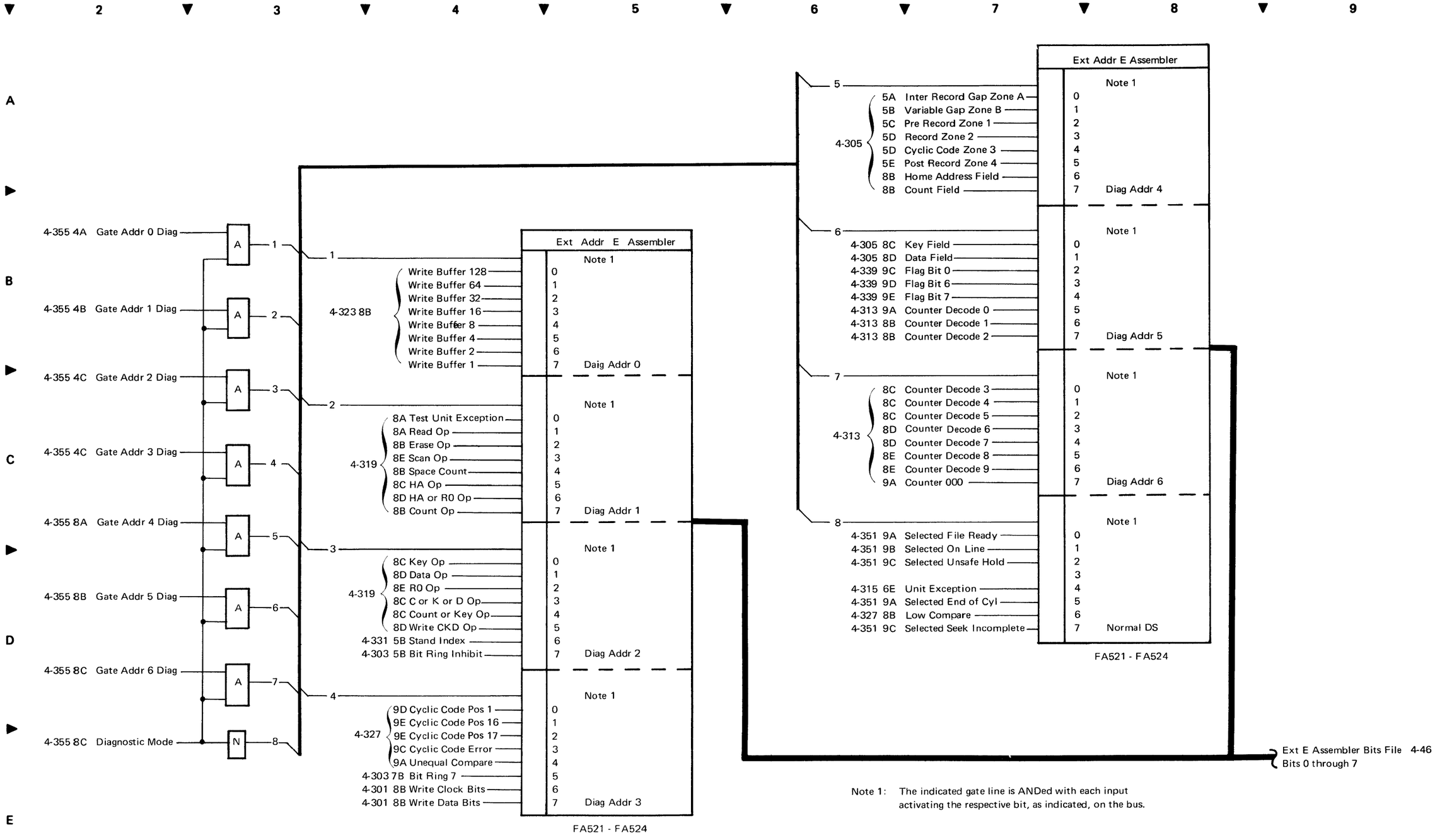
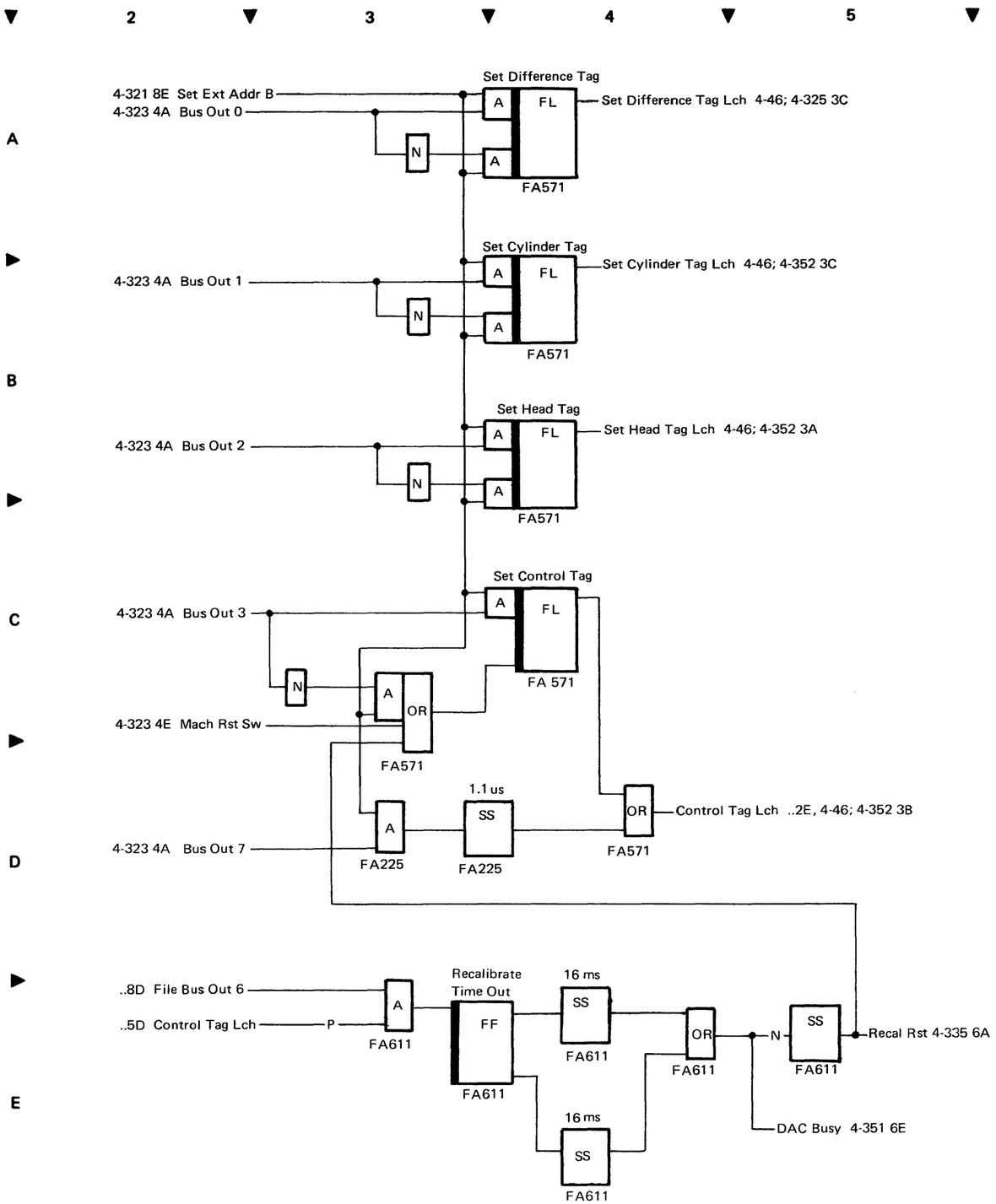


Diagram 4-341. Reset Controls

Diagram 4-345. External Decode E Assembler




2
3
4
5
A
B
C
D
E
Set Difference Tag
4-321 8E Set Ext Addr B
4-323 4A Bus Out 0
A
FL
Set Difference Tag Lch 4-46; 4-325 3C
N
A
FA571
Set Cylinder Tag
4-323 4A Bus Out 1
Set Cylinder Tag Lch 4-46; 4-352 3C
FA571
Set Head Tag
4-323 4A Bus Out 2
Set Head Tag Lch 4-46; 4-352 3A
FA571
Set Control Tag
4-323 4A Bus Out 3
FA 571
OR
4-323 4E Mach Rst Sw
FA571
1.1 us
SS
4-323 4A Bus Out 7
Control Tag Lch ..2E, 4-46; 4-352 3B
FA225
FA225
FA571
..8D File Bus Out 6
..5D Control Tag Lch
P
Recalibrate
Time Out
16 ms
FF
FA611
FA611
FA611
FA611
Recal Rst 4-335 6A
DAC Busy 4-351 6E

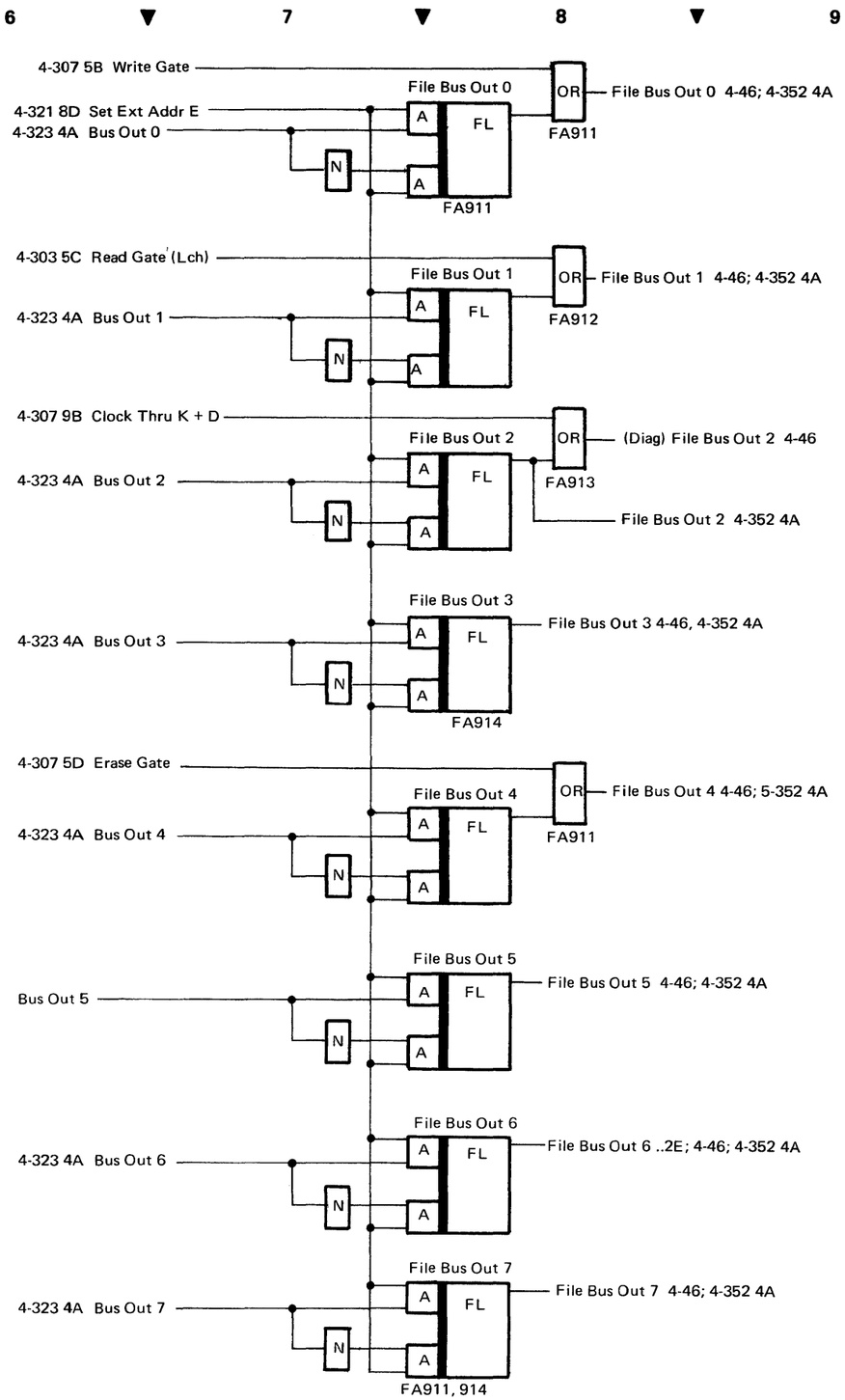
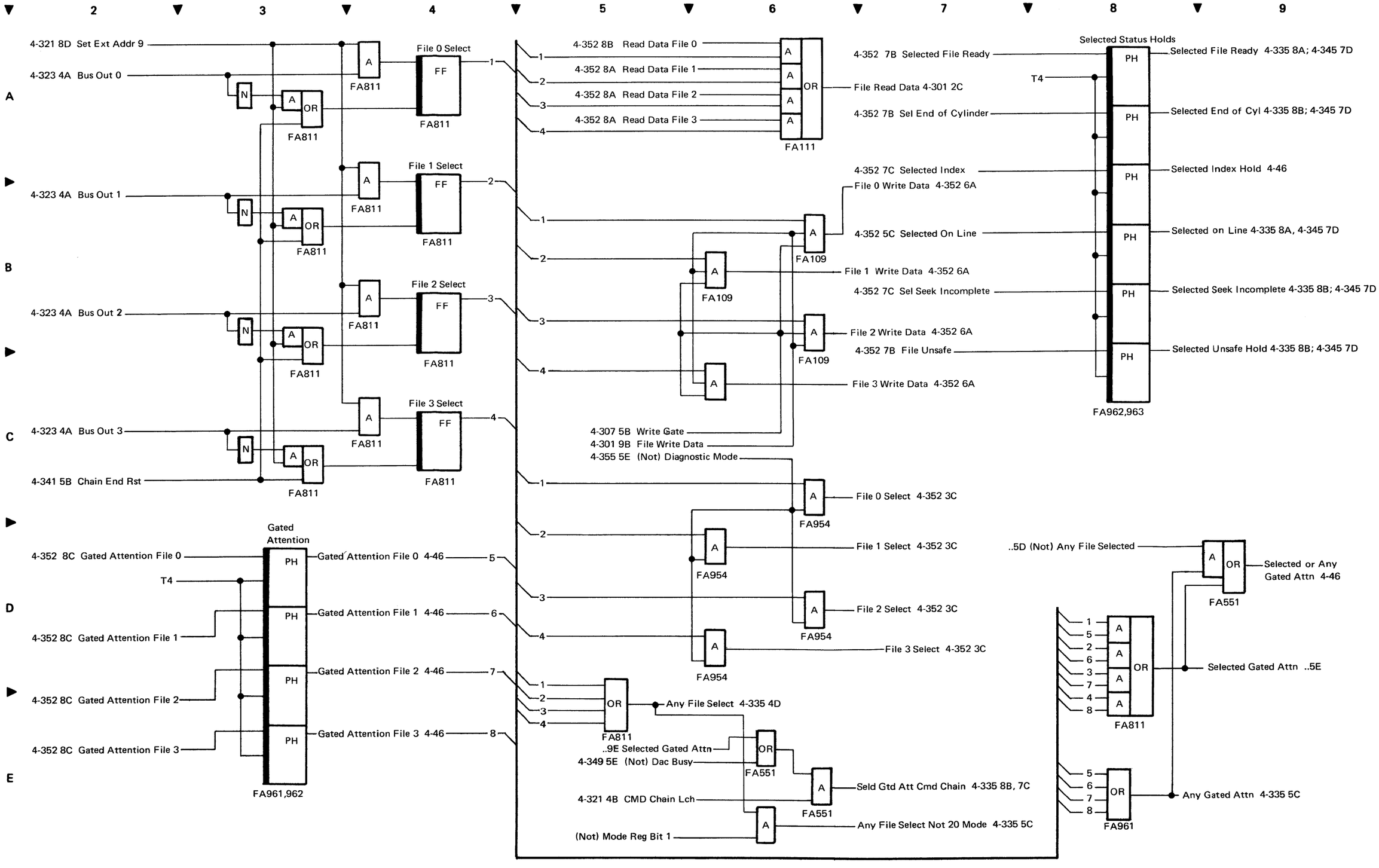
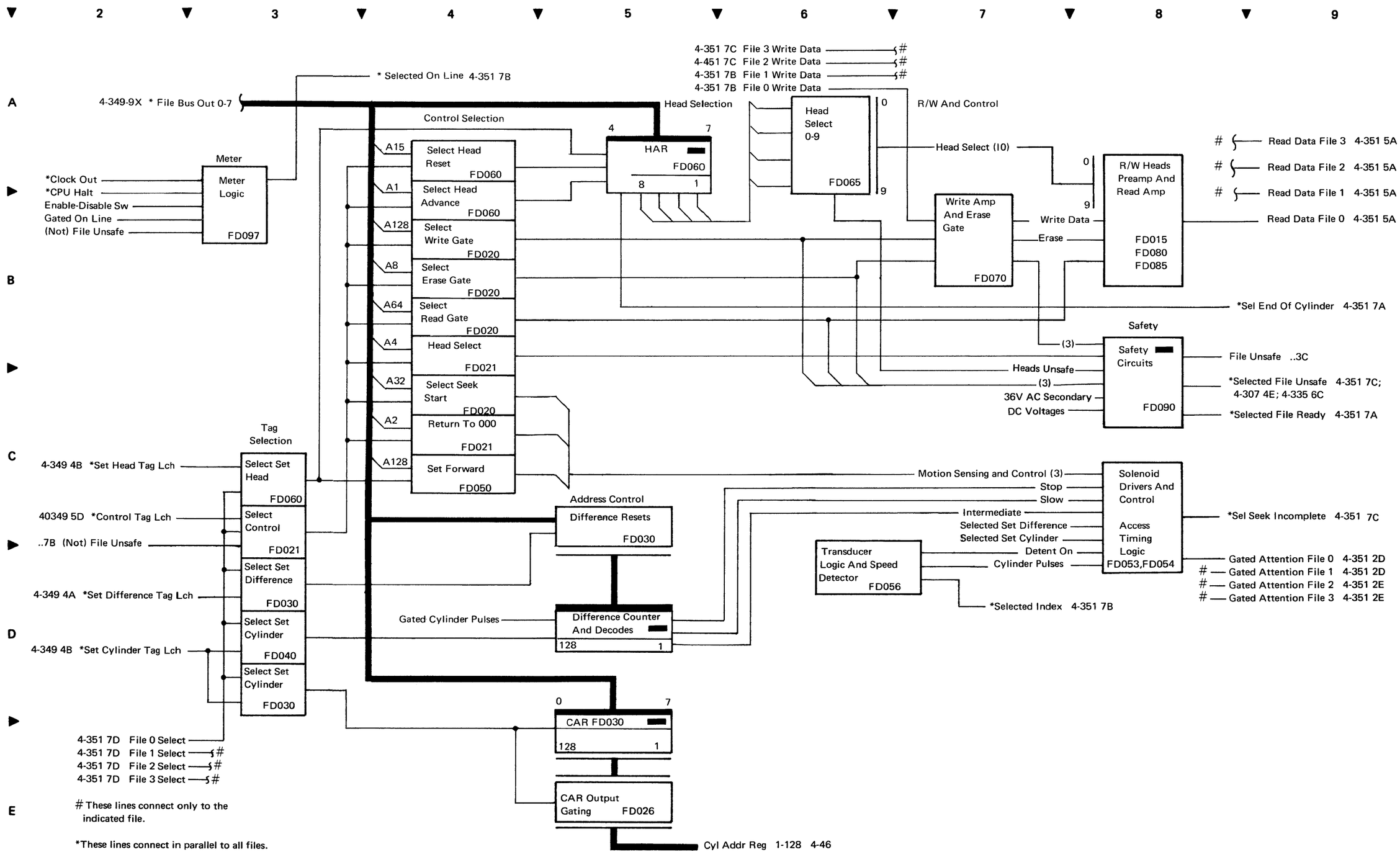
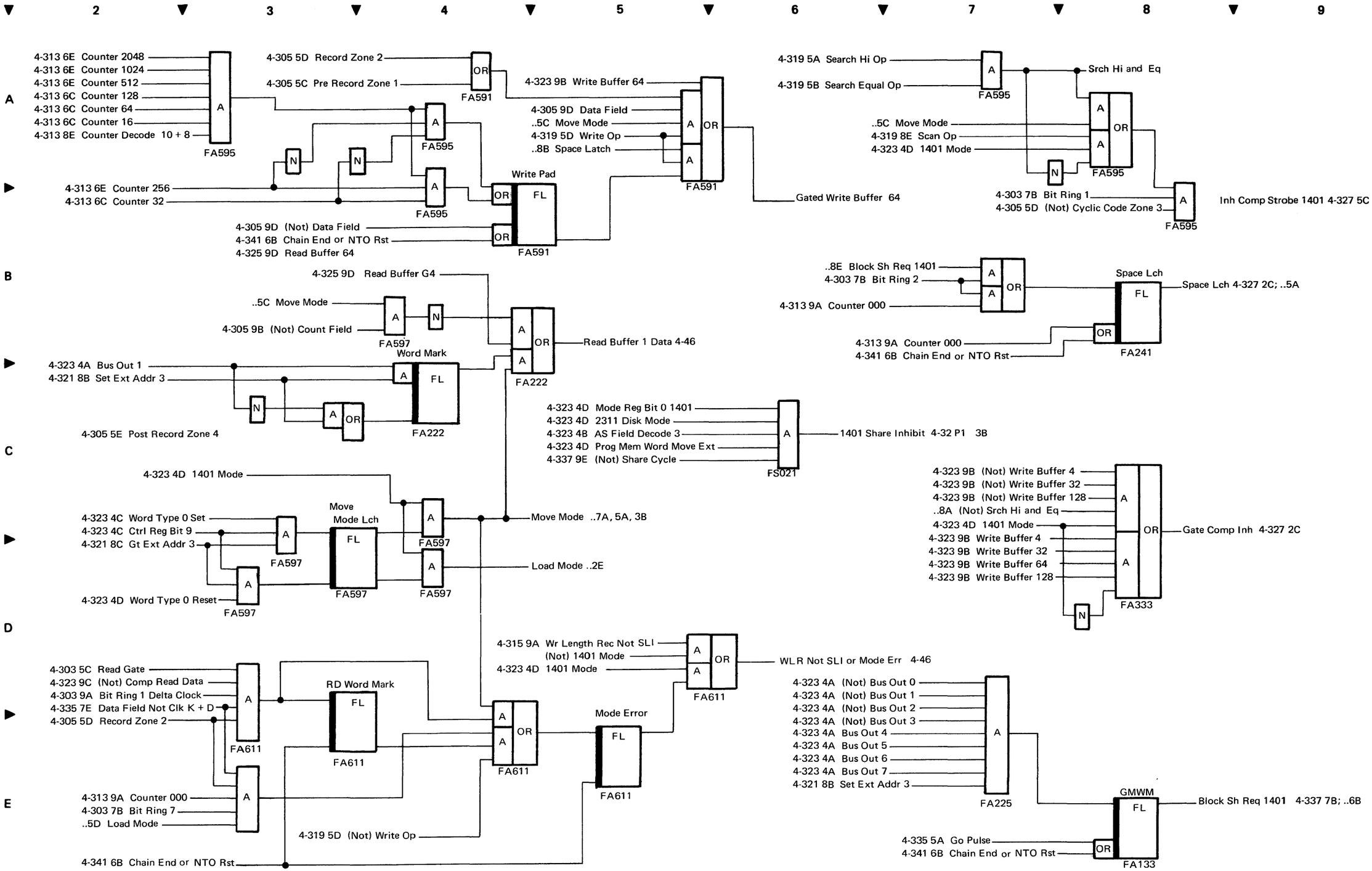

6
7
8
9
4-307 5B Write Gate
File Bus Out 0
OR
File Bus Out 0 4-46; 4-352 4A
4-321 8D Set Ext Addr E
4-323 4A Bus Out 0
FA911
FA911
4-303 5C Read Gate (Lch)
File Bus Out 1
File Bus Out 1 4-46; 4-352 4A
4-323 4A Bus Out 1
FA912
4-307 9B Clock Thru K + D
File Bus Out 2
(Diag) File Bus Out 2 4-46
4-323 4A Bus Out 2
FA913
File Bus Out 2 4-352 4A
File Bus Out 3
4-323 4A Bus Out 3
File Bus Out 3 4-46, 4-352 4A
FA914
4-307 5D Erase Gate
File Bus Out 4
File Bus Out 4 4-46; 5-352 4A
4-323 4A Bus Out 4
FA911
File Bus Out 5
Bus Out 5
File Bus Out 5 4-46; 4-352 4A
File Bus Out 6
4-323 4A Bus Out 6
File Bus Out 6 ..2E; 4-46; 4-352 4A
File Bus Out 7
4-323 4A Bus Out 7
File Bus Out 7 4-46; 4-352 4A
FA911, 914

Diagram 4-351. File Interface Status and Module Selection




2
3
4
5
6
7
8
9
A
B
C
D
E
4-351 7C File 3 Write Data
4-451 7C File 2 Write Data
4-351 7B File 1 Write Data
4-351 7B File 0 Write Data
* Selected On Line 4-351 7B
4-349-9X * File Bus Out 0-7
Head Selection
Control Selection
Meter
*Clock Out
*CPU Halt
Enable-Disable Sw
Gated On Line
(Not) File Unsafe
Meter Logic FD097
A15
Select Head Reset FD060
A1
Select Head Advance FD060
A128
Select Write Gate FD020
A8
Select Erase Gate FD020
A64
Select Read Gate FD020
A4
Head Select FD021
A32
Select Seek Start FD020
A2
Return To 000 FD021
A128
Set Forward FD050
HAR FD060
Head Select 0-9 FD065
R/W And Control
Head Select (10)
Write Amp And Erase Gate FD070
Write Data
Erase
R/W Heads Preamp And Read Amp FD015 FD080 FD085
Read Data File 3 4-351 5A
Read Data File 2 4-351 5A
Read Data File 1 4-351 5A
Read Data File 0 4-351 5A
*Sel End Of Cylinder 4-351 7A
Safety
Safety Circuits FD090
(3)
Heads Unsafe
(3)
36V AC Secondary
DC Voltages
File Unsafe ..3C
*Selected File Unsafe 4-351 7C; 4-307 4E; 4-335 6C
*Selected File Ready 4-351 7A
Tag Selection
4-349 4B *Set Head Tag Lch
40349 5D *Control Tag Lch
..7B (Not) File Unsafe
4-349 4A *Set Difference Tag Lch
4-349 4B *Set Cylinder Tag Lch
Select Set Head FD060
Select Control FD021
Select Set Difference FD030
Select Set Cylinder FD040
Select Set Cylinder FD030
4-351 7D File 0 Select
4-351 7D File 1 Select
4-351 7D File 2 Select
4-351 7D File 3 Select
Address Control
Difference Resets FD030
Gated Cylinder Pulses
Difference Counter And Decodes
CAR FD030
CAR Output Gating FD026
Cyl Addr Reg 1-128 4-46
Motion Sensing and Control (3)
Stop
Slow
Intermediate
Selected Set Difference
Selected Set Cylinder
Detent On
Cylinder Pulses
Transducer Logic And Speed Detector FD056
*Selected Index 4-351 7B
Solenoid Drivers And Control
Access Timing Logic FD053,FD054
*Sel Seek Incomplete 4-351 7C
Gated Attention File 0 4-351 2D
Gated Attention File 1 4-351 2D
Gated Attention File 2 4-351 2E
Gated Attention File 3 4-351 2E
These lines connect only to the indicated file.
*These lines connect in parallel to all files.


2
3
4
5
6
7
8
9
A
B
C
D
E
4-313 6E Counter 2048
4-313 6E Counter 1024
4-313 6E Counter 512
4-313 6C Counter 128
4-313 6C Counter 64
4-313 6C Counter 16
4-313 8E Counter Decode 10 + 8
FA595
4-305 5D Record Zone 2
4-305 5C Pre Record Zone 1
FA591
4-323 9B Write Buffer 64
4-305 9D Data Field
..5C Move Mode
4-319 5D Write Op
..8B Space Latch
FA591
4-319 5A Search Hi Op
4-319 5B Search Equal Op
FA595
Srch Hi and Eq
..5C Move Mode
4-319 8E Scan Op
4-323 4D 1401 Mode
FA595
4-313 6E Counter 256
4-313 6C Counter 32
FA595
Write Pad
FA591
Gated Write Buffer 64
4-303 7B Bit Ring 1
4-305 5D (Not) Cyclic Code Zone 3
FA595
Inh Comp Strobe 1401 4-327 5C
4-305 9D (Not) Data Field
4-341 6B Chain End or NTO Rst
4-325 9D Read Buffer 64
..8E Block Sh Req 1401
4-303 7B Bit Ring 2
4-313 9A Counter 000
Space Lch
FA241
Space Lch 4-327 2C; ..5A
4-313 9A Counter 000
4-341 6B Chain End or NTO Rst
4-325 9D Read Buffer G4
..5C Move Mode
4-305 9B (Not) Count Field
FA597
Word Mark
FA222
Read Buffer 1 Data 4-46
4-323 4A Bus Out 1
4-321 8B Set Ext Addr 3
4-305 5E Post Record Zone 4
FA222
4-323 4D Mode Reg Bit 0 1401
4-323 4D 2311 Disk Mode
4-323 4B AS Field Decode 3
4-323 4D Prog Mem Word Move Ext
4-337 9E (Not) Share Cycle
FS021
1401 Share Inhibit 4-32 P1 3B
4-323 4D 1401 Mode
4-323 4C Word Type 0 Set
4-323 4C Ctrl Reg Bit 9
4-321 8C Gt Ext Addr 3
FA597
Move
Mode Lch
FA597
Move Mode ..7A, 5A, 3B
Load Mode ..2E
4-323 4D Word Type 0 Reset
FA597
FA597
4-323 9B (Not) Write Buffer 4
4-323 9B (Not) Write Buffer 32
4-323 9B (Not) Write Buffer 128
..8A (Not) Srch Hi and Eq
4-323 4D 1401 Mode
4-323 9B Write Buffer 4
4-323 9B Write Buffer 32
4-323 9B Write Buffer 64
4-323 9B Write Buffer 128
FA333
Gate Comp Inh 4-327 2C
4-315 9A Wr Length Rec Not SLI
(Not) 1401 Mode
4-323 4D 1401 Mode
FA611
WLR Not SLI or Mode Err 4-46
4-303 5C Read Gate
4-323 9C (Not) Comp Read Data
4-303 9A Bit Ring 1 Delta Clock
4-335 7E Data Field Not Clk K + D
4-305 5D Record Zone 2
FA611
RD Word Mark
FA611
FA611
Mode Error
FA611
4-323 4A (Not) Bus Out 0
4-323 4A (Not) Bus Out 1
4-323 4A (Not) Bus Out 2
4-323 4A (Not) Bus Out 3
4-323 4A Bus Out 4
4-323 4A Bus Out 5
4-323 4A Bus Out 6
4-323 4A Bus Out 7
4-321 8B Set Ext Addr 3
FA225
GMWM
FA133
Block Sh Req 1401 4-337 7B; ..6B
4-335 5A Go Pulse
4-341 6B Chain End or NTO Rst
4-313 9A Counter 000
4-303 7B Bit Ring 7
..5D Load Mode
4-319 5D (Not) Write Op
4-341 6B Chain End or NTO Rst

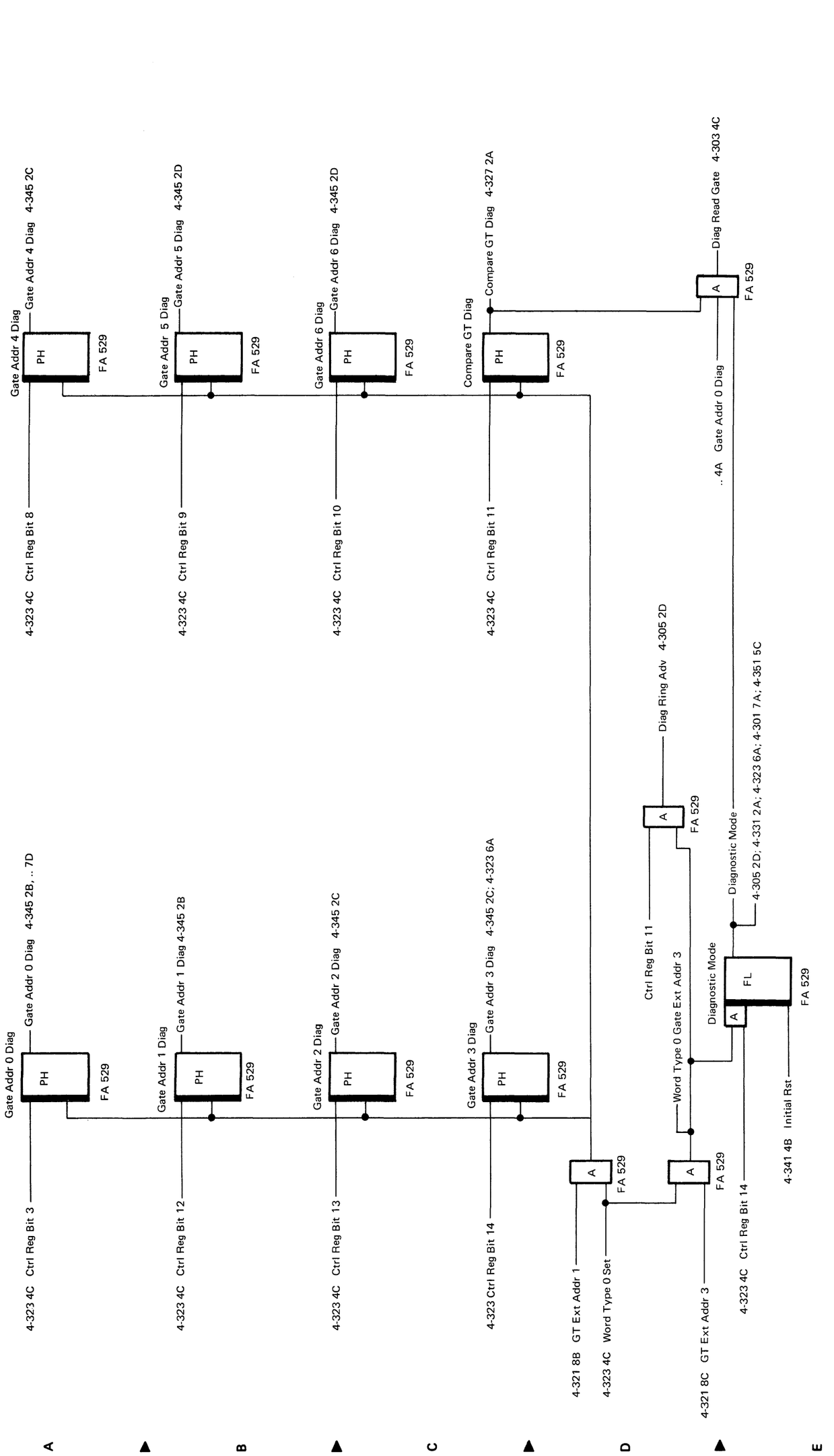


Diagram 4-355. Diagnostic Controls

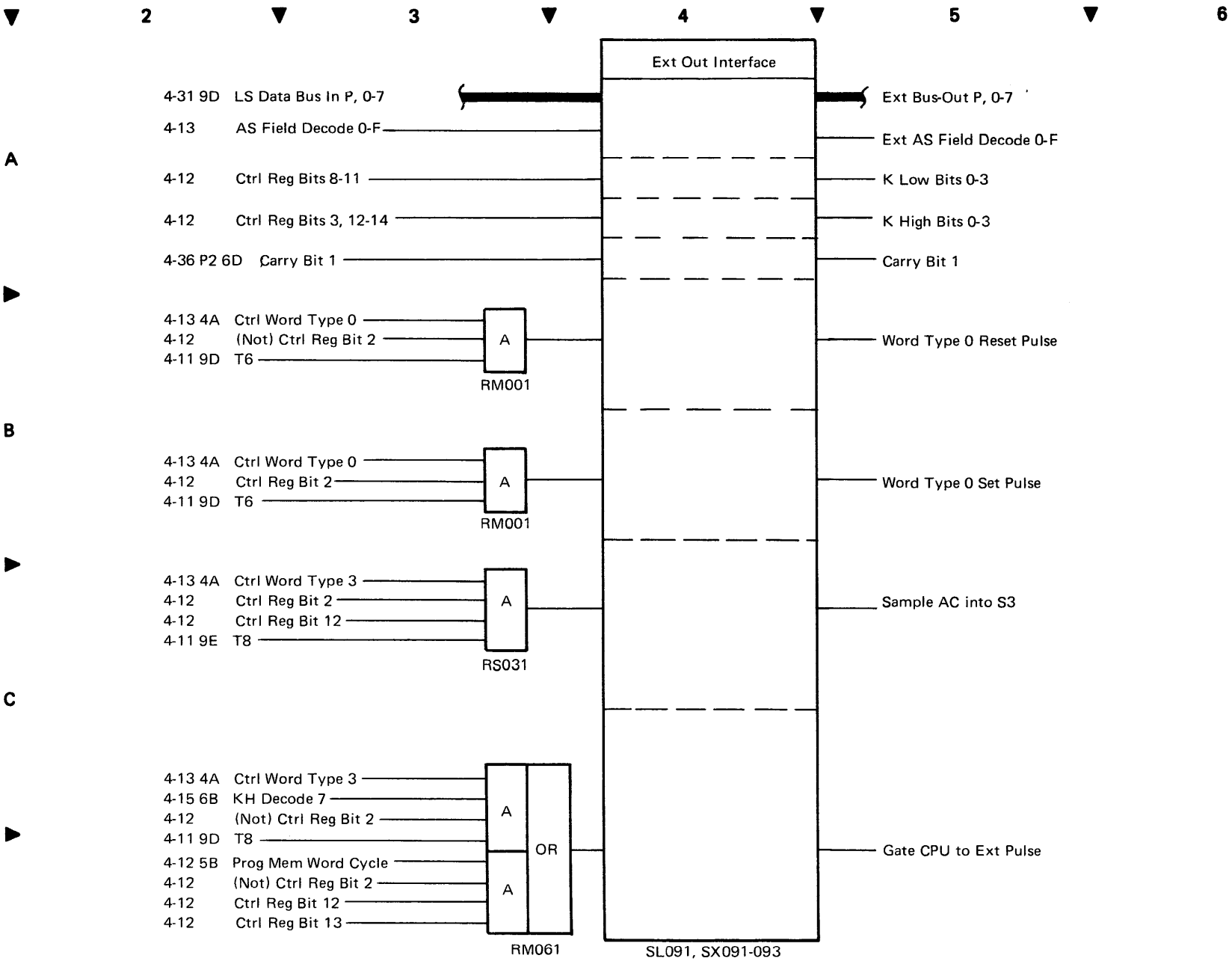


Diagram 4-400. External Out Interface Channel

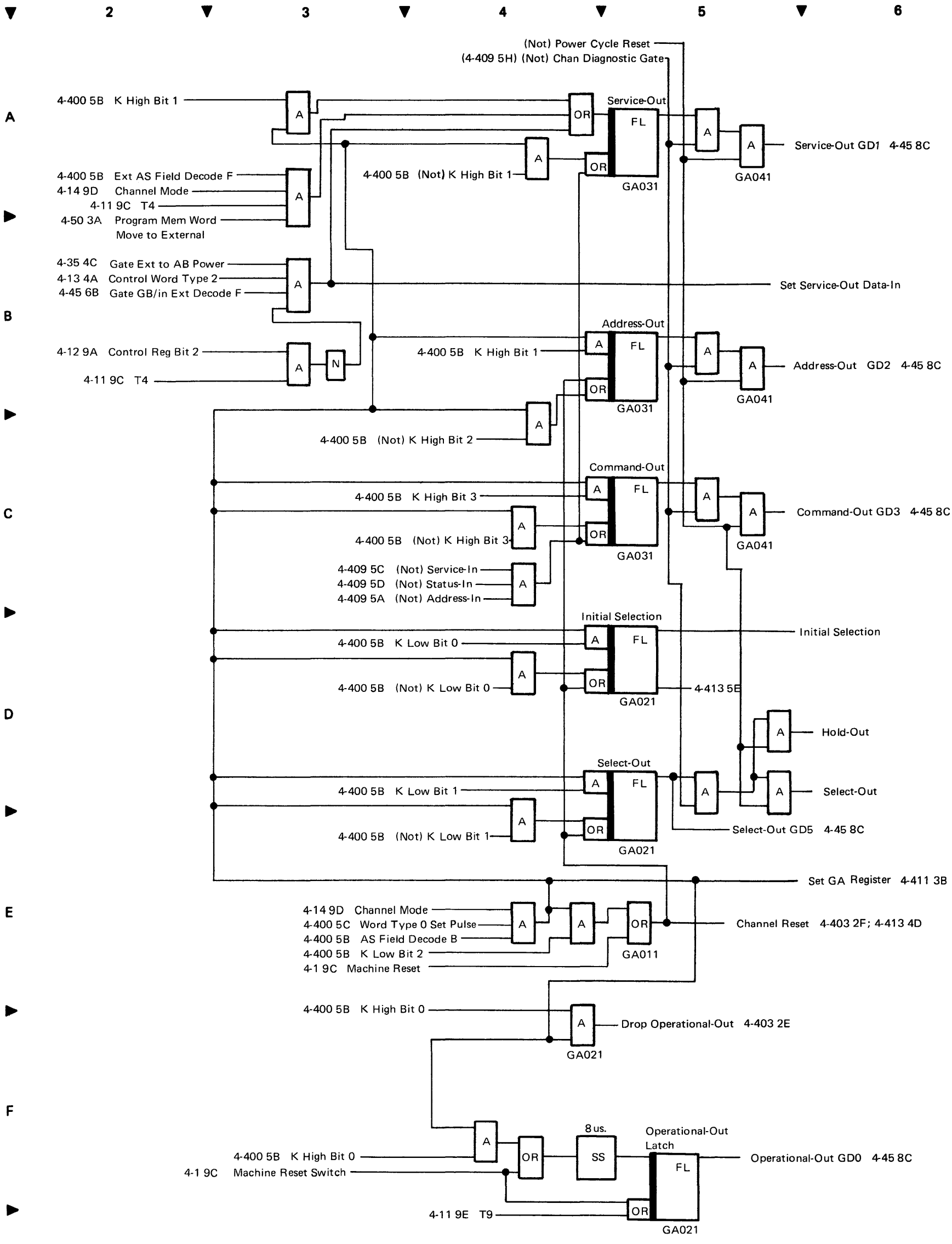


Diagram 4-401. Circuits Controlled by the Set/Reset GA Control Word

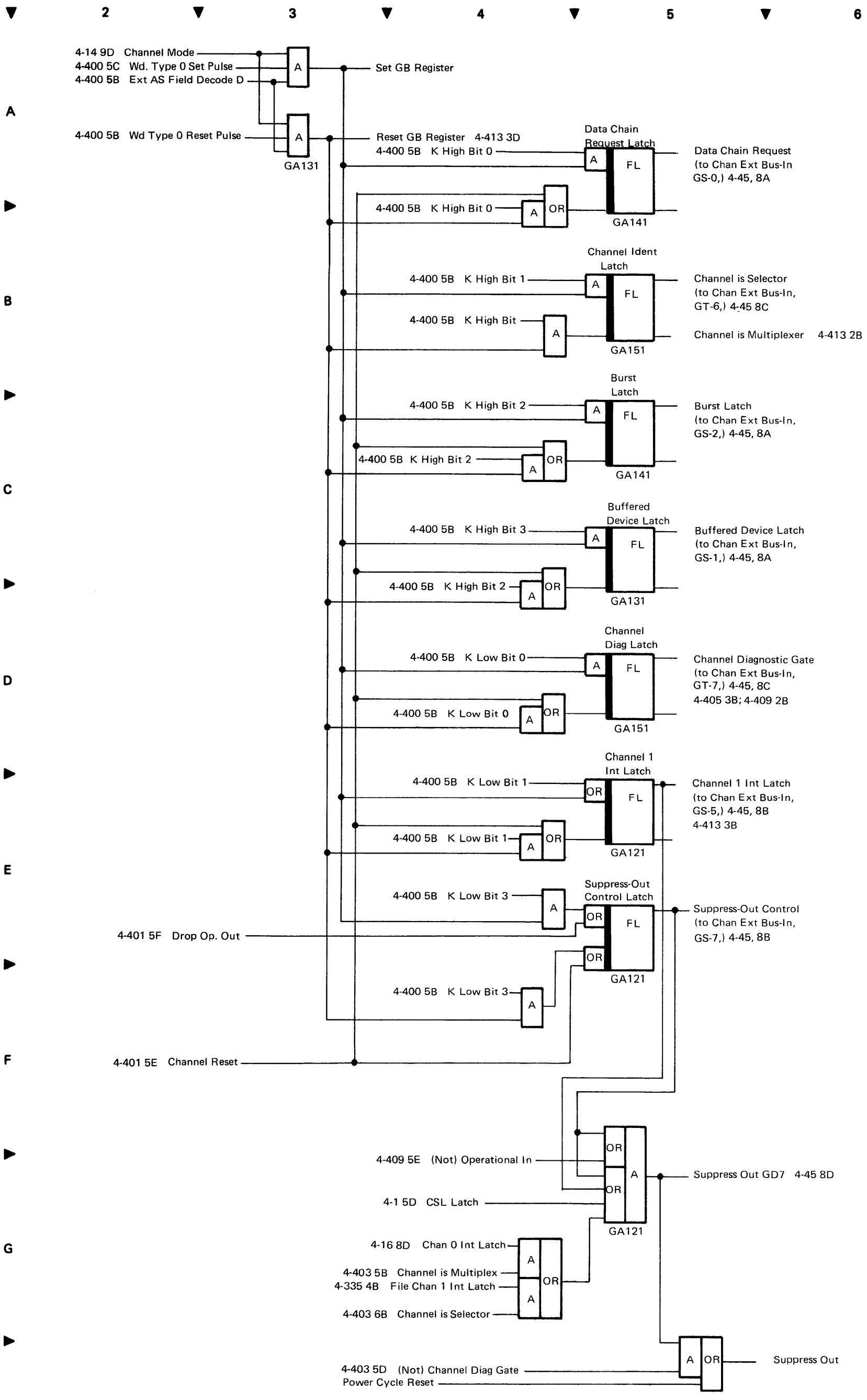


Diagram 4-403. Circuits Controlled by the Set/Reset GB Control Word

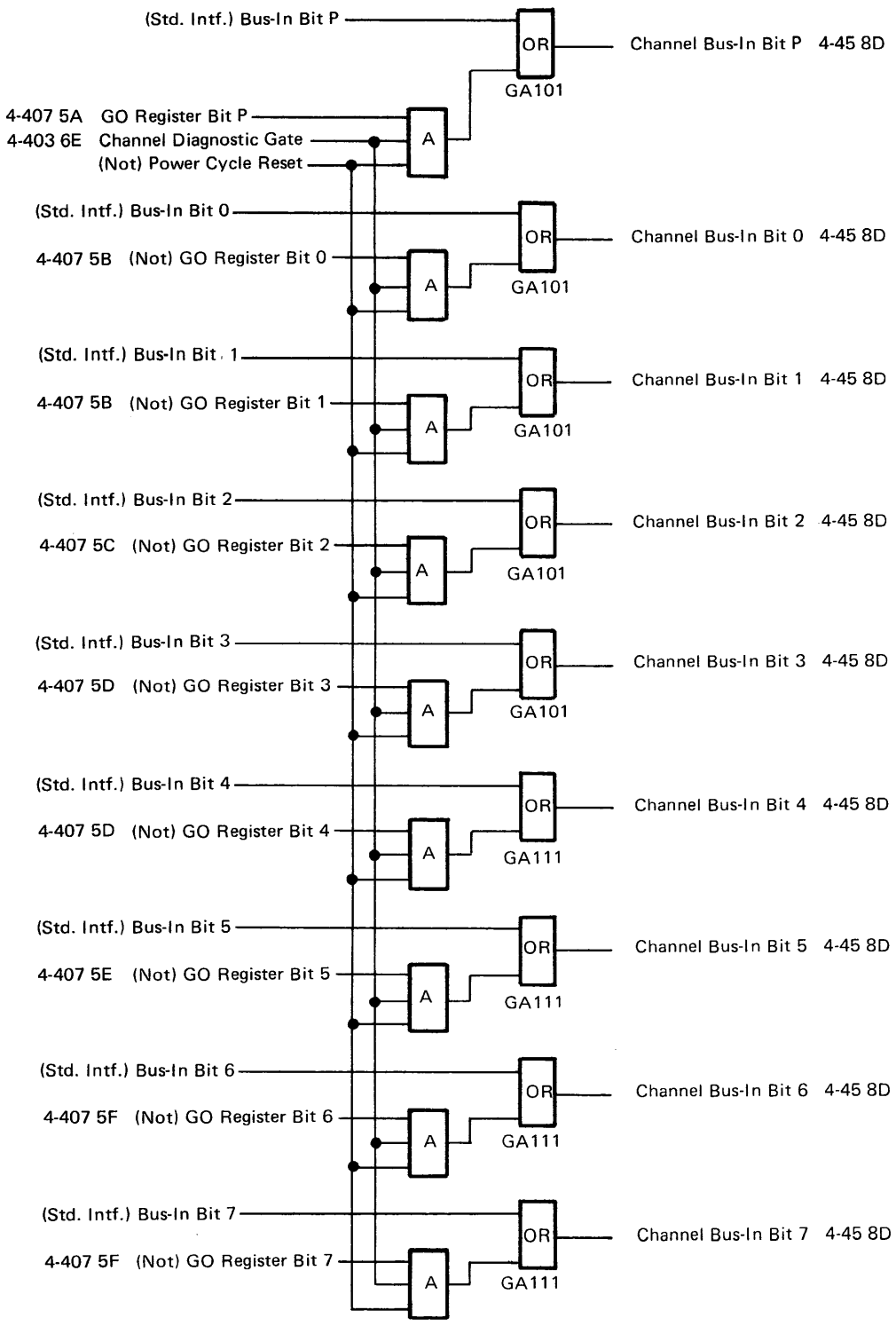


Diagram 4-405. Logic Diagram of the Bus/In Register (GI)

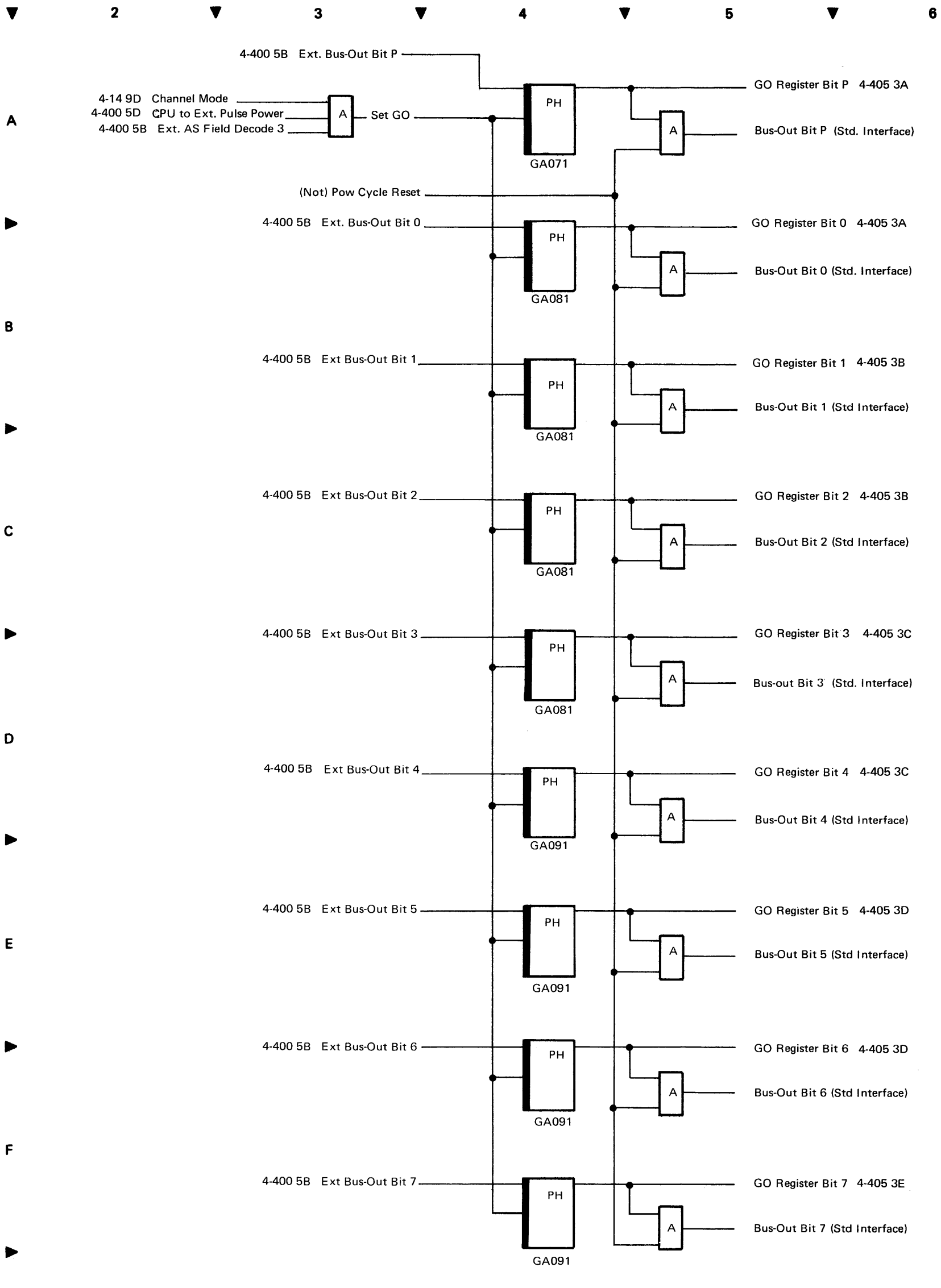


Diagram 4-407. Logic Diagram of the Bus/Out (GO) Register External Facility

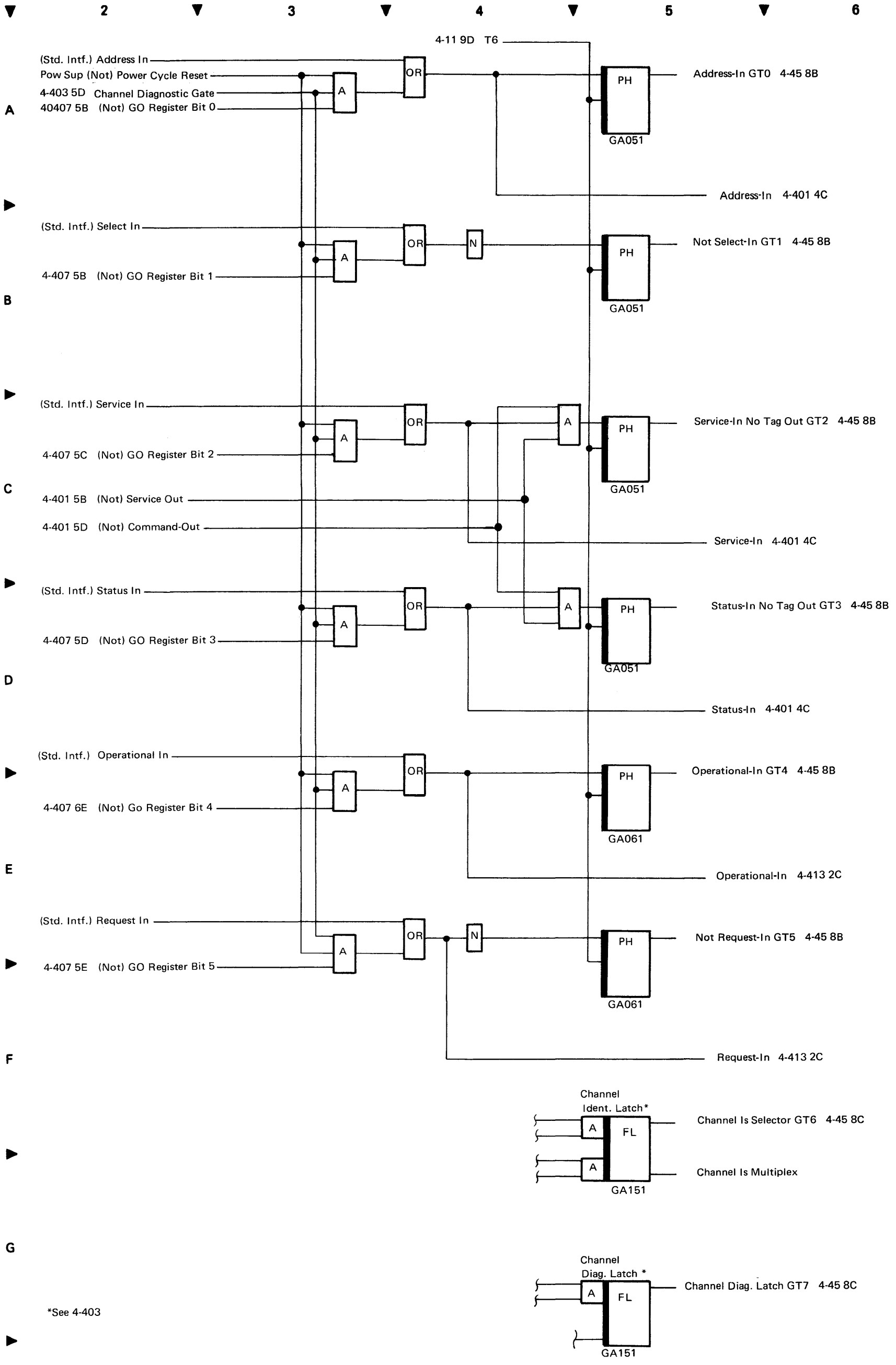


Diagram 4-409. Logic Diagram of the GT External Facility

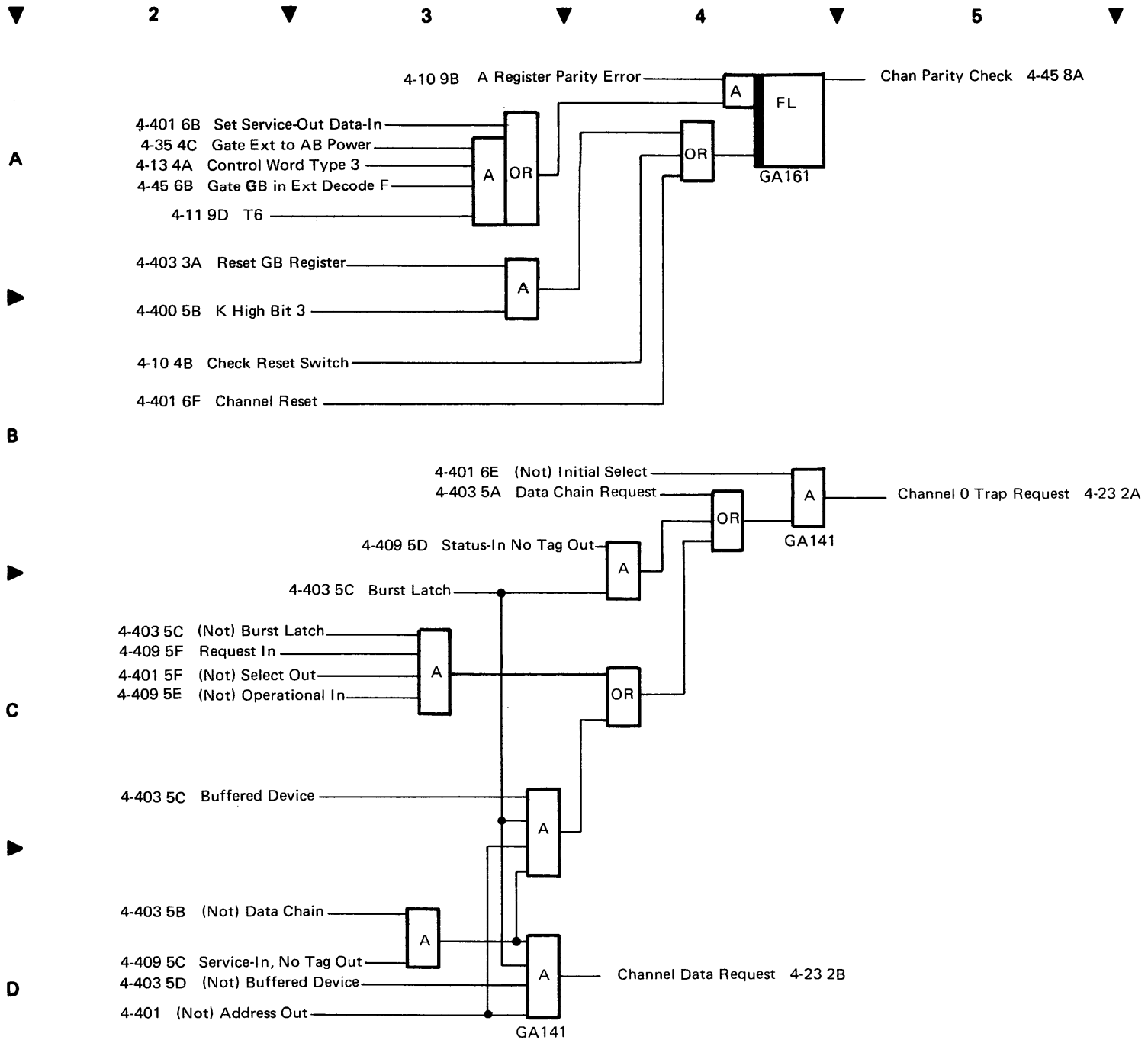
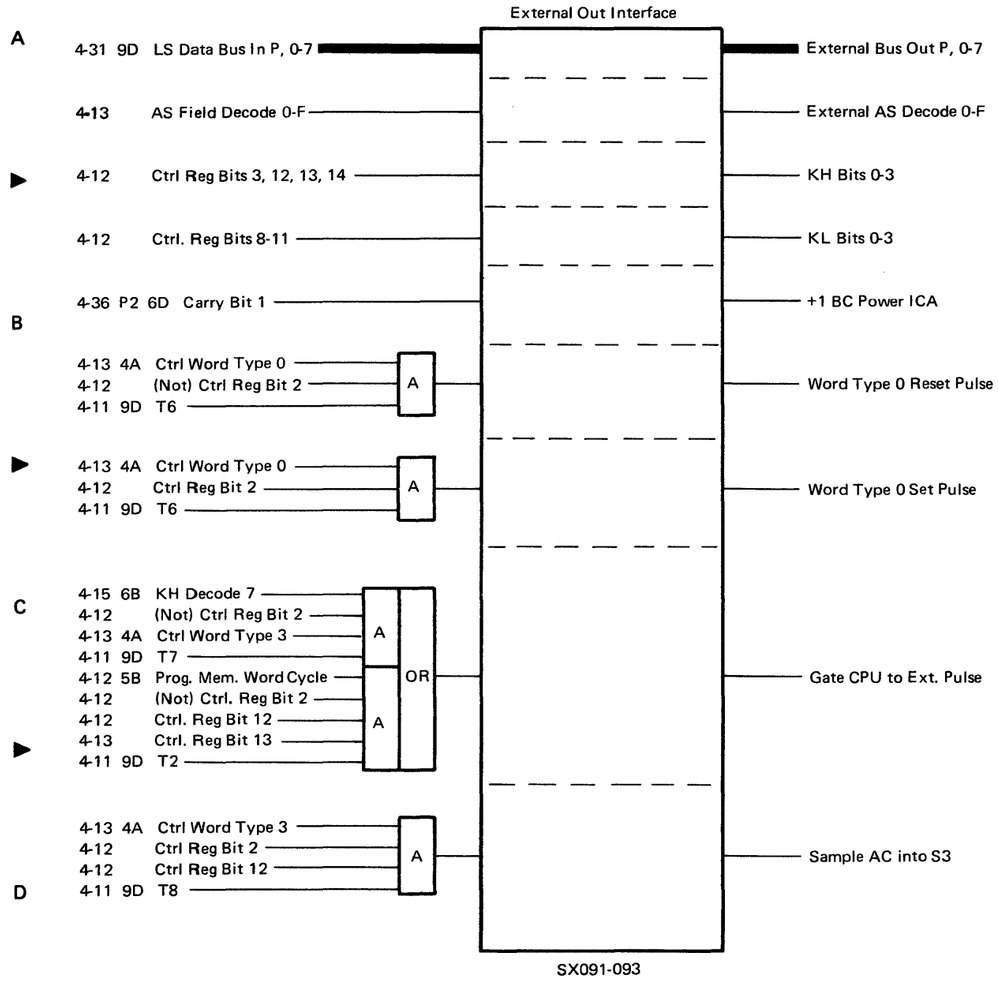


Diagram 4-413. Development of Channel Parity Check, Trap Request, and Channel Data Request Signals



	ALD Location	MDM Location
Common Controls	HA004-HA142	4-500 to 4-525
Start/Stop LA0	HA201-HA209	4-527 to 4-535
Start/Stop LA1	HA211-HA219	
Start/Stop LA2	HA221-HA229	
Start/Stop LA3	HA231-HA239	
Start/Stop LA4	HA241-HA249	
Start/Stop LA5	HA251-HA259	
Telegraph LA0	HA401-HA409	
Telegraph LA1	HA411-HA419	
Telegraph LA2	HA421-HA429	
Telegraph LA3	HA431-HA439	
Telegraph LA4	HA441-HA449	
Telegraph LA5	HA451-HA459	
Synchronous LA	HA813-HA893	4-537 to 4-559
ACU 0	HA905-HA916	4-583 to 4-585
ACU 1	HA921-HA926	
Sync Int. Clock 1	HA971-HA978	4-587 to 4-591
Sync Int. Clock 2	HA981-HA988	

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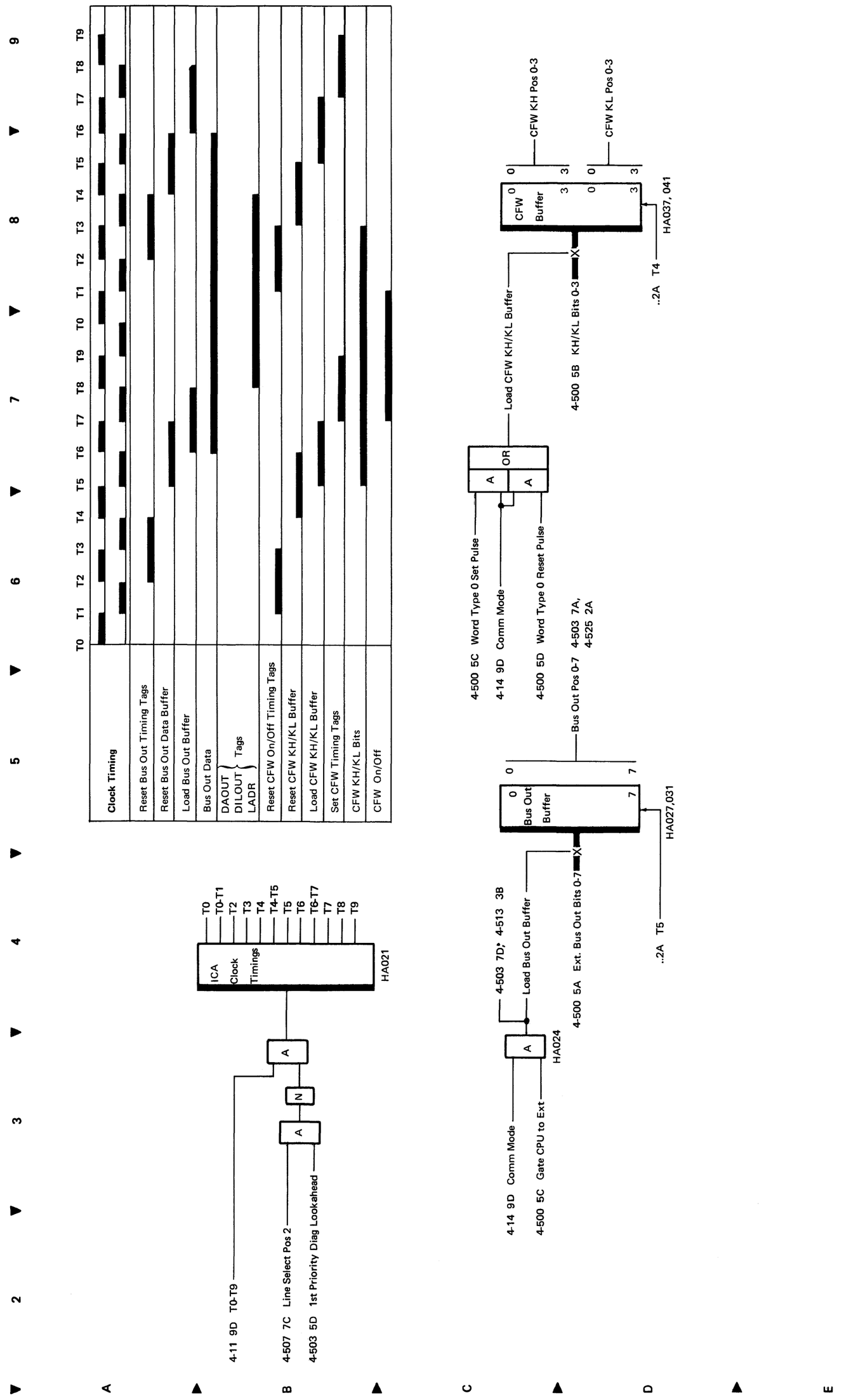
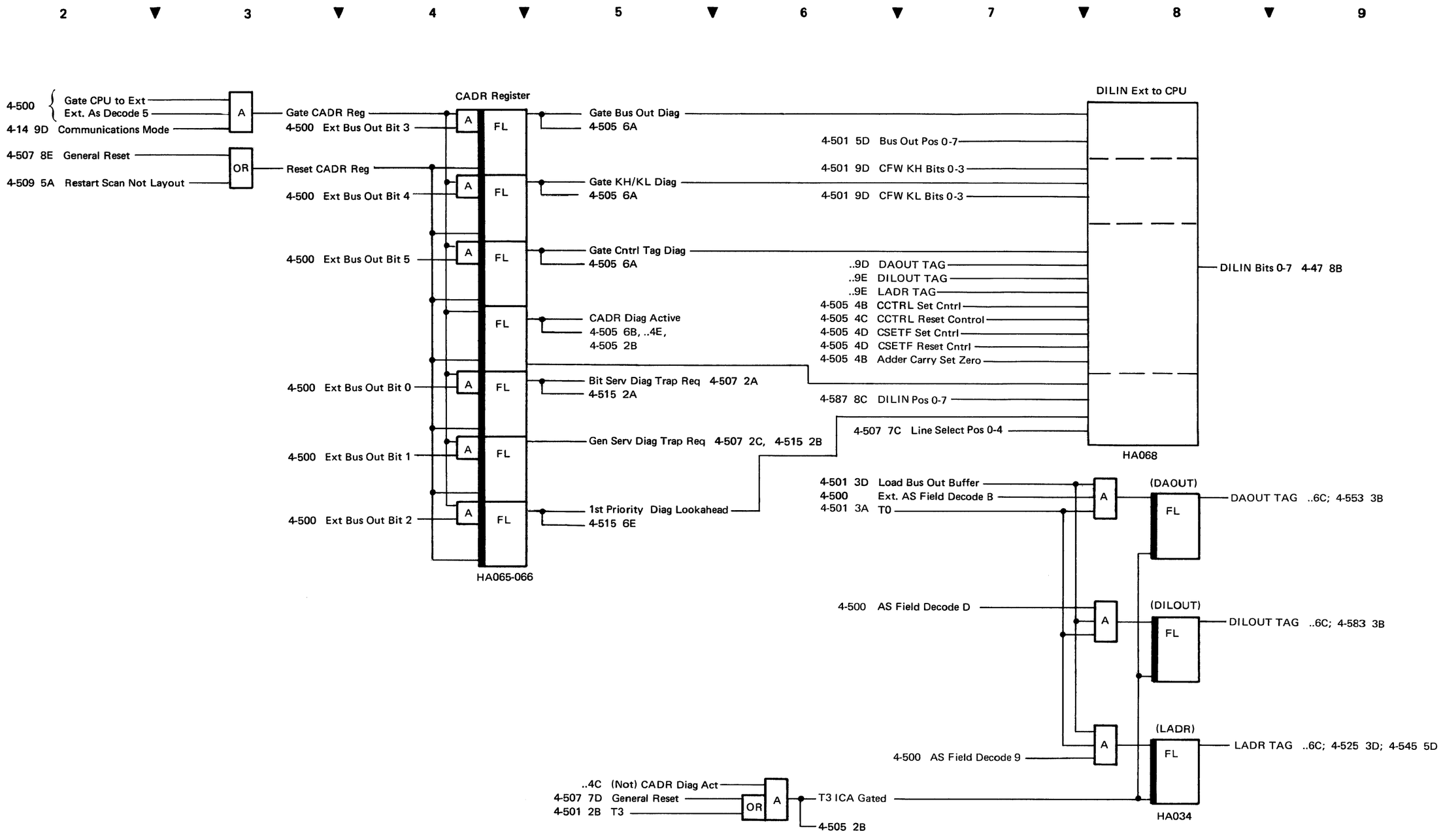


● Diagram 4-501. Clock Timings, Bus Out Buffer and CFW Buffer



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● Diagram 4-505. Adder Carry, Set/Reset Word Control Tags, and LACON 2

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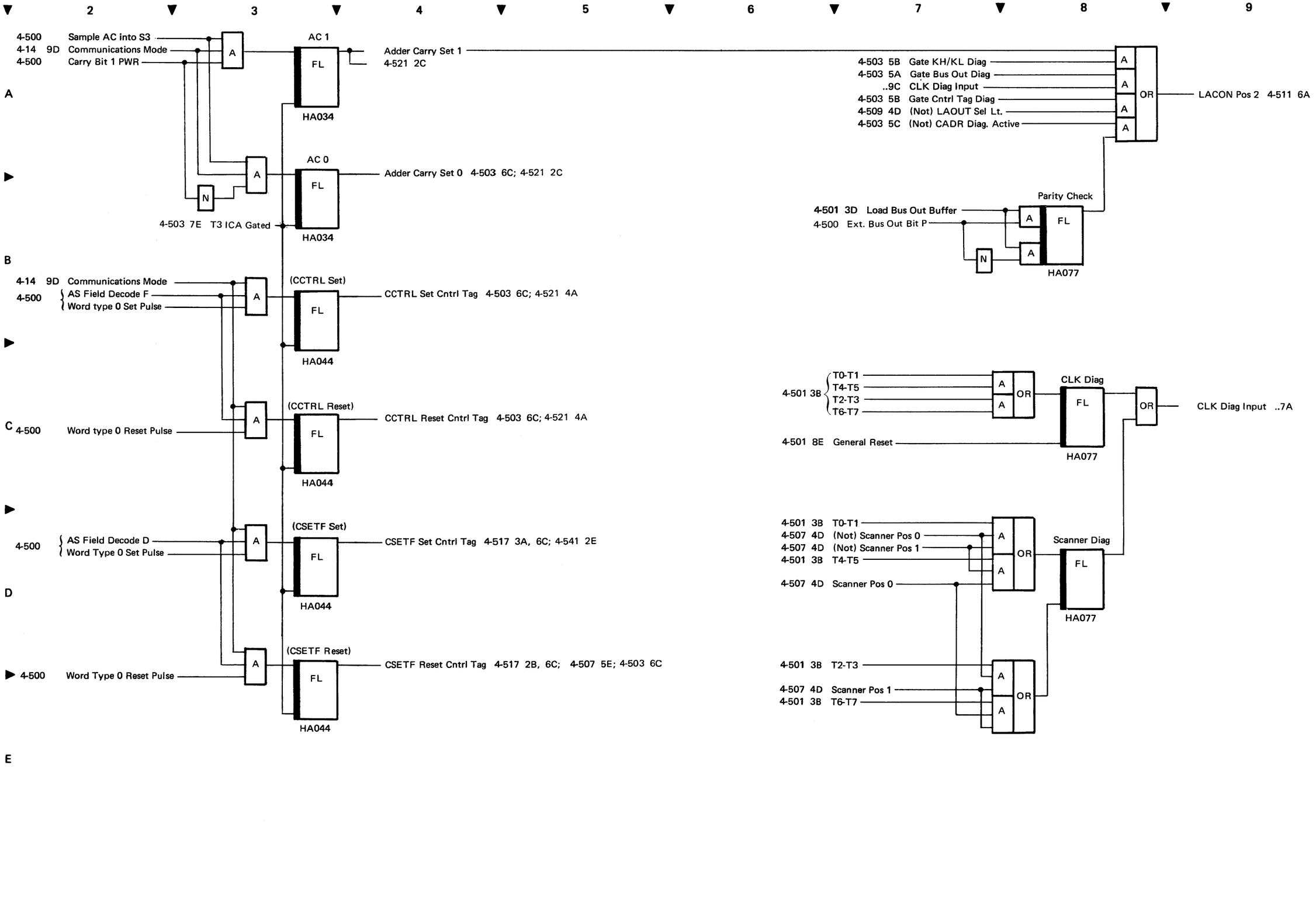

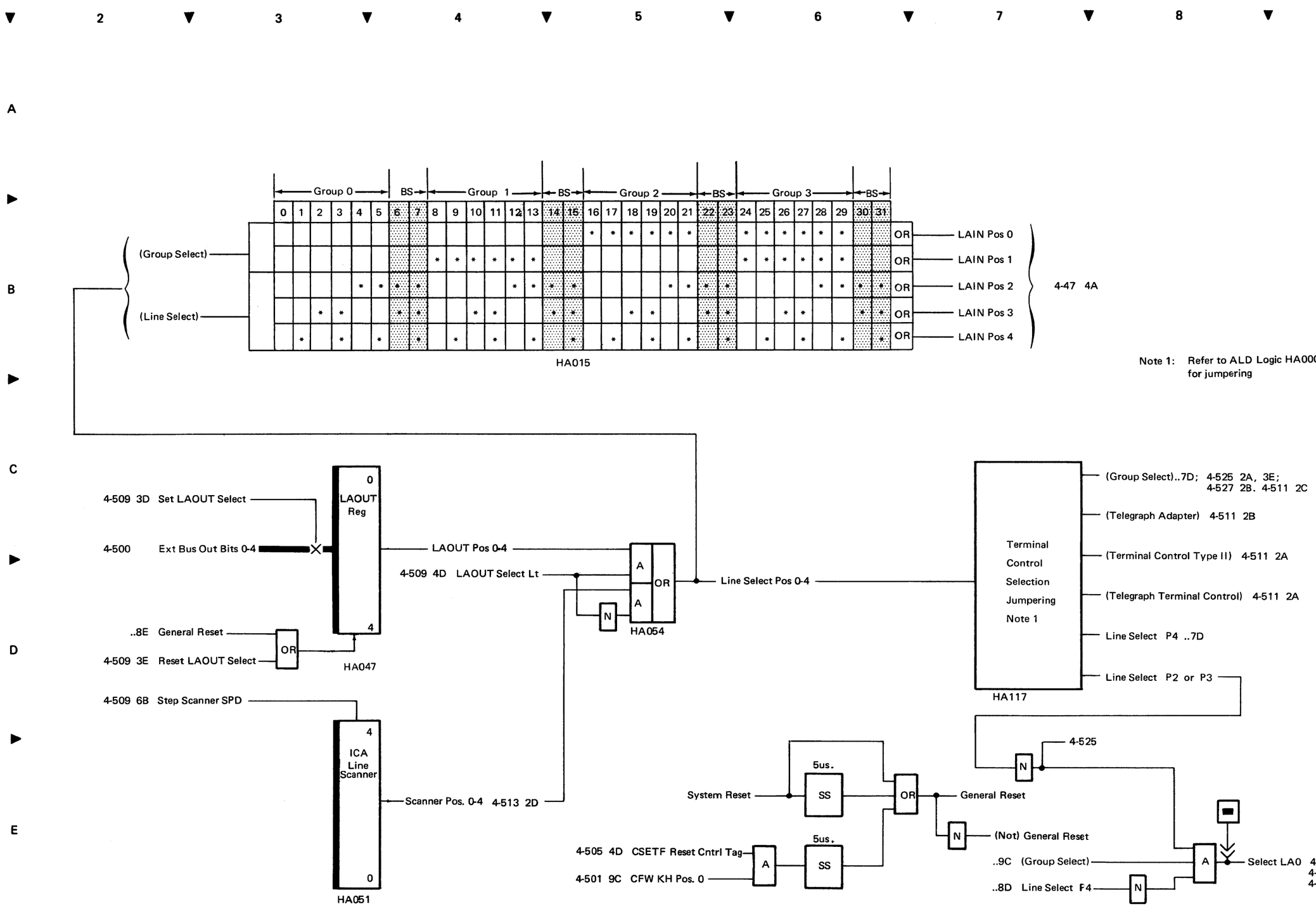

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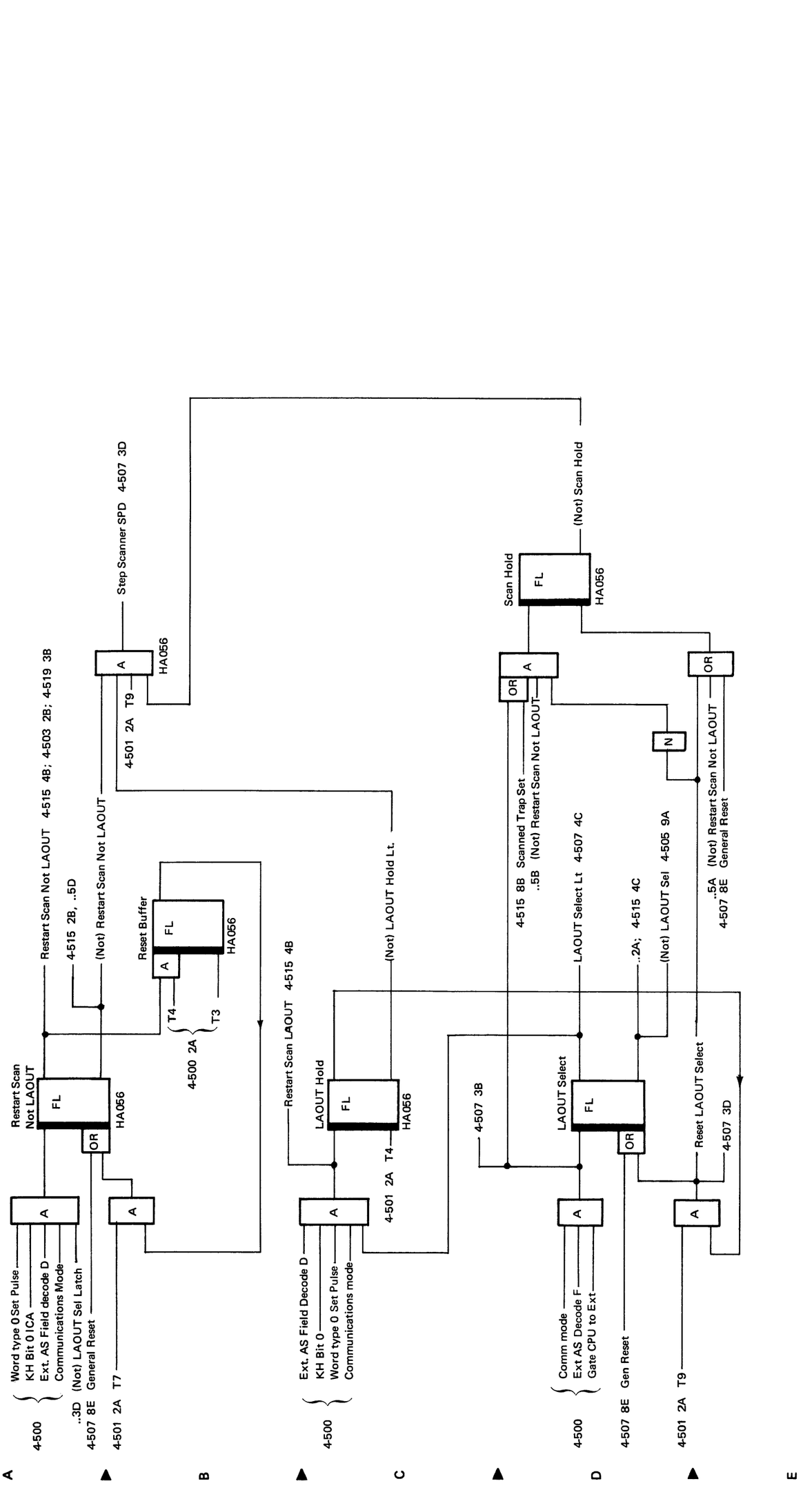
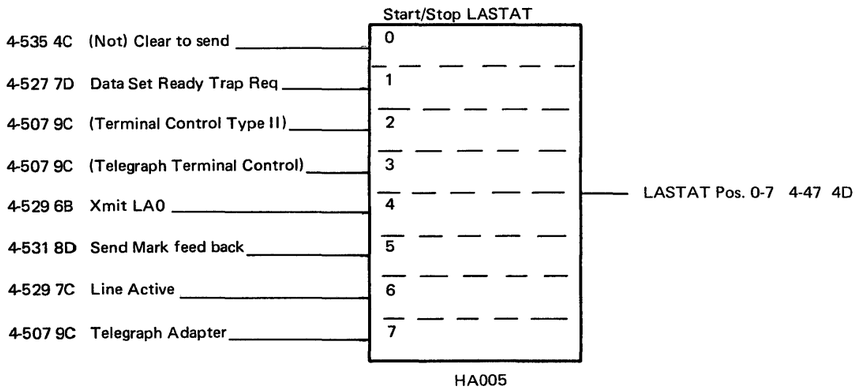
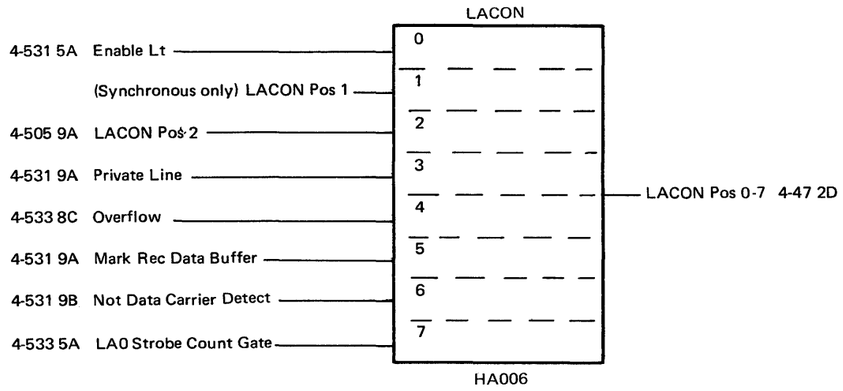
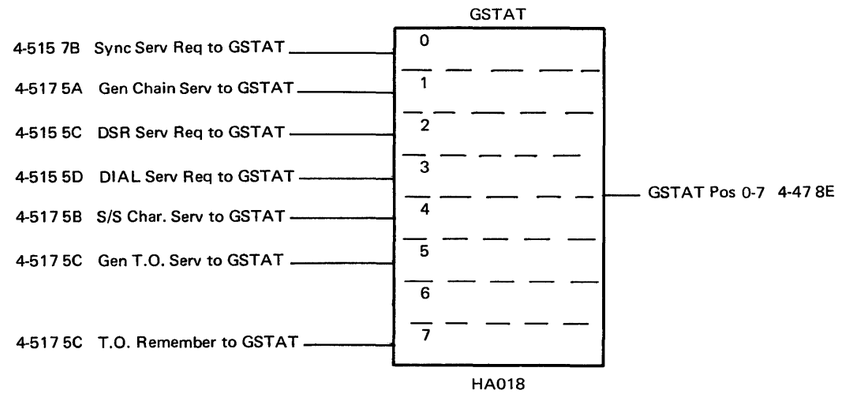
FES Y24-0506



● Diagram 4-509. Line Scanner Controls







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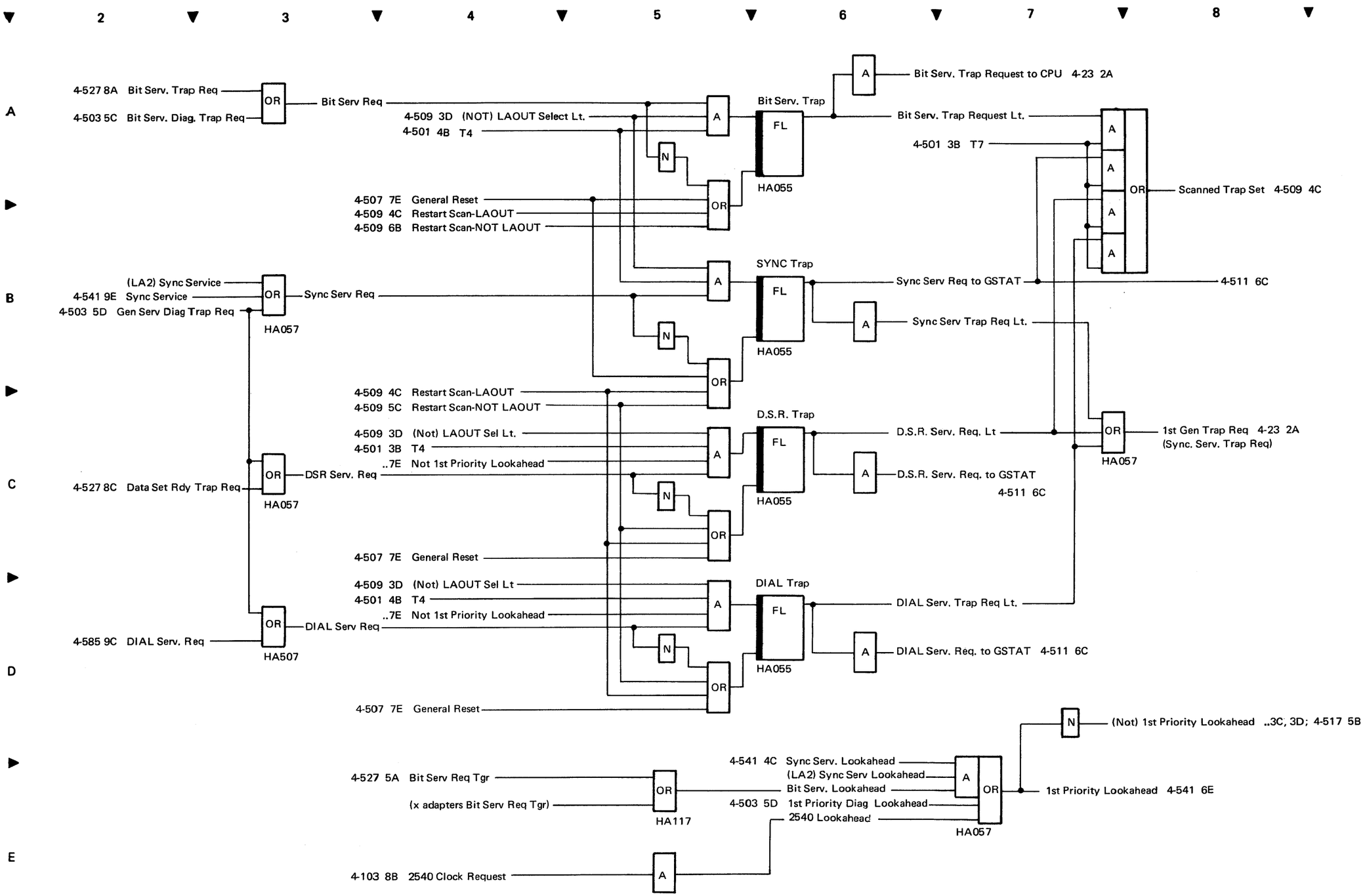
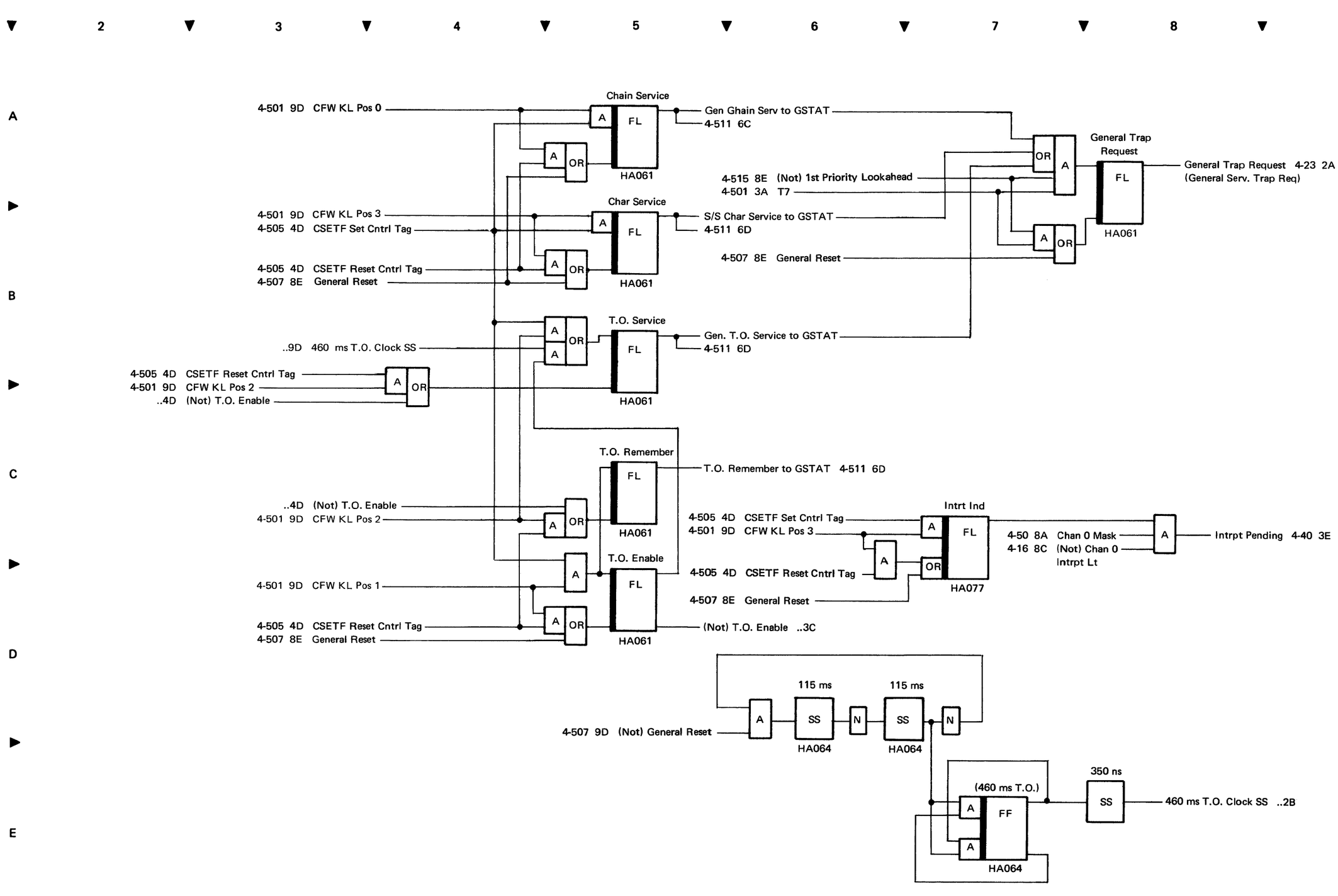

2
3
4
5
6
7
8
9
A
B
C
D
E
4-527 8A Bit Serv. Trap Req
4-503 5C Bit Serv. Diag. Trap Req
OR
Bit Serv Req
4-509 3D (NOT) LAOUT Select Lt.
4-501 4B T4
N
A
OR
Bit Serv. Trap
FL
HA055
A
Bit Serv. Trap Request to CPU 4-23 2A
Bit Serv. Trap Request Lt.
4-501 3B T7
A
A
A
A
OR
Scanned Trap Set 4-509 4C
4-507 7E General Reset
4-509 4C Restart Scan-LAOUT
4-509 6B Restart Scan-NOT LAOUT
(LA2) Sync Service
4-541 9E Sync Service
4-503 5D Gen Serv Diag Trap Req
OR
Sync Serv Req
HA057
SYNC Trap
Sync Serv Req to GSTAT
4-511 6C
Sync Serv Trap Req Lt.
4-509 4C Restart Scan-LAOUT
4-509 5C Restart Scan-NOT LAOUT
D.S.R. Trap
D.S.R. Serv. Req. Lt
4-509 3D (Not) LAOUT Sel Lt.
4-501 3B T4
..7E Not 1st Priority Lookahead
OR
1st Gen Trap Req 4-23 2A
(Sync. Serv. Trap Req)
4-527 8C Data Set Rdy Trap Req
DSR Serv. Req
D.S.R. Serv. Req. to GSTAT
4-511 6C
4-507 7E General Reset
4-509 3D (Not) LAOUT Sel Lt
4-501 4B T4
..7E Not 1st Priority Lookahead
DIAL Trap
DIAL Serv. Trap Req Lt.
4-585 9C DIAL Serv. Req
DIAL Serv Req
DIAL Serv. Req. to GSTAT 4-511 6C
4-507 7E General Reset
(Not) 1st Priority Lookahead ..3C, 3D; 4-517 5B
4-541 4C Sync Serv. Lookahead
(LA2) Sync Serv Lookahead
Bit Serv. Lookahead
4-503 5D 1st Priority Diag Lookahead
2540 Lookahead
1st Priority Lookahead 4-541 6E
4-527 5A Bit Serv Req Tgr
(x adapters Bit Serv Req Tgr)
HA117
4-103 8B 2540 Clock Request



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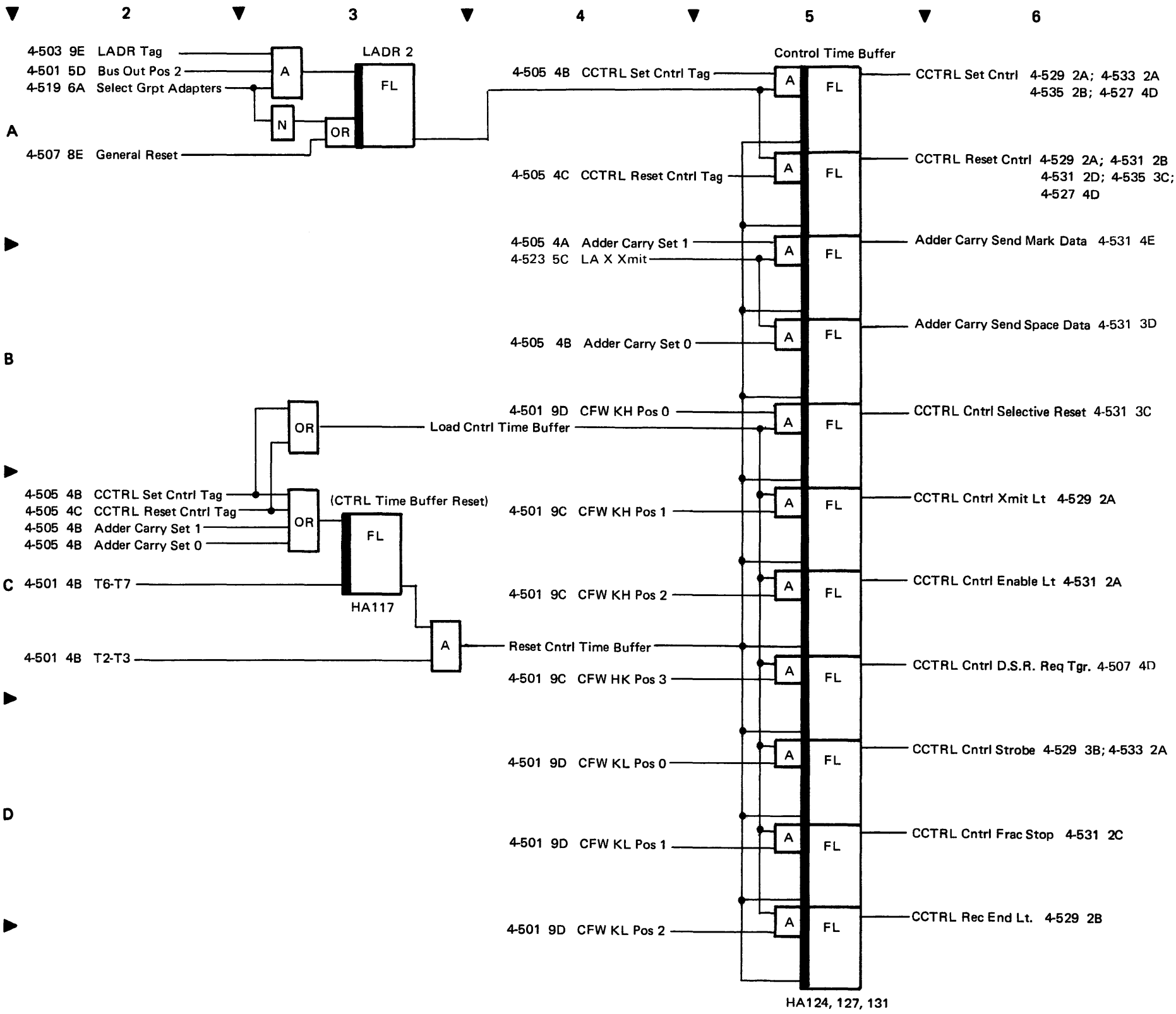
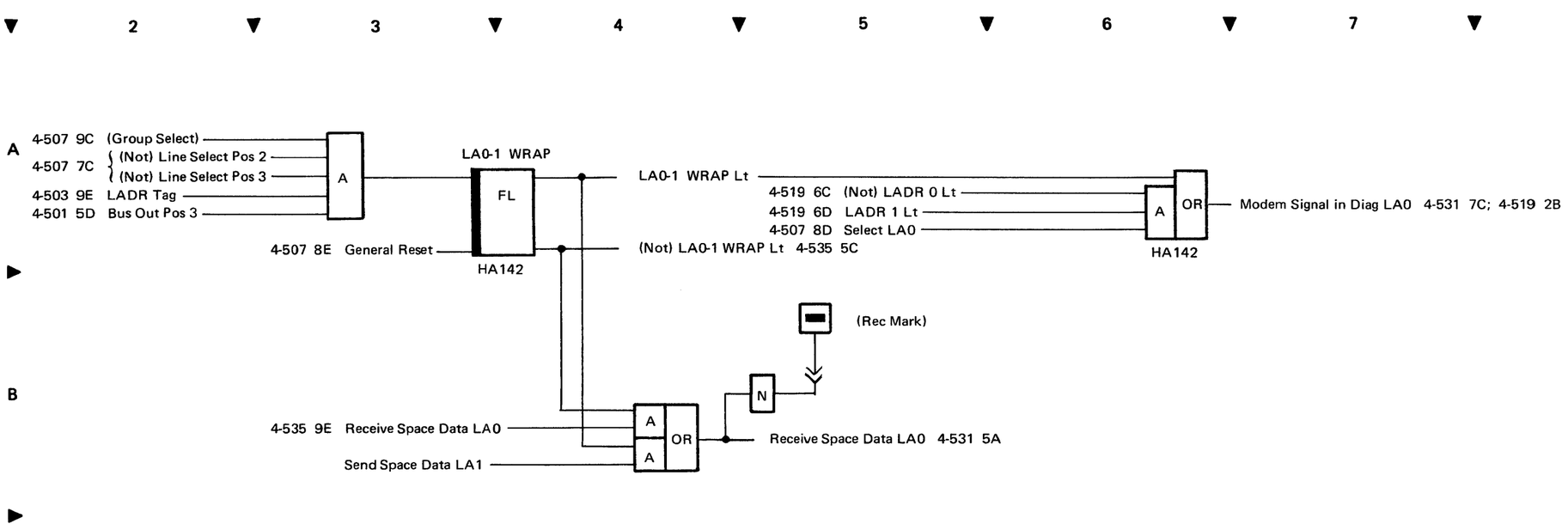
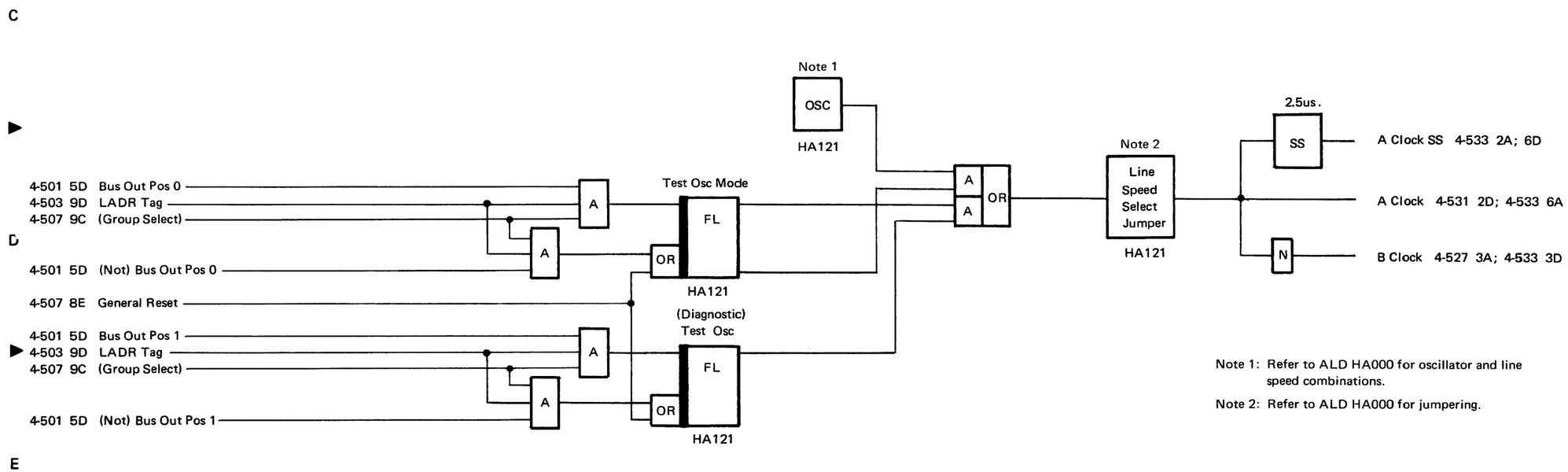


● Diagram 4-521. Control Tag Time Buffer





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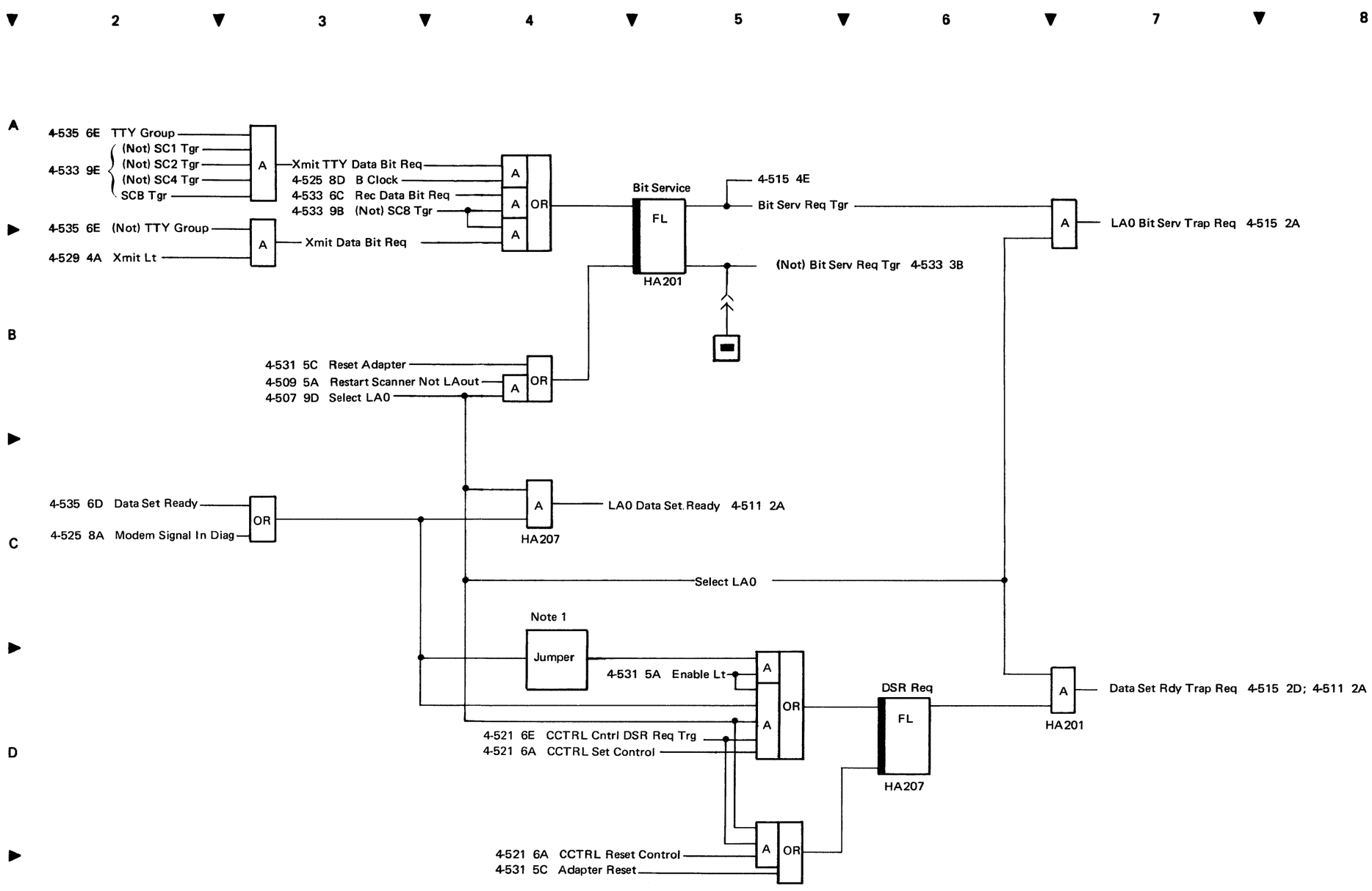
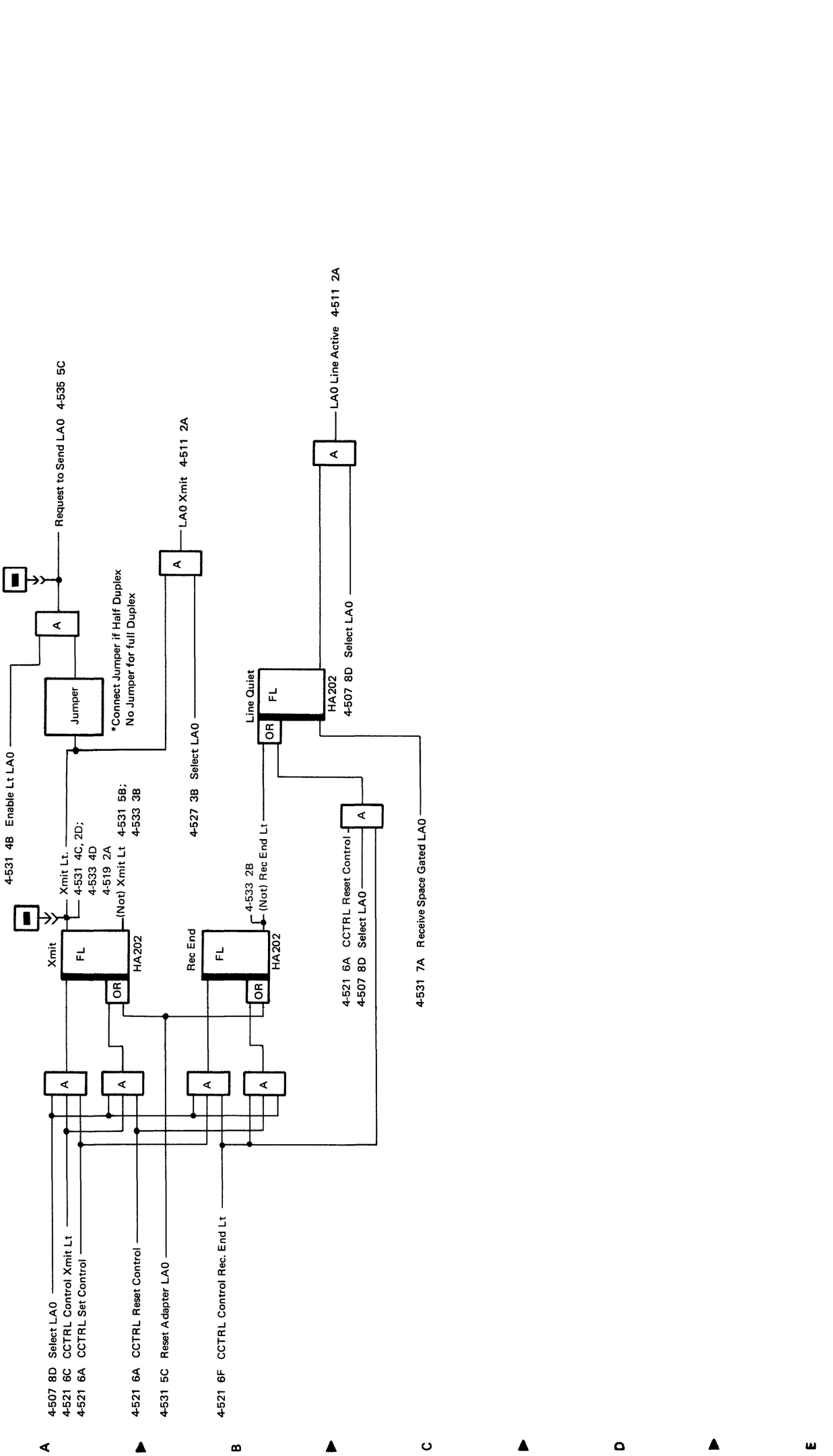
FES Y24-0506

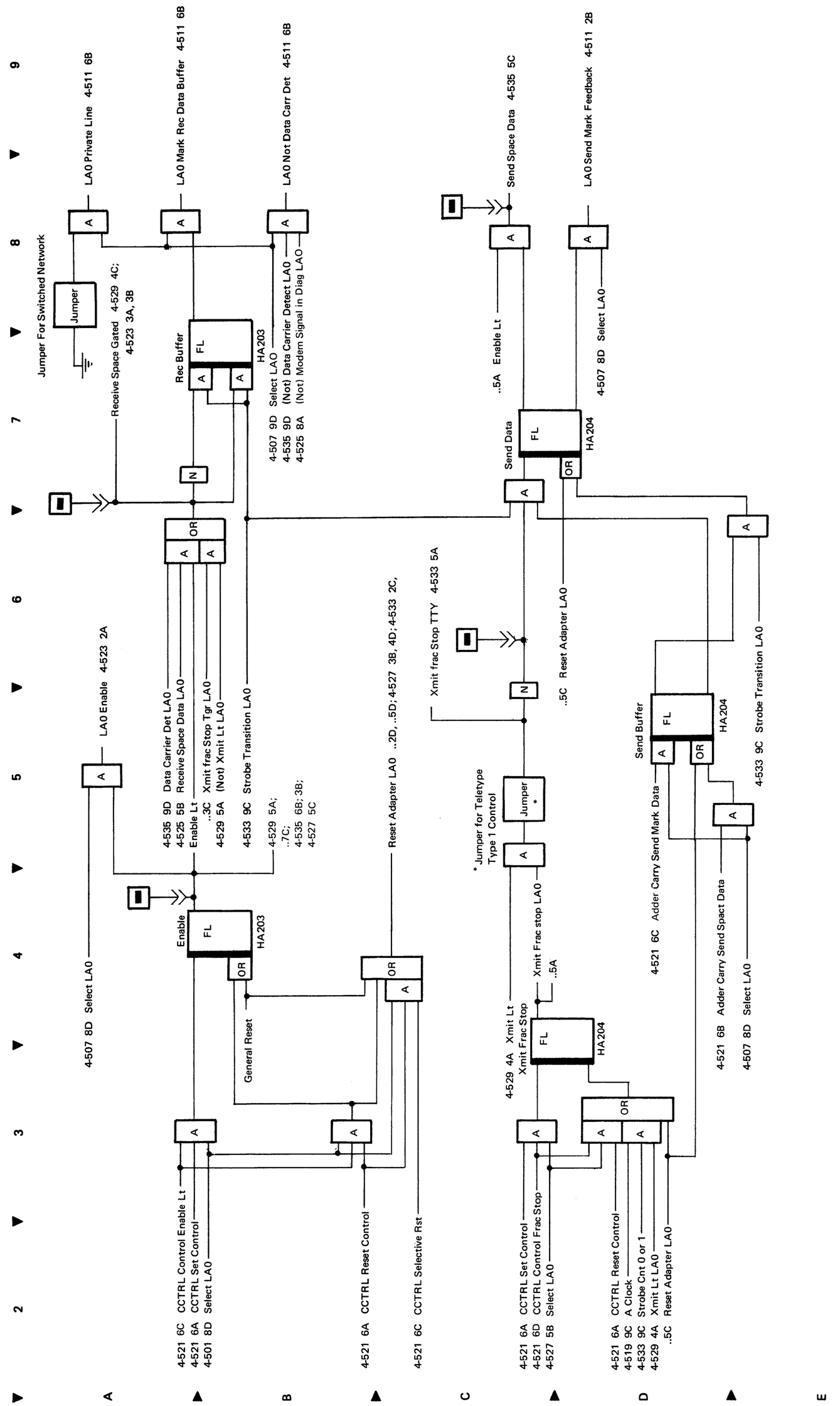
● Diagram 4-527. Bit Service Request and Data Set Ready Request



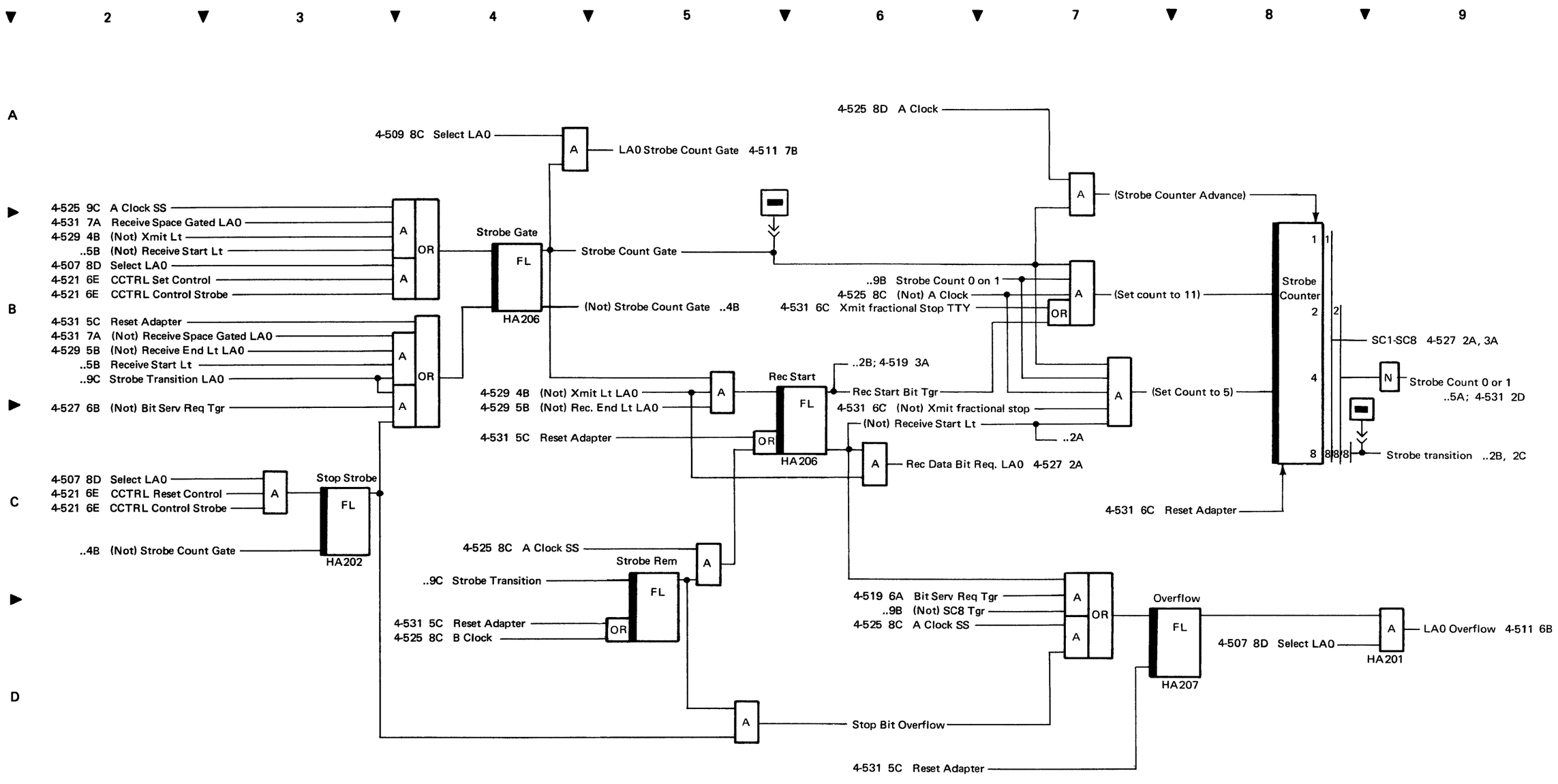
Note 1. Connect jumper for switched network.



● Diagram 4-529. Start/Stop Xmit Latch and Line Quiet Controls

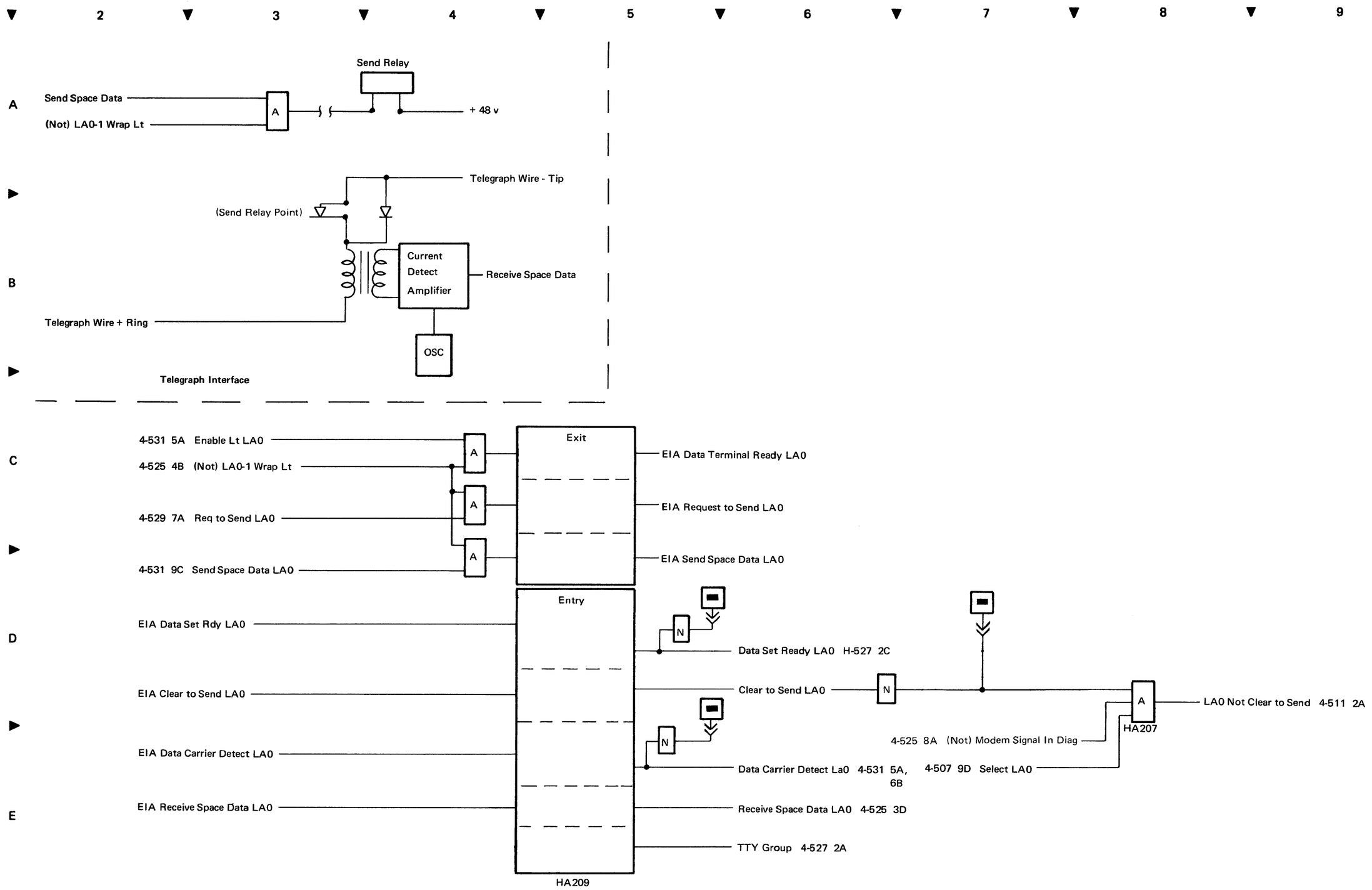


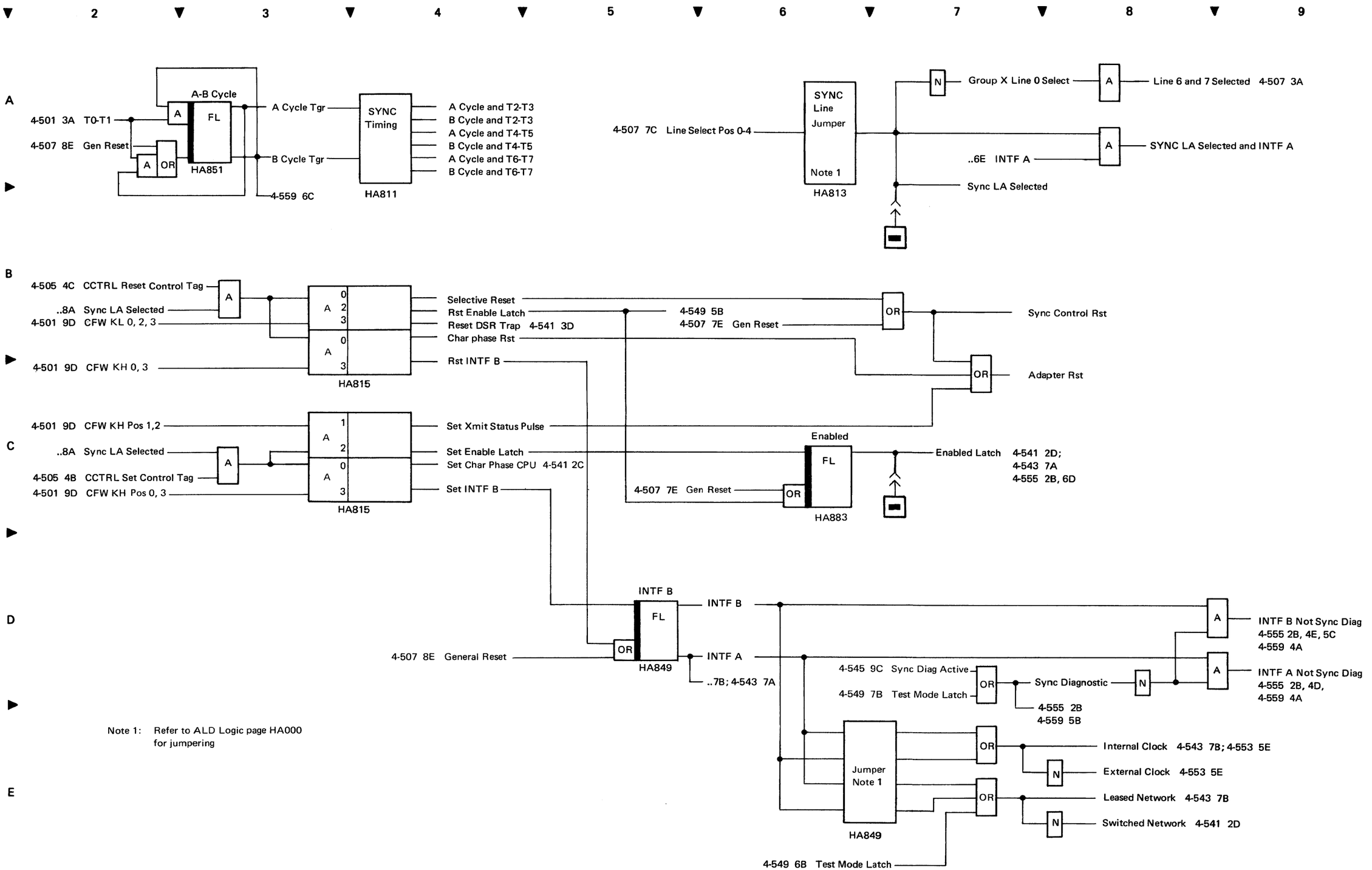
● Diagram 4-531. Start/Stop Receive and Xmit Controls



Form Y24-3529-0
FES Y24-0506

Form Y24-3529-0
FES Y24-0506

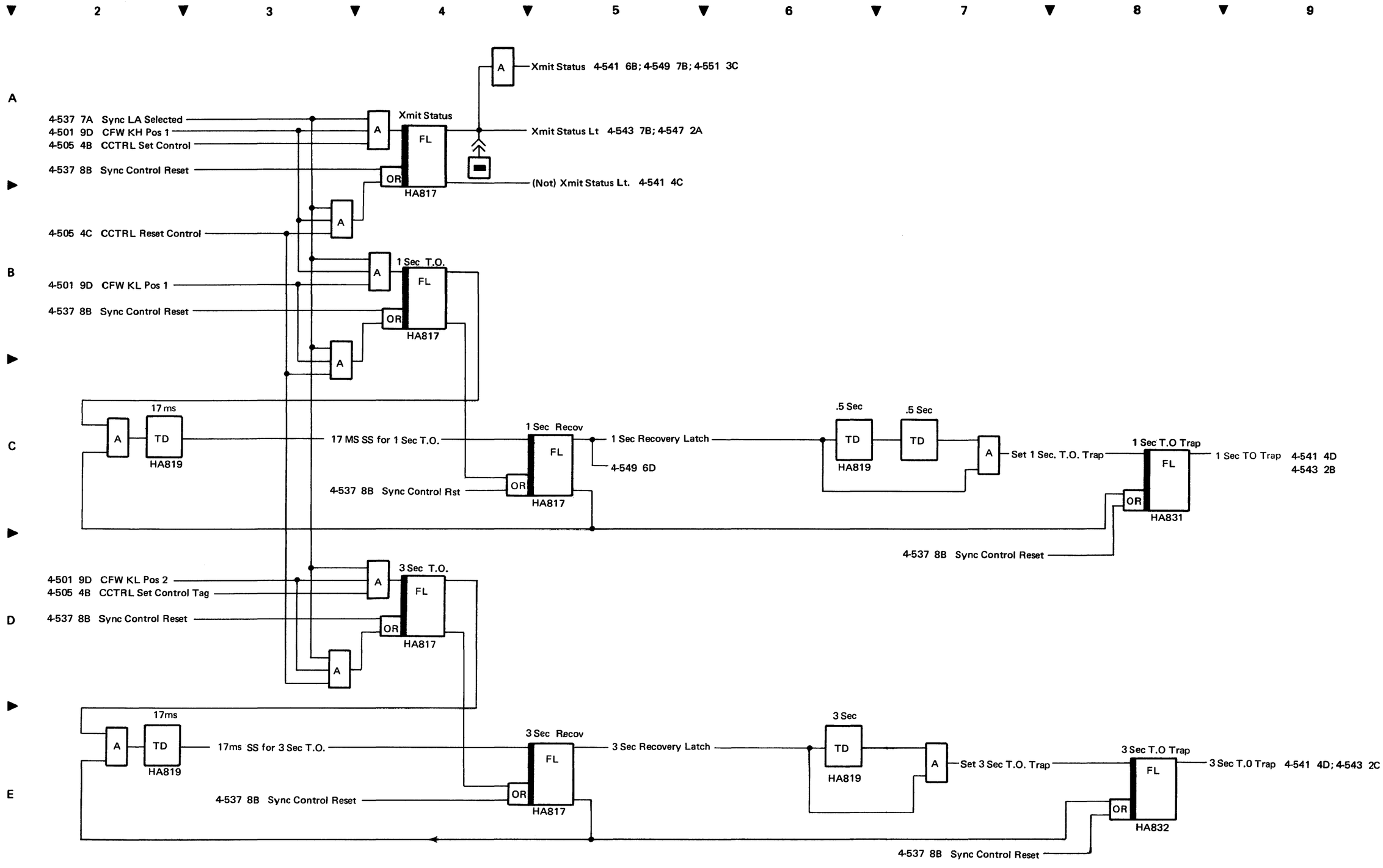


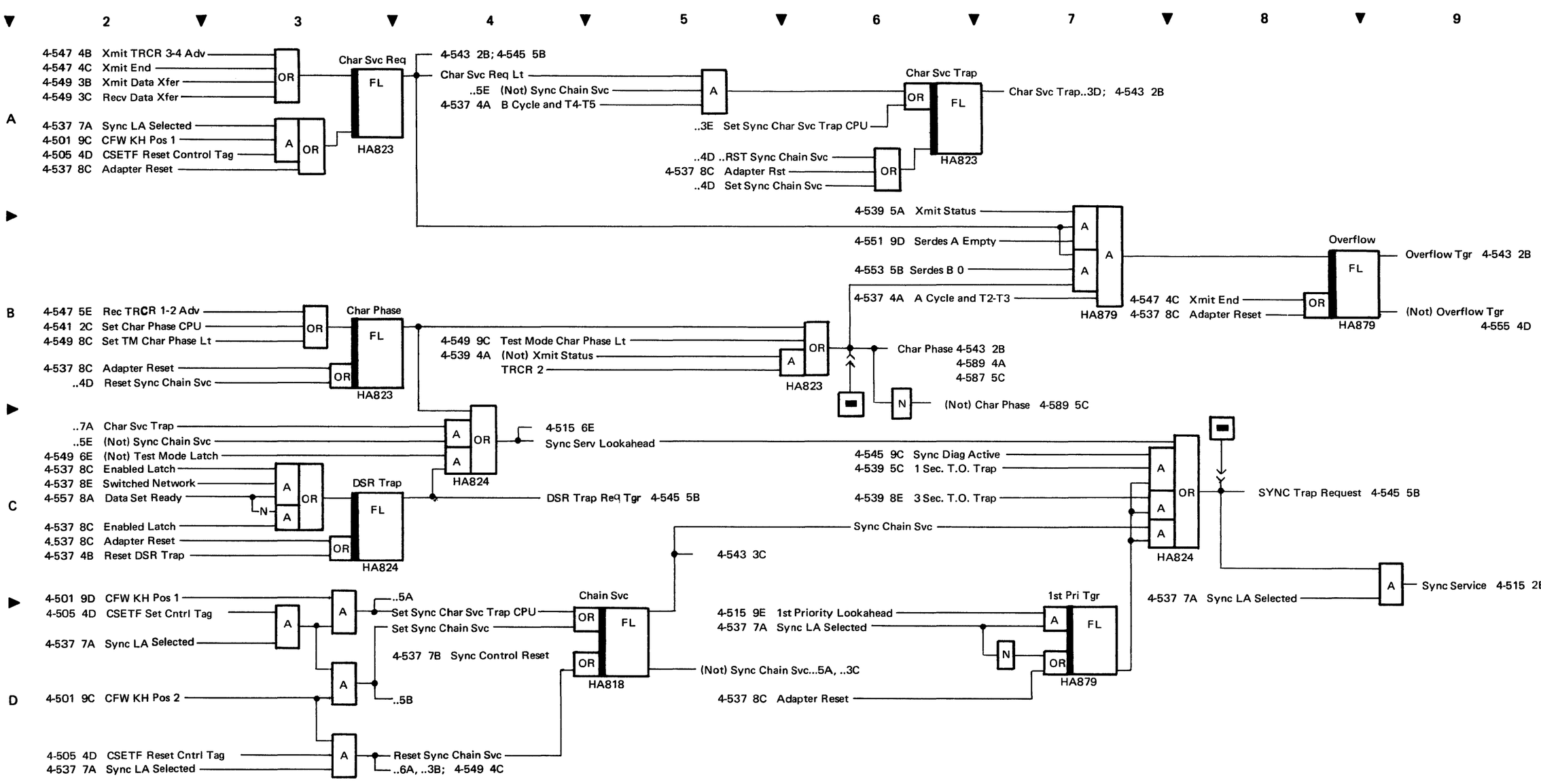


Note 1: Refer to ALD Logic page HA000 for jumpering

Form Y24-3529-0
FES Y24-0506

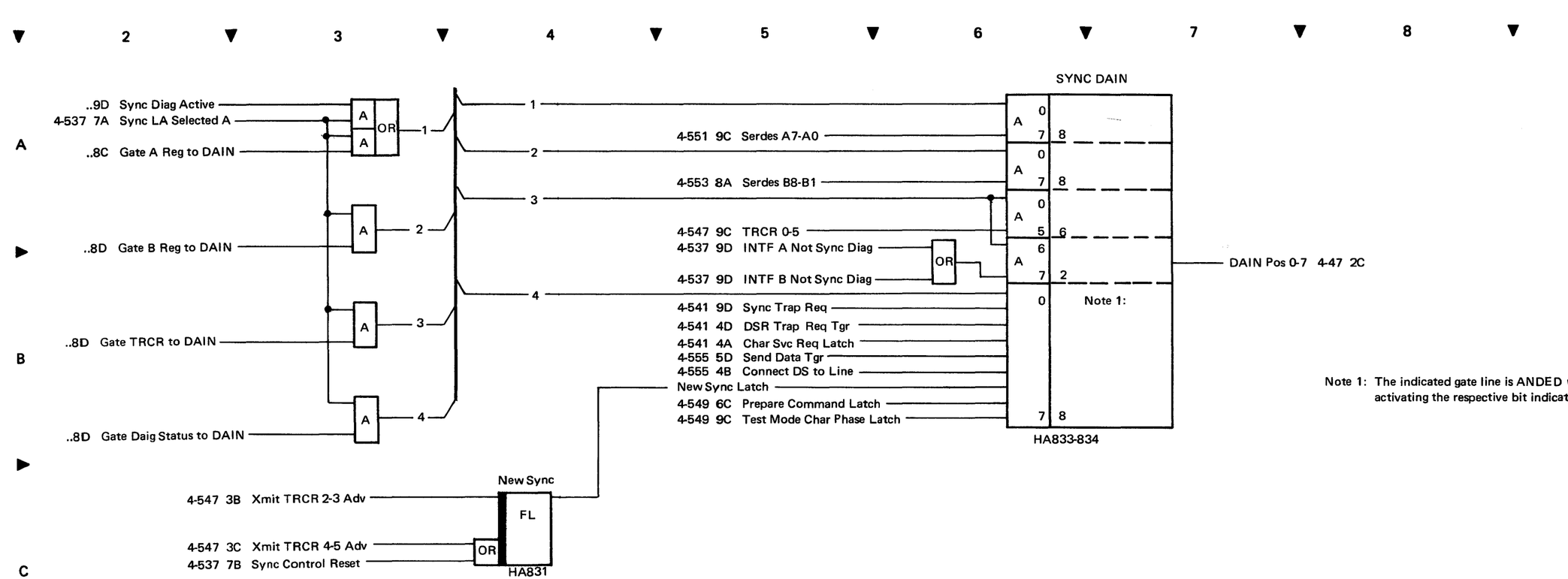
● Diagram 4-539. Sync 1 and 3 Second Timeout Traps

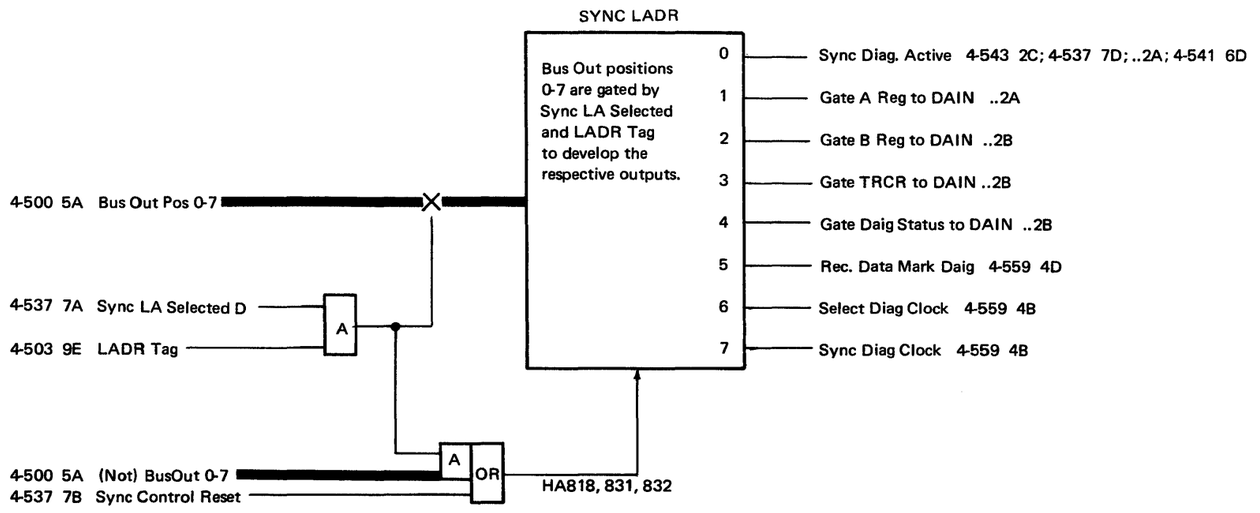




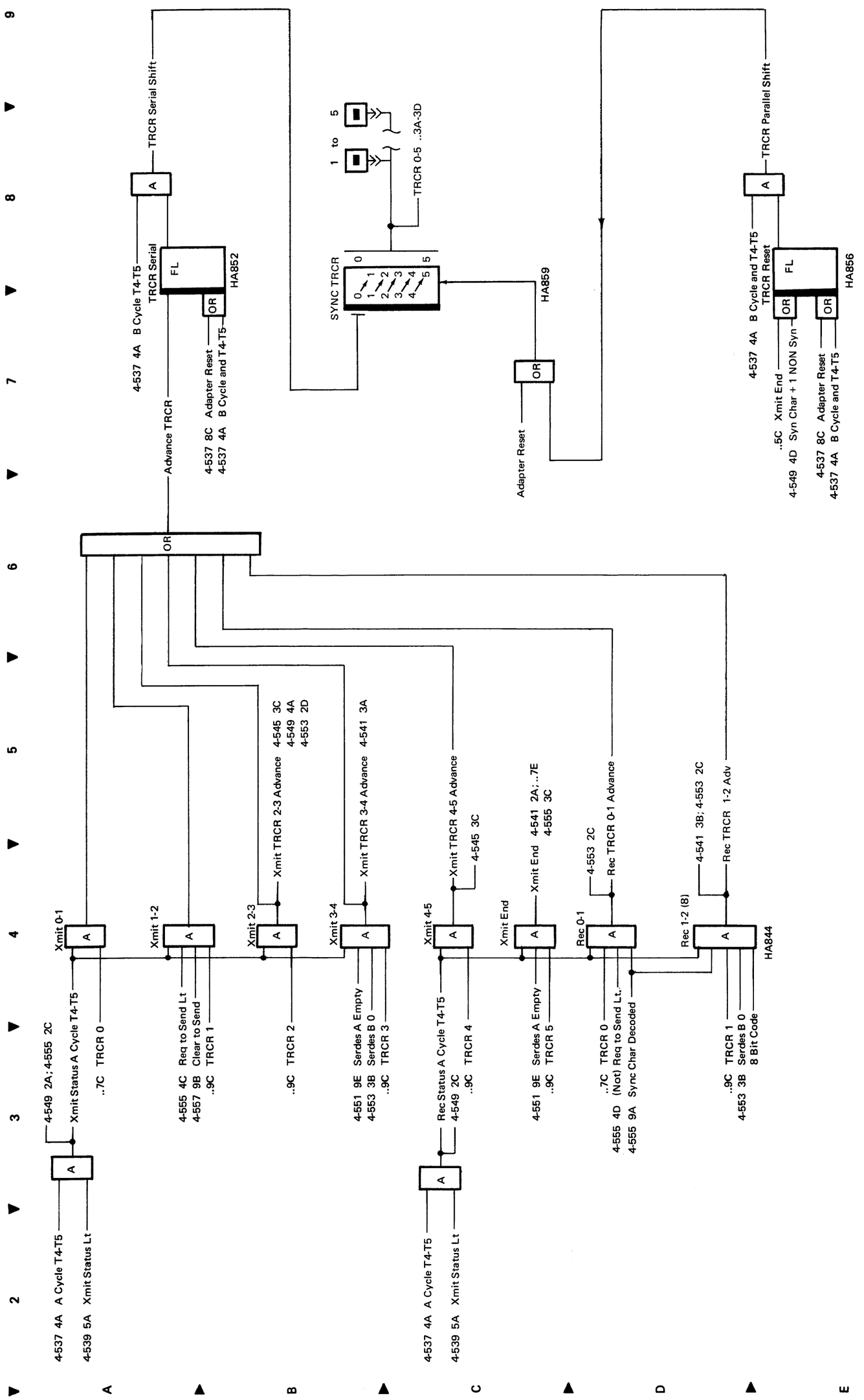
Form Y24-3529-0
FES Y24-0506

● Diagram 4-543. Sync LASTAT and LACON

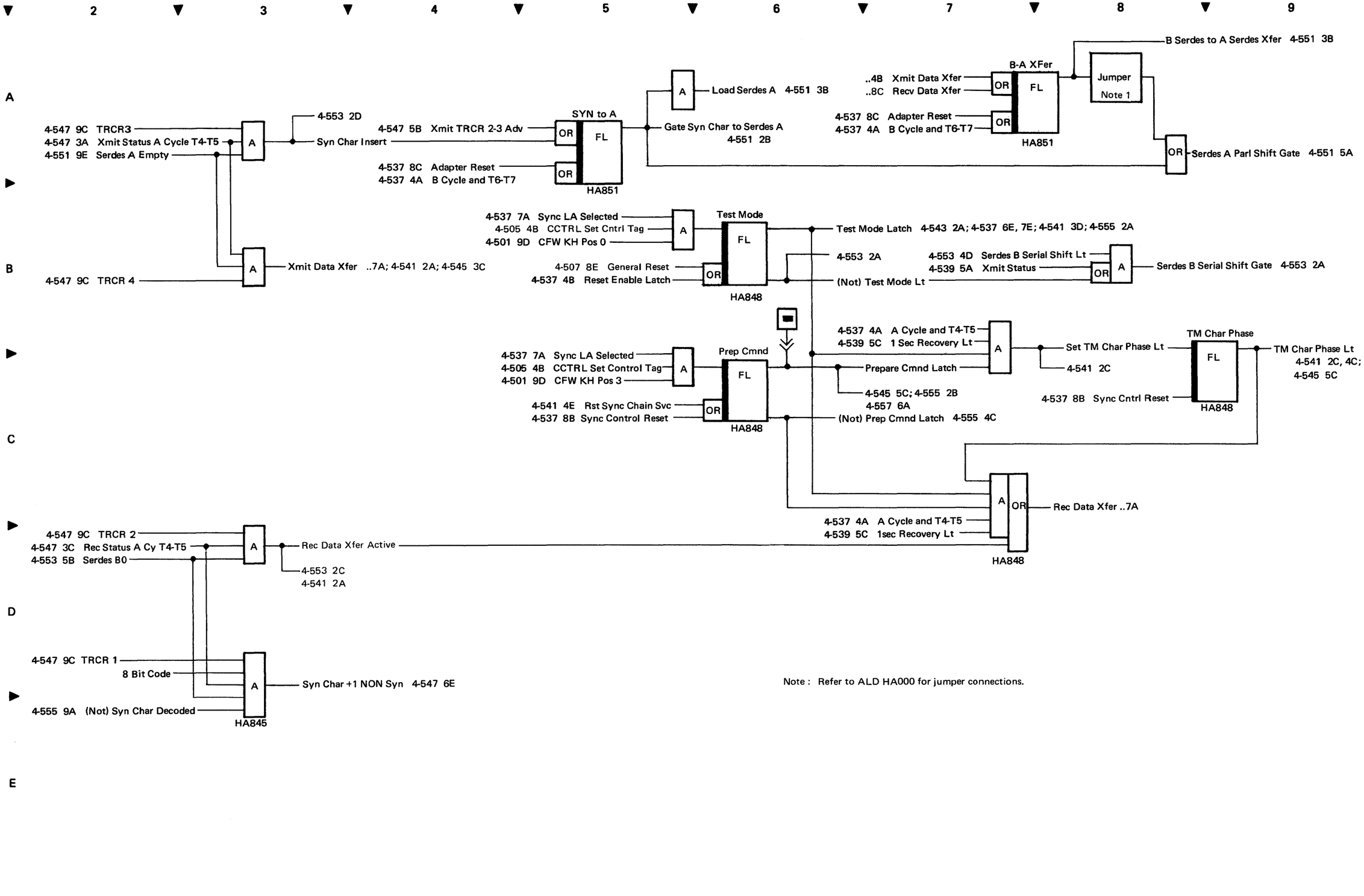




Form Y24-3529-0
FES Y24-0506

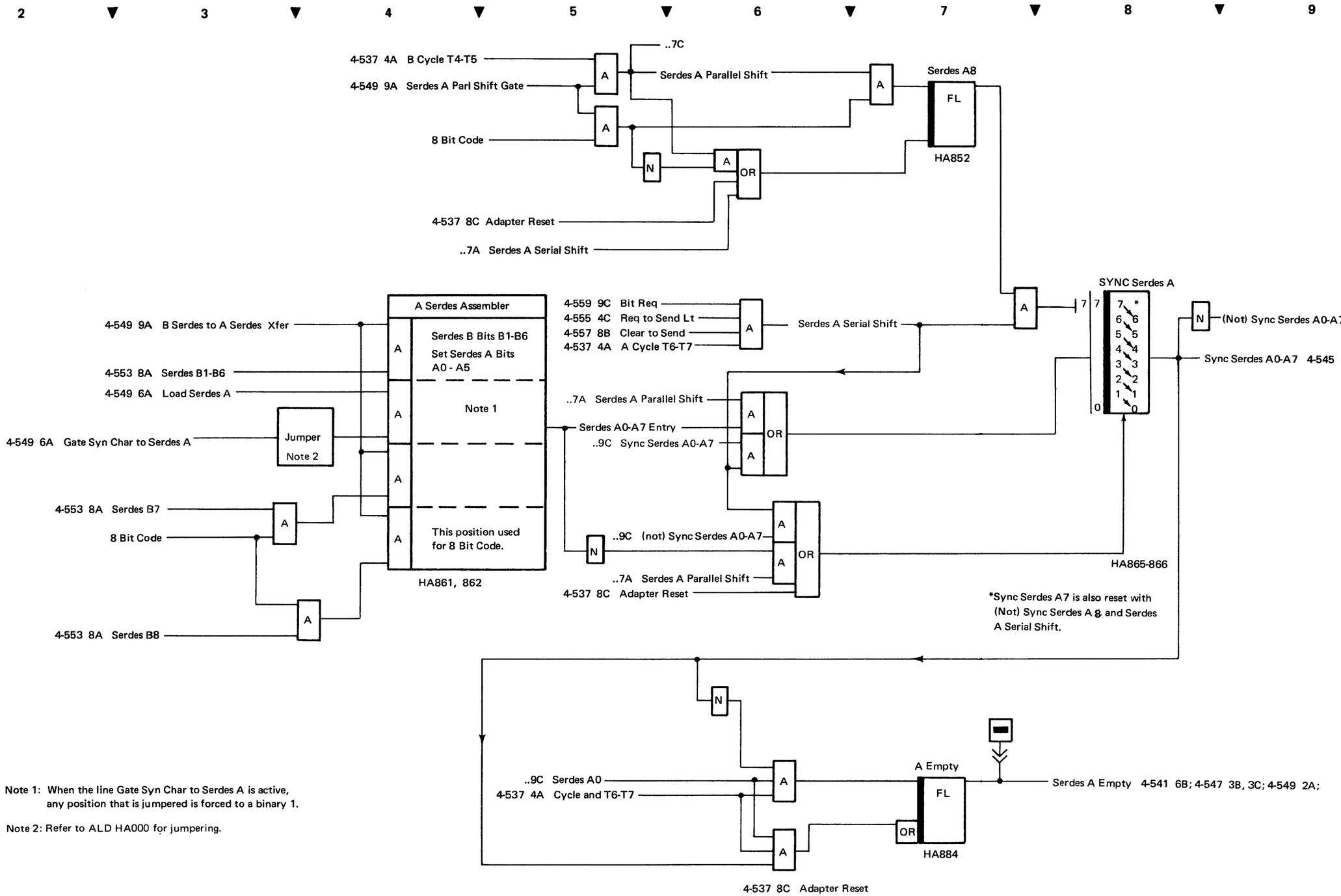


●Diagram 4-547. Sync Transmit Receive Control Register (TRCR)



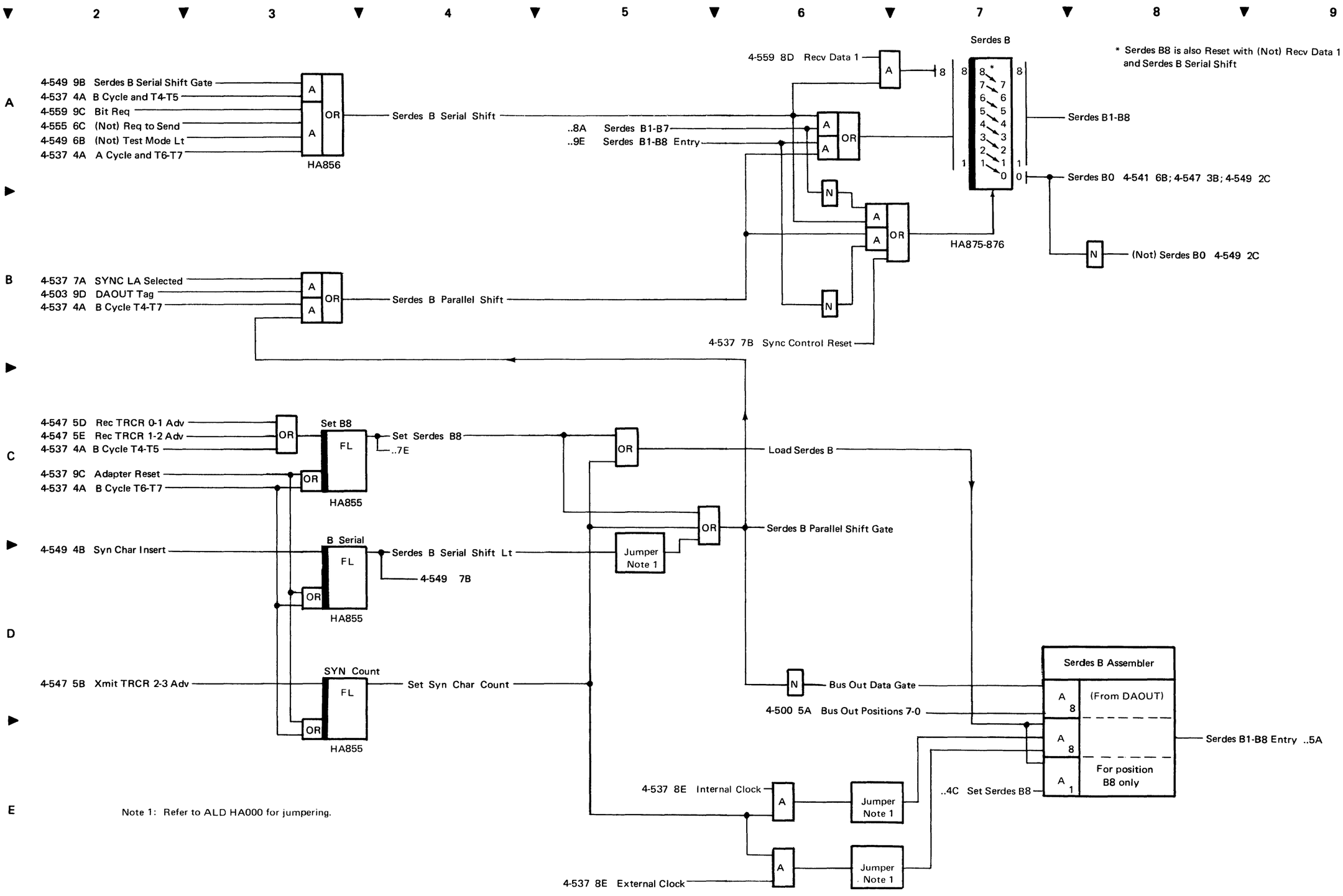
Note : Refer to ALD HA000 for jumper connections.

Form Y24-3529-0
FES Y24-0506



Note 1: When the line Gate Syn Char to Serdes A is active, any position that is jumpered is forced to a binary 1.

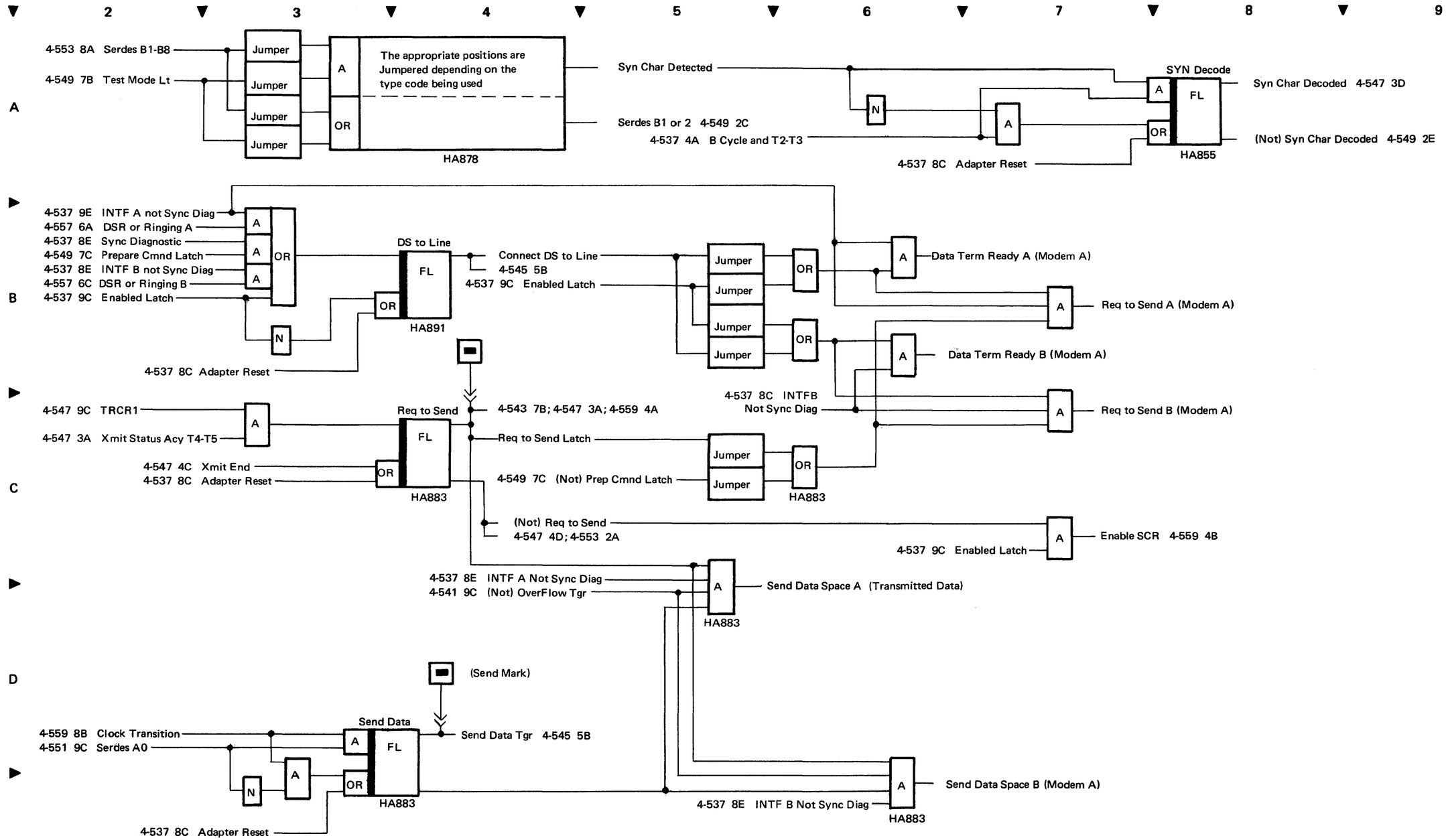
Note 2: Refer to ALD HA000 for jumpering.

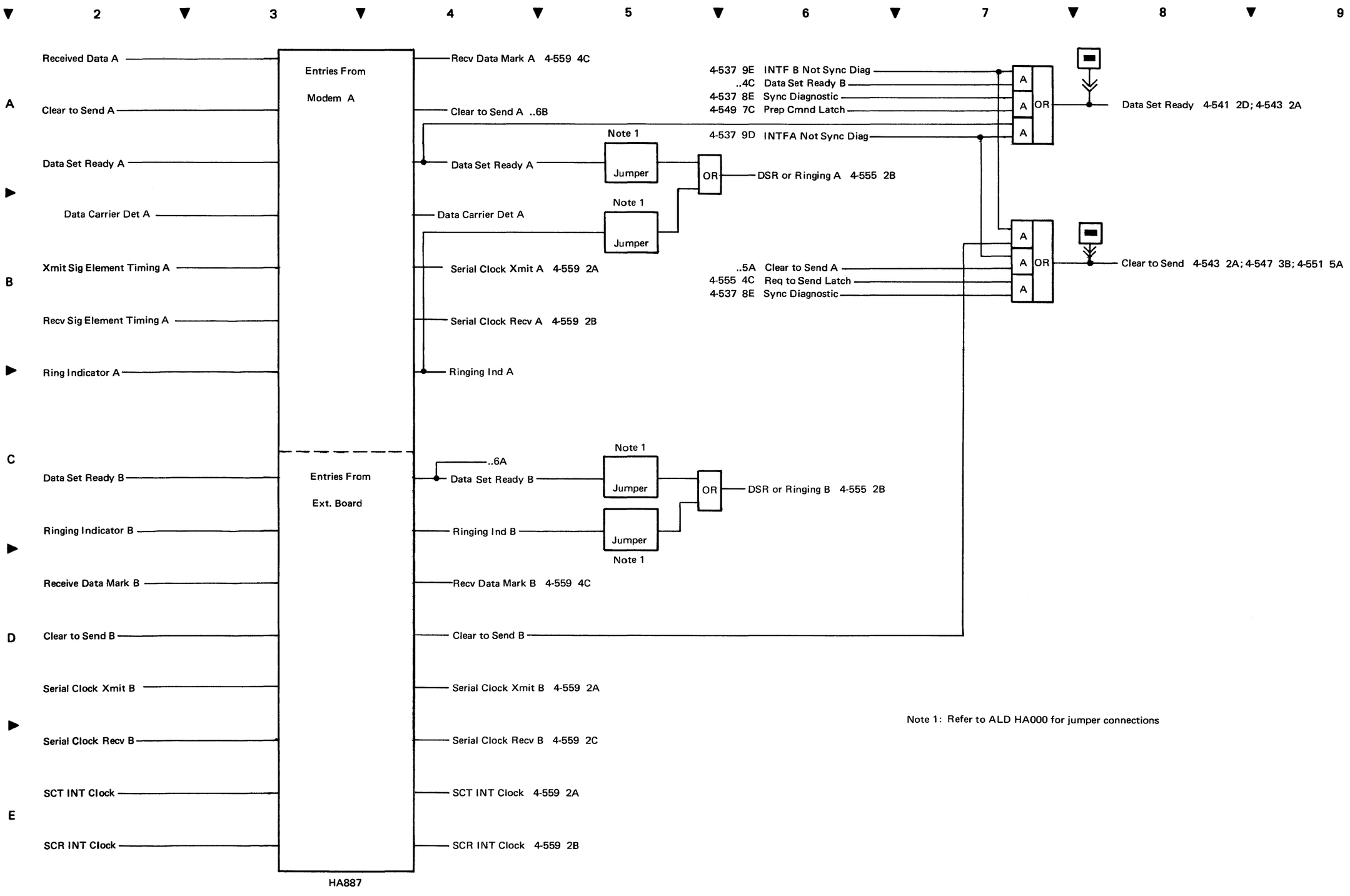


Form Y24-3529-0
FES Y24-0506

● Diagram 4-555. Sync Request to Send, Send Data, and SYN Character Decode

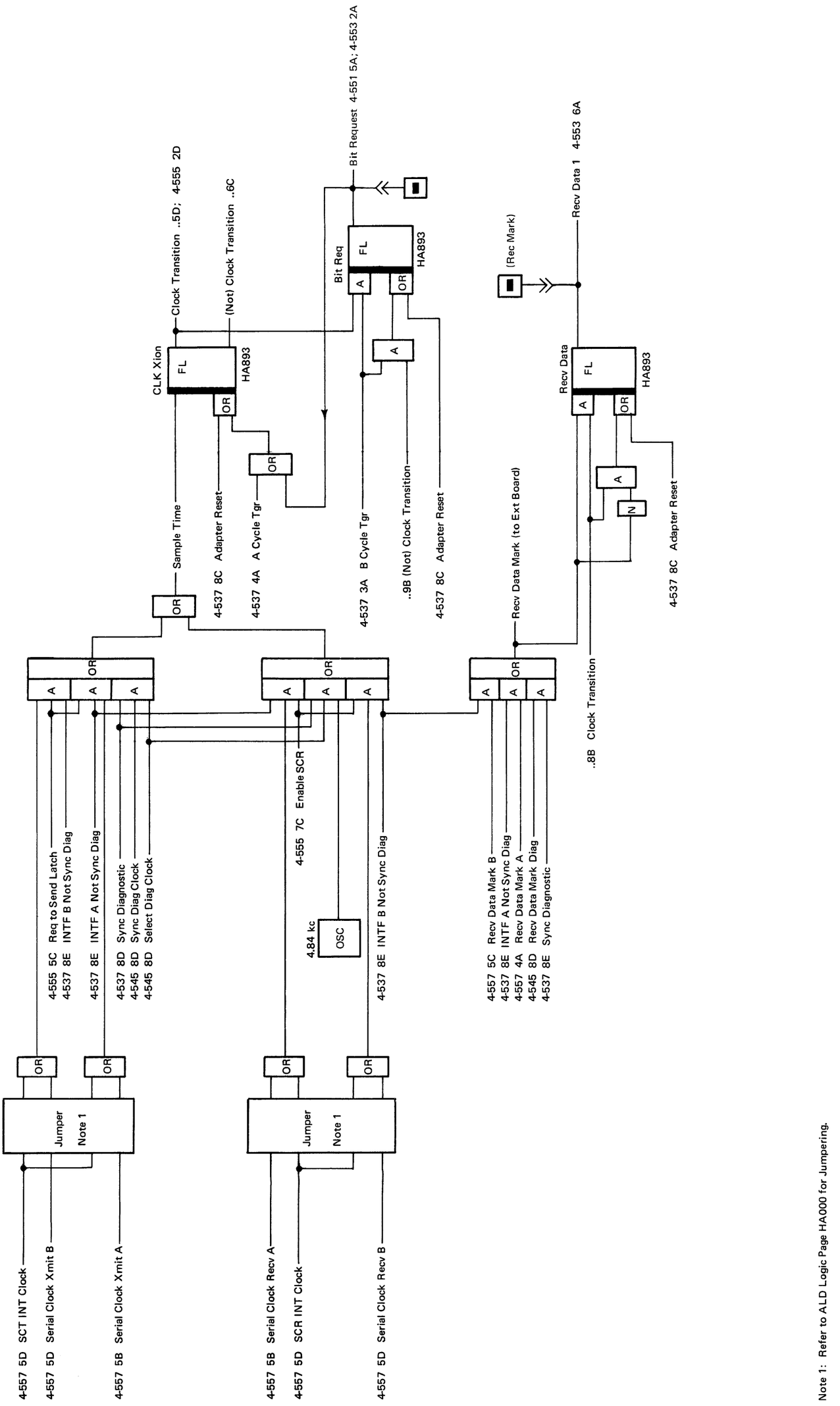
Form Y24-3529-0
FES Y24-0506



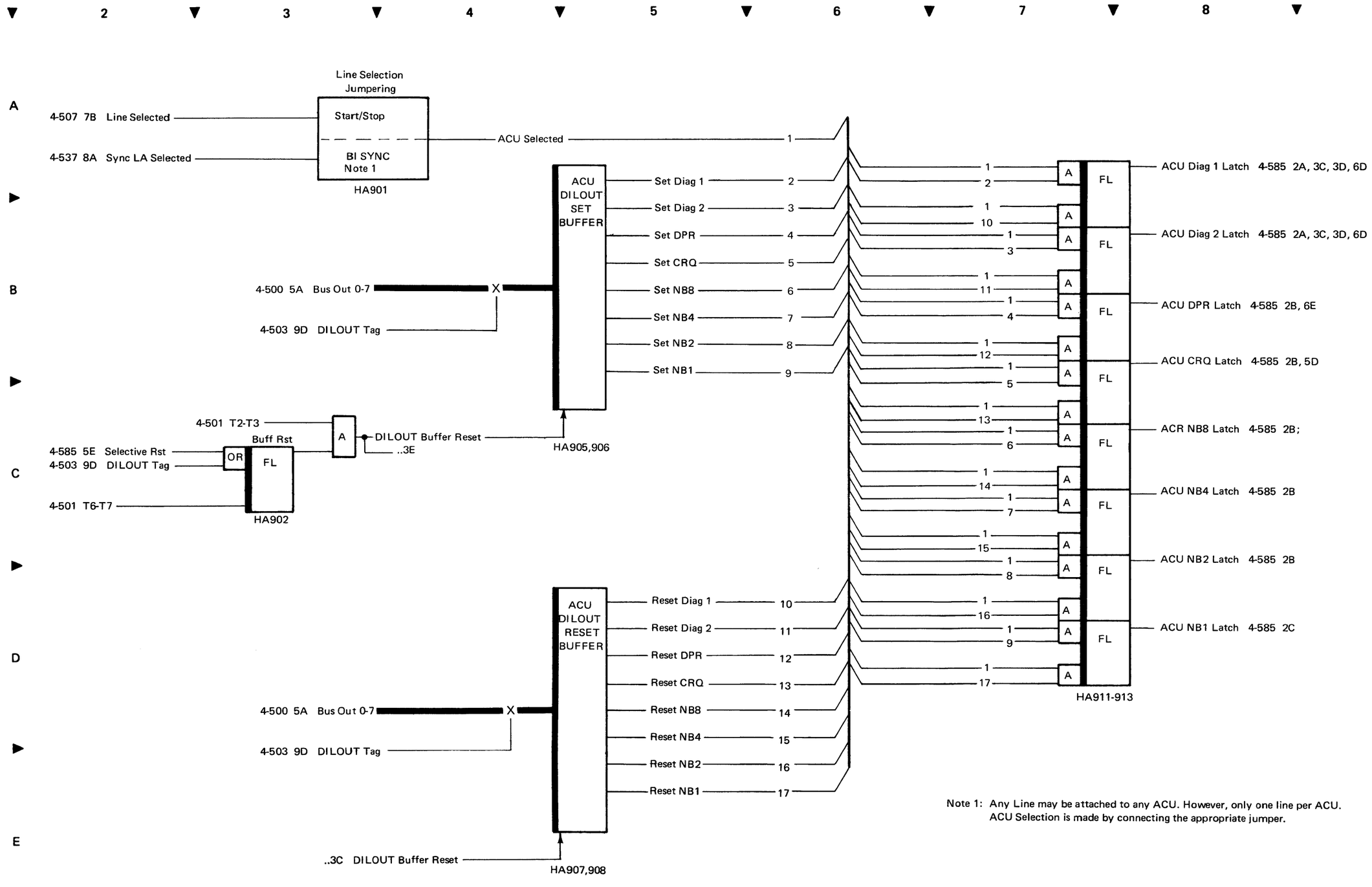


Note 1: Refer to ALD HA000 for jumper connections

Form Y24-3529-0
FES Y24-0506



● Diagram 4-559. Sync Data Set Clock Control

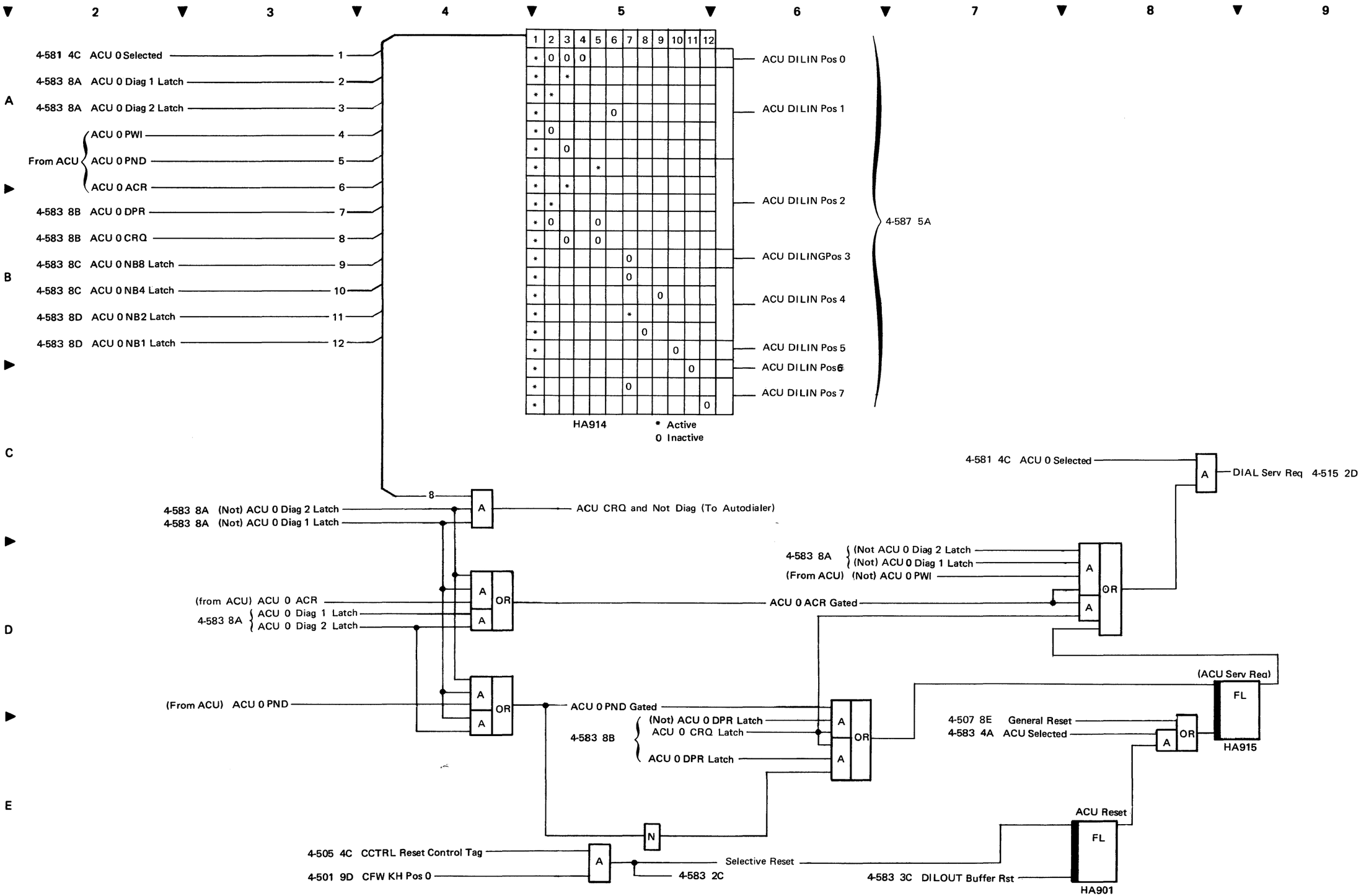


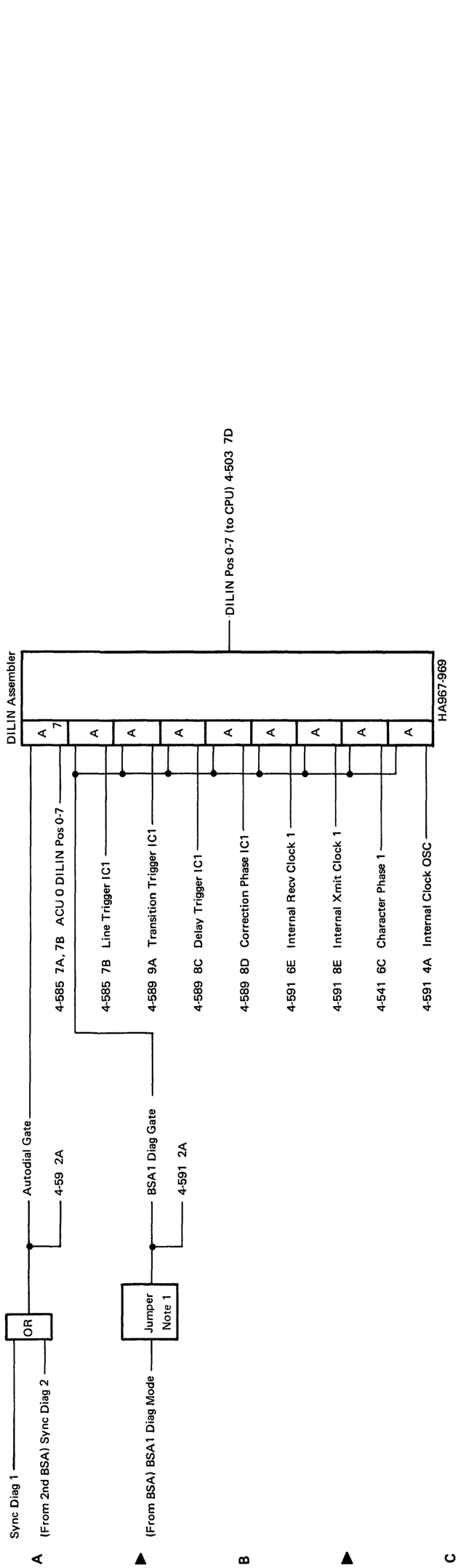
Note 1: Any Line may be attached to any ACU. However, only one line per ACU. ACU Selection is made by connecting the appropriate jumper.

Form Y24-3529-0
FES Y24-0506

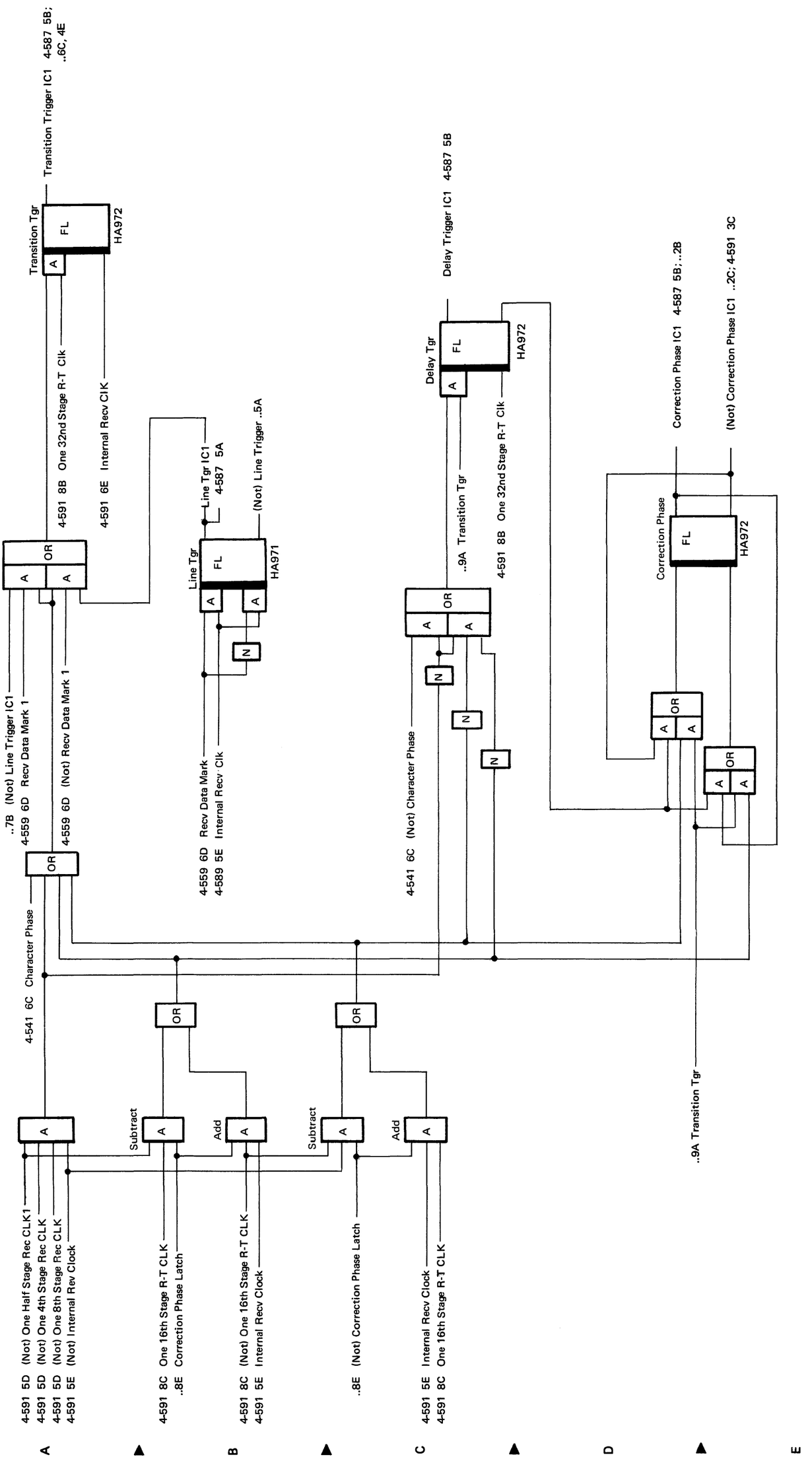
● Diagram 4-585. Automatic Calling Unit (ACU) DILIN and Trap Request

Form Y24-3529-0
FES Y24-0506

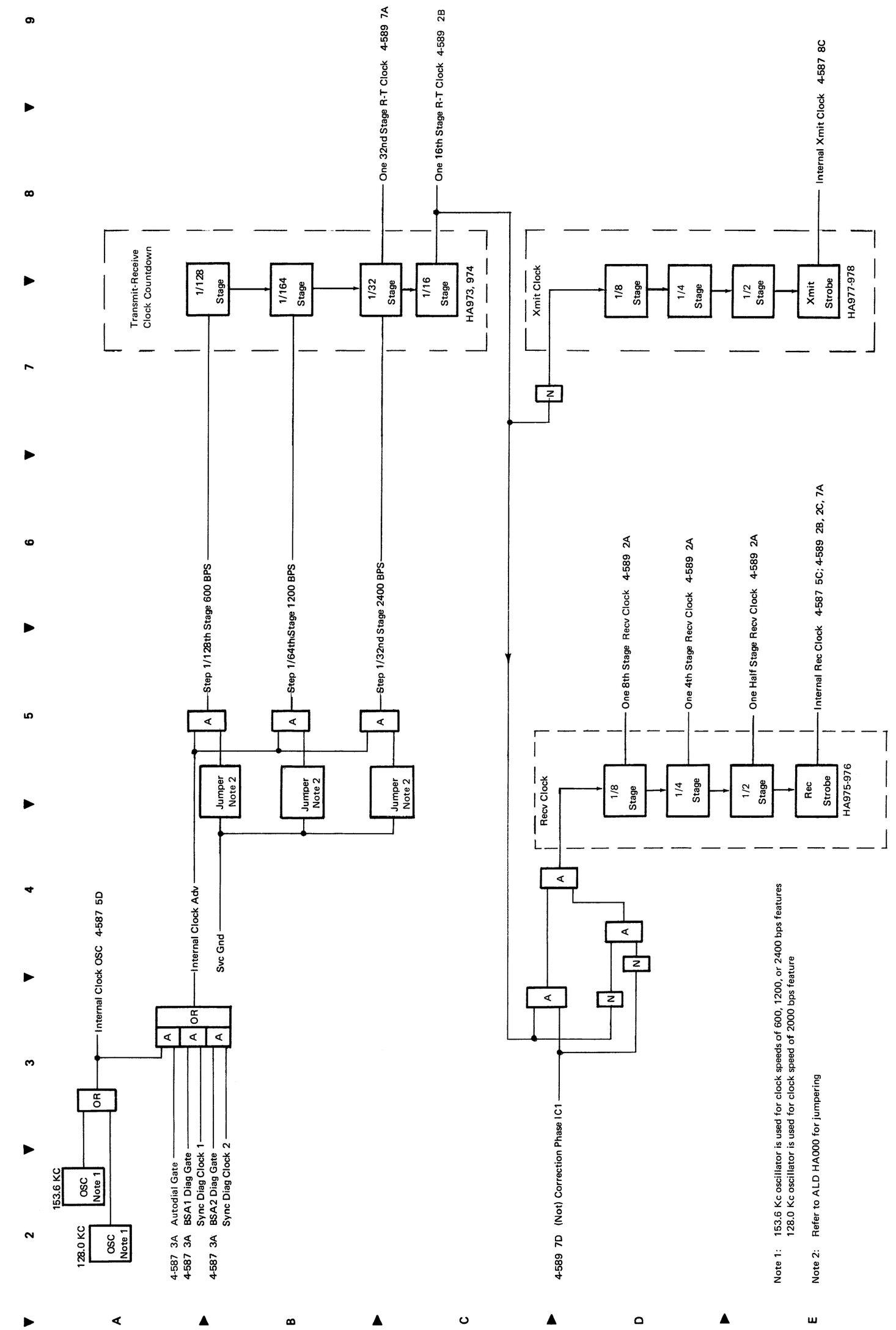




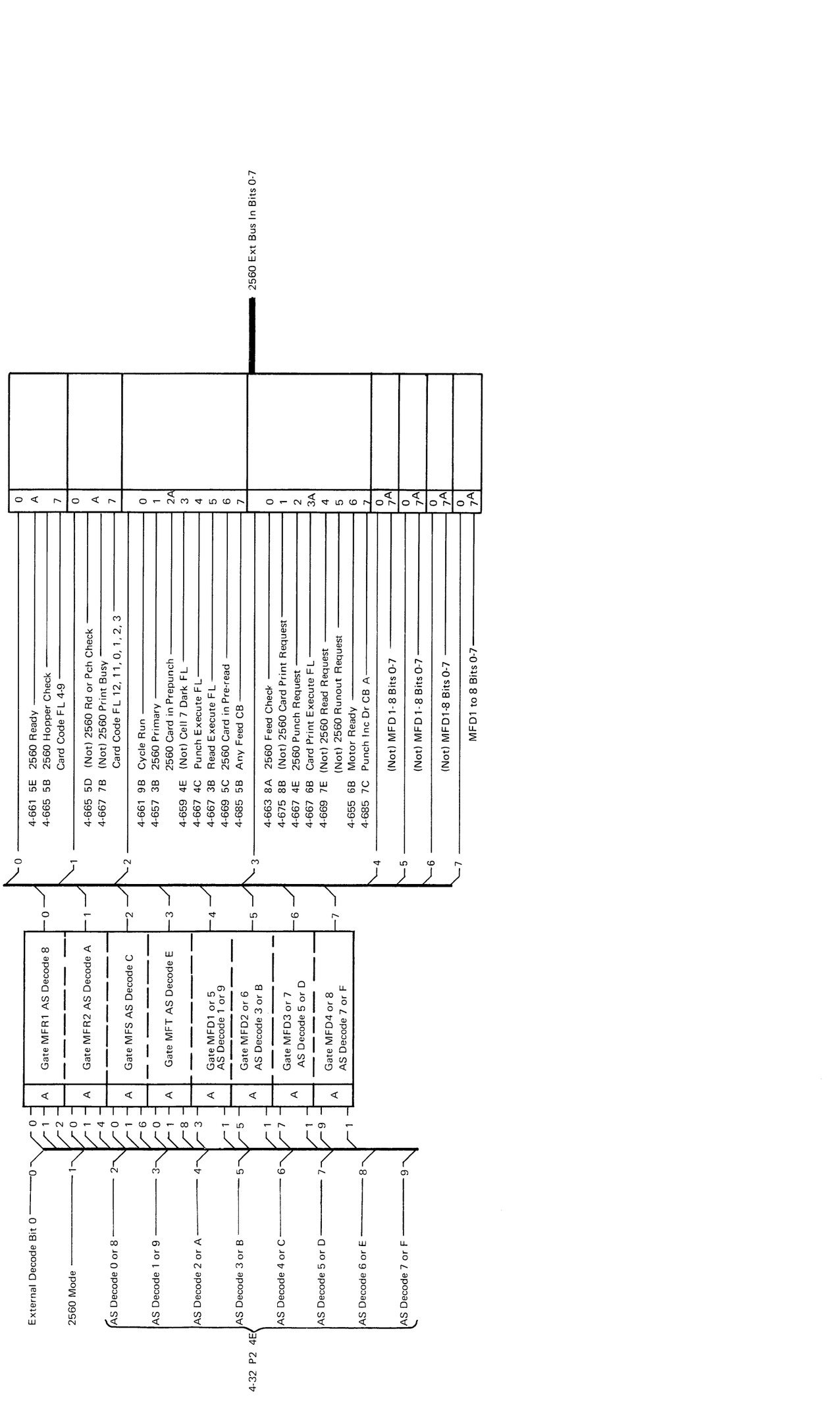
●Diagram 4-587. Automatic Calling Unit (ACU) DILIN Assembler



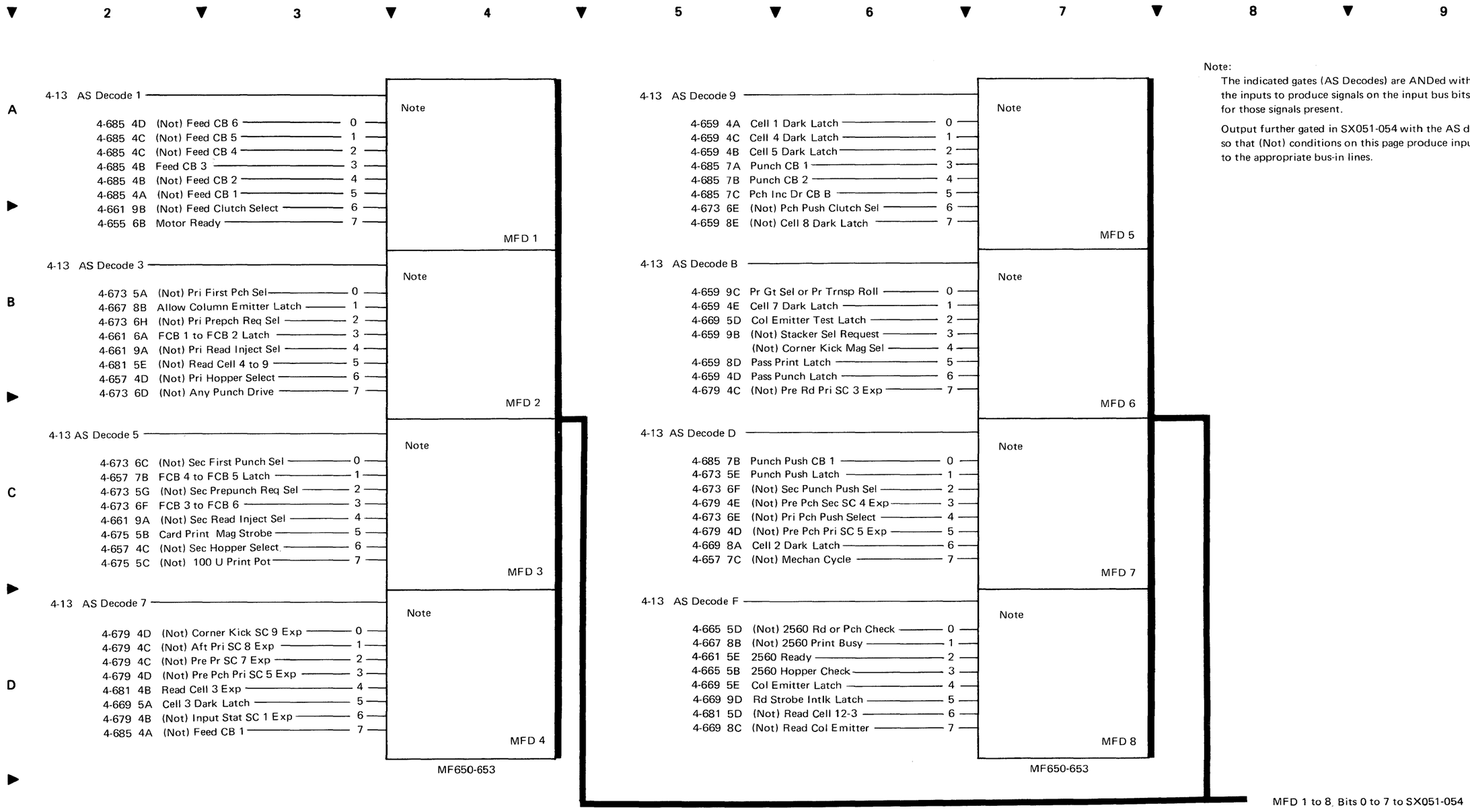
●Diagram 4-589. Sync Internal Clock (IC) Phase Correction



● Diagram 4-591. Sync Internal Clock (IC) Receive-Transmit Clock, Receive Clock, and Transmit Clock



● Diagram 4-651. External Facilities for the IBM 2560 Attachment (2560 Mode)



Note:

The indicated gates (AS Decodes) are ANDed with the inputs to produce signals on the input bus bits 0-7 for those signals present.

Output further gated in SX051-054 with the AS decodes so that (Not) conditions on this page produce inputs to the appropriate bus-in lines.

2 3 4 5 6 7 8 9

A
4-663 9B (Not) 2560 Feed Ck
4-661 9B 2560 Cycle Run
4-679 8B 2560 NPRO Latch
4-667 5A Any 2560 Execute
OR
Execute Command 4-663 6D
Motor Latch
A FL
MF101

4-657 3D Start Inhibit
2560 (Not) Motor Hold Sw
4-661 5D Stop Condition
OR

N A Motor Delay 500ms Min
DLY Motor TD
Motor Relay Select 2560

Power On Reset
Set Power On Reset Latch
4-679 4A (Not) Diag On
2560 NPRO Key
N A FL
MF522

B
4-659 4D (Not) Pass Punch Latch
4-657 8D Run-in Cycle
A Run In Rattle 2560

(Not) Card Print Bit 15
DLY Control A Delayed 4-667 3B; 4-673 4F

4-13 Ext AS Field Decode F
2560 Mode
Wd Type 0 Set Pulse
A Control A 4-657 2B 4-661 7D

4-679 4A Diag On
2560 By Pass Motor Rdy Dly
N N OR OR OR A
MF101

Motor Ready

4-12 K Low Bit 2
4-679 8D NPRO Intlk Latch
4-685 4C FCB 5
CPU CSL Sw
A OR

Reset Emulate 4-693 3B; 4-695 2B
OR Power On Reset ..7E
OR 2560 Reset 4-659 3A; 4-655 3B, 7B; 4-667 3D
OR 2560 Stop or Reset 4-667 6B; 4-675 6C
Machine Reset Sw

C
4-13 Ext AS Field Decode D
A Control B 4-661 3C; 4-665 3D; 4-667 3D

4-13 Ext AS Field Decode B
A Control C 4-661 7D; 4-665 7A, 3C

Motor TD
A FL
N
MF610

4-659 4A Cell 1
Dark Latch
3A Execute Command
A

(CE Switch) CE Mode
A Unconditional Check Stop 4-679 6C
Jumper MF522

4-667 7B 2560 I/O Check 2
4-679 4A Diag On
OR 2560 Error to Console

2560 Stop Key
N OR Stop or All Stations Empty 4-661 3C

D
Wd Type 0 Reset Pulse
A Control A Prime 4-693 4A; 4-695 3D

A Control B Prime 4-693 3C 4-695 2A

4-659 4D Pass Punch Latch
4-669 8A Cell 2 Dark Latch
4-669 5A Cell 3 Dark Latch
4-659 4C Cell 4 Dark Latch
4-659 4B Cell 5 Dark Latch
4-659 4E Cell 7 Dark Latch
OR (Not) All Stations Empty
MF101

A Control C Prime 4-661 3B; 4-693 4E

E
A 2560 Ext Gate 4-675 6A

Gate CPU to Ext Pulse Pwr
4-13 Ext AS Field Decode 3
A Punch Data Buffer Gate 4-665 3D 4-667 5E

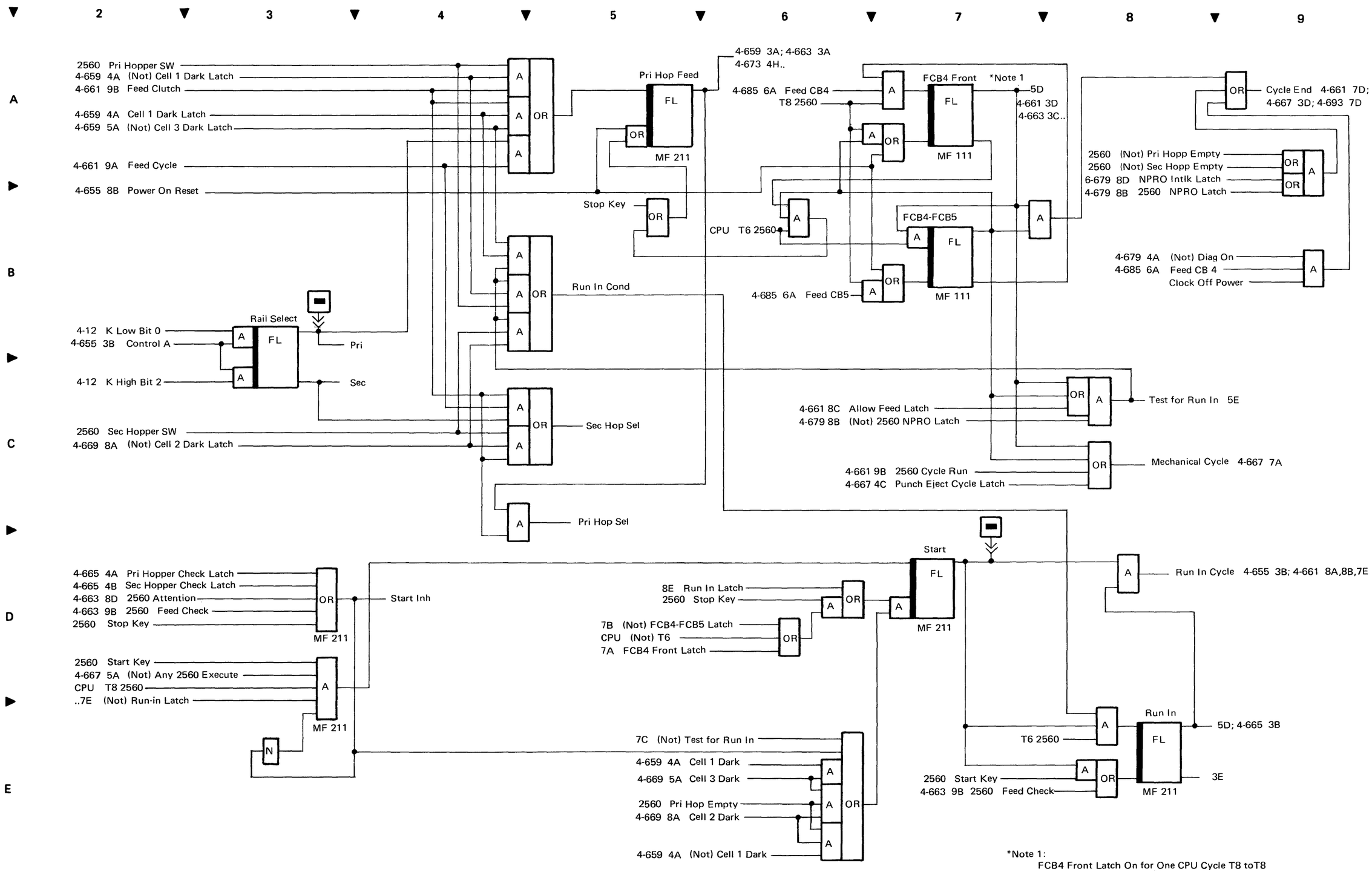
4-13 Ext AS Field Decode 1
A Set Stacker Sel Req 4-659 7A 4-667 7D

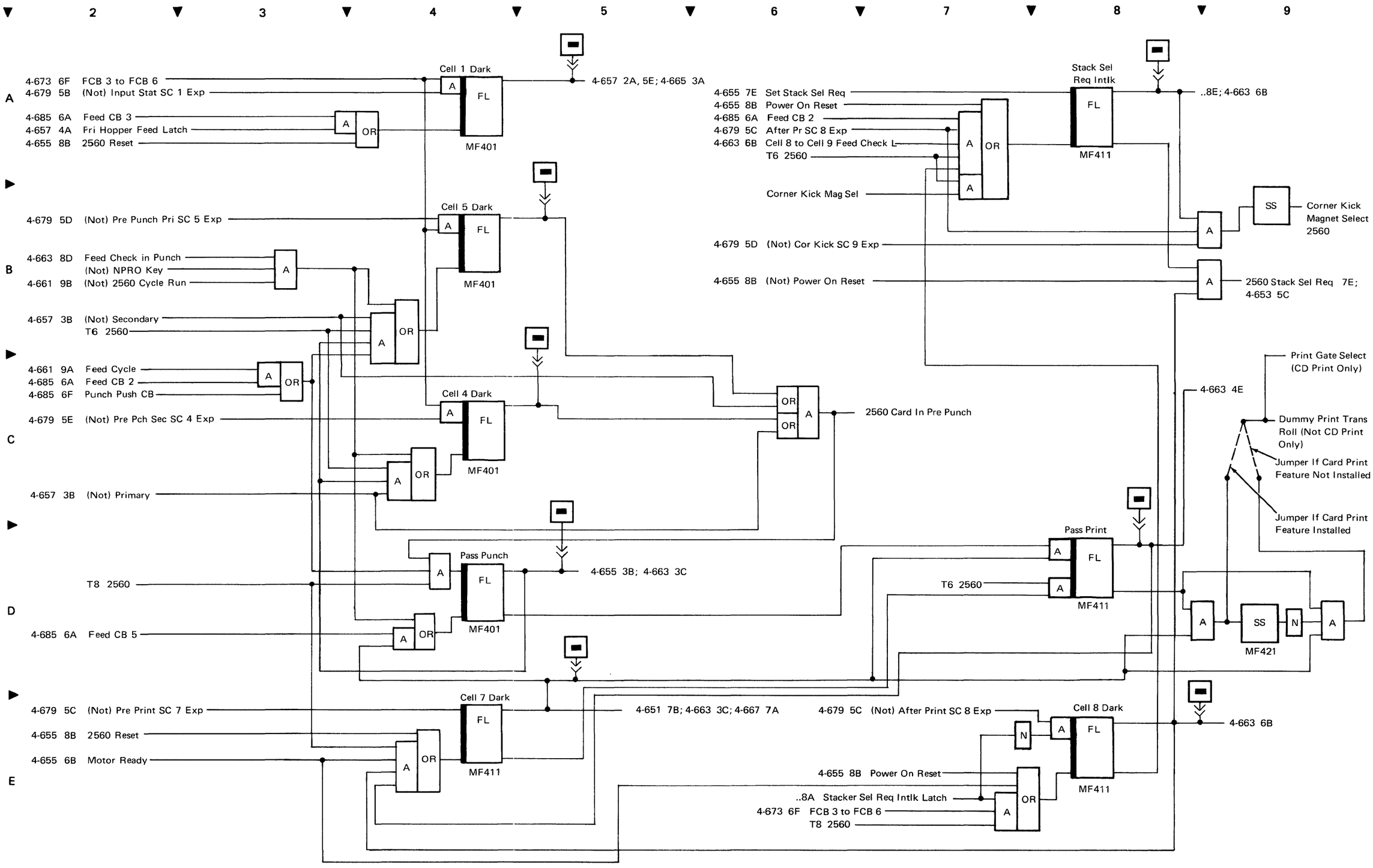
4-13 Ext AS Field Decode 5
A Set Head Sel Req 4-675 3D

2560 Meter
4-667 5A Any 2560 Execute
FL
Metering Out
A 2560 Meter Go
..8B Power On Reset
4-679 8B NPRO Latch
OR
MF101

Form Y24-3529-0
FES Y24-0503

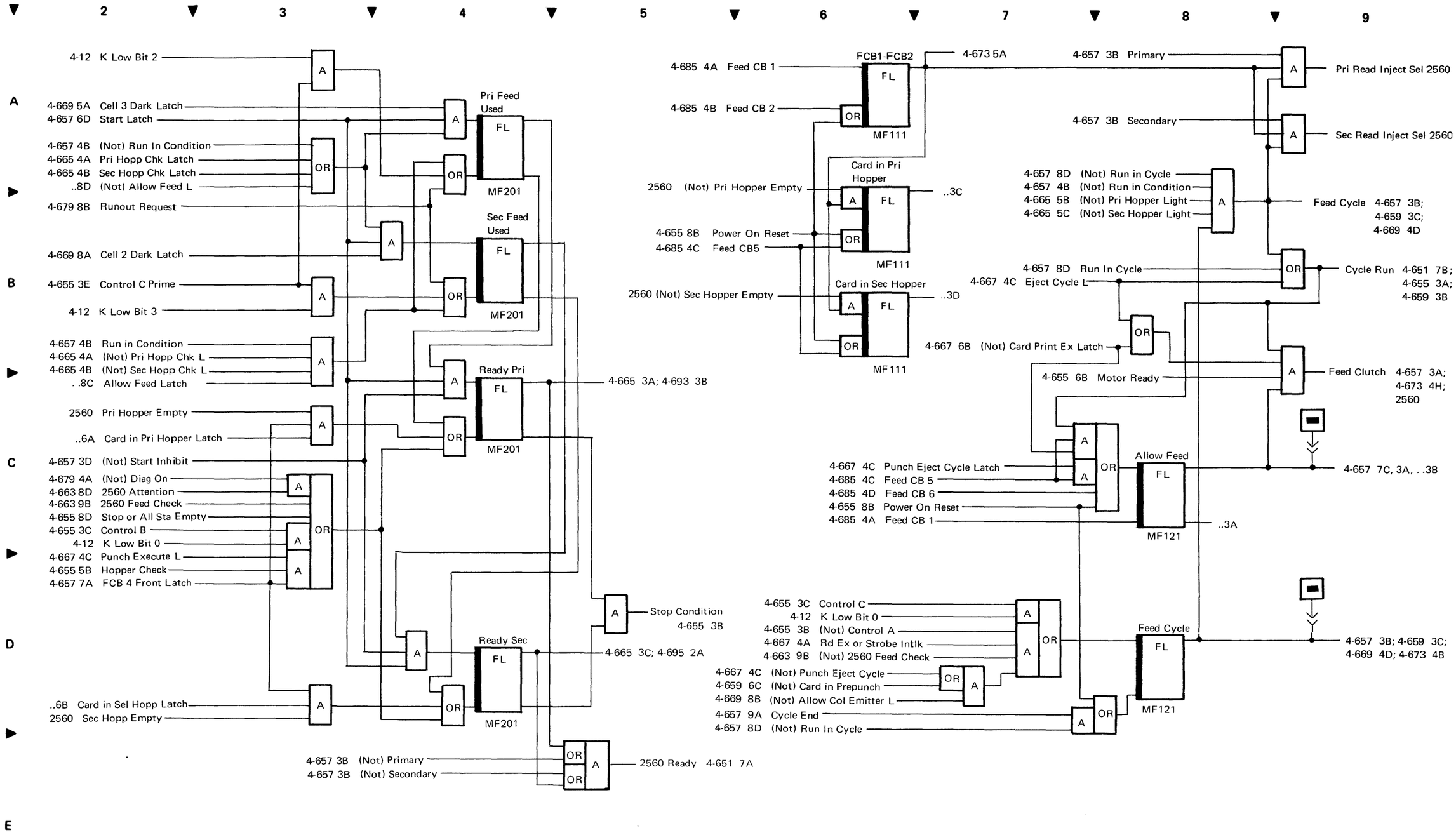
Form Y24-3529-0
FES Y24-0503

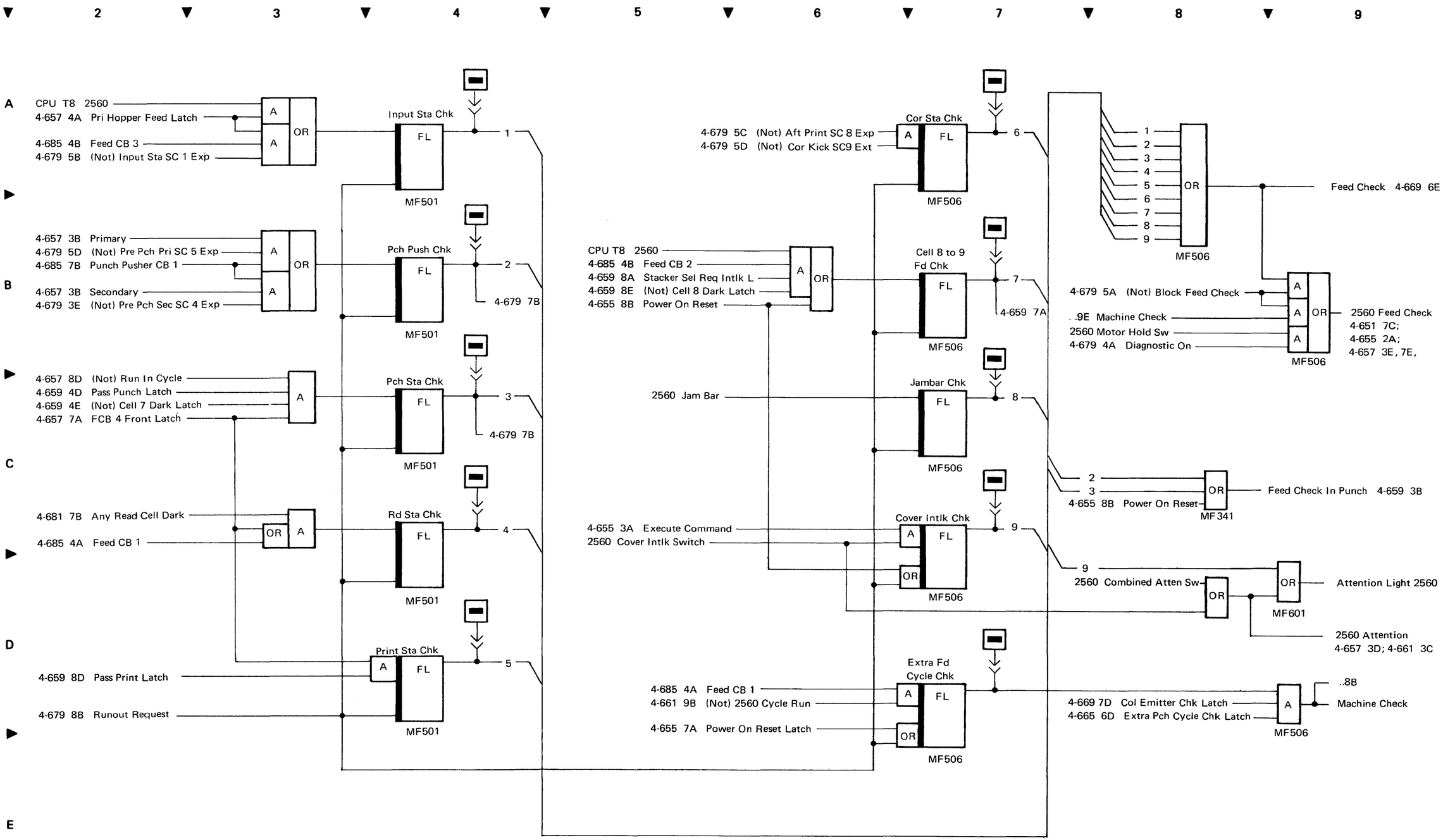




Form Y24-3329-0
FES Y24-0503

● Diagram 4-661. Ready Signals, Feed Control (2560)

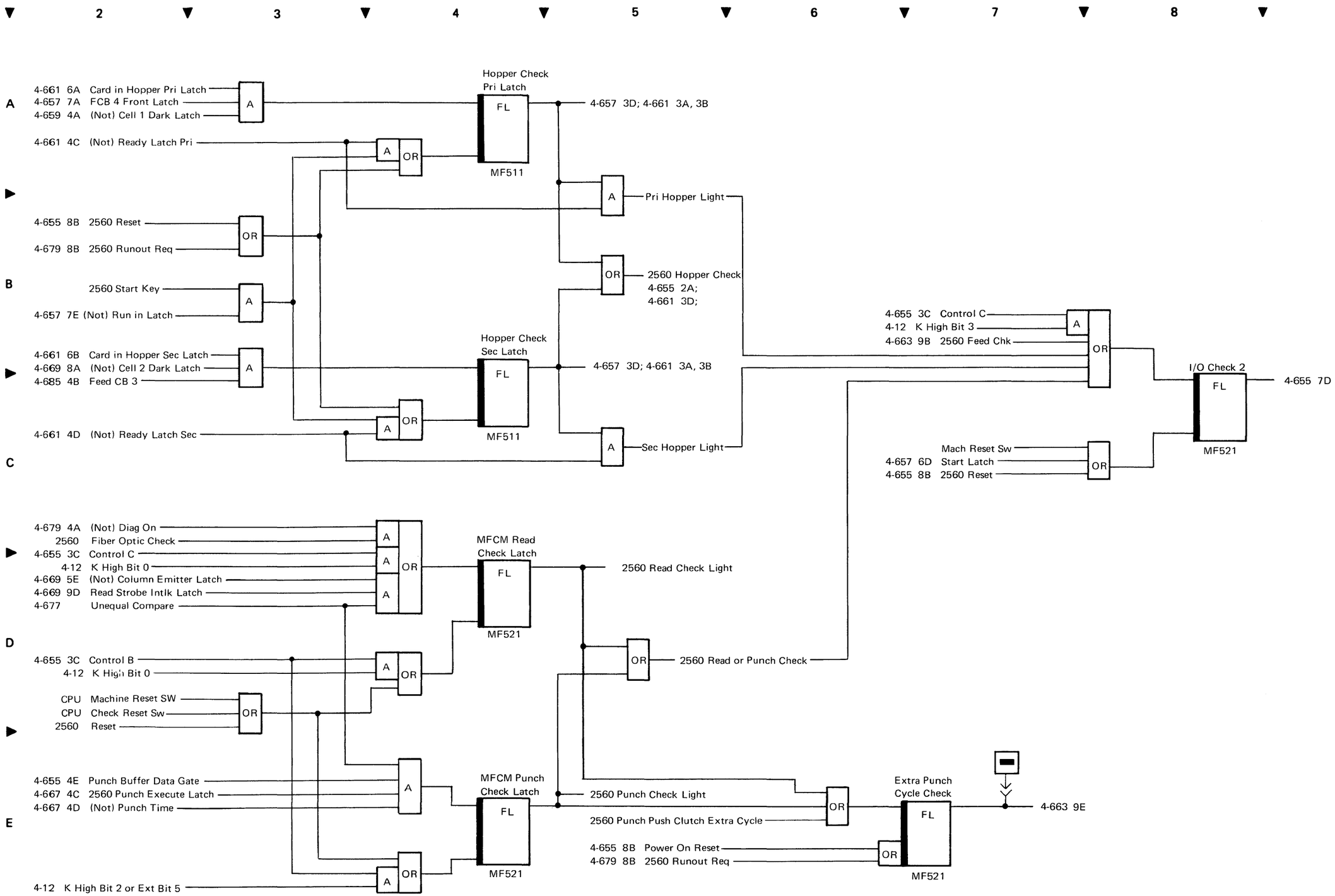


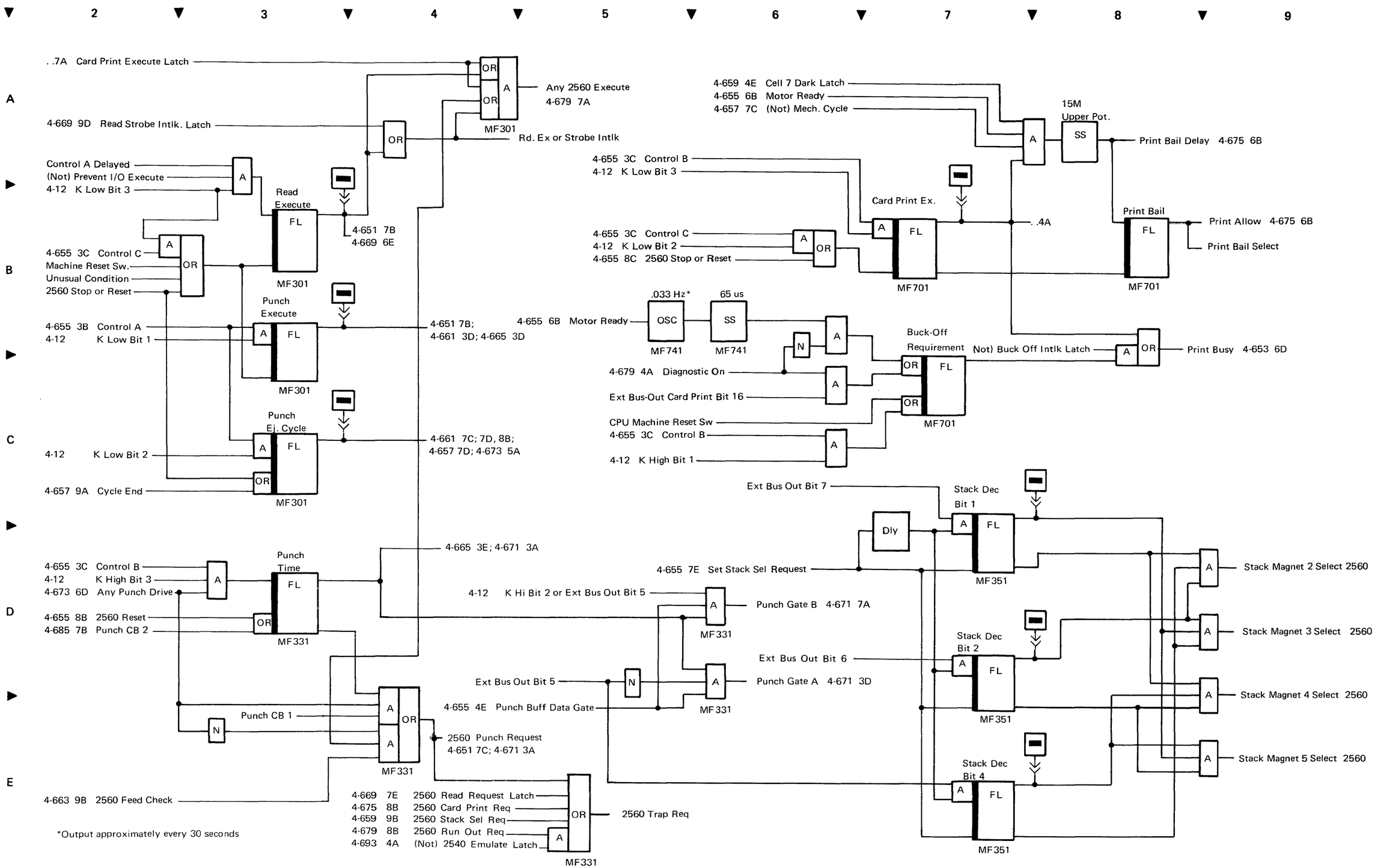


Form Y24-3529-0
FES Y24-0503

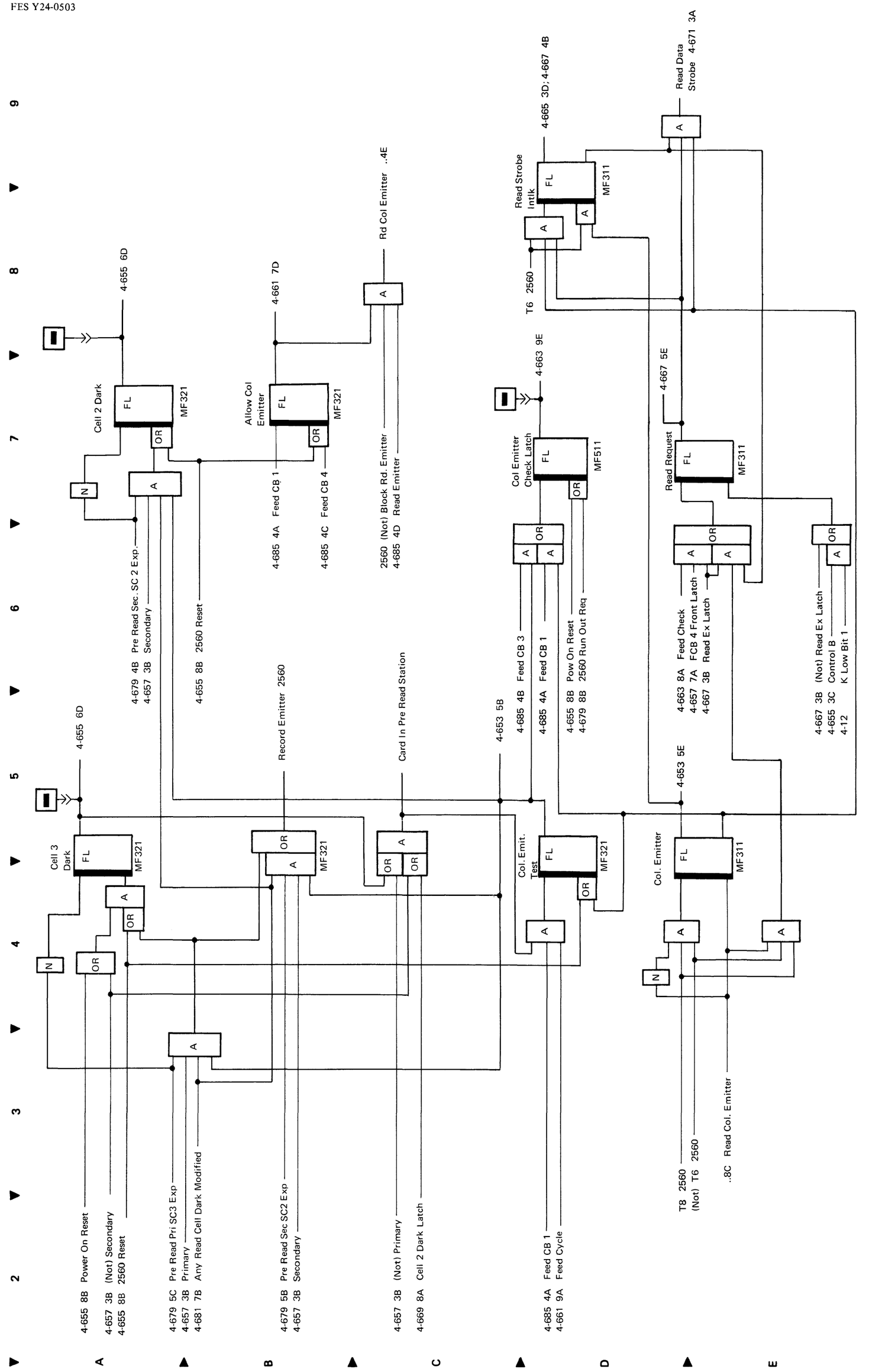
● Diagram 4-665. Check Latches

Form Y24-3529-0
FES Y24-0503

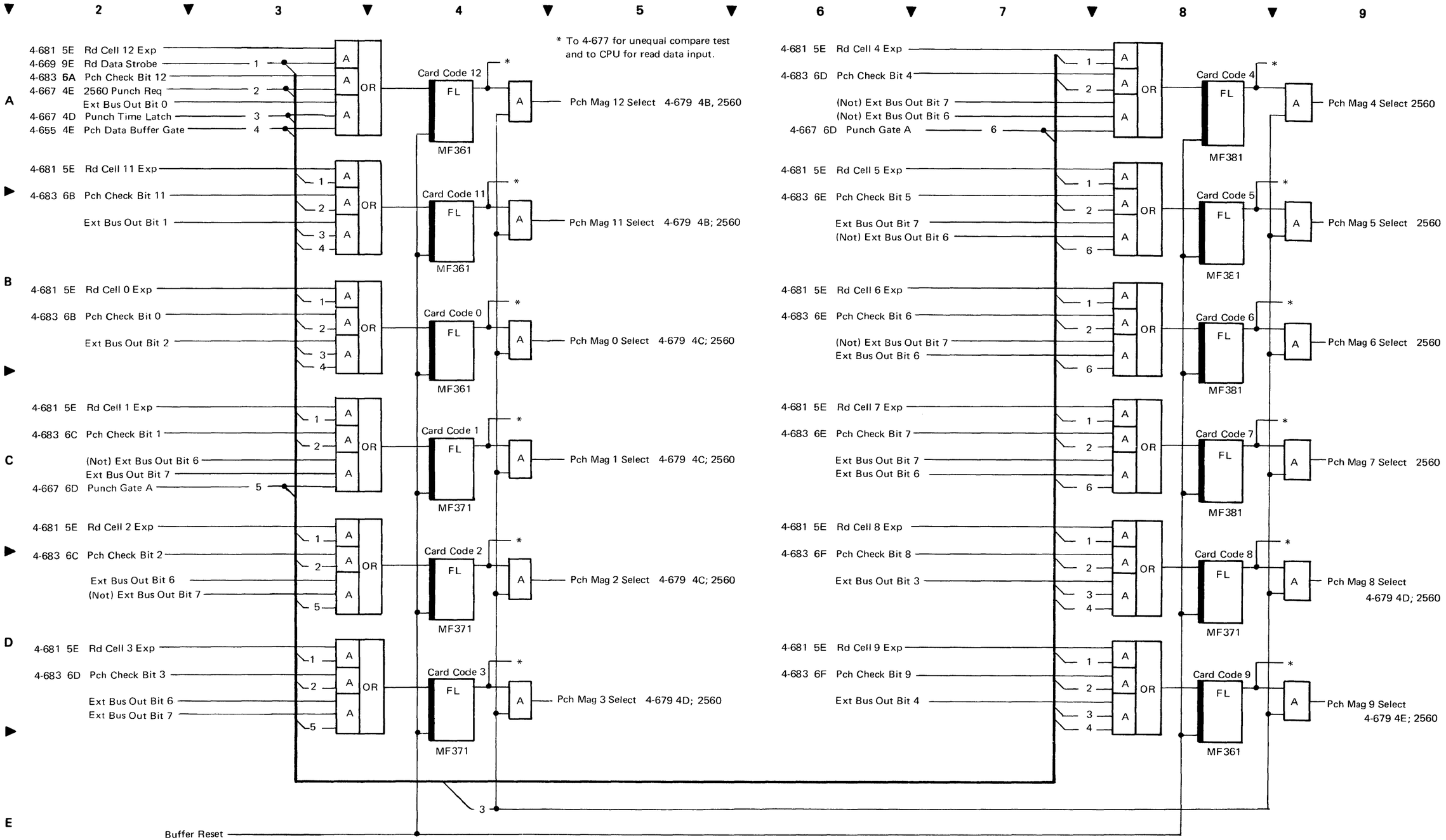




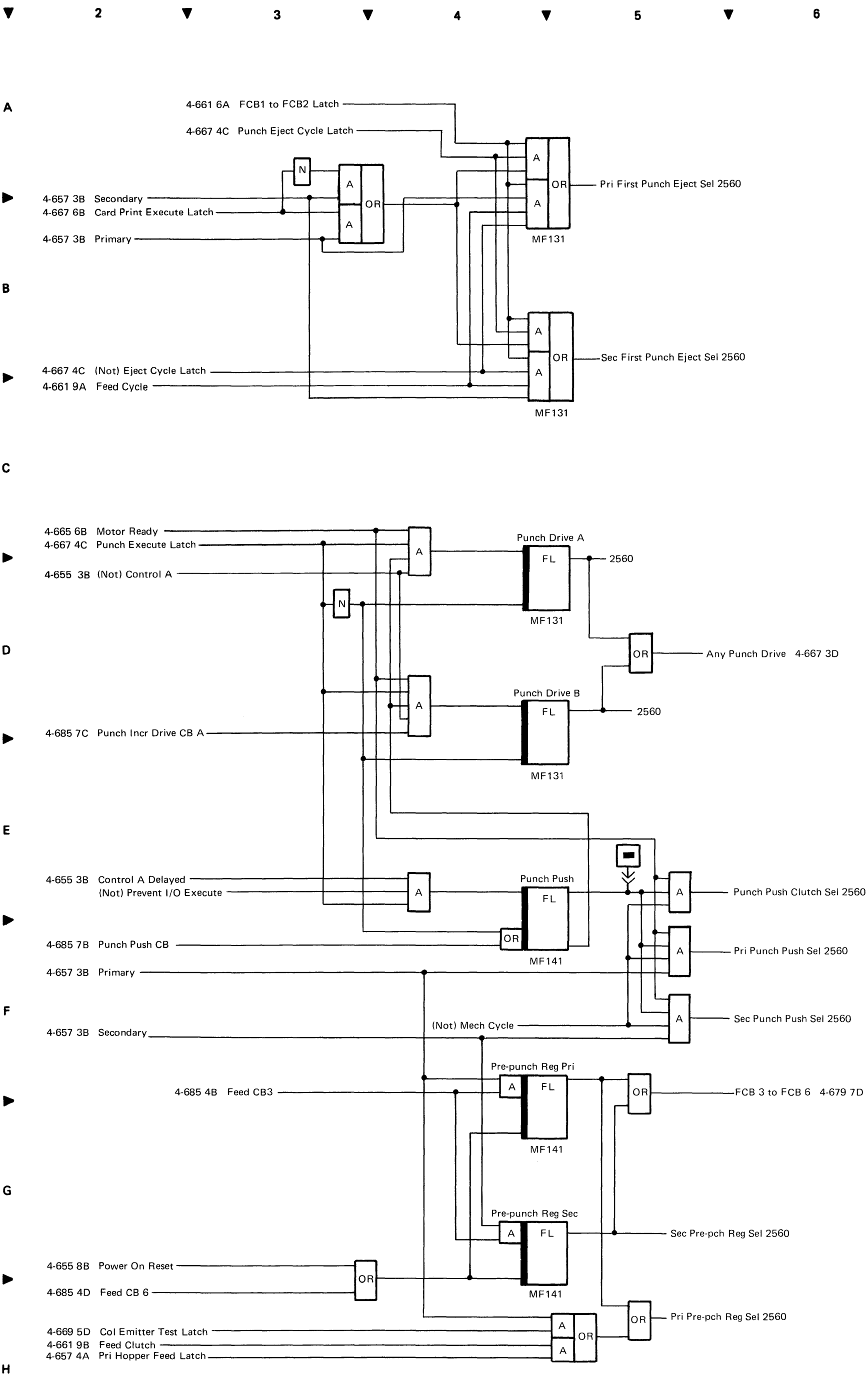
Form Y24-3529-0
FES Y24-0503



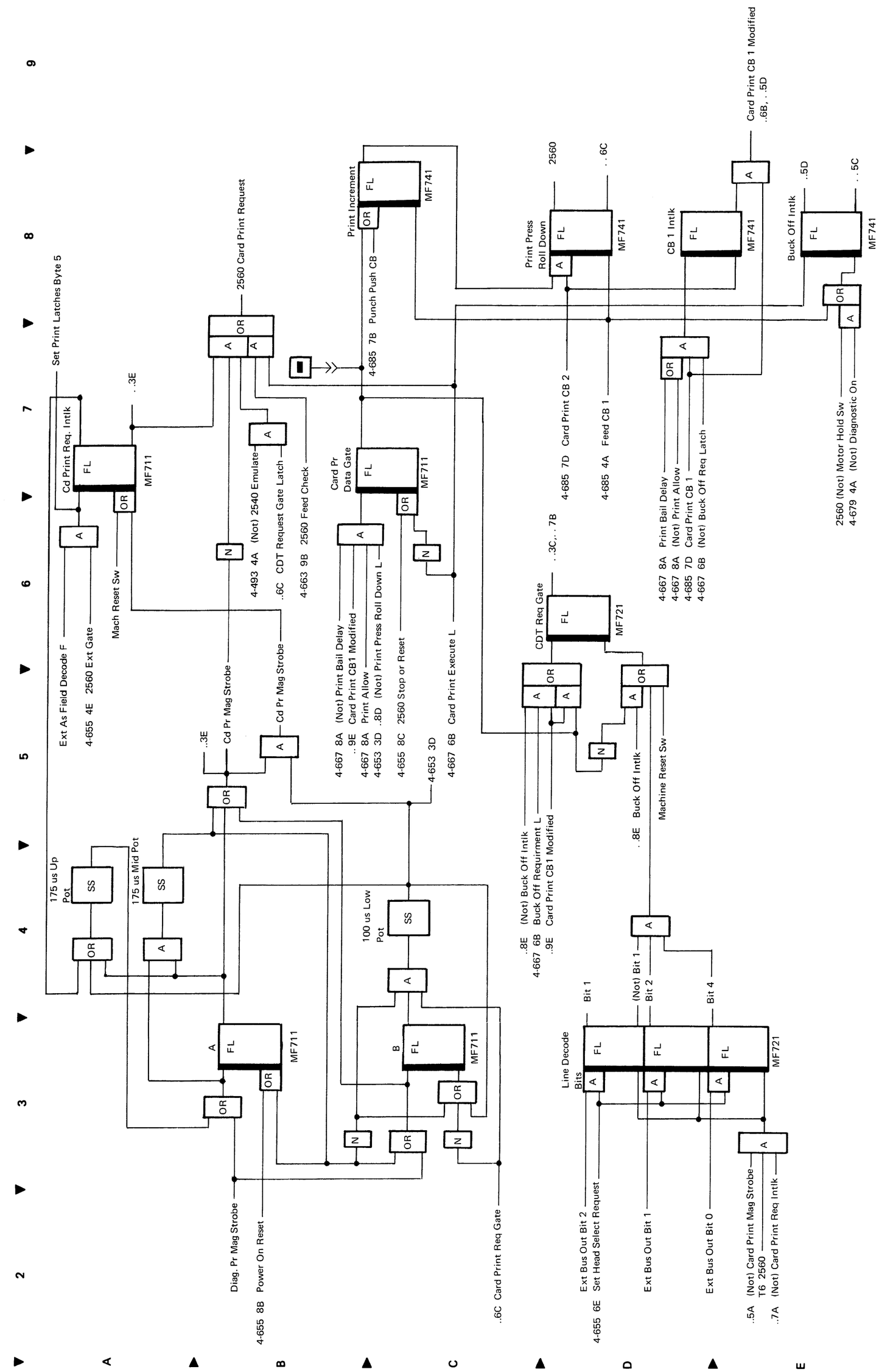
● Diagram 4-669. Read Request, Column Emitter, Read Strobe Interlock



Form Y24-3529-0
FES Y25-0503



● Diagram 4-673. Punch Feed and Drive Control, Punch Push Control (2560)



● Diagram 4-675. 2560 Card Print Control

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

A

Card Code Latch Set	Conditions for Satisfying Not Unequal Compare Read Cell Exp (or) Ext Bus-Out Bits		Result
12	12	0 =	Not Unequal Compare
11	11	1 =	
0	0	2 =	
1	1	7, not 5, not 6 =	
2	2	5, 6, not 7 =	
3	3	6, 7, not 5 =	
4	4	5, not 6, not 7 =	
5	5	5, 7, not 6 =	
6	6	5, 6, not 7 =	
7	7	5, 6, 7 =	
8	8	3 =	
9	9	4 =	

B

The Read and Punch Compare Check circuit tests for (1) the presence of the proper read cell exposed during a read cycle and (2) the presence of the proper external bus-out bits during a punch cycle. The table shows the conditions required to satisfy not unequal compare for each card code latch set. For example, when card code latch 12 is set, either read cell 12 exposed or external bus-out bit 0 must be present to produce the not unequal compare signal.

C

D

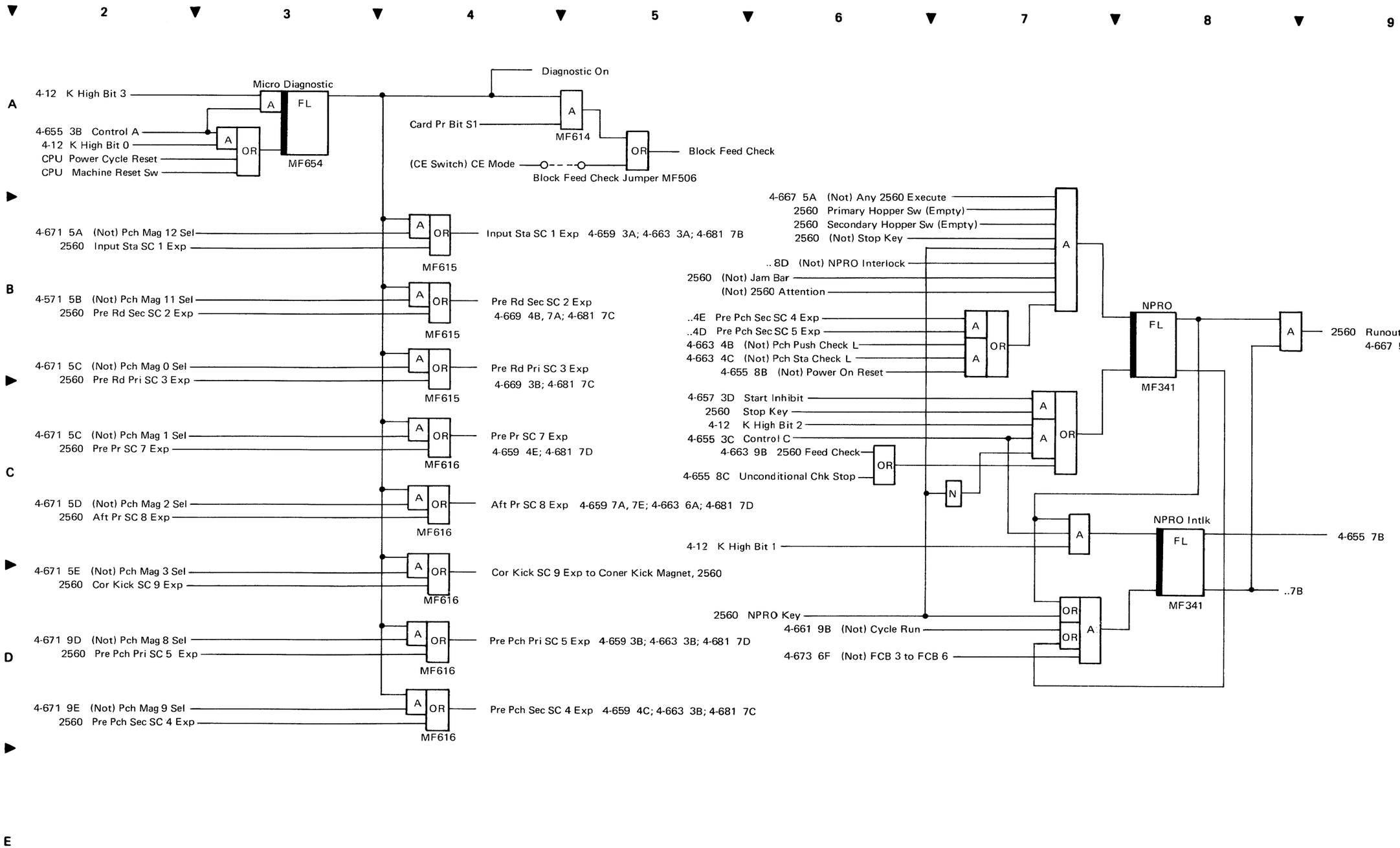
E

F

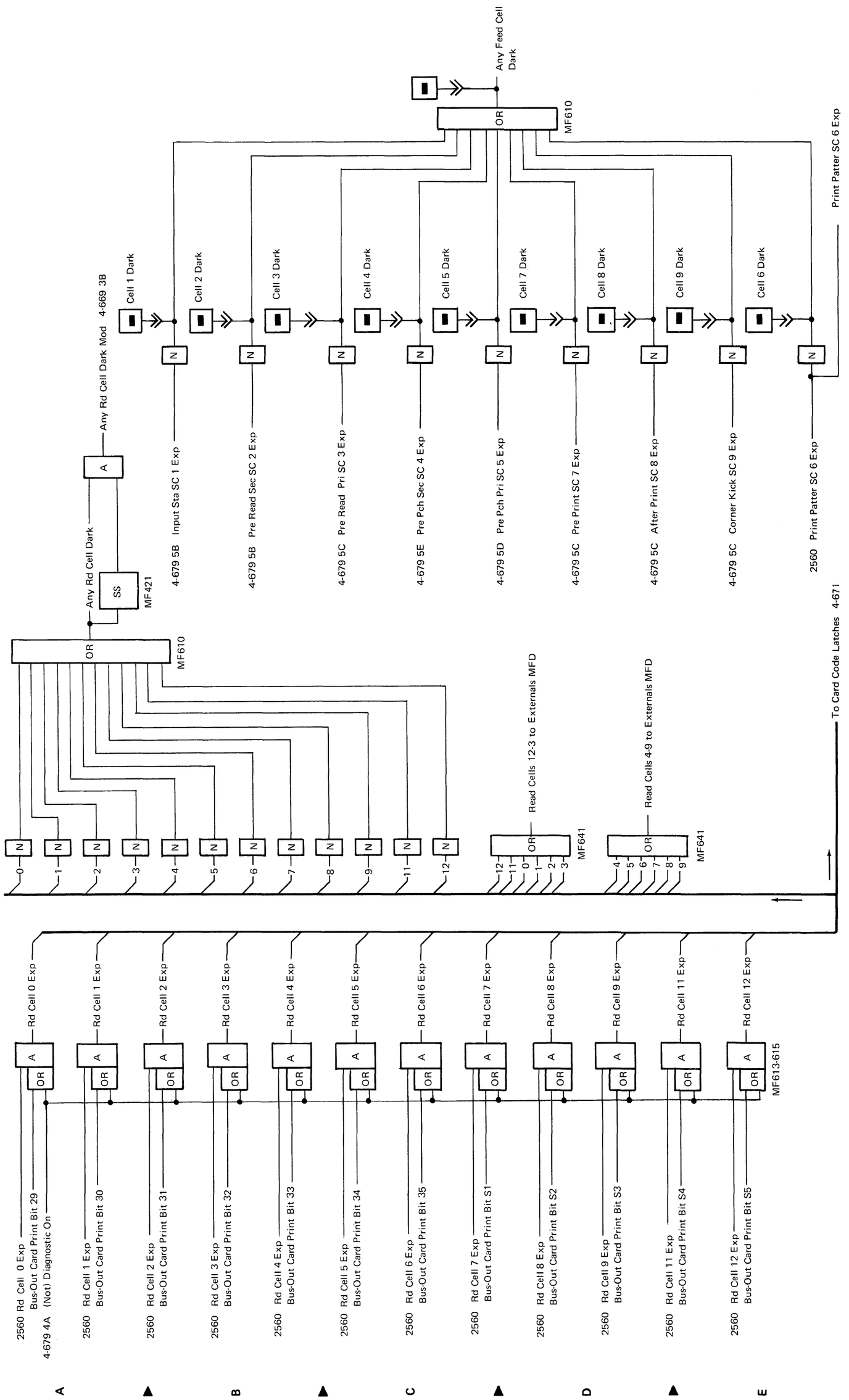
G

H

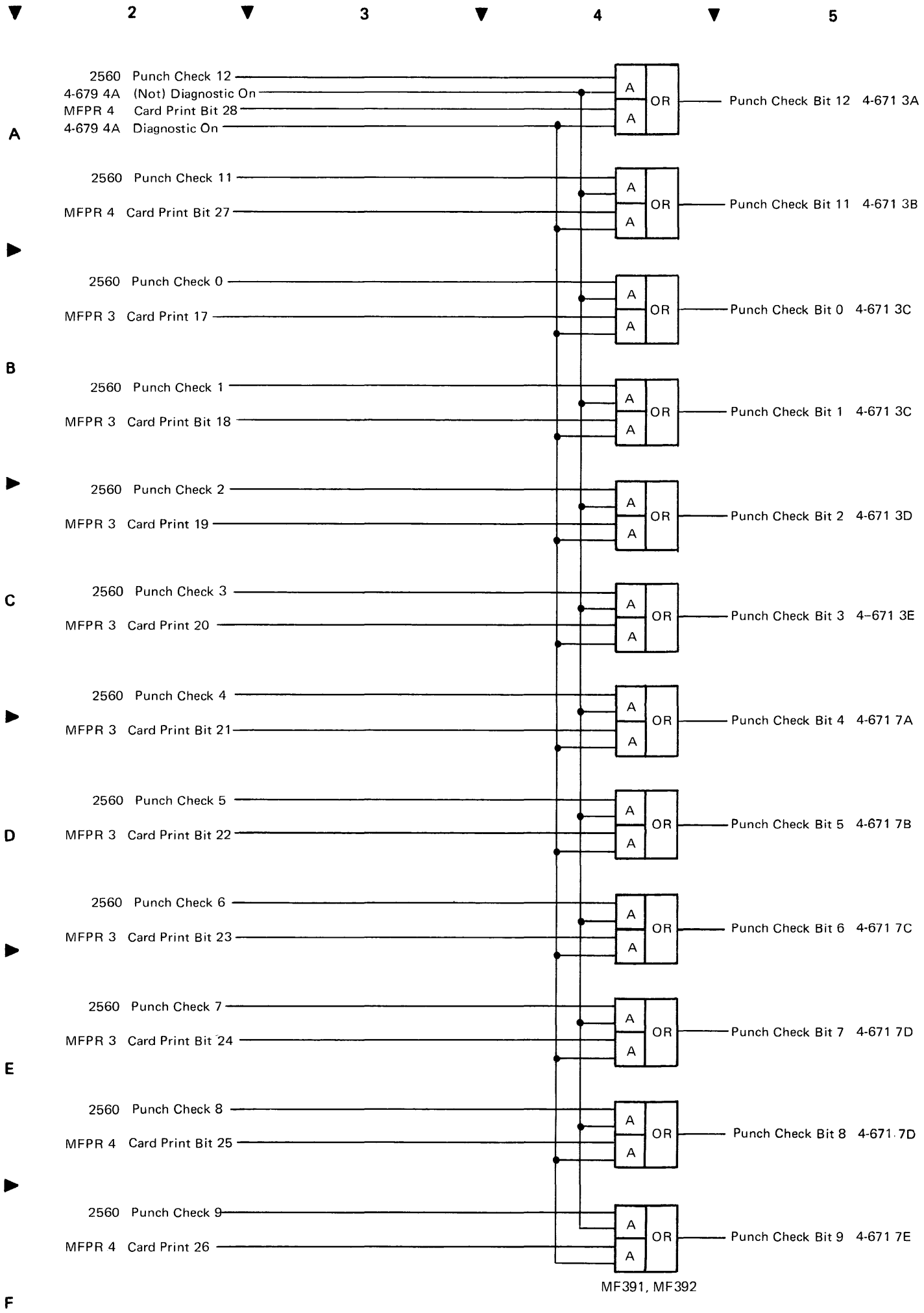
● Diagram 4-677. Read and Punch Compare Check



Form Y24-3529-0
FES Y24-0503



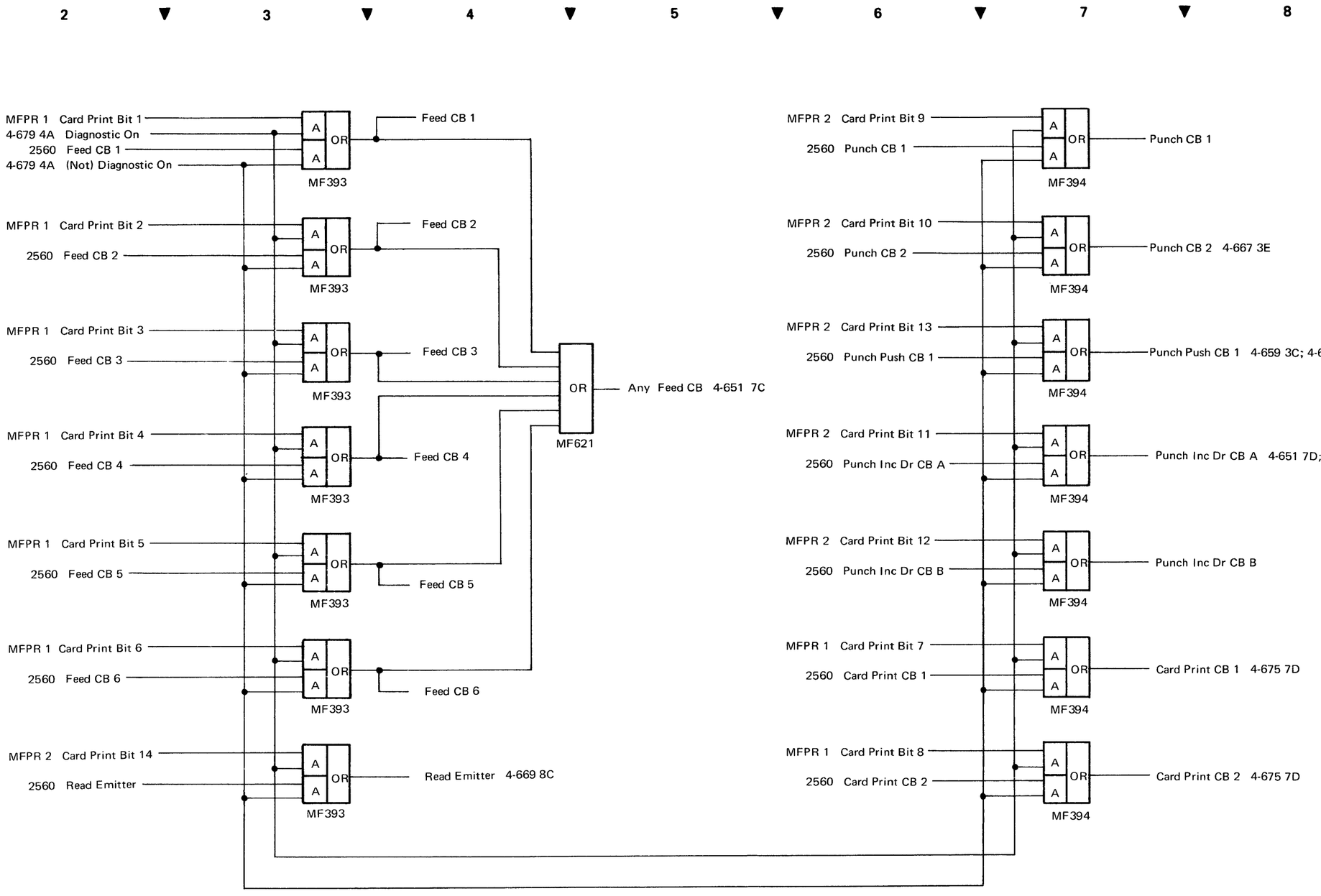
● Diagram 4-681. Read Solar Cells, Diagnostic SC Wrap, Any Feed or Read Cell Dark

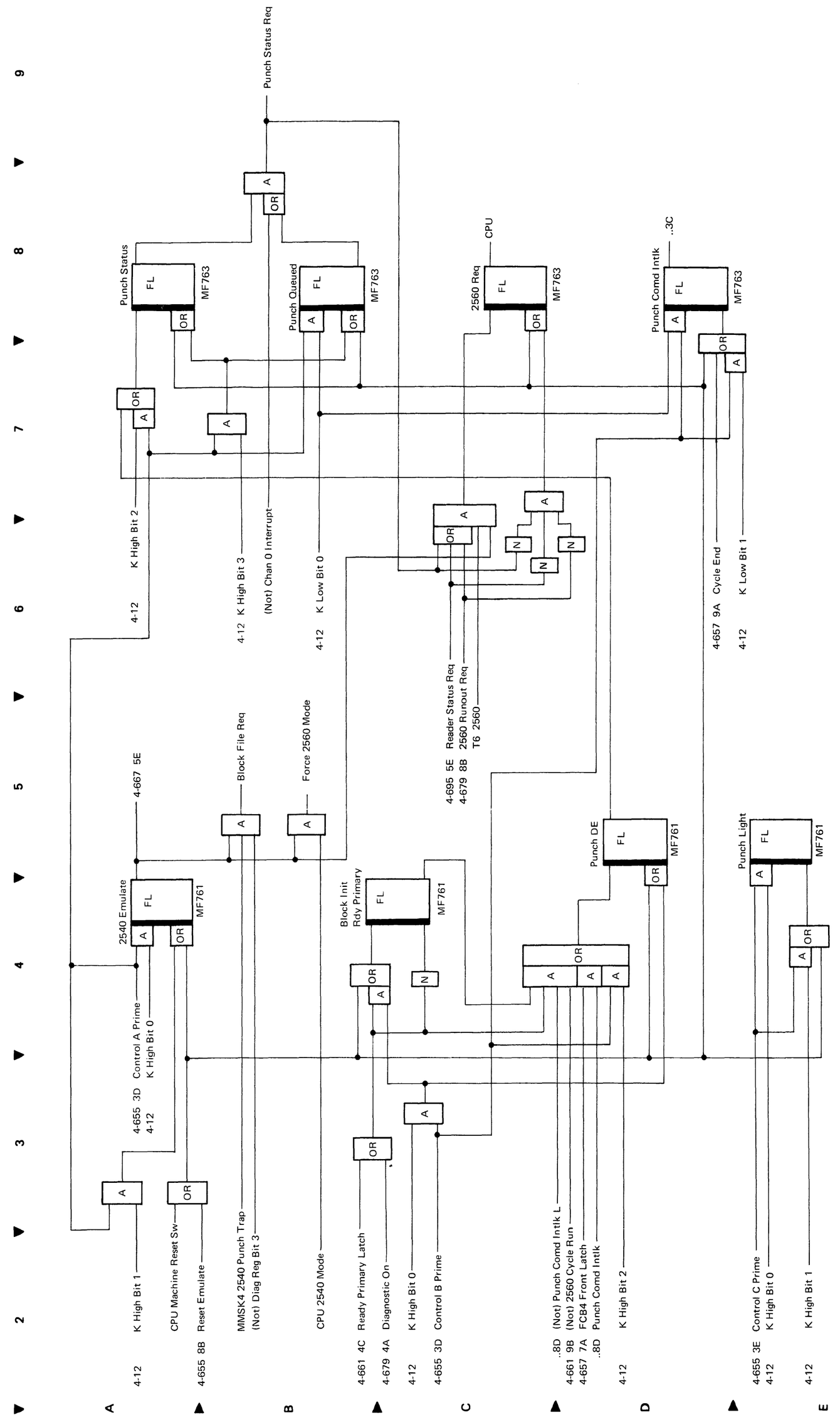


●Diagram 4-683. Punch Check and Diagnostic Gating

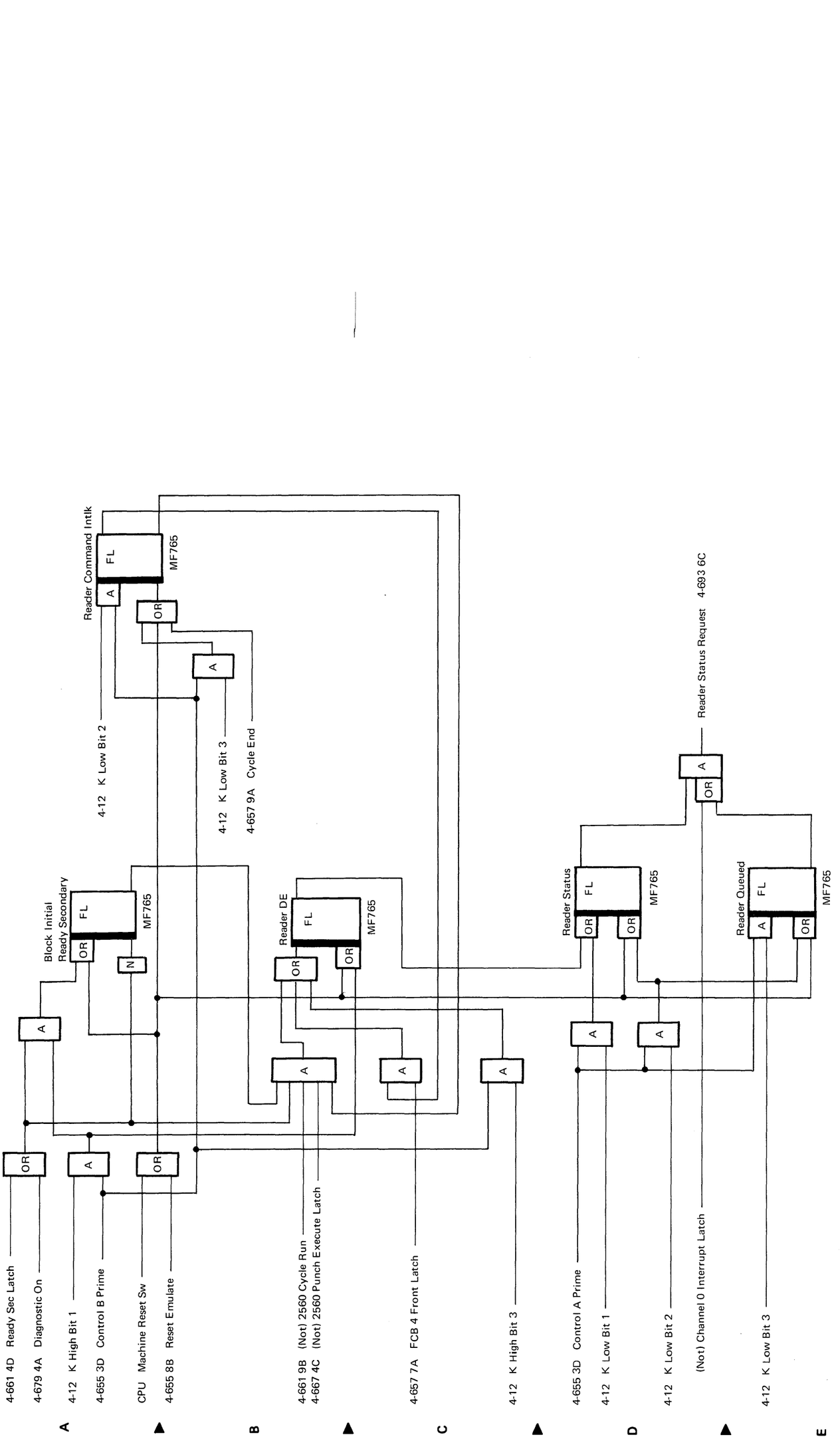
● Diagram 4-685. Entry and Diagnostic Gating

Form Y24-3529-0
FES Y24-0503





● Diagram 4-693. 2540 Emulation Control



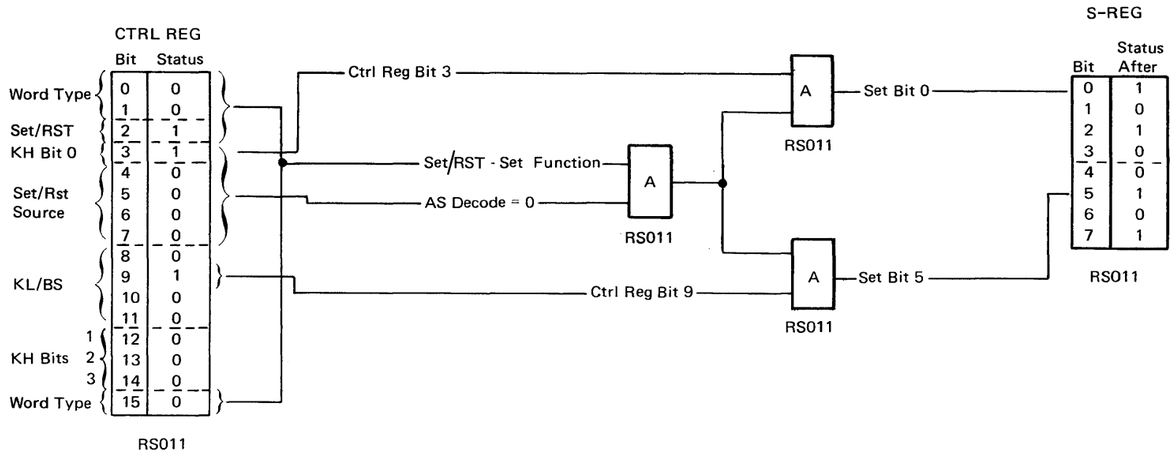
● Diagram 4-695. 2540 Emulation Control, Read

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

S-Reg Before

Bit	0	1	2	3	4	5	6	7
Status	0	0	1	0	0	0	0	1

A



B

C

EXAMPLE STATMENT

SET S K = 84

Objectives:

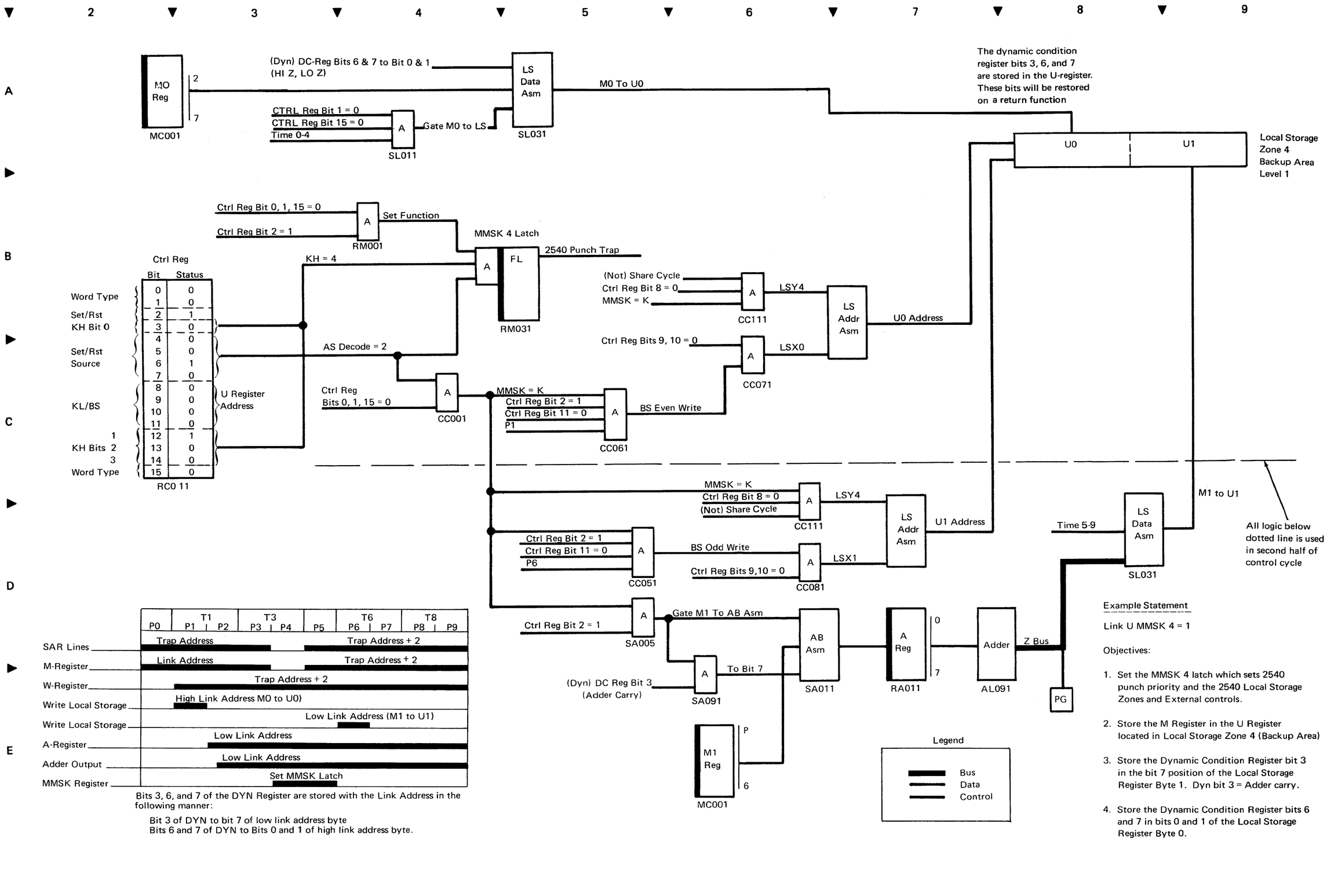
1. Set the bits in the S-Register that correspond to the bits of the K value of the Set/RST Word.
   The bits of the S-Register that are not addressed by bits of the K-Field, are not affected.

Note: Bits 1 and 2 of the S-Register cannot be set by the Set/RST Word, but may be reset by the Set/RST Word.

D

E

Diagram 5-2. Set Reset Word Link Function (Word Type 0)



Bits 3, 6, and 7 of the DYN Register are stored with the Link Address in the following manner:

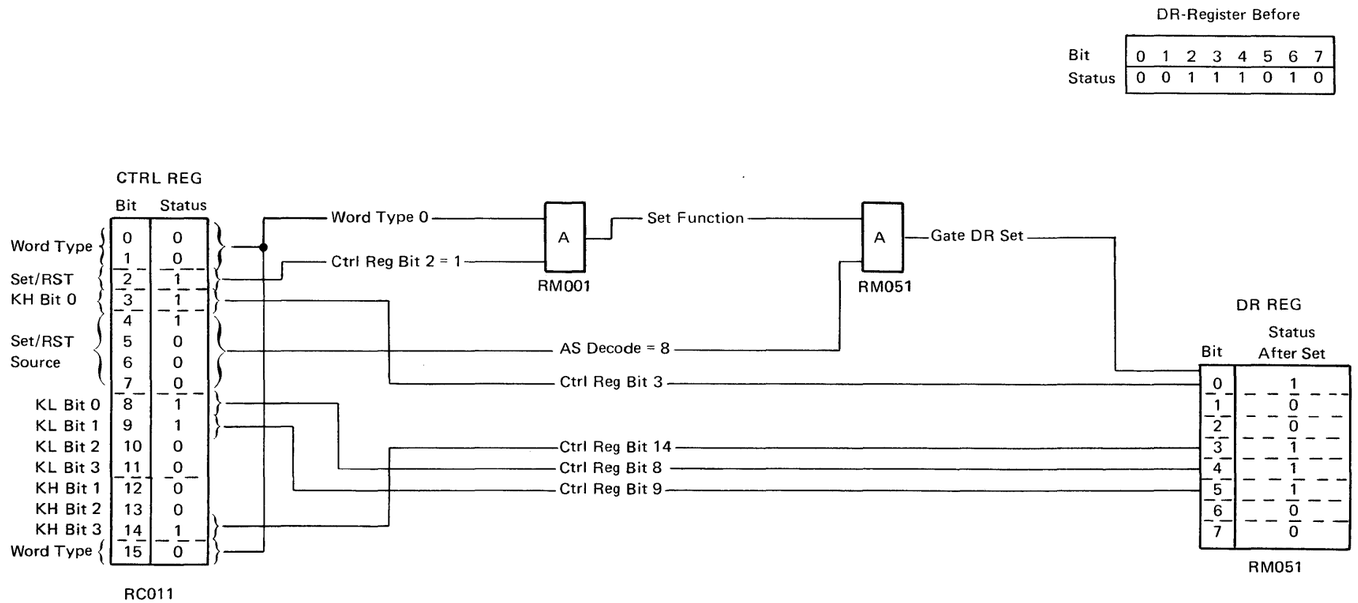
Bit 3 of DYN to bit 7 of low link address byte
Bits 6 and 7 of DYN to Bits 0 and 1 of high link address byte.

Example Statement

Link U MMSK 4 = 1

Objectives:

1. Set the MMSK 4 latch which sets 2540 punch priority and the 2540 Local Storage Zones and External controls.
2. Store the M Register in the U Register located in Local Storage Zone 4 (Backup Area)
3. Store the Dynamic Condition Register bit 3 in the bit 7 position of the Local Storage Register Byte 1. Dyn bit 3 = Adder carry.
4. Store the Dynamic Condition Register bits 6 and 7 in bits 0 and 1 of the Local Storage Register Byte 0.



Example Statement

As Seen in Microlistings

Set DR K = 9C

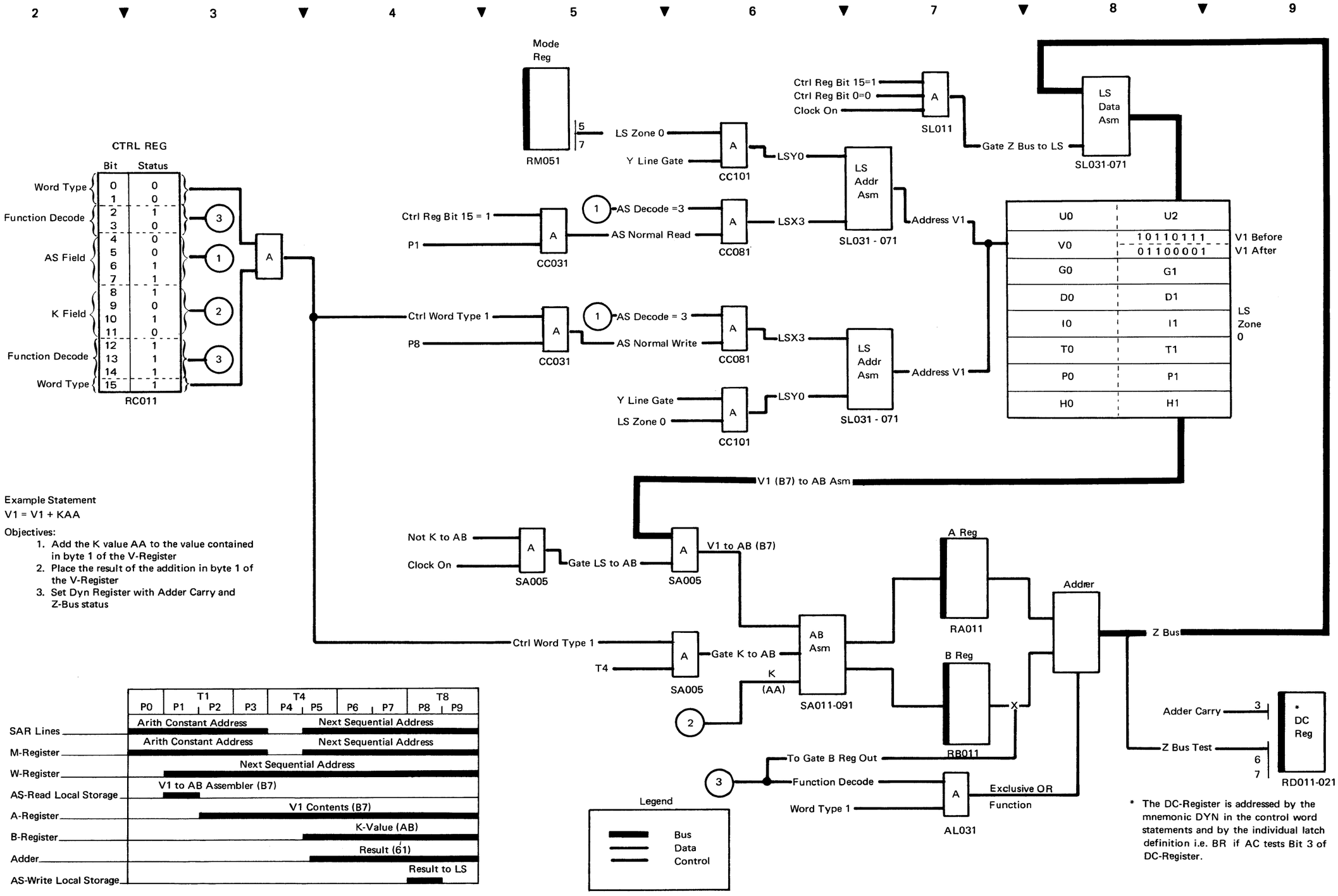
Objectives:

1. Set the DR Register to the K value of the Set/RST Word.

   Note: The bits of the DR Register that are not addressed by bits of the K field, are reset.

The DR (Diagnostic Register) is set to the value represented in the K field of the Set/RST Word.

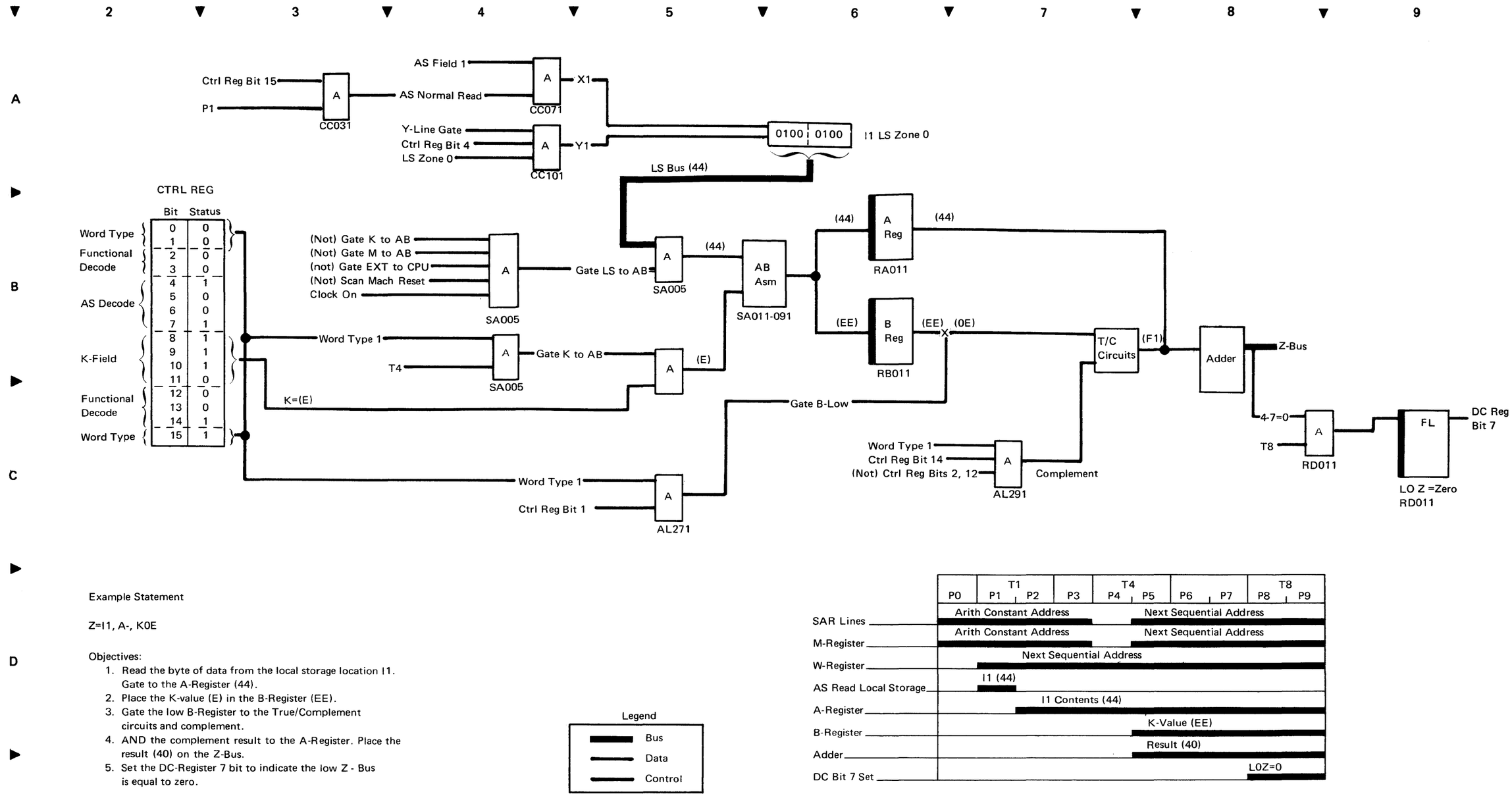
Diagram 5-4. Arith Constant Word (Word Type 1)



Example Statement
V1 = V1 + KAA

Objectives:
1. Add the K value AA to the value contained in byte 1 of the V-Register
2. Place the result of the addition in byte 1 of the V-Register
3. Set Dyn Register with Adder Carry and Z-Bus status

* The DC-Register is addressed by the mnemonic DYN in the control word statements and by the individual latch definition i.e. BR if AC tests Bit 3 of DC-Register.



Example Statement

Z=I1, A-, K0E

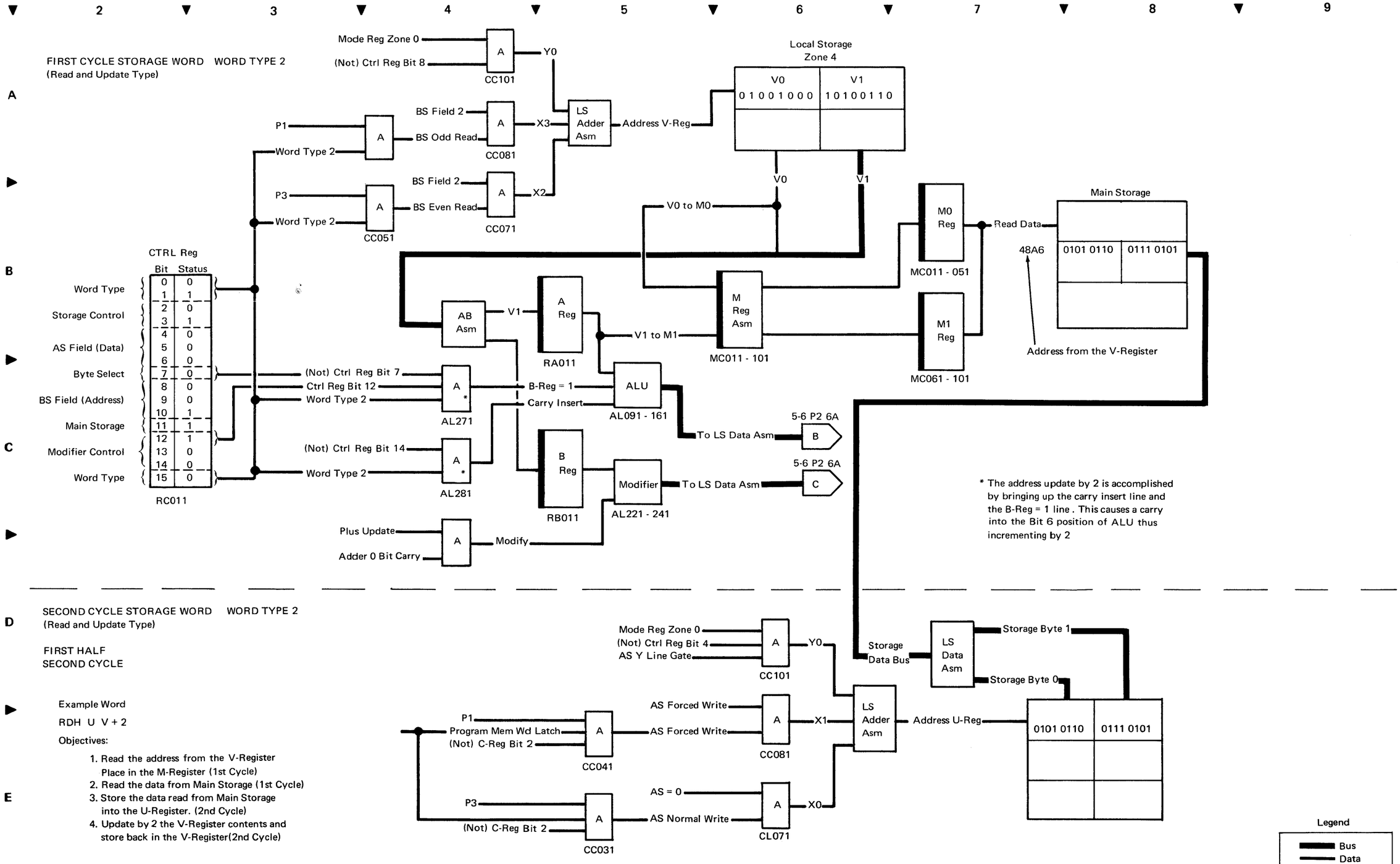
Objectives:

1. Read the byte of data from the local storage location I1. Gate to the A-Register (44).
2. Place the K-value (E) in the B-Register (EE).
3. Gate the low B-Register to the True/Complement circuits and complement.
4. AND the complement result to the A-Register. Place the result (40) on the Z-Bus.
5. Set the DC-Register 7 bit to indicate the low Z - Bus is equal to zero.

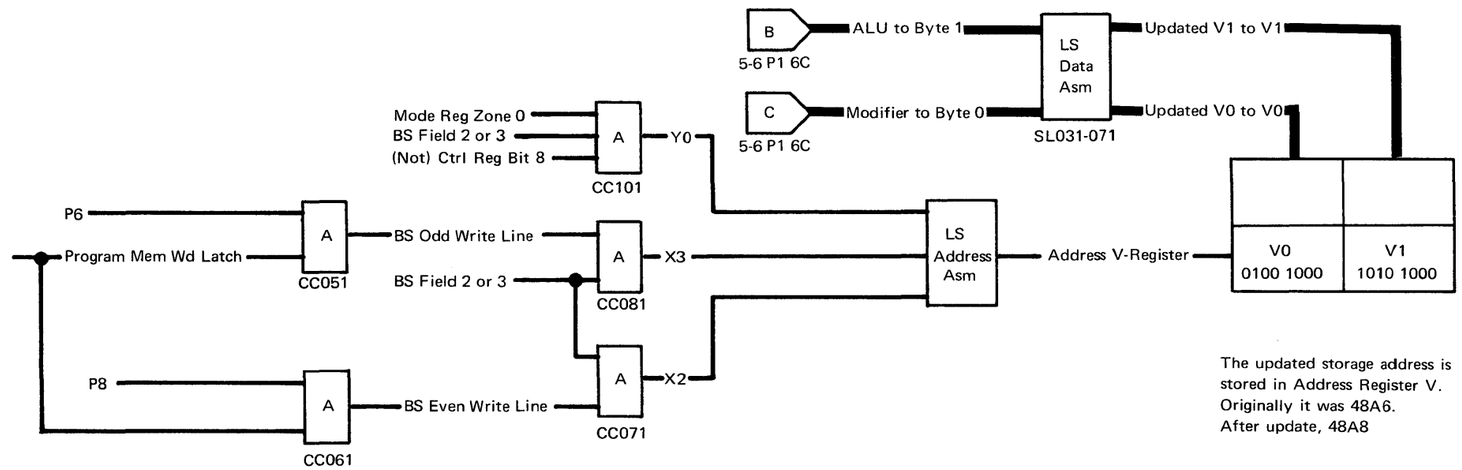
Legend

- Bus
- Data
- Control

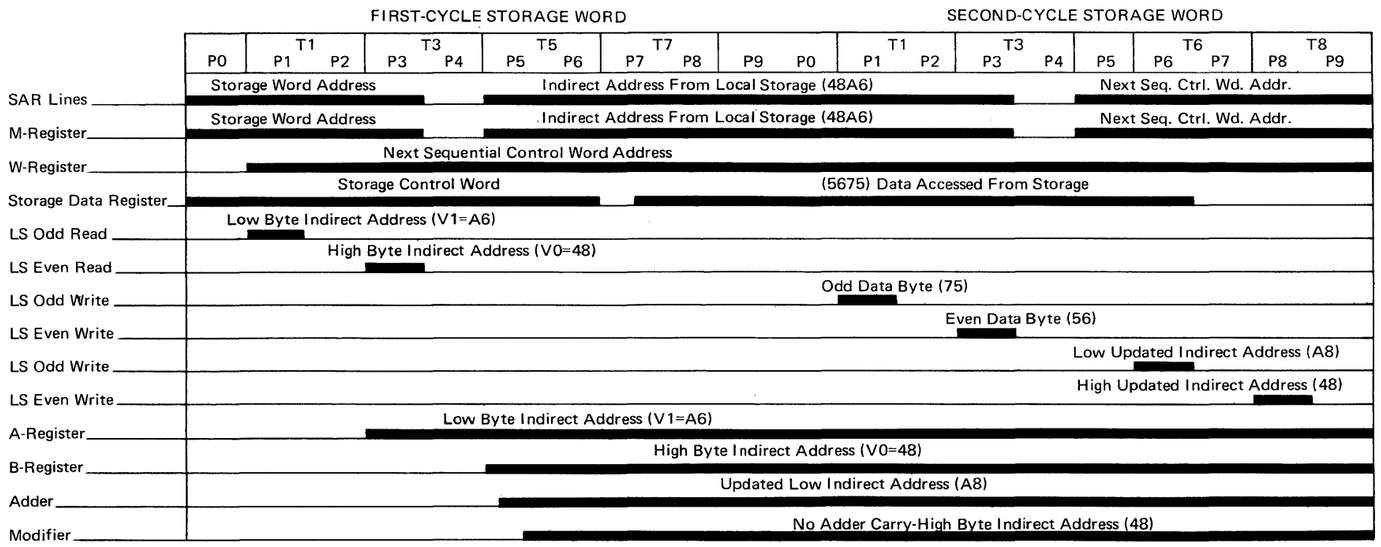
Diagram 5-6. First Cycle Storage Word (Word Type 2) (Part 1 of 2)



SECOND HALF
SECOND CYCLE



The updated storage address is stored in Address Register V.
Originally it was 48A6.
After update, 48A8



Legend
- Bus
- Data
- Control

Diagram 5-6. Second Cycle Storage Word (Word Type 2) (Part 2 of 2)

Diagram 5-7. Storage Word (Double Byte Modify) Word Type 2

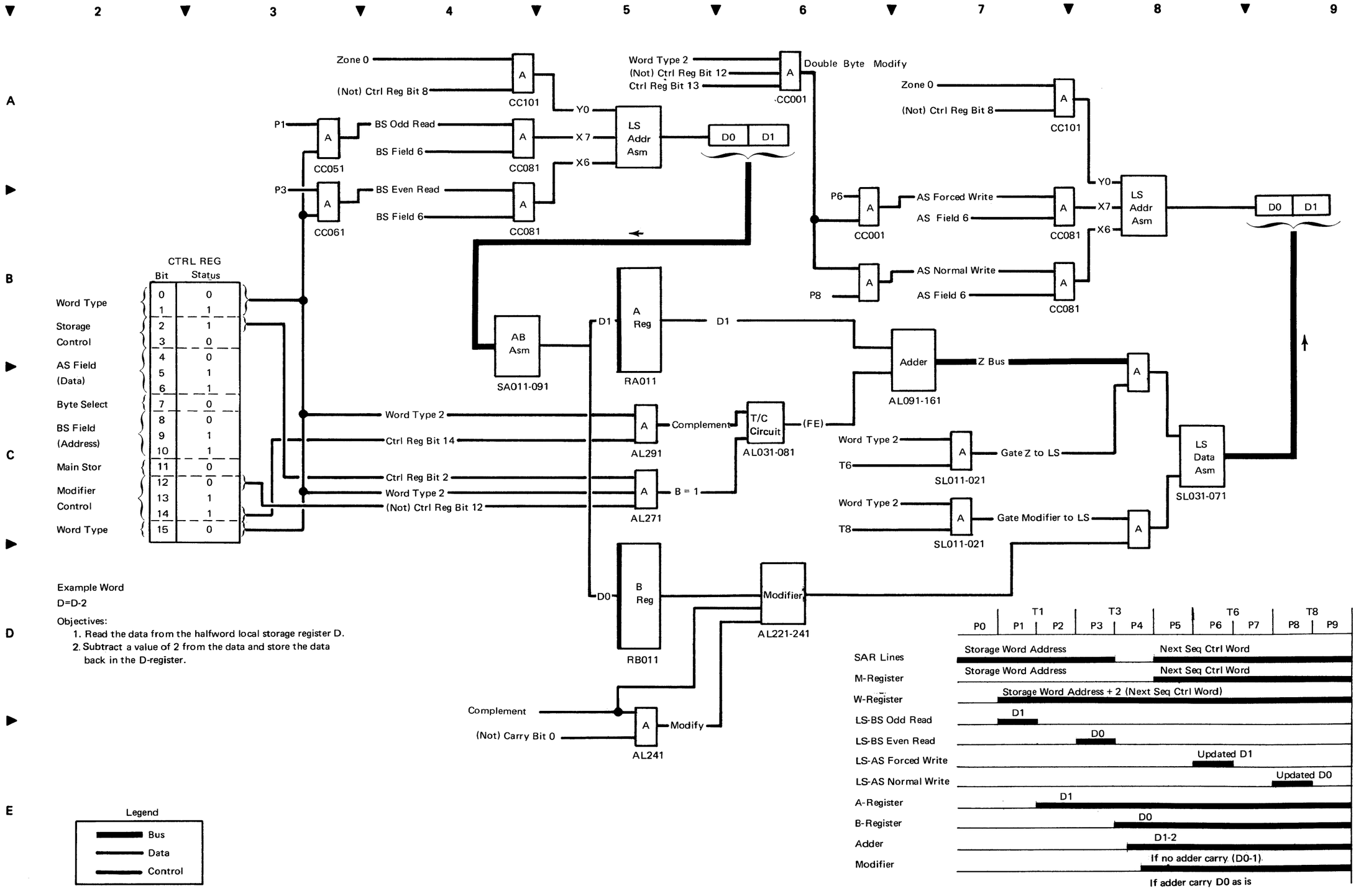
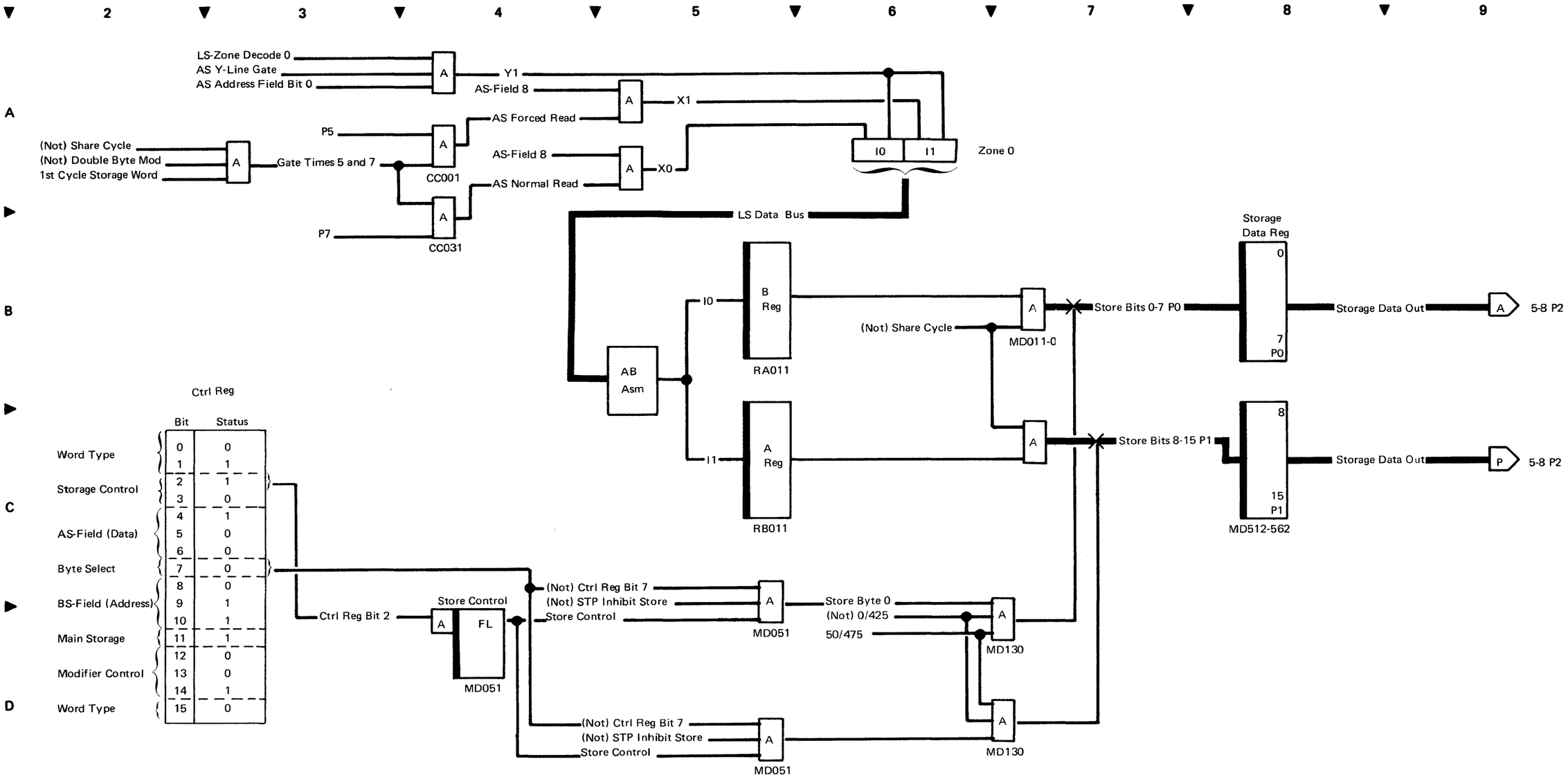
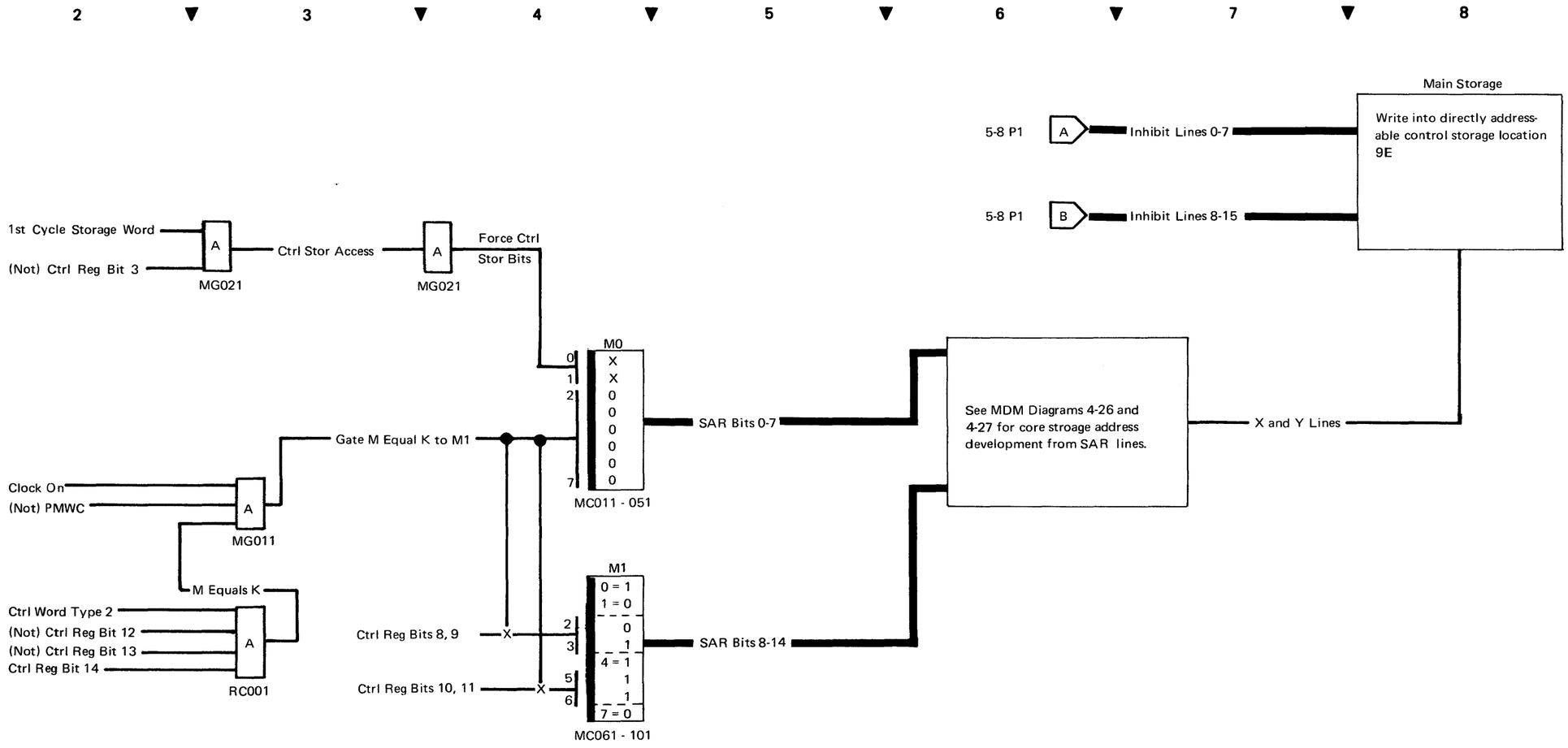


Diagram 5-8. Direct Addressable Control Storage, Storage Word Type 2 (Part 1 of 2)

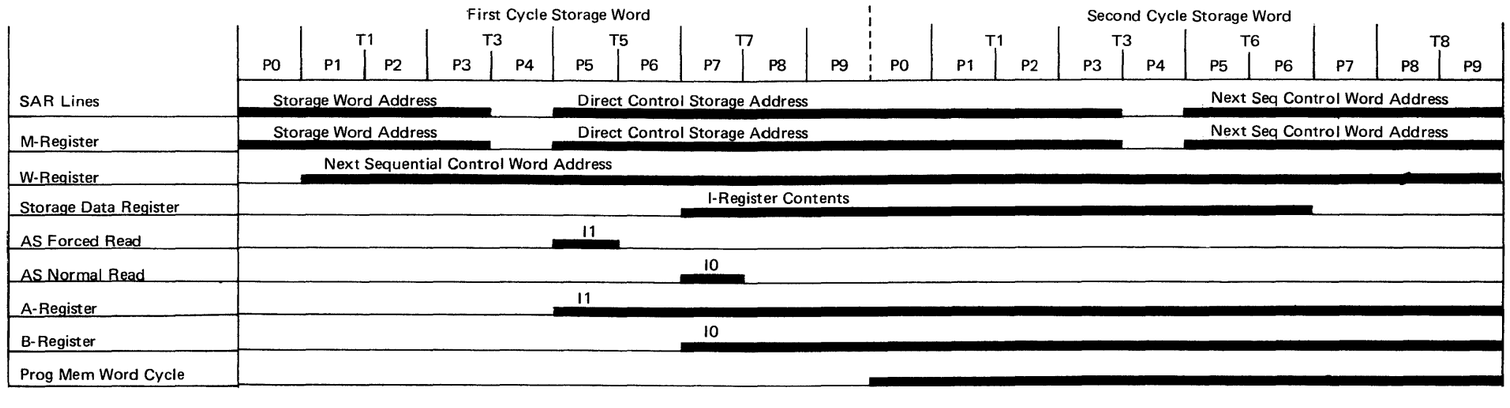




Bits 0 and 1 of M0 are set according to storage size:

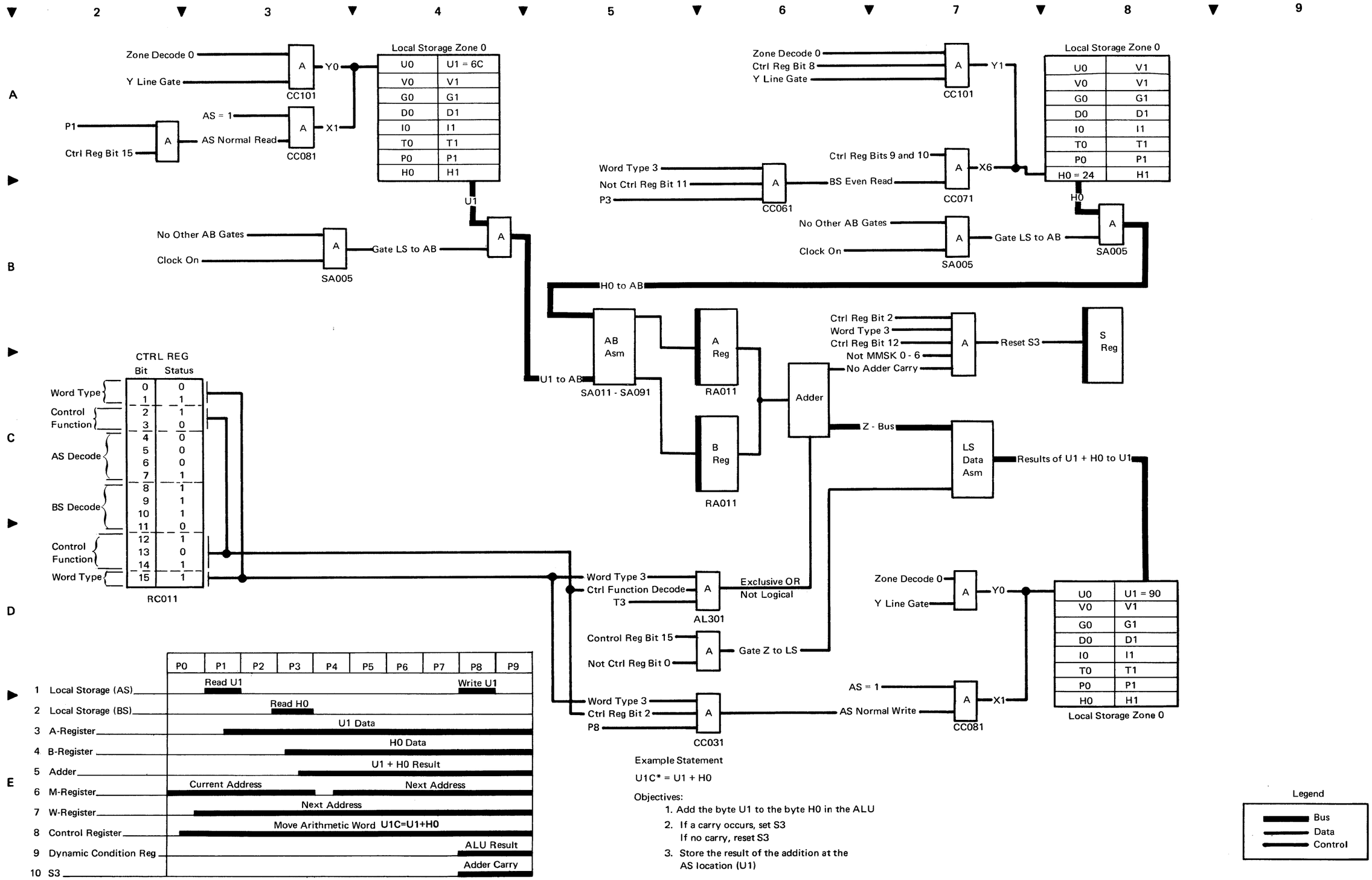
Core Size	Bits 01
16K	01
24K	10
32K	10
48K	11

Bits 0 and 4 of M1 are forced to 1.
Bits 1 and 7 of M1 are forced to 0.
Bits 2, 3, 5, and 6 are set by Ctrl Reg Bits 8, 9, 10, and 11 respectively.



Refer to MDM Diagram 4-27 for write timing into core storage.

Diagram 5-9 Move/Arithmetic Word (Word Type 3)



2 3 4 5 6 7 8 9

A

B

C

D

E

Switches

F C

A B

Sw A (Bits 0-3) Sw B (Bits 0-3)

The switch values will be set into both the A- and B-Registers, but only the B-Register will be gated through the Adder.

Ctrl Reg

	Bit	Status
Word Type	0	0
	1	1
Functional Decode	2	0
	3	1
AS Decode	4	0
	5	0
	6	0
	7	0
BS Decode	8	1
	9	1
	10	0
	11	0
Functional Decode	12	1
	13	1
	14	1
Word Type	15	1

RC011

Word Type 3
Ctrl Reg Bit 3
Ctrl Reg Bit 12
A
SA005
Gate External to AB

CPU Mode
AS Decode 0
A
SA007
Gate Sw AB to AB

A
AB Asm
SA011

A Reg
RA011
Blocked
B Reg
RA011

Adder
Z Bus
A
LS Data Asm
SL031

(Not) Ctrl Reg Bit 0
Ctrl Reg Bit 15
Clock On
A
SL011
Gate Z Bus to LS

Word Type 3
(Not) Ctrl Bits 2, 11
P8
A
CC061

BS Even Write
(Not) Ctrl Reg Bit 10
Ctrl Reg Bit 9
A
CC081
LS Addr X4

0 1 2 3 4 5 6 7
1 1 1 1 1 1 0 0
P0 LS Zone 0

Ctrl Reg Bit 8
LS Zone Decode 0
A
CC101
LS Addr Y1

Example Statement

P0 = SWAB

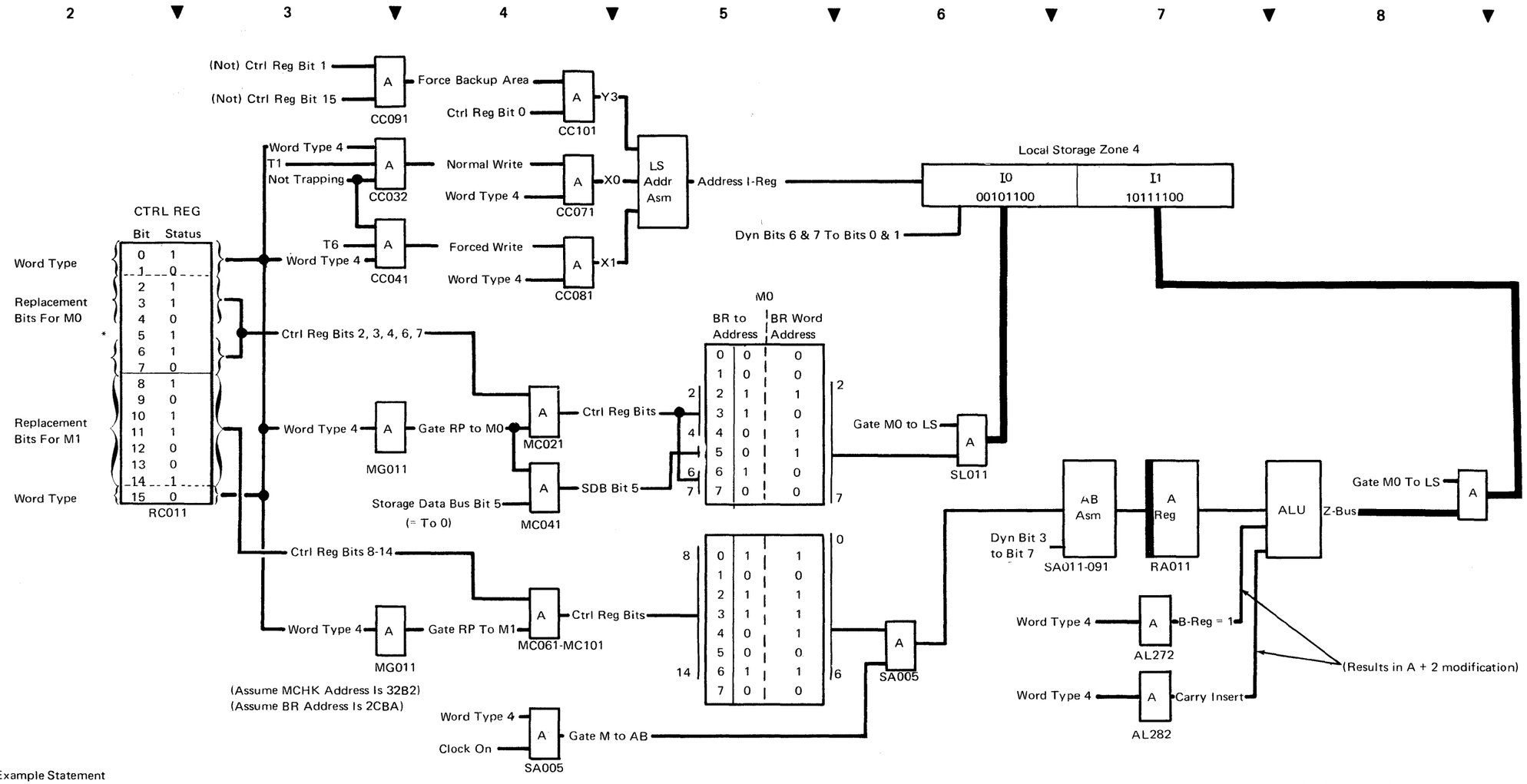
Objectives:

1. Move the Switch A and B values to the Local Storage Register P0. The hexidecimal value decoded from Switch A will be placed in the high 4 bits of P0. The hexidecimal value decoded from Switch B will be placed in the low 4 bits of P0.

Legend

Bus
Data
Control

Diagram 5-11. Unconditional Branch Word (Word Type 4)



D

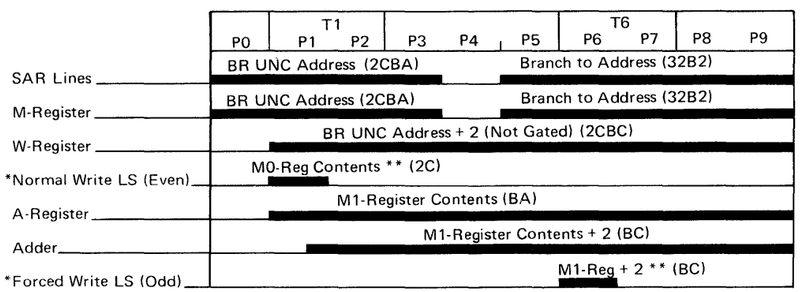
Example Statement

Next Address	Statement
MCHK	BR

Objective:

1. Replace the designated M0 and M1 Bits with the replacement bits from the BR control word. The address of the BR word will be incremented by 2 and stored in the I-Register backup area (Zone 4). There is no bit distinction between a BAL (Branch and Link) and a BR word

* Ctrl Reg Bit 5 is set to a 1 for this word, as it is for a BR conditional and branch mask word. The storage data bus bit 5 is used as the replacement bit 5 for the M0 register.



* The address of the next sequential control word following the branch unconditional word is stored in the I-Register of local storage zone 4. This is done whether the word is designated BR or BAL on the microlisting.

** DYN-Register Bits 6 and 7 are stored in Bits 0, 1 of I0 at P1 time. DYN-Register Bit 3 is stored in Bit 7 of I1 at P6 time.

E

Legend

Bus
Data
Control

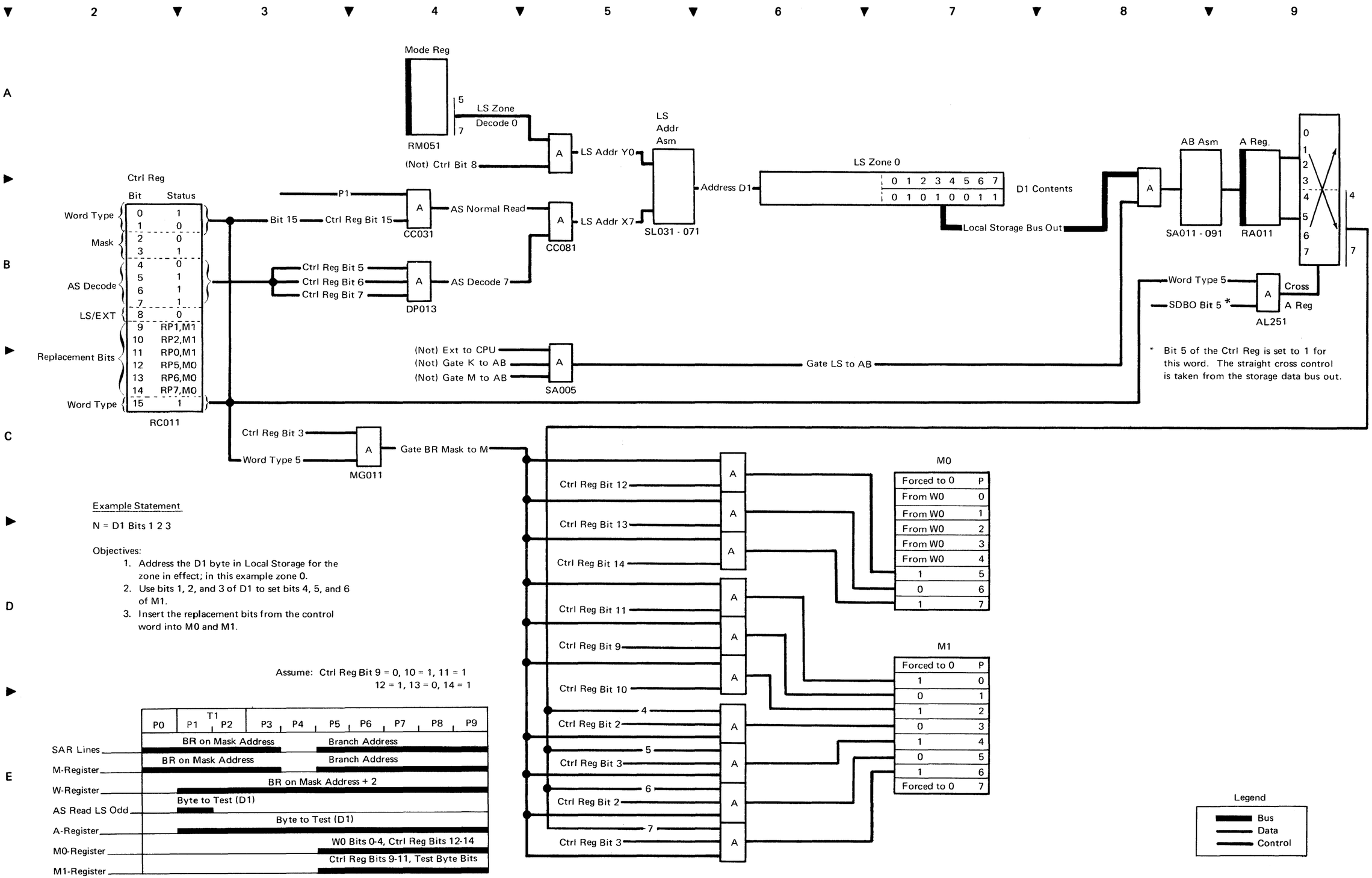
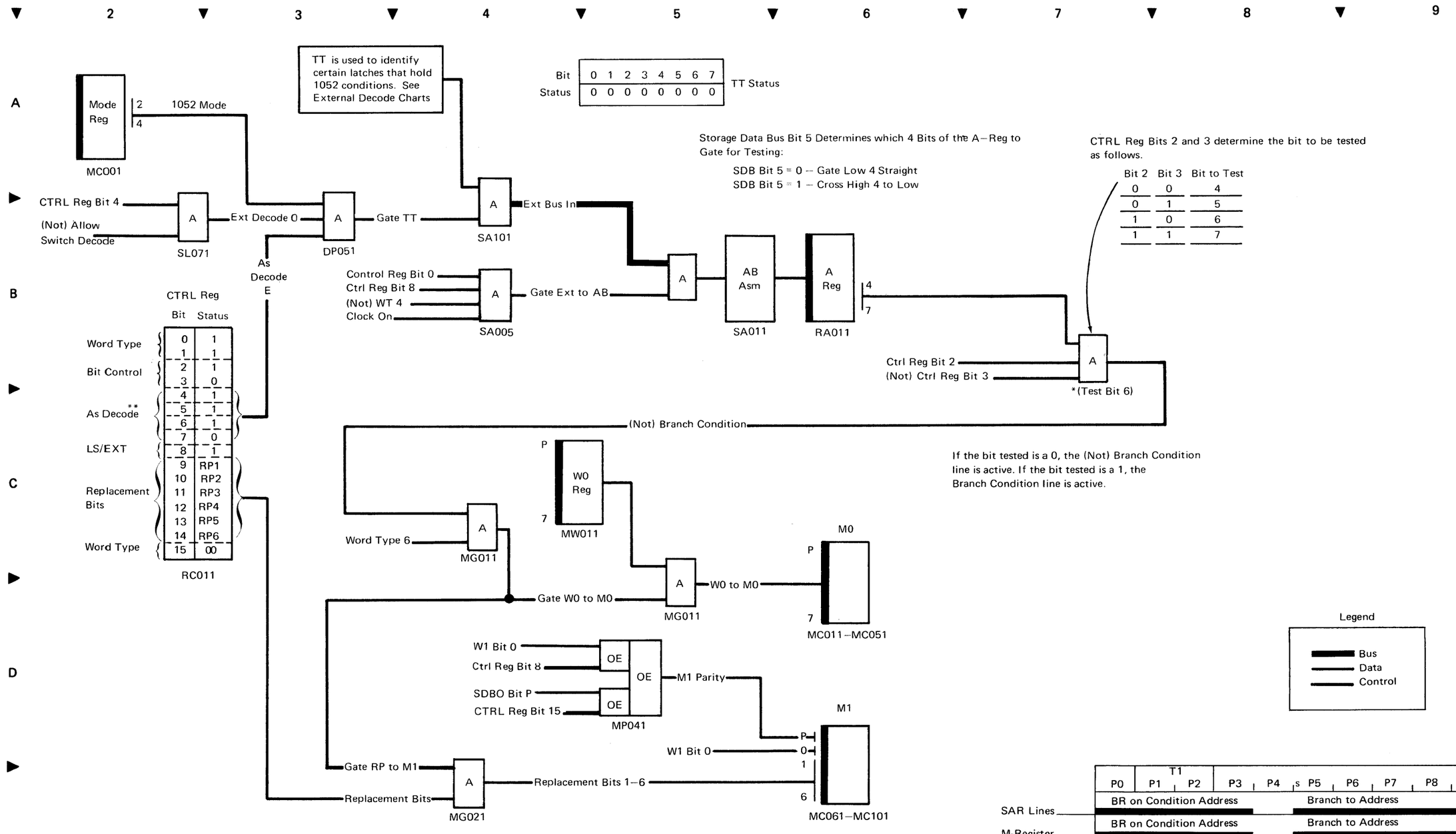

2
3
4
5
6
7
8
9
A
B
C
D
E
Mode Reg
RM051
5
7
LS Zone
Decode 0
(Not) Ctrl Bit 8
A
LS Addr Y0
LS Addr X7
LS Addr Asm
SL031 - 071
Address D1
LS Zone 0
0 1 2 3 4 5 6 7
0 1 0 1 0 0 1 1
D1 Contents
Local Storage Bus Out
AB Asm
SA011 - 091
A Reg.
RA011
0 1 2 3 4 5 6 7
4
7
Ctrl Reg
Bit Status
Word Type 0 1
1 0
Mask 2 0
3 1
AS Decode 4 0
5 1
6 1
7 1
LS/EXT 8 0
Replacement Bits 9 RP1,M1
10 RP2,M1
11 RP0,M1
12 RP5,M0
13 RP6,M0
14 RP7,M0
Word Type 15 1
RC011
P1
Bit 15
Ctrl Reg Bit 15
CC031
AS Normal Read
CC081
Ctrl Reg Bit 5
Ctrl Reg Bit 6
Ctrl Reg Bit 7
DP013
AS Decode 7
(Not) Ext to CPU
(Not) Gate K to AB
(Not) Gate M to AB
SA005
Gate LS to AB
Word Type 5
SDBO Bit 5 *
Cross
A Reg
AL251
* Bit 5 of the Ctrl Reg is set to 1 for this word. The straight cross control is taken from the storage data bus out.
Ctrl Reg Bit 3
Word Type 5
Gate BR Mask to M
MG011
Ctrl Reg Bit 12
Ctrl Reg Bit 13
Ctrl Reg Bit 14
Ctrl Reg Bit 11
Ctrl Reg Bit 9
Ctrl Reg Bit 10
Ctrl Reg Bit 2
Ctrl Reg Bit 3
Ctrl Reg Bit 2
Ctrl Reg Bit 3
4
5
6
7
M0
Forced to 0 P
From W0 0
From W0 1
From W0 2
From W0 3
From W0 4
1 5
0 6
1 7
M1
Forced to 0 P
1 0
0 1
1 2
0 3
1 4
0 5
1 6
Forced to 0 7
Legend
Bus
Data
Control
Example Statement
N = D1 Bits 1 2 3
Objectives:
1. Address the D1 byte in Local Storage for the zone in effect; in this example zone 0.
2. Use bits 1, 2, and 3 of D1 to set bits 4, 5, and 6 of M1.
3. Insert the replacement bits from the control word into M0 and M1.
Assume: Ctrl Reg Bit 9 = 0, 10 = 1, 11 = 1
12 = 1, 13 = 0, 14 = 1
T1
P0 P1 P2 P3 P4 P5 P6 P7 P8 P9
SAR Lines
M-Register
W-Register
AS Read LS Odd
A-Register
M0-Register
M1-Register
BR on Mask Address
Branch Address
BR on Mask Address
Branch Address
BR on Mask Address + 2
Byte to Test (D1)
Byte to Test (D1)
W0 Bits 0-4, Ctrl Reg Bits 12-14
Ctrl Reg Bits 9-11, Test Byte Bits

Diagram 5-13. Branch on Condition Word (Word Type 6 or 7)



Example Statement

BR IF TT Bit 6=0

Objectives:

1. Address the External facility TT which contains information pertaining to 1052 Status.
2. Branch to an address specified by the replacement bits in the control word if bit 6 of TT = 0. (Branching takes place by loading the M1 Register with the replacement bits).

* Bit 6 of TT, if equal to 1, indicates 1052 request.

** Bit 5 of the CTRL Register is forced to a 1 for this word. Storage Data Bus Bit 5 is tested for A-Register straight or cross gating.

	Hex addr	Hexwrd	Next addr	Name	Next label	Statement	Comments	Statement No.
					CICY			
A	12E6	5498		I-Start 3		RDH G I +2		CICY008
	12E8	B435	CICY016		OPHI N	N=G0H		CICY009
	12A2	B015	CICY148	OPHI 1	OPIX N	N=G0L		CICY017
	1292	AABC	CBIN005	OPIX 9	CBIN RROP19	BR		CICY157
					CBIN			
▶	2ABC	9F64	CCOM036	RROP19	CCOM CRGET	BAL		CBIN005
					CCOM			
	IF64	55B3		CRGET		T1=G1XH		CCOM036
	IF66	52A8				RDH V AS,T+2		CCOM037
	IF68	50AA				RDH U AS,T-2		CCOM038
	IF6A	55BB				T1=G1H		CCOM039
B	IF6C	56A8				RDH D AS,T+2		CCOM040
	IF6E	5EAA				BDH H AS,T-2		CCOM041
	IF70	100E				RST S K=F0		CCOM042
	IF72	128E				RTN		CCOM043
					CBIN			
	2ABE	924A	CBIN009		CXCOMP	BR		CBIN006
▶	124A	B69A	CCOM086	CXCOMP	CCOM CSLOOP	BAL		CBIN009
					CCOM			
	369A	3002		CSLOOP		SET S K=90		CCOM086
	369C	7F1D		CXLOOP		H1C=H1,+-,U1+C		CCOM087
	369E	7E0D				H0C=H0,+-,U0+C		CCOM088
C	36A1	773D				D1C=D1,+-,V1+C		CCOM089
	36A2	762D				D0C=D0,+-,V0+C		CCOM090
	36A4	1288				RTN		CCOM091

CBIN

	124C	E4D0	CBIN012		OVER	BR IF NOVFL		CBIN010
▶	124E	168D				D0=D0,OR,K80		CBIN011
	1250	E5D7	CBIN015	OVER	NZO	BR IF S2=1		CBIN012
	1252	2C07				P0=0		CBIN013
	1254	81F5	CICY005		CICY ISTART N	N=S BITS67		CBIN014
	1256	C645	CBIN018	NZO	ALOW	BR IF D0.0=1		CBIN015
	1258	2C25				P0=0.OR.K20		CBIN016
	125A	81F5	CICY005		CICY ISTART N	N=S BITS67		CBIN017
D	1244	2C55		ALOW		P0=0,OR,K50		CBIN018
	1246	81F5	CICY005		CICY ISTART N	N=S BITS67		CBIN019

▶

This example shows only the portion of each microroutine used by the compare op. The control words in the final CBIN routine block that are not used are shaded.

E

Instruction = OP R1 R2: 1 9 6 7 — R1 = FC E6 B7 CB — R2 = FC E6 B7 CA

Read out instruction and place in G-register. G = 19 67
Test Op-code and branch to proper routine.

Branch to common routine to read out operands.

Read out operands and place in local storage
in preparation for compare.
T-register is set up to use as an indirect
address register.
First, read out general purpose reg 7 (2nd operand).
Then read out general purpose reg 6 (1st operand).

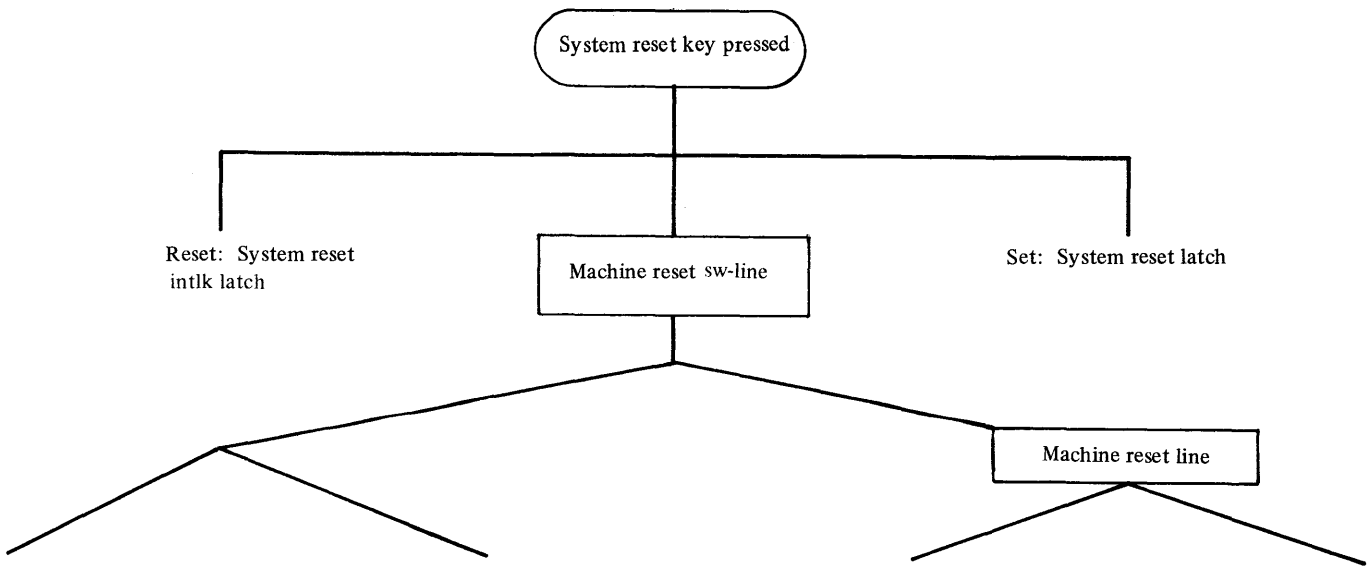
V = FC E6 U = B7 CA 2nd operand
D = FC E6 H = B7 CB 1st operand

Branch to common routine to compare.

Set S0 to indicate complement addition.
Set S3 to provide "Hot One" for first addition.
2nd operand is complemented and added to 1st operand.

```
1st oper =   F C E 6   B 7 C B
Comp
2nd oper =   0 3 1 9   4 8 3 4
                                1 S3
Result =     0 0 0 0   0 0 0 1      H = 0 0 0 0   D = 0 0 0 1
                                    S3 = 1
```

Test for adder overflow. There is none, therefore, the branch is taken to test S2. S2 is set to 1 during the complement addition performed in the CCOM routine to indicate that the result was not zero.
Branch to test D0 bit 0. D0 bit 0 is not one, therefore, P0 is set to a value of 20. The high hex digit of P0 is the condition code; a hex 2 indicates that the first operand is larger than the second operand.
Branch to 1 cycles to continue machine instruction processing.



Registers

Reset
- Control reg.
- MODE reg.
- MMSK reg.
- M-reg
- DC-reg
- System mask reg.
- External intr reg.
- Interval timer counter
- S-reg. bits 0-5 and 7

Set
- S-reg. bit 6

Latches

Reset
- Load latch
- CSL latch
- Clock start latch
- Set IC latch
- Inst step latch
- Soft-stop latch
- Console intr latch
- Control address set latch
- Display store latch
- Manual inhibit latch
- Inhibit man. alter latch
- Alter storage latch
- Alter storage intlk. latch
- Allow PC latch
- Hard-stop latch
- Storage data chk latch
- Cntrl wd cycle latch
- Storage address chk latch
- Machine chk latch
- A-reg chk latch
- B-reg chk latch
- ALU chk latch
- Clock start pulse latch
- Control cycle latch
- Prog mem wd cycle latch
- Trap address intlk. latch
- Gate chan trap latch
- Gate chan trap intlk latch
- Storage wrap latch
- Read direct enable latch
- Main-storage scan latch
- Aux scan latch
- Worst case scan latch

Set
- IPL intlk latch
- Console intr intlk latch
- Gate M to SAR latch

Registers

Reset
- Diag. reg
- W-reg
- A-reg
- B-reg

Latches

Reset
- Clock start intlk latch
- Clock 1 - 4 latches
- Diag. branch latch
- Adr. match soft stop
- Read call latch
- Store control latch
- T0-T4 latch
- Mach chk mask latch
- Wait state latch
- STP violation latch
- File STP violation latch
- STP parity-error latch

Set
- Clock off latch
- Clock 5 latch
- Scan worst case

2540 - Causes native reader punch reset

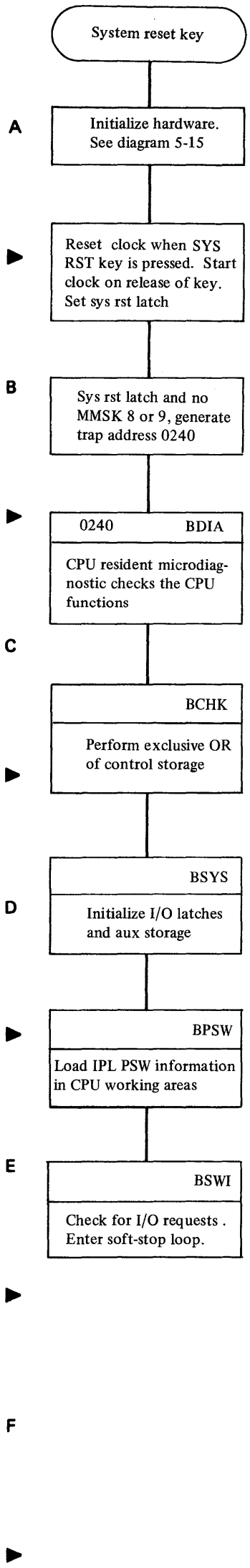
2311 - Sets chain end latch
Resets prog. control interrupt latch

1403 - Brings up 1403 machine reset
Resets single cycle latch

1052 - Sets attach reset latch
Resets TE-Data register

When the system reset latch is on and there is no MMSK 8 or 9, generate a microprogram trap to control storage address 0240.

Diagram 5-15. System Reset Key Hardware Function



BDIA routine checks: Branching capabilities, ALU functions, mode-register setting, core storage read and write, storage addressing, local storage read/write and addressing, dynamic condition register, ALU error detection, parity detection.

BPSW routine: The IPL PSW is loaded into the following working areas.

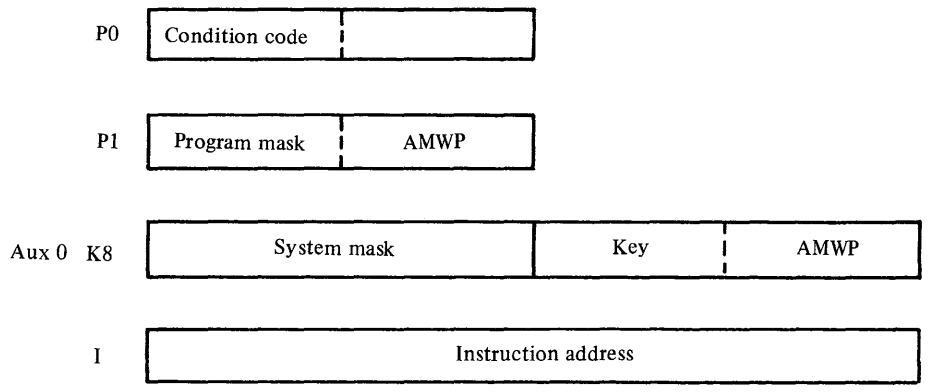
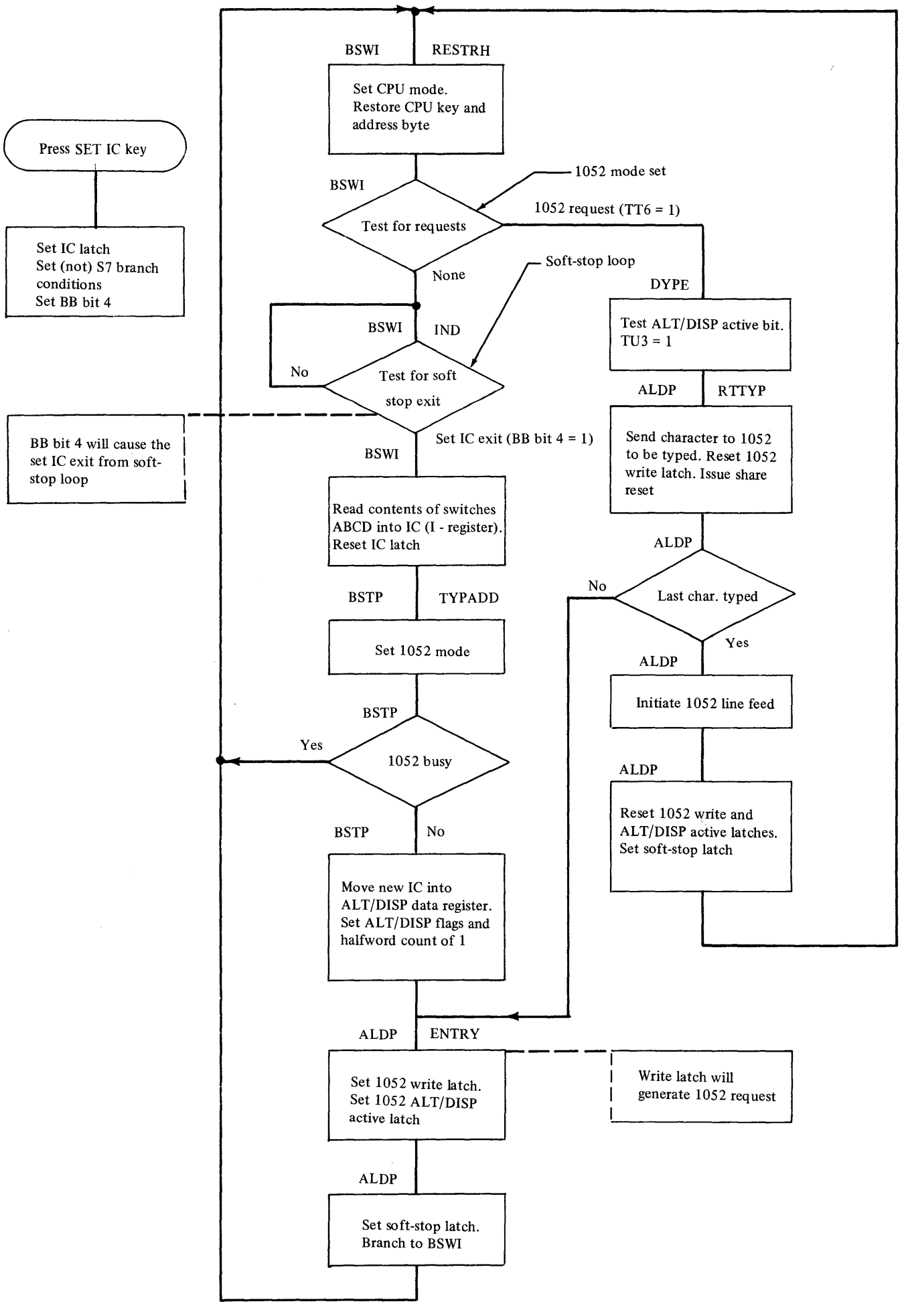


Diagram 5-16. System Reset Key



The SET IC key is effective only in the soft-stop condition.

Objectives:

1. Set IC latch.
2. Exit from soft-stop loop.
3. Place address from switches ABCD into instruction counter.
4. Print new address on the 1052.
5. Return to soft-stop loop.

Diagram 5-17. Set I C Key Function

Conditions:

Microprogram is in soft-stop loop. Assume that the previous operation was set 1C or address stop.

Objectives:

1. Turn mode switch to insn step position.
2. Press start key to exit from soft-stop loop.
3. Execute current instruction.
4. Return to 1-cycles and recognize (not) S7 branch condition.
5. Set insn step latch (BC0).
6. Type out instruction counter. Return to soft-stop loop to await PR-KB request after each character or function.
7. Wait in soft-stop loop until start key is pressed again (step 2).

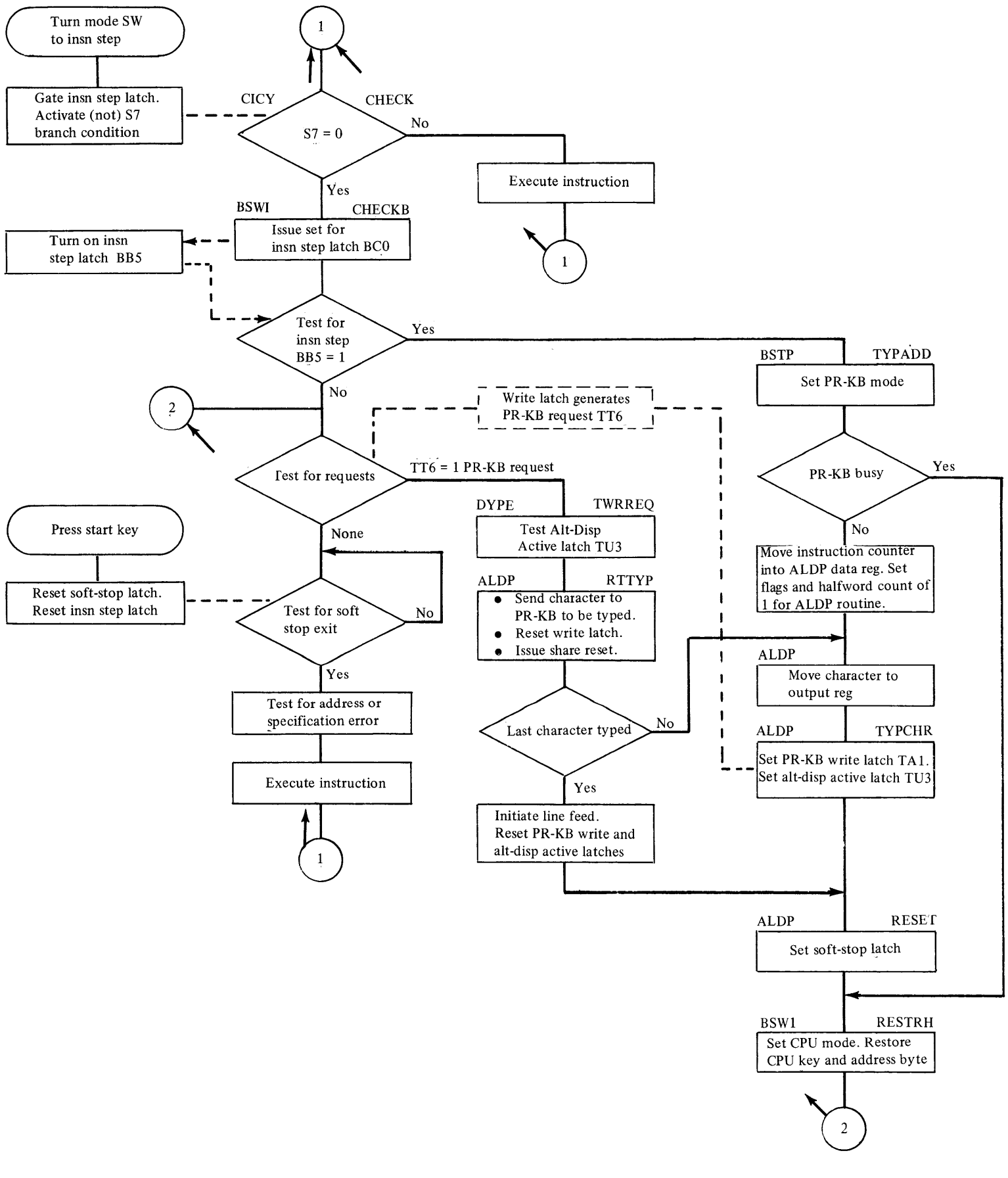


Diagram 5-18. Instruction Step Function

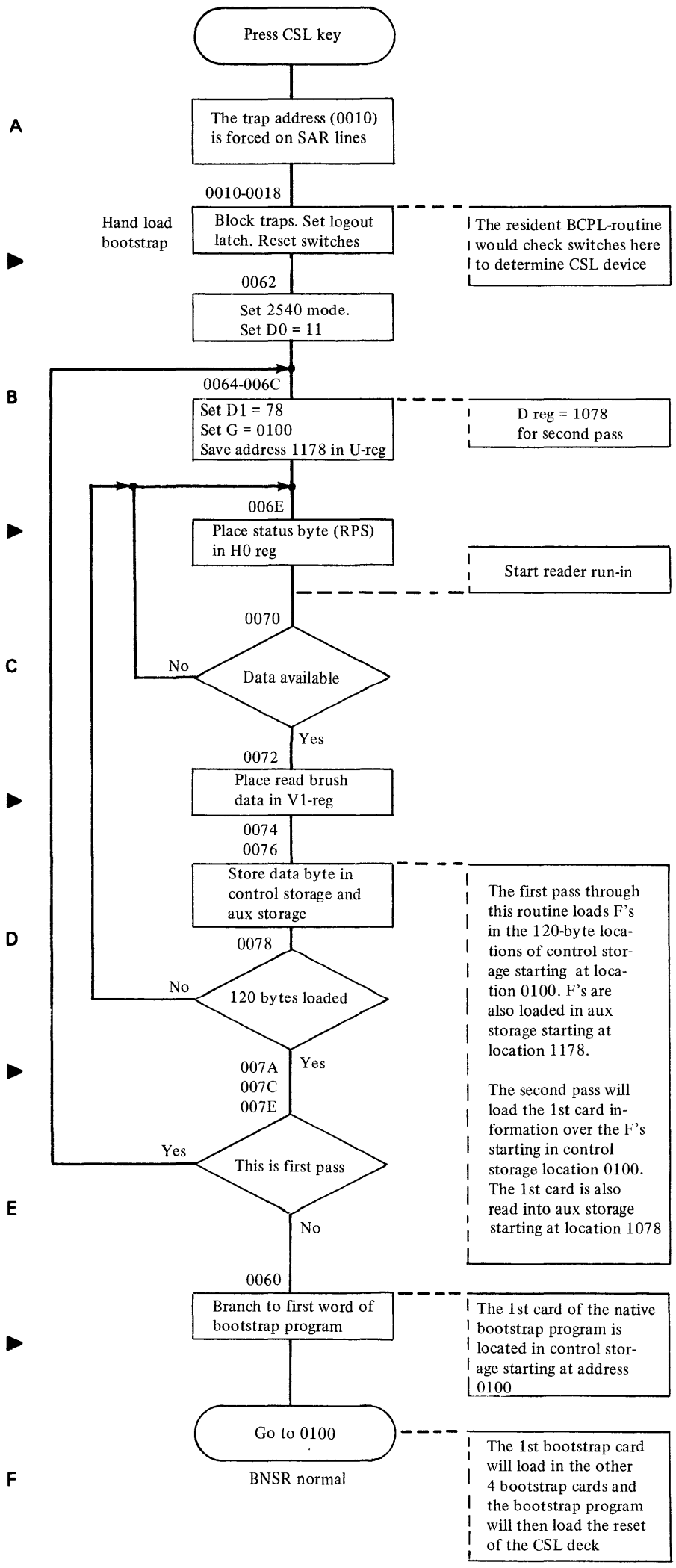
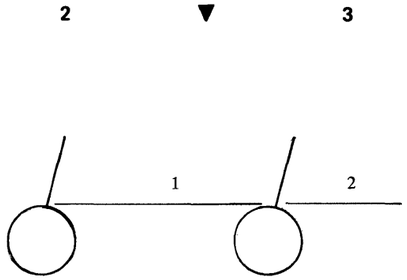


Diagram 5-19. CSL for Integrated 2540 (Part 1 of 3)



Control Storage

0100
Bootstrap Card
#1
0177

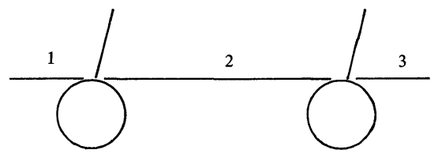
Auxiliary Storage

1001
Check Buffer
Bootstrap Card
#1
1078

After the hand-loaded bootstrap located at address 0010 has been executed, the 1st bootstrap card is located in the control storage and the check buffer.

The hand-loaded boostrap gives control to the microprogram located, at this point, at address 0100.

The second bootstrap card load and 1st bootstrap card check begin.



Control Storage

0100
Bootstrap Card
#1
0177

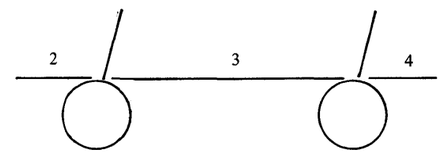
0178
Bootstrap Card
#2
01EF

Auxiliary Storage

1001
Check Buffer
Bootstrap Card
#2
1078

At this point in the load procedure, the 1st bootstrap card has been checked by a compare from the 2nd read brushes and the check buffer.

The 2nd bootstrap card has been loaded into control storage and into the check buffer.



Auxiliary Storage

3F00
Translate Table
Bootstrap Card
#3
3F77

Control Storage

0100
Bootstrap Card
#1
0177

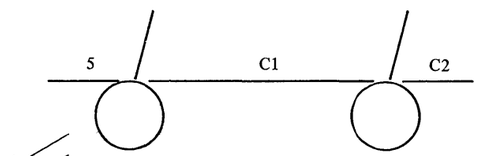
0178
Bootstrap Card
#2
01EF

Auxiliary Storage

1001
Check Buffer
Bootstrap Card
#3
1078

The 2nd bootstrap card has been checked and the 3rd bootstrap card has been loaded into the check buffer and the translate table.

The same load loop will continue until the remaining 2 bootstrap cards have been loaded.



Auxiliary Storage

3F00
Translate Table
Bootstrap Card
#3
3F77

3F78
Bootstrap Card
#4
3FEF

3FEF
Bootstrap Card
#5
34067

4068
1st card of
Control Storage
load #C1
40E0

Control Storage

0100
Bootstrap Card
#1
0177

0178
Bootstrap Card
#2
01EF

Auxiliary Storage

1001
Check Buffer
#C1
1078

All 5 bootstrap cards have now been loaded and the 1st card of the CSL deck has been loaded into the check buffer and into a portion of auxiliary storage beneath the translate table.

As the C1 card is read at the 2nd read brushes, the bootstrap program builds a translate table address area (1080 – 10F7) in aux stor.

The addresses formed will be used to address the translate table, built by cards 3, 4 and 5, to find the hex values to be loaded into control storage.

Card Image
Example For
First Card
Of CSL Deck
See CHART 2

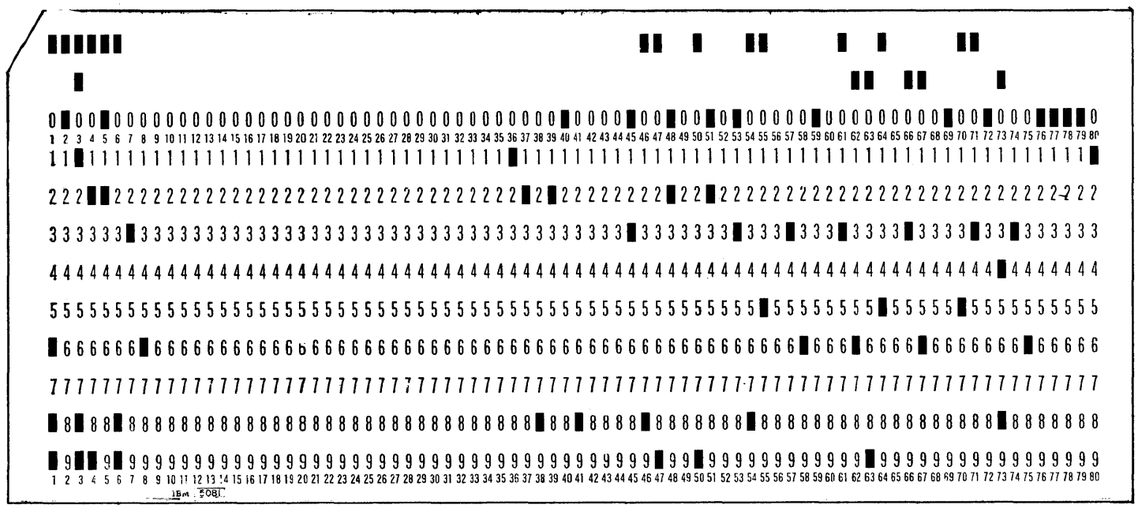


Diagram 5-19. CSL for Integrated 2540 (Part 3 of 3)

Entry point for the start of CSL READ is at label

BNSR NORMAL

As the CSL card is read at the 2nd read brushes it is checked against the check buffer. The translate table address area is built.

For each row that is read and tested, a specific bit combination is ORed into the table whenever a punch is detected in a column.

Bit Combination	Row
40	9
80	8
07	7
06	6
05	5
04	4
03	3
02	2
01	1
08	0
10	11
20	12

The table development shown in this diagram uses the card shown in diagram 5-15 Chart 1.

After the address table is built, the bootstrap program uses the address table to address the translate table to look up the hex data to be used in the loading of storage.

9-Row

Column 1 2 3 4 5 6 7 8

Starting Address is 1080 Aux Storage

9	40		40	40		40		
17								
25								
33								
41							40	
49		40						
51							40	
65								
73								

6-Row

C6		C0	40		C0		06
					80		
80					80	40	
	40				80		
	06				06	40	
		06					
80		06					

3-Row

C6		C0	40		C0	03	06
					80		
80				03	80	40	
	40			03	80	05	
03	06			03	06	40	05
	03	06			05	03	
84	03	06					

0-Row

C6	08	C1	42	0A	C0	03	06
			01	02	80	02	08
80			0B	80	40	0A	
	40	0A		0B	80	05	
03	06	08		03	06	40	05
	03	06		08	05	03	08
84	03	06	08	08	08	08	01

8-Row

C0		C0	40		C0		
					80		
80					80	40	
	40				80		
						40	
80							

5-Row

C6		C0	40		C0		06
					80		
80					80	40	
	40				80	05	
	06				06	40	05
		06			05		
80		06					

2-Row

C6		C0	42	02	C0	03	06
				02	80	02	
80				03	80	40	02
	40	02		03	80	05	
03	06			03	06	40	05
	03	06			05	03	
84	03	06					

11-Row

C6	08	D1	42	0A	C0	03	06
			01	02	80	02	08
80			0B	80	40	0A	
	40	0A		0B	80	05	
03	06	08		03	16	50	05
	13	16		08	05	03	08
94	03	06	08	08	08	08	01

7-Row

C0		C0	40		C0		
					80		
80					80	40	
	40				80		
						40	
80							

4-Row

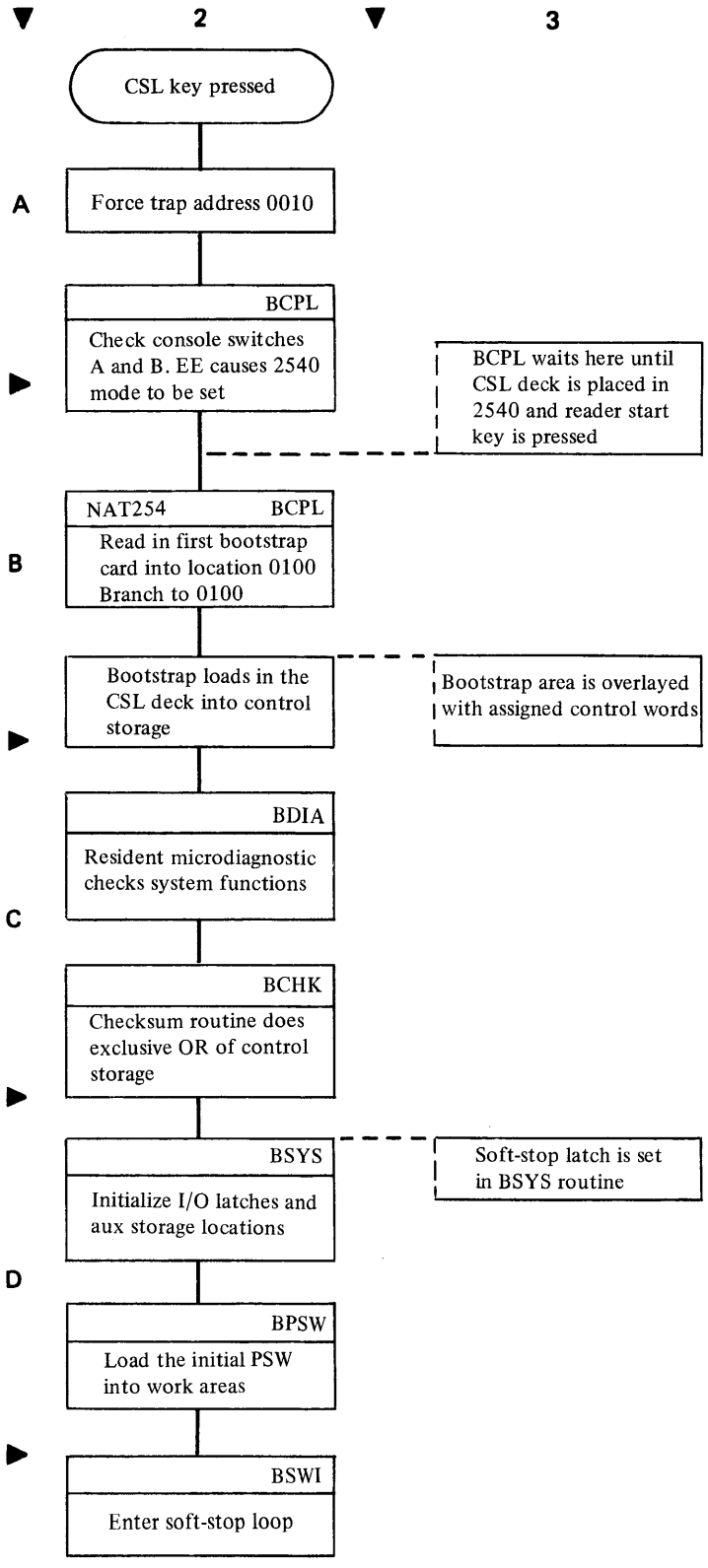
C6		C0	40		C0		01
					80		
80					80	40	
	40				80	05	
	06				06	40	05
		06			05		
84		06					

1-Row

C6		C1	42	02	C0	03	06
			01	02	80	02	
80				03	80	40	02
	40	02		03	80	05	
03	06			03	06	40	05
	03	06			05	03	
84	03	06					01

12-Row

E6	28	F1	62	2A	E0	03	06
			01	02	80	02	08
80				0B	A0	60	0A
	60	0A		0B	A0	25	
03	06	08		23	16	50	25
	13	16		08	25	23	08
94	03	06	08	08	08	08	01



The CSL procedure for the integrated 2540 is:

1. Set console switches A and B to position E.
2. Press the CSL key.
3. Place the CSL deck in the 2540 reader and ready the reader.
   The CSL indicator remains on until the CSL is completed.
   If the CSL check indicator is lit, the CSL either failed, or the CSL deck that was loaded does not match the EC level of the system.
   Re-CSL to try again, or press CHECK RESET then START to continue.

Diagram 5-20. CSL With Integrated 2540

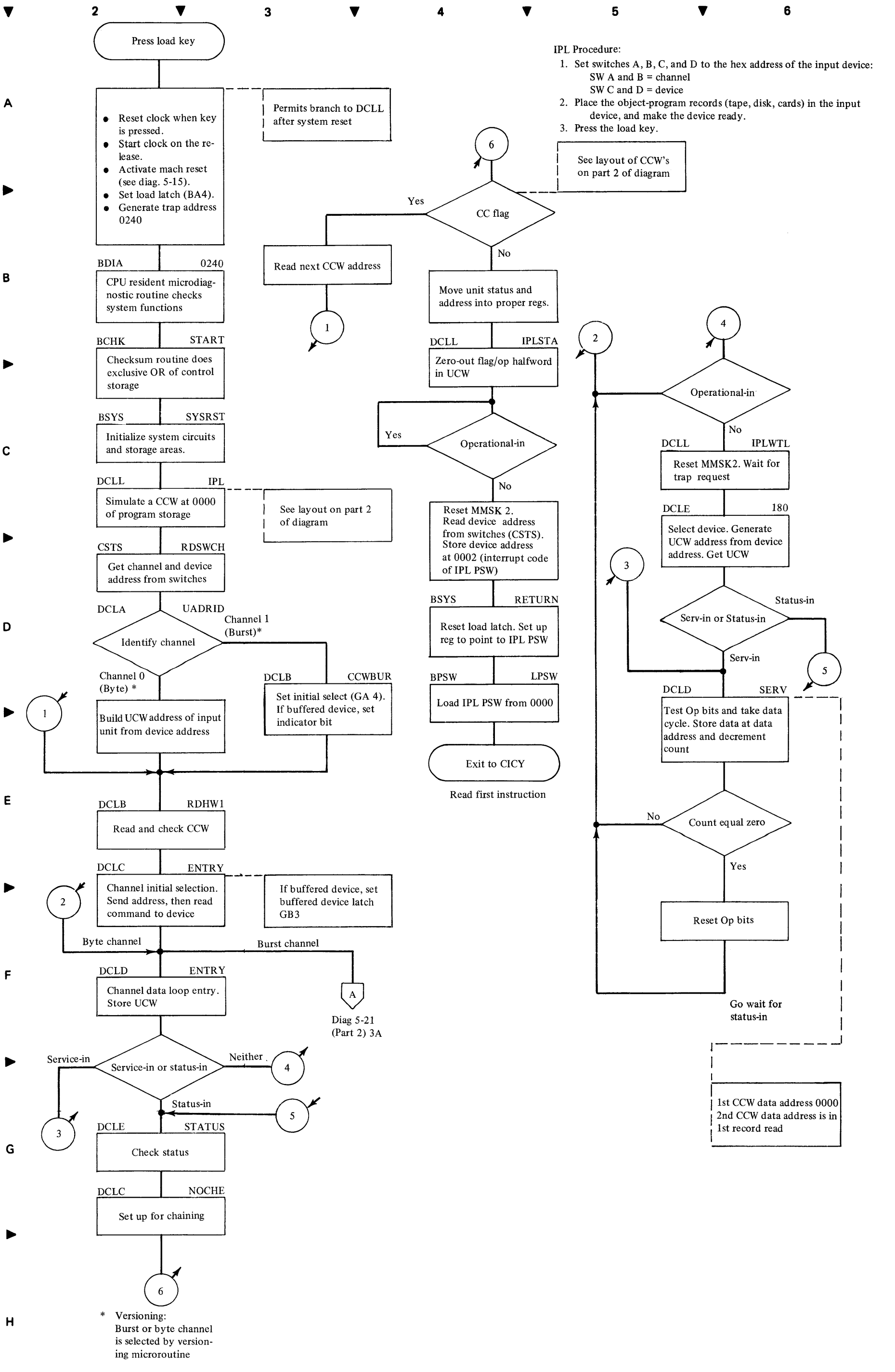


Diagram 5-22. IPL Load Operation and Byte Channel (Part 1 of 2)

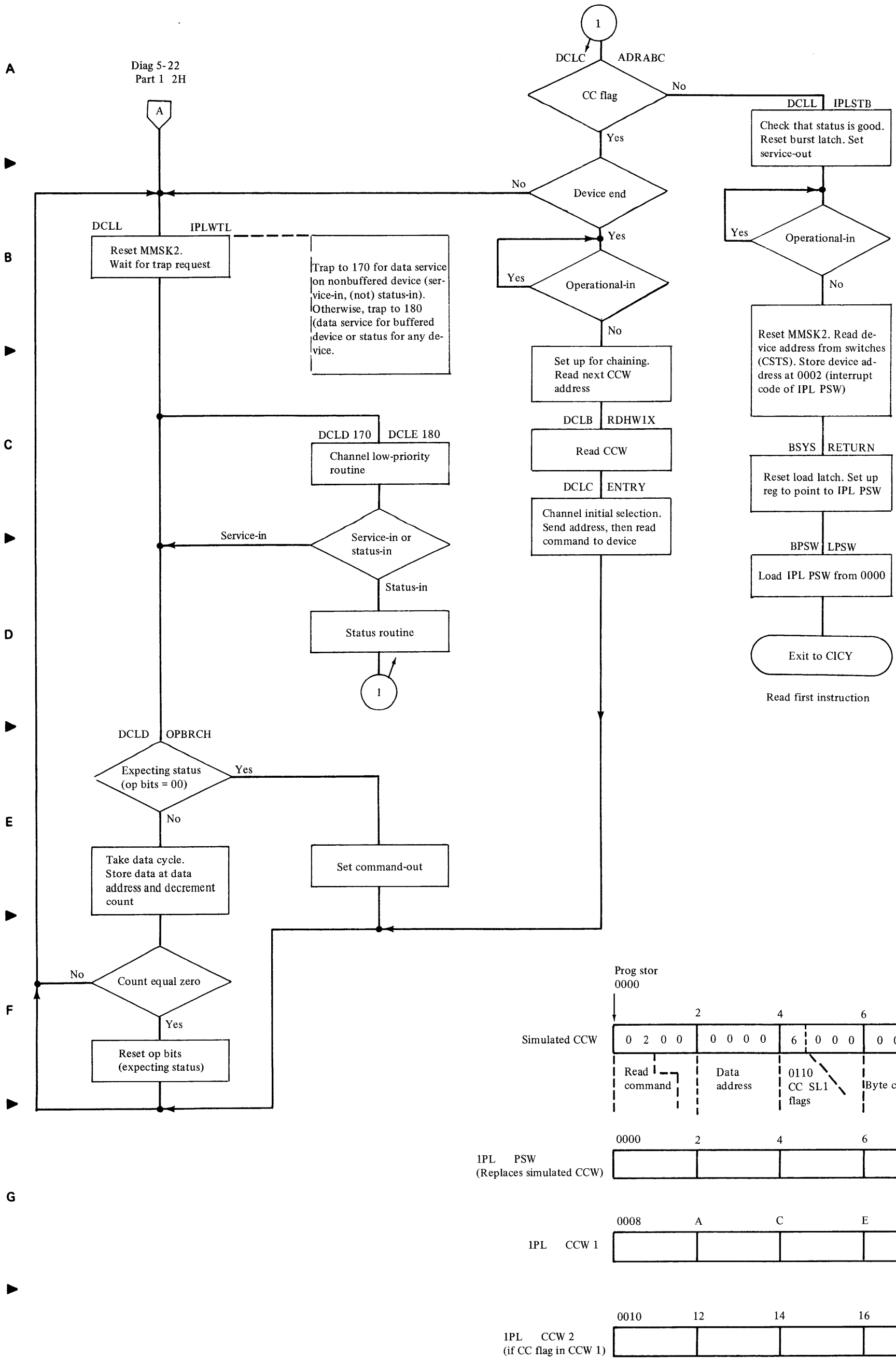
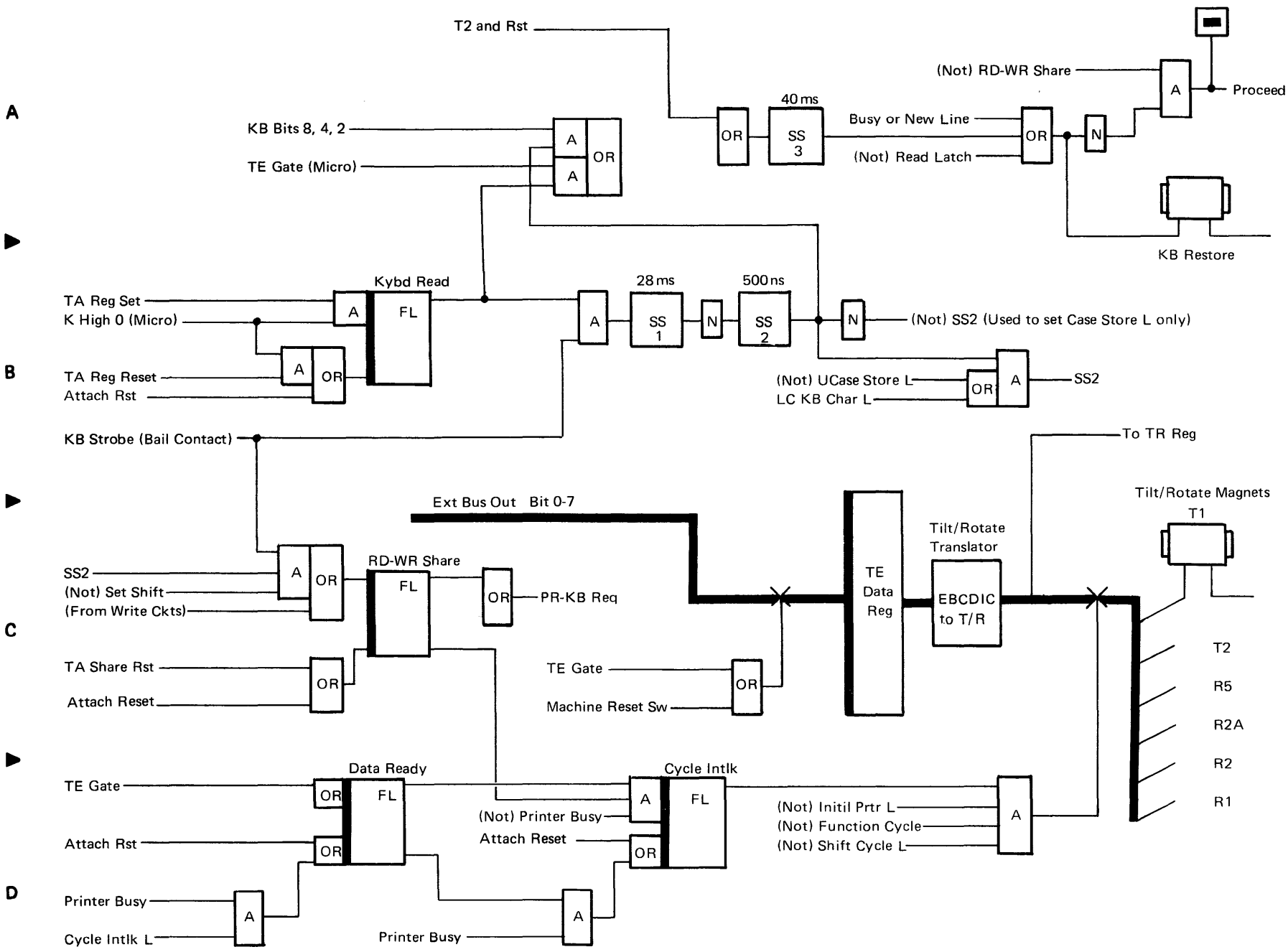


Diagram 5-22. IPL Load Burst Channel (Part 2 of 2)



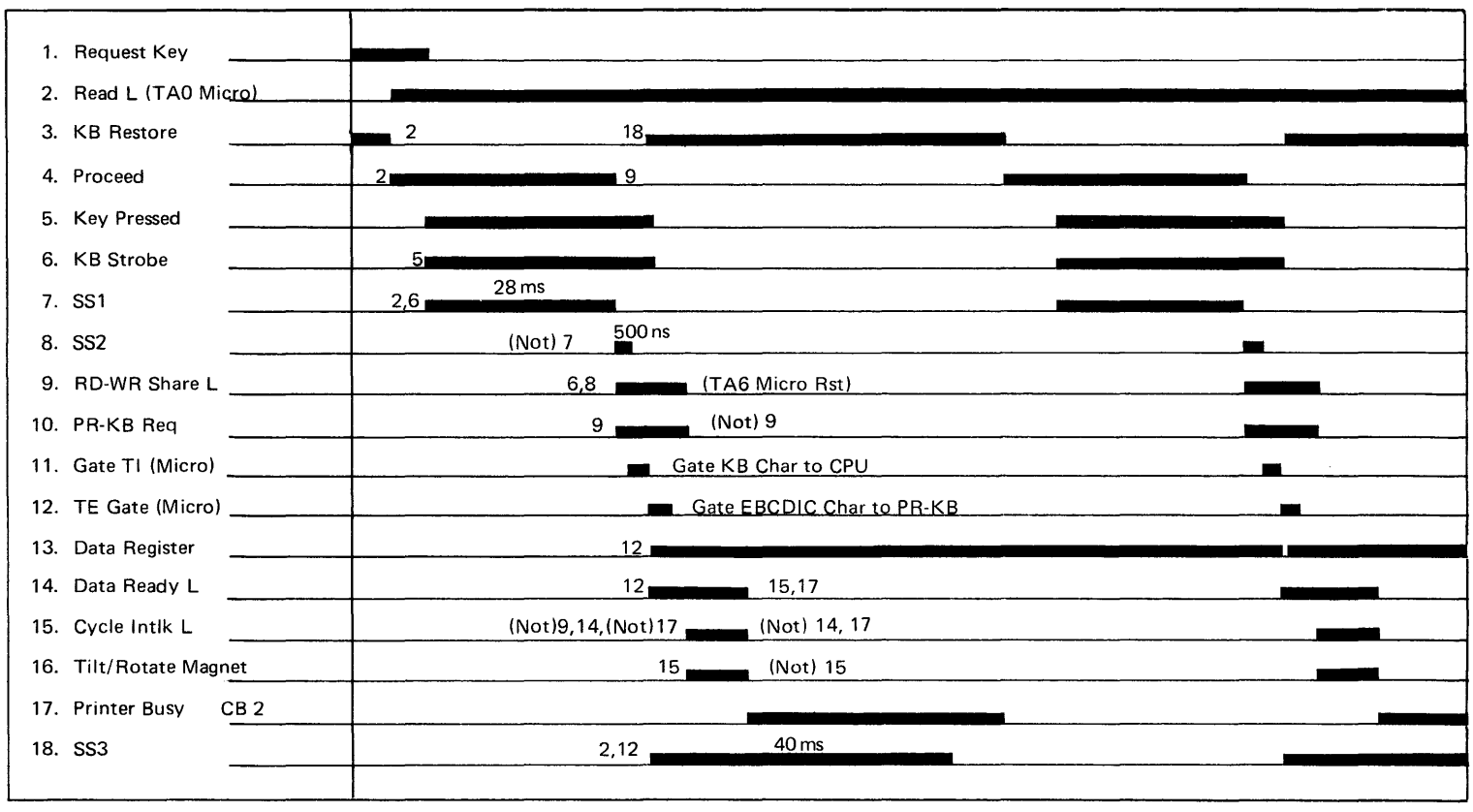
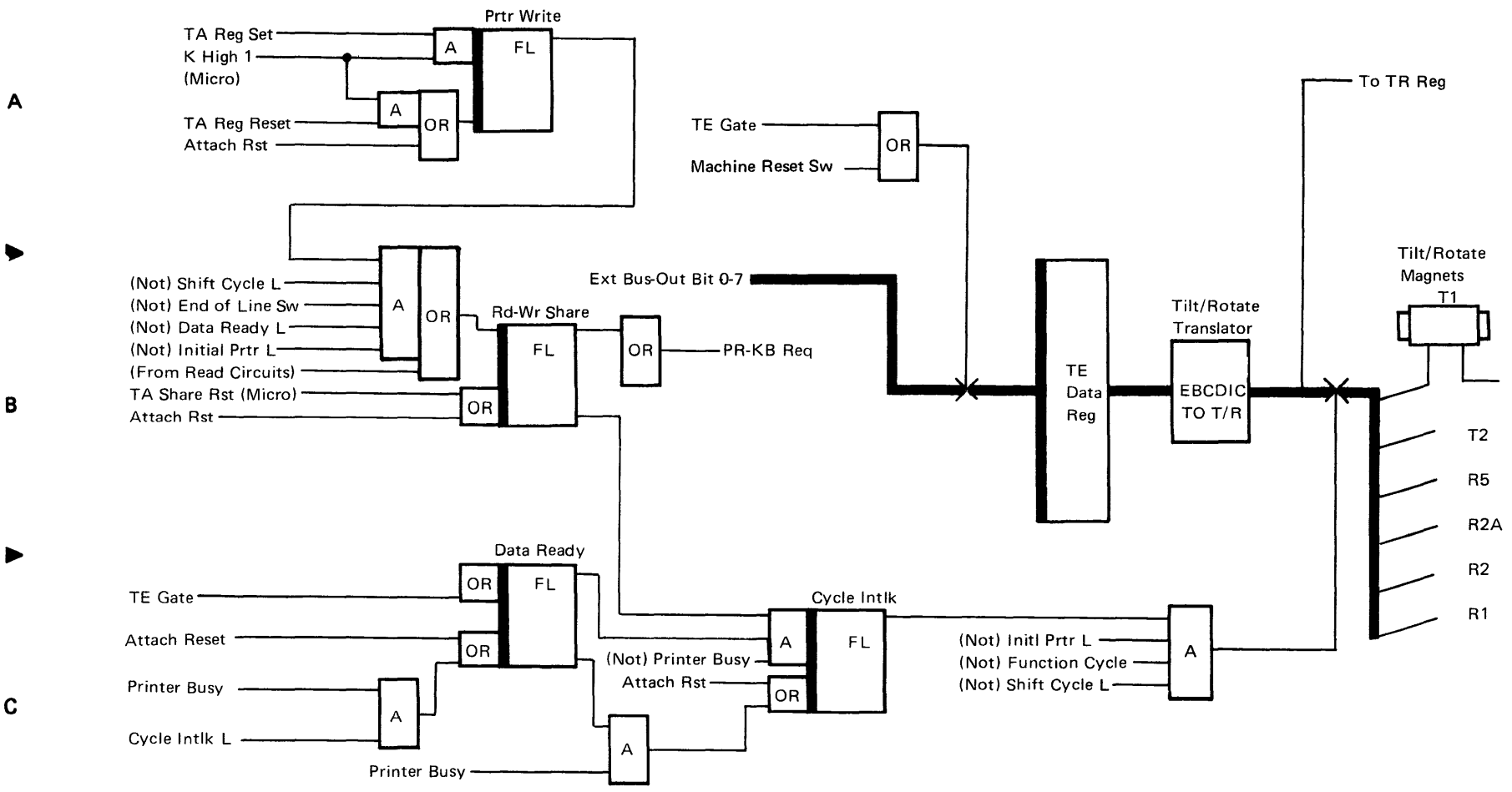


Diagram 5-71. 1052 Read Operation



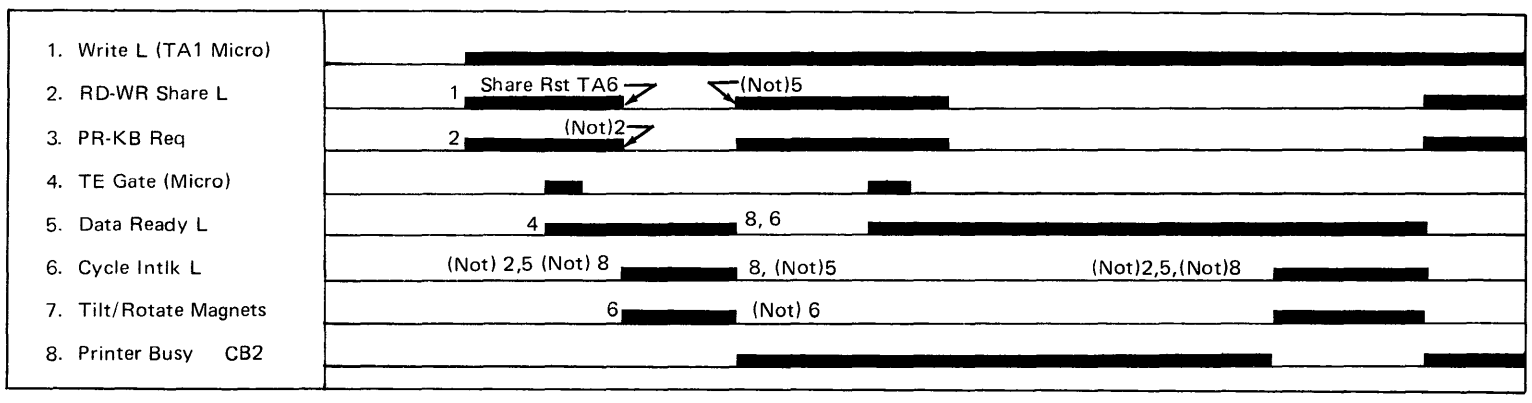
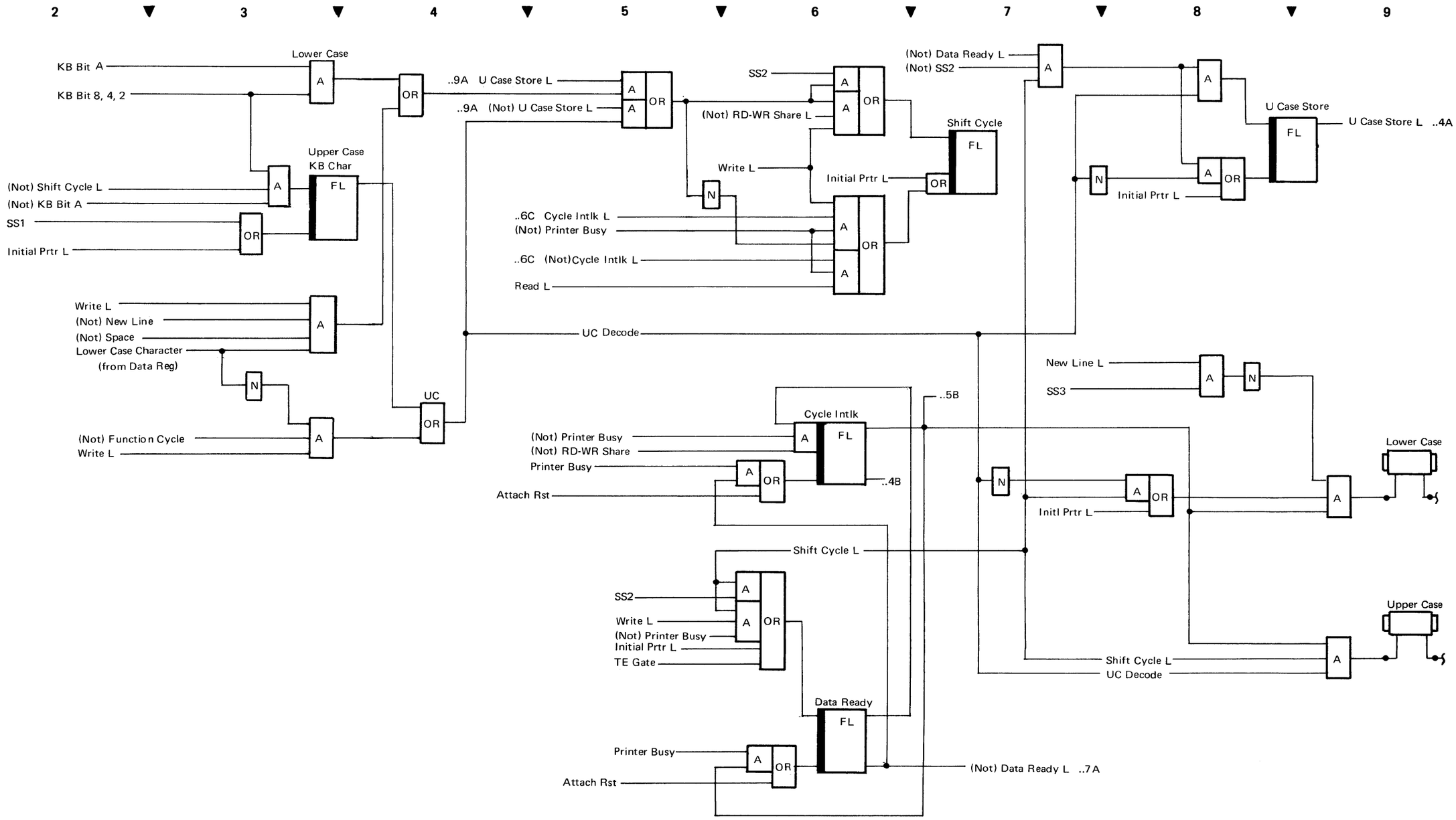
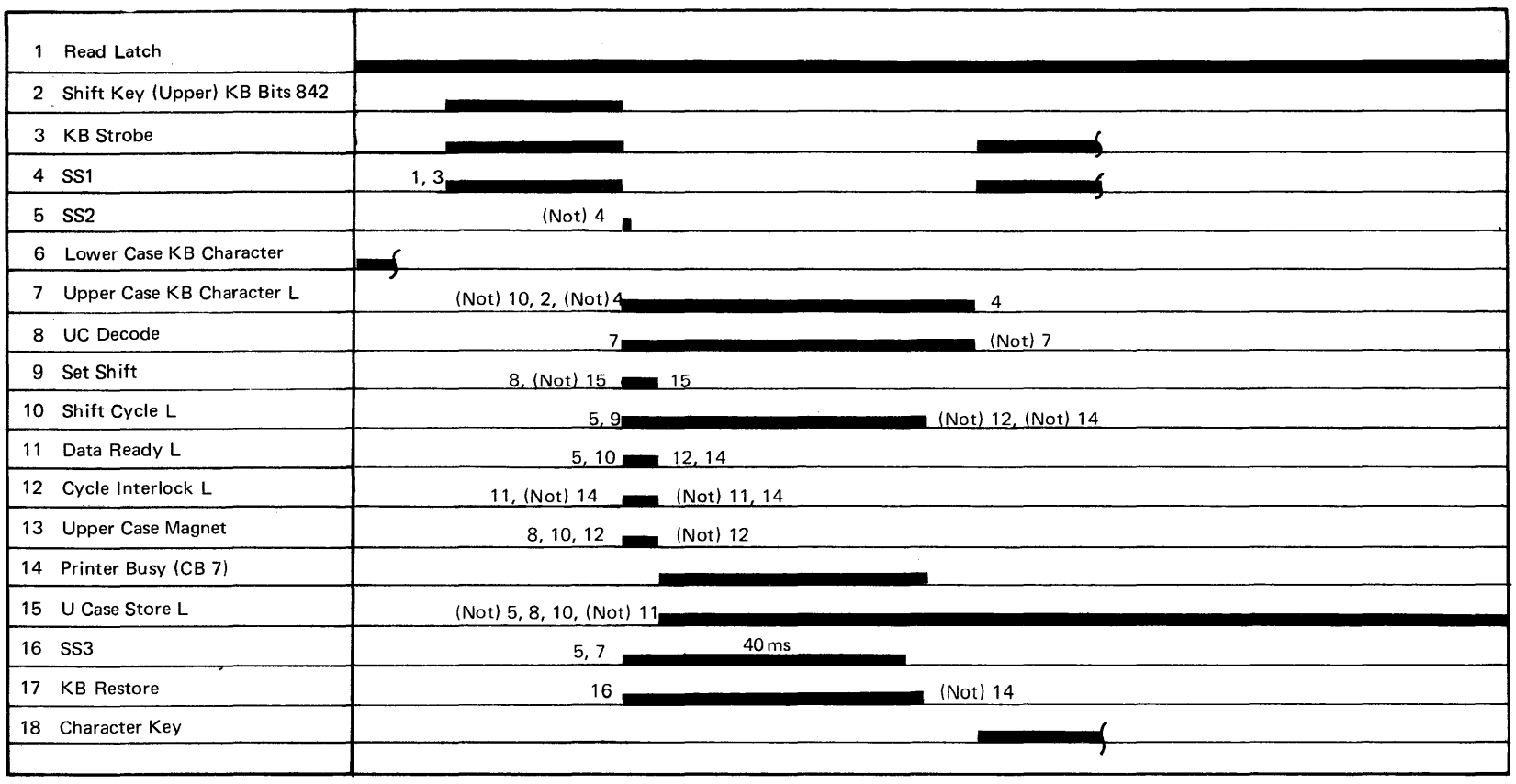


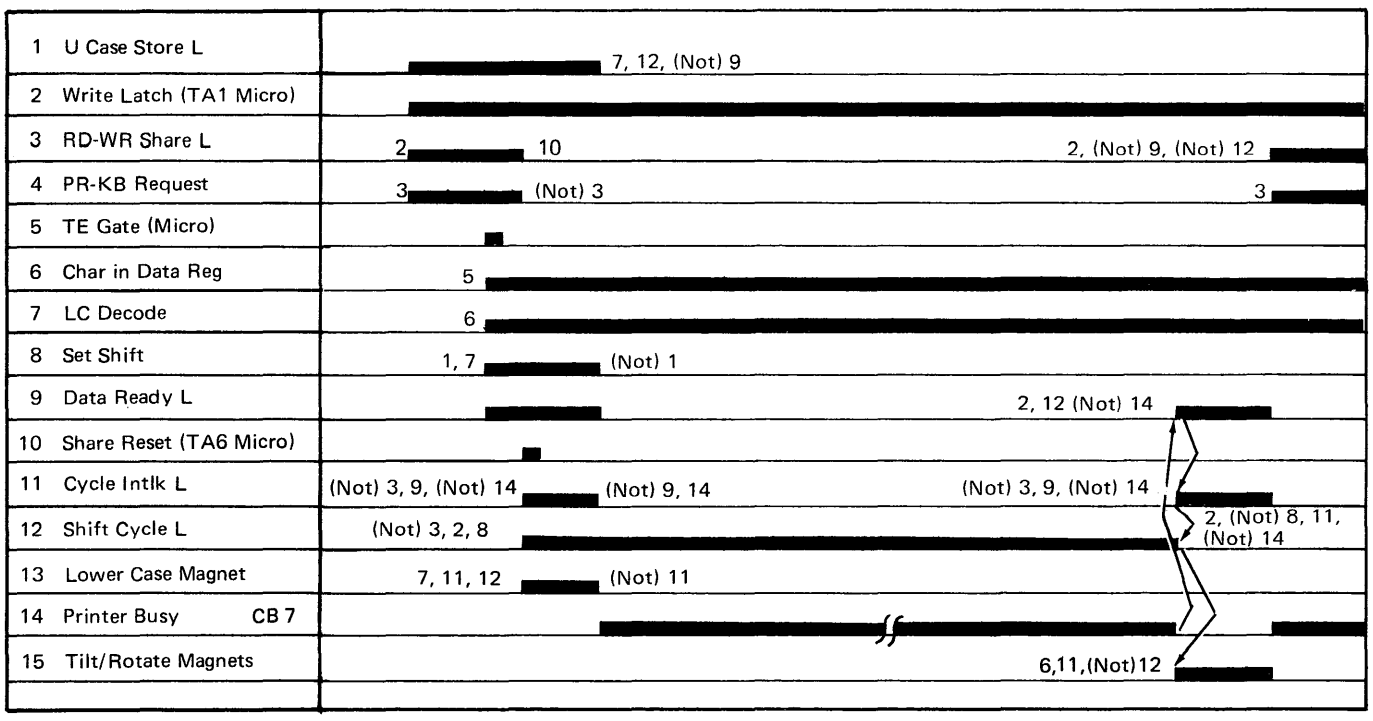
Diagram 5-72. 1052 Write Operation

Diagram 5-73. PR-KB Case Shift (Part 1 of 2)





Upper Case Shift (Read Operation)

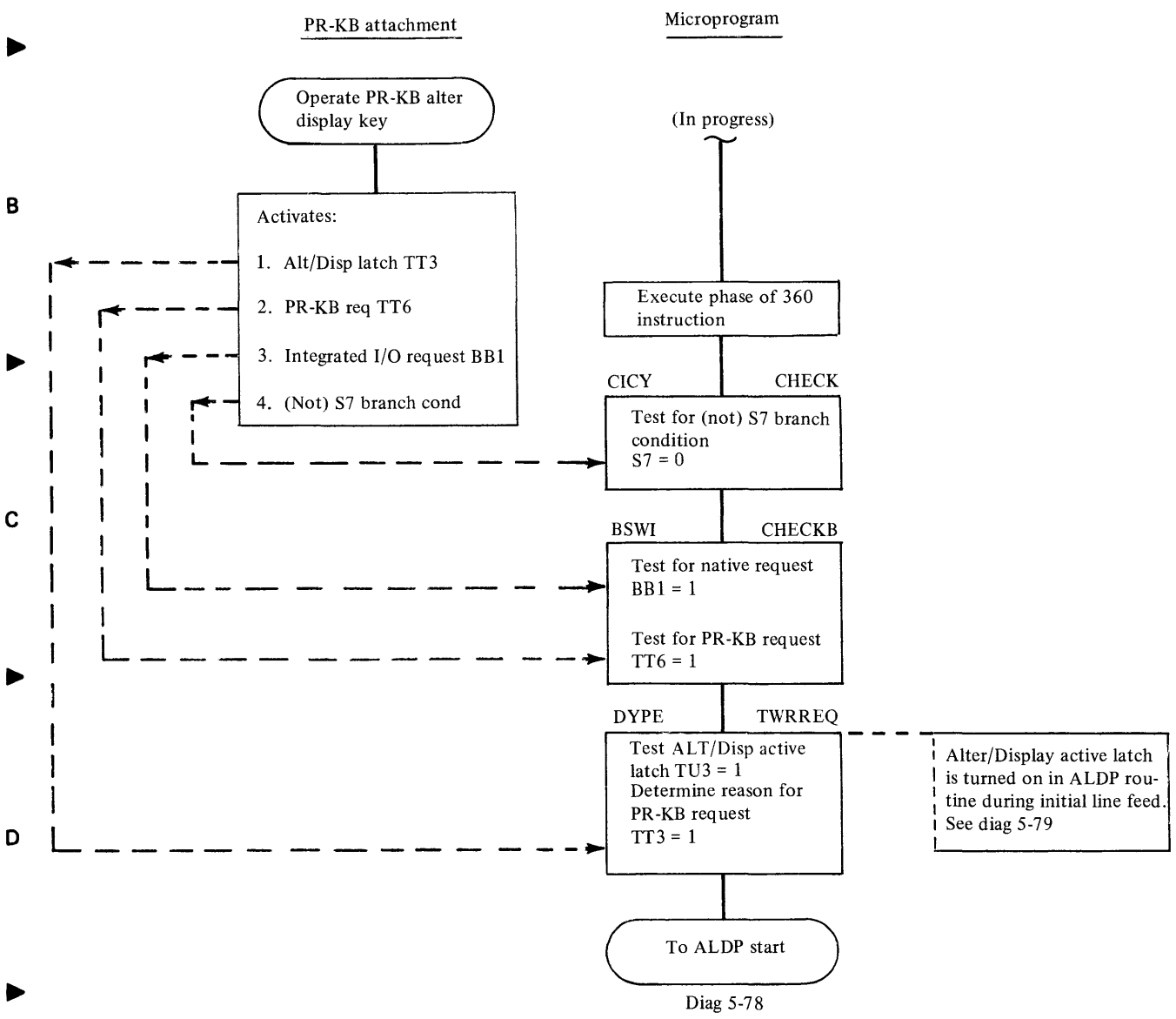


Shift To Lower Case During Write Operation

Diagram 5-73. PR-KB Case Shift (Part 2 of 2)

Objective: Start a PR-KB alter or display operation.

Assume:
1. PR-KB alter display switch is operated during the execute phase of a 360 arithmetic or logic instruction.
2. No other I/O requests or interrupts are pending.



Diag 5-78

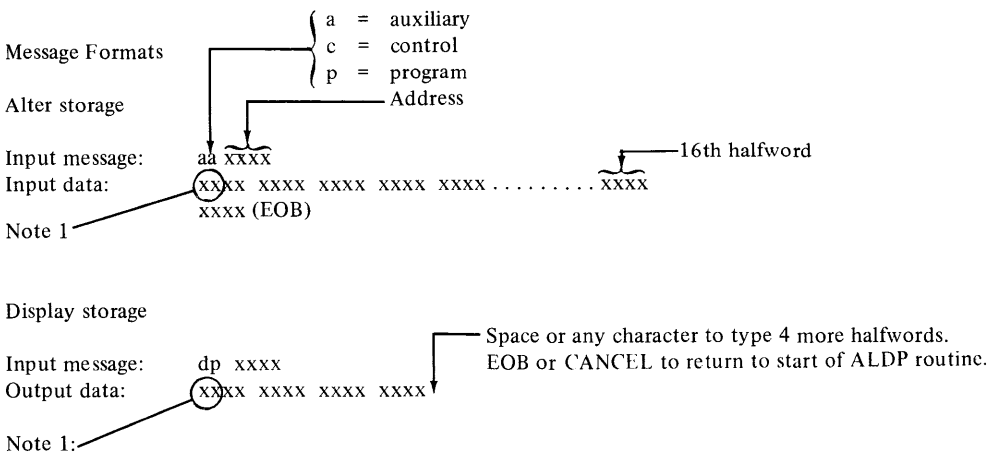


Diagram 5-77. PR-KB Alter-Display Start

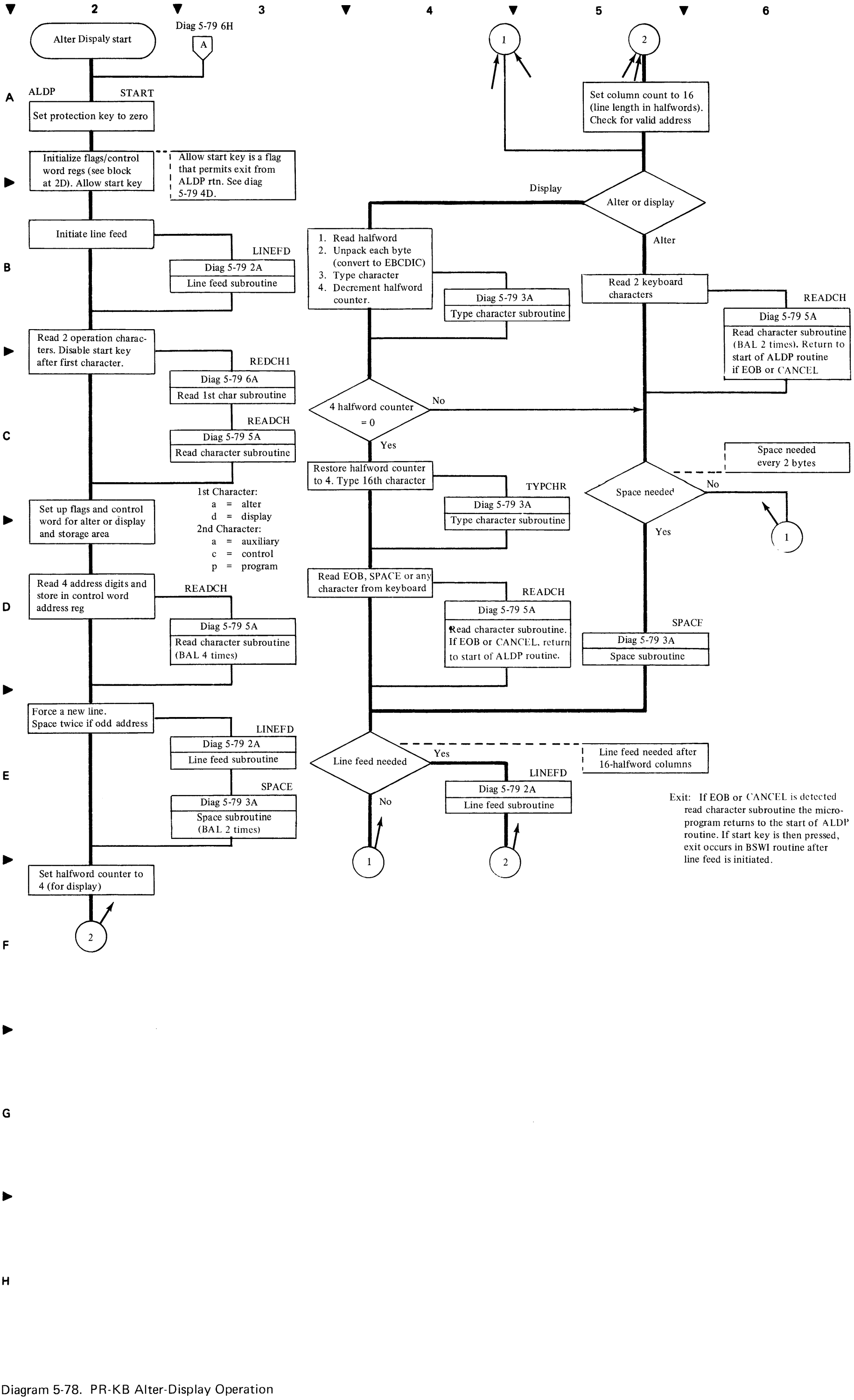


Diagram 5-78. PR-KB Alter-Display Operation

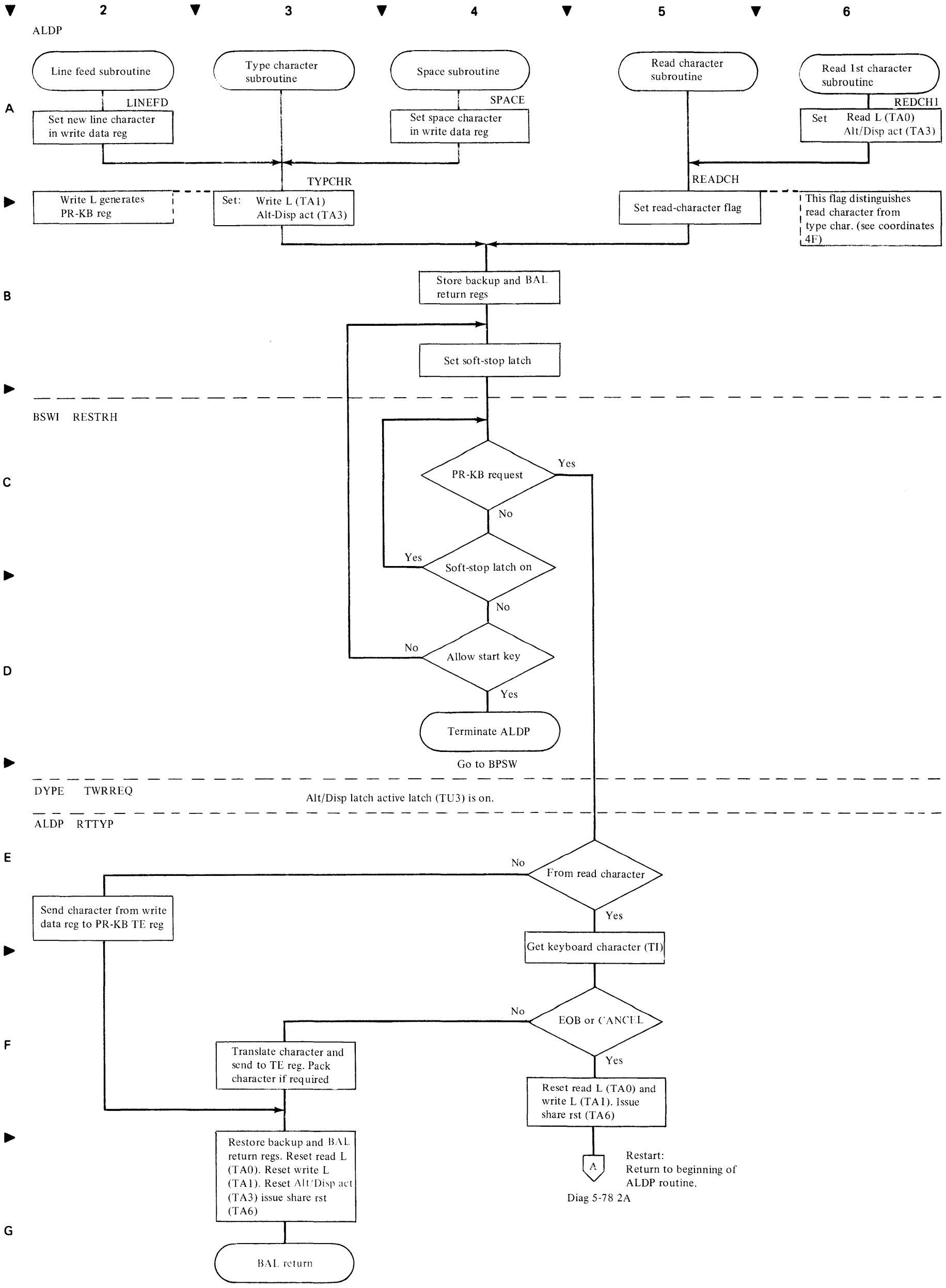


Diagram 5-79. PR-KB Alter/Display Subroutines

Program Storage
Address Hex 0080

LOGOUT AREA

80	81	82	83	84 85
Micro-Program Mask Reg (MMSK)	Branch Conditon Reg (BA)	Machine Check Reg (MC)	Count of Mach Check Errors * *	Address of Control Word where Machine Check Occurred

0	Channel High Trap	0	Chnl 0 Interrupt	*0	File Control Check
1	2311 Disk Control Trap	1	Mode Bit 0	1	Storage Protect Check
2	Channel Low Trap	2	Mode Bit 1	2	Storage Address Check
3	2540 Reader Trap	3	Mode Bit 2	3	Control Word Parity Latch
4	2540 Punch Trap	4	IPL Latch	4	Storage Data Parity Latch
5	Communication Bit Service	5	LS Zone Bit 0	5	ALU Error Latch
6	Communication Char Serv	6	LS Zone Bit 1	6	A-Reg Parity Latch
7	Level 1 Priority Hold	7	LS Zone Bit 2	7	B-Reg Parity Latch

** Bits 0–1 are logout code (00 for machine check)
* Bit 0= 1 indicates that the machine check indicated in bits 1–7 occurred while in 2311 Disk Mode (not File Share Cycle)

Note: This diagram shows machine check logout only. For channel interface control check, layout of logout area is changed as follows:

Byte
82 GS chnl ext conds
84 GT chnl ext conds
85 GD chnl Ext conds
86-87 Unit ID

Conditions

The microprogram traps to address 0220 if all of the following conditons are satisfied:

1. MMSK bit 8 and 9 off. (Not system reset, CSL, IPL or prior machine check)
2. The Mach Chk Mask latch (MW bit 5) is on. This latch is set if PSW bit 13 is on when the PSW is loaded (BPSW routine).
3. The Mach Chk latch turns on. The conditons that turn the Mach Chk latch on are indicated by the MC-Reg shown at the top of this page.

Objectives

A. Machine Check During I/O Trap
   1. Terminate I/O operation.
   2. Attempt I/O interrupt.
   3. Store logout information and print logout area before next CPU instruction.

B. Machine Check, Not I/O Trap
   1. Take machine check interrupt. Store machine check old PSW and load new PSW.
   2. Store logout information.
   3. Print logout area.

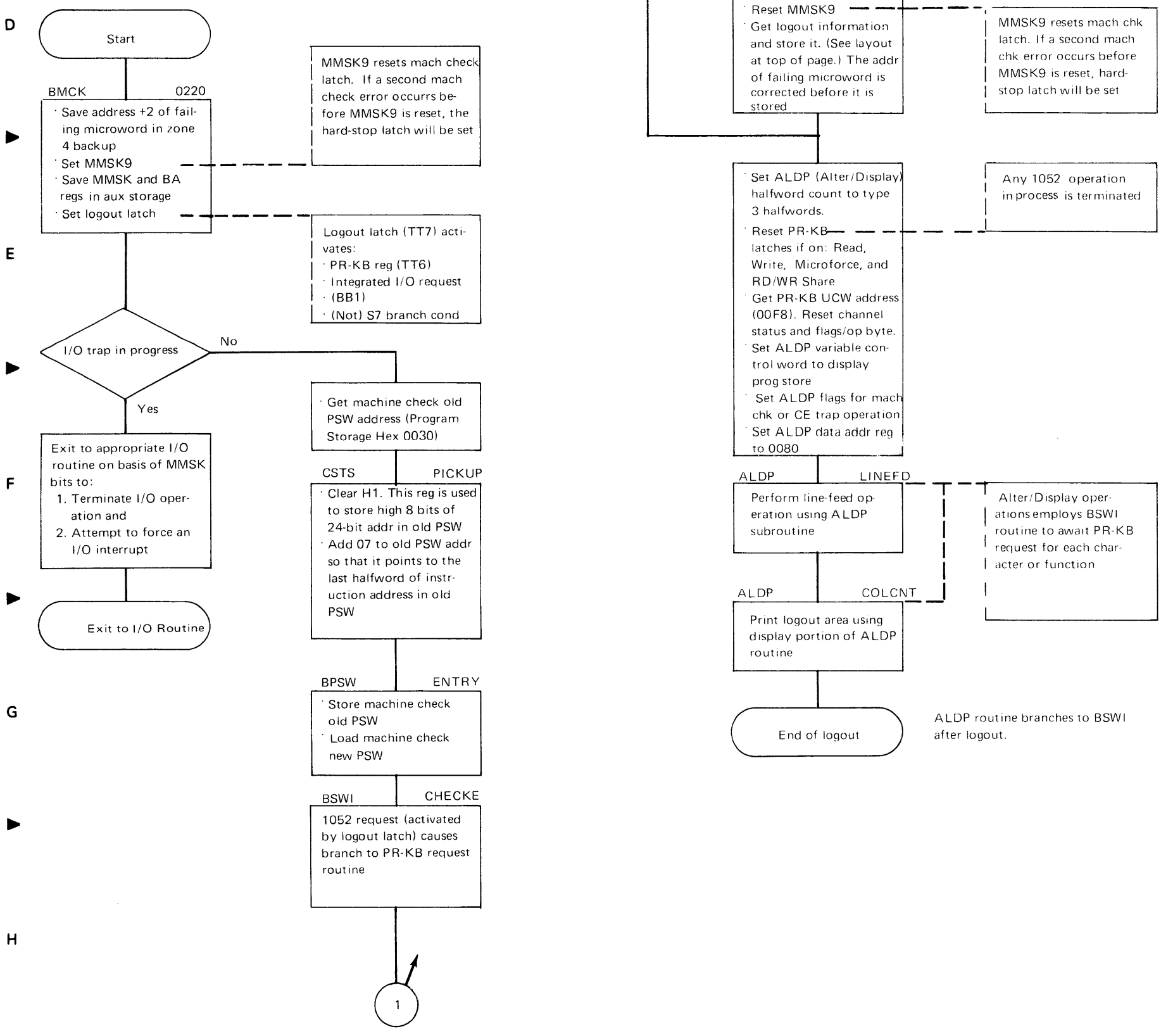


Diagram 5-80. Mach Check Logout

Diagram 5-85. Move Arithmetic Word, External Facility to Local Storage (Word Type 3)

2 3 4 5 6 7 8 9

A

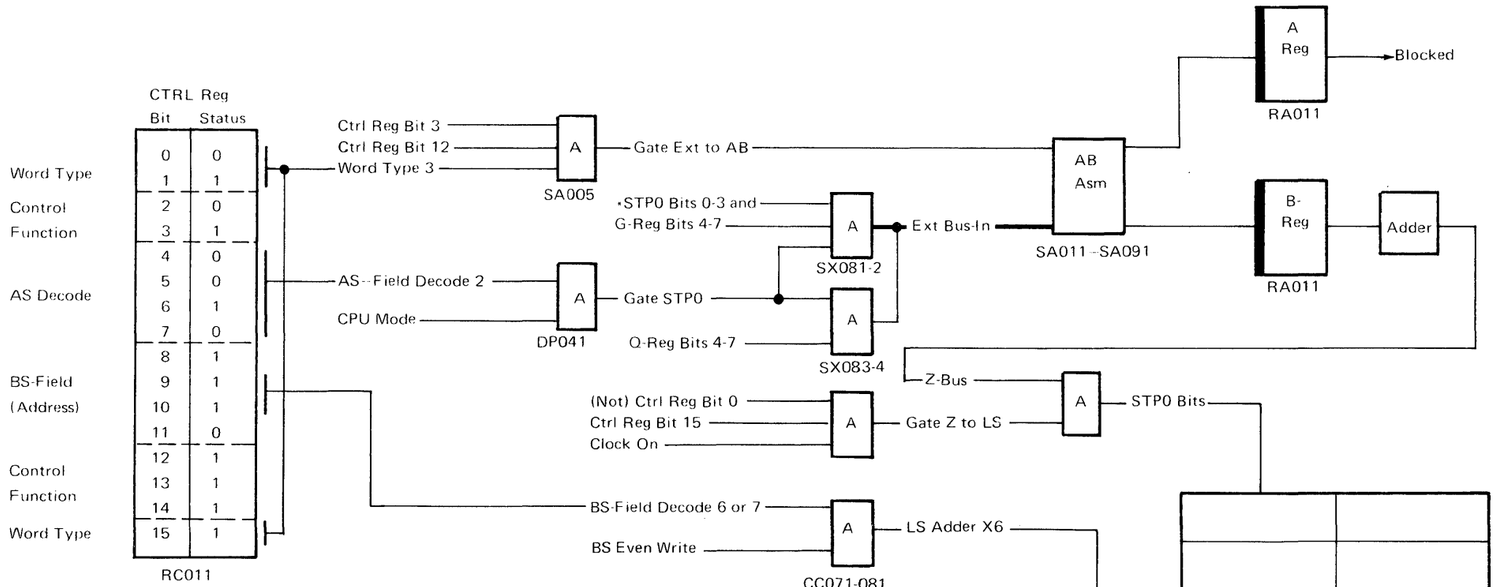
Move/Arithmetic Word (Word Type 3)

(External Facility to Local Storage)

*STP0 is an external register determined (gated) by the contents of the mode register (TR052 or MDM4-14). Refer to MDM4-90, Part 1 for STP0 and Q-Reg gating:

CPU Mode: STP0=Q-Reg
2311 Mode: STP0=FQ-Reg
Channel Mode: STP0=GQ-Reg
Communications Mode=HQ-Reg

B



C

D

Example Word

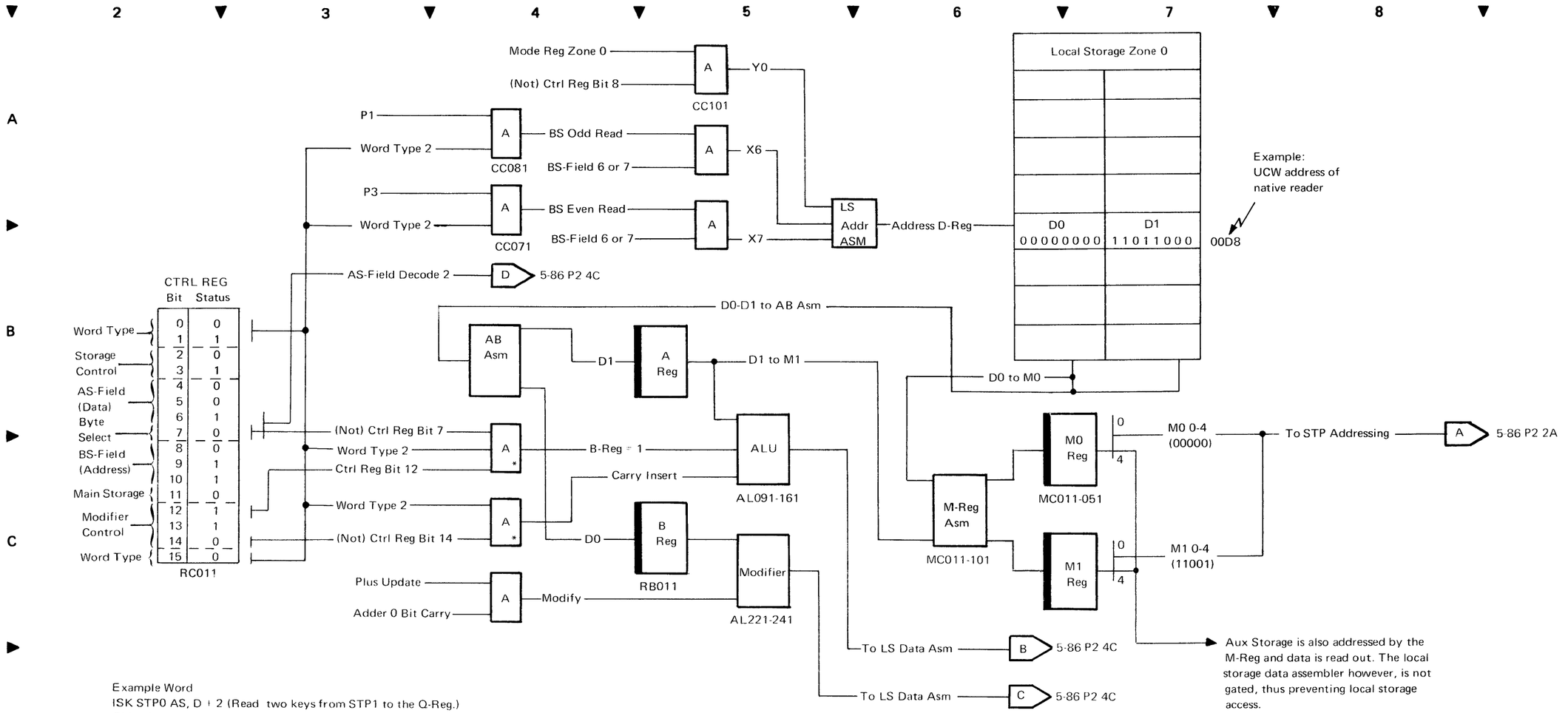
H0=STP0

Objectives:

1. Address *STP0 (Q-Reg in CPU Mode)
2. Gate STP0 to Local Storage
3. Address : H0
4. Write STP0 into H0

E

Diagram 5-86. Storage Word, Insert Storage Key (Word Type 2) (Part 1 of 2)



Example Word
ISK STP0 AS, D + 2 (Read two keys from STP1 to the Q-Reg.)
Objectives:
1. Read the indirect address from D-Register (UCW address) and place in M-Register.
2. Read halfword from auxiliary storage address by M-Reg and block.
3. Read out halfword from STP1 address by M-Register to Q-Register.
4. Update the indirect address by 2.

* The address update by 2 is accomplished by bringing up the carry insert line and the B-Reg line, causing a carry into the bit-6 position of ALU, thus incrementing by 2.

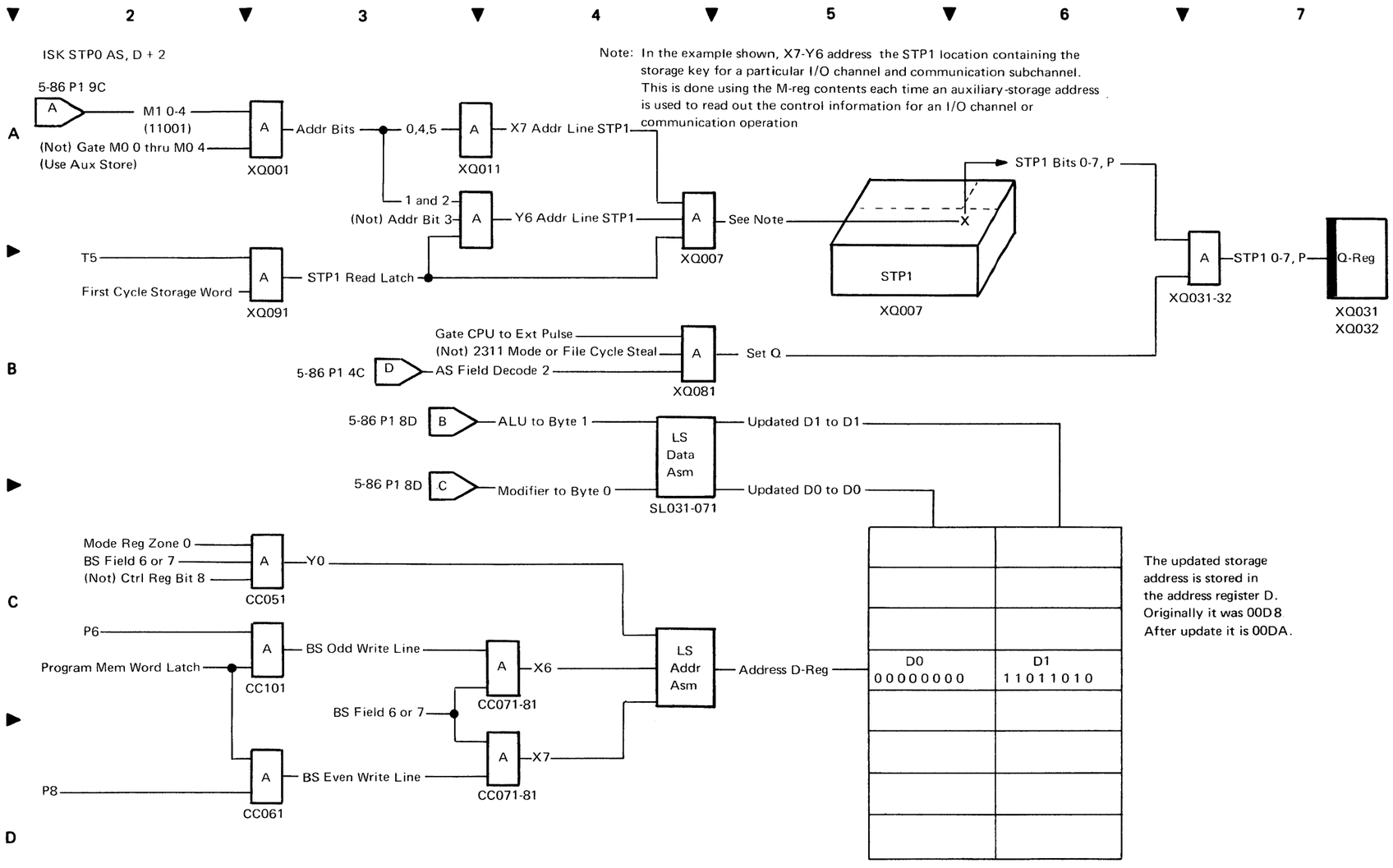
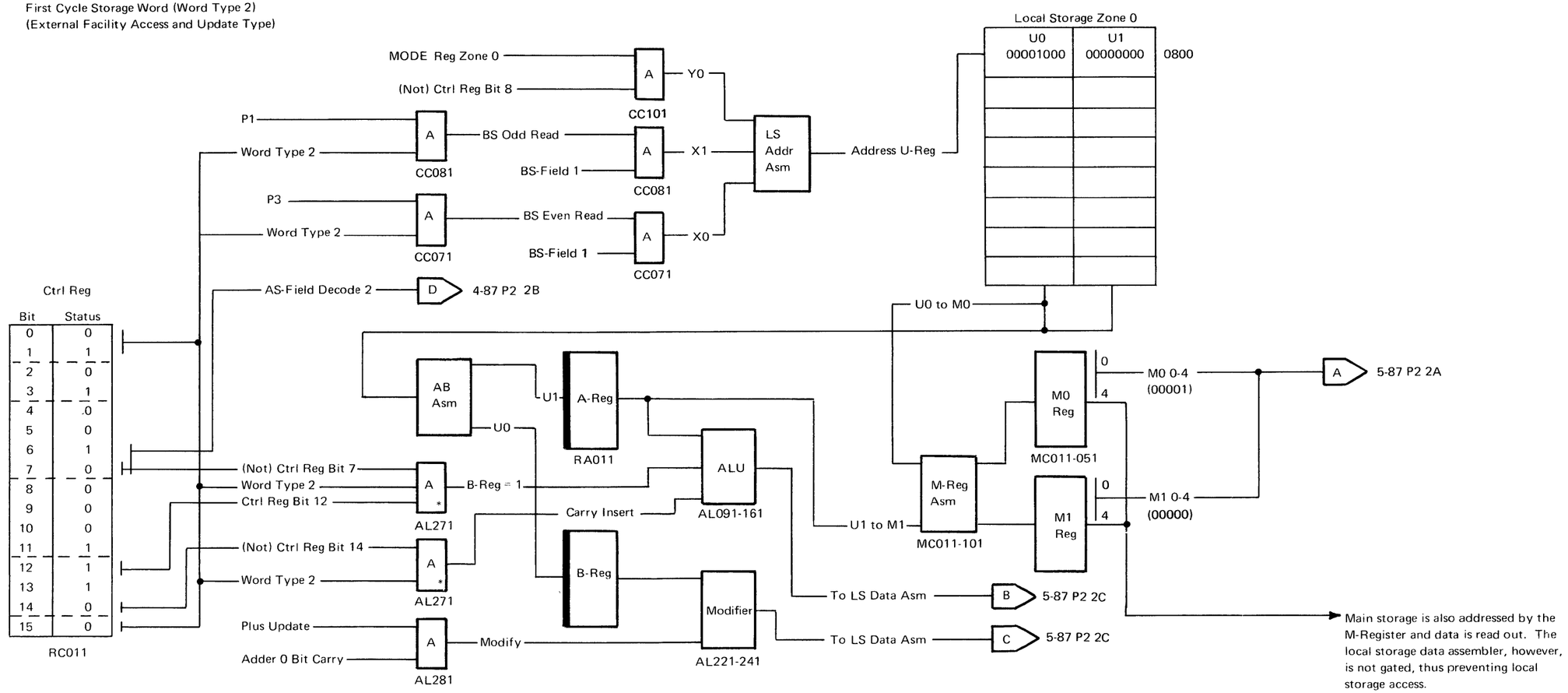

2
3
4
5
6
7
8
9
A
B
C
D
E
ISK STP0 AS, D + 2
5-86 P1 9C
A
M1 0-4
(11001)
(Not) Gate M0 0 thru M0 4
(Use Aux Store)
XQ001
Addr Bits
0,4,5
XQ011
X7 Addr Line STP1
1 and 2
(Not) Addr Bit 3
Y6 Addr Line STP1
XQ007
See Note
Note: In the example shown, X7-Y6 address the STP1 location containing the storage key for a particular I/O channel and communication subchannel. This is done using the M-reg contents each time an auxiliary-storage address is used to read out the control information for an I/O channel or communication operation
STP1 Bits 0-7, P
STP1
XQ007
T5
First Cycle Storage Word
XQ091
STP1 Read Latch
XQ031-32
STP1 0-7, P
Q-Reg
XQ031
XQ032
Gate CPU to Ext Pulse
(Not) 2311 Mode or File Cycle Steal
5-86 P1 4C
D
AS Field Decode 2
XQ081
Set Q
5-86 P1 8D
B
ALU to Byte 1
LS
Data
Asm
SL031-071
Updated D1 to D1
5-86 P1 8D
C
Modifier to Byte 0
Updated D0 to D0
Mode Reg Zone 0
BS Field 6 or 7
(Not) Ctrl Reg Bit 8
CC051
Y0
P6
Program Mem Word Latch
CC101
BS Odd Write Line
X6
CC071-81
BS Field 6 or 7
P8
CC061
BS Even Write Line
X7
CC071-81
LS
Addr
Asm
Address D-Reg
D0
00000000
D1
11011010
The updated storage address is stored in the address register D. Originally it was 00D8. After update it is 00DA.

Diagram 5-87. Stor. Word, Insert Stor. Key Function (Part 1 of 2)

2 3 4 5 6 7 8 9

First Cycle Storage Word (Word Type 2)
(External Facility Access and Update Type)



Example Word
ISK STP0 U + 2 (Read Key from STPL into the Q-Reg)

Objectives;

1. Read the indirect address from U-Register and place in the M-Register (1st Cycle).
2. Read data from program storage and block (1st Cycle).
3. Read out the storage key from STP1 (addressed by the M-Register) into the Q-Register.
4. Update the indirect address by 2.

* The address update by 2 is accomplished by bringing up the carry insert line and the B-Register = 1 line, causing a carry into the Bit-6 position of ALU, thus incrementing by 2.

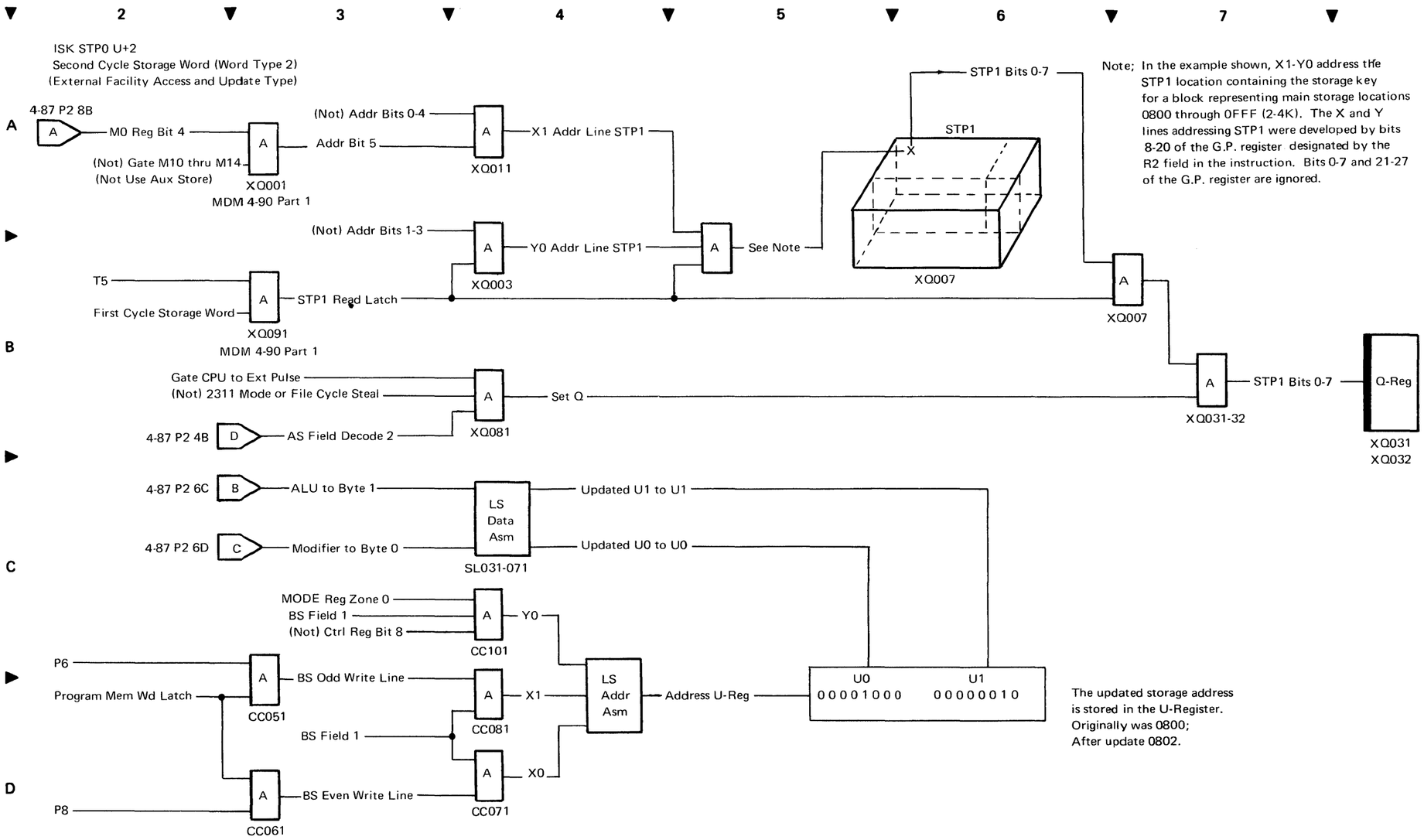
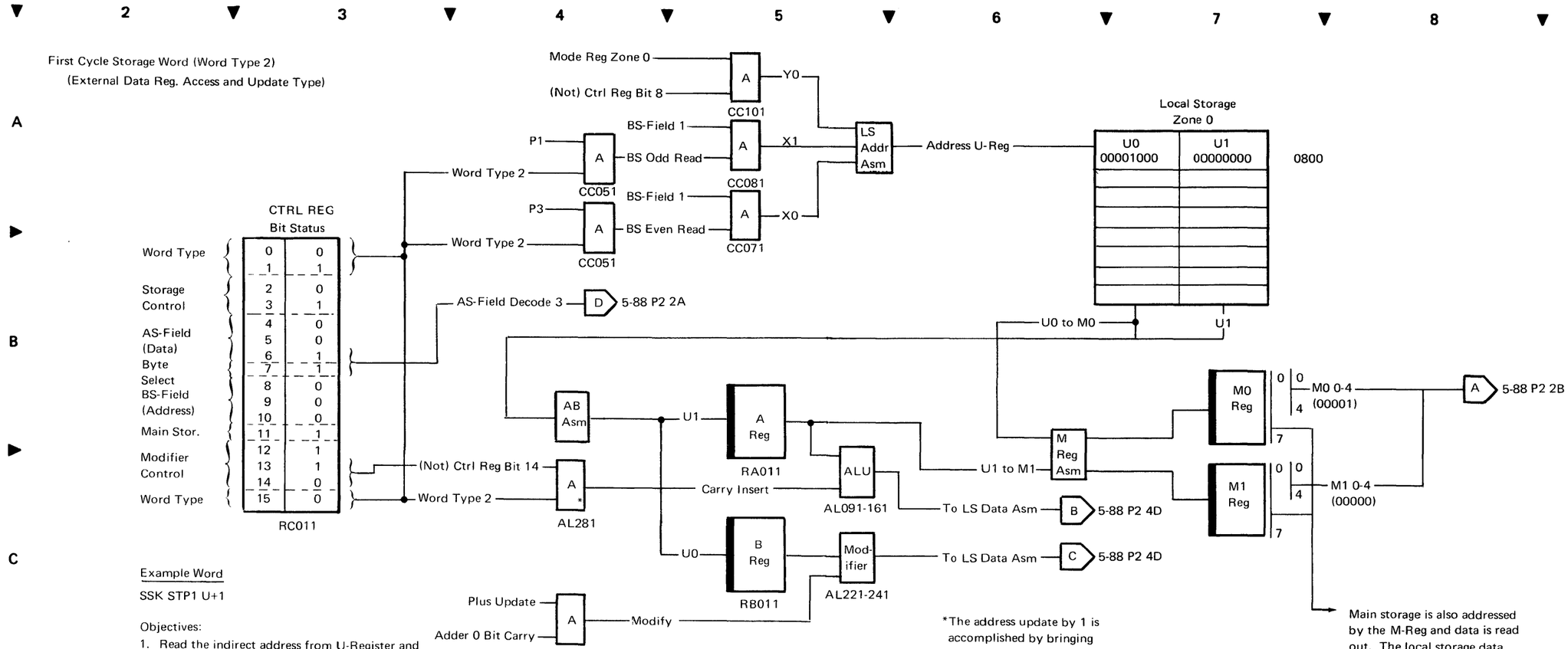

2
3
4
5
6
7
8
9
A
B
C
D
E
ISK STP0 U+2
Second Cycle Storage Word (Word Type 2)
(External Facility Access and Update Type)
4-87 P2 8B
M0 Reg Bit 4
(Not) Gate M10 thru M14
(Not Use Aux Store)
XQ001
MDM 4-90 Part 1
(Not) Addr Bits 0-4
Addr Bit 5
XQ011
X1 Addr Line STP1
(Not) Addr Bits 1-3
Y0 Addr Line STP1
XQ003
See Note
STP1 Bits 0-7
STP1
X
XQ007
T5
First Cycle Storage Word
STP1 Read Latch
XQ091
MDM 4-90 Part 1
XQ007
Gate CPU to Ext Pulse
(Not) 2311 Mode or File Cycle Steal
Set Q
XQ081
4-87 P2 4B
AS Field Decode 2
XQ031-32
STP1 Bits 0-7
Q-Reg
XQ031
XQ032
4-87 P2 6C
ALU to Byte 1
4-87 P2 6D
Modifier to Byte 0
LS
Data
Asm
SL031-071
Updated U1 to U1
Updated U0 to U0
MODE Reg Zone 0
BS Field 1
(Not) Ctrl Reg Bit 8
CC101
Y0
P6
Program Mem Wd Latch
CC051
BS Odd Write Line
BS Field 1
CC081
X1
LS
Addr
Asm
Address U-Reg
U0
0 0 0 0 1 0 0 0
U1
0 0 0 0 0 0 1 0
P8
CC061
BS Even Write Line
CC071
X0
Note; In the example shown, X1-Y0 address the STP1 location containing the storage key for a block representing main storage locations 0800 through 0FFF (2-4K). The X and Y lines addressing STP1 were developed by bits 8-20 of the G.P. register designated by the R2 field in the instruction. Bits 0-7 and 21-27 of the G.P. register are ignored.
The updated storage address is stored in the U-Register. Originally was 0800; After update 0802.

Diagram 5-88. Storage Word, Set Storage Key Function (Word Type 2) (Part 1 of 2)



2 3 4 5 6 7 8 9

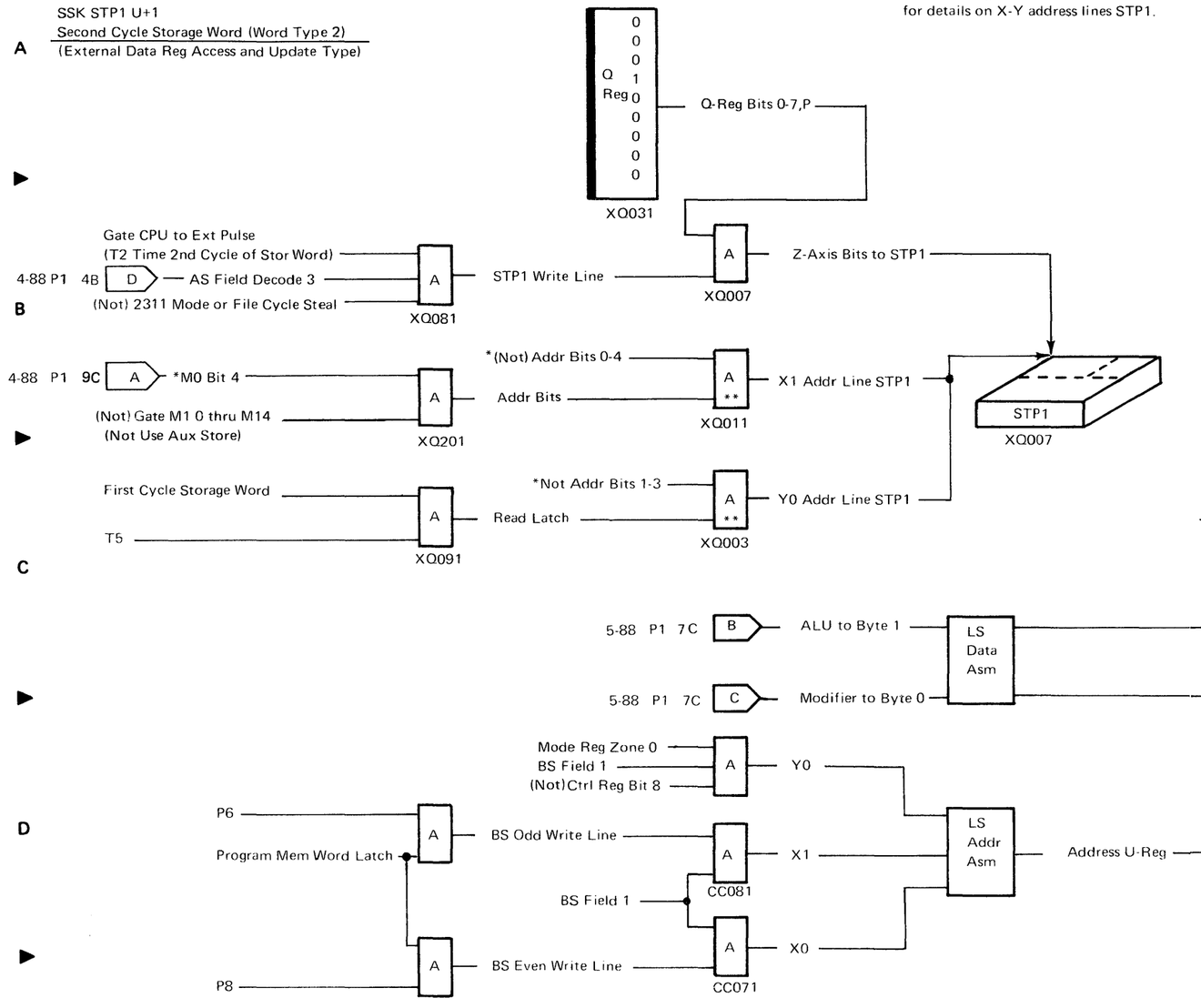
SSK STP1 U+1
Second Cycle Storage Word (Word Type 2)
(External Data Reg Access and Update Type)

**Refer to Diag 4-90 Part 1
for details on X-Y address lines STP1.

*In this example, only M0 bit 4 is active, thus only address bit 5 is developed.

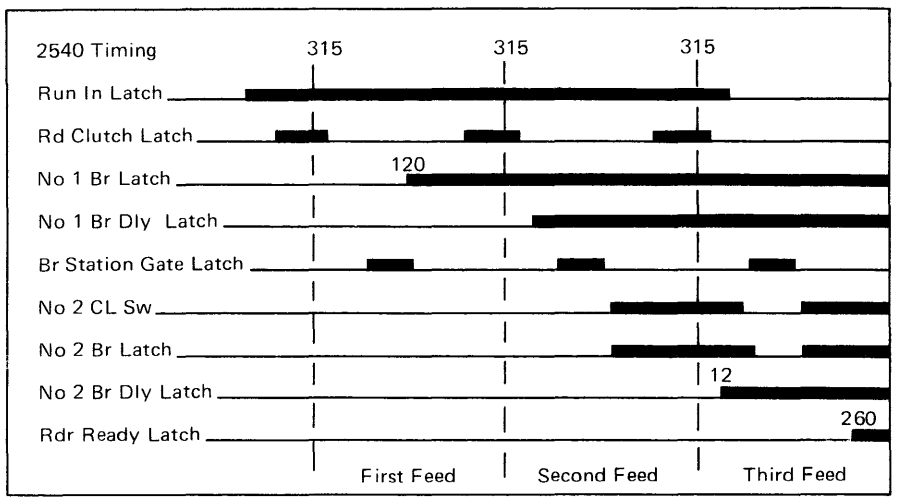
STP1 Storage Allocations

1 Program Storage Keys--X:0-3, Y:0-5, Z:0-3
2 Channel Keys--X:4-7, Y:0-7, Z:0-3
3 Communications Keys--X:4-7, Y:0-7, Z:4-7



Run In Objectives:

Feed three cards into the reader.
Data from first card in the column image buffer.
First card checked for hole count errors.
A Data from second card in the row image buffer.



B

Microroutines | Integrated Control | 2540 | First Feed Cycle

Diag 5-106
Reader trap. Setup row image address and trap counter

Set the rdr clutch latch (MDM 4-102).
This sets the reader-request trap latch. The reader-request trap latch sets the rdr trap inlk latch (MDM 4-102)

Cards ready to feed.
Press START key.
Motor starts
Rd clutch latch energizes and starts a feed cycle

C Return to link adr

Diag 5-106
120 traps (data) are taken. The row image buffer contains 120 bytes; each byte is set to FF.
After the last trap (120) data) set the rdr status req latch.
Set R K=02
Reset rdr cmd inlk
Rst RP K=20
Set the transfer bit

Normal trap operation occurs (see timing chart on MDM 4-111). False read errors are ignored

Card 1 is being fed, reader brush impulses are sent to the control section

D

Set rdr status latch.
Set status req latch at T4 (MDM 4-104).
Rest rdr cmd inlk latch (MDM 4-104).
This resets the read feed latch., stacker select latches and sets the intervention req latch if not set

E Return to link adr

B
Diag 5-101 P2 2G
CICY ISTARTN
Recognize that an interrupt exists (S7=0)

Rdr status request causes the external facility RS bit 6 to indicate a 1.
The external facility: S7 to indicate a 0; BB bit 1 to indicate a 1 (MDM 4-40)

F
CCOM STORHL
Store H1 (H1=00)

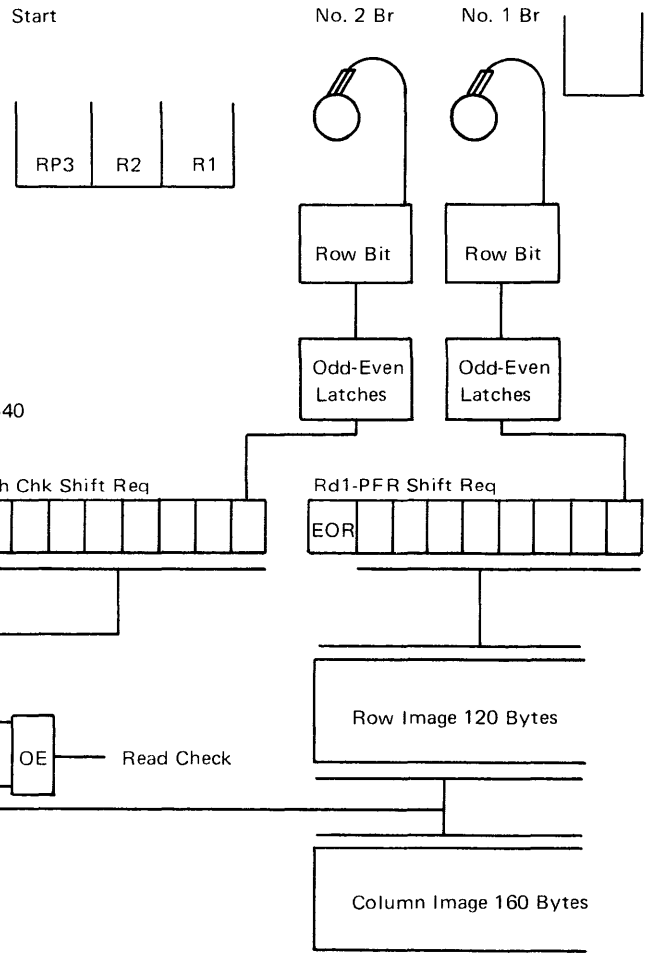
BSWI CHECKB
Set S5 and S4

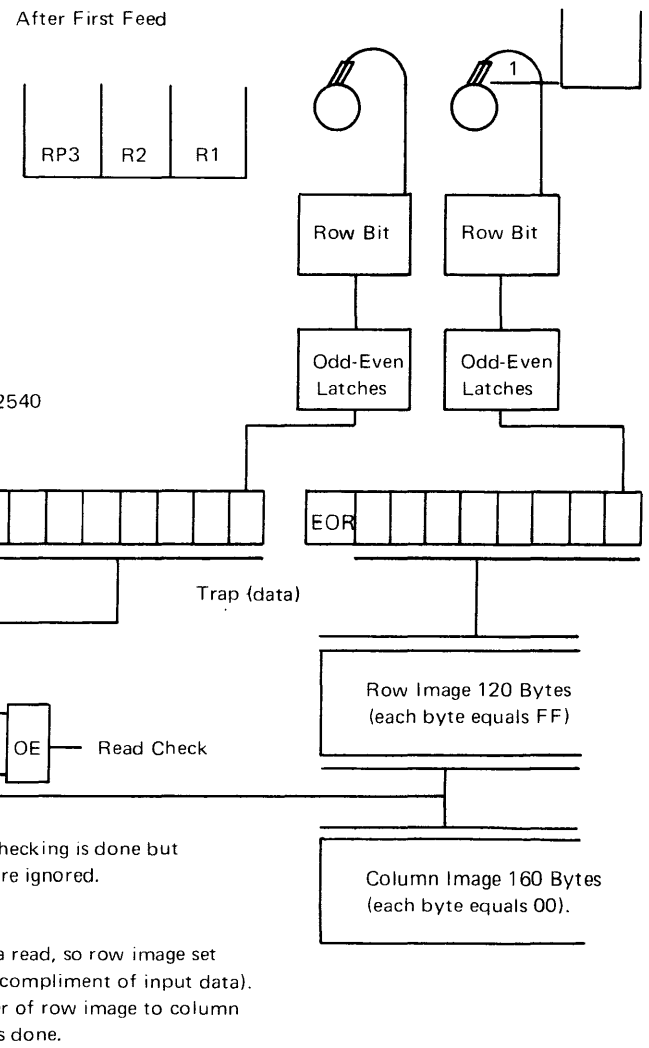
BSWI
Recognize reader status request

G
ERRQ RDST
Readout UCW bytes into local storage registers.
Recognize transfer bit being on.
Reset rdr status and device end.
Rst R K=03

Reset rdr status (MDM 4-104). This resets rdr status, device end and status req

H A
Diag 5-101 P2 2A





Error checking is done but errors are ignored.

No data read, so row image set to FF (compliment of input data). Transfer of row image to column image is done.

Diagram 5-101. Reader Run In (Part 1 of 3)

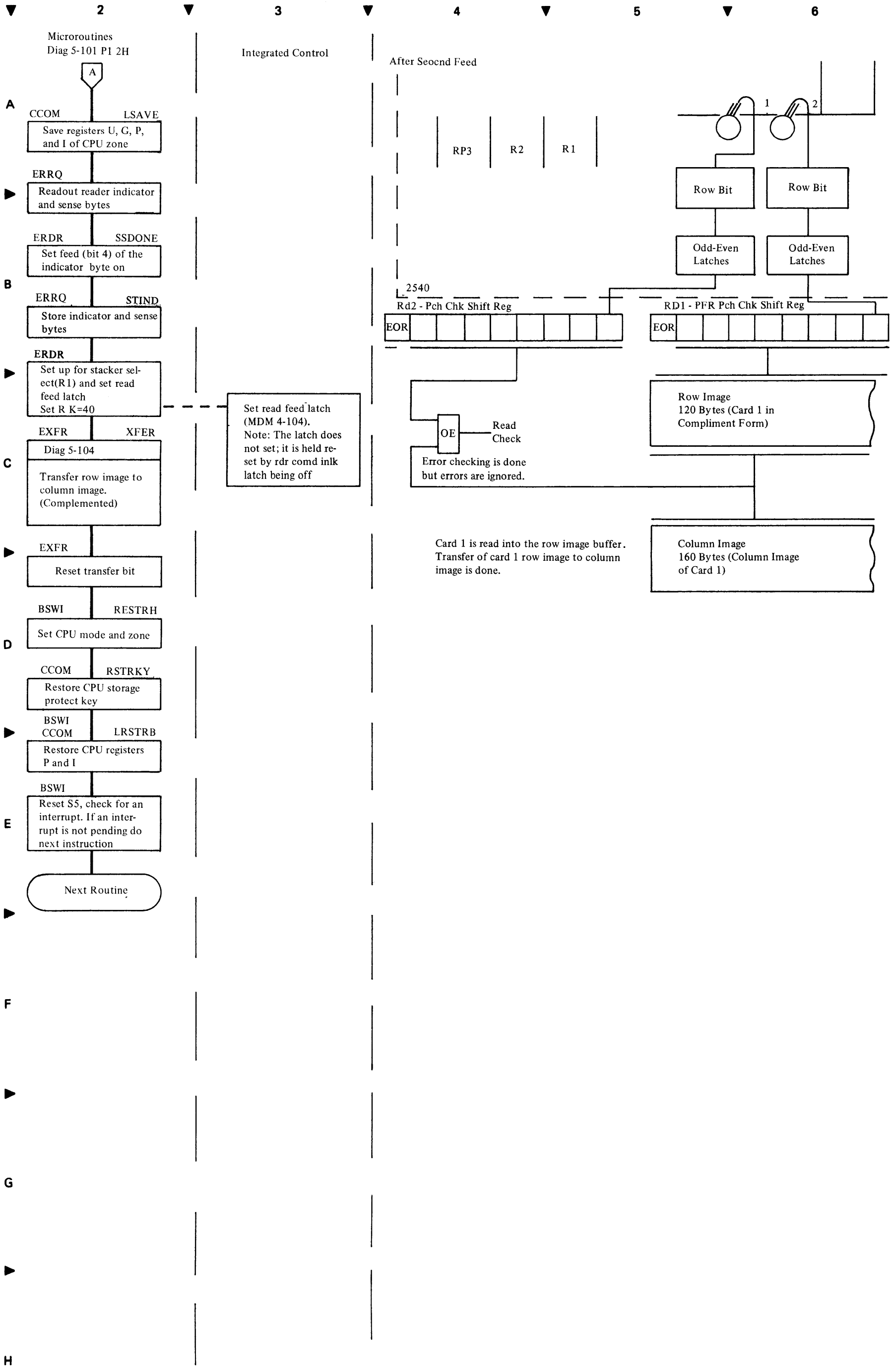


Diagram 5-101. Reader Run-In (Part 2 of 3)

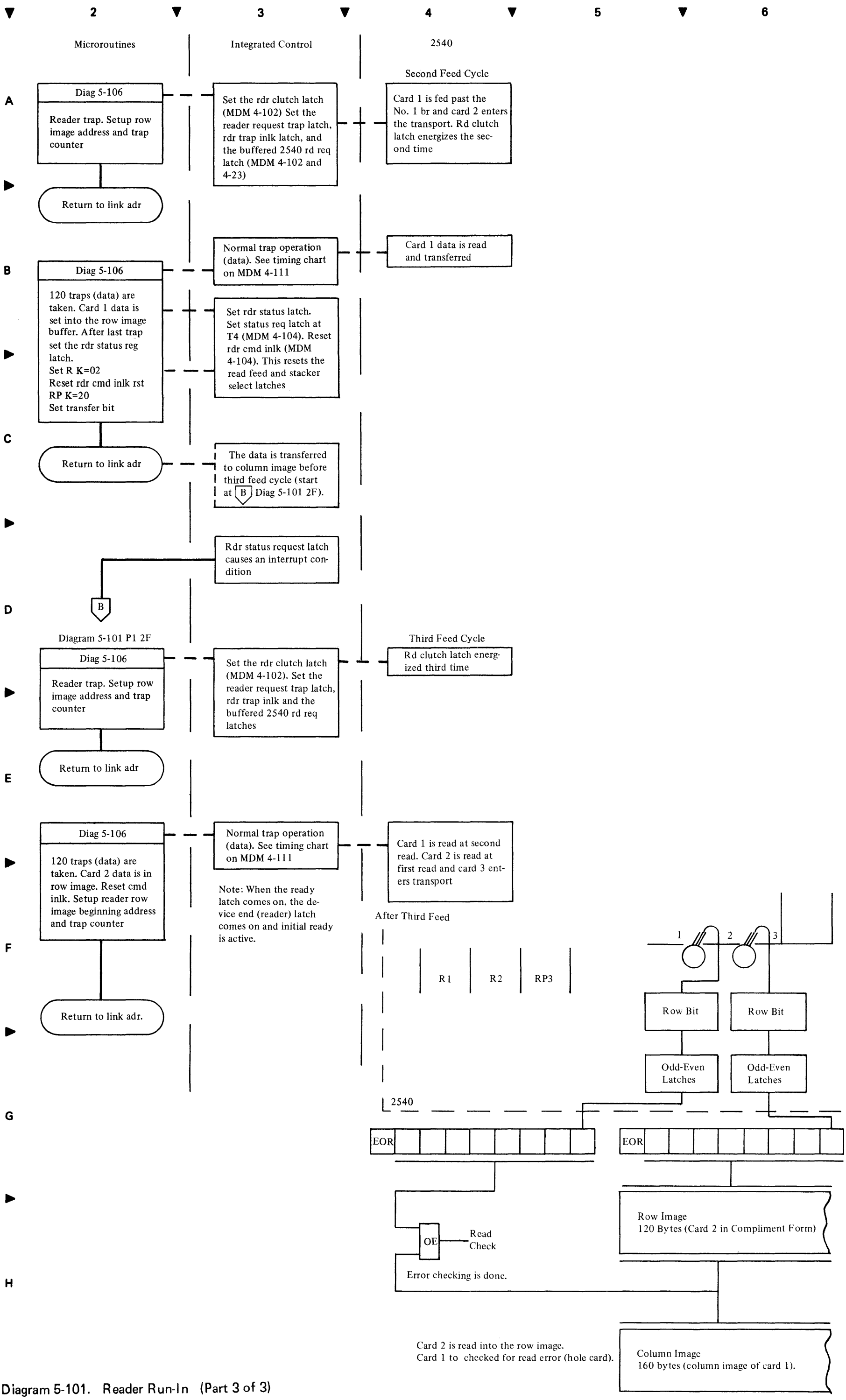
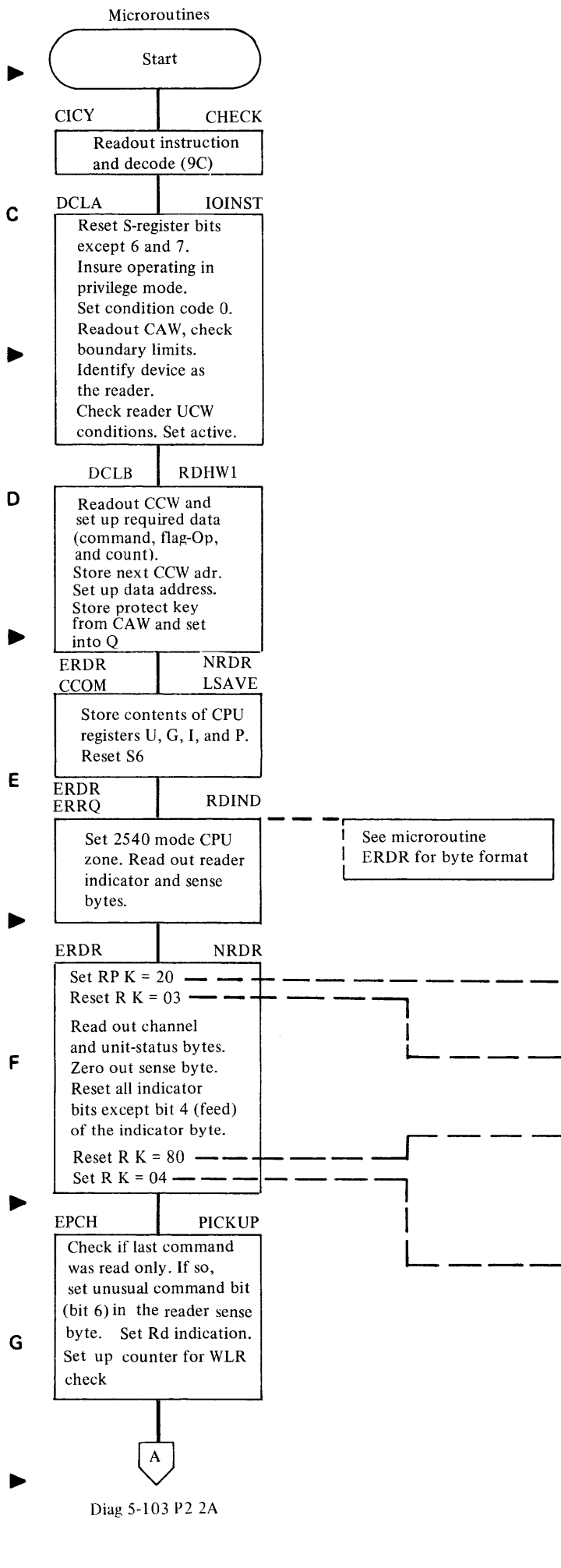


Diagram 5-101. Reader Run-In (Part 3 of 3)

Instruction: Start I/O (9C).
Command: Read and feed, select stacker R2 (Mode 1)

Conditions: First command after run-in.
Status bytes and flag byte clear.
Card 1 data is in column-image buffer.
Card 2 data is in row-image buffer.

Objectives:
1. Set up reader UCW.
2. Set up for read and feed command.
3. Translate card 1 data and store into main storage.
4. Check validity of each character.
5. Set up reader for feed and stacker select.
6. Set channel-end.
7. Start card feed.
8. Transfer (card 2) row-image to column-image.
9. Read card 3 and set into row-image buffer (via traps).
10. Read card 2 from second read brushes and compare to information read out of row-image for card 1.
11. Set reader check if one occurs.
12. Set device-end, reset reader command and SS latches.



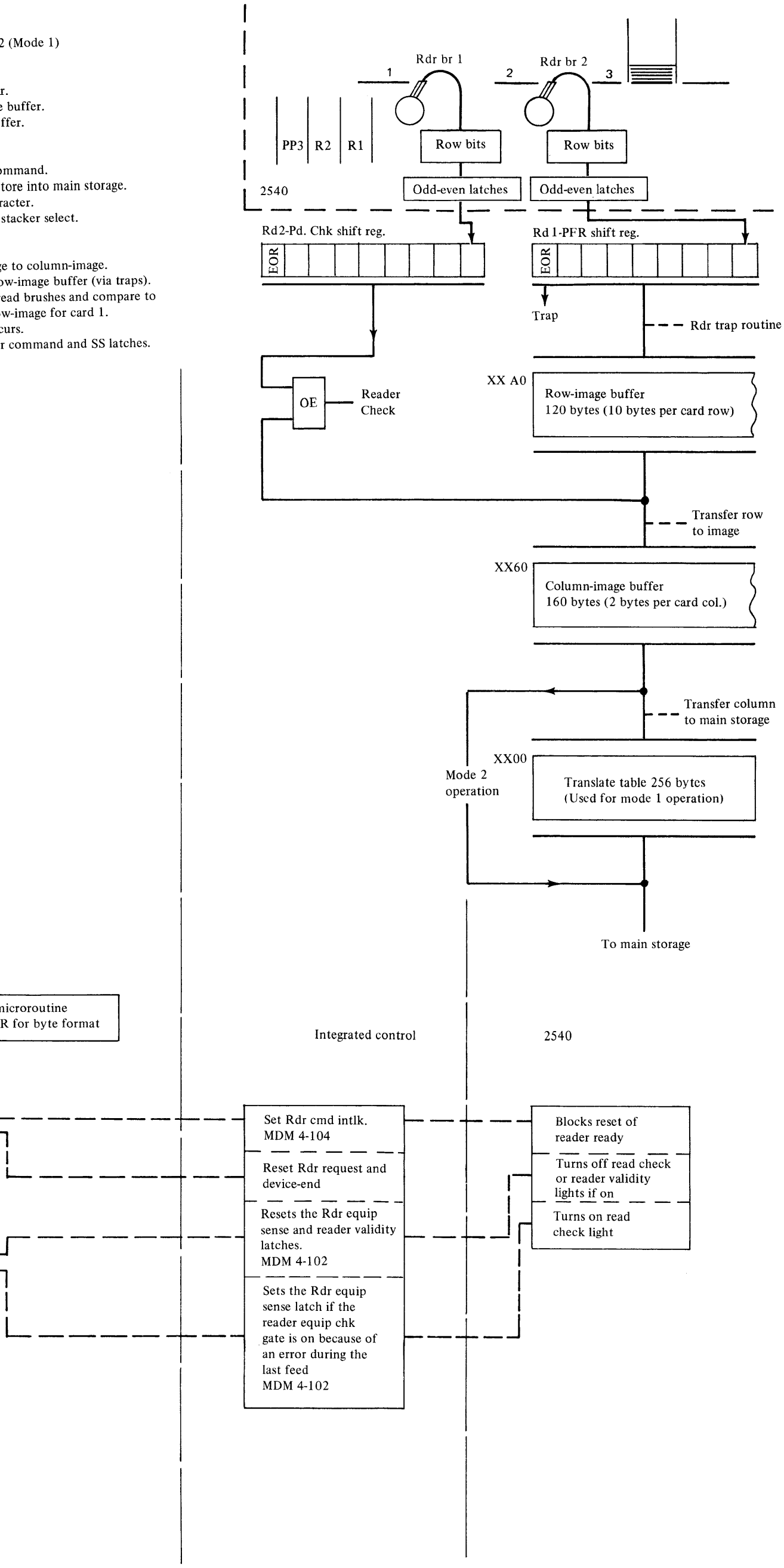


Diagram 5-103. Read Feed and Stacker Select (Reader) (Part 1 of 3)

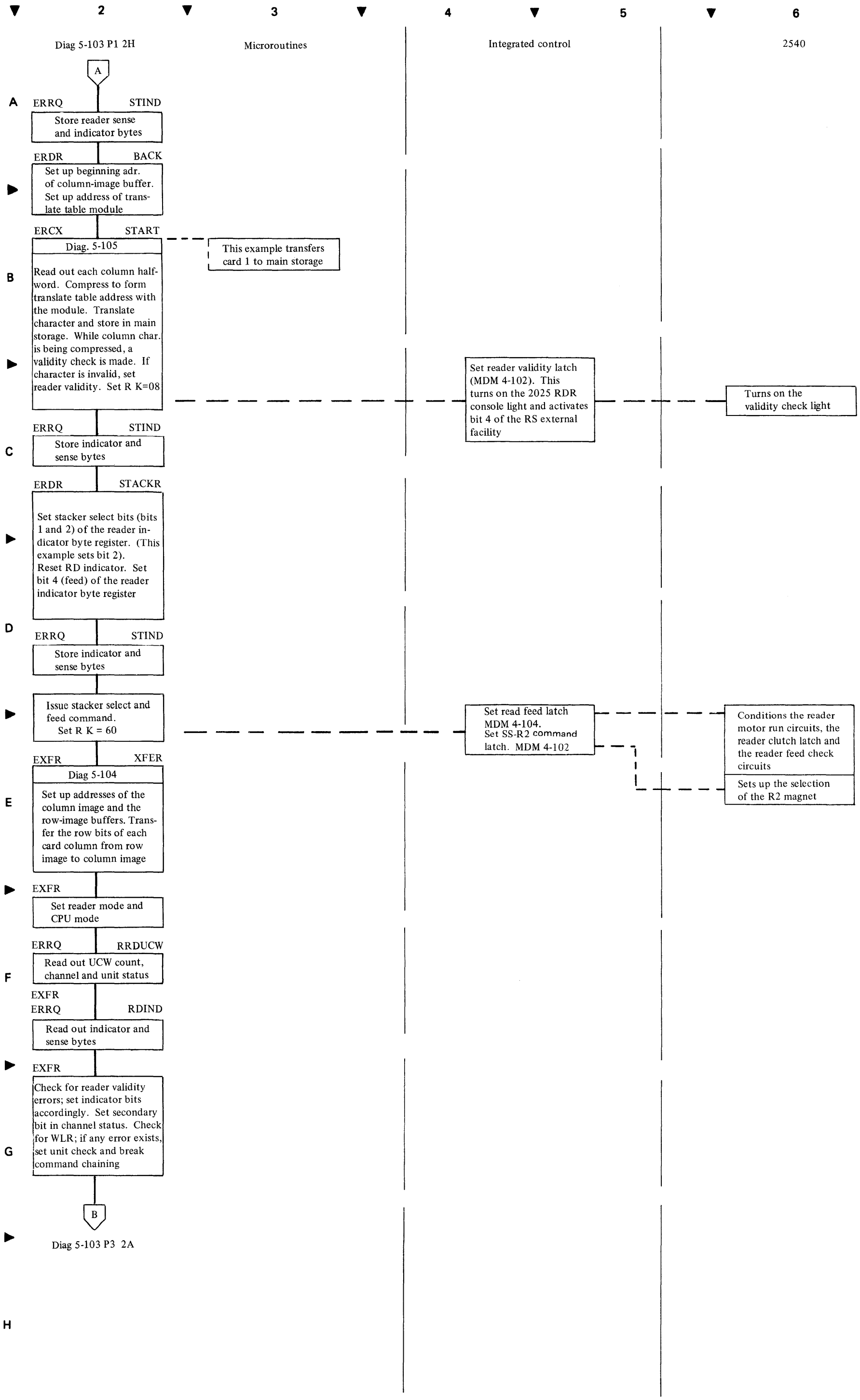


Diagram 5-103. Read Feed and Stacker Select (Part 2 of 3)

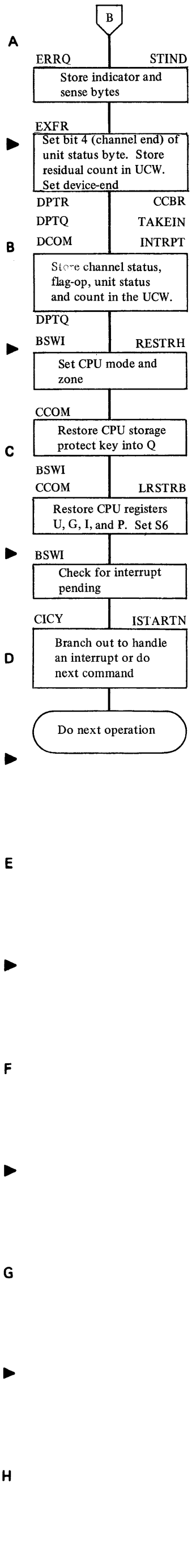
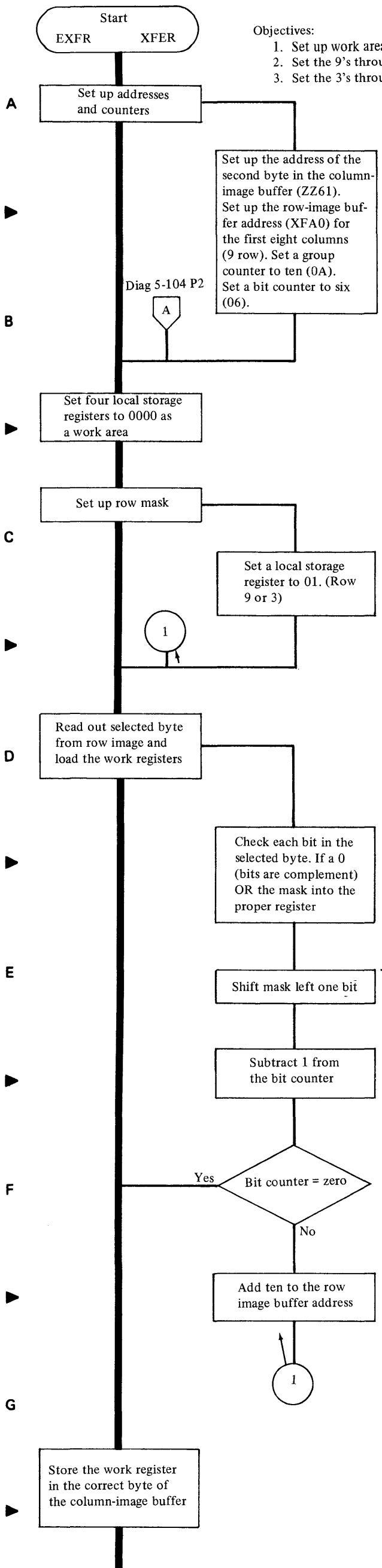
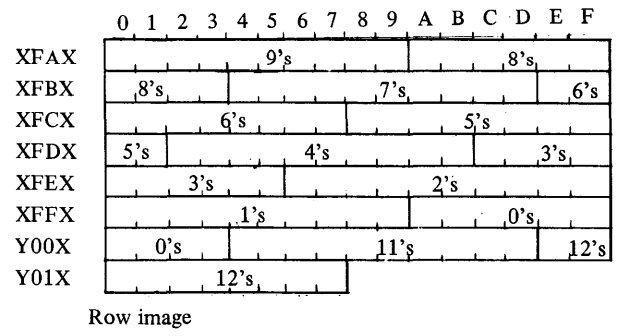
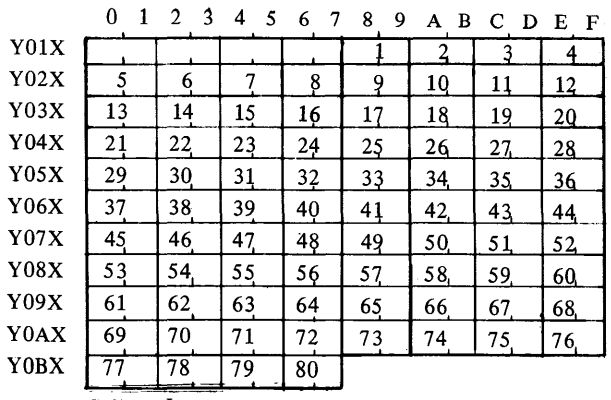


Diagram 5-103. Read Feed and Stacker Select (Part 3 of 3)





Row image



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Y01X									1	2	3	4				
Y02X	5	6	7	8	9	10	11	12								
Y03X	13	14	15	16	17	18	19	20								
Y04X	21	22	23	24	25	26	27	28								
Y05X	29	30	31	32	33	34	35	36								
Y06X	37	38	39	40	41	42	43	44								
Y07X	45	46	47	48	49	50	51	52								
Y08X	53	54	55	56	57	58	59	60								
Y09X	61	62	63	64	65	66	67	68								
Y0AX	69	70	71	72	73	74	75	76								
Y0BX	77	78	79	80												

Column Image

Example:
First eight columns contain A, b1, TEST b1 I - - - -

Row-image address	contains
XFA0	FE - 1111 1110
XFAA	FF - 1111 1111
XFB4	FF - 1111 1111
XFBE	FF - 1111 1111
XFC8	EF - 1110 1111
XFD2	FF - 1111 1111
XFDC	DB - 1101 1011
XFE6	F7 - 1111 0111
XFF0	7F - 0111 1111
XFFA	D3 - 1101 0011
Y004	FF - 1111 1111
Y00E	6E - 0110 1110

Work registers after loaded with 9's through 4's for columns 1 through 8.

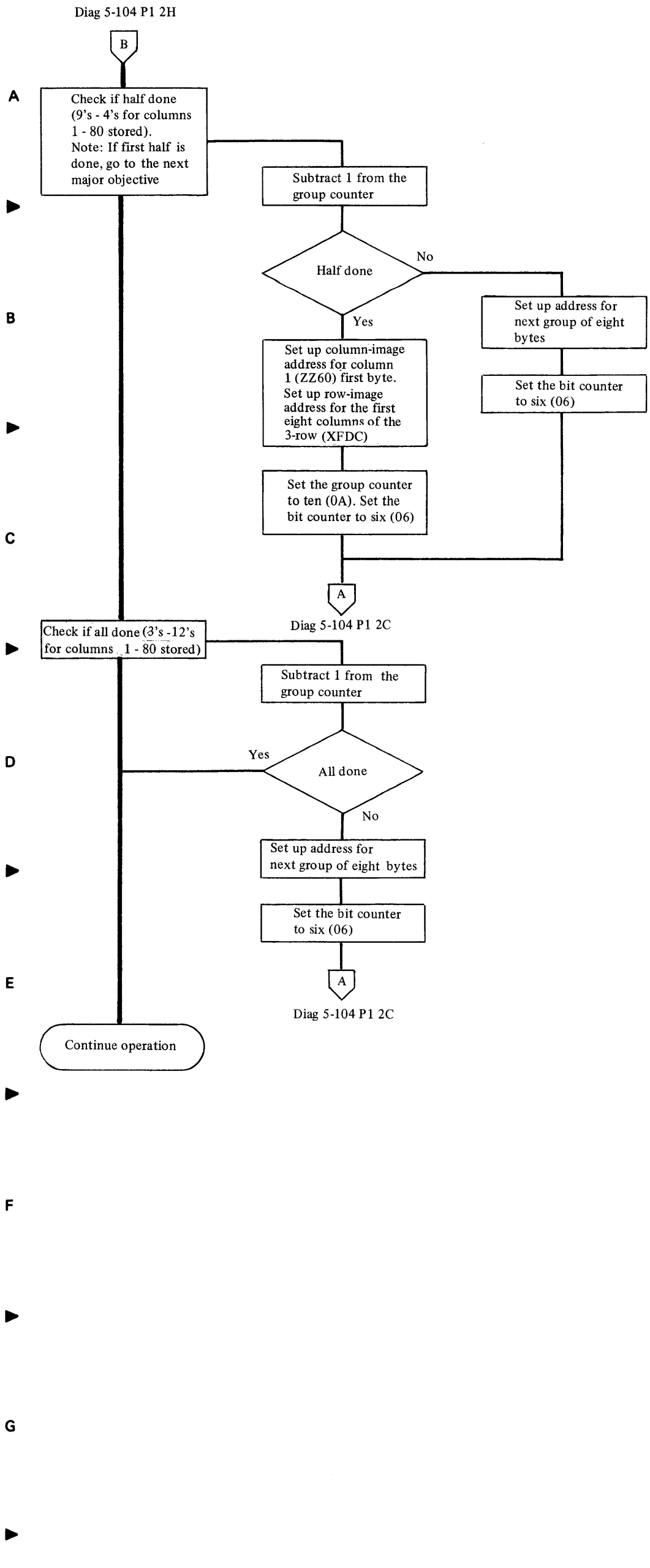
Byte 0	Byte 1		Byte 0	Byte 1
00010000	00000001	R1	Col. 4	Col. 8
00000000	00000000	R2	Col. 3	Col. 7
00000000	00000000	R3	Col. 2	Col. 6
00000000	00000000	R4	Col. 1	Col. 5

Store work registers into column image.

Work Register	Byte into	Column-image Adr
R - 4	0	Y019
R 3	0	Y01B
R 2	0	Y01D
R 1	0	Y01F
R 4	1	Y021
R 3	1	Y023
R 2	1	Y025
R 1	1	Y027

(continued in Part 2)

Diagram 5-104. Row Image to Column Image (Part 1 of 2)



Example (continued from Part 1)

Work registers loaded with 3's through 12's for columns 1 through 8.

Byte 0	Byte 1		Byte 0	Byte 1
00100000	00100000	R1	Col. 4	Col. 8
00001001	00000000	R2	Col. 3	Col. 7
00000000	00001001	R3	Col. 2	Col. 6
00100100	00001010	R4	Col. 1	Col. 5

Store work register into column image.
Work register - byte into column-image adr.

R4	0	Y01B
R3	0	Y018
R2	0	Y01C
R1	0	Y01E
R4	1	Y020
R3	1	Y022
R2	1	Y024
R1	1	Y027

Column-image buffer for first eight columns contents (in hex):

	Col 1		Col 2		Col 3		Col 4	
0 1	2 3	4 5	6 7	8 9	A B	C D	E F
				2400	0000	0900	2010
0A00	0900	0000	2001				
Col 5	Col 6	Col 7	Col 8	Col 9			

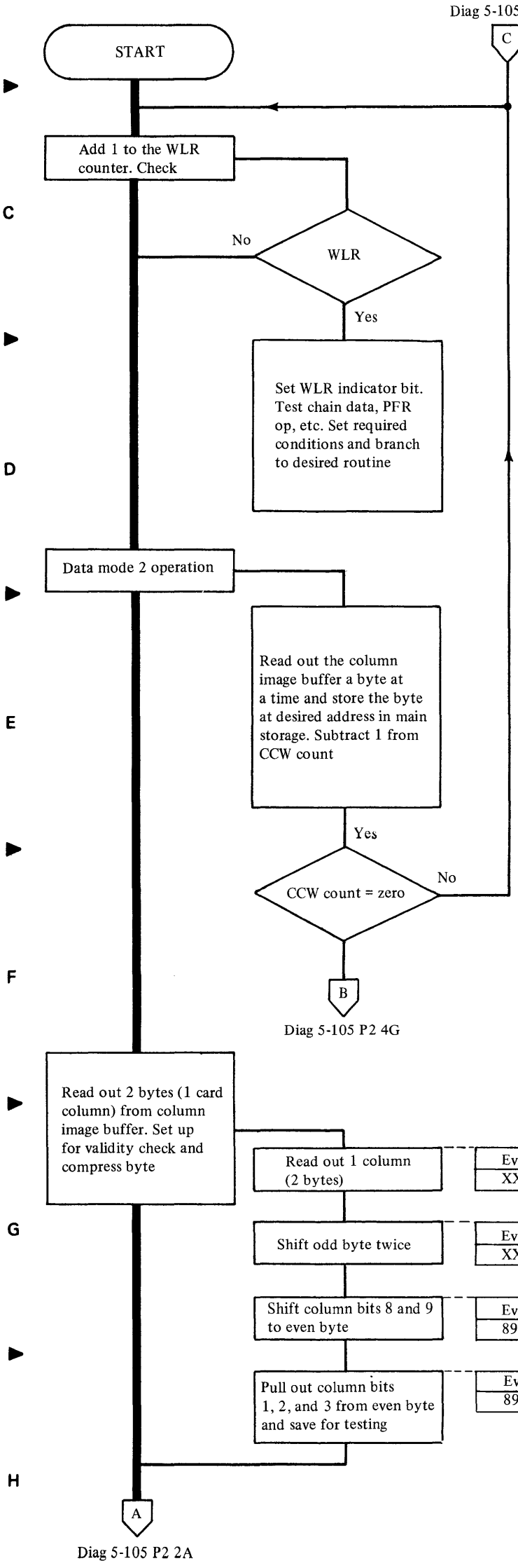
Diagram 5-104. Row Image to Column Image (Part 2 of 2)

Objectives:

Mode 1 -
1. Check column-image character for validity (2 bytes).
2. Compress column-image character to develop translate table address.
3. Store translated character at desired location in main storage.
4. Check for wrong length record.

Mode 2 -
1. Read out column-image buffer 1 byte at a time and store in main storage at the desired location.
2. Check for wrong length record.

Diag 5-105 P2 2G



Diag 5-105 P2 2A

	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	X	X	12	11	0	1	2	3	X	X	4	5	6	7	8	9

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Y01X	-	-	-	-	1	2	3	4								
Y02X	5	6	7	8	9	10	11	12								
Y03X	13	14	15	16	17	18	19	20								
Y04X	21	22	23	24	25	26	27	28								
Y05X	29	30	31	32	33	34	35	36								
Y06X	37	38	39	40	41	42	43	44								
Y07X	45	46	47	48	49	50	51	52								
Y08X	53	54	55	56	57	58	59	60								
Y09X	61	62	63	64	65	66	67	68								
Y0AX	69	70	71	72	73	74	75	76								
Y0BX	77	78	79	80	-	-	-	-								

Column image

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
XX0X	40	F1	F2	F3	F4	F5	F6	F7	F0	61	E2	E3	E4	E5	E6	E7
XX1X	61	D1	D2	D3	D4	D5	D6	D7	D0	A1	A2	A3	A4	A5	A6	A7
XX2X	50	C1	C2	C3	C4	C5	C6	C7	C0	81	82	83	84	85	86	87
XX3X	6A	91	92	93	94	95	96	97	70	B1	B2	B3	B4	B5	B6	B7
XX4X	F9	31	32	33	34	35	36	37	E9	21	22	23	24	25	26	27
XX5X	D9	11	12	13	14	15	16	17	A9	E1	62	63	64	65	66	67
XX6X	C9	01	02	03	04	05	06	07	89	41	42	43	44	45	46	47
XX7X	99	51	52	53	54	55	56	57	B9	71	72	73	74	75	76	77
XX8X	F8	79	7A	7B	7C	7D	7E	7F	E8	69	E0	6B	6C	6D	6E	6F
XX9X	D8	59	5A	5B	5C	5D	5E	5F	A8	A0	AA	AB	AC	AD	AE	AF
XXAX	C8	49	4A	4B	4C	4D	4E	4F	88	80	8A	8B	8C	8D	8E	8F
XXBX	98	90	9A	9B	9C	9D	9E	9F	B8	B0	BA	BB	BC	BD	BE	BF
XXCX	38	39	3A	3B	3C	3D	3E	3F	28	29	2A	2B	2C	2D	2E	2F
XXDX	18	19	1A	1B	1C	1D	1E	1F	68	20	EA	EB	EC	ED	EE	EF
XXEX	08	09	0A	0B	0C	0D	0E	0F	48	00	CA	CB	CC	CD	CE	CF
XXFX	58	10	DA	DB	DC	DD	DE	DF	78	30	FA	FB	FC	FD	FE	FF

2540 Reader translate table (hex code)

Example:
Mode 1 operation, card column contains a period (12 - 3 - 8).

Even byte	Odd byte
00100001	00000010

Even byte	Odd byte
00100001	00001000

Even byte	Odd byte
10100001	00001000

Even byte	Odd byte
10100000	00001000

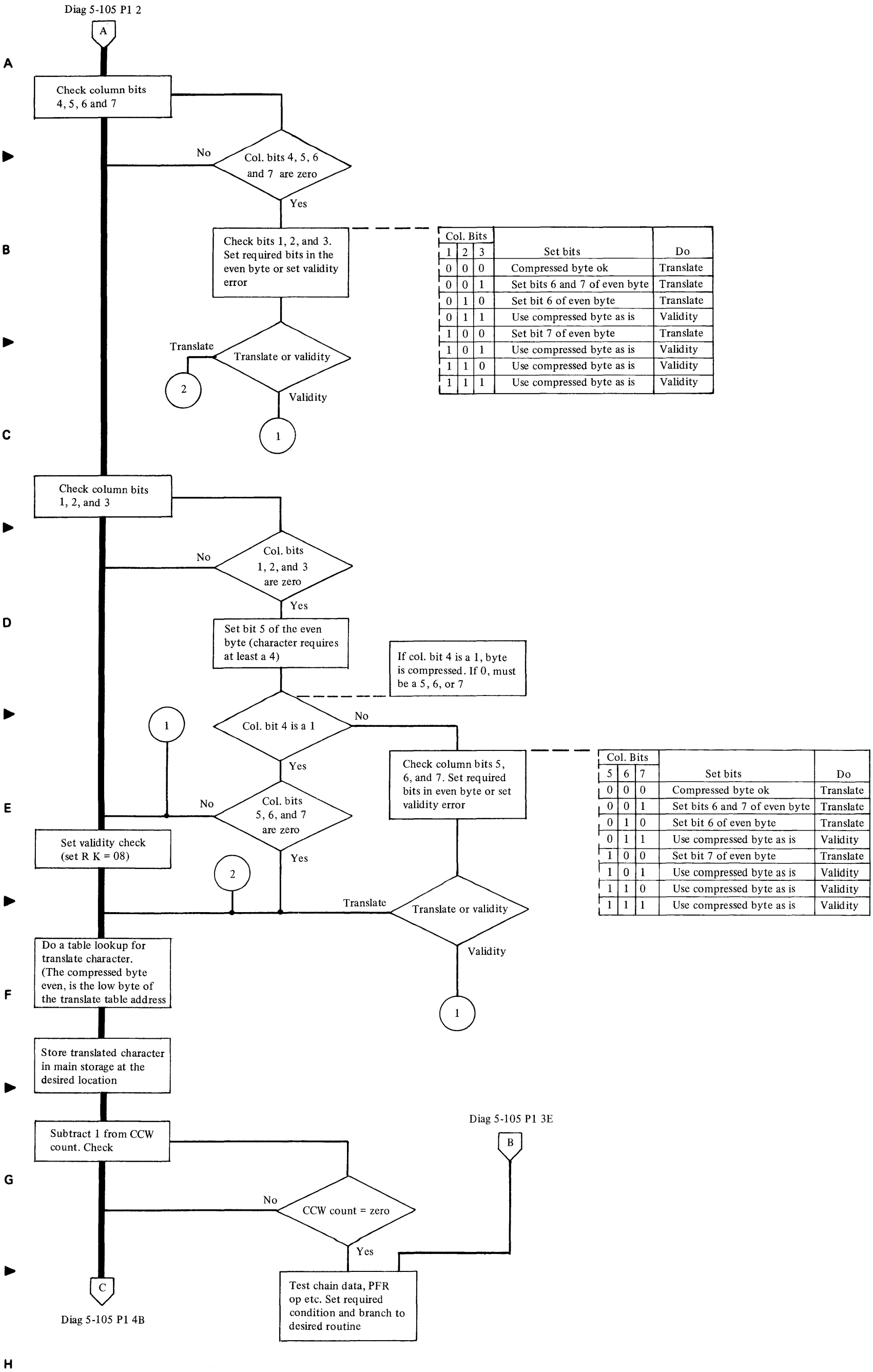
Set even byte bits 6 and 7

Even byte	Odd byte
10100011	00001000

Column Bits 123		
0	0	1

Even byte is the compressed byte that forms the translate table low two hex address digits. For this example it is A3, which reads out a hex code of 4B. Hex code for a period is 4B.

Diagram 5-105. Read Column Image to Storage (Part 1 of 2)



Col. Bits			Set bits	Do
1	2	3		
0	0	0	Compressed byte ok	Translate
0	0	1	Set bits 6 and 7 of even byte	Translate
0	1	0	Set bit 6 of even byte	Translate
0	1	1	Use compressed byte as is	Validity
1	0	0	Set bit 7 of even byte	Translate
1	0	1	Use compressed byte as is	Validity
1	1	0	Use compressed byte as is	Validity
1	1	1	Use compressed byte as is	Validity

Col. Bits			Set bits	Do
5	6	7		
0	0	0	Compressed byte ok	Translate
0	0	1	Set bits 6 and 7 of even byte	Translate
0	1	0	Set bit 6 of even byte	Translate
0	1	1	Use compressed byte as is	Validity
1	0	0	Set bit 7 of even byte	Translate
1	0	1	Use compressed byte as is	Validity
1	1	0	Use compressed byte as is	Validity
1	1	1	Use compressed byte as is	Validity

Diagram 5-105. Read Column Image to Storage (Part 2 of 2)

1. Condition:
   Clutch is energized to feed a card.

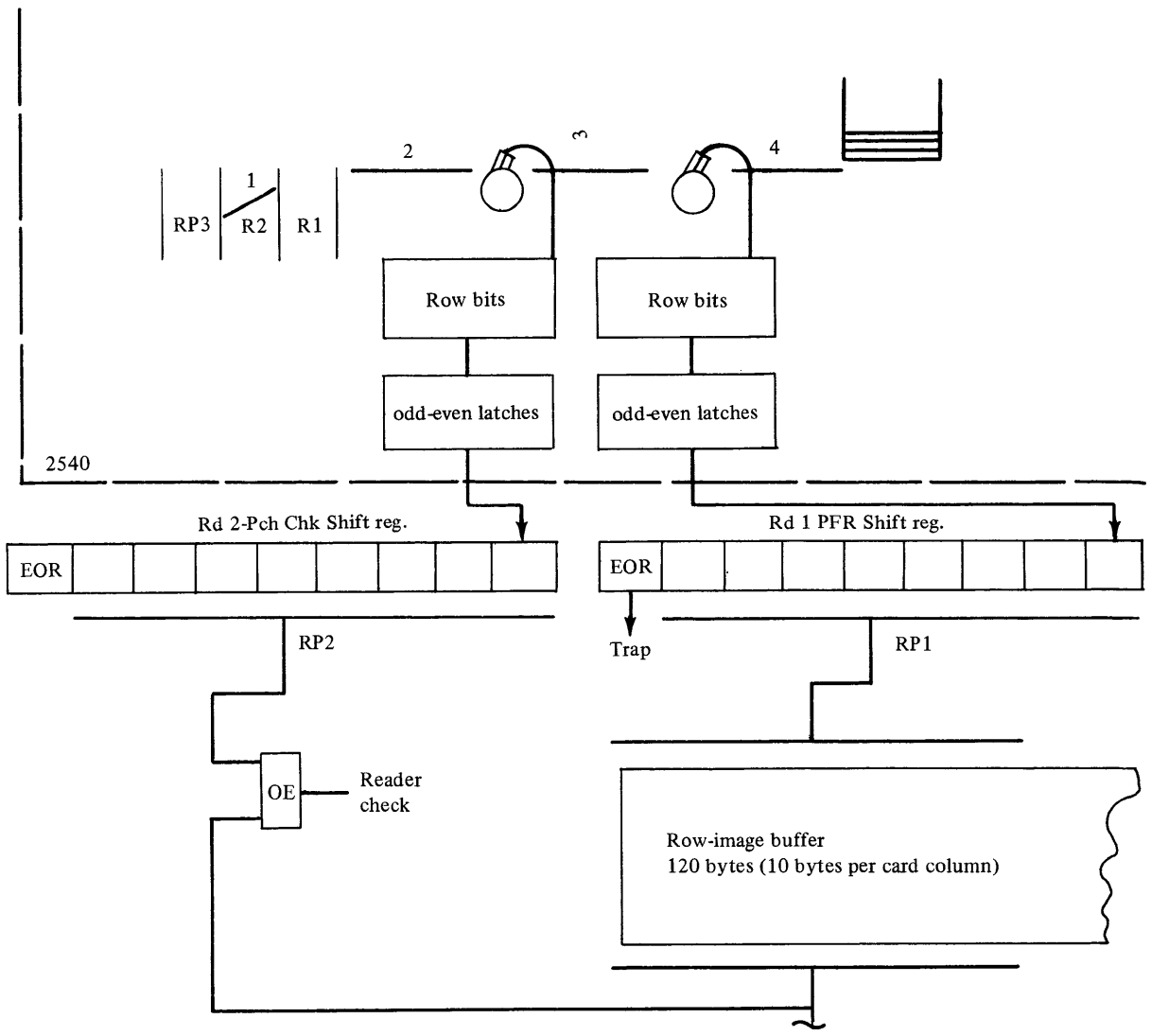
   Objectives:
   Set reader trap.
   Set up row-image address.
   Set up trap counter.

2. Condition:
   Run-in (data).

   Objectives:
   Set up conditions to force row image transfer to column image for first two feed cycles.

3. Condition:
   After Run-in (data).

   Objectives:
   Transfer shift registers to row image.



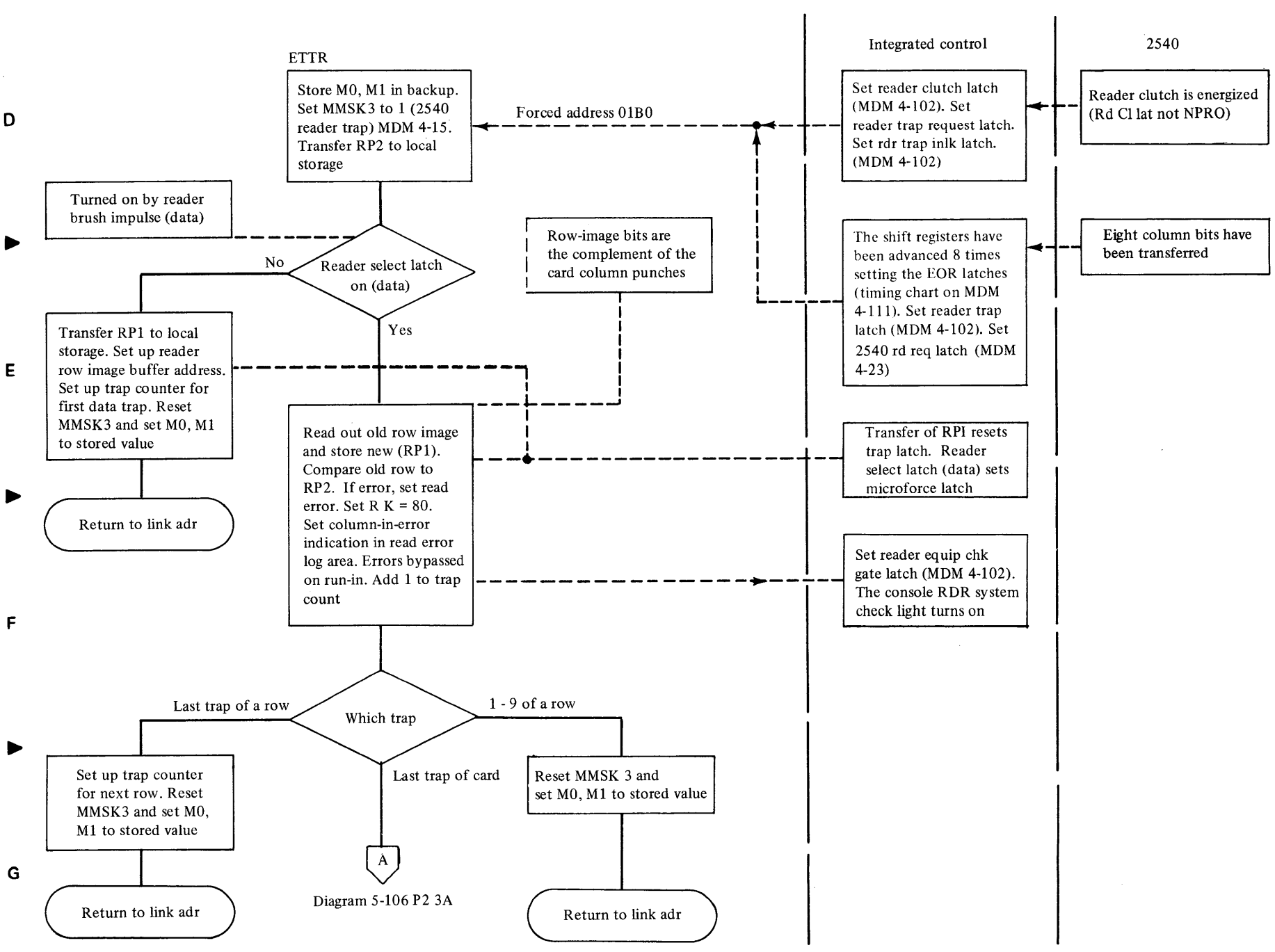


Diagram 5-106. Reader Trap (Part 1 of 2)

Diag 5-106 P130

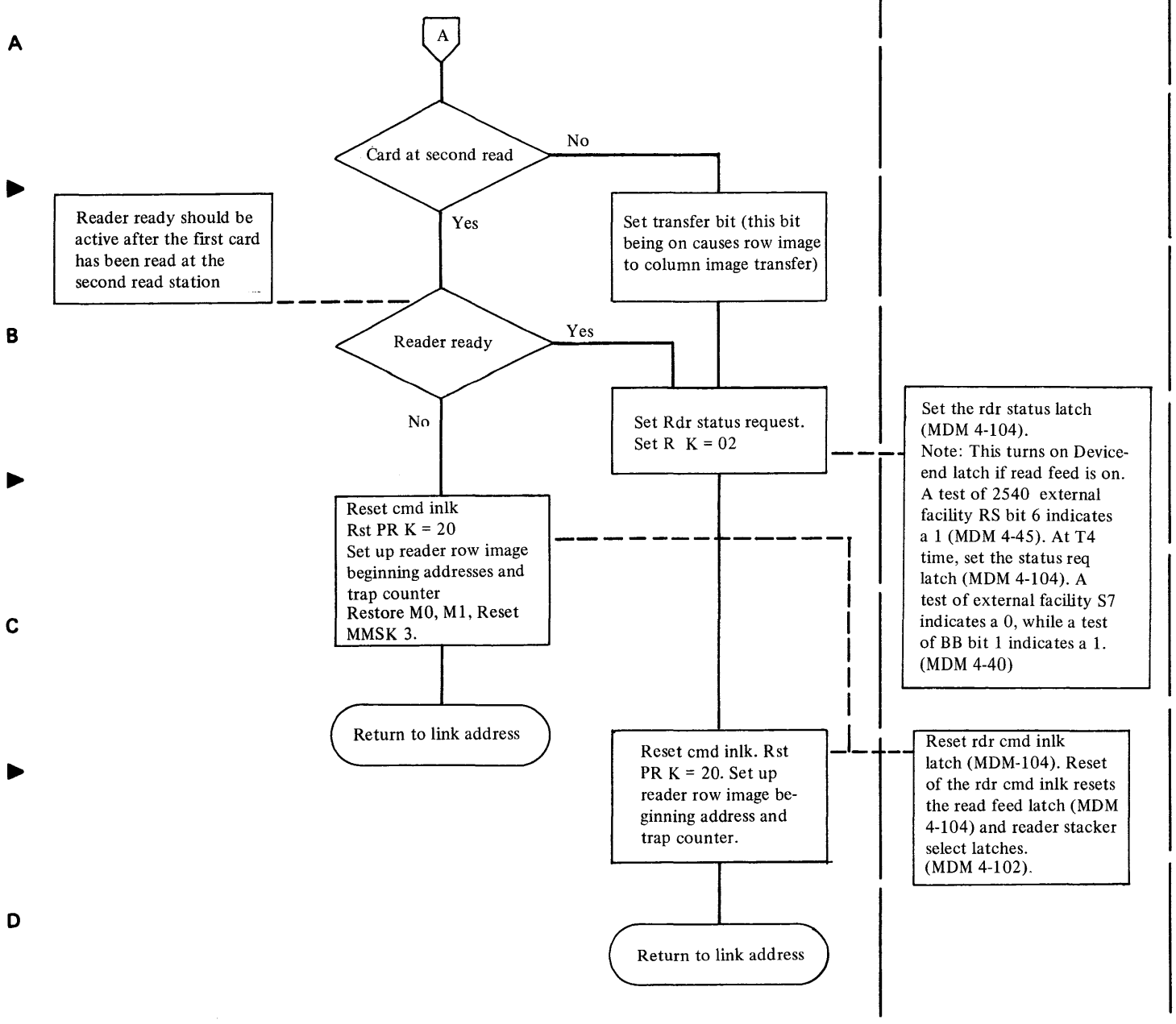


Diagram 5-106. Reader Trap (Part 2 of 2)

Objective: Handle status (channel-end and/or device-end) except for IPL on the reader or punch.

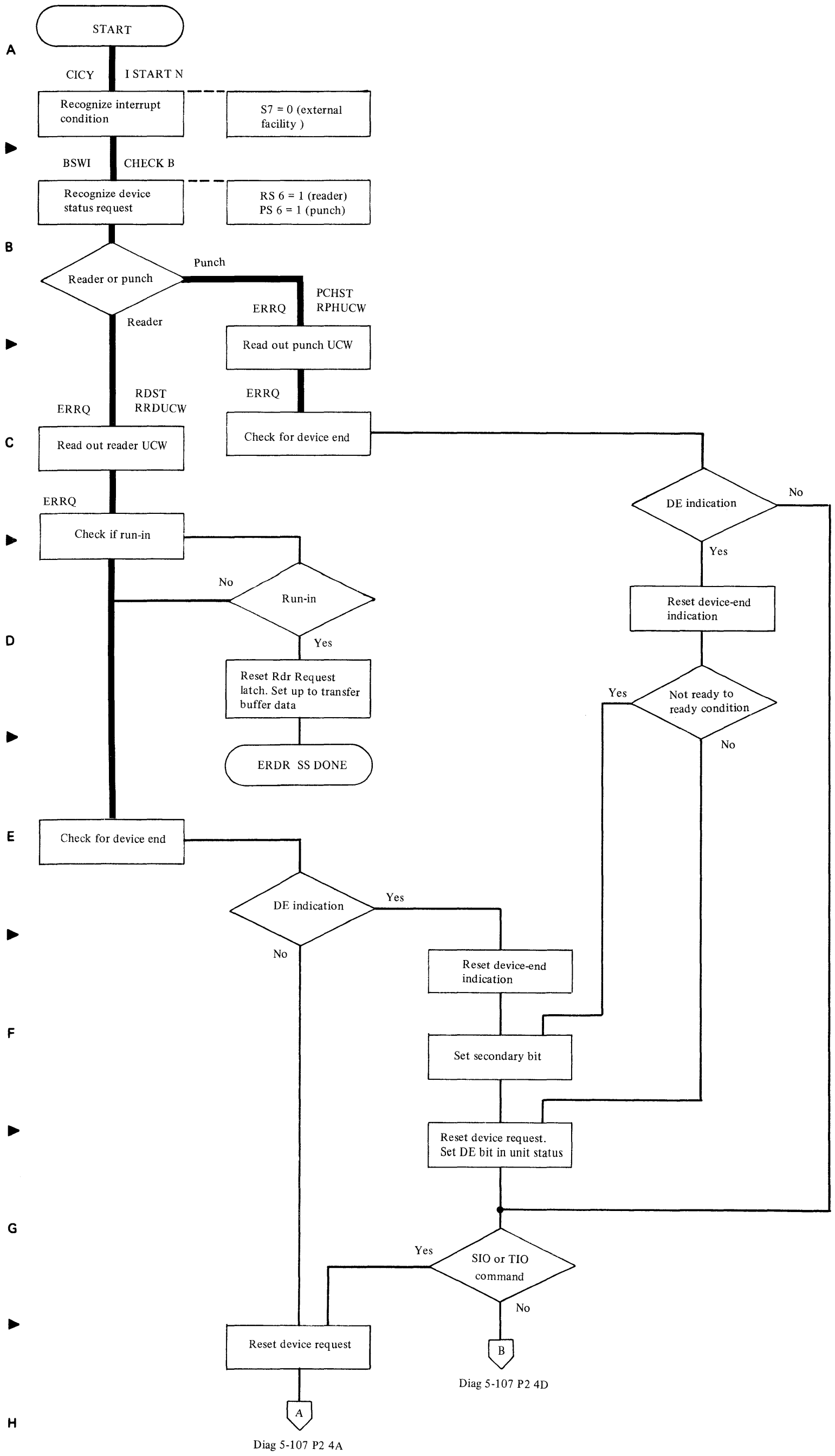
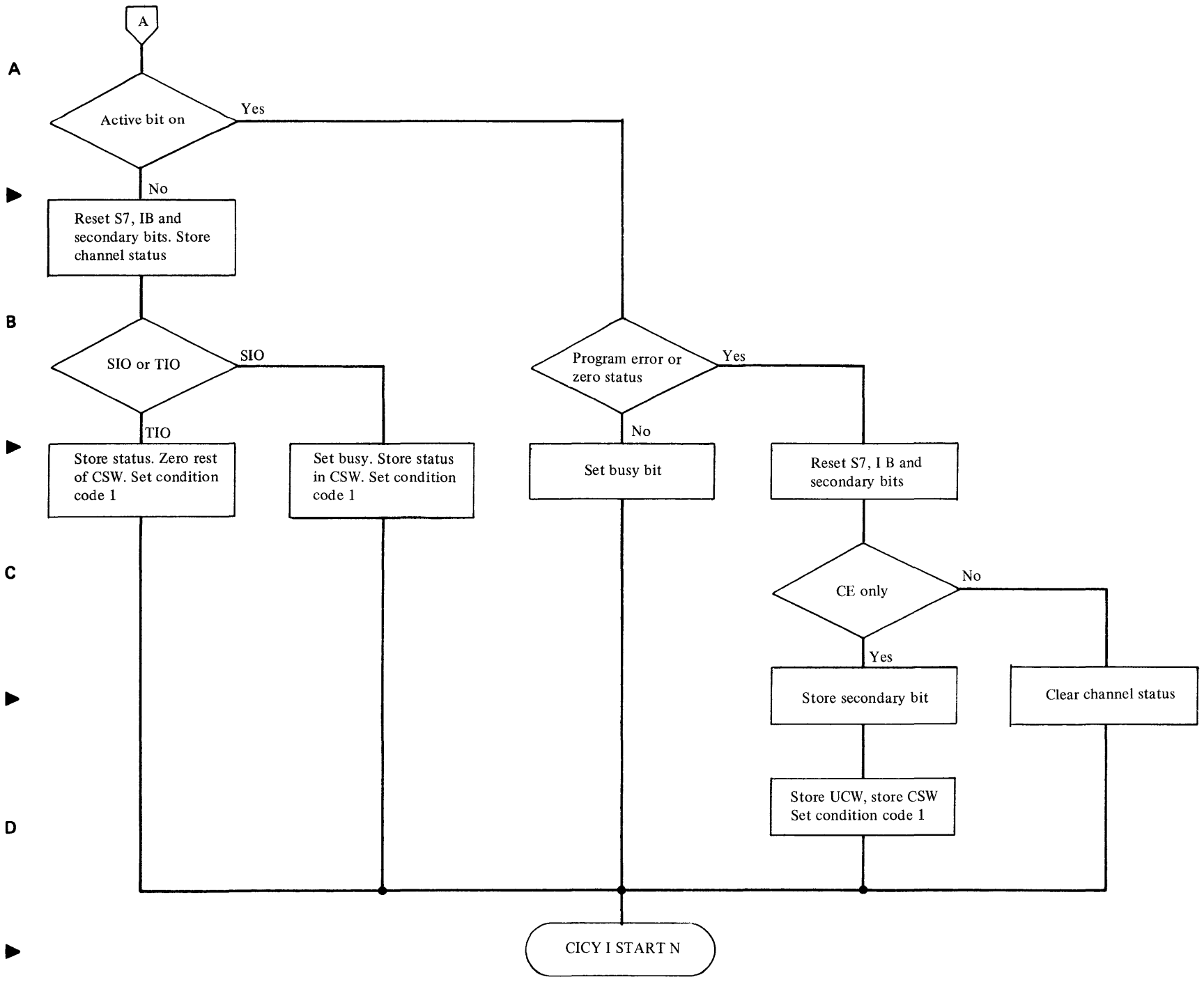


Diagram 5-107. Reader-Punch Status (Part 1 of 2)

Diag 5-107 P1 3G



Diag 5-107 P1 5G

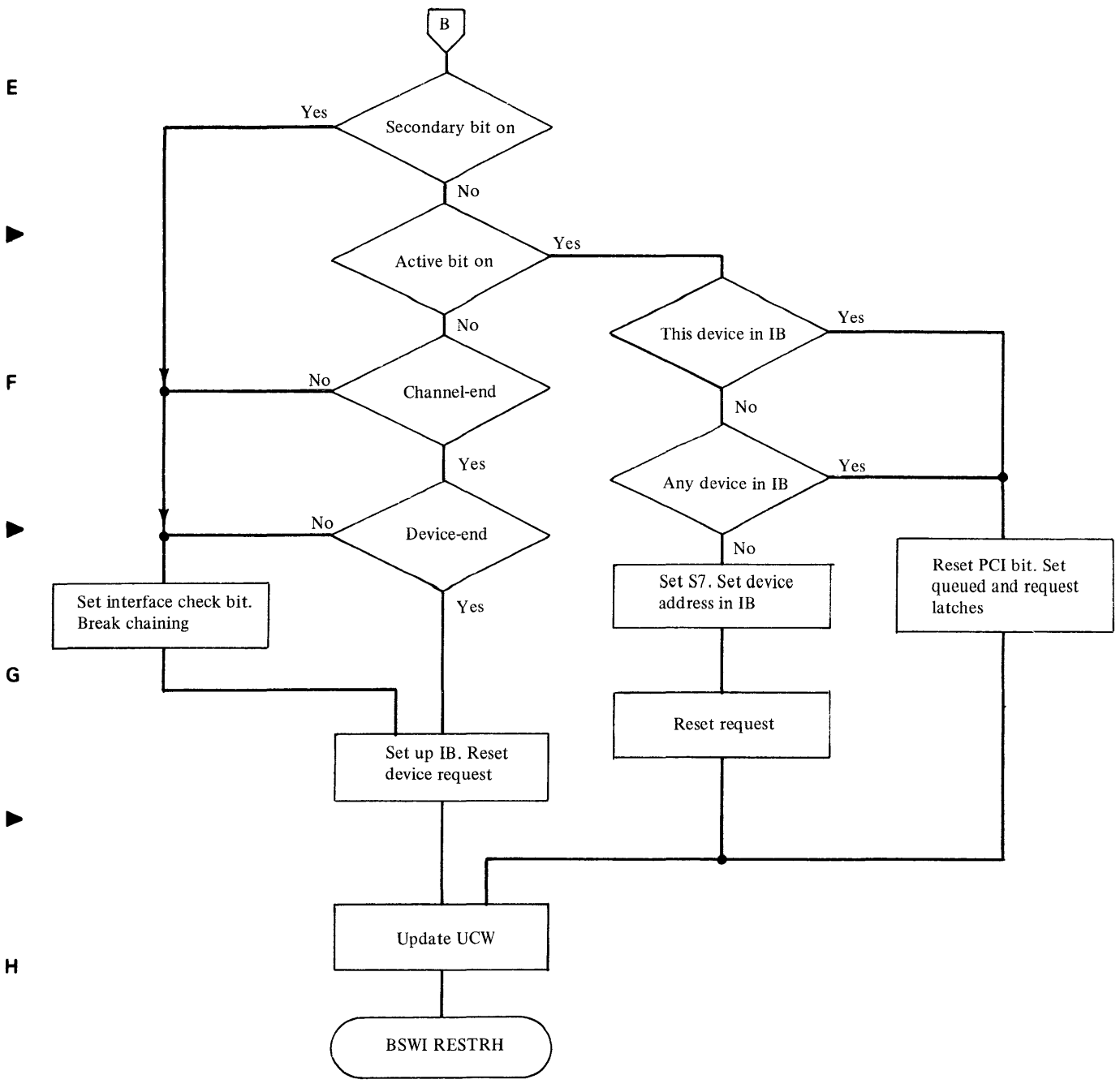
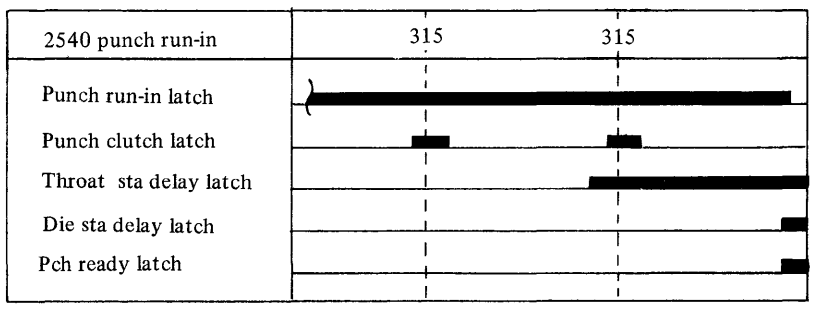
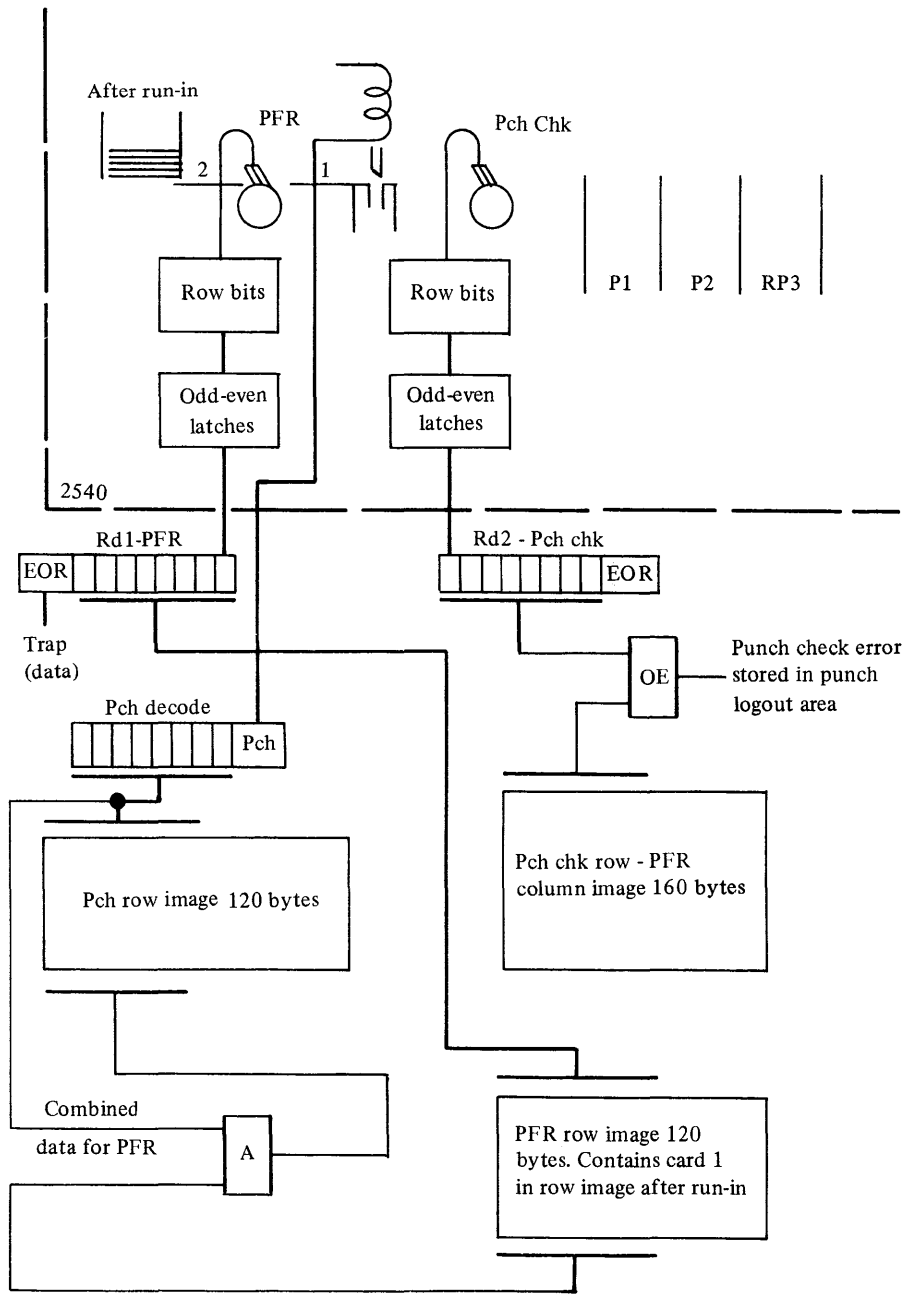


Diagram 5-107. Reader-Punch Status (Part 2 of 2)

Objectives:

1. Feed two cards.
2. Set card 1 row image into PFR row-image buffer.
3. Set device-end and punch status request.





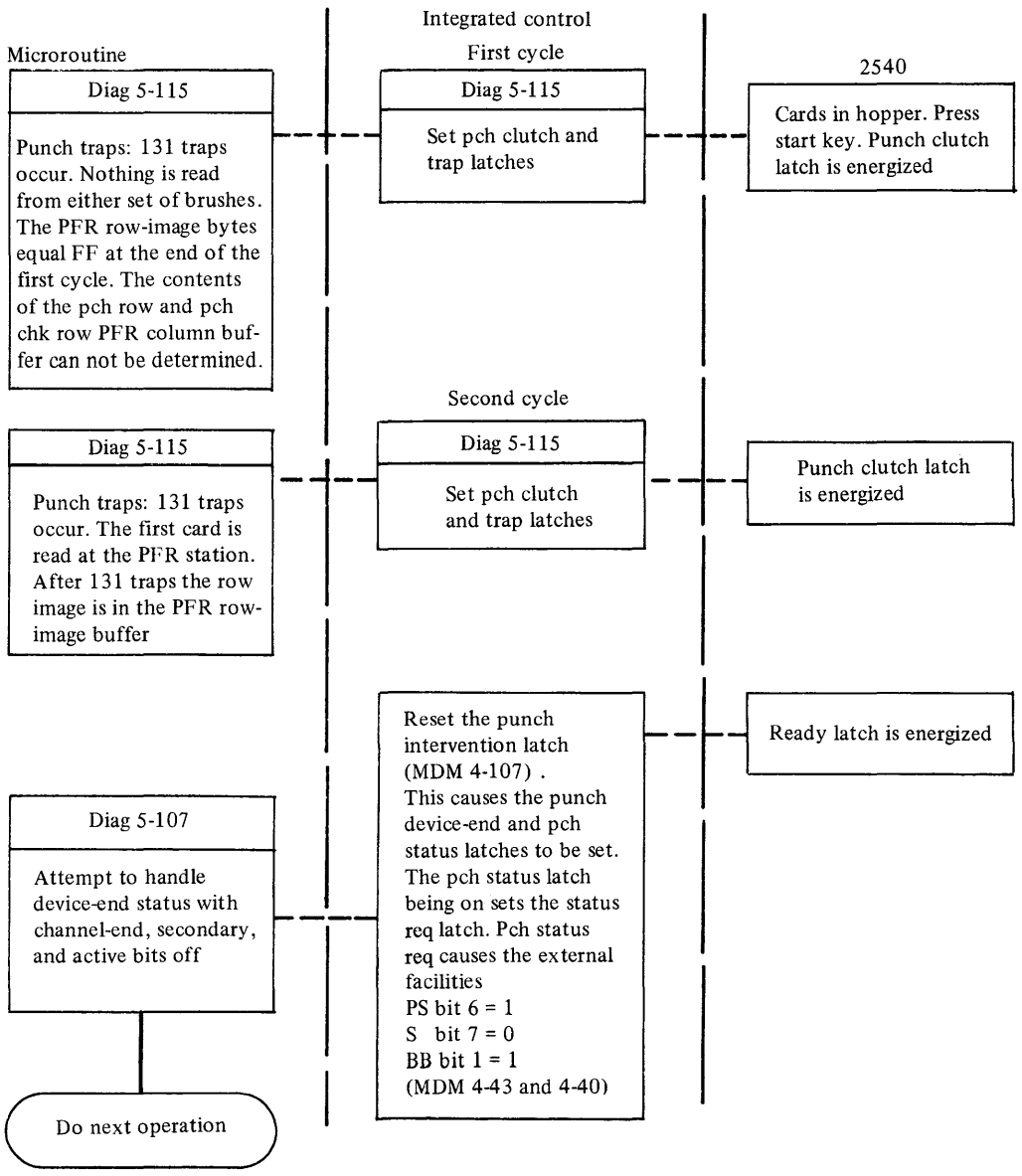


Diagram 5-111. Punch Run-In (Normal)

Objectives:

1. Decode command ZZ00 1001 PFR write.
   ZZ00 0001 punch write.
2. Set up stacker selection for card to be punched.
3. Transfer pch row image to pch chk row.
4. Translate data to be punched and set into pch row image.
5. Issue stacker selection for card to be read at pch chk brushes.
6. Issue feed command.
7. Set channel-end.

Microroutines

Start

CICY / CHECK

Read out instruction and decode (9C)

DCLA / IOINST

Reset S-register bits except 6 and 7. Insure operating in privilege mode. Read out CAW; check boundary limits. Identify device as the punch. Check punch UCW conditions. Set up active

DCLB / RDHW1

Read out CCW and set up data (command, flag-op, and count). Store next CCW adr. Set up data address. Store protect key from CAW and set into Q

ERDR CCOM / NRDR LSAVE

Save local storage register U, G, I, and P

ERDR ERRQ / RDIND

Read out punch indicator and sense bytes

ERDR

Set pch cmd inlk. Set RP K = 08 Reset request latch. Rst P K = 03

EPCH / NPCH

Reset punch and validity check latches. Rst P K = 80 Set up indicator and sense bytes for this command; save in local storage

Last cmd PFR write — Yes → Command reject

No

Cmd is a PFR write — Yes

EPCH

Set PFR wr feed bit (bit 6) of indicator byte. Set PFR restart latch. Set P K = 04 Set 2540 (punch) mode and 2540 zone (6). Set PFR indicator bit

No

EPCH

Set 2540 (punch) mode and 2540 zone (6). Set not PFR indicator bit

A

Diag 5-112 P2 2A

Integrated control

Set the pch cmd inlk latch (MDM 4-107). Reset status request and device-end latches

Block the reset of the punch ready latch

Reset the PFR validity and pch equip chk latches. (MDM 4-105)

Set the PFR restart gate latch. (MDM 4-111)

Conditions the set of the restart latch. This allows a three card run-in after a NPRO if no errors have occurred

2540

PFR

Pch chk

P1 P2 RP3

Row bits

Odd-even latches

Row bits

Odd-even latches

Rd1-PFR

EOR

Rd2 - Pch chk

EOR

OE

Punch check stored in logout area.

Pch decode

Pch

Pch row image 120 bytes
Contains row image of data to be punched

Pch chk row -
PFR column image
160 bytes.
Contains punch row image of card to be read next by the pch chk brushes

PFR row image
120 bytes
Contains row image of last PFR card or card 1 of run-in

From translate

A

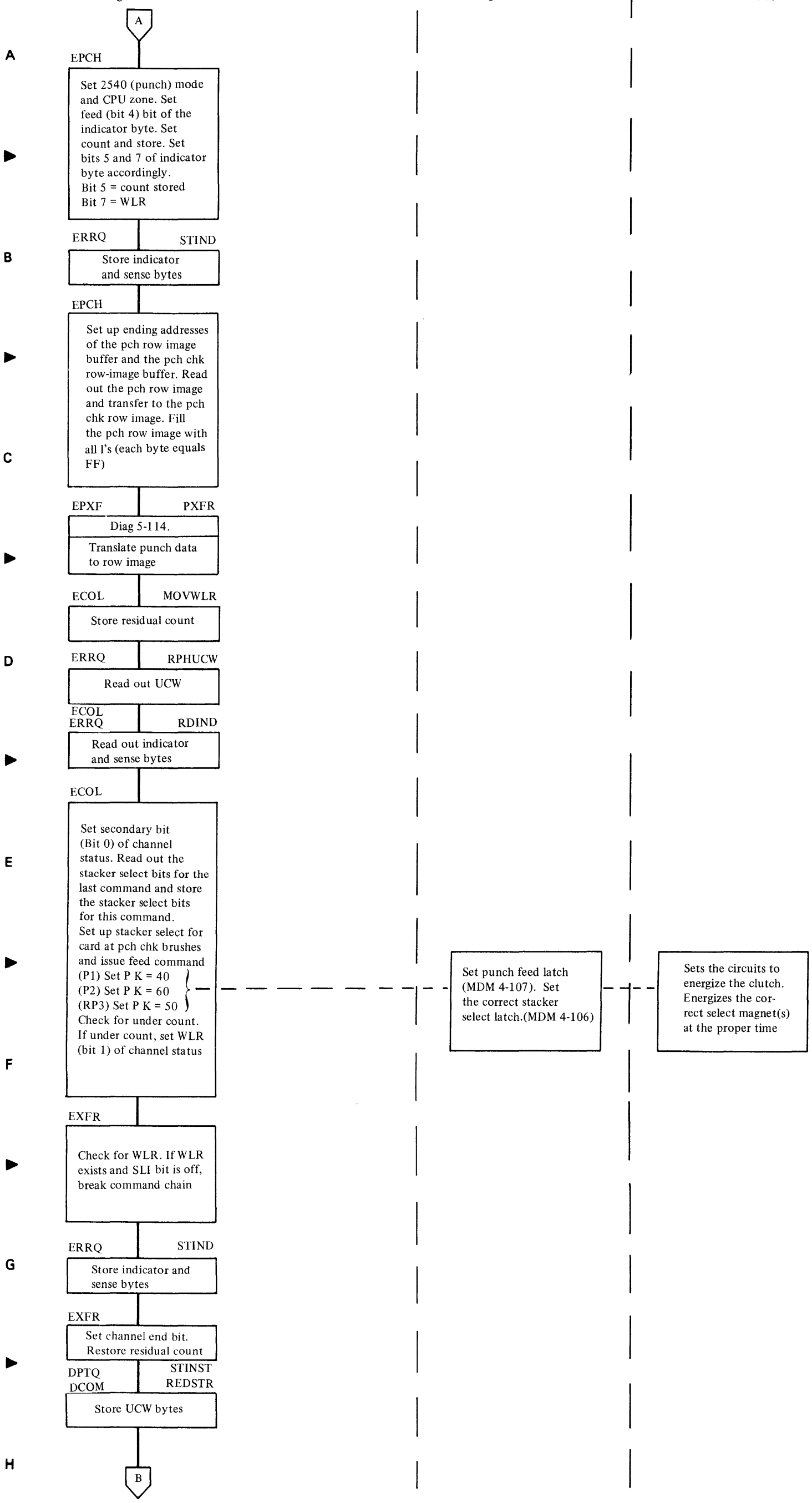
Diagram 5-112. Start I/O (Punch Write) (Part 1 of 3)

Diag 5-112 P1 2H

Micro routines

Integrated control

2540



Diag 5-112 P3 2A

Diagram 5-112. Start I/O (Punch Write) (Part 2 of 3)

Diagram 5-112. Start I/O (Punch Write) (Part 3 of 3)

Microroutines

Start

A — CICY / CHECK
Read out instruction and decode (9C)

DCLA / IOINST
Reset S-register bits except 6 and 7. Insure operating in privilege mode. Read out CAW; check boundary limits. Identify device as the punch. Check punch UCW conditions. Set up active

B — DCLB / RDHW1
Read out CCW and set up data (command, flag-op, and count). Store next CCW addr. Set up data address. Store protect key from CAW and set into Q.

C — ERDR / NRDR, CCOM / LSAVE
Save local storage registers U, G, I, and P

ERDR / RDIND
ERRQ
Read out punch indicator and sense bytes

D — ERDR
Set pch cmd inlk.
Set RP K=08.
Reset request latch.
Rst P K=03

EPCH / NPCH
Reset punch and validity check latches.
Rst P K=80

Integrated control

Set the pch cmd inlk latch (MDM 4-107).
Reset the status request and device-end latches. (MDM 4-107)

Reset the PFR validity and pch equip chk latches. (MDM 4-105)

E — PFR unit exception gate
Yes → ERDR UEXPFR
No

F — EPCH
Check for two consecutive read commands. If two reads, set unusual cmd bit (bit 6) of the punch sense byte. Set bits 5 and 7 of indicator byte accordingly.
Bit 5 = count stored
Bit 7 = WLR

ERRQ / STIND
Store indicator and sense bytes

G — ERDR / BACK
Set up beginning address of the PFR column-image buffer and the ending address of the PFR row-image buffer

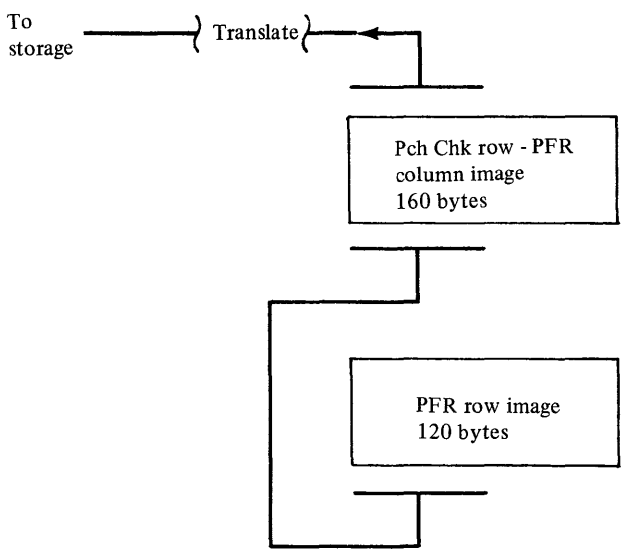
By starting with ending address of PFR row image (9's), the same routine used for the reader can be used for the punch

A

Diag 5-113 P2 2A

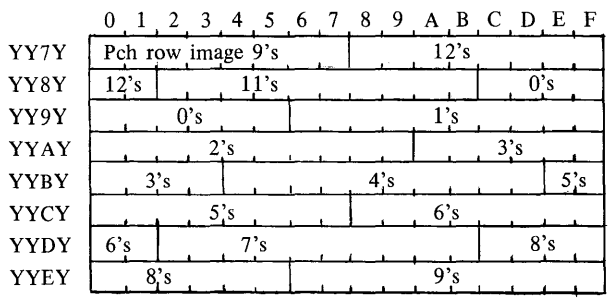
H

Objective:
1. Decode command 1100 1010 PFR read
2. Transfer the PFR row image to the PFR column image.
3. Compress the PFR column-image byte and translate the compressed byte to the actual desired character.



PFR column image

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
XX0X	1		2		3		4		5		6		7		8	
XX1X	9		10		11		12		13		14		15		16	
XX2X	17		18		19		20		21		22		23		24	
XX3X	25		26		27		28		29		30		31		32	
XX4X	33		34		35		36		37		38		39		40	
XX5X	41		42		43		44		45		46		47		48	
XX6X	49		50		51		52		53		54		55		56	
XX7X	57		58		59		60		61		62		63		64	
XX8X	65		66		67		68		69		70		71		72	
XX9X	73		74		75		76		77		78		79		80	



PFR row image

2540

Block reset of the punch ready latch

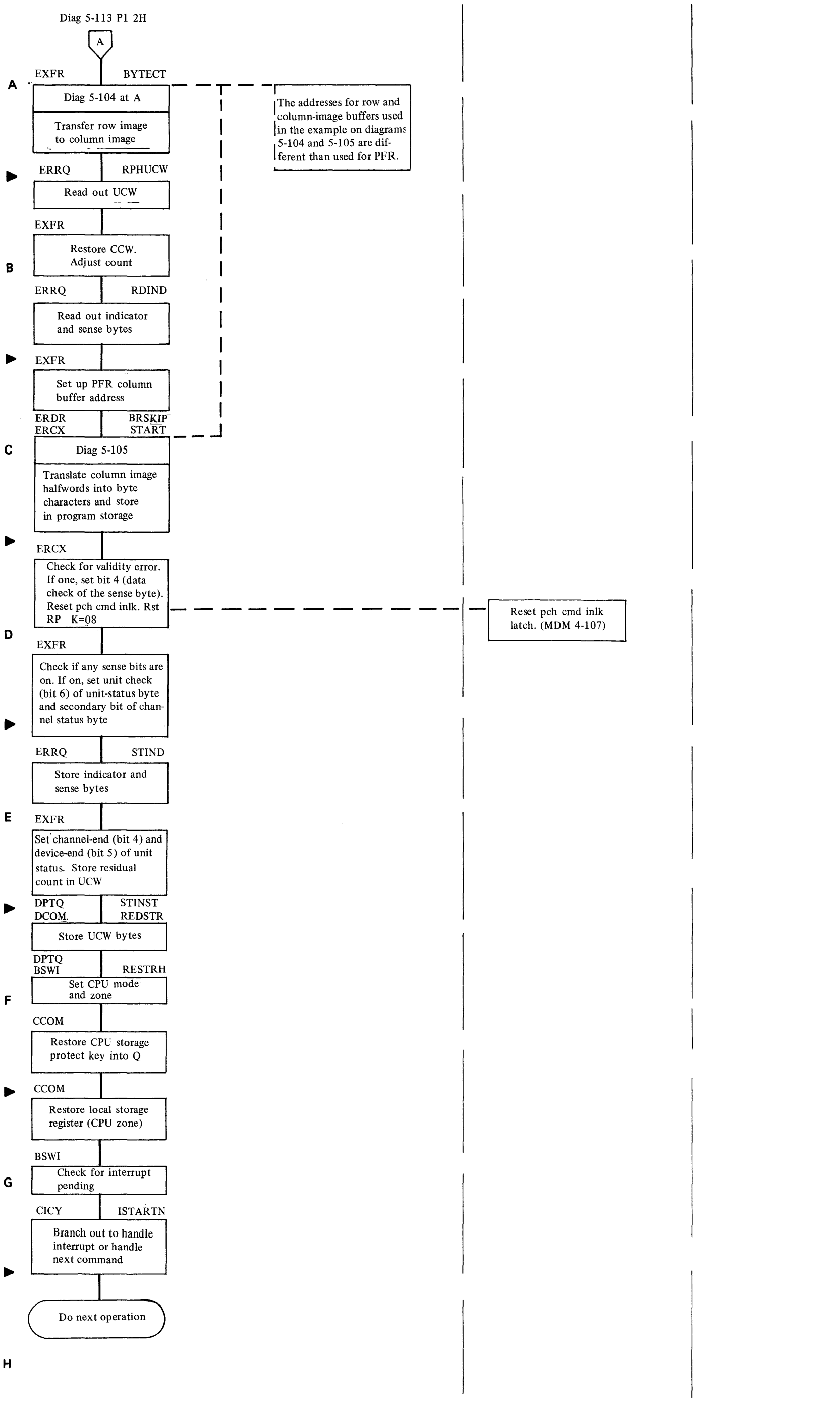
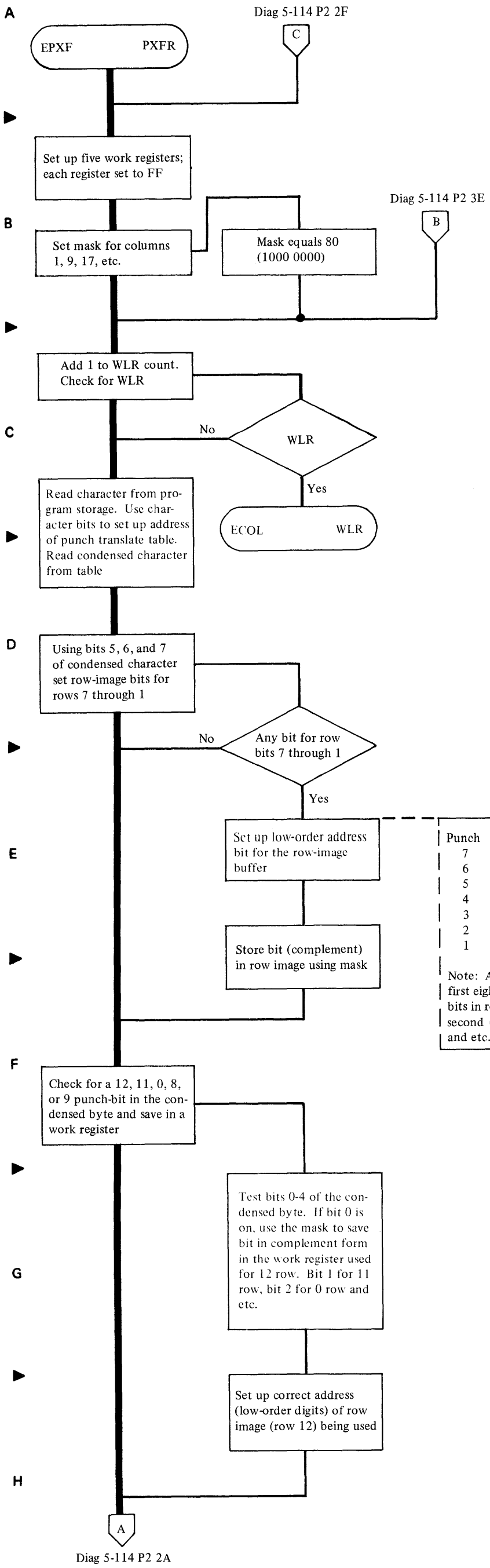


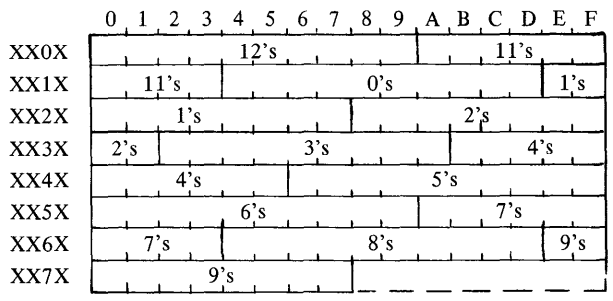
Diagram 5-113. Punch Feed Read (Part 2 of 2)

Objectives:
1. Set up work area and counter.
2. Translate data to be punched and set into punch row image in complement form.



Punch	Address
7	5A, 5B, 5C
6	50, 51, 52
5	46, 47, 48
4	3C, 3D, 3E
3	32, 33, 34
2	28, 29, 2A
1	1E, 1F, 20

Note: Address 5A is for first eight columns of row bits in row 7; 5B for second eight columns and etc.



Punch row-image buffer

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
ZZ0Z	B9	89	8A	8B	8C	8D	8E	8F	98	99	9A	9B	9C	9D	9E	9F
ZZ1Z	D9	49	4A	4B	4C	4D	4E	4F	58	59	5A	5B	5C	5D	5E	5F
ZZ2Z	79	29	2A	2B	2C	2D	2E	2F	38	39	3A	3B	3C	3D	3E	3F
ZZ3Z	F9	09	0A	0B	0C	0D	0E	0F	18	19	1A	1B	1C	1D	1E	1F
ZZ4Z	00	A9	AA	AB	AC	AD	AE	AF	B8	91	92	93	94	95	96	97
ZZ5Z	80	C9	CA	CB	CC	CD	CE	CF	D8	51	52	53	54	55	56	57
ZZ6Z	40	21	6A	6B	6C	6D	6E	6F	78	31	C0	33	34	35	36	37
ZZ7Z	E0	E9	EA	EB	EC	ED	EE	EF	F8	11	12	13	14	15	16	17
ZZ8Z	B1	A1	A2	A3	A4	A5	A6	A7	B0	A8	B2	B3	B4	B5	B6	B7
ZZ9Z	D1	C1	C2	C3	C4	C5	C6	C7	D0	C8	D2	D3	D4	D5	D6	D7
ZZAZ	71	61	62	63	64	65	66	67	70	68	72	73	74	75	76	77
ZZBZ	F1	E1	E2	E3	E4	E5	E6	E7	F0	E8	F2	F3	F4	F5	F6	F7
ZZCZ	A0	81	82	83	84	85	86	87	90	88	BA	BB	BC	BD	BE	BF
ZZDZ	60	41	42	43	44	45	46	47	50	48	DA	DB	DC	DD	DE	DF
ZZEZ	32	69	22	23	24	25	26	27	30	28	7A	7B	7C	7D	7E	7F
ZZFZ	20	01	02	03	04	05	06	07	10	08	FA	FB	FC	FD	FE	FF

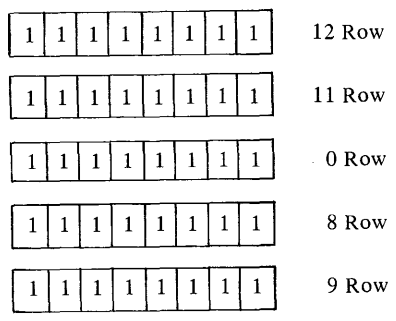
Punch translate table (condensed byte)

Condensed byte

Bits	0	1	2	3	4	5	6	7	
Punch	12	11	0	8	9	X	X	X	Punch
						0	0	1	1
						0	1	0	2
						0	1	1	3
						1	0	0	4
						1	0	1	5
						1	1	0	6
						1	1	1	7

Example:
First eight columns (data) to be punch are 1 bl FOX bl RA.

Work registers



Read data character for column 1; 1 = F1.

Read out condensed byte using data character as low-digit address. ZZ F1 = 01.

Condensed byte = 0000 0001.

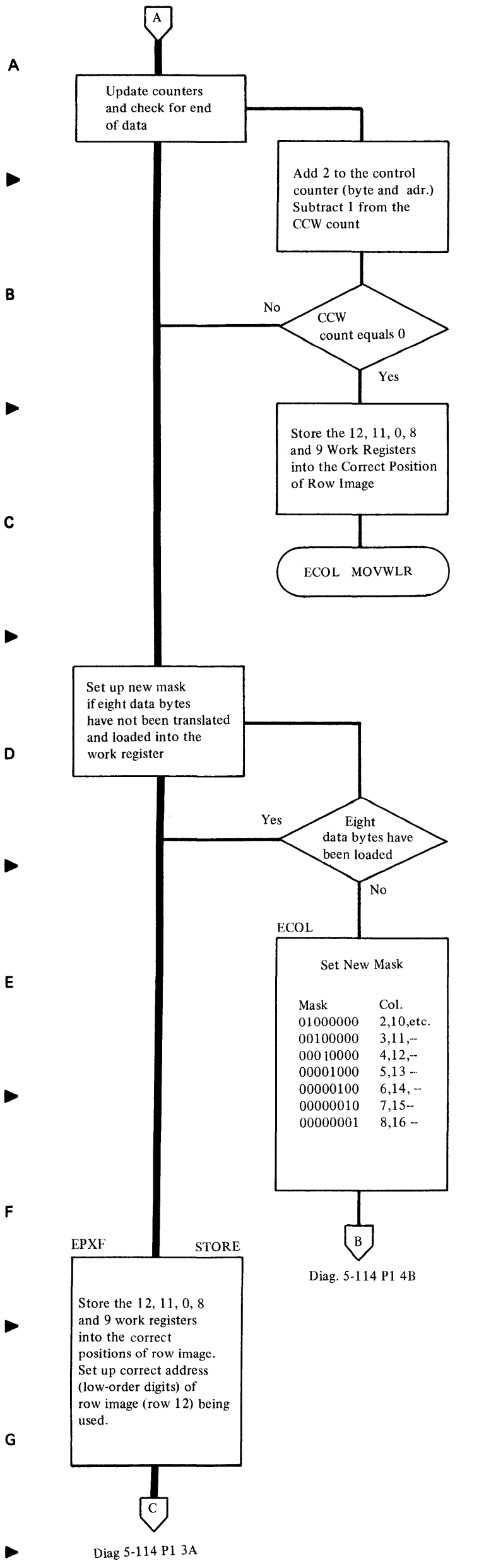
Check bits 5, 6, and 7 (001). This provides a row-image address of XX1E. The byte at this address is for the first eight columns of the 1 row. Bit 0 is for column 1. Prior to this time all of row image has been set to 1's. Exclusive ORing the mask 80 with FF results in 7F. This identifies column 1 of the card, to be punched with a 1 punch. Store result into row image at the same address.

Because condensed byte bits 0-4 are all zero, nothing is stored in the work register.

Update the counters.
Set up new mask for column 2; 40.

Read out second data character; bl=40
Read out condensed byte using data character as a low-digit address. ZZ 40 = 00.
Condensed byte = 0000 0000.

Diagram 5-114. Load Punch Row Image (Part 1 of 2)



Because testing of the byte indicates no punches nothing is stored or loaded into the work registers.
Update the counters.
Setup new mask for column 3; 20.
Read out third data character; F = C6.
Read out condensed byte using data character as a low-digit address. ZZC6 = 86.
Condensed byte = 10000110.
Check bits 5, 6, and 7 (110). This provides a row-image address of XX50. The byte at this address is for the first eight columns of the 6 row. Bit 2 is for column 3. Exclusive ORing the mask 20 with FF results in DF. This identifies column 3 of the card, to be punched with a 6 punch. Store result into row image at the same address.
Test of condensed byte bits 0-4 indicates that bit 0 is on. This causes the mask 20 to be exclusive ORed with work register 1. The results in work register 1 set to DF.
Update the counters.
Set up new mask for column 4; 10.
Continue routine until eight-byte (data) have been loaded into row image and work registers.
For this example the work registers contain the following

Work Registers

1	1	1	0	1	1	1	1	0	12 Row
2	1	1	1	0	1	1	0	1	11 Row
3	1	1	1	1	0	1	1	1	0 Row
4	1	1	1	1	1	1	1	1	8 Row
5	1	1	1	1	1	1	0	1	9 Row

Transfer the work registers to the correct locations in row image.
Row-image bytes for the first eight columns for this example are:

Row	Address	Byte
12	XX00	11011110
11	XX0A	11101101
0	XX14	11110111
1	XX1E	01111110
2	XX28	11111111
3	XX32	11111111
4	XX3C	11111111
5	XX46	11111111
6	XX50	11001111
7	XX5A	11110111
8	XX64	11111111
9	XX6E	11111101

The address for row image now points to the next set of bytes (eight more columns).
Set the five work register to FF and repeat routine for next eight columns.

Diagram 5-114. Load Punch Row Image (Part 2 of 2)

1. Condition:
   Clutch is energized to feed a card.
   Objectives:
   Set punch trap.
   Set up beginning address of pch row image.
   Set the first eights bits into the punch decode shift register.

2. Condition:
   Run-in (data)
   Objective:
   Transfer the PFR row image into the pch row image.
   Store the data from Rd1-PFR in the PFR row image.

3. Condition:
   After run-in (data)
   Objectives:
   Transfer data to be punched from pch row image to punch magnets.
   Check the punched card at the pch chk brushes with the pch chk buffer. Save the error condition after one card has passed the pch chk brushes.

4. Condition:
   After run in (data) PFR
   Objectives:
   Transfer data to be punched from pch row image to punch magnets.
   Combine the PFR row image with the pch row image and store in pch row image.
   Store the data from Rd1-PFR in the PFR row image.
   Check the punched card at the pch chk brushes with the pch chk buffer. Save the error condition after one card has passed the pch chk brushes.

Microroutine

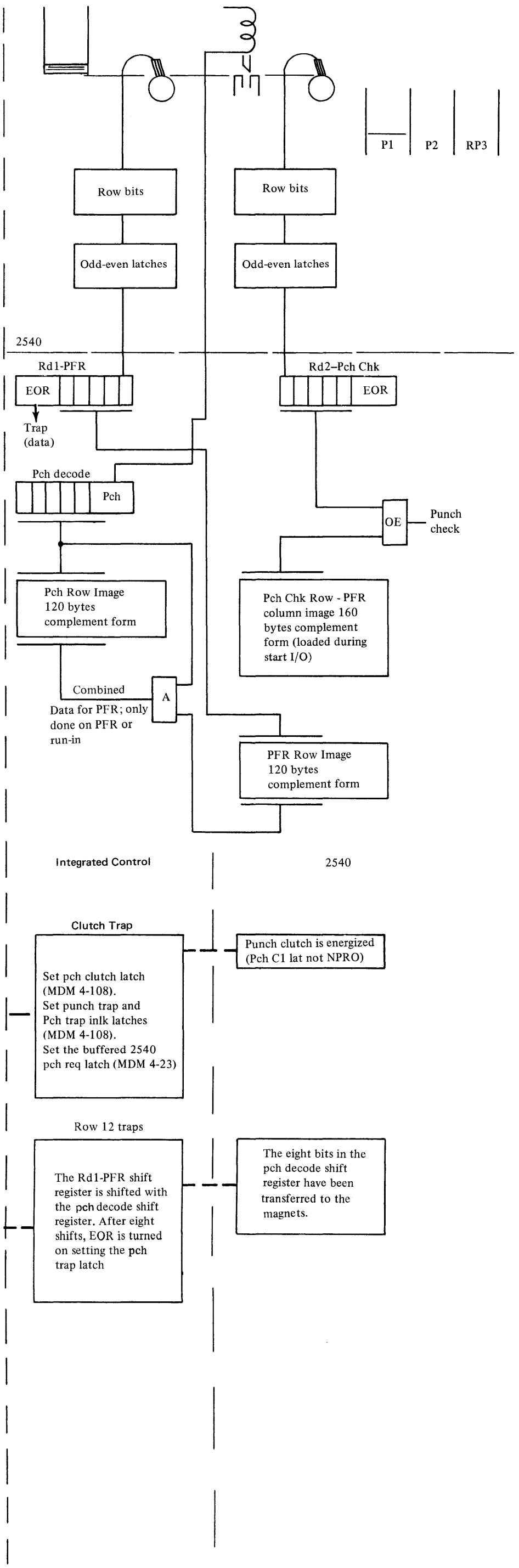


Diagram 5-115. Punch Trap (Part 1 of 2)

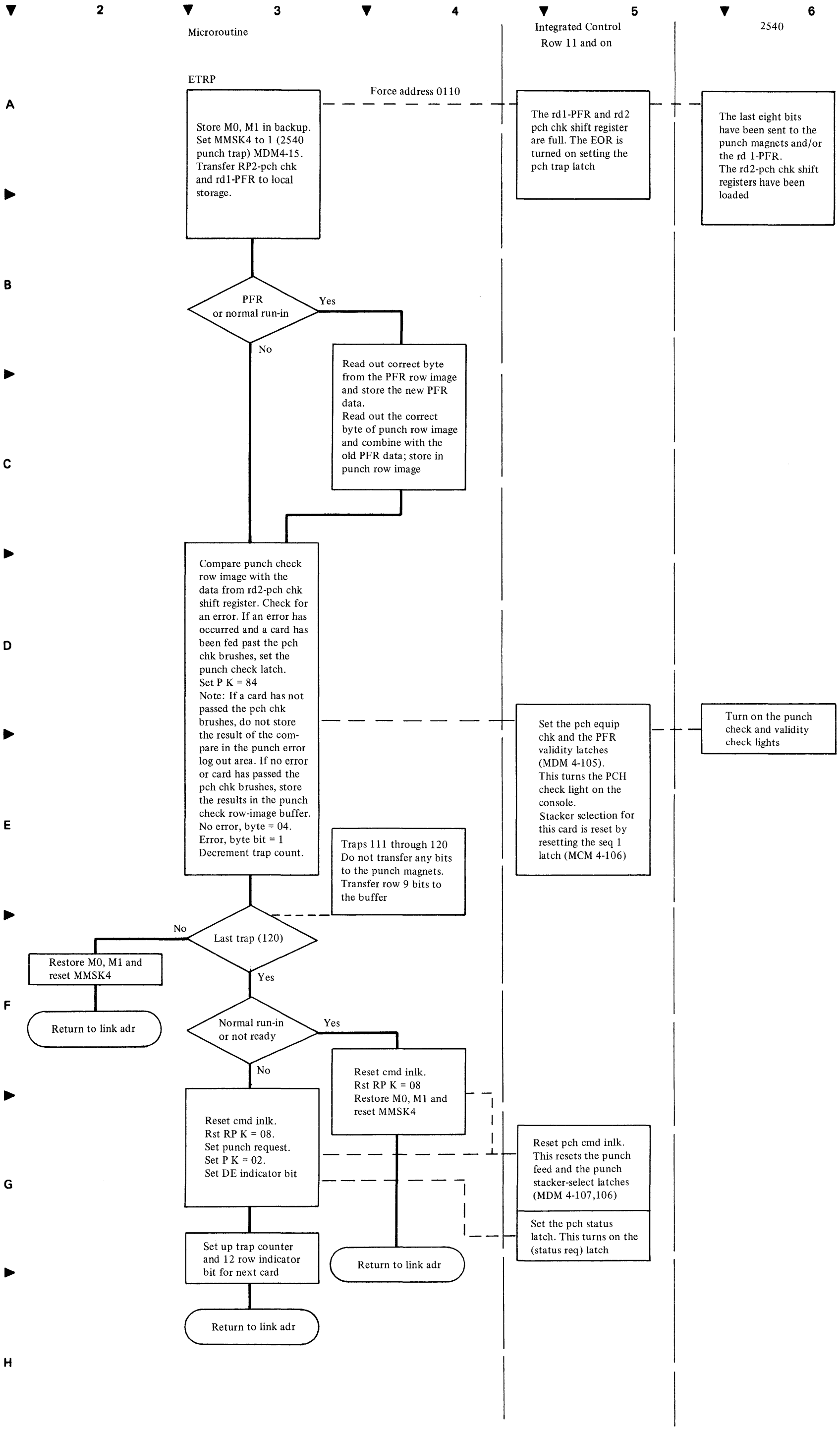


Diagram 5-115. Punch Trap (Part 2 of 2)

Instruction: Start I/O
Command: Write space 1 after print.
Condition: Print ready
Standard 48-character chain length
Status clear
Objectives: Buffer load
Set channel-end.
Set print busy.
Set print gate.

Constant	Function
01 (note 1)	PLBAR value
84 (note 2)	PLB count
2C	PLBAR constant
70	Translate table address

Note 1. This value is set to 01. The value is updated each buffer cycle.

Note 2. The PLB count is set to 84 (dec. 132) and decremented by 1 each buffer cycle.

Start

CICY
Read out instruction and decode (9C)

DCLA
Reset S-reg. bits except 6 and 7. Read out CAW and check boundary limits. Construct UCW address and identify the printer

DCLB
Read out the CCW. Store the next CCW and fetch data address. Store UCW count and data address

DPTS
Set 1403 mode and decode the 1403 command

DPTR
Set up constants
PLBAR value = 01
PLB count = 84 (HEX 132)
PLBAR constant = 2C
Translate table address = 70

Diag. 5-201 P2 6B
B

DPTR
Read character from memory area specified by the data address. The data character develops the lines necessary to address the translate table. Place the character from translate table into local storage

DPTR
Load the PLBAR. The value of the PLBAR is placed on EXT, bus-out lines to set the PLBAR

1403 attachment
The PLBAR triggers 1-128 are set with ext bus out bits and PLBAR set sample. MDM 4-207

DPTR
Set read control. Set PR AK = 20

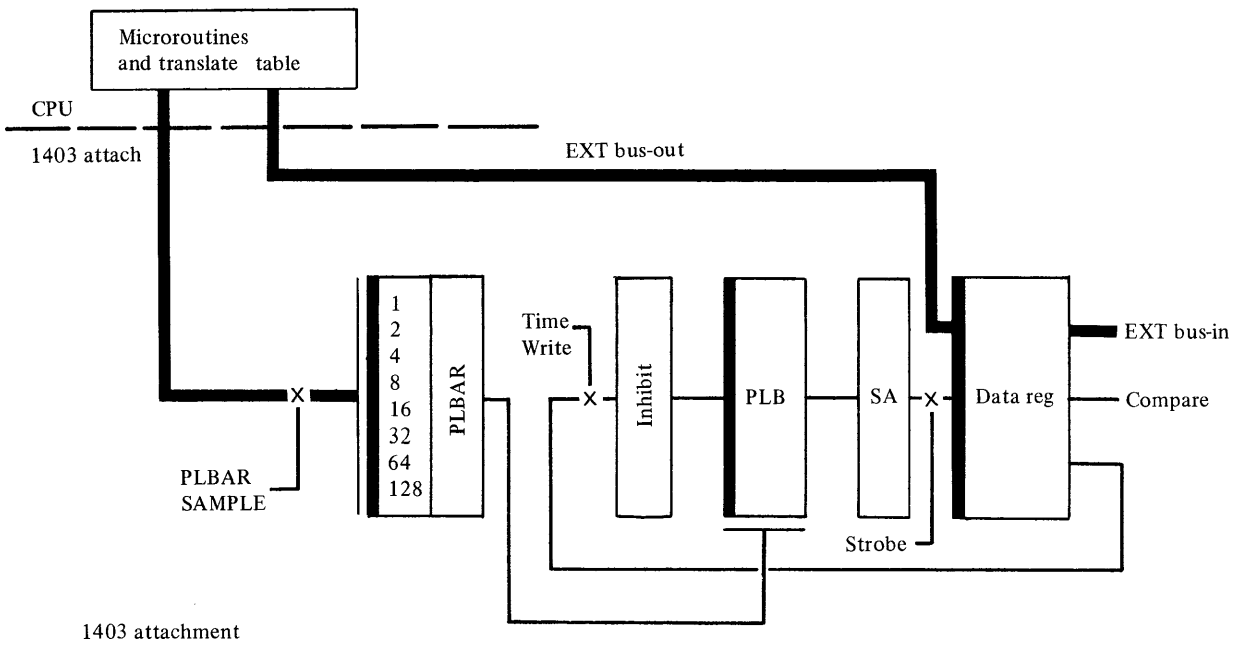
Set read control latch. Develop SA strobe and reset the PLB data reg. See chart - 6E MDM 4-207

DPTR
Test translated character for bit pattern greater than the maximum graphic position number. If FF pattern is detected, set data check. Set FF in PLB

DPTR
Load PLB. Transfer the translated character from local storage to the PLB data reg. and at write time, into the buffer.

Reset the data reg with ctl. Word type 3 and AS decode of B. Set the data reg, latches with ext/bus out bits 0-7 and PLB sample. Write control is brought up by ext. AS decode B and control word type 3. Refer to timing chart MDM 4-208

A
Diag. 5-201 P2 2A



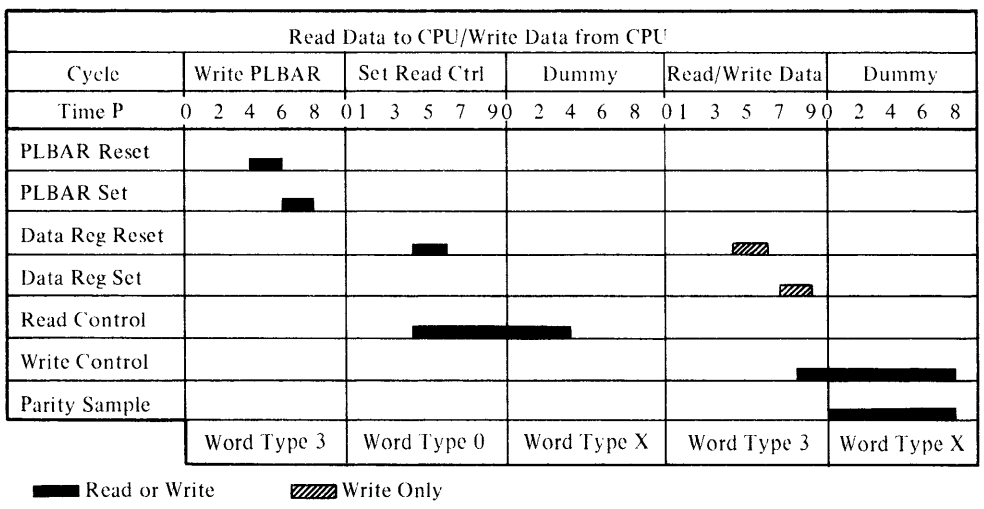
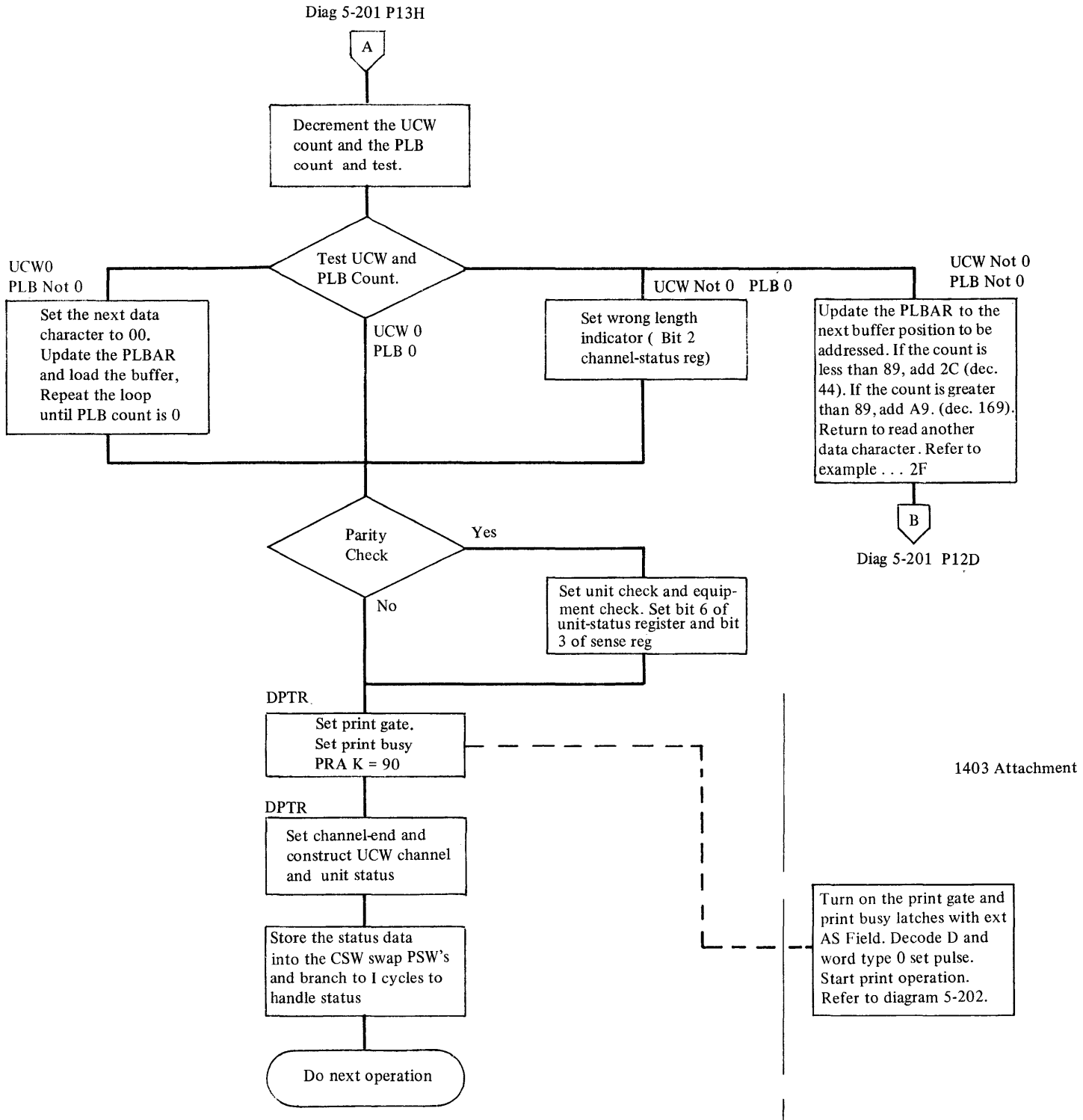


Diagram 5-201. Buffer Load (Part 1 of 2)

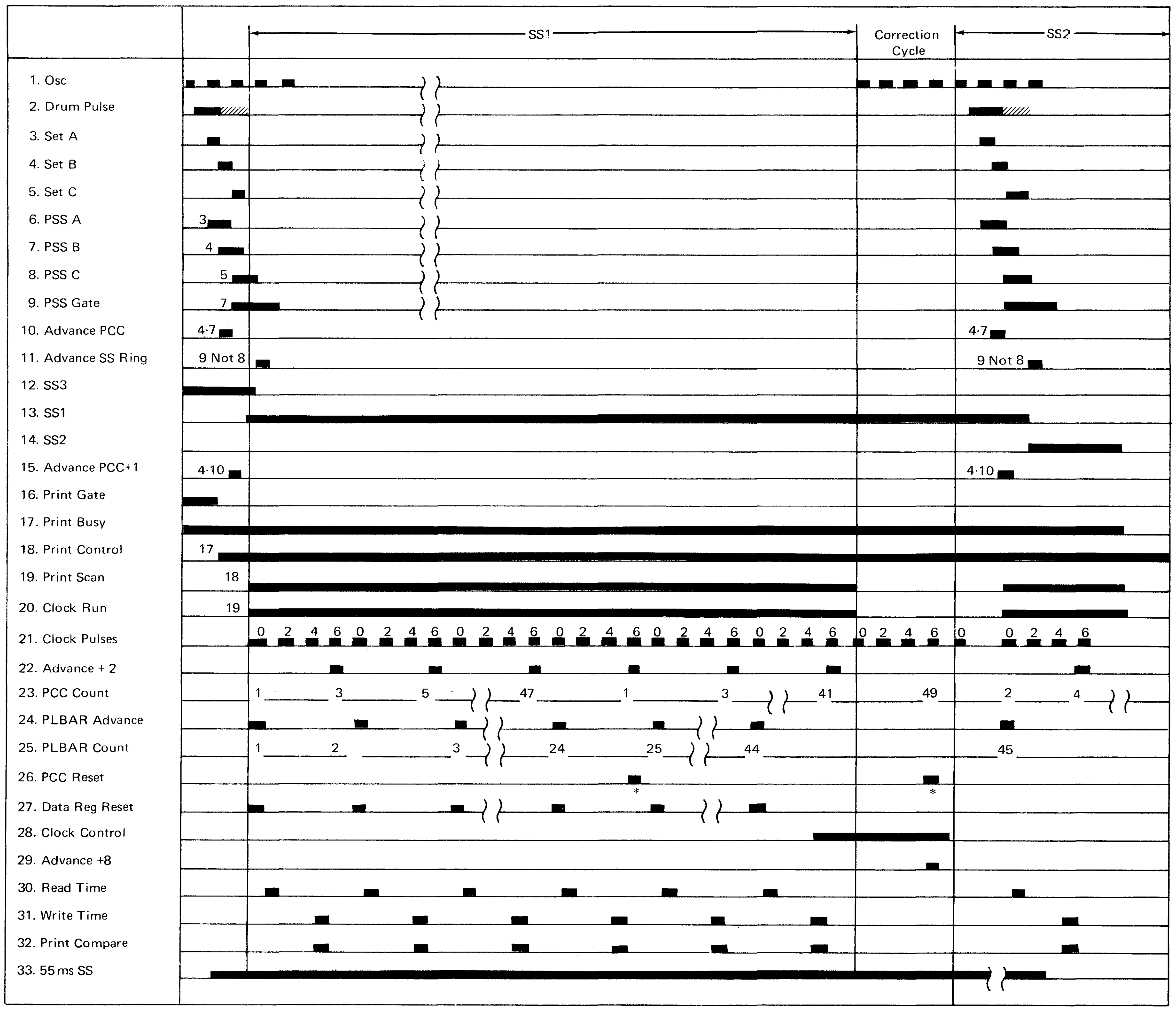


Example of PLBAR update

PLBAR VALUE	01	(dec. 01)
Constant	+2C	
Updated PLBAR	2D	(dec. 45)
PLBAR	2D	
Constant	+2C	
	59	(dec. 89)
PLBAR	59	
Constant	+A9	
	02	(dec. 02)
PLBAR	02	
Constant	+2C	
	2E	(dec. 46)
PLBAR	2E	
Constant	+2C	
	5A	(dec. 90)
PLBAR	5A	
Constant	+A9	
	03	(dec. 03)

Diagram 5-201. Buffer Load (Part 2 of 2)

Diagram 5-202. Print Operation



* The Pcc reset during clock control resets triggers 16-128.

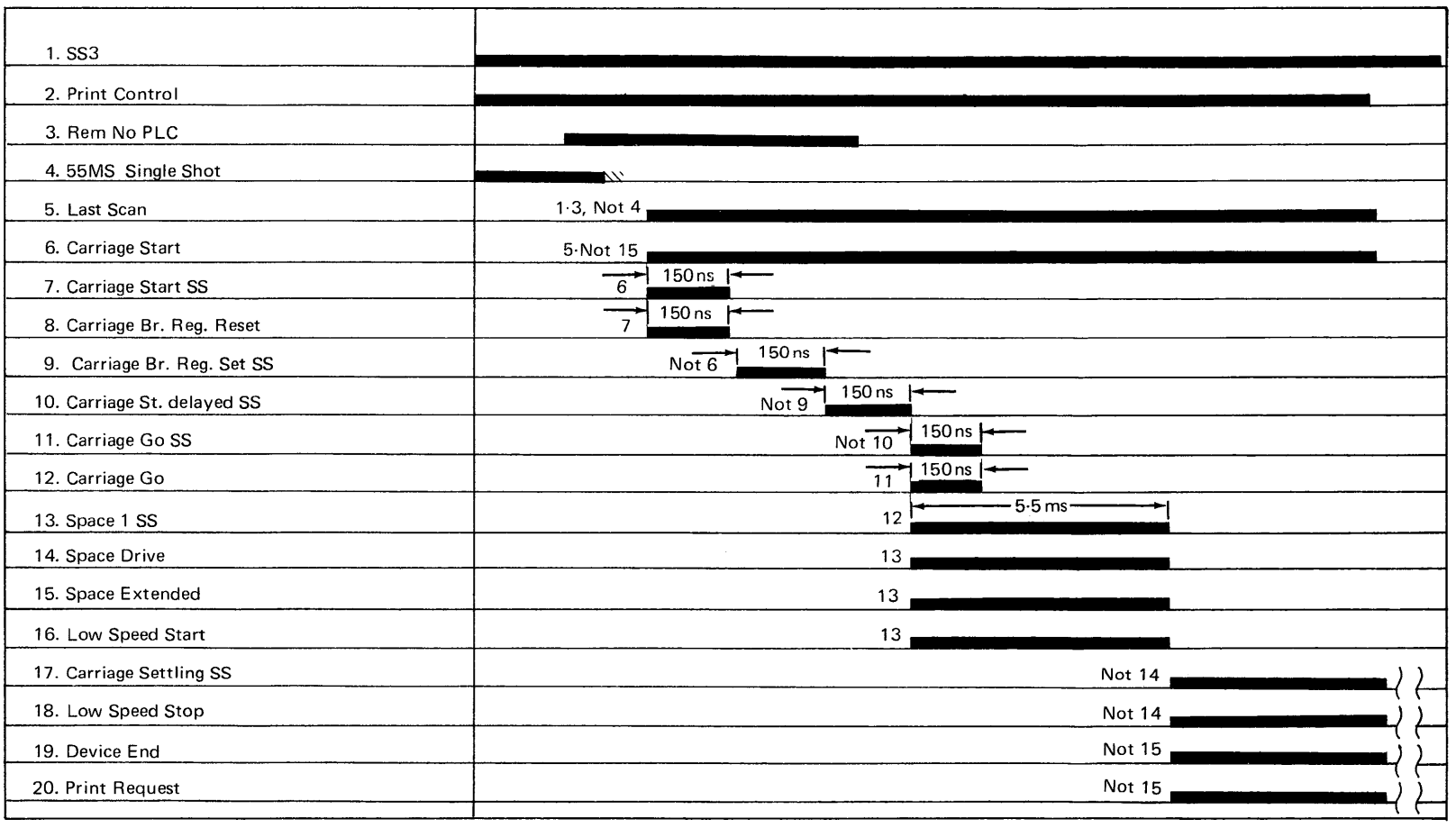
At all other times, the PCC reset resets triggers 4-128

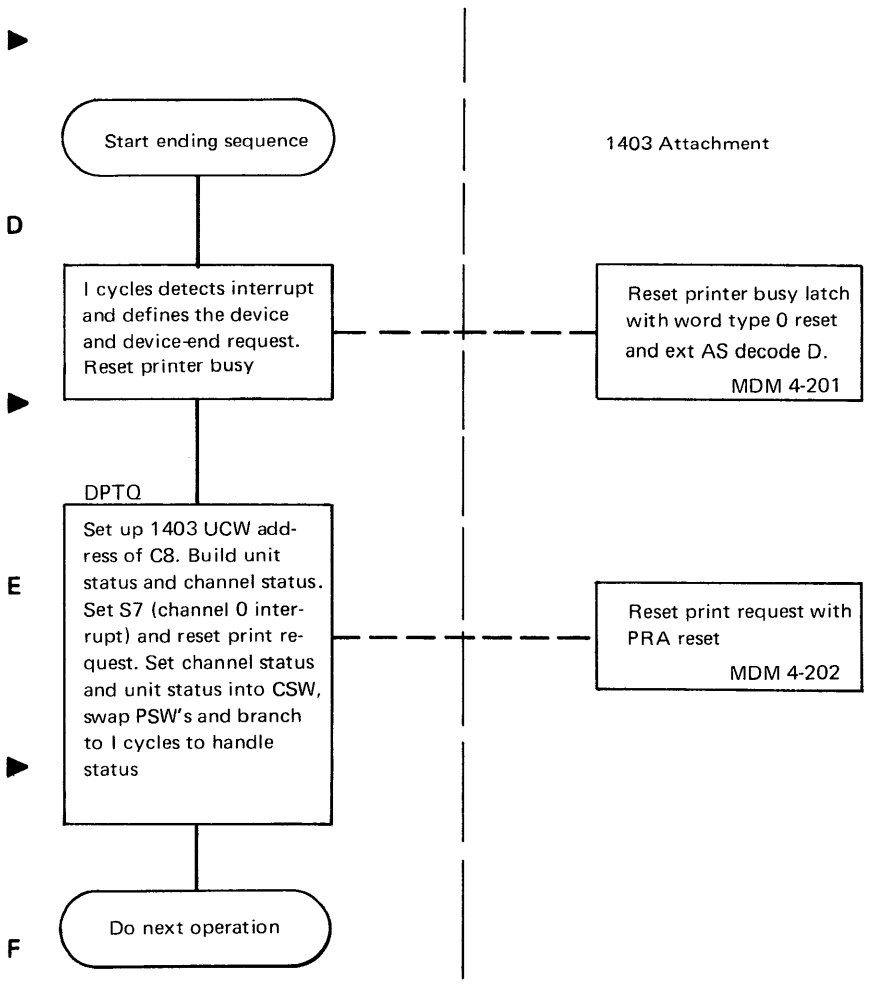
Example: Print Model 25

Buffer Position	1	2	3	4	5	—	44
Character	(M)	(E)	(2)				
Print Position	1	4	7	10	13	—	130
Buffer Position	45	46	47	48	49	—	88
Character	(0)	(L)	(5)				
Print Position	2	5	8	11	14	—	131
Buffer Position	89	90	91	92	93	—	132
Character	(D)	(SP)					
Print Position	3	6	9	12	15	—	132

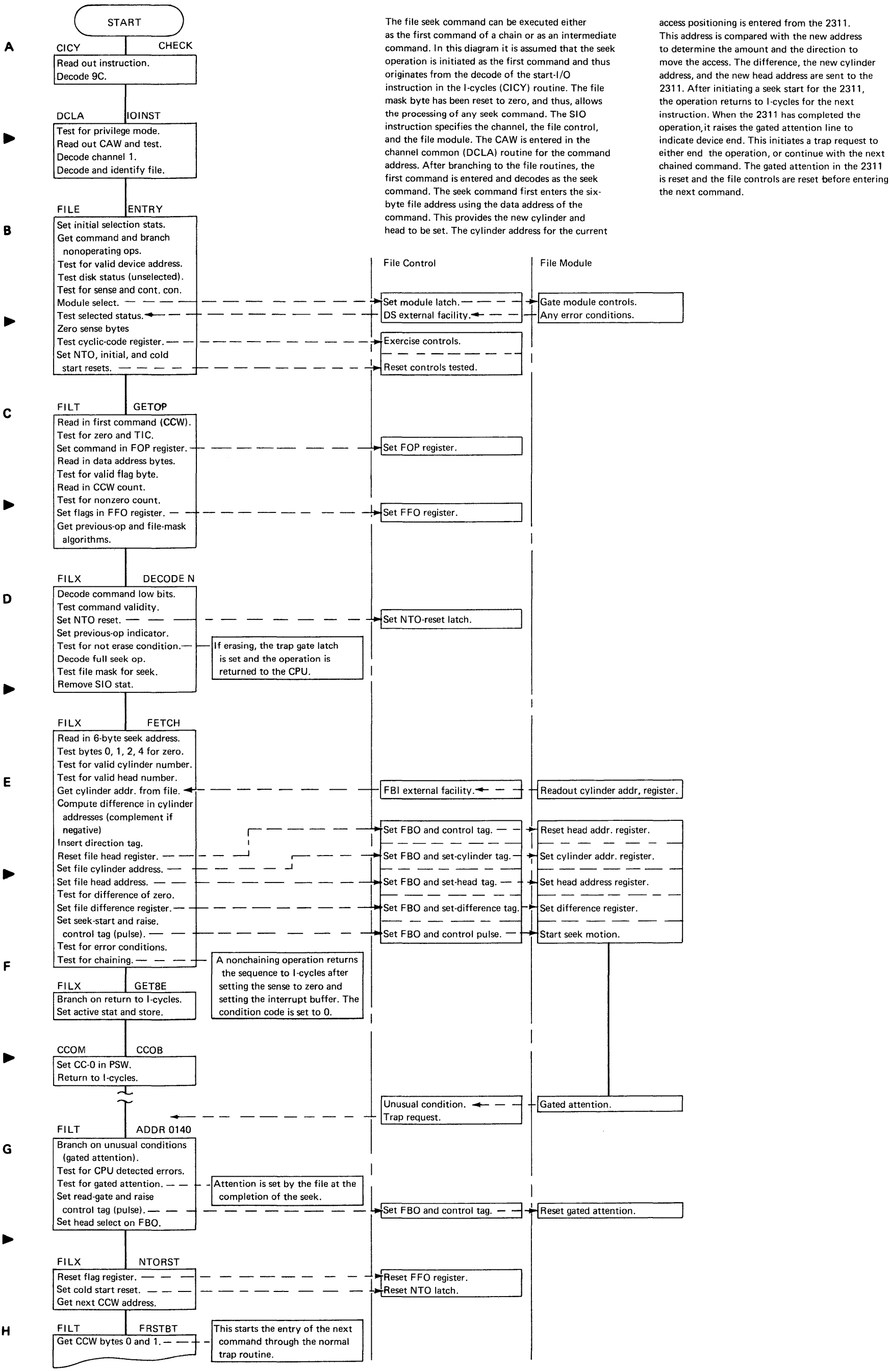
▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Carriage Operation: Space 1 after print.



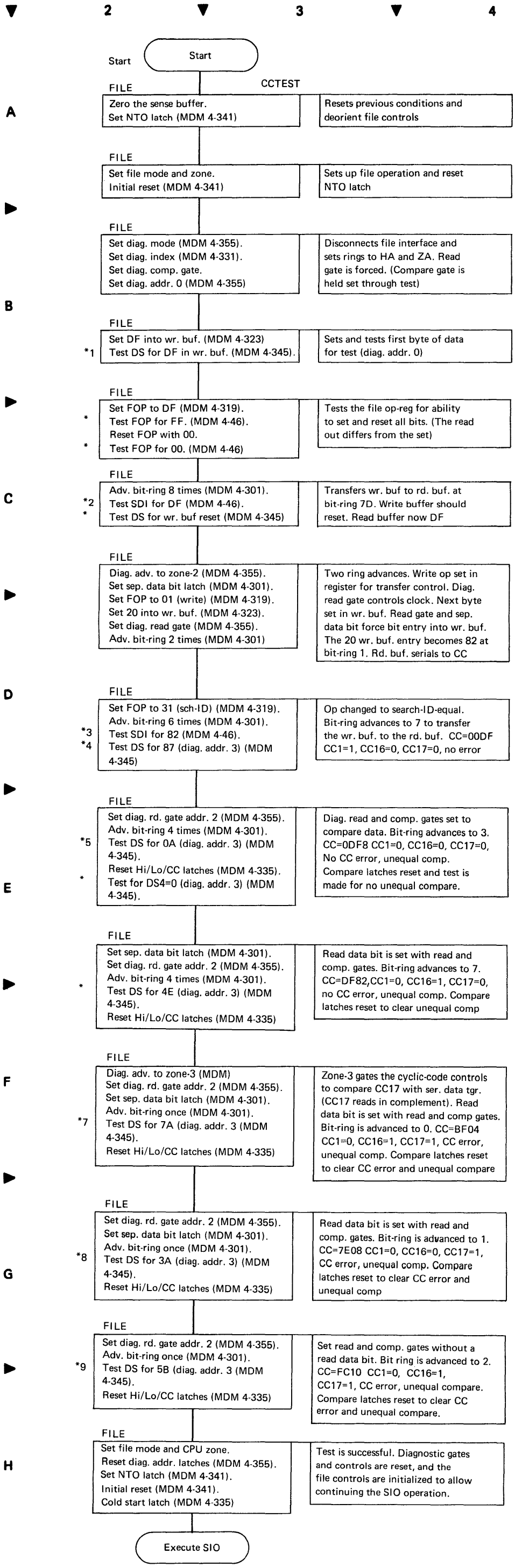


● Diagram 5-203. Space 1 After Print



The file seek command can be executed either as the first command of a chain or as an intermediate command. In this diagram it is assumed that the seek operation is initiated as the first command and thus originates from the decode of the start-I/O instruction in the I-cycles (CICY) routine. The file mask byte has been reset to zero, and thus, allows the processing of any seek command. The SIO instruction specifies the channel, the file control, and the file module. The CAW is entered in the channel common (DCLA) routine for the command address. After branching to the file routines, the first command is entered and decodes as the seek command. The seek command first enters the six-byte file address using the data address of the command. This provides the new cylinder and head to be set. The cylinder address for the current access positioning is entered from the 2311. This address is compared with the new address to determine the amount and the direction to move the access. The difference, the new cylinder address, and the new head address are sent to the 2311. After initiating a seek start for the 2311, the operation returns to I-cycles for the next instruction. When the 2311 has completed the operation, it raises the gated attention line to indicate device end. This initiates a trap request to either end the operation, or continue with the next chained command. The gated attention in the 2311 is reset and the file controls are reset before entering the next command.

● Diagram 5-301. Seek Operation, File



The cyclic-code test is made during the entry into each SIO operation to determine whether the file error detection circuits are functioning. This test makes use of the file diagnostic controls for the clock advances and the special test conditions. In diagnostic mode, the file interface is disconnected to ensure that the file records are not changed during the forced write operation. The file rings are first deoriented and then restarted at the index point with the diagnostic controls. The write-clock-gate trigger is controlling the clock operation, and advances are made by forcing the write-phase-A line.

Data bytes are forced into the write buffer and then transferred to the read buffer when the clock reaches bit-ring 7. Tests are made to determine that the entries are correct and that both registers are advanced serially from their controls. The bits serially reading from the read buffer enter the cyclic-code register for later tests. Two full bytes are shifted out of the read buffer to fill the cyclic-code register.

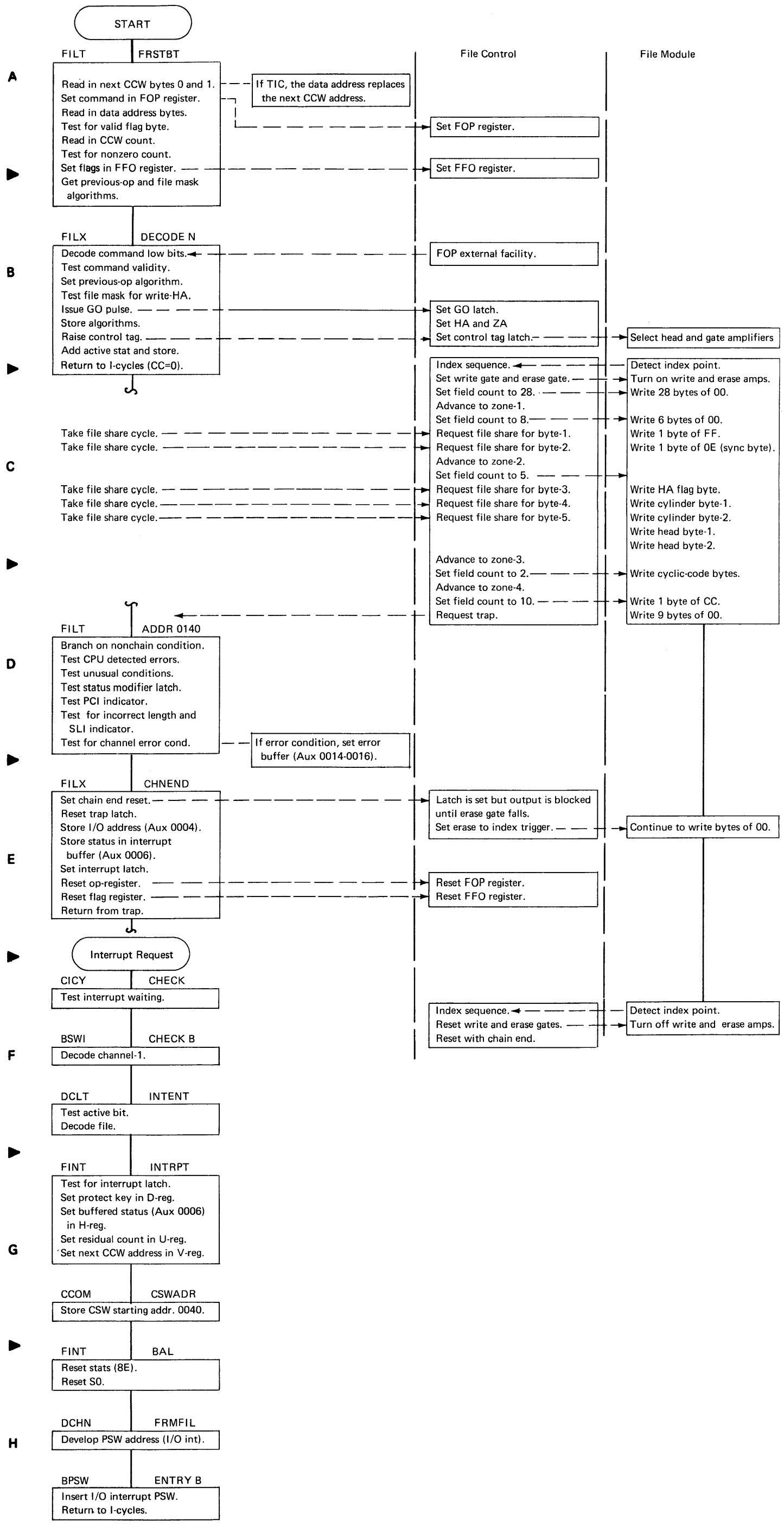
After loading the cyclic-code register, the ring is advanced to zone-3 and the diagnostic compare gate is set to test the cyclic-code compare and the data compare circuits. The separate-data-bit trigger is forced with the diagnotic control to provide a compare bit. The CC-error and the unequal-compare conditions are tested and reset after each bit-ring advance. If the results of all tests are correct, the diagnostic controls are reset and the file controls are reinitialized. The SIO operation is then performed as specified.

A failure to match any of the test conditions causes a branch to the error ending. The diagnostic controls and the file controls are reset. This routine also sets the CC-error sense bit before ending the SIO operation.

*All of the error test conditions branch to a common ending sequence if the conditions do not match. If this address is used to set the hard-stop, the W-register contains the address of the branch word plus-2. The numbered items all branch from a common test routine and result in the same W-register address. In each of these cases, the P1-register is loaded with the test conditions. A display of the P1 information points to the error condition as follows:

1	P1=DF	5	P1=0A
2	P1=DF	6	P2=4E
3	P1=82	7	P1=7A
4	P1=87	8	P1=3A
		9	P1=5B

● Diagram 5-302. 510 Cyclic Code Test



● Diagram 5-303. Write Home Operation, File

The write home address command for the file cannot be performed without first setting the file mask to allow the operation. This diagram assumes that the file mask command has been executed and that the write home address command is chained to it but that no other command follows. The operation remains in the initial sequence after setting the mask and returns to the trap routine to enter the next CCW. The new command is entered and decoded as the write home address. The flags, the data address, and the count are also entered from the CCW.

A test is made for the file mask condition to allow the operation. The file control waits for the 2311 to reach the index point before starting the write operation by setting the rings to the home address field and zone-A. After writing the home address gap, the home address is written with its cyclic-code bytes. The device end condition for the command initiates a trap request for the next command. When no command is chained, the GO pulse is not raised before the end of zone-4 and results in the setting of the erase to index latch. The microroutine sets the interrupt latch and loads the buffer before ending the operation.

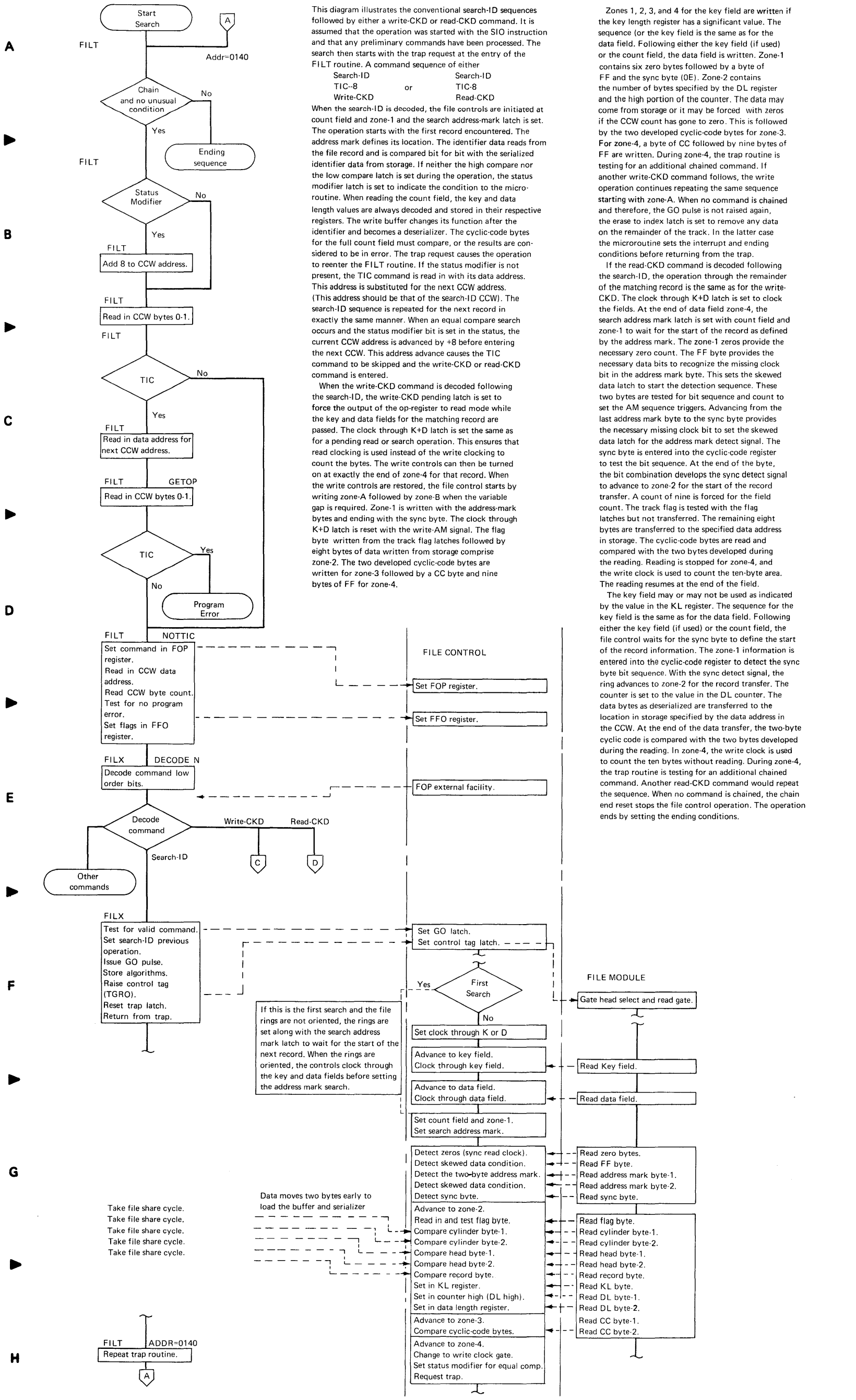
The interrupt routine loads the ending information into the CSW for program analysis when permitted by the system mask.

2 3 4 5 6

The read-HA operation has less restrictions than the other commands for use. It does not require a previous search, mask, or seek operation. It is assumed for this diagram that a seek command that caused access motion has preceded, and therefore, the entry is made through the trap routine. It is also assumed that no command follows. If the command is chained, the operation would branch at the second entry of the trap routine.

The read-HA requires the index point and the rings set to HA field and zone-A. The file control waits for the index point indication from the disk file before advancing. A space of nineteen bytes is clocked in before advancing to zone-1. No address-mark is used with the home address field. The read data is entered into the cyclic code register to sample the bits for the sync byte. When the last five bits of the byte are sensed in the correct order, the sync detect signal is developed to advance the ring to zone-2. A field count of five is set into the counter. All five bytes are deserialized and transferred to the storage area defined by the data address of the CCW. The flag byte is also used to set the track flag latches. During zone-3 the two byte cyclic code developed while reading the five bytes is compared with the two bytes read from the track. In zone-4 the write clock is used to count the ten bytes without reading. During zone-4, the trap routine is testing for an additional chained command. When no command is chained, the chain end reset stops the file control operation. The operation ends by storing the interrupt buffer, setting the interrupt latch, and perform the necessary resets to end the sequence before returning from the trap.

● Diagram 5-304. Read Home Address Operation, File



This diagram illustrates the conventional search-ID sequences followed by either a write-CKD or read-CKD command. It is assumed that the operation was started with the SIO instruction and that any preliminary commands have been processed. The search then starts with the trap request at the entry of the FILT routine. A command sequence of either

Search-ID		Search-ID
TIC--8	or	TIC-8
Write-CKD		Read-CKD

When the search-ID is decoded, the file controls are initiated at count field and zone-1 and the search address-mark latch is set. The operation starts with the first record encountered. The address mark defines its location. The identifier data reads from the file record and is compared bit for bit with the serialized identifier data from storage. If neither the high compare nor the low compare latch is set during the operation, the status modifier latch is set to indicate the condition to the micro-routine. When reading the count field, the key and data length values are always decoded and stored in their respective registers. The write buffer changes its function after the identifier and becomes a deserializer. The cyclic-code bytes for the full count field must compare, or the results are considered to be in error. The trap request causes the operation to reenter the FILT routine. If the status modifier is not present, the TIC command is read in with its data address. This address is substituted for the next CCW address. (This address should be that of the search-ID CCW). The search-ID sequence is repeated for the next record in exactly the same manner. When an equal compare search occurs and the status modifier bit is set in the status, the current CCW address is advanced by +8 before entering the next CCW. This address advance causes the TIC command to be skipped and the write-CKD or read-CKD command is entered.

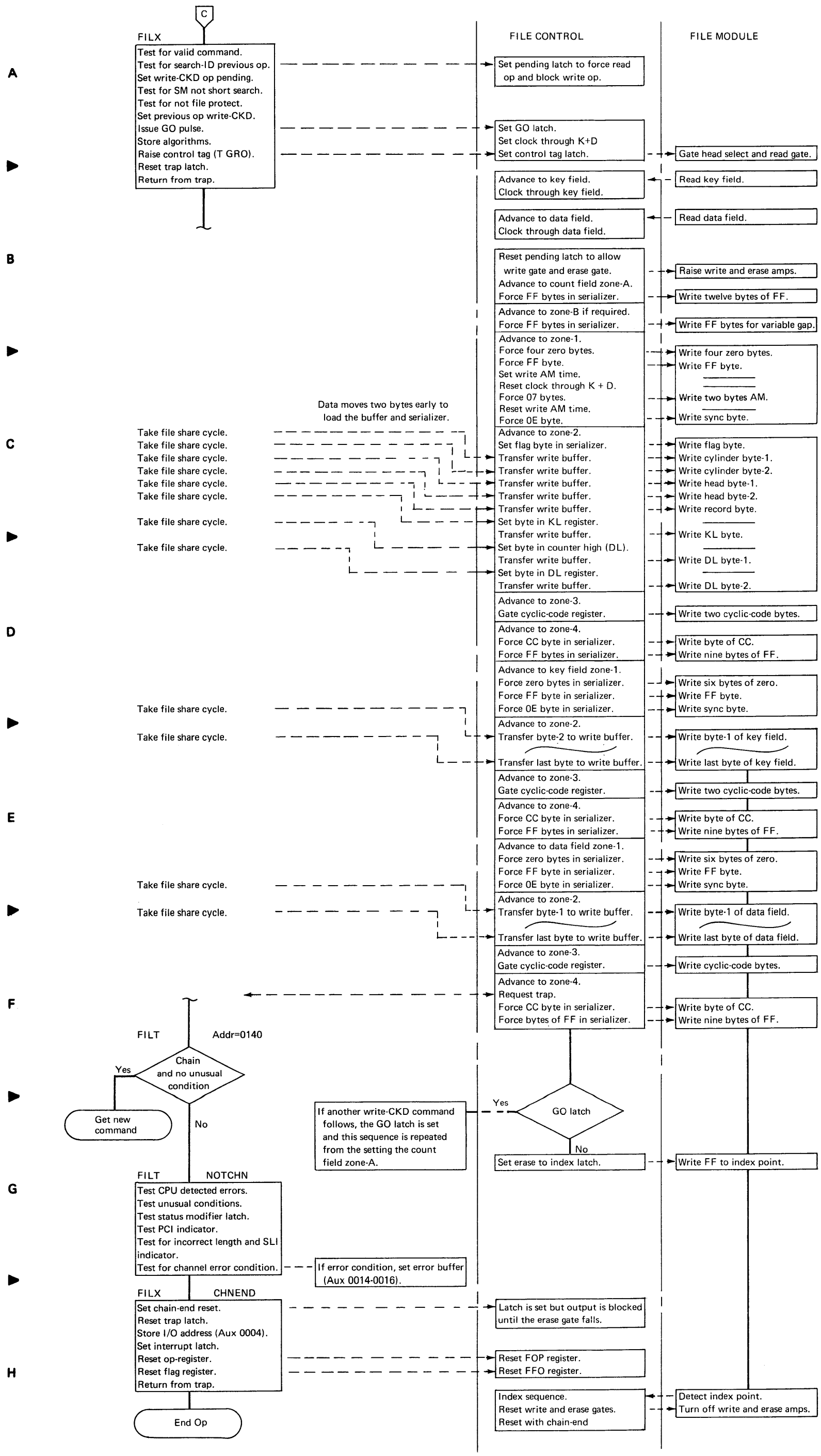
When the write-CKD command is decoded following the search-ID, the write-CKD pending latch is set to force the output of the op-register to read mode while the key and data fields for the matching record are passed. The clock through K+D latch is set the same as for a pending read or search operation. This ensures that read clocking is used instead of the write clocking to count the bytes. The write controls can then be turned on at exactly the end of zone-4 for that record. When the write controls are restored, the file control starts by writing zone-A followed by zone-B when the variable gap is required. Zone-1 is written with the address-mark bytes and ending with the sync byte. The clock through K+D latch is reset with the write-AM signal. The flag byte written from the track flag latches followed by eight bytes of data written from storage comprise zone-2. The two developed cyclic-code bytes are written for zone-3 followed by a CC byte and nine bytes of FF for zone-4.

Zones 1, 2, 3, and 4 for the key field are written if the key length register has a significant value. The sequence (or the key field is the same as for the data field. Following either the key field (if used) or the count field, the data field is written. Zone-1 contains six zero bytes followed by a byte of FF and the sync byte (0E). Zone-2 contains the number of bytes specified by the DL register and the high portion of the counter. The data may come from storage or it may be forced with zeros if the CCW count has gone to zero. This is followed by the two developed cyclic-code bytes for zone-3. For zone-4, a byte of CC followed by nine bytes of FF are written. During zone-4, the trap routine is testing for an additional chained command. If another write-CKD command follows, the write operation continues repeating the same sequence starting with zone-A. When no command is chained and therefore, the GO pulse is not raised again, the erase to index latch is set to remove any data on the remainder of the track. In the latter case the microroutine sets the interrupt and ending conditions before returning from the trap.

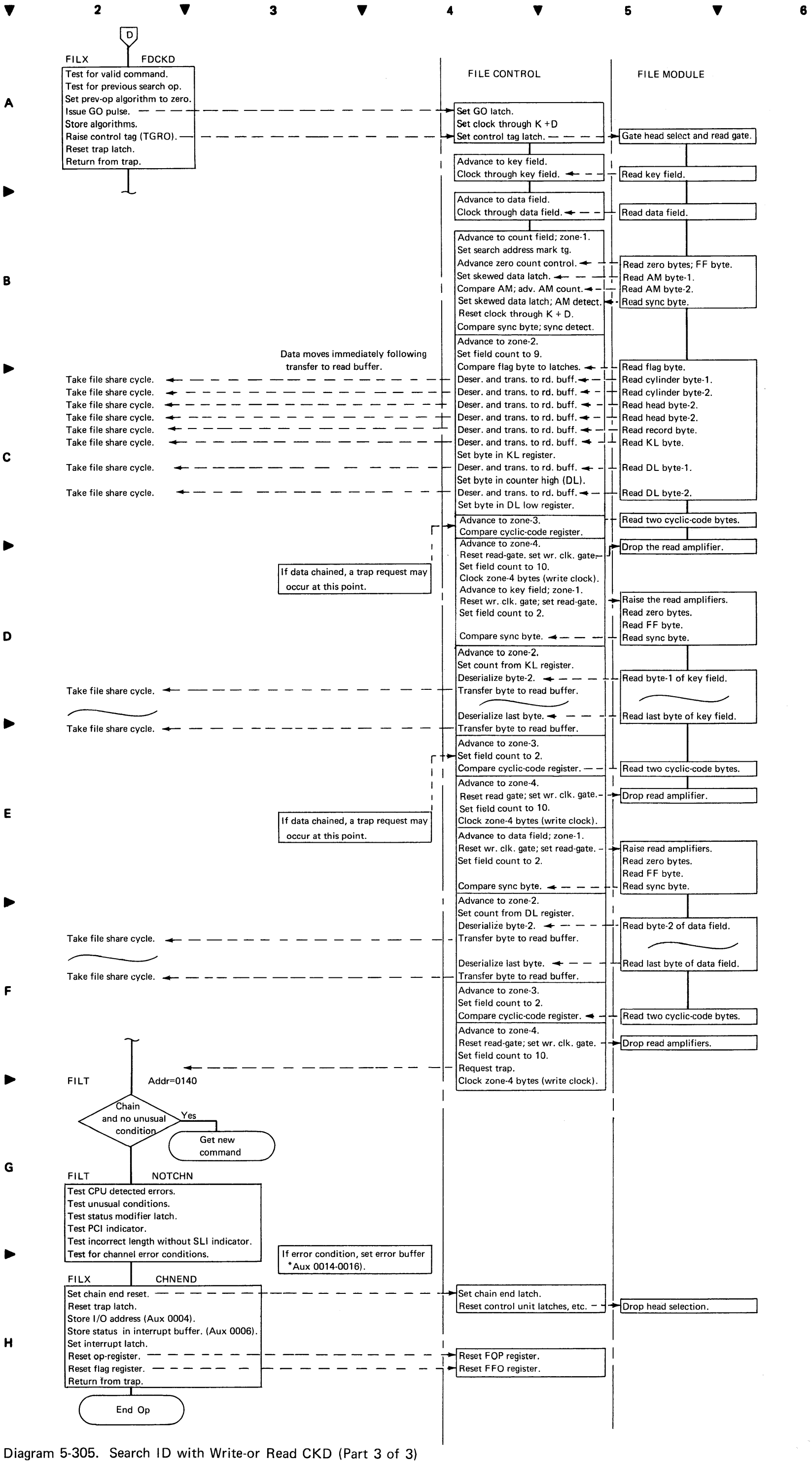
If the read-CKD command is decoded following the search-ID, the operation through the remainder of the matching record is the same as for the write-CKD. The clock through K+D latch is set to clock the fields. At the end of data field zone-4, the search address mark latch is set with count field and zone-1 to wait for the start of the record as defined by the address mark. The zone-1 zeros provide the necessary zero count. The FF byte provides the necessary data bits to recognize the missing clock bit in the address mark byte. This sets the skewed data latch to start the detection sequence. These two bytes are tested for bit sequence and count to set the AM sequence triggers. Advancing from the last address mark byte to the sync byte provides the necessary missing clock bit to set the skewed data latch for the address mark detect signal. The sync byte is entered into the cyclic-code register to test the bit sequence. At the end of the byte, the bit combination develops the sync detect signal to advance to zone-2 for the start of the record transfer. A count of nine is forced for the field count. The track flag is tested with the flag latches but not transferred. The remaining eight bytes are transferred to the specified data address in storage. The cyclic-code bytes are read and compared with the two bytes developed during the reading. Reading is stopped for zone-4, and the write clock is used to count the ten-byte area. The reading resumes at the end of the field.

The key field may or may not be used as indicated by the value in the KL register. The sequence for the key field is the same as for the data field. Following either the key field (if used) or the count field, the file control waits for the sync byte to define the start of the record information. The zone-1 information is entered into the cyclic-code register to detect the sync byte bit sequence. With the sync detect signal, the ring advances to zone-2 for the record transfer. The counter is set to the value in the DL counter. The data bytes as deserialized are transferred to the location in storage specified by the data address in the CCW. At the end of the data transfer, the two-byte cyclic code is compared with the two bytes developed during the reading. In zone-4, the write clock is used to count the ten bytes without reading. During zone-4, the trap routine is testing for an additional chained command. Another read-CKD command would repeat the sequence. When no command is chained, the chain end reset stops the file control operation. The operation ends by setting the ending conditions.

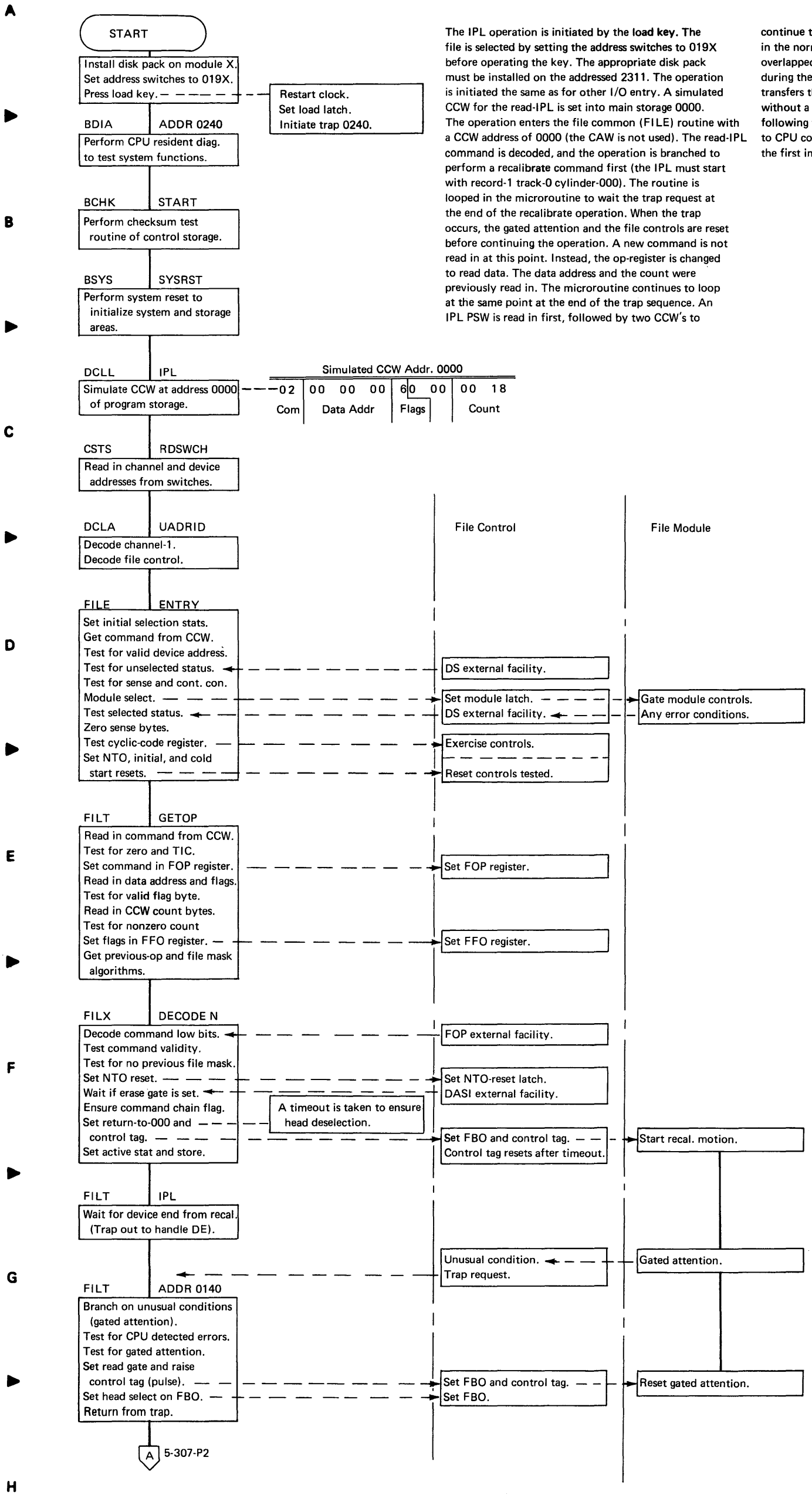
● Diagram 5-305. Search-ID with Write- or Read-CKD (Part 1 of 3)



● Diagram 5-305. Search-ID with Write- or Read-CKD (Part 2 of 3)

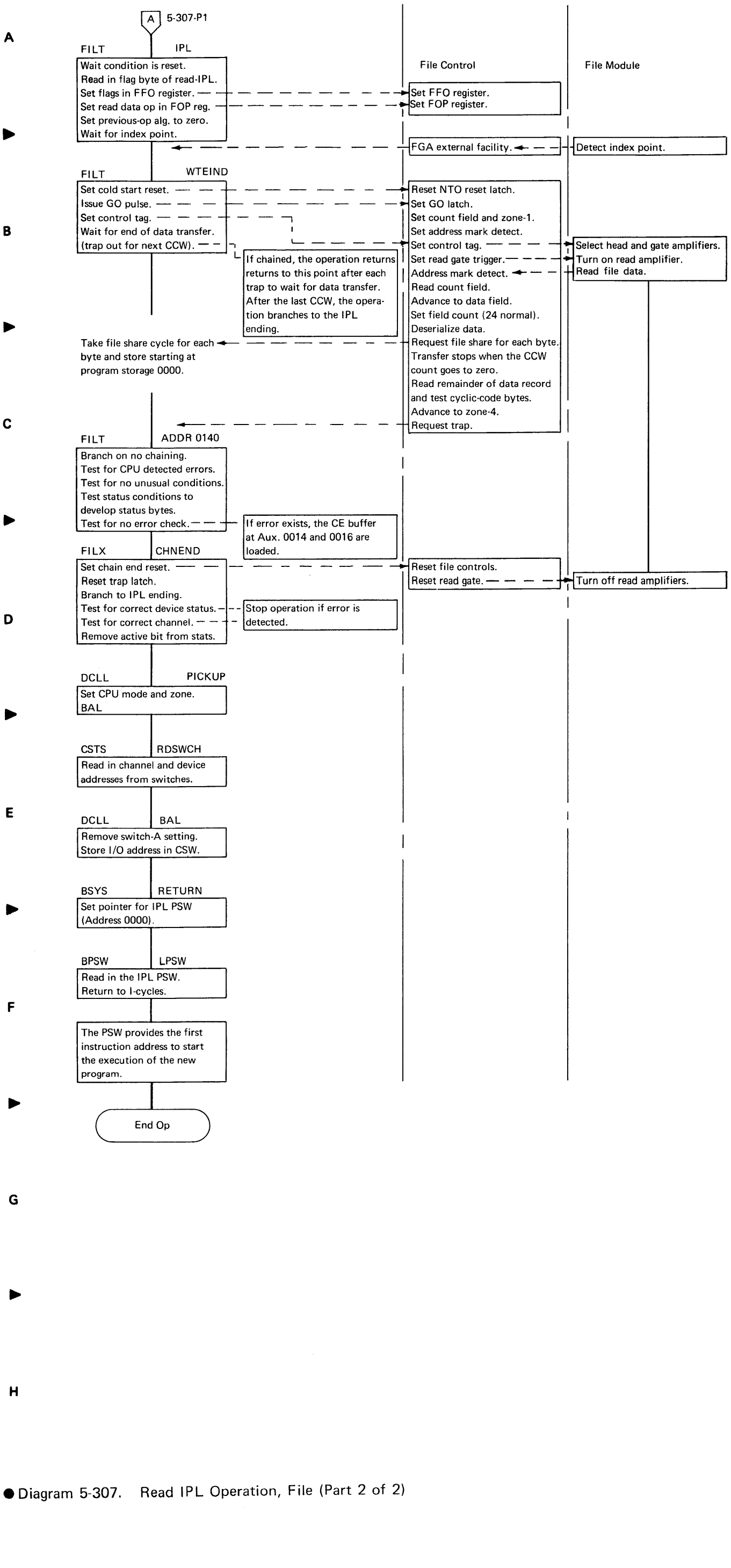


● Diagram 5-305. Search ID with Write-or Read CKD (Part 3 of 3)



The IPL operation is initiated by the **load key.** The file is selected by setting the address switches to 019X before operating the key. The appropriate disk pack must be installed on the addressed 2311. The operation is initiated the same as for other I/O entry. A simulated CCW for the read-IPL is set into main storage 0000. The operation enters the file common (FILE) routine with a CCW address of 0000 (the CAW is not used). The read-IPL command is decoded, and the operation is branched to perform a recalibrate command first (the IPL must start with record-1 track-0 cylinder-000). The routine is looped in the microroutine to wait the trap request at the end of the recalibrate operation. When the trap occurs, the gated attention and the file controls are reset before continuing the operation. A new command is not read in at this point. Instead, the op-register is changed to read data. The data address and the count were previously read in. The microroutine continues to loop at the same point at the end of the trap sequence. An IPL PSW is read in first, followed by two CCW's to continue the file operation. The operation is executed in the normal manner except that no CPU operation is overlapped. Instead, the microroutine continues to loop during the reading periods. The normal file share cycle transfers the data. The operation ends when a CCW without a command chain flag is processed. During the following trap sequence, the operation is branched back to CPU control to end the routine. The IPL PSW provides the first instruction address to start the program operation.

● Diagram 5-307. Read IPL Operation, File (Part 1 of 2)



● Diagram 5-307. Read IPL Operation, File (Part 2 of 2)

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

CHANNEL OPERATION (Start I/O, Read Command) On Selector Channel

Read out and decode instruction (9C). In routine DCLA, test to see that machine is in supervisor state.
Determine that I/O operation to be performed and branch accordingly. Read CAW in two-byte increments.
A See that CCW is on 8-byte boundary. Identify channel involved and branch to proper routine.
Test if file operation. Test if burst channel operation.

In routine DCLB, test active bit, set condition code in PSW and set to channel mode. Determine if specified
I/O device is fully buffered. Test if inbound or outbound command. Check if data chain is indicated.
Test for nonzero byte count. Branch to initial selection outine, DCLC.

▶ Routine DCLC

Test for program control interrupt. If PCI, set channel 1 interrupt latch

Set initial selection latch

Place Device Address on Bus-Out — Device Address (Bus- Out) →
B

Set Address-Out signal (tag) — Address-Out →

Set Select-Out — Select-Out and Hold-Out →

Address-Out reset by the microprogram upon receipt of Op-In. — ← Operational-In (generated by I/O device)

▶ ← Address-In (tag)

← Device Address (bus-in)

Test address parity and match. — Command (bus-out) →

C — Command-Out →

Address-In drops

Command-Out drops.

← Status (bus-in)

▶ ← Status-In (tag)

Set Service-Out — Service-Out →

Status-In drops

D Service-Out drops.

Set burst latch and turn on active bit in 8E K addressable auxiliary storage.
Select-Out is still up, holding the device on the interface.

Mode register set to CPU mode and program returns to I cycles. When the first byte of data is ready
▶ to be transmitted from the I/O drvice to the CPU, the device raises service-in causing a hardware trap
to the data handling routine (DCLD).

Channel Data Request is developed and causes the address of the first — ← Service-In, No Tag-Out
instruction in the data loop to be generated.

← Data (bus-in)

E — Service-Out →

Service-In is reset

Service-Out is reset

The data loop is repeated until all data has been transferred, at which time the ending
▶ sequence begins. Status-In causes a hardware trap to the status handling routine (DCLE)

DCLE and DCLC routines

← Status (bus-in)

Status-In

F With status-in up, the burst latch on, and data chain request off, channel 0 trap request is generated. This causes the address of the first microword of the ending sequence to be generated and gated to the storage address assembler. Thus the ending sequence is executed.

Test parity of the status byte; test for presence of chain command; test for PCI.
Store status, set interrupt buffer latch. — Service-Out →
▶

(signals acceptance of status)

Operational-In drops

Return to original routine.

G

▶

H

Diagram 5-401. Operation Chart Start I/O Burst Channel

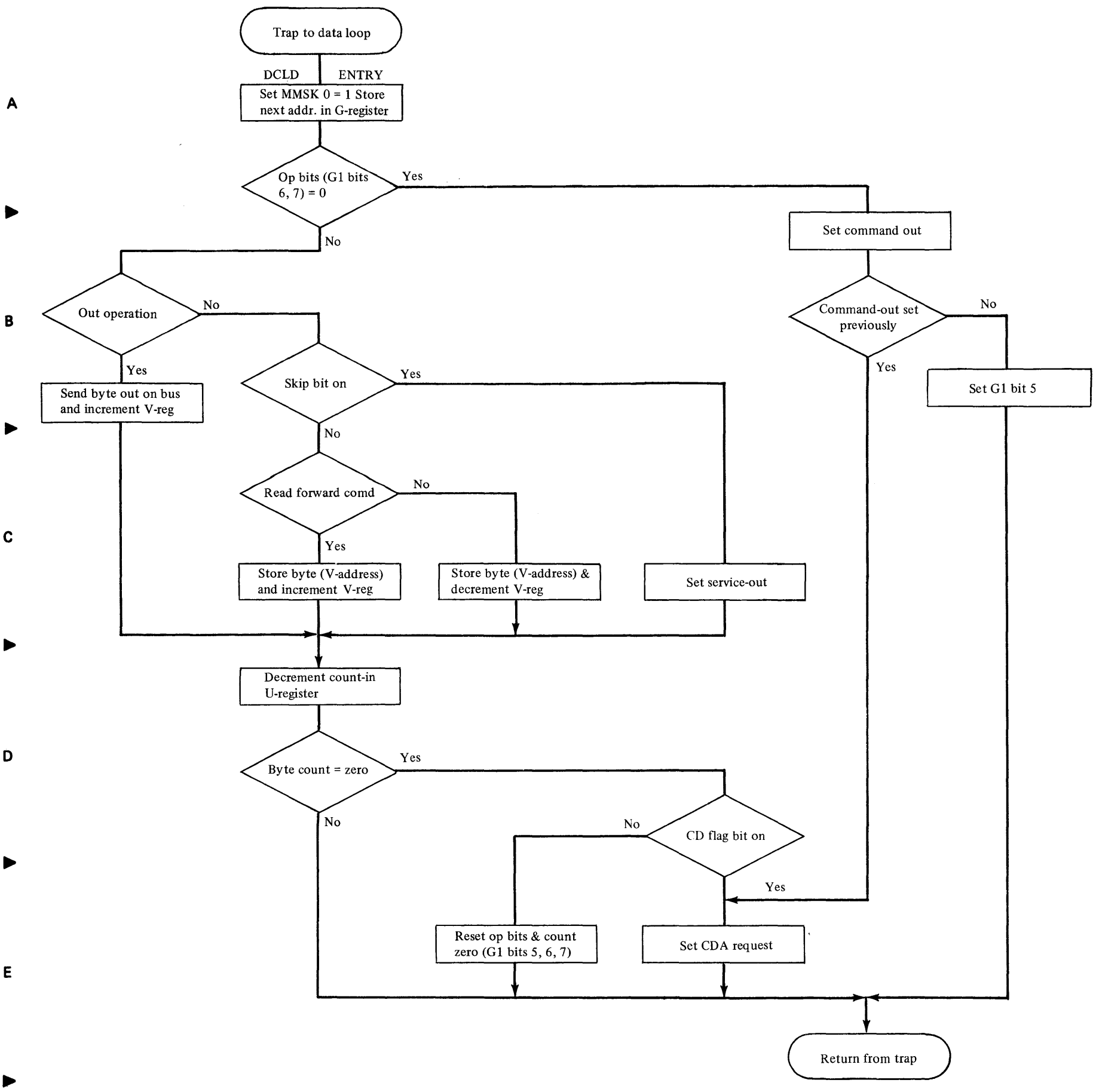


Diagram 5-403. Flowchart of Data Loop for Selector Channel (Routine DCLD)

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

CHANNEL OPERATION (Byte Mode)

	CPU	CHANNEL and I/O DEVICE
A	Read and decode instruction in microroutine CICY and branch to DCLA	
	DCLA Machine must be in supervisor state. (Check program mask)	
	Determine I/O operation to be performed and branch to the proper routine.	
▶	Determine that channel 0 is specified. Construct UCW address, using the device and control unit address. Test active bit. Branch to DCLB.	
B	DCLB Fetch and edit the CCW. Test for TIC command. (TIC should not occur as first command.) Test for valid flags (3 low-order flag bits must be zero). If flags present, branch to DCLR to handle. Test for data chain indication. Test Op bits and branch accordingly (outbound, in forward, in backward). Test for non-zero byte count. Construct UCW using information in CCW. Branch to DCLC.	
▶	DCLC Test for presence of PCI bit. If present, set channel 1 interrupt latch. Perform initial selection placing I/O device on interface.	
C	Set initial selection latch.	
	Place device address on Bus-Out	Bus-Out (address) →
	Set Address-Out tag.	Address-Out →
	Set Select-Out.	Select-Out →
	Set Hold-Out	Hold-Out →
▶	Op-In generated by I/O device)	Operational-In ←
	Drop Address-Out	
	(Device address is on Bus-In.)	Address-In ←
D		Bus-In (address) ←
	Place Command on Bus-Out.	Bus-Out (Command) →
	Test address on Bus-In for parity error and agreement with Address-Out.	
	Set Command-Out	Command-Out →
▶	Drop Select-Out.	
	Drop Hold-Out.	
	Drop Address-In and Command-Out.	
E	Set Status-In	Status-In ←
	Place status on Bus-In	Bus-In (status) ←
	Test for parity error; set Service-Out.	Service-Out →
▶	Drop Status-In, Service-Out and Operational-In. Set condition code 0 and active bit. Return to I-Cycles.	
F		
▶		
G		
▶		
H		

Diagram 5-405. Operation Chart for Start I/O on Byte Channel

Figure 5-407 Flowchart of Data Loop in Byte Channel Operation.

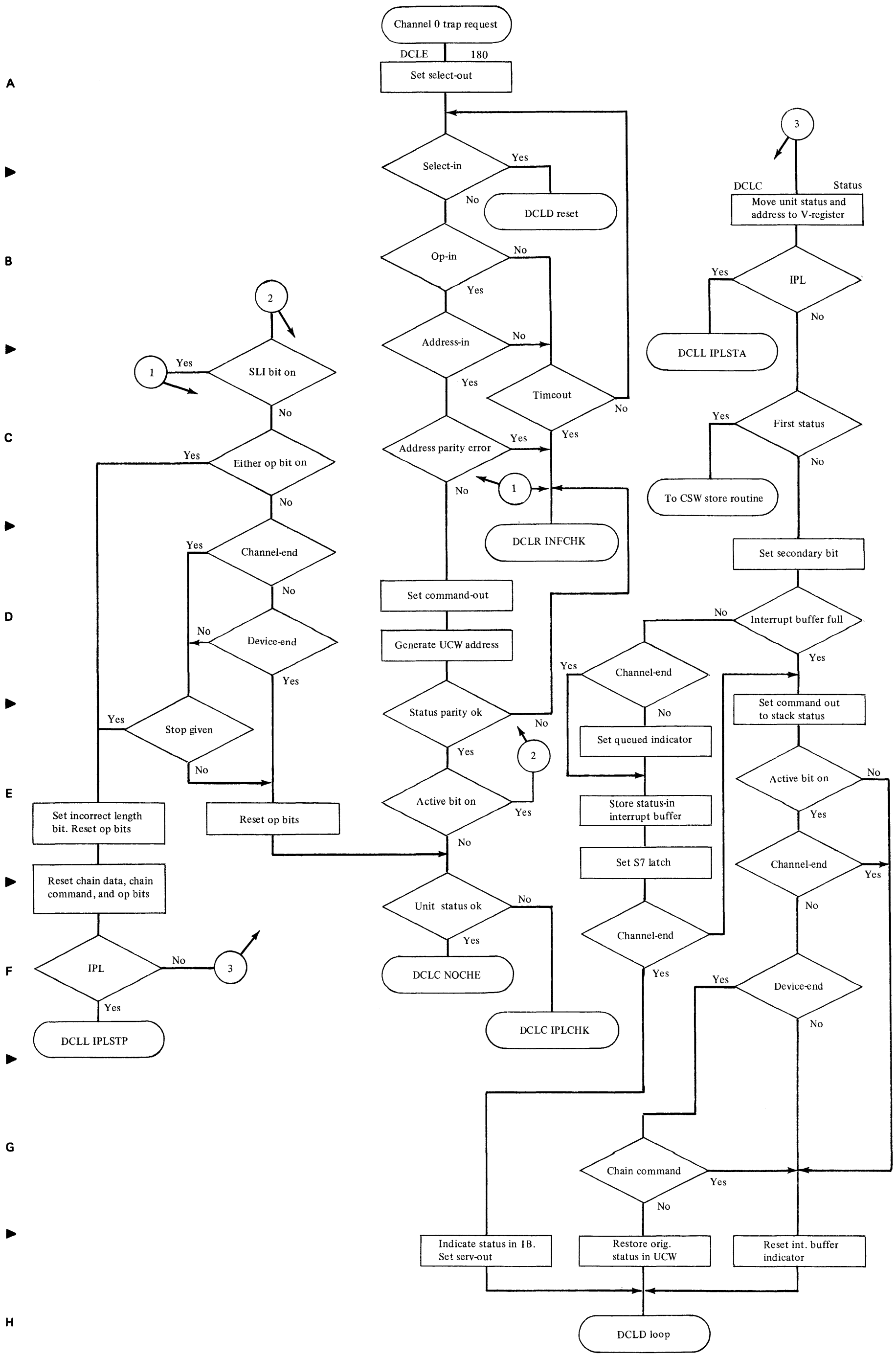
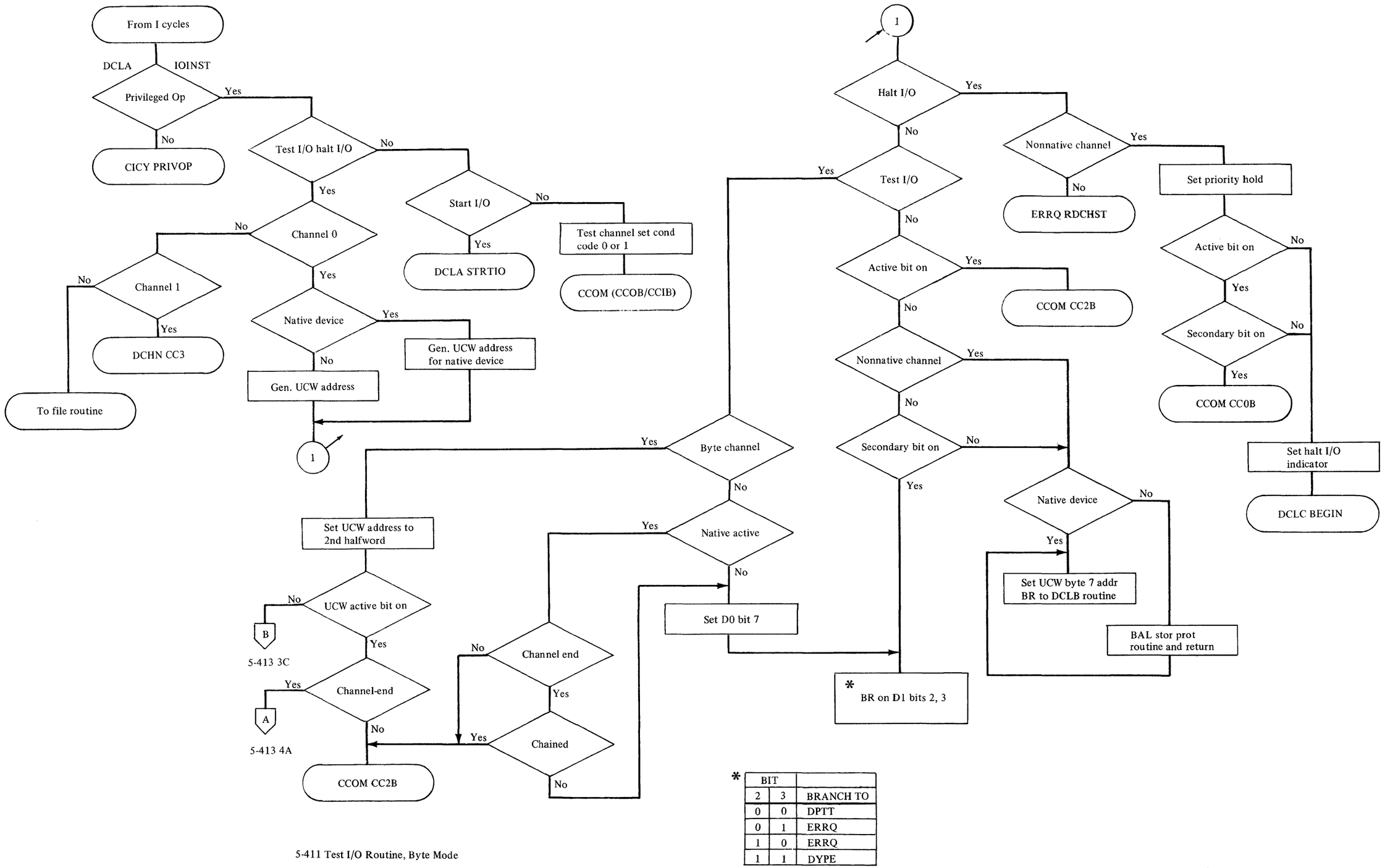


Diagram 5-409. Ending Operation on Byte Channel



5-411 Test I/O Routine, Byte Mode

*

BIT		
2	3	BRANCH TO
0	0	DPTT
0	1	ERRQ
1	0	ERRQ
1	1	DYPE

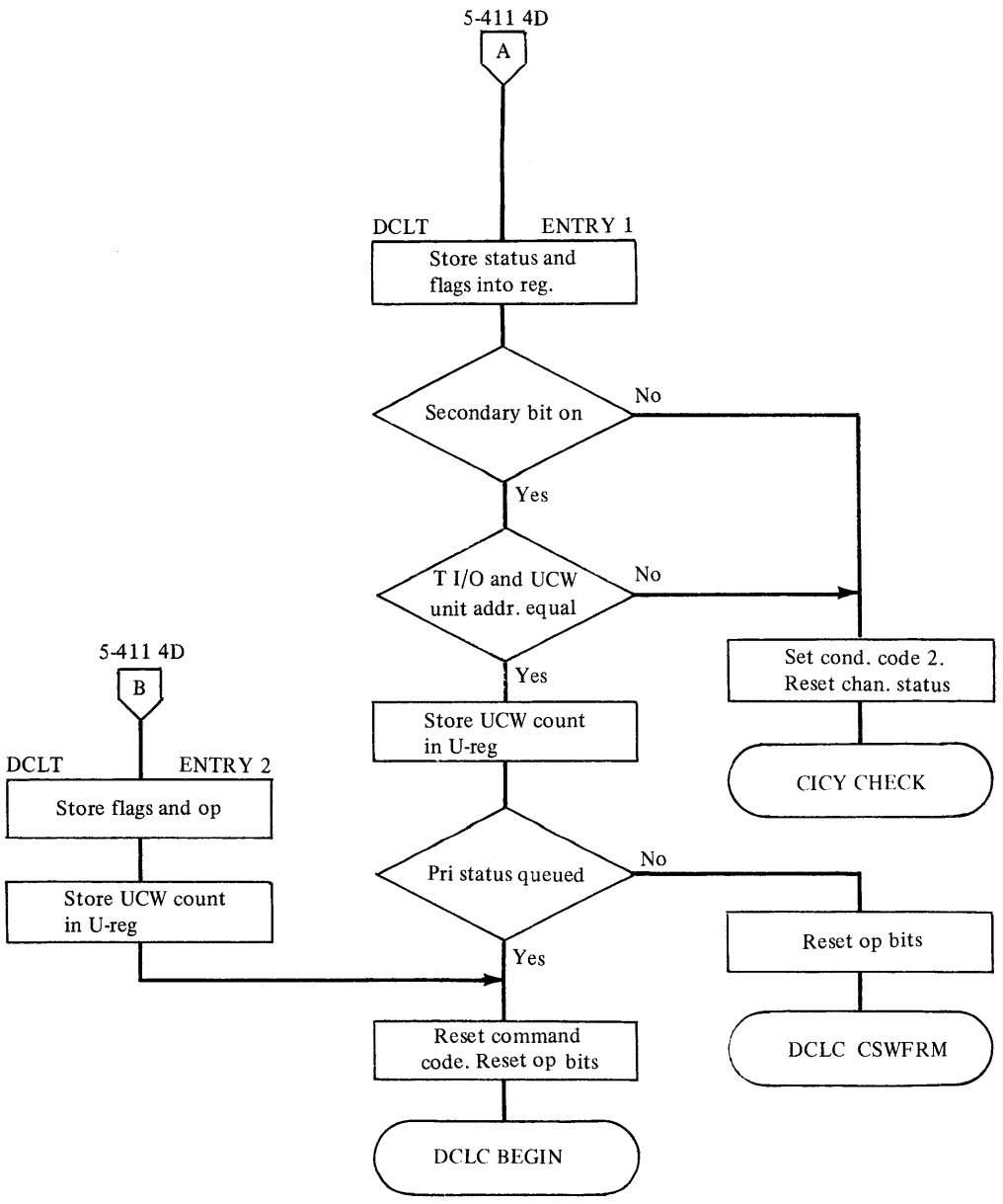
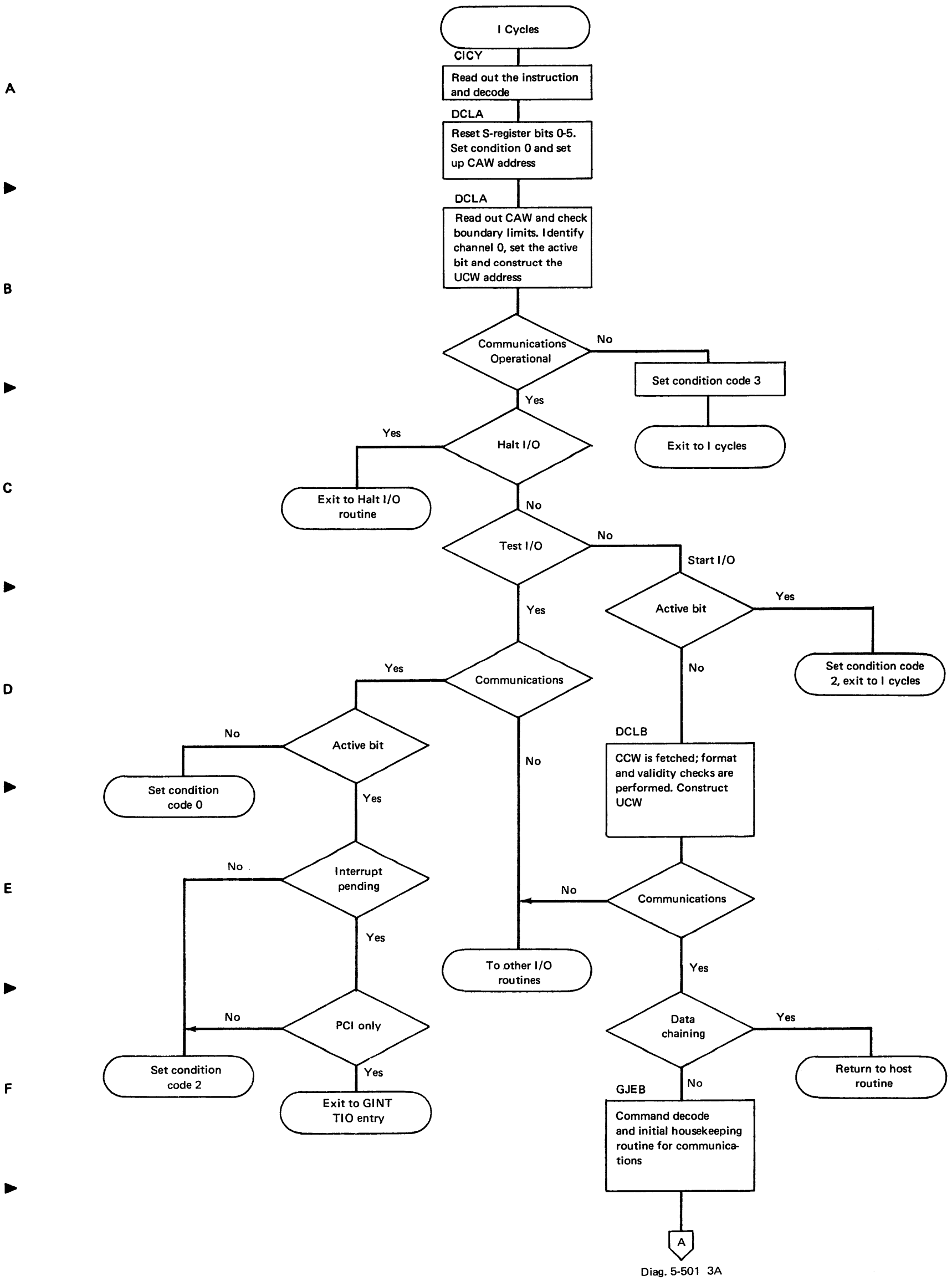


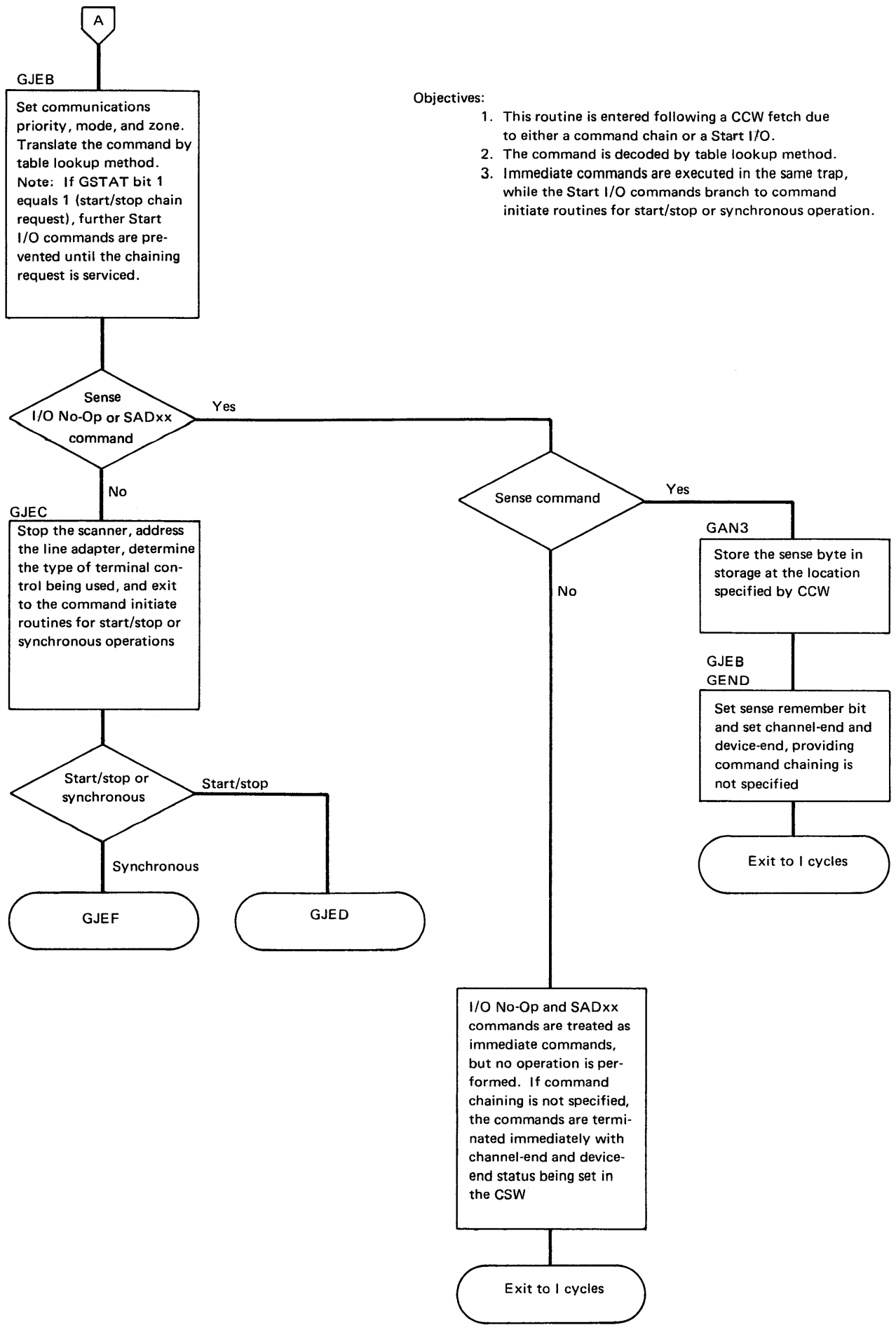
Diagram 5-413. Test I/O Routine, Byte Channel



Diag. 5-501 3A

● Diagram 5-500. Communications Command Decode

Diag 5-500 5G



Objectives:

1. This routine is entered following a CCW fetch due to either a command chain or a Start I/O.
2. The command is decoded by table lookup method.
3. Immediate commands are executed in the same trap, while the Start I/O commands branch to command initiate routines for start/stop or synchronous operation.

● Diagram 5-501. Communications Command Decode Initial Housekeeping

2 3 4 5 6

Start/Stop Read command

A

An enable command must precede a read command. The enable command turns on the enable latch

GJED

A read Start I/O command is decoded by table look-up. The scanner is stopped and the line adapter is addressed. Set timeout enable and remember latches (Note 1). Ensure data set ready (DSR) and restart the scanner. The microprogram returns to I cycles

B

When the start bit is received, it is checked to ensure that it is not a false start, (through hardware circuits) and the strobe is started.

C

GJE1

Strobe transition forces a bit service trap at address 01E0. It takes nine bit service traps to receive the character into the assembler/disassembler. (See chart in 3 and 4B, C.) The last bit service trap (stop bit) transfers the assembled character into the LCW buffer and forces a character service trap

D

GSRO

A character service trap checks the parity of the character and checks for control character. The character is transferred from the LCW buffer to main storage. Restart the scanner and exit the trap

E

GEND

After the LRC has been checked in a character service trap, channel-end and device-end are set

F

End command

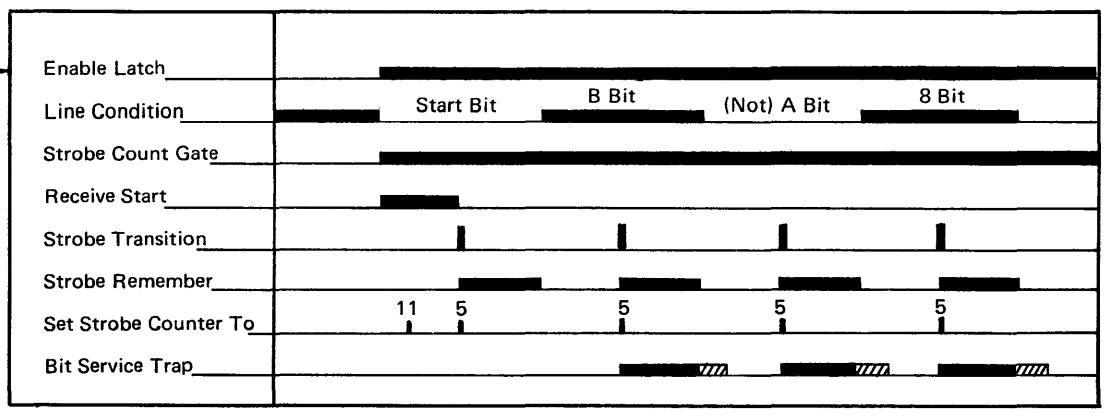
Objectives:

1. Receive the following characters. V, (B), LRC.
2. Transfer the character to main storage.
3. Set channel-end and device-end.

Note: Program should chain to a write command to transmit the answerback.

Bit Service Trap	G0	G1	Bit Position	
1	EX	0000 0000	B of V	
2	3X	0000 0001	A of V	
3	4X	0000 0010	8 of V	
4	5X	0000 0101	4 of V	
5	6X	0000 1010	2 of V	
6	7X	0001 0101	1 of V	
7	8X	0010 1010	C of V	
8	9X	0000 0000	Stop	→ Character Service Trap
	EX	0000 0000	Start	
9	EX	0000 0000	B of (B)	
10	3X	0000 0001	A of (B)	
11	4X	0000 0011	8 of (B)	
12	5X	0000 0111	4 of (B)	
13	6X	0000 1111	2 of (B)	
14	7X	0001 1110	1 of (B)	
15	8X	0011 1101	C of (B)	
16	9X	0000 0000	Stop	→ Character Service Trap
	EX	0000 0000	Start	
17	EX	0000 0000	B of LRC	
18	3X	0000 0000	A of LRC	
19	4X	0000 0001	8 of LRC	
20	5X	0000 0010	4 of LRC	
21	6X	0000 0101	2 of LRC	
22	7X	0000 1011	1 of LRC	
23	8X	0001 0111	C of LRC	
24	9X	0000 0000	Stop	→ Character Service Trap
25	CX	0000 0000	Stop	

Note: Additional bit service traps are taken to decrement the count in G0 and to monitor the line status.



GJE1

Note 1:

Timeout enable and remember latches are not turned on for Start/Stop inhibit commands. Inhibit commands are performed the same as read commands with this exception: Inhibit commands are issued normally to a keyboard device where the speed of operation is dependent upon operator capability.

G

H

● Diagram 5-502. Start/Stop Read Command

2 3 4 5 6

Objectives:

1. Set controls for transmit operation.
2. Transmit the following characters:

   V, Ⓑ , and LRC.
3. Set channel-end and device-end.

Note: Program should be chained to a read command to receive answerback.

Conditions:

1. Start/stop operation
2. IBM Type I terminal control
3. Data set ready and line adapter enabled.

GJED

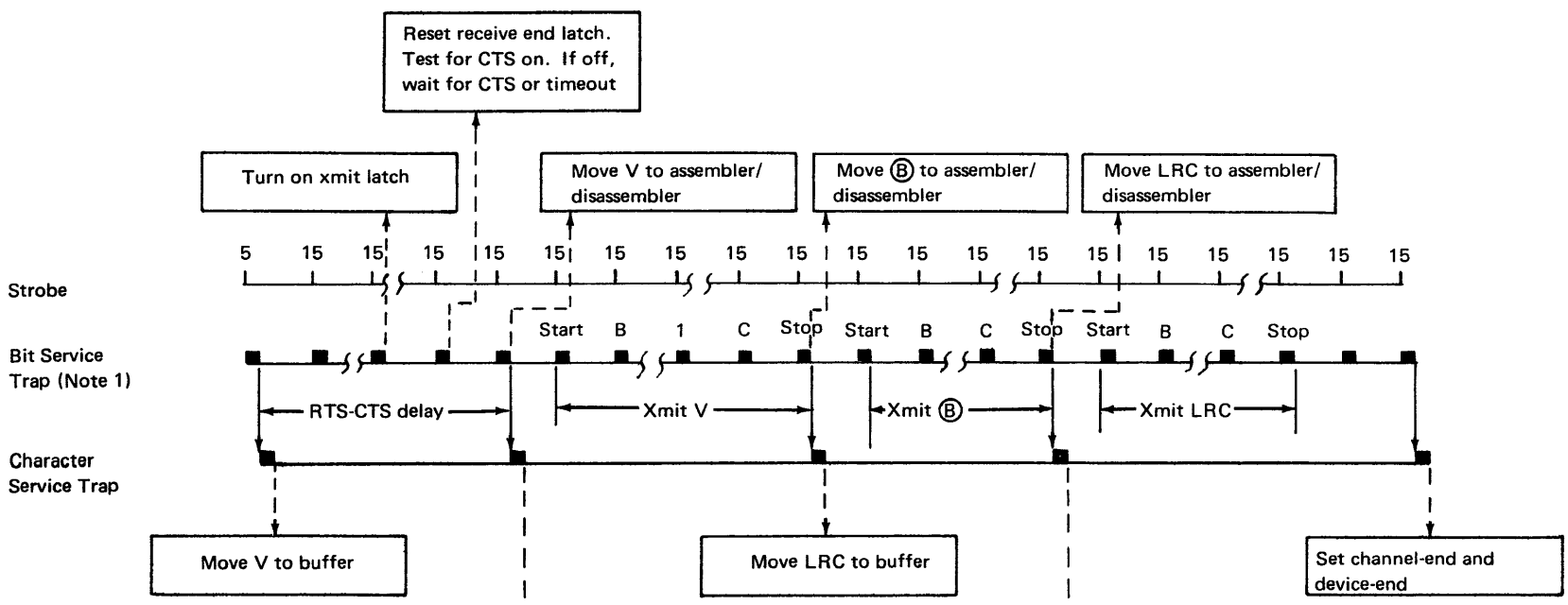
This routine sets write state and receive end latch for RTS-CTS delay. Start the strobe. Set timeout enable and remember latches. Set timeout command. Restart the scanner and exit routine

GJE1 (Bit Service Trap)

When the strobe count reaches count 15 (strobe transition), a bit service trap is forced starting at address 01E0. The first bit service trap forces a character service request. Approximately 9 bit service traps are required for RTS-CTS delay. The transmit latch is turned on after RTS delay has been completed. Bit service traps transmit the character serially by bit. The stop bit service trap moves the character serially by bit. The stop bit service trap moves the character from the LCW buffer to the assembler/ disassembler if the character service trap has occured. If not, a PAD character is transmitted. The stop bit service trap also forces a character service request

GSRO (Character Service Trap)

The character service trap routine moves the character from main storage to the LCW buffer. The character service trap also sets up the ending sequence prior to transmission of the LRC character. Channel-end and device-end are set in the character service trap following the LRC character



Note 1:
The operation of the bit service trap routine (GJE1) is dependent upon the bit count in the LCW.

Bit count 0 (Start)
Shift out start bit.
Set the bit count to first data bit.

Bit count 1 (First data)
Test for PAD character. If not a PAD character, test for transfer check or echo check, set the appropriate flags, set bit count to stop bit (count F), restart scanner and exit trap.
If PAD character is detected, bypass error checks, increment the bit count, shift out the start bit, restart the scanner and exit trap.

Bit count 2-8 (Normal data)
Test the bit for errors. If errors are detected, set appropriate flags, force bit count to F, restart the scanner and exit trap.
If no errors are detected, increment the bit count, restart the scanner and exit trap.

Bit Count 9 (Stop Bit)
Move character from LCW buffer to the assembler/disassembler. Force a character service trap request.

Ending Sequence
Two additional bit service traps (xmit end 1- and 2) are taken following the transmission of the LRC Stop.
The second bit service trap forces a character service trap request for channel-end and device-end.

● Diagram 5-503. Start/Stop Write Operation

2 3 4 5 6

A start/stop addressing operation is performed by a sequence of chained commands as follows.

Write Start I/O
Read
Write

Ⓒ A 1 →
← Ⓨ or Ⓝ
Text Ⓓ →

Ⓒ = control character
A = address character
1 = component select character
Ⓨ = positive acknowledgment
Ⓝ = negative acknowledgment
Ⓓ = end of address; text following

Write Start I/O

GJED

This routine sets write state in the LCW and turns on the receive end latch for RTS-CTS delay. Start the strobe. Set timeout enable and timeout remember latches, restart the scanner and exit routine.

Start the strobe counter. When the strobe count reaches 15, (strobe transition) a bit service trap is forced at address 01E0. Start a 3.5 second timeout.

GJE1

The first bit service trap generates a character service trap

GSRO

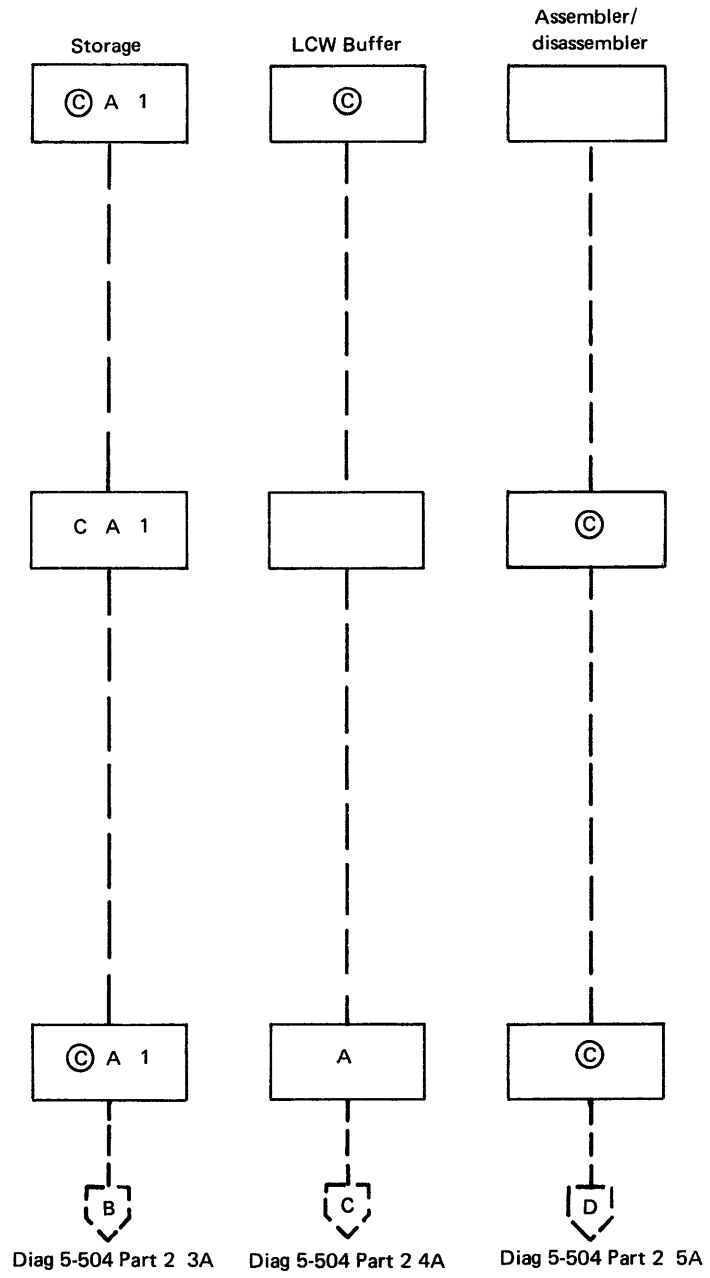
The character service trap fetches a character from storage (under control of the CCW byte count), determines that it is a control character, and places the Ⓒ character in the LCW buffer. Write state and IBM control mode are set in the LCW state field. Restart the scanner and exit trap

GJE1

Approximately 9 bit service traps (under control of the strobe counter) are taken for RTS-CTS delay. The transmit latch (MDM 4-529) is set during this delay. When CTS (clear to send) becomes active, a character service trap is generated. Reset timeout indicator. Move Ⓒ to the assembler/disassembler, restart the scanner and exit trap.

GSRO

Move the address character (A) to the LCW buffer, decrement the count, restart the scanner and exit the trap.



A
Diag 5-504 Part 2 2A

● Diagram 5-504. Start/Stop Addressing Operation (Part 1 of 3)

2 3 4 5 6

Diag 5-504 Part 1 2G

A

GJE1

Nine bit service traps are taken to transmit the Ⓒ The stop bit service trap transfers the address character to the assembler/disassembler and generates a character service trap.

GSRO

Move the component select character (1) to the LCW buffer, decrement the count, restart the scanner and exit the trap.

GJE1

Nine bit service traps are taken to send the address character. The stop bit service trap moves the component select character to the assembler/disassembler, generates a character service trap.

GSRO

Set LCW +0 for Xmit end sequence.

GJE1

Nine bit service traps are taken to send the component select character. The stop bit service trap generates a character service trap.

GSRO

This character service trap sets write end in the LCW state field and turns on the Start/Stop chain request latch. Restart the scanner and exit the trap.

E

Diag 5-504 Part 3 2A

Diag 5-504 Part 1 3G

B

Ⓒ A 1

Ⓒ A 1

Ⓒ A 1

Ⓒ A 1

Diag 5-504 Part 1 4G

C

1

Diag 5-504 Part 1 5G

D

A

A

1

1

Ⓒ

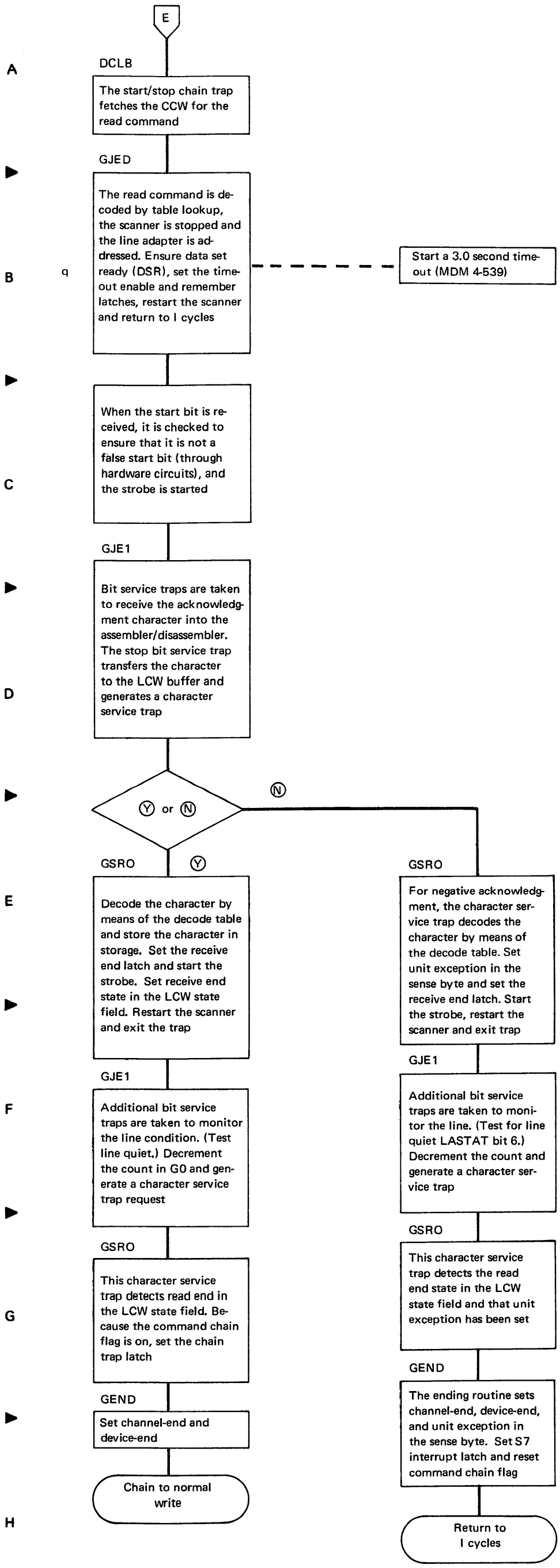
A

1

● Diagram 5-504. Start/Stop Addressing Operation (Part 2 of 3)

2 3 4 5 6

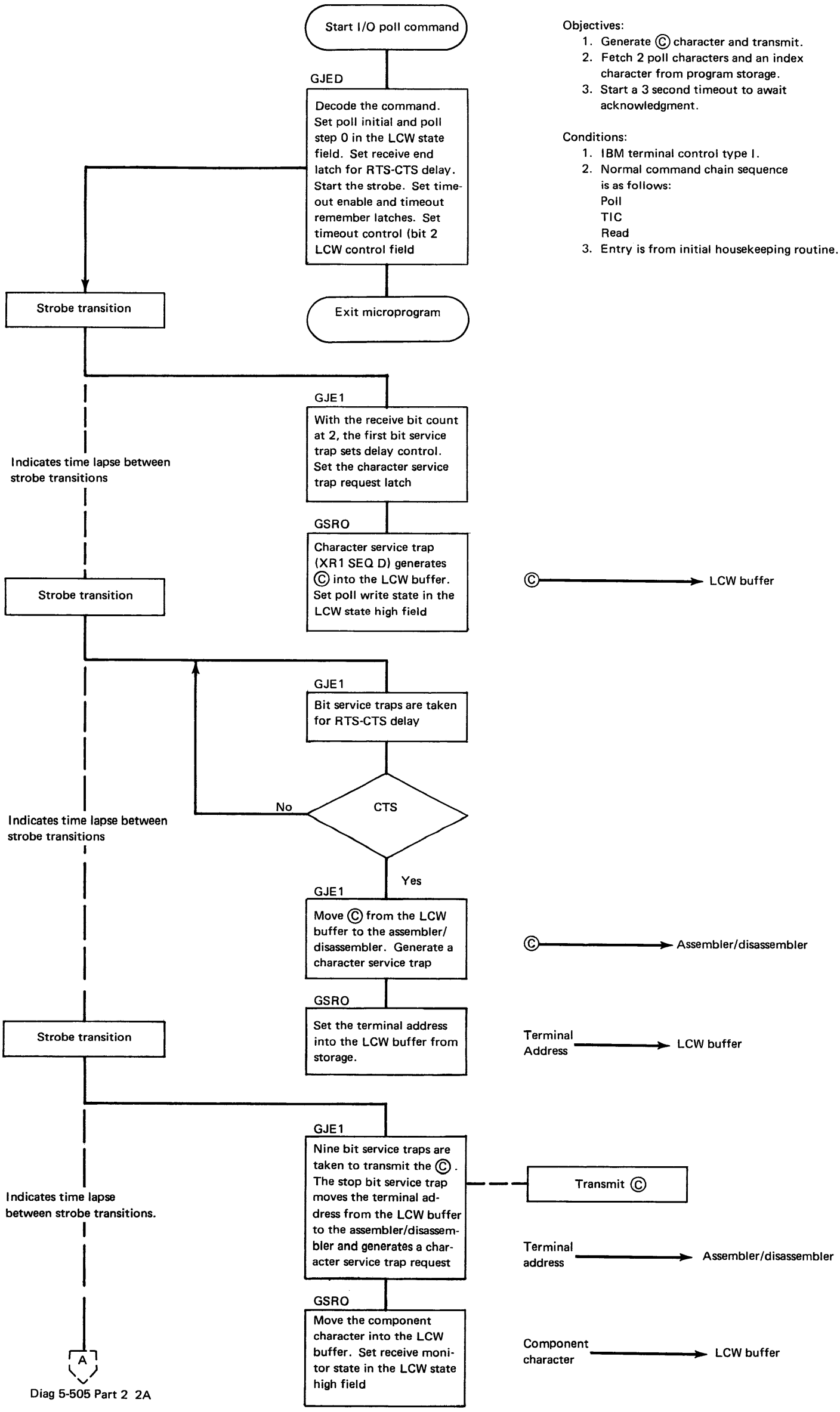
Diag 5-504 P2 2F



● Diagram 5-504. Start/Stop Addressing Operation (Part 3 of 3)

2 3 4 5 6

A B C D E F G H



Objectives:
1. Generate © character and transmit.
2. Fetch 2 poll characters and an index character from program storage.
3. Start a 3 second timeout to await acknowledgment.

Conditions:
1. IBM terminal control type I.
2. Normal command chain sequence is as follows:
   Poll
   TIC
   Read
3. Entry is from initial housekeeping routine.

● Diagram 5-505. Start/Stop Poll Command (Part 1 of 2)

2 3 4 5 6

Diag 5-505 Part 1 3G

A

Strobe transition

GJE1

Nine bit service traps are taken to transmit the terminal address. The stop bit service trap moves the component character from the LCW buffer to the assembler/disassembler and generates a character service request

Transmit terminal address

Component character → Assembler/disassembler

B

Indicates time lapse between strobe transitions

GSRO

Set write end and poll flag in the LCW state field. Set the index character into the LCW back-up buffer. (Poll step 1)

Index character → LCW buffer

C

Strobe transition

GJE1

Nine bit service traps are taken to transmit the component character. The stop bit service trap generates a character service trap request

Transmit component character

D

Indicates time lapse between strobe transitions

GJE1

Set poll read state in the LCW state high field. Set timeout remember and timeout enable latches

Start an approximate 3-second timeout for the reception of the acknowledgment character

E

When a valid start bit is received, the strobe counter is started to develop strobe transition

GJE1

Nine bit service traps are taken to receive the acknowledgment character. Generate a character service trap request

Receive the acknowledgment character into the assembler/disassembler

F

GSRO

Recognize the Ⓓ as a positive acknowledgment character. Set status modifier (bit 1 of unit status). Set receive monitor state in the state Hi field. Set text in downshift in the state Lo field. Reset the LRC

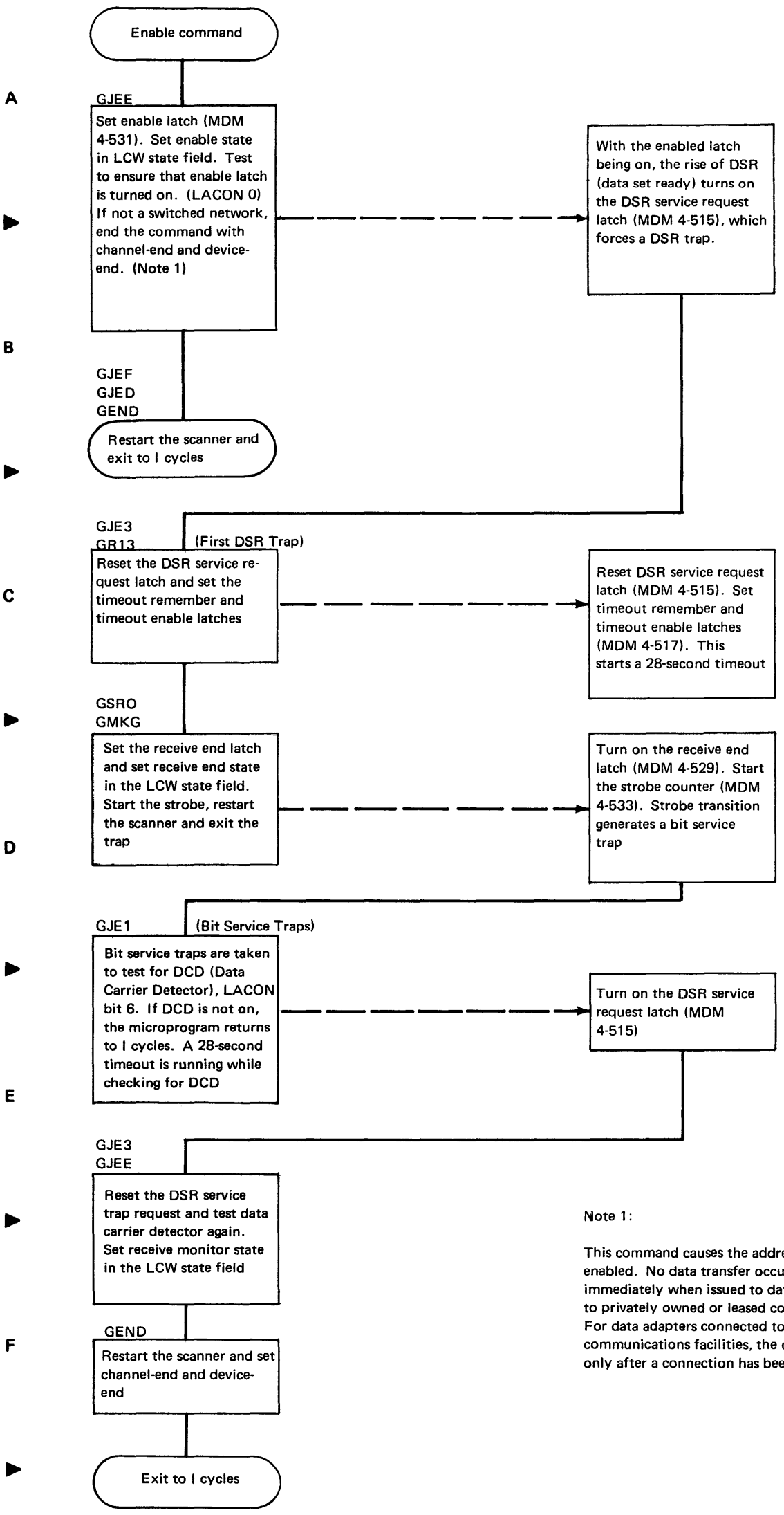
G

The poll command normally is chained to a read command to receive the data or message from the polled terminal. If chaining is not specified, the command is ended with channel-end and device-end. Set the S7 interrupt bit

H

Exit I cycles

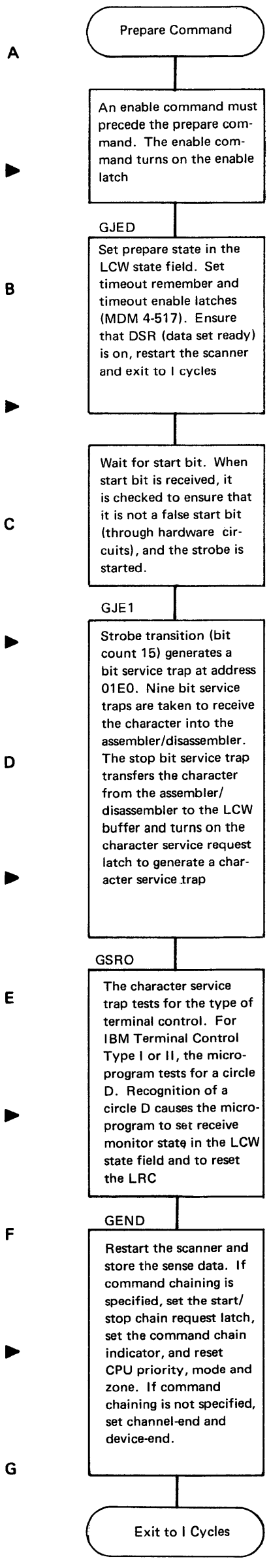
● Diagram 5-505. Start/Stop Poll Command (Part 2 of 2)



Note 1:

This command causes the addressed data adapter to be enabled. No data transfer occurs. The command ends immediately when issued to data adapters connected to privately owned or leased communications facilities. For data adapters connected to switched-network communications facilities, the command is terminated only after a connection has been established.

● Diagram 5-506. Start/Stop Enable Command

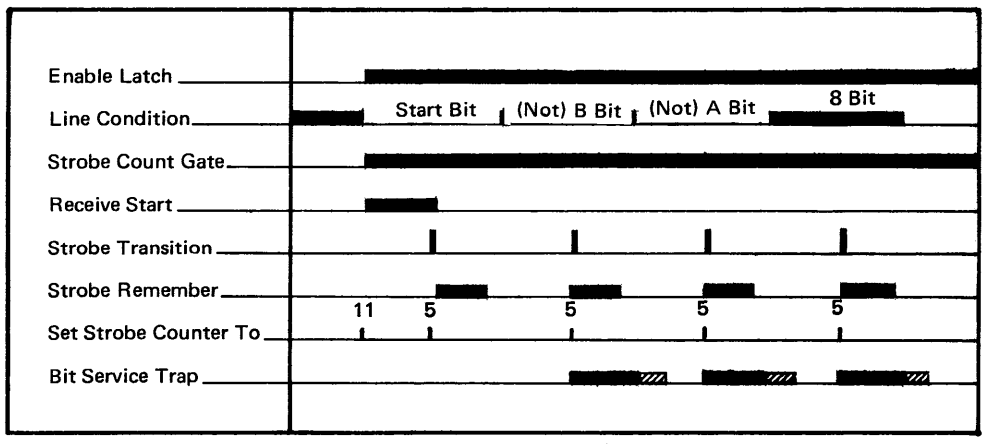


Objectives:

This read type command is used in contention type systems to permit the ICA to monitor the addressed line to signal the program that a character has been detected. An enable command must precede this read type command.

IBM Terminal Control Types I and II check for a circle D character.

The command is terminated after one character has been received. No data is transferred to storage. Channel-end and device-end are set only if command chaining is not specified.



● Diagram 5-507. Start/Stop Prepare Command

2 3 4 5 6

MICRO

Start I/O

GJEB
GJEC
GJEF

The read command is decoded by table lookup. (02 decodes as FD) The scanner is stopped and read state is set. Set the 3-second timeout

GJED

Ensure that data set ready (DSR) is on, and restart the scanner

Exit to I cycles

Objectives:
1. Hardware recognizes 2 SYN characters and develops character phase.
2. Receive control and data characters.
3. Set channel-end and device-end.

Conditions:
1. Line adapter enabled.
2. Data set ready.

ICA

Synchronous hardware controls are conditioned to receive SYN characters and data characters from the line. The line is monitored in SERDES B for the first SYN character. Set the SYN decode latch (MDM 4-555). Reset SERDES B and turn on the set B8 latch (MDM 4-553). (This turns on Sync SERDES B position 8.)

Shift in the second SYN character. Decode the second SYN character and advance the TRCR to 2. Set the character phase latch (MDM 5-451)

Serially shift in the next character. (When SERDES B bit 0 equals 1, a character has been received.) Turn on the line 'receive data transfer'. This causes a B SERDES-to-A SERDES transfer and sets the character service request latch. (MDM 4-541)

Reset TRCR (MDM 4-547)

Character Service Traps
GMKA, GMKB

The first character service trap resets the character phase latch. (Although the character phase latch is reset, the line 'character phase' remains active.)
MDM 4-541
The character service traps perform the following functions depending on the character received.

SOH or STX
Read the character from A SERDES to the P1-register. Invert the character (Chart in 5E) and decode the character as SOH or STX. Set text mode in the LCW, reset the BCC and the timeout. Store the character in main storage, restart the scanner and exit the trap.
Note: SOH or STX characters are not included in the BCC accumulation except when in text mode.

Data
Decode the character as data, invert the data and transfer to main storage. Update the BCC, reset the character service trap and set data remember. Restart the scanner and exit the trap.

SYN (Text Mode)
The SYN character is read to the P1-register and inverted. Decode the character as a SYN character and set SYN remember. The following character service trap tests for another SYN character. Restart the scanner and exit the trap.

Data (Following the SYN character in text mode)
The data is read to the P1-register and inverted. The data is tested to ensure that it is not a SYN character. Reset and set the 3-second timeout, update the BCC and store the data in main storage. Restart the scanner and exit trap.

ETX
Read the ETX character to the P1-register and invert. Decode the character as ETX, update the BCC, reset text mode and store the character in main storage. Restart the scanner and exit trap.

First BCC (1st check)
Read the character to the P1-register and invert. Compare BCC1, restart the scanner and exit trap.

Second BCC (2nd Check)
Read the character to the P1-register and invert. Compare BCC2. Reset character phase and timeouts and set receive monitor state. Set channel-end and device-end, set interrupt request latch, restart the scanner and exit trap.

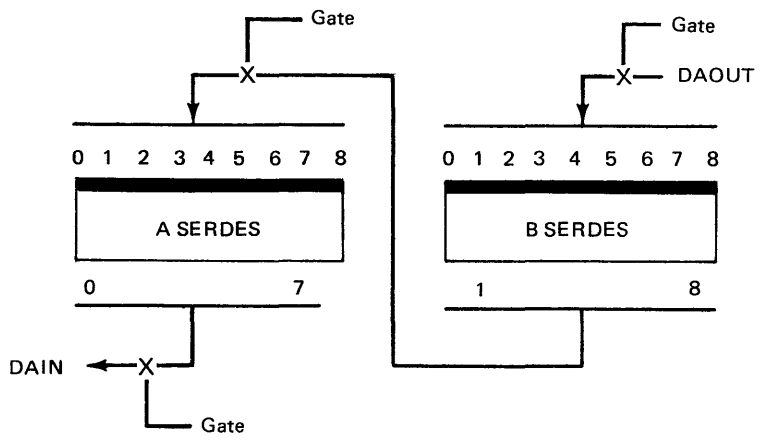
Character transfer from main storage to the line and from the line to main storage.
Character G Hex configuration 1100 0111 (C7)

Storage	1100 0111	C 7
↓		
DAOUT	1100 0111	C 7
↓		
B SERDES	1100 0111	E 3
↓		
A SERDES	1110 0011	E 3
↓		
Data Set	1110 0011	E 3
↓		
Line	1110 0011	E 3
↓		
Data Set	1110 0011	E 3
↓		
B SERDES	1110 0011	E 3
↓		
A SERDES	1110 0011	E 3
↓		
DAIN	*0011 1000	3 8
↓		
Micro	1100 0111	C 7
↓		
Storage	1100 0111	C 7

{ DAOUT 0-7 to DAIN 7-0

*The inversion process is executed by the use of the external DAIN and one microword statement. The original systems used inverters.

{ A SERDES 0-7 to DAIN 7-0



● Diagram 5-508. Synchronous Receive Operation

2 3 4 5 6

Micro

Start I/O

GJEB, GJEC, GJEF

Translate the command as a synchronous write command. Set transmit mode and 3-second time-out

GJED

Start the scanner and exit to I cycles

ICA Hardware

Set the transmit status latch (MDM 4-539).
Set the 3-second timeout latch (MDM 4-539).
Advance the TRCR 0-1 (MDM 4-547)
1. Turn on request to send (RTS).
2. Wait for clear to send (CTS).
Advance TRCR 1-2.
Advance TRCR 2-3
1. Gate the SYN character and the tag to A SERDES.
2. Set the SYN character count to SERDES B.
Serialize SYN to line. (Send 7 SYN characters for internal clock or 3 SYN characters for external clock.) When the last SYN is in A Serdes, the TRCR is advanced to 04. This sets the character service request latch that causes a character service trap

Character Service Trap

Character service traps fetch the character from main storage, decode the character, and place it in DAOUT. In addition, the following functions occur as determined by the character and LCW 4 (State high and state low fields).
SOH (Start of header)
1. Set the 1- and 3-second timeout.
2. Reset the BCC (Block check character).
The first SOH or STX character service trap resets the BCC and is not included in the BCC.
Data
1. Update the BCC.
After the 1-second timeout is complete, the microprogram generates two SYN characters to maintain character phase. The 1- and 3-second timeouts are reset and set.
ETX (End of text)
1. Decode the character as end of text.
2. Update the BCC.
Following the ETX character, character service traps are taken to send two BCC characters and the PAD character. Reset the transmit latch and the timeout latches. (This occurs in the character service trap following the PAD character.)

Advance the TRCR to 05. (SERDES A empty)
Set transmit end.
1. Reset RTS
2. Reset TRCR to 00.
3. Turn on character service request latch that causes a character service trap

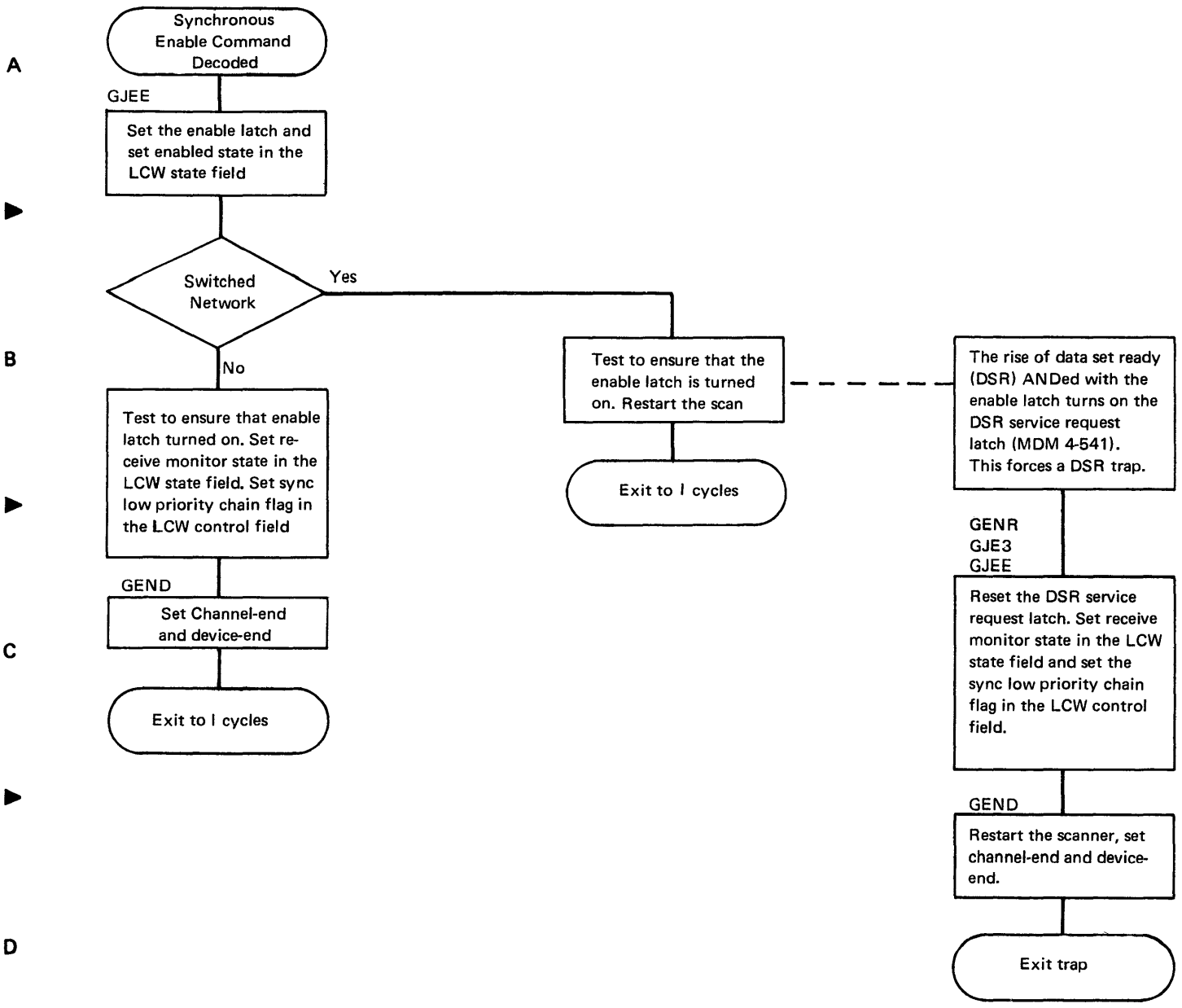
Set receive monitor state and restart the scanner. Set channel-end and device-end and set the interrupt request latch. (Reset S7)

Objectives:
1. Translate the command for synchronous write.
2. Condition the hardware controls.
3. Set channel-end and device-end.

Conditions:
1. Data set ready and enabled.
2. EBCDIC code.

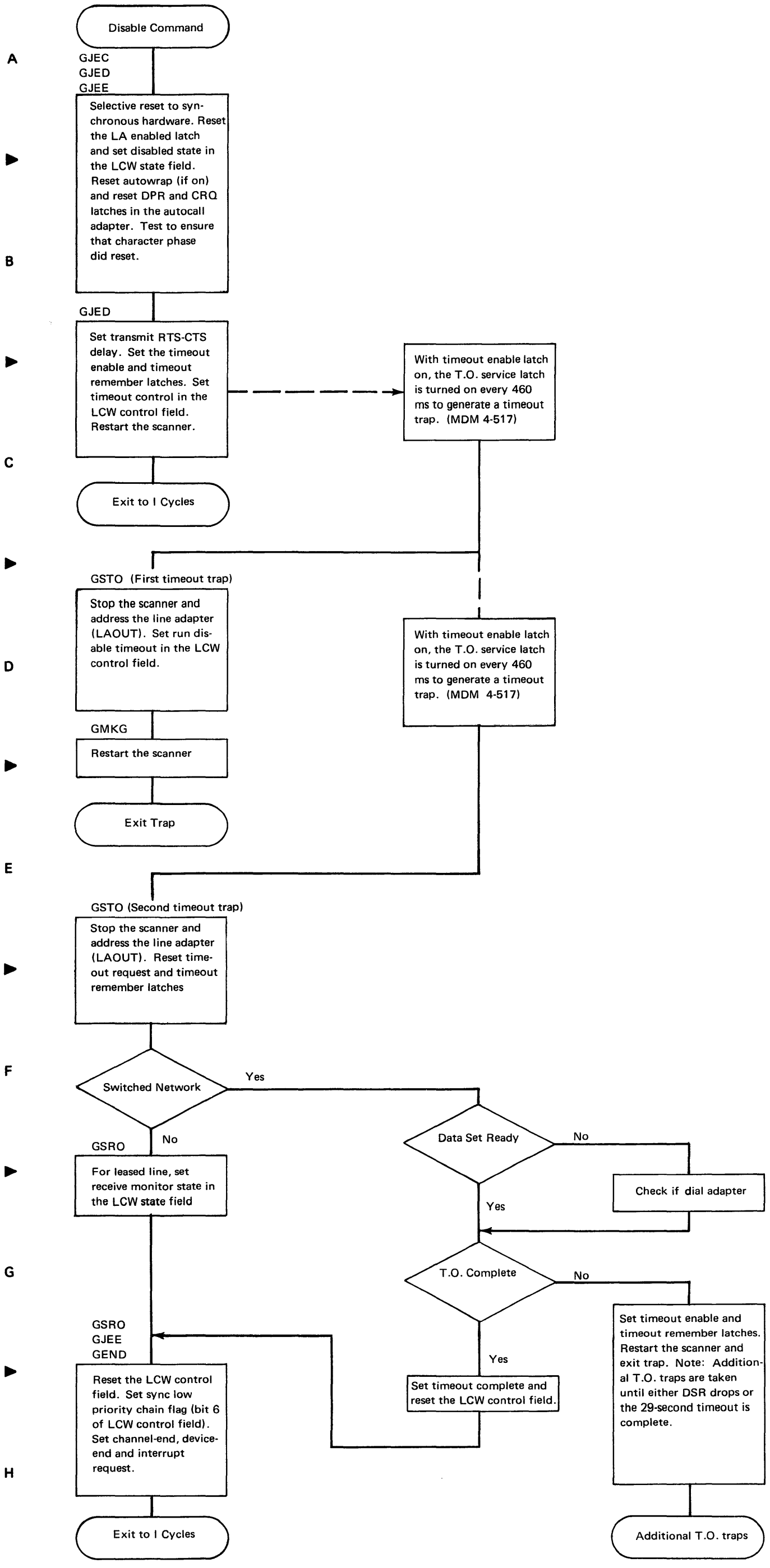
● Diagram 5-509. Synchronous Write Operation

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6



The enable command causes the addressed data adapter to be enabled.
No data transfer occurs.
The command is terminated immediately if issued to a private or leased line.
If issued to a switched line, the command is not terminated until the rise of DSR is detected.

● Diagram 5-510. Synchronous Enable Command



● Diagram 5-511. Synchronous Disable Command

2 3 4 5 6

A Polling of synchronous terminals is done under a Start I/O that refers to the following channel command word sequence.
Poll
Tic
Read

Start I/O

DCLA

B The command is decoded and the appropriate operations are performed depending on the command and the status of the active bit

GJEB
GJEB
GJEF

C Translate the command (09 to 88), stop the scanner, set poll transmit state and transmit mode. Set the 3-second timeout

The ICA hardware sends the SYN characters, advances the TRCR to 4 and sets the character service request latch. (For detail of ICA hardware operation, refer to Diagram 5-509 Synchronous Write operation.)

GJED

Restart the scanner and exit trap

Character Service Trap (EOT)

D Reset and set the 1- and 3-second timeouts. Fetch the EOT character from storage and transfer it to DAOUT. Decode the EOT. Set EOT decoded and UE remember. Restart the scanner and exit trap

Character Service Trap (SYN)

E Fetch the SYN character from storage and transfer it to DAOUT. Decode the SYN character. (32 to DB) Update the LCW state Hi and state Lo fields. Restart the scanner and exit trap.

Note: A character service trap is taken for each SYN character

Character Service Trap
(First character of poll address)

F Fetch the character from storage and transfer to DAOUT. Decode the character as data and set data remember in LCW 4. Restart the scanner and exit the trap.

Note: The address field may be from 1 to 7 characters

G Character Service Trap (ENQ)

Fetch ENQ from storage and transfer it to DAOUT. Decode the ENQ character. (2D to AF) Update LCW 4, restart the scanner and exit trap

H (1)

Character Sequence

S	S	S	E	F	S	S	S	A	X	X	X	X	X	X	E	P
Y	Y	Y	O	F	Y	Y	Y	D							N	A
N	N	N	T		N	N	N	D							Q	D

(1)

Character Service Trap
(Index character and PAD)

Fetch index character from storage and place it in LCW 6. Develop a PAD character (FF) and transfer it to DAOUT. Update the state Hi field (LCW 4), restart the scanner and exit trap.

Character Service Trap
(Following the PAD character)

Reset the 1- and 3-second timeouts and transmit status. Restart the scanner and exit trap

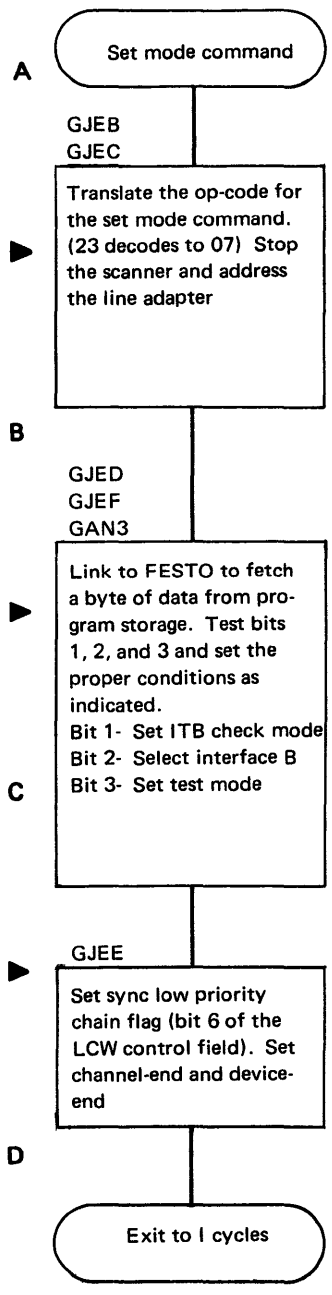
Transmit status being reset causes the TRCR to advance to 05 (MDM 4-547). The advance of the TRCR to 05 develops 'transmit end' that resets the 'request to send' latch and resets the TRCR to 00. Transmit end turns on the character service request latch (MDM 4-541)

Character Service Trap
(Turnaround)

Reset the poll flag. Set poll receive in LCW 4, set the 3-second poll read timeout, start the scanner and exit trap.

Note: The poll command is not ended until character phase is detected or the 3-second timeout is completed

● Diagram 5-512. Synchronous Poll Write Command



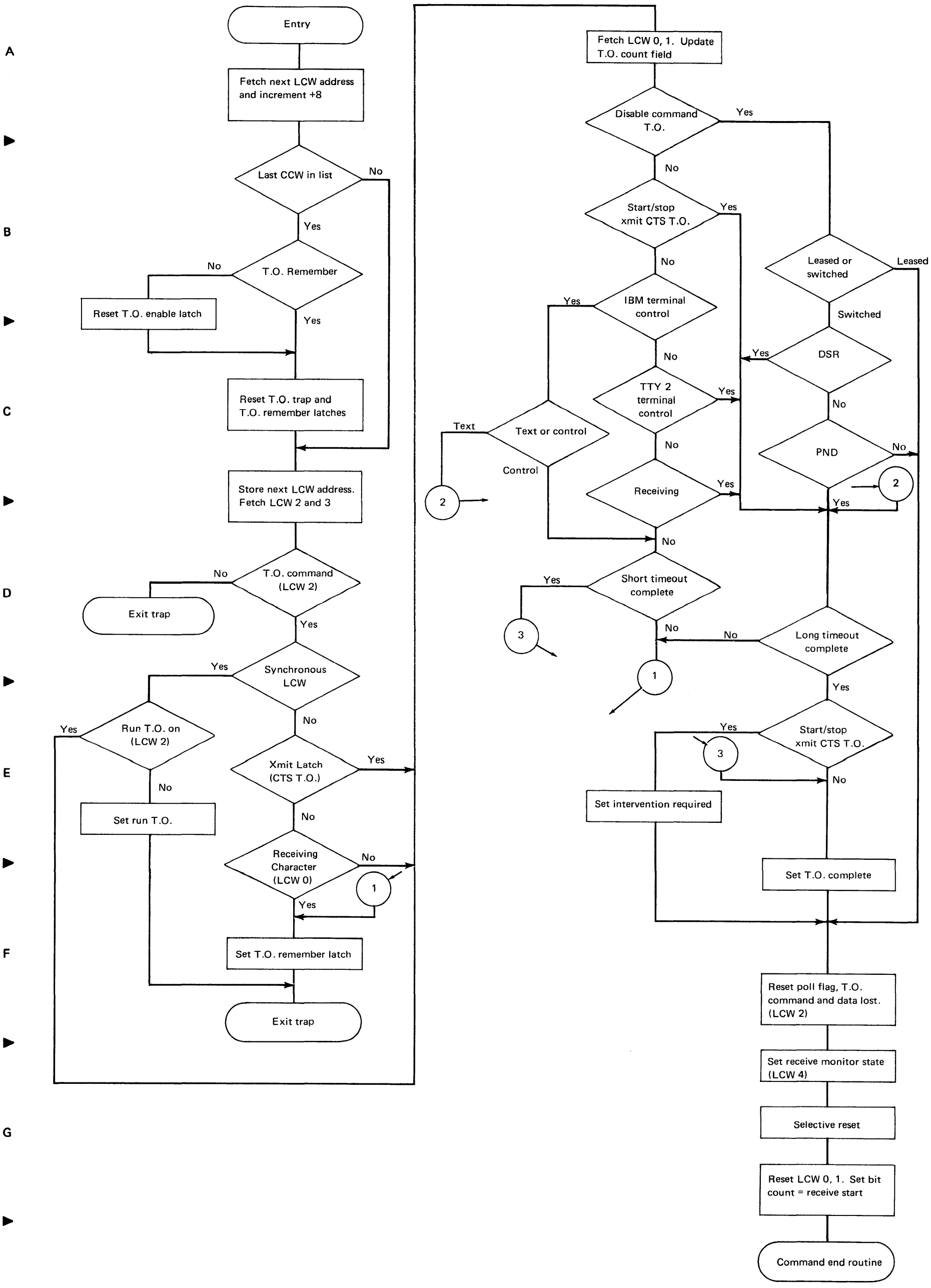
This command is a control command that causes a single byte of data to be fetched from program storage.
Bits 1, 2, and 3 are used to set the following conditions.
Bit 1 -Places the adapter in ITB mode.
Bit 2--Selects interface B. (Interface B can only set on the first adapter with dual communications interface feature.)
Bit 3 -Places the adapter in test mode.

Bits 1 and 2 are reset by system reset.
Bit 3 is reset by issuing a disable command.

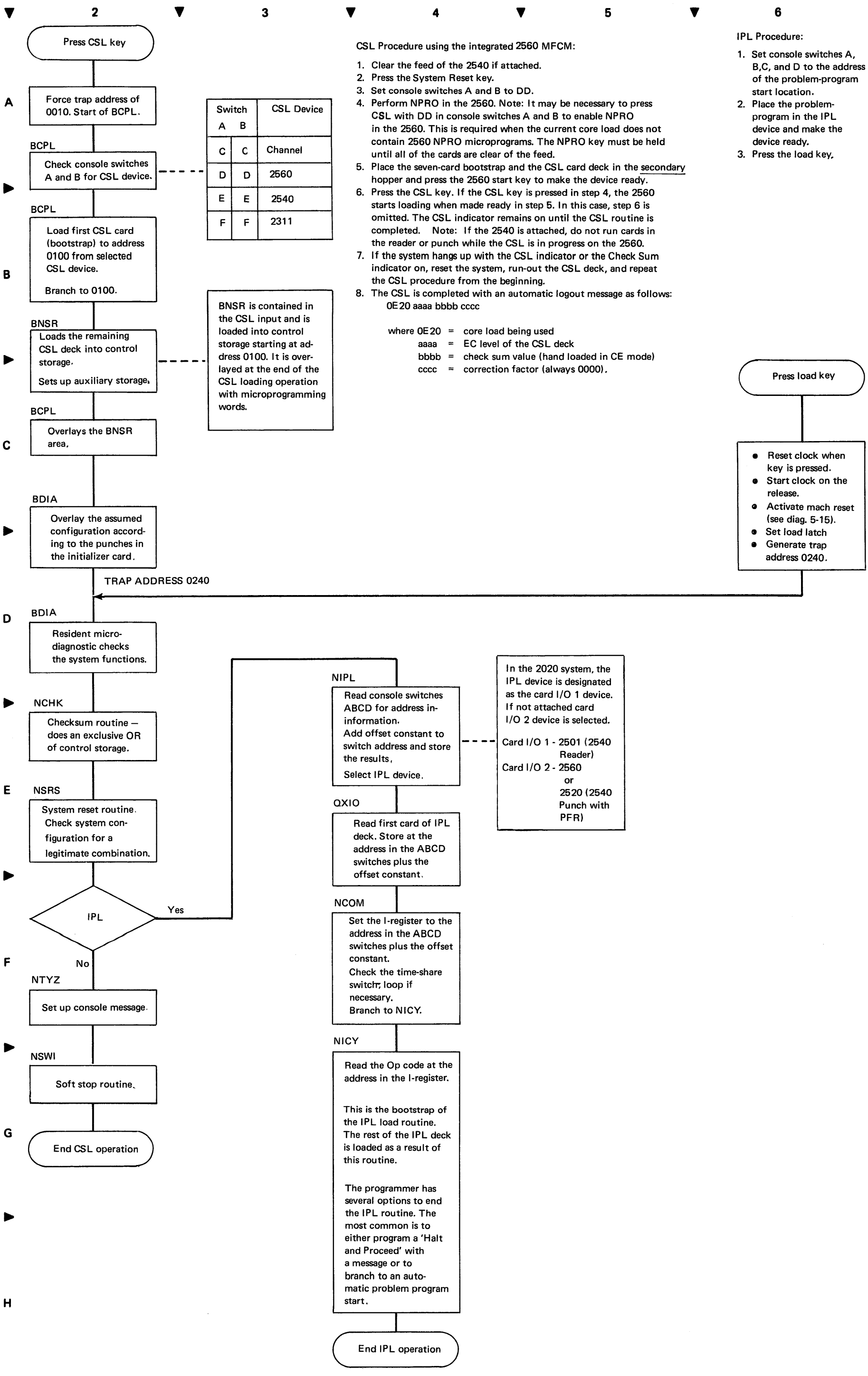
The existing mode setting can be changed by issuing another set mode command.

Program note: To change interface designation, a disable command must precede the set mode command.

● Diagram 5-513. Synchronous Set Mode Command



● Diagram 5-514. Timeout Update Trap Routine



● Diagram 5-600. CSL/IPL Operational Diagram

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

ERROR MESSAGE HANDLING

After the microprogram recognizes an error, in this case the invalid operation code 9C, the routines are used to form the error message and to print it out on the 1052 Printer/Keyboard.

The objectives of this routine are:

A
1. Recognize the invalid operation code 9C (NICY).
2. Store the address of the invalid instruction (0244) in the I-Recall area of Auxiliary Storage and to setup the error identification code (NERR).
3. Set the 'Soft Stop' latch and build the error message in the console message area of the Auxiliary Storage (NTYZ).
4. Print the error message (NTYZ).
5. Return to the Soft Stop routine and wait for operator intervention.

Conditions

▶ 1. No other I/O device working.
2. The PRKB is ready.
3. No other errors detected.

Error Message Format:

xx aaaa nn

xx = operation code

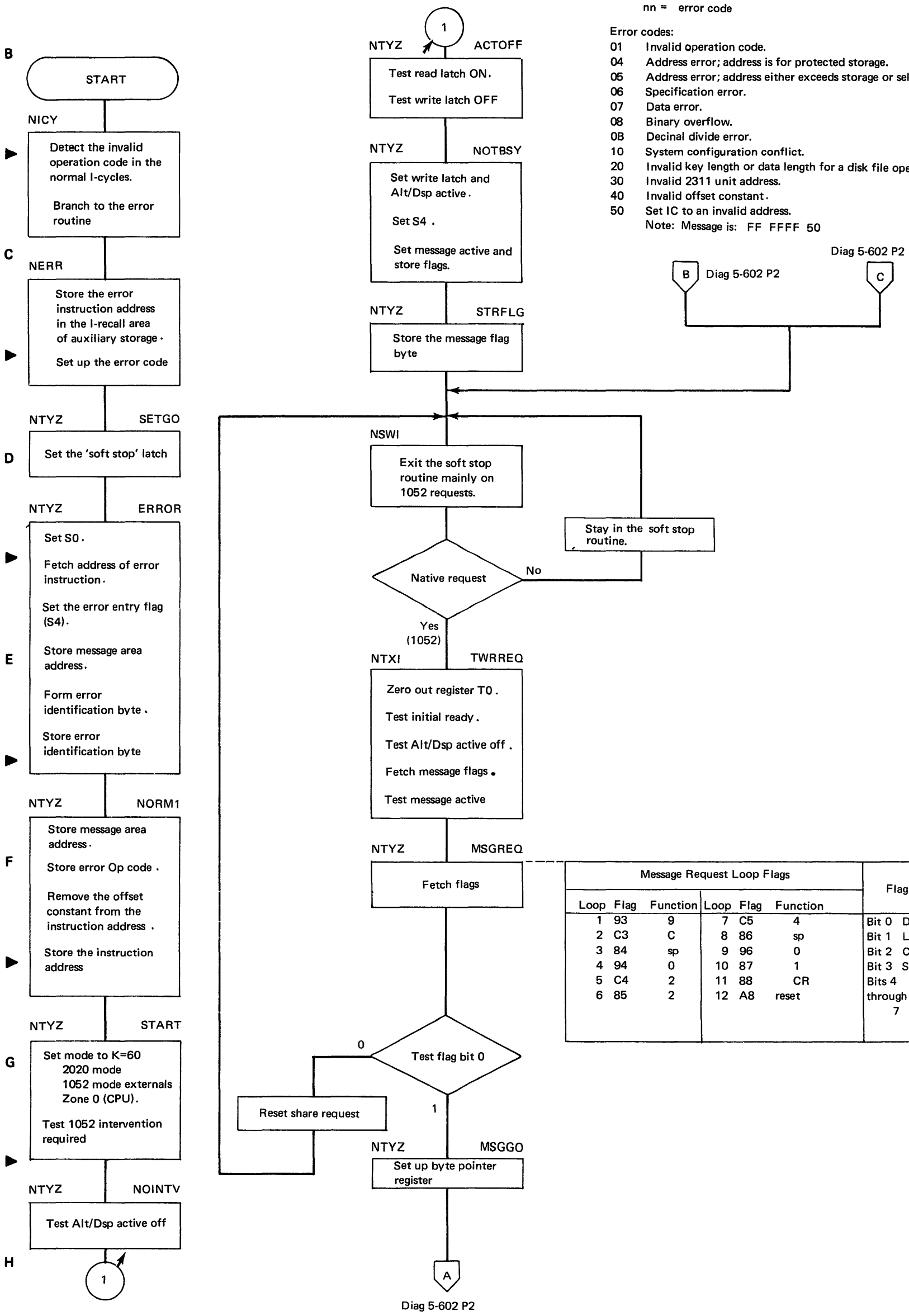
aaaa = instruction address

nn = error code

Error codes:

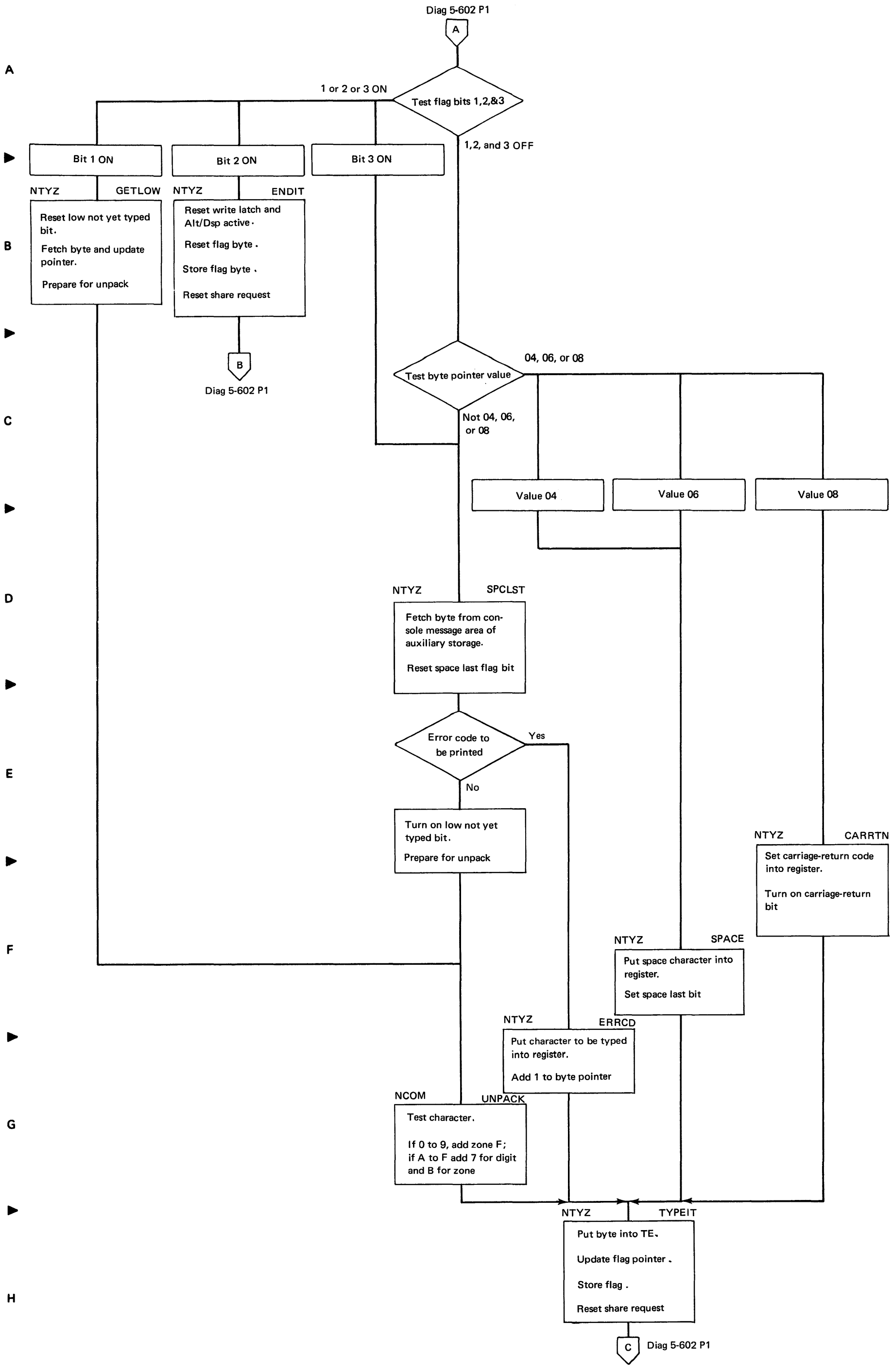
01	Invalid operation code.
04	Address error; address is for protected storage.
05	Address error; address either exceeds storage or selects an invalid register.
06	Specification error.
07	Data error.
08	Binary overflow.
0B	Decinal divide error.
10	System configuration conflict.
20	Invalid key length or data length for a disk file operation.
30	Invalid 2311 unit address.
40	Invalid offset constant.
50	Set IC to an invalid address.

Note: Message is: FF FFFF 50



Message Request Loop Flags						Flag Bit Significance
Loop	Flag	Function	Loop	Flag	Function	
1	93	9	7	C5	4	Bit 0 Display active.
2	C3	C	8	86	sp	Bit 1 Low not yet typed.
3	84	sp	9	96	0	Bit 2 Carriage return (CR).
4	94	0	10	87	1	Bit 3 Space last.
5	C4	2	11	88	CR	Bits 4 through 7 Error byte pointer.
6	85	2	12	A8	reset	

● Diagram 5-602. Error Message Procedure (Part 1 of 2)



● Diagram 5-602. Error Message Procedure (Part 2 of 2)

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

SYSTEM/360 MODEL 20 ERROR SUMMARY

The following errors are recognized by the System/360 Model 20 system and cause a program stop in that system. In the System/360 Model 20 Mode feature, the microprogram analyzes the problem program and data for the same type of errors.

If an error is found, an error message is typed on the printer/keyboard and the microprogram waits in the soft stop loop for operator handling. The error message includes the error codes shown here to identify the type of error. See MDM 5-602 for additional information.

A

I. Programming Error Stop Conditions

01 Error Code — Invalid Operating Code

04 Error Code — Addressing Error

1. An instruction address or an operand address refers to the protected first 144 bytes of main storage.

▶

05 Error Code — Addressing Error

1. An instruction address or an operand address is outside of available storage.
2. The R1 or R2 fields of an RR or an RX format binary instruction contain binary values 0 through 7, the R1 field in a branch and store instruction contains binary values 0 through 7, or the R2 field of an RR format branch instruction contains binary values 1 through 7.
3. An instruction byte is located at the last available storage position.

B

06 Error Code — Specification Error

1. An instruction address is not located on a half-word boundary of main storage.
2. A binary operand is not located on a specified boundary of main storage.
3. For decimal add, decimal subtract, zero and add, and decimal compare instructions, the length code L2 is greater than the length code L1.
4. For decimal multiply and decimal divide instructions, the length code L2 is greater than 7 or greater than or equal to the length code L1.
5. Bits 12 through 15 of an RX format instruction are not all zero.

▶

6. A 2560 write card instruction is encountered in the program and there is no card in the punch or print station, or no print head has been selected.
7. The field length specified in an input/output instruction is zero or is greater than the maximum allowable number for the I/O device addressed.

07 Error Code — Data Error

1. A sign or digit code of an operand in the decimal instructions zero and add, add, subtract, compare, multiply, or divide is incorrect or the operand fields in these operations overlap incorrectly.
2. The multiplicand field (first operand) in a decimal multiply instruction has insufficient high-order zeros.

C

3. An invalid digit code is contained within the second operand field of an edit operation.

08 Error Code — Binary Overflow Check

0B Error Code — Decimal Divide Check

1. The resultant quotient in a divide decimal instruction exceeds the specified data field instruction (including division by zero) or the dividend has no leading zero.

▶

II. Process Error Stop Condition

(No Error Code) — Parity Error

Each system handles parity as an internal processing error. No error message or error code is assigned.

III. I/O Error Conditions (CPU)

D

01 Error Code — Invalid Operation Code

04 Error Code — Addressing Error

NOTE: An input/output instruction containing an I/O device address that specifies a device not attached to the system is treated as a no-operation.

1. An instruction address or the address of an input/output data field refers to the protected first 144 bytes of main storage.

05 Error Code — Addressing Error

1. An instruction address, the address of an input/output data field, or a branch address is outside available storage.
2. An instruction part is located in the last two main-storage positions.

▶

06 Error Code — Specification Error

1. An instruction address is not located on a half-word boundary of main storage.
2. A 2560 write card instruction is encountered in the program, and there is no card in the punch or print station, or no print head has been selected.
3. The field length specified in an input/output instruction is zero or is greater than the maximum allowable number for the I/O device addressed.

E

IV. I/O Error Conditions (I/O)

Error conditions that may occur in I/O devices are included in the IBM Systems Reference Library publication for the respective device.

▶

F

▶

G

▶

H

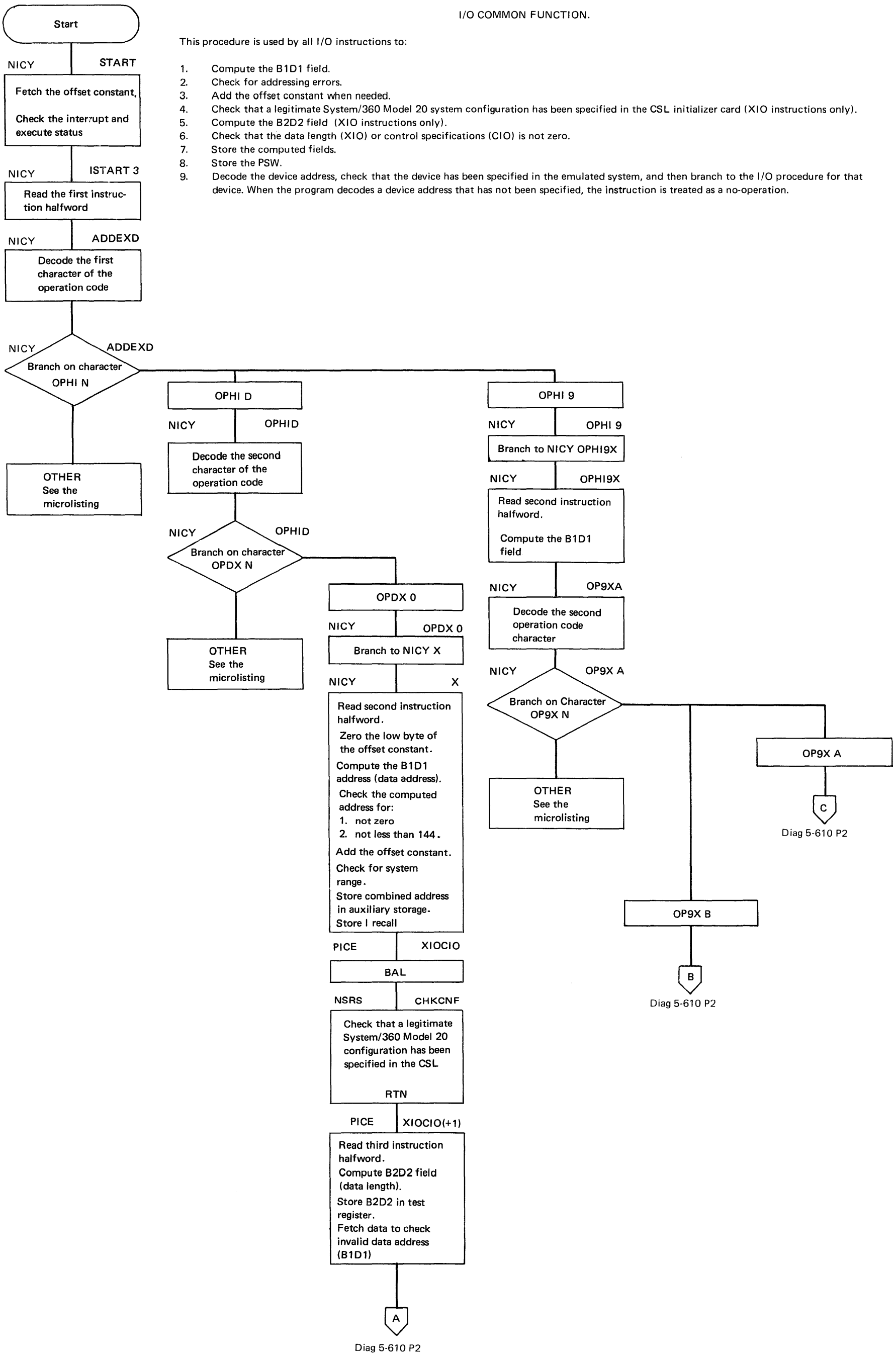
● Diagram 5-604. Summary of System/360 Model 20 Error Codes

2 3 4 5 6

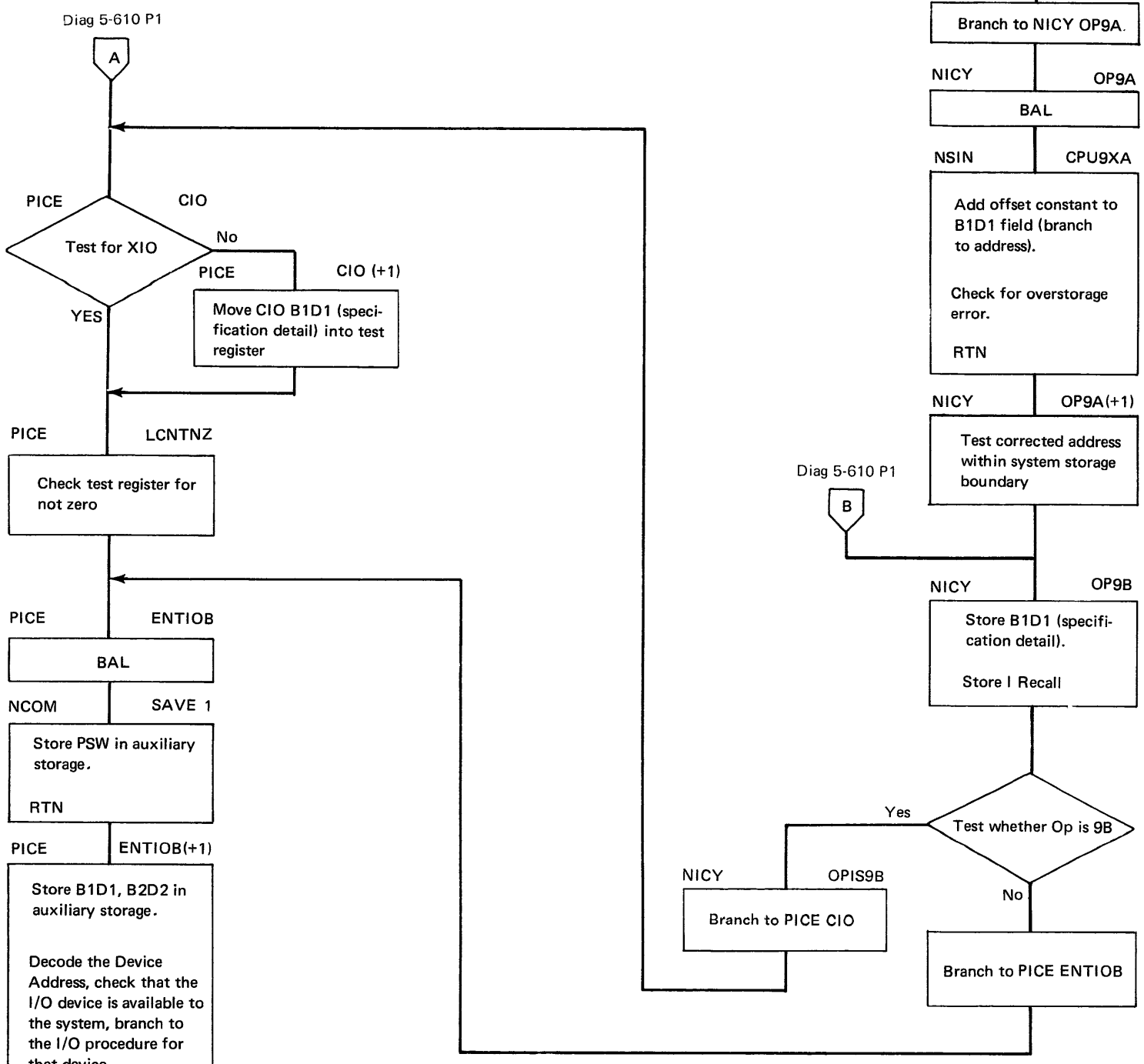
I/O COMMON FUNCTION.

This procedure is used by all I/O instructions to:

1. Compute the B1D1 field.
2. Check for addressing errors.
3. Add the offset constant when needed.
4. Check that a legitimate System/360 Model 20 system configuration has been specified in the CSL initializer card (XIO instructions only).
5. Compute the B2D2 field (XIO instructions only).
6. Check that the data length (XIO) or control specifications (CIO) is not zero.
7. Store the computed fields.
8. Store the PSW.
9. Decode the device address, check that the device has been specified in the emulated system, and then branch to the I/O procedure for that device. When the program decodes a device address that has not been specified, the instruction is treated as a no-operation.



● Diagram 5-610. I/O Common Routine (Part 1 of 2)



Device Address	I/O Procedure	MDM Diagram
0	No Op	
1 (2501)	QXIO RD2540	5-612 Read a Card (XIO) 5-618 Test Reader Busy (TIOB)
2 (2520)	QAAD RP2520	
(2560)	PCIO MF2560	
3 (1442)	QPXI SRTXIO	5-614 Punch a Card (XIO)
4 (2203)	PRTB START	5-616 Print a Line (XIO)
(1403)	PRTB START	5-620 Delayed Skip to 1 (CIO)
5	No Op	
6	No Op	
7 (IOC)	RTAA IOCHNL	5-640 Channel Operation
8 (2311)	RFIL FILE20	5-631 Write Count and Data (Write Format) 5-632 Read Data Operation
9	No Op	
A	No Op	
B	No Op	
C	No Op	
D	No Op	
E (2152)	NTOP START	
F	No Op	

● Diagram 5-610. I/O Common Routine (Part 2 of 2)

READ A CARD

Instruction: D0 1 2 B1D1 B2D2

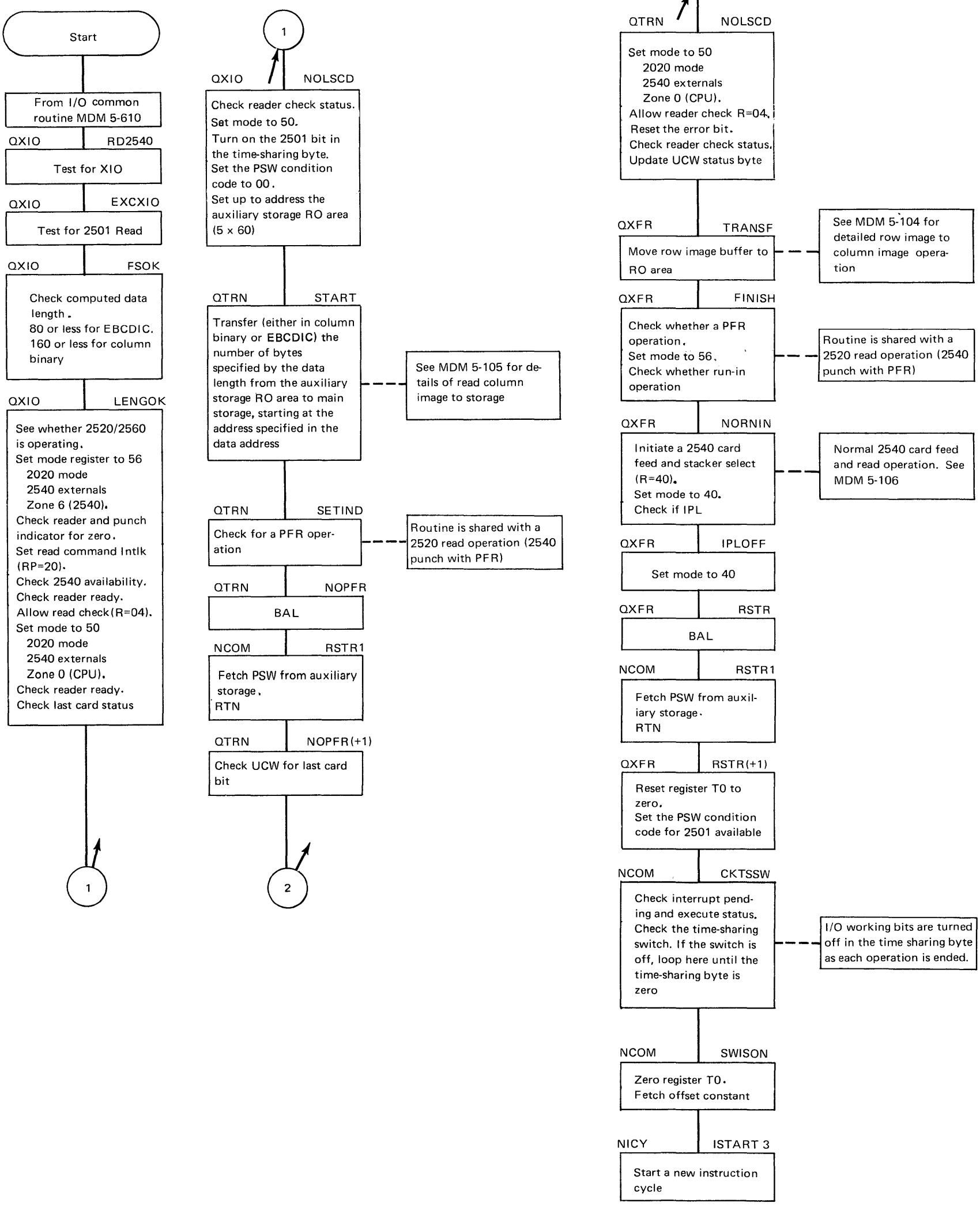
D0: XIO instruction (data transfer).
1: Device address (2501).
2: Function specification (read a card).
B1D1: Data address.
B2D2: Data length.

Conditions:

1. No other I/O device is working.
2. No errors on read-in.
3. Not the last card.

Objectives:

1. To emulate the 2501 serial read operation on the 2540:
   A. Read a card (read and feed with an automatic selection of stacker R1 on the 2540).
   B. Transfer to the program storage the number of bytes (card columns) specified by the B2D2 field.
   C. Start with the address specified by the B1D1 field.
2. To recognize the 2501 error conditions.



● Diagram 5-612. 2501/2540 Read a Card (XIO)

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

PUNCH A CARD

Instruction: D0 3 6 B1D1 B2D2

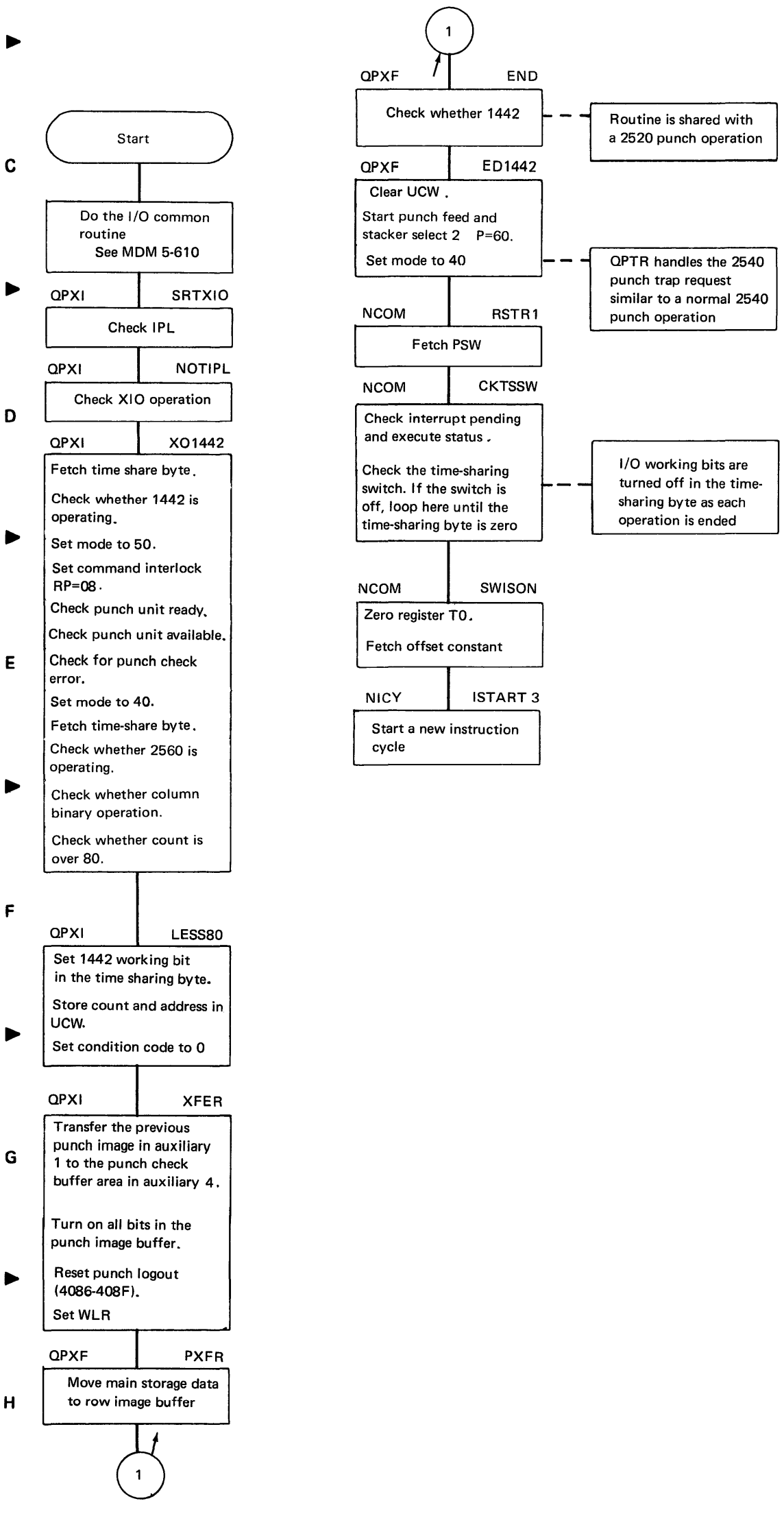
- D0 : XIO instruction (data transfer)
- 3 : Device address (1442)
- 6 : Function specification (punch and feed)
- B1D1: Data address
- B2D2: Data length

Conditions:

1. Not IPL.
2. No other I/O device is operating.
3. Not column binary.
4. No I/O errors.

Objectives:

1. Emulate a 1442 serial punch and feed operation on the 2540.
2. Stacker select P2 for non-error cards, and P1 for error cards.



● Diagram 5-614. 1442/2540 Punch a Card (XIO)

2 3 4 5 6

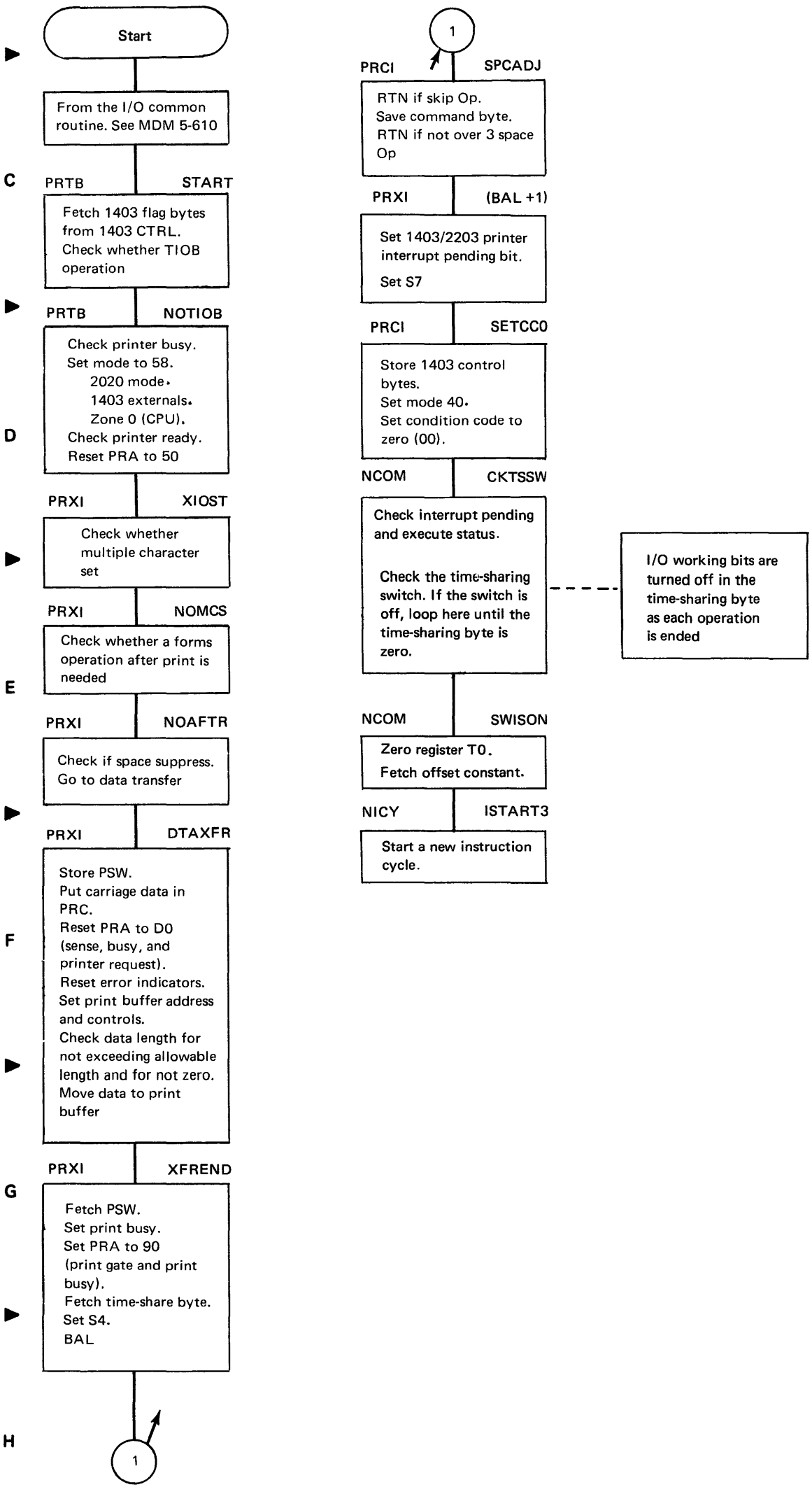
PRINT A LINE

Instruction: D0 4 0 B1D1 B2D2

- D0 : XIO instruction (data transfer).
- 4 : Device address (either 1403 or 2203).
- 0 : Function specification (print and space).
- B1D1: Data address.
- B2D2: Data length.

Conditions:

1. No other I/O device is operating.
2. No I/O errors have occurred.
3. Single space.
4. No carriage operation (skipping).



● Diagram 5-616. 1403/1403 Print a Line (XIO)

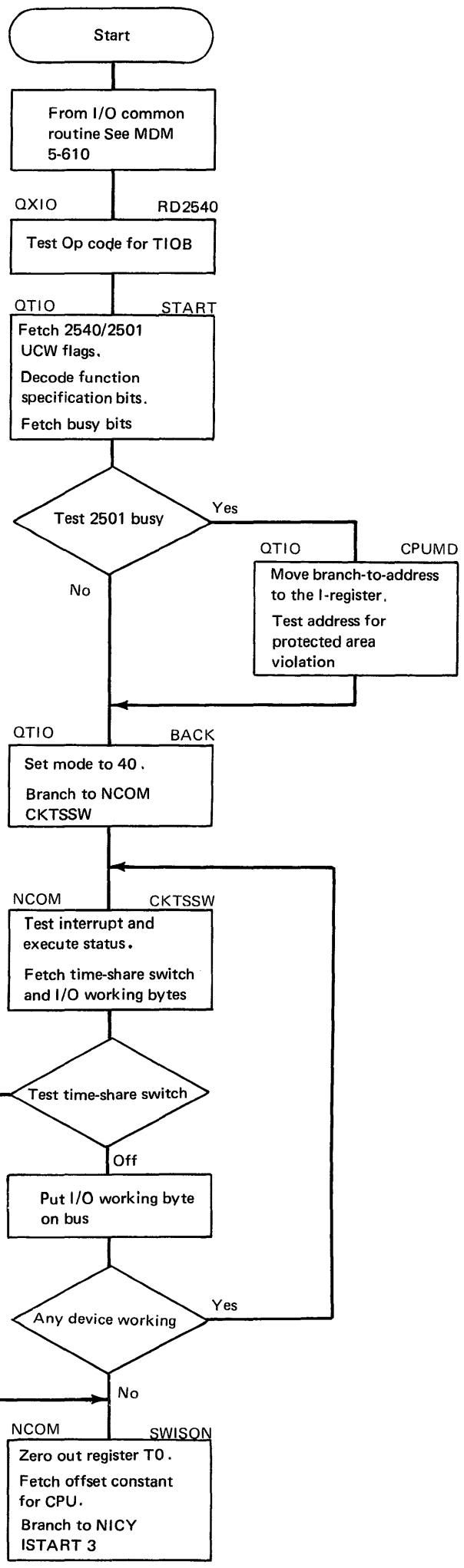
TEST I/O AND BRANCH

Instruction: (020E) 9A 1 0 020E

A
(020E): Instruction address.
9A : Operation code (TIOB).
1 : Device address (2501).
0 : Function specification (test reader busy).
020E : Branch to address.

Objectives:

1. Decode Op code (9A) as a TIOB instruction
2. Fetch busy bits from auxiliary storage.
3. If 2501 busy bit is ON:
   a. Move branch address to I-register.
   b. Test branch to address for non-protected area.
   c. Test-time sharing switch.
   d. Branch to NICY ISTART 3.
4. If 2501 busy bit is OFF:
   a. Test time-sharing switch.
   b. Branch to NICY ISTART 3.
   (I-reg contains the address of the next sequential instruction)



● Diagram 5-618. 2501/2540 Test Reader Busy (TIOB)

2 3 4 5 6

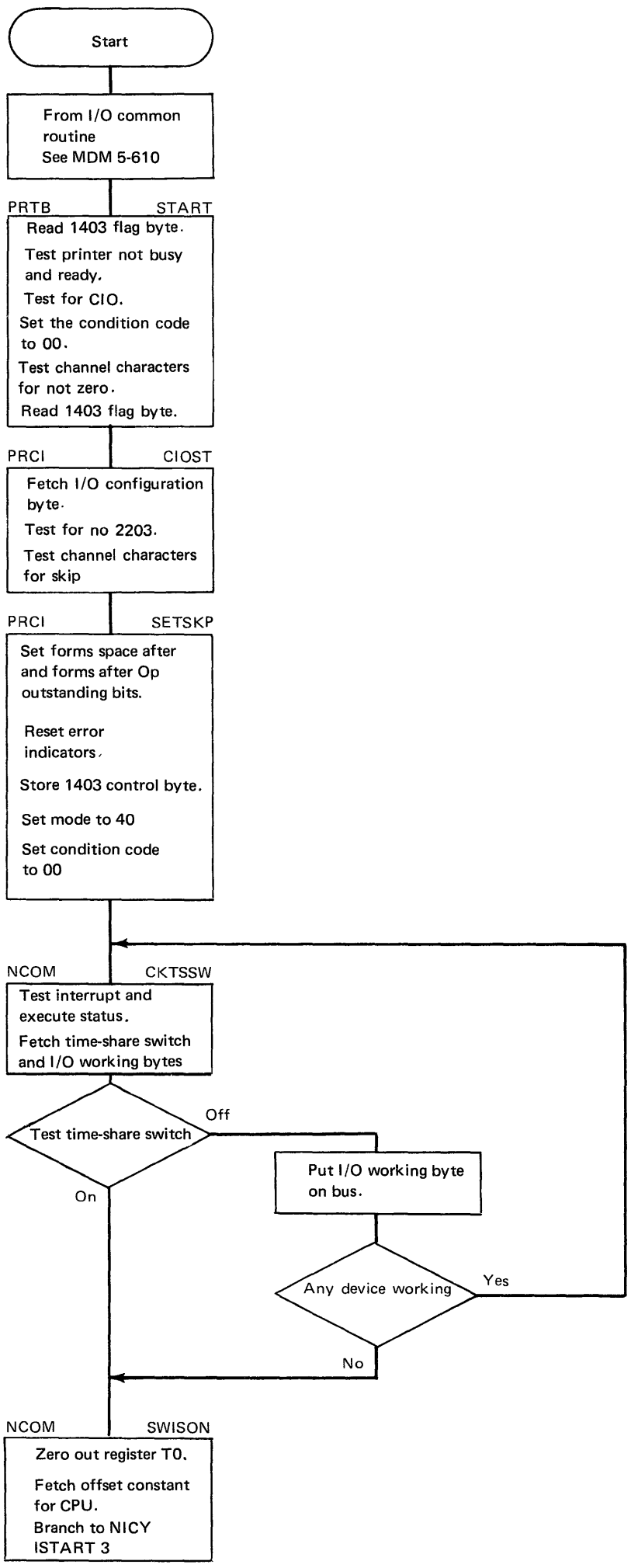
CONTROL I/O

Instruction: 9B 4 7 0001

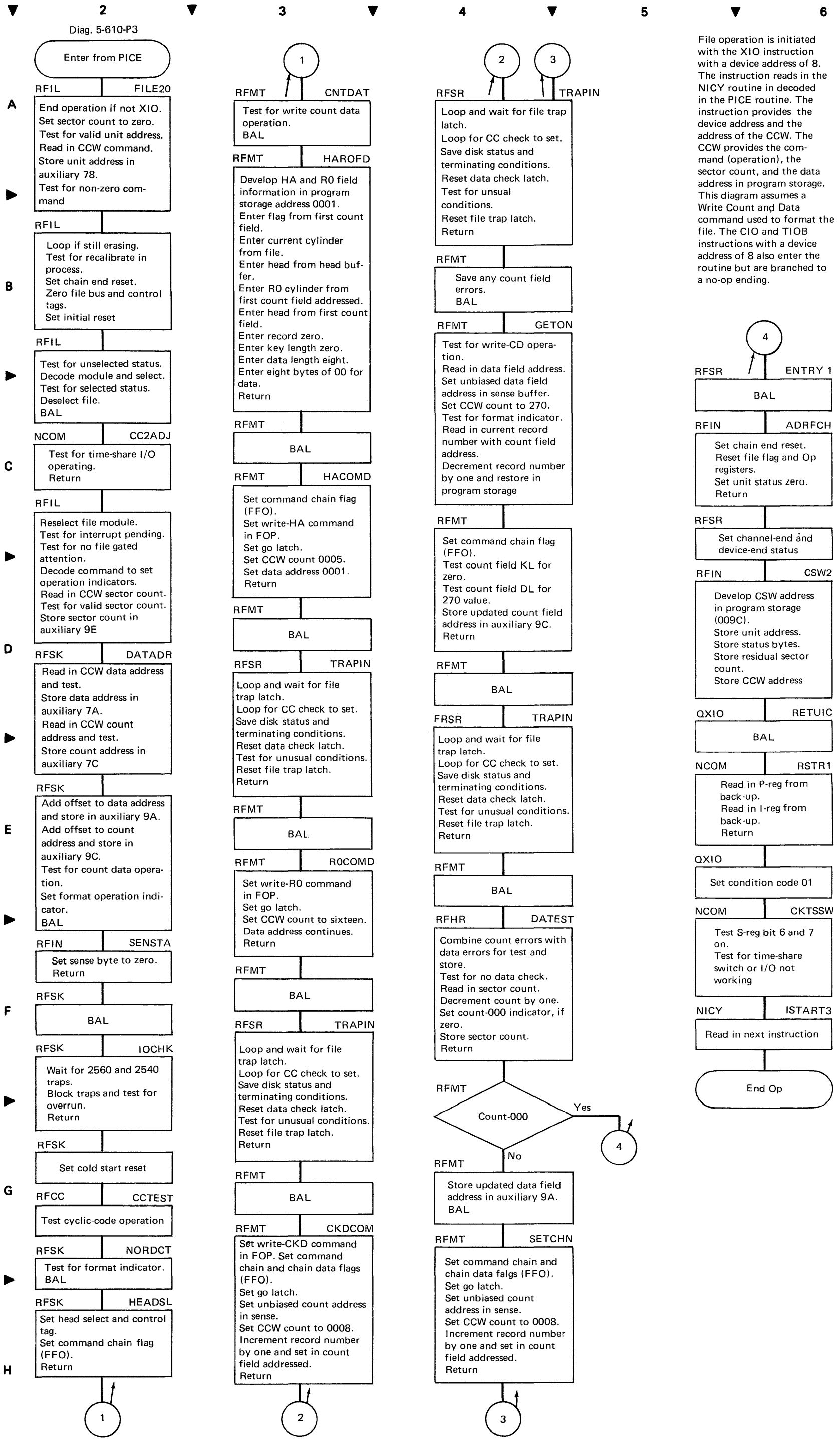
9B : Operation code (CIO).
4 : Device address (printer 2203 or 1403).
7 : Function specification (delayed skip).
0001 : Detailed functional specification (carriage tape channel 1).

Objectives:

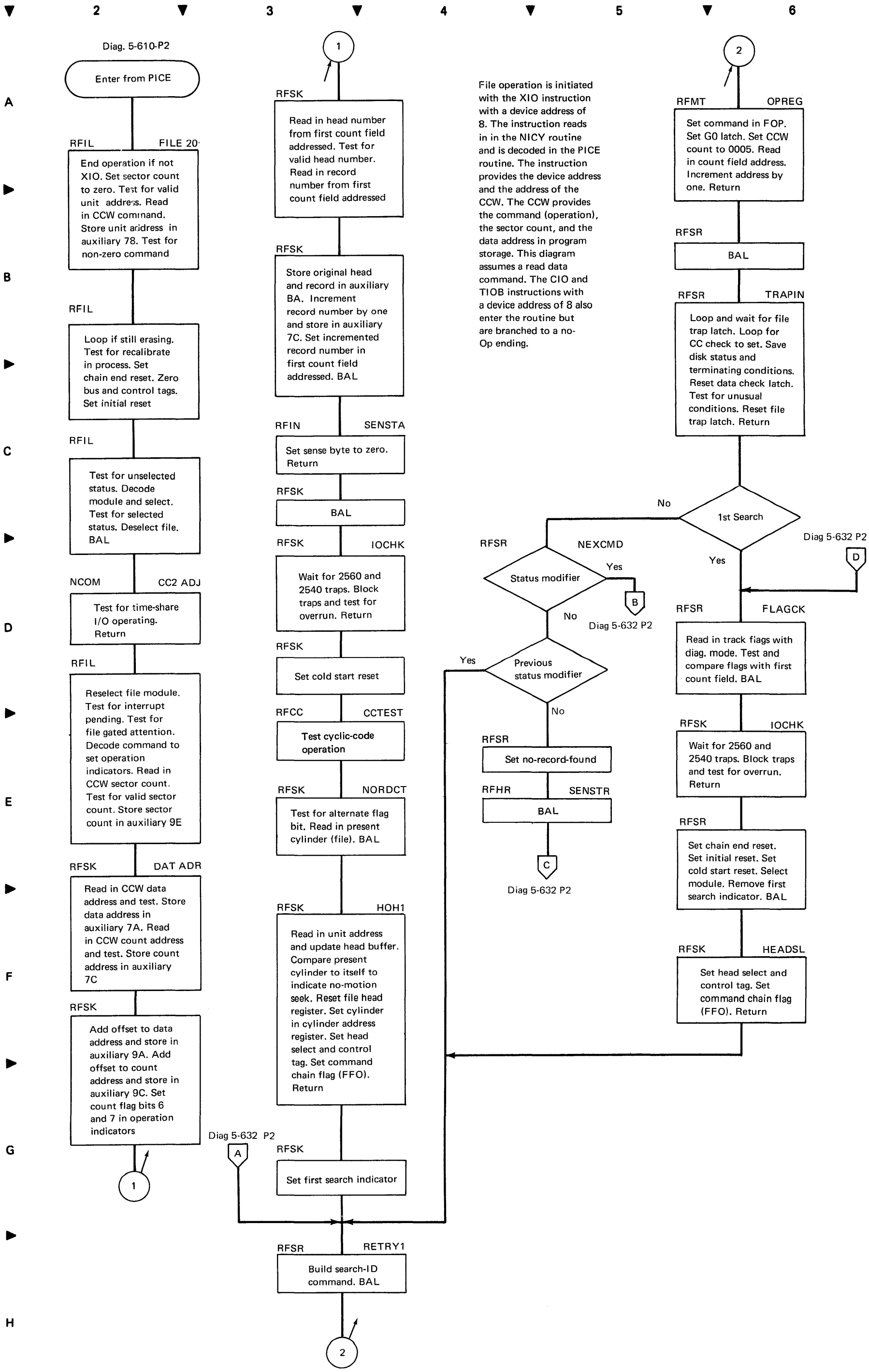
1. Read 1403 flag byte from 1403 UCW.
2. Test for printer ready and not busy.
3. Test for CIO operation.
4. Zero out condition code.
5. Test function specified.
6. Test I/O configuration.
7. Store condition in 1403 UCW flag byte.
8. Test time-share switch.
9. Branch to NICY ISTART 3.
10. Skip will be stored until after the next print operation.



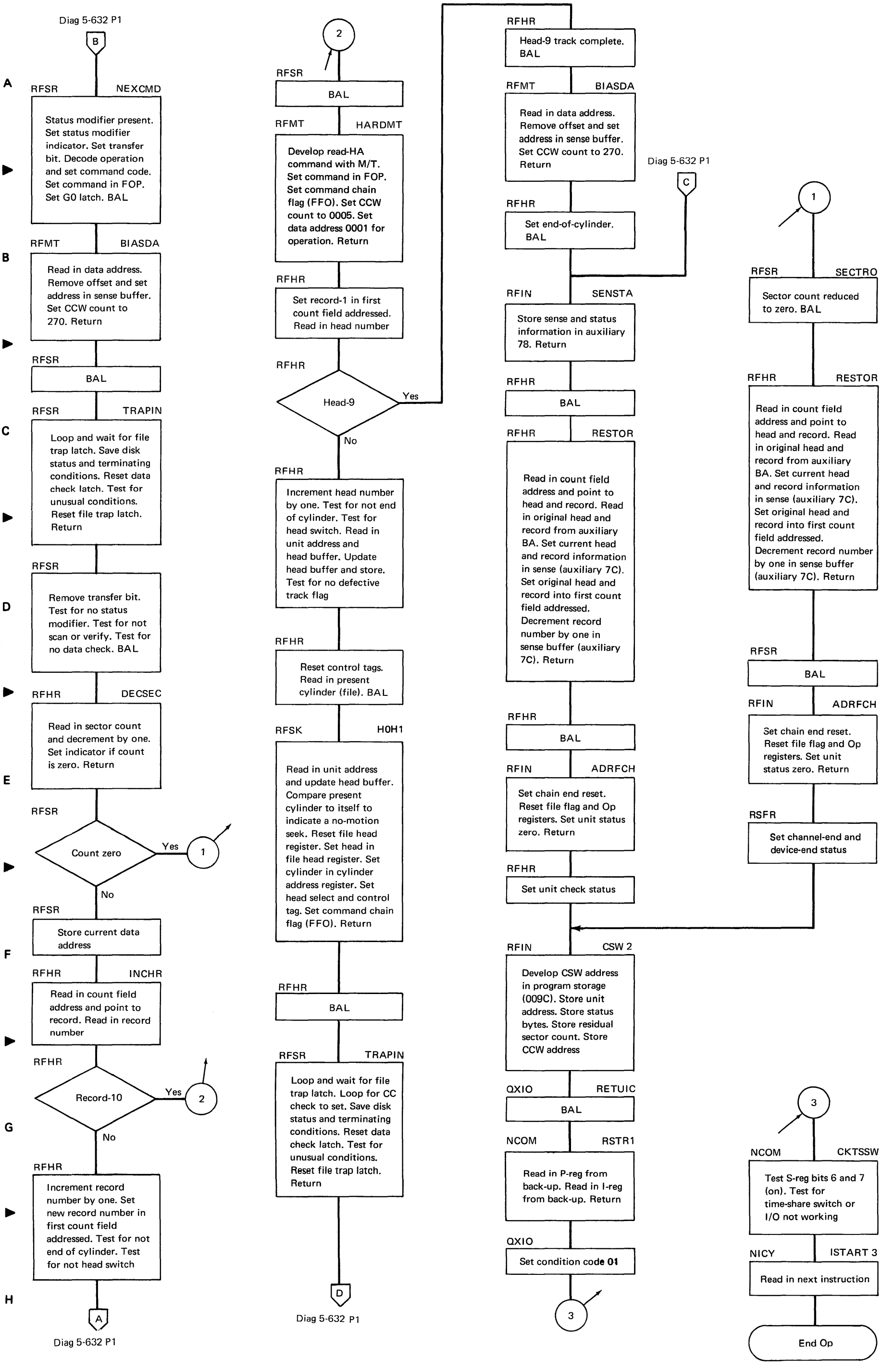
● Diagram 5-620. 1403/1403 Delayed Skip to 1 (CIO)



● Diagram 5-631. File, Write Count Data Operation



● Diagram 5-632. File, Read Data Operation (Part 1 of 2)



● Diagram 5-632. File, Read Data Operation (Part 2 of 2)

2 3 4 5 6

Diag. 5-610-P3

Enter from PICE

A

RTAA IOCHNL

Set first command and not previous TIC flags. End operation if not XIO instruction. Test device address for non-zero. Remove control unit address and replace with address in auxiliary 86. Store original device address in auxiliary BE for the CSW. Store the CCW address in auxiliary BC. BAL

B

NCOM CC2 ADJ

Test for no time-share I/O operating. Return

C

RTAA

Test for no 2560 operation

1 2

RTAA FCHCCW

Read in CCW complete. Remove the high-order four bits of count. Store next CCW address in auxiliary BC. Reset all flags except the chain bit

D

RTCD STDECD

Decode command and set operating flags

RTCD

TIC command — Yes

E

No

1st command or Previous TIC — No

Yes

RTCD

Set previous TIC flag. Add offset to data address for next CCW address

1

RTCD CNTCHK

Test for non-zero count. Reset first command and previous TIC indicators. Test for valid data address. Add offset to data address. Read device address from auxiliary

F

Program check end

RTIS INTSEL

Block traps. Set device address on bus-out. Raise address-out and select-out. Loop and wait for control unit response

G

3

H

Channel operation is initiated with the X10 instruction with a device address of 7. The instruction reads in in the NICY routine and is decoded in the PICE routine. The instruction provides the device address and the address of the first CCW. The CCW provides the command (operation), the data address in program storage, and the byte count. Additional CCW's may be chained. The CIO and TIOB instructions with a device address of 7 also enter the routine but are branched to a no-Op ending

3

RTIS

Op-in up — No

Yes

RTIS

Test for select-in up. Allow traps. Reset tags. Set condition code 11

NICY Start

Test interrupt and time-share

End Op

RTIS OPINUP

Drop address-out. Loop and wait for address-in. Read in bus-in address. Compare channel address with polled address for match. Set command on bus-out. Raise command-out line. Loop and wait for status-in. Read in bus-in status. Set burst mode. Reset status trap taken flag. Raise service-out and select-out. Allow traps

RTIS WAIT 5

Loop and wait for status trap taken flag (sets in status trap). Data loop traps in and returns

RTIS

Test for no program check. Block channel traps

RTEC ENDCHK

Test for channel-end and device-end

RTEC

Chain flag — Yes

No

RTEC

Test for not control operation. Test for correct length. Read in next CCW address. Reset tags and burst mode.

2

RTEC STRCSW

Reset tags and burst mode. Reset command

RTSC SETADR

Read in device address for CSW. Read in device status for CSW. Test correct record length. Read in channel status for CSW. Read in next CCW address from auxiliary. Decrement address by six for current CCW address. Develop CSW address. Store CSW information. Set condition code 01

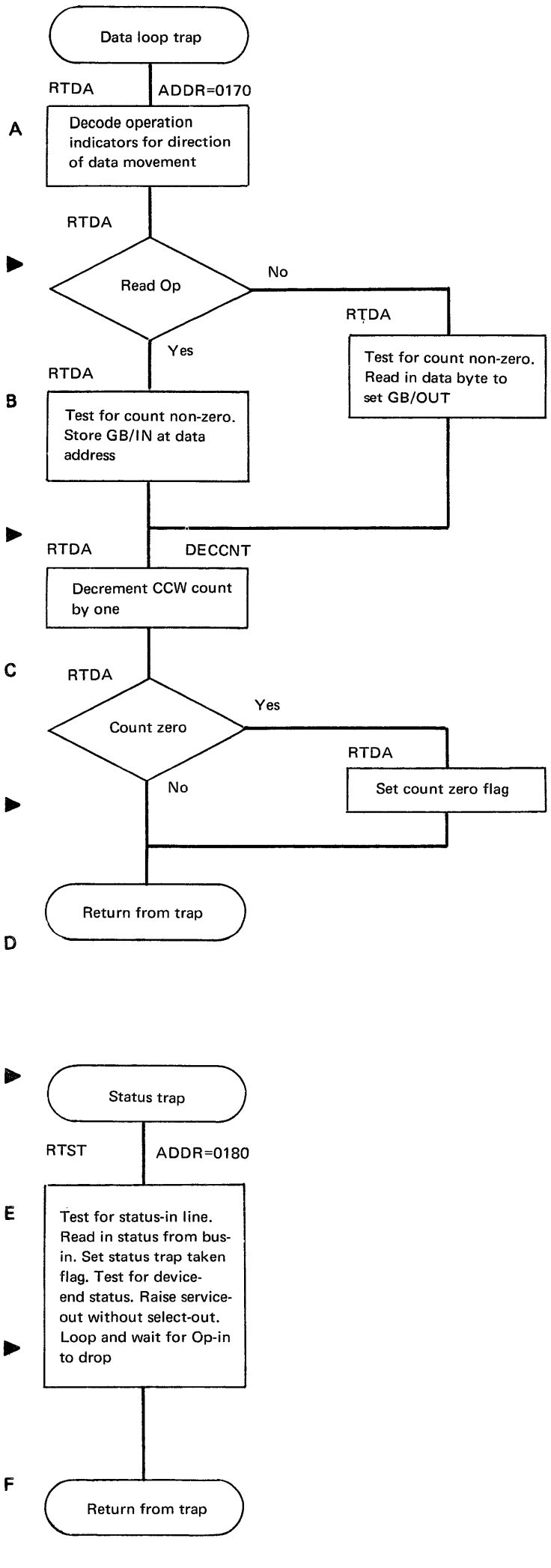
NICY START

Test interrupt and time share.

End Op

● Diagram 5-640. Channel Operation (Part 1 of 2)

2 3 4 5 6



● Diagram 5-640. Channel Operation (Part 2 of 2)

2 3 4 5 6

Instruction: D0 22 B1D1 B2D2

D0: XIO instruction (data transfer)
2: Device address (2560)
2: Function specification (read a primary card)
B1D1: Data Address
B2D2: Data Length Count.

Conditions:
1. No other I/O device is working.
2. No errors, and primary feed is ready.
3. Not last card.

Objectives:
1. Read a card from the primary feed of the 2560.
2. Transfer the number of bytes specified by the B2D2 field.
3. Transfer these bytes into storage, starting at the address specified by the B1D1 field.

MDM 5-610

From common I/O routine

PCIO — MF2560
Set mode K=70, 20 mode, 2540 externals, CPU zone 0, branch to 2560 XIO

PMRD — XO2560
Check time share byte and loop on cycle run if time share is off. Using MFS externals, test if 2560 is busy; if busy, set CC=1 (working). Branch to I-phase

PMRD — NOTPCO
Set MMSK K=81 to prevent traps while checking read or punch channel-end pending.
Reset MMSK K=81

PMRD
Bal to check length count. Store data address, length count and DA/FS in UCW

PMRD
Check FS and select primary. Check 2560 ready and not hopper check. Branch to special E-phase

PMRD — RDOPER
Check card in preread and reset read interrupt bit. Set read execute (initiate card motion)

PMSR — CCAVAIL
Set condition code = 0 (available), and set mode K=40 (20 mode, CPU externals, and CPU zone 0)

NICY — ISTART3
Return to I-phase. The program continues until a read emitter pulse initiates a 2560 read trap request

Trap Routine

PMTR — SRDTRP
Using MFR1 and MFR2 externals, transfer the read data to work registers

PMTR
Develop translate table address and fetch EBCDIC code. Fetch data address from UCW and store the EBCDIC character in program storage. Increase the data address by 1 and store in the UCW. Decrement the length count by 1 and store in the UCW

Length count = 0?
Yes
No

PMTR
Reset read request

Reset read execute and set the read channel-end bit

PMTR
Return to the point of interruption

The 2560 read trap request forces address PMTR 0140.

● Diagram 5-651. 2560 Read Operation

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Instruction: D0 27 B1D1 B2D2

A

D0: XIO instruction (data transfer)
2: Device address (2560)
7: Function specification (punch and feed a secondary card)
B1D1: Data Address
B2D2: Data Length Count

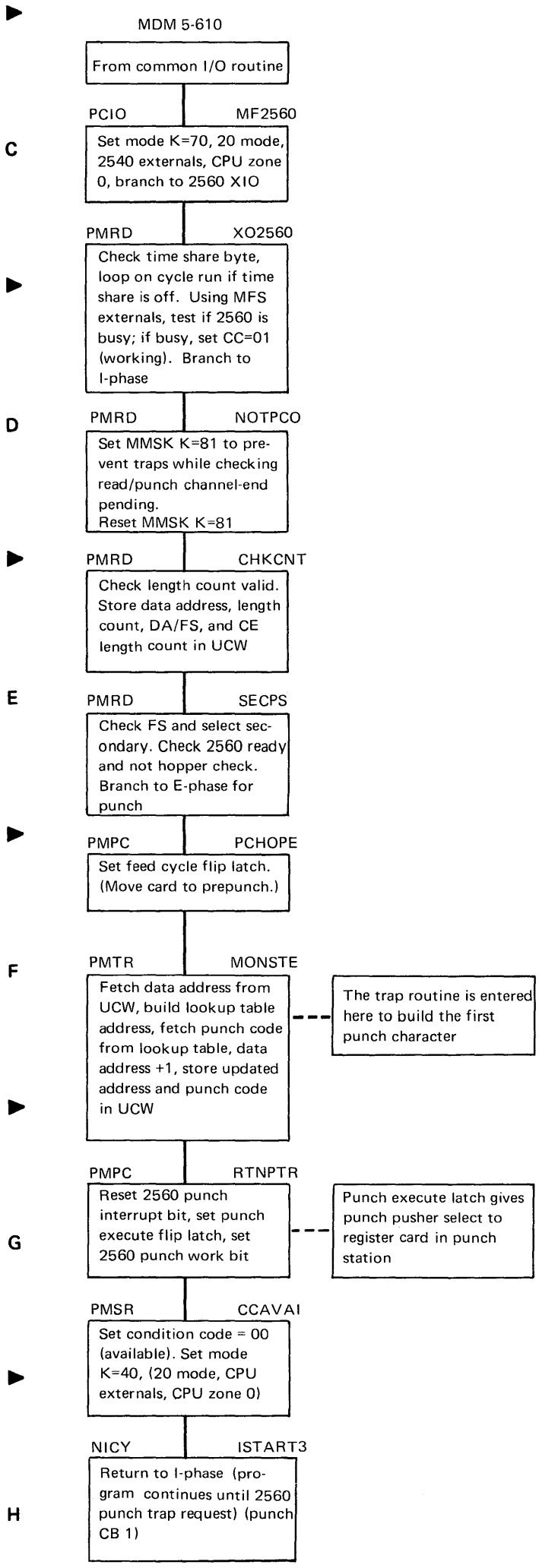
Conditions:

1. No other I/O device is working.
2. No errors, and secondary feed is ready.
3. No previous instructions.
4. Not last card.

Objectives:

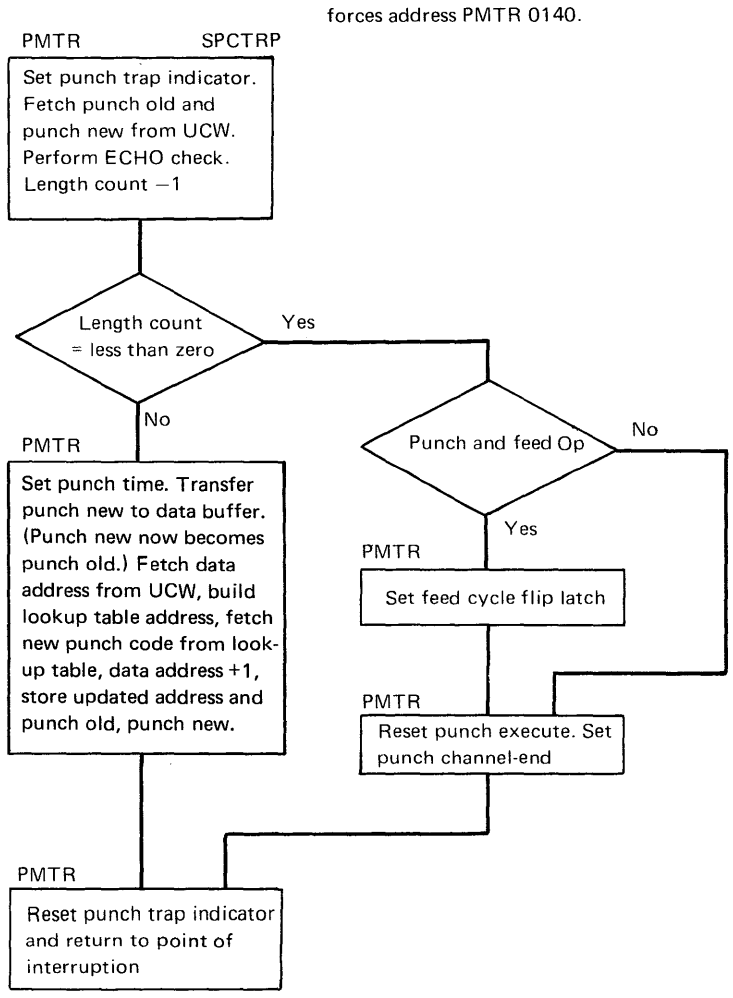
B

1. Punch a card from the 2560 secondary feed.
2. Transfer the number of bytes specified by the B2D2 field.
3. Transfer these bytes from storage to the punch, starting at the address specified by the B1D1 field.



Trap Routine

The 2560 punch trap request forces address PMTR 0140.



●Diagram 5-653. 2560 Punch Operation Chart

2 3 4 5 6

Instruction: D0 20 B1D1 B2D2

A

D0: XIO instruction (data transfer)
2: Device Address (2560)
0: Function Specification (write a card)
B1D1: Data Address
B2D2: Data Length Count

Conditions:

1. No other I/O device is working.
2. No errors, and this instruction follows a punch and stop operation in the program. (card is sitting in punch station).
3. A CIO instruction preceded the write a card XIO (to select a head).
4. Not last card.

B

Objectives:

1. Write a card from the 2560 card print station.
2. Transfer and print the number of characters specified by the B2D2 field.
3. Transfer these characters to the print magnet unit, starting at the address specified by the B1D1 field.

C

MDM 5-610

From common I/O routine

PCIO — MF2560

Set mode K=70, 20 mode, 2540 externals, CPU zone 0, branch to 2560 XIO

D

PMRD — XO2560

Check time share byte, loop on cycle run if time share bit is off. Using MFS externals, test if 2560 is busy; if busy, set CC=01 (working) and branch to I-phase. Check FS for card print Op, and branch to card print special E-phase

PMPT — CDPRNT

Set MMSK K=81, to prevent traps while checking card print channel-end pending. Reset MMSK K=81

E

PMPT — CHENO

Check length count valid (not higher than 64), store length count in UCW, put data address in work register, and fetch initial head select pattern

F

Any head select — No → Program error

Yes

Previous Op punch — No

Yes

G

PMPT — PEJF

Set punch eject flip latch (move and register card at print station)

PMPT — PPIND

Set previous print indicator and store (for next operation)

H

1

1

PMTR — CIAF

The trap routine is entered here to prepare the first character for print. Store recall address, and data address to print UCW. Fetch EBCDIC from main storage, build translate table address and store in UCW. Head count +1, and store updated head count in UCW

PMPT — GARBO

Set card print execute, set 2560 card print work bit, reset 2560 card print interrupt bit

PMSR — CCAVAI

Set condition code = 00 (available). Set mode K=40 (20 mode, CPU externals, CPU zone 0)

NICY — ISTART3

Return to I-phase (program continues until 2560 card print trap request) (print CB-1)

Trap Routine

The 2560 card print request forces address PMTR 0140.

PMTR — PRTTRP

Fetch head count, current head select pattern, and translate table address to work register. Using MFPR externals, set print pattern to print latches, select head and print

Head count = 6 — Yes

No

PMTR

Shift head select pattern once

1 — No — Next head selected

Yes

PMTR

Increase data address by 64

PMTR — JIMJE

Fetch EBCDIC to work register

PMTR

Generate translate table address and store in UCW. Head count +1 and store in UCW

PMTR — HDCT6

Length count — 1

Length count = 0 — Yes

No

PMTR — CNZE

Store length count in UCW. Recall address +1, store recall address and data address in UCW. Set head count = 0

Head 1 selected — Yes

1

No

PMTR

Set EBCDIC = 0

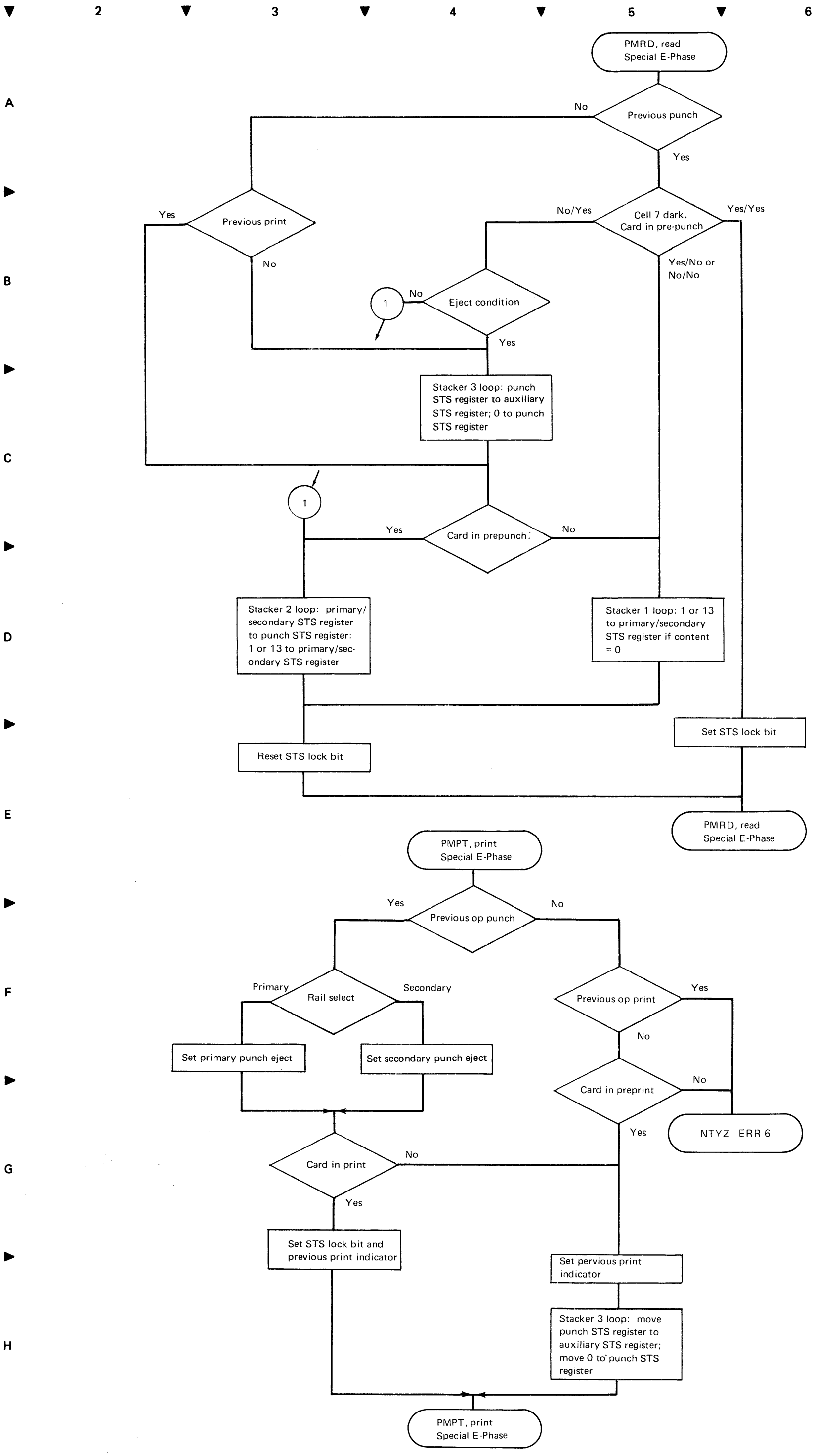
PMTR — CHARL

Reset card print execute latch. Set card print channel-end bit. Set head count = 1, store current head count, and head select pattern

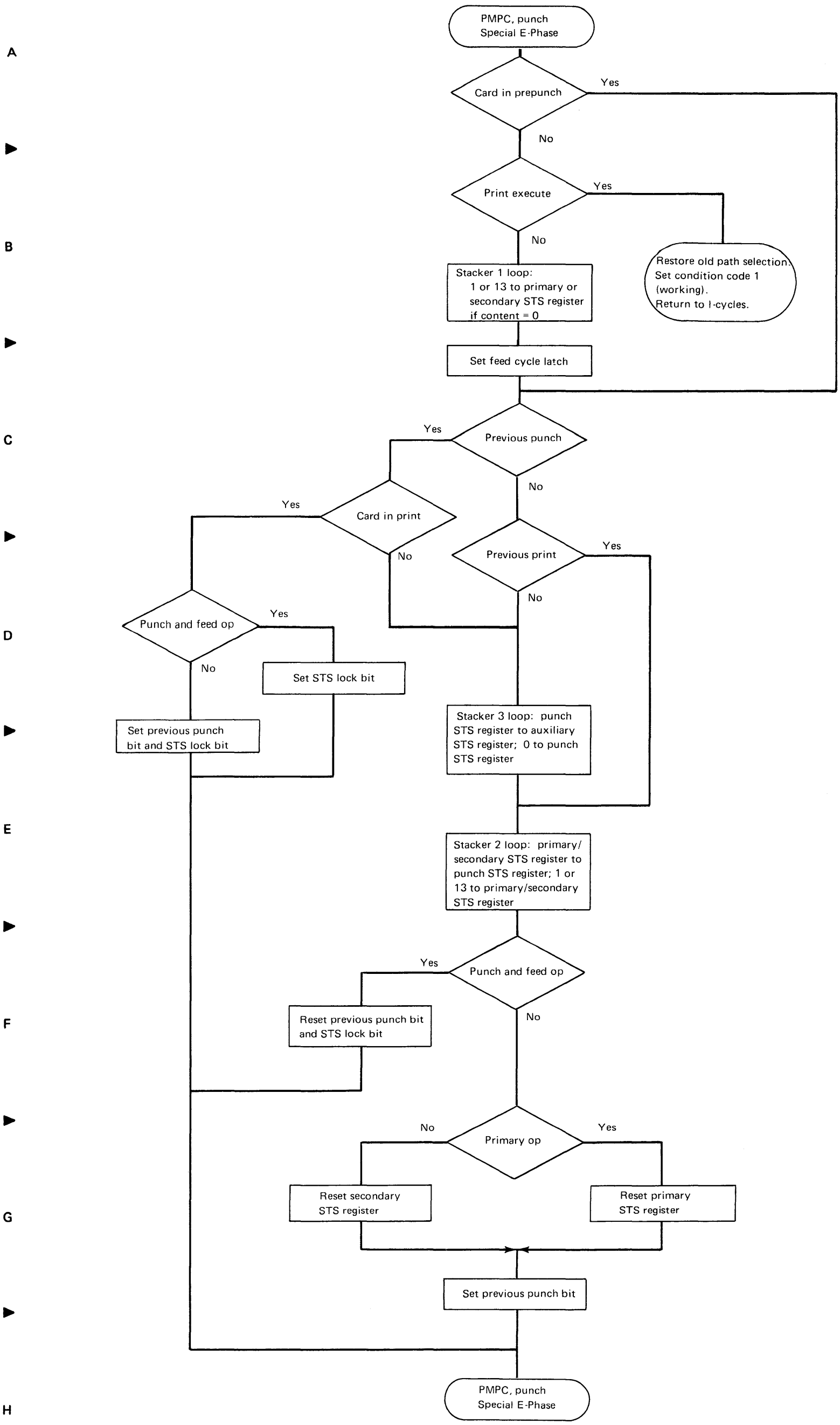
PMTR

Return to point of interruption

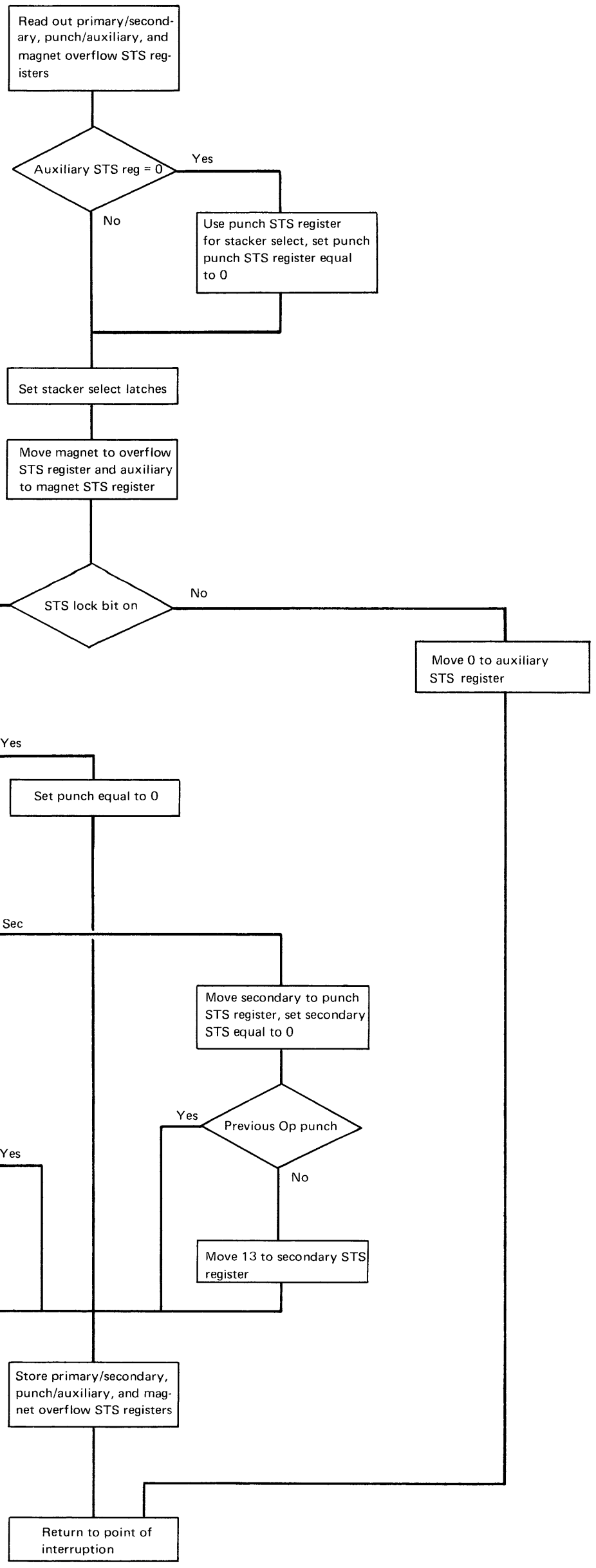
● Diagram 5-655. 2560 Print Operation Chart



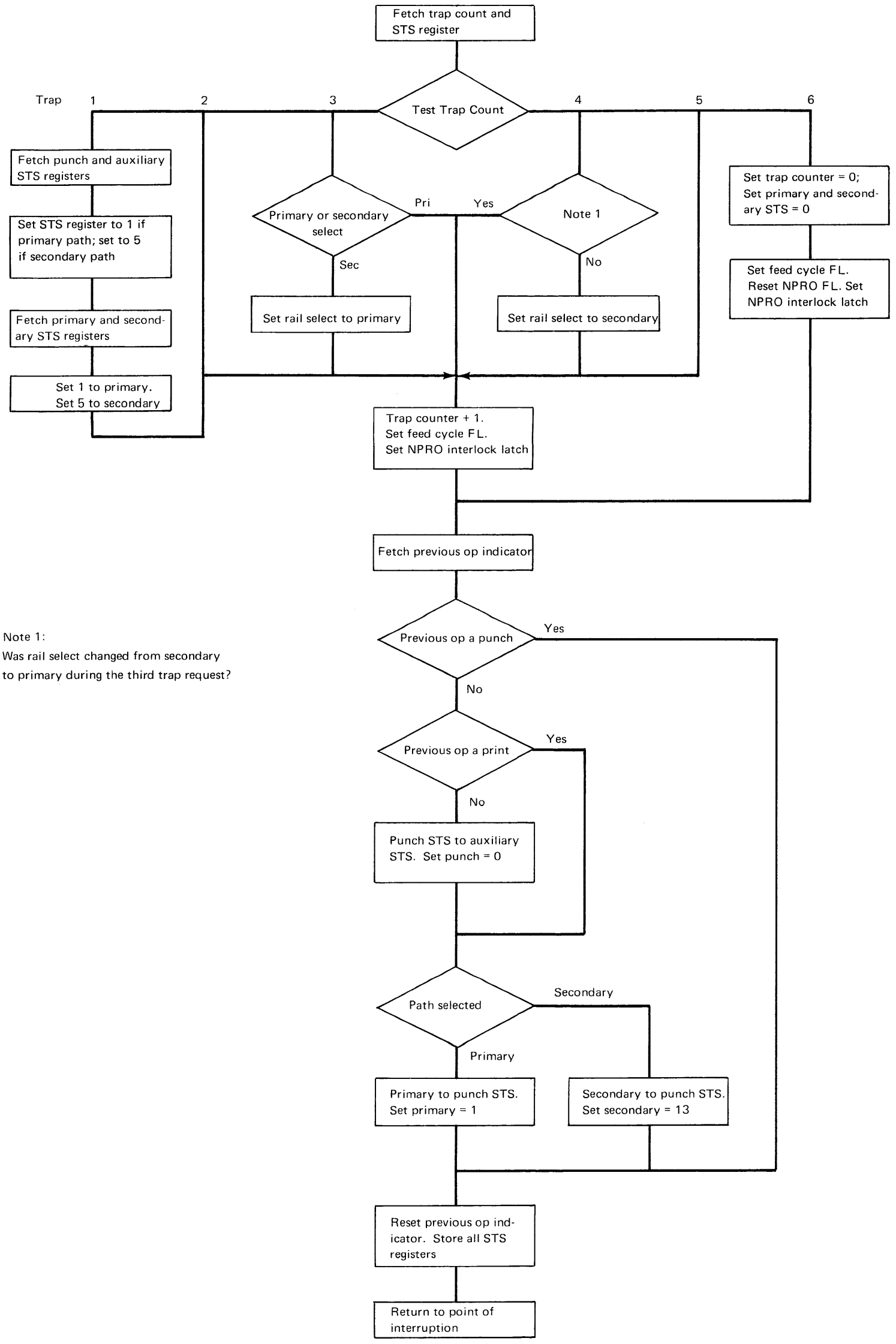
● Diagram 5-657. 2560 Read, and Print Stacker Select Operations, In Special E-Phase



● Diagram 5-659. 2560 Punch Stacker Select Operation, in Special E-Phase



● Diagram 5-661. 2560 STS Trap Routine Chart



Note 1:
Was rail select changed from secondary to primary during the third trap request?

●Diagram 5-663. 2560 NPRO Trap Routine Chart

2 3 4 5 6

Instruction: Start I/O (9C)

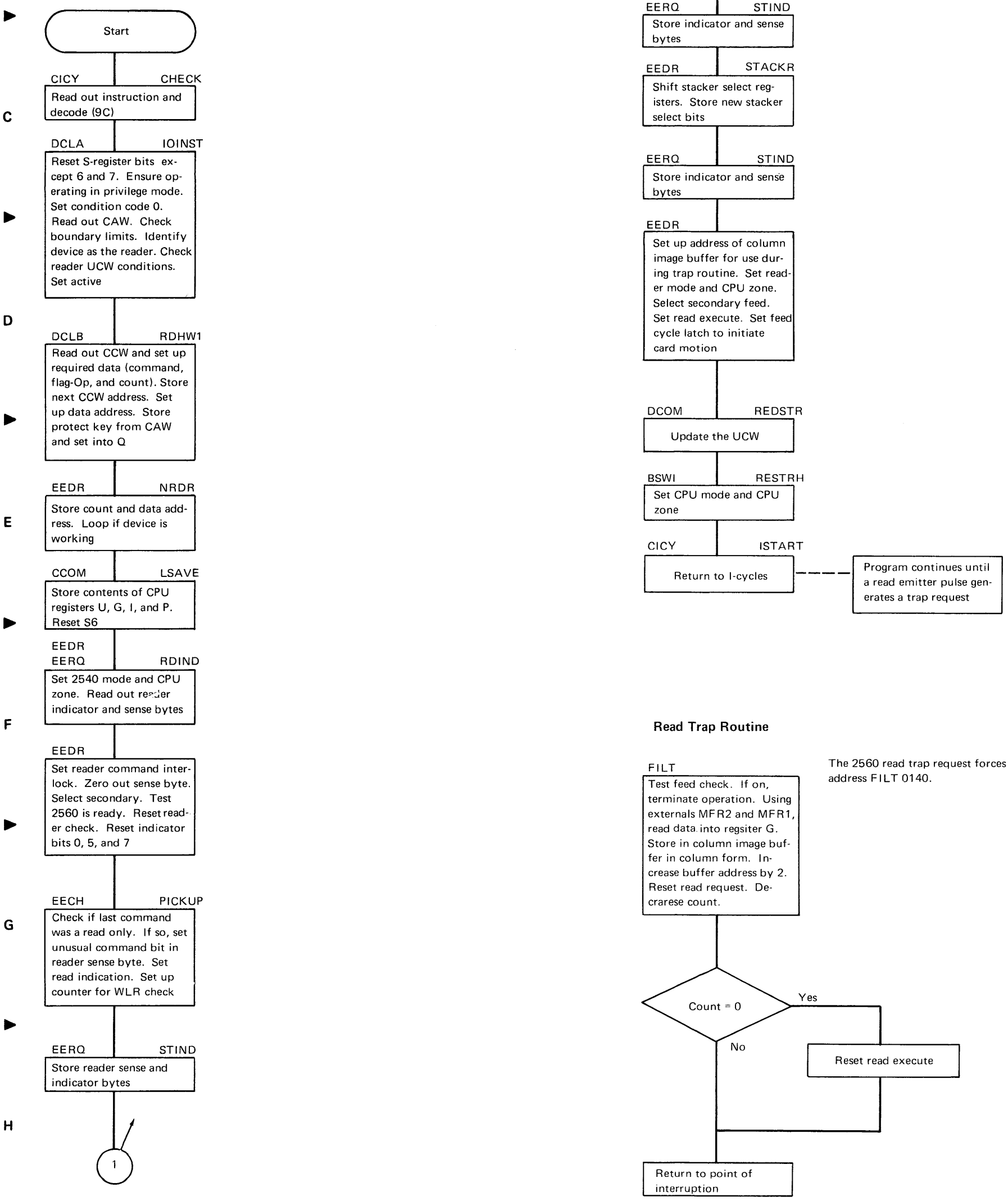
Command: Read and feed, Select Stacker

Conditions:

1. First command after run-in.
2. Status bytes and flag byte clear.
3. Card read on run-in is in the column image buffer.

Objectives:

1. Emulate the 2540 read, feed, and stacker select command using the 2560.
2. Set up reader UCW.
3. Set up for read and feed command.
4. Translate the card read on run-in and store in main storage.
5. Check validity of each character.
6. Set up 2560 for secondary feed and stacker select.
7. Start card feed and set read execute.
8. Store the card being read (in binary) in the column image buffer. This requires 80 read trap requests.
9. Set reader check if one occurs.
10. Set reader device-end.



Read Trap Routine

● Diagram 5-671. Read, Feed, and Stacker Select in 2560 Emulating the 2540

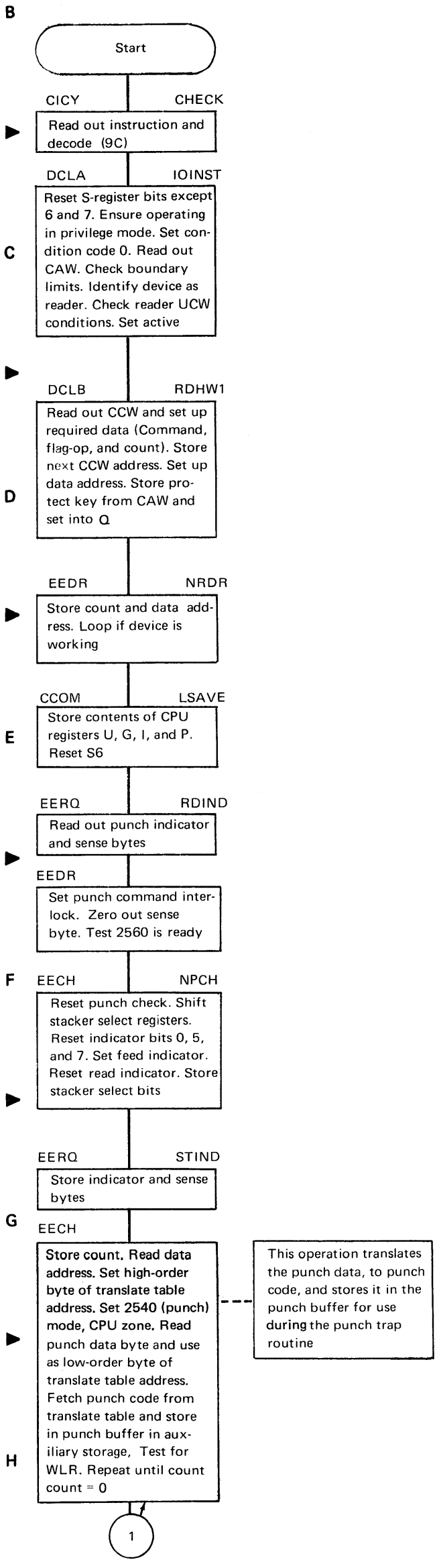
▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Instruction: Start I/O (9C)

Command: PFR Write, Feed, and Stacker Select

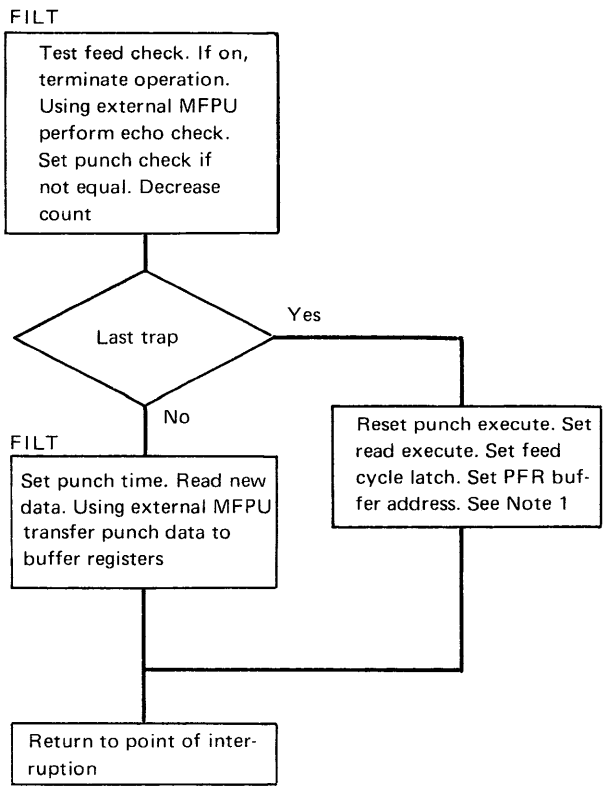
Conditions:
1. Command follows a PFR read command.
2. Status bytes and flag byte clear.
3. Cards are run-in and 2560 is ready.

Objectives:
1. Emulate the 2540 PFR write, feed, and stacker select command using the 2560.
2. Transfer and translate to punch code, the punch data from main storage to the punch buffer in auxiliary storage.
3. Transfer the punch code to the 2560 for punching.
4. Set punch check if one occurs. This will be presented with device-end of the next punch command.
5. Initiate a read cycle when punching is completed.
6. Transfer the data being read to the PFR buffer.
7. Set PFR read check if one occurs.
8. Set punch device-end.



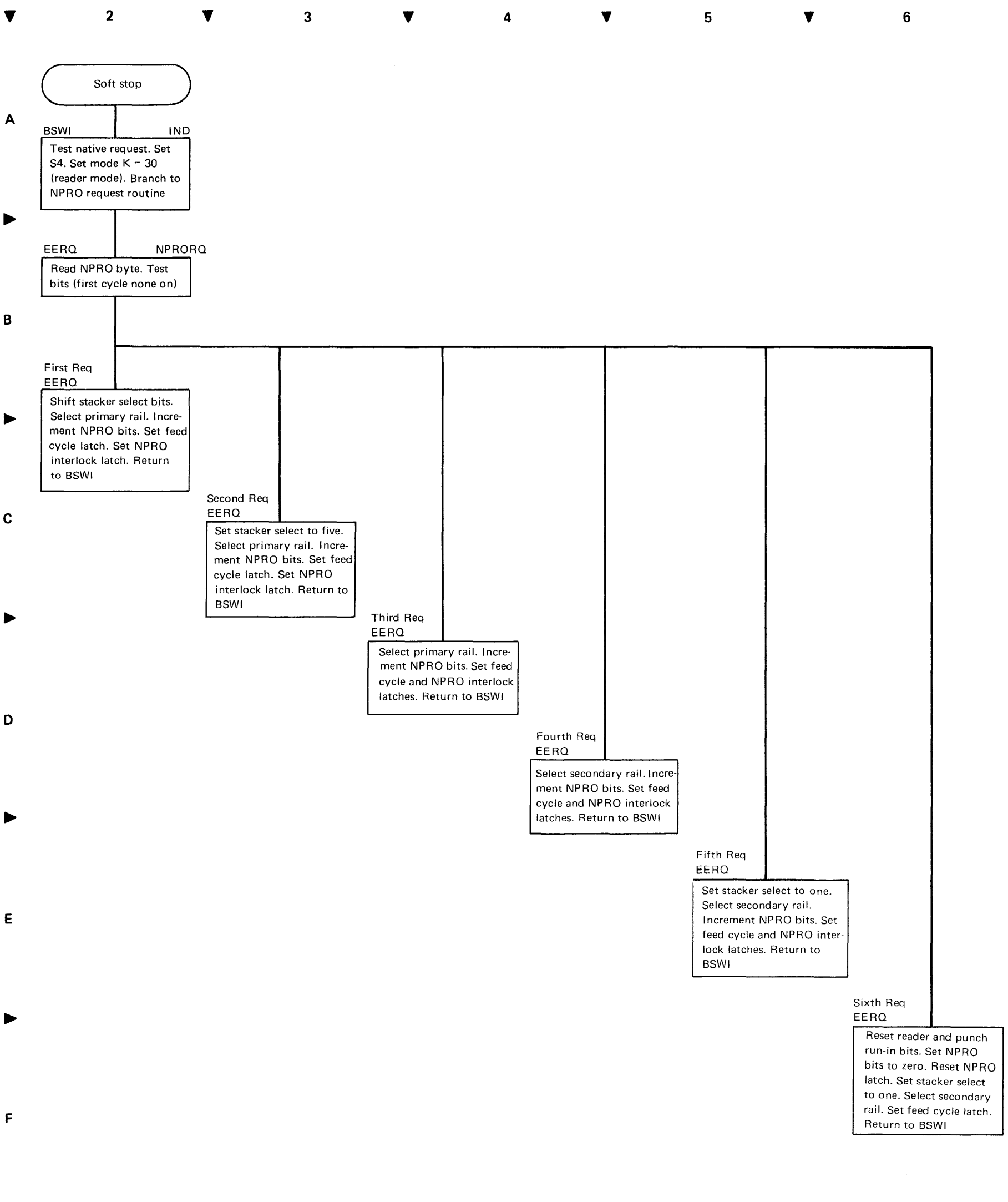
Punch Trap Routine

The 2560 punch trap request forces address FILT 0140.



Note 1: The read execute, feed cycle latch, and PFR buffer address are set to cause PFR reading of the card passing the read station. Eighty read traps occur during the resulting feed cycle. This completes the operation.

●Diagram 5-673. Write, Feed, and Stacker Select in 2560 Emulating the 2540



● Diagram 5-675. NPRO 2560 Emulating 2540

I-Cycles

General example of I8 operation (Type BIIIBBBd) showing some of the exits for other instruction types I/O portion is shown.

Microroutine

Start ICYC HISTRT

A

Objectives:
- Convert op code
- Convert addresses
- Perform indexing if required (exit to index routine and return)
- Decode operation and exit to appropriate routine for execution

Read op code
Check for exceptional condition. Check WM.
Read converted op code from aux storage,
Set in G1.

I op

Exceptional condition S7 = 0
No
Yes
INRU routine

Op code No WM
No
Yes
IERR routine

Read hundreds position. Check WM. Exit if I1 op.

I1

WM
Yes
OPI478
Set chain cmnd flag. Operation alone back date I-STAR decode op; exit.
Operation alone. Exit to appropriate routine for execution
No

5-701 Part 2
F

Translate hundreds zones & bias. Set A-address valid test for I/O ops.

Cross hundreds

1

Special character
No
NOSPCH
Shift low by 1 bit
Yes

Slash /
Yes
Translate hundreds & bias from aux storage to T-reg
No

A-hunds or B-hunds
A
B

MLU Op
Yes
Test for invalid hundreds. Set G-reg for I/O. Read tens, units and I4. Branch to compute B-address
E 5-701 Part 2
No

Blank
Yes
Set invalid hunds
1
No

Branch Op
No
Yes
Decrement I-STAR
IUBR routine

Read tens. Check WM exit if I2 or I5 op Check indexing exit if required

I2/I5

WM
No
Yes
I2/I5 op set modifier in D1 Set status decode and exit.
To appropriate routine for execution

Special character
Yes
2
No

Substitute blank
Yes
No

Tens zone
No
Yes
B Indexing routine Diag 5-703

Blank
Yes
No
2
Set invalid hundreds

5-701 Part 2

Diagram 5-701. 1400 Compatibility, I-Cycles (Part 1 of 2)

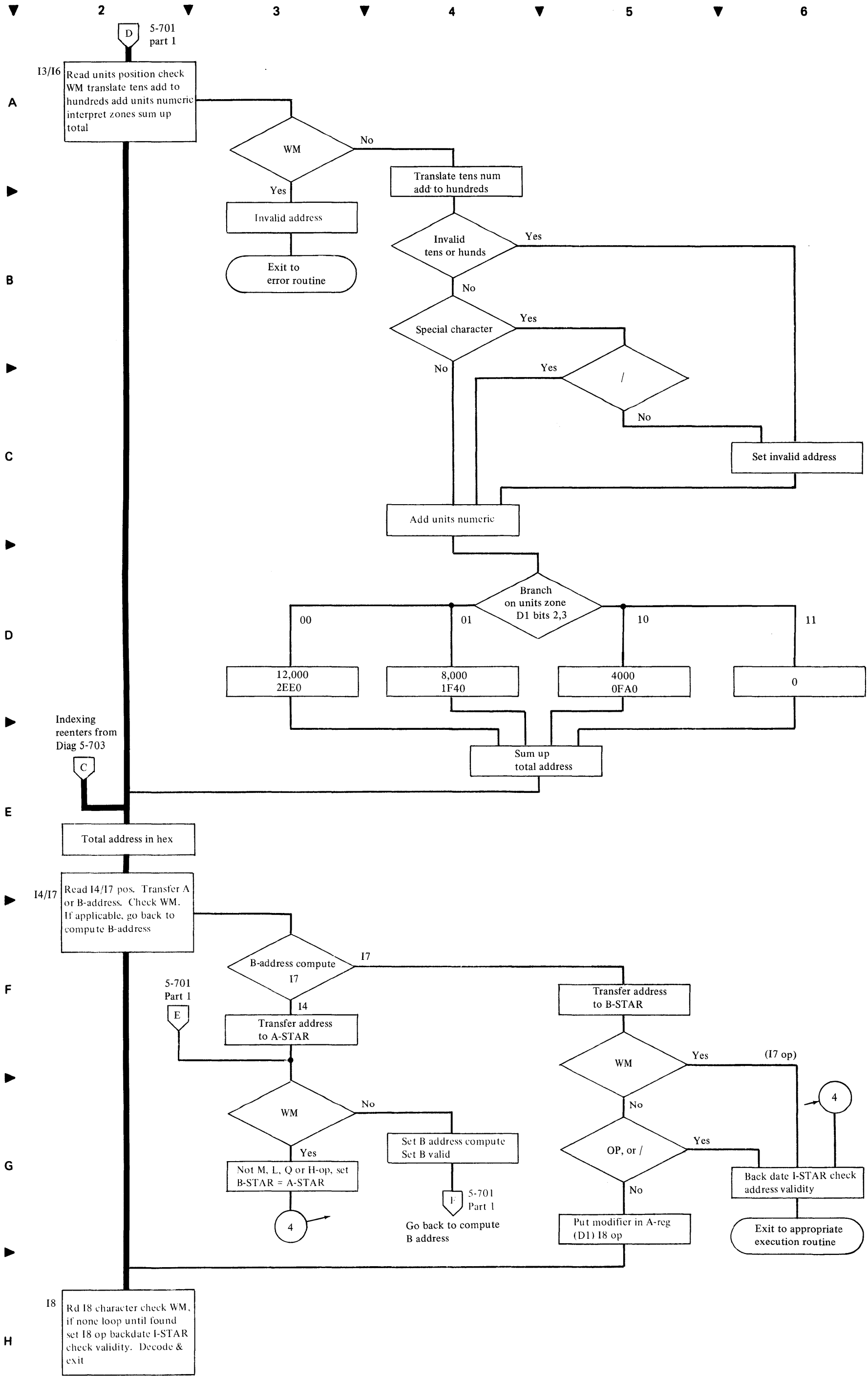
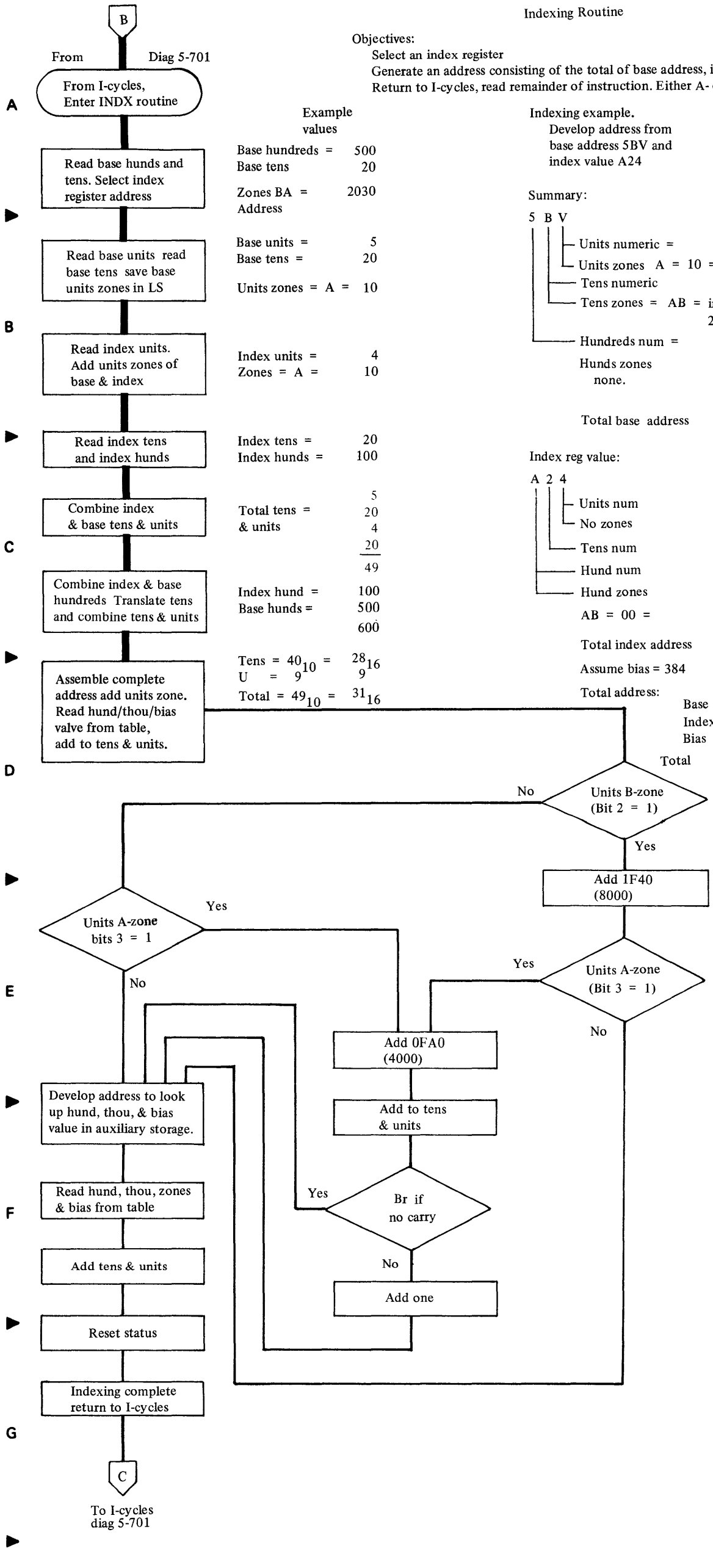


Diagram 5-701. 1400 Compatibility, I-Cycles (Part 2 of 2)

Indexing Routine

Objectives:
Select an index register
Generate an address consisting of the total of base address, index register and the bias.
Return to I-cycles, read remainder of instruction. Either A- or B-address or both may be indexed.



Example values

Base hundreds = 500
Base tens 20

Zones BA = 2030
Address

Base units = 5
Base tens = 20

Units zones = A = 10

Index units = 4
Zones = A = 10

Index tens = 20
Index hunds = 100

Total tens = 5
& units 20
4
20
49

Index hund = 100
Base hunds = 500
600

Tens = 40_{10} = 28_{16}
U = 9_{10} = 9_{16}
Total = 49_{10} = 31_{16}

Base
Index
Bias
Total

Indexing example.
Develop address from base address 5BV and index value A24

Summary:

5 B V
- Units numeric =
- Units zones A = 10 =
- Tens numeric
- Tens zones = AB = index reg 2030
- Hundreds num =

Hunds zones none.

Total base address

Index reg value:

A 2 4
- Units num
- No zones
- Tens num
- Hund num
- Hund zones

AB = 00 =

Total index address

Assume bias = 384

Total address:

Index register addresses

Tens position BCD zones	EBCDIC bits 2, 3	Aux storage address
None	11	None
A	10	2010
B	01	2020
BA	00	2030

5
4000
20
500

Hundreds zones values

4525

1400 BA	BCD	EBCDIC	Decimal value
BA	11	00	3000
B	10	01	200
A	01	10	1000
None	00	11	

4
20
100

Units zones values

3000

1400 BA	BCD	EBCDIC	Decimal value
BA	11	00	12,000
B	10	01	8,000
A	01	10	4,000
None	00	11	

3124
4525
3124
384
8033_{10}
or $1F6_{16}$

Example (cont)

(Accumulate amounts in boxes

Unit A-zone: 0FA0

Table location 2078

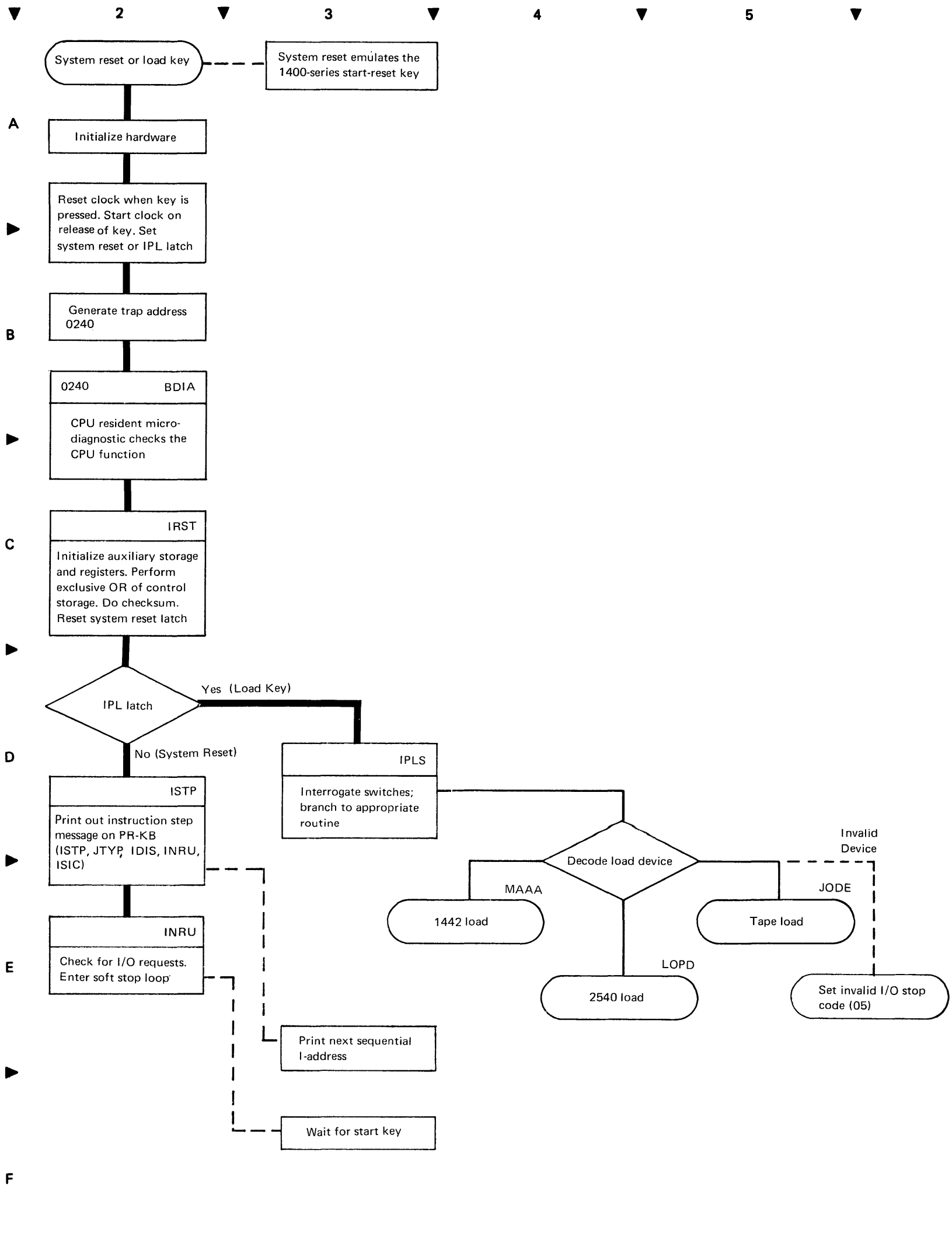
From table (inc bias): 0F90

Units & tens: 31

Total = 1F61

(Decimal 8,033)

Diagram 5-703. 1400 Compatibility, Indexing



● Diagram 5-709. 1400 Compatibility–System Reset/IPL

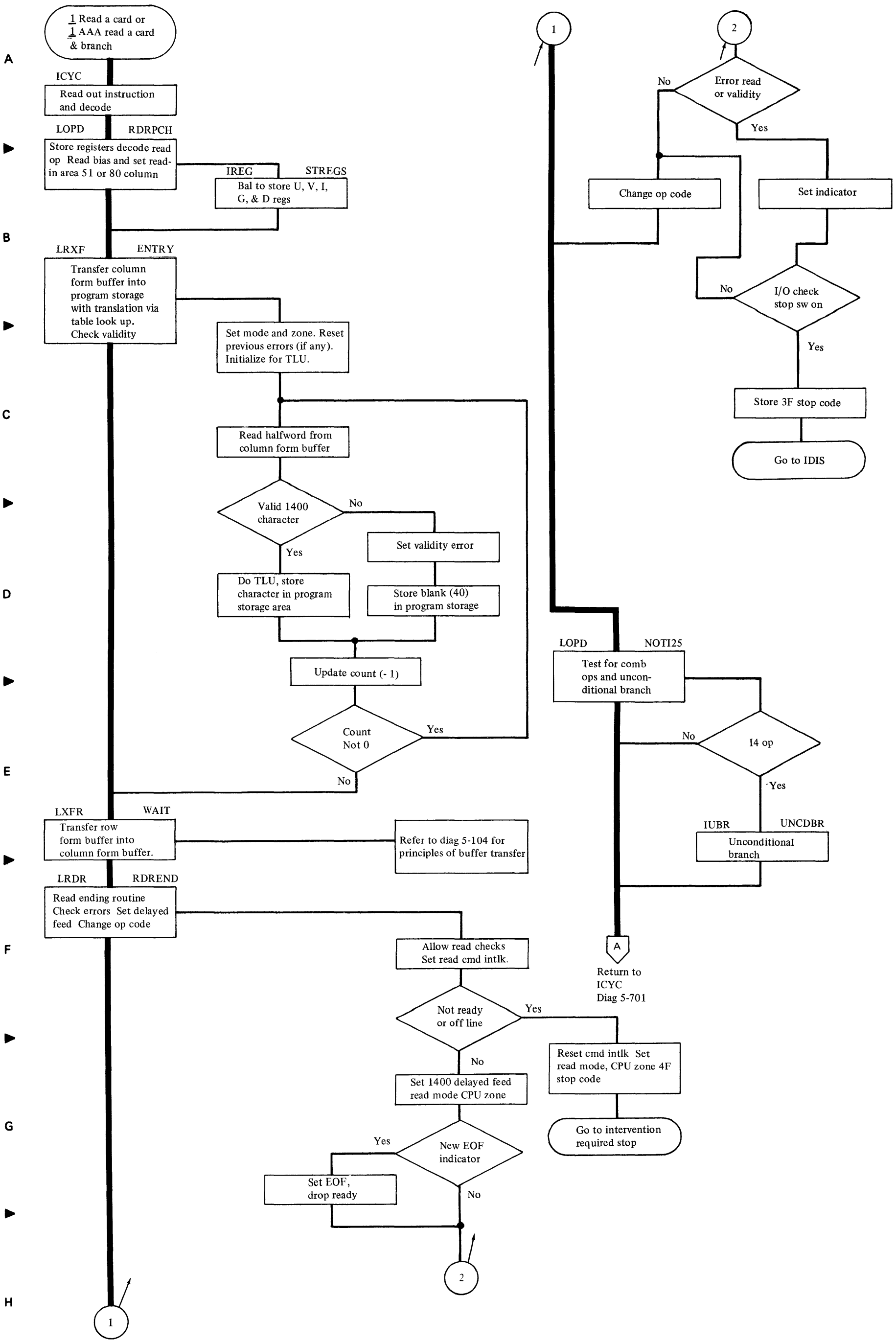


Diagram 5-713. 1400 Compatibility, 1402 Read

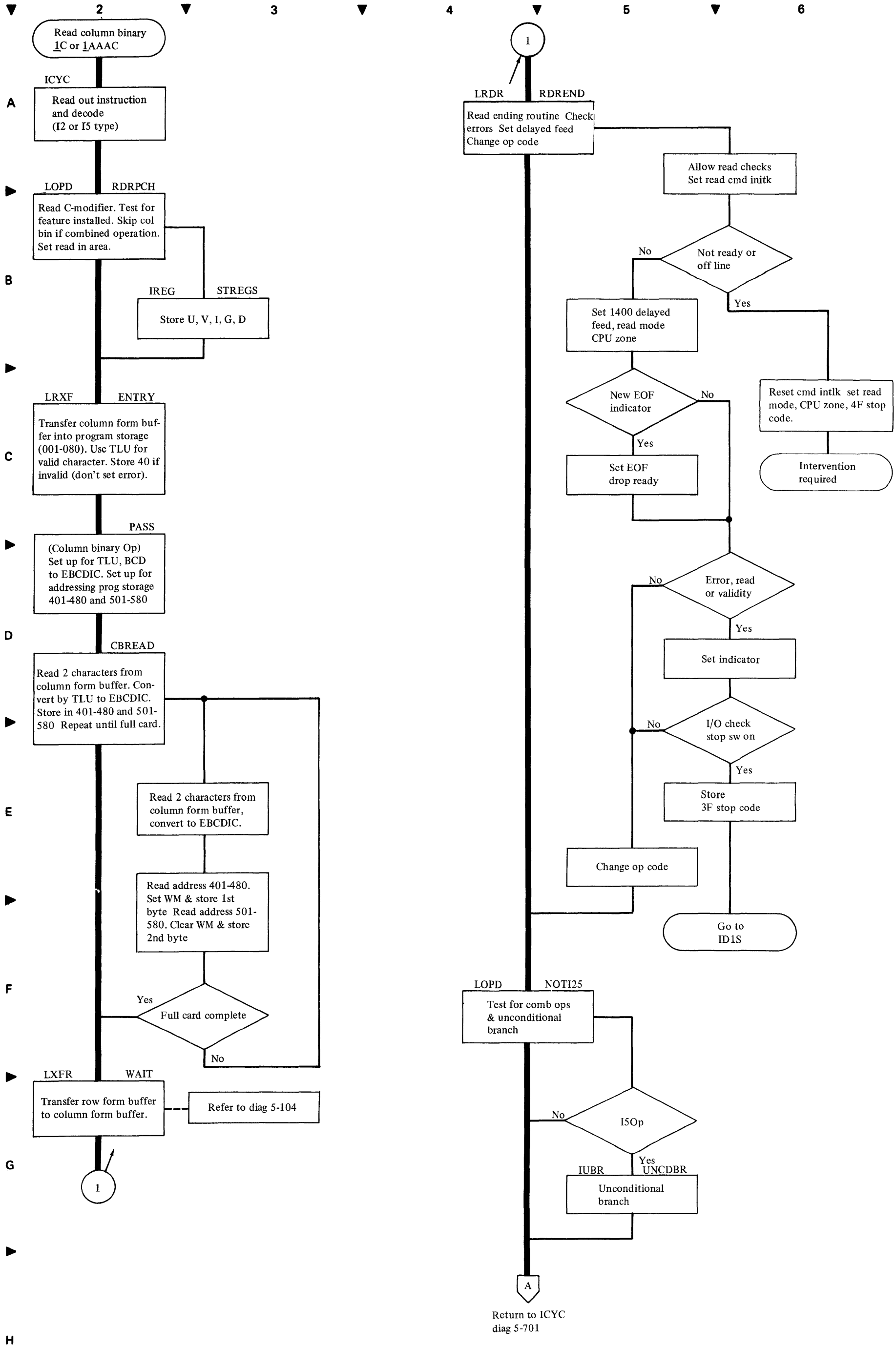


Diagram 5-715. 1400 Compatibility, 1402 Read Column Binary

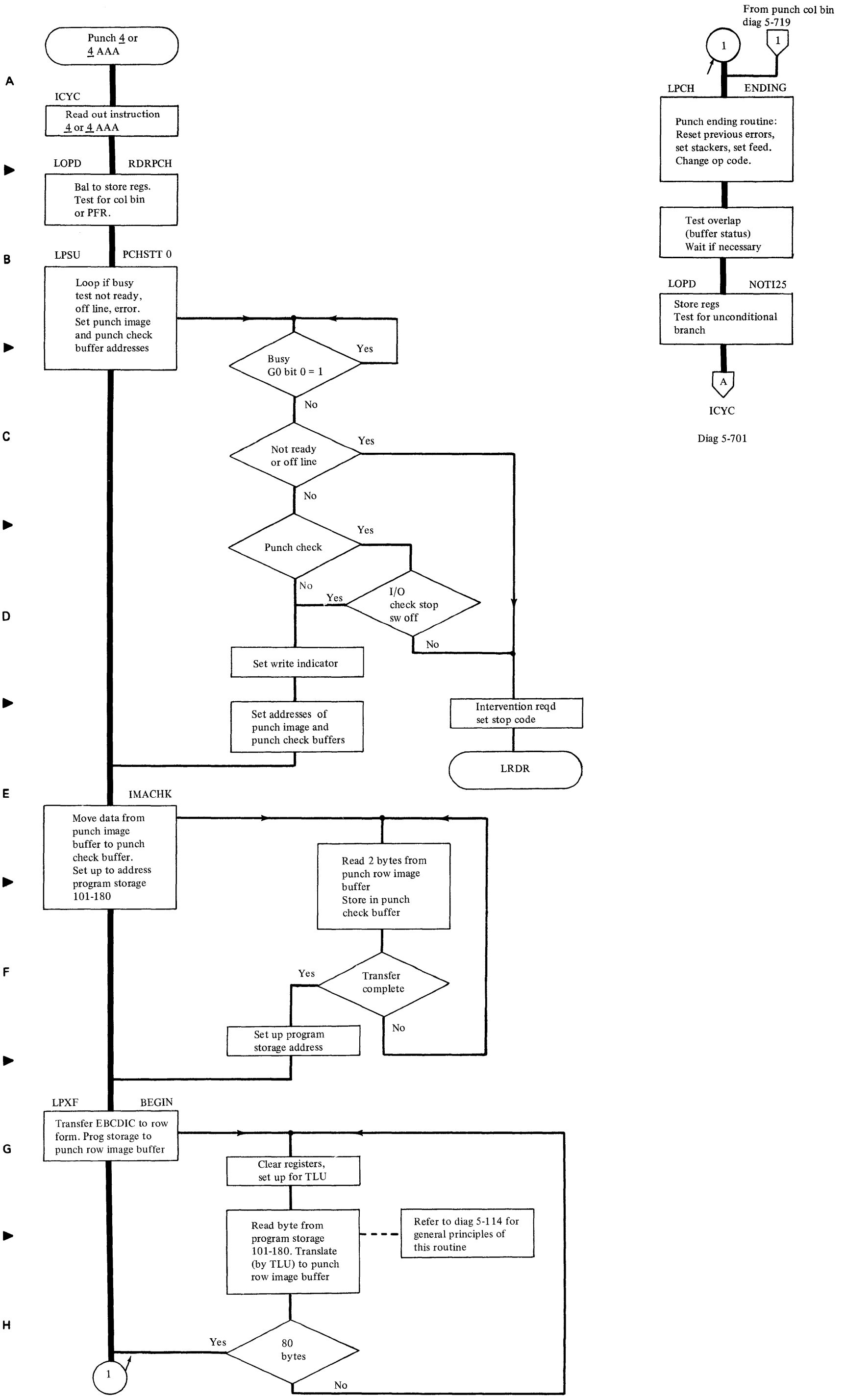


Diagram 5-717 1400 Compatibility, 1402 Punch

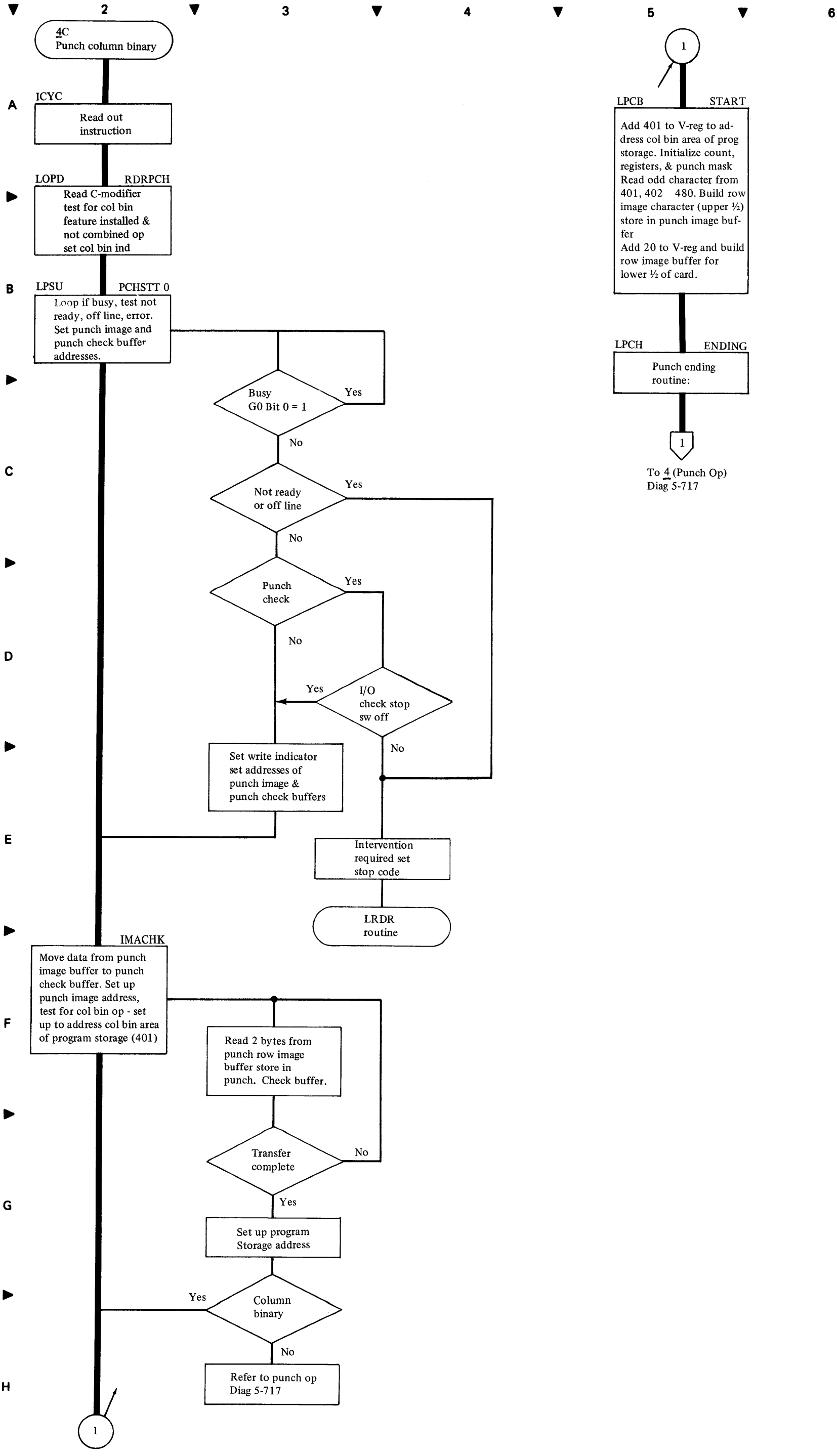
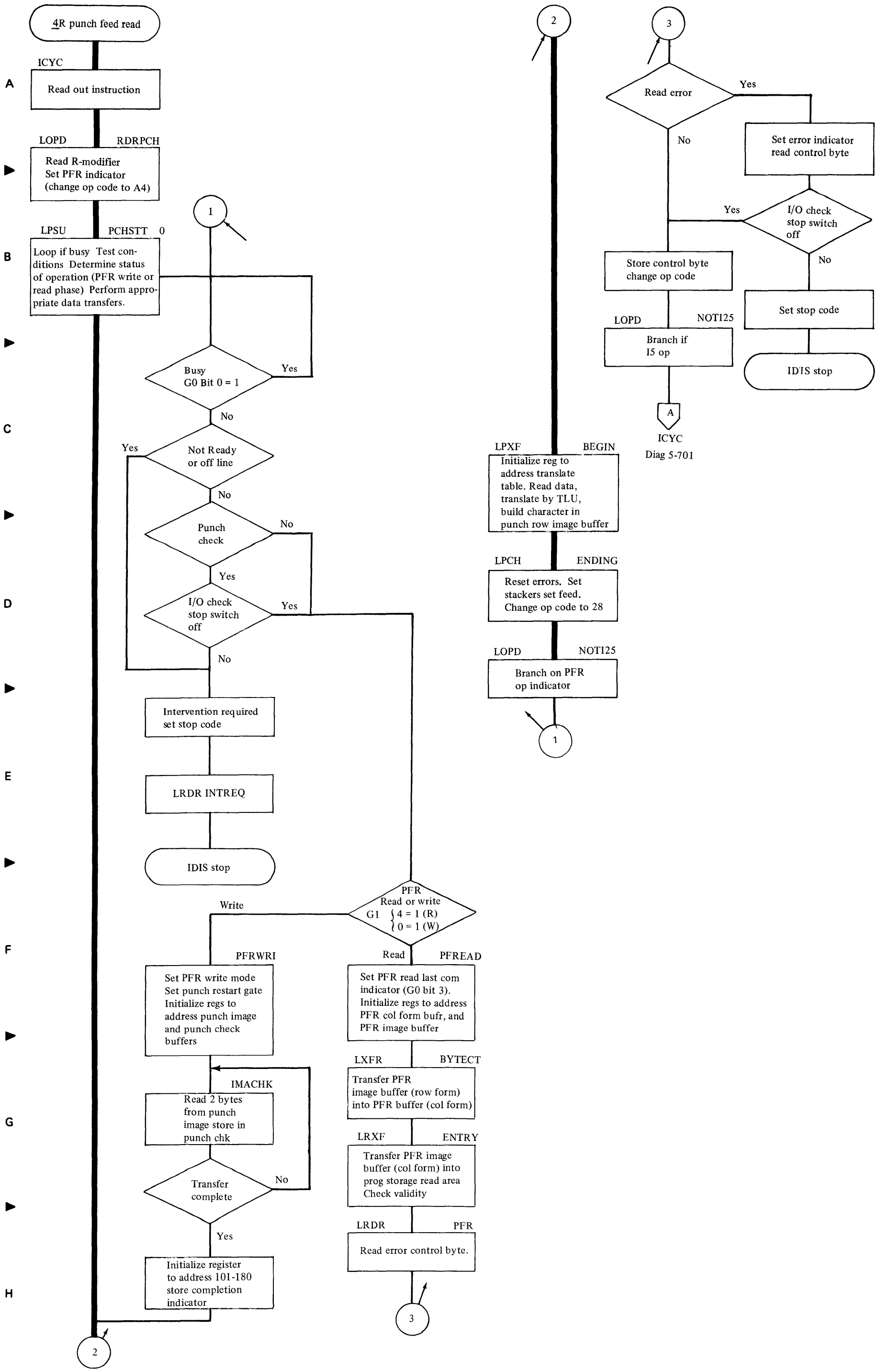
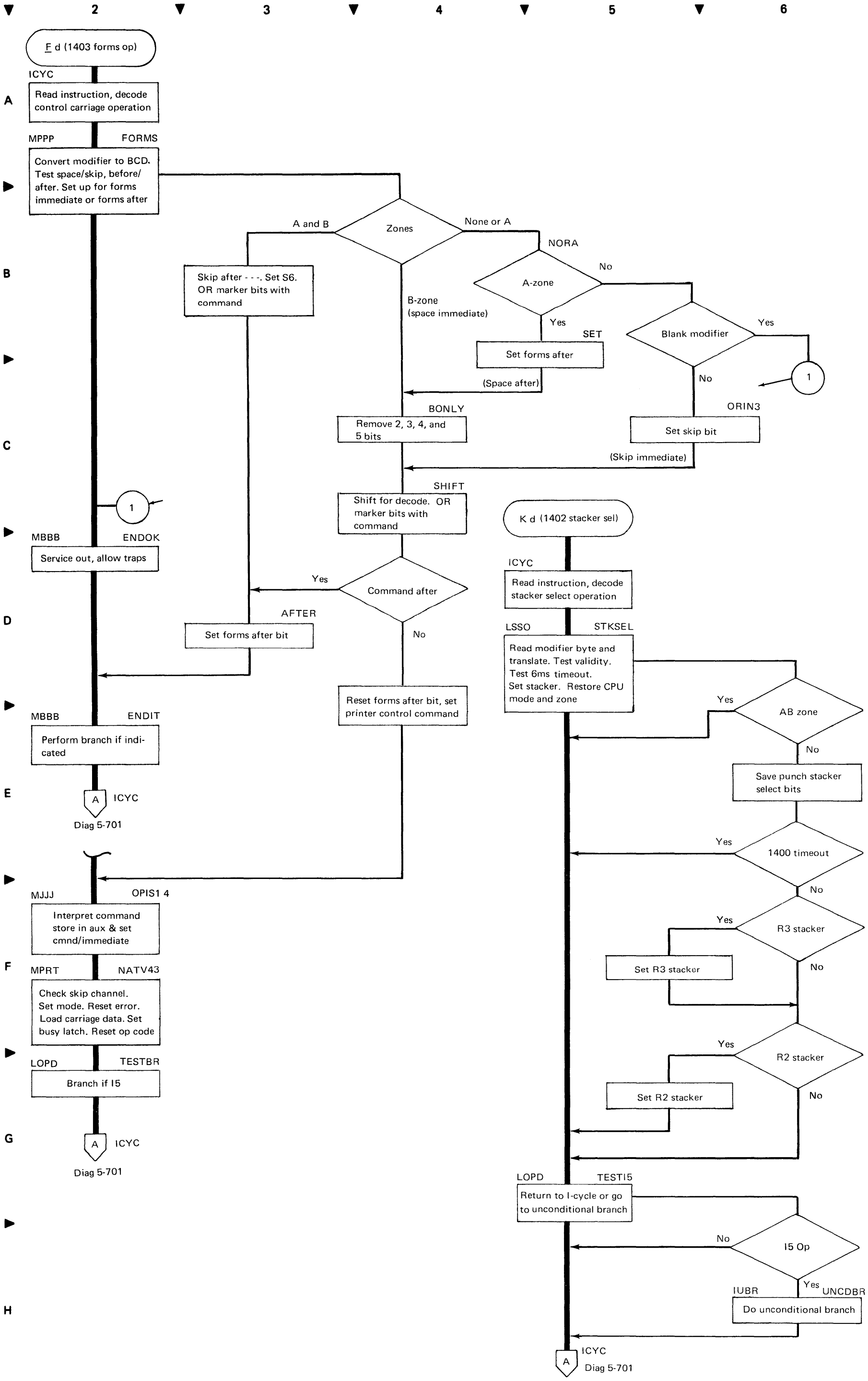


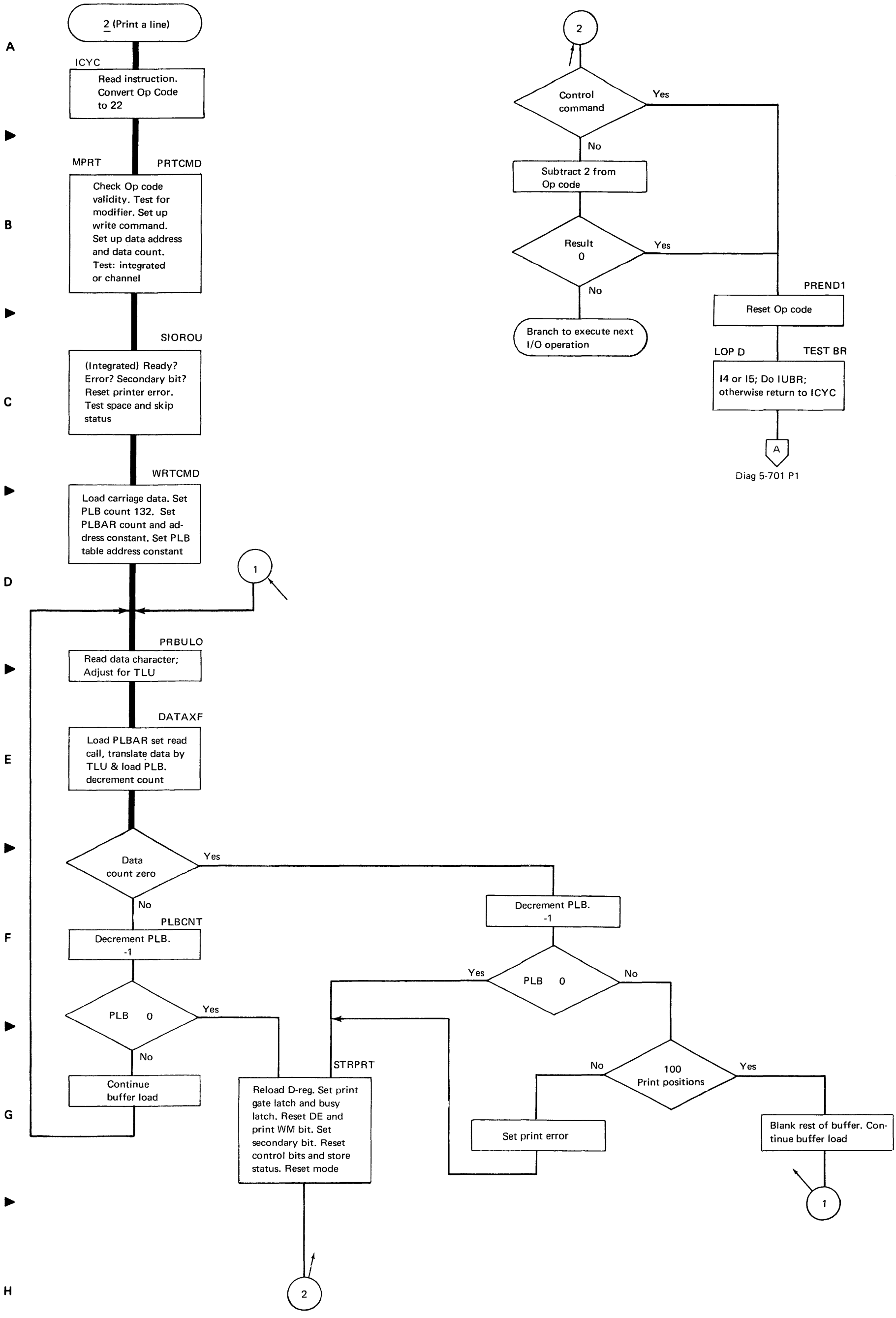
Diagram 5-719 1400 Compatibility, 1402 Punch Column Binary



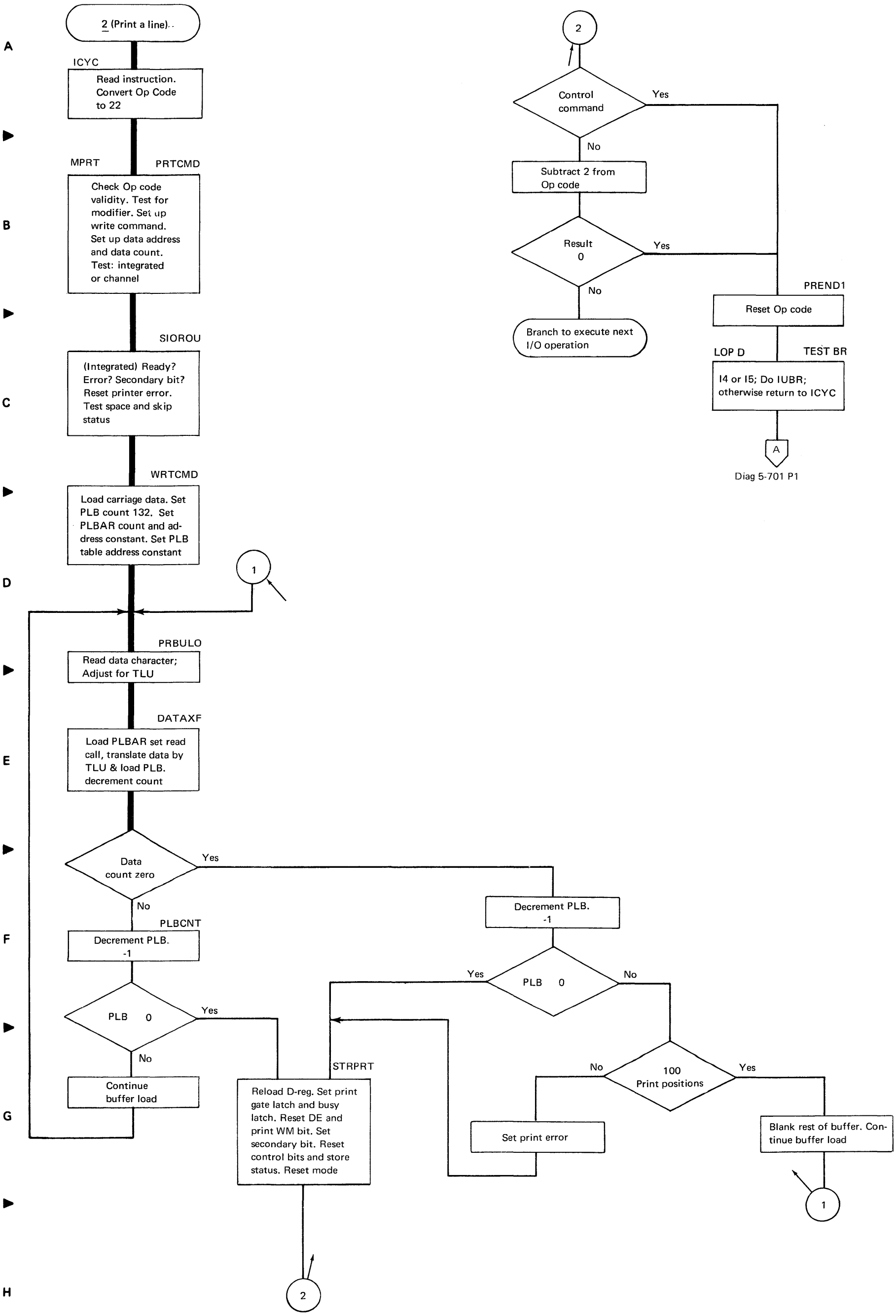
● Diagram 5-721 1400 Compatibility, 1402 Punch Feed Read



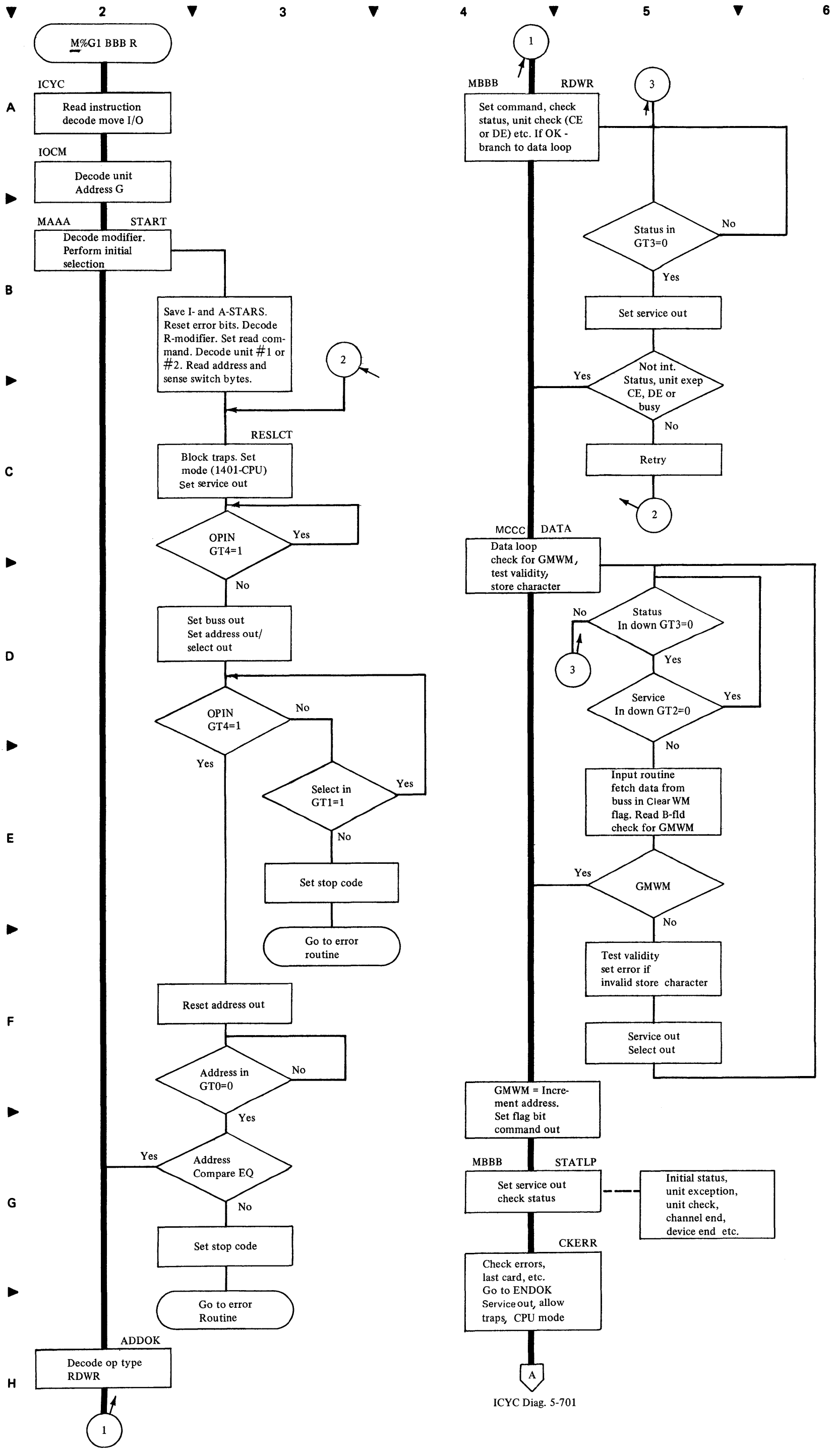
● Diagram 5-722. 1400 Compatibility–1403 Forms Op and 1442 Stacker Select Op



● Diagram 5-723. 1400 Compatibility - 1403 Print

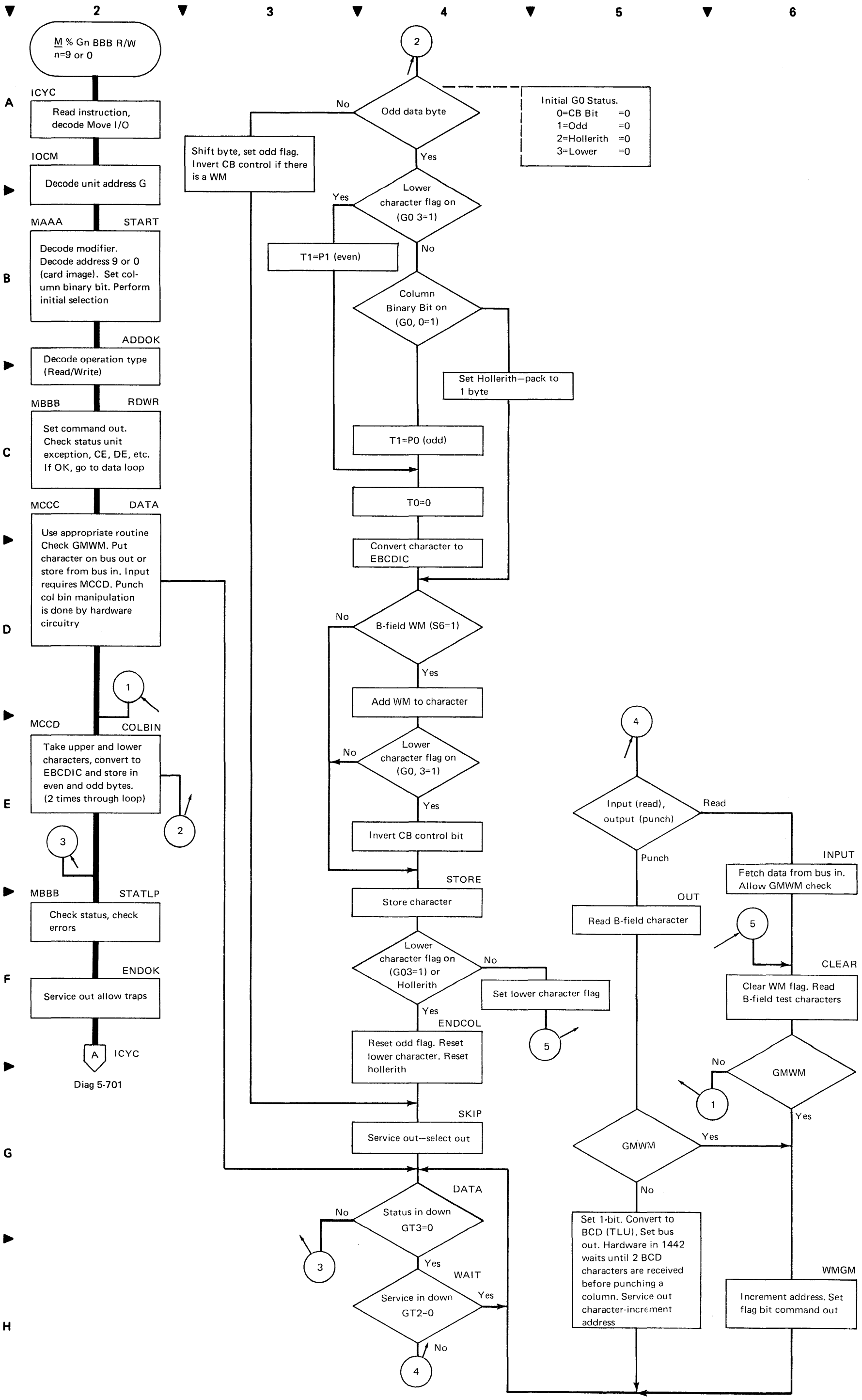


● Diagram 5-723. 1400 Compatibility - 1403 Print

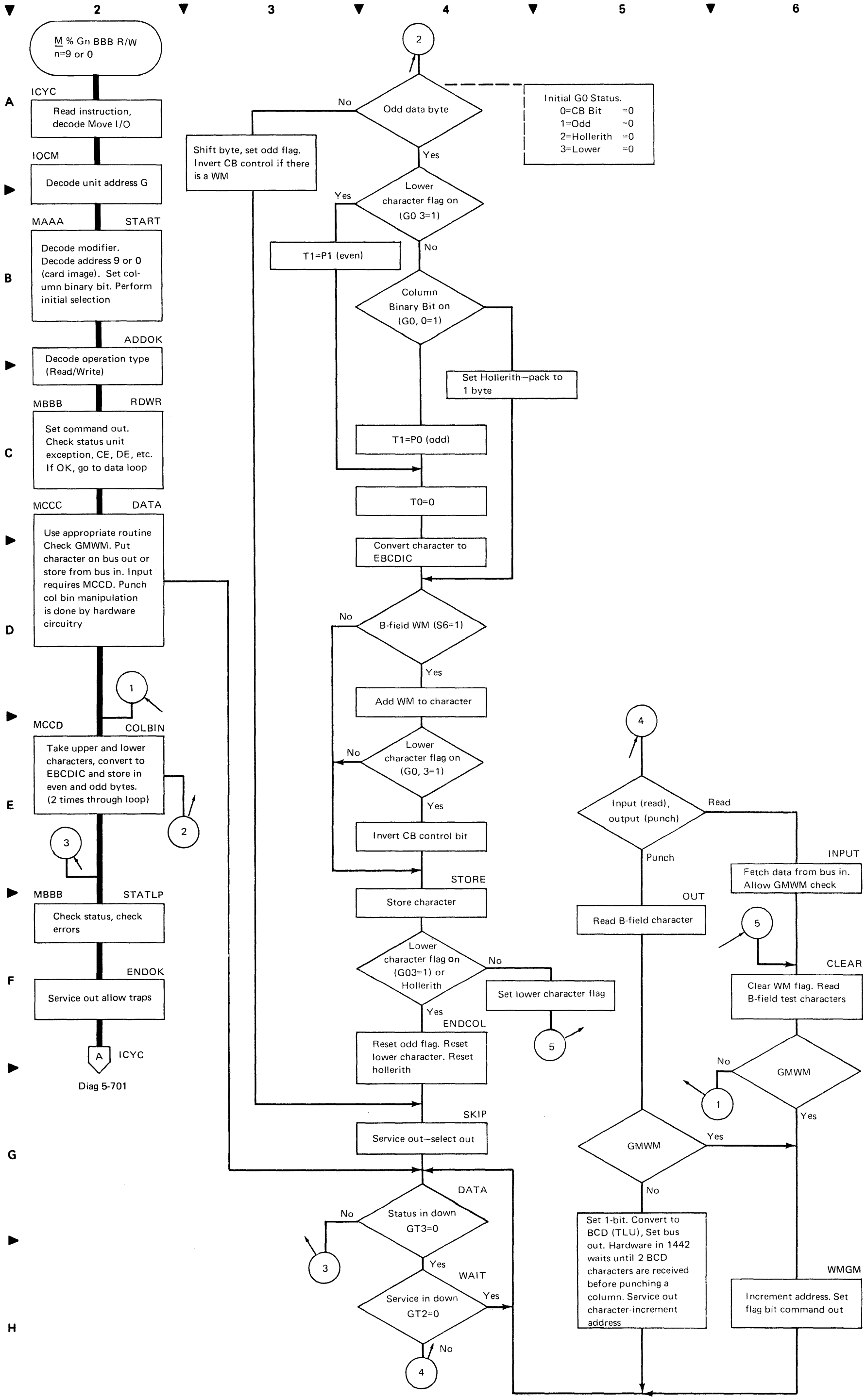


ICYC Diag. 5-701

Diagram 5-725. 1400 Compatibility, 1442 Read



● Diagram 5-727. 1400 Compatibility–1442 Read/Punch Card Image



● Diagram 5-727. 1400 Compatibility–1442 Read/Punch Card Image

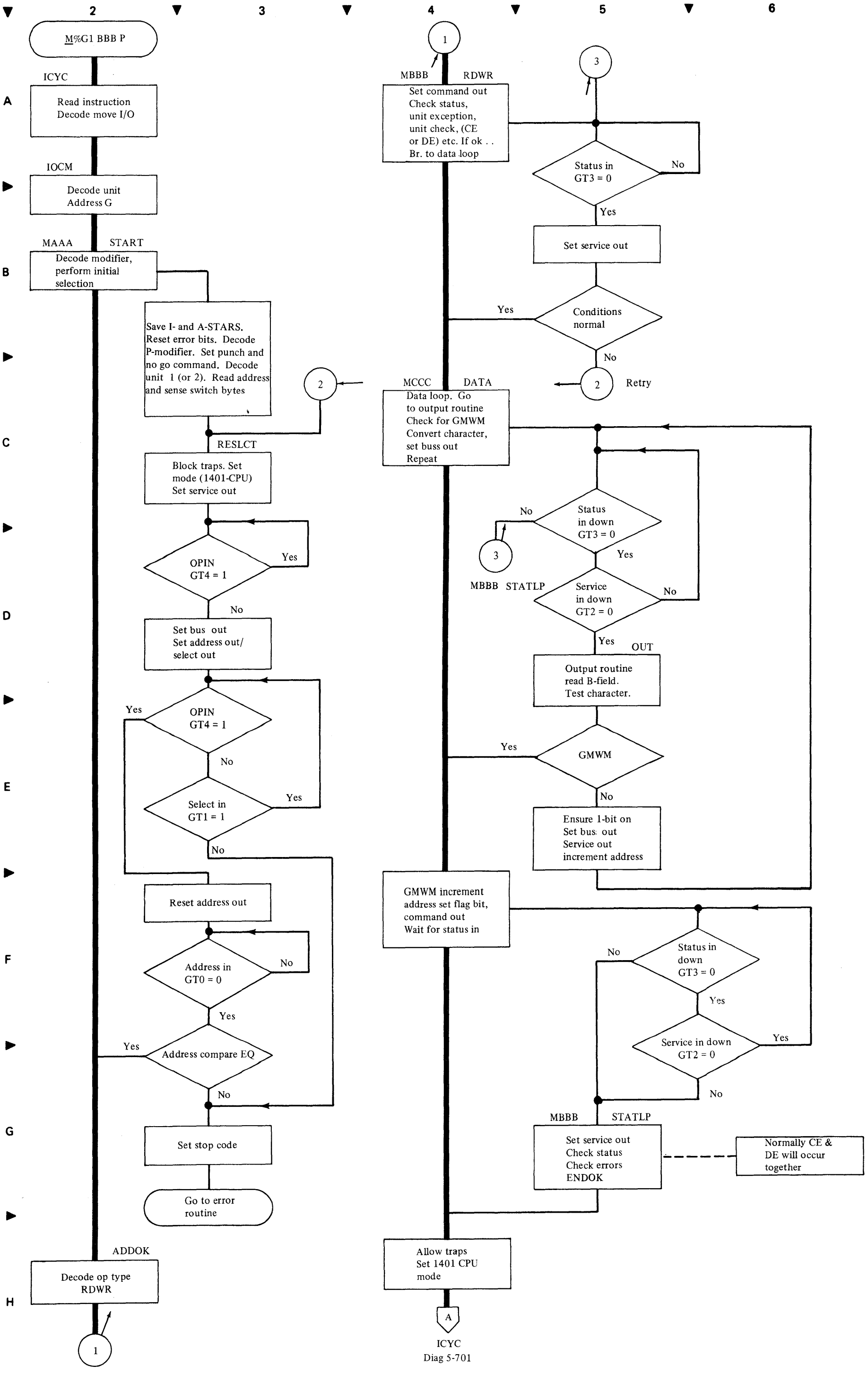
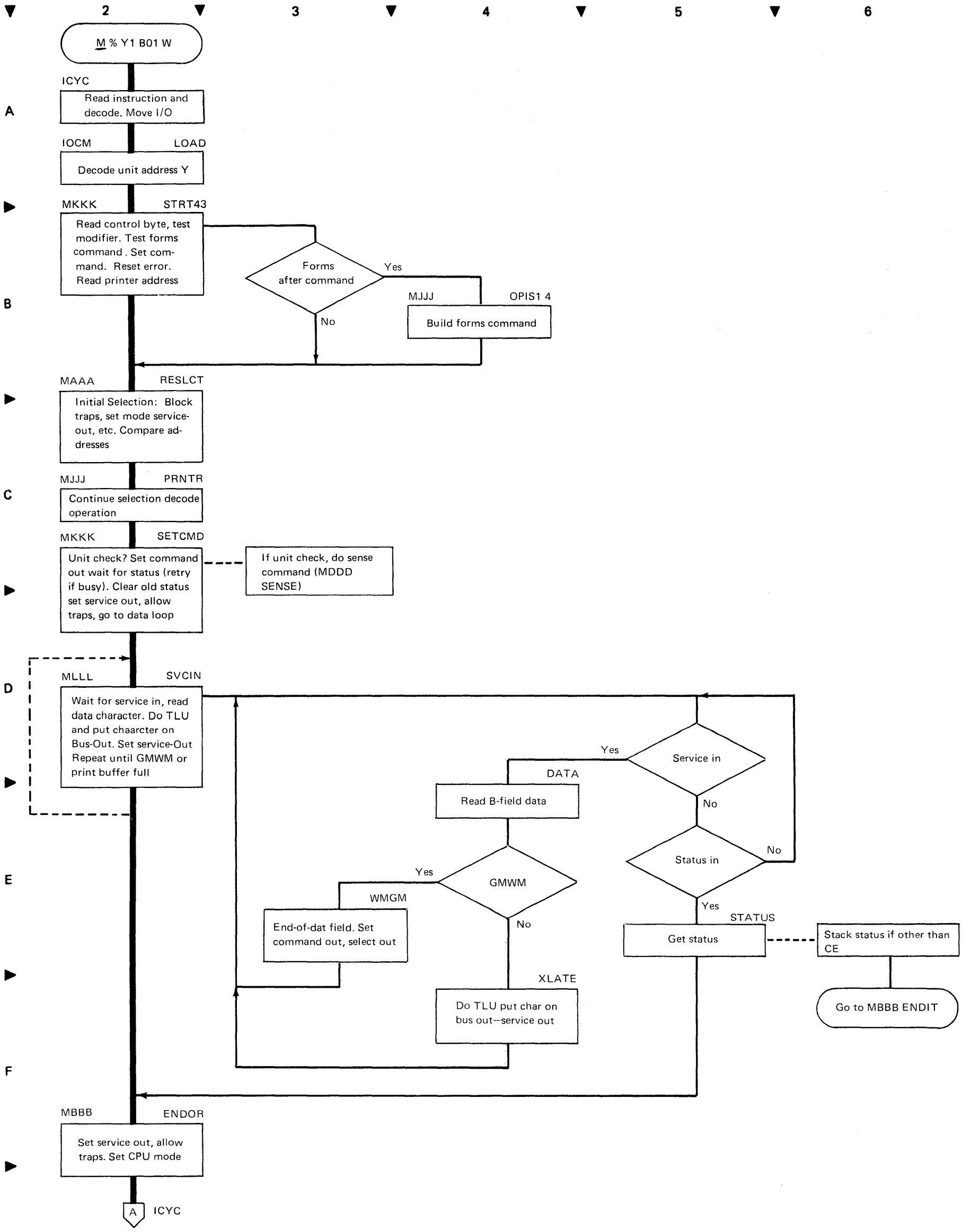


Diagram 5-729. 1400 Compatibility, 1442 Punch

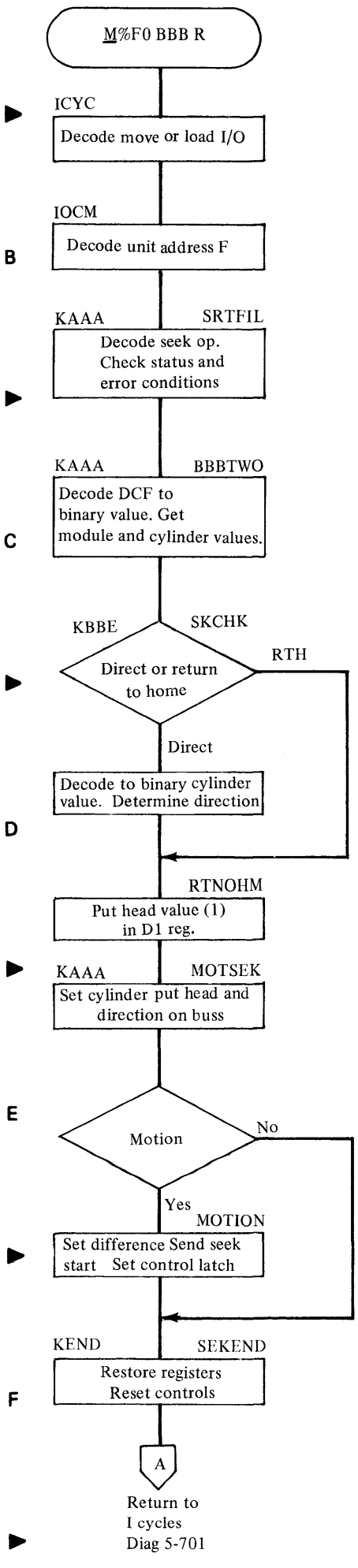


● Diagram 5-733. 1400 Compatibility–1443 Print

▼ 2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Seek
Return to home & direct

Objectives:
Decode the disk control field for module and cylinder values
Determine direction of seek motion (if direct seek) set head and direction; seek start.



Return to
I cycles
Diag 5-701

G

H

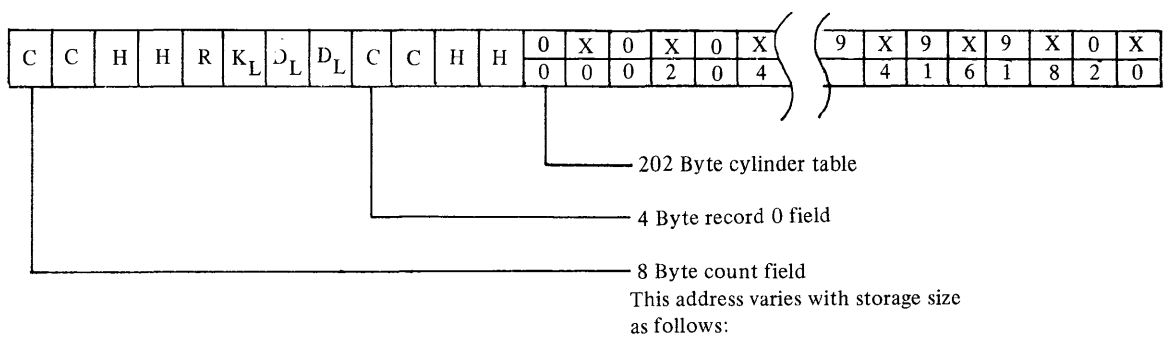
Miscellaneous disk file information

Auxiliary storage module 0

K0	K1	K2	K3	K4	K5	K6	K7
88	8A	8C	8E Work Area Count Field Address	98 Work Area File Data Address	9A Work Area Zone to zone transfer 9B Present selected module	9C	9E
89	8B	8D				9D	9F

K8	K9	KA	KB	KC	KD	KE	KF
A8	AA	AC	AE Previous file operation	B8	BA	BC Work Area Present DCF mod value	BE Work Word Area count 2980 100 move
Scan cond 0 = Hi 1 = Uneq 2 = Lo 3 = Eq	AB	AD	0 = RBC Inlk 1 = Recal seq 2 = X 3 = \ 4 = W 5 = Y 6 = V 7 = N	B9	BB	BD Present cylinder value	BF 2982 90 Load

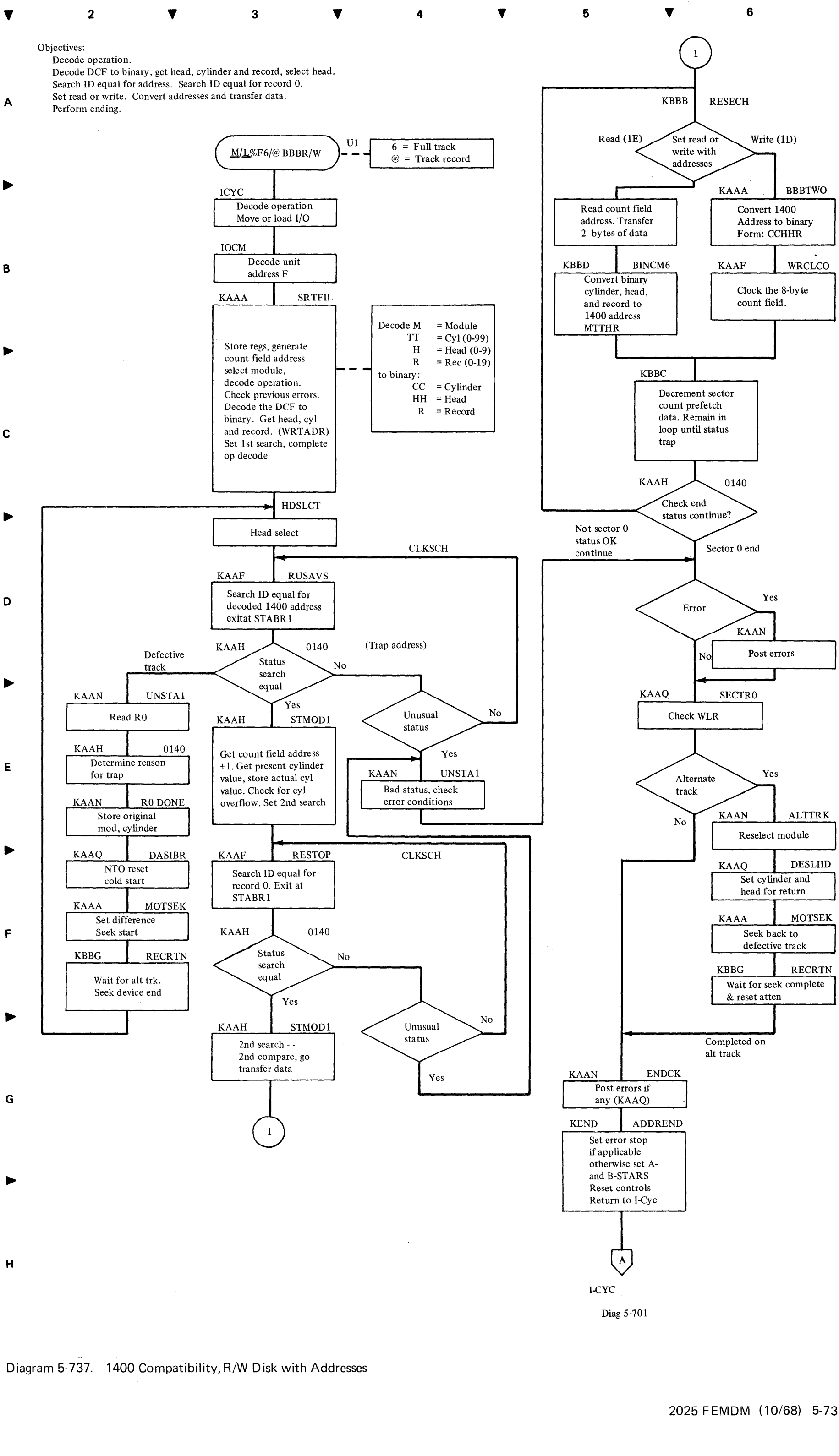
Program storage positions reserved for file tables



1400 \ 25	16,384	24,576	32,768	49,152
16K	0000	2000	4000	8000
12K	1000	3000	5000	9000
8K	1F00	3F00	5F00	9F00
4K	2F00	4F00	6F00	AF00
2K	3700	5700	7700	B700
1.4K	3900	5900	7900	B900

● Diagram 5-735. 1400 Compatibility, Seek Disk

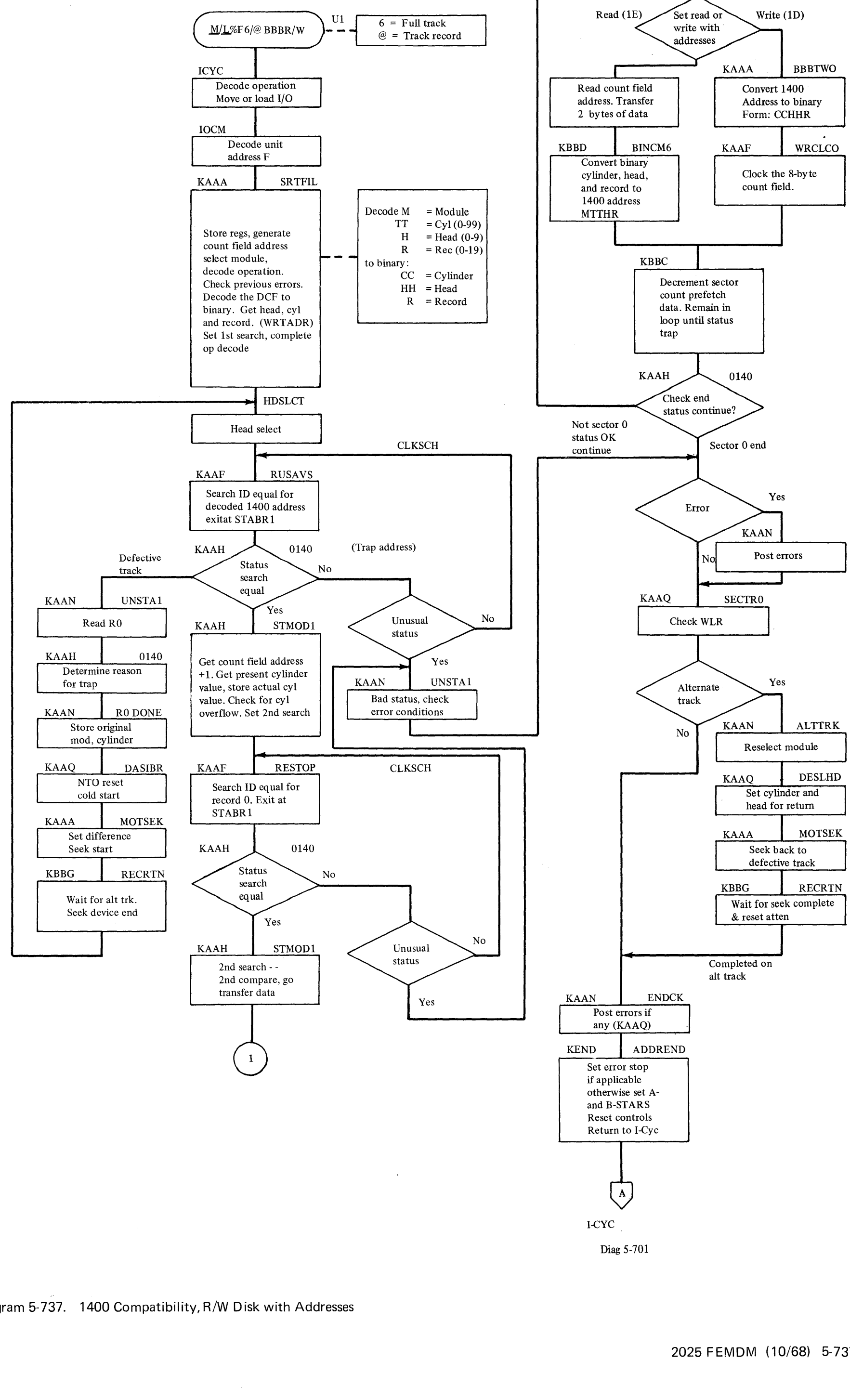
Objectives:
Decode operation.
Decode DCF to binary, get head, cylinder and record, select head.
Search ID equal for address. Search ID equal for record 0.
Set read or write. Convert addresses and transfer data.
Perform ending.



Diag 5-701

Diagram 5-737. 1400 Compatibility, R/W Disk with Addresses

Objectives:
Decode operation.
Decode DCF to binary, get head, cylinder and record, select head.
Search ID equal for address. Search ID equal for record 0.
Set read or write. Convert addresses and transfer data.
Perform ending.



Diag 5-701

Diagram 5-737. 1400 Compatibility, R/W Disk with Addresses

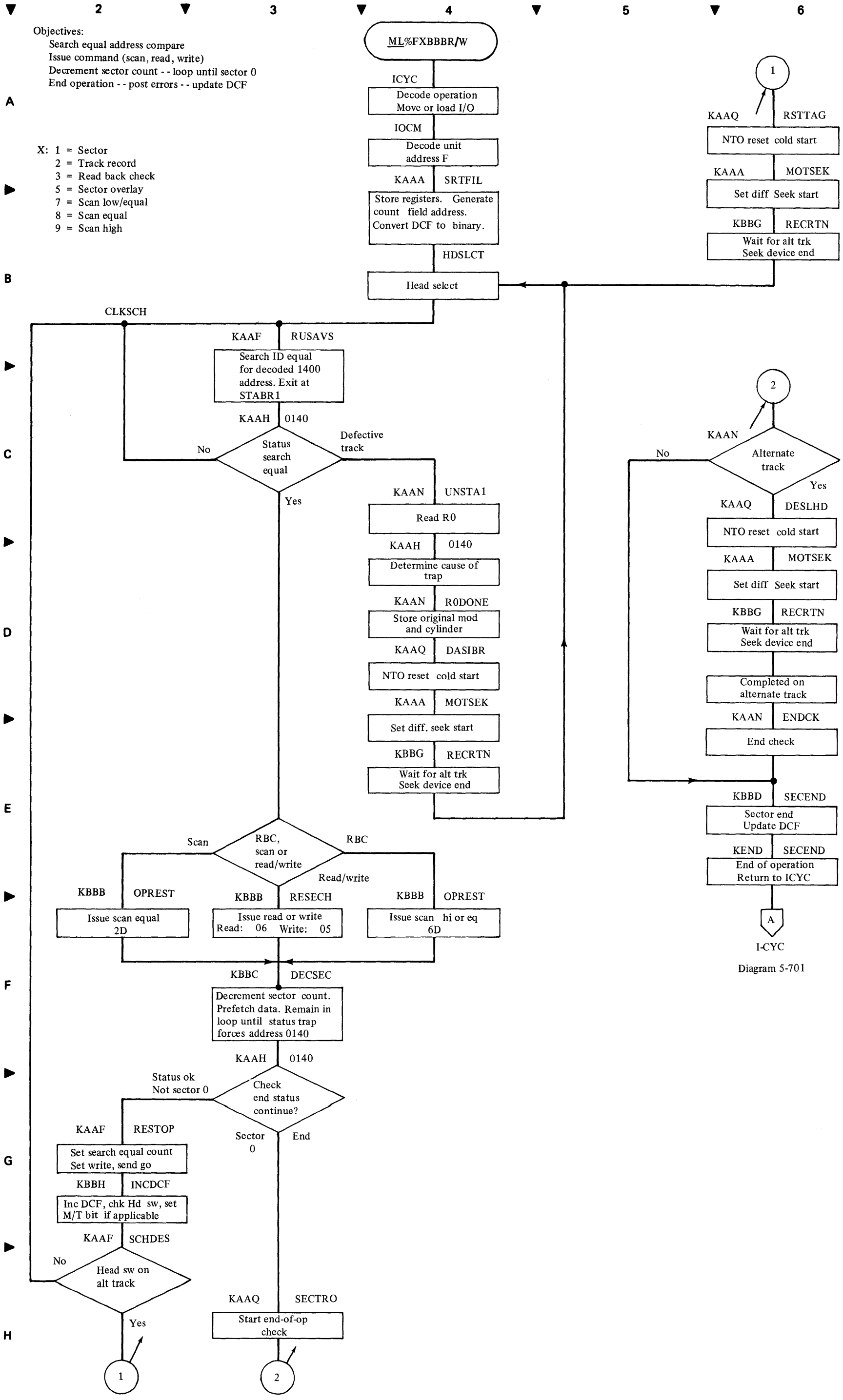


Diagram 5-701

Diagram 5-739. 1400 Compatibility R/W Disk Sector Mode

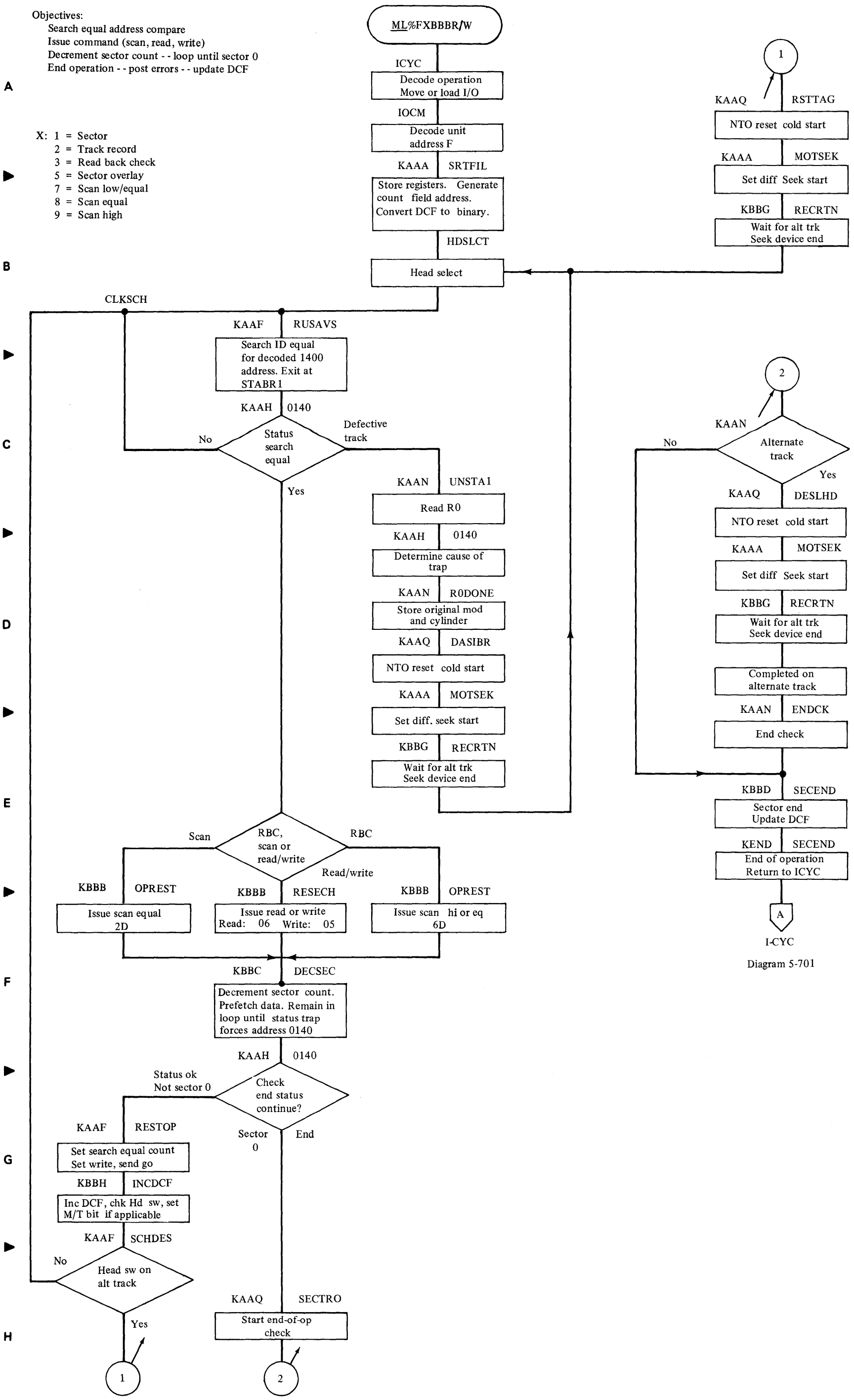
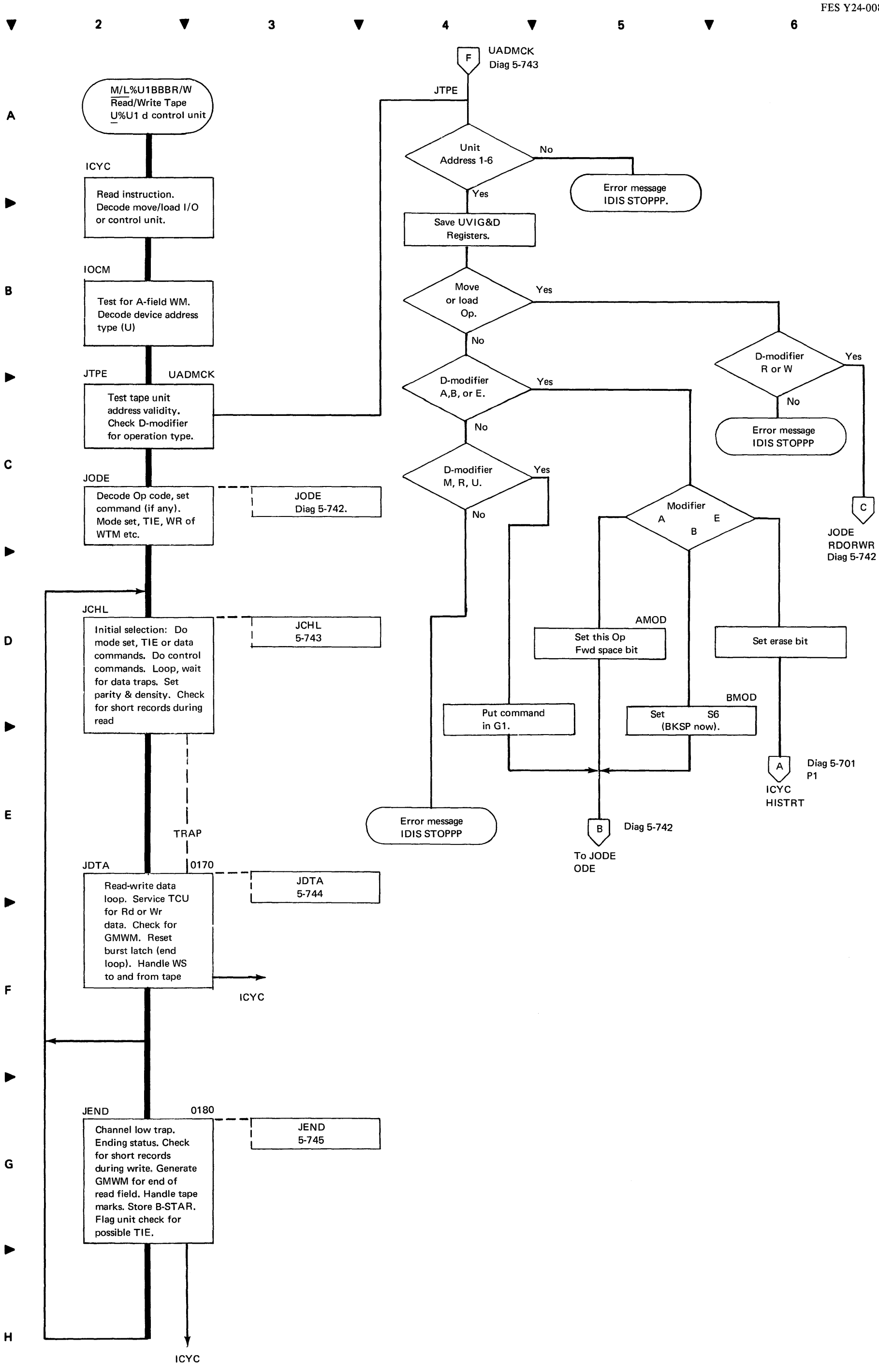
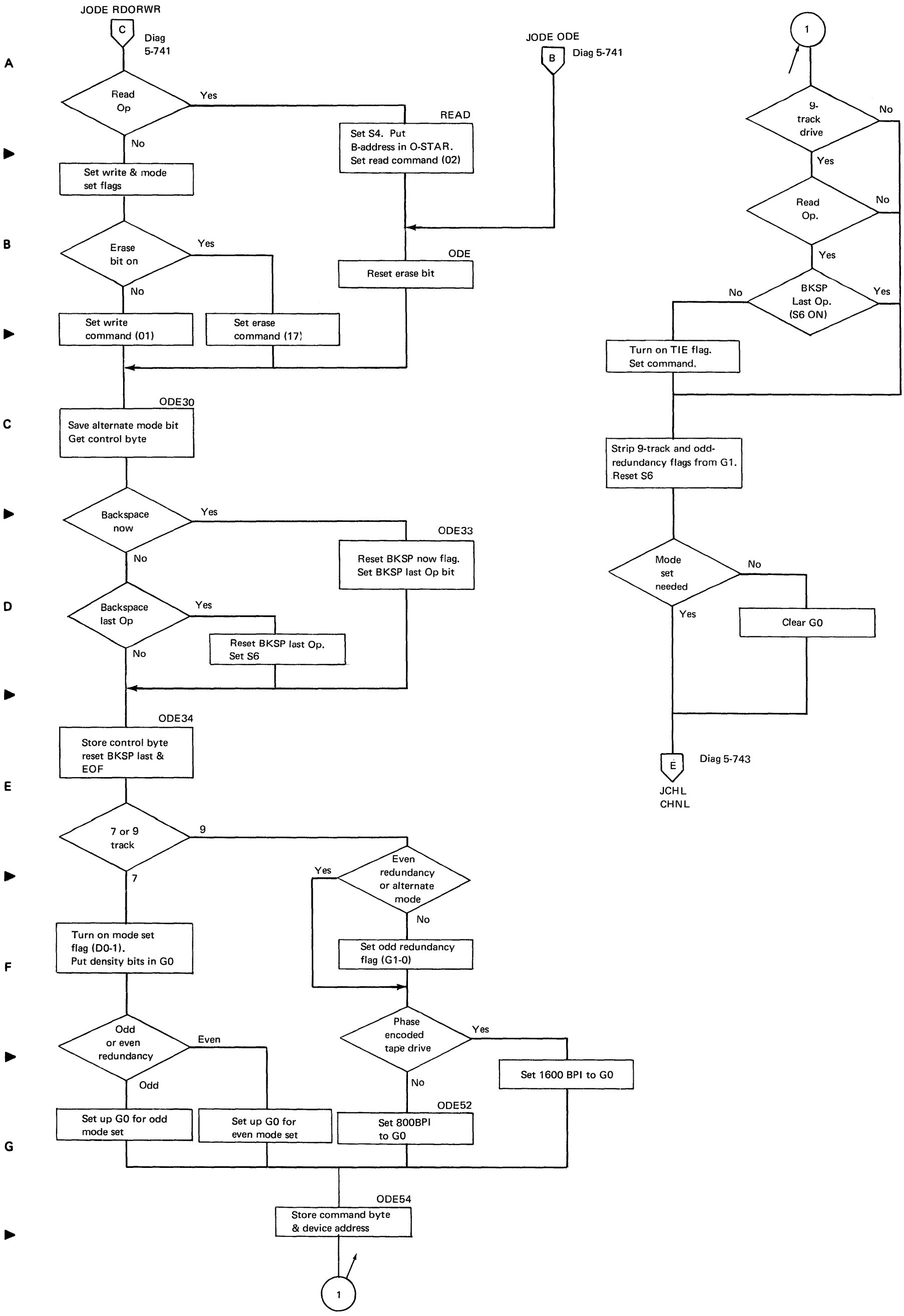


Diagram 5-701

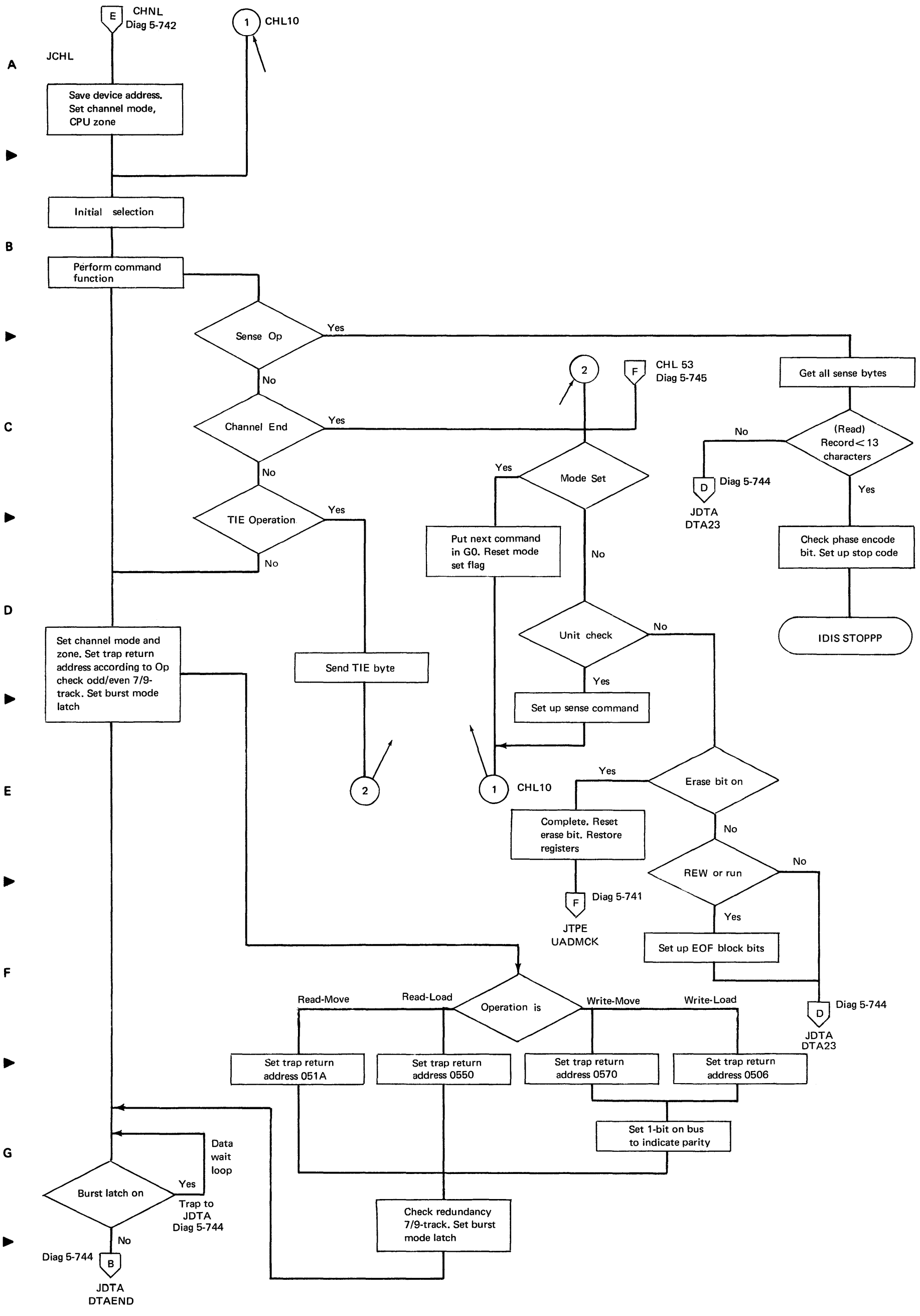
Diagram 5-739. 1400 Compatibility R/W Disk Sector Mode



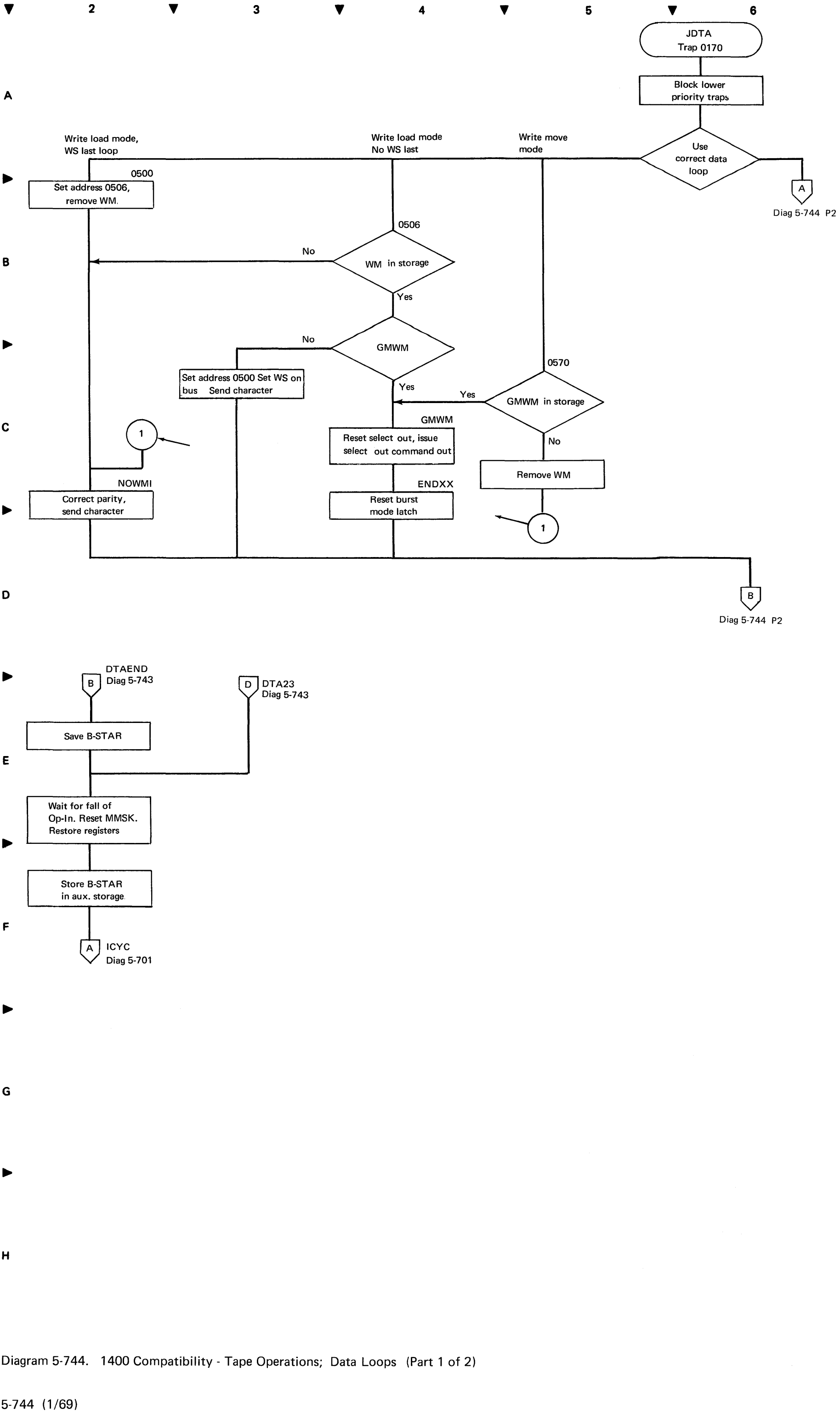
● Diagram 5-741. 1400 Compatibility - Tape Operations; General



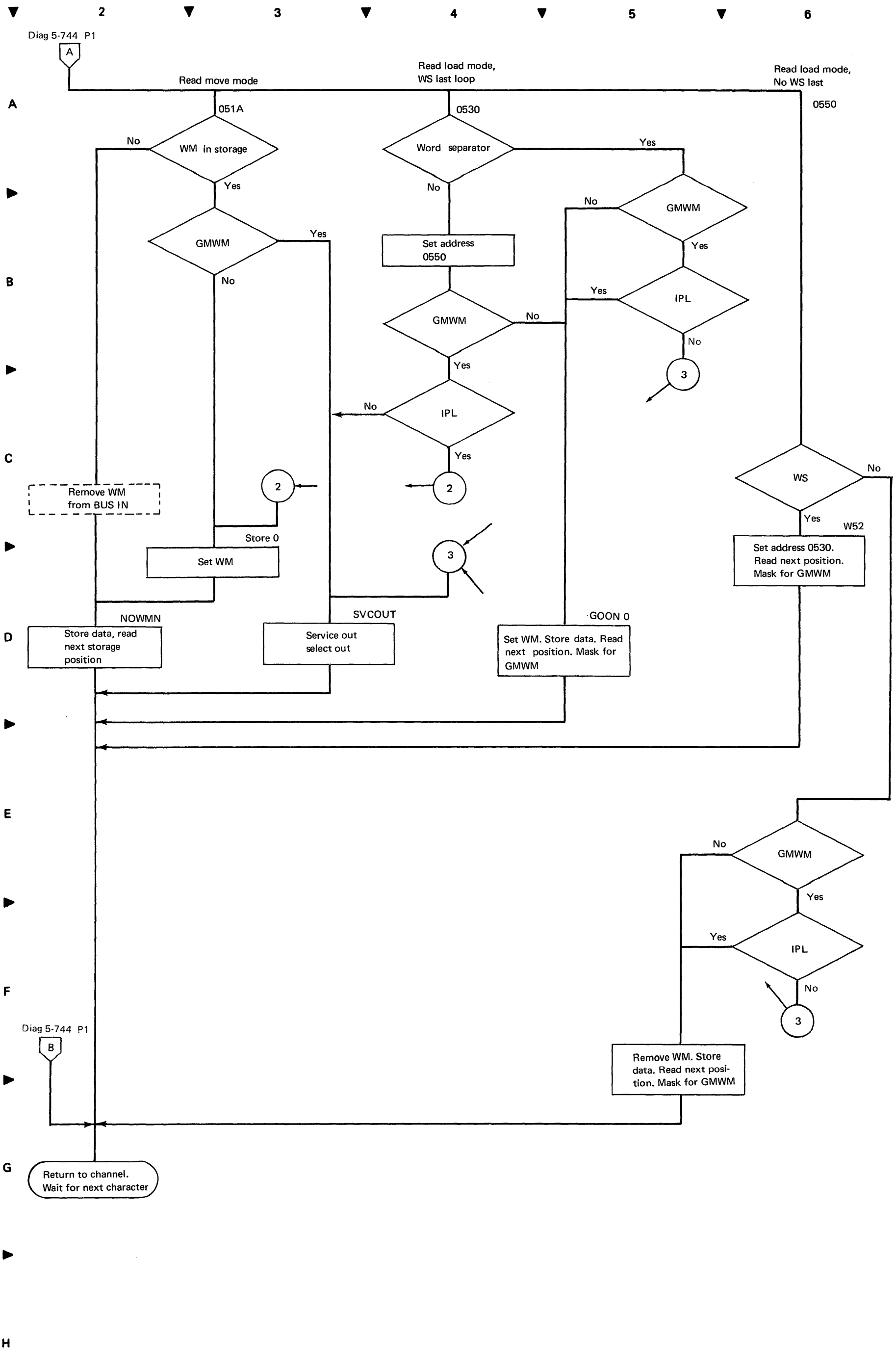
● Diagram 5-742. 1400 Compatibility - Tape Operations; Op Code Decode



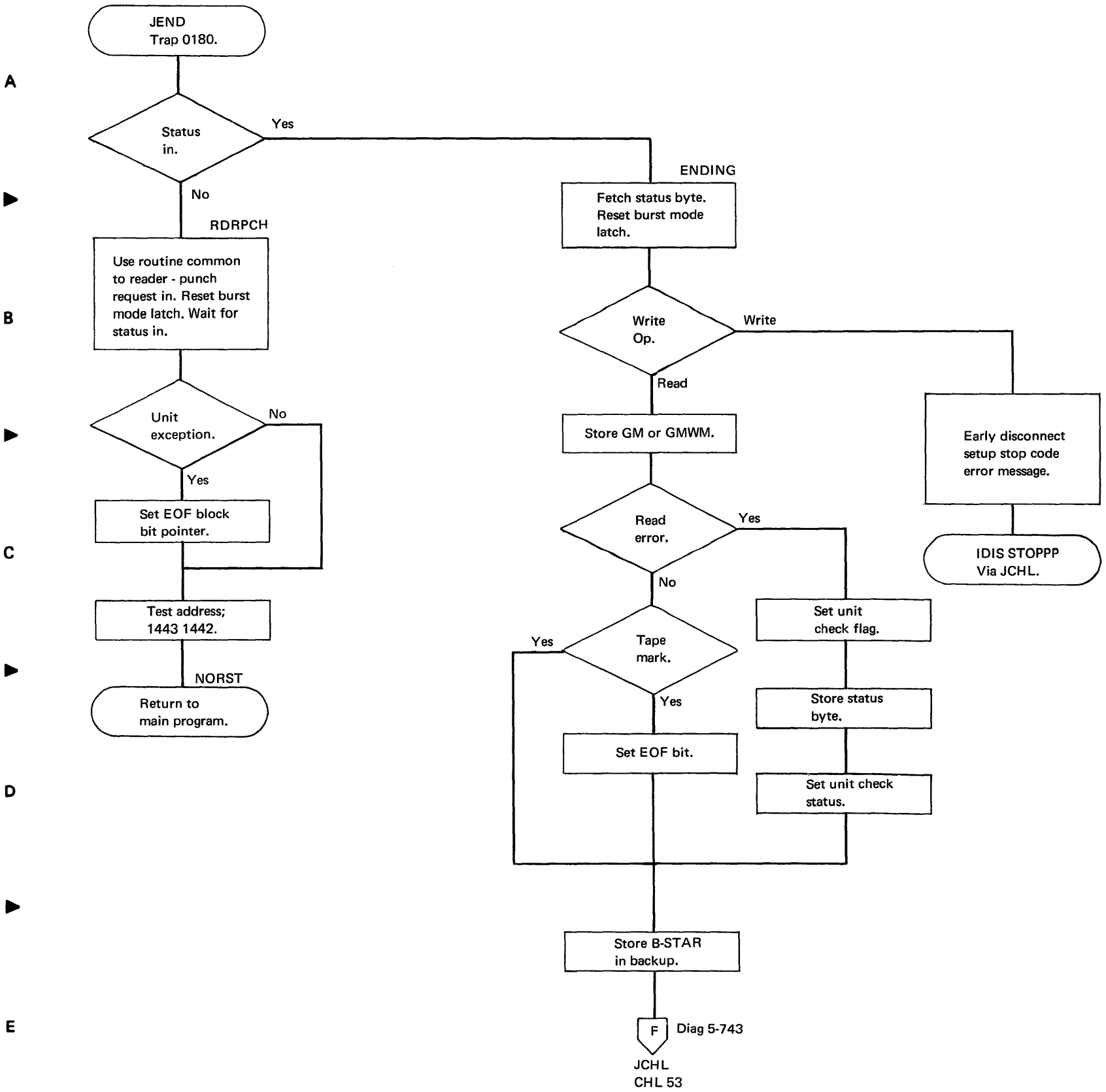
● Diagram 5-743. 1400 Compatibility - Tape Operations; Channel



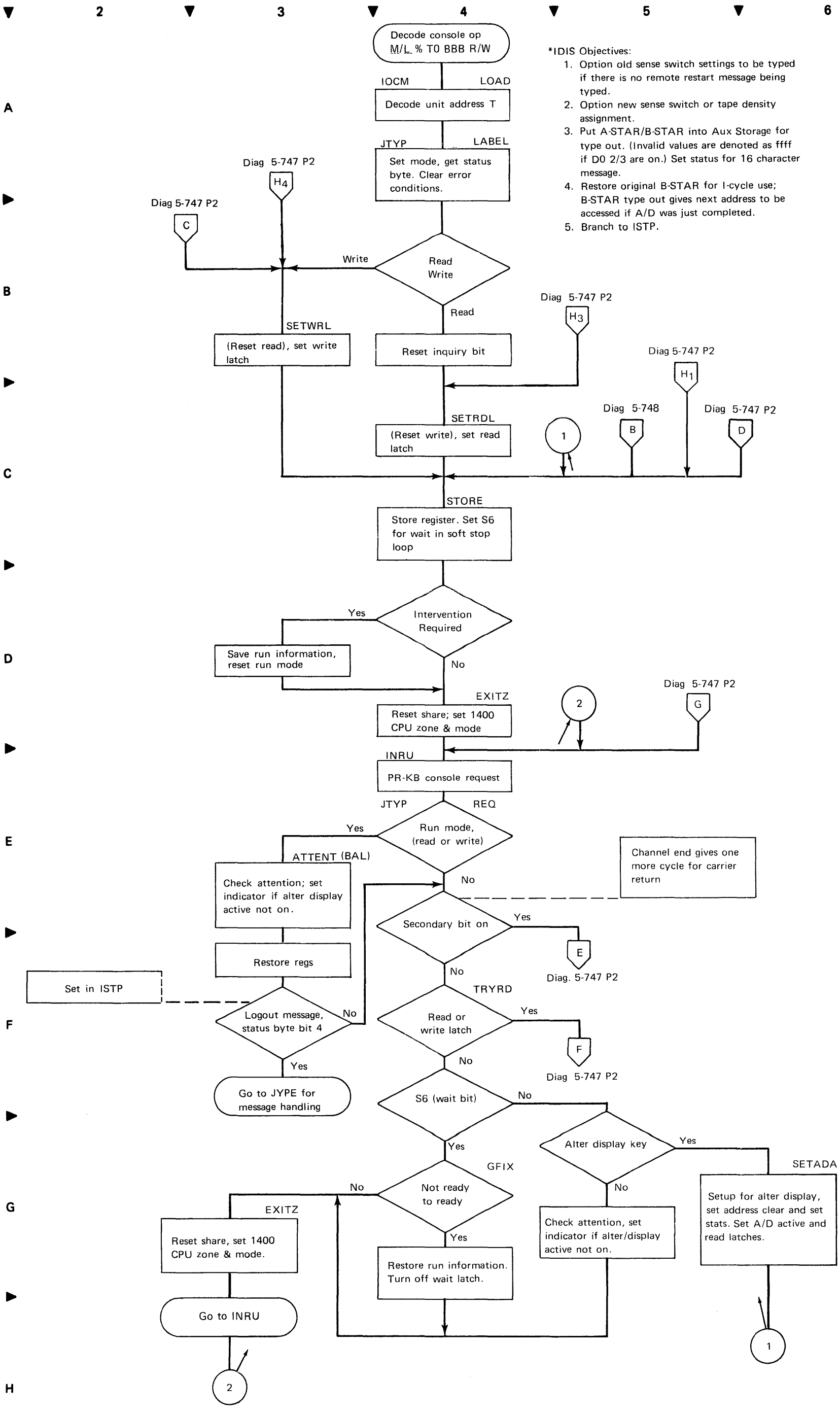
● Diagram 5-744. 1400 Compatibility - Tape Operations; Data Loops (Part 1 of 2)



● Diagram 5-744. 1400 Compatibility - Tape Operations; Data Loops (Part 2 of 2)



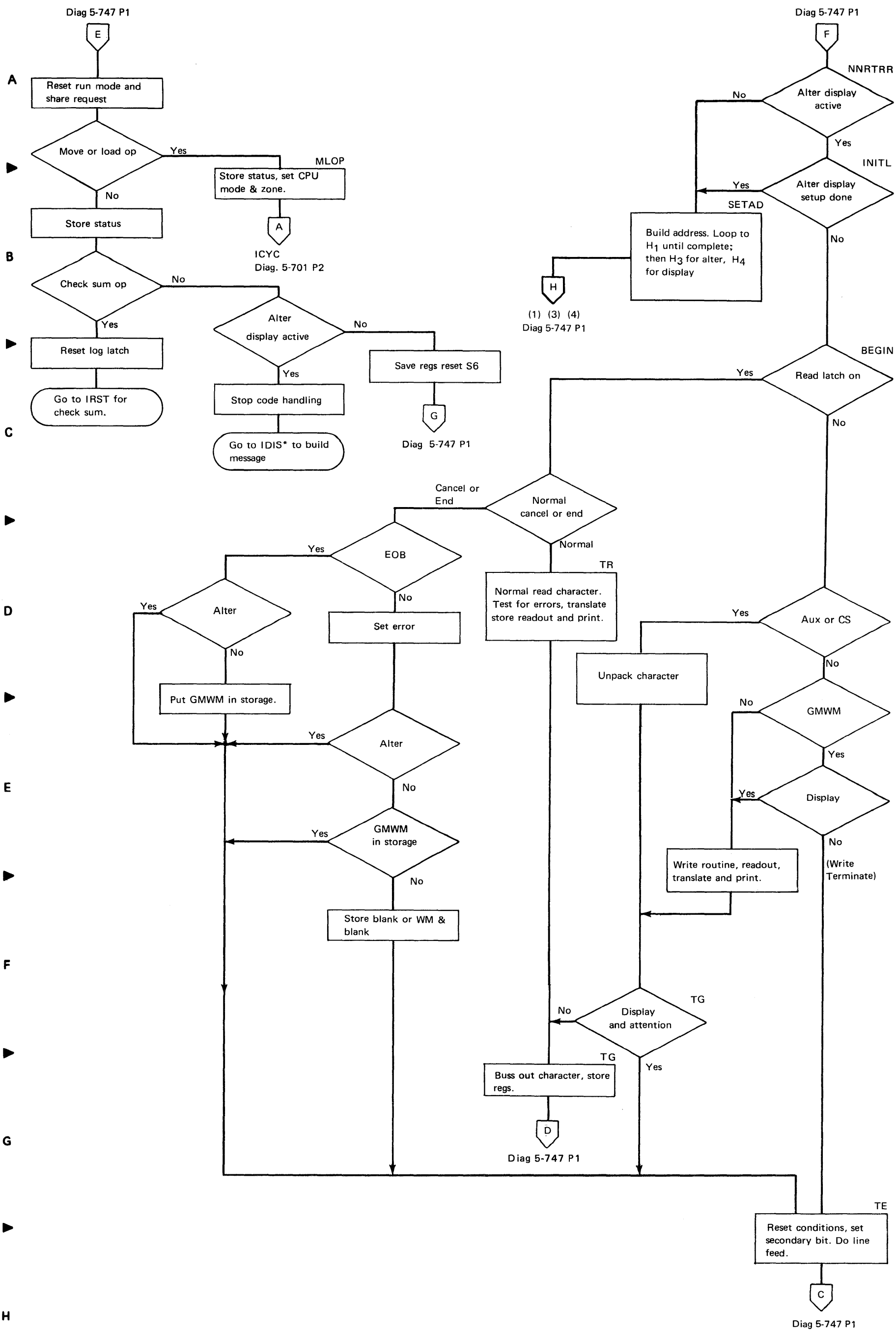
● Diagram 5-745. 1400 Compatibility - Tape Operations; Ending



*IDIS Objectives:

1. Option old sense switch settings to be typed if there is no remote restart message being typed.
2. Option new sense switch or tape density assignment.
3. Put A-STAR/B-STAR into Aux Storage for type out. (Invalid values are denoted as ffff if D0 2/3 are on.) Set status for 16 character message.
4. Restore original B-STAR for I-cycle use; B-STAR type out gives next address to be accessed if A/D was just completed.
5. Branch to ISTP.

● Diagram 5-747. 1400 Compatibility–PR-KB Share Request Handling Routine (Part 1 of 2)



● Diagram 5-747. 1400 Compatibility–PR-KB Share Request Handling Routine (Part 2 of 2)

2 3 4 5 6

From JTYP 1052 request

JYPE LABEL

A Message logout after stats set in ISTP

Initial stats:
H1=00
P0=14
S5=0
T&G=Unpacked halfword to be typed

*ISTP Objectives:
1. Provide input for instruction step operation (4 character).
2. Provide typeout of set IC value (8 character).
3. Enter at STOPCD (from IDIS) for 16 character message.
4. Unpack half-words from H-register to T&G registers.
5. Set layout stat to use JYPE (instead of JTYP) when PR-KB request is honored.

Line feed set up (P0 7=1)? No / Yes

B Need space S4=1? CKEND Yes / No

Space desired, issue space, make P0 even — SPACE

Set IC Op? Yes / No GETAUX

(16-character message is output)

C D0 bit 5=1? No / Yes

4 or 8-character message; don't set S4

16-character message, set S4

D Issue line feed — LINEFD

B

Diag 5-747

Bit 7=1 Bit 6=1? Third / Bit 7=1 (First) / Bit 6=1 (2nd)

Fetch B-STAR, reset D0 6

Fetch A-STAR. Reset D0 7 — ASTAR

Fetch coded byte from "BE". Reset S4

E Remote restart capability? No / Yes

Set soft stop

Unpack S5=1? No / Yes CKUNPK

Reset S5 go to ISTP

*ISTP TYPEAG

Unpack H-reg into T&G regs. Return to JTYP STORE

B

Diag 5-747

8-character message

I-STAR in H. Reset D0 7

Put information into H-reg. (Unpack is from H).

NEXT

Set S0, S5.

H1 bit 7? No / Yes SECOND

Buss out 1st/3rd character. Set H1 bit 7 for 2nd character

Bus out 2nd/4th character

S0=0? No / Yes

Move G to T. Reset S0

H1 switch

F S4 on? EXIT No / Yes MORE

Build space

Change P0 to allow CKEND next time

G To JTYP to store registers. To INRU, wait for request

As long as S4 is on, another halfword will be accessed and unpacked for typing

H

Diagram 5-748. 1400 Compatibility–PR-KB Display Messages

IBM FE Supplement

System: System/360 Model 25

Re: Form No. Y24-3529-0

This Supplement No. Y24-0506

Date: June 12, 1969

Previous Supplement No. Y24-0086
Y24-0094
Y24-0503

LOGIC DIAGRAMS AND OPERATIONAL DIAGRAMS FOR THE SYSTEM/360 MODEL 25, INTEGRATED COMMUNICATIONS ATTACHMENT FEATURE

This supplement adds new diagrams to the Field Engineering Maintenance Diagram Manual, 2025 Processing Unit, Form Y24-3529-0. Diagrams to be inserted and/or removed are listed below.

iii, iv
v
vii, viii (added due
ix, x to change
xi, xii in layout)
1-1 (9 parts), 1-3
3-11, 3-12 (added)
4-500 through 591 (added)
5-500 through 514 (added)

A change to the text or a small change to an illustration is indicated by a vertical line to the left of the change; a changed or added illustration is denoted by the symbol ● to the left of the caption.

Summary of Amendments.

This supplement provides logic diagrams, operational diagrams, and revised diagnostic strategy diagrams for the Integrated Communications Attachment. Front matter pages (pages numbered with roman numerals) are included because of re-layout. Parts 4 and 9 of diagram 1-1 are included because of the addition of technical information. The remaining parts of diagram 1-1 are included because of re-layout and do not reflect any technical changes.

File this cover letter at the back of the manual to provide a record of the changes.

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IBM FE Supplement

System: System/360 Model 25

Re: Form No. Y24-3529-0

This Supplement No. Y24-0503

Date: March 25, 1969

Previous Supplement No. Y24-0086
Y24-0094

LOGIC DIAGRAMS AND OPERATIONAL DIAGRAMS FOR SYSTEM/360 MODEL 25, INTEGRATED 2560 ATTACHMENT

This supplement adds new diagrams to the Field Engineering Maintenance Diagram Manual, 2025 Processing Unit, Form Y24-3529-0.

List of diagrams to be inserted and/or removed.

iii, iv
4-213, 4-301
4-651 through 4-695 (added)
5-203
5-651 through 5-675 (added)
5-709
5-721, 5-722
5-723
5-725, 5-727
5-735
5-747 (Part 1)

A change to the text is indicated by a vertical line to the left of the change; added illustrations are denoted by the symbol ● to the left of the caption.

Summary of Amendments.

Logic diagrams for System/360 Model 25 Integrated 2560 Attachment are added.

Operational diagrams for System/360 Model 25 Integrated 2560 Attachment are added.

Operational diagrams for System/360 Model 25 1400 Compatibility Feature are included in this supplement to correct the numerical sequence in supplement number Y24-0094.

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System System/360 Model 25

Re: Form No. Y24-3529-0

This Supplement No. Y24-0094

Date: February 28, 1969

Previous Supplement No. Y24-0086

This supplement provides replacement pages for the 2025 Processing Unit, Field Engineering Maintenance Diagram Manual, Form Y24-3529-0.

List of pages to be inserted and/or removed.

ii
iii, iv
4-200 through 4-213
5-301 through 5-307 (added)
5-709 (added)
5-722 (added)
5-727 (added)
5-733 (added)
5-747 (added)
5-748 (added)

A change to the text or a small change to an illustration is indicated by a vertical line to the left of the change; a changed or added diagram is denoted by the symbol ● next to the caption or folio.

Summary of Amendments.

Logic diagrams for the Integrated 1403 Attachment have been updated to reflect 1403 Model N1 capability.

Operational diagrams for the Integrated 2311 Attachment are added.

Additional operational diagrams for the 1400 Compatibility feature are added.

File this cover letter at the back of the manual to provide a record of changes.

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IBM **FE Supplement**

System System/360 Model 25

Re: Form No. Y24-3529-0

This Supplement No. Y24-0086

Date: January 20, 1969

Previous Supplement No. None

OPERATIONAL DIAGRAMS FOR SYSTEM/360 MODEL 20 MODE FEATURE AND 1400 COMPATIBILITY TAPE OPERATIONS.

This supplement replaces diagrams in the Field Engineering Maintenance Diagram Manual, 2025 Processing Unit, Form Y24-3529-0.

List of diagrams to be inserted and/or removed.

iii, iv
1-1 through 1-300 (Category 1 replaced entirely)
5-600 through 5-640 (added)
5-721, 5-723,
5-725, blank
5-741 through 5-745 (added)

A changed or added diagram is indicated by the symbol ● near the caption.

Summary of Amendments.

Category 1 is replaced entirely and includes the diagnostic techniques for the System/360 Model 20 Mode feature.

Operational diagrams for System/360 Model 20 Mode feature are added to Category 5.

Operational diagrams for 1400 Compatibility Tape Operations and 1403 Printer are also added to Category 5.

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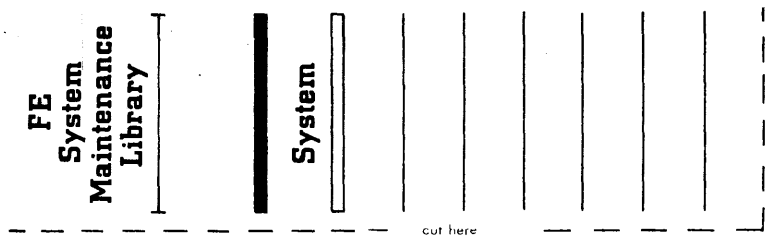

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