IBM Field Engineering Handbook

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System/360 Model 50

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Fourth Edition
This is a reprint of Form Z22-2855-2 incorporating changes released in FE Supplement Z22-6647 dated March 20, 1967.

Specifications contained herein are subject to change from time to time. Any such change will be reported in subsequent revisions or FE Supplements.

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CONTENTS (Cont'd)

MACHINE VOLTAGES PRESENT WITH POWER OFF OR WITH DC OFF

1.	208 vac	In the power control compartment On the contactor gate At the CE panel circuit breakers At the convenience outlet transformer
2.	115 vac	At the convenience outlet transformer At relays 49, 50, 51, and 52
3.	48 vdc	On the relay gate On the contactor gate On the CE panel On the 48v bus On all thermals On all power supply terminal board positions 7, 8, and 9
4.	24 vac	In the power control compartments On the relay gate On the contactor gate At the console emergency off switch

LIST OF MODEL 50 FE MANUALS

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S/360 Model 50 Comprehensive Introduction, FEMI	223-2821
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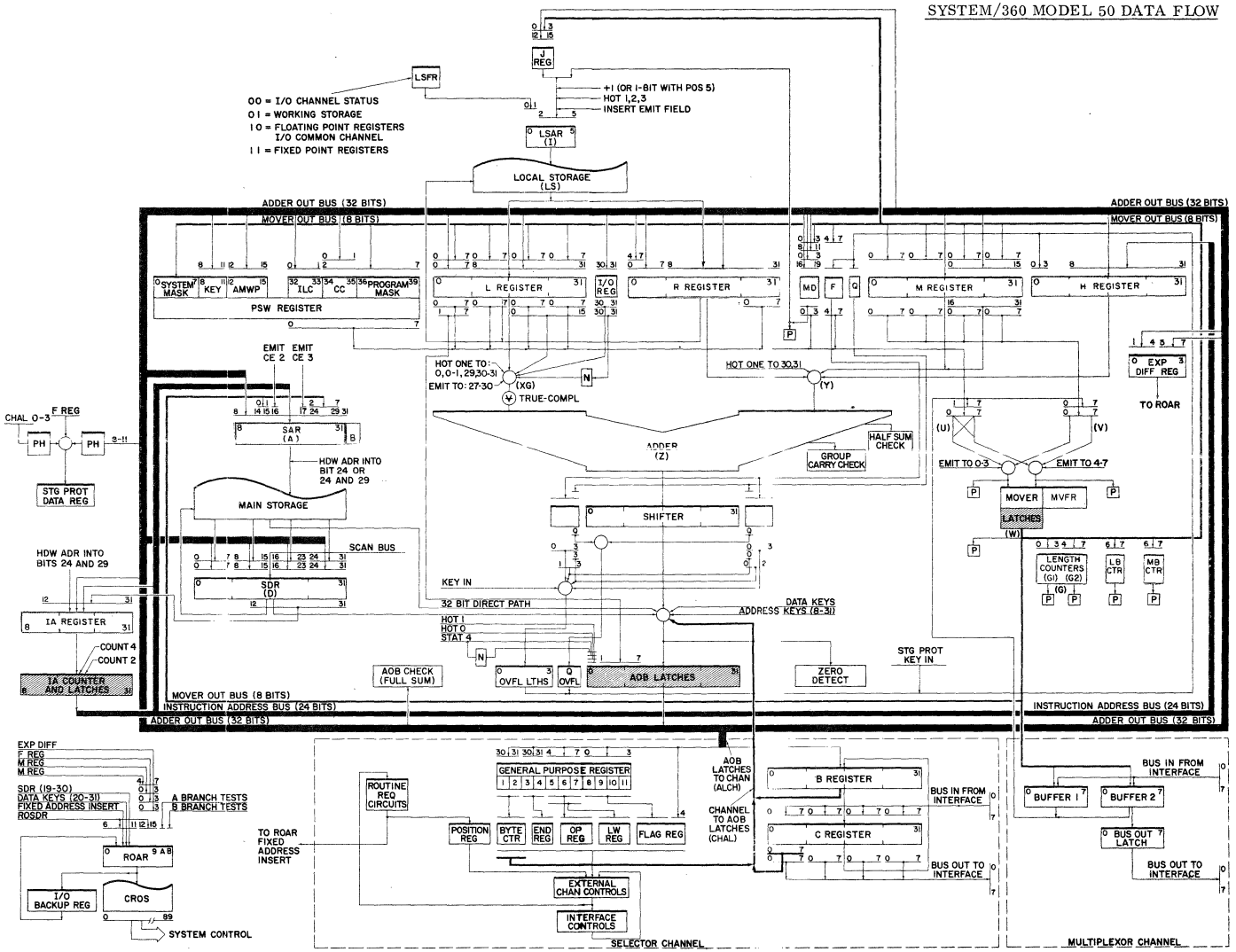
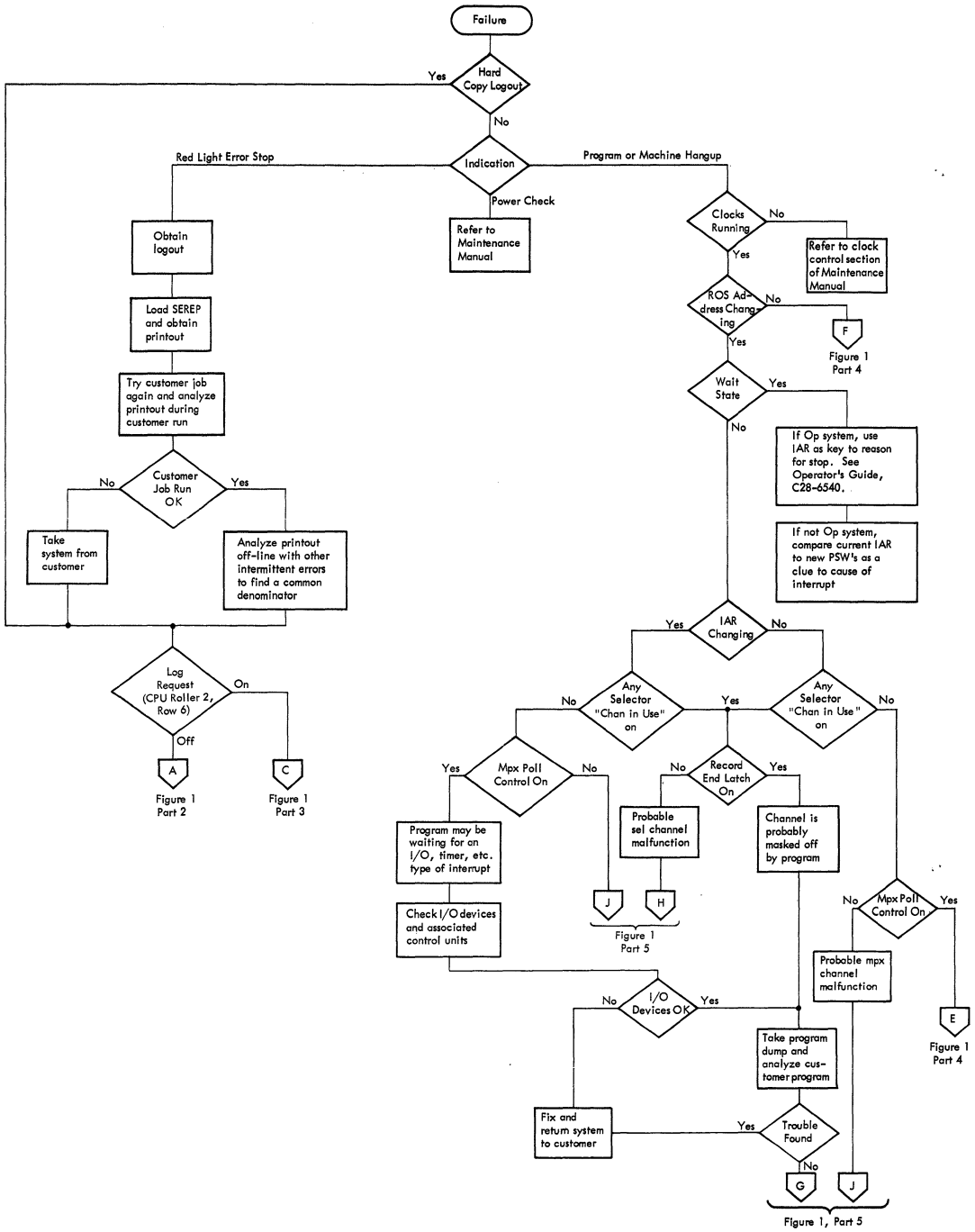
S/360 Model 50 7070/7074 Compatibility Feature, FETOM	Y22-2925

SYSTEM/360 MODEL 50 DATA FLOW



Form Z22-2855-2
FES 222-6647-0



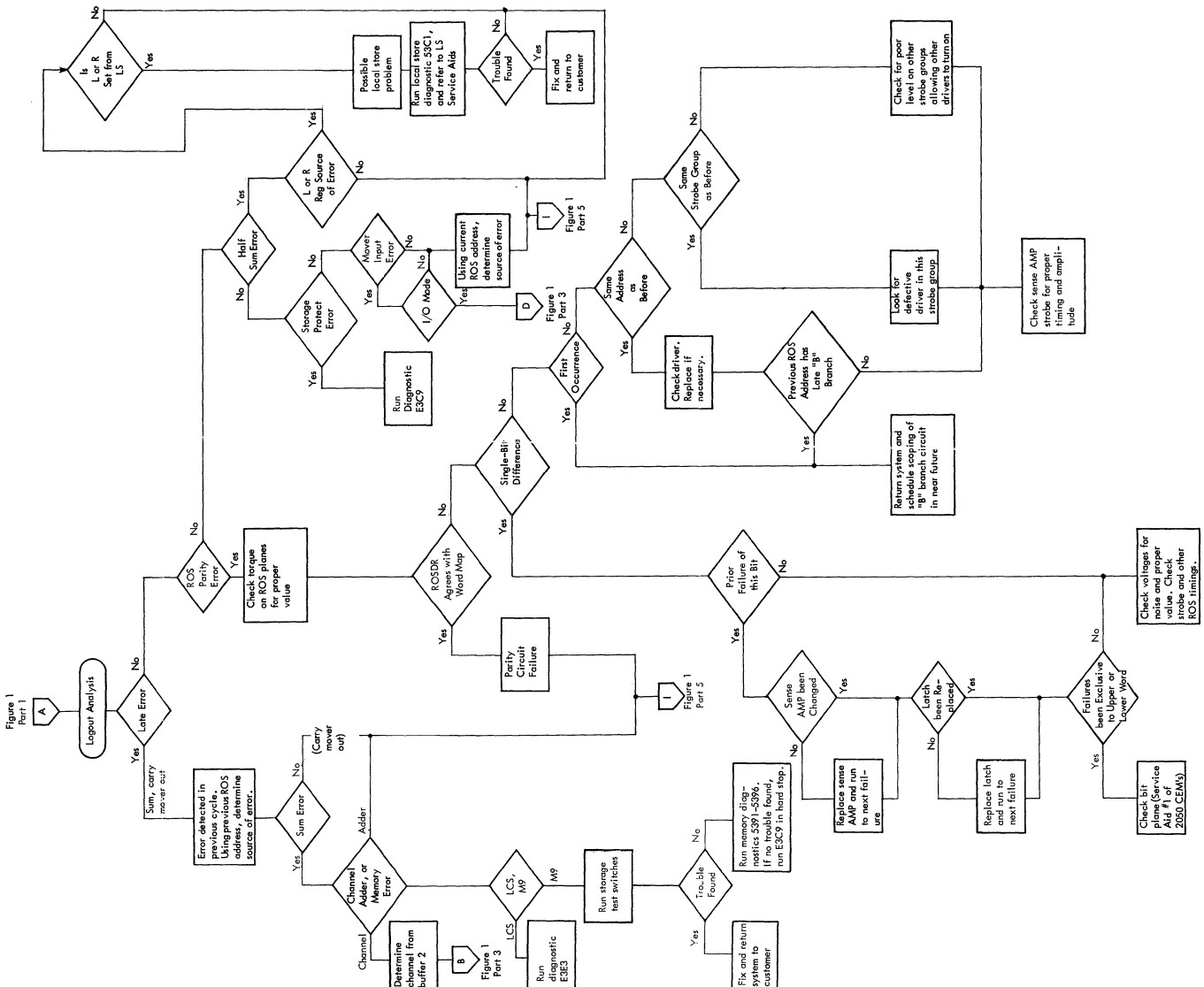
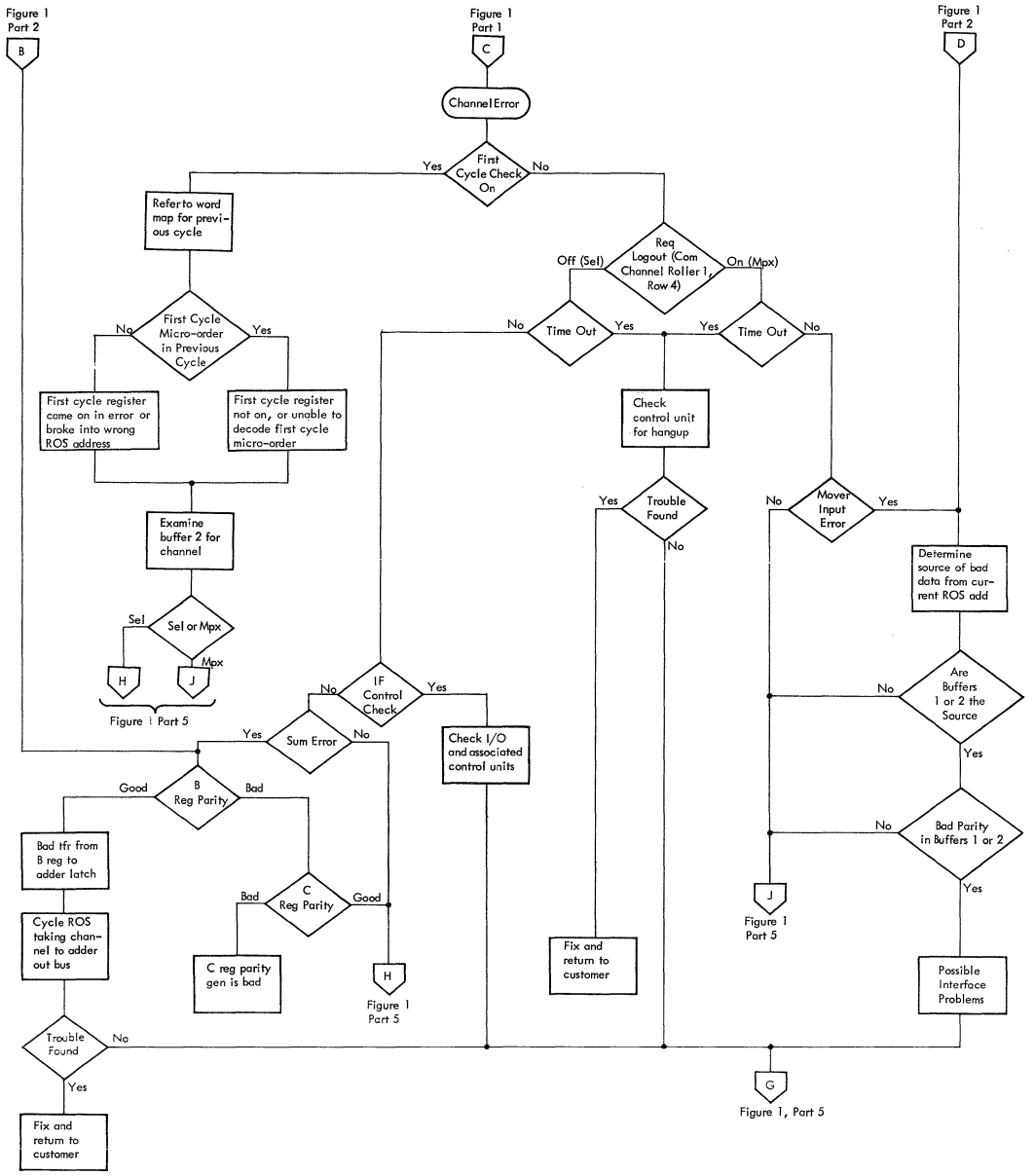
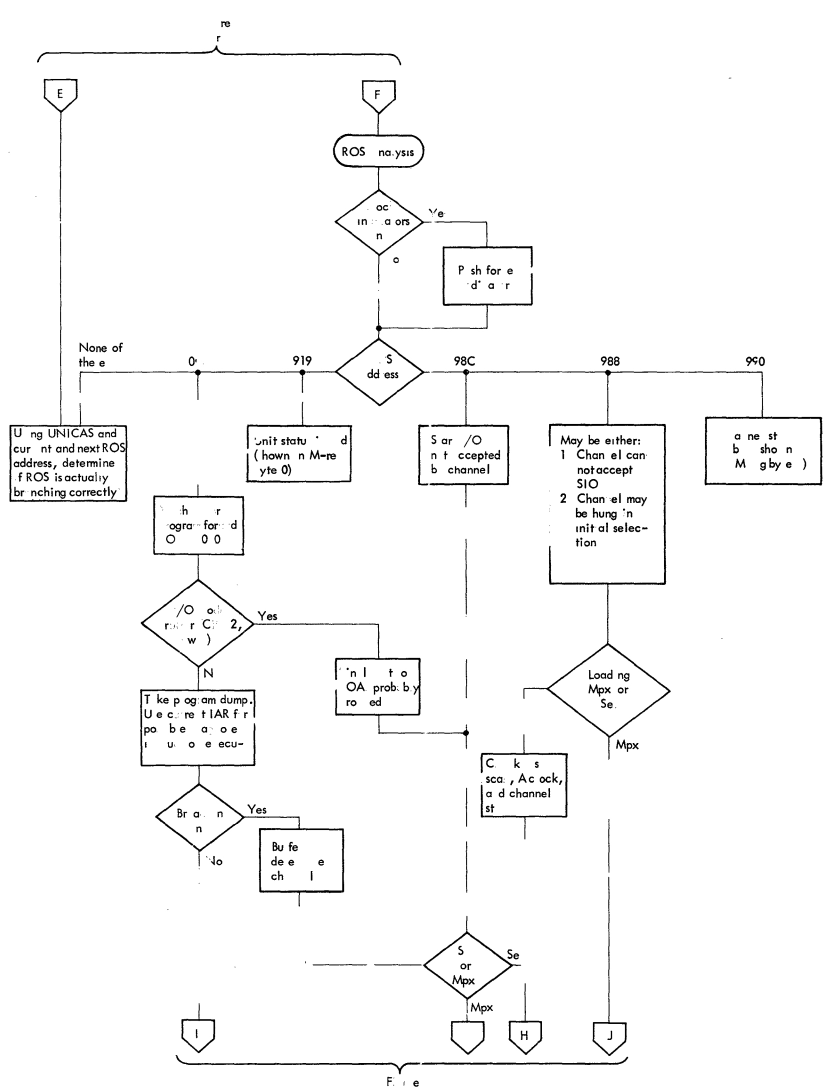


Figure 1 Part 1
A
Logout Analysis
Late Error
No
Yes
Sum, carry mower out
Error detected in previous cycle. Using previous ROS address, determine source of error.
Sum Error
No
Yes
(Carry mower out)
Adder
Channel Adder, or Memory Error
Channel
Determine channel from buffer 2
B
Figure 1 Part 3
LCS, M9
LCS
Run diagnostic E3E3
M9
Run storage test switches
Trouble Found
No
Yes
Run memory diagnostics 5391-5396. If no trouble found, run E3C9 in hard stop.
Fix and return system to customer
ROS Parity Error
No
Yes
Check torque on ROS planes for proper value
ROSDR Agrees with Word Map
No
Yes
Parity Circuit Failure
Figure 1 Part 5
Single-Bit Difference
No
Yes
Prior Failure of this Bit
No
Yes
Sense AMP been Changed
No
Yes
Replace sense AMP and run to next failure
Latch been Replaced
No
Yes
Replace latch and run to next failure
Failures been Exclusive to Upper or Lower Word
No
Yes
Check bit plane (Service Aid #1 of 2050 CEMs)
Check voltages for noise and proper value. Check strobe and other ROS timings.
First Occurrence
No
Yes
Previous ROS Address has Late "B" Branch
No
Yes
Return system and schedule scoping of "B" branch circuit in near future
Same Address as Before
No
Yes
Check driver, Replace if necessary.
Same Strobe Group as Before
No
Yes
Look for defective driver in this strobe group
Check for poor level on other strobe groups allowing other drivers to turn on
Check sense AMP strobe for proper timing and amplitude
Figure 1 Part 3
D
Mover Input Error
No
Yes
I/O Mode
No
Yes
Using current ROS address, determine source of error
Storage Protect Error
No
Yes
Run Diagnostic E3C9
Half Sum Error
No
Yes
L or R Reg Source of Error
No
Yes
Figure 1 Part 5
Is L or R Set from L5
No
Yes
Possible local store problem
Run local store diagnostic 53C1, and refer to L5 Service Aids
Trouble Found
No
Yes
Fix and return to customer



Form 122-2855-2
FES 222-6647-0

Form Z22 2855 2
FES Z22-6647-0



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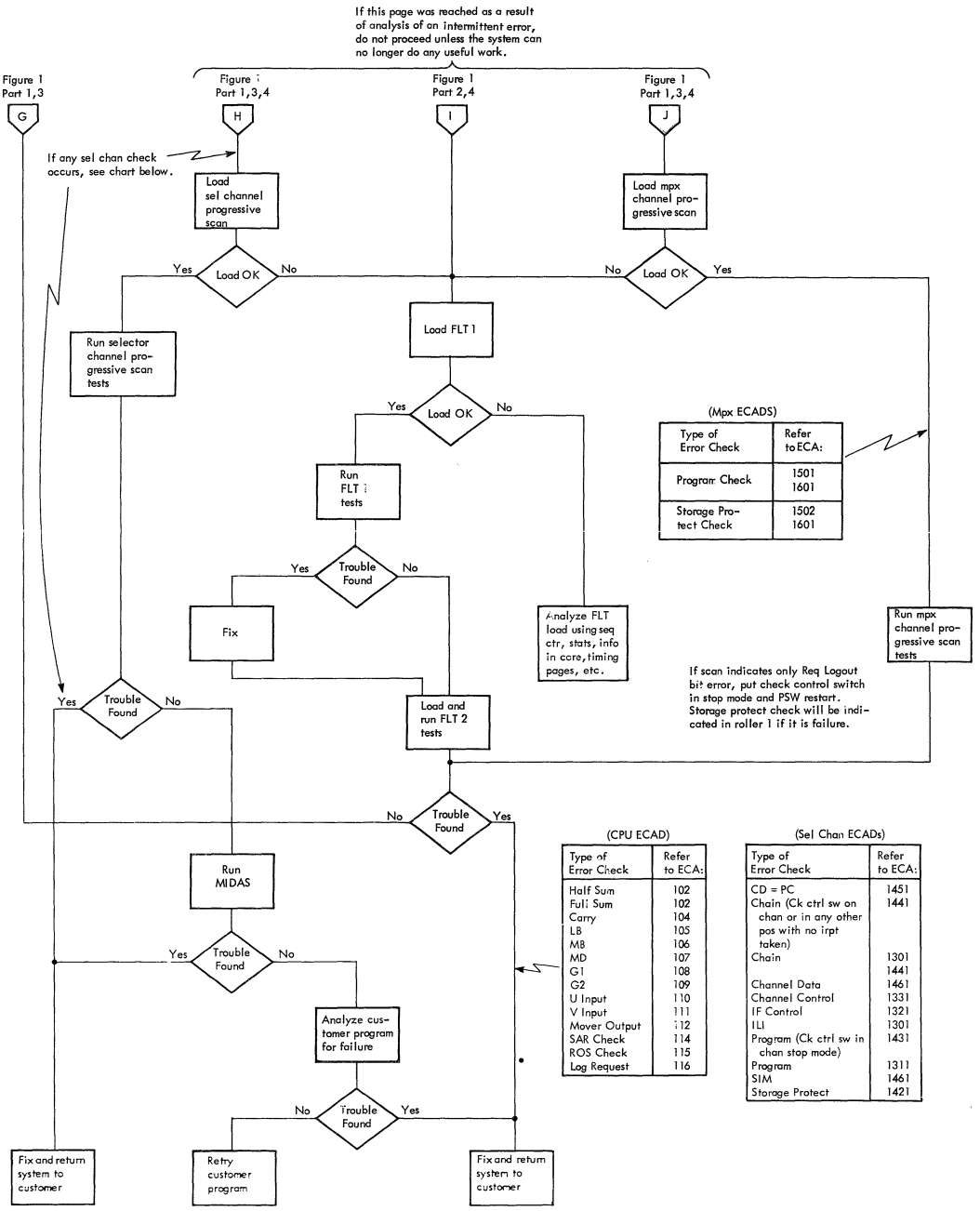


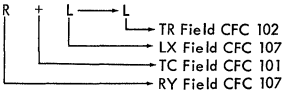
ALD PAGE INDEX (INCLUDING SELECTOR CHANNEL)

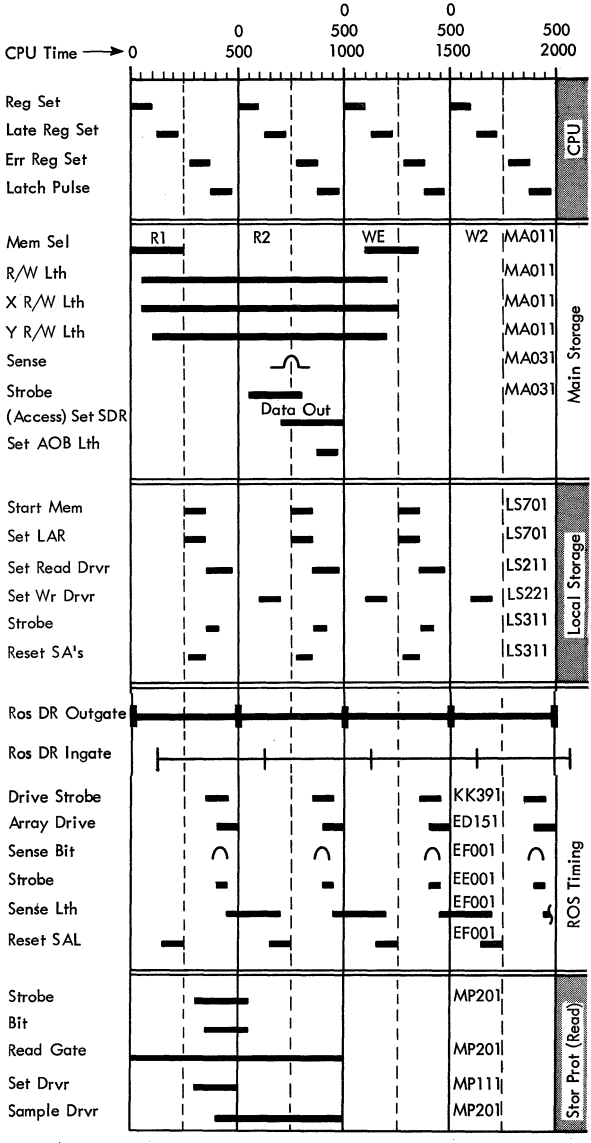
Edge Char	Format	Sym	Fld I/O	Fld CPU	Name	CFC Page CPU	CFC Page I/O
E	0000 [binary]		CE	CE	Control Emit Data	106	206
A	[RRR] ± [LLL]→[TTT]	R	RY	RY	Right Input to Adder [Y]	107	207
		±	TC*	TC*	True - Compliment Control	107	207
		L	LX	LX	Left Input to Adder [XC]	107	207
		T		TR	Adder Latch Destination	102	
	[UUUU] or [V→VVV→V]	U		AD*	Adder Function	107	
		V	AL	AL	Shift Gate and Adder Latch Control	104	204
	Hot 1		HC		Hot Carry to Adder		205
B	[GGG]→ U	G	LU	LU	Mover Input, Left Side [U]	101	201
	[BBB]→ V	B	MV	MV	Mover Input, Right Side [V]	101	201
	[CCC]→WL [DDD]→WR	C	UL*	UL*	Mover Action 0-3	106	206
		D	UR*	UR*	Mover Action 4-7	106	206
	W→[FFF] or W[FF]→[FFF]	F	WL	WM	Mover Output Destination	105	205
	SEMT		RY	RY	(Or SDR Parity Bits to CE Bits)	107	207
D	[AAAA]→[TTTT]	A	AL	AL	Shift Control and Adder Latch Ingate	104	204
		T	TR	TR	Adder Latch Destination	102	202
	[x]→LB, MB, MD or	X		UP*	Counter Function Control	105	
	LB, MB, MD ± [X]	LB		LB	Select L Byte Counter	105	
		MB		MB	Select M Byte Counter	105	
		MD		MD	Select MD Counter	105	
	[JJJJ]→ ADDER or G[J] -1	J		DG	Length CTR and Carry Insert Ctl	105	
L	[WWW]→LSA	W	SA	WS*	Local Store Addressing	103	203
	[SSS]→ LS or LS→[SSS]	S	SF*	SF*	Local Store Function	103	203
	2, 3, or 0, C		CS		Local Store Address Sector		203
S	IA + [Z]→ A or	Z		IV	Instr Address Reg Control	103	
	IA + [Z]→ A, IA		CT		Timing Signals to External Channel		203
	HA→ A		TR	TR	Adder Latch Destination	102	202
	SMIF		ZN*	ZN*	(Suppress Memory Instr Fetch)	101	201

Edge Char	Format	Sym	Fld I/O	Fld CPU	Name	CFC Page CPU	CFC Page I/O
C	[Z/Z]⟶IVD IA + [Z] or IA + [Z/Z]	Z		IV	Invalid Digit Test	103	
	[HHHH]	H	CT		Timing Signals to External Channel		203
	[KKKK]IOS or IOS[KKKK]	K	MS		Mpx Channel Stat Control		205
	CH BI or 1 PRI or 1 LCY		CG		Control Signals to Channel		205
	[EEEE] TEST	E	MG		Multiplex Channel Gate Control		205
		E	CL		Selector Channel Adder Latch Test		207
	All Others		SS	SS	Stat Setting and Misc Control	111	211
R	[MMM]⟶ROAR or SCAN	M	ZF	ZF	Function Branch Control	101	201
	[P] Ω [P = P]⟶ A or B or FNTRAP	P	ZN*	ZN*	ROS Address Control	101	201
	All others on last R line		AB	AB	A Condition Test (Left Side)	108	
			BB	BB	B Condition Test (Right Side)	110	

Notes: 1. * = Null generated unless otherwise indicated by a microorder.
2. Letters in brackets refer only to symbol column; i.e. [RRRR] . Letters without brackets appear as on a CAS page. To find a CFC page, use edge character. Then, within that block, find format closest to microorder.

Example: A R + L ⟶ L




0
0
0
500
500
500
CPU Time → 0
500
1000
1500
2000
Reg Set
Late Reg Set
Err Reg Set
Latch Pulse
CPU
Mem Sel
R1
R2
WE
W2
MA011
R/W Lth
MA011
X R/W Lth
MA011
Y R/W Lth
MA011
Sense
MA031
Strobe
MA031
(Access) Set SDR
Data Out
Set AOB Lth
Main Storage
Start Mem
LS701
Set LAR
LS701
Set Read Drvr
LS211
Set Wr Drvr
LS221
Strobe
LS311
Reset SA's
LS311
Local Storage
Ros DR Outgate
Ros DR Ingate
Drive Strobe
KK391
Array Drive
ED151
Sense Bit
EF001
Strobe
EE001
Sense Lth
EF001
Reset SAL
EF001
ROS Timing
Strobe
MP201
Bit
Read Gate
MP201
Set Drvr
MP111
Sample Drvr
MP201
Stor Prot (Read)

BOARD LAYOUT INGATES

HINGE

GT-A	A	B	C	D	E
1	A & B Branch Control	SAR-IAR Chan to Adr Lth.	LTH & SDR 0-15 H Reg 0-15	G1 & G2 F & Q Reg 5 ROSDR Bits Gate Into L & H Control	12 ROSDR Bits Valid Digit Test Direct Cntl Mover Cntl
2	A & B Branch & Adder Test	Adder 0-15 Half Sum Chk 0-15	LTH & SDR 17-31 H Reg 16-31	MD Ctr W Parity W Checking	ROS Decode VFL Sign VFL Invalid Mover Br
3	Stats	Adder 16-31 Half Sum Chk 16-31	Gt Into Reg Cntl Adr Lth to Chan Full Sum Chk M Reg	Mover & Lth Mpx Bfr in Bus Term Mover Left & Right Gts	BAL & BAM WFCN LS Cntl LS Adr Chk Mover Edit J Reg
4	Stat & Feature Control	Emit Field X & Y Gating	LS S9 L Reg R Reg	S9 Local Store	S9 LSAR LSFN

GT-C	A	B	C	D	E
1	CROS Gate-D Has Only a Top Portion and It is Part of CROS				CROS Logic
2					CROS Logic
3	CE Panel Mixing Board	ROAR Backup	CROS Control	CROS Control	CROS Control
4	CE Panel Mixing Board		Chan To Chan Adapter	1052 Adapter X1	1052 Adapter Y1

HINGE

GT-B	A	B	C	D	E
1	Mpx Chan	Mpx Chan	Common Chan	MS Ripple Test Storage & Timing Holdoff	Inst Ctr Supervisory Cntls
2	Mpx Chan	Mpx Chan	Common Chan	Supervisory Cntls	Supervisory Cntls
3	Selector Chan 1 K3	Selector Chan 1 L3	Hi Speed Adapter	Selector Chan 1 N3	Central Clock
4	Selector Chan 1 K4	Selector Chan 1 L4	Selector Chan 1 M4	Selector Chan 1 N4	

GT-E	A	B	C	D	E
1	Sel Chan 3 K3	Sel Chan 3 L3		Sel Chan 3 N3	
2	Sel Chan 3 K4	Sel Chan 3 L4	Sel Chan 3 M4	Sel Chan 3 N4	
3	Sel Chan 2 K3	Sel Chan 2 L3	Common Chan	Sel Chan 2 N3	
4	Sel Chan 2 K4	Sel Chan 2 L4	Sel Chan 2 M4	Sel Chan 2 N4	

CONSOLE ROLLERS

Common Channel Roller - Left Side

	I/O INSTRUCTION				CHAN NUMBER			INSTRUCTION REPLY						PRCD ON IRPT	TIME OUT	TIME OUT CHK	FOUL	
1	START I/O	TEST I/O	HALT I/O	TEST CHAN	4	2	1	0	1	2	3	REPLY	BCHI					

															SBCR			
2	RTNE RECD	PCI ENABL	BREAK IN	I/O RTNE	EARLY FIRST CYCLE	FIRST CYCLE	CHAIN FIRST CYCLE	LS RD	LS WR	CHAL DTC	ALCH DTC	CHAIN	LAST CYCLE	BREAK OUT	0	1	2	3

	BUFFER 1				BUFFER 2				BUFFER 3				I/O STATS					
3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	4	

Multiplexor Channel Roller - Left Side

	BUFFER 1									BUFFER 2								
4	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7

						OUT			IN					BUS OUT				
5	SEL OUT	SEL IN	OP IN	SUP OUT	REQ IN	SVC	ADR	CMND	SVC	ADR	STAT			P	0	1	2	3

	CONTROLLED EMIT				ROUTINE REQUEST TGRS					PRIORITY			CONTROL TRIGGERS						
6	0	1	2	3	A	E1	E2	E3	E4	2	3	PCI	CC	DTC	UCW	IB FULL	POLL	BURST MODE

7																		

8																		

Common/Multiplexor Channel Status

Word 1		Word 2		Word 3		Word 4		Word 5		Word 6	
START I/O	KE001	RTNE RCVD	KE301	BUFFER 1	KE341	BUFFER 1	FA011	SEL OUT	FA141		
TEST I/O	KE001	PCI ENABL	KE131	BUFFER 1	KE341	BUFFER 1	FA011	SEL IN	FA361	CONTROLLED 0	FA063
HALT I/O	KE001	BREAK IN	KE301	BUFFER 1	KE351	BUFFER 1	FA011	OP IN	FA361	CONTROLLED 1	FA063
TEST CHAN	KE001	I/O RTNE	KE311	BUFFER 1	KE351	BUFFER 1	FA021	SUP IN	FA151	EMIT 2	FA063
CHAN 4	KE021	EARLY FIRST CYC	KE301	BUFFER 2	KE341	BUFFER 1	FA021	REQ IN	FA361	EMIT 3	FA063
CHAN 2	KE021	FIRST CYC	KE301	BUFFER 2	KE341	BUFFER 1	FA021	SVC OUT	FA141	RTNE A	FA171
NUMBER 1	KE021	CHAIN FIRST CYC	KE321	BUFFER 2	KE351	BUFFER 1	FA031	ADR OUT	FA131	REQ E1	FA171
INSTR 0	KE051	LS RD	KE471	BUFFER 2	KE351	BUFFER 1	FA031	CMND OUT	FA141	TGRS E2	FA171
INSTR 1	KE051	LS WR	KE471	BUFFER 2	KE341	BUFFER 1	FA031	SVC IN	FA351	TGRS E3	FA171
REPLY 2	KE061	CHAL DTC	KE441	BUFFER 3	KE341	BUFFER 1	FA011	ADR IN	FA351	TGRS E4	FA171
REPLY 3	KE061	ALCH DTC	KE441	BUFFER 3	KE351	BUFFER 2	FA011	STAT IN	FA351	PRIORITY 2	FA261
REPLY	KE071	CHAIN	KE321	BUFFER 3	KE351	BUFFER 2	FA011			PRIORITY 3	FA261
BCHI	KE141	LAST CYC	KE321			BUFFER 2	FA021	P	FA051	PRIORITY PCI	FA261
PRCD ON IRPT	KE101	BREAK OUT	KE321	BUFFER 4	KE151	BUFFER 2	FA021	0	FA051	CTRL CC	FA251
TIME OUT	KE091			BUFFER 4	KE161	BUFFER 2	FA021	1	FA051	CTRL DTC	FA261
TIME OUT CHK	KE091	SBCR 0	KE381	I/O	KE171	BUS	FA021	2	FA051	CTRL UCW	FA251
FOUL	KE091	SBCR 1	KE381	STATS	KE181	OUT	FA031	3	FA051	CTRL IB FULL	FA331
IOHS	KE191	SBCR 2	KE381	STATS	KE191		FA031	4	FA051	CTRL POLL	FA341
		SBCR 3	KE381	I/O CHK MODE	KE311		FA031	5	FA051	CTRL BURST MODE	FA311
			KE441	LOGS 1	KE661	REQ LOG OUT	FA341	6	FA051	MPX 0	FA091
		ROS 34	KE441	LOGS 2	KE661			7	FA051	I/O 1	FA101
		BITS 47	KE321	LOGS 3	KE661			PRGM CHK	FA371	STATS 2	FA111
		BITS 48	KE321	GATE STATUS	KE671			STOR PROT CHK	FA371	STATS 3	FA121
		FIRST CYC CHK	KE531	RESET	KE671					DATA XFR CTRL	FA071
										CC RESET CTRL	FA252

Common Channel Roller - Right Side

																	1
	ROS BITS				FIRST CYCLE CHK												2
	33	34	47	48													
I/O CHK MODE	LOGS			GATE STATUS	RESET												3
	1	2	3														
					REQ LOG OUT												4
	BUS OUT				CHECKS												5
4	5	6	7	PGRM	STOR PROT*												
	MPX I/O STATS				DATA XFER CNTL	CC RESET CNTL											6
0	1	2	3														
																	7
																	8

* = Key Mismatch

CONSOLE

Selector Channel Roller - Left Side

1	B REGISTER																	
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
2	C REGISTER																	C
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
3	BYTE COUNTER						END REG		LAST WORDS			END OF RECORD						REGS
	A			B								COUNT			READ	B	LS	
	P	2	1	P	2	1	2	1	3	2	1	INTLK	1	2	INTLK	AC	ENABL	LS
4	POSITION REGISTER									CYCLE COUNTER PHASE A STEP				CLOCK			LS	PCI
	UA FETCH	CCW1 TYPE	CCW2 TYPE	UNIT SEL	RD STORE	WR FETCH	END UP	COMP	IRPT	0	1	2	3	A0	A1	STEP	REQ	REQ
5	POS REG TRF	INH RD STOR	A CLOCK				SP		INSN SCAN	CHAN IN USE	POLL	POLL IRPT END	INSN INH	BC RDY	UA TO BUS = 0	U SEL ADR OUT	COMPARE	
			A	B	C	D	D1	D2									=	≠
6		GENERAL PURPOSE REGISTER										FLAG REG						FIRST WORD
		1	2	3	4	5	6	7				CDA	CC	SILI	SKIP	PCI	FIN	
7															FILE	LOAD MODE	ODD PARITY	TRANS-LATE *
8																		

* 1410-7010 Emulator

Selector Channel Status

Word 1		Word 2		Word 3		Word 4		Word 5		Word 6	
B REG		C REG									
P0-7	GH101	P0-7	GH101	BYTE P	GR131	UA FETCH	GB181	POS REG TRF	GB171	1	GC101
0	GH111	0	GH111	CTR 2	GR131	CCW1 TYPE	GB181	INH RD STOR	GG131	2	GC101
1	GH121	1	GH121	A 1	GR131	CCW2 TYPE	GB181	A	GA101	GENERAL 3	GC101
2	GH131	2	GH131	BYTE P	GR131	UNIT SEL	GB181	B	GA101	PURPOSE 4	GC101
3	GH141	3	GH141	CTR 2	GR131	RD STORE	GB181	CLOCK C	GA101	REG 5	GC121
4	GH151	4	GH151	B 1	GR131	WR FETCH	GB181	D	GA101	6	GC121
5	GH161	5	GH161	END 2	GC111	END UP	GB181	SP D1	GA161	7	GC121
6	GH171	6	GH171	REG 1	GC111	COMPARE	GB181	D2	GA161	CDA	GC161
7	GH181	7	GH181	LAST 3	GC141	INTERRUPT	GB181	INSN SCAN	GF111	FLAG CC	GC161
P8-15	GJ101	P8-15	GJ101	WORDS 2	GC141	CYCLE 0	GA131	CHAN IN USE	GF111	REG SILI	GC161
8	GJ111	8	GJ111	1	GC141	CTR 1	GA131	POLL	GR121	SKIP	GC161
9	GJ121	9	GJ121	CNT INTLK	GC151	PHASE A 2	GA131	POLL IRPT END	GR121	PCI	GC161
10	GJ131	10	GJ131	EOR 1	GC151	STEP 3	GA131	INSN INH	GD131	FINISH	GB161
11	GJ141	11	GJ141	2	GC151	A0	GA111	BC RDY	GF141	FIRST WORD	GF161
12	GJ151	12	GJ151	RD INTLK	GC151	CLOCK A1	GA111	UA TO BUS = 0	GV121	FIRST BYTE	GF161
13	GJ161	13	GJ161	BAC	GG131	STEP	GA111	UNIT SEL ADR OUT	GV121	TOTAL REC FETCH	GF111
14	GJ171	14	GJ171	LS ENABL	GG131	LS REQ	GG101	COMPARE =	GR151	WR CHAIN PRCD	GT131
15	GJ181	15	GJ181		GC171	PCI REQ	GG181	≠	GR151	STOP REL	GV111
P16-23	GK101	P16-23	GK101	REG LS	GC171		GB141	STOP	GV101	STAT NEXT	GT161
16	GK111	16	GK111	FULL B	GT141	PRIORITY 1	GB141	IF CDA FIRST BYTE	GT161	C1	GA141
17	GK121	17	GK121	BKWD	GC131	2	GB151	CD	GF111	MP C2	GA141
18	GK131	18	GK131	READ OP	GC131	3	GB101	BC MOD ENABL	GR141	C3	GA151
19	GK141	19	GK141	RDY	GF161	0	GB101	WR CHAIN RDY	GF161	C4	GA151
20	GK151	20	GK151	IF	GT121	REQUEST 1	GB101	REC END	GF111	SUP OUT	GS131
21	GK161	21	GK161	OP	GC131	REG 2	GB101	OP IN TEST	GR101	REQ IN	GS141
22	GK171	22	GK171	WRITE RDY	GF161	3	GB111	CHAN STOP	GE121	SVC OUT HOLD	GV151
23	GK181	23	GK181	IF	GT121	4	GB111	SEL OUT	GR101	BLOCK STAT IN	GS111
P24-31	GL101	P24-31	GL101	CD=PC TYPE	GE111	5	GB111	SEL OUT	GR101		
24	GL111	24	GL111	SIM	GG131	STATS 0	GB131	STOP RTNE	GV101		
25	GL121	25	GL121	ILI	GE111	1	GB121	SEL IN	GS121		
26	GL131	26	GL131	CHAN PGRM	GE111	2	GB121	OP IN	GS121		
27	GL141	27	GL141	CHKS STOR PROT	GE111	3	GB131	SVC OUT	GS131		
28	GL151	28	GL151	CHAN DATA	GE111	LS	GA030	ADR OUT	GS131		
29	GL161	29	GL161	CHAN CTRL	GE101	COM PRI 1	GA030	CMND OUT	GS131		
30	GL171	30	GL171	IF CTRL	GE101	CHAN PRI 2-3	GA030	SVC IN	GS111		
31	GL181	31	GL181	CHAIN 1	GE111	DETECT PCI	GA030	ADR IN	GS111		
						INH RTNE	GA030	STAT IN	GS111		

Selector Channel Roller - Right Side

B REGISTER																		
P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	1
C REGISTER																		
P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	2
FULL		READ				WRITE			CHANNEL CHECKS									
B	C	BKWD	OP	RDY	IF	OP	RDY	IF	CD=PC TYPE	SIM	ILI	PRGM	STOR PROT*	CHAN DATA	CHAN CTRL	IF CTRL	CHAIN 1	3
REQUEST REGISTER													COMMON CHAN DETECT					
PRIORITY			STAT											PRI 1	PRI 2-3		INH RTNE	4
1	2	3	0	1	2	3	4	5	0	1	2	3	LS			PCI		
	IF CDA FIRST		BC MOD	WR CHAIN		OP IN						OUT			IN			
STOP	BYTE	CD	ENABL	RDY	REC END	TEST	CHAN STOP	SEL OUT	STOP RTNE	SEL IN	OP IN	SVC	ADR	CMND	SVC	ADR	STAT	5
		TOTAL	WR							MP						SVC	BLOCK	
	FIRST BYTE	REC FETCH	CHAIN PRCD	STOP REL				STAT NEXT		C1	C2	C3	C4	SUP OUT	REQ IN	OUT HOLD	STAT IN	6
																		7
																		8

* = Key Mismatch

CPU Roller 1 - Left Side

1	L REGISTER																	
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
2	R REGISTER																	
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
3	M REGISTER																	
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
4	H REGISTER																	
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
5	SAR																	
	P 8-15	8	9	10	11	12	13	14	15	P 16-23	16	17	18	19	20	21	22	23
6	ROS	CE				LX			TC	RY			AD					
	P 57-89	57	58	59	60	61	62	63	64	65	66	67	CL 68	69	70	71	72	73
7	PRIORITY TRIGGERS			INSERT	REMOTE	LCS CONTROL			LCS READY									
	REQ	MASTER	LAST CYCLE	PREFIX TGR	STOR READY	SYNC TGR	RING INH	INVAL ADDR	1	2	3	4						
8	CHECK					UNIT IDENTITY												
	MARK	KEY	ADDR	DATE		1	2	3	4									

CPU #1 Status

Word 1		Word 2		Word 3		Word 4		Word 5		Word 6		
L REG		R REG		M REG		H REG		SAR				
P0-7	RL001	P0-7	RR001	P0-7	RM001	P0-7	RH001	P8-15	RA061	ROS P57-89		RK301
0	RL001	0	RR001	0	RM001	0	RH001	8	RA003		57	RK301
1	RL001	1	RR001	1	RM001	1	RH001	9	RA003		58	RK301
2	RL001	2	RR001	2	RM001	2	RH001	10	RA002	CE	59	RK301
3	RL001	3	RR001	3	RM001	3	RH001	11	RA002		60	RK301
4	RL011	4	RR011	4	RM011	4	RH011	12	RA002		61	RK311
5	RL011	5	RR011	5	RM011	5	RH011	13	RA002	LX	62	RK311
6	RL011	6	RR011	6	RM011	6	RH011	14	RA001		63	RK311
7	RL011	7	RR011	7	RM011	7	RH011	15	RA011	TC	64	RK311
P8-15	RL021	P8-15	RR021	P8-15	RM021	P8-15	RH021	P16-23	RA061		65	RK311
8	RL021	8	RR021	8	RM021	8	RH021	16	RA011	RY	66	RK311
9	RL021	9	RR021	9	RM021	9	RH021	17	RA011		67	RK311
10	RL021	10	RR021	10	RM021	10	RH021	18	RA011		68	BH061
11	RL021	11	RR021	11	RM021	11	RH021	19	RA011	CL	69	BH061
12	RL031	12	RR031	12	RM031	12	RH031	20	RA021	AD	70	BH061
13	RL031	13	RR031	13	RM031	13	RH031	21	RA021		71	BH061
14	RL031	14	RR031	14	RM031	14	RH031	22	RA021		72	RK331
15	RL031	15	RR031	15	RM031	15	RH031	23	RA021		73	RK331
P16-23	RL041	P16-23	RR041	P16-23	RM041	P16-23	RH041	P24-31	RA061	AB	74	RK331
16	RL041	16	RR041	16	RM041	16	RH041	24	RA021		75	RK331
17	RL041	17	RR041	17	RM041	17	RH041	25	RA031		76	RK331
18	RL041	18	RR041	18	RM041	18	RH041	26	RA031		77	RK331
19	RL041	19	RR041	19	RM041	19	RH041	27	RA031		78	RK341
20	RL051	20	RR051	20	RM051	20	RH051	28	RA031		79	RK341
21	RL051	21	RR051	21	RM051	21	RH051	29	RA031	BB	80	RK341
22	RL051	22	RR051	22	RM051	22	RH051	30	RA061		81	RK341
23	RL051	23	RR051	23	RM051	23	RH051	31	RA061		82	RK341
P24-31	RL061	P24-31	RR061	P24-31	RM061	P24-31	RH061	0	KS001		84	RK351
24	RL061	24	RR061	24	RM061	24	RH061	BYTE 1	KS001		85	RK351
25	RL061	25	RR061	25	RM061	25	RH061	STATS 2	KS001	SS	86	RK351
26	RL061	26	RR061	26	RM061	26	RH061	3	KS011		87	RK351
27	RL061	27	RR061	27	RM061	27	RH061	BYTE 0	KS021		88	RK351
28	RL071	28	RR071	28	RM071	28	RH071	STORE 1	KS021		89	RK351
29	RL071	29	RR071	29	RM071	29	RH071	STATS 2	KS031			
30	RL071	30	RR071	30	RM071	30	RH071	3	KS031			
31	RL071	31	RR071	31	RM071	31	RH071					

CPU Roller 1 - Right Side

L REGISTER																	1
P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
R REGISTER																	2
P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
M REGISTER																	3
P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
H REGISTER																	4
P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
SAR										BYTE STATS				BYTE STORE STATS				5
P 24-31	24	25	26	27	28	29	30	31		0	1	2	3	0	1	2	3	
AB				BB					UX	SS								6
74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89			
				See Below								EM STAT						7
				92	93	94	95	96	97									
																		8

CPU#1 Status			
Word 7		Word 8	
Stor Sync Tgr	KT277	Mark Ck	BH132
Stor Ring Inh	KT272	Key Ck	BH132
LCS Inv Addr	BH131	Addr Ck	BH132
LCS Rdy 1-4	BH131	Data Ck	BH132
ROS 92-97	XF001	Unit ID 1-4	BH132
EM Stat	XF501		

CPU Roller 2 - Left Side

1	ROS P 1-30	LU			MV		ZP						ZF				ZN	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
2	ROS P 32-55	IV CT			AL					WM WL			HC	UP		MD	LB MS	MB CG
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
3	ONE SYL OP	RE-FETCH					NEXT ROS ADDRESS											
						EXT	ROS BASE ADDRESS						FUNCTION BIT				BRANCH	
							0	1	2	3	4	5	0	1	2	3	A	B
4	I/O MODE	I/O REGISTER			TIMER IRPT	CONS IRPT	L BYTE CNTR			M BYTE CNTR			F REG					Q REQ
		P	0	1			P	0	1	P	0	1	P	0	1	2	3	
5	LSAR							FN	LS	J REG					MD			
	P	0	1	2	3	4	5	0	1	P	0	1	2	3	P	0	1	2
6	ADDER									COUNTERS					MOVER			
	HALF SUM				SUM										INPUTS		OUTPUTS	
	0-7	8-15	16-23	24-31	0-7	8-15	16-23	24-31	CARRY	L BYTE	M BYTE	MD	G1	G2	L	R		
7							CURRENT ROS ADDRESS											
						EXT	0	1	2	3	4	5	6	7	8	9	10	11
8							PREVIOUS ROS ADDRESS											
						EXT	0	1	2	3	4	5	6	7	8	9	10	11

CPU #2 Status

Word 1		Word 2		Word 3		Word 4		Word 5		Word 6	
ROS P1-30	BH091	ROS P30-55	RK211	ONE SYL OP	KS221	I/O MODE	KU111	0	LS111	0-7	KT011
LU 1	RK121	IV-CT 32	RK201	RE-FETCH	KS211	I/O P	RL111	1	LS111	8-15	KT011
2	RK121	33	RK201	ROS 0	KK301	REG 0	RL111	2	LS111	HALF 16-23	KT011
3	RK121	34	RK201	BASE 1	KK301	1	RL111	3	LS121	SUM 24-31	KT011
MV 4	RK121	35	RK211	ADR 2	KK311	TIMER IRPT	KS251	4	LS121	0-7	KT011
5	RK121	36	RK211	3	KK311	CONS IRPT	KS251	5	LS121	8-15	KT011
6	KK301	AL 37	RK211	4	KK321	L BYTE P	CL001	0	KL001	SUM 16-23	KT011
7	KK301	38	RK211	NEXT 5	KK301	0	CL001	1	KL001	24-31	KT011
ZP 8	KK311	39	RK211	ROS ADDR 0	KK011	CNTR 1	CL001	LSFN P	RJ011	CARRY	KT021
9	KK311	WM WL 40	RK221	FUNCT 1	KK021	P	CM001	J 0	RJ001	L BYTE	KT021
10	KK321	41	RK221	BIT 2	KK031	MB 0	CM001	REG 1	RJ001	CNTRS M BYTE	KT021
11	KK301	42	RK221	3	KK041	CNTR 1	CM001	2	RJ001	MD	KT021
12	KK001	HC 43	RK221	BRANCH A	KK261	P	RF021	3	RJ001	G1	KT031
ZF 13	KK001	UP 44	RK221	B	KK271	F 0	RF001	P	CD021	G2	KT031
14	KK001	MS 45	RK221	1	KS271	REG 1	RF001	MD 0	CD001	MVR IN L	KT021
15	KK001	MD 46	RK231	EXT 2	KS271	2	RF001	CTR 1	CD001	MVR IN R	KT021
16	KK003	LB 47	RK231	IRPT 3	KS271	3	RF011	2	CD011	MVR OUT	KT021
ZN 17	KK003	CG MB 48	RK231	REG 4	KS281	Q REQ	RF031	3	CD011	8-15	KT031
18	KK003	49	RK231	5	KS281	EDIT 1	KK581	S	KP031	SAR 16-23	KT031
19	RK101	DG-MG 50	RK231	6	KS281	STATS 2	KK581	P	CG101	24-31	KT031
20	RK101	51	RK231	ILC 32	RP001	0	KS101	G1 0	CG101	1-30	KT031
TR 21	RK101	UL 52	RK201	33	RP001	1	KS111	1	CG101	ROS 32-55	KT031
22	RK101	53	RK201	CC 34	RP011	2	KS121	2	CG101	57-89	KT031
23	RK101	UR 54	RK201	35	RP021	GP 3	KS131	3	CG101	PROT TAG	KT041
24	XG401	55	RK201	PSW 36	RP001	STATS 4	KS141	S	KP031	LCS	KT041
WS CS- 25	RK111	MVR 0	KQ001	37	RP001	5	KS151	P	CG201	LOG REQ	KT041
SA 26	RK111	FUNCT 1	KQ001	PM 38	RP001	6	KS161	0	CG201		
27	RK111	CPU 2	KQ001	39	RP001	7	KS171	G2 1	CG201		
SF 28	RK111	MVR 0	KQ001			L SIGN	KS201	2	CG201		
29	RK111	FUNCT 1	KQ001			R SIGN	KS201	3	CG201		
30	RK111	I/O 2	KQ001			CARRY	KS231				
						RTL	KS631				
						STORAGE R1	KC501				
						RING R2	KC501				
						R3	KC501				
						W1	KC501				

CPU Roller 2 - Right Side

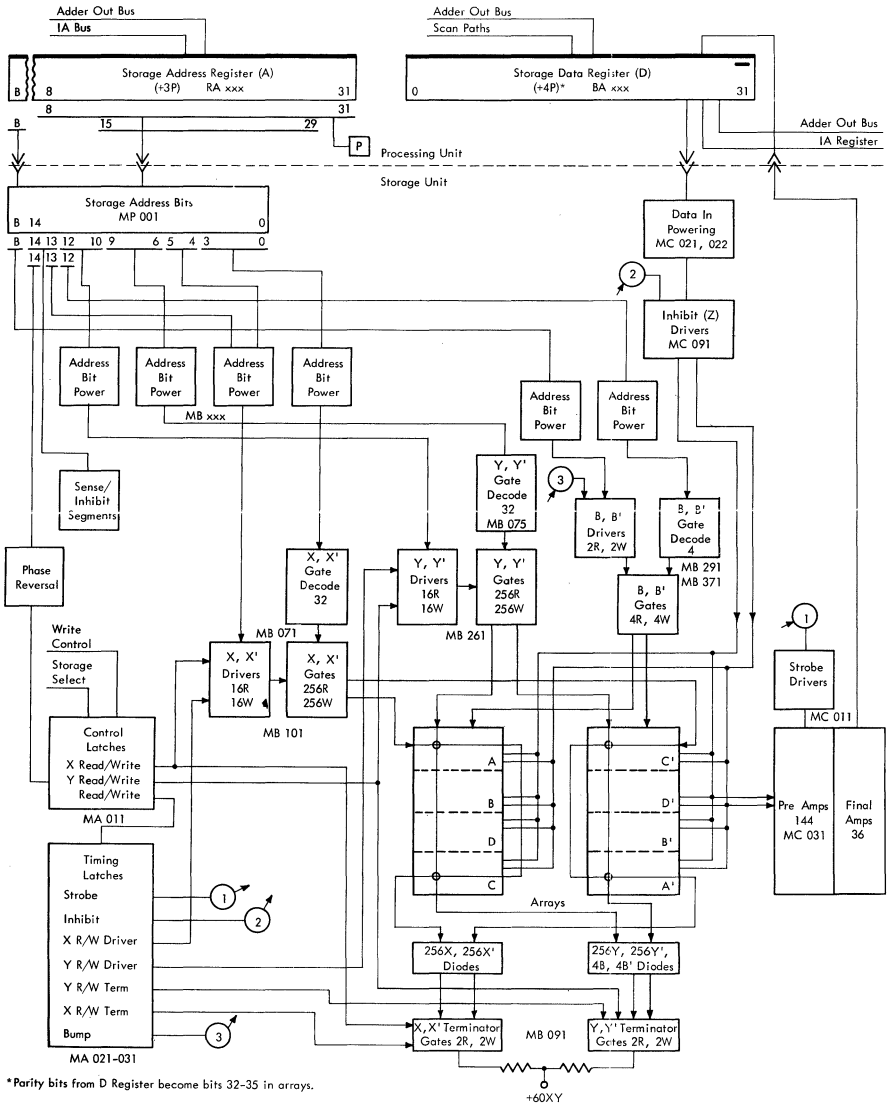
ZN		TR					ZR	WS			SF						
								CS	SA								1
18		19	20	21	22	23	24	25	26	27	28	29	30				
DG		UL		UR			MOVER FUNCTION										
MG								CPU			I/O						2
49	50	51	52	53	54	55		0	1	2	0	1	2				
EXTERNAL INTERRUPT REGISTER							PSW										
							ILC		CC		PM						3
1	2	3	4	5	6		32	33	34	35	36	37	38	39			
EDIT STATS		GENERAL PURPOSE STATS													STORAGE RING				
											L	R						4
1	2	0	1	2	3	4	5	6	7		SIGN	SIGN	CARRY	RTL	R1	R2	R3	W1	
MD		G1						G2											
																			5
3		S	P	0	1	2	3	S	P	0	1	2	3						
SAR			ROS			*													
						PROT		LOG											6
8-15	16-23	24-31	1-30	32-55	57-89	TAG	LCS	REQ											
																			7
																			8

* = Parity Error in Stg Protect

CPU #2 Status			
Word 7		Word 8	
Current ROS Address		Previous ROS Address	
Ext	KK302	Ext	KK302
0	KK312	0	KK312
1	KK312	1	KK312
2	KK312	2	KK312
3	KK312	3	KK312
4	KK312	4	KK312
5	KK312	5	KK312
6	KK313	6	KK313
7	KK313	7	KK313
8	KK313	8	KK313
9	KK313	9	KK313
10	KK313	10	KK313
11	KK313	11	KK313

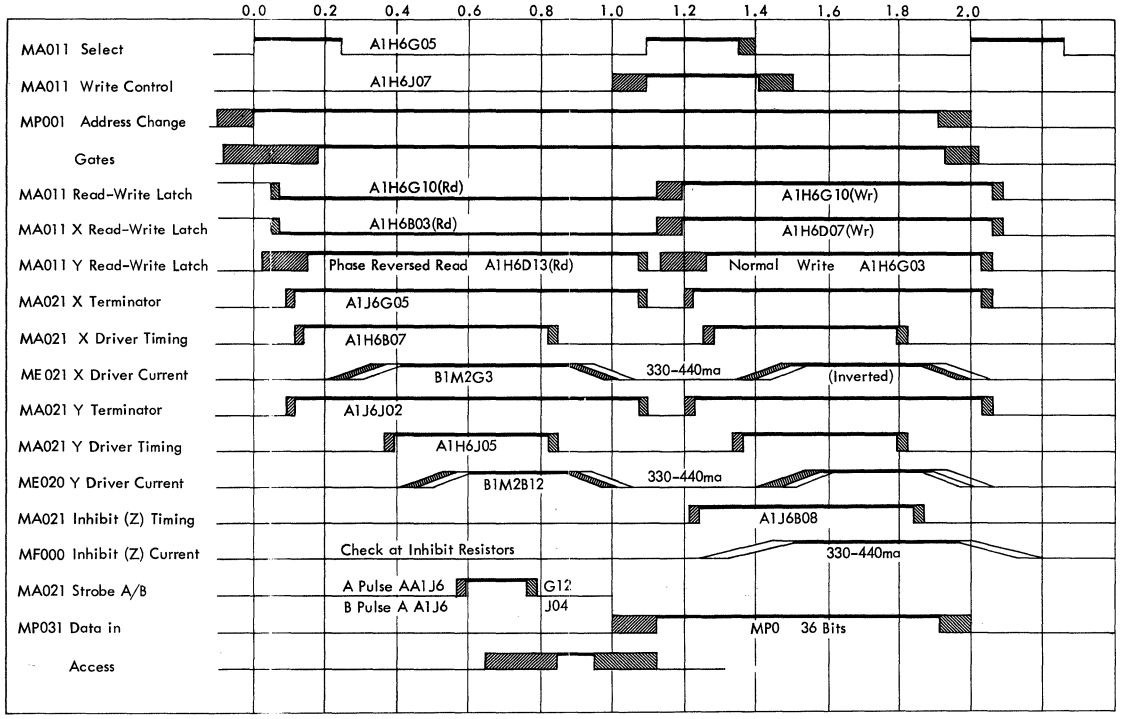
Emulator ROS Fields	
1410-7010	7070-7074
ZR-24 UX-83 YC-92,93,94	ZR-24 WT-92,93 EE-94,75,96

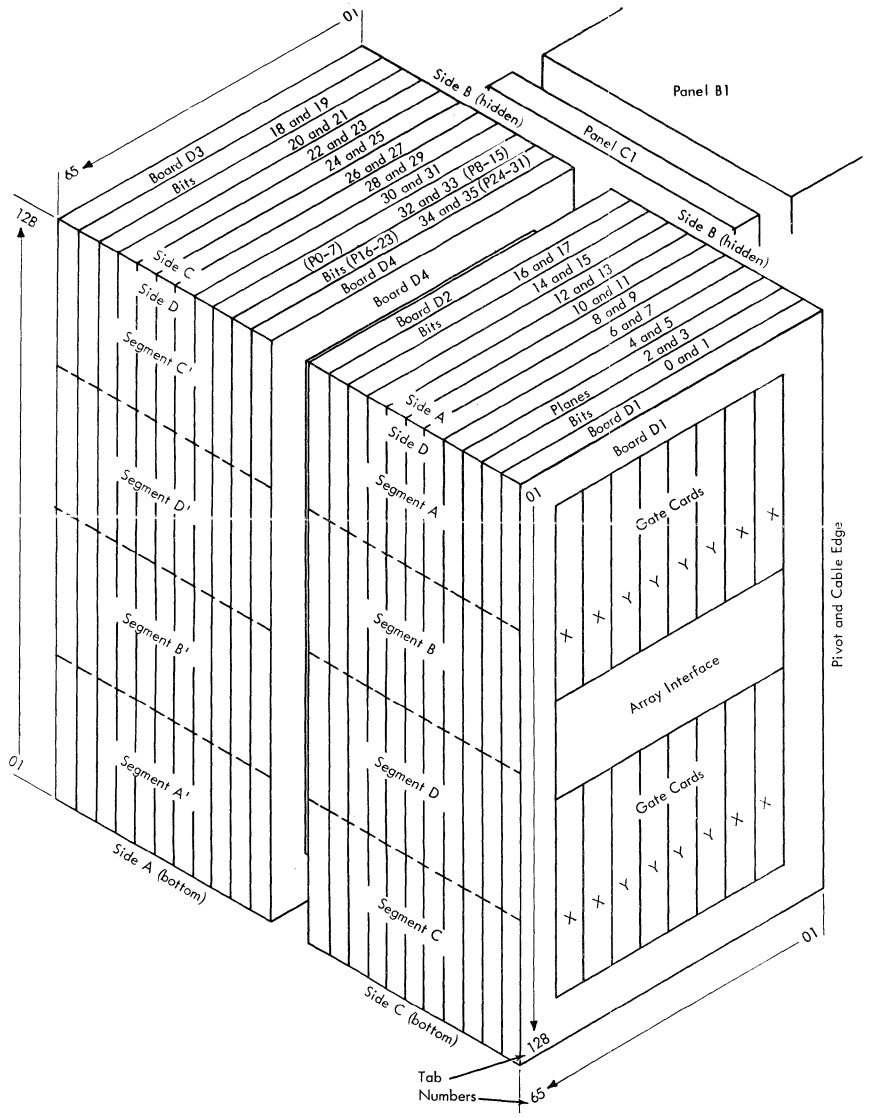
SDR		IAR		Maintenance Chk	
P0-7	BA072	P8-15	CA171	PASS	KH321
0	BA001	8	CA161	FAIL	KH321
1	BA011	9	CA161	BINARY TGR	KH211
2	BA021	10	CA161	TEST CTR = 0	KH311
3	BA031	11	CA161	FLT 0	KH111
4	BA041	12	CA151	FLT 1	KH111
5	BA051	13	CA151	OP 2	KH111
6	BA061	14	CA151	REG 3	KH111
7	BA071	15	CA151	REG 4	KH111
P8-15	BA152	P16-23	CA171	REG 5	KH111
8	BA081	16	CA141	SEQ CTR 4	KH341
9	BA091	17	CA141	SEQ CTR 2	KH341
10	BA101	18	CA141	SEQ CTR 1	KH341
11	BA111	19	CA141	SEQ STAT 1	KH345
12	BA121	20	CA131	SEQ STAT 2	KH345
13	BA131	21	CA131	SEQ STAT 3	KH345
14	BA141	22	CA131	SEQ STAT 4	KH345
15	BA151	23	CA131	FLT LD CHK	KH555
P16-23	BA232	P24-31	CA171	SUPV STAT	KH321
16	BA161	24	CA121	PROGSV SCAN STAT	KH321
17	BA171	25	CA121	SUPV ENABL STOR	KH321
18	BA181	26	CA121	MODE SEQ CTR	KT151
19	BA191	27	CA121	MODE MAIN STOR	KT151
20	BA201	28	CA111	MODE ROS	KT151
21	BA211	29	CA111	ALT PREFIX	
22	BA221	30	CA111	HARD STOP	KT161
23	BA231	31	CA111	LOG TGR	KT151
P24-31	BA312			BLOCK IND	KH231
24	BA241	System Status		SINGLE CYC	KT271
25	BA251			CLOCK CPU	KT215
26	BA261			CLOCK CHAN	KT211
27	BA271	MASTER CHK	KT081	CLOCK ROS	KT211
28	BA281	LOAD	PL031	CLOCK MAIN STOR	KT211
29	BA291	TEST	PK101	IRPT CHK ENABLD	KT161
30	BA301	WAIT	PK101	CHK REG GATED	KT161
31	BA311	MANUAL	PK101	CHK PEND	KT081
		SYSTEM	PK101		



*Parity bits from D Register become bits 32-35 in arrays.

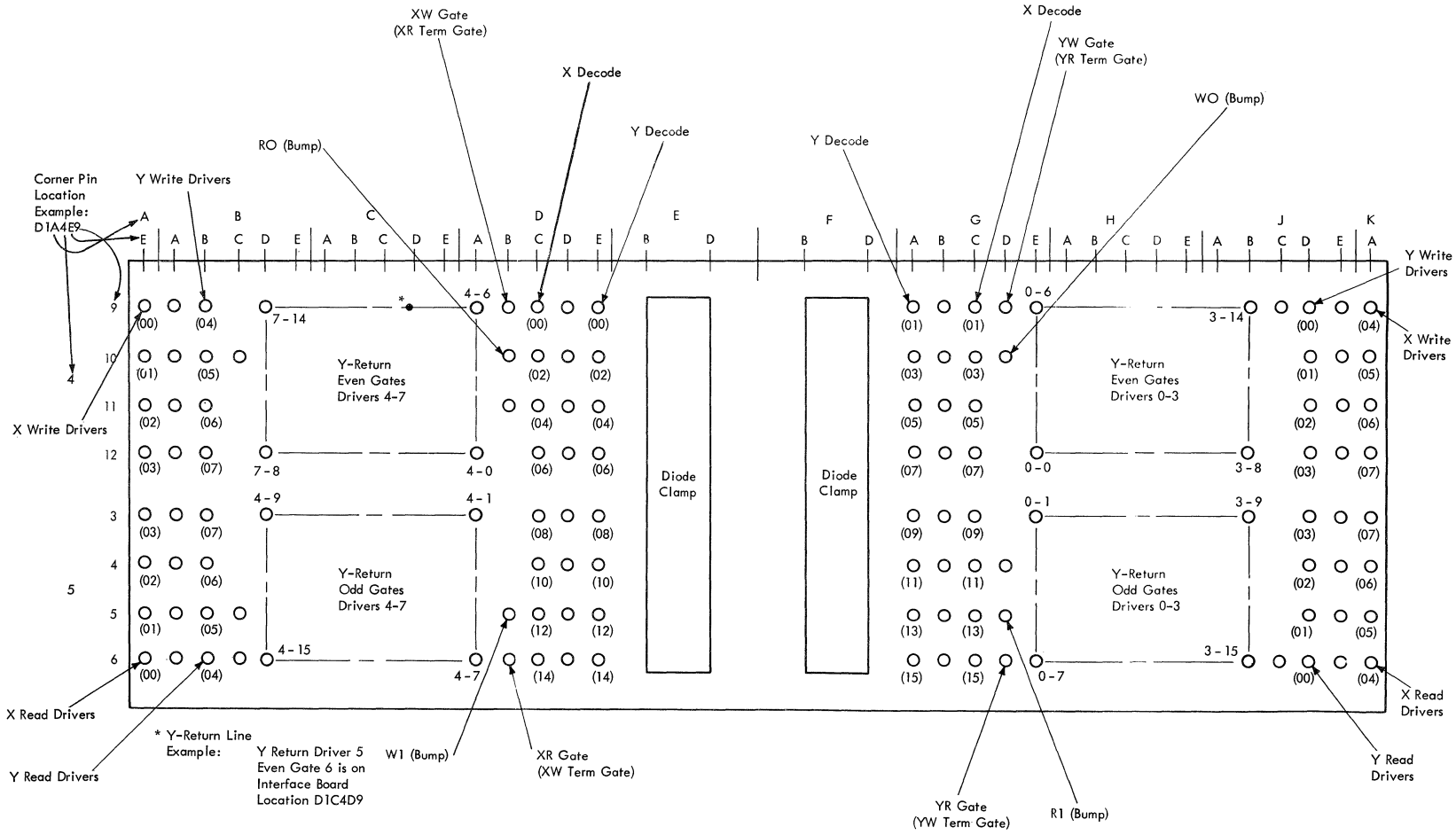
MAIN STORAGE TIMING

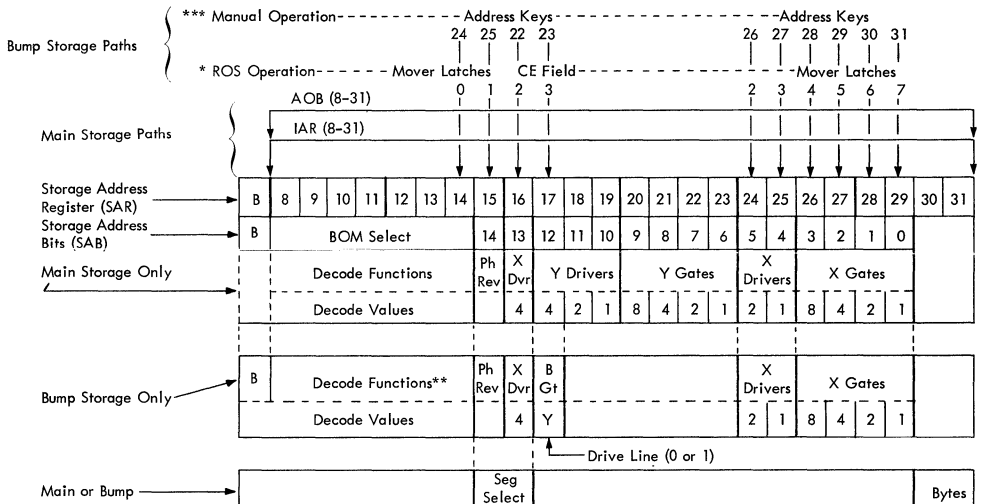




ADDRESS BITS 13 AND 14 RELATIONSHIP TO STROBE -- INHIBIT SEGMENTS, PLANES AND ADDRESSES

Address Bit 14	Address Bit 13	Strobe Pulse	Strobe Bytes	Strobe Segments	Inhibit Segments	Planes (Bits) Array 1	Planes (Bits) Array 2	Addresses
		B	0,2	A, A'	A, A'	0 - 8	18 - 26	0000-8191
	1	B	0,2	B, B'	B, B'	0 - 8	18 - 26	8192-16383
1		A	0,2	C, C'	C, C'	0 - 8	18 - 26	16384-24575
1	1	A	0,2	D, D'	D, D'	0 - 8	18 - 26	24576-32767
		A	1,3	A, A'	A, A'	9 - 17	27 - 35	0000-8191
	1	A	1,3	B, B'	B, B'	9 - 17	27 - 35	8192-16383
1		B	1,3	C, C'	C, C'	9 - 17	27 - 35	16384-24575
1	1	B	1,3	D, D'	D, D'	9 - 17	27 - 35	24576-32767

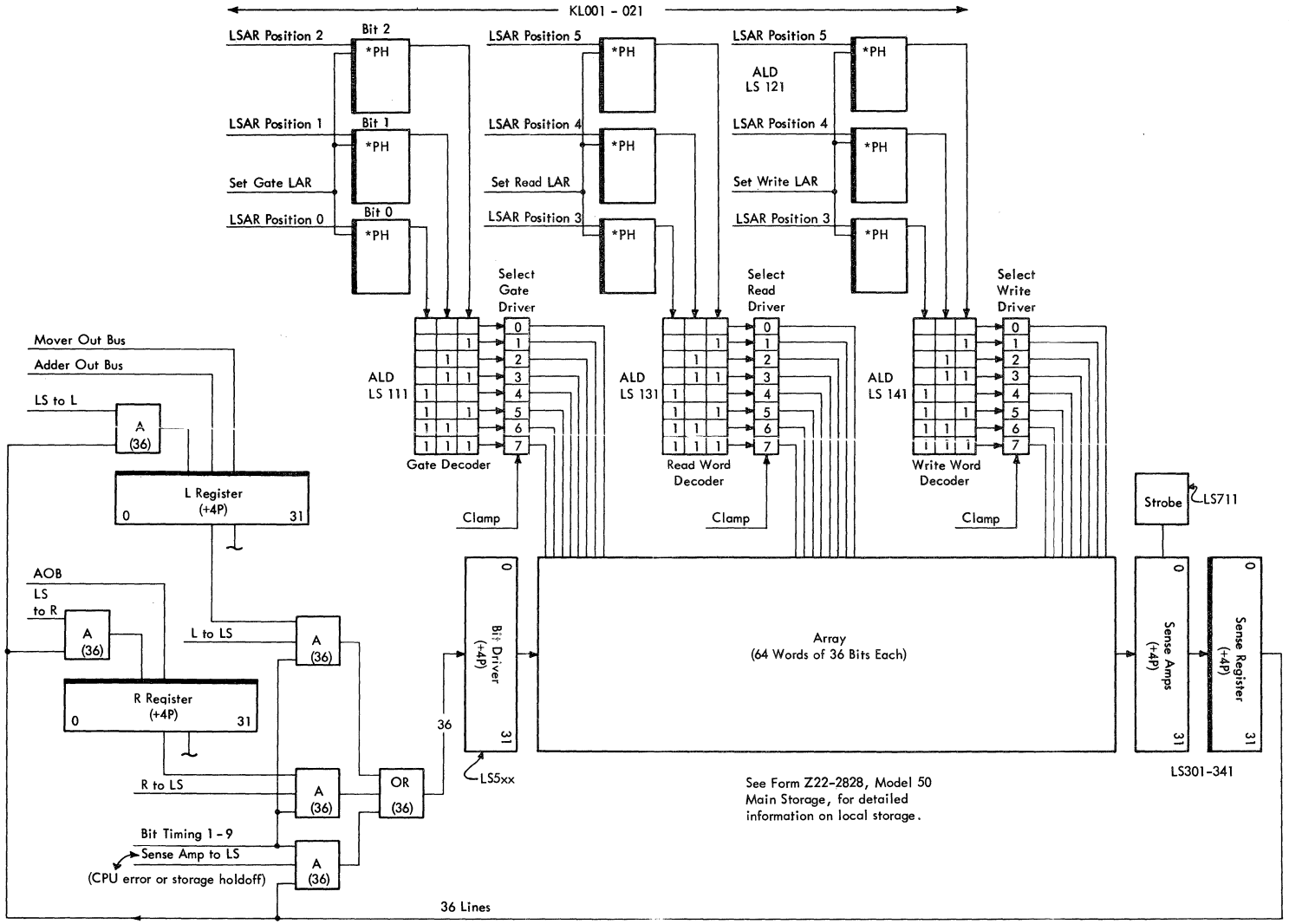


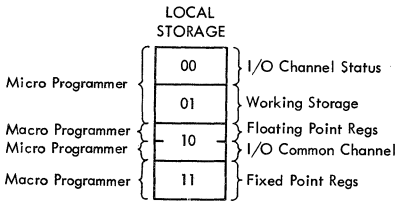


* These operations are brought up by microorders [W, E → A; or W, E → A (S)] which turn on the B bit in SAR.

** W(0) is used to determine which BOM is addressed for 256 subchannel feature.

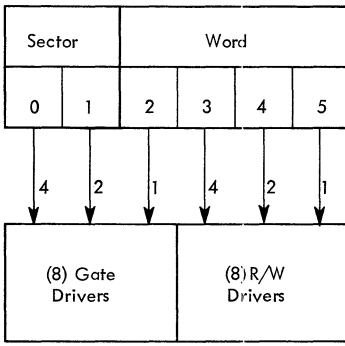
*** For shared subchannel manual operation use UA prime.

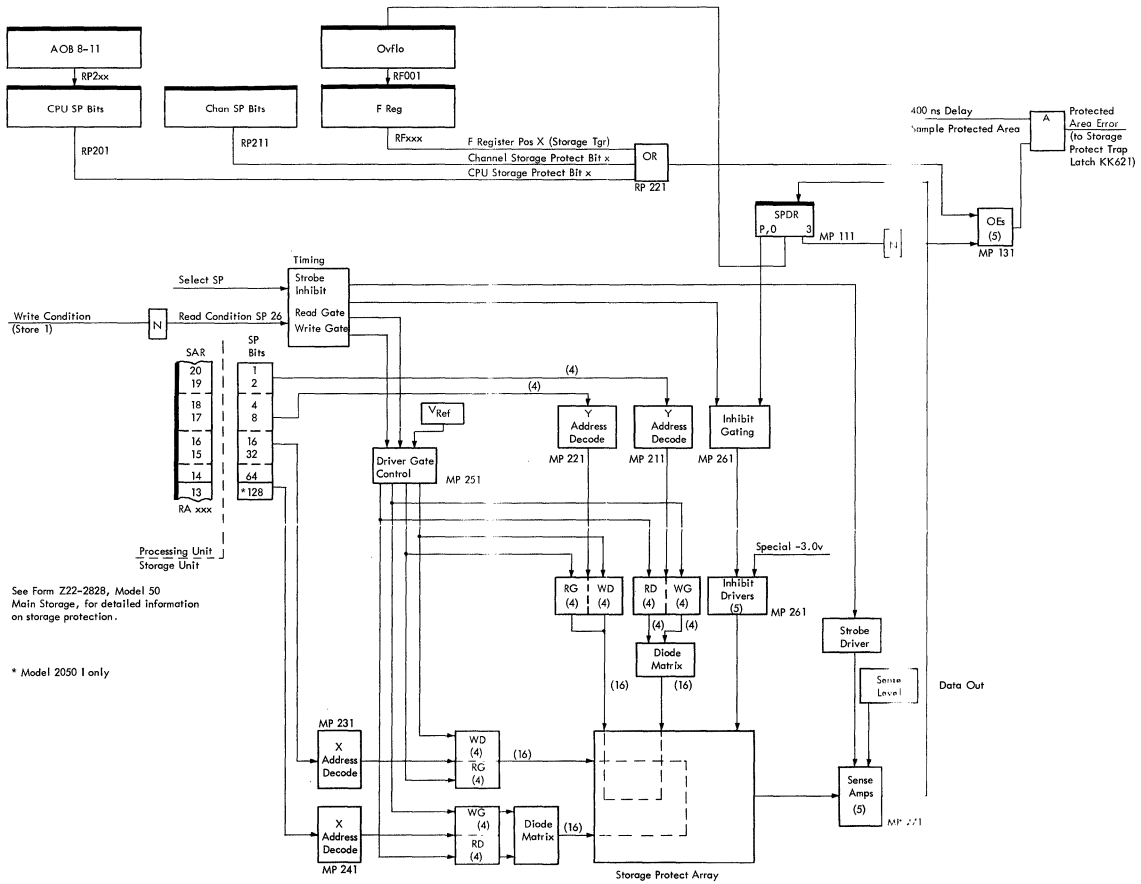

KL001 - 021
LSAR Position 2
Bit 2
*PH
LSAR Position 1
Bit 1
Set Gate LAR
LSAR Position 0
Bit 0
LSAR Position 5
LSAR Position 4
Set Read LAR
LSAR Position 3
ALD
LS 121
Set Write LAR
Select
Gate
Driver
Select
Read
Driver
Select
Write
Driver
ALD
LS 111
ALD
LS 131
ALD
LS 141
Gate Decoder
Read Word
Decoder
Write Word
Decoder
Clamp
Mover Out Bus
Adder Out Bus
LS to L
A
(36)
L Register
(+4P)
AOB
LS
to R
L to LS
R Register
(+4P)
R to LS
OR
Bit Timing 1 - 9
Sense Amp to LS
(CPU error or storage holdoff)
36 Lines
36
Bit Driver
(+4P)
LS5xx
Array
(64 Words of 36 Bits Each)
Strobe
LS711
Sense Amps
(+4P)
Sense Register
(+4P)
LS301-341
See Form Z22-2828, Model 50
Main Storage, for detailed
information on local storage.



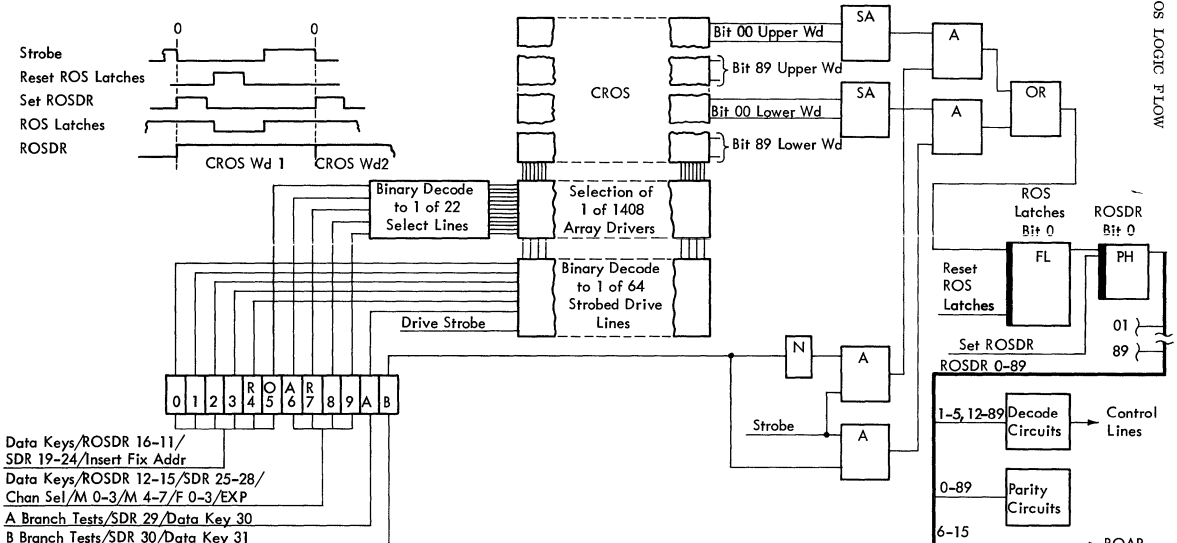
				Address		
				Sector	Word	
Sector 00 I/O Channel Status (16 Positions)	Channel 00	Command Address	Selector Channel	00	00	00
		Data Address		00	00	01
		Count		00	00	10
		Data		00	00	11
	01	Command Address	Selector Channel	00	01	00
		Data Address		00	01	01
		Count		00	01	10
		Data		00	01	11
	10	Command Address	Selector Channel	00	10	00
		Data Address		00	10	01
		Count		00	10	10
		Data		00	10	11
	11	Command Address	Multiplexor Channel	00	11	00
		Data Address		00	11	01
		Count		00	11	10
		Unit Address		00	11	11
Sector 01 Working Storage (16 Positions)		≈	≈	01	XX	XX
Sector 10 (16 Positions) Floating Point (8 Regs)		≈	≈	10	0X	XX
I/O Common Channel (8 Regs)		Not Used		10	10	00
		Not Used		10	10	01
		Not Used		10	10	10
		Not Used		10	10	11
		R Register Backup		10	11	00
		L Register Backup		10	11	01
		Interrupt Buffer		10	11	10
		Backup Buffer #3		10	11	11
Sector 11 Fixed Point Registers (16 Positions)		≈	≈	11	XX	XX

NOTE: For emulator format, see "Emulator Service Aids."


Sector
Word
0
1
2
3
4
5
4
2
1
4
2
1
(8) Gate Drivers
(8) R/W Drivers


AOB 8-11
RP2xx
CPU SP Bits
RP201
Chan SP Bits
RP211
Ovflo
RF001
F Reg
RFxxx
F Register Pos X (Storage Tgr)
Channel Storage Protect Bit x
CPU Storage Protect Bit x
OR
RP 221
400 ns Delay
Sample Protected Area
A
Protected Area Error (to Storage Protect Trap Latch KK621)
SPDR
P,0 3
MP 111
OEs (5)
MP 131
Timing
Strobe Inhibit
Read Gate
Write Gate
Select SP
Write Condition (Store 1)
N
Read Condition SP 26
SAR
20
19
18
17
16
15
14
13
RA xxx
SP Bits
1
2
4
8
16
32
64
*128
Processing Unit
Storage Unit
See Form Z22-2828, Model 50 Main Storage, for detailed information on storage protection.
* Model 2050 I only
(4)
(4)
VRef
Y Address Decode
MP 221
Y Address Decode
MP 211
Inhibit Gating
MP 261
Driver Gate Control
MP 251
Special -3.0v
RG (4)
WD (4)
RD (4)
WG (4)
Inhibit Drivers (5)
MP 261
(4)
(4)
Diode Matrix
(16)
(16)
Strobe Driver
Sense Level
Data Out
MP 231
X Address Decode
WD (4)
RG (4)
(16)
WG (4)
RD (4)
Diode Matrix
(16)
X Address Decode
MP 241
Sense Amps (5)
Storage Protect Array

2050 Model	Bytes of Main Storage	Positions of SP	X Address					Y Address			
			SAR	13	14	15	16	17	18	19	20
F	65K	32					16	8	4	2	1
G	131K	64	SP			32	16	8	4	2	1
H	262K	128	Bits		64	32	16	8	4	2	1
I	524K	256		128	64	32	16	8	4	2	1



READ-ONLY STORAGE

BINARY DECODE OF ROAR TO 1 OF 64 DRIVER LINES

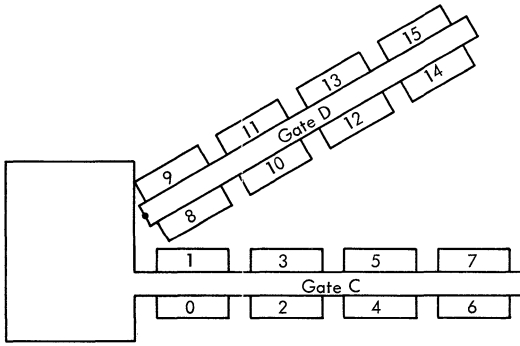
Base Addresses			First Drive Lines	Base Address		Second Drive Lines	Decoded Drive Lines	
BA0	BA1	BA2		BA3	BA4		No A Branch Bit	A Branch Bit
				0	0	SD0	Drive 0 P00-QP0	Drive 1 P00-QP1
0	0	0	FD0	0	1	SD1	Drive 2 P00-QP2	Drive 3 P00-QP3
				1	0	SD2	Drive 4 P01-QP0	Drive 5 P01-QP1
				1	1	SD3	Drive 6 P01-QP2	Drive 7 P01-QP3
				0	0	SD4	Drive 8 P02-QP0	Drive 9 P02-QP1
0	0	1	FD1	0	1	SD5	Drive 10 P02-QP2	Drive 11 P02-QP3
				1	0	SD6	Drive 12 P03-QP0	Drive 13 P03-QP1
				1	1	SD7	Drive 14 P03-QP2	Drive 15 P03-QP3
				0	0	SD8	Drive 16 P04-QP0	Drive 17 P04-QP1
0	1	0	FD2	0	1	SD9	Drive 18 P04-QP2	Drive 19 P04-QP3
				1	0	SD10	Drive 20 P05-QP0	Drive 21 P05-QP1
				1	1	SD11	Drive 22 P05-QP2	Drive 23 P05-QP3
				0	0	SD12	Drive 24 P06-QP0	Drive 25 P06-QP1
0	1	1	FD3	0	1	SD13	Drive 26 P06-QP2	Drive 27 P06-QP3
				1	0	SD14	Drive 28 P07-QP0	Drive 29 P07-QP1
				1	1	SD15	Drive 30 P07-QP2	Drive 31 P07-QP3
				0	0	SD16	Drive 32 P08-QP0	Drive 33 P08-QP1
1	0	0	FD4	0	1	SD17	Drive 34 P08-QP2	Drive 35 P08-QP3
				1	0	SD18	Drive 36 P09-QP0	Drive 37 P09-QP1
				1	1	SD19	Drive 38 P09-QP2	Drive 39 P09-QP3
				0	0	SD20	Drive 40 P10-QP0	Drive 41 P10-QP1
1	0	1	FD5	0	1	SD21	Drive 42 P10-QP2	Drive 43 P10-QP3
				1	0	SD22	Drive 44 P11-QP0	Drive 45 P11-QP1
				1	1	SD23	Drive 46 P11-QP2	Drive 47 P11-QP3
				0	0	SD24	Drive 48 P12-QP0	Drive 49 P12-QP1
1	1	0	FD6	0	1	SD25	Drive 50 P12-QP2	Drive 51 P12-QP3
				1	0	SD26	Drive 52 P13-QP0	Drive 53 P13-QP1
				1	1	SD27	Drive 54 P13-QP2	Drive 55 P13-QP3
				0	0	SD28	Drive 56 P14-QP0	Drive 57 P14-QP1
1	1	1	FD7	0	1	SD29	Drive 58 P14-QP2	Drive 59 P14-QP3
				1	0	SD30	Drive 60 P15-QP0	Drive 61 P15-QP1
				1	1	SD31	Drive 62 P15-QP2	Drive 63 P15-QP3

BINARY DECODE OF ROAR TO SELECT LINES

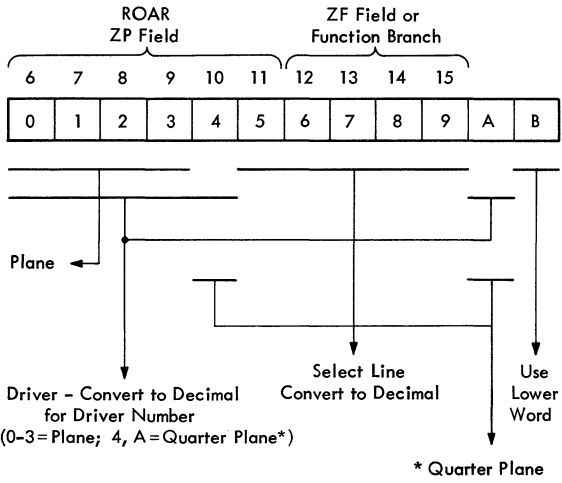
Select Lines	ROAR Positions				
	5	6	7	8	9
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	-	0	1	1	0
7	-	0	1	1	1
8	-	1	0	0	0
9	-	1	0	0	1
10	-	1	0	1	0
11	-	1	0	1	1
12	-	1	1	0	0
13	-	1	1	0	1
14	-	1	1	1	0
15	-	1	1	1	1
16	1	-	0	0	0
17	1	-	0	0	1
18	1	-	0	1	0
19	1	-	0	1	1
20	1	-	1	0	0
21	1	-	1	0	1

Select Lines 0-5 are decoded from ROAR Pos 5, 6, 7, 8, and 9
Select Lines 6-15 are decoded from ROAR Pos 6, 7, 8, and 9
Select Lines 16-21 are decoded from ROAR Pos 5, 7, 8, and 9

CROS PLANE LOCATIONS - TOP VIEW

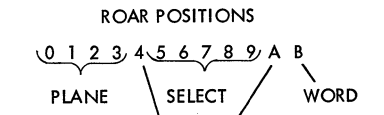


READ-ONLY ADDRESS REGISTER

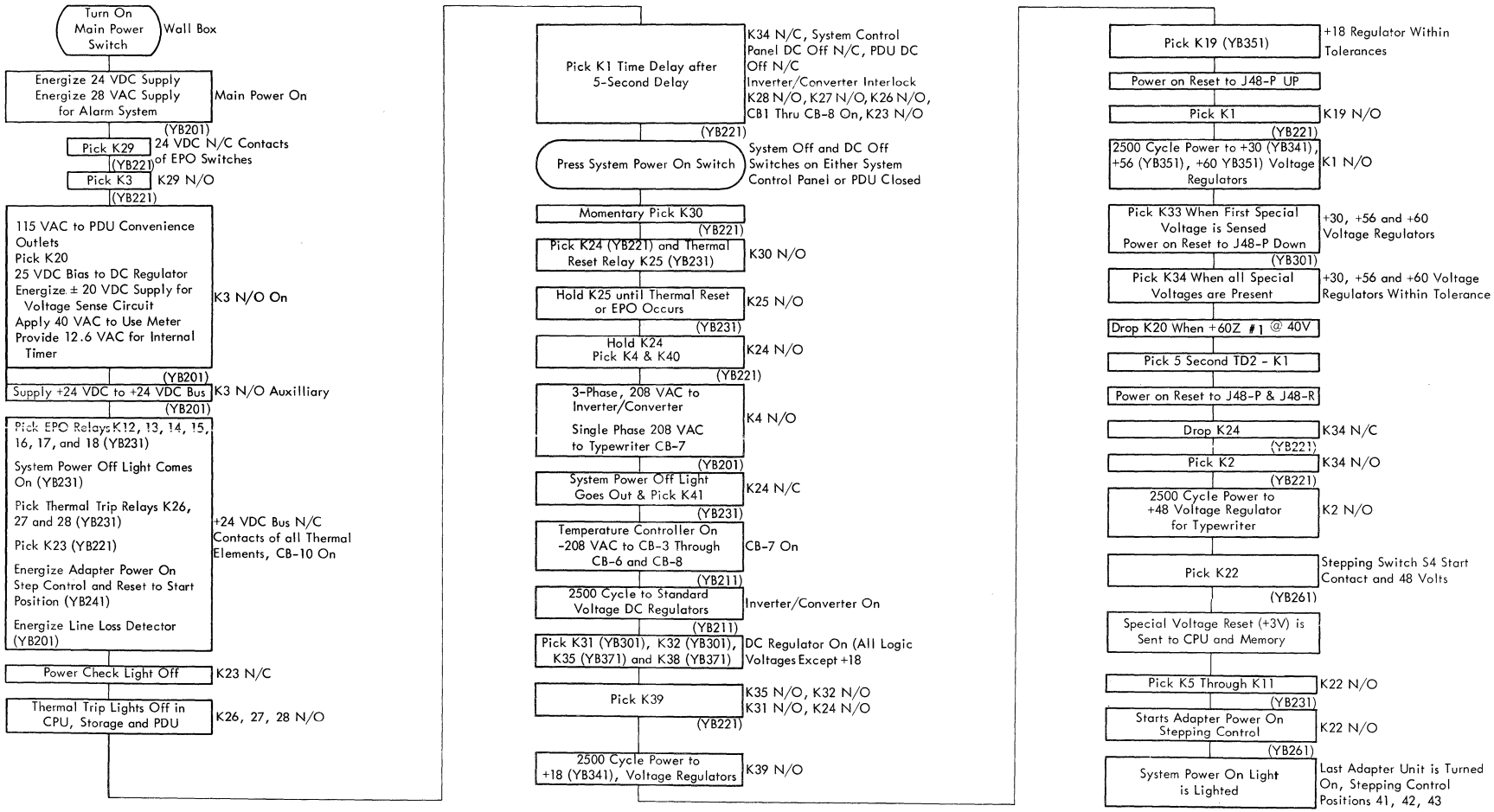


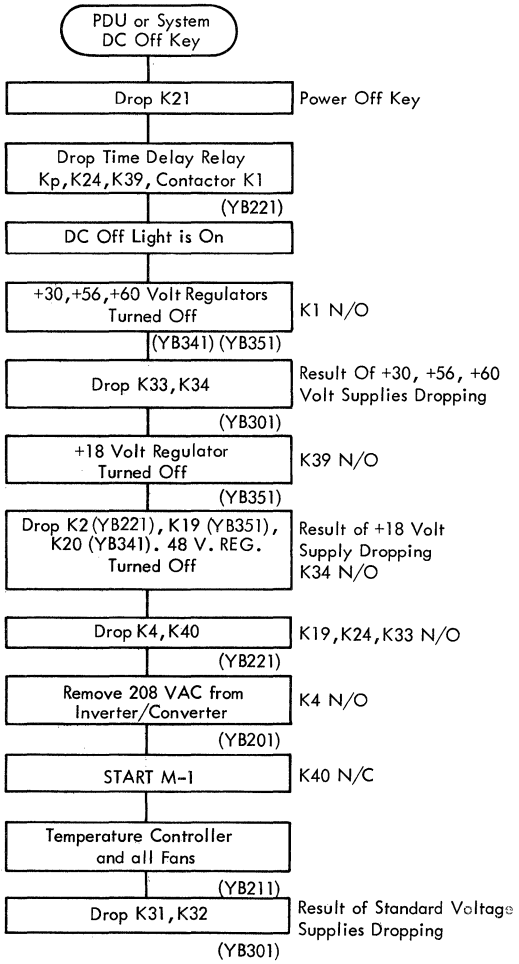
*Quarter planes are numbered left to right from pressure plate side

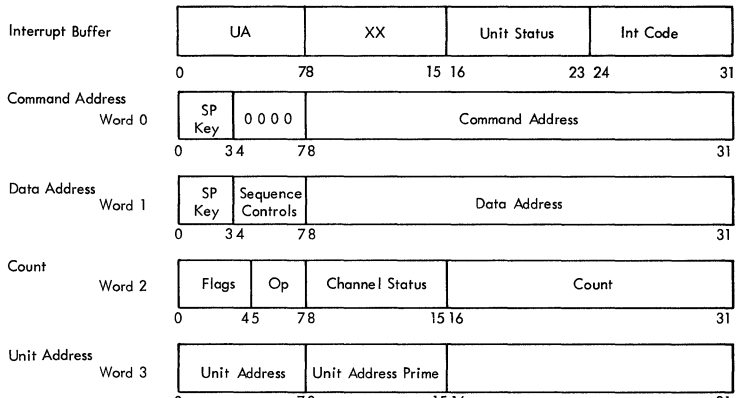
LOCATIONS OF CROS DRIVERS



GATE	PANEL	PLANE	Q.P.	SELECT	CARD LCN
C	D2	0,1	0	00-10	M6
C	C2	2,3		11-21	L6
C	B2	4,5	1	00-10	J6
C	A2	6,7		11-21	H6
D	A2	8,9	2	00-10	F6
D	B2	10,11		11-21	E6
D	C2	12,13	3	00-10	C6
D	D2	14,15		11-21	B6


Turn On Main Power Switch
Wall Box
Energize 24 VDC Supply
Energize 28 VAC Supply for Alarm System
Main Power On
(YB201)
Pick K29
24 VDC N/C Contacts of EPO Switches
(YB221)
Pick K3
K29 N/O
(YB221)
115 VAC to PDU Convenience Outlets
Pick K20
25 VDC Bias to DC Regulator
Energize ± 20 VDC Supply for Voltage Sense Circuit
Apply 40 VAC to Use Meter
Provide 12.6 VAC for Internal Timer
K3 N/O On
(YB201)
Supply +24 VDC to +24 VDC Bus
K3 N/O Auxilliary
(YB201)
Pick EPO Relays K12, 13, 14, 15, 16, 17, and 18 (YB231)
System Power Off Light Comes On (YB231)
Pick Thermal Trip Relays K26, 27 and 28 (YB231)
Pick K23 (YB221)
Energize Adapter Power On Step Control and Reset to Start Position (YB241)
Energize Line Loss Detector (YB201)
+24 VDC Bus N/C Contacts of all Thermal Elements, CB-10 On
Power Check Light Off
K23 N/C
Thermal Trip Lights Off in CPU, Storage and PDU
K26, 27, 28 N/O
Pick K1 Time Delay after 5-Second Delay
K34 N/C, System Control Panel DC Off N/C, PDU DC Off N/C
Inverter/Converter Interlock K28 N/O, K27 N/O, K26 N/O, CB1 Thru CB-8 On, K23 N/O
(YB221)
Press System Power On Switch
System Off and DC Off Switches on Either System Control Panel or PDU Closed
Momentary Pick K30
(YB221)
Pick K24 (YB221) and Thermal Reset Relay K25 (YB231)
K30 N/O
Hold K25 until Thermal Reset or EPO Occurs
K25 N/O
(YB231)
Hold K24
Pick K4 & K40
K24 N/O
(YB221)
3-Phase, 208 VAC to Inverter/Converter
Single Phase 208 VAC to Typewriter CB-7
K4 N/O
(YB201)
System Power Off Light Goes Out & Pick K41
K24 N/C
(YB231)
Temperature Controller On -208 VAC to CB-3 Through CB-6 and CB-8
CB-7 On
(YB211)
2500 Cycle to Standard Voltage DC Regulators
Inverter/Converter On
(YB211)
Pick K31 (YB301), K32 (YB301), K35 (YB371) and K38 (YB371)
DC Regulator On (All Logic Voltages Except +18
Pick K39
K35 N/O, K32 N/O
K31 N/O, K24 N/O
(YB221)
2500 Cycle Power to +18 (YB341), Voltage Regulators
K39 N/O
Pick K19 (YB351)
+18 Regulator Within Tolerances
Power on Reset to J48-P UP
Pick K1
K19 N/O
(YB221)
2500 Cycle Power to +30 (YB341), +56 (YB351), +60 YB351) Voltage Regulators
K1 N/O
Pick K33 When First Special Voltage is Sensed
Power on Reset to J48-P Down
+30, +56 and +60 Voltage Regulators
(YB301)
Pick K34 When all Special Voltages are Present
+30, +56 and +60 Voltage Regulators Within Tolerance
Drop K20 When +60Z #1 @ 40V
Pick 5 Second TD2 - K1
Power on Reset to J48-P & J48-R
Drop K24
K34 N/C
(YB221)
Pick K2
K34 N/O
(YB221)
2500 Cycle Power to +48 Voltage Regulator for Typewriter
K2 N/O
Pick K22
Stepping Switch S4 Start Contact and 48 Volts
(YB261)
Special Voltage Reset (+3V) is Sent to CPU and Memory
Pick K5 Through K11
K22 N/O
(YB231)
Starts Adapter Power On Stepping Control
K22 N/O
(YB261)
System Power On Light is Lighted
Last Adapter Unit is Turned On, Stepping Control Positions 41, 42, 43


PDU or System DC Off Key
Drop K21
Power Off Key
Drop Time Delay Relay Kp, K24, K39, Contactor K1
(YB221)
DC Off Light is On
+30, +56, +60 Volt Regulators Turned Off
K1 N/O
(YB341) (YB351)
Drop K33, K34
Result Of +30, +56, +60 Volt Supplies Dropping
(YB301)
+18 Volt Regulator Turned Off
K39 N/O
(YB351)
Drop K2 (YB221), K19 (YB351), K20 (YB341). 48 V. REG. Turned Off
Result of +18 Volt Supply Dropping K34 N/O
Drop K4, K40
K19, K24, K33 N/O
(YB221)
Remove 208 VAC from Inverter/Converter
K4 N/O
(YB201)
START M-1
K40 N/C
Temperature Controller and all Fans
(YB211)
Drop K31, K32
Result of Standard Voltage Supplies Dropping
(YB301)



Flags

0 CD
1 CC
2 SILI
3 Skip
4 PCI

Op

000 - Input Forward
001 - Input Backward
110 - Output Forward
011 - Input Skip
111 - Stop
100 - End Status AND Not WLR
101 - End Status AND WLR

Sequence Controls

0000 - Idle
0001 - Busy
0011 - CC End Read
0101 - Chan End in 1B
0111 - Chan End Qued
0110 - Device End/Attention in 1B

Channel Status

0 PCI
1 WLR
2 Program Check
3 Protection Check
4 Channel Data Check
5 Channel Control Check
6 Interface Control Check
7 Chaining Check

Interrupt Code

00 - PCI/Ch End
01 - PCI
02 - DE
03 - Chan End

* Only appears in local storage

Signal	W 0-7 Bits on the mover-out bus	CPU stats 4-7 Identifies the signal after the stat 3 relay	Function
Interrupt Test I/O	1000 0000	1001	Issued to the multiplexor channel for a device end interrupt. The channel will set the unit status in M (0-7). The unit address is in L (0-7).
Time-out Check	0100 0000	X X X 0	Issued when the channel fails to respond (in 8 cycles) to the time-out signal with a stat 3 reply (resets chan 0).
Time-out	0010 0000	X X X 0	Issued when the "153 countdown loop" counts to zero without a stat 3 reply.
Foul on Start I/O	0001 0000	0010	Issued when the CAW is invalid.
Test Channel	0000 1000	0000	Requests the common channel circuits to test the state of the channel addressed by bits 21-23 of the L register, and set the condition code to identify the state of the channel.
Test I/O	0000 0100	0100	Issued to initiate a channel routine to test the status of the I/O unit addressed by bits 21-31 of the L register. The channel either loads the R and M registers with CSW data, or sets the condition code.
Halt I/O	0000 0010	0000	Issued to halt the data transfer occurring in the I/O unit addressed by bits 21-31 of the L register. The channel either loads the R and M registers with CSW data, or sets the condition code.
Start I/O	0000 0001	0010	Issued to initiate the I/O command specified by the CCW-1 in the M register. The CAW is in the R register and the unit and channel address is in the L register.

Common Channel Decode Lines	Emit Field	Function
E⟶Ch Emit 0	0000	Selector channel interrupt routine in process. Generates an immediate stat 3 reply
E⟶Ch Emit 1	0001	Log reset. Resets the selector channel after a selector channel log-out
E⟶Ch Emit 2	0010	Gate Status. Gates the selector channel status to the CPU after a log-out
E⟶Ch Emit 3	0011	Sets the interface register
E⟶Ch Emit 4	0100	Sets the scan channel latch
E⟶Ch Emit 5	0101	Sets the log trigger
E⟶Ch Emit 6	0110	Resets the common channel and multiplexor channel after log-out
E⟶CH Emit 7	0111	Local store "Write DTC"
E⟶Ch Emit 9	1001	Proceed on Interrupt signal. Selector channel starts to load the L, R, and M registers with CSW data. Multiplexor channel generates an immediate stat 3 reply
E⟶Ch Emit A	1010	Selector channel end update test
E⟶Ch Emit 8	1011	High speed channel time-out

REPLIES (Different Combinations are Decoded by the Status of CPU Stats 0, 1, 2, and 3)

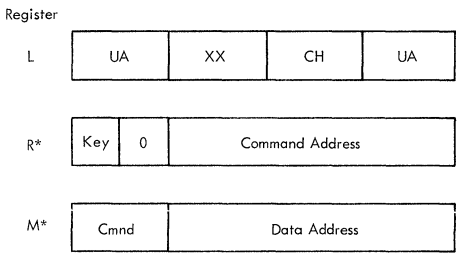
Request	X001	X011	X101	X111	Countdown/No Reply
Foul on Start I/O	The start I/O would not have been excuted because the subchannel is busy or unavailable. Don't recognize the invalid CAW as a program check. The CC is set to 2 or 3 and the microprogram returns to 1-fetch	not valid	The multiplexor channel requests a reset of the countdown. At the moment, the channel is working continously in multiplex mode	The path is available so the invalid CAW is a program error. Store a program check indication in the CSW, set the condition code to 01, and return to 1-fetch	The multiplexor channel is in burst mode, or a circuit malfunction may be causing the problem. A time out signal will be issued to see if the channel is operational
Start I/O	If 1001: The start I/O was initiated on the Mpx ch, and a device end type interrupt may have to be reset. CC is set to 0, 2 or 3. If 0001: The start I/O was initiated on a Sel Ch. CC is set to 0, 2 or 3. Return to 1-fetch	An immediate command has been executed, a malfunction has occurred, or the command was not accepted. The reason is indicated in the status of the CSW, the CC is set to 1, and the microprogram returns to 1-fetch		not valid	

Request	X001	X011	X101	X111	Countdown/No Reply
Test I/O	The condition code has been set to 00, 10, or 11; return to I-fetch	Load the CSW from the data in the R and M register, set the condition code to 01, and return to I-fetch	The multiplexor channel requests a reset of the countdown. At the moment, the channel is working continuously in multiplex mode	not valid	The multiplexor channel is in burst mode, or a circuit malfunction may be causing the problem. A time out signal will be issued to see if the channel is operational
Halt I/O	The condition code has been set to 00, 10, or 11; return to I-fetch	A multiplex operation has been terminated. Load the unit and channel status into the CSW, set the condition code to 01, and return to I-fetch		not valid	
Proceed on Interrupt	Mpx reply: If it was a device end type, issue Interrupt Test I/O If it was any other type, fetch the interrupt data from 'bump', store it in the CSW, and Trap to the new I/O PSW	Sel reply: Load the CSW from the data in the R and M registers, and Trap to the new I/O PSW		not valid	

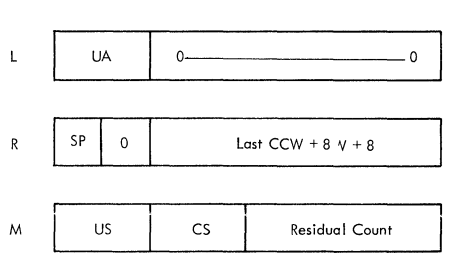
Request	X001	X011	X101	X111	Countdown/No Reply
Test Channel	The condition code has been set to 00, 01, 10, or 11; return to I-fetch	not valid	not valid	not valid	Refer to Sheet 1 or 2
Interrupt Test I/O	not valid	Mpx reply: Load the CSW from the data in the R and M registers and Trap to the new I/O PSW	not valid	not valid	The multiplexor channel is in burst mode. Reset the IB full stat and return to I-fetch
Time-out	The multiplexor channel is operating in burst mode, the condition code is set to 10 (2), and the microprogram returns to I-fetch	not valid	not valid	not valid	Circuit Malfunction Either log the error or store "Ch Ctrl Ck" in the CSW and set the condition code to 01 (Eight cycle) countdown)
Time-out Check	This is the "die" signal to the channel, and no reply is expected				

Legend: X..not important 0..stat is off 1..stat is on

Start I/O Register Setup

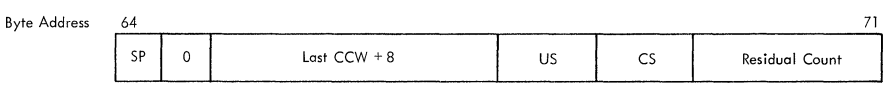


CSW Setup for Load 64



* Not used on Test I/O, Halt I/O, or Test Channel

Channel Status Word



Legend:
- CH = Channel
- CS = Channel Status Byte
- SP = Storage Protect Key
- UA = Unit Address
- US = Unit Status Byte

	Control or Data Error in CPU	Data Error in Channel	Control Error in Channel	Time Out	Time-Out Check
Normal Mode with PSW Bit 13=1	1. Error set into check reg 2. CPU and chan stop 3. CPU and chan are logged 4. Subchannel is reset 5. Machine check trap	Not applicable	1. Same as error in CPU	1. Mpx chan sets log request into CPU check reg 2. Same as error in CPU 3. If chan is unable to respond, then time out check will occur	1. Common chan sets log request into CPU check reg 2. Same as error in CPU
Normal Mode with PSW Bit 13=0	1. Error set into check reg 2. When PSW bit 13 goes to 1: a. CPU and chan stop b. CPU and chan are logged c. Currently operating sub-channel is reset d. Machine check trap	Not applicable	1. Error is set into check reg 2. Operation on subchannel is terminated by sel reset 3. When PSW bit 13 goes to 1: a. CPU and chan are logged b. Currently operating sub-channel is reset c. Machine check trap	1. Mpx chan sets log request into CPU check reg 2. Time out check will always occur	1. Common chan sets log request into CPU check reg 2. Set CC1 3. Load 64 with CCK 4. Operation on subchannel is terminated by sel reset 5. When bit 13 goes to 1: a. CPU and chan are logged b. Currently operating sub-channel is reset c. Machine check trap
Stop Mode	1. Error set into check reg 2. CPU and chan stop	Not applicable	1. Same as error in CPU	1. Mpx sets log request into CPU check reg 2. Same as error in CPU 3. If chan is unable to set check reg, then time out check	1. Common chan sets log request into CPU check reg 2. CPU and chan stop
Disable Mode	1. Error set into check reg 2. No indication to chan 3. Operation continues	Not applicable	1. Error is set into check reg 2. Subchannel is reset 3. Machine check trap (no log out)	1. Ignore time-out signal	1. Common channel sets log request into CPU check reg 2. Set CC1 3. Load 64 with CK 4. Operation on subchannel is terminated by sel reset

	Control or Data Error in CPU	Data Error in Channel	Control Error in Channel	Time Out	Time-Out Check
Normal Mode with PSW Bit 13=1	1. Error set into CPU chk reg 2. Ctrl chk sent to ext chan 3. Chan stops 4. CPU and chan in error logged 5. Chan reset 6. Mach chk interrupt	1. Chan stops at end of record with data chk in its status reg 2. When chan not masked, I/O interrupt occurs	1. Chan stops with chan ctrl chk or IF ctrl chk in its status reg 2. When chan not masked, a chan log out occurs 3. After log out, an I/O interrupt is forced 4. Chan is reset	1. Upon receipt of time out, chks for chan error conditions 2. If conditions exist, a chan log out is requested 3. After log out, CSW* is stored with chan ctrl chk or IF ctrl chk in chan status 4. Cond code set to 01 and chan reset 5. If error conditions not existing, time out chk occurs	1. Log request set into CPU chk reg Same as ctrl or data error in CPU
Normal Mode with PSW Bit 13=0	1. Error set into CPU chk reg 2. Log chan X latch in com chan set 3. No error signal sent to ext chan WHEN PSW BIT 13 = 1: 4. CPU and chan X are logged 5. Chan reset 6. Mach chk interrupt	Same as above	Same as above	Same as above	1. Log request set into CPU chk reg and chan stops with ctrl chk in status reg 2. Log chan X latch set 3. CSW* is stored and cond code set to 01 4. Chan is reset WHEN PSW BIT 13 = 1: 5. CPU and chan X logged 6. Chan is reset 7. Mach chk interrupt
Stop Mode or Chan Stop Mode	1. Error is displayed in CPU chk reg 2. Ctrl chk sent to chan 3. CPU and chan stopped	1. Channel stops 2. During initial selection, a log reg stops the CPU 3. After initial sel, if chan is not masked, a log req stops CPU	1. Channel stops 2. During initial selection, a log req stops the CPU 3. After initial sel, if chan is not masked, a log req stops the CPU	1. Channel stops 2. During initial selection, a log req stops CPU 3. After initial sel, if chan is not masked, a log req stops CPU	1. Same as ctrl or data error in CPU
Disable Mode	1. Error is set into CPU chk reg 2. No error signal sent to ext chan	1. Chan stops at end of record with a data chk in its status reg 2. When chan not masked, an interrupt is requested (Same as normal mode with PSW bit 13 = 1)	1. Chan stops with chan ctrl chk or IF ctrl chk in its status reg 2. When chan not masked, an interrupt is requested (Same as normal mode with PSW bit 13 = 1, except no log out)	1. Ignore time out signal	1. Log request set into CPU chk reg 2. CSW* is stored with status = chan ctrl chk 3. Cond code set to 01 4. Chan is reset

*Could be partial or complete CSW depending on op code.

Chan Read -- Data errors detected at the interface are corrected (parity inverted).

Chan Write -- Data errors detected at the interface are not corrected.

Chan Stop mode differs from stop mode in that the channel will stop on program, protect, and chain checks detected in channel in addition to above errors when in chan stop mode.

Syncs (All Plus)

CPU Zero	01C-C3G2D12(KC451)
Main Osc	01B-D2C5D12(KC451)
Reg Pulse	01C-C3G2D12(KC451)
Stg. Sel.	01A-B1E7D06(KC301)
	02A-A1H6G05(MA011)
Set SAR	01A-B1E5D12(KC241)
ROS Comp.	01C-A4E4D04(KK461)
IAR Comp.	01C-A4C2D04(KS651)
FLT Sync (Minus)	01BD1C3D10(KH331)
SAR Comp.	01CA4F3D09(PK011)

SAR Compare uses data Keys 8-31 and either/or both 0 for CPU, 1 for I/O plus the SAR Compare Switch.

Caution - Don't hit system reset while program is running - Hit Stop - then System Reset. Can put back bad parity in SP and M9. Hardstop may also!

Caution - If changing CPU timings pull cards at 01A-D4-H4 & G4 to prevent blowing fuses in Local Store.

Auto Recycle

To auto recycle a program by PSW Restart:

1. Jumper 01C-A4E4D07(KS651) (Minus on IAR Sync) to 01C-D3L4D12(KK701) (PSW Restart)
2. Set up restart in 0-7, and Address Keys = to IAR setting where desired to programs end.

IPL 1052

To IPL 1052 - read 24 bytes in: Ground 01C-D4C4B02

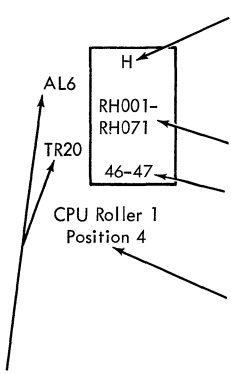
Error Interrupt

To tie down Error Interrupt A2B3D12 - Ground KT051).

FLT Hint

FLT's do not check L.S., Main Storage above 4K words, Sig. Protect and much of A and B branching.

ECAD Description



2 Name of Register: Self-Explanatory

4 Scoping Point: Refers to an entry in a test point table, from which scoping information can be obtained.

3 ALD Pages: Self-Explanatory

5 Log Out Location: Refers to the storage word(s) into which the register is logged on an error log out. This is a decimal word address.

6 Indication: Specifies where in the switchable indicators the register is displayed.

1 ROS Functions: Specifies the gating into the register. Enough of the control field specifications are reproduced to permit interpretation of the function. In this example, AL6 would be shown as IAR H(8-31), and TR20 would be shown as Latch H(0-31). Thus the two sources of input to the H register are the latch and IAR. By examining the ROS word in control during the error cycle, the source of the data in the H register can be pinpointed.

System Reset/Indicator On

Roller	Word	Indicators On
Mpx	4	Buf. 1 'P', Buf. 2 = Last Data Byte
	5	Bus Out 'P'
	6	Poll, Stat 3
Sel	1	B Reg 'P' Bits
	2	C Reg 'P' Bits
	3	Byte Cnt 'P' Bits
	4	Cycle Cntr. Stepping
	5	Pos Reg Tfr. SPDZ, Insn Scn, A Clock Stepping
	6	FIN
CPU # 1	1	L Reg = PSW Backup
	2	R Reg 'P' Bits
	3	M Reg 'P' Bits
	4	H Reg 'P' Bits
	5	SAR 17, Byte Sto. Sts, I/O & Byte Stats Unchng
	6	ROSDR = Halt Loop
CPU # 2	1	ROSDR = Halt Loop
	2	ROSDR = Halt Loop

3 Isylop, ILC = 1, Next ROAR = Halt Loop
4 I/O Reg 'P', RTL, D Byte = 2, M Byte = 7, Freq. Edit Stats - Carry = Unchanged
5 LSAR = 17, LSFN = 1, J = 7, Md = 3, G1&2 = S&P
7 Current ROAR = Halt Loop
8 Previous ROAR = Halt Loop

Indicators shown on all others are Off!!

Note: Storage Protect is untouched. If System Reset occurs in R1, R2 Time it will leave a core location empty, also S.P. will be empty.

Prevent Clock Stops

To prevent clock stop on disable ground A-A2B3D12(KT051).

Continuous Bump Reset

Continuous bump reset-tie down A Branch A-A3F6D07(KK211) keeps machine in system reset loop.

Biasing

Biasing machine affects FLT Hardware also, along with rest of CPU.

Tape Loading

To use FLT Load to load in regular tape, tie down 1BE1E4B02. This prevents ORing on FLT Load.

IPL ROS Hang Loops

988 Wait for channel response.
900 Channel Status bad.
919 Unit Status bad.
98C Start I/O not accepted by channel.

Line Locations

System Reset on QU100
Halt Loop QT200
Countdown Loop QK701

CAS - Edge Character Designations

A - Arithmetic Function
B - Mover Function

D - Data Flow not through Mover or Adder
L - Local Storage Data Flow or Addressing
S - Storage Control or Addressing
C - Miscellaneous Controls
R - Branching of ROS
Letter designation within CAS blocks:
A - SAR (start memory); D - SDR; G - length counters;
LS - Local Storage Data; LSA-L.S. Addressing:
U - Mover Entry Left; V - Mover Entry Right; W - Mover output latches to bus; T - Adder out bus latches;
IO - I/O Mode; WS1 - Working Storage (scratch pad) of Local Storage.

Control Field, Charts

CFC - Control Field Charts 100 series for CPU mode
200 series for I/O mode.

Word Maps

Word Maps on QZ pages.

CAS Page Index

Index of CAS pages in front of the Maintenance Manual (will fit in handbook).

Clocks

1. ROS controls sequencing of ROS.

2. MS controls hardware associated with MS and some FLT functions.

3. Free-running clocks: Error, Latch, Set LSAR R/W ROS Sense Amp Reset and Strobe, ROS Ingate Set.

4. Non Free-running clocks: Set Reg CPU, Set Reg ROS, Set Reg MM, Read/Write Sel.

I-Fetch Listing

I-Fetch CPU Status after 2nd level I fetch in back of RR, RX and RS, SI, SS books.

I-Fetch Levels

Two levels of I Fetch:

1. Format of Inst. by MO-3 to ROAR.

2. Op code by M4-7 to ROAR.

Bringup Aids (QW111)

ROS Repeat 202, then go to Normal Position

1. Repeats AK SAR (R.O. & R gen)
   AK IAR
   Data Keys L, R, H, M
   SDR, J (12-18) MD (8-11)

Note: For ZCT failures use this Rtne to load all Regs.

ROS 200 See Main Storage S.A.

ROS 201 See Local Storage S.A.

Special Voltages

Don't exceed 68 Volts for XY or Z.

Sense Amps

Sense AMP Card Part Number - 5804927

A. If swapped to locate a trouble, return to original position.

B. After replacement - check schmoo.

Shmoo

Shmoo - Do on installation - Factory chart on MA003

A. Check Each Month

1. Record temperature run console test switches for worst and reverse worst.

2. Plot a running shmoo.

3. Check with diagnostics 5393 and 5394 after shmoo. Only the corners need be checked with the diagnostics.

Temperature Compensation

Check by observing console meter XY then Z and pulling array fan (#1 Array) for each BOM.

Fans

On installation check all five fans on each BOM.

Bump

Bump - Tie down 01A - B1 H7 B12 (SAR Bit B)

BOM Switching

To switch 2 BOMS - On storage array panel 02A3D7 top half cable swap B03 and B04. Storage Select 1 and 2 (Use SLT Extender).

Power Drop

Dropping power while running storage tests may cause card failure.

ROS 200 Regeneration

ROS 200 Regenerates all through the storage

Caution - IAR will wrap around allowing select to 1 BOM only part of the time

Bad Parity

To scan for bad parity with check switch in stop position.

```
 0 - 00000000
 4 - 00000008
 8 - 41101004      LA1, 4 (0, 1)
 C - D2041000      MVC 0 (4, 1) 0 (1)
10 - 100047F0      BC X'F'8 (Op)
14 - 00080000
     GP - 1 should contain hex 18.
 On Stop - SDR is Bad Word
           SAR is Bad Word Address
 (Puts Good Parity in Memory on Regen.)
```

Write Consecutive Locations

To write into consecutive locations.

a. Cycle ROS Loop 200
   (D Keys D : IA+4 A, IA)

Write Desired Characters

To write any desired character and test consecutive locations in MS.

a. Load: GPR 1 with 01E
         GPR 2 with 001

   (To cycle same location set GPR 1 = 0.)

```
000 - 00000000  Start
  4 - 00000008  PSW
  8 - 92MM1000  MVI
  C - 91MM1000  TM
```

```
10 - 47100018   BC
14 - 00000000   Error
18 - 1A1247F0   ARBC
1C - 0008       BC
```

MM = Desired test character

If Error Stop - Examine R for Error Address.

Scope Bump Storage

1. To Scope 1 Word

WWW	83020F2A	Scan In L, R
	UA, UA, UA, UA	Bump Addr. Each Byte
	ZZZZZZZZ	Specified Data
	0400XXXX	Store Data to Bump
	0000XXXX	Read Data from Bump
	00001F72	Exit to I-Fetch
	47F00WWW	Branch to Begin

XXXX
1F6A for bump word 00
1E6A for bump word 01
1F68 for bump word 10
1E68 for bump word 11

UA = Unit Address

WWW = Starting Address of Program

Loop Sector From Bring-up Aid: (QW111)

1. Set Sector by executing: (ROS Repeat in Single Cycle)

   F51 - Sector 0
   F11 - " 1
   F00 - " 2
   F90 - " 3

2. ROS Repeat 201 (Data Keys to LS) This will ripple Sector.

Check For Parity Errors

To allow data keys to local store for any Sector (using Addr. Keys 32, 33) and check for parity error. Errors appear as half sum.

Caution - Any Interrupt results are unpredictable as PSW backup is affected if using Sector 1.

PROCEDURE:
1. Clear Storage to Parity Bits (ROS 200)
2. Disable Interval Timer
3. Check Control to Stop
4. Key In Program Below
5. Set IC to 500
6. Set Data Keys as Described
7. Set Sector in Addr. Keys 22, 23
8. Stop the machine with the Stop Key before changing data or Address Keys.

PROGRAM:

Location	Data	ROS-Page	Comment
500	83230191	191-QT200	Diag. PSS-SS
		18C	Gets LB to 2
504	86000416	20B-QT220	LCW - PSS-SS
		244,2C1,210-213	Addr. Keys to LSFN
508	E6000402	201-QW111	LCW PSS,SS
50C	E6000402	201-QW111	LCW PSS,SS
510	E6000402	201-QW111	LCW PSS,SS
514	00001F72	FB9	Go to I Fetch
518	47F00500	I Fetch	Branch

RESTART PROCEDURE:

1. Store Machine Ck Bit (13) on, Addr. 500 in Bytes 0-7.

2. PSW Restart

3. Check Validity of Stored Program

4. Coded New Machine Check PSW may be used if not rippling Sector 1.

Local Storage Heater

Scope cycle time on installation. Record it and the temperature coming into gate near local store, on M9 schmoo page.

Cycle Time Approx: 6 seconds on, 20 seconds off.

Local Storage Fuses

4192 Card - 3/10 AMP - P/N 492522
4469 Card - 3/4 AMP - P/N 492545

CAS - Edge Character Designations

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B - Mover Function
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Letter designation within CAS blocks:
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LS - Local Storage Data; LSA-L.S. Addressing:
U - Mover Entry Left; V - Mover Entry Right; W - Mover output latches to bus; T - Adder out bus latches;
IO - I/O Mode; WS1 - Working Storage (scratch pad) of Local Storage.

ROS Parity Errors

ROS Repeat - Error
FD5 0-30 Roller - Pos
FD6 31-55 CPU - 2-6
FD7 56-89

Ones and Zeros

F00 upper word all ones but 16, 24, 83
F03 lower word all ones but 16, 24, 83
F01 lower word all zeros but Parity (good)
F02 upper word all zeros but Parity (good)

ROS Address 000

ROS Addr. 000 has only bits 16, 35, 37, 38, 39, 50, 56 (ZN4) (AL23) (DG2)

ROS Loop

To determine a ROS address while in a loop without stopping the machine:

1. Set up scope to trigger on ROS Sync. (Sync box or Plus at 01C-A4E4D4)

2. Set assumed ROS address in Data Keys and watch for trace on scope.

3. Follow through CAS setting possible ROS addresses in Data Keys.

Recycle any Maint. Console PB Operation

1. Tie C-A4H2B3 (Manual Control Pulses SS) PK001 to A-A4E2D2. (60 cycle Int. Timer, KS252)

2. Depress PB to be tested and hold PB depressed as long as cycling is desired.

   Note: The 60 cycle Int. Timer pulse will fire the Manual Control Pulses SS and as long as any Maint. Console PB is depressed the operation will be restarted by the Pulse that updates the timer.

Check Channel Break in Operation

To check the functions of Channel Break In, continuously cycle address 000.

DTC's

DTC 1 370* Ingate (late reg.)
DTC 2 150* Outgate (reg set)
ITD's
1=65 (adj) 2 = 100* 3-100*

*Nanoseconds

Interface Register

The locations are given and present labels. The register positions will be changed to correspond to LCW bit positions.

LCW Bit	ALD Block	Present Name
0	KE841 - AT	Sim Sel In
1	" AR	Sim Op In
2	KE822 - AH	
3	KE821 - AT	Sim Pri 3 Ch 1
4	" - AR	
8 (IF Ctrl.)	KE701 - AD	Scan
9	" - AG	Channel Select
10	" - AJ	Channel Select
11 (CC Ctrl.)	KE721 - AN	Sim Pri
12	KE701 - AK	Reset
16	KE801 - BB	If Reg 0
17	" - BC	If Reg 1
18	" - BD	If Reg 2
19	" - BE	If Reg 3
20	" - BF	If Reg 4
21	KE811 - AW	If Reg 5
22	" - AX	If Reg 6
23	" - AY	If Reg 7
P 24-31	" - AZ	If Reg 8
24	KE831 - AL	Sim Req. In
25	" - AT	Sim Addr. In
26	" - AR	Sim Stat In
27	KE841 - AL	Sim Svc In

Manual Operation of Multiplexor Channel

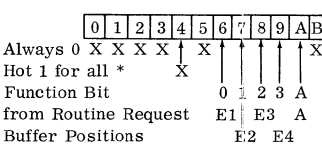
1. Place Channel Control switch to MPX.
2. Set IPL switches to address any unit on MPX Chan.
3. Push LOAD pushbutton.
4. Set the address keys for OP IN and ADDRESS In.
5. Set data keys (byte 0) to the unit address you have in the IPL switches (2 low order positions).
6. Hit ENTER pushbutton.
7. Set OP IN and STATUS IN in address keys. Set data keys off (up) and hit ENTER pushbutton.
8. Set OP IN and SVC IN in the address keys, and set some byte of data into byte 0 of data keys.
9. Hit ENTER. Notice that the data will be in Buffer 2.
10. Set SVC IN off and hit ENTER.
11. Repeat steps 8 and 9 for each byte of data.

Note: If you single cycle, you can observe the update of the data address and count as well as the passage of data bytes through CPU registers. The data byte you set up in byte 0 of data keys will appear in B.

Note: If, while you are single cycling thru this (or any other) routine, you wish to display local or main storage, you may do this by forcing ROAR to an address in the Halt Loop and hitting the start key then display what you want in the normal way. This method will leave your channel sequence intact. When you finish your display you need only force ROAR to the ROS address that was next in your single cycling.

Note: It is possible to IPL the 1052 by grounding 01C-D4C4B02. This will enable you to enter 24 bytes of data which will be the IPL PSW and the two pairs of CCW's.

ROAR Addressing for Multiplexor Channel



*Routine CO (PCI) starts at ROAR 002.
All other routines are from 80 to BE.

Unique Micro Orders for Multiplexor Channel

First Cycle - Send CK signal to Common Channel

BFR 2→BIB: OK
BFR 1→BIB: OK
BFR 2→BUSO: Gate BFR 1 to BIB then gate BFR 2 to Bus out.
BOB→BFR 1: Gate BFR 1 to BIB then BOB to BFR 1.
BOB→BFR 2: Gate BFR 1 to BIB then gate BOB to BFR2.
BUSI→BFR 1: Gate BFR 1 to BIB then gate BUS IN to BFR 1
BUSI→BFR 2: Gate BFR 1 to BIB then gate BUS IN to BFR 2
BIB 4, ERR→IOS:

Bus In Bit 4 IOS 'O'
Bus In Bit "0" or 2 or 3 or 6 or 7 or (bit 1 and not 5) to IOS "1".
IOS 1 On = Error

Bits Equal	5 = Dev. End
0 = Attn.	6 = Unit Ck.
2 = Ch. End	7 = Unit Excep.
3 = Busy	1 & 5 = St. Mod & Dev. E

Bit 4 = Channel End

1→PRI = End of Ch. Rtne. signal to the priority circuits

1→LCY - Signal of last cycle to priority circuits.

O, CH X→LSA - Means set LSAR to OOYYX with X equal to word 0-3. (00 to 11) and YY equal to 3 (11) for Multiplexor.

DTC1 Sets the Emit Field into the Branch Register.

DTC 2 does not.

Manual Operation of Selector Channel

1. Put Channel Control Switch to SEL.
2. Selector Channel display switch to Sel Ch 1 (2 or 3)
3. Set IPL address switches for any unit address and Channel 1 address.
4. Push LOAD pushbutton.
5. Set OP IN in the address keys.
   Set a unit address in byte 0 of the data keys.
   (It should match the IPL Switch Address).
   Hit ENTER pushbutton.
6. Push down the Address In Key, leave address in the data keys and Op In down, Hit Enter.

7. Set OP IN and STATUS IN in the address keys.
   Set all bits to zero in byte 0 of data keys, Hit ENTER.
8. Set OP IN alone in address keys. Hit ENTER.
9. Set SERVICE IN and OP IN address keys.
   Put all bits to 1 (down) in byte 0 of data keys.
   Hit ENTER.
10. Set OP IN alone in address keys. Hit ENTER.
11. Repeat steps 10 and 11 twenty three more times.
    This completes IPL twenty four bytes.
12. Set Up In and Status In.
    Set data bits 4, 5, on.
    Hit Enter (this enters ending status)
13. Set all data and other keys off.
    Hit Enter. This completes IPL.

ROAR Addressing for Selector Channel

	0	1	2	3	4	5	6	7	8	9	A	B
Always	0	X	X	X	X	X	X				X	X
From Address Reg. Pos.							0	1	2	3		

Selector Channel Routines

Rtne	Start Addr.	CAS	Rtne.	Start Addr.	CAS
S10	010 QV	100	End Up.	00C QV	106
T1C	02C	101	Intpt.	004	107
CCW1	028	102	LS Write	044	108
CCW2	030	103	LS rd	040	109
Wr. Fetch	020	104	UA Fetch	008	110
Rd. Store	024	105	Compare	014	111

Note: All routines are from 00B to 044.

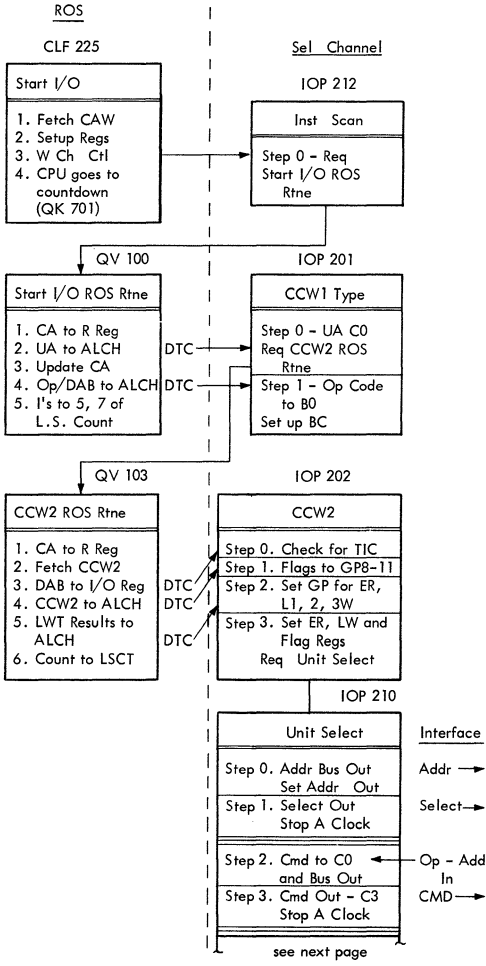
Selector Channel Log Word 4 Test

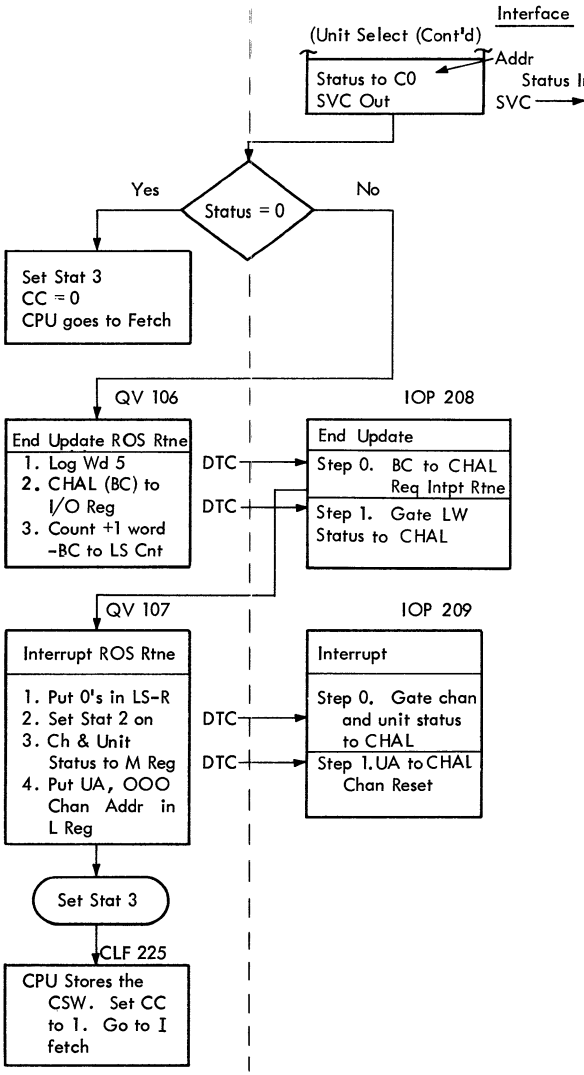
Compares the channel status to the ROS status in the AOB:

Chan Pos Reg	AOB Latch	ROS Bit	Micro Order
UA Fetch	P (0-7)	3	MD, F→ U
CCW1	0	1	L0 ——→ U
CCW2	1	2	R3 ——→ U
Unit Sel	2	Hardware	
Rd Store	3	4	BIB ——→ V
Wr Fetch	4	52	VL ——→ WL
End Update	5	53	UL ——→ WL
Compare	6	54	VR ——→ WR
Interrupt	7	55	UR ——→ WR

Cycle Counter	AOB Latch	ROS Bit	Micro Order
0	P (8-15)	46	BIB (0-3)→IOS
1	8	44	BIB (4-7)→IOS*E
2	9	45	BIB (4-7)→IOS
3	10	Hardware	

Selector Channel Start I/O




Interface
(Unit Select (Cont'd)
Addr
Status to C0
SVC Out
Status In
SVC
Yes
Status = 0
No
Set Stat 3
CC = 0
CPU goes to Fetch
QV 106
IOP 208
End Update ROS Rtne
1. Log Wd 5
2. CHAL (BC) to I/O Reg
3. Count +1 word -BC to LS Cnt
DTC
DTC
End Update
Step 0. BC to CHAL Req Intpt Rtne
Step 1. Gate LW Status to CHAL
QV 107
IOP 209
Interrupt ROS Rtne
1. Put 0's in LS-R
2. Set Stat 2 on
3. Ch & Unit Status to M Reg
4. Put UA, OOO Chan Addr in L Reg
DTC
DTC
Interrupt
Step 0. Gate chan and unit status to CHAL
Step 1. UA to CHAL Chan Reset
Set Stat 3
CLF 225
CPU Stores the CSW. Set CC to 1. Go to I fetch

Analyze Selector Channel Trouble

Difficult-to-analyze channel troubles may be simplified when using progressive scan by comparing the failing channel to a working channel. Assume we are working on a Selector Channel looping diagnose address Hex 1000 and syncing on ROS FC5:

1. Lift repeat inst. key.
2. System Reset (probably not necessary).
3. Store new channel number in 5011.
4. Put Hex 1000 in address keys.
5. Put IAR comp stop key down.
6. PSW restart.
7. Lift IAR comp stop key.
8. Put repeat inst. key down.

The same routine will now be cycling on the working channel and timings may be compared. The failing channel can be looped again by going thru the above procedure again storing the failing channel number back in 5011.

Note that PSW restart is to "Pick Up" the channel number change in 5011.

IAR comp stop is necessary because there will be no failure on the working channel so it would otherwise pass and continue running subsequent tests.

Random-Channel/Progressive-Scan Notes

When looping on prog scan diag address, lift the IAR repeat key to see the chan and common chan state at log out time.

Try addr stopping on ROS FC5 then go to single cycle and/or use clock stop, ITD stop keys etc. to observe chan operation. Look at "Time Cycle" on the scan print out. For example, if it is "2ND DTC of CCW2" ROS addr stop on the first ROS addr of the CCW2 routine can be used to evaluate the state of the chan and common chan. Single cycle may then be used to observe the failure.

Become familiar with the above procedure. Some troubles are isolated quickly when channel and CPU are stopped at the critical time so that the problem area may be scoped statically.

Feed Thru Capacitors

Regulator feed thru capacitors may short out inverter-converter fuses. If one fuse blows replace both. This condition may be caused by a bad card with a large heat sink (picks K2).

400 usec Square Wave

Adjust pot on Osc card for 400 usec square wave with highest amplitude. May be scoped with machine power off.

Open SCR

Test points on gate cards will indicate open SCR's.

Line Filters

If the line filters are open, they may cause intermittent errors. To scope 3 phase - TB3 pins 1-3 (Inverter-Converter).

512K Power On and Off

Hold the button until auxiliary power supply reacts.

Installation or P.S. Problems

Bring up power sequentially after removing J3, 4, 5, 6, from inverter-converter. Bring up power. Check for following regulators and voltages:

Reg	Voltages/Amps	Use	Feed Thru Capacitors	Load (See Note)
1	+6/.5	VAR (ROS)	C1, 2	25/25
1	+6/1.5	TC (ROS)	C3, 4	10/25
1	+6/2.5	ROS	C13, 14	5/25
2	+3/40A	Gate A	C18, 19	.5/100
3	+6/40A	Gate B,C,E Mem	C22, 23	1.0/100
4	+6/40A	Gate A, B,C	C31, 32	1.0/100
12	-18/11A	Gate C	C84, 85	5.0/100
10	-3/40A	Gate C, Mem	C68, 69	.5/100

Then drop power, connect J3, bring up and check for:

Reg	Voltages/Amps	Use	Feed Thru Capacitors	Load (See Note)
5	+3/40A	Gate B, C	C62, 63	.5/100
6	+3/40A	Gate C, E Mem	C70, 71	.5/100
7	-3/40A	Gate A, E	C78, 79	.5/100
8	+6 NON/HOA	Gate A, C Mem	C86, 87	1.0

Then drop power, connect J8, bring up and check for:

Reg	Voltages/Amps	Use	Feed Thru Capacitors	Load (See Note)
13	+18/11A	Mem	C88, 89	5.0/100

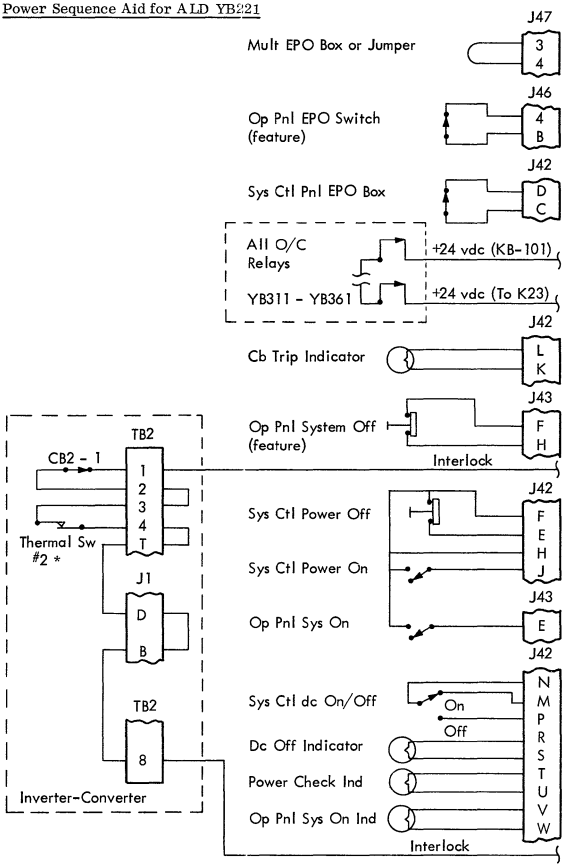
Reg.	Voltages/Amps	Use	Feed Thru Capacitors	Load (See Note)
11	+30	Gate A	C76, 77	25/100

Note: For initial installation, the ROS unit will run correctly at this time and the M9 Memory Select Pulse can be scoped. After this is checked, drop power connect J5, bring up power and check for:

Reg	Voltages/Amps	Use	Feed Thru Capacitors	Load (See Note)
14	+56XY/4A	BOM 1	C94, 95	50./100
15	+60Z/8A	BOM 1	C102, 103	50./100
16	+56XY/4A	BOM 2	C119, 120	50./100
17	+60Z/8A	BOM 2	C127, 128	50./100
9	+48/2A	Type	C56, 58	5.0/100

Note: These loads can be put on a regulator to test the output of the regulator isolated from the machine. Values shown are Ohms/Watts.

Power Sequence Aid for ALD YB221



* Does not indicate

Displaying or Storing

When displaying or storing from the console, the clocks must be running and the machine must be in manual mode (in the halt loop). The adder out bus is displayed in the B register, Roller 2, Side 1.

Main Storage

See "Display and Store Operations" in Appendix manual *.

To Clear Storage

Note: Termination must be as specified to prevent storing bad parity in storage protect.

1. Set Data Key 22 down (all others up).
2. Set ROS Repeat Switch Down
3. System Reset
4. Raise ROS Repeat Switch
5. Raise Data Key 22
6. ROS Repeat down to terminate
7. System Reset

Local Storage

See "Display and Store Operations" in Appendix manual *.

Bump Storage

See "Display and Store Operations" in Appendix manual *.

Note: System Reset will reset all of Bump Storage.

ROS

Display

1. Enter ROS address in Data Keys.
2. Rate switch to single cycle.
3. Push ROS Repeat Switch down.
4. Look at CPU roller 2, Row 1 and 2, CPU Roller 1, Row 6.

Set ROS Address

1. Enter desired ROS Address in Data Keys.
2. ROS Repeat Instruction.
3. Display next ROS address to check.

*Field Engineering Theory of Operation Manual, IBM System/360 Model 50, Appendix, Form Y22-2831.

Storage Protect

1. Set desired address in Address Keys 8-20.
2. Turn Storage Select switch to Storage Protect.
3. Push Display - Look at F Reg. (CPU-2 Row 4)
4. For Storing use Data Keys 28-31.

To Display or Alter the Working PSW

Refer to M50 Appendix Manual, Page 18

Miscellaneous Operations

To Set the Instruction Counter to Stop on an Instruc
To Reset an error indication.
(Refer to M50 Appendix Manual, Page 18).

To Stop on a SAR Address

1. Set Stop Address in Data Keys.
2. Set Data Key 0 down for CPU Mode.
   Set Data Key 1 down for I/O Mode.
   Both down for CPU or I/O Mode.
3. Set SAR Compare Switch to Stop.

Model 50 Diagnostics

5340 5341	Diagnose	Pt. 1 Pt. 2	Also exercise bump/LS
5342	CPU Error Ckts. (Needs scratch tape)		
5350	ROS Ripple Tape Generator		
5391	Main Storage - Addressing - Z Driver		
5392	Main Storage - Alt. Planes Discrim		
5393	Main Storage - Sense Amp Worst		
5394	Main Storage - Sense Amp Worst Modif.		
5395	Main Storage - Least ones, zeros		
5396	Main Storage - Half Select Beat		
5396	Main Storage - Random Number		
53C1	Local Storage		
53C4	Bump Storage		

5F80 SEREP

Note: 1. Look at Diagnostic Descriptions, volume 2, for a write-up on above and all CPU, Stg. Ptk., Int. timer, etc.
2. See Volume 1 - Diag. Desc. for Monitors - FOFF etc.
3. CEM Section 15, #4, contains an Index to all Diagnostics.

MIDAS Sense Switches

0	Paper Saver
1-4	Undefined
5-7	Isolation Num, 0-7
8	Isolate
*9	Analyze
10	Loop Isol Number in 5-7
*11	Terminate
12	Test Loader Device
*13	Load/Run Diagnostics
14	End Report Period
15	Extend Report

* Not currently available

Logout from Hardstop or Channel stop

1. Single Cycle *DO NOT change the Check Control Switch
2. Logout Pushbutton
3. Instruction Step
4. Start

Logout is now completed. SEREP can now be run to edit and print the Logout.

SEREP To IPL and Bypass System Reset

1. Disable Mode See note.
2. Rate switch to Process
3. Set ROS stop at 2AF
4. IPL SEREP
5. Single Cycle
6. Restore ROS stop
7. Set ROS address keys to 243 and ROS repeat switch on
8. Press Start
9. Restore ROS repeat
10. Rate switch to Process
11. Press Start

Channel Logout

To log a Selector Channel from a Hardstop the Channel Log Trigger. (Common Channel Roller - Row 3 - Right Side) must be on for Channel desired. Only 1 can be on for logout.

1. They can be set or reset by grounding:

Channel	Set	Reset	
1	B-C1H7B7	B-C1H5D4	KE651
2	B-C1H7B2	B-C1J6D6	"
3	B-C1H6D9	B-C1J6D10	"

Note: Setting on by this method doesn't turn on the indicator.

Important: PSW bit 13 must be on to logout the channel when it follows the CPU logout.

Local Storage Changes During SEREP

The following locations are changed in L.S. during a SEREP load.

Sector	Words
00	12, 13, 14, 15 MPX
01	1, 7, 14 (WS)
10	12, 13, 14, 15 MPX

SEREP Deck

In the card following the End card (control card) punch the following:

Cols:	1-4	=	Output Device
	5-8	=	Pseudo IPL Device
	10	=	Channel 0 *
	11	=	Channel 1 *
	13	=	Channel 3 *

*Channel Codes
0 = Low Speed Multiplex
1 = Storage Channel

4 = Low Speed Selector

= Not Attached

Note - To print the Selector Channel Logout Store a "1" in bit 12, 13, or 14 of hex location 44.

Error Logout

Error logout is in 3 parts:

1. Log SDR, SAR, IAR in Seq. Ctr. Mode.
2. Log ROSDR and ROAR in M.S. Mode.
3. In ROS Mode log 32 more words. See chart in Maint Manual.

FLT Op Reg controls the scan lines:
1. In M.S. mode Op Reg loaded from SDR parity bits.
2. In ROS mode Emit field and micro order loads it.

To check machine using FLT tapes:

I. Run hardware storage tests, all positions both for write and for read.

   A. Check FLT Op reg with all ones in storage. Turn Stg Test switch back to PROCESS. Op code F and step binary trigger.

II. FLT Tape One Main Storage Mode--Hardcore - ROS Bit

   A. Hardcore

      1. FLT Mode Sw. on Ld. and FLT Control Sw. to "Halt After Load".

      2. Check Control Sw. to Stop, Press System Reset.

      3. Press Load after setting switches to address of the unit having tape or disk.
         OBSERVE: IAR = 24, SEQ CTR. 1 & 2 on SEQ.
         Stat 3 on, SEQ, (Ring) CTR. Mode & Load on.
         (Load is successful)

      4. FLT Control Sw. to Process & Push Start
         OBSERVE 3 stops: (Force Indicators)

         a. CURRENT ROAR is FD5 & HARDSTOP lite on
         b. CURRENT ROAR is FD6 & HARDSTOP lite on
         c. CURRENT ROAR is FD7 & HARDSTOP lite on
            (3 ROS words with Bad Parity)

      5. Push Start - Stop with SDR = PFF $\overline{p}$FF PFF PFF

   B. ROS Bit Tests (Runs about 3 minutes)

      1. Entered by pushing Start after correct stop at item 5 above.

      2. Stop. CURRENT ROAR is FD5 and HARDSTOP. Set Check Control Sw. to Disable.

      3. Push Start, correct end stop is SDR = PFF $\overline{p}$FF PFF PFF

      ERROR: For an ERROR Stop, SDR 16-19 tells whether bit expected is a 0 or a 1; SDR 24-31 tells which ROS bit; SDR 0-11 or 1-12 tells the ROS Address depending on EC Level.

NOTE: FLT 01-01 is listing for MAIN STORE HC.
FLT 04-01 is listing for MAIN STORE ROS bit tests.
(In Instructional Diags. or Vol. 31)

III. FLT Tape Two--ROS Mode Hardcore - Zero, One Cycle Tests

A. Hardcore

1. FLT Mode Sw. on Ld. FLT Control Sw. to Halt After Load.

2. Check Control Sw. to Disable and then; System Reset Load.

3. Stop. IAR = 3FFC, SEQ. CTR. 1 & 2 on, SEQ. Stat 3 on.
SEQ. (Ring) CTR. Mode & Load Light on.

4. Put FLT Control Sw. to Process.

5. Push Start. Stop IAR = 0490; SDR=PFF p̄FF PFF PFF.
The Fail Trigger and the Binary Trigger should be on.

6. Push Start, GO TO: B

B. Zero Cycle Tests

1. Should run to completion of ZCT and 1CT without stops.

Error: SDR 16-19 = 0 (Segment #) SDR 7 = 1 (Term. Bit)
SDR 20-31 = TEST Number used to refer to Zero
Cycle Test listing. (Inst. Diagrams or Vol. 31)

C. ROS Mode One Cycle Tests

After the ZCT's run, the 1CT's should run to the end of the tape without stopping. SDR = PFF pFF PFF PFF

Error: SDR 16 - 19 $\neq$ 0 (Segment #) SDR 7 = 1 (term)
SDR 16 - 31 = SCOPEX Information
(20-31 = Test Number)

To repeat a test after a Termination Stop, FLT Control Sw. to Repeat. Push Start.

1. Get proper segment and Page using SDR 16-19 for segment + SDR 20-31 for test.

2. Top Line - AA Pt. Locate Ald page and set up scope with sync on FLT sync. looking at Clock Pulse (Reg Time) that is setting the output latch. (Will be within 1 us from sync.)

3. Look at pin ref for proper level (1 or 0) states for A, B, C, or D with reference to time.

4. If incorrect, check entries for state given (1 or 0) during time.

5. If entries OK - Go back to "Fed By" inputs for top line. Check "G/F" (good fail) labeled pins first.

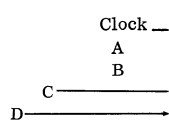
6. Follow thru until a good or correct pin is found. The failure is in the previously checked circuit.

Note: See next page for Scoping.

a. This allows a dynamic scoping of the test:

(1) Sync = on FLT CYCLE SYNC (sync box)
(if no sync box; Minus at B-D1C3D10 (KH331)

(2) Compare with clock on the PH circuit listed as the AA line of the SCOPEX list:



Note: The clock pulse will be within 1 microsecond of the FLT sync pulse.

FLT SYNC PULSE

b. To scope statically after stopping on an error:

(1) Set ROAR Address to Data Keys 20-31
For 1CT (segments 1-3, 5, 7) use Current ROAR
For 2CT (segments 4, 6) use Previous ROAR

(2) Set ROS Address Compare Sw. to Stop, FLT Control Sw. to Repeat, Push Start.

Note: The current and previous ROAR freeze the address of ROS from the 12th word setup. (LCW)

To check the result of the SCAN IN before allowing the ROS unit to cycle from the 12th word setup. ROS compare stop with F49.

To check the actual response after doing the SCAN OUT, ROS compare stop on F4F. Look at SDR.

If tests stop with no Termination Bit:

1. If IAR is less than 148 refer to the program listing as this means a load or Main Storage Mode error.

2. If the IAR is greater than 148, location 84 (hex) in memory contains the address of word 15 in the last test executed.

FLT Zero and One Cycle Test

Segment	Function
0	Zero, Cycle Tests
1	L, F, I/O, Carry Stat, PSW 32-39, LB, MB, MD, WFN
2	R, H Regs, GP Stats, ERROR (1/2 Sum)
3	M Reg, G1, G2, J Reg, L Sign, 1 Syl. Op. Refetch, Error U. V
4	ERROR (full sum, carry, mover out (2 cycle)
5	LSAR, LSFN
6	ROAR (2 cycle)
7	Misc. ERRORS (LB, MB, MD, G1, G2, LB & MB Parity)

FLT Zero and One Cycle Test Format

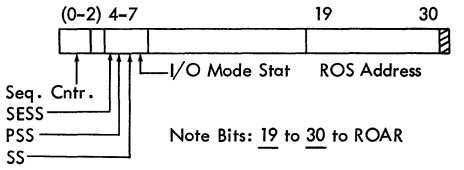
This shows the 1st and part of the 2nd test of every record.

Core Loc.	Test Word	Description
148	1	
14C	2	
150	3	
154	4	These 11 words of SCAN IN Data refer to SCAN in
158	5	IN chart on page of the Maint. Manual for the
15C	6	word and bit destination.
160	7	
164	8	
168	9	
16C	10	
170	11	
174	12	Bit 0-2 4 5 6 7 See Dest. - Seq. Ctr. SESS PSS SS I/O Tgr. ROAR (note)
178	13	Address of Actual Response (In Logout Area)
17C	14	Core Address of word 15 (180 in this test)
180	15	Mask
184	16	Expected Response (either 1's or not all 1's)
188	17	Address of start of this test - 148
18C	18	Address of start of next test - 1A0
190	19	Termination bit and SCOPEX information
194	20	Start addr. of this test - 148 - This is used on Start, after an error stop.
198	21	Start addr. of next test - 1A0 - This is used on FORCE PASS and Start (twice)
19C	22	Test Number and Segment Number (data only)
		Test Number 2
1A0 to 1C8		11 Words Scan in Data for Test 2

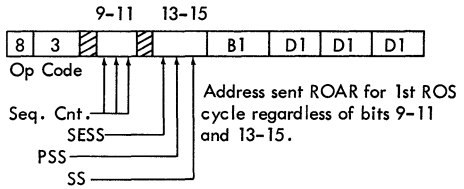
Note: At term, stop, the ROAR Current (for 1CT) has the ROS block cycled, and the ROAR previous has the 1st cycled block for 2 cycle tests.

LCW

Fetched from Main Store by ROS on QY110. Used as a Diagnose without I fetch.



Diagnose



SS Bit On = Set Seq. Cntr. to comp. of bits 9-11
When Seq. Cntr = 7 force ROAR to 2C0.
Note: SS on, Bits 9-11 = 0 causes 8 ROS Cycles

SS Bit Off = Go to first Addr. Spec. and continue under ROS c.

SESS On = Allow storage changes blocked by SS.

SESS Off & SS On = No change to: SAR, SDR, IAR, or PSS Tgr. by any micro order.

PSS Bit sets PSS Tgr. for micro program branches.
Note: PSS Trg. turned off by a branch except SS on, Not SESS.

FLT Load Problems

If SEQ Stat and SEQ CTR are as follows, the problem is: (Fig. 24 MM)

SEQ Stat	CTR	Problem
1	0	Fail to Reg PRI-3 SIO
1	5	No CCW 2 or RD Store Reg.
2	3	No "Status = Zero"
2	4	No End Update or RD Store/CCW 2
2	7	Int Rtne Req
3	6	No W2
3	4	No RD Store Reg (odd # of words)

FLT Load Check or Halt After Load

Unit and Channel Status displayed in CPU Roller # 2

Left Side as shown below:

Unit Status

Attn	Stat Mod	C U End	Busy	C E	D E	Unit Chk	Unit Exc

Channel Status

PCI	ILI	Prog Chk	Prot Chk	Ch Data Chk	Ch Ctrl Chk	IF Ctrl Chk	Chan Chk

1. CE, DE, and ILI are normal.

2. Tape Read Failure would be indicated by CE, DE, Unit Chk and ILI.

3. Data Failure in the Channel would be indicated by CE, DE, Chan Data Chk, and ILI.

4. FLT Load Check with the normal status of CE, DE, and ILI would indicate an error on the data lines where they are parity checked between channel and SDR. Note that FLT load uses a data path from channel to SDR that is parity checked as opposed to the CH-AL path used on normal channel operations.

Note: While Single Cycling Prog. Scan place FLT load switch to Normal.

Multiplexor Progressive Scan

I. Check Control Sw. to DISABLE FLT Mode Sw. to FLT load. Disable interval timer. System Reset. Push LOAD. At stop IAR = 800, press START.

II. STOP and IAR = all 1's is option WAIT state. Core 5010 is normally all 0's set to 0200xxxx to select series xxxx set to 0600xxxx sel. series, and ignore errors. Interrupt to continue from WAIT state.

III. Testing begins. Series 4-9 is HARDCORE. An ERROR enters a display loop. Fail tgr. ON. The L Reg. = Series (12-19), Rtne (20-23) and Test (24-31). Pressing START enters Log word display loop:

SEQ. CTR. = Log word number see MC003
FAIL TGR. = On if test failed
L Reg. = Exclusive OR of actual and the expected response bit on is pointing to an error position)
R Reg = Expected response, 1 or 0 in each position
SDR = Address of the DIAGNOSE used in the failing test. Place Diagnose Address in ADDRESS Keys, put on Repeat IAR, System Reset to loop on test.

To scope use FC5 as ROS SYNC (01C-A4E4D04 +)

IV. To leave a display loop; lift Repeat IAR (if on), FORCE PASS and START. Should go to the WAIT state:

1. IPL (FLT Mode to LOAD) to call next record.

2. PSW RESTART repeats tests in core up to the failing test.

3. Interrupt PB continues with the next test.

V. End of PROGRESSIVE SCAN: SDR = all 1's, IAR = 00FFF NORMAL IPL will rewind the tape.

Selector Channel Progressive Scan

The following operating procedure will:

1st Portion - Run all tests and print pass or fail for each rtne. (You can now eliminate known failing tests such as those for sel. chan. 2, etc.)

2nd Portion - Run all tests again and print 1st error of each rtne. and loads next routine. (You can now select the "best" failing routine to work with) and ---

3rd Portion - Loop the selected failing routine and bypass error prints and waits (for scoping).

Things to Remember:

To rewind tape - perform Normal IPL
The leftmost column of the test ID#
E - Designates Hardcore test;
C - Designates common channel tests;
and any number in that column designates a selector channel test. Machine check lite is normal.

Operating Procedure:

1st Portion

1. Place check control switch to disable & FLT mode to load.
2. Load & Ready the Sel. chan. prog. scan tape.
3. Set Load switches to desired unit and Press load.
4. System may stop at hex 100 (due to manual state before LD) If so, press start.
5. Message will print on typewriter (assuming your address 01F)
6. Set 66D0 in address keys and desired printer address in data keys 16-31 and store it.
   (6F03 at EC 256458 and higher)
7. Now set 5010 in address keys and 050Y0000 in data keys and store. (Y = channel # - i.e. 1 for sel. chan. 1)
8. Press start and interrupt.

9. Options will print out - press interrupt.
   Correct Stop - SDR Equals All Ones

2nd Portion

10. To Print Errors - Rewind Tape and repeat steps 3 thru 9, but in step 7 instead of storing 050Y0000 into 5010, store 060Y000 into 5010.

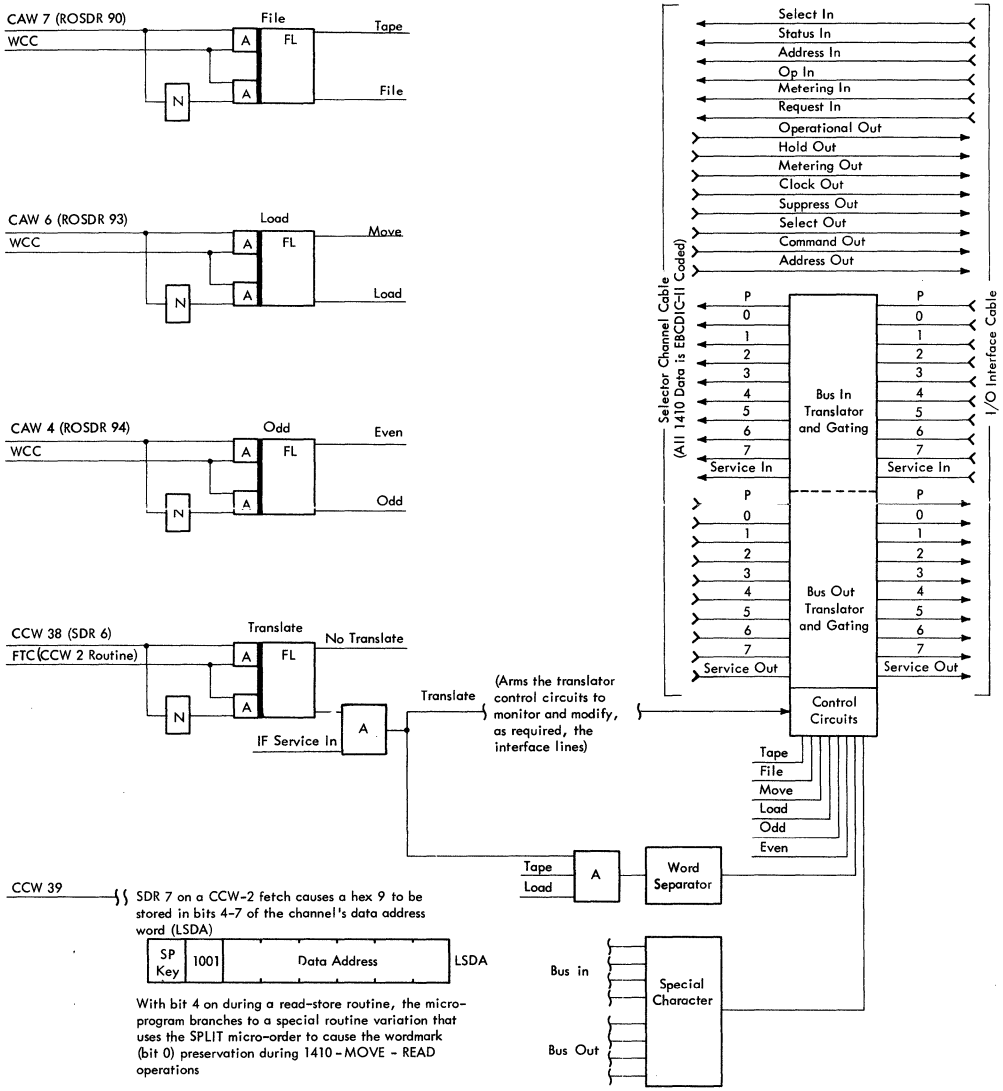
3rd Portion

11. To Scope Failure - Rewind tape and repeat steps 3 thru 9. This time in step 7, we must store 0204XXXX into Loc. 5010 When error is reached and we start printing, then stop CPU and put address of diagnose instruction into the address keys and put the "Repeat IAR" switch down. (The Adr. of the Diag Inst. was found in Step 10) (XXXX = the Failing Routine) (Sync Point = ROS ADR FC5)

Local Storage Assignment Map

Address Binary Sector	Word	Location Name	Byte 0	Byte 1	Byte 2	Byte 3
1	E	WSE	Operation Buffer for Normal Model 50 I-fetch (not for 1410-7010 I-fetch)			
2	0	FPR 0		Starting Address of 1410-7010 Core Storage		
2	1		Number of tables	Starting Address of the Device Table		
2	3	FPR 2	Base Address of the Linkout Table			
2	5	FPR 4		Base Address of the Linkout Table		
2	6	FPR 6	(Used to Load PSW 0-31 During a Linkback)			
2	7		(Used to Load PSW 0-31 During a Linkout)			
2	8		R-Register Backup			
2	9		L-Register Backup			
2	A		Interrupt Buffer (Mpx Ch)			
2	B		Backup Buffer 3 (Mpx Ch)			
3	3	GPR 3	System Byte	"Y" Op Indicators	"J" Op Indicators (I/O)	"J" Op Indicators (CPU)
3	4	GPR 4	Current d-Modifier	Channel 1 Status	Channel 2 Status	Channel 3 Status
3	5	GPR 5	Communication Byte	Working IAR (for Linkout)		
3	6	GPR 6	Zero	AAR		
3	7	GPR 7	Zero	BAR		
3	8	GPR 8		Original IAR (for I/O, E, and S/360 Exception Linkouts)		

CAW and CCW Control for 1410 I/O Operations



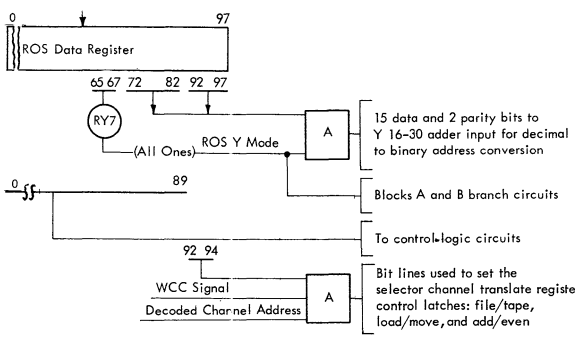
Name	1410/7010 Graphic	EBCDIC-II Code	Length	Execute	
				Micro-Program	Emulator Routine
No Operation	N	D5	any	(1)	
Add	A	C1	1, 6, 11[2]	X	
Subtract	S	E2	1, 6, 11[2]	X	
Zero and Add	?	C0	1, 6, 11[2]	X	
Zero and Subtract	!	D0	1, 6, 11[2]	X	
Multiply	@	BC	1, 6, 11[2]	X	
Divide	%	AC	1, 6, 11[2]	X	
Compare	C	C3	1, 6, 11[2]	X	
Set Wordmark	'	AB	1, 6, 11[2]	X	
Clear Wordmark	¤	8C	1, 6, 11[2]	X	
Clear Storage/Clear Storage and Branch	/	E1	1, 6, 11[2]	X	
Edit	E	C6	1, 6, 11[2]		X
Zero Suppress	Z	E9	1, 6, 11[2]		X
Branch if Character Equal	B	C2	1, 6, 12[2]	X	
Branch if Bit Equal	W	E6	1, 6, 12[2]	X	
Branch if WM and/or Zone Equal	V	E5	1, 6, 12[2]	X	
Branch on C bit	≠	E0	1, 6, 12[2]	X	
Table Lookup	T	E3	1, 6, 12[2]	X	
Move Data	D	C4	1, 6, 12[2]	X	
Test and Branch	J	D1	1, 7[2]	X	
Branch on Channel 1 Status	R	D9	7[2]	X	
Branch on Channel 2 Status	X	E7	7[2]	X	
Branch on Channel 3 Status	3	F3	7[2]	X	
Priority Test and Branch	Y	E8	1, 7	X	
Store Address Register	G	C7	7	X	
Store or Restore Status	$	9B	1, 7	X	
Halt/Halt and Branch		8B	1/6		X
Read or Write without Wordmark	M	D4	10		X
Read or Write with Wordmark	L	D3	10		X
Unit Control	U	E4	5		X
Stacker Select and Feed	K	D2	2		X
Carriage Control	F	C6	2		X

Note 1:
Stays in 1410 I-fetch and scans the succeeding characters until the next wordmark character is detected (the next op code)

Note 2:
Indicates the instruction length for which a 1410 priority interrupt can occur

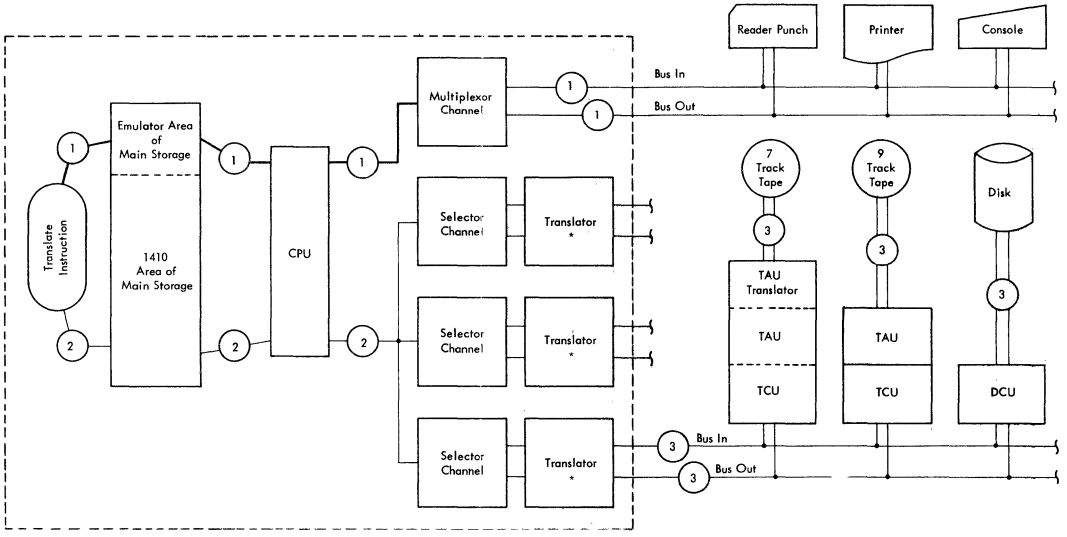
1052 Print-out ID	Function Emulated
E	1410 Error Halt
R	Reply (Console Write)
S	1410 Programmed Halt
1052 Key Depression	**Emulator-Simulated 1415 Console Function**
A	Alter 1410 Storage
B	Address Set (IAR only)
D	Display 1410 Storage
I	Inquiry Request (Console Read)
S	Console Stop Key
2	Console Start Key
3	Alter I/O Configuration Table
4	Program Reset
5	Computer Reset
5 (Alt code)	Release
0 (Alt code)	Cancel

Data Flow for the Additional CROS



Mirco-Order	CROS Field and Bit Value	Description	Mode	ALD Page
	72-77	A Branch Field		
AWB0	001011	A-branch if mover-out bus bit zero is a 1-bit	CPU	
AWB1	001111	A-branch if mover-out bus bit one is a 1-bit	CPU	
AWB23	100110	A-branch if mover-out but bits two and three are 1-bits	CPU	
AR4	111110	A-branch if R-register bit four is a 1-bit	CPU-I/O	
	84-89	Stat Setting Field		
SPLIT	000001	Split main storage cycle control for 1410 wordmark preservation. Storing a byte while regenerating bit zero (wordmark bit)	I/O	
IRSM	000010	Invert the R-sign stat if mover out bus bits two and three are 01	CPU	
	68-70	Selector Channel Adder Latch Tests		
FTC	010	SDR bit six to channel translator control, during a sel ch CCW-2 routine	I/O	
	4-5	Mover Right Input		
R3V	11	R-register bits 24-31 to the V-input of the mover	CPU	
	83-54-55	Mover Action-Right Digit		
ADDR	100	Add the U and V inputs to the one-digit adder	CPU	
SUBR	101	Complement the U-input and add to the V input in the one-digit adder	CPU	
SRIV	110	U 4-7 to W 4-7; if U 4-7 is greater than 9, turn on the R-sign stat. If U 4-7 is 9 or less, do nothing to the R-sign stat	CPU	
	65-67	Adder-Right Input		
ROSY	111	Gate ROSDR bits to the adder's Y-input (bits 16-30). Also inhibits normal condition branching because the A-branch and B-branch fields are used for the Y-input	CPU-I/O	
	40-43	Gates ROSDR bits 92-94 to the sel ch translate reg latches, in addition to its normal		
WCC	0111	function	I/O	

Data Flow Paths and Coding for 1410 I/O Operation



——— Multiplexor channel data flow

——— Selector channel data flow

1 EBCDIC code under emulator program control

2 EBCDIC-II (the 2050 coding for 1410 characters)

3 See the tables. The interface and device coding for 1410 data is under selector translator or TAU translator control

* The translators do not change the data coding if they are inactive. The translators are activated when the emulator program uses the special start I/O instruction (a diagnose kernel) in conjunction with special coding in the CAW and CCW to control the specific type of code translation

The CAW preconditions the translator as follows:

CAW 4-7	Function	
0100	Tape move mode, even parity	For 7 track tape, the TAU translator must be preconditioned with a mode-set command
1100	Tape move mode, odd parity	
0110	Tape load mode, even parity	For 9 track tape, the interface code is the device code
1110	Tape load mode, odd parity	
0101	Disk move mode (even)	
0111	Disk load mode (even)	

xxxx --(all other coding combinations are invalid when used with the diagnose start I/O, and result in issuing the "Foul on Start I/O" signal to the channel

Each CCW further controls the translator in conjunction with the preconditioning of the CAW as follows:

CCW 38-39	Function
00	No translation
01	Undefined
10	Load mode read (tape or disk)
11	Move mode read with wordmark preservation (tape or disk)(or, depending on the I/O operation) Write translation

The CCW control must be consistent within data chained CCW's but can change during command chaining, Turning the translator on/off under CCW control permits mixing System/360 code and 1410 code on the interface and is useful during disk operations

The translators also perform the wordmark insert/delete function for load mode operations with tape

Additional Micro Orders

Mnemonic	CROS Field and Bit Value	Description
	72-77 (AB)	A-Branch Field
RD7 = 9	001011(AB11)	Set A bit to 1 if digit 7 of R reg equals 1001.
EMSTAT	001111(AB15)	Set A bit to the value of the emulator stat.
L(22)	101000(AB40)	Set A bit to the value of L reg position 22.
W(6) → A, 1 → B	110001(AB49) and BB = 00001(BB1)	Set A bit to the value of mover bit 6. Set B bit to 1.
W6 → A, W7 Ω S2 → B	110001(AB49) and BB = 00100(BB4)	Set A bit to the value of mover bit 6. Set B bit to the OR of mover bit 7 and stat 2.

	94-96(EE)	Emulator Address Scrambler, Data Converter
L01 → S	001(EE1)	L reg bytes 0, 1 to address scrambler; address scrambler to AOB(8-31).
L23 → S	010(EE2)	L reg bytes 2, 3 to address scrambler; address scrambler to AOB(8-31).
L23 → S, +4 → A	011(EE3) and TR = 01111(TR15)	L reg bytes 2, 3 to address scrambler; address scrambler + 4 to SAR.
L23 → S, +4 → R, A	011(EE3) and TR = 00110(TR6)	L reg bytes 2, 3 to address scrambler; address scrambler + 4 to SAR and R reg.
L2 → S	100(EE4)	L reg byte 2 to address scrambler; address scrambler to AOB(8-31).
L3 → S	102(EE5)	L reg byte 3 to address scrambler; address scrambler to AOB(8-31).
U → (E → 70) → W	110(EE6) and UL = 10(UL2) and UR = 10(UR2)	Mover U to EBCDIC to 7070 converter; EBCDIC to 7070 converter to mover W.
U → (70 → E) → W	110(EE6) and UL = 10(UL2) and UR = 10(UR2)	Mover U to 7070 to EBCDIC converter; 7070 to EBCDIC converter to mover W.

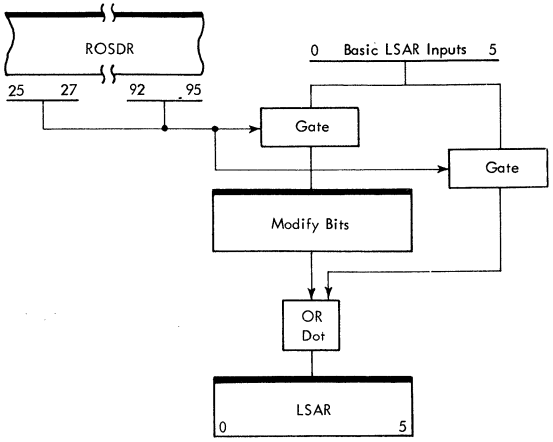
	84-89(SS)	Stat Setting and Miscellaneous Control
E(3) → EMSTAT	000001(SS1)	Set emulator stat = to bit 3 of emit field.
C*M → COP	000010(SS2)	M(23-31) to 7070 op code converter. Emit field to byte stats. AOB(30) to stat 3.
U=0F, ALPHA	110101(SS53)	If U = 0F, set stat 0 to 1. If U(2-3) = 1, set stat 4 to 1.

	92-93(WT) 10(WT2) and	Additional Local Storage Addressing
FP0 → LSA	WS = 000(WS0)	Set LSAR to 100000 to address word 0 of FP0.
FP0+1 → LSA	10(WT2) and WS = 001(WS1)	Set LSAR to 100001 to address word 1 of FP0.
FP2 → LSA	10(WT2) and WS = 010(WS2)	Set LSAR to 100010 to address word 0 of FP2.
FP2+1 → LSA	10(WT2) and WS = 011(WS3)	Set LSAR to 100011 to address word 1 of FP2.
FP4 → LSA	10(WT2) and WS = 100(WS4)	Set LSAR to 100100 to address word 0 of FP4.
FP4+1 → LSA	10(WT2) and WS = 101(WS5)	Set LSAR to 100101 to address word 1 of FP4.
GP6 → LSA	11(WT3) and WS = 110(WS6)	Set LSAR to 110110 to address GP6.
GP7 → LSA	11(WT3) and WS = 111(WS7)	Set LSAR to 110111 to address GP7.
GP8 → LSA	11(WT3) and WS = 000(WS0)	Set LSAR to 111000 to address GP8.
GP9 → LSA	11(WT3) and WS = 001(WS1)	Set LSAR to 111001 to address GP9.
GP10 → LSA	11(WT3) and WS = 010(WS2)	Set LSAR to 111010 to address GP10.
GP11 → LSA	11(WT3) and WS = 011(WS3)	Set LSAR to 111011 to address GP11.
GP12 → LSA	11(WT3) and WS = 100(WS4)	Set LSAR to 111100 to address GP12.
GP13 → LSA	11(WT3) and WS = 101(WS5)	Set LSAR to 111101 to address GP13.

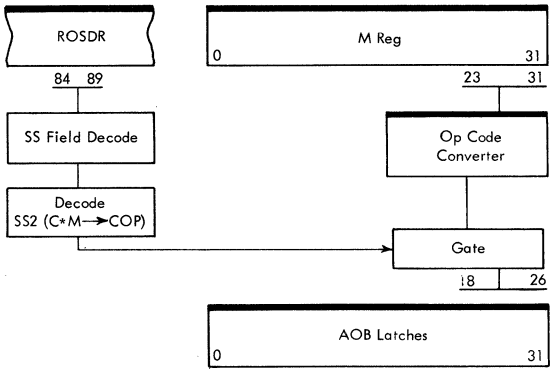
7070/7074 Op Code to Model 50 Address Conversion Table

High-Order Op Code Digit	Low-Order Op Code Digit 0	1	2	3	4	5	6	7	8	9
+0	003800	003840	003880	0038C0	003900	003940	003980	0039C0	003A00	003A40
-0	003820	003860	0038A0	0038E0	003920	003960	0039A0	0039E0	003A20	003A60
+1	003C00	003C40	003C80	003CC0	003D00	003D40	003D80	003DC0	003E00	003E40
-1	003C20	003C60	003CA0	003CE0	003D20	003D60	003DA0	003DE0	003E20	003E60
+2	003000	003040	003080	0030C0	003100	003140	003180	0031C0	003200	003240
-2	003020	003060	0030A0	0030E0	003120	003160	0031A0	0031E0	003220	003260
+3	003400	003440	003480	0034C0	003500	003540	003580	0035C0	003600	003640
-3	003420	003460	0034A0	0034E0	003520	003560	0035A0	0035E0	003620	003660
+4	002800	002840	002880	0028C0	002900	002940	002980	0029C0	002A00	002A40
-4	002820	002860	0028A0	0028E0	002920	002960	0029A0	0029E0	002A20	002A60
+5	002C00	002C40	002C80	002CC0	002D00	002D40	002D80	002DC0	002E00	002E40
-5	002C20	002C60	002CA0	002CE0	002D20	002D60	002DA0	002DE0	002E20	002E60
+6	002000	002040	002080	0020C0	002100	002140	002180	0021C0	002200	002240
-6	002020	002060	0020A0	0020E0	002120	002160	0021A0	0021E0	002220	002260
+7	002400	002440	002480	0024C0	002500	002540	002580	0025C0	002600	002640
-7	002420	002460	0024A0	0024E0	002520	002560	0025A0	0025E0	002620	002660
+8	001800	001840	001880	0018C0	001900	001940	001980	0019C0	001A00	001A40
-8	001820	001860	0018A0	0018E0	001920	001960	0019A0	0019E0	001A20	001A60
+9	001C00	001C40	001C80	001CC0	001D00	001D40	001D80	001DC0	001E00	001E40
-9	001C20	001C60	001CA0	001CE0	001D20	001D60	001DA0	001DE0	001E20	001E60

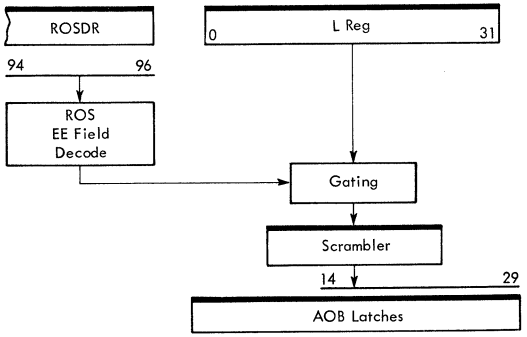
Modified LSAR Input Data Flow



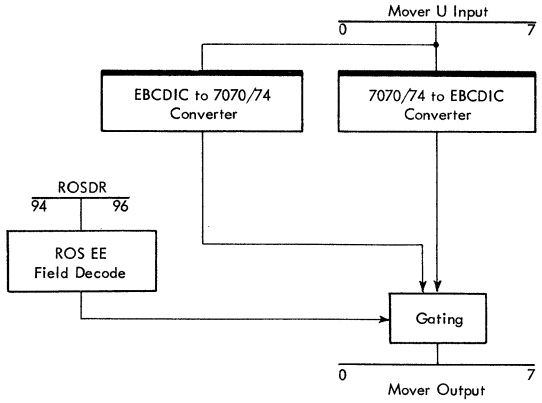
Operation Code Converter Data Flow



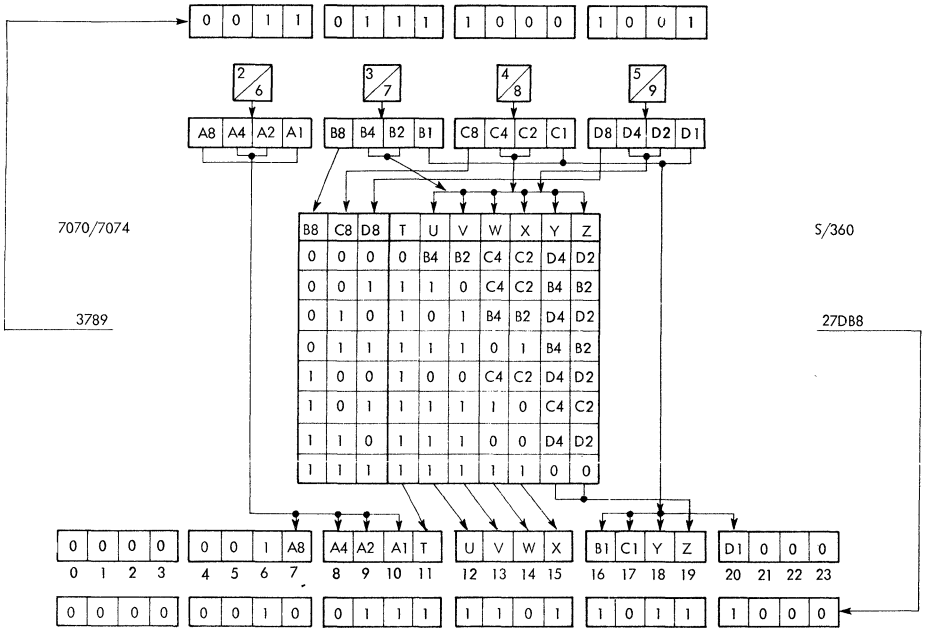
Address Scrambler Data Flow (ALD page XF2xx)



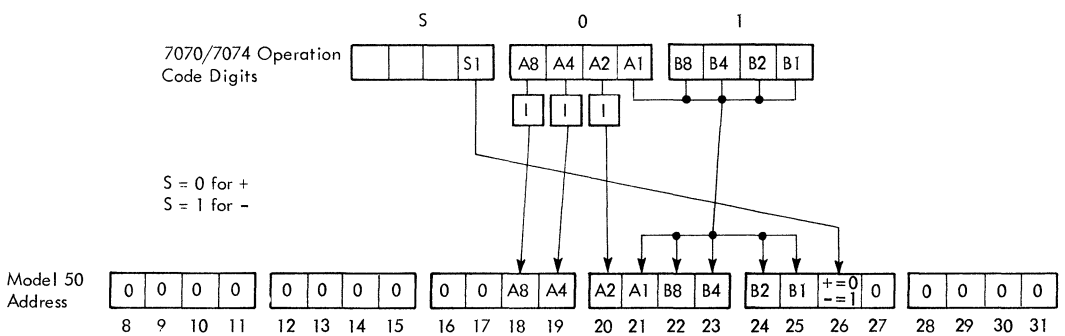
Converter Data Flow (ALD page XF4xx)



7070/7074 to System/360 Model 50 Address Conversion Example



7070/7074 Code to Model 50 Address Conversion



EBCDIC to 7070/7074 Code Conversion

High-Order Digit

Low-Order Digit	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	FF	FF	FF	FF	00*	20*	30*	00	FF	FF	FF	FF	60*	70*	80*	90*
1					11	21*	31*	41					61*	71*	81	91*
2					12	22	32	42					62*	72*	82*	92*
3					13	23	33	43					63*	73*	83*	93*
	(These Translate to FF)								(These Translate to FF)							
4					14	24	34	44					64*	74*	84*	94*
5					15	25	35	45					65*	75*	85*	95*
6					16	26	36	46					66*	76*	86*	96*
7					17	27	37	47					67*	77*	86*	97*
8					18	28	38	48					68*	78*	88*	98*
9					19	29	39	49					69*	79*	89*	99*
A					00	20	30	00*					60	70	80	90
B					15*	25*	35*	45*					65	75	85	95
C					16*	26*	36*	46*					66	76	86	96
D					17*	27*	37*	47*					67	77	87	97
E					18*	28*	38*	48*					68	78	78	98
F					19*	29*	39*	49*					69	79	89	99

* Valid 7074 characters on tape.

7070/7074 Emulator Code to EBCDIC Conversion

High-Order Digit

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	40*	40	50*	60*	70	70	C0*	D0*	E0*	F0*	F0	F0	F0	E0	E0	E0
1	41	41	51	61*	71	71	C1*	D1*	E1	F1*	F1	F1	F1	E1	E1	E1
2	40	40	50	60	70	70	C2*	D2*	E2*	F2*	F2	F2	F2	E2	E2	E2
3	41	41	51	61	71	71	C3*	D3*	E3*	F3*	F3	F3	F3	E3	E3	E3
4	4A	4A	5A	6A	7A	7A	C4*	D4*	E4*	F4*	F4	F4	F4	E4	E4	E4
5	4B	4B*	5B*	6B*	7B*	7B	C5*	D5*	E5*	F5*	F5	F5	F5	E5	E5	E5
6	4C	4C*	5C*	6C*	7C*	7C	C6*	D6*	E6*	F6*	F6	F6	F6	E6	E6	E6
7	4D	4D*	5D*	6D*	7D*	7D	C7*	D7*	E7*	F7*	F7	F7	F7	E7	E7	E7
8	4E	4E*	5E*	6E*	7E*	7E	C8*	D8*	E8*	F8*	F8	F8	F8	E8	E8	E8
9	4F	4F*	5F*	6F*	7F*	7F	C9*	D9*	E9*	F9*	F9	F9	F9	E9	E9	E9
A	4C	4C	5C	6C	7C	7C	CA	DA	EA	FA	FA	FA	FA	EA	EA	EA
B	4D	4D	5D	6D	7D	7D	CB	DB	EB	FB	FB	FB	FB	EB	EB	EB
C	4C	4C	5C	6C	7C	7C	CC	DC	EC	FC	FC	FC	FC	EC	EC	EC
D	4D	4D	5D	6D	7D	7D	CD	DD	ED	FD	FD	FD	FD	ED	ED	ED
E	4C	4C	5C	6C	7C	7C	CE	DE	EE	FE	FE	FE	FE	EE	EE	EE
F	4D	4D	5D	6D	7D	7D	CF	DF	EF	FF	FF	FF	FF	EF	EF	EF

NOTE:* Valid 7074 character.

Conditions and Cause of Error	DC Logout Lines				Pulsed Error Lines			LCS Caused Machine Check
	Key	Mark	Data	SAR	SAR	Data	SAP	
Store/Fetch/Test and Set								
Data Parity			X			X (1)		No
Key Parity (2)	X				X			Yes
Address Parity				X	X			Yes
Mark Bus Parity		X			X			Yes
Key Mismatch (3)							X	No (3)
Insert or Set Key								
Key Parity (4)	X					X		Yes
Address Parity				X	X			Yes
Mark Bus Parity		X			X			Yes

NOTE: Data Parity not possible on Insert/Set key.

(1) The data parity is ignored. An LCS data parity will be detected only when it is sent through the AOB, just as is main storage.
(2) In-key parity or Out-key parity if In key $\neq$ 0 (SPF check).
(3) SAP check occurs only if keys mismatch and CPU/Channel key is not zero. This will cause a program interrupt if masked on.
(4) In-key parity on Set Key or Out-key parity if Insert key (SPF check).

Notes

TEAR ALONG DOTTED LINE

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Circle one of the comments and explain in the space provided:

Suggested Addition (page ___) Suggested Deletion (page ___) Error (page ___)

Explanation:

Suggestions from IBM Employees giving specific solutions intended for award considerations should be submitted through the IBM Suggestion Plan.

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