File Number S360-01
Form A24-3373-2

IBM Systems Reference Library

IBM System/360 Model 30
Operating Guide

This reference publication describes operator procedures for the IBM 2030 Processing Unit and the IBM 1052 Printer Keyboard (attached to the IBM System/360 Model 30). For additional information for operation of the various input/output devices, refer to the publications listed in the IBM System/360 Bibliography, Form A22-6822.

Third Edition

This is a reprint of A24-3373-1 incorporating changes released in the following Technical Newsletter.

Form Number	Pages Affected	Date
N24-0390	20	December 28, 1966

Significant changes or additions to the specifications contained in this publication will be reported in subsequent revisions or Technical Newsletters

Copies of this and other IBM publications can be obtained through IBM Branch Offices.
This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. 171, P. O. Box 6, Endicott, New York 13760
Address comments regarding this publication to this address.

CONTENTS

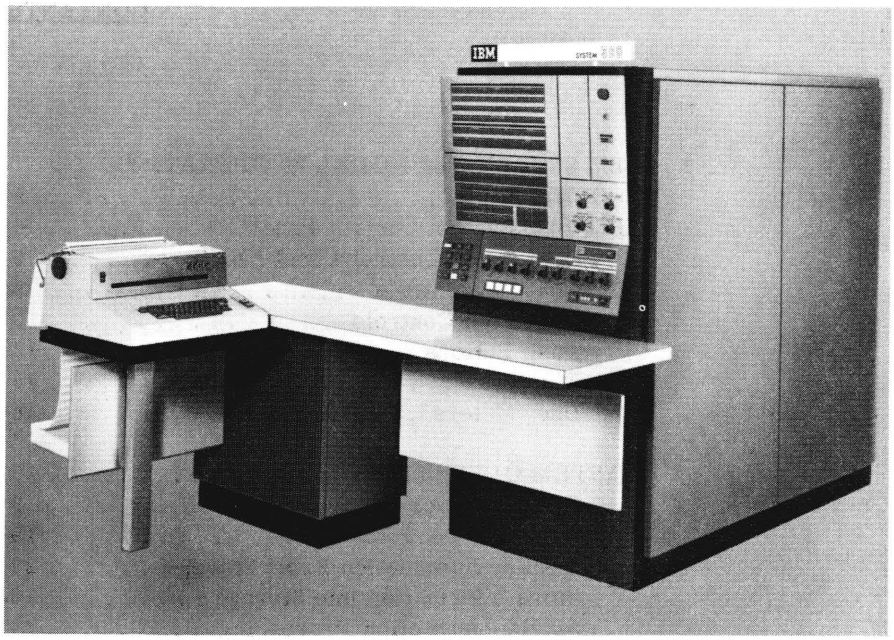


Figure 1. IBM System/360 Model 30 with IBM 1052 Printer Keyboard

The IBM System/360 Model 30 (Figure 1) is a solid-state, high-speed data processing system that is compatible with the other models of System/360 as described in IBM System/360, Principles of Operation, Form A22-6821.

The operator controls needed for normal program processing (turning power on and off and loading and starting a program) are contained on the 2030 system control panel (console). The IBM 1052 Printer-Keyboard can be added to the system so that communication between the operator and the system can be documented.

The IBM 2030 Central Processing Unit is provided with a number of indicators and manual controls that permit operation of the system in any of several modes, and observation of the results of any operation. These indicators and controls are assembled on a panel (Figure 2) that serves as both an operator's system control console and an IBM Customer Engineer's panel. The lower right-hand portion of the console is designated as the Operator's Control Panel (OCP). This section contains four push buttons, three 16-position rotary switches, and six indicators. Except for the nomenclature printed on the panel, the OCP is identical on all CPU's (Central Processing Units) in System/360. The OCP contains all controls and indicators necessary for normal problem-program processing.

OPERATOR'S CONTROL PANEL (OCP)

This section of the 2030 console (lower right corner) has the following controls and indicators:

Power-On Key

The power-on sequence for the CPU and all on-line I/O units starts when this key is pressed. A system reset function occurs. All data-flow registers (but not the general-purpose or floating-point registers) are reset, as are any priorities that happen to turn on. The CPU clock is reset to prevent access to storage so that information in storage is not disturbed. Hence, system power can be turned off and restored without destroying information in main storage.

The I/O units are sequenced ON one by one. If power cannot be brought up for a unit, further power-on sequencing is interrupted (console Power On light remains off) until corrective action is taken for that unit. All on-line I/O units are also reset. The power-on sequence bypasses off-line I/O devices. The time required for a power-on sequence depends on the number of on-line I/O units.

Note: The following procedure must be used when applying or removing electrical power to input/output devices:

1. Press the 2030 Stop key and wait for the Manual light to come on.
2. Set the Rate switch to the Single-Cycle position.
3. Press the 2030 Start key.
4. Turn power on or off on the I/O unit.
5. Set the Rate switch to the Process position.
6. Press the console Start key to resume operation.

This procedure ensures that the system is in a cycle in which read/write storage is not being accessed. Thus, any electrical surge on the channel that might have been caused by applying or removing power to the unit does not affect the contents of storage.

If power is removed from the last I/O unit (because maintenance is required) on a channel, the line terminators must be relocated in order to continue CPU operations. The last I/O unit on any channel must be on as long as the system is on.

Power-Off Key

This key removes power to the CPU and all on-line I/O units. The contents of main storage are not altered during the power-off operation, except that if a storage-read cycle has been taken (the Allow-Write indicator is on), a manual-write cycle is forced to ensure that the contents of the location just read are not lost.

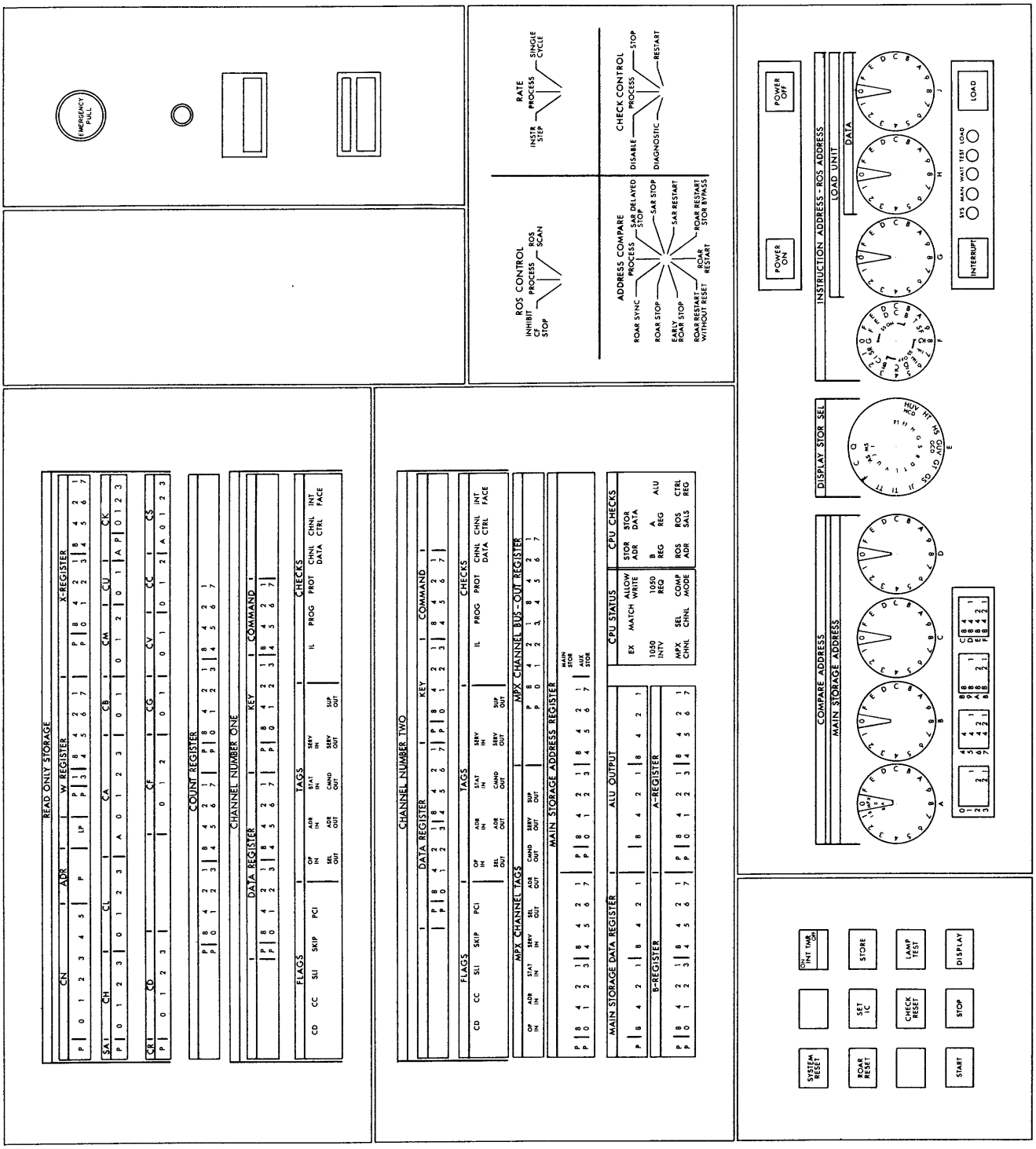


Figure 2. IBM 2030 System Control Panel (Console)

I/O interruption conditions are reset when the Power-Off Key is operated. Therefore, any pending I/O interruptions are lost during a power-off operation.

The Power-Off key takes precedence over the Power-On key.

The recommended power-off procedure is:

1. Press the console Stop key and wait for the Manual light to come on. (The Stop keys on the attached I/O units do not cause the system to enter the manual state.)

2. Press the Power-Off key.

Emergency Pull Switch

The Emergency Pull Switch removes all primary electrical power (including power to all on-line I/O units) with no regard to sequencing. The contents of storage may be altered if this switch is operated. As the name implies, the Emergency Pull Switch should be used only if necessary. This switch must be manually reset by the Customer Engineer.

The system is protected by thermal overload switches. If the temperature of the operating environment is too high, these switches drop system power. Contact the Customer Engineer whenever system power cannot be maintained.

System (SYS) Indicator

This indicator is normally on whenever either of the use meters is running. (See the Use Meters section.)

Manual (MAN) Indicator

This light indicates that the CPU clock is stopped and that no channel operation is in progress (as long as the System light is off). Several of the manual console controls are effective only when this lamp is on.

Wait Indicator

When this light is on, the CPU clock is running but no instruction processing occurs. If an interruption occurs, processing is initiated as required by the program.

Test Indicator

The Test light is on whenever the Address Compare, Check Control, ROS Control, or Rate switch is not set to Process (normal processing position).

Load Indicator

This indicator turns on when the Load key is pressed and released. It remains on until the load microprogram is successfully completed (the initial-load PSW is set into circuitry). See the Load Key section.

Load Key

This key is used to initialize the system. The following functions occur:

1. An automatic System Reset is performed.

2. The CPU clock is started.

3. The basic test microprogram is performed. This test is looped 128 times.

4. The clear UCW microprogram is run to reset all the flag bytes in the UCW area of auxiliary storage.

5. The load microprogram is begun. This routine analyzes switches G, H, and J to determine the address of the program-loading I/O device (load-unit address). When this routine is completed, the Initial Program Load (IPL) PSW has been successfully set up, and the Load light is turned off.

Note that the system mask is reset when the load key is pressed. The system mask in the IPL PSW is then effective as soon as the IPL PSW is set up.

Interrupt Key

When this key is pressed, the interruption code of the external old PSW is altered to indicate that an external interruption is pending. The system recognizes this interruption only if programmed to do so.

Switches F, G, H, and J

These rotary switches are normally used by the operator for the following operations:

1. Manual alteration of an instruction address or a ROS address (F, G, H, and J).

2. Manual entry of the load-unit address (G, H, and J).

3. Manual entry of a byte of information into main storage or into a data-flow register (H and J).

Note: The functions of these four switches are described in detail in other sections of this manual. Switch F is also used for 1400 compatibility operations (see IBM System/360 Model 1400 Compatibility Feature, Form A24-3255). Switches F and G have particular significance for 1620 compatibility operations (see IBM System/360 Model 30, 1620 Compatibility Feature, Form A24-3365).

CONSOLE CONTROLS

The manual controls on the 2030 console permit the operator to initiate system operation in any of several modes, and to perform display and store operations.

Note: Storage Protection is not effective during main-storage alteration or display operations initiated from the console. Care must be exercised to ensure that useful data is not unintentionally altered.

Data and Address Entry Switches

Eight rotary switches are provided for manually entering data or addresses into the system. Each of these sixteen-position switches provides one hexadecimal digit (four bits plus parity). Switches A, B, C, and D are used to enter an address for manual operations involving main or auxiliary storage, or to set up a compare address. These four switches are connected to the main-storage address register and to the compare (match) circuits. Switches F, G, H, and J are used to set up an instruction address, a ROS address, a load-unit address, or enter manual data into the system. These four switches are connected to the data-flow system through the A- and B-registers.

These switches are normally used as follows:

Switch	Function
A,B,C,D	A stop or restart address to be matched against the contents of the Main Storage Data Register (MSDR) or the ROS address register (WX).
A,B,C,D	A main-storage address for manual store or display operations.
F,G,H,J	An instruction-Start address or a ROS-Start address for a manual operation.
G,H,J	The load-unit address (I/O device and channel address from which the program is to be loaded).
H,J	A data byte to be loaded into main or auxiliary storage, or into a data-flow register.

The specific functions provided by these eight switches are detailed in various sections of this publication.

Switches F and G also have functions unique to the 1400 and 1620 compatibility features.

Display-Storage Selection Dial

This control can be used to display information from (or store into certain) system registers that do not have full-time indicators on the console. In addition, provision is made to display from or store into any main-storage or auxiliary-storage location. The dual-concentric rotary switch labeled E is used to access the registers and system control points shown on the dial (Figure 3).

Use of the Storage-Display Selector switch is described in the Display and Store Operations section.

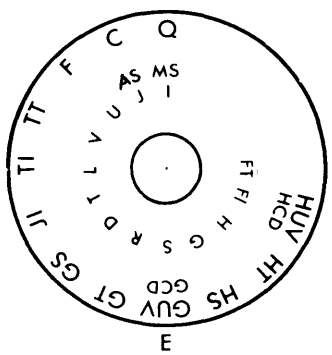


Figure 3. Display-Storage Selection Switch

OPERATION CONTROLS

Four rotary control switches are provided to allow any of several modes of system operation. Although these controls are normally used only by the IBM Customer Engineer, certain of their functions are useful to the programmer and operator. The Test light is on if these four switches are not all set to the Process position.

Rate Switch

The three modes of operation provided by this control are:

Instruction Step (INSN STEP) Position

When the Rate switch is in this position, one complete instruction (including all pending unmasked interruptions) is executed each time the Start key is pressed. After the instruction has been executed, the A- and B-registers contain the address of the next instruction. The stop that then occurs is identical to the stop that occurs when the Stop key is pressed.

If an input/output instruction is executed, the I/O instruction and all associated chaining is completed before the final stop occurs. If the start key is pressed again during the chaining operation, the next instruction is processed.

Process Position

This position of the Rate switch is used for normal program processing.

Single-Cycle Position

When the Rate switch is in this position, the system advances only one ROS cycle each time the Start key is pressed. Data overruns may occur if this mode is used for input/output operations.

Check Control Switch

The setting of this switch determines the system reaction when an error is detected in the CPU or I/O channels. Several courses of action are allowed as follows:

Diagnostic Position

In this mode, system control in case of an error is under control of a special microprogram.

Disable Position

When the system is operated in this mode, parity errors are logged (in associated check circuitry), but otherwise the failure is ignored. Note, however, that certain system errors cannot be ignored; that is, automatic correction of read-only storage addressing is not provided; and the wrong word will be accessed. Results obtained while processing a problem program in this mode may be wrong.

Process Position

This position of the Check Control switch is used for problem-program processing. When a parity check occurs, the malfunction trap microprogram is automatically initiated. This routine stores the contents of the machine check register and the program status word in fixed main-storage locations and originates a machine check interruption (refer to the IBM System/360 Principles of Operation, Form A22-6821).

Stop Position

Detection of a parity error in this mode causes an unconditional CPU clock stop, regardless of machine-check masks. I/O data overruns may occur if the system is operated in this mode.

Restart Position

When an error occurs in this mode, the resultant system response is dependent upon the setting of the Address Compare switch as follows:

1. With the Address Compare switch set to SAR Restart, a System Reset is initiated, the basic micro-diagnostic and clear-UCW routines are executed, the instruction counter is set to the address specified by switches F, G, H, and J, and an instruction cycle is started.

2. With the Address Compare switch set to ROAR Restart or ROAR Restart Storage Bypass position, the circuitry registers (not general-purpose, floating-point, or UCWs) are reset, the ROS address register is set as specified by switches F, G, H, and J, and the resulting microprogram is initiated (with or without affecting main storage, depending on the setting of the Address Compare switch).

3. With the Address Compare switch set to ROAR Restart Without Reset, operation is identical to that of ROAR Restart except that no reset is initiated.

4. With the Address Compare switch set to any other position, the address specified by switches F, G, H, and J is placed in the instruction counter and an I-cycle is started.

Address Compare Switch

This switch determines whether the CPU match circuit is connected to the Read-Only Storage Address Register (ROAR) or to the Main-Storage Address Register (SAR), and the system's reaction when an address match occurs. When the switch is in any position that contains the term ROAR, the read-only storage address register is compared to switches A, B, C, and D; other positions apply to the main-storage address register. The switch positions and the associated system responses are as follows:

Process Position

This position is used for normal problem-program processing.

ROAR SYNC Position

This position provides a sync pulse (for Field Engineering purposes) when the address specified by switches A, B, C, and D matches the contents of the read-only storage address register (WX register).

ROAR Stop Position

With this setting, system operation proceeds until the contents of the ROAR match the address specified by switches A, B, C, and D. When this match occurs, the CPU clock is turned off (at the end of the ROS cycle in progress) and the system stops.

Early ROAR Stop Position

With this setting, processing proceeds until the contents of the ROAR match the address specified by switches A, B, C, and D. When the match occurs, the CPU clock is turned off (at the end of the current ROS cycle) and the system stops. The ROAR indicators display the address of the ROS word just prior to the ROS word-address set in switches A, B, C, and D. The ROS word displayed, however, is the one at the address specified in switches A, B, C, and D.

ROAR Restart
ROAR Restart Without Reset, and
ROAR Restart Storage Bypass Positions

These three settings are similar in that the occurrence of a match between a ROAR address and switches A, B, C, and D causes the ROAR to be reset to the value specified by switches F, G, H, and J. In no case are the general-purpose or floating-point registers, or the UCW flag bytes reset.

For ROAR Restart, CPU registers are reset before the ROAR is reset.

For ROAR Restart Storage Bypass, the function is identical except that main storage is not permitted to operate; hence, normal problem-program processing cannot be done in this mode.

In the ROAR Restart without Reset position, the function is the same as with ROAR Restart except that no reset is performed.

SAR Restart Position

When a match occurs in this mode, a fixed address is forced into the ROAR. The basic micro-diagnostic and clear-UCW routines are performed, the address specified by switches F, G, H, and J is loaded into the instruction counter, and an instruction cycle is started.

SAR Stop Position

When a match between the SAR and switches A, B, C, and D occurs in this mode, the CPU clock is stopped at the end of the write cycle in which the match occurs.

SAR Delayed Stop Position

In this mode, a match between the SAR and switches A, B, C, and D causes the CPU clock to stop at the

conclusion of execution of the instruction in which a match occurs. All pending interruptions are taken before the clock stops.

ROS Control Switch

This switch is primarily for Field Engineering use.

ROS Scan Position

This mode is used when certain diagnostic tests (scan ROS or read/write storage) are run.

Inhibit CF Stop Position

In this mode, processing occurs in the normal fashion except that microprogram stops (determined by the CF field) are ignored.

Process Position

This position is used for normal program processing.

PUSH BUTTONS

Several push button switches are provided to allow the operator to perform manual operations or to initiate system functions. The title given to each button describes the resulting function when the switch is operated.

Power-On Key,
Power-Off Key, and
Emergency Pull Switch

These controls are discussed in the Operator's Control Panel section.

System Reset Key

Pressing this key resets the CPU clock, all registers (except the general-purpose and floating-point registers in local storage), the controls in the CPU, and all I/O units (including all sense and status for the I/O units). In addition, when the Start key is pressed after operation of the System Reset key, the Basic Test and UCW Reset microprograms are initiated. (The Basic Test routine is looped 128 times, so disregard the various error indicators during this time.) See the ROAR Reset Key section.

Also, when the System Reset key is operated, the current system mask is reset. However, upon restart, the same current system mask controls the system if that mask in local storage has not been altered before restart (see Current Program Status Word Selection section).

ROAR Reset Key

This key is used to manually alter the ROAR address (WX registers) from the contents of switches F, G, H, and J. The ROAR Reset key is active only when the CPU clock is stopped; its function is initiated when the Start key is pressed.

If the ROAR Reset key is pressed after a System Reset function but before the Start Key is pressed, the Basic Test and Clear UCW microprograms are not initiated, that is, the UCW flag bytes in the MPX storages are not reset to zeros.

Start Key

If the Start key is pressed after a normal stop (for example, after the Stop key is pressed), instruction processing continues as if no stop had occurred. Machine status is unaffected.

If the Start key is pressed after a Start Reset function, the Basic Test routine is performed, and the Clear UCW routine resets all UCW flag bytes to zeros. If the Start key is operated again, the PSW located at address 0000 is loaded into circuitry, and processing starts. (See Start Reset Key and ROAR Reset Key sections.)

Set IC Key

This key is used to manually alter the Instruction Counter (IC) address from the contents of switches F, G, H, and J, and is active only when the CPU clock is stopped (Manual light is on). When the Set IC key is pressed, the altered instruction address is displayed in the B- and A-registers, and the system stops. Any outstanding channel share cycles are completed before this microprogram stop occurs. Processing begins at the new instruction address when the Start key is pressed.

If the Set IC key is pressed after a System Reset function, the instruction counter is set to the address entered from switches F, G, H, and J.

Check Reset Key

This key resets all machine-check logic circuits. The Check Reset key may be used at any time (CPU clock running or stopped).

Stop Key

When this key is pressed, the system enters the stopped state when:

1. The instruction being processed has been completed,
2. All pending interruptions have been serviced, and
3. Any I/O operation in progress has been finished.

If data or command chaining is involved, it is completed before the CPU clock is stopped. The System light stays on as long as any I/O unit (except the 1050) is engaged in an I/O operation; that is until device-end is accepted for the last command in a chain for that I/O device).

Note that the machine environment is not destroyed and the program that was in progress can be restarted (by operation of the Start key). The address of the next instruction is displayed in the B- and A-registers.

When the system is in the stopped state, the multiplexor channel is allowed to accept share-request traps (microprogram branches), and the selector channel is allowed to accept data cycles. This provision permits input-terminal and multi-system operations even though the 2030 program in progress has been manually interrupted.

Even though these operations are in progress, data can be stored or displayed. At the instant a cycle is being used for a channel operation, the manual store and display circuits are inactive. However, if the Store or Display key is held operated, the data is stored or displayed. If the store key is operated only during a channel-operation cycle, the data to be manually stored is not stored. It is advisable, therefore, to display any location (in which data is manually stored) so that storing can be verified.

Interval Timer Switch (INT TMR)

When the Interval Timer feature is installed and this switch is on, the interval timer is allowed to generate program interruptions. If the switch is off, the interval timer is ignored and the main-storage timer locations are not changed.

Store Key

This key causes the hexadecimal byte specified by switches H and J to be entered into the area selected by the Display Storage Selection dial (switch E).

If a register is selected by switch E, the data byte is entered into that register and displayed in both the B- and A-registers. Information cannot be stored in all the registers selectable by switch E. See the Store and Display Section.

When main storage (MS) or auxiliary storage (AS) is selected by switch E, switches A, B, C, and D specify the address into which the data byte is stored. The data byte (from switches H and J) is displayed in both the B- and A-registers.

The CPU clock must be stopped for the store operation. If main or auxiliary storage is being accessed, the Allow Write light must be off.

Lamp Test Key

Pressing this key causes all indicator lights on the 2030 console to turn on. This test does not affect system operation and can be performed during program execution if desired. (The console lamps will be slightly dimmer than during normal operation.)

Display Key

The function of this key is similar to that of the Store key, except that the accessed location is not altered. The Display key is provided so that registers that do not have their own console indicators can be displayed.

Main-storage (MS) and auxiliary-storage (AS) locations are displayed by setting switch E to the storage area desired, and switches A, B, C, and D to the address of the location to be displayed. The Main Storage Data Register (MSDR) is used to display the contents of the accessed storage location. If the original value in the MSDR will be needed when the program is restarted, record this value so the MSDR can be restored after the display operation. If the ROS control, Rate, Address Compare, and Check Control switches are all set to Process, and the system is allowed to come to a normal stop (Stop key was pressed and the manual light is on), the contents of the MSDR need not be restored before the Start key is pressed to resume program operation.

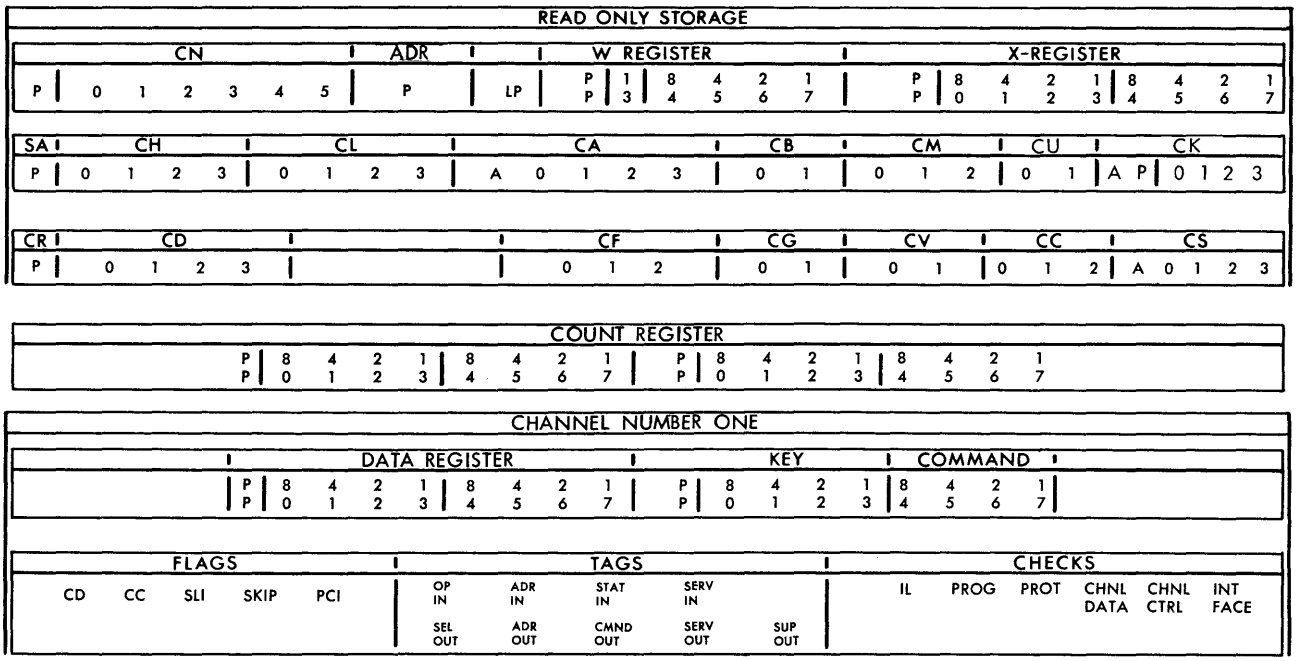


Figure 4. Console Display Indicators (Part 1 of 2)

A register selected by switch E is displayed in the A-register. When either the I- or J register (see Figure 8) is selected, both the I- and J-registers are displayed in the Main Storage Address Register (MSAR). This is also true for the U- and V-registers (see Figure 8). (The selected register is also displayed in the A-register.)

The CPU clock must be stopped and the Allow Write indicator must be off for any display operations involving storage, or for displays of the IJ or UV registers. Note, however, that the contents of the I-, J-, U-, or V-registers can be displayed in the A-register if the Allow Write indicator is on.

DISPLAYS

Several indicators are provided to display control information, data bytes, and system status. Each indicator shows the binary condition of a latch or signal line. When a latch is set, or a signal is on, its associated lamp is lighted. In cases where the position of a bit in a field is important, the numerals 0, 1, 2, 3, etc, are lighted; but where bits are grouped to form a numeric digit, the binary bit values are lighted (8,4,2,1). The P lamps associated with many of the console displays represent the parity bit for the information.

In addition to the control information provided by the read-only storage display, the 2030 console displays the contents of certain data registers, the read/write storage address register, a number of CPU status conditions, the multiplexor channel tags, and several check conditions. Although only some of the registers are displayed, provision is made to display the contents of all CPU registers as described in the Display, and Store section of this publication.

CPU Status Indicators

The CPU status indicators (Figure 4, Part 2 of 2) signal the actual operating status of the CPU at any time. These indicators and their corresponding meanings are:

EX. This lamp turns on at the end of each instruction execution (that is, whenever the micro-instruction branch-on-interrupt occurs). In the micro-instruction word immediately following the interrupt word, the EX latch is reset. Note that if the system is programmed to stop at the end of instruction execution (for example, if the stop button has been pressed), the EX lamp remains on. It turns off when the CPU clock is restarted.

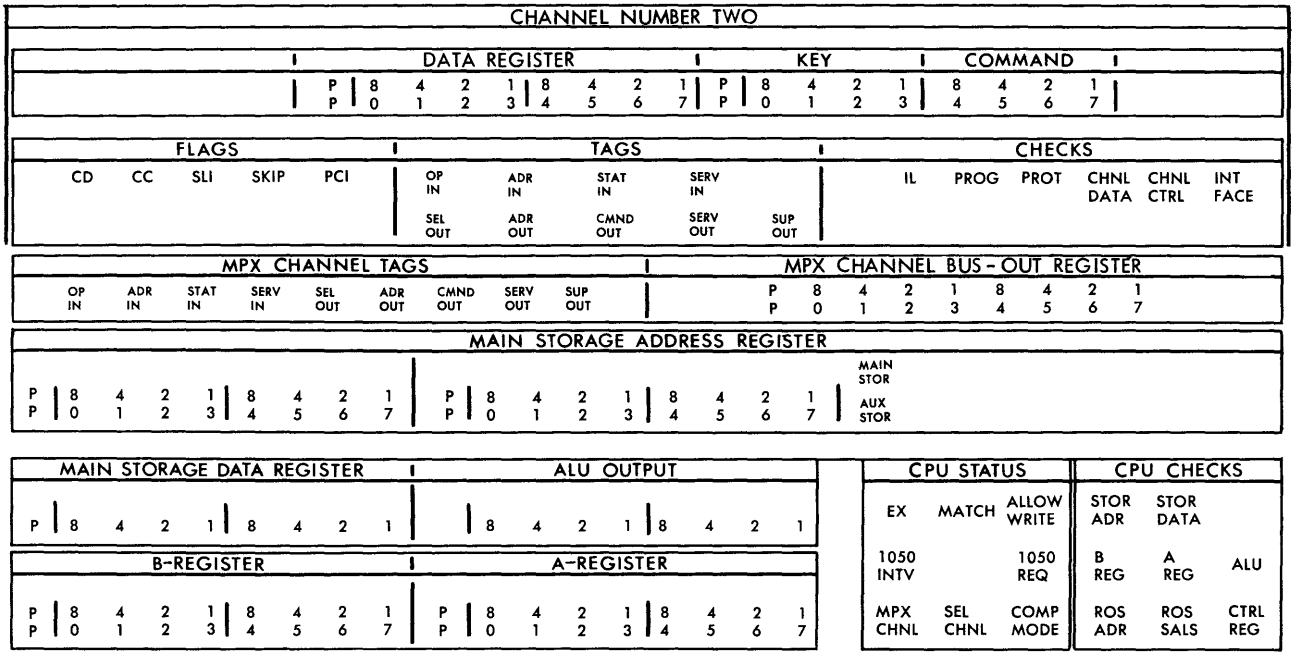


Figure 4. Console Display Indicators (Part 2 of 2)

Match. Some modes of operation require the use of an exclusive OR match circuit. The match indicator turns on whenever the compare address in switches A, B, C, and D matches the contents of either the Main Storage Address Register (MSAR) or the Read-Only Storage Address Register (ROAR). The position of the address-compare switch determines which of these registers is monitored, as well as the system response to a match.

Allow Write. Whenever the allow-write indicator is on, main or auxiliary storage has completed a read operation, but not the corresponding write operation. When this indicator is on, manual display and store operations of main or auxiliary storage are not possible.

1050 INTV. This indicator is turned on when an addressed IBM 1050 system device requires manual intervention (out of cards, out of forms, etc). The light is turned on only if the device was in run mode at the time the intervention became necessary. The 1050 INTV light is turned off when the unit has been made ready and when that unit is re-addressed, or by the 2030 System Reset or Load keys.

1050 REQ. This light turns on whenever the operator presses the request key on the 1052. It is reset when attention status is recognized by the attachment and accepted into the unit status register.

MPX CHNL. Whenever a multiplexor channel share request is recognized by the CPU, this light turns on. This light turns off at the completion of the share cycle.

SEL CHNL. This lamp is lighted whenever either selector channel is using the read-only storage (such as for a selector-channel chaining operation).

COMP MODE. Whenever the system is operating in compatibility mode, this light is on. This lamp is turned on at the same time as the W3 lamp (the W-register read-only-storage display bit-3 position position--see Part 1 of Figure 4).

CPU Check Indicators

In the central processing unit are several check circuits. Whenever a check is detected, a check latch is set. and a bit is turned on in the machine-check (MC) register, as follows:

MC Register Position	Indication
0	A-REG
1	B-REG
2	STOR ADR
3	CTRL REG
4	ROS SALS (Read-Only Storage Sense Amplifier Latches)
5	ROS ADR
6	STOR DATA
7	ALU

Except for the ALU check, the turning on of any of these lights is an indication of detected bad parity in the associated register. In the ALU, a duplicate check is made because the ALU does not use the parity bit (input is complemented and the operation is performed in both uncomplemented and complemented form, and the answers are compared). When the CPU stops during normal program processing with any one or more of these indicators on, call the Customer Engineer.

Registers

The following registers have full-time indicators on the 2030 console (left center and upper left portions of the console, Figure 3).

The ALU Output is not a register but is listed here because of its relationship with the actual registers.

B- and A-Register Displays

These indicators provide full-time display of the contents of the B- and A-registers.

During manual operations, the display from the A-register depends on the settings of console switches (see the Display Key section).

When the system is in the Wait state (instruction processing stopped and the program is waiting for an interruption) or when in the process-stop condition (such as when the Stop key is pressed), the instruction counter (IC) is displayed in the B-register (I-register contents) and the A-register (J-register contents).

Main-Storage Data Register (MSDR) Display

For CPU or multiplexor-channel operations, these indicators display information being transferred to or from either main or auxiliary storage. The MSDR indicators, therefore, provide full-time display of the contents of the R-register.

For manual operations, the MSDR indicators display the data byte being stored, displayed, etc., depending upon the setting of 2030 console switches.

ALU Output Display

These indicators provide full-time display of the output of the arithmetic-logic unit (ALU).

MAIN STOR Indicator

When on, this light (located to the right of the MSAR lamps) indicates that a main-storage address is being displayed by the MSAR lights.

AUX STOR Indicator

When on, this light (located to the right of the MSAR lamps) indicates that an auxiliary-storage address is being displayed by the MSAR lights.

Main Storage Address Register (MSAR) Display

When the MAIN STOR indicator is on during normal processing operations these lights display the address of the main-storage location being accessed.

During manual operations, the information displayed in the MSAR lights may apply to any of several internal system registers, depending upon the setting of the Display Storage Selection dial (switch E) and/or rotary switches A, B, C, and D.

When the AUX STOR indicator is on, the high-order hexadecimal digit (four high-order bits) of the MSAR specify which part of auxiliary storage is addressed (that is, local storage or one of the MPX storages).

Note that when the system is in Wait state or in the process-stop condition, the address of the next instruction to be executed (instruction counter--IC) is displayed in the B- and A-registers. The operation code is not displayed.

Multiplexor-Channel Displays

MPX Channel Bus-Out Register

These lights indicate the byte of information being sent from the main-storage data register (MSDR) to the multiplexor channel.

MPX Channel Tags

These lights provide display of the current status of various multiplexor-channel I/O interface control lines.

OP IN. The operational in (OP IN) lamp indicates that an I/O unit is selected and is in communication with the channel.

ADR IN The address in (ADR IN) light indicates that the address of the currently selected I/O unit is on bus-in. (Bus-in is the data and control transmission network for information transfer from a control unit to the CPU.)

STAT IN. The status in (STAT IN) light indicates that the selected I/O unit has placed status information on bus-in.

SERV IN. The Service in (SERV IN) light indicates that the selected I/O unit is ready to send or receive data.

SEL OUT. The select out (SEL OUT) light indicates that the various I/O units attached to the multiplexor channel are being polled to determine whether any device requests service.

ADR OUT. The address out (ADR OUT) light indicates that address information is on bus-out. (Bus-out is the data and control information network from the CPU to the control unit.)

CMND OUT. The command out (CMND OUT) light indicates that the information on bus-out is a command.

SERV OUT. The service out (SERV OUT) light indicates that the CPU has accepted the information on bus-in or has provided data on bus-out.

SUPP OUT. The suppress out (SUPP OUT) light indicates that status and data transfers are suppressed, that command-control chaining is in progress, or that a malfunction (selective) reset is being effected with regard to the selected I/O unit.

Selector-Channel Displays

Several indicators are provided for each selector channel. The Channel Number One lights refer to selector-channel one; the Channel Number Two lights refer to selector-channel two.

The Count Register (located above the Channel Number One lights) is used to observe the current byte count for selector-channel one (switch E set to GUV-GCD) or selector-channel two (switch E set to HUV-HCD).

Data Register

Whenever a main-storage share cycle is initiated by a channel, these lights provide full-time display of information being transferred.

Key

These lights provide full-time display of the main-storage (CAW) protection key for all commands associated with the Start I/O instruction.

Command

The four low-order bits of the CCW operation code are displayed by these lights.

Flags

This group of five indicators displays the manner in which a channel command should be executed, as follows:

CD. This light indicates chaining of data addresses.

CC. This light indicates command chaining.

SLI. This light (suppress-length indication) indicates that the program will not be notified in the event of a wrong-length record.

SKIP. This light specifies suppression of information-transfer to storage during a read, read backward, or sense operation.

PCI. This light (program-control interruption) indicates that the channel will generate an interruption condition when the CCW takes control of the channel.

Selector-Channel Tags

The nine tag indicators for each selector channel perform the same functions as the corresponding indicators for the multiplexor channel (see MPX Channel Tags section).

Selector-Channel Checks

Each selector channel has a number of check circuits that continually monitor channel operation. When a malfunction is detected, the appropriate check light is turned on. These checks are:

IL. If the SLI flag is not on, this light (incorrect length condition) is turned on when the number of bytes in the assigned storage area is not equal to the number of bytes requested or offered by the I/O unit.

PROG. This light (program check) indicates that the channel has detected a programming error.

PROT. This light (protection check) indicates that the channel attempted to violate a portion of main storage that is protected for the current operation.

CHNL Data. . This light (channel data check) indicates that the channel has detected a parity error in the information transferred to or from main storage during an I/O operation.

CHNL CTRL. This light (channel control check) indicates that a machine malfunction affecting channel controls has occurred.

INT Face. The interface control check is caused by sequencing problems on the I/O interface.

Read-Only Storage Displays

In general, these indicators are for Customer Engineering use. Therefore, only a short description of each ROS field is presented here.

CA, CB, CC, CF, CG, CV. These fields control operation of the ALU.

CD. This field selects one of the several system registers to receive the output of the ALU. A given register can be used as both the source and destination during a single ROS cycle.

CK. This field provides a source of data and control bits (that is, generates constants).

CM, CU. These two fields control storage operation. They determine which storage area (main or auxiliary) is to participate in a particular read or write operation.

CN, CH, CL. These fields control the address of the next ROS word.

LP. This light indicates that the air pressure in the read-only storage unit is low, or that the temperature of main storage is below the optimum operating range.

W- and X-Register. These indicators display the address of the ROS word just read.

CS. This field supplies status indications to various machine control points.

USE METERS

The 2030 console has two direct-reading meters that measure operating time: a customer's meter and a Customer Engineer's meter. The position of a key switch determines whether the customer's meter or the CE meter is operating. The Customer Engineer holds the key for this switch; and whenever he is performing either scheduled or unscheduled maintenance in the CPU, he will set the switch to cause the CE meter to operate. One of these meters (determined by key-switch setting) operates whenever the CPU clock is running and either:

1. The CPU is not in the wait state or,

2. There is an interruption pending, or

3. A manual store or display operation is in progress. The System indicator is on when either meter is running. It indicates that some productive activity is in progress. The System light stays on as long as any I/O unit (except the 1050) is engaged in an I/O operation (that is until device-end occurs for the last command in a chain for that I/O device). This can occur after the Stop key is pressed.

   The use meter (customer or CE) operates for a minimum of 400 milliseconds each time it is started.

SYSTEM POWER-ON AND POWER-OFF

Power to all system units is brought up during a system power-on sequence. If power cannot be successfully brought up on an I/O unit that is on-line to the CPU, the system power-on sequence cannot be completed. See the Operator's Control Panel section.

PROGRAM LOAD ROUTINE

Prepare the I/O unit from which the program is to be loaded as follows. (Refer to the appropriate Systems Reference Library publication for information concerning the particular I/O unit involved.)

Card I/O Unit Preparation

When the program to be loaded is contained in punched cards, a card reader must be initialized. The following steps generally apply to all card readers:

- Run the cards out of the read feed by performing a nonprocess runout as described for the particular card reader.
- Place the program-load deck in the read-feed hopper.
- Press the reader start key.

The card reader is now ready to read the program deck.

Disk I/O Unit Preparation

When the program is to be loaded from a magnetic disk unit:

- Turn the disk-drive meter switch on. This allows the device to be used for input/output.
- Place the disk pack containing the desired program on the disk drive and operate the disk-drive start key.

The disk storage unit is ready when its ready light is on.

Tape I/O Unit Preparation

When a magnetic tape unit is being used to load the problem program:

- Open the tape unit door for access to the tape reels and read/write assembly.
- Place the tape reel containing the program on the left reel hub and lock it in place.
- Thread the tape along the tape path and onto the take-up reel.
- Wind the tape until the load-point marker is well past the read/write head.
- Close the access door.
- Press the load-rewind key.

The tape unit is now ready to be used as input when called on by the program-load routine.

Console Operation (Program Loading)

With the system power on and the appropriate I/O load unit set up:

1. Set the address of the I/O load unit that contains the program to be loaded in rotary switches G, H, and J (see Figure 2, OCP section). The channel address is set in switch G; the unit address in switches H and J.
2. Make sure that the ROS Control, Rate, Address Compare, and Check Control switches are all in the PROCESS position (see Figure 2, right center section). The Test light on the OCP portion (see Figure 2) of the 2030 console is off only when all four of these switches are in the PROCESS position.
3. Press the Load key on the OCP portion of the 2030 console. The Load light (see Figure 2, OCP section) turns on when the Load key is pressed, and it turns off after the load routine has been completed (when the loading of the new PSW has been completed).

A system reset is initiated when the Load key is pressed. The Basic Test microprogram is looped 128 times. A microprogram (ROS) then automatically resets the UCW's in the multiplexor storages. It may or may not be necessary to clear the contents of core storage into which the new program is loaded; this is dependent upon the program.

After the program has been loaded, processing will proceed immediately unless the program loaded is written in such a manner as to prevent this. Therefore, system operating procedures and the program determine what subsequent action is to be taken. If the system is programmed to go to the wait state after the program has been loaded, operating procedures may indicate that the following action is to be initiated:

1. Press the Stop key to enter stopped state (Manual light on). Wait for the system light to turn off.
2. Load an instruction address from rotary switches F, G, H, and J into IC (Instruction Counter) by using the set-IC key (see IC in the Push buttons section of this publication).
3. Press the start key to start processing at the instruction address loaded.

DISPLAY INFORMATION FROM STORAGE

The contents of any byte of storage can be displayed when the CPU clock is stopped (the Manual light on the OCP is on) and the Allow-Write indicator (in CPU status section of 2030 console--Part 2 of Figure 3) is off. The Allow-Write indicator, when on, indicates that a read-from-storage operation has been completed but that the associated write cycle has not been performed.

Procedure

The contents of any storage position can be displayed when the following procedure is used (assume that the test light is out and normal program processing is in progress):

1. Press the stop key (lower left portion of 2030 console--Figure 2). The system stops after the current instruction is processed, and all pending interrupts have been serviced.
2. After the system stops, the allow-write indicator is off and the manual light is on.
3. Set the rotary display-storage-select switch (switch E) to the MS or AS position (depending upon whether Main Storage or Auxiliary Storage is to be used in this operation). (See lower portion of Figure 2.)
4. Place the address of the desired byte in rotary switches A,B,C, and D (Figure 2).

Note: If a byte of auxiliary storage is to be displayed, set rotary switch A to LS (for Local Storage) or to the desired MPX (multiplexor) storage position. If auxiliary is used, the address of the desired byte is then set in switches C and D.

5. Press the display key (lower left section of Figure 2).
6. Make sure that the appropriate indicator, MAIN STOR (main storage) or AUX STOR (auxiliary storage), is on. These indicators are just to the right of the main-storage address register display (see Part 2 of Figure 3).
7. The address of the accessed location is then displayed in the main-storage address register (Part 2 of Figure 3). Make sure this is the address desired. (You may inadvertently have set up rotary switches A, B, C, and D incorrectly.)
8. The data stored in the addressed location is displayed in the main-storage data register indicators on the 2030 console.
9. When the system and wait lights are on and the stop key does not allow a display of storage, the operator should set the rate switch to SINGLE-CYCLE to turn off the system light and turn on the manual light.
10. Only when all the preceding nine items fail, should system reset be performed.

STORE INFORMATION INTO STORAGE

Store operations are similar to display operations. That is, the contents of any position of storage can be altered if the allow-write indicator is off and the manual light is on (CPU clock stopped). If the allow-write indicator is on or the manual light is off, the store key (on OCP section of 2030 console, see Figure 2) is interlocked so that the contents of storage cannot be altered.

Procedure

To store a byte into storage:

1. When the system stops (stop key has been pressed), the allow-write indicator is off and the manual light is on.

2. Select the area of storage (to be altered) with the rotary display-storage-selection switch (switch E). Use the MS position for storing into Main Storage and the AS position for storing into Auxiliary Storage (see lower section of Figure 2).

3. Set the address of the selected byte of storage into rotary switches A, B, C, and D.

Note: If you are going to store a byte into auxiliary storage, set rotary switch A to LS (for Local Storage) or to the desired MPX (multiplexor storage) position. Then set switches C and D to the address to be used in auxiliary storage.

4. Set the byte of information to be stored in rotary switches H and J (hexadecimal representation of byte).

5. Press the store key (see Figure 2, lower left portion).

6. The data byte to be stored is displayed in the main storage data register indicators on the 2030 console. The address at which the displayed byte is stored is displayed in the main-storage address register indicators (see Part 2 of Figure 3). Check these indicators to make sure the correct data is entered onto the desired location.

Addressing Bytes of Auxiliary Storage

In most instances, you will have no need to store or display in auxiliary storage. The following descriptions, however, are provided here for reference. The other areas of auxiliary storage are not applicable to operator use, or not used, or used only in special situations (such as for compatibility modes). Follow the appropriate procedure as described in the Display Information from Storage and Store Information in Storage sections. Use this section to determine the address of a particular location in auxiliary storage.

1. Set rotary switch A to the desired area of auxiliary storage (Figure 5):

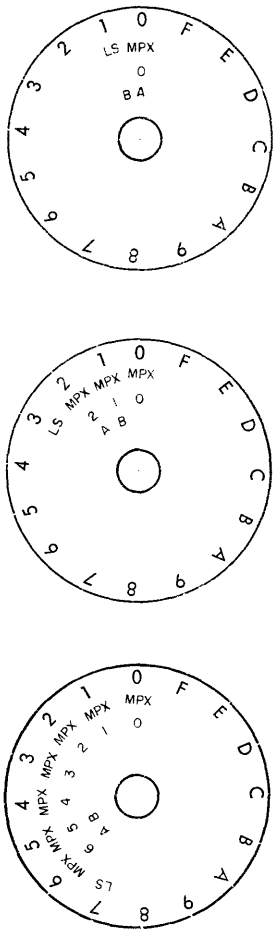


Figure 5. Rotary Switch A

Switch A Setting	Auxiliary Storage Accessed
MPX 0	Multiplexor Channel Unit Control Words 0 through 31
MPX 1	Multiplexor Channel Unit Control Words 32 through 63
MPX 2	Multiplexor Channel Unit Control Words 64 through 95
MPX 3	Multiplexor Channel Unit Control Words 96 through 127
MPX 4	Multiplexor Channel Unit Control Words 128 through 159
MPX 5	Multiplexor Channel Unit Control Words 160 through 191
MPX 6	Multiplexor Channel Unit Control Words 192 through 223
LS	Local Storage

Note: The MPX 0 setting is on all 2030 consoles. The MPX 1 and MPX 2 settings are on all 2030's that have 16K or more main-storage addresses. MPX 3, MPX 4, MPX 5, and MPX 6 settings are on 2030's (with 32K or more main-storage addresses) that have the 224 subchannel special feature.

2. Set rotary switch B to 0.

3. Set the desired byte address in rotary switches C and D as described in the following sections.

General-Purpose Register Selection

General-purpose registers 0 through 15 are selected by setting switch C to the corresponding hexadecimal equivalent (0 for register 0, F for register 15).

The desired byte in the selected general register is specified by switch D (bytes 0 through 3 by switch positions 0 through 3).

Floating-Point Register (Special Feature) Selection

Floating-point registers 0, 2, 4, and 6 are selected by setting switch C to 0, 2, 4, or 6, respectively.

The desired byte in the selected floating-point register is specified by switch D as follows:

Switch D Setting	Selected Byte
8	0
9	1
A	2
B	3
C	4
D	5
E	6
F	7

In all floating-point formats, the sign is contained in the high-order bit (bit 0) of byte 0 and the characteristic is contained in bit positions 1 through 7 of byte 0.

In short floating-point formats, the fraction is contained in bytes 1, 2, and 3. In long floating-point formats, the fraction is contained by bytes 1,2,3,4,5, 6, and 7.

CPU-Registers Stored in Local Storage

During multiplexor-channel operations CPU registers are temporarily stored in local storage. To display or store in this area:

1. Set switch C to 5.

2. Set switch D to the desired register storage as follows:

Switch D Setting	Stored Register Selected (General Function)	
8	I	(Instruction Address)
9	J	
A	G	(Instruction Operation Code)
B	U	(Data Address)
C	V	
D	L	(Instruction Length)
E	D	(General-Purpose Data Register)
F	S	(CPU Status)

Unit Control Word (UCW) Selection

1. Make sure that switch A is set to the proper MPX setting (MPX 0 to MPX 6, depending upon model and features).

Switch C ↓	Unit-Control Words Selected (depends upon UCW capacity and switch-A setting)						
0	0,16	32,48	64,80	96,112	128,144	160,176	192,208
1	1,17	33,49	65,81	97,113	129,145	161,177	193,209
2	2,18	34,50	66,82	98,114	130,146	162,178	194,210
3	3,19	35,51	67,83	99,115	131,147	163,179	195,211
4	4,20	36,52	68,84	100,116	132,148	164,180	196,212
5	5,21	37,53	69,85	101,117	133,149	165,181	197,213
6	6,22	38,54	70,86	102,118	134,150	166,182	198,214
7	7,23	39,55	71,87	103,119	135,151	167,183	199,215
8	8,24	40,56	72,88	104,120	136,152	168,184	200,216
9	9,25	41,57	73,89	105,121	137,153	169,185	201,217
A	10,26	42,58	74,90	106,122	138,154	170,186	202,218
B	11,27	43,59	75,91	107,123	139,155	171,187	203,219
C	12,28	44,60	76,92	108,124	140,156	172,188	204,220
D	13,29	45,61	77,93	109,125	141,157	173,189	205,221
E	14,30	46,62	78,94	110,126	142,158	174,190	206,222
F	15,31	47,63	79,95	111,127	143,159	175,191	207,223
Switch A →	MPX 0	MPX 1	MPX 2	MPX 3	MPX 4	MPX 5	MPX 6

Figure 6. Selection of Unit Control Words

2. Set switch C to select the desired UCW's as shown in Figure 6.

3. Set switch D to select the desired byte from the selected UCW as follows:

Switch D Setting	Byte Selected	In UCW (depends upon setting of switches A and C)
0	0	First of two UCW's selected by switch C: If, for example, switch A selects MPX 0 and switch C selects UCW's 0 and 16 (Figure 6), switch D selects one of bytes 0 through 7 in UCW 0. (Thus, if switch D is set to 3, byte 3 of UCW 0 is selected.)
1	1	
2	2	
3	3	
4	4	
5	5	
6	6	
7	7	
8	0	Second of two UCW's selected by switch C: If, for example, switch A selects MPX 0 and switch C selects UCW's 0 and 16 (Figure 6), switch D selects one of bytes 0 through 7 in UCW 16.
9	1	
A	2	
B	3	
C	4	
D	5	
E	6	
F	7	

The format of the UCW's is shown in Figure 7. This section presents a description of the contents of UCW bytes.

Channel Status	Op and Flags Byte	Count		Data Address		Next CCW Address	
		High	Low	High	Low	High	Low
0	1	2	3	4	5	6	7

Figure 7. Unit Control Word Format

Channel Status Byte:

Bit	Function
0	Not Used (Channel Data Check) in 2030.
1	Channel Control Check
2	Interface Control Check
3	First Status Received*
4	Status Next *
5	Incorrect Length
6	Program Check
7	Protection Check

*Combinations of Bits 3 and 4 Indicate:

3	4	
0	0	Handling data; expecting data
0	1	Device instructed to stop; expecting status
1	0	Status stacked at control unit
1	1	Status is in Interrupt Buffer (IB)

Op and Flags Byte

Bit	Function
0	Chain Data Address (CDA)
1	Command Chaining (CC)
2	Suppress-Length Indication (SLI)
3	Skip
4	Program-Controlled Interrupt (PCI)
5	Active
6	Output (write)
7	Decrement Data Address

Current Program-Status-Word (PSW) Selection

The various portions of the current PSW can be displayed at any time that the CPU clock is off and the allow-write indicator is off.

PSW Field	Local Storage Address (Hexadecimal)
System Mask	B8
Protection Key	B9 (high-order four bits). The protection key can also be displayed from the Q-register.
ASCII Mode	B9 (bit 4)
Machine-Check Mask	B9 (bit 5)
Wait State	B9 (bit 6)
Problem State	B9 (bit 7)
Interruption Code	(available in old PSW in main storage, bits 16 through 31).
Instruction Length Code	8C (can also be decoded from the two high-order bits of the G register).
Condition Code	BB (high-order four bits) This is in a four-bit code to correspond to the branch-on-condition mask.
Program Mask	BB (low-order four bits)
Instruction Address	(available in IJ register)

SINGLE-INSTRUCTION PROCESSING

One method that can be used to debug programs is to process one instruction at a time, service all interruptions, and stop. The next instruction address is then displayed in the B- and A-register display.

To process one instruction at a time:

1. Press the Stop key (if necessary to stop processing), wait for the Manual light to come on, and then set the Rate switch to the instruction step position (see Figure 2).

2. Press the Start key to process each instruction and service all pending interruptions.

When this procedure is used, the program is run basically in the same way as during normal processing except that the operation is much slower. Data exchanged between the CPU and I/O devices is not lost when the Rate switch is used as just described. Note, however, that I/O interruptions may occur at different times in the sequence of instructions being processed in single-cycle mode as contrasted with normal instruction processing. That is, an I/O interruption indicating completion of an I/O operation for a relatively slow I/O unit may occur before the start key is pressed for execution of the next instruction. In normal program processing this interruption may occur after several other instructions have been processed. If this difference in time-of-occurrence of an interruption can affect expected program results, a segment of the program should be run (for check-out purposes) rather than only one instruction at a time.

When the CPU stops, the address of the next instruction to be processed is displayed in the B- and A-register indicators.

SINGLE-CYCLE, DISPLAY, AND STORE OPERATIONS

Although single-cycle operations are intended primarily for Customer Engineering use, you may wish to examine the contents of, or store information into, various registers. An instruction can be processed one machine-cycle at a time and the system stopped after the cycle is completed. To perform this operation:

1. Use the procedure described under Single-Instruction Processing to arrive at the desired instruction. The address of the next instruction to be processed is displayed in the B- and A-registers (Part 2 of Figure 4).

2. Place the rate switch in the single-cycle position (see Figure 2).

3. Press the start key once for each machine cycle desired.

At the completion of any machine cycle you can display or store information. (Note that the methods of storing or displaying storage data are presented in other sections of this publication.) The selection is made with the Display-Stor-Sel switch (switch E):

1. With the Manual light on, set the display-storage-select switch to the desired location.

2. For display of the selected location, press the Display key.

3. To store data, set the appropriate hexadecimal representation of the information to be stored into switches H and J. Press the Store key.

Figure 8 indicates the general functions of the various areas that can be selected and where they are displayed during display operation. It is important to realize that data overruns can occur during single-cycle operations. Therefore, data sent to or from an I/O device can be lost and the resulting console indications may not be exactly what is expected.

PROCESSING A PROGRAM SECTION

To examine the results caused by processing a section of a program, use the following procedure:

1. Set the desired stop address in switches A, B, C, and D and place the Address-Compare switch (see Figure 2) in the SAR delayed stop position.

2. Load the program as described in the Program-Load Routine section.

3. If the load program clears storage, press the Start key after the first stop. Press the Start key again after the second stop (this stop occurs when the program is being loaded). The third stop then occurs after execution of the instruction (including all pending interruptions) in which the address match occurred. You can now examine conditions produced by the processing of the program segment. Subsequent instructions can then be processed, one at a time, by using the procedure described in the Single-Instruction Processing section.

The program may use the Interval Timer feature. If so, the Interval Timer may decrement through zero after the system has processed a program segment and then entered the stopped state. Then, when you restart the program, an interval timer interruption will occur and you may not obtain the desired results. If your program depends upon the Interval Timer but you do not want to have interval timer interrupts while checking out a program segment, set the Interval Timer switch to the OFF position (see Figure 2, lower left).

STARTING AT A SPECIFIC INSTRUCTION (SET IC) PROCEDURE

1. Press the Stop key.

2. Set the desired instruction address in switches F, G, H, and J.

3. Press the Set-IC key.

4. Press the Start key.

Note: If an invalid address is entered, a machine-check error will occur. The Check Reset key can be used to clear this check condition.

Program processing starts at the instruction address that was set into switches F, G, H, and J. If you desire to stop just after a particular instruction has been processed, use the procedure described in the Process a Section of a Program section.

An important point to note is that your program segment may start in problem mode and stop in supervisor mode. If you then attempt to start at an instruction (by using the set-IC routine) that should be handled in problem mode, the system "sees" the problem instructions as if they were in supervisor mode. (A program interruption occurs if a privileged instruction is encountered in the problem state.) The program run may then give different results than expected. Therefore, you should know, from your program, what mode you are in when starting and stopping the program segment. If you are not sure, you can display local storage location address B9 (hexadecimal). Bit 7 of this location is the problem/supervisor bit of the current PSW. When this bit is a zero, the CPU is in the supervisor mode; when it is a one, the CPU is in the problem mode.

If you are not in the desired mode, you can manually alter bit 7 of local storage location B9. Anyone performing this type of operation, however, should have an intimate knowledge of the program being used.

Other fields in the current PSW may have to be altered due to the requirements of your program segment. To avoid performing a number of manual store operations, you can use the following procedure:

1. Store a PSW in main-storage address 0. (Anyone performing this type of operation should have an intimate knowledge of the program being used because certain IBM programming systems use main-storage addresses 0, 1, 2, etc for other purposes.) This PSW is loaded with information that applies to your program segment. For example, the mode (problem or supervisor) system mask, and instruction

Register to be Displayed	Usual Function	Where Displayed
I	Instruction Address (high-order bits)	A-register (also the high-order eight bits of the main-storage address register if the allow-write indicator is off)
J	Instruction Address (low-order bits)	A-register (also the low-order eight bits of the main-storage address register if the allow-write indicator is off)
U	Data Address (high-order bits)	A-register (also the high-order eight bits of the main-storage address register if the allow-write indicator is off)
V	Data Address (low-order bits)	A-register (also the low-order eight bits of the main-storage address register if the allow-write indicator is off)
L	Data Length	A-register
T	Auxiliary Storage Address	A-register
D	General Purpose Data Register	A-register
R	Storage Data Register	A-register (Also has own display in main-storage data-register indicators)
S	Status (CPU)	A-register
G	Instruction Operation Code	A-register
H	Priority Status Register	A-register
*FI	Multiplexor Channel Bus-In	A-register
*FT	Multiplexor Channel Tags	A-register
Q	Storage-Protection key in PSW (High 4-bits) Storage-Protectection key of block of storage just used (low 4-bits)	A-register
*C	Interval Timer Count	A-register
*F	External Interrupt: Interval Timer (bit 0) Console (bit 1) Six direct-control interrupts (bits 2 through 7)	A-register
*TT	1050 Documentary Console Tags	A-register
*TI	1050 Documentary Console Bus-In	A-register
*JI	Direct Control Bus-In	A-register
*GS	Selector Channel One Status	A-register
*GT	Selector Channel One Tags	A-register
*GUV-GCD	GUV contains storage address for data for selector-channel one. GCD contains the current byte count for selector-channel one	GUV in main-storage address register. GCD in count register (18 bits each).
*HS	Selector Channel Two Status	A-register
*HT	Selector Channel Two Tags	A-register
*HUV-HCD	HUV contains storage address for data for selector-channel two. HCD contains the current byte count for selector-channel two.	HUV in main-storage address register. HCD in count register (18 bits each)

Note: *Indicates that you cannot manually store data in the designated register

Figure 8. Display

address loaded indicate the system state at the starting point of your program segment.

2. After each run of your program segment you can then press the System-Reset key once. Then press the Start key twice. This procedure allows you to start, using the PSW in location 0.

MANUAL INTERVENTION

Various conditions may arise that require some type of manual operation to be performed. For example, the hopper on a card reader may empty (it must be reloaded by the operator). Lights on the various I/O units indicate the condition of the I/O units (refer to the specific I/O device publication for information). The 2030 console, however, does not explicitly indicate I/O device conditions. In a basic card system (for example: a CPU, a printer, a 1052 Printer Keyboard, and a card read-punch), indicators on the I/O units can be inspected with little difficulty. As the number of I/O units increases, however, it becomes increasingly difficult for the operator to see the indicators on all the I/O units.

How does the operator know when an I/O unit requires manual attention? A variety of methods can be used. Each depends upon the operating procedures at the installation. Procedures that can be used are:

- Messages in Main Storage. Messages to the operator can be placed in storage locations (such as 0, 1, 2, and 3) and the system programmed to enter the wait state. When wait state is entered, the operator can examine the message and perform any necessary action. The programmer should supply information (to the operator) that describes what the messages signify.

  Note: The system should be programmed to enter wait state if it cannot proceed because data is unavailable from an I/O unit (card reader out of cards).

- If an IBM 1052 Printer-Keyboard is used, the program can be written to type out messages to the operator when I/O units require attention.

- The program can be written to sound the alarm (special feature) whenever an I/O unit requires attention. One of the preceding procedures can then be used to provide more specific information.

MICROPROGRAM TEST ROUTINES

Several test microprograms, normally used by the IBM Customer Engineer, that are stored in ROS can be useful to the programmer and operator. Be sure that all console switches are reset before normal programming operations are resumed.

Note: These tests disregard storage-protection requests. Care must be exercised so as not to unintentionally alter useful data.

BASIC TEST

This test exercises basic components of the system and is used to detect malfunctions caused by CPU circuitry. Functions that control read/write storage and the I/O channels are not tested by this ROS routine.

The basic test is initiated when the system is restarted after a System Reset or when an IPL procedure is performed, unless the Check Control switch is set to Disable. The test loops 128 times: it is normal for all machine-check lights to flash on and off.

DISPLAY READ/WRITE STORAGE

This test can be used to display successive main-storage locations as follows:

1. Set the Check Control switch to Stop.

2. Press the System Reset key.

3. Enter the address of the first location to be displayed, using switches F, G, H, and J and then press the Set IC key.

4. Enter ROS address 0BF7, using switches, F, G, H, and J, and the ROAR Reset key.

5. Press the Start key to display succeeding locations in the main-storage data register.

ALTER READ/WRITE STORAGE

This test can be used to alter the contents of successive main-storage locations as follows:

1. Set the Check Control switch to Stop.
2. Press the System Reset key.
3. Enter the address of the first location to be altered using switches F, G, H, and J, and then Set IC key.
4. Enter ROS address 0BF6, using switches F, G, H and J, and the ROAR Reset key.
5. Enter the desired character(s) from switches H and J. Press the Start key for each consecutive byte to be altered. The microprogram stops after each location is altered. This step is repeated as many times as required.

ALTER A BLOCK OF READ/WRITE STORAGE

This test can be used to alter the contents of a specified block of main storage. The character set in switch H and J is loaded into all locations, starting at the address initially set in switches F, G, H, and J, and ending with the location addressed by switches A, B, C, and D.

1. Set the Check Control to Stop.
2. Press the System Reset key.
3. Enter the address of the first location to be altered, using switches F, G, H, and J, and then press the Set IC key.
4. Enter ROS address 0BF6, using switches F, G, H, and J, and the ROAR Reset key.
5. Enter the address of the last main-storage location to be affected from switches A, B, C, and D.
6. Set the Address Compare switch to SAR Stop.
7. Set the ROS Control switch to Inhibit CF Stop.
8. Enter the desired character in switches H and J. (Use 00 to reset the block.)
9. Press the Start key. The system stops after the location addressed by switches A, B, C, and D has been altered.

The IBM 1052 Printer-Keyboard is the basic console printer-keyboard for the System/360 Model 30. Communication between operator and program is, therefore, effected through the 1052. Besides the 1052, a variety of IBM 1050 console devices is available to increase the flexibility of the system. These devices (including the 1052) are attached to the IBM 2030 Processing Unit through an IBM 1051 Control Unit and the 1051 Attachment feature, which is located in the 2030.

The maximum number of 1050 console devices attachable through this feature are:

- One keyboard
- Two printers
- One reader (either card or paper tape)
- One punch (either card or paper tape).

These devices can be operated separately from the 2030 (even if CPU power is off) on a 24-hour basis. Additional use-rental is not charged for the 2030 while the 1050 devices are used in this manner. This type of operation is called off-line (off-line signifying that the 1050 devices are not being used in operations that affect the 2030). Off-line operation provides for media conversion (such as transferring data from card to paper tape), card or paper tape listing or preparation, and other 1050 operations that do not depend on 2030 functions.

Interdependent operations between the 2030 and the console devices are termed on-line operations. An example is an operator request for information from the 2030 by means of the IBM 1052 Printer-Keyboard.

Additional flexibility is gained through a data communications link. Here the local 1050 devices (located near the 2030) can exchange information with up to 26 remote 1050 terminals. This communication link can be operated off-line only. That is, messages sent and received by the local 1050 devices are not controlled and not sent or received by the 2030. The local 1050 I/O devices not being used in the data communications link can, however, be operated on-line with the 2030. This operation can occur at the same time as the off-line data communications operation.

To distinguish between data communications operations and local operations we use the terms line loop and home loop. Home loop 1050 device operations can be on-line to the 2030 or off-line, as already described, among the local 1050 devices. Line loop refers to operations on the communications line. These operations can occur only between local 1050 devices and remote 1050 terminals that all operate off-line to the 2030.

To summarize:

1. On-line refers to operations between devices and the 2030.
2. Off-line refers to operations that do not involve the 2030.
3. Home loop refers to operations on a local basis, either on-line or off-line.
4. Line loop refers to communications line operations.

Because the usage of I/O devices can become critical in time-dependent applications, it is important that the programmer fully understand the meanings of the terms on-line and off-line.

Off-line line-loop operations require an IBM 1051 Model 1 Control Unit with the Master Station feature. The 1051 Model 1 has two control unit data loops:

1. One of these, called the home loop, can be operated on-line or off-line to the 2030.
2. The other, called line loop, has data communication capabilities and can be operated only off-line with respect to the 2030.

Local 1050 devices can be transferred to operate on one loop or the other (line loop or home loop) by switches on the local units.

Multiplexor Channel Address

The unit address of the 1050 console is a fixed multiplexor channel address. In a 2030 with 8,192 positions of main storage, the 1050 console address is always 1F (hexadecimal). System/360 Model 30

processing units that have 16,384 or more positions of main storage use address 1F or 5F for the 1050 console (one or the other, not both). This arrangement allows for the possibility of two systems connected through the channel-to-channel adapter. If, for example, a system with 16,384 storage positions is connected to a system with 8,192 storage positions, both systems use 1F as the address for the 1050 console. Hence, communication is provided to a console from either system.

If a system has the 224 subchannels feature, the console address can be 1F, 5F, or DF (only one, not any combination). The 1050 attachment can be selectively assigned to be first or last in terms of multiplexor-channel polling priority.

Address 09 can also be used in any 2030 for the 1050 multiplexor-channel address. The desired address is set by the Customer Engineer at installation time.

IBM 1052 Lights, Switches, and Functional Keys

The following describes the 1050 lights, switches, and functional keys for on-line 1050 home-loop operation.

The IBM 1052 Printer-Keyboard models that can be used with System/360 Model 30 are:

1. Model 3 (Figure 9) is used whenever the IBM 1051 Model 1 Control Unit is used in the console configuration.

2. Model 5 (Figure 10) is used with the IBM 1051 Model N1 Control Unit when 1050 I/O components or features requiring switches (in addition to the basic IBM 1052 Printer-Keyboard) are used in the system.

3. Model 6 (Figure 11) is used with the IBM 1051 Model N1. Model 6 provides switch control for the basic IBM 1052 Printer-Keyboard, but it does not provide the capability for adding more 1050 I/O devices or features that require switches. The 1052 Model 6 can be obtained only on an "as available" basis. (See your IBM representative.)

   If the Systems Console Attachment Feature is installed in the 1051 Model N1 and in the 1052 Model 6, certain functions are inoperative:

   - When a command is sent to the Model 6 to tab, backspace, or line feed, the 1052 spaces.
   - No action occurs when a ribbon shift and line-feed select is received by the Model 6.
   - Tab, Backspace, and Line-feed keys do not function.

   Any programs that provide for these functions will operate, but the functions will not be performed.

4. The 1052 Model 8 (Figure 12) is used with the IBM 1051 Model N1 and replaces the 1052 Model 6 as the standard console keyboard. Model 8 provides the basic mechanisms and functions necessary in a system console environment. This model provides switch control for the basic IBM 1052 Printer-Keyboard, but it does not provide the capability for adding more 1050 I/O devices or features that require switches.

   The Tab, Backspace, and Line-feed keys are blank and the functions associated with these keys are not provided in the 1052 Model 8. Also, no action occurs when a ribbon shift and line feed select is received by the 1052 Model 8. Any problem program written to control these functions will operate with Model 8, even though the functions are not performed. Whenever one of the codes representing one of these functions is sent to the Model 8, a space with no printing occurs. Prefix codes are accepted by the 1051 with attached 1052 Model 8, but the prefix character and the printable character in the prefix sequence are ignored.

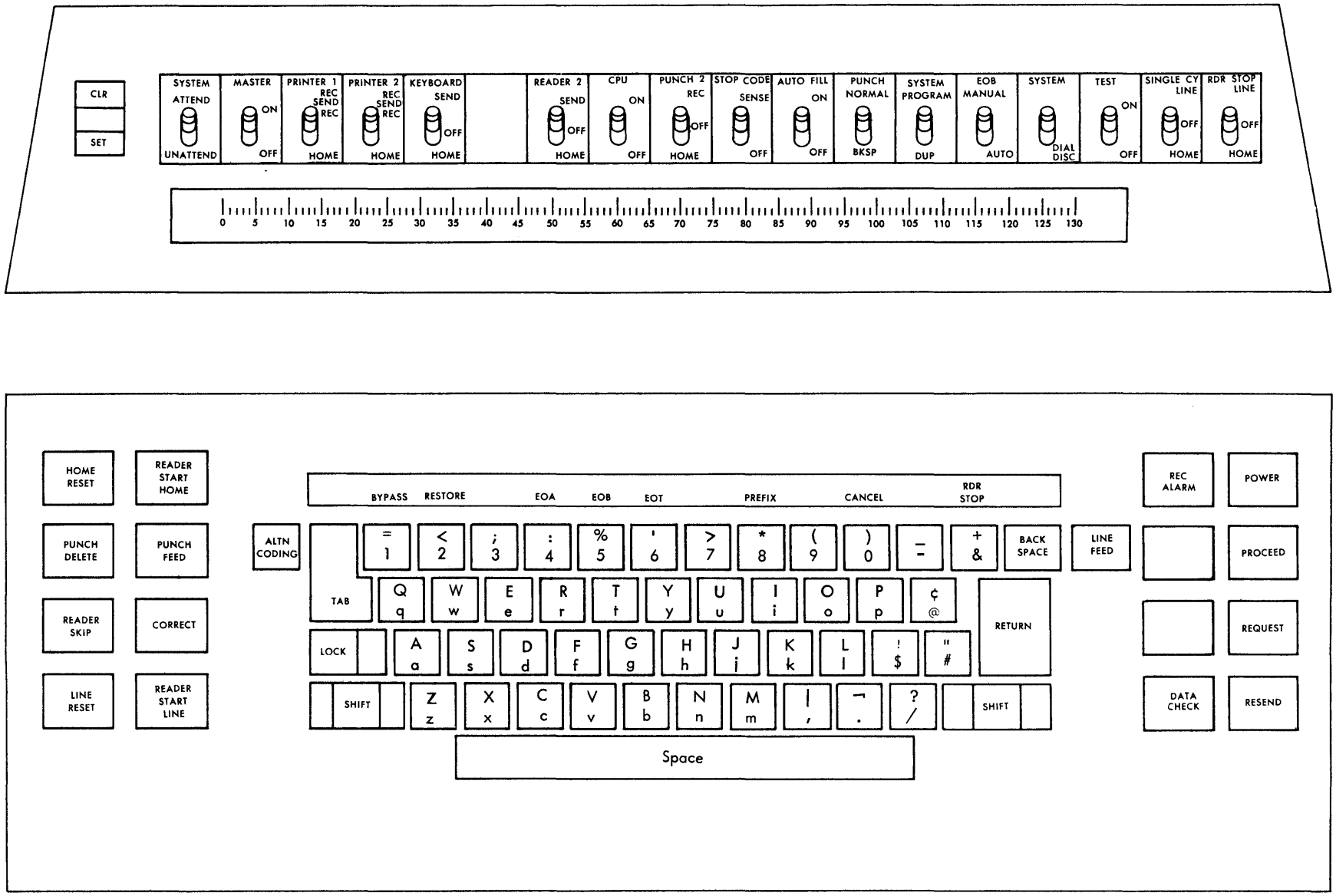


Figure 9. IBM 1052 Model 3 Keyboard and Switch Panel

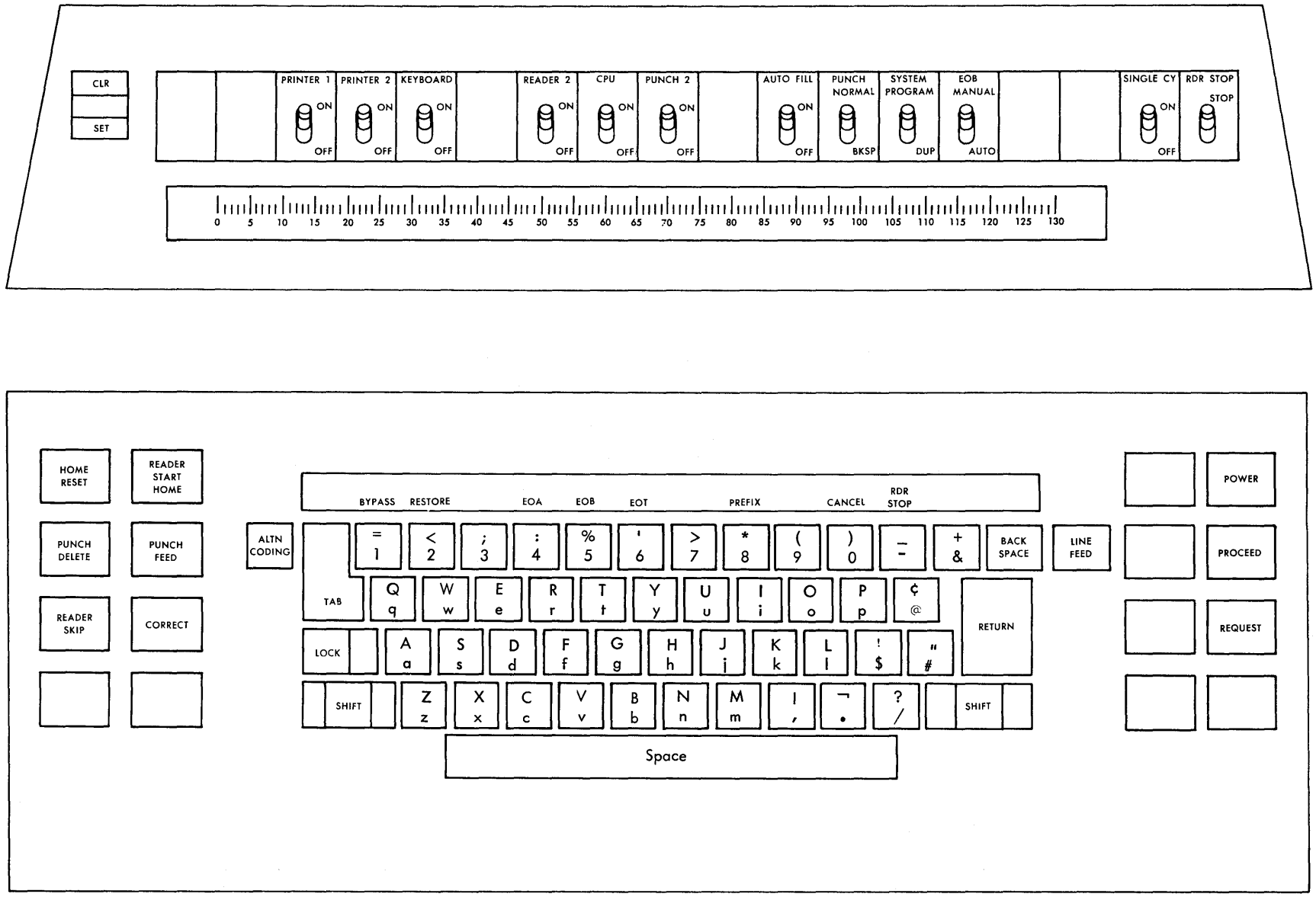


Figure 10. IBM 1052 Model 5 Keyboard and Switch Panel

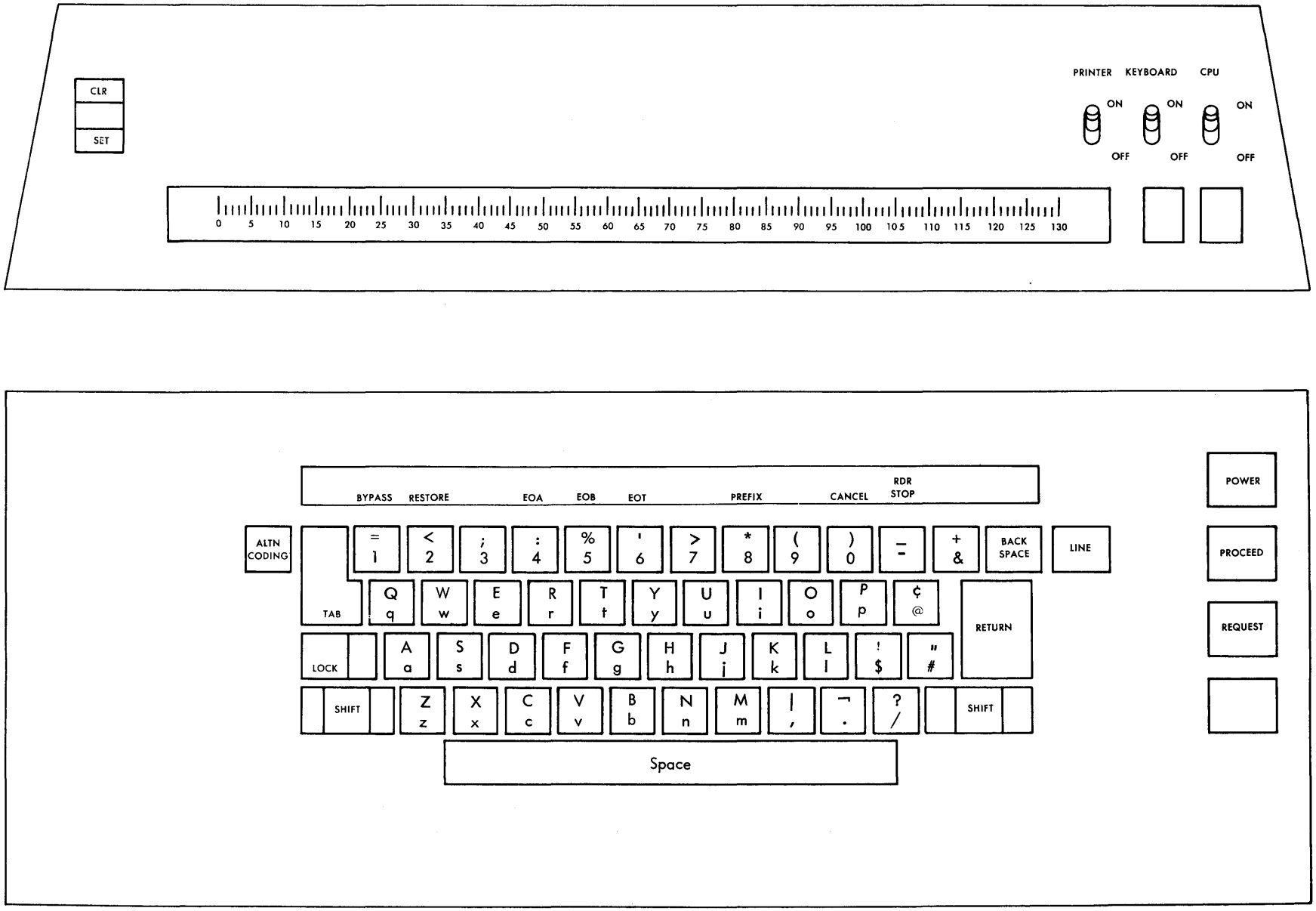


Figure 11. IBM 1052 Model 6 Keyboard and Switch Panel

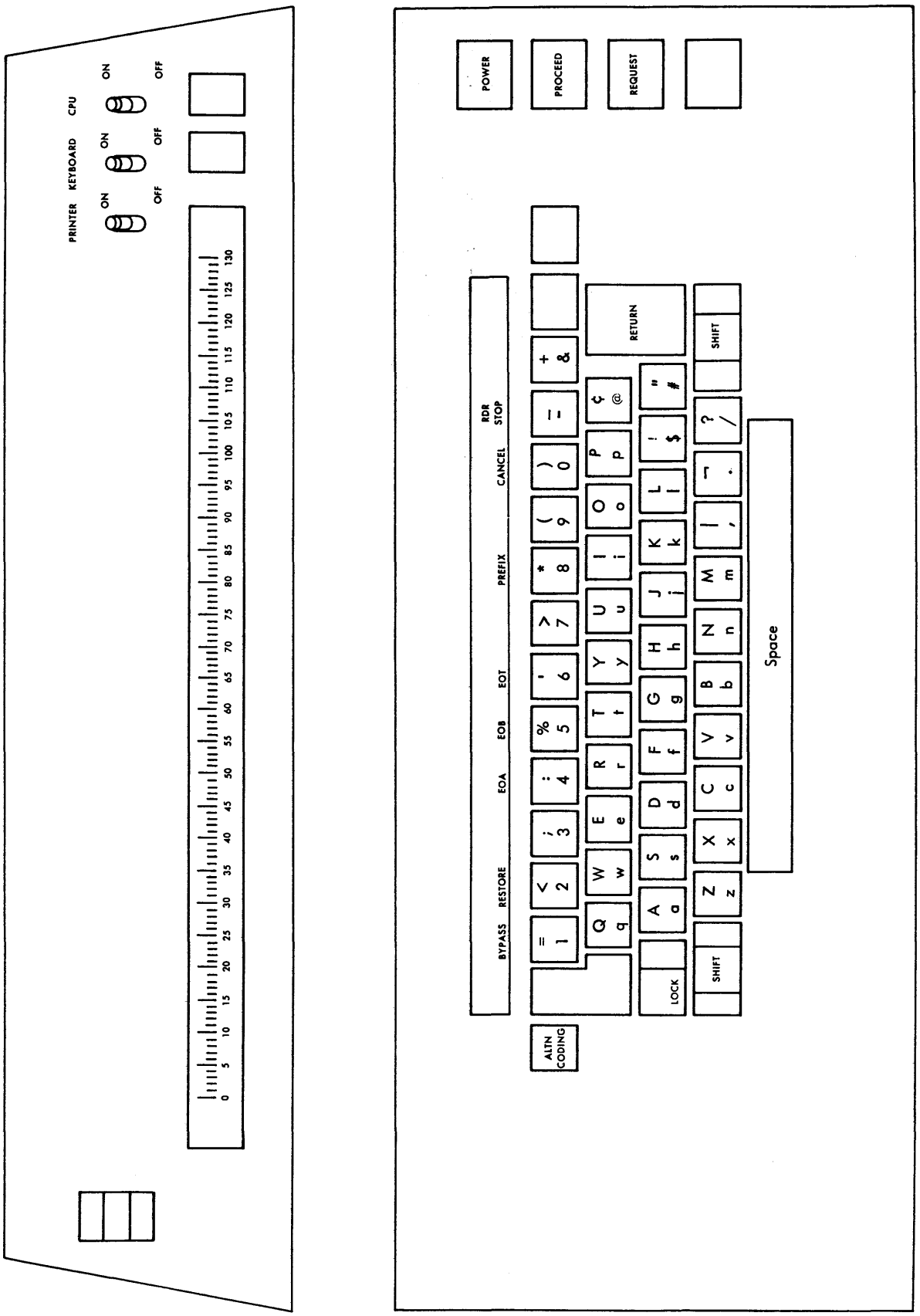


Figure 12. IBM 1052 Model 8 Keyboard and Switch Panel

The following items are standard on the Model 8:

- A 13 1/8 inch pin feed platen,
- A 12 1/2 inch (maximum) printing line,
- Six lines per inch line feeding, and
- Character spacing of ten per inch

No additional special features are available for the Model 8.

Also, the following functions and manual controls are removed or inoperative on the Model 8:

- Left and right margin set (the left and right margins are fixed),
- Single-double index lever,
- Paper release bar,
- Tab clear-set lever,
- Ribbon shift lever,
- End-of-line bell, and
- Pressure feed rolls.

The Systems Console Attachment Feature is required (in the 1051 Model N1) to attach a 1052 Model 8.

CPU Connect Switch

CPU On. In the CPU-on position, this switch connects the 1050 to the CPU. If all dc power is on in the 1051 when this switch is thrown to the on position, a 1050 operational signal results. A transition from 1050 not-operational to 1050 operational initiates a 1050 ready interrupt with the device-end bit on in the CSW.

CPU Off. In the off position, this switch takes the 1050 system completely off-line. Any 1050 read or write commands are then rejected with condition code 3 (device not operational). When the CPU connect switch is returned to the home or on position, a ready condition interrupt with device-end status is initiated.

Request Key

Pressing the request key causes an attention status to be established in the 1051 attachment. The 1051 attachment holds this attention status until the 1051 attachment becomes available, at which time an attention interrupt is initiated in the CPU.

Proceed Light

The proceed light indicates that the 1051 attachment channel is available for operator-initiated keyboard and/or Reader-2 input through the 1051 home loop. When the proceed light is on, the keyboard is unlocked and an interlock is removed from Reader 2.

System Program/Duplicate Switch

Program Position. Two-character program control sequences from any source cause the proper component control, and the two-character sequences are not printed or punched. During a read command, neither character of a two-character control sequence is stored.

With the 1051 Home Component Recognition feature, an output other than the first printer must have its home-component-recognition latch turned on by a two-character program control sequence as well as having its assignment switch in the home position to satisfy the output select and ready interlock to the 1051 attachment during write commands.

Duplicate Position. With this switch in the duplicate position:

1. Manual component assignment is required and the 1051 Home Component Recognition special feature is not effective.
2. The prefix code is not printed or stored, but it is punched. The following numeric or alphabetic character is then stored, printed, and punched.
3. The output select and ready interlock to the 1051 attachment is not dependent upon any of the output home-component-recognition latches being on.

Auto-Fill Switch (with the 1051 Auto-Fill Special Feature)

In the on position, fill characters (idle code) are automatically generated by the 1051 during the execution time of printer functions such as new line and tab. Write commands are interlocked during the same period of time. On read commands, the idle codes are not read into storage.

In the off position, fill characters (idle code) are not generated.

System Attend/Unattend Switch (1051 Model 1 Only)

This switch must be in the attend position for all on-line operations, or the 1051 will not indicate an operational condition to the 2030-1051 attachment.

1050 Intervention-Required Light (on 2030 Console)

This light turns on whenever a command execution is terminated with an intervention-required condition. It is reset by the next 1050 read or write command, or by a 2030 system reset.

1050 Request Light (on 2030 Console)

This light turns on whenever the 1050 request key on the 1052 is pressed. It is reset when attention status is recognized by the attachment and accepted into the unit status register.

I/O Assignment Switches

The I/O assignment switches transfer the various 1050 I/O devices to the desired 1050 loop, or they disconnect them from the 1050 completely. When the 1050 home loop is switched to on-line operation (CPU connect switch on), the devices that are to be made available to the CPU must have their switches in the home position.

Alternate-Code Key

When the alternate code key is held down while a numeric key is pressed on the 1052, a 1050 control character is generated.

Alternate Code--Zero (Cancel). Whenever the alternate-code key and the zero key are pressed, a unique cancel character is generated that terminates the keyboard entry with channel-end, device-end, and unit-exception statuses. The cancel character is not read into storage.

Alternate Code--Five (EOB). Whenever the alternate code key and the 5-key are pressed, an EOB (End of Block) character is generated. This initiates a normal end to the keyboard entry. The EOB character is not read into storage. Alternate code six (EOT) produces the same function as EOB.

For a description of other standard or optional 1050 lights, switches, and manual controls, refer to IBM 1050 Operator's Guide, Form A24-3125.

Read Inquiry

To send data from the 1050 to 2030:

1. Make sure that 1050 power is on and the CPU connect switch is in the on position.

2. Press the request key.

3. Wait for the proceed light (on 1052) to turn on.

4. Make sure that the keyboard switch is in the home or on position if you wish to enter data from the 1052.

5. Make sure that the Reader-2 switch is in the home or on position if you wish to enter data from a 1054 or 1056.

6. Enter data. You can enter data alternately from the keyboard and reader (either paper tape or card). Assume that you enter data from the 1052 first. Then press the home-reader start key to enter data from the reader. The 1052 keyboard is locked when the home-reader start key is pressed.

7. Reading from the reader can be transferred back to the keyboard by:

   a. A reader stop code read in the card (or paper tape).
   b. Pressing the home-reader stop key on the 1052.

   Note: The normal procedure is to use step "a" so that text reading will not inadvertently be stopped at the wrong point in the message.

8. The operation can be continued by entering data from the 1052 (the keyboard is unlocked when Reader 2 is stopped--step 7).

9. To stop the operation from the 1052:

   a. Press and hold the alternate code key.
   b. Press the 1052- 5-key (EOB) or the 6-key (EOT).

10. To stop the operation from Reader 2:

    a. The EOB (or EOT) character is read (after the last data character is read) from tape, or
    b. The EOB (or EOT) character is read from the card or the trailing edge of the card feeds far enough to generate the stop.

11. At the end of the operation, the proceed light turns off. The keyboard is locked and an automatic carrier return and line feed is attempted to any 1050 printer copying the input.

Note that 1050 operations with the 2030 are under control of the program. That is, the preceding operations can be accomplished only if the program controlling the 2030 is written to recognize requests from the 1050 devices.

The operation can also be stopped by the channel. This stop occurs when the CCW (Channel Command Word) byte count goes to zero. If data was being entered from the 1052, the proceed light is turned off, the keyboard is locked, an automatic carrier return and line feed is initiated to any 1050 printer copying the input, and a hold condition is placed on Reader 2.

If the data was being read from Reader 2, the attachment remains busy until EOB is detected. No more data characters are then transferred to storage. If the count was N, and data is from the keyboard, the N + 1 character prints (if a printable character) but is not transferred to storage. If data was being entered from Reader 2, all printable characters up to EOB/EOTprint (unless the printers are deselected or in the bypass mode).

At EOB, the proceed light is turned off. The keyboard remains locked. A hold condition is placed on Reader 2. An automatic carrier return and line feed is initiated to any 1050 printer copying the input.

Cancel Operation

A cancel operation can be initiated from the keyboard during a read inquiry at any time after the proceed light comes on, provided the keyboard still has control (the reader start key has not been pressed).

A cancel operation is executed by pressing the alternate-code key and the zero key while still holding the alternate-code key down.

The read inquiry operation is then terminated. The proceed light is turned off. The keyboard is locked, a hold condition is placed on Reader 2, and an automatic carrier return and line feed is initiated. The cancel character is not transferred to storage. Programming determines what is done to the data characters transferred to storage before the cancel character is generated.

Read-Inquiry Command (with Home Component Recognition Feature)

With the Home Component Recognition feature active in the 1051, the read-inquiry command functions as described in the following paragraphs.

Initial Selection Initiated by Start I/O Instruction

Printer 1 (either 1052 or 1053) is automatically selected for monitoring.

Execution of Read-Inquiry Command

If the operator desires a different or an additional output to monitor during the inquiry operation, he can:

1. Prefix outputs on and off from the keyboard before entering data, or

2. Put the PROG/DUP switch in the DUP mode and manually switch-select the desired monitoring outputs. (He must return the switch to program mode before entering EOB.)

If the operator presses the home reader Start key to enter his inquiry from Reader 2, the adapter continuously tests for Reader 2 select-and-ready during that portion of the inquiry operation.

End Operation

At the end of each read inquiry command, all 1050 output devices are deselected.

Carrier Return

When operating on-line, if the carrier reaches the right margin without a carrier return signal from the program, the carrier returns automatically and a single line feed occurs. Printing is suppressed during the carrier return.

Off-Line 1050 Functions

Home Component Recognition operates in its normal manner when the 1050 is operated off-line.

1050 I/O Prefix Selection

Printer 1	Prefix 1
Printer 2	Prefix 2
Punch 2 on	Prefix 4
Printer 1 off	Prefix 5
Printer 2 off	Prefix 6
Punch 2 off	Prefix 8
*Ribbon Shift up	Prefix A
*Ribbon Shift down	Prefix B
*Single-Line Feed	Prefix C
*Double-Line Feed	Prefix D

*Requires Automatic Ribbon Shift and Line Feed Select feature in the 1051.

Note: When the 1050 is operating on-line, Reader 1, Reader 2, and Punch 1 are always automatically selected on.

Operations Terminated by Intervention-Required

If the execution of a command is terminated by an intervention-required status:

1. An automatic carrier return and line feed is attempted but may not be executed to monitoring printers. The carrier may have to be returned from the keyboard off-line, after the cause of the intervention-required condition is removed, and before the 1050 is returned to on-line operation.

2. If paper tape was being read, the paper tape reader stops within the record being read. The paper tape must be manually repositioned after the cause of the intervention-required condition is removed and before the 1050 is returned to on-line operation.

3. If cards were being punched or read, the punch or reader stops within the card being processed. The cards must be manually released or ejected.

Halt I/O

Keyboard Entry

If a halt I/O command is executed during a keyboard entry, the operation is terminated immediately. The keyboard is locked and the proceed light is turned off. Channel-end status and device-end status are established, and an automatic carrier return and the line feed is initiated. Any chaining flags are turned off.

Write

If a halt I/O command is executed during a write command, the current write command is terminated immediately. Channel-end status and device-end status and an interrupt condition are established. An automatic carrier return and line feed is initiated. Any chaining flags are turned off.

Read from Reader 2

If a halt I/O command is executed during a read command, the data transfer is terminated and channel-end status and an interrupt condition are established. The attachment and 1050 remain busy until the normal end of media is reached, at which time device-end and an interrupt condition are established. Any chaining flags are turned off. An automatic carrier return and line feed is initiated to any monitoring printers.

Codes

The following automatic translation is performed between the 1050 PTTC/EBCD and the System/360 EBCDI code. For the PTTC/EBCD code refer to Figure 13; for the EBCDI code, Figure 14.

Input

The following codes are translated on input:

26 Lower-case alphabetic (a through z)

26 Upper-case alphabetic (A through Z)

10 Numeric (0 through 9)

26 Special graphics #@/,-$&.=<;:%'>*)"(¢?
_└¬+!

4 Printer control codes (line feed, new line, tab, backspace)
1 Space/blank
93 Total

All other 1050 control codes are deleted and not entered into storage.

Output

The following codes are translated on output:

26 Lower-case alphabetic (a through z)

26 Upper-case alphabetic (A through Z)

10 Numeric (0 through 9)

26 Special graphics #@/,-$&.=<;:%'>*)"(¢?
_!|¬+

1 Space/blank

16 1050 control codes

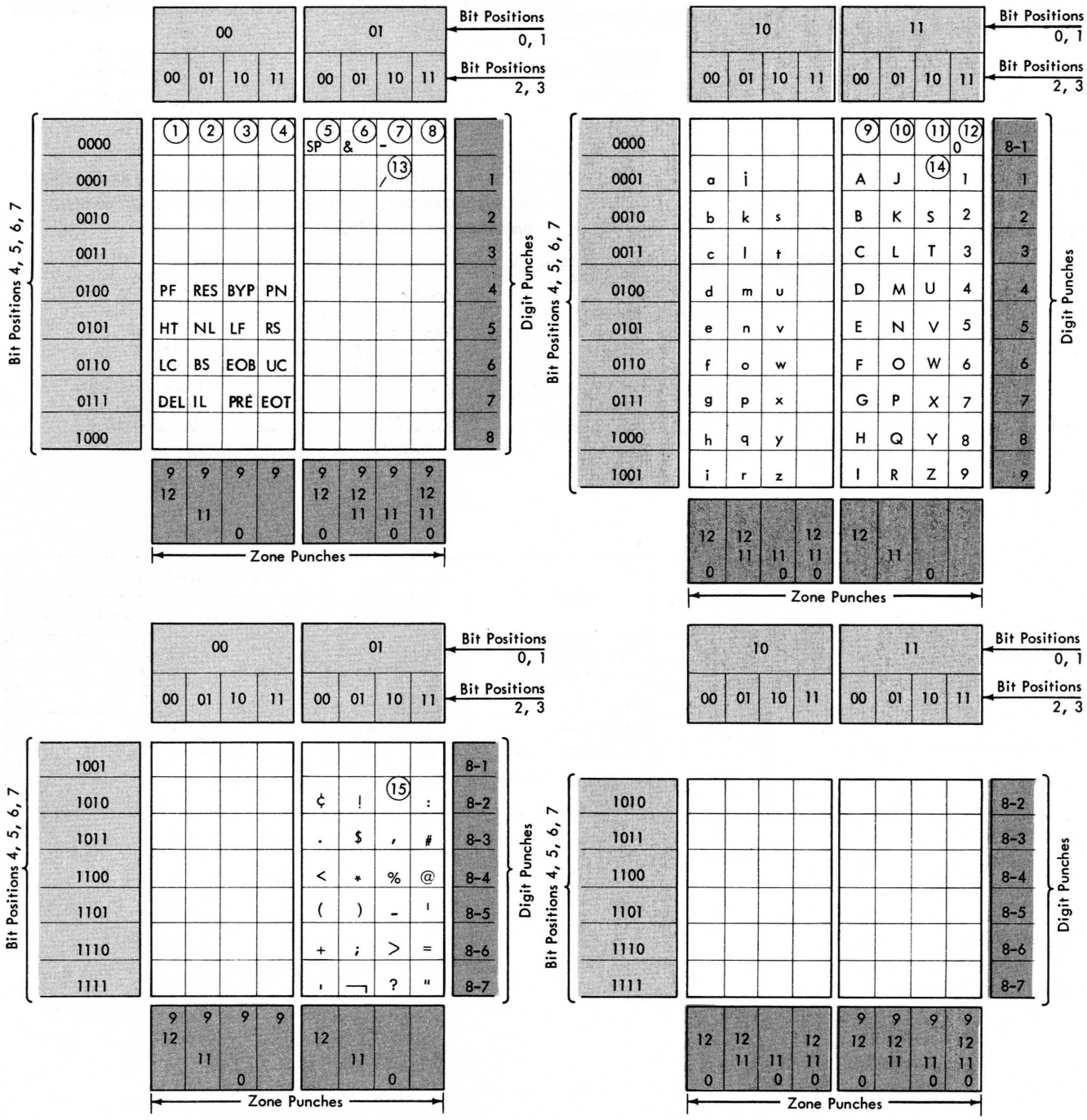
105 Total

UPPER CASE						
	PTTC/EBCD					
Character	B	A	8	4	2	1
Space						
A	B	A				1
B	B	A			2	
C	B	A			2	1
D	B	A		4		
E	B	A		4		1
F	B	A		4	2	
G	B	A		4	2	1
H	B	A	8			
I	B	A	8			1
J	B					1
K	B				2	
L	B				2	1
M	B			4		
N	B			4		1
O	B			4	2	
P	B			4	2	1
Q	B		8			
R	B		8			1
S		A			2	
T		A			2	1
U		A		4		
V		A		4		1
W		A		4	2	
X		A		4	2	1
Y		A	8			
Z		A	8			1
+		A				
¬	B	A	8		2	1
–	B					
⊥	B		8		2	1
¢		A				
?		A				1
!		A	8		2	1
=						1
<					2	
;					2	1
:				4		
%				4		1
'				4	2	
>				4	2	1
*			8			
(			8			1
)			8		2	
"			8		2	1
PF (Punch Off)	B	A	8	4		
HT (Horizontal Tab)	B	A	8	4		1
LC (Lower Case)	B	A	8	4	2	
DEL (Delete)	B	A	8	4	2	1
RES (Restore)	B		8	4		
NL (New Line)	B		8	4		1
BS (Backspace)	B		8	4	2	
IL (Idle)	B		8	4	2	1
BYP (Bypass)		A	8	4		
LF (Line Feed)		A	8	4		1
EOB (End of Block)		A	8	4	2	
PRE (Prefix)		A	8	4	2	1
PN (Punch On)			8	4		
RS (Reader Stop)			8	4		1
UC (Upper Case)			8	4	2	
EOT (End of Transmission)			8	4	2	1

LOWER CASE						
	PTTC/EBCD					
Character	B	A	8	4	2	1
Space						
a	B	A				1
b	B	A			2	
c	B	A			2	1
d	B	A		4		
e	B	A		4		1
f	B	A		4	2	
g	B	A		4	2	1
h	B	A	8			
i	B	A	8			1
j	B					1
k	B				2	
l	B				2	1
m	B			4		
n	B			4		1
o	B			4	2	
p	B			4	2	1
q	B		8			
r	B		8			1
s		A			2	
t		A			2	1
u		A		4		
v		A		4		1
w		A		4	2	
x		A		4	2	1
y		A	8			
z		A	8			1
&	B	A				
.	B	A	8		2	1
-	B					
$	B		8		2	1
@		A				
/		A				1
,		A	8		2	1
#			8		2	1
1						1
2					2	
3					2	1
4				4		
5				4		1
6				4	2	
7				4	2	1
8			8			
9			8			1
0			8		2	
PF (Punch Off)	B	A	8	4		
HT (Horizontal Tab)	B	A	8	4		1
LC (Lower Case)	B	A	8	4	2	
DEL (Delete)	B	A	8	4	2	1
RES (Restore)	B		8	4		
NL (New Line)	B		8	4		1
BS (Backspace)	B		8	4	2	
IL (Idle)	B		8	4	2	1
BYP (Bypass)		A	8	4		
LF (Line Feed)		A	8	4		1
EOB (End of Block)		A	8	4	2	
PRE (Prefix)		A	8	4	2	1
PN (Punch On)			8	4		
RS (Reader Stop)			8	4		1
UC (Upper Case)			8	4	2	
EOT (End of Transmission)			8	4	2	1

Figure 13. Perforated Tape and Transmission Code/EBCD

Figure 14 shows bit positions, bit patterns, card-punch patterns, graphic characters, and control characters for EBCDIC.



Exceptions:

(1)	12-0-9-8-1	(5)	No Punches	(9)	12-0	(13)	0-1
(2)	12-11-9-8-1	(6)	12	(10)	11-0	(14)	11-0-9-1
(3)	11-0-9-8-1	(7)	11	(11)	0-8-2	(15)	12-11
(4)	12-11-0-9-8-1	(8)	12-11-0	(12)	0		

Figure 14A. Extended Binary Coded Decimal Interchange Code

Control Characters

PF	Punch Off	BS	Backspace	PN	Punch On
HT	Horizontal Tab	IL	Idle	RS	Reader Stop
LC	Lower Case	BYP	Bypass	UC	Upper Case
DEL	Delete	LF	Line Feed	EOT	End of Transmission
RES	Restore	EOB	End of Block	SP	Space
NL	New Line	PRE	Prefix		

Special Graphic Characters

¢	Cent Sign	*	Asterisk	>	Greater-than Sign
.	Period, Decimal Point	)	Right Parenthesis	?	Question Mark
<	Less-than Sign	;	Semicolon	:	Colon
(	Left Parenthesis	¬	Logical NOT	#	Number Sign
+	Plus Sign	-	Minus Sign, Hyphen	@	At Sign
|	Vertical Bar, Logical OR	/	Slash	'	Prime, Apostrophe
&	Ampersand	,	Comma	=	Equal Sign
!	Exclamation Point	%	Percent	"	Quotation Mark
$	Dollar Sign	_	Underscore		

Examples	Type	Bit Pattern Bit Positions 01 23 4567	Hole Pattern	
			Zone Punches	Digit Punches
PF	Control Character	00 00 0100	12 -9	4
%	Special Graphic	01 10 1100	0	8 - 4
R	Upper Case	11 01 1001	11	9
a	Lower Case	10 00 0001	12 -0	1
	Control Character, function not yet assigned	00 11 0000	12 - 11 - 0 -9	8 - 1

Figure 14B. Key to Figure 14A.

Auxiliary Storage (AUX or AS)

1. Any storage media (tape, disk, external core storage, etc) not contained within the CPU.

2. An addendum to CPU main storage containing CPU local storage and multiplexor storage.

   Local storage contains the sixteen general-purpose and the four floating-point registers, and certain other areas that cannot be accessed directly by the programmer.

   Multiplexor storage contains unit control words (UCW's) that maintain records of I/O unit operations.

Central Processing Unit (CPU). This unit contains the controls, programs, and storage facilities of the system.

Hexadecimal. A base-sixteen numeric representation using four bits that are arbitrarily assigned values of 8, 4, 2, and 1. All bit combinations are valid.

Binary Value 8421	Hex Value	Binary Value 8421	Hex Value
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

Hexadecimal notation is used both for addressing and arithmetic functions.

Interruption. The interruption system permits the CPU to change state as a result of conditions external to the system (in input/output units) or in the CPU itself.

Local Storage. See Auxiliary Storage.

Manual Light. The System/360 Model 30 manual light is on when the CPU is in the stopped state. Certain manual operations (such as manual display) are permitted only when the CPU is in the stopped state.

Manual State. In the manual (or stopped) state, the manual light is on. Instructions are not executed, and interruptions are not honored.

Mask. A tool used by the programmer either to allow or inhibit certain interruptions.

Microprogram. A sequence of control operations within the CPU.

Multiplexor Storage. See Auxiliary Storage.

Operator's Control Panel (OCP). The operator's control panel section of the system console consists of those controls normally required to run a job. These are: the power-on, power-off, interrupt, and load keys, the load-unit address rotary switches G, H, and J, and the five lights labeled SYS (system), MAN (manual), WAIT, TEST, and LOAD.

Problem Program. Any of the class of routines that perform data processing operations, including routines that solve problems, monitor and control industrial processes, sort and merge records, perform computations, process transactions against stored records, etc.

Problem State. In this state, all privileged instructions are invalid and will cause a program interruption. When the CPU is in the problem state, bit 15 of the PSW is on. Problem/supervisor status is not indicated on the console.

Program Status Word (PSW). The program status word contains the information required for proper program operation.

Read-Only Storage (ROS). This storage medium in the System/360 Model 30 is the control system, and hence contains the microprograms necessary to implement the various functions of the system.

Read/Write Storage. Core storage is used as required in the execution of problem programs. Some areas of read/write storage are reserved (see System/360 Principles of Operation, Form A22-6821, and System/360 Model 30 Functional Characteristics, Form A24-3231).

ROS. See Read-Only Storage

Running State. In the running or operating state, the CPU executes instructions (if not waiting) and interruptions (if not masked off).

Status. System states are defined as: problem/supervisor, wait/running, masked/interruptable, and stopped/operating.

Stopped State. See Manual State.

Supervisor Program. A control routine, which is executed in the supervisor state, that performs the following functions:

Controls input/output operations.

Coordinates system resources.

Maintains the flow of operations through the CPU. Acts in response to requirements for altering or interrupting the flow of operations.

Supervisor State. All instructions are valid. PSW-bit 15 is off.

Tag. Symbols that give information about an I/O operation.

Trap. A change in microprogramming that is automatically initiated by some machine condition.

UCW. See Auxiliary Storage.

Wait State. In the wait state (wait light on), no instructions are processed. Bit 14 of the PSW is on. The CPU clock continues to run, however, and interruptions are executed unless masked off.

IBM S/360 (Mod. 30) Printed in U. S. A. A24-3373-2

IBM®

International Business Machines Corporation
Data Processing Division
112 East Post Road, White Plains, N.Y. 10601
[USA Only]

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
[International]