SY26-3823-1
File No. S370-30

Systems

OS/VS2 I/O Supervisor Logic

VS2 Release 1

IBM

Second Edition (March 1973)

This edition replaces the previous edition (numbered SY26-3823-0) and makes that edition obsolete.

This edition applies to Release 1.6 of OS/VS2 and to all subsequent releases of that system unless otherwise indicated in new editions or technical newsletters.

Significant technical and editorial changes made in this edition are outlined in "Summary of Amendments" following the list of figures. Each technical change is marked by a vertical line to the left of the change.

Information in this publication is subject to significant change. Any such changes will be published in new editions or technical newsletters. Before using the publication, consult the latest *IBM System/360 and System/370 Bibliography*, GA22-6822, and the latest *IBM System/370 Advanced Function Bibliography*, GC20-1763, and the technical newsletters that amend those bibliographies, to learn which editions and technical newsletters are applicable and current.

Requests for copies of IBM publications should be made to the IBM branch office that serves you.

Forms for readers' comments are provided at the back of this publication. If the forms have been removed, comments may be addressed to IBM Corporation, Programming Center—Publishing, Department D58, Monterey and Cottle Roads, San Jose, California 95193. All comments become the property of IBM.

PREFACE

This publication, when used with the program listings, enables you to understand the internal operation of the I/O supervisor and to makes changes to it when necessary.

This publication does not replace the program listings; it supplements them and makes the information in them more accessible. This publication has the following sections:

- "Introduction," which contains information about the I/O supervisor's services and overall operation.
- "Method of Operation," which contains diagrams that describe the operation of the I/O supervisor. The diagrams are high-level and are designed to guide you to a particular area of the program listing.
- "Program Organization." which contains a functional organization chart for each of the main functions of the I/O supervisor, and describes what each routine does.
- "Directories," which contains cross-reference lists that include a data area directory, module directory, and routine directory.
- "Data Areas," which contains descriptions of the interrelationship and content of data areas and control blocks that are used primarily by the I/O supervisor.
- "Diagnostic Aids," which contains information to help you interpret the program listings and diagnose program failures.
- "Appendix A: Supporting SVC Routines," which contains information about supporting SVC routines.
- "Appendix B: Alternate Path Retry," which contains information about the alternate path selective retry option and its relationship to the I/O supervisor.
- "Appendix C: Direct-Access Volume Verification," which contains information about the direct-access volume verification option and its relationship to the I/O supervisor.
- "Appendix D: Dynamic Device Reconfiguration," which contains information about the dynamic device reconfiguration option and its relationship to the I/O supervisor.
- "Appendix E: Program Check Recovery Subroutine," which contains information about the program check recovery subroutine.
- "Appendix F: Shared Direct-Access Storage Device," which contains information about the shared direct-access storage device option and its relationship to the I/O supervisor.
- "Appendix G: I/O Supervisor—OLTEP Synchronizing Module (IECIOCTS)," which contains the requirements of the Online Test Executive Program for the I/O supervisor.
- "Appendix H: Device-Dependent Error Routines," which describes device-dependent error routines and contains information about writing error recovery messages to the operator.
- "Glossary of Terms, Acronyms, and Abbreviations," which contains definitions of terms used in this publication along with the meanings of the acronyms and abbreviations used.

How to Use This Publication

Before using this publication, read the "Introduction" to establish perspective, and then at least scan the remainder of the publication to familiarize yourself with its content. This publication is primarily a reference manual because each section contains a specific type of information. You will be better able to service the program when you can refer quickly to the section containing the type of information you need.

The "Method of Operation" section contains diagrams, each consisting of two pages. The first page (left or upper) is the actual diagram. The second page (right or lower) consists of expanded text and references to other diagrams and flowcharts. The diagrams are at a high level; therefore, some of the I/O supervisor functions are not shown. The routine directory (see "Directories" can be used to find entry points into the routines that are not included in the diagrams.

Referenced System and Data Management Publications

The following publications (listed in order-number order) are referenced throughout this publication:

- *OS/VS Recovery Management Logic,* GC27-7239
- *OS/VS2 Planning and Use Guide,* GC28-0600
- *OS/VS Data Management for System Programmers,* GC28-0631
- *OS/VS2 Debugging Guide,* GC28-0632
- *OS/VS Service Aids,* GC28-0633
- *OS/VS Utilities,* GC35-0005
- *OS/VS Message Library: VS2 System Messages,* GC38-1002
- *OS/VS Message Library: VS2 System Codes,* GC38-1008
- *OS/VS2 Supervisor Logic,* SY27-7244
- *OS/VS2 System Data Areas,* SY28-0606
- *OS/VS OLTEP Logic,* SY28-0637
- *OS/VS SYS1.LOGREC Error Recording Logic,* SY28-0639

Other OS/VS publications are listed in the *IBM System/360 and System/370 Bibliography,* GA22-6822.

CONTENTS

Page

Page

FIGURES

Page

Page

SUMMARY OF AMENDMENTS

Release 1.6

CCW Translation Header BEBLK

The CCW translation header block has been deleted and a new data area, the CCW translation header BEBLK, has been added. The CCW translation header BEBLK combines the functions of the old data areas, the CCW translation header block and the BEBLK. (Note that the addresses of the real CCWs have been deleted from the BEBLK.) If the channel program requires a second BEBLK (other than the header BEBLK), the format of the BEBLK will be the same as that described in the "Data Areas" section under BEBLK (Beginning-End Block).

The TSTHDR field of the RQE now points to the page fix list before translation, and to the CCW translation header BEBLK during and after translation.

IOS Support of the IBM 3333 Disk Storage and Control

IOS now fully supports the IBM 3333 Disk Storage and Control. The 3333 is functionally equivalent to the 3330 Disk Storage. All references to the 3330 also apply to the 3333.

INTRODUCTION

Following execution of the statements or instructions written by programmers to cause I/O activity, a sequence of events begins in which the I/O supervisor plays a major role. This section defines that role and describes the environment in which it is performed.

An I/O operation can be described as the sequence of events beginning with the execution of the statement or instruction a programmer writes to cause data to be written on or read from an I/O device, and ending when all related activity is completed. Although the I/O supervisor plays a major role in an I/O operation, it is not the only control program element involved. This section establishes the scope and objectives of the I/O supervisor.

The User and the I/O Supervisor

Three methods a programmer can use to request an I/O operation are shown in Figure 1. The actions taken by the I/O supervisor in satisfying the request are shown below the horizontal line that divides the figure. Specific input data must always be provided to the I/O supervisor, but the extent to which the programmer must define that input data depends upon how he requests the I/O operation.

The user of a higher-level language (PL/I, for example) describes files and writes OPEN and GET statements. When his program is executed, one PL/I subroutine uses a DCB macro instruction to build a data control block (DCB), and an OPEN macro instruction to cause data management routines to build a channel program, and input/output block (IOB), a data extent block (DEB), and an event control block (ECB). Another PL/I subroutine uses a GET macro instruction, and a data management routine executes an EXCP macro instruction that causes entry to the I/O supervisor.

Adjacent to the steps taken by a programmer who uses a higher-level language are shown the steps a programmer must take when he is using an assembler language and chooses to use an access method. With an access method, a programmer must essentially do what the PL/I compiler did; that is, he must himself write all needed DCB, OPEN, and GET macro instructions.

The user of an EXCP macro instruction must provide directly all of the input that is required by the I/O supervisor. He may use the DCB and OPEN macro instructions, and he may use the I/O appendages—user-written routines that receive control at appropriate exits in the I/O supervisor code—but he must write his own channel program, and he must build his own IOB and ECB. To request any kind of I/O activity, he must use the EXCP macro instruction.

The EXCP user has the option, at OPEN time, to specify the use of I/O appendages during the progress of I/O operations associated with his data set. These appendages gain control at specific points in the I/O supervisor. They gain control:

- During page fixing
- During extent checking, if an out-of-extent condition is detected
- Prior to issuing the SIO instruction
- If a PCI interruption is received
- If a normal channel end interruption is detected
- If any abnormal condition is detected with a primary interruption

I/O appendages give the EXCP user a means of extending and altering I/O operations. For further information about I/O appendages, see *OS/VS Data Management for System Programmers.*

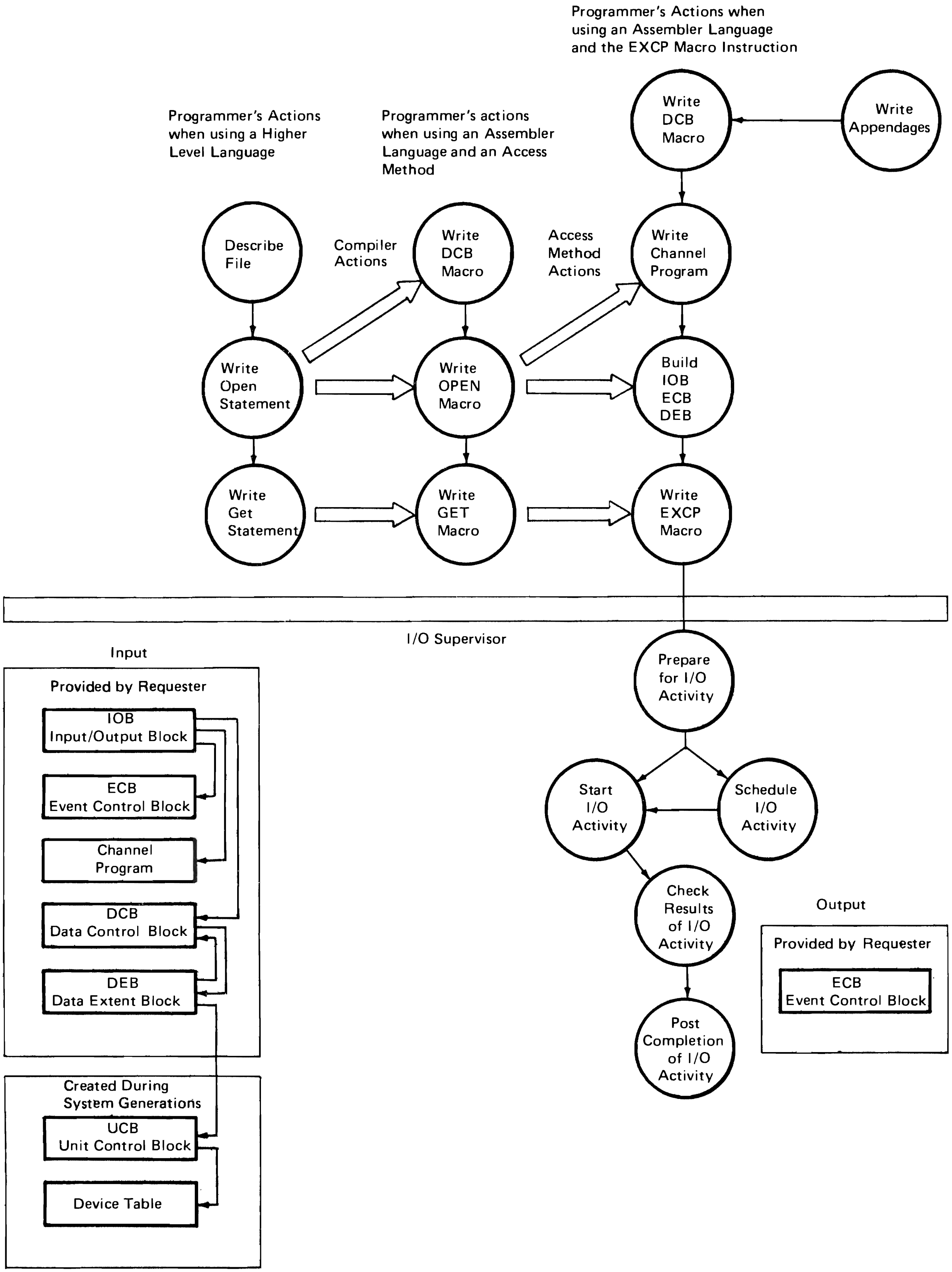


Figure 1. The User and the I/O Supervisor

Note from Figure 1 how a higher-level language compiler uses access method routines, and note also the similarity between what access method routines do and what a programmer must do when he uses the EXCP macro instruction.

The Page Supervisor and VS Subsystems

The page supervisor and VS subsystems uses the EXCPVR macro instruction to request I/O services from the I/O supervisor. (The EXCPVR macro instruction is not available to other users of the I/O supervisor.) The EXCPVR macro instruction generates a calling sequence to the I/O supervisor that creates linkages and issues an SVC 114. The basic difference between an SVC 114 request and SVC 0 request is that an SVC 114 request needs little or no translation service and thus can be processed faster than an SVC 0 request.

VS subsystems prepare channel programs (CCW chains) in fixed virtual address space using real data addresses. Subsystems also fix pages for their own control blocks, I/O appendages, and data areas.

Consequently, the I/O supervisor does not fix pages for subsystems'control blocks, I/O appendages, channel programs, or data areas, and does not translate the CCW data addresses to real addresses. However, the I/O supervisor does translate the CCW start address to *real* at EXCPVR time, and also translates the address of the last CCW+8 in the CSW to *virtual* when an I/O interruption occurs.

The page supervisor prepares CCWs and control blocks in nonpageable storage, so page fixing or address translation operations are not performed by the I/O supervisor.

The I/O Supervisor and the Control Program

Many control program elements are involved in I/O operations besides the I/O supervisor. Their functions are supporting functions needed to coordinate the actions of the I/O supervisor with other system actions. The general system environment of the I/O supervisor is shown in Figure 1.

When an EXCP macro instruction is encountered during assembly of a processing program, the assembler obtains the corresponding macro expansion from the SYS1.MACLIB data set and inserts it into the object program. The last instruction in the EXCP macro expansion is an SVC 0 instruction.

During execution of the processing program, the SVC 0 instruction causes an SVC interruption and immediate entry to the supervisor's SVC first level interruption handler (SVC FLIH). The SVC FLIH is always given control after SVC interruptions. It refers to a list of SVC numbers (called an SVC table) to determine 1) what SVC routine is to service the request and 2) whether or not the needed SVC routine is of the type that is contained in *real* storage. In the case of SVC 0, the routine to be given control is always the first of the two major I/O supervisor routines; the EXCP supervisor and the I/O interruption supervisor.

In giving control to the EXCP supervisor, the SVC FLIH passes the address of the input/output block (IOB), the key item of input data, to the I/O supervisor, and identifies the requester type. See Figure 2 for the characteristics of I/O requesters.

Because channels cannot translate virtual storage addresses, IOS tranlates any virtual addresses used in the channel program. Figure 3 shows the interface between the I/O supervisor and control program.

IOS also ensures that the pages pertaining to the requested I/O operation are fixed in real storage. For virtual requesters, IOS passes control to the page supervisor to fix pages for:

Type of Requester	CCW Chain Location	CCW Translation Requirements	Page Fixing Requirements	SVC Generated
Virtual	Pageable storage	IOS must translate CCW chains.	Control blocks and appendages must be fixed.	EXCP macro generates an SVC 0.
Fixed (VS subsystems only)	Pageable storage	CCW chains have been translated by the requester.	Control blocks and appendages have been fixed by the requester.	EXCPVR macro generates an SVC 114.
Nonpageable	Nonpageable Storage	None	None	EXCP macro generates an SVC 0.
Page Supervisor	Nonpageable Storage	None	None	EXCPVR macro generates an SVC 114.

Figure 2. Characteristics of I/O Requesters

- I/O areas specified in the channel program
- Control blocks (IOB, DCB, DEB, ECB/DECB and AVT)
- I/O appendages

Using input data it obtains from addresses in the IOB, the EXCP supervisor either starts the I/O device or, if the needed device is unavailable, schedules the I/O request by placing an element representing the request into a queue.

For virtual requesters, starting the I/O device involves building a real channel program equivalent to the requester's virtual channel program and then having the channel begin executing the real channel program. The real channel program is built in the system queue area (SQA) of real storage.

The EXCP supervisor then gives control to the supervisor's type 1 Exit routine. All type 1 SVC routines (except those abnormally terminated) pass control to the type 1 Exit routine.

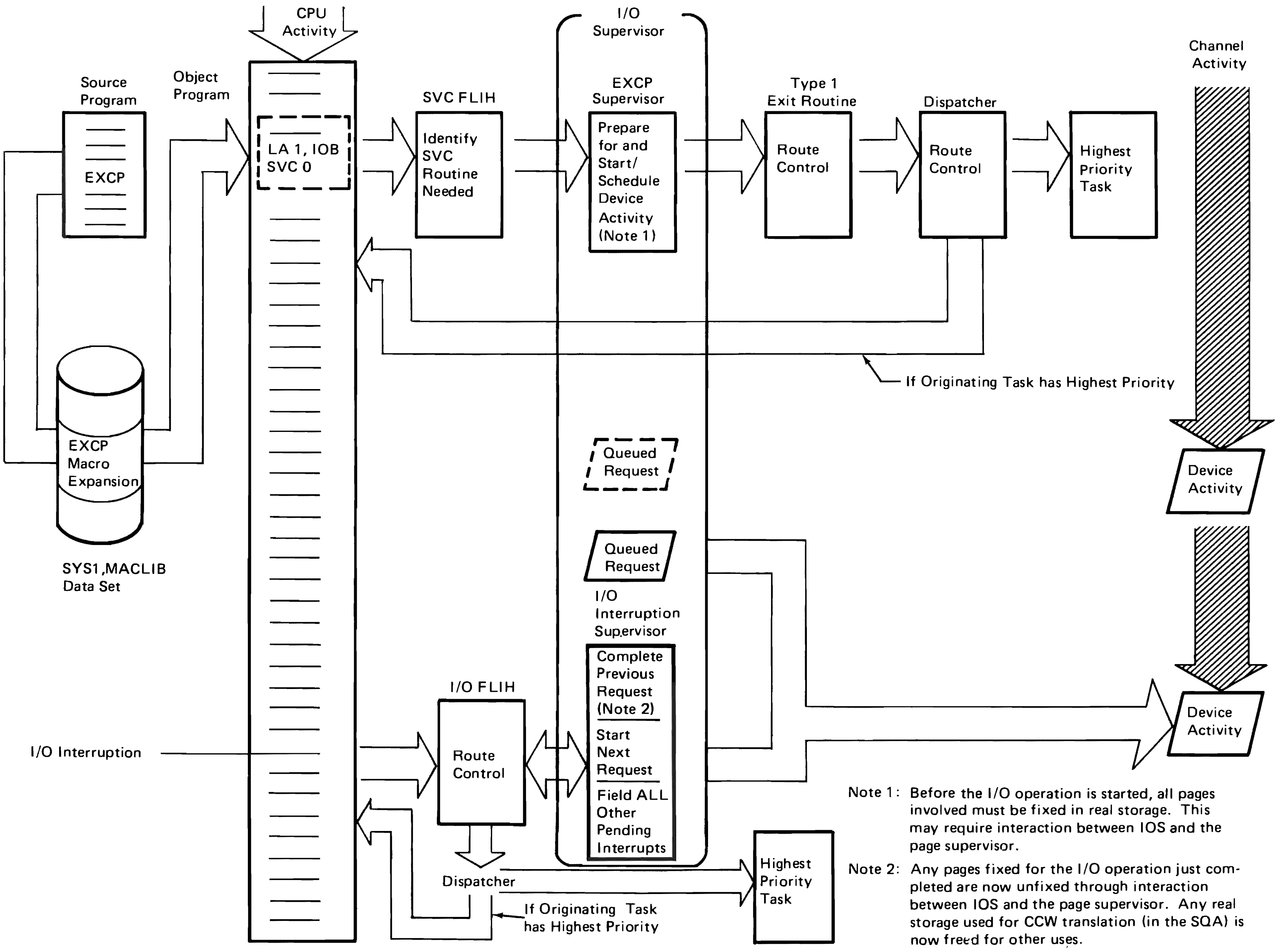
If the routine in which the request for the I/O operation was made is still the highest-priority task in the system, the type 1 Exit routine restores the environment that existed at the time of the interruption and returns control to the dispatcher routine. The dispatcher routine either returns control to the requesting routine or to a routine of a new task with a higher priority.

The next event occurs asynchronously. When the device has completed its part of the I/O operation, it causes an I/O interruption. Following I/O interruptions, control is given to the supervisor's I/O first-level interruption handler (I/O FLIH). The I/O FLIH saves a record of the interrupted environment and gives control to the second of the two major I/O supervisor routines, the I/O interruption supervisor.

For virtual and fixed requesters, the I/O interruption supervisor must retranslate the address of the "last CCW+8" in the CSW to the corresponding virtual address; it must also interface with the page supervisor to unfix any pages that were fixed specifically for the I/O operation just completed. In addition, it now frees the real storage area used for translating the CCWs of virtual requesters.

The I/O interruption supervisor signals the requester that the I/O operation is completed (the task supervisor's post routine posts the requester's event control block), and starts other devices on the channel in response to any requests that were queued while the device, data set, or channel was busy with the request just completed.

While the I/O interruption handler processes on interruption, one or more other interruptions may occur. Because I/O interruptions are disabled, they are stacked (saved



Note 1: Before the I/O operation is started, all pages involved must be fixed in real storage. This may require interaction between IOS and the page supervisor.

Note 2: Any pages fixed for the I/O operation just completed are now unfixed through interaction between IOS and the page supervisor. Any real storage used for CCW translation (in the SQA) is now freed for other uses.

Figure 3. The I/O Supervisor and the Control Program

by the hardware), thus creating a pending interruption. After an interruption is processed and the user is posted, the I/O supervisor enables the system for the I/O interruptions. At this time, one of the stacked interruptions is fielded and processed. This process continues until all pending interruptions have been fielded and all queued I/O requests that can be started have been started. The I/O supervisor enables the system for I/O interruptions one last time to check whether there are any more interruptions to be processed. If there are none, the I/O supervisor exits to the I/O FLIH.

When the I/O interruption supervisor returns control to the I/O FLIH, control via the dispatcher, is routed either to the requesting routine or to a routine of a higher-priority task.

The I/O Supervisor

The overall objective of the I/O supervisor is to make sure that a requested I/O operation is performed. To achieve its objective, the I/O supervisor performs three major functions: starting I/O operations, terminating I/O operations, and restarting I/O operations (for error-correction purposes). These functions, the two major I/O supervisor routines, and the general control flow to and from the routines, are shown in Figure 4.

Note: The EXCP supervisor and error EXCP supervisor share most of the same routines. However, since their functions are separate and distinct, they are treated separately throughout this manual.

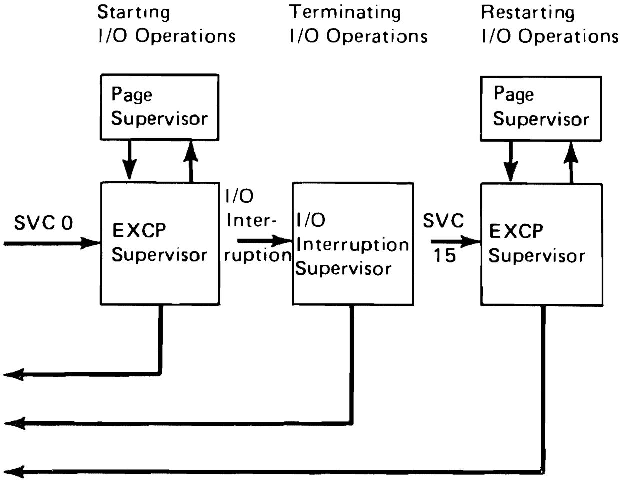


Figure 4. I/O Supervision

The basic control flow to and from the EXCP supervisor and the I/O interruption supervisor has already been shown in Figure 1. However, for restarting I/O operations, an SVC 15 instruction (rather than an SVC 0 instruction) causes entry to the EXCP supervisor for retry of an error condition.

In Figure 5 the major functions are expressed in more detail. The three coordinative functions have been added: scheduling I/O operations, starting scheduled I/O operations, and scheduling restarts of I/O operations.

The first flow diagram in Figure 5 shows the flow for a straightforward I/O operation where the Start I/O instruction is accepted and there is no need to schedule I/O device activity. This flow is shown separately to illustrate how the request queue is checked following completion of every I/O operation. The queue is checked repeatedly until no pending requests remain. If after terminating an I/O operation, the status indicators

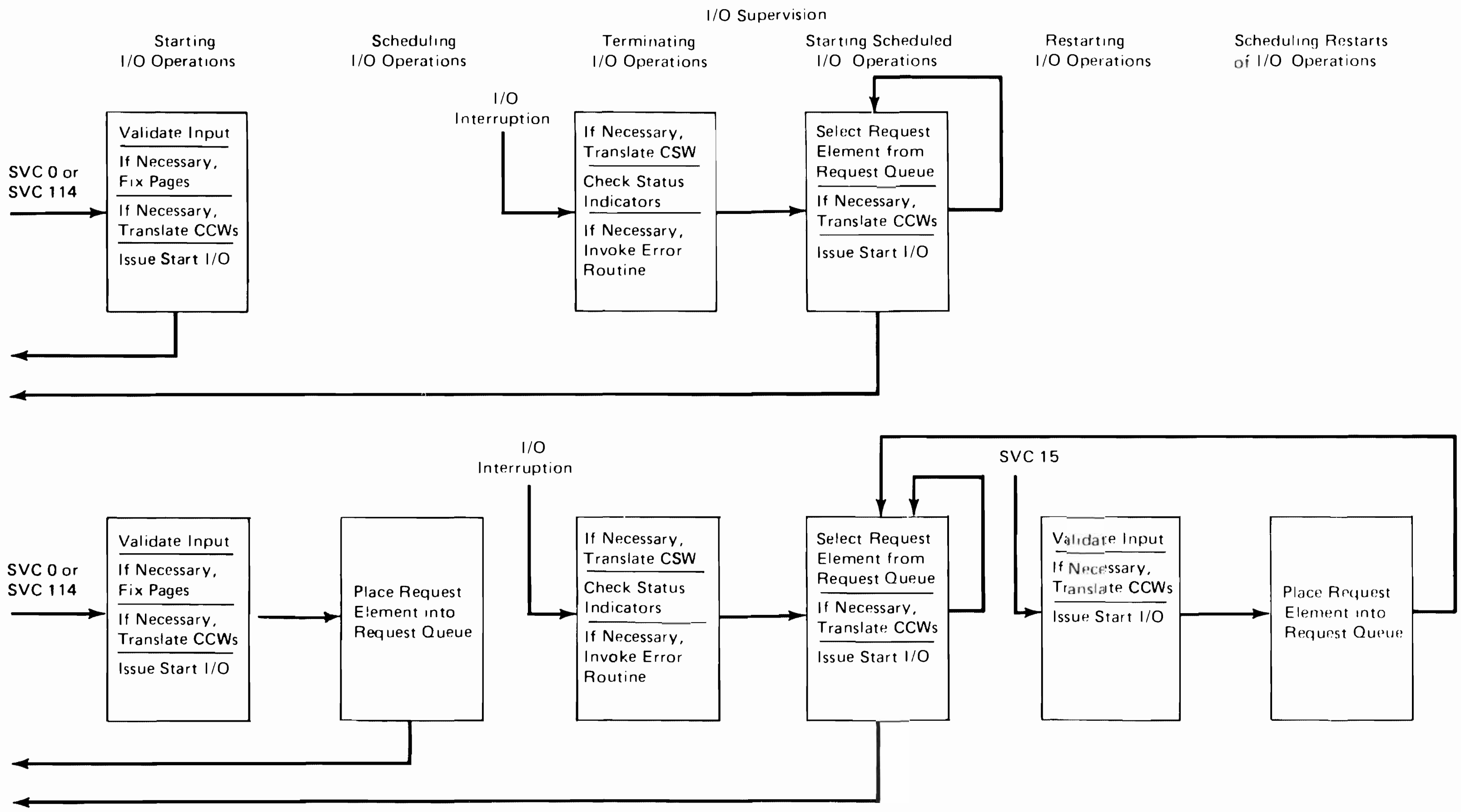

I/O Supervision
Starting I/O Operations
Scheduling I/O Operations
Terminating I/O Operations
Starting Scheduled I/O Operations
Restarting I/O Operations
Scheduling Restarts of I/O Operations
SVC 0 or SVC 114
Validate Input
If Necessary, Fix Pages
If Necessary, Translate CCWs
Issue Start I/O
I/O Interruption
If Necessary, Translate CSW
Check Status Indicators
If Necessary, Invoke Error Routine
Select Request Element from Request Queue
If Necessary, Translate CCWs
Issue Start I/O
SVC 0 or SVC 114
Validate Input
If Necessary, Fix Pages
If Necessary, Translate CCWs
Issue Start I/O
Place Request Element into Request Queue
I/O Interruption
If Necessary, Translate CSW
Check Status Indicators
If Necessary, Invoke Error Routine
Select Request Element from Request Queue
If Necessary, Translate CCWs
Issue Start I/O
SVC 15
Validate Input
If Necessary, Translate CCWs
Issue Start I/O
Place Request Element into Request Queue

Figure 5. I/O Supervisor Functions

show an error condition to exist, the I/O interruption supervisor invokes a user-written or IBM-supplied error correction routine. Error routines can request a retry by issuing an SVC 15 instruction, which will result in entry to the error EXCP supervisor for the retry.

The second flow diagram in Figure 5 shows the flow for an I/O operation that could not be started immediately. Note that the request queue is examined after a restart of the I/O operation is scheduled, just as it is when an I/O operation is terminated.

Concept of Logical Channels

The queues into which request elements are placed when I/O activity cannot be started immediately do not always correspond one-for-one with the physical channels attached to a system. Rather, they correspond to logical channels. A logical channel is the set of all physical channels by which a device can be reached.

Queuing in logical queues makes possible path-device groups in which a common set of paths can be tried for each device of a group. The result is simplified alternate-path logic.

Unless a switching device or a two-channel switch is installed, providing multiple-path capability, every physical channel is also a logical channel and there is a one-for-one correspondence. With switching devices, however, the relationship between physical and logical channels varies, depending upon both the number of switches and their placement.

A system without two-channel switches is shown symbolically at the top of Figure 6. Because each device can only be reached via one path, each physical channel is also a logical channel.

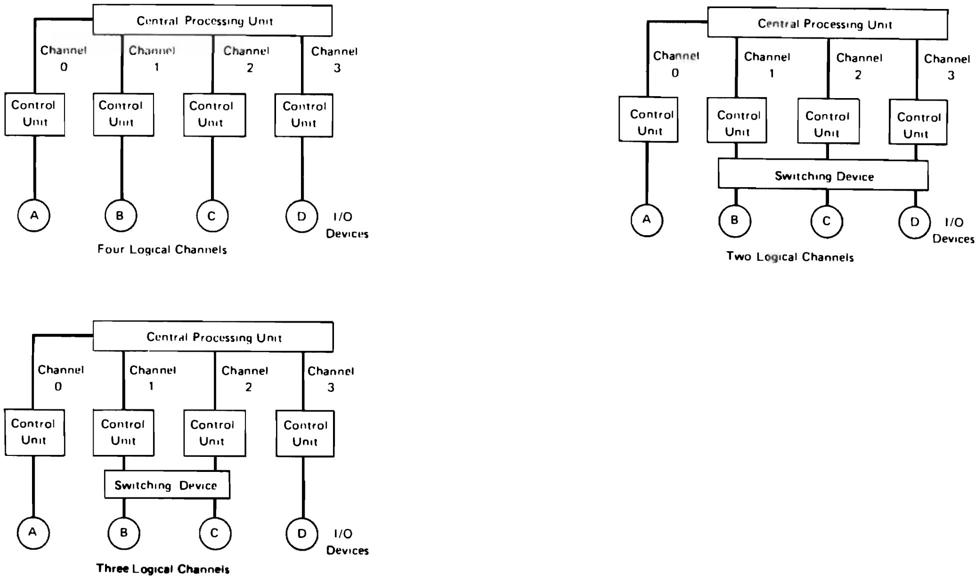


Figure 6. Logical Channel—Physical Channel Relationships

Also shown in Figure 6 is a system in which a switching device connects two control units. Devices B and C can then be reached via channel 1 or channel 2. Devices B and C are both in the logical channel comprising physical channels 1 and 2.

Another configuration with a switching device is shown at the right in Figure 6. This time, devices B, C, and D may be reached via channels 1, 2, and 3; devices B, C, and D are all in the same logical channel.

Except for the 2870 Multiplexor Channel, all devices attached via the same multiplexor channel will always be in the same logical channel. The devices attached via a 2870 Multiplexor Channel may be contained in more than one logical channel, however, because each of the four optional selector subchannels is considered separately.

METHOD OF OPERATION

This section contains diagrams that are designed to give you a general knowledge of the I/O supervisor's operation and to guide you through the program listing. To do this effectively, the diagrams must be kept at a high level. Therefore, there are some functions of the I/O supervisor that are not shown. Use the I/O supervisor routine directory (Figure 27) to find entry points into the listing for routines that are not included in this section.

Each diagram consists of two pages. The (upper) first is the actual diagram. The second (lower) page consists of expanded text, references to other diagrams, and flowcharts, and a program organization chart that highlights a particular function of the I/O supervisor.

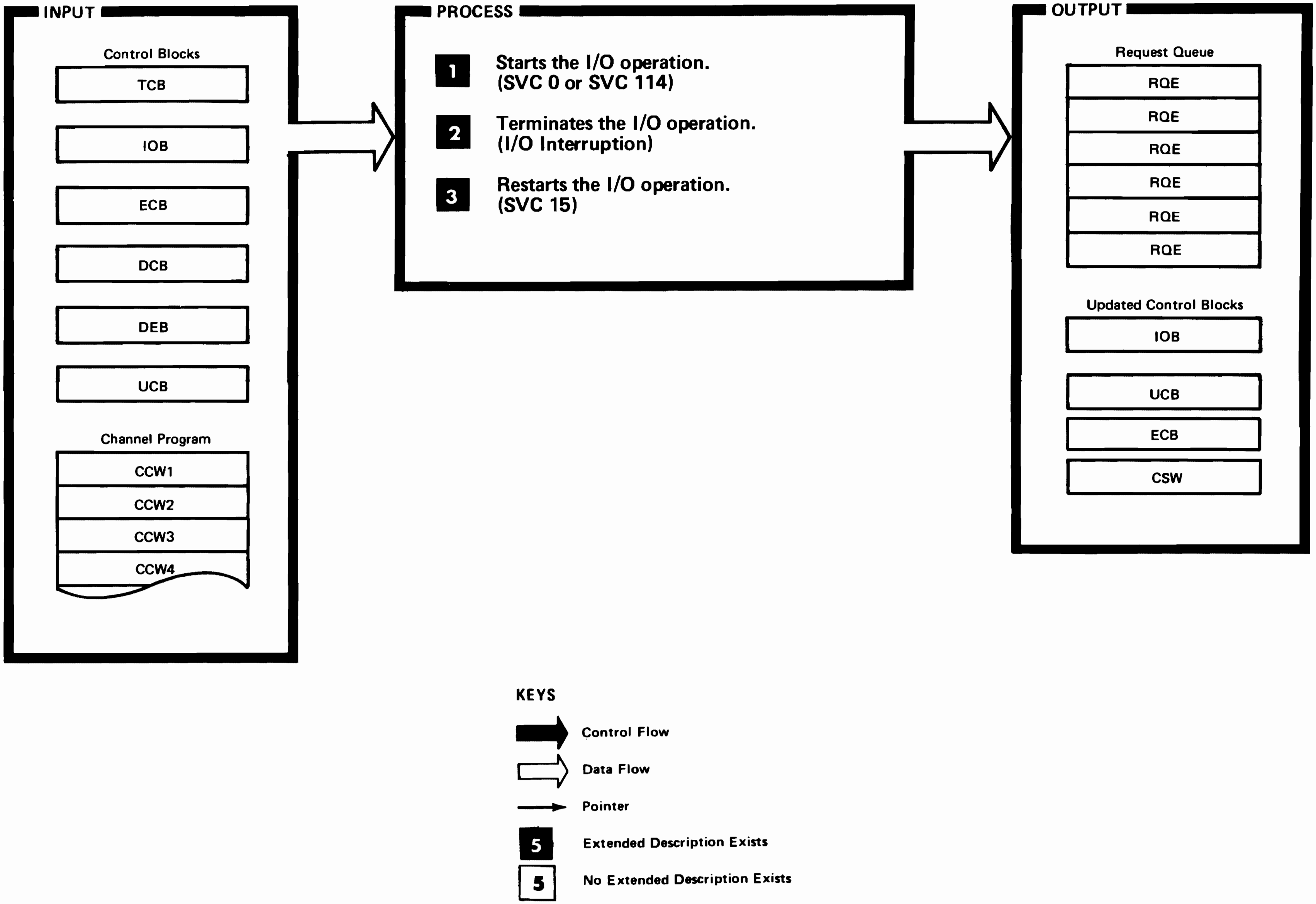

INPUT
Control Blocks
TCB
IOB
ECB
DCB
DEB
UCB
Channel Program
CCW1
CCW2
CCW3
CCW4
PROCESS
1 Starts the I/O operation. (SVC 0 or SVC 114)
2 Terminates the I/O operation. (I/O Interruption)
3 Restarts the I/O operation. (SVC 15)
OUTPUT
Request Queue
RQE
RQE
RQE
RQE
RQE
RQE
Updated Control Blocks
IOB
UCB
ECB
CSW
KEYS
Control Flow
Data Flow
Pointer
5 Extended Description Exists
5 No Extended Description Exists

Figure 7. (Part 1 of 2) I/O Supervisor

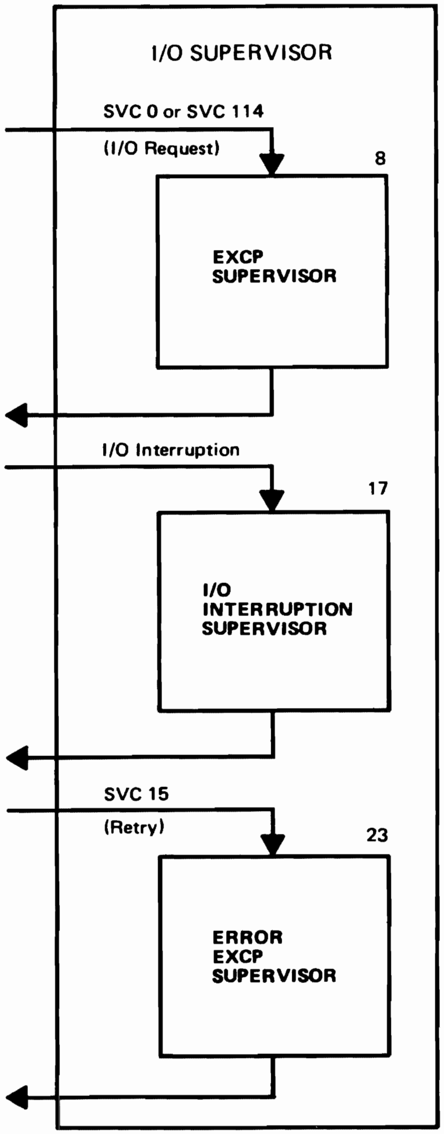
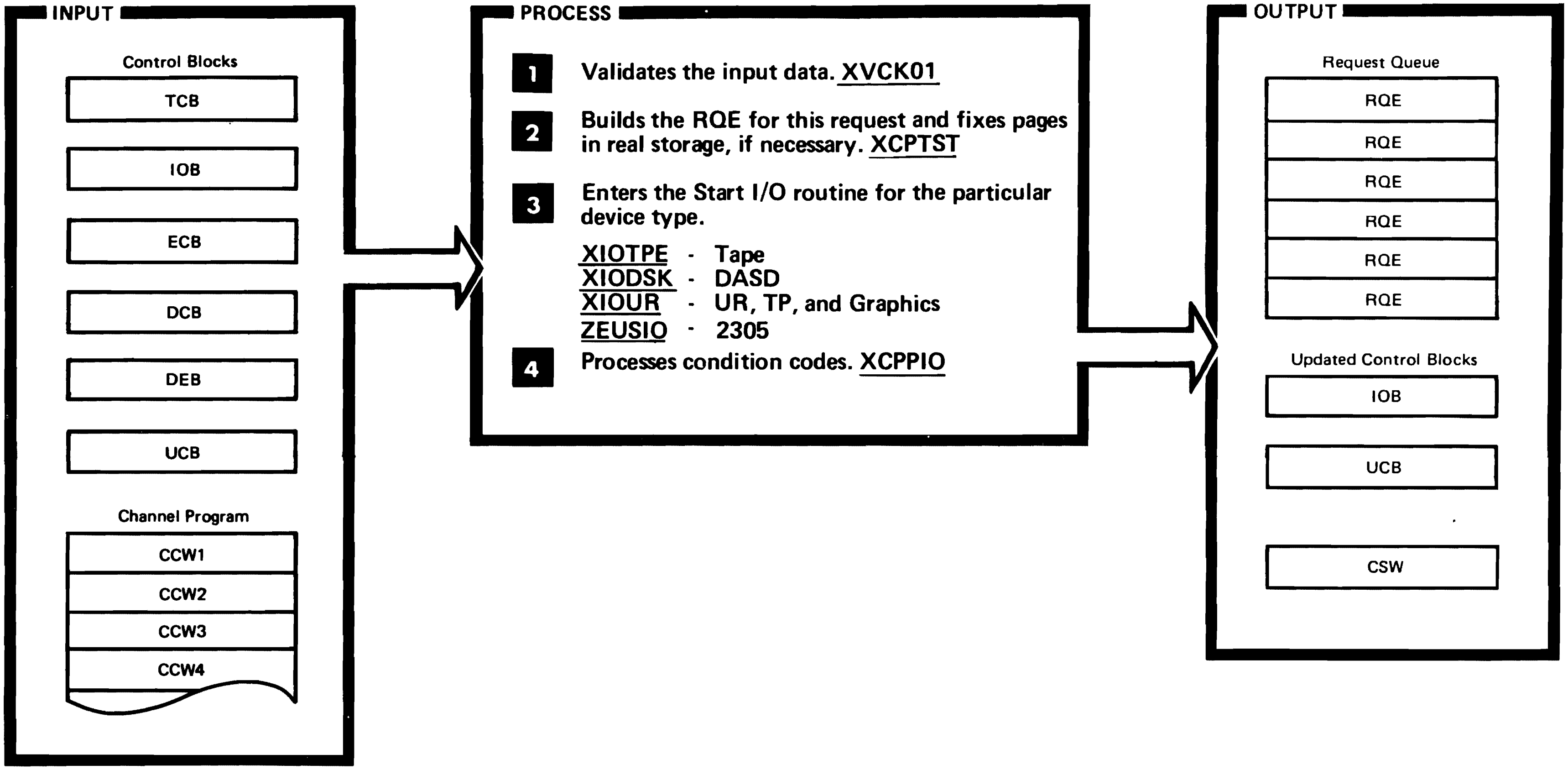


Figure 7. (Part 2 of 2) I/O Supervisor

	Extended Description	Figure
1	An SVC 0 or SVC 114 initiates an I/O operation. This causes entry into the EXCP supervisor where: ● Input data is validated. ● An RQE is initialized for the request. ● Associated pages are fixed in real storage. ● The channel program is translated (SVC 0). ● The Start I/O instruction is issued. ● The resulting condition codes are checked.	8
2	When an I/O interruption occurs, the I/O Interruption Supervisor is entered. If the I/O operation terminated successfully, its RQE is returned to the freelist and another interruption is processed. If there are no other interruptions pending, another device can be started on the channel. If the I/O operation results in an error condition, the error recovery routine is executed.	17
3	The Error EXCP Supervisor is entered from the error recovery routine. The requestor's control blocks are validated, and the I/O operation is either retried or terminated.	23



1 Validates the input data. XVCK01

2 Builds the RQE for this request and fixes pages in real storage, if necessary. XCPTST

3 Enters the Start I/O routine for the particular device type.

XIOTPE - Tape
XIODSK - DASD
XIOUR - UR, TP, and Graphics
ZEUSIO - 2305

4 Processes condition codes. XCPPIO

Figure 8. (Part 1 of 2) EXCP Supervisor

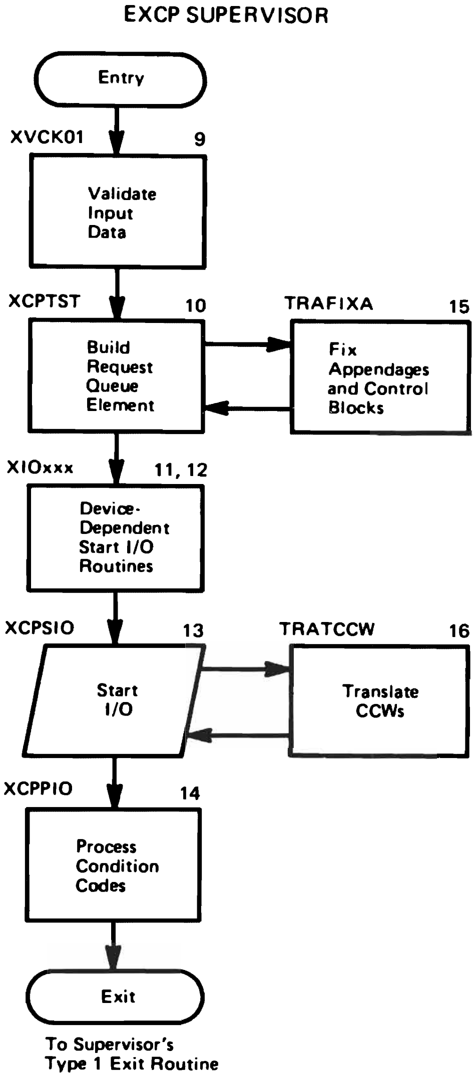


Figure 8. (Part 2 of 2) EXCP Supervisor

	Extended Description	Figure
1	Various fields within the control blocks are checked to prevent vital system data from being destroyed.	9
2	An RQE is built for each I/O request. If the request cannot be immediately satisfied, the RQE is placed in the logical channel request queue for that device. For virtual and fixed requestors, the pages involved in the requested I/O operation are fixed in real storage. This prevents the pages from being moved into auxiliary storage through normal paging operations.	10
3	The Start I/O module builds any device-dependent prefix CCW chains needed. The SIO subroutine is entered to translate the virtual channel program and execute the SIO instruction.	11, 12
4	The Post Start I/O routine processes the condition codes that resulted from the Start I/O and translates the CCW address in the CSW back to virtual. The IOB and UCB are updated and the RQE is dequeued before exiting to the supervisor's Type 1 exit routine.	14

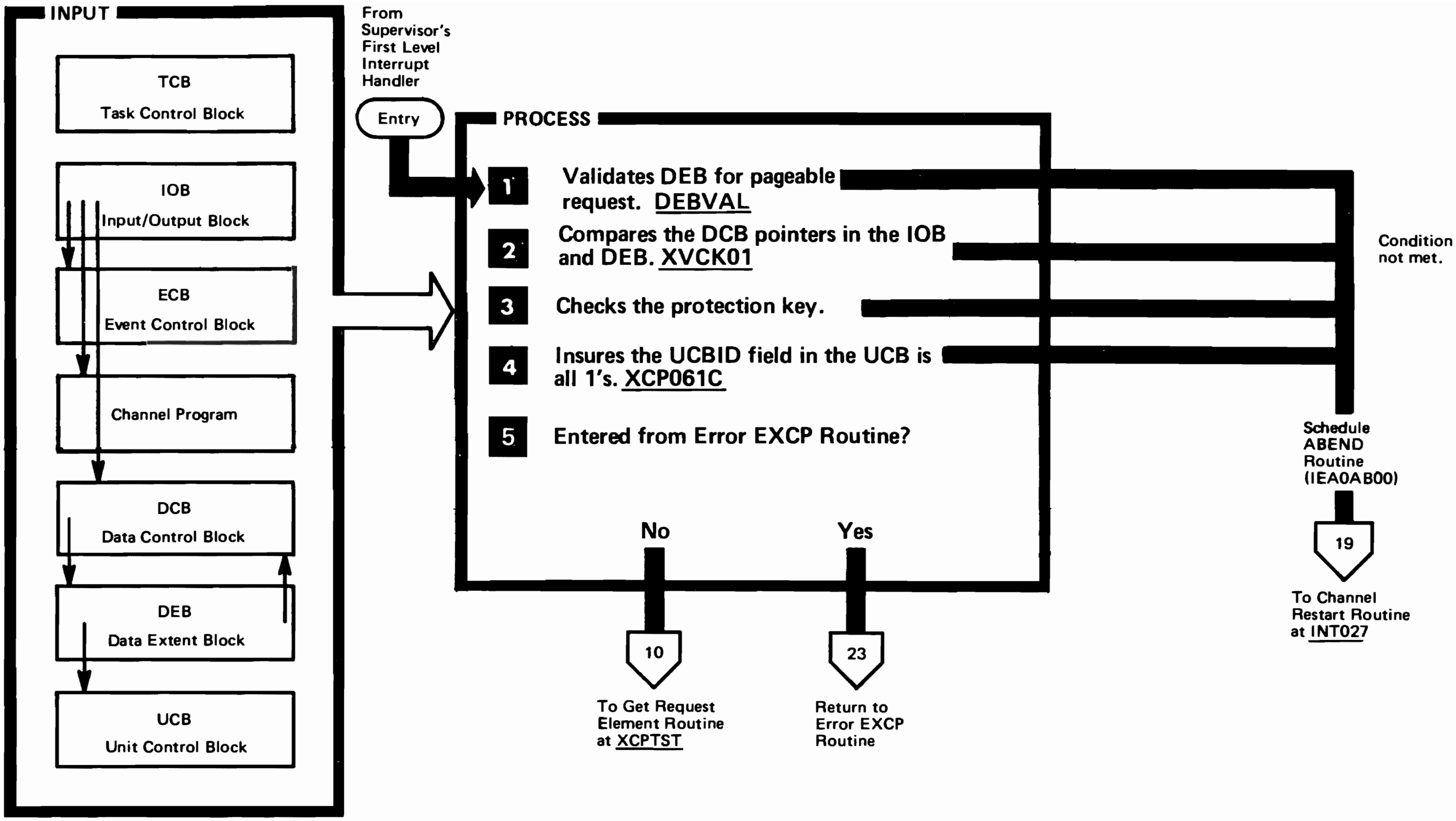
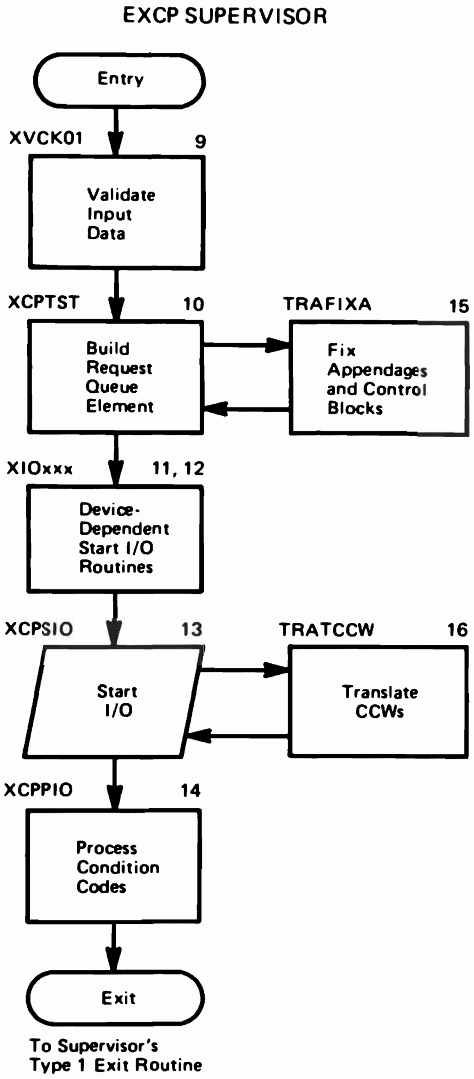
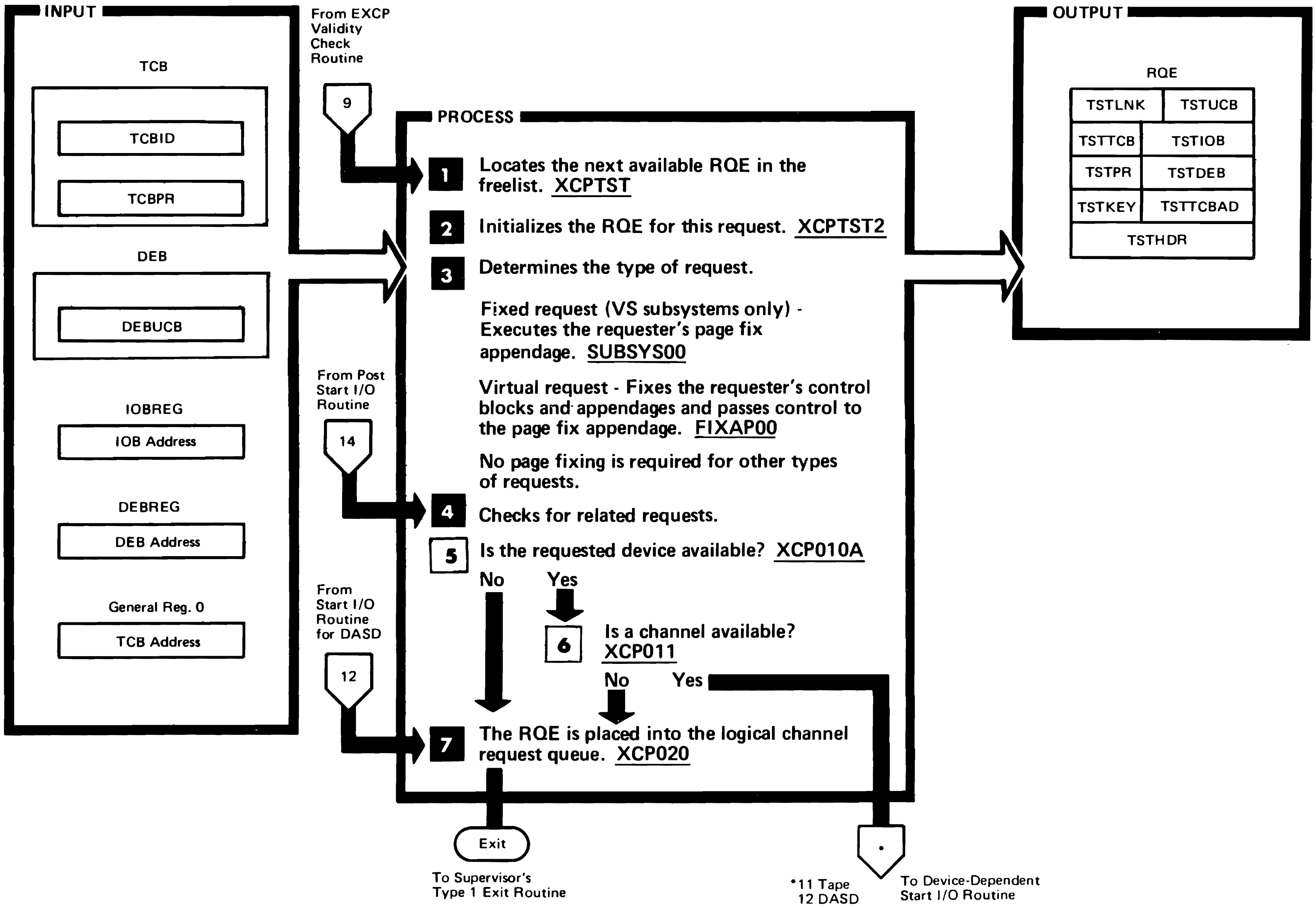

INPUT
TCB
Task Control Block
IOB
Input/Output Block
ECB
Event Control Block
Channel Program
DCB
Data Control Block
DEB
Data Extent Block
UCB
Unit Control Block
From Supervisor's First Level Interrupt Handler
Entry
PROCESS
1 Validates DEB for pageable request. DEBVAL
2 Compares the DCB pointers in the IOB and DEB. XVCK01
3 Checks the protection key.
4 Insures the UCBID field in the UCB is all 1's. XCP061C
5 Entered from Error EXCP Routine?
No
Yes
10
To Get Request Element Routine at XCPTST
23
Return to Error EXCP Routine
Condition not met.
Schedule ABEND Routine (IEA0AB00)
19
To Channel Restart Routine at INT027

Figure 9. (Part 1 of 2) Validity Check Routine



	Extended Description	Figure
1	The DEB Validity Check module, IFGDEBVR, for pageable request is entered to ensure that the DEB passed to IOS is on the DEB chain. If not, the ABEND routine is entered; otherwise, the routine goes to step 4.	
2	The IOB's pointer to the DCB must be the same as the DEB's pointer to the DCB. If not, the ABEND routine is entered.	
3	If the system has the protection feature, a non-supervisor requester's key must equal the storage key in the DEB. The ABEND routine is entered if the keys do not match.	
4	The UCB is invalid if the UCBID field is not all 1's.	
5	If this routine is entered from the supervisor's SVC First Level Interruption Handler, the Get Request Element routine is entered to build an RQE for this request.	10
	If this routine is entered from the Error EXCP routine, the address of the logical channel word is calculated and placed in a register. The Error EXCP routine is then reentered.	23

Figure 9. (Part 2 of 2) Validity Check Routine



1 Locates the next available RQE in the freelist. XCPTST

2 Initializes the RQE for this request. XCPTST2

3 Determines the type of request.

Fixed request (VS subsystems only) - Executes the requester's page fix appendage. SUBSYS00

Virtual request - Fixes the requester's control blocks and appendages and passes control to the page fix appendage. FIXAP00

No page fixing is required for other types of requests.

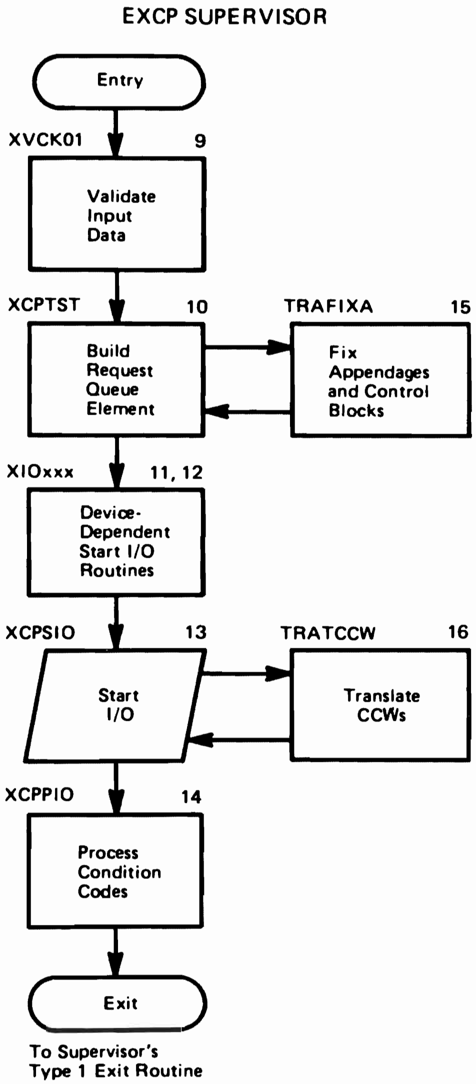
4 Checks for related requests.

5 Is the requested device available? XCP010A

6 Is a channel available? XCP011

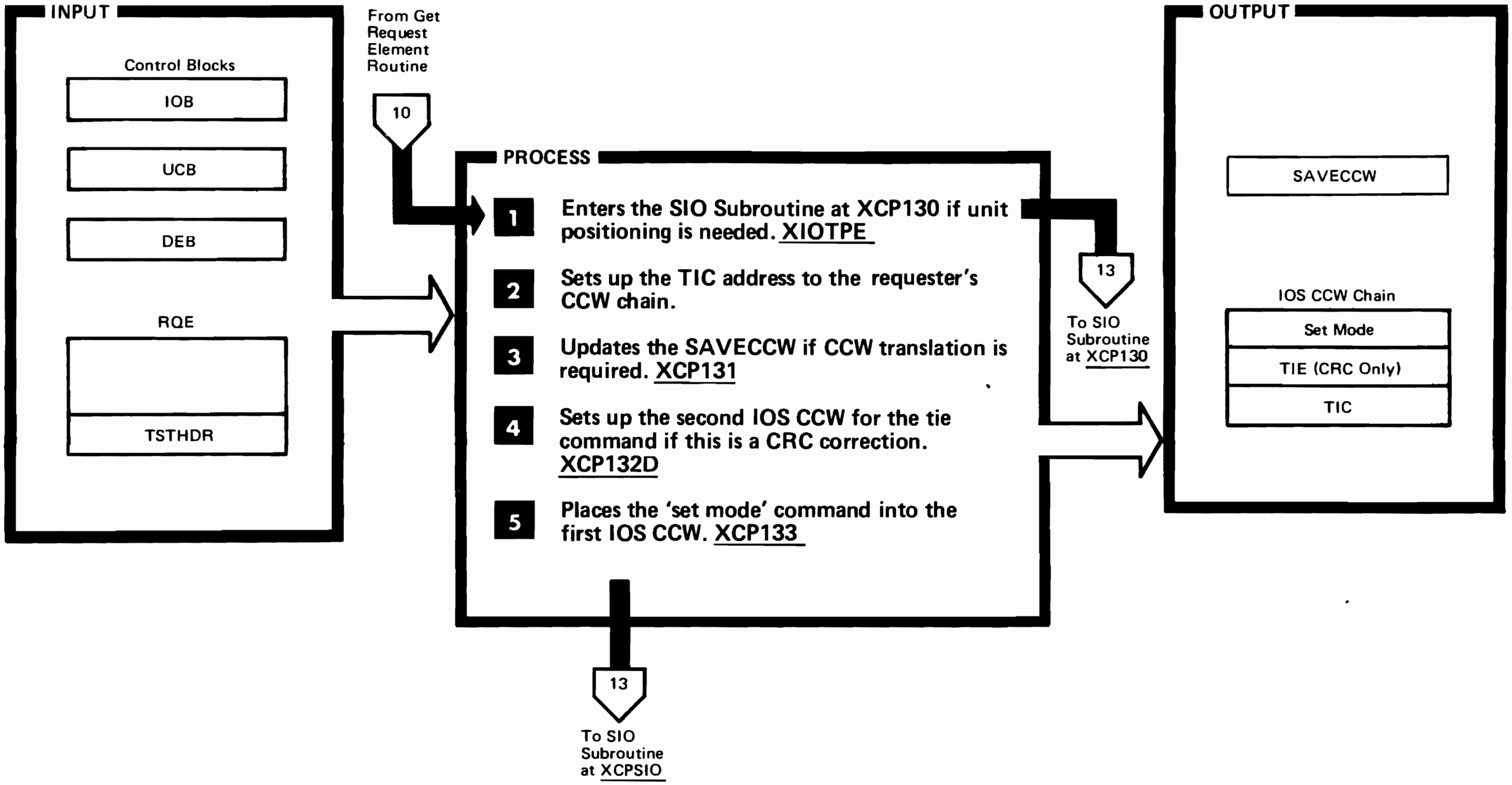
7 The RQE is placed into the logical channel request queue. XCP020

Figure 10. (Part 1 of 2) Get Request Element Routine



	Extended Description	Figure
1	The NEXAVL pointer points to the next available RQE in the freelist. The TSTLNK field of the removed RQE becomes the new pointer.	
2	The RQE for a particular request is initialized with pointers obtained from various control blocks and registers. Until this time, the only valid RQE field was the TSTLNK field.	
3	The type of request is indicated in the high-order byte of the TSTHDR field. For subsystem (SVC 114) requests, the pages to be fixed are specified in the requester's page fix appendage. The Page Supervisor is then entered to fix the pages. For virtual requests, the Page Fix Routine is executed to fix control blocks and appendages.	15
4	If a previous related request has not yet completed, the RQE is placed into the logical channel queue. If a previous related request resulted in a permanent error or intercept condition, its RQE is removed from the logical channel queue and the Abnormal End appendage is entered.	
7	The RQE is queued by one of three methods: ● FIFO - First In/First Out. ● Priority - In order of the requesting task's priority. ● Ordered Seek - In order of the cylinder address of the requested DASD.	

Figure 10. (Part 2 of 2) Get Request Element Routine



1 Enters the SIO Subroutine at XCP130 if unit positioning is needed. XIOTPE

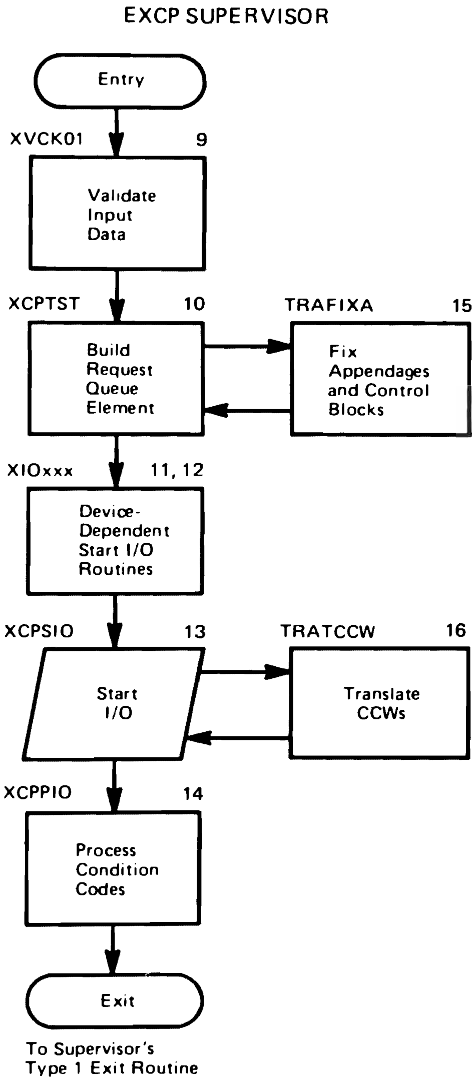
2 Sets up the TIC address to the requester's CCW chain.

3 Updates the SAVECCW if CCW translation is required. XCP131

4 Sets up the second IOS CCW for the tie command if this is a CRC correction. XCP132D

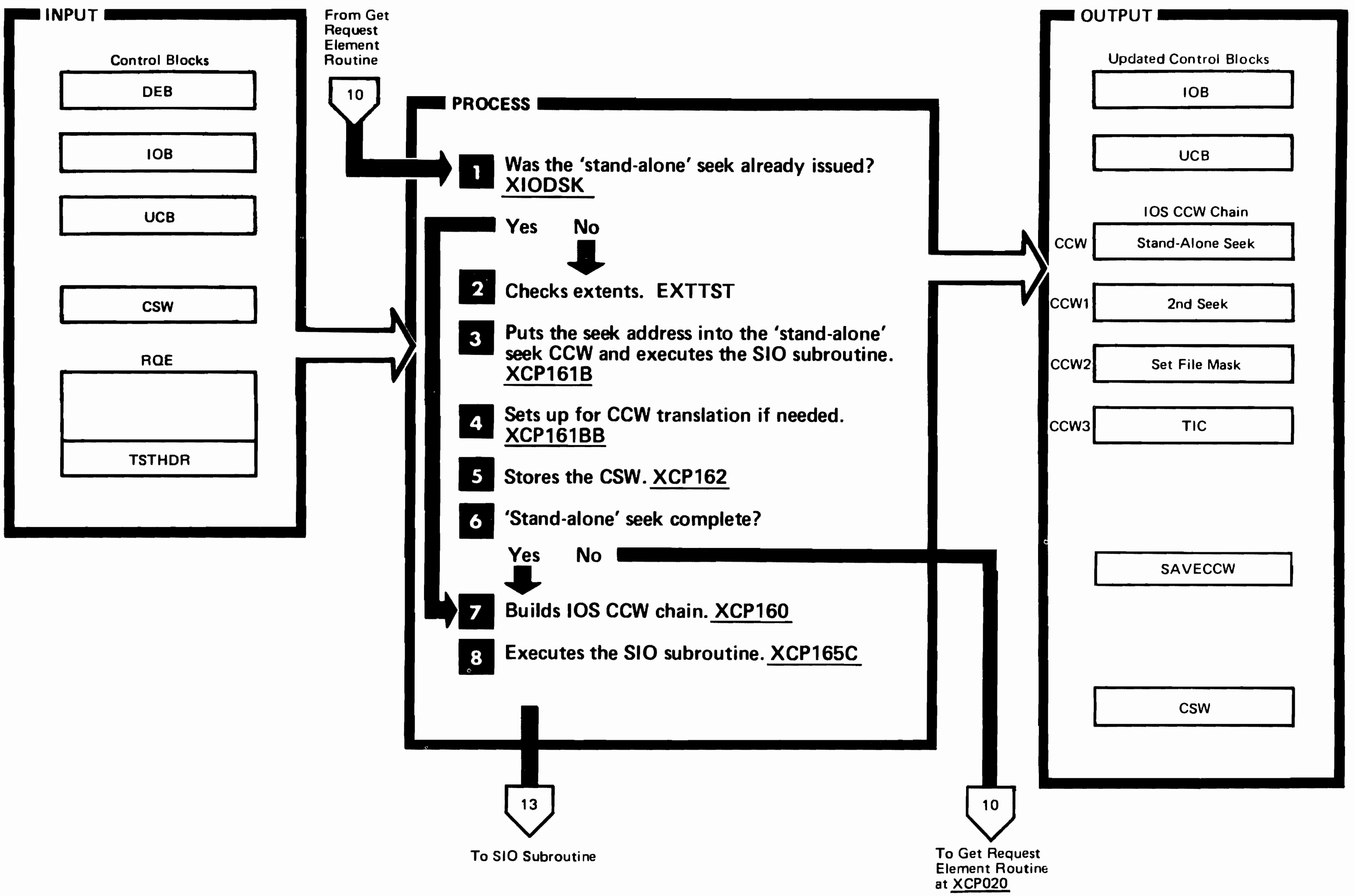
5 Places the 'set mode' command into the first IOS CCW. XCP133

Figure 11. (Part 1 of 2) Start I/O Routine for Tape



	Extended Description	Figure
1	The IOB is checked to determine if positioning is needed. If it is, the SIO subroutine is entered to execute a stand-alone CCW.	13
2	The TIC address is determined by the type of request. Non-subsystem 'start': Virtual address of the requester's 'start' CCW. Non-subsystem 'restart': Virtual address of the requester's 'restart' CCW. Subsystem 'start': Real address of the requester's 'start' CCW. Subsystem 'restart': Real address of the requester's 'restart' CCW. Read Opposite Recovery: The address of the ROR CCW which is obtained from the UCB.	
3	SAVECCW is loaded with the virtual address of the requester's first CCW.	
4	This CCW is used only for CRC correction. All other tape operations require only two CCWs.	
5	The 'set mode' command is obtained from the DEBMDM field of the DEB. This CCW sets parity and density.	

Figure 11. (Part 2 of 2) Start I/O Routine for Tape.



1 Was the 'stand-alone' seek already issued? XIODSK

2 Checks extents. EXTTST

3 Puts the seek address into the 'stand-alone' seek CCW and executes the SIO subroutine. XCP161B

4 Sets up for CCW translation if needed. XCP161BB

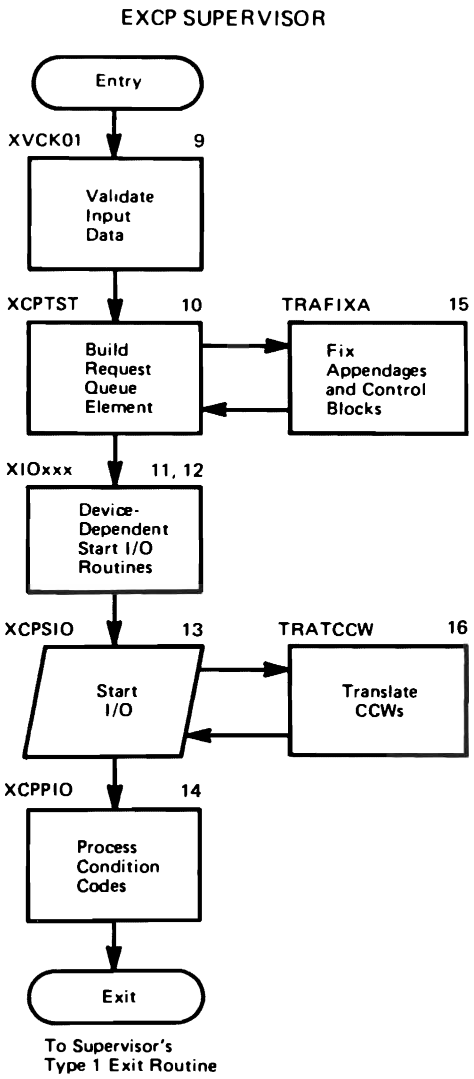
5 Stores the CSW. XCP162

6 'Stand-alone' seek complete?

7 Builds IOS CCW chain. XCP160

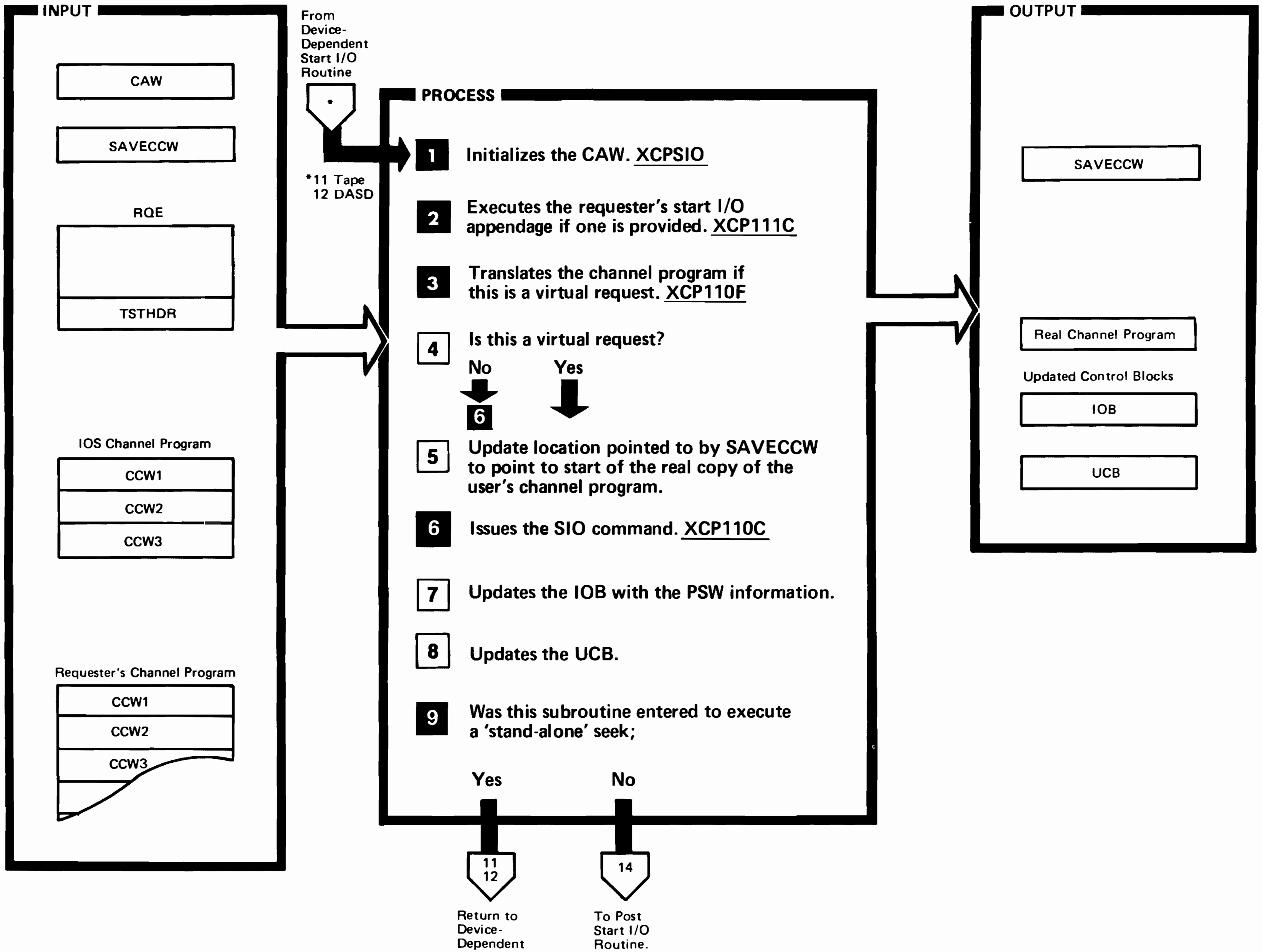
8 Executes the SIO subroutine. XCP165C

Figure 12. (Part 1 of 2) Start I/O Routine for DASD



	Extended Description	Figure
1	The 'stand-alone' seek is issued so that other I/O operations can be executed on the channel while the seek is taking place.	
2	The Extent Test routine is entered to determine if the seek address falls within the extent limits. If it doesn't, the routine exits to the Abnormal End appendage.	
3	The SIO subroutine is entered to start the access mechanism in motion.	13
4	If this is a virtual storage request, SAVECCW will point to a pointer that will indicate where CCW translation is to start.	
5	The status resulting from the 'stand-alone' seek is moved from the CSW to the IOB.	
6	If Device End occurs, the remainder of the IOSCCW chain is executed. Otherwise, the Get Request Element routine is entered to enqueue the RQE and process other requests.	10
7	Three IOS CCWs are generated: 2nd Seek: Reinstates in the control unit, the address at which data transfer begins. Set File Mask: Indicates to the channel, those commands that are valid for the current request. TIC: Contains the address of the requester's 1st CCW.	
8	The SIO subroutine performs any necessary CCW translation, then executes the SIO instruction.	13

Figure 12. (Part 2 of 2) Start I/O Routine for DASD



1 Initializes the CAW. XCPSIO

2 Executes the requester's start I/O appendage if one is provided. XCP111C

3 Translates the channel program if this is a virtual request. XCP110F

4 Is this a virtual request?

No → 6 Yes

5 Update location pointed to by SAVECCW to point to start of the real copy of the user's channel program.

6 Issues the SIO command. XCP110C

7 Updates the IOB with the PSW information.

8 Updates the UCB.

9 Was this subroutine entered to execute a 'stand-alone' seek;

Yes No

Figure 13. (Part 1 of 2) SIO Subroutine

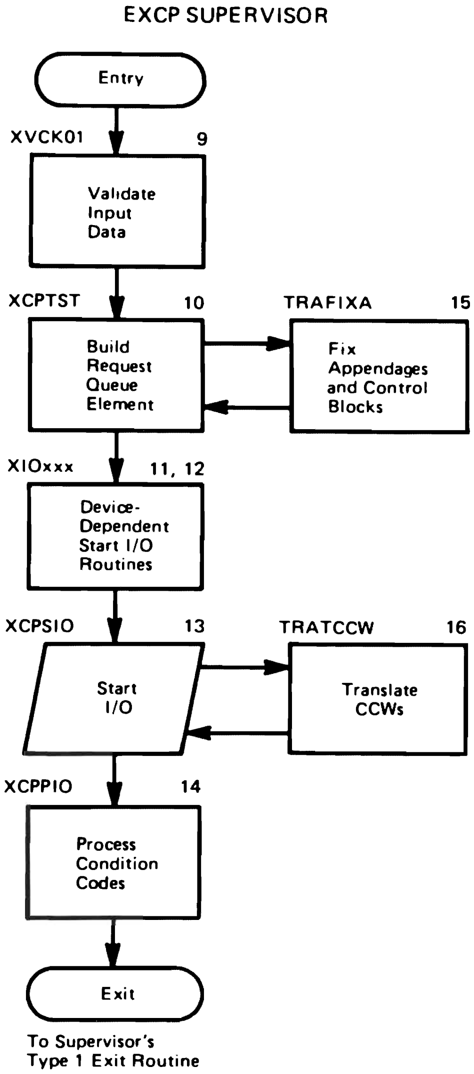
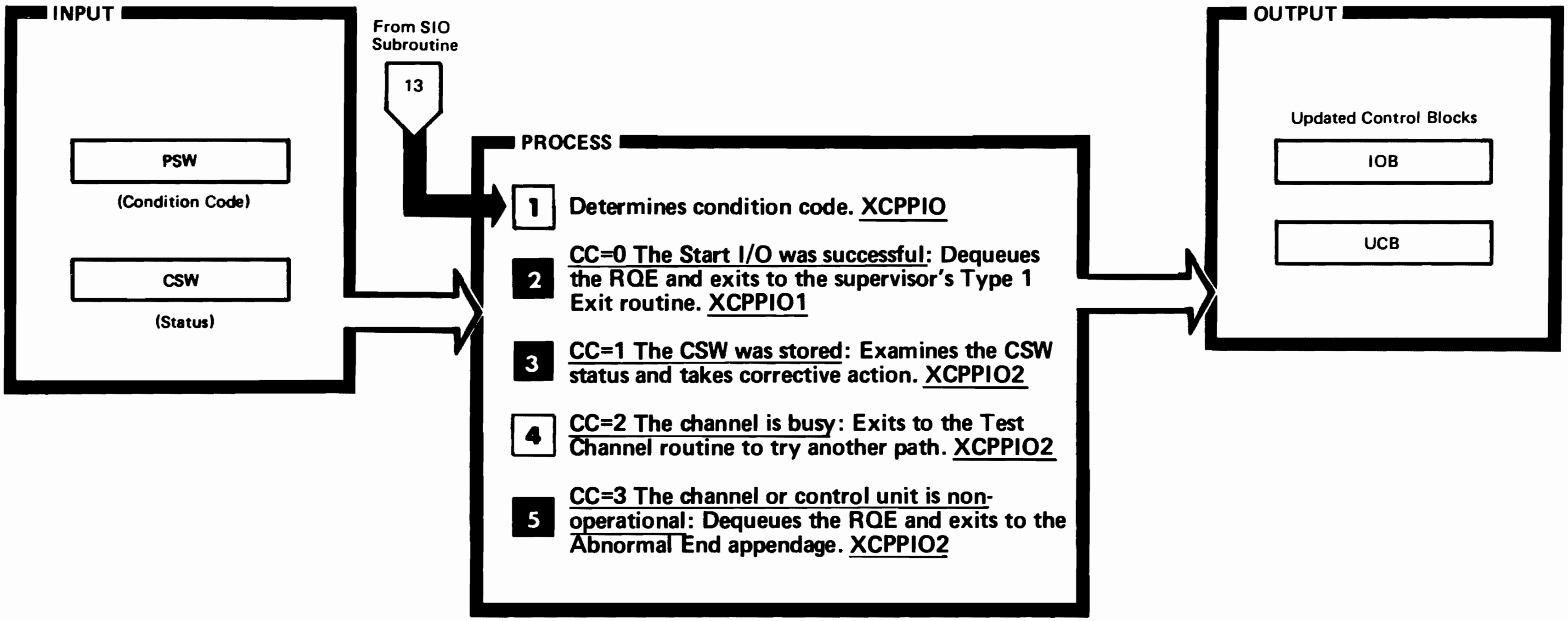


Figure 13. (Part 2 of 2) SIO Subroutine

	Extended Description	Figure
1	The address of the first IOS CCW is placed into the CAW.	
2	The requester is given the opportunity to modify or extend the channel program prior to CCW translation, or to skip the SIO operation via the requester's SIO appendage.	
3	The TSTHDR field of the RQE is checked to determine if this is a virtual request. If it is, a pointer to the address of the requester's first CCW is placed in a one-word field (SAVECCW). The CCW translate routine is then entered to translate the virtual channel program to a real-channel program.	16
6	The condition code, instruction length code, and program mask are stored in the IOB. The condition codes are: 0 - The I/O operation was initiated and the channel is proceeding with its execution. 1 - The CSW was stored. 2 - The channel or subchannel is busy. 3 - The channel or control unit is not operational.	
9	The address of the RQE and the address of the physical channel used for this I/O operation are stored in the UCB for later use by the Sense routine.	21



1 Determines condition code. XCPPIO

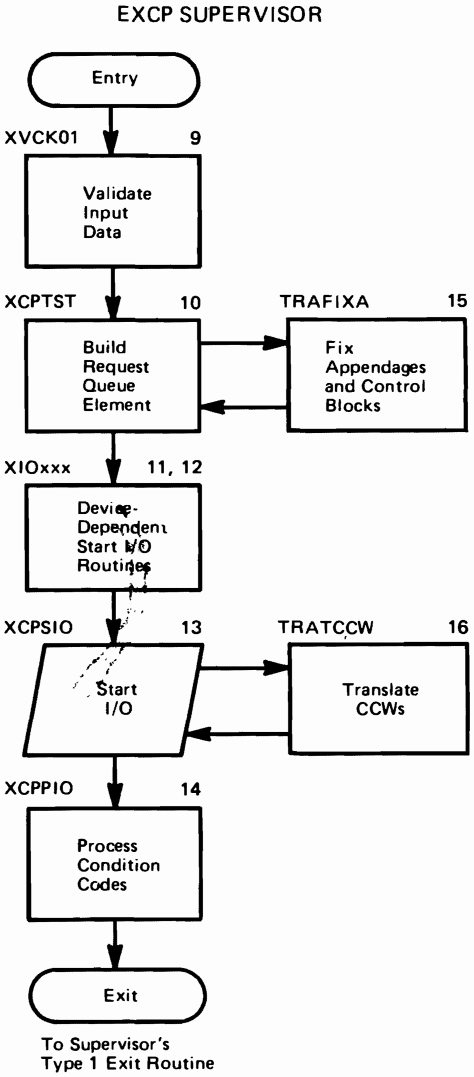
2 CC=0 The Start I/O was successful: Dequeues the RQE and exits to the supervisor's Type 1 Exit routine. XCPPIO1

3 CC=1 The CSW was stored: Examines the CSW status and takes corrective action. XCPPIO2

4 CC=2 The channel is busy: Exits to the Test Channel routine to try another path. XCPPIO2

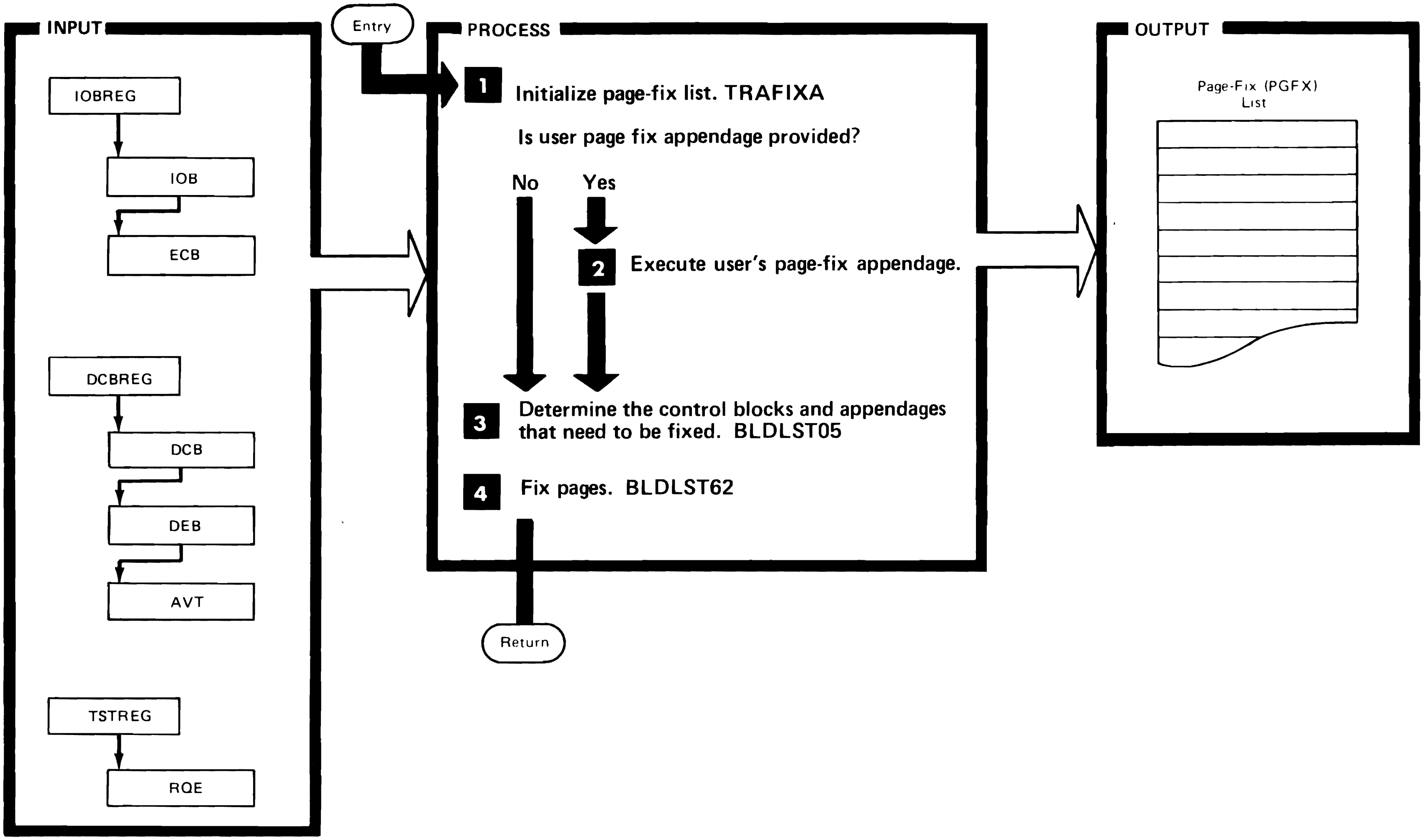
5 CC=3 The channel or control unit is non-operational: Dequeues the RQE and exits to the Abnormal End appendage. XCPPIO2

Figure 14. (Part 1 of 2) Post Start I/O Routine



	Extended Description	Figure
2	The dequeue routine is entered at XCPPDQ to remove the RQE from the logical channel queue.	
3	If it was a virtual or fixed request, the real CCW address in the CSW is translated to virtual and put in the IOB along with the 7 low-order bytes of the CSW. The CSW status is then examined and the following actions taken: Catastrophic Error: The unit address is put into I/O old CSW and the Channel Check Handler is entered. XCPP103 Control Unit End: The get Request Element routine is reentered at XCP011 to try the I/O operation again. XCP056EA Attention Status or Device End: The I/O Interruption Supervisor is entered at INTATT2 to execute the attention routine, if provided, and to restart the channel. XCPPIO4 For all other conditions, the Test Channel routine is entered to retry the I/O operation	10
5	If it was a virtual or fixed request, the real CCW address in the CSW is translated to virtual and put in the IOB along with the 7 low order bytes of the CSW. The unit check and intervention required indicators are set in the IOB, and the RQE is dequeued before exiting to the Abnormal End appendage.	

Figure 14. (Part 2 of 2) Post Start I/O Routine



1 Initialize page-fix list. TRAFIXA

Is user page fix appendage provided?

2 Execute user's page-fix appendage.

3 Determine the control blocks and appendages that need to be fixed. BLDLST05

4 Fix pages. BLDLST62

Figure 15. (Part 1 of 2) Page Fix Routine

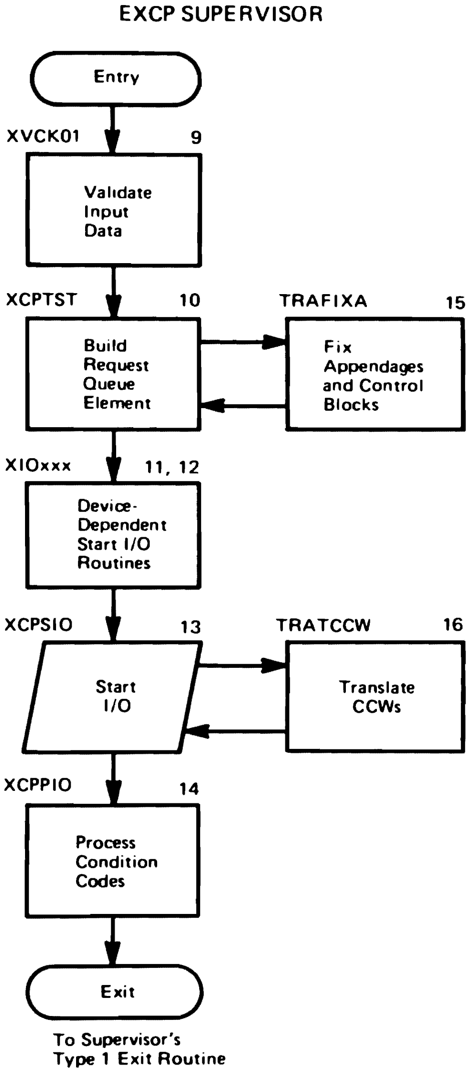
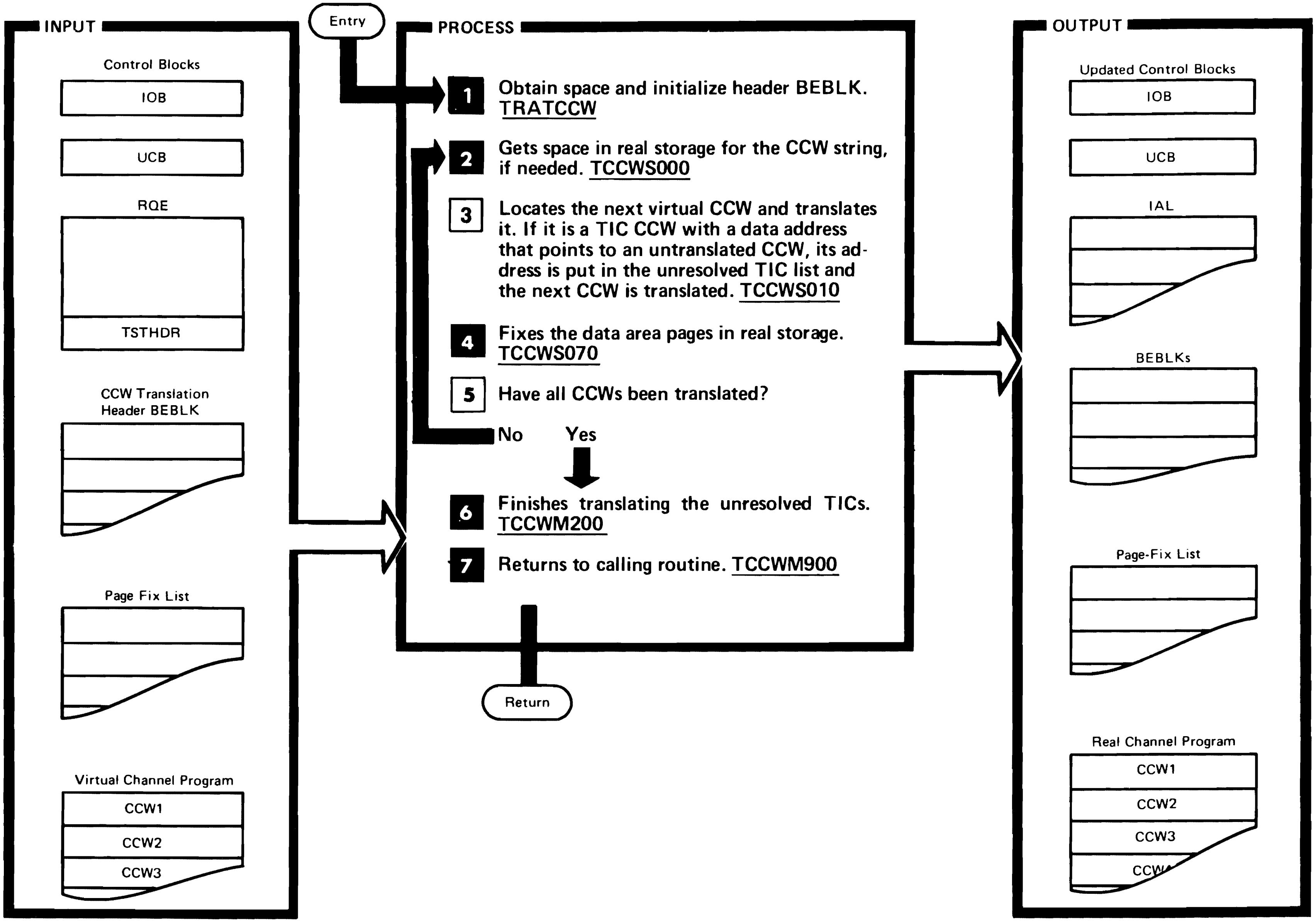


Figure 15. (Part 2 of 2) Page Fix Routine

Extended Description		Figure
1	A block to be used as a page-fix list is acquired from the SQA space owned by IOS. The TSTHDR field of the RQE points to the page-fix list until translation time.	
2	The user can make entries in the page-fix list for I/O appendages and other data. A maximum of seven entries are permitted. Ten entries may be specified with a special return vector (+4). The user must also include entries for his DCB, DECB, and IOB.	
3	Pages for the IOB, ECB, DCB, AVT, and IOS appendages must all be fixed in real storage. Those that are not already fixed are added to the page-fix list.	
4	The Page Supervisor fixes all of the pages that are specified by the page-fix list. If the page is not already in real storage, an I/O operation (page-in) is requested.	



1 Obtain space and initialize header BEBLK. TRATCCW

2 Gets space in real storage for the CCW string, if needed. TCCWS000

3 Locates the next virtual CCW and translates it. If it is a TIC CCW with a data address that points to an untranslated CCW, its address is put in the unresolved TIC list and the next CCW is translated. TCCWS010

4 Fixes the data area pages in real storage. TCCWS070

5 Have all CCWs been translated?

6 Finishes translating the unresolved TICs. TCCWM200

7 Returns to calling routine. TCCWM900

Figure 16. (Part 1 of 2) CCW Translator

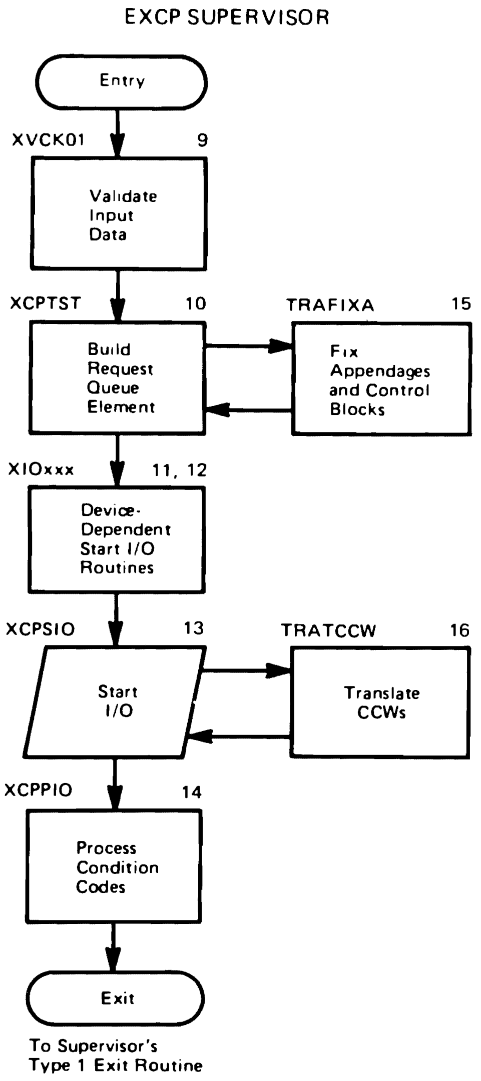


Figure 16. (Part 2 of 2) CCW Translator

	Extended Description	Figure
1	Space is obtained from the IOS owned SQA for a CCW translation header BEBLK. The TSTHDR field of the RQE is updated to point to the header BEBLK. The page-fix list obtained earlier is now pointed to by the HDRPGLK field of the header BEBLK.	
2	If the channel program exceeds the capacity of the header BEBLK, additional space is required to complete the translation and subroutine TCCWM300 is entered. This routine acquires SQA space for a new BEBLK. The new BEBLK is initialized and a TIC CCW is placed in the previous channel program segment. This TIC CCW contains a pointer to the first CCW slot in the new BEBLK. CCW translation continues.	
4	If the data area specified by the CCW crosses a page boundary, the page fix list is checked to ensure the page is fixed, and an IAL is generated. The IAL address is placed into the CCW's data address field. When the channel program is executed, data transfer begins with the first address of the IAL and continues until a 2K boundary is reached. It then continues data transfer from the next address in the IAL. This is repeated until the count in the CCW expires.	
6	Translation of the unresolved TICs can be completed by referencing the BEBLKs. The virtual addresses in the BEBLKs are scanned until a match is made with the TIC's virtual data address. The corresponding real address is then stored in the TIC command.	
7	The starting address of the real channel program is put into the HDRTICL field of the header BEBLK for use by the SIO routine.	

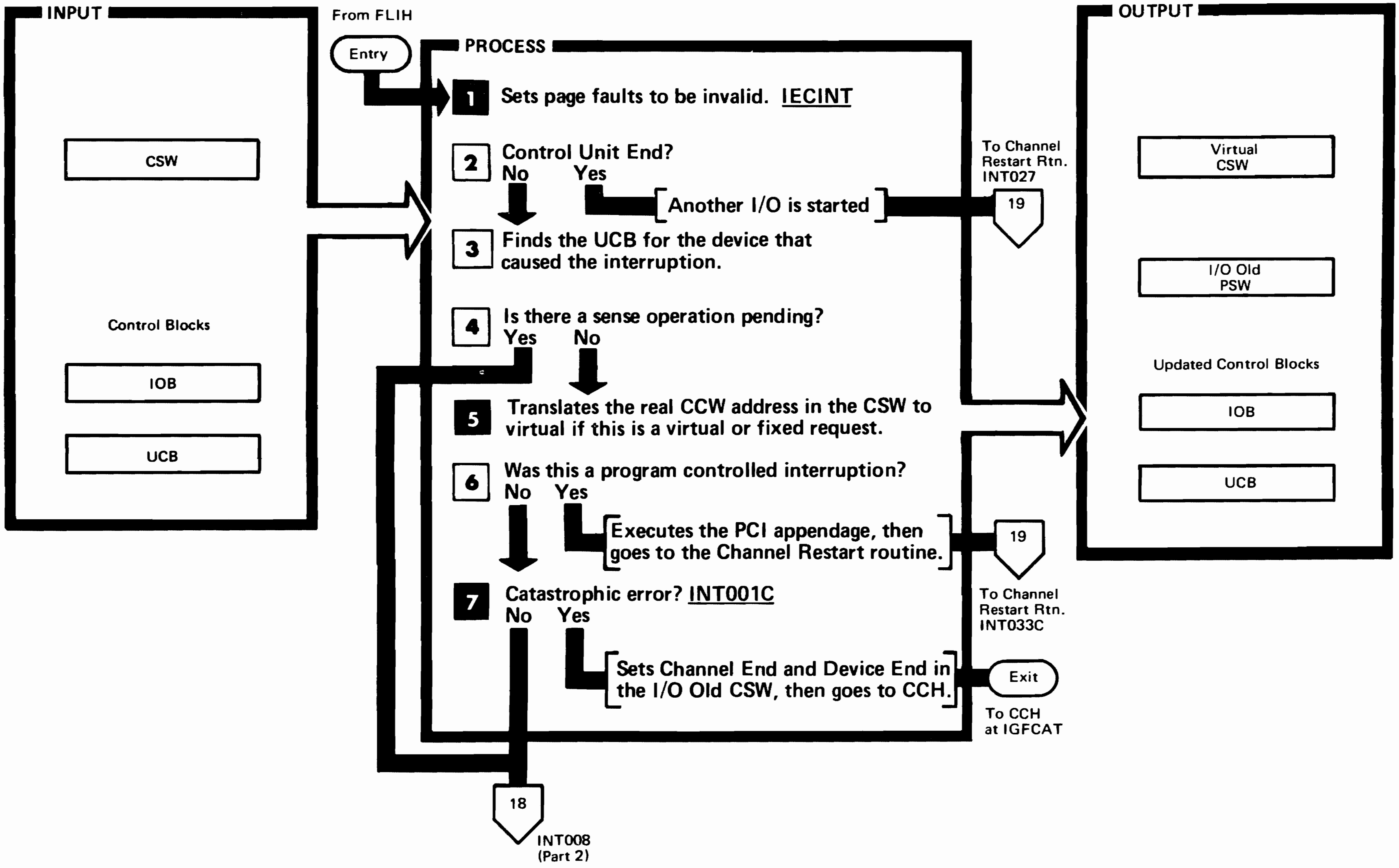
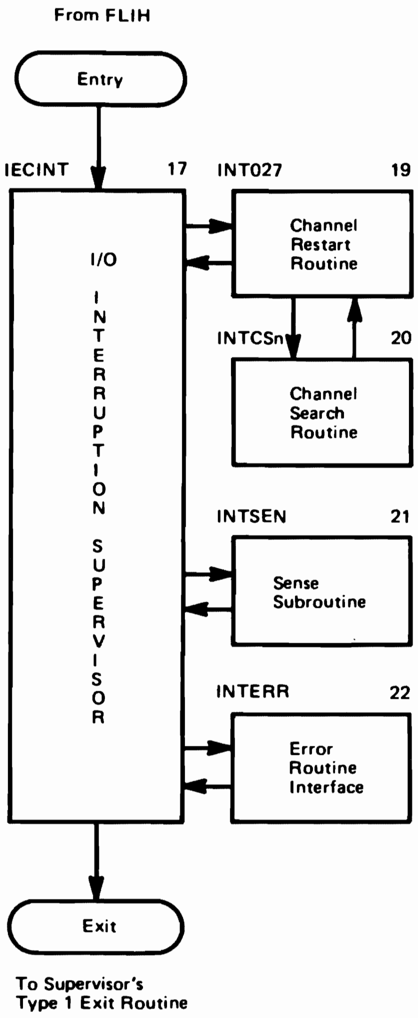

INPUT
CSW
Control Blocks
IOB
UCB
From FLIH
Entry
PROCESS
1 Sets page faults to be invalid. IECINT
2 Control Unit End?
No
Yes
Another I/O is started
To Channel Restart Rtn. INT027
19
3 Finds the UCB for the device that caused the interruption.
4 Is there a sense operation pending?
Yes
No
5 Translates the real CCW address in the CSW to virtual if this is a virtual or fixed request.
6 Was this a program controlled interruption?
No
Yes
Executes the PCI appendage, then goes to the Channel Restart routine.
19
To Channel Restart Rtn. INT033C
7 Catastrophic error? INT001C
No
Yes
Sets Channel End and Device End in the I/O Old CSW, then goes to CCH.
Exit
To CCH at IGFCAT
18
INT008 (Part 2)
OUTPUT
Virtual CSW
I/O Old PSW
Updated Control Blocks
IOB
UCB

Figure 17. (Part 1 of 2) I/O Interruption Supervisor (Part 1)



Extended Description		Figure
5	The CSW Translator is entered at TRATCSW. If it was a virtual or fixed request, the real CCW address in the CSW is replaced by the corresponding virtual CCW address found in the BEBLK.	
7	Catastrophic errors are: ● Channel Control Check ● Interface Control Check ● Channel Data Check	

Figure 17. (Part 2 of 2) I/O Interruption Supervisor (Part 1)

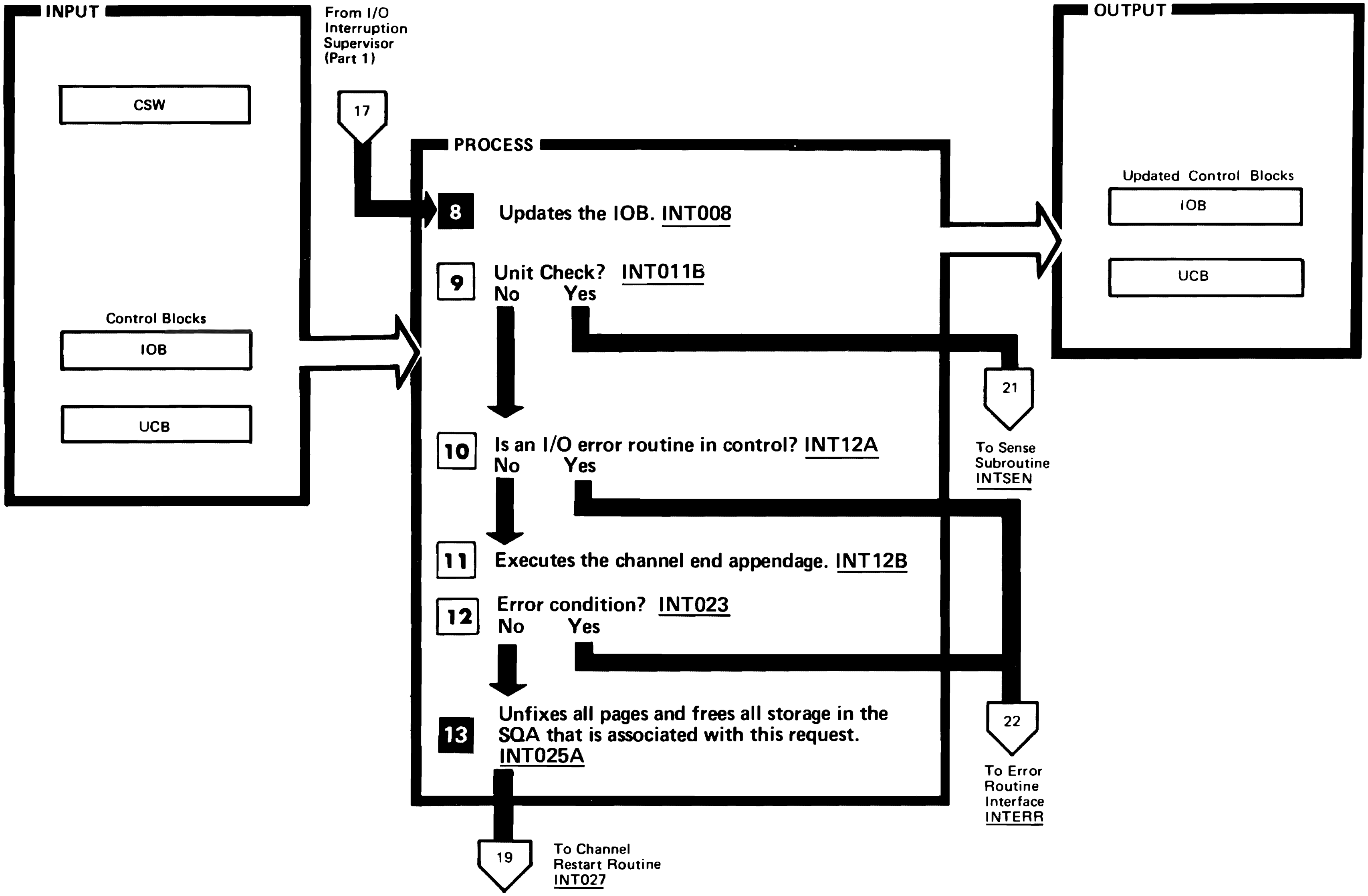
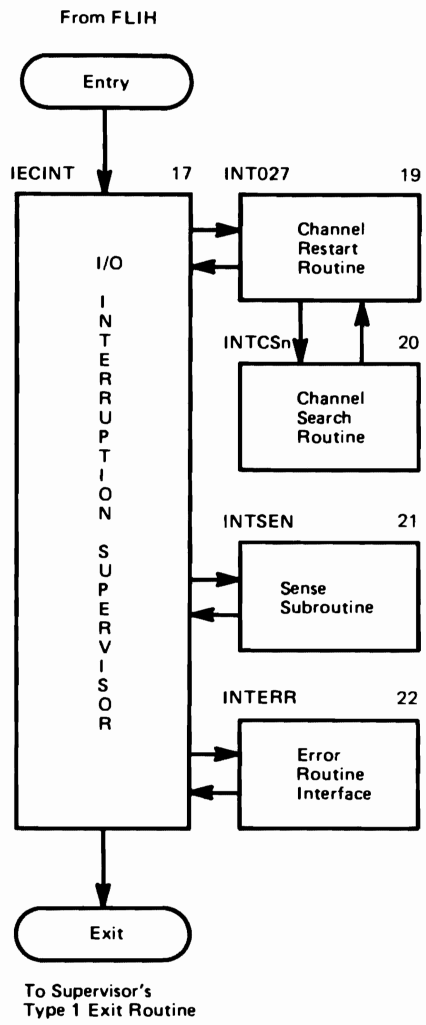
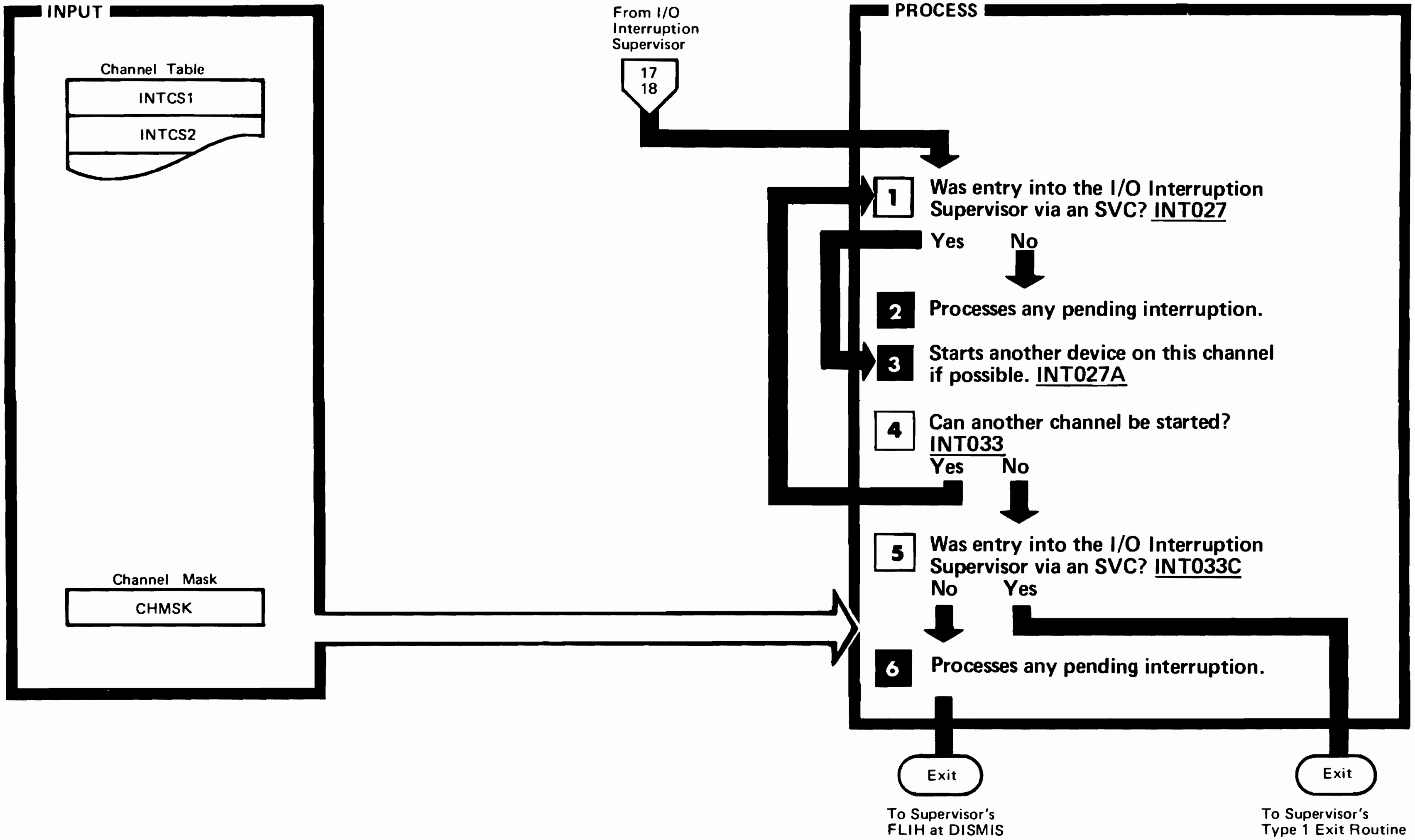


Figure 18. (Part 1 of 2) I/O Interruption Supervisor (Part 2)



Extended Description		Figure
8	The seven low-order bytes of the CSW are placed into the IOB.	
13	The Unfix/Free routine of the CCW Translator is entered at TRAUFRE. Pages used for control blocks and appendages are unfixed, and space in the SQA that was used for the page-fix list and translation header record is freed.	

Figure 18. (Part 2 of 2) I/O Interruption Supervisor (Part 2)


INPUT
Channel Table
INTCS1
INTCS2
Channel Mask
CHMSK
From I/O Interruption Supervisor
17
18
PROCESS
Yes
No
Yes
No
No
Yes
Exit
To Supervisor's FLIH at DISMIS
Exit
To Supervisor's Type 1 Exit Routine

1 Was entry into the I/O Interruption Supervisor via an SVC? INT027

2 Processes any pending interruption.

3 Starts another device on this channel if possible. INT027A

4 Can another channel be started? INT033

5 Was entry into the I/O Interruption Supervisor via an SVC? INT033C

6 Processes any pending interruption.

Figure 19. (Part 1 of 2) Channel Restart Routine

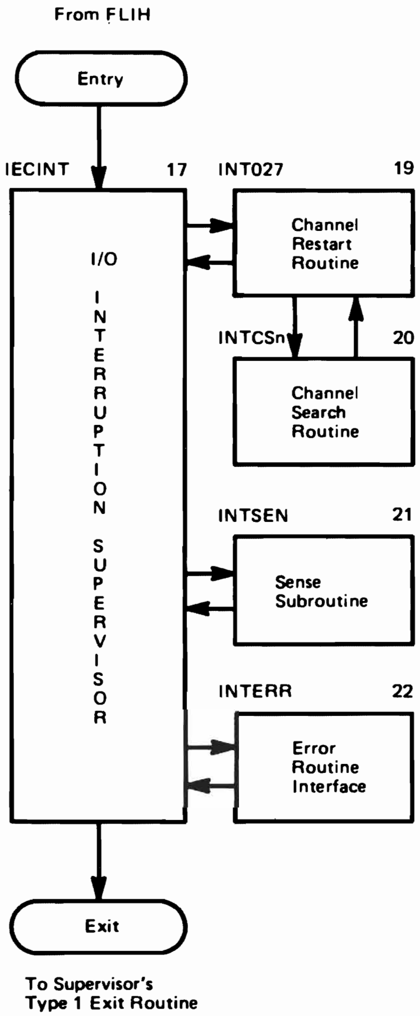
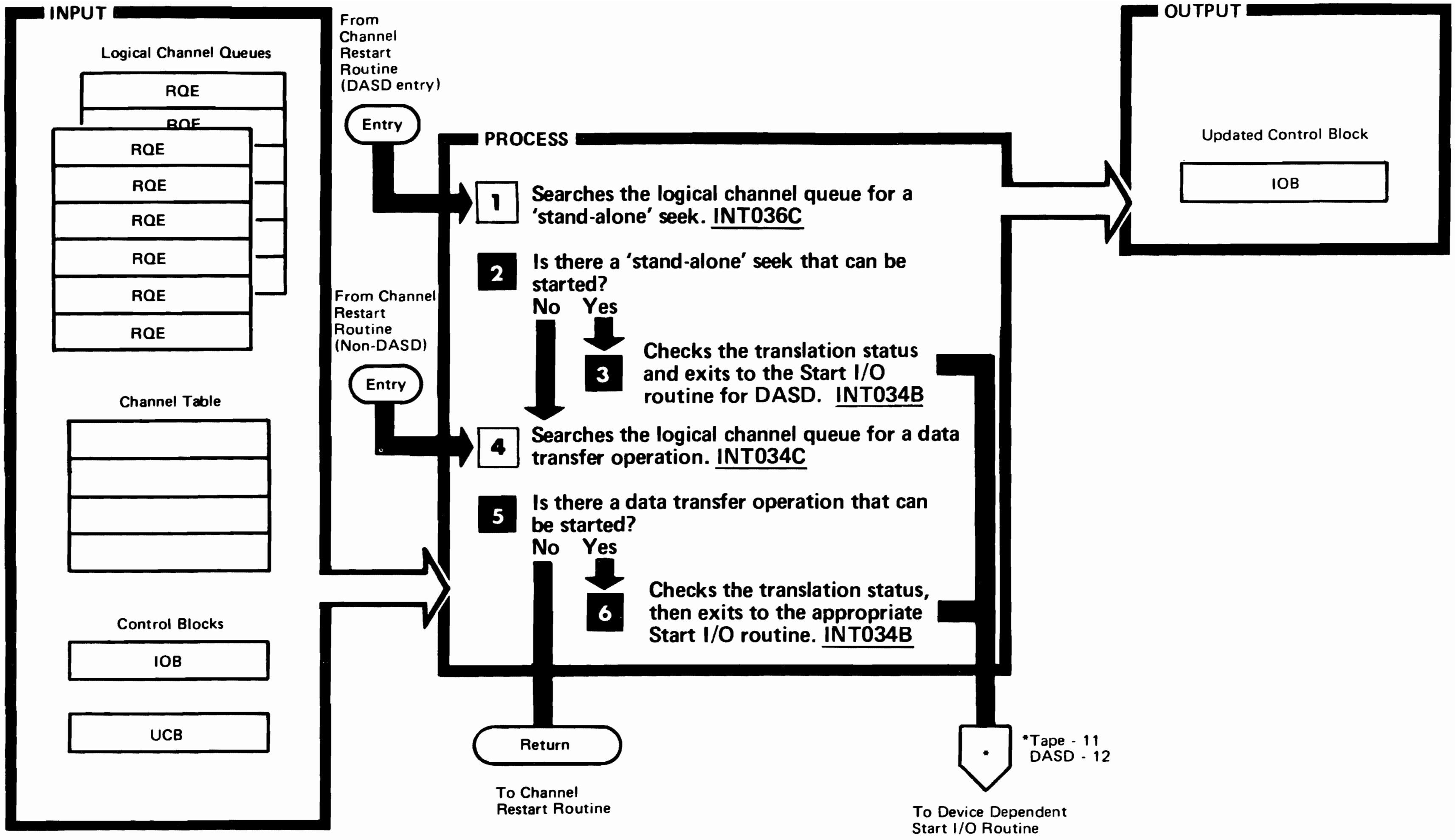


Figure 19. (Part 2 of 2) Channel Restart Routine

	Extended Description	Figure
2	If there is an interruption pending, the I/O Interruption Supervisor is reentered at IECINT.	17
3	The Channel Search routine is entered at INTCSn to determine if another I/O operation can be started on this logical channel. The channel table contains the Channel Search routine entry point for each logical channel.	20
6	Same as 2	



1 Searches the logical channel queue for a 'stand-alone' seek. INT036C

2 Is there a 'stand-alone' seek that can be started?

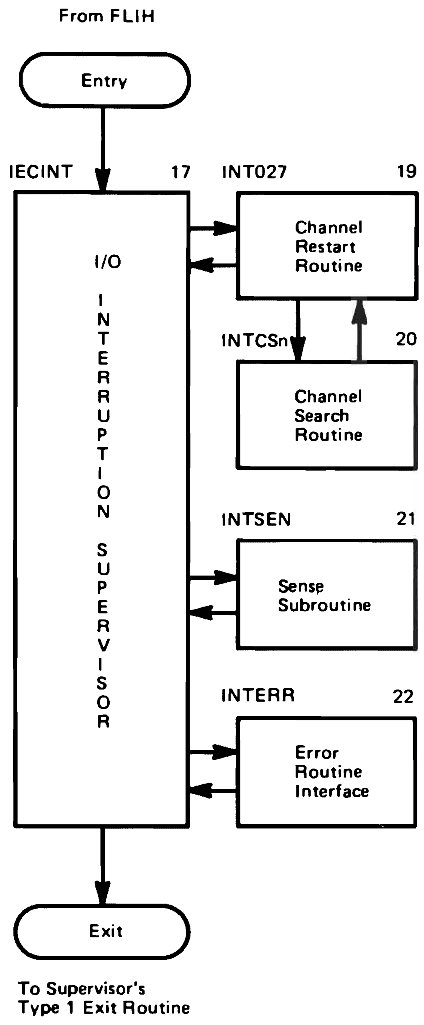
3 Checks the translation status and exits to the Start I/O routine for DASD. INT034B

4 Searches the logical channel queue for a data transfer operation. INT034C

5 Is there a data transfer operation that can be started?

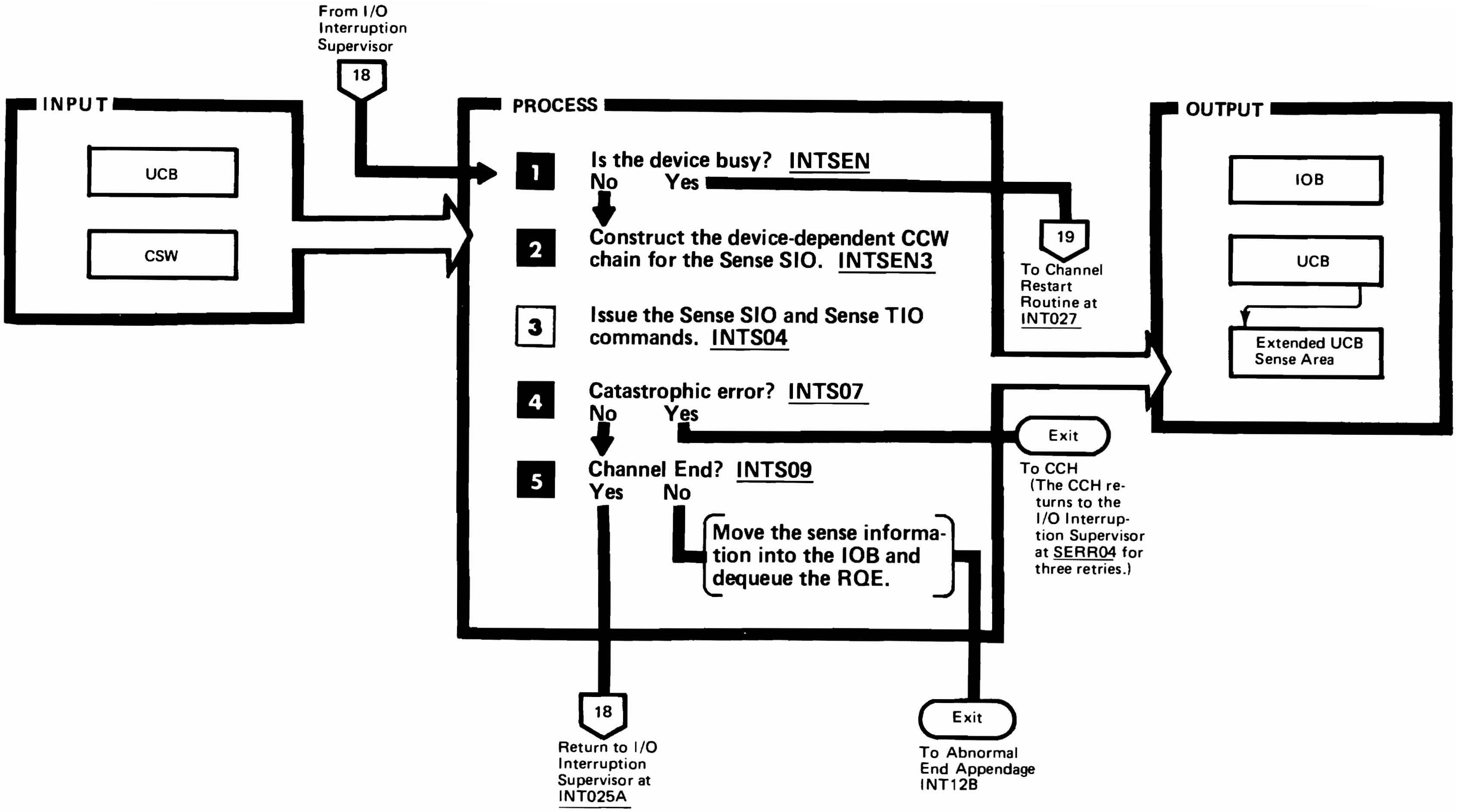
6 Checks the translation status, then exits to the appropriate Start I/O routine. INT034B

Figure 20. (Part 1 of 2) Channel Search Routine



Extended Description		Figure
2	If there is no stand-alone seek found that can be started, and there are alternate paths available, the next associated logical channel queue is searched. This is repeated until all the paths are checked or a stand-alone seek is found.	
3	If this is a virtual request and the CCW translation was not done, this RQE is bypassed. This routine is reentered at INTCIC to continue the search where it left off. If this request is related to another request that resulted in an error, exit is taken to the Abnormal End appendage.	
5	If there are no I/O operations that can be started on this channel, and there are alternate paths available, the next associated logical channel queue is searched. This is repeated until all paths are checked or until a startable I/O operation is found.	
6	Same as 3	

Figure 20. (Part 2 of 2) Channel Search Routine


From I/O Interruption Supervisor
18
INPUT
UCB
CSW
PROCESS
OUTPUT
IOB
UCB
Extended UCB Sense Area
19
To Channel Restart Routine at INT027
Exit
To CCH (The CCH returns to the I/O Interruption Supervisor at SERR04 for three retries.)
18
Return to I/O Interruption Supervisor at INT025A
Exit
To Abnormal End Appendage INT12B

1 Is the device busy? INTSEN
No Yes

2 Construct the device-dependent CCW chain for the Sense SIO. INTSEN3

3 Issue the Sense SIO and Sense TIO commands. INTS04

4 Catastrophic error? INTS07
No Yes

5 Channel End? INTS09
Yes No

Move the sense information into the IOB and dequeue the RQE.

Figure 21. (Part 1 of 2) Sense Subroutine

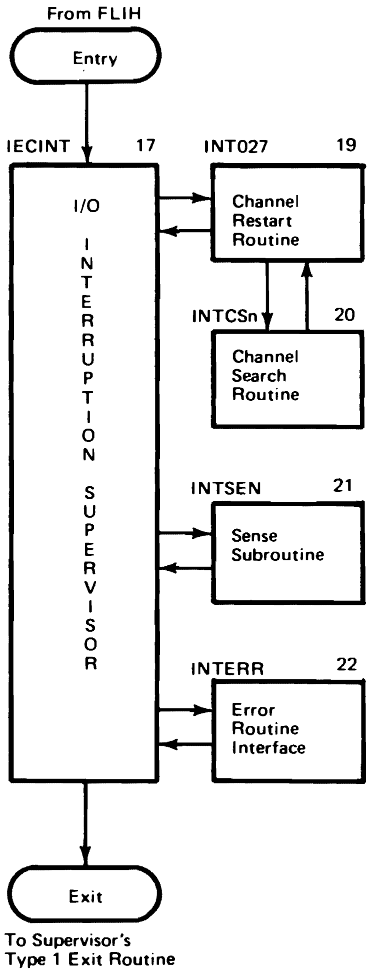


Figure 21. (Part 2 of 2) Sense Subroutine

Extended Description		Figure
1	A flag is set in the IOB to cause this routine to be reentered after Device End occurs.	
2	1403 with UCS, 3211,--Initialize the CCW chain to read the sense data into the 2305, 3330, and 3333 extended UCB sense area. All other devices--Initialize the CCW chain to read up to 6 sense bytes into the UCB.	
4	Catastrophic errors are: ● Channel Control Check ● Interface Control Check ● Channel Data Check	
5	The UCBPST flag in the UCB is checked to determine if the RQE is active. This flag is set when the I/O operation is started, and is reset when Channel End is encountered.	

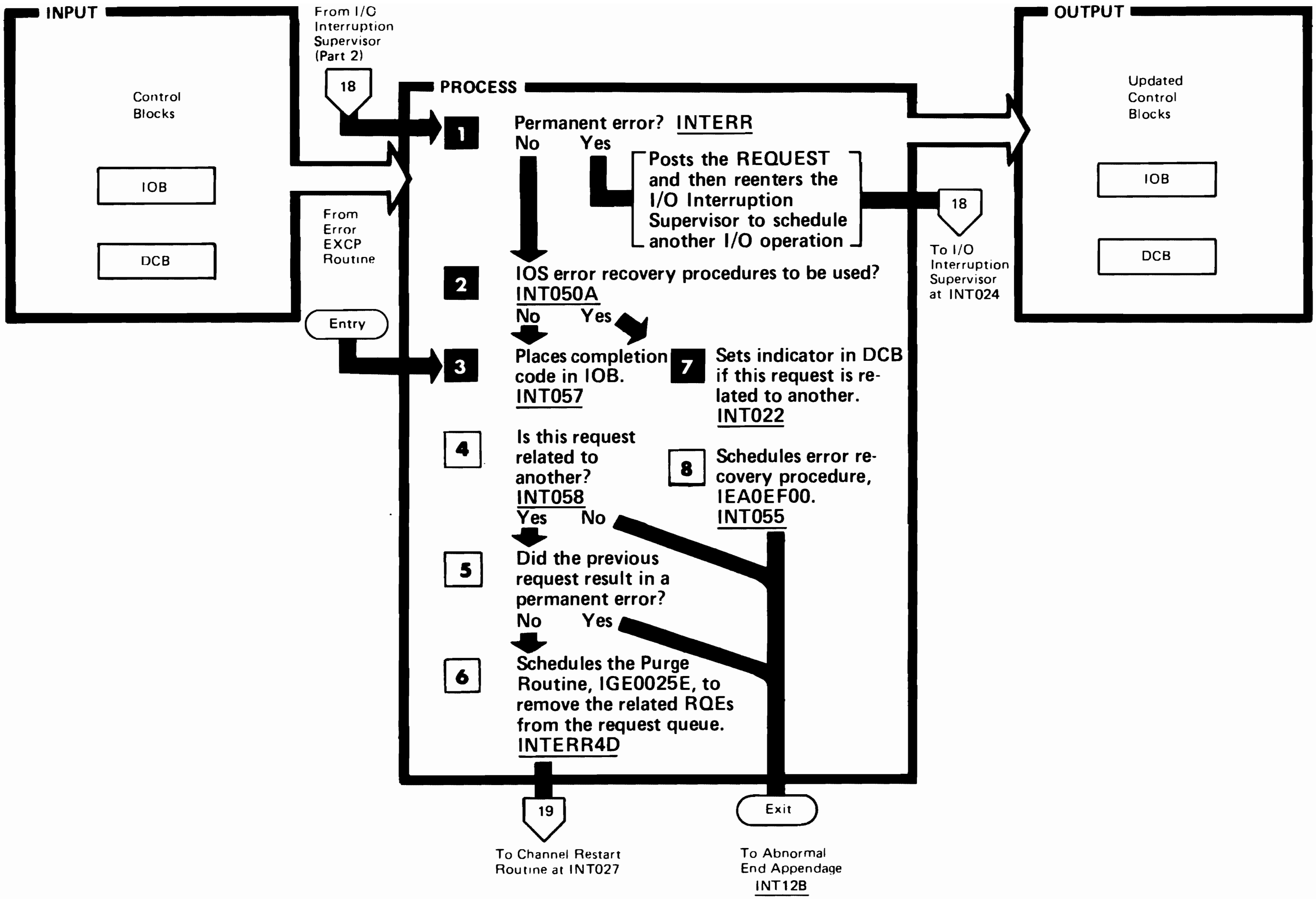
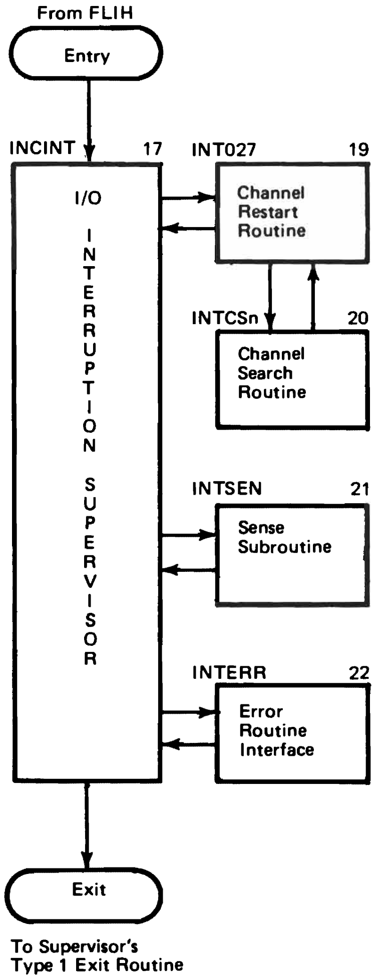

INPUT
Control Blocks
IOB
DCB
From I/O Interruption Supervisor (Part 2)
18
From Error EXCP Routine
Entry
PROCESS
1
Permanent error? INTERR
No
Yes
Posts the REQUEST and then reenters the I/O Interruption Supervisor to schedule another I/O operation
2
IOS error recovery procedures to be used? INT050A
No
Yes
3
Places completion code in IOB. INT057
7
Sets indicator in DCB if this request is related to another. INT022
4
Is this request related to another? INT058
Yes
No
8
Schedules error recovery procedure, IEA0EF00. INT055
5
Did the previous request result in a permanent error?
No
Yes
6
Schedules the Purge Routine, IGE0025E, to remove the related RQEs from the request queue. INTERR4D
19
To Channel Restart Routine at INT027
Exit
To Abnormal End Appendage INT12B
18
To I/O Interruption Supervisor at INT024
OUTPUT
Updated Control Blocks
IOB
DCB

Figure 22. (Part 1 of 2) Error Routine Interface



	Extended Description	Figure
1	An X'41' in the completion code byte of the IOB, IOBCD, indicates a permanent error.	
2	An X'0C' in the DCBFL byte of the DCB indicates IOS ERPs are to be used.	
3	The completion code, IOBCOD, is set to: X'44' (Intercepted Request) if this request is an intercepted I/O request. X'41' (Permanent Error) if this request is not related to a previous request that resulted in a permanent error. Unchanged if this request is related to a previous request that resulted in a permanent error.	
7	An X'40' is placed into the DCBFL byte to indicate error correction is in progress.	

Figure 22. (Part 2 of 2) Error Routine Interface

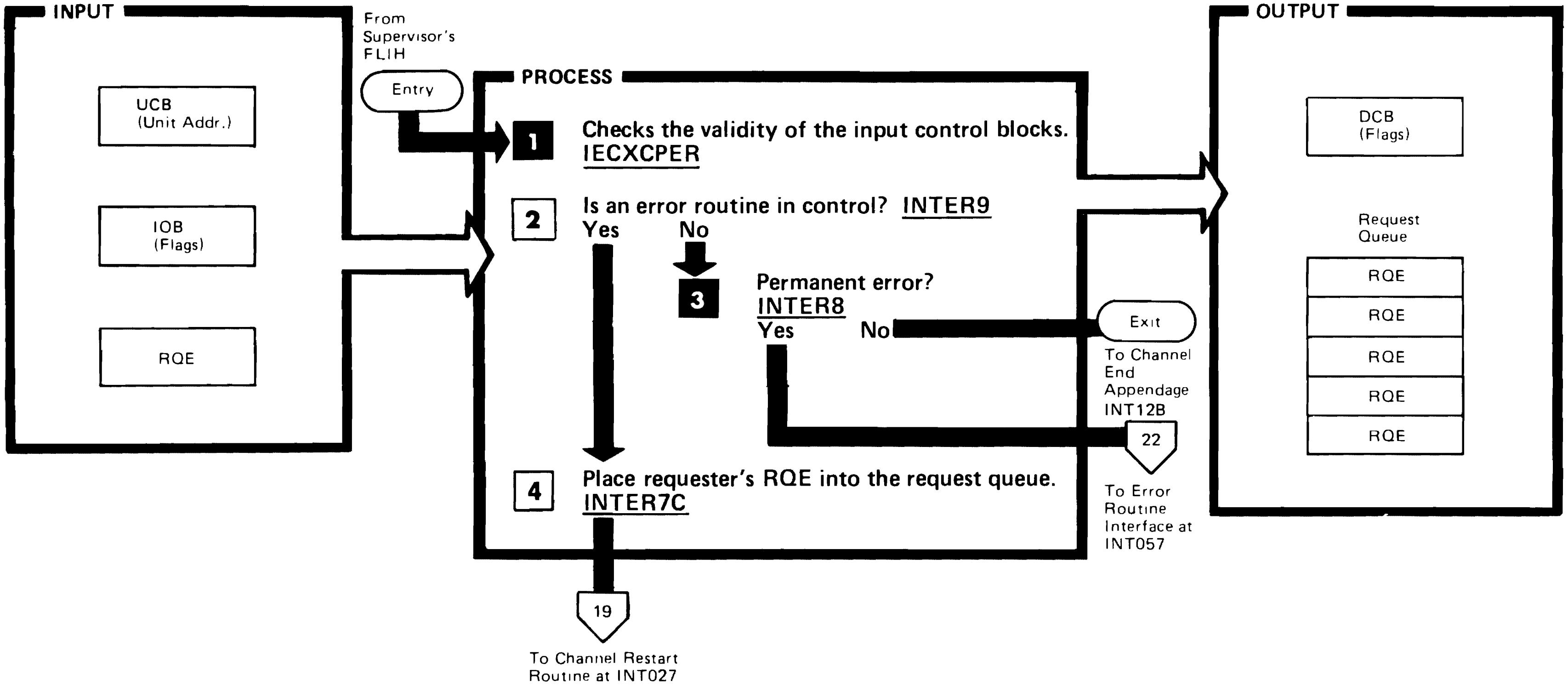

INPUT
UCB (Unit Addr.)
IOB (Flags)
RQE
From Supervisor's FLIH
Entry
PROCESS
1 Checks the validity of the input control blocks. IECXCPER
2 Is an error routine in control? INTER9
Yes
No
3 Permanent error? INTER8
Yes
No
Exit
To Channel End Appendage INT12B
22
To Error Routine Interface at INT057
4 Place requester's RQE into the request queue. INTER7C
19
To Channel Restart Routine at INT027
OUTPUT
DCB (Flags)
Request Queue
RQE
RQE
RQE
RQE
RQE

Figure 23. (Part 1 of 2) Error EXCP Routine

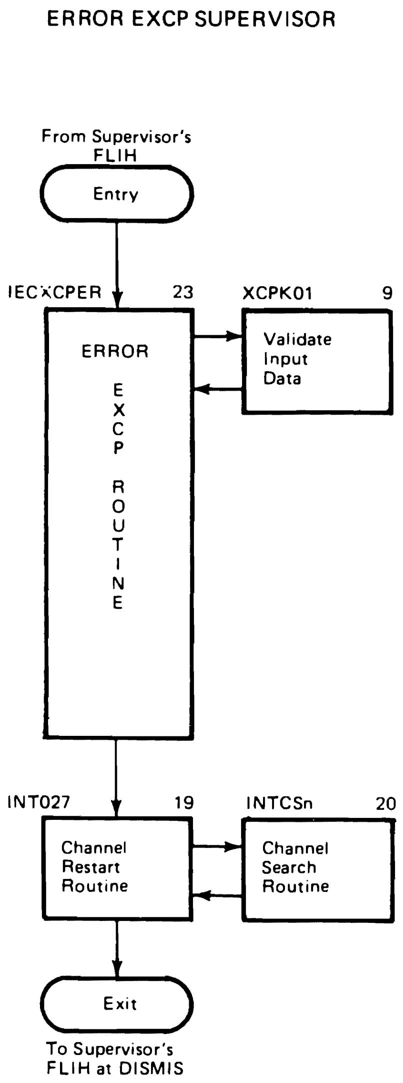


Figure 23. (Part 2 of 2) Error EXCP Routine

Extended Description		Figure
1	The Validity Check routine is executed to ensure various fields within the control blocks are valid. If any of the tests are not satisfied, the ABEND routine, IEA0AB00, is entered.	9
3	If this is not a permanent error, the 'I/O Error Routine in Control' flag in the DCB is turned off before exiting to the Channel End Appendage.	

PROGRAM ORGANIZATION

This section contains functional organization charts and a description of the individual routines. There is a functional organization chart for each of the three functions of the I/O supervisor.

Description of Routines

In Figure 24, 25, and 26 the major I/O supervisor routines are grouped according to the functions that they perform. Brief descriptions of the routines and optional user-written appendage routines follow.

Abnormal end appendage: Optional user-written appendage to which the I/O interruption supervisor exits when there is an error associated with the processing of I/O.

Attention Routine Interface: Determines the address of the appropriate Attention routine; invokes the Attention routine.

Channel Command Word Translator routine: Converts the virtual channel program to a real channel program.

Channel Check Handler routine: Builds error recovery procedure interface block to indicate cause of channel failure; builds inboard record to describe environment at time of failure.

Channel Check Handler Routine Interface: Places a code into register 15 that indicates which IOS routine intercepted the channel failure and branches to the Channel Check Handler routine.

Channel end appendage: Optional user-written appendage to which the I/O interruption supervisor exits after a channel end interruption before indicating to the user how his I/O request ended. Also entered when channel end interruption is accompanied by either a wrong length indicator or a unit exception, or by both conditions.

Channel Restart routine: Scans logical channel queues. Selects RQEs representing requests for I/O activity that can be started. Starts the I/O activity. For direct-access devices, first starts all seeks, then starts the data transfer.

Channel Search routines: One for every physical channel. "Driver" type routines consisting mostly of branch instructions. Direct the search of logical channel queues and the starting of I/O activity.

Channel Status Word Translator routine: Converts the real CSW address to a virtual address for virtual requesters.

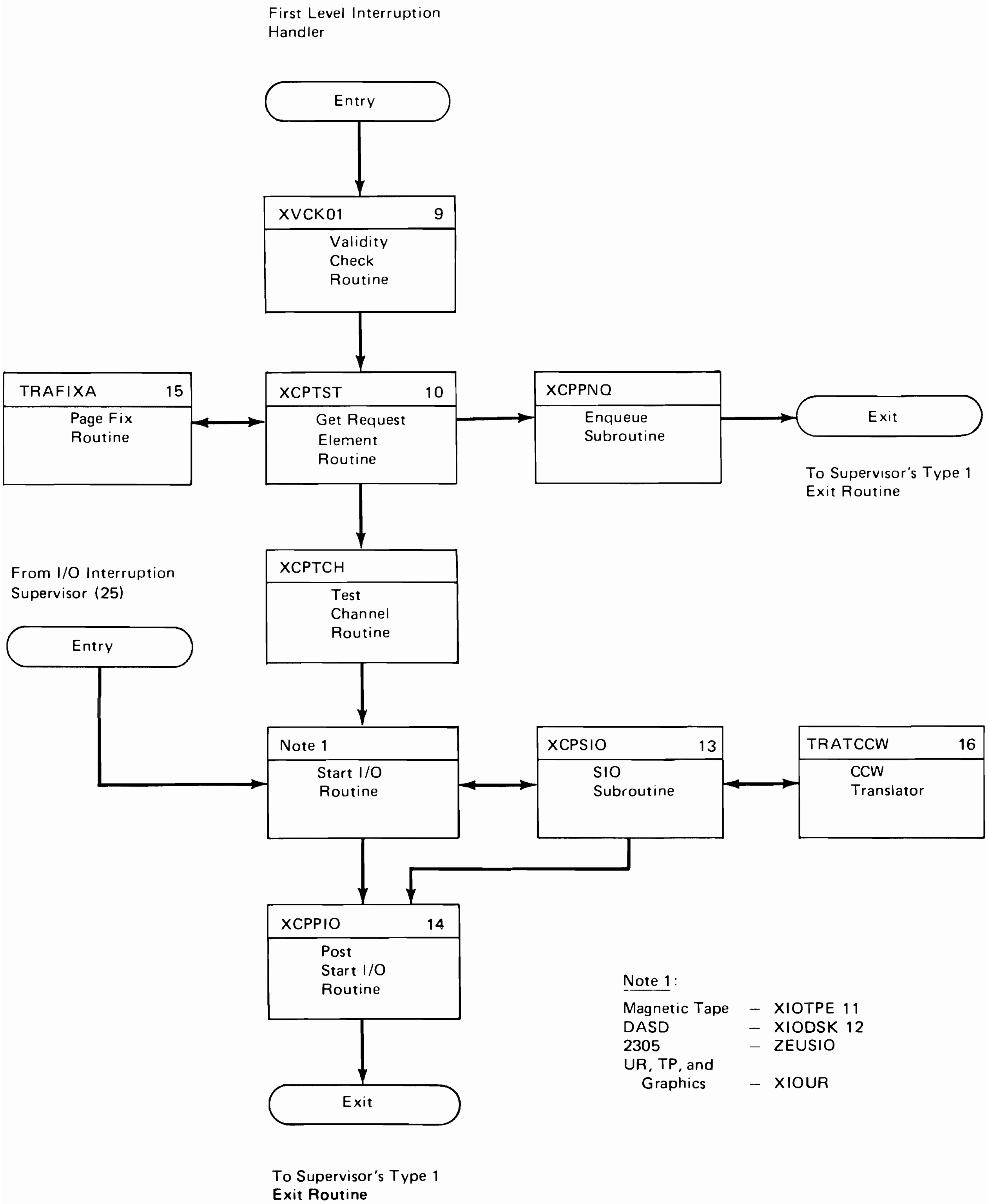
Dequeue subroutine: Locates an RQE in a logical channel queue, removes it from the queue, and returns it to the freelist.

End-of-extent appendage: Optional user-written appendage to which the EXCP supervisor exits when the execution of I/O request will violate the extent limits of a direct-access device.

Enqueue subroutine: Places an RQE into a logical channel queue. Normally queues by order of arrival. Optionally queues by requestor's priority or by seek address.

Error Recovery routine: Determines if I/O activity can be retried. Supervises retry attempts.

Error Routine Interface: Prepares for and invokes, or schedules the execution of, an error recovery routine.



Note 1:

Magnetic Tape	–	XIOTPE 11
DASD	–	XIODSK 12
2305	–	ZEUSIO
UR, TP, and Graphics	–	XIOUR

Figure 24. Functional Organization, EXCP Supervisor

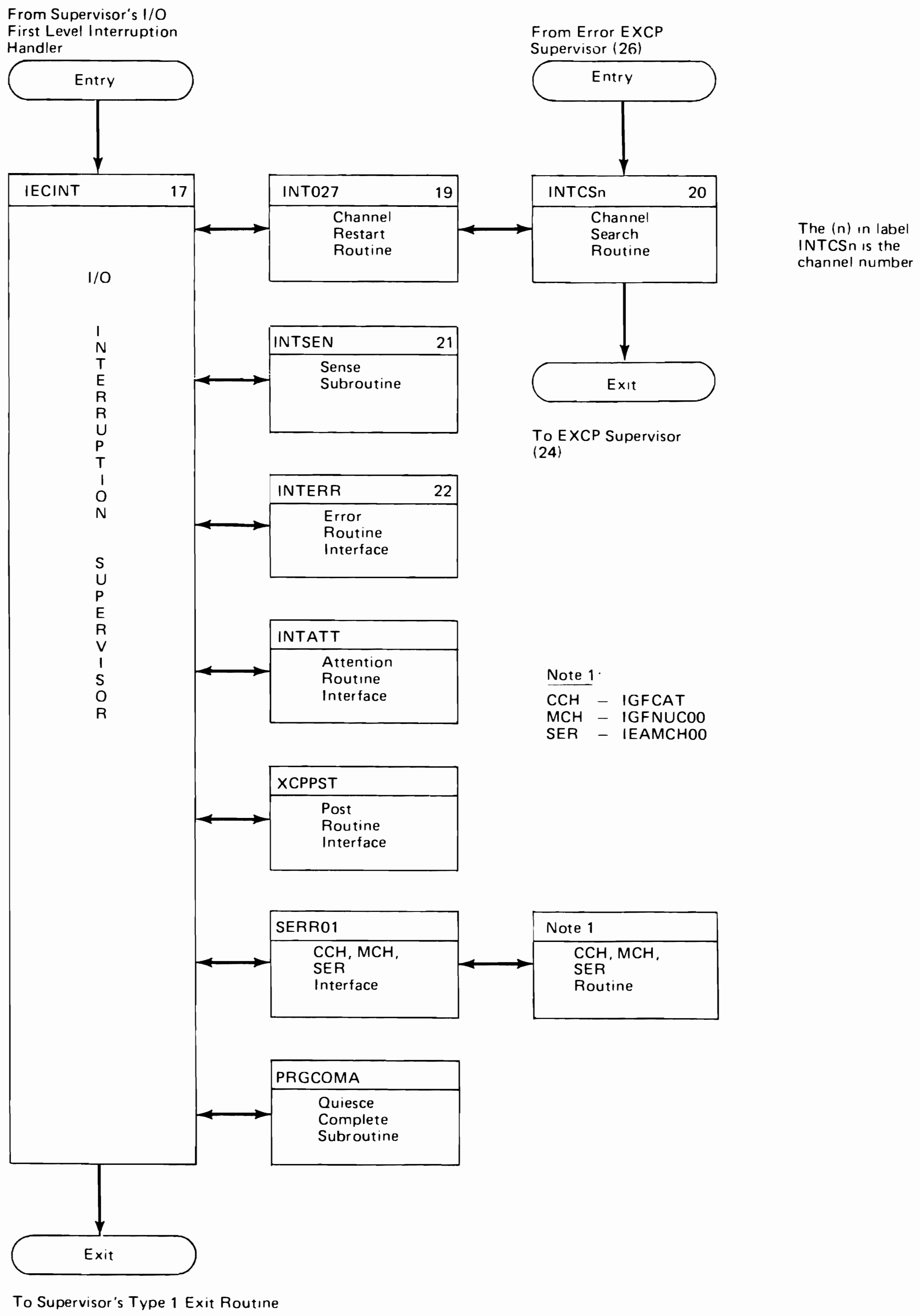
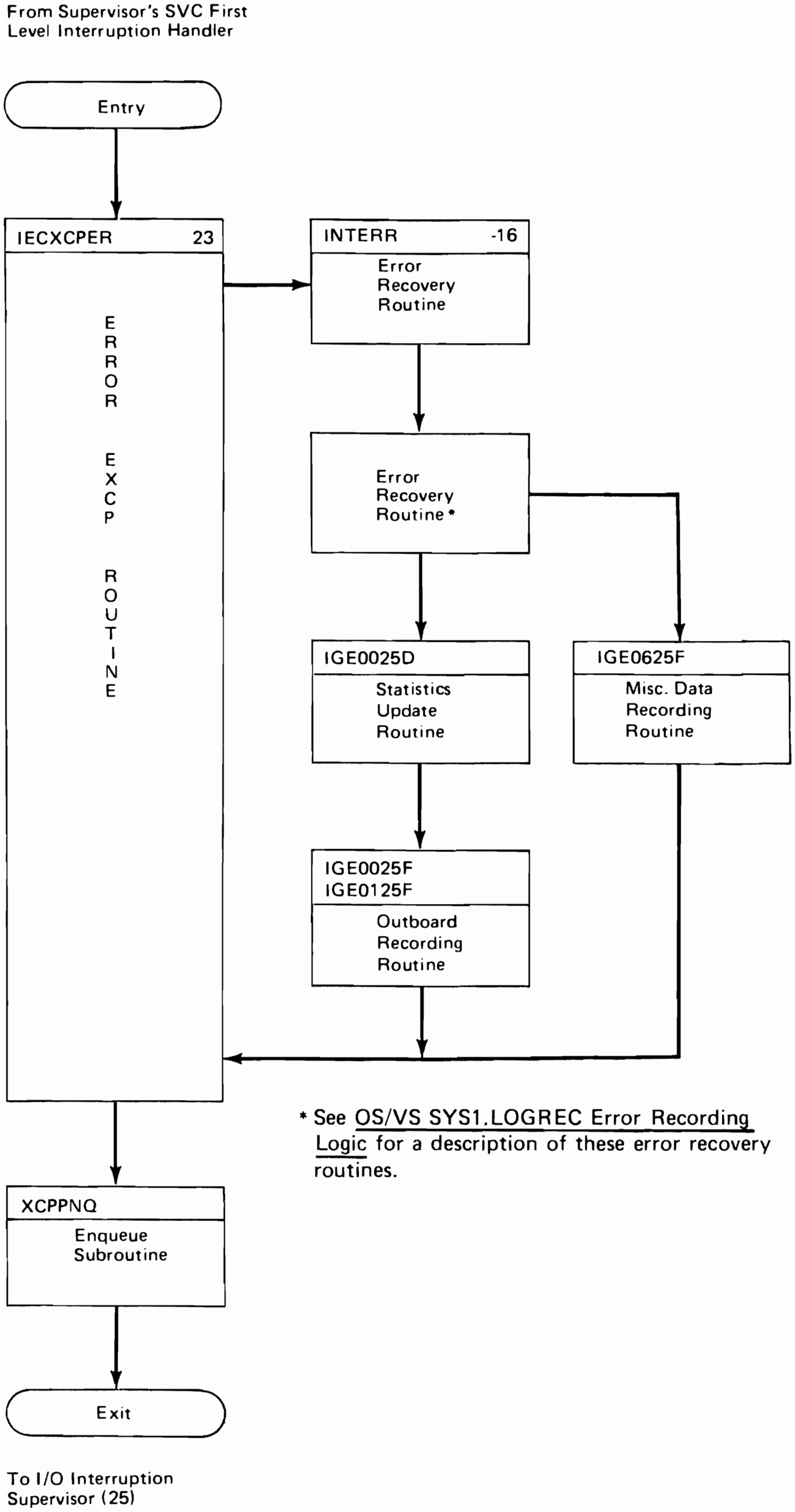


Figure 25. Functional Organization, I/O Interruption Supervisor


From Supervisor's SVC First Level Interruption Handler
Entry
IECXCPER 23
ERROR EXCP ROUTINE
INTERR -16
Error Recovery Routine
Error Recovery Routine *
IGE0025D
Statistics Update Routine
IGE0625F
Misc. Data Recording Routine
IGE0025F
IGE0125F
Outboard Recording Routine
XCPPNQ
Enqueue Subroutine
Exit
To I/O Interruption Supervisor (25)

* See OS/VS SYS1.LOGREC Error Recording Logic for a description of these error recovery routines.

Figure 26. Functional Organization, Error EXCP Supervisor

EXCP Validity Check routine: Does most of the housekeeping for the EXCP supervisor. Checks for a valid DCB, DEB, IOB, and UCB. With Protection feature uses Validity Check subroutine to check storage keys of input data areas.

Get Request Element routine: Obtains an RQE from the freelist and initializes it. If device is unavailable, causes the RQE to be queued in logical channel request queue.

Page Fix Routine: Fixes pages in real storage for control blocks and appendages.

Program-controlled interrupt appendage: Optional user-written appendage to which I/O interruption supervisor exits when program-controlled interruption (PCI) is indicated. Returns control to I/O interruption supervisor where the modified CCW is translated, if a virtual request and normal processing continues.

Post Routine Interface: Invokes the supervisor's Post routine, passing to it an event completion code and the address of the requester's ECB. The Post routine posts the requester's ECB.

Post Start I/O routine: Routes control, depending upon resulting condition codes of the Start I/O instruction and status bits in the CSW (if the CSW was stored).

Quiesce Complete subroutine: Invokes the supervisor's Post routine, passing to it an event completion code and the address of the purge parameter list. The Post routine posts the Purge routine ECB.

Sense subroutine: Issues a Start I/O instruction to cause a Sense command to be executed. Places the first two bytes of sense data in the requester's IOB.

System Environment Recording Routine Interface: Places an error code into the machine check new PSW. Uses a Load PSW instruction to invoke the SER0 or SER1 routine.

Start I/O appendage: Optional user-written routine to which the EXCP supervisor exits before the execution of the Start I/O (SIO) instruction for a requested I/O operation.

Start I/O routine for direct-access devices: Prepares an I/O supervisor channel program consisting of three CCWs: a Seek command, a Set File Mask command, and a Transfer-in-Channel command. The 2314 direct-access device uses the Start I/O subroutine twice, once to perform a stand-alone seek and once to perform the data transfer.

Start I/O routine for magnetic-tape devices: Prepares an I/O supervisor channel program that may consist of two CCWs (normal start, restart, or opposite direction recovery), or three CCWs (operations following a cyclic redundancy check condition). The last CCW contains a Transfer-in-Channel command containing the address of the requester's first CCW. Uses the Start I/O subroutine.

Start I/O routine for unit record and communications devices: Initializes a register with the address of the requester's first CCW. Uses the Start I/O subroutine.

Start I/O subroutine: Prepares the CAW and issues a Start I/O instruction. Does some checking of resulting condition codes.

Test Channel routine: For selector channels, issues a Test Channel instruction. Causes the RQE to be queued if the channel is unavailable. Tries all channels of multiple-path arrangements. Does not issue a Test Channel instruction for byte-multiplexor channels.

Trap routines: One for each device class. Perform device-dependent functions following channel-end and device-end interruptions.

Validity Check subroutine: Checks storage keys of areas containing IOB, DCB, and ECB against the requester's protection key; checks that DEB storage key is 0.

DIRECTORIES

This section contains cross-reference lists that include a data area directory, module directory and a routine directory.

Data Area Directory

Figure 27 contains a summary of information about the major data areas used by the I/O supervisor. The column headings and their meanings are:

Data Area Name: The name of the data area and its abbreviation, if there is one.

Beginning Symbol: Meaningful only for data areas contained in the nucleus. This symbol identifies the beginning of the data area, and can be used to locate the data area in the program listings.

Creation: Contains some indication as to the origin of the data area.

> Permanent Storage Assignment means that the area is part of the hardware and always occupies the real-storage location shown in the "Storage Area" column.
>
> Requester means that creation and maintenance of the data area is the responsibility of the requester of the I/O activity. All requesters do not have to explicitly create the needed data areas. (See Figure 1 and its accompanying text.)
>
> System Generation means that the data area is created during system generation. (This means that space is set aside for the area during system generation.)
>
> Supervisor means that the area is created and maintained by the supervisor portion of the control program.

Storage Area: Indicates where the data area can be found in real storage. Where "Requester's" appears in this column, the data area is obtained by the requester when it is needed; consequently, its location is not fixed.

Size: The size of the data area.

Means of Access: The most commonly used way of referring to the data area or one of its entries.

Data Area Name	Beginning Symbol	Creation	Storage Area	Size	Means of Access
Alternate Path Table	SCPCHnB	System Generation	Nucleus	Three to Five Fullwords, Depending Upon No. of Paths to a Device	Beginning symbol.
Beginning-End Block (BEBLK)	BEBNXTB	I/O Supervisor	SQA	136 Bytes	TSTHDR field of the RQE.
Channel Address Word (CAW)	CAWLOC	Permanent Storage Assignment	72(48)	Word	Beginning symbol.
Channel Command Word (CCW)		By Requester when Needed. IOS CCWs are Created during System Generation	Requester's Nucleus	Doubleword	Address at requester's first CCW is contained at off-sets IOBST (start) or IOBSRS (restart) fields of IOB. Access to IOS CCWs varies with device type and circumstances.
Channel Error Block Table	CEBTAB	System Generation	Nucleus	24 Bytes	Beginning Symbol.
Channel Status Word (CSW)	CSWLOC	Permanent Storage Assignment	64(40)	Doubleword	Beginning symbol.
Channel Table	IECCST	System Generation	Nucleus	One-Word Entry for Each Physical Channel	To locate entry for specific channel, channel number is multiplied by four and added to beginning address of table.
Data Control Block (DCB)		By Requester	Requester's	Varies with Access Method	Symbolic names equated to offsets of files.
Data Extent Block (DEB)		By Requester	Requester's	Varies with Devices and Access method	Symbolic names equated to offsets of fields.
Device Statistics Table	IECSTB	System Generation	Nucleus	One 10-Byte Entry for Each Device, plus One 10 Byte Control Field	Normally, the address of an entry for a device is obtained by multiplying the statistics table index in the device's UCB by 10 and adding the result to the beginning address of the device statistics table: STATAB x 10 + Beginning Address When there are more than 256 devices, however, the following method is used: (STATAB) + 256) x 10 + Beginning Address

Figure 27. (Part 1 of 3) Data Area Directory

Data Area Name	Beginning Symbol	Creation	Storage Area	Size	Means of Access
					In the above, n is the number one or two to indicate the second and third 256-entry group in the device statistics table. The UCB addresses in the control field of the table are used to determine the number n. For the 2314 Direct-Access Storage Facility, the low-order four bits of the fifth sense byte are added to the statistics table index before the index is used.
Device Table	DEVTAB	System Generation	Nucleus	One 6-Byte Entry for Each Queuing Option Selected for Each Device Type	Desired entry located by adding device table index from UCB to beginning address of table. A specific field within the entry is then located by adding the field's offset to the above sum.
Event Control Block (ECB)		By Requester	Requester's	Word	Via address contained at offset 5 of the IOB.
Indirect Address List (IAL)	IALCHAIN	I/O Supervisor	SQA	136 Bytes	HDRINDL field of the CCW translation header BEBLK.
Input/Output Block (IOB)		By Requester	Requester's	32 Bytes, plus a Variable Amount that Depends Upon the Access Method	Initially, address is provided in register 1 by requester. It is moved to and maintained in register 2 (IOBREG).
Logical Channel Table (LCH)	LCHTAB IECILCH	System Generation	Nucleus	One Doubleword Logical Channel Word for Each Logical	To locate a needed logical channel word, the logical channel index in the UCB is multiplied by 8 and added to the beginning address of the logical channel table.
Page Fix List (PGFX)	FXLSTCHN	I/O Supervisor	SQA	136 Bytes	Before CCW translation, the TSTHDR field of RQE. HDRPGLK field of the translation header BEBLK.
Program Status Word (PSW)		Permanent Storage Assignment			
SVC Old PSW	SVCOPSW			32(20)	Beginning symbol.
I/O Old PSW	IOPSWO			56(38)	Beginning symbol.
I/O New PSW	IONPSW			120(78)	Beginning symbol.

Figure 27. (Part 2 of 3) Data Area Directory

Data Area Name	Beginning Symbol	Creation	Storage Area	Size	Means of Access
Request Queue Element (RQE)	TSTAR TECIOQET	System Generation	Nucleus	20 Bytes 20 Bytes	Varies depending upon status of request: Address of RQE available for assignment is contained in location NEXAVL. Address of assigned (but not queued) RQE is contained in requester 1 (TSTREG). Address of the first RQE in a logical channel queue is contained in the LCHFTS field of the logical channel word for that queue.
Task Control Block (TCB)		By Supervisor	Nucleus	171 Bytes	Symbolic names equated to offsets of fields.
Translation Header BEBLK	BEBNXTB	I/O Supervisor	SQA	136 Bytes	TSTHDR field of the RQE.
Unit Control Block (UCB)		System Generation	Nucleus	Variable from 24 10 288 Bytes. one UCB for Each Device Address Defined for the System.	Initially, via address contained in the UCB address field of DEB. The address is moved to the request queue element. Following interruptions, the address of the UCB for the device that caused the interruption is obtained via the UCB lookup table.
UCB Lookup Table	UCGTAB IECILKI	System Generation	Nucleus	Variable, depending upon Number and Addresses of Devices, Control Units, and Channels, and Number of Zero Entries Eliminated by Table-Building Routine.	Beginning symbol.
Volume Statistics Table		System	Nucleus	24 Bytes for Each Entry	Via address contained in field at offset 49 of the UCB containing the volume. Each entry is effectively an extension to a UCB.

Figure 27. (Part 3 of 3) Data Area Directory

Module Directory

Figure 28 contains information about the physical structure of the I/O supervisor. The column headings and their meanings are:

Symbolic Name: The symbolic name of a table, routine, object module, or control section.

Description: The type of item to which the symbolic name applies.

Object Module Name: The name of the object module containing the item. The microfiche cards containing program listings are ordered by object module name.

Control Section Name: The name of the control section containing the item.

Publication References: Places in this publication where more information about the item can be found.

Library: The data set normally containing the item.

Code	Data Set
NUC	SYS1.NUCLEUS
SVC	SYS1.LPALIB

If SVC Routine: Information about I/O supervisor SVC routines. There are four types of SVC routines.

Type 1 SVC routines are part of the nucleus and are disabled (masked) for all interruptions except machine check interruptions.

Type 2 SVC routines are part of the nucleus but may be enabled (interruptable) for part of their operation.

Type 3 SVC routines are nonresident and may be enabled.

Type 4 SVC routines are nonresident and may be enabled.

Name: The name of the item being described.

When the control section name for an item is not the same as the object module name, the item will have two entries in the table—one filed by control section name and the other filed by object module name. Therefore, it is unnecessary to check beyond the first column when looking for a symbolic name.

The three major groups of routines that make up the I/O supervisor—the EXCP supervisor, the I/O interruption supervisor, and the error EXCP supervisor—are contained in the control program nucleus. As a result, there are no CSECT names or load module names in these three major groups of routines. Linkage parameter lists, usually associated with multi-load routines, are also unnecessary. Therefore entry points are not of the formal one-or-two-entries-only type (due to stringent parameter list requirements), but rather are ordinary symbolic labels, undistinguishable from other symbolic labels.

									If SVC Routine
		Object	**Control**				**Macro**		
Symbolic		**Module**	**Section**	**Publication**			**Instruc-**	**SVC**	
Name	**Description**	**Name**	**Name**	**Reference**	**Library**	**Type**	**tion**	**No.**	**Name**
CAWLOC	Table	*	*	Data Areas					Channel Address Word
CSWLOC	Table	*	*	Data Areas					Channel Status Word
DEVTAB	Table	*	*	Data Areas	NUC				Device Table
IEAQFX00	Object Module	IEAQFX00	IEAQFX00	All	NUC				IOS Nucleus
IECCST	Table	*	*	Data Areas	NUC				Channel Table
IECILCH	Table	*	*	Data Areas	NUC				Logical Channel Table
IECILK1	Table	*	*	Data Areas	NUC				UCB Lookup Table
IECINT	Routine	*	*	Program Organization	NUC				I/O Interruption Supervisor
IECINTRP	Object Module	IECINTRP	IECINTRP	Method of Operation	NUC				Error Interpreter Routine
IECIOQET	Table	*	*	Data Areas	NUC				Request Queue Element Table
IECIPRTS	Object Module	IECIPRTS	IGC016	Appendix A	SVC	2	PURGE	16	Purge Routine (TSO)
IECIPR16	Object Module	IECIPR16	IGC016	Appendix A	SVC	2	PURGE	16	Purge Routine
IECSTB	Table	*	*	Data Areas	NUC				Statistics Table
IECWTORA	Control Section	IGE0125C	IECWTORA	Appendix H	SVC				Write-to-Operator Routine, Load 1 of 5[1]
IECWTORB	Control Section	IGE0125C	IECWTORB	Appendix H	SVC				Write-to-Operator Routine, Load 2 of 5[1]
IECWTORC	Control Section	IGE0225C	IECWTORC	Appendix H	SVC				Write-to-Operator Routine, Load 3 of 5[1]
IECWTORD	Control Section	IGE0325C	IECWTORD	Appendix H	SVC				Write-to-Operator Routine, Load 4 of 5[1]
IECWTORE	Control Section	IEC0425C	IECWTORE	Appendix H	SVC				Write-to-Operator Routine, Load 5 of 5[1]
IEC1052A	Control Section	IGE0000D	IEC1052A	Appendix H	SVC				1052, 3210, and 3215 Error Routine
IEC1402A	Control Section	IGE0001C	IEC1402A	Appendix H	SVC				2540 Error Routine, Load 1 of 2
IEC1402B	Control Section	IGE0101C	IEC1402B	Appendix H	SVC				2540 Error Routine, Load 2 of 2
IEC1403A	Control Section	IGE0000G	IEC1403A	Appendix H	SVC				1403 and 1443 Error Routine
IEC1442A	Control Section	IGE0000E	IEC1442A	Appendix H	SVC				2501, 2520, and 1442 Error Routine
IEC23XXF	Object Module	*	*	Appendix H	NUC				2305, 2314, 2319, 3330, and 3333 Error Routine

* Refer to installation system generation listing.

[1] Do not confuse with the Write-to-Operator SVC routine (SVC 35), described in other OS/VS publications.

Figure 28. (Part 1 of 5) Module Directory

									If SVC Routine
		Object	Control				Macro		
Symbolic		Module	Section	Publication			Instruc-	SVC	
Name	Description	Name	Name	Reference	Library	Type	tion	No.	Name
IEC24001	Control Section	IGE09001	IEC24001	Appendix H	SVC				2400/3400 Tape Series Error Routine, Load 6 of 7
IEC3211A	Control Section	IGE000F	IEC3211A	Appendix H	SVC				3211 Error Routine
IEC3211B	Control Section	IGE0100F	IEC3211B	Appendix H	SVC				3211 Error Routine
IEC3420J	Control Section	IGE08001	IEC3420J	Appendix H	SVC				2400/3400 Tape Series Error Routine, Load 7 of 7
IGC000	Routine	*	*	Method of Operation, Program Organization	NUC	1	EXCP	0	EXCP Supervisor
IGC0001G	Object Module	IGC00001G	SVC017	Appendix A	SVC	3	RESTORE	17	Restore Routine
IGC0003C	Object Module	IGC0003C	IGC00033	Appendix A	SVC	3	IOHALT	33	IOHALT Routine
IGC00033	Control Section	IGC0003C	IGC00033	Appendix A	SVC	3	IOHALT	33	IOHALT Routine
IGC0009A	Object Module	IGC0009A	IGC0009A	Appendix A	SVC	3	-none-	91	VOLSTAT Routine
IGC0010A	Object Module	IGC0010A	IGC0010A	Appendix H	SVC				Loads 2305/3330/3333
IGC0024	Control Section	IGC0002D	IGC0024	Appendix A	SVC	3	DEVTYPE	24	DEVTYPE Routine
IGC015	Routine	*	*	Method of Operation, Program Organization	NUC	1	-none-	15	Error EXCP Supervisor
IEC016	Control Section	IECIPRTS	IGC016	Appendix A	SVC	2	PURGE	16	Purge Routine (TSO)
IGC016	Control Section	IECIPR16	IGC016	Appendix A	SVC	2	PURGE	16	Purge Routine
IGC092	Routine	*	*	Appendix A	NUC	1	-none-	92	TCB EXCP Routine (TSO)
IGE0000D	Object Module	IGE0000D	IEC1052A	Appendix H	SVC				1052, 3210, and 3215 Error Routine
IGE0000E	Object Module	IGE0000E	IEC1442A	Appendix H	SVC				2501 and 2520 Routine
IGE0000F	Object Module	IGE0000F	IEC3211A	Appendix H	SVC				3211 Error Routine
IGE0000G	Object Module	IGE0000G	IEC1403A	Appendix H	SVC				1403 and 1443 Error Routine

* Refer to installation system generation listing.

Figure 28. (Part 2 of 5) Module Directory

								If SVC Routine
Symbolic Name	Description	Object Module Name	Control Section Name	Publication Reference	Library Type	Macro Instruction	SVC No.	Name
IGE00001	Object Module	IGE00001	IGE00001	Appendix H	SVC			2400/3400 Tape Series Error Routine, Load 1 of 7
IGE0001C	Object Module	IGE0001C	IEC1402A	Appendix H	SVC			2540 Error Routine, Load 1 of 2
IGE0010A	Object Module	IGE0010A	IGE0010A	Appendix H	SVC			2250 Error Routine
IGE0010B	Object Module	IGE0010B	IGE0010B	Appendix H	SVC			2260 and 1053 Error Routine, Load 1 of 2
IGE0011A	Object Module	IGE0011A	IGE0011A	Appendix H	SVC			2495 Error Routine
IGE0011C	Object Module	IGE0011C	IGE0011C	Appendix H	SVC			1287 Error Routine
IGE0011D	Object Module	IGE0011D	IGE0011D	Appendix H	SVC			1288 Error Routine
IGE0011E	Object Module	IGE0011E	IGE0011E	Appendix H	SVC			1419/1275 Error Routine
IGE0025C	Object Module	IGE0025C	IECWTORA	Appendix H	SVC			Write-to-Operator Routine, Load 1 of 5[1]
IGE0025E	Object Module	IGE0025E	IGE0025E	Appendix A	SVC			I/O Purge Routine
IGE0100F	Object Module	IGE0100F	IEC3211B	Appendix H	SVC			3211 Error Routine, Load 2 of 2
IGE01001	Object Module	IGE0100I	IGE0100I	Appendix H	SVC			2400/3400 Tape Series Error Routine, Load 2 of 7
IGE0101C	Object Module	IGE0101C	IEC1402B	Appendix H	SVC			2540 Error Routine, Load 2 of 2
IGE0110B	Object Module	IGE0110B	IGE0110B	Appendix H	SVC			2260 and 1053 Error Routine, Load 2 of 2
IGE0125C	Object Module	IGE0125C	IECWTORB	Appendix H	SVC			Write-to-Operator Routine, Load 2 of 5[1]
IGE0125E	Object Module	IGE0125E	IGE0125E	Appendix C	SVC			Volume Verification Routine, Load 1 of 2
IGE02001	Object Module	IGE02001	IGE02001	Appendix H	SVC			2400/3400 Tape Series Error Routine, Load 3 of 7
IGE0225C	Object Module	IGE0225C	IECWTORC	Appendix H	SVC			Write-to-Operator Routine, Load 3 of 5[1]
IGE0225E	Object Module	IGE0225E	IGE0225E	Appendix C	SVC			Volume Verification Routine Load 2 of 2
IGE03001	Object Module	IGE03001	IGE03001	Appendix H	SVC			2400/3400 Tape Series Error Routine, Load 4 of 7

[1] Do not confuse with the Write-to-Operator SVC routine (SVC 35), described in other OS/VS publications.

Figure 28. (Part 3 of 5) Module Directory

Symbolic Name	Description	Object Module Name	Control Section Name	Publication Reference	Library Type	Macro Instruction	SVC No.	If SVC Routine Name
IGE0325C	Control Section	IGE0325C	IECWTORD	Appendix H	SVC			Write-to-Operator Routine, Load 4 of 5[1]
IGE04001	Object Module	IGE04001	IGE04001	Appendix H	SVC			2400/3400 Tape Series Error Routine, Load 5 of 7
IGE0425C	Control Section	IGE0425C	IECWTORE	Appendix H	SVC			Write-to-Operator Routine, Load 5 of 5[1]
IGE0425F	Object Module	IGE0425F	IGE0425F	Program Organization	SVC			System Environment Recording Message Routine
IGE0800I	Object Module	IGE0800I	IEC3420J	Appendix H	SVC			2400/3400 Tape Series Error Routine, Load 7 of 7
IGE09001	Object Module	IGE09001	IEC24001	Appendix H	SVC			2400/3400 Tape Series Error Routine, Load 6 of 7
IGFCAT	Routine	*	IGFCAT	Program Organization	NUC			Channel Check Handler Routine
IGX00015	Object Module	IGX00015	IGX00015	Appendix A	SVC			Extended SVC Routine
INTAPR01	Routine	*	*	Appendix B	NUC			Alternate Path Retry Routine
INTATT	Routine	*	*	Program Organization	NUC			Attention Routine Interface
INTCS	Routine	*	*	Program Organization	NUC			Channel Search Routine
INTDAT	Routine	*	*	Program Organization	NUC			Trap Routine for Direct-Access Devices
INTERR	Routine	*	*	Program Organization	NUC			Error Routine Interface
INTSEN	Routine	*	*	Program Organization	NUC			Sense Subroutine
INTTAT	Routine	*	*	Program Organization	NUC			Trap Routine for Magnetic Tape Devices
INTURT	Routine	*	*	Program Organization	NUC			Trap Routine for Unit Record and Communications Devices
INT027	Routine	*	*	Program Organization	NUC			Channel Restart Routine
IONPSW	Table	*	*	Data Areas				I/O New PSW
IOPSWO	Table	*	*	Data Areas				I/O Old PSW
PRGCOMA	Routine	*	*	Program Organization	NUC			Quiesce Complete Subroutine

* Refer to installation system generation listing.

[1] Do not confuse with the Write-To-Operator SVC routine (SVC35 described in the other OS/VS publications.

Figure 28. (Part 4 of 5) Module Directory

Symbolic Name	Description	Object Module Name	Control Section Name	Publication Reference	Library	Type	Macro Instruction	SVC No.	If SVC Routine Name
SERR01	Routine	*	*	Program Organization	NUC				SER CCH/MCH Routine Interface
SVCOPSW	Table	*	*	Data Areas					SVC Old PSW
SVC017	Control Section	IGC0001G	SVC017	Appendix A	SVC	3	RESTORE	17	Restore Routine
TSTAR	Table	*	*	Data Areas	NUC				Request Queue Element Table
VALCHK	Routine	*	*	Program Organization	NUC				Validity Check Subroutine
XCPCH	Routine	*	*	Program Organization	NUC				Test Channel Routine
XCPPDQ	Routine	*	*	Program Organization	NUC				Dequeue Subroutine
XCPPIO	Routine	*	*	Program Organization	NUC				Post Start I/O Routine
XCPPNQ	Routine	*	*	Program Organization	NUC				Enqueue Subroutine
XCPPST	Routine	*	*	Program Organization	NUC				Post Routine Interface
XCPSIO	Routine	*	*	Method of Operation	NUC				Start I/O Subroutine
XCPTST	Routine	*	*	Method of Operation	NUC				Get Request Element Routine
XIODSKI	Routine	*	*	Method of Operation	NUC				Start I/O Routine for Direct-Access Devices
XIOTPE	Routine	*	*	Method of Operation	NUC				Start I/O Routine for Magnetic Tape Devices
XIOUR	Routine	*	*	Method of Operation	NUC				Start I/O Routine for Unit Record and Communications Devices
XVCK01	Routine	*	*	Method of Operation	NUC				EXCP Validity Check Routine

* Refer to installation system generation listing.

Figure 28. (Part 5 of 5) Module Directory

Routine Directory

Figure 29 lists the routines that make up the I/O supervisor's nucleus. The routines are listed alphabetically by name with their entry point and reference.

Routine Name	Entry Point	Method of Operation Figure	Program Operation Figure
ABTERM interface	XERX04	....	....
Alternate Path Retry	INTAPR01	....	....
Attention Routine Interface	INTATT	....	25
CCW Translator	TRATCCW	16	24
Channel Check Handler	IGFCAT	....	25
Channel Check Handler Interface	SERR01	....	25
Channel Restart	INT027	19	25
Channel Search	INTCSn	20	25
CSW Translate	TRATCSW	....	
DAVV Attention	INTATN	....	....
DDR Appendage Support Interface	DDRAPNVT	....	....
DEB Validity Check	DEBVAL	9	....
Dequeue	XCPPDQ	....	....
Direct Access Extent Test	EXTTST	....	....
Direct Access Trap	INTDAT	....	....
Enqueue Subroutine	XCPPNQ		24,26
Error EXCP	IECXCPER	23	26
Error Recovery Routine			26
Error Routine Interface	INTERR	22	25,26
EXCP Supervisor	XEXCP	8	....
FIFO Enqueue	XCPENQ	....	....
Get Request Element	XCPTST	10	....
HIO	IECIHIO	....	....
I/O Interruption Supervisor	IECINT	17	....
Inline Fix/Unfix Subroutine	ILFXS100	....	....
Local GETMAIN Subroutine	GTFRM000	....	....
Machine Check Handler	IGFNUC00	....	25
Machine Check Handler Interface	IERR01	....	25
Ordered Seek Enqueue	XCPSEQ	....	25
Page Exception Handler	IECXPGEY	....	....
Page Fix	TRAFIXA	15	24
Page-Fix Appendage Interface	PGFXINT	....	....
Post Routine Interface	XCPPST	....	25
Post Start I/O	XCPPIO	14	24
Priority Enqueue	XCPPRQ	....	....
Program Check Recovery	IECCPL00	....	....

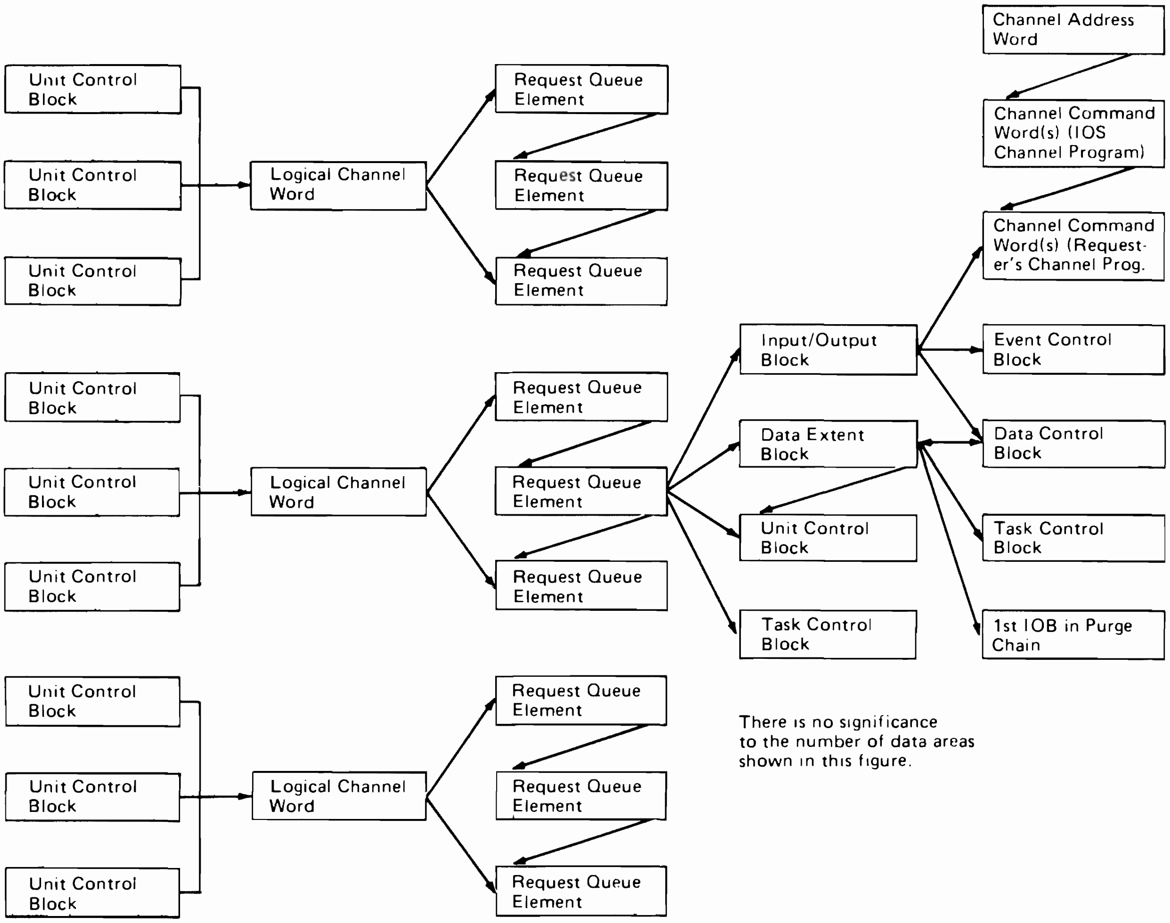
Figure 29. (Part 1 of 2) Routine Directory

Routine Name	Entry Point	Method of Operation Figure	Program Operation Figure
Quiesce Complete Subroutine	PRGCOMA	....	25
RMS Channel Restart Interface	INTRMS	....	....
RMS Module Loader Interface	IECRMS	....	....
Sense Subroutine	INTSEN	21	25
Service Interface Routine	IEASIRBE	....	....
SIO Subroutine	XCPSIO	13	24
Start I/O Routine for DASD	XIODSK	12	24
Start I/O Routine for Tape	XIOTPE	11	24
Start I/O Routine for UR and TP	XIOUR	....	24
Start I/O Routine for 2305	XEUSIO	....	24
System Environment Recording	IEAMCH00	....	25
System Environment Recording Interface	SERR01	....	25
Test Channel	XCPTCH	....	24
TSO TCB EXCP Interface	IECXPT	....	....
Unfix/Freemain	TRAUFRE	....	....
Unit Record Trap	INTURT	....	....
Validity Check	XVCK01	9	24

Figure 29. (Part 2 of 2) Routine Directory

DATA AREAS

The major paths by which I/O supervisor routines can reach specific data areas are shown in Figure 30. The longer paths are seldom used, because pointers to major data areas are normally maintained in registers. For example IOBREG, which is register 2, will normally contain the address of the IOB for a request in process. One exception is the Purge routine, which must use the longer paths in locating and removing elements from queues.



There is no significance to the number of data areas shown in this figure.

Data Area Name	Offset	Field Name	Content
Data Extent Block	1(1)	DEBTCBAD	Task Control Block
	17(11)	DEBUSRPG	First IOB in Purge Chain
	25(19)	DEBDCBAD	Data Control Block
	33(21)	DEBUCBAD	Unit Control Block
Input/Output Block	5(5)	IOBECB	Event Control Block
	17(11)	IOBST	Requester's Channel Program
	21(15)	IOBDCB	Data Control Block
Logical Channel Word	0(0)	LCHFTS	First RQE in Logical Channel Queue
	2(2)	LCHLTS	Last RQE in Logical Channel Queue
Request Queue Element	0(0)	TSTLNK	Next RQE in Logical Channel Queue
	2(2)	TSTUCB	Unit Control Block
	5(5)	TSTIOB	Input/Output Block
	9(9)	TSTDEB	Data Extent Block
	12(0C)	TSTKEY	Protect Key
	13(0D)	TSTTCBAD	Task Control Block
	16(10)	TSTHDR	**Page-fix list before translation. Translation Header BEBLK during and after translation.**
Unit Control Block	10(A)	UCBLCI	Value which, when multiplied by 8, becomes an index to the logical channel word for the logical channel containing device.

Figure 30. Data Area Relationships

Data Area Layouts

This section contains descriptions of the principle data areas used by routines of the I/O supervisor. Refer to *OS/VS2 System Data Areas* for data areas that are common to other VS functions.

The symbolic names shown in individual data area fields represent the offset, in bytes, from the beginning of a table to the field. Access is gained to a specific field by using an instruction in which the beginning address of the table (usually contained in a register) is the base address, and the symbolic field name represents the displacement.

Usage of the data area fields can be traced in the I/O supervisor listings by first locating the symbolic field names in the cross-reference table at the back of the listings and then noting where the names are used. Where no symbolic name appears in a data area field, the field is not referred to by the I/O supervisor.

Alternate Path Table

The alternate path table (Figure 31) contains a record of the paths by which a device can be reached. There is one alternate path table for each logical channel that contains more than one channel. In the listings, an alternate path table immediately precedes the Test Channel routine for its associated channel.

Channel Address	Path Number	Two to Four Fullword Entries, Depending Upon Number of Alternate Paths.
" "	" "	
" "	" "	
" "	" "	
No. of Paths	Sum of Path Numbers	Control Entry.

Figure 31. Alternate Path Table

Appendage Vector Table

The Appendage Vector Table (AVT, Figure 32) contains the virtual address of each I/O appendage and the number of pages that must be fixed for each appendage. The first byte of each 4-byte field contains the number of pages to be fixed for the appendage whose virtual address is in the remaining three bytes of the field.

Dec	Hex		
0	0	APGEOE	End of Extent (EOE)
4	4	APGSIO	Start I/O (SIO) and Page-Fix Appendage. See Note.
8	8	APGPCI	Program Controlled Interrupt (PCI)
12	0C	APGCHE	Channel End (CE)
16	10	APGABE	Abnormal End (XCE)

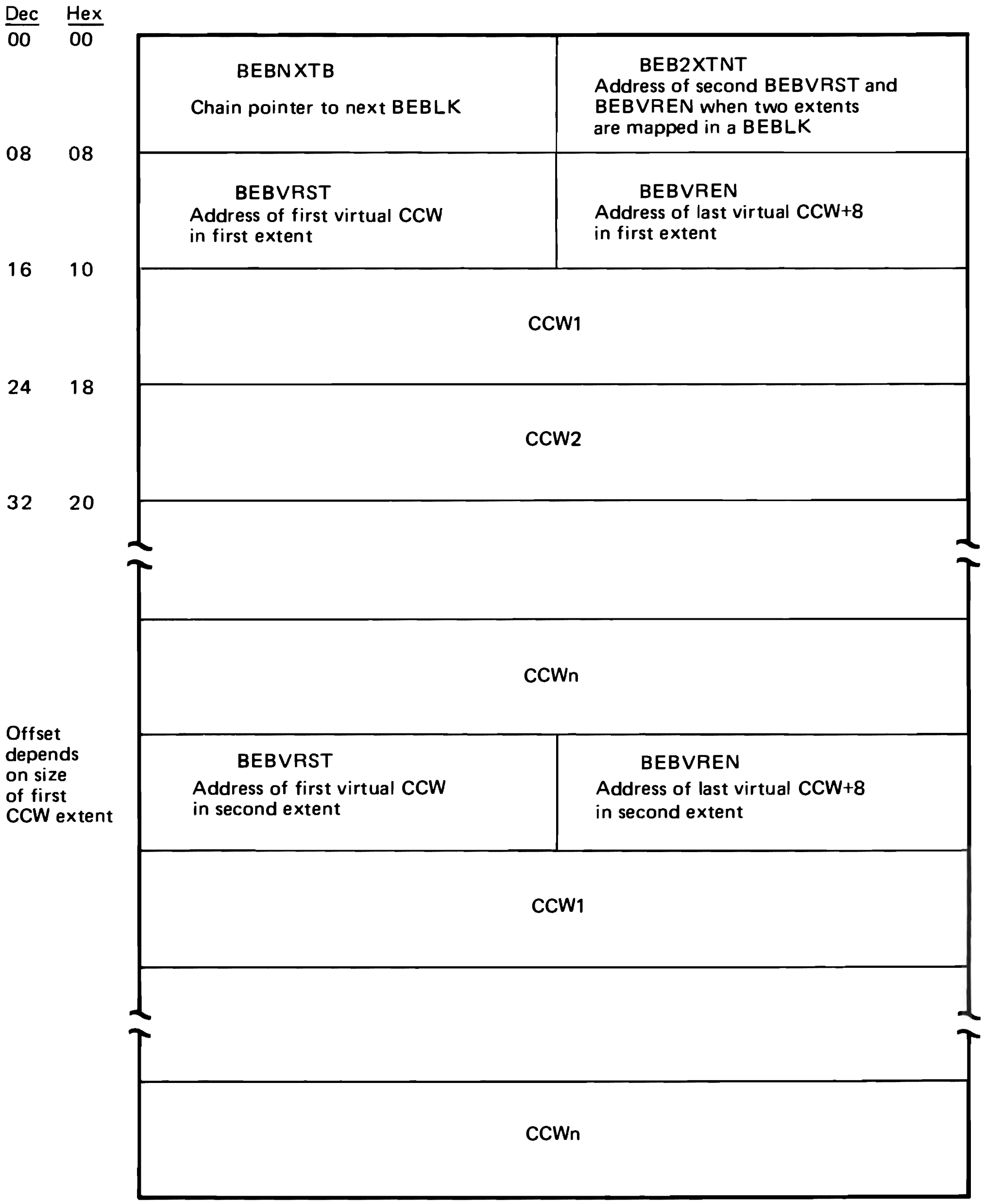
Note: If bit 0 of byte 4 is set to 1, the SIO appendage contains the page fix (PGFX) appendage. If bit 1 of byte 4 is set to 1, the SIO appendage is entered even if ERP is active.

Field	Dec	Hex	Field	Dec	Hex
APGABE	0016	0010	CE	0013	000D
APGCHE	0012	000C	EOE	0001	0001
APGEOE	0000	0000	PCI	0009	0009
APGPCI	0008	0008	SIO	0005	0005
APGSIO	0004	0004	XCE	0017	0011

Figure 32. Appendage Vector Table

BEBLK (Beginning-End Block)

A beginning-end block (BEBLK, Figure 33) contains the real copy of the CCWs and the beginning and ending addresses of the user's virtual CCWs, of which these CCWs are the equivalent. A BEBLK can map up to 15 contiguous CCWs. If two CCW extents are mapped, then up to 14 CCWs and a second set of beginning and ending addresses of the user's virtual CCWs are contained in the BEBLK. The second extent information is located directly after the last CCW required for the first range.


Dec Hex
00 00
08 08
16 10
24 18
32 20
Offset depends on size of first CCW extent
BEBNXTB
Chain pointer to next BEBLK
BEB2XTNT
Address of second BEBVRST and BEBVREN when two extents are mapped in a BEBLK
BEBVRST
Address of first virtual CCW in first extent
BEBVREN
Address of last virtual CCW+8 in first extent
CCW1
CCW2
CCWn
BEBVRST
Address of first virtual CCW in second extent
BEBVREN
Address of last virtual CCW+8 in second extent
CCW1
CCWn

Field	Dec	Hex	Field	Dec	Hex
BEBNXTB	00	00	BEBVREN	12	0C
BEB2XTNT	04	04	CCW1	16	10
BEBVRST	08	08	CCW2	24	18

Figure 33. Beginning-End Block

Channel Address Word

A channel refers to the Channel Address Word (CAW, Figure 34) during execution of a start I/O instruction. It provides the channel with a means of determining the real storage location from which it should fetch the first CCW. The CAW is permanently assigned to real storage location 72.

Dec	Hex		
0	0	CAWLOC Protection Key	Address of CCW

Field	Dec	Hex
CAWLOC	0000	0000
CCW Address	0001	0001

Figure 34. Channel Address Word

Channel Command Word

The Channel Command Word (CCW, Figure 35) indicates to a channel what I/O operation should be started. For operations involving data transfer, the CCW also indicates the real storage location into which data is to be placed or read from, and how many bytes of data are to be transferred.

Command Code	Data Address	Flags*	0 0 0	▨	Count
0 7	8 31	32 36	37 39	40 47	48 63

*Flags and Masks

Flag Field	Contains	Hex	Means
Flags	Chain-data (CD) flag	X'80'	The data area designated by the next CCW to be used with current operation.
	Chain-command (CC) flag	X'40'	The operation specified by the command code of the next CCW is to be initiated on normal completion of the current operation.
	Suppress-incorrect-length indicator (SILI)	X'20'	The incorrect length status bit in the channel status word is not to be set by the channel if an incorrect length condition is detected.
	Skip flag	X'10'	Data transfer to storage is suppressed. Valid only for read, read backward, and sense operations.
	PCI flag	X'08'	The channel causes an interruption when this CCW is fetched.
	Indirect address flag	X'04'	The channel references the indirect address list at the start of the I/O operation and whenever a 2K boundary is reached during data transfer.

Figure 35. Channel Command Word

CCW Translation Header BEBLK

The CCW translation header BEBLK (Figure 36) contains the addresses of the first and last CCWs in the corresponding virtual channel program. This BEBLK can map up to 12 contiguous CCWs. If two CCW extents are mapped, then up to 11 CCWs and a second set of beginning and ending addresses of the user's virtual CCWs are contained in the header BEBLK. The second extent information is located directly after the last CCW of the first extent. This block also contains pointers required for translation of the entire channel program. Figure 37 shows the interrelationship of the translation control blocks.

Dec	Hex							
00	00	BEBNXTB Chain pointer to next BEBLK	BEB2XTNT Address of BEBVRST and BEBVREN for second CCW extent; otherwise, zero				BEBVRST Address of first virtual CCW in first extent	BEBVREN Address of last virtual CCW+8 in first extent
16	10	CCW1					CCW2	
		CCWn					BEBVRST Address of first virtual CCW in second extent	BEBVREN Address of last virtual CCW+8 in second extent
		CCW1					CCW2	
112	70	HDRPGLK Pointer to page-fix list	HDRINDL Pointer to indirect address list	TCCW MODB 1	TCCW CCWL 2	TCCW INDL 3	TCCW OPBT 4	HDRTICL During translation-address of first unresolved TIC CCW. After translation-address of first real CCW.
128	80	TCCWMFAD Pointer to SIO extend or PCI modify parameter list	TCCWMFCT Number of entries in SIO extend or PCI modify parameter list	HDRRQE Address of RQE				

Field	Dec	Hex
BEBNXTB	000	000
BEB2XTNT	004	004
BEBVRST	008	008
BEBVREN	012	00C
HDRPGLK	112	070
HDRINDL	116	074
TCCWMODB	120	078
TCCWCCWL	121	079
TCCWINDL	122	07A
TCCWOPBT	123	07B
HDRTICL	124	07C
TCCWMFAD	128	080
TCCWMFCT	132	084
HDRRQE	134	086

Footnotes

1. X'10' indicates SIO extend function being used
   X'20' indicates PCI modify option being used
2. Number of CCW slots remaining in current or header BEBLK
3. Number of entries remaining in current IAL
4. Operation code of CCW being translated

Figure 36. CCW Translation Header BEBLK

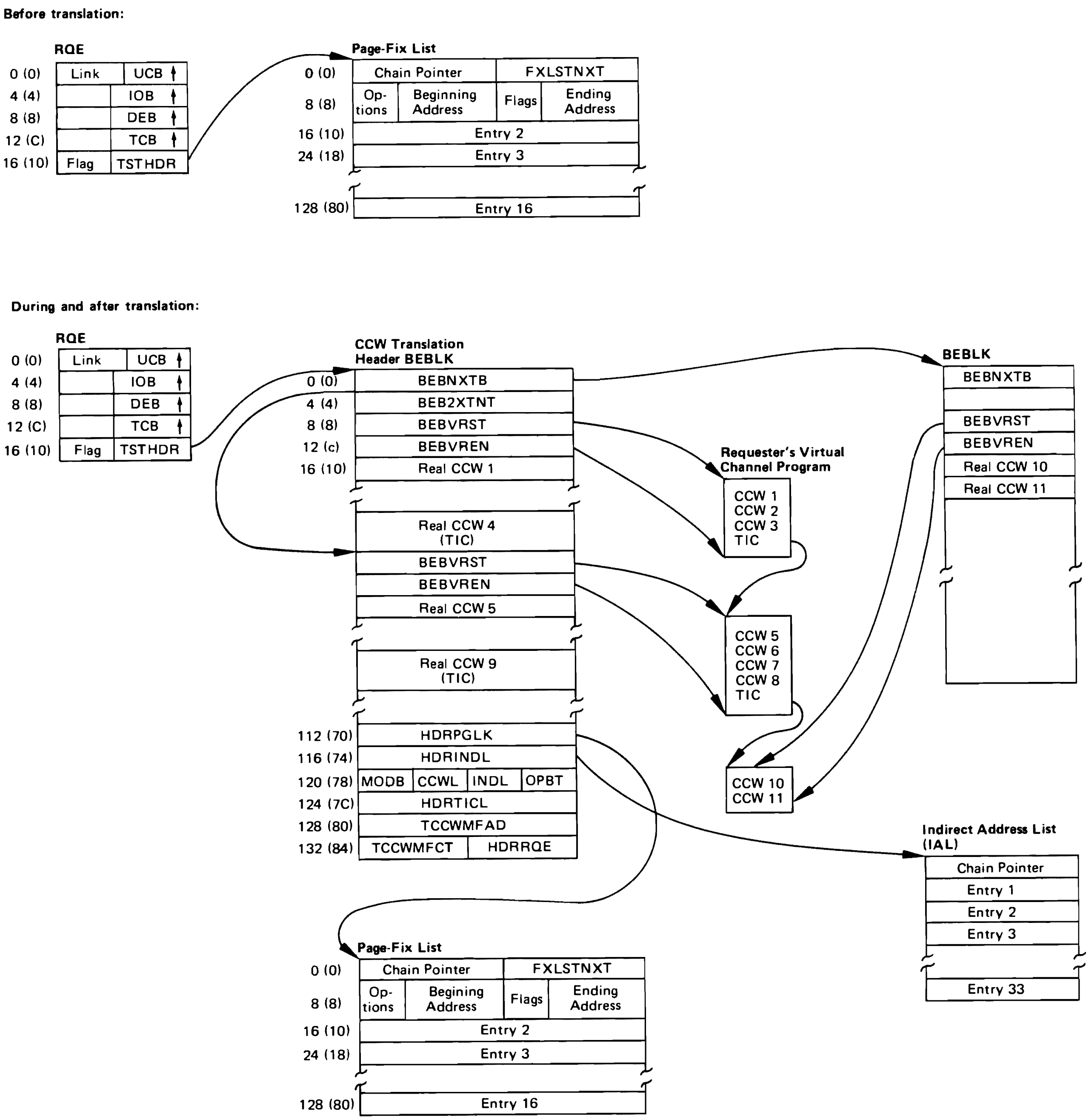


Figure 37. CCW Translation

Channel Error Block Table

The optional alternate path retry routines use the channel error block table (Figure 38). It contains entries (Figure 39) used to keep track of the failing paths to a device. (Alternate path retry routines remove failing paths from contention so that retries are only attempted on remaining nonfailing paths.)

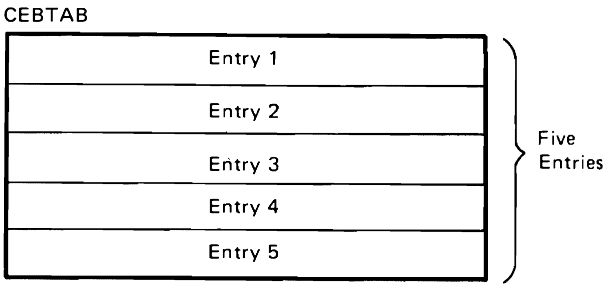
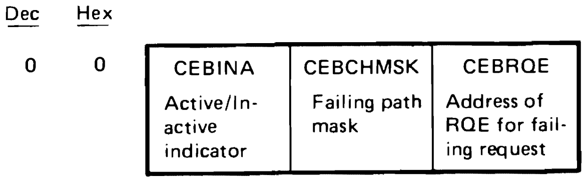


Figure 38. Channel Error Block Table


Dec
Hex
0
0
CEBINA
Active/In-active indicator
CEBCHMSK
Failing path mask
CEBRQE
Address of RQE for fail-ing request

Field	Dec	Hex
CEBCHMSK	0001	0001
CEBINA	0000	0000
CEBRQE	0002	0002

Figure 39. Channel Error Block Table Entry

Channel Status Word

The Channel Status Word (CSW, Figure 40) indicates to a program the status of an I/O device, control unit, channel, and subchannel. The CSW is assigned permanently to real storage location 64. After an I/O interruption, the channel stores information in the CSW, and also during execution of the start I/O, test I/O, and halt I/O instructions.

Dec	Hex		
0	0	Protection Key	Address of Last CCW + 8
4	4	Status	Count

Field	Dec	Hex
Address of Last CCW + 8	0001	0001
Count	0006	0006
Protection Key	0000	0000
*Status	0004	0004

*Flags and Masks

Flag Field	Contains	Hex Value	Means
Status	Byte 1	X'80'	Attention
		X'40'	Status modifier
		X'20'	Control unit end
		X'10'	Busy
		X'08'	Channel end
		X'04'	Device end
		X'02'	Unit check
		X'01'	Unit exception
	Byte 2	X'80'	Program controlled interruption
		X'40'	Incorrect length
		X'20'	Program check
		X'10'	Protection check
		X'08'	Channel data check
		X'04'	Channel control check
		X'02'	Interface control check
		X'01'	Chaining check

Figure 40. Channel Status Word

Channel Table

The channel table consists of entries containing address of channel search routines, arranged in channel number order (Figure 41). It is used when a channel becomes free and a channel-dependent channel search routine is needed to select requests that should be started next. The format of a channel table entry is shown in Figure 42.

IECCST

Entry for Multiplexer Channel
Entry for Selector Channel 1
Entry for Selector Channel 2
•
•
•
Entry for Selector Channel 6

Figure 41. Channel Table

Dec	Hex			
0	0	Address of Channel Search Routine	Channel Mask	Reserved

Field	Dec	Hex
Address of Channel Search Routine	0000	0000
*Channel Mask	0002	0002
Reserved	0003	0003

*Flags and Masks

Flag Field	Contains	Hex Value	Means
Channel Mask		X'80'	Channel 0
		X'40'	Channel 1
		X'20'	Channel 2
		X'10'	Channel 3
		X'08'	Channel 4
		X'04'	Channel 5
		X'02'	Channel 6
		X'01'	Channel 7

Figure 42. Channel Table Entry

Device Statistics Table

The device statistics table contains counters that are used to keep track of the number of times error conditions have occurred on I/O devices.

There is one 10-byte entry in the device statistics table for each I/O device in a system; in addition, there is a 10-byte control field at the beginning of the table which is used in locating entries to be updated (Figure 43).

In the case of the 3400 tape devices, a 20-byte statistics table entry is allocated for each device in a system.

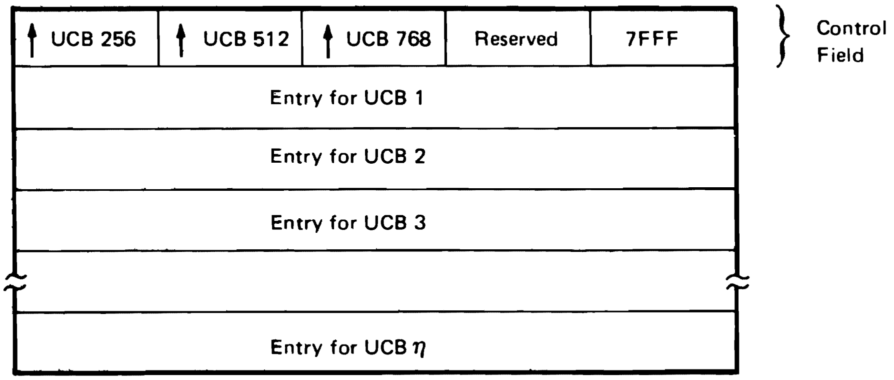


Figure 43. Device Statistics Table

There are four general formats of device statistics table entries (Figure 44). Bytes 0 through 7 of every entry contain as many four-bit counters as are needed to keep the relevant statistics for the device. Bytes 8 and 9 of each entry are work areas into which error routines place bit patterns indicating which counters are to be incremented.

Unit Record Devices

0(0) Temporary Read Failures Temporary Write Failures	1(1) Bus-Out Check	2(2) Equipment Check Overrun	3(3) Device Dependent (Sense Byte 6) Device Dependent (Sense Byte 7)
4(4)	5(5)	6(6)	7(7)
8(8) Work Area	9(9) Work Area		

2400/3400 Series Magnetic Tape Devices

0(0) Temporary Read Failures Temporary Write Failures	1(1) Intervention Required Bus-Out Check	2(2) Equipment Check Overrun	3(3) Word Count Zero Data Converter Check
4(4) Read/Write Vert. Red. Check Longitudinal Redundancy Check	5(5) Skew Cyclic Redundancy Check	6(6) Skew Reg. Vert. Red. Check Noise	7(7) Read Opposite Recovery Channel Data Check
8(8) Work Area	9(9) Work Area		

2314 Devices

0(0) Temporary Read Failures Temporary Write Failures	1(1) Bus-Out Check	2(2) Equipment Check Overrun	3(3) Track Condition Check Seek Check
4(4) Unsafe	5(5) Serializer/ Deserializer Control Unit Tag Line	6(6) Arithmetic Logical Unit	7(7) Missing Address Marker
8(8) Work Area	9(9) Work Area		

3410 Series Magnetic Tape Devices

0(0)	1(1) Noise 1,0	2(2) VRC 3,0	3(3) MTE/LRCR 3,1
4(4) EDC/CRC 3,3	5(5) Envelope Check 3,4	6(6) Overrun 0,5 Skew 3,2	7(7) Spare 3,7 Spare 4,3
8(8) PE ID CH 5,3 Mask Bit Expansion P	9(9) Track in Error Mask Bits 2,0-7 0 1 2 3 4 5 6 7	10(A) Write TM Check 5,2 Parity Compare 5,4	11(B) Tach Check 5,5 False End Mark 5,6
12(C) Spare 8,0 Feed-Through Check 8,1	13(D) Spare 8,2 End Velocity Check 8,3	14(E) No Readback Data 8,4 Start Velocity Check 8,5	15(F) Spare 8,6 Spare 8,7
16(10) Not Used 9,0 Not Used 9,1	17(11) Not Used 9,2 Not Used 9,3	18(12) Backward 3,6	19(13) Bus Out Check 0,2 Tape Unit Positioning Check 4,0

Figure 44. (Part 1 of 2) Device Statistics Table Entries

3420 Series Magnetic Tape Devices

0(0)	1(1) Noise 1,0	2(2) Read Write VRC 3,0	3(3) MTE/LRCR 3,1
4(4) EDC/CRC 3,3	5(5) Envelope Check /VRC 3,4	6(6) Overrun 0,5 Skew 3,2	7(7) C-Compare 3,7 Write Trigger VRC 4,3
8(8) PE ID CH 5,3 Mask Bit Expansion P	9(9) Track in Error Mask Bits 2,0-7 0 1 2 3 4 5 6 7	10(A) Write TM Check 5,2 Start Read Check 5,4	11(B) Partial Record 5,5 Excessive Post Amble or TM 5,6
12(C) IBG Drop While Writing 8,0 Feed-Through Check 8,1	13(D) Spare 8,2 Early Begin Read Back Check 8,3	14(E) Early End Read Back Check 8,4 Slow Begin Read Back Check 8,5	15(F) Slow End Read Back Check 8,6 Velocity Retry 8,7
16(10) Not Used 9,0 Vel. Change During Write 9,1	17(11) Not Used 9,2 Not Used 9,3	18(12) Backward 3,6	19(13) Bus Out Check 0,2 ALU Hardware Error 4,0

Figure 44. (Part 2 of 2) Device Statistics Table Entries

Device Table

The device table (Figure 45) provides the I/O supervisor with a means for obtaining the addresses of certain device and queuing-option dependent routines. The format of a device table entry is shown in Figure 46.

Priority Queuing Entry	Unit Record Device Entries
FIFO Queuing Entry	
Priority Queuing Entry	Magnetic Tape Device Entries
FIFO Queuing Entry	
Priority Queuing Entry	Direct Access Device Entries
FIFO Queuing Entry	
Ordered Seek Queuing Entry	
Priority Queuing Entry	Telecommunications Device Entries
FIFO Queuing Entry	
Priority Queuing Entry	Graphics Device Entries
FIFO Queuing Entry	
Priority Queuing Entry	Dummy Device Entries
FIFO Queuing Entry	

Figure 45. Device Table

Dec	Hex		
0	0	DVTENQ Address of enqueue routine	DVTSIO Address of start I/O routine
4	4	DVTTRP Address of trapcode routine	DVTSEN Address of sense routine

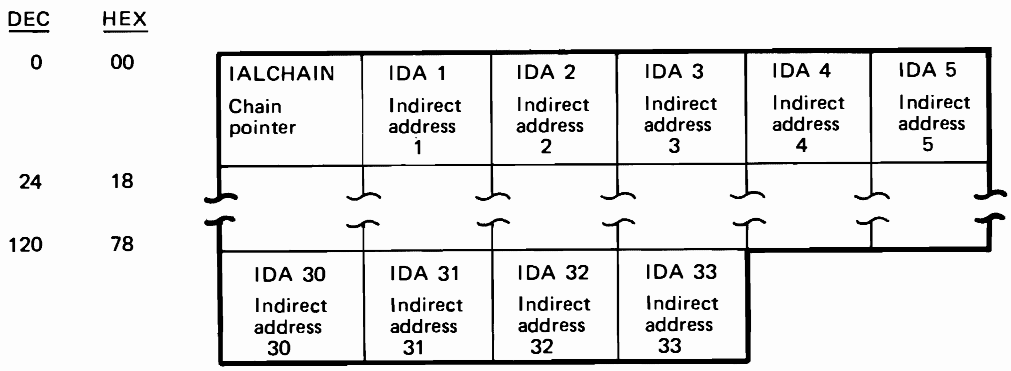
Field	Dec	Hex
DVTENQ	0000	0000
DVTSEN	0006	0006
DVTSIO	0002	0002
DVTTRP	0004	0004

Figure 46. Device Table Entry

Indirect Address List

The Indirect Address List (IAL, Figure 47) contains the beginning address of the data areas that are not contiguous in real storage.

The real CCW's data address points to the IAL. Data transfer begins with the first address in the IAL and continues until a 2K boundary is reached. It then proceeds from the second address in the IAL. This process continues until the end of the data area is reached.



DEC	HEX					
0	00	IALCHAIN Chain pointer	IDA 1 Indirect address 1	IDA 2 Indirect address 2	IDA 3 Indirect address 3	IDA 4 Indirect address 4	IDA 5 Indirect address 5
24	18						
120	78	IDA 30 Indirect address 30	IDA 31 Indirect address 31	IDA 32 Indirect address 32	IDA 33 Indirect address 33		

Field	DEC	HEX	Field	DEC	HEX
IALCHAIN	0000	0000	IDA 17	0068	0044
IDA 1	0004	0004	IDA 18	0072	0048
IDA 2	0008	0008	IDA 19	0076	004C
IDA 3	0012	000C	IDA 20	0080	0050
IDA 4	0016	0010	IDA 21	0084	0054
IDA 5	0020	0014	IDA 22	0088	0058
IDA 6	0024	0018	IDA 23	0092	005C
IDA 7	0028	001C	IDA 24	0096	0060
IDA 8	0032	0020	IDA 25	0100	0064
IDA 9	0036	0024	IDA 26	0104	0068
IDA 10	0040	0028	IDA 27	0108	006C
IDA 11	0044	002C	IDA 28	0112	0070
IDA 12	0048	0030	IDA 29	0116	0074
IDA 13	0052	0034	IDA 30	0120	0078
IDA 14	0056	0038	IDA 31	0124	007C
IDA 15	0060	003C	IDA 32	0128	0080
IDA 16	0064	0040	IDA 33	0132	0084

Figure 47. Indirect Address List

Logical Channel Word

The Logical Channel Word (LCH, Figure 48) is an 8-byte data area which is used primarily to define the bounds of a logical channel queue. There is one logical channel word for each logical channel queue. All of the logical channel words together make up a table called the *logical channel table*. The format of a logical channel word is shown in Figure 49.

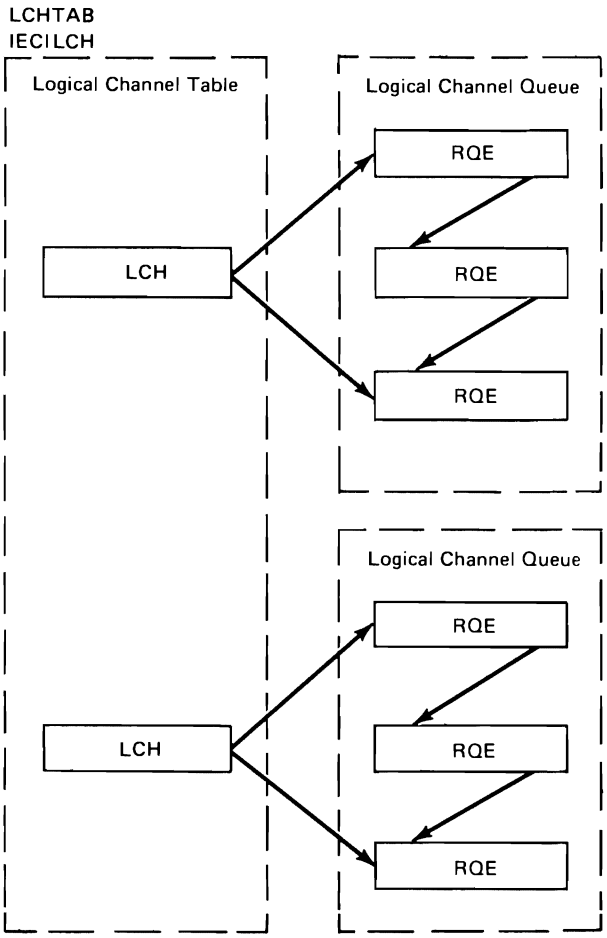


Figure 48. Logical Channel Queues

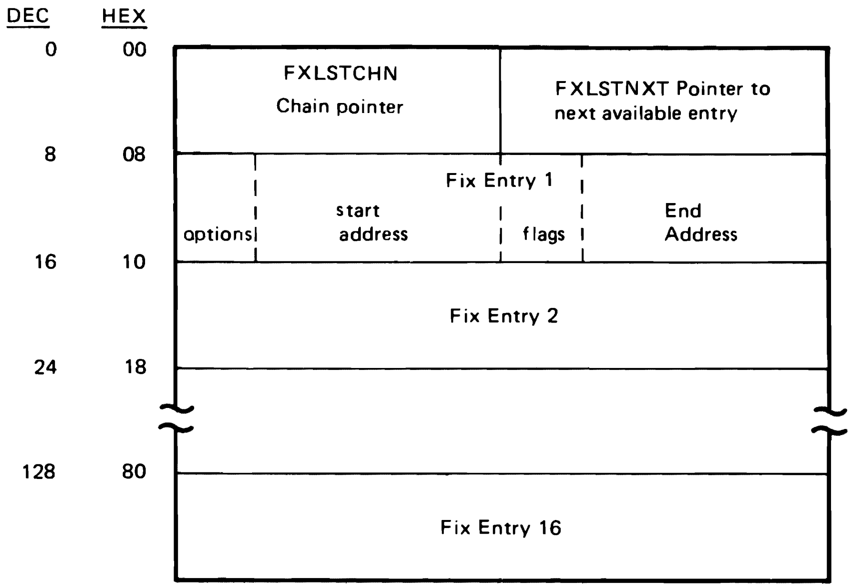
Dec	Hex		
0	0	LCHFTS Address of first RQE in logical channel queue	LCHLTS Address of last RQE in logical channel queue
4	4	LCHSRH Work area	LCHTCH Address of test channel routine

Field	Dec	Hex
LCHFTS	0000	0000
LCHLTS	0002	0002
LCHSRH	0004	0004
LCHTCH	0006	0006

Figure 49. Logical Channel Word

Page Fix List

The Page Fix List (PGFX), built by the page fix routine, contains the address of pages that should not be removed from real storage through normal paging operations. Entries are made for control blocks and up to five appendages. The user page fix appendage, if provided, can also make entries into the list. Figure 50 shows the format of the page fix list.



Field	DEC	HEX
Fix Entry 1	0008	0008
Fix Entry 2	0016	0010
Fix Entry 3	0024	0018
Fix Entry 4	0032	0020
Fix Entry 5	0040	0028
Fix Entry 6	0048	0030
Fix Entry 7	0056	0038
Fix Entry 8	0064	0040
Fix Entry 9	0072	0048
Fix Entry 10	0080	0050
Fix Entry 11	0088	0058
Fix Entry 12	0096	0060
Fix Entry 13	0104	0068
Fix Entry 14	0112	0070
Fix Entry 15	0120	0078
Fix Entry 16	0128	0080
FXLSTCHN	0000	0000
FXLSTNXT	0004	0004

Options and Flags

Options—bits 1-7 valid on first entry only

Hex	Means
X'80'	Continuation flag
X'40'	Fix request
X'20'	Free request
X'10'	Page load to be done
X'08'	Release option
X'02'	Long term fix

Flags—valid on End Address entry

Hex	Means
X'80'	Last entry
X'40'	Null entry
X'20'	Real address option for fix
X'10'	Error flag
X'08'	Suspend option for fix

Figure 50. Page Fix List

Program Controlled Interrupt Modify Parameter List

A Program Control Interrupt (PCI) appendage builds the PCI modify parameter list to define to the I/O interruption supervisor the CCWs that were modified during the execution of the PCI appendage. The I/O interruption supervisor then modifies the real channel program in the SQA according to the changes made by the PCI appendage.

Figure 51 shows the format of an entry in the list.

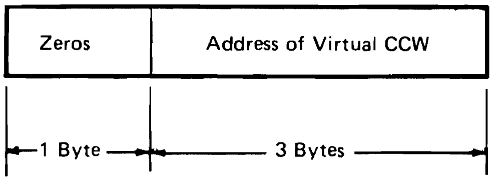


Figure 51. PCI Modify Parameter List Entry

Program Status Word

The Program Status Word (PSW, Figure 52) is a two-way communication link between a CPU and a program. All PSWs occupy permanently assigned virtual storage locations. The PSWs to which the I/O supervisor refers are:

Name	**Location**	**Symbolic Name**
SVC Old PSW	32(20)	SVCOPSW
I/O Old PSW	56(38)	IOPSWO
I/O New PSW	120(78)	IONPSW

Dec	Hex				
0	0	0R00ATIE	Protection Key and 1MWP	Condition Code and Program Mask	0——0
4	4	Instruction Address			

Field	Dec	Hex
*1MWP	0001	0001
1 Condition Code	0002	0002
Instruction Address	0004	0004
*Program Mask	0002	0002
Protection Key	0001	0001
*0R00ATIE	0000	0000

*Flags and Masks

Flag Field	Contains	Hex Value	Means
1MWP		X'08'	EC mode bit must be set to 1.
		X'04'	Machine check interruptions can occur.
		X'02'	The CPU is in the wait state.
		X'01'	The CPU is in the problem state.
		X'00'	The CPU is in the supervisor state.
0R00ATIE		X'80'	Enabled for monitor calls
		X'40'	Enabled for program event recording
		X'20'	0
		X'10'	0
		X'08'	31-bit addressing
		X'04'	Dynamic address translation
		X'02'	Enabled for I/O interruptions
		X'01'	Enabled for external interruptions
Program Mask		X'08'	Fixed point overflow
		X'04'	Decimal overflow
		X'02'	Exponent underflow
		X'01'	Significance

Figure 52. Program Status Word

Request Queue Element

The Request Queue Element (RQE, Figure 53) contains the address of the major control blocks needed to process a request for I/O activity.

During system generation, a number of RQEs are created to equal the maximum number of a new I/O operations that can be processed simultaneously by the new operating system. Except for the last, each of these unassigned RQEs contains only the address of the next RQE; the last RQE contains ones in its address, or link field. The chain of unassigned RQEs is called a freelist.

When a request for I/O activity is received by the I/O supervisor, it removes one RQE from the freelist, and the RQE is initialized with the addresses of control blocks needed to process the request.

When a request cannot be started immediately, the RQE is placed into a logical channel queue. The RQE remains in the queue until the needed device and a path to the device becomes available and, optionally, until high-priority requests for the same device and path are satisfied.

During the I/O activity, the address of the RQE is in the UCBLTS field of the UCB. An RQE is returned to the freelist when all I/O activity associated with the request it represents is completed.

All of the RQEs are located contiguously in real storage and are sometimes referred to as the request queue element table. The term table is used loosely, however, because access is gained to the specific RQEs by way of pointers and not by offsets from the beginning of the table.

Dec	Hex		
0	0	TSTLNK Address of next RQE	TSTUCB Address of UCB
4	4	TSTTCB Task ID	TSTIOB Address of IOB
8	8	TSTPR Priority	TSTDEB Address of DEB
12	0C	TSTKEY Requester's Protection Key	TSTTCBAD Address of TCB
16	10	TSTHDR CCW Translation flags; address of page-fix list before CCW translation and address of header BEBLK during and after CCW translation.	

Field	Dec	Hex
TSTDEB	0009	0009
*TSTHDR	0016	0010
TSTIOB	0005	0005
TSTKEY	0012	000C
TSTLNK	0000	0000
TSTPR	0008	0008
TSTTCB	0004	0004
TSTTCBAD	0013	000D
TSTUCB	0002	0002

*Flags and Masks

Flag		Hex	
Field	Contains	Value	Means
TSTHDR	CCW Translation Flags	X'80'	Fixed requester SVC 114
		X'40'	Virtual requester
		X'20'	Nonpageable requester
		X'10'	Page supervisor is requester
		X'08'	Translation in progress
		X'04'	Translation complete
		X'02	Used by an SVC 114 request to re-execute a channel program out of the channel-end appendage following error recovery.
		X'01'	RQE has been queued on LCH

Figure 53. Request Queue Element

Start Input/Output Extend Parameter List

A Start Input/Output (SIO) appendage (Figure 54) builds the SIO extend parameter list to define to the EXCP supervisor all of the CCWs that might be used in an I/O operation. The EXCP supervisor then translates all of the CCWs referenced on the list before issuing the start I/O instruction to the I/O device. Each entry in the list has the following format.

- If bit 0 of byte 0 of the count field is a 0, the count field specifies the number of contiguous CCWs in the string to be translated. The EXCP supervisor then translates the CCW string to real addresses. If the first CCW in the string has already been translated the EXCP supervisor assumes the entire string has been translated and bypasses the entry.
- If bit 0 of byte 0 of the count field is a 1, the count field specifies the maximum number of indirect address words required for the CCW. This implies that the CCW data address or length can change. The count is the maximum CCW data length to be used divided by 2K. Such entries must refer to CCWs within the CCW strings specified in the list. The EXCP supervisor constructs a corresponding real CCW with the indirect address word bit, bit 37(25), set to one and creates an indirect address list whether or not it is required.

Count	Address of a Virtual CCW
1 Byte	3 Bytes

Figure 54. SIO Extend Parameter List

Volume Statistics Table

The volume statistics table contains information and statistics pertaining to volumes on 2400/3400 series magnetic tape devices. It contains one entry for each 2400 and 3400 magnetic tape device in a system.

The address of each entry is contained in the UCB for the device containing the volume. The entries may or may not be contiguous. The format of each entry varies according to the options selected at system generation time. If neither the error volume analysis (EVA) nor the error statistics by volume (ESV) options are selected, an entry will consist of only the first 8 bytes shown in Figure 55. If only EVA was specified, each entry will consist of the first 16 bytes whown. If ESV or both ESV and EVA were specified, the length of each entry will be the full 24 bytes.

For 3400 series magnetic-tape units, the length of each entry is always 24 bytes.

For 3400 series magnetic-tape units, the length of each entry is always 24 bytes.

<table>
<tr><th>Dec</th><th>Hex</th><th colspan="8"></th></tr>
<tr><td>0</td><td>0</td><td colspan="8">CCW for Read-Opposite Recovery</td></tr>
<tr><td>8</td><td>8</td><td colspan="2">Statistics Update Mask</td><td>Read Error Threshold</td><td>Write Error Threshold</td><td>Temporary Read Errors</td><td>Temporary Write Errors</td><td colspan="2">Start I/O</td></tr>
<tr><td>16</td><td>10</td><td>Permanent Read Errors</td><td>Permanent Write Errors</td><td>Noise Blocks</td><td>Reserved*</td><td colspan="2">Erase Gaps</td><td colspan="2">Cleaner Actions</td></tr>
</table>

*'Mode Set' when tape device has extended sense.

Field	Dec	Hex	Field	Dec	Hex
CCW for Read-Opposite			Read Error Threshold	0010	000A
Recovery	0000	0000	Reserved	0019	0013
Cleaner Actions	0022	0016	Start I/O	0014	000E
Erase Gaps	0020	0014	Statistics Update Mask	0008	0008
Noise Blocks	0018	0012	Temporary Read Errors	0012	000C
Permanent Read Errors	0016	0010	Temporary Write Errors	0013	000D
Permanent Write Errors	0017	0011	Write Error Threshold	0011	000B

Figure 55. Volume Statistics Table Entry

DIAGNOSTIC AIDS

This section contains information to help you interpret the program listings and diagnose program failures.

General Register Assignments

Figure 56 shows the general register assignments for the resident parts of the I/O supervisor (EXCP Supervisor, I/O Interruption Supervisor, and Error EXCP Supervisor). Assignments for other routines can be found in the prologs to the routine listings.

Register	Symbol	Assignment
0	REG0	Temporary storage
1	TSTREG	RQE Address (For assigned but not-queued RQE)
2	IOBREG	IOB address
3	BASREG3	Base register for translator
3	DEBREG	DEB address
4	BASREG5	Third base register
4	DCBREG	DCB address
5	BASREG	Base register for I/O supervisor
6	BASREG4	Second base register for translator
6	UAREG	Channel and unit address
7	UCBREG	UCB address
8	LNKGR1	Second Base register
9	ICREG HDRREG TCCWREG	Work register Pointer to CCW translation header BEBLK Pointer to CCW translation header BEBLK
10	WKREG1	Work register
11	WKREG2	Work register
	PRFXREG	Prefix storage address register
12	WKREG3 LINKRG3	Spare work/linkage register
13	BEBREG	Address of current BEBLK
13	LCHREG	Logical channel word address
14	LNKRG2	Linkage register
15	APBSRG	Used for calculating addresses of appendages to be invoked and used as a base register for the appendages.

Figure 56. General Register Assignments

System Completion Codes

When a task is terminated abnormally, a three-digit system completion code printed in the storage dump generally indicates why. See *OS/VS Message Library: VS2 System Codes* for a complete list of system completion codes. The meanings of the codes produced when abnormal termination results from trouble during input/output processing are shown in Figure 57.

Code	Explanation	Comments
200	An error was detected during EXCP processing; the storage protection key of the IOB, ECB, or DCB was not the same as the protection key field in the DEB.	This system completion code will result if a program check occurs while the DCB, ECB, or IOB is being loaded for IOS EXCP validity checking. Typical causes are premature freeing or overrunning of control blocks. If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0, 64, 84, and 92 in the IOS problem determination area.
300	An error was detected when an I/O operation was requested; the storage protection key of the DEB was not zero or the DEB validity check routine IFGDEBCK returned to IOS with a nonzero return code.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0 and 64 in the IOS problem determination area.
400	The control block chain between the IOB, DCB, DEB, and UCB was invalid. The control program found that one of the blocks was incorrectly modified or built.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0 and 64 in the IOS problem determination area.
500	An unexpected program interruption occurred during processing of IOS. Note that the program interruption can be due to a page exception.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0, 64, 84, 92, and 96 in the IOS problem determination area.
600	An SVC 114 was issued with one of the following conditions: • The 'SVC114 authorization' bit was not set in the DEB. • The protection key was not zero. • The request was not issued in supervisor state. • The authorization bit was not set in the JSCB.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offset 0 in the IOS problem determination area.
700	A program check occurred in a supervisor service routine called by IOS.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0, 64, 84, and 92 in the IOS problem determination area.
800	An error occurred when IOS attempted to fix a page for this EXCP request.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0, 64, 84, and 212 in the IOS problem dete-mination area.
900	A program check occurred in a user appendage or an attention routine.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0, 64, 84, and 92 in the IOS problem determination area.
A00	In translating CCWs out of the PCI appendage, IOS found one of the following: • A buffer or channel program area had not been fixed. • An invalid IAL entry in the SIO extent list.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0 and 64 in the IOS problem determination area.
C00	Too many entries were specified by the page fix appendage in its page fix list.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0, 64, and 84 in the IOS problem determination area.
D00	A page which was referenced within the control blocks, channel program, user page-fix list, or an appendage of IOS which was not within the user's region, LSQA, nucleus, SQA, or LPA.	If an abnormal termination dump is available, see "Problem Determination Area" for the meaning of offsets 0, 64, 84, and 212 in the IOS problem determination area.

Figure 57. System Completion Codes for I/O Operations

Problem Determination Area

If an abnormal termination dump is available, the TCB field (TCBIOSAB) at offset 192 will contain a pointer to the IOS problem determination area. The format of this area is:

Offset		Field Description, Contents, Meaning
Dec	Hex	
0	0	Registers at the time of error
64	40	Contents of the RQE
84	54	Program check PSW at the time of the program check, or first page fix list if this is an ABEND 800, C00, or D00.
92	5C	ILC and interruption code
96	60	Only meaningful on page faults. This field contains the address causing the last page fault.
212	D4	Second page fix list if it exists.

Patch Area at IECINT

At IECINT is a 17-word storage area that can be used for diagnostic work. Since its location is not standard but differs for each system, refer to the address constant at label IOSORG for the true address.

Generalized Trace Facility

The Generalized Trace Facility (GTF) provides a method of tracing program events and recording information about these events. The trace records that are generated by GTF are stored internally in a table or recorded externally on a data set that becomes input to the AMDPRDMP service aid program. AMDPRDMP edits and formats the trace records as specified by an EDIT control statement.

The I/O supervisor interfaces with GTF when it is optioned by using monitor call instructions (GTF hooks). Figure 58 shows the location of the GTF hooks and the information that is traced.

More information about GTF can be obtained from the following publications:

OS/VS Service Aids

OS/VS2 Debugging Guide

Location	Function	Register Contents	Information Traced
After label INT001C	Detects the occurrence of an I/O interrupt with an associated UCB. (Normal I/O interrupt)	R7 - UCB address R10 - Real CCW address from the CSW if an RQE exists for this request. R10 - Zero if no RQE exists.	I/O Old PSW CSW (Contains the virtual CCW address+8 if it was a virtual request.) RQE JOBNAME DDNAME Sense bytes 0 - 3. I/O interrupt code. Real CCW address+8. TCB address.
After labels INT001 and INT00A	Detects the occurrence of an I/O interrupt without an associated UCB.	N/A	I/O Old PSW CSW (Contains the real CCW address.) I/O interrupt code.
After label XCP110D	Detects the occurrence of SIOs in the SIO subroutine.	R1 - RQE address. R6 - Device address. R10 - SIO condition code in low order byte.	CSW (Contains real CCW address) CAW (Contains real CCW address) RQE JOBNAME TCB address. SIO condition code. Device address. Virtual address of the virtual channel program.
After label INT024C	Detects an I/O interrupt with PCI status.	R7 - UCB address. R10 - Real CCW address+8	I/O Old PSW CSW RQE JOBNAME DDNAME Sense bytes 0-3. Real CCW address. I/O interrupt code. TCB address.

Figure 58. GTF Interfaces

APPENDIX A: SUPPORTING SVC ROUTINES

The SVC routines described in this appendix are not generally used during normal processing of requests for I/O operations. They do, however, provide users with a capability for referring to, obtaining, and changing some of the data used in processing the I/O requests.

Purge Routine (SVC 16)

The Purge routine stops the processing of I/O requests by removing request queue elements (RQEs) from queues. Depending upon the options specified in a parameter list which is provided as input (Figure 59), the Purge routine can remove RQEs from:

- A logical channel queue
- The supervisor's request block queues
- The supervisor's asynchronous exit queue
- The DDR wait queue

The Purge routine can remove the elements representing all requests for a particular data set or task. The method to be used is indicated in the seventh bit of the options field in the parameter list. The general flow of control within the Purge routine is shown in Figure 62. The PURGE macro instruction is described in *OS/VS Data Management for System Programmers.*

0(0) PRGOPT Purge Options	1(1) PRGDEB Address of Data Extent Block
4(4) PRGCOD Completion Code	5(5) PRGTCB Address of Task Control Block
8(8) PRGCTR Quiesce Count	9(9) PRGCHN Address of First Link in Chain
12(0C) * PRGFLG Flags	13 (0D) PRGQPL Address of Quiesce I/O Parameter List

* TSO only

Figure 59. Purge Routine Parameter List

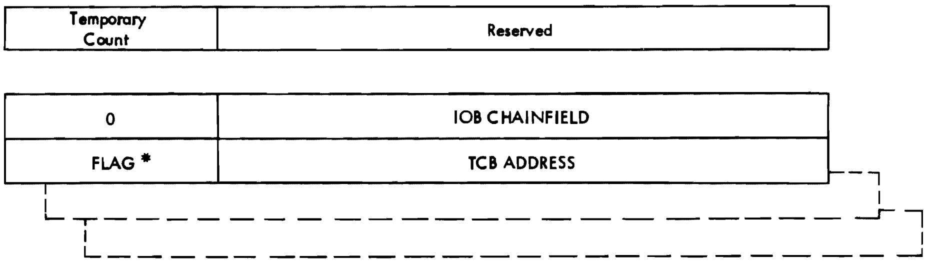
Removing Elements From Logical Channel Queues

If all requests for a particular data set are to be purged, the Purge routine examines the data extent block (DEB) for the data set, and removes all RQEs from the logical channel queue for the device or devices whose unit control block (UCB) addresses are contained in the DEB. When an active shared device is allocated with a purged request, the I/O supervisor sets the UCB's HIO flag to issue a RELEASE to the device if its UCB reserve count field is zero.

When the elements for all requests associated with a particular task are to be purged, the Purge routine scans the entire request element table to locate and remove the RQEs for the task.

Purge Routine Parameter List

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	PRGOPT	Purge options.
		0...	Purge request queue elements for all entries in the data extent block (DEB) chain, starting with the DEB whose address is in PRGDEB.
		1...	Purge only the request queue element for the DEB whose address is in PRGDEB.
		.0..	Do not post the event control blocks for the purged request queue elements.
		.1..	Post the event control blocks for the purged RQEs. (A X'48' completion code is used.)
		..0.	Allow the activity to quiesce.
		..1.	Halt the I/O activity. (The effect of the Halt I/O instruction is simulated if the operation is a seek.)
		...0	Purge all requests.
		...1	Purge only related requests.
		.... 0...	Normal purge.
		.... 1...	Purge TCB list.
		.... .0..	Purge the asynchronous exit queue, the request block queue, the logical channel queue, and the DDR wait queue.
		.... .1..	Purge the asynchronous exit queue, the request asynchronous exit queue removing only RQEs for requests in error, and the DDR wait queue. Bypass the request blocks.
		.... ..0.	Purge by data extent block.
		.... ..1.	Purge by task control block. When this bit is on, the setting of bit 0 is ignored.
		x	Not used.
1(1)	. 3	PRGDEB	Address of data extent block.
4(4)	1	PRGCOD	Purge routine completion code.
5(5)	. 3	PRGTCB	Address of task control block.
8(8)	1	PRGCTR	Quiesce count. The number of active request queue elements for which I/O activity has not yet been completed.
9(9)	. 3	PRGCHN	Address of the first link in the chain of IOBs which are purged. The first link can be located in the user's area, or in the DEBUSPRG field of the DEB. It will point to the first IOB in the chain. The last IOB in the chain will contain ones in the low-order byte of the restart address (IOBRST) field.
12(C)	1	PRGFLG	Purge flags.
		0...	Purge entry.
		1...	Wait entry.
		.0..	Return before wait.
		.1..	Purge and wait.
		..0.	DEQ before WAIT.
		..1.	No DEQ before WAIT (set before system DEB purged).
		...x	Not used.
		.... x...	Not used.
		.... .x..	Not used.
		.... ..x.	Not used.
		x	Not used.



* Field for Last Entry is X '80'

Figure 60. Quiesce I/O Parameter List

Quiesce I/O Parameter List (TSO Only)

Offset	Bytes and Alignment	Field Description
0(0)	1	Temporary count field.
1(1)	. 3	Not used.
8(8)	8	First parameter list entry.

Byte	Description	
0	Not used.	
1-3	IOB chain field.	
4	QPL flags.	
	0...	More entries follow.
	1...	Last entry.
	.0..	Not a current entry.
	.1..	Current entry.
5-7	Address of TCB to be purged.	

Additional parameter list entries may be present.

Removing Elements From the Supervisor's Request Block Queues

To remove elements from a supervisor request block queue, the Purge routine obtains the address of the first request block in the queue from the TCB whose address is passed as input. When no TCB address is passed, it assumes that the current TCB is the input TCB. The Purge routine then scans the entire request block queue. For each system interruption request block (SIRB) and interruption request block (IRB) in the queue, the Purge routine removes the RQEs containing a DEB address which matches the input DEB address (for a purge by data set); or removes the RQEs containing a TCB address which matches the address of the input TCB (for a purge by task).

Descriptions of the SIRB and IRB are contained in *OS/VS2 System Data Areas.*

Removing Elements From the Supervisor's Asynchronous Exit Queues

To remove request queue elements from the supervisor's asynchronous exit queue, the Purge routine first obtains the address of the queue from the communications vector table. It then scans the entire asynchronous exit queue, removing every RQE containing a DEB address which matches the input DEB address (for a purge by data set); or removing every RQE containing a TCB address which matches the address of the input TCB (for a purge by task). When a TCB address is not passed as input for a purge by task request, the Purge routine uses the current TCB for the matches.

The communications vector table is described in *OS/VS2 System Data Areas.*

The IOB Chain

The Purge routine links the IOBs for purged requests together in a chain beginning at the address specified in the third word of the Purge routine parameter list (Figure 61). A RESTORE macro instruction could then be used to restart the requests. The Purge routine does not create an IOB chain when the halt I/O option is specified with the purge-by-TCB option.

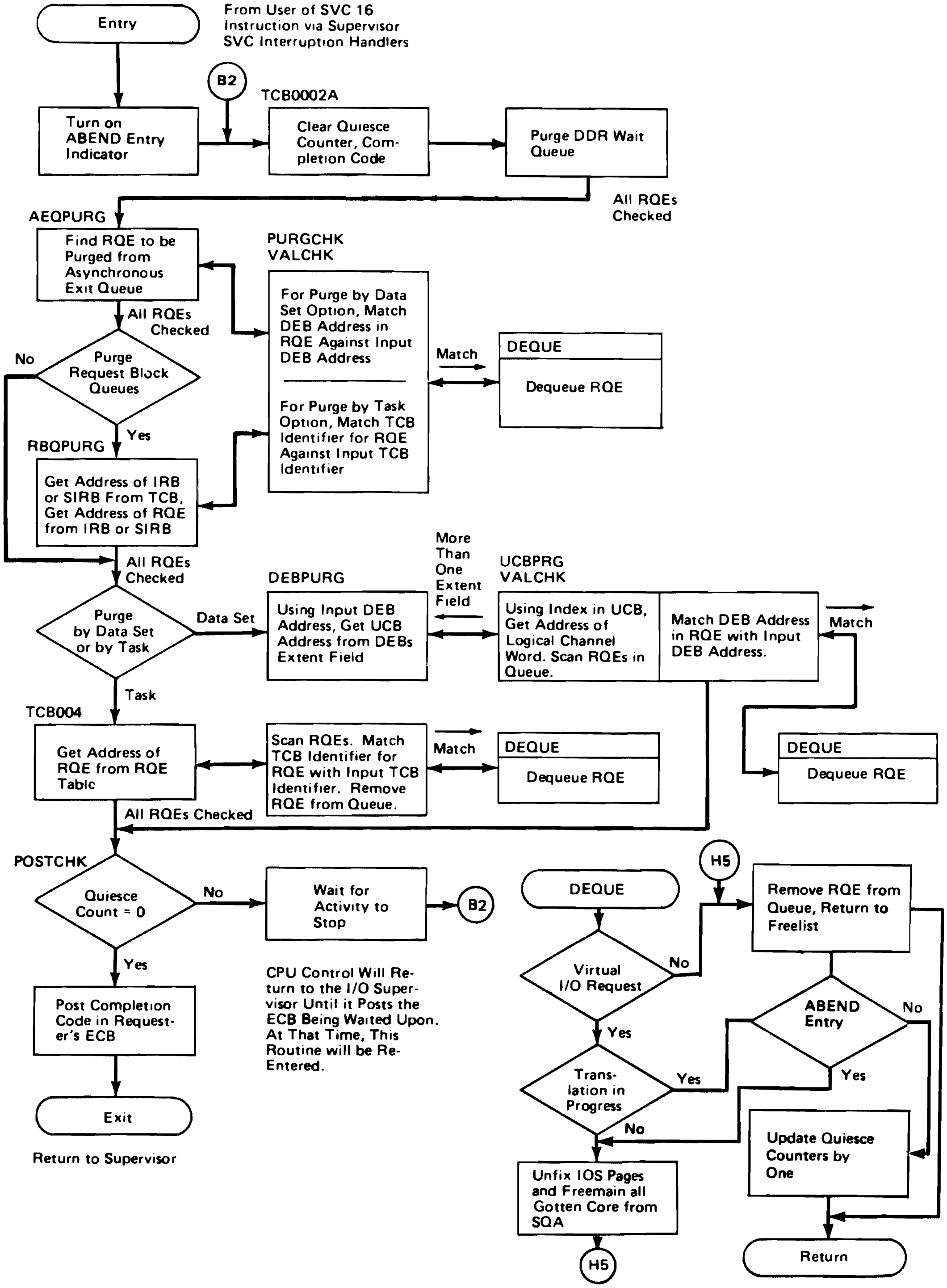

Entry
From User of SVC 16 Instruction via Supervisor SVC Interruption Handlers
B2
TCB0002A
Turn on ABEND Entry Indicator
Clear Quiesce Counter, Completion Code
Purge DDR Wait Queue
All RQEs Checked
AEQPURG
Find RQE to be Purged from Asynchronous Exit Queue
PURGCHK
VALCHK
For Purge by Data Set Option, Match DEB Address in RQE Against Input DEB Address
For Purge by Task Option, Match TCB Identifier for RQE Against Input TCB Identifier
Match
DEQUE
Dequeue RQE
All RQEs Checked
No
Purge Request Block Queues
Yes
RBQPURG
Get Address of IRB or SIRB From TCB, Get Address of RQE from IRB or SIRB
All RQEs Checked
More Than One Extent Field
UCBPRG
VALCHK
DEBPURG
Purge by Data Set or by Task
Data Set
Using Input DEB Address, Get UCB Address from DEBs Extent Field
Using Index in UCB, Get Address of Logical Channel Word. Scan RQEs in Queue.
Match DEB Address in RQE with Input DEB Address.
Match
Task
TCB004
Get Address of RQE from RQE Table
Scan RQEs. Match TCB Identifier for RQE with Input TCB Identifier. Remove RQE from Queue.
Match
DEQUE
Dequeue RQE
DEQUE
Dequeue RQE
All RQEs Checked
POSTCHK
Quiesce Count = 0
No
Wait for Activity to Stop
B2
CPU Control Will Return to the I/O Supervisor Until it Posts the ECB Being Waited Upon. At That Time, This Routine will be Re-Entered.
Yes
Post Completion Code in Requester's ECB
Exit
Return to Supervisor
DEQUE
H5
Virtual I/O Request
No
Yes
Remove RQE from Queue, Return to Freelist
ABEND Entry
No
Yes
Trans-lation in Progress
Yes
No
Unfix IOS Pages and Freemain all Gotten Core from SQA
H5
Update Quiesce Counters by One
Return

Figure 61. Purge Routine

The Quiesce Option

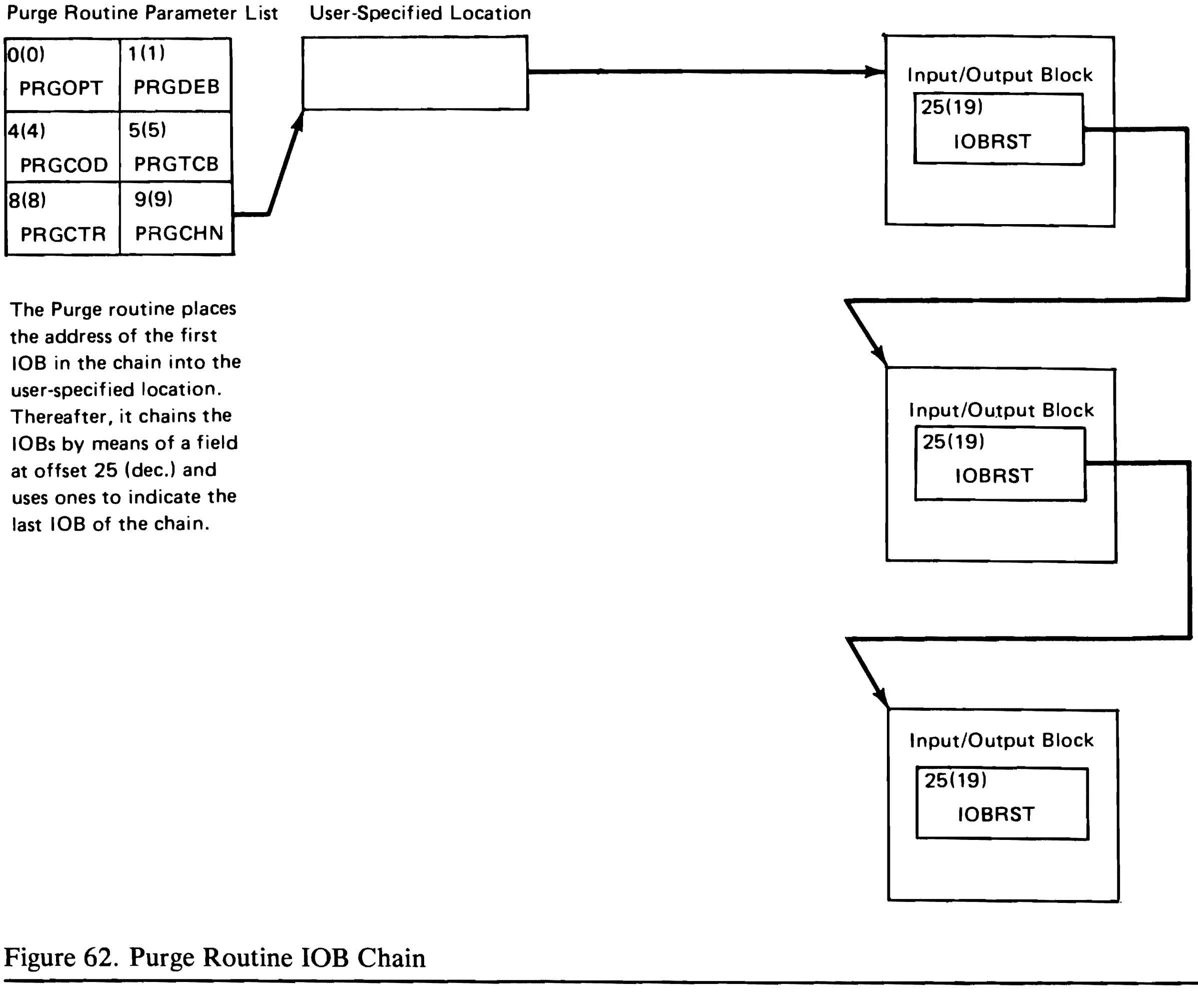
When the quiesce option is specified, the Purge routine increments two counters by one for each I/O request awaiting completion:

- A main purge counter in the parameter list
- A secondary counter in each effected DEB

Thus, if there is a request to quiesce activity for a specific data set, both counters will have a count of one. If there is a request to quiesce the activity on all data sets of a task, however, there will be counts in each DEB counter reflecting the number of not-yet-completed requests for the data sets, and there will be a total count in the main counter.

Every time the Purge routine increments a counter, it places a pointer to the purge parameter list into the 'address of purge parameter list' field of the DEB. Also, after it has put the total count in the main counter, the Purge routine issues a WAIT macro instruction.

When I/O activity has been completed for a request, the I/O interruption supervisor will enter its Quiesce Complete subroutine (entry point PRGCOMA or PRGCOMB) if it finds an address in the 'address of purge parameter list' field of the DEB for the newly completed activity. The Quiesce Complete subroutine decrements both the main and secondary counters by one. If a DEB secondary counter is zeroed, the 'address of purge



The Purge routine places the address of the first IOB in the chain into the user-specified location. Thereafter, it chains the IOBs by means of a field at offset 25 (dec.) and uses ones to indicate the last IOB of the chain.

Figure 62. Purge Routine IOB Chain

parameter list' field in the DEB is also zeroed. When the main counter in the parameter list is zeroed, indicating the quiesce is complete, the Quiesce Complete subroutine posts the purge ECB. If the main counter is not zeroed, the Quiesce Complete subroutine return control to the I/O interruption supervisor.

Purging a Virtual I/O Request

When purging a virtual I/O request, the CCW translation status must be considered before returning the RQE to the freelist. If translation is finished, the purge routine links to the I/O supervisor to unfix the pages and to return the SQA space that was gotten for this request to IOS. The RQE is then returned to the freelist.

If CCW translation is not finished, a paging I/O operation is in progress. In this case, the RQE is quiesced and the address of the purge parameter list is placed into the DEB. The purge routine then processes the next RQE. When the paging I/O operation is finished, the CCW translator examines the DEB to see if the RQE it was translating was purged. If it was, it completes the purge as stated in the previous paragraph.

Restore Routine (SVC 17)

The Restore routine restarts the processing of requests that have been dequeued by means of the Purge routine if Halt I/O option was not specified with the purge-by-task option. Using a pointer to the first IOB in a chain of IOBs that it receives as input in register 1, the Restore routine issues an SVC 0 or an SVC 114 for each IOB in the chain, depending on the type of I/O operation purged.

The RESTORE macro instruction is described in *OS/VS Data Management for System Programmers.*

DEVTYPE Routine (SVC 24)

The DEVTYPE routine supplies information about the characteristics of I/O devices. The instructions in the expansion of the Locate Device Characteristics (DEVTYPE) macro instruction place parameters into general registers, and the DEVTYPE routine uses the parameters to identify the device and to find where it should place the output information.

The DEVTYPE macro instruction is described in the publication *OS/VS Data Management for System Programmers.*

Using the DD name it receives as input, the DEVTYPE routine finds the corresponding task input/output table (TIOT) entry, and uses it to locate the proper UCB. The DEVTYPE routine then obtains the device type field from the UCB and places it into the first word of the output area.

If the DEVTAB parameter was not specified, the output area will contain two words of information. The DEVTYPE routine determines the maximum block size from the device charactersitics table (if the device is a direct-access device) or from internal constants, and moves it to the second word of the output area.

If the DEVTAB parameter was specified in the DEVTYPE macro instruction, and the device is a direct-access device, the DEVTYPE routine will provide three additional words of information. The DEVTYPE routine locates the device characteristics table via the communication vector table, moves the appropriate entry into the low-order three words of the output area, and moves the blocksize field to the second word of the output area.

Before relinquishing control, the DEVTYPE routine places a return code into register 15. A return code of 00 indicates that the request was completed successfully. A return code of 04 indicates one of the following conditions:

- No output area specified: The area parameter was not included in the DEVTYPE macro instruction.
- DD name not found: No TIOT entry exists that corresponds to the DD name supplied.
- Invalid UCB unit type field: The UCB unit type field (byte 4 of the device code field) does not specify a direct-access, tape, or unit record device.

A return code of 08 indicates that an invalid output area address was specified.

IOHALT Routine (SVC 33)

The IOHALT routine stops all activity on the teleprocessing device whose unit control block (UCB) address is passed in register 1. It does not stop activity on nonteleprocessing devices.

The IOHALT routine checks the validity of the UCB address it receives by matching it against the UCB addresses in the UCB lookup table. If the address passed is valid and if the device to be stopped is a teleprocessing device, the IOHALT routine gives control to the resident Halt I/O routine (entry point IECIHIO), which issues a Halt I/O instruction and returns. The IOHALT routine places a completion code into register 15 before relinquishing control:

Code (Hex.)	Meaning
00	The device was stopped.
04	The device is not running.
08	The device was not stopped because it is not a teleprocessing device.
0C	The device was not stopped because the UCB address was invalid.

VOLSTAT Routine (SVC 91)

The first load module of the VOLSTAT routine constructs error-statistics-by-volume (ESV) records and, depending upon what was specified during system generation, writes them on either the console output device or the system management facilities (SYS1.MAN) data set.

Data management Close and EOV routines pass control to the VOLSTAT routine when the volume is demounted.

The VOLSTAT routine obtains error statistics from the volume statistics table, and obtains other identifying information from the UCB, DCB, or JFCB and DEB. After writing an ESV record, the VOLSTAT routine clears the counters in the volume statistics table and returns control to the Close or EOV routine.

The second load module is called to read the buffered log data of an IBM 2305 Fixed Head Storage, IBM 3330 Disk Storage, or IBM 3333 Disk Storage and Control. This load module is activated when a new volume is mounted or when the operator enters a HALT EOD command.

TCB EXCP (SVC 92) (TSO only)

The TCB EXCP routine allows the user to specify, in register 0, a TCB address associated with the IOB address passed in register 1. The specified TCB will be the one associated with the RQE.

Extended SVC Routine (SVC 109)

The Extended SVC routine is used by the Task Termination routine to ensure that a task cannot leave outstanding I/O requests.

The routine checks each RQE in the system, unless outstanding teleprocessing-based I/O is found. If an RQE is assigned, the TCB is checked for an equal condition. If the equal condition is found, the UCB is checked for a teleprocessing-device indicator. If the device indicator is found, an ABEND is issued.

If there are no RQEs assigned for the terminating task, an SVC 3 is issued. If the assigned RQEs do not represent the teleprocessing-associated I/O, the Extended SVC routine issues the PURGE macro to call the Purge routine (SVC 16). If an IOB chain for the Restore routine (SVC 17) results, an ABEND is issued. If no IOB chain is built, an SVC 3 is issued.

APPENDIX B: ALTERNATE PATH RETRY

In systems with the alternate path selective retry option, when a device can be reached by more than one path and there is a failure of one of the paths, the others are automatically tried, one by one, either until the operation is successful or until the error is declared permanent. In addition, the operator is provided with a 'vary path' command by which he may add or remove paths to a device. The two alternate path retry functions are called 'selective retry' and 'vary path,' respectively.

The Selective Retry Function

Without alternate path retry, each time there is a channel failure and the Test Channel routine is entered preparatory to retrying the I/O activity, it selects a path for the retry from the alternate path table. The selected path may or may not be the failing channel, because the alternate path table is not changed after I/O errors.

With alternate path retry, the Test Channel routine refers to the path mask field of the unit control block for the requested device rather than to the alternate path table, and failing paths are removed from the path mask when channel errors occur.

Error recovery routines pass control to the Alternate Path Retry routine before attempting each restart. The Alternate Path Retry routine obtains and saves the original path mask from the requested device's unit control block in a table called the channel error block table. It then turns off the failing channel's bit in the channel mask field of the unit control block and returns control to the I/O error routine, which begins the retry attempts.

To prevent a situation where all paths would become unavailable, the Alternate Path Retry routine restores the original path mask to the unit control block if the last available path is about to be used. The I/O error routine may then initiate the retry cycle again, depending upon whether the specified number of retries has been reached.

The Vary Path Function

When the operator issues any command, job management command processing routines are entered. For the 'vary path' command, the Vary Path Command Processor routine is given control (Figure 63). It adds or removes paths to a device by setting bits in the path mask table of a unit control block on or off.

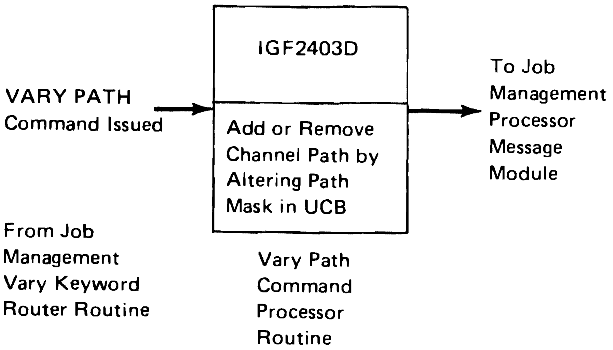


Figure 63. Vary Path Command Processing

APPENDIX C: DIRECT-ACCESS VOLUME VERIFICATION

If the direct-access volume verification (DAVV) option is selected during system generation, the input/output supervisor checks the serial numbers of newly mounted volumes against serial numbers in the unit control blocks (UCBs) for the devices containing the volumes. It issues messages to the operator when the wrong volumes have been mounted.

When an operator readies a device after mounting a volume, he causes an I/O interruption and entry to the I/O interruption supervisor. If the UCB for that device contains a volume serial number, the I/O interruption supervisor sets a flag in the UCB for the device to indicate that volume verification is to be performed. The next time there is a request for activity on the device, the I/O supervisor, having checked the flag, schedules module IGE0025E. When IGE0025E gains control, it checks the flag in the UCB to determine if volume verification is required. If it is, control is transferred to module IGE0125E, the first module of the two-module volume verification routine.

Module IGE0125E tests if the UCB volume serial number is zeros or if the data management bit is set. If either condition exists, an SVC 15 instruction is issued to execute the user's channel program. If, however, there is a volume serial number in the UCB and the mount bit is not on, module IGE0125E constructs a channel program to read the volume label for the mounted volume and issues an SVC 15 instruction to cause the channel program to be executed. When it receives control a second time, after the volume label has been read, module IGE0125E matches the volume serial number of the mounted volume against the serial number in the UCB for the device. When the serial numbers agree, IGE0125E uses an SVC 15 instruction to cause the originally requested activity to be performed. If the volume serial numbers do not agree, or if the channel program was terminated in error IGE0125E invokes the second module of the Volume Verification routine, IGE0225E. The second module issues a demount message for the mounted volume and a mount message for the volume whose serial number appears in the UCB.

If an I/O error occurs during reading of the volume label, 10 retries are attempted. If the condition cannot be corrected, IGE0125E invokes IGE0225E to issue an error message.

APPENDIX D: DYNAMIC DEVICE RECONFIGURATION

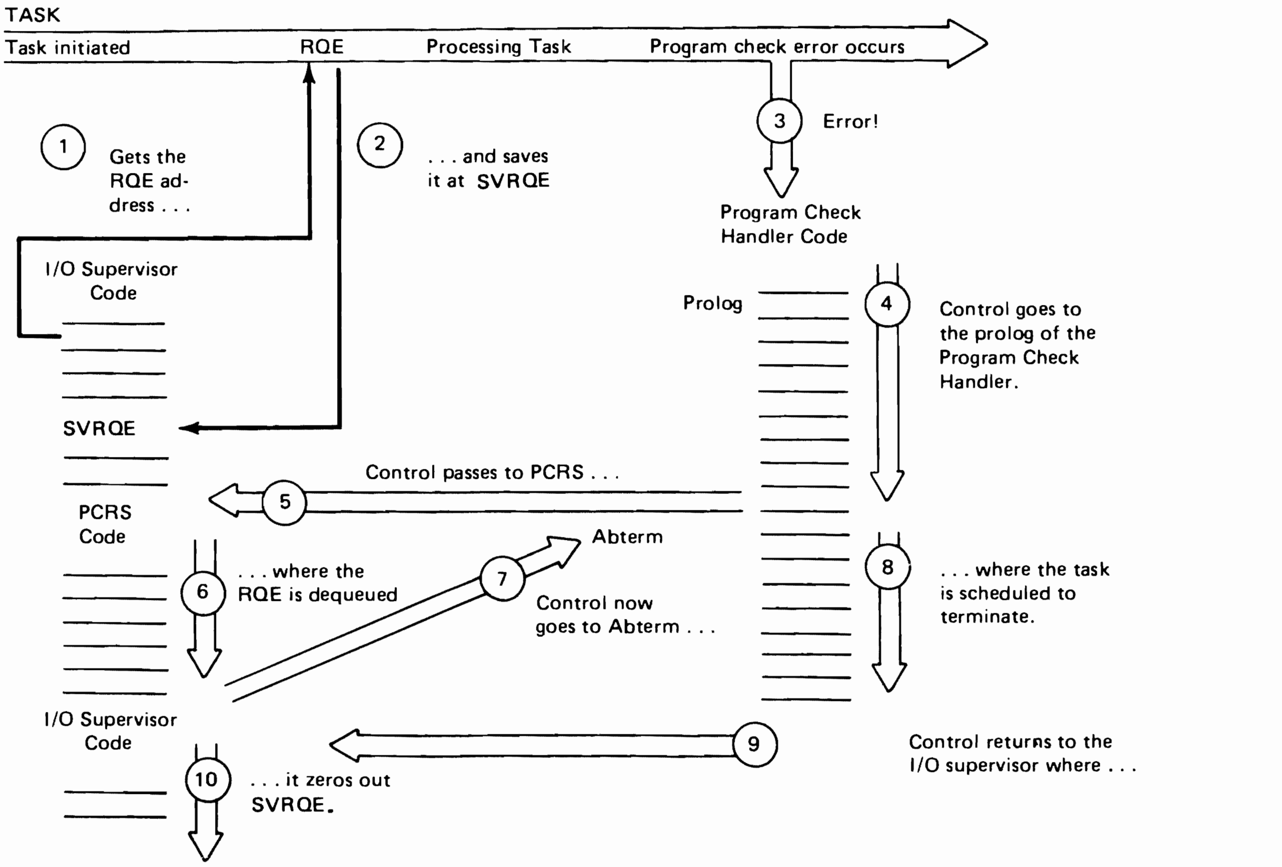
In systems with the dynamic device reconfiguration (DDR) option, a volume mounted and in use on one device can be removed and taken to another device where the activity on the volume will be resumed. Volumes can be moved at the request of an operator or, when there is a permanent I/O error, at the request of the system. Such moves can be made without restarting a job to cause device reallocation by job management routines, because I/O supervisor DDR routines effectively reallocate by exchanging the device-dependent information in the unit control blocks of the two already allocated devices. The affected devices may be contained in different logical channels, because DDR routines also transfer the request queue elements for any queued requests for the devices to the correct logical channel queues.

Refer to *OS/VS Recovery Management Logic* for detailed information on DDR.

APPENDIX E: PROGRAM CHECK RECOVERY SUBROUTINE

The Program Check Recovery Subroutine (PCRS) is assembled within I/O supervisor code. PCRS works with the two sections of the Program Check Handler, Prolog and ABTERM, to clean up the I/O supervisor control blocks and queues, and to terminate tasks. PCRs gains control from the Prolog section of the Program Check Handler when a program check error occurs in a task in the I/O supervisor, its appendages, or any routine branched to by the I/O supervisor. See Figure 64 for the general flow of control.

Preparations for processing a program check begin before an error occurs. The I/O supervisor, when it first gets control of an RQE, saves the address of the RQE in a special save area SVRQE. This allows the PCRS to determine the interrupted task without depending on the passing of registers between the routines which gain control at a program check. PCRS dequeues the RQE from its logical channel queue by using the address at SVRQE, and sets the flags in UCBFL1 to zero, to clear them for the next RQE. Finally, PCRS determines the associated TCB for the task, checks it validity, and determines the proper ABEND code. Control passes from PCRS to the ABTERM section of the Program Check Handler, which schedules the termination. The program check error handling ends when ABTERM gives control back to the I/O supervisor which places the RQE in the freelist and exits either to the SVC First Level Interruption Handler routine, if the program check occurred during an SVC 0, or to the Channel Restart routine, if the program check occurred during an SVC 15 or an I/O interruption. Now the I/O supervisor readies itself for a new RQE by zeroing out the special save area SVRQE.



TASK
Task initiated
RQE
Processing Task
Program check error occurs
1
Gets the RQE address . . .
2
. . . and saves it at SVRQE
3
Error!
Program Check Handler Code
I/O Supervisor Code
Prolog
4
Control goes to the prolog of the Program Check Handler.
SVRQE
Control passes to PCRS . . .
5
PCRS Code
Abterm
6
. . . where the RQE is dequeued
7
Control now goes to Abterm . . .
8
. . . where the task is scheduled to terminate.
I/O Supervisor Code
9
Control returns to the I/O supervisor where . . .
10
. . . it zeros out SVRQE.

Figure 64. Operation of PCRS During a Program Check

Two exceptional conditions may arise: there may be no RQE associated with the program check, indicated by the save area SVRQE being zero, and a recurrence may occur in PCRS.

When there is no valid RQE, PCRS determines whether an SVC 0 was in process, and if so, the task pointed to by the current TCB is abnormally terminated with the appropriate completion code. If there is no valid RQE and either an SVC 15 or interruption is in process, abnormal termination is not attempted.

In case of recurrence, the Program Check Recovery Subroutine determines if there is a valid RQE, and if so, determines if there is a valid TCB. If a valid RQE and TCB can be determined the task is abnormally terminated with the appropriate completion code. If there is no valid RQE or no valid TCB, processing is handled the same way as when there is no valid RQE.

APPENDIX F: SHARED DIRECT-ACCESS STORAGE DEVICE

The shared direct-access storage device (DASD) option allows one direct-access device to be shared between two CPUs. The I/O supervisor must, therefore, provide special code to allow successful data transfer between the device and each CPU. Since a program seeking access to a shared-file device may require either exclusive use of the device or shared use of the device, the I/O supervisor uses two special command codes, release and reserve. Reserve (X‘B4’) manipulates the switching device to allow exclusive use of the device by the CPU; release (X‘94’) manipulates the switching device to allow shared use of the device by the CPU.

A program requiring exclusive use of the shared device must issue a RESERVE macro. This causes the reserve count in the UCB to be incremented. Once the reserve command is issued, the other CPU has no access to the device until a release command is issued to the device. The I/O supervisor issues a release command if the reserve count field is zero. This count field is decremented each time the user issues a DEQ macro.

Regardless of whether or not the user has issued a RESERVE macro, the I/O supervisor must also issue a reserve command with every stand-alone seek, regardless of the value in the reserve count fields. This prevents the other CPU from moving the access mechanism once it has been positioned for the first CPU. If the reserve count is zero, a release is issued with the data transfer channel program to free the device for the other CPU.

If a unit check or a channel error requires a sense operation to be done, a read home address and record zero channel program is chained to the sense command; if the reserve count in the UCB is zero, the sense command is changed to a release command—a special type of sense command. The home address and record zero data, read into the UCB's work area, is required by the device-dependent error recovery procedure. The release command frees the device for possible use by the second CPU during the first CPU's error recovery cycle.

If an active shared device is associated with a purged request, the UCB's HIO flag is set by the purge routine. This causes the I/O supervisor to issue a release to the device, if its reserve count is zero.

APPENDIX G: I/O SUPERVISOR—OLTEP SYNCHRONIZING MODULE (IECIOLTS)

The Online Test Executive Program (OLTEP) requires the following special support from the I/O supervisor:

- Attention-interruption posting
- Device-end posting when device-end occurs separately from channel-end
- Return SIO condition codes when either of above functions is active
- Exclusive use of a channel by OLTEP
- Bypassing of the system channel programs for tape devices and direct access devices
- Specific exposure path selection for multiple exposure devices

The I/O supervisor maintains the module IECIOLTS which coordinates the I/O supervisor functions requested by OLTEP. The address of this routine is contained in the I/O supervisor-OLTEP vector table, IECOLTVT.

To indicate that OLTEP requires assistance from the I/O supervisor, the SVC 59 instruction sets a series of switches in the IECOLTSW field of IECOLTVT. The I/O supervisor exits from four places in its code to check these switches:

- It exits during the Test Channel routine.
- It exits during the Halt I/O routine.
- It exits during the Start I/O routine.
- It exits during the SIO module for multiple exposure devices.

If OLTEP indicates a channel function on a 2880 channel, control passes from the Test Channel routine in the I/O supervisor to the subroutine in IECIOLTS at label OLTCHN. Processing in that subroutine determines whether or not OLTEP has exclusive control of a channel.

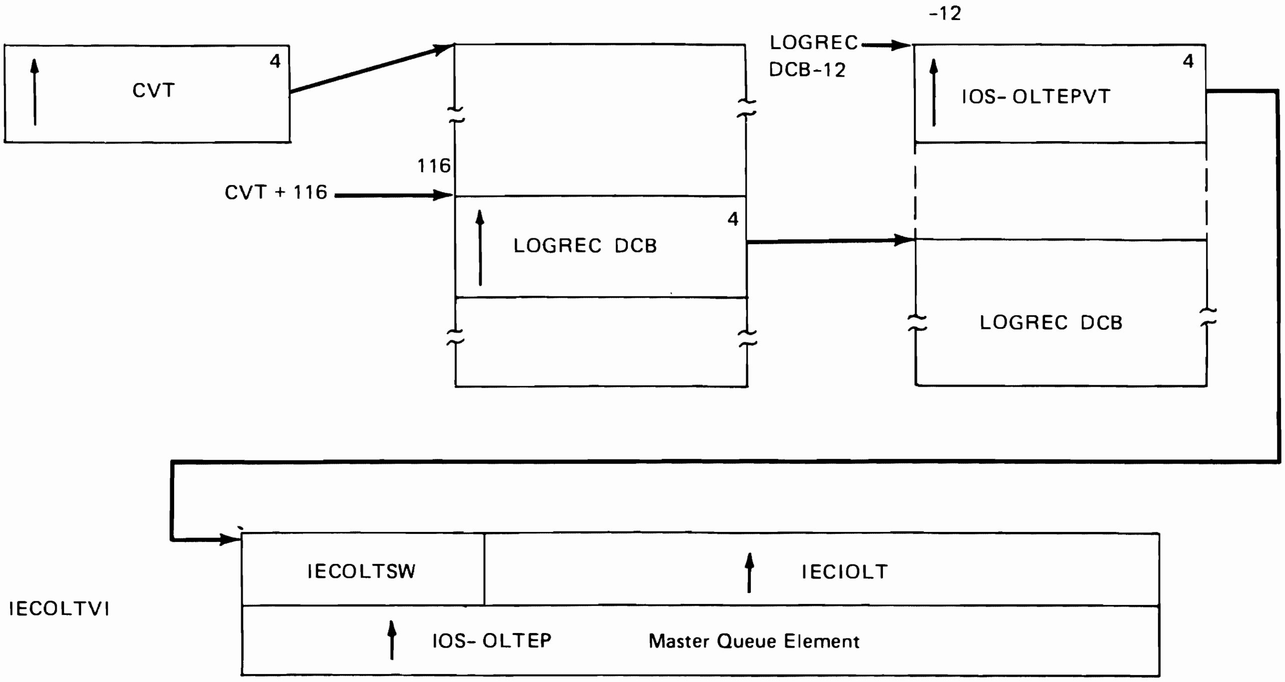
The SIO appendage in IECIOLTS at label SIOAPP is entered normally. This appendage checks the bypass function bit. If it is on, normal I/O channel programs are bypassed and OLTEP operations continue on that channel.

If OLTEP indicates either device-end or attention posting, control passes from the halt I/O routine in the I/O supervisor to the subroutine in IECIOLTS at label OLTHLT. This subroutine determines if IOS may issue an HIO on the input device.

Special OLTEP multiple exposure device code in the I/O supervisor exits to IECIOLTS at label OLTEXP to select a specific-exposure access path for OLTEP.

More information about the routines and appendages in IECIOLTS can be found in *OS/VS OLTEP Logic.*

The I/O supervisor uses the addressing scheme shown in Figure 65 to gain access to IECOLTVT.



Byte	Bit		Bit Checked By
1	1	Channel Function	Test channel routine in I/O supervisor
	. 1	Device-end posting	Halt I/O routine in I/O supervisor
	. . 1	Attention posting	Halt I/O routine in I/O supervisor
	. . . 1	Bypass function	SIO appendage in IECIOLTS
	. . . . 1 . . .	Exposure function	Exposure selection routine in IECIOLTS

Figure 65. IECIOLTS Addressing Scheme and Bit Settings

APPENDIX H: DEVICE-DEPENDENT ERROR ROUTINES

Device-dependent error routines gain control from the contents supervisor. See *OS/VS2 Supervisor Logic.* Even though each routine has specific characteristics tailored for each device type, the basic programming techniques are similar. Each routine sets the IOB error indicator bits, examines the sense and CSW status bits that are stored in the IOB to determine the type of error, and attempts to recovery from the error, if at all possible, by retrying the channel program by means of a direct branch for direct-access devices or an SVC 15 instruction for devices other than direct-access.

The IOB exception flag (IOBEX) and error flag (IOBERR) are turned on by all the device-dependent error routines. These settings serve a three-fold purpose: both flags on indicate that an error routine is in process; IOBEX on and IOBERR off indicate a permanent error; and both flags off indicate a successful retry. The tables included for each error routine explain the sense bit settings and describe when retry is or is not attempted.

The sense and CSW bits that are stored in the IOB are checked by the device-dependent error routines. By checking the IOBFL1 field of the IOB, chaining types are determined. If the IOBFL1 field indicates data and command chaining, no error retry is attempted; if it indicates command chaining; error retry is attempted from the address of the CCW which caused the error; and if it indicates data chaining or no chaining, the error is retried from the first CCW. By checking the CSW status bits in the IOB, the error routine determines the type of error that occurred. The bits tested, the priority of the testing, and the labels in the error routine to which control goes are shown in the tables listed for each device-dependent routine.

The device-dependent error routines attempt retry of the channel program by issuing an SVC 15 instruction. If the retry succeeds, the IOB exception bit and errors flags are reset to zero, and normal processing continues. The number of retries attempted depends on the device.

If the CSW status contains a unit check, the device-dependent routine (except for a 2305, 3330, and 3333) gives control to the statistics update routine to update the statistics table.

Writing Error Recovery Messages to the Operator

When an error is uncorrectable or when a condition exists that could be changed by operator action, an I/O error routine invokes the I/O supervisor's Write-to-Operator routine, which composes a message to be written on the console output device (Diagram 12). The Write-to-Operator routine handles three messages: Uncorrectable Input/Output Error (IEA000I), Inoperative Path (IEA001I), and Intervention Required (IEA000A). It uses a WTO macro instruction to cause them to be written on the console output device.

The I/O supervisor Write-to-Operator routine is contained in five modules. The first (IGE0025C) determines which modules to invoke and produces the 'intervention required' message. The second (IGE0125C) determines which message is to be written and invokes either the third (IGE0225C) or fifth (IGE0425C) load to produce the 'uncorrectable input/output error' message. Load four (IGE0325C) produces 'start I/O condition code 3 error' messages. The full text of each message is in *OS/VS Message Library: VS2 System Messages.*

Individual Routines

The routine descriptions that follow all have the same organization: a brief description of any characteristics of the routine or device that could be of use in interpreting the listings; a table, the Error Analysis Sequence Table, showing the order of examination of sense and status bits with pointers to the listings: and a table showing the meanings of IOB sense bits, flags, and error count fields for the particular device.

The tables are to be used as guides in getting to and interpreting the listings, which should be considered the final authority. Also:

- Cross references may sometimes point to approximately where in a listing some action is taken. This is because some functions cannot be grouped 'cleanly.' As a result, some studying may be required to check fully what happens when a particular condition arises.
- The explanations of sense bit meanings are meant to be quick-reference guides. More information can be found in the publications mentioned with each routine.
- The priority of examination of status and sense bits is a design priority. In some cases a variation will be found in the implementation.

The examination of status and sense bits is usually performed by a small utility-type routine called the Error Interpreter routine, which is used in common by the error routines. It determines which status or sense bits are on, and returns control to requesting error routines at the instruction sequences where the errors can be handled.

Each time the Error Interpreter routine is entered, it checks one bit. An arrangement of offset values and addresses in a list within the requesting I/O error routine directs the Error Interpreter. The list indicates which bits are to be tested and in what order, and it also contains the addresses of the instruction sequences to be used for 'on' conditions.

If a channel error has occurred, the error recovery routine that is entered will have available to it an 8-byte area called the error recovery procedure interface block. This is produced by the Channel Check Handler routine and includes information that could be of use in determining whether or not a restart should be attempted.

Descriptions of routines in the remainder of this appendix appear in numerical order according to the first (or only) device number indicated in the name of the routine. (Some routines serve more than one device, but the related routine description is included only once.) For example, "2260 and 1053 Error Routines" is included only once, among the 22xx routines; it is not also included among the 10xx routines. The table that follows indicates which devices (left column) are handled by which routines (right column).

Device	**Name of Routine**
1052 Printer	1052 Error Routine
1053 Printer	2260 and 1053 Error Routines
1275 Optical Reader Sorter	1419 and 1275 Error Routines
1287 Optical Reader	1287 and 1288 Error Routines
1288 Optical Page Reader	1287 and 1288 Error Routines
1403 Printer	1403 and 1443 Error Routines
1419 Magnetic Character Reader	1419 and 1275 Error Routines
1443 Printer	1403 and 1443 Error Routines
2250 Display Unit	2250 Error Routine
2260 Display Station	2260 and 1053 Error Routines
2305 Fixed Head Storage	2305, 2314, 2319, 3330, and 3333 Error Routines

2314 Direct-Access Storage Facility	2305, 2314, 2319, 3330, and 3333 Error Routines
2319 Direct-Access Storage Facility	2305, 2314, 2319, 3330, and 3333 Error Routines
2400 Series Magnetic Tape Units	2400 and 3400 Tape Series Error Routines
2495 Tape Cartridge Reader	2495 Error Routine
2501 Card Reader	2501 and 2520 Error Routines
2520 Card Read Punch	2501 and 2520 Error Routines
2540 Card Read Punch	2540 Error Routine
3211 Printer	3211 Error Routine
3330 Disk Storage	2305, 2314, 2319, 3330, and 3333 Error Routines
3333 Disk Storage and Control	2305, 2314, 2319, 3330, and 3333 Error Routines
3410 Magnetic Tape	2400 and 3400 Tape Series Error Routines
3420 Magnetic Tape	2400 and 3400 Tape Series Error Routines
3505 Card Reader	3505 and 3525 Error Routines
3525 Card Punch with Read and Punch Features	3505 and 3525 Error Routines

1052 Error Routine

Special considerations are necessary for errors on the IBM 1052 Printer-Keyboard. Messages can be issued through the Write-to-Operator routine only for read errors. The operator is notified of other types of errors by use of the console alarm bell.

The 1052 error routine attempts recovery from channel data checks. The 1052 error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The 1052 error routine uses bits M0 and M1 in the third byte of the IOB flags field to control its procedure on subsequent entries after an error. If both bits are set to 0, the Error Interpreter routine is used to determine the type of error. If M0 has been set to 1, a permanent error has occurred and control has been received from the Error EXCP routine to ring the console alarm. If M1 has been set to 1, 'intervention required' has been signaled, and the original channel program is to be retried.

The error analysis sequence for the 1052 is shown in Figure 66. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Figure 67. More information can be obtained from *IBM System/360 Component Descriptions and Operating Procedures: IBM 1052 Printer-Keyboard Model 7 with IBM 2150 Console,* GA22-6877.

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject
This bit is set when an invalid command code is detected. The IOB error flag is turned off and the IOB exception flag is turned on indicating a permanent error. Control is returned to the I/O supervisor via an SVC 15 instruction for abnormal termination.

Bit 1: Intervention Required
This bit is set when the printer runs out of forms or when the not-ready key has been depressed. The error routine places the control command to ring the console alarm in the reposition modifier field of the IOB. The modifier flag 1 is set in the IOB to signal the Unit Record SIO routine to build a CCW employing this command code. Bit M1 is

	Status	Sense			Applicable to:		
Priority	**Bit**	**Byte**	**Bit**	**Condition**	**Read**	**Write**	**Pointer**
1	45			Channel Control Check	X	X	ERR530
1	46			Interface Control Check	X	X	ERR530
2	47			Chaining Check	X	X	ERR524A
3	38			Unit Check	X	X	ERR501
4		0	7	Should Not Occur	X	X	ERR504
5		0	6	Should Not Occur	X	X	ERR504
6		0	5	Should Not Occur	X	X	ERR504
7		0	4	Should Not Occur	X	X	ERR504
8		0	3	Equipment Check	X	X	ERR506
9		0	1	Intervention Required	X	X	ERR509
10		0	2	Bus-Out Check	X	X	ERR510
11		0	0	Command Reject	X	X	ERR518A
12	44			Channel Data Check	X	X	ERR525
13	42			Program Check	X	X	ERR518A
14	43			Protection Check	X	X	ERR518A
15	39			Unit Exception	X		ERR518B
16	41			Incorrect Length	X	X	ERR518A

Figure 66. 1052 Error Analysis Sequence (Module IGE0000D)

set in the IOB and control returned by SVC 15. The intervention-required condition does not terminate a read or write operation that is already in progress.

Bit 2: Bus-Out Check

This bit is set when a parity error is detected on a command or data byte. The error routine sets the bus-out flag in the IOB and retries the user's channel program via SVC 15. If the error recurs, the control command to ring the console alarm is placed in the reposition modifier field of the IOB, and modifier flag 1 is set to signal the Unit

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	——	——	——	——
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	Modifier Flag 1	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL3	——	——	Write Error Count	Bus-Out Error Count	Control Bit M1	Message Type	Control Bit M0	Logout Flag
Error Counts IOBECT Byte 1	——	——	——	——	Multiple Console Support Retry	Multiple Console Support Retry	Multiple Console Support Retry	Channel Data Check and MCS Retry
Error Counts IOBECT Byte 2	——	——	——	——	——	——	——	Channel Control Check, Interface Control Check

Figure 67. 1052 Sense Bits, IOB Flags and, IOB Error Counts

Record SIO routine to construct a CCW with this command. IOB bit M0 is set and control returned via SVC 15. Five retries are attempted on console devices of systems with multiple console support.

Bit 3: Equipment Check
This bit is set when one of the following occurs:

- Keyboard parity error.
- Keyboard-printer compare check.
- Printer failed to take a mechanical cycle during a read or write operation.

If the error occurred on a read command, a permanent error is assumed and the Write-to-Operator routine is invoked; it writes a message (IEA000I) indicating failure to read input messages. For write errors, the error routine retries the channel program via SVC 15. On the second occurrence of the error, the console bell is rung via the procedure described above for bus-out check. Five retries are attempted on console devices of systems with multiple console support.

Bits 4-7: Should Not Occur
If any of these bits is set, a catastrophic error is assumed. A permanent error is signaled to the Unit Record SIO routine and control is returned via SVC 15. Five retries are first attempted on console devices of systems with multiple console support.

1287 and 1288 Error Routines

The IBM 1287 Optical Reader error routine (module IGE0011C), 1287 Error routine (module IGE0011C) and the IBM 1288 error routine (module IGE0011D) attempt recovery from channel data checks. They also examine the error recovery procedure interface block to determine whether they should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the 1287 and 1288 is shown in Figure 68. The meanings of sense bits, IOB flags, and IOB error counts for the devices are shown in Figure 69. More information can be obtained from the following publications:

- *IBM 1287 Optical Reader Component Description and Operating Procedures,* GA21-9064
- *IBM 1288 Optical Page Reader Model 1 Component Description,* GA21-9081

Sense Byte Meanings

Byte 0, Bit 0: Command Reject
This bit is set when the command is incorrect for the operating mode, such as a Mark Line command in document mode or a normal command in CE diagnostic mode. An invalid command sequence, such as two consecutive ejects, will also cause the bit to be set.

Byte 0, Bit 1: Intervention Required
This bit is set when the device is not in ready status.

Byte 0, Bit 2: Bus-Out Check
This bit indicates that invalid parity has occurred in a command or data.

Byte 0, Bit 3: Equipment Check
One of the following has occurred: (1) the device was unable to completely read a line or field, (2) the 1287 or 1288 could not locate the reference mark, or (3) the 1288 failed to find a timing mark.

Byte 0, Bit 4: Data Check
The optical reader has sent at least one reject character or substitute character.

Priority	Status Bit	Sense Byte	 Bit	Condition	Pointer
1	45			Channel Control Check	ERR0041
2	46			Interface Control Check	ERR0041
3	44			Channel Data Check	ERR0041
4	32			Control Unit End	ERR0041
5	38			Unit Check	ERR0041
6		1	3	Should Not Occur	ERR006
6		1	5	Should Not Occur	ERR006
6		1	6	Should Not Occur	ERR006
6		1	7	Should Not Occur	ERR006
7		1	0	Tape Mode (1287 only)	ERR006
8		0	7	Should Not Occur	ERR006
9		0	3	Equipment Check	ERR006C
10		0	6	Non-Recovery	ERR006C
11		0	1	Intervention Required	ERR006C
12		0	2	Bus-Out Check	ERR006C
13		0	4	Data Check	ERR006C
14		0	5	Overrun	ERR006C
15		0	0	Command Reject	ERR006C
16		1	4	Invalid Operation	ERR006C
17	47			Chaining Check	ERR004B1
18	42			Program Check	ERR004B1
19	43			Protection Check	ERR004B1
20	41			Incorrect Length	ERR004B1

Figure 68. 1287 and 1288 Error Analysis Sequence

Byte 0, Bit 5: Overrun

An overrun condition occurs when the channel fails to service the optical reader in time and at least one character is lost.

Byte 0, Bit 6: Non-recovery

The operator must reload and restart the optical reader because (1) the document or tape is jammed, (2) the runout key was depressed while a document or tape was being processed, or (3) the scanner door was open when the device was not in the line display mode.

Byte 0, Bit 7: Keyboard Correction

The 1287 has displayed at least one unreadable character for online correction.

Byte 1, Bit 0: Tape Mode

The 1287 Model 2 is operating in the tape mode.

Byte 1, Bit 1: End of Page (1288)

The bottom of the page has been detected while reading in the unformatted document mode.

Byte 1, Bit 1: Late Stacker Select (1287)

The Stacker Select command did not arrive in time and the document was placed into the reject stacker.

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	Non-Recovery	Keyboard Correction (1285, 1287 Tape Mode Only)
Sense Byte 1 (1287, 1288 Only)	Tape Mode (1287 Only)	Late SS or End of Page	No Document Found	——	Invalid Operation	——	——	——
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL3	——	——	——	——	——	Message Type	——	Logout Flag
IOBINCAM (Byte 1)	Data Check Count							
IOBINCAM (Byte 2)	Incorrect Length Count							
IOB Error Counts Byte 1	Equipment Check Count							
IOB Error Counts Byte 2	Overrun Error Count				Bus-Out Count	Chaining Check Count		

Figure 69. 1287 and 1288 Sense Bits, IOB Flags, and IOB Error Counts

Byte 1, Bit 2: No Document Found

A document did not enter the reading station after the last eject command and there was no jam.

Byte 1, Bit 3: Not Used

Byte 1, Bit 4: Invalid Operation

Invalid information was specified in the load format instruction. For example: bit 2, 3, 4, or 5 of the fourth byte represents bits not used; fewer than four bytes were transmitted; or an uninstalled font was specified in the CCW.

Byte 1, Bits 5-7: Not Used

1403 and 1443 Error Routines

The IBM 1403 Printer and IBM 1443 Printer error routine attempts recovery from the special condition where channel data checks occur with bus-out checks. The 1403 and 1443 error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the 1403 and 1443 is shown in Figure 70. The meanings of sense bits, IOB flags, and IOB error counts are shown in Figure 71. More information can be obtained from the following publications:

- *IBM 1403 Printer Component Description,* GA24-3073
- *IBM 1443 Printer Models 1 to 4 and N1; IBM 1445 Printer Models 1 and N1,* GA24-3120

	Status	**Sense**			
Priority	**Bit**	**Byte**	**Bit**	**Condition**	**Pointer**
1	45			Channel Control Check	ERR051
1	46			Interface Control Check	ERR051
2	47			Chaining Check	ERR071
3	38			Unit Check	ERR053
4		0	6	Should Not Occur	ERR052F
5		0	3	Equipment Check	ERR052F
6		0	1	Intervention Required	ERR054
7		0	2	Bus-Out Check	ERR056
8		0	7	Channel 9	ERR059
9		0	0	Command Reject	ERR052E
10	44			Channel Data Check	ERR067
11	42			Program Check	ERR063
12	43			Protection Check	ERR063
13	39			Unit Exception	ERR064
14	41			Incorrect Length	ERR068

The sequence shown above is for the 1403 without the Universal Character Set (UCS) feature, and for the 1443.

For 1403s with UCS, bits 4 and 5 of sense byte 0 mean 'data check' and 'parity check,' respectively. Their priority falls between 9 and 10 and 5 and 6, respectively.

9.1		0	4	Data Check	ERR052E
5.1		0	5	Parity Check	ERR052D

Figure 70. 1403 and 1443 Error Analysis Sequence (Module IGE0000G)

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set when one of the following occurs:

- A Read Backward command is received.
- A carriage instruction to space more than three lines is received.
- A carriage instruction to skip to channel 0, 13, 14, or 15 of the carriage control tape is received.
- Any command is received which the device is not designed to execute.

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check / Typebar Selection	Parity Error / Typebar Selection	——	Channel 9
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL3	——	Entry Bit	UCS Parity Error Count	Bus-Out or Channel Data Check Error Count	——	Message Type	——	Logout Flag
Error Counts IOBECT Byte 1	——	——	——	——	Multiple Console Support Retry	Multiple Console Support Retry	Multiple Console Support Retry	Multiple Console Support Retry
Error Counts IOBECT Byte 2	——	——	——	——	——	——	——	Channel Control Check, Interface Control Check

Figure 71. 1403 and 1443 Sense Bits, IOB Flags, and IOB Error Counts

The error is considered permanent.

Bit 1: Intervention Required

This bit indicates a not-ready condition due to one of the following:

- The printer has run out of forms or the forms have jammed.
- The Stop Key has been depressed.
- The cover interlock switch is open.
- The typebar motor switch is set to the OFF or REMOVE position.

When this bit and bit 7 (Channel 9) are on, the error is handled as a Channel 9 condition. In all cases, an Intervention Required message is issued to the operator who must correct the condition. When the intervention required condition alone is corrected, the last operation is repeated.

Bit 2: Bus-Out Check

This bit indicates that a parity error has occurred on a bus-out command or data byte. If this bit is set during the initial selection of a control unit or a device, the operation is retried. If it is set during channel end, the error is automatically considered permanent unless it occurs on the console device of a system having the Multiple Console Support feature, where it is retried five times.

Bit 3: Equipment Check

This bit indicates that a program-correctable malfunction was detected in the printer or in its controls. The malfunctions are buffer or hammer checks on the 1403 and typebar-synchronization errors on the 1443. These errors are reset by the next Write or Control command. Five retries are attempted on systems with multiple console support before the error is considered permanent, if the printer is being used as a console. Otherwise, the error is considered to be permanent, and no retry is attempted.

Bit 4: Data Check (1403 Only)

If the 1403 has the Universal Character Set (UCS) feature, this bit is set when a code in a data record sent to the printer does not match a code in the UCS feature storage.

(Without UCS, this bit should not be set.) The error is automatically considered permanent unless it occurs on the console device of a system having the Multiple Console Support feature, where it is retried five times.

Bit 5: Parity Error (1403 Only)
If the 1403 has the Universal Character Set (UCS) feature, this bit indicates a parity error was detected in data being written into or read from UCS feature storage. If the error occurs while the UCS storage is being loaded, one retry is attempted. If it occurs at any other time, the error is considered permanent. In systems having the Multiple Console Support feature, five retries are attempted for console devices.

Bits 4 and 5: Typebar Selection (1443 Only)
The combination of these two bits indicates the position of the typebar selector switch.

Bit 4	Bit 5	Switch Setting
0	0	52-character set
0	1	13-character set
1	0	39-character set
1	1	63-character set

These bits can be changed only by repositioning the typebar selector switch. They are considered normal, and the error routine continues the channel program.

Bit 6: Should Not Occur
If this bit is set, a catastrophic error is assumed. The logout flag is set in the IOB, a permanent error is signaled to the Error EXCP routine, and control is returned via SVC 15.

Bit 7: Channel 9
This bit is set when a hole is sensed in channel 9 of the carriage control tape.

1419 and 1275 Error Routines

The IBM 1419 Magnetic Character Reader and IBM 1275 Optical Reader Sorter error routine attempts recovery from channel data checks. The 1419/1275 error routine also examines the error recovery procedure inteıface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence is shown in Figure 72. The meanings of sense bits, IOB flags, and IOB error counts are shown in Figure 73. Sense byte 2 is applicable only to the secondary control unit of systems with the Dual Address Adapter feature.

More information can be obtained from the following publications:

- *IBM 1219 Reader Sorter, IBM 1419 Magnetic Character Reader,* GA24-1499
- *IBM 1419 Magnetic Character Reader and IBM 1275 Optical Reader Sorter, Device-Dependent BSAM Program Logic Manual,* GY21-0012

Sense Byte Meanings

Byte 0, Bit 0: Command Reject
This bit is set when an invalid command is received. Invalid commands include:

- Two Read commands without an intervening Stacker Select command when the 1419 is in program-sort mode
- A Stacker Select command given for an auto-selected document
- A second Stacker Select command after one has been accepted for a document
- A Write command given when the machine is not in diagnostic mode

	Status	Sense			
Priority	Bit	Byte	Bit	Condition	Pointer
1	45			Channel Control Check	ERR020
2	46			Interface Control Check	ERR020
3	44			Channel Data Check	ERR020
4	38			Unit Check	ERR020
5		0	3	Should Not Occur	ERR051
6		0	7	Document Spacing Error	ERR051
7		0	1	Intervention Required	ERR051
8		0	2	Bus-Out Check	ERR051
9		0	4	Data Check	ERR051
10		0	5	Overrun	ERR051
11		0	6	Auto Select	ERR051
12		0	0	Command Reject	ERR051
13	47			Chaining Check	ERR069
14	42			Program Check	ERR069
15	43			Protection Check	ERR069
16	41			Incorrect Length	ERR069

For the secondary control unit, the following sense bytes are examined in place of those shown above:

5		2	2	Bus-Out Check	ERR061
6		2	4	Should Not Occur	ERR061
7		2	3	Should Not Occur	ERR061
8		2	1	Intervention Required	ERR061
9		2	7	Operator Attention	ERR061
10		2	0	Command Reject	ERR061
11		2	5	Late Stacker Select	ERR061
12		2	6	Auto Select	ERR061

Figure 72. 1419/1275 Error Analysis Sequence (Module IGE0011E)

Byte 0, Bit 1: Intervention Required

This bit indicates that operator attention is needed for one or more of the following reasons:

- Document jam
- Full stacker
- Sort-check
- Endorser stop
- End-of-transport stop
- Film stop
- Batch number advance check stop
- Motor not running

Byte 0, Bit 2: Bus-Out Check

This bit is set for parity errors on information coming from the CPU via the interface.

Byte 0, Bit 3: Should Not Occur

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	——	Data Check	Overrun	Auto-Select	——
Sense Byte 1	——	——	Document Under Read Head	Amount Field Valid	Process Control Field Valid	Account Number Field Valid	Transit Field Valid	Serial Number Field Valid
Sense Byte 2 (Secondary Control Unit Only)	Command Reject	Intervention Required	Bus-Out Check	——	——	Late Stacker	Auto-Select	Operator Attention
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	——
IOBFL2	——	Sense Bit	Purge Flag	——	——	——	——	——
IOBFL3	——	——	——	——	——	Permanent Error	——	Logout Flag

Figure 73. 1419/1275 Sense Bits, IOB Flags, and IOB Error Counts

Byte 0, Bit 4: Data Check
This bit indicates that one or more of the selected fields in the document was not read correctly.

Byte 0, Bit 5: Overrun
This bit is set when a character is not accepted. The field containing the error is identified by a 0 in bits 3 to 7 of sense byte 1.

Byte 0, Bit 6: Auto-Select
This bit is set when a document is automatically selected into the reject pocket. A 51-column card turns the indicator on if the 51-column feature is not installed. If a Stacker Select command is issued for an auto-selected document, the command reject bit will be set.

Byte 0, Bit 7: Should Not Occur

Byte 1, Bit 0: Should Not Occur

Byte 1, Bit 1: Should Not Occur

Byte 1, Bit 2: Document Under Read Head
This bit is normally used in diagnostic mode only.

Byte 1, Bit 3: Amount Field Valid —When this field is selected at the operator panel, and is read without error (including symbols), the bit is set to one.

Byte 1, Bit 4: Process Control Field Valid —When this field is selected at the operator panel, and is read without error (including symbols), the bit is set to one.

Byte 1, Bit 5: Account Number Field Valid —When this field is selected at the operator panel, and is read without error (including symbols), the bit is set to one.

Byte 1, Bit 6: Transit Field Valid —When this field is selected at the operator panel, and is read without error (including symbols), the bit is set to one.

Byte 1, Bit 7: Serial Number Field Valid —When this field is selected at the operator panel, and is read without error (including symbols), the bit is set to one.

Byte 2 (Secondary Control Unit Only):

Byte 2, Bit 0: Command Reject
This bit is set when an invalid command is received by the secondary control unit (SCU). The following commands are considered invalid in the SCU:

- Read
- Read Backwards
- Write

Byte 2, Bit 1: Intervention Required
See byte 0, bit 1.

Byte 2, Bit 2: Bus-Out Check
This bit is set for parity errors on information coming from the CPU via the interface.

Byte 2, Bit 3: Should Not Occur

Byte 2, Bit 4: Should Not Occur

Byte 2, Bit 5: Late Stacker Select.
This bit is set when a Stacker Select command is given for a document which has passed the select station. The document is rejected.

Byte 2, Bit 6: Auto-Select
This bit is set when a Stacker Select command is issued for a document that is auto-selected.

Byte 2, Bit 7: Operator Attention
This bit is set when the Update switch is off and a Stacker Select command is issued to effect batch-numbering update.

2501 and 2520 Error Routines

The IBM 2501 Card Reader and 2520 Card Read Punch error routine attempts recovery from channel data checks on 2501 and 2520 read errors. Each read operation is retried once.

The error analysis sequence is shown in Figure 74. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Figure 75. More information about the individual devices can be obtained from the following publications:

- *IBM 2501 Models B1 and B2 Component Description and Operating Procedures,* GA21-9026
- *IBM 2520-B1, B2, and B3 Component Description and Operating Procedures,* GA21-9027

Priority	Status Bit	Sense Byte	Bit	Condition	Pointer
1	45			Channel Control Check	ERR002
1	46			Interface Control Check	ERR002
2	38			Unit Check	ERR002
3		0	6	Should Not Occur	ERR004
4		0	3	Equipment Check	ERR008
5		0	7	Should Not Occur	ERR004
6		0	1	Intervention Required	ERR036
7		0	2	Bus-Out Check	ERR013
8		0	4	Data Check	ERR017
9		0	5	Overrun	ERR020
10		0	0	Command Reject	ERR006
11	44			Channel Data Check	ERR035
12	47			Chaining Check	ERR029
13	42			Program Check	ERR029
14	43			Protection Check	ERR029
15	39			Unit Exception	ERR029
16	41			Incorrect Length	ERR029

Figure 74. 2501 and 2520 Error Analysis Sequence (Module IGE0000E)

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set when a Read Backward command is issued, or when any other command is received which the device has not been designed to execute. The error is considered permanent.

Bit 1: Intervention Required

This bit is set when one of the following occurs:

- The power is off.
- Cards are not registered at the read station.
- The stacker is full.
- The feed check light is on.
- The stop key has been depressed.
- The chip box is full, or has been removed.
- There are no cards in the hopper and the End-of-File light is not on.
- The cover interlock switch is open.

A message is given to the operator, who must take action. Upon correction of the condition, the interrupted operation is repeated.

Bit 2: Bus-Out Check

This bit is set when a parity error has occurred on bus-out during transfer of command or data bytes, but not during the time period of address-out or command-out proceed. For a command byte one retry is attempted. If the error is not corrected it is considered permanent. For a data byte, the card is already punched and the error is considered permanent. However, on a 2501, the error is automatically retried once.

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	———	———
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	———	———	Exceptional Condition	———	0 Start 1 Restart
IOBFL3	———	Entry Bit	Read Error Count	Bus-Out Error Count	Data Check Flag	Message Type	Overrun Count	Logout Flag

Figure 75. 2501 and 2520 Sense Bits, IOB Flags, and IOB Error Counts

Bit 3: Equipment Check

This bit is set when one of the following occurs:

- An invalid card code is detected during a punch operation.
- During a read or punch operation an error is detected during the 9-bit match.

The invalid card code part of equipment check is not set during card image punch.

If the error occurs during a punch operation other than QSAM, it is automatically considered permanent. With QSAM an error occurring during a punch operation is retried. If it occurs during a read operation, one retry is attempted.

Bit 4: Data Check

This bit is set when an invalid card code is detected during a read operation. This error pertains to the last card for which data was sent. A message is typed and an operator must reposition the cards for one retry. If the error persists, it is considered permanent.

Bit 5: Overrun

This bit is set if during a read operation the interface has not transmitted a character by the time the next character is to be read into the register. The operator must reposition the cards. The operation is retried once and if the error persists it is considered permanent, and a message is written to the console.

Bits 6 and 7: Should Not Occur

If either of these bits is set, a catastrophic error is assumed. A permanent error is signaled to the Error EXCP routine and control is returned via SVC 15.

2250 Error Routine

The IBM 2250 Display Unit error routine attempts recovery from channel data checks. The 2250 error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the 2250 is shown in Figure 76. The meanings of sense bits, IOB flags, and IOB error counts are shown in Figure 77. More information can be obtained from the following publications:

- *IBM System/360 Component Description: IBM 2250 Display Unit Model 1,* GA27-2701

- *IBM System/360 Component Description: IBM 2250 Display Unit Model 2; IBM 2840 Display Control Model 1,* GA27-2702

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject
This bit is set when there is an invalid modifier bit in a command or an invalid invalid command sequence. The error is considered permanent.

Bit 1: Should Not Occur
When this bit is set, a catastrophic error is assumed. The logout flag in the IOB is set and the permanent error procedure is performed.

Bit 2: Bus-Out Check
This bit is set when a parity error is detected on a command or data byte during bus-out. The operation is retried once. If the retry is unsuccessful, a message is written to the operator.

Bit 3: Equipment Check (Model 2); Should Not Occur on Others (See Bit 1).

Bit 4: Data Check
This bit is set when a buffer parity error is detected either during a read operation or during image regeneration. The operation is retried once. If the retry is unsuccessful, a message is written to the operator.

Bit 5: Should Not Occur (See Bit 1)

Bit 6: Buffer Running
This bit indicates that regeneration is in process. When accompanied by Command Reject, a permanent error is assumed.

Bit 7: Should Not Occur (See Bit 1)

	Status	Sense			Applicable to		
Priority	Bit	Byte	Bit	Condition	2250-1	2250-2	Pointer
1	45			Channel Control Check	X	X	ASRON
2	46			Interface Control Check	X	X	ASRON
3	44			Channel Data Check	X	X	TESTST
4	38			Unit Check	X	X	MAINER
5		0	1	Should Not Occur	X		SEROUT
5		0	3	Should Not Occur	X	X	SEROUT
5		0	5	Should Not Occur	X	X	SEROUT
5		0	7	Should Not Occur	X	X	SEROUT
6		0	2	Bus-Out Check	X	X	B01CHK
7		0	4	Data Check	X	X	DATACX
8		0	0	Command Reject	X	X	PERMER
		0	0	Command Reject	Note 1		PERMER
9		0	6	Buffer Running	X	X	
10	42			Program Check	X	X	PERMER
11	43			Protection Check	X	X	PERMER
12	41			Incorrect Length	X	X	PERMER

Note: For an unbuffered 2250 Model 1 the following changes are necessary:

a. Command Reject with Buffer Running is a 'Should Not Occur' condition with Priority 5, Pointer SEROUT.

b. Priorities 10, 11, and 12 become 9, 10, and 11, respectively.

Figure 76. 2250 Error Analysis Sequence (Module IGE0010A)

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	——	Bus-Out Check	Equipment Check (Model 2)	Data Check	——	Buffer Running	——
Sense Byte 1	Light Pen Defect	End Order Sequence	Character Mode	——	——	2840 Output Check	2840 Input Check	——
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL2	Halt I/O Issued	Sense Flag	——	——	——	——	Film Unit Flag	——
IOBFL3	——	——	——	——	——	Message Type	——	Logout Flag
IOB Error Counts Byte 1	Bus-Out 1 Retry Indicator	Bus-Out 2 Retry Indicator	Datc Check	Equipment Check	2840 Input Check	2840 Output Check	Abnormal End Appendage Bit	Channel Data Check
IOB Error Counts Byte 2	Interface Control Check or Channel Control Check	——	——	——	——	——	——	——

Figure 77. 2250 Sense Bits, IOB Flags, and IOB Error Counts

2260 and 1053 Error Routines

The IBM 2260 Display Station and IBM 1053 Printer error routine attempts recovery from channel data checks. The 2260 and 1053 error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the 2260 and 1053 is shown in Figure 78. The meanings of sense bits, IOB flags, and IOB error counts are shown in Figure 79. More information can be obtained from the publication *IBM System/360 Component Description: IBM 2260 Display Station; IBM 2848 Display Control,* GA27-2700.

	Status	Sense			Applicable to			
Priority	Bit	Byte	Bit	Condition	2260	1053	Pointer	Load[1]
1	45			Channel Control Check	X	X	ASRON	1
2	46			Interface Control Check	X	X	ASRON	1
3	44			Channel Data Check	X	X	TESTST	1
4	38			Unit Check	X	X	MAINER	1
5		0	4	Should Not Occur	X	X	SEROUT	1
5		0	5	Should Not Occur	X	X	SEROUT	1
5		0	6	Should Not Occur	X	X	SEROUT	1
6		0	3	Equipment Check	X		EC	1
7		0	1	Intervention Required		X	2260-SEROUT	1
8		0	2	Bus-Out Check Initial Selection	X	X	B01	1
8		0	2	Bus-Out Check Data Transfer	X		ISBUSOUT	1
8		0	2	Bus-Out Check Data Transfer		X	ISBUSOUT	1
9		0	0	Command Reject	X	X	PERMER	1
10	42			Program Check	X	X	PERMER	1
11	43			Protection Check	X	X	PERMER	1
12	41			Incorrect Length	X	X	PERMER	1

[1] Only first-time equipment check errors are handled by load 2.

Figure 78. 2260 and 1053 Error Analysis Sequence (Load 1—IGE0010B or Load 2—IGE0100B)

Sense Byte Meanings and Actions Taken

Bit 0: Command Reject. This bit is set when there is an invalid modifier bit in a command, or an invalid command sequence. The error is considered permanent.

Bit 1: Intervention Required
This bit is set when a 1053 Write command is given but the 1053 is not ready. A message is written to the operator.

Bit 2: Bus-Out Check
This bit is set when a parity error is detected on a command or data byte during bus-out. Processing depends upon when the bus-out check occurred and what command was last executed:

If the bus-out check occurred during initial selection, or during data transmission for the 2260 after a Write Line Address or an Erase command, one retry is attempted. If the retry is unsuccessful a message is written to the operator.

If the bus-out check occurred during data transmission for the 2260 after a Write Buffer Storage command, one retry is attempted, but before that retry an Erase Buffer Storage command is issued. If the retry is unsuccessful, a message is written to the operator.

Bit 3: Equipment Check
This bit is set when a parity error is detected during a manual read input operation. The second load of the 2260 and 1053 error routine erases the message in error and displays an error message on the screen. No automatic retry occurs. If a retry is desired, the necessary coding must be included in the user's program. (If the error occurs a second time, the user's program should consider it permanent.)

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	——	——	——	——
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL2	——	Sense Flag	——	——	——	——	Film Unit Flag	——
IOBFL3	——	——	——	——	——	Message Type	——	Logout Flag
IOB Error Counts Byte 1	Bus-Out Count 1	Bus-Out Count 2	Bus-Out Count 3	Error Routine Channel Program	——	Channel Data Check	Abnormal End Appendage Bit	Check
IOB Error Counts Byte 2	Interface Control Check or Channel Control Check	——	——	——	——	——	——	——

Figure 79. 2260 and 1053 Sense Bits, IOB Flags, and IOB Error Counts

Bits 4-7: Should Not Occur

If one of these bits is set, a catastrophic error condition is assumed. The logout bit in the IOB is set, and a permanent error procedure is performed.

2305, 2314, 2319, 3330, and 3333 Error Routines

This routine is resident and is generated by a macro during system generation to service the types of devices at an installation.

This routine attempts recovery from channel data checks. It also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

Channel programs are usually restarted from the beginning to avoid a repositioning problem, command and data chaining problems, and to simplify the handling of errors within errors.

When a 'track condition check' error occurs, the home address record and record 0 are read to determine whether the track is defective or is an alternate track. A bit in the UCB is checked to determine whether the home address and record 0 have already been read by DSS; if not, ERP does the read. If the track is defective, the address of the alternate track is used in a Seek command, and the the operation is resumed on the alternate track. If the track condition check occurred on an alternate track, the defective track's address, plus 1, is used in a Seek command and the operation is resumed on the new track.

When a 'no-record-found' error occurs, a console message is not issued if the access arm has been positioned at the correct track. A 'permanent error' indicator is set in the input/output block.

When the overflow incomplete bit (sense byte 1, bit 7) is set, only a partial record has been read or written, and a CCW is constructed so the remainder of the record can be processed. When the 'overflow incomplete' bit is set and the 'file mask violation', 'end-of-cylinder', or 'track condition check' bit is also set, the error routine assumes that the first record of the continuation track is properly identified as record number 1.

This error routine handles cylinder and head switching for both sequential and split cylinders.

A bit in the CVT is checked prior to the ERP attempting to cause any transients to be loaded. This bit is turned on by NIP at IPL time and turned off when NIP has proceeded far enough to allow transients to be loaded.

When a permanent I/O error is detected for the Paging Supervisor, a Deferred Incident Record is built by the ERP for subsequent recording into SYS1.LOGREC. This record contains, essentially, the same information as the non-Paging Supervisor permanent I/O SYS1.LOGREC record. See *OS/VS SYS1.LOGREC Error Recording Logic* for more information about error recording.

When a 2305, 3330, or 3333 presents a unit check, IOS performs a sense I/O command for 24 bytes and then enters the resident direct access ERPs. The ERP then checks the error indications in the CSW and sense bits according to the following precedence table (Figure 81) until a bit is found on. The action referred to will then be performed.

The control units for a 2305, 3330, and 3333 have an error correction capability known as the Error Correction Function, or ECF. If a data check occurs in a count or key area, the control unit performs ECF internally. If a data check occurs in the data field, the sense bytes contain a displacement and a 3-byte correction code for the ERP to use in correcting the error. The ECF supplied by a 3330, 3333, and 2305 corrects up to three contiguous bytes of data.

A 3330 or 3333 control unit presents the displacement to the error starting from the beginning of the data field, which allows the ERP to apply the correction code when data chaining is being performed in the data field. Because a 2305 control unit presents the displacement from the last byte transferred, the ERP only corrects the last segment if data chaining in the data field is used. If the error is not in the last segment, up to ten retries are performed, but the correction code is not applied.

For the Paging Supervisor and subsystem I/O, the ERP leaves Relocate Mode to apply the correction code.

The error analysis sequence for the IBM 2314 and 2319 Direct-access Storage Facility is shown in Figure 80. Figure 81 shows the error analysis sequence for the IBM 2305 Fixed Head Storage, 3330 Disk Storage, and 3333 Disk Storage and Control. The meanings of sense bits, IOB flags, and IOB error counts for all of the direct access devices are given in Figure 82. More information about the individual devices can be obtained from the following publications:

- *IBM System/360 Component Descriptions: 2314 Direct Access Storage Facility and 2844 Auxiliary Storage Control,* GA26-3599
- *IBM System/360 Component Descriptions: 2835 Storage Control and 2305 Fixed Head Storage,* GA26-1589
- *Reference Manual for 3830 Storage Control and 3330 Disk Storage,* GA26-1592
- *Reference Manual for 3333 Disk Storage and Control,* GA26-1615

Priority	Status Bit	Sense Byte	Bit	Condition	Pointer
1	45			Channel Control Check	ERNT
2	46			Interface Control Check	ERNT
3	44			Channel Data Check	ERNT
4		0	3	Equipment Check	ERNT
5		1	4	No Record Found	ERNT
6		0	7	Seek Check	ERNT
7		0	1	Intervention Required	ERNT
8		0	2	Bus-Out Check	ERNT
9		0	4	Data Check	ERNT
10		0	5	Overrun	ERNT
11		1	6	Missing Address Markers	ERNT
12		0	0	Command Reject	ERNT
13		0	6	Track Condition Check	ERNT
14		1	1	Track Overrun	ERNT
15		1	2	End of Cylinder	ERNT
16		1	5	File Protect	ERNT
17	38			Unit Check	ERNT
18	47			Chaining Check	ERNT
19	42			Program Check	ERNT
20	43			Protection Check	ERNT
21	39			Unit Exception	ERNT
22	41			Incorrect Length	ERNT

IEC23XXF logs statistics in the System Data Recording work area.

Figure 80. 2314 and 2319 Error Analysis Sequence (Module IEC23XXF)

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

When this bit and bit 5 of sense byte 1 (File Protected) are set, the write inhibit portion of the file mask has been violated.

When this bit and bit 3 of byte 1 (Invalid Command Sequence) are set, one of the following has occurred:

- A Write command was not preceded by the necessary Search or Write command.
- A Set File Mask, Reserve, or Release command has been issued in a chain where a previous Set File Mask command was given.
- Head switching is being attempted in a command chain not containing a previous seek.
- Space count has been chained from a Write command.
- A formatting command is being attempted after record 0 on a defective track or following a record which is flagged as an overflow record.

When this bit and bit 7 of byte 0 (seek check) are set, the 2841 detected an invalid seek address or was given a seek address consisting of fewer than six bytes. A seek is not initiated.

	Status	Sense			
Priority	Bit	Byte	Bit	Condition	Pointer
1	45			Channel Control Check	ERNT
2	46			Interface Control Check	ERNT
3	44			Channel Data Check	ERNT
4	47			Chaining Check	ERNT
5		1	0	Permanent Error	ERNT
6		0	3	Equipment Check	ERNT
7		0	2	Bus-Out Check	ERNT
8		0	1	Intervention Required	ERNT
9		0	0	Command Reject	ERNT
10		1	4	No Record Found	ERNT
11		0	5	Overrun	ERNT
12		1	1	Invalid Track Format	ERNT
13		0	4	Data Check	ERNT
14		1	2	End of Cylinder	ERNT
15		1	5	File Protect	ERNT
16		1	7	Overflow	ERNT
17	38			Unit Check	ERNT
18	42			Program Check	ERNT
19	43			Protection Check	ERNT
20	39			Unit Exception	ERNT
21	41			Incorrect Length	ERNT

IEC23XXF logs statistics in the System Data Recording work area.

Figure 81. 2305, 3330, and 3333 Error Analysis Sequence (Module IEC23XXF)

When the 'command reject' bit is on and the File Protected, Invalid Command Sequence, or Seek Check bits mentioned above are not on, one of the following has occurred:

- An invalid command was given.
- An invalid file mask was given.
- The sum of a key length plus data length exceeds $2^{16}-1$.
- An IPL command was given after a Set File Mask command.
- Command out has been presented in response to a request for the first byte of a Write Home Address CCW.

Bit 1: Intervention Required

This bit indicates that the device is not physically attached to the system, or is physically attached but is not available for use because the file motor is not on, a cover is open, etc.

Bit 2: Bus-Out Check

This bit is set when a parity error is detected during information transfer from the channel to the control unit. The check is an odd parity check which is made on control, write, and search operations. (Parity errors which are detected during command transfer result in bus-out checks and not command reject.) Ten retries are attempted. If the error remains uncorrected, a message is written to the operator and the control unit is considered inoperative.

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0 2305, 3330, 3333	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	———	———
Sense Byte 0 2314, 2319	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	Track Condition Check	Seek Check
Sense Byte 1 2305, 3330, 3333	Permanent Error	Invalid Track Format	End of Cylinder	———	No Record Found	File Protected	Write Inhibit (3330 and 3333 only)	Operation Incomplete
Sense Byte 1 2314, 2319	Data Check in Count Area	Track Overrun	End of Cylinder	Invalid Command Sequence	No Record Found	File Protected	Missing Address Market	Overflow Incomplete
Sense Byte 2 2305, 3330, 3333	Buffered Log Full (2305 only)	Correctable	———	Environmental Data Present (3330 and 3333 only)	———	———	———	———
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	———	———	Exceptional Condition	Overflow Indicator	0 Start 1 Restart
IOBFL2	Halt Input/ Output	Sense Bit	Purge Flag	Read Home Address Flag	No End Extent Flag	Track Address Update Flag	———	———
IOBFL3	Indicator 1	Track Condition Flag	No Record Found	Bus-Out Error Count	Restore Flag	Message Type	———	Log-Out Flag

Figure 82. 2305, 2314, 2319, 3330, and 3333 Sense Bits, IOB Flags, and IOB Error Counts

Bit 3: Equipment Check

This bit indicates a malfunctioning control unit or device. A message is written to the operator. Except for 2305, 3330, and 3333, the conditions that cause this bit to be set are defined in sense byte 2, bits 0, 2, 4, and 5.

Bit 4: Data Check

This bit is set when an error is defected in the information received from the device. Data Check will usually occur when an attempt is made to read a record which overflows a track. For 2305, 3330, and 3333, if the correctable bit (byte 2, bit 1) is on, the Error Correction Function is used.

Bit 5: Overrun

This bit is set when a chained CCW is received too late to be properly executed or when channel response is too slow during data transfer. Ten retries are attempted. If the retries are unsuccessful the error is considered permanent and a message is written to the operator. An overrun condition always results in an immediate stop of data transmission. For Write operations, the record area is padded with zeros.

Bit 6: Track Condition Check

This bit is set when one of the following conditions has occurred:

- Any single track command other than Search Home Address, Read Home Address, or Read Record 0 is executed on a defective track.
- Any multitrack command other than Search Home Address, Read Home Address, or Read Record 0 causes a switch to a defective track, or an overflow operation is attempted to a defective track.
- Any multitrack command or overflow operation attempts to switch from an alternate, or defective track on which a read or search type command has been executed.

Bit 7: Seek Check

This bit is set when the device is unable to successfully complete a seek because:

- The seek address is invalid. Command Reject (byte 0, bit 0) is also set.
- The seek address consists of fewer than six bytes. Command Reject (byte 0, bit 0) is also set.
- The access mechanism has malfunctioned.
- The last three bytes at the track's home address are not identical to the last three bytes of the seek address.

2400 and 3400 Tape Series Error Routines

The IBM 2400/3400 Tape Series error routine uses two operations designed to clear or circumvent sections of the tape that are presumably contaminated or defective. These operations are (1) the tape cleaner action and (2) the erase gap action.

The tape cleaner action is a "shoe shining" operation in which the tape is run back and forth to produce a wiping action both at the read head and at the tape cleaner blade. This action transfers contaminants from the read head to the tape and from the tape to the cleaner blade.

If the tape is being read forward, the cleaner action consists of a backward motion (toward the supply reel) equal in length to five records, followed by a forward motion equal in length to four records, positioning the read/write head at the beginning of the record that was being read when the data check occurred.

If the tape is being read backward, the cleaner action consists of a backward motion equal in length to four records, followed by a forward motion equal in length to five records, positioning the read/write head at the end of the record that was being read when the data check occurred.

The erase gap action is performed whenever a write error is detected. It consists of erasing a 3-1/2 inch portion of the tape, starting at the beginning of the write area assumed to be defective. This action treats the error as unrecoverable; the gap is a detour around the defective area.

The noise bit (byte 1, bit 0) is set if a data check occurs and: phase encoding (PE) is used; or non-return-to-zero-inverse (NRZI) encoding is used. If a data check occurs and the noise bit is not set, it is assumed that the data check may have been caused by too short a record block. In this case, the record length is checked, and if it is less than 12 bytes, the record block is defined as a "noise block." Noise blocks are skipped and treated as permanent errors except when found by an integrated emulator on 7-track tapes; then all noise blocks are returned to the emulator for further processing. The DEBOFLGS field of the DEB identifies the tape as an emulator tape.

The error routines also treat parity errors differently on 7-track tapes being read by an integrated emulator. Rather than being a permanent error, the parity is switched (DEBVMOD field of the DEB) and the block reread in the alternate parity until 10 read-recovery sequences have been executed (40 retries) or the read is successful. After 10 read-recovery sequences, the parity is switched back to the original parity and the block is reread until 10 read-recovery sequences have been executed (a permanent error) or the read is successful.

When an ending status (channel end, device end, or unit check) appears in the channel status word, the 2400/3400 error routine increments the 'block count' field of the data control block by the amount shown in the 'block count increment' field of the input/output block (IOB).

If an error remains uncorrected after retry attempts, or if no retries are attempted, a message (IEA000I) is written to the operator. For all error conditions except 'command reject, load point, data converter check' and 'not capable,' the logout flag of the IOB is set before entry to the I/O supervisor's Write-to-Operator routine. This is an indication to the I/O supervisor's Write-to-Operator routine to invoke the Outboard Recorder after

	Status	Sense			Applicable to:				
Priority	Bit	Byte	Bit	Condition	Read	Write	Control	Pointer	Load[1]
1	45			Channel Control Check	X	X	X	ER2404B	4
2	46			Interface Control Check	X	X	X	ER2404B	4
3	38			Unit Check	X	X	X	ER2404B	4
4		0	3	Equipment Check	X	X	X	ER2404A	4
5		0	2	Bus-Out Check	X	X	X	ER2404A	4
6		0	1	Intervention Required	X	X	X	ER2404A	4
7		0	0	Command Reject	X	X	X	ER2404A	4
8		0	5	Overrun	X	X		ER2404A	4
9		1	4	Load Point	X	X		ER2404A	4
10		0	4	Data Check	X	X	X	ER2404A	4
11		7	4	Data Security Erase			X	ER2402A	2
12	44			Channel Data Check	X	X	X	ER2404A	4
13		0	7	Data Converter Check	X			ER2404A	4
14		1	7	Not Capable	X			ER2404A	4
15		5	3	PE ID Burst Check		X	X	ER2401A	1
16				No Previous Sense Bits On	X	X	X	ER2404A	4
17	47			Chaining Check	X			ER2404B	
18	42			Program Check	X	X	X	ER2404B	4
19	43			Protection Check	X			ER2404B	4
20	41			Incorrect Length	X	X		ER2404B	4

[1] Only errors that occur during Read-opposite recovery are handled by Load 3.

Figure 83. 2400/3400 Error Analysis Sequence (Load 1—IGE0000I, Load 2—IGE0100I, Load 3—IGE0200I, Load 4—IGE0300I, Load 5—IGE0400I, or Load 6—IGE0900I)

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	Word Count Zero	Data Converter Check
Sense Byte 1	Noise Bit	Unit Status A	Unit Status B	7-Track Tape Unit	Tape At Load Point	Unit in Write Status	File Protect Status	Not Capable
Sense Byte 2	———	———	———	———	———	———	Multi Error	Track Exists
Sense Byte 3	Read/Write Vertical Redundancy Check	Longitudinal Redundancy Check	Skew	Cyclic Redundancy Check	Skew Register Vertical Redundancy Check	Phase Encoding	Backward	C-Compare
Sense Byte 4	———	Reject Tape Unit	Read Clock	Write Clock	Delay Counter	C Sequence	B Sequence	A Sequence
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	Reposition Tape	Cyclic Redundancy Check Bit	Exceptional Condition	———	0 Start 1 Restart
IOBFL 2	———	Sense Bit	Purge Flag	———	Read/Write Unit Exception	Use Read Opposite Recovery CCW from IOB	———	———
IOBFL 3	Noise Message Given	IOB Entry Bit	Tape Cleaning Bit	Control Flag	Read Opposite Recovery	Message Type	Control Unit Busy	Logout Flag
IOB Error Counts Byte 1	Interface Control Check or Channel Control Check	Overrun, Bus-Out Check, Channel Data Check, Chaining Check			———	Cleaner Control Count		
IOB Error Counts Byte 2	Write Indicator	Read Data Check Counts						
					User ERG Data Check			
		Error Routine ERG Data Check			Write Check Counts			

Figure 84. 2400/3400 Sense Bits, IOB Flags, and IOB Error Counts

it writes the message. See *OS/VS SYS1.LOGREC Error Recording Logic* for information about outboard recording.

The error analysis sequence for the 2400/3400 is shown in Figure 83. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Figure 84. More information can be obtained from the following publications:

- *IBM System/360 Component Description: 2400 Series Magnetic Tape Units,* *2803/2804 Tape Controls, and 2816 Switching Unit, Model 1,* GA22-6866

- *IBM System/360 Component Description: 3803/3420 Magnetic Tape Subsystems,* GA32-0020
- *IBM 3410/3411 Magnetic Tape Subsystem Component Summary,* GA32-0015

Sense Byte 0 Meanings and Actions Taken

Byte 0 Bit 0: Command Reject

This bit is set when a command is received which the device has not been designed to execute. The error is considered permanent.

Byte 0 Bit 1: Intervention Required

This bit indicates a not-ready condition. Actions taken depend upon whether a device end status was also received:

> With no device end, unit status B (sense byte 1, bit 2) is examined. If 0, the device is assumed not to exist and the error is considered permanent. If unit status B is 1, a message is given the operator. When he readies the device, the operation is attempted again.
>
> With device end, if a Rewind Unload command was the last command executed, a successful completion is assumed and processing continues. Otherwise, the condition is ignored and the scan of sense bits is continued.

Byte 0 Bit 2: Bus-Out Check

This bit is set when even parity appears on the information bus lines from the channel to the control unit. The command is attempted again. The tape is first repositioned if the bus-out check occurred during a write operation.

Byte 0 Bit 3: Equipment Check

This bit is set when a unit fails to respond to a set read or a set write status when instructed, or becomes not ready during execution of a tape motion operation. The error is considered permanent.

Byte 0 Bit 4: Data Check

During a read or read backward operation: If the noise bit (byte 1, bit 0) is off and the blocksize is less than 12 bytes, the noise block flag in the statistics update mask is set and regular operation is resumed with the next block (except when 7-track tapes are being read by an integrated emulator, in which case the noise block is passed back to the emulator).

If the noise bit is off, but the blocksize is 12 bytes or greater, or if noise bit is on, a read recovery sequence is initiated. This sequence consists of the following steps:

1. Reposition the tape.
2. Issue the Track-in-Error command to send error information (byte 2, bit 7) to the tape control unit.
3. Re-read the tape. If error persists, post (or repost) the applicable flag bit (representing a temporary 'read' error) in temporary storage.
4. Repeat steps one through three for a total of four rereads unless a good read is obtained.
5. Perform a tape cleaner action and increment the temporary cleaner action counter in the Volume Statistics Table.

A total of ten read recovery sequences can be initiated. If the error is not cleared by that time, a read-opposite recovery sequence is initiated, provided that none of the following conditions exists:

- Data chaining is being performed.

- Data conversion mode and 7-track tape are being used.
- The original CCW count is less than the physical block size on the tape.
- "Suppress data transfer" is specified in the original CCW.

During a write or write tape mark operation: reposition the tape, issue an erase gap, issue a mode set (if 7-track), and reissue the command.

3400 write: repeat this procedure until successful or until 14 retries have been attempted. If the error persists after 14 retries, go to step 1 below.

2400 write: (2400/3420 write tapemark) repeat this procedure until successful or until 15 retries have been attempted. If the error persists after 15 retries, go to step 2 below.

Step 1. Change the failing write CCW to a "loop-write-to-read" CCW. The write CCW must not be a command or data chained from or to any of the CCWs in the original failing CCW chain. After the loop-write-to-read has been completed, the failing write CCW is issued to complete the fifteenth retry.

Step 2. Provide an operator message, post completed with error condition, and exit to operating system.

During an ERG: reissue the command. Repeat this procedure until 3 retries have been attempted. If the error persists, provide an operator message, post completed with error condition, and exit to the operating system.

Byte 0 Bit 5: Overrun
This bit is set when service is requested but data cannot be transferred during a read, write, or read backward operation. Five retries are attempted. Before each retry, the tape is repositioned. *Note:* A data check during overrun suppresses the overrun indication.

Byte 0 Bit 6: Word Count Zero
This bit is set during a write operation if transfer of data is prevented before the first byte is written. This indicator is ignored.

Byte 0 Bit 7: Data Converter Check
This bit is set when an error occurs during operation of the data conversion feature. The error is considered permanent.

Other Actions Taken

Byte 1 Bit 7: Not Capable
Set on some models when density handling features are not compatible with actual tapedensity. No retries are attempted.

Byte 5 Bit 3: Phase Encoding ID Burst Check
Reposition to load point with a Rewind command and reissue the command. Repeat this procedure until successful, or until 14 retries have been attempted. A Loop-write-to-read command is issued and the fifteenth write retry is issued.

Byte 7 Bit 4: Data Security Erase Error
Print a message to the operator and record as a permanent error.

Unexpected Device End
Print a message to the operator and reissue the command.

Channel Data Check
This status bit is set when a channel detects a parity error in the information transferred to or from virtual storage during an I/O operation. Five retries are attempted. The tape is repositioned before each retry of a read or write operation.

Chaining Check

This status bit is set when channel overrun occurs during data chaining on read operations. Five retries are attempted. The tape is repositioned before each retry.

Interface Control Check
Channel Control Check

An interface control check is caused by an invalid signal on the I/O interface; channel control check is caused by any machine malfunction affecting channel controls. Actions taken by the 2400/3400 error routine are shown below. Error recovery procedure interface bytes (ERPIB) are supplied by the Channel Check Handler routine.

No retries are attempted when:

- ERPIB byte 4, bit 7 is on (unconditional no-retry).
- ERPIB byte 6, bit 3 or 4 or 5 is off (retry code invalid, unit status invalid, or command address invalid).
- ERPIB are not produced.
- ERPIB byte 7, bits 0 and 1 are both on (system reset).
- ERPIB byte 4, bit 2 is on (Test I/O with no pending interruption stored a CSW).
- ERPIB byte 4, bit 3 is on (Halt I/O stored a CSW).
- ERPIB byte 4, bits 0 and 1 are both on or both off.
- ERPIB byte 4, bit 5 is off (if unit check).
- There is a unit check and an equipment check.
- The interface control check or channel control check occurred during tape repositioning (unless cc = 1).

Retries are attempted when none of the above conditions exists and ERPIB termination codes and retry combinations are:

- Termination code 10, retry code 010. Write command—retry once.
- Termination code 01, retry code 011 or 101. Write or Read command—reposition and retry once. For other commands (except Set, Mode, and Transfer-in-Channel) the operation is considered complete and no recovery is attempted.

If the device is one of the 3400 series, retries are attempted when any of the following conditions exist:

- Read or Read Backward, termination code of 00, 01, or 10, and sequence code 001.
- Write, termination code 00, 01, or 10, and sequence code 001.
- Control (Read/Write), termination code 00, 01, or 10, and sequence code 001.
- Control (Rewind/Unload/Mode Set), termination code 00, 01, or 10, and sequence code 001 or 010.
- Sense, termination code 00 or 01, and sequence code 001, 010, 011, or 101.
- For all other termination and sequence code combinations, the errors are not retriable.

2495 Error Routine

The IBM 2495 Tape Cartridge Reader error routine attempts recovery from channel data checks. The 2495 error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence is shown in Figure 85. The meanings of sense bits, IOB flags, and IOB error counts are shown in Figure 86.

More information can be obtained from the following publication: *IBM System/360 Component Description, IBM 2495 Tape Cartridge Reader,* GA27-2726

Bit 0: Command Reject

This bit is set when:

- An invalid command is received and the control unit is not busy.
- A Read command is received after end-of-tape is encountered.
- A Control Rewind or Control Backspace command is received when the tape is in the load position.
- A Control Backspace command is received immediately following a position check caused by another Control Backspace command.

No retries are attempted.

Bit 1: Intervention Required

This bit is set when a command is received and the control unit is in the not-ready state because:

- The stop key was depressed.
- The hopper is empty and the end-of-file key has not been depressed.
- The power is off.
- The stacker is full.
- An auto-loader malfunction occurred.

The requester's RQE is queued so that when the tape drive is made ready the command will be reissued.

Bit 2: Bus-Out Check

This bit is set when a command with even parity appears on a bus-out operation. If the bit is set during initial selection, the operation is retried once. On the second occurrence, the error is considered permanent.

Bit 3: Equipment Check

This bit is set when:

- The leader is disconnected.
- The tape is jammed.
- The tape is not repositioned.
- A motion detection device fails.

The error is considered permanent.

Bit 4: Data Check

This bit is set when a byte with even parity is detected in the data register during a Read command. The tape is backspaced one byte and the remaining portion is read. The sequence is repeated up to ten times. The UCB extension is used as a work area for constructing a backspace CCW, a residual read CCW, and, for command chaining,

Priority	Status Bit	Sense Byte	Bit	Condition	Pointer
1	45			Channel Control Check	ERR033
2	46			Interface Control Check	ERR033
3	44			Channel Data Check	ERR033
4	42			Program Check	ERR033
5	43			Protection Check	ERR033
6	38			Unit Check	ERR033
7		0	5	Should Not Occur	ERR046
7		0	7	Should Not Occur	ERR046
8		0	3	Equipment Check	ERR046
9		0	2	Bus-Out Check	ERR046
10		0	1	Intervention Required	ERR046
11		0	6	Position Check	ERR046
12		0	4	Data Check	ERR046
13		0	0	Command Reject	ERR046
14				None of the Above Sense Bits On	ERR046
None	39			Unit Exception	ERR033
None	41			Incorrect Length	ERR033

Figure 85. 2495 Error Analysis Sequence (Module IGE0011A)

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	——	Position Check	——
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	Unrelated Flag	0 Start 1 Restart
IOBFL 2	——	Sense Bit	Purge Flag	——	——	——	——	——
IOBFL 3	——	IOB Entry Flag	Read Channel Data Check Count	Bus-Out Error Count	——	Message Type	——	Logout Flag
IOB Error Counts Byte 1	Read Position Check Count				Read Data Check Count			

Figure 86. 2495 Sense Bits, IOB Flags, and IOB Error Counts

a transfer-in-channel to the next user CCW. If the error remains after ten retries, it is considered permanent.

Bit 5: Should Not Occur
When this bit is set, a catastrophic error is assumed.

Bit 6: Position Check (Read Command)
This bit is set when a Read command causes the reading of tape past the stop code, beyond the end of valid data. The stop code was not detected or was ignored by the program. The tape is backspaced one byte and the data is reread. The sequence is repeated up to ten times. If the error remains, it is considered permanent. The UCB extension is used as a work area for constructing a backspace CCW, a residual read CCW, and, for command chaining, a transfer-in-channel to the next user CCW.

Bit 6: Position Check (Control)
This bit is set by indicate that a Control Backspace command has caused backspacing to the beginning of the tape. No retries are attempted.

Bit 7: Should Not Occur
When this bit is set, a catastrophic error is assumed.

2540 Error Routine

The IBM 2540 Card Read Punch error routine attempts recovery from channel data checks. Read operations are retried five times; punch operations are retried once, if a bus-out check resulted from the channel data check. The 2540 error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence is shown in Figure 87. The meanings of sense bits, IOB flags, and IOB error counts are shown in Figure 88. More information can be obtained from the following publications:

- *IBM System/360 Component Description and Operating Procedures: IBM 2540 Card Read Punch,* GA21-9033
- *IBM 2821 Control Unit,* GA24-3312

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject
The setting of this bit indicates one of the following:

- A Read Backward or a Write command was issued to the reader.
- A Read Backward control other than NOP or a Read Feed and Stacker Select command was issued to a punch without the Punch-Feed-Read feature.
- A Read Backward or Control command was issued to a punch with the Punch-Feed-Read feature.
- An incorrect sequence of instructions was issued.
- An invalid command was received.

The error is considered permanent.

Bit 1: Intervention Required
The setting of this bit indicates a not-ready condition due to one of the following:

- Cards are not at each station (not end-of-file for the reader).
- The stacker is full.
- The hopper is empty (not end-of-file for the reader).
- The Stop key was depressed.
- The chipbox is full or has been removed.

	Status	Sense			Applicable to:				
Priority	Bit	Byte	Bit	Condition	Read	Punch	Control	Pointer	Load
1	45			Channel Control Check	X	X	X	ERR551	1
1	46			Interface Control Check	X	X	X	ERR551	1
2	47			Chaining Check	X	X	X	ERR546	1
3	44			Channel Data Check	X			ERR524	1
4	38			Unit Check	X	X	X	ERR525	1
5		0	5	Should Not Occur	X	X	X	ERR546	1
5		0	7	Should Not Occur	X	X	X	ERR546	1
6		0	3	Equipment Check	X	X		ERR528	1
7		0	1	Intervention Required	X	X		ERR552	2
8		0	2	Bus-Out Check	X	X		ERR534	2
9		0	4	Data Check	X			ERR536	2
10		0	0	Command Reject	X	X	X	ERR548	2
11		0	6	Unusual Command Sequence	X			ERR555	2
12	42			Program Check	X	X	X	ERR543	2
13	43			Protection Check	X	X	X	ERR543	2
14	39			Unit Exception	X			ERR543	2
15	41			Incorrect Length	X	X		ERR543	2

Figure 87. 2540 Error Analysis Sequence (Load 1-IGE0001C or Load 2-IGE0101C)

- There is a card jam.

A message is given the operator, who must take action. Upon correction of the condition, the interrupted operation is repeated.

Bit 2: Bus-Out Check

This bit is set when a parity error has occurred on bus-out on a command or data byte (bus-out is a data transfer from the processing unit to the control unit). When this error is detected, no punching occurs. The operation is retried once and if the error occurs a second time it is considered to be permanent.

Bit 3: Equipment Check

This bit is set after one of the following:

- A hole count error
- A buffer parity error
- A translate check
- An address check

The error applies to the card that preceded the one from which data was transmitted; it is considered permanent. If the error occurred during the processing of a Read command, the operation is retried five times. If the error occurred during a QSAM operation, one retry is attempted.

Bit 4: Data Check

This bit is set when an invalid card code is detected. The operation is retried five times. On the sixth occurrence, it is denoted as a permanent error.

Bit 5: Should Not Occur

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	——	Unusual Command Sequence	——
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL 2	——	——	——	——	——	——	——	QSAM Access Method
IOBFL 3	Indicator 1	Entry Flag	Read Error Count	Bus-Out Error Count	Punch Relay	Message Type	QSAM Count	Logout Flag
Error Counts IOBECT Byte 2	Accept Unusual Command Sequence	——	——	——	Data Check, Channel Data Check, Equipment Check Count			Channel Control Check, Interface Control Check

Figure 88. 2540 Sense Bits, IOB Flags, and IOB Error Counts

Bit 6: Unusual Command Sequence
This bit is set when there are two consecutive reads without an intervening feed. The error is considered permanent.
Bit 7: Should Not Occur

3211 Error Routine

The IBM 3211 Printer error routine attempts recovery from channel data checks only if they occur with bus-out checks. A channel data check occurring alone is not considered an error.

The 3211 error routine also attempts recovery from channel control checks and interface control checks.

In addition to handling the normal functions of an error recovery procedure, the 3211 ERP compiles data for device dependent OBR records. These records are then recorded on SYS1.LOGREC by the recording module IGE0625F. The following information will be recorded:

1. FCB Parity Check—Carriage Control Address Register (CCAR) and the FCBID in the UCB

2. PLB Parity Check—Diagnostic Check Read Data and the first 10 positions of the PLB

3. UCS Parity Check—Contents of UCS buffer and the UCSID in the UCB

See *OS/VS SYS1.LOGREC Error Recording Logic* for more information about the SYS1.LOGREC data set recording.

The error recovery procedure for the 3211 Printer is shown in Figure 89. The meanings of sense bits, IOB flags and IOB error counts are shown in Figure 90.

Priority	Status Bit	Sense Byte	Bit	Condition	Pointer
1	45			Channel Control Check	ERR031
1	46			Interface Control Check	ERR031
2	47			Chaining Check	ERR070
3	38			Unit Check	ERR040
4		1	5	Command Suppress	ERR050A
5		0	3	Equipment Check	ERR051
6		0	2	Bus-Out Check	ERR052
7		0	4	Data Check	ERR055E
8		0	5	Buffer Parity Check	ERR053
9		0	0	Command Reject	ERR071
10		0	6	Load Check	ERR070
11		0	1	Intervention Required	ERR055
12		0	7	Channel 9	ERR064A
13	44			Channel Data Check	ERR061
14	42			Program Check	ERR062
15	43			Protection Check	ERR062
16	41			Incorrect Length	ERR063
17	39			Unit Exception	ERR064

Figure 89. 3211 Error Analysis Sequence (Module IGE0000F)

More information can be obtained from the following publication: *IBM 3211 Printer and 3811 Control Unit Component Description,* GA24-5343.

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Buffer Parity Error	Load Check	Channel 9
Sense Byte 1	Command Retry	Print Check	Print Quality	Line Position	Forms Check	Command Suppress	Mechanical Motion	——
Sense Byte 2	Carriage Fail to Move	Carriage Sequence Check	Carriage Stop Check	Platen Fail to Advance	Platen Fail to Retract	Forms Jam	Ribbon Motion	Train Overload
Sense Byte 3	UCSB Parity	PLB Parity	FCB Parity	Coil Protect	Hammer Fire Check	Field Engineering	UCSAR Sync Check	Sep Sync Check
IOBFL1	00 - No Chaining 01 - Command Chaining 10 - Data Chaining 11 - Both		Error Routine in Control	——	——	Exceptional Condition	——	0 - Start 1 - Restart
IOBFL3	MCS Flag	Entry Flag	Command Suppress Error Count	Bus-Out Error Count	Buffer Flag	Message Type	TPER Flag	Logout Flag
IOBECT	FCB Count	——	——	——	FCB Count	UCS Count	Channel Error Count	——
IOBECT+1	——	——	——	——	——	MCS Count	MCS Count	MCS Count

Figure 90. 3211 Sense Bits, IOB Flags, and IOB Error Counts

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject
This bit is set during Initial Selection when a command other than those defined for the printer is given. The error is considered permanent.

Bit 1: Intervention Required
This bit indicates a not-ready condition due to one of the following:

- Platen failure
- Ribbon motion or ribbon skew
- Jammed or torn forms
- Carriage Stop-Release Off
- Interlock condition

An 'Intervention Required' message is issued for the operator; when the condition is corrected the last operation is repeated. If this occurs with channel 9 (bit 7) the message is given to the operator, but the error is handled as a channel 9 condition. The operator has the option of forcing a permanent error by pressing the Cancel button on the 3211.

Bit 2: Bus-Out Check
This results when the control unit receives a data byte or a command byte with invalid parity. The operation is retried once in a non-multiple console support system and 5 times in an MCS system.

Bit 3: Equipment Check
This bit indicates a malfunction that affects the operation in process. The specific condition will be indicated by a bit in byte 1.

Bit 4: Data Check
This bit signifies that there is an incomparable code in the UCSB or in the FCB. An 'Intervention Required' message will be written to the operator and when the condition is corrected the previous operation will be retried. The operator will have the option of causing a permanent error by pressing the Cancel button on the 3211.

Bit 5: Buffer Parity Check
This bit indicates invalid parity in the UCSB or FCB. The error is considered permanent.

Bit 6: Load Check
This bit is given for a load UCSB or load FCB command when the load was invalid. The error is considered permanent.

Bit 7: A channel 9 code was sensed in the FCB during a carriage motion.

Sense Byte 1 Meanings

Bit 0: Command Retry—This indicates a parity error in the print line buffer. The error is considered permanent. In a system with MCS the error is retried 5 times before it is considered permanent.

Bit 1: Print Check—Indicates the line in process may contain one or more print errors.

Bit 2: Print Quality—Indicates a machine failure that could affect print quality.

Bit 3: Line Position—Indicates that the previous line or next line to be printed may be in the wrong place.

The last three conditions will result in an 'Intervention Required' message to the operator. When the condition is corrected the last operation is repeated. The operator will have the option to cause a permanent error by pressing the Cancel button on the 3211.

Bit 6: Mechanical Motion—Signifies that the command in process cannot be completed and the results are unpredictable due to hardware failure. The error is considered permanent.

If bit 3 of byte 0 is set and no bits in byte 1 are set, a sync check or train overload exists. These errors are considered permanent.

3505 and 3525 Error Routines

The error routine for the IBM 3505 Card Reader and IBM 3525 Card Punch with Read and Punch features attempts recovery from I/O errors that cause an interruption. The condition causing the interruption is indicated in the channel status word (CSW). If the unit check (bit 38) is present in the CSW, a sense command is performed to obtain further information about the error interrupt. The status byte and sense byte 0 provide information and reasons for a unit check detected in the last operation. Sense byte 1 defines the ERP actions required for the unit check.

The error analysis sequence is shown in Figure 91. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Figure 92. More information can be obtained from *IBM 3505 Card Read and IBM 3525 Card Punch Subsystem,* GA21-9124.

	Status	Sense			Applicable to:				
Priority	Bit	Byte	Bit	Condition	Read	Punch	Printer	Control	Pointer
1	45			Channel Control Check	X	X	X	X	ERR001
2	46			Interface Control Check	X	X	X	X	ERR011
3	44			Channel Data Check		X	X	X	ERR012
4	32			Should Not Occur	X	X	X	X	EXIT12
5	33			Should Not Occur	X	X	X	X	EXIT12
6	34			Should Not Occur	X	X	X	X	EXIT12
7	38			Unit Check	X	X	X	X	SENSE0
8		0	5	Should Not Occur	X	X	X	X	EXIT12
9		0	7	Permanent Error (Key)	X	X	X	X	EXIT22
10		0	3	Equipment Check	X	X	X		ERR002
11		0	6	Abnormal Format Reset	X				SENSE1
12		0	1	Intervention Required	X	X	X	X	ERR003
13		0	2	Bus-Out Check	X	X	X	X	SENSE1
14		0	4	Data Check	X				SENSE1
15		0	0	Command Reject	X	X	X	X	SENSE1
16	47			Chaining Check	X				EXIT12
17	42			Program Check	X	X	X		ERR004
18	43			Protection Check	X	X	X	X	ERR004
19	39			Unit Exception	X				ERR004
20	41			Incorrect Length	X	X			ERR004

Figure 91. 3505/3525 Error Analysis Sequence (Module IGE0001A)

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set on for invalid commands such as read backwards and for commands for uninstalled features. The error is considered a permanent condition.

Bit 1: Intervention Required

This bit is set on for a hopper misfeed, hopper jam, cornering station misfeed, Read station check, transport jam, and normal user occurrences such as hopper empty, joggler open, stacker full, stop key depressed, or covers open.

Recovery from this error is possible as defined by recovery indicators on the machine.

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	——	Abnormal Format Reset	Permanent Error Key
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL 2	——	——	——	——	——	——	——	QSAM Access Method
IOBFL 3	Auto. Retry Flag Command	Entry Flag	Channel Control Check	Interface Control Check	Punch Retry	Message Type	QSAM Count	Logout Flag
Error Counts IOBECT Byte 2		——	——	——				Channel Control Check, Interface Control Check

Figure 92. 3505/3525 Sense Bits, IOB Flags, and IOB Error Counts

Bit 2: Bus-Out Check

This results in a bad parity on bus-out during initial selection. The error is considered a permanent condition only after the second try.

Bit 3: Equipment Check

This bit is turned on for errors due to data compare check, emitter check, and CU internal parity check detected between IS and CE.

A recovery can be made as defined by the recovery indicators on the machine.

Bit 4: Data Check

This results when an invalid EBCDIC card code is found when Data Mode 1 is read. Recovery can be made as defined by recovery indicators on the machine.

Bit 5: Not Used

Bit 6: Abnormal Format Reset

Bit 7: Permanent Error (Error Bypass Key)

This results when the operator presses the Error Bypass Key rather than performing recovery assistance. The error is considered a permanent condition.

Sense Byte 1 Meanings

Bit 0: Permanent Error

This bit directs the ERP to post a permanent error condition and proceed with appropriate disposition of the condition. It is set only with sense byte 0, bit 0 or bit 1.

Bit 1: Automatic Retry

This results in retrying the failing CCW once. If successful, normal program execution continues. If unsuccessful, a permanent error condition is posted and the procedure is continued with the appropriate disposition of the condition. This occurs only with sense byte 0, bits 2 and 3.

Bit 2: Motion Malfunction

This bit is turned on with Intervention Required when the cause is other than a normal user occurrence. It is set only with sense byte 0, bit 1. This bit is not required by the ERP to effect recovery but is included to facilitate the measurement of SSIs.

Bit 3: Retry After Intervention Required Complete

After a normal not-ready to ready Device End, the failing CCW is reissued. This occurs only with sense byte 0, bits 1, 3, 4, and 6.

Bits 4-7: Not Used.

Sense Byte 2 Meanings

This sense byte is for diagnostic purposes only. It defines the first error in the 3505 or 3525 and also serves as a pointer to the appropriate maintenance documentation.

Sense Byte 3 Meanings

This sense byte is for diagnostic purposes only. It serves to further resolve a limited group of errors.

Channel Checks

Recovery from channel errors (channel control check, interface control check, and channel data check) is as follows:

If Selective Reset or Interface Disconnect was given between Initial Selection and Channel End, reissue the command to the 3505 or 3525.

GLOSSARY OF TERMS, ACRONYMS, AND ABBREVIATIONS

The following list of terms are defined as they are used in this publication. Acronyms and abbreviations with their meanings are also listed in alphabetical sequence with the list of terms. If you do not find the term you are looking for, refer to the index or to the *IBM Data Processing Glossary,* GC20-1699.

access method: Any of the data management techniques available to the user for transferring data between real storage and an input/output device.

address translation: The process of changing the address of a data item or an instruction from its virtual address to its real storage address. See also dynamic address translation.

allocate: To assign a resource for use in performing a specific task.

alternate path retry (APR): A facility that allows an I/O operation that has developed an error to be retried on another channel assigned to the device performing the I/O operation. APR also provides the capability to establish other paths to an online or offline device.

alternate track: For direct-access devices, a track designated to contain data in place of a defective primary track.

APR: Alternate path retry.

ASCII: American National Standard Code for Information Interchange.

asynchronous: Without regular time relationship; unexpected or unpredictable with respect to the execution of a program's instructions.

automatic priority group: A group of tasks at a single priority level that are dispatched according to a special algorithm that attempts to provide optimum use of CPU and I/O resources by these tasks. See also dynamic dispatching.

available page queue: A queue of the pages whose real storage is currently available for allocation to any task.

AVT: Appendage vector table.

BEBLK: Beginning-end block.

BSAM: Basic sequential access method.

BTAM: Basic teleprocessing access method.

buffer: An area of storage that is temporarily reserved for use in performing an input/output operation, into which data is read or from which data is written. Synonymous with I/O area.

burst mode: A means of transferring data to or from a particular I/O device on either the multiplexer or selector channel. All channel controls are monopolized for the duration of data transfer.

byte mode: See multiplex mode.

CAW: Channel address word.

CC: Condition code; chain command.

CCC: Channel control check.

CCH: Channel check handler.

CCW: Channel command word.

CCW translation: See channel program translation.

CD: Chain data.

CE: Channel end.

CEB: Channel error block.

channel: A hardware device that connects the CPU and real storage with the I/O control units.

channel address word (CAW): A word in real storage that specifies the location in real storage where a channel program begins.

channel check handler (CCH): A feature that, when a channel error occurs, records information about the error and issues a message to the operator.

channel command: An instruction that directs a channel, control unit, or device to perform an operation or set of operations.

channel command word (CCW): A doubleword at the location in real storage specified by the channel address word. One or more CCWs make up the channel program that directs channel operations.

channel program: One or more channel command words that control a specific sequence of channel operations. Execution of the specific sequence is initiated by a single start I/O instruction.

channel program translation: In a channel program, replacement by software of virtual addresses with real addresses.

channel status word (CSW): A doubleword in real storage that provides information about the termination of I/O operations.

control block: A storage area used by an operating system to hold control information.

control program: A program that is designed to schedule and supervise the performance of data processing work by a computing system.

CPU: Central processing unit.

CRC: Cyclic redundancy check.

CSW: Channel status word.

CUA: Channel and unit address.

CVT: Communications vector table.

DASD: Direct-access storage device.

DAT: Dynamic address translation.

data set: The major unit of data storage and retrieval in an operating system, consisting of a collection of data in one of several prescribed arrangements and described by control information to which the system has access.

DAVV: Direct-access volume verification.

DCB: Data control block.

DDR: Dynamic device reconfiguration.

DEB: Data extent block.

DEC: Decimal.

demand paging: Transfer of a page from external page storage to real storage at the time it is needed for execution.

device number: A part of an external page address that refers to a particular paging device; together with a group number and a slot number, it identifies the location of a page in external page storage.

DIDOCS: Device independent display operator's console support.

direct access: Retrieval or storage of data by a reference to its location on a volume, rather than relative to the previously retrieved or stored data.

direct-access storage device (DASD): A device in which the access time is effectively independent of the location of the data.

disabled page fault: A page fault that occurs when I/O and external interruptions are disallowed by the CPU.

disk storage: Storage on direct-access devices that record data magnetically on rotating disks.

drum storage: A direct-access storage device which records data magnetically on a rotating cylinder.

DSCB: Data set control block.

DSS: Dynamic support system.

dynamic address translation (DAT): The change of a virtual storage address to a real storage address during execution of an instruction. See also address translation.

dynamic dispatching: A facility that assigns priorities to tasks within an automatic priority group to provide optimum use of CPU and I/O resources.

dynamic support system (DSS): An interactive debugging facility that allows authorized maintenance personnel to monitor and analyze events and alter data.

EBCDIC: Extended binary-coded-decimal interchange code.

ECB: Event control block.

ECF: Error correction function.

enabled page fault: A page fault that occurs when I/O and external interruptions are allowed by the CPU.

EOD: End-of-day.

EOF: End-of-file.

EOV: End-of-volume.

ERG: Error record gap.

ERP: Error recovery procedure.

ERPIB: Error recovery procedure interface block.

ESV: Error statistics by volume.

EVA: Error volume analysis.

EXCP: Execute channel program.

EXCPVR: Execute channel program virtual equal real. An I/O request issued from a virtual region whose channel program contains real addresses. This channel program does not require translation by IOS.

external page address: An address that identifies the location of a page in a page data set. The address consists of a relative device number, a relative group number, and a relative slot number.

external page storage: The portion of auxiliary storage that is used to contain pages.

external page table (XPT): An extension of a page table that identifies the location on external page storage of each page in the page table.

external storage: Data storage other than real storage; for example, storage on magnetic tape or direct-access devices.

FIFO: First-in, first-out.

fixed: Not capable of being paged out.

fixed page: A page in real storage that is not to be paged out.

FLIH: First level interuption handler.

frame: See page frame.

frame number: The part of a real storage address needed to refer to a frame. See also page number and segment number.

frame table: See page frame table.

frame table entry (FTE): An entry in the page frame table that describes how a frame is being used.

FREELIST: A chain of unassigned RQEs.

FTE: Frame table entry.

group: See slot group.

group number: A part of an external page address that refers to a slot group; together with a device number and a slot number, it identifies the location of a page in external page storage.

GTF: Generalized trace facility.

HA: Home address.

HEX: Hexadecimal.

HIO: Halt input/output.

HIPO: Hierarchy input-process-output.

hold page queue: A queue to which pages in real storage are initially assigned through operations such as page-in or page reclamation. See also available page queue.

IAL: Indirect address list.

ICC: Interface control check.

ILC: Instruction length code.

input/output: A general term for the equipment used to communicate with a computer, commonly called I/O. The data involved in such communication.

input-output error: A general term used to denote any of the conditions that would preclude normal (or successful) completion of an I/O operation. Input-output errors are generally a result of malfunctioning input/output devices.

intercepted I/O request: A request for I/O activity on which processing has been suspended so that an I/O error routine could be used to process an error that occurred after channel end for the last activity on the needed device.

invalid page: A page that cannot be directly addressed by the dynamic address translation feature of the central processing unit.

I/O: Input/output.

IOB: Input/output block.

IOS: Input/output supervisor.

IPL: Initial program loading.

IRB: Interruption request block.

job pack area (JPA): See region job pack area.

JPA: Job pack area.

LCH: Logical channel.

link pack area (LPA): An area of virtual storage containing selected reenterable and serially reusable routines that are loaded at IPL time and can be used concurrently by all tasks in the system.

link pack area directory: A directory that contains an entry for each entry point in link pack area modules.

link pack area library: A partitioned data set that contains the modules specified to be in the link pack area.

link pack area queue: A queue that contains a contents directory entry for each link pack area module currently in use, for each module in the link pack update area, and for each module in the fixed link pack area.

link pack update area: An area in virtual storage containing modules that are additions to replacements for link pack area modules for the current IPL.

local system queue area (LSQA): One or more segments associated with each virtual storage region that contains job-related system control blocks.

lock/unlock facility: A supervisor facility that controls the execution of instruction strings when a disabled page fault occurs.

logical channel: The set of all physical channels by which a device may be reached.

LPA: Link pack area.

LSQA: Local system queue area.

MCH: Machine check handler.

NIP: Nucleus initialization program.

nondynamic area: The area of virtual storage occupied by the resident portion of the control program (the nucleus and the link pack area). Contrast with dynamic area.

nonpageable dynamic area: An area of virtual storage whose virtual addresses are identical to real addresses; it is used for programs or parts of programs that are not to be paged during execution.

nonpageable region: A subdivision of the nonpageable dynamic area that is allocated to a job step or system task that is not to be paged during execution. In a nonpageable region, each virtual address is identical to its real address.

NRZI: Non-return-to-zero-inverse encoding.

OBR: Outboard recorder; outboard recording.

OLTEP: Online Test Executive Program.

page: A fixed-length block of instructions, data, or both, that can be transferred between real storage and external page storage.

page fault: A program interruption that occurs when a page marked "not in real storage" is referred to by an active page. Synonymous with page translation exception.

page fixing: Marking a page as nonpageable so that it remains in real storage.

page frame: A block of real storage that can contain a page.

page frame table: A table that contains an entry for each frame. Each frame table entry describes how the frame is being used.

page-in: The process of transferring a page from external page storage to real storage.

page-out: The process of transferring a page from real storage to external page storage.

paging: The process of transferring pages between real storage and external page storage.

paging device: A direct-access storage device on which a page data set (and possibly other data sets) are stored.

paging supervisor: A part of the supervisor that allocates and releases real storage space (page frames) for pages, and initiated page-in and page-out operations.

PCI: Program controlled interruption.

PCRS: Program check recovery subroutine.

PCU: Primary control unit.

permanent error: An I/O error that either cannot be corrected or remains uncorrected after error recovery procedures have been used.

PGFX: Page fix.

PL/I: Programming Language I.

primary paging device: An auxiliary storage device that is used in preference to secondary paging devices for paging operations. Portions of a primary paging device can be used for purposes other than paging operations.

processing program: Any program capable of operating in the problem program mode. This included IBM-distributed language processors, application programs, service and utility programs, and user-written programs.

PSA: Prefixed storage area.

PSW: Program status word.

QSAM: Queued sequential access method.

quick cell: A reserved space in the system queue area or a local system queue area that can be used to reduce that time required to allocate space for a control block.

real storage: The storage from which the central processing unit can directly obtain instructions and data, and to which it can directly return results.

reference bit: A bit associated with a page in real storage; the reference bit is turned "ON" by hardware whenever the associated page in real storage is referred to (read or stored into). There is a reference bit in each of two storage key areas associated with each page frame.

region: See virtual storage region.

region job pack area (JPA): An area in a virtual storage region that contains modules that are not in the link pack area but are needed for the execution of jobs.

relocate hardware: See dynamic address translation.

RQE: Request queue element.

R0: Record zero.

SAVECCW: Pointer to an address of the user's channel program.

SCU: Secondary control unit.

SER: System environment recording.

secondary paging device: An auxiliary storage device that is not used for paging operations until the available space on primary paging devices falls below a specified minimum. Portions of a secondary paging device can be used for purposes other than paging operations.

segment: A continuous 64K area of virtual storage, which is allocated to a job or system task.

segment table entry (STE): An entry in the segment table that indicates the length, location, and availability of a corresponding page table.

segment translation exception: A program interruption that occurs when a virtual address cannot be translated by the hardware because the invalid bit in the segment table entry for that address is set. See also page translation exception, translation specification exception.

SIO: Start input/output.

SIRB: System interruption request block.

SLI: Suppress length indication.

slot: A continuous area on a paging device in which a page can be stored.

slot group: A set of slots on one or more tracks within a cylinder on a paging device.

slot number: A part of an external page address that refers to a slot; together with a device number and a group number, it identifies the location of a page in external page storage.

SMF: System management facilities.

SQA: System queue area.

STE: System table entry.

supervisor call (SVC): An instruction which causes an SVC interruption in the hardware to give control to a control program routine (called an SVC routine) for some specific action, such as reassigning parts of real storage or retrieving data from an I/O device.

supervisor lock: An indicator used to inhibit entry to disabled code while a disabled page fault is being resolved.

SVC: Supervisor call.

TCB: Task control block.

TCH: Test channel.

TIC: Transfer in channel.

TIE: Track in error.

TIOT: Task input/output table.

TP: Teleprocessing.

track address: In direct-access devices, an address made up of a cylinder number and a read-write head number. Every track of a direct-access device has a unique track address.

translation specification exception: A program interruption that occurs when a page table entry, segment table entry, or the control register pointing to the segment table contains information in an invalid format. See also page translation exception, segment translation exception.

UCS: Universal character set.

UR: Unit record.

virtual address: An address that refers to virtual storage and must, therefore, be translated into a real storage address when it is used.

virtual equals real (V=R) storage: An area of virtual storage that has the same range of addresses as real storage and is used for a program or part of a program that cannot be paged during execution.

virtual storage: Addressable space that appears to the user as real storage, from which instructions and data are mapped into real storage locations. The size of virtual storage is limited by the addressing scheme of the computing system and by the amount of auxiliary storage available, rather than by the actual number of real storage locations.

virtual storage region: A subdivision of the dynamic area that is allocated (in segment-size blocks) to a job step or a system task.

VS: Virtual storage.

WTO: Write-to-operator.

XPT: External page table.

INDEX

Indexes to program logic manuals are consolidated in the publication *OS/VS Master Index of Logic*, GY28-0603. For additional information about any subject listed below, refer to other publications listed for the same subject in the master index.

SY26-3823-1

OS/VS2 I/O Supervisor Logic (File No. S370-30) Printed in U.S.A. SY26-3823-1

IBM®

International Business Machines Corporation
Data Processing Division
1133 Westchester Avenue, White Plains, New York 10604
(U.S.A. only)

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
(International)

OS/VS2 I/O Supervisor Logic
SY26-3823-1

Reader's Comment Form

Your comments about this publication will help us to improve it for you. Comment in the space below, giving specific page and paragraph references whenever possible. All comments become the property of IBM.

Please do not use this form to ask technical questions about IBM systems and programs or to request copies of publications. Rather, direct such questions or requests to your local IBM representative.

If you would like a reply, please provide your name, job title, and business address (including ZIP code).

Fold on two lines, staple, and mail. No postage necessary if mailed in the U.S.A. (Elsewhere, any IBM representative will be happy to forward your comments.) Thank you for your cooperation.

SY26-3823-1

Fold and Staple

First Class Permit
Number 2078
San Jose, California

Business Reply Mail
No postage necessary if mailed in the U.S.A.

Postage will be paid by:

IBM Corporation
Programming Center – Publishing
Department D58
Monterey and Cottle Roads
San Jose, California 95193

Fold and Staple

IBM®

International Business Machines Corporation
Data Processing Division
1133 Westchester Avenue, White Plains, New York 10604
(U.S.A. only)

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
(International)

OS/VS2 I/O Supervisor Logic (File No. S370-30) Printed in U.S.A. SY26-3823-1

OS/VS2 I/O Supervisor Logic
SY26-3823-1

Reader's Comment Form

Your comments about this publication will help us to improve it for you. Comment in the space below, giving specific page and paragraph references whenever possible. All comments become the property of IBM.

Please do not use this form to ask technical questions about IBM systems and programs or to request copies of publications. Rather, direct such questions or requests to your local IBM representative.

If you would like a reply, please provide your name, job title, and business address (including ZIP code).

Fold on two lines, staple, and mail. No postage necessary if mailed in the U.S.A. (Elsewhere, any IBM representative will be happy to forward your comments.) Thank you for your cooperation.

SY26-3823-1

Fold and Staple

First Class Permit
Number 2078
San Jose, California

Business Reply Mail

No postage necessary if mailed in the U.S.A.

Postage will be paid by:

IBM Corporation
Programming Center – Publishing
Department D58
Monterey and Cottle Roads
San Jose, California 95193

Fold and Staple

OS/VS2 I/O Supervisor Logic (File No. S370-30) Printed in U.S.A. SY26-3823-1

IBM ®

International Business Machines Corporation
Data Processing Division
1133 Westchester Avenue, White Plains, New York 10604
(U.S.A. only)

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
(International)