IBM Maintenance Library

3125 Processing Unit Multiplexer Channel

SY33-1067-1

Third Edition (August, 1973)

This manual is a major revision of, and makes obsolete, SY33-1067-0; it also obsoletes the preliminary manual ZZ33-1067 (IBM Confidential). Changes are continually made to the information in this manual; any such changes will be reported in subsequent revisions or Technical Newsletters.

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Preface

This manual describes the theory of operation of the multiplexer channel and provides maintenance information for the multiplexer channel. Readers of the manual should have a basic understanding of IBM system concepts. The manual supplements the System/370 Model 125 CE course and serves also as a recall aid; it is not intended for self-education.

The manual is divided into seven chapters. *Chapter 1* contains a general introduction to channel operations, together with the overall data flow of System/370 Model 125 and physical locations. *Chapter 2* describes the principles of operation of the multiplexer channel. *Chapter 3* describes the operation of the multiplexer channel in detail. Flowcharts of the MPX microprogram show the major objectives of the operations and instructions. *Chapter 4* describes the major units of the multiplexer channel. Maintenance information is given in *Chapters 5 and 6. Chapter 7* contains a combined abbreviations list and glossary of terms. Common abbreviations for the system and an explanation of the symbols used are given in *IBM 3125 Processing Unit, General System Information,* Maintenance Library Manual, Order No. SY33-1059.

Prerequisite Reading

IBM 3125 Processing Unit, Microinstructions, Maintenance Library Manual, Order No. SY33-1058.
IBM 3125 Processing Unit, General System Information, Maintenance Library Manual, Order No. SY33-1059.
IBM 3125 Processing Unit, Input/Output Processor, Maintenance Library Manual, Order No. SY33-1063.
IBM System/360 and System/370 I/O Interface Channel to Control Unit, Original Equipment Manufacturers Information Manual, Order No. GA22-6974.

Associated Publications

IBM System/360 Principles of Operation, Systems Library Manual, Order No. GA22-6821.
IBM System/370 Principles of Operation, Systems Library Manual, Order No. GA22-7000.
IBM 3125 Processing Unit, Power Supplies, Maintenance Library Manual, Order No. SY33-1060.
IBM 3125 Processing Unit, Main Storage Controller, Maintenance Library Manual, Order No. SY33-1061.
IBM 3125 Processing Unit, Instruction Processing Unit, Maintenance Library Manual, Order No. SY33-1062.
IBM 3125 Processing Unit, Magnetic Tape Adapter, Maintenance Library Manual, Order No. SY33-1064.
IBM 3125 Processing Unit, Service Processor Subsystem, Maintenance Library Manual, Order No. SY33-1065.
Section 1: Service Processor (SVP).
Section 2: Console Disk File.
Section 3: Display Unit and Keyboard.
IBM 3125 Processing Unit, Main Storage, Maintenance Library Manual, Order No. SY33-1066.
IBM 3125 Processing Unit, 2560 Attachment, Front End, Maintenance Library Manual, Order No. SY33-1068.
IBM 3125 Processing Unit, 3525 Attachment, Front End, Maintenance Library Manual, Order No. SY33-1070.
IBM 3125 Processing Unit, 3504 Attachment, Front End, Maintenance Library Manual, Order No. SY33-1071.
IBM 3125 Processing Unit, 1403 Attachment, Front End, Maintenance Library Manual, Order No. SY33-1072.
IBM 3125 Processing Unit, 3330 Direct Disk Attachment, Maintenance Library Manual, Order No. SY33-1073.
IBM 3125 Processing Unit, Integrated Console Matrix Printer Attachment, Maintenance Library Manual, Order No. SY33-1074.
IBM 3125 Processing Unit, Integrated Communications Adapter, Maintenance Library Manual, Part B/M1876075.
IBM 3125 Processing Unit, Installation Instructions, Maintenance Library Manual, Part 4014001.
IBM 3125 Central Test Manual, Maintenance Library Manual. Contains pages appropriate to the individual 3125 Processing Unit.
IBM 3125 Processing Unit, Parts Catalog, Maintenance Library Manual, Order No. S135-1000.

Contents

Safety

Personal Safety

Personal safety cannot be over-emphasized; it is a vital part of customer engineering. To ensure your safety and that of co-workers, always observe the safety precautions given during your safety training and adhere to the following:

General Safety Practices

Observe the general safety practices and the procedure for performing artificial respiration that are outlined in *CE Safety Practices* card, order no. S229-1264 (shown here).

Grounding

Ground current may reach dangerous levels. Never operate the system with the grounding conductor removed.

Line-Powered Equipment

Ground all line-powered test equipment through the third-wire grounding conductor in the power cord of the machine being tested.

Machine Warning Labels

Heed the warning labels placed in hazardous areas of the machines.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. — use suitable rubber mats purchased localiy if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE YOUR EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. The maximum load to be lifted is that which in the opinion of you and management does not jeopardize your own health or well-being or that of other employees.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.
12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope — do not touch ANYTHING — it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machines while performing and after completing maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT — ELIMINATE UNSAFE ACTS

11/71 S229-1264-2

Artificial Respiration

GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects — Pull tongue forward.
3. **Loosen Clothing — Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Reprint Courtesy Mine Safety Appliances Co.

Rescue Breathing for Adults
Victim on His Back Immediately

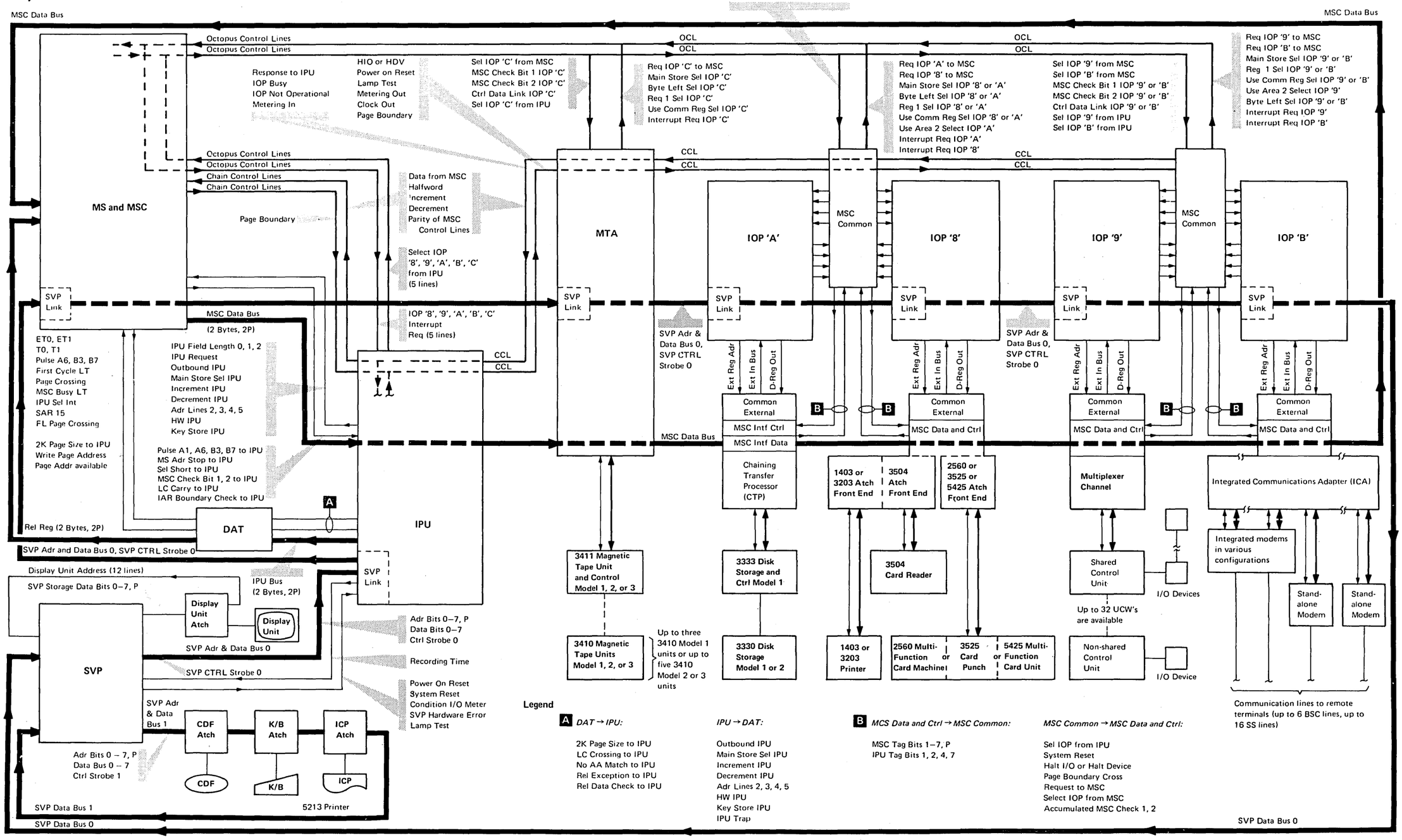
1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. Blow until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

Thumb and finger positions

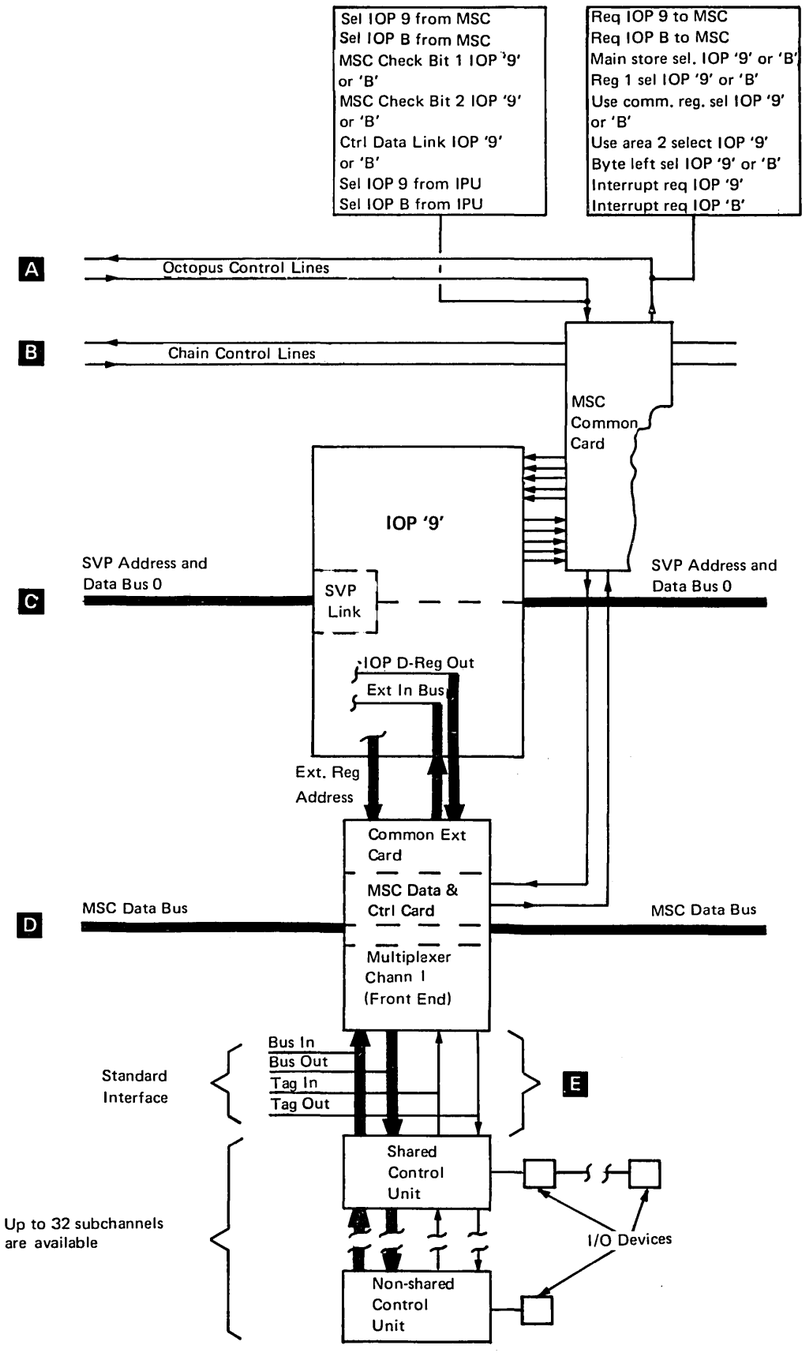
Chapter 1. Introduction

System Data and Control Flow



General Information

- The multiplexer channel is a specific Front End that is connected to IOP '9'.
- The functions of the multiplexer channel are as follows:
  Analyzes the I/O instruction.
  Initiates the operation of the I/O device.
  Controls data transfers between I/O devices and MSC.
  Requests interrupts.
- The multiplexer channel normally serves I/O devices that have relatively low data transmission rates.
- The multiplexer channel can operate in two different modes:
  1. Byte mode (25 kilobytes per second).
  2. Burst mode (29 kilobytes per second).
- All multiplexer functions, except interrupt requests, are initiated by the I/O instructions(refer to Page 2-020) and are under microprogram control.
- The microprogram is stored in the control storage of IOP '9'.
- The microprogram principle is shown on Pages 2-080 and 2-090. Detailed microprogram flowcharts are given on Pages 3-020 to 3-080 and 5-030.
- Multiplexer modes are defined by the control units that are connected to the standard interface. (For more details, refer to Pages 2-050 and 2-055.),



System Internal Buses

- Interconnection between multiplexer channel and the system is made via IOP '9' and the system internal buses.
- The system internal buses are:

A 12-line bus (see Note) containing octopus control lines (OCL)

B 16-line bus containing chain control lines (CCL)

C 17-bit SVP Address and Data Bus
(Address Bus is 9 bits);
Data Bus is 8 bits)

D 18-bit MSC Data Bus.

Note: These 12 lines are used by one IOP.

For detailed information refer to *IBM 3125 Processing Unit Input /Output Processor,* Maintenance Library Manual, order number SY33-1063.

Standard Interface

- I/O devices with their control units are connected to the multiplexer channel via a standard interface.
- The standard interface consists of four groups of lines:

E
- One-byte Bus In
- One-byte Bus Out
- 7 Tag in lines
  (6 part of standard interface part of IBM System 370 interface extension)
- 7 Tag Out lines fall part of the standard interface)

- The standard interface cables are connected to the multiplexer channel by:
  Bus "serpent" connectors, and
  Tag "serpent" connectors.
- For the explanation of the standard interface Tag lines, refer to Page 4-040.

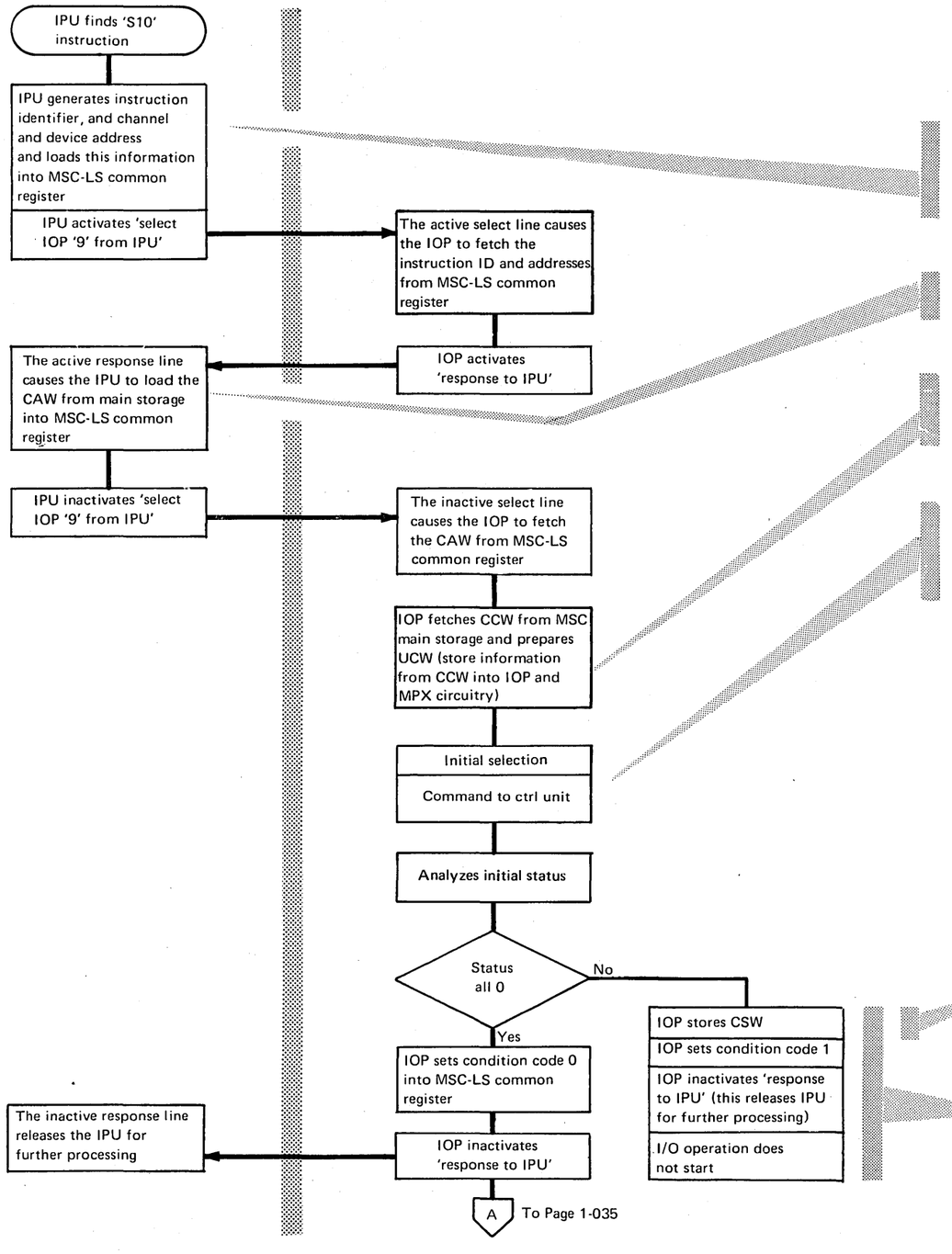
Channel Operation

Initialization

This flowchart shows:

- Communication between IPU and IOP/multiplexer channel during initiation of an I/O instruction. (The 'SIO' instruction is used as an example.)
- Activation and inactivation of:
  a. 'Select IOP from IPU' (OCL) line and
  b. 'Response to IPU' (CCL) line.

For further details refer to "General Microprogram Flow" on Pages 2-080 and 2-085, and to "Multiplexer Microprogram" on Pages 3-020 to 3-040.



For details about instruction identifier and MSC-LS common register layout, refer to *IBM 3125 Processing Unit, Input/Output Processor,* Maintenance Library Manual, Order SY33-1063.

Address range of device addresses are shown on Page 2-070.

CAW layout and location in main storage are shown on Page 2-020.

All necessary device individual information that is required to control an I/O operation is held in the UCW that is assigned to the device. (UCWs are also called subchannel). UCW layout is shown on Page 2-025. UCW addressing is shown on Page 2-070.

Before the operation is started the control unit of the device is selected (initial selection) and the control unit presents an initial status. This status shows whether the I/O device is able to perform the operation, or whether any unusual conditions exist which would prevent the operation from starting.

CSW layout and location in main storage are shown on Page 2-020.

For more details, refer to the "ending sequence" shown on Page 4-050. Refer also to the microprogram flowcharts on Page 3-040.

Data Transfers

Two operation types can be performed with the MPX

- Read type operation
- Write type operation.

The flow chart on this page shows:

- Data transfers for a read type operation (from control unit to MPX and from MPX to main storage)
- Data transfers for a write type operation (from main storage to MPX and from MPX to control unit)
- Channel End and
- Device End presentation.

Data transfers between main storage and IOP/MPX take place for a

- Read type operation: as soon as data byte or halfword is available in MPX
- Write type operation: as soon as data byte is required in MPX.

Transfer conditions to MSC are specified by chain- and octopus-control lines.

Refer also to microprogram flow charts on pages 3-040 to 3-070.

Data transfers between IOP/MPX and I/O devices are always

- byte transfers.

Transfer conditions are specified by TAG IN- or TAG OUT-lines.

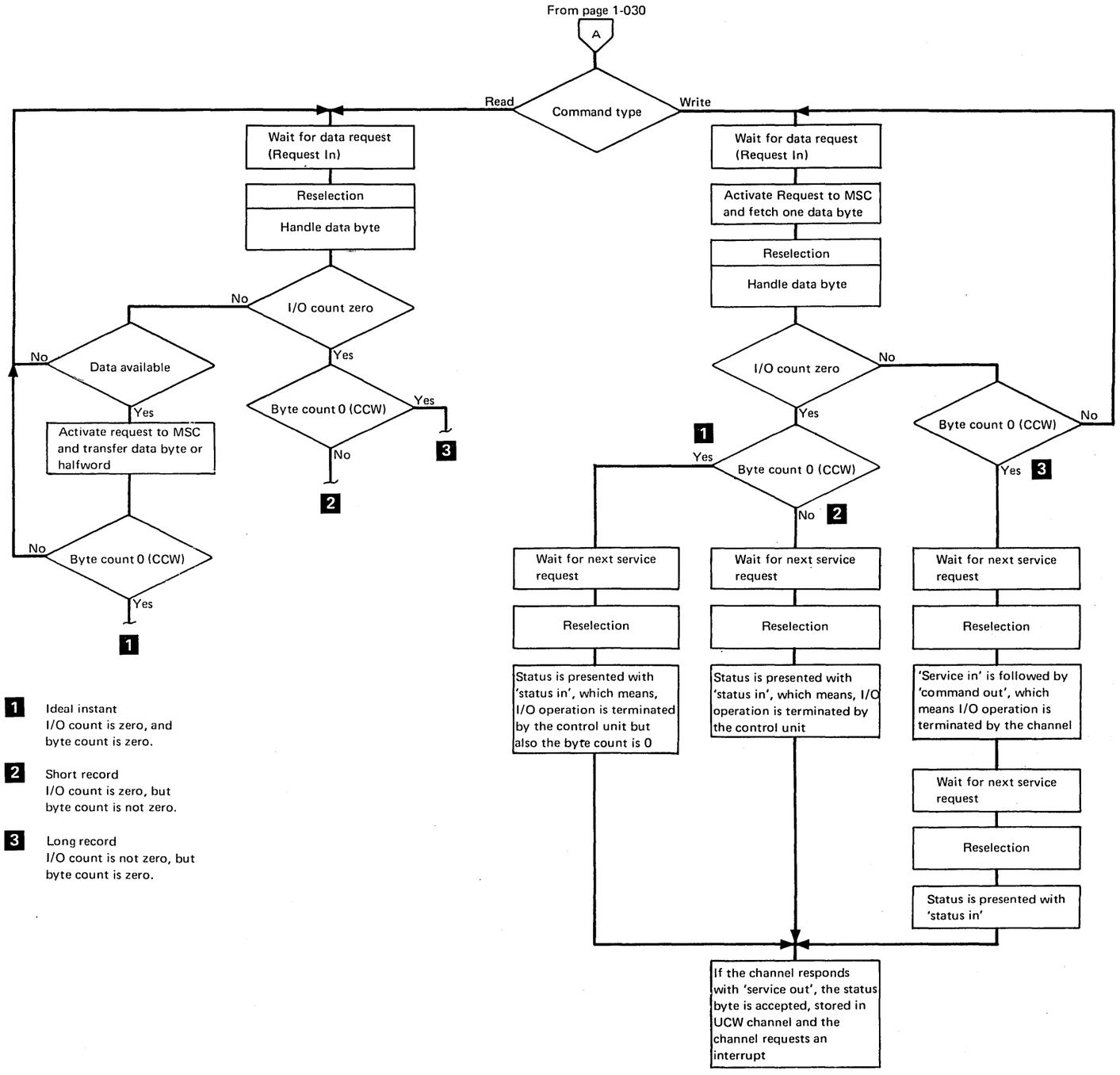
- Channel end is generated by the control unit, as soon as the data transfer between channel and control unit is terminated.

Either with channel end alone or with channel and device end together (designated as primary status) the channel requests an interrupt. Status byte is held in the UCW which keeps the channel free for further operations, while the subchannel remains with a pending interrupt until the interrupt request is accepted by the IPU.

- Device end is generated by the control unit, as soon as the I/O device has completed its mechanical operation. This means, generation of device end very much depends upon the type of I/O device.

Device end condition (designated as secondary status) is rejected by the channel ('status in' is followed by 'command out') and stacked in the control unit. Further status presentation is suppressed by the channel (by activating 'suppress out').

The channel requests an interrupt and the I/O device remains with a waiting interrupt until this interrupt request is accepted by the IPU and the channel has fetched the status byte.



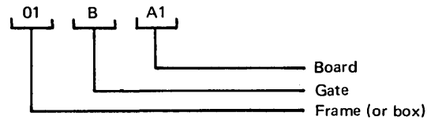
1 Ideal instant
I/O count is zero, and
byte count is zero.

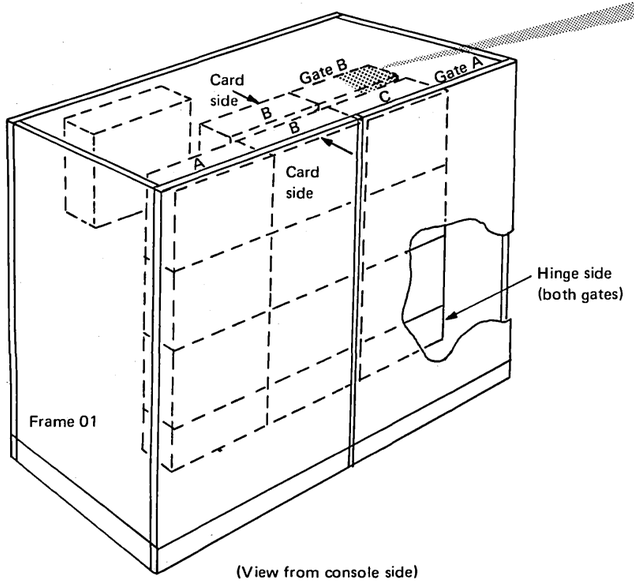
2 Short record
I/O count is zero, but
byte count is not zero.

3 Long record
I/O count is not zero, but
byte count is zero.

Physical Locations

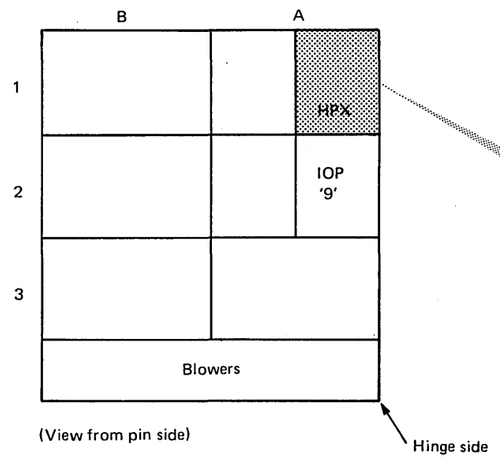
- This page shows the physical location of the multiplexer channel cards.
- The actual location is





(View from console side)

Board Location



(View from pin side)

MPX Control Card

- See Pages 4-070 and 4-075.
- ALD Pages are KA 22X.

External Register Card

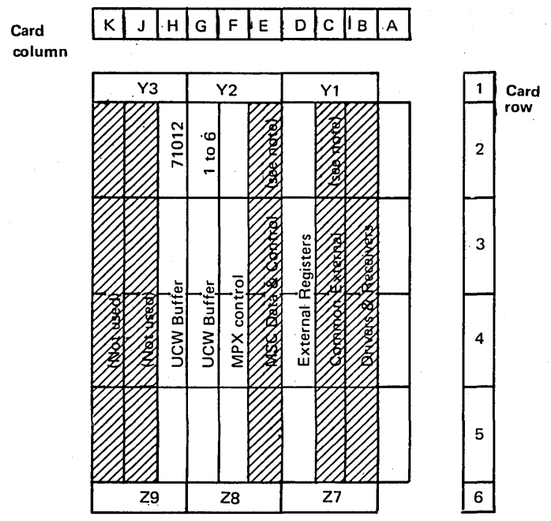
- See Page 4-080.
- ALD Pages are KA 28X.

UCW Buffer Cards

- See Page 4-090.
- ALD Pages are KA 10X and KA 16X.

Note: The common external card and the MSC data and control card are described in *IBM 3125 Processing Unit, Input/Output Processor,* Maintenance Library Manual order SY33-1063.

Card Location



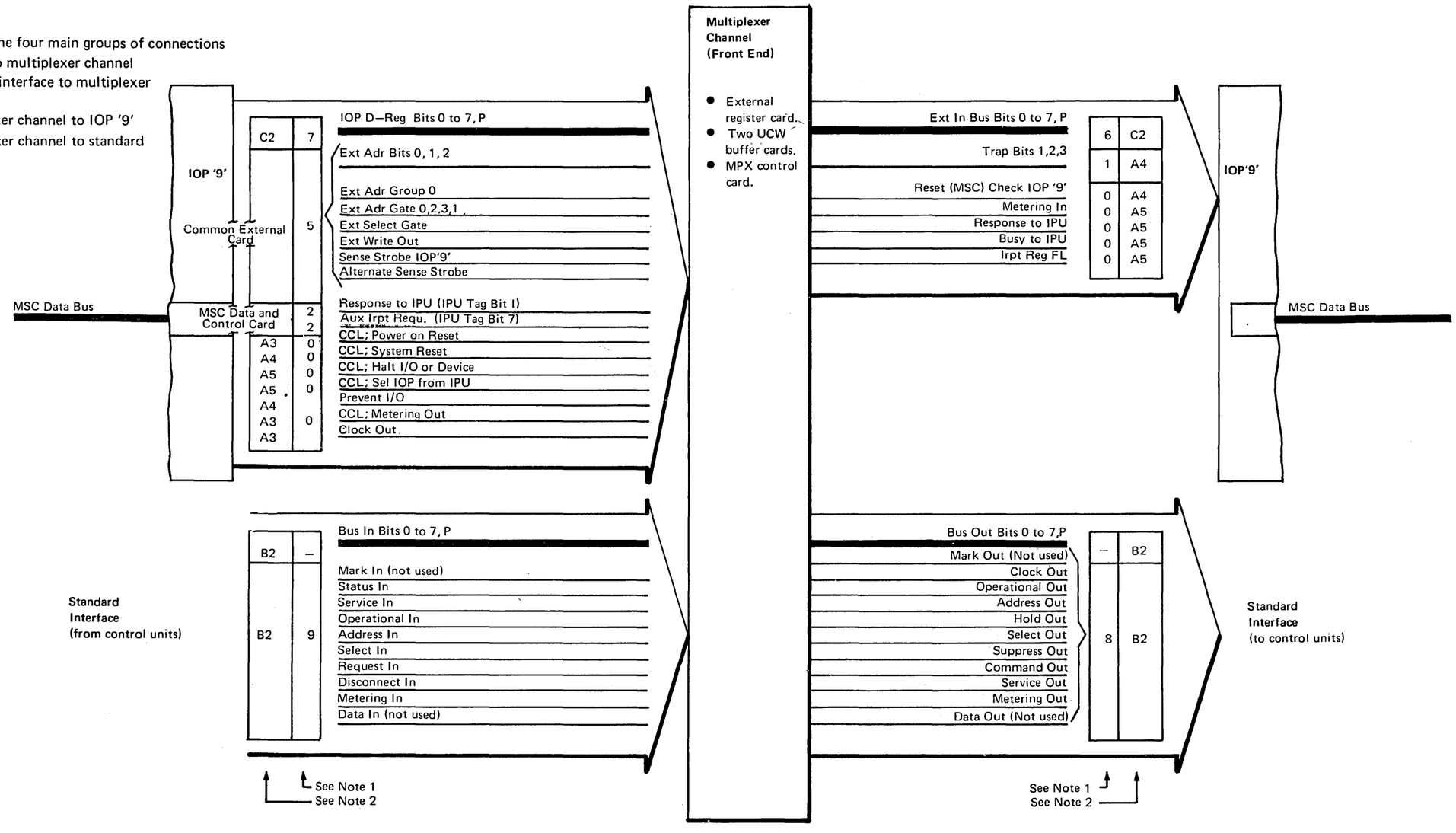
(View from pin side)

Not described in this manual.

Signal Interface

This page shows the four main groups of connections

- from IOP '9' to multiplexer channel
- from standard interface to multiplexer channel
- from multiplexer channel to IOP '9'
- from multiplexer channel to standard interface.



Note 1: The numbers in these columns define the line groups as they are shown on Page 4-010 and described on Pages 4-030 and 4-040.

Note 2: These letter/number combinations define the plug locations of the cables on multiplexer channel board.

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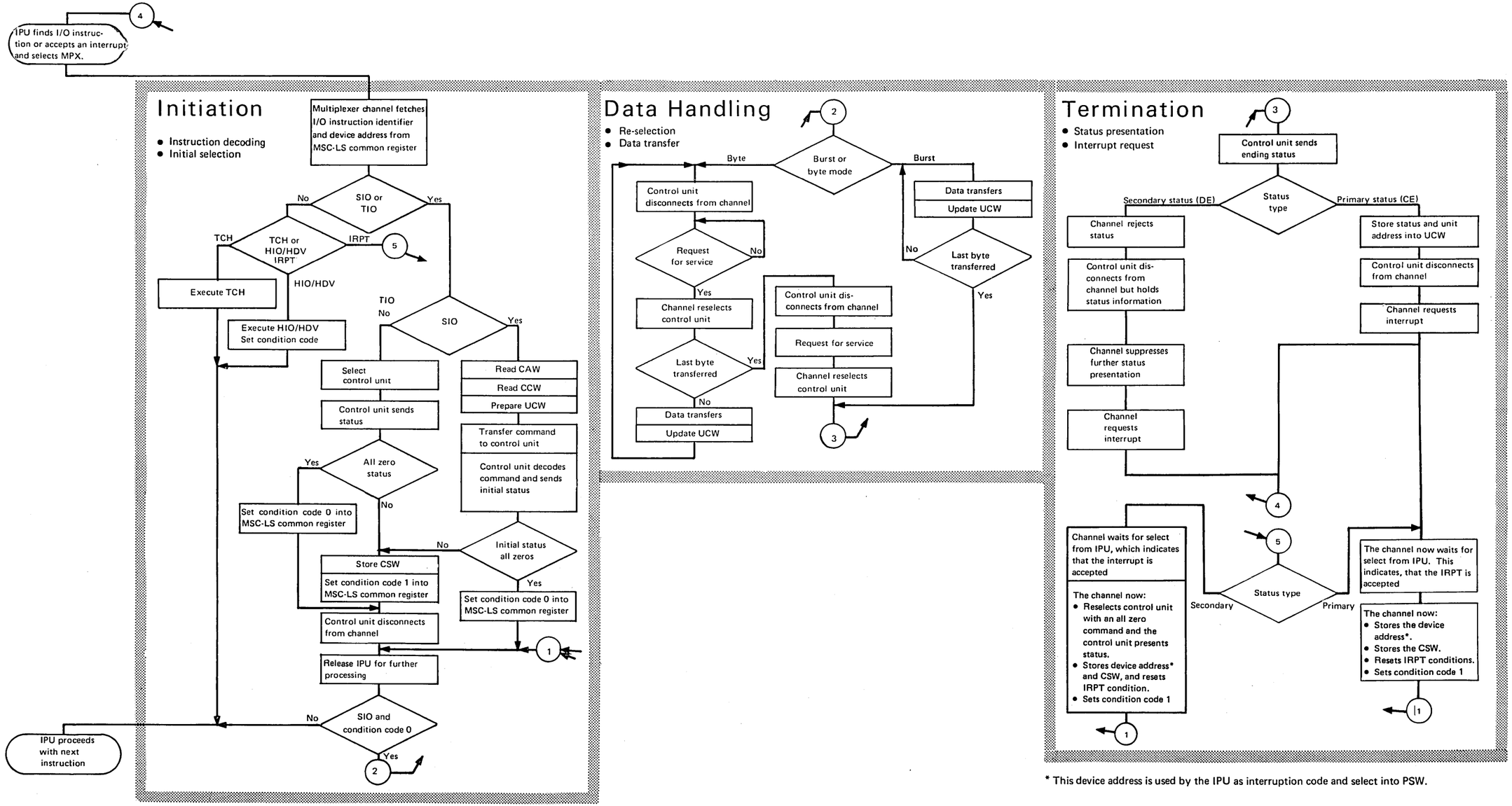
Chapter 2. Principles of Operation

Any channel operation can be divided into three major portions:
Initiation
Data Handling
Termination.
These three functions are described on this page. For further details, refer to the "Multiplexer Microprogram" on Pages 3-020 to 3-080.

With this flowchart it is assumed, that in all cases the I/O device is available. I/O instructions to devices, that are busy or not operational, are not included here.
For more details refer to pages 2-080, 2-085, 2-090, 3-020 through 3-080.



* This device address is used by the IPU as interruption code and select into PSW.

I/O Instructions

The following instructions are used with the multiplexer channel:
Start I/O (SIO)
Halt I/O (HIO)
Halt device (HDV)
Test I/O (TIO)
Test channel (TCH)
Store channel identifier (STIDC)
Start I/O fast release (SIOF)

Start I/O (SIO)

Initiates an I/O operation. The address part specifies channel and device. The actual I/O operation is specified by the command in the CCW.

Halt I/O (HIO)

Terminates an operation that was started by an 'SIO' instruction. The termination is performed in the electronic circuitry while the mechanical operation of the device runs until its normal end.

Assume that two devices A and B are connected to a channel.

1. If both devices are working in multiplex mode, the addressed device is asked to stop without affecting the other device.
2. If device A is currently not working, but device B is working in burst mode, an 'HIO' to device A would stop device B.

Halt Device (HDV)

Terminates an operation that was started by an 'SIO' instruction. The termination is performed in the electronic circuitry while the mechanical operation of the device runs to its normal end.

The addressed device is asked to stop. As long as one device operates in burst mode, an 'HDV' to another device is not performed until the burst operation of the first device is completed.

Test I/O (TIO)

Set a condition code into the PSW to indicate the status of the addressed channel, subchannel and device. A CSW may be stored. This instruction may also be used to clear interrupts.

Test Channel (TCH)

Sets a condition code into the PSW to indicate the status of the addressed channel.

Store Channel Identifier (STIDC)

This instruction is completely handled by the IPU and sets four bytes of information into main storage at location 168 (decimal); see "Formats".

Start I/O Fast Release (SIOF)

This instruction is handled like an 'SIO' instruction.

Formats

I/O Instructions Format in main storage

0 7	8 14	15	16 19	20 31
Op-Code	Ignored	*	Register Address	Displacement

* for 'HDV' only

All I/O instructions use this format. The displacement is added to the contents of a specified register; the result then represents the channel and device address.

From the Op-code an *instruction identifier* is generated.

The device address and instruction identifier are then transfered, via MSC-LS common register, to the multiplexer channel.

(Format after processing in IPU)

0 3	4 15	16 23	24 31
(not used)		Channel address	Device address
Ch. Type	Ch. Model Number	Set to zero	

After successful generation of fetched channel and device address the CAW is fetched.

Layout of the four bytes stored (by the IPU) with STIDC

Channel Address Word (CAW)

- Located in MSC main storage position 72 decimal (48 hexadecimal)

0 3	4 7	8 31
Key	Zeros	Command Address

The command address of the CAW specifies the location of the first CCW in the main storage

Channel Command Word (CCW)

- Essential parts stored into UCW of address device

0 7	8 31	32 37		40	48 63
Command	Data Address or, if TIC, New CCW Address	Flags	Zero	Ignored	Length Count or Byte Count

CCWs have to be located on double word boundaries in main storage. After a CCW is transferred to the multiplexer channel and the command does not contain a TIC, the specified command is initiated.

If IDA flag is set, data are addressed indirect via IDA List, whose address is specified in CCW.

Data transfer ends when either the byte count or the I/O count reaches zero.

3 ending conditions are normal

- CCW count 0, I/O count 0
- CCW count 0, I/O count not 0
- CCW count not 0, I/O count 0.

After the last byte is transferred, the MPX requests an Interrupt. If accepted, interruption code (dev. as is set into PSW and either stator, complete CSW is stored according to conditions during the I/O operation.

Commands are:

read	(transfers data from device to MSC)
write	(transfers data from MSC to device)
read backward	(read, but in reverse order)
sense (SNS)	(device information to MSC)
control (CTL)	(set up conditions in addressed device)
TIC	(transfer in channel); allows branching in strings of CCWs and does not initiate any I/O operation).

'Sense' and 'control' commands do not actually transfer I/O data The 'sense' command fetches the sense bytes from a selected control unit and device. The 'control' command sets control information into a selected control unit and device.

Flags are:

32 = CD (chain data). (only with read commands)
33 = CC (chain command)
34 = SILI (suppress incorrect length indication)
35 = Skip (allows suppression of transfer of zero bytes)
36 = PCI (allows program controlled interrupts)
37 = IDA (indirect data addressing is specified)

Channel Status Word (CSW)

- Located in MSC main storage position 64 decimal (40 hexadecimal)

0 3	4 7	8 31	32 39	40 47	48 63
Key	Zeros	Command address	Unit or Device Status	Channel Status	Residual Count

Command Address = Last CCW address +8

32 = Attention
33 = Status modifier
34 = Control unit end
35 = Busy
36 = Channel end
37 = Device end
38 = Unit check
39 = Unit exception
40 = PCI (program - controlled interrupt)
41 = Incorrect length
42 = Program check
43 = Protection check
44 = Channel data check
45 = Channel control check
46 = Interface control check
47 = Chaining check

Residual Count = Number of bytes that have not been transferred

Formats (continued)

Unit Control Word (UCW)

The multiplexer channel allows simultaneous operation of several I/O devices. Normal mode for the multiplexer channel is, therefore, byte mode.

Because a data transfer of one device may be followed by a data transfer of another device, the conditions of the progress in these data transfers must be individually stored for each I/O device. This is done in the UCW, which is also called a subchannel.

Each UCW is 24 bytes wide. One group of 12 bytes contains:

- Next IDA word address
- Next command address
- ECSW bytes
- Device address
- Unit status.

This group is stored in control storage of IOP '9'.

Another group of 12 bytes contains:

- Flags and operation control
- Key and actual data address
- Byte count
- Buffer byte
- Next data address
- Channel status.

This group is stored in a separate UCW storage area located on the multiplexer channel board.

For a description of the UCW buffer card, refer to page 4-090.

UCW portion, stored in control storage of IOP '9'

0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7,P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P
Next Command Address			ECSW Bytes				Next IDA Word Address			Device Address	Unit Status
			1	2	3	4					

(A definition of bits is given on Pages 2-020 and 5-010).

These numbers specify the hexadecimal external address.

UCW portion, stored in UCW buffer of MPX Front End

02	03	06	07	0A	0B		0E	0F	12	13	16	17
0 to 7, P	0 to 7, P	0 to 7, P	0 to 7,P	0 to 7, P	0–3	4–7P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P	0 to 7, P
Flags and Operation Control. The meaning of each bit is shown on Page 3-100		Byte Count		Buffer	Key		Actual Data Address		Channel Status (A definition of bits is given on Pages 2-020 and 5-010.)	Next Data Address		

ECSW Bytes

1. Contains detect field, here the unit that detected the error is identified.
2. Contains source field, here the unit that probably caused the error is identified.
3. Contains validity flags to indicate validity of the information stored in designated fields.
4. Contains type of termination and sequence code.

Unit status — indicates conditions, detected by the I/O device or control unit. These conditions are indicated to the channel via standard I/O interface. The channel does not modify the status bit pattern and stores the status byte into CSW as it was received from the control unit.

Channel status — indicates conditions detected by the channel, except those that are caused by equipment mal-function during execution of an I/O operation.

Buffer — is used as a work register and may hold different information during an I/O operation. Its main use is to hold one I/O data byte for preparing halfword transfers to main storage with read operations.

Write Type Operation

These two pages show the manner in which a write operation is performed. The paragraphs should be read in numerical order. Data is transferred from main storage to the I/O device. The data path is from MSC Data Bus to Std Interface Bus Out.

For further details refer to the microprogram flowcharts shown on Pages 3-060 and 3-070.

3

- IOP '9' D-register controls are set in such a way, that write data from the 'external in bus 1' is set into the IOP '9' D-register.

2

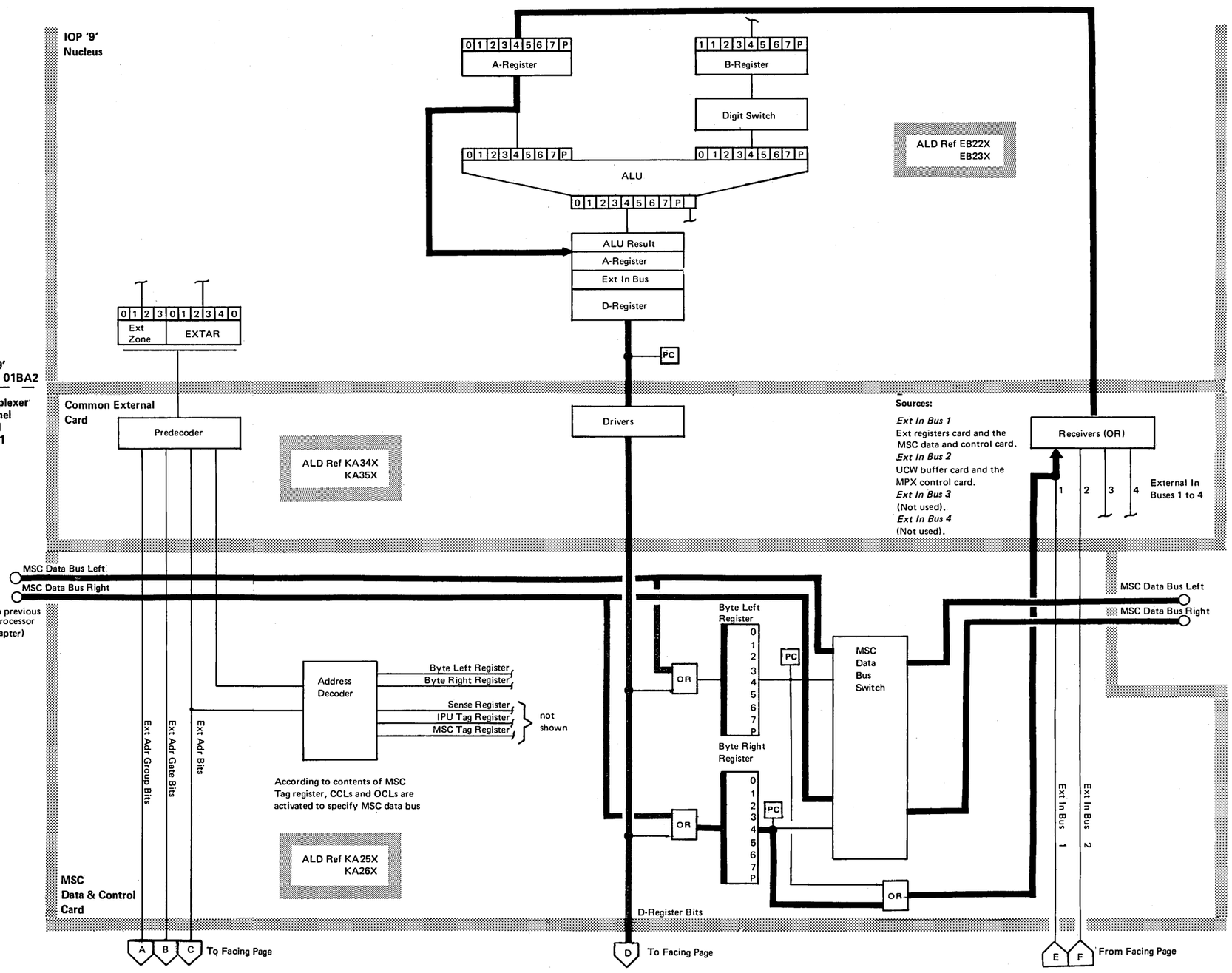
- Write data is gated via 'external in bus 1' to IOP '9' D-register.

4

- The contents of IOP '9' D-register are gated to the external register card.

1

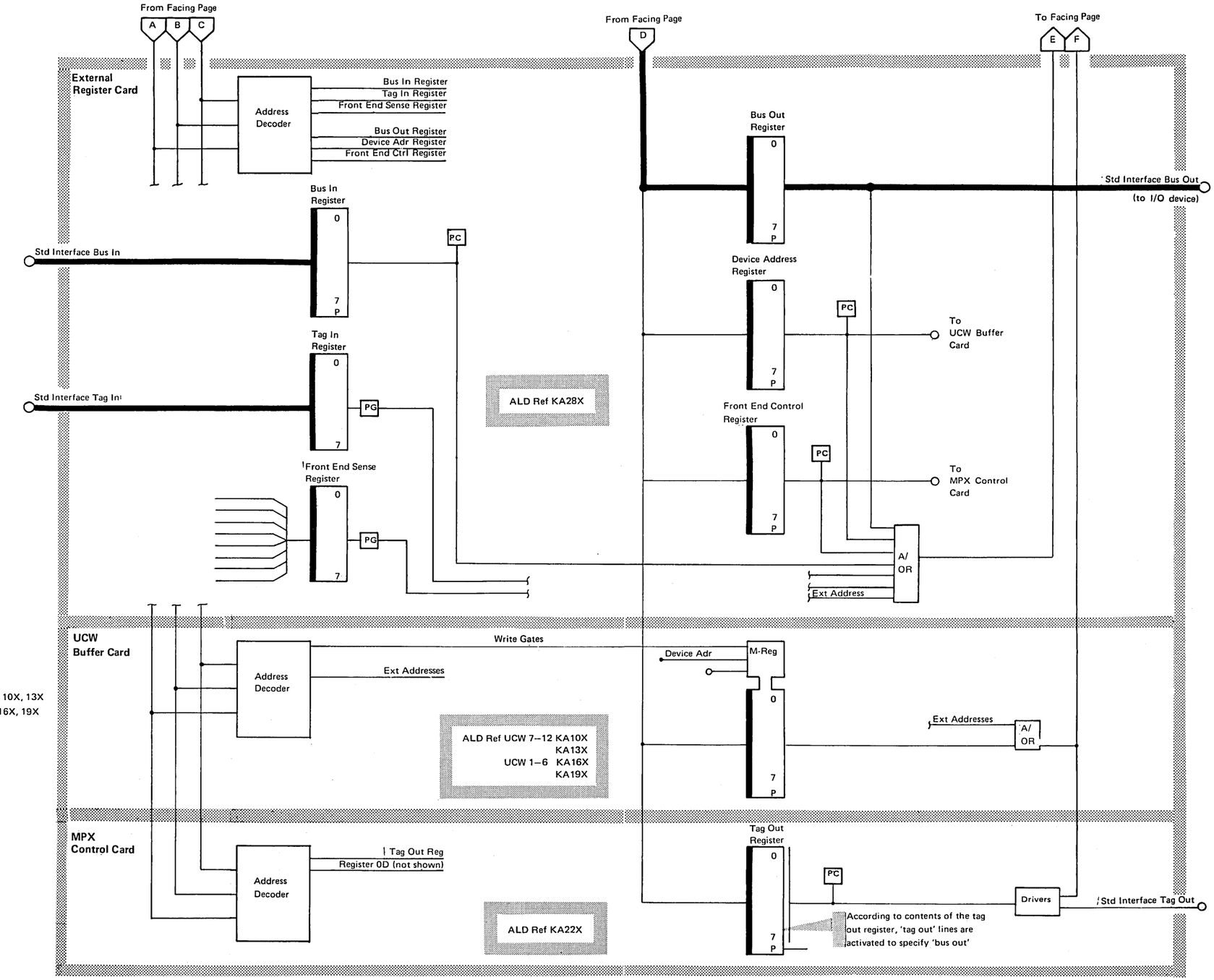
- As soon as a device requires service, this device causes activation of 'Trap 1 request', which forces the multiplexer channel microprogram to its data handling routine.
- The data handling routine controls data path between MSC data bus registers and bus out register.
- Controls of MSC data bus registers are activated according to the micro-program steps of the data handling routine.
- With write operations, only byte transfers and forward operations take place. Thus, a data byte is set into the byte right register and gated via 'external in bus 1' into the IOP D-register. (The contents of the byte left register are ignored.)



A
B
C
D
E

5

- Write data is set from the IOP '9' D-register into the bus out register.
- Activation of respective 'std interface tag out' lines is done under control of the multiplexer channel microprogram.



UCW 7–12 KA 10X, 13X
UCW 1–6 KA 16X, 19X

Read Type Operation

These two pages show the manner in which a read operation is performed. The paragraphs should be read in numerical order. Data is transferred from the I/O device to main storage. The data path is from Std Interface bus in to MSC Data bus.

Byte and halfword transfers can take place with a read operation (see "Data Transfer Conditions").

For further details refer to the microprogram flowcharts given on Pages 3-060 and 3-070.

3

- IOP '9' D-register controls are set in such a way that read data from external in bus is set into the D-register.

2

- Read data is gated via External In Bus 1 to IOP '9' D-register

4

- The contents of IOP '9' D-register are gated to MSC data bus registers.

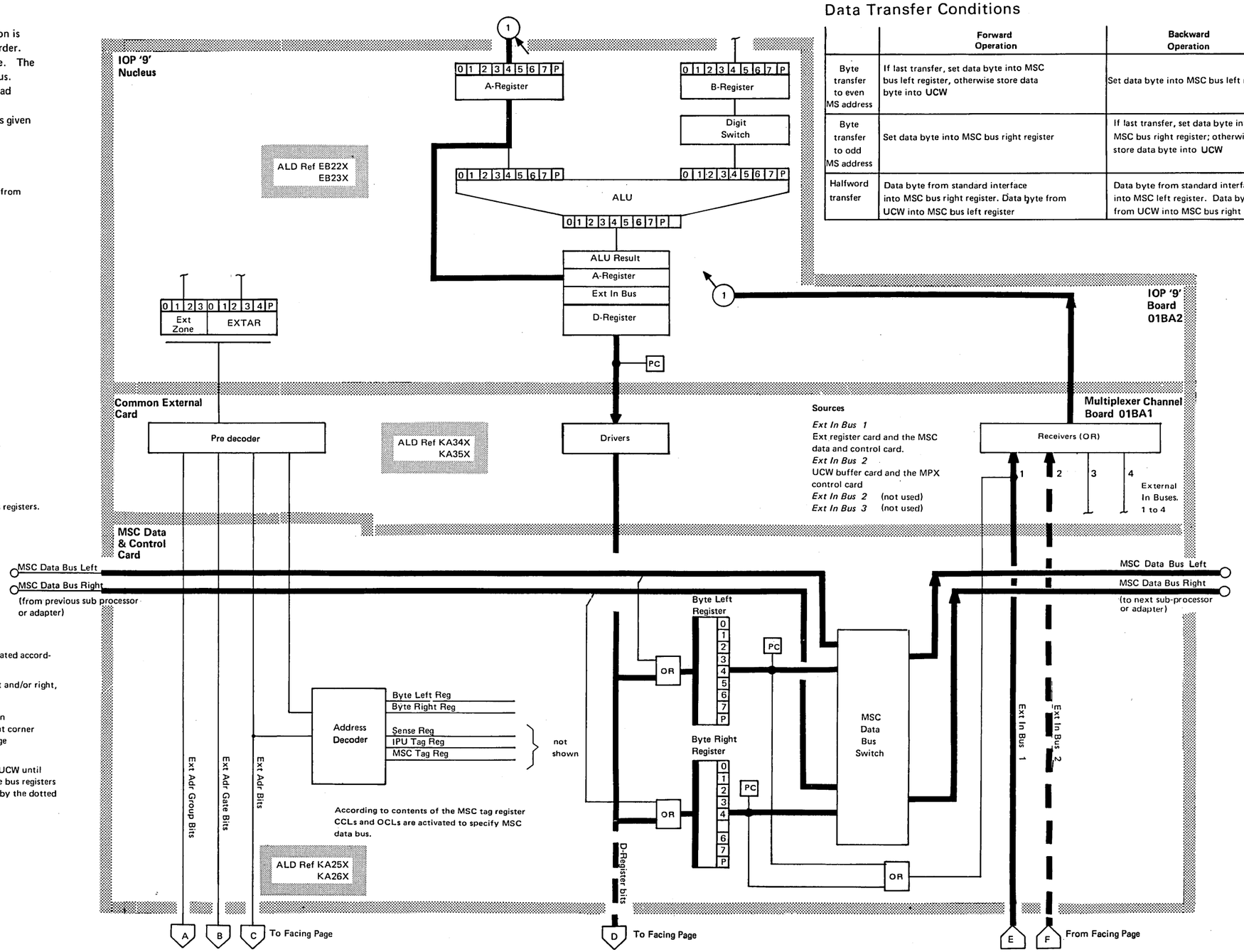
5

- The controls of MSC data bus registers left and right are activated according to microprogram steps of the data handling routine.
- The contents of IOP '9' D-register are set into bus register left and/or right, according to data transfer requirements.
- The data transfer requirements depend upon:
  a. Forward or backward operation and
  b. last byte transfer or
  c. halfword or byte transfer.

  } see table in upper right corner of this page
- For halfword transfers, the first data byte read is held in the UCW until the second data byte is read. Then both bytes are set into the bus registers and are transferred to main storage (along the path indicated by the dotted line ▬ ▬).

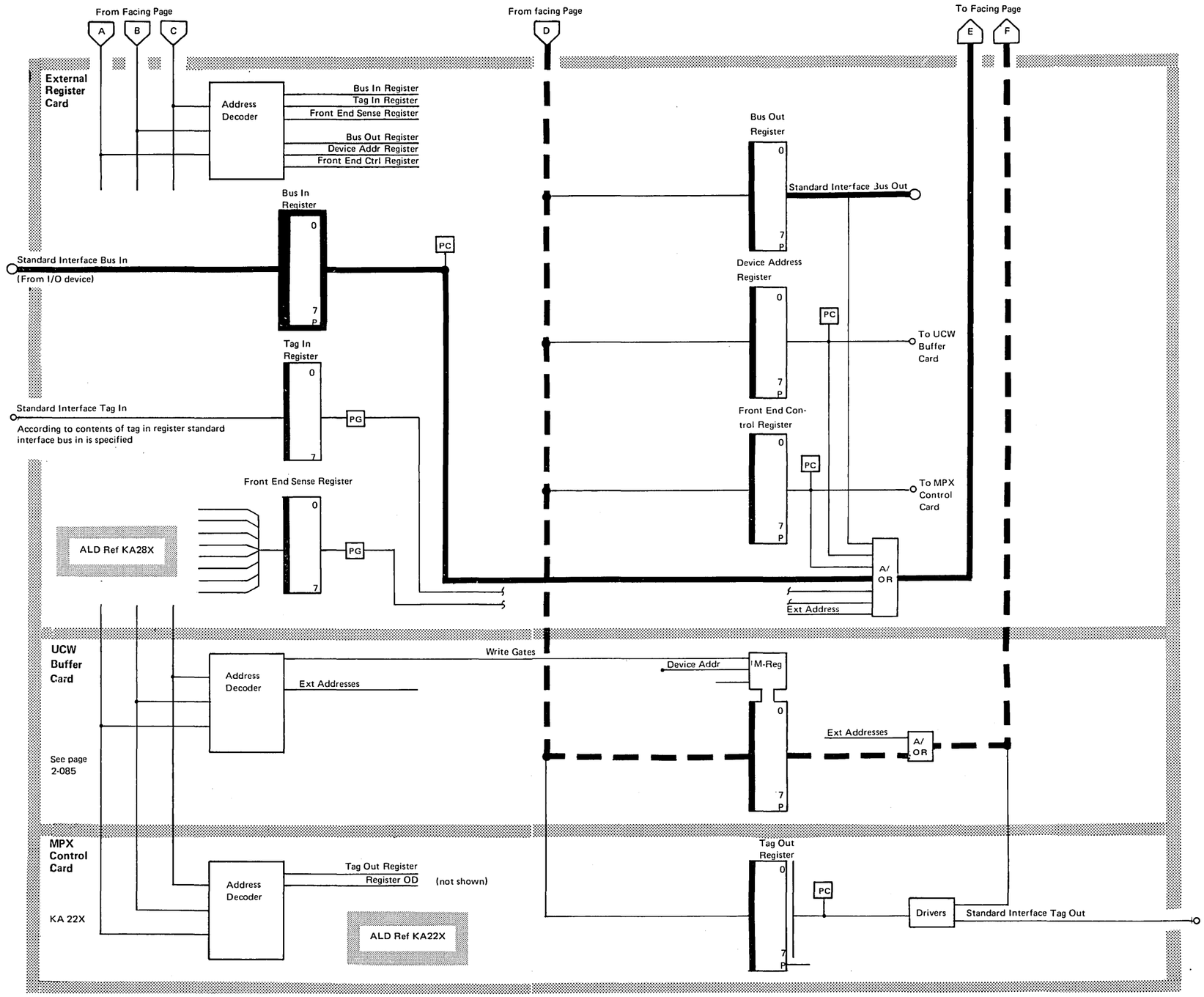
Data Transfer Conditions

	Forward Operation	Backward Operation
Byte transfer to even MS address	If last transfer, set data byte into MSC bus left register, otherwise store data byte into UCW	Set data byte into MSC bus left register
Byte transfer to odd MS address	Set data byte into MSC bus right register	If last transfer, set data byte into MSC bus right register; otherwise store data byte into UCW
Halfword transfer	Data byte from standard interface into MSC bus right register. Data byte from UCW into MSC bus left register	Data byte from standard interface into MSC left register. Data byte from UCW into MSC bus right register



1

- As soon as a device requires service this device causes activation of 'trap 1 request', which forces the multiplexer channel micro-program to its data handling routine.
- The data handling routine controls the data path from the bus in register to the MSC data bus.
- At service In time data from standard interface is set in to Bus In register.
- Contents of Bus In register then are gated via External In Bus 1 to IOP '9' D-register.



Modes of Operation

Byte Mode

MPX can serve more than one device at a time in "Byte Mode".

Here one byte of one device is handled during one IOP cycle and one byte of another device is handled during a subsequent IOP cycle.

Because after a byte transfer the device disconnects from channel, one UCW is required per device in order to store control in formation of each device.

Each data transfer is initiated by a request from one device. The request is followed by a reselection of the device. After the data transfer is completed the device again disconnects from the channel and the channel waits for the next request. This procedure is repeated until the last byte of a record is handled or the byte circuit reaches zero.

With the next request following a data transfer, the status is presented to the channel. According to type of status this status will be accepted or stacked.

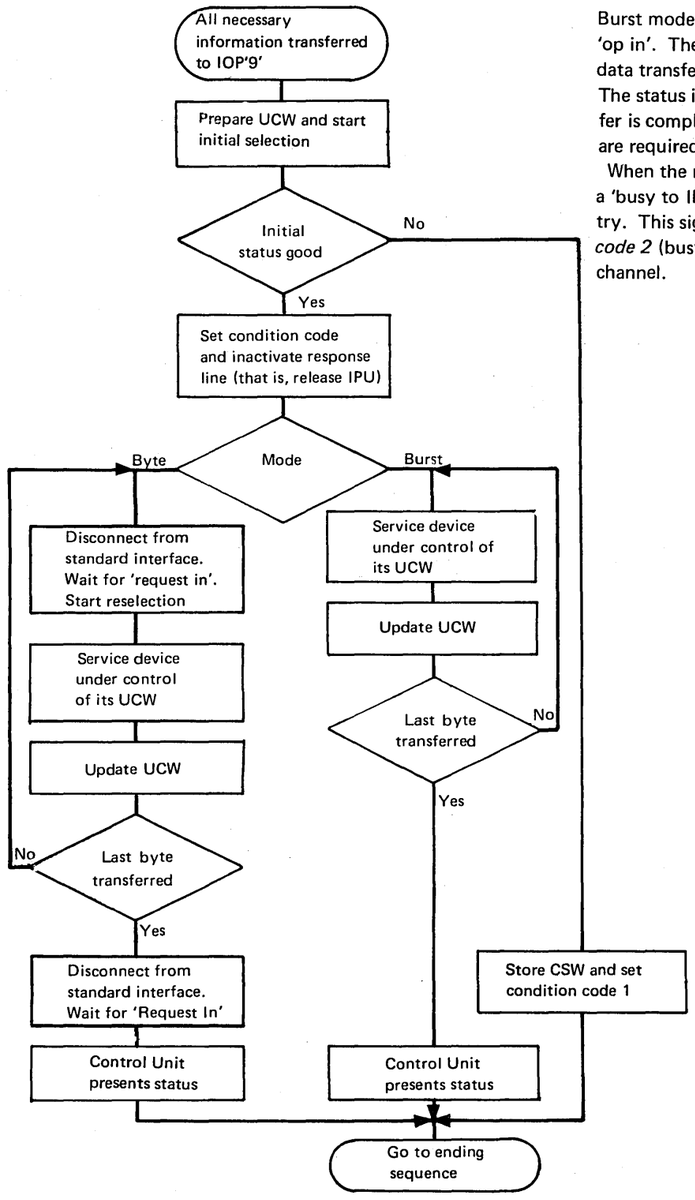
If accepted, the channel stores status information into the unit status byte (which is part of the UCW) and activates its 'interrupt request' line to the IPU.

If stacked the channel status is held in the control unit and has to be presented later.

Multiple Byte Mode

In principle *multiple byte mode* is the same type of operation as *byte mode*, but with the exception that a predetermined number of bytes is transferred.

Multiple byte mode and the number of bytes to be transferred are specified by the control unit by holding up 'op in' for as long as it is required.



Burst Mode

Burst mode is specified by the control unit by holding up 'op in'. The initial selection is directly followed by the data transfer of the complete record (first to last byte). The status is also directly presented after the data transfer is completed. (No separate request and re-selection are required.)

When the multiplexer channel is working in burst mode a 'busy to IPU' line is generated by the channel circuitry. This signal causes the IPU to generate *condition code 2* (busy) whenever the IPU selects the multiplexer channel.

Example of Byte Mode Operation

The IPU, when processing the customer program finds an 'SIO' instruction for device X in the stream of instructions.
The following actions now take place:
1. Select multiplexer channel
2. Transfer of necessary data to multiplexer channel
3. Prepare UCW
4. Start device
5. Release IPU for further processing.

The MPX microprogram returns to its idle loop and waits for the next selection from IPU, or for service request.

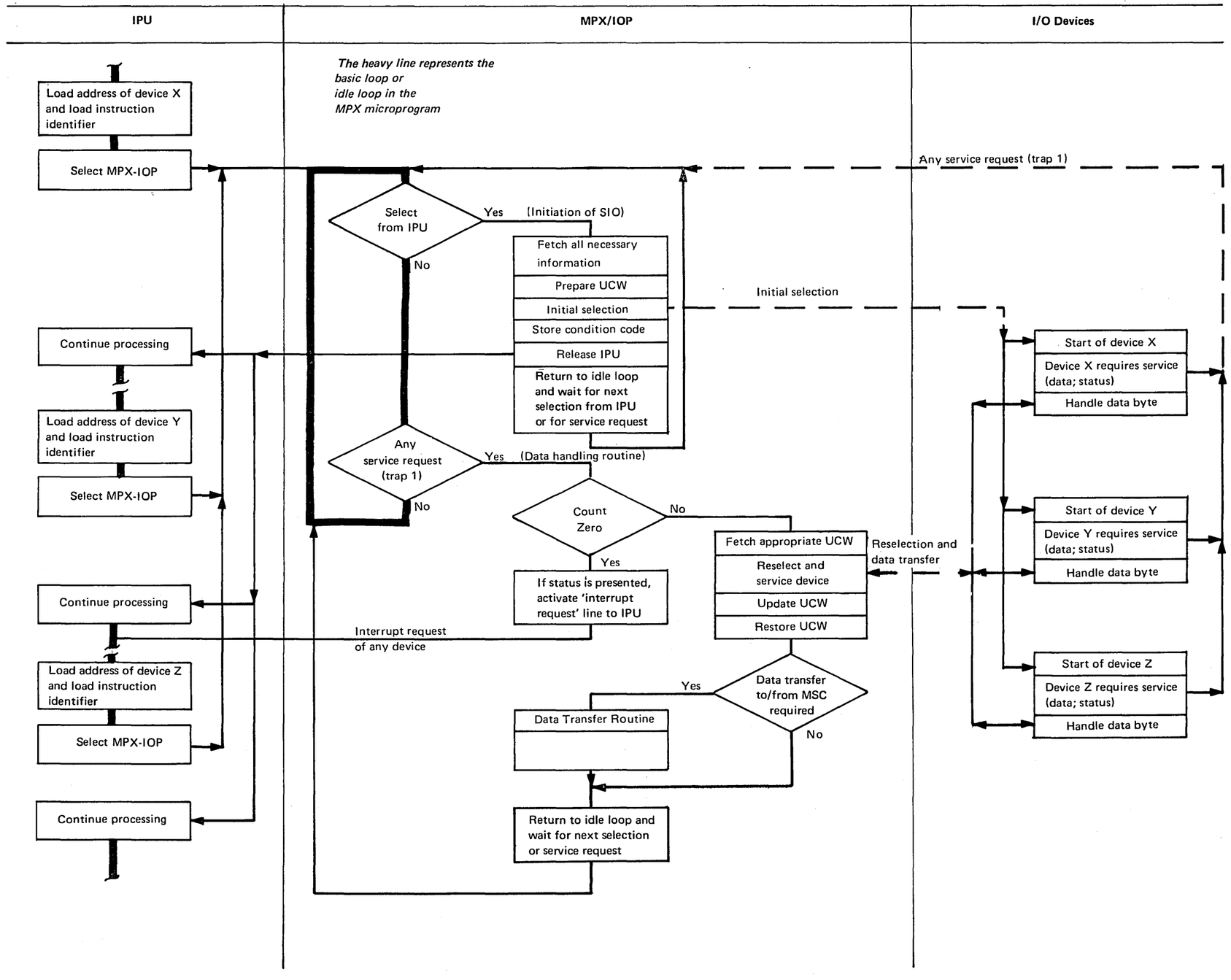
The IPU now continues executing the customer program and finds the next 'SIO' instruction in the instruction stream. The same actions (listed above) take place.

The IPU again continues executing the customer program and finds a third 'SIO' instruction in the instruction stream. The same actions listed above for first 'SIO' instruction take place and the IPU is again released for further processing. The MPX microprogram returns to its idle loop.

As soon as one of the devices requires service 'Trap 1 request' is activated, which causes the trap bit 1 to be gated to IOP '9' nucleus. This trap bit 1 forces the MPX microprogram to its data handling routine. The following actions now take place:
1. Load UCW of requesting device into work area
2. Reselect device
3. Handle data byte
4. Update and restore UCW

The MPX microprogram returns to its idle loop and waits for the next selection or service request.

Starting more than one device (byte mode) gives the impression that these devices are operated simultaneously. Actually, the mechanical operations of the started devices *are* running simultaneously, but only one device can be serviced at a time. This is because all the devices use the same circuitry and the same microprogram.



General Information

Microprogram

The multiplexer channel is completely controlled by microprogram. After successful loading of the MPX microprogram into the control storage of IOP '9', the microprogram idles in its basic loop and waits either for selection from IPU or for service requests from the I/O devices.

Five program levels exist (levels 0, 1, 2, 3, and 7) within the MPX microprogram. Switching from one level to another is achieved by an internal trapping system. Different jobs within the MPX microprogram are programmed at different program levels (also called trap levels). These trap levels also classify a priority sequence.

The following list shows the trap or program levels (from lowest to highest priority) and the jobs programmed at each level:

Ptr	Progm or TRAP Level	Priority	Job
0	0	Lowest	• Communication with IPU
1	1		• Data Transfer • Interrupt Request
2	2		• HIO/HDV in worst mode
3	3		• Error handling • System reset, start
	7	Highest	• System reset, execution

If a request for a specific job to be done becomes active, trap bits are generated in the multiplexer channel. These trap bits are gated to IOP '9' where they are ORed with the link portions of index words. (The trap register is located on the ALS/CSAR card).

Alteration of the link portion of an index word (comparable with a branch operation) causes a change of the chain of index words. This, in turn, causes the use of other IARs.

Level 0

In byte mode a new I/O operation can be started after all higher trap requests are serviced.

In burst mode the multiplexer channel does not accept a second SIO. The IPU terminates this second SIO as a result of the active 'IOP busy' line and sets condition code 2.

Level 1

Requests for data transfers are handled as soon as an I/O device requires service and all higher trap requests are serviced.

Requests for interrupts are placed after termination of an I/O operation by activating the line interrupt request. (Interrupt requests are the result of the status presentation.)

Level 2

I/O operations can be interrupted if the IPU issues an HIO or HDV to the multiplexer channel.

Level 3

If parity errors in distinct Front End registers are found or the 'system reset' line becomes active, or a standard interface 'tag in check' is detected, trap 3 is generated.

Trap bit 3 forces the microprogram to the error handling routine that prepares information.

Level 7

Level 7 is forced by microprogram and represents system reset routine, which is executed after it was started in level 3.

Interrupts

Channel End

Channel End indicates the completion of that part of an I/O operation that involves:

- Transfer of I/O data
- Transfer of sense information
- Transfer of control information between multiplexer channel and main storage and between multiplexer channel and control unit.

Channel end is accepted for all devices and is stored in the corresponding UCW (subchannel). The 'interrupt request' line then signals the waiting interrupts.

When the IPU is ready to process interrupts, level 0 routine selects one waiting interrupt and stores an interruption code (device address) into MSC-LS common register. Subsequently, the multiplexer channel stores a CSW, resets the interrupt condition, and releases the IPU for further processing.

This means, the subchannel appears with a pending interrupt to subsequent SIO instructions until its interrupt request has been accepted.

The instant (within an I/O operation) that channel end is generated depends upon the operation and the type of device. Operations that do not cause any data to be transferred can provide channel end condition already with presentation of the initial status.

When chaining takes place only the channel end of the last operation of the chain is made available to the program.

Device End

Device end indicates:

(a) The completion of an I/O operation at the I/O device.

(b) A manual change of the device from the "not ready" to the "ready" state.

Device end is stacked by the channel.

Device end status remains stacked in the control unit until the channel is free to handle them either by an interrupt or TIO.

When chaining is specified receipt of device end condition (and no unusual condition) causes the channel to initiate the next operation. Only the device end of the last operation of the chain is made available to the program.

Dependent upon I/O device type, device end condition is generated either simultaneously with the channel end condition or later

Chaining

Two types of chaining are possible
Data chaining (DC)
Command chaining (CC).
Chaining which is specified by the CCW flags, is detected and performed by microprogram.

When chaining is specified, the microprogram branches to a chaining routine. This chaining routine tests the chaining conditions and performs the following:

1. Fetching of new CCW
2. Testing for TIC
3. Testing for IDA
4. Loading of new CCW information into UCW.

Data chaining means that the command code of the previous CCW remains valid for the new CCW.

Command chaining means that the new CCW completely replaces the previous one.

Unusual or Exceptional Conditions

Unusual or exceptional conditions that occurred during execution of an I/O instruction are indicated in the status bytes. These unusual or exceptional conditions are handled by the operating system being used.

For arrangement of the status bytes in the CSW, see Page 2-020. For status bit definitions, see Page 5-010.

Status Bytes

Status bytes are presented at the beginning (*initial status*) and end (*ending status*) of an I/O operation.

Initial status indicates whether an I/O device is ready to execute a given command.

Ending status indicates whether an I/O operation was successful.

For arrangement of the status bytes in the CSW, see Page 2-020. For status bit definitions, see Page 5-010.

Sense Bytes

Simultaneously with the execution of an I/O operation sense bytes are generated and updated in the control unit. If a status byte indicates a unit check, these sense bytes provide additional, device specific, information about the cause of that malfunction.

Sense byte 0 is common for all I/O devices. The number and the content of all other sense bytes depend upon device type and the requirements of the device.

Sense bytes are fetched with a 'sense' command in the CCW of a 'SIO' instruction and are analyzed by the operating system being used.

For more information about sense bytes, refer to the respective control unit and/or I/O device documentation. A brief explanation of sense byte 0 is given on Page 5-010.

Indirect Data Addressing

If indirect data addressing is used the CCW contains an indirect data address (indicated by a flag bit; see CCW Format given on Page 2-020).

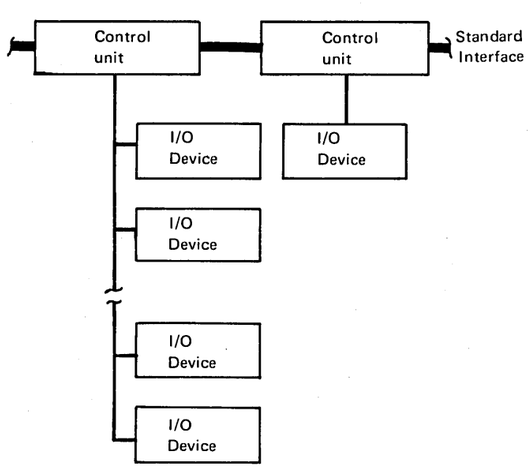
This IDA flag bit 'on' causes the MPX microprogram to fetch the actual data address from the IDA list in main storage (see microprogram flowchart on Page 3-030).

Subchannel Arrangement and Addressing

UCWs may be shared or non-shared. A shared UCW means that this UCW serves a group of I/O devices that are connected to one control unit, but only serviced one at a time. A non-shared UCW means that this UCW serves only one I/O device.

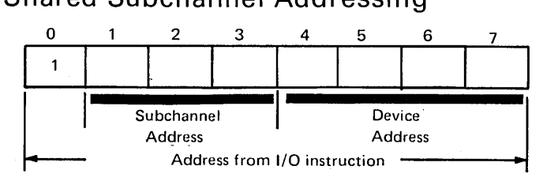
Out of the 32 UCWs, the first eight alternatively can operate as shared UCWs. Each control unit associated with a shared UCW may have up to 16 I/O devices attached.

When a subchannel is addressed by an I/O address, bit 0 of the address byte defines whether the subchannel is shared (bit 0 = 1) or non-shared (bit 0 = 0). Bit 0, therefore, is not part of the actual address.



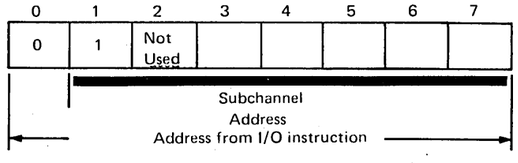
Shared *Non-shared*

Shared Subchannel Addressing



Device Addresses: 80 to FF (hex)
(see table on the right)

Non-Shared Subchannel Addressing



Device Addresses: 40 to 7F (hex)
(see table on the right)

Because shared subchannels 0 to 7 use the same UCW as the non-shared subchannels 0 to 7, addresses of shared subchannels must be chosen in such as way that they do not conflict with addresses of non-shared subchannels.

Device Address Assignments

Certain restrictions apply to address assignment. In any one row of the following table, only one of three address assignments can be chosen for devices which are to operate simultaneously. Taking the first row, for instance, if address 40 (hex) is assigned, addresses 60 (hex) and 80 through 8F (hex) should not be assigned.

Nonshared Subchannels (hexadecimal)		Shared Subchannels (hexadecimal)
40	60	80 to 8F
41	61	90 to 9F
42	62	A0 to AF
43	63	B0 to BF
44	64	C0 to CF
45	65	D0 to DF
46	66	E0 to EF
47	67	F0 to FF
48	68	
49	69	
4A	6A	
4B	6B	
4C	6C	
4D	6D	
4E	6E	
4F	6F	
50	70	
51	71	
52	72	
53	73	
54	74	
55	75	
56	76	
57	77	
58	78	
59	79	
5A	7A	
5B	7B	
5C	7C	
5D	7D	
5E	7E	
5F	7F	

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2 Principles of Operation

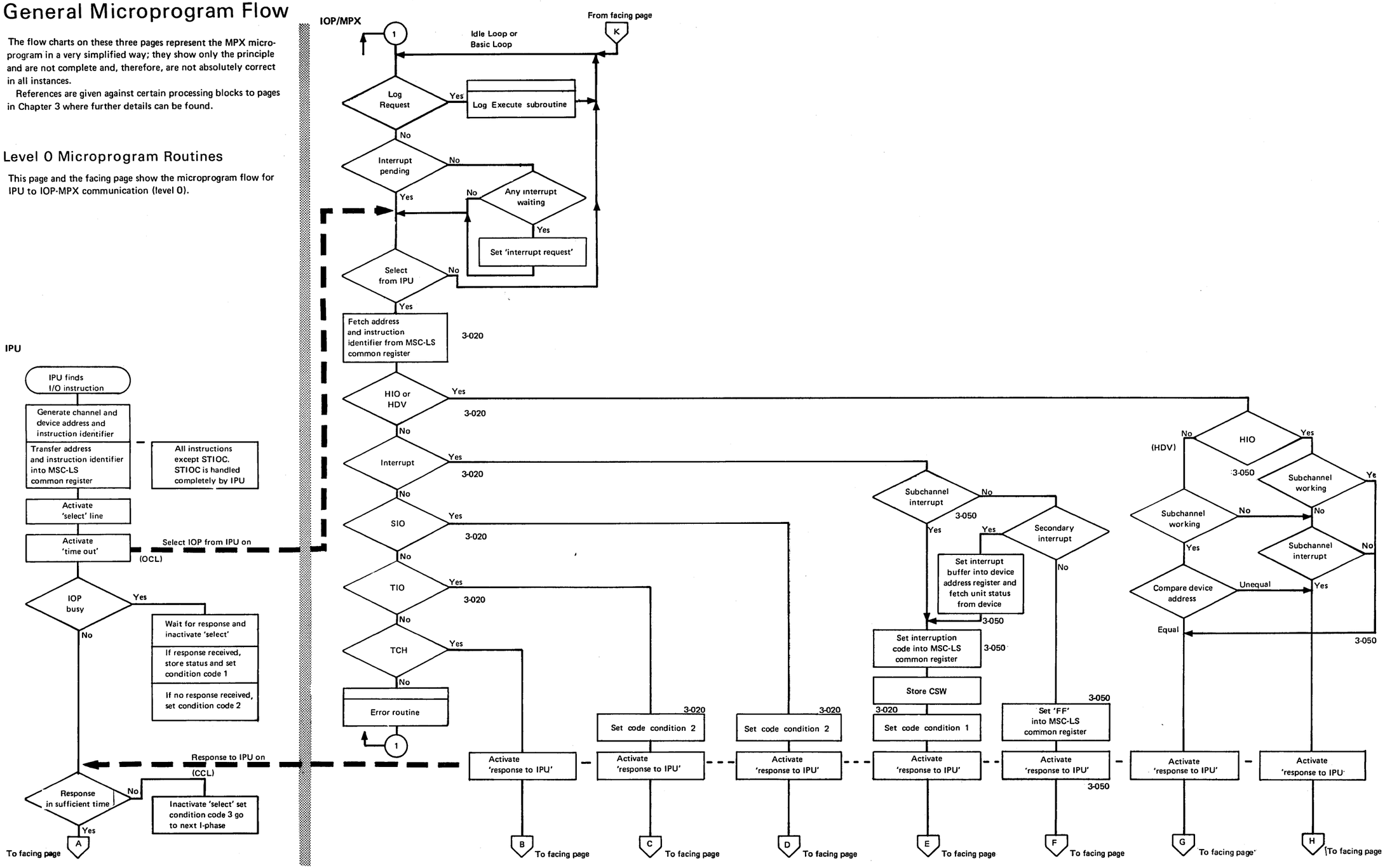
General Microprogram Flow

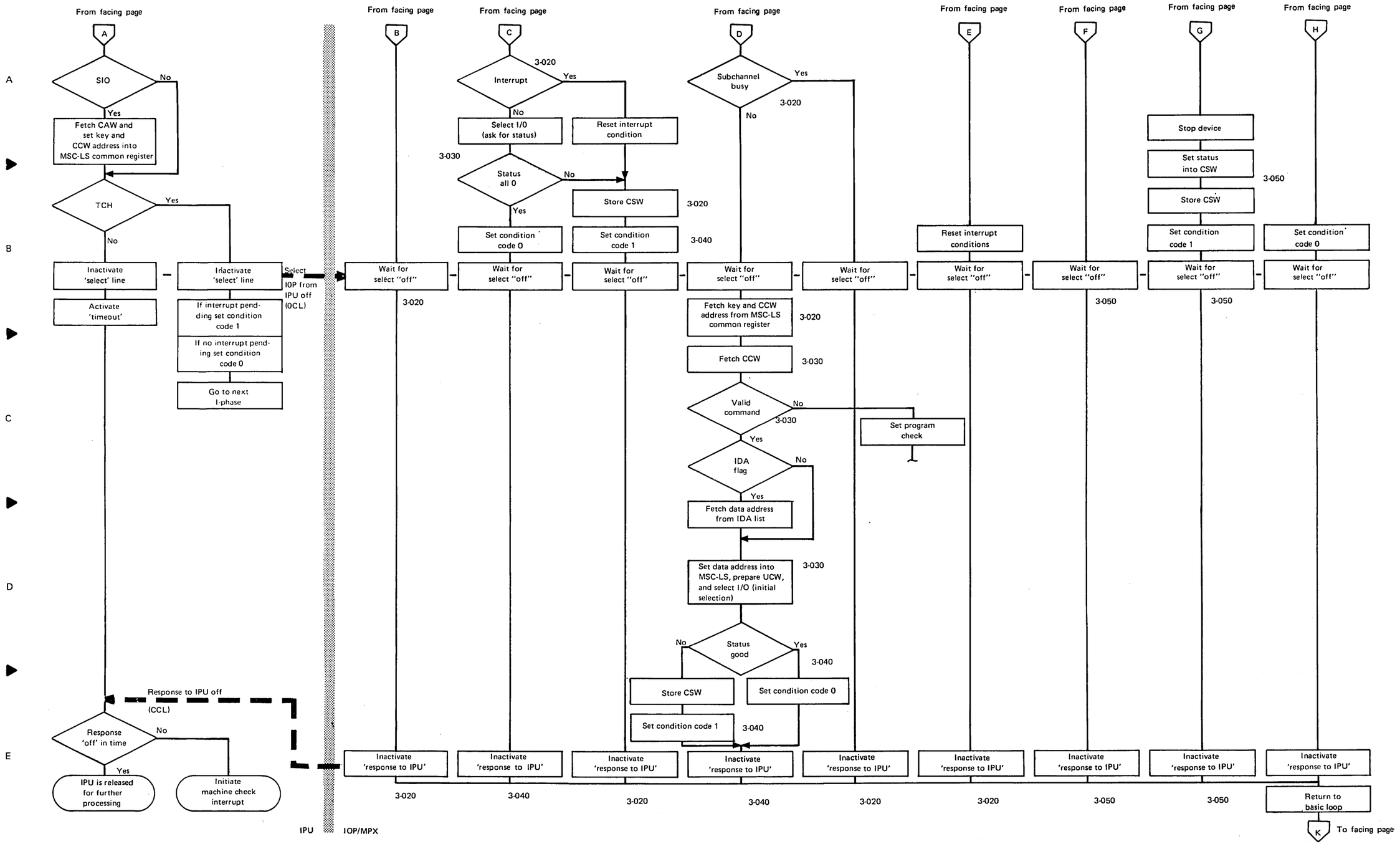
The flow charts on these three pages represent the MPX microprogram in a very simplified way; they show only the principle and are not complete and, therefore, are not absolutely correct in all instances.

References are given against certain processing blocks to pages in Chapter 3 where further details can be found.

Level 0 Microprogram Routines

This page and the facing page show the microprogram flow for IPU to IOP-MPX communication (level 0).

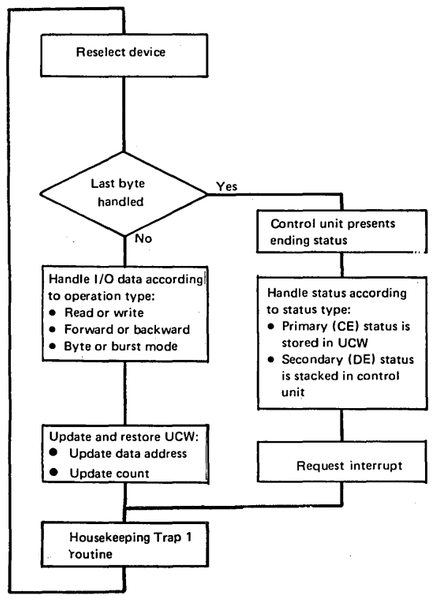



2
3
4
5
6
7
8
9
A
B
C
D
E
From facing page
A
SIO
No
Yes
Fetch CAW and set key and CCW address into MSC-LS common register
TCH
Yes
No
Inactivate 'select' line
Activate 'timeout'
Inactivate 'select' line
If interrupt pending set condition code 1
If no interrupt pending set condition code 0
Go to next I-phase
Select IOP from IPU off (OCL)
Response to IPU off (CCL)
Response 'off' in time
No
Yes
IPU is released for further processing
Initiate machine check interrupt
B
Wait for select "off"
3-020
C
Interrupt
3-020
Yes
No
Select I/O (ask for status)
Reset interrupt condition
3-030
Status all 0
No
Yes
Store CSW
3-020
Set condition code 0
Set condition code 1
3-040
Wait for select "off"
Wait for select "off"
D
Subchannel busy
Yes
3-020
No
Wait for select "off"
Fetch key and CCW address from MSC-LS common register
3-020
Fetch CCW
3-030
Valid command
No
3-030
Yes
IDA flag
No
Yes
Fetch data address from IDA list
Set data address into MSC-LS, prepare UCW, and select I/O (initial selection)
3-030
No
Status good
Yes
3-040
Store CSW
Set condition code 0
Set condition code 1
3-040
Wait for select "off"
Set program check
E
Reset interrupt conditions
Wait for select "off"
F
Wait for select "off"
3-050
G
Stop device
Set status into CSW
3-050
Store CSW
Set condition code 1
Wait for select "off"
3-050
H
Set condition code 0
Wait for select "off"
Inactivate 'response to IPU'
3-020
3-040
3-020
3-040
3-020
3-020
3-050
3-050
Return to basic loop
K
To facing page
IPU
IOP/MPX

General Microprogram Flow (continued)

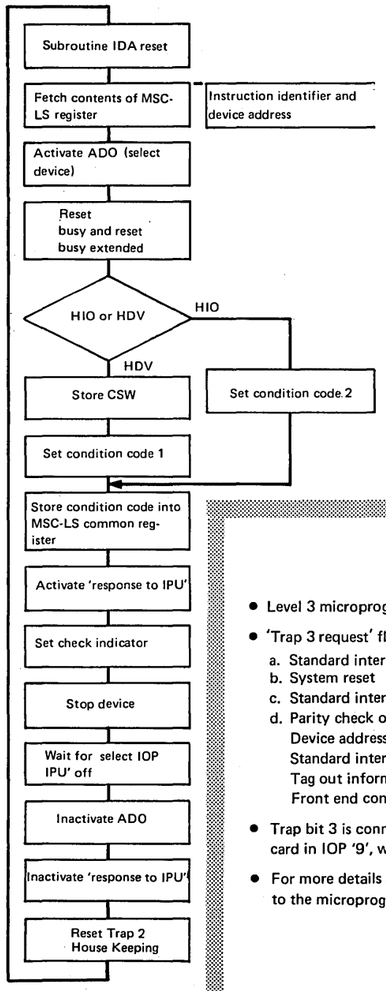
Level 1 Microprogram Routines

- Level 1 microprogram routines are for:
  "Data Handling" and
  "Status Handling"
- 'Trap 1 request' fliplatch is set with the standard interface "tag in" lines:
  Request in
  Operational in
- Trap bit 1 is connected to the trap register on the ALS/CSAR card in IOP '9', where it alters the link portion of index words.
- For more details about Level 1 microprogram routines, refer to the microprogram flowcharts on Pages 3-060 and 3-070.



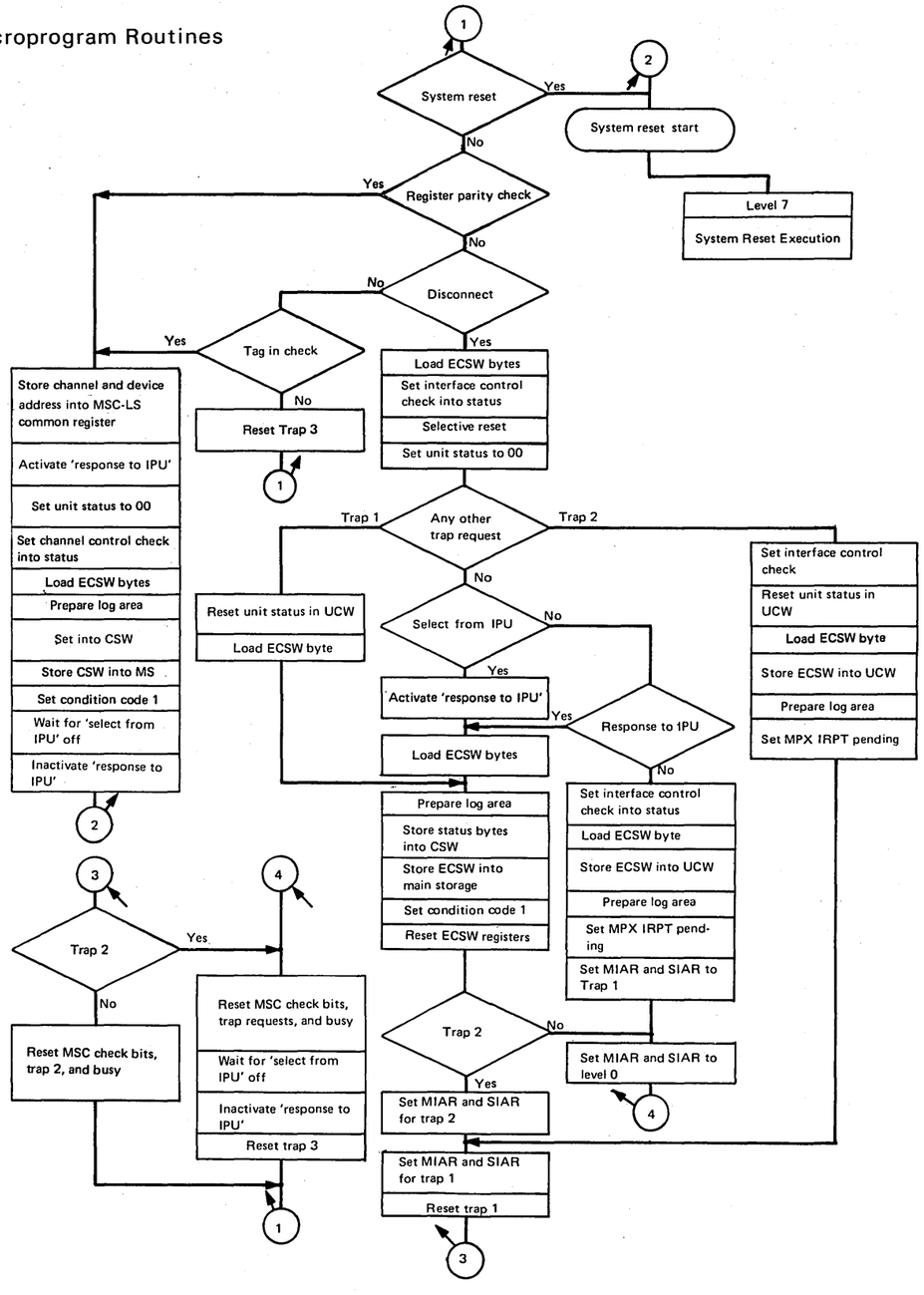
Level 2 Microprogram Routines

- Level 2 microprogram routines are for:
  "HIO" and "HDV" when the multiplexer channel is working in burst mode.
- 'Trap 2 request' fliplatch is set with burst mode and the 'HIO/HDV' line from IOP.
- Trap bit 2 is connected to the trap register on the ALS/CSAR card in IOP '9', where it alters the link portion of index words.
- For more details about level 2 microprogram routines, refer to the microprogram flowcharts on Page 3-080.



Level 3 Microprogram Routines

- Level 3 microprogram routines are for "Error Handling"
- 'Trap 3 request' fliplatch is set with one of the following:
  a. Standard interface tag in line 'disconnect in' active
  b. System reset
  c. Standard interface tag in check
  d. Parity check of the registers that hold
     Device address
     Standard interface
     Tag out information
     Front end control information
- Trap bit 3 is connected to the trap register on the ALS/CSAR card in IOP '9', where it alters the link portion of index words.
- For more details about level 3 microprogram routines, refer to the microprogram flowcharts on Page 5-030.



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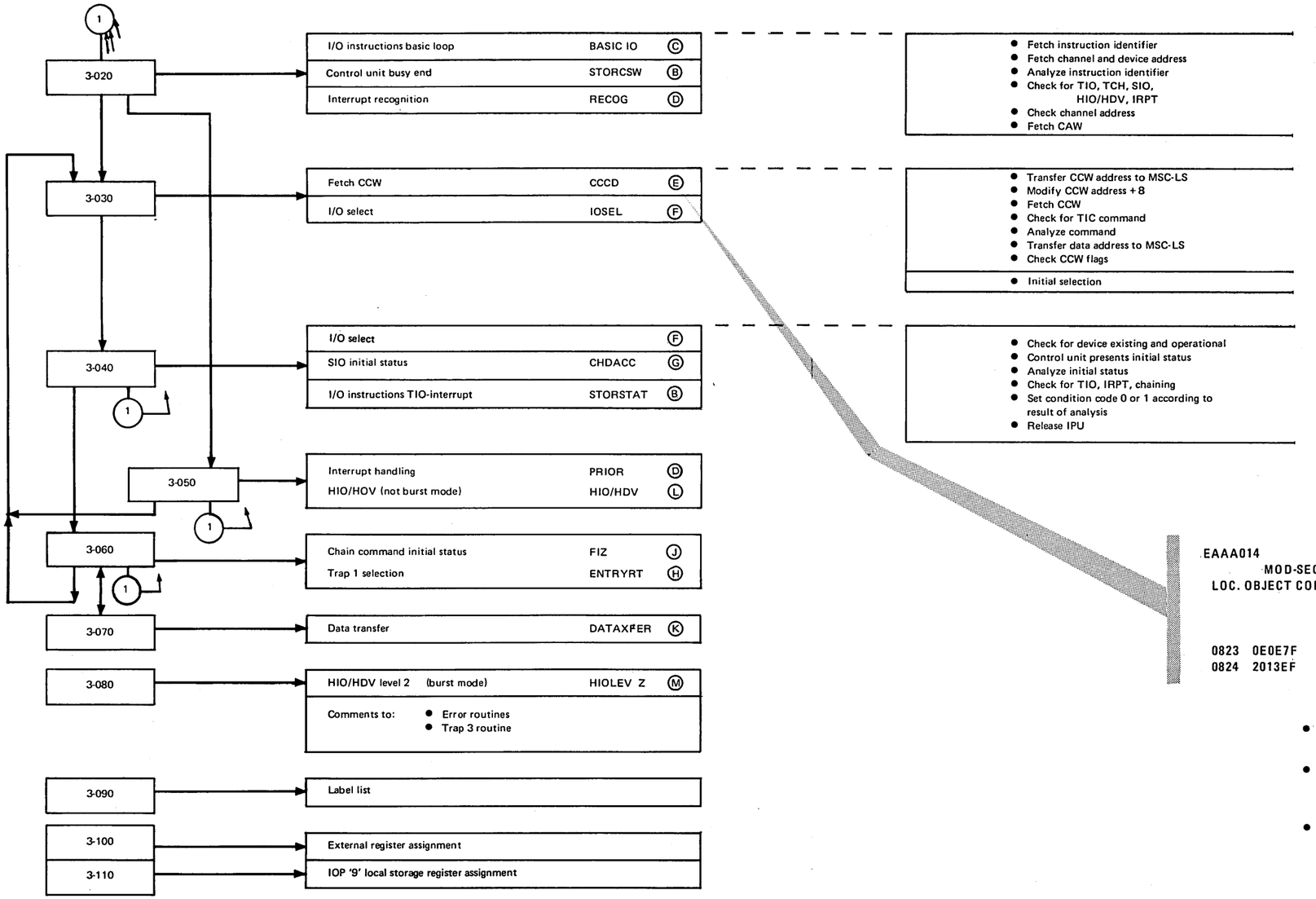
2 Principles of Operation

Chapter 3. Operational Details

Visual Index for MPX Microprogram

- Represents a summary of the MPX microprogram.
- Provides a guide to the microprogram flow.
- Relates various routines to pages within this chapter.
- Provides cross-references to the microprogram listing.



- The various routines of the MPX microprogram are documented in different sections of the microprogram listing.
- The circled letters after the labels (in the flowcharts on the following pages) point to these sections of the microprogram listing.
- These letters can be found in the microprogram listing header above the module sequence number.

Arrangement of MPX Microprogram Listing

This page represents a "table of contents" of the microprogram listing per section (or sheet) as defined by the circled letters.

Error Description
Declares and Equates of External and Local registers
System Reset
Start Routine

Ⓑ **I/O Instructions – TIO-Interrupt**
- CU busy end
- Interrupt
- Normal status
- CU busy

Ⓒ **I/O Instructions – Basic Loop**

Ⓓ **Interrupt Handling**
- Interrupt priorities
- Interrupt recognition

Ⓔ **Fetch CCW**
- CCW address to MSC-LS 1
- CCW update
- Store CCW address +8
- Save CCW address +8
- CCW update
- CCW address to MSC-LS 1
- Execute TIC

Indirect Data Addressing

Ⓕ **I/O Select**
- Control unit busy
- SIO
- Set up CSW address
- Store 2 status bytes
- Reset UCW
- Withdraw stacked status

Ⓖ **SIO Initial Status**
- Execute command chaining
- Indicate command chaining
- I/O operation ANDed, no chaining
- Set up CCW address
- Store 2 status bytes
- Condition code 1
- Reset UCW
- Command accepted

Ⓗ **TRAP I/O Selection**

Ⓙ **CC Initial Status**
- Indicate chaining
- Execute chaining
- Command accepted, I/O started

Ⓚ **Data Transfer**

Ⓜ **HIO/HDV – Level 2**
- Set up CSW address

Prepare New Page for Indirect Data Addressing
- Subroutine store condition code 0
- Subroutine prepare for Trap 1 when 'request in'

Ⓛ **HIO/HDV – Not Burst**
- Set up CSW address
- Reset Time Out counter

Common Error Routines for SIO
Common Error Routines for CC
Common Error Routines for TIO
Subroutine Time Out
Common Subroutines
- Subroutine information for SVP
- Subroutine generate UCW address
- Set up CSW address +4 and store 2 status bytes
- Subroutine prepare system reset from Trap 3

Subroutine Address and Store CSW
Subroutine NOP
Subroutine Address and Store ECSW
Subroutine Store Condition Code 1
- Entry of routine IPU end
- Entry of routine channel handling 1 +2

Subroutine Channel Handling 3
Subroutine Interface Disconnect with Selective Reset
Subroutine Reset Prefetched IDA Word
Subroutine Prepare and Store ECSW into Data Store
Subroutine Prepare Log Area
Trap 3 Handling
Tag In Check
System Reset from Trap 3
External Register Parity Check
Disconnect In
MPX System Reset
Subroutine Log Execute for Level 0, 1, 2, and 3
Error Routines for Sections (or Sheets) B, C, D, E, F, G, H, J, K, M
UCW Area Definition
Cross References

This is an alphabetical listing of all labels used in that microprogram listing. In connection with all labels:
- their storage location and statement number
- all statement numbers that use the label as symbolic "branch to" address

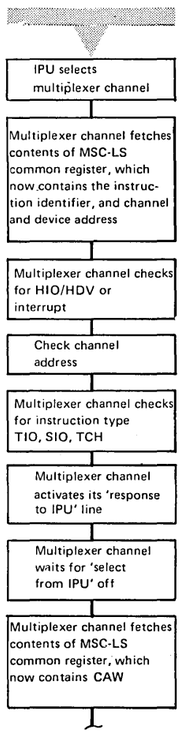
are shown.

MPX Microprogram Flowcharts

This page and the following pages up to page 3-080 show the MPX microprogram in a simplified way. Because these flowcharts are not as detailed as the microprogram listings the flowcharts are not correct in all details. If detailed information is needed refer to the microprogram listings.

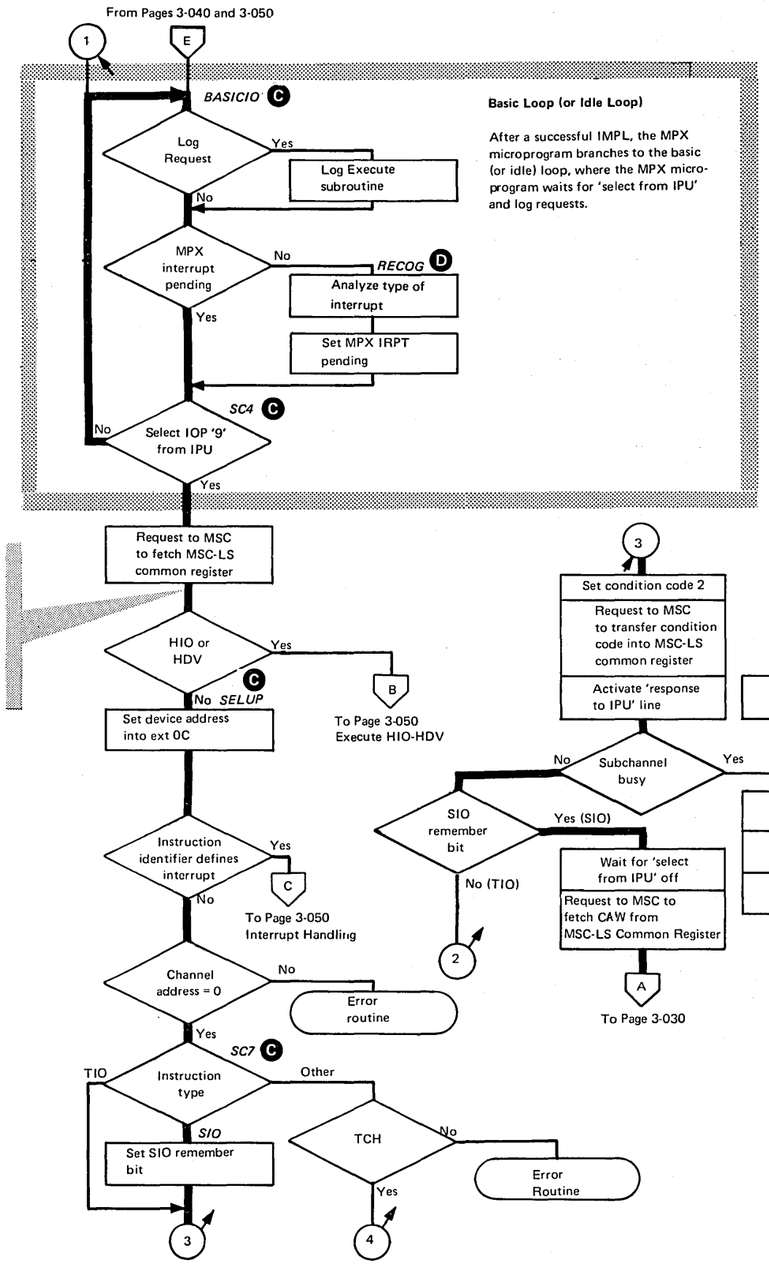
The various routines covered on this page are:
Control unit busy end (B)
I/O instructions basic loop (C)
Interrupt recognition (D)

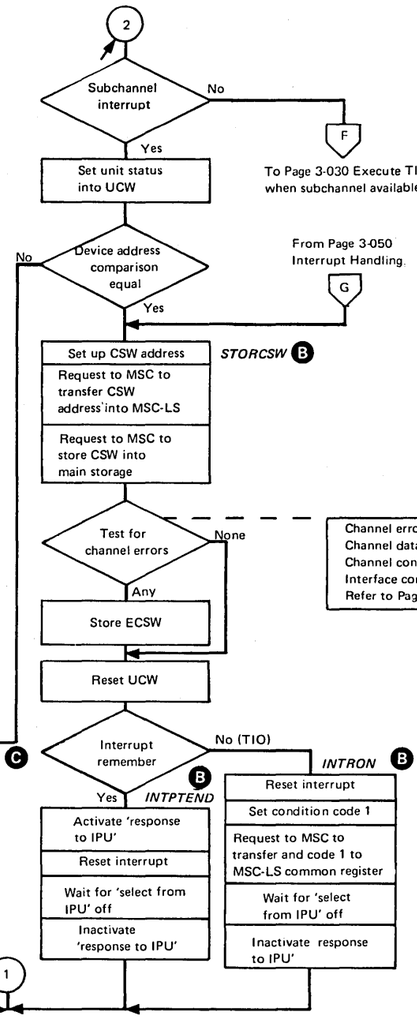
This flowchart is a simplification of the main flowcharts and represents the steps for an 'SIO' instruction.



The thick line through these flowcharts shows the flow for an SIO instruction.

For all other instructions and operations, follow the thin lines.

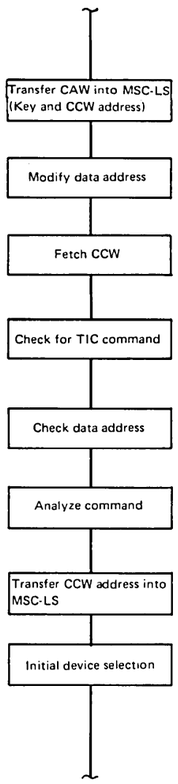


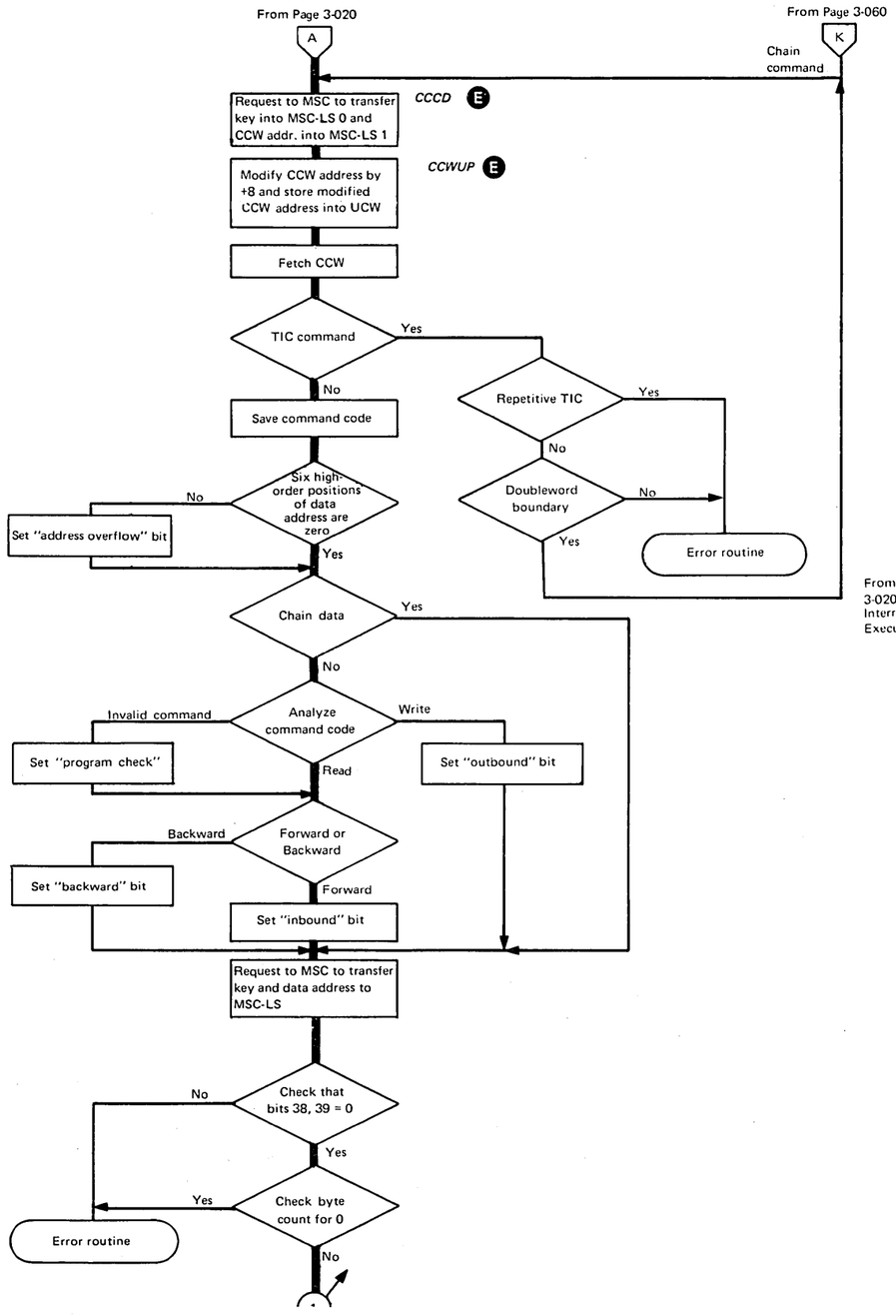


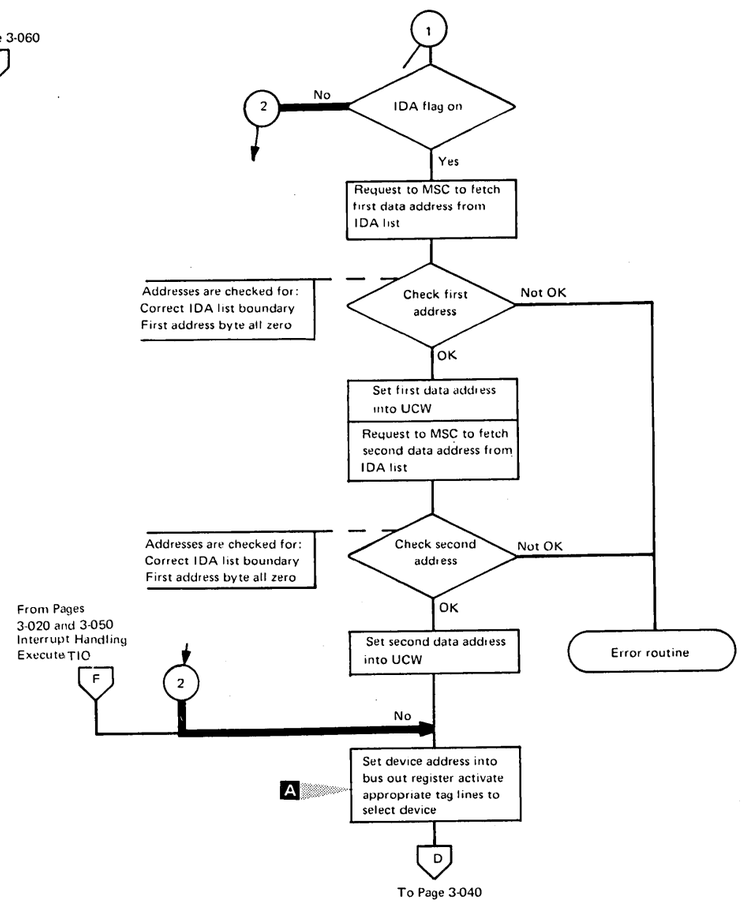
The subroutines covered on this page are:

Fetch CCW (E)

I/O Select (F)





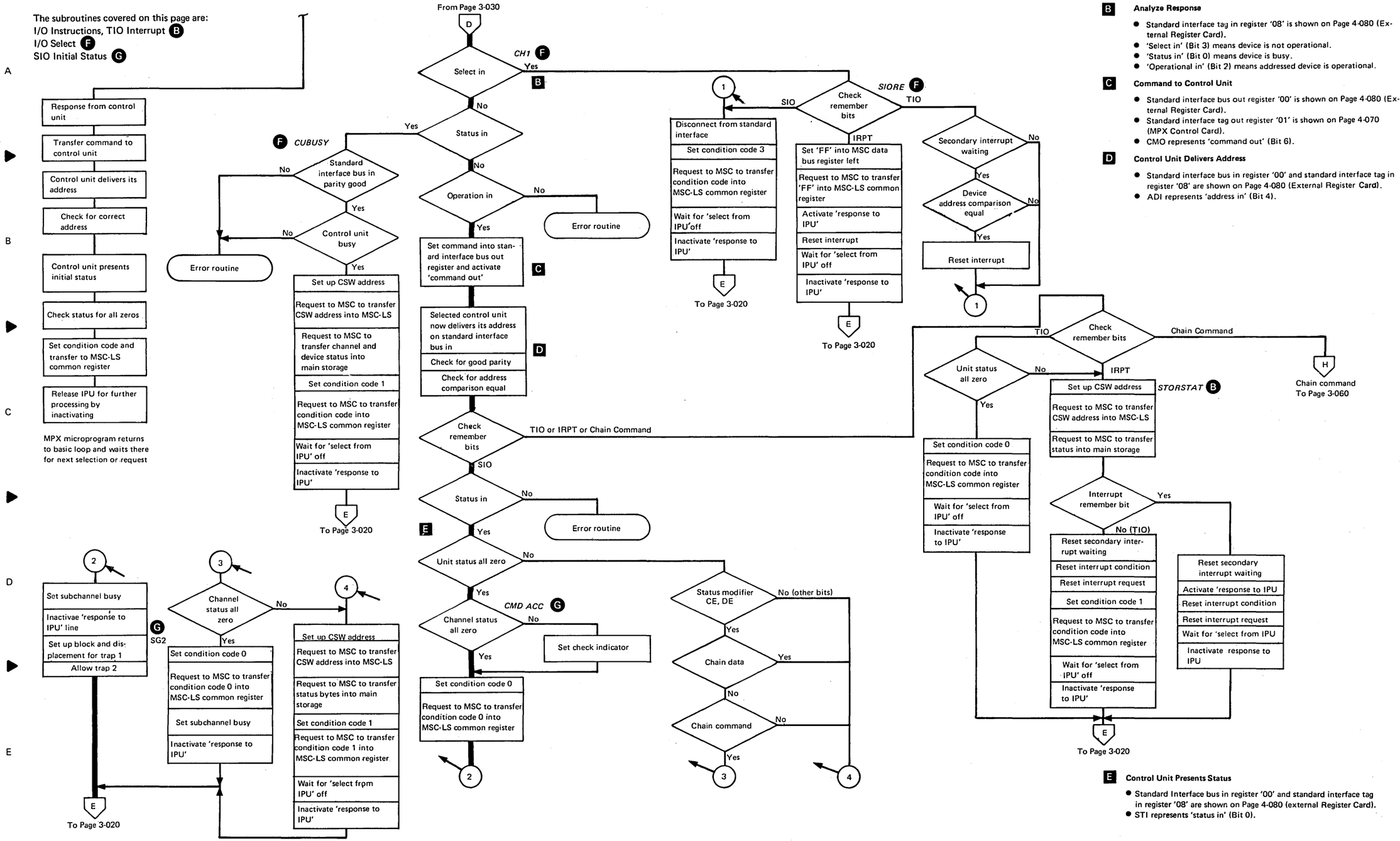


A Address device

- Standard interface bus out register '04' is shown on Page 4-080 external register card.
- Standard interface tag out register '01' is shown on Page 4-070 (MPX control card)
- The bit pattern that is set into the tag out register causes activation of the tag out lines.
  ADO – Address Out (Bit 1)
  HO – Hold Out (Bit 2)
  SLO – Select out (Bit 3)
- Interface sequence, showing communication between multiplexer channel and control unit for initial selection, is shown on Page 4-050.
- Data path for write operations is shown on Pages 2-030 and 2-035.
- Data path for read operations is shown on Pages 2-040 and 2-045.

MPX Microprogram Flowcharts (continued)

The subroutines covered on this page are:
I/O Instructions, TIO Interrupt (B)
I/O Select (F)
SIO Initial Status (G)



B Analyze Response

- Standard interface tag in register '08' is shown on Page 4-080 (External Register Card).
- 'Select in' (Bit 3) means device is not operational.
- 'Status in' (Bit 0) means device is busy.
- 'Operational in' (Bit 2) means addressed device is operational.

C Command to Control Unit

- Standard interface bus out register '00' is shown on Page 4-080 (External Register Card).
- Standard interface tag out register '01' is shown on Page 4-070 (MPX Control Card).
- CMO represents 'command out' (Bit 6).

D Control Unit Delivers Address

- Standard interface bus in register '00' and standard interface tag in register '08' are shown on Page 4-080 (External Register Card).
- ADI represents 'address in' (Bit 4).

E Control Unit Presents Status

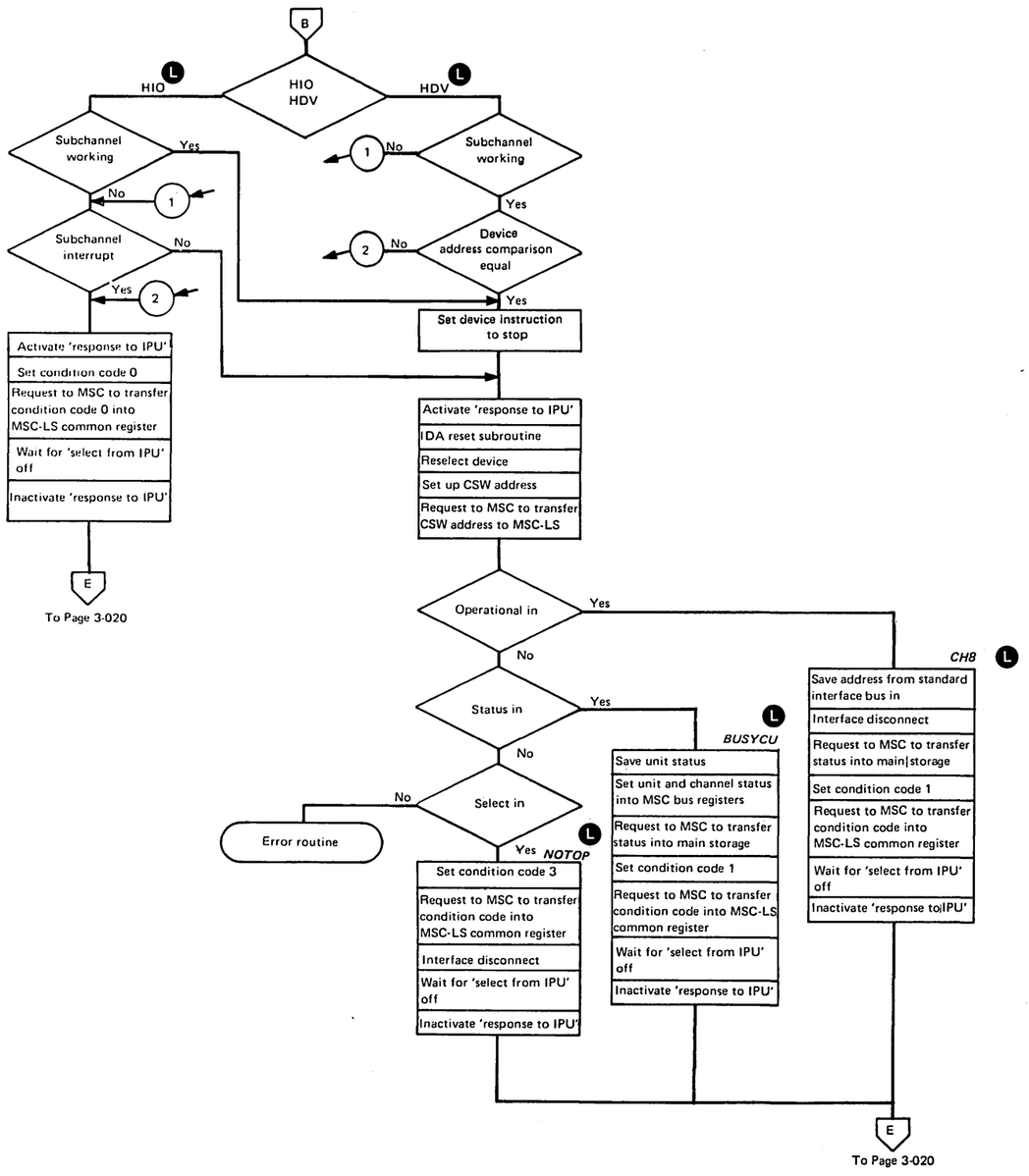
- Standard Interface bus in register '00' and standard interface tag in register '08' are shown on Page 4-080 (external Register Card).
- STI represents 'status in' (Bit 0).

The subroutines covered on this page are:

Interrupt Handling (D)
HIO/HDV (MPX not in burst mode) (L)

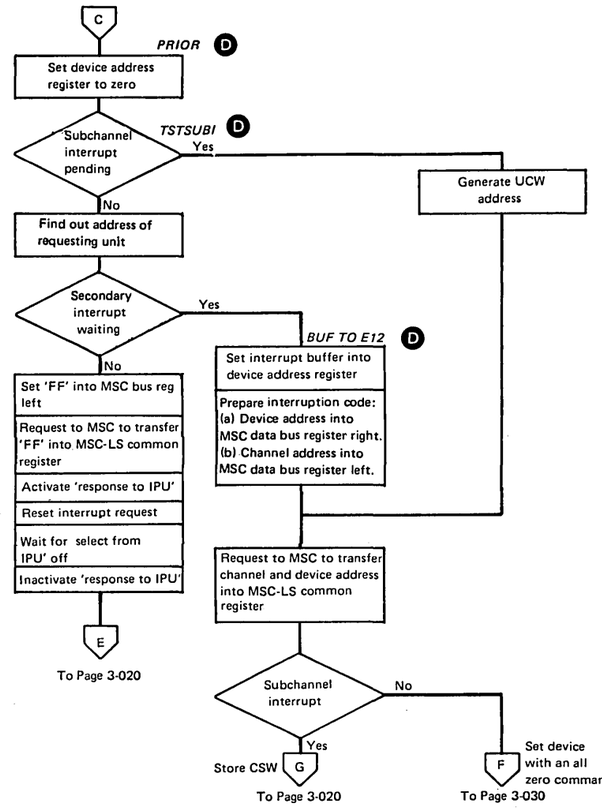
This routine is the continuation from the basic loop after analyzing the instruction identifier, the result being either and HIO or an HDV.

From Page 3-020



This routine is the continuation from the basic loop after analyzing the instruction identifier, the result being an interrupt.

From Page 3-020

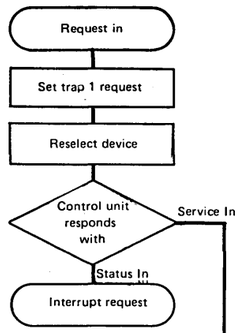


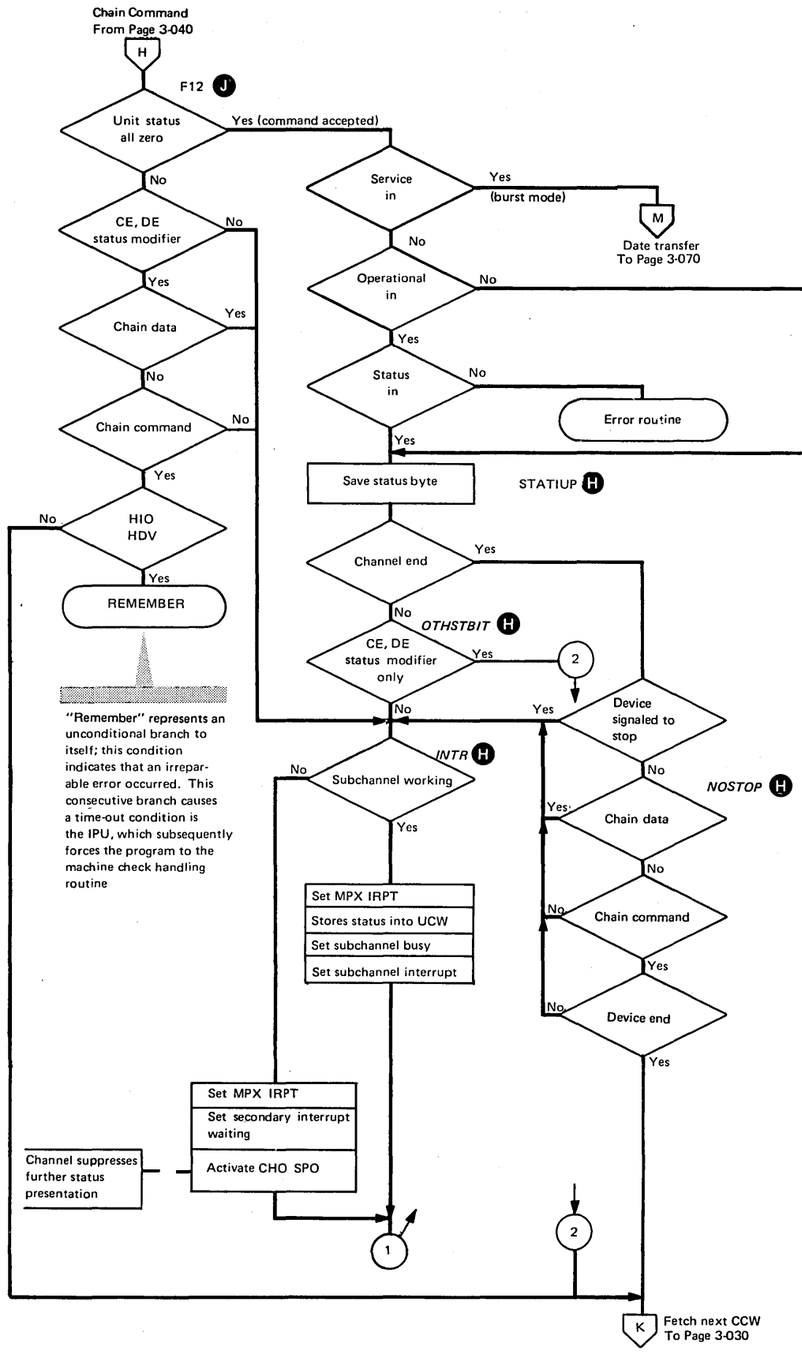
MPX Microprogram Flowcharts (continued)

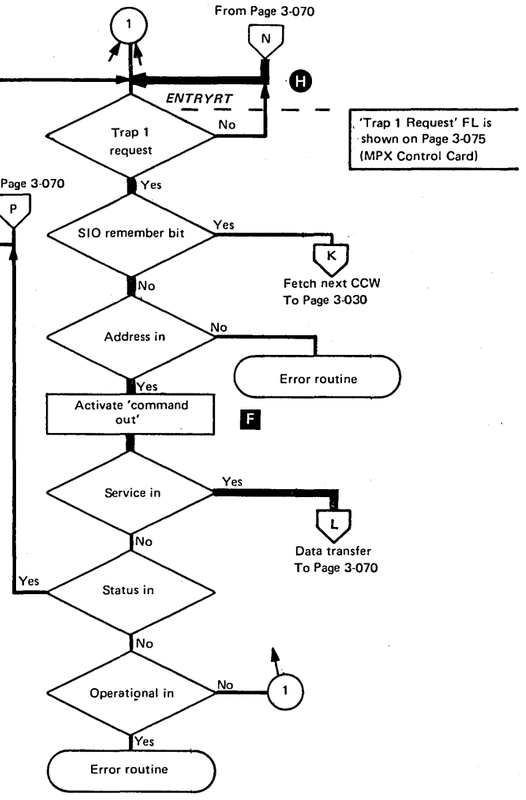
The subroutines covered on this page are:

Trap 1 Selection (H)

Chain Command Initial Status (J)



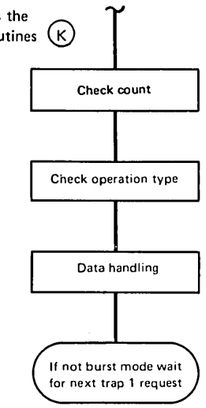


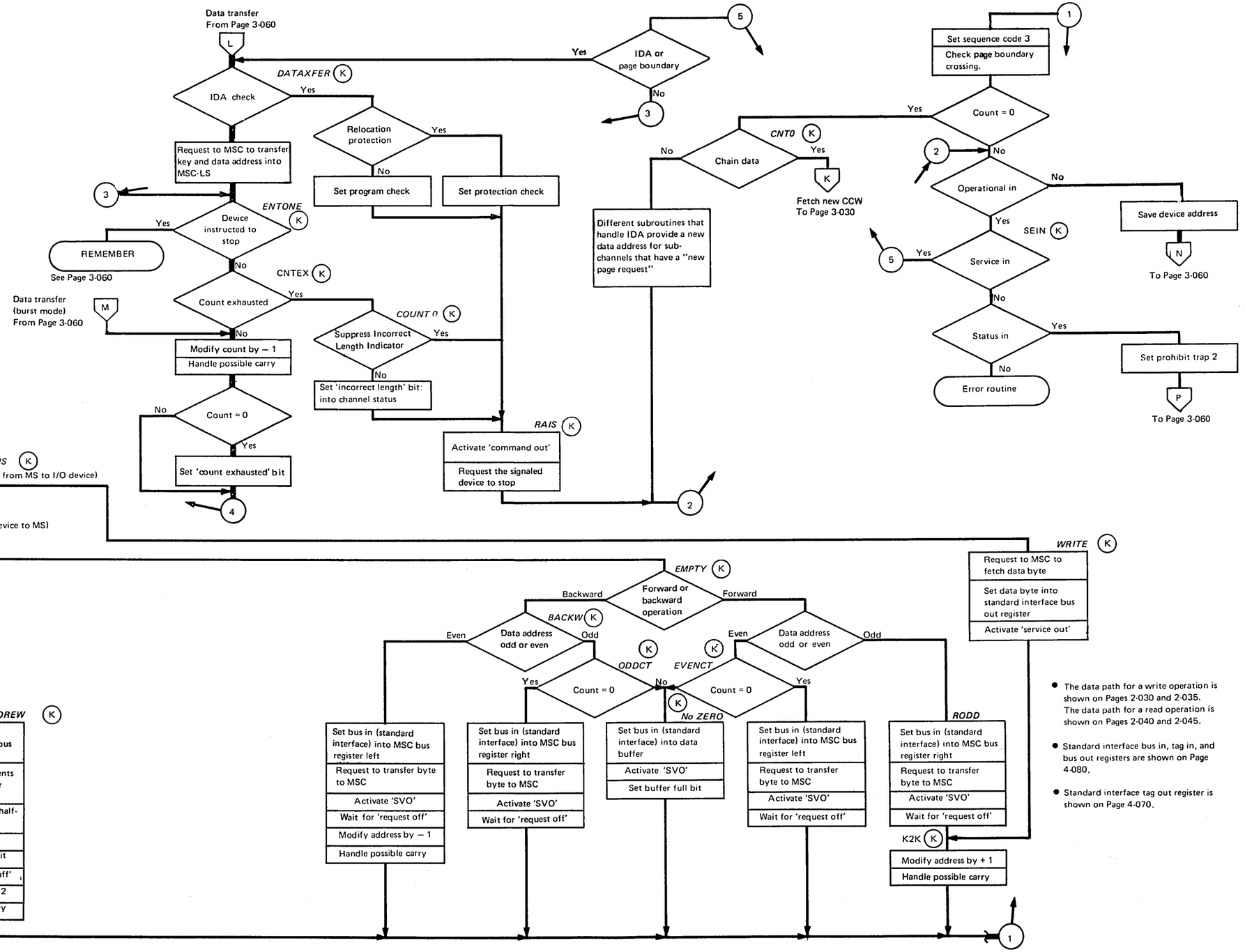


F **Reselection**

- Sequence of signals on standard interface for reselection is shown on Page 4-050.
- Standard interface bus in register '00', tag in register '08', and bus out register '04' are shown on Page 4-080.
- Standard interface tag out register '01' is shown on Page 4-070.

This page shows the data transfer routines on level 1. (K)

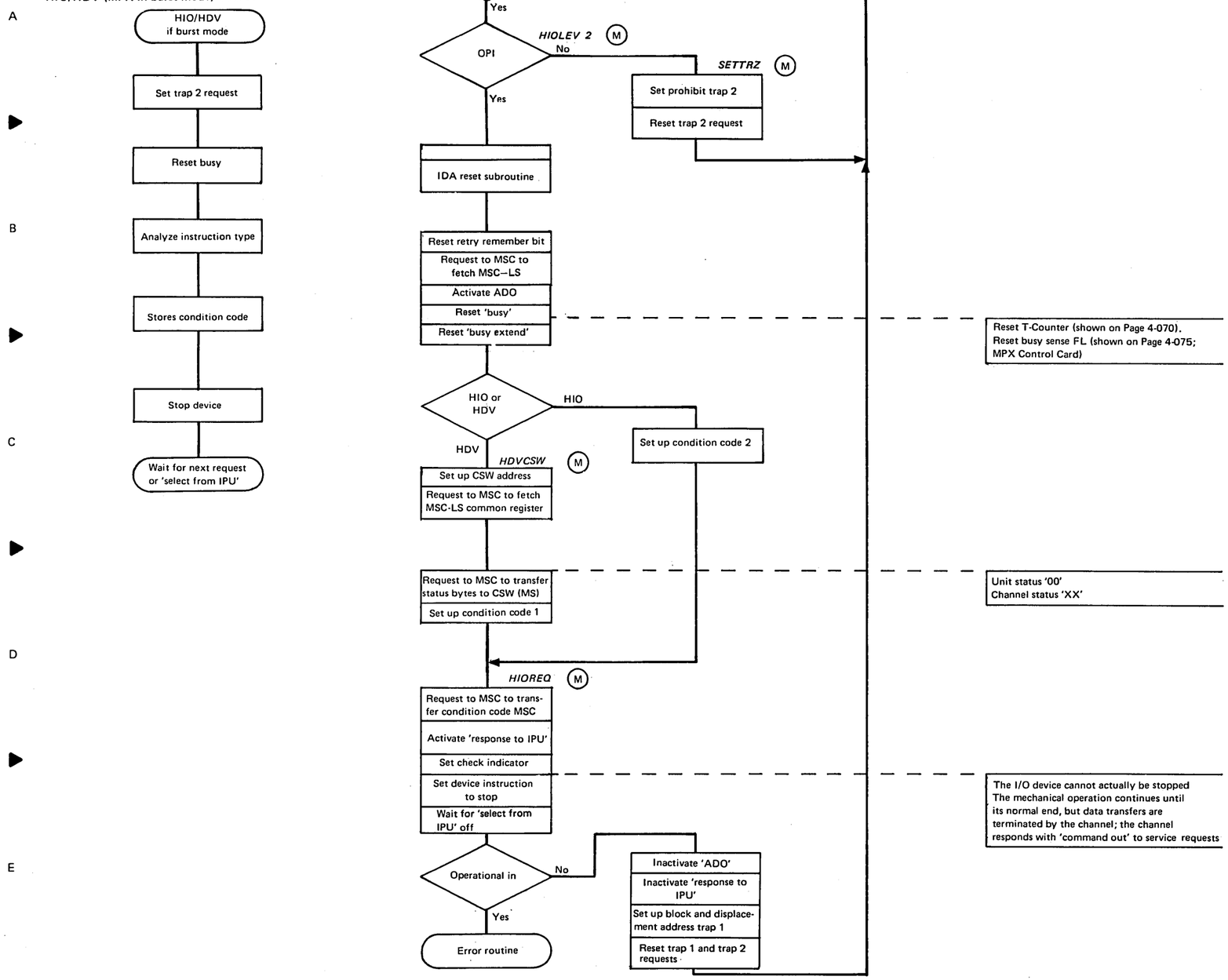




- The data path for a write operation is shown on Pages 2-030 and 2-035. The data path for a read operation is shown on Pages 2-040 and 2-045.
- Standard interface bus in, tag in, and bus out registers are shown on Page 4-080.
- Standard interface tag out register is shown on Page 4-070.

MPX Microprogram Flowcharts (continued)

This page covers the following subroutine:
HIO/HDV (MPX in burst mode) level 2.



Error Routine

Because the flowcharts on Pages 3-020 to 3-080 shows the MPX microprogram in simplified form (not all instructions in the microprogram listings are covered) many checks are not shown.

To prevent an incomplete and perhaps incorrect reproduction no information about the error routines is given in this chapter.

The error routine principle and the use of the error numbers are briefly explained on Page 6-020.

Trap 3 Routine

Trap 3 routine is a stand-alone microprogram routine which is documented in detail on Page 5-030.

MPX Microprogram Label List

B

BACKW	3-070	D6
BASIC IO	3-020	A5
BUF TO E 12	3-050	C8
BUSYCU	3-050	D5

C

CCCD	3-030	A5
CCW UP	3-030	A5
CH 1	3-040	A5
CH 8	3-050	C6
CMDACC	3-040	D4
CNTEX	3-070	B4
CNT 0	3-070	A7
COUNT 0	3-070	B5
CU BUSY	3-040	A3

D

DATAXFER	3-070	A4

E

EMPTY	3-070	D7
ENTONE	3-070	B4
ENTRYRT	3-060	B8
EVENCT	3-070	D7

F

FOREW	3-070	D3
F 12	3-060	A4

H

HDV	3-050	A4
HIO	3-050	A3
HIO LEV 2	3-080	A4
HDV CSW	3-080	C4
HIO RER	3-080	D4

I

INTRON	3-020	E8
IOSEL	3-030	D7
INTR	3-060	C5
INTRTEND	3-020	E7

K

K2K	3-070	E8

N

NO TOP	3-050	D4
NO STOP	3-060	C6

O

ODD CT	3-070	D6
OTH ST BIT	3-060	C5

P

PRIOR	3-050	A8

R

RAIS	3-070	C6
RECOG	3-020	B6
RECTRANS	3-070	C4
REMEMBER	3-060	C3
RODD	3-070	D8

S

SC 4	3-020	B5
SC 7	3-020	D5
SCH BUSY	3-020	C7
SE IN	3-070	B8
SEL UP	3-020	C5
SETTR 2	3-080	A5
SG 2	3-040	D2
SIO RE	3-040	A7
STATI UP	3-060	B5
STORCSW	3-020	C7
STOR STAT	3-040	C8
SW 1	5-030	B3
SW 3	5-030	C3
SW 5	5-030	C3
SW 7	5-030	E2
SW 8	5-030	E4
SW 10	5-030	B5
SW 14	5-030	C5
SW 15	5-030	D4
SW 16	5-030	C6
SW 17	5-030	C7
SW 18	5-030	D5
SW 20	5-030	A8
SW 21	5-030	B9
SW 22	5-030	B8
SW 23	5-030	B8
SW 24	5-030	B8
SW 25	5-030	D8
SW 28	5-030	A8
SW 29	5-030	A8

T

TRAP 3	5-030	A5
TSTSUBI	3-050	B8

W

WRITE	3-070	C9

External Register Assignments

- This chart shows the meaning of each single bit in the different registers.
- UCW buffer byte locations are to be considered as registers.
- Register addresses are shown in hexadecimal values.

Register Number	S = sense C = control	Registers Name	Bit Position 0	1	2	3	4	5	6	7	Remarks
00	S	Standard interface bus in	0	1	2	3	4	5	6	7	See page 4-080
01	S C	Standard interface bus out	OPO	ADO	HO	SLO	SPO	Allow Reg Check	CMO	SVO	See page 4-070
02	*	UCW Flags & Op-Control	CD	CC	SLI	Skip	PCI	Check indicator	Count zero	CC denoted	
03	*	UCW Op-Control	CC indicated	Read backward	Inbound	Sequence code 3 valid,	Subchannel busy	Device instruction to stop	Page boundary crossing	Subch interrupt pending	
04	S C	Standard interface bus out	0	1	2	3	4	5	6	7	See page 4-080
05		Not used	–	–	–	–	–	–	–	–	
06	*	UCW count left	← Number of bytes to be transferred →								High-order positions
07	*	UCW count right	← Number of bytes to be transferred →								Low-order positions
08	S	Standard Interface tag in	STI	SVI	OPI	SLI	ADI	RQI	Disconnect in	Not tag in check	See page 4-080
A 09	C	Resets	Trap 1	'Busy sense' FL	Busy (T-counter)	Interrupt request	Trap 3	Trap 2	Power on	'MSC check' FF	Generates check reset; see page 4-070
B 0A	*	UCW byte buffer	← See note B below →								
0B	*	UCW keys	0	1	2	3	Data buffer full	Actual data address	Actual data address	Actual data address	High portion
0C	S C	Device address	0	1	2	3	4	5	6	7	See page 4-080
0D	S	Sense register B	Reg '01' pty check	Reg '0C' pty check	Reg '14' pty check	Response to IPU	Select from IPU	HIO/HDV	–	No interrupt request sense	See page 4-070
0E	*	UCW actual data address	0	1	2	3	4	5	6	7	Medium portion
0F	*	UCW actual data address	0	1	2	3	4	5	6	7	Low portion
C 10	S	Sense register A	Bus in pty check	Busy (burst mode)	Busy extension	–	(Not) trap 1 register	Trap 2 register	Trap 3 register	–	See page 4-080
11		Not used	–	–	–	–	–	–	–	–	
12	*	UCW channel status	PCI	Incorrect length	Program check	Protection check	Channel data check	Channel control check	Interface control check	Chaining check	
13	*	UCW op-control	Paging active	Not paging ready	Prepare new page	Not program check **	Prog. or Prot. check **	Next data address	Next data address	Next data address	High portion **Relocation
14	S C	Control register	(Not) force trap 1	Hi level control reg	Invalid parity	Allow trap 2	–	–	–	–	See page 4-080
15		Not used	–	–	–	–	–	–	–	–	
16	*	UCW next data address	0	1	2	3	4	5	6	7	Medium portion
17	*	UCW next data address	0	1	2	3	4	5	6	7	Low portion
18	S C	MSC tag register	MSC – main storage	Byte left	Register 1	Use common register	Increment	Decrement	Halfword	From MSC	MSC Data and Control Card (IOP)
19	S C	IPU tag register	–	Response to IPU	MPX secondary interrupt	–	–	–	–	Interrupt request	MSC Data and Control Card (IOP)
1A	S	Sence register (Read)	Accumulator data check	Pty check	System reset trap 3	–	Page boundary crossing	Request to MSC	MSC check bit 1	MSC check bit 2	MSC Data and Control Card (IOP)
D 1B		Reset	← This address is used to reset 'accumulated data check' FL and register 1A →								MSC Data and Control Card (IOP)
1C	S C	MSC-bus left no register	0	1	2	3	4	5	6	7	MSC Data and Control Card (IOP)
1D	S C	MSC-bus left register	0	1	2	3	4	5	6	7	MSC Data and Control Card (IOP)
1E	S C	MSC-bus right no register	0	1	2	3	4	5	6	7	MSC Data and Control Card (IOP)
1F	S C	MSC-bus right register	0	1	2	3	4	5	6	7	MSC Data and Control Card (IOP)

A Register '09': This is not actually a register; with this address active, the bit pattern from IOP D-register is directly used as a reset condition.

B Register '0A': This byte either completes the halfword that is to be transferred to the MSC or is one byte of the halfword that was received from the MSC.

C Register '10' bit 2 (busy extensions): Represents the 'busy' FF so that the busy condition can be stored after a burst mode operation.

D Register '1B': This is not actually a register; with this address active, the 'accumulated data check' FL on the MSC Data and Control Card is reset.

* All registers marked with an asterisk represent the portion of the UCW, that is stored in the UCW buffer of the multiplexer channel.

IOP '9' Local Storage Register Assignments

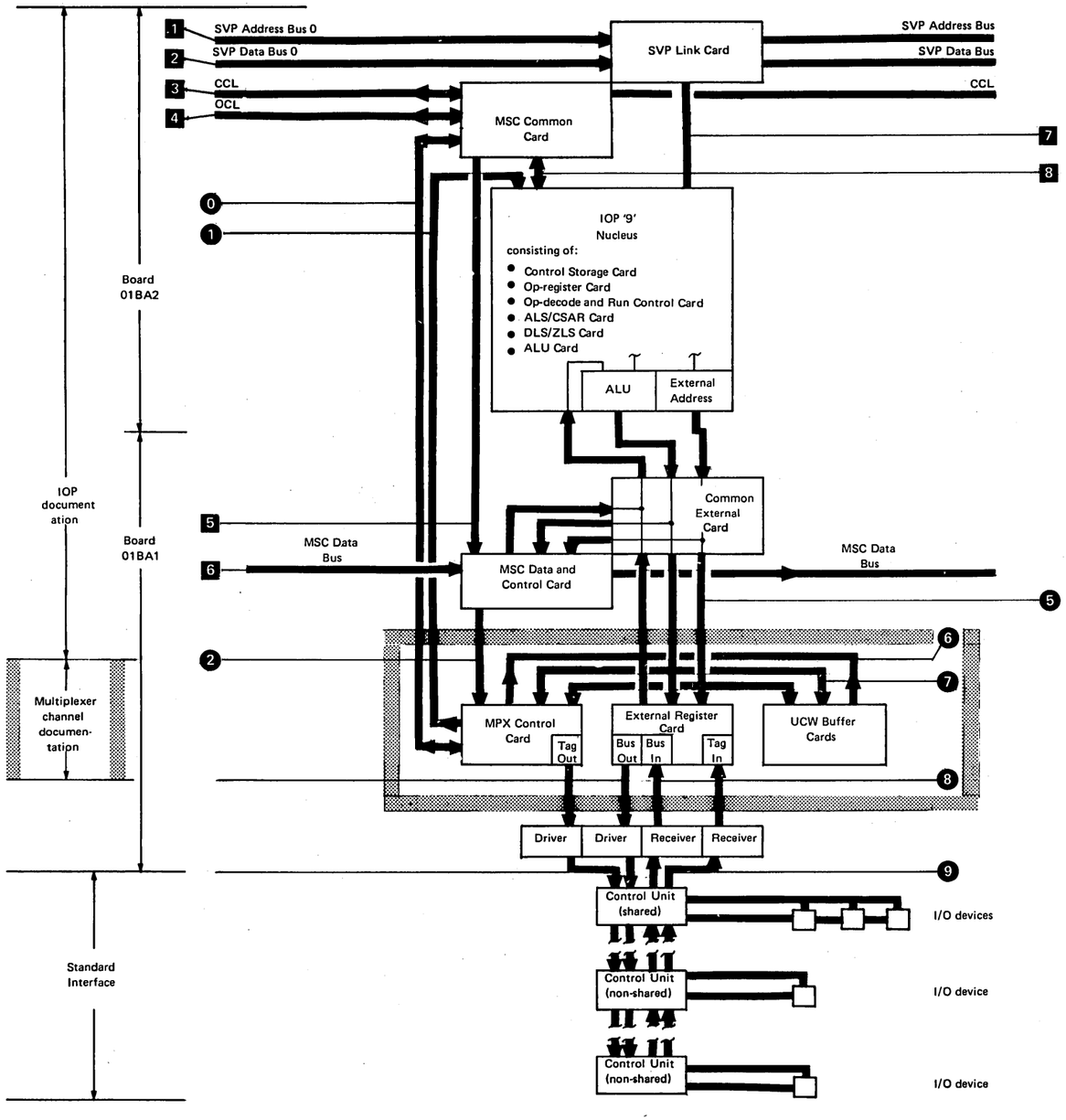
- This chart shows the usage of IOP '9' local storage registers.
- Register addresses are shown in hexadecimal values.

Register Number		Label of Register	0	1	– 2	3	4	5	6	7	Remarks
00		UCWADDR	Address of UCW and ECSW in control storage								
01		LOGDATA D	Address of log area in control storage								
02		CCWADDHI	Next CCW address high								
03		SAVEREG	Save register								
04		CCWSTORE									
05		IDAWHI	IDA word high order byte								
06		IDAWMI	IDA word middle-order byte								
07		IDAWLO	IDA word low-order byte								
08		UNITSTAT	Attention	Status modifier	Control unit end	Busy	Channel end	Device end	Unit check	Unit exception	Unit status for CSW
09		SVEDEVAD	Save area for device address								
0A		TOCNT 1	Timeout counter (high portion)								
0B		TOCNT 2	Timeout counter (middle portion)								
0C		TOCNT 3	Timeout counter (low portion)								
0D		PROFREG	Used for different purposes during execution of microprogram								
0E		TESTREG	TIC	Status modifier	Chain data	–	SIO	TIO interrupt	Interrupt	Timeout exhausted	Remember bits
0F		ZEROREG	Used for "add zero with carry" operation								
10		IDABRA	Branch address for relocation								
11		IDAUCW	UCW address for relocation								
12		IDAROUT	Address of IDA routine								
13		WORKREG 3	Work register								
14		ECSWBYT 0	Used for storing ECSW byte 0								
15		ECSWBYT 1	Used for storing ECSW byte 1								
16		ECSWBYT 2	Used for storing ECSW byte 2								
17		ECSWBYT 3	Used for storing ECSW byte 3								
18		ERRORNR	Error number for log.								
19		IRPTBUFF	Used as interrupt buffer								
1A		WORKREG 1	Work register								
1B		WORKREG 2	Work register								
1C		LOGCOUNT	Log counter								
1D		CONTROLS	MSC check	Error ckeck	Selective reset	–	Log request	Log execute	Channel working	Store ECSW	Remember bits
1E		CHANSTAT	PCI	Incorrect length	Program check	Protection check	Channel data check	Channel control check	Interface control check	Chaining check	Channel status for CSW
1F		MINUS 1	Used for "subtract one" operation								
20		IDADEV	Device address for relocation								
21		IDADEVSV	Save area for device address for relocation								
22		DEVSAVE	Save device address when trap 1								
23											
24											
25		FIDAHI	IDA word high-order								
26		FIDAMI	IDA word middle-order portion								
27		FIDALO	IDA word low-order portion								
28 to 3F		Not used									

Chapter 4. Functional Units

Interconnections

This page shows the manner in which the systems internal buses, IOP '9', multiplexer channel, and the standard interface are connected.



1 to 8 These lines are not described in the multiplexer channel documentation. For more details, refer to *IBM 3125 Processing Unit, Input/Output Processor,* Maintenance Library Manual, Order No. SY33-1063.

0 Chain control lines (CCL), octopus control lines (OCL), and other controls.

1 Trap bit lines

2 IPU tag register bits 1 and 7

3 Standard interface bus out lines.
Information is transferred from the multiplexer channel to I/O devices via the bus out lines under control of the tag out lines.

4 Standard interface tag out lines.

5 External register addressing and control lines.

6 External in buses.

7 IOP D-register out.

8 Standard interface bus in lines.
Information is transferred from the I/O devices to the multiplexer channel via the bus in lines under control of the tag in lines.

Standard interface tag in lines.

For detailed explanations of each line refer to pages 4-030 and 4-040.

- The multiplexer channel provides 32 UCWs (or subchannels).
- UCWs 0 to 7 may be shared UCWs, but UCWs 8 to 31 are non-shared (see page 2-070).
- Up to 8 control units may be attached to the multiplexer channel. This restriction is made in order to prevent load problems on standard interface.
- Up to 32 UCWs are available.

General Description of Cards

MPX Control Card (01BA1F)

The MPX control card consists of the following:

Register '01'. Used as the tag out register and holds information that defines standard interface bus out.

'Trap Request' Fliplatches. Used to control execution of the microprogram.

Circuitry. To generate signals and to control the multiplexer channel. This circuitry handles the following:

Interrupt requests
Response to IPU
Power on reset, etc.

T-Counter. Defines burst mode.

Register 'OD'. Holds control and check information.

For more details refer to the following Pages:

3-100 — tag out register layout
4-040 — Description of tag out lines
4-070, 4-075 — MPX control and circuitry.

The ALD reference for the MPX control is KA22X.

External Register Card (01BA1D)

The external register card consists of six registers and their addressing circuitry. These registers each are one byte wide and are used to communicate with both the system and the attached devices.

Reg '00'. Used as bus in register and hols the information that was transferred from the I/O devices.

Reg '04'. Used as bus out register and holds the information that was transferred from the multiplexer channel to the I/O devices.

Reg '08'. Used as tag in register and holds information that defines standard interface bus in.

Reg '10'. Used as front end sense register and holds the multiplexer channel control information.

Reg '0C'. Used as I/O device address register and holds the address of the currently operating device. This register is used to address the UCW on the UCW buffer card.

Reg '14'. Used as front end control register and holds the multiplexer channel control information.

For more details refer to the following Pages:

3-100 — External register layout
4-040 — Description of tag in lines
4-080 — External register card circuitry.

The ALD reference for the external register card is KA28X.

UCW Buffer Cards (01BA1G and H)

The UCW buffer cards together consist of 12 x 32 registers with their addressing circuitry. These registers hold 12 bytes out of the 24 bytes from all the 32 UCWs. All the registers are one byte wide.

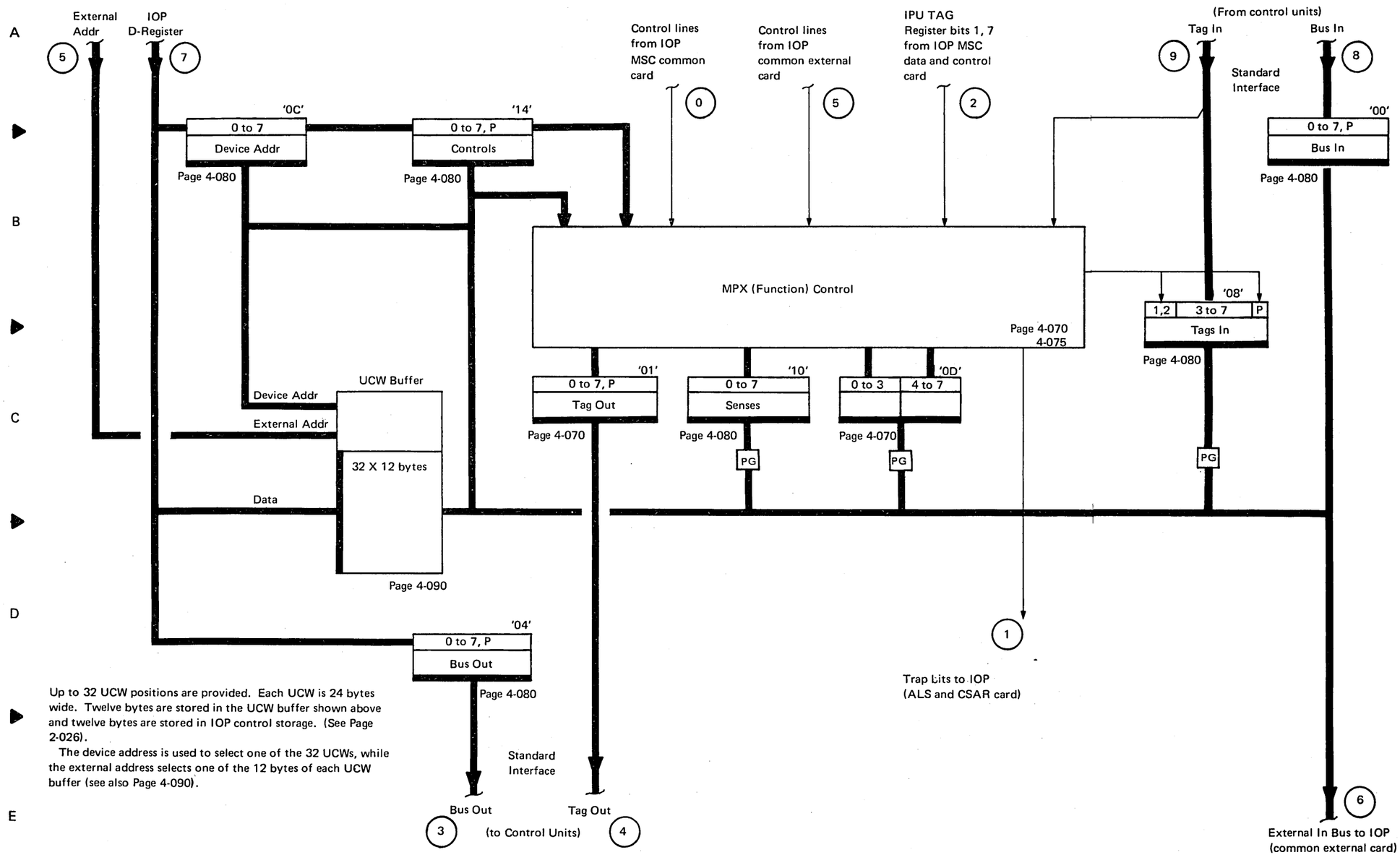
UCWs (a group of 12 registers) are addressed by the device address, which is held in register 'OC' on the external register card. Each byte out of the group of 12 registers is addressed or selected by the external register addresses.

For more details refer to the following Pages:

2-025 — UCW format
3-100 — UCW registers layout
4-090 — UCW buffer card circuitry.

The ALD references for the UCW buffer card are KA16X (UCWs 1 to 6) and KA10X (UCWs 7 to 12).

MPX Front End Data Flow



Note: The circled numbers represent the line groups as they are shown on Pages 4-010, 4-030 and 4-040;

Up to 32 UCW positions are provided. Each UCW is 24 bytes wide. Twelve bytes are stored in the UCW buffer shown above and twelve bytes are stored in IOP control storage. (See Page 2-026).

The device address is used to select one of the 32 UCWs, while the external address selects one of the 12 bytes of each UCW buffer (see also Page 4-090).

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4 Functional Units

Lines from IOP '9' to Multiplexer Channel Front End

The circled numbers in the first column of each table represe
the line group as shown on Page 4-010.

Line Group	Line Name	Line Description
0	Halt I/O or halt device	This line signals that an I/O operation has to be terminated and causes 'trap 2' FL to be set.
	Metering out	This line is activated by the IPU at the moment when the process meters begin to run.
	Power on reset	This line is activated when power is switched on, and causes the 'power on reset' FL to be set.
	Select IOP from IPU	This line is active when MPX-IOP communicates with the IPU.
	System reset	This line is activated by the system reset manual operation and causes the 'trap 3' FL to be set.
2	Aux irpt request (IPU tag register bit 7)	These two lines actually are bits from the IPU tag register on the MSC data and control card.
	Response to IPU (IPU tag register)	These two lines cause the 'irpt/requ' and 'response' FLs to be set according to multiplexer channel requirements.
5	External address bits 0, 1, 2 External address gate bits 0 to 3 External address group bit 0	These lines are activated by the MPX-IOP under control of the MPX microprogram and are used to address the multiplexer channel external registers.
	External select gate	Activated by the MPX - IOP for all those microinstructions that use external addresses.
	External write out	Activated by the MPX-IOP for all those microinstructions that load information from the multiplexer channel into external registers.
	Alternate sense strobe	This is a T56 timing pulse that controls the reset and set of external registers.
	Sense strobe IOP '9'	This is a T02 timing pulse that controls the reset and set of external sense registers.
7	IOP D-register bits 0 to 7, P	This is the exit of MPX-IOP ALU D-register. These lines are to be considered as IOP bus out.

Lines from Multiplexer Channel Front End to IOP '9'

Line Group	Line Description	Line Description
0	Busy to IPU	This line is activated by the multiplexer channel to signal that a burst operation is in progress.
	Interrupt request	This line is activated to request an interrupt in the IPU.
	Metering in	This line signals that an I/O operation is in progress and is activated by the control units
	Reset (MSC) check IOP '9'	This line is activated in the multiplexer channel and is gated to the MSC common card. The line is used to reset the MSC check bits.
	Response to IPU	This line is active as a result of setting the 'response' FL. The line controls communication between MPX-IOP and IPU.
1	Trap 1, 2, 3 request	Trap requests are activated according to multiplexer channel requirements. The trap bits are gated to the trap register in the IOP nucleus where they are used to alter the chain of index words. This, in turn, controls the execution of microprogram routines.
6	External in buses, bits 0 to 7, P	Four external in buses are connected to an IOP. Information is transferred, via these external in buses, from the multiplexer channel cards to the ALU card in the IOP nucleus.

Lines from Standard Interface to Multiplexer Channel Front End

Line Group	Line Name	Line Description
(9)	Lines listed in this section belong to IBM standard interface	
	Address in (ADI)	When active, this line signals that the device address is on bus in.
	Operational in (OPI)	When active, this line signals that the addressed device is selected.
	Request in (RQI)	When active, this line signals that one or more control units require service.
	Select in (SLI)	This line extends the 'SLO' line from the last control unit back to the channel. If the line is active, it means that no unit is selected.
	Service in (SVI)	When active, this line signals either that the control unit offers a byte to the channel on bus in or that the control unit expects a byte from the channel on bus out.
	Status in (STI)	When active, this line signals that a status byte is on bus in.
	Lines listed in this section belong to IBM System/370 interface extension	
	Data in	Not used by multiplexer channel
	Mark in	Not used by multiplexer channel
	Disconnect in	This line is connected from control units to the channel. In conjunction with OPI, this line when active, signals that an error condition occurred in the control unit or device and prevents further data handling. When the line is active, trap 3 is forced in the multiplexer channel, resulting in termination of the operation by selective reset becoming active.

Lines from Multiplexer Channel Front End to Standard Interface

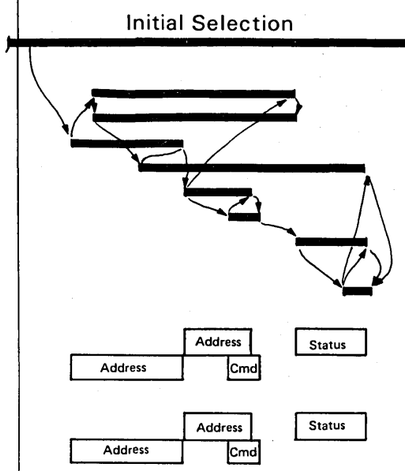
Line Group	Line Name	Line Description
(4)	Lines listed in this section belong to IBM standard interface	
	Address out (ADO)	This line provides two functions: a. *I/O Selection.* Signals the control unit that the device address is on bus out. b. *Disconnect Operation.* If 'ADO' is active when 'hold out' is inactive the control unit has to inactivate 'operational in'.
	Command out (CMO)	When active, this line signals that the command is on bus out. In addition, if 'CMO' follows: • ADI, it means proceed (during reselection) • SVI, it means stop • STI, it means stock status.
	Hold out (HO)	This line may be considered as gating for the 'SLO' line.
	Operational out (OPO)	This line is used for interlock purposes. In connection with 'SPO', it causes a 'selective reset'.
	Select out (SLO)	This line is used for selection purposes. Propagation of 'SLO' is suppressed as soon as a control unit or device, respectively, is selected (that is, activation of operational in).
	Service out (SVO)	This line specifies: • When following SVI, that the channel accepted the byte that was offered by the control unit on bus in or that the channel sets the byte that was expected by the control unit on bus out. • When following STI, that the channel accepted status.
	Suppress out (SPO)	This line has different functions. It is used in connection with the following: • Command chaining • Reject status • Selective reset • Devices working at an adjustable data rate.
	Lines listed in this section belong to IBM System/370 interface extension	
	Data out	Not used by multiplexer channel
	Mark out	Not used by multiplexer channel
	Clock out	Not used by multiplexer channel

Sequence of Tag Lines on Standard Interface

The microprogram controls the activation and inactivation of the necessary tag out lines in proper sequence.

The address control unit in turn answers, by activating and inactivating the appropriate tag in lines.

Initial Selection



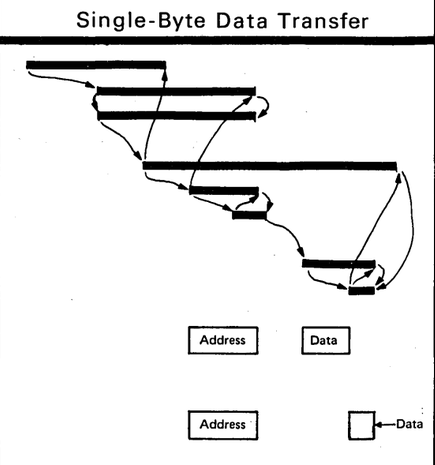
To initiate an I/O operation, the channel places the device address on bus out and activates the 'address out' line.

After activating 'select out' and 'hold out', the first control unit on the standard interface decodes the address on 'bus out' and propagates 'select out' if the address does not match. The control unit with the matching address does not propagate 'select out' and activates 'operational in'.

Subsequently the control unit replies with 'address in', the channel transfers the command to the control unit and, if no unusual condition exists, the control unit sends an all-zero status.

After the channel replies with 'service out', the control unit inactivates the 'operational in' line, which means disconnection from the standard interface.

Single-Byte Data Transfer



As soon as a control unit is ready to transfer data to the channel (input operation) or a control unit requires data from the channel (output operation), the control unit activates its 'request in' line.

The channel starts a reselection by activating 'hold out' and 'select out'. The control unit then activates its 'operational in' line and sends its address to the channel. The channel answers with 'command out' which means proceed.

On an input operation, a control unit then places the data byte with 'service in' on 'bus in'. As soon as the channel has accepted this data byte, it responds with 'service out'.

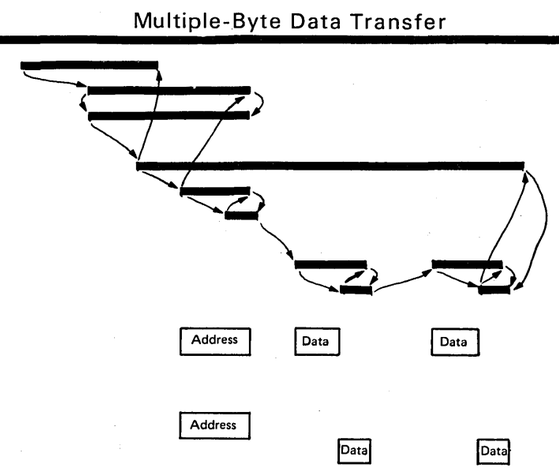
On an output operation, a control unit requests data from the channel by activating the 'service in' line. The channel places data on 'bus out' with 'service out' active.

Single- or multiple-byte transfer is determined by the control unit by holding up 'operational in' as long as necessary.

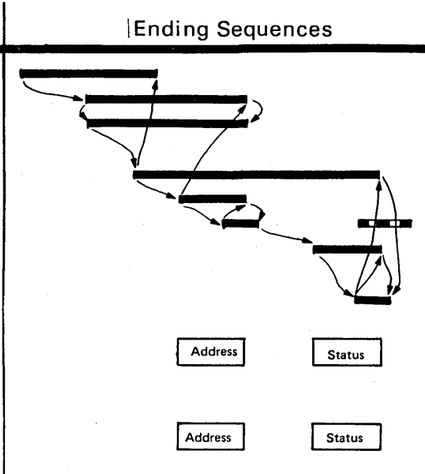
Regular conditions under which data transfers may be terminated are:

a. Data offered by device and byte count equals the I/O count, for example, read 80 columns, byte count = 80. Data transfer ends with SVI/SVO and the status is presented with 'request in'.
b. Data offered by device and byte count is lower than the I/O count, for example, read 80 column, byte count = 40. Data transfer ends when the forty-first byte is offered with SVI because the channel responds with CM0.
c. Data offered by device and byte count is higher than I/O count, for example, read 80 columns, byte count = 100. Data transfer ends after 80 bytes have been transferred because the status is then presented by the control unit.

Multiple-Byte Data Transfer



Ending Sequences



With channel end alone, or channel end with device end, the status byte is set into the unit status byte in the UCW. STI is followed by SVO, indicating that the status is accepted. Subsequently the 'interrupt request' FL is set, which in turn causes activation of the 'interrupt request' line to the IPU.

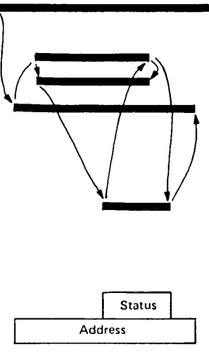
Device end alone is always stacked until an interrupt occurs or a 'TIO' instruction is issued. Device end status is then fetched from the control unit.

Signal

Operational Out
Request In
Hold Out
Select Out
Address Out
Operational In
Address In
Command Out
Status In
Service In
Service Out

Bus In
Bus Out

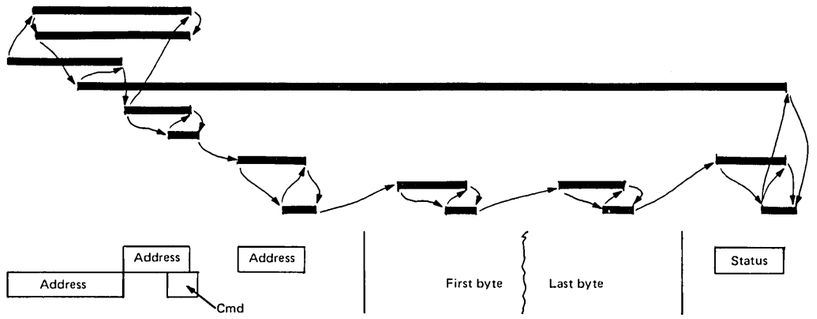
Selection of a Busy Control Unit



If the addressed control unit is found busy, SLO is immediately followed by STI.

The status byte contains a busy bit and a 'status modifier' bit.

Data Transfer in Burst Mode



Initial selection

If no unusual condition is found, initial status contains only zeros.

If the device is found to be busy, the operation is terminated after the initial selection. The initial status contains a 'busy' bit.

If a device is found with device end not yet accepted (that is stacked status) the initial status contains the device end.

Data Transfer

In burst mode the control unit keeps the line 'OPI' active until the operation is completed. This allows transfer of the full record from first to last byte.

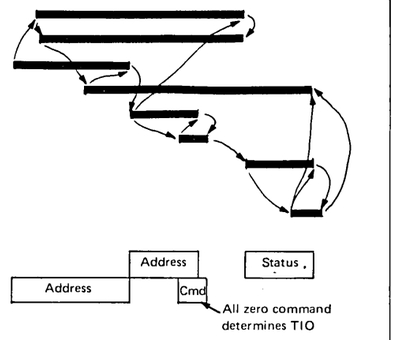
Ending Sequence

The status byte is presented automatically under the following conditions:

a. Byte count equals the I/O count.
b. Byte count is greater than the I/O count.

If the I/O count is higher than the byte count, the I/O device tries to transfer another byte after the byte count becomes zero. The channel rejects this byte by activating 'CMO'. After this "unsuccessful" data transfer, the control unit presents its status.

Test I/O



The 'TIO' (all zero) command is issued with the 'TIO' instruction, when the subchannel is available, or when a secondary interrupt is handled in order to retrieve a stacked device end status from the device.

The sequence of tag lines is the same as for a regular initial selection.

MPX Control Card

External In Buses

Either register '01' or register '0D' is gated with its address and 'card select' to 'external in bus 2'. Note that only the lower half of register '0D' has the ability to store.

'Card select' is also used to suppress 'external in bus 2' if no register on this card is selected.

Tag Out Register

The reset and set of register '01' (which is the tag out register) is microprogram-controlled, but with the following exception:

A specific reset condition exists for the 'command out' and 'service out' lines. These two lines are set by microprogram and reset by the multiplexer channel circuitry.

'Command out' is inactivated when either 'address in' or 'status in' or 'service in' becomes inactive.

'Service out' is inactivated when either 'status in' or 'service in' becomes inactive.

During "stack status" (that is, device end status) 'command out' is held active until 'operational in' becomes inactive by means of 'suppress out'. (See also the microprogram flowcharts on Page 3-060.)

T-Counter

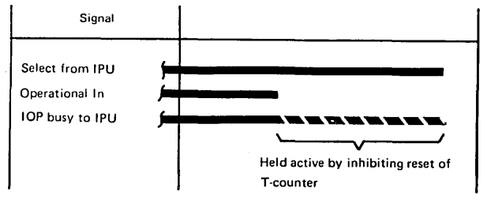
This counter is used to define burst mode. If the multiplexer channel is not working, T-counter 'reset' is kept active by the inactive 'operational in' line.

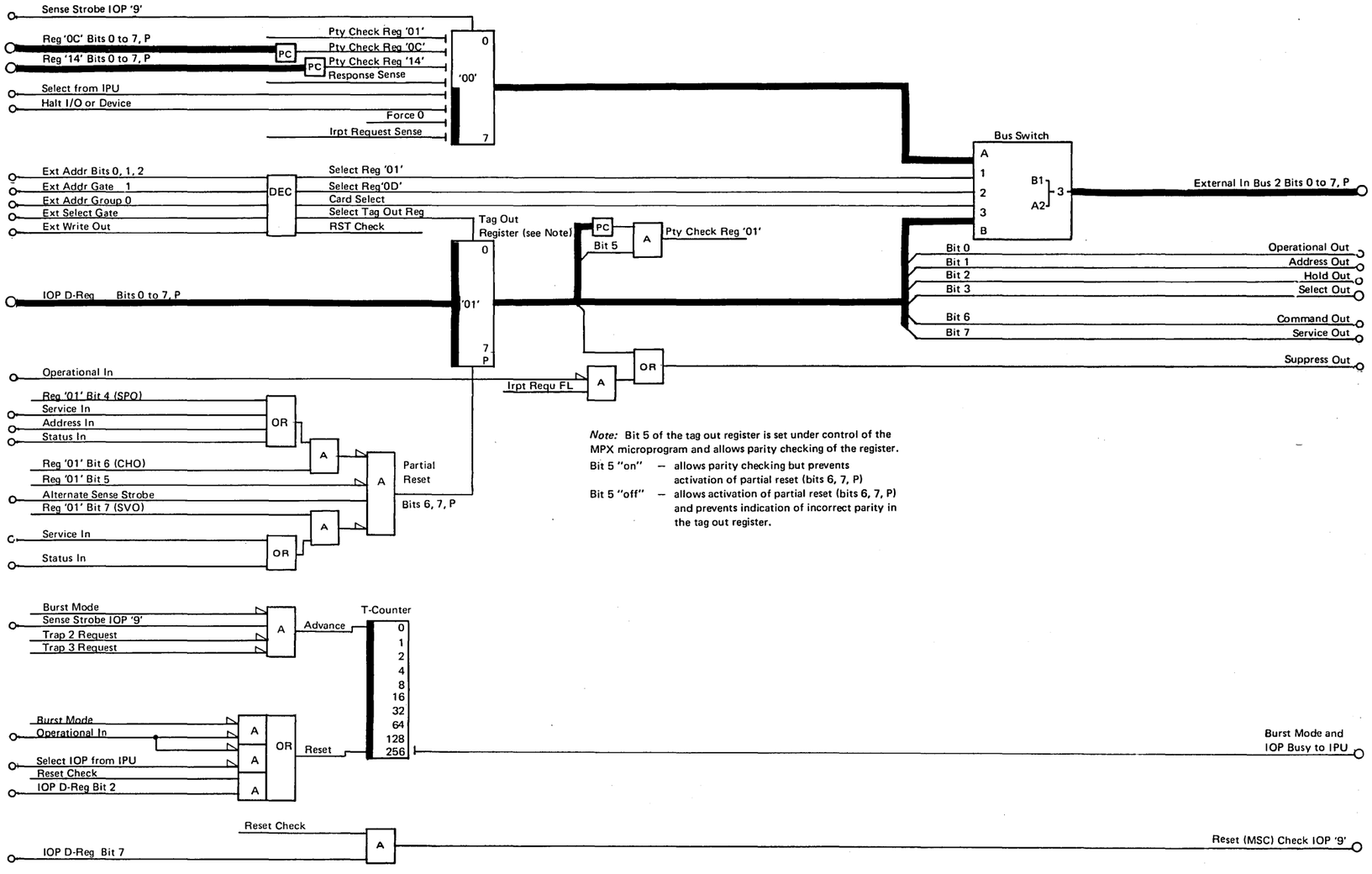
If no higher trap request, except for data transfer, is present and 'operational in' becomes active, T-counter 'reset' becomes inactive and advance pulses now step the T-counter. When the T-counter reaches half of its maximum value (after approximately 115 μs) counter position 256 switches and defines burst mode.

If 'operational in' becomes inactive again, the T-counter is reset.

If a higher trap request becomes active, the T-counter advance pulses are suppressed and burst mode cannot be specified. T-counter advance pulses are strobed by the signal 'sense strobe'.

If 'operational in' becomes inactive shortly after 'select from IPU' became active with the multiplexer channel working in burst mode, the IPU must recognise the 'IOP busy to IPU' line. The 'IOP busy to IPU' line is held active by inhibiting the T-counter reset for as long as 'select from IPU' is active.





ALD Ref KA22X

Trap Request FLs

The circuitry on this page shows the conditions under which the 'trap request' FLs are activated.

A

'Trap 1 Request' FL

- Handles data transfers between MPX and I/O device and status representations with 'request in'
- See also the microprogram flowcharts on Page 3-060.

'Trap 2 Request' FL

- Handles HIO or HDV when the multiplexer channel is working in burst mode.
- See also the microprogram flowcharts on Page 3-080.

B

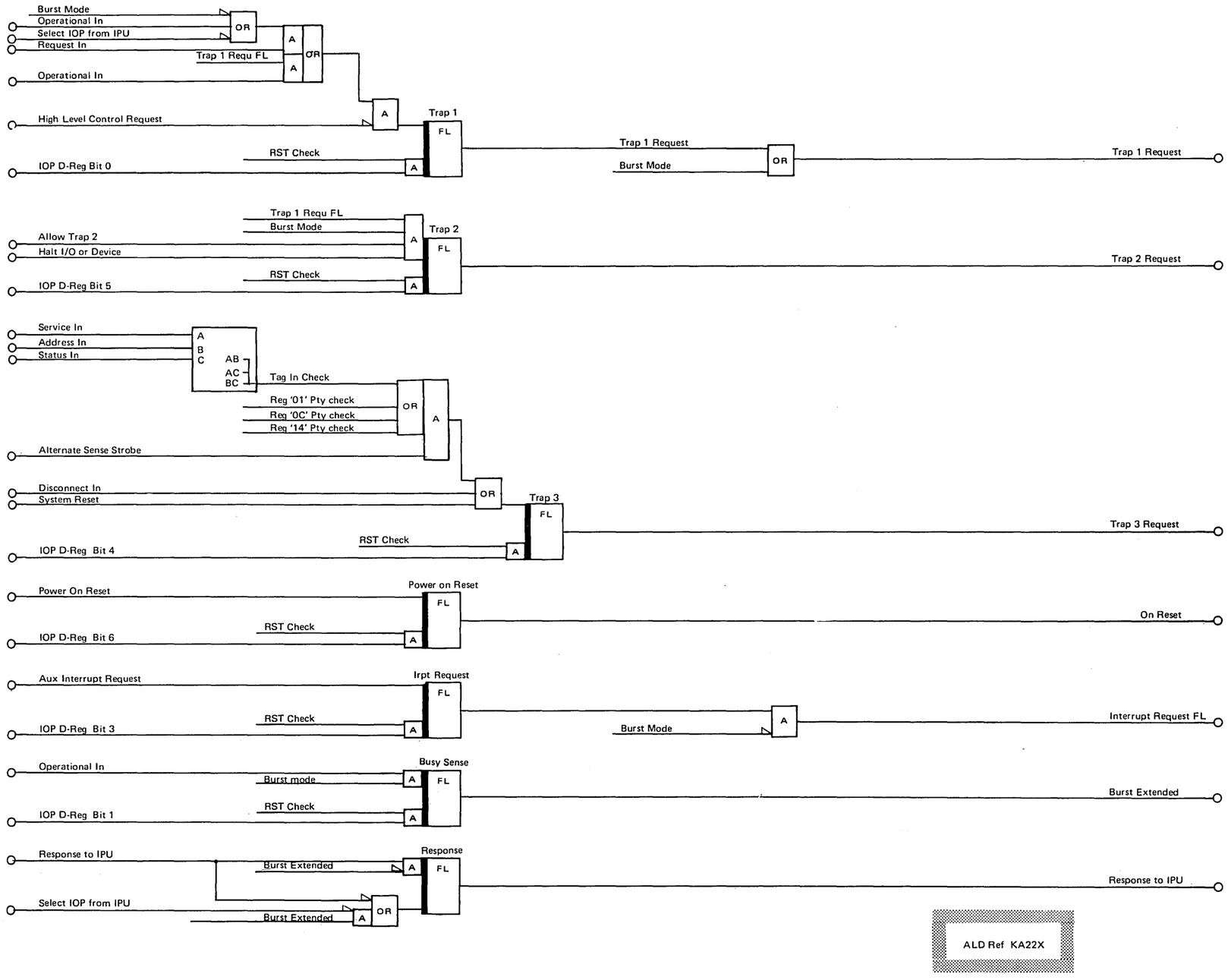
'Trap 3 Request' FL

- This trap is for error handling:
  - Tag in check
  - Register parity checks
  - Disconnect in
  - System reset.
- See also the microprogram flowcharts on Page 5-030.

C

D

E



External Register Card

External In Bus

A The bit patterns of the registers shown here are gated with their corresponding addresses and with the signal 'card select' to IOP '9'. The gating is done in the bus switch circuitry.

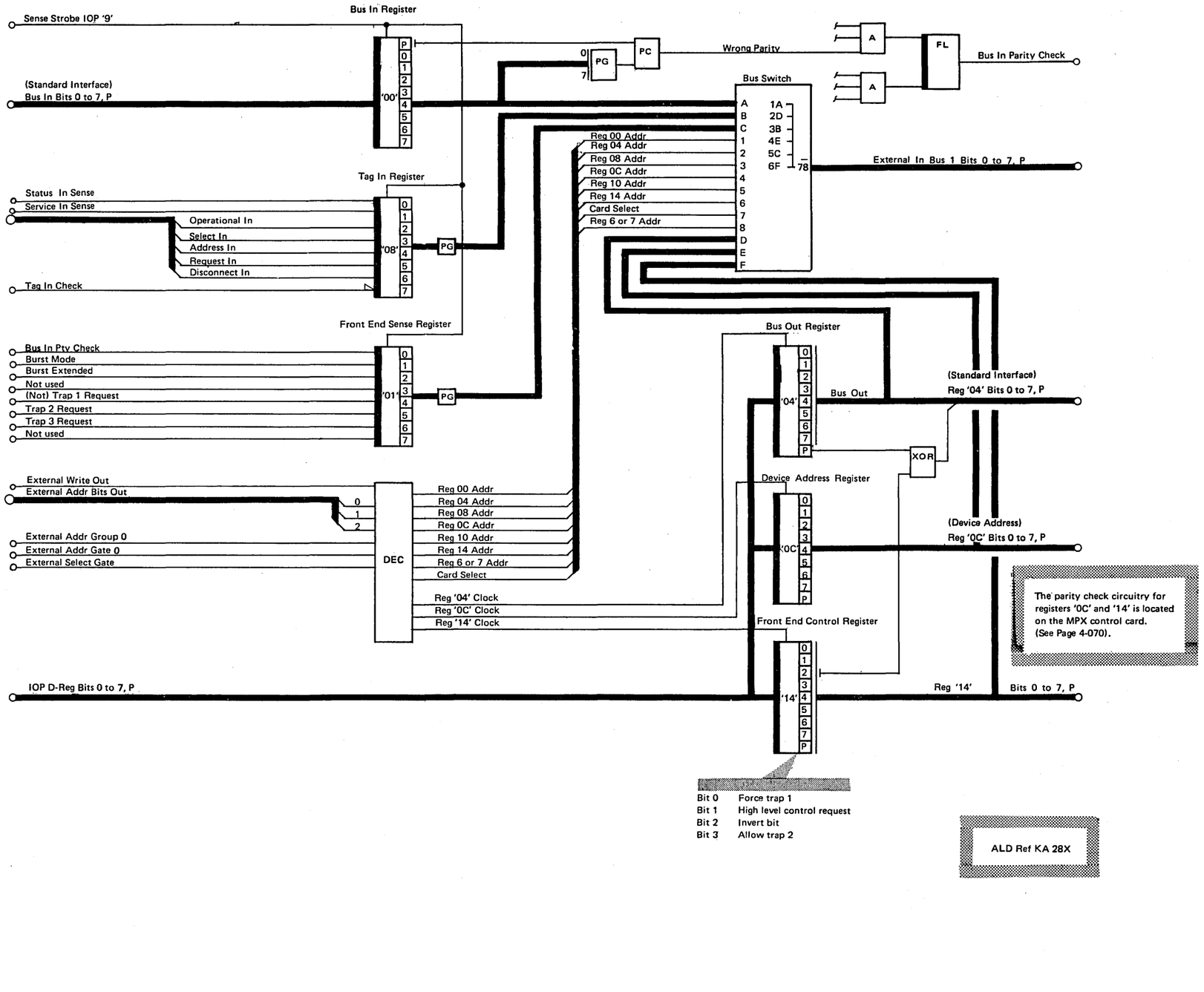
Suppression of External In Bus

'External in bus' suppression is required to avoid double selection on the 'external in bus' between the external register card and the MSC data and control card. The line 'reg 6 or 7 addr' active actually does the suppression.

External register cards contain 6 registers. Three external address bits are used for the addressing of these registers.

B Because the decoded addresses 06 and 07 are not needed on the external register card, these two addresses are used to address registers on the MSC data and control card, independent of the zone in the microinstruction. This in turn causes 'card select' to be activated without a register being selected on the external register card.

Further details are given on Pages 2-030 (write operation) and 2-040 (read operation).



UCW Buffer Cards

This buffer or storage is used to store
12 bytes out of the 34 bytes of the 32 UCWs.

UCWs are generated and loaded into UCW buffer under control of MPX microprogram.

UCW buffer is addressed by decoding the device address that is held in external register '0C'.

When addressed, the twelve bytes appear at the exit of the UCW buffer.

The desired byte in turn is selected by
External Addr. Bits 0, 1, 2, and
External Addr. Gate 2 and 3.

Because the selection of a single byte follows the same scheme as used with external register addressing

- External Addr Bits 0, 1, 2 address 6 registers, while
- External Addr Gate 2 and 3 group the twelve registers in two groups of 6 bytes each.

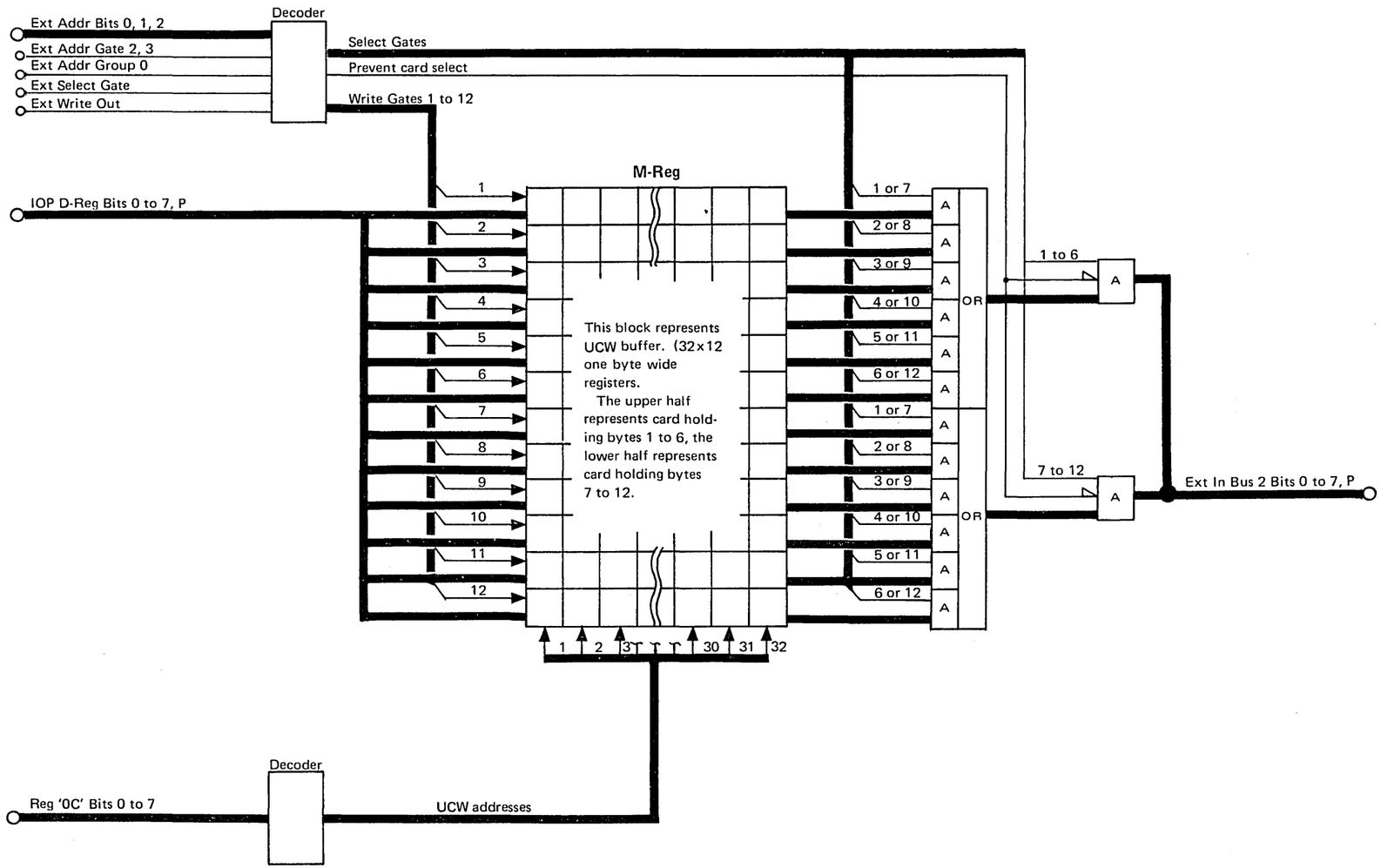
Write gates are also generated separately for each single byte.

This allows to either

- read or
- write

each byte of each UCW independently.

The signal 'prevent card select' suppresses External In Bus to avoid double selection of card exits on dotted External In connections. (See also note 1 on page 4-080).



Chapter 5. Error Conditions

Introduction

This chapter contains two categories of information about error conditions:

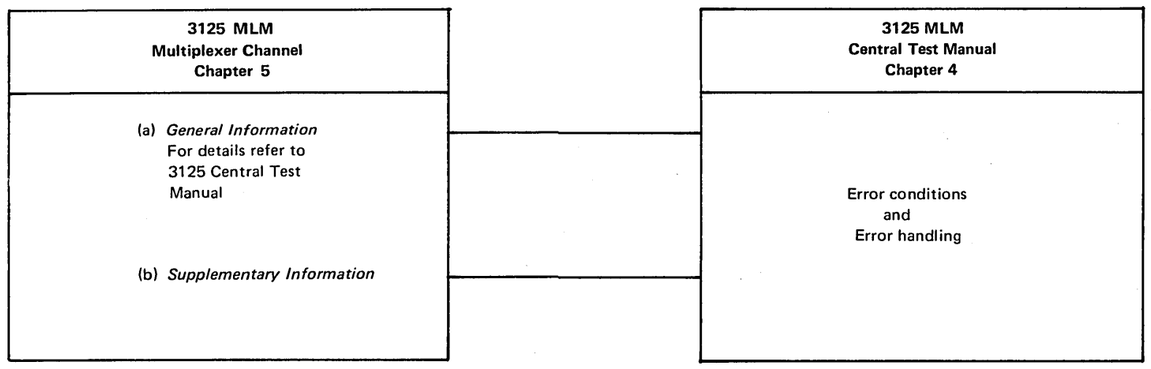
(a) *General Information*

- Error types
- Error handling
- Results of errors.

(b) *Supplementary Information to 3125 Central Test Manual*

- Generation of error signals
- Trap 3 microroutine.

The error conditions and error handling are detailed comprehensively in Chapter 4 of the EC-controlled *3125 Central Test Manual,* Maintenance Library Manual.



Unusual or Exceptional Conditions

Unusual or exceptional conditions are caused either by channel malfunction or device malfunction and are therefore indicated in either the channel status or the unit status.

The table below shows these unusual or exceptional conditions as they are set into either the channel status byte or the unit status byte.
(See also Pages 2-020 for CSW Layout and 2-025 for UCW Layout).

The lowest section of the table shows part of sense byte 0, which is common for all I/O devices. (Bits 6 and 7 are device specific.) For the other sense bytes, which contain device specific information, refer to the respective I/O device documentation or control unit documentation.

Status byte and sense bytes are delivered from the addressed control unit and are transferred via the channel to main storage. Status- and sense-byte information is analyzed by the operating system that is used and corrective actions are initiated.

Error Type	Bit Pos	Byte	Error Caused	Result
Channel Control Check	5	Channel Status	By any machine malfunction that affects the channel controls. This condition includes parity errors on the CCW and data addresses.	Operation is terminated
Interface Control Check	6		By device malfunctions such as: a. Address or status byte received has invalid parity. b. Device responds with an address other than that specified. c. Device appears not operatoinal during chaining. d. A signal from the device appears at an invalid time or has invalid duration.	Operation is terminated
Channel Data Check	4		By parity errors with the information transferred to/from main storage.	Operation is not terminated; chaining is suppressed
Chaining Check	7		By an overrun condition during data chaining.	Operation is terminated; chaining is suppressed
Program Check	2		By one or more of the following conditions; Invalid CCW address; invalid command code; invalid count; invalid data address; invalid key; invalid CAW format; invalid CCW format; invalid sequence.	Operation is terminated; chaining is suppressed In connection with CCW, operation is not initiated. In connection with data, operation is terminated and chaining is suppressed.
Protection Check	3		By an attempt to fetch data from or store data into a protected storage area.	
Incorrect Length	1		If offered or requested, data does not correspond with length or byte count.	If SLI flag is not set to "on": chaining is suppressed.
Unit Check	6	Unit Status	If unusual conditions are found in the device; details are given with the information delivered by the sense command. See Note	Chaining is suppressed
Unit Exception	7		Indicates a typical condition for any particular command and type of device.	Chaining is suppressed
Command Reject	0	Sense Byte 0	By command to a device which is not designed to execute that command, for example, read to a printer, rewind to disk file.	Program error operation is terminated after initial selection
Intervention Required	1		By a condition that requires some type of intervention at the device, for example, stacker full, hopper empty, printer out of paper.	Operation is not executed
Bus Out Check	2		By parity errors on the standard interface.	If data parity error, operation is not terminated. If command parity error, operation is not executed.
Equipment Check	3		By equipment malfunction, for example, print buffer parity error.	Operation is terminated
Data Check	4		By errors that are associated with a recording medium, for example, reading invalid card code.	Operation is not terminated
Overrun	5		By not responding in time to a request from a device for service.	Operation is not terminated

Note: Unit check is generated individually according to particularities of the different I/O devices. For details refer to respective I/O device as control unit documentation.

Error Handling

The errors can be divided into two categories.

A a. Channel-sensed errors
b. Hand error

Channel-Sensed Errors

- These errors do not stop IOP 9 ; they cause a trap 3 request.
- Trap 3 request forces the microprogram to the trap 3 routine.
- Trap 3 routine does the following:
  a. Sets a check bit into channel status
  b. Prepares CSW, ECSW and LOG area
  c. Terminates the operation (except for channel data check)
  d. Requests an interrupt

B e. Stores interruption code
  f. Stores CSW and ECSW
  g. Activates log request (sets PCR bit into SVP idle SENS)

- Trap 3 routine is detailed on Page 5-030.

Hard Errors

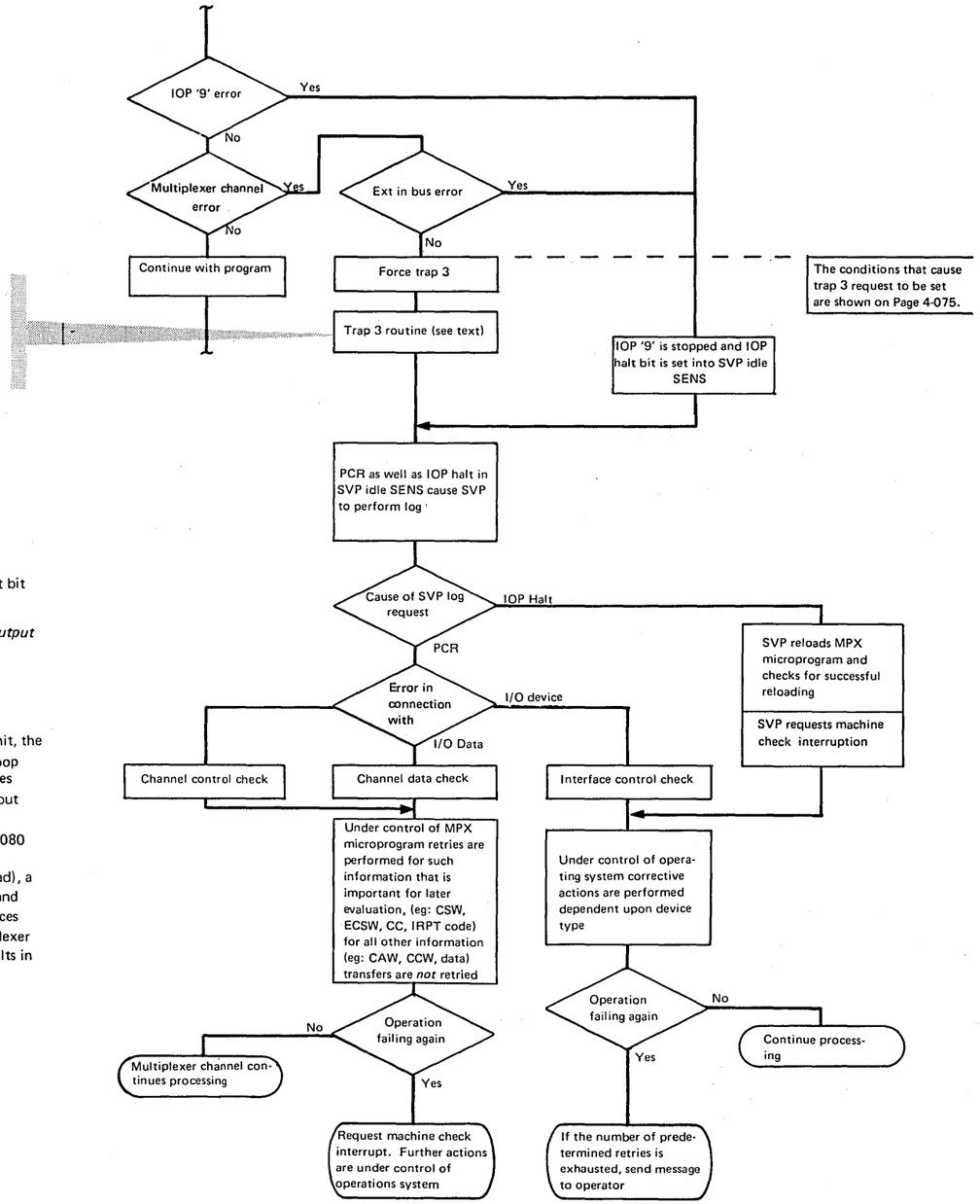
- These errors are caused by the following:
  a. Parity errors on the external in bus to IOP '9
  b. Errors in the IOP '9' circuitry.
- These hand errors cause log request by activating the IOP halt bit in SVP idle SENS.

C
- For more details refer to *IBM 3125 Processing Unit Input/Output Processor,* Maintenance Library Manual Order SY33-1063.

Timeout Conditions

Timeout conditions are checked at numerous points in the MPX microprogram. To check the correct response from a control unit, the multiplexer channel sets a *timeout counter.* A microprogram loop periodically decreases the counter value by 1. If the count reaches zero before a response is received from the control unit, a 'timeout exhausted' bit is set, which causes a branch to an error routine. (General information about error conditions is given on Pages 3-080 and 6-020).

D For certain circuit errors (for example, SVI or SVO tag lines dead), a 30-second timeout allows the MPX microprogram to recognise and handle the error. If the program starts a new operation that forces the same error condition while logging is in progress, the multiplexer channel will not transmit correct log data to the SVP. This results in a *log error* condition, and no log is stored on the diskette.

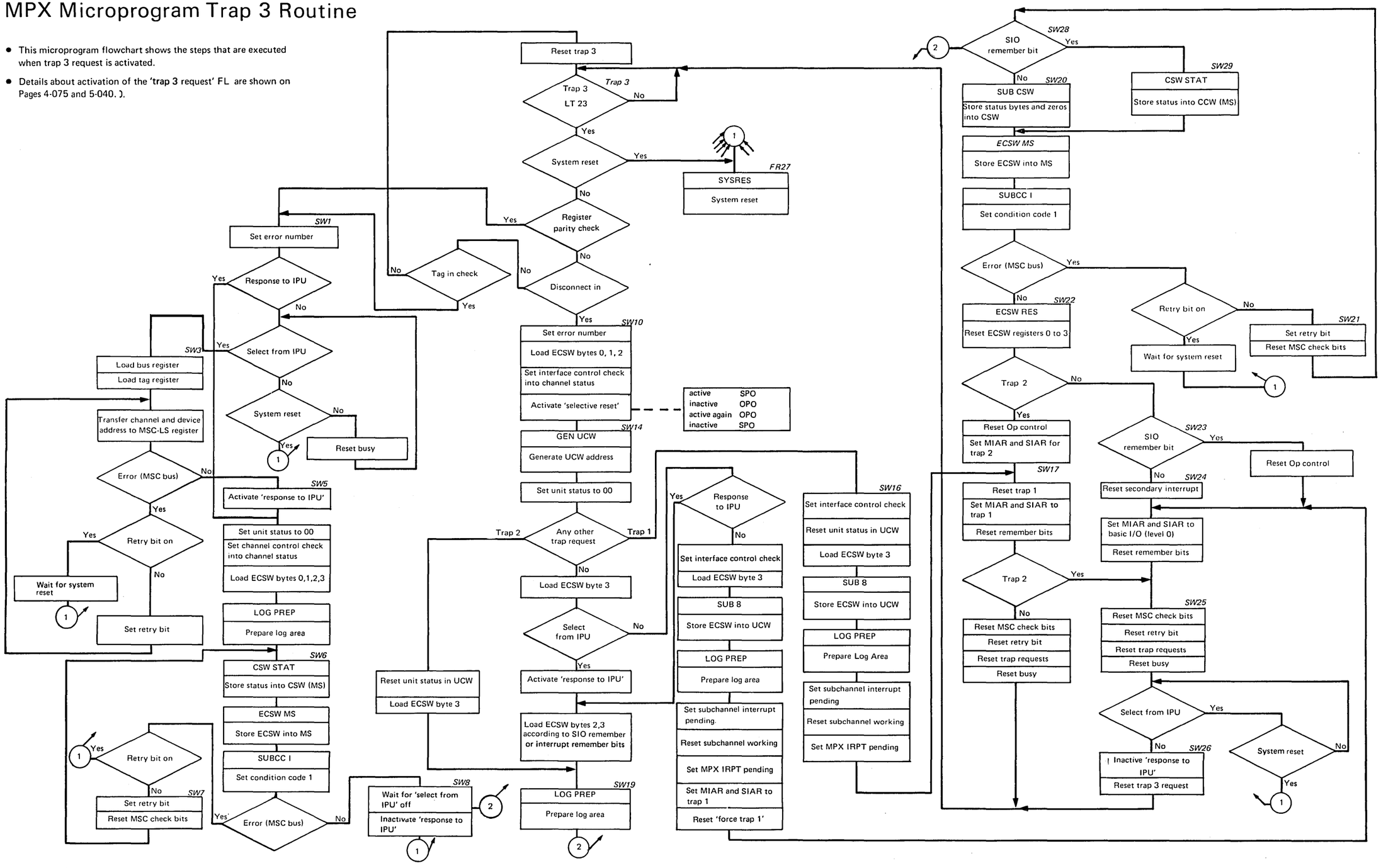


Logging

- To ensure error data retention for system malfunction analysis all solid and intermittent errors are recorded on a system diskette.
- Error recording is performed as long as the SVP main SENS loop is active, but will not be performed during application of micro-diagnostics and manual CE operations.
- Each system component to be recorded is assigned a separate log area.
- The multiplexer channel log area consists of:
  Header
  Lost log
  Condensed log.
- Recorded log data (that is, last log, as well as condensed log) can be:
  a. Displayed or
  b. Evaluated by log analysis program or
  c. Erased if no longer required.
- The last log contains the following:
  Device address
  Unit status
  Channel status
  Error data.
- The condensed log contains the following:
  Error data
  Error count
- During log recording, the keyboard remains locked.

MPX Microprogram Trap 3 Routine

- This microprogram flowchart shows the steps that are executed when trap 3 request is activated.
- Details about activation of the **'trap 3 request'** FL are shown on Pages 4-075 and 5-040.).



Error Circuits

External Register Card

On external register card the bus in register is parity checked. A

With parity errors, the parity check FL is set, the output of which is gated via the front end sense register and external in bus into IOP '9'. The MPX microprogram then recognises the check condition and causes a channel data check to be set into the status.

MPX Control Card

On the MPX control card, the tag out register is parity checked. B

The outputs of registers '0C' (device address) and '14' (front end control) on the external register card are connected to the MPX control card where these two registers are parity checked.

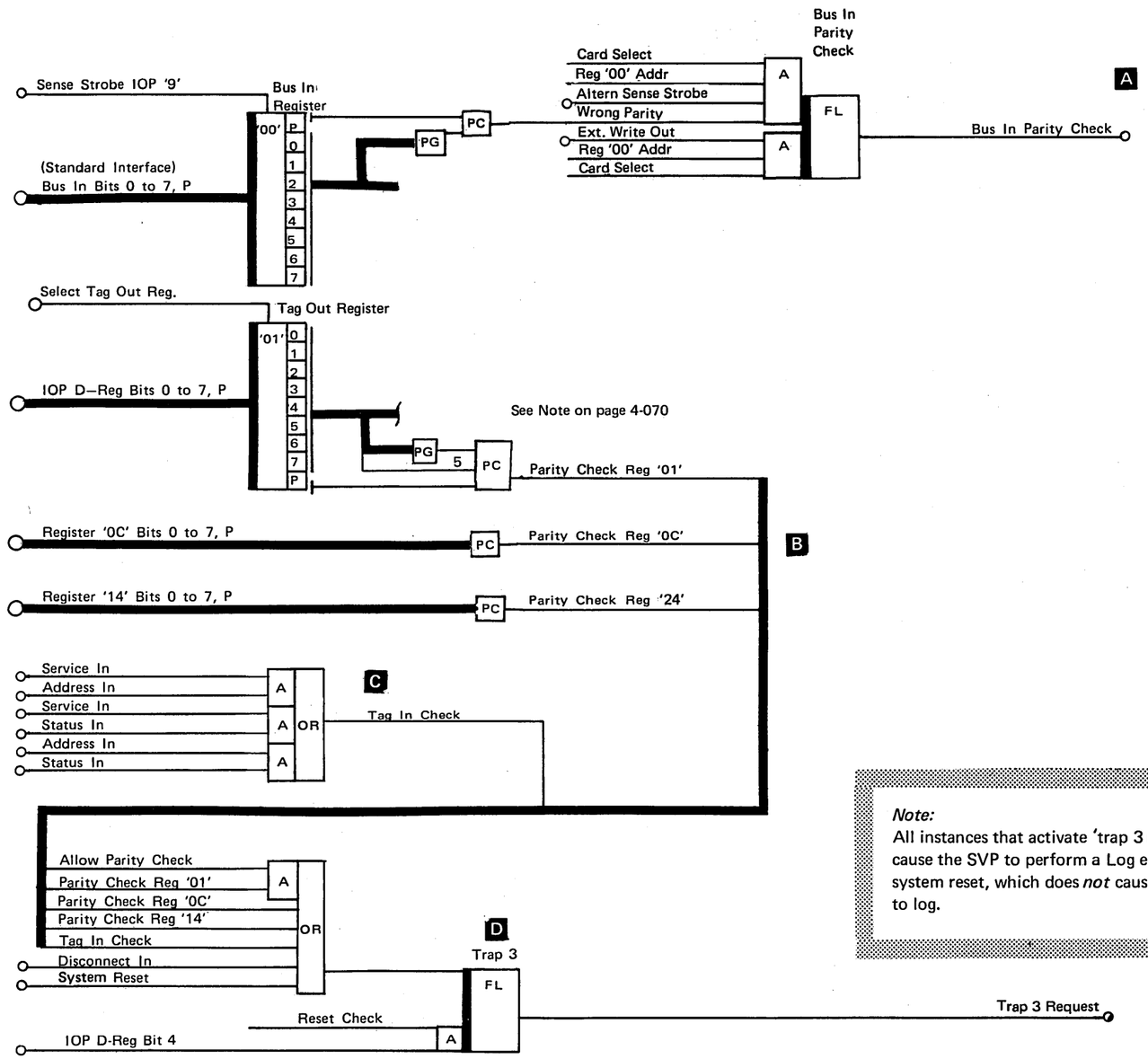
A tag in check is also generated. C

The three register parity checks, together with 'tag in check', 'disconnect in' and 'system reset' cause the 'trap 3' FL to be set. D

The output of 'trap 3' FL is the 'trap 3 request' line which is connected to the trap register on the ALS/CSAR card of the IOP nucleus. The MPX microprogram is forced to its trap 3 routine (highest priority) by altering the link portion of the currently used index word. The trap 3 microprogram routine handles the error condition. For details, see the microprogram flowchart on Page 5-030.

Wrong parity of any external register that is gated to the IOP '9', via external in buses, causes a hard-stop of IOP '9'

The error circuitry of the IOP '9' is given in *IBM 3125 Processing Unit, Input/Output processor,* Maintenance Library Manual, Order SY33-1063.



Note:
All instances that activate 'trap 3 request' cause the SVP to perform a Log except for system reset, which does *not* cause the SVP to log.

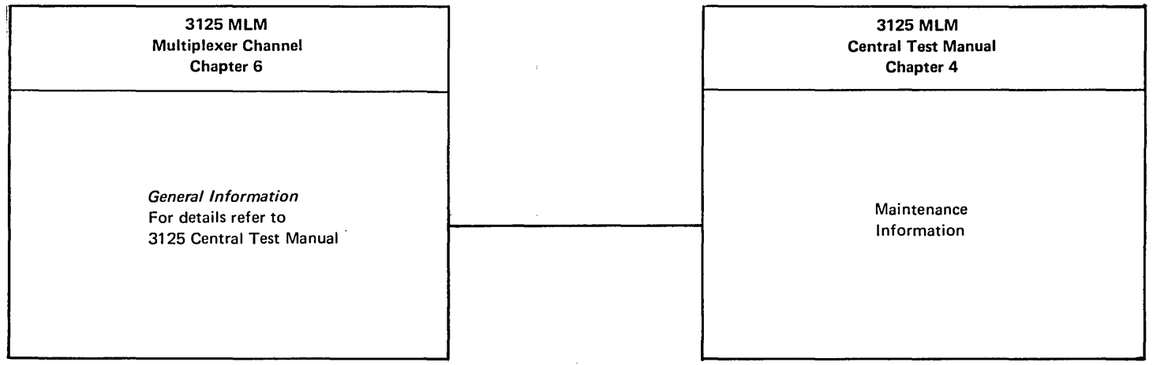
Chapter 6. Maintenance Information

Introduction

This chapter contains general information about the following:

- Maintenance concept
- Diagnostic techniques
- Test programs.

Comprehensive maintenance information is given in Chapter 4 of the EC-controlled *3125 Central Test Manual,* Maintenance Library Manual.



Maintenance Concept

- The multiplexer channel does not contain any circuits that require adjustments (for example, singleshots, time delays, etc).
- In the event of a malfunction, eliminate the cause by changing cards according to the instructions given on the display unit.
- Whenever cards are changed, check the socket pins.
- The information displayed on the display unit is the result of the log analysis program. The log analysis program analyzes and evaluates log information that was stored during the normal run phase.
- Where more than one card is suspected, the suspected cards are indicated according to the degree of probability for the cause of the fault. This indication is called the *replacement sequence*.
- The replacement sequence is coded as follows:
  1 = High probability
  2 = Low probability
  3 = Very low probability
- If card changing does not remove the fault, refer to the *IBM 3125 Processing Unit, Central Test Manual*, Maintenance Library Manual.

  Note: Before the multiplexer channel is tested, ensure that IOP '9' is functioning correctly.

Diagnostic Techniques and Tests

- Microdiagnostic test programs are designed for error detection and error location.
- The microdiagnostic test programs either directly refer to the failing field replaceable unit (FRU) or they display detailed test results.
- For communication between the system and the user, use both the keyboard and the display unit.
- The automatic system checkout program (ASCP) is stored on the service diskette and checks the reliability of the whole system.
- Online tests (OLTs) check the channel-attached I/O devices.
- Microdiagnostic function tests are stored on the service diskette. Individual tests are available for each system component and are selected by pressing appropriate keys on the keyboard according to instructions given on the display unit.
- Error log and analysis programs are stored on the system diskette.
- The error log program automatically logs all error information every time an error occurs.
- The log analysis program analyzes log information and presents repair instructions on the display unit screen.

Scope Sense

- *Scope Sense 1* and *Scope Sense 2* represent two groups of accessible pins on the SVP link card on the IOP '9' board.
- Suspected signals may be connected to these pins.
- If the display unit is used as a digital oscilloscope (possibly under control of a special microroutine on the system diskette), selected signals can be displayed and compared with other reference signals.
- Signals that are connected to the scope sense pins are logged. This allows additional conditions to be stored for later analysis.

Matrix

- The matrix provides the possibility to run IOP '9' under control of a string of SVP SENS and CTRL operations.

For further information, refer to *IBM 3125 Processing Unit, Input/Output Processor,* Maintenance Library Manual, Order No. SY33-1063.

MPX Microprogram Error Routines

At numerous points the MPX microprogram checks for error conditions; if an error condition is active, a branch to an error routine is performed.

Each error routine starts with loading of an error number; this error number exactly defines the type of error and the point at which the error occurred in the microprogram. According to type of error and the different requirements to handle the error condition, the error routines perform the following steps:

Loads error number
Prepares log area
Prepares CSW and ECSW
Sets respective check bit into channel status
Requests interrupt
Stores CSW and ECSW
Sets condition code

MPX Microprogram Error Numbers

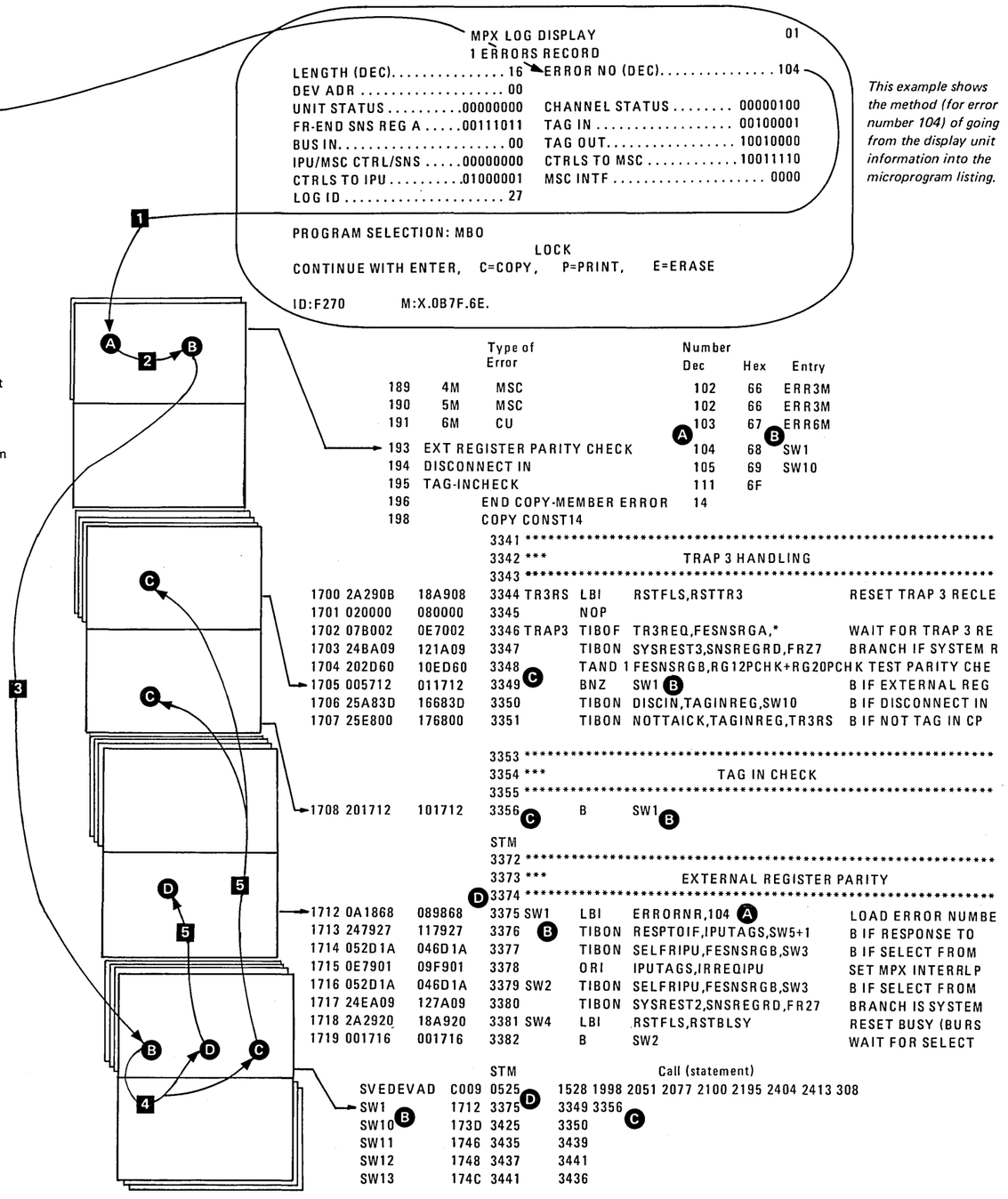
The error numbers, which define the error type and the point at which the error occurred are:

a. Displayed on the screen
b. Listed at the beginning of the microprogram listing.

The error number is important information for log analysis.

The way to find a point within the microprogram listing from the indicated error number is as follows:

1. Look up the error number (A) in the first pages of the microprogram listing.
2. In connection with the error number:
   Type of error, and
   Entry label are found (B)
3. Look up the entry label (B) in the cross reference list at the end of the microprogram listing.
4. In connection with the entry label CALL (C) is found. CALL defines the statement number of the microinstruction(s) from where a branch to the error routine is performed.
   Besides the CALL information, a location count and statement number (D) of the entry label is found. The statement number of the entry label shows in the microprogram listing the location of the first instruction of the error routine.
5. Look up the statement number (C) or (D) in the microprogram listing. These statement numbers either point directly (D) to the error routine, or point to the microinstruction from where a branch to the error routine is performed (C).



This example shows the method (for error number 104) of going from the display unit information into the microprogram listing.

Chapter 7. Reference Information

Abbreviations and Glossary

A

adr	address
addr	address
ADI	address in
ADO	address out
ASCP	automatic system checkout program
aux	auxiliary

B

BC	basic control mode
BFR	buffer
burst mode	The mode whereby a device remains connected to the multiplexer channel for the transfer of the whole record, from first to last byte, without interruption
bus in	That part of the standard interface which transfers data to the channel
bus out	That part of the standard interface which transfers data to the device
byte mode	The mode whereby a device is disconnected from the multiplexer channel after each byte or a number of bytes have been transferred

C

CAW	channel address word
CC	chain command
CC	condition code
CCL	chain control line
CCW	channel command word
CD	chain data
CE	channel end
Ch	channel
ChE	channel end
CIO	clear I/O
cmnd	command
CMO	command out
com reg	command register
command	An operation, such as read, that is to be executed by the I/O device
control command	see "Immediate Command"
CPU	Central processing unit, represented by the IPU, MSC, and SVP
CSW	channel status word
CTM	Central Test Manual
ctrl	control
CU	control unit

D

DE	device end
DFT	diagnostic function test

E

EC	extended control
ECSW	extended CSW
ending status	The status that is presented, after an operation has been executed, to show the state of the control unit and device
ext	external
ext reg	external register
ext in bus	The bus between the multiplexer channel and the IOP
external register	The circuits that link the multiplexer channel to the IOP

F

FL	flip latch

H

HDV	halt device
HIO	halt I/O
HO	hold out

I

IAR	indirect address register
ID	identifier
IDA	indirect data addressing
immediate command	The command that presents channel end with initial status
initial selection	The selection of a control unit before an operation is executed
initial status	The status that is presented after initial selection, to show the state of the control unit and device before an operation is executed
int	internal
I/O	input/output
IOP	Input/Output processor. This device links the multiplexer channel to the CPU
IPU	instruction processing unit
irpt	interrupt

K

KB	keyboard

L

LCL	limited channel logout
log	Information, pertinent to error conditions, that is stored in a reserved area
LS	local storage

M

MPX	multiplexer channel
MSC	main storage controller
MSC-LS	MSC-local storage
multiplex mode	A means of transferring records to or from low-speed I/O devices on the multiplexer channel, by interleaving bytes of data. The multiplexer channel sustains simultaneous I/O operations on several subchannels. Bytes of data are interleaved and then routed to or from the selected I/O devices, or to and from the desired locations in main storage.

N

nonshared UCW	A subchannel that serves a control unit to which only one device is connected

O

OCL	octopus control line
OP	operation
OPI	operation in
OPO	operation out

P

PC	parity check
pending interrupt	An interrupt that is requested but not accepted. With a channel end interrupt status is held in the channel; with a device end interrupt status is held in the control unit. As long as an interrupt is pending, the channel or control unit holding the stacked status indicates "interrupt pending" to any subsequent operation. See also "Ending Sequence" on page 1-060

PG	parity generation
POR	power on reset
primary interrupt	A normal channel-end interrupt
PSW	program status word

R

rec	receiver
reg	register
register	A circuit that can store information
req	request
reselection	The selection of a control unit and device during an operation when the multiplexer channel is working in byte mode
RQI	request in

S

secondary interrupt	A normal device-end interrupt
shared UCW	A subchannel that serves a control unit to which more than one device is connected
sel	select
SIO	start I/O
SIOF	start I/O fast release
SLD	simplified logic diagram
SLI	select in
SLO	select out
SPO	suppress out
stacked status	A status that is kept in the control unit until the channel reselects the I/O device to fetch the status
standard interface	Standardized lines to which I/O devices, with their control units, are connected. The standard interface consists of bus in, bus out, tag in, and tag out lines
std	standard
std intf	standard interface
STI	status in
STIDC	store channel identifier
subchannel	see UCW
SVI	service in
SVO	service out
SVP	service processor

T

tag in	control lines used to define bus in
tag out	control lines used to define bus out
TCH	test channel
TIC	transfer in channel
TIO	test I/O
trap bit	A bit that is ORed with the link portion of an index word. The changed index word causes a jump from one microprogram routine to another

U

UCW	Unit control word, holds control information that is necessary to run a device, UCWs are also called subchannels
UCW buffer	Buffer or storage, used to store 12 out of the 20 bytes of each UCW

W

waiting interrupt	see "Pending Interrupt"

Index

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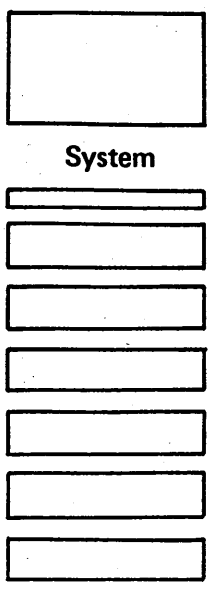

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