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**Systems**

**A Guide to the IBM 4381  
Processor**

## **Systems**

# **A Guide to the IBM 4381 Processor**

This guide presents hardware, I/O device, programming systems, and other pertinent information describing the significant new features and advantages of the IBM 4381 Processor. Knowledge of System/370 or 4300 hardware and I/O devices is assumed. The content of the guide is intended to acquaint the reader with the 4381 Processor and to be of benefit in planning for its installation.

The IBM logo, consisting of the letters "IBM" in a bold, sans-serif font, with horizontal lines through the letters.

### **Third Edition (April 1986)**

This edition is a major revision obsoleting GC20-2021-1. It discusses 4381 Processor Model Groups 11, 12, 13, and 14. New and changed information is indicated by a vertical rule in the left margin.

This guide is intended for planning purposes only. It will be updated from time to time; however, the readers should remember that the authoritative sources of system information are the system library publications for the 4381 Processor, its associated components and its programming support. These publications will first reflect any changes.

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## Preface

This publication is designed for readers who are knowledgeable about System/370 architecture (as implemented in a System/370 or 4300 processor), and 4300/System/370 channels, I/O devices, and programming systems. Features of 4381 Processor model groups that are like the same features in 4341 Processors are identified, and only those hardware and programming systems features of 4381 Processors that are different from those of 4341 Processors are described in detail. Compatibility among the architectures implemented in 4381, other 4300, and System/370 processors and their programming systems support is also discussed.

Information about the currently available 4381 model groups (11, 12, 13, and 14) and the withdrawn model groups (1, 2, and 3) is given in this guide.



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## Section 01: Highlights

The 4381 Processor, available in four model groups, is an intermediate-scale, general purpose processor that is compatible with System/370, other 4300, and 30XX processors. It implements System/370 architecture (as in System/370, 4300, and 30XX processors) and System/370 extended architecture (as in 308X and 3090 processors).

Model Groups 11, 12, 13, and 14 of the 4381 Processor, which offer a wide range of performance, are provided. Model Group 11, 12, and 13 4381 Processor units are uniprocessors containing one instruction execution function. The Model Group 14 4381 Processor unit is a dual processor that contains two instruction execution functions each of which has its own channels. The Model Group 14 processor unit operates as a tightly coupled multiprocessing configuration under the control of one operating system in which processor storage is shared.

Field upgrades of 4381 Processor model groups is supported. A 4381 Model Group 11 Processor can be field upgraded to a 4381 Model Group 12 Processor, a 4381 Model Group 12 can be field upgraded to a 4381 Model Group 13, and a 4381 Model Group 13 can be field upgraded to a 4381 Model Group 14. This support provides significant performance growth. The 4381 Model Group 14 has an internal throughput rate of up to 4.9 times that of a 4381 Model Group 11 for commercial processing and of up to 5.4 times that of a 4381 Model Group 11 for scientific processing.

Model Groups 11 through 14 of the 4381 Processor offer improved price performance relative to Model Groups 1, 2, and 3 of the 4381 Processor, which are withdrawn from marketing, as are model upgrades within these withdrawn model groups. However, optional features, including processor storage upgrades, can be installed in 4381 Model Group 1, 2, and 3 Processors. In addition, these withdrawn model groups can be field upgraded to the current 4381 model groups as follows: 4381 Model Group 1 to a 4381 Model Group 12 or 13, 4381 Model Group 2 to a 4381 Model Group 13 or 14, and 4381 Model Group 3 to a 4381 Model Group 14.

The 4381 Processors offer higher internal performance and improved price performance for intermediate system users relative to 4341 Processors. This improved performance is made possible by the use of large-scale integrated technology for logic and processor storage. The logic packaging and cooling designs implemented in 4381 Processors provide increased logic density without the need for water cooling.

The 4381 Processors support the range of commercial and engineering/scientific data processing capabilities offered by System/370, 4300, and 30XX processors, as well as the advanced functions provided by System/370 and System/370 extended architectures.

The 4381 Processor Model Group 11 is a logical growth processor for System/370 processors (such as Models 135 to 148) and smaller 4341 Processors. Model Groups 12, 13, and 14 of the 4381 Processor provide a growth path for users of larger 4341 Processor model groups, System/370 Models 155 to 168, and 303X processors.

Relative to 4341 Processors, 4381 Processors offer intermediate system users increased internal performance and channel performance; improved price performance; reliability, availability, and serviceability improvements; hardware and programming systems compatibility; System/370 extended architecture advantages; and a wide range of operating system support.

The 4381 Processors can be utilized in decentralized and distributed processing environments that require higher internal performance and more channel capability than is provided by 4341 Processors. They can also be used in 30XX installations to support application offloading.

The 4381 Processors are particularly well suited to handle engineering/scientific applications, such as CAD/CAM, graphics, and problem solving. The performance of floating-point and binary multiply operations in 4381 Processors is significantly improved. Standard engineering/scientific assist features can be used to further improve floating-point arithmetic performance for selected functions.

The 4381 Processors operate with a broad spectrum of IBM products that support engineering/scientific applications, including the 3251 Display Station and 5080 Graphics System, 3838 Array Processor, 7350 Image Processing System, Series/1 processors, and IBM personal computers. The 4381 Processors can also be used with the IBM Device Attachment Control Unit and 7171 ASCII Device Attachment Control Unit to implement engineering/scientific applications that require the use of non-IBM devices. The IBM 4994 ASCII Device Control Unit can be channel-attached to 4381 Processors. The 3044 Fiber Optic Channel Extender Link can be used to extend the distance between terminals/devices and the 4381 Processor (up to two kilometers) while providing near local terminal response time.

System/370 extended architecture, which is implemented in 308X and 3090 processors, is also implemented in 4381 Processors, which are supported by the MVS/Extended Architecture (MVS/XA) operating system. Therefore, a 4381 Processor can be used for MVS/XA testing in a 308X or 3090 installation or as the entry MVS/XA processor in installations that expect growth to a 308X or 3090 processor and MVS/XA.

The 4381 Processors have extensive operating system support. When operating with System/370 architecture in effect (in System/370 mode), 4381 Processors are supported by the same operating systems as 4341 Processors operating in System/370 mode. When operating with System/370 extended architecture in effect (in System/370 extended architecture mode), 4381 Processors are supported by the same operating systems as 308X and 3090 processors operating in System/370 extended architecture mode.

Model Groups 11, 12, and 13 of the 4381 Processor operating in System/370 mode are supported by the following IBM-supplied virtual storage programming systems (which also support 4381 Processor Model Groups 1 and 2):

- Disk Operating System/Virtual Storage Extended (DOS/VSE) with VSE/Advanced Functions as of Release 1.3.5 (the VSE System) or VSE/System Package (VSE/SP) as of Release 1.3.5
- Operating System/Virtual Storage 1 (OS/VS1) Release 7 with OS/VS1 Basic Programming Extensions Release 4
- Operating System/Virtual Storage 2 Multiple Virtual Storage (OS/VS2 MVS) Release 3.8 with an MVS/System Product (MVS/SP) Version 1 Release 3.3 or 3.5 program product (MVS/System Product-JES2 or MVS/System Product-JES3) installed and the appropriate PTF applied. This version of MVS is MVS/370 (MVS with MVS/SP Version 1).
- Virtual Machine/370 (VM/370) Release 6 with VM/System Product (VM/SP) Release 3 or later and without or with VM/SP High Performance Option Release 3.2 or later. VM/SP High Performance Option is required to support more than 16Mb of processor storage.
- Virtual Machine/Entry (VM/Entry)
- Airline Control Program/Transaction Processing Facility (ACP/TPF) Version 2.3

Model Groups 11, 12, and 13 of the 4381 Processor operating in System/370 extended architecture mode are supported by the following (which also support 4381 Processor Model Groups 1 and 2):

- MVS Release 3.8 with MVS/SP (MVS/SP-JES2 or MVS/SP-JES3) Version 2 Releases 1.2 and 1.3 and (with the appropriate PTF applied) and MVS/XA Data Facility Product (the MVS/XA operating system)
- Virtual Machine/Extended Architecture (VM/XA) Migration Aid Release 2 or later
- Virtual Machine/Extended Architecture (VM/XA) Systems Facility Release 1

The 4381 Processor Model Group 14 operating in System/370 mode is supported by the following (which also support the 4381 Model Group 3):

- MVS/SP-JES2 or MVS/SP-JES3 Version 1 Releases 3.3 and 3.5
- VM/SP Release 3 or later without or with VM/SP High Performance Option Release 3.4 or later. VM/SP High Performance Option is required to support more than 16Mb of processor storage.

The 4381 Processor Model Group 14 operating in System/370 extended architecture mode is supported by the following (which also support the 4381 Model Group 3):

- MVS/SP-JES2 or MVS/SP-JES3 Version 2 Release 1.1 or 1.3 with the appropriate PTFs applied.

- VM/XA Migration Aid Release 2 or later
- VM/XA Systems Facility Release 1

The hardware facilities of, and I/O devices for, 4381 Processors can most effectively be used by the MVS/370, MVS/XA, and VM/370 operating systems. To aid in the transition from DOS/VSE to MVS/370 with installation of a 4381 Processor, two migration aids are provided (see discussion in Section 70:05). Less effort is required to convert from OS/VS1 to MVS/370 than from DOS/VSE to MVS/370 because of the basic compatibility between the OS/VS1 and OS/VS2 operating systems.

Highlights of 4381 Processor Model Groups 11, 12, 13, and 14 are as follows:

- Upward compatibility with 4300 System/370 mode, System/370, and 30XX architecture and programming systems has been maintained in 4381 Processors through implementation of the System/370 mode of processor operation. This mode provides compatibility for 4300 System/370 mode, System/370, and 30XX control programs and problem programs. Problem programs that operate in 4341 Processors under a DOS/VSE ECPS:VSE mode supervisor can also operate in a 4381 Processor under a DOS/VSE System/370 mode supervisor if they are not processor- or time-dependent. The ECPS:VSE mode implemented in 4341 Processors is not implemented in 4381 Processors.

The System/370 extended architecture mode of operation, not provided in 4341 Processors, is also implemented in 4381 Processors. This mode provides compatibility for most 4300, 30XX, and System/370 problem programs and most MVS/370 subsystems but requires a control program with System/370 extended architecture support, such as MVS/XA.

- The following are instruction processing function features of 4381 Processors.

Instruction processing function logic is implemented in large-scale integrated technology. Logic chips (704-circuit) with faster circuit speeds than the 704-circuit chip used in most 4300 Processors are used in 4381 Processors. However, the logic packaging and cooling technique implemented in 4381 Processors significantly increase the logic circuit density on a logic board without the need for water cooling. (See Section 10:05 for a detailed logic technology discussion.)

Implementation of a System/370 mode and a System/370 extended architecture (System/370-XA) mode is standard. The System/370 architecture implemented for System/370 mode operations includes nearly all the extensions implemented in large-scale processors, such as the 308X and 3090.

System/370 extended architecture is System/370 architecture with certain changes and additions. The major new functions provided by this architecture are 31-bit addressing and dynamic channel subsystem architecture. The 31-bit addressing capability enables two gigabytes (over 2 billion bytes) of virtual storage and real storage to be addressed, versus a maximum of over 16 million bytes for the 24-bit addressing supported by System/370 architecture. A bimodal operation is supported that permits programs that use 24-bit addressing and programs that use 31-bit addressing to operate concurrently when System/370-XA mode is in effect.

The dynamic channel subsystem architecture eliminates channel addressing, supports queuing of all I/O requests, provides channel path selection for all requested I/O operations in hardware, and supports an expanded I/O interruption mechanism and extended I/O device addressing.

The mode in which the 4381 Processor is to operate is determined by the operator at initial microcode load (IML) time. The mode selected remains in effect until another IML is performed and causes the System/370 mode or System/370-XA mode microcode to be used for this IML.

The cycle time of 4381 Model Group 11 and 12 Processors is 68 nanoseconds. For 4381 Model Groups 13 and 14, cycle time is 56 nanoseconds.

The instruction processing function design provides increased instruction execution performance. Instruction prefetching is implemented that results in the overlap of instruction fetching with instruction execution during sequential instruction processing. In addition, an eight-byte-wide arithmetic logic unit is used that enhances the performance of decimal and floating-point operations.

Improvements in the number of functions performed during the instruction cycle of 4381 instruction execution (like those in 4341 Processors) result in the faster execution of many other instructions, most of which are among the more frequently used instructions.

The standard instruction set for 4381 System/370 mode of operation provides decimal, binary, and floating-point arithmetic operations (including the extended floating-point format that provides the equivalent of up to 34 decimal digits). For 4381 Model Groups 11, 12, and 13, it consists of the entire instruction set defined for System/370 except for direct control and RESUME I/O instructions and those associated with multiprocessing (as discussed in Section 10:10). For the 4381 Model Group 14, multiprocessing instructions are also standard.

The standard instruction set for 4381 System/370-XA mode of operation includes all the instructions defined for System/370 extended architecture. All the semiprivileged and all the nonprivileged instructions in System/370 architecture are also defined for System/370 extended architecture but differences exist in the set of privileged instructions supported by the two architectures (see Section 10:10).

Three engineering/scientific assists are provided for 4381 Processors. The Multiply and Add Facility is standard in 4381 Model Groups 11, 12, 13, and 14. It is designed to improve the performance of certain mathematical computations, such as matrix inversion, decomposition, and multiplication. These computations are used, for example, in finite element analysis, linear programming, and statistical analysis. This feature supports only long-format (64-bit) floating-point numbers and can provide a reduction in instruction processing function busy time of up to 35 percent for the instructions replaced by the MULTIPLY AND ADD instruction (see Section 20:05).

The Square Root Facility is standard in 4381 Model Groups 11, 12, 13, and 14 to improve the performance of square root operations involving long- or short-precision floating-point arithmetic.

The Mathematical Function Facility (not implemented in 4341 Processors) is standard in 4381 Model Group 12, 13, and 14 Processors and provides a group of eight register-to-register floating-point instructions that perform elementary mathematical functions. The supported functions are exponentiation and natural and common logarithms. The instructions support short and long precision for the two operands involved (see Section 20:05). This facility reduces processor busy time by up to 65 percent for the assisted functions. It permits selected scientific subroutines to be executed faster than with conventional programming (FORTRAN subroutines).

Timing and debugging features like those in System/370, 30XX, and other 4300 Processors (3.3-ms-resolution interval timer, time-of-day clock, CPU timer, clock comparator, monitoring feature, and program event recording) are standard in 4381 Processors. The time-of-day clock and CPU timer have a one-microsecond resolution.

The standard byte-oriented operands facility permits byte boundary alignment for the operands of nonprivileged instructions, making it unnecessary to add padding bytes within records or to blocked records to align fixed- or floating-point data. In 4381 Processors, minimal performance degradation results from the use of unaligned data.

Functions of the System/370 Extended Facility/Feature for 30XX Processors are standard in 4381 Processors. These facilities are low address protection (to protect the contents of locations 0 to 511 from accidental modification), the TEST PROTECTION and INVALIDATE PAGE TABLE ENTRY instructions (for control program use), the common segment facility (to improve address translation performance for MVS and VM/370 environments), MVS-dependent instructions (ECPS:MVS feature in 4381 Processors), and Virtual Machine Extended Facility Assist.

The facilities provided by the 3033 Extension feature for 30XX Processors are standard in 4381 Processors. The Dual Address Space Facility for both modes (which improves the performance of MVS/SP Cross Memory Services), START I/O FAST RELEASE instruction queuing for System/370 mode only (which is basic to the System/370-XA mode channel subsystem), and two MVS assists (included in the 4381 ECPS:MVS feature) are implemented in 4381 Processors. The suspend and resume facility provided by the 3033 Extension feature is not implemented for 4381 System/370 mode of operation but a comparable function is basic to the channel subsystem defined for System/370-XA mode.

Dynamic address translation and channel indirect data addressing features to support a virtual storage and/or virtual machine environment are standard. For System/370 mode (which uses 24-bit addressing), one virtual storage of 16,777,216 bytes (16Mb) maximum or multiple virtual storages up to 16M-bytes each can be supported. For System/370-XA mode (which uses 31-bit addressing), one virtual storage of up to 2,147,483,648 bytes (2 gigabytes) or multiple virtual storages of up to 2 gigabytes each can be supported.

A segment protection facility (not provided for 4341 Processors) that provides the ability to prevent stores to protected virtual storage segments is standard for System/370 mode. For System/370-XA mode, a page protection facility is

provided instead of the segment protection facility. Page protection can be used to prevent any writing in protected 4K pages of virtual storage.

A VM/370 hardware assist function (ECPS:VM/370) and an MVS hardware assist facility (ECPS:MVS) are standard in 4381 Processors. ECPS:VM/370 and ECPS:MVS can be used concurrently to improve performance when MVS/SP Version 1 executes in a virtual machine under the control of VM/370 with the VM/System Product.

ECPS:VM/370 consists of the Virtual Machine Assist, Control Program Assist, Expanded Virtual Machine Assist, Virtual Interval Timer Assist, and Shadow-Table Bypass Assist components. It can be used only when System/370 mode is in effect.

ECPS:MVS consists of 13 privileged instructions and the page fault assist function, all of which are operative during System/370 mode operations. Six of the 13 instructions are operative for System/370-XA mode operations. The standard Virtual Machine Extended Facility Assist enables the ECPS:MVS instructions to be executed directly by an MVS virtual machine to improve performance.

Preferred Machine Assist (not provided for 4341 Processors) is standard in 4381 Processors and can be used only during System/370 mode operations. It is designed to improve the performance of MVS/SP Version 1 running in a preferred virtual machine.

Instruction retry is standard to attempt to correct errors that occur during instruction execution without programming assistance. For certain hardware facilities (reloadable control storage, channel buffers, and the high-speed buffer and its swap buffer), the instruction retry facility provides automatic hardware reconfiguration to assign spare storage when a retry does not correct an error. The reconfiguration facility permits continued system operation, without performance degradation in some cases. Maintenance is performed when reconfiguration is no longer possible.

- The following are significant storage features of 4381 Processors.

All storage in a 4381 Processor—processor, control, high-speed buffer, and local—is implemented using monolithic technology. The technology used for processor storage in 4381 Processors provides much denser storage chips (64K bits per chip as in 4341 Processors and a 256K-bit chip for processor storage above 16Mb) than is used in System/370, 303X, or 308X processors (2K, 4K, or 16K bits per chip).

A two-level storage system is implemented, consisting of large processor storage used as backing storage for a smaller high-speed buffer storage. The instruction processing function works mostly with the high-speed buffer so that the effective processor storage cycle is a fraction of the actual processor storage cycle.

4K bytes for a 4381 Model Group 11, 32K bytes for a 4381 Model Group 12, and 64K bytes for a Model Group 13 of high-speed buffer storage (where  $K=1024$ ) are standard. The full buffer size is used when the page size in effect is 4K bytes. When page size is 2K bytes in a 4381 Model Group 11 or 12, only half of the high-speed buffer is used. A doubleword of data is fetched

from the buffer in 68 nanoseconds and stored in the buffer in 102 nanoseconds for 4381 Model Groups 11 and 12. For a 4381 Model Group 13, 56 or 84 nanoseconds are required for a fetch or store, respectively.

For the 4381 Model Group 14, each of the two instruction processing functions has its own dedicated 64K-byte high-speed buffer as a standard feature. These two high-speed buffers operate using 4K-byte pages only. Facilities for the required high-speed buffer communication in a multiprocessing environment are implemented in the Model Group 14, including buffer-to-buffer data transfer.

4Mb, 8Mb, and 16Mb of processor storage are available for the 4381 Model Group 11 (where  $M=1,048,576$ ). For 4381 Model Group 12 and 13 Processors, 8Mb, 16Mb, 24Mb, and 32Mb are available. A Model Group 14 can have 16Mb, 24Mb, or 32Mb of processor storage. Store and fetch protection and reference and change recording are standard. Store and fetch protection are provided on a 2Kb basis (one key for each 2Kb) for 4381 processors with up to 16Mb installed. For 4381 processors with more than 16Mb installed, store and fetch protection are provided on a 4Kb basis.

A portion of highest addressed installed processor storage in a 4381 Processor will not be accessible to programs, as in 4341 Processors. The amount of unavailable processor storage for 4381 Processors (called auxiliary storage) is a minimum of 64Kb (104Kb for the Model Group 14) for System/370 mode of operation for the minimum number of UCWs (128) defined. For System/370-XA mode, a minimum of 112Kb (220Kb for the Model Group 14) of auxiliary storage is required for zero subchannels and 128 control units defined.

Reloadable control storage to contain all the microcode required by the instruction processing function of 4381 Processors is standard. Use of writable, instead of read-only, control storage offers the advantages of improved system serviceability and ease of optional feature and engineering change installation.

The TEST BLOCK instruction (not implemented in 4341 Processors) is provided to enable the control program to determine which 4Kb blocks of processor storage and/or their associated one or two storage protect keys are unusable because of uncorrectable errors. Known unusable blocks and keys are saved across power-offs. This instruction can also be used for processor storage validation.

The TEST BLOCK instruction enables the operating system to delete unusable 4Kb blocks from its list of assignable page frames and prevents abnormal program terminations that could result from the uncorrectable storage errors.

Error checking and correction (ECC) hardware is standard. It automatically corrects all single-bit processor storage errors, and detects but does not correct all double-bit and most multiple-bit errors. Correction of double-bit errors that consist of one solid and one intermittent error (which is not implemented in 4341 Processors) is also provided via microcode (see discussion in Section 60:10).

- The following channel features are provided for 4381 Processors.

Two channel groups are available for Model Groups 11, 12, and 13. The standard channel group consists of one byte multiplexer and five block multiplexer channels addressed 0 through 5. The optional channel group consists of six block multiplexer channels addressed 6 through B. Block multiplexer channel 5 in the standard channel group can be configured as a byte multiplexer instead of as a block multiplexer channel.

For the 4381 Model Group 14, one channel group consisting of one byte multiplexer channel (0) and five block multiplexer channels (1 through 5) is standard for each of the two instruction processing functions. The fifth block multiplexer channel in each channel group can be configured as a byte multiplexer channel. Optionally, one additional channel group, which provides three additional block multiplexer channels for each channel group (a total of six additional channels) can be installed.

Functionally, a byte multiplexer channel for a 4381 Processor is equivalent to that for System/370, 30XX, and other 4300 processors. The standard (channel 0) and optional (channel 5) byte multiplexer channels in Model Groups 11, 12, and 13 each have a 24Kb/sec maximum data rate (28Kb/sec for the Model Group 14) for one-byte transfer operations for byte mode operations. Unbuffered burst mode I/O devices cannot be attached to the byte multiplexer channels in a 4381 Processor.

Functionally, a block multiplexer channel in a 4381 Processor is equivalent to that for System/370, 30XX, and 4300 processors. A block multiplexer channel in 4381 Processors can also operate in selector channel mode.

The data streaming mode of channel operation that is provided for 4341 and 30XX Processors is standard for all the block multiplexer channels in a 4381 Processor. Data streaming mode enables certain 4381 channels to handle faster data rates (up to 3Mb/sec) over a longer channel-to-control unit cable length for attached control units that are also capable of operating in data streaming mode (see discussion in Section 20:20). Both data streaming and nonstreaming devices can be attached to the block multiplexer channels in a 4381 Processor.

For the standard channel group in a 4381 Model Group 11, 12, or 13, the maximum aggregate data rate is 14 Mb/sec. For the optional channel group in a Model Group 11, the maximum aggregate data rate is 8Mb/sec, providing a 22Mb/sec maximum aggregate for eleven block multiplexer channels. For a Model Group 12, the optional channel group has a maximum aggregate data rate of 10Mb/sec, providing a 24Mb/sec maximum aggregate for the eleven block multiplexer channels. The maximum aggregate data rate for the optional channel group in a Model Group 13 is 16Mb/sec, with a 30Mb/sec maximum aggregate data rate for eleven block multiplexer channels.

For the Model Group 14, a maximum aggregate data rate of 30Mb/sec for the ten block multiplexer channels (15Mb/sec for each channel group) is possible. The maximum aggregate data rate for 16 block multiplexer channels is 36Mb/sec (18Mb/sec for each eight-channel group).

Channels with data rates of up to 3 Mb/sec and the block multiplexing capability support attachment to the 4381 Processor of 3380, 3375, 3370,

3330-series, 3340/3344, and 3350 direct access storage. These disk devices have rotational position sensing capability and can be used only with block multiplexer channels.

Optionally, one Channel-to-Channel Adapter can be installed in a 4381 Processor (any model group) and attached to any block multiplexer channel. The adapter can be used to connect a channel in a 4381 Processor to a channel in a System/360, System/370, 30XX, 4321, 4331, 4341, 4361, or another 4381 Processor. Alternatively, the 3088 Multisystem Channel Communication Unit can be used to interconnect the 4381 Processor with certain other processors via channels.

The fast release function of the START I/O FAST RELEASE (SIOF) instruction (implemented only in Model Group 12 4341 Processors) and queuing of SIOF instructions (not implemented in 4341 Processors) are standard features in 4381 Processors. These functions are designed to reduce I/O processing time.

- A 3205 Color Display Console, or a 3278 Model 2A Display Console or 3279 Model 2C Color Display Console equipped with an operator console keyboard and operator control panel feature is required as the operator console for a 4381 Processor. Display mode and (for System/370 mode only) a printer-keyboard mode are standard. The display console natively attaches to 4381 Processors. The display console is used for manual operations, operator-to-operating system communication, and by the customer engineer to perform diagnostic functions.

Up to three displays and/or printers can be natively attached to a 4381 Processor in addition to the required 3205, 3278 Model 2A, or 3279 Model 2C console. The additional three units can be 3205 Color Display Consoles, 3278 Model 2A Display Consoles, 3279 Color Display Consoles Model 2C, 3268 Model 2 Printers, 3268 Model 2C Color Printers, and/or 3287 Printers Models 1, 2, 1C, and/or 2C in any combination with the restriction that 3205 displays cannot be installed together with 3278 Model 2A or 3279 Model 2C displays. The additional displays can be used as alternate and/or additional consoles.

The 3287 or 3268 Printer can be used for hard-copy backup of an operator console that operates in display mode. Models 1C and 2C of the 3287 and the 3268 Model 2C provide color printing. A printer is recommended for hard-copy output when the display console operates in printer-keyboard mode.

The Remote Operator Console Facility (ROCF), a no-charge specify option that requires the Remote Support Facility, gives an operator at a host location the ability to dial up and control a powered-on remote 4381 Processor using a 3275 Display Terminal or an emulated 3275 attached to a host processor. Host processor program support for ROCF is provided by MVS/370, MVS/XA, and VM/370 with the appropriate program products installed (see discussion in Section 40:15).

- I/O devices that attach to 4341 Processors and that are available from IBM will also attach to 4381 Processors.
- The Device Attachment Control Unit (DACU) can be attached to a block multiplexer channel in 4381 Processors. The DACU provides two commonly used industry interfaces for the attachment of non-IBM I/O devices: UNIBUS

(a registered trademark of the Digital Equipment Corporation), which provides a parallel direct memory access (DMA) interface, and EIA RS-232C, which is an industry standard serial communication interface. The DACU permits attachment of a wide variety of non-IBM I/O devices, such as plotters, sensors, graphic devices, laboratory instruments, and minicomputers. This control unit makes a 4381 Processor suitable for a variety of engineering and scientific applications.

- The large-scale integrated technology implemented in 4381 Processors for most logic and all processor storage provides higher internal performance, increased reliability, and compact processor unit design. The module-on-board logic packaging eliminates one entire level of packaging (logic cards), and the impingement cooling technique assures adequate cooling of the high-density logic modules using only room-temperature air as the cooling medium. (See technology discussion in Section 10:05.)
- The power system hardware in 4381 Processors is totally different from the power hardware used in most 4341 Processors. The 4381 power hardware increases reliability, reduces space requirements, and aids serviceability. Improvements in the fault-locating ability and the usability of power diagnostics have also been made.
- Extensive hardware and programming systems error recovery and repair features for 4381 Processor hardware errors are provided to improve system availability and serviceability. These features include enhanced facilities implemented in other 4300 Processors, such as automatic diagnosis of logout data after a hardware error occurs to generate a reference code that identifies the field-replaceable unit or the procedure to follow to attempt to locate the malfunction. Additional recovery facilities (such as double-bit error correction and hardware reconfiguration) are implemented.

The Problem Analysis facility is provided for 4381 Processors. This facility is designed to be used by the operator to aid in problem determination and can result in faster fault isolation and reduced system downtime. It provides usability and functional improvements over the Problem Analysis facility provided for 4341 Processors (see discussion in Section 60:15).

Inquiry into a remote data bank by the on-site customer engineer and remote diagnosis of hardware failures by IBM support center personnel are supported via the recommended, no-charge Remote Support Facility (RSF), which is functionally like RSF for 4341 Processors.

The physical components of a 4381 Processor configuration are a 4381 Processor, an operator console (a 3205 Color Display Console, 3278 Model 2A Display Console, or 3279 Model 2C Color Display Console), and I/O devices. The 4381 Processor, which is air-cooled, is shown in Figure 1 on page 12.

The 4381 Processor unit contains two diskette drives (instead of one as in a 4341 Processor). These drives (shown in Figure 1 on page 12) are easily accessible to the operator and space is provided to the left of the two drives to store diskettes not in use. The second diskette drive is required to support System/370 extended architecture functions and operations and enables more diagnostics (such as Problem Analysis) to be online for ease of use. Two

different operational diskettes (called functional diskette 1 and functional diskette 2) are provided for the two diskette drives.

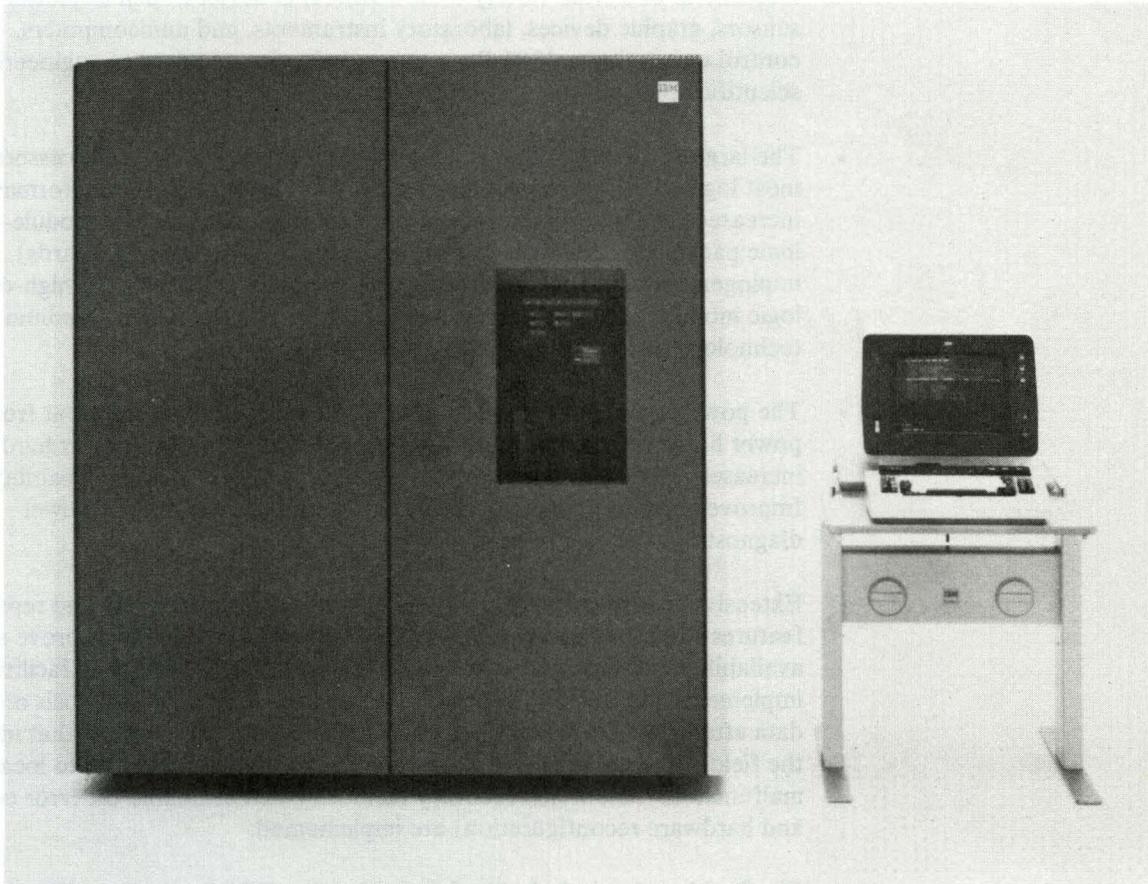


Figure 1. The 4381 Processor and console

While the logical designs of the functional components of a 4381 Processor are very similar to the designs in a 4341 Processor, the physical design and most physical components in a 4381 and 4341 Processor are different.

The logic package, the cooling components, power hardware components, the support processor, the diskette drives, and the Channel-to-Channel Adapter hardware are different in 4381 and 4341 Processors. These differences improve speed and reliability, reduce cost, and/or reduce space requirements. The upright design of the 4381 Processor also reduces space requirements and the 4381 Processor unit is the same size for all 4381 model groups (1 through 3 and 11 through 14). Any 4381 model group can be installed with or without a raised floor and thus can be placed in end-user work areas.

The 4381 Model Group 12 has about twice the number of logic circuits and provides twice the internal performance of the 4341 Model Group 2 but occupies 69% of the floor space, uses 89% of the power, dissipates 83% of the heat, and weighs 84% as much as a 4341 Model Group 2. The 4381 Model Group 11 provides twice the internal performance of the 4341 Model Group 1 but occupies 69% of the floor space, uses 107% of the power, dissipates 99% of the heat, and weighs 95% as much as the 4341 Model Group 1. These comparisons assume a 4341 without a Channel-to-Channel

Adapter, which requires an additional frame in a 4341 Processor but not in a 4381 Processor.

In summary, 4381 Processors offer intermediate system users:

- Improved internal performance, price performance, and channel performance relative to 4341 Processors
- Improved engineering/scientific performance relative to 4341 Processors
- Implementation of nearly all System/370 architecture facilities and all the new facilities of System/370 extended architecture
- Compatibility with other 4300, 30XX, and System/370 processors
- A full range of operating system support for both System/370 and System/370-XA modes
- Improved reliability and availability characteristics and the expanded serviceability functions implemented in 4341 Processors
- Evolutionary logic technology packaging that provides greater logic chip densities with air cooling
- Reduced floor space requirements relative to 4341 Processors
- Four field upgradeable models that provide a wide range of performance and nondisruptive growth

## Section 10: Technology and Architecture

### 10:05 Technology

#### Introduction

The price performance and compact size of the 4381 Processor unit have been achieved in part through the use of large-scale integrated bipolar semiconductor technology for logic chips and large-scale integrated packaging of logic chips. In addition, a 64K-bit and 256K-bit dynamic storage chip are used for processor storage.

Large-scale integrated technology and packaging are utilized to increase logic circuit density. The major benefits of increased circuit density are faster logic speed and higher logic reliability. In addition, logic cost and space requirements are reduced.

The speed of logic circuitry is affected by the distance signals have to travel. The shorter the distance, the less the time it takes for the signals to travel from one circuit to another, and at the same time less power is consumed. The use of less power reduces the total amount of heat generated by the circuitry, which reduces the total amount of cooling required. However, the higher density of circuits concentrates the heat that is generated in a smaller area.

The reliability of logic circuitry is related to the (1) number of circuit interconnections and (2) level of packaging (location and wire length) at which the interconnections occur (which determines the number of times an electrical current must flow between dissimilar materials). External connections (the wiring among circuits) are the least reliable part of logic circuitry. Thus, circuit connections made on a chip are more reliable than those made off a chip. Reductions in the number and length of external connections (those made off the chip via a card or board, for example) improve reliability.

The large-scale integrated (LSI) technology in which the logic in the 4381 Processor is implemented is very similar to the LSI technology implemented in 4341 Processors but provides faster circuit speeds. The packaging of 4381 logic chips on a ceramic substrate is an extension of the packaging used in 4341 Processors and is similar to the packaging used for 308X logic modules; however, fewer chips are placed on a substrate for the 4381 Processor than for the 308X Processor Unit to reduce cooling requirements. The packaging of a logic module

and the cooling process used in 4381 Processors had not been implemented in IBM processors before the 4381.

The multilayer logic board design first used in the 3081 Processor Unit is also used in the 4381 Processor. The logic module packaging and logic module board design for the 4381 Processor eliminate an entire level of packaging, aid logic reliability, and increase logic speed relative to the 4341 implementation. Logic in the 4381 utilizes advanced features that were first used to package logic chips in other 4300 Processors but extends these features to significantly increase the circuit density of a substrate.

Logic wiring in IBM processors other than the 4381, 308X, and 3090 occurs at several levels. First, elementary components (transistors, diodes, and resistors) on a chip are connected to form circuits, which are then interconnected at the chip level. Additional circuit connections are then made at the logic module level (that is, within the substrate) and at the card level. Cards are mounted on boards (card-on-board packaging) and circuit connections among the cards on the same board and among cards on different boards are made via cabling. This design is used in 4300 Processors other than 4381 Processors.

Card-on-board packaging is not used for most of the logic in the 4381 Processor unit. Instead, logic modules are mounted directly on a multilayered board, which provides the ability to interconnect the logic modules on the board via imbedded wiring, thus eliminating most intraboard cabling.

## Logic Chip, Module, and Board Design

The logic chip used in the 4381 Processor unit is 4.57 by 4.57 millimeters (approximately  $3/16$  of an inch square) and contains over 7000 elementary components (resistors, diodes, and transistors). The 7000 elementary components on a chip can be connected to form a maximum of 704 logic circuits.

The logic chip for the 4381 Processor has the same maximum logic circuit capacity (704) as the chip used in other 4300 Processors. However, a slightly different technology than is used for the 704-circuit chip in 4341 Processors is used for the 4381 chip. This technology reduces the size of the transistors on a 4381 chip and more power is used. These differences result in a 4381 chip circuit speed that is 1.15 nanoseconds for 4381 Model Groups 11, 12, 1, 2, and 3 (approximately one-half that of the 4341 Model Group 2 logic chip) and a chip circuit speed of .7 nanoseconds for 4381 Model Groups 13 and 14.

Of the 704 circuits available on a single chip, the average number actually utilized in the logic implemented in the 4381 Processor is 650. The high circuit utilization per chip is made possible in part because three layers of wiring are used for interconnections on the chip itself. A logic chip in the 4381 Processor can contain several feet of wire that interconnects the elementary components and circuits on the chip.

The 4381 logic chips are mounted on a multilayer ceramic substrate that is 64 millimeters (about 2.5 inches) square and 5.5 millimeters (.2 of an inch) thick, which is larger than the ceramic substrate for 4341 Processor logic (50 millimeters by 50 millimeters or approximately 2 inches square) but smaller than the ceramic substrate for the 3081 logic module (90 millimeters, about 3.5 inches, square).

The 64-millimeter (mm) ceramic substrate for the 4381 has 36 chip positions, which compares to 9 positions maximum per 4341 ceramic substrate. On average, 30 logic chips are mounted on a ceramic substrate in a 4381 Processor. The 64-mm substrate, which is called a multichip module (MCM), is shown in Figure 2.

Logic and array chips can be intermixed on the ceramic substrate used in the 4381 logic module. The mixing of logic and array chips on a substrate was first done in 4331 and 4341 Processors. This approach permits arrays to be located closer to the logic that utilizes them and, therefore, increases logic speed.

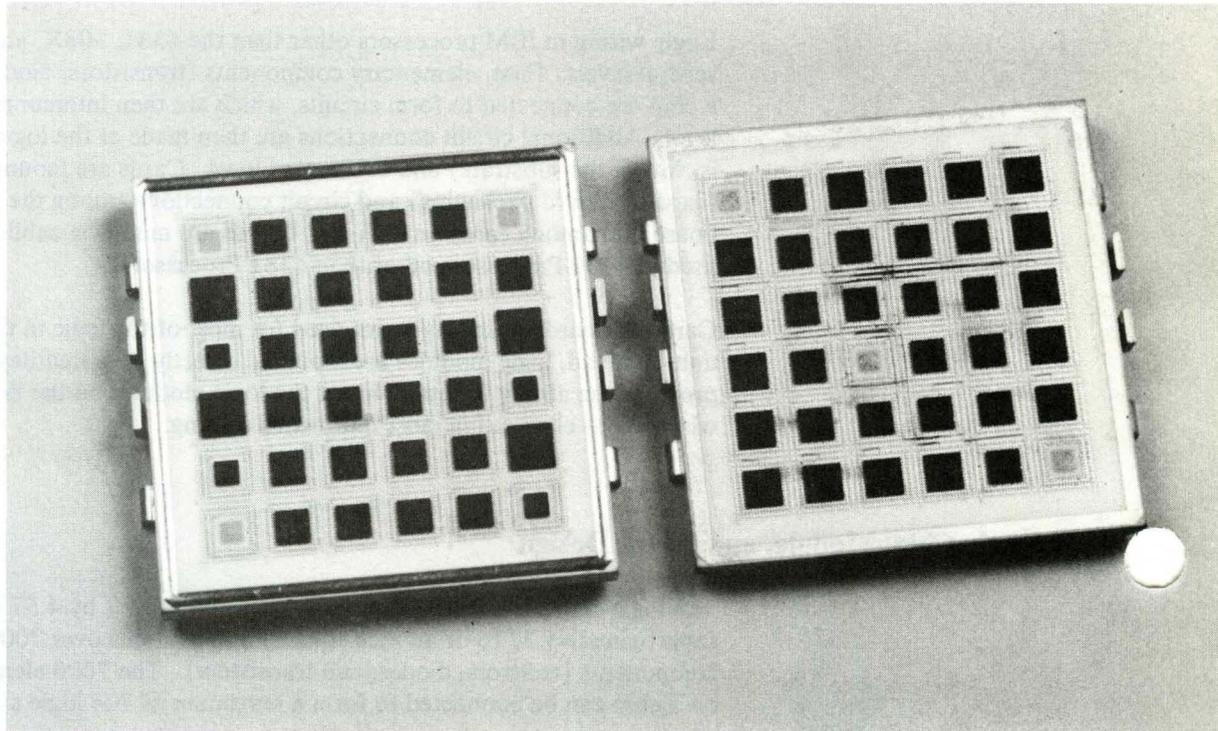


Figure 2. Two 64-mm MCMs

The 4381 ceramic substrate contains from 20 to 32 layers for interconnecting the mounted chips. The ceramic substrate has 882 pins brazed to the bottom of it to provide input/output and power capabilities. This compares with 361 pins in the 50-millimeter logic module in a 4341 Processor.

The MCM is the basic field-replaceable unit (FRU) for 4381 logic. The module (including the attached heat sink used for cooling as described later) is 35 millimeters (about 1.4 inches) high and weighs 250 grams (a little over one-half a pound). An MCM can be quickly and easily removed from the MCM board and replaced with another MCM. Figure 3 on page 17 shows an MCM being hand held.

The advances implemented in the ceramic substrate for 4381 logic can be seen by comparing it with the substrate for 4341 Processors. A maximum of 23 layers is present in the 50-mm ceramic substrate used in 4341 Processor logic. On average, six chips are contained in the 50-mm module.

The MCMs for the 4381 Processor are mounted directly on a multilayer board similar to that used in 308X processors. The MCM board for a 4381 Processor is

700 by 600 millimeters (27.6 by 23.6 inches) in size and 4.6 millimeters (about 1/4 of an inch) thick (the same size as the TCM board in a 308X Processor Unit). The MCM board has 22 module positions and is shown in Figure 4 on page 18. Figure 5 on page 18 shows how MCMs are mounted on the MCM board.

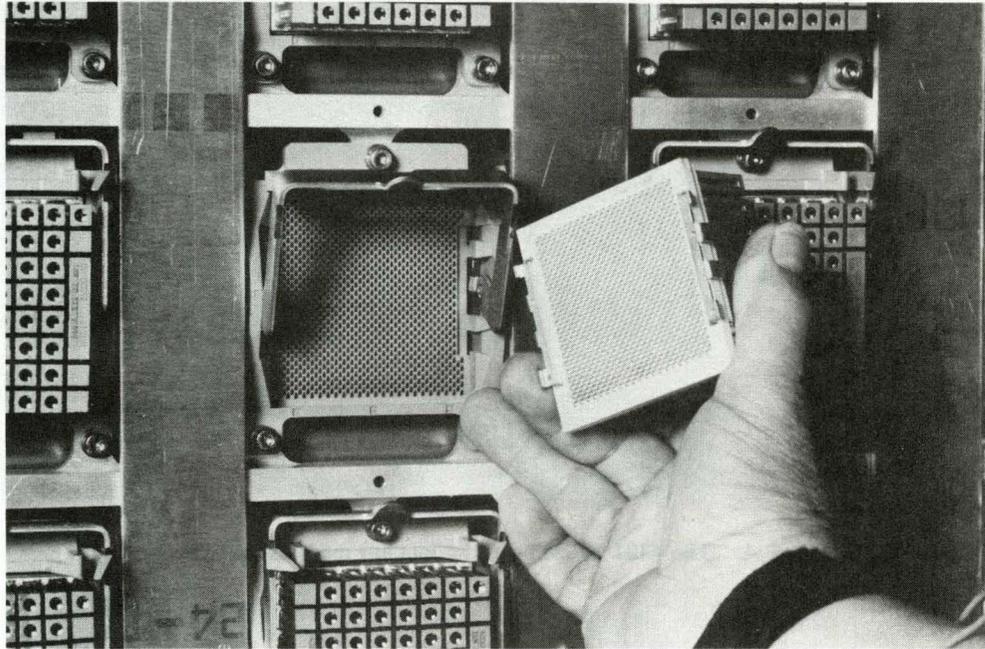


Figure 3. A 64-mm MCM being hand held

The instruction processing logic for 4381 Processor Model Groups 11, 12, and 13 (exclusive of that for the support processor subsystem and some channel functions) is contained in 22 MCMs and these modules are mounted on one MCM board. The 4381 Processor Model Group 14 contains two MCM boards. The fully loaded MCM board weighs 37 kilograms (81.4 pounds). The MCM board has 8 layers for interconnecting the circuits on the MCMs and contains 1435 meters (about 4707 feet) of wiring for circuit interconnections. Figure 6 on page 19 shows the MCM board as it is mounted on its side within the frame of a 4381 Processor.

Since all instruction processing logic is contained on one board in a 4381 Processor Model Group 11, 12, or 13, interboard cabling for logic is eliminated, which increases logic speed and reliability. In the 4341 Processor, two boards are required for logic and 400 cables are used for circuit connections between the two boards. For a 4381 Model Group 14, some cabling between the two MCM boards is required for communication between the two instruction processing functions.

The standard card-on-board approach (a 22-card board) is used for other functional components of the 4381 Processor. There is one processor storage board, one board to support certain channel functions, and two boards for support processor components.

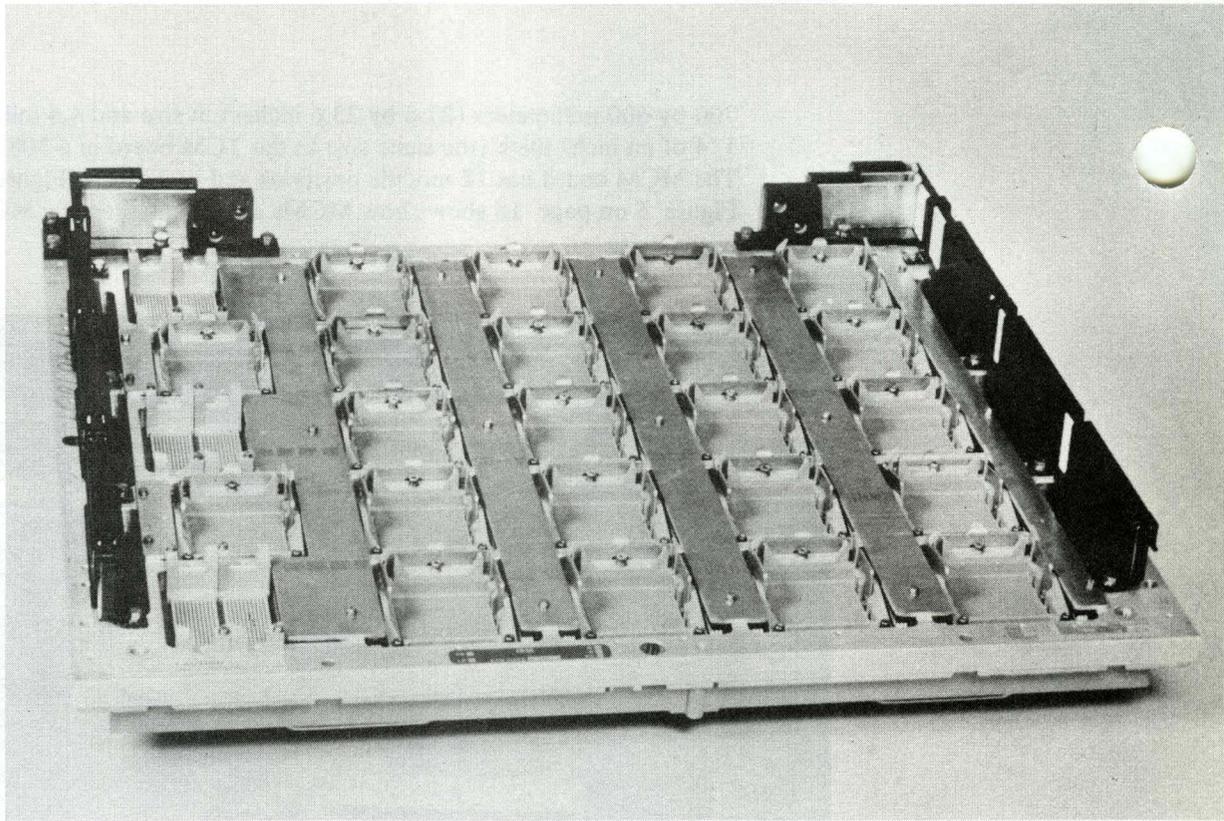


Figure 4. The 4381 MCM board without any modules mounted

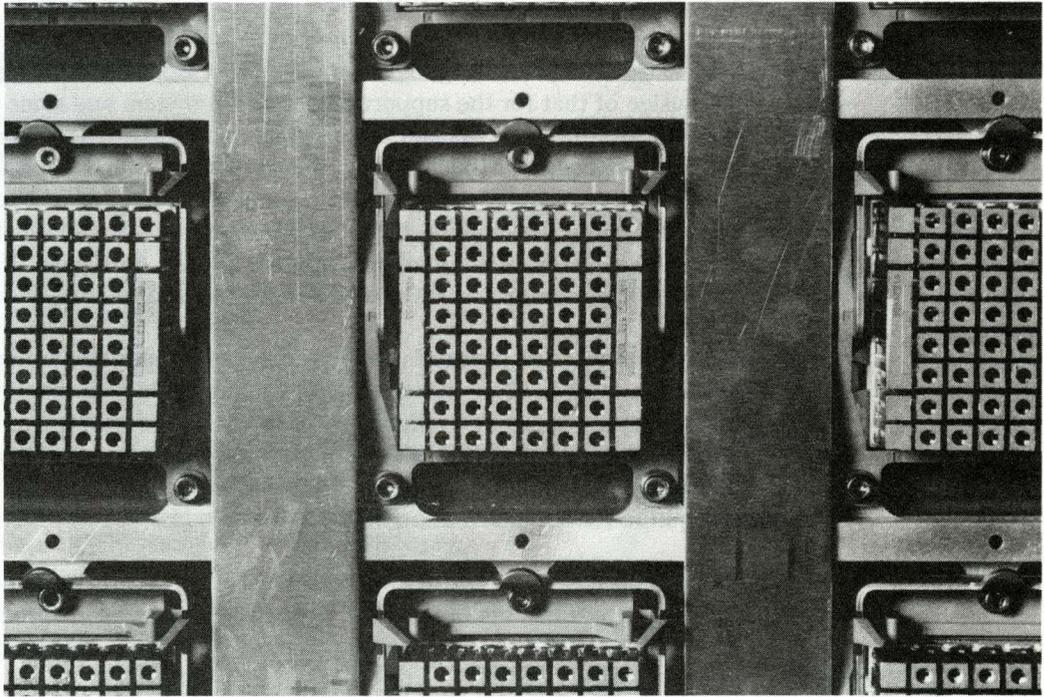


Figure 5. 64-mm MCMs mounted on the MCM board

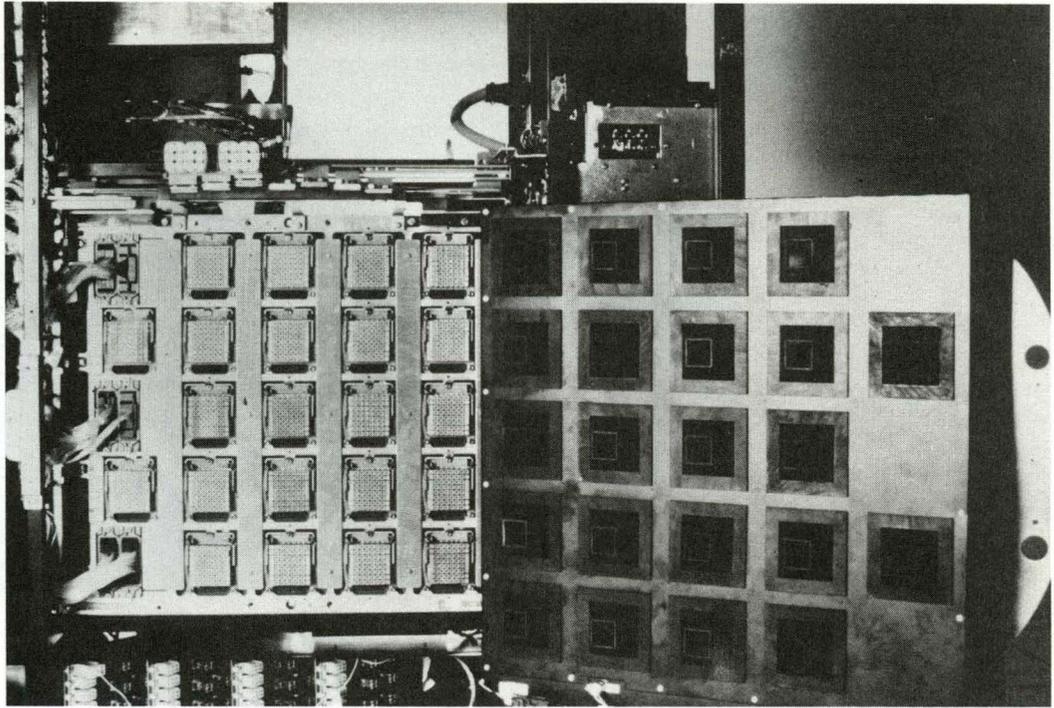


Figure 6. MCM board mounted within the 4381 Processor

## Logic Cooling

The high density of the logic circuits on the ceramic substrate used for 4381 logic required a new method of removing the heat generated. The approach used, called impingement cooling, permits room-temperature air instead of water to be used to cool the MCMs.

A ceramic cap covers the chips mounted on the 64-mm ceramic substrate. An aluminum heat sink is mounted over the ceramic cap. Figure 7 on page 20 shows a 64-mm MCM with a portion of the heat sink cut away. Air to cool the circuit on the substrate is blown toward the heat sink. The air is blown through nozzles (one for each MCM) located about one-eighth of an inch away from the MCMs. Figure 8 on page 20 shows an impingement cooling nozzle.

The nozzles are attached to the impingement cooling chamber, which receives air from the room. The air from the chamber is blown through the nozzles to the heat sinks. Thus, the MCMs are cooled individually (or in parallel), as opposed to the serial approach usually used in air cooling, in which air is blown from one side of the board across the logic. In the serial approach, the circuits closest to the side from which the air is blown receive cooler air than the circuits at the other side of the board.

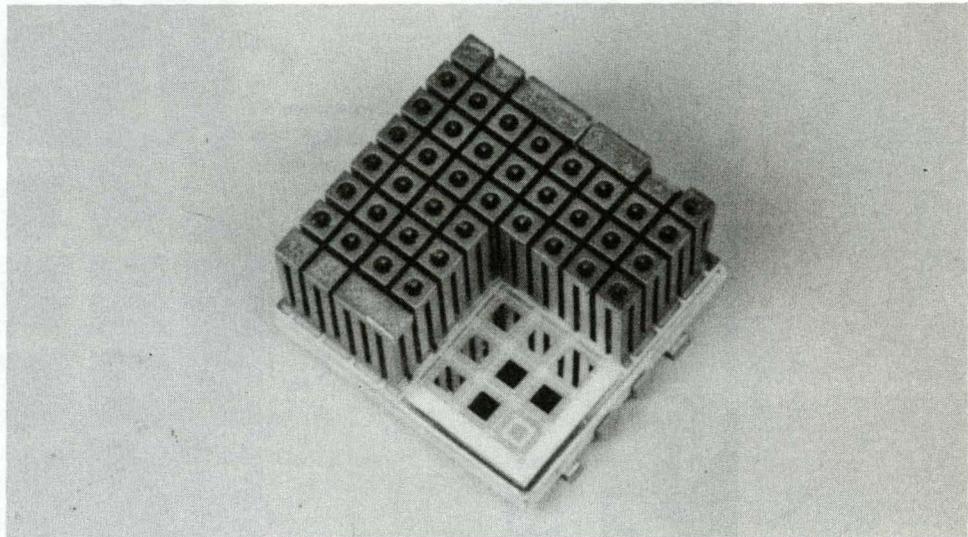


Figure 7. 64-mm MCM with a portion of the heat sink cut away

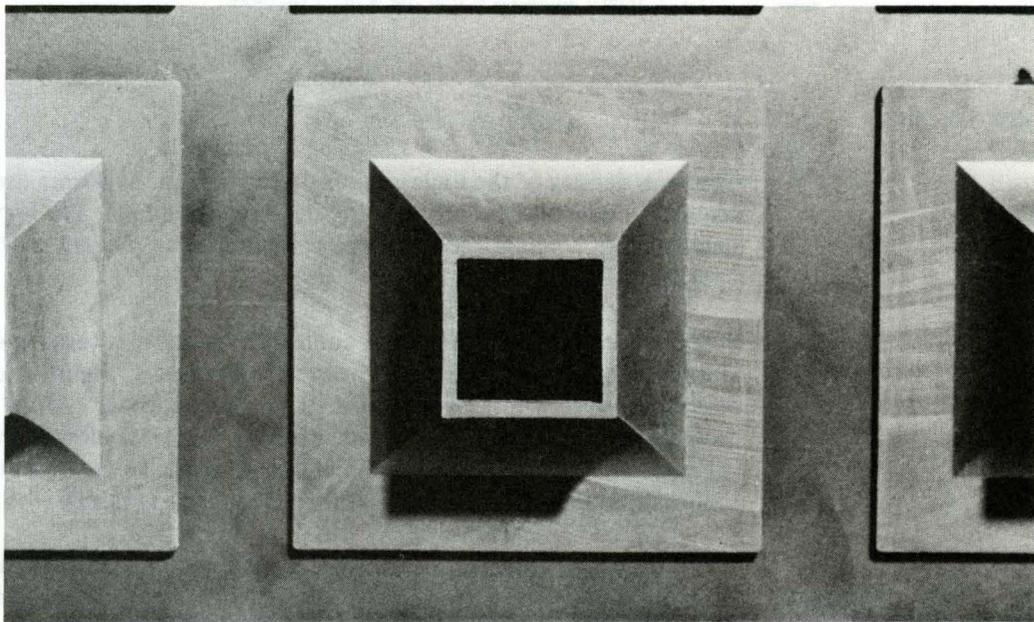


Figure 8. An impingement cooling nozzle

## Storage Technology

The 64K-bit SAMOS (Silicon and Aluminum Metal Oxide Semiconductor) FET (Field Effect Transistor) storage chip that is used for processor storage in 4341 Processors is used to implement processor storage of up to 16Mb in 4381 Processors. The 64K-bit chips are packaged to provide 1Mb of processor storage per storage card. For processor storage above 16Mb in a 4381 processor, a 256K-bit enhanced SAMOS FET chip is used and its packaging provides 2Mb per storage card. The speed of the 256K-bit chip is faster than that of the 64K-bit chip (250 ns versus 370 ns).

An array chip that had not previously been used in other IBM processors is used to implement reloadable control storage and high-speed buffer storage in 4381 Processors. This array chip has a capacity of 1K bytes and a 20-ns cycle time. A faster, lower capacity chip that is contained in other IBM processors is used to implement the high-speed buffer directory and local storage in a 4381 instruction processing function.

## 10:10 Architecture

Two architectures are implemented in 4381 Processors: System/370 architecture and System/370 extended architecture. The mode of processor operation selected during an initial microcode load (IML) of a 4381 Processor determines the architecture that is functional. When System/370 mode is selected, System/370 architecture is functional. When System/370-XA mode is selected, System/370 extended architecture is functional.

### System/370 Architecture

The System/370 architecture implemented in 4381 Processors includes nearly all the facilities defined for System/370, as described in *IBM System/370 Principles of Operation* (GA22-7000). Basic control (BC) and extended control (EC) modes are implemented.

The System/370 architecture implemented in 4381 Processors does not include the following facilities that are defined for optional implementation in System/370 processors:

- Extended machine check logout (that processor-dependent data logged beginning at the processor storage address specified in control register 15—normally location 512), the processor-dependent logout to locations 256 to 351, and the processor-dependent I/O extended logout (that data logged beginning at the address in the word at processor storage location 172)
- Direct Control (READ DIRECT and WRITE DIRECT) instructions. The external signals facility in 4381 Processors provide the six external interruption lines included in the Direct Control facility without the two instructions READ DIRECT and WRITE DIRECT
- Suspend and resume

- Multiprocessing (includes SET PREFIX, STORE PREFIX, SIGNAL PROCESSOR, and STORE CPU ADDRESS instructions)—implemented in 4381 Model Groups 14 and 3 only
- Channel Set Switching (CONNECT CHANNEL SET and DISCONNECT CHANNEL SET instructions)
- Compatibility features for emulation of other processors (1401/1440/1400 Compatibility, for example)
- Certain control program assists (such as OS/VS1 assist, APL assist, and OS/DOS Emulation)
- Certain processor dependencies

Control and problem programs written for System/370, 4300 System/370 mode, or 30XX Processors can be run without modification in a 4381 Processor operating in System/370 mode that has a comparable hardware configuration, with the following exceptions:

1. Programs that depend on facilities that are not defined in the System/370 architecture for 4381 Processors (READ DIRECT, WRITE DIRECT, Channel Set Switching instructions, for example)
2. Time-dependent programs. (They may or may not run correctly.)
3. Programs that depend on results defined in the *System/370 Principles of Operation* (GA22-7000) to be unpredictable or processor-dependent
4. Programs that use unassigned fields in processor formats (instruction formats, for example) that are not explicitly made available for program use
5. Programs that depend on interruptions caused by errors, such as unassigned operation codes or command codes

System/370 architecture as implemented in 4381 Processors provides the ability to execute:

- 4300 System/370 mode control and problem programs that are not time-dependent or 4300 Processor-dependent
- 4300 problem programs that are designed to operate with 4300 ECPS:VSE mode control programs and that are not time-dependent or 4300 Processor-dependent. (A 4300 ECPS:VSE mode control program cannot execute in a 4381 Processor.)
- System/370 or 30XX control and problem programs that are not time-dependent or System/370 processor-dependent
- System/360 control and problem programs that are not time-dependent or System/360 processor-dependent

## System/370 Extended Architecture

System/370 extended architecture is System/370 architecture with certain exclusions and a set of functional extensions. The new facilities provided by System/370 extended architecture as implemented in the 4381 Processor are the following:

- A 31-bit addressing capability that provides for addressing more than two gigabytes (2G-bytes) of virtual and real storage
- Dynamic channel subsystem architecture that provides additional channel control functions that are designed to improve I/O performance
- An expanded trace capability that provides for branch tracing, address space tracing, and explicitly initiated tracing
- Page protection, which can be used to prevent storing into selected virtual storage pages (see Section 50)
- An instruction (START INTERPRETIVE EXECUTION) to handle interpretive instruction execution that provides a mechanism for implementing virtual machine support
- A sort microcode assist

The new capabilities provided in System/370 extended architecture are designed to extend the functional capabilities of System/370 architecture while maintaining compatibility between the two architectures for problem programs. The instruction set for System/370 extended architecture includes all the problem state and semiprivileged instructions defined for System/370 mode of operation (including MOVE INVERSE).

The instruction set for System/370 extended architecture contains all the privileged instructions defined for System/370 architecture except the following:

- INSERT STORAGE KEY (ISK)
- SET STORAGE KEY (SSK)
- RESET REFERENCE BIT (RRB)
- CLEAR CHANNEL (CLRCH)
- CLEAR I/O (CLRIO)
- HALT DEVICE (HDV)
- HALT I/O (HIO)
- RESUME I/O (RIO)
- START I/O (SIO)
- START I/O FAST RELEASE (SIOF)

- STORE CHANNEL ID (STIDC)
- TEST CHANNEL (TCH)
- TEST I/O (TIO)

The following instructions are implemented in System/370 extended architecture but not in System/370 architecture:

- BRANCH AND SAVE AND SET MODE (BASSM)
- BRANCH AND SET MODE (BSM)
- DIVIDE-extended (DXR)
- INSERT PROGRAM MASK (IPM)
- START INTERPRETIVE EXECUTION (SIE)
- TRACE (TRACE)
- CLEAR SUBCHANNEL (CSCH)
- HALT SUBCHANNEL (HSCH)
- MODIFY SUBCHANNEL (MSCH)
- RESET CHANNEL PATH (RCHP)
- RESUME SUBCHANNEL (RSCH)
- SET ADDRESS LIMIT (SAL)
- SET CHANNEL MONITOR (SCHM)
- START SUBCHANNEL (SSCH)
- STORE CHANNEL PATH STATUS (STCPS)
- STORE CHANNEL REPORT WORD (STCRW)
- STORE SUBCHANNEL (STSCH)
- TEST PENDING INTERRUPTION (TPI)
- TEST SUBCHANNEL (TSCH)

## 31-Bit Addressing

The 31-bit addressing capability significantly increases the amount of virtual and real storage that can be addressed in a virtual storage environment—over 2 billion bytes versus over 16 million bytes for the 24-bit addressing capability used in 4381 System/370 mode of operation. To maintain problem program compatibility for System/370 and System/370-XA modes, bimodal operation is supported for System/370-XA mode that permits concurrent execution of problem programs that use 24-bit addressing and those that use 31-bit addressing.

The addressing mode in effect is determined by bit 32 in the current PSW. When bit 32 is zero, 24-bit addressing mode is in effect. When bit 32 is one, 31-bit addressing is in effect. The addressing mode controls the size of the effective address generated for instructions and instruction operands. It does not control the size of PER addresses or of the addresses used to access DAT, ASSN, linkage, entry, and trace tables. These addresses are always 31 bits in size.

Note that the 24-bit addresses that are generated when 24-bit addressing mode is in effect are converted to 31-bit addresses by the addition of seven high-order zeros.

## Dynamic Channel Subsystem

The dynamic channel subsystem defined for System/370-XA mode of operation provides improvements and additional functional capabilities. The major differences between the channel architecture for System/370-XA mode and System/370 mode in 4381 Processors are the following:

- Channels are not assigned a channel number. The instruction processor issues I/O requests that specify the I/O device to be used. A channel is not specified. All types of I/O requests are queued (not just SIOF requests, as in System/370 mode of operation), and instruction processing function execution continues after any I/O request is issued without waiting for any status information from channel control hardware. A new set of I/O instructions is defined for handling I/O operations.
- Channel path management is performed by the channel control function rather than by the I/O supervisor portion of the control program. The channel path to be used to access an I/O device is selected by the channel control function. When multiple channel paths exist to a device, the set of paths specified for the device is inspected in the sequence defined by the installation using the Input/Output Control Program, which is discussed in Section 20:20. The 4381 Processor supports up to four paths per I/O device.
- A dynamic reconnection capability is supported that permits an I/O device to reconnect a disconnected channel program to the first available channel path to the device when multiple paths to the device exist, rather than only to the channel path from which the channel program disconnected. This capability is utilized, for example, by 3880 Storage Control Models 2 and 3 with attached 3380 Model AA4 Direct Access Storage (which has dynamic path selection). For devices without dynamic path selection, reconnection occurs only to the path from which the channel program disconnected.

- Faster restart of I/O devices is provided by dequeuing the next request for an I/O device when ending status for a completed I/O operation on the device is passed to the instruction processing function.
- A reformatted channel command word (CCW) is defined that uses 31-bit addressing. However, channel programs that use the CCW format defined for System/370 mode of operation will operate in System/370-XA mode for compatibility purposes. This implementation enables existing programs that have their own channel programs and that use the OS/VS EXCP macro to request I/O operations to operate with System/370-XA mode in effect without modification.
- Device addressing is expanded to permit up to 65,535 devices to be addressed in one configuration. However, in a 4381 Processor, a maximum of 2048 I/O devices can be addressed. Up to 256 channel paths in one system can be addressed (as in System/370 architecture). However, a maximum of 12 (Model Groups 11, 12, 13, 1, and 2) or 18 (Model Groups 14 and 3) channels can be addressed in a 4381 Processor.

The changes implemented in dynamic channel subsystem architecture are designed to improve I/O performance by reducing delays in the start of I/O operations and by relieving the operating system I/O supervisor of path-scheduling functions. The changes affect the operating system I/O control program and channel control microcode rather than problem programs. Byte multiplexer channel, block multiplexer channel, and data streaming mode definitions are the same for System/370-XA and System/370 modes of operation, as is the physical structure of the 4381 channel hardware. All differences between channel operations for the two modes in a 4381 Processor are handled by channel microcode.

## Compatibility

Problem state programs that execute in System/370, 30XX, or 4300 processors (subject to constraints listed for System/370 mode) or in a 4381 Processor operating in System/370 mode can execute in a 4381 Processor operating in System/370-XA mode without modification. Programs that operate in supervisor state and use any of the System/370 mode privileged instructions that are not implemented for System/370-XA mode cannot execute in a 4381 Processor operating in System/370-XA mode without modification.

## Section 20: 4381 Processor Uniprocessor Model Groups

The functional components physically contained within the frames of a 4381 uniprocessor (Model Group 11, 12, 13, 1, or 2) unit are one instruction processing function, all processor storage, the storage control function, channels, and the support processor subsystem. Figure 9 shows the logical components of uniprocessor model groups of the 4381 Processor.

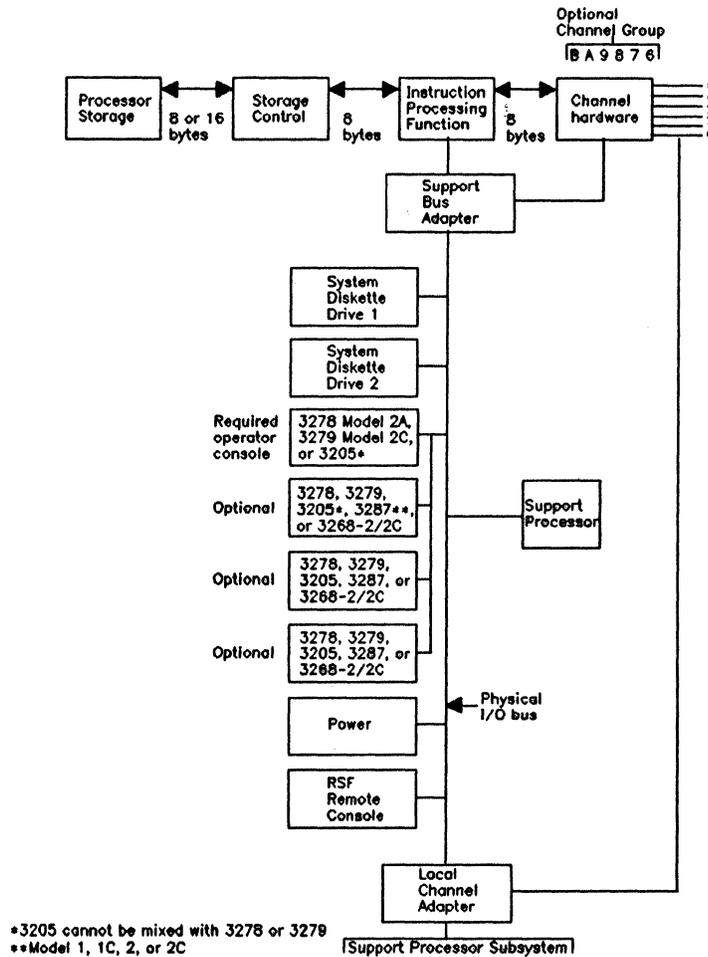


Figure 9. Logical components in a 4381 Processor Model Group 11, 12, 13, 1, or 2

## 20:05 Instruction Processing Function

### General Description

The instruction processing function contains all the elements necessary to decode and execute the instructions in the instruction set for 4381 Processors. I/O instructions are partially processed by the instruction processing function and partially processed by channel hardware. Extensive parity checking is done within the instruction processing function to ensure data validity.

All instruction execution functions and most channel operations are microcode controlled. Microinstructions are four bytes in length. Reloadable control storage for the residence of instruction processing function microcode is standard.

Certain basic control and service functions are provided for 4381 Processors by the support processor, a component of the support processor subsystem, instead of by the instruction processing function. The support processor is a microcoded controller with its own control storage. The support processor also handles I/O operations for the operator console device and up to three other display consoles and/or printer devices that are directly attached to a 4381 Processor. In addition, the support processor controls diagnostic facilities (see discussions in Sections 20:15 and 60:15).

The instruction processing function in a 4381 Processor Model Group 11, 12, 1, or 2 has a 68-nanosecond cycle time. A 4381 Processor Model Group 13 has a 56-nanosecond cycle time. The primary data path within the instruction processing function and between the instruction processing function and processor storage and the channels is eight bytes wide (as in 4341 Processors), which is the widest primary data path implemented in IBM large-scale (System/370 and 30XX) processors.

Elements included in the instruction processing function to perform instruction execution are instruction buffers for instruction prefetching, an eight-byte-wide arithmetic logic unit, an eight-byte MQ register, an eight-byte-wide byte shifter, an eight-byte-wide bit shifter, and external registers. These same elements are implemented in 4341 Processors and are functionally alike in 4381 and 4341 Processors.

The instruction processing function in 4381 Processors includes facilities like those in 4341 Processors that are designed to speed up instruction execution. First, during sequential instruction processing, instruction fetching is overlapped with instruction execution. Unoverlapped instruction fetching usually occurs only when a successful branch instruction is processed.

Second, several functions are performed during the single instruction cycle of 68 or 56 nanoseconds that precedes the execution cycle(s) of each instruction. The following are performed during the instruction cycle of a 4381 Processor: instruction decoding, selection of the microcode required to execute the instruction, calculation of the required storage address using base register and displacement values for instructions that reference storage, fetching of the contents of the register 1 specification in RR- and RS-type instructions, testing for any interruptions, and complete execution of certain instructions (BC and BCR when a

branch is not taken, LA when the index register is zero, LR, and LTR instructions).

Third, floating-point additions and subtractions that involve values with equal exponents, and decimal additions and subtractions may be performed with the same speed as binary additions and subtractions. This is made possible by the use of an eight-byte-wide arithmetic logic unit for floating-point and decimal arithmetic instructions as well as for binary arithmetic. Usually, additions and subtractions performed using binary arithmetic operate much faster than when decimal or floating-point arithmetic is used.

Fourth, decimal arithmetic operations are performed significantly faster in 4381 Processors than in intermediate-scale System/370 processors and execute as fast as decimal operations in certain large-scale System/370 processors. Fifth, an eight-byte-wide shifter is utilized. This shifter allows a shift to be performed in one cycle instead of multiple cycles.

The shifter is also used to align data that is not on the proper boundary. The use of the shifter instead of microcode for the alignment function eliminates in 4381 Processors nearly all the performance degradation that is experienced in many System/370 processors when data is not aligned on the correct boundary. In 4381 Processors, no performance degradation occurs when alignment is performed within a doubleword. Some degradation occurs when the unaligned data required spans two doublewords, since both doublewords must be fetched to obtain the needed data.

The multifunction instruction cycle, eight-byte-wide arithmetic logic unit, and eight-byte-wide shifter give the instruction processing function the ability to execute 21 of the 4381 Processor instructions (such as the RR-type and certain other instructions) in two cycles (one instruction and one execution).

Eight-byte external registers are included in the instruction processing function. These hardware registers provide data links between instruction processing function microcode and channel or instruction processing function hardware. The external registers contain such items as the PSW, the time-of-day clock, storage address registers, the channel storage address register, interruption registers, the next instruction buffer register, and status registers.

The instruction processing function of 4381 Processors has been functionally improved over the instruction processing function in 4341 Processors in the following major areas:

- Microcode or hardware changes have been made where possible to speed up the execution of many instructions.
- A high-speed hardware multiplier is implemented in the instruction processing function (all 4381 model groups except 1 and 11) to improve binary and floating-point multiply operations.
- System/370 extended architecture is supported (most of the changes required for this support are in microcode).
- More checking circuits are included for error detection to aid in improved fault isolation (1200 for uniprocessor and 2600 for multiprocessor 4381 model groups).

The instruction processing function contains a data local storage area of 256 doublewords for use during the execution of instructions. This data local storage contains certain control registers, the general registers, the floating-point registers, twelve channel work areas, save areas, and work areas.

A trace array of 32 entries is included in the instruction processing function to trace the addresses of executed microcode. The array is always updated during instruction execution and can be set to operate in one of two modes. In one mode, the trace array contains the addresses of the last 32 microinstructions executed. In the other mode, the trace array contains the addresses of the last 32 microinstructions that caused switching from one microcode module to another. The trace array is provided to aid in error detection and recovery. The array helps to indicate the cycle that caused the error when a machine check occurs.

A reconfiguration function is implemented for reloadable control storage, which contains a spare area for this function. (Reconfiguration is provided for each reloadable control storage in a 4381 Model Group 14 or 3 processor). If a parity error occurs during a read from control storage, the read operation is retried once. If the error is not corrected, reconfiguration is performed by the instruction retry facility. The failing control storage address is placed in a reconfiguration register and a space is allocated from the spare area. This space is then loaded with the required microcode from the appropriate functional diskette. Thereafter, when the reconfigured address is referenced, the spare area is accessed.

The operator is not notified when control storage reconfiguration is done and no performance degradation occurs. Up to eight errors can be reconfigured. When the ninth error occurs, reconfiguration is no longer possible, system operation terminates, and the operator is notified that repair must be performed.

The address translation facilities provided for System/370 and System/370-XA modes are discussed in Section 50. Other significant features of the instruction processing function of 4381 Processors are discussed in the remainder of this subsection.

## **Instruction Set**

The standard instruction set for 4381 Processors contains all the instructions implemented for 4381 Processors (no instructions are optional). The standard instruction set for a 4381 Processor Model Group 11, 12, 13, 1, or 2 operating in System/370 mode consists of all the System/370 instructions defined in *IBM System/370 Principles of Operation* (GA22-7000) except those associated with features not implemented in these 4381 model groups (READ DIRECT, WRITE DIRECT, RESUME I/O, and multiprocessing and channel set switching instructions).

The standard instruction set for a 4381 Processor operating in System/370-XA mode consists of all the instructions defined in *IBM System/370 Extended Architecture Principles of Operation* (SA22-7085).

The STORE CPU ID instruction, which permits a program to determine the processor and version of the processor upon which it is operating and provides the processor serial number, stores the following version codes:

- X'06' for the Model Group 11
- X'08' for the Model Group 12
- X'03' for the Model Group 13
- X'02' for the Model Group 1
- X'00' for the Model Group 2

The DIAGNOSE MSSFCALL instruction is implemented in 4381 Processors for System/370-XA mode of operation. It is used by the MVS/XA operating system. This instruction supports seven commands and can be issued only by a program that is operating in supervisor state. It specifies the function to be performed and the location of a data area in processor storage (up to 2K bytes in size) that is to receive completion status for the instruction and any requested configuration information.

The following DIAGNOSE MSSFCALL commands are implemented in 4381 Processors:

- SCP INFO (provides processor storage and auxiliary storage sizes)
- CHANNEL PATH INFO (provides channels installed and online/offline status)
- VARY CHANNEL PATH OFF (used to vary a channel path offline)
- VARY CHANNEL PATH ON (used to vary a channel path online)
- READ RESTART REASON (enables the operating system to obtain a one-byte restart modifier that was entered by the operator and saved in auxiliary storage after a restart was initiated)
- WRITE CONSOLE TEXT (enables the operating system to place display information for the operator console in auxiliary storage)
- READ LOOP RECORDING (enables a stand-alone dump program to obtain trace data saved in auxiliary storage to aid in debugging)

The configuration commands are processed by the instruction processing function. The support processor is not involved. The auxiliary storage area is accessed as required to process all the DIAGNOSE MSSFCALL commands.

## Multiply and Add Facility

The standard Multiply and Add Facility for all uniprocessor 4381 model groups provides the MULTIPLY AND ADD instruction and is functional in System/370 and System/370-XA modes. This instruction performs a combination of vector multiplication and addition operations that can replace the inner loop of common matrix computations to improve the performance of the multiply and add operations (up to 35% reduction in compute-intensive subroutine execution time).

The MULTIPLY AND ADD instruction performs the function  $A = (B \times S) + C$  where A, B, and C are vectors and S is a scalar. A, B, and S must consist of normalized, long-format floating-point numbers, while vector C can contain unnormalized, long-format elements.

A common use for this assist is to have an installation-written Assembler Language routine containing this instruction called from high-level language programs as required. The MADS mnemonic is supported by the Assembler Language. For detailed information about this instruction, see *IBM System/370 Mathematical Assists* (SA22-7094).

## Elementary Math Library Facility

The Elementary Math Library Facility feature is standard in the 4381 Processor Model Group 2. It is functional in System/370 and System/370-XA modes. It provides four functions (eight instructions) that use short- and long-format floating-point operands. The instructions are SQUARE ROOT (SQDR and SQER), EXPONENTIAL (EXPD and EXPE), COMMON LOGARITHM (LGCD and LGCE), and NATURAL LOGARITHM (LGND and LGNE). The two operands are contained in floating-point registers.

The Elementary Math Library (EML) Programming RPQ (5799-BTB) for VS FORTRAN Mathematical Library supports this facility for operation under VM/CMS, MVS/370, and MVS/XA. This assist can reduce processor-busy time by up to 64 percent for the assisted functions.

The publication *IBM System/370 Mathematical Assists* (SA22-7094) describes the Elementary Math Library Facility instructions.

## Square Root Facility and Mathematical Function Facility

These two features provide the functions included in the Elementary Math Library Facility for the 4381 Model Group 2. The Square Root Facility is standard in all 4381 uniprocessor model groups and performs an assist for the square root function using long- or short-precision floating-point arithmetic.

The Mathematical Function Facility is standard in 4381 Model Groups 12 and 13 to assist in exponential, common logarithms, and natural logarithm functions using short- or long-format floating point arithmetic. Reductions in compute-intensive subroutine execution time vary from 37% to 64% using this facility.

## ECPS:MVS

ECPS:MVS is a standard facility in 4381 uniprocessor model groups. It provides 13 privileged instructions and the Page Fault Assist function that are required to execute MVS with the MVS/System Product-JES2 or MVS/System Product-JES3 program product installed in a 4381 Processor. The provided instructions are the following:

- ADD FRR\*
- FIX PAGE
- SVC ASSIST\*
- OBTAIN LOCAL LOCK\*
- RELEASE LOCAL LOCK\*
- OBTAIN CMS LOCK\*
- RELEASE CMS LOCK\*
- TRACE SVC INTERRUPTION
- TRACE PROGRAM INTERRUPTION
- TRACE INITIAL SRB DISPATCH
- TRACE I/O INTERRUPTION
- TRACE TASK DISPATCH
- TRACE SVC RETURN

All 13 instructions listed above and the Page Fault Assist function can be utilized when System/370 mode is in effect. For System/370-XA mode, only the instructions identified by an asterisk are utilized. The facilities of ECPS:MVS are discussed in *IBM System/370 Assists for MVS (GA22-7079)*.

Virtual Machine Extended Facility Assist is also standard to enable the ECPS:MVS instructions to be executed directly by an MVS virtual machine without an interruption and simulation by the VM/370 CP (Control Program).

ECPS:MVS and ECPS:VM/370 (described below) can be used concurrently to improve performance when MVS/370 executes in a virtual machine in a VM/370 environment in a 4381 Processor.

## ECPS:VM/370

The ECPS:VM/370 feature is standard in 4381 uniprocessor model groups and is functional only when System/370 mode is active. It consists of the Virtual Machine Assist, Control Program Assist, Expanded Virtual Machine Assist, Virtual Interval Timer Assist, and Shadow Table Bypass Assist components. The first four components are functionally equivalent to the same components of the ECPS:VM/370 feature for 4341 Processors and the VM/370 hardware assist function for System/370 Models 135, 138, 145, and 148. These components are designed to improve the performance of the Control Program component of VM/370. The Shadow Table Bypass Assist function is designed to improve the performance of MVS/SP Version 1 operating in a virtual equals real (V=R) virtual machine in a VM/370 environment.

### Preferred Machine Assist

The standard Preferred Machine Assist feature for all uniprocessor 4381 model groups is operative only in System/370 mode. It is designed to improve the performance of MVS/SP Version 1 running in a V=R preferred virtual machine. When supported by VM/System Product High Performance Option, Preferred Machine Assist permits the MVS/SP V=R virtual machine to operate with a minimum of VM/370 control program support and to perform native I/O operations on dedicated and nondedicated channels.

## 20:10 Storage

The 4381 Processors have a two-level storage system — a small high-speed buffer storage backed by a large processor storage. The use of a two-level storage system, in which the instruction processing function works mostly with the high-speed buffer, significantly reduces the effective processor storage cycle of 4381 Processors and greatly contributes to their high internal performance.

## Processor Storage

Processor storage is available for 4381 Processor uniprocessor model groups as follows:

4381 Model Group	Processor Storage Sizes in Megabytes (Mb)	Storage Model
11	4	L11
	8	M11
	16	P11
12	8	M12
	16	P12
	24	Q12
	32	R12
13	8	M13
	16	P13
	24	Q13
	32	R13
1	4	L1
	8	M1
	16	P1
2	4	L2
	8	M2
	16	P2
	24	Q2
	32	R2

Field upgrades from one processor storage model to another in the same 4381 model group are supported for all uniprocessor model groups. A portion of the installed processor storage is reserved for processor use and is called auxiliary storage.

Access to processor storage is made via the storage control function, which operates under the control of the instruction processing function. The path to and from processor storage is 16 bytes wide (two doublewords). Data that enters/leaves processor storage is aligned on a doubleword boundary.

Error checking and correction (ECC) hardware provides automatic detection and correction of all single-bit processor storage errors and detection of all double-bit and many multiple-bit errors. Certain double-bit errors can also be corrected by microcode. ECC logic is contained in the storage control function and performs checking on a doubleword basis. The ECC feature and double-bit error correction are discussed in Section 60.

Store and fetch protection are standard. For 4381 uniprocessor configurations with up to 16Mb of processor storage, one 7-bit storage protection key is provided

for each 2K-byte block of processor storage. For a 4381 uniprocessor configuration with more than 16Mb of processor storage installed, one 7-bit storage protect key for each 4K-byte block of processor storage is supported, since only one key for every 4K bytes is provided in the processor storage above 16Mb.

The standard Extended Addressing feature in 4381 Model Groups 12, 13, and 2 permits processor storage above 16Mb to be utilized. The feature provides the following:

- Extended real addressing, which provides the ability to address up to 64Mb of real storage using an additional two bits in page table entries to generate a 26-bit real address from a 24-bit virtual address. As implemented in 4381 Model Groups 12, 13, and 2, Extended Addressing permits up to 32Mb of real storage to be addressed.
- Storage-key 4K-byte block, which permits storage keys to be provided for 2048-byte blocks and/or 4096-byte blocks (instead of only for 2048-byte blocks)
- Storage key instruction extension, which provides the instructions SET STORAGE KEY EXTENDED, INSERT STORAGE KEY EXTENDED, and RESET REFERENCE BIT EXTENDED that can specify a 31-bit real address and can be used regardless of whether keys are provided on a 2048- or 4096-byte block basis
- 31-bit IDAW, which permits an indirect data address word to specify a 31-bit absolute address

The TEST BLOCK (TB) privileged instruction (not implemented in 4341 Processors) is provided to enable a program to (1) determine the usability of a 4K-byte block of processor storage and its associated one or two 7-bit protection keys and (2) perform storage validation by storing zeros in the 4K bytes to attempt to set up good ECC bits in all the doublewords.

The TB instruction specifies the 31-bit real address of a 4K-byte block on a 4K-byte address boundary in processor storage that is to be tested. The specified real address is tested for an addressing exception (address outside of installed processor storage) and violation of low address protection. The real address is not tested for key-controlled protection or segment protection.

The condition code is set for a TB instruction to indicate the usability of the specified 4K-byte block and its protection keys. If both the block and its protection key(s) are usable, condition code 0 is set. Condition code 1 is set if the 4K-byte block is unusable, one or both of its keys are unusable, or any combination of block and keys is unusable.

In 4381 Processors, if the protection keys for the specified 4K-byte block are both usable the TB instruction sets them both to zero. If either key is not usable the TB instruction leaves both keys unmodified. The TB instruction stores zeros in the 4K-byte block, whether the block or its keys are usable, to attempt to establish good ECC bits.

The TB instruction accesses the TEST BLOCK area within auxiliary storage to determine the usability of the specified 4K-byte block and its two protection keys. There is one internal record for 4K-byte block errors and one internal record for

protect key errors. There is one bit in the 4K-byte block record for each 4K bytes of processor storage and one bit in the protect key record for its one or two associated keys. A one in a bit position indicates the associated 4K-byte block or protect key is unusable. To execute a TB instruction, the instruction processing function inspects the two appropriate bits in the TEST BLOCK internal records, sets the condition code, and stores zeros in the addressed 4K-byte block and in both keys if they are both unusable.

The two TEST BLOCK internal records are placed in auxiliary storage during IML. These two records are maintained on functional diskette 1, which is shipped to a 4381 installation with all zeros in both records. During processor operation, any time a double-bit error consisting of two solid errors or two consecutive protect key errors occur, the TEST BLOCK internal record in auxiliary storage and that on functional diskette 1 are updated. Thus, known unusable 4K-byte blocks are saved across IMLs and power-offs. The TEST BLOCK internal records on functional diskette 1 are updated as appropriate whenever processor storage is repaired.

The TB instruction is designed to be used during IPL to enable the operating system to build a page frame table that indicates the known unusable 4K-byte page frames to avoid their assignment. TB should also be issued if an uncorrectable storage error is encountered during system operation to attempt to validate the unusable block (store good ECC bits). Successful validation will prevent the occurrence of a machine check if the unusable block is prefetched or inadvertently referenced.

## Auxiliary Storage

The UCWs for System/370 mode or the subchannels and control unit blocks for System/370-XA mode, the I/O queuing area, a trace area, the TEST BLOCK internal records, and certain work areas are located in highest addressed processor storage. This storage, called auxiliary storage, is reserved for processor rather than program use and is inaccessible to all programs.

The size of auxiliary storage in bytes for a 4381 Processor Model Group 11, 12, 1, or 2 operating in System/370 mode is 56,320 (57,344 for the Model Group 3) plus 64 times the number of UCWs defined (128 to 2048) rounded up to a 4K boundary. For System/370-XA mode, auxiliary storage size in bytes for 4381 Model Groups 11, 12, 1, and 2 is 103,168 (104,704 for the Model Group 3) plus 70 times the number of control units defined (1 to 256) plus 180 times the number of subchannels defined (up to 2048) rounded up to a 4K boundary.

The minimum auxiliary storage requirement for System/370 mode of operation is 64Kb (128 UCWs defined), while the maximum requirement is 184Kb (2048 UCWs defined). For System/370-XA mode of operation, a minimum of 112Kb is required (for 0 subchannels and 128 control unit control blocks) and the maximum requirement is 480Kb (for 2048 subchannels and 256 control unit control blocks).

The size of auxiliary storage is determined during IML. The processor storage address of the first byte of auxiliary storage is calculated and placed in an address check boundary (ACB) register. Any attempt to access an address equal to or above the ACB register value during program execution results in an addressing exception program interruption.

The contents of auxiliary storage vary depending on the mode, System/370 or System/370-XA, in effect. During an IML, the required auxiliary storage area is initialized as appropriate, using information contained on the functional diskette(s). Auxiliary storage for System/370 mode contains the following in the highest to the lowest addressed locations:

- UCW area with a minimum of 128 and a maximum of 2048 UCWs
- SIOF queuing area
- I/O trace area
- Channel error logout area
- Channel UCW directory area
- Instruction tracing area
- Channel data buffer reconfiguration test data
- Restart text save area
- Two internal records for the TEST BLOCK instruction (one for unusable protect keys and one for unusable 4K-byte blocks)
- Engineering/scientific assist feature table
- Program event recording area
- Control storage link information
- K-addressable auxiliary storage area of 1K bytes. This area contains various pointers and data fields used by the instruction processing function (pointers to the beginning of the other areas in auxiliary storage, the time-of-day clock, the CPU timer, the clock comparator, the interval timer, for example).

For System/370-XA mode, auxiliary storage contains the following in the highest to the lowest addressed locations:

- Monitoring data area (32 bytes/subchannel)
- I/O trace area
- Channel error log
- CRW (channel report word) queue
- Subchannel area
- Control unit block area (70 bytes/control unit)
- Channel directories
- Channel data buffer reconfiguration test data

- I/O queuing information
- Interrupt area
- Restart text save area
- SIE instruction work area
- Two internal records for the TEST BLOCK instruction
- Instruction tracing area
- Engineering/scientific assist feature table
- Program event recording area
- Control storage link information
- K-addressable auxiliary storage area of 1K bytes. The contents of this area varies slightly for System/370-XA and System/370 modes.

### Storage Control Function

The storage control function operates under the control of the instruction processing function to handle all access to processor storage. The following components are part of the storage control function:

- High-speed buffer storage and its directory
- The TLB for translating virtual storage addresses in instructions to real storage addresses for both System/370 and System/370-XA modes (discussed in Section 50)
- The key stack that contains the 7-bit keys for the processor storage installed. Each key consists of four access control (store protection) bits, one fetch protection bit, one reference bit, and one change bit.
- The ECC logic for processor storage (see Section 60)
- The input/output (I/O) data register that is used to transfer data (1) among the components of the storage control function and (2) between processor storage and the instruction processing function

The I/O data register is 64 bytes wide to improve instruction execution speed. For fetches/stores involving the instruction processing function (including those done for the channels), only 8 bytes of the 64-byte I/O data register are used, while 16 bytes are used for fetches/stores involving processor storage.

## High-Speed Buffer Storage

The high internal performance of 4381 Processor model groups is achieved in part by the inclusion of high-speed buffer storage. The high-speed buffer is a standard feature and provides high-speed data access for instruction processing function fetches and stores.

The high-speed buffer storage provided in 4381 uniprocessor model groups is the following:

4381 Model Group	High-Speed Buffer Storage (Kb)
11	4
12	32
13	64
1	8
2	32

When the page size in effect is 4K bytes, the full capacity of the high-speed buffer is used in any uniprocessor model group. When a 2K-byte page size is in effect, half the capacity of the high-speed buffer is used in any uniprocessor model group.

Buffer storage control and use are handled entirely by buffer control function hardware and are transparent to the programmer, who need not adhere to any particular program structure in order to obtain close to optimum use of the buffer. Parity checking is used for data verification in the buffer.

When a fetch request is made by the instruction processing function for instructions or data, high-speed buffer storage control determines whether the requested doubleword is in the high-speed buffer by interrogating the buffer directory, which indicates the current contents of the buffer. If the doubleword requested is present in the buffer and valid, it is sent directly to the instruction processing function without a processor storage reference.

If the requested doubleword is not currently in the high-speed buffer, a processor storage fetch is made, the data is assigned a buffer location and stored in the buffer, and the requested doubleword is sent to the instruction processing function.

When data is stored by the instruction processing function, the high-speed buffer is updated if the contents of the processor storage location being altered are currently being maintained in the buffer. Processor storage is not modified, however, since the high-speed buffer in 4381 Processors is a store-in, rather than a store-through, type of buffer. If the data is not currently being maintained in the buffer, a processor storage fetch is made to obtain the required block of data and load it in the buffer. The store is then made to the just loaded buffer location and processor storage is not modified.

If the data in the buffer location that is to receive the new block of data has been changed while in the buffer, this data must be unloaded before the new data can be loaded. In order to reduce the time the instruction processing function must wait for the requested data in this situation, a swap buffer is implemented. The changed data is written to the swap buffer while processor storage is being accessed for the new block of data to overlap most block unload time with processor storage access time. After the new block is loaded and the requested data is sent to the instruction processing function, the data in the swap buffer is written to processor storage.

The channels read into and write from processor storage using the input/output data register in the storage control function. When a channel writes data (input operation from an I/O device), the buffer directory is interrogated. If data from the affected processor storage address is being maintained in the buffer, the channel writes the data to the high-speed buffer and processor storage is not modified. Otherwise, the data is written to processor storage only.

When a channel reads data (output operation to an I/O device), the buffer directory is interrogated, and if the required data is in the buffer and valid, it is read from the buffer and presented to the channel. If the buffer does not contain the required data, the channel reads the data from processor storage and the buffer is not modified.

The store-in approach used for the high-speed buffers in 4381 Processors is like that used in 4341, 4331 Model Group 2, 4361, 308X, and 3090 processors but contrasts with the store-through approach used in the high-speed buffers in System/370 and 303X processors in which processor storage is altered whenever data is stored in the buffer. The store-in approach reduces the number of accesses to processor storage, since changed buffer data is written to processor storage only if it must be replaced by another block (or when a buffer purge is required). The store-in approach becomes more and more advantageous as the difference between processor storage and high-speed buffer storage cycle times becomes greater.

Buffer reconfiguration, which is not implemented in 4341 Processors, is standard in 4381 Processors. If a double-bit error occurs during the loading of a buffer block, the load is tried once more. If the error is not corrected, buffer reconfiguration is done, if possible, as part of the instruction retry function. The buffer array in Model Groups 12, 13, and 2 contains spare space that is used for reconfiguration purposes.

When an uncorrectable storage error occurs in a byte in a buffer block, space in the reconfiguration area is allocated and a bit is set to indicate the reconfiguration area is to be used for this buffer block. The buffer load is retried and operations continue using the reconfiguration area for that buffer block if the load is successful.

If a load is not successful after the reconfiguration (assigned reconfiguration array location is malfunctioning), the buffer block location that caused the error can no longer be used and the malfunctioning bit in the directory entry for the malfunctioning block is turned on. The operator is notified that degradation is occurring and system operation continues.

Up to eight buffer block errors can be reconfigured as long as no more than one error occurs in a given byte position within a doubleword. When this limit is reached, the operator is notified that the buffer should be repaired.

Reconfiguration is also attempted for errors that occur in the swap buffer. A substitute array for the swap buffer is provided and, as for the high-speed buffer, up to eight errors can be reconfigured as long as no more than one error occurs in a given byte-pair position within a 16-byte data entry in the array. If the reconfiguration limit is reached or an error occurs in a reconfigured byte position of the swap array, the operator is notified that repair is required.

Operation of the entire high-speed buffer cannot be disabled in a 4381 Processor. However, utilization of an individual buffer block can be disabled by turning on the

malfunctioning bit in the associated directory entry, as is done when reconfiguration is not possible.

## 20:15 Support Processor Subsystem

### Components and Functions

The support processor subsystem provides basic operational functions for 4381 Processors and is the primary maintenance tool for diagnosing hardware malfunctions. It is designed to maximize total system availability and to provide rapid fault location and repair, where possible.

The components of the support processor subsystem are the support processor, support bus adapter, local channel adapter, console attachment adapter and attached devices, power adapter, power information panel, common communications adapter for the Remote Support Facility, and two system diskette drives and associated adapters.

While the support processor subsystem in 4381 Processors has the same types of functional components as those in 4341 Processors, certain of the physical components in this subsystem in 4381 and 4341 Processors are not the same. Specifically, the support processor in 4381 Processors is different. It is faster and more reliable (because of more dense technology) than that in 4341 Processors and has twice the storage capacity. The 4381 support processor is implemented on one card (the 4341 support processor requires four cards) and is program compatible with the 4341 support processor. In addition, a number of support logic cards have been eliminated or reassigned to make the support processor subsystem more efficient and to aid in easier fault location. A dump-to-diskette button on the processor control panel on the 4381 Processor can be used to dump the contents of support processor storage to diskette (functional diskette 2). This dump information can be sent to the IBM Support Center for analysis when error history is required to aid in problem determination.

The same two-sided diskettes (with a 1M-byte capacity) are used in 4381 and 4341 Processors but a different diskette drive is used in 4381 Processors and there are two diskette drives in the 4381 instead of one. The two diskette drives in a 4381 Processor fit in the same space as the single diskette drive in a 4341 Processor. Two diskette drives are required in a 4381 Processor in order to support System/370-XA mode of operation. The second diskette drive also allows some Problem Analysis routines to be kept online for operator use to avoid diskette changing.

In addition, communication between the support processor and the instruction processing function has been improved in 4381 Processors when compared with the 4341 implementation (see discussion under "Support Bus Adapter" in this subsection).

The microcoded support processor controls the operation of the support processor subsystem. The support processor subsystem is responsible for the following:

- System initialization functions (IML and IPL), including microcode loading for the support processor and instruction processing function
- Manual control functions for the operator and customer engineer (such as instruction step mode, address compare mode, alter/displays)
- Control of the two system diskette drives
- Control of the I/O devices that natively attach to a 4381 Processor via the console attachment adapter. These devices include the operator console display and up to three additional display consoles and/or printers.
- System I/O configuration definition for System/370 and System/370-XA modes
- Analysis of logout data, the writing of processor logout data and analysis information (reference code) to functional diskette 1 after an error is detected, initiation of a retry of retryable instructions and interruptions after an error occurs, and reconfiguration when an uncorrectable error occurs in a reconfigurable component
- Diagnostic program loading and execution
- Microcode-controlled power sequencing, power monitoring to detect under- and over-voltage conditions, and temperature monitoring
- Control of the Remote Support Facility and the Remote Operator Console Facility

Operation of the support processor is independent of, and overlapped with, operation of the instruction processing function for certain of its functions. During system operation, while instruction execution occurs, the support processor controls the operation of the natively attached display consoles and printers. It also performs power and temperature monitoring under microcode control and, when necessary, logging of environmental conditions to functional diskette 1.

Whenever a machine check condition occurs, the instruction processing function stops and the support processor receives control to initiate an instruction retry operation or machine check interruption in the instruction processing function, as appropriate. While the instruction processing function is operating, the support processor logs the error to functional diskette 1 and performs error diagnosis using the logout data to generate a reference code.

Details about the last four functions listed for the support processor subsystem are covered in Section 60. Manual control functions are discussed in Section 40. The other functions are discussed in the remainder of this subsection.

## System Diskette Drives

The two system diskette drives are small read/write drives, located in the front of the 4381 Processor unit (as shown in Figure 9 on page 27) and accessible to the operator. They read removable prerecorded disk cartridges (diskettes). Recording is done on both sides of the diskette. Space is provided to the left of the diskette drives for diskette storage.

A power-on of a 4381 Processor causes the two system diskette drives to be turned on. Operation of the system diskette drives is controlled by the support processor and there are no I/O instructions or commands that a user program can execute to cause read or write operations to a system diskette drive.

Five diskettes are sent to each 4381 Processor installation. Two identical functional diskettes (one for backup) for each system diskette drive are provided in addition to the service diskette. The microcode on the functional diskettes is not installation-customized. Functional diskette 1 contains all the microcode required for a 4381 configuration operating in System/370 mode (instruction processing function and support processor microcode), the TEST BLOCK internal records, areas for logout data from the 4381 Processor, most Problem Analysis routines, some diagnostic programs, and error analysis programs.

Functional diskette 2 primarily provides support microcode and programming for System/370-XA mode. It contains the microcode required for a 4381 configuration operating in System/370-XA mode (all instruction processing function and that support processor microcode that is different for System/370-XA mode), the I/O configuration data sets, the I/O Control Program (IOCP), the Test Case Monitor, Problem Analysis diagnostics, and certain of the machine speed diagnostics for fault location (see additional discussion of the functional diskettes in Section 60).

For normal system operation, functional diskette 1 is mounted on system diskette drive 1 and functional diskette 2 is mounted on system diskette drive 2. This configuration permits a 4381 Processor to be IMLed for System/370 or System/370-XA mode of operation and permits the operator to execute Problem Analysis routines, if necessary, without changing diskettes.

Operation of a 4381 Processor in System/370 mode is possible if only one of the two diskette drives (either one) is functional. However, the malfunctioning diskette drive should be repaired as soon as possible because diagnostics cannot be executed with only one operational diskette drive. Two operational diskette drives are required in order to operate a 4381 Processor in System/370-XA mode.

When the functional diskettes are mounted on the system diskette drives, an IML of instruction processing function microcode can occur automatically after a power-on of a 4381 Processor is performed. The operator can establish this mode of operation using the operator console. If an IML for the instruction processing function is required thereafter, it can be performed using the operator console. Parity checking is used for reloadable control storage during processor operation.

A procedure exists that enables the customer engineer to temporarily patch the instruction execution function microcode in reloadable control storage or the support processor. Any patches made are also made to the microcode on the appropriate mounted functional diskette.

Note that when processor power is turned off, the data in support processor storage, processor storage, and control storage for the instruction processing function is lost, and an IML must be performed when power is turned on again.

Each functional diskette for a given 4381 Processor contains the processor serial number and is not portable from one 4381 Processor to another (since the serial number on the diskette is checked against the processor serial number during any IML and a mismatch causes termination of the IML procedure). The functional diskettes for a given 4381 Processor also contain I/O configuration information specific to that 4381 Processor (such as UCW assignments for System/370 and the I/O configuration data set for System/370-XA mode) that precludes portability.

The system diskette drives are also used for loading and executing diagnostic routines and are a basic debugging tool for the system. A comprehensive set of fault-locating diagnostic routines is supplied to each 4381 Processor installation on the service diskette. These routines can be loaded directly from system diskette drive 2 into the 4381 Processor and executed (see Section 60:15).

## System Initialization

When the power-on/IML pushbutton on the operator control panel is pressed, a microprocessor based (MBC) logic card is logically activated to power on the support processor, system diskette drives, and adapters connected to the I/O bus of the support processor.

Diagnostics resident in storage of the support processor are executed to test the operation of the support processor and the system diskette drives and adapters. If these tests execute successfully, the resident microcode for the support processor is loaded from functional diskette 1. Diagnostics that verify the correct operation of the console attachment adapter, operator console, and power controller adapter are then loaded into the support processor and executed. The power controller adapter is initialized if no errors occur.

When the bootstrap functions have completed successfully, the support processor loads its own control storage and reads the IML program for the instruction processing function from functional diskette 1. The path to the primary operator console is tested and finally the microcode-controlled power-on sequence for the balance of the 4381 Processor is initiated. The instruction processing function and channel hardware, Channel-to-Channel Adapter (if installed), and channel-attached I/O devices with their power control switch set to the remote position are powered on, in the sequence listed, by power-sequencing microcode.

Powering of the natively displays and printers must be done by the operator using the on/off switch on these units. The instruction processing function and the Channel-to-Channel Adapter can be powered off and on individually when CE mode is in effect. CE mode is established using a customer engineer panel that is located within the frames of the 4381 Processor.

If no errors occur during powering, instruction processing function hardware is initialized at the completion of the power-on sequence. The microcode for the instruction processing function is then loaded into reloadable control storage from functional diskette 1 or 2, as appropriate to the mode selected by the operator if the installation has established execution of an automatic IML at the successful

completion of a power-on. After completion of power-on and/or IML, the program load display is shown on the operator console.

## Natively Attached Devices

Up to four devices can be natively attached to a 4381 Processor via the I/O bus of the support processor. The natively attached devices attach to channel 0 in 4381 uniprocessors and to channel 0 in channel group 0 in 4381 dual processors via the local channel adapter. The following devices can be natively attached:

- Required 3205 Color Display Console, 3278 Display Console Model 2A, or 3279 Color Display Console Model 2C
- Up to three additional devices, which can be any combination of 3205, 3278 Model 2A, and 3279 Model 2C consoles, 3268 Printers Model 2, 3268 Color Printers Model 2C, and 3287 Model 1, 1C, 2, and/or 2C Printers with the exception that 3205 displays cannot be installed in a 4381 configuration that contains a 3278 Model 2A or 3279 Model 2C display

The additional 3205, 3278 Model 2A, or 3279 Model 2C displays can be used as alternate and/or additional consoles, as supported by the operating system utilized. The 3287 and 3268 Printers can be used for hard-copy backup of the 3205, 3278 Model 2A, or 3279 Model 2C displays. The 3287 Printer is a desktop printer with a print speed of 80 characters per second (Models 1 and 1C) or 120 characters per second (Models 2 and 2C). The 3268 Printer provides faster printing (up to 340 characters per second). The 3287 Models 1C and 2C and the 3268 Model 2C provide printing in colors.

## Support Bus Adapter

The support bus adapter provides an interface between the support processor and the instruction processing function and channel hardware. Via this direct path, the support processor can access maintenance hardware (maintenance logic chips) in the instruction processing function and channels.

This interface enables the support processor to perform scan-in operations to initialize logic and scan-out operations to obtain status information after an error is detected during processor operation (see discussion of scan-in, scan-out, and scan rings in Section 60:10). The scan-in and scan-out facilities are used by maintenance programs to isolate faults and verify repairs. The support processor also issues commands (such as start clocks and stop clocks) to the maintenance chips via the support bus adapter interface.

The support bus adapter also provides an interval timing facility for power-monitoring microcode in the support processor. This adapter also drives the system and wait indicators and the lamp test switch on the switch on the operator control panel.

Implementation of the preceding functions is the same in 4381 and 4341 Processors. However, in 4381 Processors the support bus adapter is also used for microcoded communication between the instruction processing function and the

support processor. The scan-in and scan-out functions are used to transfer data between the two components, for example, data or programs read by the support processor from a diskette drive (such as the TEST BLOCK internal records, I/O configuration data set, and Input/Output Configuration Program). In 4341 Processors, the local channel adapter interface is used for such communication.

In addition, the 4381 instruction processing function can set an interrupt for the support processor to indicate its services are needed (for example, a state change occurs, such as a machine check that requires a scan-out). This eliminates polling by the support processor, as is done in 4341 Processors.

Communication between the operating system and the operator (via the operator console) is handled via the local channel adapter in 4381 Processors, as in 4341 Processors. However, since the local channel adapter is not used for communication between the instruction processing function and the support processor, communications problems between these components that can arise in a 4341 Processor when channel 0 is in a hung condition do not arise in a 4381 Processor.

## 20:20 Channels

### General Description

The 4381 Processors implement advanced channel functions like those implemented in 4341 Processors, such as block multiplexing and data streaming, and also offer more channels and higher aggregate channel data rates than do 4341 Processors.

One standard and one optional channel group are provided for all uniprocessor 4381 model groups. The standard channel group consists of one byte multiplexer channel, addressed as channel 0, and five block multiplexer channels, addressed as channels 1 through 5. Channel 5 can be configured as a byte, instead of a block, multiplexer channel. The optional channel group (Block Multiplexer Channels, Additional feature) provides six block multiplexer channels addressed as channels 6 through B.

A byte multiplexer channel in a 4381 Processor can handle the concurrent operation of multiple slower speed devices when operating in byte interleave mode, while a block multiplexer channel can support interleaved, concurrent execution of multiple high-speed channel programs.

Each installed byte or block multiplexer channel can have up to eight control units attached. For byte multiplexer channel 0, one control unit position is used by the local channel adapter. This internal adapter provides attachment of support processor subsystem devices to this byte multiplexer channel. As a standard feature, automatic control unit powering is provided for up to 32 control units attached to a 4381 Processor.

Comprehensive error checking is incorporated in the basic design of the channel hardware. Checking is performed on the control logic in most areas, and standard

parity checking is done on the data flow between the channels and the instruction processing function.

For System/370 mode of operation, the fast release function of the START I/O FAST RELEASE (SIOF) instruction is implemented in 4381 Processors as is queuing of SIOF instructions. These two functions are inherent in the design of the channel subsystem for System/370-XA mode of operation. These facilities reduce the instruction processing function processing time required for an SIOF instruction when compared with the time required for a START I/O (SIO) instruction.

Optionally, one Channel-to-Channel Adapter can be installed in a 4381 Processor and attached to any block multiplexer channel. The other channel to which the adapter is attached can be contained in another 4381 Processor or a System/360, System/370, 30XX, 4341, 4361, 4331, or 4321 processor. Three control unit positions on each channel and one nonshared UCW for each of the two channels interconnected via the 4381 Channel-to-Channel Adapter are required. The adapter operates in burst mode and transfers data at the rate of the lower speed channel to which it is attached.

The Channel-to-Channel Adapter provided for 4381 Processors is functionally equivalent to the adapter provided for System/370 and 4300 processors but is implemented in a higher density technology that reduces its size.

The 3088 Multisystem Channel Communication Unit can also be used to interconnect 303X, 308X, 3090, 4341, and 4381 processors via block multiplexer channels.

## **Device Addresses and Unit Control Words For System/370 Mode**

The byte multiplexer channel and each block multiplexer channel installed in a 4381 uniprocessor model group can have 256 device addresses (00 to FF). Any device addresses can be used for block multiplexer channels 1 through B or for channel 5 when it is a byte multiplexer channel. For byte multiplexer channel 0, addresses 0F0 to 0FF are reserved for support processor subsystem devices attached via the local channel adapter and any device addresses other than these can be used for the I/O devices attached to the byte multiplexer channel via external control units. Thus, only 240 device addresses (000 to 0EF) can be assigned to user devices natively attached to channel 0 or via external control units.

A 4381 Processor can have a minimum of 128 and a maximum of 2048 UCWs as a standard feature for System/370 mode of operation. UCWs are allocated by the customer engineer or operator, using the display console. UCWs above 128 are allocated in groups of 64. Each UCW is 64 bytes in size and resides in auxiliary storage. Each group of 64 UCWs requires 4K bytes of storage. Thus, a minimum of 8K bytes and a maximum of 128K bytes are required for UCW storage.

The UCWs allocated are assigned a three-digit reference number 000 to N-1, where N is the number of UCWs allocated. UCWs with the reference numbers 000 to 020 are reserved for internal functions (support processor, for example) and support subsystem devices. In addition, each channel is assigned one channel-shared UCW that is used to present asynchronous interruptions for any I/O devices attached to the channel that are not allocated a UCW (defined to the system).

The UCWs defined can be assigned to any of the channels actually present in the 4381 Processor. A maximum of 256 UCWs can be assigned to any one channel. The customer engineer or operator assigns UCWs to specific channel addresses using the operator console. Each UCW can be designated as shared or nonshared.

A shared UCW can be used by a set of devices, one device at a time. A shared UCW generally is assigned to a control unit that has multiple devices attached, only one of which can be in operation at a time. A nonshared UCW is one that is assigned to only one device. A nonshared UCW is designed for use with a control unit that has only one I/O device attached or that has multiple I/O devices attached that can operate concurrently.

A channel directory for each channel is allocated in auxiliary storage. Each channel directory has 256 entries, one for each of the possible device addresses for a channel. A directory entry indicates whether a UCW is assigned to the associated device address, characteristics of the assigned UCW, and characteristics of the device assigned the associated device address.

A channel directory entry contains the following:

- Reference number of the UCW assigned (all device addresses have a UCW assigned)
- Assigned bit to indicate whether an I/O device is defined for the associated device address
- An indication of whether the UCW is shared or nonshared (shared bit)
- An indication of whether the associated device operates in byte multiplexer mode
- An indication of whether the associated device must operate in selector mode rather than block multiplexer mode
- An indication of whether the device is attached to a control unit that is to use the START I/O FAST queuing function
- An indication of whether the associated device is attached to a control unit that is capable of operating in data streaming mode
- An indication of the mode in which channel 5 is to operate (byte or block multiplexer)

Devices attached to a block multiplexer channel that are capable of block multiplexing should have the shared and selector mode bits off in their channel directory entry to indicate allocation of a nonshared UCW that is capable of disconnecting. For devices attached to a control unit that is capable of data streaming mode of operation (such as a 3880 storage director), the directory entry should have the data streaming mode bit on.

The customer engineer or installation operator can select displays associated with UCWs. The functions provided by the UCW displays enable the customer engineer/operator to display the allocated UCW reference numbers and the device addresses they are assigned, and to display and alter the attributes of the UCWs.

The alter capability is used to change device addresses and attributes assigned to UCWs. The UCWs for the natively attached displays/printers are preassigned.

Device addresses for natively attached and all other I/O devices and UCWs for devices that are not natively attached must be selected during installation. If a UCW assignment is changed, it becomes effective during the next IML, unless it is for a natively attached device. Changes to UCWs for natively attached devices become effective immediately.

The channel directory entry for each device address for which a device has not been assigned (assigned bit is off) has a UCW assigned. All the device addresses without an assigned I/O device for the same channel have the same channel-shared UCW assigned. Thus, if an I/O device exists in a 4381 configuration but has not been defined as part of the I/O configuration, the shared UCW is used to present any status information that may be generated by the undefined device. However, if any I/O instruction is issued to an undefined device, a not operational condition code is generated for the I/O instruction.

## **Subchannels For System/370-XA Mode**

For System/370 extended architecture mode of operation, a byte or block multiplexer channel can have a maximum of 256 device addresses assigned, as for System/370 mode, and the same channel device addresses (0F0 to 0FF) are reserved for system use. Up to 2049 subchannels (2048 plus 1 for microcode usage) can be defined, each of which requires 128 bytes in auxiliary storage. In addition, each physical control unit attached to a 4381 Processor (up to 256 plus 1 for microcode usage) requires 70 bytes of auxiliary storage.

A channel directory for each channel is allocated in auxiliary storage. There are 256 directory entries per channel. A directory entry is four bytes in size and contains subchannel numbers and path management (control unit and device) information.

For System/370-XA mode of operation, the installation-defined I/O device configuration resides in a data set on functional diskette 2 called the I/O configuration data set. This data set is accessed by the support processor during IML to construct the I/O portion of auxiliary storage. The I/O configuration data set is not accessed thereafter during normal system operation.

When a 4381 Processor is shipped, an initial I/O configuration data set is provided on functional diskette 2. This initial version defines only the I/O configuration required for customer engineer checkout of the 4381 system. It does not define enough I/O devices to enable an MVS/XA system generation to be performed.

An I/O configuration data set that specifies the customer-defined I/O configuration for the particular 4381 Processor being installed must be created using the IBM-supplied I/O Configuration Program (IOCP). The IOCP is also used after initial installation of a 4381 Processor to make changes to the I/O configuration data set to reflect any alteration of the installed I/O configuration.

The IOCP for 4381 Processors is a stand-alone program and requires the 4381 Processor to be operating in System/370 mode. It is supplied on functional diskette 2 and is executed using the operator console for control and specification

of I/O devices. This is a different IOCP from that provided for 308X configurations, but it essentially provides the same functions (creation of I/O configuration data sets and report printing).

The IOCP is used to create the initial I/O configuration data set at installation of a 4381 Processor before an operating system that supports System/370-XA is installed. Input to the IOCP that describes the I/O configuration must be provided by the installation but the customer engineer will actually create the initial I/O configuration data set as part of the installation process if so requested.

Input to the 4381 IOCP consists of definition statements in 80-column card-image format. This input can be entered from a card reader, a magnetic tape unit, or the system console. For MVS/XA installations, the IOCP definition statements can be maintained as a separate data set or included in the Stage I input to the MVS/XA system generation procedure. For VM/XA installations, a separate set of IOCP statements must be maintained (they cannot be combined with VM/370 system generation statements).

MVS/XA support of 4381 Processors includes acceptance of the IOCP definition statements as the I/O definition portion of the input to Stage I of the MVS/XA system generation procedure. The MVS/XA system generation procedure will accept either the IOCP channel definition statement (CHPID macro) or its own CHANNEL macro (but not both types in the same input) as the channel-defining statements. The MVS/XA system generation procedure will ignore any parameter on an I/O definition statement that applies only to the IOCP (CUNUMBER, for example) as well as the IOCP ID and CNTLUNIT macros.

The IOCP will accept the existing Stage I input to the MVS/XA system generation procedure from which all CHANNEL statements have been removed and all required IOCP statements and parameters have been added. The IOCP will ignore non-I/O definition MVS/XA generation statements contained in the Stage I input (CTRLPROG, GENERATE, for example) and unknown keywords on I/O device defining statements unless instructed to flag them as errors.

Therefore, 4381 installations with MVS/XA installed need create and maintain only one input data set for both the MVS/XA system generation procedure and I/O configuration data set processing using the IOCP. A common input also eliminates the chance of inconsistencies between the I/O configuration definition for the hardware and that for the MVS/XA operating system.

The IOCP permits channels and I/O devices that can be included in a 4381 configuration but that are not installed in the 4381 configuration to be defined in the input. This permits one system generation deck to be used as input to the IOCP, the system generation for the 4381 configuration, and the system generation for another system in the installation (for example, a 303X, 308X, or 3090 Processor Complex with more channels and/or I/O devices).

The IOCP is used to write a new I/O configuration data set on functional diskette 2 using the supplied I/O configuration definition statements. The entire set of definition statements must be supplied even if all that is required is alteration of one or more existing definition statements. The existing I/O configuration data set is deleted and a new one is written using the supplied input. The IOCP does not support actual modification of an existing I/O configuration data set. If no catastrophic errors are detected in the input, the I/O configuration data set is written if desired.

The IOCP also provides four types of configuration reports. These reports are written to a printer. The Channel Path Summary Configuration Report lists the channel paths defined in the I/O configuration data and the mode of operation for each listed channel path. The Channel Path Configuration Report provides the information given in the channel path summary report plus the control units and devices assigned to the channel path. Other information, such as the mode of operation (data streaming or DC interlock) used by the control units attached to each channel, is also given.

The I/O Device Configuration Report lists the I/O devices defined together with their characteristics and attachment to the 4381 Processor (control unit and channel paths and subchannel type assignment, for example). The Logical Control Unit Report shows how IOCP has grouped control units and I/O devices for performance data gathering.

Two different I/O configuration data sets can be present on functional diskette 2. The two I/O configuration data sets are physically identified as data sets 0 and 1. One I/O configuration data set is designated the currently active I/O configuration data set using the operator console. The currently active data set is read when the auxiliary storage area must be built.

Information about the IOCP is contained in *IBM 4381 Processor Input/Output Configuration Program User's Guide and Reference Manual*, GC24-3964.

## General Operation of the Channels

The channels in 4381 Processors are microcode- and hardware-controlled. Operationally, they are integrated channels and, thus, share the use of certain hardware with the instruction processing function, such as the arithmetic logic unit, byte shifter, and control storage.

The general flow of data between I/O devices and processor storage via the channels in 4381 Processors is shown in Figure 10 on page 53. This data flow is the same as in 4341 Processors. Each installed channel has an interface controller that contains a data-in and a data-out register for transferring data between the standard I/O interface to I/O devices. All the interface controllers can be transferring data to I/O devices (one device per controller) at the same time.

Data is transferred between the individual interface controllers and the channel data buffer via a channel-in and channel-out register, each of which is two bytes in size. One or two bytes are transferred at a time. The channel data buffer contains one 256-byte buffer area for each channel. Only one channel can be transferring data to, or receiving data from, the channel data buffer at a time. A set sequence for handling channel requests is implemented in the channel control hardware.

Data is transferred between a buffer area in the channel data buffer and processor storage via the eight-byte data transfer register and the eight-byte shifter, which is in the instruction processing function. This data transfer is microcode-controlled. The shifter provides doubleword boundary alignment for data entering processor storage, when required, and any needed alignment for eight bytes of data entering the channel data buffer.

A data transfer between processor storage and the channel data buffer handles 64 bytes aligned on a 64-byte boundary, except for beginning and ending transfers for a processor storage buffer that is not located on a 64-byte boundary. A 64-byte data transfer requires 1.9 microseconds in a Model Group 1, 2, 3, 11, or 12 and 1.7 microseconds in a Model Group 13 or 14 4381 Processor.

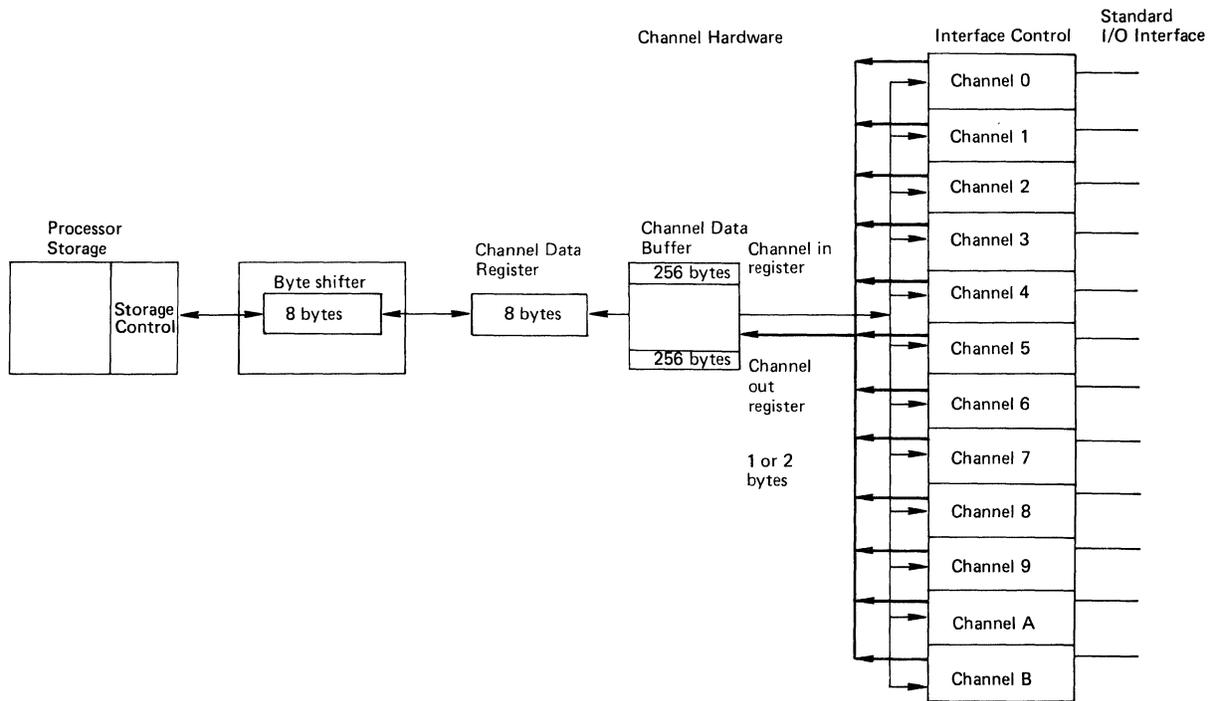


Figure 10. General flow of data between the channels and processor storage

Channel control hardware determines the priority for servicing the channels according to predetermined priorities. When multiple channel trap requests (requests for microcode service) are outstanding, the lowest numbered channel with an outstanding request is serviced first. A trap request for this channel will not be serviced again until the other channels with a request outstanding have one trap request serviced. That is, each channel is guaranteed not to have to wait for the servicing of more than an average of five (if the optional channels are not installed) or eleven other trap requests between the servicing of two successive trap requests of its own (each channel is guaranteed, on an average, every fifth or eleventh trap service).

The channels are given priority over the instruction processing function for access to shared facilities. The channels interfere with instruction processing function operation when a channel trap request is serviced. Trap requests occur for such operations as data transfer between processor storage and the channel data buffer, processing of a UCW, command chaining, data chaining, and status handling.

A 4381 Processor generates less total interference with instruction execution than a 4341 Processor because half the amount of time is required to transfer a byte of data between processor storage and the channel data buffer during an I/O operation (64 bytes are transferred in 1.9 microseconds in a 4381 uniprocessor versus four microseconds in a 4341 Processor).

The channels in 4381 Processors do not prefetch CCWs (channel control words) for input operations. For output operations, a CCW, an IDAW (indirect data address word), or data can be prefetched.

A reconfiguration function is implemented for the channel data buffers. This function is invoked by the instruction retry facility when an uncorrectable hardware failure occurs during a write from a channel data buffer. Two additional channel data buffers are associated with each channel group. One of the spare two buffers for a group can be substituted for a failing channel data buffer in the first channel group, while the other can be substituted for a failing channel data buffer in the second channel group.

At any time, two malfunctioning channel data buffers can be reconfigured. The four spare channel data buffers can be reconfigured to handle two failing channel data buffers in either channel group or one failing channel data buffer in each channel group. If one of the allocated spare channel data buffers malfunctions, one of the other two spares can be assigned.

The operator is not notified when a channel data buffer is reconfigured and no performance degradation occurs. If a third channel data buffer fails after reconfiguration has been done for two other malfunctioning buffers, a channel data check error is reported for the affected I/O operation as would be done if reconfiguration were not implemented.

## Byte Multiplexer Channels

The byte multiplexer channel for 4381 Processors is functionally identical to the byte multiplexer channel for System/370, 30XX, and other 4300 processors. A byte multiplexer channel can operate in byte interleave mode to permit several slower speed I/O devices to operate concurrently or in burst mode to permit one buffered device to operate. Unbuffered burst mode devices that are subject to data overrun, such as magnetic tape units, cannot be attached to a byte multiplexer channel in a 4381 Processor.

For byte multiplexer channel input operations in a uniprocessor 4381 model group, a maximum of up to 2 Mb/sec for channel 0 or 5 is possible for a burst mode operation involving a buffered device. The output rate for burst mode buffered devices equals the device rate in Mb/sec divided by 1 plus the device rate in Mb/sec for device rates less than or equal to 2 Mb/sec. These data rates assume small interface and control unit generated delays.

The data rate for byte mode operation depends on other channel activity and the number of bytes transferred per burst. For one-byte transfers, the maximum data rate is 24Kb/sec for 4381 Model Groups 11, 12, 13, 1, and 2. For two-byte transfers, 48Kb/sec is the maximum data rate, while for four-byte transfers a maximum data rate of 96Kb/sec is possible. The maximum data rates can be achieved only when there is no activity on any other channel or a console device.

For byte multiplexer channel data rates when there is activity on other channels, see *IBM 4381 Processor Channel Characteristics*, GA24-3948.

I/O devices in the support processor subsystem attach to byte multiplexer channel 0 via the local channel adapter, which occupies the last control unit position on this channel. Thus, a maximum of seven external control units can be attached to byte multiplexer channel 0 in a uniprocessor.

The local channel adapter operates like a channel-to-channel adapter that connects the I/O bus of the support processor to channel 0. The local channel adapter provides a low-cost method of attaching support processor subsystem devices to byte multiplexer channel 0.

The local channel adapter appears as a shared control unit that can have multiple device addresses. It operates in multibyte mode in the 4381 Processor. Data is transferred from the local channel adapter to the byte multiplexer channel two bytes at a time.

## Block Multiplexer Channels

The block multiplexer channels in a 4381 Processor can operate in block multiplexer or selector mode. When operating in selector mode of block multiplexer mode, a block multiplexer channel in a 4381 Processor is functionally equivalent to a selector or block multiplexer channel in System/370, 30XX, and other 4300 processors. A block multiplexer channel presents a standard I/O interface and can have a maximum of eight control units attached.

The table below shows the maximum individual block multiplexer channel data rate for each permissible channel in each uniprocessor 4381 configuration as well as the maximum aggregate data rate of each channel group and the 4381 system. All figures are Mb/sec.

4381 Model Group	Standard Block Multiplexer Channels					Maximum Aggregate Standard Group	Optional Block Multiplexer Channels						Maximum Aggregate Optional Group	Maximum Aggregate System
	1	2	3	4	5		6	7	8	9	A	B		
11	3	3	3	3	2	14	2	2	1	1	1	1	8	22
12	3	3	3	3	2	14	3	3	1	1	1	1	10	24
13	3	3	3	3	2	14	3	3	3	3	3	1	16	30
1	3	3	3	3	2	14	2	2	1	1	1	1	8	22
2	3	3	3	3	2	14	2	2	1	1	1	1	8	22

Like a byte multiplexer, a block multiplexer channel can have multiple subchannels, each of which can support one I/O operation. The setting of a channel mode bit (0) in control register 0 determines whether the addressed subchannel of a block multiplexer channel operates in block multiplexer mode (assuming it is capable of operating in block multiplexer mode) or selector mode when a start instruction is issued. The mode bit is set to 0 (selector mode) at IPL and can be altered by programming at any time.

## Data Streaming Mode

Data streaming mode of operation is standard for all the block multiplexer channels present in a 4381 Processor. Data streaming mode enables certain 4381 block multiplexer channels to handle faster data rates and all 4381 block multiplexer channels to handle a longer channel-to-control-unit cable length. Specifically, a maximum channel-to-control-unit cable length of approximately 122 meters (400 feet) is supported for control units that are capable of operating in streaming mode and a data rate of up to 3 Mb/sec can be achieved for this cable length for channels 1 through 4 in uniprocessor 4381 model groups.

When a block multiplexer channel is capable of data streaming, both data streaming and nonstreaming control units can be attached to the block multiplexer channel. Control units that are capable of streaming must be set by the customer engineer to operate in streaming or nonstreaming mode for each I/O interface to which they are attached. In addition, control units set to operate in streaming mode must be allocated UCWs (for System/370 mode of operation) that are assigned streaming mode. Nonstreaming control units connected to a channel that is capable of streaming are still subject to their normal maximum channel-to-channel-unit cable length and operate at their usual rated speed.

The following can be set to operate in data streaming mode:

- 3880 Storage Control (all models)
- 3848 Cryptographic Unit with the appropriate EC installed
- 3838 Array Processor with the optional Data Streaming feature installed (to permit operation at 3 Mb/sec)
- 3088 Multisystem Channel Control Unit

For a 3880 unit, the use of streaming or nonstreaming mode is set for each channel to which the two storage directors are attached. Thus, when no channel-switching feature is installed, a storage director always operates in the mode, streaming or nonstreaming, set for the channel to which it is connected. When channel switching is installed the mode of operation, streaming or nonstreaming, is set for each channel to which the storage director is attached, and the storage director can operate in streaming mode for some channels and nonstreaming mode for others, if necessary.

For a 3880 Model 1 or 2 with 3330-series, 3340/3344, 3350, 3370, or 3375 drives attached, each storage director can be set to operate in streaming or nonstreaming mode. The maximum channel-to-control-unit cable length for a 3880 Model 1 or 2 with 3330-series, 3340/3344, or 3350 drives attached is 122 meters (400 feet) for both streaming and nonstreaming mode of 3880 operation when the 3880 is attached to a 4381 Processor.

The maximum channel-to-control unit cable length for a 3880 Model 1, 2, or 4 with 3370 or 3375 drives attached is 61 meters (200 feet) for nonstreaming mode and 122 meters (400 feet) for streaming mode of 3880 operation when the 3880 is attached to a 4381 Processor.

A 3880 Model 2 or 3 storage director with 3380 devices attached must be attached to channel with a 3 Mb/sec data rate in a 4381 Processor and operate in data

streaming mode. The Speed Matching Buffer for 3380 feature can be installed on the storage director but the data rate supported is still 3 Mb/sec. Operation of 3380 Direct Access Devices at a 1.5 Mb/sec data rate using the speed matching buffer is not supported for the 4381 Processor. The maximum channel-to-control-unit cable length is 122 meters (400 feet).

## **SIOF Instruction For System/370 Mode**

The fast release function of the SIOF instruction and queuing of SIOF instructions that are issued to a busy block multiplexer channel or control unit are designed to reduce the time required to start I/O operations. These two facilities are always active. However, the queuing facility must be specified for those control units for which it is to be effective.

SIOF instruction fast release and queuing can be done only for control units attached to block multiplexer channels (not for control units attached to byte multiplexer channels). SIOF queuing is done only for devices that have a nonshared subchannel assigned (not for shared subchannels). An SIOF instruction that is issued to a byte multiplexer channel or to a block multiplexer channel operating in selector mode is executed as an SIO instruction.

Up to eight control units per channel can be configured for queuing. When a control unit is configured for SIOF queuing, the range of device addresses for which queuing is to be active must be specified. To ensure the correct operation of SIOF queuing, the entire range of addresses that the control unit can recognize as plugged by the customer engineer (for example 8, 16, or 32 for 3830 Model 2 Storage Control or a 3380 storage director) must be specified, even if fewer than the maximum number of I/O devices are actually attached to the control unit. For the 3850 Mass Storage System, possible real and virtual address ranges must be specified for each control unit. This address specification requirement permits the SIOF queuing facility to handle all control unit end conditions (which can be presented using any device address that is associated with a control unit).

When a string of direct access devices can be switched between two control unit functions, two device address ranges (one for each control unit function) should be specified as usual. The specification of one device address range for one control unit that covers the range of addresses available to both control units will cause performance degradation.

The fast release and queuing functions are performed by channel microcode. Channel, control unit, and device queues are maintained. Space is allocated in auxiliary storage to support the queuing function.

Processing of an SIOF instruction for which fast release and queuing can be done is handled as follows by channel microcode. The status of the channel specified is determined. If the channel is busy, the status of the required subchannel is determined. If the subchannel is already in use or already queued, a condition code 2 (busy) is presented for the SIOF instruction and the request is not queued. If the subchannel is available when the channel is busy, the request is placed at the end of the channel queue and a condition code of 0 (request accepted) is generated. The instruction processing function then resumes processing.

If the requested channel is available, the channel microcode attempts to start the I/O operation to the specified channel, control unit, and device. If the status returned from initial device selection indicates the path is available, condition code 0 is presented, since the I/O operation has been started. If control unit busy status with no errors is returned, the request is placed at the end of the control unit queue and condition code 0 is presented. If any error status is returned for the control unit, no queuing is done and condition code 1 (CSW stored) is returned. If the required control unit is available but the specified I/O device is busy, the request is placed on the device queue. The instruction processing function resumes processing after the appropriate condition code has been generated.

Dequeuing of requests is done when the channel becomes available (a device disconnects), control unit end occurs, or device end occurs. When the no-longer-busy condition is received, all requests on the associated queue (channel, control unit, or device) are moved to a list for that channel and the operations will be redriven as soon as the current System/370 instruction is completed.

When an I/O operation terminates, a delay code is stored at location 185 in processor storage to indicate the busy condition (channel, control unit, or device) encountered, if any, when the SIOF instruction was first processed.

## 20:25 Standard and Optional Features

### Standard Features

The following are standard features of 4381 Model Group 11, 12, 13, 1, and 2 Processors that are operative for both System/370 and System/370-XA modes:

- Binary arithmetic
- BRANCH and SAVE instructions
- Byte-oriented operands
- Channel indirect data addressing
- Channels 0 through 5, which can be configured as one byte and five block multiplexer channels or two byte and four block multiplexer channels
- Command retry for block multiplexer channels
- Conditional Swapping
- Control Unit Powering (for up to 32 control units)
- CPU timer and clock comparator (one microsecond resolution)
- Data Streaming for all installed block multiplexer channels
- Decimal arithmetic
- Dual Address Space Facility
- ECC on processor storage and error correction for certain double-bit errors
- ECPS:MVS (tracing functions not implemented for System/370-XA mode)
- EC mode of operation
- Elementary Math Library Facility (Model Group 2 only)
- Expanded machine check interruption class
- Extended Addressing (Model Groups 12, 13, and 2 only)
- Floating-point arithmetic

- High-speed buffer storage—4Kb for the Model Group 11, 8Kb for the Model Group 1, 32Kb for the Model Groups 12 and 2, and 64Kb for the Model Group 13
- Instruction retry
- Interruption for SSM instruction
- Low address protection
- Mathematical Function Facility (Model Groups 12 and 13)
- Monitoring feature
- MOVE INVERSE instruction
- Multiply and Add Facility
- Problem Analysis
- Program event recording
- PSW key handling
- Reconfiguration functions
- Reference and change recording
- Reloadable control storage
- Square Root Facility (Model Groups 11, 12, and 13)
- Storage key instruction extensions (ISKE, RRBE, and SSKE instructions)
- Store and fetch protection (one key per 2K-byte block for up to 16Mb installed or one key per 4K-byte block for Model Group 12, 13, or 2 configurations with more than 16Mb installed)
- Store status
- Support processor subsystem
- System/370 Extended feature (common segment bit, INVALIDATE PAGE TABLE ENTRY instruction, low address protection, TEST PROTECTION instruction)
- TEST BLOCK instruction
- Time-of-day clock (one-microsecond resolution)

The following are standard features for 4381 Model Groups 11, 12, 13, 1, and 2 that operate only when System/370 mode is in effect:

- BC mode
- Block multiplexer control bit in control register 0
- Channel masks in control register 2
- Channel retry data in a limited channel logout area
- Dynamic address translation for 24-bit virtual and real addresses using 2K or 4K pages and 64K or 1024K segments
- ECPS:VM/370
- External signals
- Interval timer
- INSERT STORAGE KEY instruction
- Instructions for System/370 architecture (includes all defined except READ DIRECT, WRITE DIRECT, multiprocessing, RESUME I/O, and channel set switching instructions)
- Limited channel logout
- Machine check external damage code
- Preferred Machine Assist
- Recovery extensions
- RESET REFERENCE BIT instruction
- Segment protection
- SET STORAGE KEY instruction
- STORE CHANNEL ID instruction (and all other System/370 I/O instructions)

- SIOF instruction fast release and queuing (comparable facilities are inherent in the System/370-XA mode channel subsystem definition)
- VM Extended Facility Assist
- 128 to 2048 UCWs in increments of 64

The following are standard features for 4381 Model Groups 11, 12, 13, 1, and 2 that operate only when System/370-XA mode is in effect:

- Bimodal addressing
- Channel subsystem designed for System/370 extended architecture
- DIAGNOSE MSSFCALL instruction
- Dynamic address translation for 31-bit (or 24-bit) virtual and real addresses using 4K pages and 1024K segments
- Instructions for System/370 extended architecture (includes all defined for System/370 extended architecture)
- Page protection
- Sort assist
- Tracing
- Up to 2048 subchannels

## Optional Features

Optional features for 4381 Model Group 11, 12, 13, 1, and 2 Processors, all of which can operate with System/370 or System/370-XA mode in effect and can be field-installed, are:

- 3205 Color Display Console, 3278 Model 2A Display Console, or 3279 Color Display Console Model 2C (includes printer-keyboard mode for System/370 mode only and display mode for System/370 and System/370-XA modes)—required feature
- Block Multiplexer Channels, Additional (provides six block multiplexer channels)
- Channel-to-Channel Adapter (one maximum)
- Remote Operator Console Facility (specify feature—no charge)
- Remote Support Facility (recommended specify feature—no charge)

## Section 30: 4381 Processor Multiprocessor Model Groups

### 30:05 Configuration Description

The 4381 Model Groups 14 and 3 are dual processor configurations that implement tightly coupled multiprocessing. The 4381 Model Group 14 or 13 unit contains two instruction processing functions, each of which has its own dedicated set of channels. The channels attached to one instruction processing function cannot be accessed by the other instruction processing function. All processor storage in the 4381 processor unit is shared by the two instruction processing functions. The 4381 operates under the control of a single multiprocessing control program when operating as a dual processor with two executing instruction processing functions and supports the simultaneous operation of two tasks. System operation with two instruction processing functions is also possible if the channel subsystem of one instruction processing function fails.

The 4381 dual processor configuration cannot be partitioned into two independent uniprocessor systems. However, it can operate as a single uniprocessor configuration using either instruction processing function. Thus, 4381 system operation can continue with degraded performance if one instruction processing function is malfunctioning. When operating as a uniprocessor, the channels of the nonoperational instruction processing function cannot be accessed by the operational instruction processing function. Thus, the I/O configuration should be as symmetrical as possible with appropriate switching features installed, as discussed in Section 30:25.

The 4381 dual processor configuration is similar to the 3081 dyadic configuration but the 4381 does not have a system controller or external data controller and channels are dedicated to an instruction processing function. Thus, channel set switching is not implemented in a 4381 Processor.

The functional components physically contained within the frames of a 4381 Model Group 14 or 3 Processor are two instruction processing functions (addressed as 0 and 1), all processor storage (which is shared by the two instruction processors), one storage control function, two sets of channels (one dedicated to each instruction processor), and one support processor subsystem. Figure 11 on page 62 shows the logical components of a 4381 Model Group 14 or 3 Processor.

As shown in Figure 11 on page 62, each instruction processing function has its own control storage, high-speed buffer storage, storage control function, and support bus adapter. One channel set is dedicated to each instruction processing function but the local channel adapter is attached only to channel 0 of the channel

set for instruction processing function 0. Processor storage can be accessed by both instruction processing functions via the storage control function.

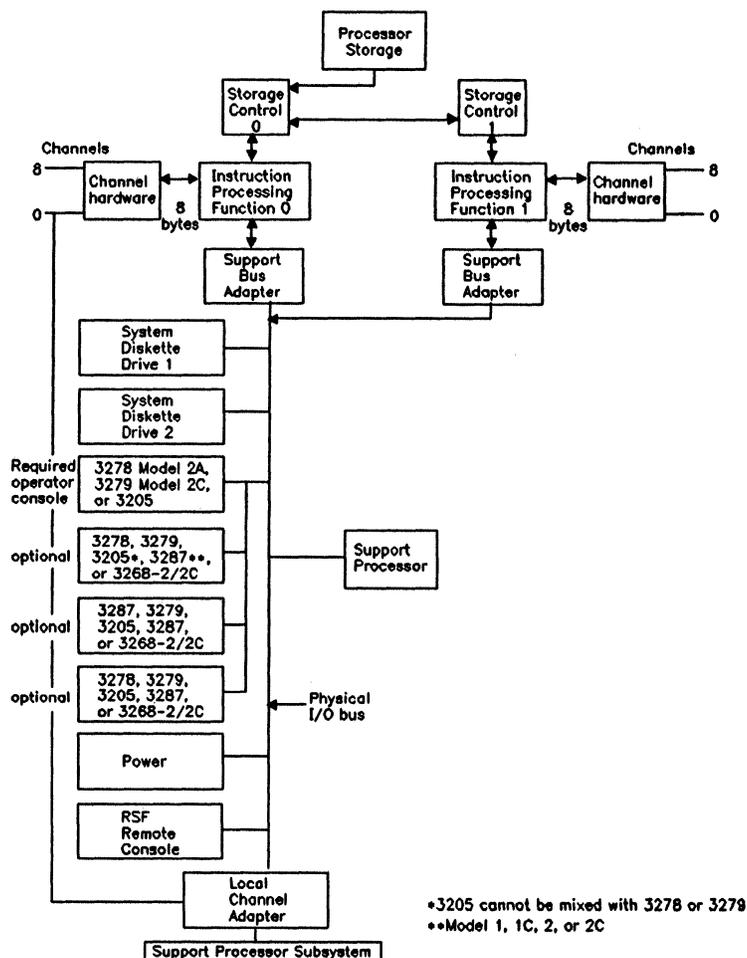


Figure 11. Logical components in a 4381 Processor Model Group 14 or 3

The 4381 Model Group 14 or 3 can be initialized by the operator to operate as a uniprocessor. The 4381 Model Group 14 or 3 can also be set to operate as a uniprocessor during system operation by the Alternate CPU Recovery (ACR) facility of MVS or VM/370 after one instruction processing function becomes nonfunctional.

When ACR receives control it attempts to transfer work from the failing instruction processor to the operational instruction processor and tries to recover the tasks that were operational at the time of the failure. The channels of the failing instruction processor are reset to handle any outstanding I/O and reserve requests. An attempt is made to restart the operational I/O requests using channels in the group for the operational instruction processor. The failing instruction processor and its channel group are varied offline. No more I/O requests or tasks will be allocated to these components. If the primary console is attached to channel 0 of the failing instruction processor, the primary console function is switched to an alternate console attached to channel 0 of the operative instruction processor if such a console is available.

## 30:10 Instruction Processing Function

### General Description

Each of the two instruction processing functions in a 4381 Model Group 14 or 3 contains all the elements necessary to decode and execute the instructions in the instruction set for 4381 Processors. I/O instructions are partially processed by the instruction processing function and partially processed by channel hardware. Extensive parity checking is done within the instruction processing function to ensure data validity.

All instruction execution functions and most channel operations are microcode controlled. Microinstructions are four bytes in length. Reloadable control storage for the residence of instruction processing function microcode is standard in each instruction processing function.

Certain basic control and service functions are provided for 4381 Processors by the support processor, a component of the support processor subsystem, instead of by the instruction processing function. The support processor is a microcoded controller with its own control storage. The support processor also handles I/O operations for the operator console device and up to three other display consoles and/or printer devices that are directly attached to a 4381 Processor. In addition, the support processor controls diagnostic facilities (see discussions in Sections 30:15 and 60:15).

The two instruction processing functions in the 4381 Model Group 14 have a 56-nanosecond cycle time (68 nanoseconds for a Model Group 3) and are functionally identical. They are addressed as 0 and 1 and functionally like the instruction processing function in the 4381 Model Group 13, as described in Section 20:10 under "General Description," but have additional facilities to support tightly coupled multiprocessing. The Model Group 3 instruction processing functions are like the Model Group 2 instruction processing function.

The following facilities are implemented in a 4381 Model Group 14 or 3 to support multiprocessing:

- Prefixing – a method of assigning unique areas of processor storage to addresses 0 to 4095 for each instruction processor. The SET PREFIX and STORE PREFIX instructions are provided.
- Processor addressing and STORE CPU ADDRESS instruction – required to specifically identify each instruction processor. The instruction processor address (0 or 1) is stored during certain external interruptions to identify the instruction processor involved and the STORE CPU ADDRESS instruction enables a program to obtain the address of the instruction processor in which it is executing.
- Interprocessor programmed communication via the SIGNAL PROCESSOR (SIGP) instruction – required to enable an instruction processor to request services of the other instruction processor and to alert it to conditions to which it must respond during dual processor mode operations. For example, this capability is used during the initialization of dual processor mode operations, for reconfiguring hardware components, and in recovery procedures that occur after an instruction processor failure.

In the 4381 Model Group 14 or 3, the CPU reset and initial CPU reset SIGP orders are not implemented for System/370 mode and the IML SIGP order is not implemented for System/370 or System/370-XA mode. See the *Principles of Operation* manuals for the orders provided for the SIGP instruction.

- Interprocessor hardware communication – required to alert an instruction processor to conditions in the other instruction processor and to synchronize certain operations in both instruction processors during dual processor mode operations.

The communication facilities include the following:

- Synchronization of the two physical time-of-day clocks to provide one logical clock for the dual processor configuration
- Malfunction alert indication sent to the operational instruction processor when one instruction processor enters the clock stopped state because of a machine check error
- High-speed buffer intercommunication to permit the buffer storage controls to ensure that all real storage references by each instruction processor result in access to the most current copy of the addressed data. This communication is discussed in Section 30:15 under “High-Speed Buffer Storage.”

The address translation facilities provided for System/370 and System/370-XA modes for all 4381 model groups are discussed in Section 50. Other significant features of the instruction processing functions in 4381 Model Groups 14 and 3 are discussed in the remainder of this subsection.

## Instruction Set

The standard instruction set for 4381 Processors contains all the instructions implemented for 4381 Processors (no instructions are optional). The standard instruction set for a 4381 Model Group 14 or 3 Processor operating in System/370 mode consists of all the System/370 instructions defined in *IBM System/370 Principles of Operation (GA22-7000)* except those associated with features not implemented in the 4381 Model Group 14 or 3 Processor (READ DIRECT, WRITE DIRECT, RESUME I/O, and channel set switching instructions). The 4381 Model Group 14 or 3 has the same instruction set for System/370 mode as uniprocessor 4381 model groups plus the multiprocessing instructions previously described.

The standard instruction set for a 4381 Processor operating in System/370-XA mode consists of all the instructions defined in *IBM System/370 Extended Architecture Principles of Operation (SA22-7085)*.

The STORE CPU ID instruction, which permits a program to determine the processor and version of the processor upon which it is operating and provides the processor serial number, stores a version code of X'04' for the 4381 Model Group 14 and of X'01' for the 4381 Model Group 3. The instruction processing function is identified as 0 or 1 by bits 8 through 11 of the stored field.

The DIAGNOSE MSSFCALL instruction is implemented in all 4381 Processors for System/370-XA mode of operation. It is used by the MVS/XA operating system. This instruction supports seven commands and can be issued only by a program that is operating in supervisor state. It specifies the function to be performed and the location of a data area in processor storage (up to 2K bytes in size) that is to receive completion status for the instruction and any requested configuration information.

The following DIAGNOSE MSSFCALL commands are implemented in 4381 Processors:

- SCP INFO (provides processor storage and auxiliary storage sizes)
- CHANNEL PATH INFO (provides channels installed and online/offline status)
- VARY CHANNEL PATH OFF (used to vary a channel path offline)
- VARY CHANNEL PATH ON (used to vary a channel path online)
- READ RESTART REASON (enables the operating system to obtain a one-byte restart modifier that was entered by the operator and saved in auxiliary storage after a restart was initiated)
- WRITE CONSOLE TEXT (enables the operating system to place display information for the operator console in auxiliary storage)
- READ LOOP RECORDING (enables a stand-alone dump program to obtain trace data saved in auxiliary storage to aid in debugging)

The configuration commands are processed by the instruction processing function. The support processor is not involved. The auxiliary storage area is accessed as required to process all the DIAGNOSE MSSFCALL commands.

## Other Features

The Multiply and Add Facility, Square Root Facility, Mathematical Function Facility, ECPS:MVS, ECPS:VM/370, and Preferred Machine Assist features are standard in 4381 Model Group 14 Processors.

The Multiply and Add Facility, Elementary Math Library Facility, ECPS: MVS, ECPS:VM/370, and Preferred Machine Assist features are standard in 4381 Model Group 3 Processors (see discussions of these features in Section 20:05).

## 30:15 Storage

The 4381 Model Group 14 or 3 Processor has a two-level storage system— a small high-speed buffer storage in each instruction processing function backed by shared large processor storage. The use of a two-level storage system, in which the two instruction processing functions work mostly with the two high-speed buffers, significantly reduces the effective processor storage cycle of the 4381 Model Group 14 or 3 and greatly contributes to its high internal performance.

## Processor Storage

Processor storage is available for the 4381 Model Group 14 in sizes of 16Mb, 24Mb, and 32Mb (Models P14, Q14, and R14, respectively) and for the Model Group 3 in sizes of 8Mb, 16Mb, 24Mb, and 32Mb (Models M03, P03, Q03, and R03, respectively). Field upgrades from one processor storage model to another in the same 4381 model group are supported. A portion of the installed processor storage is reserved for processor use and is called auxiliary storage.

Access to processor storage is made via the storage control functions, which operate under the control of the instruction processing functions. The path to and from processor storage is 16 bytes wide (two doublewords). Data that enters/leaves processor storage is aligned on a doubleword boundary.

Error checking and correction (ECC) hardware provides automatic detection and correction of all single-bit processor storage errors and detection of all double-bit and many multiple-bit errors. Certain double-bit errors can also be corrected by microcode. ECC logic performs checking on a doubleword basis. The ECC feature and double-bit error correction are discussed in Section 60.

Store and fetch protection are standard. For a 4381 Model Group 14 or 3 with no more than 16Mb of processor storage, one 7-bit storage protection key is provided for each 2K-byte block of processor storage. For a 4381 Model Group 14 or 3 configuration with 24Mb or 32Mb of processor storage installed, one 7-bit storage protect key for each 4K-byte block of processor storage is supported, since only one key for every 4K bytes is provided in the processor storage above 16Mb.

The standard Extended Addressing feature in the 4381 Model Group 14 or 3 permits processor storage above 16Mb to be utilized. The feature provides the following:

- Extended real addressing, which provides the ability to address up to 64Mb of real storage using an additional two bits in page table entries to generate a 26-bit real address from a 24-bit virtual address. As implemented in 4381 Model Group 14 and 3 Processors, Extended Addressing permits up to 32Mb of real storage to be addressed.
- Storage-key 4K-byte block, which permits storage keys to be provided for 2048-byte and/or 4096-byte blocks (instead of only for 2048-byte blocks)
- Storage key instruction extension, which provides the instructions SET STORAGE KEY EXTENDED, INSERT STORAGE KEY EXTENDED, and RESET REFERENCE BIT EXTENDED that can specify a 31-bit real address and can be used regardless of whether keys are provided on a 2048- or 4096-byte block basis
- 31-bit IDAW, which permits an indirect data address word to specify a 31-bit absolute address

The TEST BLOCK (TB) privileged instruction (not implemented in 4341 Processors) is provided to enable a program to (1) determine the usability of a 4K-byte block of processor storage and its associated one or two 7-bit protection keys and (2) perform storage validation by storing zeros in the 4K bytes to attempt to set up good ECC bits in all the doublewords.

The TB instruction specifies the 31-bit real address of a 4K-byte block on a 4K-byte address boundary in processor storage that is to be tested. The specified real address is tested for an addressing exception (address outside of installed processor storage) and violation of low address protection. The real address is not tested for key controlled protection or segment protection.

The condition code is set for a TB instruction to indicate the usability of the specified 4K-byte block and its protection keys. If both the block and its protection key(s) are usable, condition code 0 is set. Condition code 1 is set if the 4K-byte block is unusable, one or both of its keys are unusable, or any combination of block and keys is unusable.

In 4381 Processors, if the protection keys for the specified 4K-byte block are both usable the TB instruction sets them both to zero. If either key is not usable the TB instruction leaves both keys unmodified. The TB instruction stores zeros in the 4K-byte block, whether the block or its keys are usable, to attempt to establish good ECC bits.

The TB instruction accesses the TEST BLOCK area within auxiliary storage to determine the usability of the specified 4K-byte block and its two protection keys. There is one internal record for 4K-byte block errors and one internal record for protect key errors. There is one bit in the 4K-byte block record for each 4K bytes of processor storage and one bit in the protect key record for its one or two associated keys. A one in a bit position indicates the associated 4K-byte block or protect key is unusable. To execute a TB instruction, the instruction processing function inspects the two appropriate bits in the TEST BLOCK internal records,

sets the condition code, and stores zeros in the addressed 4K-byte block and in both keys if they are both unusable.

The two TEST BLOCK internal records are placed in auxiliary storage during IML. These two records are maintained on functional diskette 1, which is shipped to a 4381 installation with all zeros in both records. During processor operation, any time a double-bit error consisting of two solid errors or two consecutive protect key errors occur, the TEST BLOCK internal record in auxiliary storage and that on functional diskette 1 are updated. Thus, known unusable 4K-byte blocks are saved across IMLs and power-offs. The TEST BLOCK internal records on functional diskette 1 are updated as appropriate whenever processor storage is repaired.

The TB instruction is designed to be used during IPL to enable the operating system to build a page frame table that indicates the known unusable 4K-byte page frames to avoid their assignment. The TB should also be issued if an uncorrectable storage error is encountered during system operation to attempt to validate the unusable block (store good ECC bits). Successful validation will prevent the occurrence of a machine check if the unusable block is prefetched or inadvertently referenced.

## Auxiliary Storage

The UCWs for System/370 mode or the subchannels and control unit blocks for System/370-XA mode, the I/O queuing area, a trace area, the TEST BLOCK internal records, and certain work areas are located in highest addressed processor storage. This storage, called auxiliary storage, is reserved for processor rather than program use and is inaccessible to all programs.

The size of auxiliary storage in bytes for a 4381 Processor Model Group 14 operating in System/370 mode is 90,120 (86,016 for the Model Group 3) plus 64 times the number of UCWs defined (128 to 2048) for each instruction processing function rounded up to a 4K boundary. For System/370-XA mode, auxiliary storage size in bytes for Model Groups 14 and 3 is 192,512 plus 70 times the number of control units defined (1 to 256) plus 180 times the number of subchannels defined (up to 2048) rounded up to a 4K boundary.

The minimum auxiliary storage requirement for System/370 mode of operation is 104Kb for the Model Group 14 (100Kb for the Model Group 3) for 128 UCWs defined for each instruction processing function, while the maximum requirement is 344Kb for the Model Group 14 (340Kb for the Model Group 3) for 2048 UCWs defined for each instruction processing function. For System/370-XA mode of operation, a minimum of 220Kb is required (for 128 subchannels and 128 control unit control blocks) and the maximum requirement is 568Kb for 2048 subchannels and 256 control unit control blocks.

The size of auxiliary storage is determined during IML. The processor storage address of the first byte of auxiliary storage is calculated and placed in an address check boundary (ACB) register. Any attempt to access an address equal to or above the ACB register value during program execution results in an addressing exception program interruption.

The contents of auxiliary storage vary depending on the mode, System/370 or System/370-XA, in effect. During an IML, the required auxiliary storage area is initialized as appropriate, using information contained on the functional diskette(s).

Auxiliary storage for System/370 mode contains the following in the highest to the lowest addressed locations:

- UCW area for each instruction processing function with a minimum of 128 and a maximum of 2048 UCWs
- SIOF queuing area
- I/O trace area
- Channel error logout area
- Channel UCW directory area
- Instruction tracing area
- Channel data buffer reconfiguration test data
- Restart text save area
- Two internal records for the TEST BLOCK instruction (one for unusable protect keys and one for unusable 4K-byte blocks)
- Engineering/scientific assist table
- Program event recording area
- Control storage link information
- K-addressable auxiliary storage area of 1K bytes. This area contains various pointers and data fields used by the instruction processing functions (pointers to the beginning of the other areas in auxiliary storage, the time-of-day clock, the CPU timer, the clock comparator, the interval timer, for example)

For System/370-XA mode, auxiliary storage contains the following in the highest to the lowest addressed locations:

- Monitoring data area (32 bytes/subchannel)
- I/O trace area
- Channel error log
- CRW (channel report word) queue
- Subchannel area
- Control unit block area (70 bytes/control unit)
- Channel directories
- Channel data buffer reconfiguration test data
- I/O queuing information

- Interrupt area
- Restart text save area
- SIE instruction work area
- Two internal records for the TEST BLOCK instruction
- Instruction tracing area
- Engineering/scientific assist table
- Program event recording area
- Control storage link information
- K-addressable auxiliary storage area of 1K bytes. The contents of this area varies slightly for System/370-XA and System/370 modes.

## Storage Control Function

Each storage control function operates under the control of its associated instruction processing function to handle all access to processor storage. The following components are part of each storage control function:

- High-speed buffer storage and its directory
- The TLB for translating virtual storage addresses in instructions to real storage addresses for both System/370 and System/370-XA modes (discussed in Section 50)
- The key stack that contains the 7-bit keys for the processor storage installed. Each key consists of four access control (store protection) bits, one fetch protection bit, one reference bit, and one change bit.
- The ECC logic for processor storage – only in the storage control function for instruction processing function 0 (see Section 60)
- Data flow control
- The input/output (I/O) data register that is used to transfer data (1) among the components of the storage control function and (2) between processor storage and the instruction processing function

The I/O data register is 64 bytes wide to improve instruction execution speed. For fetches/stores involving the instruction processing function (including those done for the channels), only 8 bytes of the 64-byte I/O data register are used, while 16 bytes are used for fetches/stores involving processor storage.

## High-Speed Buffer Storage

The high-speed buffer is a standard feature and provides high-speed data access for instruction processing function fetches and stores. The 4381 Model Group 14 has one standard 64Kb high-speed buffer storage for each instruction processing function. The 4381 Processor Model Group 3 has one standard 32K-byte high-speed buffer storage for each instruction processing function.

Buffer storage control and use are handled entirely by buffer control function hardware and are transparent to the programmer, who need not adhere to any particular program structure in order to obtain close to optimum use of the buffer. Parity checking is used for data verification in the buffer.

The flow of data from each instruction processing function to and from processor storage via the high-speed buffers in a 4381 Model Group 14 or 3 is shown in Figure 12. One ECC checking function is shared by the two instruction processing functions. The data flow control logic provides a data path between (1) the ECC checking function and high-speed buffers 0 and 1 for data fetch/store operations from/to processor storage and (2) high-speed buffers 0 and 1 for interbuffer data transfers.

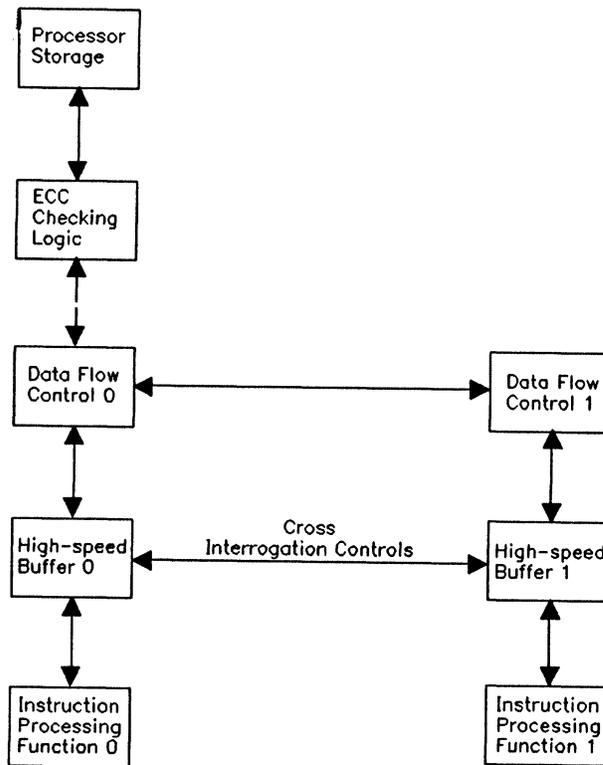


Figure 12. Data flow to and from processor storage via the high-speed buffers in a 4381 Model Group 14 or 3

Cross interrogation controls are provided for the two high-speed buffers to permit each buffer storage control to access the buffer directory of the other high-speed buffer.

General operation of the two high-speed buffers is as follows. When a fetch request is made by an instruction processing function (say 0) for instructions or data, its high-speed buffer storage control determines whether the requested doubleword is in high-speed buffer 0 by interrogating buffer directory 0, which indicates the current contents of buffer 0. If the doubleword requested is present in buffer 0 and valid, it is sent directly to instruction processing function 0 without a processor storage reference.

If the requested doubleword is not currently in high-speed buffer 0, the cross interrogation controls are used to search the buffer directory for high-speed buffer 1. If the requested doubleword is not in high-speed buffer 1 either, a processor storage fetch is made, the data is assigned a buffer location and stored in buffer 0, and the requested doubleword is sent to instruction processing function 0.

When data is stored by instruction processing function 0, high-speed buffer 0 is updated if the contents of the processor storage location being altered are currently being maintained in buffer 0. Processor storage is not modified, however, since the high-speed buffer in 4381 Processors is a store-in, rather than a store-through, type of buffer. If the data is not currently being maintained in buffer 0, the cross interrogation controls are used to search the buffer directory for high-speed buffer 1. If the data is not currently being maintained in high-speed buffer 1 either, a processor storage fetch is made to obtain the required block of data and load it into buffer 0. The store is then made to the just loaded buffer location and processor storage is not modified.

When a fetch or store request is made by instruction processing function 0 and the referenced data is not in high-speed buffer 0 but is being maintained in high-speed buffer 1, the action taken depends on whether the referenced data block in high-speed buffer 1 has been modified. If it has, a buffer-to-buffer transfer is performed to move the referenced block from buffer 1 to buffer 0 and this block is marked invalid in buffer 1. The fetch or store is then made to the block in buffer 0.

If the referenced data block has not been modified in buffer 1 and a store request was issued, the referenced block is invalidated in buffer 1, the referenced block of data is loaded into buffer 0 from processor storage, and store is made to the block in buffer 0. For a fetch request, the referenced block of data is loaded in buffer 0 from processor storage. The referenced block in buffer 1 is not invalidated but a bit (copy) is set for this block in each buffer directory. If a write is subsequently issued for a buffer block whose copy bit is on, the buffer block is changed in the addressed buffer and invalidated in the other buffer.

If the data in the buffer location that is to receive new block of data for a fetch or a store request had been changed while in the buffer, this data must be unloaded before the new data can be loaded. In order to reduce the time the instruction processing function must wait for the requested data in this situation, a swap buffer is implemented for each high-speed buffer. The changed data is written to the swap buffer while processor storage is being accessed for the new block of data to overlap most block unload time with processor storage access time. After the new block is loaded and the requested data is sent to the instruction processing function, the data in the swap buffer is written to processor storage.

The channels read into and write from processor storage using the input/output data register in the storage control function. When a channel writes data (input operation from an I/O device), each buffer directory is interrogated. If data from the affected processor storage address is being maintained in a high-speed buffer, the channel writes the data to that high-speed buffer and processor storage is not modified. Otherwise, the data is written to processor storage only.

When a channel attempts a read or write operation, each buffer directory is interrogated. If the required data is present in the local buffer, the channel read or write is done from/to that buffer and processor storage is not affected. If the required data is not present in the local buffer and is either not present or present and not modified in the other buffer, the channel read or write is done from/to processor storage. If the required data is not present in the local buffer, but is present in the other buffer and modified, the block of data is transferred to processor storage and then the channel read or write is done from/to processor storage.

The store-in approach used for the high-speed buffers in 4381 Processors is like that used in 4341, 4331 Model Group 2, 4361, 308X, and 3090 processors but contrasts with the store-through approach used in the high-speed buffers in System/370 and 303X processors in which processor storage is altered whenever data is stored in the buffer. The store-in approach reduces the number of accesses to processor storage, since changed buffer data is written to processor storage only if it must be replaced by another block (or when a buffer purge is required). The store-in approach becomes more and more advantageous as the difference between processor storage and high-speed buffer storage cycle times becomes greater.

Buffer reconfiguration, which is not implemented in 4341 Processors, is standard in 4381 Processors. If a double-bit error occurs during the loading of a buffer block, the load is tried once more. If the error is not corrected, buffer reconfiguration is done, if possible, as part of the instruction retry function. The high-speed buffer array for each instruction processor in a Model Group 14 or 3 contains spare space that is used for reconfiguration purposes. When an uncorrectable storage error occurs in a byte in a buffer block, space in the reconfiguration area is allocated and a bit is set to indicate the reconfiguration area is to be used for this buffer block. The buffer load is retried and operations continue using the reconfiguration area for that buffer block if the load is successful.

If a load is not successful after the reconfiguration (assigned reconfiguration array location is malfunctioning), the buffer block location that caused the error can no longer be used and the malfunctioning bit in the directory entry for the malfunctioning block is turned on. The operator is notified that degradation is occurring and system operation continues.

Up to eight buffer block errors can be reconfigured as long as no more than one error occurs in a given byte position within a doubleword. When this limit is reached, the operator is notified that the buffer should be repaired.

Reconfiguration is also attempted for errors that occur in the swap buffer for the high-speed buffer in instruction processing function 0. A substitute array for the swap buffer is provided and, as for a high-speed buffer, up to eight errors can be reconfigured as long as no more than one error occurs in a given byte-pair position within a 16-byte data entry in the array. If the reconfiguration limit is reached or an error occurs in a reconfigured byte position of the swap array, the operator is notified that repair is required.

Operation of the entire high-speed buffer for an instruction processing function cannot be disabled in a 4381 Processor. However, utilization of an individual buffer block can be disabled by turning on the malfunctioning bit in the associated directory entry, as is done when reconfiguration is not possible.

## 30:20 Support Processor Subsystem

### Components and Functions

The support processor subsystem provides basic operational functions for 4381 Processors and is the primary maintenance tool for diagnosing hardware malfunctions. It is designed to maximize total system availability and to provide rapid fault location and repair, where possible.

The components of the support processor subsystem are the support processor, support bus adapter, local channel adapter, console attachment adapter and attached devices, power adapter, power information panel, common communications adapter for the Remote Support Facility, and two system diskette drives and associated adapters.

The support processor subsystem in 4381 Model Groups 14 and 3 is functionally like that in uniprocessor 4381 model groups as described in Section 20:15.

Note that in a 4381 Model Group 14 or 3 Processor, the natively attached primary console and up to three additional displays and/or printers attach only to byte multiplexer channel 0 for instruction processing function 0 via the local channel adapter. Thus, if a malfunction prevents operation of instruction processing function 0, the 4381 cannot be used in uniprocessor mode with only instruction processing function 1 operating unless an alternate console is connected to a channel in the group for instruction processing function 1.

## 30:25 Channels

### General Description

The 4381 Processors implement advanced channel functions like those implemented in 4341 Processors, such as block multiplexing and data streaming, and also offer more channels and higher aggregate channel data rates than do 4341 Processors.

Two standard channel groups, one for each instruction processing function, are provided for 4381 Model Group 14 and 3 Processors. Each standard channel group consists of one byte multiplexer channel, addressed as channel 0, and five block multiplexer channels, addressed as channels 1 through 5, providing twelve standard channels in the configuration. Channel 5 in each channel group can be configured as a byte, instead of a block, multiplexer channel.

One channel group (Block Multiplexer Channels, Additional feature) is optional for a 4381 Model Group 14 or 3. This feature provides six block multiplexer channels, three for each instruction processing function addressed 6 through 8, for a total of 18 channels in the configuration. None of the channels in the optional channel group can be configured as a byte multiplexer channel and the six channels provided must be divided equally between the two channel groups (three channels to each).

For System/370 mode operations, the channel group for instruction processing function 0 is dedicated to that instruction processor and cannot be accessed during dual processor or uniprocessor mode operations by instruction processing function 1, whose channel group cannot be accessed by instruction processing function 0. Channel set switching, which permits an instruction processor to access the channel set of another instruction processor in a tightly coupled multiprocessing configuration, is not implemented in Model Group 14 and 3 4381 Processors.

For System/370 mode dual processor operations, the operating system determines the path selected for an I/O operation. If an I/O device is accessible via a channel in both channel groups, I/O requests for that device that are issued by a program executing in either instruction processor can be started by either instruction processor. However, if a program executing in instruction processor 0 issues a request for an I/O device that is only accessible via a channel in the group for instruction processor 1, the request must be started by instruction processor 1.

To ensure maximum system availability for System/370 mode operations, the I/O configuration for a 4381 Model Group 14 or 3 should be designed to permit uniprocessor mode of operation with access to all or most I/O devices if an instruction processing function becomes inoperable. Thus, as many I/O devices as possible should be accessible to both instruction processing functions using channel and control unit switching features to provide at least one channel path to each device from each channel group. For devices for which programmed switches are not available, manual switching can be installed to permit the operator to switch access between the two channel groups. Redundant control units should be installed for all critical devices and an alternate operator console should be attached to channel 0 for instruction processing function 1.

For System/370-XA mode of operation, the microcoded dynamic channel subsystem can start an I/O operation to a device via any channel path that is defined for that device regardless of which instruction processor issued the I/O request.

A byte multiplexer channel in a 4381 Processor can handle the concurrent operation of multiple slower speed devices when operating in byte interleave mode, while a block multiplexer channel can support interleaved, concurrent execution of multiple high-speed channel programs.

Each installed channel can have up to eight control units attached. For byte multiplexer channel 0 in the channel group for instruction processing function 0, one control unit position is used by the local channel adapter. This internal adapter provides attachment of support processor subsystem devices to this byte multiplexer channel. As a standard feature, automatic control unit powering is provided for up to 32 control units attached to a 4381 Processor.

Comprehensive error checking is incorporated in the basic design of the channel hardware. Checking is performed on the control logic in most areas, and standard

parity checking is done on the data flow between the channels and instruction processing function.

For System/370 mode of operation, the fast release function of the START I/O FAST RELEASE (SIOF) instruction is implemented in 4381 Processors as is queuing of SIOF instructions. These two functions are inherent in the design of the channel subsystem for System/370-XA mode of operation. These facilities reduce the instruction processing function processing time required for an SIOF instruction when compared with the time required for a START I/O (SIO) instruction.

Optionally, one Channel-to-Channel Adapter can be installed in a 4381 Processor Model Group 14 or 3 and attached to any block multiplexer channel. The other channel to which the adapter is attached can be contained in another 4381 Processor or a System/360, System/370, 30XX, 4341, 4361, 4331, or 4321 processor. Three control unit positions on each channel and one nonshared UCW for each of the two channels interconnected via the 4381 Channel-to-Channel Adapter are required. The adapter operates in burst mode and transfers data at the rate of the lower speed channel to which it is attached.

The Channel-to-Channel Adapter provided for 4381 Processors is functionally equivalent to the adapter provided for System/370 and 4300 processors but is implemented in a higher density technology that reduces its size.

The 3088 Multisystem Channel Communication Unit can also be used to interconnect 303X, 308X, 3090, 4341, and 4381 processors via block multiplexer channels.

## **Device Addresses and Unit Control Words For System/370 Mode**

Each byte multiplexer channel and each block multiplexer channel installed in a 4381 Processor Model Group 14 or 3 can have 256 device addresses (00 to FF). For each channel group, any device addresses can be used for block multiplexer channels 1 through 8 or for channel 5 when it is a byte multiplexer channel. For byte multiplexer channel 0 in the channel group for instruction processing function 0, addresses 0F0 to 0FF are reserved for support processor subsystem devices attached via the local channel adapter and any device addresses other than these can be used for the I/O devices attached to byte multiplexer channel 0 via external control units. Thus, only 240 device addresses (000 to 0EF) can be assigned to user devices natively attached to this channel 0 or via external control units. Any device addresses can be used for byte multiplexer 0 in the channel group for instruction processing function 1.

Each instruction processing function in a 4381 Processor Model Group 14 or 3 can have a minimum of 128 and a maximum of 2048 UCWs as a standard feature for System/370 mode of operation. UCWs are allocated by the customer engineer or operator, using the display console. UCWs above 128 are allocated in groups of 64. Each UCW is 64 bytes in size and resides in auxiliary storage. Each group of 64 UCWs requires 4K bytes of storage. Thus, a minimum of 8K bytes and a maximum of 128K bytes are required for UCW storage.

The UCWs allocated for each instruction processing function are assigned a three-digit reference number 000 to N-1, where N is the number of UCWs allocated. UCWs for instruction processing function 0 with the reference numbers 000 to 030 are reserved for internal functions (support processor, for example) and

support subsystem devices. In addition, each channel is assigned one channel-shared UCW that is used to present asynchronous interruptions for any I/O devices attached to the channel that are not allocated a UCW (defined to the system).

The UCWs defined for an instruction processing function can be assigned to any of the channels actually present in the channel group for that instruction processor. A maximum of 256 UCWs can be assigned to any one channel. The customer engineer or operator assigns UCWs to specific channel addresses using the operator console. Each UCW can be designated as shared or nonshared.

A shared UCW can be used by a set of devices, one device at a time. A shared UCW generally is assigned to a control unit that has multiple devices attached, only one of which can be in operation at a time. A nonshared UCW is one that is assigned to only one device. A nonshared UCW is designed for use with a control unit that has only one I/O device attached or that has multiple I/O devices attached that can operate concurrently.

A channel directory for each channel is allocated in auxiliary storage. Each channel directory has 256 entries, one for each of the possible device addresses for a channel. A directory entry indicates whether a UCW is assigned to the associated device address, characteristics of the assigned UCW, and characteristics of the device assigned the associated device address.

A channel directory entry contains the following:

- Reference number of the UCW assigned (all device addresses have a UCW assigned)
- Assigned bit to indicate whether an I/O device is defined for the associated device address
- An indication of whether the associated device operates in byte multiplexer mode
- An indication of whether the UCW is shared or nonshared (shared bit)
- An indication of whether the associated device must operate in selector mode rather than block multiplexer mode
- An indication of whether the device is attached to a control unit that is to use the START I/O FAST queuing function
- An indication of whether the associated device is attached to a control unit that is capable of operating in data streaming mode
- An indication of the mode in which channel 5 is to operate (byte or block multiplexer)

Devices attached to a block multiplexer channel that are capable of block multiplexing should have the shared and selector mode bits off in their channel directory entry to indicate allocation of a nonshared UCW that is capable of disconnecting. For devices attached to a control unit that is capable of data streaming mode of operation (such as a 3880 storage director), the directory entry should have the data streaming mode bit on.

The customer engineer or installation operator can select displays associated with UCWs. The functions provided by the UCW displays enable the customer engineer/operator to display the allocated UCW reference numbers and the device addresses they are assigned, and to display and alter the attributes of the UCWs. The alter capability is used to change device addresses and attributes assigned to UCWs. The UCWs for the natively attached displays/printers are preassigned.

Device addresses for natively attached and all other I/O devices and UCWs for devices that are not natively attached must be selected during installation. If a UCW assignment is changed, it becomes effective during the next IML, unless it is for a natively attached device. Changes to UCWs for natively attached devices become effective immediately.

The channel directory entry for each device address for which a device has not been assigned (assigned bit is off) has a UCW assigned. All the device addresses without an assigned I/O device for the same channel have the same channel-shared UCW assigned. Thus, if an I/O device exists in a 4381 configuration but has not been defined as part of the I/O configuration, the shared UCW is used to present any status information that may be generated by the undefined device. However, if any I/O instruction is issued to an undefined device, a not operational conditional code is generated for the I/O instruction.

### **Subchannels For System/370-XA Mode**

For System/370 extended architecture mode of operation, a byte or block multiplexer channel can have a maximum of 256 device addresses assigned, as for System/370 mode, and the same channel device addresses (0F0 to 0FF) for byte multiplexer channel 0 for instruction processing function 0 are reserved for system use. Up to 2049 subchannels (2048 plus 1 for microcode usage) can be defined, each of which requires 128 bytes in auxiliary storage. In addition, each physical control unit attached to a 4381 Processor (up to 256 plus 1 for microcode usage) requires 70 bytes of auxiliary storage.

Subchannels for System/370-XA mode are the same for all 4381 model groups, as described in Section 20:20.

### **General Operation of the Channels**

The channels in 4381 Processors are microcode- and hardware-controlled. Operationally, they are integrated channels and, thus, share the use of certain hardware with the instruction processing function, such as the arithmetic logic unit, byte shifter, and control storage.

The operation of each channel group in a 4381 Model Group 14 or 3 Processor is the same as the operation of the channels in a uniprocessor 4381 model group, as described in Section 20:20.

## Byte Multiplexer Channels

The byte multiplexer channel for 4381 Processors is functionally identical to the byte multiplexer channel for System/370, 30XX, and other 4300 processors. A byte multiplexer channel can operate in byte interleave mode to permit several slower speed I/O devices to operate concurrently or in burst mode to permit one buffered device to operate. Unbuffered burst mode devices that are subject to data overrun, such as magnetic tape units, cannot be attached to a byte multiplexer channel in a 4381 Processor.

For byte multiplexer channel input operations, a maximum of up to 2 Mb/sec for channel 0 or 5 is possible for a burst mode operation involving a buffered device. The output rate for burst mode buffered devices equals the device rate in Mb/sec divided by 1 plus the device rate in Mb/sec for device rates less than or equal to 2 Mb/sec. These data rates assume small interface and control unit generated delays.

The data rate for byte mode operation depends on other channel activity and the number of bytes transferred per burst. For one-byte, two-byte, and four-byte transfers, the maximum data rates are 28Kb/sec, 56Kb/sec, and 112Kb/sec for the 4381 Model Group 14 and for channel 5 of the 4381 Model Group 3. For channel 0 of the 4381 Model Group 3, maximum data rates are 24Kb/sec, 48Kb/sec, and 96Kb/sec for one-byte, two-byte, and four-byte transfers, respectively. The maximum data rate can be achieved only when there is no activity on any other channel or a console device. For byte multiplexer data rates when there is other channel activity, see *IBM 4381 Processor Channel Characteristics*, GA24-3948.

I/O devices in the support processor subsystem attach to byte multiplexer channel 0 for instruction processing function 0 via the local channel adapter, which occupies the last control unit position on this channel. Thus, a maximum of seven external control units can be attached to byte multiplexer channel 0 for instruction processing function 0. There is no local channel adapter for byte multiplexer channel 0 for instruction processing function 1.

The local channel adapter operates like a channel-to-channel adapter that connects the I/O bus of the support processor to byte multiplexer channel 0. The local channel adapter provides a low-cost method of attaching support processor subsystem devices to a channel.

The local channel adapter appears as a shared control unit that can have multiple device addresses. It operates in multibyte mode in the 4381 Processor. Data is transferred from the local channel adapter to the byte multiplexer channel two bytes at a time.

## Block Multiplexer Channels

The block multiplexer channels in a 4381 Processor can operate in block multiplexer or selector mode. When operating in selector or block multiplexer mode, a block multiplexer channel in a 4381 Processor is functionally equivalent to a selector or block multiplexer channel in System/370, 30XX, and other 4300 processors. A block multiplexer channel presents a standard I/O interface and can have a maximum of eight control units attached.

The maximum data rate for block multiplexer channels 1 through 5 in each standard channel group in a 4381 Model Group 14 or 3 Processor is 3 Mb/sec each for data streaming mode of operation. The maximum aggregate data rate for the ten standard block multiplexer channels is the sum of these rates, or 30 Mb/sec.

When the optional channel group is installed in a 4381 Model Group 14, each of the six channels has a maximum data rate of 3 Mb/sec. The maximum aggregate data rate for the nine channels in each group is 18 Mb/sec, providing a maximum aggregate data rate of 36 Mb/sec for the two groups.

When the optional channel group is installed in a 4381 Model Group 3, channel 6 in each channel group has a maximum data rate of 3 Mb/sec, while channels 7 and 8 in each channel group can operate at a maximum of 2 Mb/sec each. The maximum aggregate data rate of the nine channels in each group is 16 Mb/sec for a maximum aggregate of 32 Mb/sec for the two groups.

Like a byte multiplexer, a block multiplexer channel can have multiple subchannels, each of which can support one I/O operation. The setting of a channel mode bit (0) in control register 0 determines whether the addressed subchannel of a block multiplexer channel operates in block multiplexer mode (assuming it is capable of operating in block multiplexer mode) or selector mode when a start instruction is issued. The mode bit is set to 0 (selector mode) at IPL and can be altered by programming at any time.

### **Data Streaming Mode**

Data streaming mode of operation is standard for all the block multiplexer channels present in a 4381 Model Group 14 or 3 Processor. Data streaming mode enables all (Model Group 14) or certain (Model Group 3) 4381 block multiplexer channels to handle faster data rates and all 4381 block multiplexer channels to handle a longer channel-to-control-unit cable length. Specifically, a maximum channel-to-control-unit cable length of approximately 122 meters (400 feet) is supported for control units that are capable of operating in streaming mode and a data rate of up to 3 Mb/sec can be achieved for this cable length for channels 1 through 8 in each channel group in a 4381 Model Group 14 and for channels 1 through 6 in each channel group in a 4381 Model Group 3.

Data streaming mode of operation is the same in all 4381 model groups, as discussed in Section 20:20.

### **SIOF Instruction For System/370 Mode**

The fast release function of the SIOF instruction and queuing of SIOF instructions that are issued to a busy block multiplexer channel or control unit are designed to reduce the time required to start I/O operations. These two facilities are the same in all 4381 model groups, as discussed in Section 20:20.

## 30:30 Standard and Optional Features

### Standard Features

The following are standard features of 4381 Model Group 14 and 3 Processors that are operative for both System/370 and System/370-XA modes:

- Binary arithmetic
- BRANCH and SAVE instructions
- Byte-oriented operands
- Channel indirect data addressing
- Channels 0 to 5 for each instruction processing function, which can be configured as one byte and five block multiplexer channels or two byte and four block multiplexer channels
- Command retry for block multiplexer channels
- Conditional Swapping
- Control Unit Powering (for up to 32 control units)
- CPU timer and clock comparator (one microsecond resolution)
- Data Streaming for all installed block multiplexer channels
- Decimal arithmetic
- Dual Address Space Facility
- ECC on processor storage and error correction for certain double-bit errors
- ECPS:MVS (tracing functions not implemented for System/370-XA mode)
- EC mode of operation
- Elementary Math Library Facility (Model Group 3)
- Expanded machine check interruption class
- Extended Addressing
- Floating-point arithmetic (including extended precision)
- High-speed buffer storage—64K bytes for each instruction processing function in the Model Group 14 and 32K bytes for each instruction processing function in the Model Group 3
- Instruction retry
- Interruption for SSM instruction
- Low address protection
- Mathematical Function Facility (Model Group 14)
- Monitoring feature
- MOVE INVERSE instruction
- Multiply and Add Facility
- Multiprocessing
- Problem Analysis
- Program event recording
- PSW key handling
- Reconfiguration functions
- Reference and change recording
- Reloadable control storage
- Square Root Facility (Model Group 14)
- Storage key instruction extensions (ISKE, RRBE, and SSKE instructions)
- Store and fetch protection (one key per 2K-byte block for up to 16Mb installed or one key per 4K-byte block for more than 16Mb installed)
- Store status
- Support processor subsystem

- System/370 Extended feature (common segment bit, INVALIDATE PAGE TABLE ENTRY instruction, low address protection, TEST PROTECTION instruction)
- TEST BLOCK instruction
- Time-of-day clock (one-microsecond resolution)

The following are standard features for 4381 Model Groups 14 and 3 that operate only when System/370 mode is in effect:

- BC mode
- Block multiplexer control bit in control register 0
- Channel masks in control register 2
- Channel retry data in a limited channel logout area
- Dynamic address translation for 24-bit virtual and real addresses using 2K or 4K pages and 64K or 1024K segments
- ECPS:VM/370
- External signals
- Interval timer
- INSERT STORAGE KEY instruction
- Instructions for System/370 architecture (includes all defined except READ DIRECT, WRITE DIRECT, RESUME I/O, and channel set switching instructions)
- Limited channel logout
- Machine check external damage code
- Preferred Machine Assist
- Recovery extensions
- RESET REFERENCE BIT instruction
- Segment protection
- SET STORAGE KEY instruction
- STORE CHANNEL ID instruction (and all other System/370 I/O instructions)
- SIOF instruction fast release and queuing (comparable facilities are inherent in the System/370-XA mode channel subsystem definition)
- VM Extended Facility Assist
- 128 to 2048 UCWs in increments of 64

The following are standard features for 4381 Model Groups 14 and 3 that operate only when System/370-XA mode is in effect:

- Bimodal addressing
- Channel subsystem designed for System/370 extended architecture
- DIAGNOSE MSSFCALL instruction
- Dynamic address translation for 31-bit (or 24-bit) virtual and real addresses using 4K pages and 1024K segments
- Instructions for System/370 extended architecture (includes all defined for System/370 extended architecture)
- Page protection
- Tracing
- Sort assist
- Up to 2048 subchannels

## Optional Features

Optional features for 4381 Model Group 14 and 3 Processors, all of which can operate with System/370 or System/370-XA mode in effect and can be field-installed, are:

- 3205 Color Display Console, 3278 Model 2A Display Console, or 3279 Color Display Console Model 2C (includes printer-keyboard mode for System/370 mode only and display mode for System/370 and System/370-XA modes)—required feature
- Block Multiplexer Channels, Additional (provides six block multiplexer channels)
- Channel-to-Channel Adapter (one maximum)
- Remote Operator Console Facility (specify feature—no charge)
- Remote Support Facility (recommended specify feature—no charge)

## Section 40: Operator Console

### 40:05 General Description

A display console for system control and operator/operating system communication is required for any 4381 Processor model group. The operator console is used to (1) manually control operation of the 4381 Processor when the console is in manual mode, (2) communicate with the operating system when the console is in system mode, and (3) perform diagnostic operations when CE mode is in effect. CE mode is made effective when the CE switch on the CE panel located within the frames of the 4381 Processor is turned on. The cable connecting the primary operator console to the 4381 Processor can be a maximum of 6 meters (20 feet) in length.

The operator console for 4381 Processors is the (1) 3205 Color Display Console, (2) 3278 Model 2A Display Console, or (3) 3279 Color Display Console Model 2C. For the 3205, the operator control panel is a no-charge feature that is provided with the 4381 Processor. A 3278 Model 2A or 3279 Model 2C with the appropriate console keyboard feature installed provides an operator control panel in addition to the required keyboard.

The 3205 Color Display Console can also be used as the operator console for a 4361 Processor. The provided operator control panel can be attached to the 3205 unit or located separately. While up to four 3205 consoles can be natively attached to a 4381 Processor, the operator control panel can be used with only one 3205 display (the primary console). The 3205 cannot be included in a 4381 configuration that contains a 3279 Color Model 2C or 3278 Model 2A display.

The 3205 Color Display is functionally equivalent to the 3279 Color Display Console Model 2C and has a compatible keyboard layout. It is a lower cost console than the 3279 Model 2C or 3278 Model 2A console that displays characters on an etched, enhanced contrast, 14-inch CRT (cathode ray tube) screen. The 3205 can be set to display two colors (to emulate the 3278 Model 2A) or four colors (to emulate the 3279 Model 2C).

The 3205 is a compact unit that requires approximately one-third less space than a 3279 Model 2C and is 22 lbs. (10 kilograms) lighter. The standard video pedestal for the 3205 provides 19.4 degrees of tilt (minus 4.4 to plus 15 degrees) and 180 degrees of swivel (plus or minus 90 degrees from the center position).

The 3278 Model 2A or 3279 Model 2C is also used as the operator console for a 4341, 4361, 4331, or 4321 Processor and the operator control panel on the console is the same for 4381 and 4341 Processors.

The 3205, 3278 Model 2A, and 3279 Model 2C operator consoles have twelve program function keys. The audible alarm, which is sounded under program control, is also standard on these consoles. The security keylock feature is optional for the 3278 Model 2A and 3279 Model 2C consoles and standard for the 3205 console. The security key can be used to control the availability of the display. That is, when the security key is in the locked position, the console becomes inoperative, with the keyboard locked and the screen blank. When the Remote Operator Console Facility is used, the security key can be used to control use of the display (as discussed in Section 40:15)

The screen of the 3205, 3278 Model 2A, or 3279 Model 2C operator console can simultaneously display 25 lines of 80 characters each. Lines 21 to 25 on the screen cannot be used for operator-to-operating system communication. Predefined displays are provided to enable the operator to select and execute manual functions (such as resets, IPLs, address compares, etc.).

Note that the one-to-three natively attached displays other than the primary operator console can be connected to a 4381 Processor via a cable up to 1500 meters (4920 feet) in length.

## **Operator/Operating System Communication Modes**

The 3205 Color Display Console, 3278 Model 2A Display Console, and 3279 Model 2C Color Display Console for 4381 Processors have two standard modes of operation for operator/operating system communication: display and printer-keyboard. Printer-keyboard mode is provided to enable the operator console to emulate 1052, 3210, and 3215 printer-keyboards. Printer-keyboard mode must be used when an operating system that uses a 1052 or 3210/3215 as the operator console executes in a 4381 Processor and this mode is not supported when a 4381 Processor is operating in System/370-XA mode.

### **Display Mode**

For display mode, the operator console appears to be a 3277 display attached to a 3272 Model 2 Control Unit. The keyboard is used for input and the cathode ray tube for output. The first 20 lines of the screen are used by the operator and operating system. Optionally, a natively attached 3287 Model 1 or 1C Printer (80 characters per second), 3287 Model 2 or 2C Printer (120 characters per second), or 3268 Printer Model 2 or 2C (340 characters per second) can be used for hard-copy output. The 3287 Model 1C and 2C and 3268 Model 2C Printers provide color printing.

The display/keyboard combination and console printer, if present, are addressed separately when display mode is in effect. While addresses in the range of 000 to 0EF can be utilized, for compatibility with System/370 processors the preferred addresses for the display/keyboard are X'01F' and X'009' and for the 3287 Printer, X'011' and X'015'.

DOS/VSE, OS/VS1, MVS/370, MVS/XA, and VM/370 support display mode operations for the 3278 Model 2A and 3279 Model 2C. The 3287 Printer Models 1, 1C, 2, and 2C and 3268 Models 2 and 2C are supported for hard copy during display mode operations by these operating systems. The operator can also use the copy key to write the contents of the display console to the hard-copy printer. This copy capability must be established through use of the appropriate display.

For display mode, the first 20 lines of the screen are the system area while the next 4 lines are the system status area. Line 25 is used as a console indicator area. The system area is used for communication between the operator and the operating system and for displays associated with manual operations performed by the operator or customer engineer.

### **Printer-Keyboard Mode**

For printer-keyboard mode, the display console appears to the 4381 Processor as a 1052 Printer-Keyboard if a System/360 operating system is being used or as a 3210/3215 Console Printer-Keyboard if a System/370 operating system is being used. The keyboard is used for input and the cathode ray tube is used for output. A natively attached 3287 (Model 1, 1C, 2, or 2C) or 3268 Model 2 or 2C Printer is optional for hard-copy output. Device address X'01F' or X'009' would normally be used for the display/keyboard.

For printer-keyboard mode, the message area for operator-to-operating system communication consists of lines 1 to 18. All of line 19 and the first 46 characters of line 20 are the operator input area that displays the data the operator keys in (up to 126 characters). Character positions 48 through 79 of line 20 are used as an indicator area. Lines 21 to 25 are used for the same functions as when display mode is in effect. When a 3287 or 3268 Printer is designated for hard copy, data entered via the keyboard and displayed on the screen is automatically written to the 3287 or 3268 Printer.

When printer-keyboard mode is in effect, the screen is treated like a printer-keyboard device. Messages appear on the screen in successive lines until the screen becomes full. Then the top six lines are deleted automatically by the hardware and the remaining lines are moved up to leave six blank lines in positions 13 to 18. Since the operator cannot control the contents of the screen, as with display mode, the 3287 or 3268 Printer is recommended for hard-copy output.

In printer-keyboard mode, the 3205, 3278 Model 2A, or 3279 Model 2C is controlled using 3210/3215 commands. The display/keyboard and optional 3287 or 3268 Printer have the same address and the same data is automatically printed on the 3287 or 3268 as is displayed on the screen. A maximum of two of the natively attached 3278 Model 2A and/or 3279 Model 2C displays can be operating in printer-keyboard mode. Each can have an associated hard-copy printer.

### **Operator Control Panel**

The operator control panel for a 3205 primary console can be attached to the 3205 unit or located separately from the 3205. For a primary 3278 Model 2A or 3279 Model 2C console, the operator control panel is located on the keyboard of the console. The operator control panel contains the following pushbutton controls and indicators:

- **Power on/IML pushbutton.** When this pushbutton is pressed, a power-on of the support processor subsystem and IML of the support processor occur. At the successful completion of these operations, the balance of the 4381 Processor (including the Channel-to-Channel Adapter if installed) is powered on as are all I/O devices that are set to be powered on/off with the processor. An IML of instruction processing function microcode occurs automatically if

the operator has specified an automatic IML after power-on using the System Configuration-Customer display.

Then a power-on reset of the 4381 Processor (clear reset and time-of-day clock reset) is performed. The processor is placed in the stopped state and the Program Load display is shown on the operator console. When a power-on is not successful, an IML and reset do not occur. This pushbutton is also used to perform an IML of the support processor only when power is already on.

The natively attached 3205 or 3278 Model 2A and/or 3279 Model 2C displays and 3287 and/or 3268 Printers must be powered on individually. Power to these natively attached devices should be turned on before the Power on/IML pushbutton is pressed. At least one display console must be powered on in order to power up a 4381 Processor. The Channel-to-Channel Adapter must be enabled using the channel-to-channel pushbutton.

- **Power-off pushbutton.** This pushbutton is used only to remove power from the 4381 Processor (not the 3205, 3278, and 3279 displays or 3287 and 3268 printers) under control of the power-off sequencing microcode that is resident in the support processor.
- **Channel-to-channel pushbutton.** When the optional Channel-to-Channel Adapter is installed, this pushbutton is used to enable and disable the logical interface to the other processor to which the adapter is attached.
- **Chan-chan disabled indicator.** This indicator is lit to indicate the Channel-to-Channel Adapter logical interface to the other processor is not enabled. This indicator should be on before the 4381 Processor is powered off. In addition, before a 4381 Processor with the Channel-to-Channel Adapter is powered on or off, the processor to which the adapter is attached should be soft stopped to ensure its operation is not impacted.
- **Power-in-process indicator.** This light turns on as soon as the power-on/IML pushbutton is pressed and stays on until power-on sequencing of all system components is successfully completed, at which time it is turned off. This light also turns on during a power off sequence.
- **Power-complete indicator.** When lit, this light indicates power is on. It is turned on at the successful completion of a power-on sequence when the power-in-process indicator is turned off.
- **Basic check indicator.** When this indicator is lit, a hardware malfunction exists in the support processor or the processor is in CE mode.
- **System indicator.** This indicator is lit whenever instruction processing or I/O data transfer is taking place.
- **Wait indicator.** This indicator is lit when instruction execution is not occurring because the current PSW has the wait bit on. For a 4381 Model Group 14 or 3, this indicator is lit if either instruction processor is in the wait state.
- **Lamp test pushbutton.** When pressed, this pushbutton causes all functional indicator bulbs on the operator control panel to be lit and is used for testing purposes.

## Keyboard

There are 75 keys on the keyboard. Certain keys have a normal and an alternate function. The alternate function is selected by holding the ALT key down and pressing the desired functional key.

In addition to alphabetic, numeric, cursor control, and keyboard control, the following keys are provided:

- **MODE SEL/DIAG.** This key is used to initiate use of the display screen for manual operations instead of operator-to-operating system communication (switch from system to manual mode). Activation of the mode select function invokes a general selection display that lists the manual functions the operator can perform. The specific mode selection display shown depends on whether System/370 or System/370-XA mode is in effect. Activation of the DIAG function causes a diagnostic program (the Test Case Monitor discussed in Section 60:15) to be loaded into the support processor and executed.
- **CHG DPLY.** This key causes a switch between system and manual modes and a switch in the display currently being shown.
- **CNCL (PA2).** When system mode is in effect, this key causes an attention interruption (PA2 type) to be generated for display mode operations or a unit exception when printer-keyboard mode is in effect. The key is active only in specific cases when manual mode is in effect.
- **INTR/LINE DISC.** When the INTR function is selected, an external interruption occurs. The LINE DISC function is used to terminate operation of the Remote Support Facility or Remote Operator Console Facility.
- **REQ (PA1)/COMM REQ.** When the REQ function is selected, an attention interruption (PA1 type) is generated for display mode. An attention interruption without the PA1 indication is generated when printer-keyboard mode is in effect. The COMM REQ function is used to request communication between a local and remote customer engineer when the Remote Support Facility is active or to request communication between the host and remote locations when the Remote Operator Console Facility is active.
- **COPY.** When this key is pressed, the contents of lines 1 through 24 of the current display are written to the locally attached 3287 or 3268 Printer that has been designated to receive copy-key data. This key is functional at all times.
- **START and STOP keys.** These keys are used to start and stop instruction processing.
- **Page up and page down keys.** These keys increase and decrease addresses during manual operations. The increment/decrement depends on the operation being performed.
- **Program function keys 1 to 12.** These keys are effective only when the ALT key is pressed. The function performed by each of these keys is defined via programming.

- SP/MO key (alternate function for the ERASE EOF key). This support processor manual operations key is active only when the CE mode is active and is used to invoke manual operations (read, display, modify, instruction step, for example) for support processor microcode for debugging purposes.

## System Configuration Displays

One system configuration display for customer use and one for the customer engineer are provided. Each can be selected from the General Selection display. Configuration data about the 4381 Processor is displayed when the System Configuration-Service display is selected. The customer engineer can use this display to change configuration data.

The System Configuration-Service display indicates the processor type and model number, processor serial number, diskette serial number along with its engineering change level and latest REAs, number of the installed Power Logics, Bill of Material of the processor, processor storage installed, control storage size, the presence of a Remote Operator Console Facility modem or not, the presence of a Channel-to-Channel Adapter or not, and number of channels installed.

The System Configuration-Customer display is provided to enable the operator to configure system functions and request displays for configuring I/O functions. This display is used to set and/or display the following:

- The diskettes mounted on each diskette drive (display only)
- I/O power-on timeout (number of minutes to wait for automatic powering of I/O devices)
- Whether an automatic IML is to be performed at power-on time
- Whether an automatic IML and IPL are to be done at power-on time
- Whether one or both instruction processing functions in a Model Group 14 or 3 processor are to be activated (set uniprocessor or dual processor mode of operation)
- Console mode (display or printer-keyboard)
- Printer assignment for the copy key
- Mode for channel 5 (byte or block multiplexer)
- Configuration information for the natively attached I/O devices

The System Configuration-Customer display is also used to select the I/O configuration display. This display is used to select other displays that are used to enter/display UCW information for System/370 mode and to execute the IOCP to create/update the I/O configuration data set for System/370-XA mode.

## 40:10 Operator Displays

Several displays are provided that enable the operator to perform manual operations. The functions the operator can perform are listed in the General Selection display. Each function has a single or multiple-character identification associated with it. The operator selects the function to be performed by keying in the associated identification. Certain functions have their own display associated with them.

### General Selection Display

The General Selection display for operator use is shown in Figure 13. When CE mode is in effect, additional functions that can be utilized only in CE mode are listed as well. The General Selection display is automatically displayed when manual mode operations are initiated and can be selected by pressing the mode select key. This display can also be selected from other operator displays.

GENERAL SELECTION	
Y TIME-OF-DAY ENABLE	F CONFIGURATION/REMOTE
J INTERVAL TIMER SWITCH	L PROGRAM LOAD
S STORE STATUS	A COMPARE/TRACE
N SYSTEM RESET-NORMAL	K CHECK CONTROL
C SYSTEM RESET-CLEAR	O OPERATION RATE
R RESTART	D DISPLAY/ALTER
T TARGET PU-SWITCH	B BLOCK/PATCH
P PROBLEM ANALYSIS	E ERROR DISPLAYS
Z RETURN TO PROG SYS	

COMMAND:

Figure 13. The General Selection display

The functions listed on the General Selection display are the same for System/370 and System/370-XA modes with one exception. When System/370-XA mode is in effect, the interval timer function is not listed.

The operator displays provided for 4381 Processors are very similar to those provided for 4341 Processors. For discussion of the contents and use of the displays for 4381 Processors, see *IBM 4381 Processor Operations Manual*

(GA24-3949). This manual also identifies operational similarities and differences for 4381 and 4341 Processors and enhancements made for 4381 Processors.

## 40:15 Remote Operator Console Facility (ROCF)

ROCF support in the support processor of a remote 4381 Processor provides the ability to:

- Dial up and control a remote powered-on 4381 Processor from a 3275 Model 2 Display Terminal at a host location, as shown in Figure 14. The operator at the host location can perform all the supported 4381 manual control functions (IPL, instruction processor function IML, display, alter, etc.) using the 3275 display that can be performed using a local console except for a power-on of the 4381 system and functions that require manual operation at the 4381 site (support processor IML, diskette change, for example). A DOS/VSE, VS1, MVS/370, MVS/XA, or VM/370 operating system can be IPLed in the 4381 Processor via a remote 3275 display.

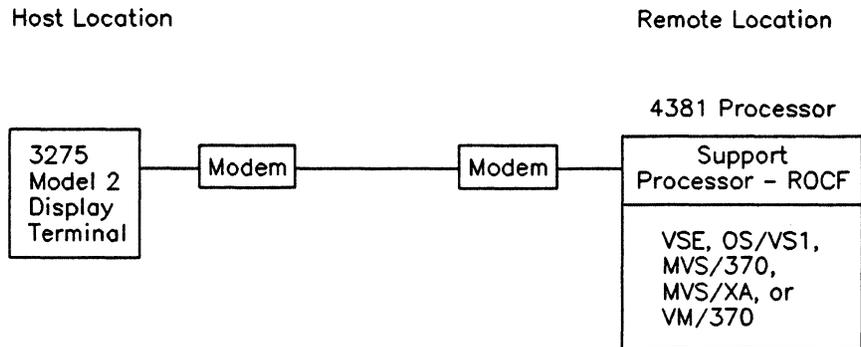


Figure 14. Dialup of a remote 4381 Processor via a 3275 display

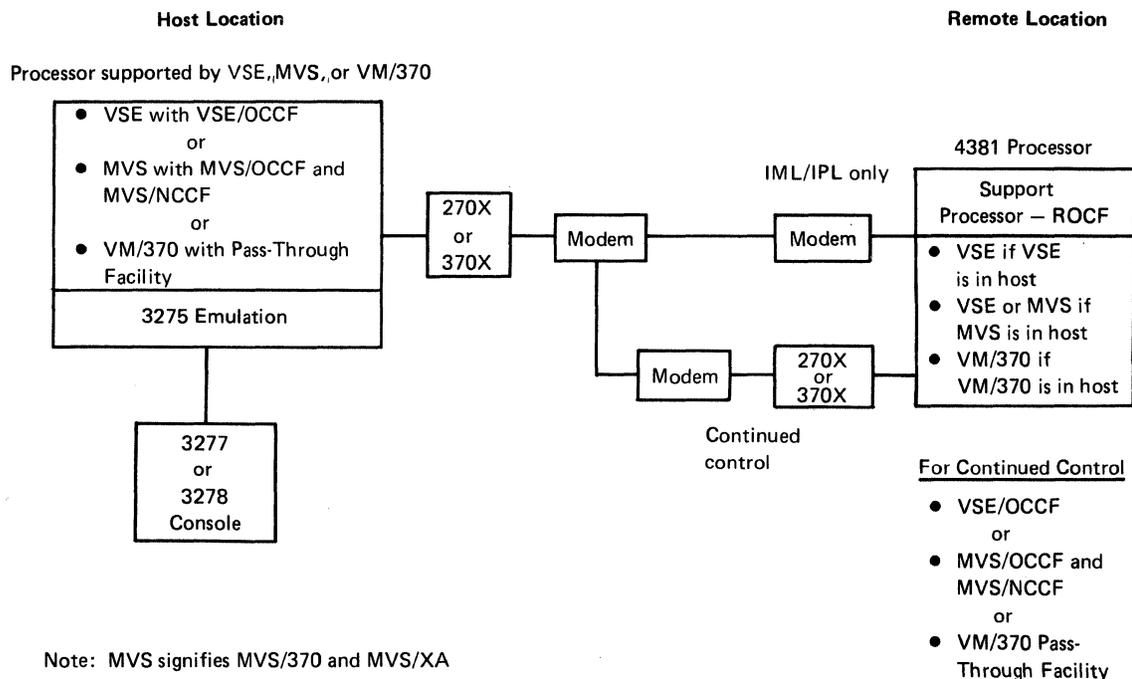
Once the 4381 Processor is operating, the operator at the 3275 display can disconnect the 3275 from the RSF port in the 4381 Processor. The 4381 support processor will then enable autoanswer mode so that a remote dialup via a 3275 is again possible. If continued control of jobs in the remote 4381 Processor is desired, a normal teleprocessing network (involving 270X and/or 370X controllers) should be used.

- Dial up and control a remote powered-on 4381 Processor from a 327X display connected to a host processor that is emulating a 3275 display, as shown in Figure 15 on page 92. The 327X display can be used to perform the same manual functions as can a stand-alone 3275 at the host location discussed above. Once the 4381 Processor is operating, the 327X can be disconnected from the ROCF link and a standard communication network can be established if continued control of the jobs in the remote 4381 Processor is required. The host processor used to dial up and control the jobs in the remote 4381 Processor must be running under the control of MVS/370, MVS/XA, or VM/370.

For an MVS environment, MVS/SP-JES2 Version 1 as of Release 3.2, MVS/Operator Communication Control Facility (MVS/OCCF), and MVS/Network Communications Control Facility (MVS/NCCF) as of Release

2 must be present in the host processor in order to initialize the remote 4381 Processor. The remote 4381 Processor must use an MVS operating system. If continued control of the jobs in the remote 4381 Processor via a standard communications network is required, the remote 4381 must also be running under MVS/370 or MVS/XA with MVS/OCCF and MVS/NCCF.

For a VM/370 environment, the VM/Pass-Through Facility as of Release 2 is required in the host processor to initiate remote 4381 Processor operation. The remote 4381 Processor must use VM/370. If continued control of the jobs operating in the remote 4381 Processor is desired, VM/SP as of Release 2 with the Programmable Operator Facility is required in the remote 4381 Processor.



**Figure 15. Dialup of a remote 4381 Processor via a host processor emulating a 3275 display**

When ROCF support is present in a 4381 support processor, an ROCF Installation display is provided. This display allows an operator at the 4381 Processor site to enable and disable ROCF mode. When ROCF is enabled, the ROCF function is automatically activated during each IML of the support processor in the 4381 Processor. This activation permits remote dialup of the 4381 Processor. When ROCF mode is disabled, the ROCF function is not activated and a remote dialup of the 4381 Processor is not possible.

Password protection is supported to prevent unauthorized access to the remote 4381 Processor. When a dialup of a remote 4381 Processor occurs, the first display sent to the host location is the ROCF Password display. The operator at the host location must enter the correct password within a certain time interval or the telephone link between the 4381 Processor and host location is automatically disconnected. If the password is correct, the next display sent to the host location is the General Selection display. At this time, the host operator can select functions to display hardware information, IML or IPL the system, or return to operating system displays.

A local/remote switch function is also supported for ROCF when the optional keylock feature is present on the operator console display for the 4381 Processor. When the 4381 operator console is locked, its keyboard is disabled and the screen remains blank. Console input can be entered into the 4381 Processor only via the ROCF console at the host location when the ROCF line is active. In addition, the screen of the 4381 Processor operator console remains blank. Any messages for the operator console are sent to the console of the host location, if one is connected.

When the 4381 operator console is unlocked, console input to the 4381 Processor can be entered via the 4381 operator console and the console at the host location, if a console is connected. Messages to the console are displayed on the 4381 operator console and the console at the host location, if a console is connected.

## 40:20 Maintenance

The *IBM 3278 Model 2A Display Console Problem Determination Guide* (GA23-0020), *3279 Color Display Station Problem Determination Guide* (GA33-3094), or *3205 Color Display Console Operator Reference and Problem Determination Guide* (GA18-2399), depending on the type of console installed, is provided with each 4381 Processor. These guides contain problem determination and abbreviated operating and reference information. The *IBM 4381 Processor Operations Manual* (GA24-3949) also contains problem determination procedures. If the operator console malfunctions, the operator can take the steps outlined in the guides before calling the customer engineer.

## Section 50: Virtual Storage and Address Translation

When a 4381 Processor is operating in System/370 and EC modes or in System/370-XA mode, dynamic address translation (DAT) hardware is made operative by turning on the translation mode bit in the current PSW. When DAT is operative, virtual storage addresses in programs referring to instructions and data are translated into real storage addresses after instructions are fetched during program execution. The address in the instruction counter is translated also. When DAT is not operative and System/370 or System/370-XA mode is in effect, storage addresses in programs are used as real storage addresses.

When DAT is operative, the storage addresses in CCW lists are not translated by channel hardware during channel program operation. The channel indirect data addressing feature, also standard in 4381 Processors, and programmed channel program translation are used for address translation for channel programs for both System/370 and System/370-XA modes.

The following privileged instructions are associated with the dynamic address translation facility: LOAD REAL ADDRESS (LRA), RESET REFERENCE BIT (RRB) for System/370 mode only, RESET REFERENCE BIT EXTENDED (RRBE), INVALIDATE PAGE TABLE ENTRY (IPTE), and PURGE TLB (PTLB).

### Virtual Storage Organization

The 4381 Processors operating in System/370 mode support a virtual storage size of 16Mb (16,777,216 bytes) using a 24-bit address. A virtual storage segment size of either 64K or 1024K bytes, is implemented. With either segment size, the page size can be 2K or 4K for all 4381 models except 14 and 3 for which page size is always 4K bytes. A segment size of 64K bytes is supported by DOS/VSE, OS/VS1, MVS/370, and VM/370. For 4381 Processors with more than 16M-bytes installed, only 4K-byte pages can be used.

While a 16Mb virtual storage is always available for System/370 mode operations as far as the DAT hardware is concerned, the actual amount of virtual storage to be supported for a given 4381 Processor is defined by the installation when a DOS/VSE or VS1 operating system is generated. DOS/VSE with VSE/Advanced Functions Release 2.1.0 supports up to three virtual storages. Each can be up to 16Mb in size with a maximum of 40Mb supported for the three virtual storages. MVS/370 supports multiple 16Mb virtual storages and VM/370 supports a virtual storage up to 16Mb for each virtual machine.

The 4381 Processor operating in System/370-XA mode supports a virtual storage size of 2Gb (2,147,483,648 bytes) using a 31-bit address. A virtual storage segment size of 1024K bytes and a page size of 4K bytes are implemented for

System/370-XA mode and supported by MVS/XA. Multiple virtual storages of 2Gb each are supported by MVS/XA.

## Address Translation

The address translation process (a two-level table lookup) using segment and page tables and the DAT hardware is the same in 4381, 30XX, System/370, and other 4300 processors, as described in *IBM System/370 Principles of Operation* (GA22-7000) and *IBM System/370 Extended Architecture Principles of Operation* (SA22-7085).

However, there are differences in the format and contents of the segment and page table entries for System/370 and System/370-XA modes of operation. In addition, a 24-bit address is generated for System/370 mode and a 31-bit address is generated for System/370-XA mode.

For System/370 mode of operation, the segment table entry has page table length, page table origin (to supply a 24-bit address), segment protection, common segment, and segment invalid fields. The segment protection bit in an entry controls whether storing is permitted into the associated segment of virtual storage. When this bit is zero, both fetching and storing are permitted for the segment. When this bit is on, only fetching is permitted and a program interruption for protection occurs if a store is attempted. The common segment bit is used with the translation lookaside buffer (TLB), as described below.

For System/370-XA mode of operation, the segment table entry has page table length, page table origin (to supply a 31-bit address), common segment, and segment invalid fields. The common segment bit is functionally the same for System/370 and System/370-XA modes. The common segment bit indicates whether a page is contained in a private or common segment. The common segment bit indicates the pages in the segment have the same addresses in every virtual storage in which they appear. The common segment bit is used to avoid invalidating entries in the TLB that are identified as common when the TLB must be purged in a multiple virtual storage environment (such as MVS/370, MVS/XA, or VM/370).

For System/370 mode of operation, the page table entry (a two-byte entry) has a page frame address (to supply a 24-bit address) and an invalid bit. One bit is available for programming use. One extended storage address bit in a page table entry (defined for the Extended Addressing feature) is used in 4381 Processors with more than 16Mb installed.

For System/370-XA mode of operation, the page table entry (a four-byte entry) has a page frame address (to supply a 31-bit address), invalid bit, and page protection bit. Eight bits are available for program use. The page protection bit controls whether storing is permitted into the associated page of virtual storage. When this bit is zero, both fetching and storing are permitted for the page. When this bit is on, only fetching is permitted and a program interruption for protection occurs if a store is attempted.

## Translation Lookaside Buffer

The time required for address translation utilizing the DAT hardware for System/370 or System/370-XA mode is eliminated if the translation lookaside buffer can be used for the translation. A translation lookaside buffer is implemented primarily to minimize the amount of time required to perform address translation when DAT mode is enabled.

However, in a 4381 Processor, the TLB is also used when System/370 mode is in effect for BC mode operations and when EC mode is in effect without DAT enabled. The TLB is used also for System/370-XA mode when DAT is not enabled. The TLB is used for all modes so that the same microcode can be used, regardless of the other modes in effect, and because accessing the protect key in the TLB is faster than accessing the key stack.

The TLB contains 32 rows and 2 columns. Each row contains two entries (one per column). Each entry contains one address translation, three status bits, a five-bit store and fetch protect key, a common segment bit, and a page protect bit (to support segment protection in System/370 mode and page protection in System/370-XA mode). One least recently used (LRU) bit is associated with each row (pair of entries) to determine which column to assign when a new translation is loaded.

Two instructions are provided to perform programmed TLB invalidation. When the INVALIDATE PAGE TABLE ENTRY (IPTE) instruction is issued, the specified page table entry is invalidated and the TLB is inspected by hardware for entries that use the now invalid page table entry. This instruction eliminates the need to purge the entire TLB when only one TLB entry is invalidated.

All entries in the TLB are automatically invalidated when the segment or page size in effect changes. The PURGE TLB instruction provides the capability of invalidating all the TLB entries by programming (such as when control is switched from one virtual storage to another). Any TLB entry with its common segment bit on is not invalidated when TLB purging is done. The control program purges the TLB as required.

Operation of the TLB cannot be disabled in a 4381 Processor. If an error occurs in the TLB, the instruction in execution when the error occurred is retried if it is a retryable instruction. For unretryable or uncorrectable errors, a machine check error condition (system damage or instruction processing damage, depending on the instruction being executed) exists.

## **Section 60: Reliability, Availability, and Serviceability (RAS)**

### **60:05 Introduction**

The objectives of the RAS features of 4381 Processors are to (1) reduce the frequency and impact of system interruptions that are caused by hardware failure and that necessitate a re-IPL and (2) reduce the time required to locate and repair malfunctions. RAS features of 4381 Processors are as follows:

- Hardware reliability is enhanced through use of inherently more reliable logic technology packaging than was used in previous intermediate-scale processors.
- Recovery facilities, both hardware- and program-supported, are provided to reduce the number of failures that cause a complete system termination. This permits deferred maintenance.
- Extensive diagnostic facilities are provided that are designed to reduce problem location and repair time.

Each availability and serviceability feature is discussed in the remainder of this section. The following recovery/repair features are implemented in hardware and microcode:

- Automatic retry of instructions when an instruction processing function error occurs during the execution of most instructions. Hardware reconfiguration facilities are also implemented to permit continued system operation when solid failures occur in certain hardware components.
- ECC validity checking on processor storage to correct all single-bit and detect all double-bit and most multiple-bit errors. Most types of double-bit errors can also be corrected via microcode.
- I/O operation retry facilities, including channel retry data provided in the limited channel logout area (for System/370 mode) and channel/control unit command retry procedures to correct failing I/O operations
- Expanded machine check interruption facilities to support better error recording and recovery procedures
- Machine check error diagnosis (reference code generation) and logging by the support processor to aid the customer engineer in faster problem determination and to provide the ability to record errors even when the instruction processing function malfunctions

- Microcode-controlled power sequencing and power and temperature monitoring performed by the support processor

The following diagnostic facilities are provided:

- Online Test Executive Program (OLTEP) and Online Tests (OLTs) that execute under operating system control and provide online diagnosis of channel-attached I/O devices for most devices that attach to 4381 Processors
- System Test for checking the basic operating capability of a 4381 Processor
- Problem analysis routines provided in microcode that the operator can execute to aid in hardware fault location
- Microdiagnostics for the components of a 4381 Processor (instruction processing function, processor storage, support processor, etc.)
- Manual operations that the customer engineer can perform using the operator console and appropriate support documentation
- A Remote Support Facility that enables the on-site customer engineer to access a remote data bank and allows malfunction diagnosis to be performed by a remote customer engineer at a support center

The hardware and programmed recovery aids are designed to improve system availability. Hardware reconfiguration is used where possible to permit the system to run with normal performance or in a degraded mode, when necessary, so that maintenance can be deferred. When solid failures that cannot be circumvented do occur, their impact can be reduced by utilizing the expanded diagnostic facilities, such as Problem Analysis, which are designed to reduce the time required to isolate and repair a malfunction.

## 60:10 Recovery Features

Additional hardware and microcode, which attempts correction of most hardware errors without programming assistance and performs certain reconfiguration operations, is included as a basic part of a 4381 Processor. The control program can be notified, via an interruption, of both intermittent and solid hardware errors so that error recording and recovery procedures can take place.

### Automatic Instruction Retry

If a hardware error is detected during the execution of instructions, the failing instruction is automatically retried once by the processor without programming assistance if it is a retryable instruction. The error retry procedure is initiated by the support processor. The data required for a retry is saved during the execution of instructions.

The following instructions are retryable at any point during their execution (see *System/370 Principles of Operation* for the instructions in each instruction group):

- All general instructions except SET PROGRAM MASK (includes binary arithmetic instructions)
- All decimal and floating-point instructions
- Control instructions whose names begin with STORE except for STORE THEN AND SYSTEM MASK and STORE THEN OR SYSTEM MASK

The instructions not contained in the groups listed above are initially retryable but become unretryable at some point during their execution. Note that retry is also performed if an error is detected during the execution of interruption handling microcode.

If the instruction retry is successful, a machine check interruption is taken, if the processor is enabled for recovery interruptions, so that error recording can be done by the operating system. If the instruction cannot be retried at all or if the retry is unsuccessful in correcting the error, a machine check interruption occurs, if the processor is enabled for such interruptions, and programmed error recovery procedures should be executed by the operating system.

The retry facility in 4381 Processors includes an automatic hardware reconfiguration function that is not implemented in 4341 Processors. A reconfiguration procedure is implemented for errors that occur in the high-speed buffer, control storage, channel data buffer, and swap buffer, as previously described.

When reconfiguration is done, a record describing the reconfiguration is written to functional diskette 1. Therefore, if a re-IML is done, the 4381 Processor is returned to its reconfigured state as indicated in the reconfiguration records. The reconfiguration records are updated as appropriate when a repair operation is performed.

The instruction retry feature provides a 4381 Processor with the ability to recover from many intermittent processor failures that would otherwise cause a system halt and necessitate a re-IPL or that would cause an executing program to be terminated. Corrected errors are logged by recovery routines for later diagnosis, thereby increasing system availability. Reconfiguration functions permit continued processor operation after certain solid hardware failures, thereby allowing maintenance to be deferred.

## **ECC Validity Checking On Processor Storage**

The ECC method of validity checking on processor storage provides automatic single-bit error detection and correction. It also detects all double-bit and many multiple-bit processor storage errors. Certain types of double-bit errors are also corrected via a microcode procedure. Double-bit error correction is not implemented in other 4300 Processors except in 4361 Processors.

Validity checking for processor storage is handled on an eight-byte basis, using an eight-bit code, rather than on a single-byte basis, using a single parity bit. However, parity checking is still used to verify other data in a 4381 Processor that is not contained in processor storage.

As data enters and leaves processor storage, ECC logic performs validity checking on each doubleword. When a doubleword (72 bits) is fetched from processor storage, the eight-bit ECC code is checked to validate the 64 data bits. If the data is correct, the appropriate parity bit for each of the eight data bytes is generated and the doubleword is reformatted so that each eight data bits are followed by a parity bit. If a single-bit error is detected, the identified data bit in error is corrected automatically by ECC logic with no additional fetch time.

When a doubleword is to be placed in processor storage by a program, the eight parity bits are removed and the eight-bit ECC code is generated and appended to the 64 data bits. The 72 bits are then stored with the ECC bits.

If a double- or multiple-bit error occurs during instruction execution and the instruction is retryable, it is retried one time. If the double-bit or multiple error does not recur, processing continues. Otherwise, for a double-bit error, correction may be attempted depending on the type of double-bit error.

In a dynamic storage, alpha particles (defined as radiation from the packaging materials and solder used in processor storage) can cause the state of a bit position to change. That is, alpha particles can remove the charge stored in a capacitor that represents a bit position. A state change causes a single-bit error (an intermittent error) in a doubleword that has no solid single-bit error. Such a single-bit error can be corrected by ECC logic as usual. However, if a doubleword has a solid single-bit error, a bit change caused by an alpha particle results in a double-bit error (one solid error and one intermittent error), which is uncorrectable by ECC logic. Double-bit error correction is implemented primarily to correct double-bit errors consisting of one alpha particle caused intermittent error and one solid error.

The following procedures are performed to handle double-bit errors that are detected in a doubleword above or below the ACB in processor storage (that is, in the user-addressable or auxiliary storage area):

- For one solid and one intermittent error, the syndrome bits are used to correct the intermittent error in the doubleword in processor storage. The operation is retried and ECC logic corrects the single-bit solid error. A system recovery machine check interruption is generated with storage error corrected indicated in the machine check code (bit 17 is turned on).
- For two solid errors, the two error bits are corrected in the doubleword in the buffer. A machine check interruption is generated with storage degradation indicated in the machine check code (bit 19 is turned on). The operating system should unload the data with the error to a different location in processor storage to avoid repetition of a double-bit error when the doubleword is fetched again.
- For two intermittent errors in the program addressable area, a machine check interruption is generated with storage error uncorrected specified in the machine check code (bit 16 is turned on). For two intermittent errors in the auxiliary storage area, a timing facilities damage machine check interruption is generated if the double-bit error occurred in the CPU timer or clock comparator area of auxiliary storage. If not, for System/370 mode, a system damage machine check interruption is generated. For System/370-XA mode, system damage is reported unless the error is located in a doubleword that contains channel or subchannel data, in which case channel subsystem damage is reported.

When a double- or multiple-bit processor storage error occurs during an I/O operation, it is reported during the ensuing I/O interruption so that error recording and I/O retry procedures can be executed.

The ECC feature and double-bit error correction increase the availability of 4381 Processors by permitting system operation to continue normally and without abnormal job terminations after single-bit and certain double-bit processor storage errors occur and are corrected.

## I/O Operation Retry

Channel retry and command retry features (like those for System/370 and other 4300 processors) are provided to reduce the number of abnormal program terminations and unscheduled system halts that occur because of I/O errors.

Channel retry is implemented to ensure that most failing channel operations can be retried by error-handling routines. A limited channel logout area is implemented for System/370 mode of operation. When a channel error or a processor error associated with a channel operation occurs, the channel status word (CSW) and a limited channel logout word are stored in the fixed lower processor storage area (locations 176 to 179) during the I/O interruption. The limited channel logout data provides additional, more exact status information about the channel failure. The CCH routine passes this data to a device-dependent error recovery routine to be used in the retry of the failing I/O operation.

Command retry for System/370 and System/370-XA modes is a channel/control unit procedure that can cause an improperly executed command in a channel program to be retried automatically by hardware so that an I/O interruption and programmed error recovery are not required. An indication is presented when the control unit recognizes this situation.

In 4381 Processors, the command retry capability is implemented for the block multiplexer channels and can be utilized with 3370, 3375, 3380, 3330-series, and 3350 disk storage.

## Machine Check Facilities

A 4381 Processor presents one of seven types of machine check interruption conditions, depending on the specific machine malfunction, and each type of interruption is maskable. The interruption types implemented for System/370 and System/370-XA modes vary slightly.

Machine check interruption conditions are either *repressible* or *exigent*. A repressible machine check condition exists in the 4381 Processor after an error has occurred that does not prevent continued successful execution of instructions (successful instruction retry, for example). An interruption can occur after a repressible machine check condition so that the failure can be recorded. System operation continues after the error is logged.

An exigent machine check condition exists when an uncorrectable error (such as an unretryable or uncorrectable instruction failure) occurs. Exigent conditions are those that prevent the successful execution of the current instruction.

For 4381 Processors, as for other 4300 Processors, the fixed area is 512 bytes and no processor-dependent data is stored within these 512 bytes. This approach is different from that implemented in System/370 processors (except 308X and 3090 Processor Units) in which processor-dependent data is stored in certain fields in locations 0 to 511 and a processor-dependent extended logout is also stored when a machine check interruption occurs (usually beginning at location 512). The length of the processor-dependent extended logout varies by System/370 processor.

The approach taken in 4381 and other 4300 Processors permits a processor-independent (1) fixed area size, (2) machine check handler routine, and (3) logout data interpreting and printing routine (EREP) to be used. This approach removes operating system portability constraints for 4381 and other 4300 Processors that exist for System/370 processors because of processor-dependent logouts.

A logout to appropriate fields in processor storage locations 0 to 511 occurs in a 4381 Processor when any type of machine check interruption is taken. The logout data indicates the reason for the interruption in machine check code (locations 232 to 239). The save areas in locations 216 to 511 in the fixed area preserve the status of the processor at the time of the machine check interruption and contain the contents of the general, floating-point, and control registers as well as CPU timer and clock comparator values.

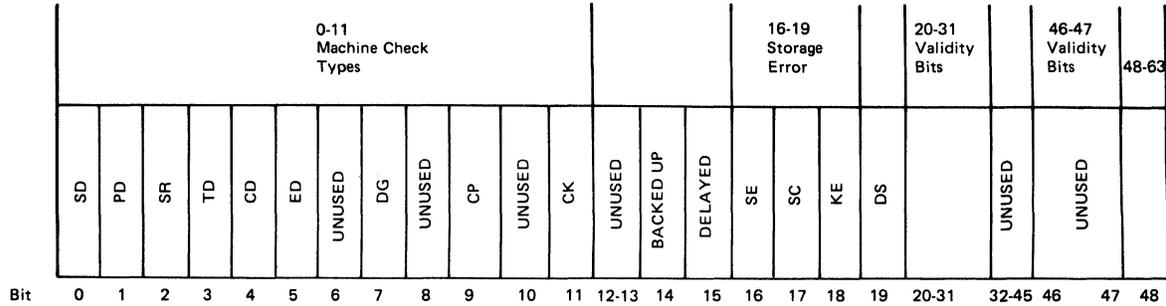
Figure 16 on page 103 shows the layout and contents of the eight-byte machine check code for 4381 Processors that is stored in processor storage locations 232 to 239. The machine check code indicates which type of interruption occurred and the validity of certain fields stored in the fixed area.

Figure 17 on page 105 lists the machine check types defined for 4381 Processors and the mode(s) for which they are implemented (System/370 and/or System/370-XA). They are described in the discussion that follows. The mask bits used to enable or disable the processor for interruptions for each type are indicated and the setting of the machine check code is discussed.

PSW bit 13 and four other mask bits are used to enable and disable the processor for machine check interruptions. The recovery (R), degradation (D), external damage (E) for System/370 mode or timing facilities damage (T) for System/370-XA mode, and channel status (C) mask bits are contained in control register 14 and operate subject to PSW bit 13. If PSW bit 13 is off, the processor is disabled for all machine check interruptions. If PSW bit 13 is on, the settings of the four additional mask bits determine whether interruptions for repressible machine check conditions will be taken.

Note that these mask bits control logouts to processor storage locations 0 to 511 only. They do not control logging to functional diskette 1, which is controlled by the setting established via the operator console (check control display).

Fixed Logout Area Locations 232-239



Bit	Interruption Type	Bit	Storage Error	Bit	Valid Fixed Area Data
0	SD—System Damage	15	Delayed (S/370 only)	20-23	Machine Check Old PSW (48-55)
1	PD—Instruction Processing Damage	16	Storage Error		20 AMWP
2	SR—System Recovery		Uncorrected		21 Masks and Protect Key
3	TD—Timer Damage (S/370 only)	17	Storage Error		22 Program Mask and Condition Code
4	CD—Timing Facilities Damage		Corrected	24	23 Instruction Address
5	ED—External Damage (S/370 only)	18	Key in	25	Failing Storage Address (248,249)
7	DG—Degradation		Storage Error	26	Unused
9	CP—Pending CRW Report (370-XA only)	19	Storage Degradation	27	External Damage Code
11	CK—Channel Subsystem Damage (370-XA only)		Uncorrected	28	Floating Point Registers (352-383)
14	B—Backed up			29	General Registers (384-447)
				30	Control Registers (448-511)
				31	Unused
					Storage (Validity of processor storage being processed by instructions when interruption occurred)
				46	CPU Timer Value
				47	Clock Comparator Value

Figure 16. 4381 Processor machine check code

Repressible Machine Check Interruptions

Repressible machine check interruptions are the following:

- Interval Timer Damage. This interruption can occur if PSW bit 13 and the external damage mask bit are on to indicate damage to the interval timer in System/370 mode. The TD bit is stored in the machine check code. An interval timer is not implemented for System/370-XA mode of operation.
- Timing Facilities Damage. This interruption can occur when PSW bit 13 and the external damage mask (for System/370 mode) or timing facilities damage mask (for System/370-XA mode) bit are on. It indicates damage to the time-of-day clock, CPU timer, or clock comparator. The CD bit is stored in the machine check code. No differentiation among errors in these three timing facilities is made because of the implementation used. If one facility is failing, none is usable, since a time-of-day clock and a hardware decremter are used to implement the three timing facilities.

An interval timer/timing facilities damage machine check interruption is generated when the time-of-day clock enters the error state as a result of a detected malfunction that could have affected the validity of the clock value or when damage to the interval timer, CPU timer, or clock comparator occurs. This interruption (with instruction processing damage as well as timer damage indicated) is also taken when (1) a SET CPU TIMER or STORE CPU TIMER

instruction is issued to a damaged CPU timer or (2) a SET CLOCK COMPARATOR or STORE CLOCK COMPARATOR is issued to a damaged clock comparator.

- **Recovery Report.** This interruption can occur when PSW bit 13 and the recovery report mask bit are on. It indicates the instruction retry facility was successful in correcting a retryable malfunction that occurred during the execution of an instruction, a double-bit error in processor storage was corrected, or channel data buffer or high-speed buffer reconfiguration was done without loss of data.
- **External Damage.** This interruption can occur when PSW bit 13 and the external damage mask bit are on. It is implemented only for System/370 mode. The ED bit is stored in the machine check code, and the external damage code at location 244 indicates the reason for the interruption.

External damage bits 2, 3, and 4 are implemented in 4381 Processors to indicate (1) a processor storage error or protect key error was not corrected during an I/O operation, (2) one or more channels have detected an error of such severity that operations cannot continue and each has entered the not-operational state while signaling system reset to their attached devices (channel-not-operational condition), or (3) one or more channels have lost power or detected an error of such severity that operations cannot continue and all these channels may not have signaled system reset to their attached devices (channel control failure condition).

- **Degradation.** This interruption can occur when PSW bit 13 and the external damage mask bit are on. Degradation is set when a portion of the high-speed buffer is deleted (malfunctioning bit is turned on in a directory entry).
- **Pending Channel Report.** This interruption can occur during System/370-XA mode of operation if PSW bit 13 and the channel status mask bits are on to indicate one or more channel report words are pending. Channel report words provide information related to a channel subsystem recovery or the completion of a RESET CHANNEL PATH instruction.
- **Channel Subsystem Damage.** This interruption can occur during System/370-XA mode of operation when PSW bit 13 is on. It indicates a multiple-bit or uncorrectable double-bit error occurred in channel or subchannel data located in auxiliary storage.

Mode	Mask Bit(s)	Interruption Type and Cause	Machine Check Condition
S/370 370-XA	PSW 13 and R	System Recovery <ul style="list-style-type: none"> <li>• Error during instruction execution corrected by instruction retry</li> <li>• Double-bit processor storage error corrections</li> <li>• Reconfiguration without loss of data (channel data buffer or high-speed buffer reconfiguration)</li> </ul>	Repressible
S/370	PSW 13 and E	Interval Timer Damage	Repressible
S/370 370-XA	PSW 13 and E or T	Timing Facilities Damage <ul style="list-style-type: none"> <li>• Time-of-day clock error</li> <li>• Clock comparator error</li> <li>• CPU timer error</li> </ul>	Repressible
S/370	PSW 13 and E	External Damage <ul style="list-style-type: none"> <li>• Uncorrectable processor storage or protect key error during an I/O operation</li> <li>• Channel not operational condition</li> <li>• Channel control failure condition</li> </ul>	Repressible
S/370 370-XA	PSW 13 and E	Degradation <ul style="list-style-type: none"> <li>• Malfunctioning bit turned on in the high-speed buffer directory</li> </ul>	Repressible
370-XA	PSW 13 and C	Channel Report Pending <ul style="list-style-type: none"> <li>• One or more channel report words are available</li> </ul>	Repressible
370-XA	PSW 13	Channel Subsystem Damage <ul style="list-style-type: none"> <li>• Uncorrectable double-bit error in channel or subchannel data in auxiliary storage</li> </ul>	Repressible
S/370 370-XA	PSW 13	System Damage <ul style="list-style-type: none"> <li>• Severe damage for any unretryable privileged instruction</li> <li>• An uncorrectable processor storage error occurred in the auxiliary storage area except in the CPU timer or clock comparator area or for System/370-XA mode in channel or subchannel data in auxiliary storage</li> </ul>	Exigent

Figure 17 (Part 1 of 2). 4381 Processor machine check interruptions

Mode	Mask Bit(s)	Interruption Type and Cause	Machine Check Condition
S/370 370-XA	PSW 13	Instruction Processing Damage One of the following occurs during instruction execution: <ul style="list-style-type: none"> <li>• An unretryable malfunction for a nonprivileged instruction</li> <li>• A retryable malfunction, including a double- or multiple-bit processor storage error or access control key failure, not corrected by instruction retry</li> </ul>	Exigent

Figure 17 (Part 2 of 2). 4381 Processor machine check interruptions

### Exigent Machine Check Interruptions

Exigent machine check interruptions are the following:

- **Instruction Processing Damage.** This interruption can occur when PSW bit 13 is on. The PD bit in the stored machine check code (bit 1) is used to indicate that an error occurred during the execution of the instruction indicated by the machine check old PSW. This error is posted when a nonretryable malfunction occurs for a nonprivileged instruction or a retryable malfunction is not corrected after one retry is performed. If failure of a storage protection key or a double- or multiple-bit processor storage error caused the error, the failing address field will contain the address of the 2K or 4K storage block associated with the malfunctioning storage protection key or the failing address itself, respectively.
- **System Damage.** This interruption can occur when PSW bit 13 is on. The SD bit is stored in the machine check code. This interruption is caused by an uncorrectable storage error in auxiliary storage (other than in the CPU timer or clock comparator area, the interval timer area for System/370 mode, or channel/subchannel data for System/370-XA mode) or when severe damage occurs during the execution of an unretryable privileged instruction. Some errors that occur during nonprivileged instruction execution (certain clocking errors, for example), may also cause system damage.

### Modes of System Operation for Machine Check Interruptions

Using the check control display, the operator can set the 4381 Processor to operate in normal, hard stop, no retry, disable, or stop after log mode. The mode set determines the actions taken after a machine check error condition occurs. When normal mode is in effect, a logout to functional diskette 1 occurs, retry is done if applicable, and (when the processor is enabled for the specific machine check condition) a machine check interruption and logout to processor storage take place after a machine check condition occurs.

A check-stop state is defined for the 4381 Processor. If a check-stop condition occurs when a 4381 Processor is set to normal mode for machine checks, a logout to functional diskette 1 occurs, after which the 4381 Processor stops without the occurrence of a logout to the fixed area in processor storage (locations 0 to 511). Check-stop is initiated by hardware rather than by programming. Implementation of a check-stop state prevents system operations from continuing when the nature of the machine malfunction prevents the processor from presenting meaningful status data.

The check-stop function is controlled by a check-stop control bit as in System/370 processors. When a 4381 Processor enters the check-stop state, the start key and restart function are made inoperative. Processor operation can be resumed only after a system reset or IPL is performed.

The following conditions cause a check-stop for a 4381 Processor when it is in normal mode for machine check conditions:

- Certain clocking checks, such as a refresh clock check
- Second unretryable error occurs while the first is being processed

When hard-stop mode is in effect, after any type of machine check is detected, the 4381 Processor enters the machine check state immediately without any retry or reference code generation. There is no logout to functional diskette 1 and no machine check interruption and logout to appropriate fields in processor storage locations 0 to 511 before the stop. The suppressed log is kept until the 4381 Processor is started again, at which time the logouts to functional diskette 1 and processor storage occur.

When a 4381 Processor is set to operate in no-retry mode, logging to functional diskette 1 is done but the instruction retry function is inhibited and an instruction processing damage or system damage machine check is generated after the error is logged. When disable mode is in effect, the processor is prevented from entering the check-stop state and taking any machine check interruptions. When a machine check condition occurs with disable mode in effect, the processor attempts to continue operation without a logout to functional diskette 1 or a machine check interruption.

The stop after log mode is provided for use with System/360 operating systems. When this mode is in effect, retry occurs after an error but system operation stops after a logout to functional diskette 1 occurs to prevent erroneous continued operation because of instructions or data overlaid by the logout to processor storage.

The state of a 4381 Processor for machine check interruptions after IPL or an initial CPU reset is:

1. External damage interruptions and check-stops are enabled.
2. Recovery, interval timer, timing facilities, degradation, and channel status interruptions are disabled.
3. PSW bit 13 normally is set to one by the IPL PSW (it is set to zero by the IPL system reset procedure) to enable the processor for system damage, instruction processing damage, and channel subsystem damage interruptions.

## Machine Check Analysis and Logging

The 4381 Processor implements an error analysis function like that implemented in other 4300 Processors, and the analysis and writing of logout data is handled by the support processor so that a logout is obtained even when the instruction processing function cannot successfully perform a machine check and logout to processor storage.

When a hardware error is detected in the logic of a 4381 Processor, system clocks are stopped, the support processor receives control, and a logout of the status of the 4381 Processor occurs to the support processor. The logout is done via a scan-out operation, which is a serial-by-bit transfer of all the data in the scan ring logic. This logout data provides the complete status of the logic, which is significantly more information than is available for most System/370 processors. The use of LSI technology and the implementation of scan rings for the logic enable all status data to be accessed after an error is detected.

The support processor inspects the logout data and determines whether a check-stop condition exists. If not, the support processor determines whether the error is retryable and, if so, reinitializes the instruction processing function for an instruction retry. The initialization includes a scan-in operation, which is a serial-by-bit transfer of initialization data into the scan ring logic. The clocks of the instruction processing function are then started, and it performs a retry.

If a retry is not possible, the instruction processing function is initialized for a machine check interruption and a machine check interruption request is presented to the instruction processing function. If the processor is enabled for the machine check type, the interruption is taken and a logout of processor-independent information is placed in appropriate fields in program processor storage locations 0 to 511. The machine check handler routine then writes the 512-byte logout to the operating system logout data set/file (SYS1.LOGREC in OS/VS or SYSREC in DOS/VSE, for example) and takes appropriate recovery action.

While the instruction processing function is performing a retry or machine check interruption, the support processor writes the processor-dependent logout data to functional diskette 1. An error analysis routine is loaded into the support processor from functional diskette 1. The error analysis program inspects the data logged to the support processor and, if possible, generates an eight-digit reference code to identify the malfunction.

The error analysis program then writes the reference code to functional diskette 1 and, if the error is critical, displays it on line 23 of the display console. The audible alarm is sounded when a reference code is displayed. The reference code remains displayed until replaced by another reference code or a system reset is performed. When a reference code is displayed or a processor malfunction occurs, the operator should invoke Problem Analysis immediately to aid in diagnosing the problem. Then IBM Service should be called. See discussion of Problem Analysis in Section 60:15.

## Functional Diskette 1 Logouts

Four basic types of processor-dependent error logouts are written to the 4381 Processor functional diskette 1: support processor, instruction processing function, reference code history, and power. Power logouts are discussed under "Power System" in this subsection. The support processor logouts consist of one support processor summary record and up to eight support processor detail records. The summary record contains summary data about the existing detail records, which contain status data about the support processor and its adapters for the last nine support processor errors.

The instruction processing function logouts consist of one processing unit summary record, one processing unit directory record, and two status (checks-in-system and scan rings) log records for each logout (up to nine) listed in the directory record. For the 4381 Model Group 14 or 3, up to nine logouts are saved for each instruction processing function.

The processing unit directory record identifies the processor-dependent logout data currently recorded on functional diskette 1. Logout data for the last three correctable errors and the last uncorrectable error is maintained in the status log records. The processing unit directory record contains the following for each logout: the logout identification number of the log, the reference code, the date and time of the error, and the error type (recoverable or nonrecoverable).

The checks-in-system and scan-rings-log records for a given error contain detailed processor-dependent information about the status of the processor at the time of the failure and the logout identification number of the error.

The reference code history record contains the last 31 reference codes generated by the support processor and each is time stamped.

The IBM customer engineer can display the contents of each type of support processor and instruction processing function log record and the reference code history record on the display console using the general selection display when CE mode is in effect. The IBM customer engineer can also print the contents of log records on a natively attached 3287 or 3268 Printer (via the copy key) and purge log records using the console. If a 3287 or 3268 Printer is not installed, log records can be printed on a channel-attached printer by configuring the copy key for the channel-attached printer.

## Power System

### Components

The power system in 4381 Processors consists of the following functional units:

- Power supplies
- A single logic card that provides microprocessor-controlled sequencing for powering the support processor, its adapters, and the system diskette drives
- Power controller hardware that provides digital and analog sense points to permit power on/off control and power monitoring via microcode
- The power controller adapter diagnostic program, which is executed during the power-on procedure before the instruction processing function is powered up, as part of the hardware check-out procedure
- The power feature table that contains configuration-dependent power information for use by the microcode power sequencing and power monitoring programs
- Power sequencing, monitoring, logging, and shutdown programs
- A power-up/power-down program the customer engineer can use to individually power up/down the instruction processing function and the Channel-to-Channel Adapter. The support processor subsystem must be completely operational to execute this program.
- A CE service panel that enables the customer engineer to power the 4381 Processor on and off.

The power controller adapter is attached to the support bus of the support processor to provide two-way communication between the support processor and the power controller adapter. Via the power controller adapter, the support processor controls power on/off sequencing, monitors voltage and current conditions, and monitors thermal and airflow sensors in the 4381 Processor. The adapter contains circuitry that performs digital and analog sensing as well as digital to analog conversions. This circuitry provides voltage and temperature monitoring and measurement.

Although the functional power components in 4381 and 4341 Processors are the same, the actual power hardware in 4381 Processors is completely different from that in most 4341 Processors. There are fewer power parts in 4381 Processors and they are smaller than in 4341 Processors. This results in improved reliability, space savings, and better power fault location.

The power components in 4381 Processors require only one frame while two frames are required in a 4341 Processor. The high-current power supplies and MCM logic are all on one fixed gate in a 4381 Model Group 11, 12, 13, 1, or 2 Processor, eliminating the swinging gate for these functions that is implemented in a 4341 Processor.

To further improve reliability, all power connectors used in 4381 Processors are the positive retention type (fewer than half of those in a 4341 Processor have positive retention). To reduce field upgrade times, all the power supplies required for a 4381 Processor are part of the basic 4381 Processor. Significant functional improvements that will aid serviceability have also been made for 4381 Processors, as discussed below.

## Functional Operation

Once the support processor is powered on via microprocessor-controlled sequencing, the power-on sequence for the rest of the 4381 Processor system is microcode-controlled and handled by the support processor. The hardwired power sequencing in 4381 Processors is controlled by a single-card maintenance bias controller (MBC) instead of a controller implemented on one board with five cards, as in 4341 Processors. The MBC improves reliability, reduces cost, and aids serviceability by providing reference codes that are used to automatically isolate many of the faults that can occur during initial power-on sequencing of the support processor. In 4341 Processors, such fault isolation has to be done via manual probing.

In addition, the switching power regulators in 4381 Processors have internal sensors to detect the presence and level of the externally supplied bias voltages. If a bias voltage is out of specification or missing, a digital status line to the MBC is activated and the power microcode receives control to generate the appropriate reference code. This facility improves fault detection capability for the case in which intermittent errors are caused by cabling.

After the support processor power sequencing is completed, the power diagnostic program is executed as part of the power-on procedure to test the operation of the power controller adapter. If an error is found during these tests, the power-on procedure is terminated and a reference code that identifies the power failure is displayed on the operator console.

During the IML procedure, the power feature table is generated based on the 4381 Processor configuration specified on functional diskette 1. The table contains configuration-dependent power sensor and control data information in the form of strings and masks. This table is used by the power monitor program.

The power monitor program is resident in storage of the support processor during system operation. Once a power-on is successfully completed, the power monitor program is executed periodically.

The power monitor program reads all the analog and digital sense points to determine whether any power or thermal fault conditions exist. The sense data read is compared against the mask in the power feature table. If the comparison indicates no fault exists, execution of the power monitor program is terminated. If the comparison detects a fault, the power monitor program rereads all the sense points and repeats the comparison to suppress spurious faults. If the readings still show a fault, the power monitor program determines whether the readings indicate power or thermal conditions are critical enough to warrant a power-down of the processor. If so, a reference code is generated, a power logout record is written to functional diskette 1 that includes the reference code, the reference code is displayed on the operator console, and a power-down of the processor is initiated. Neither the operating system nor the operator is notified that a power-down is to

occur. When the readings indicate power or thermal conditions do not warrant a power-down, a reference code is displayed and processor operation continues.

The power interrupt handler program performs the same functions as the power monitor program except that it is invoked to read sense data as a result of a power adapter interruption. Such an interruption occurs when a digital sense point becomes active.

Functional diskette 1 contains detailed information about the four most recent power error logouts. These logouts contain power sensor and control latch status at the time of the power fault. The last 16 power reference codes generated are also recorded. The power logout records can be displayed using the operator console.

## **Maintenance Facilities**

While the power diagnostic facilities in 4381 Processors are like those provided for 4341 Processors, several improvements have been made for 4381 Processors to improve fault isolation and thereby reduce the time the processor is unavailable because of a power failure.

The power diagnostics used for 4381 Processors provide simplified displays for customer engineer use to improve their usability and can isolate a failure to a smaller field replaceable unit (FRU) group than those for 4341 Processors because of both power microcode and hardware changes in the 4381 Processor.

In addition, the Problem Analysis facility for 4381 Processors supports analysis of power failures, which is not done for 4341 Processors. Problem Analysis can be used by the operator to perform some preliminary power retry functions and to execute power diagnostics to attempt power fault isolation before the customer engineer is called. Problem Analysis provides a reference code and a list of the most probable failing FRUs. If this information is conveyed to IBM when a repair call is made, the customer engineer can bring replacements for the suspected failing FRUs.

Significant improvements in the power maintenance documentation provided for customer engineer use have also been made. The Maintenance Analysis Procedure (MAP) documentation provided for 4341 Processors has been replaced with Repair Action Procedure (RAP) documentation. RAP documentation provides step-by-step isolation procedures with all required information for a procedure in one place to eliminate the cross references among several documents that is required by MAP. For the small percentage of cases for which RAP does not provide power fault isolation, detailed power schematics (instead of automated logic diagrams, which do not resemble power schematics) are provided to support manual fault isolation.

In summary, the power system implemented in 4381 Processors, like that in 4341 Processors, offers serviceability and availability advantages. Microcode-controlled power sequencing, versus hardwired control, is a more flexible method of control. It enables engineering changes to be installed more rapidly and sense point data to be obtained more quickly. The customer engineer can display the status of sense points on the console and need not manually obtain these readings by scoping. The power monitoring facility can provide early warning of potential power failures and may prevent catastrophic power failures.

In addition, reliability and serviceability improvements made to the power system implementation for 4381 Processors are designed to increase system availability.

## 60:15 Diagnostic and Remote Support Facilities

There are several diagnostic programs and procedures that can be used to isolate an error to a field-replaceable unit. A subset of these diagnostic programs is available to the customer using Problem Analysis to verify the hardware of the 4381 Processor. The customer engineer, with the support of the field support center, can utilize other diagnostic programs and procedures to help resolve non-reference code errors more effectively. A basic system checkout test is also provided, as for other 4300 and System/370 processors.

For 4381 Processors, the following diagnostic programs are provided:

- Problem Analysis. These routines are on functional diskettes 1 and 2.
- Support processor subsystem diagnostics (basic, extended, and optional tests). The basic tests are in read-only control storage of the support processor and on functional diskette 1. The extended and optional tests are contained on the diagnostic diskette.
- Power controller adapter diagnostics. These are on functional diskette 1.
- Instruction processing function diagnostics (basic diagnostics and machine speed microdiagnostics). These are on functional diskette 2 and the diagnostic diskette.
- System Test. The System Test is provided on tape.

### Problem Analysis

Problem Analysis is an automated routine that should be run when a processor problem is suspected. It may also be of assistance when a system failure or operating problem is suspected. The Problem Analysis function is included in the basic microcode contained on functional diskettes 1 and 2.

Problem Analysis is designed to resolve problems quickly so that normal job processing can be resumed. It collects and analyzes data related to a problem and guides operator actions through highlighted messages on the display. By using Problem Analysis, the operator can resolve some problems or, if assistance is needed, provide pertinent information to IBM service personnel before they arrive. In many instances this allows service personnel to bring the correct part for repair. Problem Analysis also allows some service calls to be deferred. By logging information about a problem on functional diskette 1, Problem Analysis allows the operator to restart the system, transfer the saved data to a remote specialist via the Remote Support Facility, and defer the call until a more convenient time.

Problem Analysis consists of a set of microcode routines that can be executed by the operator on a 4381 Processor. Six Problem Analysis options are provided. Each is invoked from the Problem Analysis display, which is requested using the

General Selection display. A Problem Analysis guide is provided to explain step-by-step use of Problem Analysis procedures. A subset of Problem Analysis routines can be executed on a remote 4381 Processor using the Remote Operator Console Facility.

The intent of Problem Analysis is to:

- Provide automated processor problem determination procedures
- Capture the state of the processor at the time of the error
- Identify recovery procedures
- Verify processor hardware integrity
- Identify the parts required
- Collect and transmit error data needed for remote analysis
- Improve customer availability

To obtain the maximum benefit from Problem Analysis and the remote maintenance approach, the Remote Support Facility must be specified and functional.

Problem Analysis Option 1 is the normal starting point for Problem Analysis. This option collects status information about the processor and records it on functional diskette 1. The processor error logs are then analyzed to determine if any failures have occurred in the previous 24 hours. If an operator correctable problem is detected, a screen is displayed that explains the problem, lists the probable causes, and gives steps to correct the problem. If a hardware problem is detected, a screen is displayed that directs the operator to run the Processing Unit Analysis (option 3). If no trouble is detected, a NO TROUBLE FOUND message is displayed.

Option 2 allows the redisplay of all of the messages (screens) that were displayed by Options 1 and 3 for the last six times Problem Analysis was run. This allows a system programmer or service representative to see exactly what Problem Analysis displayed to the operator.

Option 3 selects Processing Unit Analysis. This consists of the execution of processing unit diagnostics that reside on functional diskette 2. Since an IML and IPL are required after running these tests, all processing should be terminated prior to selecting this option. If a solid failure is detected, an error code is displayed. The error code allows the customer engineer to bring the probable repair parts. If an intermittent failure is detected, the operator is instructed to restart processor operations and to call for service at his convenience. If no failures are detected, the operator is instructed to restart processor operations.

Option 4 of Problem Analysis is used to send service information gathered by Problem Analysis Options 1 and 3 to a remote specialist for further analysis. This information is sent via the Remote Support Facility. Execution of this option is requested by the remote specialist, if necessary, and can operate concurrently with normal processor operation after it is initiated (the operator console cannot be used for operator-to-operating system communication during the initialization time). Option 4 can be used, for example, to aid in fault diagnosis for intermittent errors.

Option 5 displays the detailed system information that was gathered when Option 1 was run. This information may be useful to system programmers or the customer engineer to analyze nonhardware failures.

Option 6 displays a screen that contains information that is used by Option 4 to send service data. Option 6 also allows the customer to create a password that must be used before processor storage data can be sent to IBM. This allows the customer to protect programs and sensitive data.

Problem Analysis for 4381 Processors has been improved relative to the Problem Analysis provided for 4341 Processors as follows:

- The diagnostics executed by Problem Analysis are online on functional diskette 2 so that diskette changing is not required to execute them.
- More fault isolation capability has been added.
- Support processor subsystem and power logouts are analyzed.
- Processor error logs for the previous 24 hours are analyzed.
- Six national languages are supported for messages (Spanish, French, Italian, German, Brazilian, and Japanese). Functional diskette 2 contains English messages and one additional set of messages can be copied from the diagnostic diskette to functional diskette 2.

Problem Analysis operating instructions are contained in *4381 Problem Analysis Guide* (GA24-3955).

## **Support Processor Subsystem Diagnostics**

Basic diagnostics for support processor subsystem components are contained on functional diskette 1 and in read-only control storage in the support processor. When the support processor is powered on or re-IMLed (power-on/IML pushbutton is pressed), these diagnostics are executed to test for the correct operation of the support processor, diskette drives and adapters, console attachment adapters, and the operator console. These tests execute regardless of the diskette mounted or the setting of the CE mode switch. If an error is found, a reference code is generated and displayed on the operator console or an error indication is displayed on the CE panel.

The extended and optional diagnostics for the support processor subsystem provide more extensive testing of the components of the support processor subsystem than the basic tests. Reference codes are displayed on the display console to indicate errors.

## **Power Controller Adapter Diagnostics**

Functional diskette 1 contains a complete set of power controller adapter tests. Whenever the support processor is powered on, these tests are automatically executed after successful execution of the support processor subsystem diagnostics that are resident in the support processor. When CE mode is in effect, execution of these tests can be invoked using the console, and error information is displayed on the console.

## **Instruction Processing Function Diagnostics**

The basic diagnostics and machine speed microdiagnostics for the instruction processing function operate in conjunction with the Test Case Monitor and machine speed microdiagnostics monitor programs. These monitor programs control the loading and execution of the diagnostic programs and, utilizing the operator console, provide communication between the customer engineer and the diagnostics. The Test Case Monitor program is loaded when the IBM TESTS function on the CE mode General Selection display is selected or when the DIAG key is activated.

### **Basic Diagnostics**

The basic diagnostics execute in the support processor under control of the Test Case Monitor program, which is contained on functional diskette 2 and the diagnostic diskette. The basic diagnostics (which are contained on functional diskette 2) test the error checking hardware and other hardware in the processor that is required to execute the machine speed microdiagnostics. Additional basic diagnostics reside on diagnostic diskette 1 to test hardware not required for, or tested by, the machine speed microdiagnostics.

Error checking hardware, maintenance chips, scan rings, control storage, and clock distribution are tested via the support bus adapter interface to the instruction processing function. Errors are indicated via the displaying of reference codes on the display console.

### **Machine Speed Microdiagnostics**

The machine speed microdiagnostics execute in instruction processing function control storage under the control of the machine speed microdiagnostics monitor program. The microdiagnostics and monitor are contained on functional diskette 2 and are loaded under control of the Test Case Monitor.

The machine speed microdiagnostics exercise the instruction processing function at processor speed to test the interaction between control storage, the instruction processing function, the storage controller, and channel hardware. Errors are indicated via the displaying of reference codes on the display console.

## **Error Logout Analysis Program**

The error logout analysis program is automatically invoked after each machine check occurs to analyze processor logout data contained on functional diskette 1 and to provide fault isolation.

## **System Test**

The System Test performs a functional test of the system hardware components, including the support processor, storage, channels, and most locally channel-attached I/O devices. Two versions of the System Test are available for 4381 Processors. System Test/4381 supports 4381 Processors operating only in System/370 mode. It is supplied on tape and can be loaded to direct access storage for use in a 4381 installation.

System Test/4381XA is a copyrighted, proprietary IBM program that supports 4381 Processors operating in System/370 or System/370-XA mode. It is supplied on tape and its use is controlled by IBM. The System Test/4381XA is not to be loaded to customer direct access storage and will be executed only from tape.

The System Test can be used for the following purposes:

1. To determine that the hardware configuration operates correctly after initial installation and before any IPL is performed
2. To locate a malfunctioning unit in the system. (The specific error component within the unit is not identified.)
3. To verify correct system operation after a malfunctioning unit has been repaired
4. To verify correct 4381 operation after engineering change installation, MES installation, or configuration changes have been made

## **Remote Support Facility**

The Remote Support Facility (RSF) feature is a highly recommended, no-charge specify feature that is designed to offer an advanced level of problem determination and enhanced serviceability.

The Remote Support Facility provides the capability of establishing a teleprocessing link between the 4381 support processor and RETAIN or a 3275 display. This function is controlled by microcode within the support processor and is used to enhance the maintenance of 4381 Processors.

Four modes of operation are available:

- Problem Analysis mode, which permits the customer to transmit processor log data to the RETAIN system, as discussed previously in this subsection.
- Data Bank mode, which permits an IBM customer engineer to access the RETAIN data base facilities from the customer site.

- Remote Console mode, which permits remote control of the 4381 Processor from any RETAIN terminal or from a 3275 display.
- Remote Operator Console Facility (ROCF) mode, which permits the customer to operate the system console from a remote location (as described in Section 40:15).

*Data Bank Mode.* When the local customer engineer cannot locate the cause of a problem utilizing the generated reference code and MAPS documentation or when a reference code is not generated, the customer engineer can invoke RSF to access the data bank. When Data Bank mode of RSF is activated, the 3278 Model 2A, 3279 Model 2C, or 3205 console of the 4381 Processor appears to be a terminal with a processor-to-processor interface to a special data bank system dial port.

The 4381 Processor must be in hard-stop mode before Data Bank mode can be invoked and only one console and one hard-copy printer can be active during Data Bank mode operations. When Data Bank mode is terminated, the state of the 4381 Processor is unpredictable. Thus, a re-IML or re-IPL will be necessary, depending on the state in effect.

*Remote Console Mode.* When the Field Support Center (FSC) is contacted by a local customer engineer, the FSC may instruct the local customer engineer to invoke the Remote Console mode of RSF to enable a remote customer engineer specialist to control operation of the malfunctioning 4381 Processor for diagnostic purposes.

To activate Remote Console mode, the local customer engineer must (1) select the Remote Console Initialization display from the Configuration display, (2) select the remote console entry, (3) enter identifying information about the 4381 Processor (for example, branch office and customer number), and (4) dial the data bank system to establish a communication link. This causes the data bank system to perform a security check on the specified 4381 Processor and the link is disconnected if the 4381 Processor is not registered.

*Advantages.* The basic design of the Remote Support Facility includes customer security features. First, operation of RSF can be requested only from the customer installation and a security check is performed before the facility is initiated. Second, via the local operator console, the customer can monitor all operations performed while RSF is active and the facility can be deactivated immediately at any time by depression of the LINE DISC key on the local operator console. (RSF can also be deactivated by the remote specialist via the data bank or 3275 terminal.)

## Section 70: Programming Systems Support

Model Groups 11, 12, 13, 1, and 2 of the 4381 Processor support operating systems that use a 2K or 4K page size. For configurations with up to 16Mb of processor storage, operating systems that use a 2K or 4K storage protect key are supported. For a 4381 Model Group 12, 13, or 2 with more than 16Mb, an operating system that supports 4K protect keys is required.

The 4381 Processor Model Group 14 or 3 supports operating systems that use a 4K page size only. Thus, if a Model Group 14 or 3 is initialized as a uniprocessor, DOS/VSE can be run only if VSE/Advanced Functions Release 2.1.1 is used, since the latter supports 4K keys, and OS/VS1 cannot be run.

### 70:05 DOS/VSE

DOS/VSE with VSE/Advanced Functions (VSE/AF) as of Release 1.3.5 and VSE/SP as of Release 1.3.5 supports 4381 Model Group 11, 12, 13, 1, and 2 Processors operating in System/370 mode with up to 8Mb of processor storage. DOS/VSE with VSE/AF Release 1.3.5 and VSE/SP 1.3.5 can execute in a uniprocessor 4381 Processor with 16Mb of processor storage but can use a maximum of only 8Mb. When the VM Linkage Enhancements of VSE/AF is specified, a DOS/VSE system executing in a virtual machine can use up to 16Mb of processor storage. When VSE/AF Release 2.1.0 is used with DOS/VSE, up to 16Mb of processor storage is supported. VSE/AF Release 1.3.5 or 2.1.0 supports only 2K pages, while VSE/AF Release 2.1.1 supports 4K pages.

VSE/AF as of Release 1.3.5 provides support of fixed block architecture (FBA) devices (3370 for 4381 Processors) for System/370 mode supervisors (rather than for ECPS:VSE mode supervisors only). It also uses the SIOF instruction and supports SIOF queuing by processing deferred condition 1 interruptions. In addition, this release permits up to 16Mb of virtual storage (less supervisor and any real partition requirements) to be used regardless of the size of real storage and supports additional I/O devices.

Two DOS/VSE to MVS migration aids (program offerings) are available. The UCC Two (DOS/VSE to MVS Migration Aid) adapts DOS/VSE executable code (DOS/VSE Core Image Library modules) to operate under MVS. The adapted DOS/VSE modules reside in an MVS load module library and operate under MVS using MVS job control statements and MVS data sets (DOS/VSE files must be converted to MVS data sets). The VSE JCL Conversion Aid can be used to convert DOS/VSE job control statements to MVS job control statements.

## 70:10 OS/VS1

OS/VS1 Release 7 with OS/VS1 Basic Programming Extensions Release 4 supports 4381 Model Group 11, 12, 13, 1, and 2 Processors operating in System/370 mode. Basic Programming Extensions Release 3 with the proper PTF applied supports 4381 Model Group 2 Processors only operating in System/370 mode. OS/VS1 will operate in a 4381 Processor with 16Mb installed but only supports up to 8Mb of processor storage. However, an OS/VS1 supervisor with the VM Handshaking feature specified can use up to 16Mb when operating in a virtual machine in a 4381 Processor. One virtual storage of up to 16Mb is supported.

## 70:15 MVS/370

All 4381 model groups operating in System/370 mode are supported by MVS Release 3.8 with MVS/SP-JES2 Version 1 Release 3.3 or 3.5 or MVS/SP-JES3 Version 1 Release 3.3 or 3.5 installed. The appropriate PTF must be installed in the MVS/SP product used. Version 1 of MVS/SP supports only System/370 architecture and is referred to as MVS/370. Up to 16Mb of processor storage and multiple 16Mb virtual storages are supported. Dual processor mode is supported for 4381 Model Groups 14 and 3.

MVS/SP Version 1 Release 3 utilizes ECPS:MVS (including the page fault assist function and ADD FRR instruction) and will also use the Dual Address Space Facility hardware to support Cross Memory Services to improve performance. It also supports segment protection for that portion of the MVS pageable link pack area that is contained in full 64K segments and utilizes the TEST BLOCK instruction. MVS/SP Version 1 as of Release 3.1 and the Data Facility/Device Support program product support the 3880 Model 11 paging and swapping subsystem. The 3880 Model 13 for application data is supported by MVS/SP Version 1 as of Release 3.

## 70:20 VM/370

Support of 4381 Model Group 11, 12, and 13 Processors operating in System/370 mode is provided by VM/370 Release 6 with VM/System Product (VM/SP) Release 3 or later. VM/370 Release 6 with VM/SP Release 2 or later supports 4381 Model Groups 1 and 2. VM/System Product High Performance Option Release 3.2 or later for Model Groups 11, 12, and 13 or Release 3 or later for Model Groups 1 and 2 is optional. VM/SP Release 3 or later with or without the VM/SP High Performance Option is required to support dual processor configurations (Release 3.4 or later for the 4381 Model Group 14 and Release 3.2 or later for the 4381 Model Group 3). Up to 16Mb of processor storage and multiple virtual machines with up to 16Mb of virtual storage each are supported.

The VM/SP High Performance Option is required to support the use of Dual Address Space Facility hardware for the Cross Memory Services facility of MVS/SP in a virtual machine or to support more than 16Mb of processor storage.

VM/SP High Performance Release 3.4 or later is recommended for the 4381 Model Group 3 to support the VM assists. Installation of the VM/SP High Performance Option program product may be required to support certain of the I/O devices contained in a 4381 configuration or certain hardware features.

Preferred Machine Assist is utilized to improve the performance of MVS/370 running in a virtual machine.

## 70:25 MVS/XA

All 4381 model groups operating in System/370-XA mode are supported by MVS/Extended Architecture (MVS/XA). MVS/XA consists of the MVS/SP-JES2 Version 2 or MVS/SP-JES3 Version 2 program product and the MVS/XA Data Facility Product program product, which require MVS Release 3.8 as a base. MVS/SP Releases 1.2 and 1.3 with the appropriate PTF support 4381 Model Groups 11, 12, 13, and 14. MVS/SP Version 2 Release 1.1 or later with the appropriate PTFs applied is required for a 4381 Processor Model Group 1, 2, or 3.

MVS/XA is designed to utilize the new facilities defined in System/370 extended architecture and provides the following major facilities:

- Support of real and virtual storage of up to two gigabytes using 31-bit addressing. In addition, certain MVS code and control blocks have been moved from the first 16Mb area of virtual storage to virtual storage above 16Mb (which is called the extended virtual storage area). This change makes more virtual storage below 16Mb available to user programs and to MVS system functions that can operate only in that virtual storage addressable by 24 bits.
- Bimodal operation. Programs that utilize 24-bit addressing and programs that utilize 31-bit addressing can operate concurrently when System/370-XA mode is in effect. This capability enables existing MVS/370 programs to be used together with new programs that are designed to utilize 31-bit addressing.
- Support of the dynamic channel subsystem. Up to 4096 I/O devices (versus up to 1917 for MVS/370), up to 256 channel paths (versus a maximum of 16 for a processor in MVS/370), and up to eight channel paths per I/O device are supported. Channel path selection and I/O queuing support are removed from MVS/XA and MVS I/O control block definitions (unit control blocks) can be located anywhere within the first 16Mb of real storage.
- Support of the sort assist facility by the Data Facility Sort (DFSORT) as of Release 7 operating under MVS/XA
- New system trace facilities that use the tracing capabilities defined in System/370 extended architecture. These trace facilities are compatible and can operate concurrently with the Generalized Trace Facility (GTF).
- Page protection to prevent any writing in certain system areas, such as the pageable link pack area

The MVS/SP Version 2 JES2 and JES3 program products differ from their counterpart MVS/SP Version 1 program products in that the former have been modified as required to support System/370 extended architecture facilities, and new availability, serviceability, and usability facilities have been added. Otherwise, MVS/SP Version 2 offers the same facilities as the BCP and JES (JES2 or JES3) components of MVS/SP Version 1 Release 3. MVS/SP Version 2 will operate only in processors with System/370 extended architecture implemented (4381, 308X, and 3090 processors).

The MVS/XA Data Facility Product program product provides data management, device support, program library management, and utility functions. It supports System/370 extended architecture facilities and includes the functions provided by the following for MVS/SP Version 1:

- Data Facility Device Support
- Sequential Access Method-Extended
- Data Facility/Extended Function
- Offline IBM 3800 Utility
- Access Method Services Cryptographic Option
- 3800 Enhancements and prerequisite program service

MVS/XA is designed to be compatible with MVS/370 as far as is possible. User-written MVS System/370 mode programs that use published external interfaces will operate under MVS/XA without modification, with minor exceptions. In general, IBM-supplied MVS programs, products, and subsystems will operate with MVS/370 or MVS/XA. MVS/370 and MVS/XA job control and user data set formats are compatible and most MVS/370 operator messages and commands are utilized as is in MVS/XA.

Assembler H Version 2 is provided to support System/370 extended architecture (new operation codes, new channel command word format, specification of the addressing to be used, etc.).

## **70:30 VM/Extended Architecture Migration Aid**

The VM/Extended Architecture (VM/XA) Migration Aid is designed to execute in all 4381 model groups operating in System/370-XA mode. Release 2 or later supports 4381 Model Groups 11, 12, 13, and 14. Release 1 or later supports 4381 Model Groups 1, 2, and 3. This program product is designed for a DOS/VSE, VS1, or MVS/370 user who wishes to migrate to MVS/XA and to execute production work and MVS/XA testing using one 4381 system. The VM/XA Migration Aid supports only a subset of the functions provided by the System/370 mode VM/370 programming system and its program products, but is extended to support specific facilities for a combined MVS/370 production and MVS/XA testing environment.

The CMS capabilities included in the VM/XA Migration Aid are provided only to support installation, service, and conversion facilities for the migration aid. Full CMS support can be obtained by executing VM/SP or VM/SP High Performance Option as a V=R (or V=V) virtual machine.

The VM/XA Migration Aid supports the operation of one production V=R preferred virtual machine in which DOS/VSE Release 3, OS/VS1 with BPE Release 3, or MVS/SP Version 1 Release 1.1 (or later releases) is operating and one or more V=V test virtual machines in which MVS/XA and the preceding operating systems are operating. In a 4381 uniprocessor configuration, the VM/XA Migration Aid cannot allocate one instruction processor to the production MVS/SP virtual machine and one instruction processor to the test MVS/XA virtual machine(s) as is done in a 3081 processor, which has two instruction processors. Therefore, running MVS/SP Version 1 production under the VM/XA Migration Aid in a 4381 uniprocessor or configuration should be assessed carefully.

As of Release 2 of VM/XA Migration Aid, virtual machine support of operating systems is as follows. DOS/VSE, OS/VS1, MVS/SP Version 1, MVS/XA, VM/SP, or VM/SP High Performance Option (each operating in uniprocessor mode) can execute in a V=R preferred virtual machine. DOS/VSE, OS/VS1, MVS/SP Version 1, MVS/XA, VM/SP, VM/SP High Performance Option, VM/XA Migration Aid, or VM/XA Migration Aid CMS (each operating in uniprocessor mode) can execute in a V=V virtual machine. MVS/XA or VM/XA Migration Aid operating in virtual MP mode can execute in a V=V virtual machine.

Facilities are also included to improve the performance of the production MVS/SP Version 1 virtual machine, such as improved handling of its I/O using the dynamic channel subsystem of System/370 extended architecture and automatic recovery of the production virtual machine whenever possible after an abnormal termination and automatic restart of the VM/XA Migration Aid occurs. The execution of all virtual machines is initiated using the MVS/XA instruction START INTERPRETIVE EXECUTION, and 31-bit addressing is supported for MVS/XA virtual machines.

## **70:35 Virtual Machine/System Product-Entry**

Virtual Machine/System Product Entry (VM/SP-Entry) supports 4381 uniprocessor model groups operating in System/370 mode with a minimum of 4Mb of processor storage. VM/SP-Entry is a preconfigured system that provides interactive, easy-to-install, load-and-go VM/SP entry-level support. It supports CMS virtual machines and server virtual machines (such as RSCS and SQL/DS). No other operating systems executing in a virtual machine are supported. A maximum of 128 virtual machines (CMS only or CMS and server) can be active at a time.

## 70:40 Virtual Machine/Extended Architecture Systems Facility

Virtual Machine/Extended Architecture (VM/XA) Systems Facility supports all 4381 model groups operating in System/370-XA mode. It supports all the facilities of the VM/XA Migration Aid and offers additional function. It also utilizes the START INTERPRETIVE EXECUTION (SIE) instruction to significantly improve performance and is designed to exploit the capabilities of 4381 Model Group 14 and 3 dual processors and dyadic processors (3081 and 3090 Model 200 configurations, or a 3084 or 3090 Model 400 configuration operating in partitioned mode).

VM/XA Systems Facility supports the concurrent operation of one production virtual machine for the current operating system (VSE, VS1, or MVS/370), normally as a V=R preferred guest, and one or more test MVS/XA virtual machines. Full CMS support can be obtained by executing VM/SP or VM/SP High Performance Option as a V=V or V=R virtual machine.

For a 4381 Processor Model Group 14 or 3, an operating system that supports a dual processor configuration, such as MVS/XA or VM/SP High Performance Option, executing in a V=R virtual machine will operate in both instruction execution functions simultaneously in dual processor mode and can utilize all of the available system resources. V=V virtual machines may execute using both instruction execution functions when no dedicated V=R virtual machine is logged on.

## 70:45 Programming Systems Support Table

4381 Function	DOS/VSE with VSE/AF Release 1.3.5 or later/ VSE/SP Release 1.1 or later	VS1 with BPE Release 4	MVS/370 (with MVS/SP Version 1 Release 3 or later)	MVS/XA (with MVS/SP Version 2 Release 1.1 or later)	VM/370 with VM/SP Release 2 or later
A. Mode of operation	System/370 and EC	System/370 and EC	System/370 and EC	System/370-XA	System/370 and EC
B. Processor storage supported (maximum)	8Mb. Up to 16Mb supported in a DOS/VSE virtual machine with VM Linkage Enhancements. For VSE/AF 2.1.0 or later, up to 16Mb is supported for System/370 mode.	8Mb. Up to 16Mb in a VS1 virtual machine with VM Handshaking	32Mb	32Mb	32Mb VM/SP High Performance Option Release 3 or later is required for more than 16Mb.
C. Virtual storage supported	One up to 16Mb for VSE/AF 1.3.5. For VSE/AF 2.1.0, up to three virtual address spaces are supported. Each can be up to 16Mb with a maximum of 40Mb for the three.	One up to 16Mb	Multiple. Each is 16Mb.	Multiple. Each is 2 gigabytes.	Multiple. Each is up to 16Mb.
D. Features					
– Common segment	No	No	Yes	Yes	No
– CPU timer, clock comparator	Yes	Yes	Yes	Yes	Yes
– Diagnose MSSFCALL	No	No	Yes	Yes	No
– Dual Address Space Facility	No	No	Yes (Cross Memory Services in MVS/SP)	Yes (Cross Memory Services in MVS/SP)	Use by an MVS/370 virtual machine supported when Preferred Machine Assist and VM/SP High Performance Option are used.
– Dynamic Address translation	2K page 64K segment 24-bit addressing for VSE/AF 1.3.5 or 2.1.0. For VSE/AF 2.1.1, 4K pages are also supported for System/370 mode.	2K page 64K segment 24-bit addressing	4K page 64K segment 24-bit addressing	4K page 1024K segment 31-bit addressing	4K page 64K segment 24-bit addressing

4381 Function	DOS/VSE with VSE/AF Release 1.3.5 or later/ VSE/SP Release 1.1 or later	VS1 with BPE Release 4	MVS/370 (with MVS/SP Version 1 Release 3 or later)	MVS/XA (with MVS/SP Version 2 Release 1.1 or later)	VM/370 with VM/SP Release 2 or later
- ECPS:MVS	-	-	Yes-all functions	A portion is utilized.	Supported in a virtual machine.
- ECPS:VM/370	-	-	-	-	Yes
- Elementary Math Library Facility	Assembler mnemonics	Assembler mnemonics	Assembler mnemonics (PRPQ available for FORTRAN Library support.)	Assembler mnemonics (PRPQ available for FORTRAN Library support.)	Can be issued in a virtual machine. (PRPQ available for FORTRAN Library support.)
- Fetch protection	No	Yes 2K key	Yes 4K key	Yes 4K key	Yes 2K or 4K key for virtual machine
- INVALIDATE PAGE TABLE ENTRY instruction	No	No	Yes	Yes	Yes
- MOVE INVERSE instruction	Yes	Yes	Yes	Yes	Yes
- Multiply and Add Facility	Assembler mnemonic	Assembler mnemonic	Assembler mnemonic	Assembler mnemonic	Can be issued in a virtual machine.
- Page protection	NA	NA	NA	Yes	NA
- Preferred Machine Assist	NA	NA	NA	NA	VM/SP High Performance Option Release 2 or later required.
- Segment protection	No	No	Yes	NA	VM/SP High Performance Option (any release)
- SIOF queuing	Yes	No	Yes	Yes	Yes
- Store protection	Yes 2K block	Yes 2K block	Yes 4K block	Yes 4K block	Yes - 2K or 4K block for a virtual machine
- Square Root Facility	Assembler mnemonic	Assembler mnemonic	(PRPQ available for FORTRAN Library support.)	(PRPQ available for FORTRAN Library support.)	(PRPQ available for FORTRAN Library support.)
- TEST BLOCK instruction	No	No	Yes	Yes	Used by VM/SP and can be issued in a virtual machine.
- TEST PROTECTION instruction	No	No	Yes	Yes	Can be issued in a virtual machine.
- Time-of-day clock	Yes	Yes	Yes	Yes	Yes

## **Section 80: Comparison Table of Hardware - 4341 Model Group 12 and 4381 Processors**

This table (80:05) compares the hardware features of the 4341 Model Group 12 Processor and 4381 Processor Model Groups 11, 12, 13, and 14 and indicates the operating systems that support each.

## 80:05 Hardware Features of the 4341 Model Group 12 Processor and 4381 Model Group 11, 12, 13, and 14 Processors

Hardware Features	4341 Model Group 12	4381 Model Groups 11, 12, 13, and 14
<b>I. PROCESSOR</b>		
A. Number of instruction execution functions	One	One for Model Groups 11, 12, and 13 Two for the Model Group 14
B. Modes of operation	1. System/370-BC and EC modes 2. ECPS:VSE-BC and EC modes	1. System/370-BC and EC modes 2. System/370 extended architecture-EC mode
C. Processor cycle time	Variable from 115 to 230 nanoseconds-8-byte data flow	68 nanoseconds-Models 11 and 12 56 nanoseconds-Models 13 and 14 8-byte data flow
D. Instruction fetching overlapped with instruction execution	Yes	Yes
<b>E. Features</b>		
- Byte-oriented operands	Standard	Standard
- Channel indirect data addressing	Standard	Standard
- Clock comparator	Standard (one-microsecond resolution)	Standard (one-microsecond resolution)
- Conditional swapping	Standard	Standard
- CPU timer	Standard (one-microsecond resolution)	Standard (one-microsecond resolution)
- Decimal arithmetic	Standard	Standard
- Diagnose MSSFCALL	Not implemented	Standard (one-microsecond resolution)
- Dual address space facility	Standard	Standard
- Dynamic address translation	Standard	Standard
	- 2K or 4K pages, 64K or 1024K segments, and 24-bit addressing (16Mb virtual storage) for System/370 mode	- Same as 4341 for System/370 mode - 4K pages, 1024 segments, and 31-bit addressing (2 gigabyte virtual storage) for System/370-XA mode
	- 2K pages and 24-bit addressing (16Mb virtual storage) for ECPS:VSE mode	- Processor TLB standard (32 rows) including common segment and page protection bits.
	- Processor TLB standard (32 rows)	

**Hardware Features****4341 Model Group 12****4381 Model Groups 11, 12, 13, and 14**

– ECPS:MVS	Standard—Includes: – 13 MVS assist instructions – INVALIDATE PAGE TABLE ENTRY instruction – TEST PROTECTION instruction – Dual address space facility	Standard—Includes: – 13 MVS assist instructions – Page fault assist – Virtual Machine Extended Facility Assist (Other functions included in ECPS:MVS for the 4341 are standard in the 4381.)
– ECPS:VS1	Standard	Not implemented
– ECPS:VM/370	Standard—Includes: – Virtual machine assist – Control program assist – Expanded virtual machine assist – Virtual interval timer assist When ECPS:MVS and ECPS:VM/370 are enabled together, ECPS:VM/370 includes: – Shadow table bypass assist – Page fault assist	Standard—Includes: – Virtual machine assist – Control program assist – Expanded virtual machine assist – Virtual interval timer assist – Shadow table bypass assist ECPS:MVS AND ECPS:VM/370 can operate together.
– Expanded machine check	Occurs after corrected and uncorrected errors. There are four types and the fixed area is 512 bytes.	Occurs after corrected and uncorrected errors. There are seven types and the fixed area is 512 bytes.
– External signals	Standard	Standard
– Floating-point arithmetic (including extended precision)	Standard	Standard
– Instruction retry by hardware	Standard (one retry). No reconfiguration functions in hardware.	Standard (one retry). Automatic hardware reconfiguration for an uncorrectable error in: – Control storage – High-speed buffer storage – A channel data buffer – The swap buffer
– Low address protection	Not implemented	Standard
– Mathematical Functions Facility	Not implemented	Standard (except Model Group 11)
– Multiply and Add Facility	Standard (Engineering Scientific Assist feature)	Standard
– Monitoring	Standard	Standard
– Page protection	Not implemented	Standard (System/370-XA mode)
– Preferred Machine Assist	Not implemented	Standard
– Problem Analysis	Standard	Standard (with additional functions)
– Program event recording	Standard	Standard
– Reference and change recording	Standard	Standard
– Reloadable control storage	Standard	Standard
– Segment protection	Not implemented	Standard (System/370 mode)
– Square Root Facility	Not implemented	Standard
– SSM suppression	Standard	Standard

**Hardware Features****4341 Model Group 12****4381 Model Groups 11, 12, 13, and 14**

- SIOF instruction (System/370 mode)	Fast release implemented. Queuing not implemented.	Fast release and queuing implemented.
- Storage key extensions (SSKE, ISKE, RRBE)	Not implemented	Standard
- Store and fetch protection (2K keys)	Standard	Standard
- Store status	Standard	Standard
- Suspend and resume	Not implemented	Not implemented
- TEST BLOCK instruction	Not implemented	Standard
- Time-of-day clock (one-microsecond resolution)	Standard	Standard
- UCWs/subchannels	128 to 1024 UCWs standard for both modes	128 to 2048 UCWs standard for System/370 mode 128 to 2048 subchannels standard for System/370-XA mode
- VM Extended Facility Assist	Not implemented	Standard

**F. Instruction set**

System/370 mode includes all System/370 architecture instructions except:

- READ DIRECT, WRITE DIRECT
- Channel set switching
- Multiprocessing
- RESUME I/O
- BRANCH AND SAVE
- TEST BLOCK
- SET STORAGE KEY EXTENDED
- RESET REFERENCE BIT EXTENDED
- INSERT STORAGE KEY EXTENDED

System/370 mode includes all System/370 architecture instructions except:

- READ DIRECT, WRITE DIRECT
- Channel set switching
- Multiprocessing
- RESUME I/O

**G. Logic technology**

- Chip	- 704 circuit chip	- 704 circuit chip (faster switching speeds)
- Packaging	- Ceramic module on card on board (up to 9 chips per module)	- Ceramic module on board (up to 36 chips per module)
- Cooling	- Air	- Air (impingement technique to handle higher logic density)

**II. STORAGE****A. Control storage**

Reloadable monolithic with parity checking

Reloadable monolithic with parity checking

**B. High-speed buffer**

- 16K bytes standard
- 115 nanoseconds fetch and 173 nanoseconds store for a doubleword

- 4K bytes standard in Model Group 11
- 32K bytes standard in Model Group 12
- 64K bytes standard in Model Group 13
- 64K bytes standard for each instruction processor in Model Group 14
- For 4K page, total buffer used
- For 2K page, only half the buffer used for Models 11, 12, 1, and 2
- 68 or 56 nanoseconds fetch and 102 or 84 nanoseconds store for a doubleword

**Hardware Features**

**4341 Model Group 12**

**4381 Model Groups 11, 12, 13, and 14**

C. Processor storage	- 2Mb	- 4Mb (Model Group 11 only)
1. Sizes	- 4Mb	- 8Mb (not Model Group 14)
	- 8Mb	- 16Mb
	- 12Mb	- 24Mb (not Model Group 11)
	- 16Mb	- 32Mb (not Model Group 11)
2. Path to high-speed buffer	16 bytes (two doublewords)	16 bytes (two doublewords)
3. Validity checking	- ECC on a doubleword	- ECC on a doubleword
	- All single-bit errors corrected	- All single-bit and some double-bit errors corrected
4. Technology	- 64K-bit chip, dynamic	- 64K-bit chip, dynamic for up to 16Mb
		- 256K-bit chip dynamic for storage above 16Mb

**III. CHANNELS**

A. Number available	Six standard	- Six standard, six optional for Model Groups 11, 12, and 13
		- Twelve standard, six optional for the Model Group 14
B. Byte multiplexer	- One standard (channel 0)	- One standard (channel 0) for Model Groups 11, 12, and 13
1. Number available	- Channel 4 or 5 can be configured as a second	- Two standard (channel 0 in each group) for Model Group 14
2. Data rates	- 24 Kb/sec for one-byte transfers	- Channel 5 can be configured as a second in Model Groups 11, 12, and 13
		- Channel 5 in each group can be configured as a second for the group in a Model Group 14
		- 24Kb/sec (28Kb for the Model Group 14) for one-byte transfers
		- 2Mb/sec for burst mode (all models)
3. UCWs/subchannels	Up to 256 for a channel	Up to 256 for a channel
C. Block multiplexer	- Five standard	- Five standard and six optional for Model Groups 11, 12, and 13
		- Ten standard and six optional for the Model Group 14
1. Number and data rates in Mb/sec	- Channel 1 - 3	Model Groups 11, 12, and 13
	- Channel 2 - 3	- Channel 1 - 3
	- Channel 3 - 2	- Channel 2 - 3
	- Channel 4 - 3	- Channel 3 - 3
	- Channel 5 - 2	- Channel 4 - 3
	Max Aggregate - 13	- Channel 5 - 2
		Max Aggregate 5 channels - 14
		Model Groups 11, 12, and 13
		- Channel 6 - 2   3   3
		- Channel 7 - 2   3   3
		- Channel 8 - 1   1   3
		- Channel 9 - 1   1   3
		- Channel A - 1   1   3
		- Channel B - 1   1   1
		Max Aggregate 11 channels - 22, 24, and 30

**Hardware Features**

**4341 Model Group 12**

**4381 Model Groups 11, 12, 13, and 14**

		<p>Model Group 14</p> <p>Channel Group 1      Channel Group 2</p> <p>– Channel 1 - 3      Channel 1 - 3</p> <p>– Channel 2 - 3      Channel 2 - 3</p> <p>– Channel 3 - 3      Channel 3 - 3</p> <p>– Channel 4 - 3      Channel 4 - 3</p> <p>– Channel 5 - 3      Channel 5 - 3</p> <p>Max Aggregate 10 channels - 30</p> <p>– Channel 6 - 3      Channel 6 - 3</p> <p>– Channel 7 - 3      Channel 7 - 3</p> <p>– Channel 8 - 3      Channel 8 - 3</p> <p>Max Aggregate 16 channels - 36</p>
2. Selector mode implemented	Yes	Yes
3. Data streaming	Standard on all	Standard on all
4. UCWs/subchannels	Up to 256 on a channel	Up to 256 on a channel
D. Channel retry data in limited channel logout	Yes	Yes—System/370 mode
E. Channel indirect data addressing	Standard	Standard
F. Channel-to-Channel Adapter	One optional	One optional (new packaging)

**IV. SUPPORT PROCESSOR SUBSYSTEM**

A. Components	<ul style="list-style-type: none"> <li>– Support processor</li> <li>– Support bus adapter</li> <li>– Local channel adapter</li> <li>– Console attachment for four natively attached devices</li> <li>– Power adapter</li> <li>– Common communications adapter</li> <li>– One system diskette drive and adapter</li> </ul>	<ul style="list-style-type: none"> <li>– Same as 4341 except two system diskette drives are standard. Different support processor and diskette drives used.</li> </ul>
B. Natively attached devices	<ul style="list-style-type: none"> <li>– Required 3278 Model 2A or 3279 Model 2C as operator console (display and printer-keyboard modes standard)</li> <li>– Up to three units in any combination of 3278 Model 2 displays, 3279 Model 2C displays, 3268 Model 2 or 2C Printers, and 3287 Model 1, 1C, 2, or 2C Printers</li> </ul>	<p>Same as 4341 plus 3205 Color Display Console is available</p> <p>Same as 4341 plus 3205 display, which can not be mixed with 3278 Model 2A or 3279 Model 2C</p>
C. Remote Support Facility	No-charge specify	No-charge specify
D. Remote Operator Console Facility	No-charge specify	No-charge specify

Hardware Features

V. PROGRAMMING SYSTEMS SUPPORT

4341 Model Group 12

System/370 mode:

- DOS/VSE with VSE/Advanced Functions
- OS/VS1 with or without Basic Programming Extensions
- MVS/370 (MVS Release 3.8 with MVS/SP Version 1)
- VM/370 Release 6 without or with VM/Basic System Extensions, or VM/System Extensions, or VM/System Product with or without VM/SP High Performance Option
- VM/SP-Entry
- ACP/TPF

ECPS:VSE mode:

- DOS/VSE with VSE/Advanced Functions
- SSX/VSE Release 2 and later

System/370-XA mode not available

4381 Model Groups 11, 12, 13, and 14

System/370 mode:

- DOS/VSE (with VSE/Advanced Functions) and VSE/SP (Model Groups 11, 12, and 13)
- OS/VS1 with Basic Programming Extensions (Model Groups 11, 12, and 13)
- MVS/370 (MVS Release 3.8 with MVS/SP Version 1 Releases 3.3 and 3.5)
- VM/370 Release 6 with VM/System Product and with or without VM/SP High Performance Option Release 3.2 or later
- VM/SP-Entry (Model Groups 11, 12, and 13)
- ACP/TPF Version 2.3 (Model Groups 11, 12, and 13)

ECPS:VSE mode not available

System/370-XA mode:

- MVS/XA (with MVS/SP Version 2 Release 1.2 or 1.3 and PTFs)
- VM/XA Migration Aid
- VM/XA Systems Facility

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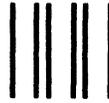
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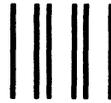
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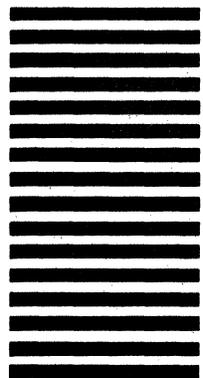
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