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Manual of Instruction

7604 Tape Control

Printed in U.S.A.

A. 7604 TAPE CONTROL

CONTENTS

FOREWORD

This manual is intended for use in training Customer Engineers in the operations of the IBM 7604 Tape Control Unit used with the IBM 7070 System. Illustrations accompany the text. In most cases, the sections, subsections, and items contained within this manual, are written so that the preceding information serves as a building block for subsequent study.

Each program controlled operation is discussed in detail and is accompanied by operation flow charts and sequence charts. Major signals, key timings, and logic locations are also given in chart form. Operations under CE panel control are discussed in a like manner.

Because of the similarity to Tape operations, Disk Storage operations with reference to channel controls are not discussed in this manual.

Future engineering changes may cause minor discrepancies in some of the timings given in sequence charts and other charts (signal, timing, and location). They should not change the philosophy of the operations unless the changes are of a major nature and constitute revisions to data flow and operation sequence.

ILLUSTRATIONS

1.0.00 INTRODUCTION

The 7070 Tape System is used in block transmission of data. With this system a group or several groups of words can be moved with a single instruction. The number of words moved and the blocks they are divided into are limited only by the capacity of core storage.

The locations of the various blocks of storage to be read into or written from are defined by record definition words (control words). The data address portion of a tape instruction (positions 6 - 9) contains the location of the first record definition word to be used. A record definition word contains the first and last address of the first block of storage words to be read into or written from. When it is addressed by the program instruction, it is parallel-transferred to the record-definition register which is located in a channel control unit.

1.1.00 TAPE SYSTEM

Although the tape system operates independently from A&P, several units eral units are needed to make up a system. Figure 1.1-1 shows these various units and the bus system used for addressing core storage and the transferring of data to and from tape.

1.1.01 Arithmetic and Programming Unit (7601)

The Arithmetic and Programming Unit (A & P) identifies the tape operation and initiates the tape signals to select the proper tape channel control unit and the tape drive unit. With the tape channel control unit and tape drive selected, the tape instruction is transferred to the tape channel control unit and the A & P unit is restarted.

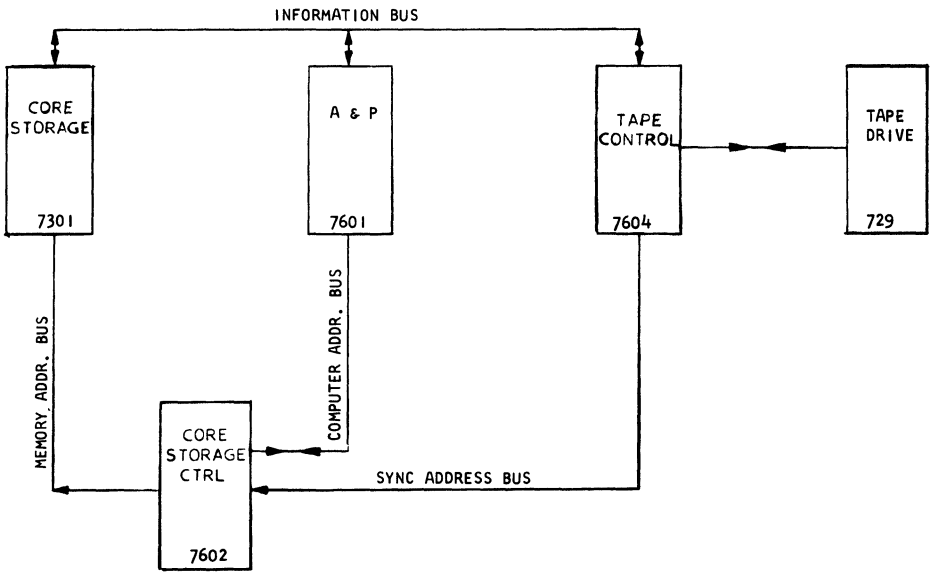


FIGURE 1.1-1. TAPE SYSTEM

1.1.02 Power and Core Control Unit (7602)

The Power and Core Control Unit is used to control the addressing of core storage for reading in and reading out. Both the Computer Address Bus and the Tape Sync Address Bus are coupled to this unit which in turn furnishes the address to the core storage unit via the memory address bus. An address generator provides a means of generating core storage addresses. This circuitry is used to develop the addresses for the various areas which are reserved within core storage.

1.1.03 Core Storage Unit (7301)

The Core Storage Unit consists of the 5,000 or 9,990 words of storage. This unit also contains the various drivers and controls to read in or read out the addressed location.

1.1.04 Tape Control Unit (7604)

The Tape Control Unit contains the two tape channels and their respective tape-adapter controls. The channels control the transfer of data to and from core storage. The tape adapter circuitry controls the flow of data between the control unit and the specified tape drive unit.

1.1.05 Tape Drive (729)

The 729 Model II or IV Tape Drive Units are used with the 7070 system. Both drives are modified multifunction tape drives which have the ability to write in two densities, high and low.

	MODEL II		MODEL IV	
	High	Low	High	Low
CHARACTER PER INCH	556	200	556	200
PASSING SPEED - INCH/SEC.	75	75	112.5	112.5
CHARACTERS PER SECOND	41,700	15,000	62,500	22,500

6 tape drives per sync Standard
~~Optional~~ tape drives 7-10 extra feature on each sync.

1.2.00 CONTROL UNIT COMPONENTS

The 7070 Tape System contains two tape channel control units, each of which connects to as many as six tape drive units (Figure 1.2-1).

Each of these channel control units contains the following components:

1. Record Definition Register
2. Control Register A
3. Match, Mismatch and One Upper
4. Buffer Registers A and B

1.2.01 Record Definition Register

The Record Definition Register is a combination of two 4-position shift registers which contain the start and stop portions of the tape control words during a tape operation. Positions 2 - 5 of the control word contain the start address and designate the the first word of a block to be transferred. Positions 6 - 9 contain the stop address and identify the last word of a block. The start address becomes the working address and specifies the storage location that the first word on tape is to be read into or written from.

1.2.02 Match, Mismatch and One Upper

During the tape read or write operations, the start and stop addresses are read out to the match and mismatch circuitry where they are compared. If a mismatch is sensed, the start address is increased by one via the one upper circuitry, and the next word is moved to or from the new core storage location specified by the start address. This process continues until the start and stop addresses become equal. When they do, the last word is transferred, and the control word sign latches are tested to see if a new control word is to be read in or the operation stopped.

The compare operation between the start and stop addresses is on an equal-unequal basis only. If the start address of the control word should be higher than the stop address, the operation continues until the start address exceeds the capacity of core storage or the end of a record is reached on reading. An error is indicated for either condition. The start address must be smaller than the stop address in all control words to obtain a match condition.

1.2.03 Control Register A

The Control Register A designates the locations of the tape control words. The setting of this register can also be increased by one via the one upper circuitry under control of the control word sign latches. If the control word sign is plus, the Control Address Register A is increased by one and a new control word is brought in from core storage to designate a new block of words, and the process begins again. If the sign is minus, it means that this word is the last record definition word to be used in the operation.

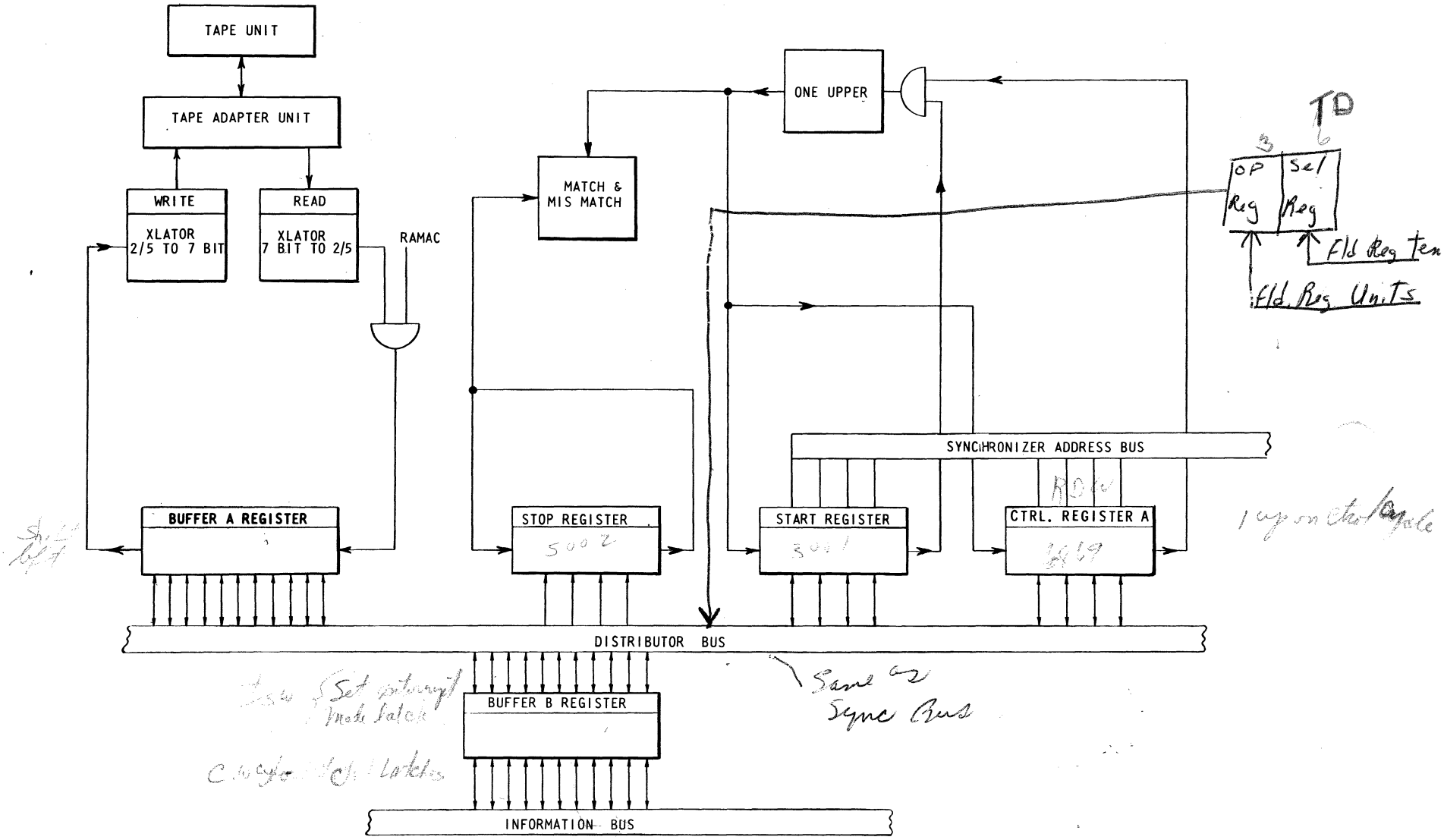


FIGURE 1.2-1. TAPE CHANNEL CONTROL UNITS

1.2.04 Buffer Registers A and B

When reading or writing on tape, all data passes through both the buffer B and buffer A registers. These registers change the type of transmission from serial to parallel, or vice versa, and to synchronize between the speeds of tape and the speed of core storage. Data must move to and from tape serially, but is always sent to and from core storage in parallel.

When reading a tape, the characters are read serially into register A until the ten digit positions are filled. Register A is then parallel transferred to buffer B, and register A starts filling up serially again. The contents of register B are parallel transferred to the location specified by the start address of the record definition register.

When writing on tape from core storage, the data word is parallel transferred to the B register and from there is parallel transferred to register A. The data is then read out serially to the specified tape drive.

1.3.00 TAPE FORMAT

Each word is written and read in either the alphanumeric or numeric mode. An alpha word written on tape consists of five characters. A numeric word takes one tape character for each digit, and appears on tape as it is in core storage, except that the sign is recorded as a zone with the units character.

In tape writing the sign of each core storage word determines the mode. Tape writing automatically starts in alpha mode. Each time the sign changes from alpha-to-numeric mode or numeric-to-alpha mode a mode character is automatically recorded on tape (△). The mode character appears only on tape; it can never enter core storage from tape.

An example of a three-word record written on tape is as follows:

+0 1 2 3 4 6 8 9 2 4

-6 7 5 5 3 2 0 6 4 9

A 7 4 6 1 8 8 9 1 9 0

The record is written on tape as follows:

△ 0 1 2 3 4 6 8 9 2 D 6 7 5 5 3 2 0 6 4 R △ M A Y 1 0

Because tape writing always starts in the alpha mode, the first character written is the mode change designation (△). This designates a change in mode from alpha to numeric. The second △ on the tape is created by the alpha sign in the third word. The letter D is created by the units-digit four and the plus sign. The R is created by the digit nine and the minus sign.

When reading from tape, the sign of the record determines the alpha or numeric mode. Tape reading automatically starts in the alpha mode. The mode is changed to numeric when the mode change character is detected. When in the alpha mode, the five character record is automatically translated into a ten-digit word with an alphabetic

sign. Numeric words are read without change except for the units position, whose zone is interpreted to give a plus or a minus designation to the word.

1.4.00 DATA FLOW

The tape read or write operations are performed in various steps, these are as follows:

1. Instruction Word
2. Initial Status Word
3. Control Word
4. Data Word
5. Final Status Word

Each of these steps is used in requesting the use of core storage, and controlling the transferring of data to and from tape.

1.4.01 Instruction Word

In the A & P unit, a tape instruction word is read from core storage into the Op Register, Field Register and the Program Register D via the information bus. While the instruction is on the information bus, it is sampled to see if an index operation is to be performed on the data portion of the instruction. The contents of the program field register are read out to the tape channel control unit to set up the specified tape controls and to select the proper tape drive. The A & P unit will not interpret the operation code until it is assured that the tape channel control unit is not busy.

If the busy signal is not present, the A & P furnishes a tape call signal to the selected channel control unit. The tape call signal conditions the buffer B register to accept the contents of the Op Register, I Counter and the Program Register D, which are transferred via the information bus. A restart signal from the channel control unit is then sent out to restart the A & P unit.

1.4.02 Initial Status Word

On a read or write operation the instruction word is operated upon in register B to insert the tape operation code into position one. The channel control unit then requests a memory cycle to store this new word, called the Initial Status Word. When core storage accepts the request, it replies with an address gate and an information gate. During the initial status word cycle, the alpha sign latch is set so that both tape read and write operations start in the alpha mode.

At address gate time the memory address trigger register is set by the address generator as conditioned by the selected tape drive and tape channel control unit. Figure 1.4-1 shows the locations assigned for the various tape drive control unit combinations. At information gate time the contents of the buffer B register (ISW) are parallel transferred to this core storage location. At the time that the initial status word is read out to the information bus, the data address portion and the sign are read out to the distributor bus. The data address is stored in Control Register A. The sign position is analyzed and, if plus, the interrupt mode latch is set.

1.4.03 Control Word

With the data address in the Control Register A, the channel control unit requests another memory cycle. When core storage accepts the request, its reply is sent in the form of an address gate followed by an information gate. The address gate allows the contents of the Control Register A to be parallel-transferred, via the sync address bus, to the memory address trigger registers to condition the location within core storage which has the control word (record definition word). The contents of the Control Register A are regenerated.

At information gate time, the control word is parallel-transferred from core storage to the buffer B register via the information bus. The contents of the buffer B register are then parallel-transferred, via the distributor bus, to the record definition register to set up the start and stop addresses of the block of information to be transferred. As the control word is read out to the distributor bus, the sign position is analyzed and the appropriate control word sign latch set.

During the reading in of the control word, the Control Register A address is increased by one to develop the address of the next control word.

1.4.04 Data Word

During the reading in of the control word, the channel control unit immediately requests another memory cycle. When core storage is free, an address gate is developed and sent to the control unit. The address gate conditions the controls to read out the start address on the sync address bus. This start address specifies the word of a block that is to be transferred to the buffer B register.

At information time the data word is parallel-transferred via the information bus to the buffer B register. During the transfer of the data word, the start and stop addresses are compared for a match or a mismatch.

As the compare operation is being performed the contents of buffer B are parallel-transferred to buffer A via the distributor bus. As the ten digits of information and the sign are placed on the distributor bus, the sign position is analyzed and the alpha or numeric sign latch is set. The alpha sign latch was initially set during the initial status word cycle; if a numeric designation is sensed, a mode change is performed.

The outputs from the sign latches are used to condition the tape translator and also to set the tag position associated with the buffer A register. The tag is used to signify the end of a ten-digit shift operation. The tag is set in position eight for a numeric word and position four for an alpha word.

With the tag set and the translator conditioned, buffer register A is left-shifted to place the first digit of information into the translator. If a numeric word has been sensed, the register serially shifts one position at a time. However, with an alpha word, two positions are shifted at a time.

The information entering the translator on a write operation is in the 2-out-of-5 code (63210). This information is translated into the seven-bit code (C B A 8421). Reading from tape, the seven-bit code is translated into the 2-out-of-5 code. Both the reading and writing translation takes place in the same core matrix translator.

When the tape drive is selected and ready to write, the contents of the buffer A register continue to left-shift serially character by character.

During the reading in of the data word to buffer B, a 0-up start operation is performed to determine if more than one data word is to be used. If, at the completion of the 0-up operation, a mismatch is sensed, the start register address is increased by one. At the completion of the 1-up operation, the second data word request is initiated to place the data word into buffer B. With the reading in of the second data word, the 0-Up and 1-Up operation is repeated to determine the address of the next data word.

The third data word request is not used until the BA register is performing its last serial shift.

If, at the completion of a 0-up operation, a match signal is present, the control word sign is analyzed. With a plus sign sensed a new control word (record definition word), specified by the Control Register A, is read out of core storage to the record definition register (start and stop register).

With a minus sign sensed, the operation is discontinued and a signal is created after the last character is checked to start the final status word cycle.

1.4.05 Final Status Word

To initiate the final status word cycle the tape channel control unit sends out a memory request signal. When core storage replies with an address gate, a location within core storage is also addressed by the address generator according to the tape drive and the tape control unit that were used. Figure 1.4-1 shows the locations reserved for the various tape drive and synchronizer combinations.

TAPE	CHANNEL 1		CHANNEL 2		CHANNEL 3		CHANNEL 4	
DRIVE	FINAL	INITIAL	FINAL	INITIAL	FINAL	INITIAL	FINAL	INITIAL
0	0110	0160	0120	0170	0130	0180	0140	0190
1	0111	0161	0121	0171	0131	0181	0141	0191
2	0112	0162	0122	0172	0132	0182	0142	0192
3	0113	0163	0123	0173	0133	0183	0143	0193
4	0114	0164	0124	0174	0134	0184	0144	0194
5	0115	0165	0125	0175	0135	0185	0145	0195
6	0116	0166	0126	0176	0136	0186	0146	0196
7	0117	0167	0127	0177	0137	0187	0147	0197
8	0118	0168	0128	0178	0138	0188	0148	0198
9	0119	0169	0129	0179	0139	0189	0149	0199

FIGURE 1.4-1. STATUS WORD LOCATION

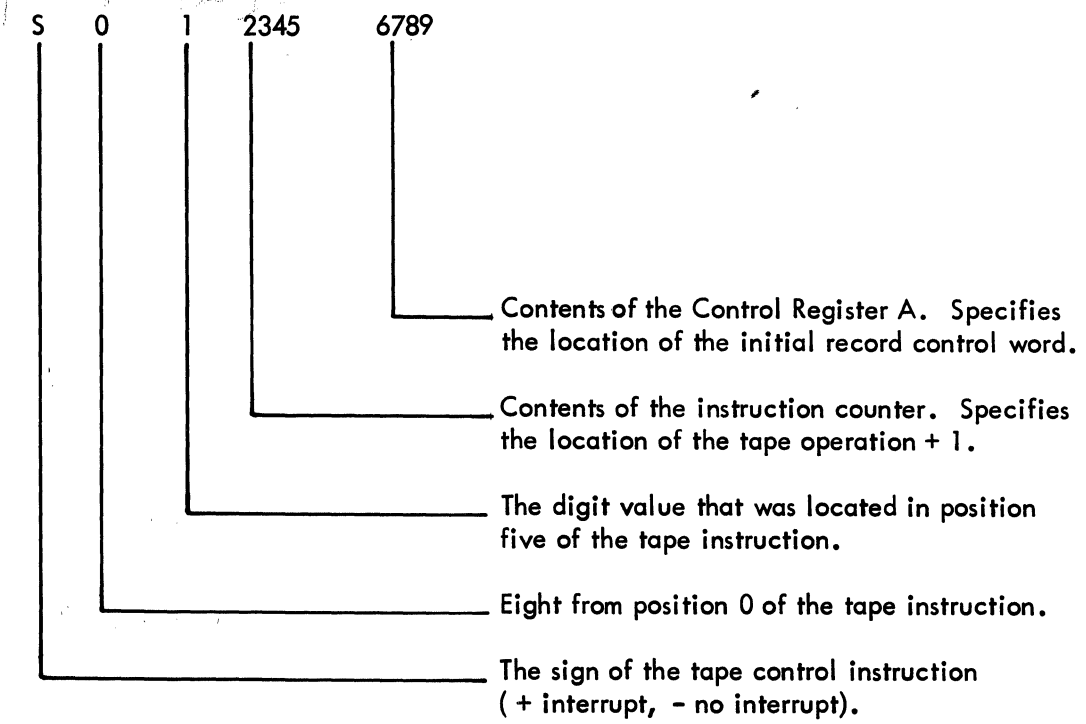
At information gate time the contents of the conditioned core storage location are parallel transferred via the information bus to the buffer B register. Buffer B now has the final status word, which was developed from a previous tape operation using the same tape drive and channel control unit.

With this word transferred into the buffer B register, the tape channel control unit requests another memory cycle. When core storage replies with an address gate, the contents of the start address, control register A and the + sign and the error condition are inserted via the distributor bus to the buffer B register. This forms the final status word. At information time the new contents of the buffer B register are parallel transferred via the information bus to its specified final status word location within core storage.

1.5.00 STATUS WORDS

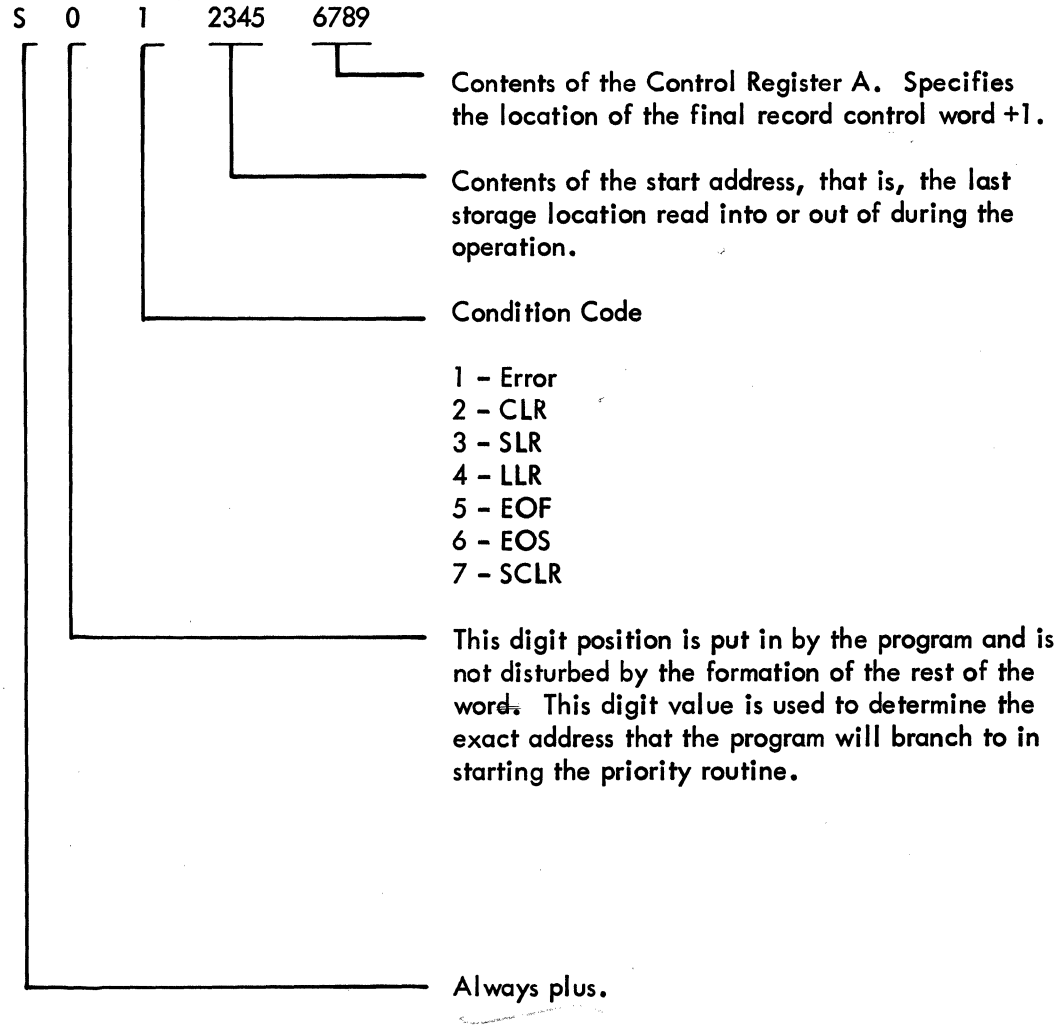
There are two status words formed, initial and final. Every tape instruction that might cause an interrupt signal when it is completed automatically creates an initial status word at the beginning of the operation. The format of the initial status word is as follows:

1.5.01 Initial Status Word



1.5.02 Final Status Word

A final status word is automatically created at the conclusion of each tape operation which also formed an initial status word.



The condition code in position one indicates whether the priority signal is due to a normal or an unusual condition, and specifically what the condition is. All but CLR are unusual codes. The digits in this position have the following meaning:

1. Error

These are machine checks.

a. Vertical redundancy check on tape character.
b. Longitudinal redundancy check on a tape record.
c. Two-out-of-five validity check on data transferred.

d. A translator input bit loss.
e. In reading numeric data, ten digits are read with no sign indication.
f. An invalid address.
g. Core inhibit driver error.
h. Match error.
i. Control word sign error.
j. Memory request error.
k. A two digit combination in an alpha word which does not represent an alpha character.
l. Failure of all write heads to operate.

The occurrence of an error condition takes precedence over any other condition that may exist at the same time.

2. Correct Length Record (CLR)

This is the normal condition without error.

3. Short Length Record (SLR)

This occurs if the start and stop addresses in the record definition register are not the same when the end of tape record is reached (the inter-record gap) in tape reading.

4. Long Length Record (LLR)

The long length record occurs if the start and stop address in the record definition register coincides before the tape record has been entirely read.

5. End of File (EOF)

The end of file indication occurs when a tape mark is sensed during a read operation or the end of file reflective spot is sensed when writing.

Either of these operations turns on the tape indicator in the tape drive.

6. End of Segment (EOS)

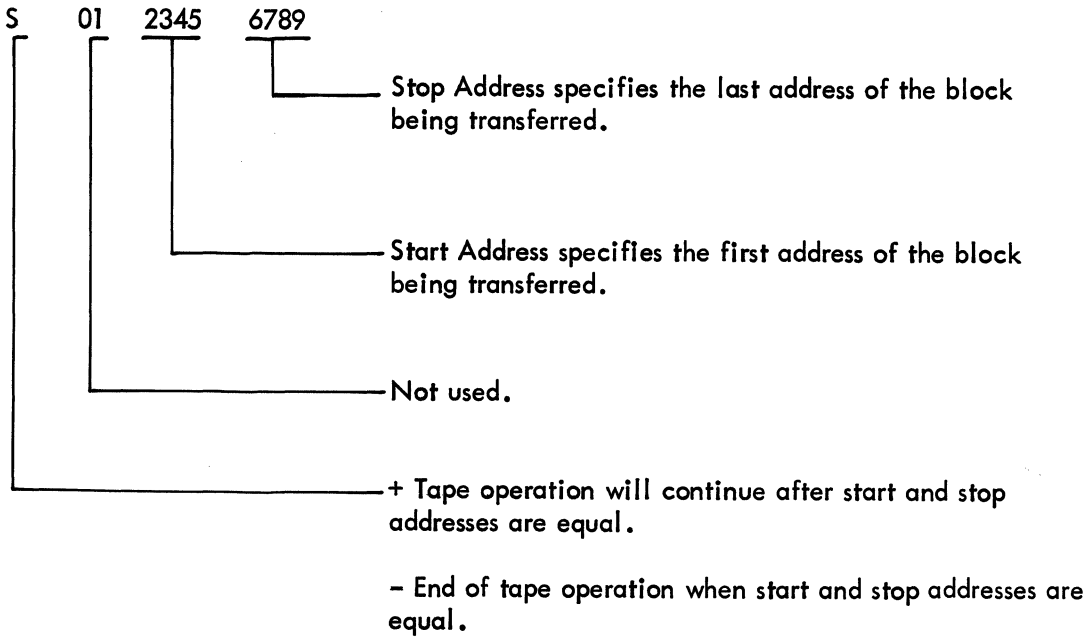
The end of segment occurs on reading a segment mark during a read operation (CA 8421).

7. Short Character Length Record (SCLR)

This occurs when the number of characters is not an exact word length. In such cases the rest of the word is filled with zeros before storing.

1.5.03 Record Definition Word (Control Word)

The locations of the various blocks of core storage to be read into or written from are defined by record defintion words (control words). The control word uses the following format:



2.0.00 DATA PROCESSING ELEMENTS

Magnetic-core shift registers are used in the tape channel control units. These registers have multiple read-in and read-out windings to provide flexible operations.

The shift registers are capable of both serial and parallel transfers and are designed to handle 2-out-of-5 data transfers.

A six microsecond transfer timing is used within the channel control unit (UVWXYZ). This timing is used to synchronize the read-in and read-out of all the registers. The registers are read out at U-time and read into at Y-time.

2.1.00 BUFFER A REGISTER (Figure 2.1-1)

The buffer A register is a magnetic-core shift register with ten digit positions and a sign position. The A-register is used to change the type of transmission from serial to parallel or parallel to serial. Data is moved to and from tape serially but is always sent to and from core storage in parallel. This register is also used as a synchronous storage media between the tape drive and core storage.

The A-register is composed of SR3 cards with three inputs and three outputs. The entire register can be parallel-transferred to and from the distributor bus in one transfer time. The contents of the A-register regenerate in parallel by reading out to the serial capacitors at U-time and reading in at Y-time.

The A-register has the ability to have zeros entered into the six low-order positions. These zeros are inserted prior to a read numeric operation. If a six-digit word is read in from tape, the four high-order positions will be zeros, so that a complete ten-digit word is available for parallel transfer to core storage. An error condition is signalled if more than ten or fewer than five digits are read to core storage. These zeros are read into the buffer A register at the beginning of a tape read operation and thereafter on each data word transfer from buffer A to buffer B.

When writing on tape the information is read from the high-order position of the register (0-position). On reading from tape, the information is read into the low-order position (9-position).

The A-register is also left-shifted a digit at a time when reading or writing on tape. Because the tape may be reading or writing alpha or numeric information, the register is equipped with two types of left shifts. When a ten-digit numeric word is read or written, the information is left-shifted, digit by digit. This type of operation takes ten left shifts per word. When an alpha word is read from or written on tape, the information is left-shifted in digit pairs; therefore in alpha mode, five left shifts are needed per word.

For example, when an alpha character is written on tape, the contents of the 0 and 1 position is read out at the same time, the contents of the second position reads into position 0, and the contents of the third position reads into position 1 (Figure 2.1-1), etc.

To keep track of the number of places to be shifted, a tag position has been added to the A register. The tag position is made up of five SR 1 cards (ten positions) and is left shifted a digit at a time.

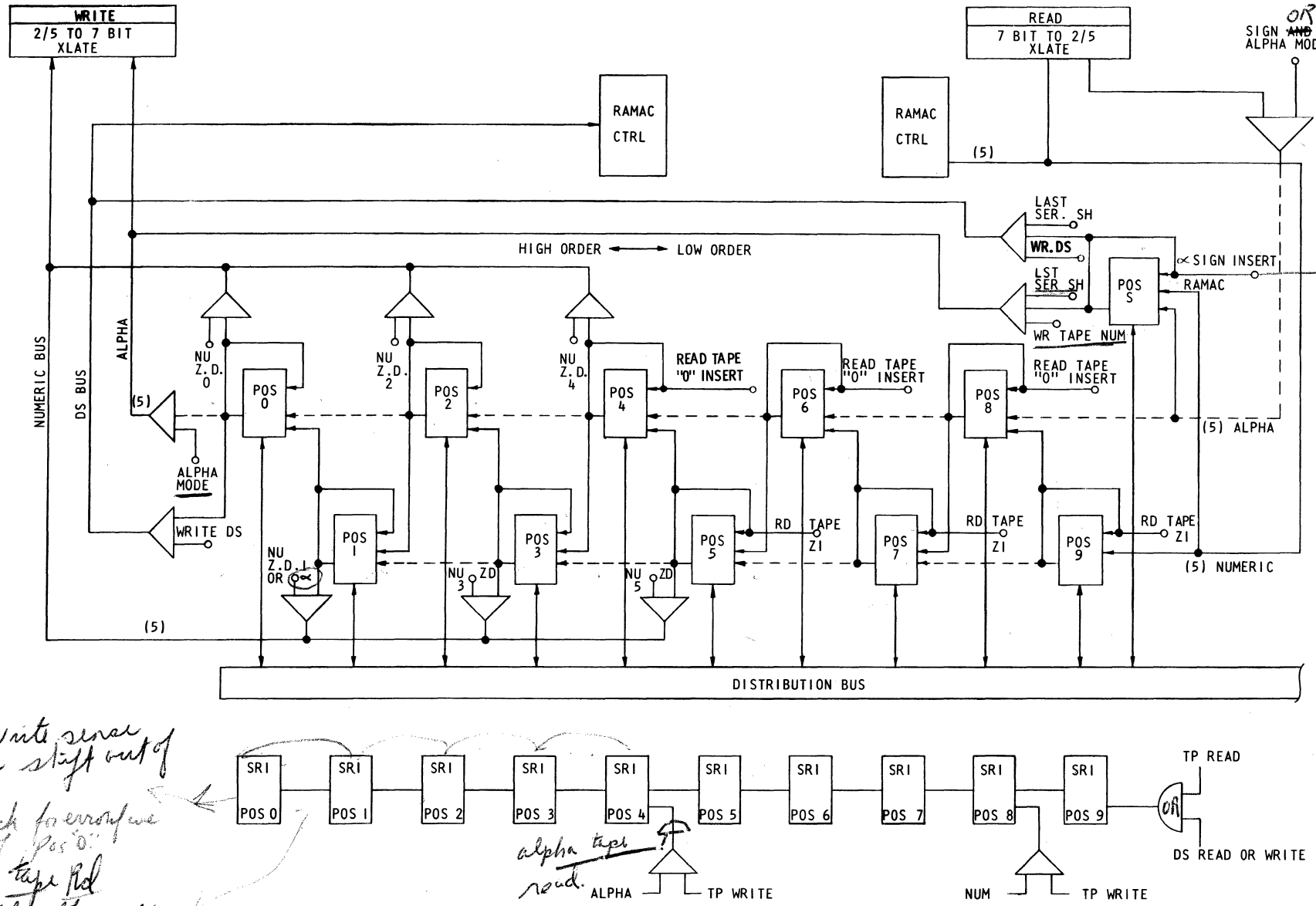


FIGURE 2.1-1. BUFFER A REGISTER AND TAG INSERT

When a numeric word is written, the tag is inserted into the output capacitor of position eight. As the tag advances out of position 0, it is sensed. This signifies that one more left-shift is to be taken.

Because an alpha word takes only five left-shifts, the tag is inserted into the output capacitor of position four. When the tag advances into position 0, it signifies that one more left shift is to be taken. The tag position advances digit by digit, while the register advances two digits at a time.

During read operations, the tag is inserted into position 9 for numeric operations and position 4 for alpha operations. If the tag is read out of position zero during a numeric read operation, an error condition is developed which signifies a missing sign over units.

The tag can also be sensed in positions 5, 4, 3, 2, 1. This type of tag sense is used during a zero elimination operation.

2.2.00 BUFFER B REGISTER (Figure 2.2-1)

The buffer B register is a magnetic-core shift register with ten digit positions and a sign position. The buffer B register can be used for parallel-transferring of data to and from core storage via the information bus. The buffer B register also has provisions for parallel-transferring of data to the distributor bus.

The B register is composed of SR 1 cards with two inputs and two outputs. The entire register can be parallel-transferred to and from the information bus or the distributor bus in one digit time. Regeneration in the B register is accomplished by reading out in parallel to the capacitors on the distributor bus at U-time and reading in from the capacitors at Y-time.

The buffer B register also has the ability to read out to the information bus and the distributor bus during the same digit time. To accomplish this operation both the read out control drivers are turned on. One driver controls the reading out to the information bus, and another set of drivers allows the distributor bus capacitors to be charged at U-time. The following read-in time (Y-time) the information bus capacitors are sensed by core storage and cleared, and the distributor bus is read into the conditioned register. During this operation, therefore, the buffer B register cannot be regenerated.

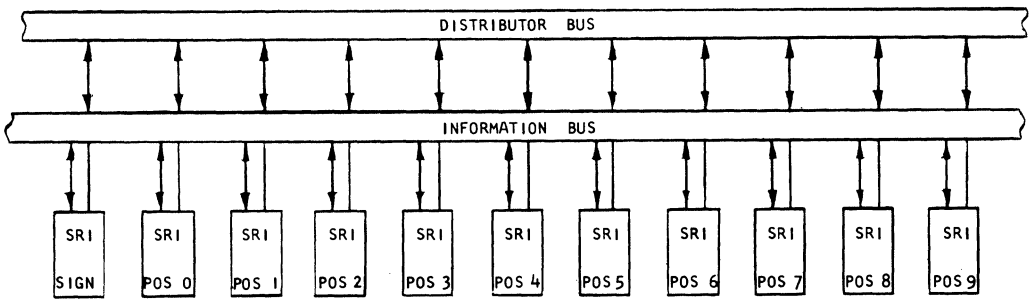


FIGURE 2.2-1. BUFFER B REGISTER

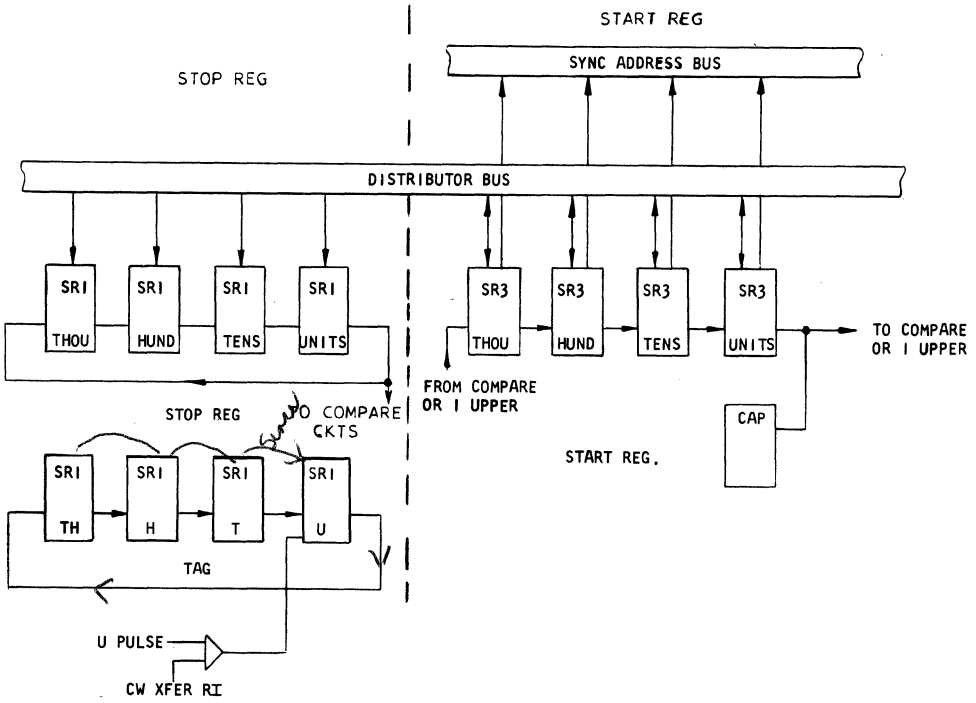


FIGURE 2.3-1. RECORD DEFINITION REGISTER

2.3.00 RECORD DEFINITION REGISTER (Figure 2.3-1)

The record definition register is made up of two 4-position shift registers which receive the tape control words during a tape operation. Four positions are used to hold the start address, and the other four positions the stop address. These two registers can be parallel transferred and serially right-shifted.

2.3.01 Start Register

The start register is a four-position core-shift register with the ability to parallel transfer, and serially shift-right.

The start register is composed of SR 3 cards with three inputs and three outputs. The entire register can be parallel transferred in one digit time. The register reads out and regenerates every digit time. This is accomplished by reading into the serial shift capacitor at U-time and reading back at Y-time.

When the data is parallel transferring onto the sync address bus or the distributor bus, both the appropriate parallel read-out control driver and the serial read-out control driver are brought up. The contents of the start register is read out to the bus capacitors and the serial capacitors at the same time. At read-in time the contents of the serial capacitors are read back into the cores, thereby retaining the contents of the registers.

The start register also has the ability to serial right-shift a digit at a time. When right shifting, the units position is read out to an external capacitor which in turn is read into the one-upper circuitry. The output of the one-upper circuitry is read back into the thousands position of the register during the same digit time. A shift of four places takes four digit times (24 usec).

2.3.02 Stop Register

The stop register is a four-position core-shift register with the ability to be parallel transferred into and serially right-shifted.

The stop register is composed of SR 1 cards with two inputs and two outputs. The stop register is also used as a ring to indicate the number of shifts for 0-up and 1-up operations.

When the register is not shifting, the contents of the register is regenerated by reading out to the serial capacitors at U-time and reading back in at Y-time.

When right shifting, the units position of the register is read out to the match-mismatch circuitry. The contents of the stop register is retained by connecting the serial output from the units position of the register to the serial input in the thousands position.

To keep track of the number of places shifted, a tag position has been added to the stop register. The tag position is made up of four SR 1 cards.

The tag is inserted into the units position serial capacitor. With the first serial right-shift the tag is advanced into the thousands position. When the tag advances ~~into~~ out of the tens position, it is sensed to indicate a shift of four places.

2.4.00 CONTROL REGISTER A (Figure 2.4-1)

The control register A is a four-position core-shift register with the abilty to paralle' transfer and serially right-shift.

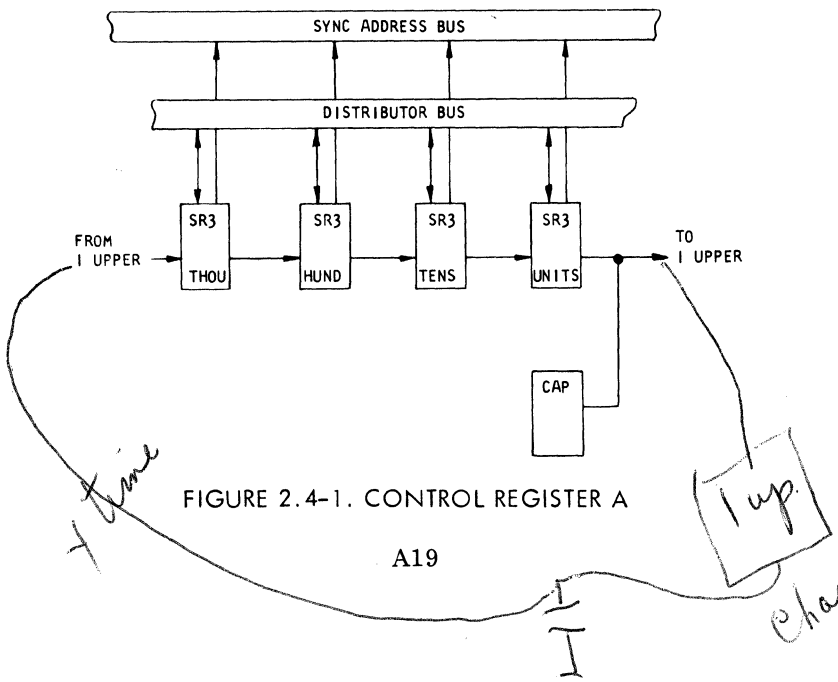


FIGURE 2.4-1. CONTROL REGISTER A

The control register is composed of SR 3 cards with three inputs and three outputs. The entire register can be parallel-transferred in one digit time. The register will read out and regenerate every digit time. This is accomplished by reading into the serial shift capacitor at U-time and reading back at Y-time.

When parallel-transferring the data onto the sync address bus or the distributor bus, both the appropriate parallel read-out control driver and the serial read-out control driver are brought up. The contents of the control register is read out to the bus capacitors and the serial capacitors at the same time. At read-in time the contents of the serial capacitors is read back into the cores, thereby retaining the contents of the register.

The control register also has the ability to serial right-shift a digit at a time. When right-shifting, the units position is read out to an external capacitor which in turn is read into one-upper circuitry. The output of the one-upper circuitry is read back into the thousands position of the register during the same digit time. A shift of four places takes four digit times (24 usec).

2.5.00 ONE-UPPER, MATCH AND MISMATCH

The one-upper and matching circuits are necessary to generate new addresses and control the record definition register. The addresses within a group are sequential and are used for addressing core storage.

The record definition register is pre-set with start and stop addresses of the control word. The range of addresses between the start and stop are produced by adding one to the start register via the one-upper circuitry. The results are matched with the stop register.

When the coincidence between start and stop is reached; another condition, a plus or minus in the sign position of the control word, determines whether to stop the generation of addresses or to order a new group of addresses.

The location of the new group of addresses is determined by the contents of control register A. This address specifies the word in core storage that contains the new start and stop addresses. These words are called control words and have previously been stored in sequential core storage locations.

Figure 2.5-1 shows a block diagram of the registers and the various paths for reading into the match, mismatch and one-upper circuitry.

As the control word is placed into the record definition register, a tag is inserted into the units position of the stop register. The tag output from the units position along with a 0-up signal causes the mismatch latch to be reset and the match latch turned on. With the first serial shift-right, the tag is read into the high-order position of the tag register. The stop register acts as a ring to indicate a shift of four places for the 0-up and 1-up operations.

The one-upper and match and mismatch operations are performed in steps. Each of these steps is controlled by the following latches: 0-up start, 1-up start, and 1-up control register latch.

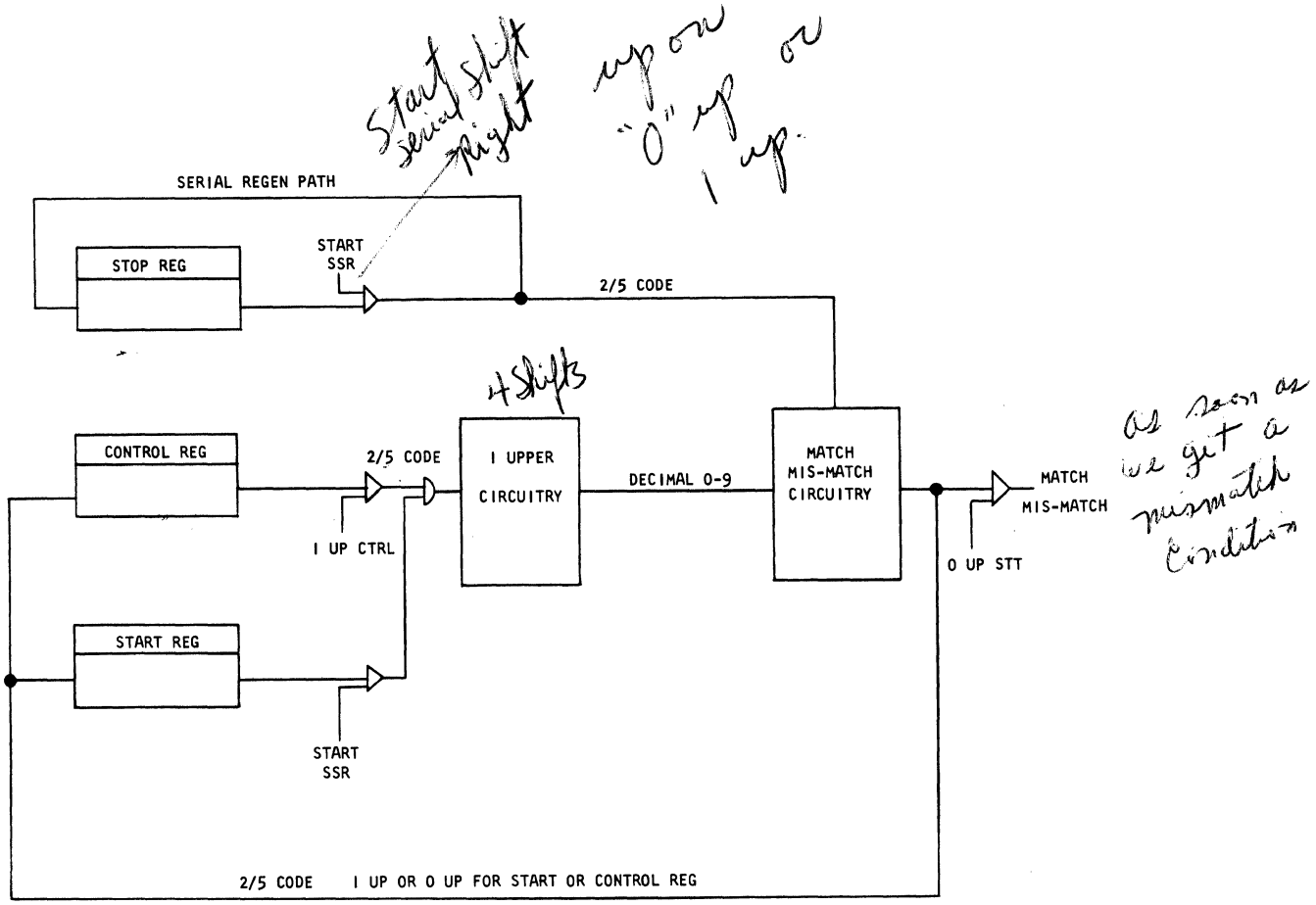


FIGURE 2.5-1. ONE-UPPER, MATCH AND MIS-MATCH BLOCK DIAGRAM

2.5.01 Zero-up (0-up) Start Operation

The comparing of the start and stop addresses is started the moment the data word is requested from core storage. It is necessary to compare the initial start address with the stop address before adding 1 to the start register to prevent missing a match on a one-word record.

The comparing of the start and stop register is started by turning on the 0-up start latch. The output of the 0-up start latch is used to gate the contents of both start and stop register to the match-mismatch circuits. The gating of the registers is accomplished by developing the start serial shift-right signal. It can be seen from Figures 2.5-1 and 2.5-2 that the 2-out-of-5 contents of the start register is converted to decimal form and then gated into the match-mismatch circuitry, via the one-upper by the STT SRR signal. This signal was developed when the 0-up start latch was turned on.

The contents of the stop register is also gated by the start serial shift-right signal and sent to the match-mismatch circuits where the comparison is performed digit by digit. The contents of the stop register remains in the 2-out-of-5 code. The stop register is regenerated via the serial regen path. The contents of the start register are serially read into the high-order position via the 0-up path.

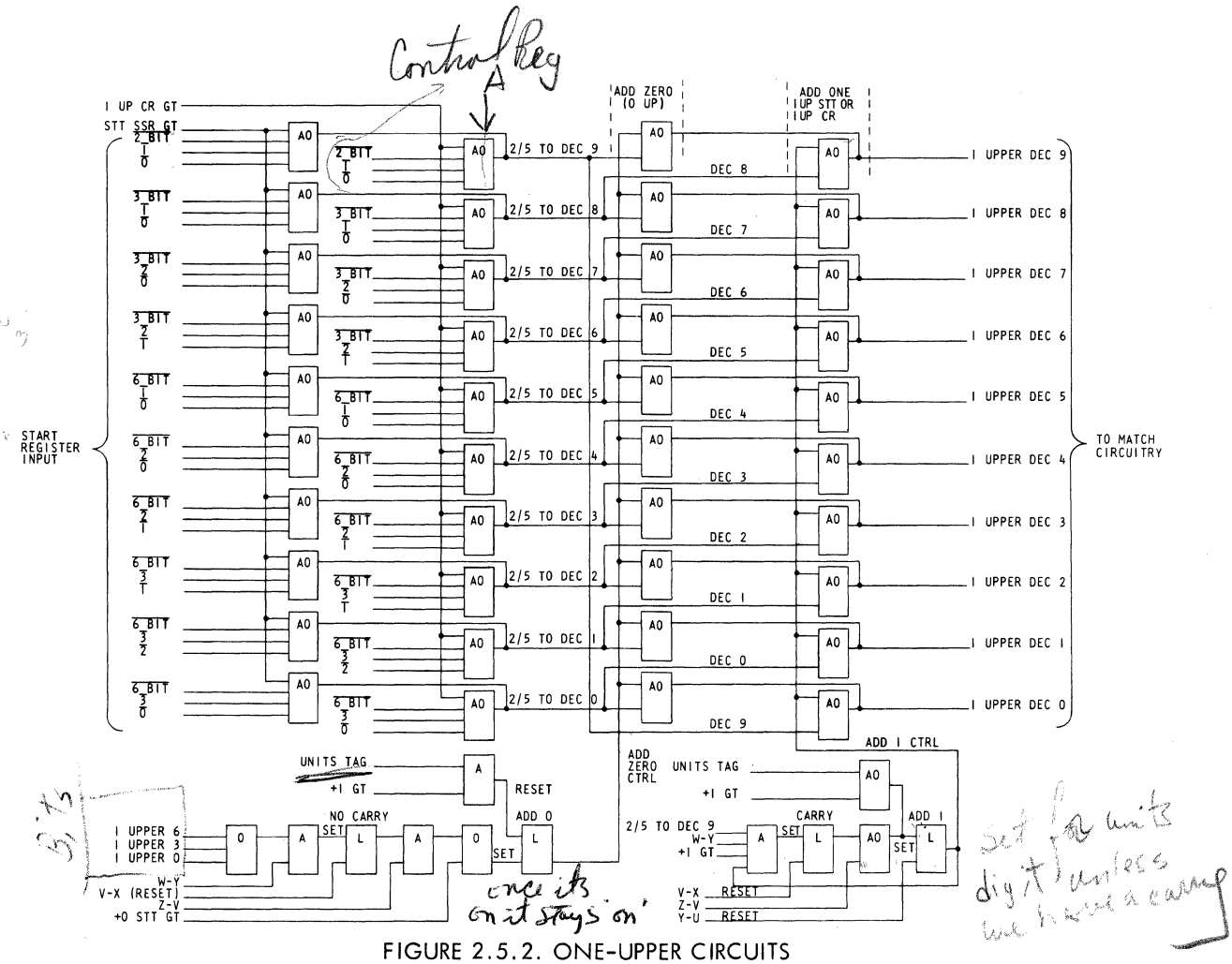


FIGURE 2.5.2. ONE-UPPER CIRCUITS

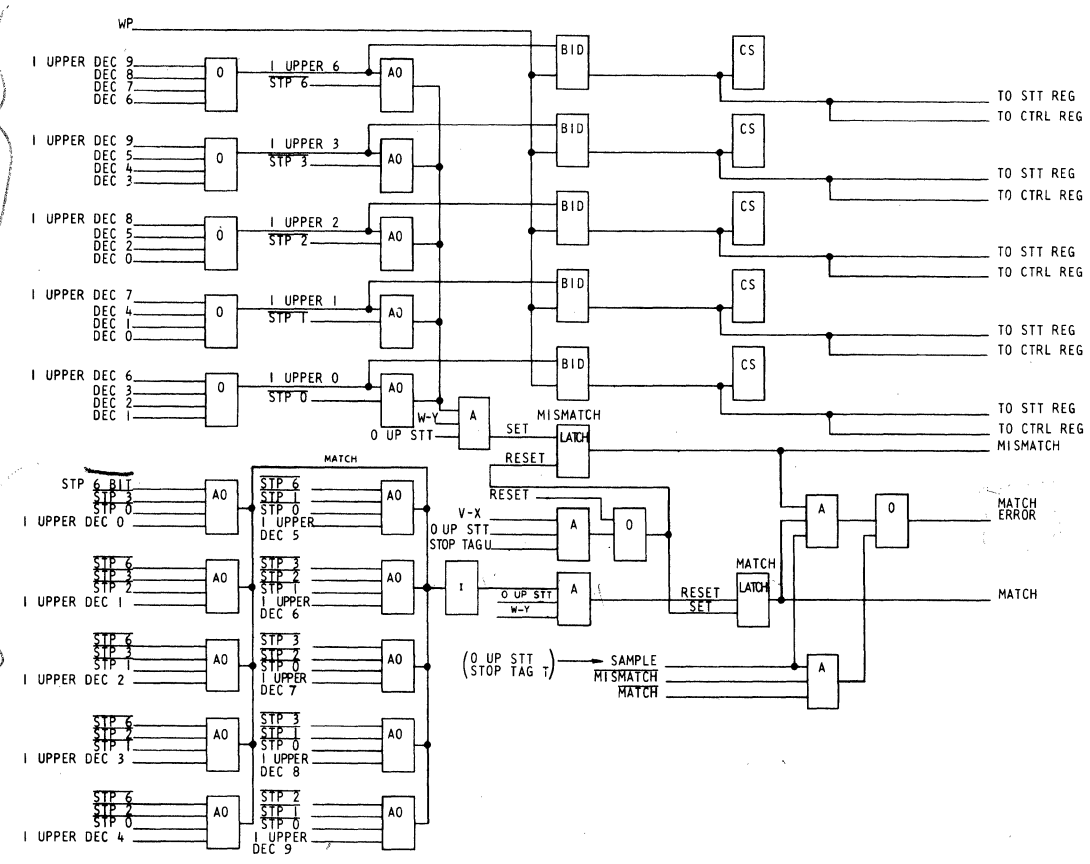


FIGURE 2.5-3. MATCH --MIS-MATCH CIRCUITS

Assume the following values are in the record definition register:

Start	Address	0100
Stop	Address	0110

On the first right-shift, the compare circuitry develops a match signal, because the units positions of the start and stop register have the same value. On the second right-shift operation, a mismatch is sensed, because the tens position of the start and stop register differ. With a mismatch sensed, the match latch is turned off and the mismatch latch is turned on (Figure 2.5-3). The mismatch latch remains on for the following two shifts even though the next two digits match.

The end of the compare operation is sensed when the tag advances out of the tens position of the stop register. This signifies that a right-shift of four places has been completed. At this point the 0-up start latch is reset and the 1-up start operation is initiated.

2.5.02 One-Up Operation

With a mismatch sensed, the units position of the start address must be updated by one via the one-upper circuitry.

As the 0-up start latch was reset, the 1-up start latch is turned on. The output of this latch develops the start serial shift-right gate and also turns on the add-one latch. The start serial shift-right gate allows the contents of both the start and stop registers to be right-shifted digit by digit. The contents of the stop register is regenerated via the serial regen path.

Figure 2.5-2 shows that the contents of the start register is converted to decimal and sent to the match-mismatch circuitry via the add-one switching. The output of the match-mismatch circuitry is converted to the 2-out-of-5 code and stored back into the high-order position of the start register. At the completion of adding one to the units position of the start register, the add-one latch is reset. However, if a carry was developed from the units position, the add-one latch remains on to 1-up the tens position of the start register. The adding of one to the start register positions continues until a no-carry is sensed. A no-carry turns on the add-0 latch and zeros are added to the rest of the digits being read out.

The 1-Up start operation continues until the tag is sensed in the tens position of the stop register. This signifies that a shift of four places has been completed.

2.5.03 One-Up Control Operation

The one-upping of the control register is performed during each control word cycle. The 1-up control register latch is turned on after the core storage address triggers have been conditioned to read out the control word.

Figure 2.5-2 shows that the contents of the control register is converted to decimal form and entered into the one-upper via the add-one switching. The output of the one-upper is converted back to 2-out-of-5 code and stored back into the high-order

position of the control register. At this point the add-one latch is reset. However, if a carry was developed from the units position, the add-one latch remains on and the tens position of the control register would be updated by one. The adding of one to the control register continues until a no-carry is sensed. A no-carry turns on the add-0 latch and zeros are added to the rest of the digits being read out.

The updated address in the control register is used if the sign of the control word is plus. This address then specifies the location of the next control word. If a minus sign is sensed, the end of the tape operation is signalled.

2.6.00 CORE MATRIX TRANSLATOR

A core matrix translator is used to translate the BCD tape code to the 2-out-of-5 code when reading from tape. The same cores are also used to translate the 2-out-of-5 code to the BCD code when writing on tape.

The translator is made up of a single plane core matrix which uses ~~105~~ 116 ribbon wound cores. ~~Eighty-four~~ 92 of these cores have a specific alpha, numeric, or special character designation (Figure 2.6-1). The remaining 21 cores are used for noise cancellation and error detection. A total of fifty drive and sense lines are threaded through the array with a maximum of twenty-eight lines through any one core.

The principle of operation is essentially one of negative logic. Instead of passing windings through a core which represents a character in the BCD code, windings representing the negative, or complement, value of a character are passed through the specified core.

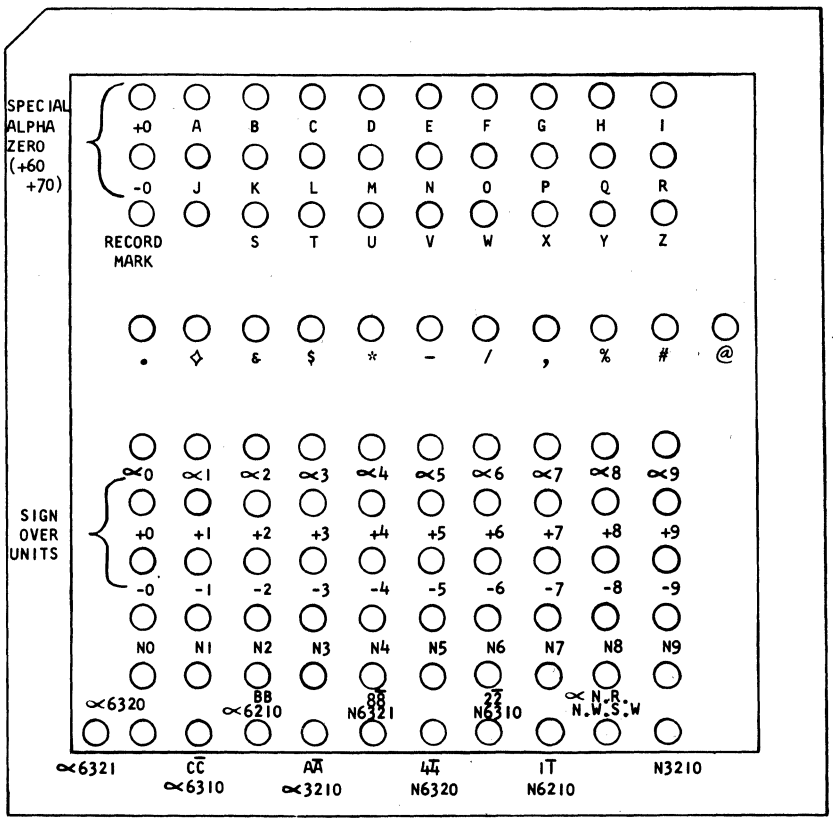


FIGURE 2.6-1. CORE MATRIX TRANSLATOR-CHARACTER LAYOUT

For example: The character A, in the BCD code is represented by a CBA $\overline{8}\ \overline{4}\ \overline{2}$ 1. The core which stores the character A has the negative information lines $\overline{CBA}$ 8 4 2 $\overline{1}$ passing through it.

Because the decimal equivalent for A is a 6 1 in the 2-out-of-5 code, four output sense windings are needed for the translation - the alpha 6 and 0 bits together with numeric 0 and 1 bits. Refer to Figure 2.6-2 for the schematic of the core and its windings.

The same character A core is used for the 2-out-of-5 to BCD translator. As mentioned previously the decimal equivalent for an A is 6 1. Because the principle of operation is negative logic, the alpha 3 2 1 and the numeric 6 3 2 are wound through this core.

The A designation in the BCD code is CBA 1; therefore, four output sense windings are used.

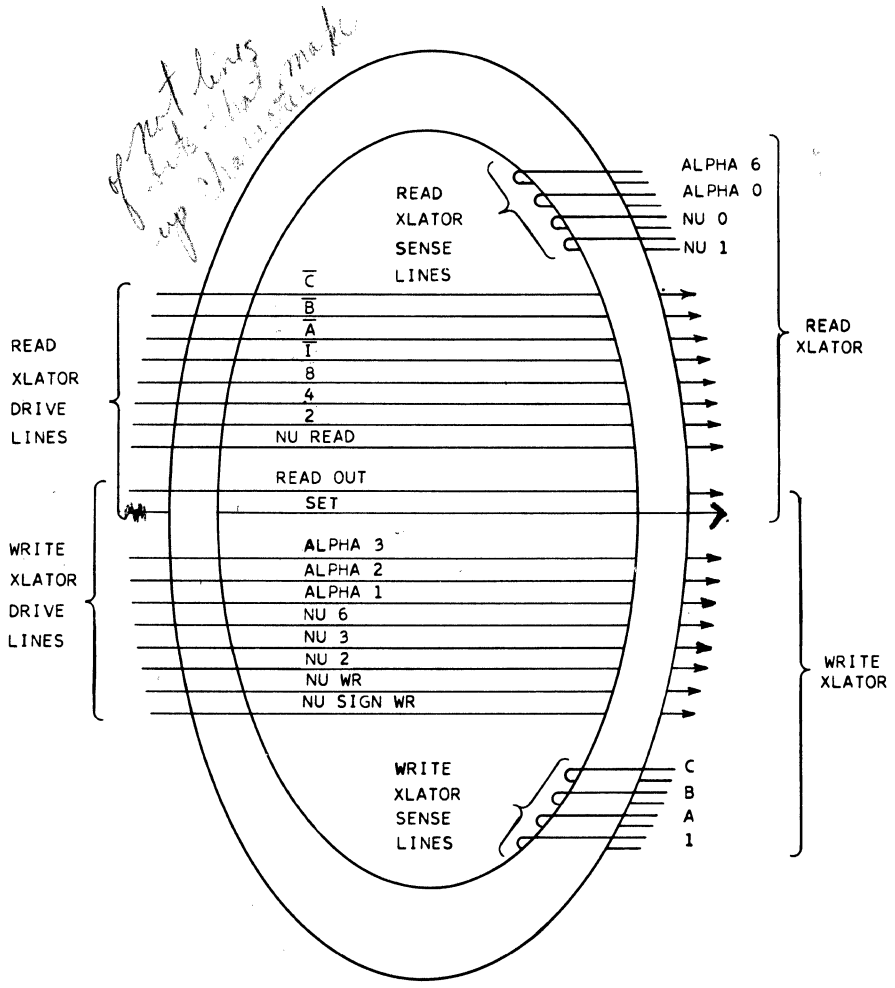


FIGURE 2.6-2. CHARACTER A WINDINGS

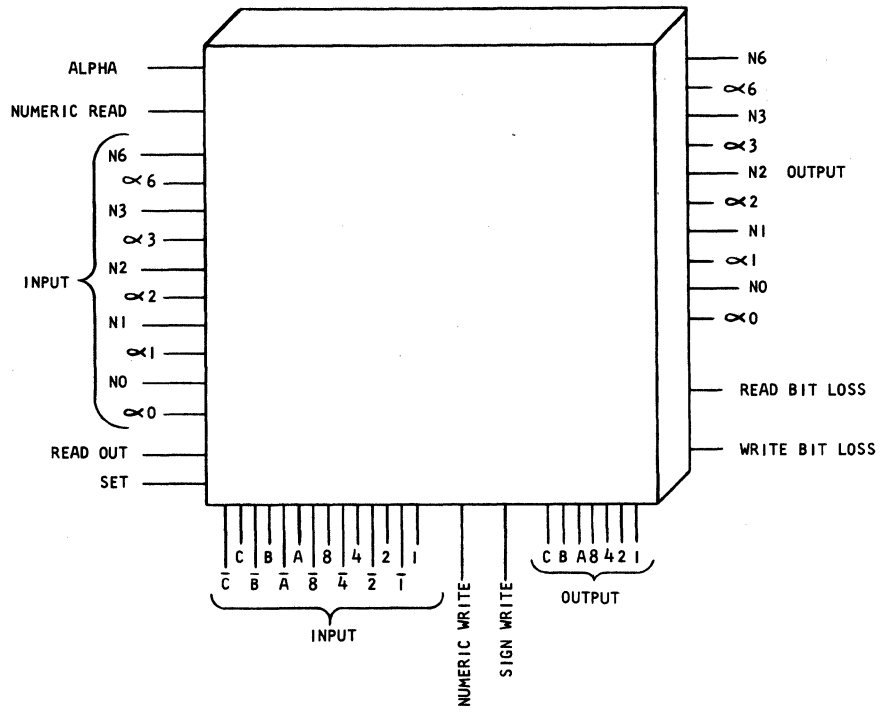


FIGURE 2.6-3. CORE MATRIX TRANSLATOR-DRIVE LINES

2.6.01 Control Windings (Figure 2.6-3)

In addition to the digit entries, six control windings are used to carry full current.

Set

The set control winding supplies full current, opposite in direction to the information windings, to all character cores. When the set current is applied, the selected core is switched to the one state.

Read-Out

The read-out control winding is laced through all cores in the same current direction as the information windings and is used to reset the selected core. When the selected core is reset the output is sensed.

Alpha Character

The alpha character control winding is laced through the sign cores, and the numeric cores to inhibit these positions during an alpha operation.

Read Numeric Control

The read numeric control winding is laced through the sign cores, special character, and alpha cores to inhibit these positions during a read numeric operation.

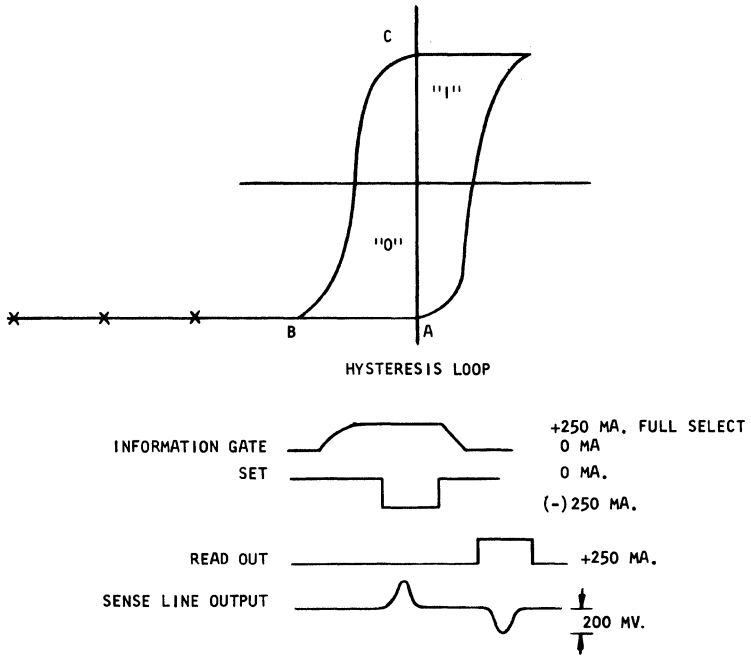


FIGURE 2.6-4. TRANSLATOR PULSE SEQUENCE

Write Numeric Control

The write numeric control winding is laced through the sign cores, special character, and alpha core to inhibit these positions during a write numeric operation.

Sign-Write

The sign-write control winding is laced through the alpha, numeric, and special character cores to inhibit these positions during a write sign operation.

2.6.02 Operating Examples

The translator operates in the following manner:

Prior to the use of the translator, all cores are reset to their 0 state (Refer to Figure 2.6-4, Point A on the Hysteresis loop).

When information is being read into the translator, each of the non-selected cores has at least one information line carrying full current through the core. Thus, each of the non-selected cores is further biased in the 0 state, as illustrated by the X marks on Figure 2.6-4.

As the information is read into the translator, a set pulse whose current is in the opposite direction to that of the information current is put through the array. When the set current is applied, those cores which are at point B are returned to point A at best. However, the selected core which remained at point A (Figure 2.6-4) due to the absence of any drive current is switched to point C on the hysteresis loop (one state).

During read-out time a full select current is supplied in the same direction as the information current. The read-out current causes the non-selected cores to be placed further into the 0 state. The selected core which is at point C of the loop is switched to point A (Figure 2.6-4) causing an output to be induced on the sense lines. At the end of read-out time all cores are back in their zero state.

2.6.03 Validity Check

The core translator checks the validity of the incoming information. It gives an error indication if any of the following conditions are sensed:

1. Loss of one or more bits (driver failure).
2. Gain of one or more bits.
3. Correct number of bits - invalid combination.

Loss of One or More Bits

The core translator has the ability to check for driver failures. This is accomplished by reserving eleven cores which are used to indicate a loss of one or more bits. Both the 2-out-of-5 and BCD code use the same core (Figure 2.6-1).

The loss of a bit in the BCD code is accomplished by threading a bit and a no bit winding through a core. For example: the C and $\overline{C}$ bit drive line is placed through a core. With one drive line conditioned, the core is placed further into the 0 state. At set time the core is prevented from setting.

However, if neither of the drive lines were conditioned, the core would be set indicating the loss of a bit. At read-out time the core would be reset and an output would be present on the driver failure sense winding indicating a bit loss.

Any combination of missing bits in the 2-out-of-5 code can be detected by the following combinations of bit windings:

6 3 2 1 -

6 3 2 - 0

6 3 - 1 0

6 - 2 1 0

- 3 2 1 0

There are two identical groups (10 cores): one for alpha, and the other for numeric word translation.

Assume a numeric 1 is read into the translator. This means that the 1-bit and 0-bit drivers would be in conduction, supplying full current. It can be seen from the preceding chart that each of the cores has the 1-bit or 0-bit winding passing through the core. This furnishes full current in each of these cores allowing it to be further biased into the 0 state. At set time none of the cores would be changed to the 1 state.

If only one driver was conducting, a missing-bit indication would be sensed. Assume that the 0-bit driver was not in conduction. It can be seen from the chart that only one group (6 3 2 - 0) would not have a winding supplying full current. At set time this core would be set to the 1 state and at read-out time a missing bit would be sensed.

Gain of One or More Bits

Because the logic of the translator is one of core elimination, only one core will remain un-biased when a character is read into the translator. Passing through the selected core is the control and bit drive lines which represent either the negative or the complement of the character. Thus, if a bit is gained, it will have to be one of the negative or complement drive lines, thereby furnishing full select current which in turn biases the selected core further into the 0 state.

When the set pulse is applied, the selected core will not be switched to the 1 state. At RO time none of the cores will be reset; therefore, no output will be available on the sense lines.

Correct Number of Bits - Invalid Combination

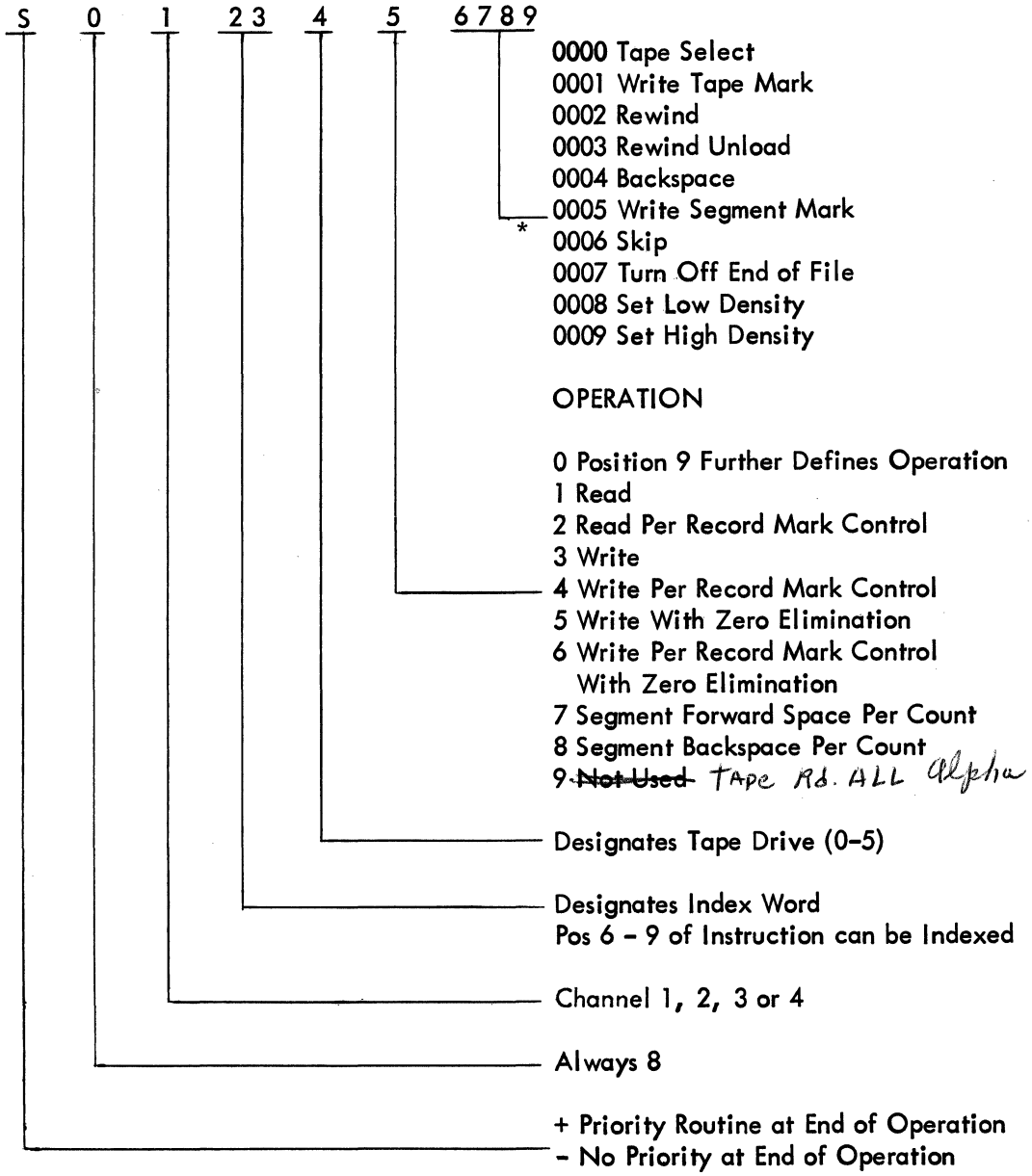
An error condition is sensed when the bits that are selected produce a combination which is different from any of the 84 code combinations. The translator will function in the same manner as when one or more bits were gained. The entire matrix will be biased further in the 0 state. When the set pulse is applied, none of the cores will be set; thus, at read-out time no output will be available on the sense lines.

When writing tape, the validity check in the TAU will indicate an error.

When reading tape, the validity check on the information bus will indicate the error.

3.0.00 INSTRUCTION EXECUTION

All tape instructions are specified by a ± 81 or ± 82 operation code. The format of the tape control instruction is as follows:



*Depends on whether a 0 is in position 5. If position 5 contains anything but 0, positions 6-9 are addresses of the record definition word that is to be used.

3.1.00 TAPE READ INSTRUCTIONS

The IBM 7070 tape system can scatter words read from tape into several core storage blocks. The number of words to be read from tape is controlled by the record definition register (start and stop registers). As the read operation progresses, the start address is updated each time the tape completely fills the buffer A register. The read operation continues until the start and stop addresses match. At this point the control word sign is analyzed to see if another record definition word is to be used. If the previous control word sign was plus, the address in the Control Register A specifies the location of the new record definition word which contains the next core storage that is to be used.

A second tape read instruction called Read Per Record Mark Control has been added to increase the scattering of the words read from tape. This is accomplished by having a second means of indicating a block of information. In previous discussions the end of a block has been indicated by the start and stop addresses becoming equal.

During a read-per-record-mark control operation the detection of a record mark in the low-order positions of the word (positions 8-9) automatically denotes the end of a core storage block. The sensing of the record mark has the same effect as the start and stop addresses becoming equal.

Prior to each word read in from tape, zeros are automatically inserted into the six low-order positions of the buffer A register. As the word is read from tape, the register is left-shifted, allowing the zeros to progress to the high-order positions of the buffer A register. An error is detected if more than 10 or fewer than 5 digits are read from a numeric tape.

All read operations start in alpha mode. The mode is changed to numeric by detection of the mode change character, which is also used to change from numeric to alpha.

3.1.01 Tape Read

As mentioned previously the read operation is performed in various cycles. Each of these cycles is used to request the use of memory and control the transfer of data to and from tape. The following objectives are accomplished during the read operation:

Analyze Tape Instruction

Perform Initial Status Word Cycle

Perform Control Word Cycle

Read A Tape Word

Perform Data Word Cycle

Sense End of Read Operation

Perform Final Status Word Cycle

Analyze Tape Instruction (Figure 3.1-1)

Each tape call is analyzed for a tape movement, or a tape read or write operation. The tape codes that are specified by a significant digit in position 5 of the tape instruction conditions the Decoder A latch. The Decoder A output along with a sample gate is used to develop the Field Register Op Sample and the Field Register Select Sample gates.

The field register op sample is gated with the static output of the field register units position to turn on the op register latches which determine the tape operation.

The field register select sample is gated with the static output of the field register tens position to turn on the select register latches. The output of these latches is used to select the tape drive.

When a tape call is sensed, the contents of the Program Reg D, I Counter and Op register are parallel transferred from A & P via the information bus to buffer B.

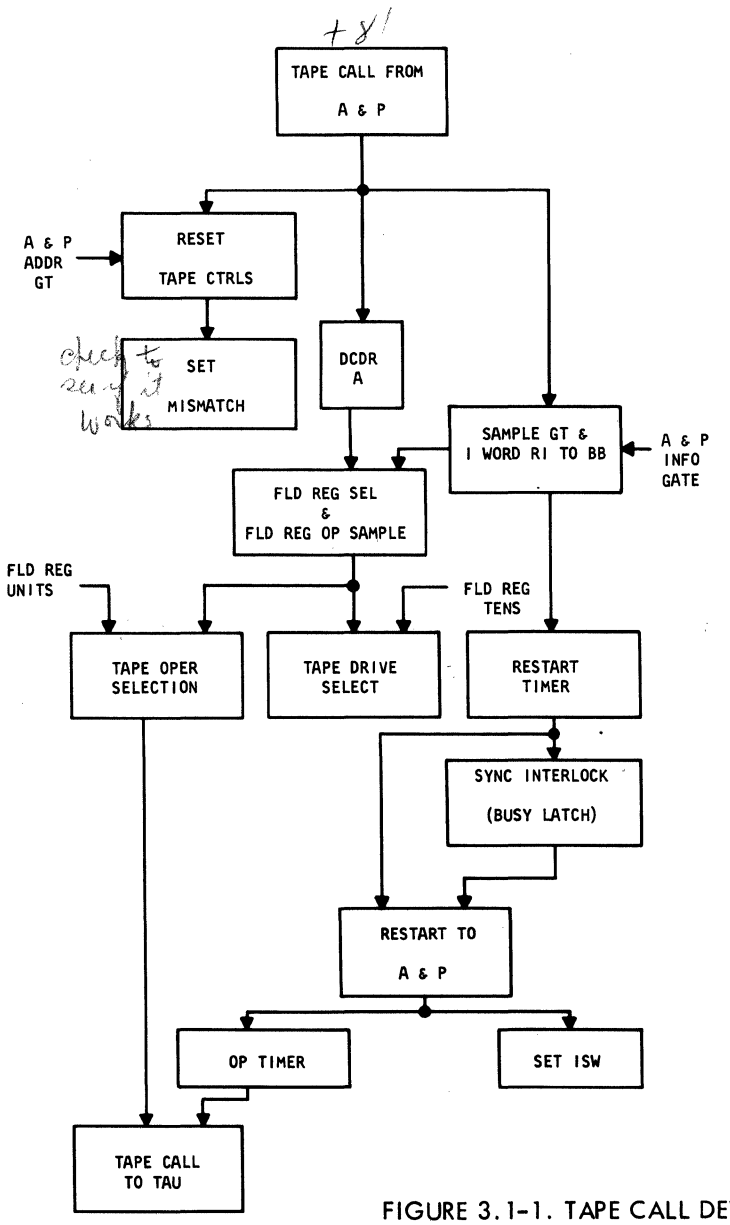


FIGURE 3.1-1. TAPE CALL DEVELOPMENT

With the op register and select register latches set, the restart timer latch is turned on. The restart timer output is used to develop the synchronizer interlock by turning on the Busy latch. With the synchronizer interlocked, a restart signal is developed to restart A & P.

The restart signal is also used to develop the Timer Op Gt and set the ISW command. The Timer Op Gate along with the static output of the Op Register latches develops the Tape Read Call, which is sent to TAU.

Command	Timing	Logic
Set Tape Call A	Fld Reg Non Zero Tape Call	5C-62.61.02
Set DCDR A	Tape Call A	3B-62.61.03
Set Status Word Gt	TP DCDR A	2C-62.61.18
Develop Channel Reset	Addr Gt, Any Call, No CE Op	4D-62.61.14
Reset Mis-match	Reset	65.51.43
Set Match Latch	Reset	65.51.43
I Word RI to BB	Info Gt, Any Call No CE Op	4B-62.61.04
Set Sample Gt	Info Gt, Any Call, No CE Op, X-Z	4B-62.61.04
Set Fld Reg Sel	Any TP DCDR, Sample Gt	4J-62.61.04
Set Fld Reg Op Spl	DCDR A or R, Sample Gt	4G-62.61.04
Set Restart Timer	Sample Gt, V-X	3A-62.61.05
Set Busy Latch	Restart Timer, Continue Sync Op, X-Z	2G-62.61.06
Set Restart Latch	Restart Timer, Busy, Z-V	3C-62.61.05
Set ISW	Status Word Gt, Any TP DCDR, Restart	5H-62.61.05
Set TMR Op Gt	Busy, Restart, V-X	3J-62.61.07
Develop Read Call	TMR Op Gt, Any TP Rd	4B-62.61.23

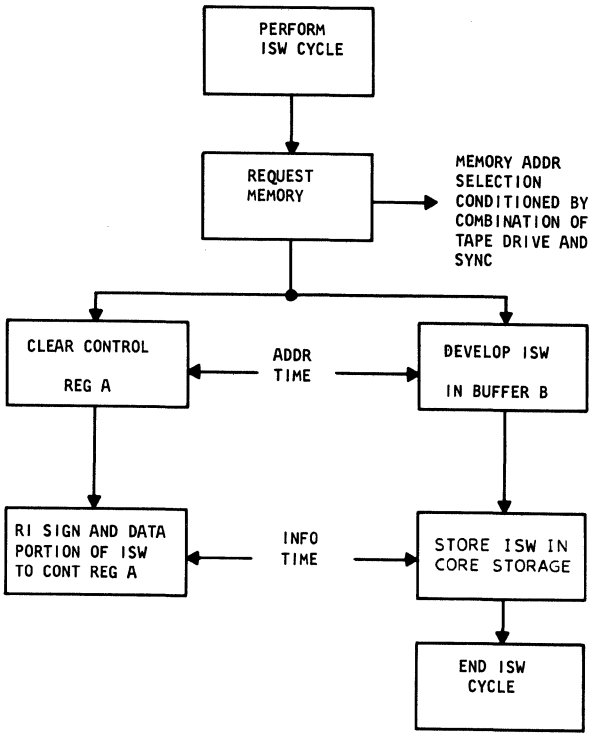


FIGURE 3.1-2. INITIAL STATUS WORD CYCLE

Perform Initial Status Word (Figures 3.1-2 and 3.1-3)

Every tape operation that might cause a priority signal when it is completed automatically creates an initial status word (ISW) at the beginning of each operation.

The function of the initial status word is to have a record of the type of tape operation that was performed and the location of the first record definition word that was used.

With A & P restarted and the specified synchronizer interlocked, the initial status word cycle is performed. The first step requests the use of memory to store the initial status word into the location specified by the addressed channel control unit and tape drive. When the priority control can accept the tape request, it replies in the form of an Addr Gt and an Info Gt.

These gates are used to condition the various controls needed to develop the initial status word in buffer B and to read out the four low-order positions of the buffer B register into the control register A.

As the ISW is parallel transferred to core storage via the Info Bus, the data portion (positions 6 - 9) and sing are read out to the Distributor Bus. If the sign is plus, the Interrupt Mode latch is turned on which signifies that an interrupt routine is to be performed at the completion of the operation. The occurrence of an error condition takes precedence over any other priority conditions that may exist.

The contents of positions 6 -9 contain the location of the first record definition word that is to be used. Because all tape read or write operations start in alpha, the alpha latch is set during the ISW cycle.

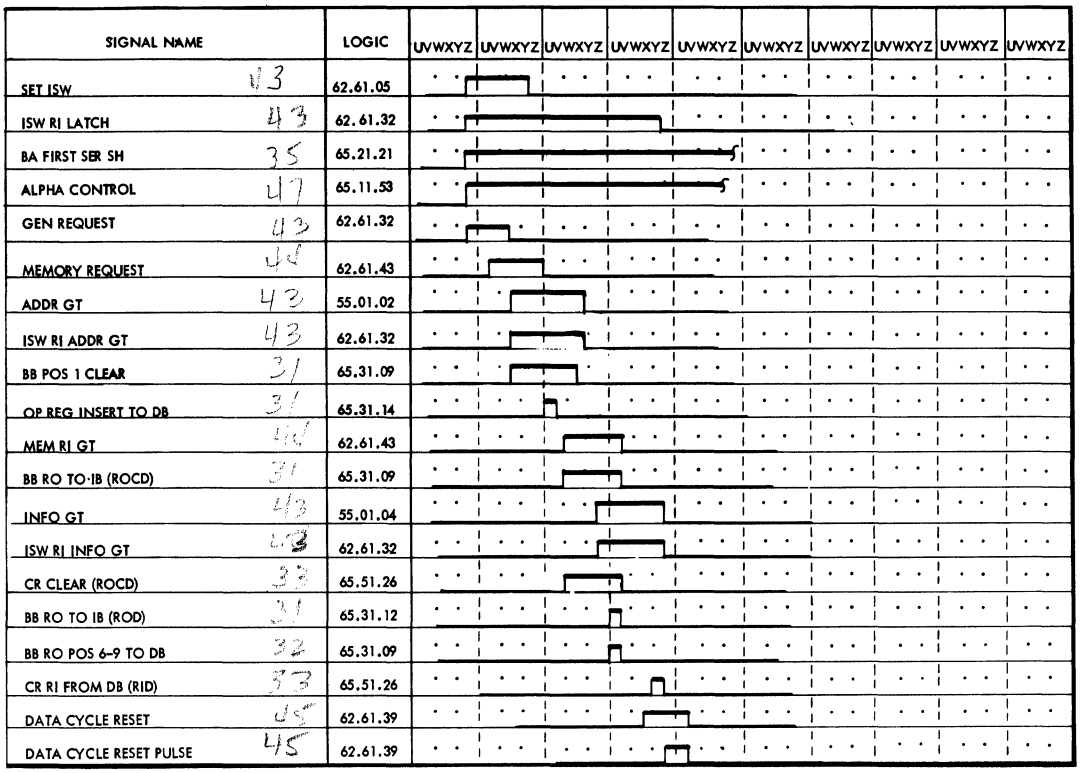


FIGURE 3.1-3. ISW CONTROL TIMING

Command	Timing	Logic
Set ISW	Restart, TP DCDR, Status Word Gt	5H-62.61.05
Set ISW RI Latch	Set ISW	3D-62.61.32
Request Memory	ISW RI Latch, No addr, No Info Gt	6G-62.61.32
Set Alpha Control	ISW RI Latch	3C-65.11.53
Insert Op Reg Bits	ISW RI Addr Gt	4D-65.31.09
Set Memory RI	ISW RI Addr Gt, No Mem Req, W - Y	2F-62.61.43
Clear Control Reg A	ISW RI, Mem RI	2D-65.51.26
BB RO to IB	Mem RI, U Time	6B-65.31.09
CR RI from DB	ISW RI Info Gt, Y Time	5E-65.51.26
Set Interrupt Mode	ISW RI Info Gt, SP 6 Bit and 3 Bit	3E-62.61.37
Data Cycle Reset	ISW RI Info Gt, X - Z	3E-62.61.39

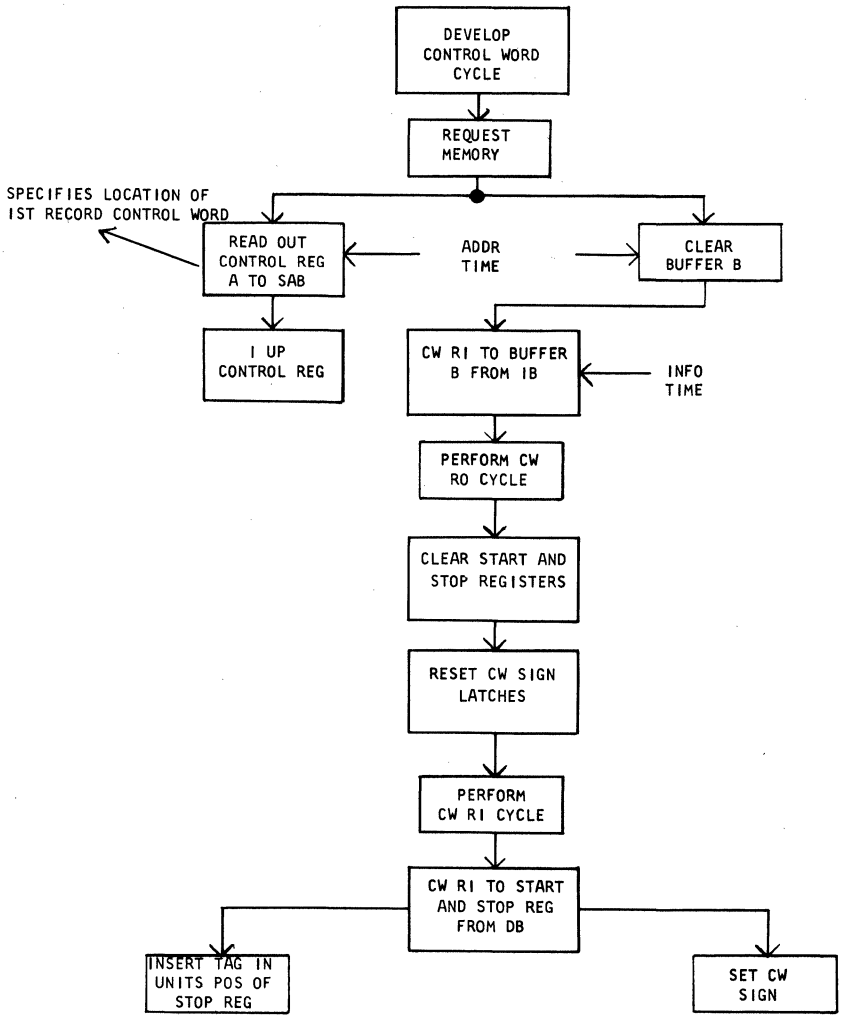


FIGURE 3.1-4. CONTROL WORD CYCLE

Perform Control Word Cycle (Figures 3.1-4 and 3.1-5)

To store the records being read in from tape, a control word cycle must be performed. The control word cycle is performed in two steps:

1. The CW Xfer RO step which conditions the record definition register to accept the control word.

2. The CW Xfer RI which transfers the control word from Buffer B to the record definition register.

When a set control word signal is developed, a memory request is made to read out a control word from core storage. When the core storage priority controls accept the tape request, it replies in the form of an Addr Gate and an Info Gate.

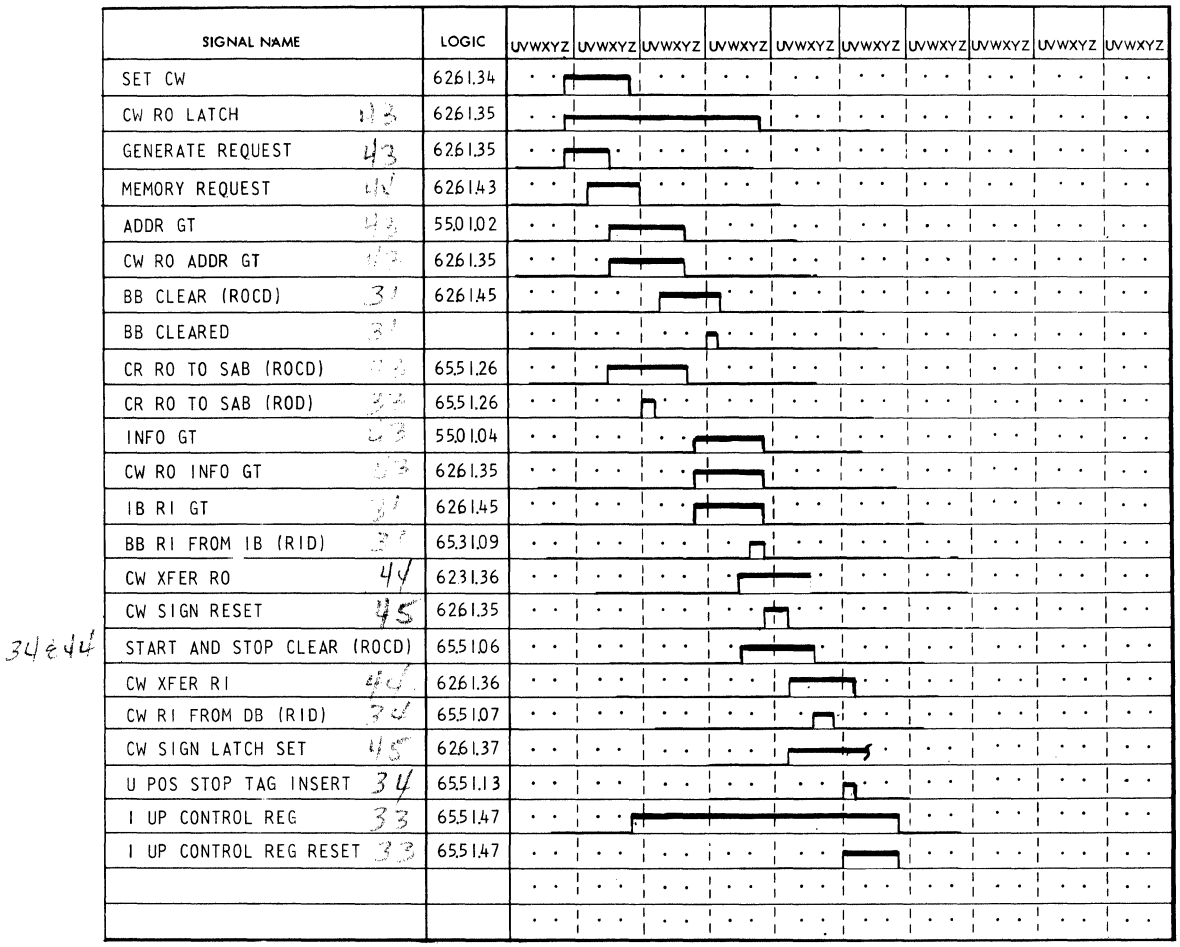


FIGURE 3.1-5. CONTROL WORD TIMING

During Addr Gate time, the contents of the control register A are read out to the Sync Addr Bus to condition the core storage location which contains the control word. Buffer B is cleared at this time to accept the control word when it is read out of core storage.

With the core storage address triggers conditioned to read out the control word, the control register A address is increased by one. The 1-upping of the control register is performed in the same manner for both the read and write operations.

At Info Gate time the control word is read out of its core storage location and placed into buffer B.

With the control word in buffer B, the CW Xfer RO signal is developed. This signal clears the Start and Stop Reg and resets the CW sign latches.

With the Xfer controls conditioned, the CW Xfer RI signal is developed which transfers the contents of buffer B to the start and stop register and inserts the stop tag into the units position of the stop register. As the contents of buffer B is placed onto the distributor bus, the sign is sampled to set either the CW minus or CW plus latch.

Command	Timing	Logic
Set CW RO	ISW RI Info Gt	3D-62.61.34
Set CW RO Latch	Set CW RO	4B-62.61.35
Request Memory	CW RO Latch, No Addr, No Info Gt	6C-62.61.35
Set CW RO Addr Gt	CW RO Latch, Addr Gt	4E-62.61.35
CR RO to SAB	CW RO Latch, Addr Gt	4C-62.61.35
1 Up Control Reg	CW RO Latch, Addr Gt, Z - V	65.51.47
Clear Buffer B	CW RO Addr Gt, W - Y	2B-62.61.45
Set CW RO Info Gt	CW RO Latch. Info Gt	4F-62.61.35
Set IB RI Gt	CW RO Info Gt	4F-62.61.45
Set CW Xfer RO	CW RO Info Gt, X - Z	2C-62.61.36
BB RI from IB	IB RI Gt, No CE Op, Y Pulse	2F-65.31.09
Clear Start and Stop Reg	CW Xfer RO	3H-65.51.06
Set CW Xfer RI	CW Xfer RO, V - X	2F-62.61.36
CW Sign Set	CW Xfer RI, No CE Op, SP Bits	4B-4D-62.61.37
CW RI from DB	CW Xfer RI, Y Pulse	4B-65.51.07
Insert Stop Tag	CW Xfer RI, Op	5J-65.51.13
Set 1 up Cont Reg Reset	1 Up CR, Stop Tag U, No SSR	65.51.47

Read a Tape Word (Figure 3.1-6)

Because the tape channel can be used with different speed tape drives, the channel control unit is designed to operate under control of the TAU unit. To insure that the characters read from tape are translated and stored into the buffer A register, three read start latches are used (R Stt 1, 2 and 3).

Each time a character is sensed from tape, one of these latches is turned on. The output of the latch, in turn, conditions the tape translator and controls the advance of the buffer A register.

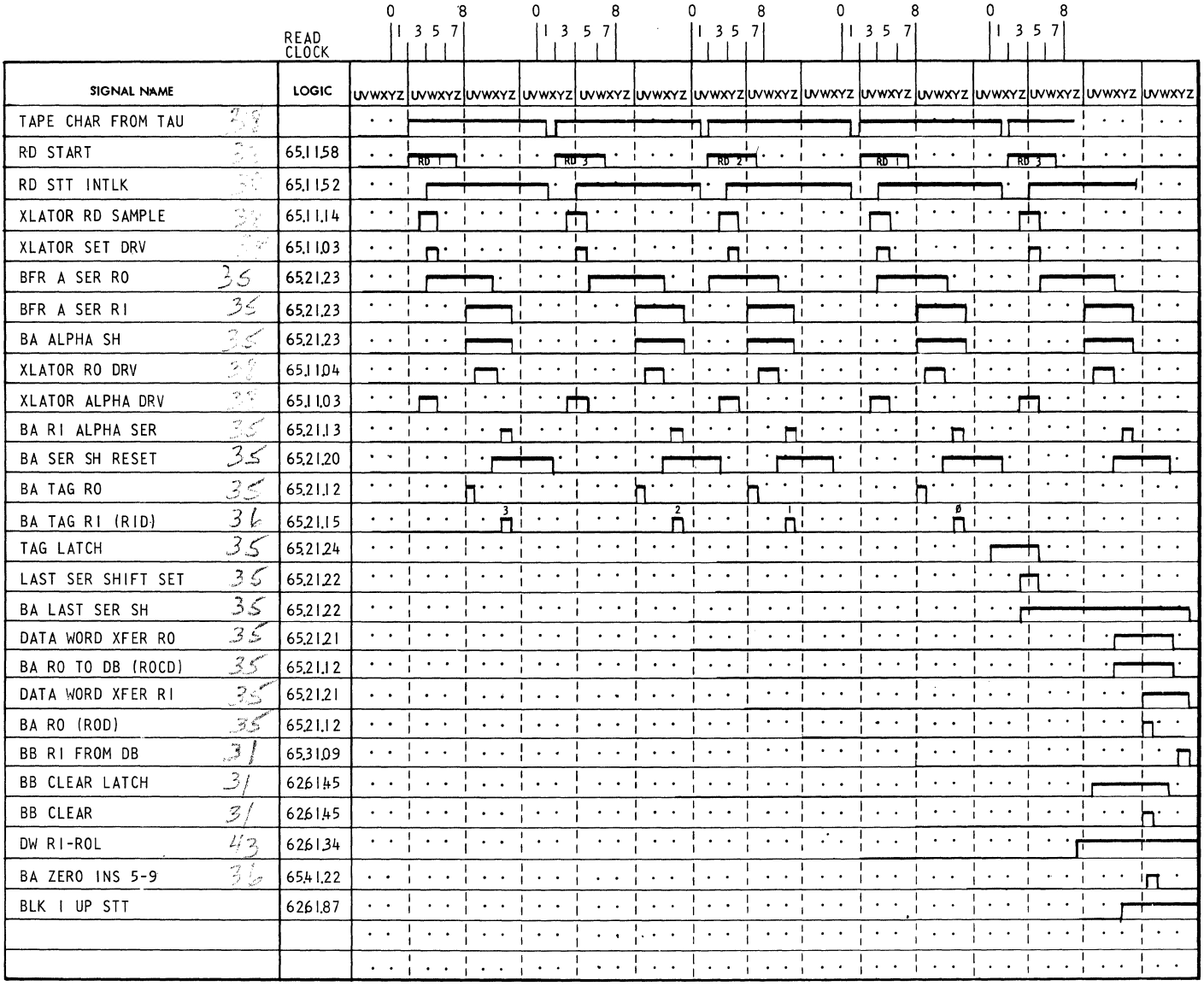


FIGURE 3.1-6. READ-ALPHA WORD

During a numeric read operation, the sign over units signifies that the register has received a complete word from tape. For an alpha read operation the sensing of the alpha tag signifies a complete alpha word.

For the following explanation assume an alpha character is read in from tape every 16 usec.

Whenever a bit is sensed from TAU, an Enable Rd Stt signal is developed which turns on a read start control latch. With a read start latch turned on, a Translator Rd Sample Pulse is developed to gate the alpha character into the read translator.

The Rd Stt latch output is also switched with alpha control to develop the Translator Alpha Drive. This drive line inhibits the numeric and special character cores.

To set the core which represents the alpha character sensed from tape, the translator set drive must be brought up. For further information on the translator refer to section 2.6.00 of the Tape Control Manual.

The read start control latch is used to set the BA controls which cause the buffer A register to accept the alpha digit when it is read out of the translator.

With the BA controls conditioned, the Bfr A Ser RI latch output conditions the Translator RO Driver to read out the alpha character to a bit insert driver (BID). The BID charges the capacitors for both the numeric and alpha portion of the character. The following Y-time, the capacitors are discharged, which causes the alpha character to be read into the buffer A register (positions 8 and 9).

This operation is repeated for every alpha digit that is read from tape. As the alpha characters are read into buffer A, the tag is advanced a digit position at a time. Because the alpha word takes only five left-shifts to fill the register, the tag is inserted into the capacitor of position 4 of the tag register. The first left-shift reads the tag into position 3. The end of the alpha transfer is determined when the tag is read out of position 1. At this point the BA Tag Hold latch is turned on which signifies that one more left-shift is needed.

Prior to reading the last alpha character into buffer A, buffer B is cleared. As the last character is read into buffer A, a Data Word Xfer RO Gate is brought up, which transfers the contents of BA to BB via the distributor bus.

During DW Xfer RO, the block 1-up start latch is turned on. This latch insures that the start address remains as the last effective start address in the event of a short length record.

With the transfer of BA to BB completed, zeros are automatically added to the six low-order positions of buffer A to condition BA for the next word that is to be read from tape.

Sense First Alpha Character

Command	Timing	Logic
Set Enable Rd Stt	Any TP Bit, No Rd Stt Intlk, No BA Ser RO-RI	5E-65.11.57
Set Read Start 1	No Rd Stt 3, No Rd Stt 2, Enable Rd Stt, UP	3A-65.11.58
Set Xlator Rd Sample	Rd Stt 1, V - X	3A-65.11.14
Set Xlator Alpha Drive	Xlator Rd Sample, Alpha Ctrl	3A-65.11.03
Xlator Set Drive	Rd Stt 1, WP	3F-65.11.03
Set Rd Stt Intlk	Rd Stt 1, WP	2C-65.11.52
Set Bfr A Ser RO	Rd Stt 1, W - Y	2B-65.21.20

Command	Timing	Logic
Set Bfr A ser RI	No Rd Stt 3, U - W, Bfr A Ser RO	4D-65.21.20
Set Xlator RO Drive	Bfr A Ser RI, TP Rd, No Mode Change, V - X	3E-65.11.04
Set BA Alpha Shift	Bfr A Ser RI, Alpha Ctrl, Any TP DCDR, No Mode Change	5C-65.21.23
Set Rd Xlator BA Sample	Bfr A Ser RI, Any TP Read, V - X, No Mode Change	2H-65.11.30
BA RI Alpha Serial	BA Alpha Shift, YP	4E-65.21.13
Set Bfr A Ser Sh Reset	BA Ser RI, X - Z	4H-65.21.20

Sense Last Alpha Character

Command	Timing	Logic
Set BA Tag Hold	BA Tag, W - Y	3G-65.21.24
Set BA Last Ser Sh	BA Tag Hold, Z - V	3D-65.21.22
Set Enable Rd Stt	Any TP Bit, No Bfr A Ser RO or RI, No Rd Stt Intlk	5E-65.11.57
Set Rd Stt 3	No RD Stt 1 or 2, YP, Enable Rd Stt	3A-65.11.60
Set Xlator Rd Sample	Rd Stt 3, Z - V	3D-65.11.14
Set Xlator Alpha Drive	Xlator Rd Sample 3, Alpha Ctrl	3A-65.11.03
Xlator Set Drive	Rd Stt 3 Latch	3F-65.11.03
Set Rd Stt Intlk	Rd Stt 3, UP	2E-65.11.52
Set Bfr A Ser RO	Rd Stt 3, V - X	2D-65.21.20
Clear Buffer B	BA Last Ser Shift, BA Ser RO, Rd Ctrl	4C-62.61.45
Set Bfr A Ser RI	No Rd Stt 3, U - W, Bfr A Ser RO	4D-65.21.20

Command	Timing	Logic
Set BA Alpha Shift	Bfr A Ser RI, Alpha Ctrl, Any TP DCDR, No Mode Change	5C-65.21.23
Set Xlator RO Drive	Bfr A Ser RI, TP Rd, No Mode Change, V - X	3E-65.11.04
Data Word Xfer RO	Bfr A Ser RI, W - Y BA Last Ser Sh	3C-65.21.21.
Set BLK 1 Up Stt	CW Xfer RO, Z - V	4A-62.61.87
BA RO to DB	Read Control, Data Word Xfer RO	3C-65.21.27
Data Word Xfer RI	Data Word Xfer RO, U - W	3E-65.21.21
BA 0 Ins Posn 4 - 9	Data Word Xfer RI, TP Rd	3B-65.41.22

Perform Data Word Cycle (Figures 3.1-7 and 3.1-8)

The data word cycle is used to store the tape word into the core storage location specified by the address in the start register. As the last character is being read into buffer A from tape, a Set DATA CW RI-RO signal is developed. With the DW RI-RO latch turned on, a memory request is made.

With memory requested and the last character read into BA, the contents of BA is transferred to BB via the distributor bus. Prior to reading into buffer B the register must be cleared. As soon as the contents of BA is transferred to buffer B, zeros are inserted into the ~~five~~ six low-order positions of the buffer A register.

When the core storage controls accept the tape request, it replies in the form of an Addr Gt and an Info Gt.

At Address Gate time, the contents of the start register is read out to the Sync Addr Bus to condition the core storage location into which the tape word is to be stored. With the core storage location conditioned, the contents of the start register is 1-upped and compared, providing a mismatch had been developed from the last compare operation.

During Addr Gate time, the Memory RI latch is turned on to condition the Buffer B ROCD. With the ROCD conditioned, the contents of buffer B is read out to the information bus the following U-time.

With the tape word stored in core storage, the DW Cycle Reset latch is turned on during Info Gt time to reset the DW RI controls.

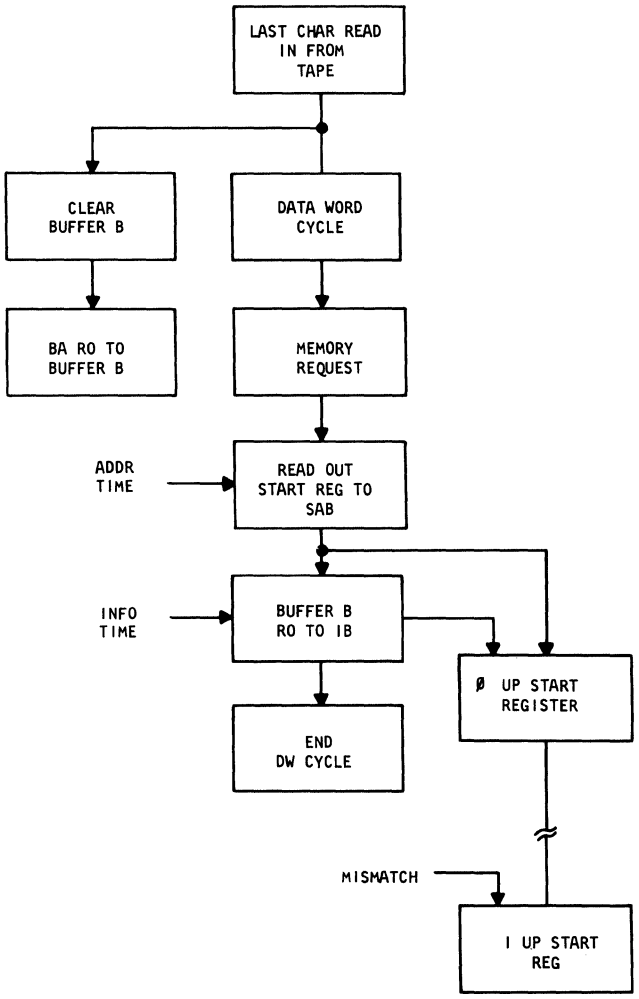


FIGURE 3.1-7. DATA WORD CYCLE (READ)

Command	Timing	Logic
Set DW RI-RO	BA Last Ser Sh. Z - V, BA Ser RO, Read Ctrl, No Info Stop	5H-62.61.34
Set DW RI-RO Latch	DW RI-RO	3A-62.61.38
Request Memory	DW RI-RO Latch, No SSR, No Addr Gt, No Info Gt	6C-62.61.38
Set DW RI Addr Gt	DW RI-RO Latch, Read Ctrl, Addr Gt	4F-62.61.38
RO Stt Reg to SAB	DW RI-RO Latch, Addr Gt	3D-65.51.06
Set Memory RI	DW RI Addr Gt, No Mem Req, W - Y	2H-62.61.43

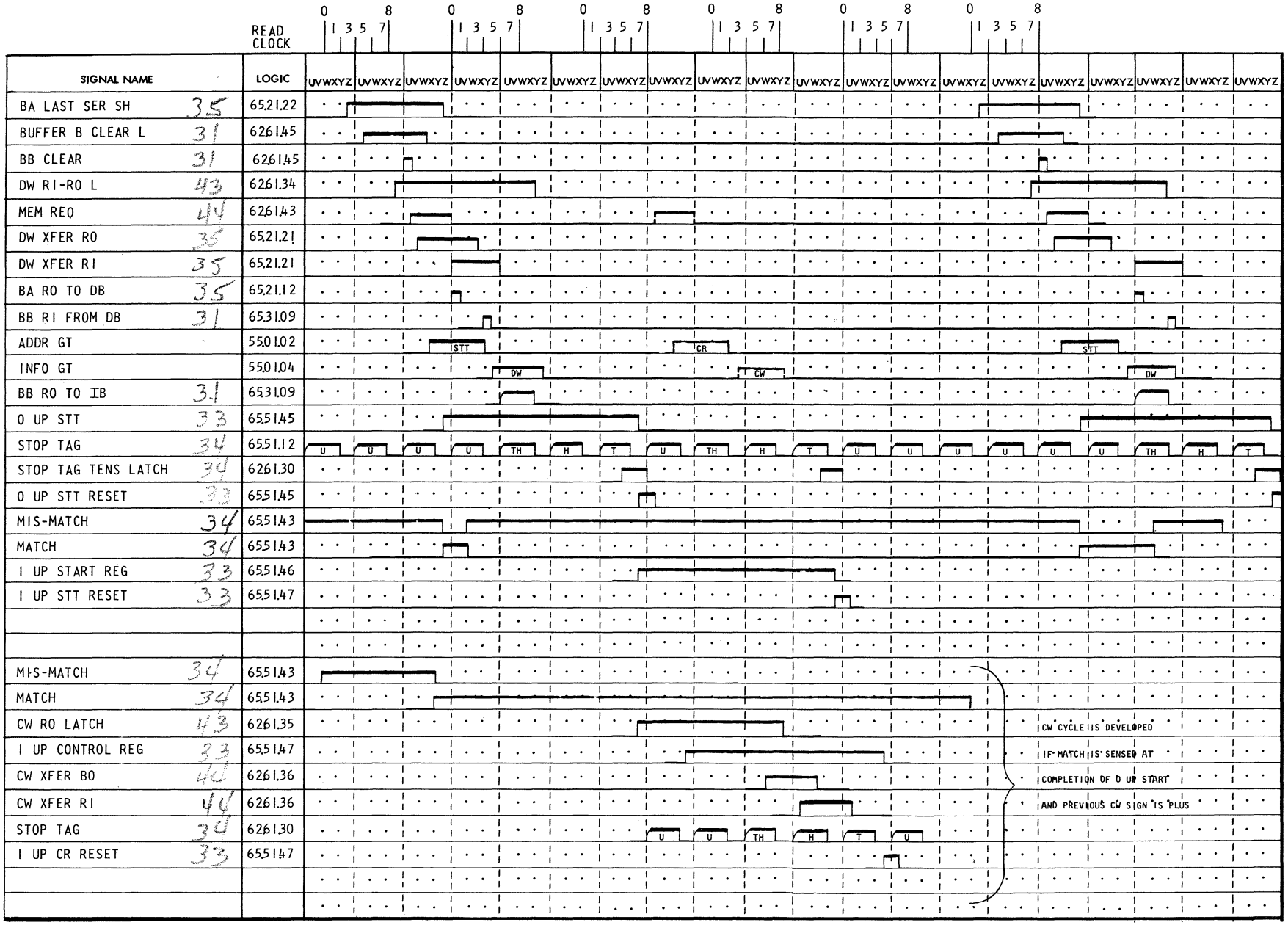


FIGURE 3.1-8. READ OPERATION-DATA WORD TIMING

Set BB RO to IB	Memory RI GT	3C-65.31.09
Set DW RI Info GT	DW RI-RO Latch, Read Ctrl, Info Gt	4H-62.61.38
Set Data Cycle Reset	DW RI Info Gt, X - Z	3E-62.61.38

Perform 0-Up and 1-Up Operation

With the core storage address selection triggers conditioned to read in the data word, the 0-up start latch is conditioned. The 0-up start operation causes both the start and stop registers to advance a digit at a time through the match circuitry to determine a match or mismatch condition.

At the completion of the 0-up operation, if a mismatch condition is present, the 1-up start latch is turned on to increase the start address by one. The adding of one develops the address of the next location that is to be used to store the next word read from tape. This operation continues until a match condition is sensed at the completion of the 0-up operation.

With a match condition sensed, the control word sign is analyzed to determine if a control word is needed or the end of operation is to be signalled.

Command	Timing	Logic
Set 0-Up Start	DW RI-RO Latch, No 1-Up CR Gate, Addr Gt, Z - V	65.51.45
Develop Start Serial Shift Right	0-Up Start	65.51.45
Advance Start Reg (ROD)	Stt-Stop RO, UP	65.51.06
Advance Stop Reg (ROD)	Stt-Stop RO, UP	65.51.15
Start RI Serial (RID)	Start Serial Shift Right, Y - P	65.51.07
Stop RI Serial (RID)	Start Serial Shift Right, Y - P	65.51.15
Rest 0-Up Start	0-Up Start Latch, Stop Tag Tens	65.51.45
Set 1-Up Start	0-Up Start, Z - V, Mismatch, No Blk 1 Up Stt	65.51.46
Develop Start Serial Shift Right	1-Up Start	65.51.45
Set 1-Up Start Reset	Stop Tag Tens, 1-Up Start, No 0-Up Start Reset	65.51.46

Request a Control Word

During the storing of each tape word in core storage, the match circuit output and the control word sign are analyzed to see if a CW cycle is to be performed. If a match signal and a plus control word are sensed, a control-word cycle is performed.

The control-word cycle requests the use of memory to read out a new control word into the record definition register. The tape drive continues to read the records from tape; however these records will be stored in a different core storage block specified by the new addresses in the Start and Stop registers.

Command	Timing	Logic
Set CW RO	Match, CW Plus, 0 Up Reset	62.61.34

Sense End of Read Operation

The end-of-a-read operation is determined when the start and stop register contents match, and the control word sign is minus. When these conditions exist, and the last word read from tape is stored in buffer B, the end-of-record delay latch is turned on. The output of this latch is used to reset the condition 3 latch (SLR).

With the EOR delay latch on, the tape channel control unit waits for the tape adapter unit to furnish a read disconnect delay 36 signal. The RDD 36 signal indicates that the last character of a record has been read. The RDD 36 signal is used to set the condition 2 latch (Correct Length Record).

When the tape drive is disconnected and the LRCR is sampled for an error, a Read Disconnect 136 signal is developed. This signal is used to develop a Set Final Status Word Signal.

If an additional tape word is read from tape after the end-of-record latch is set, the condition 4 latch is turned on. This signifies a long length record. With the condition 4 latch turned on, the Info Stop latch is brought up to inhibit these words from being stored in core storage.

Command	Timing	Logic
Set EOR Delay	CW Minus, No Seq A or B Rec Mk Match, DW Xfer RI, No SSR Gt	3C-62.61.70
Reset Cond 3 Latch	EOR Delay, Any TP DCDR	3C-62.61.86
Set Cond 2 Latch (Set R/W Clear)	EOR Delay, RDD 36, Read Ctrl	5D-62.61.70
Set Final Status Word	RDD 136, No Blk Cnt Ctrl	4B-62.61.07

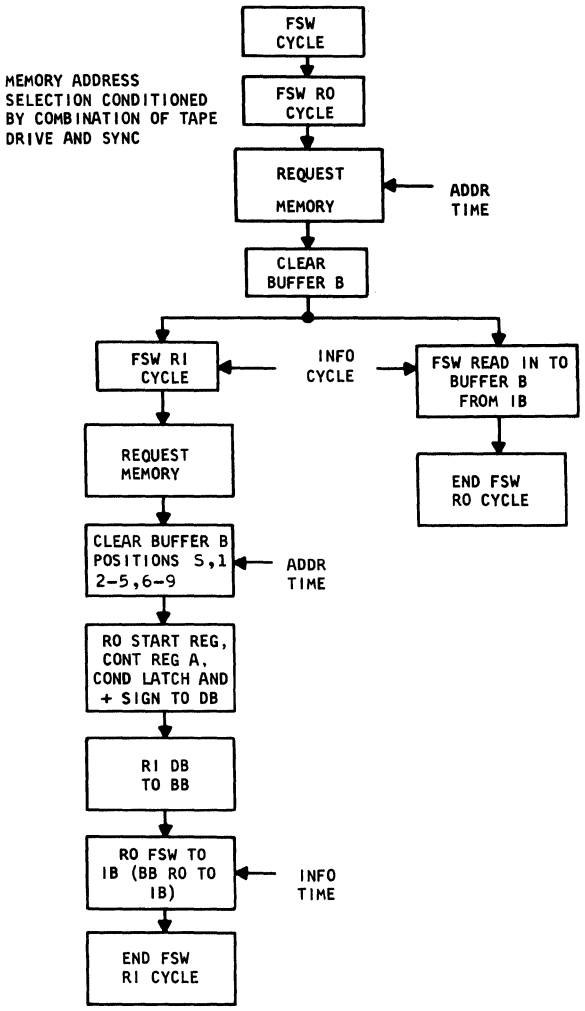


FIGURE 3.1-9. FINAL STATUS WORD CYCLE

Perform Final Status Word Cycle (Figures 3.1-9 and 3.1-10)

The final status words are automatically developed at the conclusion of each tape read or write operation. The final status word is performed in a two-step operation: Final Status Word Read-Out, and Final Status Word Read-In.

The final status word read-out operation requests a memory cycle to read out the final status word. The core storage location is specified by the addressed combination of tape drive and tape channel control unit.

With the final status word transferred to buffer B, the FSW RI operation is performed. During this operation a memory request is made to store the final status word back into its prescribed core storage location.

When core storage replies in the form of an addr gate, the following positions of buffer B are cleared: sign, 1, 2 - 5, and 6 - 9. With these positions cleared the contents of the start register, control register A, condition latch output and a plus sign are placed onto the distributor bus. The following read-in time (Y-time) the contents on the distributor bus is read into buffer B.

SIGNAL NAME		LOGIC	UVWXYZ	UVWXYZ	UVWXYZ	UVWXYZ	UVWXYZ	UVWXYZ	UVWXYZ	UVWXYZ	UVWXYZ	UVWXYZ
SET FSW	42	6261.07										
FSW RO LATCH	43	6261.40										
GEN REQUEST	43	6261.40										
MEMORY REQUEST	44	6261.43										
ADDR GT	43	5501.02										
FSW RO ADDR GT	43	6261.40										
BB CLEAR (ROCD)	31	6261.45										
BB CLEAR (ROD)	31	6261.45										
INFO GT	43	5501.04										
FSW RO INFO GT	43	6261.40										
IB RI GATE	31	6261.45										
BB RI FROM IB	31	6531.09										
FSW RI LATCH	43	6261.41										
RO CYCLE RESET LATCH	45	6261.39										
RO CYCLE RESET PULSE	45	6261.39										
FSW RI ADDR GT	43	6261.41										
MEM RI GATE	44	6261.43										
COND LATCH AND +SIGN INSERT TO DB	31	6261.46										
STT AND CR RO TO DB (ROCD)	34 & 33	6551.06										
STT AND CR RO TO DB (ROD)	34 & 33	6551.06										
BB REGEN (RID)	31	6261.45										
BB RO TO IB (ROCD)	31	6531.09										
BB RO TO IB (ROD)	31	6531.09										
FSW RI INFO GT	43	6261.41										
DATA CYCLE LATCH	45	6261.39										
DATA CYCLE RESET	45	6261.39										

FIGURE 3.1-10. FSW CONTROL TIMING

During Info Gate time, the contents of buffer B is transferred back into the specified FSW core storage location.

With the FSW stored, the tape call signal to TAU is dropped, and an interrupt signal is developed, if the interrupt latch was turned on. The interrupt latch could be turned on at the beginning of a tape operation, or if an error condition had been detected during the tape operation. If an interrupt routine is to be performed, an interrupt signal is developed to turn on the stacking latch located in the core storage control unit (7602).

Before the synchronizer interlock can be released, an interrupt reply signal is sent back from the 7602, which signifies that the stacking latch has been set.

Command	Timing	Logic
Set FSW	RDD 136, No Blk Cnt Ctrl	4B-62.61.07
Set FSW RO Latch	Set FSW	4B-62.61.40
Request Memory	FSW RO Latch, No Addr, No Info, V - X	2B-62.61.43
Set FSW RO Addr Gt	FSW RO Latch, Addr Gt	5E-62.61.40
Clear Buffer B	FSW RO Addr Gt, W - Y	2D-62.61.45
Set FSW RO Info Gt	FSW RO Latch, Info Gt	6F-62.61.45
RI FSW to BB	IB RI Gt, YP	6F-65.31.09
Set RO Cycle Reset	FSW RO Info Gt, X - Z	3E-62.61.39
Set FSW RI Latch	FSW RO Info Gt	3B-62.61.41
Request Memory	FSW RI Latch, No Info Gt, No Addr Gt	6F-62.61.41
Clear Buffer B (Except Pos 0)	FSW RI Addr Gt	4A, 4D, 4F-65.31.09
Set FSW RI Addr Gt	FSW RI Latch, Addr Gt	4H-62.61.41
RO CR and Stt Reg to DB	FSW RI Latch, Addr Gt DCDR A	3F-65.51.06
Set FSW Insert Gt	FSW RI, Addr Gt	2B-62.61.46
Set Memory RI	FSW RI Latch, Addr Gt, No Mem Req, W - Y	2G-62.61.43
BB RO to IB (ROCD)	Mem RI Gt	5B-65.31.09
Set FSW RI Info Gt	FSW RI Latch, Info Gt	4G-62.61.41
Set Op Reset	FSW RI Info Gt, Status Word, V - X	4C-62.61.73
Develop Interrupt	Intr Mode Latch, Status Word Gt, FSW RI Info Gt, V - X	5F-62.61.73
Set Op Reset Tmr	End Op Reset, Status Word Gt, Z - V	4E-62.61.74
Reset Busy	Intr Reply, Op Reset Tmr, Inter Mode, Any TP DCDR, X-Z, No Hang Up ERR	3B-3C-5C-6C 62.62.06

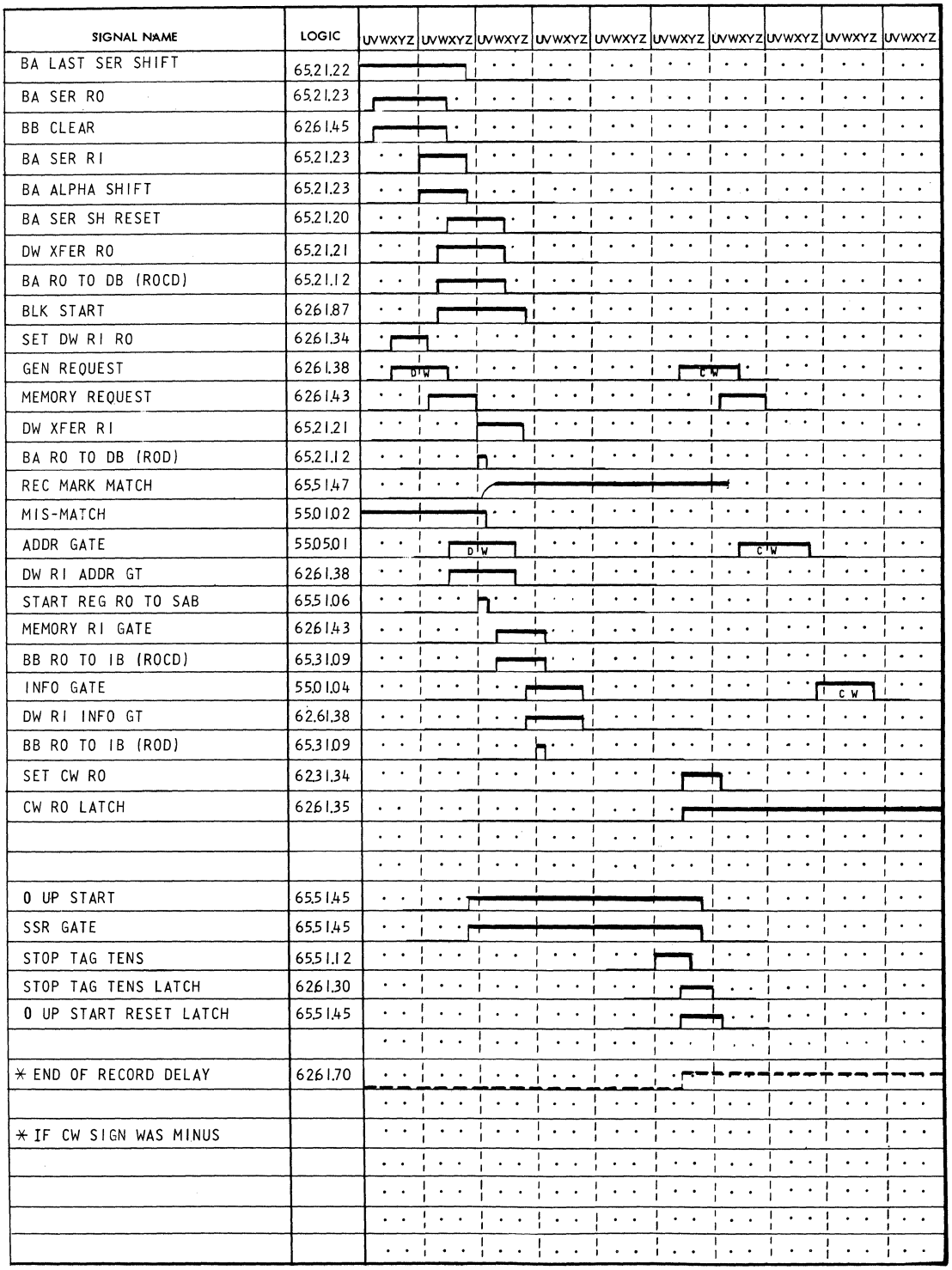


FIGURE 3.1-11. READ-PER-RECORD-MARK CONTROL

3.1.02 Read Per Record Mark Control (Figure 3.1-11)

During the read-per-record-mark control operation, the tape unit reads the words into core storage in accordance with the record definition register. Detection of the record mark word automatically denotes the end of a core storage blcok and has the same effect as the start and stop addresses becoming equal.

When a record mark is sensed, a new control word is read into the record definition register providing the sign of the previous control word was plus. If a minus sign is sensed, the read operation is completed, and the channel interlock is released.

To perform the read-per-record-mark operation, the word must be alphabetic, and the record mark must be in the low-order positions of the word (positions 8 - 9). With the record mark in any other position of the word, it is read as any other alpha character.

The initial status word, control word, data word and the final status word are performed in the same manner as explained under the alpha read operation. The following explanation deals with the controls that are affected by the sensing of a record mark.

As the last character is read into buffer A, a data word request is made to store the word read from tape. When the contents of BA is transferred to buffer B, via the distributor bus, the low-order positions of the word are sampled for an alpha 80's code.

When an alpha 80's code is sensed, the record mark latch is turned on and is used to reset the mismatch latch that was turned on at the beginning of the operation.

When core storage replies in the form of an address gate and an information gate, the data-word cycle is performed to store the word containing the record mark. This word is the last word stored into the core storage block.

During DW RI Addr Gate time, the 0-up latch is turned on to perform a 0-up start operation. If, during the 0-up operation, a mismatch is sensed, the record mark signal prevents the mismatch latch from turning on. At the completion of the 0-up operation, the previous control word sign is analyzed. If a plus sign is sensed, a memory request is initiated to perform a control-word cycle which places a new control word into the record definition register.

As the data word cycle and control word cycle are being performed, the tape drive continues to read into buffer A. However, this word is stored into the new core storage block. The read operation continues to fill the core storage block until another record mark is sensed, or the start and stop addresses become equal.

If the previous control word sign was minus when a record mark was sensed, the end-of-record delay latch would be turned on which signifies the end of a read operation (Figure 3.1-11).

Command	Timing	Logic
Sense Record Mrk	8 pos 6 and 2 Bit, 9 pos 2 and 1 Bit, SP 3 and 0 Bit, Rec Mk Ctrl	3B-65.51.47
Reset Mismatch Latch	Record Mark Latch	4D-65.51.43
Set Match Latch	Record Mark Latch	65.51.43
Set DW.RI RO	BA Ser RO L, BA Last Ser Shift, Read Ctrl, No Info Stop	62.61.34
Set 0-Up Start	DW RI-RO L, Addr Gt, Z - V	65.51.45
Set 0-Up Start Reset	Stop Tag Tens, 0-Up Start	62.61.34
Set CW RO	0-Up Reset, CW Plus, Match, Read Ctrl	62.61.34

3.1.03 Segment Forward Space Per Count (Figure 3.1-14)

The forward-space-per-count code is designed to allow spacing over a series of tape records until a segment mark(block mark) or several segment marks have been found. The number of segments skipped is controlled by the setting of the start and stop registers. The start register is updated by one each time a segment mark is found. The end of the operation is reached when the start and stop addresses match. Only one control word is used during the segment count operations regardless of the control word sign (plus or minus).

The forward-space-per-count operation is performed in much the same manner as a normal read operation. The main differences are in the use of the start and stop register, and in preventing the data read from tape from entering into the buffer A register.

During the block-count operation the mode change latch is turned on to prevent the data from being read into the buffer A register as the tape records are being scanned for segment marks. When a segment mark is sensed, a block mark signal is developed, and the contents of the start register are updated by one.

To insure that the segment mark search is accomplished, the read disconnect delay signals (RDD 36, RDD 136) are inhibited from the tape channel until a match is found.

During the block-count operations, the tape drive ignores the inter record gaps due to the read call signal being available until the match has been found.

If a tape mark or a load point is sensed, the select and tape indicator is turned on. With this signal available, a final status word cycle is developed and the condition 5 latch (end of file) is turned on. At the same time the final status word cycle is inhibited, the timer op latch is reset. This drops the read call signal to TAU.

The following signals and controls are directly affected during the Forward Block Count Op development (Figure 3.1-14 for the Forward Block Count Op timing):

Command	Timing	Logic
Develop FWD Blk Count	DCDR Gt A, Op Reg 1 Bit, Op Reg 6 Bit	4H-62.61.15
Set Blk Count Ctrl	FWD Blk Cnt	2F-62.61.18
Set Mode Change	Blk Count Ctrl	2J-65.11.55
Develop Read Call	Any Tp RD, Tmr Op Gate	5B-62.61.23
Set ISW RI	Any Tp DCDR, Status Word Gt, Restart	5H-62.61.32
Set CW RO Latch	DCDR A, ISW RI Info Gt	3D-62.61.34
Set CW Xfer RO	CW RO Info Gt, X - Z	2C-62.61.36
Set CW Xfer RI	CW Xfer RO, V - X	2F-62.61.36
Perform 1-Up CR	CW RO L, Addr Gt, Z - V	65.51.47

End Block Count

Command	Timing	Logic
Set Enable Read Start	Any Tape Bit, No RD Stt Intlk, No BA Ser RO, No BA Ser RI	4E-65.11.57
Set Read Start # 3	Enable RD Stt, No Rd Stt 1 or 2, Y - P	2A-65.11.60
Sense Block Mark	C, A, 8, 4, 2, 1 Rd Bit, Spl 7	3C-65.11.16
Set Rd Start Intlk	Rd Stt 3, U Pulse	2E-65.11.52
Set BA Ser RO	Rd Stt 3, V - X	2D-65.21.20
Set BA Ser RI	No Rd Stt 3, BA Ser RO, U - W	4C-65.21.20

Command	Timing	Logic
0-Up Start Reg	Blk Cnt Ctrl, Blk Mark, BA Ser RO	65.51.45
Set End of Record Delay	Match, CW Minus, 0-Up Reset	62.61.70
Set Cond 2 Latch (TP R-W CLR)	RDD 36, Read Ctrl, End of Record Delay	5D-62.61.70
Set FSW RO Latch	Blk Cnt Ctrl RDD 136	4B-62.61.40
Reset Timer Op Gate	Set FSW	4G-62.61.40
Set FSW RI Latch	FSW RO Info Gt, No D Cy Reset	3C-62.61.41
Set End Op Reset Gate	Status Word Gt, FSW RI Info Gt, V - X	4C-62.61.73
Set Op Reset Timer	End Op Reset Gt, Status Word Gt, Z - V	4E-62.61.74
Reset Busy Latch	Op Reset Timer, Any Tp DCDR, No Intr, No Hang Up Error	3B-3C-62.61.06

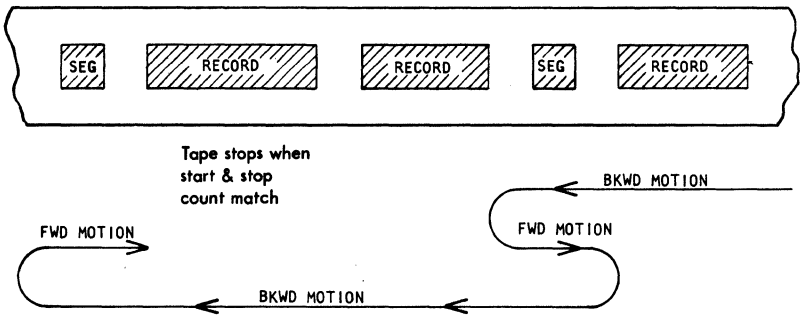
3.1.04 Segment Backspace Per Count (Figures 3.1-12, 13, 14, 15, 16A, and 16B)

The backspace-per-block-count operation is designed to allow spacing over a series of tape records while the tape drive is backspacing. The number of records spaced over is controlled by the setting of the start and stop register. Each time a segment mark (block mark) is found, the start address is updated by one. The end of the operation is reached when the start and stop addresses match. Only one control word is used during this operation, regardless of whether the control word sign is plus or minus.

The beginning of the backspace-block-count operation is performed in the same manner as the forward-block-count operation. Figure 3.1-14 has the various differences between the forward and backward op development. The following explanation deals with the controls that are necessary for sensing a block mark while backspacing.

Sensing a Segment Mark

To sense a segment mark while backspacing, each character read from tape is analyzed for read clock cycles. Due to the increased amount of skew when reading the tape while backspacing, it is possible to get two read clock cycles per character. Each time a character is detected that may be a segment mark, the tape drive is placed in the forward status to re-read the mark (Figure 3.1-12).



BKWD MOTION - USED TO SENSE SEGMENT MARK

FWD MOTION - USED TO RE-READ SEGMENT MARK

INTER RECORD GAPS ARE IGNORED DURING BLOCK COUNT OPERATIONS

FIGURE 3.1-12. BACKSPACE BLOCK COUNT TAPE MOVEMENT

To keep track of the number of read clock cycles sensed, a five-position block count ring is used. Each time a read clock cycle is sensed, two read sample pulses are developed: a sample 3 and a sample 7 pulse. These sample pulses are used to advance the block count ring whenever a tape character is sensed. This ring is used to determine whether the tape is to continue backspacing or is to stop, go into forward status, and re-read the character.

If at least two and no more than four read clock cycles are sensed, a control read signal is developed and the control backspace signal is dropped. The control backspace going off drops the backspace call signal to TAU. The control read signal is used to develop the read call signal which is sent to TAU to re-read the mark while in forward status (area 2 of Figure 3.1-16A).

Because a segment mark is written on tape as a one-character record, another character is not sensed for .4 ms. This causes a backspace read disconnect operation in TAU. At the .4 ms point, the read condition trigger is turned off. At the 2 ms point, the Go latch is turned off stopping the backwards motion of the tape (tape movement delays Figure 3.1-13).

At the 6.4 ms point, the backspace trigger is turned off ending the backspace operation. However, the read disconnect continues for another 4.8 ms to allow the electromechanical action to change from backward to forward status.

Command	Timing	Logic
Set Bksp Blk Count	Tp DCDR A, Op Reg 6 and 2 Bit	4J-62.61.15
Set Control Bksp	Bksp Blk Count, No 2, 3, or 4 Count Latch	6B-62.61.62
Bksp Call	Timer Op Gate, Cntr Bksp	4D-62.61.23
Set Count Pos 1 (1 st Read Clock Cycle)	Bksp Blk Cnt, Spl 7, No 2,3, or 4 Count Latch	2A-62.61.61

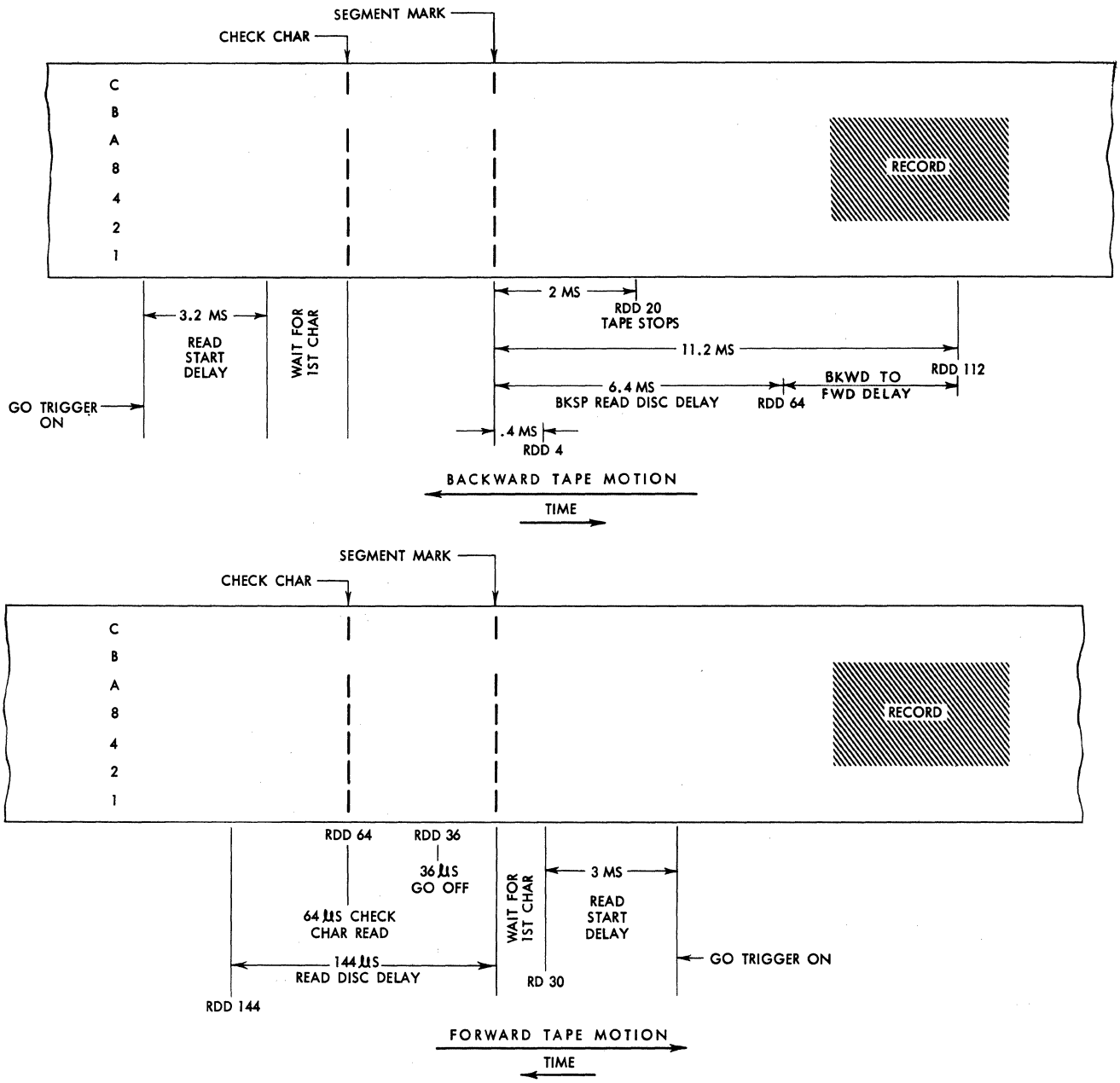


FIGURE 3.1-13. TAPE MOVEMENT DELAYS

Command	Timing	Logic
Set Count Pos 2 (2 nd Read Clock Cycle)	Count 1 Latch, Spl 3	4C-62.61.61
Set Control Read	Bksp Blk Count, Count 2 Latch	4H-62.61.62
Reset Control Bksp	Control Read	5B-62.61.62
Develop Read Call	Control Read, Timer Op Gate	4A-62.61.23

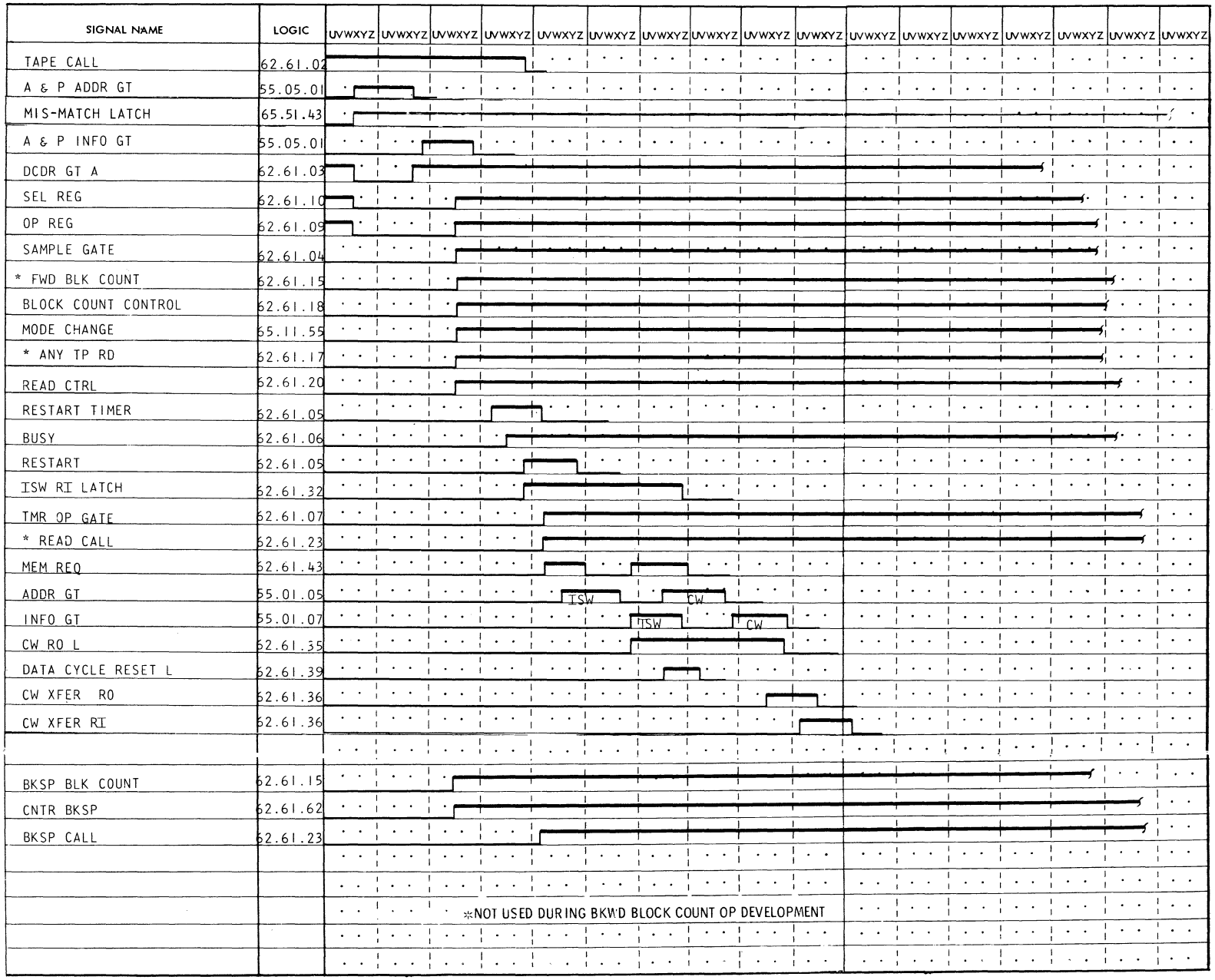


FIGURE 3.1-14. FWD & BKWD BLOCK COUNT OP DEVELOPMENT

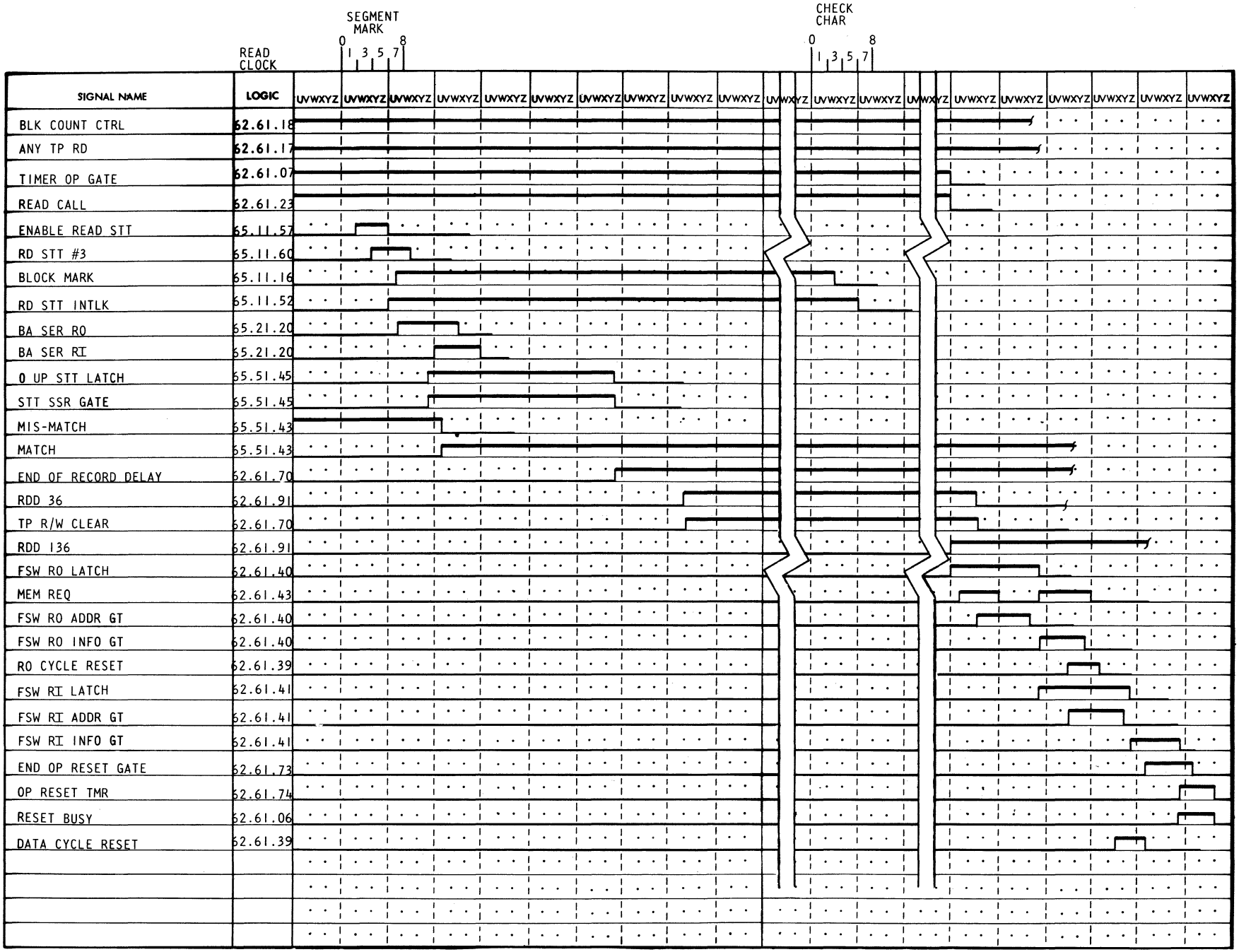


FIGURE 3.1-15. END BLOCK COUNT

Re-Read Segment Mark

With the block count ring in the tape channel control unit furnishing a read call signal to TAU, the Go trigger is turned on and the tape moves in the forward direction. The normal read delay of 3 ms is performed to allow the tape to get up to speed before turning on the read condition trigger in TAU (Figure 3.1-13 for the forward tape motion delays).

The first character read from tape is the segment mark. The sensing of the segment mark (block mark) is used to develop the 0-up start and 1-up start operation, which increases the contents of the start register by one. As mentioned previously, the segment mark is written as a one-character record, so a normal read disconnect is performed after reading the segment mark (area 3 of Figure 3.1-16B).

Command	Timing	Logic
Set Enable Read Start	Any Tp Bit, No Rd Stt Intlk, No BA Ser RO, No BA Ser RI	4E-65.11.57
Set Read Start # 3	Enable Rd Stt, No Rd Stt 1 or 2, Y-pulse	2A-65.11.60
Sense Block Mark	Spl 7, C, A, 8, 4, 2, 1 Bit	3C-65.11.16
Set RD Stt Intlk	RD Stt 3, U-pulse	2E-65.11.52
Set BA Ser RO	RD Stt 3, V-X	2D-65.21.20
Set BA Ser RI	No Rd Stt 3, BA Ser RO, U - W	4C-65.21.20
0-Up Start Reg	Blk Count Ctrl, Blk Mark, BA Ser RO L	65.51.45
0-Up Start Reset	Stop Tag Tens L, 0-Up Start	65.51.45
1-Up Start Reg	0-Up Start, Z - V, Mismatch	65.51.46

Prevent Sensing of Same Mark

Because no other character is sensed, the tape drive goes into its normal read disconnect cycle. When the check character is sensed, the count stop latch is turned on. This latch being on prevents the sensing of the same segment mark by inhibiting the turn-on of the count latches when a read clock cycle is sensed. The count stop latch remains on until an end count signal is developed.

At the same time the control stop latch is turned on, a control reset is developed to reset the condition latches. With the count latches reset, the control read gate is dropped, and the control backspace gate is turned on.

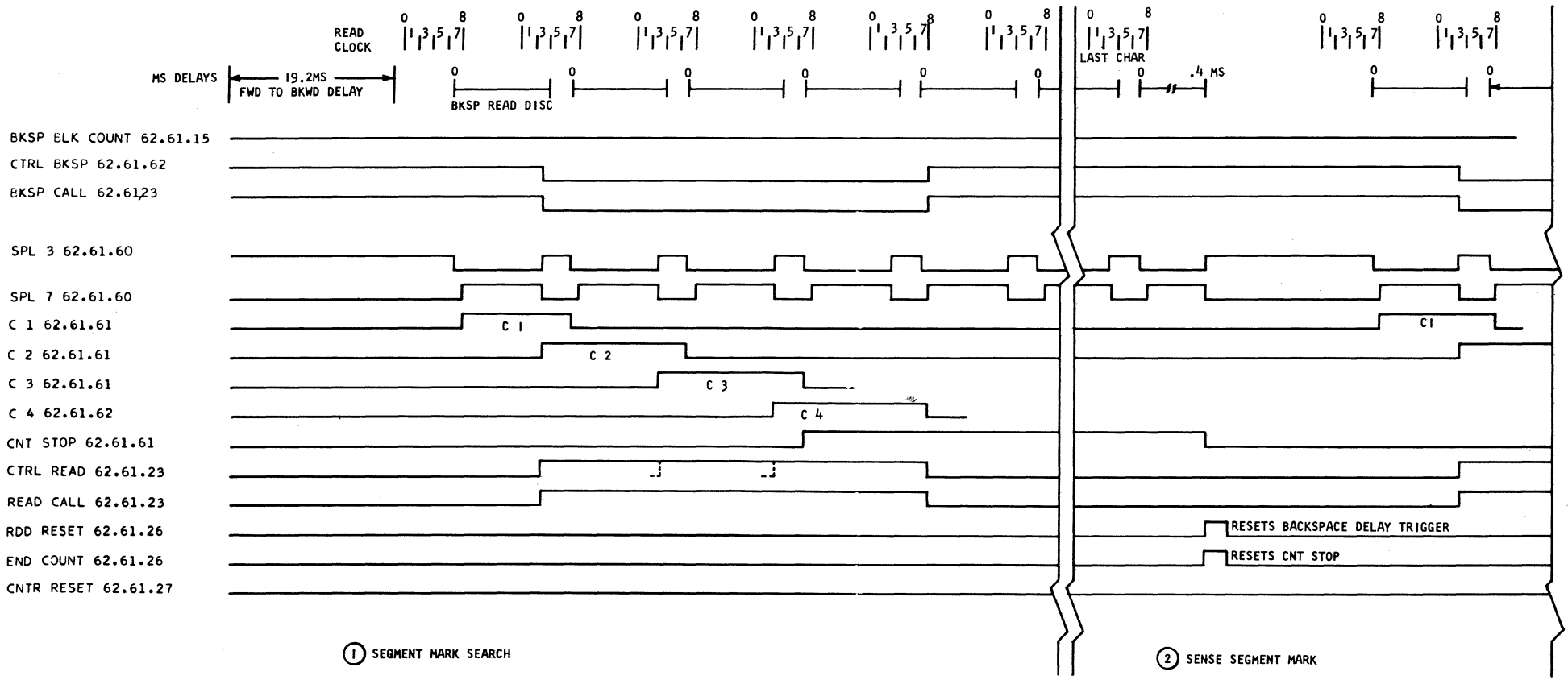


FIGURE 3.1-16A. BACKSPACE COUNT TIMING (AREAS 1 AND 2)

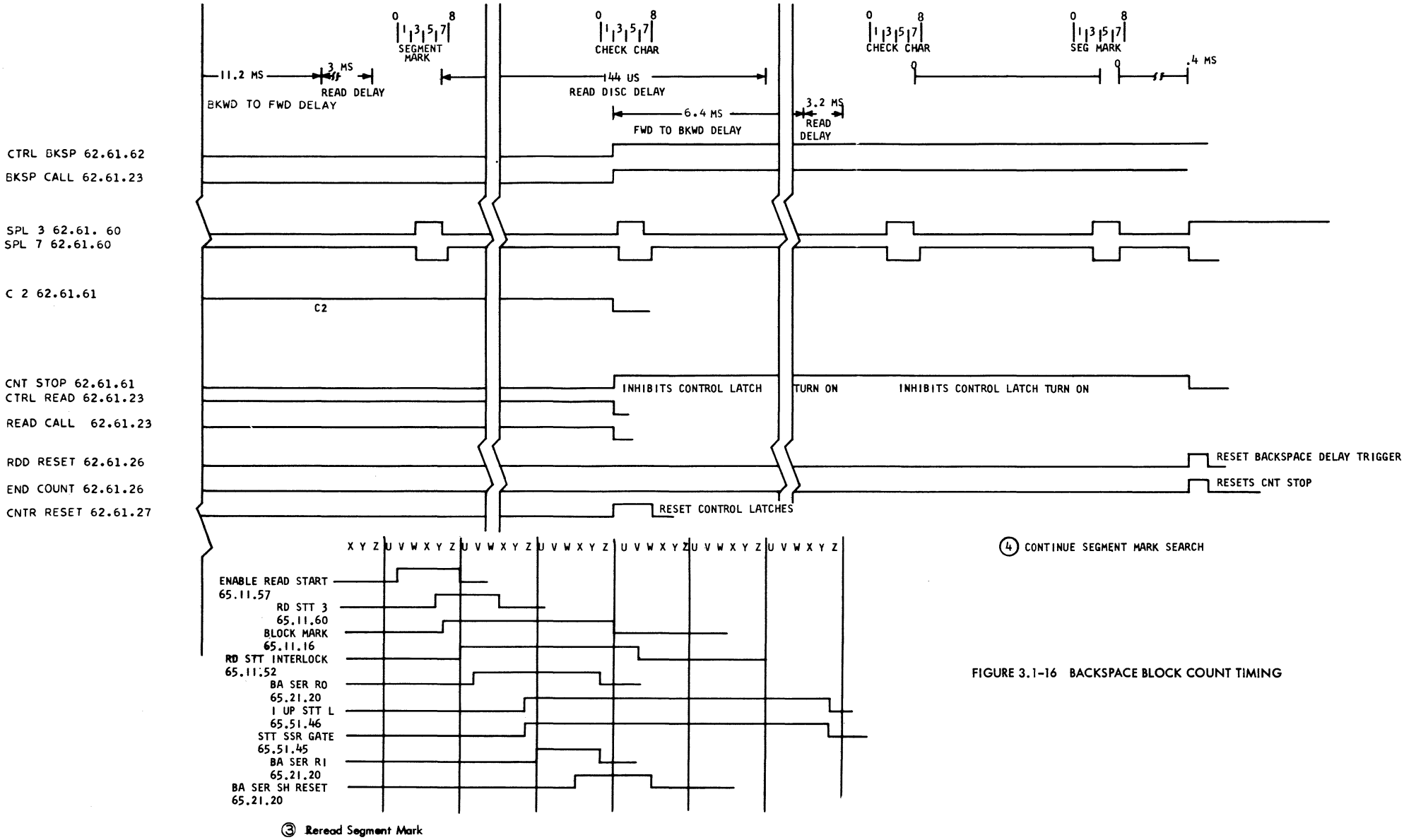


FIGURE 3.1-16 BACKSPACE BLOCK COUNT TIMING

FIGURE 3.1-16B. BACKSPACE COUNT TIMING (AREAS 3 AND 4)

Command	Timing	Logic
Set Count Stop Latch	Check Char	62.61.62
Develop Control Reset	Check Char	5A-62.61.27
Reset Count Latches	Control Reset	62.61.61
Reset Control Read Gate	No Count 2 Latch	5H-62.61.62
Set Control Backspace	Bksp Blk Count, No 2, 3 or 4 Count Latch	5B-62.61.62
Develop Bksp Call	Timer Op Gate, Ctrl Bksp	4D-62.61.23

Develop Backspace Call

With the control backspace gate available, a backspace call signal is developed and sent to TAU. The tape drive again goes into a forward-to-backward status. The first character read is the segment mark that was just re-read. However, the sensing of this character is inhibited in the channel control unit by the control stop latch.

Prevent Forward to Backward Transfer

As the tape backspaces past the segment mark, a bit does not occur for .4 ms, and the read condition trigger in TAU is turned off. Normally, at the 2 ms point the Go trigger is turned off and the tape drive stops. However, with a control backspace signal available, a read disconnect delay reset is developed at the .4 ms point in the channel control unit. This reset signal resets the delay trigger in TAU. With the delay trigger off, the Go trigger remains on, and the tape continues to move backwards (area 4 of Figure 3.1-16B).

Command	Timing	Logic
Develop RDD Reset	.4 ms, Ctrl Bksp	3B-62.61.26

Continue Backspace Per Count

As the read disconnect delay reset is developed, an end-count signal is developed to reset the control stop latch. With the control stop latch reset, the characters are again analyzed for read clock cycles. The second read clock cycle causes the control backspace gate to be dropped, and the control read gate to be turned on.

When a segment mark is not found, the block count ring advances into its last position, which is the control stop position. As the ring advances into the last position, the control read gate is dropped, and the control backspace is again turned on. With no segment mark found, the forward-to-backward transfer is inhibited in the same manner as previously described (area 1 of Figure 3.1-16A).

Command	Timing	Logic
Develop End Count	Ctrl Bksp, .4 ms	3B-62.61.26
Reset Count Stop	End Count	4D-62.61.62

End Backspace Per Count

When a segment mark is found that causes the start and stop register to match, a read disconnect operation is performed. At the 136 usec point of the read disconnect delay, a reset signal is developed to turn off the timer op gate. With the timer op gate off, the backspace call to the tape adapter unit is dropped. Because the tape drive is setting in the forward status, the tape drive busy signal is dropped, thereby releasing the tape drive unit.

The RDD 136 signal is also used to develop the final status word cycle. The synchronizer busy latch is released at the completion of the final status word cycle (Figure 3.1-15).

Command	Timing	Logic
Set End of Record Delay	CW Minus, 0-Up Reset, Match	62.61.70
Reset Condition 3 Latch	Any Tp DCDR, End of Record Delay	62.61.86
Set Condition 2 Latch (Tp R - W Clear)	RDD 36, Read Ctrl, End of Record Delay	5D-62.61.70
Set FSW RO Latch	Blk Cnt Ctrl, RDD 136	4B-62.61.40
Reset Timer Op Gate	Set FSW	4G-62.61.40
Set End Op Reset	Status Word Gt, FSW RI Info Gt, V - X	4C-62.61.73
Set Op Reset Timer	End Op Reset Gt, Status Word Gt, Z - V	4E-62.61.74
Reset Busy Latch	Op Reset Timer, Any Tp DCDR, No Intr, No Hang Up Error	3B-3C-62.61.06

3.2.00 TAPE-WRITE INSTRUCTIONS

The tape-write operation is performed under control of the record definition register (start and stop). The alpha or numeric words read from core storage are recorded on tape high-order position first (pos 0).

The numeric word is written on tape as a ten-character word with the tenth character made up of the units position and sign.

The alpha word is written on tape as a five-character word with no sign designation. All data words are parallel transferred from core storage to the buffer B register. The data word is then parallel transferred to buffer A via the distributor bus. As the data word is placed onto the distributor bus, the sign is analyzed. All write operations start in alpha mode. If a numeric sign is sensed on the first word, a mode change mark is written prior to writing the word on tape. Thereafter, a mode change mark is written prior to writing any word whose sign is not the same as the word preceding it (alpha or numeric).

On a continuous write operation, as the first data word is placed into buffer A, the second data word request is initiated to place a data word into buffer B. When the last character is read out of buffer A, the contents of buffer B are parallel transferred to buffer A. At this point the third data word request is initiated to fill up buffer B. This operation continues until the start and stop addresses become equal.

The start register is 0-upped and matched against the stop register as each data word is transferred in from core storage. On the first data word transfer, a 0-up start is performed and the start register is matched with the contents of the stop register to check if one, or more than one data word, is to be used. At the completion of the 0-up start operation, if a mismatch is sensed, the start register content is increased by one. This allows the next data word address to be available when needed.

If at the completion of the 0-up start operation a match signal is sensed, the address in the control register will specify the location of the next control word if the previous control word sign was plus.

The control register A is 1-upped after the control register A address is used to specify the location of the control word.

3.2.01 Tape-Write

The tape-write operation is performed in much the same manner as tape-read. The initial status word, control word, and final status word cycles are explained under the read instruction, section 3.1.00. The main differences are in controlling the data word cycle (Figure 3.2-1).

Request Data Words

During a write operation, as the control register is being 1-upped, the first data word request is made. At the completion of the 1-upping of the control register, a 0-up start operation is performed to determine if another data word request is to be made.

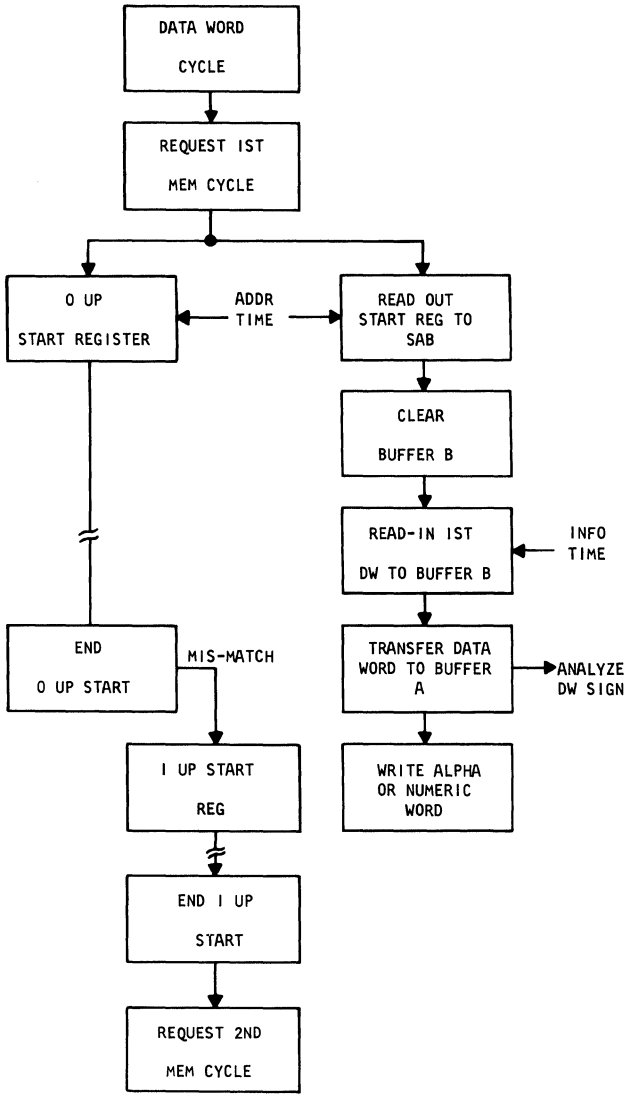


FIGURE 3.2-1. DATA WORD CYCLE (WRITE)

If a mismatch is available at the completion of the 0-up start operation, the data word request latch is turned on. However, the memory request latch is inhibited from requesting memory until the 1-up start operation is completed. The 1-upping of the start register develops the address location of the next data word.

At the completion of the 1-up operation, the memory request data signal is sent to core storage priority controls. All data request signals have priority over control requests, regardless of which tape channel is making the request.

When core storage accepts the request, it replies in the form of an address and an information gate. At address gate time, the start address is placed onto the sync address bus to condition the core storage address triggers. With core storage addressed to read out the second data word, a 0-up start operation is initiated to see if a third data word is to be used. At the completion of the 0-up operation, if a mismatch is sensed, a 1-up start operation is initiated to develop the address for the third word.

The third data word request is not made until the last character of the first data word is read out to the translator. This operation continues in the same manner until a match is sensed at the completion of the 0-up operation.

With a match signal present, the control word sign is analyzed to determine whether an additional control word, or an end of record has been detected.

Command	Timing	Logic
Request First Data Word (Set DW RI-RO)	CW Xfer RI, First Word, Write Ctrl	62.61.34
Request Memory	DW RI-RO, No Addr Gt, No Info Gt, No SSR	62.61.38
Set Memory Request Data	DW RI-RO L, Mem Req, No CE On	62.61.43
RO Stt Reg to SAB	DW RI-RO L, Addr Gt	62.61.45
Clear Buffer B	DW RO Addr Gt, W-Y	62.61.45
0-up Start Reg	DW-RI-RO L, No 1-up CR Gate, Addr Gt, Z-V	65.51.45
RI First Data Word to BB	DW RO Info Gt	62.61.45
End DW RO Cycle	DW RO Info Gt, Y-Z	62.61.39
Set 0-up Reset	Stop Tag Tens Latch, 0-up Start	65.51.45
Set DW RI-RO Latch	1st DW Xfer, Write Ctrl, Mismatch	62.61.34
1-up Start Reg	0-up Start Reset, Z-V, Mismatch, No Blk 1-Up Stt	65.51.46
Set 1-up Start Reset	Stop Tag Tens Latch 1-Up Stt	65.51.46

Sense A Continuous Write Operation

It can be seen from Figures 3.2-2 and 3.2-3 that a mismatch has been assumed at the completion of the 0-up operation. With a mismatch sensed, the Set DW Rl-RO Signal is developed; however, a memory request is not made until the start register is 1-upped. The 1-up operation develops the address, in core storage, of the second data word.

As the 1-up start operation is being performed, buffer A is cleared before the first data word is transferred from buffer B. As the data word is transferred to buffer

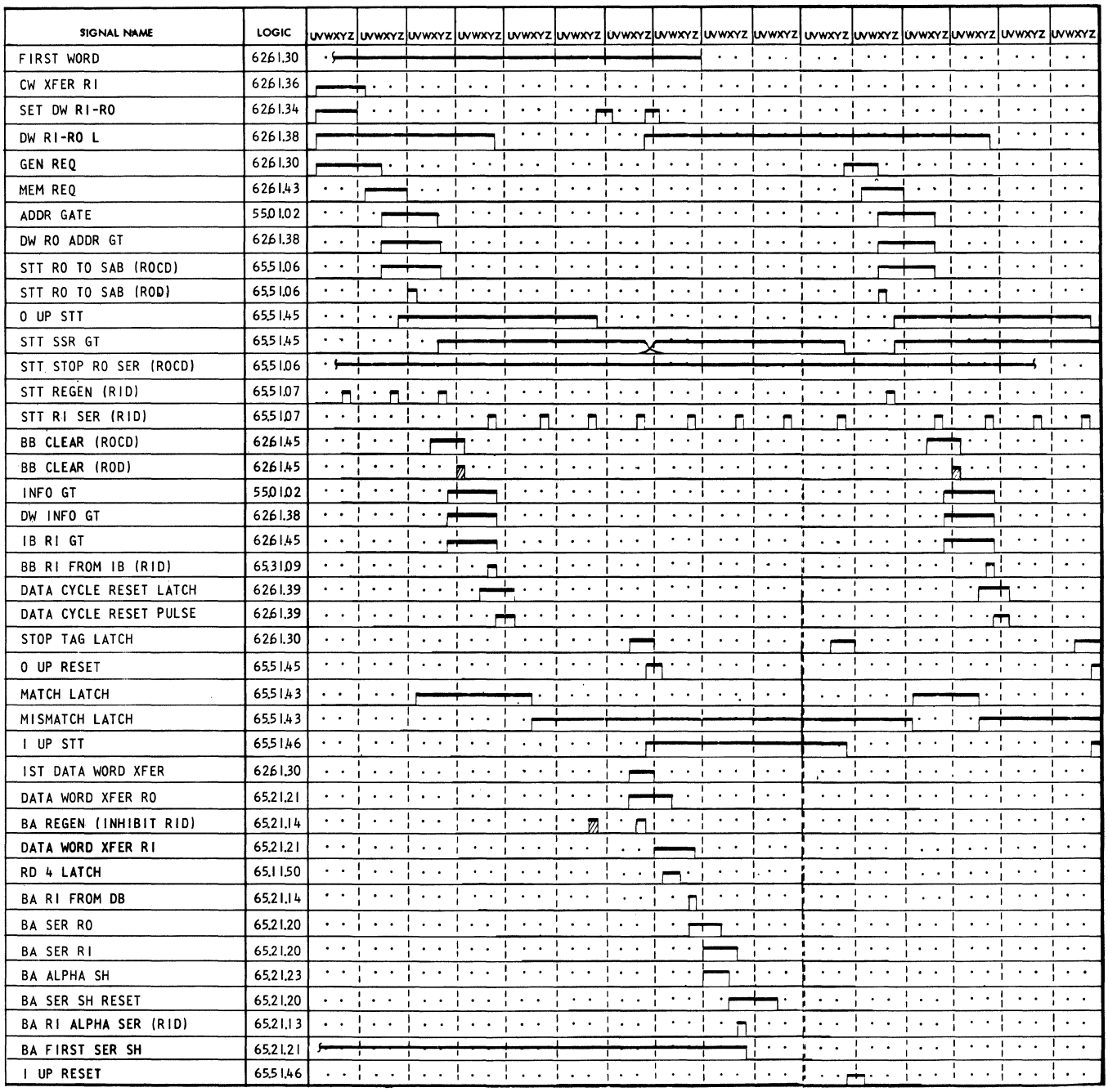


FIGURE 3.2-2. FIRST AND SECOND DATA WORD TRANSFER (NO MODE CHANGE)

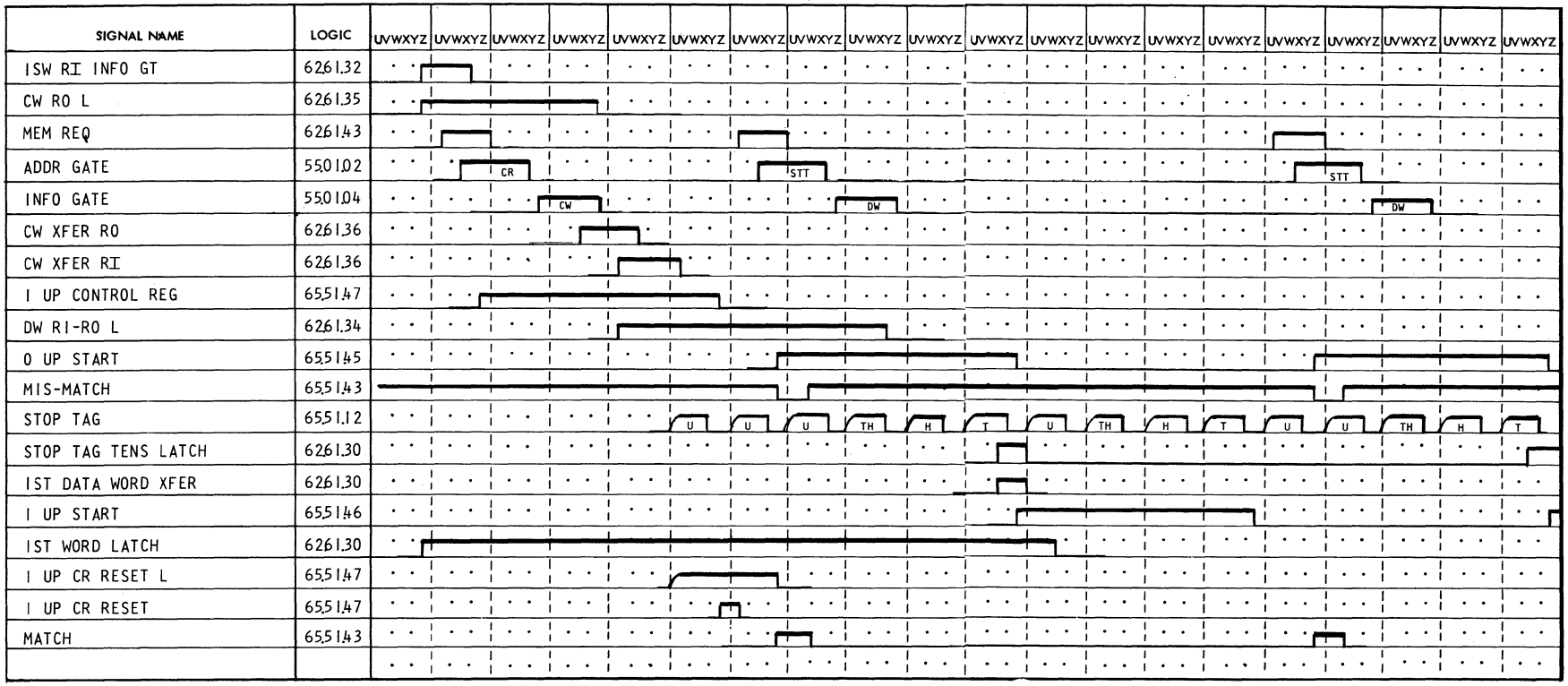


FIGURE 3.2-3. WRITE OPERATION--LOAD FIRST TWO WORDS (FIRST CW GREATER THAN TWO WORDS)

A, the sign is analyzed to determine if the first word is alpha or numeric. Figure 3.2-2 shows that a no mode change has been assumed.

With no mode change, the Tp Start 4 latch is turned on. The output of this latch is used to control the advance of buffer A, which places the first alpha character into the translator.

To condition the translator, the translator alpha drive is brought up to allow the first alpha digit to be read into the translator. With the alpha character read into the translator, the non-selected cores are further biased into the zero state. A translator set pulse is then developed to switch the selected core to the 1 state. For further information on the translator operation, refer to section 2.6.00.

Command	Timing	Logic
Set 2nd DW RI-RO	First Word, 0-up Stt Reset, Mismatch, Z-V	3G-62.61.34
1-up Start Reg	0-up Stt Reset, Mismatch, Z-V	2A-65.51.46
Clear Buffer A	Data Word Xfer RO L	2E-65.21.12
BA RI from DB	Data Word Xfer RI L, Write Ctrl	4A-65.21.27
Perform First Alpha Shift	Bfr A Ser RI, Alpha Ctrl, Any Tp DCDR, No Mode Change	5B-65.21.23
Set Xlator Alpha Drive	Alpha Ctrl, Write Bfr A Ser RI, V-Y	3B-65.11.03
Xlator Set Drive	Bfr A Ser RI, Any Write	2G-65.11.03

Write First Alpha Character

When the write-clock signal is received from the tape adapter unit, the translator RO drive is brought up. This transfers the first alpha character to TAU.

The write-clock signal is also used to turn on the Tp Rd Start 4 latch to repeat the advancing of the A-register and the loading of the translator. The write operation continues in this fashion until the Alpha Tag is sensed.

Command	Timing	Logic
Xlator RO Drive	Wr Clock Timing	3D-65.11.04
Perform 2nd Alpha Shift	Bfr A Ser RI, Any Tp DCDR, Alpha Ctrl	5B-65.21.23
Set Alpha Drive	Bfr A Ser RI, Alpha Write, V-Y	3B-65.11.03
Xlator Set Drive	Bfr A Ser RI, Write	2G-65.11.03

Perform Second Data Word Request

As the 1-up start operation is completed, the second data word memory request is initiated to read out the second data word. The DW RI-RO latch had been previously set; however, the generate request signal could not be developed until the start serial shift right gate was dropped (Figure 3.2-2).

When the priority controls accept the request, the start register address is read out to the sync addr bus during addr gate time. During addr time, the buffer B register is cleared to accept the second data word when it is read out of core storage during info gate time.

With a mismatch sensed, the start register is again 0-upped and matched with the stop register. This operation continues until a match is reached between the start and stop registers.

Command	Timing	Logic
Request Memory	DW RI-RO Latch, No addr and No Info Gt, No SSR	6C-62.61.38
RO Stt Reg to SAB	DW RI-RO Latch, Addr Gt	3C-65.51.06
Clear Buffer B	DW RO Addr Gt, W-Y	2C-62.61.45
Initiate 0-up Stt	DW RO Addr Gt, Mismatch, Z-V	2C-65.51.46
RI 2nd DW to BB (IB-RI Gate)	DW RO Info Gt	5F-62.61.45

Request a Control Word

Whenever a match is sensed at the completion of a 0-up operation, it signifies that the last data word has been placed into buffer B.

As the last character of the next to last word is read out of buffer A, the contents of buffer B is parallel-transferred to buffer A. At this point, a control word request is initiated if the previous control word sign was plus (Figure 3.2-4 or 3.2-5).

At the completion of the control-word cycle, a data word request is developed. The data request places a data word into buffer B from the new memory block. For a complete timing on the control word and data word cycle, refer to Figures 3.1-5 and 3.2-2.

Command	Timing	Logic
Request C W RO	CW Plus, Match, Write Ctrl, BA Ser RO L, BA Last Ser SH, Z-V	62-61.34
Set DW RI-RO	CW Xfer RI, Match, Write Ctrl	62.61.34

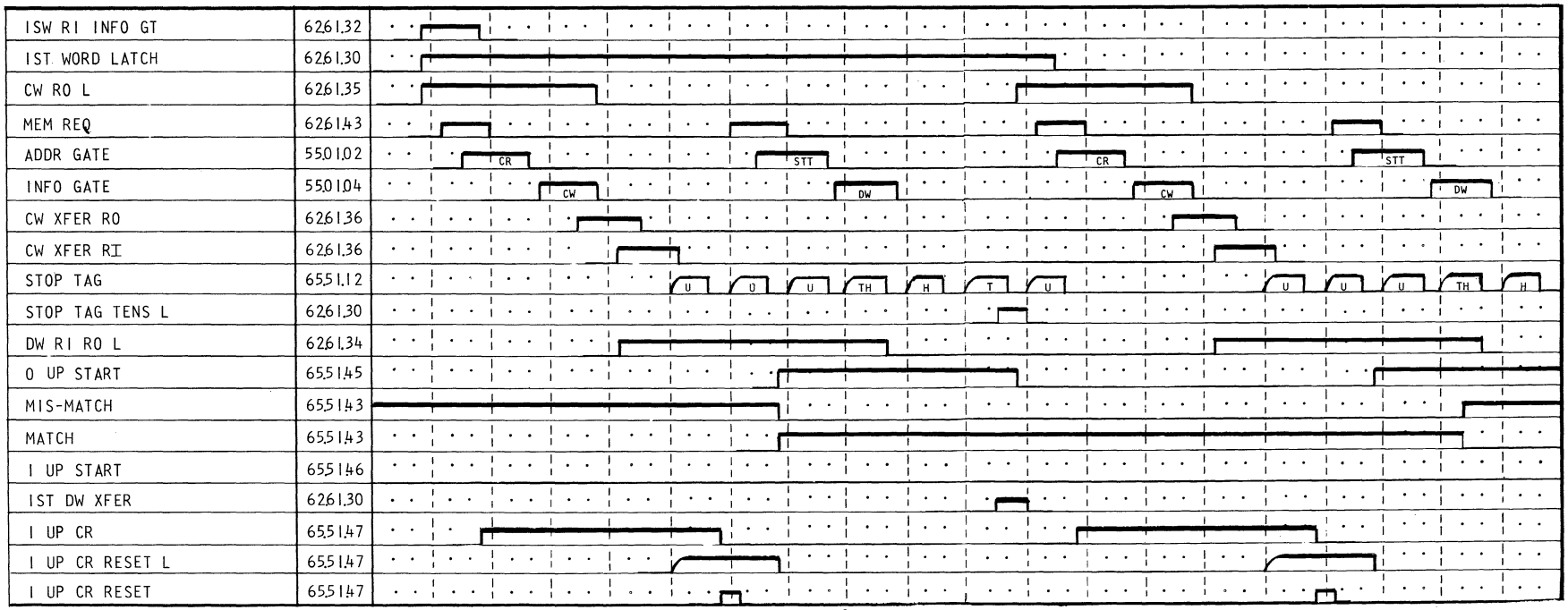


FIGURE 3.2-4. WRITE OPERATION--LOAD FIRST TWO WORDS (FIRST CW IS ONE DATA WORD; SECOND CW IS GREATER THAN ONE)

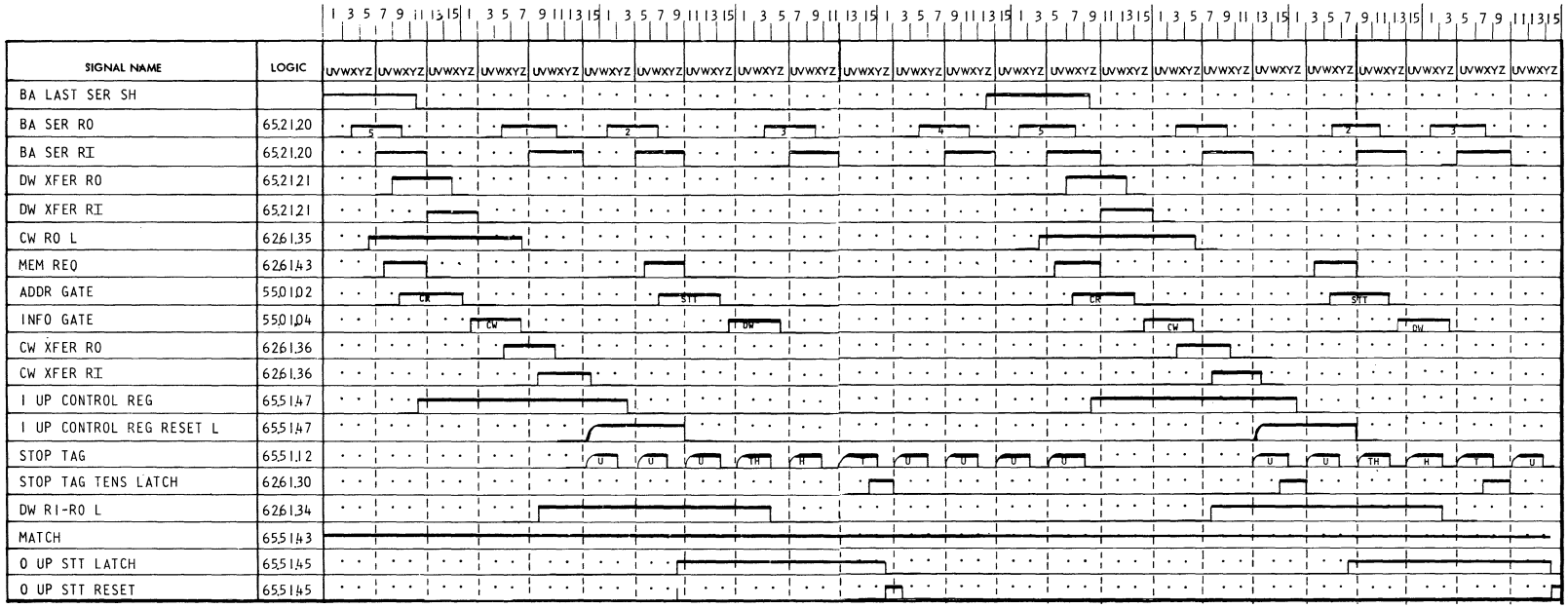


FIGURE 3.2-5. WRITE OPERATION (ONE WORD SCATTER)

Sense a Mode Change

During a write operation, if a mode change is sensed when transferring a data word to buffer A (via the distributor bus), the first character is prevented from reading into the translator.

As the Data Word Xfer RO latch is turned on, the alpha or numeric hold latch is turned on. The turning on of the hold latch is dependent upon the previous setting of the alpha or numeric latch. For example, if the alpha latch was on during the previous data word operation, the alpha hold latch is turned on. The function of the hold latch is to have an indication of the previous operation, because both the alpha and numeric latches are reset by the Data Word Xfer RO signal.

When the Data Word Xfer RI latch is turned on, the contents of buffer B is transferred to buffer A. As the contents of buffer B is placed onto the distributor bus, the sign position is analyzed. Figure 3.2-6 shows that the previous operation was alpha, and that a numeric sign was sensed to turn on the mode-change latch.

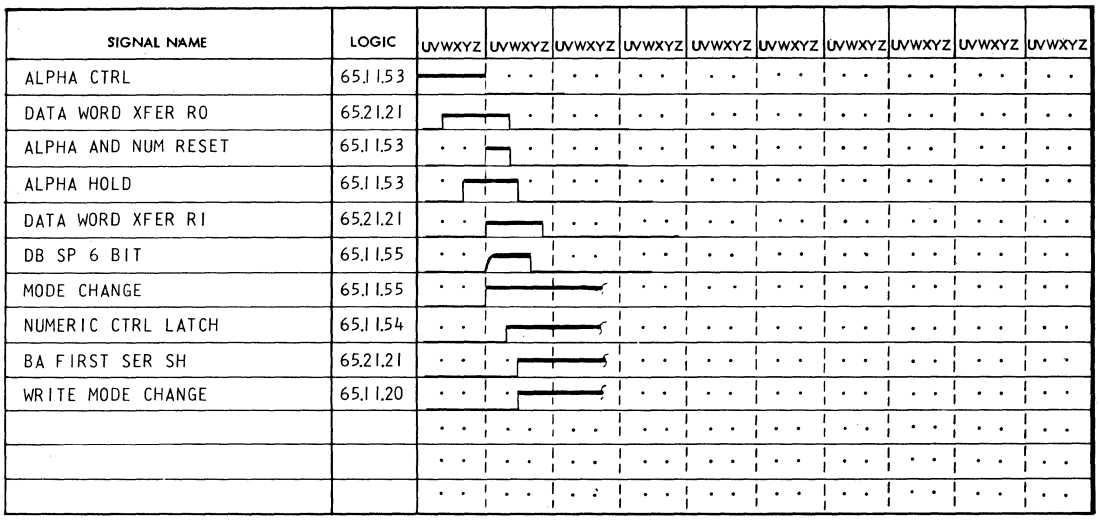


FIGURE 3.2-6. WRITE MODE CHANGE

With the mode-change latch on, both the advancing of buffer A and the development of the translator control drive lines are inhibited. The reason for inhibiting is because a mode-change character must be written prior to the data word.

The first write clock pulse from the tape adapter unit records the mode change character on tape. The write clock pulse also causes the buffer A register to left-shift placing a numeric character into the translator. The rest of the write operation is performed in its normal manner.

If a mode change is sensed when the last character is in the translator, the writing of the mode change character is prevented until the last character is written on tape. For a further explanation, refer to the Write Sign Over Units section, which follows.

Command	Timing	Logic
Set DW Xfer RO	Bfr A Ser RI, BA Last Ser Sh, W-Y	3C-65.21.21
Clear Buffer A	DW Xfer RO L	2E-65.21.12
Set Alpha Hold	DW Xfer RO, Write,	3G-65.11.53
Reset Alpha & Numeric	DW Xfer RO, Write, U-W	3F-65.11.53
Set DW Xfer RI,	DW Xfer RO, U-W	3E-65.21.21
Set Mode Change	DW Xfer RI, Write, DB SP 6B	3B-65.11.55
Set Numeric Control	DW Xfer RI, Write, DB SP 6B, W-Y	3D-65.11.54
Set BA First Ser Sh	DW Xfer RI, X-Z	5F-65.21.21
Set Data Lines	Mode Change, No Last Char Latch, BA First Ser Sh	3G-65.11.20
Write Mode Change Char	Write Clock Pulse	(TAU)
Perform Numeric Shift	Bfr A Ser RI, Numeric Ctrl, Any Tp DCDR	5D-65.21.23
Set Wr Xlator Numeric Drive	Bfr A Ser RI, Write, Numeric Ctrl, Y-X	3A-65.11.05
Xlator Set Drive	Bfr A Ser RI, Write, X-Pulse	2G-65.11.03

Write Sign Over Units (Figure 3.2-7)

A numeric-write operation is performed in much the same manner as an alpha-write. The main differences are in the insertion of the tag into position 8, and the writing of the sign over units.

When the tag is sensed, the BA last serial latch is turned on, which signifies that one more left-shift is needed to clear the buffer A register. As a write-clock pulse is furnished from TAU, the next to last character is read out of the translator. With the character read out of the translator, the BA serial controls are conditioned to perform the BA last serial shift. The BA ser RI latch along with the BA last serial shift latch is used to develop the BA write sign gate and to bring up the Xlator Sign Drive.

The BA Write Sign Gate is used to sample the contents of the BA Sign and place the sign value onto the Alpha Write Bus. At the same time, the contents of the units position is placed onto the Numeric Write Bus.

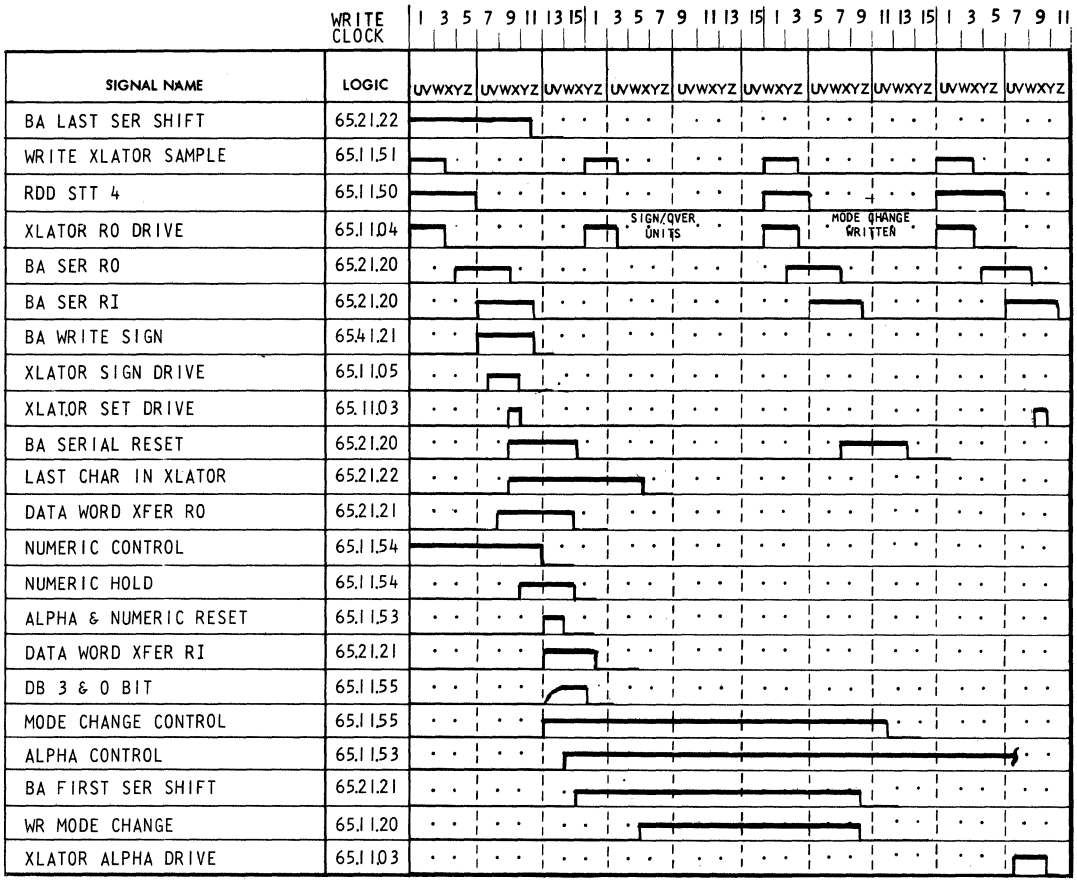


FIGURE 3.2-7. WRITE SIGN OVER UNITS (WITH MODE CHANGES)

The Xlator Sign Drive is used to inhibit the use of the alpha and numeric cores and to read in the sign and the contents of the units position into the translator. Both the sign and units position are combined within the translator to set the core for the particular combination of sign and units digit. Refer to the following table for the coding of the sign over units.

	Numeric Value	CBA Code	7070 Code
+ SIGN	0	BA 82	90
	1	CB A 1	91
	2	CB A 2	92
	3	BA 21	93
	4	CB A 4	94
	5	BA 41	95
	6	BA 42	96
	7	CBA 421	97
	8	CBA 8	98
	9	BA 81	99

- SIGN	0	CB 82	60
	1	B 1	61
	2	B 2	62
	3	CB 21	63
	4	B 4	64
	5	CB 41	65
	6	CB 42	66
	7	B 421	67
	8	B 8	68
	9	CB 81	69

Sense Mode Change

During a write operation as the BA last serial shift operation is being performed, the Last-Character-In-Translator latch is turned on.

If a mode change is sensed when the last character is in the translator, the writing of the mode change character is prevented until the last character is written on tape.

On the next write pulse from TAU, the last character is read out of the translator and recorded on tape. However, with the last-character-in-translator latch on, and a mode change present, the Rd Stt 4 latch is prevented from turning on. With the Rd Stt 4 latch off, the advancing of the buffer A register is inhibited, thereby preventing a character from being placed into the translator. At write clock 5 time, the last-character-in-translator latch is turned off.

With this latch off, the next write clock 1 pulse causes the mode change character to be written on tape and a character placed in the translator.

Write Next to Last Character

Command	Timing	Logic
Set Last Serial Sh	BA Tag, Z-V	3D-65.21.22
Set Write Xlator Sample	Write Clock 1 Pulse	3D-65.11.52
Set Xlator RO Drive	Wr Xlator Sample, No Mode Chg, No First Ser Sh	3D-65.11.04
Set Rd Stt 4	Wr Xlator Sample, No Last Char Latch, No Mode Chg	3D-65.11.50
BA Ser RO	Rd Stt 4, Y-U, No DS Write	2A-65.21.20
BA Ser RI,	BA Ser RO, U-W, No Rd Stt 3	4C-65.21.20

Command	Timing	Logic
BA Write Sign	Tp Write, Numeric Ctrl, BA Ser RI, Last Ser Sh	4F-65.41.21
Set Xlator Sign Drive	BA Ser RI, BA Last Ser Sh, Numeric Ctrl, V-X	3C-65.11.05
Xlator Set Drive	BA Ser RI, Any Tp Wr, X	3G-65.11.03
BA Ser Reset	BA Ser RI, X-Z	4H-65.21.20
Set Last Char In Xlator Latch	Any Tp Wr, BA Last Ser Sh, BA Ser RI, X-Z	4G-65.21.22
Set DW Xfer RO	BA Ser RI, Last Ser Sh, W-Y	3C-65.21.21
Set Numeric Hold	DW Xfer RO, Tp Wr, Num Ctrl, Y-U	2J-4J-65.11.54
Reset Alpha & Numeric	DW Xfer RO, U-W	3F-65.11.53
Set DW Xfer RI	DW Xfer RO, U-W	3E-65.21.21
BA RI from DB	DW Xfer RI, Write Ctrl, Y Time	4A-65.21.27
Sense Mode Change	DB 3 & 0 Bit, DW Xfer RI, Numeric Hold	3D-65.11.55
Set Alpha Ctrl	DW Xfer RI, DB 3 & 0 Bit, W-Y, Any Tp Wr	3D-65.11.53
BA First Ser Sh	DW Xfer RI, X-Z	3F-65.21.21

Write Sign Over Units

Command	Timing	Logic
Wr Xlator Sample	Wr Clock 1	3D-65.11.51
Xlator RO Drive	Wr Xlator Sample	3D-65.11.04
Inhibit Rd Stt 4	Last Char L, Mode Chg	2B-65.11.50
Set Wr Mode Chg Gate	No Last Char Latch, BA First Ser Sh, Mode Chg	3G-65.11.20

Write Mode Change

Wr Xlator Sample	Wr Clock 1	3D-65.11.51
Inhibit Xlator RO	BA First Ser Sh, Mode Chg, No Last Char Latch	3C-65.11.04
Set Rd Stt 4	Wr Xlator Sample, No Last Char	3D-65.11.50
Set BA Ser RO	Rd Stt 4, Y-U	2A-65.21.20
Set BA Ser RI	BA Ser RO, U-W	4C-65.21.20
BA Alpha Shift	BA Ser RI, Alpha Ctrl, Any Tp DCDR	5B-65.21.23
BA Serial Reset	BA Ser RI, X-Z	4H-65.21.20

Sense-End-of-Write Operation

The end of a tape operation is determined when a match signal is sensed along with a control word minus sign.

When the last data word is transferred from buffer B to buffer A, the end-of-record-delay latch is turned on. The output of this latch is used to reset the short length record latch (cond 3 latch).

As the last data word character is serially transferred from buffer A, the write-end-of-record latch is turned on. After the last character has been written, the output of this latch is used to develop a Disc Call Signal, which is sent to the TAU. The end-of-record latch is also used to set the correct length record latch (Figure 3.2-8).

Command	Timing	Logic
Set End of Record Delay	DW Xfer RI, CW Minus Match, Write Ctrl	62.61.70
Reset Cond 3 Latch	EOR Dly, Any Tp DCDR	3C-62.61.86
Set Wr End of Record	EOR Delay, BA Ser RO L, BA Last Ser Sh, Wr Ctrl	2C-62.61.71
Set Correct Length Record (Tp R-W Clear)	Wr End of Record, BA Ser RI L, Any Tp DCDR	5E-62.61.70
Develop Disc Call	WR End of Record, Last Char Written	5D-62.61.71

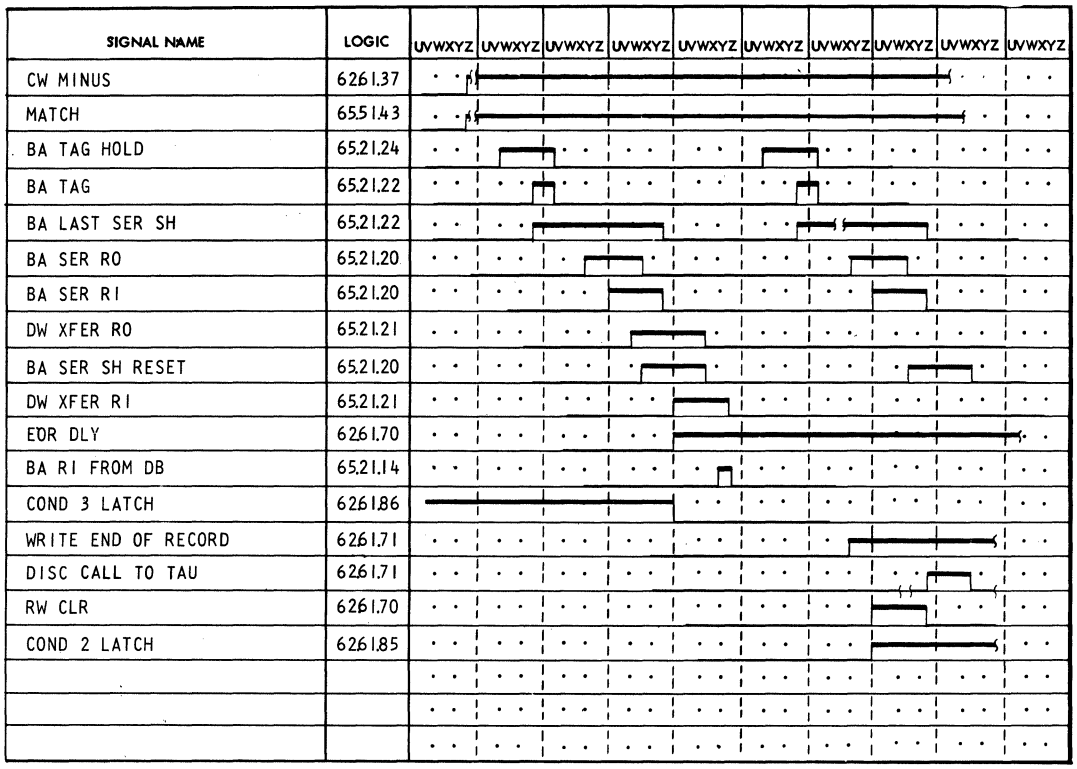


FIGURE 3.2-8. WRITE END OF RECORD

3.2.02 Write-Per-Record-Mark Control

The write-per-record-mark operation is performed in the same manner as an alpha-write operation. To perform the write-per-record-mark operation, the word must be alphabetic, and the record mark must be in the low-order positions of the data word (positions 8-9). With the record mark in any other position of the data word, it is written as any other alpha character.

The sensing of the record mark is accomplished when the data word is placed onto the distributor bus. When a record mark is sensed, it has the same effect as the start and stop addresses becoming equal.

The word having the record mark is the last word written on the tape from the core storage block specified by the start and stop register. If the previous control word sign was plus, a new control word is read into the record definition register. However, if the previous control word sign was minus, the end-of-record-delay latch is turned on, and the normal tape write disconnect operation takes place.

Analyze First and Second Data Word for Rec Mark (Figure 3.2-9)

As the first data word is brought into buffer B, the start register is 0-upped and matched against the stop register to see if more than one word is to be read in from core storage. As the data word is read out on the distributor bus and regenerated, the sign and positions 8 and 9 are analyzed for a record mark.

At the completion of the 1-up operation, data word request is initiated to move the second data word into buffer B.

During the data word transfer cycle, the Rd Stt 4 latch is turned on to condition the buffer A serial left-shift controls to place the first alpha character into the translator.

When the tape adapter unit furnishes a write-sample pulse, the first alpha character is read out to the read-write register in the tape adapter unit. The write sample pulse is also used to turn on the Rd Stt 4 latch, which conditions the buffer A serial shift controls to read out the second alpha character to the translator.

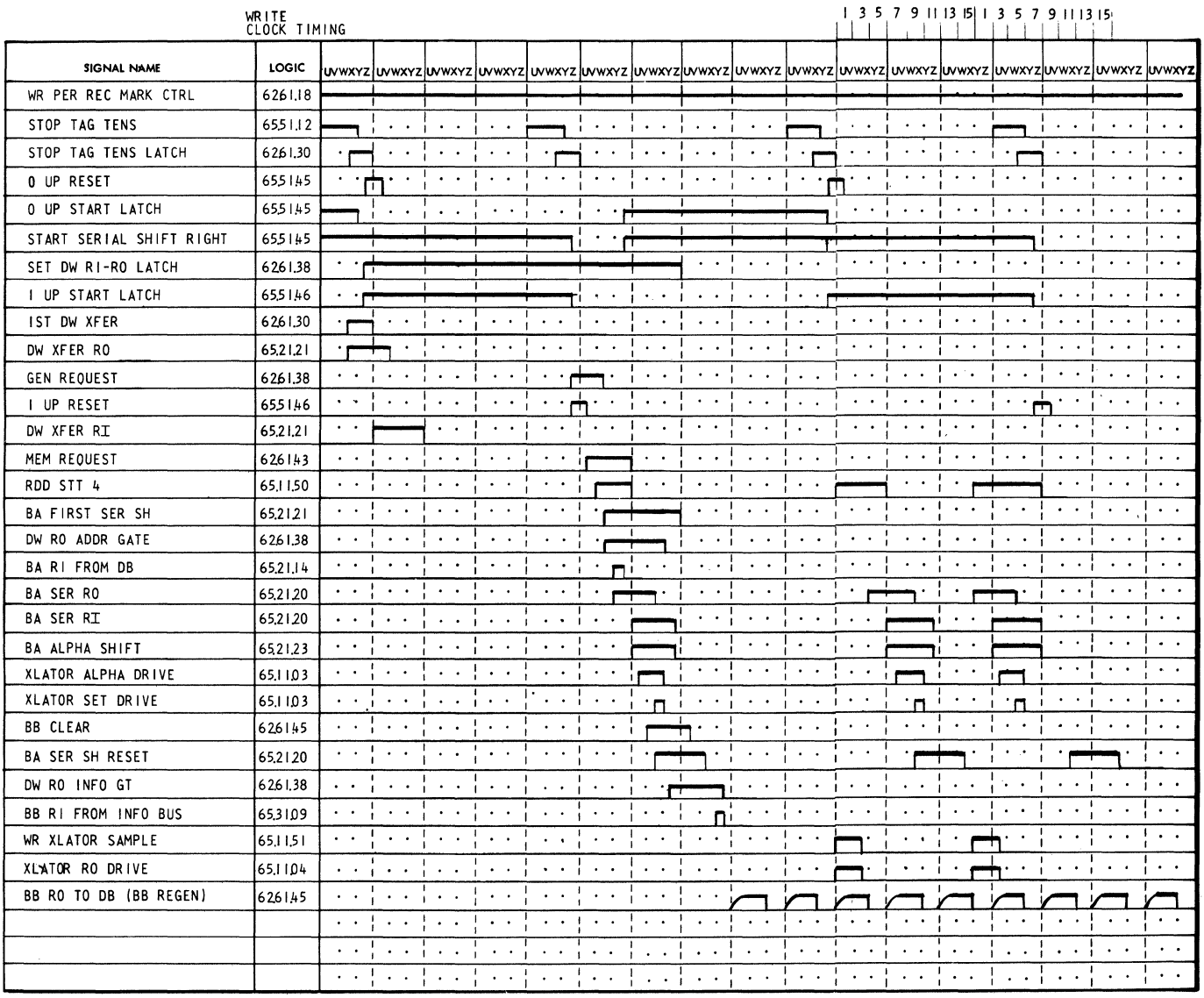


FIGURE 3.2-9. WRITE PER RECORD MARK CONTROL (FIRST AND SECOND DW CYCLE)

Command	Timing	Logic
Set DW RI-RO	First Word L, 0-up Reset, Z-V, Mismatch	4G-62.61.34
Set 1st DW Xfer	Stop Tag Tens, 0-up Stt, First Word L	5F-62.61.30
Set DW Xfer RO	1st DW Xfer, W-Y	3A-65.21.21
1-up Reset	Stop Tag Tens, 1-up Stt, No 0-up Stt, Z-V	4G-65.51.46
Set Generate Request	No SSR Gt, DW RI-RO, No Addr & No Info Gt	6C-62.61.38
Set DW Xfer RI	DW Xfer RO, U-W	3E-65.21.21
Request Memory	Gen Request, V-X	2B-62.21.43
Set Rd Stt 4	DW Xfer RI, No Mode Chg, First Word, V-X	3E-65.11.50
Set BA First Ser Sh	DW Xfer RI, X-Z	3F-65.21.21
Set DW RO Addr Gt	DW RI-RO L, Addr Gate, Write Ctrl	4G-62.61.38
BA RI from DB	DW Xfer RI, Write Ctrl	4A-65.21.27
Set BA Ser RO	Rd Stt 4, Y-U	2A-65.21.20
Set BA Ser RI	BA Ser RO, U-W	4A-65.21.20
Set BA Alpha Sh	Alpha Ctrl, BA Ser RI	5C-65.21.23
Xlator Alpha Drive	BA Ser RI, Alpha Ctrl	2A-65.11.03
Xlator Set Drive	BA Ser RI, Tp Write, X Pulse	2G-65.11.03
BB Clear	DW RO Addr Gt, W-Y	2C-62.61.45
BA Ser Sh Reset	BA Ser RI, X-Z	4H-65.21.20

Command	Timing	Logic
DW RO Info Gt	DW RI-RO, Info Gt, Write Ctrl	4J-62.61.38
Reset First Ser Sh	Ser Sh Reset, No Mode Chg, Z-V	3H-65.21.21
Set IB RI Gate	DW RO Info Gt	5F-62.61.45
BB RI from IB	IB RI Gate, Y-Pulse	6F-65.31.09
BB RO to DB (Regen)	No DW Xfer RI, No ISW RI Info, No CW Xfer RI,	5H-62.61.45
Read-Out First Alpha Character to TAU		
Set Wr Xlator Sample	Wr Clock 1 Pulse	3D-65.11.51
Xlator RO Drive	Wr Xlator Sample	3D-65.11.04
Set Rd Stt 4	Wr Xlator Sample, No Mode Chg	3D-65.11.50
Set BA Ser RO	Stt 4, Y-U	2A-65.21.20
Set BA Ser RI	BA Ser RO, U-W	4A-65.21.20
BA Alpha Shift	Alpha Ctrl, BA Ser RI,	5C-65.21.23
Reset Block 1-up Start	No BA First Ser Sh, BA Ser RO, Z-V	2C-62.61.87
Develop 1-up Start SSR Gate	1-up Start, No Block 1-up Stt	6E-65.51.46
Xlator Alpha Drive	BA Ser RI, Alpha Ctrl	2A-65.11.03
Xlator Set Drive	BA Ser RI, Tp Wr, X Pulse	2G-65.11.03
BA Ser Sh Reset	BA Ser RI, X-Z	4H-65.21.20

Sense a Record Mark (Figure 3.2-10)

When the buffer A tag is sensed, the BA last serial shift latch is turned on to signify that one more left-shift is needed to clear the buffer A register. As a write clock pulse is furnished from TAU, the alpha character is read out of the translator, and the last character is read out of buffer A into the translator.

With the last character in the translator, a Data Word Xfer Cycle is initiated to transfer the data word from buffer B to buffer A. At the same time, a data word request is initiated to read in a new data word into buffer B.

As the contents of buffer B is placed onto the distributor bus and regenerated, an alpha 80's code is sensed and the record mark latch is turned on. With a record mark sensed, the mismatch latch is turned off, and the match latch is turned on.

With the record mark sensed, the CW sign is analyzed to determine the next step of the operation. As the last character in the next to last word is read out of buffer A, and the word containing the record mark is transferred from BB to BA, a set control word read-out cycle is developed. The CW RO Cycle reads out a new control word into the record definition register and the write-per-record-mark operation continues.

If a minus control word sign is sensed, the end-of-record delay latch is turned on, and the normal end of a write operation is performed.

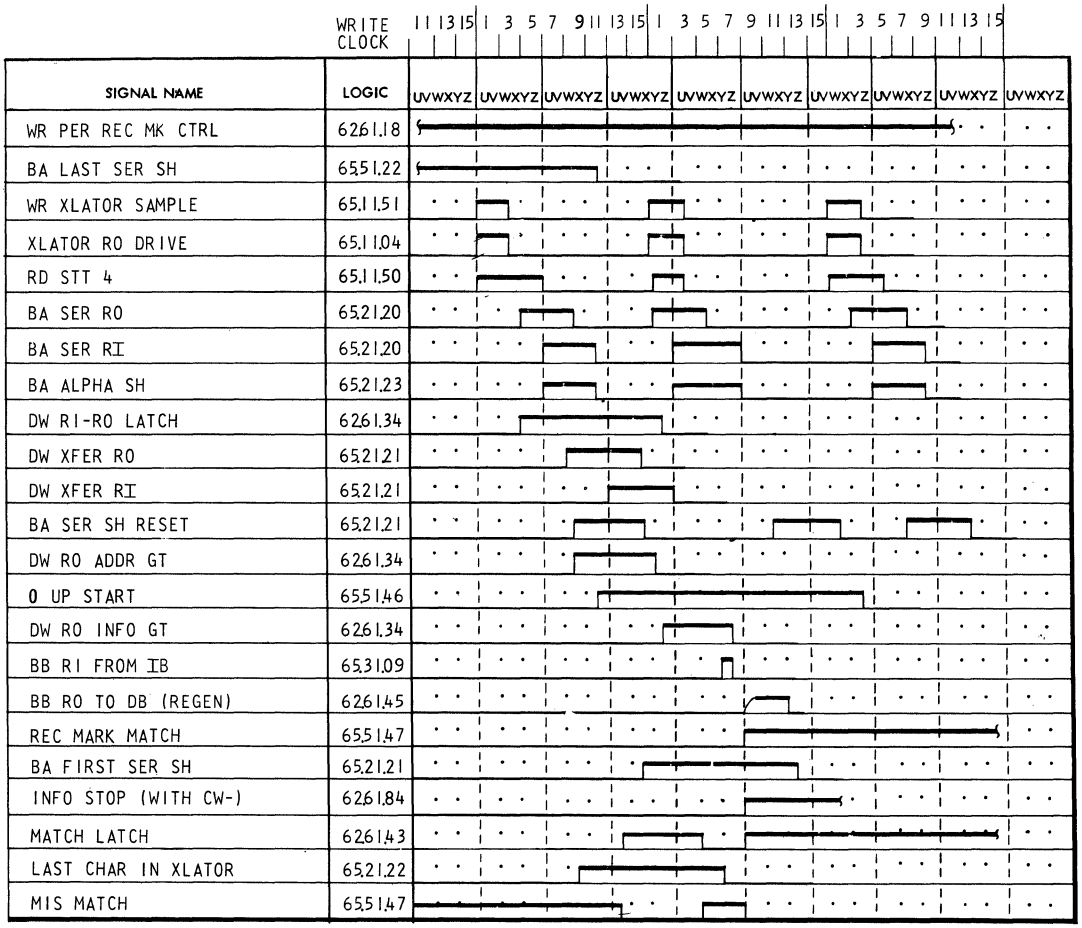


FIGURE 3.2-10. WRITE PER RECORD MARK CONTROL (RECORD MARK SENSE)

Sense a Record Mark

Command	Timing	Logic
Set Record Mark Latch	Rec Mk Ctrl, Alpha Sign, DB 9 P 2 & 1 Bit, DB 8 P 6 & 2 Bit	3B-65.51.47
Reset Mis-Match Latch	Rec Mk Match	65.51.43
Set Match Latch	Rec Mk Match	65.51.43

Record Mark With CW Sign Plus

Command	Timing	Logic
Set Control Word RO	BA Last Ser Sh, Z-V, CW Plus, Write Ctrl, Match, BA Ser RO	3H-62.61.34

Record Mark With CW Sign Minus

Command	Timing	Logic
Set End of Record Delay	CW Sign Minus, DW Xfer RI, Rec Mk Match, No Seq A or B	3C-62.61.70
Wr End of Record	EOR Delay, BA Last Ser Sh, BA Ser RO L	2C-62.61.71

3.2.03 Write With Zero Elimination (Figures 3.2-11, 12, and 13)

The write-with-zero elimination enables each numeric word written to have as many as five leading zeros eliminated. Alpha words are written in their normal mode, five characters per word. The write-with-zero elimination is performed as a normal write operation. The main difference is in the sampling of positions 0-4 for zeros (2 & 1 bits). The sampling is done as the contents of buffer B is transferred to buffer A.

The write-with-zero elimination is performed under control of the start and stop registers. All other phases, such as the initial status word, control word, data word and final status word, are performed in the same manner as previously described. The following explanation deals with the controls that are directly affected during a write-with-zero elimination operation.

As the contents of buffer B are parallel transferred to buffer A (via the distributor bus) the five high-order positions are sampled for zeros. Assume that the first 3 positions (0, 1, 2) have zeros. This signifies that the first significant digit is located in position 3. With a significant digit sensed, the third position zero detect latch is turned on. The turn-on of any one of the detection latches automatically inhibits the normal position 0 write control.

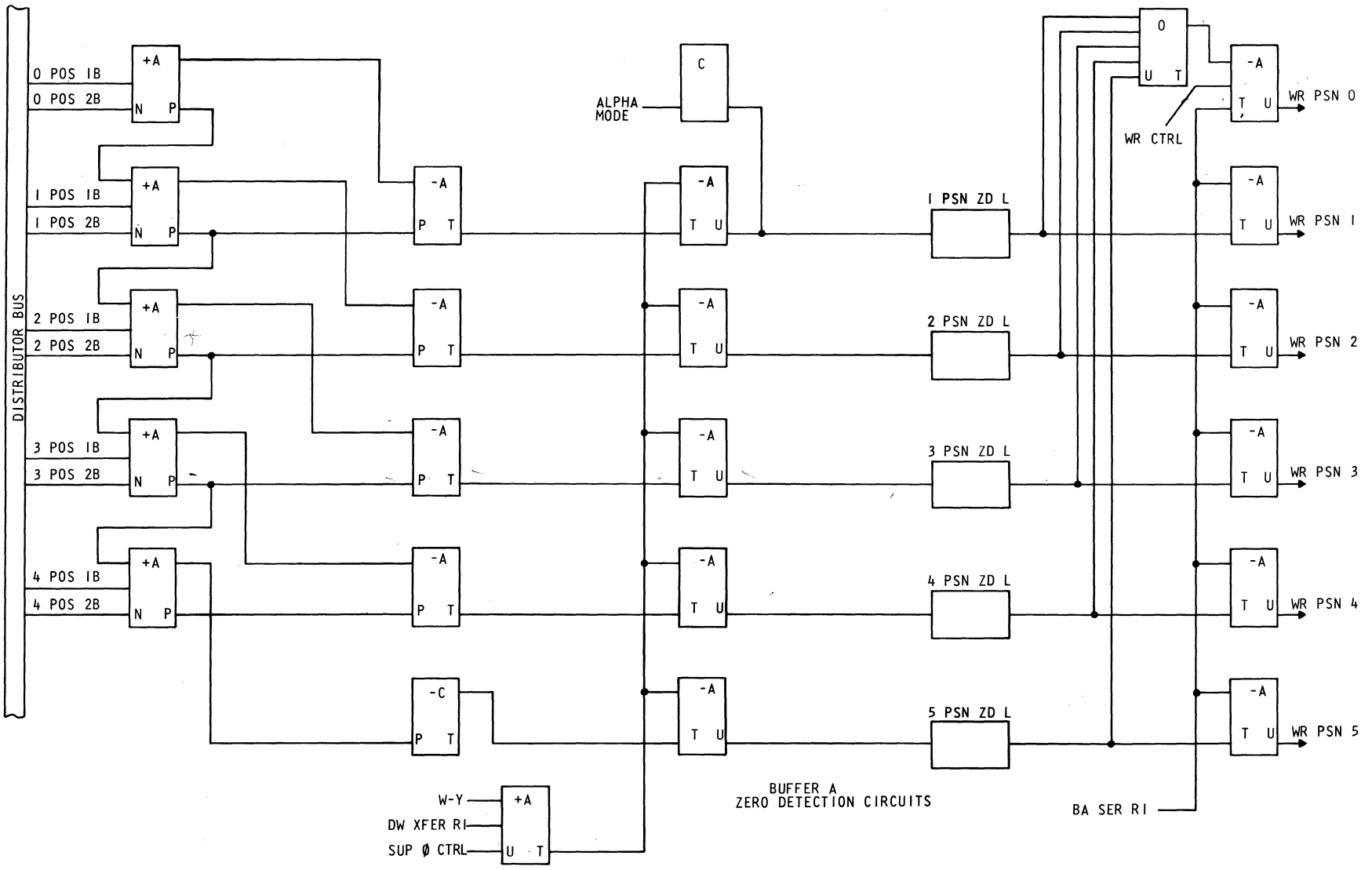


FIGURE 3.2-11. BUFFER A ZERO DETECTION CIRCUITS

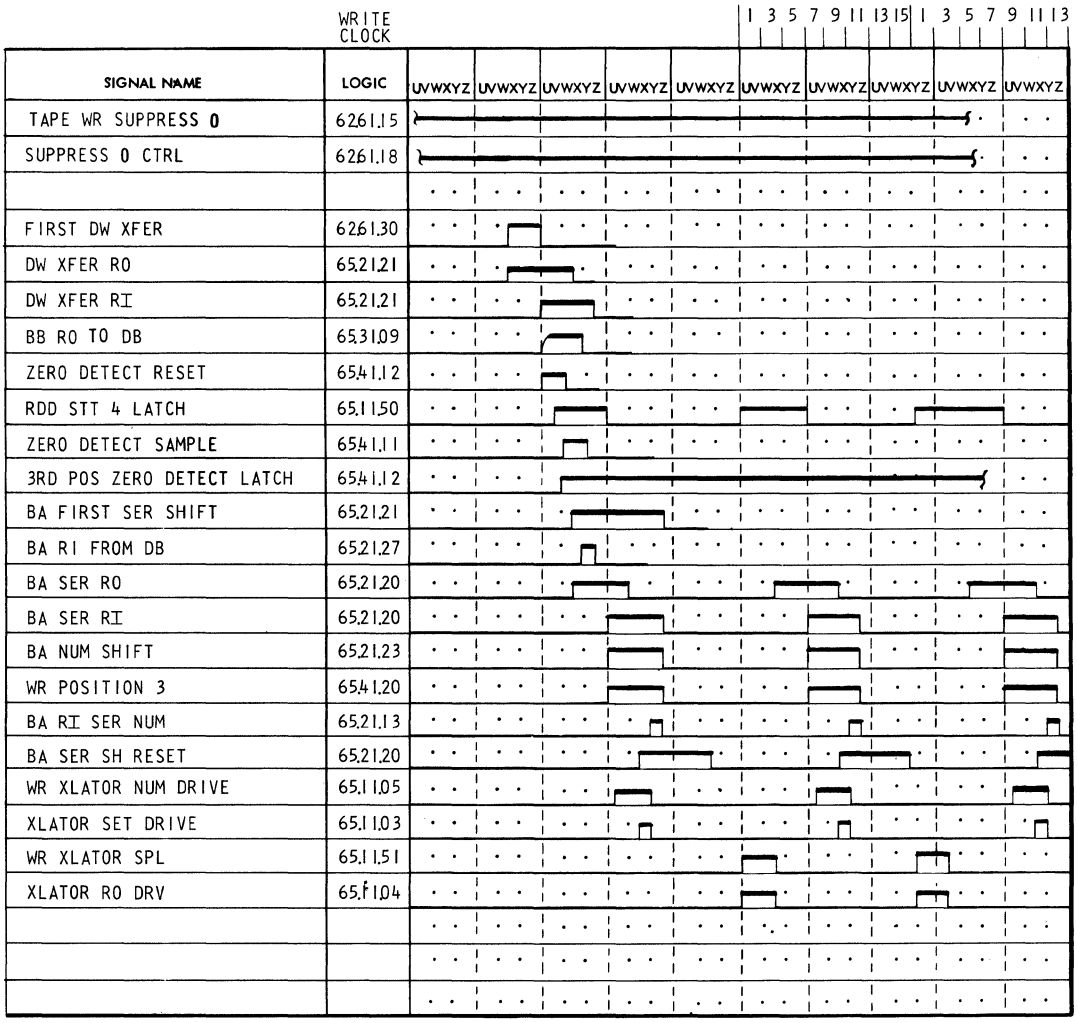


FIGURE 3.2-12. WRITE WITH ZERO ELIMINATION (NO MODE CHANGE)

If more than five leading zeros are detected, the fifth position zero detection latch is turned on. This latch is used to insure that only five high-order zeros are eliminated.

At the same time the zeros are being sampled, the sign position is analyzed for an alpha or numeric word. If an alpha word is sensed, the first position detect latch is turned on which signifies that position 1 of buffer A, along with position 0, are read out to the translator.

For this explanation, assume a numeric word is to be written. Because this is the first word of a record, a mode change is sensed. With a mode change sensed, a mode change character must be written on tape prior to the first character of the numeric word.

The first write clock 1 pulse causes the mode change character to be written. At the same time, the Rd Start 4 latch is turned on to bring up the controls to left-shift the contents of buffer A and read in the first character into the translator.

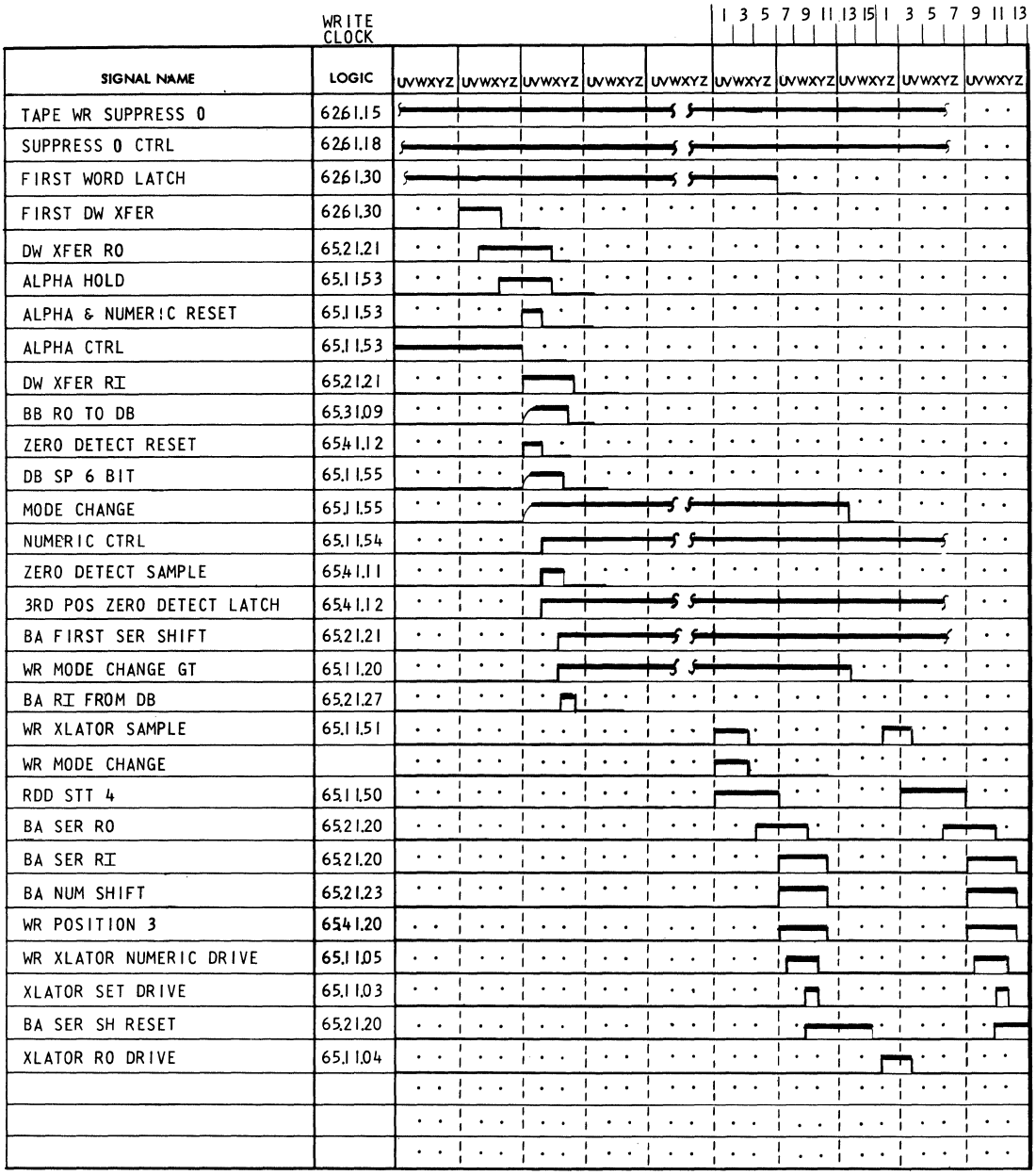


FIGURE 3.2-13. WRITE WITH ZERO ELIMINATION (MODE CHANGE)

The output of the buffer A Serial RI latch is switched with the static output of the position 3 zero detect latch. This develops the write position 3 gate, which allows the contents of position 3 to be the first character read into the translator.

With zeros in the first three positions, a left-shift of 7 places is needed to clear the register. The end-of-the-zero-detect operation is sensed when the tag advances into the third position of buffer A.

When the tag is sensed, the normal sign over units operation is performed, and the next data word is analyzed for zeros and placed into the buffer A register.

Command	Timing	Logic
Set First DW Xfer	0-up Stt, Stop Tag Tens, First Word	5F-62.61.30
Set DW Xfer RO	First DW Xfer, W-Y	3A-65.21.21
Set Alpha Hold	DW Xfer RO, X-Z, Tp Wr, Alpha Ctrl	6J-65.11.53
Reset Alpha & Numeric Ctrl	DW Xfer RO, Tp Wr, U-W	3F-65.11.53
Set DW Xfer RI	DW Xfer RO, U-W	3E-65.21.21
Reset Zero Detect	DW Xfer RO, U-W	4G-65.41.12
Sense Mode Change	DB 6 Bit, DW Xfer RI, Alpha Hold	3B-65.11.55
Set Numeric Latch	DB 6 Bit, DW Xfer RI, W-Y	3D-65.11.54
Zero Detect Sample	DW Xfer RI, Sup 0 Ctrl, W-Y	3B-65.41.11
Set PSN 3 Zero Detect Latch	Zero Detect Sample, 3 PSN Zero Detect	3A-65.41.12
Set BA First Ser Sh	DW Xfer RI, X-Z	3F-65.21.21
Set Wr Mode Chg Gate	Mode Chg, No Last Char, BA First Ser Sh	3G-65.11.20
BA RI from DB	DW Xfer RI, Write Ctrl	4A-65.21.27
Set Wr Xlator Sample	Write Clock 1 Pulse	3D-65.11.51
Set Rd Stt 4	Wr Xlator Sample, No Hang up Error	4D-65.11.50
Set BA Ser RO	Rd Stt 4, Y-U No DS Write	2A-65.21.20
Set BA Ser RI	BA Ser RO, U-W	4C-65.21.20

Command	Timing	Logic
BA Num Shift	BA Ser RI, Num Ctrl, Any Tp Data	5D-65.21.23
Wr PSN 3	BA Ser RI, 3 PSN Z D L	4H-65.41.20
Xlator Num Drive	BA Ser RI, Numeric Ctrl, U-Y	3A-65.11.05
Xlator Set Drive	BA Ser RI, Tp Write, X	2G-65.11.03
BA Ser Sh Reset	BA Ser RI, X-Z	4H-65.21.20

3.2.04 Write-Per-Record-Mark Control With Zero Elimination

The write-per-record-mark control with zero elimination is a combination of the write-per-record-mark and the write-with-zero-elimination operations.

This code enables the programmer to perform both of these codes with one instruction. However, the operations are independent of one another and are under control of the sign control latches.

If an alpha sign is present, the write-per-record-mark operation is performed in the same manner as explained under section 3.2.02.

With a numeric sign sensed, the write-with-zero-elimination operation is performed in the same manner as explained under section 3.2.03.

3.2.05 Write Tape Mark (Figure 3.2-14)

The write tape mark instruction is defined by a digit 0 in position 5 and a 0001 in position 6-9 of the tape instruction. The tape mark is written as an 8421 and is used as a group mark for indicating a tape record.

Because the write tape mark operation can be used to signal a priority, both the initial and final status word cycles are developed. During the write tape mark operation, the control word and data word cycles are inhibited.

The final status word is performed slightly different from the normal manner. The control register and start register are inhibited from being placed into the final status word. The only change in the final status word is the insertion of the condition latch.

With the channel control unit interlocked and A&P restarted, a write tape mark call signal is developed and sent to TAU. The turn on of the write tape mark trigger conditions the tape controls to advance the tape and write the tape mark character. The tape mark signal conditions the disconnect trigger which causes a normal write disconnect cycle.

At the completion of the write tape mark operation, a read disconnect cycle occurs to check the validity of the tape mark and send a read disc signal (RDD 136) to the synchronizer. The RDD 136 signal is used to develop the final status word cycle.

As mentioned previously, the final status word is performed in the normal manner with the exception of the reading out of the control register and start register. The inhibiting of the read out of these registers is accomplished by the use of the decoder B gate.

The following is a listing of the controls that are directly affected during the write tape mark operation. For the initial status word and final status word sequence, refer to Figures 3.1-3 and 3.1-9.

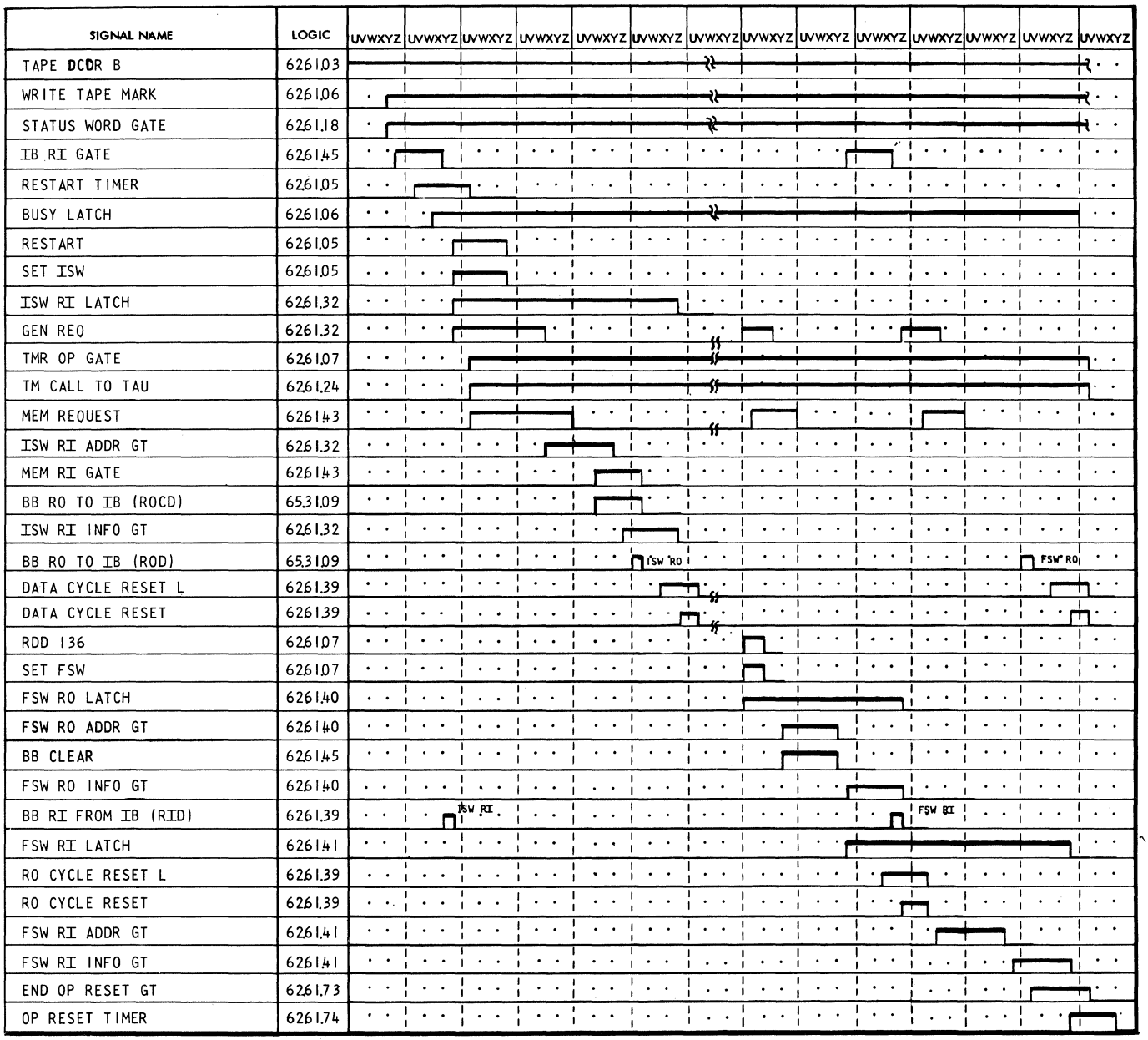


FIGURE 3.2-14. WRITE TAPE MARK

Command	Timing	Logic
Set DCDR B	Fld Reg 2 & 1 Bit, Tape Call	5F-62.61.02
Set Wr Tm Call	OP Reg 0 & 1 Bit, DCDR B	4C-62.61.06
Inhibit Xlator RO	Wr Tape Mark	65.11.04
Inhibit CR and Stt Reg RO to DB	FSW RI Latch, Addr Gt, No DCDR R or A	3F-65.51.06

3.2.06 Write Segment Mark (Figure 3.2-15)

The write tape segment instruction is defined by a digit 0 in position 5 and a 0005 in position 6-9 of the tape instruction. The segment mark is written as a CA 8421 and is used to indicate logical segments within a group of tape records. For example, a sixty-word alpha or numeric record could be broken up into six groups of ten words each. At the completion of each of these groups, a segment mark is written to indicate the group.

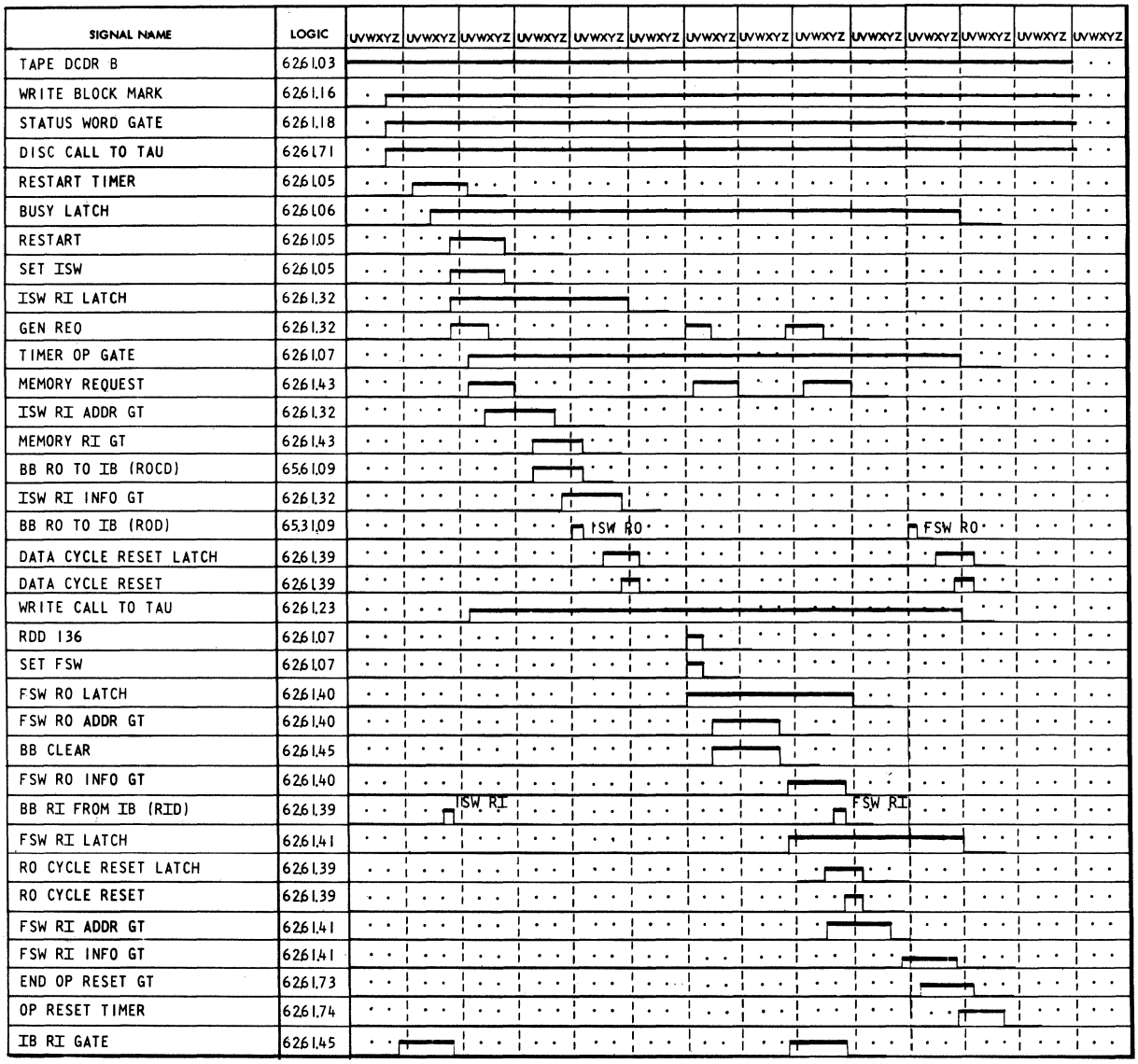


FIGURE 3.2-15 WRITE SEGMENT MARK

Special tape instructions are provided to cause the tape to be moved forward or backward over a specified number of segment marks.

Because the write segment mark operation can be used to signal a priority, both the initial and final status word cycles are developed. During the write segment mark operation, both the control word and data word cycles are inhibited.

The final status word is performed in a slightly different manner because the control register and start register are inhibited from being placed into the final status word. The only change in the final status word is the insertion of the condition latch.

The initial status word is performed in the normal manner as previously described. The main difference between this operation and the normal write operation is the development of the disconnect signal at the beginning of the operation. The disconnect call signal is sent to TAU to indicate that a one-character record is to be written.

With the synchronizer interlocked and A & P restarted, a write call signal is developed to turn on the write controls in the tape adapter unit.

When the tape drive is up to speed, TAU furnishes a write clock 1/8 pulse to the channel control unit to develop a write sample pulse. The write sample pulse is sent back to TAU to condition the read-write registers.

A read disconnect operation occurs after the normal write operation, to check the validity of the segment mark and to develop a disconnect signal (RDD 136). This signal is sent to the channel control unit to develop the final status word cycle.

The final status word is performed in the normal manner with the exception of the reading out of the control register and start register. The inhibiting of the read out of these registers is accomplished by the use of the decoder B gate.

The following is a listing of the controls that are directly affected during the write segment operation. For the ISW and FSW sequence of events, refer to Figure 3.1-3 and 3.1-9 or to the ISW and FSW write up under section 3.1.01.

Command	Timing	Logic
Set DCDR B	Fld Reg 2 & 1 Bit, Tape Call	5F-62.61.02
Set Wr Blk Mk	Op Reg 3 & 2 Bit, DCDR B	4G-62.61.16
Set Disc Call	Wr Blk Mk	3B-62.61.71
Inhibit Xlator RO	Wr Blk Mk	3B-65.11.04
Inhibit CR and Stt Reg RO to DB	FSW RI Latch, Addr Gt, No DCDR A or R	3F-65.51.06

3.3.00 TAPE MOVEMENT CODES

The tape movement codes are defined by a digit 0 in position 5 of the tape instruction. When a digit 0 is sensed, it signifies that the data address portion of the tape instruction further defines the instruction. There are six tape movement instructions specified by the data address:

0000	tape select
0002	rewind
0003	rewind unload
0004	backspace
0006	skip
0007	turn off end of file

Each tape-movement instruction is performed in a similar manner. The main differences are in the op register selection and the conditions which release the synchronizer interlock. Figure 3.3-1 shows the controls that are needed to perform the various movement operations.

3.3.01 No-Op Select (0000) (Figure 3.3-2)

The tape select operation is used to select the tape drive that is specified by position 4 of the tape instruction. The selected tape drive must be at its load point to release the synchronizer interlock.

The actual test on the availablity of the tape synchronizer is performed by the + 51 code (branch busy code). With the selected synchronizer busy, the data portion of the branch code specifies the location of the next instruction. If a not-busy is sensed, the next instruction is taken from the instruction Counter.

Objectives:

1. Analyze the tape instruction
2. Condition selected synchronizer
   a. Determine tape movement instruction (62.61.02)
   b. Reset synchronizer controls (62.61.03)
   c. Clear Buffer B (62.61.45)
3. Transfer instruction word to buffer B (62.61.45)
4. Determine tape operation (62.61.04)
   a. Select tape drive (62.61.04)
   b. Select op registers (62.61.04)
5. Prevent initial status word development (62.61.18)
6. Develop synchronizer interlock (62.61.06)
7. Prevent op reg and sel reg selection (62.61.04)
8. Restart A & P (62.61.05)
9. Develop no-Op select call (62.61.24)
10. Release synchronizer interlock (62.61.72)

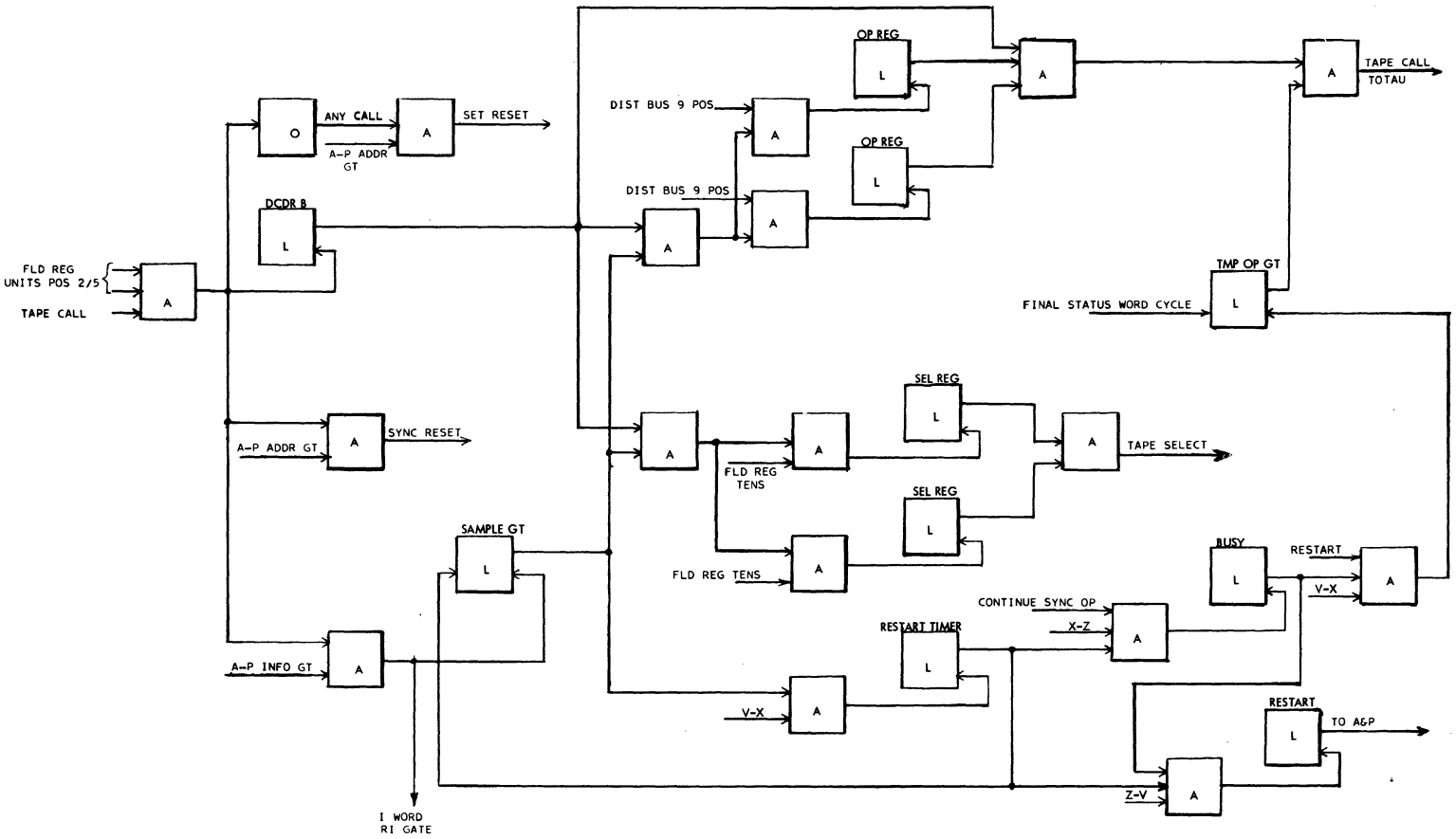


FIGURE 3.3-1. DECODER B CONTROLS

1. Analyze the Tape Instruction

The beginning of each tape operation is analyzed for an index operation and an interrupt routine.

When an 80's code is sensed, the index portion (positions 2 and 3) is analyzed to determine if an index operation is to be performed. At the completion of the index operation, the stacking latches are sampled to see if an interrupt request has been previously made for the addressed combination of tape drive and synchronizer.

If the stacking latch had been set from a previous operation, the tape synchronizer is not interlocked, and the A&P does not advance to the next program step The A & P continues to test the stacking latch until a no-interrupt reply is sensed.

If, at the beginning of the tape operation, a no-index and a no-interrupt reply is sensed, the specified synchronizer is interlocked, and the instruction counter is updated. This allows the tape operation to proceed immediately so that the A & P can advance to the next program step.

2. Condition Selected Synchronizer

The units position (position 1) of the operation code is analyzed in A & P to determine whether the tape call signal is to be developed for synchronizer 1 or 2.

a. Determine Tape Movement Instruction. The tape call signal is sent to the specified synchronizer where it is switched at 5F (62.61.02) with the static output of the field register units position (position 5) to develop the tape call B and any-tape call signals.

   The tape-call signal is used to turn on the Tape Decode B latch at 3E (62.61.03). The DCDR B latch signifies that the data portion of the instruction further defines the tape operation.

b. Reset Synchronizer Controls. When the data request signal is developed in A & P, an address gate and an information gate are sent to the tape synchronizer.

   The address gate signal is used to form the coincidence at 4D (62.61.14) with a No CE Op and Any Tape Call to develop the Reset Sync and the Select Reset signals. These signals are used to reset the synchronizer controls that were used in the previous operation.

c. Clear Buffer B. Prior to the transferring of the Program Register D, I Counter, and Op Register, the buffer B register must be reset. This is accomplished by switching the Reset Sync signal with a V - X pulse to turn on the buffer B clear latch (4A-62.61.45).

   The output of the buffer B clear latch is used to prevent the buffer B register from reading out to the distributor bus at U-time. Because the distributor bus capacitors were not charged at U-time, the reading in at Y-time produces a blank register.

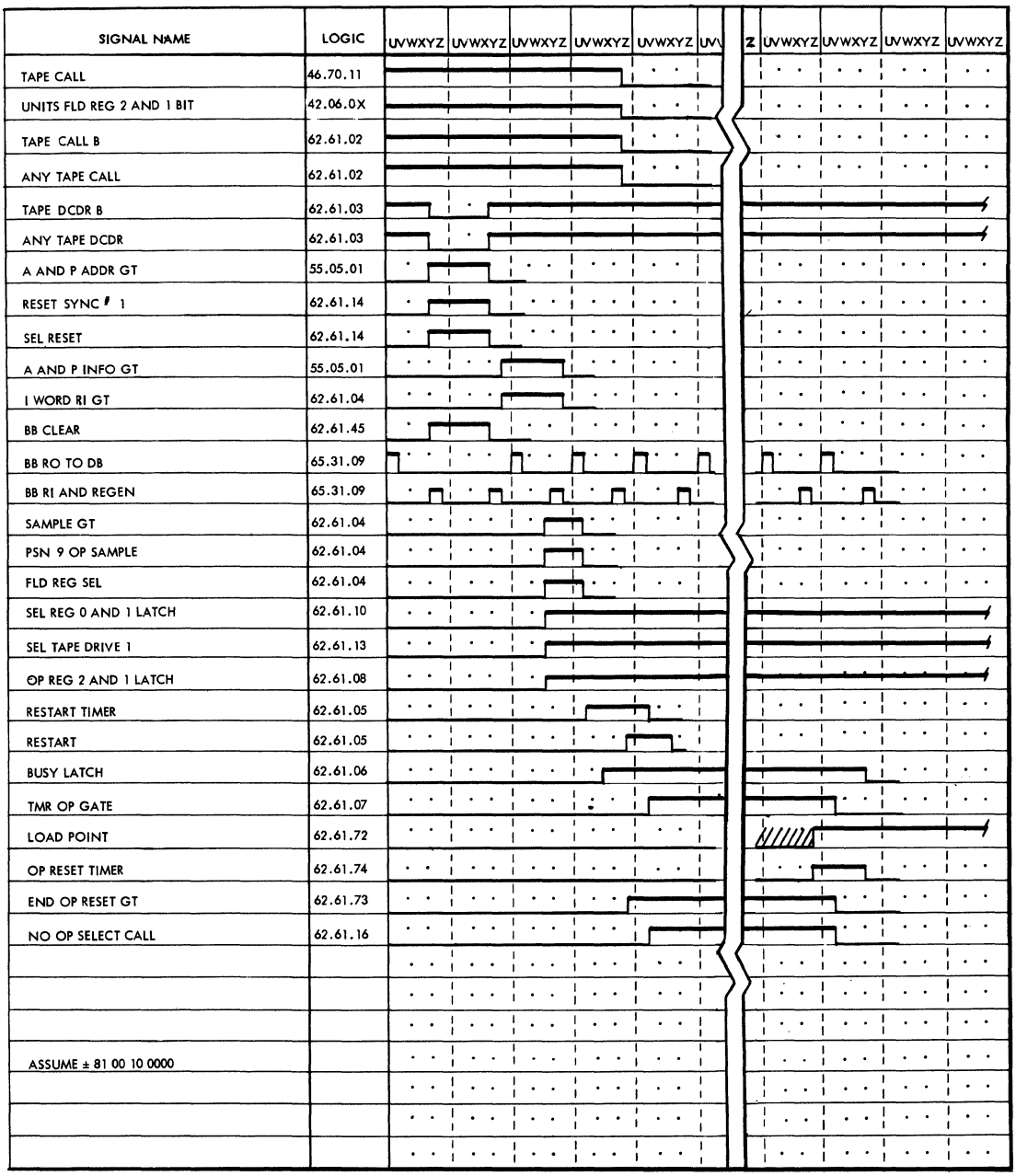


FIGURE 3.3-2. NO OP SELECT

3. Transfer Instruction Word to Buffer B

During A & P information gate time, the contents of the program register D, I counter, and Op Register are parallel-transferred onto the information bus at U-time. The contents of the information bus is then read into the buffer B register at Y-time.

The reading into the B B register is accomplished by switching the information gate, Any Tape Call and a No CE Op signal at 4B (62.61.04). The coincidence of these signals forms the I Word RI gate, which is used to develop the IB RI gate (62.61.45). The IB RI gate is switched with a Y-pulse to turn on the read-in driver. This allows the contents of the information bus to read into the buffer B register.

4. Determine Tape Operation

To analyze the tape instruction, the sample gate latch must be turned on. This is accomplished by switching the I word RI gate with a X - Z pulse at 3D (62.61.04).

a. Select Tape Drive. The sample gate output is switched with Any TP DCDR at 4J (62.61.04) to develop the field register select sample pulse. This pulse is, in turn, gated with the static output of field register, tens position, to turn on the specified select register latches. The output of these latches is used to condition the selected tape drive unit.

b. Select Op Registers. To determine the No-Op Code, position 9 of the B B register must be sampled. To accomplish this, the sample gate is switched with Tape DCDR B at 4H to develop Position 9 Op Sample gate (62.61.04).

As the Buffer B register is read out to the distributor bus during the regen cycle, the 9's position 2 and the 1-bit Op Register latches are on (62.61.08). The output of these latches is used to develop the No-Op Select signal (62.61.16).

5. Prevent Initial Status Word (ISW) Development

During the No-Op Select operation, the storing of the initial status word (ISW) is prevented by inhibiting the development of the status word gate. The status word gate is developed when the Tape DCDR A signal is up, or during a write tape mark, or block mark operation (62.61.18).

6. Develop Synchronizer Interlock

Before A & P can be restarted, the tape synchronizer must be interlocked. To accomplish this, the sample gate is switched with a V - X pulse at 3A (62.61.05) to turn on the restart timer latch. The restart timer latch is used to form the coincidence at 2G with a Continue Sync Op and a X - Z pulse to turn on the Busy latch (62.61.06). The Busy latch remains on until the operation is completed.

7. Prevent Op Reg and Sel Reg Selection

The restart timer latch coming on prevents the development of another tape select

and op select. The restart timer latch is used to reset the sample gate at Z - V time (2E-62.61.04). With the sample gate reset, the field register sample and the Position 9 Op Sample signals are turned off.

8. Restart A & P

With the Synchronizer Busy latch turned on, the restart timer latch and a Z - V pulse form the coincidence at 2D to turn on the restart latch (62.61.05). The output from this latch is used to restart the A & P.

9. Develop No-Op Select Call

Before the No-Op Call can be developed and sent to TAU, the Timer Op gate must be turned on. The Timer Op gate allows a delay that insures that the synchronizer is interlocked and A & P is restarted. The switching to accomplish this can be found on Logic 62.61.07, Switch 3J.

The output of the Timer Op gate is switched at 4G (62.61.24) with a No-Op Select signal to develop the No-Op Select Call.

10. Release Synchronizer Interlock

The synchronizer interlock is released after the load point indication is sensed from the tape drive unit. With the load point sensed on the selected tape drive and the No-Op Select signal up, the coincidence is formed at 4B (62.61.72) to develop the Set-Op Reset gate. The Set-Op Reset gate is switched with a Z - V pulse and an End-Op Reset gate at 4E (62.61.74) to turn on the Op Reset Timer. The output of this latch is used to reset the Busy latch which releases the tape synchronizer.

If the selected tape drive unit was not at its load point, the Busy latch would remain on allowing the synchronizer to stay interlocked.

The Op Reset Timer signal is also used to reset the Timer Op Gate, which in turn causes the No-Op Select Call signal to be dropped (62.61.24).

3.3.02 Rewind (0002) (Figure 3.3-3)

The rewind instruction causes the specified tape unit to rewind its tape. Before a rewind operation can be accomplished, the tape unit is automatically placed in read status.

The synchronizer is released the moment that a Sel and Rewind signal is sent back to the synchronizer from the tape adapter unit. This signal effectively disconnects the tape unit from A & P, allowing the particular synchronizer to be programmed.

When the specified tape unit reaches its load point, the tape unit ready light turns on and the unit is again available for use by the program.

Objectives:

1. Analyze the tape instruction.
2. Condition selected synchronizer
   a. Determine tape movement instruction (62.61.02)
   b. Reset synchronizer controls (62.61.03)
   c. Clear buffer B (62.61.45)
3. Transfer instruction word to buffer B (62.61.45)
4. Determine tape operation (62.61.04)
   a. Select tape drive (62.61.04)
   b. Select op registers (62.61.04)
5. Prevent initial status word development (62.61.18)
6. Develop synchronizer interlock (62.61.06)
7. Prevent op reg and sel reg selection (62.61.04)
8. Restart A & P (62.61.05)
9. Develop rewind call (62.61.24)
10. Release synchronizer interlock (62.61.72)

1. Analyze the Tape Instruction

The beginning of each tape operation is analyzed for an index operation and an interrupt routine. When an 80's code is sensed, the index portion (position 2 and 3) is analyzed to determine if an index operation is to be performed. At the completion of the index operation, the stacking latches are sampled to see if an interrupt request has been previously made for the addressed combination of tape drive and synchronizer.

If the stacking latch had been set from a previous operation, the tape synchronizer is not interlocked and A & P does not advance to the next program step. The A & P continues to test the stacking latch until a no-interrupt reply is sensed.

If, at the beginning of the tape operation, a no-index and a no-interrupt reply is sensed, the specified synchronizer is interlocked, and the instruction counter is updated. This allows the tape operation to proceed immediately and A & P advances to the next program step.

2. Condition Selected Synchronizer

The units position (Position 1) of the operation code is analyzed in A & P to determine whether the tape-call signal is to be developed for synchronizer 1, or 2.

a. Determine Tape Movement Instruction. The tape-call signal is sent to the specified synchronizer where it is switched at 5F (62.61.02) with the static output of the field register units position (position 5) to develop the Tape Call B and Any Tape-Call signals.

   The tape-call signal is used to turn on the Tape Decoder B latch at 3E (62.61.03). The DCDR B latch signifies that the data portion of the instruction further defines the tape operation.

b. Reset Synchronizer Controls. When the data request signal is developed in A & P, an address gate and an information gate are sent to the tape synchronizer.

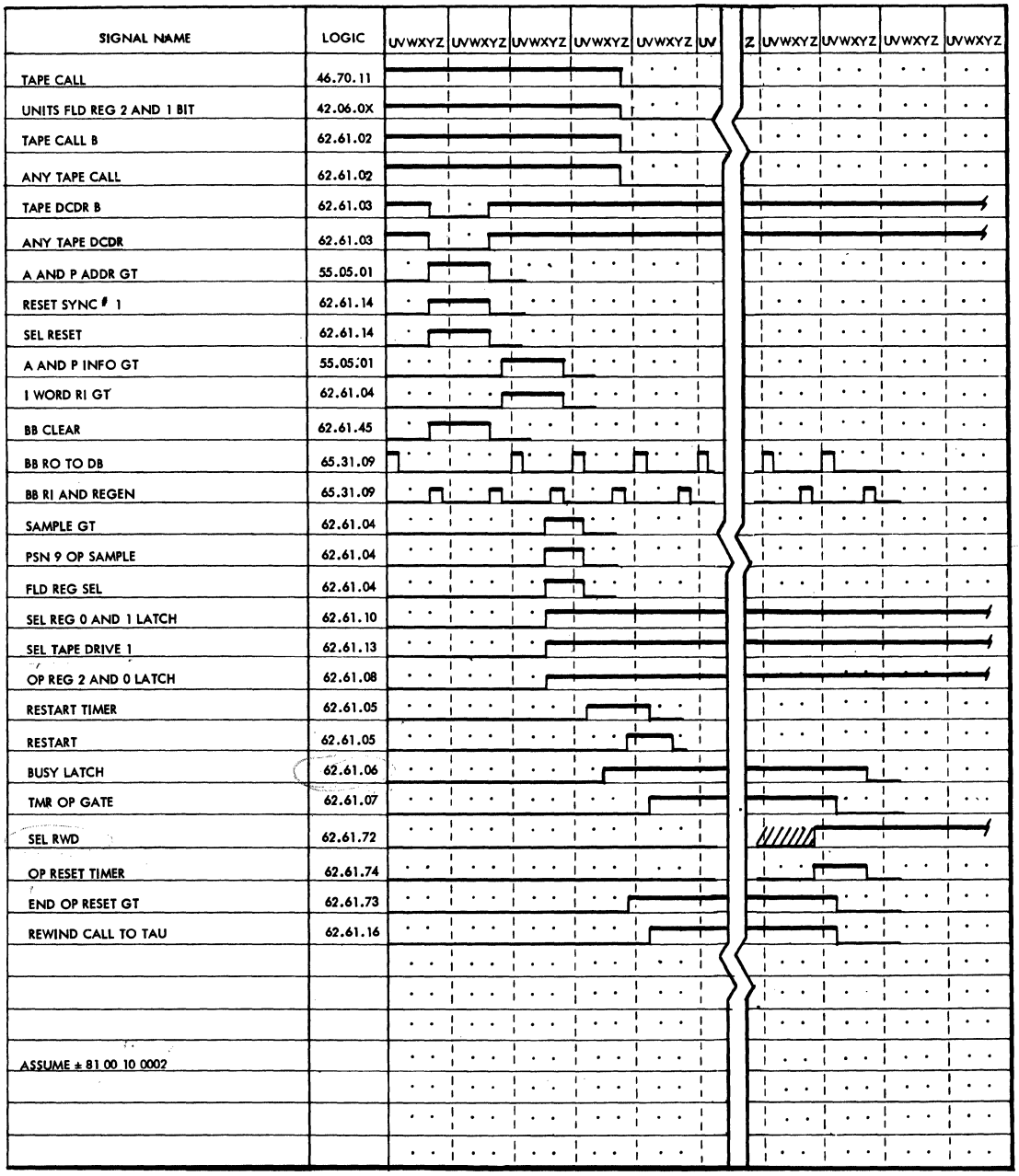


FIGURE 3.3-3. REWIND

The address gate signal is used to form the coincidence at 4D (62.61.14) with a No CE Op and Any Tape Call to develop the Reset Sync and the Select Reset signals. These signals are used to reset the synchronizer controls that were used in the previous operation.

c. Clear Buffer B. Prior to the transferring of the Program Register D, Instruction Counter, and the Op Register, the buffer B register must be reset. This is accomplished by switching the Reset Sync signal with a V - X pulse to turn on the buffer B Clear latch (4A-62.61.45).

The output of this latch is used to prevent the buffer B register from reading out to the distributor bus at U-time. Because the distributor bus capacitors were not charged at U-time, the reading-in at Y-time produces a blank register.

3. Transfer Instruction Word to Buffer B

During A & P Information Gate time, the contents of the Program Register D, Instruction Counter, and Op Register are parallel-transferred onto the information bus at U-time. The contents of the information bus is then read into the buffer B register at Y-time.

The reading into the B B register is accomplished by switching the information gate, any tape call, and a No CE Op signal at 4B (62.61.04). The coincidence of these signals forms the I Word RI gate which is used to develop the IB RI gate (62.61.45). The IB RI gate is switched with a Y-pulse to turn on the read in driver. This allows the contents of the information bus to read into the buffer B register.

4. Determine Tape Operation

To analyze the tape instruction, the sample gate latch must be turned on. This is accomplished by switching the I word RI gate with a X - Z pulse at 3D (62.61.04).

a. Select Tape Drive. The sample gate output is switched with Any TP DCDR at 4J (62.61.04) to develop the field register select sample pulse. This pulse is, in turn, gated with the static output of field register tens position to turn on the specified select register latches. The output of these latches is used to condition the selected tape drive unit.

b. Select Op Register. To determine the rewind operation, Position 9 of the B B register must be sampled. To accomplish this, the sample gate is switched with Tape DCDR B at 4H to develop Position 9 Op Sample gate (62.61.04).

As the buffer B register is read out to the distributor bus during the regen cycle, the 9's position is sampled. Because the rewind code is specified as a 2 in the 9's position, the 2 and the 0-bit Op Register latches are on (62.61.08). The output of these latches is used to develop the rewind signal (62.61.16).

5. Prevent Initial Status Word Development

During the rewind operation, the storing of the initial status word is prevented. This is accomplished by inhibiting the development of the status word gate. The status word gate is developed when the Tape DCDR A signal is up, or during a write tape mark or block mark operation (62.61.18).

6. Develop Synchronizer Interlock

Before A & P can be restarted, the tape synchronizer must be interlocked. To accomplish this, the sample gate is switched with a V - X pulse at 3A (62.61.05) to turn on the restart timer latch. The restart timer latch is used to form the coincidence at 2G with a Continue Sync Op and a X - Z pulse to turn on the Busy latch (62.61.06). The Busy latch remains on until the operation is completed.

7. Prevent Op Reg and Sel Reg Selection

The Restart Timer latch coming on prevents the development of another Tape Select and Op Select. The restart timer latch is used to reset the sample gate at Z - V time (2E-62.61.04). With the sample gate reset, the field register sample and the Position 9 Op Sample signals are turned off.

8. Restart A & P

With the synchronizer Busy latch turned on, the restart timer latch and a Z - V pulse form the coincidence at 2D to turn on the restart latch (62.61.05). The output from this latch is used to restart A & P.

9. Develop Rewind Call

Before the rewind call can be developed and sent to TAU, the Timer Op gate must be turned on. The Timer Op gate allows a delay that insures that the synchronizer is interlocked and A & P is restarted. The switching to accomplish this can be found on Logic 62.61.07, Switch 3J.

The output of the Timer Op gate is switched at 4D (62.61.24) with a Rewind signal to develop the Rewind Call which is sent to TAU.

10. Release Synchronizer Interlock

The synchronizer interlock is released the moment the Select and Rewind signal is received from TAU. The tape drive remains in the rewind status until the load point is sensed.

The select and rewind signal is sent to the specified synchronizer where a coincidence is formed with the rewind call signal to turn on the Op Reset Timer latch (3C-62.61.74). The output of the Op Reset Timer latch is used to reset the Busy latch which releases the tape synchronizer.

The Op Reset Timer latch signal is switched with Any Tape DCDR at V - X time to develop a 2 usec pulse, which is used to reset the Timer Op Gate.

With the Timer Op Gate reset, the coincidence that was necessary to develop the rewind call signal is dropped (62.61.07).

3.3.03 Rewind Unload (0003)

The rewind unload operation functions in the same manner as the rewind, except that the specified tape unit is not available for programming at the completion of the rewind operation.

3.3.04 Backspace (0004) (Figure 3.3-4)

The backspace operation is used to move the tape backwards over one record. If the tape backspaces over a segment mark or a tape mark, this is considered as one record.

When a backspace operation is called for, the tape drive unit may be either in write or read status.

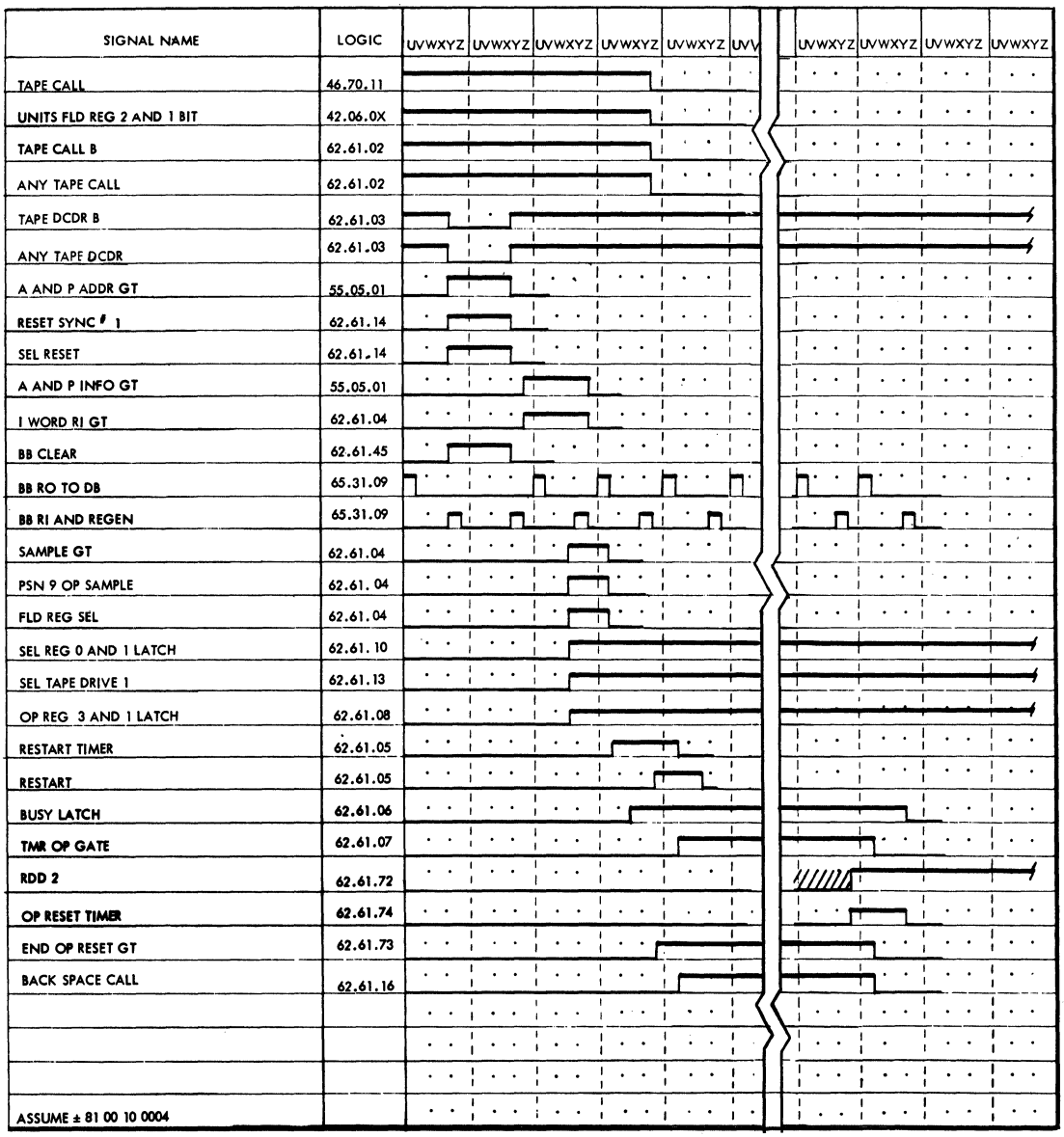


FIGURE 3.3-4. BACKSPACE

With the tape unit in write status, the tape is moved forward, and the tape read write trigger is placed in read status.

If the tape unit is in read status when the backspace operation is called for, the tape drive is reversed and the tape moves backwards over one record.

If the tape unit was at its load point at the time the backspace command was given, no tape motion takes place.

Objectives:

1. Anaylze the tape instruction
2. Condition selected synchronizer
   a. Determine tape movement instruction (62.61.02)
   b. Reset synchronizer controls (62.61.03)
   c. Clear buffer B (62.61.45)
3. Transfer instruction word to buffer B (62.61.04)
4. Determine tape operation (62.61.04)
   a. Select tape drive (62.61.04)
   b. Select Op registers (62.61.04)
5. Prevent initial status word development (62.61.18)
6. Develop synchronizer interlock (62.61.06)
7. Prevent Op Reg and Sel Reg selection (62.61.04)
8. Restart A & P (62.61.05)
9. Develop backspace call (62.61.24)
10. Release synchronizer interlock (62.61.72)

1. Analyze the Tape Instruction

The beginning of each tape operation is analyzed for an index operation and an interrupt routine.

When an 80's code is sensed, the index portion (Positions 2 and 3) is analyzed to determine if an index operation is to be performed. At the completion of the index operation, the stacking latches are sampled to see if an interrupt request has been previously made for the addressed combination of tape drive and synchronizer.

If the stacking latch had been set from a previous operation, the tape synchronizer is not interlocked and A & P does not advance to the next program step. A & P continues to test the stacking latch until a no-interrupt reply is sensed.

If, at the beginning of the tape operation, a no-index and a no-interrupt reply is sensed, the specified synchronizer is interlocked and the instruction counter is updated. This allows the tape operation to proceed immediately, and A & P advances to the next program step.

2. Condition Selected Synchronizer

The units position (Position 1) of the operation code is analyzed in A & P to determine whether the tape call signal is to be developed for synchronizer 1 or 2.

a. Determine Tape Movement Instruction. The tape-call signal is sent to the specified synchronizer where it is switched at 5F (62.61.02) with the static output of the field register units position (Position 5) to develop the Tape Call B and Any Tape Call signals. The tape call signal is used to turn on the Tape Decoder B latch at 3E (62.61.03). The DCDR B latch signifies that the data portion of the instruction further defines the tape operation.

b. Reset Synchronizer Controls. When the data request signal is developed in A & P, an address gate and an information gate are sent to the tape synchronizer.

The address gate signal is used to form the coincidence at 4D (62.61.14) with a No CE Op and Any Tape Call to develop the Reset Sync and the Select Reset signals. These signals are used to reset the synchronizer controls that were used in the previous operation.

c. Clear Buffer B. Prior to the transferring of the Program Register D, Instruction Counter, and Op Register, the Buffer B register must be reset. This is accomplished by switching the Reset Sync signal with a V - X pulse to turn on the Buffer B Clear latch (4A-62.61.45).

The output of this latch is used to prevent the buffer B register from reading out to the distributor bus at U-time. Because the distributor bus capacitors were not charged at U-time, the reading in at Y-time produces a blank register.

3. Transfer Instruction Word to Buffer B

During A & P information gate time, the contents of the program register D, instruction counter, and op register are parallel-transferred onto the information bus at U-time. The contents of the information bus is then read into the buffer B register at Y-time.

The reading into the BB register is accomplished by switching the Information Gate, Any Tape Call and a No CE Op signal at 4B (62.61.04). The coincidence of these signals forms the I Word RI gate which is used to develop the IB RI gate (62.61.45). The IB RI gate is switched with a Y-pulse to turn on the read in driver. This allows the contents of the information bus to read intothe buffer B register.

4. Determine Tape Operation

To analyze the tape instruction, the sample gate latch must be turned on. This is accomplished by switching the I word RI gate with a X - Z pulse at 3D (62.61.04).

a. Select Tape Drive. The sample gate output is switched with Any TP DCDR at 4J(62.61.04) to develop the field register select sample pulse. This pulse is, in turn, gated with the static output of field register tens position to turn on the specified select register latches. The output of these latches is used to condition the selected tape drive unit.

b. Select Op Registers. To determine the backspace operation, Position 9 of the BB register must be sampled. To accomplish this, the sample

gate is switched with Tape DCDR B at 4H to develop Position 9 Op Sample gate (62.61.04).

As the buffer B register is read out to the distributor bus during the regen cycle, the 9's position is sampled. Because the backspace code is specified as a 4 in the 9's position, the 3 and the 1-bit Op Register latches are on (62.61.08). The output of these latches is used to develop the backspace signal (62.61.16).

5. Prevent Initial Status Word Development

During the backspace operation, the storing of the initial status word is prevented. This is accomplished by inhibiting the development of the status word gate. The status word gate is developed when the Tape DCDR A signal is up, or during a write tape mark or block mark operation (62.61.18).

6. Develop Synchronizer Interlock

Before A & P can be restarted, the tape synchronizer must be interlocked. To accomplish this, the sample gate is switched with a V - X pulse at 3A (62.61.05) to turn on the restart timer latch. The restart timer latch is used to form the coincidence at 2G with a Continue Sync Op and a X - Z pulse to turn on the Busy latch (62.61.06). The Busy latch remains on until the operation is completed.

7. Prevent Op Reg and Sel Reg Selection

The restart timer latch coming on prevents the development of another Tape Select and Op Select. The restart timer latch is used to reset the sample gate at Z - V time (2E-62.61.04). With the sample gate reset, the field register sample and the Position 9 Op Sample signals are turned off.

8. Restart A & P

With the synchronizer Busy latch turned on, the restart timer latch and a Z - V pulse form the coincidence at 2D to turn on the restart latch (62.61.05). The output from this latch is used to restart A & P.

9. Develop Backspace Call

Before the Backspace Call can be developed and sent to TAU, the Timer Op gate must be turned on. The Timer Op gate allows a delay that insures that the synchronizer is interlocked and A & P is restarted. The switching to accomplish this can be found on Logic 62.61.07, Switch 3J.

The output of the Timer Op Gate is switched at 4D (62.61.23) with a backspace select signal to develop the backspace call which is sent to TAU.

10. Release Synchronizer Interlock

The synchronizer interlock is released the moment the read-disconnect delay is received from TAU.

The read disconnect delay signal is switched at 4E with a backspace call and a No Blk Cnt Ctrl signal to develop the Set-Op-Reset gate. The Set-Op-Reset gate is

then switched with a Z - V pulse and an End-Op-Reset gate at 4E (62.61.74) to turn on the Op-Reset Timer. The output of this latch is used to reset the Busy latch.

The Op Reset Timer latch signal is switched with Any Tape DCDR at V - X time to develop a 2 usec pulse, which is used to reset the Timer Op gate. With the Timer Op Gate reset, the coincidence that was necessary to develop the backspace call signal is dropped (62.61.07).

3.3.05 Skip (0006) (Figure 3.3-5)

The skip instruction causes the specified tape unit to go into an erase forward condition which erases approximately five or six inches of tape on the next write call.

The tape skip instruction is used during a write operation when an error is detected due to a defective piece of tape. This enables defective or worn tape sections to be bypassed during the write operation.

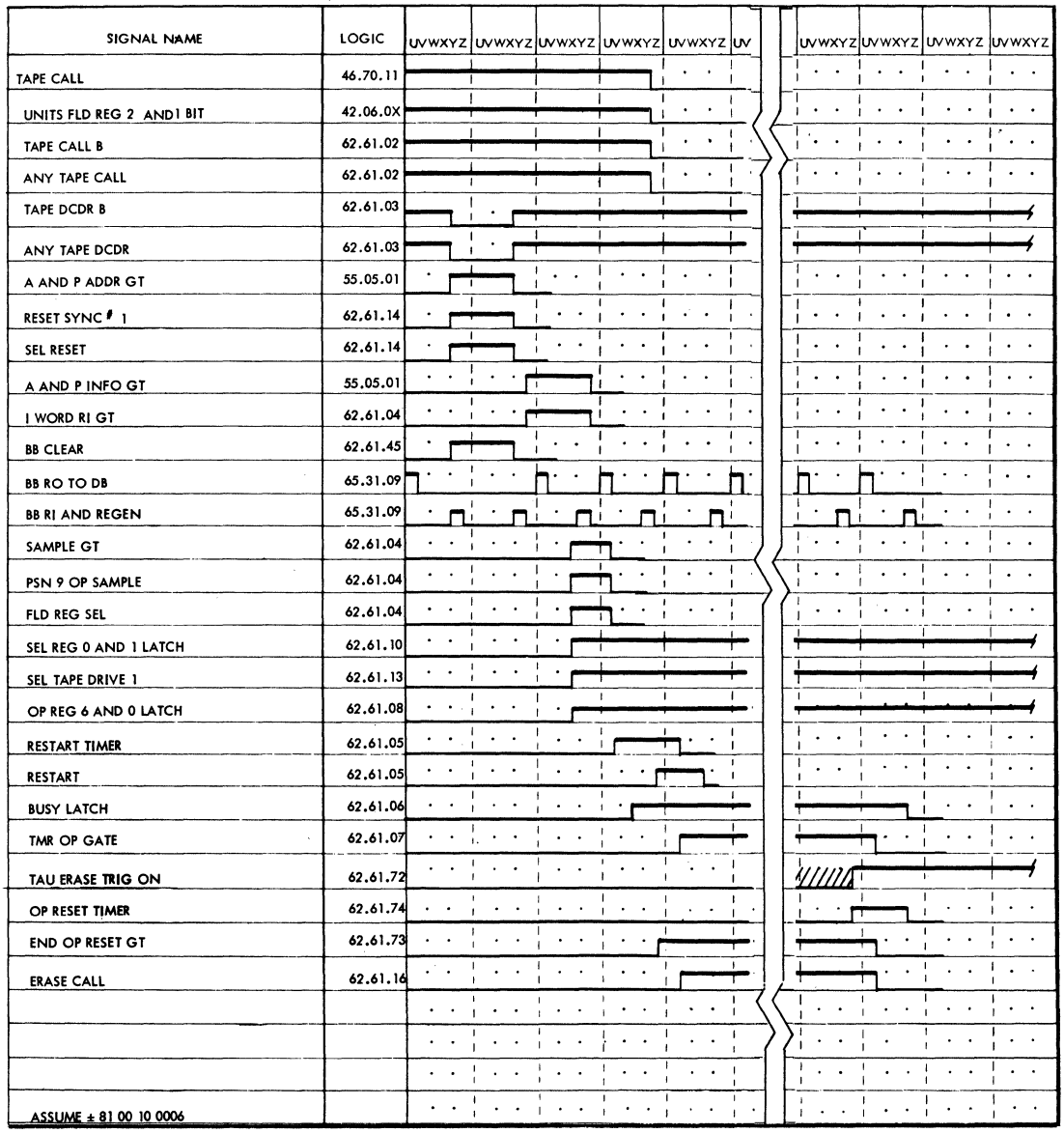


FIGURE 3.3-5. SKIP

The skip instruction operates the same as the other tape movement codes. The main differences are in the selection of the Op Register latches and the condition which releases the synchronizer interlock.

Objectives:

1. Analyze the tape instruction
2. Condition selected synchronizer
   a. Determine tape movement instruction (62.61.02)
   b. Reset synchronizer controls (62.61.03)
   c. Clear buffer B (62.61.45)
3. Transfer instruction word to Buffer B (62.61.45)
4. Determine tape operation (62.61.04)
   a. Select tape drive (62.61.04)
   b. Select Op registers (62.61.04)
5. Prevent initial status word development (62.61.18)
6. Develop synchronizer interlock (62.61.06)
7. Prevent Op Reg and Sel Reg selection (62.61.04)
8. Restart A & P (62.61.05)
9. Develop erase call (62.61.24)
10. Release synchronizer interlock (62.61.72)

1. Analyze the Tape Instruction

The beginning of each tape operation is analyzed for an index operation and an interrupt routine.

When an 80's code is sensed, the index portion (Positions 2 and 3) is analyzed to determine if an index operation is to be performed. At the completion of the index operation, the stacking latches are sampled to see if an interrupt request has been previously made for the addressed combination of tape drive and synchronizer.

If the stacking latch had been set from a previous operation, the tape synchronizer is not interlocked and A & P does not advance to the next program step. A & P continues to test the stacking latch until a no-interrupt reply is sensed.

If, at the beginning of the tape operation, a no-index and a no-interrupt reply is sensed, the specified synchronizer is interlocked and the instruction counter is updated. This allows the tape operation to proceed immediately and A & P advances to the next program step.

2. Condition Selected Synchronizer

The units position (Position 1) of the operation code is analyzed in A & P to determine whether the tape call signal is to be developed for synchronizer 1, or 2.

a. Determine Tape Movement Instruction. The tape call signal is sent to the specified synchronizer where it is switched at 5F (62.61.02) with the static output of the field register units position (Position 5) to develop the Tape Call B and Any Tape Call signals.

   The Tape Call signal is used to turn on the Tape Decoder B latch at 3E (62.61.03). The DCDR B latch signifies that the data portion of the instruction further defines the tape operation.

b. Reset Synchronizer Controls. When the data request signal is developed in A & P, an address gate and an information gate are sent to the tape synchronizer.

The address gate signal is used to form the coincidence at 4D (62.61.14) with a No CE Op and Any Tape Call to develop the Reset Sync and the Select Reset signals. These signals are used to reset the synchronizer controls that were used in the previous operation.

c. Clear Buffer B. Prior to the transferring of the Program Register D, Instruction Counter, and Op Register, the buffer B register must be reset. This is accomplished by switching the Reset Sync signal with a V - X pulse to turn on the Buffer B Clear latch (4A-62.61.45).

The output of this latch is used to prevent the buffer B register from reading out to the distributor bus at U-time. Because the distributor bus capacitors were not charged at U-time, the reading in at Y-time produces a blank register.

3. Transfer Instruction Word to Buffer B

During A & P Information Gate time, the contents of the Program Register D, Instruction Counter, and Op Register are parallel-transferred onto the Information Bus at U-time. The contents of the information bus is then read into the Buffer B register at Y-time.

The reading into the BB register is accomplished by switching the Information Gate, Any Tape Call, and a No CE Op signal at 4B (62.61.04). The coincidence of these signals forms the I Word RI Gate, which is used to develop the IB RI gate (62.61.45). The IB RI gate is switched with a Y-pulse to turn on the read-in driver. This allows the contents of the information bus to read into the buffer B register.

4. Determine Tape Operation

To analyze the tape instruction, the sample gate latch must be turned on. This is accomplished by switching the I Word RI gate with a X - Z pulse at 3D (62.61.04).

a. Select Tape Drive. The sample gate output is switched with Any TP DCDR at 4J (62.61.04) to develop the field register select sample pulse. This pulse is, in turn, gated with the static output of field register tens position to turn on the specified select register latches. The output of these latches is used to condition the selected tape drive unit.

b. Select Op Registers. To determine the skip operation, position 9 of the B B register must be sampled. To accomplish this, the sample gate is switched with Tape DCDR B at 4H to develop Position 9 OP Sample Gate (62.61.04).

As the Buffer B register is read out to the distributor bus during regen cycle, the 9's position is sampled. Because the skip code is specified as a 6 in the 9's position, the 6 and the 0-bit Op Register latches are on (62.61.08). The output of these latches is used to develop the skip signal (62.61.16).

5. Prevent Initial Status Word Development

During the skip operation, the storing of the initial status word is prevented. This is accomplished by inhibiting the development of the status word gate. The status word gate is developed when the Tape DCDR A signal is up, or during a write tape mark or block mark operation (62.61.18).

6. Develop Synchronizer Interlock

Before A & P can be restarted, the tape synchronizer must be interlocked. To accomplish this, the sample gate is switched with a V - X pulse at 3A (62.61.05) to turn on the restart timer latch. The restart timer latch is used to form the coincidence at 2G with a Continue Sync Op and an X - Z pulse to turn on the Busy latch (62.61.06). The Busy latch remains on until the operation is completed.

7. Prevent Op Reg and Sel Reg Selection

The restart timer latch coming on prevents the development of another Tape Select and Op Select. The restart timer latch is used to reset the Sample Gate at Z - V time (2E-62.61.04). With the sample gate reset, the field register sample, and the Position 9 Op Sample signals are turned off.

8. Restart A & P

With the synchronizer Busy latch turned on, the restart timer latch, and a Z - V pulse form the coincidence at 2D to turn on the restart latch (62.61.05). The output from this latch is used to restart A&P.

9. Develop Erase Call

Before the Erase Call can be developed and sent to TAU, the Timer Op gate must be turned on. The Timer Op gate allows a delay that insures that the synchronizer is interlocked and A & P is restarted. The switching to accomplish this can be found on Logic 62.61.07, Switch 3J.

The output of the Timer Op gate is switched at 4F (62.61.24) with an Erase signal to develop the Erase Call which is sent to the TAU.

10. Release Synchronizer Interlock

The synchronizer interlock is released the moment the erase trigger is turned on in TAU.

The Erase Trigger signal is switched at 4D (62.61.72) with the Erase Call signal to develop the Set Op Reset signal. This signal is used to turn on the Op Reset Timer latch (62.61.74). The output of the Op Reset Timer latch is used to reset the Busy latch which releases the tape synchronizer.

The Op Reset Timer signal is switched with Any Tape DCDR at V - X time to develop a 2 usec pulse, which is used to reset the Timer Op gate. With the Timer Op gate reset, the coincidence that was necessary to develop the Erase Call signal is dropped (62.61.07).

3.3.06 Turn-Off-End-of-File (0007) (Figure 3.3-6)

The Turn-Off-End-of-File instruction resets the condition 5 latch (EOF latch) and turns off the tape indicator light located on the specified tape drive.

The sensing of a tape mark, during a read operation turns on the tape indicator light in the specified tape unit. When either of these conditions is sensed, the BA RI serial shift (alpha or numeric) is inhibited.

During a write operation, the tape indicator light is turned on when the end-of-file mark is sensed from tape. With an end-of-field sensed, a Select and TI On signal is developed and sent to the synchronizer to turn on the end-of-file latch (Condition 5 latch).

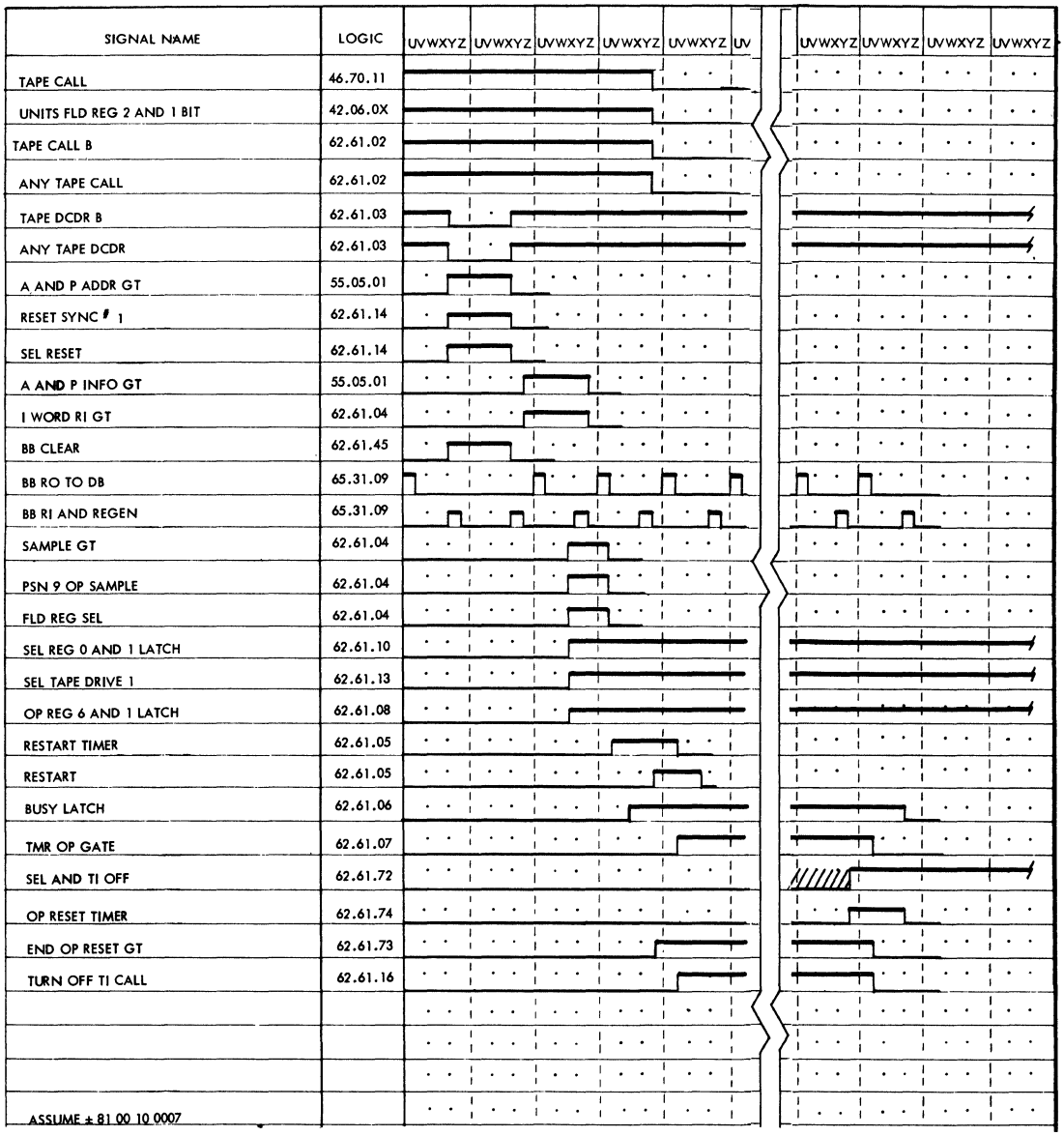


FIGURE 3.3-6. TURN OFF T. I.

Objectives:

1. Analyze the tape instruction
2. Condition selected synchronizer
   a. Determine tape movement instruction (62.61.02)
   b. Reset synchronizer controls (62.61.03)
   c. Clear Buffer B (62.61.45)
3. Transfer instruction word to buffer B (62.61.45)
4. Determine tape operation (62.61.04)
   a. Select tape drive (62.61.04)
   b. Select Op registers (62.61.04)
5. Prevent initial status word developement (62.61.18)
6. Develop synchronizer interlock (62.61.06)
7. Prevent Op Reg and Sel Reg selection (62.61.04)
8. Restart A & P (62.61.05)
9. Develop turn-off-end-of-file call (62.61.24)
10. Release synchronizer interlock (62.61.72)

1. Analyze the Tape Instruction

The beginning of each tape operation is analyzed for an index operation and an interrupt routine.

When an 80's code is sensed, the index portion (Positions 2 and 3) is analyzed to determine if an index operation is to be performed. At the completion of the index operation, the stacking latches are sampled to see if an interrupt request has been previously made for the addressed combination of tape drive and synchronizer.

If the stacking latch had been set from a previous operation, the tape synchronizer is not interlocked, and A & P does not advance to the next program step. A & P continues to test the stacking latch until a no-interrupt reply is sensed.

If, at the beginning of the tape operation, a no-index and a no-interrupt reply is sensed, the specified synchronizer is interlocked and the instruction counter is updated. This allows the tape operation to proceed immediately and A & P advances to the next program step.

2. Condition Selected Synchronizer

The units position (Position 1) of the operation code is analyzed in A & P to determine whether the tape call signal will be developed for synchronizer 1, or 2.

a. Determine Tape Movement Instruction. The tape-call signal is sent to the specified synchronizer where it is switched at 5F (62.61.02) with the static output of the Field Register Units Position (Position 5) to develop the Tape Call B and Any Tape Call signals.

   The Tape Call signal is used to turn on the Tape Decoder B latch at 3E (62.61.03). The DCDR B latch signifies that the data portion of the instruction further defines the tape operation.

b. Reset Synchronizer Control. When the data request signal is developed in A & P, an address gate and an information gate are sent to the tape synchronizer.

The address gate signal is used to form the coincidence at 4D (62.61.14) with a No CE Op and Any Tape Call to develop the Reset Sync and the Select Reset signals. These signals are used to reset the synchronizer controls that were used in the previous operation.

c. Clear Buffer B. Prior to the transferring of the Program Register D, Instruction Counter, and Op Register, the buffer B register must be reset. This is accomplished by switching the Reset Sync signal with a V - X pulse to turn on the Buffer B Clear latch (4A-62.61.45).

The output of this latch is used to prevent the buffer B register from reading out to the distributor bus at U-time. Because the distributor bus capacitors were not charged at U-time, the reading-in at Y-time produces a blank register.

3. Transfer Instruction Word to Buffer B

During the A&P Information Gate time, the contents of the Program Register D, Instruction Counter, and Op Register are parallel transferred onto the information bus at U-time. The contents of the information bus is then read into the buffer B register at Y-time. The reading into the BB register is accomplished by switching the Information Gate, Any Tape Call, and a No Ce Op signal at 4B (62.61.04). The coincidence of these signals forms the I Word RI gate, which is used to develop the IB RI gate (62.61.45). The IB RI gate is switched with a Y-pulse to turn on the read-in driver. This allows the contents of the information bus to read into the buffer B register.

4. Determine Tape Operation

To analyze the tape instruction, the sample gate latch must be turned on. This is accomplished by switching the I word RI gate with a X - Z pulse at 3D (62.61.04).

a. Select Tape Drive. The sample gate output is switched with Any TP DCDR at 4J (62.61.04) to develop the field register select sample pulse. This pulse is, in turn, gated with the static output of Field Register Tens Position to turn on the specified select register latches. The output of these latches is used to condition the selected tape drive unit.

b. Select Op Registers. To determine the turn-off-end-of-file operation, Position 9 of the B B register must be sampled. To accomplish this, the sample gate is switched with Tape DCDR B at 4H to develop Position 9 Op Sample gate (62.61.04).

As the Buffer B register is read out to the distributor bus during the regen cycle, the 9's position is sampled. Because the turn-off-end-of-file code is specified as a 7 in the 9's position, the 6 and the 1-bit Op Register latches are on (62.61.08). The output of these latches is used to develop the turn-off-end-of-file signal (62.61.16).

5. Prevent Initial Status Word Development

During the turn-off-end-of-file operation, the storing of the initial status word is prevented. This is accomplished by inhibiting the development of the status word gate. The status word gate is developed when the Tape DCDR A signal is up, or during a write tape mark or block mark operation (62.61.18).

6. Develop Synchronizer Interlock

Before A&P can be restarted, the tape synchronizer must be interlocked. To accomplish this, the sample gate is switched with a V - X pulse at 3A(62.61.05) to turn on the restart timer latch. The restart timer latch is used to form the coincidence at 2G with a Continue Sync Op and an X - Z pulse to turn on the Busy latch (62.61.06). The Busy latch remains on until the operation is completed.

7. Prevent Op Reg and Sel Reg Selection

The restart timer latch coming on prevents the development of another Tape Select and Op Select. The restart timer latch is used to reset the sample gate at Z - V time (2E-62.61.04). With the sample gate reset, the field register sample and the Position 9 Op Sample signals are turned off.

8. Restart A & P

With the synchronizer Busy latch turned on, the restart timer latch and a Z - V pulse form the coincidence at 2D to turn on the restart latch (62.61.05). The output from this latch is used to restart A & P.

9. Develop Turn-Off-End-Of-File Call

Before the turn-off-end-of-file call can be developed and sent to TAU, the Timer Op Gate must be turned on. The Timer Op Gate allows a delay that insures that that the synchronizer is interlocked and A & P is restarted. The switching to accomplish this can be found on Logic 62.61.07, Switch 3J.

The output of the Timer Op Gate is switched at 4C (62.61.24) with a Turn Off T I signal to develop the Turn Off T I Call, which is sent to TAU.

10. Release Synchronizer Interlock

The synchronizer interlock is released the moment a Select and T I Off signal is received from TAU.

The Sel and TI Off signal is switched at 4C (62.61.72) with the Sel and TI Call signal to develop the Set Op Reset signal. This signal is used to turn on the Op Reset Timer latch (62.61.74). The output of the Op Reset Timer is used to reset the Busy latch which releases the tape synchronizer.

The Op Reset Timer signal is switched with Any Tape DCDR at V - X time to develop a 2 usec pulse which is used to reset the Timer Op Gate. With the Timer Op Gate reset, the coincidence that was necessary to develop the Turn Off T I Call signal is dropped (62.61.07).

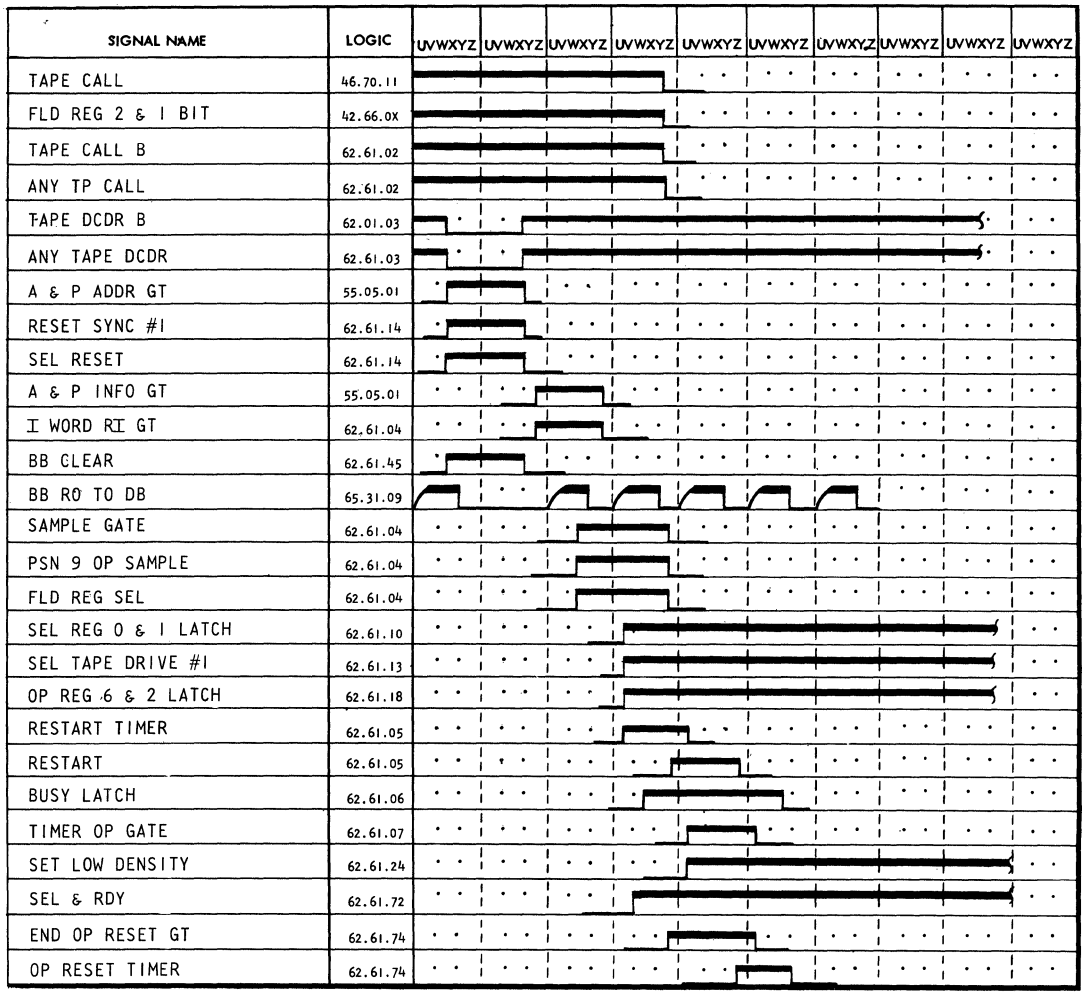


FIGURE 3.3-7. SET LOW DENSITY

3.3.07 Set Low Density (0008) (Figure 3.3-7)

There are two-bit density codes specified by positions 6 - 9 of the tape instruction. These codes provide both models II and IV with the ability to write multifunction tapes.

The setting of the density mode can be accomplished by programming, or by the use of the density change switch on the tape drive unit. Each time the density mode is changed, the high-or low-density indicator lamp is turned on at the tape drive.

During the power-on sequence, all tape drives are placed in the high-density mode (556 char per inch).

The set-low-density command is specified by an 8 in position 9 of a tape instruction. This code changes the bit density to 200 characters per inch. The changing of the bit density is accomplished by using the 667 kc and the 240 kc oscillator outputs to develop the tape adapter read and write clock timing.

Both reading and writing of tape must be done in the same density. In the event the tape is written in low density and the read operation is performed in high density, a TAU error is developed (R/W register, LRC error).

The low-density instruction is performed in much the same manner as any other tape decoder B operation. The differences are in the Op Register selection and the conditions which are used for ending the density instruction.

The following is a listing of objectives which are necessary to perform the set-low-density operation:

1. Analyze the tape instruction
2. Condition selected channel
   a. Determine tape movement instruction
   b. Reset channel controls
   c. Clear buffer B
3. Transfer instruction word to buffer B
4. Determine tape operation
   a. Select tape drive
   b. Select op registers
5. Prevent initial status word development
6. Develop channel interlock
7. Prevent op reg and sel reg selection
8. Restart A & P
9. Develop low density call
10. Release channel interlock

The explanation for the first eight objectives can be found under the No-Op Select Write Op, section 3.3.02. The development of the low-density call and the release channel interlock are explained as follows.

9. Develop Low-Density Call

Before the set-low-density call can be developed and sent to TAU, the timer op gate must be turned on. The timer op gate allows a delay that insures that the tape channel is interlocked and A & P is restarted. The switching to accomplish this can be found on logic 62.61.07, Switch J.

The output from the Timer Op gate is switched with the DCDR B signal and an Op Reg 6 & 2 bit to develop the set-low-density call (5J-62.61.24).

10. Release Channel Interlock

With the channel interlocked, a set-low-density signal is sent to TAU. The set-low-density signal is used to condition the 667 kc and 240 kc oscillators.

To release the channel interlock the tape drive must be selected and a no high density signal be available.

Command	Timing	Logic
Set End Op Reset Gt	Restart, U - X, No Status Word Gt	3C-62.61.73
Set Op Reset Tmr Gt	Sel & Rdy, Set Low Density, No High Density	4G-62.61.72

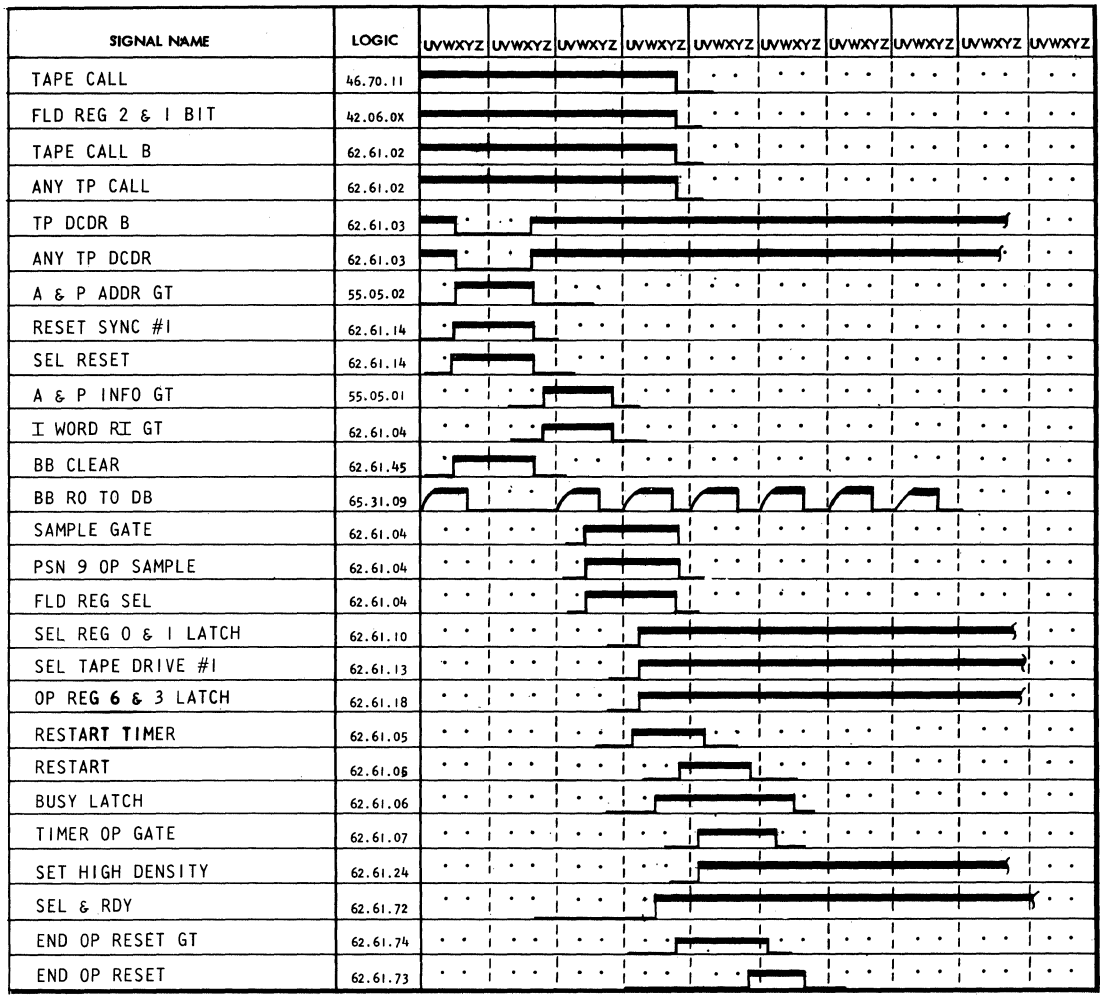


FIGURE 3.3-8. SET HIGH DENSITY

Command	Timing	Logic
Set Op Reset Tmr L	Op Reset Tmr, Z - V, Op Reset Gt	4E-62.61.74
Develop Op Tmr Reset A	Any Tp DCDR, V - X, Op Reset Tmr	3G-62.61.07
Reset Tmr Op Gt	Op Tmr Reset A	4H-62.61.07
Reset Busy	Op Tmr Reset, X - Z, No Hang Up	6C-62.61.06

3.3.08 Set-High-Density (0009) (Figure 3.3-8)

The set-high-density command is specified by a 9 in position 9 of a tape instruction. This code changes the bit density to 556 characters per inch. The changing of the bit density is accomplished by using the 1 mc and 360 kc oscillator outputs to develop the TAU timing.

Normally, all tape drives are in the high density position due to the power-on sequence.

Both reading and writing of tape must be done in the same bit density. If the tape is written in high density and read in low density a TAU error is developed (R/W Reg, LRC error).

The high-density command is performed in the same manner as the set-low density instruction. The only differences are in the op register selection and the conditions used for sensing the end of the set-high-density operation.

The following is a listing of the objectives which are necessary to performe the set-high-density operation:

1. Analyze the tape instruction
2. Condition selected channel
   a. Determine tape movement instruction
   b. Reset channel controls
   c. Clear buffer B
3. Transfer instruction word to buffer B
4. Determine tape operation
5. Prevent initial status word development
6. Develop channel interlock
7. Prevent op reg and sel reg selection
8. Restart A & P
9. Develop high density call
10. Release channel interlock

The explanation for the first eight objectives can be found under the No-Op Select Write-up, Section 3.3.01. The development of the high-density call and the release channel interlock are explaned as follows.

9. Develop High-Density Call

Before the set-high-density call can be developed and sent to TAU, the timer-op-gate must be turned on. The timer-op-gate allows a delay to insure that the tape channel is interlocked and A & P is restarted. The switching to accomplish this can be found on logic 62.61.07, Switch 3J.

The output from the timer op gate is switched with the DCDR B signal and an Op Reg 6 & 3 bit to develop the set-high-density call (5H-62.61.24).

10. Release Channel Interlock

With the channel interlocked, a set-high-density signal is sent to TAU. The set-high-density signal is used to condition the 1 mc and the 360 kc oscillators.

To release the channel interlock, the tape drive must be selected and a high-density-back signal be available.

Command	Timing	Logic
Set End Op Reset Gt	Restart, V - X, No Status Word Gt	3C-62.61.73
Set Op Reset Tmr Gt	Sel & Rdy, Set Low Density, No High Density	4G-62.61.72

Command	Timing	Logic
Set Op Reset Tmr L	Op Reset Tmr, Z - V, Op Reset Gt	4E-62.61.74
Develop Op Tmr Reset A	Any Tp DCDR, V - X, Op Reset Tmr	3G-62.61.07
Reset Tmr Op Gt	Op Tmr Reset A	4H-62.61.07
Reset Busy	Op Tmr Reset, X - Z, No Hang Up	6C-62.61.06

4.0.00 CONDITION CODES

A group of seven condition latches is used to indicate a priority (interrupt) signal at the completion of a read or write operation. Each condition latch indicates a specific error condition that indicates an unusual tape condition, with the exception of the condition 2 latch which indicates a correct length record.

The condition latches are used to indicate two types of error conditions:

1. An error in reading or writing of tape that may be corrected by repeating the operation.
2. Errors in the channel control unit operation that cannot be corrected by repeating the operation.

Channel control unit errors are considered hang-up errors. The first type of errors releases the Sync Busy latch after the specific stacking latch in the 7602 has been set. The second type of errors does not release the Sync Busy latch and A & P locks up in the event the channel control unit is re-addressed. To release the channel control unit, the computer reset or the error reset is used. The computer reset resets the whole machine; the error reset resets the channel control units and all error latches in the machine.

4.1.00 ERROR (COND #1)

The Error Condition #1 latch is turned on when any error is sensed. This condition latch for tape takes precedence over any other condition latch that was previously set. The error conditions for the channel control unit can be seen on Figure 4.1-1 which shows that the Info Stop latch is turned on for some error conditions to prevent the possibility of having data read into core storage locations that are not addressed.

4.1.01 Timing Error

When a previous memory request has not been serviced, the timing-error latch is turned on. This condition is detected as the last character is being read into or read out of buffer A. The timing error prevents any further data word requests during a read operation by turning on the Info Stop latch. During a write operation the data word requests continue until the start and stop addresses match.

Command	Timing	Logic
Set Timing Error	Memory Req, BA Ser RO L BA Last Ser Sh	2H-62.61.82
Set Info Stop	Timing Error	3B-62.61.84
Set Hang Up Error	Timing Error	2D-62.61.83

A timing error is also detected if a Data Word Xfer RI cycle is initiated before the Control Word Xfer cycle is completed. This check insures that the reading or writing of tape does not exceed its prescribed tape speed. With an increase in tape speed a timing problem can arise within the core storage priority controls that would prevent the handling of all memory requests.

Command	Timing	Logic
Set Timing Error	DW Xfer RI, CW Xfer RI, X-Z	62.61.82
Set Info Stop	Timing Error	3B-62.61.84
Set Hang Up Error	Timing Error	2D-62.61.83

4.1.02 Tape Word Error

When the tape word error is on, it indicates that one of the following error conditions has occurred during a tape read operation. Each of these conditions also turns on the Info Stop latch, thereby inhibiting data word requests.

1. A mode change in the middle of a word.
2. Missing sign over units.
3. Short length word.

Mode Change in Middle of a Word

The Mode Change in the Middle of a Word can occur if a numeric word is preceded by a short length alpha word. This is indicated as an error because the mode change did not occur at the end of a full word.

Command	Timing	Logic
Set Tape Word Error	Mode Change, BA Ser RI, No BA First Ser Sh, Read Ctrl	3A-62.61.82
Set Info Stop	Tape Word Error	3D-62.61.84
Set Hang Up Error	Tape Word Error	3F-62.61.83

Missing Sign Over Units

A Missing Sign over Units is detected when the buffer A register advances more than ten places. As mentioned previously, during a numeric read operation, the tag is inserted into the capacitor of position 9 of the tag register. Because an end of a numeric word is detected by the sensing of the sign over units, a missing sign allows the buffer A register to continue to advance. As the tag advances out of position zero, a shift of more than ten places is detected. The detection of the tag and a No BA Last Serial Shift turns on the Tape Word Error latch. This condition also causes the Info Stop latch to be turned on to prevent the tape word from being stored in core storage.

Command	Timing	Logic
Set Tape Word Error	BA 0 Psn Tag, No BA Last Ser Sh, Numeric Ctrl, Read Ctrl, BA Ser RI	3C-62.61.82
Set Hang Up Error	Tape Word Error	2F-62.61.83
Set Info Stop	Tape Word Error	3D-62.61.84

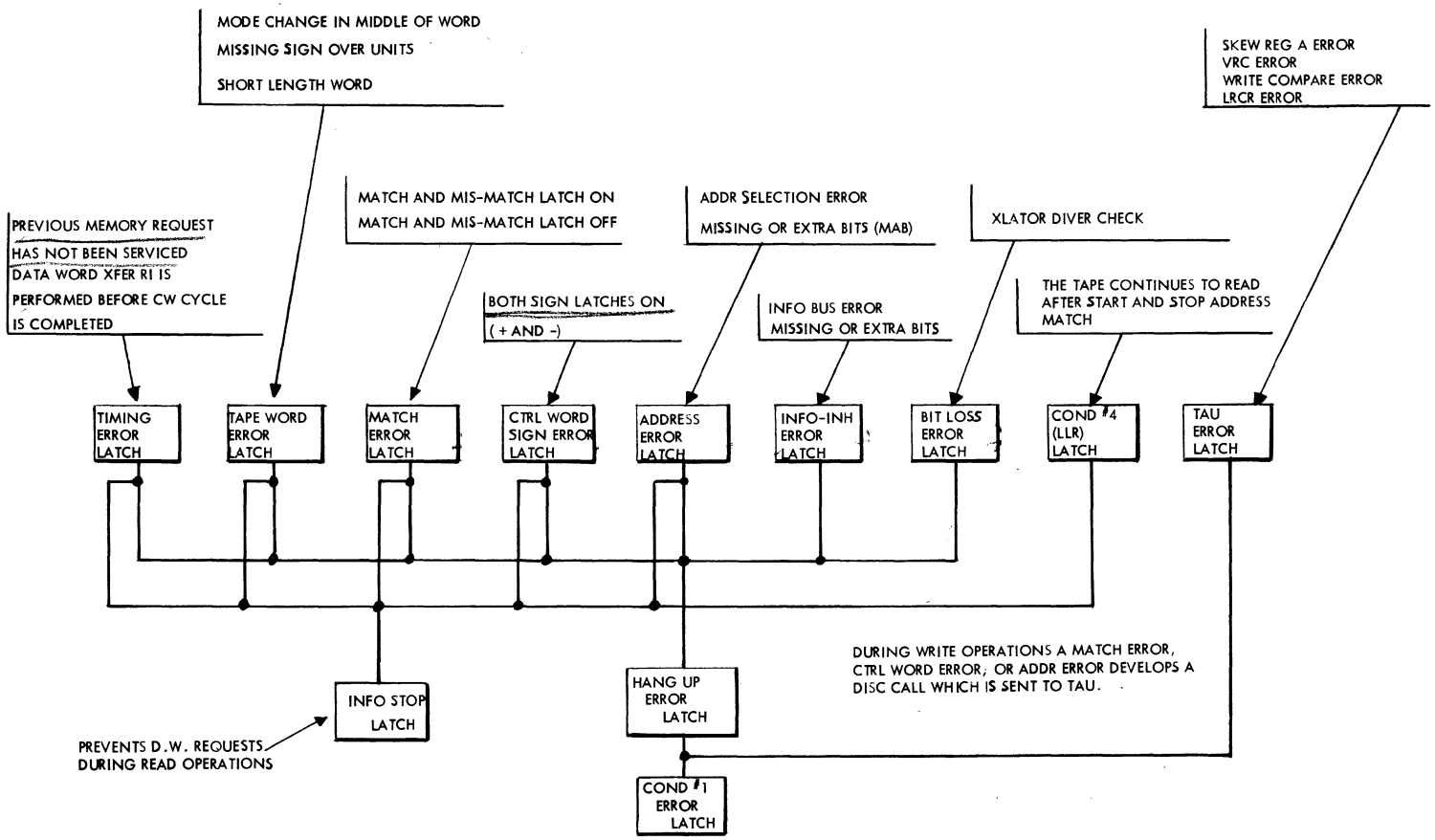


FIGURE 4.1-1. CONDITION LATCHES

Short Length Word

A Short Length Numeric Word is detected if a zero is not read out of the high order position of the buffer A register during the BA Last Serial Shift Operation. This check insures that each numeric word must have at least five digits of numeric information. At the beginning of each read operation, six zeros are automatically added to the low-order positions of buffer A for this purpose.

With a short length word detected, the tape-word-error latch is turned on. This latch, in turn, conditions the Info Stop latch to prevent the tape words from being stored in core storage.

Command	Timing	Logic
Set Tape Word Error	BA Last Ser Sh, BA Ser RI, Numeric Ctrl, Read Ctrl, No BA 0 Pos 0 Bit	3E-62.61.82
Set Info Stop	Tape Word Error	3D-62.61.84
Set Hang Up Error	Tape Word Error	2F-62.61.83

4.1.03 Match Error

With the match-error latch on, one of the following error conditions may be present:

1. Both match and mis-match latches on.
2. Both match and mis-match latches off.

The match mis-match circuitry checks for extra or missing bits in the stop register and also checks for component failures. The sampling for a match error is accomplished each time the stop tag reads out of the tens position. At this time, a check is made to insure that at least one latch (either match or mis-match) is turned on.

Missing Bits

With missing bits in the stop register, both the match and mis-match latches are turned on. This combination is treated as an invalid match, and a match error is developed. With no bits in the stop register, both the match and mis-match latches are turned on.

Extra Bits

With extra bits in the stop register, both the match and mis-match latches remain off. This combination is also treated as an invalid match, and the match error is developed.

With missing or extra bits in the stop register, an error condition is not developed until the other positions of the start and stop register match.

Start	0 1 6 2	No Error Sensed
Stop	0 - 5 2	

Start	0 1 6 2	Error Sensed
Stop	0 - 6 2	

During a read operation, a match error turns on the Info Stop latch which prevents any further data word requests. However, a final status word is not developed until the tape drive reaches the end of the tape record.

During a write operation, a match error develops a disconnect signal which stops the tape drive and initiates a final status word cycle.

Any error condition, such as missing or extra bits in the start register, is detected when the start address is read out onto the Sync Address Bus.

Component Failure

As mentioned previously, the match and mis-match switching circuits are analyzed for component failures. These failures are listed with the type of indication that is available to turn on the match error latch.

1. Open Diode - Both match and mis-match on.
2. Open Transistor - Both match and mis-match off.
3. Shorted Transistor - Both match and mis-match on.

Command	Timing	Logic
Set Match Error	Match and Mis-match Off or Match and Mis-match On	6G-65.51.43 5J-65.51.43
Set Hang Up Error	Match Error	3D-62.61.83
Set Info Stop	Match Error	4B-62.61.84
Develop Disc Call	Match Error	5G-62.61.71

4.1.04 Control Word Error

With both control word sign latches on (+ or -) the control word error latch is turned on. This error condition prevents data word requests during a read operation and also stops the tape drive during a write operation. The control word error is classified as a hang-up error, and the condition 1 latch is turned on.

A control word sign error during a read operation allows the tape to continue to read until the end of the tape record is sensed. The words read from tape are placed into the buffer A register. When buffer A has a complete word, it is transferred to buffer B. However, because a control word error is present, the data word cycles are inhibited. When the end of the tape record is sensed, the normal read disconnect takes place and a final status word cycle is initiated.

With a control word sign error detected during a write operation, a disconnect call signal can be developed before the tape drive gets up to speed. Under this condition, the tape drive writes one character and then performs its normal write disconnect operation. At Read Disconnect Delay 136 time a Final Status Word cycle is developed to store the tape error condition code.

Missing Control Word Sign

During a read operation, when a match signal is available with No Control Word Sign, the tape drive continues to read the tape record. The words read after the match has been found are stored into the core storage location specified by the last start address. This operation continues until the end of the tape record is reached. Normally, at read disconnect delay 36 time, the condition #2 latch (correct length record) is turned on. However, because the end-of-record-delay latch could not be turned on due to the absence of the control word sign, the condition #3 latch (short length record) remains on.

If, during a write operation, a match signal is available with no control word sign, the tape drive continues to run until the foil strip on the tape is sensed. Prior to sensing the foil strip, the Bit Loss Latch is turned on after the last character of the last word is read out of buffer A. The data requests are inhibited due to the absence of a mis-match signal.

With the last character written on tape, the read disconnect delay reaches its 136 u sec point and a final status word cycle is initiated to store the condition #1 latch indication. Without a control word sign, a disconnect call cannot be developed. This allows the tape drive to run until the foil strip is sensed and the tape indicator is turned on. During normal operations, with the tape indicator on, the condition #5 latch (end of file) is turned on. However, due to condition #1 being on, the turn on of condition #5 is inhibited.

Command	Timing	Logic
Set Ctrl Word Sign	CW Sign + and -	4G-62.61.81
Set Hang Up Error	CW Sign + and -	2C-62.61.83
Set Info Stop	CW Sign + and -	3E-62.61.84
Set Cond #1	CW Sign + and -	3E-62.61.85
Reset Cond #3	Cond #1 (Error)	5C-62.61.86
Develop Disc Call	Ctrl Word Sign Error	4G-62.61.71

4.1.05 Address Validity Check Error

When a missing or extra bit has been detected on the memory address bus, the address error latch is turned on. This error condition can occur when either the Control Register A or the Start Register contents are read out to the address bus. When this type of error condition occurs, it is gated with the particular sync that is making the memory request to develop a Sync Addr Validity Check signal in the 7602. This signal is sent to the channel control unit to condition the address error latch. An address validity check error is classified as a hang-up error and the condition #1 latch is turned on.

When an address validity-check error is detected during a read operation, the Info Stop latch is turned on to prevent data word requests. The Info Stop latch is

turned on any time a possibility arises that may destroy the information in the core storage locations which were not addressed. The tape drive continues to feed until the end of the tape record is sensed. With the end of the record sensed, the read disconnect delay 136 usec point is reached, and a final status word cycle is initiated to store the condition #1 indication.

An address validity-check error during a write operation causes a disconnect call signal to be developed. This signal is sent to TAU to initiate the Write Disconnect Delay, which causes the tape drive to stop and the Read Disconnect Delay to reach the 136 usec point. With the write operation completed, the final status word is developed and the interrupt mode latch turned on.

Command	Timing	Logic
Set Addr Vc Latch	Addr Vc, Y-U	5A-62.61.81
Set Hang-Up Error	Addr Vc, Y-U	2B-62.61.83
Set Info Stop	Addr Vc, Y-U	3H-62.61.84
Set Cond #1	Hang Up Error	5C-62.61.85
Reset Cond #3	Cond #1 (Error)	5C-62.61.86
Develop Disc Call	Addr Vc Error	4F-62.61.71

4.1.06 Information and Inhibit Driver Validity Check

The Information and Inhibit Error latch indicates two types of errors:

1. Missing or extra bits on the information bus.
2. Missing or extra bits detected by the inhibit drivers when regening the addressed word back into core storage.

When this type of error condition occurs, it is gated with the particular Sync that is making the memory request to turn on a Sync Validity Check latch in the 7602. This error signal is sent to the channel control unit to condition the Info-Inh Error latch. The Info-Inh Error condition is considered as a hang-up error and the condition #1 latch is turned on.

During a read operation, the Info-Inh latch is turned on to indicate that missing or extra bits have been detected. The read operation continues until the end of the tape record is sensed. At the completion of the operation, a final status word is developed to store the condition #1 indication and turn on the Interrupt Mode latch.

On a write operation, the Info-Inh Error latch being on indicates that either an Information Bus Error, or an Inhibit Driver Error, has been detected. The tape write operation continues until the start and stop register match, and the control word sign is minus. With these conditions available, a disconnect call is sent to TAU to stop the tape drive. At the completion of the write operation, a final status word cycle is initiated to store the condition #1 indication and to set the Interrupt latch.

With a missing bit detected, the Bit Loss Error latch is also conditioned due to the absence of the proper drive lines.

With an extra bit, a TAU Error is also indicated, for at RO time the translator does not furnish an output to TAU.

Command	Timing	Logic
Set Info Bus or Inh Driver Error	IB-Inh Vc, Y-U	4G-62.61.80
Set Hang-Up Error Latch	IB- Inh Vc, Y-U	2A-62.61.83
Set Cond #1	Hang-Up Error	5C-62.61.84
Reset Cond #3	Cond #1 (Error)	5C-62.61.86

4.1.07 Bit Loss Error

If one or more translator drivers have failed during the read or write operation, the bit-loss latch is turned on.

The core matrix translator has the ability to check for driver failures by reserving eleven cores to indicate the loss of one or more drive lines. Both the 2-out-of-5 code and the BCD code use the same cores for detecting a bit loss. For a further explanation of the driver check, refer to the translator validity check write-up, Section 2.6.03.

The bit loss is considered a hang-up condition which prevents the synchronizer-busy latch from being reset at the completion of the read or write operation.

On a write operation, the driver failure may cause a TAU error to be developed. Under this condition, the hang-up error latch is reset. The resetting of the hang-up error latch enables the channel control unit to be re-addressed in the event a re-write operation is to be performed.

On a read operation, the loss of the driver may also cause an information bus error, if extra or missing bits were furnished by the translator.

Command	Timing	Logic
Set Bit Loss Error	Bit Loss	3A-62.61.82
Set Hang-Up Error	Bit Loss	3C-62.61.83
Set Cond #1	Hang-Up Error	5C-62.61.84
Reset Cond #3	Cond #1 (Error)	5C-62.61.86

4.1.08 TAU Error

The TAU Error latch being on indicates that one or more of the following error conditions have been detected during the actual reading or writing of a tape record:

1. Skew Register Error
2. Write Compare Error
3. VRC Error
4. LRCR Error

Because the TAU error condition may have been caused by a bad piece of tape, the TAU Error latch resets the hang-up error latch. With the hang-up error latch reset, the programmer can re-address the channel control unit to re-read or re-write the record.

To insure that the complete record has been checked, the resetting of the hang-up error condition and the setting of the condition #1 latch (error) is performed during the final status word cycle.

Command	Timing	Logic
Set TAU Error	RSW RO L, RAU Error, Any TP RD or WR	3A-62.61.80
Set Cond #1	TAU Error	5F-62.61.84
Set Hang-Up Release	TAU Error	4F-62.61.83
Reset Hang-Up Latch	Hang-Up Release	4C-62.61.83

4.2.00 CORRECT LENGTH RECORD (COND #2)

The correct length record condition latch indicates during a read operation that the record received from tape is coincident with the start and stop match condition, and a no-error condition has occurred. On write operations, the correct length record latch turns on to indicate that the write operation has been performed without an error. When this condition latch is on, it does not cause a priority routine.

During a read operation, the correct length record latch is turned on when the end of a tape record is sensed, and the read disconnect delay reaches its 36 usec. point.

Command	Timing	Logic
Develop Tp R/W Clear	EOR Delay, Read Ctrl, Rdd 36	5D-62.61.70
Set Cond #2	Tp R/W Clear	6D-62.61.85
Reset Cond #3	Any Tp DCDR, Cond #2 latch	4B-62.61.86

During a write operation, the correct length latch is turned on when the last character of a record has been written.

Command	Timing	Logic
Set WR End of Record	EORDelay, BA Last Ser Sh, BA Ser RO L	2B-62.61.71
Develop Tp R/W Clear	Wr End of Record, Any Tp DCDR, BA Ser RI	5E-62.61.70

Command	Timing	Logic
Set Cond #2	Tp R/W Clear	6D-62.61.85
Reset Cond #3	Any Tp DCDR, Cond #2	4B-62.61.86

4.3.00 SHORT LENGTH RECORD (COND #3)

The short length record latch is turned on prior to each tape operation. When the short length record latch is on at the end of a tape read operation, it indicates that a record gap has been reached prior to the start and stop registers becoming equal (match). The address in positions 2-5 of the final status word is the last core storage word filled.

The short length record latch may remain on due to a missing control word sign. For further explanation, refer to the Missing Control Word Sign write-up (Section 4.1.04).

During normal operations, the condition 2 latch turn-on resets the condition 3 latch. With the condition 2 latch off, the interrupt mode latch is turned on to condition the stacking latch in the 7602.

Command	Timing	Logic
Set Cond #3	ISW RI Info GT, Any TP DCDR	3A-62.61.86

4.4.00 LONG LENGTH RECORD (COND #4)

The long length record occurs during a read operation and indicates that the end of the tape record occurred after the start and stop register reached their match condition. When this condition exists, the start register continues to be 1-upped until the end of the tape record has been reached. The start register indicates the number of words that were read after the start and stop address became equal. Memory requests are not performed after a match has been found, due to the turn on of the Info Stop latch which prevents the development of data word requests.

Command	Timing	Logic
Set Cond #4	EOR Delay, BA Ser RI Tape RD	4C-62.61.86
Reset Cond #2	Cond #4, RSW RO Info Gt Any Tp DCDR	5H-62.61.85
Set Info Stop	Cond #4, Any Tp DCDR	4G-62.61.84

4.5.00 END OF FILE (COND #5)

When a foil strip is sensed during a write operation, the end-of-file condition latch is turned on. During a read operation, the end-of-file condition indicates that a tape mark has been sensed. The end-of-file condition latch is turned on when the Select and Tape Indicate signal is available from TAU.

With the Select and Tape Indicator signal available, a final status word cycle is developed when the Read Disconnect Delay reaches its 136 usec point.

Command	Timing	Logic
Set Cond #5	Sel and TI On, Any TP DCDR	5E-62.61.86
Develop RSW Cycle	Sel and TI On, Rdd 136, No Blk Cnt Ctrl	4C-62.61.07
Reset Cond #3	Cond #5	6C-62.61.86

4.6.00 END OF SEGMENT (COND #6)

The end-of-segment latch indicates that a segment mark has been sensed during a read operation. The sensing of the segment mark resets either the condition #3 latch (SLR) or the condition #2 latch (CLR). This is dependent on whether one or more words are to be read from tape. If a single word was to be read from tape, the condition #2 latch would have been set, provided the control word sign was minus.

Because the segment mark is written as a single character record, a final status word cycle is developed when the read disconnect delay reaches the 136 usec point.

Command	Timing	Logic
Set Cond #6	No Blk Cnt Ctrl, Blk Mark	5G-62.61.86
Reset Cond #3	Cond #6	5A-62.61.86
Develop FSW Cycle	No Blk Cnt Ctrl, Rdd 136	4B-62.61.07

4.7.00 SHORT CHARACTER-LENGTH-RECORD (COND #7)

When the short character-length-record latch is on, the last alpha word read from tape must have zeros added to complete the word. If a record gap is sensed prior to sensing the buffer A tag, the condition #7 latch (SCLR) is turned on. The output of this latch is used to advance the buffer A register and to insert zeros into the low-order position (pos 8-9). The zero insertion continues until the buffer A tag is sensed which indicates that one more left shift is needed to complete the word. With the last zeros inserted, the normal data word transfer cycle is developed to transfer the contents of buffer A to buffer B. At this time, a data word request is initiated to store the last alpha word.

This operation is inhibited if the condition #4 latch (LLR) has been turned on prior to sensing the short character-length record.

When the read disconnect delay reaches the 136 usec point, the final status word cycle is initiated to store the condition #7 indication. With the Final Status Word RI latch on, the interrupt mode latch is turned on to set the stacking latch in the 7602.

Command	Timing	Logic
Set Cond #7	No Blk Stt, No Blk Cnt Ctrl, Rdd 36, No Cond #4	5F-62.61.87
Reset Cond #3	Cond #7	5A-62.61.86
Develop SCLR 0 Ins	Cond #7, No Blk Stt	7F-62.61.87
Set BA Ser RO L	SCLR 0 Ins	4C-65.21.20
Ins Zero In Pos 8 & 9	BA Ser RI, SCLR 0 Ins	3D-65.41.22

5.0.00 CE CONSOLE OPERATION

The tape channel CE control panel was designed for a two-fold purpose: one, as a neon display for programmer's use; second, as a Customer Engineering Tool.

When used for a neon display, the CE panel is located in the 7070 CE console which is located next to the 7150 operator's console. With the CE panel in the 7070 CE console, all selection and control switches are inoperative with the exception of the channel selection switch.

When it is used as a customer engineering tool, the CE panel is removed from the CE console and plugged into the core control unit (7602). Because of the test control logics built into the 7602 and 7604 units, the CE is able to perform all basic tape operations. This provides customer engineering personnel with the following advantages:

1. Enables the tape system to be removed from the rest of the system for servicing.
2. Performs the various tape operations without requiring the use of the logic in A & P.
3. Confines testing procedures and servicing techniques to a small machine area.

The CE operations are designed to use the normal control circuitry within the tape channel. All tape operations are performed in much the same manner as the normal instructions. The differences are in the use of the CE address and information gates, and limiting the memory request to the 7604 unit.

The following sections explain the various groups of indicators, selection switches, and control switches.

5.1.00 INDICATORS AND SWITCHES

5.1.01 Indicators (Figure 5.1-1)

Read Write (R/W) Register

The R/W register indicators display the bit combinations that have been read into the register from either the high or low registers (skew registers).

High Register

The high-register indicators (skew reg A) display the bit combinations that are available during a read or write operation.

Low Register

The low-register indicators (skew reg B) display the bit combinations that are available during the read or write operations.

Longitudinal Redundancy Check (LRC) Register

The longitudinal redundancy check indicators display the write triggers that are not reset if an LRC error has been detected.

Clock Indicator

The write and read indicators display how far the write or read clock has advanced in the event of an error.

Delay Indicator

The delay indicator displays how far the various tape delays have progressed in the event of a delay error.

Delay Control Indicators

The delay control indicators, along with the delay indicators, are used to determine what type delay was being performed and how far the delay progressed.

Operating Indicators

The operating indicators are used to display the various TAU triggers that are conditioned to perform the specific tape operations.

Validity Indicators

The validity indicators display the various TAU errors that can be detected during a read or write operation.

Status Indicators

The status indicators are used to display the status of the particular channel that is being used.

Checking Indicators

The checking indicators display the various channel errors that can occur during a tape read or write operation. The checking indicators also display the condition latch that has been set and stored in the final status word at the completion of a tape operation.

Control Indicators

The control indicators display the various control latches that are set to perform a specific tape operation.

5.1.02 Selection Switches (Figure 5.1-1)

CE Control Switch

The CE control switch is used to initiate the CE on operation and develop the Tape Op or Disk Op call. The switch turned to either position interlocks the particular tape channel.

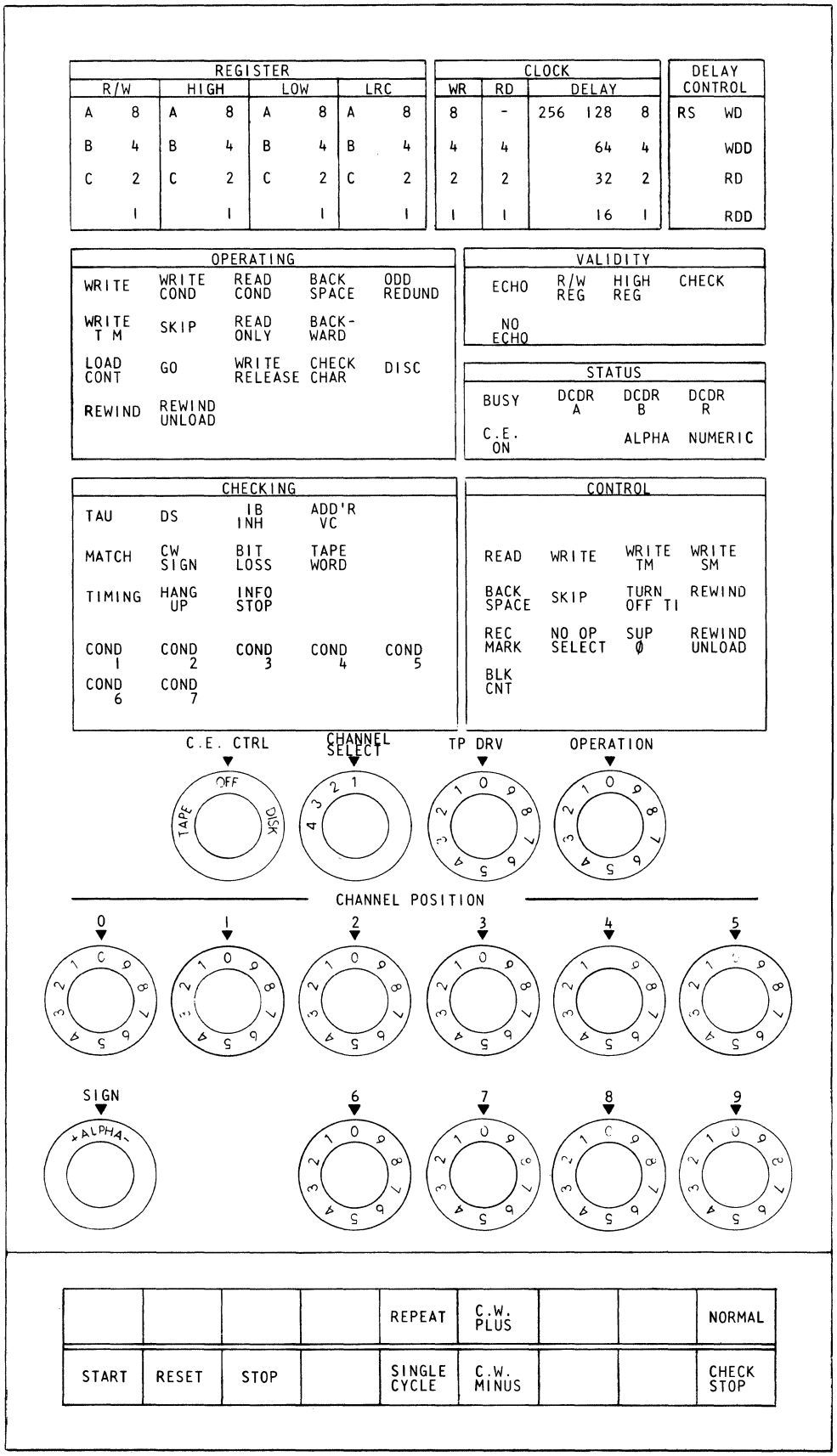


FIGURE 5.1-1 CE CONSOLE--TAPE PANEL

Channel Select Switch

The channel select switch is the only switch that can be operated when the 7604 CE console is located in the 7070 CE console. This switch selects the individual tape channel for indicator display.

When used during CE operation, the channel select switch should be positioned to the selected channel before placing the CE control switch to the Tape or Disk position.

Tape Drive Select Switch

The tape drive select switch specifies the tape drive that is to be used when reading or writing from the CE console. This switch simulates position 1 of the tape instruction.

Operation Switch

The operation switch simulates position 5 of a normal tape instruction. This switch specifies the tape operation that is to be performed and also determines whether decoder A or B is to be used. With the selection switch setting on zero, the decoder B latch is turned on. This signifies that position 9 of the tape instruction further defines the tape operation. The selection switch setting on any other position develops decoder A, along with the tape operation that is to be performed.

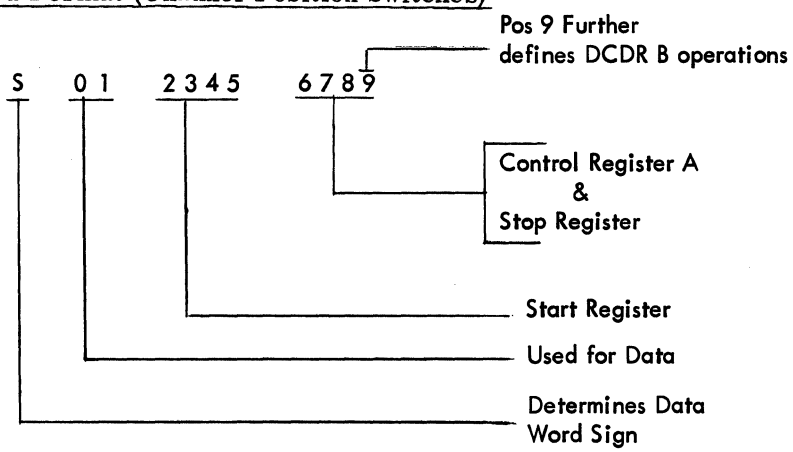
Sign Switch

The sign switch is used to insert the sign value into the sign position of the buffer B register. This sign is used to determine the sign of the data word. The normal sign analysis for determining the control word sign and the interrupt mode is inhibited during a CE operation.

Channel Position Switches

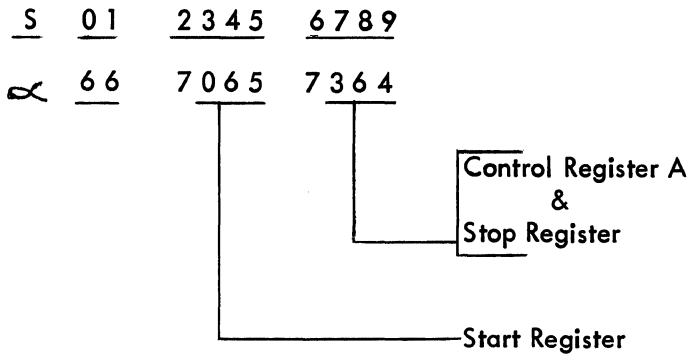
The channel position switches 0-9 are used to simulate a ten-digit data word on the information bus. Positions 2-9 are also used for determining the control word and the control register A setting. Under this condition, both the control register A and the stop register have the same value.

CE Word Format (Channel Position Switches)



If an alpha word is to be written, positions 2-9 are also used to develop the control word and the control register A address.

Alpha Word Format (Channel Position Switches)



If the operation switch is set on zero, position 9 of the alpha word designates a backspace operation due to the 4 in position 9.

5.1.03 Control Switches (Figure 5.1-1)

Start Switch

Depressing the start switch sets the CE Start latch. The start latch is used to develop a CE A & P address and information gate to start the CE operation.

Reset Switch

Depressing the reset switch causes a channel reset to be developed which resets the selected tape channel.

Stop Switch

Depressing the stop switch sets the CE stop latch. With the CE stop signal available, the control word plus latch is turned off and the control word minus latch turned on. The tape operation continues until the start and stop registers develop a match signal. The stop latch can also be set automatically if an error condition is sensed or a select and TI signal is developed.

Repeat-Single Cycle Switch

Repeat Position. With the switch in the repeat position, a repeat signal is available to turn on the CE start latch after the final status word is developed. The repeat cycle functions only if the control word sign is minus.

Single Cycle Position. With the switch in the single cycle position, the tape operation reads or writes a single record. The single cycle operation is dependent upon the control word sign being minus. With a plus sign available, a read or write operation is performed.

Control Word Sign Switch

Control Word Plus Position. With a control word plus sign available, the tape read or write operation continues until the CE stop latch is turned on. If the start and stop registers develop a match, a control word cycle is initiated to place the contents of the channel selection switches into the start and stop registers. This allows a continuous read or write operation to be performed.

Control Word Minus Position. With a control word minus sign available, the tape read or write operation continues until the start and stop registers develop a match signal. With a match signal and the minus sign, the end of the operation is signaled and a final status word cycle is initiated. Whether the CE operation is to be automatically repeated is dependent upon the setting of the repeat-single cycle switch.

Normal-Check Stop Switch

Normal Position. With the switch set in the normal position, the CE operation continues until the CE stop switch is depressed or until the normal end of a tape operation is developed.

Check Stop Position. With the switch set to the check stop position, all continuous CE tape operations are prevented if an error condition is sensed (Cond #1).

5.2.00 CE READ OPERATION

The CE read operation uses the normal tape channel read circuits with the exception that all status words, control words, and data word requests are confined to the 7604 unit. To perform a CE read operation, the following CE control switches must be selected:

Set Channel Select Switch
Set CE Ctrl to Tape
Select Tape Drive
Set Operation Switch to Pos 1
Set Channel Position Switches
Set Data Word Sign
Set Control Word Sign
Set Repeat-Single Cycle Switch
Set Normal-Check Stop Switch
Depress CE Start Switch

5.2.01 CE Op Code Analysis

The CE Op Code is analyzed in the same manner as a normal tape operation, with the exception that all external signals are furnished from the CE panel instead of A & P.

The tape operation is determined by the setting of the CE Operation switch. The output of this switch is used to develop the CE field register units position (position 5 of a normal tape instruction). The CE field register units position and a CE Tape Op signal are switched to develop the Tape Call A Gate (Figure 5.2-1).

The tape drive is determined by the tape drive select switch setting. The output of this switch simulates the field register tens position (position 4 of a normal tape instruction).

To initiate a CE operation, the CE start latch is turned on by the depression of the CE start button. This latch being on develops a CE A & P address and information gate which functions in the same manner as the A & P gates. For a detailed explanation of the normal operation code analyzation, refer to section 3.1.02.

The main differences between a CE operation and a normal tape operation are (1) the confining of the restart signal to the 7604, and (2) the reading in from the channel select switches to buffer B. The reading-in of the channel select switches simulates the instruction word read-in at the beginning of a normal tape operation.

The tape channel interlocks when the CE control switch is placed in the tape operating position.

5.2.02 CE ISW Cycle

With the tape channel interlocked, an initial status word cycle is initiated. The CE ISW cycle differs because the memory request to store the ISW is prevented from reaching the 7602 unit. Each time a memory request is initiated, a CE address and information gate is developed. These gates provide the necessary timing to simulate the ISW cycle.

The remainder of the ISW cycle is performed in its normal manner with the exception of the interrupt sign analysis. During normal operations, as the ISW is read out to the information bus, positions 6-9 and the sign are placed onto the distributor bus. Positions 6-9 are read into the control register A and the sign determines if an interrupt is to be performed at the completion of the operation. During CE operations sign analysis is inhibited due to the CE on signal.

5.2.03 CE Control Word Cycle

The main difference between a CE control word cycle and a normal control word cycle is that all control word memory requests are confined to the 7604. In addition, the start and stop addresses are specified by the channel selection switches (2-5 start 6-9 stop) and the control word sign is specified by the control word sign switch.

At the completion of the ISW cycle, a control word memory request is initiated. With the normal memory request inhibited, the CE address and information gate is developed.

During the CW read-out cycle, the contents of the channel selection switches are read into buffer B. With the start and stop addresses in buffer B, a control word Xfer RI cycle is initiated to transfer the buffer B contents to the start and stop register. During normal operations, the control word sign is analyzed as this transfer is made. However, during CE operations, the sign is specified by the control word sign switch.

During the control word cycle, the control register A contents is increased by one. This operation is performed in the same manner as a normal tape operation.

5.2.04 CE Data Word Cycle

The reading of a tape is performed in the same manner as explained in Section 3.0.00. The main differences are the inhibiting of the start address from being placed on the sync addr bus and the inhibiting of the tape words from reaching core storage during the data word cycles.

At the completion of the simulated data word address gate cycle, the normal 0-up start operation is performed. If, at the completion of the 0-up operation a mismatch is sensed, the 1-up start operation is performed.

The CE read operation continues in this manner until a match is sensed at the completion of the 0-up start operation.

5.2.05 CE Final Status Word Cycle

A final status word cycle is developed if a control word minus signal is present when a match is sensed between the start and stop register. The CE final status word cycle is performed in much the same manner as explained in Section 3.0.00, except for inhibiting of all memory requests.

During the final status word read-out cycle, the buffer B read-in from the information bus is inhibited. This allows the contents of the channel select switches to be read into buffer B to simulate the final status word RO. The development of the final status word in buffer B is performed in the same manner as explained in Section 3.0.00

With the final status word developed in buffer B, a final status word read-in cycle is initiated. During normal operations, this cycle causes the contents of buffer B to be transferred to its specified core storage location. However, during a CE operation, the Memory RI gate is prevented from being developed and this prevents the read-out of buffer B onto the information bus.

5.2.06 Continuous CE Operations

The CE panel performs a continuous read or write operation by developing a control word plus sign instead of a minus sign. With a plus sign available, a control word cycle is initiated each time a match is sensed. This allows the tape operation to continue its read or write operation until the CE stop switch is depressed.

If the control word sign is minus and the repeat switch is set, the tape read or write operation is repeated at the completion of the final status word cycle. This is accomplished by setting the CE start latch which develops the CE Addr and Info Gates (Figure 5.2-1).

During a CE operation, the CE has the ability to stop the continuous tape operations if an error is detected, by setting the normal check stop switch on Check Stop. When an error is detected, the error circuits function in their normal manner (refer to section 4.0.00).

With an error detected and the check stop switch on, the CE stop latch is turned on (67.61.00). The stop latch resets the control word plus latch and sets the control

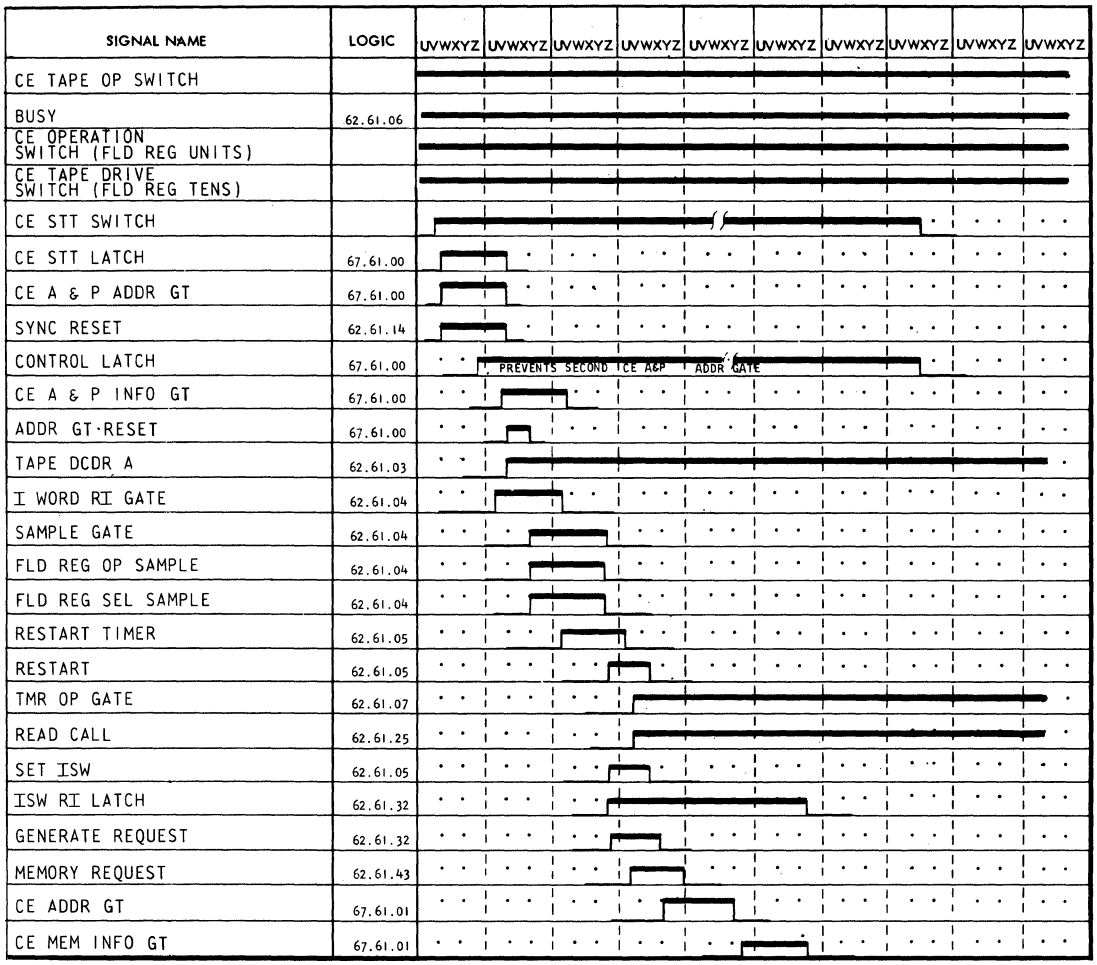


FIGURE 5.2-1. CE READ OP CODE TIMING

word minus latch. This latch prevents the CE start latch from turning on if the repeat switch is set.

5.3.00 CE WRITE OPERATION

The CE write operation is performed in much the same manner as described under the CE read operation except for data word cycles.

5.3.01 Write Data Word Cycle

During a CE write operation, as the control word is placed into the start and stop register, a data word request is initiated. The simulated data word request prevents the tape start register from reading out to the sync address bus and inhibits the memory request from reaching the 7602 unit. Each time a data word request is performed, the contents of the channel position switches are read into buffer B.

With the first word placed into buffer B, the start register is 0-upped to check if more than one word is to be written on tape. At the completion of the 0-up operation, the first data word transfer operation is developed to transfer the first data word from buffer B to buffer A.

With a mismatch signal available at the completion of the 0-up start operation, a 1-up start operation is initiated to increase the contents of the start register by one. At the completion of the 1-up operation, the second data word request is initiated to read in the second data word from the channel position switches.

The CE write operation continues in this manner until a match is sensed at the completion of the 0-up start operation. With a match sensed, the control word sign is analyzed for a continuous-write operation or an end-of-write operation. With the previous control word sign plus, a control word cycle is initiated and the write operation continues.

If a minus control word sign is sensed, a disconnect operation is sent to TAU and a final status word cycle is developed.

At the completion of the final status word cycle, the tape-write operation can be repeated if the CE repeat switch is set. During a CE repeat operation, the write operation is performed after the final status word cycle.

5.4.00 TAPE MOVEMENT CODES

The CE tape movement codes are specified by the operation switch setting at position 0. With the switch in this position, the 9th position of the channel position switches further specifies the tape movement instructions.

The differences between the normal tape movement and the CE tape movement instructions is the confining of all memory requests to the 7604 unit and the use of the CE address and information gates. For a complete explanation of the tape movement codes, refer to section 3.3.00.