7095 CHANNEL SIMULATION STUDY

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CHANNEL SIMULATION - COMPATIBILITY MODE STUDY

INTRODUCTION

I.

This report presents the results of evaluation and study of the IBM 7095 data channel logic. It briefly discusses the 7095 channel logic and makes certain recommendations for changes to be made for 7095 operation. 7094 Input/Output compatibility and simulation techniques are also discussed, with emphasis on modifications or additions to the 7094 system.

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7095 CHANNEL LOGIC

2.

II.

The following comments and recommendations are based upon <u>7095 Data</u> Channel, Functional Objectives, dated 3/16/64.

Input/Output Instructions

1. The start channel (STC) and channel test (CHT) instructions require a channel select word while the store channel (SCH) and halt channel (HCH) require no additional word because the channel number is specified in the operation code. This inconsistency was also present on previous machines, and it seems advisable to eliminate it in the 7095 design by making all Input/Output instructions the two-word type.

It will be useful from the programming standpoint to standardize all Input/Output instructions as two-word instructions.

It is stated that the restore channel traps (RCT) instruction restores channel trapping for only those channels not inhibited by the most recent inhibit channel traps (ICT) instruction. The implication is that channels inhibited by an ICT can only be restored to trapping status by a subsequent ICT. However, this is not clearly delineated in the descriptions of the ICT and RCT instructions.

The RCT instruction should be defined as Release Automatic Inhibit (RAI), and the ICT should be defined as Set Channel Trapping (SCT) good to clarify the operational effect of the instructions and to avoid confusion with 7094 instructions that do not perform the same functions.

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Channel Commands

1.

It is not clear what significance the address field has for Control Unit Operations which require a Data Control Word (DCW).

Using the address field of commands which require DCWs will eliminate the need for a transfer channel (TCH) if the DCWs are not in sequential order.

2. The responses of the channel to the following combinations of commands are not clear.

a. A DCW is encountered after an unchained DCW with the current command set to Advance.

b. An end signal is received near the beginning of a long string of chained DCWs with the Advance bit set in the current command.

c. A DCW is encountered when the channel is not operating under a current command that requires a DCW.

d. The current command requires a DCW and the next location contains another command not of the sequence type.

To facilitate the handling of short-length records, the channel should disconnect and trap on end signal if the next sequential command is a DCW, regardless of the status of the advance/disconnect bit. Otherwise, much time might be wasted by the channel searching through a list of DCWs and sequence commands intended for the processing of a longer record in order to find a command that signals a disconnect. In general, improper combinations of commands should cause a trap and disconnect, and the trap status indicator for the channel set to indicate "Input/Output sequence error. "

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Channel Trapping

2.

1. It is not clear which channel indicators or registers will be kept intact by the channel after a disconnect. As an example, must a new enable (ENB) command be given each time the channel is started?

To aid the simulation package, the channel should retain all registers and indicators until a new STC instruction is given.

Is it possible to give the command ENB with the disconnect bit set such that the channel is not in a transmitting condition but is conditioned to generated attention traps?

Changes in device status, such as completion of a rewind or changing from not ready to ready status, should be able to cause attention traps at any time.

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III. SIMULATION CONCEPTS

7094 Input/Output Compatibility

For almost all of the operations codes listed in <u>7095 File Memo #6</u>, dated 3/5/64, the compatibility trap feature for the 7094 compatible mode provides a direct efficient manner for entry into groups of 7094 Input/Output simulation routines. However, to avoid simulating the non-IO \pm 0760 class instructions, further analysis of the codes in the address fields of the \pm 0760 class instructions is required before an Input/Output compatibility trap is generated.

Input/Output Status Testing

The instructions which test channel status indicators will require that the simulation routines maintain pseudo-status indicators for each simulated 7094 channel. These indicators will be set from the results of 7095 CHT operations and trap status indicators to determine the proper simulation response. Those test instructions which reset the indicators will result in resetting the simulated indicators when the indicator is "on". The test instructions which are dependent upon the ENB mask for the channel will be treated according to a pseudo-mask to determine whether the instruction should be considered "active".

Channel Overlap

Operations on different channels will result in different relative timing due to the intervention of the simulation packages and to the differences in devices actually operated.

Operations which in normal 7094 configuration deal with different channels, but which refer to actual 7095 devices attached to the same channel, will be performed sequentially, rather than overlapped, unless automatic channel switching is available.

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7607 Time Dependent Operations

If 7094 interrupts are enabled, any command sequence which ends in an IOCT will be considered, for simulation purposes, to be completed instantaneously and cause an interrupt. With 7094 interrupts prevented, a load channel (LCH) instruction is accepted, irrespective of timing, if there is more information available. It is not feasible to attempt to simulate 7094 CPU/channel timing.

Additional 7909 Channel Requirements

All of the above considerations will be generally applicable to 7909 channel simulation. Additional coding will be required to maintain sufficient pseudo-registers to simulate the full range of operations which can be performed with the 7909 channel logic. Direct simulation of the 7909 channel involves considerable interpretation during the compatibility interrupt. Not only must the actual input-output aspects of the 7909 channel be analyzed and reconstructed in terms of the 7095 channel; but the control, register, and channel interrupt facilities of the 7909 must all be simulated as well. Since the 7095 I/O interrupt philosophy is one of minimum-duration activity, this simulation must occur during the compatibility interrupt, with consequent delay of the main program. This delay encompasses the time required to simulate both the 7909 channel program and its interrupt program. Considerable overhead is required, for example, to simulate the 7909 assembly register feature of retaining the last transmitted word.

System Input/Output Routines

It appears at this time that the most efficient approach to System Input/Output routines which are either completely self-contained or which use standard select routines, is to replace such routines with equivalent 7095 routines. The method employed will be to leave the compatible mode, initiate the Input/Output directly on the 7095 channel, and then reenter the compatible mode.

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Simulation Techniques

1. Simulation Conclusions

From known experience with direct couple simulation and proposed 7095 hardware characteristics, simulation appears to be feasible using either direct or buffered simulation, as applicable.

2. Direct Simulation

If the Select Routines used by a particular program do not involve selfmodifying channel command sequence, it appears feasible to perform the Input/Output simulation on a dynamic basis. In this type of operation, the referenced channel commands will be interpreted after a compatibility trap for an Input/Output select and the equivalent 7095 channel operations will be started. At the 7095 trap time the results of the operation will be checked, the appropriate "7094" status indicators set, and a determination will be made as to whether a 7094 "trap" is appropriate. If it is, a transfer equivalent to a trap will be made.

3. Simulation with Buffering

If self-loading command sequences are to be simulated, the data will be searched for the modifying 7094 commands. These commands, which signify the amount and destination of the data, will be simulated by appropriate core-to-core transfers. Record size will be maintained in simulation up to about 12,000 word records. The selection of the method of simulation to be used (direct or buffered) may be indicated by a control card option.

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