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Design of Monolithic Circuit Chips

Abstract: The influence of semiconductor chip design on the logic partitioning of a computer is discussed and some design rules are given. A chip size of 60 × 60 mils with 24 terminals and 168 components was shown to be optimum. RF-sputtered quartz insulation was used for multilevel wiring and a hermetic seal. Using a master chip technique, a 9-part-number logic set was successfully fabricated. Propagation delays for the circuits were 2.5 to 3 nsec.

Introduction

Functional multicircuit monolithic chips, such as binary counters and shift registers, have been available for some time. Most monolithic systems use unit logic supplemented with these few general functions. A more efficient system can be realized if the logic of the computer is partitioned into unique functional blocks. This paper describes the design of such monolithic functional blocks that are custom tailored for specific machines.

The need for automated assembly of these functional chips to packages requires standardization of both chip size and terminal configuration. One of the first choices to be made in the semiconductor area is maximum chip size and component density. When a maximum chip size has been chosen, two ground rules can be stated for the logic designer. One is the total number of components which will fit onto the chip. The second ground rule is the number of terminals available for input-output. This number is a function of the semiconductor-package interface, where requirements of automatic handling and terminal bonding dominate. These are the two constraints within which the logic designer must partition his machine.

The philosophy of chip logic partitioning has been discussed at length by other authors.[1,2] It is evident that the best partitioning will result from due consideration of the total system. Items of special concern are machine organization, logic design, circuit logic power, packaging, facility for change or repair, manufacturability, and total system cost.

This paper will describe the factors which influence the design of semiconductor chips. Logic and circuit design, component design, optimum chip size and wireability for monolithic computer chips will be discussed. Chips using sputtered quartz as an insulator to permit multilevel wiring will be described and the results of a chip set generated with this technology will be shown.

Circuits

The choice considered here was between current switch logic (CSL) and diode transistor logic (DTL). An analysis of these two logic systems for speed, power and circuit utilization was completed.[3] It was determined that for a given IBM System/360 computer with 10 nsec machine speed (raw circuit delay + wire delay + loading) the normalized relations shown in Table 1 could be obtained. For machine speeds of faster than 10 nsec, DTL becomes even less competitive.

Other considerations were ease of process and parameter control for each circuit family. Since the current switch circuitry is nonsaturating, it eliminates the need for storage time control and also relaxes the requirements on the collector saturation voltage. The junction breakdown voltage requirements for this circuitry are lower because of the lower-voltage power supplies, and high-value (large area) resistors are not required. The current switch circuitry does require V_{eb} and resistor tracking, both of

Table 1 A comparison of normalized relations for diode transistor logic and current switch logic.

	DTL	*CSL*
Power	1.75	1
Total components	2.0	1
Number of different circuit configurations	1.70	1
Quantity of circuits used	1.80	1
Number of power supplies	0.67	1

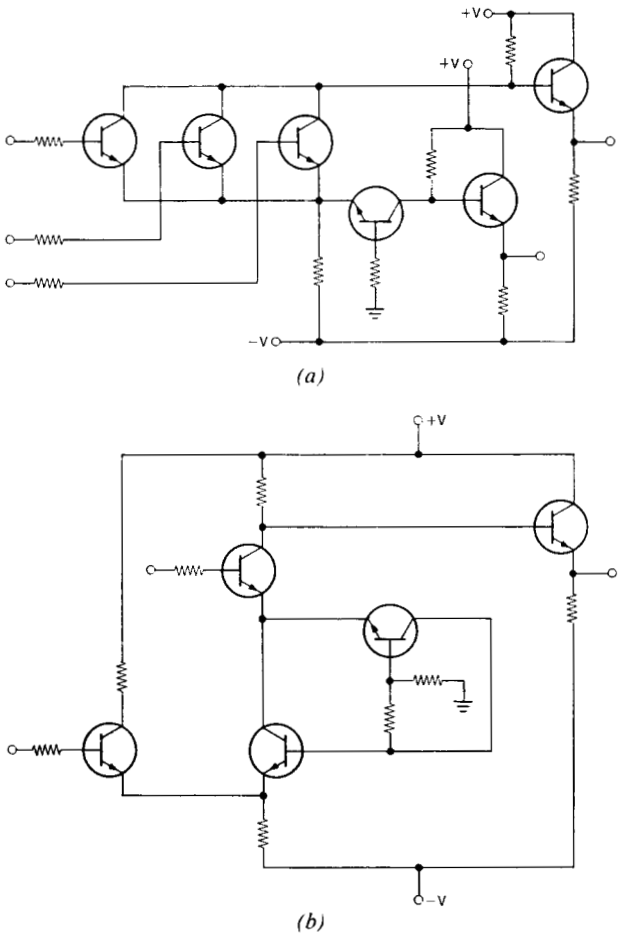


Figure 1 (a) The current switch emiter follower circuit; (b) the cascode circuit.

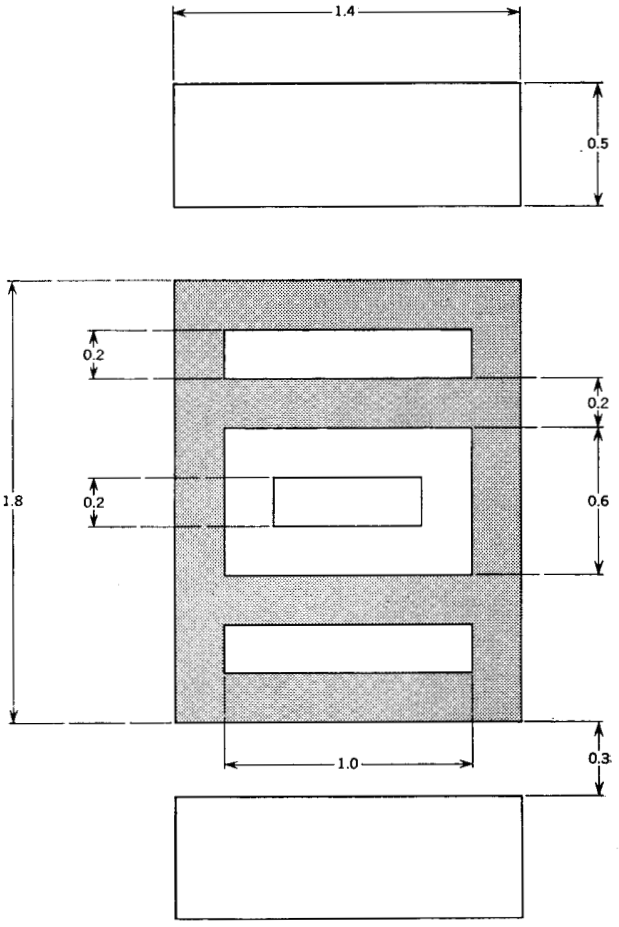


Figure 2 Transistor geometry variations.

which are natural products of monolithic circuits. Based on all the above factors, the current switch circuit family was chosen for this study.

Two variations of the current switch circuits were used (Fig. 1), the emitter follower and the cascode circuit. They both require three voltage supplies (+, −, and ground). The circuits were designed to the following component specifications. A resistor within any circuit on any chip must be within $\pm 13\%$ of its design value. All resistors within one circuit must track within 5%. The beta of any transistor must be between 25 and 75. The emitter-base voltage (V_{eb}) for all transistors must be within ± 25 mV of its design value. The V_{eb} of all transistors within any one circuit must track within 5 mV of each other.

The transistor design was influenced by the circuit current and speed, and by mask fabrication tolerance. Mask tolerance was a prime consideration as the interest was in large arrays with high yields; therefore, the minimum tolerance used was 0.2 mil. Figure 2 shows the transistor geometry designed for these conditions.

Table 2 lists the resulting device parameters and the circuit performance of a four-input current switch tested as shown in Fig. 3.

These circuits were fabricated with techniques compatible with those used in the industry or described in the literature.[4] P-N junction rather than dielectric isolation was used to electrically separate the individual circuit elements.

Optimum chip size

The merit of a computing system is normally measured by its cost/performance ratio. A major factor in determining this ratio is the cost per circuit and the circuit density in the computer. Both factors can be directly related to yield.

The subject of monolithic integrated circuit yield has been previously considered by several authors, among them B. T. Murphy[5] and E. A. Sack.[6]

Murphy has theoretically treated the case of a circuit consisting of N identical components. Based on this assumption, he has predicted that a yield-area relationship

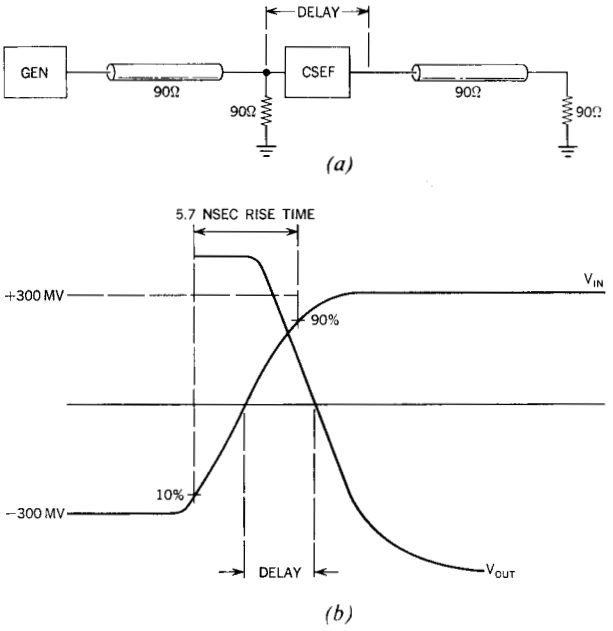
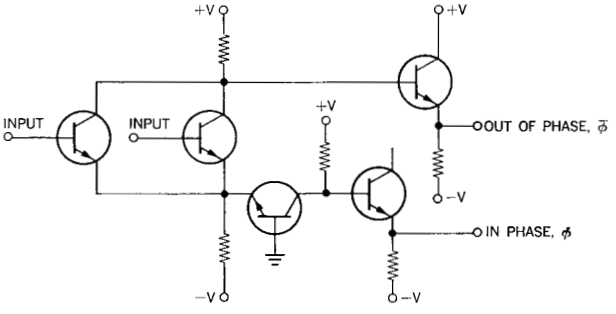


Figure 3 (a) Schematic of the test circuit; (b) input and output waveforms.

Table 2 Transistor and circuit characteristics

Emitter width (mils)	0.6
Emitter length (mils)	1.0
V_{be}@ 4 mA (Volts)	0.790
h_{fe}@ 1V I_c = 4 mA (mc),	600
h_{FE}@ I_C = 4 mA	30
Circuit power in mW	22
In-phase propagation delay (nsec)*	2.80
Rise time (nsec)	4.73
Fall time (nsec)	4.33
Out-of-phase propagation delay (nsec)**	2.97
Rise time (nsec)	6.65
Fall time (nsec)	5.32



* "In-phase propagation delay": the input signal and output signal are rising or falling toward the same polarity.
** "Out-of-phase propagation delay": the input and output signals are always approaching opposite polarities.

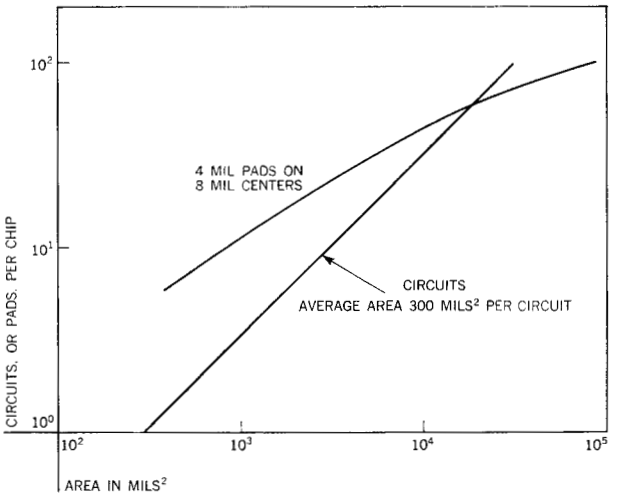


Figure 4 Circuits and terminals vs chip size.

must exist and that the component yield is a maximum at a chip size which is determined primarily by the spot defect density. As a result, he finds that the optimum chip size lies between 20 and 60 mils square for a wide range of parameter values. The predominant yield loss was attributed to spot defects such as diffusion pipes and oxide pinholes introduced at the various masking steps.

For the purposes of our study, it was essential to find the optimum chip size, so that the logic could be partitioned most effectively. A figure of merit for optimum chip size was defined as:

$$\text{Figure of Merit} = (\text{Yield})\left(\frac{\text{Circuits}}{\text{Chip}}\right)\left(\frac{\text{Chips}}{\text{Wafer}}\right),$$

where yield refers to the percentage of chips at final test that meet functional voltage level specifications. The yield is a function of chip size and component density, and is subject to improvement as technology advances.

Chips with low circuit count are undesirable because they are essentially unit logic, and therefore the chip size is a function of the number of terminals only.

High-speed automatic chip handling precludes the use of the scribe and break techniques for chip dicing. Gang sawing is adequate but results in a 4 to 5 mil kerf, which reduces the efficiency of the fabrication process for small chips, since it drastically reduces the number of chips each wafer will yield.

For circuit-limited chips, with the technology used, the average area per circuit was 300 mil^2. The average circuit contains 5 transistors and 5 resistors. The relationship between total number of circuits and chip area is plotted in Fig. 4. The maximum number of terminals for each chip area is also plotted in the same Figure. The terminals were restricted to the periphery of the chip and were 4

Table 3 Comparison of three chip sets

	Set A	*Set B*	*Set C*
Number of chips in set	18	8	9
Number of pads	24	18	24
Maximum components used	195	56	111
Average components used	94	36	77
Chip size in mil²	7800	2000	3600
Mil² per average component used	83	55	46

mils in diameter on 8 mil centers. These tolerances were necessary to permit automatic simultaneous terminal-to-package connections. For any given chip size one can determine from Fig. 4 the maximum number of circuits and terminals that are available to the logic designer.

Experiments were carried out to establish the yield vs the number of circuits per chip for the technology being used. The results of these experiments are shown in Fig. 5 for typical and best cases. Using the typical case in conjunction with the information on chip size in Fig. 4 the figure of merit can be calculated. Figure 6 is a plot of the figure of merit vs. chip size. Since the curve peaks at 60 × 60 mils, this was the chip size chosen. This chip has a maximum of 12 circuits and 24 terminals. The reason for the lower figure of merit for small chips is that for less than approximately 8 circuits the chip size is determined by the number of terminals and not by the circuit count. This wastes silicon area and the dicing kerf wastes additional area. Both of these factors reduce the Chip/Wafer ratio used to calculate the figure of merit. For chips larger than 60 × 60 mils the yield factor dominates.

Logic partitioning

Several chip sets have been designed based on a study of a specific IBM System/360 computer. The early chip sets designed prior to the determination of the figure of merit demonstrated that without a knowledge of semiconductor fabrication requirements the logic designer may design a very inefficient chip set. With proper information a much more balanced result is obtained. A comparative study of three chip sets is shown in Table 3.

Set A was designed around a twenty-four terminal limitation and resulted in an excessive spread between the maximum and average number of components per chip. This forced a large, inefficient chip. Set B was designed under the restriction of six circuits per chip maximum. In this case the logic designer used eighteen terminals, which again forced a large, inefficient chip.

Set C was designed under the ground rules for the maximum number of circuits and terminals on an optimum 60 × 60 mil chip. This set has the minimum silicon area per average component used.

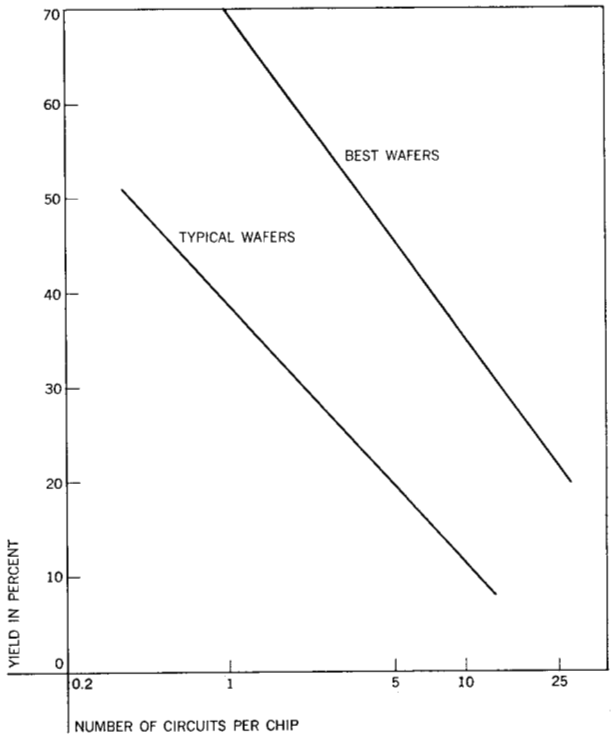
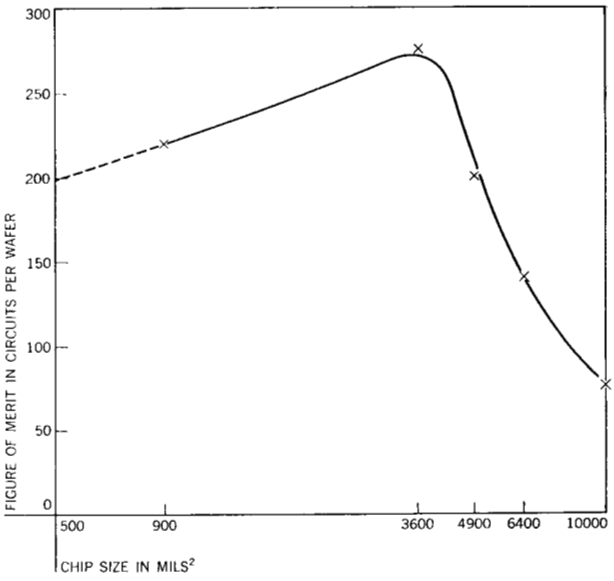


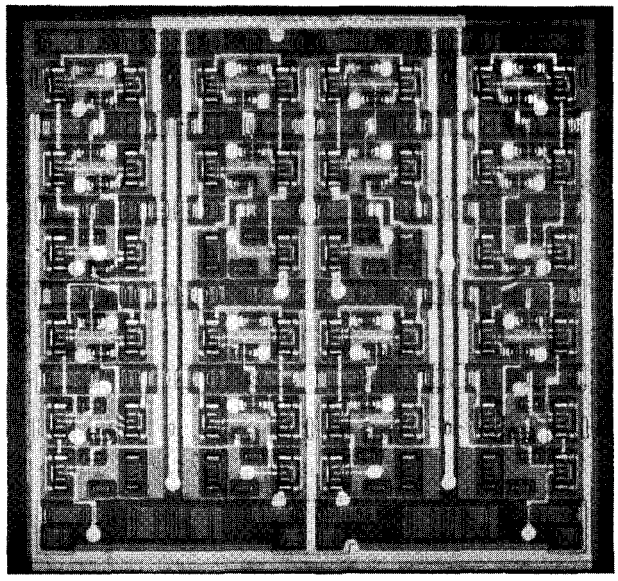
Figure 5 Yield vs number of circuits per chip.

Figure 6 Figure of merit vs chip size.

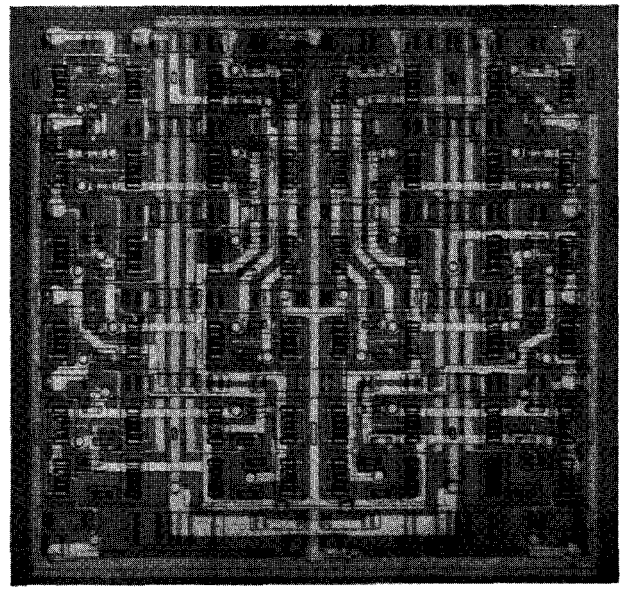


Chip design

The semiconductor chip designer cannot consider any logic set complete because of the continuing need for special machine features and engineering changes. This fact, coupled with the fixed chip size and terminal locations,



(a)



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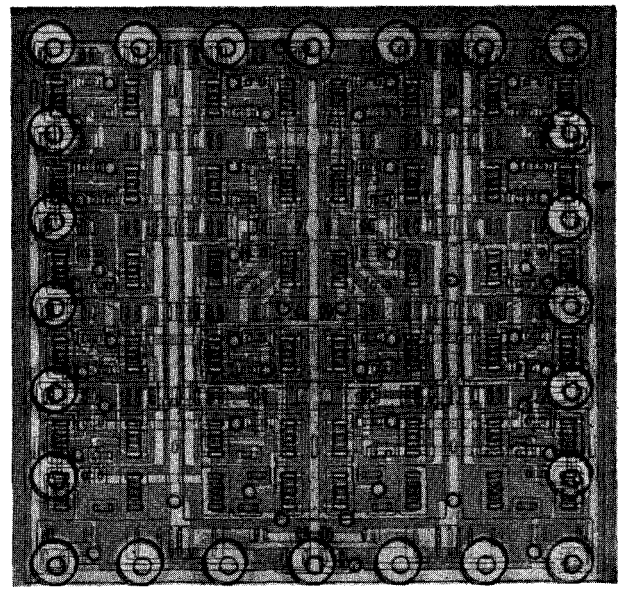

(c)

Figure 7 Microphotographs and chip fabrication sequence (a), (b), and (c).

leads naturally to a master chip approach. A master chip silicon wafer is designed such that only new interconnection patterns are necessary to implement a new chip design. This allows new designs to be completed quickly and permits low-cost generation of part numbers. Each 1.25-inch diameter wafer contains an array of approximately 250 identical master chips. Each master chip consists of an orderly array of components that have been designed to be wireable into any combination of circuits in the circuit family. The master chip must be made general enough to accommodate future logic designs without compromising the density with redundant components or extra wiring channels. These future logic designs are bound by a set of equations which can be derived from the master chip. For the Set C chip these equations are:

$$(\text{Circuits}) + (\text{Inputs}) + (\text{Emitter Followers}) + (\text{Clamped Outputs}) \leq 48 \quad (1)$$

$$(\text{Circuits}) + (\text{Undotted Emitter Followers}) + (\text{Groups of Dotted Emitter Followers}) \leq 24 \quad (2)$$

$$(\text{Circuits}) - (\text{Dotted In-Phase Current Switch Outputs}) \leq 12 \quad (3)$$

$$(\text{Circuits}) - (\text{Dotted Out-of-Phase Current Switch Outputs}) \leq 12 \quad (4)$$

$$(\text{Clamped Outputs}) \leq 4, \quad (5)$$

where: a clamped output consists of a transistor-resistor network which fixes the level of the output;

dotted emitter followers share a common emitter resistor; and

dotted collectors share a common collector resistor.

Satisfying these equations is a necessary but not sufficient condition for a new part number. The final criterion for each new part number is its wireability.

The wireability of the chip is a function of the position

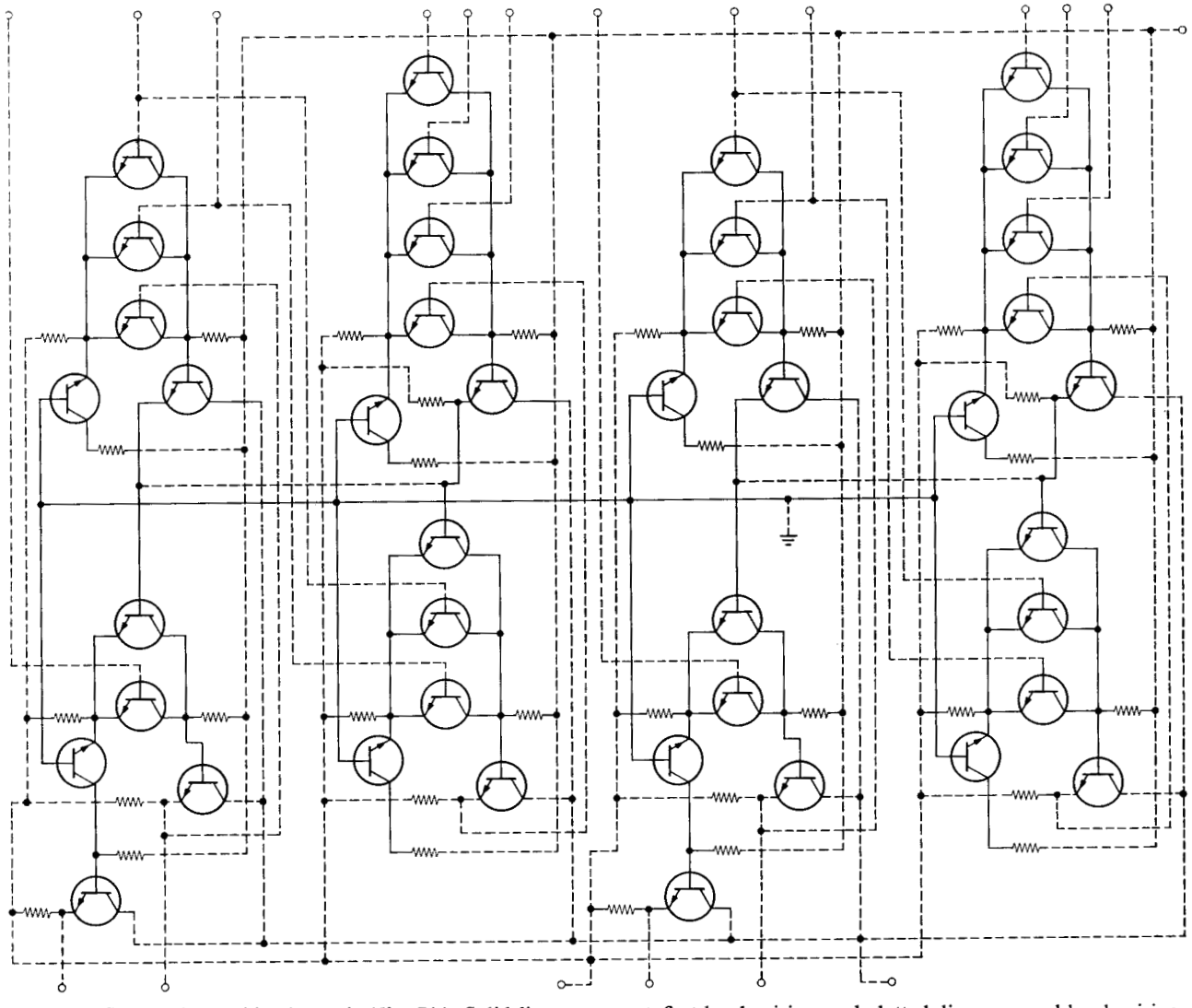

Figure 8 Schematic of chip shown in Fig. 7(c). Solid lines represent first-level wiring and dotted lines, second-level wiring.

and number of available components. The resistor placement has a major effect on wireability. We have chosen to utilize the resistors to the fullest possible extent by considering them part of a fixed power supply distribution system. This allows the routing of three power supplies on one level of metallization.

The transistors and resistors are positioned so that any current-switch circuit can be efficiently wired. The components are wired into individual circuits and connected to the power supply distribution system with this first level of metallization. The interconnection of these circuits into their logical function requires a second level of metallization.

The insulating layer between these two levels of interconnection is accomplished by RF sputtering[7] a 1.5-micron film of silicon dioxide over the first level of metallization. "Via" holes are chemically etched through the silicon dioxide layer using photoresist techniques prior to the deposition of the second level interconnections. The RF sputtering technique is again used to deposit another 1.5-micron silicon dioxide film over the second level interconnections. Via holes are then etched and metal terminals are evaporated around the periphery of the chip.

The sputtered quartz and the refractory metal used in the terminals provide a hermetic seal for the semiconductor and its interconnection metallurgy. The interconnection sequence is shown in Fig. 7. A schematic of this same chip is shown in Fig. 8.

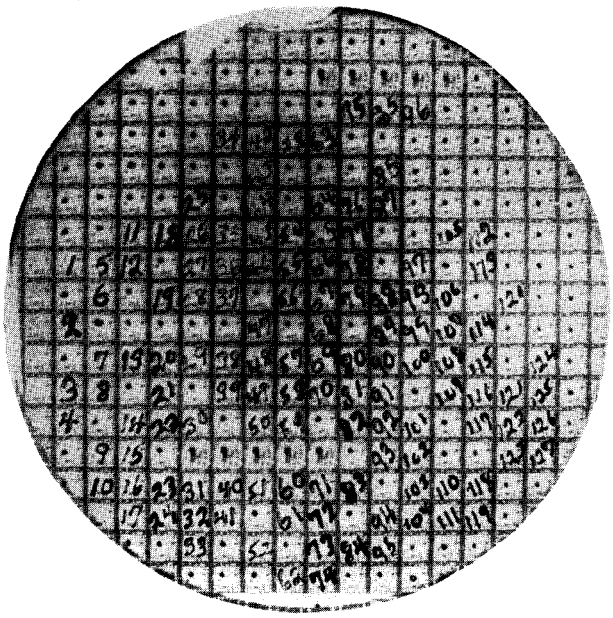

Figure 9 High-yield wafer.

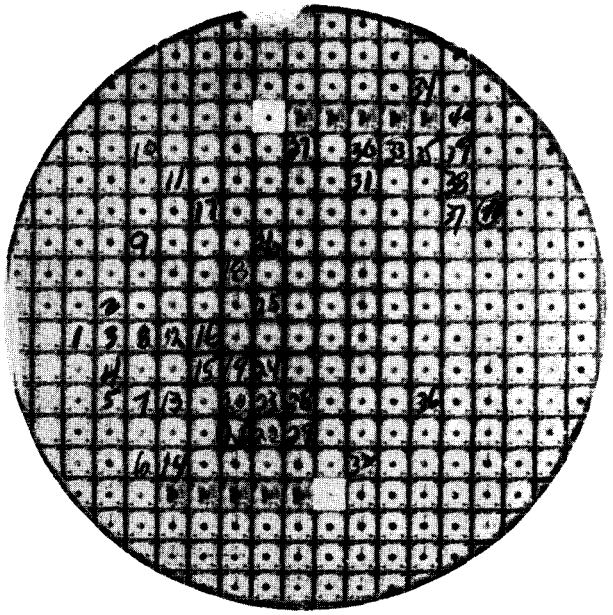

Figure 10 Typical-yield wafer.

Results and conclusions

It has been shown that an efficient common chip can be designed to implement a complete set of functional logic blocks providing certain logic partitioning rules are followed.

The nine part numbers in Set C have been designed and fabricated. The nine separate part numbers, each with its specified logic function, have the general appearance of Fig. 7(c). These functional blocks have been fabricated with reasonable yields. Figure 9 is a photograph of a high-yield wafer. The good chips are numbered on the photograph. Figure 10 is a photograph of a typical wafer. These yields confirm that this chip set was consistent with our predictions and our technology.

Testing and failure analysis of these functional chips were more difficult than anticipated, and this points out a problem area for chips with larger logic functions. Testing will become particularly critical when optimum chip size increases to include more circuits and greater functionality. The optimum chip size will increase as the figure of merit increases becauses of yield improvement. The increased functionality of larger chips and the broad spectrum of computer logic design will dictate a multitude of part numbers. While the common-chip concept reduces the part-number generation problem, the task of designing and checking the artwork is still overwhelming unless computer-assisted design techniques are available. Such techniques are now being developed to generate instruction tapes for an automatic artwork generator. With this system and improvements in photomask technology more complex chips with much smaller devices for high-speed circuitry will be investigated.

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