S. Magdo

Theory and Operation of Space-charge-limited Transistors with Transverse Injection

Abstract: The development of a new device, called the space-charge-limited (SCL) transistor with transverse injection is reported in this paper. A theoretical model for space-charge-limited transistors, both npn and pnp, on high-resistivity silicon substrates is described and a quantitative analysis is given. Experimental results for SCL transistors are presented to support the model's validity. According to the model, current in SCL transistors is controlled by the base of a parallel-connected lateral transistor in two ways. First, the base of the parallel transistor controls the potential step in the high resistivity base of the SCL transistor. Second, the base of the parallel transistor injects carriers in the direction transverse to the SCL current flow. These carriers are of types opposite to those that carry the current flow in the SCL transistor and thus partly neutralize the space-charge in the current flow. The carriers propagate, predominantly by drift, across the high-resistivity base region of the SCL transistor. The resulting base transit time is about two orders of magnitude faster than that of a bipolar transistor with equal base width. No charge storage takes place in saturation. These features and the very low device capacitances make the SCL transistor attractive for low-power, fast-switching applications. Current gains as high as 70,000 are obtained at low current levels. The current gain decreases at higher current levels because the parallel lateral transistor turns on. It is also demonstrated that complementary pairs of SCL transistors can be fabricated with three masking steps, including metalization.

Introduction

Space-charge-limited current in vacuum tubes is well-known to be proportional to $V^{\frac{3}{2}}/d^2$, where V is the applied voltage and d the interelectrode distance. A similar law for one-carrier current through semiconductors or insulators was developed by Mott and Gurney [1] before the invention of transistors in 1940. According to this law, the current is proportional to V^2/d^3. The difference comes from the fact that electrons travel with constant velocity in semiconductors and with constant acceleration in a vacuum. After the invention of the transistor, authors such as Shockley [2], Rose [3], Smith [4], Lampert [5], and Wright [6,7] analyzed and reported space-charge-limited current in insulators and semiconductors.

The SCL transistor, termed the "analog transistor" was originally proposed by Shockley [8]. Later, other authors [9,10] described similar devices. However, the practical realization of SCL transistors has, to our knowledge, not been reported. Most of the proposed devices have embedded grid structures which are, technically, not feasible. In addition, none of the structures is compatible with planar technology.

The space-charge-limited current in previously reported SCL transistors is controlled by varying the electric field in the high-resistivity base region with a control electrode analogous to the grid in a vacuum triode. The SCL transistor described in this paper operates in a fundamentally different way. Here the space-charge-limited current in the high-resistivity base region is controlled by transverse double injection as well as by electric field variation. The injected carriers are of types opposite to those that carry the current and thus partly neutralize the space-charge in the current.

This paper describes the theory and operation of SCL transistors and presents some dc test results. The structure of complementary SCL transistors and their operation in switching circuits was described recently [11]. Complementary SCL transistors with cut-off frequency values between 800 and 900 MHz were fabricated on 30kΩ/cm substrates with three masking steps. Delay-times of 45ns were measured in inverter circuits with discrete SCL transistors having 5pF loads. The power dissipation was 12μW per stage. Both npn and pnp SCL transistors turn on at much lower forward bias than bipolar transistors, and supply voltage can thus be significantly reduced. Complementary pairs have been operated in a flip-flop circuit with supply voltages as low as 0.37V. The corresponding standby power was 35nW. Results also indicate that device capacitances are much lower for SCL than for bipolar transistors. The leakage resistance between adjacent collectors is about 5nA at 1V.

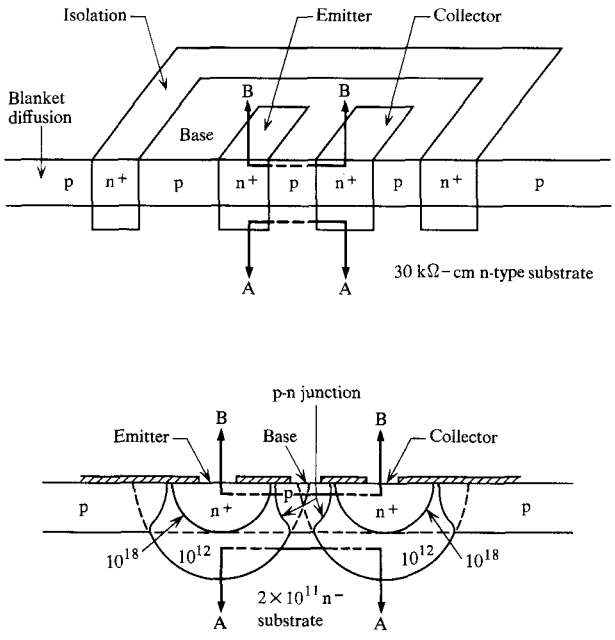


Figure 1 npn SCL transistor structure. The numerals in the detailed portion are doping level orders of magnitude.

Description of SCL transistors

Complementary transistor structures [11] are shown in Fig. 1 (npn) and Fig. 2 (pnp), respectively. The npn transistor has a striped structure with identical emitter and collector. The pnp transistor has an enclosed structure with a collector surrounding the emitter. The two structures, however, can be interchanged for npn and pnp transistors. The fabrication of the complementary pair requires only three masking steps.

The SCL transistor is a combination of a bipolar lateral npn transistor (Section B-B in Fig. 1) and a parallel-connected nn^-n SCL transistor (Section A-A in Fig. 1). The principle of operation can be described as follows. If zero bias is applied to the base and a positive voltage to the collector of the upper npn transistor, the currents will be cut off in both the upper npn and lower SCL transistors. The high resistivity n^- base of the SCL transistor is completely depleted by the p base of the upper transistor. This depleted region reaches well beyond the depth of the n^+ regions. The potential step at the nn^- emitter junction of the SCL transistor is smaller than that at the np emitter junction of the upper transistor.

If the base of the upper npn transistor is gradually forward biased, the depleted region in the base of the SCL transistor contracts. This in turn lowers the potential step at the emitter junction of the SCL transistor and electrons will be injected from the emitter into the n^- base. These electrons form a cloud, and thereby a negative space-charge with a potential minimum, in the base. Electrons are drawn from this potential minimum, which takes the role of the emitter junction, toward the positively biased collector. The result is a space-charge-limited current, i.e., a current limited by the repelling force between injected electrons. The electrons travel from the potential minimum to the collector by a drift mechanism. At this stage the current in the SCL transistor is controlled by varying the electric field in its high-resistivity base by means of the bias on the base of the upper npn transistor. According to the Mott-Gurney law [1] the current is proportional to the square of the forward bias. The upper npn transistor is not yet turned on because its built-in voltage at the emitter junction is higher. The current control in the SCL transistor is similar to that of a vacuum triode in which a potential minimum, called a virtual cathode, forms in front of the cathode. The electrostatic field of the control grid (equivalent to the base of the upper transistor) changes the depth of the potential minimum and thus controls the current. The electrostatic field of the plate (equivalent to the collector of the SCL transistor) also influences the potential minimum but its effect is reduced by the electrostatic shielding of the control grid. In the SCL transistor a similar electrostatic shielding reduces the effect of the collector voltage on the potential minimum.

If the forward bias of the upper npn transistor is increased, a second current-controlling mechanism appears in the SCL transistor. Holes will be injected from the base of the npn transistor to the base of the nn^-n SCL transistor since the potential step is reduced at the horizontal pn^- junction. Most of the hole injection is concentrated at the potential minimum in the n^- base because the potential step for holes at the horizontal pn^- junction has a minimum there. The injected holes partly neutralize the negative electron space-charge at the potential minimum and thus increase the collector current of the SCL transistor. It can be seen that the injected holes from the p base to the n^- base also control the current flow in the SCL transistor. The injected holes, however, do not contribute to the collector current. The hole injection varies exponentially with the base bias and thus the I_C-V_{BE} characteristic of the SCL transistor, which started as a quadratic function will change into an exponential one. If the forward bias is further increased, the upper npn transistor also turns on and an increasingly higher percentage of the total current will be carried by the upper transistor. The upper transistor can be represented as an array of parallel-connected transistors with increasing base doping. Thus the turn-on of the upper transistor is gradual.

Since the lifetimes of both holes and electrons in the almost intrinsic n^- region are very long, the current gain β of the SCL transistor is very high at low forward bias.

With increasing bias the current gain drops monotonically to a level corresponding to that of the upper npn transistor. The same is true for the cut-off frequency, F_t. The base transit time of the SCL transistor is about two orders of magnitude shorter than that of the upper npn transistor. This is due to two phenomena. First, carriers in the base of the SCL transistor propagate by drift as compared to diffusion in the upper transistor. Second, the mobility of electrons in the almost undoped base of the SCL transistor is much higher than that of the highly doped base region of the upper transistor. For this reason also, the F_t drops monotonically with increasing forward bias to the level corresponding to the upper transistor.

The same diffusion cycles can be used to fabricate a pnp SCL transistor on the same chip as shown in Fig. 2. The pnp SCL transistor is also a combination of a conventional lateral pnp transistor (Section B-B in Fig. 2) and a parallel connected pn^-p SCL transistor (Section A-A in Fig. 2). The base of the conventional transistor controls the space-charge-limited current in the SCL transistor through the horizontal n^+n^- junction between the two bases. The physical mechanism and the control of SCL current is similar to that of the npn SCL transistor. Of course, the roles of electrons and holes are interchanged and the positive bias on base and collector is changed to negative.

It can be seen that the principle of operation of the SCL transistor is quite different from that of the bipolar transistor. The operation of the bipolar transistor is based upon the principle of charge neutrality. Each charge carrier injected from the emitter into the base is instantly neutralized by an opposite charge carrier via dielectric (or ohmic) relaxation. The dielectric relaxation time for a bipolar transistor is much less than one picosecond. Thus space-charge cannot develop in the base, and carriers propagate by diffusion to the collector.

If space-charge-limited current is to be observed in the SCL transistor, then the dielectric relaxation time in its n^- base region has to be much larger than the base transit time [7]:

$$\epsilon\rho \gg \tau. \tag{1}$$

This requirement means that the resistivity of the base region has to be sufficiently high in order to prevent the injected charge from leaking away by ohmic conduction while traversing the active regions of the device. It also implies that charge neutrality does not hold and thus that conductivity modulation cannot take place at high injection levels. The SCL transistors shown in Figs. 1 and 2, were fabricated on 30kΩ-cm silicon substrates. The corresponding dielectric relaxation time is about 30ns. The transit time calculated from the measured f_t value of

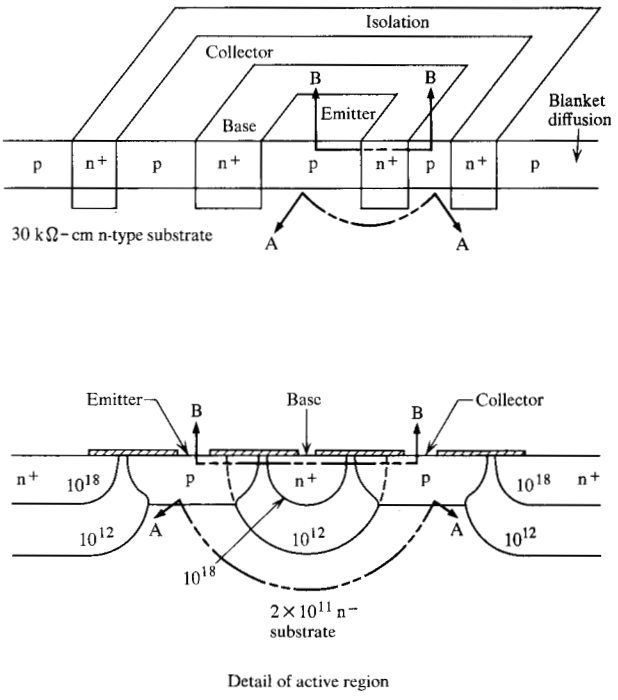


Figure 2 pnp SCL transistor structure.

900MHz is $\tau \approx 1/2\pi f_t = 177$ps. Thus the requirement set forth in (1) is met. This is the first time, to our knowledge, that the practical realization of a transistor structure, which meets the requirement of SCL current flow and operates with transverse injection, has been reported. The Three Mask Transistor [12] has a structure similar to that of the SCL transistor. Its substrate resistivity is, however, 1000Ω-cm, which is too low to satisfy the requirement of (1). The corresponding dielectric relaxation time is 1.0 ns. The transit time calculated from the reported f_t value of 100MHz is $\tau = 1.5$ ns.

The high resistivity substrate itself is a necessary but not sufficient condition for space-charge-limited current flow. The enlarged active regions and the doping levels in those regions for both types of SCL transistor are shown in the lower parts of Figs. 1 and 2. To achieve SCL current in Section A-A of Fig. 1, the two n^+ diffusions (emitter and collector) must be separated by a high resistivity n^- region doped to about 2×10^{11} cm^{-3} below the bottom of the blanket p diffusion. The two n^+ diffusions cannot intersect each other laterally at doping levels higher than 10^{12} cm^{-3}, which would be the case if the depth of the blanket p diffusion were reduced. In that case the base resistivity of the SCL transistor would be too low and Eq. (1) would no longer be satisfied. Thus the depths of both the n^+ and the p diffusion and the separation between the two n^+ diffusions have to be adjusted accordingly. The above requirement is also true for the pnp transistor shown in Fig. 2.

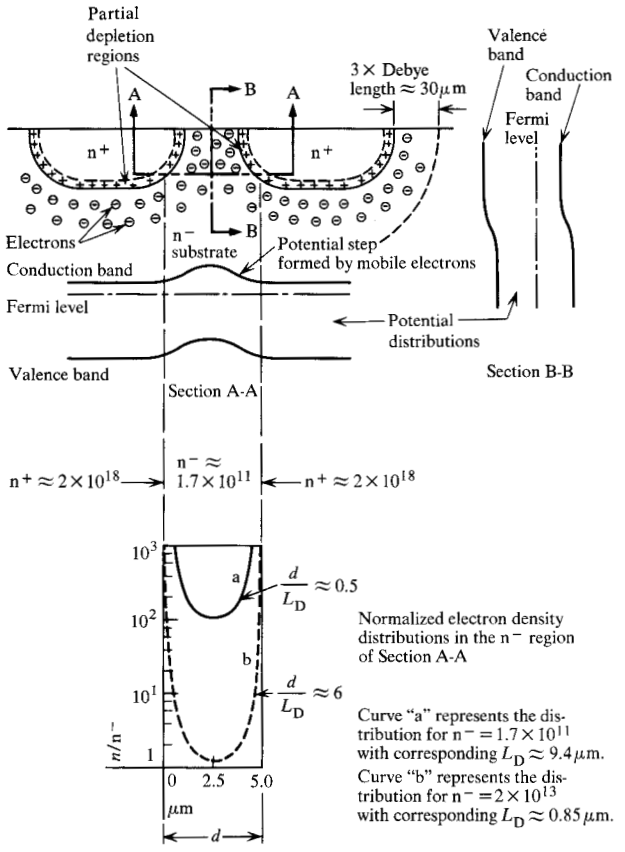


Figure 3 $n^+n^-n^+$ SCL diode; zero-current case.

The substrate resistivity for the structures shown in Figs. 1 and 2 must be n type. The reason for this will be explained later. Of course, if the diffusions in Figs. 1 and 2 are changed to the opposite type, a p type substrate must be used.

Qualitative theory of SCL transistor operation

In this section the theory of the SCL transistor is described qualitatively to establish the basis for an approximation; namely, that the current is limited only by mobile space-charge with an infinite source at the potential minimum. The quantitative theory of the SCL transistor, described in the next section, will be based on this approximation.

Figure 3 shows the nn^-n structure of Fig. 1 without its upper bipolar transistor. Electrons diffuse from the n^+ regions into the n^- substrate to form a negative mobile space-charge region, and a positively charged, partly depleted region forms on the n^+ side. The result is a high-low junction between the n^+ and n^- regions. The depth of the diffused electron cloud in the n^- substrate is about $3L_D$ [14], where L_D is the Debye length. For 30 kΩ-cm n type silicon, $L_D \approx 9.4\mu m$ while the separation between the two n^+ diffusions is about $5\mu m$ for the SCL transistor. For the above reason the electron clouds diffused from the two separated n^+ regions will join each other as shown in Fig. 3.

The horizontal potential distributions between the two n^+ diffusions are shown in Section A-A of Fig. 3. One can see that the diffused electrons form a potential minimum in the middle between the two n^+ diffusions. Application of the slightest bias between the two n^+ diffusions would result in a space-charge-limited current because the potential minimum is formed by mobile electrons. The vertical potential distributions between the n^+ diffused regions are shown in Section B-B of Fig. 3.

The free electron density distributions in the n^- region of Section A-A for two specific n^- doping levels are also shown in Fig. 3. These distribution curves were calculated from Fig. A7 in the Appendix. The free electron density n is normalized in terms of the doping level of the n^- region. Curve "a" represents the distributions for the SCL transistor with its actual doping level $n^- = 1.7 \times 10^{11}$ and $L_D \approx 9.4\mu m$. Curve "b" represents the distribution if the doping level were increased to $n^- = 2 \times 10^{13}$ with a corresponding $L_D \approx 0.85\mu m$. For both curves the doping level on the n^+ side is about 2×10^{18} and the separation between n^+ regions is $d = 5\mu m$. One can see that the free electron density at the potential minimum in the n^- region is about two orders of magnitude higher than the compensated electron density corresponding to its doping level if the ratio $d/L_D = 0.5$. This assures space-charge limitation even at the lowest current level. If the d/L_D ratio had been increased to six or larger, the electron density would relax to its thermal equilibrium value at the potential minimum establishing quasi-charge neutrality there. For this reason there would be no space-charge-limitation at low current levels and the electrons would propagate by diffusion. At higher current level some partial space-charge can arise [13] if the dielectric relaxation time is sufficiently long compared to the transit time across the quasi-neutral region. At this stage however, the upper transistor of Fig. 1 turns on and practically no space-charge-limited current would be observed.

If space-charge-limited current is to be observed in the SCL transistor, the Debye length in its base has to be at least equal to or, preferably larger than, the base width. This requirement is related [14] to that of Eq. (1). It is, however, somewhat more specific and stringent than the dielectric relaxation time requirement.

Figure 4(a) indicates the change that occurs when relatively shallow p regions are diffused between and outside the n^+ regions of Fig. 3. The resulting structure is identical to that of Fig. 1. The potential distributions of Fig. 4(a) represent the zero-current case. The p regions in Fig. 4(a) will deplete the n^- substrate to a depth of $65\mu m$ at zero bias. The depletion regions, however, do

not join each other because of the screening effect of the deeper n^+ diffusion. The electron clouds diffused from the emitter and collector are separated in the substrate by a positive immobile space-charge region. It should be noted that some hole diffusion takes place from the p region into the depleted n^- region [14] even at zero bias. This hole diffusion however does not change the result of the qualitative analysis. The change in the vertical potential distribution between n^+ regions is shown in Section B-B. One can see that the p region pulls both the conduction and valence bands in the n^- substrate close to the p level in the vicinity of the n^+ regions and thus separates the diffused electron clouds from each other. The horizontal potential distribution between the n^+ regions will change accordingly, as shown in Section A-A. The potential step previously formed by mobile electrons is replaced by a higher potential step formed by immobile negative ions in the p region. In other words, the conduction and valence bands of the p region extend deep into the n^- substrate separating the electron clouds from each other with a firm potential step. The increase of the potential step is V_S, which gives rise to a threshold as shown in Fig. 4(a). V_S is about equal to the built-in voltage at the p-n^- junction. Thus, if a positive voltage is applied to the collector in Fig. 4(a), with emitter and base at ground level, current will flow only if the collector voltage reaches a certain level (about 8 volts) that lowers the potential step by V_S in Section A-A so that electrons can be injected into the depleted region. The effect of collector voltage on the potential step is relatively small (about 5%) because of the electrostatic shielding effect of the depleted region. The potential distribution in the upper npn transistor (Section C-C) is also shown in Fig. 4(a). The potential step, between emitter and base, of the upper transistor is larger than that of the lower SCL transistor.

Figure 4(b) shows how the potential distributions change if a small forward bias (about 0.4V) is applied to the base of the upper transistor and the collector-base junction is reverse biased. Since the forward bias is about equal to the built in voltage of the horizontal p-n^- junction, the deep depletion region below the p base region contracts and disappears. Thereby the potential step separating the electron clouds is also removed. The electron cloud surrounding the emitter experiences an electric field and will move toward the collector. The space-charge of the moving electron cloud forms a potential minimum "virtual emitter" in the base of the SCL transistor as shown in Section A-A of Fig. 4(b). This potential minimum represents a potential step for electrons and thus controls the current in the SCL transistor. The upper npn transistor is not turned on yet because the potential step at its emitter junction is too high for electrons as shown in Section C-C of Fig. 4(b). The

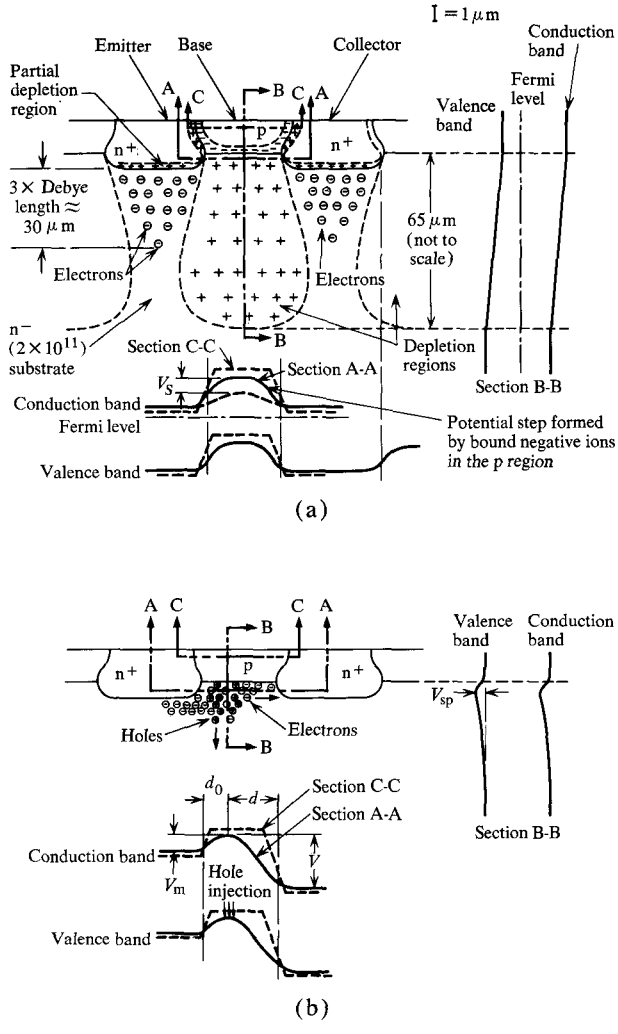


Figure 4 SCL transistor on n^- substrate. (a) Zero-current case; (b) current-carrying case.

base of the upper transistor, through its extended depletion region, turns on and controls the current in the SCL transistor like the grid in a vacuum triode.

However, the control becomes more complicated because hole injection takes place in the transverse direction from the forward biased p base to the n^- substrate as shown in Fig. 4(b). The hole injection is mostly at the potential minimum because the potential difference between valence bands of Sections A-A and C-C of Fig. 4(b) is at a minimum. The injected holes partly neutralize the negative space-charge of electrons in the potential minimum and thus increase the collector current. The hole injection is also space-charge-limited with a potential maximum formation shown in Section B-B of Fig. 4(b). The potential maximum coincides with the potential minimum and forms a saddle point on both the conduction and valence band surfaces [15]. The saddle-point potential V_{sp} controls both the electron and hole

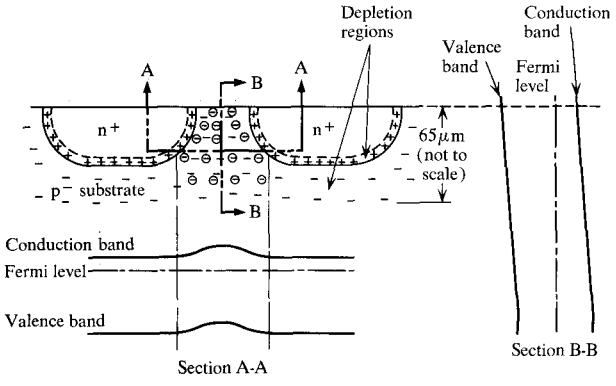


Figure 5 $n^+p^-n^+$ SCL diode; zero-current case.

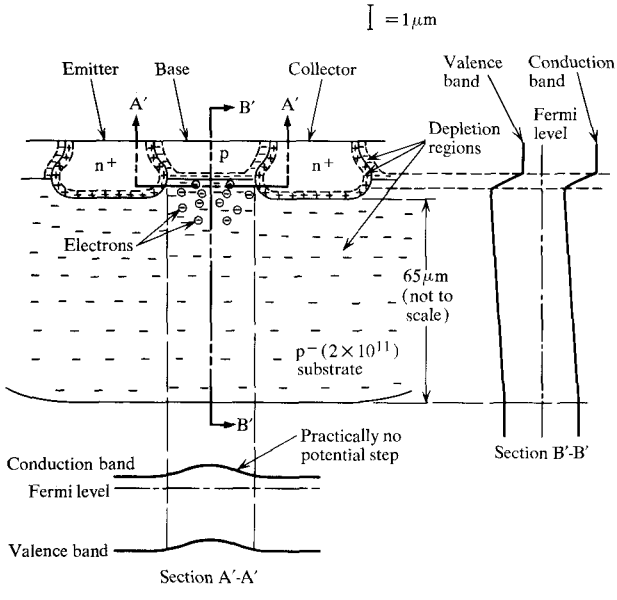


Figure 6 SCL transistor on p^- substrate; zero-current case.

currents flowing in transverse directions. Its effect on electron current is, however, opposite to that on hole current. If the saddle-point potential is made more positive by increasing the collector voltage, the electron current will increase while the hole current decreases. The potential maximum in Section B-B of Fig. 4(b) is formed by the negative space-charge of the transverse electron current. The potential step between the p and n^- regions is equal to the built-in voltage for the zero current case as shown in Section B-B of Fig. 4(a). This potential step increases with V_{sp} for the current-carrying case as can be seen in Section B-B of Fig. 4(b).

The recombination rate in the high-resistivity n^- region is very low because high-quality silicon crystal, practically free of trapping centers, was used. Thus the current gain of the SCL transistor is very high as long as the upper transistor is not turned on.

The electron injection actually takes place at the potential minimum because the electron supply is very large there. The injected electrons travel from the potential minimum to the collector by a drift mechanism. From Schockley's approximation [2], the transit time across the base region is determined by $\tau = 4d^2/3\mu_{ni}V$, where d is the distance from the potential minimum to the collector and V is the sum of the applied collector voltage and the depth of the potential minimum V_m as shown in Fig. 4(b). For zero current the potential minimum is at the middle of the base ($d_0 \approx d$) and V_m is about 0.5V (half the band gap). Thus V cannot be less than $\approx$0.5V even with zero collector voltage. μ_{ni} is the intrisic bulk mobility for electrons and is equal to 1450 cm^2/V-sec. The transit time τ for the upper npn transistor is approximately $(d_0 + d)^2/\mu_n(kT/e)$, where $\mu_n \approx$ 350 cm^2/V-sec. Here the thermal voltage kT/e (0.026V) takes the role of the drift voltage V. One can see that the transit time of the SCL transistor is at least two orders of magnitude smaller than that of the upper npn transistor.

The requirement for establishing a predominantly drift current across the base of the SCL transistor is that the uncompensated electron density be very high at the potential minimum. This, in turn, requires that the extrinsic Debye length in the base be about equal to the base width. Reducing the Debye length by decreasing the subtrate resistivity would also reduce the free electron density at the potential minimum. Most of the electrons would be injected from the emitter instead of the potential minimum and travel through the potential minimum by a diffusion mechanism. The resulting transit time would be considerably longer.

It is obvious from Fig. 4 that a pnp transistor with the same structure can also be fabricated. In this case the base will be the emitter, the collector the base, and the outside p region on the right, the collector. Since the depleted regions in the n^- substrate do not join each other, the emitter and the collector of the pnp transistor will also be separated by a firm potential step in the valence band as shown in Section A-A of Fig. 4(a). Negative bias applied to the base (n^+ region) will lower this potential step and thus control the hole flow. In addition, more electrons will be injected into the n^- base of the pnp SCL transistor. These electrons partly neutralize the space-charge of holes, thus also controlling the hole flow in a way similar to that by which the holes control the electron flow in the npn SCL transistor. This means of control will predominate in the pnp transistor since electrons are already injected at zero forward bias.

The reason the above theory does not hold for a p^- substrate is made evident in Figs. 5 and 6. Figure 5 shows two separated n^+ diffusions in a high-resistivity (30k ohm-cm) p^- substrate. The n^+ regions will deplete

the p^- substrate to a depth of 65μm at zero bias. The depletion regions join each other as shown in Fig. 5. In addition, the p^- substrate between the n^+ regions is flooded with electrons. The vertical potential distribution between the n^+ regions is shown in Section B-B. As can be seen, the conduction and the valence bands in the depleted p^- region are pulled down nearly to the n^+ level in the vicinity of the n^+ regions. Accordingly the horizontal potential distribution between the n^+ regions will be approximately constant as shown in Section A-A. A slight potential step is formed between the n^+ regions. Application of bias between the two n^+ regions will result in a space-charge-limited current flow.

Figure 6 indicates the change that occurs when relatively shallower p regions are diffused between and outside the n^+ regions. The change in the vertical potential distribution between n^+ regions is shown in Section B′-B′. One can see that both conduction and valence bands are pulled up to the p level in the p region. The potentials of both bands, however, drop rapidly nearly to the n^+ level in the p^- substrate which still remains depleted by the n^+ regions. As a result the horizontal potential distribution between n^+ regions, shown in Section A′-A′, remains approximately unchanged. Practically no potential step is formed. It is obvious that even with reverse (negative) bias on the base the electron flow cannot be cut off if a small positive voltage is applied to the collector. The potentials in the depleted p^- region are held firmly by the n^+ regions, thus the controlling action of the base is very poor. Experimental evidence supports the above theory.

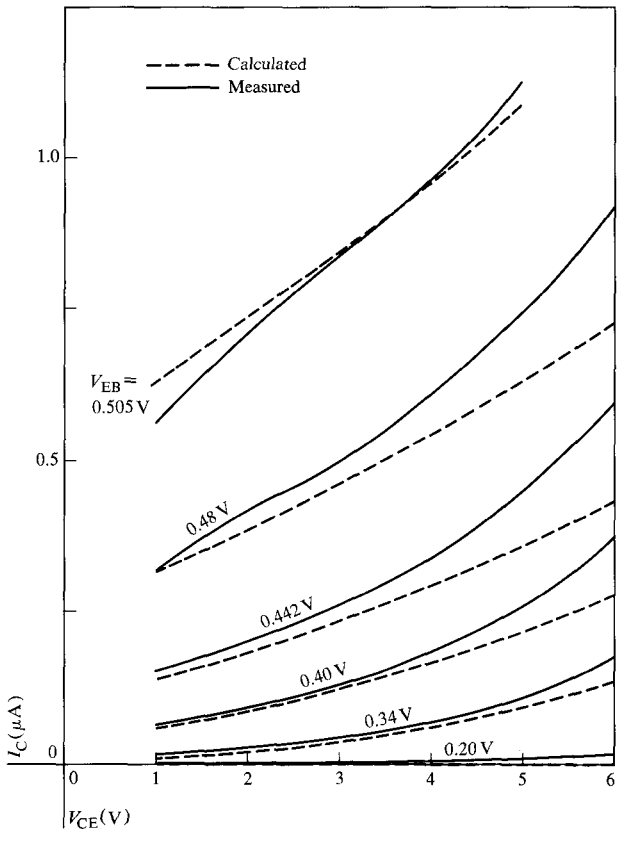


Figure 7 Comparison of measured and calculated I_C-V_C characteristics.

• *Quantitative theory of SCL transistor operation*

Collector current The complete mathematical model based on space-charge-limitation approximation is derived in the Appendix. According to this model the collector current density is

$$J_c = 3.36 \times 10^{-7} \times \frac{(V_S + V_{BE} + DV_{CE}) \exp (V_{sp} + V_{BE})/0.026}{d(\frac{1}{2} + D)} + 1.2 \times 10^{-8} \frac{(V_S + V_{BE} + DV_{CE})^2}{d^3(1 + 2.83D)^2}, \quad (2)$$

where V_S is the threshold potential between emitter and collector in the n^- region as shown in Fig. 4(a), Section A-A; V_{sp} is the threshold potential at the pn^- junction as shown in Fig. A1 (Appendix); V_{BE} and V_{CE} are the voltages applied to the base and the collector, respectively; D is the penetration factor; and d is the separation between emitter and collector.

The transconductance is given by

$$G_m = \frac{\partial J_C}{\partial V_{BE}} = \frac{3.36 \times 10^{-7} \exp [(V_{sp} + V_{BE})/0.026]}{0.026d(\frac{1}{2} + D)} \times (0.026 + V_S + V_{BE} + DV_{CE}) + 2.4 \times 10^{-8} \frac{V_S + V_{BE} + DV_{CE}}{d^3(1 + 2.83D)^2} \quad (3)$$

The second term in Eq. (2) represents the pure space-charge-limited current which varies with the square of the applied voltage according to the Mott-Gurney law [1]. The first term in Eq. (2) is due to the hole injection into the n^- base region which partly neutralizes the space charge of electrons. This term gives a linear variation of collector current as a function of collector voltage. Since this exponential term is dominant, the SCL transistor has an exponential turn-on characteristic like that of conventional transistors. In contrast, FETs and vacuum triodes have slow 2- and 3/2-power turn-on

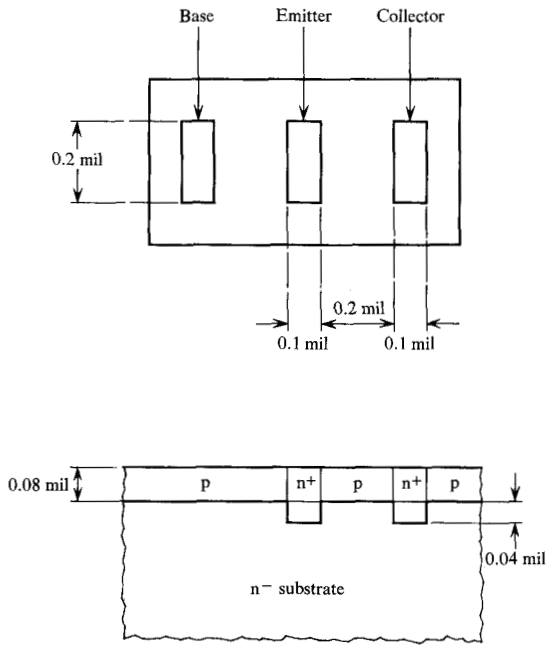


Figure 8 Dimensions of an npn SCL transistor.

characteristics, respectively. The exponential turn-on characteristic makes the SCL transistor very attractive for switching applications.

Figure 7 shows the calculated and measured I_C-V_{CE} characteristic of an SCL npn transistor with constant voltages as a parameter. The geometry of the SCL transistor is shown in Fig. 8. The actual emitter-to-collector distance is 4.4μm, determined with staining. The penetration factor D was determined by measuring the voltage amplification factor, μ, on the device. D approaches $1/\mu$ near cut-off. V_S and V_{sp} cannot be calculated or measured directly. Their values were adjusted to get the best fit with experimental results ($V_S = -0.33$V and $V_{sp} = -0.241$V).

As can be seen from Fig. 7, the agreement between calculated and measured characteristics is good. The deviation of the measured collector current from the calculated current is caused by collector multiplication since the collector-base breakdown is about 7 volts. In Figs. 9 and 10, the first and second terms of Eq. (2) are plotted separately to show their relative contributions to the collector current. One can see from Fig. 10 that the pure space-charge-limited current is dominant at low current levels (low forward bias). At higher current levels (high forward bias), however, the current term caused by hole injection prevails as shown in Fig. 9. The effect of temperature on the collector current is discussed in the Appendix. According to the mathematical model the temperature dependence is expected to be less than that of bipolar transistors.

Base current The exact mathematical model for base current is also described in the Appendix. Since the calculation is quite complicated, we do not carry it out here. We want only to compare the qualitative conclusions, drawn in the Appendix, with experimental results.

According to the Appendix the current gain increases rapidly with increasing collector voltage, keeping the collector current constant. Figure 11 shows the measured I_C-V_{CE} characteristic of the same npn transistor. Here, in addition to the V_{EB} constant curves, the I_B constant curves are also plotted. It can be seen that the current gain β at high collector voltages (6V) and 0.5μA

Figure 9 Calculated I_C-V_C characteristic due to hole injection.

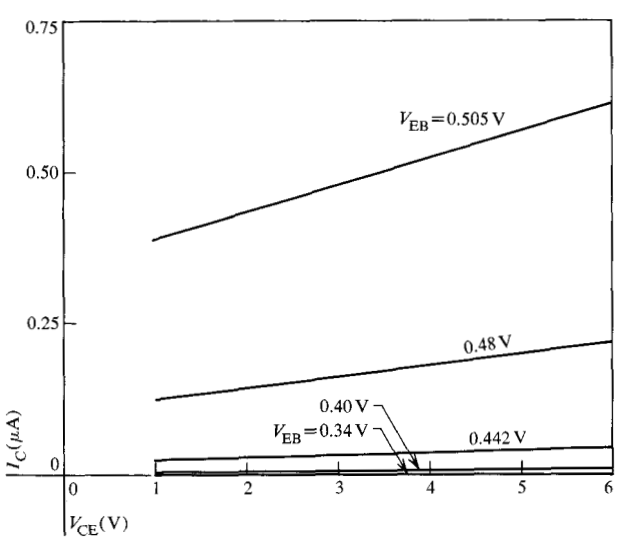
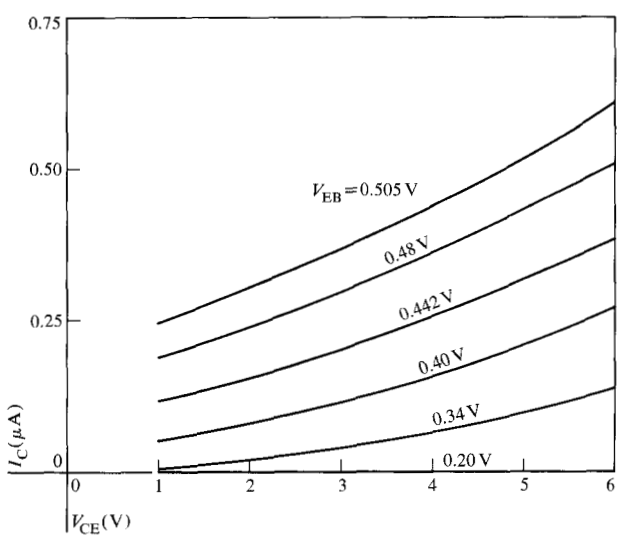


Figure 10 Calculated I_C-V_C characteristic due to pure SCL current.



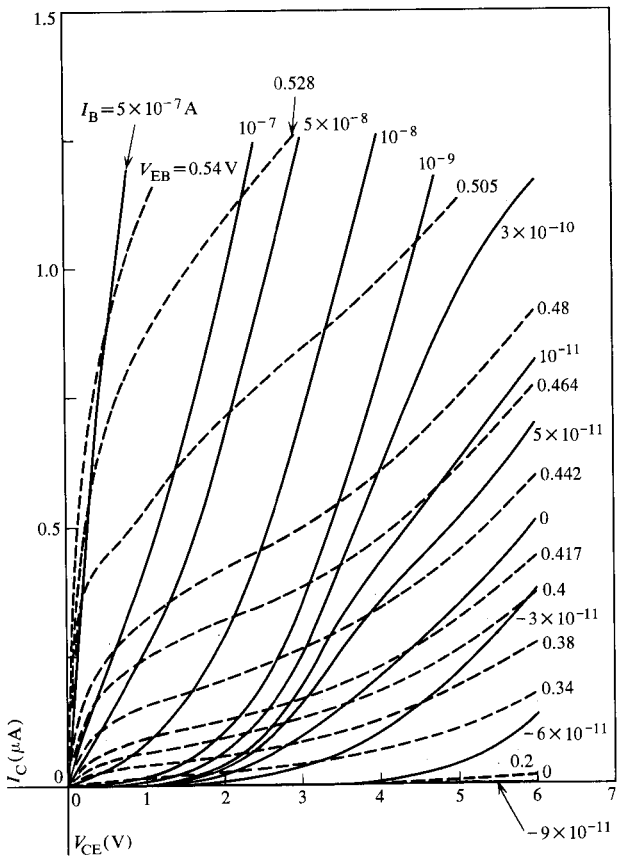


Figure 11 I_C-V_C characteristic of an npn SCL transistor. Dashed lines: V_{EB} in volts; solid lines: I_B in amps.

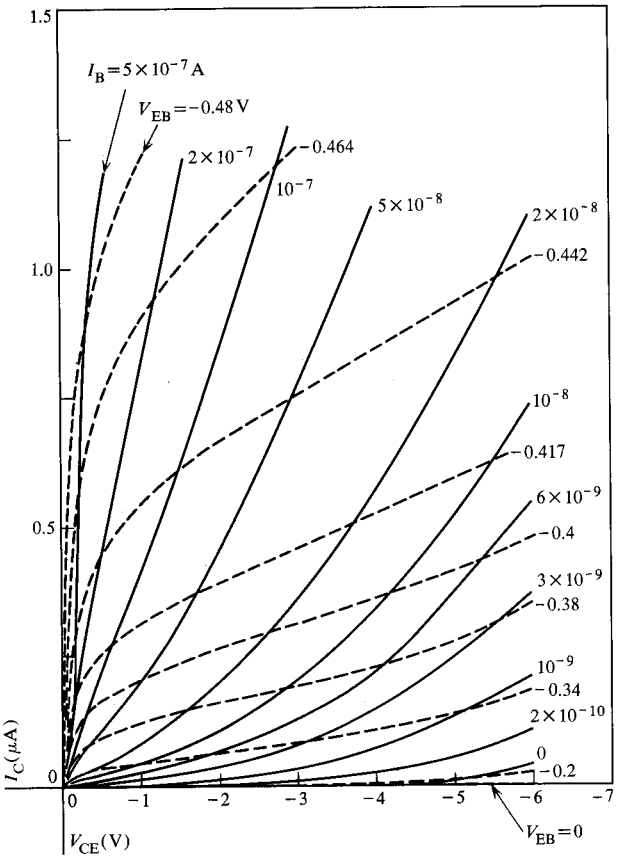
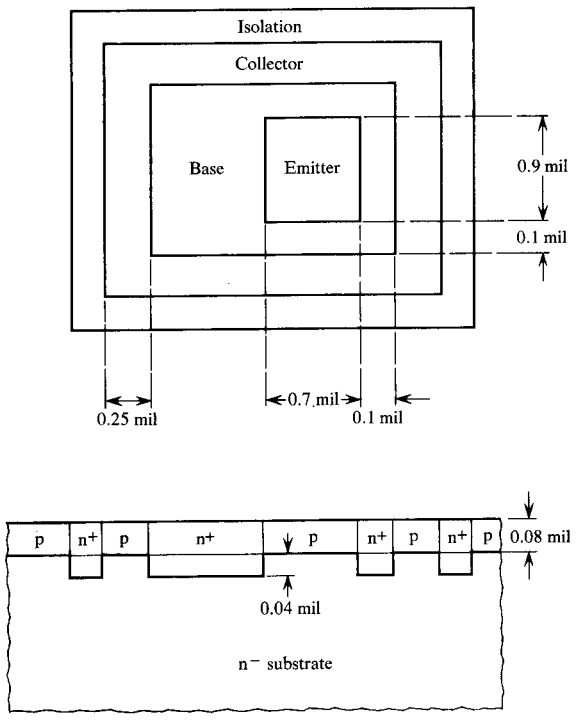


Figure 12 I_C-V_C characteristic of a pnp SCL transistor. Dashed lines: V_{EB} in volts; solid lines: I_B in amps

collector current is about 4000. The base current changes sign below 0.5μA collector current. This is due to the collector-to-base leakage current of the upper lateral transistor (see Fig. 8) which is multiplied by the high β. It can also be seen that β drops down rapidly at lower collector voltages. One can see that this is exactly the expected current gain behavior. Current gain as high as 70,000 was measured on another SCL transistor at $V_{CE} = 6$V and $I_C = 1\mu$A. The collector current dropped below 1nA if the forward base bias was reduced to zero, which shows the excellent cut-off behavior of the SCL transistor.

The other important feature, derived from the mathematical model, is the switching mechanism of the base current. No charge storage takes place in saturation. During the "on" period the base current propagates by diffusion. During switching, however, the base current carriers are injected and removed by drift to and from the base, respectively. This increases the switching speed of the SCL transistor considerably. For comparison, Fig. 12 shows the I_C-V_{CE} characteristics of a closely matched SCL pnp transistor that was processed with the same diffusion cycles as the npn transistor. The geometry of the pnp transistor is shown in Fig. 13.

Figure 13 Dimensions of a pnp SCL transistor.



Conclusions

A theoretical model for both npn and pnp SCL transistors on high resistivity n^- silicon substrates has been described. According to this model the space-charge-limited current in the SCL transistor is controlled by the base of a parallel connected lateral transistor in two ways. First, the base of the parallel transistor controls the potential step in the high-resistivity base between the emitter and the collector of the SCL transistor. Second, the base of the parallel transistor injects carriers in the direction transverse to the SCL current flow. These carriers are of opposite type to those that carry the current and thus partly neutralize the space charge in the current. The theoretically calculated I_C-V_{CE} characteristics agree well with the measured ones. The space-charge-neutralization effect gives the SCL transistor an exponential turn-on characteristic (I_C-V_{BE}). The carriers propagate across the high-resistivity base region of the SCL transistor predominantly by drift. The resulting base transit time is about two orders of magnitude faster than that of a bipolar transistor with equal base width. No charge storage takes place in saturation because both collector and base currents are space-charge-limited. The above features and the low device capacitances make the SCL transistor very attractive for low-voltage, fast-switching applications. Current gains as high as 70,000 were measured at low forward bias. These high gains occur because surface recombination is eliminated and the recombination center density is very low in the high resistivity substrate. The current gain, however, becomes lower at higher forward bias because the parallel lateral transistor turns on. If the parallel transistor action is reduced or eliminated, the high current gain can be extended to high current levels. It was also demonstrated that complementary pairs of SCL transistors can be fabricated with three masking steps.

Appendix

• *Collector current calculation*

To calculate the space-charge-limited current flow in the SCL transistor, we start out with the energy band configuration of the $n^+n^-n^+$; structure shown in Fig. A1. The base of the upper npn transistor (not shown) is assumed to be forward biased. This forward bias is equal to the built-in voltage of the horizontal p-n^- junction as shown in Section B-B of Fig. 4(b). Curves "a" represent the potential distributions in the conduction and valence bands for zero collector voltage. One can see that a flat potential minimum is formed in the middle of the n^- region in both the conduction and valence bands. These flat portions of curves "a" are at the same potential as the conduction and valence bands of the p base of the upper transistor. The depth of the potential minimum V_{m0} is about equal to the half band gap. If positive bias is applied to the collector, current starts to flow and the potential distributions change as shown in curves "b." It can be seen that the potential minimum moved close to the emitter and its depth was reduced to V_m in a way similar to that in a vacuum diode. The reduction of the potential minimum is indicated as V_{sp}. The detailed analysis of potential minimum formation for space-charge-limited current flow in intrinsic semiconductors is given by G. T. Wright [7]. His results show that once the current is established, the variation of the potential minimum depth is slow. It varies logarithmically with applied voltages and current. The effect of potential minimum formation on space-charge-limited current can be neglected for high current densities.

As a first-order approximation, the effect of potential minimum formation will be neglected except for the hole injection from the p region into the n^- base region. The V_{sp} potential step in the valence band of the n^- region forms a threshold for the holes. By applying forward bias to the p region, for zero current case, holes would be injected into the valence band, shown as curve "a," of the n^- region. For the current-carrying case, however, the holes have to be injected into the modified valence band of the n^- region, shown as curve "b." The hole injection will start at the potential minimum when the forward bias is sufficiently high to reduce the V_{sp} threshold potential to zero. As a first-order approximation, we assume that the V_{sp} threshold potential is constant.

This hole injection in the SCL transistor comes from a p region above the n^- region as shown in Fig. 4(b). The mechanism of this hole injection will be incorporated into the theory later. If forward bias is applied to the diode, as shown by curves "b" in Fig. A1, the current is carried only by electrons since holes experience a repelling field from both n^+ regions. Thus, the current density is

$$J = J_n = e\mu_n nE, \tag{A1}$$

where e is the charge of an electron, μ_n is the electron mobility, n is the electron density, and E is the electric field.

In Eq. (A1) the electron diffusion is neglected because its effect is small. From Poisson's equation we can derive the electric field in the n^- region by solving

$$\frac{dE}{dx} = -\frac{e(n-p)}{\epsilon}, \tag{A2}$$

where p is the hole density and ϵ is the dielectric constant of silicon.

As can be seen the hole density influences the electric field. We assume that the ratio of electron to hole density is the same [6] at every point in the n^- region:

$p/n = \gamma =$ constant as a function of x. (A3)

This assumption will be justified later.

In the above equations it was also assumed that carrier generation and recombination is negligible. This is justified because surface effects are eliminated by the blanket p diffusion and the doping level is very low (2×10^{11}) in the n^- region. Substitution of Eqs. (A1) and (A3) into Eq. (A2) gives

$$\frac{dE}{dx} = -\frac{J(1-\gamma)}{\mu_n \epsilon E}. \tag{A4}$$

Integrating Eq. (A4), we obtain

$$\tfrac{1}{2}\mu_n \epsilon E^2 = -J(1-\gamma)x + \text{constant}. \tag{A5}$$

The boundary condition for space-charge-limited current requires that $E = 0$ at $x = 0$. Hence the constant is zero and the electric field in the n^- region is

$$E = -\left[-\frac{2Jx(1-\gamma)}{\epsilon\mu_n}\right]^{\frac{1}{2}}. \tag{A6}$$

Substituting Eq. (A6) into Eq. (A1) we get the electron density distribution in the n^- region:

$$n = \frac{1}{e}\left[-\frac{\epsilon J}{2x(1-\gamma)\mu_n}\right]^{\frac{1}{2}}. \tag{A7}$$

To get the electrostatic potential V, we substitute $E = dV/dx$ into Eq. (A5) and integrate:

$$\sqrt{\tfrac{1}{2}\mu_n \epsilon}\, V = \tfrac{2}{3}\sqrt{-J(1-\gamma)}\, x^{\frac{3}{2}} + \text{constant}. \tag{A8}$$

We set the potential $V = 0$ at $x = 0$. Hence the constant is zero, so that

$$V = \tfrac{2}{3}\left[-\frac{2J(1-\gamma)}{\epsilon\mu_n}\right]^{\frac{1}{2}} d^{\frac{3}{2}} \tag{A9}$$

and the current density is

$$-J = \tfrac{9}{8}\frac{\epsilon\mu_n}{(1-\gamma)}\frac{V^2}{d^3} = P\frac{V^2}{d^3}, \tag{A10}$$

where d is the separation between n^+ regions, V is the applied voltage between n^+ regions, and $P = (9/8)\epsilon\mu_n/(1-\gamma)$.

The value of γ remains to be determined. By substituting Eqs. (A3) and (A9) into Eq. (A7),

$$\gamma = \frac{4ped^2}{3\epsilon V + 4ped^2}, \tag{A11}$$

where p is the injected hole density to be determined later.

Substituting Eq. (A11) into (A10) gives the current density

$$-J = -J_1 - J_2 = P_1\frac{V}{d} + P_2\frac{V^2}{d^3}, \tag{A12}$$

where

$$P_1 = \frac{3ep\mu_n}{2} \text{ and } P_2 = \frac{9\epsilon\mu_n}{8}.$$

The second term in Eq. (A12) is the well known Mott-Gurney law. The first term shows the effect of injected holes. These injected holes partly neutralize the space-charge of the electrons.

Equation (A12) describes the space-charge-limited current in a $n^+n^-n^+$ diode where a hole density of p is injected in the n^- region. In an SCL transistor this hole injection takes place from a shallow p region, called the base, between the two n^+ regions as shown in Fig. 4(b). It is evident that the injected hole density, p, will depend on the applied base voltage only. The potential, V, in Eq. (A12), however, will depend upon both applied base and collector voltages in a manner similar to that in a vacuum triode, where the potential in the grid plane (effective potential) depends upon both grid and plate voltages. Because of this similarity, the analysis used for vacuum triodes, will be developed for SCL transistors. By analogy with the vacuum triode we can rewrite Eq. (A12) as

$$-J = -J_1 - J_2 = P_1K_1(V_S + V_{BE} + DV_{CE}) + P_2K_2(V_S + V_{BE} + DV_{CE})^2, \tag{A13}$$

where V_S is the height of the potential step between the two n^+ regions as shown in Fig. 4(a) (Section A-A); K_1 and K_2 are constants to be determined later; and V_{BE} and V_{CE} are the voltages applied to the base and collector, respectively.

D is the penetration factor [16] or "Durchgriff," which is the ratio of base voltage to collector voltage for a condition of cut-off (zero current). Since the potential step caused by the base is exactly in the middle of the emitter-to-collector distance (Fig. 4(a), Section A-A), the constants K_1 and K_2 can be determined [17] by giving the base the same potential that would exist in the middle of the n^- region, $x = d/2$. We determine K_2 from the second term of Eq. (A12), where

$$V_{CE} = \sqrt{\frac{-J_2}{P_2}}\, d^{\frac{3}{2}} \text{ and} \tag{A14}$$

$$V_S + V_{BE} = \sqrt{\frac{-J_2}{P_2}}\left(\frac{d}{2}\right)^{\frac{3}{2}}. \tag{A15}$$

Substitution into the second term of Eq. (A13) and manipulation yields

$$K_2 = \left[\left(\frac{d}{2}\right)^3 (1 + 2.83D)^2\right]^{-1} \tag{A16}$$

Similarly, from the first term of Eq. (A12),

$$K_1 = [d(\tfrac{1}{2} + D)]^{-1}. \tag{A17}$$

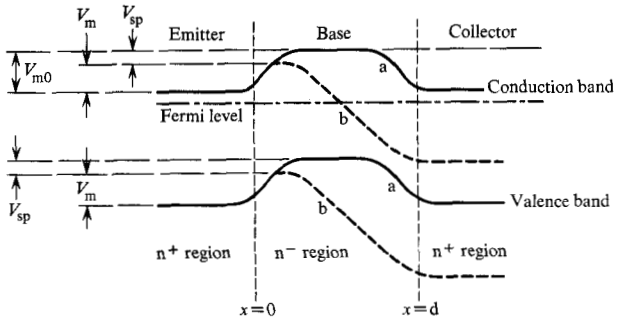


Figure A1 Energy band configuration for the $n^+n^-n^+$ structure. Curves "a" represent the zero collector bias case. Curves "b" represent the positive collector bias case.

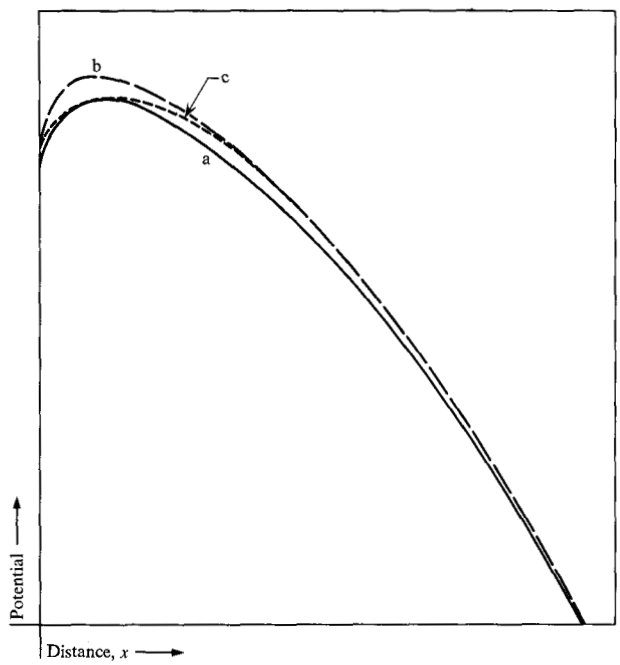


Figure A2 Potential distribution in the n^- region. Curves "a" and "b" represent the γ = constant and $\gamma = 0$ cases, respectively. Curve "c" represents the actual case.

The hole density, p, injected into the n^- region can be calculated from

$$p = p_n \exp\,[-e(V_{sp} + V_{BE})/kT], \qquad \text{(A18)}$$

where p_n is the hole density in the n^- region, V_{sp} is the threshold potential shown in Fig. A1; and $-e/kT = 1/0.026$ at room temperature.

Substituting Eqs. (A16) – (A18) into (A13) gives

$$-J_C = \frac{3\mu_n e(V_S + V_{BE} + DV_{CE})p_n \exp\,[-e(V_{sp} + V_{BE})/kT]}{2d(\frac{1}{2} + D)} + \frac{9\epsilon\mu_n(V_S + V_{BE} + DV_{CE})^2}{d^3(1 + 2.83D)^2}. \qquad \text{(A19)}$$

The values of the physical constants in (A19) are

$\mu_n = 1450$ cm^2/V-sec,
$\epsilon = 1.065 \times 10^{-12}$ Farad/cm,
$e = 1.6 \times 10^{-19}$ Coulomb, and
$p_n = 1.12 \times 10^9$ for a 30kohm-cm n^- substrate. (A20)

Inserting these values into (A19) we obtain

$$-J_C = 3.36 \times 10^{-7} \times \frac{(V_S + V_{BE} + DV_{CE}) \exp\,[(V_{sp} + V_{BE})/0.026]}{d(\frac{1}{2} + D)} + 1.2 \times 10^{-8} \frac{(V_S + V_{BE} + DV_{CE})^2}{d^3(1 + 2.83D)^2}. \qquad \text{(A21)}$$

This is the final formula for an SCL npn transistor. The same equation can also be used for a pnp SCL transistor if p_n is replaced with n_n.

Let us now return to the assumption that the ratio of electron-to-hole density, γ, is constant at every point in the n^- region. First of all, the constant γ is $\ll 1$ because the electron density at the potential minimum is very high. Equation (A9) shows that the potential varies with distance in the n^- region as

$$V = c(1 - \gamma)^{1/2} x^{3/2} = c'x^{3/2} \qquad \text{(A22)}$$

if γ is constant. For the zero hole injection case ($\gamma = 0$), the variation remains the same except that c' increases slightly. In Fig. A2 the potential distributions are plotted for γ = constant (curve "a") and $\gamma = 0$ (curve "b") cases. Both curves to the right of the potential minimum were approximated by using Eq. (A22) which is justified for high currents. Hole injection takes place mostly around the potential minimum as was explained earlier. Thus γ is constant only in the immediate vicinity of the potential minimum and drops to zero rapidly in both directions. One can see that the actual potential distribution is between curves "a" and "b" as shown by curve "c." It is also evident that the error, which is the difference between curves "a" and "c," is small. Most important is that the depth of the potential minimum, which determines the current, is not affected by the approximation.

• *Base current calculation*

The two-dimensional potential distribution in the valence band of the base region with SCL current flow is shown in Fig. A3. The emitter-base is forward biased ($-V_S$) and the collector-base is reverse biased. Due to the SCL current a potential minimum is formed in the valence band close to the emitter in the n^- base. The potential at the minimum is higher than the potential of the n^- valence band as we know from Fig. A1. The increase is equal to V_{sp}. Since the forward bias $-V_S$ is larger than V_{sp}, holes will be injected from the p region into the

channel formed by the potential minimum in the n^- region. The potential distribution in the p base region is such that the resulting electric field funnels the holes into the channel. The injected holes propagate along the channel toward the n^- substrate by diffusion since the axial field in the channel is zero. The hole flow in the channel, however, experiences a transverse electric field that focuses the holes toward the bottom of the channel. This focusing action increases the neutralization of the negative space-charge at the potential minimum and thus makes the current control more effective. The potential distribution along the bottom of the channel is shown in Fig. A4. One can see that the injected holes always propagate only by diffusion during the nonswitching period. The axial electric field in the channel is zero which changes into a very slight accelerating field at the end of the channel. It can also be seen from Fig. A4 that when the forward bias V_{BE} is reduced to zero, the channel region becomes depleted and the SCL current is cut off. During switching, however, the injection and removal of holes from the n^- base is by drift because a large electric field develops along the channel. This feature increases the switching speed of the SCL transistor. According to Fig. A3, the base current is

$$J_B = \frac{eD_p p_i}{L_p} \exp \frac{e(V_{BE} - \frac{1}{2}V_g)}{kT} \int_0^{x=d} \exp \frac{eV(x,J_C)}{kT}\, dx, \tag{A23}$$

where D_p is the diffusion constant of holes, L_p is the diffusion length of holes, p_i is the intrinsic hole concentration, V_g is the band gap, $V(x, J_C)$ is the potential distribution in the x direction in the channel, d is the emitter-to-collector distance.

According to Wright [7] function $V(x, J_C)$ can be calculated as follows:

$$V(x,J_C) = \frac{kT}{e} \ln\left[\left(\frac{Z_0}{Z}\right)^{2/3} \frac{1}{B_0}\left[\frac{J_{-2/3}(Z_0) + J_{2/3}(Z_0)}{\beta I_{-1/3}(Z) + I_{1/3}(Z)}\right]^2\right] + V_0 \tag{A24}$$

or

$$V(x,J_C) = \frac{kT}{e} \ln\left[\left(\frac{Z_0}{Z}\right)^{2/3} \frac{1}{B_0}\left[\frac{J_{-2/3}(Z_0) + J_{2/3}(Z_0)}{-I_{-1/3}(Z) + J_{1/3}(Z)}\right]^2\right] + V_0 \tag{A25}$$

where V_0 is the potential difference between Fermi level and conduction band in the n^+ emitter, I_n and J_n are Bessel functions, J_C is the collector current,

$$Z = \frac{\sqrt{2}}{3j}\left(j\frac{x}{d} - 2.946j^{\frac{2}{3}}\right)^{\frac{3}{2}} + i\frac{\sqrt{2}}{3j}\left(-j\frac{x}{d} + 2.946j^{\frac{2}{3}}\right)^{\frac{3}{2}},$$

$$Z_0 = -\frac{\sqrt{2}}{3}(2.946)^{\frac{3}{2}} + i\frac{\sqrt{2}}{3}(2.946)^{\frac{3}{2}},$$

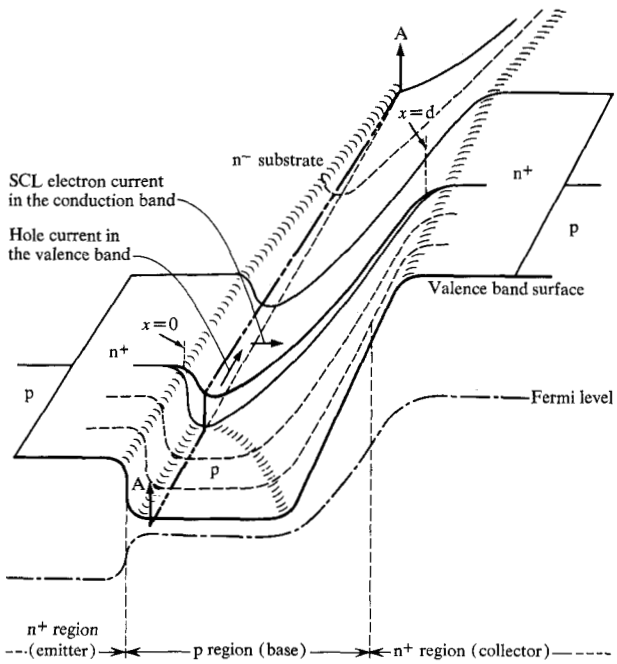


Figure A3 Two dimensional potential distribution in the valence band of the base region with SCL current flow.

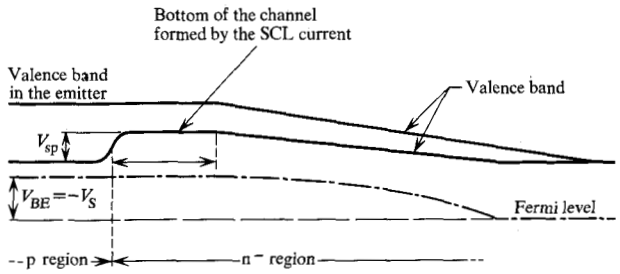


Figure A4 Potential distribution in Section A-A of Fig. A3.

$$j = -e^2 d^3 J_C / \epsilon \mu_n k^2 T^2,$$

$$B_0 = \left[\frac{-J_{2/3}(Z_0) + J_{-2/3}(Z_0)}{-J_{-1/3}(Z_0) + J_{1/3}(Z_0)}\right]^2,$$

$$-\beta = \frac{12Z_1 e^{Z_1} + \left(\cos\frac{\pi}{6}\right)e^{-Z_1}}{12Z_1 e^{Z_1} - \left(\cos\frac{\pi}{6}\right)e^{-Z_1}}, \text{ and}$$

$$Z_1 = \frac{\sqrt{2}}{3j}(j - 2.946j^{\frac{2}{3}})^{\frac{3}{2}} + i\frac{\sqrt{2}}{3j}(-j + 2.946j^{\frac{2}{3}})^{\frac{3}{2}}.$$

We may select the real part of Z if $[j(x/d) - 2.946j^{\frac{2}{3}}]$ is positive and the imaginary part if it is negative. In the first case Eq. (A24) and in the second case Eq. (A25) must be used. Eqs. (A24) and (A25) give a good approximation for the actual potential from $x = 0$ to about $x = d/2$ where most of the hole injection takes place. The approximation of the actual potential with the "effective potential" in Eq. (A13) is valid only in the

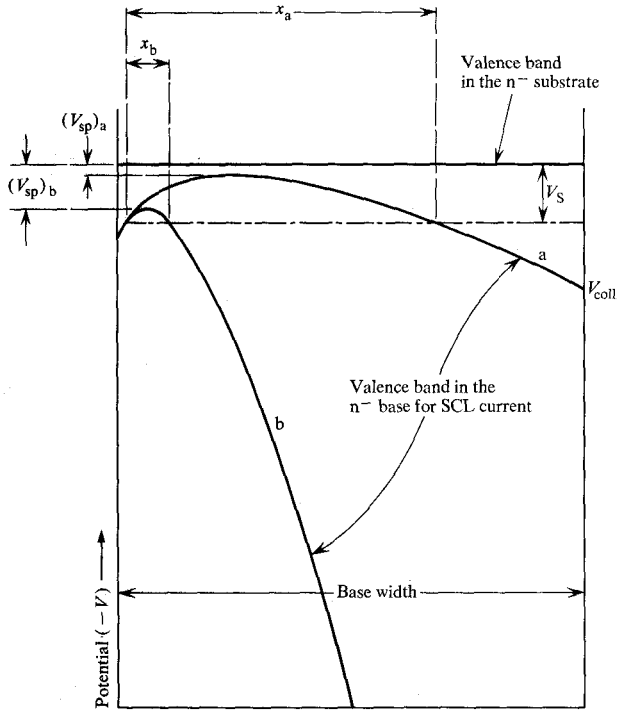


Figure A5 Variation of hole injection into the n⁻ base for small (curve "a") and large (curve "b") collector bias.

above range. Near the collector, $x \approx d$, the actual potential approaches the applied collector voltage.

Using the above results, we can calculate the base current and the corresponding collector current as follows: For the given base and collector bias we calculate the space-charge-limited component, J_C', of the collector current using the second term in Eq. (A19). Using this J_C' value, we calculate the base current from Eq. (A23). We now calculate V_{sp} using the minimum value of Eq. (A24) or (A25):

$$V_{sp} = V_{Fn} - [V(x, J_C)]_{min}, \qquad \text{(A26)}$$

where V_{Fn} is the Fermi level potential in the n⁻ region.

Substituting V_{sp} into Eq. (A19), we obtain the total collector current J_C which corresponds to the calculated base current J_B. We can correct Eq. (A19) for the error caused by the potential minimum by multiplying [7] $V_{eff} = (V_S + V_{BE} + DV_{CE})$ by

$$\left(1 + \frac{kT}{eV_{eff}} \ln C\right)$$

and d by

$$[1 - (3/j^{\frac{1}{3}})],$$

respectively, where $C = B_0/(2.4\pi Z_1^{\frac{1}{3}} Z^{\frac{2}{3}})$.

On this basis of the above model we can draw qualitative conclusions about the current gain behavior of the SCL transistor. Curve "a" in Fig. A5, calculated from Eq. (A24) or (A25), represents the potential distribution in the n⁻ base for small applied collector bias. The base is forward biased at $-V_S$ to compensate for the threshold potential V_S shown in Fig. 4(a). A large amount of hole injection will take place from the p region into the SCL n⁻ region because the threshold potential $(V_{sp})_a$ for holes is small and the channel width x_a is large. Nearly the whole base region is flooded with holes. Consequently, the SCL electron current and thereby the collector current increases. The corresponding base current is relatively very high and the current gain low. Curve "b" in Fig. A5 shows the potential distribution if the collector bias is increased. One can see immediately that the amount of hole injection is drastically decreased for two reasons. First, the $(V_{sp})_b$, due to the potential minimum, decreased in the SCL region. Second, the channel width x_a decreased to x_b. The resulting collector current will be somewhat larger than in the case of small collector voltage. The corresponding base current, however, is extremely small and the current gain very high. It has to be pointed out that even in the case of "b," when the collector bias is large, the collector current can be cut off completely if the forward base bias $-V_S$ is reduced to about zero. This increases the potential minimum for curve "b" in the negative direction by an amount V_S, which in turn cuts off the electron current.

One can also see from Fig. A5 and Eq. (A19) that the transverse hole injection into the high resistivity base region cannot be interpreted as conductivity modulation in the "usual" sense. First the holes are injected only into a restricted region of the base near the potential minimum. Thus neutralization of negative space-charge takes place only here, while the other regions of the base are unaffected. Second, the charge neutralization increases the value of V_{sp} in Eq. (A20) and thereby the potential step for hole injection. In other words, it acts like a negative feedback for hole injection. For the above reasons no charge storage occurs in the space-charge-limited transistor in saturation if the supply voltage is low enough that the upper lateral transistor cannot turn on. Conductivity modulation and thereby charge storage can take place only if the requirement for space-charge-limited current set forth in Eq. (1) is not satisfied. In this case the injected charge is neutralized through dielectric relaxation because the resistivity in the base region is low.

The temperature dependence of SCL transistors with transverse double injection is expected to be less than that of conventional bipolar transistors. The pure space-charge-limited current corresponding to the second term in Eq. (A19) has a negative temperature dependence because the electron mobility μ_n decreases with increasing temperature. This negative temperature dependence

was verified experimentally [6]. The second term in Eq. (A19) corresponding to the current caused by hole injection increases exponentially with increasing temperature in a manner similar to that of bipolar transistors. This increase is reduced, however, by the previously mentioned feed-back effect caused by the change of V_{sp}. It is also reduced somewhat by the decreasing mobility μ_n. Increasing temperature can also affect the current in Eq. (A20) indirectly by reducing the substrate resistivity to the extent that the requirement in Eq. (1) is no longer satisfied. This effect, however, can be neglected up to 80°C, and possibly higher. At 80°C the 30kΩ/cm substrate resistivity is reduced to about 10kΩ/cm. The dielectric relaxation time ϵ_ρ is reduced from 30 to 10 ns. The transit time is about 200 ps in the SCL transistors and Eq. (1) is still satisfied.

• *Asymmetric and high-low junctions*

The base region of the SCL transistor is bounded by three junctions as shown in Fig. A6. The left and right boundaries are n-n$^-$ high-low junctions. The upper boundary is a highly asymmetric p-n$^-$ junction.

We first investigate the asymmetric p-n$^-$ junction. The fundamental relationship between the electrostatic potential ψ and the charge in the space-charge layer can be written [18] as:

$$\frac{d^2\psi}{dx} = \frac{2en_i}{\epsilon}\left(\sinh\frac{e\psi}{kT} + \frac{N_a - N_d}{2n_i}\right), \qquad \text{(A27)}$$

where N_a and N_d are the acceptor and donor concentrations, respectively.

This nonlinear differential equation cannot be solved exactly in closed form, although various approximate solutions can be obtained. The depletion approximation widely used in transistor theory is one of such approximate solutions. This approximation requires that both sides of the junction be heavily doped ($N_d \gg n_i$ and $N_a \gg n_i$). Numerical solutions of Eq. (A27), for cases when one side of the junction is lightly doped, indicate that the electrical junction does not coincide with the metallurgical junction [18]. The reason for this is that far less than complete carrier depletion on the heavily doped side is able to provide the required amount of ionic charge. On the lightly doped side of the junction, the equilibrium concentration of carriers diffusing from the heavily doped side constitutes an appreciable fraction of the opposite-type space charge. Complete carrier depletion occurs somewhere beyond this carrier-enhanced region on the lightly doped side. Hence the depleted region does not span the metallurgical junction. This means that in Fig. 4(a) the representation of the p-n$^-$ junction with completely depleted regions is not exactly valid. Some hole diffusion takes place from the p region into the upper part of the depleted n$^-$ region. This hole diffusion, however, does not appreciably change the potential distribution.

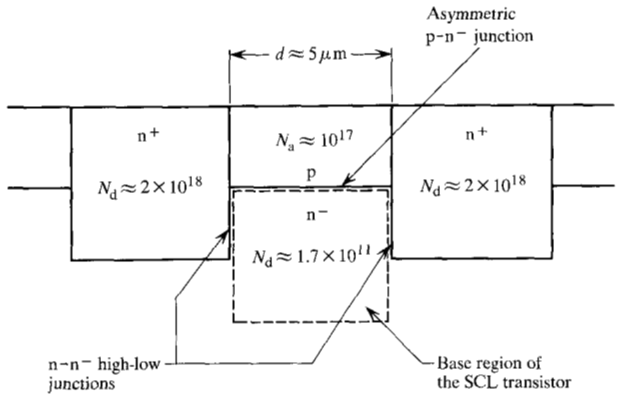


Figure A6 Boundary conditions for the base region of the SCL transistor.

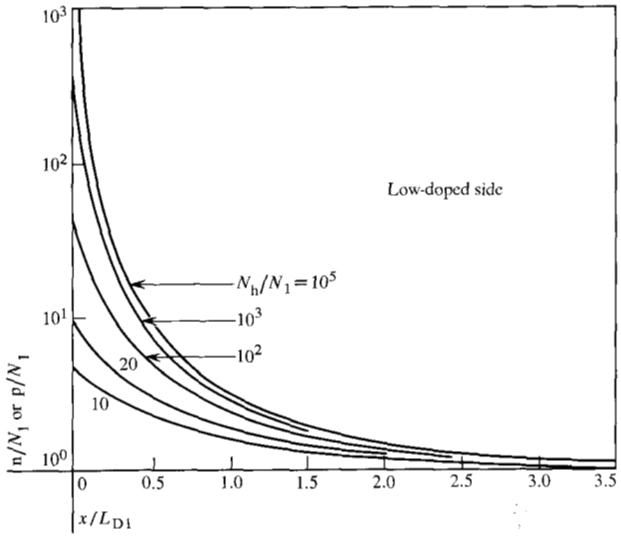


Figure A7 Calculated majority carrier distribution in the low-doped side of an abrupt high-low junction (silicon) according to Kennedy [19]. N_h is the doping level on the high-doped side; N_l is the doping level on the low-doped side; and L_{Dl} is the Debye length on the low-doped side.

Numerical solutions can also be obtained for the n-n$^-$ high-low junction from Eq. (A27). Kennedy [19] carried out a detailed numerical calculation for high-low junctions. The calculated majority carrier distribution in the low-doped side of a high-low junction is shown in Fig. A7. The majority carrier density (n or p) is normalized in terms of its thermal equilibrium value on the low-doped side (N_l). The distance is normalized in terms of the Debye length on the low-doped side.

$$L_D^2 = \epsilon kT/2e^2 n_i\{1 + [(N_d - N_a)/2n_i]^2\}^{\frac{1}{2}}, \qquad \text{(A28)}$$

where ϵ is the dielectric constant of silicon, e is the electronic charge, and n_i is the intrinsic electron concentration.

For intrinsic and extrinsic silicon the Debye lengths are

$$L_{Di} = \left(\frac{\epsilon kT}{2e^2 n_i}\right)^{\frac{1}{2}}, \tag{A29}$$

and

$$L_{De} = \left(\frac{\epsilon kT}{e^2 N_d}\right)^{\frac{1}{2}}, \tag{A30}$$

respectively.

The extrinsic Debye length can be rewritten as a function of dielectric relaxation time:

$$L_{De} = (D_e \epsilon p)^{\frac{1}{2}} = (D_e \tau)^{\frac{1}{2}}, \tag{A31}$$

where D_e is the diffusion constant for electrons and τ is the dielectric relaxation time.

The L_{De} for the base ($N_d \approx 1.7 \times 10^{11}$) of the SCL transistor is about 9.4μm. The corresponding τ is about 30ns. The emitter-to-collector separation $d \approx 5\mu$m. The doping level ratio N_h/N_l of the high-low junction in the SCL transistor is about 10^7, which is not shown in Fig. A7. It can be seen from the distribution of curves in Fig. A7 that the curve for a 10^7 doping ratio would be slightly above the curve for the 10^5 ratio.

Figure A7 indicates that carriers diffuse from the high-doped side of the junction to the low-doped side, leaving a partly depleted region on the high-doped side. One can see from the curves that when an initially large departure in majority carrier density from its thermal equilibrium value drops very fast within one Debye length from the high-low junction because it is in the highly nonlinear region of Eq. (A27). This rate of drop decreases and approaches an exponential decline several Debye lengths away from the junction where Eq. (A27) reduces to a quasi-linear differential equation. Within about $3L_D$ practically all the departure from charge neutrality vanishes.

In the base of the SCL transistor (see Fig. 3) electrons will diffuse from both high-low junctions to establish a potential minimum in the middle. This potential minimum is about $0.25L_D$ away from both high-low junctions. The majority carrier density at the potential minimum is more than twice that of the case when only one boundary condition exists since Eq. (A27) is nonlinear. We can make a qualitative conclusion from Fig. A7 that the normalized electron density, n/N_l, at the potential minimum is at least 10^2 for the zero current case. The conclusion forms the basis for calculating the currents in the SCL transistor. The theory of SCL currents in solids requires that the free carrier density at the potential minimum should be very high and the compensated carrier density should be negligible in comparison to the free carrier density.

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