Preface

Pin-in-hole technology (ceramic electronic-circuit-chip carriers with pins that are inserted into the plated through holes of epoxy–glass printed circuit cards) dominated IBM subsystem-assembly technology through the 1960s and 1970s. The 1980s saw the emergence of surface mount technology (SMT), peripherally leaded components mounted on the surface of printed circuit cards. SMT no longer required large plated through holes in the circuit cards to accommodate chip carriers with pins and thereby provided higher-efficiency packaging. In the 1990s the need for packages with higher and higher I/O counts is being driven by the increased circuit density of CMOS device technology. These I/O demands are driving peripherally leaded surface-mounted components to smaller pitches (lead-to-lead spacing), which in turn has decreased circuit card assembly yields through added process complexity, and has thus increased the overall device packaging cost.

An alternative to peripherally leaded components is a family of surface mount packages with high numbers of connections arranged in rectangular grids. The IBM Solder Ball Connect (SBC) technology, known as ball grid array in the microelectronics packaging industry, allows direct attachment of high-I/O-count chip carriers to industry-standard printed circuit cards, using standard surface mount assembly processes. The connections, both mechanical and electrical, between the chip carriers (modules) and cards are made by arrays of tiny balls of solder. This technology was fully developed through the efforts of an intersite Technology Products team led by the East Fishkill Packaging Laboratory, and including Endicott card-development and Endicott/Austin card-assembly-development organizations. SBC packaging, a major, visionary technology innovation, will satisfy high-I/O-device packaging requirements into the 21st century.

The May 1969 issue of the *IBM Journal of Research and Development* (Volume 13/Number 3) presented six technical papers related to controlled collapse chip connection (C-4) interconnection technology, which IBM has successfully practiced for over 25 years. SBC is a natural technology extension of the C-4 interconnections. In fact, much of the fundamental modeling, methodology, and understanding of solder fatigue established for C-4 interconnections has been found to be directly applicable to SBC. This *Journal* issue contains six technical papers related to SBC technology. Notable in these papers are the latest analytical tools, both hardware and software, utilized in the development of SBC technology. For example, computational mechanics, such as the finite element method; a high-resolution, whole-field strain-measurement technique, namely moiré interferometry; advanced modeling and simulation software packages; and a novel image-processing approach, computational Fourier transform moiré, which allows automatic calculation of a full-field strain from digitized images of moiré fringes. These tools have been instrumental in accelerating the fundamental understanding of the mechanical reliability of SBC interconnections.

The first paper, by Corbin, addresses structural design and its optimization by minimization of mechanical strains. The reliability associated with the thermal–mechanical fatigue mechanism in SBC is the primary focus of this design optimization. By means of finite element analysis, Corbin models the total structure, consisting of the ceramic chip carrier, the solder connection, and the printed circuit card, and simulates the SBC response under accelerated thermal cyclic loading. The result is well-defined optimum geometries for the entire SBC structure.

Design optimization is not an island. It must be complemented by "reality," such as manufacturability considerations (for example, robust assembly processes), which keenly affect yields and, therefore, cost. The next paper, by Ries et al., deals with assembly-process development activities. The authors worked to ensure that the optimized design geometries were in harmony with robust assembly processes. For example, the sensitivity of yield to variations in solder volume was considered, as well as compatibility of design requirements with existing surface mount assembly technology processes and near-perfect first-pass assembly yield. Near-perfect yield is especially important because of the lack of a total inspection capability for SBC assemblies.

An integral part of the assembly-process work included thermal modeling and empirical verification. The paper by Mahaney analyzes three-dimensional transient thermal phenomena for the radiative exchange within the infrared oven used to reflow the solder and for the nonisotropic heat conduction within the ceramic chip carriers and card. His finite element analysis, verified by empirical measurements, demonstrates that the SBC modules are relatively isothermal throughout the infrared reflow process. Accordingly, every solder ball within the array experiences a nearly identical thermal profile. This is a significant finding that increases confidence that inspection of the solder ball interconnections around the periphery of the assembled modules will lead to an appropriate appraisal of the integrity of the entire array of interconnections.

The effective coefficient of thermal expansion (CTE) of a printed circuit card is one of the key parameters that governs reliability and mechanical integrity of the SBC package. The CTEs of ceramic modules do not vary much from 6.2 ppm. However, the CTEs of FR-4-based printed circuit cards vary considerably as they are affected by the card construction. For example, the type of woven-glass fabric, fraction (by volume) of epoxy resin, drilled-hole parameters, copper content, and solder in the plated

through hole have a profound influence on the CTE of printed circuit cards. The paper by Wu et al. describes a systematic study of effective CTE in multilayer printed circuit cards. A quantitative three-dimensional engineering model based on classical mechanics and rule-of-mixtures theory was developed in which the in-plane and out-of-plane CTE can be accurately predicted. The verification of the model by a series of experimental measurements, including moiré interferometry, is also presented.

The paper by Guo et al. describes the basics of moiré interferometry, a very powerful method capable of measuring the whole-field displacement and strain in tiny solder joints, such as C-4 interconnections. This paper introduces the concept of local (micro) strain and global (macro) strain in SBC structures due to thermal cycling of assemblies. This leads to the identification of risk sites in SBC joints. The technique can also be used to make measurements of micro-displacements within SBC structures. Such measurements were made and used to verify the displacements predicted in Corbin's FEM study. This very high-resolution optical interferometry technique is ideally suited to address a broad range of problems encountered in electronic packaging.

In the final paper, Part II of the previous paper, Choi et al. introduce a new image-processing technique, the computational Fourier transform moiré method. This technique provides a detailed full-field strain from digitized images of interferometric moiré fringes. This image-processing scheme enhances the experimental data obtained by moiré interferometry and can bring out information that might otherwise be missed. The paper also demonstrates the use of the technique in analyzing the reliability of SBC assemblies.

Almost a quarter century spans the 1969 *IBM Journal of Research and Development* issue on C-4 technology and this 1993 issue on SBC. Powerful advanced workstations for carrying out the analyses are more readily available today, and the algorithms for computational mechanics are advancing at a rapid pace. These advanced tools are essential in the current environment of ever-decreasing development cycles. On the surface, SBC technology may appear to be a collection of simple balls of solder. However, a great deal of science and engineering development was required to guarantee field reliability of SBC technology. Collectively, the papers presented in this issue of the *Journal* represent the foundation of scientific understanding of SBC technology that enhances IBM's leadership in electronic packaging.

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Editor's note

The next issue of the *IBM Journal of Research and Development* (November 1993) will consist of a Cumulative Index of the *Journal* covering its entire history from 1957 to 1993. The Index will include listings of titles, authors, subjects, issue topics, and abstracts.

The Author and Subject Indexes for Volume 37 (1993) will appear in the first issue of Volume 38 (January 1994 issue).