Modeling the cosmic-ray-induced soft-error rate in integrated circuits: An overview

by G. R. Srinivasan

This paper is an overview of the concepts and methodologies used to predict soft-error rates (SER) due to cosmic and high-energy particle radiation in integrated circuit chips. The paper emphasizes the need for the SER simulation using the actual chip circuit model which includes device, process, and technology parameters as opposed to using either the discrete device simulation or generic circuit simulation that is commonly employed in SER modeling. Concepts such as funneling, event-by-event simulation, nuclear history files, critical charge, and charge sharing are examined. Also discussed are the relative importance of elastic and inelastic nuclear collisions, rare event statistics, and device vs. circuit simulations. The semi-empirical methodologies used in the aerospace community to arrive at SERs [also referred to as single-event upset (SEU) rates] in integrated circuit chips are reviewed. This paper is one of four in this special issue relating to SER modeling. Together, they provide a comprehensive account of this modeling effort, which has resulted in a unique modeling tool called the Soft-Error Monte Carlo Model, or SEMM.

1. Introduction

The fact that cosmic rays cause soft errors in integrated circuits (ICs) has been recognized in the aerospace community for many years, but the observation of soft errors at ground level has been reported only recently [1–3]. Since Binder et al. [4] and May and Woods [5] discovered that high-energy particle radiation can cause soft fails in electronic components, there have been many symposia and conferences devoted to this subject. The reader is referred to the proceedings of the annual Nuclear and Space Radiation Conferences, which are published as the December issues of the *IEEE Transactions on Nuclear Science*. The subject of soft errors has taken two rather independent paths, that of ground-based systems used in the computer industry, and that of aerospace applications.

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The former is mostly concerned with the effect of alpha-particles emanating from radioactive impurities in the chip materials, and the latter is focused primarily on cosmic-ray-induced fails. Although it is not generally appreciated that cosmic-ray-induced soft errors affect ICs at sea level, there has been much activity within IBM on this subject over a number of years. (See [3] for the experimental part of this study.) From a theoretical standpoint, one major outcome of this activity is the development of a state-of-the-art computer software called the Soft-Error Monte Carlo Model, or SEMM, for predictive modeling of this phenomenon [1, 6].

SEMM was developed as a modeling methodology that is truly predictive, *without* the need for arbitrary parameter fitting or expensive high-energy beam testing. This was made possible by adopting a physically based modeling approach. In this paper we describe the principles and methodologies of such an approach. SEMM has been used routinely in the design of several generations of IBM bipolar and CMOS IC chips in order to enhance their soft-fail reliability. The ability to estimate SER at an early stage of IC design allows the designer to evaluate different designs of circuit elements and package alternatives in order to meet his performance-reliability goals. This is especially true for IC chips with high alpha-emissions, or for applications in which cosmic rays play a significant role in producing soft fails. Chip designers at IBM have used SEMM to develop soft-error hard-chip designs and to make performance–reliability trade-offs at early design phases of a product. For example, the use of SEMM was a crucial factor in the design of a bipolar logic chip used in the 3090 machines, in which the low-power embedded array designs which were initially very sensitive to radiation-induced soft errors were modified. In another example of CMOS and bi-CMOS SRAMs which used four device NMOS cells with high-resistivity polysilicon loads, the high SER sensitivity was decreased sixfold after SEMM was used to redesign the chip by adding a boron implant in the epitaxial layers under the sensitive junctions. SER specifications continue to be important design requirements in CMOS DRAM and SRAM development in IBM, and SEMM is used in this design cycle.

There are many process, device, and technology solutions to mitigate the soft-failure rate in computer chips. Reduction in the diffusion area, deep-trench isolation, double-well structures, implant under the sensitive nodes, and the use of silicon-on-insulator technology are some of the solutions employed in combating the soft-error problem. Some circuit solutions such as the addition of cross-coupled resistors and capacitors, decreased bit-line float time, clock reset, and parity check are also used. From a system point of view, one can employ error-correction codes and store-through cache, leading to improved SER reliability.

This overview is the first of four papers being published on SER modeling in this issue. A detailed description of the SEMM computer program is given in [7]. The nuclear modeling of the cosmic ray interaction is presented in [8]. Finally, the methodology and the calculation of the circuit critical charge for a bipolar memory cell are presented in [9]. Together, these papers describe a unique modeling package for the predictive modeling of the soft-error rate in IC chips. In Section 2 of this paper, relevant modeling concepts are examined. Semi-empirical methodologies using heavy ion and proton accelerators and charge-collection measurements are discussed in Section 3. In addition to [1, 6], experimental verification of SEMM, not presented before, is discussed in Section 4. Finally, in the last section we summarize SER modeling considerations together with some future requirements.

2. Modeling concepts

Some notable items that are incorporated in SEMM are the field funneling phenomenon [10–12]; Monte Carlo modeling of charge transport and collection [13–15]; nuclear interactions of the cosmic ray particles [16, 17]; circuit definition of critical charge and its dependence on pulse shape [6, 9]; the concept of nuclear history files and the use of event-by-event simulation; modeling of the charge sharing by several neighboring circuit nodes; device vs. circuit simulations; and, finally, statistics of low-probability events. These developments are discussed in the following sections.

- *Field funneling*

A transient distortion of the electric field in the depletion region occurs when an ion track intercepts a p-n junction. The equipotential lines are stretched in the shape of a funnel along the track, and the excess charges produced by a radiation track inside this funneling region are collected very rapidly (typically within a fraction of a nanosecond), which results in a return of the field to the steady-state condition. The funnel has two effects as far as the SER is concerned. First, it increases the total amount of charge collected by the radiated junction as it encompasses a larger portion of the radiation track; second, it produces a sharp peak in the disturb current because of the rapid collection process. These have different effects on static and dynamic RAM circuits. In DRAM circuits, where the storage cells are periodically refreshed, the cell state changes if a disturb current pulse generated by the ion track causes the cell node voltage to change within the time duration of the refresh cycle. This time is large (a few ns) relative to the charge-collection times from drift/diffusion in the semiconductor. Thus, the total charge of the disturb pulse which is collected within the refresh cycle determines whether or not a change of state has occurred. On the other hand, in SRAM circuits the cell

stabilization is produced by the inverter circuits within a short cell response time of few tens of picoseconds, and one does not have a long refresh cycle. Thus, for a circuit failure due to an ion strike to occur, sufficient charge must be collected at the struck node before the node recovers within a very short time, thus making the pulse duration important. A sharp disturb pulse pumps more charge in a shorter time than a slow-rising pulse. For this reason, the pulse shape effects are more important for SRAMs than for DRAMs. Nevertheless, funneling increases the SER for both SRAMs and DRAMs because of the increased charge-collection volume, as mentioned earlier. SER radiation hardening schemes use structures that limit the funnel, such as silicon-on-insulator or heavily doped substrates. Any successful SER modeling methodology must include the funneling effect. For modeling purposes, the funnel is characterized by the funneling depth within which rapid collection occurs. To model angular strikes of ions, it is necessary to determine the extent of the funnel along the angular track. Experiments [18] and 3D device simulations [19] indicate a $\cos\theta$ dependence of the funneling depth with the angle of the track. The effect of funneling on the SER is discussed further in the subsection on critical charge.

• *Monte Carlo modeling of charge transport*

Sai-Halasz [13–15] developed a three-dimensional Monte Carlo model based on random walk for the transport of excess carriers generated by the passage of an ion through a semiconductor body. The governing assumptions in the model were that the excess carriers created by the radiation event do not significantly alter the steady-state fields in a device structure, and that diffusion/drift can be simulated by the Monte Carlo procedure to obtain the average solution to the transport equation. A simple three-dimensional random walk is set up with spatially dependent drift. The random steps that are consistent with the diffusion constant of the carriers are modified in the presence of a field by a deterministic drift in the direction of the field after each random step. The Monte Carlo results agreed well with the charge-collection experiments [13], validating the model assumptions. The Monte Carlo approach greatly alleviates the need to solve device equations in three dimensions, and allows the modeling of a large number of devices in an integrated circuit in one simulation. We have modified this model to include funneling and pulse shape effects. These are inputs into SEMM from a separate transient device analysis from which the funneling depth and the expected current pulse shape are determined at various device junctions. SEMM has an additional, important advantage over conventional device simulators in that it allows a separate circuit analysis of the effect of the disturb currents to be input into SEMM. The circuit simulator uses the actual chip circuitry, which contains circuit, device, process, and topology information. For a detailed discussion of this subject, the reader is referred to the paper by Freeman in this issue [9].

Since the Monte Carlo transport model involves tens of thousands of diffusion steps, it uses a considerable amount of computer time and memory, typically of the order of several CPU hours and megabytes, respectively. However, it is much simpler and less expensive than using 3D device modeling programs for a large number of devices that are connected in a chip circuitry, especially when dealing with nuclear tracks in random directions.

• *Modeling the nuclear interactions*

Central to any modeling of the cosmic-ray-induced soft failure is the understanding of the nuclear interaction of cosmic ray particles with the nuclei of the atoms in the chip. Cosmic rays may be divided into primary or galactic cosmic rays and secondary or terrestrial cosmic rays. The former exist in the space environment above the earth's atmosphere and consist primarily of protons, alpha-particles, and heavy nuclei such as Fe. The terrestrial cosmic rays, on the other hand, are the result of the cascades of primary protons through the earth's atmosphere and their interaction with the atmospheric nuclei. The terrestrial cosmic rays are of considerable geophysical interest, and a large body of knowledge exists. (See [20] in this issue for a review.) Heavy ions do not reach the surface of the earth, and we need only consider secondary protons, neutrons, pions, muons, and electrons in dealing with the terrestrial cosmic rays. Among these, only protons, neutrons, and pions produce strong nuclear interactions with the chip nuclei, resulting in energetic ion fragments which cause charge tracks in the semiconductor. Muons and electrons do not produce nuclear fragments and also do not have sufficient electron–hole charge density in their tracks to cause soft fails.

There are two types of nuclear interactions of cosmic ray particles: elastic and inelastic. The former does not produce nuclear fragments, and no energy is lost to the internal excitations of the target nucleus. The kinematics of an elastic event is simulated using models based on optical potentials [21, 22]. The inelastic interactions, also called nuclear spallation, involve the interaction of the cosmic particle with the nucleons inside the nucleus. There are many nuclear spallation codes (for example, [23–25]) that simulate these nuclear strong interactions. Briefly, these codes model spallation in two stages: a cascade and an evaporation stage. In the cascade stage, the incoming particle suffers a series of binary collisions with the nucleons inside the nucleus, as specified by the free nucleon–nucleon scattering cross sections. It is a semiclassical model obeying the Fermi motion and the Pauli principle. In this cascade stage, protons or neutrons may escape the nucleus. The resulting nucleus is highly

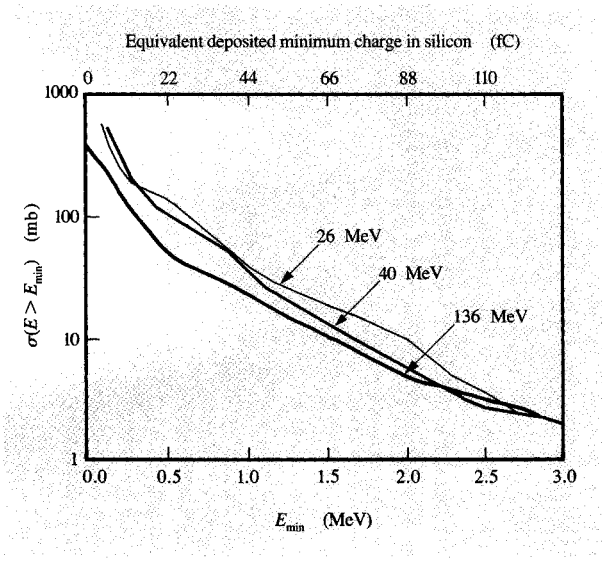

Figure 1

Experimentally measured cross sections (σ) of elastically scattered recoiling nuclei with kinetic energies, E, greater than E_{min}; i.e., $\sigma(E > E_{min})$, plotted vs. E_{min} for neutrons with different energies incident on Al. E_{min} is the minimum energy deposited in the chip by a recoiling nucleus. Note that nuclear elastic scattering cross sections for Al and Si are similar. The minimum equivalent charge deposited in Si (top) corresponding to E_{min} is also shown. (1 mb = 10^{-27} cm^2.)

excited, and it reaches thermodynamic equilibrium by a nuclear evaporation process which may result in the emission of both light and heavy nuclear fragments. Both the cascade step and the evaporation step can be modeled by Monte Carlo techniques. For further details, the reader is referred to the paper by Tang [8] in this issue.

We have developed a nuclear simulator, NUSPA [16], based on the work of Bertini's MECC program [23]. A new evaporation code is written in NUSPA to replace that of MECC, taking into account appropriate inverse capture cross sections and all of the exit channels. In [16, 17] we have demonstrated that NUSPA reproduces the nuclear spallation data much more accurately than MECC.

It is important to investigate the relative importance of the elastic and inelastic events, since many workers consider elastic events to be one of the primary contributors to SER. As the following discussion shows, this is not the case.

When an incoming nucleon (neutron or proton) hits a target silicon nucleus in the IC chip and suffers nuclear elastic scattering, the nucleon is scattered mostly in the forward direction, producing a recoiling silicon nucleus. The scattering phenomenon is described by the quantum mechanics of the compound system. The 2D classical analog of the scattering is that from a circular disk, which results in a scattered wave whose intensity is maximum in the forward direction and falls off rapidly with the angle. The nuclear elastic scattering is similar to this. The incident nucleon is forward-peaked, and the recoil nucleus moves in a direction nearly perpendicular to the incident direction. The recoil energy of the target nucleus can be calculated from the conservation of energy and momentum. This discussion is limited to "shape elastic scattering" and does not consider a small contribution from "compound elastic scattering," which involves nuclear reaction. **Figure 1** shows the experimental data of the elastic scattering of neutrons from aluminum, where the scattering cross section, $\sigma(E > E_{min})$, for a recoil energy (E) larger than a minimum energy (E_{min}) is plotted against the minimum energy for 26-MeV, 40-MeV, and 136-MeV incident neutron energies[1]. The 136-MeV curve is partly derived by theoretical extrapolation due to incomplete measurements of the angular spectra. For soft errors, E_{min} can be taken as the minimum energy deposited by the recoil nucleus. (For silicon, 1 MeV of deposited energy is equivalent to 44 fC of charge.) The following observations are made from this figure: First, the elastic recoil cross section increases with decreasing deposited energy. This means that there are more elastic events that produce low-energy recoils than high-energy recoils. Since the cross sections in Figure 1 are plotted on a log scale, this increase in the probability (cross section) of low-energy deposition events is quite large and could cause serious SER consequences when the critical charge necessary to trip the circuit approaches 10–15 fC. Second, the elastic recoil probability increases as the incident neutron energy decreases. Thus, the elastic contribution is more important at low neutron energies than at high energies.

In order to further compare the contributions of elastic and inelastic nuclear events, we ran SEMM for the case of a 30-MeV neutron hitting the chip. A CMOS SRAM chip was used for the simulation. The critical charge of the chip was scaled to low values, approaching zero. SERs were calculated for both elastic and inelastic collisions. **Figure 2** shows the results of this simulation, where the probability of a soft fail is plotted as a function of the critical charge. A low value of neutron energy (30 MeV) was chosen to increase the probability of elastic contribution to SER, as discussed earlier. The figure shows that even at very low values of the critical charge, the inelastic contribution dominates the soft-fail phenomenon. The elastic contribution is about 20% of the total. This simulation experiment indicates that for all foreseeable device technologies, SERs will be dominated by inelastic events. It is also interesting to observe that the SER sensitivity to changes in the critical charge increases sharply below ~25 fC.

[1] N. Azziz (unpublished work).

In addition to the spallation reactions of protons and neutrons, we have also modeled the effect of pions. These results [1] show that pions could contribute significantly to the energy deposition, and at energies around 250 MeV, pions deposit more energy than protons because of a resonance in the pion–proton interactions in the nucleus. However, the pion flux is much lower than the proton or neutron flux at sea level, so that the pion contribution to sea-level SERs would still be small.

- *Critical charge*

The concept of a charge threshold necessary to alter the state of a memory cell is well accepted, both in terms of theory and experiment. However, a definition for this critical charge (Q_{crit}) varies with the techniques used for its determination. From a theoretical standpoint, circuit Q_{crit} must be defined in terms of the actual chip circuitry, which includes all of the device, process, and layout aspects. As we have discussed in the subsection on field funneling, DRAM and SRAM circuits have different soft-failure modes, and hence the specification of Q_{crit} is different for these cases. For SRAM circuits, Q_{crit} depends not only on the total charge collected by the sensitive node in the circuit, but also on the temporal shape of the current pulse. Because of the long refresh cycle times in DRAM circuits, on the other hand, the pulse shape effects are not important.

Calculation of the circuit Q_{crit} for SRAMs is made by injecting current pulses into the sensitive nodes and determining the smallest charge of the pulse necessary to switch the state of the circuit. The paper by Freeman in this issue [9] describes this technique in detail for a bipolar SRAM circuit. It should be pointed out that the time it takes the circuit to recover from a disturb pulse depends on how close the collected charge is to Q_{crit}. When the collected charge is very close to Q_{crit}, the circuit may go into a metastable state with long recovery times, and circuit failure occurs when a random noise in the circuit trips the circuit. For this reason, an operational definition of Q_{crit} is made as the largest charge for which the cell recovers to, for example, 90% of its original node voltage within 10 ns. These parameters are at the discretion of the chip designer to define fails in a circuit.

Chip IC critical charge is a phenomenological parameter that depends, in turn, on many device, circuit, and technology parameters. As Freeman points out [9], the critical charge calculations involve pulse shape effects, statistical variations of the power supply voltage, temperature, and process parameters, word and drain line resistance, etc. This is illustrated in **Table 1,** which shows how Q_{crit} changes with the $\pm 3\sigma$ variations in the bipolar technology parameters. This demonstrates how the Q_{crit} is intertwined with the technology parameters. Thus, for an accurate calculation of Q_{crit} for the chip integrated circuit, one needs a good chip circuit model which considers all

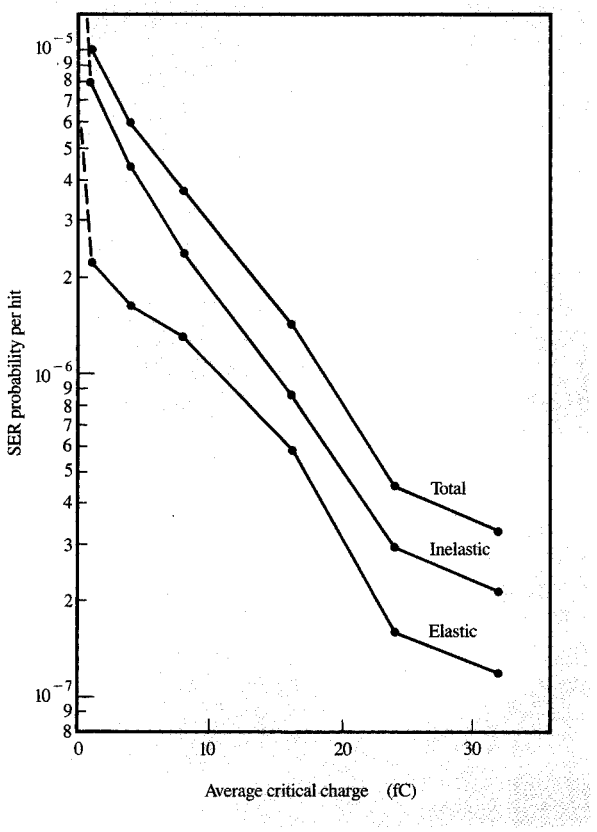

Figure 2

SEMM simulation of the elastic and inelastic contributions to the probability of a soft error for each collision (hit) of a 30-MeV neutron as a function of the average critical charge for an SRAM chip.

Table 1 Range in critical charge due to $\pm 3\sigma$ variations in processing, device, and operating parameters for a bipolar cell with a nominal Q_{crit} of 498.7 fC. This table is taken from Figure 8, Reference [9], p. 125 of this issue, with permission of the author.

$\pm 3\sigma$ variation in	Q_{crit} (fC)
Epitaxial layer thickness	−81 to +57.6
Extrinsic base hole current	−48.8 to +69.6
Base polysilicon pattern	−46.3 to +65.1
Inverse npn electron perimeter current	−37.9 to +52.2
Junction temperature	−39.8 to +40.5
Epitaxial layer dopant concentration	−26.1 to +34.8
Extrinsic base electron current	−23.6 to +36
Base-implant-to-isolation spacing	−13.4 to +19.6
Subcollector-reachthrough-to-isolation spacing	−10.9 to +18.6
Lateral pnp base width tracking	−10.5 to +13.9
Isolation pattern	−7.2 to +14.9
npn emitter mask tracking	−9 to +11

such parameters. This is provided by the chip designer, who has the circuit model with calibrated device cross sections. For this reason, attempts to calculate SERs by device simulations do not yield a correct picture.

In SEMM we took the following approach: First, Q_{crit} for the chip circuitry in question is calculated by injecting current pulses into the individual sensitive nodes in the actual chip circuit; the information is collected in tabular form for various pulse shapes. As described earlier [6], the pulse shape is characterized by a double exponential with a pulse rise time constant and a pulse decay time constant. For most practical purposes, we define the rise time constant to be very short (1 ps), and constant, for all pulses. The decay time constant, τ_d, is treated as a variable. Simulations of the chip circuitry are made using a circuit simulator such as ASTAP or SPICE to produce a Q_{crit} vs. τ_d table for each node. These tables are saved in SEMM for later determination of whether or not a certain pulse-creating event has caused a circuit failure. The partial charges on different nodes are summed up in accordance with the way the nodes are connected in the circuit path, with appropriate signs and weights. We return to this point later in the subsection on charge sharing.

SEMM uses these Q_{crit} vs. τ_d lookup tables in the following way. When an ionizing track is set up and the resulting charges are collected by all the junctions in the analysis region with their times of arrival, a program fits these charges to a double exponential, as mentioned earlier. From this, the pulse shape, the time constant (τ_d), and the total charge collected (Q_{coll}) are recorded for that event. The SEMM postprocessor looks up the Q_{crit} table for that time constant and determines the Q_{crit}. This is repeated for all of the nodes connected in the circuit path, and the ratios of Q_{coll} to Q_{crit} are added, with appropriate weights assigned to them by the wiring rules. If this sum is equal to or greater than one, a failure has occurred. This result is written to a statistical file, and the process is repeated for tens of thousands of ionizing events to determine the corresponding SER. The reader is referred to the paper by Murley and Srinivasan in this issue [7] for more details of this procedure. It is to be emphasized that a nuclear spallation event may cause simultaneous, multiple tracks, and the procedure must include charge collection from all of the tracks before a determination of circuit failure is made for that event. In the same way, one can determine the occurrence of two or three simultaneous fails due to an ionizing event. It should also be pointed out that since each random track intercepts the depletion and funneling regions to different extents depending on the position of the hit and the angle of the track, different pulse shapes can arise from different events of the same kind. Also, each event is considered to be independent of the others, since the cell recovery times are short compared to the time between the ionizing hits, even for particle beam experiments. In this way, soft-fail statistics can be accumulated.

- *Nuclear history files and event-by-event SER simulation*

Previous SER models have used average nuclear cross sections and collection probabilities. These methods do not allow for variations in the Q_{crit} and sensitive volume of different nodes. The present author has developed a clear departure from this average description of the nuclear events which is based on an event-by-event simulation of the nucleon hit from cosmic rays or particle beams. This forms the basis of the cosmic ray SER modeling in SEMM. The advantages of using the event-by-event simulation are the following: 1) each p-n junction in a detailed chip layout can be treated separately; 2) the common assumption of a uniform and sensitive volume on a chip can be avoided; 3) the dependence of pulse shape on the position and angle of a track can be included; 4) the formation of multiple tracks in a cosmic ray collision, each of which may hit different devices at the same time, thus causing multiple bit fails, can be modeled; and 5) charge sharing by different nodes in the circuit path can be modeled.

To achieve event-by-event simulation in the modeling of cosmic-ray-induced SERs, NUSPA [16] is used to determine the kinematics of nuclear spallations, and ABACUS [22] for the nuclear elastic kinematics. By running NUSPA and ABACUS programs many thousands of times, nuclear history files of events are constructed in which the direction and energies of the track-producing particles are stored for a given incident nucleon energy. This is repeated for several incident energies. Since the elastic and spallation events are random, each successive identical event produces a different kinematic result for identical initial conditions. Thus, each event produces a different pulse shape and circuit failure consequence. For present applications, where Q_{crit} values range from 30 to 40 fC, it is sufficient to consider the alpha-particles and the recoil nucleus in a nucleonic collision. But as the chip technology advances, with ever-decreasing Q_{crit}, other particle emissions from the nuclear spallation such as deuterons, tritons, and low-energy secondary protons must also be considered. For modeling the effects of terrestrial cosmic rays on chip SER, we need to consider nucleons of various energies that constitute the cosmic ray spectrum. Accordingly, NUSPA results are stored for many energies. The cosmic ray fluxes are also stored as a function of energy geomagnetic longitude and latitude, and altitude [20]. The SEMM postprocessor integrates the flux vs. energy data with the SER vs. energy data to obtain the total SER. For details of this procedure, see [7].

- *Charge sharing*

When an ion track hits two or more neighboring nodes, or when it hits one node and passes close to a second node,

the amount of charge shared by these nodes and their effect on the circuit failure must be calculated. This calculation is necessary when an event-by-event simulation is made and the charge-sharing nodes are connected in a circuit path. When neither of the nodes collects enough charge to individually cause soft failure, a calculation must be made to determine whether the contributions from these nodes are additive. Using a circuit simulation program, we have investigated the additive effects of multiple current sources in a circuit, and have found that in most cases a linear superposition technique is adequate. In these cases, the fractional charges divided by the Q_{crit} of the respective nodes are summed with their weights and signs. A soft fail is said to have occurred if the sum is greater than one. For example, switching occurred in an SRAM cell when half of the critical current of the high node was injected into the high node and nearly half of the critical current of the low node was injected into the low node in the reverse direction. This indicates an equal weighting of the high and low nodes in a symmetrical SRAM configuration. When an ionizing particle collides with one node and the other neighboring node is not bombarded but is close to the ionizing track, the bombarded node collects the charge rapidly through the funneling mechanism, while the other node collects the charge by diffusion. The current pulse shapes are quite different for these two nodes. The bombarded node has a sharper pulse and, hence, a lower Q_{crit}, while the other node has a slower-rising pulse and a higher Q_{crit}. The SEMM program automatically adds these Q_{coll}/Q_{crit} ratios algebraically.

• *Device vs. circuit simulations*

The collection dynamics of excess carriers generated by radiation events is traditionally estimated from device simulations [10, 19, 26–28] which focus on the device details, such as funneling and ion track structure. The simulations, while valuable from a device charge-collection perspective, do not take the chip circuitry fully into consideration. Recently, some attempts were made to include elements of circuit considerations in simulating SERs [29–31], but they still lack the advantages of the Monte Carlo method in treating the full 3D geometry of a complex chip. The soft failure rate is a statistical number which requires modeling of hundreds of thousands of charge-producing events in order to obtain a statistically meaningful picture. The statistical running of a conventional device simulator, taking into account all angles of tracks full 3D, is a prohibitive cpu task. The Monte Carlo technique allows this statistical, event-by-event simulation in a reasonable cpu time in the order of hours. Also, the soft failure on a chip is a complicated phenomenon involving charge sharing, multiple tracks, and pulse shape effects. Even the definition of the critical charge requires a full simulation of the circuit response and

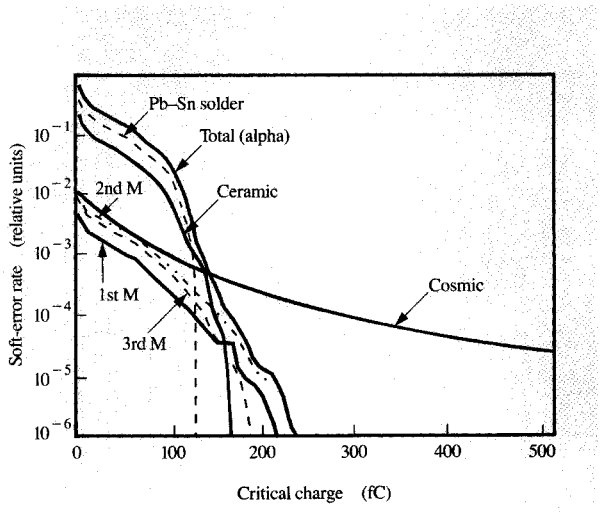

Figure 3

SEMM simulation of soft-error rates as a function of critical charge for a bipolar memory cell due to cosmic radiation and to alpha-particle sources. The alpha-particle sources are radioactive contaminants in the first-, second-, and third-level metal (M) layers, the ceramic layer, and the Pb–Sn solder pads.

the inclusion of technology parameters [9], as discussed previously. The SEMM program uses the circuit response simulation, requiring a chip layout, vertical dopant profiles, and Q_{crit} as a function of pulse decay time constant. With the SEMM approach, soft-error rates can be simulated for complex chip structures. As an illustration, we show the SEMM simulation results in **Figure 3** for a bipolar chip where the soft-error rate is plotted as a function of Q_{crit} due to many chip alpha-radiation sources and terrestrial cosmic rays at sea level. The critical charge shown in this figure corresponds to a constant, trapezoidal pulse shape. For cases where pulse shapes are important, a dynamical critical charge must be defined. This is done as follows: After the SEMM run is made for thousands of hits, with each radiation hit causing a different pulse shape, the decay time constants of all of the pulses in the simulation which cause fails are arithmetically averaged, and a "dynamical Q_{crit}" corresponding to this average time constant is defined. This dynamical Q_{crit} is taken as an indicator of the average critical charge for the chip. We note from the figure that while the chip alpha-induced SER decreases drastically with increasing Q_{crit}, the cosmic ray contribution persists for large values of Q_{crit}.

• *Statistics of low-probability events*

The soft-error rate is usually a very low-probability event, and when a small number of discrete observations (obtained from measurements or simulations) of soft errors

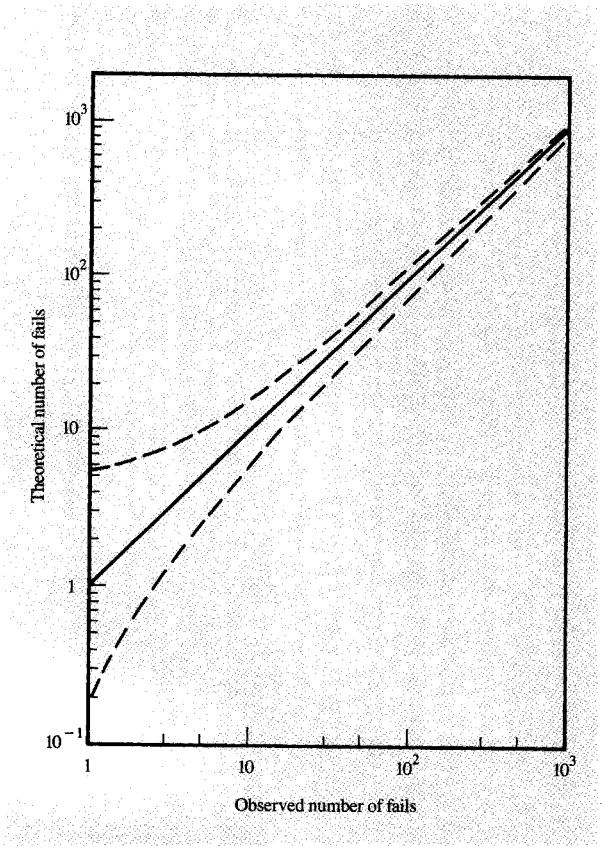

Figure 4

The 90% confidence limits for the theoretical number of fails as a function of the number of fails observed by simulation or measurement.

are made, it is important to establish the confidence limits on the SER number. In SEMM we provide a means to sort out the data by dividing the failure data into a small number of statistical samples from which the variance can be estimated. This is valid when a large number of soft errors have been simulated; i.e., when the product $n \cdot p$, where n is the number of events (trials) and p is the probability of error, is large, the statistical distribution can be approximated by a Gaussian. However, for small $n \cdot p$ the distribution approaches the Poisson distribution. For this case, O'Brien[2] has shown that the 90% confidence limits on the theoretical number of fails are a function of the observed number of fails. His results are shown in **Figure 4**. It is interesting to note that the theoretical number of fails is not a function of the number of events (trials); it is instead a function of the observed number of fails. Thus, for example, when only one fail is observed, the theoretical 90% confidence limits will be 0.2 and 5. For an observation of 20 fails, the 90% limits will be 15 and 30. This point should be considered when the number of soft-fail observations, either in the simulation or in the measurement, is small.

3. Semi-empirical methods

Single-event upsets (SEUs) due to cosmic rays have been observed both in space satellites and aircraft. In the near-earth space environment (1–10 earth radii), protons and heavy nuclei are the primary cause of SEUs. (For a recent review on this subject, see [32].) At aircraft altitudes (about 10 km), neutrons are the main cause of SEUs [33]. Detailed chip information is often not used in the SEU models for aerospace applications. Instead, semi-empirical methods, described below, have been developed to characterize the chips using high-energy particle beam testing or charge-collection measurements.

- *Methods based on proton testing*

The most direct semi-empirical method of estimating SER due to protons was developed by Bendel and Petersen [34]. The basis for this method is that a curve characterized by a "threshold energy" and a saturation cross section is obtained when the measured SEU cross section per proton for a chip is plotted against the proton energy. This curve is described by an equation with one [34] or two [35] "Bendel parameters." Generalized curves of proton SEU cross section vs. proton energy for several values of the Bendel parameters have been plotted. When an SER for a chip is required, the Bendel parameters for that chip are determined by one or more proton accelerator experiments. By using the generalized Bendel curves, the SEU cross section is obtained as a function of proton energy for that particular chip. The total SER for the chip is then obtained by convoluting the proton environment (flux vs. energy) with the cross-section curve. This method has been widely used in modeling single-event upsets due to protons in primary cosmic rays (see for example [35]). The method used in the proton accelerator experiments for terrestrial SER projections reported in this issue [3] is based on a similar convolution procedure; the proton SEU cross sections are measured at many energies and then interpolated. For terrestrial applications, where neutrons are the species responsible for soft fails, because the protons are absorbed in the shielding materials, an assumption is made that protons and neutrons behave identically. This allows the use of proton accelerator experimental data for estimating neutron-induced soft-error rates at ground locations. However, below 50–100 MeV, Coulomb effects become increasingly important, and differences between proton- and neutron-induced spallations must be included.

[2] R. R. O'Brien (unpublished work).

• *Methods based on neutron testing*

Recently, a new experimental determination of SER due to cosmic rays at aircraft altitudes was reported using a continuous-energy neutron source at the Los Alamos National Laboratory's Weapons Neutron Research (WNR) facility [36]. The neutron beam at WNR has nearly the same energy spectral shape as the cosmic ray neutrons at high altitudes, but with an intensity that is 10^5 times that of neutrons at flight altitudes. Since most of the SER at high aircraft altitudes is due to neutrons [33], the SER of a chip at high altitudes is determined in a single, short accelerator experiment. This method can also be used for estimating ground-level SERs, since the neutron spectral shape at sea level is also very similar to the WNR spectrum. Thus, the WNR experiment provides a fast and direct way to estimate the cosmic-ray-induced SER of a chip at terrestrial altitudes.

• *Methods based on heavy-ion testing*

To calculate the soft-error rate for a chip for which no design information is available, methods are needed to estimate the sensitive volume and the critical charge for devices in the chip. Both quantities are estimated by using heavy-ion beam experiments [37, 38] using a LET (linear energy transfer) parameter. (For a critical review of these LET-based techniques, see Petersen et al. [39] and Xapsos [40].) The LET is equal to the stopping power of the ion per unit length in the semiconductor medium if all of the energy absorbed by the medium is converted into the production of electron–hole pairs. For such a case, the LET is calculated from stopping power formulas [41]. When a chip is exposed to several types of ion beams of different LETs in a heavy-ion beam experiment and the SEU cross section vs. LET is plotted, a LET threshold and a saturation value in the cross section are obtained. The measurements are taken for different heavy-ion energies and angles to get a complete range of the plot. For nonvertical beams, an effective LET equal to LET/cos θ is defined. For point charge burst calculations, the critical charge for the chip is obtained by multiplying the value of effective LET corresponding to the initial saturation region of the SEU cross-section curve and the assumed thickness of the device charge-collection volume. For non-point burst calculations involving tracks of some length, the critical charge is obtained for the maximum possible path length of the ion inside the sensitive volume. The sensitive volume for the chip is calculated as the product of the saturation value of the SEU cross section and the assumed collection volume thickness, based on the premise that the saturation value of the SEU cross section has an area equal to the sum of all the sensitive areas in the chip and that there are no multiple fails. The sensitive volume and critical charge data thus obtained are used to calculate the SER due to cosmic ray heavy ions and

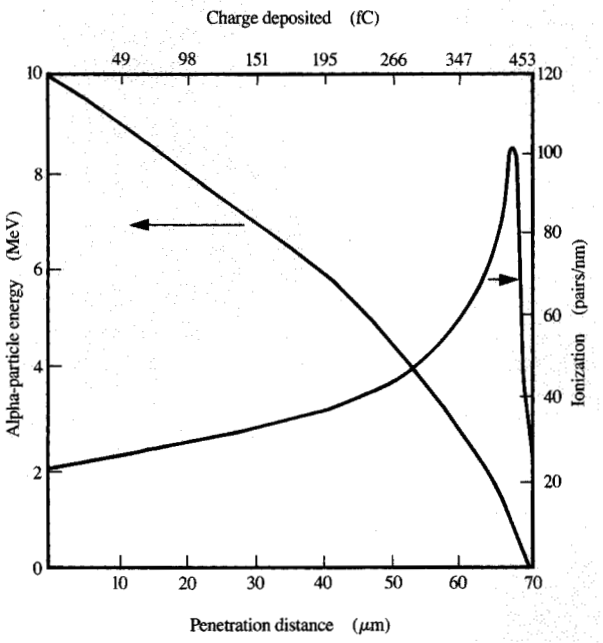

Figure 5

Variation in the energy and the number of ionization pairs along the length of a 10-MeV alpha-particle impinging on silicon.

nucleons. It should be pointed out that the LET-based simulations use the energy-loss value at the beginning of the ion track and do not consider its variation along the track. This constant LET value can cause significant errors in the SEU rate calculation. For example, we show such a LET variation in **Figure 5** for a 10-MeV alpha-particle incident on a silicon body. The LET value, as indicated by the number of ionization pairs produced, at the end of the alpha-particle track is nearly five times the incident LET value. Thus, a constant LET is not a good approximation. SEMM includes such a variation in the energy loss along the particle track.

SEU due to heavy ions in space The measured heavy-ion SEU cross section per particle per chip vs. effective LET is integrated with the cosmic flux vs. LET for various heavy ions to yield the total SEU rate for the chip in that cosmic environment. It should be pointed out that the semi-empirical calculations of SEUs for heavy ions are for the direct ionization effects, with no nuclear interactions between the heavy ions and the chip nuclei.

SEU due to protons and neutrons in cosmic rays Once the critical charge and the sensitive volume for the chip are estimated from the heavy-ion experiments, charge

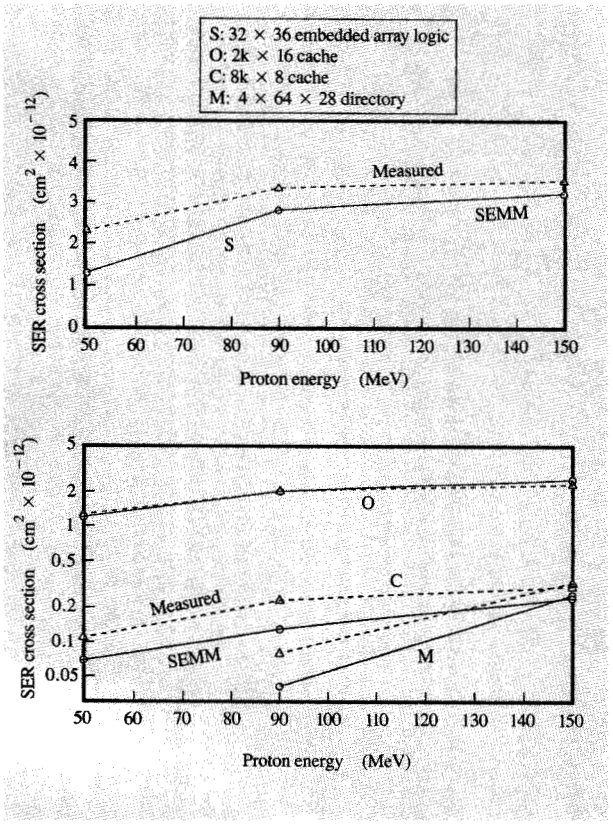

Figure 6

Comparison of SEMM simulation (solid lines) with measurements from proton beam experiments (dashed lines) of SER cross sections for four different bipolar chips.

burst calculations [42] are used to obtain a burst generation rate (BGR) for protons or neutrons as a function of their energy. In this method, the energies of the elastic recoils and of the alpha-particles are converted into electron bursts, assuming that all of the energy deposited is converted into such bursts. The recoil events are considered as point bursts, whereas the alpha-particles are treated as the rectangular parallelepiped path length (RPP) distributions in a rectangular sensitive volume [43]. This method involves many oversimplifications, such as single sensitive volume and single Q_{crit}, and thus is an imprecise indicator of SEU. Nevertheless, it is one of the methods that have been used for estimating the SEU rate of chips for which no detailed chip information is available. Some improvements in this method are made to get better charge burst cross sections by including more important inelastic recoil events in the charge burst production [44, 45]. The BGR is convoluted with the nucleon flux spectrum and integrated with respect to the nucleon energy to obtain the upset failure rate due to neutrons or protons.

- *Method based on charge-collection spectra*

McNulty et al. [46] have developed pulse height measurement techniques to determine the sensitive volume of a reverse-biased junction. The energy deposited by the passage of a high-energy ion in a silicon detector appears as a peak in the pulse height spectra; the energy deposited in the sensitive volume of the device is defined as the peak value. The sensitive volume of a circuit is estimated from the LET value of the ion, the energy absorbed, and the device cross section. An estimation of critical charge based on heavy-ion experiments can be used with these charge-collection spectral measurements to estimate the SEU rate empirically.

As mentioned earlier, the semi-empirical methods are designed to estimate the SEU rates for an IC chip when the detailed chip layout and circuit information is not available. The methods depend on many assumptions about the collection volume thickness, sensitive volume, and critical charge which are causes of large uncertainties in the SER projection [47]. The Single-Event Effects Rate (SEER) Committee recommends standards and guidelines for SEER calculation for aerospace applications [48] which use the semi-empirical methods.

4. SEMM verification

SEMM has been verified with a considerable number of SER experiments on bipolar and CMOS chips at the chip and system levels [1, 3]. SER measurements of the bipolar chips from a thorium foil experiment [6] and proton beam fixed-energy experiments [1] showed very good agreement with the results of SEMM simulation. We show in **Figure 6** additional proton beam experimental measurements, together with SEMM simulation results for four different kinds of bipolar chips. In all of these cases SEMM was run *with no parameter adjustments*. It is seen that SEMM reproduces the measurements well, thus demonstrating the predictiveness of the model. Similar results have been obtained for all recent IBM SRAM and DRAM products, where SEMM reproduces proton beam data to within ±50%. Note that these measurements are made for product chips from established product lines in which parameter control is typically tighter than $\pm 3\sigma$. Together with the excellent agreement obtained from measurements from chip testers taken at different altitudes [2] and the corresponding SEMM predictions [1], these verification experiments demonstrate the ability of an SEMM simulator to calculate SER for complex IC chips and computers.

5. Some concluding remarks

In this paper, we have presented an overview, briefly describing various concepts and methodologies that are used to model soft-error rates in integrated circuit chips. The SER modeling approaches are made at three levels of model sophistication. At the semi-empirical level, the

modeling uses some rather drastic simplifying assumptions which sometimes lead to very large errors. Also, these methods do not have the design capability needed to create soft-error hard-chip designs in the early design phase. In the next level of sophistication, modeling attempts are made to arrive at SER based on simple device/circuit considerations. The conventional device simulations do not lend themselves to using a large number of statistical runs, each requiring a prohibitively large cpu time. Furthermore, since realistic chip circuitry is not employed in these device simulations and they are based on many simplifying assumptions, they lead to uncertain results. It is important to recognize that a chip soft failure is a complex phenomenon involving many types of devices on the same chip circuitry, the production of multiple, simultaneous tracks, and pulse-shape effects. These effects leave no choice but to simulate the real chip circuitry of many devices connected in the circuit and the complex definition of chip failure. We have adopted this view in developing SEMM. Basic to this procedure are development of event-by-event treatment of the radiation hits, use of the Monte Carlo method, and soft-failure definition based on a realistic circuit analysis. With this approach and with the development of a verified nuclear physics simulator, an SER predictive design tool, SEMM, has been constructed which does not require arbitrary fitting parameters and expensive high-energy beam testing. Since the tool is predictive and all of the inputs needed are available at the design phase of an IC chip, SEMM has been used in designing chips with performance/cost and soft-fail reliability trade-offs for bipolar, CMOS, and bi-CMOS technologies. We believe that SEMM is the first model of its kind for this application. In addition to modeling the SERs due to terrestrial cosmic rays and chip alpha-radiation, SEMM can be extended to model SERs in chips used in an aerospace environment, which involves bombardment by protons, neutrons, and heavy ions. Also, as the critical charges and device dimensions reach very low values, SER effects of secondary spallation products, such as deuterons, tritons, and low-energy protons, and of low-energy neutron recoils must be taken into account. In addition, at very low critical charge values the SER sensitivity to small changes in the critical charge becomes quite large, which emphasizes the need for accurate determinations of the critical charge at these low values.

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