

Nitrided gate oxides for 3.3-V logic application: Reliability and device design considerations

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Device characteristics and reliability in a 3.3-V logic CMOS technology with various gate oxidation and nitridation processes are described. The technology was designed to extend 3.3-V devices to the ultimate dielectric reliability limit while maintaining strict manufacturing cost control. A nitrided gate oxide provided the means to maintain hot-electron reliability at the level of the previous iteration, but at higher performance and lower processing cost. Conventional furnace processes in nitrous and nitric oxide, high-pressure oxidation in oxygen and nitrous oxide, and rapid-thermal processes using nitrous and nitric oxide were investigated. We found that the concomitant variations in fixed charge and thermal budget have a significant influence on both n-FET and p-FET device parameters such as threshold voltage, carrier mobility, and inverse short-channel effect (ISCE). Reliability effects, such as charge to breakdown (Q_{BD}), hot-electron degradation,

and negative-bias temperature instability (NBTI) were examined and correlated with the nitrogen profile in the gate dielectric. Secondary ion mass spectroscopy (SIMS) profiles were used to characterize the oxidation techniques and to correlate gate dielectric composition to the parametric and reliability parameters.

Introduction

The formation of the gate dielectric is central to the CMOS process and device design. The conditions under which the dielectric is grown or deposited play a significant role in establishing the dopant profile in the silicon under the gate. For thermally grown oxide as a gate dielectric, this process probably represents the single largest diffusion step to which the well dopants will be subjected; in addition to the temperature excursion, the injection of vacancy point defects during the oxidation enhances the diffusivity of the dopants in the silicon [1-4]. The shape of the dopant profile is an important aspect of

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the design of the device. A flat dopant profile, or a profile in which the dopant decreases at greater depth, produces a device with relatively poor short-channel behavior but relatively good body effect. That is, the threshold voltage of such a device decreases rapidly at short channel lengths, thereby limiting the minimum usable length (the short-channel effect), but the threshold voltage does not increase very rapidly when the source potential is larger than the bulk potential, thereby improving the available dynamic range (the body effect). A retrograde doping profile, or one in which the dopant increases at a depth below the gate dielectric-silicon interface, produces a device in which the body effect is relatively poor, but the reduction in threshold voltage with decreasing channel length is suppressed. The precise shape of the well-doping profile is therefore critical in determining the device characteristics, and the role of gate dielectric processing that modifies the profile is important.

The final composition of the dielectric can also determine the performance and reliability of the FETs. The integrity of the silicon-silicon dioxide interface is key to the device behavior; fixed charge and unpassivated electronic states degrade the carrier mobility [5–8]. It is also important for long-term stability of the devices that the interface be able to retain its integrity under the influence of applied voltage and current flow encountered in product operation. The benefits to be gained by introducing small amounts of other elements in the silicon-silicon dioxide system have been extensively investigated [9–14]. Chlorine is often used in oxidation to keep the tools clean of sodium and other metallic contamination. Chlorine may be introduced into the process in a number of ways, such as adding HCl or TCA (trichloroacetone) to the oxidizing ambient [12]. The intended result (aside from the benefit in reducing mobile sodium) is to improve the reliability of the oxide [10]. Hot-electron immunity and carrier mobility have been shown to depend on the incorporation of trace amounts of fluorine in the gate oxide [13–17]. Adding nitrogen to the oxide has received much focus in research [18–35] and has recently been used in mainstream production [36–40]. The advantages in hot-electron immunity have been known for several years [18–20], and the benefits of suppressing boron penetration of gate oxide have been well documented [22, 23]. The incorporation of nitrogen also degrades low-field electron mobility [8], increases high-field electron mobility [30], improves charge to breakdown [24–27, 35], and increases fixed positive charge [28, 29].

Less extensively discussed in the literature are the ramifications of the nitrided gate process for FET device design. The use of a nitrided oxide introduces design parameters different from those typically considered for FET design with a conventional gate oxide. First, the well dopings must be designed to achieve the desired threshold

voltage with the fixed positive charge that results from nitridation. Depending on the method of nitridation, there may be additional thermal budget to redistribute the well dopants, limiting the steepness of the well that may be achieved and modifying the short-channel effect. Finally, the improvement in hot-electron immunity may be utilized in a variety of ways. In principle, a larger electric field may be allowed with the same level of hot-electron reliability in a device with a nitrided oxide than with a conventional oxide. To take advantage of this, faster devices might be fabricated by using shorter channel lengths. In our case, we avoid the addition of a lightly doped drain (LDD) implant to grade the junction and reduce the electric field. This reduces processing cost and complexity and improves the short-channel behavior of the device. Although the resultant electric field is higher, the nitridized oxide has greater immunity to damage, and the same hot-electron reliability is achieved as for a device with an LDD and a conventional oxide.

Although the effect of nitridation on Q_{BD} has been addressed in the literature [24–27, 35], NBTI has not been widely discussed, even though this phenomenon is clearly related to oxide and interfacial quality. The creation of fixed positive charge and interface traps in p-FET devices through temperature- and field-accelerated stress is well known, and variations in oxidation conditions have been shown to affect NBTI [41–43].

In this paper we present data (such as threshold voltage, hot-electron reliability, NBTI, electron and hole mobility, and dopant and nitrogen profiles) that illustrate the effects of various nitridation schemes with nitrous and nitric oxide on device parameters and oxide reliability. A large variation in oxidation was performed with the same basic process while holding parameters such as implant dose and energy, oxide thickness, and gate photolithography relatively constant. Data comparing conventional furnace oxidation with nitridation in nitrous and nitric oxide are given. Atmospheric furnace processes were further contrasted with high-pressure oxidations (with and without nitridation) and with rapid thermal oxidation (with and without nitridation). High-pressure oxidation and rapid-thermal processing offer greater flexibility in device design because of the lower thermal cycle employed, but all methods of introducing nitrogen do not provide the same device and reliability characteristics.

A cost-effective and simple nitridation scheme was adopted that provided adequate hot-electron reliability without unduly compromising device performance. The simplest conventional furnace process met the goals for this technology. However, the data taken from the other processes provide valuable information as to the nature of the nitrogen in the oxide. Physical and chemical explanations for the observed behavior are beyond the

Table 1 Description of the various oxidation experiments. The labels are used in Figures 1–3, 5–10, 14.

<i>Description</i>	<i>Label</i>	<i>Oxidation conditions</i>	<i>Post-polysilicon anneal</i>
Standard	E–H, <i>c</i>	800°C O ₂ /H ₂ O/950°C 20% N ₂ O/N ₂	none
No nitrogen	B	800°C O ₂ /H ₂ O	none
Undiluted	K, L	800°C O ₂ /H ₂ O/950°C 100% N ₂ O	none
Post-anneal	I	800°C O ₂ /H ₂ O/950°C 100% N ₂ O	1050°C N ₂ 60 s
	J	800°C O ₂ /H ₂ O/950°C 100% N ₂ O	1100°C N ₂ 30 s
Furnace, NO	M	NO 900°C	none
	N	NO 950°C	none
High pressure	A	O ₂ 800°C 15 atm	none
	C	N ₂ O 800°C 20 atm	none
	D	N ₂ O 800°C 15 atm	none
RTO	<i>a</i>	O ₂ 1050°C 60 s	none
	<i>b</i>	N ₂ O/O ₂ 1050°C 104 s	none
	<i>d</i>	N ₂ O 1050°C 260 s	none
	<i>e</i>	O ₂ 1050°C 56s/NO 1000°C 20 s	none
	<i>f</i>	O ₂ 1050°C 51s/NO 1000°C 120 s	none

scope of this work, but it is hoped that these observations offer practical guidelines to technology integration.

Device processing and oxidation experiments

The technology described below is for 3.3-V device applications in the 0.35- μm design rule generation; shallow-trench isolation and aluminum wire/tungsten stud planar metallization are used. The nominal channel lengths of the devices were 0.31 and 0.27 μm respectively for the n-FET and the p-FET. A shallow boron implant determines the threshold voltage and the short-channel effect for the n-FET. A deeper boron implant is included to reduce substrate resistivity and improve latch-up immunity, but has no direct impact on the n-FET device characteristics. An antimony implant determines the near-surface n-well doping, while a deep phosphorus implant defines the n-well isolation and lateral sheet resistance. The standard gate-oxidation process is a 7.0-nm nitrided oxide, grown by conventional oxidation in O₂ and H₂O at 800°C and then further oxidized in a furnace in diluted nitrous oxide at 950°C. Both n-FET and p-FET devices have a single sidewall spacer and only one implant to define the source/drain junction. Both FETs are surface-channel devices; the polysilicon gate doping is provided simultaneously with the source/drain implant. Adequate n-FET hot-electron immunity is achieved by using nitrided gate oxide, despite the lack of a graded n-FET LDD implant [36]. A single rapid-thermal anneal (RTA) at

approximately 1000°C drives and activates both source/drains. Self-aligned titanium disilicide is formed over all gates and source/drain regions. With the exception of the gate oxidation, all processing during the experiments was held constant. Implant doses and energies were nominally identical, and in every case the oxide thickness was near 7.0 nm. Shallow-trench isolation processing and metallization were nominally identical for all wafers.

As described above, the standard gate oxidation is an 800°C wet/dry oxidation, followed by further oxidation in diluted N₂O at 950°C. The various oxidation processes are briefly summarized in **Table 1**. The furnace processes were run in an ASM Model 300 vertical-tube furnace capable of running 100-wafer batches. The samples oxidized at elevated pressure were run in a GaSronics International Vertical High Pressure (VHP) system. The system is capable of pressures up to 25 atm (367 psi) and temperatures up to 1100°C in batch sizes of 63 wafers with rapid pressure and temperature ramp capability. For these experiments the gas flows, process pressure, and temperature ramps were established to optimize the oxide uniformity and nitrogen incorporation. The rapid thermal oxidation (RTO) wafers were processed in an Applied Materials RTP Centura™ system consisting of a vacuum load-lock, an N₂ purge chamber, and an isolated process chamber. For controllability and uniformity the wafer is spun at 90 rpm in the process chamber. The tool

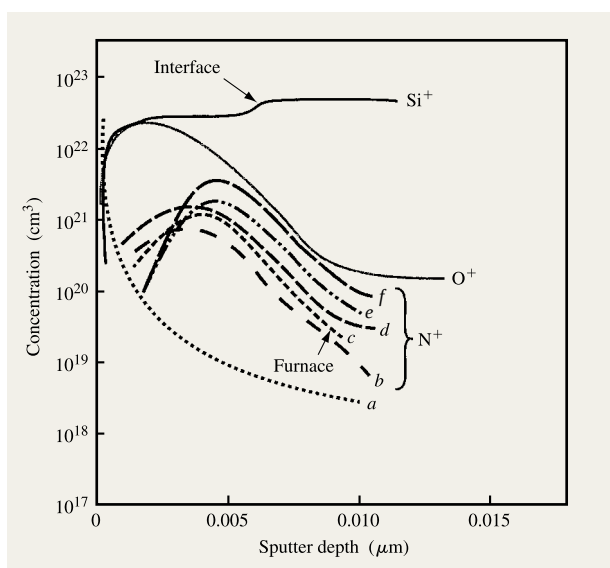


Figure 1

SIMS profiles of nitrogen, oxygen, and silicon concentration for some of the wafers in Table 1. The detected species are $^{133}\text{CsX}^+$, where X is Si, O, or N, and are designated in the figure as Si^+ , O^+ , and N^+ . The integrated nitrogen concentration and the peak nitrogen concentration are tabulated from these data in Table 2. The labels on the curves correspond to the entries in Table 2. The N_2O -nitridized samples (curves b–d) have a larger relative bulk incorporation than the NO-nitridized wafers (curves e, f).

conditions were individually optimized for controllability and uniformity for each experimental cell.

Secondary ion mass spectrometry (SIMS) was performed with a Cameca IMS4F spectrometer. The boron profiles were acquired with 8-keV O_2^+ primary ions and B^+ secondary ions. To obtain good depth resolution across the 7.0-nm oxide and minimize SIMS matrix effects in the nitrogen analysis, 3-keV Cs^+ primary ions were used and CsN^+ secondary ions were detected. After the electrical measurements were completed, a wafer from each of the experimental variations was stripped by extended immersion in hydrofluoric acid. This process removes all of the metallurgy and insulators, leaving only the gate polysilicon over the gate oxide on the wafer. The remaining polysilicon is quite rough, having been partially consumed by the formation of titanium silicide during the fabrication of the wafers. The roughness reduces the depth resolution that may be obtained from SIMS analysis, but using fully processed wafers has the advantage of correlating SIMS data on the very same wafers from which the electrical measurements were obtained. **Figure 1** shows the SIMS profiles for the various permutations of the RTO processing, as well as for the standard furnace process. Two parameters were extracted from each of

these plots. The total integrated nitrogen concentration (in cm^{-2}) was obtained by integrating the SIMS signal from the surface to the bulk. The peak concentration (in cm^{-3}) was also abstracted from the data and summarized in **Table 2**.

The amount and location of nitrogen incorporated in the oxide is a function of the oxidation sequence, the processing temperature, and the gas species used. Oxidation in nitrogen-rich gases not only incorporates nitrogen into the film as it grows, but also removes nitrogen from the bulk of the oxide [32, 33]. The standard furnace process and RTO variations e and f have an initial oxide grown in oxygen, followed by a nitridation step. This results in a peak nitrogen concentration at or near the silicon–silicon dioxide interface, with relatively little nitrogen in the bulk. The furnace N_2O -nitridized sample (curve c) has more nitrogen in the bulk of the oxide than the RTO NO-nitridized sample (curves e and f). Process variations b and d were completely oxidized in nitrous oxide. Although the peak nitrogen concentration still occurs near the interface, there is more incorporation in the bulk of the oxide than in the sample with an initial oxide. The sample run without any nitrogen is shown in curve a; the apparent presence of nitrogen near the top surface in this sample is an artifact of the SIMS measurement.

In the following sections, changes to the device characteristics and reliability for these various oxidation processes are examined. Device design considerations (fixed charge, dopant distribution, and carrier mobility) for n-FETs and p-FETs are first described. The effect on reliability parameters (hot-electron shift, Q_{BD} , and NBTI) is then discussed. Generally, the data points presented in the figures represent an average value obtained from 15 to 20 individual chips on each of two to three similarly processed wafers.

Device design

• Threshold voltage (V_t) and short-channel effects

It is known that nitridation introduces fixed positive charge into the oxide [28, 29]. The effect of the nitridation-induced fixed positive charge is readily observed in the p-FET. Although the nitridation schemes listed in Table 1 have varying thermal cycles, they have little effect on the antimony profile; therefore, the threshold voltage is only a function of the nitridation-induced fixed charge [28]. On the other hand, the boron profile in the n-FET is significantly altered by the heat applied during the nitridation; thus, the threshold voltage is a function of both the fixed charge and dopant redistribution.

We have observed that the p-FET threshold voltage varies with the amount of nitrogen in the oxide across all of the process variations investigated. Previously [28], we reported a one-to-one correlation between p-FET threshold voltage and n-FET hot-electron immunity; in this work we extend this correlation to additional process variations and also introduce SIMS data to directly relate nitrogen concentration in the gate oxide to the p-FET threshold voltage. **Figure 2** shows data from [28] with additional data points (asterisks). The new data points reinforce the correlation and extend the data to a wider range of p-FET threshold voltage variation. Reading from left to right, the new data points are RTO processing variations *a*, *b*, *d*–*f*, as indicated in Table 1.

Using the data presented in Table 2, we have correlated the p-FET threshold voltage directly with the measured nitrogen in the oxide. **Figure 3(a)** shows p-FET threshold voltage as a function of the interfacial and the integrated nitrogen concentration. The p-FET V_t is clearly related to the nitrogen content of the oxide as measured by SIMS. **Figure 3(b)** shows the n-FET threshold voltage on the same wafers as a function of the integrated and peak nitrogen concentrations. In this case, factors other than fixed positive charge must contribute to establishing the threshold voltage. The n-FET threshold voltage is a more complex function of the dopant redistribution, the fixed charge, and the interface trap density. If the same fixed positive charge were present in the n-FET as in the p-FET, the threshold voltage would follow the slope of the dotted-line curve superimposed on the data in Figure 3(b). The threshold voltage is always lower than expected, even for points *a* and *b*, which have less nitrogen and fixed charge than point *c*. This behavior may be explained by considering the boron doping profile beneath the dielectric. As described above, the n-FET well in this technology is retrograde; that is, the center of the dopant implant is located far beneath the surface. Boron diffuses to the surface to establish the threshold voltage, leaving a substantial concentration beneath the surface to arrest

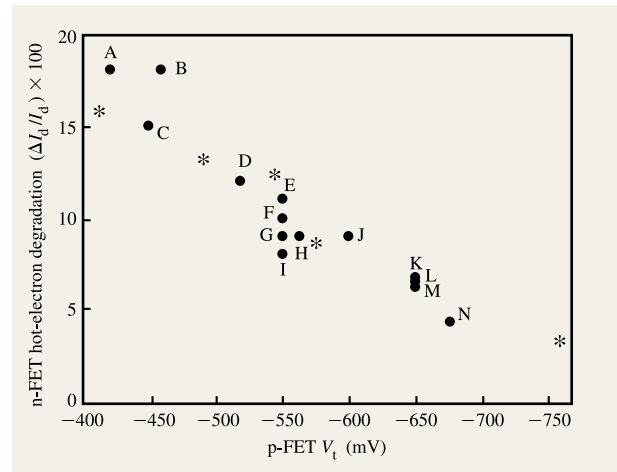


Figure 2

n-FET hot-electron shift (percentage of drain current degradation, normalized for substrate current) as a function of p-FET threshold voltage (normalized for oxide thickness). Process conditions associated with each of the points are given in Table 1. (Adapted with permission from [28]; © 1997 IEEE.)

the short-channel effect. For larger thermal cycles there is more dopant spreading and the surface dopant concentration grows, increasing the threshold voltage. Conversely, for a reduced thermal cycle, there is little diffusion of the boron toward the surface, reducing the threshold voltage. Points *a* and *b* have lower threshold voltage than point *c* because the dopant diffusion during the RTO step is less than that of the standard 950°C N₂O oxidation, and therefore the surface doping is less. The same effect has been observed with other variants to the oxidation process with lower-temperature processing than the standard process, even with similar nitrogen incorporation. By increasing the pressure during oxidation in nitrous oxide, nitrogen may be readily incorporated in the dielectric, even at only 800°C (high-pressure variants C

Table 2 Summary of SIMS data for RTO experiments. The labels appear in Figures 1, 3, 6, 8–14.

Process	Label	Oxidation conditions	Integrated nitrogen concentration (cm ⁻²)	Peak nitrogen concentration (cm ⁻³)
RTO	<i>a</i>	O ₂ 1050°C 60 s	$<3 \times 10^{13}$	0
	<i>b</i>	N ₂ O/O ₂ 1050°C 104 s	3.1×10^{14}	8.0×10^{20}
	<i>d</i>	N ₂ O 1050°C 260 s	6.3×10^{14}	1.5×10^{21}
	<i>e</i>	O ₂ 1050°C 56 s + NO 1000°C 20 s	5.7×10^{14}	2.0×10^{21}
	<i>f</i>	O ₂ 1050°C 51 s + NO 1000°C 120 s	1.1×10^{15}	3.0×10^{21}
Standard furnace	<i>c</i>	O ₂ /H ₂ O 800°C + N ₂ O/N ₂ 950°C	3.9×10^{14}	1.0×10^{21}

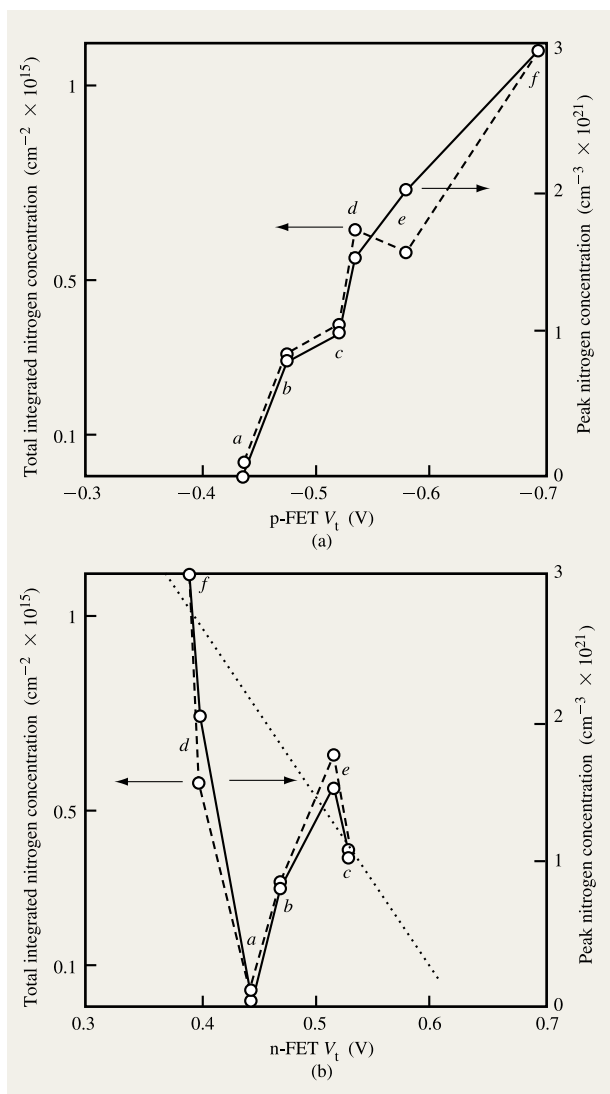


Figure 3

(a) p-FET threshold voltage plotted against both the peak and integrated nitrogen concentration as obtained from SIMS profiles in Figure 2 and tabulated in Table 2. The solid line refers to the interfacial nitrogen concentration and the dashed line to the total integrated concentration. The labels *a–f* are identified with the corresponding nitridation experiment in Table 2. (b) n-FET threshold voltage plotted against both the peak and integrated concentration of nitrogen as obtained from SIMS profiles. The dashed line refers to the total integrated nitrogen concentration, and the solid line to the interfacial concentration. The process conditions associated with the data at points *a–f* are specified in Table 2. The dotted line is the curve that would be expected if the n-FET behavior were determined only by fixed positive charge.

and D from Table 1). Data for p-FET V_t fall on the “universal” curve in Figure 2, but the n-FET V_t does not correlate directly with the fixed charge. All high-pressure-oxidation wafers have a lower threshold voltage by

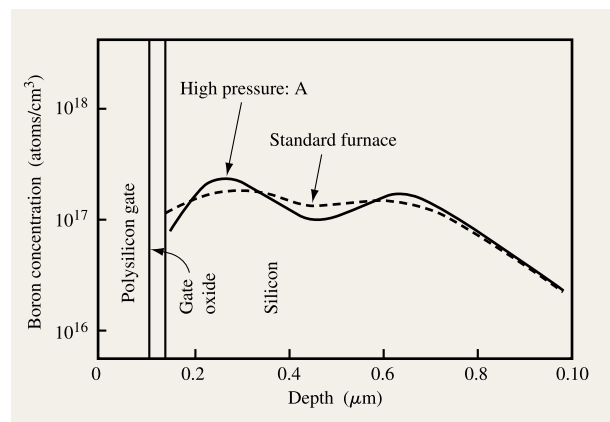


Figure 4

SIMS profiles of boron well doping for two different oxidation conditions. The boron is more evenly distributed in the standard furnace process because of the higher thermal cycle and the accompanying dopant diffusion. The concentration of boron is higher at the surface in that process, and therefore the threshold voltage is larger.

100–150 mV compared to other wafers processed in the same lot. For these wafers, the change in the n-FET threshold voltage is dominated by the difference in thermal budget between the standard furnace process and that used at elevated pressure. SIMS profiles of the boron well for two of the processes are shown in **Figure 4**. The standard process spreads the dopant significantly, particularly during the 950°C nitridation step. The high-pressure oxidation, although incorporating a similar amount of nitrogen, results in a much steeper doping profile, both in the near-surface implant and in the deep implant. It is apparent from the figure that the doping at the surface is lower; this results in a lower threshold voltage.

Another effect of reduced dopant spreading is evident in the inverse short-channel effect (ISCE); **Figure 5** shows the n-FET saturated threshold voltage as a function of inverse channel length for the standard furnace process and high-pressure variants as described in Table 1. All of the high-pressure oxidation wafers show an increase of threshold voltage at shorter channels (ISCE) before the threshold decreases owing to the short-channel effect (SCE). The threshold voltage for the standard furnace process decreases monotonically as the channel becomes shorter. ISCE is found in devices designed with a halo, or pocket, implant [44–47]. The additional p-type doping surrounding the drain region becomes more significant for shorter channels, causing the threshold to increase before it decreases at even shorter channels. There is no halo

implant in these devices; therefore, the ISCE is caused by flattening of the dopant profile near the source/drain regions, increasing the threshold voltage in a manner similar to that described above for increased processing temperatures. Flattening of the well profile near the source/drain is possible only if it is not already flattened by diffusion during gate oxidation. Therefore, the more retrograde the well profile, the greater the degree of ISCE. In accordance with expectation, wafers with steeper doping gradient, as in Figure 4, show greater ISCE, as in Figure 5.

Although the p-FET polysilicon gate is doped with boron, penetration of boron through the oxide does not affect the p-FET threshold voltage. The only major thermal cycle following the introduction of boron into the polysilicon gate is a single 1000°C (average) RTA. In an experiment in which the temperature of this anneal was altered, little change in the p-FET threshold voltage was found. **Table 3** presents these results. The change for the n-FET threshold voltage was almost identical to that of the p-FET, and may be attributed to the elimination of fixed charge associated with post-oxidation annealing [22]. If boron penetration were important in determining the p-FET threshold voltage, a higher-temperature anneal would drive more boron through the oxide and alter the threshold voltage of the p-FET independently of the n-FET. The results given in Table 3 show little dependence of the threshold voltage on the anneal, and equivalent behavior of the p-FET and the n-FET.

The quality of the silicon-silicon dioxide also contributes to the threshold voltage. As it is known that nitridized oxides can have a higher interface trap density than conventional oxide, the contribution of this component should be determined [31]. In the presence of interface traps, the threshold voltage is increased in magnitude to reflect the density of charge required to populate the traps. Another manifestation of the interface trap density is in the subthreshold slope, which is the gate-voltage dependence of the drain-source current when the gate voltage is below threshold. A typical value of this parameter at room temperature is 80–85 mV/decade; that is, the drain-source current is reduced by a factor of 10 for every 80–85 mV change in gate voltage. A larger subthreshold slope is indicative of a larger interface trap density. Therefore, a larger drain-source current for a given voltage less than the threshold voltage is a direct measure of the subthreshold slope, and therefore the interface trap density. The vertical axis of **Figure 6(a)** is the drain-source current for a short-channel p-FET device with the gate-source voltage at zero, the abscissa is the measured threshold voltage, and the slope of the curve is the subthreshold slope. A line at 80 mV/decade is drawn on the plot as a guide to the eye. Each point represents an individual chip, and the various symbols correspond to

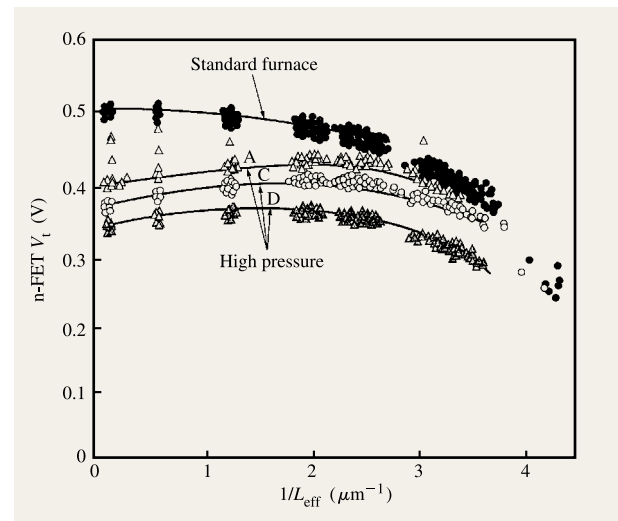


Figure 5

n-FET saturated threshold voltage as a function of the inverse of the effective channel length for various methods of oxidation. The various processes are described in Table 1. Solid circles: standard furnace process; open triangles: high pressure (A); open circles: high pressure (C); solid triangles: high pressure (D).

Table 3 Threshold voltage results of dopant activation annealing experiment (p-FET dopant: B; n-FET dopant: P).

Annealing temperature (peak) (°C)	V_t	
	p-FET	n-FET
1068	−538	527
1075	−534	532
1085	−532	536
1092	−528	541

the RTO variations from Table 2. The wafers with the highest nitrogen concentration (those to the right-hand side of the plot) show degraded subthreshold characteristics, indicative of additional interface trap density in the lower half of the silicon bandgap.

A correlation of nitrogen content to interface trap concentration has been reported elsewhere [31]. However, the threshold voltage is relatively unaffected for all but the wafers with the highest nitrogen concentration. If it were not for the increased interface trap density, the threshold voltage of these wafers would have been slightly more positive. The threshold voltage at point *f* in Figure 3(a) would have been less negative if it were not for the additional interface trap density.

Figure 6(b) shows the subthreshold slope of the n-FET; this is entirely analogous to Figure 6(a) for the p-FET.

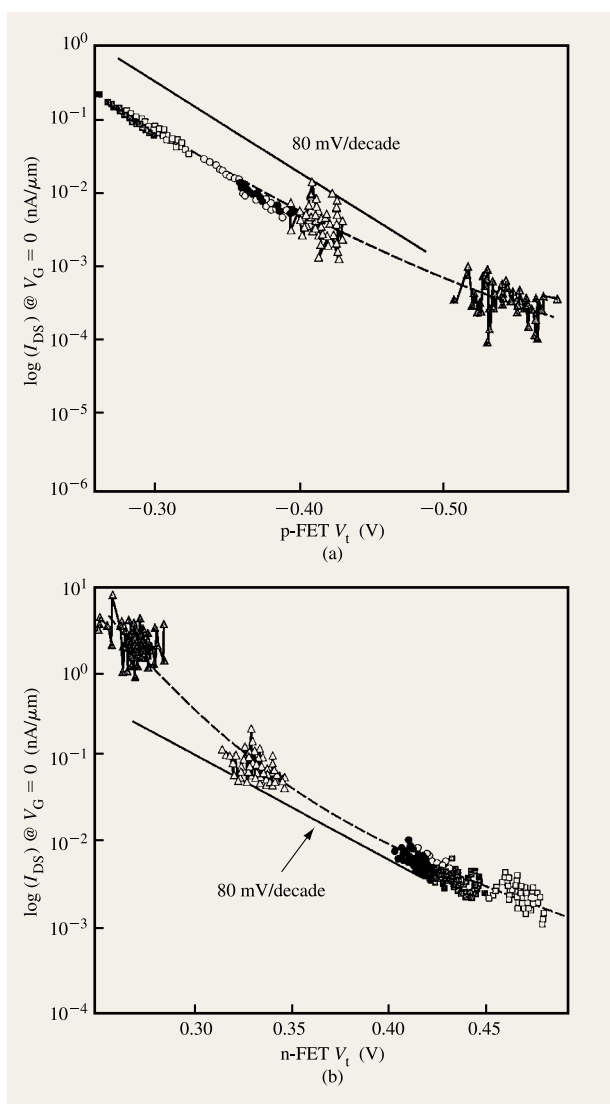


Figure 6

Drain-source current for zero gate-source voltage plotted as a function of saturated threshold voltage: (a) p-FET ($V_{DS} = -3.3$ V) and (b) n-FET ($V_{DS} = 3.3$ V). A device with an ideal silicon-silicon dioxide interface would follow a curve of 80–85 mV/decade, which is indicated in the figure. The various symbols relate to the oxidations specified in Table 2. Solid triangles: RTO in nitric oxide (f); open squares: RTO in nitric oxide (e); open triangles: RTO in nitrous oxide (d), open circles: RTO in dilute nitrous oxide (b); solid circles: standard furnace nitridation (c); solid squares: RTO in oxygen (a).

Wafers with a perfect interface are expected to see an increase in current of one decade for every 80–85 mV of threshold reduction. As with the p-FET, a marked deviation from the ideal subthreshold slope is evident in the wafers with the highest nitrogen concentration. The

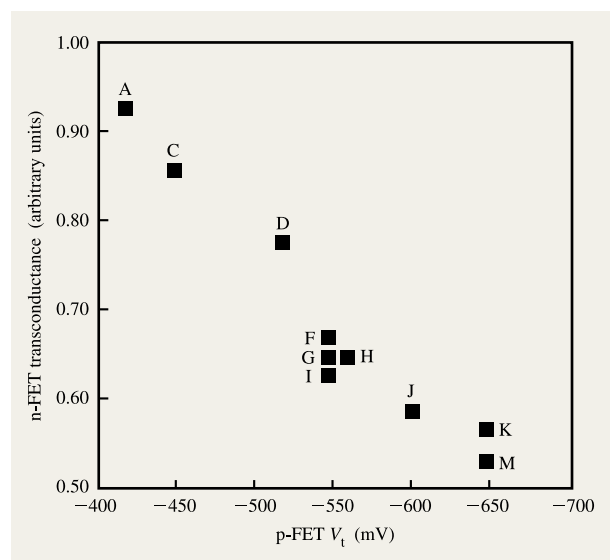


Figure 7

n-FET linear transconductance (normalized for oxide thickness) plotted against p-FET threshold voltage for various oxidation methods. Most of the variations specified in Table 1 and Figure 1 are included.

increased interface trap density increases the threshold voltage; the threshold voltage for the wafers of point f in Figure 3(b) would have been smaller in the absence of the additional interface traps.

To summarize, the p-FET threshold voltage is a relatively straightforward function of the fixed positive charge and, at the highest nitrogen concentration, the interface trap density. The n-FET threshold voltage is a function of the fixed charge, the interface trap density, the total thermal budget applied, and the resulting dopant distribution. In addition, changes in the dopant profile also alter the dependence of the threshold voltage on the channel length, modifying the ISCE.

• Mobility effects

It is well established that nitridation affects the carrier mobilities in the inversion layer [6–8]. **Figure 7** shows the n-FET linear transconductance for the various nitridation processing as a function of the p-FET threshold voltage. The p-FET threshold voltage is used here because it is the most direct measure of the charge in the oxide. Clearly, there is a direct relationship of the fixed positive charge in the p-FET and the electron mobility in the inversion layer of the n-FET. The effective mobility is nearly halved at the very highest nitrogen concentration relative to the base value. Surprisingly [22], no perturbation to the hole mobility was observed.

Overall, the performance of devices with high nitrogen content is not as degraded as the low-field electron mobility degradation might imply. **Figure 8** shows the linear drain current versus the saturated drain current for each of the gate oxidation variations in Table 2. The linear drain current is measured with a gate-source voltage of 3.3 V and a drain voltage of 100 mV. In saturated conditions, the gate-source voltage is 3.3 V, and the drain-source voltage is also 3.3 V. A straight line sketched in the figure represents equal fractional change in the linear and saturated currents. This relationship is approximately followed by chips with the same gate-oxide process, but for wafers of varying nitrogen concentration, the change in saturated current is less than that of the linear current. This is because the low-field mobility is degraded, while the high-field mobility degrades less or even increases with increasing nitrogen concentration [30]. Therefore, although the linear current is halved by the addition of a large amount of nitrogen, the saturated current is degraded by a much smaller fraction. Because the performance of many circuits is dominated by saturated current, the overall circuit degradation for nitrided oxide is much less than would be expected from the linear transconductance alone.

To summarize the device design considerations, we have found that the primary effect of nitridized oxide in the p-FET is on the threshold voltage, and that this is effectively predicted from the fixed charge alone. No significant change in dopant profile was found. For the p-FET, antimony is implanted as the well-dopant species; different effects may be found with arsenic or phosphorus. We have found no effect on the hole mobility, so the only degradation to the device performance is in the accommodation that must be made in the well doping to achieve the proper threshold voltage. With a nitrided oxide, less doping must be used to achieve a given threshold voltage, and this may limit the ability of the device to achieve very short channels. When boron is used as the well dopant for the n-FET, the dopant redistribution during the gate oxidation/nitridation step must be taken into account to predict the threshold voltage. The fixed charge and the interface trap density also play a role, but the dopant diffusion dominates the device behavior. As the profile is changed by the dielectric process, the short-channel effect is also changed. A low-thermal-budget process with a steeply retrograde well profile will have threshold roll-up, or ISCE. For the n-FET, boron is used for the well doping; different effects might be found for indium. There is a substantial decrease in transconductance with heavy nitridation, but there is less degradation in saturated current than in linear current.

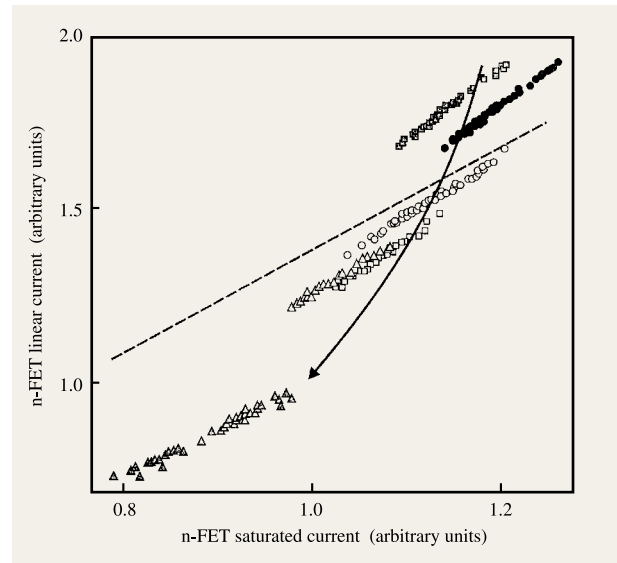


Figure 8

n-FET linear current vs. n-FET saturated current for various oxidation methods incorporating varying amounts of nitrogen. The various symbols relate to the oxidations specified in Table 2. Solid triangles: RTO in nitric oxide (*f*); open squares: RTO in nitric oxide (*e*); open triangles: RTO in nitrous oxide (*d*); open circles: RTO in dilute nitrous oxide (*b*); solid circles: standard furnace nitridation (*c*); solid squares in oxygen (*a*). The dotted line represents equal fractional change of current on both axes, and the solid line schematically indicates wafers of increasing nitrogen content. Linear current is measured at large gate-source potential but at small drain bias. Saturated current is measured at large drain-source potential as well as large gate-source voltage. For convenience, the data have been normalized to an arbitrary value.

Reliability

• n-FET hot-electron shift

The hot-electron shift for the n-FET device is illustrated in Figure 2 for all of the experimental wafers. The percentage of degradation in drain current after a short stress at maximum substrate current is plotted as the ordinate. The response to hot-electron stress is a monotonic function of the amount of nitrogen at the silicon-silicon dioxide interface, regardless of the method by which the nitrogen was introduced. For further illustrative purposes, the hot-electron shift (percentage of drain-current change) is shown as a function of the substrate current for the various RTO variants in **Figure 9**. The substrate current is generally well correlated with the hot-electron shift [48]. The substrate current increases for shorter channels and for devices with higher electric field at the drain. The substrate current is the result of the production of electron-hole pairs at the drain from

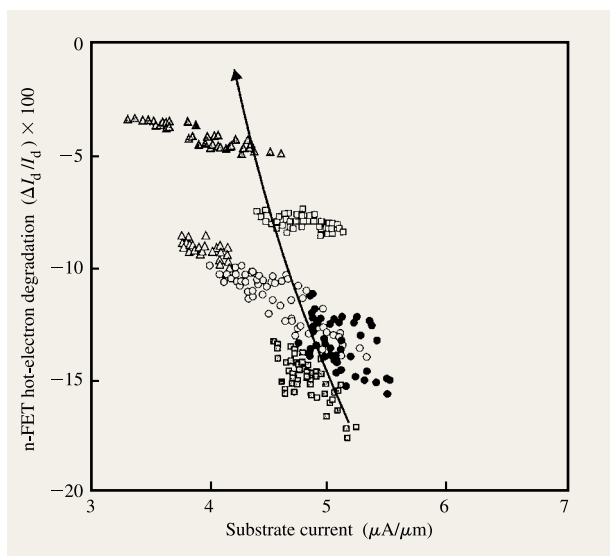


Figure 9

n-FET hot-carrier-induced drain current degradation (%) as a function of substrate current for various oxidation processes as described in Table 2. Solid triangles: RTO in nitric oxide (*f*); open squares: RTO in nitric oxide (*e*); open triangles: RTO in nitrous oxide (*d*); open circles: RTO in dilute nitrous oxide (*b*); solid circles: standard furnace nitridation (*c*); solid squares: RTO in oxygen (*a*). The solid line schematically indicates wafers of increasing nitrogen content.

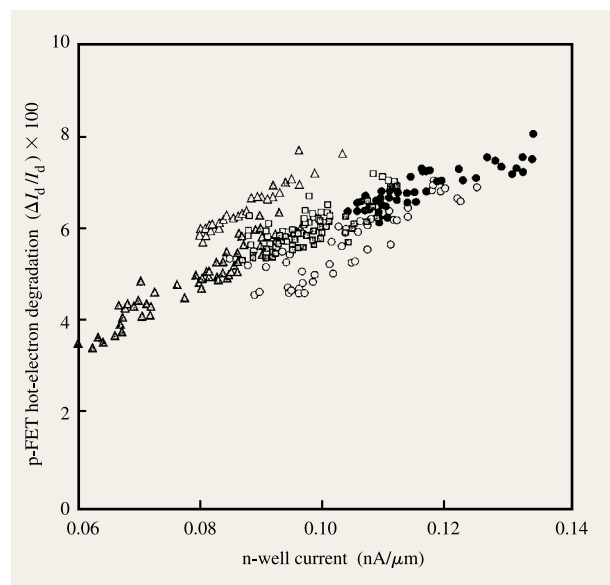


Figure 10

p-FET hot-carrier-induced drain current degradation (%) as a function of well current for various oxidation processes, as described in Table 2. Solid triangles: RTO in nitric oxide (*f*); open squares: RTO in nitric oxide (*e*); open triangles: RTO in nitrous oxide (*d*); open circles: RTO in dilute nitrous oxide (*b*); solid circles: standard furnace nitridation (*c*); solid squares: RTO in oxygen (*a*).

energetic electrons heated in the drain field. In addition to the created holes that appear as part of the substrate current, the hot electrons also affect the silicon-silicon dioxide interface. The hot electrons may become trapped or may damage the interface by creating interface traps that shift the threshold voltage and degrade the electron mobility. The incorporation of nitrogen in the dielectric makes the interface more robust with respect to damage [18–20]. In Figure 9 it is apparent that for the same substrate current, the wafers with more nitrogen have less hot-electron shift; and Figure 2 suggests that the hot-electron improvement is directly tied to the interfacial nitrogen and hence to the p-FET threshold voltage. From a device design perspective, the improved immunity to hot-electron degradation may be utilized in one of several ways: The channel length of the device may be shortened, keeping the same shift; the drain may be engineered for a higher electric field while maintaining the same shift; or a superior reliability may be offered to relieve circuit design restrictions.

- *p-FET hot-electron shift*

The shift in drain current and threshold voltage in n-FETs under hot-electron stress is caused by the creation of

interface traps and trapping of electrons in the oxide bulk [48]. It is possible for both of these mechanisms to occur in p-FETs as well [49, 50]. Under peak gate-current bias conditions, the shift in these devices is dominated by electron trapping in the oxide. A large drain-source voltage is applied, and only a moderate gate-source voltage. Under these conditions the gate potential is negative enough for a large drain-source current, but still more positive than the drain, so as to not repel electrons from traversing the gate oxide. **Figure 10** shows the percentage of shift in drain current for p-FETs. The shift is plotted against the n-well current, since, as in the n-FET and its substrate current, a higher well current indicates a larger shift, simply by virtue of indicating a larger generation of hot carriers. In Figure 10 all RTO wafers have virtually the same shift; the furnace-oxidized cell is slightly inferior to the RTO group, and of these, the N₂O is marginally superior. Essentially, hot-electron shift dependence on the nitrogen incorporation is not observed for the p-FET.

- *Charge to breakdown*

The intrinsic dielectric reliability of the oxides described in Table 2 was determined by applying an elevated voltage

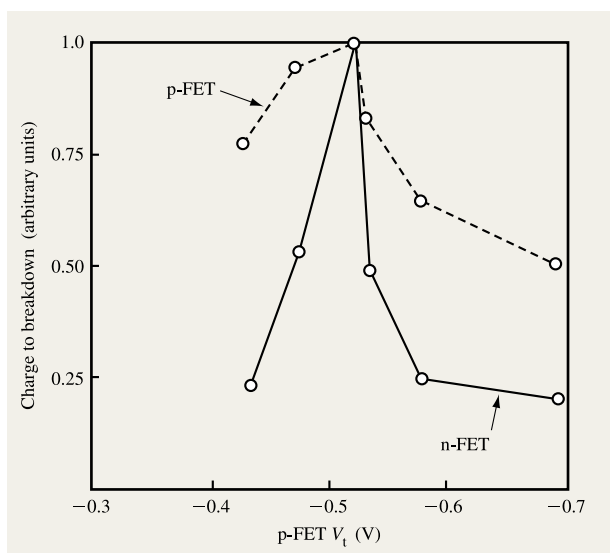


Figure 11

Charge to breakdown (p-FET + n-FET) as a function of p-FET threshold voltage. The data points correspond to the entries in Table 2, ranging in nitrogen concentration from left to right.

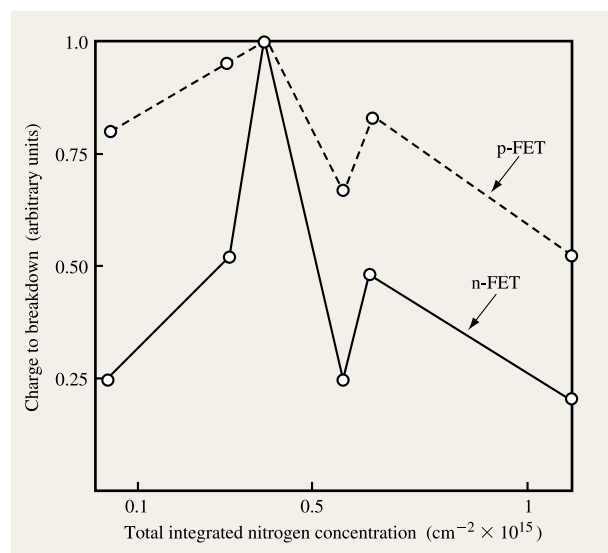


Figure 12

Charge to breakdown (p-FET + n-FET) as a function of total integrated nitrogen concentration. The data correspond to the entries in Table 2.

at an elevated temperature to capacitor structures until dielectric failure was noted. All stressing was performed with the silicon surface in inversion, and both p-FETs and n-FETs were measured. Constant voltage stressing was performed, and the current was measured during the stress. At the completion of the stress (it typically took 20–200 seconds for the capacitors to fail at 9–9.5 V), the total charge that had flowed was calculated and tabulated. The charge for which 50% of the capacitors failed is presented here as Q_{BD} . **Figure 11** shows the Q_{BD} for both n-FET and p-FET as a function of the p-FET threshold voltage, which is used because it is a measure of the oxide charge. In **Figure 12** we have used the SIMS data from Table 2, and plotted the same data points as a function of the integrated nitrogen concentration. In **Figure 13** the same Q_{BD} data are plotted against the peak nitrogen concentration from Table 2. The Q_{BD} is improved by adding some nitrogen, but further nitridation caused the charge to breakdown to degrade in both n-FETs and p-FETs. A peak nitrogen concentration in excess of $1.0 \times 10^{21} \text{ cm}^{-2}$ degrades the charge to breakdown. In these devices the poorest Q_{BD} is obtained from wafers processed with nitric oxide. The best wafers were processed with nitrous oxide.

• NBTI

Negative-bias temperature stressing was performed at elevated temperature and voltage. In this type of stressing, a negative bias of the order of 5 V is applied to the gate

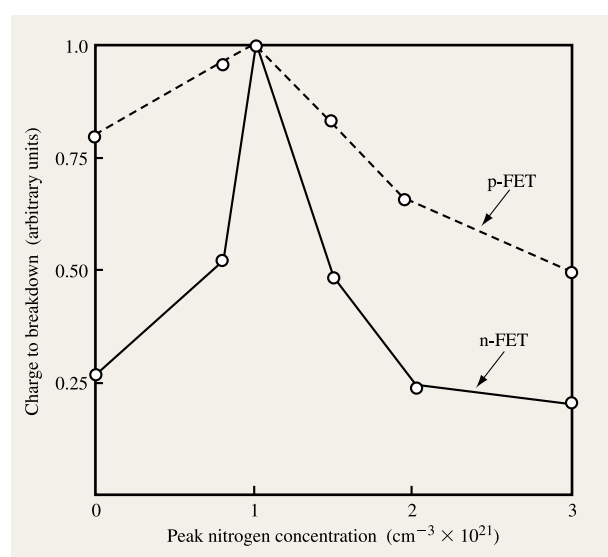


Figure 13

Charge-to-breakdown (p-FET + n-FET) as a function of peak nitrogen concentration. The points correspond to the entries in Table 2.

of a p-FET while holding the drain, source, and well at ground potential. Devices are stressed for 2–5 hr

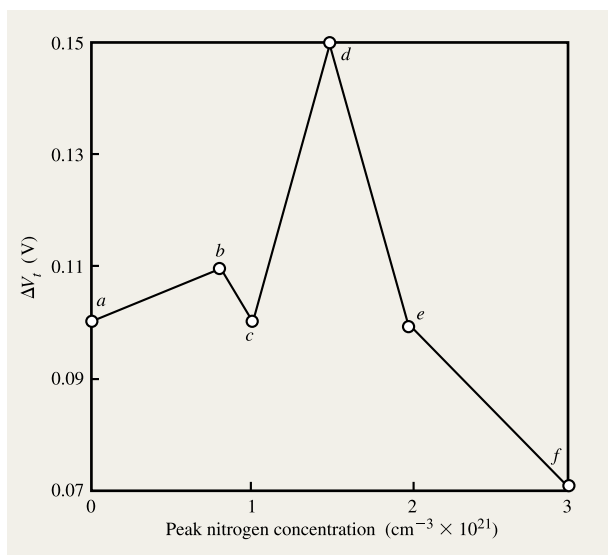


Figure 14

Shift in threshold voltage after NBTI stress as a function of peak nitrogen concentration. The points correspond to the entries in Table 2.

under these conditions. Stressing in this mode induces a threshold-voltage shift through the creation of fixed positive charge and interface traps [41–43]. **Figure 14** plots the threshold-voltage shift (normalized for t_{ox}) against the nitrogen concentration as derived from the SIMS analysis. The NBTI shift is largest at an intermediate nitrogen concentration. The degraded NBTI behavior of point *d* in Figure 14 is consistent with another experiment in which the NBTI shift in undiluted nitrous oxide-oxidized samples (points K and L from Table 1 and Figure 2) was measured to be one and one-half times as large as standard diluted N_2O samples (points E–H from Table 1 and Figure 2). It is unfortunate that the best Q_{BD} (as in Figure 13) is found at an intermediate nitrogen concentration, for which the NBTI threshold shift was the largest.

To summarize the reliability data, we have found that the improvement in n-FET hot-electron shift is directly related to the interfacial nitrogen concentration. Since the p-FET hot-electron shift is nearly unchanged by the oxidation/nitridation experiments, there appears to be no change in the trapping of electrons in the bulk oxide. The intrinsic charge to breakdown is significantly altered by the experiments, with the best Q_{BD} found at intermediate nitrogen concentration. In contrast, the NBTI threshold voltage shift is found to be worst in the wafers with intermediate nitrogen concentration.

Summary

We have examined the effects of nitrogen in the gate dielectric and various methods of its introduction on the reliability and device characteristics for a particular device design. The effects across a large range of nitrogen incorporation (from 0 to 10% of the interfacial bonds) have been studied. Data on device design and reliability across this wide range of nitrogen incorporation have been presented.

Some effects are common to all means of nitridation. Nitrogen increases the surface charge, so the well dopants must be modified to readjust the threshold voltage and maintain useful currents. The n-FET is affected by the different heat cycles that may be used to introduce the nitrogen. The optimum degree and method of nitridation will vary for different technologies, depending on the specific design goals. For instance, a steeply retrograde well design requires a low-thermal-budget process such as high-pressure oxidation or RTO, while a device design that is best satisfied by a flat well profile may utilize the simpler conventional furnace process.

The n-FET hot-electron reliability is very much improved by the interfacial nitrogen, but the p-FET electron trapping is unaffected. The dielectric integrity is improved by adding nitrogen to the interface, but not too much. The NBTI is degraded by the initial addition of nitrogen, but then improves as more is added.

A practical compromise to the trade-offs involved in a nitrided-gate oxide has been given. The standard process as described in Table 1 achieves the desired design goals of adequate hot-electron reliability with minimal cost and complexity. In addition, we have tried to show some fundamental aspects of nitrided oxides and their relationship with the device design. Improvements in hot-electron immunity appear to be invariably accompanied by increased fixed charge and degraded mobility. Data have also been presented that indicate a complex interaction of nitrogen in the classic oxide degradation mechanisms of time-dependent dielectric breakdown and NBTI.

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