

Polymer self assembly in semiconductor microelectronics

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We are inspired by the beauty and simplicity of self-organizing materials and the promise they hold for enabling continued improvements in semiconductor technology. Self assembly is the spontaneous arrangement of individual elements into regular patterns; under suitable conditions, certain materials self organize into useful nanometer-scale patterns of importance to high-performance microelectronics applications. Polymer self assembly is a nontraditional approach to patterning integrated circuit elements at dimensions and densities inaccessible to traditional lithography methods. We review here our efforts in IBM to develop and integrate self-assembly processes as high-resolution patterning alternatives and to demonstrate targeted applications in semiconductor device fabrication. We also provide a framework for understanding key requirements for the adoption of polymer self-assembly processes into semiconductor technology, as well as a discussion of the ultimate dimensional scalability of the technique.

Introduction

The challenge of lithographically defining the elements of semiconductor integrated circuits (ICs) at dimensions smaller than 100 nm has created opportunities for alternative patterning approaches. One attractive nontraditional approach uses the phenomenon of *self assembly*, which is the spontaneous organization of materials into regular patterns without human intervention [1].

Block copolymer films are similar to conventional polymer photoresist patterning materials used in semiconductor fabrication in that they are suitable for forming a well-defined latent image. Unlike photoresists, however, block copolymers can autonomously form regular patterns at dimensions not achievable by lithographic means. They are a particularly attractive choice for semiconductor patterning applications because, like photoresists used for conventional patterning, they can act as sacrificial templates for defining integrated circuit elements [2–10]. The idea of using block copolymer thin films as lithographic masks was first proposed in 1995 [11], and the first experimental demonstrations used polystyrene-*b*-polybutadiene (PS-*b*-PB) block copolymer materials [12]. The initial

implementation of a “block copolymer lithography” process utilized self-assembled nanometer-scale patterns as both positive and negative resists for etching underlying substrates of Si, Si₃N₄, and Ge [13].

As we will see, polymer self assembly can define only a limited set of pattern geometries. However, within these constraints the materials provide a straightforward means for achieving feature sizes (<20 nm), pitches (<40 nm), and densities ($\sim 10^{11}/\text{cm}^2$) that are currently not achievable by optical lithography. We have successfully integrated a polymer self-assembly process into a 200-mm semiconductor fabrication facility at the IBM Thomas J. Watson Research Center in Yorktown Heights, New York; this paper summarizes aspects of our program in IBM that target self assembly as an enabler for advances in semiconductor technology.

Diblock copolymer phases

Diblock copolymer materials spontaneously form patterns through a minimization of free energy—a process known as *microphase separation* [14]. The immiscibility of the two chemically distinct “blocks” that comprise each polymer molecule drives the system toward a minimum interaction volume, while the covalent bond

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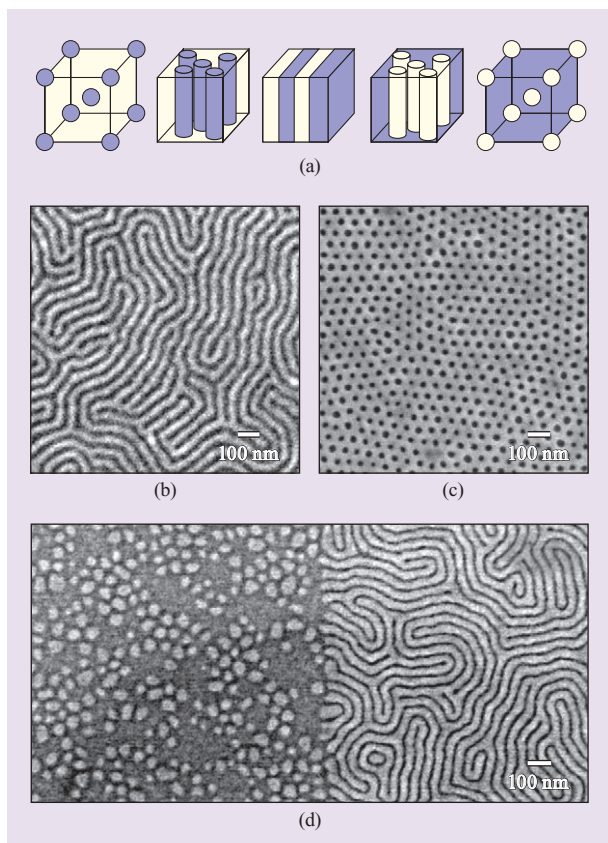


Figure 1

(a) Schematic representation of five diblock copolymer phases. Left to right: spherical, cylindrical, lamellar, inverse-cylindrical, inverse-spherical phases. (b) Surface-parallel-oriented and (c) surface-perpendicular-oriented cylindrical phase PS-b-PMMA diblock copolymer patterns. PMMA domains are dark and PS regions are light colored. (d) Left side of image shows surface-parallel-oriented lamellae; right side shows surface-perpendicular-oriented lamellae. Note that parallel cylindrical phases (b) and perpendicular lamellar phases (d) each form striped line/space patterns. (Republished from [16] with permission. ©2004 SPIE.)

between these blocks simultaneously limits the maximum distance by which the two blocks can separate. The resulting equilibrium patterns have molecular-scale dimensions determined by the intrinsic polymer properties of the degree of polymerization (N) (proportional to the polymer molecular weight), the weight ratio of the constituent blocks, and the Flory-Huggins parameter (χ), which characterizes the interaction strength of the blocks. We have integrated diblock copolymers composed of polystyrene (PS) and polymethylmethacrylate (PMMA), referred to as *PS-b-PMMA*, with total molecular weight M_n in the range of $\sim 60,000$ g/mol and polydispersity (PD) of ~ 1.1 . These materials typically produce patterns with critical dimensions in the range of 15–20 nm. We

chose to integrate PS-b-PMMA because of its material compatibility with the semiconductor fabrication infrastructure as well as the significant body of research on understanding its material properties (e.g., [15]). While our discussion focuses largely on PS-b-PMMA materials, many other block copolymer choices are possible and may ultimately prove better suited for use in IC fabrication.

The patterns generated by a self-assembling diblock copolymer film (as shown in **Figure 1**) depend on the relative mass ratio of the two blocks comprising each copolymer molecule [14]. For highly asymmetric diblock copolymers (ratios above $\sim 80:20$), patterns consist of close-packed zero-dimensional spheres. More symmetric materials ($\sim 70:30$) form one-dimensional close-packed cylinder patterns, and symmetric block copolymers ($50:50$) create alternating two-dimensional lamellae. The diblock copolymer compositional phase space is roughly symmetric, with inverse cylinders and inverse spheres possible for molecules of the associated complementary composition [14]. More exotic phases such as a bi-continuous gyroid phase form at compositional boundaries; however, patterning applications of these intricate geometries are beyond the scope of our discussion. The cylindrical and perpendicular lamellar patterns shown in Figure 1 most closely resemble a conventional lithographic photoresist profile because nanometer-scale domains run continuously from top to bottom through the entire polymer film thickness. We focus much of our discussion on applications of these two pattern types.

The process of forming self-assembled patterns from PS-b-PMMA diblock copolymers involves the deposition of a thin film, typically by spin-casting the polymer from a dilute solution to an appropriate film thickness, followed by thermal annealing above the polymer glass transition temperature [15, 17]. Typical annealing conditions are $\sim 200^\circ\text{C}$ (in vacuum or N_2) for times ranging between 30 minutes and 24 hours, depending on the application. The quality of the resulting self-assembled pattern depends on all of the process conditions (film thickness, annealing time, and annealing temperature) [17]. After pattern formation, we chemically remove the PMMA block by optional exposure to UV light [17, 18] and then immersion in an acetic acid developer [15]. An appealing aspect of the self-assembly process is its similarity to a conventional lithographic process, with steps of film casting, image formation (by self assembly rather than lithographic exposure through a mask), and chemical development.

Controlling self-assembled pattern orientation

For lithography applications of these materials, we must also control the *orientation* of the self-assembled pattern

with respect to the underlying substrate surface. While the self-assembly process is driven by microphase separation of the constituent copolymer blocks, the ultimate pattern orientation is determined by the relative strength of the surface affinity of each block. Control of domain orientation has been demonstrated by coupling the self-assembly process with an external bias via a mechanical flow field [19], directional casting [20, 21], electric field [22, 23] thermal field [24], and controlled surface interactions [15, 25–27].

In our work we have utilized a surface modification layer for controlling pattern orientation because of the relatively straightforward pathway to semiconductor process integration (compared with the other biasing methods described above) [15, 25–27]. For PS-*b*-PMMA diblock copolymers, PMMA is preferentially attracted to a clean silicon dioxide (SiO₂) surface and thus forms a uniform copolymer wetting layer on the substrate [28]. For an asymmetric diblock copolymer with a 30% PMMA minority block, these wetting conditions dictate that cylindrical-phase PS-*b*-PMMA films orient with PMMA cylinders parallel to the substrate. Viewed from the top surface, this film (70:30 PS:PMMA, $M_n = 64,000$ g/mol) is composed of a meandering pattern of 20-nm-diameter-cylindrical PMMA domains with 40-nm pitch [Figure 1(b)]. We typically remove the PMMA block after pattern formation in order to improve the scanning electron microscopy (SEM) image contrast.

We prevent preferential surface wetting of either block by rendering the substrate neutral to PS and PMMA. We neutralize an oxide surface using a PS-*r*-PMMA random copolymer brush [15, 25, 27] prior to diblock copolymer film application and self assembly. Both random copolymer brushes and thermally cross-linked random copolymers are now widely used as surface neutralization layers to promote preferred domain orientation [15, 25–27]. With a random copolymer brush undercoat, the same 70:30 PS-*b*-PMMA polymer orients with cylindrical domains perpendicular to the surface, resulting in a close-packed two-dimensional 20-nm-diameter PMMA cylinder array in a matrix of PS [Figure 1(c)]. A cross-sectional view of the close-packed cylinder pattern resembles that shown schematically in Figure 1(a).

We can similarly control the orientation of lamellar-phase PS-*b*-PMMA patterns. Because PMMA preferentially wets SiO₂, a film of lamellar-phase PS-*b*-PMMA (50:50 PS:PMMA, $M_n = 51,000$ g/mol) orients alternating PS and PMMA sheets parallel to the surface [left side of Figure 1(d)]. (Parallel lamellar thin films often appear with a disordered dot structure when viewed from the top because of surface wetting properties.) The PS-*r*-PMMA random copolymer brush pretreatment causes PS-*b*-PMMA lamellae to orient perpendicularly [27], resulting in a line/space pattern when viewed from the top

[right side of Figure 1(d)]. Note that from a top view, parallel-oriented cylindrical-phase films [Figure 1(b)] and perpendicular-oriented lamellar films [right side of Figure 1(d)] have a similar appearance, although their cross-sectional profiles are quite different [29]. By lithographically patterning chemical inhomogeneity on a surface, it is possible to change the domain orientation within a single polymer layer [30], as demonstrated in Figure 1(d) for PS-*b*-PMMA lamellae oriented surface parallel on the left side and surface perpendicular on the right.

Both the cylinder- and the lamella-forming PS-*b*-PMMA materials shown in Figure 1 spontaneously generate features with sublithographic resolution and pitch. The hole array pattern [Figure 1(c)] has a 20-nm mean critical dimension with 40-nm pitch (the standard deviation, σ , is about 10% of the mean dimensions for both diameter and pitch [17]), and the line/space pattern [Figure 1(d)] has a 37-nm pitch. Throughout this paper, we refer to a characteristic length scale for polymer self assembly, L_0 , which is defined as the pitch of the line/space pattern for lamellar materials or $\sqrt{3}/2$ times the hole-array center-to-center spacing for cylindrical materials. We note here and discuss in more detail in a later section that both self-assembled hole-array patterns and line/space patterns have a reasonable degree of *size* uniformity but lack any significant *positional* uniformity—an important factor when considering suitable target applications for these processes.

Development of processes for pattern transfer

Robust processes for pattern transfer are essential to the development of block copolymer films as patterning materials, and there have been significant advances in deposition and etching methods for pattern replication. The high density of nanometer-scale features provided by self-assembled patterns is well suited to applications in high-density magnetic recording media. For example, high-aspect-ratio magnetic nanowire arrays with density $\sim 10^{12}/\text{cm}^2$ have been fabricated by cobalt electrodeposition into thick PS-*b*-PMMA hole-array templates [31]. Lower-aspect-ratio structures can be formed using a metal lift-off process in which the magnetic material is sputtered into the templates [32]. Alternatively, using the block copolymer template as an etch mask for patterning an underlying magnetic thin film provides the advantage of decoupling thin-film deposition from the pattern transfer so that each process can be independently optimized. This approach requires the use of an intermediate hard-mask layer because of the low etch resistance and limited height of the polymeric template [33, 34]. Similar pattern-transfer techniques have been demonstrated in patterning a variety of thin-film materials including quantum dot arrays and metal dot arrays [35, 36].

Beyond functioning as templates for standard pattern-transfer processes such as material deposition or etching, block copolymer materials can serve as directing agents that guide the deposition of functional materials. Selective adsorption or chemical reaction with one of the block copolymer domains provides a method for coding spatial information into materials at nanometer-length scales. For example, Au and Ag preferentially segregate to the PS domains in PS-*b*-PMMA thin films, while In, Pb, Sn, and Bi migrate to PMMA domains. Under the appropriate metal deposition conditions, it is possible to achieve nearly 100% spatial selectivity [37]. Block copolymer self assembly has also been used to define and position metal catalysts with nanometer-scale precision. In this case, self-assembled patterns formed from polyferrocenyldimethylsilane (PFS) domains in PS-*b*-PFS diblock copolymer thin films were further processed to produce iron dot arrays for catalyzing the growth of carbon nanotubes [38]. The nanotube spatial distribution and diameter can be controlled by adjusting the periodicity and size of the self-assembled polymer pattern.

In our research program at IBM, we have used self-assembled polymer materials to address specific challenges in semiconductor device fabrication. The discussion above has introduced the strengths of this patterning technique (defining sublithographic feature sizes at sublithographic pitch; high feature densities; reasonable size uniformity; semiconductor process compatibility), as well as its weaknesses (limited pattern types; little positional order; low etch resistance). In the following sections we first highlight semiconductor device applications that take advantage of these intrinsic strengths. These examples use self-assembled patterns as a method for controlling material nanostructuring at sublithographic dimensions. Subsequent discussions emphasize the weaknesses of self assembly as a patterning technique and describe our efforts to mitigate these problems and develop a complete self-assembly patterning process providing sublithographic *size uniformity*, *positional order*, and *pattern registration*. We conclude with a discussion providing our perspective on the most desirable material properties of a self-assembling patterning material for semiconductor device fabrication, and we describe some recent materials innovations that begin to address some of the shortcomings in the present designs.

Nanostructured materials produced by polymer self assembly

The sublithographic dimensions and high feature density provided by self-assembled polymer patterns present an avenue to IC performance benefits through controlled material nanostructuring. The following sections illustrate this idea using examples in which materials and

devices incorporate designed nanostructuring in order to enhance properties such as surface area, optical refractive index, porosity, and feature density. The advantage provided by material nanostructuring in these applications stems from the intrinsic *nanometer-scale size uniformity* and *high feature density* of self-assembled polymer patterns; it does not rely on self-assembled pattern uniformity, positional order, or pattern registration to other lithographic levels. As we will see, material nanostructuring can pay real performance dividends, and the relatively loose requirements on the sublithographic patterning process in these applications (compared with the lithography applications described in later sections) mean easier incorporation of the process into future microelectronics technology generations.

Shallow-trench array capacitor

We customarily think of IC device performance improving upon scaling to smaller dimensions (for example, transistor performance improvement with shrinking gate length); however, a notable exception to this notion is a device whose performance relies on surface area. In this case, smaller device dimensions *degrade* performance: For example, the storage capacity of a passive on-chip capacitor shrinks in proportion to its area. The design of efficient capacitors means storing a required amount of electric charge in a minimal amount of chip area. Charge-storage devices such as on-chip decoupling capacitors [39], dynamic random access memory (DRAM) cells [40], and ferroelectric nonvolatile memories [41] share this same challenge, and over the years inventive techniques such as deep-trench etching [42], three-dimensional stack capacitors [43], surface roughening [44], and high-*k* dielectrics [45] have been introduced as process options for maximizing charge-storage capacity within a shrinking device footprint. We have demonstrated the use of polymer self assembly as a method for increasing capacitor surface area without introducing additional process complexity, creating high-capacitance-density devices composed of arrays of nanometer-scale shallow trenches [46, 47]. This approach is a variation of a planar MOS structure that combines the benefits of surface roughening and DRAM deep-trench devices.

We have previously discussed the importance of capacitance density in terms of both on-chip decoupling capacitors (decaps) [47], in which a required minimum circuit capacitance buffers the power supply against voltage fluctuations, and DRAM storage nodes that store an information bit as charge on a capacitor [48]. While the desired goals of both devices are similar (storing a sufficient charge amount in a minimum area), the target capacitance densities for satisfactory decap performance ($\sim 1 \mu\text{F}/\text{cm}^2$) are roughly an order of magnitude smaller than for DRAM storage nodes ($\sim 10 \mu\text{F}/\text{cm}^2$).

We have fabricated shallow-trench-array decaps by first transferring the self-assembled polymer pattern into a more rugged dielectric hard mask, which is used for further transfer into the device Si counter-electrode. The schematic process is shown in **Figure 2(a)** [48]. A silicon-gate plasma etch produces dense arrays of shallow trenches with aspect ratios, a , of more than 5 to 1 [**Figure 2(b)**], and ~ 20 -nm mean pore diameters. A cross-sectional transmission electron microscope (TEM) image of part of a completed device [**Figure 2(d)**] shows three pores of the shallow-trench array lined with a 4.5-nm SiO₂ gate dielectric (light-colored) and filled with a tantalum nitride top electrode. Narrow pore diameters and relatively high trench aspect ratios make gate electrode formation challenging, and we used TaN atomic layer deposition (ALD) to conformally coat the gate oxide [49].

The roughened silicon electrode surface has a greatly increased surface area compared with the planar substrate. We estimate the degree of surface enhancement by considering a hexagonal nanopore array and a cylindrical trench profile [48],

$$\frac{\Delta A}{A_{\text{planar}}} = \frac{\pi d h}{\ell^2 \sin(60)} = \frac{2\pi}{\sqrt{3}} \left(\frac{d}{\ell}\right)^2 a, \quad (1)$$

where d (pore diameter) and ℓ (center-to-center spacing) are characteristics of the polymer pattern, and h is the shallow-trench-array etch depth. Equation (1) shows that the surface area enhancement ($\Delta A/A_{\text{planar}}$) scales in proportion to the trench aspect ratio, a ($a \equiv h/d$), a property easily controlled through the etch process time. Enhancing the electrode surface area in this manner creates a higher charge-storage capacity ($C_{\text{patterned}}$) without increasing lateral device area (A_{planar}):

$$\begin{aligned} C_{\text{patterned}} &= C_{\text{planar}} \left[1 + \frac{\Delta A}{A_{\text{planar}}} \right] \\ &= C_{\text{planar}} \left[1 + \frac{2\pi}{\sqrt{3}} \left(\frac{d}{\ell}\right)^2 a \right]. \end{aligned} \quad (2)$$

This concept was previously implemented in DRAM stack capacitors using hemispherical grain polysilicon (HSG) [44], although HSG can provide only a limited aspect ratio increase because of the isotropic nature of the surface-roughening process.

Equation (2) estimates capacitance enhancements of ~ 400 – 500% for our shallow-trench-array devices (aspect ratios ~ 5 :1) relative to planar structures of the same lateral area, and ac capacitance measurements (100 kHz, 50-mV ac excitation) confirm this prediction for all applied voltages [**Figure 2(c)**]. The accumulation capacitance ($-V_{\text{bias}}$) increase of 410% correlates well with the geometrical estimate, while the smaller enhancement in inversion ($+V_{\text{bias}}$) ($\sim 290\%$) is caused by full substrate

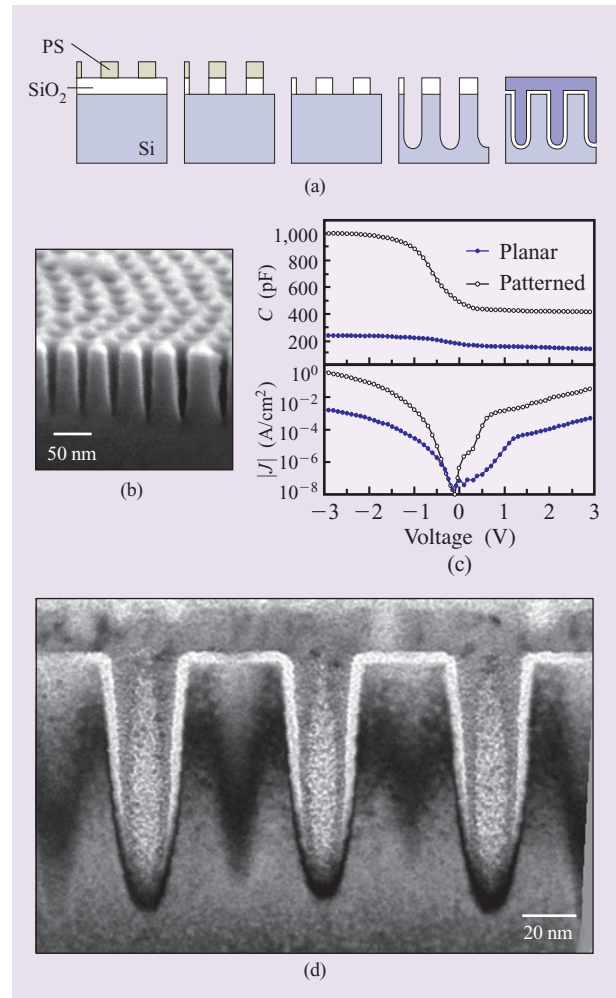


Figure 2

Shallow-trench-array capacitor. (a) Schematic process flow for shallow-trench-array decoupling capacitor fabrication. (b) 70-degree-angle SEM image of shallow-trench-array metal-oxide semiconductor (MOS) capacitor bottom Si electrode. Etched pores have a depth of 100 nm. (c) Upper chart: Capacitance versus voltage for planar (solid circles) and patterned (open circles) devices of the same lateral area. Lower chart: Leakage current per lateral device area for planar (solid circles) and patterned (open circles) devices. (d) Cross-sectional TEM image of completed shallow-trench-array MOS decoupling capacitor. [Parts (a), (b), and (c) republished from [47] with permission. ©2004 IEEE.]

depletion between nanometer-scale pores [47]. Because the gate oxide thickness varies by less than 1 nm over all trench surfaces, we attribute this enhancement to the surface area increase from nanostructuring the device counter-electrode.

One deleterious effect of capacitor electrode nanostructuring is a corresponding increase in device leakage current. The leakage current per lateral device

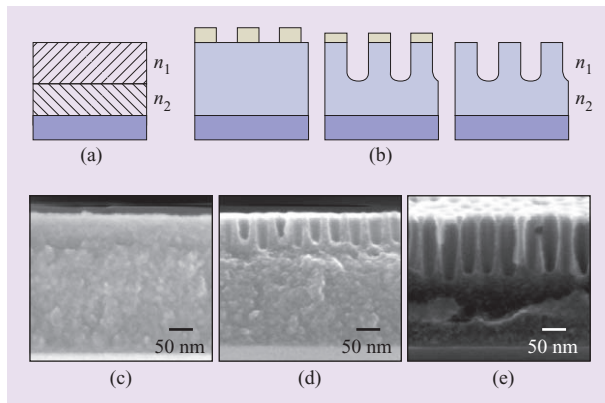


Figure 3

Engineered optical index material. (a) Schematic representation of a layered material with film of optical index n_1 on top of material with optical index n_2 . (b) Schematic process flow for fabricating a layered optical index material by engineering porosity. (c) SEM cross section of unpatterned dielectric film. (d, e) Layered materials with porous top layer patterned using self assembly and plasma etching.

area (J) for the shallow-trench-array capacitor is roughly 100 times higher than that for the planar device [Figure 2(c)]—a much greater increase than is explained by the increased device surface area alone (4.1 times). The excess current likely stems from higher charge tunneling rates in the high-curvature trench bottoms where electric fields are enhanced by a factor of [50]

$$\mu \approx \left(1 + \frac{2t_{\text{ox}}}{d}\right) = \left(1 + \frac{9}{20}\right) = 1.45, \quad (3)$$

where t_{ox} is the gate oxide thickness (4.5 nm) and d is the pore diameter (20 nm).

The shallow-trench-array decap demonstrates a type of performance tradeoff that is often encountered in device design—in this case, the need to strike a balance between enhanced capacitance and appropriate leakage current levels. State-of-the-art planar on-chip microprocessor decaps employ a gate oxide thickness of order ~ 2 nm, which translates to $C \sim 1.7 \mu\text{F}/\text{cm}^2$ and $J \sim 10^{-2} \text{ A}/\text{cm}^2$ at 1 V [45]. The shallow-trench-array decaps utilize a thicker gate oxide (4.5 nm) and can still achieve nearly twice the capacitance density ($C \sim 3.13 \mu\text{F}/\text{cm}^2$ vs. $1.7 \mu\text{F}/\text{cm}^2$) while reducing leakage current levels to $J \sim 10^{-3} \text{ A}/\text{cm}^2$ (at 1 V).

Dimensional tunability is a real advantage of self-assembly processes for nanostructuring surfaces. In addition to controlling the amount of surface area increase through the shallow-trench aspect ratio (i.e., etch process time), we can further control the surface area of the shallow-trench array by adjusting the pore diameter

[48], a dimension that can be tuned either via the initial polymer template [51, 52] or by using a post-etch widening process that controls trench diameter independently of pore separation [2, 53].

Nanostructuring electrode surfaces using polymer self assembly provides a realistic method for achieving increases of up to $\sim 10\times$ in capacitance over that of structures with equivalent planar area by using relatively standard fabrication processes and without introducing novel dielectric materials. These shallow-trench-array devices are compatible with high-performance thin silicon-on-insulator (SOI) circuits, which require special consideration because of their smaller intrinsic circuit capacitance and lack of n -well capacitance. Because these large-area devices consist of many shallow trenches, their performance tolerates variations in the self-assembly process (pattern defects and other imperfections). Device electrical properties (in this case capacitance) therefore do not depend on statistical variations in the self-assembled pattern. Furthermore, our use of self assembly in device fabrication does not require registration of the polymer pattern to other device lithographic levels.

Engineered material optical refractive index

We next explore an application involving engineering the optical properties of a transparent medium using a similar method of controlled nanostructuring. Optical waveguiding relies on the principle of total internal reflection, which is the phenomenon by which light is reflected upon encountering an interface between the medium in which it is traveling and a medium with a lower index of refraction (n). Total internal reflection is the mechanism by which traveling light remains confined in optical fibers and in on-chip optical interconnects. These interfaces between materials having different optical properties are usually fabricated from layers of different materials, such as those shown schematically in **Figure 3(a)**, in which a material of index n_1 sits atop a material of index n_2 .

Self-assembled polymer patterns afford an alternative fabrication method for the layered optical index structure shown in Figure 3(a). In this scheme we use polymer self assembly and pattern transfer into a dielectric film in order to modify the *optical properties* of a fraction of the film. By rendering only a fraction of the dielectric film porous, we create a layered structure comprising a porous top dielectric layer over a fully dense underlying dielectric film. A noteworthy aspect of this approach is that we create *layered* optical structures from a *single* dielectric film and that we can pattern the layered materials in predetermined locations in the wafer. Similar approaches to forming porous waveguiding media have used porous silicon layers [54] and silica xerogels [55]. We control the thicknesses in the stacked

dielectric film by the depth of the dielectric etch (in the same way we controlled capacitance increases by the depth of the electrode etch), thus providing a convenient method for tuning optical path lengths. The porous top dielectric layer naturally has a reduced optical index relative to the underlying dense dielectric film, creating the appropriate index mismatch for a waveguide effect. In this fabrication scheme the nonporous dielectric layer transports light and the porous dielectric cladding layer on top provides the optical confinement.

The nanometer-scale dimensions defined by polymer self assembly are important for reducing light scattering by the porous dielectric layer. The cross section, S , for light scattering by a sub-wavelength object is given by the Rayleigh formula [56],

$$S \propto \frac{d^6}{\lambda^4}, \quad (4)$$

where d is the diameter of the light scatterer and λ is the wavelength of incident light. As we have seen, typical block copolymer dimensions are $d \sim 20$ nm, so for a light wavelength $\lambda \sim 500$ nm the cross section for scattering is small ($S \sim 10^{-3}$), and we can reasonably assume that over short distances there is no scattering by the porous dielectric. Within this approximation, we can estimate the porous material optical index as a weighted volume average of the nonporous film and air ($n = 1$) [57].

We have demonstrated this nanostructuring concept [schematically shown in **Figure 3(b)**] starting with a ~ 250 -nm-thick optically transparent material on a substrate [**Figure 3(c)**]. The base index of refraction of the material is $(n - ik) = (1.56 - i0)$ for light of wavelength $\lambda = 632$ nm. We subsequently transferred a nanometer-scale pattern formed by a self-assembled cylindrical-phase PS-*b*-PMMA film into the dielectric material using a plasma etch process. We controlled the thickness of the porous dielectric layer by the plasma etch time, forming layered dielectric structures of different thickness ratios. A short dielectric etch results in a 50-nm-thick porous layer with a 200-nm-thick dense underlayer [**Figure 3(d)**], while a longer plasma etch creates a 110-nm-thick porous film with a 140-nm-thick underlayer [**Figure 3(e)**]. These demonstration materials are not suitable for practical waveguides because the underlying substrate has a higher optical index and does not provide optical confinement. In practice one would require a low-index cladding material at the bottom interface as well. We can estimate the index of the porous material as

$$\frac{n_{\text{porous}}}{n_{\text{nonporous}}} = 1 - \left(1 - \frac{1}{n_{\text{nonporous}}}\right) v, \quad (5)$$

where v is the pore volume fraction in the porous layer. Equation (5) makes clear that the change in optical index

scales linearly with the amount of film porosity, v , and also that the fractional change increases when nanostructuring high-optical-index ($n_{\text{nonporous}}$) materials. Close-packed self-assembled hole-array patterns create layers with $v \sim 30$ –50% porosity, such that the expected optical index of this demonstration material ranges from 1.39 (for 30% porosity) to 1.28 (for $v = 50\%$). A higher-index base material such as Si (with $n \sim 3.5$ for wavelengths $\lambda \sim 850$ nm to $2 \mu\text{m}$) is reduced to $n_{\text{porous}} \sim 2.7$ for 30% porosity (a decrease of 23%) and $n_{\text{porous}} \sim 2.3$ for 50% porosity (a decrease of 34%).

Nanoporous membranes

In this section we explore a further application of self assembly as a tool for engineering porosity; we demonstrate fully suspended porous silicon membrane structures fabricated using self-assembled polymer patterns [53]. Porous membrane devices are useful for interrogating materials at the size scale of the membrane pore diameters. In their simplest form, membrane devices discriminate materials solely on the basis of size—they reject materials larger than the pore diameter and accept those that are smaller. Membrane device efficiency is closely tied to *pore size uniformity* (which determines membrane selectivity) and *pore density* (which determines membrane throughput)—attributes that are well suited to the strengths of self-assembled polymer patterns [58]. With typical 20-nm mean pore diameters, d (with $\sigma/d \sim 10\%$) and pore densities of $>10^{10}/\text{cm}^2$, polymer self assembly provides the dimensions appropriate for membrane applications in areas such as high-quality molecular sorting, sensing, and filtration [59–61], as well as targeted drug delivery and even fuel cell membranes. One appeal of coupling such membrane devices into silicon technology is the possibility for tight integration with on-chip microelectronic circuits. We describe here our demonstration of building highly uniform nanoporous *silicon* membranes from self-assembled polymer patterns. Our reasons for desiring silicon membrane devices also include the robustness of the inorganic material in thermal and chemical environments. We can also envision increasing membrane selectivity by incorporating chemical functionalization into the silicon pore walls using well-established silicon surface chemistry.

We can convert a self-assembled porous PS film into a suspended silicon membrane by using the schematic process shown briefly in **Figure 4(a)**. The membrane fabrication procedure begins with an SOI wafer with top silicon thickness of 100 nm and buried oxide (BOX) thickness of 300 nm. We form a self-assembled PS template on the oxidized surface of the SOI wafer and then transfer the PS pattern into the top silicon layer (which becomes the membrane in the final structure) by using a two-step plasma etching process similar to that

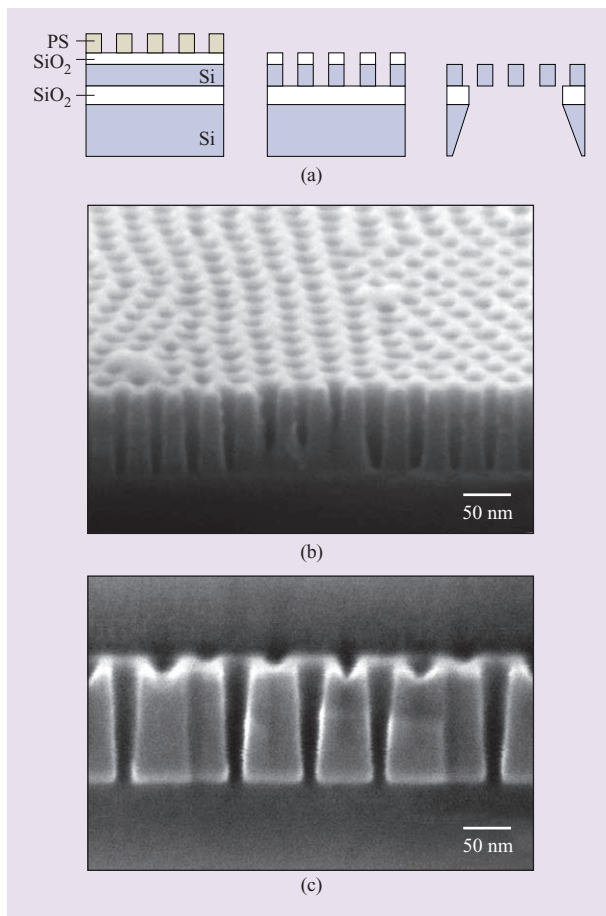


Figure 4

Nanoporous membrane. (a) Schematic process flow for porous membrane fabrication. (b) Cross-sectional SEM image of the etched top silicon layer of an SOI wafer. (c) High-magnification SEM image of a 100-nm-thick suspended porous silicon membrane. (Republished with permission from [53]. ©2006 AVS The Science & Technology Society.)

used in fabricating the shallow-trench-array devices. Cross-sectional SEM images show the completely porous 100-nm-thick silicon layer positioned on top of the oxide layer beneath [Figure 4(b)]. The membrane pore density ($\sim 10^{11}/\text{cm}^2$) reflects that of the original PS template. Standard microelectromechanical systems (MEMS) fabrication techniques are used to release the membrane from the substrate: Following membrane protection with a silicon nitride (SiN) capping layer, we pattern the wafer back side using conventional photolithography and plasma etching, and etch through the wafer using a wet potassium hydroxide (KOH) treatment. The final porous membrane can be de-protected and released using a phosphoric acid etch to strip the SiN and a buffered hydrofluoric acid etch to strip the BOX layer. A cross-

sectional SEM image of a suspended porous silicon membrane shows slightly tapered silicon pores that have a narrowed diameter at the bottom (~ 10 nm) compared with the initial 20-nm opening on the top surface [Figure 4(c)].

Because the initial pore size uniformity of the self-assembled PS template is transferred with good fidelity to the silicon membrane, we expect these devices to have a good capacity for discriminating materials on the basis of their size. The 20-nm mean pore diameter provided by the PS-*b*-PMMA template ($M_n = 64,000$ g/mol) already places these devices in a useful size range [62], and the pore size uniformity ($\sigma/d = 10\%$) may allow a high degree of selectivity. The flexibility of the polymer self-assembly process should allow tuning of membrane pore diameters for target applications. For example, the template dimensions may be adjusted through changes to the copolymer block molecular weight [17, 52, 53]. Another approach incorporates PMMA homopolymer into the diblock copolymer template, which facilitates further pore diameter scaling to 6–8 nm [63]. Polymer crosslinking has also been employed to achieve still smaller pore dimensions of only a few nanometers [64]. In addition, we have previously described fabrication schemes for adjusting the pore diameters of the final silicon structure using either thermal oxidation or conformal material deposition to shrink pore dimensions, or a thermal oxidation and wet chemical strip as a pore-widening process [2, 53]. We have demonstrated an ability to adjust membrane pore dimensions over a range from 10 to 35 nm using these techniques.

Nanocrystal Flash memory

We describe here a final example of a device performance benefit derived from controlling the nanostructure of a material using self-assembled polymer patterns. In this case the nanostructured material plays a critical role in an active electronic device, serving as the charge-storage node of a Flash memory transistor [65, 66].

One-transistor Flash memory cells are the foundation of solid-state nonvolatile memory technology [67, 68]. In simplest terms, these memory devices operate by injecting charge into a conducting floating-gate layer positioned within the gate stack of a field-effect transistor (FET) [66, 69–71]. The presence or absence of charge in the floating gate determines a reversible shift in the threshold voltage for device turn-on, thereby enabling storage of a binary bit of information. (In the late 1990s Intel introduced the StrataFLASH** technology, which allows storage of multiple bits within a single floating-gate device [72].) Device nonvolatility is ensured by using gate oxides thick enough to prevent charge leakage from the floating gate either to the device source/drain region (through the program oxide) or to the gate (through the

control oxide). Floating-gate memory technology has scaled to higher densities extremely well, with Intel recently shipping a 1-Gb NOR chip using 65-nm-technology-node lithography processes. A major challenge of scaling conventional floating-gate Flash devices to smaller dimensions (and thus higher densities) involves the limits of program oxide thickness for maintaining suitable device reliability and memory bit retention times. Estimates of lower limits on program oxide thickness are in the range of ~ 8 nm [67]. This thickness has already been reached in state-of-the-art Flash devices.

Nanocrystal floating-gate memories are predicted to offer better scalability than that of conventional Flash devices [71], providing improved retention and reliability at the same program oxide thickness as well as better cyclability (repeated read/write operations without device failure) and lower-voltage operation. Nanocrystal devices store a memory bit in a floating gate composed of a group of electrically isolated particles rather than in a continuous floating-gate layer, building redundancy into the device and providing tolerance against defects in (or damage to) extremely thin oxide layers. The nanocrystal floating-gate concept is more readily suited to NAND Flash technology, in which devices are programmed by Fowler–Nordheim processes rather than NOR technology, which uses hot electrons from the channel to program the floating gate [67]. NAND Flash chips are the high-density memory typically used in Universal Serial Bus (USB) drives and other memory cards. Despite the expected benefits of nanocrystal Flash memories, no commercial products currently utilize this effect. Of all the major semiconductor manufacturers, Freescale Semiconductor has devoted the most attention to nanocrystal Flash technology and has demonstrated a 24-Mb circuit [73]. A major challenge in fabricating such devices is in achieving sufficient control of nanocrystal size, position, and density to ensure uniformity in device performance while maintaining manufacturable processing techniques [74].

We have previously demonstrated the applicability of self assembly for addressing some of these challenges by fabricating prototype devices in which nanocrystal dimensions, density, and uniformity are defined by polymer self assembly, as shown in **Figure 5** [65, 66]. Such devices gain performance benefits from having multiple nanocrystals contained in a single-device floating gate. Although the nanocrystal dimensions reported here (~ 20 -nm diameter, ~ 40 -nm pitch) are too large to be useful in state-of-the-art Flash devices that have gate lengths of order 50 nm, our demonstration devices are meant to provide a proof of concept. In a later section we discuss at length the issues governing dimensional scaling of polymer self-assembly processes to the smaller sizes

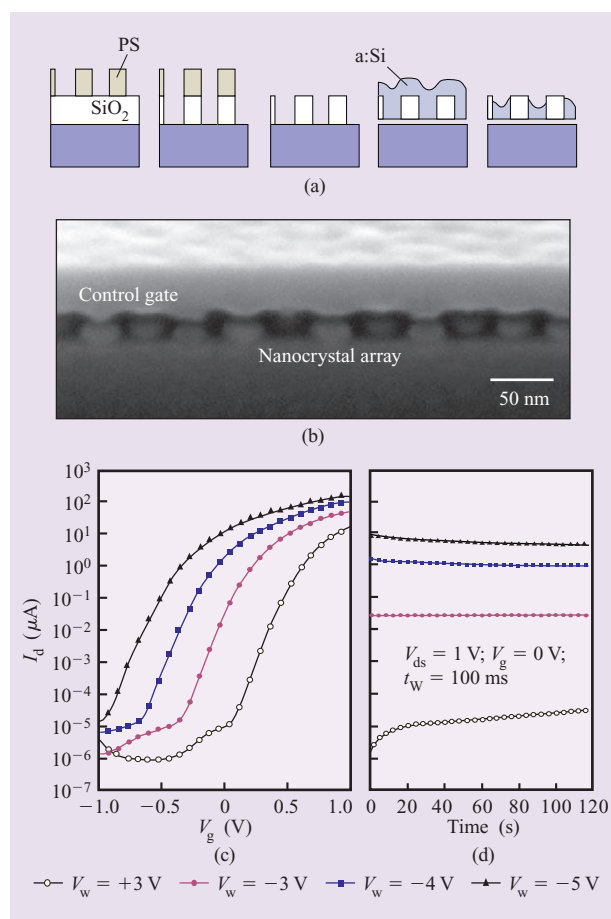


Figure 5

Nanocrystal Flash memory. (a) Schematic process flow for nanocrystal floating-gate fabrication. (b) 70-degree-angle SEM of completed nanocrystal floating-gate structure. (c) Plot of I_d vs. V_g for a nanocrystal FET in erased state (open circles) and written states (filled symbols). Erase voltage was +3 V and write voltages were -3 V, -4 V, and -5 V. Write and erase times were 100 ms. (d) I_d vs. time for a nanocrystal FET in erased state ($V_w = +3$ V) (open circles) and written states ($V_w = -3$ V, -4 V, and -5 V) (filled symbols). [Parts (a) and (b) republished from [2] with permission. ©2005 IEEE. Parts (c) and (d) republished from [65] with permission. ©2007 IEEE.]

necessary for utilization by future Flash memory technology generations.

We have fabricated long-channel nanocrystal Flash memory FETs (gate length $L = 100$ μm , width $W = 880$ μm) whose nanocrystal dimensions, density, and uniformity are defined by using a polymer self-assembly process [65, 66]. We believe that defining nanocrystal dimensions through a templated self-assembly process is inherently more controllable than through chemical vapor deposition (CVD) or aerosol deposition methods [71, 75], in which diffusion and

nucleation effects broaden nanocrystal size distributions. An attractive aspect of the templated approach to nanocrystal formation is the flexibility it offers in the choice of nanocrystal material.

The self-assembled polymer pattern acts as a high-resolution resist for defining arrays of isolated silicon nanocrystals. The process for forming the device gate stack [shown schematically in Figure 5(a)] involves a sequence of etches and depositions, including 1) perforated PS pattern formation by self assembly on a thermal oxide hard mask; 2) oxide etch and PS template removal; 3) program oxide growth by thermal oxidation ($t_{\text{prog}} = 2$ or 3 nm); 4) nanocrystal formation by conformal a:Si deposition and anisotropic a:Si etch. The embedded silicon nanocrystal array dimensions reproduce the dimensions of the initial polymer template (nanocrystal mean diameter $d \sim 20$ nm, $\sigma/d \sim 10\%$, and nanocrystal density $\sim 7 \times 10^{10}/\text{cm}^2$). We complete the nanocrystal Flash gate stack by depositing a control oxide with thickness t_{ctl} of 7 nm over the nanocrystal array floating gate and defining a polysilicon control gate by conventional lithography. A cross-sectional SEM image of the device gate stack shows a dense array of uniformly sized Si nanocrystals electrically isolated between substrate and control gate by a thin program oxide (in this case the thin program oxide is not visible) and a thicker control oxide [Figure 5(b)].

We program these Flash devices by injecting charge into the nanocrystals (through the program oxide), and erase by expelling charge from the nanocrystals. Stored charge shifts the device threshold voltage for current turn-on (V_t). The shift in V_t in response to different write voltages V_w is clearly visible in the device transfer characteristics (source-drain current I_d vs. gate voltage V_g), as shown in Figure 5(c). This data shows a ΔV_t of ~ 0.6 V for a write voltage of $V_w = -3$ V (prior to writing, the devices were erased with $V_w = +3$ V, shown as open circles), turning on at $V_g \sim 0.25$ V in the erased state and at $V_g \sim -0.35$ V in the written state. The threshold voltage shift increases to $\Delta V_t \sim 1.5$ V for $V_w = -5$ V (erase voltage was again $V_w = +3$ V). Control devices containing no nanocrystals show no change in threshold voltage for write voltages up to 10 V. These programming voltages (both write and erase) are significantly lower than those found in commercial Flash memories, which require voltages greater than ~ 12 V for operation [72]. The low programming voltages are a direct consequence of the thinner program and control oxides in these nanocrystal devices.

We evaluated the stability of the two device memory states using write voltages of $V_w = -3$ V, -4 V, and -5 V and an erase voltage of $V_w = +3$ V, and measuring I_d vs. time ($V_{\text{ds}} = 1$ V, $V_g = 0$ V) [Figure 5(d)]. Despite an extremely thin program oxide thickness ($t_{\text{prog}} = 2$ nm), the

devices show only a logarithmic change in I_d over the measured time scale (120 s). While they are not a complete indicator of memory nonvolatility, these retention results clearly indicate promise for the nanocrystal floating-gate technique. Lower-voltage operation combined with nanocrystal floating gates also pays dividends with respect to device cyclability. We have previously shown no degradation in the device memory states for as many as $\sim 10^9$ write-erase cycles [66].

Self-aligned self assembly for high-resolution lithography

Until this point, we have described semiconductor device applications that leverage only the nanometer-scale dimensions, pitch, and density of self-assembled polymer patterns to improve aspects of performance. In these examples, self assembly provides enhancements through controlled material nanostructuring, and the process provides a high degree of nanometer-scale size uniformity. Material enhancements arise from having many nanometer-scale elements operating within a single device, so that a lack of positional control in the self-assembly process does not affect performance.

A different application for polymer self assembly within the IC fabrication process is as a high-resolution lithography substitute—that is, using self assembly to pattern individual elements of devices and circuits. Although polymer self assembly can easily define only a limited set of high-symmetry patterns (unlike lithography, which can define arbitrary patterns), even such simple patterns as line and space lamellar structures and cylindrical hole arrays are useful for defining circuit elements such as FET gates and wiring levels (using line and space patterns) or contact holes (using cylinder hole arrays). This type of application obviously requires more than high pattern resolution alone. Our ability to control pattern alignment and registration to other lithographic levels while minimizing pattern defect density and roughness is a critical barrier to qualifying this technique as a legitimate lithography alternative. The following sections discuss our exploration of diblock copolymer thin-film patterning as a high-resolution lithography option, highlighting experimental progress as well as hurdles yet to be overcome.

As-formed self-assembled polymer patterns (such as the hole-array patterns and line/space patterns of Figure 1) have little positional order and a high defect density. Furthermore, the self-assembly process provides no method for registering self-assembled patterns to other pre-existing lithography levels. Pattern registration is an essential aspect of the semiconductor fabrication process, in which circuits are built up vertically in sequentially aligned layers. Several enhancements to the self-assembly process have achieved varied degrees of success in

controlling the order and defect density in nanostructured polymer films. One approach uses externally applied forces such as electric fields [22, 23, 76–80], mechanical shear [19, 81–85], or shear flow during the self-assembly process as a means to improve positional order. Solvent interactions, including solvent annealing [86–89], solvent evaporation, and solvent crystallization [90, 91], also impart preferred directionality to self-assembled patterns. More exotic ideas have included the use of nano-imprint [83] and super-critical CO₂ methods [92]. Applying these types of external fields during the assembly process reduces the energy degeneracy of block copolymer states and may reduce defect density while also controlling pattern orientation. We concentrate here on two methods that are particularly well suited to semiconductor device fabrication processes—topography-induced alignment (sometimes called *graphoepitaxy*) [84, 93–100] and guided alignment enabled by chemical pre-patterning techniques [30, 101–105].

The first experimental demonstration of self-alignment of a self-assembled block copolymer pattern to lithographically defined surface topography used thin films of sphere-forming PS-*b*-PVP (polystyrene:polyvinylpyridine) [106]. Surface topography promoted close-packed spherical domain alignment along the direction of the lithographically patterned groove sidewalls and also templated 2D single-crystal domains within micron-sized areas ~ 100 times larger than the intrinsic block copolymer period. This result and the other examples that have followed demonstrated two key aspects: Pre-patterned lithographic features provide a means for self-registration of self-assembled polymer patterns to existing structures; and the self-assembly process can subdivide large pre-patterned lithographic features into sublithographic units. Since this initial demonstration, similar self-aligned behavior has been shown in other spherical-phase materials as well as both parallel- and perpendicular-oriented cylinder patterns [32, 34, 89, 93, 94, 99, 100, 107–114]. Self-aligned cylindrical and spherical polymer patterns have been employed as fabrication tools to pattern high-density magnetic media [32, 34, 107, 113] and, more recently, transistor contact holes [108]. Perpendicular-oriented lamellar patterns have proven more difficult to self-align using this technique; however, there have been a limited number of successes [112, 114]. We shortly describe the issues involving lamellar materials in much more detail.

Aspects relating to the limits of defect density and pattern registration in self-aligned self-assembled polymer patterns have been studied in detail using spherical-phase polystyrene:polyferrocenyldimethylsilane (PS-*b*-PFS) thin films confined in linear grooves [96]. The work details careful measurements and analysis of the effects of template width and roughness on the degree of positional

order in lithographic structures ranging in width from $0.5L_0$ to $15L_0$ (L_0 is the characteristic length of block copolymer domains). The number of polymer periods (n) fitting within each lithographic groove is determined by commensurability between the lithographic template width (w) and the intrinsic polymer period (L_0). Defect-free polymer patterns comprising n periods form when the lithographic width satisfies the condition $w \approx nL_0$. A tolerance of the self-alignment process to small variations in the lithographic width is important when considering the difficulty of lithographic patterning at dimensions of ~ 100 nm [99, 109, 115].

The free energy of a confined block copolymer pattern has its local minimum at exact commensurability between L_0 and the lithographic template width (i.e., $w = nL_0$), and the free-energy increases as $\sim (w - nL_0)/n$. Defect formation is thus energetically more expensive within a narrow groove, meaning that block copolymer registration becomes more difficult and prone to defects as the lithographic feature size increases. This fact limits the ultimate degree of subdivision ($= w/L_0$) achievable by this self-alignment technique [109]. There have recently been similar experimental studies of commensurability and ultimate size limits of self-alignment processes in parallel-oriented cylinder patterns of both PS-*b*-poly(ethylene-alt-propylene) and PS-*b*-PMMA [99, 113]. Template edge roughness and nonuniformity of polymer domains also ultimately affect the placement error of self-assembled block copolymer patterns. The intrinsic limits on registration accuracy of self-aligned polymer patterns are ultimately dictated by phase-separation thermodynamics and compositional and polydispersity effects [108]. For example, typical sphere- or cylinder-forming patterns have domain size and spacing distributions with $\sigma \sim 0.03L_0$ to $0.1L_0$, which translates directly into placement error in pattern registration.

Chemical pre-patterning also provides a useful technique for self-aligning self-assembled block copolymer patterns. In this case a lithographic process is used to define a surface chemical pattern that guides the subsequent assembly of block copolymer domains. For example, perpendicular PS-*b*-PMMA lamellar patterns self-align with surfaces chemically pre-patterned with alternating PS-wetting and PMMA-wetting stripes [103, 104]. The condition for defect-free pattern registration is that the interfacial energy gain from preferential wetting of each block sufficiently compensates the strain energy that results from bending and deviation between w and L_0 [116–119]. One distinct difference between chemical pre-patterning and topographic alignment techniques is that chemical patterning does not provide for lithography subdivision; that is, the chemical pattern must be printed at dimensions and pitch close to the intrinsic dimensions of the block copolymer pattern (i.e., $w \sim L_0$). Although

this rules out chemical pre-patterning as a method for reduction of lithographic features, there are other potential advantages. For one, the self-assembly process appears to smooth out roughness and imperfections in the initial chemical pattern, potentially improving the critical dimension control of the initial lithography step. The technique has also been demonstrated to produce nonregular shapes and patterns other than the high-symmetry structures formed naturally [118].

Lithography applications of polymer self assembly

When considering self-assembly approaches for semiconductor-based device fabrication, we must first define measures by which to judge the quality of the assembled patterns. We have already mentioned statistical measures of pore diameter distributions as a method for gauging size uniformity [17], and we have discussed device applications that leverage the small feature size and high density provided by self-assembled patterns. Here we discuss our experimental efforts to understand and ultimately control the positional order of self-assembled patterns.

We refer generally to a “sufficient degree of alignment” as being a combination of orientational order, translational order, and pattern registration that is sufficiently uniform for semiconductor device fabrication. Good orientational order means that the self-assembled pattern is free from gross defects that disrupt the directional orientation. Circular defects such as disclinations, target shapes, and spirals all fall within this category of orientational defects [120, 121]. Sufficient translational order implies that the pattern is free of dislocation defects and that line fluctuations fall within the tolerances required by a particular application. For high-performance semiconductor devices, these tolerance requirements are enumerated in the ITRS Lithography Roadmap [122]. For example, the 22-nm-technology node (scheduled for manufacturing in 2016) specifies control of critical feature dimensions within $3\sigma = 0.9$ nm (for the microprocessor gate) and a linewidth roughness variation (LWR) of $3\sigma = 1.2$ nm (8% of critical dimension)—difficult targets indeed. Pattern registration means providing sufficiently accurate placement of one pattern with respect to other predefined features on the substrate, and also implies control over the location of a defect-free region in the self-assembled pattern. In the ITRS Lithography Roadmap, this “overlay” requirement is (for the 22-nm-technology node) $3\sigma = 4.0$ nm (for DRAM and Flash applications). We note that the dynamics of self-assembled pattern coarsening and the free-energy penalties associated with each type of defect vary for different block copolymer phases, such that controlling

defects in spherical, cylindrical, or lamellar patterns may require different approaches.

Defect annihilation in block copolymer thin films is a complex process, and the full molecular details are not yet fully understood. Material parameters such as χ , the product χN , elastic constants, and Young’s modulus all play a role in film defect dynamics and annihilation [121], and they may vary for different materials or for different phase morphologies. For example, while PS-b-PMMA [123], PS-b-PFS [124], and polystyrene-b-polyisoprene (PS-b-PI) [124] all have similar values for χ , PS-b-PVP [125] shows a much stronger dependence on temperature. As well, in phase-segregated domains the molecular diffusion constants perpendicular to domain orientations (D_{perp}) can be orders of magnitude smaller than those parallel to domain orientations (D_{par}) [126, 127]. This is a key point for understanding the underlying cause of slow defect annihilation of orientational defects which necessarily require layer breaking.

Among the demonstrated methods for improving the orientational order of self-assembled patterns, topography-induced graphoepitaxy [84, 93–95, 97–100, 106] and surface pre-patterning [30, 101–105, 118] stand out because of their capacity for controlling translational order as well as providing pattern registration. We focus our discussion on these techniques because of the straightforward manner in which they can be implemented in silicon device fabrication. Other important techniques for achieving orientational order were mentioned previously; their further discussion is beyond the scope of this paper [3, 6, 8, 128, 129]. Here we center our discussion on self-aligning processes for PS-b-PMMA diblock copolymers, which have been the focus of our program at IBM.

Self-aligned self assembly: Graphoepitaxy

The idea of topography-induced ordering, often referred to as *graphoepitaxy*, is straightforward: A block copolymer film is applied on top of topographic features (either recessed trenches or raised steps), and the topographic boundaries propagate ordering of the self-assembled pattern. In this way the self-assembled pattern self-registers to the (often) lithographically defined topographic pattern, while subdividing the lithographic structure.

Successful pattern alignment by graphoepitaxy depends on efficient defect annealing in the self-assembled pattern, commensurability between the length scale of the lithographic structure and the self-assembled pattern, and preferential surface wetting by the self-assembling material. We briefly discuss this last requirement here in terms of in-plane cylindrical-phase films. In these materials pattern formation depends on preferential surface wetting of the minority block (which is PMMA in

our 70:30 PS-*b*-PMMA materials). Under these conditions a monolayer PS-*b*-PMMA brush covers the entire surface, with the majority block (PS) pointing away from the surface. This brush layer provides a template for ordering of a subsequent PS matrix and decouples the in-plane cylinder pattern from the surface. Pattern formation can be complicated by pinning effects in situations in which the surface is preferentially wet by the majority block [130].

We have used surface topography to register a cylindrical-phase PS-*b*-PMMA film ($M_n = 64,000$ g/mol) to a predefined larger-scale lithographic layer [93]. We first pattern a shallow 20-nm-deep trench in an oxide surface using conventional photolithography and plasma etching. This slight topography induces preferential domain formation at the trench edges during the initial stages of polymer film assembly. The polymer domain structure builds away from the trench edges, optimally filling the entire recessed region with an aligned pattern of parallel cylinder domains. **Figure 6(a)** shows five PS-*b*-PMMA cylinder periods subdividing a 0.2- μ m-wide trench formed in an SOI layer.

A systematic study of striped cylindrical patterns of another diblock copolymer material, polystyrene-*b*-poly(ethylene-*alt*-propylene) (PS-*b*-PEP) [99], has shown that commensurability between the lithographic trench width and the natural block copolymer period (L_0) guarantees a single-valued number of stripes within each channel for widths as wide as $9L_0$ (an observation similar to the behavior we have measured for PS-*b*-PMMA). For wider lithographic trench widths ($>9L_0$), the system free-energy configuration [131, 132] does not discriminate sharply enough against dislocation defects that generate multi-valued numbers of stripes within a given channel [29, 109].

Although we have implemented self-aligned PS-*b*-PMMA cylinder patterns in fabrication of nanowire array FETs [133], these materials have significant shortcomings as high-resolution patterning materials. Cross-sectional SEM images of a self-aligned film show the profile of an aligned in-plane cylinder pattern [**Figure 6(b)**]. From a 70-degree angle, the pattern appears to form equal lines and spaces [**Figure 6(c)**]; however, the film cross section reveals that even after film development, the spaces contain a significant polymer underlayer (~ 20 nm thick) that must be removed prior to any pattern transfer process. Removing this layer is difficult because of the limited total resist thickness (only ~ 30 – 40 nm). Furthermore, because the spaces are defined by surface-parallel cylindrical PMMA domains, the PS resist profile is bowl-shaped [**Figure 6(b)**] rather than a more desirable square shape in profile [**Figure 6(d)**].

Striped lamellar-phase patterns have a more promising resist cross section with a rectangular two-dimensional

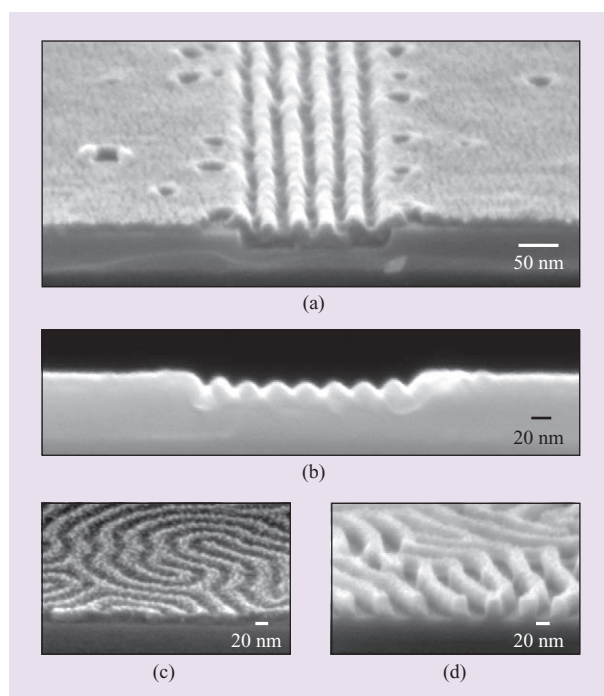


Figure 6

Self-aligned cylindrical-phase PS-*b*-PMMA diblock copolymer films. (a) 70-degree-angle SEM image showing self-aligned in-plane cylinder pattern. (b) Full SEM cross section showing film profile. (c) 70-degree-angle SEM image of unaligned cylindrical-phase striped pattern. (d) 70-degree-angle SEM image of unaligned lamellar-phase striped pattern. [Parts (a) and (b) republished from [16] with permission. ©2006 SPIE.]

density profile [16, 114, 115] [compare Figures 6(c) and 6(d)] and have the potential for a lower level of roughness [compared with striped cylinder patterns—compare Figure 1(b) with the right side of Figure 1(d) [16, 114]. Unlike graphoepitaxy of striped cylinder patterns, in this case we desire block preferential wetting only on the trench sidewalls, leaving a neutral wetting surface on the trench bottom in order to promote perpendicular lamellar orientation. One straightforward way to attain this condition is by pre-treating the trench bottom with a PS-*r*-PMMA random copolymer [25] while leaving the trench walls untreated [16, 112, 114].

Unfortunately, even with appropriate surface wetting conditions, graphoepitaxy of perpendicular lamellar striped patterns is challenging. Although lamellar and cylindrical phase materials each form striped patterns, our data suggests that the mechanisms for defect annihilation are different. Whereas spherical [134, 135] and cylindrical [29, 95, 96, 136, 137] patterns coarsen with annealing time and/or temperature, lamellar patterns do not because of very limited defect annihilation processes

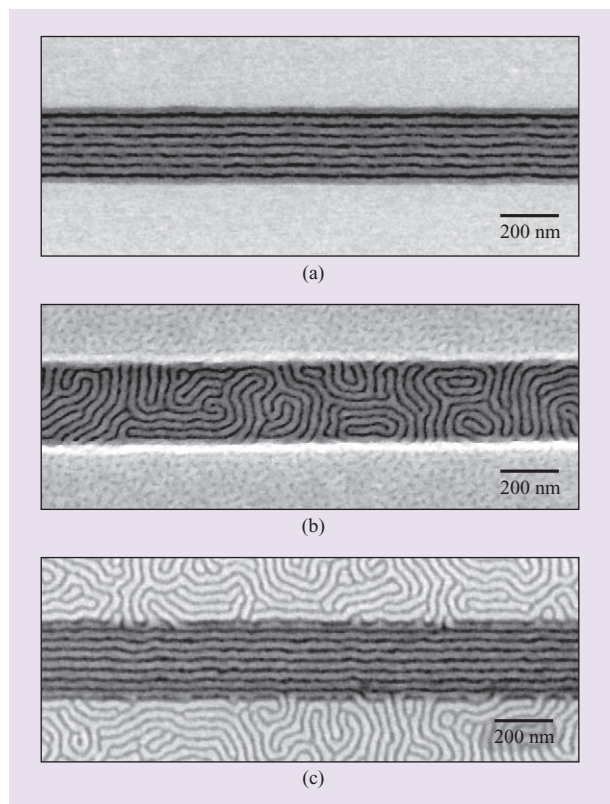


Figure 7

Pattern registration on lithographically prepatterned substrates. (a) Cylindrical-phase thin film in a silicon oxide lithographic trench. The striped pattern aligns free of defects along the trench walls. (b) Lamellar-phase thin film in the same type of trench. The pattern remains unaligned regardless of annealing conditions. (c) Aligned lamellar-phase thin film on top of a cylindrical film similar to the one shown in (a). (Republished from [29] with permission. ©2007 Wiley–VCH.)

[29]. Consequently, the only demonstrations of lamellar-phase graphoepitaxy have used either very narrow trench widths [112, 114] ($<5L_0$), lower-molecular-weight lamellar materials [114], or thinner films (thickness $<L_0/2$) in which a limited amount of pattern coarsening can occur [29]).

Enhanced graphoepitaxy using chemical surface patterning

We have mentioned the favorable qualities of perpendicularly oriented lamellar-phase materials as fabrication templates, with the caveat that fundamental material properties prevent their ordering via a convenient means such as graphoepitaxy. We describe here a method by which the graphoepitaxy technique can be augmented to facilitate sufficient ordering in these attractive material systems.

Previous experiments have demonstrated that chemical substrate patterning at the length scale of the diblock copolymer (L_0) improves the orientational and translational order of self-assembled lamellar films [30, 101–105, 118]. The idea is that the chemical pattern directs the assembly process during the initial material microphase separation and therefore minimizes nucleation of any pattern defects. With no need for defect annihilation or pattern coarsening, the lamellar pattern can achieve a high degree of uniformity over areas as large as the initial chemical pattern. This technique has been used to generate patterns containing arbitrary angles or radii of curvature [118]. A main challenge of the chemical pre-patterning technique is a need to pre-pattern at dimensions near the length scale of the final self-assembled pattern.

Our approach for addressing this challenge has been to use a self-assembly process to provide the chemical pattern as well, rather than using a high-resolution lithographic technique. We have used graphoepitaxy of a cylindrical-phase PS-*b*-PMMA film (described in the previous section) as the chemical template for inducing order in an overlying lamellar film, as shown in **Figure 7** [29]. The advantage of this approach is that the initial cylinder self assembly provides the chemical pre-patterning. The resulting final polymer double layer has a better resist aspect ratio (50 nm:15 nm = 3.33:1) vs. the cylindrical material alone ($\sim 30:15 = 2:1$). Though an improvement, the technique is still limited in that the final structure contains a PS underlayer that must be removed, and the top lamellar layer unfortunately appears to reproduce the roughness of the cylinder underlayer.

Surface engineering for local defectivity control

Because of the extremely limited degree of pattern coarsening in striped patterns of perpendicular lamellar materials, we have explored the potential of local pattern defect density control using surface engineering. Rather than striving for pattern perfection everywhere, we tailor surface properties to promote defect-free patterns in localized targeted areas [115]. A tapered trench design such as that shown schematically in **Figures 8(a)** and **8(b)** demonstrates the idea. The purpose of the tapered region is twofold: First, the narrow trench (region 1, with width commensurate with L_0) imposes a high free-energy penalty for defect formation compared with the energy cost of a defect in the wider areas (regions 2) [109, 132]. In addition, the tapered design promotes polymer shear flow that favors pattern orientation parallel to the trench walls. We have engineered topographic channels of specific geometry and chemical functionality with the goal of controlling the degree of self-assembled pattern perfection within particular areas of the substrate. Our technique optimizes polymer interfacial interactions,

commensurability effects, and polymer shear flow in forming aligned defect-free lamellar striped patterns with a two-dimensional density profile suitable for lithographic applications. The idea of controlling local pattern defects is important in systems such as thin films of symmetric PS-*b*-PMMA block copolymers, which have high energy barriers for defect annihilation. We have shown that this approach is useful in creating defect-free areas in channel widths up to $20L_0$ ($\sim 0.64 \mu\text{m}$) and as long as $5 \mu\text{m}$ [Figures 8(c)–8(f)], distances that are much larger than twice the correlation length in unconfined patterns of the same material ($\sim 128 \text{ nm}$) [115].

Nanowire array field-effect transistor

Processes for pattern alignment and registration are essential when considering any self-assembly technique as a high-resolution lithography substitute. We have described our progress in developing self-aligned self-assembly processes based on topographic registration of PS-*b*-PMMA films. The ability to precisely position nanometer-scale polymer domains relative to lithographically defined patterns opens possibilities for their use in defining the highest-resolution features of integrated circuits, such as transistor gates, wiring levels, and contact holes [108]. Here we describe another application of self-aligned polymer self assembly that demonstrates the value of lithography subdivision by patterning transistor channel elements at sublithographic dimensions and pitch [65, 133]. This is a key fabrication challenge for aggressively scaled silicon field-effect transistor designs.

The semiconductor industry [138] and the International Technology Roadmap for Semiconductors (ITRS) [122, 139] have identified several alternative FET designs that may offer continued performance improvements down to dimensions approaching 10 nm . Three of these promising designs are the finFET [140], the tri-gate FET [141], and the nanowire FET [142]. These designs gain performance advantages by defining either the device channel width (for tri-gate and nanowire FETs) or the device body thickness (for finFETs) at extremely high resolution [143], enhancing transistor gate-to-channel coupling. These device designs introduce complexity into building FETs that drive different amounts of current, which is necessary in ICs in which devices perform varied functions. The current drive of conventional FETs is adjusted through the lithographically defined width (w). In contrast, the nanowire FET channel width cannot be changed without altering fundamental device characteristics; instead, the current drive of these FETs is engineered by operating multiple channel elements together in parallel. We have seen the proficiency with which self-assembled polymer films can form regular line/space patterns, making them

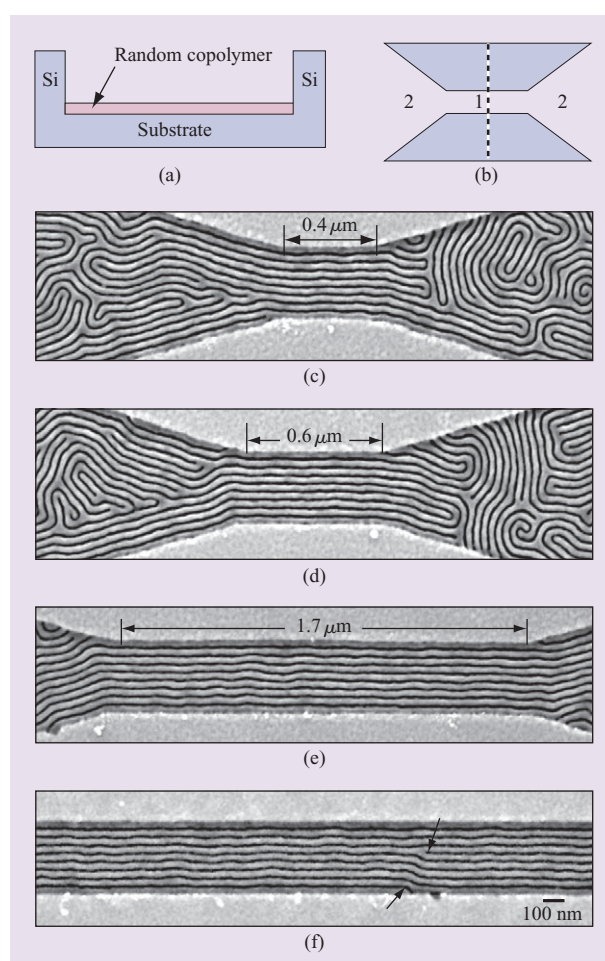


Figure 8

(a) Schematic representation of a trench cross section prior to polymer deposition taken along the dashed line shown in (b). (b) Schematic representation of a fabricated silicon channel. White areas are recessed by $\sim 20 \text{ nm}$ with respect to the gray areas. (c)–(f) Lithographic channels with narrow regions of width $w = 9L_0$ and lengths of (c) $0.4 \mu\text{m}$, (d) $0.6 \mu\text{m}$, (e) $1.7 \mu\text{m}$, and (f) $>5 \mu\text{m}$. (Republished from [115] with permission. ©2007 Wiley–VCH.)

ideally suited for this application which requires small channel elements packed in close, regular proximity.

We used the self-alignment capability of parallel-oriented cylindrical-phase PS-*b*-PMMA films to subdivide lithographic patterns of different widths, thereby forming arrays of different numbers of close-packed polymer domains [93]. The spacing of PMMA cylinders in a single layer is $(2/\sqrt{3})L_0 \sim 40 \text{ nm}$, and in these experiments we subdivided lithographic widths between 200 nm (into $200/40 = \text{five periods}$) and 600 nm (into $600/40 = \text{fifteen periods}$). An attractive benefit of this technique is that we control the number of polymer lines formed using the width of the lithographic feature. We

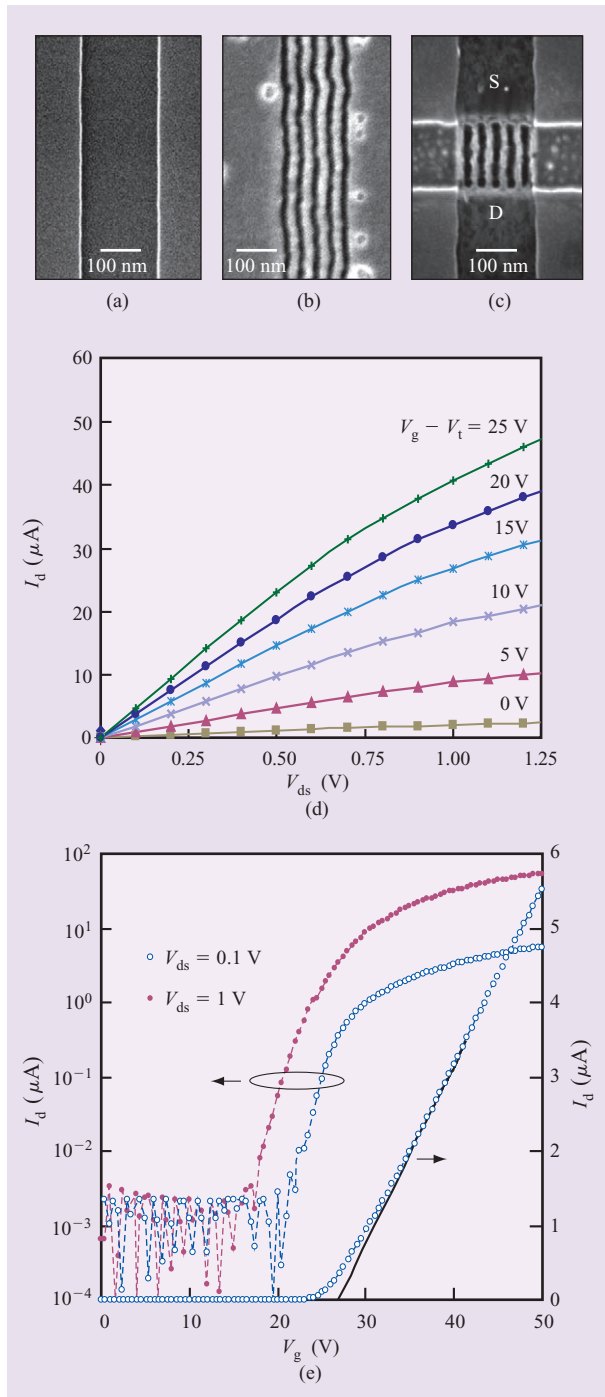


Figure 9

Nanowire array FET. (a)–(c) Nanowire array FET fabrication. (a) Lithographic definition of FET channel. (b) Self-aligned polymer self assembly subdivides lithographic feature. (c) Completed nanowire array FET six-wire channel. (d) Output characteristics. Drain current vs. drain voltage (I_d vs. V_{ds}) for an eight-nanowire FET. (e) Transfer characteristics. Drain current vs. gate voltage (I_d vs. V_g) for an eight-nanowire FET. (Republished with permission from [133]. ©2005 American Institute of Physics.)

convert the pattern formed by these self-aligned PS templates into silicon nanowire arrays via a sequence of plasma etch steps [133].

Polymer self-alignment registers the nanowire array location to larger-scale lithographic patterns and enables the fabrication of nanowire array FETs. Here we describe a FET fabrication scheme in which the self-assembly process defines the number of nanowires, the nanowire width, and nanowire pitch, and also aligns the nanowire array to two other lithographic levels. We use optical lithography and plasma etching to form a 200-nm-wide and 25-nm-deep trench in the 40-nm-thick top silicon layer of a p-type SOI wafer (resistivity = 14–18 $\Omega\text{-cm}$) [Figure 9(a)]. This lithographic feature initiates self alignment of five periods of a PS-b-PMMA cylindrical-phase film [Figure 9(b)]. A second lithography level aligned with both the trench level and the self-assembled level defines the device source and drain contacts [Figure 9(c)], and the distance between these contacts delineates the device gate length (140 nm). Titanium metal (40 nm) masks the source and drain regions during the subsequent nanowire etch and also results in a raised source and drain geometry [138, 144], which reduces device contact resistance. In Figure 9(c), the silicon plasma etch forms a six-nanowire array (wire widths $\cong 15$ nm, height $t_{Si} = 15$ nm, and pitch = 40 nm) connecting device source (S) and drain (D). We have scaled the device width to 8, 10, and 16 nanowires by varying only the lithographic width of the initial trench. Devices are completed with a 650°C anneal (2 minutes in Ar) to form TiSi_2 Schottky source and drain contacts [145], as well as a 450°C forming gas anneal (90% N_2 :10% H_2). In these demonstration devices we gate the wire arrays with the substrate through a silicon dioxide layer of thickness $t_{ox} = 145$ nm.

An eight-nanowire n-channel FET drives ~ 48 μA of current (I_d) at 25 V gate overdrive (V_g) and drain bias $V_{ds} = 1.25$ V [Figure 9(d)]. The high V_g required to operate these devices is due to their extremely thick gate oxide $t_{ox} = 145$ nm. A more appropriate t_{ox} for these nanowire array devices would be ~ 100 times thinner. These devices also operate as ambipolar FETs (i.e., both n- and p-channel) because of the metal-silicide source and drain contacts (rather than doped contact regions) [146], although we describe here only the n-channel operation. The nanowire array FET device transfer behavior (I_d vs. V_g) shows an on-current to off-current ratio (I_{on}/I_{off}) of $\sim 10^5$ ($V_{ds} = 1$ V) [Figure 9(e)], which is large for Schottky-contact FETs [147, 148] and results from a reduction in parasitic off-current leakage paths ($I_{off} \sim 1$ nA) because nanowire channels ($t_{Si} = 15$ nm) are fully depleted of charge. We measure the maximum device transconductance at high drain bias ($V_{ds} = 1$ V) of

$g_{\text{msat}} = 2.5 \mu\text{S}$. Factors that reduce g_{msat} include current limiting from Schottky source and drain barrier heights [149] and increased surface scattering from nanowire line-edge roughness. These demonstration devices have significant short-channel effects as well, caused by the thick gate oxide t_{ox} (relative to other device dimensions). The inverse subthreshold slope (S) is 2 V/decade, and the device drain-induced barrier lowering is ~ 4.5 V/V.

The self-aligned polymer self-assembly process subdivides arbitrary lithographic widths into different numbers of parallel nanowires and thus eases current drive scaling of nanowire-based devices. We have fabricated devices made of 6, 8, 10, and 16 wires by simply adjusting the lithographic width of the initial device channel. This is very similar to the process for width scaling of conventional FETs. The nanowire array FET drive current [I_d at $(V_g - V_t) = 25$ V with $V_{ds} = 1$ V] scales linearly with the number of wires comprising the device, meaning that each wire contributes equally to the device conductance.

Dimensional scaling of polymer self assembly

We have seen throughout this discussion the facility with which self-assembled block copolymer patterns provide access to sublithographic dimensions. A further attractive feature of the technique is its size tenability. That is, block copolymer patterns have the potential to meet the requirements of successive future microelectronics generations because of their ability to scale to smaller dimensions. In a block copolymer pattern, the characteristic domain length scale (L_0) scales with the material total degree of polymerization (N) as [150–152]

$$L_0 \propto N^\delta, \quad (6)$$

where $\delta = 2/3$ in the strong segregation regime (for strongly immiscible polymer blocks). Different theoretical models for more or less strongly segregated blocks all predict δ in the range of $0.5 < \delta < 1$ [153].

For a monodisperse symmetric PS-*b*-PMMA diblock copolymer, the relationship between N and the total polymer molecular weight is

$$N = M_n \left(\frac{0.5}{m_s} + \frac{0.5}{m_{\text{mma}}} \right) \approx \frac{M_n}{100}, \quad (7)$$

where M_n is the number-averaged molecular weight, and m_s and m_{mma} are the styrene and methylmethacrylate monomer molecular weights (each ~ 100 g/mol) [154]. These relationships [(6) and (7)] suggest that it is possible to tune pattern feature sizes (L_0) by selecting the appropriate polymer molecular weight (M_n). In practice, the largest achievable dimension is limited by the kinetics

of phase separation (and thus pattern formation) of high-molecular-weight polymer chains.

The minimum dimension definable by a given material is limited by the driving force for microphase separation, which is proportional to the polymer molecular weight. The block incompatibility that causes phase separation is parameterized by the product χN , where χ is the Flory–Huggins parameter characterizing the interaction strength between the blocks. Larger values of χN indicate a stronger degree of phase separation.

Typically χ decreases with increasing temperature, T , according to [121, 150, 153]

$$\chi = c_1 + \frac{c_2}{T}, \quad (8)$$

where c_1 and c_2 are material constants for specific fractional compositions. For symmetric PS-*b*-PMMA diblock copolymers, $c_1 = 0.028$ and $c_2 = 3.9$ [123]. At $\chi N \ll 1$, the copolymer melt is disordered, and the only correlations are of the order of the radius of gyration of the copolymer [150, 155]. At $\chi N \gg 10$, the copolymer pattern contains sharp interfaces separating the nearly pure block microdomains. Mean field theory calculations [150, 155] predict an order–disorder transition in the polymer for $\chi N = 10.5$, often referred to as the *order–disorder transition* (ODT). The weak segregation regime corresponds to χN in the vicinity of ODT, where polymer microdomains are weakly segregated with a sinusoidal compositional profile [150].

From this discussion we can use the value $(\chi N)_{\text{ODT}} = 10.5$ as a minimum requirement for a symmetric diblock copolymer to form a segregated pattern. Substitution of this condition into Equation (8) yields the minimum degree of polymerization necessary for pattern formation (at a given temperature), N_{ODT} :

$$N_{\text{ODT}} = \frac{10.5T}{c_1T + c_2}. \quad (9)$$

Alternatively, we form an expression in terms of the temperature above which a material of given molecular weight will not self-assemble into a sharp pattern (often called the order–disorder transition temperature, T_{ODT}):

$$T_{\text{ODT}} = \frac{c_2N}{(10.5 - c_1N)}. \quad (10)$$

A dimensionless plot of the phase diagram [Equation (10)] for a fictitious material illustrates the decrease of T_{ODT} with decreasing N [Figure 10(a)]. Regions above and to the left of the T_{ODT} boundary denote conditions for either weakly segregating materials or disordered regimes. Points below and to the right of the boundary are more strongly segregating and result in well-defined pattern formation. The T_{ODT} interface is not a sharp boundary for whether or not a material will form a pattern, but

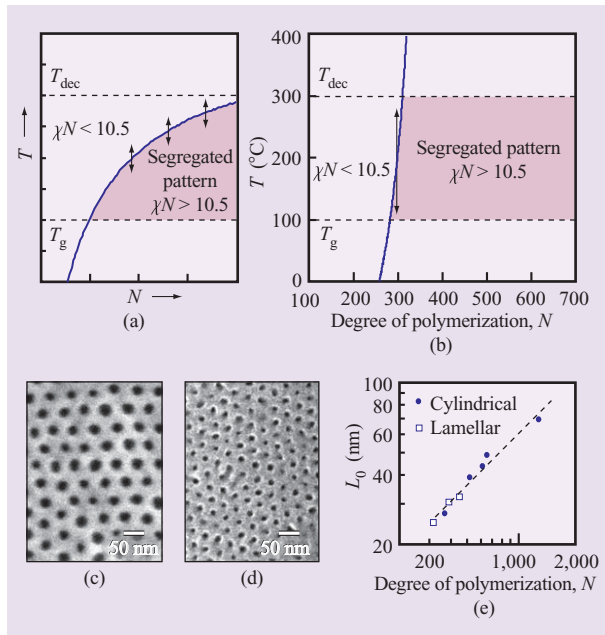


Figure 10

Temperature vs. degree of polymerization (N) phase diagram for (a) fictitious diblock copolymer material, (b) PS-b-PMMA diblock copolymer material. Curves represent the condition $\chi N = 10.5$, which is the polymer order-disorder transition temperature. (c, d) SEM images of porous cylindrical-phase PS films. (c) $M_n = 64,000$ g/mol. Mean pore diameter 20 nm and mean center-to-center spacing of 40 nm. (d) $M_n = 38,000$ g/mol. Mean pore diameter 12 nm and mean center-to-center spacing of 25 nm. (e) L_0 vs. polymer degree of polymerization. The slope of the dashed line is 0.77. [Parts (c) and (d) republished with permission from [53]. ©2006 AVS, The Science & Technology Society.]

rather an indicator of a crossover to a more weakly segregating regime, especially in thin films in which preferential surface wetting by one block is enough to induce ordering even at temperatures above ODT [156]. X-ray experiments have detected persistent self-assembled patterns in polymer films above T_{ODT} [95], although the materials have more diffuse domain boundaries. Polymer diffusion experiments have also shown no discontinuities in molecular diffusivity in the vicinity of T_{ODT} [126, 127].

The interfacial width between polymer blocks at the domain boundary also plays a role in determining the ultimate minimum definable dimension. This width (Δ) is given by [157–160]

$$\Delta_{\infty} = \frac{2a}{\sqrt{6\chi}}; \quad \Delta = \Delta_{\infty} \left[1 + \ln 2 \left(\frac{1}{\chi N_A} + \frac{1}{\chi N_B} \right) \right], \quad (11)$$

where Δ_{∞} is the interfacial width in the limit of infinitely

long polymers, and a is a statistical monomer segment length. We can estimate an average $a \sim 0.7$ nm in our PS-b-PMMA materials because the statistical lengths and molecular weights of styrene and methyl methacrylate are similar [154]. For PS-b-PMMA at 200°C, Equation (11) gives $\Delta_{\infty} \sim 3$ nm ($\chi = 0.028 + 3.9/T$) [123], while experimentally measured values of Δ are of the order of 5 nm [161, 162]. In lamellar materials with feature sizes ~ 20 nm [see Figures 1(d) and 6(d)], Δ is $\sim 25\%$ of the domain width.

For straightforward polymer thermal annealing, the experimentally accessible region of the block copolymer phase diagram [Figure 10(a)] is restricted from below by the polymer glass transition temperature (T_g) and from above by the polymer decomposition temperature (T_{dec}). Annealing temperatures (T_s) sufficiently above T_g allow the block copolymer melt to phase-separate into nanometer domains and form a self-assembled pattern [in PS-b-PMMA we find reasonable polymer mobility for $(T - T_g) > 60^\circ\text{C}$]. In general, increased annealing temperatures result in higher polymer diffusivity and thus faster pattern formation. The upper limit on annealing temperature is the polymer decomposition temperature; we have observed $T_{dec} \sim 300^\circ\text{C}$ for PS-b-PMMA materials annealed in vacuum.

In a previous section we have described defect control in self-assembled polymer patterns, and our discussion here provides further insight into this important issue. Defect melting in phase-separated polymers necessarily involves intermixing of immiscible polymer blocks, an energetically unfavorable process when the materials are strongly immiscible. As we noted above, under typical PS-b-PMMA annealing conditions the interfacial width at a domain boundary is only ~ 5 nm (25% of a typical domain size), meaning that a large fraction of material remains fully segregated. The phase diagram of Figure 10(a) illustrates that the annealing temperature is a useful experimental lever for tuning the miscibility of the material between strongly phase segregating (T below T_{ODT}) and weakly segregating (T above T_{ODT}). A series of insightful experiments has shown that pattern defect density can be greatly reduced by a thermal annealing sequence with a first stage at temperatures slightly above T_{ODT} , where polymer blocks intermix and melt defects, and subsequent cooling to below T_{ODT} , where the now more strongly immiscible materials self-organize and sharpen the domain interface (Δ) [95].

The T_{ODT} vs. degree of polymerization (N) phase diagram for a PS-b-PMMA diblock copolymer highlights an important limitation of this material [Figure 10(b)]. In creating this plot we have used the published functional form of $\chi = 0.028 + 3.9/T$ for PS-b-PMMA [123]. The weak dependence of χ on T means that T_{ODT} increases from below T_g to above T_{dec} over a very narrow

molecular weight range (around $N \sim 300$). In practice, then, it is impossible to thermally anneal pattern-forming PS-b-PMMA materials above T_{ODT} , and thus it is not possible to implement the two-step defect-reducing annealing sequence described above. A more desirable block copolymer patterning material would have a phase diagram similar to that of Figure 10(a), in which a strongly T -dependent χ ensures $T_g < T_{\text{ODT}} < T_{\text{dec}}$ over a broad range of molecular weights (N).

From the PS-b-PMMA T_{ODT} vs. N phase diagram and Equation (10), we calculate the minimum N for which $T_{\text{ODT}} > T_g$, thus allowing pattern formation to occur using standard thermal annealing. In addition, we also find a lower bound for $N_{\text{min}} \sim 300$, or [using Equation (7)], $M_{n\text{min}} \sim 30,000$ g/mol. In the strong segregation limit, Equation (6) takes the following form [150]:

$$L_0 = aN^{2/3}\chi^{1/6}, \quad (12)$$

from which we estimate $L_{0\text{min}} \sim 18$ nm for a lower limit to L_0 . Equation (12) overestimates the dimensions to which PS-b-PMMA scales because $N = 300$ PS-b-PMMA is more appropriately in the weak-segregation regime, such that $L_{0\text{min}}$ is almost certainly > 18 nm.

We have experimentally addressed the question of the ultimate extendibility of the PS-b-PMMA diblock copolymer material by systematically synthesizing and evaluating a series of polymers with decreasing molecular weights. Our study focused on vertically oriented cylindrical phase materials [see Figure 1(c)] with nominal molecular weight ratios of PS:PMMA $\sim 70:30$. We synthesized five different diblock copolymers with total M_n ranging from 38,000 to 130,000 g/mol and formed self-assembled films of vertically oriented PMMA cylinders in each material using the procedure outlined earlier. Top-down SEM images of two representative materials ($M_n = 67,000$ g/mol [Figure 10(c)] and $M_n = 38,000$ g/mol [Figure 10(d)]) confirm the scaling of both pore size and separation with M_n , with pore separation distance L_0 reaching a minimum of ~ 27 nm for the lowest M_n material synthesized. The target film thickness for achieving uniform self assembly (determined from ellipsometric measurements of films with uniform self-assembled patterns) also decreases with decreasing M_n . We measured L_0 for each material by AFM (atomic force microscopy) analysis of step heights for films forced into a terraced structure [163–166], and the relationship between L_0 and M_n is well described over this range by the power law relationship of Equation (6) with exponent $\delta \sim 0.77$ [Figure 10(e), solid circles]. This value differs from previously reported measurements of cylindrical phase films ($\delta \sim 0.58$ [17] and $\delta \sim 0.64$ [52]), and with previous neutron scattering measurements reporting $\delta \sim 0.65$ on lower-molecular-weight deuterated PS-b-dMMA [156]. Figure 10(e) also shows the characteristic dimension, L_0 ,

for three lamellar-phase PS-b-PMMA materials (open squares). The cylindrical and lamellar materials appear to follow a similar scaling law even though their fractional composition is different. Guided by the general theoretical arguments discussed above and using our extracted $\delta \sim 0.77$, we expect $M_n \sim 30,000$ g/mol (resulting in $L_0 \sim 24$ nm) to approach the minimum achievable dimension for thermally annealed PS-b-PMMA materials. At this dimension, however, the block interface width Δ is roughly 50% of the total domain width [Equation (11)].

Improved characteristics of self-assembling materials

Throughout this paper we have highlighted the favorable qualities of PS-b-PMMA block copolymers that make them attractive as sublithographic patterning materials. However, our discussion has also illuminated some concerns involving control of defects and ultimate scalability. Identification of advantageous material properties as well as limitations provides an important guide to the continued development of polymer self-assembly-based high-resolution patterning methods for high-performance semiconductor electronics. The discussion that follows gives our perspective on some important characteristics or conditions required of any improved block copolymer patterning material. We caution that this list is not exhaustive and represents our current point of view for applications within semiconductor electronics.

1. *All blocks of the block copolymer are soluble in a manufacturing-friendly common solvent.* This obvious requirement facilitates material deposition by spin-casting from solution using production tools.
2. *The polymer self-assembly process is initiated by thermal annealing.* Alternative self-assembly methods such as solvent annealing may provide distinct advantages over thermal processes; however, manufacturable solvent annealing processes have not yet been established in semiconductor device processing. Until such time, thermally processable materials stand the best chance for technology adoption. From a material property standpoint, therefore, we require $T_g < T_{\text{ODT}} < T_{\text{dec}}$ in order to access the relevant temperature phase space for efficient self assembly. For ease of processing of fully organic materials, we may desire $T_g \sim 20^\circ\text{C}$ (room temperature) for the removable block and $T_g \sim 100^\circ\text{C}$ for the permanent block in order to ensure a rigid pattern at room temperature. Preferably the material will have a large temperature window between T_g and T_{dec} .

3. *The self-assembled pattern formation process must be completed within a reasonable time.* Self assembly differs from lithographic methods in that wafers are batch-processed in parallel rather than serially, so that a direct time comparison with the lithographic exposure process is not entirely relevant. A more appropriate comparison might be with thermal oxidations which can take hours. A viable self-assembly process would have to be completed on this same time scale. Recent demonstrations of spin-coating polymer films in controlled vapor environments is one example of a method for speeding the assembly process, in some cases eliminating the need for any thermal processing [87].
4. *The polymer blocks are highly immiscible (i.e., a large χ at T_g) such that the condition for strong pattern formation ($\chi N \gg 10.5$) is met for small values of N .* This condition ensures self-assembly scalability to small pattern dimensions, as well as sharp (and smooth) interfaces in self-assembled patterns. As an example, one quantitative requirement might be $\chi > 0.1$ at T_g , which implies reasonable polymer-phase segregation for $N \sim 100$ (i.e., $\chi N \sim 10$ at T_g). Using Equations (6) and (12) from the previous section (which are valid only for PS-b-PMMA, although we use them here to provide a rough estimate), we calculate that patterns of materials with $N \sim 100$ will scale to dimensions of order $L_0 \sim 10$ nm.
5. *The interaction between polymer blocks (χ) is strongly T -dependent throughout the temperature range $T_g < T < T_{dec}$.* This requirement ensures the ability to thermally access both the disordered regime (i.e., $\chi N < 10.5$) and the strongly ordered regime ($\chi N \gg 10.5$) by adjusting T during a multi-stage thermal annealing sequence. In this process, which controls and reduces pattern defects, defects are melted during $T > T_{ODT}$ and then patterns are reordered in near-equilibrium conditions during slow cooling at $T < T_{ODT}$ [95].

We may quantitatively estimate desirable χ properties by considering the functional form of the polymer block interaction parameter χ . In general, $\chi = c_1 + c_2/T$ so that a strong T -dependence of χ is ensured by $c_2 \gg |c_1|$ throughout the relevant thermal processing range $T_g < T < T_{dec}$. We can specify an appropriately strong T -dependence by requiring $\chi N \sim 10$ at $T_g \sim 20^\circ\text{C}$ for $N \sim 100$ (condition 2) and also $\chi N \sim 10$ at $T \sim 200^\circ\text{C}$ for $N \sim 600$. In this example, we have selected a convenient annealing temperature of 200°C and a typical polymer M_n of $\sim 60,000$ g/mol ($N \sim 600$). By using these two

conditions on χN , we can estimate a desirable χ in the range of $\chi \sim -0.11 + (63/T)$. While this χ value is significantly different from that of PS-b-PMMA ($\chi_{\text{PS-b-PMMA}} = 0.028 + 3.9/T$) [123], there are other materials that more closely approach this specification (e.g., $\chi_{\text{PS-b-PEO}} = -0.007 + 21.3/T$ [167] and $\chi_{\text{PS-b-PVP}} = -0.033 + 63/T$ [125]).

6. *It must be possible to control the polymer self-assembled pattern orientation in both perpendicular and parallel orientations.* Perpendicular orientation of block copolymer domains is necessary for achieving template morphologies (both lamellar and cylindrical) suitable for pattern transfer processes, and achieving this orientation requires neutral block wetting of both the substrate and the free interfaces [15, 25]. We have also discussed the importance of preferential surface wetting by a single block (i.e., to promote parallel orientation) in self-aligned self-assembly processes. Selective-area surface treatments are an important means for specifying self-assembled pattern orientations on heterogeneous surfaces.
7. *Self-assembled polymer patterns must be rendered porous by selective removal of one polymer block.* A key attribute of PS-b-PMMA as a patterning material is the ability to solubilize the PMMA block while leaving the PS film intact [15]. The remaining PS template serves as a sacrificial mask for high-fidelity pattern transfer. Future block copolymer patterning materials must retain this attribute, although film developing may be accomplished by any of several means, for example, including chemical, thermal [87], dry-etch [10, 168], or ozone methods [4, 13].
8. *The self-assembled pattern provides a rugged template for subsequent pattern transfer.* This condition specifies important physical qualities such as high template aspect ratios as well as dense, chemically resistant template material composition.

New material directions

To our knowledge there is no existing block copolymer material that entirely satisfies this list of requirements. PS-b-PMMA block copolymers meet some of these conditions (1, 6, and 7) very well, are adequate to marginal in other categories (conditions 2, 3, 4, and 8), and fail remaining requirements (condition 5). Clearly there are many opportunities for innovation in designing next-generation self-assembled patterning materials. We devote the remainder of our discussion to describing recent material developments along these lines.

We have also been studying the favorable attributes of block copolymer materials containing *inorganic*

components, which may better meet the criteria for an optimal self-assembled patterning process. Inorganic-containing block copolymers are robust enough to withstand the conditions of pattern transfer methods such as plasma etching (condition 8), and there are other, less obvious, benefits to these materials as well. Inorganic-containing block copolymers can have strong immiscibility between blocks (i.e., a large χ), strengthening their propensity for phase separation and pattern formation. Large χ -values are necessary for scaling pattern dimensions to smaller sizes (condition 4) and for promoting sharply defined pattern features (condition 4); they also play a role in increasing the efficiency of the pattern-formation process (condition 3). Previous experiments have demonstrated sub-10-nm features in inorganic nanostructures incorporating surfactants or low-molecular-weight amphiphilic block copolymers [169].

The introduction of inorganic components into block copolymers can be accomplished by, for example, incorporating inorganic materials directly into the block copolymer synthesis (e.g., [170]). Earlier we mentioned one example of such a material, PS-*b*-PFS, in which the minority block contains iron and silicon. In this case the iron- and silicon-containing PFS domains provided excellent plasma etch contrast for silicon pillar fabrication [110] and also enabled the formation of small (~ 15 -nm) pattern elements using low- M_n materials ($M_n = 42,000$ g/mol). An alternative approach to organic-inorganic materials has been to incorporate sol-gel precursor materials into block copolymer solutions [171]. This technique allows the formation of silicon oxide nanostructured templates by incorporation of the sol-gel precursor material and subsequent thermal treatment. We have focused on a different method for incorporating silicon into block copolymer materials using inorganic precursor additions to the block copolymer solution [87].

Our organic-inorganic hybrid material comprises an organic PS:poly(ethylene oxide) diblock copolymer (PS-*b*-PEO) and a *separate* polymethylsiloxane (PMS) organosilicate precursor that is selectively miscible with PEO (and immiscible with PS). This material self-assembles by phase separation between PS and the combined PEO+PMS. In this case, the relative block ratio (and thus pattern morphology) can be tuned by adjusting the relative concentrations of PMS to PS-*b*-PEO, rather than by synthesizing an entirely new block copolymer with a different weight ratio. We have used this technique to form both cylindrical and lamellar patterns. An attractive feature of this material is the ease with which the self-assembled pattern can be developed (condition 7). A high-temperature annealing process (450°C) removes all organic components in the film (PS-*b*-PEO), leaving

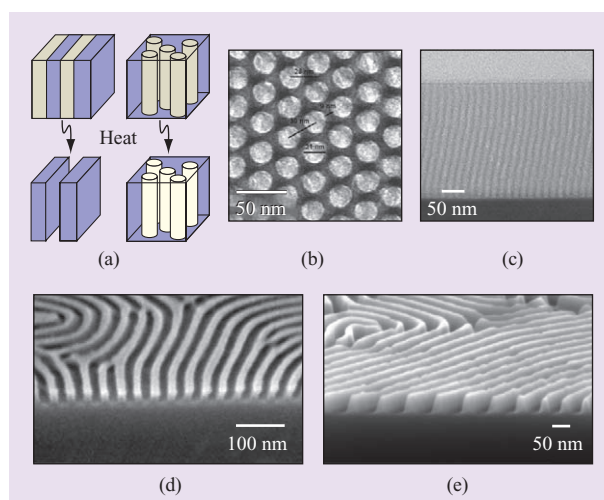


Figure 11

(a) Schematic representation of two organic-inorganic block copolymer phases converted to fully inorganic materials by heat treatment. (b) Top-down and (c) cross-sectional images of cylindrical-phase PS-*b*-(PEO+PMS) patterns after organic removal by thermal treatment. (d) 70-degree-angle SEM image of lamellar-phase PS-*b*-(PEO+PMS) pattern after organic removal by thermal treatment. (e) Etched silicon wires using PS-*b*-(PEO+PMS) pattern as mask. [Part (c) republished from [87] with permission. ©2005 American Chemical Society. Part (d) republished from [173] with permission. ©2006 American Institute of Physics.]

only cross-linked inorganic PMS features [shown schematically in **Figure 11(a)**].

We control pattern orientation of the PS-*b*-(PEO+PMS) hybrid material by tuning the interfacial energy at both substrate and air interfaces (condition 6) [87]. For example, we formed PMS films with vertically oriented cylindrical pores on both dense PMS underlayers with appropriate surface energy as well as Au surfaces [**Figures 11(b)** and **11(c)**]. The thermal stability of the nanoporous PMS makes these materials suitable templates for high-temperature growth of inorganic nanowires such as Ge or Si [172].

Perpendicularly oriented lamellar PS-*b*-(PEO+PMS) hybrid materials produce dense line/space patterns with ~ 20 nm half-pitch and ~ 40 nm height [**Figure 11(d)**] [173]. This image shows the fully developed inorganic PMS template after organic removal by thermal treatment. Quantitative analysis of similar SEM images gives an average pattern critical dimension of 22 nm and line roughness $3\sigma = 6$ nm. The roughness value is larger than the ITRS target for the 22-nm-technology generation; however, we may expect this roughness value to be reduced in well-aligned patterns that would not have long wavelength fluctuations.

The silicon-containing PS-b-(PEO+PMS) materials significantly improve the etch contrast of the self-assembled patterns (condition 8), which in turn simplifies nanostructure fabrication. Fabrication schemes using organic templates often incorporate oxide or nitride hard-mask processes and two-step etch procedures in order to achieve sufficient contrast [48, 174]. In this case the inorganic PMS template serves as the hard-mask material, so that structures such as silicon wire arrays are easily generated from lamellar material morphologies using a one-step plasma etch process [Figure 11(e)].

There has been widespread progress in the development of next-generation self-assembled patterning materials by many other academic and industrial groups. We devote our remaining discussion to selected examples of different approaches targeting materials that fulfill many of the requirements we have described above. Our selected examples are by no means an exhaustive list of all the exciting materials and developments in this active research area; there have been many other excellent recent subject reviews describing different materials aspects [2–7, 9, 10].

We have described PS-b-PMMA as a material with desirable attributes for high-resolution patterning, and several groups continue to explore enhancements to this base material system. One surprisingly straightforward method for improving aspects of PS-b-PMMA performance comes through blending small amounts of PMMA homopolymer together with the block copolymer. Mixing the proper blend of PS-b-(PMMA+PMMA) can produce self-assembled patterns with improved aspect ratios [175] as well as providing better etch resistance (condition 8). Combining this blending approach with selective cross-linking has also been demonstrated as a method for overcoming the size-scaling limitations of PS-b-PMMA imposed by χN [63, 64, 176].

Blending PS-b-PMMA diblock copolymers with small amounts of PS and PMMA homopolymers has resulted in significant advances in the combined self-assembly/chemical pre-patterning technique described earlier. In these examples (described briefly in an earlier section), lithographically predefined chemical patterns provide a template for the self assembly of a PS-b-PMMA film. The self-assembly process follows chemical templates of arbitrary shape if the proper amounts of homopolymer are added in advance; the idea here is that during film assembly the homopolymer materials migrate to regions of high pattern curvature, filling space as is necessary to complete the patterns [10, 116–118, 177, 178].

Many other organic block copolymer material choices are possible, and those consisting of highly immiscible blocks are particularly advantageous because of their potential for scaling to small dimensions (condition 3 above). For example, PS-b-PEO is a material known to

have high χ values, and it has been shown to form perpendicular cylindrical-phase patterns with low defect levels [89]. The tradeoffs that come with using the PS-b-PEO material include the lack of a convenient developing method (condition 7) and the need for a solvent-annealing process in a manufacturing-unfriendly solvent to obtain low defect levels (conditions 1 and 2). Recently, a particularly clever material design has addressed some of the issues with PS-b-PEO. Synthetic methods for new triblock copolymers composed of poly(styrene-*b*-methylmethacrylate-*b*-ethylene oxide) (PS-*b*-PMMA-*b*-PEO) have produced a material that combines the advantages of PS-*b*-PMMA (chemically developable) with those of PS-*b*-PEO (scalable to small dimensions and low defect density) [179]. This result nicely demonstrates the power of synthetic methods to target pre-specified desirable material properties.

The idea of designing functionality into constituent blocks of the block copolymer (demonstrated above for the PS-*b*-PMMA-*b*-PEO material) is attractive not only for addressing material shortcomings, but also for augmenting capabilities in entirely new ways. The best example of this approach has been the synthesis of a poly(α -methylstyrene)-*b*-poly(4-hydroxystyrene) (P α MS-*b*-PHOST) diblock copolymer [111]. In addition to its ability to form self-assembled patterns, this material also combines high-resolution resist chemistry into the block copolymer in such a way that it functions effectively as a deep-UV photoresist [7]. New materials such as these that are designed to target specific applications are exciting new research directions at the interface between lithographic and self-assembly approaches to patterning.

Summary

This review has described research efforts in IBM targeting the development and integration of polymer self-assembly processes as high-resolution patterning alternatives for high-performance semiconductor device applications. This powerful nontraditional patterning approach evokes the vision that critical integrated circuit elements could be made to “assemble themselves.” The research field is ripe with exciting progress, much of which we have attempted to highlight throughout the course of this review. Our discussion began with a summary of the self-assembly process in block copolymer materials, including important aspects for patterning such as control of pattern orientation and pattern transfer processes.

Self-assembled patterns provide sublithographic dimensions and high feature densities that facilitate material nanostructuring—a useful technique for controlled improvement of material properties. We have demonstrated the value of this approach in fabricating shallow-trench-array capacitors, controlled optical index

materials, nanoporous membranes, and nanocrystal Flash memories. Material enhancements arise from having many nanometer-scale elements operating within a single device, so that a lack of positional control in the self-assembly process does not degrade performance.

Polymer self assembly as a substitute for high-resolution lithography is a more challenging task, and we have described our efforts to develop self-assembly processes that provide sublithographic dimensions, pattern orientation, low defect density, and pattern registration. These are much loftier targets, and our discussion has been tempered with the difficult lithography requirements for future microelectronics generations. Perhaps the most exciting attribute of polymer self assembly is its ability to scale to successively finer dimensions through adjustment of fundamental material parameters, potentially providing a patterning solution suitable for several semiconductor technology nodes. We have described important material properties for dimensional scaling and have provided some estimates of the ultimate limits.

Our wish is that this review has conveyed our genuine excitement with the fundamental beauty of pattern formation by material self assembly as well as the prospects for its use in semiconductor technology. Clearly there is no shortage of innovative research ideas for further improving the technique as we continue to consider its application to high-performance microelectronics.

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