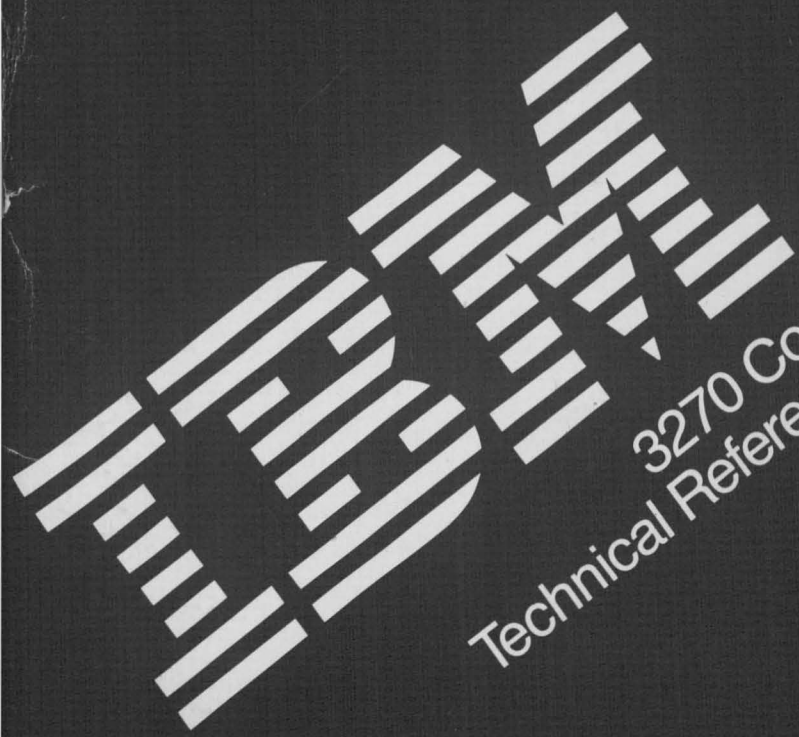
83X9705



3270 Connection Technical Reference

IBM 3270 Connection
Technical Reference

First Edition (April 1987)

The warranty terms and conditions applicable in the country of purchase in respect of an IBM product are available from the supplier. Please retain them with your proof of purchase.

No statements contained in this documentation shall affect the statutory rights of consumers.

CAUTION

This product is equipped with a 3-wire power cord and plug for the user's safety. Use this power cord in conjunction with a properly grounded electrical outlet to avoid electrical shock.

Notes:

Preface

This book provides interface information for the IBM 3270 Connection.

The information in this publication is intended for reference by hardware and software designers, programmers, engineers, and others who need to understand the design and operation of the IBM 3270 Connection.

Contents

Section 1. Introduction

The IBM 3270 Connection provides an interface allowing the Personal System/2 to emulate an IBM 3278/79 display station or an IBM 3287 printer.

The adapter card supports operation in the following modes:

- **3278/79 Emulation (CUT) Mode**

In CUT mode, the adapter emulates a 3278/79 display station, and 4K bytes of the buffer storage are available for screen display data. In other books CUT mode has been called 78E mode. The two names are equivalent. CUT stands for Control Unit Terminal.

- **3287 Emulation (87E) Mode**

In 87E mode, the adapter is configured as a 3287 printer. The buffer contains control unit input and output areas followed by a data communication area. In this mode, 4K bytes of the buffer storage are available to the user.

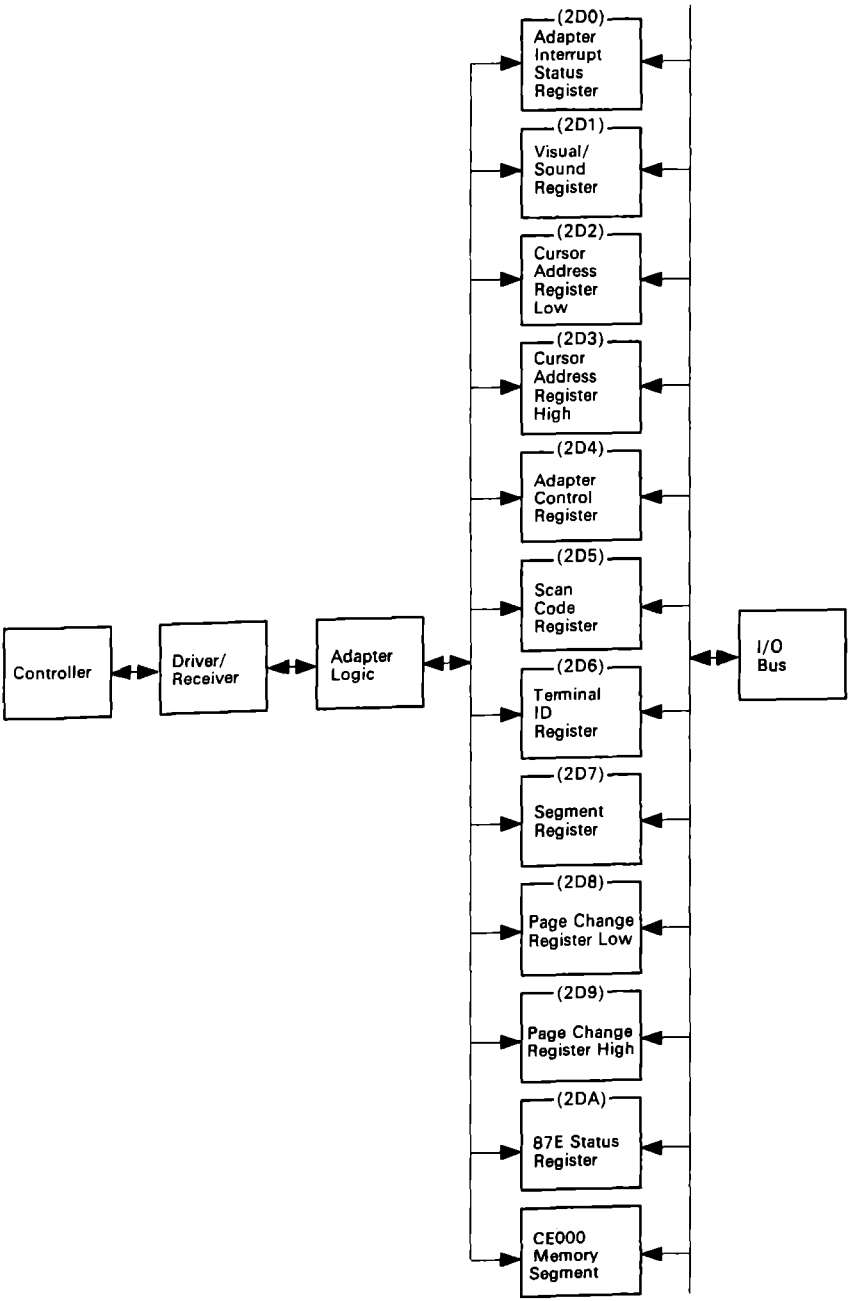
- **Distributed Function Terminal (DFT) Mode**

In DFT mode, the adapter operates as a DFT interface. The buffer contains control unit input and output areas followed by a data communication area. In this mode, 8K bytes of the buffer storage are available to the user.

This interface supports the 3270 data stream. It provides communication between the IBM Personal System/2 and the IBM 3274, 3276, and 3174 control units and the IBM 4321, 4331, 4361, and 4701 systems. The interface accepts, decodes, and executes commands issued from both the controller and the Personal System/2.

Logic Overview

The diagram on the next page is an overview of the relationship between the control unit, the adapter card, and your Personal System/2.


(2D0)
Adapter Interrupt Status Register
(2D1)
Visual/ Sound Register
(2D2)
Cursor Address Register Low
(2D3)
Cursor Address Register High
(2D4)
Adapter Control Register
(2D5)
Scan Code Register
(2D6)
Terminal ID Register
(2D7)
Segment Register
(2D8)
Page Change Register Low
(2D9)
Page Change Register High
(2DA)
87E Status Register
CE000 Memory Segment
Controller
Driver/ Receiver
Adapter Logic
I/O Bus

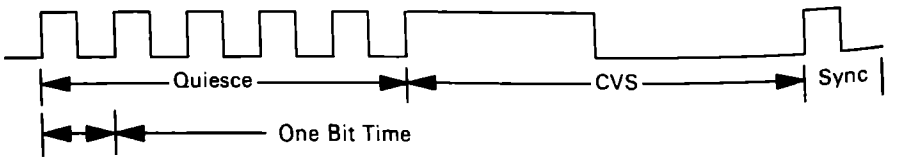
Transmission Formats

Each transmission of information between the control unit and the adapter consists of the following:

- A transmission start sequence.
- One or more data frames, where:
  - The number of frames varies with different transmissions.
  - Each frame consists of 12 bits.
  - The frames have one of three formats: command, data word, or status word.
- A transmission ending sequence.

Transmission Start Sequence (Code Violation Sequence)

The first bit sequences to be received and decoded by the adapter with any transmission are the quiesce sequences and code violation sequences (CVS). Therefore, before the adapter can convert the bi-phase line data to a binary form suitable for de-serializing, it must detect and decode this unique sequence of bits:



The quiesce sequence consists of five "1" bits followed by three half-bits of up level and three half-bits of down level. Following this sequence is the first bit of a data frame which is always a logical "1" bit and is called the sync bit. The adapter groups the incoming data bits into 12-bit data frames, each starting with a sync bit.

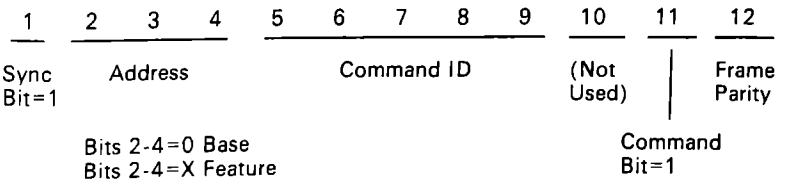
Data Frame Formats

All information sent over the coaxial cable between the control unit and the adapter is in one of the three formats described below.

Command Format

A command is sent only from the control unit, and is either a Read or a Write type.

The adapter's response to a Read command is either a status word or a data word. The response to a Write command is a Transmit Turnaround/Auto Response (TT/AR), which is also referred to as a clean or all-zero status response.

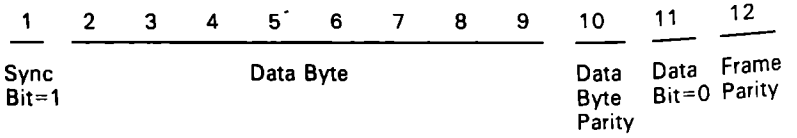


The valid commands are listed on page 2-1.

Data Word Format

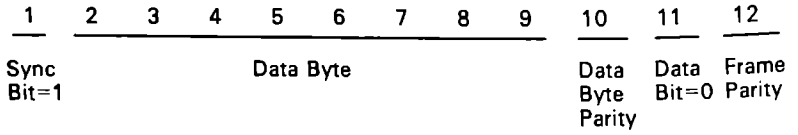
A data word can be sent from either the control unit or the adapter.

After the control unit has sent a Write command and received a TT/AR, it responds to the adapter with a data word. Similarly, the adapter responds to a Read command with a data word.



Status Word Format

A status word is sent from the adapter in response to a Poll command from the control unit.

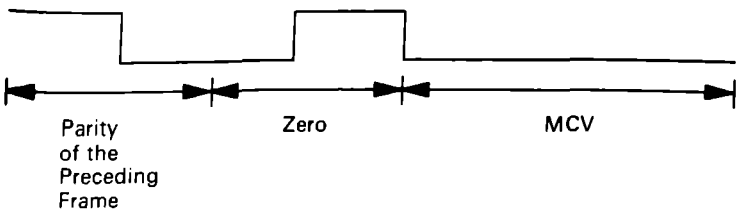


The status bits that may be set are listed below:

Status Condition	Meaning	Bit Setting
TT/AR	Clean response.	Bits 2 through 11 = 0
Poll request	Status is available in RAM.	Bit 6 = 1
Device check	Bad parity has been detected in RAM.	Bit 8 = 1
Operation complete	Busy command has completed.	Bit 9 = 1
POR complete	Power-on reset has been executed.	Bits 8 and 10 = 1
Feature error	Command has been received at other than base address.	Bit 11 = 1
Keystroke available	Keyboard scan code is on bits 2 through 9.	Bit 10 = 1

Transmission Ending Sequence (Mini Code Violation Sequence)

A transmission ending sequence signifies to the adapter the completion of a command/command data sequence. This ending sequence follows the last frame transmitted and consists of a zero bit followed by a mini code violation (MCV).



The MCV is equal to two bits with no mid-bit transition. Upon recognition of this ending sequence, the adapter initiates the appropriate response.

Transmit Turnaround/Auto Response (TT/AR)

The adapter always returns a TT/AR to the controller in response to any of the Write command/command data sequences. If transmission from the controller is good, the adapter responds within 5 microseconds of receiving the last bit of the ending sequence.

For Read commands, the driver/receiver (D/R) is set into transmit state. The adapter's response to Read commands is in the form of data bytes or a TT/AR.

Driver/Receiver Operation States

The driver/receiver on the adapter operates in three states:

- Disable state
- Receive state
- Transmit state.

Disable State

The adapter switches into disable state when the Personal System/2 sets the disable bit (bit 0 in the Connection adapter control register), or when the Personal System/2 is initially powered-on. In disable state the adapter ignores all controller commands sent over the coaxial cable and responds only to the Personal System/2. This causes the controller to time out and set the "go-to-sleep" latch in the control unit for that line, although polling continues. In this state, the controller responds only to a POR response sent by the Personal System/2 by means of the adapter.

Receive State

The adapter switches into receive state after a power-on reset (POR) sequence when the Personal System/2 has enabled the adapter, or after a transmit sequence when the adapter has just sent a poll response, a TT/AR, or data to the controller. In receive state, the adapter is able to accept any of the commands or data listed within this document. After a POR, or when the adapter returns to receive state after being disabled, the adapter resets its logic and prepares to execute the next command.

Transmit State

The adapter switches into transmit state after it has received a transmission ending sequence.

The adapter's responses to commands in transmit state are listed below:

Command Type	Valid Base 3270 Commands	Adapter Response
Read	Poll (Include priority)	Status
	Read Data	One byte of data
	Read Address Counter High	One byte of data
	Read Terminal ID	Terminal ID
	Read Multiple	One to four or 32 bytes of data (depending on the secondary control register)
	Read Status	Status
	Poll Acknowledge	TT/AR
	Read Address Counter Low	One byte of data
Write	Reset	TT/AR
	Load Address Counter High	TT/AR
	Clear	TT/AR
	Start Operation	TT/AR
	Load Control Register	TT/AR
	Write Data	TT/AR
	Insert Byte	TT/AR
	Search Forward	TT/AR
	Search Backward	TT/AR
	Load Address Counter Low	TT/AR
	Load Mask	TT/AR
	Load Secondary Control Register	TT/AR
	Diagnostic Reset	TT/AR

After its response, the adapter returns to receive state and waits for a new command/command data sequence.

Parity

Parity is generated and checked on all frames.

Generation

For all frames transmitted to the controller, the adapter generates even parity on bits 1 through 11 and inserts it into bit 12.

Checking

The adapter checks the parity on bits 1 through 11 of incoming frames. If bad parity is found, the adapter resets its logic and waits for another start sequence. It then fails to respond, forcing the controller to time out and enter an error recovery routine.

Status

Clean Status (TT/AR)

Clean status is an all-zero response from the adapter. It indicates to the controller any of the following conditions:

- There is no status to send.
- A Poll Acknowledge command was received, acknowledging the previously sent status.
- A transmission previously sent by the controller was received without error.

Nonclean Status

A nonzero response to a controller's Poll signifies that some kind of status is available. The adapter is notified that there is status available when the Personal System/2 sets the appropriate bit in the Connection adapter control register. The adapter then prepares a status frame to send to the controller in response to a Poll.

The status conditions that can be reported by the adapter are listed below:

Status Condition	Bit Setting	CUT Mode	87E Mode	DFT Mode
TT/AR	Bits 2 through 11 = 0	*	*	*
Poll request	Bit 6 = 1		*	*
Device check	Bit 8 = 1	*	*	*
Operation complete	Bit 9 = 1	*	*	
POR complete	Bits 8 and 10 = 1	*	*	*
Keystroke available	Bit 10 = 1	*		
Feature error	Bit 11 = 1	*	*	*

where * represents supported modes.

Power-On Reset (POR) Status

For CUT, 87E, and DFT modes, a POR response (bits 8 and 10 in the status word) is returned whenever the coaxial cable is enabled. In CUT mode a POR response will also be returned when a reset command has been received from the controller.

Section 2. Accepted Commands

Control unit commands recognized by the adapter are listed below:

Command Type	Valid Base 3270 Commands	Command ID (Frame Bits 5 through 9)	CUT Mode	87E Mode	DFT Mode
Read	Poll (include priority)	0 0 0 0 1	*	*	*
	Read Data	0 0 0 1 1	*	*	*
	Read Address Counter High	0 0 1 0 1	*	*	
	Read Terminal ID	0 1 0 0 1	*	*	*
	Read Multiple	0 1 0 1 1	*		*
	Read Status	0 1 1 0 1	*	*	
	Poll Acknowledge	1 0 0 0 1	*	*	*
	Read Address Counter Low	1 0 1 0 1	*	*	
Write	Reset	0 0 0 1 0	*	*	*
	Load Address Counter High	0 0 1 0 0	*	*	*
	Clear	0 0 1 1 0	*	*	
	Start Operation	0 1 0 0 0		*	*
	Load Control Register	0 1 0 1 0	*		
	Write Data	0 1 1 0 0	*	*	*
	Insert	0 1 1 1 0	*		
	Search Forward	1 0 0 0 0	*	*	
	Search Backward	1 0 0 1 0	*	*	
	Load Address Counter Low	1 0 1 0 0	*	*	*
	Load Mask	1 0 1 1 0	*	*	
	Load Secondary Control Register	1 1 0 1 0	*		*
	Diagnostic Reset	1 1 1 0 0			*

where * represents supported modes.

Note: The adapter responds to all good transmissions.

Read Commands

When a Read command is received by the adapter, the adapter places the requested data in its holding register. From there the data is inserted into a 12-bit frame and sent to the controller.

Poll

Upon receipt of a Poll command from the controller, the adapter switches into transmit state and sends a quiesce and CVS sequence to the controller. A status frame follows this sequence, with the status contained in bits 6 through 11 of the frame.

The adapter responds to a Poll command in the manner listed below:

	Frame Bits									
Response	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
POR complete	0	0	0	0	0	0	1	0	1	0
TT/AR	0	0	0	0	0	0	0	0	0	0
Keystroke available	X	X	X	X	X	X	X	X	1	0
Base status	0	0	0	0	X	0	X	X	0	X

Bit 6 = 1 Poll request (DFT and 87E modes only)
Bit 8 = 1 Device check (RAM parity error)
Bit 9 = 1 Operation complete
Bit 11 = 1 Feature error

where X represents variable data.

Multiple poll responses are stacked in the order of priority listed below:

1. Feature error (bit 11)
2. POR complete (special status code)
3. Base status (bits 6, 8, 9)
4. Keystroke available (including keyboard overrun)
5. Any other feature status.

Note: Multiple base status bits may be returned in a poll response.

If device check (base status bit 8) is returned to a Poll and acknowledged, the setting of the device-check bit is inhibited until a Write command is executed in CUT or DFT modes, or any command is executed in 87E mode.

Read Data

The Read Data command is normally sent to the adapter after a Load Address Counter Low or Load Address Counter High command has been sent to load the adapter cursor address register. Upon receiving the Read Data command without error, the adapter reads the data as described for Read commands on page 2-2.

Data wraparound in the buffer occurs at address 64K only, regardless of how much of the buffer is implemented. Data read from unimplemented RAM is all "1's" (that is, good parity). If data is accessed from the RAM with bad parity, device check is set, if not already inhibited.

Read Address Counter High

The adapter responds to this command with the high-order byte of the address counter.

In DFT mode, this command is ignored.

Read Terminal ID

When the Read Terminal ID command and ending sequence are received by the adapter, it switches into transmit state.

The adapter then returns the following response to the controller:

CUT Mode Response:

Frame Bits	Contents
Bits 2-5	Keyboard ID
Bits 6-8	Terminal ID
Bit 9	0

87E Mode Response:

Frame Bits	Contents
Bits 2-8	0 0 0 0 0 0 0
Bit 9	1

DFT Mode Response:

Frame Bits	Contents
Bits 2-8	0 0 0 0 0 0 0
Bit 9	1 (device ID available in buffer)

In DFT mode, the reception of this command causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

In 87E mode, the reception of this command causes the operation-complete and feature-error bits (bits 9 and 11 of the status word) to be reset.

Read Multiple

The adapter's response to the Read Multiple command follows much the same pattern as that of the Read Data command (see page 2-3), except that the adapter can send up to 32 consecutive data frames in response to the Read Multiple command from the controller. Therefore, up to 32 bytes of data can be transferred back to the controller. If, however, the "read-32" bit of the adapter secondary control register is "0" (the default), this command is limited to 4 bytes of data. If it is "1," then 32 bytes are allowed.

Data wraparound in the buffer occurs at address 64K only, regardless of how much of the buffer is implemented. Read data from unimplemented RAM is all "1's" (that is, good parity). If data is accessed from the RAM with bad parity, device check is set, if not already inhibited. If bad data is received by the controller in any of the data bytes, the controller re-initializes the whole sequence.

In 87E mode, this command is ignored.

Read Status

The adapter responds to this command in CUT and 87E modes in the manner listed below:

Frame Bits	1	2	3	4	5	6	7	8	9	10	11	12
	1	0	0	X	0	0	X	X	0	0	0	X

Bit 4 = 1	Not busy
Bit 7 = 1	Feature error
Bit 8 = 1	Operation complete

where X represents variable data.

In DFT mode this command is ignored.

Poll Acknowledge

The controller acknowledges the return of a nonzero status by responding with a Poll Acknowledge command. The adapter then sends a clean status response (TT/AR) and waits for the next command from the controller.

If the adapter receives a second Poll command instead of a Poll Acknowledge (that is, the status was received in error by the controller) it returns the same status to the controller. This continues until a Poll Acknowledge is received or an error threshold is reached by the controller.

If further status becomes available before a Poll Acknowledge is received for the first status that was sent, this status is stacked by the adapter. It is not sent to the controller until the adapter receives a Poll Acknowledge for the first status that was sent. Poll and Poll Acknowledge continue until the adapter has no further status to return to the controller.

In CUT mode the transfer of a keystroke followed by a Poll Acknowledge to the controller causes a keystroke-accepted interrupt to be sent to the Personal System/2. Interrupt occurs if the mask bit is off.

A Poll Acknowledge command containing a sound alarm or enable/disable clicker in CUT mode, or enable/disable operation in 87E mode causes the visual/sound-register-updated interrupt to be sent to the Personal System/2. Interrupt occurs if the mask bit is off.

Read Address Counter Low

The adapter responds to this command with the low-order byte of the address counter in both CUT and 87E modes.

In DFT mode, this command is ignored.

Write Commands

When the adapter receives a Write command from the controller, and a data word is expected but no end of message (EOM) is received, the adapter evaluates the next frame to determine whether it is another command or data.

If the next frame is another command, the adapter acts accordingly for that command and disregards the previous command. For command/data sequences, the adapter sends the data to its assigned address, increments the cursor address register by one (for a Write Data command), and responds to the ending sequence with a TT/AR. For command and data frames that are separate, the adapter returns a TT/AR after the command and ending sequence are received.

Reset

When the adapter receives a Reset command, it sets the Reset-command-decoded bit (bit 1 in the Connection adapter interrupt status register) and interrupts the Personal System/2 if the mask bit is off. RAM is not disturbed. The cursor register is set to hex 0050 in CUT or DFT mode, and 0000 in 87E mode.

In DFT and 87E modes the coaxial cable is disabled when the reset command is received. (Bit 0 of control register 2D4 is set to zero.) The adapter then responds to the controller with a TT/AR.

The adapter is able to accept two or more Reset commands (without intervening Poll commands) and respond with a single POR response to a subsequent Poll.

The Reset command is issued only during an error recovery and a controller initial microcode load sequence.

Load Address Counter High (LACH)

This is similar to the LACL command (see page 2-14), except that the data is loaded into the high-order byte of the cursor address register, rather than the low-order byte.

In CUT mode the decode of a Load Address Counter High followed by a data byte causes the Load-I/O-Address-command-decoded interrupt to be sent to the Personal System/2. Interrupt occurs if the mask bit is off. This interrupt can be disabled when the cursor is inhibited if the conditional-interrupt-disable bit (bit 6 in the Connection adapter control register) is set.

Clear

The Clear command is used to clear the storage area containing the indicator character codes. It is also used to clear all or part of the buffer storage to nulls. A byte of data, called the pattern byte, is transmitted following the Clear command. The adapter uses the pattern byte in conjunction with the previously loaded mask to terminate the clear function. The cursor address register is used to indicate the point at which the clear function starts. All locations including the starting address, up to – but not including – the location containing the byte that matches the pattern and mask, are tested and cleared. Upon completion, the address counter points to the matching location, and the operation-complete bit is set in the poll response status word. Prior to setting operation complete, the device is "busy" and its response to a Poll is a TT/AR. The command terminates at address zero (without clearing address zero) if no match occurs.

If a buffer parity error is detected, device check (bit 8 of the status word) is set (if not inhibited by a previous parity error). The clear operation does not terminate prematurely if a buffer parity error is detected.

In CUT mode, the presence of a pattern byte following the decode of this command sets the buffer-being-modified status bit (bit 6 in the Connection adapter interrupt status register). The termination of this command resets the buffer-being-modified status bit and causes a base-buffer-modified interrupt to be sent to the Personal System/2. Interrupt occurs if the mask bit is off.

Commands other than Poll, Reset, and Read Status, sent by the controller while the adapter is busy, are ignored.

In DFT mode, this command is ignored.

Start Operation

In DFT mode, a Start Operation command is decoded by the adapter. The adapter sends a TT/AR back to the controller which then sends a Start-Operation-command-decoded interrupt to the Personal System/2. Interrupt occurs if the mask bit is set off. The adapter operates similarly in 87E mode, with two exceptions:

- No action is taken by this command if there is any pending poll status.
- The setting of the interrupt also causes the enable bit in the 87E status register to be set.

In either 87E or DFT mode, the completion of the Start Operation command causes the Personal System/2 to post status available in the Connection adapter control register along with the appropriate status codes in the I/O buffer. An indication that status is now available is sent to the controller upon receipt of a Poll command. This causes the controller to read the part of storage holding the status.

In CUT mode, the decode of a Start Operation command is treated as a spare command.

Load Control Register

The Load Control Register command causes the adapter to load the next data word into the Connection adapter control register. The Connection adapter control register is set to all zeros by POR and Reset commands but otherwise unaffected by hardware.

The function of each bit in the load control register is listed below:

Frame Bits	Function
Bit 2=0	80 characters per line
Bit 2=1	132 characters per line
Bit 5=1	Inhibit feature step of I/O address counter
Bit 7=1	Inhibit cursor display
Bit 8=1	Reverse image cursor
Bit 9=1	Blink cursor

Bit 5 is set and reset by the Load Control Register command to allow program compatibility. However, since no features are implemented, no function is performed by this bit. Bit 7, when set by the controller, prevents the cursor symbol from flashing on the screen at other than its proper location. Bit 8 causes the display of the cursor as a reversed image of the associated character box. Bit 9 causes the cursor to blink.

In CUT mode, the decode of the Load Control Register command followed by a data byte causes a visual/sound-register-updated interrupt to be sent to the Personal System/2. Interrupt occurs if the mask bit is off.

In DFT and 87E modes, this command is ignored.

Write Data

When a Write Data command/data sequence is received from the controller followed by an ending sequence, the adapter responds to the command with a clean status response (TT/AR) and sends the data to an address in the on-card I/O buffer. After a command/data/ending sequence has occurred, further data transmission need not be preceded by a Write Data command if the last command received was a Write Data command.

Data wraparound in the buffer will occur at address 64K only, regardless of how much of the buffer is implemented. Data written to unimplemented RAM is lost.

In CUT mode, the first data word following the decode of a Write Data command sets the buffer-being-modified bit (bit 6 in the Connection adapter interrupt status register). On completion of a Write Data command (decode of any other type command) a base-buffer-modified interrupt is sent to the Personal Interrupt occurs if the mask bit is off.

Insert

The Insert command causes the display to accept the next data word and place it in the buffer storage at the location indicated by the current value of the address counter. The original contents of the storage location are then shifted one location ahead. This sequence continues for each successive location until a null character or attribute is found, or the I/O address counter steps to zero (in which case the character that formerly resided in the last addressable location of storage is lost).

In CUT mode, the presence of the data byte following the decode of the Insert command sets the buffer-being-modified bit (bit 6 in the Connection adapter interrupt status register). The termination of this command resets the buffer-being-modified status bit, and a base-buffer-modified interrupt is sent to the Personal System/2. Interrupt occurs if the mask bit is off.

Only one data word may follow this command. During the time that shifting takes place, the display is "busy." Refer to the description of the Clear command on page 2-8. The operation-complete bit (bit 9 of the status word) is set when this command is completed. At that time, the address counter points to the last character moved. If, however, the command has terminated at an attribute, the address counter points to the attribute, and the character that was located ahead of the attribute is lost.

The insert operation does not terminate prematurely if a buffer parity error is detected.

Upon completion of the Insert command, the mask register and pattern register contain unusable information and must be reloaded by the controller microcode prior to the next Search or Clear command.

In DFT and 87E modes, this command is ignored.

Search Forward

The Search Forward command, when followed by a pattern data byte, causes the adapter to search each buffer storage location, starting at the current value of the address counter, until a byte that matches the mask and pattern is found.

The address counter contains the value of the address in storage of the first matching byte found. If no matching byte is found, the Search command terminates at address zero.

If this command is issued in DFT mode, the adapter ignores it and returns a TT/AR.

Search Backward

The Search Backward command operates in a similar manner as the above Search Forward command. If no byte matching the mask and pattern is found, the search terminates at one location past address zero. (All address bits that have been implemented are set to "1.")

If this command is issued in DFT mode, the adapter ignores it and returns a TT/AR.

Note: The two Search commands indicate the completion of the operation by setting bit 9 in the status word response to a Poll command. While the search is in progress, the display is "busy." Refer to the description of the Clear command on page 2-8. A buffer parity error detected during a search memory cycle causes the search to terminate, and the address counter points to the location containing the byte with bad parity. Operation complete (bit 9 of the status word) is set, and device check (bit 8 of the status word) is set if not inhibited by a previous device check.

Load Address Counter Low (LACL)

This command, when sent by the controller, is normally followed by a data frame containing an address byte. The address byte is then loaded into the low-order byte of the 16-bit storage cursor address register of the adapter.

In CUT mode, the decode of a Load Address Counter Low command followed by a data byte causes the load-I/O-address-command-decoded interrupt to be sent to the Personal System/2. Interrupt occurs if the mask bit is off. This interrupt can be disabled when the cursor is inhibited if the conditional-disable interrupt bit (bit 6 of the Connection adapter control register) is set.

Load Mask

The Load Mask command causes the adapter to load the next data byte into the mask register. The mask is used in conjunction with subsequent Search and Clear commands. Any "1" bits in the mask indicate that bits in the buffer are to be compared with the pattern byte (the byte of data following the Clear command). A mask of all "0" bits prohibits a pattern test from being satisfied and causes the Clear or Search Forward commands to terminate at address zero and the Search Backward command to terminate at address 4K (or the first address encountered with bad parity).

In DFT mode this command is ignored.

Load Secondary Control Register

The decode of the Load Secondary Control Register command loads the value of the read-32 bit of the adapter secondary control register into a latch.

Subsequent Read Multiple commands interpret this bit in the manner described below:

Read-32 Bit = 0 Terminate Read Multiple command when 0 to 4 bytes have been read.

Read-32 Bit = 1 Terminate Read Multiple command when 0 to 32 bytes have been read.

Diagnostic Reset

In DFT mode, the decode of the Diagnostic Reset command causes the adapter to respond to the controller with a TT/AR. The adapter sets the diagnostic-command-decoded bit (bit 2 in the Connection adapter interrupt status register) and interrupts the Personal System/2 if the mask bit is set off.

In CUT and 87E modes, the decode of a Diagnostic Reset command is treated as a spare command.

Section 3. Personal System/2 Address Locations

The following I/O mapped addresses are defined:

Base Address Hex	Low Address Bits	Personal System Registers	Personal System Read	Personal System Write
2D0	0 0 0 0	Connection Interrupt Status	Data	Reset Mask
2D1	0 0 0 1	Visual/Sound	Data	Reset Alarm
2D2	0 0 1 0	Cursor Address (Bits 7-0)	Data	----
2D3	0 0 1 1	Cursor Address (Bits 15-8)	Data	----
2D4	0 1 0 0	Connection Control	Data	Data
2D5	0 1 0 1	Scan Code	----	Data
2D6	0 1 1 0	Terminal ID	----	Data
2D7		Reserved		
2D8	1 0 0 0	Page Change Low	Data	Reset Mask
2D9	1 0 0 1	Page Change High	Data	Reset Mask
2DA	1 0 1 0	87E Status	Data	Reset Mask
2DB		Reserved		
2DC		Reserved		
2DD		Reserved		
2DE		Reserved		
2DF		Reserved		

Section 4. Personal System/2 Registers

This section contains a description of each register in the interface (addresses hex 2D0 through 2DA), and a description of the bits within those registers.

3270 Connection Interrupt Status Register (Hex 2D0)

This is an 8-bit register internal to the adapter and accessed by the Personal System/2. Bits 0 through 5 are interrupt bits set by the adapter and bits 6 and 7 are status bits set by the adapter. Bits 0 through 5 are reset by the Personal System/2 under mask at the same address from which the status is read. A write to the 3270 Connection interrupt status register resets bits 0 through 5 only when the corresponding data bit is sent on the Micro channel® data bus. Bits 6 and 7 are reset by the adapter.

In order to prevent "missing" status bits, the software should read the register, write that value back to the hardware, and then proceed to service the cause of the interrupt.

A description of each bit in the 3270 Connection interrupt status register is listed below:

Bus Bit	Bit Type	Meaning	CUT Mode	87E Mode	DFT Mode
0	I	Keystroke accepted	*		
0	I	Start Operation command decoded		*	*
1	I	Reset command decoded	*	*	*
2	I	87E register status available		*	
2	I	Visual/Sound register updated	*		
2	I	Diagnostic Reset command decoded			*
3	I	Read Terminal ID command decoded			*
4	I	Base buffer modified complete	*		
5	I	Load Address Counter command decoded	*		
6	S	Buffer being modified	*		
7	S	Interrupt generated	*	*	*

where I represents an interrupt bit, S represents a status bit, and * represents supported modes.

Note: Interrupt level-2 should be used by the interface module.

Keystroke Accepted (Bit 0)

In CUT mode, this bit is set by the adapter when a keystroke is acknowledged by the controller, and reset by the Personal System/2. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

Start Operation Command (Bit 0)

In DFT and 87E modes, this bit is set by the adapter when a Start Operation command is received, and reset by the Personal System/2. If a Start Operation command is received in 87E mode when a poll status is pending, this bit will not be set. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

Reset Command (Bit 1)

This bit is set when a Reset command is received by the adapter, and reset by the Personal System/2. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

87E Register Status Available (Bit 2)

In 87E mode, this bit is set when the enable/disable operation has been decoded in a Poll command, and reset by the Personal System/2. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

Note that if the enable-operation bit (bit 7 of the 87E status register) is set by a Start Operation command, the interrupt is caused by the decode of a Start Operation command, not 87E status available.

Visual/Sound Register Updated (Bit 2)

This bit is set when a 3270 Connection control register command is received by the adapter or when the sound alarm enable/disable clicker has been decoded in a Poll command, and reset by the Personal System/2. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

Diagnostic Reset Command (Bit 2)

In DFT mode, this bit is set when a Diagnostic Reset command is received by the adapter, and reset by the Personal System/2. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

Read Terminal ID Command (Bit 3)

In DFT mode, this bit is set when a Read Terminal ID command is received by the adapter, and reset by the Personal System/2. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

Base Buffer Modified Complete (Bit 4)

In CUT mode, this bit is set by the adapter at the end of the hardware power-on sequence. It is set by the adapter on termination of a Write command (termination determined by decode of the next command), or on termination of a Clear or Insert command (termination determined by an operation complete status within the adapter). The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off.

Load I/O Address Command (Bit 5)

In CUT mode, this bit is set when either a Load I/O Address High or Load I/O Address Low command is received by the adapter, and reset by the Personal System/2. The setting of this bit causes an interrupt to the Personal System/2 if the mask-interrupt bit is set off. This interrupt may be disabled by setting the inhibit-cursor bit (bit 3 in the visual/sound register) if the conditional-inhibit-disable bit (bit 6 in the 3270 Connection register) is set.

Buffer Being Modified (Bit 6)

In CUT mode, this status bit is set and reset by the adapter. It indicates to the Personal System/2 that the I/O buffer is being modified by a Write Data, Clear, or Insert command.

Interrupt Generated (Bit 7)

This status bit is set by the adapter as the result of an interrupt and an interrupt-enabled condition. It is reset by the Personal System/2 when it resets the interrupt bits, or by the adapter when the mask bit is set off.

Visual/Sound Register (Hex 2D1)

In CUT mode this register is set and reset by the adapter, except for the sound alarm bit (bit 6), which is reset by the Personal System/2 by any write to this register with any data. No other bits are affected by a write to this address. Each time this register is loaded by the adapter, the visual/sound-register-updated bit (bit 2 in the 3270 Connection interrupt status register) is set.

A description of each bit in the visual/sound register is listed below:

Bus Bit	Meaning	Frame Bit Equivalent
0	Characters per line Bit 0 = 0 80 characters per line Bit 0 = 1 132 characters per line	
1	Inhibit feature step of address counter	
2	Inhibit display	Frame bit 6
3	Inhibit cursor	Frame bit 7
4	Reverse cursor	Frame bit 8
5	Blink cursor	Frame bit 9
6	Sound alarm	
7	Clicker enabled	

Cursor Address Register (Hex 2D2 and 2D3)

This 16-bit register is internal to the adapter and requires two addresses. It is set by the adapter and can be read by the Personal System/2.

This register contains the current value of the address counter (bits 15 through 0) and, in CUT mode, it indicates the location of the cursor.

3270 Connection Control Register (Hex 2D4)

This is an 8-bit read/write register accessed by the Personal System/2 (internal to the adapter), requiring one address to read and write.

A description of each bit in the Personal System/2 control register is listed below:

Bus Bit	Meaning	CUT Mode	87E Mode	DFT Mode
0	Coaxial cable enable	*	*	*
1	CUT/DFT mode Bit 1 = 0 CUT mode Bit 1 = 1 DFT mode	0	0	1
2	87E mode	0	1	0
3	Keystroke available	*		
4	Request poll		*	*
5	Test	*	*	*
6	Reset cursor		*	
6	Conditional interrupt disable	*		
7	Disable interrupt	*	*	*

where * represents supported modes.

Coaxial Cable Enable/Disable (Bit 0)

This bit is initially reset during hardware power-on. It is also reset by the Personal System/2 or by the Reset command in DFT or 87E mode. When reset, the adapter is disabled and unable to send any responses to the controller. This causes the controller to timeout and set the "go-to-sleep" latch for that line. The controller, however, continues to poll the line but ignores all responses sent to it, with the exception of a POR response. A POR response will always be returned in response to the first poll after the coaxial cable is enabled.

This bit is set by the Personal System/2 application, causing the adapter to become enabled and on the line.

CUT/DFT Mode (Bit 1)

When the Personal System/2 sets this bit, the adapter operates as a DFT interface. When it is reset, the adapter emulates a 3278 display station or a 3287 printer. This bit may not be changed

87E/CUT Mode (Bit 2)

For this bit to be set, CUT mode must also be set (bit 1 = 0). When this bit is set the adapter is configured as a 3287 printer.

This bit may not be changed while the coaxial cable is enabled.

Keystroke Available (Bit 3)

When set by the Personal System/2 in CUT mode, this bit tells the adapter that the scan code register has been loaded. The data is then treated as a keystroke. This bit is reset by a Poll Acknowledge or Reset command from the controller.

This bit should be used only in CUT mode.

Request Poll (Bit 4)

This bit is set by the Personal System/2 and causes the poll-request bit (frame bit 6) to be returned to the next poll response sent to the controller. This bit is reset by the Poll Acknowledge command sent by the controller. If a Reset command is received by the adapter before any pending status is returned to the controller, the status is reset.

Test (Bit 5)

This bit is set by the Personal System/2 in CUT mode. When set, it allows the Personal System/2 to do wrap-testing of data from the scan code register to RAM location zero. The coaxial cable is automatically disabled and commands or data can be transmitted to check the adapter function.

Reset Cursor (Bit 6)

When this bit is set, a reset is continually applied to the cursor register. Because this bit is valid only in 87E mode, the cursor is forced to reset to hex 0000.

Conditional Interrupt Disable (Bit 6)

When this bit is set in CUT mode, load-I/O-address-command-decoded interrupts are disabled whenever the inhibit-cursor bit (bit 3 of the visual/sound register) is set. This prevents the setting of the load-I/O-address-decoded bit (bit 5 of the 3270 Connection interrupt status register).

Disable Interrupts (Bit 7)

This bit is set during the hardware power-on cycle by the Personal System/2, and reset by the Personal System/2. The setting of this bit inhibits all interrupts (bits 0 through 5 in the 3270 Connection interrupt status register) from being sent to the Personal System/2, but does not prevent these interrupt-status bits from being set. If one of the interrupts is set when the mask bit is on, the subsequent removal of the mask bit allows that interrupt to pass through to the Personal System/2.

Scan Code Register (Hex 2D5)

This is an 8-bit register internal to the adapter. It is set and reset by the Personal System/2.

In CUT mode, this register is used by the Personal System/2 to send a keystroke code to the controller. The Personal System/2 must not change the contents of this register if the keystroke-available bit (bit 3 of the 3270 Connection control register) is set.

Note: The scan code placed in this register must be the one's complement of the data to be transmitted to the controller.

Terminal ID Register (Hex 2D6)

This is an 8-bit register internal to the adapter. It is set by the Personal System/2 during the hardware power-on cycle prior to enabling the coaxial cable, and reset by the Personal System/2.

The adapter's response to bits set in the terminal ID register is listed below:

CUT Mode Response:

Bits 4 through 7	Keyboard ID	
Bits 1 through 3	3278/79 Model	
	For Model 2	0 1 0
	For Model 3	0 1 1
	For Model 4	1 1 1
	For Model 5	1 1 0
Bit 0	0	

DFT Mode Response:

Bits 1 through 7	0 0 0 0 0 0 0
Bit 0	1 (device ID available in buffer)

87E Mode Response:

Bits 1 through 7	0 0 0 0 0 0 0
Bit 0	1 (device ID available in buffer)

The contents of these locations should remain unchanged while the terminal is powered-on.

Note: The terminal ID placed in this register must be the one's complement of the data to be sent to the controller.

Page Change Register Low (Hex 2D8)

This register contains one bit for every 256 bytes of buffer space of the low buffer space. When a bit is set by the adapter, it indicates that a Write command or a Personal System/2 memory write has modified at least one location within the corresponding 256-byte page of the buffer.

The buffer locations that correspond to each bit are listed below:

Personal System/2 Data Bit	Buffer Locations Hex	Decimal
0	0- FF	0- 255
1	100-1FF	256- 511
2	200-2FF	512- 767
3	300-3FF	768-1023
4	400-4FF	1024-1279
5	500-5FF	1280-1535
6	600-6FF	1536-1791
7	700-7FF	1792-2047

Bits are reset under mask by a Write command to the same address (a bit is reset if the corresponding Micro channel® data bus bit is "1").

Page Change Register High (Hex 2D9)

This register contains one bit for every 256 bytes of buffer space of the high buffer space. When a bit is set by the adapter, it indicates that a Write command or a Personal System/2 memory write has modified at least one location within the corresponding 256-byte page of the buffer.

The buffer locations that correspond to each bit are listed below:

Personal System/2 Data Bit	Buffer Locations Hex	Decimal
0	800-8FF	2048-2303
1	900-9FF	2304-2559
2	A00-AFF	2560-2815
3	B00-BFF	2816-3071
4	C00-CFF	3072-3327
5	D00-DFF	3328-3583
6	E00-EFF	3584-3839
7	F00-FFF	3840-4095

Bits are reset under mask by a Write command to the same address (a bit is reset if the corresponding Micro Channel® data bus bit is "1").

87E Status Register (Hex 2DA)

This register is used for 87E-printer-unique functions. Bits are set by hardware and reset under mask by the Personal System/2 (a write to hex 2DA with the data bit on resets that bit). The Personal System/2 may read this register at hex 2DA of I/O space.

The function of each bit is listed below:

Bus Bits	Function
0 through 4	Not used
5	87E sound alarm
6	Disable operation
7	Enable operation

The 87E-sound-alarm bit (bit 5) is set by the coaxial cable by a Poll. This is similar to CUT mode, but does not require reading the visual/sound register as well as the 87E status register.

The disabled-operation bit (bit 6) is set by a Poll or Poll Acknowledge. When this bit is set, it causes printer emulation tc stop internal operation within 10 milliseconds, and causes the cursor register to reset to hex 0000. The adapter returns operation complete to the control unit when the disable bit is reset by the Personal System/2.

The enable-operation bit (bit 7) is set by the coaxial cable commands Start Operation, and Poll or Poll Acknowledge. It is reset by the Personal System/2.

Hardware Power-On and the 3270 Connection Interrupt Status Register

A power-on sequence is initiated by the Personal System/2 when the reset line on its Micro Channel® system bus is activated.

A hardware power-on sequence puts the adapter into 3278/79 emulation mode, disables the coaxial cable, and sets the mask interrupt. At the start of this sequence, the first 4K bytes of RAM are cleared and the buffer-being-modified bit (bit 6 of the 3270 Connection interrupt status register) is set. At completion of the power-on sequence, buffer being modified is reset and the base-buffer- modified bit (bit 4 in the 3270 Connection interrupt status register) is set.

Register Condition after Hardware POR Cycle

The contents of adapter registers after a POR cycle are listed below:

Register	Bit Settings 7	6	5	4	3	2	1	0
3270 Connection Interrupt Status	0	0	X	1	X	X	X	X
Visual/Sound	X	0	0	0	0	0	0	0
Cursor Address (High Order)	X	X	X	0	0	0	0	0
Cursor Address (Low Order)	0	1	0	1	0	0	0	0
3270 Connection Control	1	0	0	0	0	0	0	0
Scan Code	X	X	X	X	X	X	X	X
Terminal ID	X	X	X	X	X	X	X	X
Page Change (Low Order)	X	X	X	X	X	X	X	X
Page Change (High Order)	X	X	X	X	X	X	X	X
87E Status	X	X	X	X	X	X	X	X

where X represents unknown contents.

Section 5. Programming the IBM 3270 Connection in CUT Mode

How to Use This Section

This section contains information that you will need in order to write application programs using the IBM 3270 Connection adapter card. In order to write Personal System/2 programs to support this card, a detailed knowledge of controller data stream programming is required.

Related Publications

In order to properly use this section, you should be familiar with the information in the following manuals:

- *IBM 3270 Character Set Reference*, GA27-2837

  This manual lists all character sets and keyboard layouts.

- *IBM 3270 Information Display System: 3274 Control Unit Description and Programming Guide*, GA23-0061

- *IBM 3270 Information Display System: 3174 Control Unit Functional Description*, GA23-0218

- *IBM 3270 Information Display System Data Stream Programmer's Reference*, GA23-0059-2

The following manuals may also prove useful:

- *IBM 3270 Information Display System: Introduction*, GA27-2739

- *IBM 3270 Information Display System: Installation Manual—Physical Planning*, GA27-2787

- *IBM 3270 Information Display System: IBM 3299 Terminal Multiplexer Product Information*, G520-4216

CUT Mode Programming

Control unit terminal (CUT) operation relies on the controller interacting with the IBM 3270 Connection adapter card in much the same way as it does with a hardware display terminal. This is necessary in order to support the many old model controllers in use. The controller uses this buffer based upon host I/O instructions and orders.

Note: Examples in this section assume a controller configured to handle a 3278 Model 2 terminal with a typewriter keyboard. The Model 2 terminal displays up to 24 lines of data, 80 characters in width, and the Operator Information Area status line.

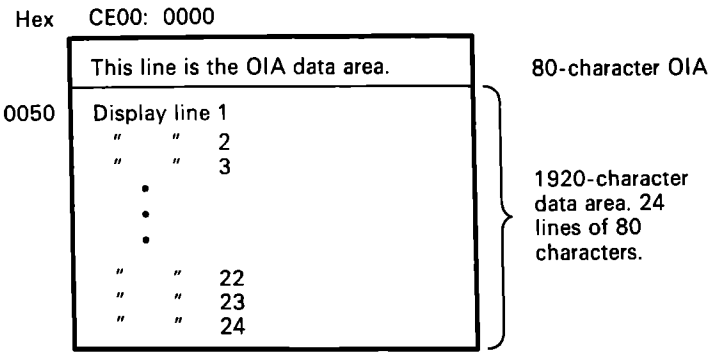


Figure 5-1. Hardware Buffer at Location Hex CE000

The first 80 characters of the hardware buffer are used by the controller to contain the operator information area (OIA) data. The hex character codes are placed in the OIA by the controller, and are used as input to a character generator that provides the video image which is customarily displayed on the last line of the screen. The controller inserts the character codes in the hardware buffer, and the adapter card then generates an interrupt to inform your program that the buffer has been modified. The controller can insert any number of characters in the buffer, up to a complete new buffer image. It is your responsibility to evaluate the contents of the buffer. Data in the

buffer will not automatically appear on the screen. It must be drawn to the display screen by your program. You may thus control the display image on the screen at all times, independently of the hex CE000 buffer.

Hardware Configurations

The following diagrams show possible configurations containing the IBM 3270 Connection adapter card:

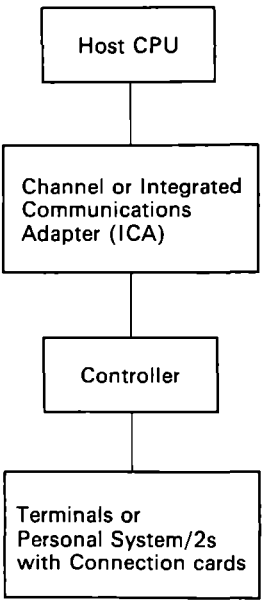


Figure 5-2. Locally-Attached Terminals

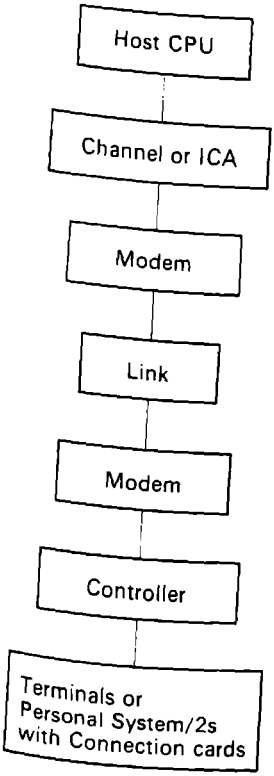


Figure 5-3. Remotely-Attached Terminals

3274 Overview

The 3274 is a polling device. In order to communicate with the adapter card, the controller must be configured to handle terminals in CUT mode. The controller communicates with terminals by sending out a 12-bit unit of data that contains space for a character code and some control bits or flags. The poll configuration causes the terminal to respond with a status word describing the state of the terminal. All communication and data transfer is performed serially and in 12-bit units.

The controller continually sends poll control words to each terminal in sequence and waits for a response. If the response contains any error information or if a terminal does not respond within a predetermined time, the controller polls the next address. The controller attempts to recover from errors. A

nonresponding terminal will still be polled, but all responses are ignored until a connect sequence (restart) is executed.

Coding Requirements

The section describes in detail the steps needed to support the IBM 3270 Connection adapter card. The coding examples are merely outlines: they should not be used literally.

The adapter card can generate an interrupt each time it receives data or control information from the controller. You must evaluate the 3270 Connection card interrupt status register (ISR) to determine the nature of the interrupt.

The following is a list of the functions (each function may be thought of as a section of code) necessary in order to use the IBM 3270 Connection adapter card in CUT mode:

1. An *initialization* module to set up the Personal System/2, initialize the adapter card, and establish communication with the control unit.

2. An *interrupt handler* to support the following interrupts generated by the adapter card:

   - Keystroke accepted
   - Sound Alarm
   - Buffer Modified
   - Reset command decoded.

3. A *keystroking and inbound data transmission* module, to handle the transmission of keystrokes to the controller. (Data going toward the host is referred to as inbound data or the inbound data stream.)

4. An *outbound data transmission* module, to handle the information coming from the host to the Personal System/2. (Data transmitted from the host/controller is referred to as outbound data or the outbound data stream.) This data will be placed in the hex CE000 hardware buffer of the adapter card. You must now process the data in the buffer to be displayed on the screen, unless you have a program to evaluate the contents of the buffer.

Figure 5-4 illustrates the flow of information among the functions listed above.

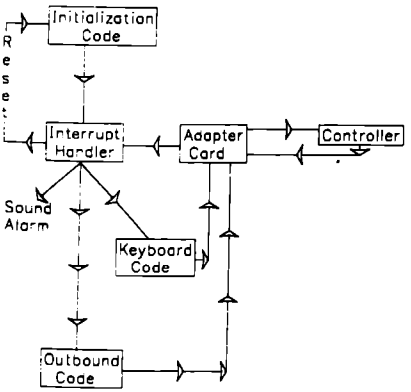


Figure 5-4. Information Flow for Modules Supporting 3270 Connection

Initialization

The initialization code must be designed to run once at IPL/startup of the controller connection, and should not be entered again for the duration of the session. The initialization process consists of several tasks to be performed in the following order.

1. Write interrupt handlers for level 2 and level 7.
2. Install the interrupt handlers.
3. Initialize and enable the IBM 3270 Connection adapter card.
4. Enable the system unit interrupt controller to allow level 2 interrupts.

Writing the Interrupt Handlers

Interrupt handlers are needed on both level 2 and level 7.

Interrupt Handler for Level 2

The first thing that your interrupt handler module must do is allow other level 2 interrupts. It must:

Clear Register AH.

Load Register AL with the value hex 62.

Write register AL to the 8259 control port address hex 20.

*Note: An I/O delay must be inserted in the code to allow the operation to complete. Otherwise, the next instruction could receive incorrect data. This is easily done with two jump instructions (J * + 2) immediately after the I/O instructions. Many programmers routinely do this to ensure compatibility among the devices containing the adapter card.*

At this point the interrupt handler must interact with the registers of the adapter card itself, beginning with address hex 2D0, the interrupt status register.

Read register hex 2D0.

Delay for I/O to complete.

Write the hex 2D0 register to reset its contents (use exact data from the previous read).

Delay for I/O to complete.

Logical OR the ISR register into the ISR save area.

The interrupt handler must now test the interrupt generated and repeat the previous steps if the hardware is still interrupting. When the interrupts have ceased, it must copy the ISR save area to a work area.

The following diagram illustrates the CUT mode interrupts used with the Connection adapter card.

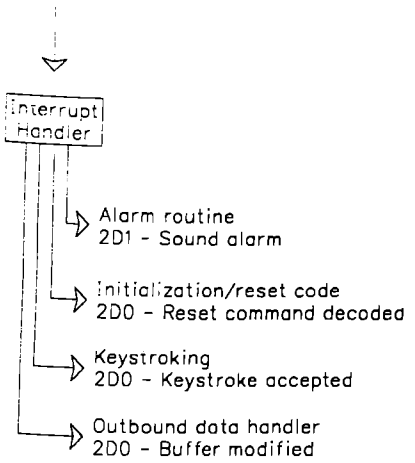


Figure 5-5. Adapter Card Interrupts in CUT Mode

Interrupt Handler for Level 7

Occasionally the Personal System/2 interrupt controller will produce a level 7 interrupt with the ISR bit for level 7 cleared. This happens when the controller is unable to determine the source of the interrupt because of the necessarily short duration of the interrupt pulse generated by the 3270 Connection. Your level 7 interrupt handler should transfer control to the level 2 interrupt handler to see if there are any interrupts pending from the adapter.

Keystroke Handling

You should now consider what you are trying to accomplish. In this example, the control unit has been customized for a typewriter keyboard. It has no support for the Personal System/2 keyboard. Therefore, you must simulate exactly the functions and scan codes of the terminal and keyboard that was described with the bit configuration in the terminal ID register. You

must also have a compatible controller with your port configured to handle your terminal type and keyboard type.

When you press a key, an interrupt will be generated in the Personal System/2. Your interrupt-handler must then receive control, recognize that a keystroke has occurred, and pass control to your keystroke handler code. The degree of sophistication built into the keystroke handler depends entirely on your needs. You must be very careful to ensure the controller remains synchronized with the Personal System/2 shift state. The scan code of a key may have totally different meaning depending on the shift state that the controller is set to. It is your responsibility to modify the shift state when necessary and inform the controller.

Four shift states exist on the Personal System/2 keyboard:

- Lowercase
- Uppercase
- Control shift
- Alternate shift

A practical method of handling this is to create a translate table with four sections, one for each shift state, and use this to translate the Personal System/2 keyboard scan code to the scan code expected at the controller for the same key. An additional level of complexity is introduced in cases where function keys and special characters are mapped to different shift states on the two keyboards in question. These conditions require special processing routines to modify the controller shift state, send the translated scan code, and synchronize the controller shift state. It is possible, therefore, to transmit up to three scan codes to the controller for these keys.

The sequence of events shown below is repeated each time a key is pressed:

1. Generate an interrupt.
2. Read the keystroke.
3. Evaluate the scan code.
4. Translate the scan code.
5. Enqueue one to three scan codes for transmission to the controller.
6. Sleep.

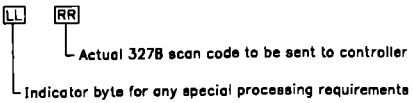
Intercepting Keystrokes

Keystrokes may be intercepted in several ways. The recommendation is that you utilize DOS Interrupt 21, which will provide the individual keystrokes in both ASCII and the true hex Personal System/2 scan code value. Translation examples in this document utilize a direct scan-code-to-scan-code translation. Refer to the *DOS Technical Reference* for information on how to code this interrupt.

Scan Code Translation

Because the keyboard scan codes generated by the Personal System/2 are not the same as those generated by the 3278 Model 2 typewriter keyboard, your program must imitate a 3278. The Personal System/2 keyboard scan code translation can be done with a table made up of 2- byte elements as shown in the example below. The right byte is the actual 3278 scan code, and the left byte is available to indicate that special processing is required and the type. The Personal System/2 scan code value multiplied by 2 becomes the index into the translate table where the

By examining the flags of the indicator byte, your code can determine if any additional scan codes or special processing is required. An example of a possible table structure follows:



In the following example several arbitrary flags are defined for the leftmost byte of each table element as follows:

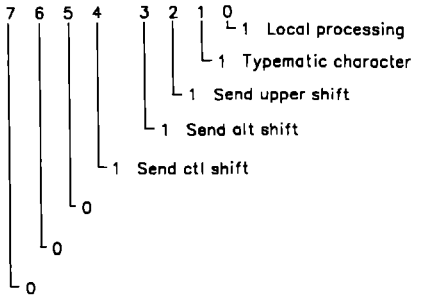


Figure 5-6. Flag Bytes

Shift State		3278 Key Function	Personal System/2 Scan Code Value
Lowercase	DW 0151H	CLEAR	01
	DW 0221H	1	02
	DW 0222H	2	03
	DW 0223H	3	04
	DW 0224H	4	05
	DW 0225H	5	06
	DW 0226H	6	07
	DW 0227H	7	08
	DW 0228H	8	09
	DW 0229H	9	0A
	DW 0220H	0	0B
	DW 0230H	-	0C
	DW 0211H	=	0D
			..
			..

Note: Reproduce the above table for each shift state of the keyboard and include appropriate scan codes and flags. You should use a unique code to indicate when a table position is not valid.

Shift State		3278 Key Function	Personal System/2 Scan Code Value
Uppercase	DW XX01H	ESC	01
	DW XX1BH	!	02
	DW XX22H	@	03
	DW XX23H	#	04
			..
			..
Alternate Shift	DW XX01H	NOP	01
	DW XX01H	NOP	02
	DW XX01H	NOP	03
	DW XX01H	NOP	04
	.. ..		..
Control Shift	DW XX01H	NOP	01
	DW XX01H	NOP	02
	DW XX01H	NOP	03
	DW XX01H	NOP	04
	.. ....	.	..
	.. ....	.	..

At this point the scan code has been translated into from one to three scan codes, and is ready to be transmitted to the controller. One method is to insert the scan codes into a small first in, first out (FIFO) queue that will handle about 20 scan codes at a time. In order to obtain maximum transmission efficiency, the scan code register on the adapter card should be loaded as soon as the previous keystroke is accepted. (Bit 0 of register hex 2D0 is set to 1.)

The following list shows the steps needed:

1. Pick up the keyboard scan code.
2. Translate by table look-up.
3. Evaluate the flags byte and call any necessary special function processing.
4. Enqueue to inbound code transmission.

Inbound Code Transmission

The following is a sample of the steps necessary to transmit the scan code to the controller.

1. Dequeue a scan code.
2. Load the scan code in register AL.
3. Load address hex 2D5 in register DX (address of scan code port).
4. Complement AL.
5. Output the scan code to the hardware.
6. Load address hex 2D4 in register DX (address of control status register).
7. Input the current CSR. Contents must be restored.
8. OR in a hex 08. Turn on the "keystroke available" bit.
9. Load the CSR back to the hardware.
10. End.

This procedure cannot be re-entered until a keystroke accepted interrupt has occurred, indicating that the keystroke was sent to the controller.

Outbound Data Handling

You may display the outbound data on the screen in several different ways. DOS interrupt 21, functions 2, 6, and 9, provide the capability of writing data to the display screen. (See the *DOS Technical Reference* for more information on this subject.) You may choose to write directly to the hex B000 or hex B8000 display buffers. In any case, this code should be initiated by your interrupt handler when a buffer modified signal is detected in port hex 2D0.

When designing this particular block of code, you must understand how the controller updates the hex CE000 buffer. Since the data is inserted into the buffer by the controller, you should keep track of the cursor location in order to calculate any changes to the screen. Since the controller utilizes the cursor as a type of addressing mark during buffer modification, the cursor location is not always a true indication of any changes until the buffer modified complete bit is set. In addition, changes in the OIA field of the hex CE000 buffer will not be detectable by the current cursor location.

Installing the Interrupt Handlers

Before installing a new handler for level 2, the hardware interrupts for level 2 must be disabled. You can accomplish this by using the following code that sets the interrupt mask in the Personal System/2 interrupt controller.

```
IN      AL,021H          ;Obtain current mask
OR      AL,4             ;Set mask for level 2
OUT     021H,AL          ;Disable level 2
```

Use the Personal System-DOS Interrupt hex 21 function calls hex 35 and hex 25 to install your handlers for levels 2 and 7. Function hex 35 provides a pointer to the current interrupt handler for the interrupt number contained in the AL register. Your handler should save the pointer so that other interrupt handlers may operate in sequence on that level. Install your interrupt handler by using function hex 25. See the *IBM Disk*

Operating System Technical Reference manual for more information on the use of Personal System-DOS interrupt hex 21.

Initializing and Enabling the 3270 Connection Adapter Card

The following procedure can be contained in one module or distributed in several sections of your code, depending on the design you select to reset or initialize the adapter card.

On entry to the code, it is a good idea to ensure that any queues that were set up for scan codes or data are reset, particularly if entry was caused by the reset command decoded bit of the (ISR) being decoded.

1. Read the contents of the ISR hex 2D0.

2. Test the "buffer being modified" bit. If it is set, loop for approximately 50 milliseconds and test it again. The buffer should not be busy the second time. If it is, an error condition must be indicated.

3. Reset all the bits of the ISR and the ISR save area.

4. Set up the terminal ID register hex 2D6 (hex E4 for a 3278 Model 2 with a typewriter keyboard). It will be interrogated by the controller immediately after the coaxial cable communication line is enabled.

   Note: This value must be complemented before the output instruction is executed.

5. Enable the adapter card and interrupts by setting the enable bit of port hex 2D4. This will cause the adapter card to perform the hardware function necessary to signal the controller that the coaxial cable has been enabled.

6. You should now ensure synchronization of the shift state between the Personal System/2 keyboard and the controller. This can be done by creating a save area to maintain the current shift state. You should begin by setting the shift state to lowercase immediately after the enable, and maintain a record of each current change. This can be done with flags, or with the most recent shift scan code sent to the controller.

The following diagrams show the meanings of the bit flags in registers hex 2D0, 2D1, and hex 2D4 for CUT mode operation.

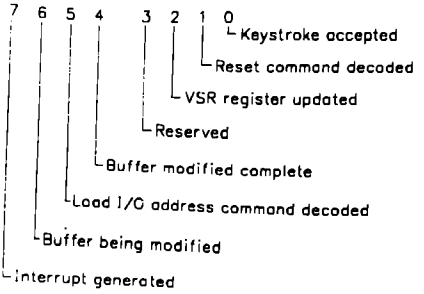


Figure 5-7. Flag Bits in ISR Hex 2D0 Register

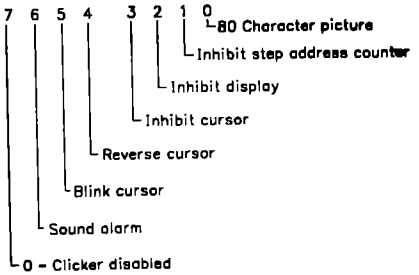


Figure 5-8. Flag Bits in VSR Hex 2D1 Register

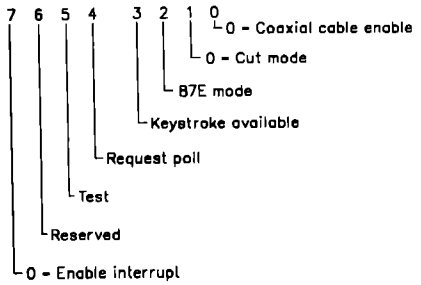


Figure 5-9. Flag Bits in CSR Hex 2D4 Register

Enabling the Interrupt Controller to Allow Level 2 Interrupts

After you have installed the interrupt handlers and initialized the adapter card, you must enable the Personal System/2 interrupt controller to allow interrupts on level 2. You can accomplish this by using the following code:

```
IN      AL,021H             ;Obtain current mask
AND     AL,0FBH             ;Clear mask for level 2
OUT     021H,AL             ;Enable hardware
```

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Numerics

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