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Volume II

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Volume II

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About This Book

Purpose

The options and adapters manual is the second part of the IBM RT PC Hardware Technical Reference manual. It is to be used in conjunction with the IBM RT PC Hardware Technical Reference, Volume 1.

Audience

The information in this manual is for reference. It is intended for hardware and program designers, programmers, engineers, and anyone else who needs to understand the design and operation of the options and adapters in the IBM RT PC Product Family.

How to Use This Book

This manual is modular in format, with each module providing information about a specific option or adapter available for the IBM RT PC family of products. Modules having a large amount of text contain indexes.

The modules are grouped by type of device. To find a specific module:

1. Locate the full length hard tab with the type of device (Displays, Printers, Storage Devices, etc.) printed on it that decribes the option or adapter you need information about.
2. Open the manual to that section.
3. Leaf through that section to find the proper module.

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4-Port Asynchronous Adapter RS232C

Contents

Description

The 4 Port Asynchronous RS232C Adapter provides four serial output ports on a 4.25- by 13.12-inch board that plugs into one I/O position. The adapter system control signals and voltage requirements are provided through a 2- by 31-position and a 2- by 18-position tab on the bottom of the adapter.

Up to four adapters may be used in one RT PC system. A DIP switch on the adapter is used to assign the adapter's I/O address range. The port I/O address assignments are contained in the adapter's I/O address range.

The adapter is fully programmable and supports asynchronous communications only. It will add and remove start bits, stop bits, and parity bits. A programmable baud-rate generator allows operation from 50 bps to 19200 bps. Five-, 6-, 7- or 8-bit characters with 1, 1-1/2, or 2 stop bits are supported. A priority interrupt system controls transmit, receive, error, line status, and data set interrupts.

Four 10-pin male connectors on the adapter provide external access to the four ports.

The heart of the adapter is an NS16450 LSI chip or a functional equivalent. Features in addition to those listed above include:

Note: The NS16450 is functionally equivalent to all INS8250.

- Full double buffering that eliminates the need for precise synchronization
- Independent receiver clock input
- Modem control functions: clear to send (CTS), request to send (RTS), data set ready (DSR), data terminal ready (DTR), ring indicator (RI), and received line signal detect (RLSD), which is also known as data carrier detect (DCD) or carrier detect (CD)
- False start bit detection
- Line-break generation and detection.

All communications protocol is a function of the system microcode that must be loaded before the adapter is operational. All pacing of the interface and control signal status must be handled by the system software. Figure 1 on page 2 is a block diagram of the 4 Port Asynchronous RS232C Adapter.

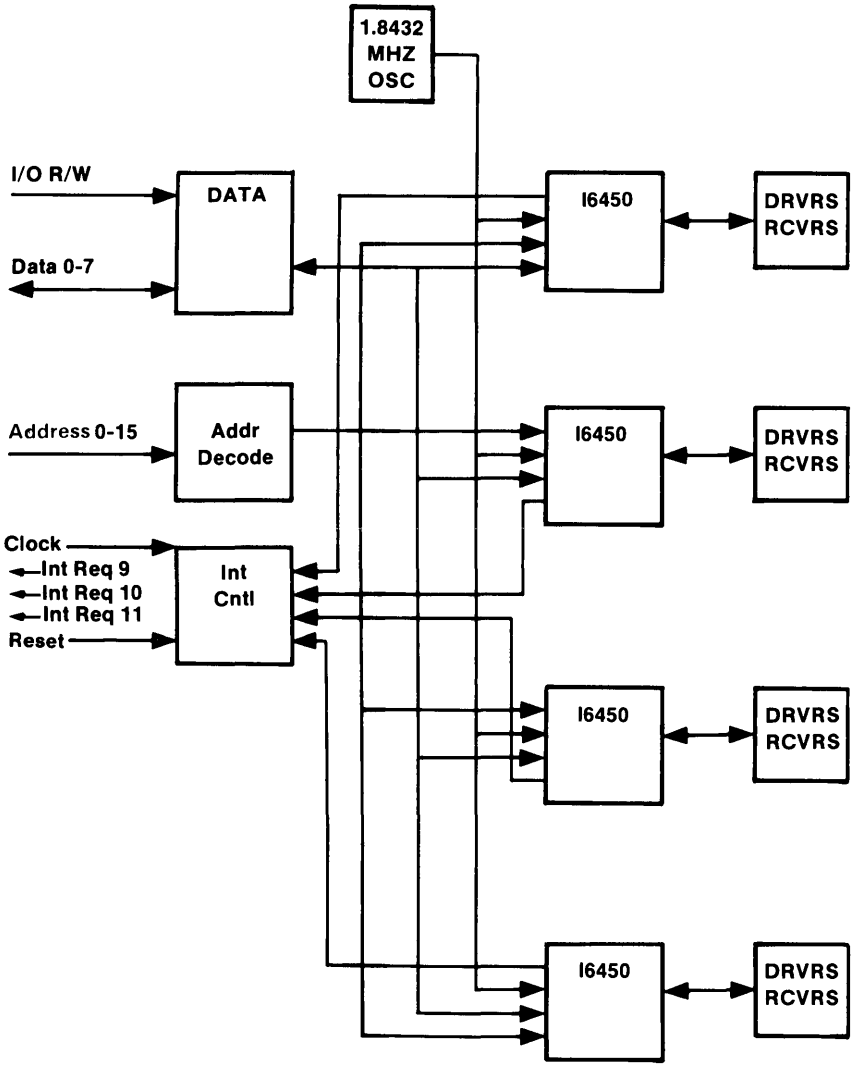


Figure 1. 4 Port Asynchronous RS232C Adapter Block Diagram

4 Port Asynchronous RS232C Adapter Switch Settings

The 4 Port Asynchronous RS232C Adapter switch settings select the interrupt level and the address range of adapters installed.

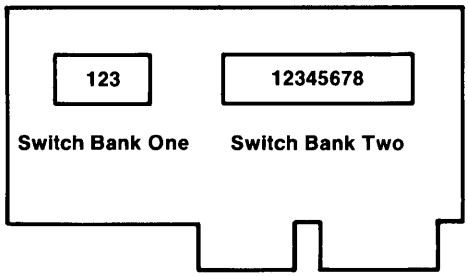


Figure 2. 4 Port Asynchronous RS232C Adapter Switches

Interrupt Level Selected	Switch Bank One Setting		
	Switch 1	**Switch 2**	**Switch 3**
Level 9	On	Off	Off
Level 10	Off	On	Off
Level 11	Off	Off	On

Figure 3. Switch Bank One Settings

Address Range of Adapters	Switch Bank Two Setting			
	Switch 1	**Switch 2**	**Switch 3**	**Switch 4**
1230-124F	On	Off	Off	Off
2230-224F	Off	On	Off	Off
3230-324F	Off	Off	On	Off
4230-424F	Off	Off	Off	On

Figure 4. Switch Bank Two Settings

Note: Switches 5 through 8 are not used.

Modes of Operation

The different modes of operation are selected by programming the NS16450 asynchronous communications element. This is done by selecting the I/O address and writing data out to the I/O address. Address bits A0, A1, and A2 select the different registers that define the modes of operation. Also, the divisor latch access bit (bit 7) of the line control register is used to select certain registers.

The address range for this adapter is Hex 1230 through Hex 424F. Figure 5 and Figure 6 on page 5 depict a value of n which represents a variable determined by the setting of switch bank two. Switches 1, 2, 3, and 4 of switch bank two allow the card to operate and select the appropriate address range.

I/O Decode (In Hex) Port B	Port A	Register Selected	DLAB State
n238	n230	TX Buffer	DLAB=0 (Write)
n238	n230	RX Buffer	DLAB=0 (Read)
n238	n230	Divisor Latch LSB	DLAB=1
n239	n231	Divisor Latch MSB	DLAB=1
n239	n231	Interrupt Enable Register	DLAB=0
n23A	n232	Interrupt Identification Register	
n23B	n233	Line Control Register	
n23C	n234	Modem Control Register	
n23D	n235	Line Status Register	
n23E	n236	Modem Status Register	

Figure 5. I/O Decodes, Port A and Port B

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

I/O Decode (In Hex) Port D	Port C	Register Selected	DLAB State
n248	n240	TX Buffer	DLAB=0 (Write)
n248	n240	RX Buffer	DLAB=0 (Read)
n248	n240	Divisor Latch LSB	DLAB=1
n249	n241	Divisor Latch MSB	DLAB=1
n249	n241	Interrupt Enable Register	DLAB=0
n24A	n242	Interrupt Identification Register	
n24B	n243	Line Control Register	
n24C	n244	Modem Control Register	
n24D	n245	Line Status Register	
n24E	n246	Modem Status Register	

Figure 6. I/O Decodes, Port C and Port D

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

A9—>A3 Decode	A2	A1	A0	DLAB	Register
See	x	x	x		
Note 1	0	0	0	0	Receive Buffer Reg. (read) Transmit Holding Reg. (write)
	0	0	1	0	Interrupt Enable
	0	1	0	x	Interrupt Identification
	0	1	1	x	Line Control
	1	0	0	x	Modem Control
	1	0	1	x	Line Status
	1	1	0	x	Modem Status
	1	1	1	x	Scratch (See note 3)
	0	0	0	1	Divisor Latch (LSB)
	0	0	1	1	Divisor Latch (MSB)

Figure 7. Address Bits

Notes:

1. Bits A9 through A3 are used to select specific adapter and serial port.
2. A2, A1, and A0 bits are "don't cares" and are used to select the different registers of the NS16450 chip.
3. The Scratch Register of the NS16450 module should be initialized to all zeros and never be written to with any data afterwards. This would cause indeterminate data when Read address X237 (see "Interrupts") is executed.

Interrupts

Three interrupts lines are provided to the system. The interrupt level (9, 10, or 11) is selected by placing the appropriate switch on switch bank one to the on position. An interrupt register (read adr n237, where n is the first digit of address range) is provided to store pending port interrupts. Interrupt register bit assignment as shown in Figure 8.

Hex Address n237							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	Port 4	Port 3	Port 2	Port 1

Figure 8. Interrupt Register Read Format

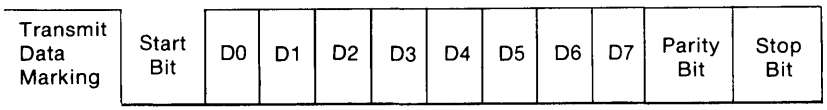
The reset or enable for interrupt level 9 is hex address 02F2.

The reset or enable for interrupt level 10 is hex address 06F2.

The reset or enable for interrupt level 11 is hex address 06F3.

Serial Data Format

The data format is as follows:



Data bit 0 is the first bit to be transmitted or received. The adapter automatically inserts the start bit, the correct parity bit (if programmed to do so), and the stop bit (1, 1-1/2, or 2 depending on the command in the line control register).

External Interface Description

The adapter provides an EIA 4 Port Asynchronous RS232C Adapter-like interface.

The pin functions for the 10-pin connector are shown in Figure 9 on page 8.

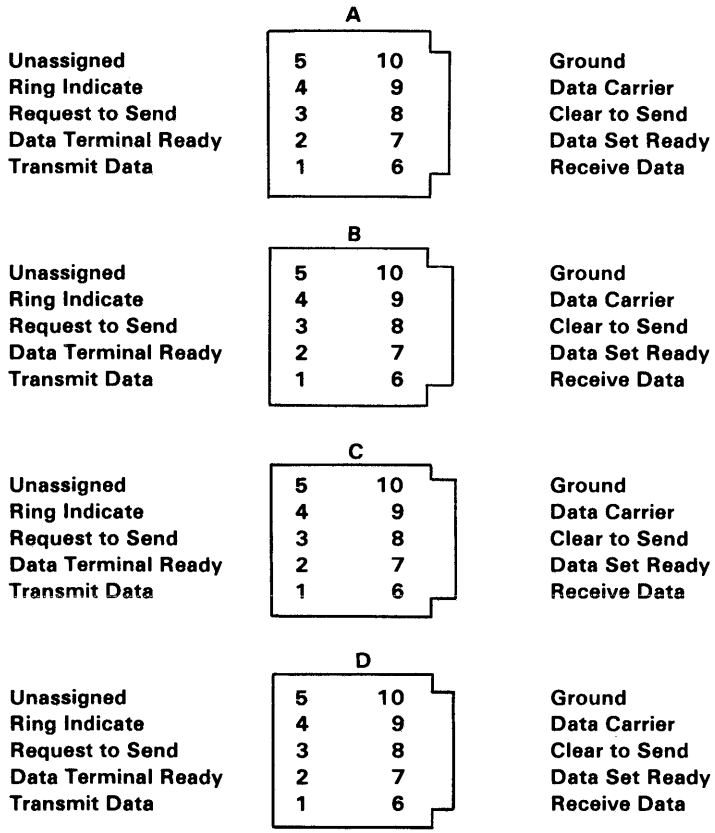


Figure 9. 10 Pin Interface Signals Connector (viewed from rear of adapter)

The adapter converts the interface signals from TTL levels to EIA 4 Port Asynchronous RS232C Adapter voltage levels, and vice versa. These signals are sampled or generated by the communications control chip. These signals can then be sensed by the system software to determine the state of the interface or peripheral device. The drivers and receivers used on the adapter are the inverting type; therefore, a 0 EIA level on the line is received or transmitted as a 0 TTL level, and a 1 EIA level is received or transmitted as a 1 TTL level.

Voltage Interchange Information

The signal will be considered in the marking condition when the voltage on the interchange circuit, measured at the interface point, is more negative than -3 Vdc with respect to signal ground. The signal will be considered in the spacing condition when the voltage is more positive than +3 Vdc with respect to signal ground. The region between +3 Vdc and -3 Vdc is defined as the transition region and is considered an invalid level. The voltage that is more negative than -15 Vdc or more positive than +15 Vdc is also considered an invalid level.

During the transmission of data, the marking condition denotes the binary state 1 and the spacing condition denotes the binary state 0.

For interface control circuits, the function is on when the voltage is more positive than +3 Vdc with respect to signal ground and is off when the voltage is more negative than -3 Vdc with respect to signal ground.

Interchange Voltage	Binary State	Signal Condition	Interface Control Function
Positive Voltage	Binary 0	Spacing	= On
Negative Voltage	Binary 1	Marking	= Off

Figure 10. 4 Port Asynchronous RS232C Adapter. Signal Levels

Asynchronous Communications Element Pin Description

The following describes the function of all NS16450 input/output pins. Some of these descriptions reference internal circuits. The use of each signal as implemented on the multiport adapter is described.

Note: In the following descriptions, a low represents a logic 0 (0 Vdc nominal) and a high represents a logic 1 (+2.4 Vdc nominal).

Input Signals

Chip Select (CS0, CS1, -CS2), Pins 12-14: When CS0 and CS1 are high and -CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) address strobe (-ADS) input. This enables communications between the NS16450 and the processor.

Data Input Strobe (DISTR, -DISTR), Pins 22 and 21: When DISTR is high or -DISTR is low while the chip is selected, the processor can read status information or data from a selected register of the NS16450.

Note: Only an active DISTR or -DISTR input is required to transfer data from the NS16450 during a read operation. Therefore, tie either the DISTR input permanently low or the -DISTR line permanently high, if not used.

Data Output Strobe (DOSTR, -DOSTR), Pins 19 and 18: When DOSTR is high or -DOSTR is low while the chip is selected, the processor can write data or control words into a selected register of the NS16450.

Note: Only an active DOSTR or -DOSTR input is required to transfer data to the NS16450 during a write operation. Therefore, tie either the DOSTR input permanently low or the -DOSTR input permanently high, if not used.

-Address Strobe (-ADS), Pin 25: When low, this signal provides latching for the register select (A0, A1, A2) and chip select (CS0, CS1, -CS2) signals.

Note: An active -ADS input is required when the register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the -ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an NS16450 register to read from or write into as indicated in Figure 11. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain NS16450 registers. The DLAB must be set high by the system software to access the baud-generator divisor latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (Read) Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable
x	0	1	0	Interrupt Identification (Read Only)
x	0	1	1	Line Control
x	1	0	0	Modem Control
x	1	0	1	Line Status
x	1	1	0	Modem Status
x	1	1	1	Scratch
1	0	0	0	Divisor Latch (Least Significant Byte)
1	0	0	1	Divisor Latch (Most Significant Byte)

Figure 11. NS16450 Register Selection

Master Reset (MR), Pin 35: When high, this signal clears all the registers (except the receive buffer, transmitter holding, and divisor latches), and the control logic of the NS16450. Also, the state of various output signals (SOUT, INTRPT, -OUT 1, -OUT 2, -RTS, -DTR) is affected by an active MR input. Refer to the table in Figure 12 on page 12 for reset functions.

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low 0-3 Forced and 4-7 Permanent
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 are Low, and Bits 3-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
Modem Status Register	Master Reset	Bits 0-3 are Low Bits 4-7 = Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errors)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRP (THRE)	Read IIR/ Write THR/MR	Low
INTRPT (Modem Status Changes) • OUT 2 • RTS • DTR • OUT 1	Read MSR/MR Master Reset Master Reset Master Reset Master Reset	Low High High High High

Figure 12. NS16450 Reset Functions

Receiver Clock (RCLK), Pin 9: This input is the 16x baud-rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, modem, or data set).

-Clear to Send (-CTS), Pin 36: The -CTS signal is a modem control function input whose condition can be tested by the processor by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates whether the -CTS input has changed state since the previous reading of the modem status register.

Note: Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

-Data Set Ready (-DSR), Pin 37: The -DSR signal is a modem control function input whose condition can be tested by the processor by reading bit 5 (DSR) of the modem status register. When low, this signal indicates that the modem or data set is ready to establish the communications link and transfer data with the NS16450. Bit 1 (DDSR) of the modem status register indicates whether the -DSR input has changed since the previous reading of the modem status register.

Note: Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

-Received Line Signal Detect (-RLSD), Pin 38: The -RLSD signal is a modem control function input whose condition the processor can test by reading bit 7 (RLSD) of the modem status register. When low, this signal indicates that the data carrier had been detected by the modem or data set. Bit 3 (DRLSD) of the modem status register indicates whether the -RLSD not input has changed state since the previous reading of the modem status register.

Notes:

1. Whenever the RLSD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.
2. Received Line Signal Detect is also called Data Carrier Detect (DCD), or Carrier Detect (CD).

-Ring Indicator (-RI), Pin 39: The -RI signal is a modem control function input whose condition the processor can test by reading bit 6 (RI) of the modem status register. When low, this signal indicates that a telephone ringing signal has been received by the modem or data set. Bit 2 (TERI) of the modem status register indicates whether the -RI input has changed from a low to high state since the previous reading of the modem status register.

Note: Whenever the RI bit of the modem status register changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.

VCC, Pin 40: +5 Vdc supply.

VSS, Pin 20: Ground (0 Vdc) reference.

Output Signals

-Data Terminal Ready (-DTR), Pin 33: When low, this signal informs the modem or data set that the NS16450 is ready to communicate. The -DTR output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. The -DTR signal is set high by a master reset operation. The -DTR signal is set high during loop mode operation.

-Request to Send (-RTS), Pin 32: When low, this signal informs the modem or data set that the NS16450 is ready to transmit data. The -RTS output signal can be set to an active low by programming bit 1 (RTS) of the modem control register. The -RTS signal is set high by a master reset operation. The -RTS signal is set high during loop mode operation.

-Output 1 (-OUT 1), Pin 34: With this signal, user-designated output can be set to an active low by programming bit 2 (-OUT 1) of the modem control register to a high level. The -OUT 1 signal is set high by a master reset operation. The -OUT 1 signal is set high during the loop mode operation.

-Output 2 (-OUT 2), Pin 31: With this signal, user-designated output can be set to an active low by programming bit 3 (-OUT 2) of the modem control register to a high level. The -OUT 2 signal is set high by a master reset operation. The -OUT 2 signal is set high during the loop mode operation.

Chip Select Out (CSOUT), Pin 24: When high, this signal indicates that the chip has been selected by active CS0, CS1, and -CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: This signal goes low whenever the processor is reading data from the NS16450. A high-level DDIS output can be used to disable an external transceiver (if used between the processor and NS16450 on the D7-D0 data bus) at all times, except when the processor is reading data.

-Baudout (-BAUDOUT), Pin 15: This signal is a 16x clock signal for the transmitter section of the NS16450. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud-generator division latches. The -Baudout may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: This signal goes high whenever any one of the following interrupt types has an active high condition and is enabled through the IER: receiver error flag, received data available, transmitter holding register empty, or modem status. The Intrpt signal is reset low upon the appropriate interrupt service or a master reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, modem or data set). The SOUT signal is set to the marking (logic 1) state upon a master reset operation.

Input/Output Signals

Data Bus (D7-D0), Pins 1-8: This bus comprises eight tri-state input/output lines. The bus provides bidirectional communications between the NS16450 and the processor. Data, control words, and status information are transferred through the D7-D0 data bus.

External Clock Input/Output (XTAL1, XTAL2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the NS16450.

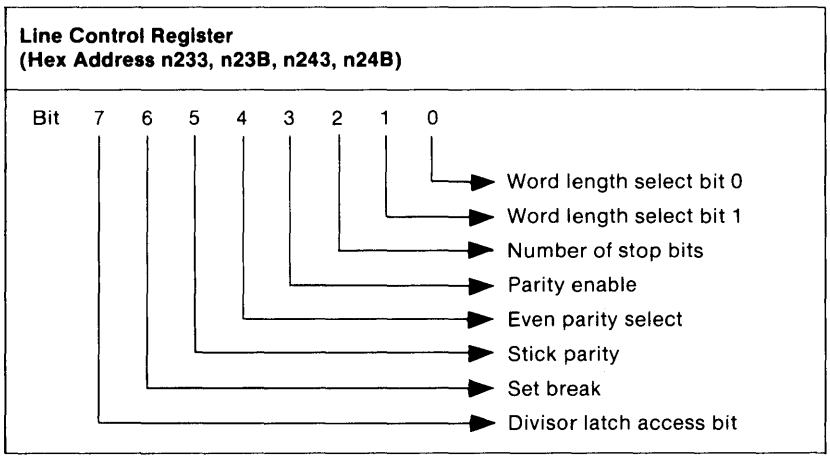
Programming Considerations

The NS16450 has a number of accessible registers. The system programmer may access or control any of the NS16450 registers through the processor. These registers are used to control NS16450 operations and to transmit and receive data.

Note: The n in address is the card number (1-4).

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange through the line control register. In addition to controlling the format, the programmer may retrieve the contents of the line control register for inspection. This feature simplifies system programming and eliminates the need for separate storage of the line characteristics in system memory. The contents of the line control register are described below:



Bits 0, 1 These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2 This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logical 0, one stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logical 1 when a 5-bit word length is selected through bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is a logical 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated or checked.

Bit 3 This bit is the parity enable bit. When bit 3 is a logical 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed.)

Bit 4 This bit is the even parity select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's are transmitted or checked in the data word bits and parity bit. When bit 3 is a logical 1 and bit 4 is a logical 1, an even number of bits are transmitted or checked.

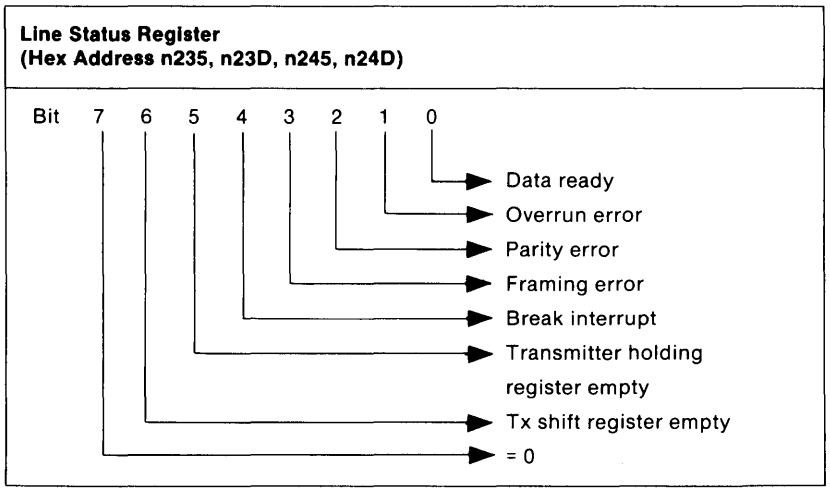
Bit 5 This bit is the stick parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is transmitted and then detected by the receiver as a logical 0 (space parity) if bit 4 is a logical 1, or as a logical 1 (mark parity) if bit 4 is a logical 0.

Bit 6 This bit is the set break control bit. When bit 6 is a logical 1, the serial output (SOUT) is forced to the spacing (logical 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logical 0. This feature enables the processor to alert a terminal in a computer communications system.

Bit 7 This bit is the divisor latch access bit (DLAB). It must be set high (logical 1) to access the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Line Status Register

This 8-bit register provides status information to the processor concerning the data transfer. The contents of the line status register are described below:



Bit 0 This bit is the receiver data ready (DR) indicator. Bit 0 is set to a logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to a logical 0 either by the processor reading the data in the receiver buffer or by writing a logical 0 into it from the processor.

Bit 1 This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the processor before the next character was transferred into the receiver buffer register, and thereby destroyed the previous character. The OE indicator is reset whenever the processor reads the contents of the line status register.

Bit 2 This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity as selected by the even parity select bit. The PE bit is set to a logical 1 whenever a parity error is detected and is reset to a logical 0 whenever the processor reads the contents of the line status register.

Bit 3 This bit is the framing error (FE) indicator. Bit 3 indicates that the received character does not have a valid stop bit. Bit 3 is set to a logical 1 whenever the stop bit following the last data bit or parity is detected as a zero bit (spacing level).

Bit 4 This bit is the break interrupt (BI) indicator. Bit 4 is set to a logical 1 whenever the received data input is held in the spacing (logical 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits).

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected.

Bit 5 This bit is the transmitter holding register empty (THRE) indicator. Bit 5 indicates that the NS16450 is ready to accept a new character for transmission. In addition, this bit causes the NS16450 to issue an interrupt to the processor when the THRE interrupt enable is set high. The THRE bit is set to a logical 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logical 0 concurrently with the loading of the transmitter holding register by the processor.

Bit 6 This bit is the transmitter empty (TEMT) indicator. Bit 6 is set to a logical 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logical 0 whenever either the THR or TSR contain a data character. Bit 6 is a read-only bit.

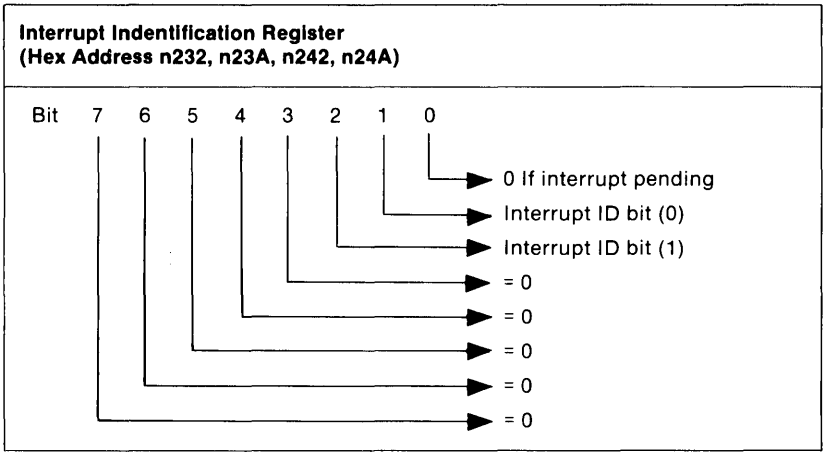
Bit 7 This bit is permanently set to logical 0.

Interrupt Identification Register

The NS16450 has an on-chip interrupt capability that allows for complete flexibility in interfacing to microprocessors. In order to provide minimum software overhead during data character transfers, the NS16450 prioritizes interrupts into four levels:

- Receiver line status (priority 1)
- Received data ready (priority 2)
- Transmitter holding register empty (priority 3)
- Modem status (priority 4).

Information indicating that a priority interrupt is pending and information on the type of interrupt is stored in the interrupt identification register. Refer to the "Interrupt Control Functions" table in Figure 13 on page 20. The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending, and no other interrupts are acknowledged until that particular interrupt is serviced by the processor. The contents of the IIR are described below.



Bit 0 This bit can be used in hardwired, priority, or polled environment to indicate whether an interrupt is pending. When bit 0 is a logical 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logical 1, no interrupt is pending and polling (if used) is continued.

Bits 1, 2 These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Figure 13 on page 20.

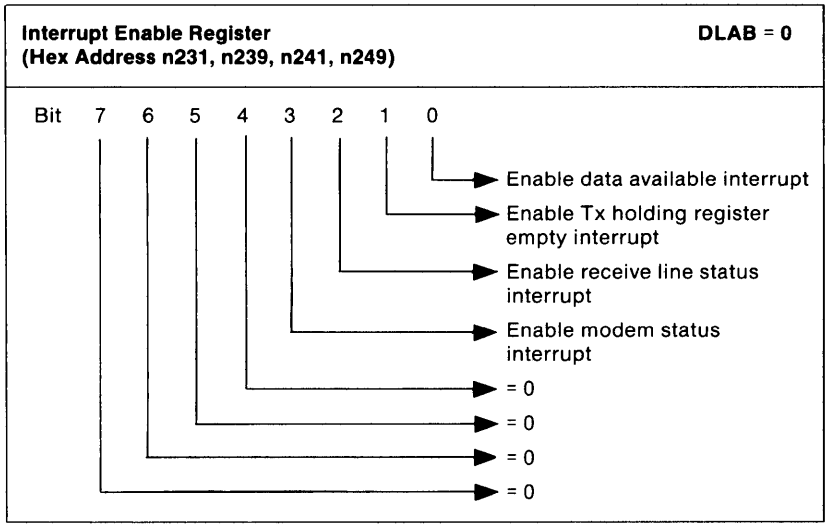
Bits 3-7 These five bits of the IIR are always logical 0.

Interrupt ID Register			Interrupt Set and Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Intrpt.	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register or Writing into the Transmitter Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Figure 13. Interrupt Control Functions

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the NS16450 to separately activate the chip interrupt (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the interrupt enable register. Similarly, by setting the appropriate bits of this register to a logical 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are described below:



Bit 0 This bit enables the received data available interrupt when set to logical 1.

Bit 1 This bit enables the transmitter holding register empty interrupt when set to logical 1.

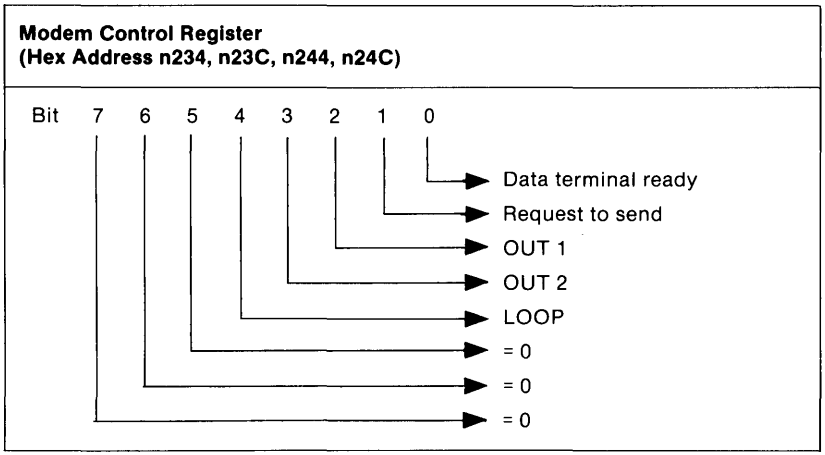
Bit 2 This bit enables the receiver line status interrupt when set to logical 1.

Bit 3 This bit enables the modem status interrupt when set to logical 1.

Bits 4-7 These four bits are always logical 0.

Modem Control Register

This 8-bit register controls the interface with the modem or data set (or other peripheral device). The contents of the modem control register are described below:



Bit 0 This bit controls the data terminal ready (-DTR) output. When bit 0 is set to a logical 1, the -DTR output is forced to a logical 0. When bit 0 is reset to a logical 0, the -DTR output is forced to a logical 1.

Note: The -DTR output of the NS16450 may be applied to an EIA inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 1 This bit controls the request to send (-RTS) output. Bit 1 affects the -RTS output in a manner identical to that described above for bit 0.

Note: The -RTS output of the NS16450 may be applied to an EIA-inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 2 This bit controls the output 1 (-OUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the -OUT 1 output in a manner identical to that described above for bit 0.

Note: The -OUT 1 output of the NS16450 may be applied to an EIA inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 3 This bit controls the output 2 (-OUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the -OUT 2 output in a manner identical to that described above for bit 0.

Note: The -OUT 2 output of the NS16450 may be applied to an EIA inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 4 This bit provides a loopback feature for diagnostic testing of the NS16450. When bit 4 is set to logical 1, the following occurs:

The transmitter serial output (SOUT) is set to the marking (logical 1) state.

The receiver serial input (SIN) is disconnected.

The output of the transmitter shift register is "looped back" into the receiver shift register input.

The four modem control inputs (-CTS, -DSR, -RLSD, and -RI) are disconnected.

The four modem control outputs (-DTR, -RTS, -OUT 1, and -OUT 2) are internally connected to the four modem control inputs, and the modem control output pins are forced high.

In the the diagnostic mode the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the sources of the interrupts are now the lower 4 bits of the modem control register instead of the 4 modem control inputs. The interrupts are still controlled by the interrupt enable register.

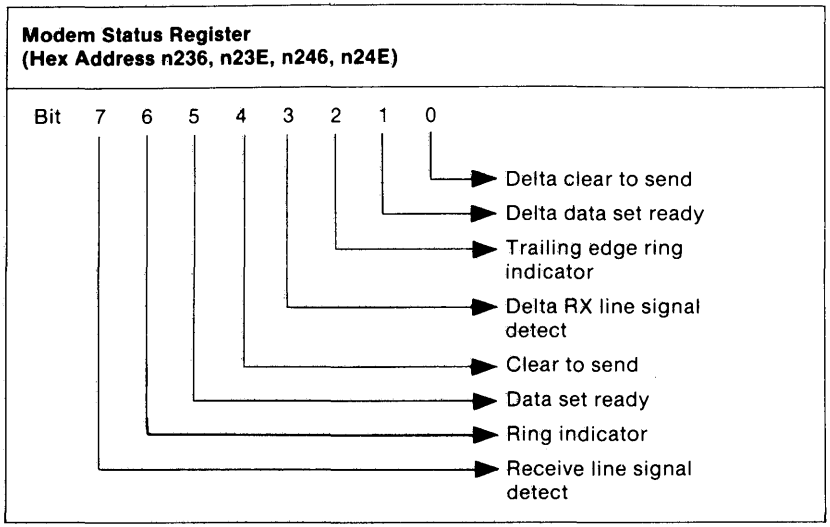
The NS16450 interrupt system can be tested by writing into the lower 6 bits of the line status register and into the lower 4 bits of the modem status register. Setting any of these bits to a logical 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal NS16450 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the modem control register must be reset to logical 0. The transmitter should be idle when this bit changes state.

Bits 5-7 These bits are permanently set to logical 0.

Modem Status Register

This 8-bit register provides the current state of the control lines from the modem (or peripheral device) to the processor. In addition to this current-state information, four bits of the modem status register provide change information. These bits are set to a logical 1 whenever a control input from the modem changes state. They are reset to logical 0 whenever the processor reads the modem status register.

The contents of the modem status register are described below:



Bit 0 This bit is the delta clear-to-send (DCTS) indicator. Bit 0 indicates that the -CTS input to the chip has changed state since the last time it was read by the processor.

Bit 1 This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the -DSR input to the chip has changed state since the last time it was read by the processor.

Bit 2 This bit is the trailing edge of the ring indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from an ON (logical 1) to an OFF (logical 0) condition.

Bit 3 This bit is the delta received line signal detector (DRLSD) indicator. Bit 3 indicates that the -RLSD input to the chip has changed state since the last time it was read by the processor.

Note: Whenever bit 0, 1, 2, or 3 is set to a logical 1, a modem status interrupt is generated, if the appropriate interrupt enable bit is set in the IER.

Bit 4 This bit is the complement of the clear to send (-CTS) input. Setting bit 4 (loop) of the MCR to a logical 1, is equivalent to RTS in the MCR.

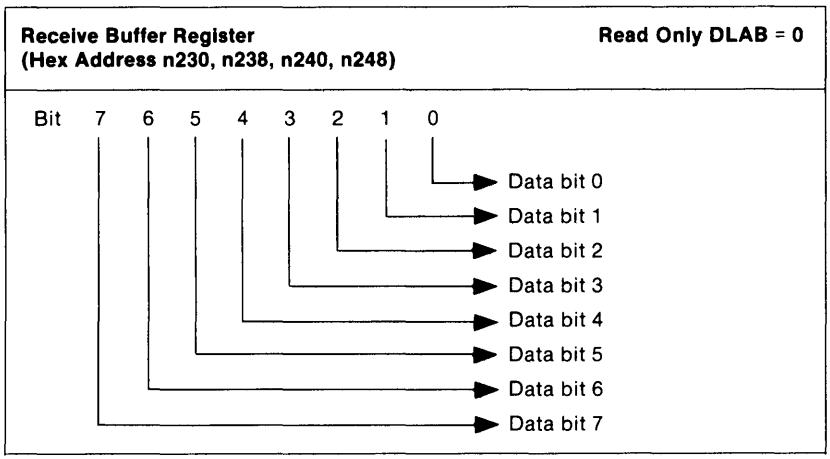
Bit 5 This bit is the complement of the data set ready (-DSR) input. If bit 4 (loop) of the MCR is set to a logical 1, this bit is equivalent to DTR in the MCR.

Bit 6 This bit is the complement of the ring indicator (-RI) input. If bit 4 (loop) of the MCR is set to a logical 1, this bit is equivalent to -OUT 1 in the MCR.

Bit 7 This bit is the complement of the received line signal detect (-RLSD) input. If bit 4 (loop) of the MCR is set to a logical 1, this bit is equivalent to -OUT 2 of the MCR.

Receiver Buffer Register

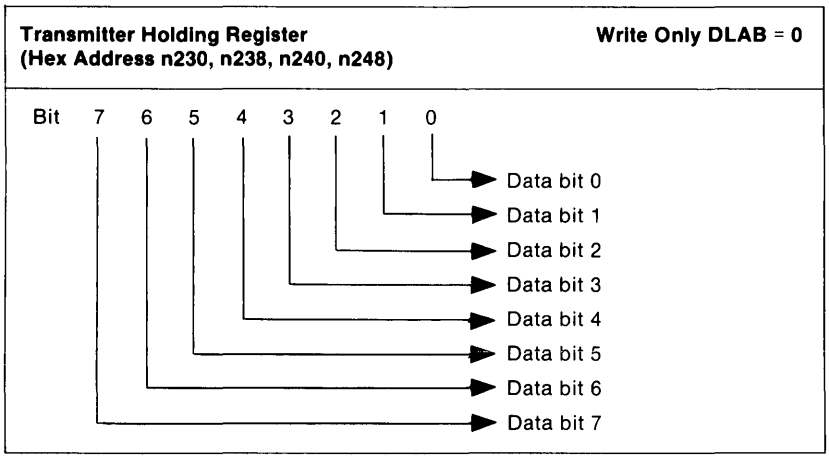
The receiver buffer register contains the received character as defined below:



Bit 0 is the least significant bit and is the first bit serially received.

Transmitter Holding Register

The transmitter holding register contains the character to be serially transmitted and is defined below:



Bit 0 is the least significant bit and is the first bit serially transmitted.

Programmable Baud-Rate Generator

The NS16450 contains a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 655,535 or 2^{16}-1. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to insure desired operation of the baud-rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The contents of the divisor latches are indicated below:

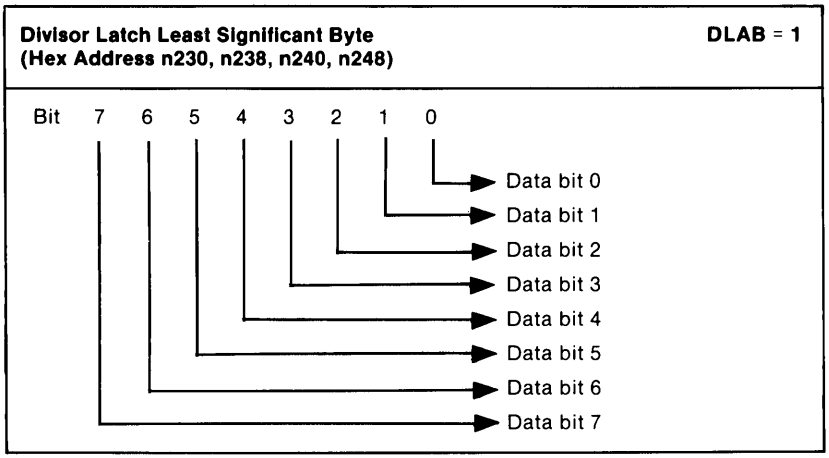


Figure 14. Divisor Latch Least Significant Byte

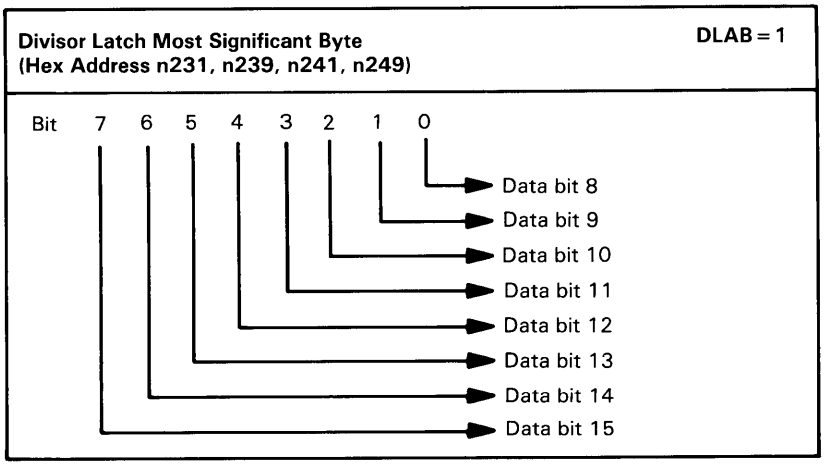


Figure 15. Divisor Latch Most Significant Byte

Figure 16 illustrates the use of the baud-rate generator with a frequency of 1.8432 MHz. For baud rates of 19,200 and below, the error obtained is minimal.

Note: The maximum operating frequency of the baud generator is 3.1 MHz. In no case should the data rate be greater than 19,200 baud.

Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent Error Difference Between Desired and Actual
50	2304	900	—
75	1536	600	—
110	1047	417	0.026
134.5	857	359	0.058
150	786	300	—
300	384	180	—
600	192	C0	—
1200	96	60	—
1800	64	40	—
2000	58	3A	0.69
2400	48	30	—
3600	32	20	—
4800	24	18	—
7200	16	10	—
9600	12	C	—
19200	6	6	—

Figure 16. Baud Rates at 1.8432 MHz

Connector Specifications

The adapter has a 10-pin connector at the rear of the adapter. The following figure shows the signals and their pin assignments.

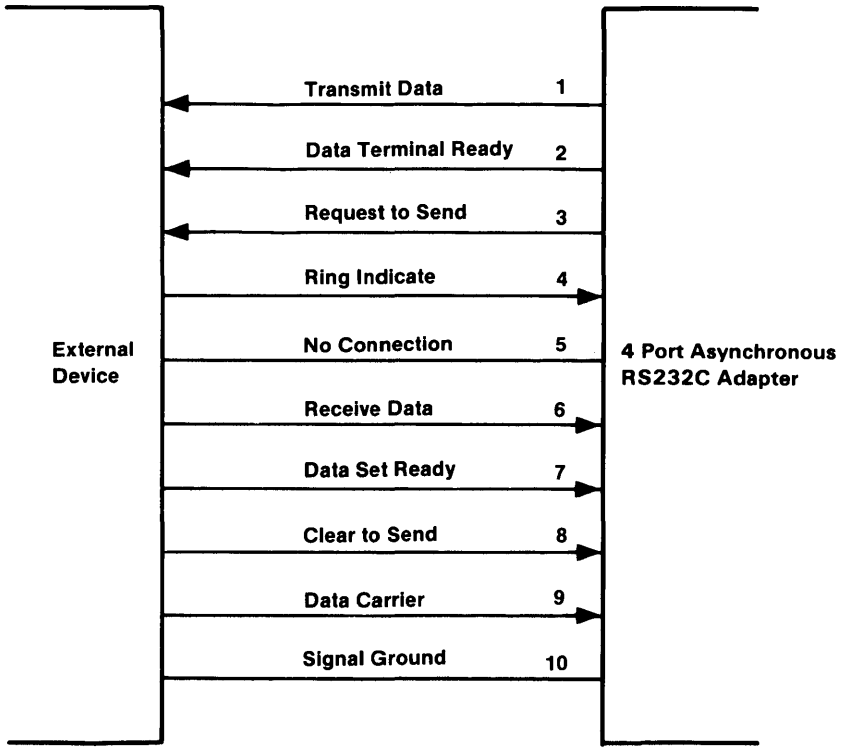
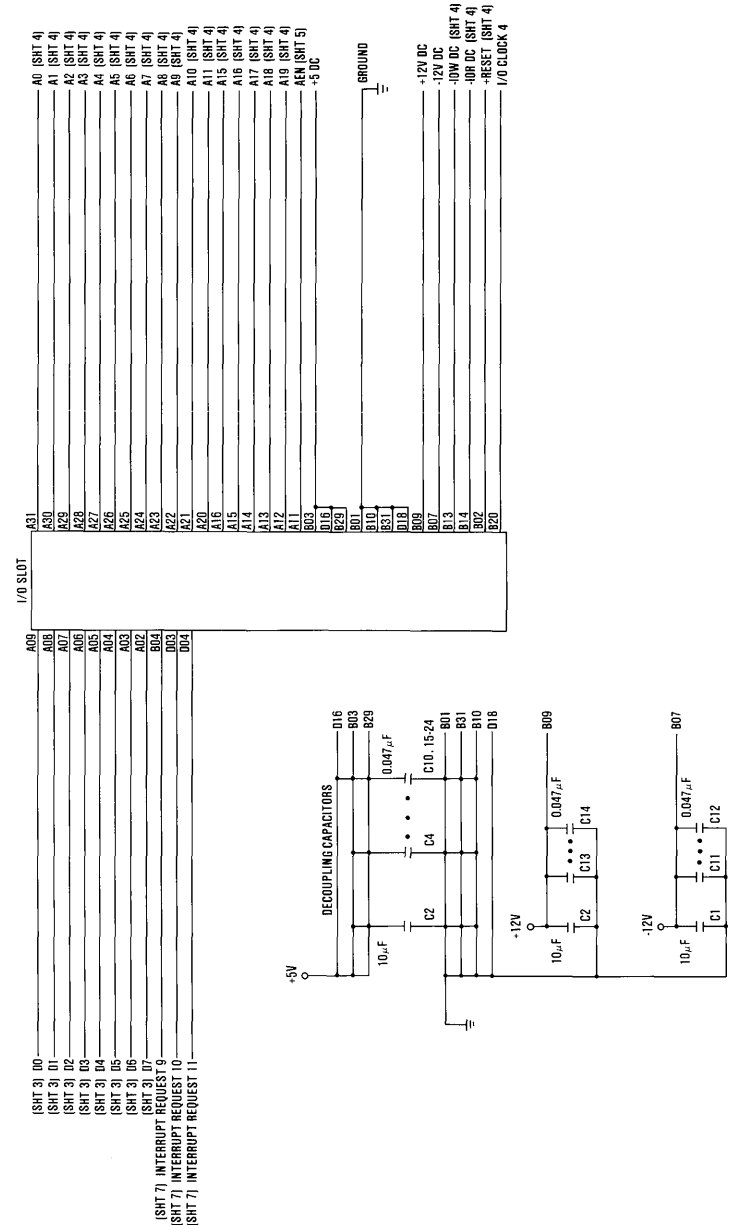


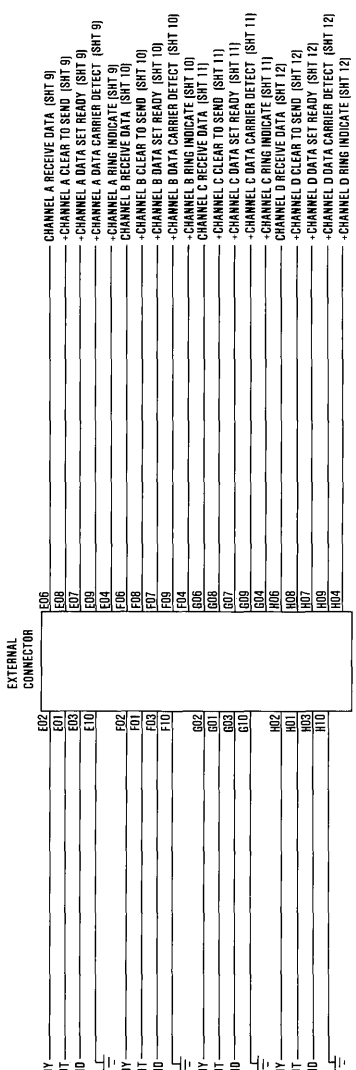
Figure 17. Connector Specifications

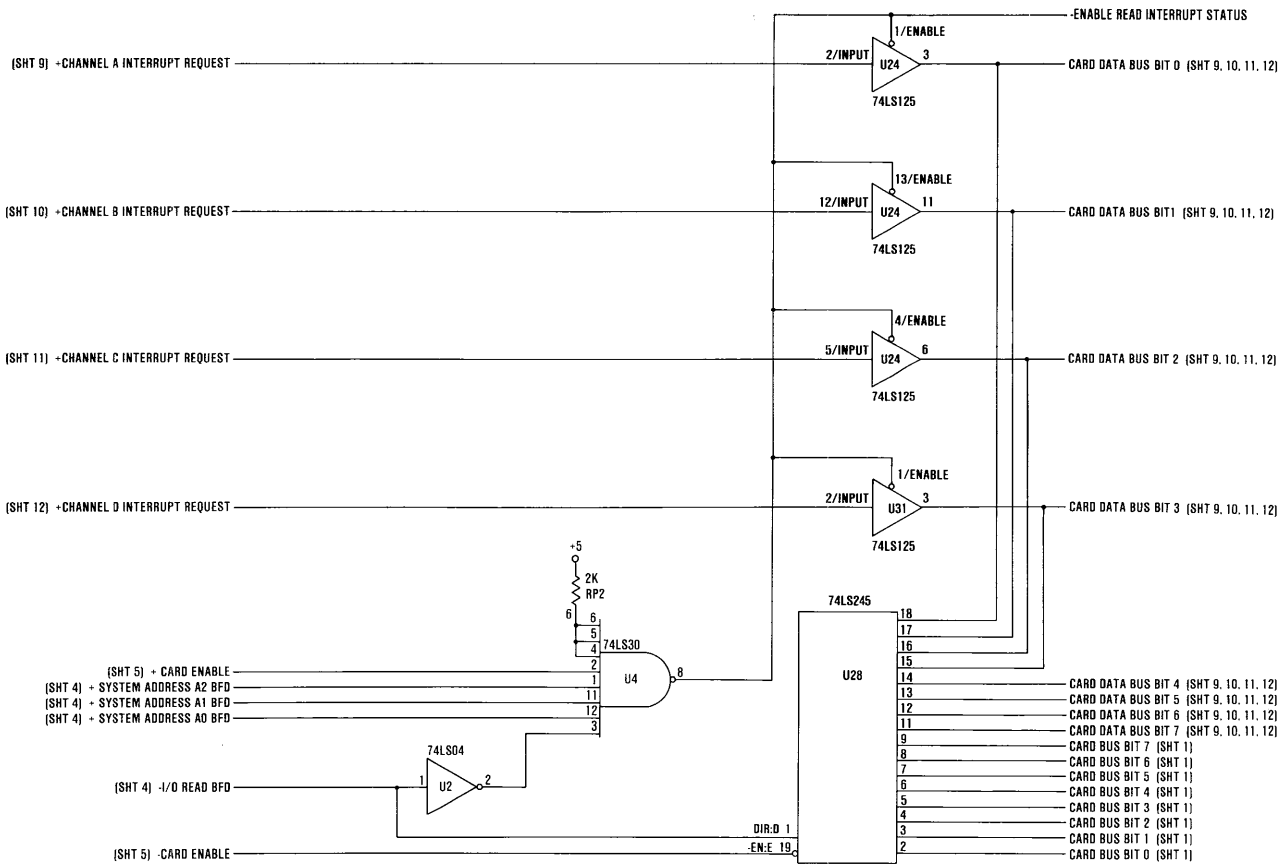
Logic Diagrams

Sheet 1 of 12

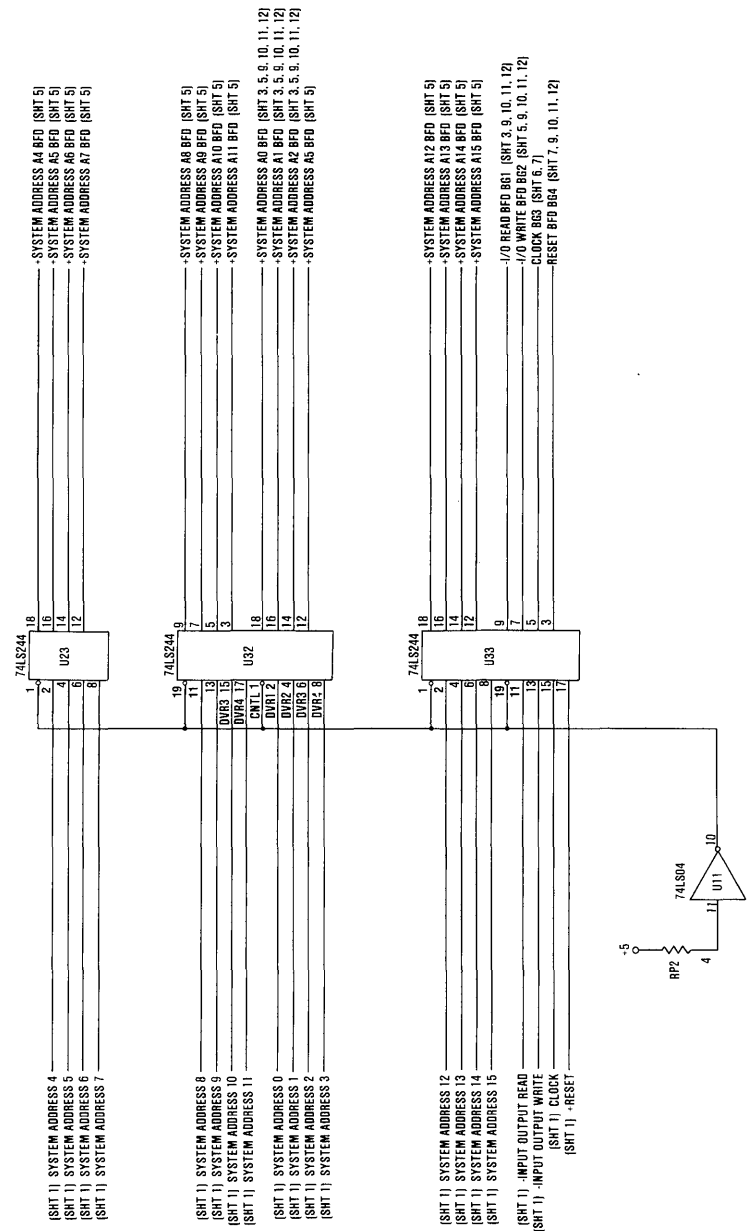


Sheet 2 of 12

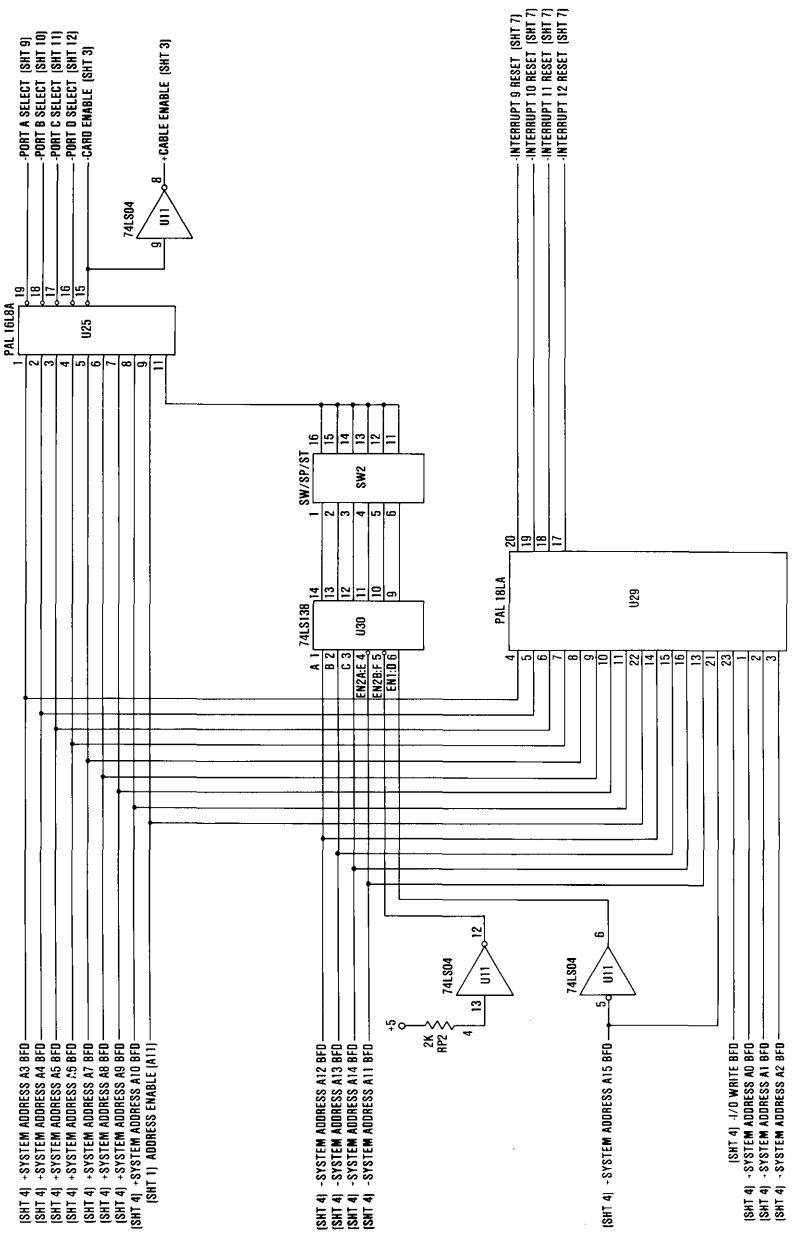

EXTERNAL CONNECTOR
E02
E01
E03
E10
F02
F01
F03
F10
G02
G01
G03
G10
H02
H01
H03
H10
E06
E08
E07
E09
E04
F06
F08
F07
F09
F04
G06
G08
G07
G09
G04
H06
H08
H07
H09
H04
[SHT 9] CHANNEL A DATA TERMINAL READY
[SHT 9] CHANNEL A SERIAL DATA OUT
[SHT 9] CHANNEL A REQUEST TO SEND
[SHT 10] CHANNEL B DATA TERMINAL READY
[SHT 10] CHANNEL B SERIAL DATA OUT
[SHT 10] CHANNEL B REQUEST TO SEND
[SHT 11] CHANNEL C DATA TERMINAL READY
[SHT 11] CHANNEL C SERIAL DATA OUT
[SHT 11] CHANNEL C REQUEST TO SEND
[SHT 12] CHANNEL D DATA TERMINAL READY
[SHT 12] CHANNEL D SERIAL DATA OUT
[SHT 12] CHANNEL D REQUEST TO SEND
CHANNEL A RECEIVE DATA [SHT 9]
+CHANNEL A CLEAR TO SEND [SHT 9]
+CHANNEL A DATA SET READY [SHT 9]
+CHANNEL A DATA CARRIER DETECT [SHT 9]
+CHANNEL A RING INDICATE [SHT 9]
CHANNEL B RECEIVE DATA [SHT 10]
+CHANNEL B CLEAR TO SEND [SHT 10]
+CHANNEL B DATA SET READY [SHT 10]
+CHANNEL B DATA CARRIER DETECT [SHT 10]
+CHANNEL B RING INDICATE [SHT 10]
CHANNEL C RECEIVE DATA [SHT 11]
+CHANNEL C CLEAR TO SEND [SHT 11]
+CHANNEL C DATA SET READY [SHT 11]
+CHANNEL C DATA CARRIER DETECT [SHT 11]
+CHANNEL C RING INDICATE [SHT 11]
CHANNEL D RECEIVE DATA [SHT 12]
+CHANNEL D CLEAR TO SEND [SHT 12]
+CHANNEL D DATA SET READY [SHT 12]
+CHANNEL D DATA CARRIER DETECT [SHT 12]
+CHANNEL D RING INDICATE [SHT 12]


-ENABLE READ INTERRUPT STATUS
1/ENABLE
(SHT 9) +CHANNEL A INTERRUPT REQUEST
2/INPUT
U24
3
74LS125
CARD DATA BUS BIT 0 (SHT 9, 10, 11, 12)
13/ENABLE
(SHT 10) +CHANNEL B INTERRUPT REQUEST
12/INPUT
U24
11
74LS125
CARD DATA BUS BIT1 (SHT 9, 10, 11, 12)
4/ENABLE
(SHT 11) +CHANNEL C INTERRUPT REQUEST
5/INPUT
U24
6
74LS125
CARD DATA BUS BIT 2 (SHT 9, 10, 11, 12)
1/ENABLE
(SHT 12) +CHANNEL D INTERRUPT REQUEST
2/INPUT
U31
3
74LS125
CARD DATA BUS BIT 3 (SHT 9, 10, 11, 12)
+5
2K
RP2
74LS30
U4
(SHT 5) + CARD ENABLE
(SHT 4) + SYSTEM ADDRESS A2 BFD
(SHT 4) + SYSTEM ADDRESS A1 BFD
(SHT 4) + SYSTEM ADDRESS A0 BFD
74LS04
U2
(SHT 4) -I/O READ BFD
(SHT 5) -CARD ENABLE
74LS245
U28
DIR:D 1
-EN:E 19
CARD DATA BUS BIT 4 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 5 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 6 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 7 (SHT 9, 10, 11, 12)
CARD BUS BIT 7 (SHT 1)
CARD BUS BIT 6 (SHT 1)
CARD BUS BIT 5 (SHT 1)
CARD BUS BIT 4 (SHT 1)
CARD BUS BIT 3 (SHT 1)
CARD BUS BIT 2 (SHT 1)
CARD BUS BIT 1 (SHT 1)
CARD BUS BIT 0 (SHT 1)

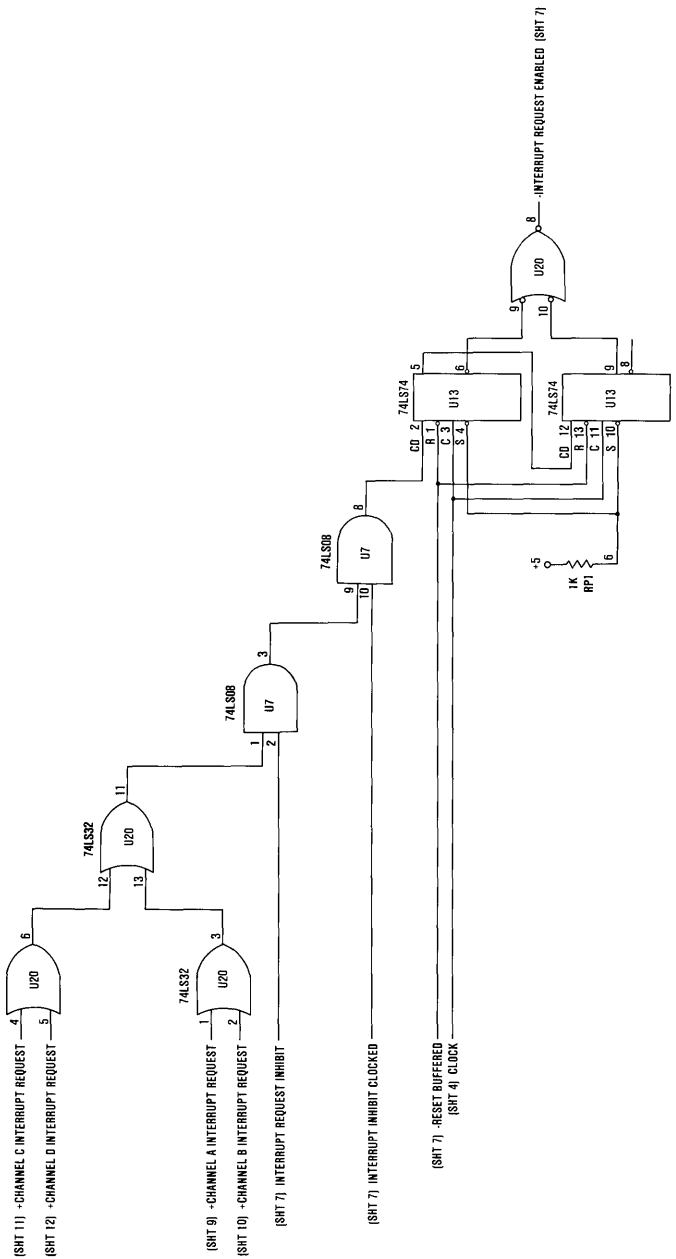
Sheet 4 of 12


74LS244
U23
U32
U33
74LS04
U11
RP2
-5
(SHT 1) SYSTEM ADDRESS 4
(SHT 1) SYSTEM ADDRESS 5
(SHT 1) SYSTEM ADDRESS 6
(SHT 1) SYSTEM ADDRESS 7
(SHT 1) SYSTEM ADDRESS 8
(SHT 1) SYSTEM ADDRESS 9
(SHT 1) SYSTEM ADDRESS 10
(SHT 1) SYSTEM ADDRESS 11
(SHT 1) SYSTEM ADDRESS 0
(SHT 1) SYSTEM ADDRESS 1
(SHT 1) SYSTEM ADDRESS 2
(SHT 1) SYSTEM ADDRESS 3
(SHT 1) SYSTEM ADDRESS 12
(SHT 1) SYSTEM ADDRESS 13
(SHT 1) SYSTEM ADDRESS 14
(SHT 1) SYSTEM ADDRESS 15
(SHT 1) -INPUT OUTPUT READ
(SHT 1) -INPUT OUTPUT WRITE
(SHT 1) CLOCK
(SHT 1) -RESET
+SYSTEM ADDRESS A4 BFD (SHT 5)
+SYSTEM ADDRESS A5 BFD (SHT 5)
+SYSTEM ADDRESS A6 BFD (SHT 5)
+SYSTEM ADDRESS A7 BFD (SHT 5)
+SYSTEM ADDRESS A8 BFD (SHT 5)
+SYSTEM ADDRESS A9 BFD (SHT 5)
+SYSTEM ADDRESS A10 BFD (SHT 5)
+SYSTEM ADDRESS A11 BFD (SHT 5)
+SYSTEM ADDRESS A0 BFD (SHT 3, 5, 9, 10, 11, 12)
+SYSTEM ADDRESS A1 BFD (SHT 3, 5, 9, 10, 11, 12)
+SYSTEM ADDRESS A2 BFD (SHT 3, 5, 9, 10, 11, 12)
+SYSTEM ADDRESS A3 BFD (SHT 5)
+SYSTEM ADDRESS A12 BFD (SHT 5)
+SYSTEM ADDRESS A13 BFD (SHT 5)
+SYSTEM ADDRESS A14 BFD (SHT 5)
+SYSTEM ADDRESS A15 BFD (SHT 5)
-I/O READ BFD BG1 (SHT 3, 9, 10, 11, 12)
-I/O WRITE BFD BG2 (SHT 5, 9, 10, 11, 12)
CLOCK BG3 (SHT 6, 7)
RESET BFD BG4 (SHT 7, 9, 10, 11, 12)
DVR1
DVR2
DVR3
DVR4
CNTL

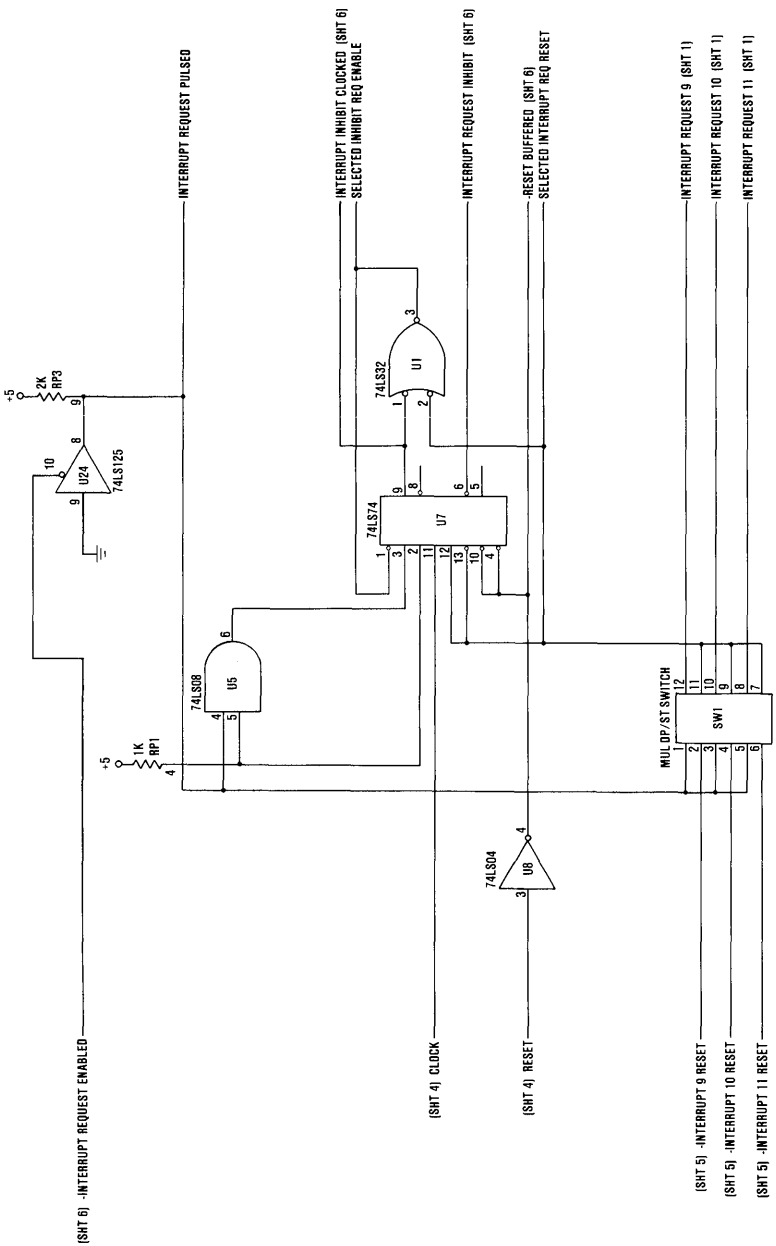
Sheet 5 of 12


PAL 16L8A
U25
74LS04
U11
74LS138
U30
SW/SP/ST
SW2
PAL 18L4
U29
2K
RP2
+5
-PORT A SELECT (SHT 9)
-PORT B SELECT (SHT 10)
-PORT C SELECT (SHT 11)
-PORT D SELECT (SHT 12)
-CARD ENABLE (SHT 3)
+CABLE ENABLE (SHT 3)
-INTERRUPT 9 RESET (SHT 7)
-INTERRUPT 10 RESET (SHT 7)
-INTERRUPT 11 RESET (SHT 7)
-INTERRUPT 12 RESET (SHT 7)
(SHT 4) -SYSTEM ADDRESS A3 BFD
(SHT 4) -SYSTEM ADDRESS A4 BFD
(SHT 4) -SYSTEM ADDRESS A5 BFD
(SHT 4) -SYSTEM ADDRESS A6 BFD
(SHT 4) -SYSTEM ADDRESS A7 BFD
(SHT 4) -SYSTEM ADDRESS A8 BFD
(SHT 4) -SYSTEM ADDRESS A9 BFD
(SHT 4) -SYSTEM ADDRESS A10 BFD
(SHT 1) ADDRESS ENABLE (A11)
(SHT 4) -SYSTEM ADDRESS A12 BFD
(SHT 4) -SYSTEM ADDRESS A13 BFD
(SHT 4) -SYSTEM ADDRESS A14 BFD
(SHT 4) -SYSTEM ADDRESS A11 BFD
(SHT 4) -SYSTEM ADDRESS A15 BFD
(SHT 4) -I/O WRITE BFD
(SHT 4) -SYSTEM ADDRESS A0 BFD
(SHT 4) -SYSTEM ADDRESS A1 BFD
(SHT 4) -SYSTEM ADDRESS A2 BFD

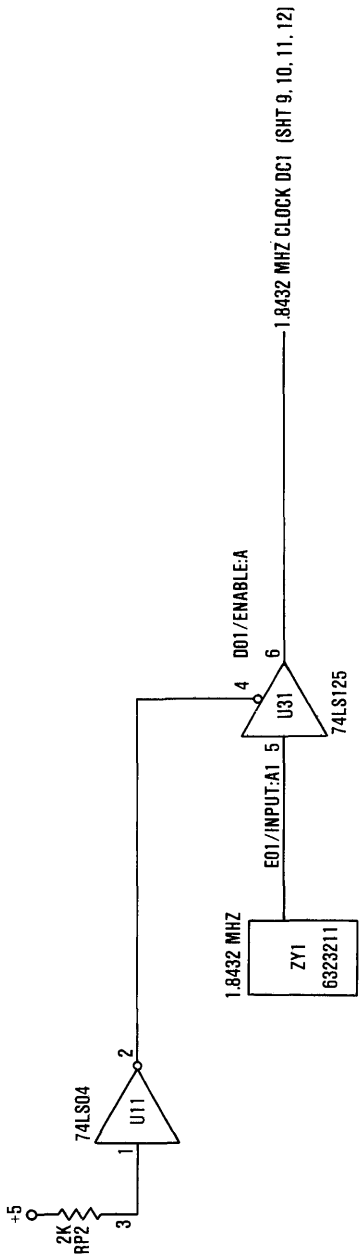
Sheet 6 of 12

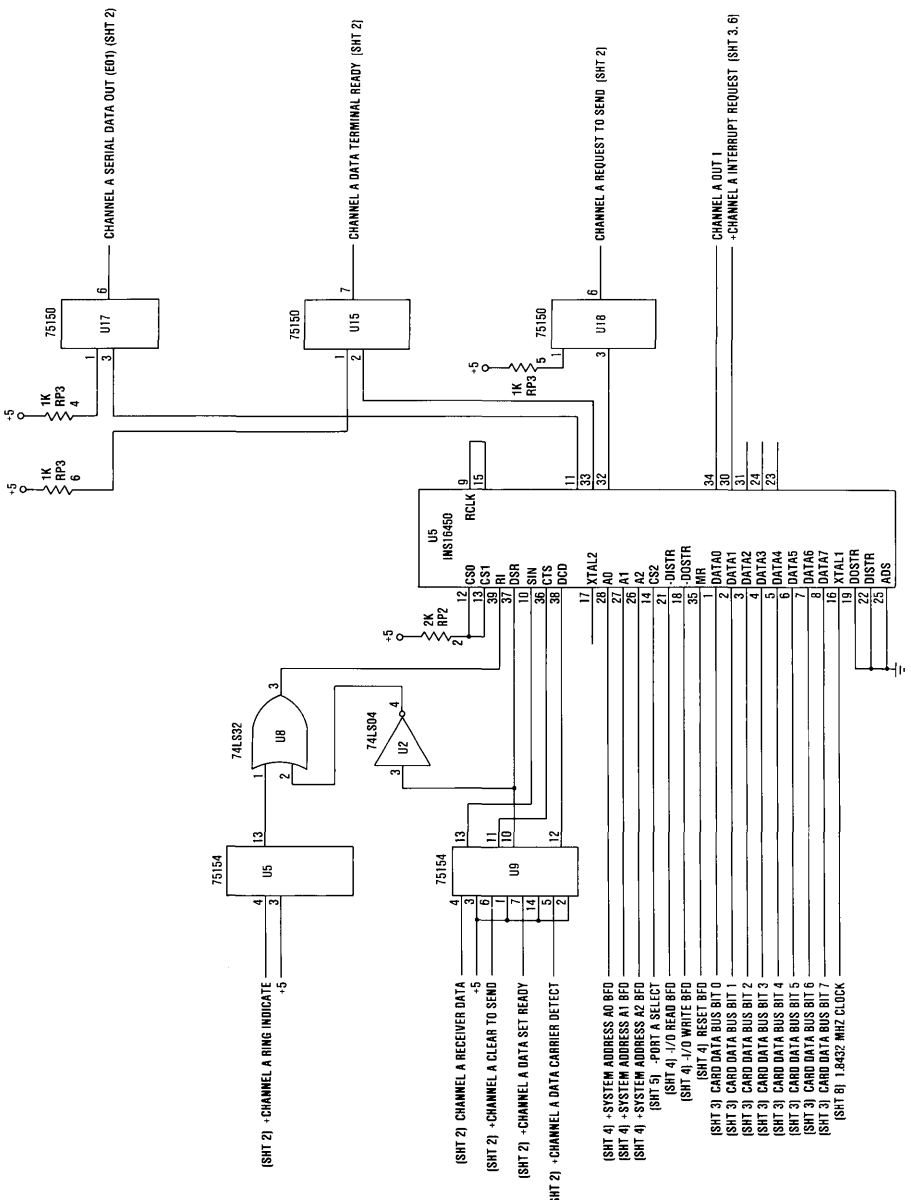

(SHT 11) +CHANNEL C INTERRUPT REQUEST
(SHT 12) +CHANNEL D INTERRUPT REQUEST
(SHT 9) +CHANNEL A INTERRUPT REQUEST
(SHT 10) +CHANNEL B INTERRUPT REQUEST
(SHT 7) INTERRUPT REQUEST INHIBIT
(SHT 7) INTERRUPT INHIBIT CLOCKED
(SHT 7) -RESET BUFFERED
(SHT 4) CLOCK
-INTERRUPT REQUEST ENABLED (SHT 7)
74LS32
74LS08
74LS74
U20
U7
U13
+5
1K
RP1

Sheet 7 of 12

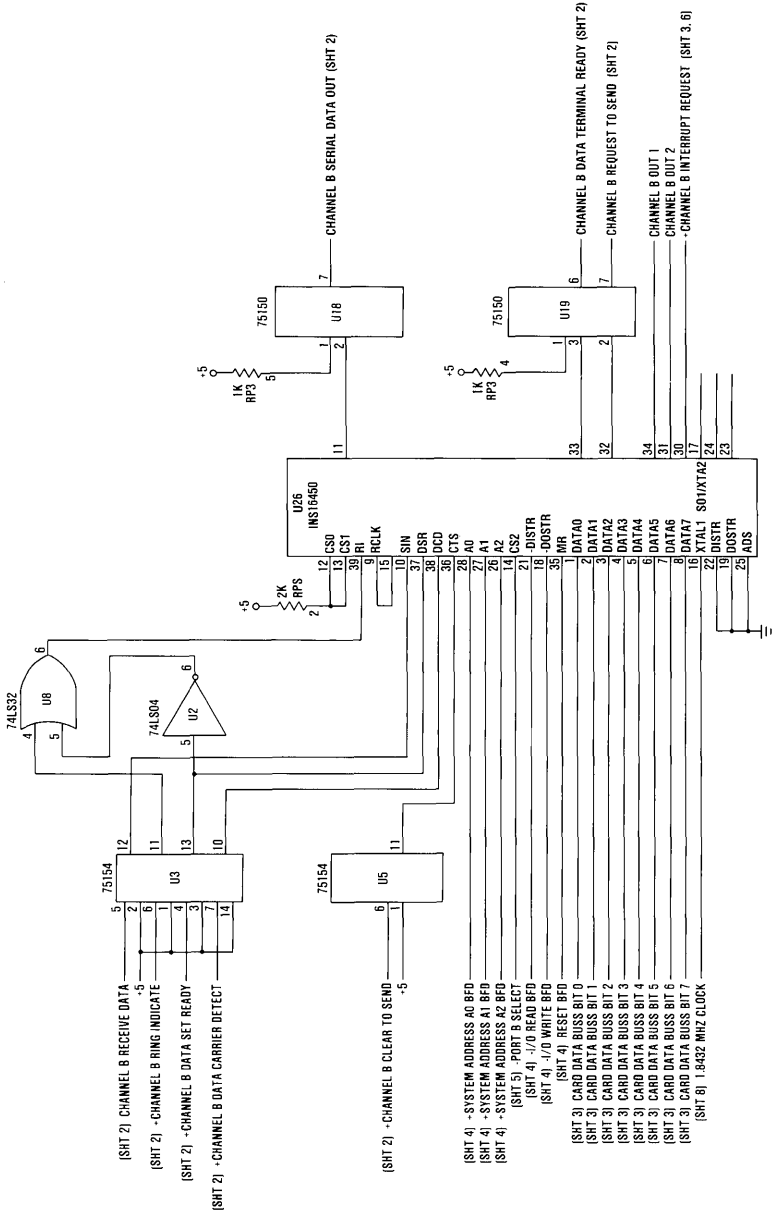

INTERRUPT REQUEST PULSED
INTERRUPT INHIBIT CLOCKED (SHT 6)
SELECTED INHIBIT REQ ENABLE
INTERRUPT REQUEST INHIBIT (SHT 6)
RESET BUFFERED (SHT 6)
SELECTED INTERRUPT REQ RESET
INTERRUPT REQUEST 9 (SHT 1)
INTERRUPT REQUEST 10 (SHT 1)
INTERRUPT REQUEST 11 (SHT 1)
+5
2K
RP3
U24
74LS125
74LS32
U1
74LS74
U7
74LS08
U5
+5
1K
RP1
74LS04
U8
MULTI DIP/ST SWITCH
SW1
(SHT 6) -INTERRUPT REQUEST ENABLED
(SHT 4) CLOCK
(SHT 4) RESET
(SHT 5) -INTERRUPT 9 RESET
(SHT 5) -INTERRUPT 10 RESET
(SHT 5) -INTERRUPT 11 RESET

Sheet 8 of 12

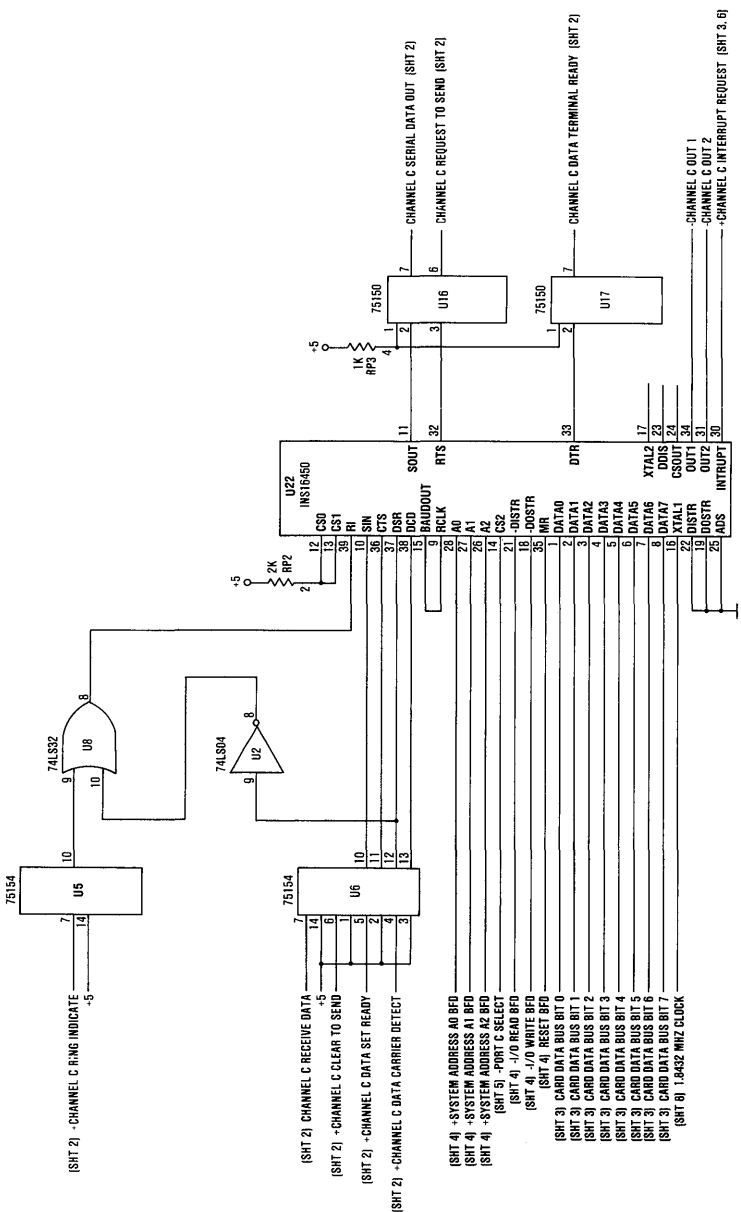

1.8432 MHZ CLOCK DC1 (SHT 9, 10, 11, 12)
DO1/ENABLE:A
U31
74LS125
EO1/INPUT:A1
1.8432 MHZ
ZY1
6323211
74LS04
U11
+5
2K
RP2


CHANNEL A SERIAL DATA OUT (E01) (SHT 2)
CHANNEL A DATA TERMINAL READY (SHT 2)
CHANNEL A REQUEST TO SEND (SHT 2)
CHANNEL A OUT 1
+CHANNEL A INTERRUPT REQUEST (SHT 3, 6)
75150
U17
U15
U18
1K RP3
+5
U5 INS16450
RCLK
CS0
CS1
RI
DSR
SIN
CTS
DCD
XTAL2
A0
A1
A2
CS2
-DISTR
-DOSTR
MR
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
XTAL1
DOSTR
DISTR
ADS
2K RP2
74LS32
U8
74LS04
U2
75154
U5
U9
(SHT 2) +CHANNEL A RING INDICATE
(SHT 2) CHANNEL A RECEIVER DATA
(SHT 2) +CHANNEL A CLEAR TO SEND
(SHT 2) +CHANNEL A DATA SET READY
(SHT 2) +CHANNEL A DATA CARRIER DETECT
(SHT 4) +SYSTEM ADDRESS A0 BFD
(SHT 4) +SYSTEM ADDRESS A1 BFD
(SHT 4) +SYSTEM ADDRESS A2 BFD
(SHT 5) -PORT A SELECT
(SHT 4) -I/O READ BFD
(SHT 4) -I/O WRITE BFD
(SHT 4) RESET BFD
(SHT 3) CARD DATA BUS BIT 0
(SHT 3) CARD DATA BUS BIT 1
(SHT 3) CARD DATA BUS BIT 2
(SHT 3) CARD DATA BUS BIT 3
(SHT 3) CARD DATA BUS BIT 4
(SHT 3) CARD DATA BUS BIT 5
(SHT 3) CARD DATA BUS BIT 6
(SHT 3) CARD DATA BUS BIT 7
(SHT 8) 1.8432 MHZ CLOCK

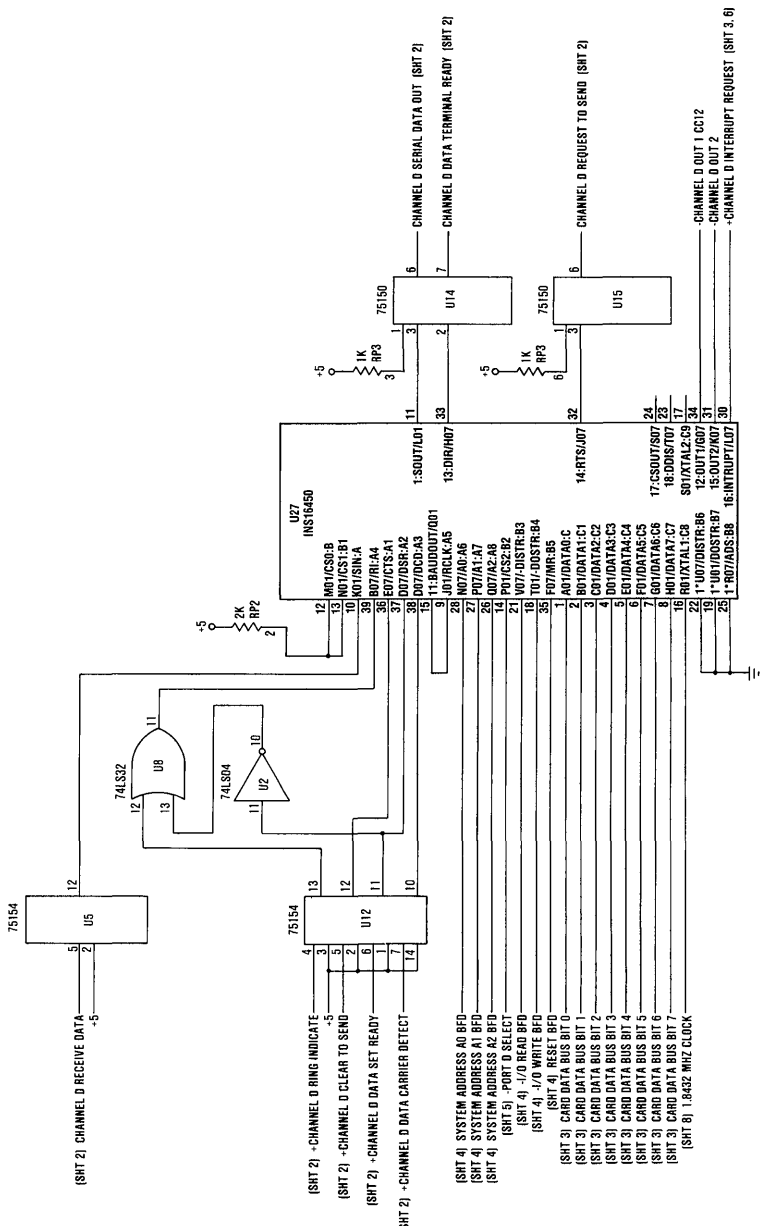
Sheet 10 of 12



Sheet 11 of 12



Sheet 12 of 12



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4-Port Asynchronous Adapter RS232C

4-PORT ASYNCHRONOUS ADAPTER RS232C

Contents

Description

The 4-Port Asynchronous RS-232C Adapter provides four serial output ports on a 4.25- by 13.12-inch board that plugs into one I/O position. The adapter system control signals and voltage requirements are provided through a 2- by 31-position and a 2- by 18-position tab on the bottom of the adapter.

Up to four adapters may be used in one &sailboat. system. A DIP switch on the adapter is used to assign the adapter's I/O address range. The port I/O address assignments are contained in the adapter's I/O address range.

The adapter is fully programmable and supports asynchronous communications only. It will add and remove start bits, stop bits, and parity bits. A programmable baud-rate generator allows operation from 50 bps to 19200 bps. Five-, 6-, 7- or 8-bit characters with 1, 1-1/2, or 2 stop bits are supported. A priority interrupt system controls transmit, receive, error, line status, and data set interrupts.

Four 10-pin male AMPMODU connectors on the adapter provide external access to the four ports.

There are two versions of this adapter, one uses the NS16450 LSI chip and the other uses the NS16550. Features in addition to those listed above include:

- Independent receiver clock input.
- Modem control functions: clear to send (CTS), request to send (RTS), data set ready (DSR), data terminal ready (DTR), ring indicator (RI), and received line signal detect (RLSD), which is also known as data carrier detect (DCD) or carrier detect (CD).
- False start bit detection.
- Line-break generation and detection.
- The NS16450 version has full double buffering that reduces the need for precise synchronization.
- The NS16550 is capable of running all existing NS16450 software in its character mode, and in its FIFO mode has a built-in 16 byte buffer for both receive and transmit operations for improved performance.

Note: The NS16550 (Buffered) adapter can be identified by a plus (+) sign stamped at the bottom of the 10-pin interface signals connector. See Figure 9 on page 9.

All pacing of the interface and control signal status must be handled by the system software. Figure 1 on page 2 is a block diagram of the 4-Port Asynchronous RS-232C Adapter.

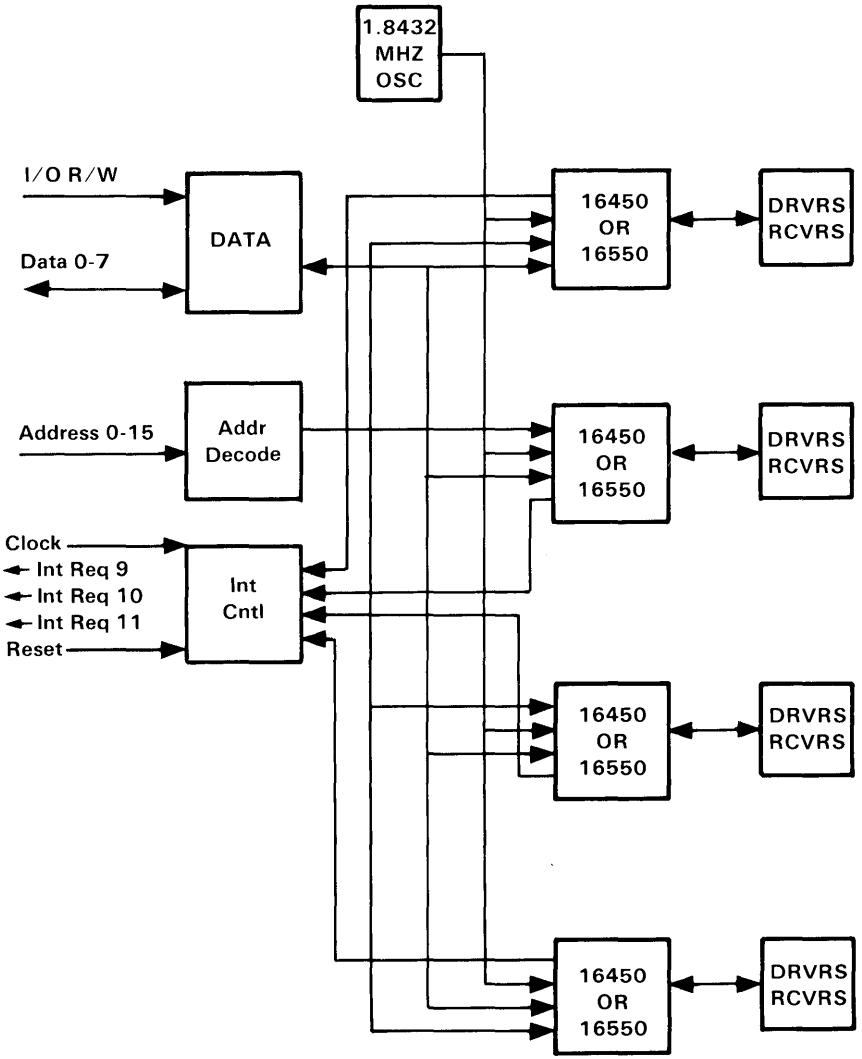


Figure 1. 4-Port Asynchronous RS-232C Adapter Block Diagram

4-Port Asynchronous RS-232C Adapter Switch Settings

The 4-Port Asynchronous RS-232C Adapter switch settings select the interrupt level and the address range of adapters installed.

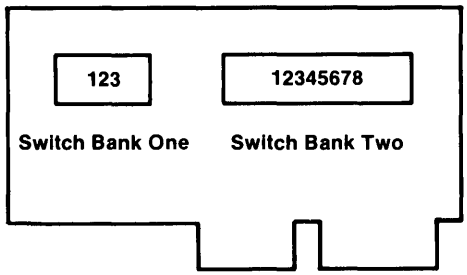


Figure 2. 4-Port Asynchronous RS-232C Adapter Switches

Interrupt Level Selected	Switch Bank One Setting		
	Switch 1	**Switch 2**	**Switch 3**
Level 9	On	Off	Off
Level 10	Off	On	Off
Level 11	Off	Off	On

Figure 3. Switch Bank One Settings

Address Range of Adapters	Switch Bank Two Setting			
	Switch 1	**Switch 2**	**Switch 3**	**Switch 4**
1230-124F	On	Off	Off	Off
2230-224F	Off	On	Off	Off
3230-324F	Off	Off	On	Off
4230-424F	Off	Off	Off	On

Figure 4. Switch Bank Two Settings

Note: Switches 5 through 8 are not used.

Modes of Operation

The different modes of operation are selected by programming the NS16450/NS16550 asynchronous communications element. Address bits A0, A1, and A2 select the different registers that define the modes of operation. Also, the divisor latch access bit (bit 7) of the line control register is used to select certain registers.

The address range for this adapter is Hex 1230 through Hex 424F. Figure 5 and Figure 6 on page 6 depict a value of n which represents a variable determined by the setting of switch bank two. Switches 1, 2, 3, and 4 of switch bank two allow the adapter to operate and select the appropriate address range.

I/O Decode (In Hex) Port B	Port A	Register Selected	DLAB State
n238	n230	TX Buffer	DLAB = 0 (Write)
n238	n230	RX Buffer	DLAB = 0 (Read)
n238	n230	Divisor Latch LSB	DLAB = 1
n239	n231	Divisor Latch MSB	DLAB = 1
n239	n231	Interrupt Enable Register	DLAB = 0
n23A	n232	Interrupt Identification Register (Read)	
n23A	n232	FIFO Control Register (Write - NS16550 Only)	
n23B	n233	Line Control Register	
n23C	n234	Modem Control Register	
n23D	n235	Line Status Register	
n23E	n236	Modem Status Register	

Figure 5. I/O Decodes, Port A and Port B

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

I/O Decode (In Hex) Port D	Port C	Register Selected	DLAB State
n248	n240	TX Buffer	DLAB = 0 (Write)
n248	n240	RX Buffer	DLAB = 0 (Read)
n248	n240	Divisor Latch LSB	DLAB = 1
n249	n241	Divisor Latch MSB	DLAB = 1
n249	n241	Interrupt Enable Register	DLAB = 0
n24A	n242	Interrupt Identification Register (Read)	
n24A	n242	FIFO Control Register (Write - NS16550 Only)	
n24B	n243	Line Control Register	
n24C	n244	Modem Control Register	
n24D	n245	Line Status Register	
n24E	n246	Modem Status Register	

Figure 6. I/O Decodes, Port C and Port D

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

A9—>A3 Decode	A2	A1	A0	DLAB	Register
See	x	x	x		
Note 1	0	0	0	0	Receive Buffer Reg. (Read) Transmit Holding Reg. (Write)
	0	0	1	0	Interrupt Enable
	0	1	0	x	Interrupt Identification (Read Only)
	0	1	0	x	FIFO Control (Write - NS16550 Only)
	0	1	1	x	Line Control
	1	0	0	x	Modem Control
	1	0	1	x	Line Status
	1	1	0	x	Modem Status
	1	1	1	x	Scratch (See note 3)
	0	0	0	1	Divisor Latch (LSB)
	0	0	1	1	Divisor Latch (MSB)

Figure 7. Address Bits

Notes:

1. Bits A9 through A3 are used to select specific adapter and serial port.
2. A2, A1, and A0 bits are *don't cares* and are used to select the different registers of the NS16450/NS16550 chip.
3. The Scratch Register of the NS16450/NS16550 module should be initialized to all ones and never be written to with any data afterwards. This would cause indeterminate data when Read address n237 (see "Interrupts" on page 8) is executed.

Interrupts

Three interrupt lines are provided to the system. The interrupt level (9, 10, or 11) is selected by placing the appropriate switch on switch bank one to the on position. An interrupt register (read adr n237, where n is first digit of the address range) is provided for storage of pending port interrupts. Interrupt register bit assignments are shown in Figure 8.

Hex Address n237							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	Port 4	Port 3	Port 2	Port 1

Figure 8. Interrupt Register Read Format

Before the 4-Port Asynchronous RS-232C Adapter can generate an interrupt to the processor, it must be enabled by writing any data byte to the interrupt enable address. This address corresponds to the interrupt level that the adapter is jumpered for.

The enable for interrupt level 9 is hex address 02F2.

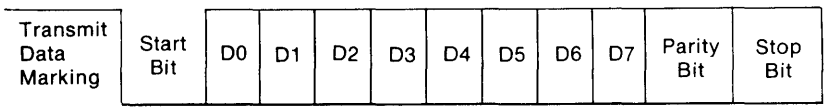
The enable for interrupt level 10 is hex address 06F2.

The enable for interrupt level 11 is hex address 06F3.

After the adapter generates an interrupt, it must be reset by writing any data byte to the interrupt enable address for that interrupt.

Serial Data Format

The data format is as follows:



Data bit 0 is the first bit to be transmitted or received. The adapter automatically inserts the start bit, the correct parity bit (if programmed to do so), and the stop bit (1, 1-1/2, or 2 depending on the command in the line control register).

External Interface Description

The adapter provides an EIA 4-Port Asynchronous RS-232C Adapter-like interface.

The pin functions for the 10-pin male connector are shown in Figure 9.

Pin	Signal
1	Transmit Data
2	Data Terminal Ready
3	Request to Send
4	Ring Indicate
5	No Connection
6	Receive Data
7	Data Set Ready
8	Clear to Send
9	Data Carrier
10	Signal Ground

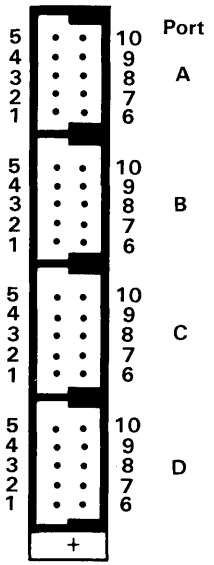


Figure 9. 10-Pin Interface Signals Connector (viewed from rear of adapter)

The adapter converts the interface signals from TTL levels to EIA 4-Port Asynchronous RS-232C Adapter voltage levels, and vice versa. These signals are sampled or generated by the communications control chip. These signals can then be sensed by the system software to determine the state of the interface or peripheral device. The drivers and receivers used on the adapter are the inverting type; therefore, a 0 EIA level on the line is received or transmitted as a 0 TTL level, and a 1 EIA level is received or transmitted as a 1 TTL level.

Voltage Interchange Information

The signal will be considered in the marking condition when the voltage on the interchange circuit, measured at the interface point, is more negative than -3 Vdc with respect to signal ground. The signal will be considered in the spacing condition when the voltage is more positive than + 3 Vdc with respect to signal ground. The region between + 3 Vdc and -3 Vdc is defined as the transition region and is considered an invalid level. The voltage that is more negative than -15 Vdc or more positive than + 15 Vdc is also considered an invalid level.

During the transmission of data, the marking condition denotes the binary state 1 and the spacing condition denotes the binary state 0.

For interface control circuits, the function is on when the voltage is more positive than + 3 Vdc with respect to signal ground and is off when the voltage is more negative than -3 Vdc with respect to signal ground.

Interchange Voltage	Binary State	Signal Condition	Interface Control Function
Positive Voltage	Binary 0	Spacing	= On
Negative Voltage	Binary 1	Marking	= Off

Figure 10. 4-Port Asynchronous RS-232C Adapter Signal Levels

Asynchronous Communications Element Pin Description

The following describes the function of all NS16450/NS16550 input/output pins. Some of these descriptions reference internal circuits. The use of each signal as implemented on the multiport adapter is described.

Note: In the following descriptions, a low represents a logic 0 (0 Vdc nominal) and a high represents a logic 1 (+ 2.4 Vdc nominal).

Input Signals

Chip Select (CS0, CS1, -CS2), Pins 12-14: When CS0 and CS1 are high and -CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) address strobe (-ADS) input. This enables communications between the NS16450/NS16550 and the processor.

Data Input Strobe (DISTR, -DISTR), Pins 22 and 21: When DISTR is high or -DISTR is low while the chip is selected, the processor can read status information or data from a selected register of the NS16450/NS16550.

Note: Only one active DISTR or -DISTR input is required to transfer data from the NS16450/NS16550 during a read operation. Therefore, the DISTR input has been permanently tied low and the -DISTR line is used.

Data Output Strobe (DOSTR, -DOSTR), Pins 19 and 18: When DOSTR is high or -DOSTR is low while the chip is selected, the processor can write data or control words into a selected register of the NS16450/NS16550.

Note: Only one active DOSTR or -DOSTR input is required to transfer data to the NS16450/NS16550 during a write operation. Therefore, the DOSTR input has been permanently tied low and the -DOSTR input is used.

-Address Strobe (-ADS), Pin 25: When low, this signal provides latching for the register select (A0, A1, A2) and chip select (CS0, CS1, -CS2) signals.

Note: The -ADS input has been tied low because the register select (A0, A1, A2) signals are stable for the duration of read and write operations.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an NS16450/NS16550 register to read from or write into as indicated in Figure 11. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain NS16450/NS16550 registers. The DLAB must be set high by the system software to access the baud-generator divisor latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (Read)
0	0	0	0	Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable
x	0	1	0	Interrupt Identification (Read Only)
x	0	1	0	FIFO Control (Write - NS16550 Only)
x	0	1	1	Line Control
x	1	0	0	Modem Control
x	1	0	1	Line Status
x	1	1	0	Modem Status
x	1	1	1	Scratch
1	0	0	0	Divisor Latch (Least Significant Byte)
1	0	0	0	Divisor Latch (Most Significant Byte)

Figure 11. NS16450/NS16550 Register Selection

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low, 0-3 Forced and 4-7 Permanent
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 are Low, and Bits 3-7 are Permanent
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
Modem Status Register	Master Reset	Bits 0-3 are Low, Bits 4-7 = Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errors)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IRR/ Write THR/ MR	Low
RCVR FIFO	MR/ FCR1•FCR0/ ΔFCR0	Low

Figure 12 (Part 1 of 2). NS16450/NS16550 Reset Functions

Register/Signal	Reset Control	Reset State
XMIT FIFO	MR/ FCR2•FCR0/ ΔFCR0	Low
FIFO Control Register	Master Reset	Low
INTRPT (Modem Status Changes)	Read MSR/ MR	Low
-OUT 2 -RTS -DTR -OUT 1	Master Reset Master Reset Master Reset Master Reset	High High High High

Figure 12 (Part 2 of 2). NS16450/NS16550 Reset Functions

Master Reset (MR), Pin 35: When high, this signal clears all the registers (except the receive buffer, transmitter holding, and divisor latches), and the control logical of the NS16450/ NS16550. Also, the state of various output signals (SOUT, INTRPT, -OUT 1, -OUT 2, -RTS, -DTR) is affected by an active MR input. Refer to Figure 12 on page 13.

Receiver Clock (RCLK), Pin 9: This input is the 16x baud-rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, modem, or data set).

-Clear to Send (-CTS), Pin 36: The -CTS signal is a modem control function input whose condition can be tested by the processor by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates whether the -CTS input has changed state since the previous reading of the modem status register.

Note: Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

-Data Set Ready (-DSR), Pin 37: The -DSR signal is a modem control function input whose condition can be tested by the processor by reading bit 5 (DSR) of the modem status register. When low, this signal indicates that the modem or data set is ready to establish the communications link and transfer data with the NS16450/NS16550. Bit 1 (DDSR) of the modem status register indicates whether the -DSR input has changed since the previous reading of the modem status register.

Note: Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

-Received Line Signal Detect (-RLSD), Pin 38: The -RLSD signal is a modem control function input whose condition the processor can test by reading bit 7 (RLSD) of the modem status register. When low, this signal indicates that the data carrier had been detected by the modem or data set. Bit 3 (DRLSD) of the modem status register indicates whether the -RLSD input has changed state since the previous reading of the modem status register.

Notes:

1. Whenever the RLSD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.
2. Received Line Signal Detect is also called Data Carrier Detect (DCD), or Carrier Detect (CD).

-Ring Indicator (-RI), Pin 39: The -RI signal is a modem control function input whose condition the processor can test by reading bit 6 (RI) of the modem status register. When low, this signal indicates that a telephone ringing signal has been received by the modem or data set. Bit 2 (TERI) of the modem status register indicates whether the -RI input has changed from a low to high state since the previous reading of the modem status register.

Note: Whenever the RI bit of the modem status register changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.

VCC, Pin 40: + 5 Vdc supply

VSS, Pin 20: Ground (0 Vdc) reference.

Output Signals

-Data Terminal Ready (-DTR), Pin 33: When low, this signal informs the modem or data set that the NS16450/NS16550 is ready to communicate. The -DTR output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. The -DTR signal is set high by a master reset operation. The -DTR signal is set high during loop mode operation.

-Request to Send (-RTS), Pin 32: When low, this signal informs the modem or data set that the NS16450/NS16550 is ready to transmit data. The -RTS output signal can be set to an active low by programming bit 1 (RTS) of the modem control register. The -RTS signal is set high by a master reset operation. The -RTS signal is set high during loop mode operation.

-Output 1 (-OUT 1), Pin 34: With this signal, user-designated output can be set to an active low by programming bit 2 (-OUT 1) of the modem control register to a high level. The -OUT 1 signal is set high by a master reset operation. The -OUT 1 signal is set high during the loop mode operation. This adapter does not use this signal.

-Output 2 (-OUT 2), Pin 31: With this signal, user-designated output can be set to an active low by programming bit 3 (-OUT 2) of the modem control register to a high level. The -OUT 2 signal is set high by a master reset operation. The -OUT 2 signal is set high during the loop mode operation. This adapter does not use this signal.

Chip Select Out (CSOUT), Pin 24, NS16450 Only: When high, this signal indicates that the chip has been selected by active CS0, CS1, and -CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. This signal is not used.

TXRDY, RXRDY, Pins 24, 29, NS16550 Only: Transmitter and Receiver pins for DMA signaling. The adapter does not use these pins.

Driver Disable (DDIS), Pin 23: This signal goes low whenever the processor is reading data from the NS16450/NS16550. The adapter does not use this signal.

-Baudout (-BAUDOUT), Pin 15: This signal is a 16x clock signal for the transmitter section of the NS16450/NS16550. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud-generator division latches. The -Baudout is also used for the receiver section.

Interrupt (INTRPT), Pin 30: This signal goes high whenever any one of the following interrupt types has an active high condition and is enabled through the IER: receiver error flag, received data available, transmitter holding register empty, or modem status. For the NS16550, the signal also goes high for timeout (FIFO mode only). The Intrpt signal is reset low upon the appropriate interrupt service or a master reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, modem or data set). The SOUT signal is set to the marking (logic 1) state upon a master reset operation.

Input/Output Signals

Data Bus (D7-D0), Pins 1-8: This bus comprises eight tri-state input/output lines. The bus provides bidirectional communications between the NS16450/NS16550 and the processor. Data, control words, and status information are transferred through the D7-D0 data bus.

External Clock Input/Output (XTAL1, XTAL2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the NS16450/NS16550.

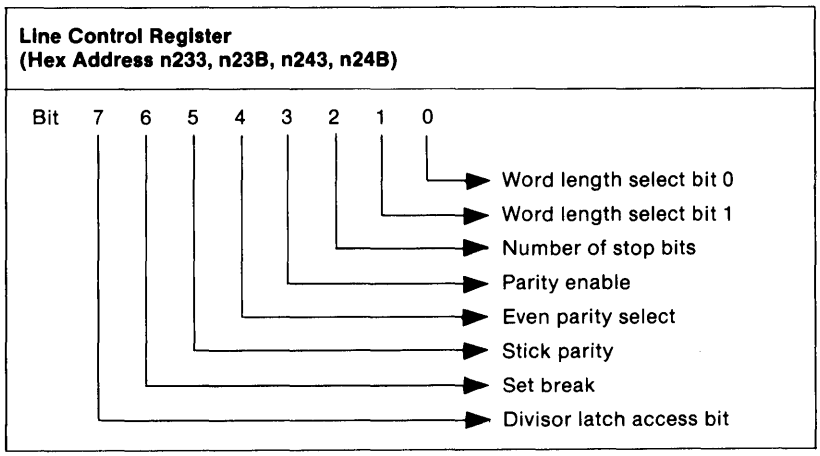
Programming Considerations

The NS16450/NS16550 has a number of accessible registers. The system programmer may access or control any of the NS16450/NS16550 registers through the processor. These registers are used to control NS16450/NS16550 operations and to transmit and receive data.

Note: The n in address is the card number (1-4).

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange through the line control register. In addition to controlling the format, the programmer may retrieve the contents of the line control register for inspection. This feature simplifies system programming and eliminates the need for separate storage of the line characteristics in system memory. The contents of the line control register are described below:



Bits 0, 1 These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2 This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logical 0, one stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logical 1 when a 5-bit word length is selected through bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is a logical 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated or checked.

Bit 3 This bit is the parity enable bit. When bit 3 is a logical 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed.)

Bit 4 This bit is the even parity select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's are transmitted or checked in the data word bits and parity bit. When bit 3 is a logical 1 and bit 4 is a logical 1, an even number of bits are transmitted or checked.

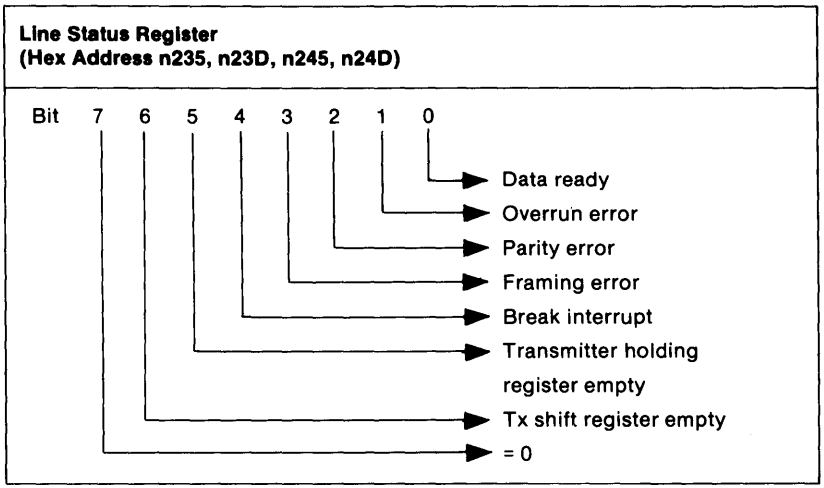
Bit 5 This bit is the stick parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is transmitted and then detected by the receiver as a logical 0 (space parity) if bit 4 is a logical 1, or as a logical 1 (mark parity) if bit 4 is a logical 0.

Bit 6 This bit is the set break control bit. When bit 6 is a logical 1, the serial output (SOUT) is forced to the spacing (logical 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logical 0. This feature enables the processor to alert a terminal in a computer communications system.

Bit 7 This bit is the divisor latch access bit (DLAB). It must be set high (logical 1) to access the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Line Status Register

This 8-bit register provides status information to the processor concerning the data transfer. The contents of the line status register are described below:



Bit 0 This bit is the receiver data ready (DR) indicator. Bit 0 is set to a logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register or the FIFO. Bit 0 may be reset to a logical 0 either by the processor reading the data in the receiver buffer or by writing a logical 0 into it from the processor.

Bit 1 This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the processor before the next character was transferred into the receiver buffer register, and that the previous character was thereby destroyed. The OE indicator is reset whenever the processor reads the contents of the line status register.

Bit 2 This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity as selected by the even parity-select bit. The PE bit is set to a logical 1 upon detection of a parity error and is reset to a logical 0 whenever the processor reads the contents of the line status register. For the NS16550 in the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the system when its associated character is at the top of the FIFO.

Bit 3 This bit is the framing error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logical 1 whenever the stop bit following the last data bit or parity is detected as a 0 bit (spacing level). The FE indicator is reset whenever the system reads the contents of the line status indicator. For the NS16550 in the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the system when its associated character is at the top of the FIFO.

Bit 4 This bit is the break interrupt (BI) indicator. Bit 4 is set to a logical 1 whenever the received data input is held in the spacing (logical 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits). The BI indicator is reset whenever the system reads the contents of the line status indicator. For the NS16550 in the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the system when its associated character is at the top of the FIFO. When break occurs only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected.

Bit 5 This bit is the transmitter holding register empty (THRE) indicator. Bit 5 indicates that the NS16450/NS16550 is ready to accept a new character for transmission. In addition, this bit causes the NS16450/NS16550 to issue an interrupt to the processor when the transmit holding register empty interrupt enable is set high. The THRE bit is set to a logical 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logical 0 concurrently with the loading of the transmitter holding register by the processor. For the NS16550 in the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.

Bit 6 This bit is the transmitter empty (TEMT) indicator. Bit 6 is set to a logical 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logical 0 whenever either the THR or TSR contain a data character. Bit 6 is a read-only bit. For the NS16550 in the FIFO mode, this bit is set to 1 whenever the transmitter FIFO and shift register are both empty.

Bit 7 In the character mode this is a 0. For the NS16550 in the FIFO mode, this bit is set when there is at least one parity error, framing error or break indication in the FIFO. Bit 7 is cleared when the processor reads the line status register, if there are no subsequent errors in the FIFO.

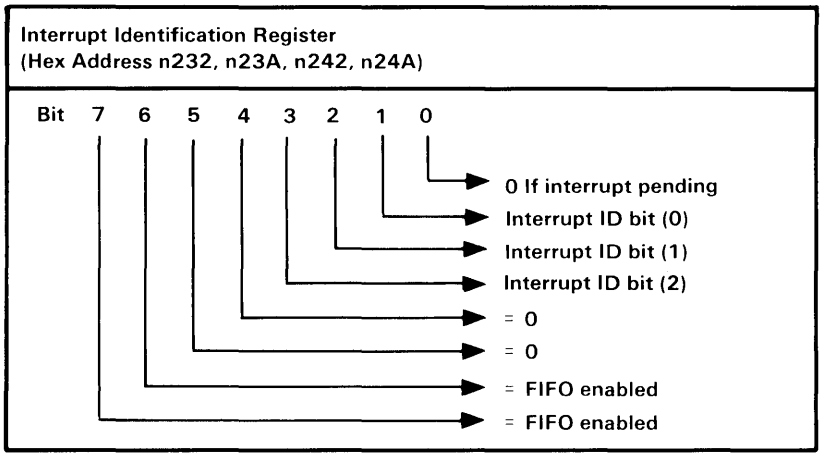
Note: The line status register is for read operations only.

Interrupt Identification Register

The NS16450/NS16550 has an on-chip interrupt capability that allows for complete flexibility in interfacing to microprocessors. In order to provide minimum software overhead during data character transfers, the NS16450/NS16550 sets interrupts into four priority levels:

- Receiver line status (priority 1)
- Received data ready (priority 2), or for the NS16550 in the FIFO mode, timeout in the FIFO.
- Transmitter holding register empty (priority 3)
- Modem status (priority 4).

Information indicating that a priority interrupt is pending and information on the type of interrupt is stored in the interrupt identification register. Refer to the "Interrupt Control Functions" table in Figure 13 on page 22. The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending, and no other interrupts are acknowledged until that particular interrupt is serviced by the processor. The contents of the IIR are described below.



Bit 0 This bit can be used in a hardwired, priority, or polled environment to indicate whether an interrupt is pending. When bit 0 is a logical 0, an interrupt is pending and the IIR contents are used as a pointer to the appropriate interrupt service routine. When bit 0 is a logical 1, no interrupt is pending, and polling (if used) is continued.

Bits 1, 2 These 2 bits of the IIR are used to identify the highest priority interrupt pending as indicated in Figure 13 on page 22.

Bits 3-7 For the NS16450 these 5 bits of the IIR are always logical 0. For the NS16550:

Bit 3 In the character mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 - 5 These 2 bits of the IRR are always logical 0.

Bit 6 - 7 These 2 bits are set when FCR0 = 1.

Interrupt ID Register				Interrupt Set and Reset Functions			
Bit 3*	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt.	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or for NS16550, Trigger Level Reached	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time.	Reading the Receiver Buffer Register

Figure 13 (Part 1 of 2). Interrupt Control Functions

Interrupt ID Register				Interrupt Set and Reset Functions			
Bit 3*	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Figure 13 (Part 2 of 2). Interrupt Control Functions

Note: * = Applicable to NS16550 only.

FIFO Control Register

This is an 8-bit write only register (NS16550 only) at the same location as the interrupt identification register. This register enables the FIFOs, clears the FIFOs, sets the RCVR FIFO trigger level, and selects the type of DMA signaling.

Bit 0 Setting bit 0 to 1 enables both the XMIT and RCVR FIFOs. Resetting bit 0 clears all bytes in both FIFOs. When changing from FIFO mode to character mode and vice versa, data is not automatically cleared from the FIFOs. Therefore, the FIFOs should be cleared before changing modes. This bit must be a 1 when other FIFO control register bits are written to or they will not be programmed.

Bit 1 Setting bit 1 to 1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 written to this bit position is self clearing.

Bit 2 Setting bit 2 to 1 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 written to this bit position is self clearing.

Bit 3 Setting bit 3 to 1 changes the RXRDY and TXRDY pins from mode 0 to mode 1 if bit 0 = 1.

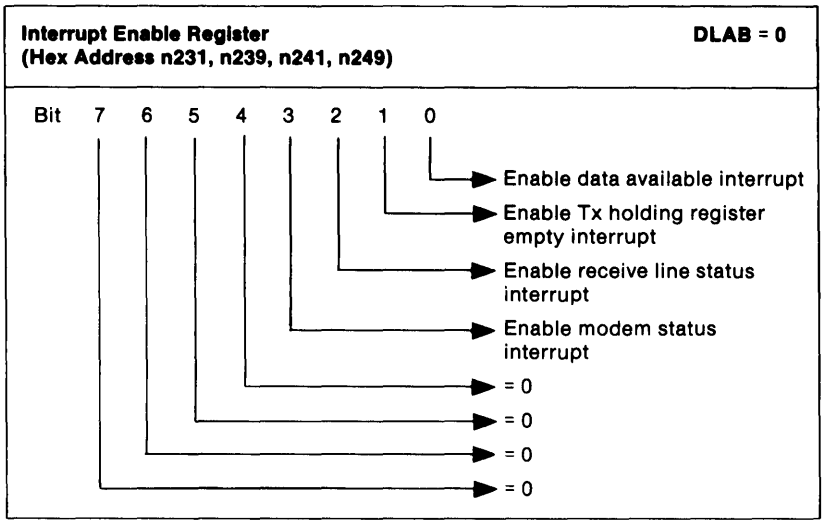
Bit 4, 5 Reserved

Bit 6,7 These two bits set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the NS16450/NS16550 to separately activate the chip interrupt (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the interrupt enable register. Similarly, setting the appropriate bits of this register to a logical 1, can enable selected interrupts. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are described below:



Bit 0 This bit enables the received data available interrupt and for the NS16550, timeout interrupts in the FIFO mode, when set to a logical 1.

Bit 1 This bit enables the transmitter holding register empty interrupt when set to a logical 1.

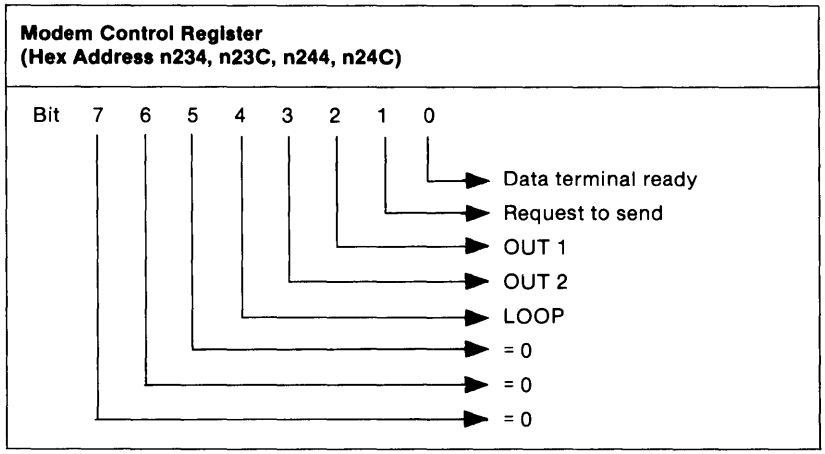
Bit 2 This bit enables the receiver line status interrupt when set to a logical 1.

Bit 3 This bit enables the modem status interrupt when set to a logical 1.

Bits 4-7 These four bits are always logical 0.

Modem Control Register

This 8-bit register controls the interface with the modem or data set (or other peripheral device). The contents of the modem control register are described below:



Bit 0 This bit controls the data terminal ready (-DTR) output. When bit 0 is set to a logical 1, the -DTR output is forced to a logical 0. When bit 0 is reset to a logical 0, the -DTR output is forced to a logical 1.

Note: The -DTR output of the NS16450/NS16550 is applied to an EIA inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 1 This bit controls the request to send (-RTS) output. Bit 1 affects the -RTS output in a manner identical to that described above for bit 0.

Note: The -RTS output of the NS16450/NS16550 is applied to an EIA-inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 2 This bit controls the output 1 (-OUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the -OUT 1 output in a manner identical to the proper polarity input at the modem or data set. This bit is not used by the adapter.

Bit 3 This bit controls the output 2 (-OUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the -OUT 2 output in a manner identical to that described above for bit 0. This bit is not used by the adapter.

Bit 4 This bit provides a loopback feature for diagnostic testing of the NS16450/NS16550. When bit 4 is set to logical 1, the following occurs:

The transmitter serial output (SOUT) is set to the marking (logical 1) state.

The receiver serial input (SIN) is disconnected.

The output of the transmitter shift register is *looped back* into the receiver shift register input.

The four modem control inputs (-CTS, -DSR, -RLSD, and -RI) are disconnected.

The four modem control outputs (-DTR, -RTS, -OUT 1, and -OUT 2) are internally connected to the four modem control inputs, and the modem control output pins are forced high.

In the the diagnostic mode the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the sources of the interrupts are now the lower 4 bits of the modem control register instead of the 4 modem control inputs. The interrupts are still controlled by the interrupt enable register.

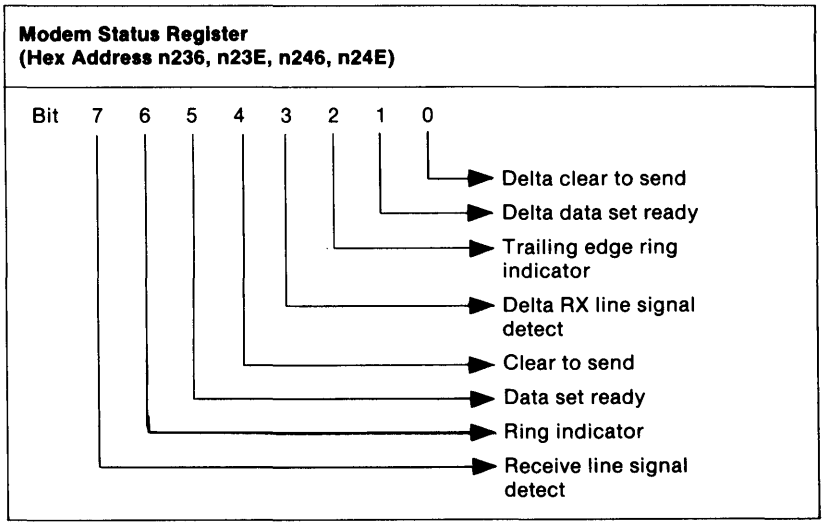
The NS16450/NS16550 interrupt system can be tested by writing into the lower 6 bits of the line status register and into the lower 4 bits of the modem status register. Setting any of these bits to a logical 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal NS16450/ NS16550 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the modem control register must be reset to logical 0. The transmitter should be idle when this bit changes state.

Bits 5-7 These bits are permanently set to logical 0.

Modem Status Register

This 8-bit register provides the current state of the control lines from the modem (or peripheral device) to the processor. In addition to this current-state information, four bits of the modem status register provide change information. These bits are set to a logical 1 whenever a control input from the modem changes state. They are reset to logical 0 whenever the processor reads the modem status register.

The contents of the modem status register are described below:



Bit 0 This bit is the delta clear-to-send (DCTS) indicator. Bit 0 indicates that the -CTS input to the chip has changed state since the last time it was read by the processor.

Bit 1 This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the -DSR input to the chip has changed state since the last time it was read by the processor.

Bit 2 This bit is the trailing edge of the ring indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from an ON (logical 1) to an OFF (logical 0) condition.

Bit 3 This bit is the delta received line signal detector (DRLSD) indicator. Bit 3 indicates that the -RLSD input to the chip has changed state since the last time it was read by the processor.

Note: Whenever bit 0, 1, 2, or 3 is set to a logical 1, a modem status interrupt is generated, if the appropriate interrupt enable bit is set in the IER.

Bit 4 This bit is the complement of the clear to send (-CTS) input. Setting bit 4 (loop) of the MCR to a logical 1, is equivalent to RTS in the MCR.

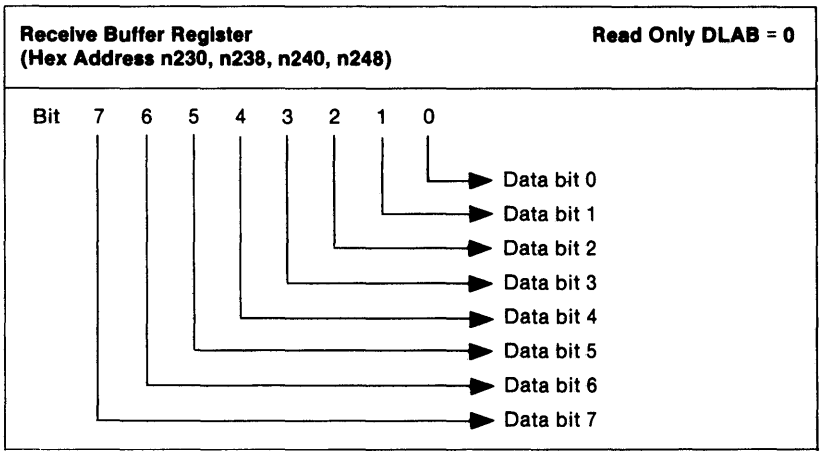
Bit 5 This bit is the complement of the data set ready (-DSR) input. If bit 4 (loop) of the MCR is set to a logical 1, this bit is equivalent to DTR in the MCR.

Bit 6 This bit is the complement of the ring indicator (-RI) input. If bit 4 (loop) of the MCR is set to a logical 1, this bit is equivalent to -OUT 1 in the MCR.

Bit 7 This bit is the complement of the received line signal detect (-RLSD) input. If bit 4 (loop) of the MCR is set to a logical 1, this bit is equivalent to -OUT 2 of the MCR.

Receiver Buffer Register

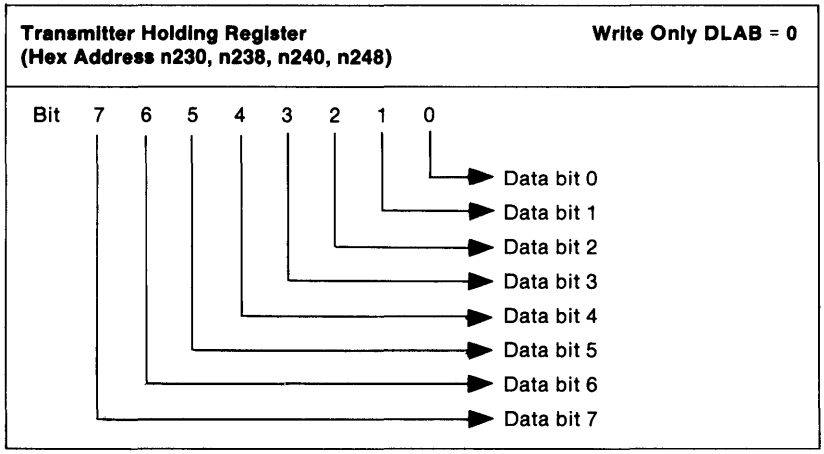
The receiver buffer register contains the received character as defined below:



Bit 0 is the least significant bit and is the first bit serially received.

Transmitter Holding Register

The transmitter holding register contains the character to be serially transmitted and is defined below:



Bit 0 is the least significant bit and is the first bit serially transmitted.

Programmable Baud-Rate Generator

The NS16450/NS16550 contains a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 655,535 or 2^{16}-1. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to insure desired operation of the baud-rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The following figures show the contents of the divisor latches.

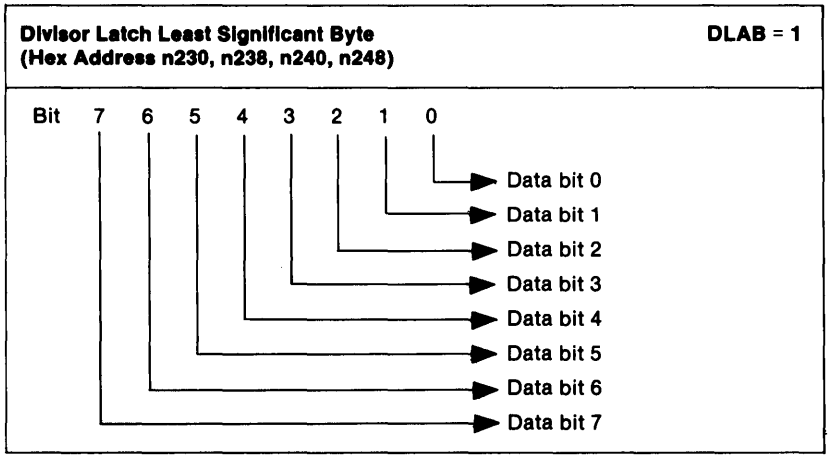


Figure 14. Divisor Latch Least Significant Byte

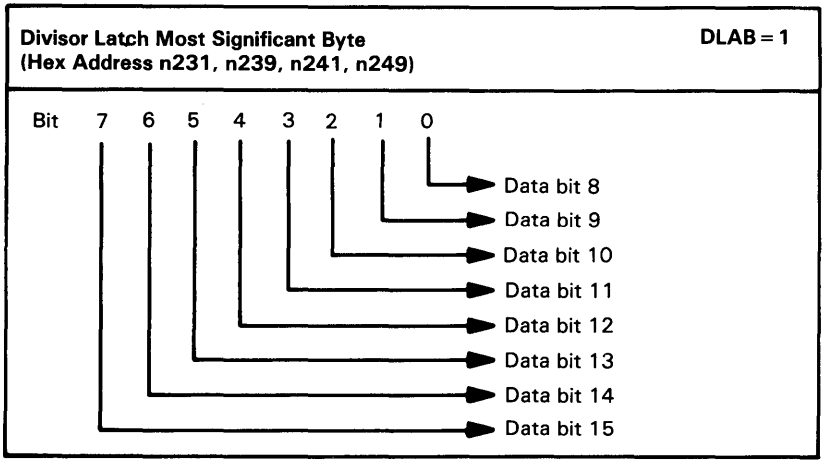


Figure 15. Divisor Latch Most Significant Byte

Figure 16 illustrates the use of the baud-rate generator with a frequency of 1.8432 MHz. For baud rates of 19,200 and below, the error obtained is minimal.

Note: The maximum operating frequency of the baud generator is 3.1 MHz. In no case should the data rate be greater than 19,200 baud.

Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent Error Difference Between Desired and Actual
50	2304	900	—
75	1536	600	—
110	1047	417	0.026
134.5	857	359	0.058
150	786	300	—
300	384	180	—
600	192	C0	—
1200	96	60	—
1800	64	40	—
2000	58	3A	0.69
2400	48	30	—
3600	32	20	—
4800	24	18	—
7200	16	10	—
9600	12	C	—
19200	6	6	—

Figure 16. Baud Rates at 1.8432 MHz

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled on the NS16550, (FCR bit 0 = 1, IER bit 0 = 1) RCVR interrupts will occur as follows:

- The receive data available interrupt is issued to the system when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below the trigger level.
- The interrupt identification register receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR = x6), as before, has higher priority than the received data available (IIR = x4) interrupt.
- The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows.

- A FIFO timeout will occur if the following conditions exist:
  - At least one character is in the FIFO
  - The most recent character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
  - The most recent system read of the FIFO was longer than 4 continuous character times ago.

    This causes a maximum character received to interrupt issued delay of 160 milliseconds at 300 BAUD with a 12 bit character.
- Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
- When a timeout interrupt has occurred it is cleared and the timer reset when the system reads one character from the RCVR FIFO.
- When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the system reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = 1 , IER bit 1 = 1), XMIT interrupts will occur as follows.

- The transmitter holding register interrupt (THRE) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

- The transmitter FIFO empty indications are delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE = 1. The first transmitter interrupt after changing FCR bit 0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

With FCR bit 0 = 1 resetting IER bits 0 through 3 puts the NS16550 in the FIFO polled mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program checks RCVR and XMITTER status via the line status register. As stated previously:

- Line status register bit 0 is set as long as there is one byte in the RCVR FIFO.
- Line status register bits 1 through 4 specify which errors have occurred. Character error status is handled the same way as when in the interrupt mode. The interrupt identification register is not affected since interrupt enable register bit 2 = 0.
- Line status register bit 5 indicates when the XMIT FIFO is empty.
- Line status register bit 6 indicates that both the XMIT FIFO and shift register are empty.
- Line status register bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO polled mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Connector Specifications

The adapter has a 10-pin connector at the rear of the adapter. The following figure shows the signals and their pin assignments.

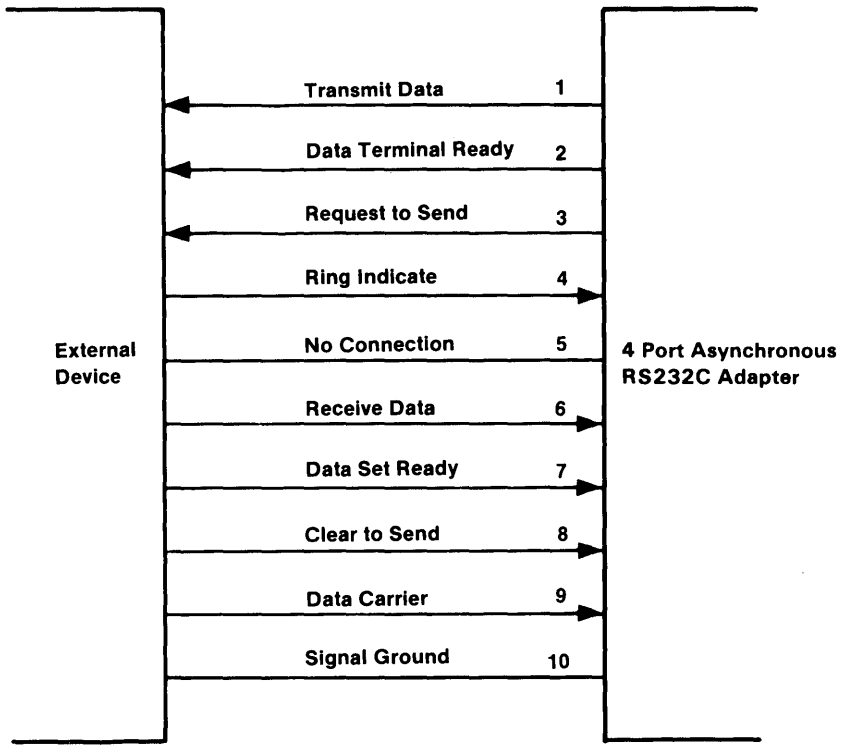


Figure 17. Connnector Specifications

Note: See Figure 9 on page for connector pin functions.

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4-Port Asynchronous Adapter RS422A

Contents

Description

The 4 Port Asynchronous RS422 Adapter provides four serial output ports on a 4.25- by 13.12-inch board that plugs into one I/O position. The adapter system control signals and voltage requirements are provided through a 2- by 31-position and a 2- by 18-position tab on the bottom of the adapter.

Up to four adapters may be used in one RT PC system. A DIP switch on the adapter is used to assign the adapter's I/O address range. The port I/O address assignments are contained in the adapter's I/O address range.

The adapter is fully programmable and supports asynchronous terminal attachment only. It adds and removes start bits, stop bits, and parity bits. A programmable baud-rate generator allows operation from 50 bps to 19200 bps. Five-, 6-, 7- or 8-bit characters with 1, 1-1/2, or 2 stop bits are supported. A priority interrupt system controls transmit, receive, error, line status, and data set interrupts.

Four 6-pin AMPMODU connectors on the adapter provide external access to the four ports.

The heart of the adapter is an NS16450 LSI chip or a functional equivalent. Features in addition to those listed above include:

- Full double buffering that eliminates the need for precise synchronization
- Independent receiver clock bit
- False start bit detection
- Line-break generation and detection.

All communications protocol is a function of the system microcode that must be loaded before the adapter is operational. All pacing of the interface and control signal status must be handled by the system software. Figure 1 on page 2 is a block diagram of the 4 Port Asynchronous RS422 Adapter.

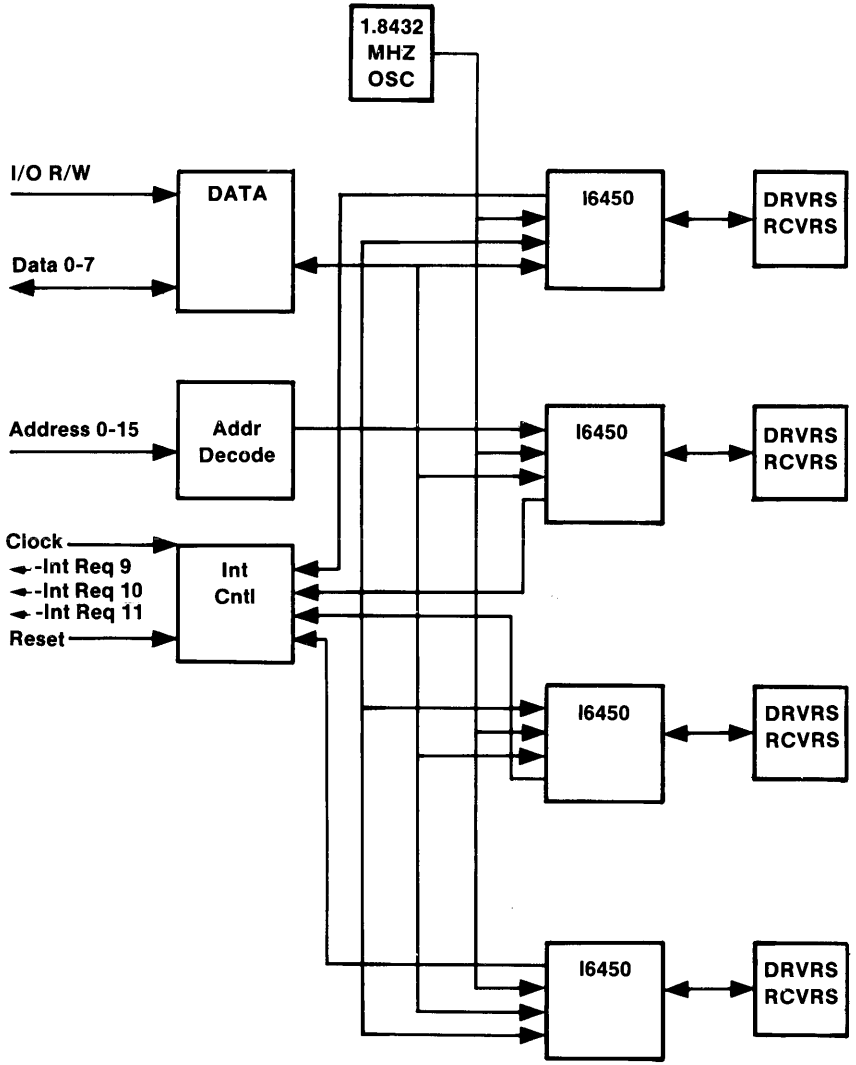


Figure 1. 4 Port Asynchronous RS422 Adapter Block Diagram

4 Port Asynchronous RS422 Adapter Switch Settings

The 4 Port Asynchronous RS422 Adapter switch settings select the interrupt level and the address range of adapters installed.

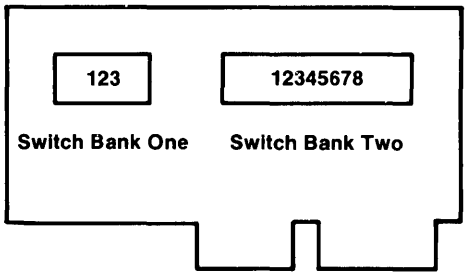


Figure 2. 4 Port Asynchronous RS422 Adapter Switches

Interrupt Level Selected	Switch Bank One Setting		
	Switch 1	**Switch 2**	**Switch 3**
Level 9	On	Off	Off
Level 10	Off	On	Off
Level 11	Off	Off	On

Figure 3. Switch Bank One Settings

Address Range of Adapters	Switch Bank Two Setting			
	Switch 1	**Switch 2**	**Switch 3**	**Switch 4**
1230-124F	On	Off	Off	Off
2230-224F	Off	On	Off	Off
3230-324F	Off	Off	On	Off
4230-424F	Off	Off	Off	On

Figure 4. Switch Bank Two Settings

Note: Switches 5 through 8 are not used.

Modes of Operation

The different modes of operation are selected by programming the NS16450 asynchronous communications element. This is done by selecting the I/O address and writing data out to the I/O address. Address bits A0, A1, and A2 select the different registers that define the modes of operation. Also, the divisor latch access bit (bit 7) of the line control register is used to select certain registers.

The address range for this adapter is Hex 1230 through Hex 424F. Figure 5 and Figure 6 on page 5 depict a value of n which represents a variable determined by the setting of switch bank two. Switches 1, 2, 3, and 4 of switch bank two allow the adapter to operate and select the appropriate address range.

I/O Decode (In Hex) Port B	Port A	Register Selected	DLAB State
n238	n230	TX Buffer	DLAB=0 (Write)
n238	n230	RX Buffer	DLAB=0 (Read)
n238	n230	Divisor Latch LSB	DLAB=1
n239	n231	Divisor Latch MSB	DLAB=1
n239	n231	Interrupt Enable Register	DLAB=0
n23A	n232	Interrupt Identification Register	
n23B	n233	Line Control Register	
n23C	n234	Modem Control Register	
n23D	n235	Line Status Register	
n23E	n236	Modem Status Register	

Figure 5. I/O Decodes, Port A and Port B

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

I/O Decode (In Hex) Port D	Port C	Register Selected	DLAB State
n248	n240	TX Buffer	DLAB=0 (Write)
n248	n240	RX Buffer	DLAB=0 (Read)
n248	n240	Divisor Latch LSB	DLAB=1
n249	n241	Divisor Latch MSB	DLAB=1
n249	n241	Interrupt Enable Register	DLAB=0
n24A	n242	Interrupt Identification Register	
n24B	n243	Line Control Register	
n24C	n244	Modem Control Register	
n24D	n245	Line Status Register	
n24E	n246	Modem Status Register	

Figure 6. I/O Decodes, Port C and Port D

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

A9—>A3 Decode	A2	A1	A0	DLAB	Register
See	x	x	x		
Note 1	0	0	0	0	Receive Buffer Reg. (read) Transmit Holding Reg. (write)
	0	0	1	0	Interrupt Enable
	0	1	0	x	Interrupt Identification
	0	1	1	x	Line Control
	1	0	0	x	Modem Control
	1	0	1	x	Line Status
	1	1	0	x	Modem Status
	1	1	1	x	Scratch (See note 3)
	0	0	0	1	Divisor Latch (LSB)
	0	0	1	1	Divisor Latch (MSB)

Figure 7. Address Bits

Notes:

1. Bits A9 through A3 are used to select specific adapter and serial port.
2. A2, A1, and A0 bits are "don't cares" and are used to select the different registers of the NS16450 chip.
3. The Scratch Register of the NS16450 module should be initialized to all ones and never be written to with any data afterwards. This would cause indeterminate data when Read address X237 (see "Interrupts") is executed.

Interrupts

Three interrupt lines are provided to the system. The interrupt level (9, 10, or 11) is selected by placing the appropriate switch on switch bank one to the on position. An interrupt register (read adr n237, where n is first digit of the address range) is provided for storage of pending port interrupts. Interrupt register bit assignments are shown in Figure 8.

Hex Address n237							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	Port 4	Port 3	Port 2	Port 1

Figure 8. Interrupt Register Read Format

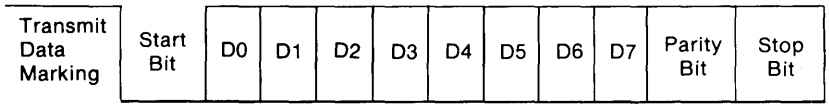
The reset or enable for interrupt level 9 is hex address 02F2.

The reset or enable for interrupt level 10 is hex address 06F2.

The reset or enable for interrupt level 11 is hex address 06F3.

Serial Data Format

The data format is as follows:



Data bit 0 is the first bit to be transmitted or received. The adapter automatically inserts the start bit, the correct parity bit (if programmed to do so), and the stop bit (1, 1-1/2, or 2 depending on the command in the line control register).

External Interface Description

The adapter provides an EIA 4 Port Asynchronous RS422 Adapter interface.

The pin functions for the 6-pin connector are shown in Figure 9 on page 8.

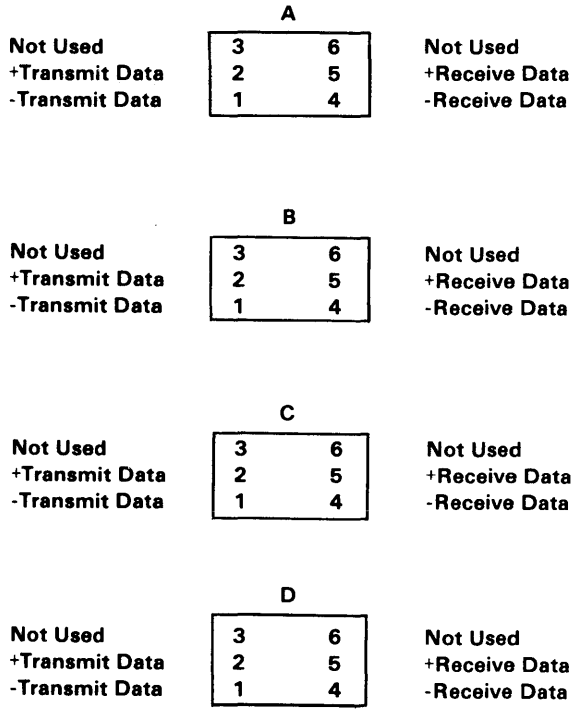


Figure 9. 6 Pin Interface Signals Connector (as viewed from rear of adapter)

The adapter converts the interface signals from TTL levels to EIA 4 Port Asynchronous RS422 Adapter voltage levels, and vice versa. These signals are sampled or generated by the communications control chip. These signals can then be sensed by the system software to determine the state of the interface or peripheral device. The drivers and receivers used on the adapter are the inverting type; therefore, a 0 EIA level on the line is received or transmitted as a 0 TTL level, and a 1 EIA level is received or transmitted as a 1 TTL level.

Voltage Interchange Information

The electrical characteristics for voltage interchange information are designed to meet the requirements of EIA RS422A standard.

For interface control circuits, the input to the receiver, measured differentially, shall be greater than +200 millivolts for a binary 0 and greater than -200 millivolts for a binary 1. (See Figure 10).

Interchange Differential Voltage (A-B)	Binary State	Signal Condition	Interface Control Function
Positive Voltage	Binary 0	Spacing	=On
Negative Voltage	Binary 1	Marking	=Off

Figure 10. 4 Port Asynchronous RS422 Adapter Signal Levels

Asynchronous Communications Element Pin Description

The following describes the function of all NS16450 input/output pins. Some of these descriptions reference internal circuits. The use of each signal as implemented on the multiport adapter is described.

Note: In the following descriptions, a low represents a logical 0 (0 Vdc nominal) and a high represents a logical 1 (+2.4 Vdc nominal).

Input Signals

Chip Select (CS0, CS1, -CS2), Pins 12-14: When CS0 and CS1 are high and -CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) address strobe (-ADS) input. This enables communications between the NS16450 and the processor.

Data Input Strobe (DISTR, -DISTR), Pins 22 and 21: When DISTR is high or -DISTR is low while the chip is selected, this signal allows the processor to read status information or data from a selected register of the NS16450.

Note: Only an active DISTR or -DISTR input is required to transfer data from the NS16450 during a read operation. Therefore, tie either the DISTR input permanently low or the -DISTR line input permanently high, if not used.

Data Output Strobe (DOSTR, -DOSTR), Pins 19 and 18: When DOSTR is high or -DOSTR is low while the chip is selected, this signal allows the processor to write data or control words into a selected register of the NS16450.

Note: Only an active DOSTR or -DOSTR input is required to transfer data to the NS16450 during a write operation. Therefore, tie either the DOSTR input permanently low or the -DOSTR input permanently high, if not used.

-Address Strobe (-ADS), Pin 25: When low, this signal provides latching for the register select (A0, A1, A2) and chip select (CS0, CS1, -CS2) signals.

Note: An active -ADS input is required when the register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the -ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an NS16450 register to read from or write into as indicated in the table below. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain NS16450 registers. The DLAB must be set high by the system software to access the baud-generator divisor latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (Read)
				Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable
x	0	1	0	Interrupt Identification (Read Only)
x	0	1	1	Line Control
x	1	0	0	Modem Control
x	1	0	1	Line Status
x	1	1	0	Modem Status
x	1	1	1	Scratch
1	0	0	0	Divisor Latch (Least Significant Byte)
1	0	0	0	Divisor Latch (Most Significant Byte)

Figure 11. NS16450 Register Selection

Master Reset (MR), Pin 35: When high, this signal clears all the registers (except the receive buffer, transmitter holding, and divisor latches), and the control logical of the NS16450. Also, the state of various output signals (SOUT, INTRPT, -OUT 1, -OUT 2, -RTS, -DTR) is affected by an active MR input. Refer to:

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low, 0-3 Forced and 4-7 Permanent
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 are Low, and Bits 3-7 are Permanent
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
Modem Status Register	Master Reset	Bits 0-3 are Low, Bits 4-7 = Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errors)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IRR/Write /THR/MR	Low
INTRPT (Modem Status Changes) • OUT 2 • RTS • DTR • OUT 1	Read MSR/MR Master Reset Master Reset Master Reset Master Reset	Low High High High High

Figure 12. NS16450 Reset Functions

Receiver Clock (RCLK), Pin 9: This input is the 16x baud-rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, modem, or data set).

-Clear to Send (-CTS), Pin 36: The -CTS signal is a modem control function input whose condition the processor can test by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates whether the -CTS input has changed state since the previous reading of the modem status register.

Note: The CTS bit of the modem status register is tied to the active state.

-Data Set Ready (-DSR), Pin 37: The -DSR signal is a modem control function input whose condition the processor can test by reading bit 5 (DSR) of the modem status register. When low, this signal indicates that the modem or data set is ready to establish the communications link and transfer data with the NS16450. Bit 1 (DDSR) of the modem status register indicates whether the -DSR input has changed since the previous reading of the modem status register.

Note: The DSR bit of the modem status register is tied to the active state.

-Received Line Signal Detect (-RLSD), Pin 38: The -RLSD signal is a modem control function input whose condition the processor can test by reading bit 7 (RLSD) of the modem status register. When low, this signal indicates that the data carrier has been detected by the modem or data set. Bit 3 (DRLSD) of the modem status register indicates whether the -RLSD not input has changed state since the previous reading of the modem status register.

Notes:

1. The RLSD bit of the modem status register is tied to the active state.
2. Received Line Signal Detect is also called Data Carrier Detect (DCD), or Carrier Detect (CD).

-Ring Indicator (-RI), Pin 39: The -RI signal is a modem control function input whose condition the processor can test by reading bit 6 (RI) of the modem status register. When low, this signal indicates that a telephone ringing signal has been received by the modem or data set. Bit 2 (TERI) of the modem status register indicates whether the -RI input has changed from a low to high state since the previous reading of the modem status register.

Note: The RI bit of the modem status register is tied to the inactive state.

VCC, Pin 40: +5 Vdc supply.

VSS, Pin 20: Ground (0 Vdc) reference.

Output Signals

-Data Terminal Ready (-DTR), Pin 33: When low, this signal informs the modem or data set that the NS16450 is ready to communicate. The -DTR output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. The -DTR signal is set high upon a master reset operation. The -DTR signal is forced to high during loop mode operation. See note below.

-Request To Send (-RTS), Pin 32: When low, this signal informs the modem or data set that the NS16450 is ready to transmit data. The -RTS output signal can be set to an active low by programming bit 1 (RTS) of the modem control register. The -RTS signal is set high by a master reset operation. The -RTS signal is forced to high during loop mode operation. See note below.

-Output 1 (-OUT 1), Pin 34: With this signal, user-designated output can be set to an active low by programming bit 2 (-OUT 1) of the modem control register to a high level. The -OUT 1 signal is set high by a master reset operation. The -OUT 1 signal is forced to high during loop mode operation. See note below.

-Output 2 (-OUT 2), Pin 31: With this signal, user-designated output can be set to an active low by programming bit 3 (-OUT 2) of the modem control register to a high level. The -OUT 2 signal is set high by a master reset operation. The -OUT 2 signal is forced to high during the loop mode operation. See note below.

Chip Select Out (CSOUT), Pin 24: When high, this signal indicates that the chip has been selected by active CS0, CS1, and -CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logical 1. See note below.

Driver Disable (DDIS), Pin 23: This signal goes low whenever the processor is reading data from the NS16450. A high-level DDIS output can be used to disable an external transceiver (if used between the processor and NS16450 on the D7-D0 data bus) at all times, except when the processor is reading data. See note below.

-Baudout (-BAUDOUT), Pin 15: This is a 16x clock signal for the transmitter section of the NS16450. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud-generator division latches. The -BAUDOUT is tied to the receiver section of the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: This signal goes high whenever any one of the following interrupt types has an active high condition and is enabled through the IIR: receiver error flag, received data available, transmitter holding register empty, or modem status. The INTRPT signal is reset low by the appropriate interrupt service or a master reset operation.

Serial Output (SOUT), Pin 11: This signal is a composite serial data output to the communications link (peripheral, modem or data set). The SOUT signal is set to the marking (logical 1) state upon a master reset operation.

Note: This pin is not used on the 4 Port Asynchronous RS422 Adapter board.

Input/Output Signals

Data Bus (D7-D0), Pins 1-8: This bus contains eight tri-state input/output lines. The bus provides bidirectional communications between the NS16450 and the processor. Data, control words, and status information are transferred through the D7-D0 data bus.

External Clock Input/Output (XTAL1, XTAL2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the NS16450.

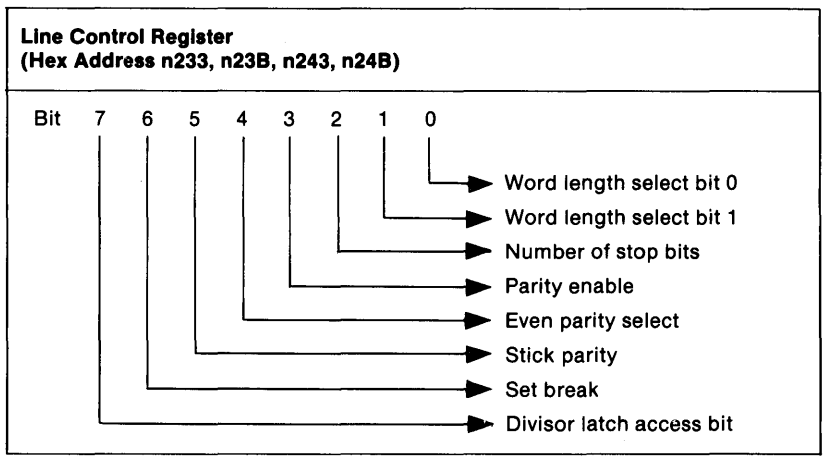
Programming Considerations

The NS16450 has a number of accessible registers. The system programmer may access or control any of the NS16450 registers through the processor. These registers are used to control NS16450 operations and to transmit and receive data.

Note: The n in address is the first digit of the adapter address range (1-4).

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange through the line control register. In addition to controlling the format, the programmer may retrieve the contents of the line control register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the line control register are described below:



Bits 0, 1 These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2 This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logical 0, one stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logical 1 when a 5-bit word length is selected through bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is a logical 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated or checked.

Bit 3 This bit is the parity enable bit. When bit 3 is a logical 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed.)

Bit 4 This bit is the even parity select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logical 1 and bit 4 is a logical 1, an even number of bits are transmitted or checked.

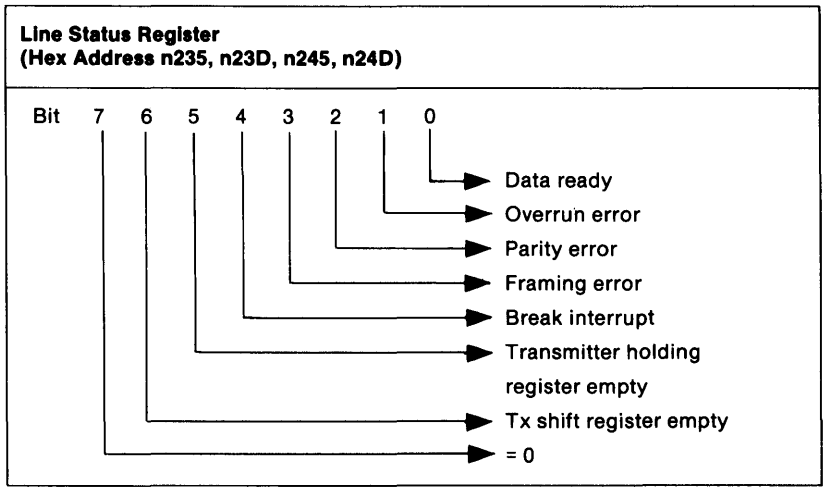
Bit 5 This bit is the stick parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is transmitted and then detected by the receiver as a logical 0 (space parity) if bit 4 is a logical 1, or as a logical 1 (mark parity) if bit 4 is a logical 0.

Bit 6 This bit is the set break control bit. When bit 6 is a logical 1, the serial output (SOUT) forces a spacing (logical 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logical 0. This feature enables the processor to alert a terminal in a computer communications system.

Bit 7 This bit is the divisor latch access bit (DLAB). It must be set high (logical 1) to access the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Line Status Register

This 8-bit register provides status information to the processor concerning the data transfer. The contents of the line status register are described below:



Bit 0 This bit is the receiver data ready (DR) indicator. Bit 0 is set to a logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to a logical 0 either by the processor reading the data in the receiver buffer or by writing a logical 0 into it from the processor.

Bit 1 This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the processor before the next character was transferred into the receiver buffer register, and that the previous character was thereby destroyed. The OE indicator is reset whenever the processor reads the contents of the line status register.

Bit 2 This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity as selected by the even parity-select bit. The PE bit is set to a logical 1 upon detection of a parity error and is reset to a logical 0 whenever the processor reads the contents of the line status register.

Bit 3 This bit is the framing error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logical 1 whenever the stop bit following the last data bit or parity is detected as a zero bit (spacing level).

Bit 4 This bit is the break interrupt (BI) indicator. Bit 4 is set to a logical 1 whenever the received data input is held in the spacing (logical 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits).

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected.

Bit 5 This bit is the transmitter holding register empty (THRE) indicator. Bit 5 indicates that the NS16450 is ready to accept a new character for transmission. In addition, this bit causes the NS16450 to issue an interrupt to the processor when the transmit holding register empty interrupt enable is set high. The THRE bit is set to a logical 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logical 0 concurrently with the loading of the transmitter holding register by the processor.

Bit 6 This bit is the transmitter empty (TEMT) indicator. Bit 6 is set to a logical 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logical 0 whenever either the THR or TSR contain a data character. Bit 6 is a read-only bit.

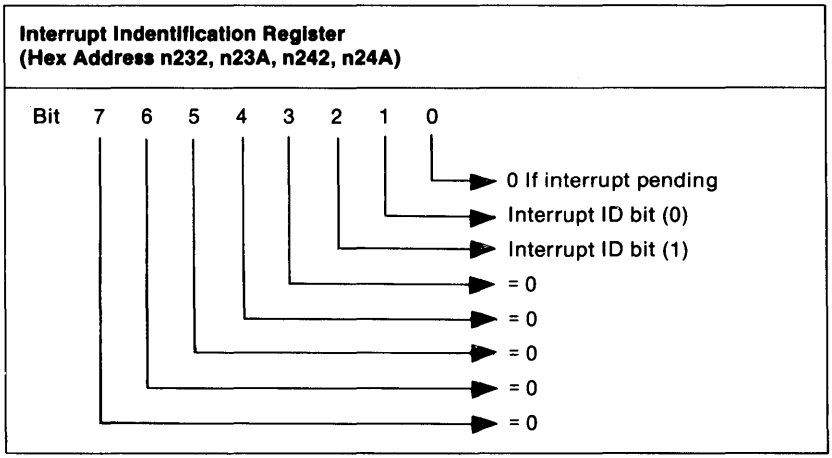
Bit 7 This bit is permanently set to logical 0.

Interrupt Identification Register

The NS16450 has an on-chip interrupt capability that allows for complete flexibility in interfacing to microprocessors. In order to provide minimum software overhead during data character transfers, the NS16450 sets interrupts into four priority levels:

- Receiver line status (priority 1)
- Received data ready (priority 2),
- Transmitter holding register empty (priority 3)
- Modem status (priority 4).

Information indicating that a priority interrupt is pending and information on the type of interrupt is stored in the interrupt identification register. Refer to the "Interrupt Control Functions" table in Figure 13 on page 19. The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending, and no other interrupts are acknowledged until that particular interrupt is serviced by the processor. The contents of the IIR are described below.



Bit 0 This bit can be used in a hardwired, priority, or polled environment to indicate whether an interrupt is pending. When bit 0 is a logical 0, an interrupt is pending and the IIR contents are used as a pointer to the appropriate interrupt service routine. When bit 0 is a logical 1, no interrupt is pending, and polling (if used) is continued.

Bits 1, 2 These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Figure 13 on page 19.

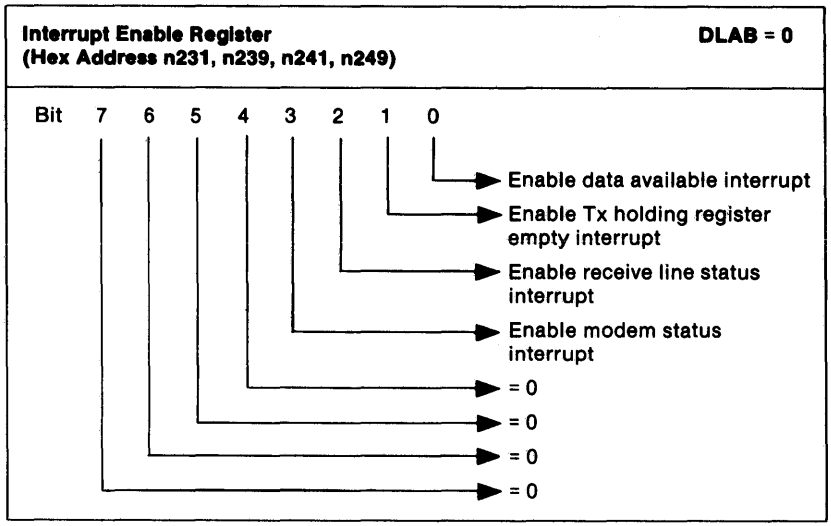
Bits 3-7 These five bits of the IIR are always logical 0.

Interrupt ID Register			Interrupt Set and Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Intrpt.	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register or Writing into the Transmitter Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Figure 13. Interrupt Control Functions

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the NS16450 to separately activate the chip interrupt (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the interrupt enable register. Similarly, setting the appropriate bits of this register to a logical 1, can enable selected interrupts. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are described below:



Bit 0 This bit enables the received data available interrupt when set to a logical 1.

Bit 1 This bit enables the transmitter holding register empty interrupt when set to a logical 1.

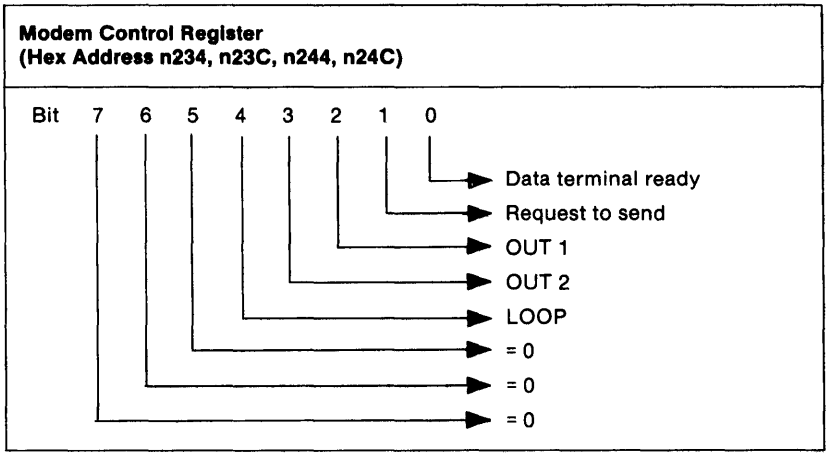
Bit 2 This bit enables the receiver line status interrupt when set to a logical 1.

Bit 3 This bit enables the modem status interrupt when set to a logical 1.

Bits 4-7 These four bits are always logical 0.

Modem Control Register

Bit four of this 8-bit register is used for diagnostic testing of the NS16450. All other bits are not used on the 4 Port Asynchronous RS422 Adapter. The contents of the modem control register are described below:



Bit 0 This bit controls the data terminal ready (-DTR) output. When bit 0 is set to a logical 1, the -DTR output is forced to a logical 0. When bit 0 is reset to a logical 0, the -DTR output is forced to a logical 1.

Bit 1 This bit controls the request to send (-RTS) output. Bit 1 affects the -RTS output in a manner identical to that described above for bit 0.

Bit 2 This bit controls the output 1 (-OUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the -OUT 1 output in a manner identical to that described above for bit 0.

Bit 3 This bit controls the output 2 (-OUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the -OUT 2 output in a manner identical to that described above for bit 0.

Note: The -OUT 2 output of the NS16450 may be applied to an EIA inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 4 This bit provides a loopback feature for diagnostic testing of the NS16450. When bit 4 is set to logical 1, the following occurs:

The transmitter serial output (SOUT) is set to the marking (logical 1) state.

The receiver serial input (SIN) is disconnected.

The output of the transmitter shift register is "looped back" into the receiver shift register input.

The four modem control inputs (-CTS, -DSR, -RLSD, and -RI) are disconnected.

The four modem control outputs (-DTR, -RTS, -OUT 1, and -OUT 2) are internally connected to the four modem control inputs.

The modem control output pins are forced high.

In the the diagnostic mode the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the sources of the interrupts are now the lower 4 bits of the modem control register instead of the 4 modem control inputs. The interrupts are still controlled by the interrupt enable register.

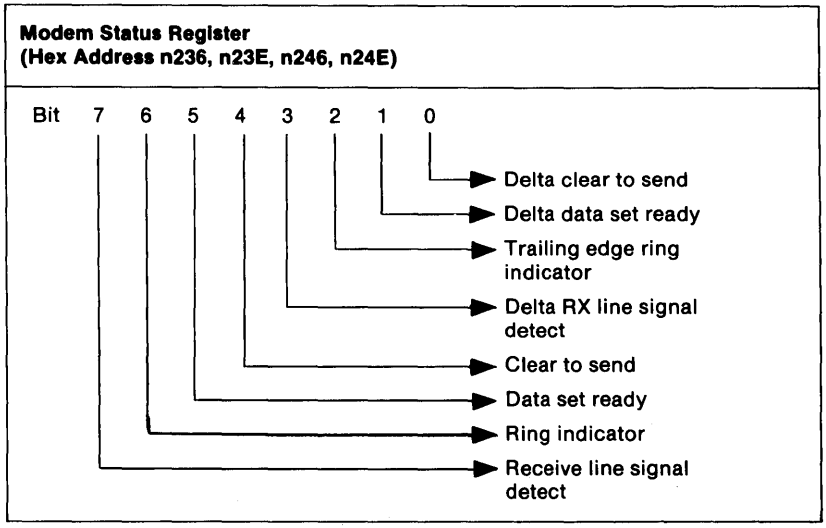
The NS16450 interrupt system can be tested by writing into the lower 6 bits of the line status register and into the lower 4 bits of the modem status register. Setting any of these bits to a logical 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal NS16450 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the modem control register must be reset to logical 0. The transmitter should be idle when this bit changes state.

Bits 5-7 These bits are permanently set to logical 0.

Modem Status Register

This 8-bit register provides the current state of the control lines to the processor.

The contents of the modem status register are described below:



Bit 0 This bit is the delta clear-to-send (DCTS) indicator. Bit 0 indicates that the -CTS input to the chip changed state since the last time it was read by the processor.

Bit 1 This bit is the delta data-set-ready (DDSR) indicator. Bit 1 indicates that the -DSR input to the chip changed state since the last time it was read by the processor.

Bit 2 This bit is the trailing edge of the ring indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from an on (logical 1) to an off (logical 0) condition.

Bit 3 This bit is the delta received line signal detector (DRLSD) indicator. Bit 3 indicates that the -RLSD input to the chip changed state since the last time it was read by the processor.

Note: Whenever bit 0, 1, 2, or 3 is set to a logical 1, a modem status interrupt is generated if the appropriate interrupt enable bit is set in the IER.

Bit 4 This bit is the complement of the clear to send (-CTS) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to RTS in the MCR.

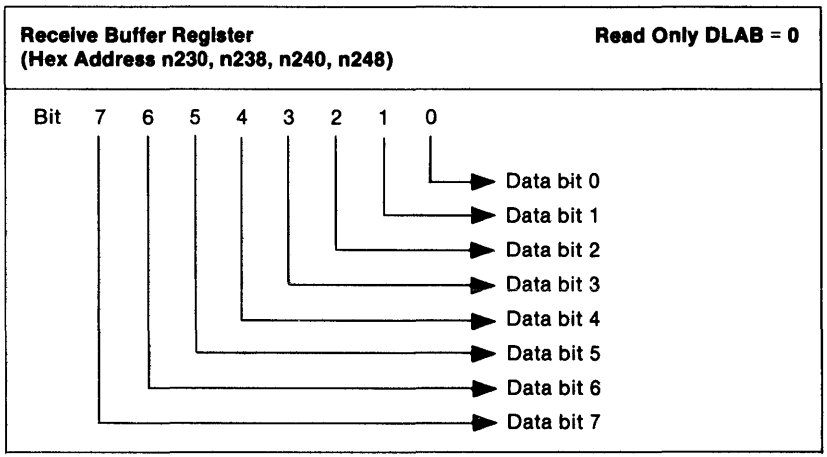
Bit 5 This bit is the complement of the data set ready (-DSR) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to DTR in the MCR.

Bit 6 This bit is the complement of the ring indicator (-RI) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to -OUT 1 in the MCR.

Bit 7 This bit is the complement of the received line signal detect (-RLSD) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to -OUT 2 of the MCR.

Receiver Buffer Register

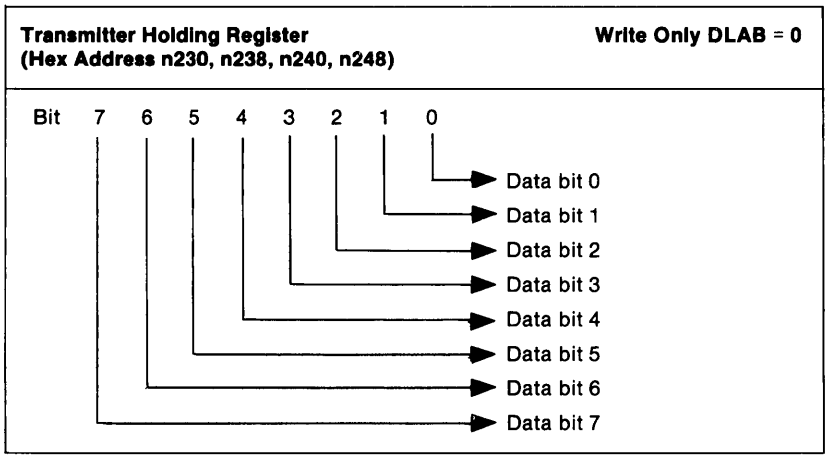
The receiver buffer register contains the received character as defined below:



Bit 0 is the least significant bit and is the first bit serially received.

Transmitter Holding Register

The transmitter holding register contains the character to be serially transmitted and is defined below:



Bit 0 is the least significant bit and is the first bit serially transmitted.

Programmable Baud-Rate Generator

The NS16450 contains a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 655,535 or 2^{16}-1. The output frequency of the baud generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to insure desired operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The contents of the divisor latches are indicated below:

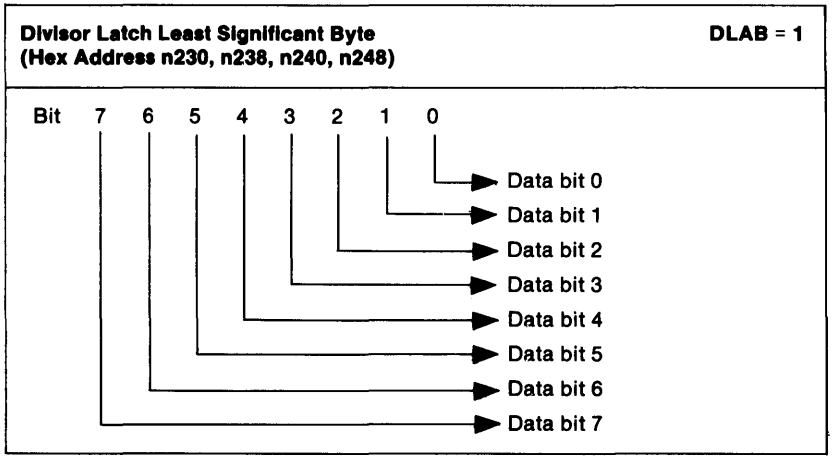


Figure 14. Divisor Latch Least Significant Byte

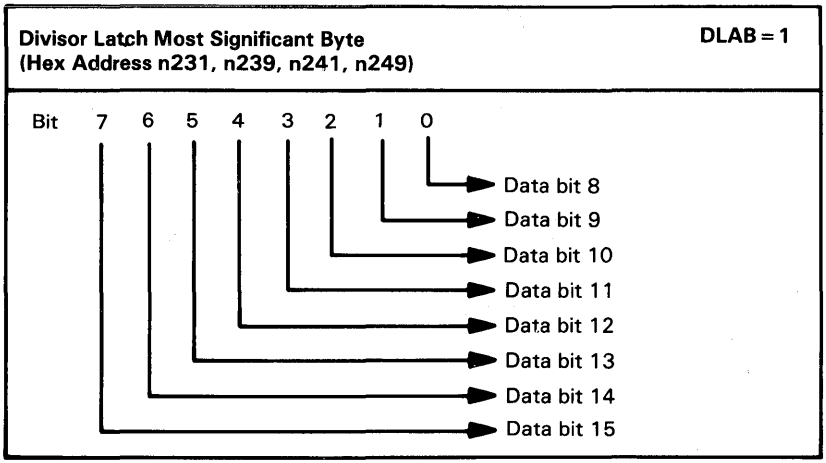


Figure 15. Divisor Latch Most Significant Byte

Figure 16 illustrates the use of the baud-rate generator with a frequency of 1.8432 MHz. For baud rates of 19,200 and below, the error obtained is minimal.

Note: In no case should the data rate be greater than 19,200 baud.

Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent Error Difference Between Desired and Actual
50	2304	900	—
75	1536	600	—
110	1047	417	0.026
134.5	857	359	0.058
150	786	300	—
300	384	180	—
600	192	C0	—
1200	96	60	—
1800	64	40	—
2000	58	3A	0.69
2400	48	30	—
3600	32	20	—
4800	24	18	—
7200	16	10	—
9600	12	C	—
19200	6	6	—

Figure 16. Baud Rates at 1.8432 MHz

Connector Specifications

The adapter has a 6-pin connector at the rear of the adapter. The following figure shows the signals and their pin assignments.

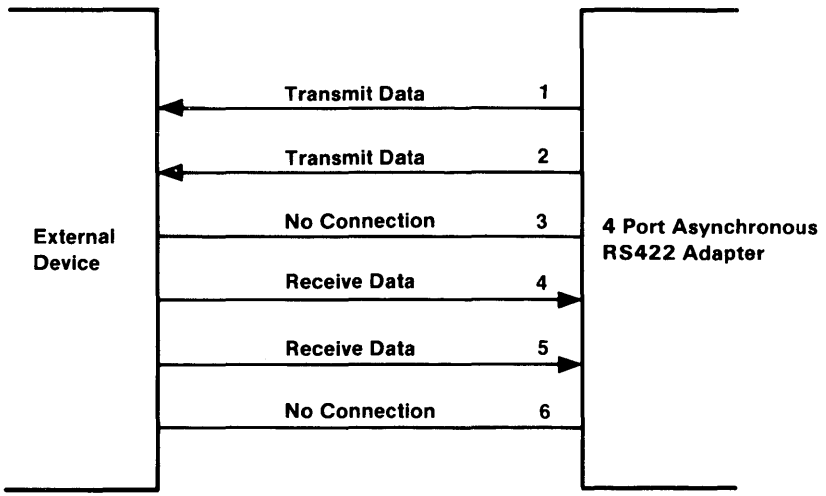
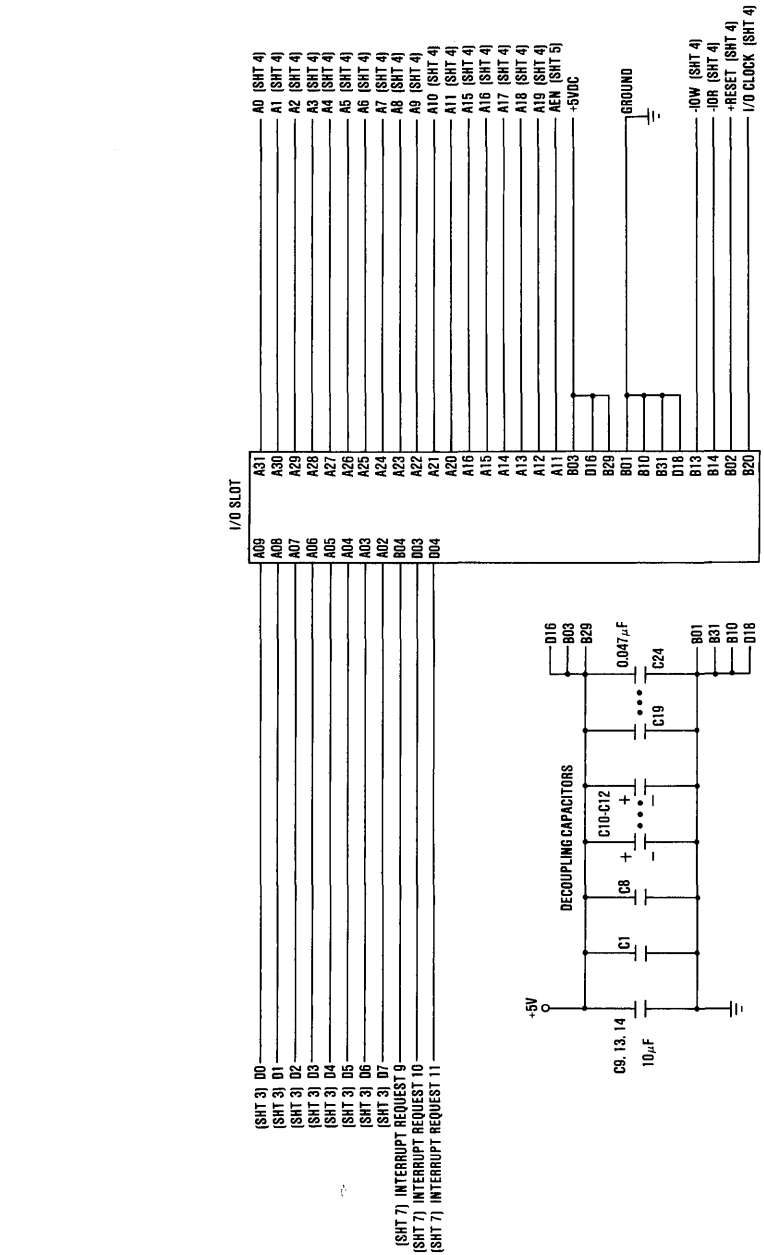
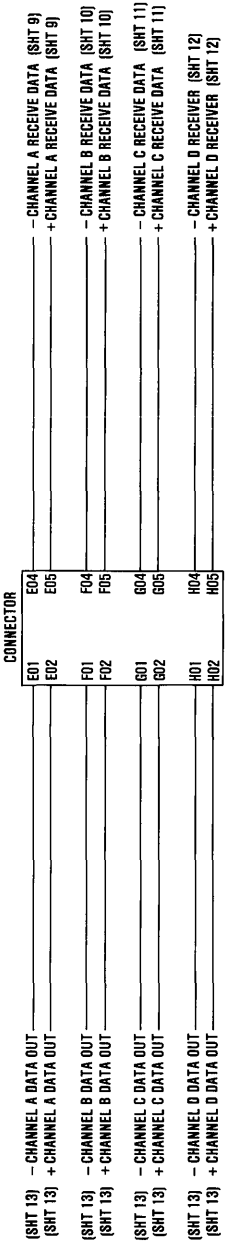


Figure 17. Connector Specifications

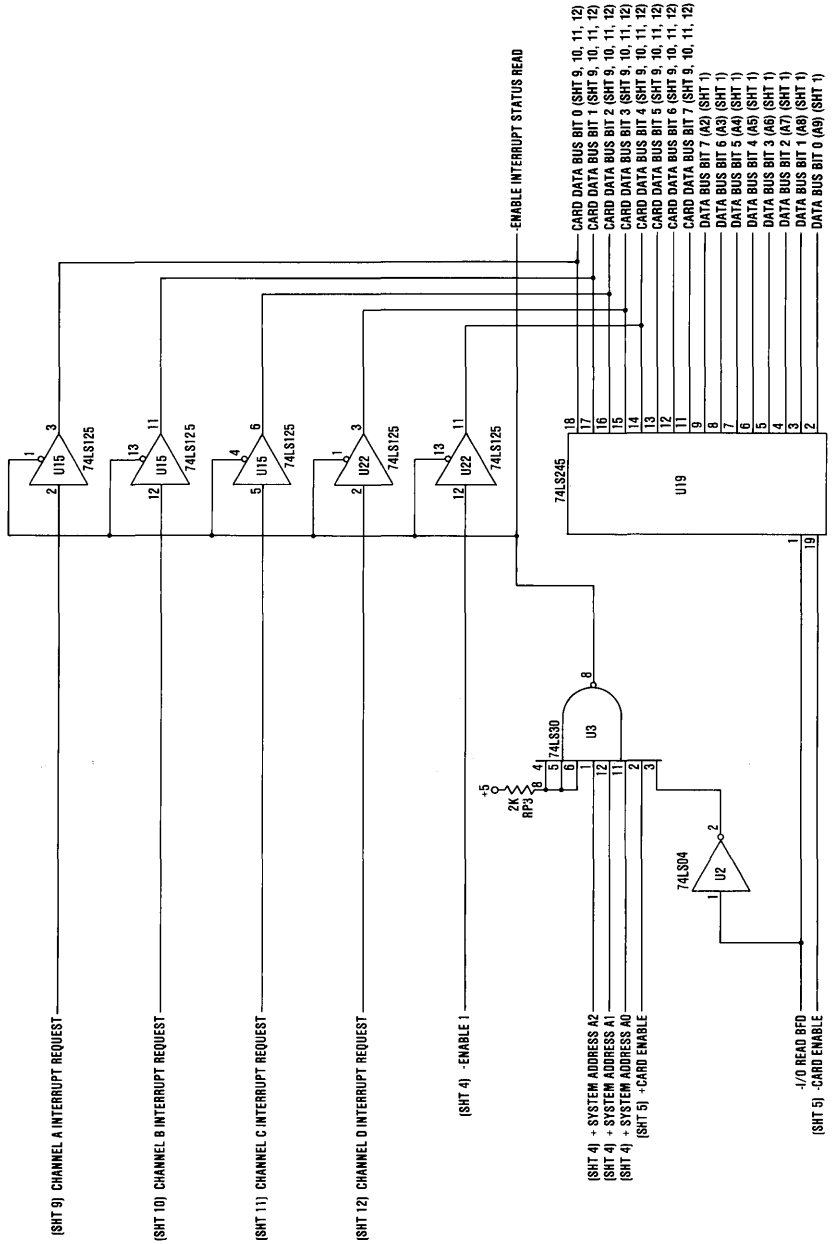
Logic Diagrams

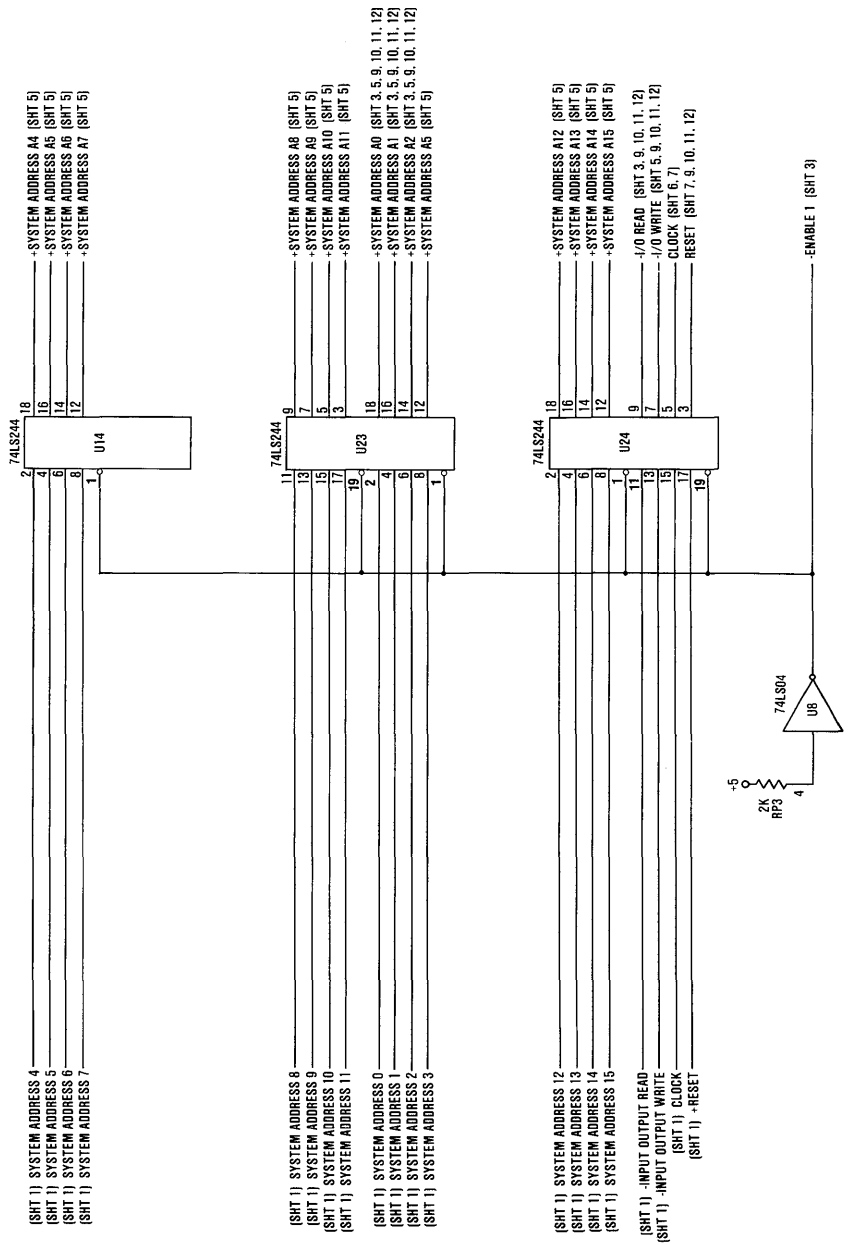
Sheet 1 of 13




EXTERNAL CONNECTOR
E01
E02
F01
F02
G01
G02
H01
H02
E04
E05
F04
F05
G04
G05
H04
H05
(SHT 13) – CHANNEL A DATA OUT
(SHT 13) + CHANNEL A DATA OUT
(SHT 13) – CHANNEL B DATA OUT
(SHT 13) + CHANNEL B DATA OUT
(SHT 13) – CHANNEL C DATA OUT
(SHT 13) + CHANNEL C DATA OUT
(SHT 13) – CHANNEL D DATA OUT
(SHT 13) + CHANNEL D DATA OUT
– CHANNEL A RECEIVE DATA (SHT 9)
+ CHANNEL A RECEIVE DATA (SHT 9)
– CHANNEL B RECEIVE DATA (SHT 10)
+ CHANNEL B RECEIVE DATA (SHT 10)
– CHANNEL C RECEIVE DATA (SHT 11)
+ CHANNEL C RECEIVE DATA (SHT 11)
– CHANNEL D RECEIVER (SHT 12)
+ CHANNEL D RECEIVER (SHT 12)

Sheet 3 of 13


-ENABLE INTERRUPT STATUS READ
CARD DATA BUS BIT 0 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 1 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 2 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 3 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 4 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 5 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 6 (SHT 9, 10, 11, 12)
CARD DATA BUS BIT 7 (SHT 9, 10, 11, 12)
DATA BUS BIT 7 (A2) (SHT 1)
DATA BUS BIT 6 (A3) (SHT 1)
DATA BUS BIT 5 (A4) (SHT 1)
DATA BUS BIT 4 (A5) (SHT 1)
DATA BUS BIT 3 (A6) (SHT 1)
DATA BUS BIT 2 (A7) (SHT 1)
DATA BUS BIT 1 (A8) (SHT 1)
DATA BUS BIT 0 (A9) (SHT 1)
U15
74LS125
U22
74LS125
74LS245
U19
74LS30
U3
74LS04
U2
+5
2K
RP3
[SHT 9) CHANNEL A INTERRUPT REQUEST
[SHT 10) CHANNEL B INTERRUPT REQUEST
[SHT 11) CHANNEL C INTERRUPT REQUEST
[SHT 12) CHANNEL D INTERRUPT REQUEST
[SHT 4) -ENABLE 1
[SHT 4) + SYSTEM ADDRESS A2
[SHT 4) + SYSTEM ADDRESS A1
[SHT 4) + SYSTEM ADDRESS A0
[SHT 5) +CARD ENABLE
-I/O READ BFD
[SHT 5) -CARD ENABLE


74LS244
U14
74LS244
U23
74LS244
U24
74LS04
U8
2K
RP3
+5
(SHT 1) SYSTEM ADDRESS 4
(SHT 1) SYSTEM ADDRESS 5
(SHT 1) SYSTEM ADDRESS 6
(SHT 1) SYSTEM ADDRESS 7
+SYSTEM ADDRESS A4 (SHT 5)
+SYSTEM ADDRESS A5 (SHT 5)
+SYSTEM ADDRESS A6 (SHT 5)
+SYSTEM ADDRESS A7 (SHT 5)
(SHT 1) SYSTEM ADDRESS 8
(SHT 1) SYSTEM ADDRESS 9
(SHT 1) SYSTEM ADDRESS 10
(SHT 1) SYSTEM ADDRESS 11
+SYSTEM ADDRESS A8 (SHT 5)
+SYSTEM ADDRESS A9 (SHT 5)
+SYSTEM ADDRESS A10 (SHT 5)
+SYSTEM ADDRESS A11 (SHT 5)
(SHT 1) SYSTEM ADDRESS 0
(SHT 1) SYSTEM ADDRESS 1
(SHT 1) SYSTEM ADDRESS 2
(SHT 1) SYSTEM ADDRESS 3
+SYSTEM ADDRESS A0 (SHT 3, 5, 9, 10, 11, 12)
+SYSTEM ADDRESS A1 (SHT 3, 5, 9, 10, 11, 12)
+SYSTEM ADDRESS A2 (SHT 3, 5, 9, 10, 11, 12)
+SYSTEM ADDRESS A5 (SHT 5)
(SHT 1) SYSTEM ADDRESS 12
(SHT 1) SYSTEM ADDRESS 13
(SHT 1) SYSTEM ADDRESS 14
(SHT 1) SYSTEM ADDRESS 15
+SYSTEM ADDRESS A12 (SHT 5)
+SYSTEM ADDRESS A13 (SHT 5)
+SYSTEM ADDRESS A14 (SHT 5)
+SYSTEM ADDRESS A15 (SHT 5)
(SHT 1) -INPUT OUTPUT READ
(SHT 1) -INPUT OUTPUT WRITE
(SHT 1) CLOCK
(SHT 1) +RESET
-I/O READ (SHT 3, 9, 10, 11, 12)
-I/O WRITE (SHT 5, 9, 10, 11, 12)
CLOCK (SHT 6, 7)
RESET (SHT 7, 9, 10, 11, 12)
-ENABLE 1 (SHT 3)

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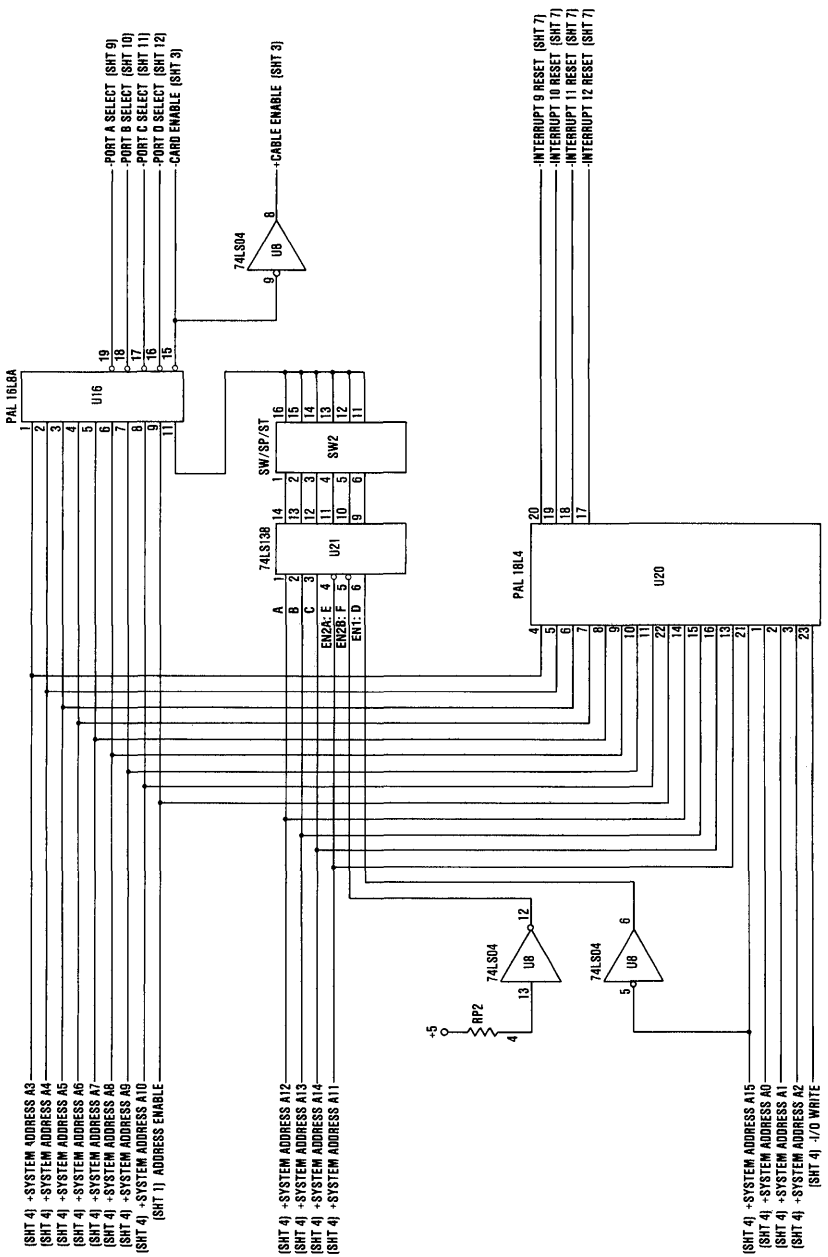
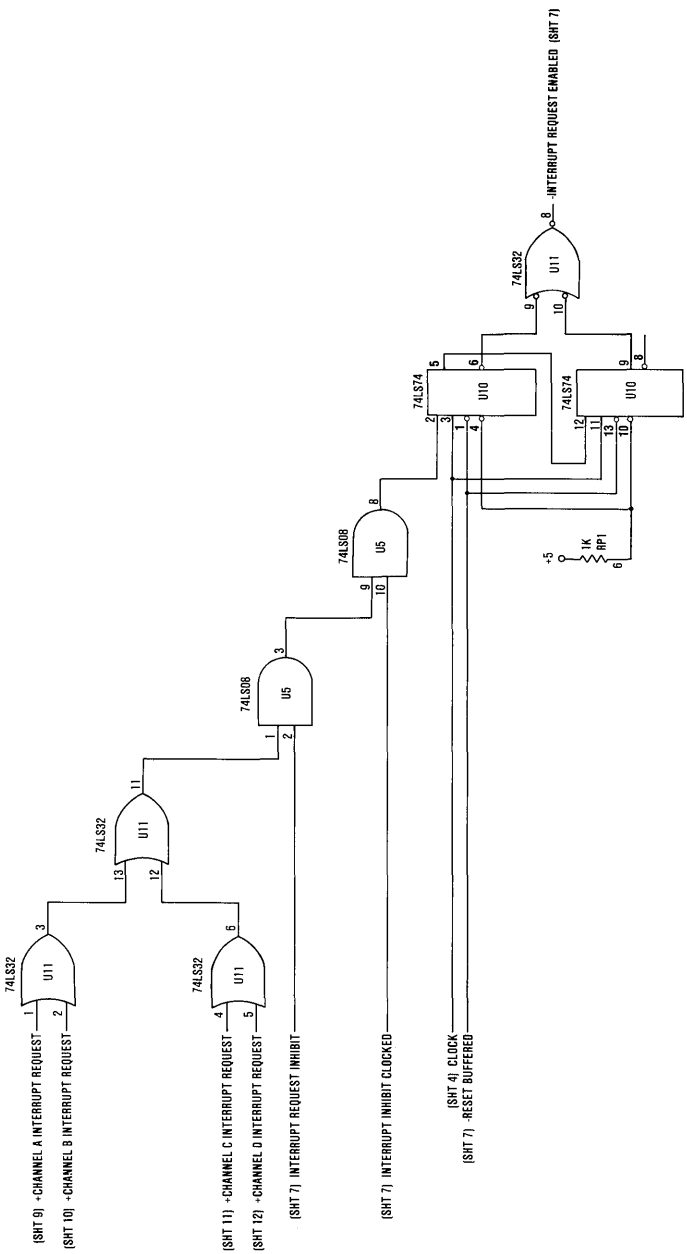
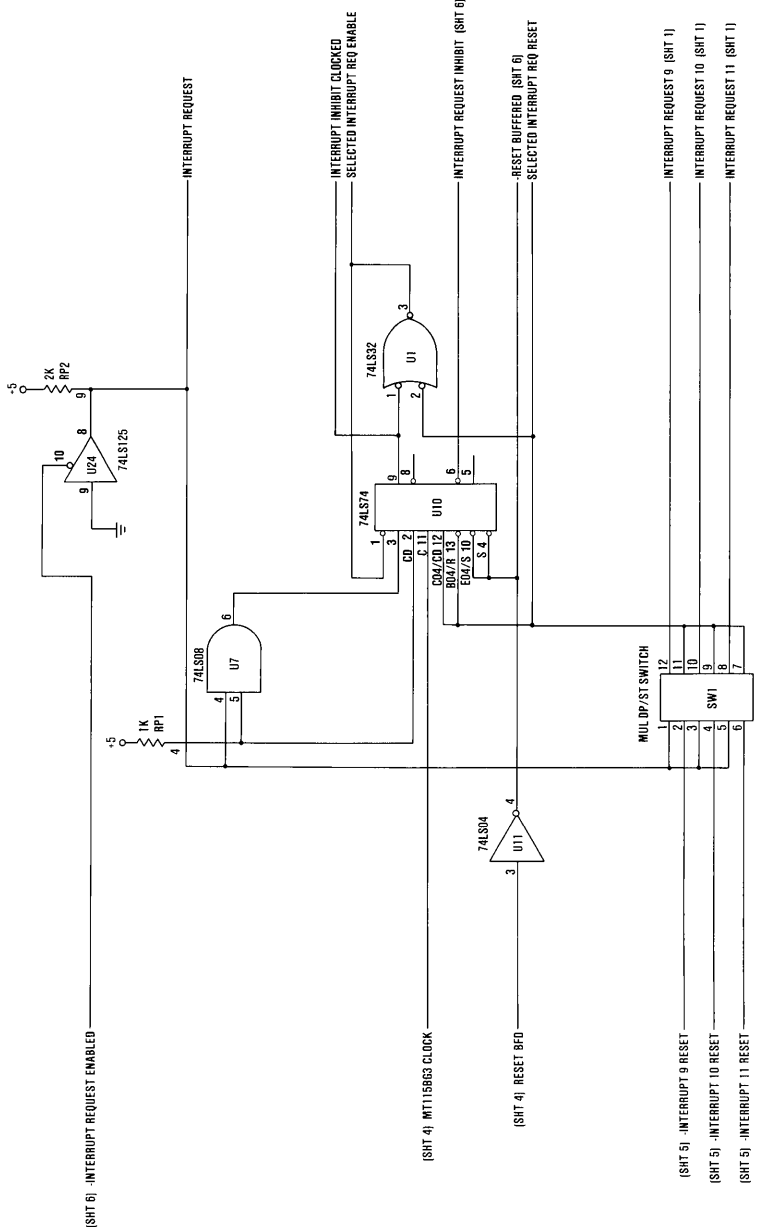

PAL 16L8A
U16
-PORT A SELECT (SHT 9)
-PORT B SELECT (SHT 10)
-PORT C SELECT (SHT 11)
-PORT D SELECT (SHT 12)
-CARD ENABLE (SHT 3)
74LS04
U8
+CABLE ENABLE (SHT 3)
SW/SP/ST
SW2
74LS138
U21
A
B
C
EN2A: E
EN2B: F
EN1: D
PAL 18L4
U20
-INTERRUPT 9 RESET (SHT 7)
-INTERRUPT 10 RESET (SHT 7)
-INTERRUPT 11 RESET (SHT 7)
-INTERRUPT 12 RESET (SHT 7)
+5
RP2
(SHT 4) +SYSTEM ADDRESS A3
(SHT 4) +SYSTEM ADDRESS A4
(SHT 4) +SYSTEM ADDRESS A5
(SHT 4) +SYSTEM ADDRESS A6
(SHT 4) +SYSTEM ADDRESS A7
(SHT 4) +SYSTEM ADDRESS A8
(SHT 4) +SYSTEM ADDRESS A9
(SHT 4) +SYSTEM ADDRESS A10
(SHT 1) ADDRESS ENABLE
(SHT 4) +SYSTEM ADDRESS A12
(SHT 4) +SYSTEM ADDRESS A13
(SHT 4) +SYSTEM ADDRESS A14
(SHT 4) +SYSTEM ADDRESS A11
(SHT 4) +SYSTEM ADDRESS A15
(SHT 4) +SYSTEM ADDRESS A0
(SHT 4) +SYSTEM ADDRESS A1
(SHT 4) +SYSTEM ADDRESS A2
(SHT 4) -I/O WRITE

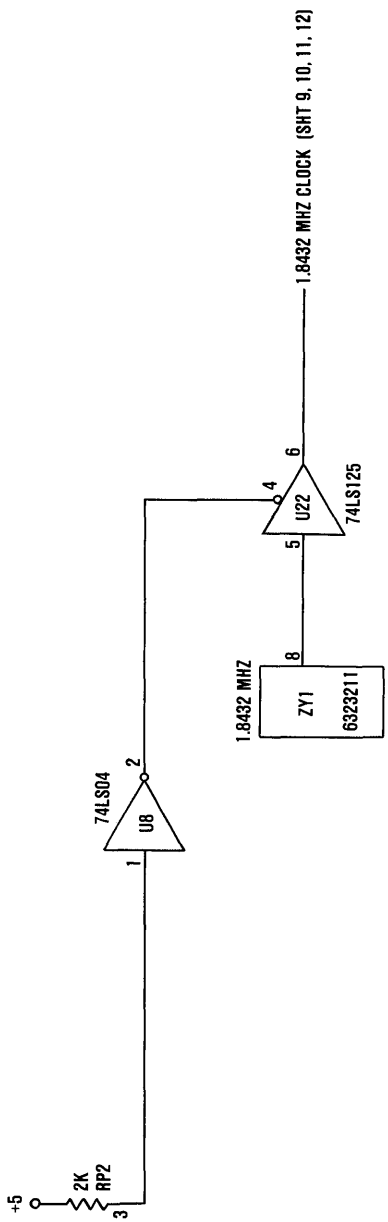
Sheet 6 of 13


(SHT 9) +CHANNEL A INTERRUPT REQUEST
(SHT 10) +CHANNEL B INTERRUPT REQUEST
(SHT 11) +CHANNEL C INTERRUPT REQUEST
(SHT 12) +CHANNEL D INTERRUPT REQUEST
(SHT 7) INTERRUPT REQUEST INHIBIT
(SHT 7) INTERRUPT INHIBIT CLOCKED
(SHT 4) CLOCK
(SHT 7) RESET BUFFERED
+5
1K
RP1
74LS32
74LS08
74LS74
U11
U5
U10
INTERRUPT REQUEST ENABLED (SHT 7)

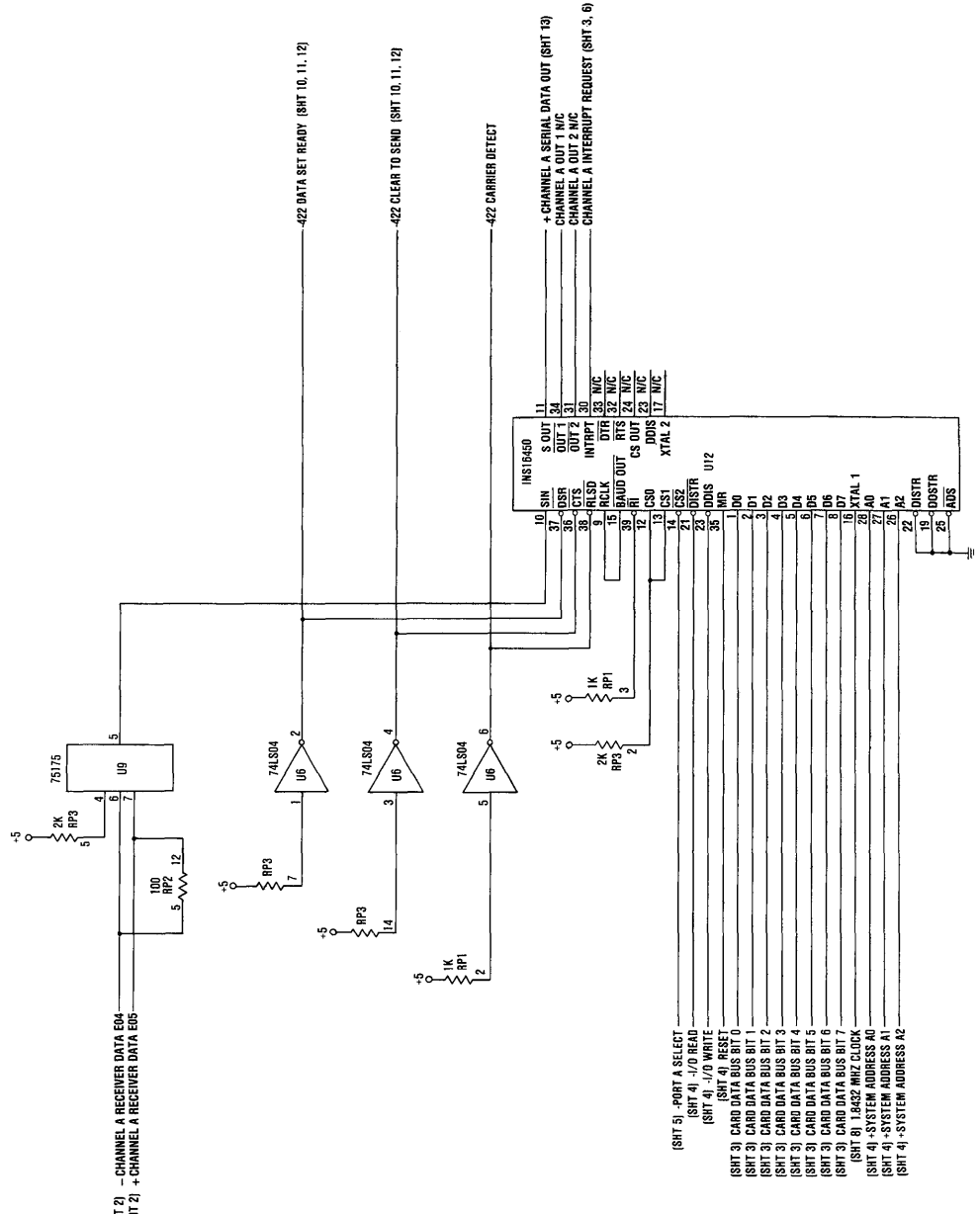
Sheet 7 of 13

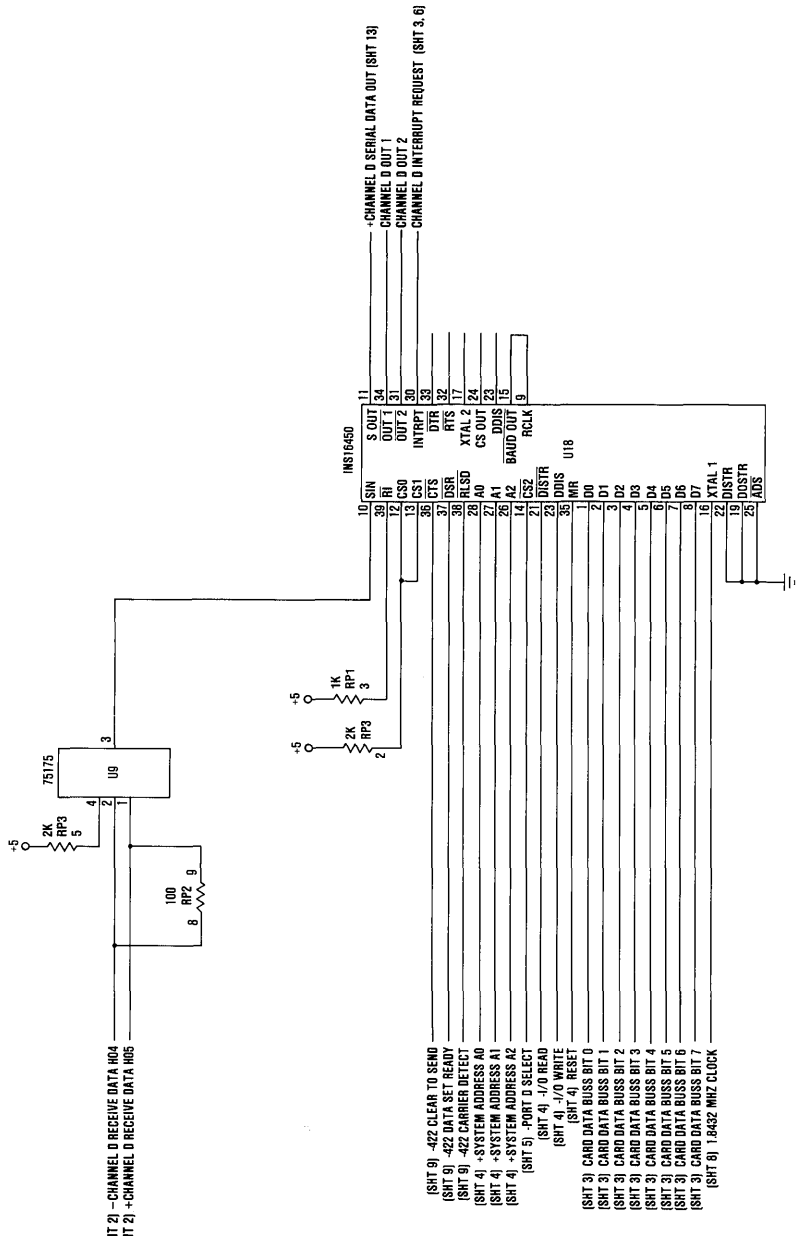

INTERRUPT REQUEST
INTERRUPT INHIBIT CLOCKED
SELECTED INTERRUPT REQ ENABLE
INTERRUPT REQUEST INHIBIT (SHT 6)
RESET BUFFERED (SHT 6)
SELECTED INTERRUPT REQ RESET
INTERRUPT REQUEST 9 (SHT 1)
INTERRUPT REQUEST 10 (SHT 1)
INTERRUPT REQUEST 11 (SHT 1)
-5
2K
RP2
74LS125
U24
74LS32
U1
74LS74
U10
74LS08
U7
1K
RP1
74LS04
U11
MUL DP/ST SWITCH
SW1
(SHT 6) -INTERRUPT REQUEST ENABLED
(SHT 4) MT1159B3 CLOCK
(SHT 4) RESET BFD
(SHT 5) -INTERRUPT 9 RESET
(SHT 5) -INTERRUPT 10 RESET
(SHT 5) -INTERRUPT 11 RESET

Sheet 8 of 13

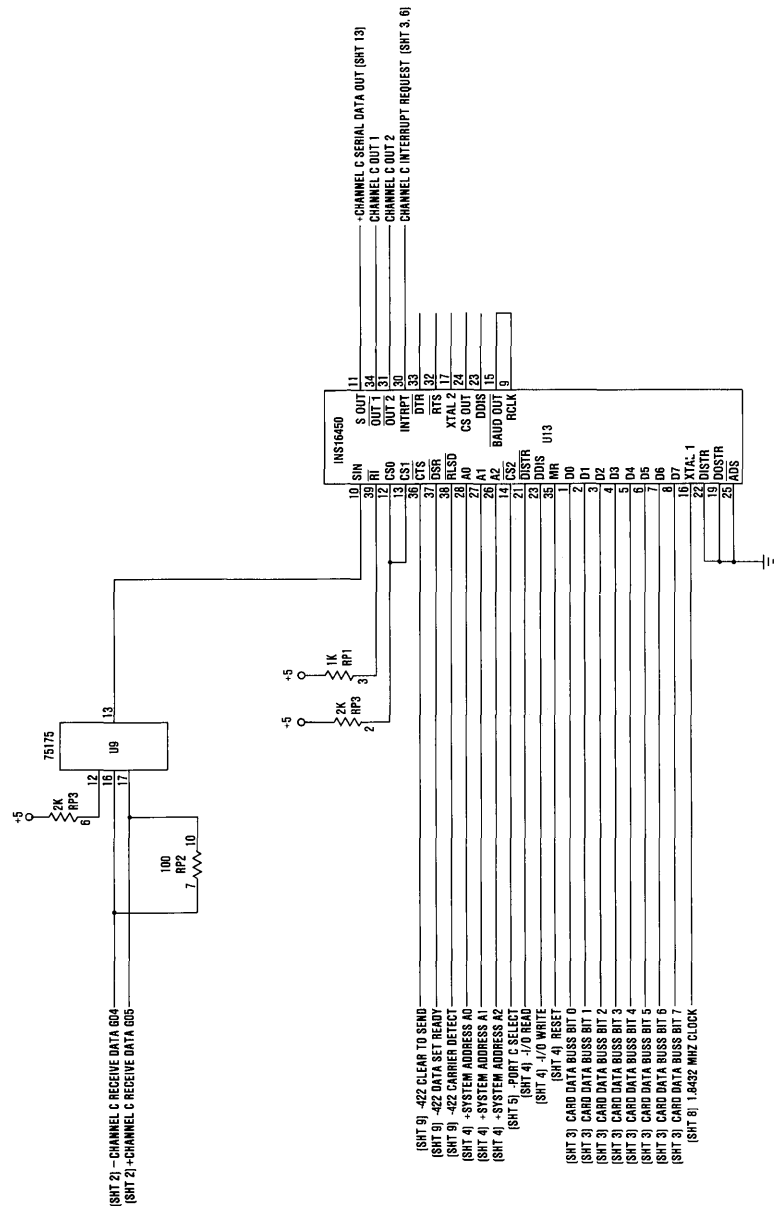

1.8432 MHZ CLOCK (SHT 9, 10, 11, 12)
6
4
U22
74LS125
5
8
1.8432 MHZ
ZY1
6323211
2
74LS04
U8
1
+5
2K
RP2
3

Sheet 9 of 13

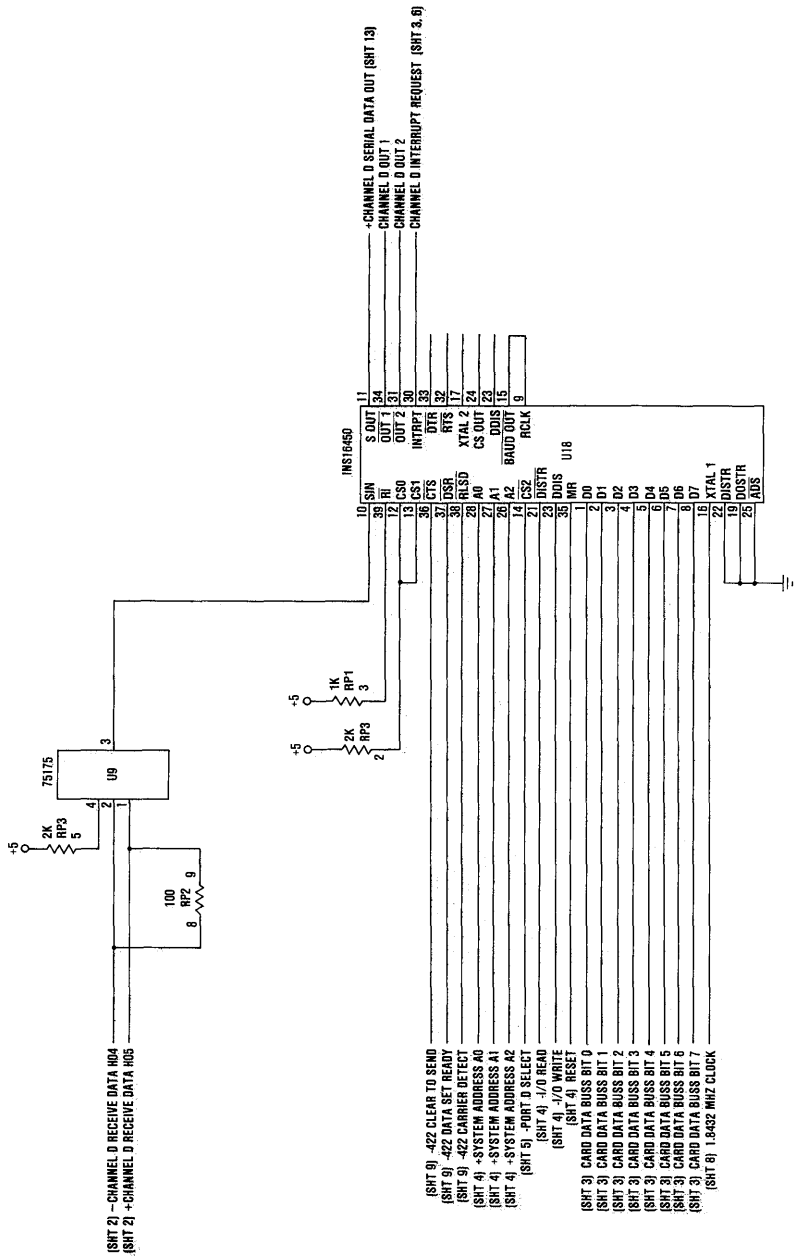

(SHT 2) – CHANNEL A RECEIVER DATA E04
(SHT 2) + CHANNEL A RECEIVER DATA E05
75175
U9
2K
RP3
100
RP2
74LS04
U6
RP3
1K
RP1
422 DATA SET READY (SHT 10, 11, 12)
422 CLEAR TO SEND (SHT 10, 11, 12)
422 CARRIER DETECT
INS16450
+ CHANNEL A SERIAL DATA OUT (SHT 13)
CHANNEL A OUT 1 N/C
CHANNEL A OUT 2 N/C
CHANNEL A INTERRUPT REQUEST (SHT 3, 6)
S OUT
OUT 1
OUT 2
INTRPT
DTR
RTS
CS OUT
DDIS
XTAL 2
SIN
DSR
CTS
RLSD
RCLK
BAUD OUT
RI
CS0
CS1
CS2
DISTR
DDIS
MR
D0
D1
D2
D3
D4
D5
D6
D7
XTAL 1
A0
A1
A2
DISTR
DDSTR
ADS
U12
(SHT 5) +PORT A SELECT
(SHT 4) -I/O READ
(SHT 4) -I/O WRITE
(SHT 4) RESET
(SHT 3) CARD DATA BUS BIT 0
(SHT 3) CARD DATA BUS BIT 1
(SHT 3) CARD DATA BUS BIT 2
(SHT 3) CARD DATA BUS BIT 3
(SHT 3) CARD DATA BUS BIT 4
(SHT 3) CARD DATA BUS BIT 5
(SHT 3) CARD DATA BUS BIT 6
(SHT 3) CARD DATA BUS BIT 7
(SHT 8) 1.8432 MHZ CLOCK
(SHT 4) +SYSTEM ADDRESS A0
(SHT 4) +SYSTEM ADDRESS A1
(SHT 4) +SYSTEM ADDRESS A2


INS16450
U18
75175
U9
+5
2K
RP3
1K
RP1
100
RP2
+CHANNEL D SERIAL DATA OUT (SHT 13)
CHANNEL D OUT 1
CHANNEL D OUT 2
CHANNEL D INTERRUPT REQUEST (SHT 3, 6)
S OUT
OUT 1
OUT 2
INTRPT
DTR
RTS
XTAL 2
CS OUT
DDIS
BAUD OUT
RCLK
SIN
RI
CS0
CS1
CTS
DSR
RLSD
A0
A1
A2
CS2
DISTR
DDIS
MR
D0
D1
D2
D3
D4
D5
D6
D7
XTAL 1
DISTR
DOSTR
ADS
(SHT 2) –CHANNEL D RECEIVE DATA H04
(SHT 2) +CHANNEL D RECEIVE DATA H05
(SHT 9) -422 CLEAR TO SEND
(SHT 9) -422 DATA SET READY
(SHT 9) -422 CARRIER DETECT
(SHT 4) +SYSTEM ADDRESS A0
(SHT 4) +SYSTEM ADDRESS A1
(SHT 4) +SYSTEM ADDRESS A2
(SHT 5) -PORT D SELECT
(SHT 4) -I/O READ
(SHT 4) -I/O WRITE
(SHT 4) RESET
(SHT 3) CARD DATA BUSS BIT 0
(SHT 3) CARD DATA BUSS BIT 1
(SHT 3) CARD DATA BUSS BIT 2
(SHT 3) CARD DATA BUSS BIT 3
(SHT 3) CARD DATA BUSS BIT 4
(SHT 3) CARD DATA BUSS BIT 5
(SHT 3) CARD DATA BUSS BIT 6
(SHT 3) CARD DATA BUSS BIT 7
(SHT 6) 1.8432 MHZ CLOCK

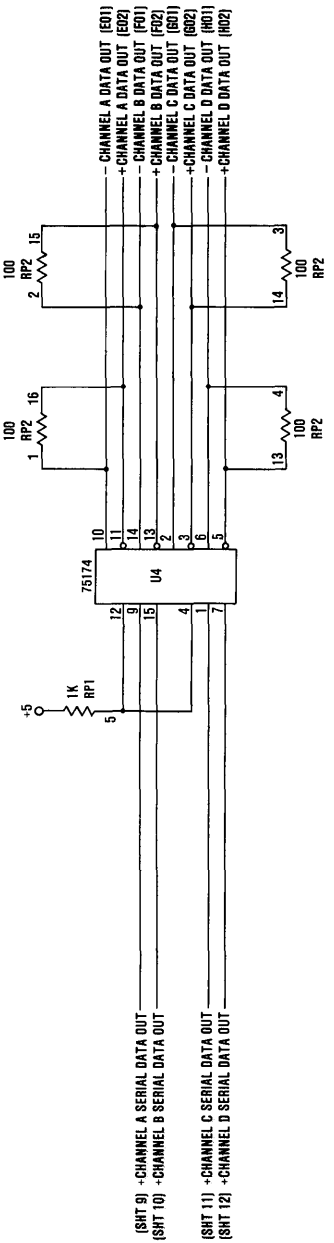
Sheet 11 of 13



Sheet 12 of 13



Sheet 13 of 13



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4-Port Asynchronous Adapter RS422A

Contents

Description

The 4-Port Asynchronous RS-422A Adapter provides four serial output ports on a 4.25- by 13.12-inch board that plugs into one I/O position. The adapter system control signals and voltage requirements are provided through a 2- by 31-position and a 2- by 18-position tab on the bottom of the adapter.

Up to four adapters may be used in one RT PC system. A DIP switch on the adapter is used to assign the adapter's I/O address range. The port I/O address assignments are contained in the adapter's I/O address range.

The adapter is fully programmable and supports asynchronous terminal attachment only. It adds and removes start bits, stop bits, and parity bits. A programmable baud-rate generator allows operation from 50 bps to 19200 bps. Five-, 6-, 7- or 8-bit characters with 1, 1-1/2, or 2 stop bits are supported. A priority interrupt system controls transmit, receive, error, line status, and data set interrupts.

Four 6-pin male AMPMODU connectors on the adapter provide external access to the four ports.

There are two versions of this adapter, one uses NS16450 LSI chip and the other uses the NS16650. Features in addition to those listed above include:

- Independent receiver clock bit.
- False start bit detection.
- Line-break generation and detection.
- The NS16450 version has full double buffering that reduces the need for precise synchronization.
- The NS16550 is capable of running all existing NS16450 software in its character mode, and in its FIFO mode has a built-in 16-byte buffer for both receive and transmit operations for improved performance.

Note: The NS16550 (Buffered) adapter can be identified by a plus (+) sign stamped at the bottom of the 6-pin interface signals connector. See Figure 9 on page 9.

All pacing of the interface and control signal status must be handled by the system software. Figure 1 on page 2 is a block diagram of the 4-Port Asynchronous RS-422A Adapter.

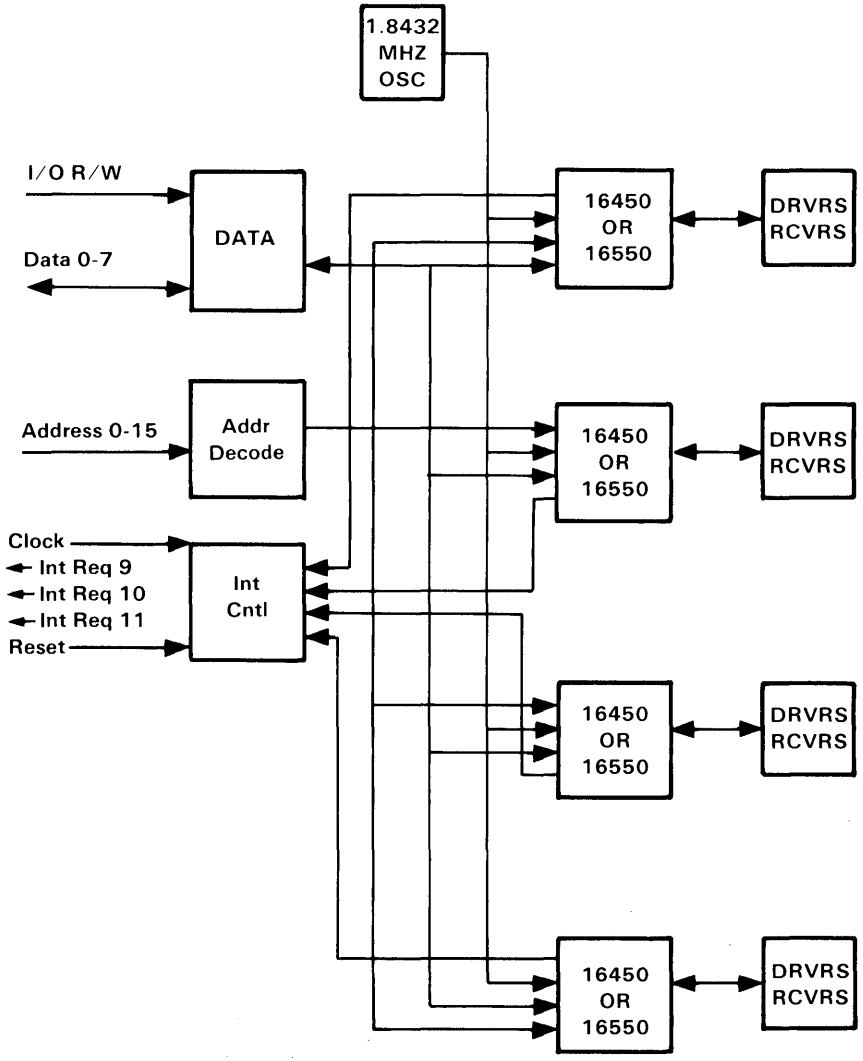


Figure 1. 4-Port Asynchronous RS-422A Adapter Block Diagram

4-Port Asynchronous RS-422A Adapter Switch Settings

The 4-Port Asynchronous RS-422A Adapter switch settings select the interrupt level and the address range of adapters installed.

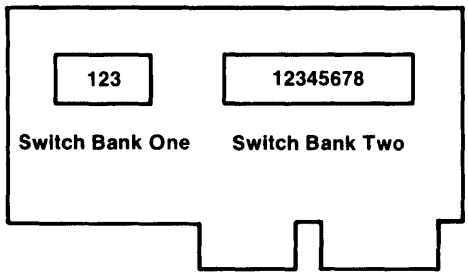


Figure 2. 4-Port Asynchronous RS-422A Adapter Switches

Interrupt Level Selected	Switch Bank One Setting		
	Switch 1	**Switch 2**	**Switch 3**
Level 9	On	Off	Off
Level 10	Off	On	Off
Level 11	Off	Off	On

Figure 3. Switch Bank One Settings

Address Range of Adapters	Switch Bank Two Setting			
	Switch 1	**Switch 2**	**Switch 3**	**Switch 4**
1230-124F	On	Off	Off	Off
2230-224F	Off	On	Off	Off
3230-324F	Off	Off	On	Off
4230-424F	Off	Off	Off	On

Figure 4. Switch Bank Two Settings

Note: Switches 5 through 8 are not used.

Modes of Operation

The different modes of operation are selected by programming the NS16450/NS16550 asynchronous communications element. Address bits A0, A1, and A2 select the different registers that define the modes of operation. Also, the divisor latch access bit (bit 7) of the line control register is used to select certain registers.

The address range for this adapter is Hex 1230 through Hex 424F. Figure 5 and Figure 6 depict a value of n which represents a variable determined by the setting of switch bank two. Switches 1, 2, 3, and 4 of switch bank two allow the adapter to operate and select the appropriate address range.

I/O Decode (In Hex) Port B	Port A	Register Selected	DLAB State
n238	n230	TX Buffer	DLAB = 0 (Write)
n238	n230	RX Buffer	DLAB = 0 (Read)
n238	n230	Divisor Latch LSB	DLAB = 1
n239	n231	Divisor Latch MSB	DLAB = 1
n239	n231	Interrupt Enable Register	DLAB = 0
n23A	n232	Interrupt Identification Register (Read)	
n23A	n232	FIFO Control Register (Write - NS16550 Only)	
n23B	n233	Line Control Register	
n23C	n234	Modem Control Register	
n23D	n235	Line Status Register	
n23E	n236	Modem Status Register	

Figure 5. I/O Decodes, Port A and Port B

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

I/O Decode (In Hex) Port D	Port C	Register Selected	DLAB State
n248	n230	TX Buffer	DLAB = 0 (Write)
n248	n240	RX Buffer	DLAB = 0 (Read)
n248	n240	Divisor Latch LSB	DLAB = 1
n249	n241	Divisor Latch MSB	DLAB = 1
n249	n241	Interrupt Enable Register	DLAB = 0
n24A	n242	Interrupt Identification Register (Read)	
n24A	n242	FIFO Control Register (Write - NS16550 Only)	
n24B	n243	Line Control Register	
n24C	n244	Modem Control Register	
n24D	n245	Line Status Register	
n24E	n246	Modem Status Register	

Figure 6. I/O Decodes, Port C and Port D

Notes:

1. n is equal to the first digit of the adapter address range
2. DLAB means Divisor Latch Access Bit.

A9—>A3 Decode	A2	A1	A0	DLAB	Register
See	x	x	x		
Note 1	0	0	0	0	Receive Buffer Reg. (Read) Transmit Holding Reg. (Write)
	0	0	1	0	Interrupt Enable
	0	1	0	x	Interrupt Identification (Read Only)
	0	1	0	x	FIFO Control (Write - NS16550 Only)
	0	1	1	x	Line Control
	1	0	0	x	Modem Control
	1	0	1	x	Line Status
	1	1	0	x	Modem Status
	1	1	1	x	Scratch (See note 3)
	0	0	0	1	Divisor Latch (LSB)
	0	0	1	1	Divisor Latch (MSB)

Figure 7. Address Bits

Notes:

1. Bits A9 through A3 are used to select specific adapter and serial port.
2. A2, A1, and A0 bits are *don't cares* and are used to select the different registers of the NS16450/NS16550 chip.
3. The Scratch Register of the NS16450/NS16550 module should be initialized to all ones and never be written to with any data afterwards. This would cause indeterminate data when Read address n237 (see "Interrupts" on page 8) is executed.

Interrupts

Three interrupt lines are provided to the system. The interrupt level (9, 10, or 11) is selected by placing the appropriate switch on switch bank one to the on position. An interrupt register (read adr n237, where n is first digit of the address range) is provided for storage of pending port interrupts. Interrupt register bit assignments are shown in Figure 8.

Hex Address n237							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	Port 4	Port 3	Port 2	Port 1

Figure 8. Interrupt Register Read Format

Before the 4-Port Asynchronous RS-422A Adapter can generate an interrupt to the processor, it must be enabled by writing any data byte to the interrupt enable address. This address corresponds to the interrupt level that the adapter is jumpered for.

The enable for interrupt level 9 is hex address 02F2.

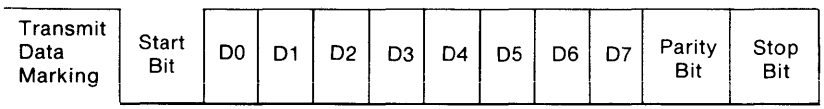
The enable for interrupt level 10 is hex address 06F2.

The enable for interrupt level 11 is hex address 06F3.

After the adapter generates an interrupt, it must be reset by writing any data byte to the interrupt enable address for that interrupt.

Serial Data Format

The data format is as follows:



Data bit 0 is the first bit to be transmitted or received. The adapter automatically inserts the start bit, the correct parity bit (if programmed to do so), and the stop bit (1, 1-1/2, or 2 depending on the command in the line control register).

External Interface Description

The adapter provides an EIA 4-Port Asynchronous RS-422A Adapter interface.

The pin functions for the 6-pin male connector are shown in Figure 9.

Pin	Signal
1	- Transmit Data
2	+ Transmit Data
3	No Connection
4	- Receive Data
5	+ Receive Data
6	No Connection

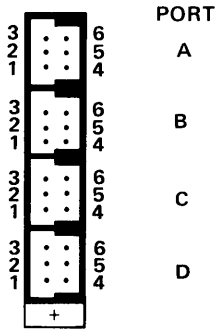


Figure 9. 6-Pin Interface Signals Connector (as viewed from rear of adapter)

The adapter converts the interface signals from TTL levels to EIA RS-422A voltage levels, and vice versa. These signals are sampled or generated by the communications control chip. These signals can then be sensed by the system software to determine the state of the interface or peripheral device. The drivers and receivers used on the adapter are the inverting type; therefore, a 0 EIA level on the line is received or transmitted as a 0 TTL level, and a 1 EIA level is received or transmitted as a 1 TTL level.

Voltage Interchange Information

The electrical characteristics for voltage interchange information are designed to meet the requirements of EIA RS-422A standard.

For interface control circuits, the input to the receiver, measured differentially, shall be greater than + 200 millivolts for a binary 0 and greater than -200 millivolts for a binary 1. (See Figure 10).

Interchange Differential Voltage (A-B)	Binary State	Signal Condition	Interface Control Function
Positive Voltage	Binary 0	Spacing	= On
Negative Voltage	Binary 1	Marking	= Off

Figure 10. 4-Port Asynchronous RS-422A Adapter Signal Levels

Asynchronous Communications Element Pin Description

The following describes the function of all NS16450/NS16550 input/output pins. Some of these descriptions reference internal circuits. The use of each signal as implemented on the multiport adapter is described.

Note: In the following descriptions, a low represents a logical 0 (0 Vdc nominal) and a high represents a logical 1 (+ 2.4 Vdc nominal).

Input Signals

Chip Select (CS0, CS1, -CS2), Pins 12-14: When CS0 and CS1 are high and -CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) address strobe (-ADS) input. This enables communications between the NS16450/NS16550 and the processor.

Data Input Strobe (DISTR, -DISTR), Pins 22 and 21: When DISTR is high or -DISTR is low while the chip is selected, this signal allows the processor to read status information or data from a selected register of the NS16450/NS16550.

Note: Only one active DISTR or -DISTR input is required to transfer data from the NS16450/NS16550 during a read operation. Therefore, the DISTR input has been permanently tied low and the -DISTR line is used.

Data Output Strobe (DOSTR, -DOSTR), Pins 19 and 18: When DOSTR is high or -DOSTR is low while the chip is selected, this signal allows the processor to write data or control words into a selected register of the NS16450/NS16550.

Note: Only one active DOSTR or -DOSTR input is required to transfer data to the NS16450/NS16550 during a write operation. Therefore, the DOSTR input has been permanently tied low and the -DOSTR input is used.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an NS16450/NS16550 register to read from or write into as indicated in the table below. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain NS16450/NS16550 registers. The DLAB must be set high by the system software to access the baud-generator divisor latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (Read)
0	0	0	0	Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable
x	0	1	0	Interrupt Identification (Read Only)
x	0	1	0	FIFO Control (Write - NS16550 Only)
x	0	1	1	Line Control
x	1	0	0	Modem Control
x	1	0	1	Line Status
x	1	1	0	Modem Status
x	1	1	1	Scratch
1	0	0	0	Divisor Latch (Least Significant Byte)
1	0	0	0	Divisor Latch (Most Significant Byte)

Figure 11. NS16450/NS16550 Register Selection

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low, 0-3 Forced and 4-7 Permanent
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 are Low, and Bits 3-7 are Permanent
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
Modem Status Register	Master Reset	Bits 0-3 are Low, Bits 4-7 = Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errors)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IRR/ Write THR/ MR	Low
RCVR FIFO	MR/ FCR1•FCR0/ ΔFCR0	Low

Figure 12 (Part 1 of 2). NS16450/NS16550 Reset Functions

Register/Signal	Reset Control	Reset State
XMIT FIFO	MR/ FCR2•FCR0/ ΔFCR0	Low
FIFO Control Register	Master Reset	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
-OUT 2 -RTS -DTR -OUT 1	Master Reset Master Reset Master Reset Master Reset	High High High High

Figure 12 (Part 2 of 2). NS16450/NS16550 Reset Functions

-Address Strobe (-ADS), Pin 25: When low, this signal provides latching for the register select (A0, A1, A2) and chip select (CS0, CS1, -CS2) signals.

Note: The -ADS input has been tied low because the register select (A0, A1, A2) signals are stable for the duration of a read or write operation.

Master Reset (MR), Pin 35: When high, this signal clears all the registers (except the receive buffer, transmitter holding, and divisor latches), and the control logical of the NS16450/ NS16550. Also, the state of various output signals (SOUT, INTRPT, -OUT 1, -OUT 2, -RTS, -DTR) is affected by an active MR input. Refer to:

Receiver Clock (RCLK), Pin 9: This input is the 16x baud-rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, modem, or data set).

-Clear to Send (-CTS), Pin 36: The -CTS signal is a modem control function input whose condition the processor can test by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates whether the -CTS input has changed state since the previous reading of the modem status register.

Note: The CTS bit of the modem status register is tied to the active state.

-Data Set Ready (-DSR), Pin 37: The -DSR signal is a modem control function input whose condition the processor can test by reading bit 5 (DSR) of the modem status register. When low, this signal indicates that the modem or data set is ready to establish the communications link and transfer data with the NS16450/NS16550. Bit 1 (DDSR) of the modem status register indicates whether the -DSR input has changed since the previous reading of the modem status register.

Note: The DSR bit of the modem status register is tied to the active state.

-Received Line Signal Detect (-RLSD), Pin 38: The -RLSD signal is a modem control function input whose condition the processor can test by reading bit 7 (RLSD) of the modem status register. When low, this signal indicates that the data carrier has been detected by the modem or data set. Bit 3 (DRLSD) of the modem status register indicates whether the -RLSD input has changed state since the previous reading of the modem status register.

Notes:

1. The RLSD bit of the modem status register is tied to the active state.
2. Received Line Signal Detect is also called Data Carrier Detect (DCD), or Carrier Detect (CD).

-Ring Indicator (-RI), Pin 39: The -RI signal is a modem control function input whose condition the processor can test by reading bit 6 (RI) of the modem status register. When low, this signal indicates that a telephone ringing signal has been received by the modem or data set. Bit 2 (TERI) of the modem status register indicates whether the -RI input has changed from a low to high state since the previous reading of the modem status register.

Note: The RI bit of the modem status register is tied to the inactive state.

VCC, Pin 40: + 5 Vdc supply

VSS, Pin 20: Ground (0 Vdc) reference.

Output Signals

-Data Terminal Ready (-DTR), Pin 33: When low, this signal informs the modem or data set that the NS16450/NS16550 is ready to communicate. The -DTR output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. The -DTR signal is set high upon a master reset operation. The -DTR signal is forced to high during loop mode operation. See note below.

-Request To Send (-RTS), Pin 32: When low, this signal informs the modem or data set that the NS16450/NS16550 is ready to transmit data. The -RTS output signal can be set to an active low by programming bit 1 (RTS) of the modem control register. The -RTS signal is set high by a master reset operation. The -RTS signal is forced to high during loop mode operation. See note below.

-Output 1 (-OUT 1), Pin 34: With this signal, user-designated output can be set to an active low by programming bit 2 (-OUT 1) of the modem control register to a high level. The -OUT 1 signal is set high by a master reset operation. The -OUT 1 signal is forced to high during loop mode operation. See note below.

-Output 2 (-OUT 2), Pin 31: With this signal, user-designated output can be set to an active low by programming bit 3 (-OUT 2) of the modem control register to a high level. The -OUT 2 signal is set high by a master reset operation. The -OUT 2 signal is forced to high during the loop mode operation. See note below.

Chip Select Out (CSOUT), Pin 24: NS16450 Only When high, this signal indicates that the chip has been selected by active CS0, CS1, and -CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logical 1. This signal is not used.

TXRDY, RXRDY, Pins 24,29: NS16550 Only; Transmitter and receiver pins for DMA signaling. The adapter does not use these pins.

Driver Disable (DDIS), Pin 23: This signal goes low whenever the processor is reading data from the NS16450/NS16550.

-Baudout (-BAUDOUT), Pin 15: This is a 16x clock signal for the transmitter section of the NS16450/NS16550. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud-generator division latches. The -BAUDOUT is tied to the receiver section of the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: This signal goes high whenever any one of the following interrupt types has an active high condition and is enabled through the IIR: receiver error flag, received data available, transmitter holding register empty, or modem status. For the NS16550, this signal also goes high for timeout (FIFO mode only). The INTRPT signal is reset lowby the appropriate interrupt service or a master reset operation.

Serial Output (SOUT), Pin 11: This signal is a composite serial data output to the communications link ripheral, modem or data set). The SOUT signal is set to the marking (logical 1) state upon a master reset operation.

Note: This pin is not used on the 4-Port Asynchronous RS-422A Adapter board.

Input/Output Signals

Data Bus (D7-D0), Pins 1-8: This bus contains eight tri-state input/output lines. The bus provides bidirectional communications between the NS16450/NS16550 and the processor. Data, control words, and status information are transferred through the D7-D0 data bus.

External Clock Input/Output (XTAL1, XTAL2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the NS16450/NS16550.

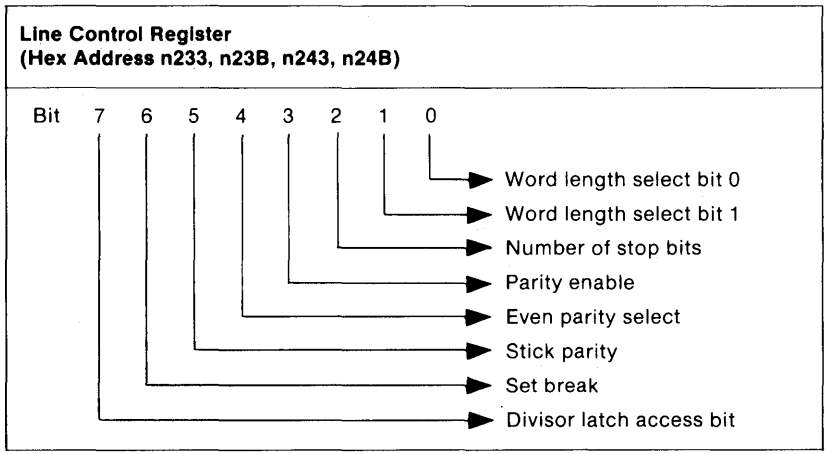
Programming Considerations

The NS16450/NS16550 has a number of accessible registers. The system programmer may access or control any of the NS16450/NS16550 registers through the processor. These registers are used to control NS16450/NS16550 operations and to transmit and receive data.

Note: The n in address is the first digit of the adapter address range (1-4).

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange through the line control register. In addition to controlling the format, the programmer may retrieve the contents of the line control register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the line control register are described below:



Bits 0, 1 These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2 This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logical 0, one stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logical 1 when a 5-bit word length is selected through bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is a logical 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated or checked.

Bit 3 This bit is the parity enable bit. When bit 3 is a logical 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed.)

Bit 4 This bit is the even parity select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logical 1 and bit 4 is a logical 1, an even number of bits are transmitted or checked.

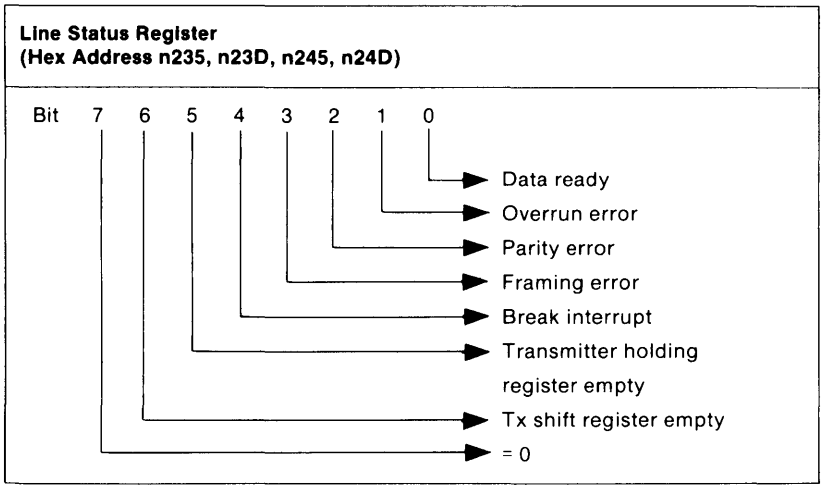
Bit 5 This bit is the stick parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is transmitted and then detected by the receiver as a logical 0 (space parity) if bit 4 is a logical 1, or as a logical 1 (mark parity) if bit 4 is a logical 0.

Bit 6 This bit is the set break control bit. When bit 6 is a logical 1, the serial output (SOUT) forces a spacing (logical 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logical 0. This feature enables the processor to alert a terminal in a computer communications system.

Bit 7 This bit is the divisor latch access bit (DLAB). It must be set high (logical 1) to access the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Line Status Register

This 8-bit register provides status information to the processor concerning the data transfer. The contents of the line status register are described below:



Bit 0 This bit is the receiver data ready (DR) indicator. Bit 0 is set to a logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register or the FIFO. Bit 0 may be reset to a logical 0 either by the processor reading the data in the receiver buffer or by writing a logical 0 into it from the processor.

Bit 1 This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the processor before the next character was transferred into the receiver buffer register, and that the previous character was thereby destroyed. The OE indicator is reset whenever the processor reads the contents of the line status register.

Bit 2 This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity as selected by the even parity-select bit. The PE bit is set to a logical 1 upon detection of a parity error and is reset to a logical 0 whenever the processor reads the contents of the line status register. For the NS16550 in the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the system when its associated character is at the top of the FIFO.

Bit 3 This bit is the framing error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logical 1 whenever the stop bit following the last data bit or parity is detected as a 0 bit (spacing level). The FE indicator is reset whenever the system reads the contents of the line status indicator. For the NS16550 in the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the system when its associated character is at the top of the FIFO.

Bit 4 This bit is the break interrupt (BI) indicator. Bit 4 is set to a logical 1 whenever the received data input is held in the spacing (logical 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits). The BI indicator is reset whenever the system reads the contents of the line status indicator. For the NS16550 in the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the system when its associated character is at the top of the FIFO. When break occurs only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected.

Bit 5 This bit is the transmitter holding register empty (THRE) indicator. Bit 5 indicates that the NS16450/NS16550 is ready to accept a new character for transmission. In addition, this bit causes the NS16450/NS16550 to issue an interrupt to the processor when the transmit holding register empty interrupt enable is set high. The THRE bit is set to a logical 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logical 0 concurrently with the loading of the transmitter holding register by the processor. For the NS16550 in the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.

Bit 6 This bit is the transmitter empty (TEMT) indicator. Bit 6 is set to a logical 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logical 0 whenever either the THR or TSR contain a data character. Bit 6 is a read-only bit. For the NS16550 in the FIFO mode, this bit is set to 1 whenever the transmitter FIFO and shift register are both empty.

Bit 7 In the character mode this is a 0. For the NS16550 in the FIFO mode, this bit is set when there is at least one parity error, framing error or break indication in the FIFO. Bit 7 is cleared when the processor reads the line status register, if there are no subsequent errors in the FIFO.

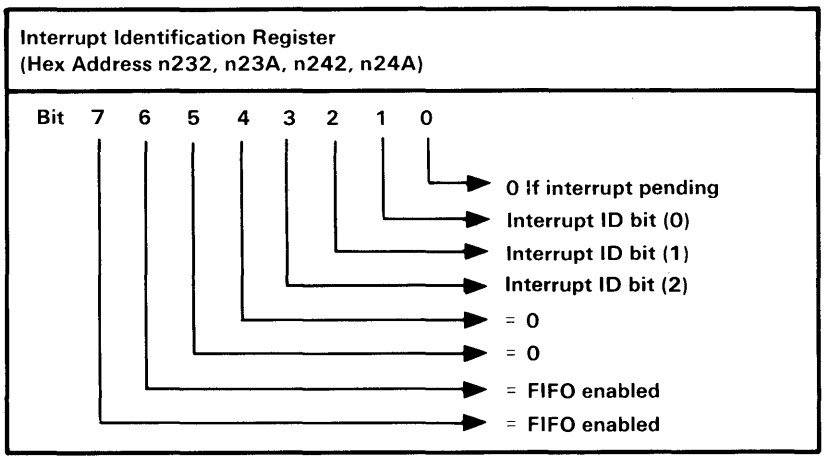
Note: The line status register is for read operations only.

Interrupt Identification Register

The NS16450/NS16550 has an on-chip interrupt capability that allows for complete flexibility in interfacing to microprocessors. In order to provide minimum software overhead during data character transfers, the NS16450/NS16550 sets interrupts into four priority levels:

- Receiver line status (priority 1)
- Received data ready (priority 2), or for the NS16550 in the FIFO mode, timeout in the FIFO.
- Transmitter holding register empty (priority 3)
- Modem status (priority 4).

Information indicating that a priority interrupt is pending and information on the type of interrupt is stored in the interrupt identification register. Refer to the "Interrupt Control Functions" table in Figure 13 on page 21. The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending, and no other interrupts are acknowledged until that particular interrupt is serviced by the processor. The contents of the IIR are described below:



Bit 0 This bit can be used in a hardwired, priority, or polled environment to indicate whether an interrupt is pending. When bit 0 is a logical 0, an interrupt is pending and the IIR contents are used as a pointer to the appropriate interrupt service routine. When bit 0 is a logical 1, no interrupt is pending, and polling (if used) is continued.

Bits 1, 2 These 2 bits of the IIR are used to identify the highest priority interrupt pending as indicated in Figure 13 on page 21.

Bits 3-7 For the NS16450 these 5 bits of the IIR are always logical 0. For the NS16550:

Bit 3 In the character mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 - 5 These 2 bits of the IRR are always logical 0.

Bit 6 - 7 These 2 bits are set when FCR0 = 1.

Interrupt ID Register				Interrupt Set and Reset Functions			
Bit 3*	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt.	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or for NS16550, Trigger Level Reached	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time.	Reading the Receiver Buffer Register

Figure 13 (Part 1 of 2). Interrupt Control Functions

Interrupt ID Register				Interrupt Set and Reset Functions			
Bit 3*	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Figure 13 (Part 2 of 2). Interrupt Control Functions

Note: * = Applicable to NS16550 only.

FIFO Control Register

This is an 8-bit write only register at the same location as the interrupt identification register. This register enables the FIFOs, clears the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Bit 0 Setting bit 0 to 1 enables both the XMIT and RCVR FIFOs. Resetting bit 0 clears all bytes in both FIFOs. When changing from FIFO mode to character mode and vice versa, data is not automatically cleared from the FIFOs. Therefore, the FIFOs should be cleared before changing modes. This bit must be a 1 when other FIFO control register bits are written to or they will not be programmed.

Bit 1 Setting bit 1 to 1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 written to this bit position is self clearing.

Bit 2 Setting bit 2 to 1 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 written to this bit position is self clearing.

Bit 3 Setting bit 3 to 1 changes the RXRDY and TXRDY pins from mode 0 to mode 1 if bit 0 = 1.

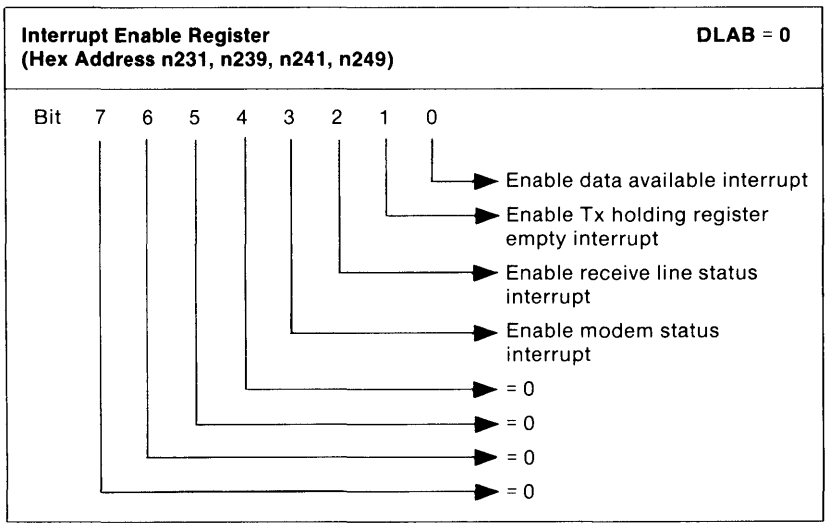
Bit 4, 5 Reserved

Bit 6,7 These 2 bits set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the NS16450/NS16550 to separately activate the chip interrupt (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the interrupt enable register. Similarly, setting the appropriate bits of this register to a logical 1, can enable selected interrupts. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are described below:



Bit 0 This bit enables the received data available interrupt and for the NS16550, timeout interrupts in the FIFO mode, when set to a logical 1.

Bit 1 This bit enables the transmitter holding register empty interrupt when set to a logical 1.

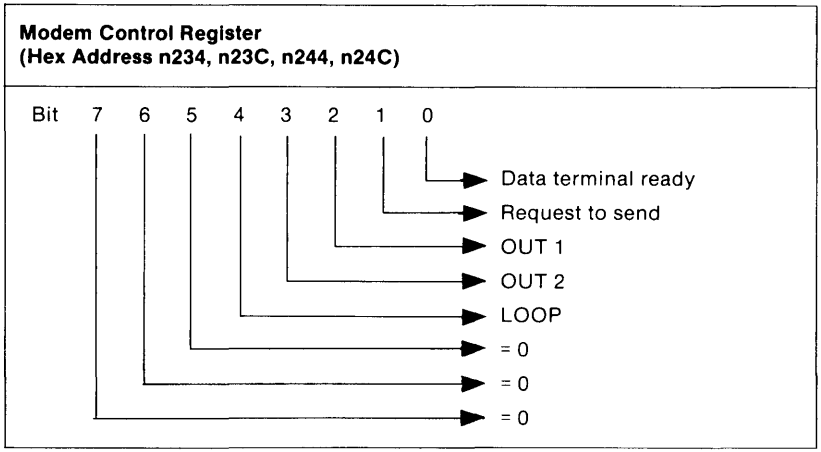
Bit 2 This bit enables the receiver line status interrupt when set to a logical 1.

Bit 3 This bit enables the modem status interrupt when set to a logical 1.

Bits 4-7 These 4 bits are always logical 0.

Modem Control Register

Bit four of this 8-bit register is used for diagnostic testing of the NS16450/NS16550. All other bits are not used on the 4-Port Asynchronous RS-422A Adapter. The contents of the modem control register are described below:



Bit 0 This bit controls the data terminal ready (-DTR) output. When bit 0 is set to a logical 1, the -DTR output is forced to a logical 0. When bit 0 is reset to a logical 0, the -DTR output is forced to a logical 1.

Bit 1 This bit controls the request to send (-RTS) output. Bit 1 affects the -RTS output in a manner identical to that described above for bit 0.

Bit 2 This bit controls the output 1 (-OUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the -OUT 1 output in a manner identical to that described above for bit 0.

Bit 3 This bit controls the output 2 (-OUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the -OUT 2 output in a manner identical to that described above for bit 0.

Note: The -OUT 2 output of the NS16450/NS16550 may be applied to an EIA inverting line driver to obtain the proper polarity input at the modem or data set.

Bit 4 This bit provides a loopback feature for diagnostic testing of the NS16450/NS16550. When bit 4 is set to logical 1, the following occurs:

The transmitter serial output (SOUT) is set to the marking (logical 1) state.

The receiver serial input (SIN) is disconnected.

The output of the transmitter shift register is *looped back* into the receiver shift register input.

The four modem control inputs (-CTS, -DSR, -RLSD, and -RI) are disconnected.

The four modem control outputs (-DTR, -RTS, -OUT 1, and -OUT 2) are internally connected to the four modem control inputs.

The modem control output pins are forced high.

In the the diagnostic mode the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the sources of the interrupts are now the lower 4 bits of the modem control register instead of the 4 modem control inputs. The interrupts are still controlled by the interrupt enable register.

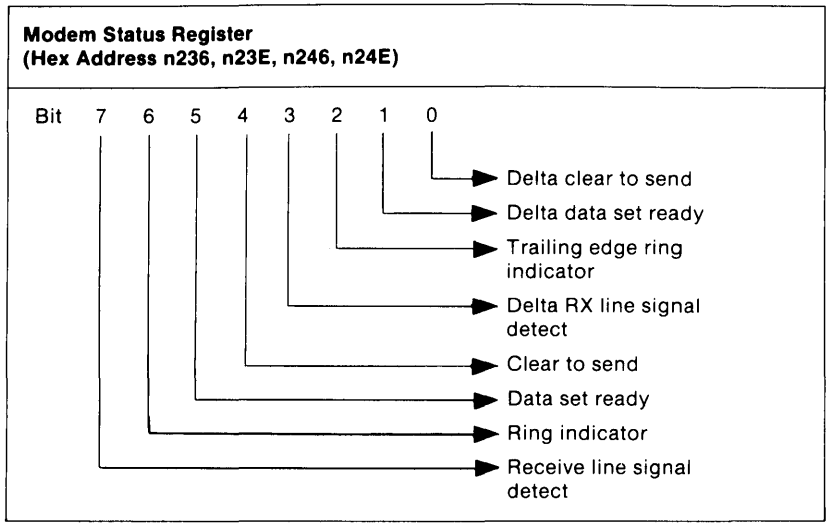
The NS16450/NS16550 interrupt system can be tested by writing into the lower 6 bits of the line status register and into the lower 4 bits of the modem status register. Setting any of these bits to a logical 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal NS16450/ NS16550 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the modem control register must be reset to logical 0. The transmitter should be idle when this bit changes state.

Bits 5-7 These bits are permanently set to logical 0.

Modem Status Register

This 8-bit register provides the current state of the control lines to the processor. Since the adapter does not use the modem control lines, this register will not present useful status.

The contents of the modem status register are described below:



Bit 0 This bit is the delta clear-to-send (DCTS) indicator. Bit 0 indicates that the -CTS input to the chip changed state since the last time it was read by the processor.

Bit 1 This bit is the delta data-set-ready (DDSR) indicator. Bit 1 indicates that the -DSR input to the chip changed state since the last time it was read by the processor.

Bit 2 This bit is the trailing edge of the ring indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from an on (logical 1) to an off (logical 0) condition.

Bit 3 This bit is the delta received line signal detector (DRLSD) indicator. Bit 3 indicates that the -RLSD input to the chip changed state since the last time it was read by the processor.

Note: Whenever bit 0, 1, 2, or 3 is set to a logical 1, a modem status interrupt is generated if the appropriate interrupt enable bit is set in the IER.

Bit 4 This bit is the complement of the clear to send (-CTS) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to RTS in the MCR.

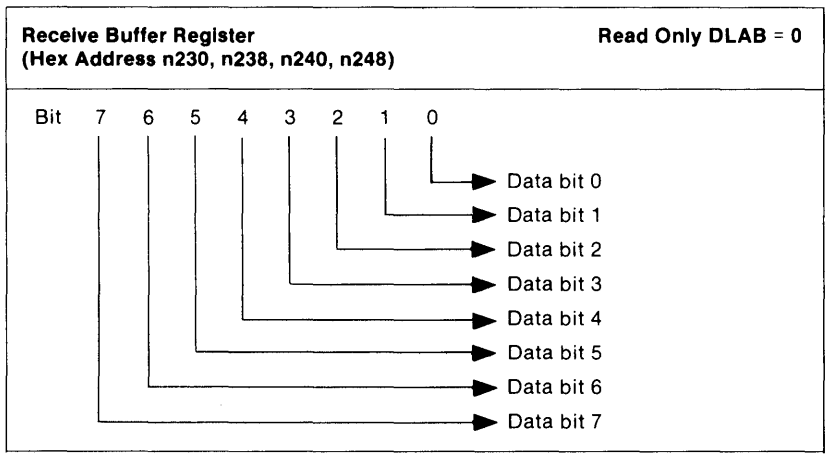
Bit 5 This bit is the complement of the data set ready (-DSR) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to DTR in the MCR.

Bit 6 This bit is the complement of the ring indicator (-RI) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to -OUT 1 in the MCR.

Bit 7 This bit is the complement of the received line signal detect (-RLSD) input. Setting bit 4 (loop) of the MCR to a logical 1, makes this bit equivalent to -OUT 2 of the MCR.

Receiver Buffer Register

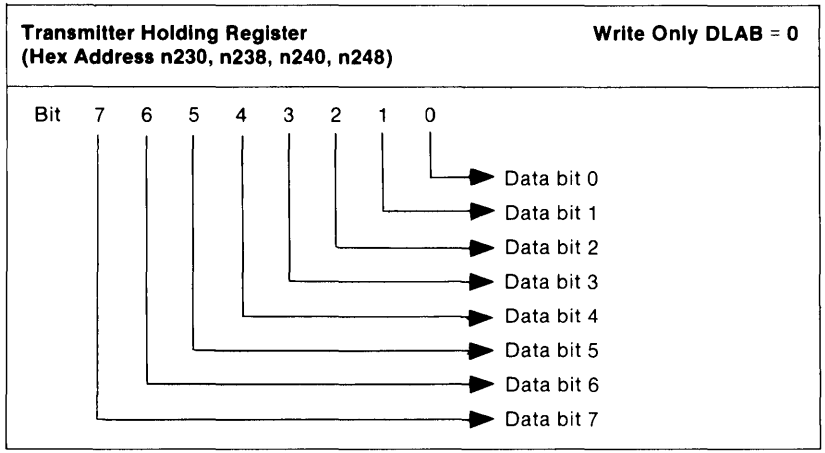
The receiver buffer register contains the received character as defined below:



Bit 0 is the least significant bit and is the first bit serially received.

Transmitter Holding Register

The transmitter holding register contains the character to be serially transmitted and is defined below:



Bit 0 is the least significant bit and is the first bit serially transmitted.

Programmable Baud-Rate Generator

The NS16450/NS16550 contains a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 655,535 or 2^{16}-1. The output frequency of the baud generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to ensure desired operation of the baud-rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The following figures show the contents of the divisor latches.

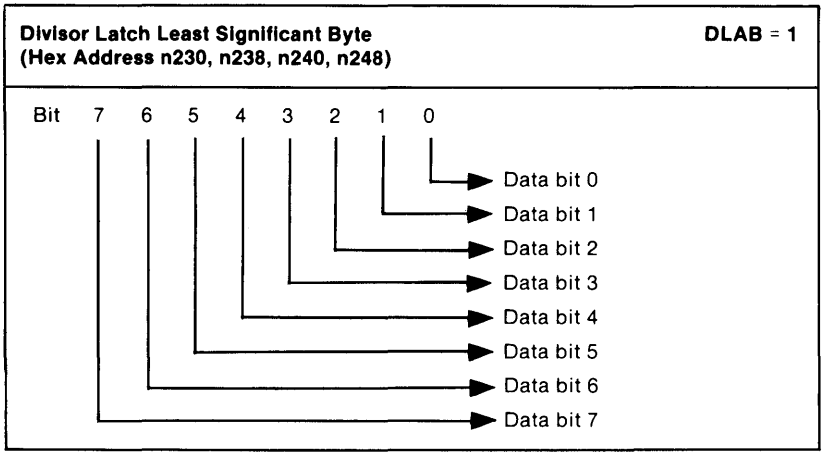


Figure 14. Divisor Latch Least Significant Byte

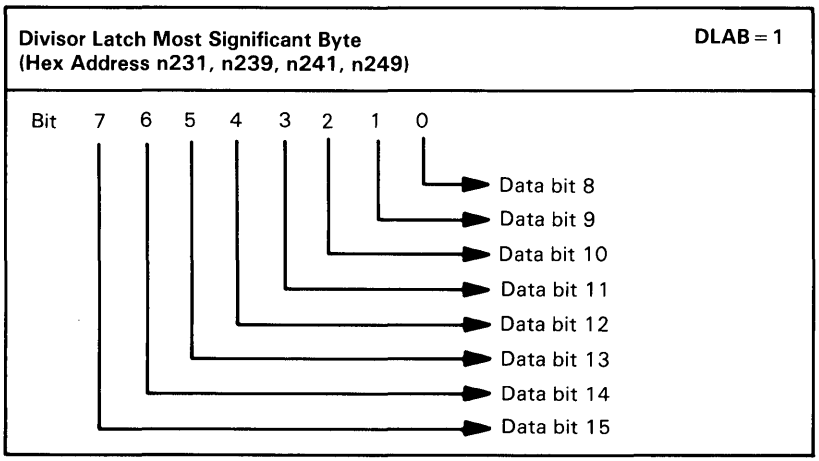


Figure 15. Divisor Latch Most Significant Byte

Figure 16 illustrates the use of the baud-rate generator with a frequency of 1.8432 MHz. For baud rates of 19,200 and below, the error obtained is minimal.

Note: In no case should the data rate be greater than 19,200 baud.

Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent Error Difference Between Desired and Actual
50	2304	900	—
75	1536	600	—
110	1047	417	0.026
134.5	857	359	0.058
150	786	300	—
300	384	180	—
600	192	C0	—
1200	96	60	—
1800	64	40	—
2000	58	3A	0.69
2400	48	30	—
3600	32	20	—
4800	24	18	—
7200	16	10	—
9600	12	C	—
19200	6	6	—

Figure 16. Baud Rates at 1.8432 MHz

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled on the NS16550, (FCR bit 0 = 1, IER bit 0 = 1) RCVR interrupts will occur as follows:

- The receive data available interrupt is issued to the system when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below the trigger level.
- The interrupt identification register receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR = x6), as before, has higher priority than the received data available (IIR = x4) interrupt.
- The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows.

- A FIFO timeout will occur if the following conditions exist:
  - At least one character is in the FIFO
  - The most recent character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
  - The most recent system read of the FIFO was longer than 4 continuous character times ago.
  - This causes a maximum character received to interrupt issued delay of 160 milliseconds at 300 BAUD with a 12 bit character.
- Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
- When a timeout interrupt has occurred, it is cleared and the timer reset when the system reads one character from the RCVR FIFO.
- When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the system reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = 1, IER bit 1 = 1), XMIT interrupts will occur as follows.

- The transmitter holding register interrupt (THRE) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

- The transmitter FIFO empty indications are delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE = 1. The first transmitter interrupt after changing FCR bit 0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

With FCR bit 0 = 1 resetting IER bits 0 through 3 puts the NS16550 in the FIFO polled mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program checks RCVR and XMITTER status via the line status register. As stated previously:

- Line status register bit 0 is set as long as there is one byte in the RCVR FIFO.
- Line status register bits 1 through 4 specify which errors have occurred. Character error status is handled the same way as when in the interrupt mode. The interrupt identification register is not affected since interrupt enable register bit 2 = 0.
- Line status register bit 5 indicates when the XMIT FIFO is empty.
- Line status register bit 6 indicates that both the XMIT FIFO and shift register are empty.
- Line status register bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO polled mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Connector Specifications

The adapter has a 6-pin connector at the rear of the adapter. The following figure shows the signals and their pin assignments.

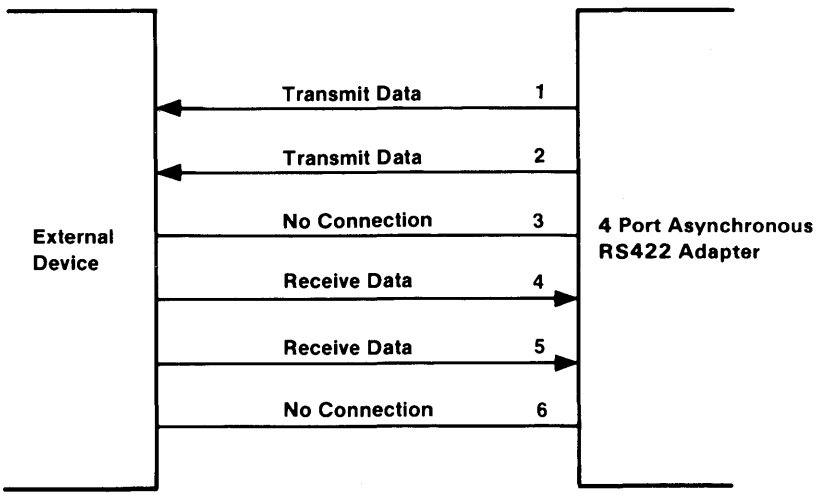


Figure 17. Connector Specifications

Note: See Figure 9 on page 9 for connector pin functions.

IBM

Personal Computer
Hardware Reference
Library

Baseband Adapter

Contents

Local Area Networks

A local area network (LAN) interconnects computers and terminals to permit high-speed data exchange and the shared use of supporting devices such as printers and disk drives.

A network's cabling system may link computers within the same office, on different floors, or in different buildings. Distances are typically under one mile, but may extend to several miles with the use of signal-boosting repeaters. LANs are usually private, but may connect to other local area networks or have gateways to public networks.

Local area networks may differ by the type of transmission cables and cable attachments used to connect stations in the network. They can also differ by the way they control a station's access to the network and manage network dataflow.

Baseband LAN (Description)

The baseband local area network is a standard network using a baseband coaxial cable to connect stations and supporting devices. The baseband cabling system may consist of either standard Ethernet coaxial cable, thin coaxial cable, or a mixture of both.

The term baseband describes the frequency bandwidth that carries network signals in the coaxial cable. It tells us that the entire bandwidth of 10 Megabits per second represents a single channel for carrying network signals. The 10Mb per second bandwidth is not subdivided into multiple channels as in broadband usage.

To describe the components and functions of a baseband cable system, this discussion is supported by figure 1. A standard coaxial cable system is discussed first and then a thin coaxial cable system. For discussion purposes, the illustrations reflect hardware commonly used in the industry. Your particular system may vary slightly.

Specification sheets for both cable types are found in "Specifications" on page 27. Consult your supplier for the specific components in your system.

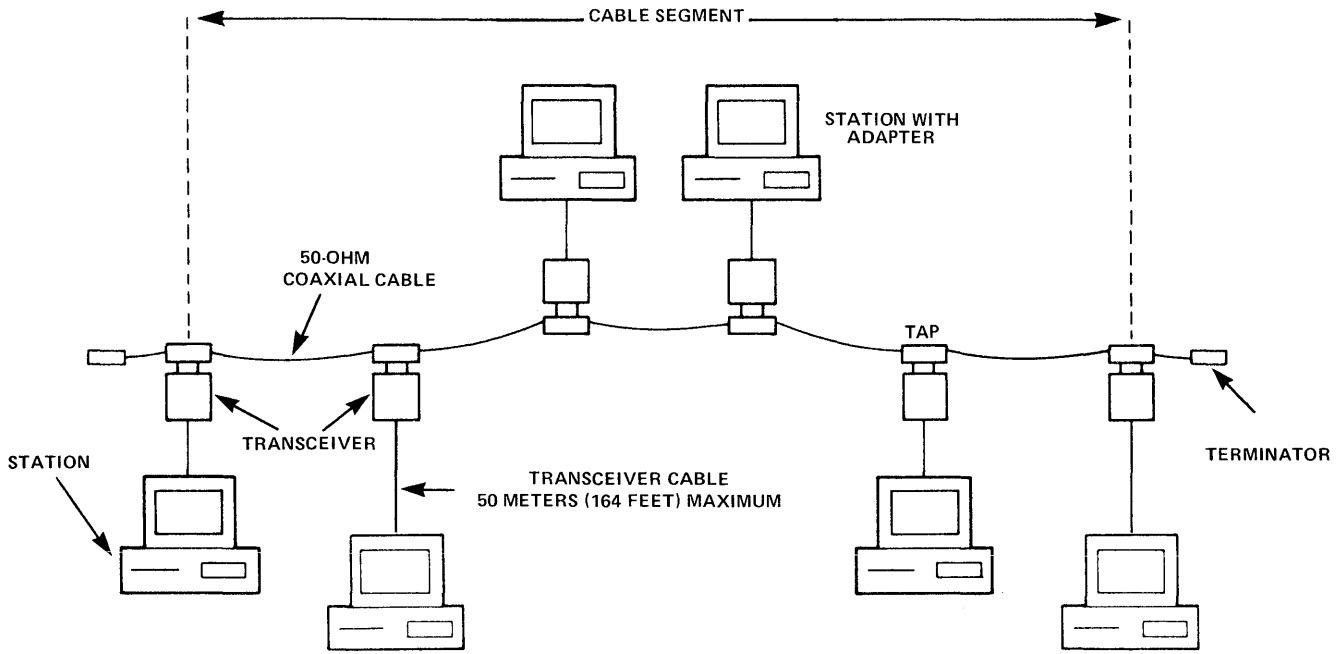


Figure 1. Baseband Cable System

General Features

- A baseband transmission cabling system connects computer stations and supporting devices and provides a standard access and control system for data exchange.
- The cabling system is equipped with access taps and transceivers to serve each station.
- The cabling system is equipped with fixtures for terminating cable segments or extending their effective range.
- The cabling system can be equipped to link the network to other independent networks, public or private.
- For each station, access to the network is controlled by an adapter controller which operates with the CPU of a host computer.

Single Channel, Half-duplex

This type of communications channel uses only one carrier bandwidth (Baseband), which is shared by all the stations on the network. The channel is a half-duplex channel which means it will not allow simultaneous transmission and reception.

Transmission Speed (10 Megabits per second)

The Baseband Adapter transmits data at the rate of 10 Megabits per second.

Multi-access Bus Topology

The cabling system connecting stations and their supporting devices is a multi-access bus. The bus serves as a single line transmission medium with an access tap for each station.

Station access to the network is regulated by the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) method. With this method each station monitors the network to detect transmissions from other stations. A listening station then transmits its data only when the network is free.

If two stations transmit at the same instant, a collision occurs. Upon colliding, each transmitting station halts and resumes at some random interval. The time intervals are measured in fractional seconds so that it appears like large numbers of stations are using the network simultaneously.

Network Components

The following sections take a closer look at the individual components comprising the network. The components fall into three general categories:

1. Major components which attach to the cable or form an interface between the cable and user stations
2. Coaxial cable and connectors which serve to extend, terminate, or condition the cable in some way
3. The user stations themselves.

Note: IBM supplies the Baseband Adapter but does not supply cables or cabling components. Consult your Ethernet cable supplier for more information.

Adapter Controller

Each station is equipped with an adapter controller. The adapter occupies one internal I/O slot and acts as an interface controller to the network.

Coaxial Cable Transmission Medium

The coaxial cable connects all the stations in the network. You can choose either standard Ethernet 50-ohm coaxial cable or 50-ohm RG-58A/U thin coaxial cable. The transmission rate for both types is 10 Megabits per second, but they have different configuration restrictions.

Primary Cable Attachments:

- Signal Repeater Units

  Repeater Units are provided on the network to compensate for weak signals that occur after specified distances are exceeded. The network can thus be extended by placing repeaters along the cable bus at specified distances.

- Transceivers (Medium Attachment Units--MAU)

  A transceiver attaches to the network at the location of an access tap. As the name implies, the transceiver transmits and receives network signals.

  It provides required electrical isolation between the controller and the baseband cable and makes it easier to install and relocate stations and signal repeater units.

The transceiver receives power from its associated network station and performs a portion of the collision detection functions for its associated network station. It does this by listening to and timing the duration of transmitted signals and initiating the sending of the collision-presence signal when a collision is detected.

- Transceiver Cable (Attachment Unit Interface).

  A transceiver cable connects the adapter controller to a transceiver. The transceiver cable allows a station to be located some convenient distance from the network baseband cable.

  The transceiver cable contains four twisted pairs (shielded and insulated).

Baseband Adapter

This section provides a description of the hardware components that make up the Baseband Adapter. At the end of the manual, "Jumper Settings" on page 30 provides jumper settings, while "Connector Pin Assignments" on page 32 provides information on the connector pin-outs.

The adapter is a full-duplex controller which implements the data link and physical link functions of a packet-switched (Ethernet) local area network (LAN). Although the LAN media is only half-duplex, the adapter appears to the host as full-duplex; the adapter can receive during a collision back-off, can transmit immediately after receipt, and can receive its own transmissions.

The hardware functions support software control through a 32K-byte block of shared RAM on the adapter. This block is located on any 32K-byte boundary at or above 512K-bytes and is structured to establish buffers, control registers, and index functions.

A PROM is provided on the adapter that contains the 6 byte network address. The upper three bytes of this address are H'00DD00' or H'00DD01' and labels on the PROM and the back of the adapter bracket display the lower three bytes in hexadecimal.

The adapter plugs into the host RT PC I/O channel. System control signals and power requirements are provided through a connector on the bottom edge of the adapter. A 15-pin D-connector on the back of the adapter provides external access to the network transceiver.

The adapter may be plugged into an IBM 6150 system unit in any of slots 2 through 7 and into an IBM 6151 system unit in any of slots 1 through 4.

Hardware Description

The major functional blocks in the adapter are:

- Host Interface
- Transmit
- Receive
- Ethernet Data Link Control
- Buffer RAM.

The adapter services requests from the host interface and the network interface in a priority sequenced cycle.

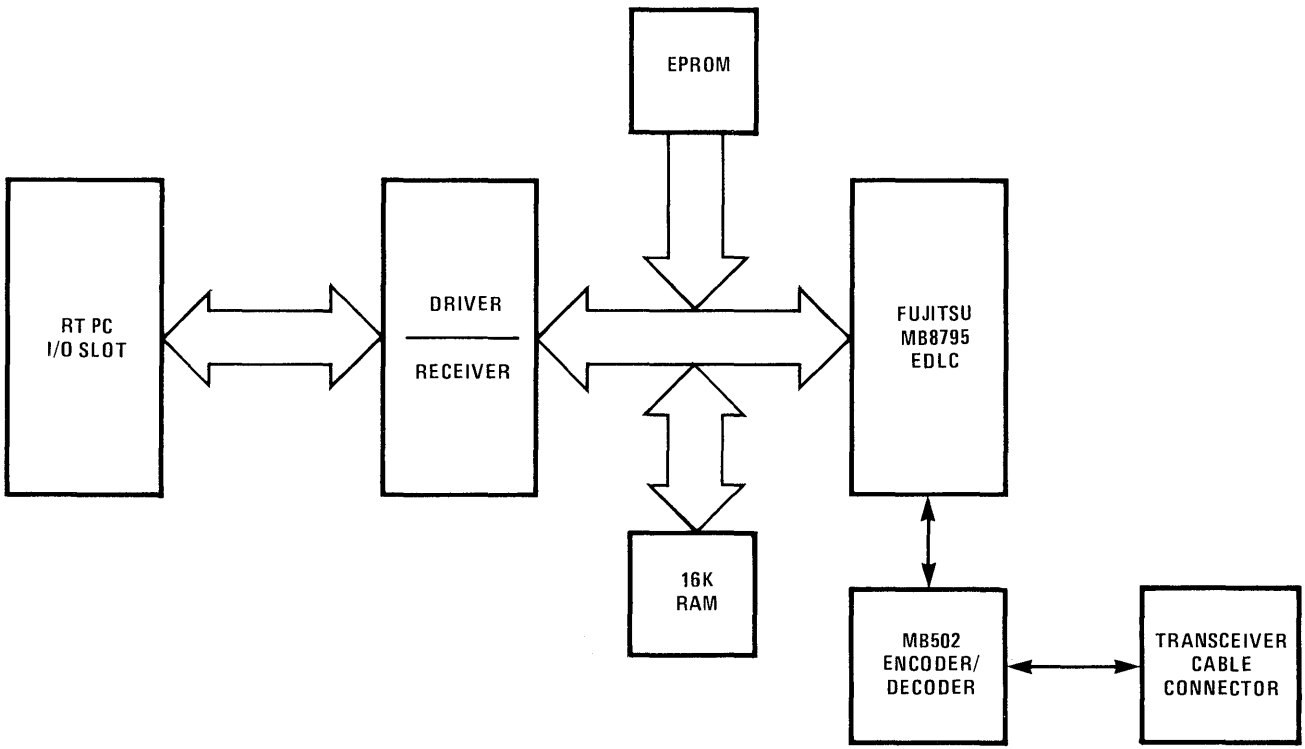


Figure 2. Adapter Data Flow Diagram

Host Interface

Data flow between the host and the network is through the adapter shared RAM. For packet transmission, data is written to the shared RAM and for packet reception, data is read from the shared RAM.

Features

- 32K-byte shared RAM interface
- Jumpers for shared RAM base address selection
- Jumpers for interrupt level selection
- Eight bit data path.

Packet Transmission

The transmit process begins with the host loading the adapter's transmit buffer with the packet to be transmitted. The transmission is initiated by reading the initiate transmit register. The adapter then clears the transmit done flag, which remains clear until the last byte in the transmit buffer has been sent. During the transmit sequence, data is transferred from the transmit buffer to a FIFO queue in the EDLC (Ethernet Data Link Controller) via on-board DMA operations, then serially to the encoder, and finally onto the network.

A retransmission occurs if the transmission fails because of a collision on the network with another transmitting station. The adapter attempts to transmit the packet a maximum of sixteen times. If the final attempt fails, the transmission is terminated and an error condition is posted.

After the last byte has been successfully transmitted (or the transmission has been terminated), the transmit done flag is set. The CRC bytes are then transmitted (unless the transmission has been terminated) and the packet transmission OK flag is set. Then if the transmission complete interrupt is enabled, the adapter interrupts the host.

The adapter supports double buffering. The addressing mechanism allows moving data into one of the transmit buffers while the other is being transmitted from. When the first transmission is complete, the second is ready to start without having to wait to fill the buffer.

Packet Reception

The receive process begins with the adapter receiving data from the LAN transceiver. As each byte of data is received, the adapter verifies that there is space for it in the receive page buffer. If the buffer is full, further incoming data is ignored until the end of the packet is encountered.

As the first six bytes are being processed, the EDLC attempts to match them to the network address range it has been programmed with. If this address recognition fails, further incoming data is ignored until the end of the packet is encountered.

The EDLC computes a Cyclic Redundancy Check (CRC) as the packet is being received. If the CRC at the end of the received packet matches the calculated CRC, the empty page pointer and packet available are updated. If the packet available interrupt is enabled, the adapter interrupts the host.

Ethernet Data Link Controller (EDLC)

The EDLC component set consists of the Fujitsu MB8795 Ethernet Data Link Controller and the Fujitsu MB502 Manchester Encoder/Decoder.

The MB8795 EDLC consists of a discrete transmitter and receiver. Each provides a small amount of asynchronous buffering and provisions for CRC, preamble, and byte parity generation or checking. The transmitter also provides contention resolution by means of binary exponential backoff.

The EDLC provides the adapter with an implementation of the data link layer of the Ethernet specification. The host communicates with the EDLC using the command and status registers allocated in the adapter shared RAM.

MB8795 EDLC Features

- Carrier Sense Multiple Access with Collision Detect (CSMA/CD)
- Forty eight bit (6-byte) address recognition
- Selectable address modes
- Binary exponential back-off
- Thirty two bit Cyclic Redundancy Check (CRC)
- Error status and signaling.

MB502 Encoder/Decoder Features

- Manchester encoding/decoding
- Carrier detect indicator
- On-board loopback
- Data rate of 10 Megabits per second.

Buffer RAM

Buffer RAM on the adapter consists of 16K-bytes of dynamic storage. 12K-bytes are allocated for receiving data and 4K-bytes are allocated for transmitting data.

The buffers are specifically allocated as follows:

Receive buffer

Comprises ninety six pages of 128 bytes each. This is a ring buffer, the last page in the buffer is logically followed by the first. Received packets are aligned at the beginning of a page and pages are concatenated as needed for packets exceeding 128 bytes.

Transmit buffers

Comprises two buffers of 2048 bytes each. All transmitted packets must be aligned in the selected buffer such that the last packet byte is in the last byte of the buffer.

Programming Interface

This section provides information necessary to write software which directly interfaces with the adapter. The following paragraphs describe the memory map, registers, control and data functions of the adapter. This section is for programmers and developers who need to understand the function of the adapter and write software for it.

Shared Memory

To communicate with the host, the adapter uses a 32K-byte block of memory. This block is structured to establish buffers, registers, and index functions. The operations that occur within these allocated structures result in orderly scheduling of events which implement the transmission and reception of data packets between stations on the Local Area Network (LAN).

Each of these memory mapped areas will be discussed in turn and are allocated as follows:

Offset	Definition
0000-1FFF	EPROM
2000-21FF	Ctrl Registers (2080-2083) Rcv Page Index (2100-215F) EDLC Registers (2180-218F)
4000-6FFF	Receive Buffer
7000-7FFF	Transmit Buffer

EPROM

The EPROM contains the adapter Ethernet address, at offset H'0010'.

Control Registers

Eight registers are mapped into the following four bytes:

Offset	R/W	Register
2080	Read Write	Initiate Transmit Transmit Start Address MS Byte
2081	Read Write	Clear Packet Available Transmit Start Address LS Byte
2082	Read Write	Interrupt and Transmit Status Interrupt Control
2083	Read Write	Empty Page Pointer and Packet Available Full Page Pointer and Interrupt Enable

Offset H'2080'

Read: Initiate Transmit (TXINIT)

Reading this register transmits the packet pointed to by the transmit start address registers. The data returned by the read is not defined. Do not read this register while a transmission is in progress.

Write: Transmit Start Address MS Byte (TSAMSB)

This register is the most significant byte of the offset. It points to the starting address of the next transmitted packet. Do not write to this register while a transmission is in progress.

Offset H'2081'

Read: Clear Packet Available (CLRPAV)

Reading this register clears the packet available bit if the EPP has not been updated by the adapter since it was last read by the host. This implies that all available packets in the receive buffer have been processed. When the receive buffer is empty, CLRPAV should be read before the full page pointer is set equal to the empty page pointer. Otherwise, the adapter assumes that the page buffer is full and will stop receiving incoming packets.

Write: Transmit Start Address LS Byte (TSALSB)

This register is the least significant byte of the offset. It points to the starting address of the next transmitted packet. Do not write to this register while a transmission is in progress.

Offset H'2082'

Read: Interrupt and Transmit Status (INTSTAT)

This register contains the status of the transmission lines and the NOT, or inverse, of the six interrupt status sources.

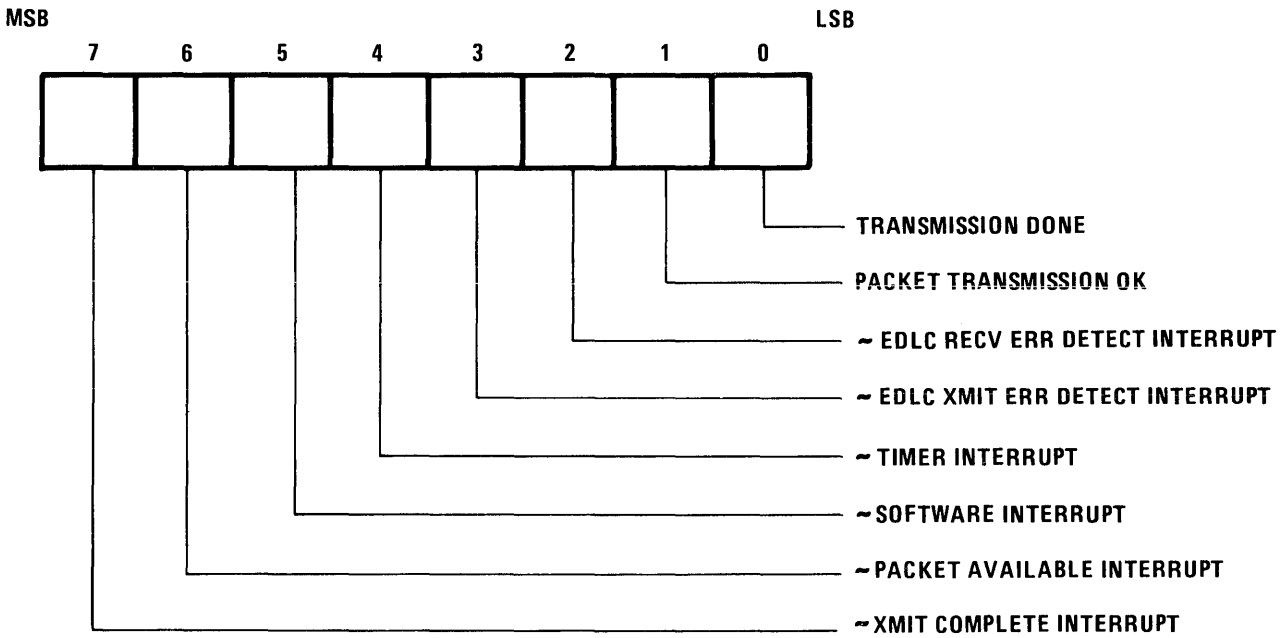


Figure 3. Offset 2082 Read

Write: Interrupt Control (INTCTL)

This register is used to enable or disable specific adapter interrupts. Each of the upper four bits enable an interrupt when set and disables the same interrupt when clear.

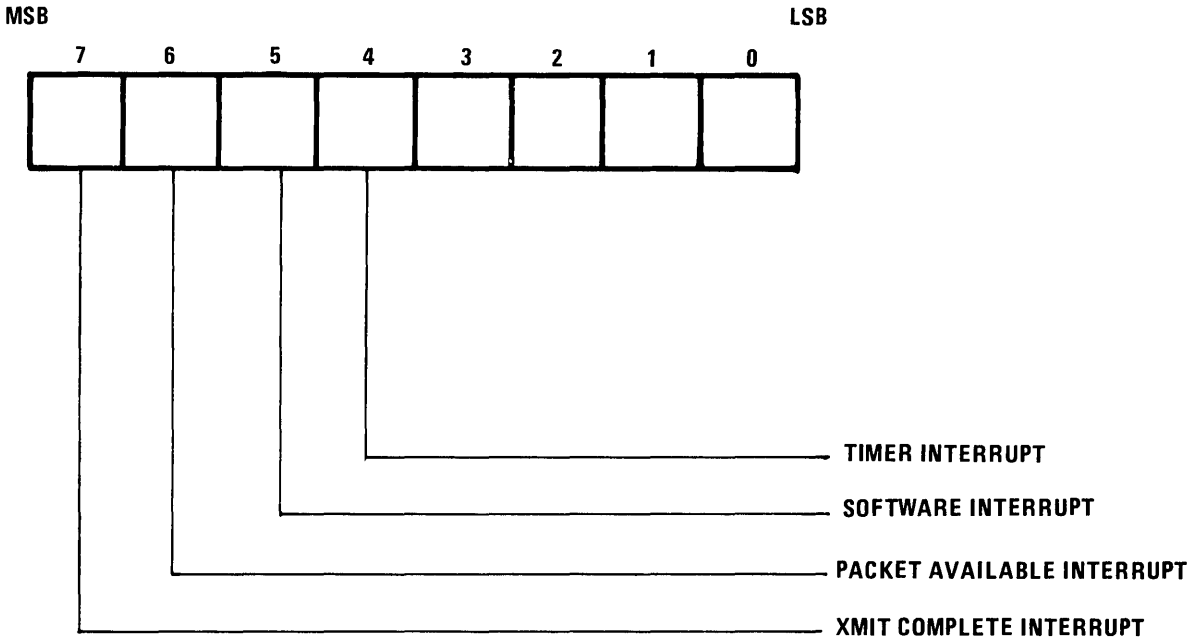


Figure 4. Offset 2082 Write

Offset H'2083'

Read: Empty Page Pointer (EPP) and Packet Available (PAV)

PAV is the high-order bit of this register and indicates that a received packet is ready to be removed from the receive buffer. This indicator is cleared by reading CLRPAV. EPP is the low-order seven bits and is an index into the receive buffer and the receive page index. The EPP points to the next free page.

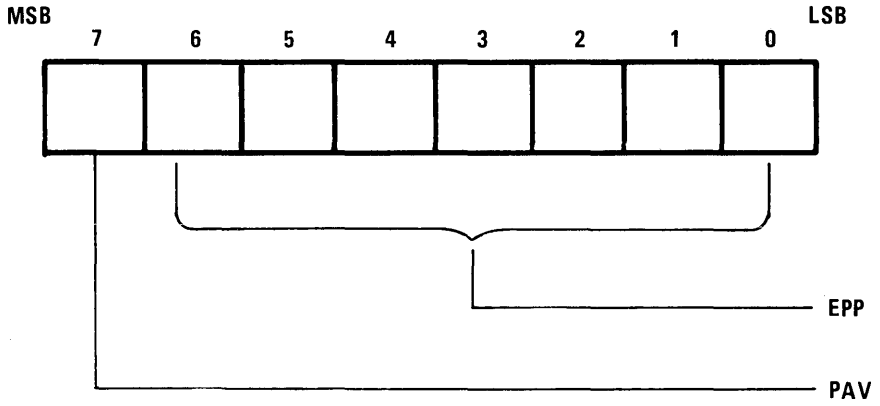


Figure 5. Offset 2083 Read

Write: Full Page Pointer (FPP) and Master Interrupt Enable (INTEN)

INTEN is the high order bit of this register. When set, it enables the jumper selected interrupt line; when cleared, it disables the line. The other seven bits are the FPP, an index into the receive buffer and the receive page index. FPP points to the next page of received data.

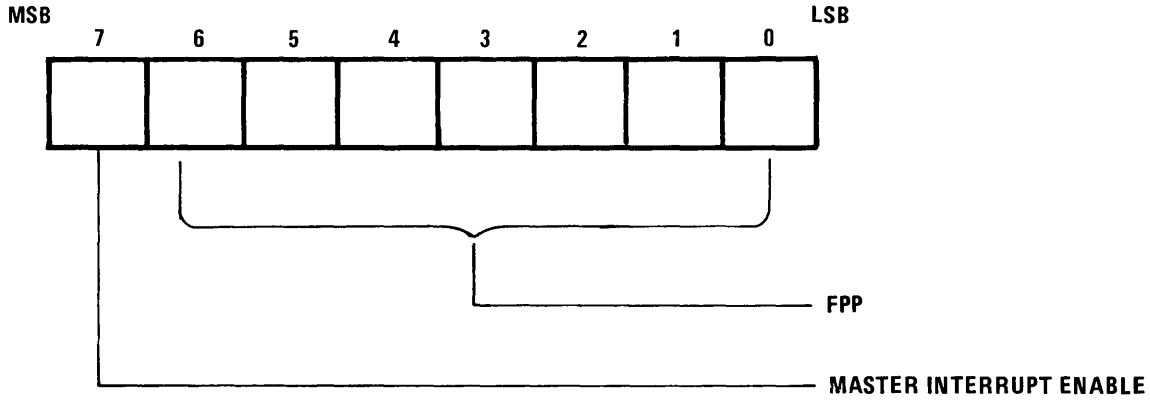


Figure 6. Offset 2083 Write

Receive Page Index Table (RPIDX)

This table is an array of 96 index bytes, one for each page in the receive buffer. The seven low-order bits of each index are the offset into the page of the last used byte of the page. This is one smaller than the number of bytes of the packet in the corresponding page. The high-order bit, when set, indicates that the corresponding page contains the end of a received packet. When this bit is clear, the corresponding page may be assumed to be full.

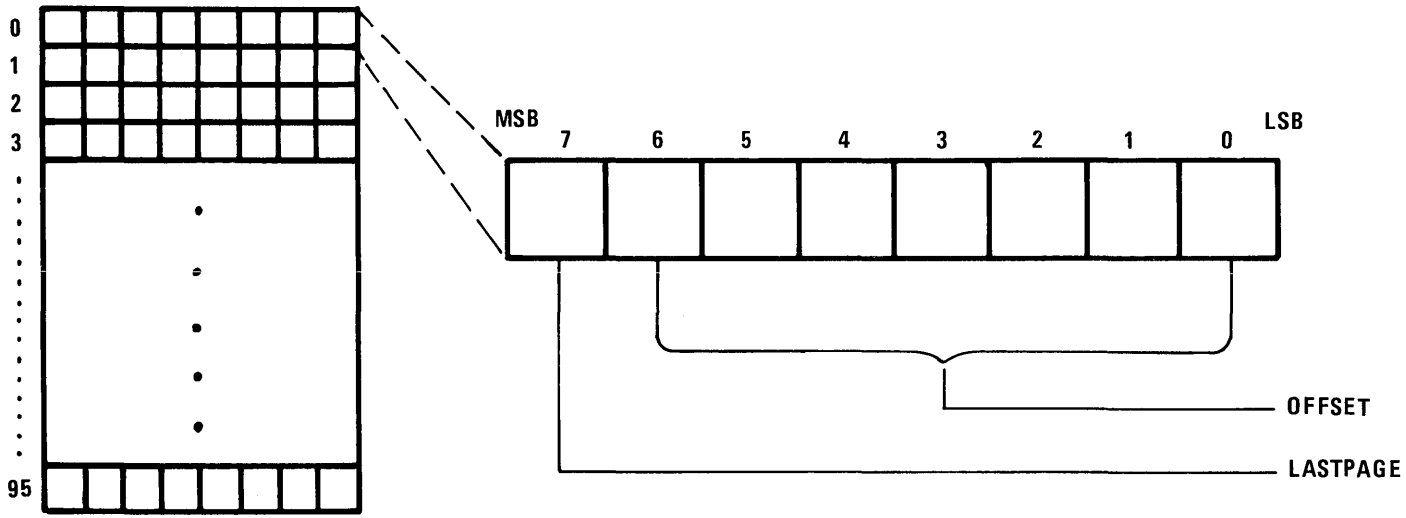


Figure 7. Receive Page Index Table

EDLC Registers

There are sixteen bytes mapped to the Ethernet Data Link Controller:

Offset	Register
2180	Transmit Status
2181	Transmit Mask
2182	Receive Status
2183	Receive Mask
2184	Transmit Mode
2185	Receive Mode
2186	EDLC Reset
2187	Transmit Data Count Low
2188	Ethernet Node ID Byte 1
2189	Ethernet Node ID Byte 2
218A	Ethernet Node ID Byte 3
218B	Ethernet Node ID Byte 4
218C	Ethernet Node ID Byte 5
218D	Ethernet Node ID Byte 6
218E	(Reserved)
218F	Transmit Data Count High

For further discussion of EDLC Registers, refer to the Initialization section.

Receive Buffer (RBUF)

This buffer consists of ninety-six pages of 128 bytes each. The RBUF is not overwritten until after its data has been removed. There is enough space for ninety-six minimum sized-packets or eight maximum sized- packets. The values in the receive page index, FPP, EPP, and PAV are all directly related to this buffer.

Transmit Buffer (TXBUF)

There are two 2K-byte buffers. Packets must be aligned at the end of the buffer where they are placed. The last byte of the packet must be in the last byte of the buffer. Only one buffer may be transmitted from at a time, but while the transmitter is sending from one, the other may be written to. TSAMSB, TSALSB, and TXINIT are directly related to these buffers.

Interrupts

There are six interrupt sources available on the adapter. Whenever any are active and INTEN is enabled, the adapter interrupts the host processor on the jumper selected interrupt line. The sources and their abbreviations are:

Interrupt Source	Abbrev
Transmission Complete	TRCINT
Packet Available	PAVINT
Software	SFTINT
Timer	TIMINT
EDLC Transmit Status	DLTINT
EDLC Receive Status	DLRINT

Enabling and Disabling

INTEN must be set to enable the adapter interrupt line. The two EDLC interrupt sources are enabled/disabled by programming the EDLC. The other interrupt sources are enabled by setting the appropriate mask bit in INTCTL and disabled by clearing the same bit.

Whenever the adapter interrupts the host processor, the status bits of the inactive interrupt source are set and the status bits of the active interrupt source are cleared in INTSTAT.

Acknowledging and Clearing

The interrupt handling routine must acknowledge the interrupt and clear it. This is done by:

1. Disabling INTEN
2. Acknowledging the interrupt
3. Enabling INTEN.

Interrupt Sources

There are six interrupt sources by which the adapter can generate a host interrupt.

TRCINT - Transmission Complete Interrupt

Indicates that the adapter is ready to transmit a packet and is cleared by disabling it in INTCTL. Notice that the adapter is ready to transmit immediately following power-on reset.

PAVINT - Packet Available Interrupt

Indicates the successful reception of a packet from the network and may be cleared by either:

- Processing the packet and clearing PAV
- Disabling PAVINT in INTCTL (which does not clear PAV).

SFTINT - Software Interrupt

Enabling SFTINT causes the adapter to interrupt the host and must be cleared by disabling it. This interrupt is user definable and might be used to indicate limited resources becoming available.

TIMINT - Timer Interrupt

Indicates that the on-board timer has expired and is cleared by disabling it. The expiration time is jumper selectable. See "Jumper Settings" on page 30. This interrupt is also user definable and might be used in certain polling schemes.

DLTINT - EDLC Transmit Interrupt

Indicates that the programmed EDLC transmission event has occurred and is acknowledged by clearing the EDLC Transmit Status Register.

DLRINT - EDLC Receive Interrupt

Indicates that the programmed EDLC reception event has occurred and is acknowledged by clearing the EDLC Receive Status Register.

Initialization

The adapter is initialized by programming the EDLC. The EDLC is programmed by moving control information into its registers. Descriptions of each of these registers are discussed below. For further information, see the Fujitsu MB8795A Technical Data Sheet.

Transmit Status Register (offset H'2180')

The lower four bits in this register indicate certain transmission events when the register is read, and clear the indicator when the same bits are written.

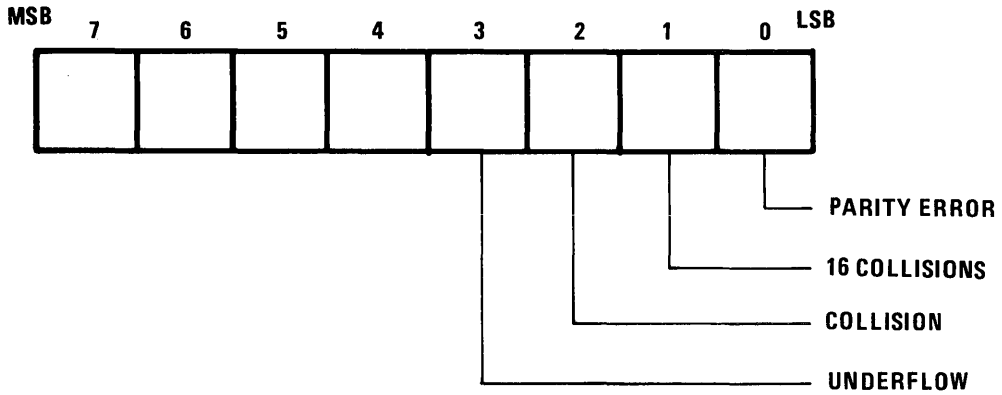


Figure 8. Transmit Status Register

Transmit Mask Register (offset H'2181')

The same values used in the transmit status register are used in this register to enable the DLTINT for that particular event.

Receive Status Register (offset H'2182')

The lower four bits in this register indicate certain reception events when the register is read, and clear the indicator when the same bits are written.

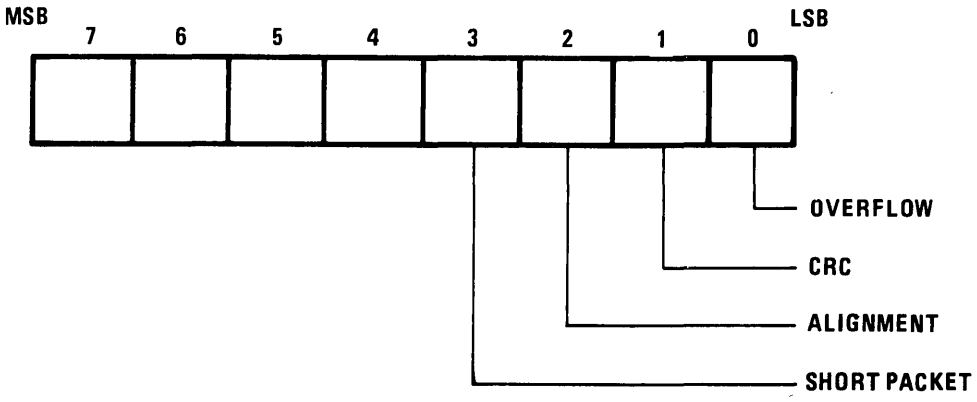


Figure 9. Receive Status Register

Receive Mask Register (offset H'2183')

The same values used in the receive status register are used in this register to enable the DLRINT for that particular event.

Transmit Mode Register (offset H'2184')

The upper half of this register contains the number of collisions that occurred during the transmission of the last packet and is cleared when the next packet transmission is started. The encoder/decoder loopback mode is enabled when an H'00' is moved to this register and an H'02' disables it.

Receive Mode Register (offset H'2185')

The range of packet addresses the EDLC will accept is defined as follows:

Bit 1	Bit 0	Definition
0	0	No addresses (no packets accepted)
0	1	Ethernet addr, Broadcasts, and limited Multicasts
1	0	Ethernet addr, Broadcasts, and all Multicasts
1	1	All addresses (promiscuous)

Limited multicasts must match the first three bytes of the packet destination address. Multicast addresses have the first bit set to 1. Broadcast addresses have all bits set to 1.

EDLC Reset (offset H'2186')

When the high-order bit is set, the EDLC is held in a reset state and is returned to an operational state when the bit is cleared. When the EDLC is taken out of reset mode, it immediately begins transmission of the packet pointed to by the transmit start address registers (TSAMSB,TSALSB).

During an initialization phase, this will probably be some random sized packet of random information. To prevent this undesirable packet from reaching the network, the encoder/decoder may be placed in loop-back mode preceding EDLC reset. This diverts the packet to the receive buffer where it may be discarded. The encoder/decoder may then be taken out of loop-back.

Transmitted Data Count Low (offset H'2187')

This is the eight least significant bits of the count of successfully transmitted bits. The six most significant bits of the count are in the transmitted data count high.

Ethernet Node ID bytes 1 to 6 (offsets H'2188' - H'218D')

These six bytes are the EDLC receiving Ethernet node ID. They are set while the EDLC is in reset mode and should be set to the six bytes of the Ethernet address in the EPROM to avoid duplicate network addresses. These registers are not readable by the host.

Transmitted Data Count High (offset H'218F')

This is the six most significant bits of the count of successfully transmitted bits. The eight least significant bits of the count are in the transmitted data count low.

Packet Reception

Incoming packets that pass EDLC address recognition and filtering are placed into the receive buffer at the start of the page indicated by EPP. EPP and PAV are only updated after the packet has been fully received. They are not updated if the packet is discarded (due to a collision or other receive errors).

Since the values of FPP and INTEN cannot be retrieved from the FPP/EPP register, they must both be maintained locally. Whenever the FPP is to be written, it must first be 'OR'ed with INTEN. INTEN and FPP must be written simultaneously.

The receive buffer is a ring buffer. Whenever EPP is incremented to point beyond the last page, it is reset to point back to the first. Incoming packets can therefore wrap around the end of the buffer. FPP must also be wrapped back to the first page of the buffer after processing of the last page is completed.

The following is a sample polling algorithm for retrieving incoming packets:

1. Wait until PAV is set.
2. Copy the receive page index byte pointed to by FPP.
3. Mask off the end of packet bit (and save it).
4. Move index+1 bytes from the page pointed to by FPP.
5. Increment the local FPP (if greater than H'5F', set to H'00').
6. If the local FPP equals EPP, read CLRPAV.
7. Write FPP (OR with INTEN first).
8. If the end of packet bit (step 3) was not set, go to step 2.
9. Repeat from step 1 when ready.

The preceding algorithm is useful when dealing with a large volume of small packets, but is not efficient when the packet size frequently exceeds the page size. A better algorithm for retrieving large packets might be as follows:

1. Wait until PAV is set.
2. Set size to zero.
3. Copy the receive page index byte pointed to by FPP.
4. Mask off the end of packet bit (and save it).
5. Add the incremented byte count to the size.
6. Increment the local FPP (if greater than H'5F', set to H'00').
7. If the local FPP equals EPP, read CLRPAV.

8. If not End Of Packet and FPP did not wrap to zero, go to 3.
9. Move size bytes from the page pointed to by FPP.
10. Write FPP (OR with INTEN first).
11. If the end of packet bit (step 3) was not set, go to step 2. Repeat from step 1 when ready.

Either algorithm is improved by making it interrupt driven.

Packet Transmission

Transmission is begun by moving an outbound packet into one of the transmit buffers and the packet start offset in the adapter shared RAM into TSAMSB and TSALSM. Following a read of TXINIT, the adapter begins transmitting the packet. If there are collisions during transmission, the EDLC automatically backs off for a random period and then attempts to retransmit. Following completion of the transmit, the adapter sets TPKTOK and TXDONE in INTSTAT.

The following is a sample transmit algorithm:

1. Wait until both TPKTOK and TXDONE are set.
2. Move the packet into the transmit buffer.
3. Move the packet offset to the transmit start address registers.
4. Read TXINIT.
5. Repeat from step 1 when ready.

This algorithm is improved by reversing the order of the first and second steps and then ensuring that the transmit buffer being written into is not the same one as the pass through the algorithm. Making the algorithm interrupt driven also improves performance.

Specifications

These cable specifications are intended as guidelines only. It is a customer responsibility to ensure that cabling components appropriate for operating an Ethernet network are used.

Ethernet Cable System Specifications

Item	Specification
Main Bus Cable Type	Ethernet 50-ohm PVC or teflon FEP coaxial cable
Connectors	N-series
Transceiver Cable	Four-stranded, twisted-pair conductors with an overall shield and insulating jacket
Data Rate	10 Megabits/sec
Maximum length of any Baseband cable segment	500 meters (0.31 miles)
Minimum distances between transceivers	2.5 meters (8.2 feet)
Maximum number of transceivers per cable segment	100 transceivers
Maximum number of stations in a network using repeaters	1024 adapters
Maximum length of transceiver cable	50 meters (164 feet)

Ethernet Cable Mechanical Requirements

The mechanical requirements for the Ethernet cable are as follows:

Item	Specification
Center Conductor	Solid copper, 2.17 mm dia + 0.0127 (0.0855 inches dia + 0.0005)
Core Dielectric	Foam
Inside diameter of innermost shield	6.15 mm (0.242 inches) min.
External shield	90% + tinned copper braid, with an outside diameter of 8.28 mm + 0.178 mm (0.326 inches + 0.007 in.)
Jacket's outside	9.27 mm (0.365 inches) min, 10.54 mm (0.415 inches) max.
Concentricity	0.51 (0.020 inches) O.C.

Cable concentricity must be such that the center of the core conductor is within 0.51 mm (0.020 inches) of its ideal concentric position with respect to the jacket.

Thin Coaxial Cable System Specifications

Item	Specification
Main bus cable type	RG-58A/U, 50-ohm coaxial cable
Connectors	BNC type
Transceiver cable type	Four-stranded, shielded twist-pair conductors with an overall shield and insulating jacket
Data rate	10 Megabits/sec
Maximum length of any thin coaxial cable segment	200 meters (656 feet)
Minimum distance between transceivers	1 meter (3.3 feet)
Maximum number of transceivers per cable segment	30 transceivers
Maximum transceiver cable length from adapter to transceiver	50 meters (164 feet)

Jumper Settings

Interrupt Level Select

Level	W9 Jumper
IRQ3	IR3
IRQ4	IR4
IRQ5	IR5
IRQ6	IR6
IRQ7	IR7
IRQ9	IR9 (IR2)

Interrupt Request Rate

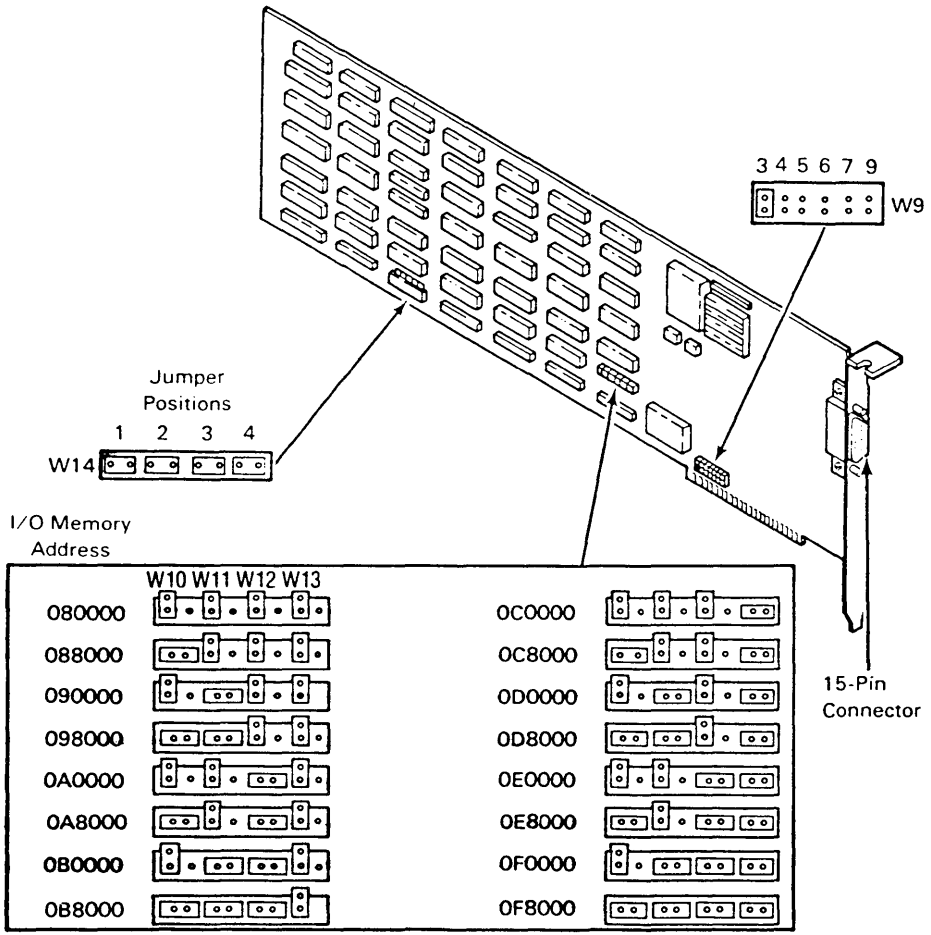
Rate	W14 Jumper
9.1 ms	Position 1
18.3 ms	Position 2
36.6 ms	Position 3
73.2 ms	Position 4

Set the jumpers as follows:

W9 Set to the interrupt level desired.

W10 - W13 Set for the 32K-byte block of memory desired.

W14 Sets the interrupt request rate.



Connector Pin Assignments

Pin	Signal	Description
Shield		Logic and frame ground
2	Col+	Collision Detect high
3	Tx Data+	Transmit Data high
4	Reserved	
5	Rcv Data+	Receive Data high
6	Power Rtn	Transceiver Power return
7	Reserved	
8	Reserved	
9	Col-	Collision Detect low
10	Tx Data-	Transmit Data low
11	Reserved	
12	Rcv Data-	Receive Data low
13	Power	+12 volts to transceiver
14	Reserved	
15	Reserved	

Figure 10. D - Connector Pin Assignments

I/O Pin	Signal Name		
A01	n/c	B01	Gnd
A02	Data 7	B02	+Reset
A03	Data 6	B03	+5
A04	Data 5	B04	IRQ 9
A05	Data 4	B05	-5
A06	Data 3	B06	n/c
A07	Data 2	B07	-12
A08	Data 1	B08	n/c
A09	Data 0	B09	+12
A10	+I/O CH RDY	B10	Gnd
A11	n/c	B11	-SMEMW
A12	SA19	B12	-SMEMR
A13	SA18	B13	n/c
A14	SA17	B14	n/c
A15	SA16	B15	n/c
A16	SA25	B16	n/c
A17	SA14	B17	n/c
A18	SA13	B18	n/c
A19	SA12	B19	-Refresh
A20	SA11	B20	n/c
A21	SA10	B21	IRQ7
A22	SA09	B22	IRQ6
A23	SA08	B23	IRQ5
A24	SA07	B24	IRQ4
A25	SA06	B25	IRQ3
A26	SA05	B26	n/c
A27	SA04	B27	n/c
A28	SA03	B28	n/c
A29	SA02	B29	+5
A30	SA01	B30	Osc
A31	SA00	B31	Gnd

Figure 11. 62 Pin Connector Pin Assignments

IBM

Personal Computer Hardware Reference Library

Multiprotocol Adapter

Contents

Description

The IBM Multiprotocol Adapter is a communications adapter that is programmable from the system to support asynchronous, character synchronous, and bit synchronous protocols using the RS232C interface. The second RS232C port may be reconfigured as an RS366 interface to support autocalling. An X.21 interface is supported using any synchronous protocol.

This adapter is an 8-bit device in PIO (Program Input/Output) mode and a 16-bit alternate controller in DMA (Direct Memory Access) mode. This means the adapter is capable of transferring data directly to and from system memory via DMA by driving the I/O channel with the appropriate address, data, and control signals. It receives system commands and returns adapter status by responding to I/O read and I/O write operations generated by the system.

The functions performed by the adapter depends on both the user provided adapter microcode and the adapter device driver.

The adapter provides all its own clocking thus not requiring any system clocking support.

This adapter plugs into the I/O channel within the RT PC work station from which it derives all system signals and power. Connectors on the board edge supply all the signals necessary to operate various combinations of one or two RS232C ports and/or a single X.21 network interface. Additionally, support of an autocall device using the RS366 interface can be selected.

Functional Block Diagram

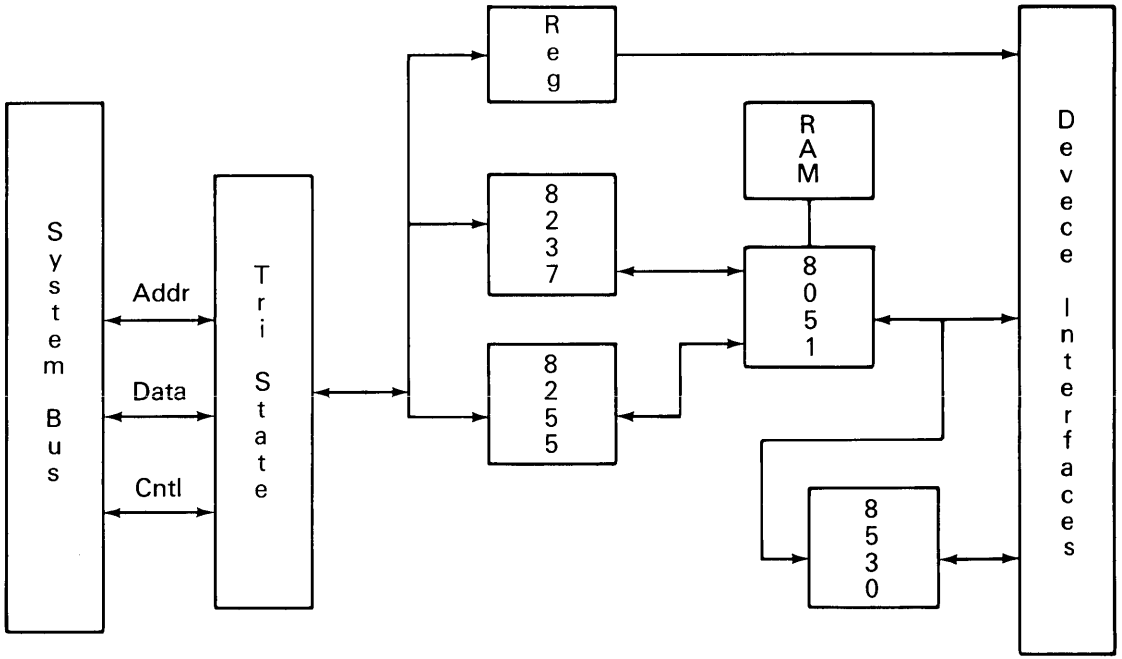


Figure 1. Multiprotocol Adapter Block Diagram

Adapter Configurations Supported

The table below describes the valid adapter operating configurations.

Configuration	Port 1	Port 2	X.21 Port
1	RS232C	Idle	Idle
2	Idle	RS232C	Idle
3	RS232C	Idle	Active
4	Idle	RS232C	Active
5	RS232C	RS232C	Idle
6	RS232C	RS366	Idle
7	Idle	Idle	Active

Figure 2. Adapter Configurations

Configuration Jumpers

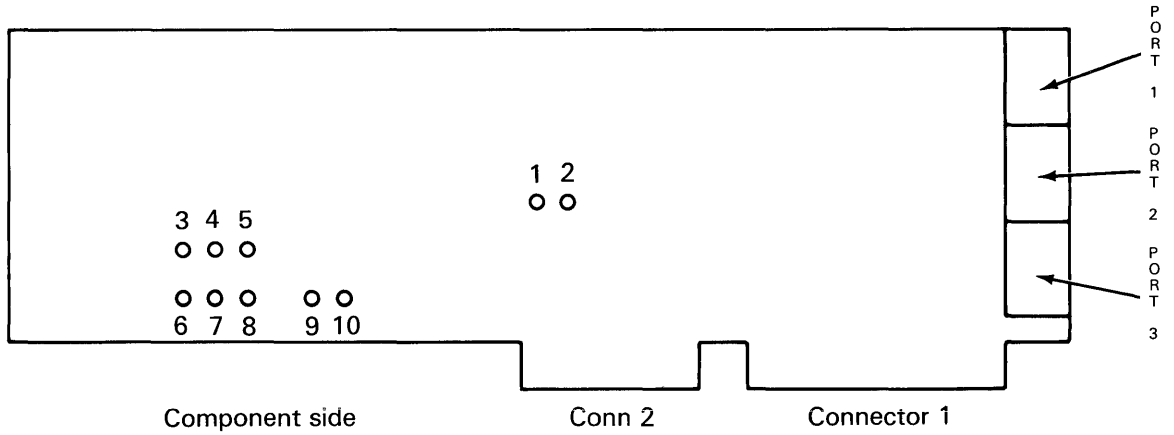


Figure 3. Configuration Jumper Pins

The adapter can be jumpered for system DMA channel 1 or 5, interrupt level 10 or 11, and one of two I/O address blocks. The following table shows which pairs of pins should be jumpered to provide the various configurations.

Pin Pair	Jumper On	Jumper Off
1 - 2	System DMA Channel 1	System DMA Channel 5
3 - 4	Interrupt Level 11	4 - 5 Must be off
4 - 5	Interrupt Level 10	3 - 4 Must be off
6 - 7	Interrupt Level 11	7 - 8 Must be off
7 - 8	Interrupt Level 10	6 - 7 Must be off
9 - 10	Address Block 05XX	Address Block 09XX

Figure 4. Jumper Configuration Table

Interrupts

The adapter supports interrupt sharing on interrupt level 10 or 11, and uses system DMA channel 1 or 5 (both jumperable). An address jumper allows either of two I/O address blocks to be decoded. This provision allows two adapters to be used concurrently in an RT PC system.

External Connector Description

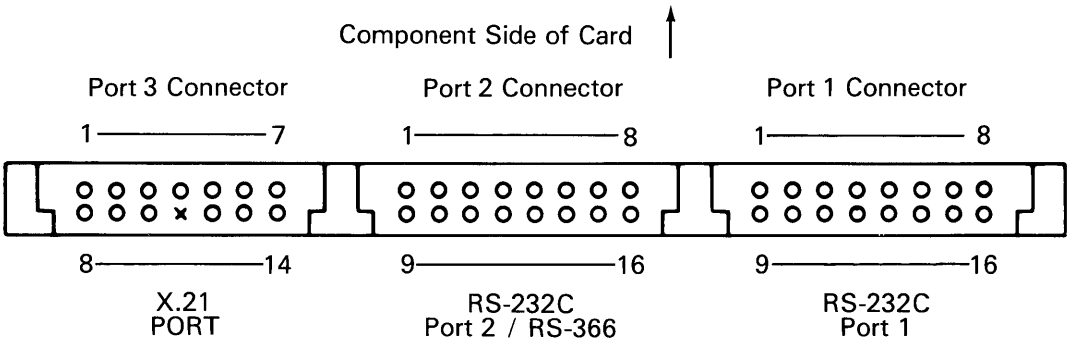


Figure 5. External Connector

Connection to the adapter board is through a three section AMP-MODU connector. The Port 1 position (RS232C Port 1) is 2x8, the Port 2 position (RS232C Port 2 or RS366) is 2x8, and the port 3 position (X.21) is 2x7. The X.21 cable is keyed to prohibit plugging into either of the first two positions. The two RS232C cables are identical but different from the RS366 cable. These cables can be swapped, which results in an interface error but no electrical damage. The connector is shown from the device side of the board. Notice that all three cables can be plugged simultaneously but there are restrictions on which combinations can be active concurrently.

Addressing Map

The following table shows the adapter I/O addresses which are accessible to the system. There is no on-board memory accessible from the system interface.

Register	Primary Addr (Hex)	Alternate Addr (Hex)
8237 DMA Controller	0510-051F	0910-091F
8255 PPI Module	0520-0523	0920-0923
DMA Addr Extension	0524-0527	0924-0927
Adapter HW Reset (See note)	0528	0928
Adapter Echo/Status Register	052B	092B
Port 1 Control Register 1	052C	092C
Port 1 Control Register 2	052D	092D
Port 2 Control Register 1	052E	092E
Port 2 Control Register 2	052F	092F
Reset Interrupt (Level 10)	X6F2	X6F2
Reset Interrupt (Level 11)	X6F3	X6F3

Figure 6. System Address Assignments

Notes:

1. Adapter reset is accomplished by software executing an I/O write to address H'0528' or H'0928' with data bit 0 a **1** followed by another write to the same address with data bit 0 a **0**. A 2 micro-second wait is necessary between the two write operations to generate a sufficiently long reset pulse.
2. Programs that perform consecutive I/O operations to address ranges H'0X10'to H'0X1F' or H'0X20' to H'0X23' must wait at least one microsecond between two operations.

Board Enable/Disable Controls

System Bus Driver Enable

The board provides a single control bit to allow the system to globally enable and disable system interface drivers. This bit is writeable from the system and is reset to the disabled state by a system POR or software reset.

Interrupt Enable

The board provides a single control bit to allow the system to enable and disable system interrupts. This bit is writeable and readable from the system. It is reset to the disabled state by a system POR or software reset.

Note: The system drivers must be enabled before interrupts can be generated to the system.

RS232C Port 1 Driver Enable

The board provides a single control bit to allow the system to enable and disable the RS232C Port 1 drivers. This bit is writeable but not readable from the system. It is reset to the disabled state by a system POR or software reset.

RS232C Port 2/RS366 Driver Enable

The board provides a single control bit to allow the system to enable and disable the RS232C Port 2/RS366 drivers. This bit is writeable but not readable from the system. It is reset to the disabled state by a system POR or software reset.

X.21 Driver/Receiver Enable

The board provides a single control bit to allow the system to enable and disable the X.21 drivers and receivers. This bit is writeable but not readable from the system interface. It is reset to the disabled state by a system POR or software reset.

Internal Programming Interface Description

8051 Memory Addressing Maps

The Multiprotocol Adapter contains a single 8K region of static RAM memory. This RAM memory can be used by the user's microcode as either program or data memory. The method of access by the 8051 varies slightly depending on the application of this memory. The following figures show the memory address spaces presented to the adapter's 8051 processor.

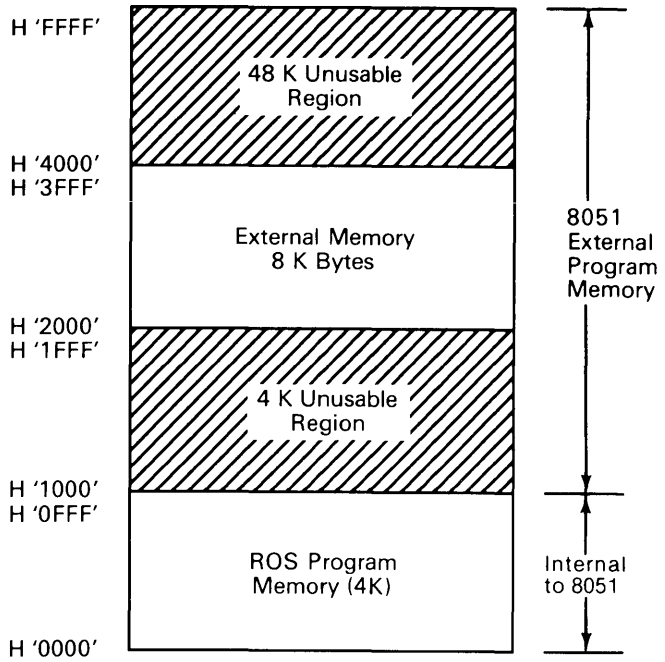


Figure 7. 8051 Program Memory Map

The external program memory map can be seen as a single 8K memory region that appears at absolute address H'2000' . The lowest order 4K region of memory contains the processor's internal 4K-ROS program memory.

External memory is automatically accessed by the 8051 for program addresses above 4K (hex address 0FFF). Microcode resident in external RAM memory is executed by simply branching to the appropriate external memory address following the completion of the RAM IPL process.

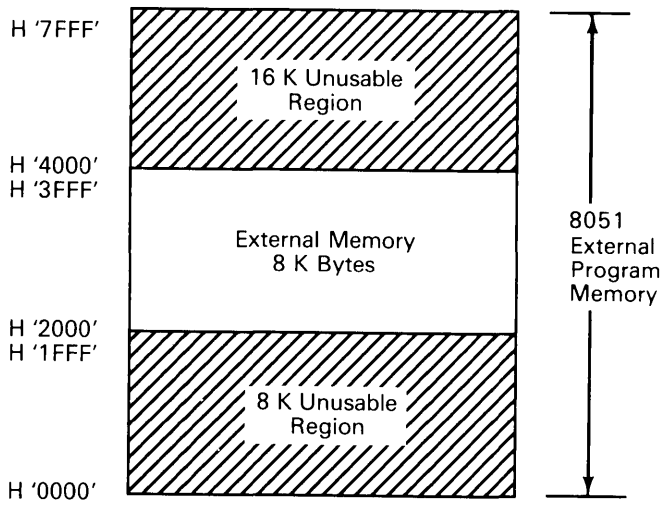


Figure 8. 8051 Data Memory Map

The external data memory map can be seen as a single 8K memory region that appears at absolute address H'2000' . This data is accessed by initializing the 8051's DPTR register to the appropriate address and executing the processor's MOVX instruction. Notice that there is a single 8K-RAM region on the adapter that is intended for both program and external data memory (if any). It is the responsibility of the user's microcode to ensure that external data regions do not unintentionally overlay external program memory.

Notice that for memory addresses in the H'2000' to H'3FFF' range that data access addressing is the same as for program execution addressing.

8051 Resident I/O

8051 I/O Port 1

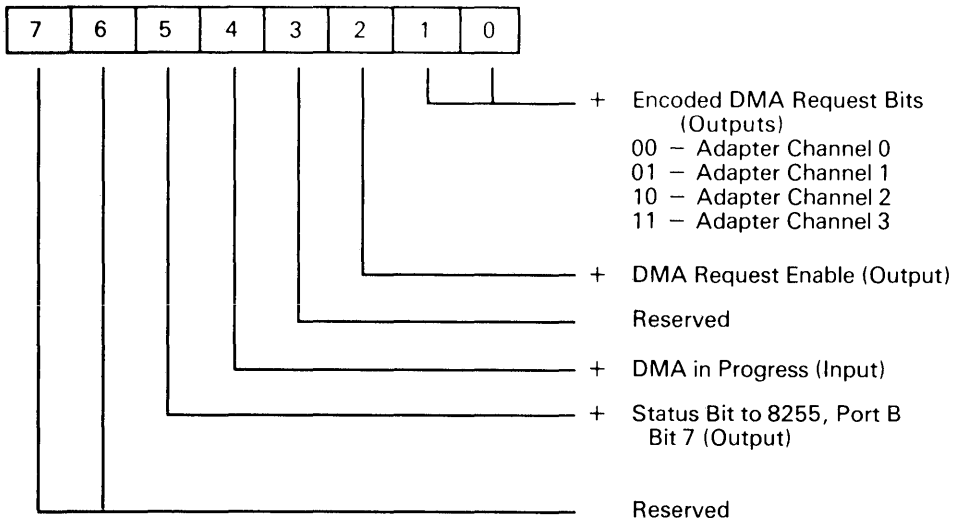


Figure 9. 8051 Port 1 Bits

The figure above defines the I/O status bits found in the 8051 processor module port 1.

8051 I/O Port 3

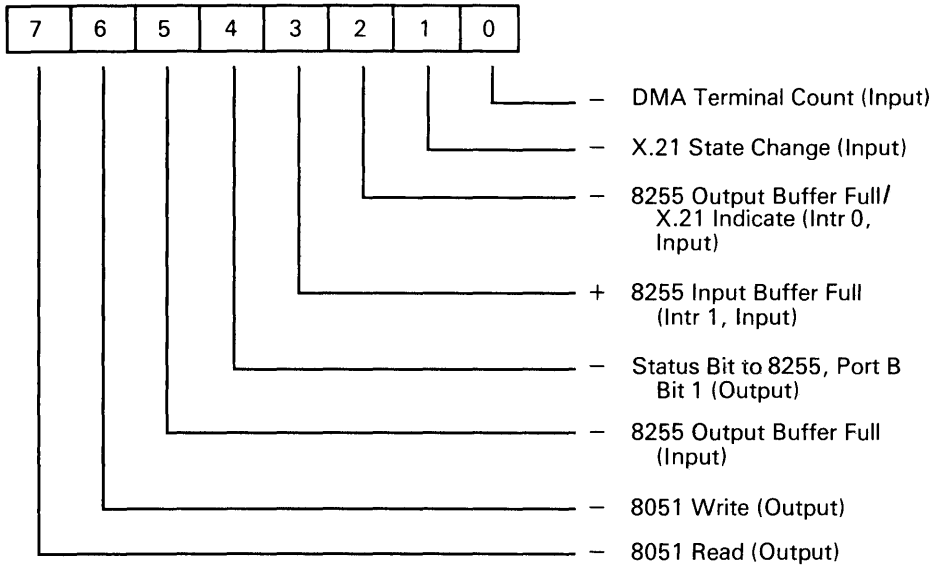


Figure 10. 8051 Port 1 Bits

The figure above defines the I/O status bits found in the 8051 processor module port 3.

8051 External I/O Address Map

The following figure shows the I/O address map as seen by the adapter's 8051 processor.

Device	I/O Address	Access Modes
Low order DMA data register	H'80XX'	Read/Write
High order DMA data register	H'88XX'	Read/Write
System Interface Port	H'90XX'	Read/Write
Communications Cntlr	H'98X0' - H'98X3'	Read/Write
Port 1 Intfc. Inputs	H'A0XX' or H'B0XX'	Read Only
Port 2 Intfc. Inputs	H'C0XX' or H'D0XX'	Read Only

Figure 11. 8051 I/O Address Assignments

8051 I/O operations are accomplished by initializing the 8051's DPTR register to the appropriate I/O address and executing the processor's MOVX instruction.

Communication Controller (8530)

The 8530 controller is used in a poll mode allowing the 8051 to read status and determine if service is required. The 8530 has two independent channels with associated read and write registers that allow the 8051 to control all necessary functions. There are shared registers to reduce the amount of interrogation required by the 8051. The following is a list of all 8530 internal registers. For a detailed description of each register please reference the ZILOG Z8030/Z8530 Serial Communications Controller Technical Manual.

Note: These registers are directly accessible only by the adapter's 8051 processor.

Register	Description	Channel	Ptr Address
Write R0	Command/Pointer Register	A and B	X0
Read R0	Xmit/Rcv Buf Stat, Ext Stat	A and B	X0
Write R1	Xmit/Rcv Intr, Xfer Mode	A and B	X1

Figure 12 (Part 1 of 2). 8530 Internal Registers

Register	Description	Channel	Ptr Address
Read R1	Special Rcv Condition Stat	A and B	X1
Write R2	Interrupt Vector	Common	X2
Read R2	Interrupt Vector	A and B	X2
Write R3	Rcv Parameters and Control	Common	X3
Read R3	Interrupt Pending Register	A and B	X3
Write R4	Xmit/Rcv Parameters, Modes	A and B	X4
Write R5	Xmit Parameters and Control	A and B	X5
Write R6	Sync Char or S/HDLC Addr	A and B	X6
Write R7	Sync Char or S/HDLC Addr	A and B	X7
Write R8	Transmit Buffer	A and B	X8
Read R8	Receive Data Register	A and B	X8
Write R9	Master Interrupt Control	Common	X9
Write R10	Xmit/Rcv Control Bits	A and B	XA
Read R10	Miscellaneous Status Bits	A and B	XA
Write R11	Clock Mode Control	A and B	XB
Write R12	Low Byte BRG Time Constant	A and B	XC
Read R12	Low Byte BRG Time Constant	A and B	XC
Write R13	High Byte BRG Time Constant	A and B	XD
Read R13	High Byte BRG Time Constant	A and B	XD
Write R14	Misc. Control Register	A and B	XE
Write R15	Ext Stat/Interrupt Control	A and B	XF
Read R15	Ext Stat/Interrupt Control	A and B	XF

Figure 12 (Part 2 of 2). 8530 Internal Registers

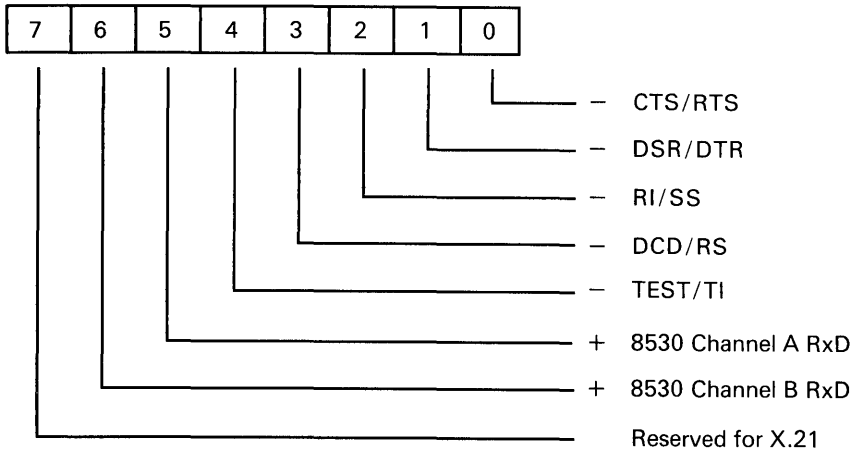
The 8530 uses the command register as an address pointer to allow the 8051 to access the other internal 8530 registers. To access any of these internal registers, the pointer register must first be written with the appropriate address. There are only three address bits used directly for the

addressing. The registers with addresses of 8 through F must be accessed using the 8530 point high command.

The following functional capabilities of the Zilog 8530 are not supported in this adapter.

1. DMA support: DMA is controlled by the adapter 8051 processor rather than by 8530 DMA controls.
2. Interrupts: 8530 interrupts are not supported. The adapter processor polls the 8530 to determine service needs.
3. Modem controls: RS232C modem outputs are not driven from the 8530 modem output bits, with the following exception. The adapter processor can drive the RS232C 'Request to Send' (RTS) output via bit 1 in the 8530 'Write Register 5'. This output is logically ORed with the RTS signal that can alternately be driven from bit 0 of either interface control register 1 or interface control register 3 (depending on port). This provides the adapter processor with the capability to initiate transmissions without device driver intervention, if desired.

Port 1 Input Modem Register

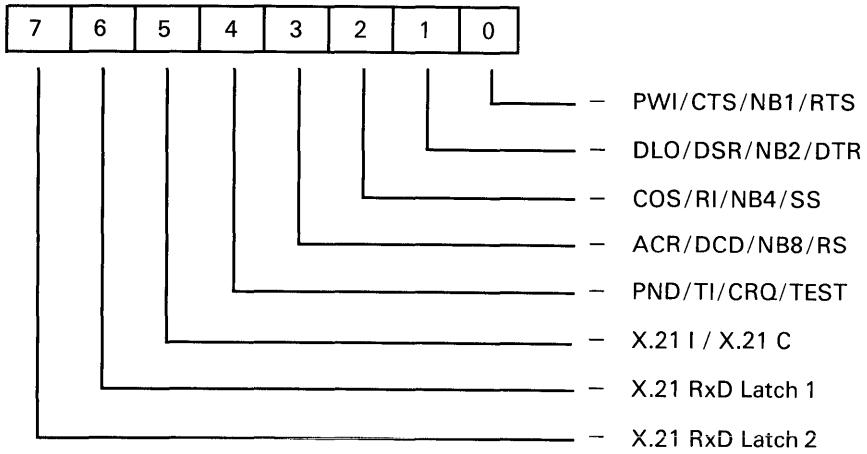


The Port 1 modem input register can only be read by the 8051. It contains the status of the control lines from the DCE to the DTE. These registers are updated on the leading edge of the 8051 read pulse and should be debounced by the user supplied microcode program.

The register inputs are multiplexed for diagnostic reasons. If the adapter is in driver or receiver wrap mode, the inputs to the register are the control lines from the adapter to the DCE (such as RTS, DTR). This allows the hardware control register bits to be tested on board.

The status bits received from the modem are negative true (0 = on) when viewed in either port input register.

Port 2 Input Modem Register



The Port 2 modem input register is identical to the port 1 register except it includes the RS366 and X.21 control signals.

Note that the control signals for RS232C Port 2, RS366, and X.21 appear multiplexed but a single control bit drives each wrapped bit. The interface driver that gets driven is controlled by adapter mode select bits in system control registers.

The register inputs are multiplexed for diagnostic reasons. If the adapter is in driver/receiver wrap mode, the inputs to the register are the control lines from the adapter to the DCE (RTS, DTR). This tests the hardware control register bits on-board.

X.21 RxD latches 1 and 2 contain the last 2 receive data bits. The bits are valid only if the X.21 PAL clock is enabled. If these bits are sampled during an X.21 PAL interrupt, they can be interpreted according to the following table.

Latch 2	Latch 1	
0	0	Last 16 receive data bits were all zeros.
0	1	Last 16 receive data bits were alternating ones and zeros.
1	0	Last 16 receive data bits were alternating ones and zeros.
1	1	Last 16 receive data bits were all ones.

Figure 13. X.21 RxD Latch Bits

8051 DMA Request Interface

The 8051 controls all DMA requests to the 8237. The system processor tells the 8051 (via 'Operating' mode commands) which DMA channel to use for a given transfer. The 8051 writes the encoded channel value to the DMA request encode bits and then sets the DMA request enable bit which generates a DMA request to the 8237. The DMA request line is disabled by the DMA acknowledge (DACK) that is returned. The DACK sets a latch that can be read by the 8051 to determine when the transfer has been completed. The 8051 can also read a latch that is set by a Terminal Count (TC) pulse (from the 8237) which allows the 8051 to detect when a given DMA channel has expired. After this, the 8051 resets the DMA request enable bit which will reset the TC latch and the DACK back latch and leave DMA request hardware ready for the next transfer request.

Adapter Clocking Options

RS232C External (DCE) Clocking

External clocking implies the DCE is providing the DTE with the necessary clocking signals for both transmit and receive. The adapter supports this type of clocking when the hardware is initialized as follows:

- The 'use RS232C port 1 modem receive clock' and 'use RS232C port 1 modem transmit clock' bits in interface control register 2 must be set to 1. These control bits gate the two clock signals to the 8530 module.
- The 8530 must be initialized to get its transmit clock from the TRxCA pin and its receive clock from the RTxCA pin. Please refer to the 8530 Technical Manual for other register initialization required to support this type of clocking.

Note: RS232C port 2 has similar initialization for this mode of operation.

RS232C Internal (DTE or BMC) Clocking

Internal clocking implies that the DTE is providing its own clocking for both transmitting and receiving. The adapter supports this type of clocking when the hardware is initialized as follows:

- The 'Use 1X Clock for BMC Clocking for RS232C Port 1' bit in interface control register 2 must be set to 1. This control bit enables on board circuitry to divide the the 32x clock signal driven by the 8530 on the TRxCA pin to produce a 1x clock signal. This 1x clock signal is used by the transmit clock. The receive clock is generated from the receive data stream using logic internal to the 8530.
- The 8530 must be initialized to have the baud rate generator (BRG) produce a clock 32 times the line baud rate.
- The digital phase locked loop (DPLL) should be set up to get its input clock from the BRG.
- The receive clock should be set up to come from the DPLL receive clock output.

- The TRxCA pin should be configured as an output and be tied to the BRG output.
- The transmit clock should be set up to come from the RTxCA pin.

Notes:

1. In this mode, three 8530 commands must be issued to 8530 WR14 to guarantee proper operation of the DPLL. They are:
   a. Set NRZI mode
   b. Set source = BR generator
   c. Enter search mode.
2. RS232C port 2 has similar initialization for this mode of operation.

X.21 Clocking

X.21 implies that the DCE is providing clocking for both transmitting and receiving. The adapter supports this type of clocking when the hardware is initialized as follows:

- The 'Enable X.21 Drivers and Receivers' bit in interface control register 2 must be set to 1.
- The 'Select Channel A (or B, but not both) for X.21' bit in interface control register 1 must be set to 1.
- The 'Enable X.21 PAL Clock' bit in interface control register 3 must be set to 1.
- The 8530 must be initialized to obtain both the transmit and receive clocks from the RTxCA pin (or RTxCB).

Providing a Clock to the DCE

The adapter has the capability for providing a 1x clock to the DCE. The adapter supports this type of clocking when the hardware is initialized as follows:

- The 'Enable Port 1 RS232C Drivers' bit and the 'Provide Transmit Clock to RS232C Port 1' bits in interface control register 2 must be set to 1.
- The 8530 must be initialized to have the BRG provide a 32x clock to the TRxCA pin and TRxCA must be configured as an output.

Note: RS232C port 2 has similar initialization for this mode of operation.

8530 Channel A Clock to 8530 Channel B

The adapter has the capability of using the BRG of 8530 channel A to provide a clock to channel B. The adapter supports this type of clocking when the hardware is initialized as follows:

- The 'Wrap 8530 Channel A Clock to Channel B' and the 'Provide Transmit Clock to RS232C Port 1' bit in interface control register 2 must be set to one.
- The 8530 channel A must be initialized to have the BRG provide a 1x clock to the TRxCA pin and TRxCA must be configured as an output.

- The 8530 channel B must be initialized to have the channel A clock as an input on the RTxCB pin.

8530 Channel B to 8530 Channel A

The adapter has the capability of using the BRG of 8530 channel B to provide a clock to channel A. The adapter supports this type of clocking when the hardware is initialized as follows:

- The 'Wrap 8530 Channel B Clock to Channel A' and the 'Provide Transmit Clock to RS232C Port 1' bit in interface control register 4 must be set to one.
- The 8530 channel B must be initialized to have the BRG provide a 1x clock to the TRxCB pin and TRxCB must be configured as an output.
- The 8530 channel A must be initialized to have the channel B clock as an input on the RTxCA pin.

RS232C Signals

Request to Send (RTS, Output)

This signal conditions the local DCE for data transmission and, on a half-duplex circuit, to control the direction of the data transmission for the local DCE. This signal is active high.

Data Terminal Ready (DTR, Output)

This signal controls switching of the DCE to the communication channel. The assertion of this signal prepares the DCE for connecting to the communications channel and maintains the connection established by external means. This signal is active high.

Rate Select (RS, Output)

This signal selects between two data signaling rates in dual data rate synchronous DCEs or between two ranges of data signaling rates in dual range nonsynchronous DCEs. This signal is active high.

Note: The EIA RS-232C Standard (August 1969) allows either of two functions (interchange circuits CH or CI) to use pin 23 of the 25-pin DTE/DCE interface connector. The RT PC Multiprotocol Adapter assigns the *Data Signal Rate Selector (DTE Source)* function (circuit CH) to pin 23. If your modem assigns the *Data Signal Rate Selector (DCE Source)* function (circuit CI) to pin 23, a functional incompatibility will exist between the Multiprotocol Adapter and your modem for this pin. However, hazards to personnel or equipment do not exist. See your modem vendor for additional information or assistance.

Select Standby (SS, Output)
This signal controls the activation of a backup switched network path available on some private (leased) line DCE facilities. The backup provides continued communications during a line failure. This signal is active high.

Test (Output)
This signal places the DCE in diagnostic test mode. This signal is active high.

Transmit Clock (TxCO, Output)
This signal supplies a transmit clock to a modem requiring external clocking.

Transmit Data (TxD, Output)
This signal carries the serial data stream from the communications adapter data outputs to the DCE. This signal is active high.

Clear to Send (CTS, Input)
This signal indicates that the DCE is ready for DTE data transmission. This signal is active high.

Data Set Ready (DSR, Input)
This signal indicates that the DCE is connected to a communications channel and that the DCE is not in test, talk, or dial mode. This signal is active high.

Ring Indicate (RI, Input)
This signal indicates the detection of a ring signal by the DCE and is used for automatic answering situations. This signal is active high.

Data Carrier Detected (DCD, Input)
This signal indicates that the DCE has detected a valid carrier. This signal is active high.

Test Indicate (TI, Input)
This signal indicates to the DTE that the DCE has entered diagnostic test mode. This signal is active high.

Receive Clock (RxCI, Input)
This signal clocks the receive data into the communications adapter for de-serialization.

Transmit Clock, DCE SOURCE (TRXI, Input)
This signal provides the DTE a clock for shifting the transmit data out of the serialization buffer.

Receive Data (RxD, Input)
This signal carries the serial data stream from the DCE to the DTE receive buffer. This signal is active high.

RS366 Signals

Call Request (CRQ, Output)
This signal requests the ACU (Automatic Calling Unit) to originate a call. This signal is active high.

Digit Present (DPR, Output)
This signal indicates to the ACU that it may read the code combination on the digit signal circuits (NB 1-4). This signal is active high.

RS366 DIAG (Output)
This signal is used in diagnostic mode only during an external wrap test to check out the RS366 drivers and receivers.

NB1 (NB1, Output)
This signal is the low order bit in the code combination. This signal is active high.

NB2 (NB2, Output)
This signal is the second order bit in the code combination. This signal is active high.

NB4 (NB4, Output)
This signal is the third order bit in the code combination. This signal is active high.

NB8 (NB8, Output)
This signal is the high order bit in the code combination. This signal is active high.

Power Indicate (PWI, Input)
This signal is an indication to the DTE that the ACU is powered on. This signal is active high.

Data Line Occupied (DLO, Input)
This signal indicates to the DTE that the communications channel is in use. This signal is active high.

Call Origination Status (COS, Input)
This signal indicates to the DTE the status of the call procedure. The ACU activates this line when the call has been successfully completed. This signal is active high.

Abandon Call and Retry (ACR, Input)
This signal indicates to the DTE that the present calling procedures is likely to fail and that the call procedure should be re-initiated. This signal is active high.

Present Next Digit (PND, Input)
This signal indicates to the DTE that the ACU is ready to accept another digit. This signal is active high.

X.21 Signals

Transmit Data (T, Output)
This signal carries the serial data from the DTE to the DCE during the data transfer phase. During call establishment and call clearing phases, control information is passed to the DCE on this line. This signal is a differential signal.

Control (C, Output)
This signal is used during the call establishment phase to indicate the status of the DTE to the DCE. This signal is a differential signal.

Indicate (I, Input)
This signal indicates to the DTE that the DCE has made a remote connection and that the DTE should enter the data transfer phase. This signal is a differential signal.

Signal Element Timing (S, Input)
This signal provides both the receive and the transmit clocking to the DTE. This signal is a differential signal.

Receive Data (R, Input)
This signal carries the serial data from the DCE to the DTE during the data transfer phase. During call establishment and call clearing phases, control information is passed to the DTE on this line. This signal is a differential signal.

Internal Programming Considerations

Control Interface

The RT PC Multiprotocol Adapter resides in the I/O address space of the system processor. Activity carried out by this adapter is initiated and controlled via I/O reads/writes over this interface. The adapter permits the system processor to directly control the Multiprotocol Adapter DMA controller, the associated address extension registers, the 8255 peripheral interface module, and a set of external device interface and adapter control registers. The 8530 communications controller module, the program storage RAM, and the modem input registers are configured as slave devices to the 8051 microcontroller.

The adapter may use alternate controller DMA for all data transfers between the adapter and the system. Alternate controller DMA is under control of the adapter board. To transfer data, the adapter gains control of the I/O channel and transfers the data directly between the adapter and the system. The adapter contains its own 8237 DMA controller that provides four independent DMA channels. Two bytes of data are transferred for each DMA operation.

Microcontroller Operating Modes

The adapter permits the 8051 microcode to execute out of adapter resident RAM memory. During a hardware adapter reset or the execution of a software adapter reset, the 8051 microcontroller begins its execution out of Read-Only Storage (ROS). This ROS is microcoded to support two commands necessary to IPL RAM and begin RAM program execution. These commands are called the POR mode 8051 commands.

After the completion of the RAM IPL operation the user provided device driver is presented with a second set of 8051 commands. These commands are the operating mode 8051 commands. The function and definition of these operating mode commands is determined by the user provided operating mode microcode. This microcode is loaded in the adapter via the RAM IPL command and receives control via the Start Execution command.

Control of the 8051 and its slave devices are accomplished via I/O reads and writes through an 8255 peripheral interface module.

Adapter DMA Control

The 8237 DMA controller generates only 16 bits of address information. These address bits drive system address bits 1 through 16. DMA address extension capability is provided by four address extension registers that are set up via system I/O control. These registers drive system address bits 17 through 23 and enable the adapter to provide a full 24 bits of DMA addressability. (Address bit 0 is forced to '0' for all adapter DMA transfers.) It is not possible to modify the contents of the DMA address extension registers during an active transfer.

The DMA addressing results in the following restrictions on Multiprotocol Adapter DMA activity:

1. DMA transfers are limited to a maximum of 128K bytes (64K half-words) in length.
2. DMA transfers are further limited because DMA addressing cannot be incremented across a 128K address boundary.
3. DMA transfers must be at least one half-word (2 bytes) in length.

The above restrictions on DMA activity stem from the facts that the adapter hardware:

1. Always forces bit 0 of the DMA address to zero (half-word transfers)
2. Cannot increment its physical address across a 128K address boundary in the real address space. An attempt to cross such a boundary results in an error as the address counter internal to the adapters 8237 DMA controller (address bits 1-16) wraps to zero and continues incrementing. Address bit 17 will not be incremented.

While these restrictions are real, the AIX Virtual Resource Manager (VRM) handling of shared system DMA channels prevents this from becoming a problem in an RT PC system. The RT PC hardware provides address translation on 2K-byte page granularity for all DMA transfers. Each

successive 2K data page can be independent in system memory and the translation function makes these pages appear adjacent to the adapter.

In this environment the 128K boundary restriction manifests itself only for the shared system DMA window size that is permitted by the VRM. By subdividing a single system DMA channel into four windows a theoretical maximum transfer of 32K-bytes can be determined. This maximum value must then be reduced by the offset into the starting page for the desired transfer. This page offset is equal to the low order 11 bits of the first data buffer address.

Consequently, for four DMA windows, VRM permits any DMA transfer that does not touch more than 16 memory pages. With the greatest possible transfer starting offset (H'07FF') a DMA transfer of 30,720 bytes is permitted, independent of the data buffer alignment with respect to any 128K address boundary. Any transfer with fewer bytes is permitted, while any longer transfer results in a failed return code from the VRM routine. The VRM routine ($STDMA) provides the address translation initialization for all RT PC DMA operations. In addition, for shared system DMA devices, this routine also returns the I/O channel address used in the initialization of the adapter 8237 DMA controller.

Adapter Command Summary

The following is a list of the adapter interface commands to support Multiprotocol Adapter operations. Listed for each command is the I/O Data (for 'Write' commands), a Read/Write indication, and the primary and secondary adapter addresses. The Multiprotocol Adapter allows two adapters to be concurrently operating in a system at any time. To aid this feature, two adapter address ranges are provided. The user must select the appropriate address range and install a jumper prior to adapter installation. Each adapter command is discussed in detail in the later sections.

Adapter I/O Commands

Command	R/W	Primary I/O Addr	Secondary I/O Addr
Adapter Sts Reg. 1	R	H'0521'	H'0921'
Adapter Cntl Reg. 1	R/W	H'0522'	H'0922'
Initialize 8255 Mode	W	H'0523'	H'0923'
Adapter Sts Reg. 2	R/W	H'052B'	H'092B'
Intf. Cntl Reg. 1	W	H'052C'	H'092C'
Intf. Cntl Reg. 2	W	H'052D	H'092D'
Intf. Cntl Reg. 3	W	H'052E'	H'092E'
Intf. Cntl Reg. 4	W	H'052F'	H'092F'
Start Adapter Reset	W	H'0528'	H'0928'
End Adapter Reset	W	H'0528'	H'0928'
Interrupt Reset (10)	W	H'X6F2'	H'X6F2'
Interrupt Reset (11)	W	H'X6F3'	H'X6F3'

DMA Control Commands

Command	R/W	Primary I/O Addr	Secondary I/O Addr
DMA Current Addr. Reg. (Chan. 0)	R/W	H'0510'	H'0910'
DMA Current Word Reg. (Chan. 0)	R/W	H'0511'	H'0911'
DMA Current Addr. Reg. (Chan. 1)	R/W	H'0512'	H'0912'
DMA Current Word Reg. (Chan. 1)	R/W	H'0513'	H'0913'
DMA Current Addr. Reg. (Chan. 2)	R/W	H'0514'	H'0914'
DMA Current Word Reg. (Chan. 2)	R/W	H'0515'	H'0915'
DMA Current Addr. Reg. (Chan. 3)	R/W	H'0516'	H'0916'
DMA Current Word Reg. (Chan. 3)	R/W	H'0517'	H'0917'
DMA Status Reg.	R	H'0518'	H'0918'
DMA Cmd. Reg.	W	H'0518'	H'0918'
DMA Mask Reg. (Single Chan.)	W	H'051A'	H'091A'
DMA Mode Reg.	W	H'051B'	H'091B'
Clear F/L Latch	W	H'051C'	H'091C'
DMA Temporary Reg.	R	H'051D'	H'091D'
DMA Master Clear	W	H'051D'	H'091D'
DMA Mask Reg. (Multi-Chan.)	W	H'051F'	H'091F'
Ch. 0 DMA Addr Ext.	W	H'0524'	H'0924'
Ch. 1 DMA Addr Ext.	W	H'0525'	H'0925'
Ch. 2 DMA Addr Ext.	W	H'0526'	H'0926'
Ch. 3 DMA Addr Ext.	W	H'0527'	H'0927'

POR Mode Single-Byte Microcontroller Commands

Code	Command	R/W	Primary I/O Addr	Secondary I/O Addr
H'3X'	IPL Ram	W	H'0520'	H'0920'
H'4X'	Start Ram Execution	W	H'0520'	H'0920'

Adapter Commands

The following is a description of the adapter I/O commands that are available to control the operation of the Multiprotocol Adapter.

Adapter commands fall into two types:

1. Address decoded commands
2. Address and single-byte data commands.

Both of these categories are described below.

Address Decoded Commands

Address Decoded commands are a class of adapter I/O commands that do not require or provide specific associated data. These commands enable or disable various hardware functions or capabilities of the adapter. Each of these commands is described in the following sections.

Interrupt Reset Command (H'X6F2' or H'X6F3')

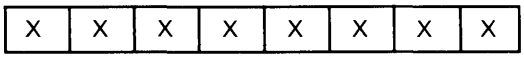
This command is issued as an I/O write to address H'X6F2' for interrupt level 10 and H'X6F3' for interrupt level 11. Execution of this command reenables adapter interrupts after the processing of a prior interrupt has completed. This command should be issued once immediately after enabling the system interface drivers, and at the termination of the interrupt handling for each adapter interrupt. In an AIX/VRM environment, this later reset operation is automatically performed by VRM in its First Level Interrupt Handler (FLIH) processing.

Single Byte Data Commands

Single byte data commands are adapter I/O commands that require or provide a single byte of associated data. These commands initialize and monitor the hardware status of the Multiprotocol Adapter. In addition, a set of single-byte commands to the adapter 8051 microcontroller provide several complex adapter functions that can be invoked using a single-byte I/O command (the 'POR Mode' 8051 command set).

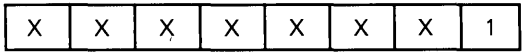
Note: The X in the address denotes a 5 or 9 for primary or alternate address.

Adapter Status Register 2 (H'0X2B')



This register provides a nondisruptive adapter presence and data bus integrity test for adapter device drivers. This is achieved by echoing specific data patterns through this register.

Start Adapter Reset Command (H'0X28')



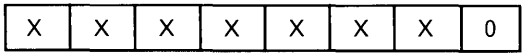
This command is issued as an I/O Write to address H'0528' or H'0928' (depending on adapter address jumpers). This command causes a hardware reset of all LSI modules and VTL latches on the adapter. This reset can be executed independently of the master system reset function. This command leaves the adapter in a bus-isolated state and requires the subsequent execution of a End Adapter Reset command followed by an 8255 Module Mode Set command to reestablish contact with the adapter. Additionally, this command could drive the adapter to a known state if it is determined that an unrecoverable adapter error has occurred. This command terminates any adapter activity.

This command starts the 8051 microcontroller doing the following:

- Resets all its registers
- Clear its internal memory
- Execute its POR diagnostics routine
- Begin waiting for the execution of any POR Mode 8051 Single-Byte command.

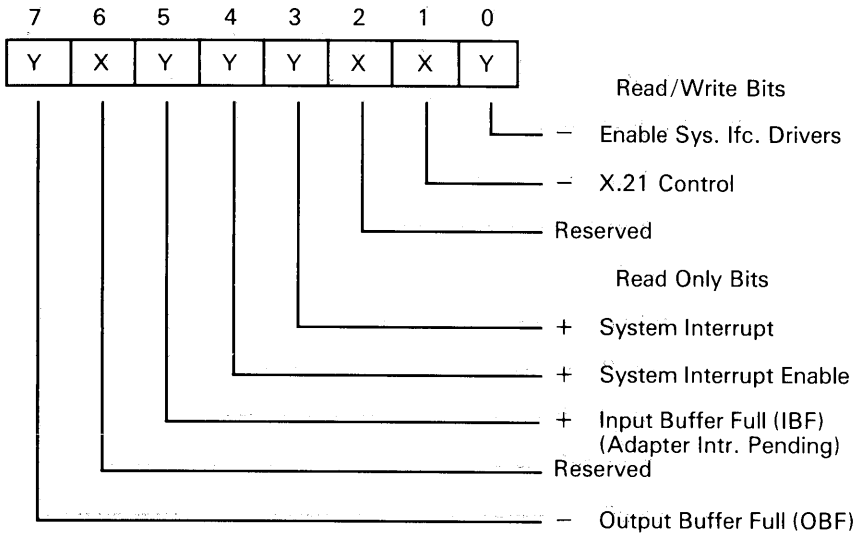
The contents of the RAM program memory should be considered invalid and the adapter RAM should be loaded before RAM execution can begin (or resume).

End Adapter Reset Command (H'0X28')



This command is issued as an I/O Write to address H'0528' or H'0928' (depending on adapter address jumpers). This command releases the adapter from the reset state entered by the Start Adapter Reset Command documented above.

Adapter Control Register 1 (H'0X22')



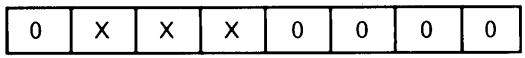
Execution of I/O to address H'0522' (or H'0922', as appropriate) allows the system device driver code to manipulate various adapter interface enables. Proper operation of this adapter control register is dependent on prior initialization of the 8255 mode register as described subsequently.

During a system hardware reset or an adapter reset operation all programmable bits of adapter control register 1 resets to 1 (all enables deactivated). The enable function of bit 0 of this register is negative true, consequently writing a 0 to this bit position enables the adapter-to-system drivers.

The register programmable bits can be individually controlled. The adapter commands required to do this are described below. After system interface initialization, the status of each bit can be obtained by reading the adapter status register 1, also described below.

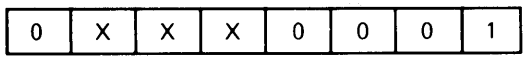
The status information contained in bit 5 is also available in bit 0 of adapter status register 1. Either of these registers can be read to determine the state of the 8255 IBF output.

Enable System Interface Drivers (H'0X23')



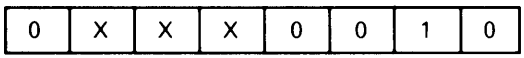
Execution of I/O to address H'0523' (or H'0923', as appropriate) enables the adapter-to-system drivers. Prior to executing this command data cannot be transferred from the adapter. Data can be transferred to the adapter regardless of enable bit status.

Disable System Interface Drivers (H'0X23')



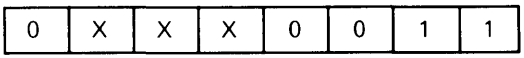
Execution of I/O to address H'0523' (or H'0923', as appropriate) disables the adapter-to-system drivers.

Drive X.21 Control On (H'0X23')



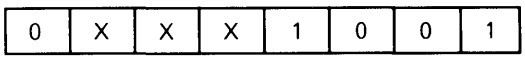
Execution of I/O to address H'0523' (or H'0923', as appropriate) asserts the X.21 Control signal to the attached X.21 DCE.

Drive X.21 Control Off (H'0X23')



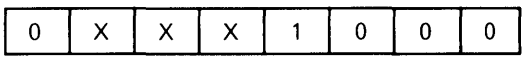
Execution of I/O to address H'0523' (or H'0923', as appropriate) deactivates the X.21 Control signal to the attached X.21 DCE.

Enable Adapter Interrupt Generation (H'0X23')



Execution of I/O to address H'0523' (or H'0923', as appropriate) enables the generation of adapter-to-system interrupts. When enabled, the 8255 module generates an interrupt when it has received a byte of status information from the 8051.

Disable Adapter Interrupts (H'0X23')



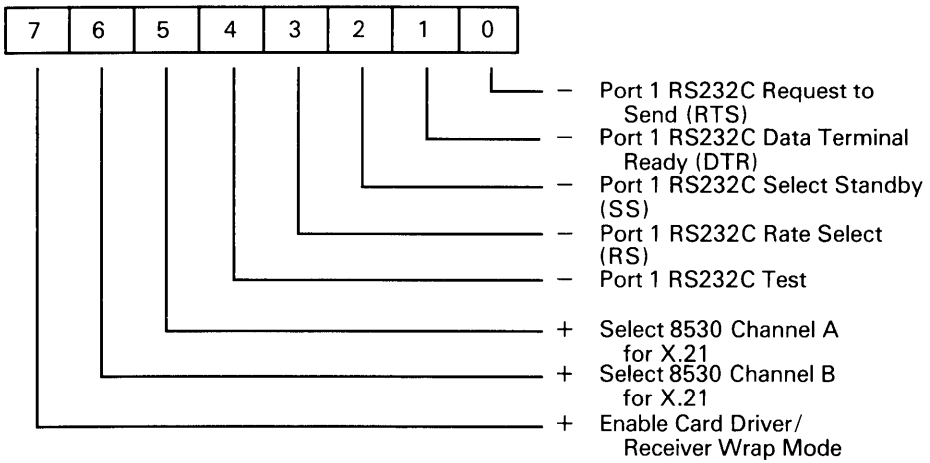
Execution of I/O to address H'0523' (or H'0923', as appropriate) disables its capability to generate interrupts.

Interface Control Register 1 (H'0X2C')

Execution of I/O to address H'052C' (or H'092C', as appropriate) allows the system device driver code to manipulate various enables and data path controls associated with the adapter Port 1.

Notice that modem control outputs are negative true and a data bit 0 activates the associated signal, while a data bit 1 is required to deactivate it. This port is output only and can only be written 8 bits at a time. The system device driver code is responsible for maintaining the current state of these outputs and changing any bits if necessary.

At adapter reset, all bits of interface control register 1 are reset to 0. The system device driver code is responsible for initializing the Port 1 interface as required prior to the enabling this external interface (see interface control register 2 below). To deactivate the RS232C outputs driven from this register prior to enabling the Port 1 outputs, a value of H'1F' should be written to this register. Notice that the control options for bits 5 through7 of this register are mutually exclusive and the device driver code is responsible for avoiding invalid configurations.



Bit 0 (Least Significant Bit)
Port 1 RS232C Request to Send. This bit controls the RTS output for adapter RS232C Port 1.

Bit 1
Port 1 RS232C Data Terminal Ready. This bit controls the DTR output for adapter RS232C Port 1.

Bit 2
Port 1 RS232C Select Standby. This bit controls the SS output for adapter RS232C Port 1.

Bit 3
Port 1 RS232C Rate Select. This bit controls the RS output for adapter RS232C Port 1.

Bit 4
Port 1 RS232C Test. This bit controls the Test output for adapter RS232C Port 1.

Bit 5
Select 8530 Channel A for X.21. This control bit enables the routing of the transmit and receive data paths for Channel A of the communication controller module to the adapter X.21 interface.

Bit 6
Select 8530 Channel B for X.21. This control bit enables the routing of the transmit and receive data paths for Channel B of the communication controller module to the adapter X.21 interface.

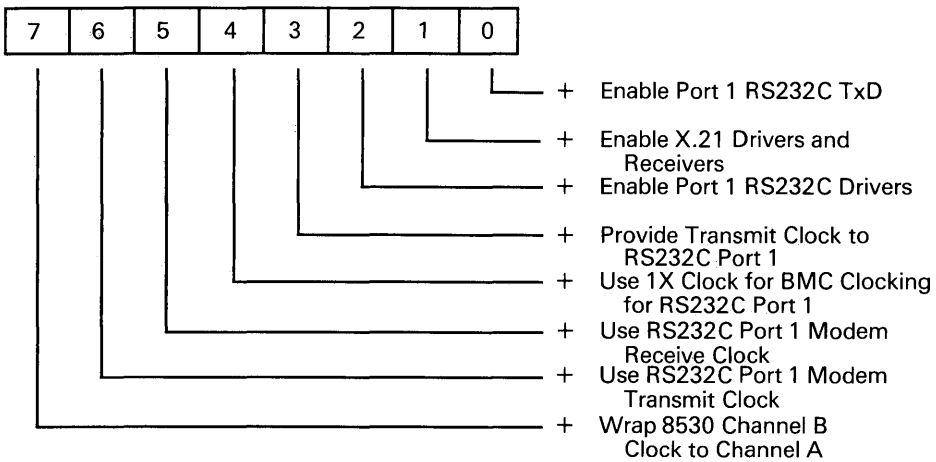
Bit 7 (Most Significant Bit)
Enable Adapter Driver/Receiver Wrap Mode. This control bit enables the routing of the 8530 channel A and B data paths to each other. Secondly, adapter interface RS232C, RS366 and X.21 outputs are wrapped back to appropriate interface inputs.

Interface Control Register 2 (H'0X2D')

Execution of I/O to address H'052D' (or H'092D', as appropriate) allows the system device driver code to manipulate various enables and clock sourcing controls associated with the adapter Port 1.

Notice that each control is positive true and thus a 1 data bit activates the associated signal, while a 0 data bit is required to deactivate it. This port is output only and can only be written 8 bits at a time. The system device driver code is responsible for maintaining the current outputs and carrying out the necessary steps to change any bits.

At adapter reset, all bits of interface control register 2 are reset to 0 (all enables deactivated). The system device driver code is responsible for initializing the Port 1 interface prior to enabling the external interface. These options can be mutually exclusive and the device driver code is responsible for avoiding invalid configurations.



Bit 0 (Least Significant Bit)

Enable Port 1 RS232C TxD. This bit enables the transmit data to the RS232C driver. It can also be used in diagnostic mode to control the TXD line on the interface. In normal operation it should be set to a 1.

Bit 1

Enable X.21 Drivers and Receivers. This bit enables (disables) the adapter X.21 interface drivers and receivers.

Bit 2

Enable Port 1 RS232C Drivers. This bit enables (disables) the adapter Port 1 RS232C interface drivers.

Bit 3

Provide Transmit Clock to RS232C Port 1. This bit enables the sourcing of Port 1 transmit data clocking by the adapter. If this bit is enabled, the adapter provides a transmit data clock signal to the modem attached to Port 1 for synchronous communications. The clock provided will be the 8530 Channel A baud rate generator clock divided by 32.

Bit 4

Use 1X Clock for BMC clocking. This enable bit causes the 8530 Channel A (Port 1) baud rate generator clock to be externally divided by 32 to facilitate its use as a data clock to clock the modem in Base Machine Clocking mode. The baud rate generator is internally required to operate at 32X the line data rate to drive the 8530 DPLL (Digital Phase-Locked Loop) circuitry. This enables the proper corresponding line data rate to be derived.

Bit 5

Use RS232C Port 1 Modem Receive Clock. This bit enables the sourcing of the Port 1 data clocking from the receive data clock of the modem attached to this port.

Bit 6

Use RS232C Port 1 Modem Transmit Clock. This bit enables the sourcing of Port 1's data clocking from the transmit data clock of the modem attached to this port.

Bit 7 (Most Significant Bit)

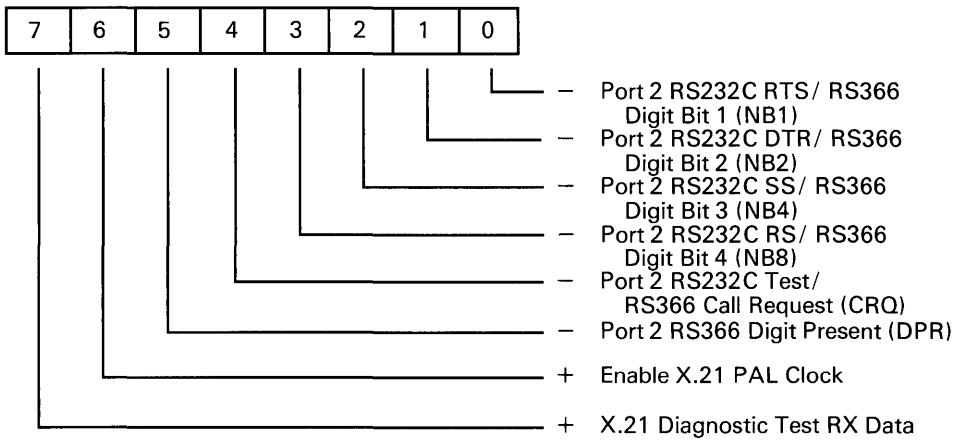
Wrap 8530 Channel B Clock to Channel A. This control bit enables the routing of the 8530 channel B Transmit Clock to the 8530 channel A Receive Clock input. The 8530 provides internal clocking options to permit the RxC input to provide both a receive and transmit clock for the appropriate channel. Zilog 8530 documentation should be consulted for additional details regarding these capabilities.

Interface Control Register 3 (H'0X2E')

Execution of I/O to address H'052E' (or H'092E', as appropriate) allows the system device driver code to manipulate various enables and controls associated with the adapter Port 2.

Notice that some controls are negative true and thus a 0 data bit activates the associated signal, while a 1 data bit is required to deactivate it. This port is output only and can only be written 8 bits at a time. The system device driver code is responsible for maintaining the current outputs and carrying out the necessary steps to change any bits.

At adapter reset, all interface control register 3 bits are reset to 0 (bits 0-5 activated). The system device driver code is responsible for initializing the Port 2 interface prior to enabling this external interface (see "Interface Control Register 4 (H'0X2F)" on page 39). To deactivate the interface outputs prior to enabling the Port 2 outputs, a value of H'3F' should be written to this register. For X.21 operation, the 6 low bits should be written off (1) and the two top bits controlled appropriately. These options are mutually exclusive and the device driver code is responsible for avoiding invalid configurations.



Output control signals for the adapter Port 2 can drive either an RS232C modem or an RS366 autocall device. Consequently, each Port 2 output has two possible definitions, only one of which is valid at any time.

Bit 0 (Least Significant Bit)

Port 2 RS232C Request to Send / RS366 Digit Bit 1. This bit controls either the RTS output (RS232C) or the NB1 output (RS366) for adapter Port 2.

Bit 1

Port 2 RS232C Data Terminal Ready / RS366 Digit Bit 2. This bit controls either the DTR output (RS232C) or the NB2 output (RS366) for adapter Port 2.

Bit 2

Port 2 RS232C Select Standby / RS366 Digit Bit 3. This bit controls either the SS output (RS232C) or the NB4 output (RS366) for adapter Port 2.

Bit 3

Port 2 RS232C Rate Select / RS366 Digit Bit 4. This bit controls either the RS output (RS232C) or the NB8 output (RS366) for adapter Port 2.

Bit 4

Port 2 RS232C Test / RS366 Call Request (CRQ). This bit controls either the Test output (RS232C) or the CRQ output (RS366) for adapter Port 2.

Bit 5

Port 2 RS366 Digit Present. This bit controls the DPR output for adapter RS366 Port 2.

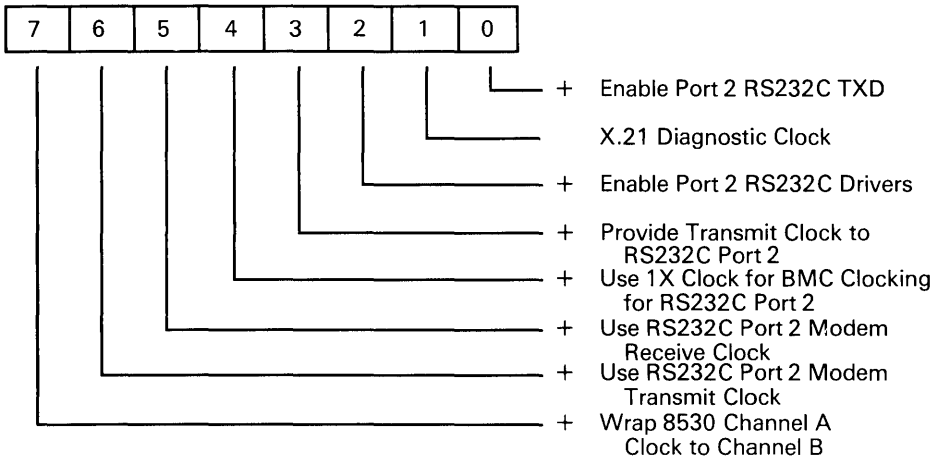
Bit 6

Enable X.21 PAL Clock. This bit enables the X.21 clock to the PAL. It also can be used in diagnostic mode to test the PAL. In normal mode, it should be set to 1 whenever X.21 interrupts are enabled.

Bit 7 (Most Significant Bit)

X.21 Diagnostic Test RX Data. This bit is used in diagnostic mode only to test the PAL. When Adapter Driver/Receiver Wrap is on, this bit controls the receive data to the PAL for testing.

Interface Control Register 4 (H'0X2F)



Execution of an I/O write to address H'052F' (or H'092F', as appropriate) allows the system device driver code to manipulate various enables and clock sourcing controls associated with the adapter Port 2.

Notice that most controls are positive true and thus a 1 data bit activates the associated signal, while a 0 data bit deactivates the signal. This port is output only and can only be written 8 bits at a time. The system device driver code is responsible for maintaining the current outputs and carrying out the necessary steps to change any bits.

At adapter reset, all interface control register 4 bits are reset to 0 (all enables deactivated). The system device driver code is responsible for initializing the Port 2 interface prior to enabling the external interface. These options can be mutually exclusive and the device driver code is responsible for avoiding invalid configurations.

Bit 0 (Least Significant Bit)

Enable Port 2 RS232C TXD. This bit enables the transmit data to the RS232 driver. It can also be used in diagnostic mode to control the TXD line on the interface. In normal operation it should be set to a 1.

Bit 1

Use this bit in diagnostic mode only. It provides a clock for wrapping the X.21 interface.

Bit 2

Enable Port 2 RS232C (RS366) Drivers. This bit enables (disables) the adapter Port 2 RS232C (RS366) interface drivers.

Bit 3

Provide Transmit Clock to RS232C Port 2. This bit enables the sourcing of Port 1 transmit data clocking by the adapter. If this bit is enabled, the adapter provides a transmit data clock signal to the modem attached to Port 2 for synchronous communications. The clock provided will be the 8530 Channel B baud rate generator clock divided by 32. Interface control register 3, bit 5 must also be set to 0 to enable this clock.

Bit 4

Use 1X Clock for BMC clocking. This enable bit causes the 8530 Channel B (Port 2) baud rate generator clock to be externally divided by 32 to facilitate its use as a data clock to clock the modem in Base Machine Clocking mode. The baud rate generator is internally operated at 32X the line data rate to drive the 8530 DPLL (Digital Phase-Locked Loop) circuitry. This enables the proper corresponding line data rate to be derived.

Bit 5

Use RS232C Port 2 Modem Receive Clock. This bit enables the sourcing of Port 2 data clocking from the receive data clock of the modem attached to this port.

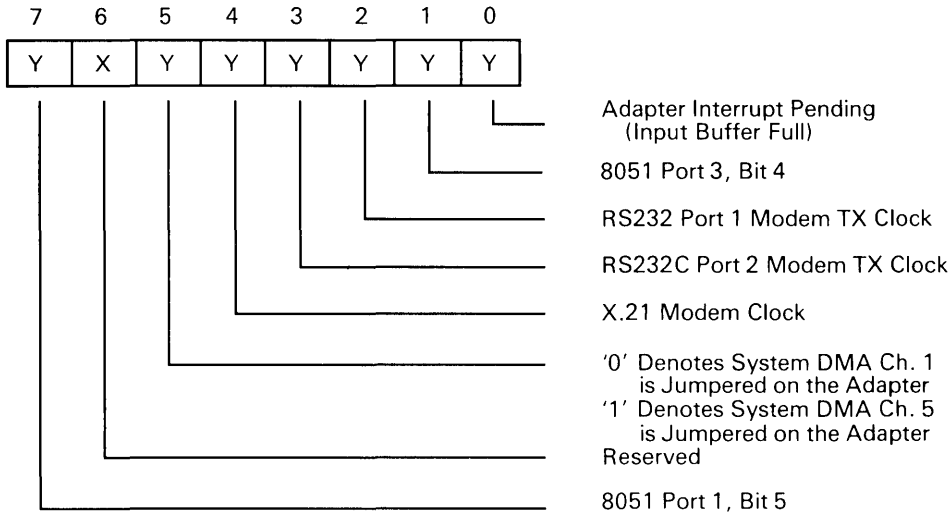
Bit 6

Use RS232C Port 2 Modem Transmit Clock. This bit enables the sourcing of Port 2 data clocking from the transmit data clock of the modem attached to this port.

Bit 7 (Most Significant Bit)

Wrap 8530 Channel A Clock to Channel B. This control bit enables the routing of the 8530 channel A Transmit clock to the 8530 channel B Receive clock input. The 8530 provides internal clocking options to permit the RxC input to provide both a receive and transmit clock for the appropriate channel. Zilog 8530 documentation should be consulted for additional details regarding these capabilities.

Adapter Status Register 1 (H'0X21')



Execution of an I/O Read from address H'0521' or H'0921' (depending on adapter address jumpers) provides the adapter status register 1 to the system processor.

In operating mode, ASR 1 Bit 0 = 1 denotes that the adapter has a pending interrupt that has not been serviced. Bit 0 = 0 denotes that there are no interrupts pending.

ASR status bit 0 indicates the presence of a status byte from the adapter processor. The adapter generates a system interrupt whenever this status byte is loaded with interrupts enabled. If interrupts are not enabled the interrupt is not propagated off the adapter, however this status bit is still available to indicate adapter-to-system status is available.

In POR mode the adapter-to-system interface is simplified. Status information is limited to the success or fail status of a limited set of ROS microcoded (mostly diagnostic) commands. This status information is passed to the system via the same register as used for interrupt status.

The input buffer full status bit (bit 0) is equivalent to the status in bit 5 of adapter control register 1 at address H'0X22'.

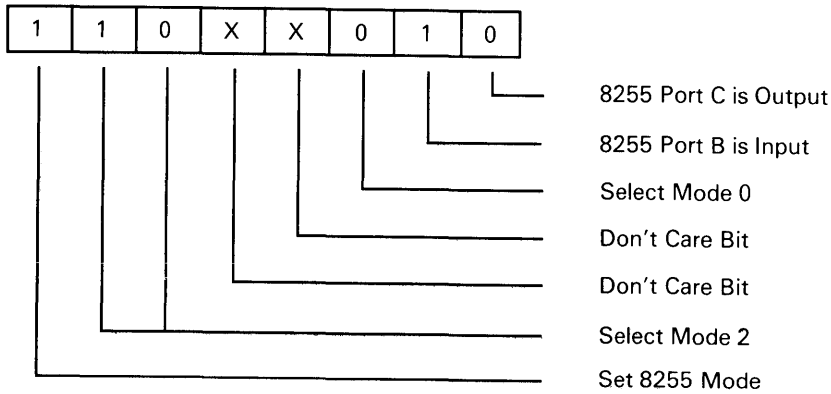
The two transmit clocks from the modem are readable for diagnostic reasons allowing the board to determine the baud rate of the clock from a synchronous modem.

Bits 2, 3, and 4 are free running clocks from the modem and should be ignored in all modes except diagnostic testing of these lines.

Bits 1 and 7 of this byte are driven directly by two 8051 I/O port bits. These bits provide a means for the 8051 to communicate status to the system processor besides normal status byte passing.

In either POR or Operating modes, these status bits are valid only after the initialization of the 8255 peripheral interface module on the adapter and the enabling of the adapter system interface drivers.

Initialize 8255 Mode Command (H'0X23')



Execution of an I/O write with data H'C2' to address H'0523' or H'0923' (depending on adapter address jumpers) is necessary to initialize the I/O interface to the 8051 adapter controller. This is accomplished by setting up the operating modes for the 8255 peripheral interface module.

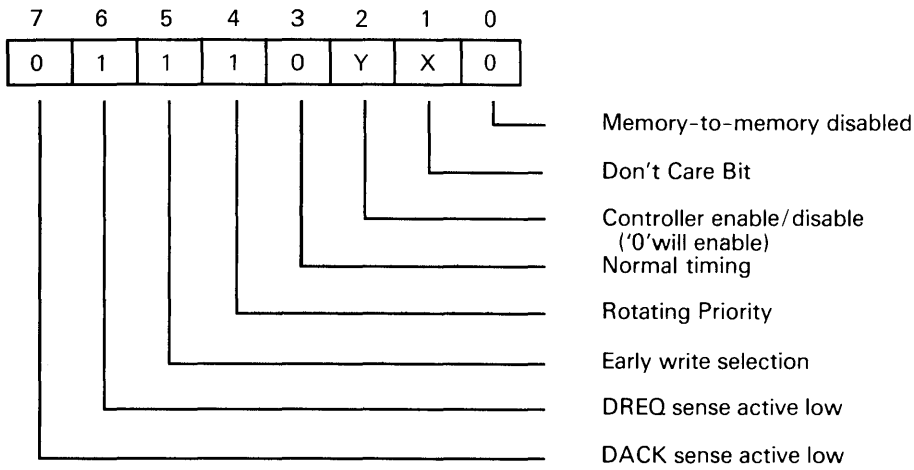
This command should be executed only once (when the adapter is first initialized) and must be executed before interrupts are enabled or any command is directed to the 8051 controller.

DMA Controller Commands

The following is a listing of the registers that must be initialized to control the operation of the 8237 DMA controller that is included on the Multiprotocol Adapter board. Additional information is included regarding two software commands needed to control the operation of the 8237 DMA controller. For additional detail regarding the functions and descriptions of these commands and registers, refer to the Intel published documentation for the 8237 DMA controller.

Notice that any of the four DMA channels can be used for any DMA transfer type. The system device driver code is responsible for the initialization of the DMA controller, and is responsible for the allocation of DMA channels for the various uses by the adapter.

DMA Command Register (H'0X18')



Execution of an I/O write to address H'0518' (or H'0918' as appropriate) is necessary to control the operation of the DMA controller. This register is cleared by a hardware system reset, an adapter reset command, or a software DMA controller reset command (see below). Initialization must be done prior to using the DMA resources of this adapter.

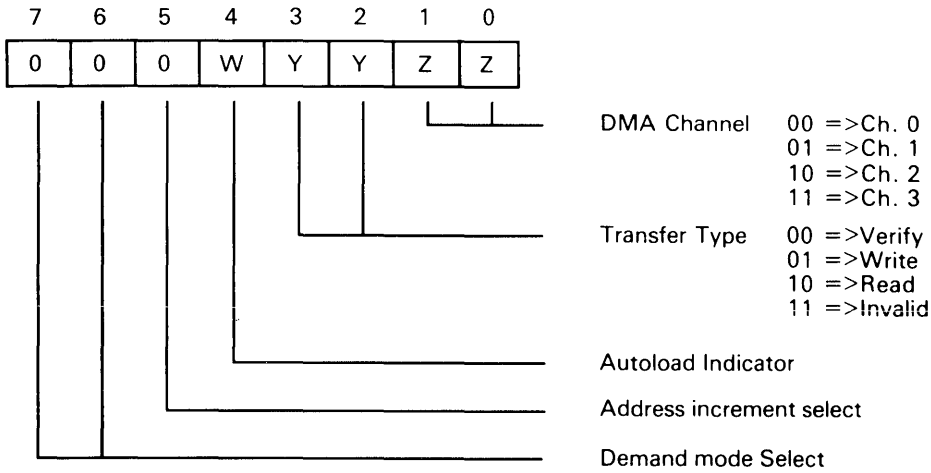
The significance of the 'Y' bit in the I/O data field is as follows:

- If this bit position is a 1 the DMA controller can be initialized but remains in a disabled state and will not respond to DMA service requests.
- If this bit position is a 0 the DMA controller is enabled and functions normally.

During first initialization of this register this bit should be set to a 1 (data byte H'74') disabling the controller. After all other DMA registers have been initialized, a second initialization should change

this bit to a 0 (data byte H'70') just before the time DMA use is anticipated. When the adapter is closed at the end of all communications activity, an adapter reset command can be issued, effectively disabling DMA at that time.

DMA Mode Registers (H'0X1B)'



Each of the four available DMA channels has a 6-bit mode register associated with it. Initialization of these registers is required to define the characteristics of the DMA transfer that is to take place on that channel. The significance of the variable data bits in these initializations is as follows:

The W bit determines whether the specific channel is used in the autoload mode. If autoload is selected, the DMA controller retains the channel base address and base transfer count parameters in its internal memory. At transfer completion, these stored parameters are automatically transferred into the channel's active base address and active count registers, thereby preparing the controller for a subsequent transfer of the same type. If this operation is desired, the W bit should be initialized to a 1.

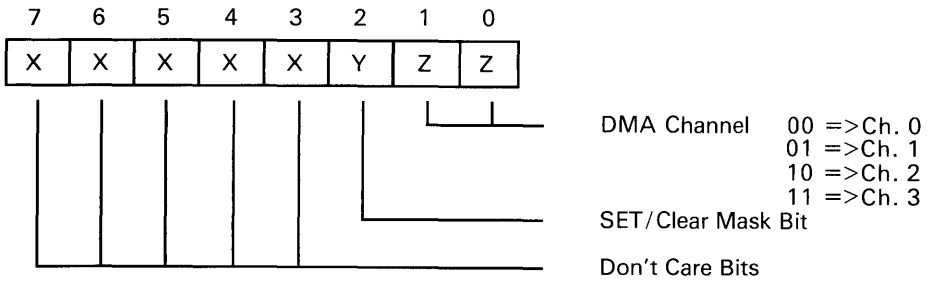
The YY bits determine the type of DMA transfer that occurs on the specific channel. This information is encoded per the following:

YY Bits	Significance
B'00'	Denotes a verify transfer.
B'01'	Denotes a write transfer. Data is transferred from the adapter to system memory. This operation transfers receive data or adapter status to the system.
B'10'	Denotes a read transfer. Data is transferred from system memory to the adapter. This operation transfers transmit data or multibyte adapter commands to the adapter.
B'11'	This data bit pattern is not valid.

The ZZ bits determine which of the four DMA channels is initialized by this command. This information is encoded per the following:

ZZ Bits	Significance
B'00'	Denotes initialize mode for channel 0.
B'01'	Denotes initialize mode for channel 1.
B'10'	Denotes initialize mode for channel 2.
B'11'	Denotes initialize mode for channel 3.

Single Channel DMA Mask Register (H'0X1A')

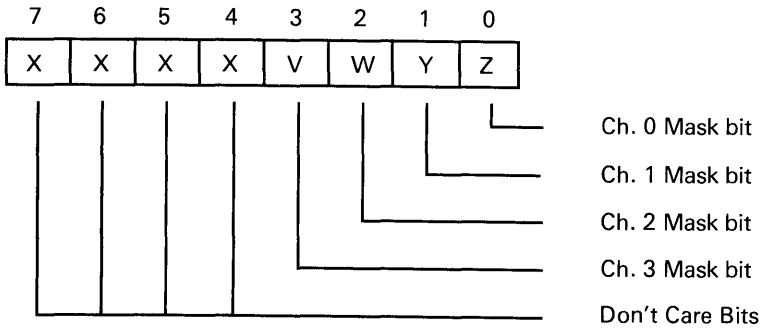


Each DMA channel has a mask bit which disables the incoming DMA request signal on that channel. Each channel's mask bit is automatically set when that channel's terminal count is reached if that channel is not in autoload mode. After reinitialization of the appropriate channel address and count registers to prepare for the next DMA transfer, the mask register is cleared to reenable that channel's DMA request.

Each mask bit can also be set or cleared independently at any time by software command. An I/O write to address H'051A' or H'091A' (as appropriate) achieves this capability on the adapter. The encoding of the Y data bit for this command is as follows:

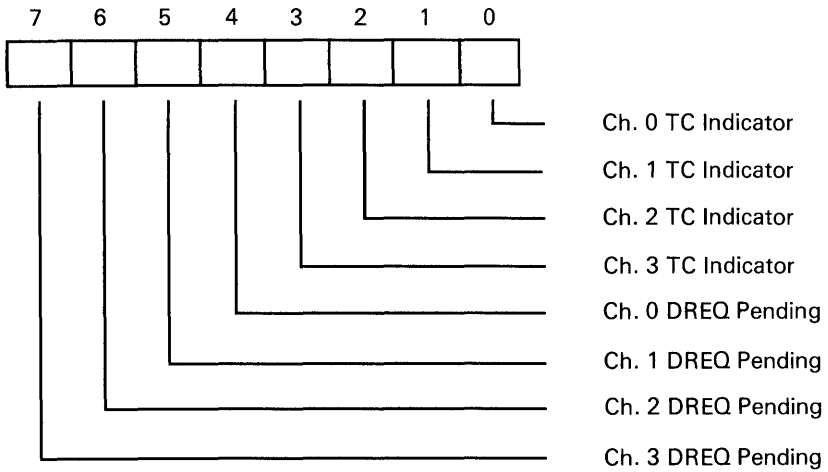
- Bit 'Y' = 1 Sets the desired mask bit.
- Bit 'Y' = 0 Clears the desired mask bit.

Multiple Channel DMA Mask Register (H'0X1F')



Besides the single channel mask command described above, the 8237 DMA controller provides the capability to change multiple channel mask bits with a single command. Execution of an I/O write to either address H'051F'or H'091F' (as appropriate) with the desired mask pattern in the data byte will simultaneously change all 4 mask bits to the values specified in this data field. A data bit value of 1 sets the designated mask bit (and thus enable DMA activity), while a value of 0 clears this mask bit (and thus disable DMA activity).

DMA Status Register (H'0X18')



The status register is read by the system processor. It contains the status of the four DMA channels. The TC indicator bit indicates that the specified channel has progressed to terminal count

and has thus completed a maximum length transfer. The DREQ pending bit indicates that the specified channel currently has a DMA service request pending. The TC Indicator bits contained in this register are reset by a status read operation.

DMA Current Address Register, Channel 0 Through Channel 3 (H'0X10','0X12','0X14','0X16')

Each DMA channel has a current address register. A DMA channel can increment over a range of 16 bit addresses. The current address register holds the address value used during DMA transfers. This address is automatically incremented or decremented after each transfer and the address intermediate values are stored in the current address register during the transfer. This register can be written or read by the system processor in successive 8-bit bytes. It may also be reinitialized by an autoinitialize back to its original value. Autoinitialize takes place only after terminal count is reached.

The adapter DMA supports only word data transfers. Consequently, the addresses generated by the 8237 DMA controller include address bits 1 through 16 as incremental bits. Address bit 0 will always be 0 for 16-bit (half-word) data transfers; system DMA buffers must begin on an even address boundary. Prior to DMA initialization, the DMA initialization address must be computed according to the following chart:

Unadjusted Parameters

DMA Start Address	DMA Byte Length	DMA Init. Address
Even	Even	(A/2)
Even	Odd	(A/2)
Odd	Even	(A-1)/2
Odd	Odd	(A-1)/2

DMA Current Transfer Count Register, Channel 0 Through 3 (H'0X11','0X13','0X15','0X17')

Each DMA channel has a 16-bit current transfer count register. This register stores the current transfer count (in half-words). The transfer count is decremented after each transfer. The intermediate transfer count value is stored in the register during the transfer. When the value in this register is decremented from zero, a terminal count (TC) is generated. This register is loaded or read by the system processor in successive 8-bit bytes in the program condition. Following DMA service it may also be reinitialized by an autoinitialization back to its original value. Autoinitialize occurs only when terminal count is reached.

DMA on the Multiprotocol Adapter supports only half-word (16-bit) data transfers. Before DMA initialization, the data transfer count must be computed according to the following chart:

Unadjusted Parameters

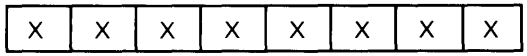
DMA Start Address	DMA Byte Length	DMA Init. Count
Even	Even	(BL/2)-1
Even	Odd	((BL+1)/2)-1
Odd	Even	((BL+2)/2)-1
Odd	Odd	((BL+1)/2)-1

DMA Base Address Registers, DMA Base Transfer Count Registers

Each DMA channel has a pair of base address and base transfer count registers. These 16-bit registers store the original value of their associated current registers. During autoinitialization these values restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register by the system processor. These registers cannot be read by the system processor.

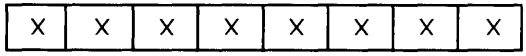
Additional DMA Software Commands

Clear First/Last Latch (H'0X1C')



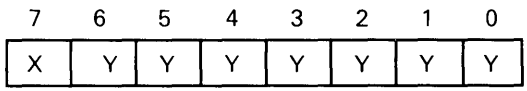
An I/O Write to this address clears the first/last byte latch. This command should be executed prior to writing or reading new address or word count information to or from the 8237. This initializes the latch to a known state so that subsequent accesses to register contents by the system processor addresses upper and lower bytes in the correct sequence.

Master Clear (H'0X1D')



An I/O Write to this address has the same effect as a hardware reset of the 8237 DMA controller. The command, status, request, temporary, and internal first/last latch registers are cleared and the mask register is set. The 8237 enters the idle cycle.

Write DMA Address Extension Register, Channel 0 through 3 (H'0X24','0X25','0X26,'0X27')



Each channel has an 8-bit write DMA address extension register. This command transfers the associated data into the DMA address extension register for the appropriate channel. The contents of I/O data bits 0 through 6 drive address bits 17 through 23 on the I/O channel when a DMA transfer takes place. Data bit 7 is not used and cannot be written by the system.

External Programming Considerations

POR Mode Microcontroller Single-Byte Commands

The following command codes are passed to the Multiprotocol Adapter via an I/O write to the 8255 peripheral interface module. Each of these adapter commands require processing by the 8051 microcontroller on the adapter. Commands included in this list are valid after an adapter or system reset, prior to issuing a Start Execution command after a RAM IPL is completed.

For the RAM IPL command, a command completion status is passed to the system as follows: After all command processing is complete the 8051 formats a command completion status byte and then outputs this byte to the system 8255 port. The system should periodically poll the 8255 during the time when one of these commands is executing. When the 8255 IBF status bit indicates that a byte has been written to the system, this byte should be read and examined to determine the success or failure of the IPL.

A status byte containing H'00' indicates the IPL has completed without error. A status byte containing one or more '1' bits indicates that an error was detected by the 8051.

Notice that if adapter interrupts are enabled, an interrupt is generated at the time completion status is written to the status port. Any code designed to run above the adapter in POR mode should be prepared to field these interrupts if interrupts are to be enabled.

Notice also that the adapter POR Mode command processor does not support multiple outstanding commands. The device driver must wait for a response to the RAM IPL command before a Start Execution command will be honored.

If an invalid (or undefined) POR command is issued, the adapter ignores the command and does not send a return code.

For the IPL RAM command, the value of the command source identifier bit (bit 3 of the command code byte) is available in bit 1 of adapter status register 1 at the time the status byte is presented by the POR mode adapter microcode.

IPL RAM (H'0X20')

0	0	1	1	Y	X	Z	Z

Execution of this command causes the 8051 to execute a DMA transfer from system memory to consecutive locations in its adapter RAM. This process starts at the 8051 program memory address H'2000' and continues until a DMA terminal count (TC) is detected. A maximum IPL of 8K-bytes of microcode is supported. The entire adapter memory space is initialized to zeros prior to the IPL process.

After detection of a DMA TC, the 8051 microcontroller calculates a checksum value for the RAM image. The 8051 successively adds each 8-bit program memory byte to the accumulator until the complete memory space (regardless of actual program length) has been checked. The 8051 accumulator should now contain a value of H'00'. Successful IPL is indicated to the system by the passing of a H'00' status byte only if the transfer and checksum calculation complete successfully. Should this verification fail, the computed nonzero checksum value will be passed. The system can attempt to repeat the IPL process if an IPL failure is indicated.

The IPL data buffer must be aligned on an even system address boundary and must be an even number of bytes in length. To ensure that the complete buffer length will be even, the optional inclusion of a H'00' pad byte is provided before the checksum byte. This structure is represented graphically in Figure 14 on page 52.

The interpretation of the Y bit in the command code is shown below.

Y Bit	**Definition** .
B'0'	This command was issued by a Port 1 VRM device driver.
B'1'	This command was issued by a Port 2 VRM device driver.

The interpretation of the ZZ bits in the command code is shown below.

ZZ Bits	**Definition** .
B'00'	Adapter DMA channel 0 is used.
B'01'	Adapter DMA channel 1 is used.
B'10'	Adapter DMA channel 2 is used.
B'11'	Adapter DMA channel 3 is used.

The specific format of the data buffer for this command is as indicated below:

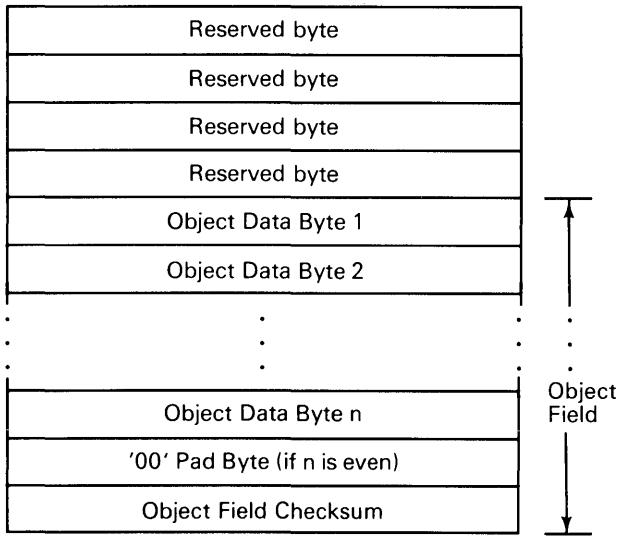


Figure 14. IPL Data Buffer

Notes:

1. Notice that the first 4 bytes of this structure are reserved. These bytes can contain arbitrary data, however they cannot be omitted from the data sent to the adapter.
2. The object data field contains the 8051 object to be downloaded.
3. The object field checksum contains the value necessary to force the complete object field, the pad byte (if present), and the checksum to sum to a value with H'00' in its least significant eight bits.

Start Execution (H'0X20')

0	1	0	0	Y	X	X	X

Execution of this command causes the 8051 to branch to RAM program memory address H'2001' and begin instruction execution.

Command success or fail status is not passed by an interrupt from the ROS adapter microcode. Indication of command completion is left to the user provided microcode program that receives control via this command.

The interpretation of the Y bit in the command code is shown below.

Y Bit	Definition
B'0'	This command was issued by a Port 1 VRM driver.
B'1'	This command was issued by a Port 2 VRM driver.

Operating Mode Microcontroller Commands

Besides the set of POR Mode (ROS resident) adapter commands, it is anticipated that the user will provide a set of operating mode adapter commands that are interpreted by a downloaded microcode program. The commands included in this list is recognized by the adapter after the completion of the RAM IPL process. This process consists of:

- Execution of a POR Mode IPL command to load the adapter's operating microcode. This microcode makes up the operating system used by the adapter processor when in operating mode.
- Execution of a POR Mode Start Execution command to transfer control to the downloaded microcode.

After the completion of this process the commands supported by the downloaded microcode are available for use by a device driver. These commands are given to the adapter processor via the same mechanism as for the prior POR mode commands, such as an I/O write through the 8255 peripheral interface module. After all command processing completes, the 8051 formats the command completion status according to conventions defined by the user and then interrupts the system processor by writing a status byte into the 8255 port to the system processor. Additional status bytes (if any) can be passed to the system after this first status byte has been read by the system processor.

The functions provided by this command set and the status returned are the responsibility of the user provided microcode program.

Operating Microcode Entry Points (from ROS)

The ROS program transfers control to the RAM executable program at the occurrence of each of the following five events. It is the responsibility of the user provided downloaded microcode to provide appropriate service routines (or immediate returns).

1. Execution of the POR mode Start Execution Command

   Execution of this POR mode command causes program control to be transferred to absolute address H'2001' in external program memory.

2. Detection of 8051 interrupt level 0

   When the 8051 processor detects this interrupt, control is automatically transferred to an address in its ROS program space. This interrupt is then revectored from ROS to RAM to absolute address H'2003'. The 8051 level 0 interrupts occur either due to a transition of the OBF signal from the 8255 module (a command was received from the system processor) or due to an X.21 interface state transition. The ROS program saves the contents of the 8051 accumulator to the stack prior to revectoring this interrupt and restores it prior to its return from interrupt. The user should execute an 8051 RET instruction from his RAM microcode and allow the return to process normally through the ROS.

3. Detection of 8051 interrupt level 1

   When the 8051 processor detects this interrupt, control is automatically transferred to an address in its ROS program space. This interrupt is then revectored from ROS to RAM to absolute address H'2006'. The 8051 level 1 interrupts occur due to a transition of the IBF signal from the 8255 module (a status byte was read by the system processor). The ROS program saves the contents of the 8051 accumulator to the stack prior to revectoring this interrupt and restores it prior to its return from interrupt. The user should execute an 8051 RET instruction from his RAM microcode and allow the return to process normally through the ROS.

4. Expiration of 8051 internal timer 0

   When the 8051 processor detects the expiration of its internal timer 0, control is automatically transferred to an address in its ROS program space. This interrupt is then revectored from ROS to RAM to absolute address H'2009'. The ROS program saves the contents of the 8051 accumulator to the stack prior to revectoring this interrupt and restores it prior to its return from interrupt. The user should execute an 8051 RET instruction from his RAM microcode and allow the return to process normally through the ROS.

5. Expiration of 8051 internal timer 1

   When the 8051 processor detects the expiration of its internal timer 1, control is automatically transferred to an address in its ROS program space. This interrupt is then revectored from ROS to RAM to absolute address H'200C'. The ROS program saves the contents of the 8051 accumulator to the stack prior to revectoring this interrupt and restores it prior to its return

from interrupt. The user should execute an 8051 RET instruction from his RAM microcode and allow the return to process normally through the ROS.

Entry Points into ROS (from RAM)

There are no supported entry points into the ROS 8051 microcode from RAM executing programs.

8051 Capabilities Precluded

The 8051 processor's integrated serial port is not supported by either this adapter or the ROS microcode.

Connector Specifications

This section describes the I/O lines that connect the adapter to the three different connectors: RS232C, RS366, and X.21.

The following tables show the device interface lines of the three adapter connectors:

Signal	Pin	Direction
TI	01	I
RxC	02	I
RxD	03	I
TxC (DCE SRC)	04	I
Ground	05	-
TEST	06	O
TxC (DTE SRC)	07	O
TxD	08	O
RTS	09	O
DTR	10	O
SS	11	O
RS	12	O
CTS	13	I
DSR	14	I
DCD	15	I
RI	16	I

Figure 15. Port 1 Connector

Signal	Pin	Direction
TI / PND	01	I
RxC	02	I
RxD / RS366 Diag.	03	I
TxC	04	I
Ground	05	-
TEST/ CRQ	06	O
TxC (DTE SRC) / DPR	07	O
TxD	08	O
RTS / NB1	09	O
DTR / NB2	10	O
SS / NB4	11	O
RS / NB8	12	O
CTS / PWI	13	I
DSR / DLO	14	I
DCD / ACR	15	I
RI / COS	16	I

Figure 16. Port 2 Connector

Signal	Pin	Direction
X.21 TxD (B)	01	O
X.21 Control (A)	02	O
X.21 RxD (A)	03	I
Ground	04	-
X.21 Indicate (B)	05	I
X.21 Sig. Ele. Timing (B)	06	I
Reserved	07	-
X.21 TxD (A)	08	O
X.21 Control (B)	09	O
X.21 RxD (B)	10	I
Reserved for Keying	11	-
X.21 Indicate (A)	12	I
X.21 Sig. Ele. Timing (A)	13	I
Reserved	14	-

Figure 17. Port 3 Connector

Sample Program

```
SASC     Sample MP ASC Microcode                                                    PAGE    2

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    A5M51 V1.9 07.09 05/09/86

                                     3 ************************************************************************
                                     4 **                                                                    **
                                     5 **  ROUTINE NAME:  MULTIPROTOCOL ADAPTER SAMPLE ASYNC MICROCODE       **
                                     6 **                                                                    **
                                     7 **  DESCRIPTIVE NAME:  SAMPLE ASYNC                                   **
                                     8 **                                                                    **
                                     9 **  CHANGE LEVEL:  A01                                                **
                                    10 **                                                                    **
                                    11 **  DATE LAST CHANGED:  05/09/86                                      **
                                    12 **                                                                    **
                                    13 **  Original Programmer:      D W Solie, F63/045 Austin               **
                                    14 **  Revised & Maintained by:  W Freeman, F63/045 Austin               **
                                    15 **                                                                    **
                                    16 **                                                                    **
                                    17 **  COPYRIGHT:  Copyright International Business Machines             **
                                    18 **              Corporation 1986.  All rights reserved.               **
                                    19 **                                                                    **
                                    20 **                                                                    **
                                    21 **  FUNCTION:                                                         **
                                    22 **  This microcode program provides an example of a functional        **
                                    23 **  adapter level program.  With appropriate device driver and        **
                                    24 **  application programming, this microcode program can be used       **
                                    25 **  to support one or two ports of async data communications.         **
                                    26 **                                                                    **
                                    27 **  NOTES:  REGISTER BANK 0 USAGE                                     **
                                    28 **                                                                    **
                                    29 **  DEPENDENCIES:  NONE                                               **
                                    30 **                                                                    **
                                    31 **  RESTRICTIONS:  NONE                                               **
                                    32 **                                                                    **
                                    33 **  SUBROUTINES CALLED:                                               **
                                    34 **                                                                    **
                                    35 ************************************************************************

                                    37 ************************************************************************
                                    38 **                                                                    **
                                    39 **  HISTORY OF CHANGES TO ROUTINE                                     **
                                    40 **  -----------------------------                                     **
                                    41 **                                                                    **
                                    42 **  DATE       RELEASE   ORIGINATOR   EXPLANATION OR                  **
                                    43 **  CHANGED    NUMBER    OF CHANGE    REASON FOR CHANGE              **
                                    44 **                                                                    **
                                    45 **  05/09/86   A01       FREEMAN      Sample Async Microcode Imple-  **
                                    46 **                                       mentation completed.         **
                                    47 **                                                                    **
                                    48 ************************************************************************
```

```
SASC     Sample MP ASC Microcode                                                    PAGE    3

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    ASM51 V1.9 07.09 05/09/86

                                    50 ************************************************************************
                                    51 ************************************************************************
                                    52 ************************************************************************
                                    53 ************************************************************************
                                    54 ****                                                                ****
                                    55 ****                                                                ****
                                    56 ****          Equates and Internal RAM label definitions for        ****
                                    57 ****               ASC communications using the Sailboat            ****
                                    58 ****               Multi-Protocol Communications Adapter            ****
                                    59 ****                                                                ****
                                    60 **** DATE LAST CHANGED:  11/25/85                                    ****
                                    61 ****                                                                ****
                                    62 **** 11/25/85:  Sample Async Microcode Implementation Completed     ****
                                    63 ****                                                                ****
                                    64 ************************************************************************
                                    65 ************************************************************************
                                    66 ************************************************************************
                                    67 ************************************************************************
```

```
SASC     Sample MP ASC Microcode                                                    PAGE    4

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    ASM51 V1.9 07.09 05/09/86

                                    70 ************************************************************************
                                    71 *                                                                      *
                                    72 *                          8051 I/O PORT EQUATES                       *
                                    73 *                                                                      *
                                    74 ************************************************************************

                                    76 *                                  8051 I/O PORT 1 BIT DEFINITIONS
90   90.0                           77 DREQ0       EQUB    P1.0                DMA REQUEST ENCODE 0
91   90.1                           78 DREQ1       EQUB    P1.1                DMA REQUEST ENCODE 1
92   90.2                           79 DMAREQEN    EQUB    P1.2                DMA REQUEST ENABLE
93   90.3                           80 P1SPARE3    EQUB    P1.3                SPARE BIT
94   90.4                           81 DACKBACK    EQUB    P1.4                ANY DACK RETURNED
95   90.5                           82 IPLCOMP     EQUB    P1.5                ADAPTER IPL COMPLETE TO 8255
96   90.6                           83 P1SPARE6    EQUB    P1.6                SPARE BIT
97   90.7                           84 P1SPARE7    EQUB    P1.7                SPARE BIT

                                    86 *                                  8051 I/O PORT 3 BIT DEFINITIONS
B0   B0.0                           87 TC          EQUB    P3.0                8237 TERMINAL COUNT
B1   B0.1                           88 P3SPARE1    EQUB    P3.1                SPARE BIT
B2   B0.2                           89 INTR0       EQUB    P3.2                OBF INTERRUPT LEVEL 0
B3   B0.3                           90 IBF         EQUB    P3.3                8255 INPUT BUFFER FULL INTR 1
B4   B0.4                           91 P1P2INTR    EQUB    P3.4                -P1/+P2 INTERRUPT SOURCE
B5   B0.5                           92 OBF         EQUB    P3.5                8255 OUTPUT BUFFER FULL INPUT
B6   B0.6                           93 WRITE       EQUB    P3.6                8051 WRITE SIGNAL OUTPUT
B7   B0.7                           94 READ        EQUB    P3.7                8051 READ SIGNAL OUTPUT
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86

                                    97 ********************************************************************************
                                    98 *                                                                              *
                                    99 *                          MISCELLANEOUS EQUATES                               *
                                   100 *                                                                              *
                                   101 ********************************************************************************

                                   103 *  REGISTER INITIALIZATION EQUATES

00000055                           105 STACK       EQU     STACKBEG-1          BEGINNING OF STACK POINTER


                                   108 * OPERATING MODE COMMAND EQUATES

00000020                           110 XSPCMD      EQU     X'20'               XMIT SPECIAL CHAR CMD
00000030                           111 RMCCMD      EQU     X'30'               MODE CONTROL COMMANDS
00000050                           112 SDMACMD     EQU     X'50'               START COMMAND DMA CMD
00000022                           113 XON1CMD     EQU     X'22'               SEND XON CHAR CMD P1
00000023                           114 XOFF1CMD    EQU     X'23'               SEND XOFF CHAR CMD P1
0000002A                           115 XON2CMD     EQU     X'2A'               SEND XON CHAR CMD P2
0000002B                           116 XOFF2CMD    EQU     X'2B'               SEND XOFF CHAR CMD P2

                                   118 * MB COMMAND CODE EQUATES

00000000                           120 INL8530A    EQU     X'00'               INIT 8530 CHAN A CMD
00000001                           121 INL8530B    EQU     X'01'               INIT 8530 CHAN B CMD

                                   123 * 8051 ADDRESSING EQUATES FOR MOVX INSTRUCTIONS

00000098                           125 H8530A      EQU     X'98'               HI BYTE ADDR FOR 8530 CHAN A
00000001                           126 L8530A      EQU     X'01'               LO BYTE ADDR FOR 8530 CHAN A
00000003                           127 L8530AD     EQU     X'03'               LO DATA ADDR FOR 8530 CHAN A
00000098                           128 H8530B      EQU     X'98'               HI BYTE ADDR FOR 8530 CHAN B
00000000                           129 L8530B      EQU     X'00'               LO BYTE ADDR FOR 8530 CHAN B
00000002                           130 L8530BD     EQU     X'02'               LO DATA ADDR FOR 8530 CHAN B
00000090                           131 ADR8255     EQU     X'90'               HI BYTE ADDR FOR 8255
000000A0                           132 ADRMDM1     EQU     X'A0'               PORT 1 MODEM INPUT REGISTER
000000C0                           133 ADRMDM2     EQU     X'C0'               PORT 2 MODEM INPUT REGISTER
00000080                           134 ADRLODMA    EQU     X'80'               ADDRESS OF LO BYTE OF DMA WORD
00000088                           135 ADRHIDMA    EQU     X'88'               ADDRESS OF HI BYTE OF DMA WORD

                                   137 * STATUS PASS EQUATES

00000001                           139 OVRSTAT     EQU     X'01'               OVR BIT ON IN STATUS BYTE
00000002                           140 PARESTAT    EQU     X'02'               PARITY ERROR STATUS VALUE
00000004                           141 FRMESTAT    EQU     X'04'               FRM BIT ON IN STATUS BYTE

00000001                           143 DMATCST     EQU     X'01'               DMA TERM COUNT STATUS BIT ON
00000020                           144 XONSTAT     EQU     X'20'               XON BIT ON IN STATUS BYTE
00000010                           145 XOFFSTAT    EQU     X'10'               XOFF BIT ON IN STATUS BYTE
00000008                           146 XBRKSTAT    EQU     X'08'               XON BIT ON IN STATUS BYTE
00000000                           147 BRKDATA     EQU     X'00'               DATA BYTE RETURNED FOR BRK RCVD
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    ASM51 V1.9 07.09 05/09/86

                                   149 * STATUS PASS JUMP TABLE EQUATES

00000000                           151 ZEROBYTE   EQU     X'00'            STATUS BYTE CNT VALUE
00000001                           152 ONEBYTE    EQU     X'01'            STATUS BYTE CNT VALUE
00000002                           153 TWOBYTE    EQU     X'02'            STATUS BYTE CNT VALUE

                                   155 * MISC OPERAING MODE EQUATES

00000008                           157 EN8530TX   EQU     X'08'            8530 ENABLE XMITTER MASK
00000001                           158 EN8530RX   EQU     X'01'            8530 ENABLE RCVER MASK
00000010                           159 ENDSTACK   EQU     CMDST7+1         1 BEYOND END OF CMD STACK

                                   161 * 8530 REGISTER EQUATES CHAN A

00000001                           163 R1A8530    EQU     X'01'            8530 REG 1 ADDR (READ OR WRITE)
00000003                           164 R3A8530    EQU     X'03'            8530 REG 3 ADDR (READ OR WRITE)
00000005                           165 R5A8530    EQU     X'05'            8530 REG 5 ADDR (READ OR WRITE)
0000000A                           166 RAA8530    EQU     X'0A'            8530 REG A ADDR (READ OR WRITE)

                                   168 * 8530 REGISTER EQUATES CHAN B

00000001                           170 R1B8530    EQU     X'0A'            8530 REG 1 ADDR (READ OR WRITE)
00000003                           171 R3B8530    EQU     X'03'            8530 REG 3 ADDR (READ OR WRITE)
00000005                           172 R5B8530    EQU     X'05'            8530 REG 5 ADDR (READ OR WRITE)
0000000A                           173 RAB8530    EQU     X'0A'            8530 REG A ADDR (READ OR WRITE)
```

LOC OBJECT CODE ADDR1 ADDR2 STMT SOURCE STATEMENT ASM51 V1.9 07.09 05/09/86

```
                        176 ************************************************************************
                        177 ************************************************************************
                        178 *                                                                      *
                        179 *  THE FOLLOWING DEFINE THE REGISTER BANK AREA                         *
                        180 *                                                                      *
                        181 ************************************************************************

000000                  183             DSECT
                        184 *                                   REGISTER BANK 0 RAM BYTES 0-7
000000                  185 RB0R0       DS      1X                 REGISTER 3
000001                  186 RB0R1       DS      1X                 REGISTER 3
000002                  187 RB0R2       DS      1X                 REGISTER 3
000003                  188 RB0R3       DS      1X                 REGISTER 3
000004                  189 RB0R4       DS      1X                 REGISTER 4
000005                  190 RB0R5       DS      1X                 REGISTER 5
000006                  191 RB0R6       DS      1X                 REGISTER 5
000007                  192 RB0R7       DS      1X                 REGISTER 5
00000000                193 CMDEXPTR    EQU     R0                 REG0 COMMAND EXEC PTR
00000001                194 CMDSTPTR    EQU     R1                 REG2 COMMAND STACK PTR
00000002                195 CMDCNT      EQU     R2                 REG1 COMMAND COUNTER
00000004                196 WORK4       EQU     R4                 TEMP WORK REG

                        198 *                                   REGISTER BANK 1 RAM BYTES 8-15
000008                  199 CMDST0      DS      1X                 COMMAND STACK BUFFER
000009                  200 CMDST1      DS      1X                 COMMAND STACK BUFFER
00000A                  201 CMDST2      DS      1X                 COMMAND STACK BUFFER
00000B                  202 CMDST3      DS      1X                 COMMAND STACK BUFFER
00000C                  203 CMDST4      DS      1X                 COMMAND STACK BUFFER
00000D                  204 CMDST5      DS      1X                 COMMAND STACK BUFFER
00000E                  205 CMDST6      DS      1X                 COMMAND STACK BUFFER
00000F                  206 CMDST7      DS      1X                 COMMAND STACK BUFFER

                        208 *                                   REGISTER BANK 2 RAM BYTES 16-23
000010                  209 SPARE10     DS      1X                 Spare byte position
000011                  210 SPARE11     DS      1X                 Spare byte position
000012                  211 SPARE12     DS      1X                 Spare byte position
000013                  212 SPARE13     DS      1X                 Spare byte position
000014                  213 SPARE14     DS      1X                 Spare byte position
000015                  214 SPARE15     DS      1X                 Spare byte position
000016                  215 SPARE16     DS      1X                 Spare byte position
000017                  216 SPARE17     DS      1X                 Spare byte position

                        218 *                                   REGISTER BANK 3 RAM BYTES 24-31
000018                  219 SPARE18     DS      1X                 Spare byte postion
000019                  220 SPARE19     DS      1X                 Spare byte postion
00001A                  221 SPARE1A     DS      1X                 Spare byte postion
00001B                  222 SPARE1B     DS      1X                 Spare byte postion
00001C                  223 SPARE1C     DS      1X                 Spare byte postion
00001D                  224 SPARE1D     DS      1X                 Spare byte postion
00001E                  225 SPARE1E     DS      1X                 Spare byte postion
00001F                  226 SPARE1F     DS      1X                 Spare byte postion
```

LOC OBJECT CODE ADDR1 ADDR2 STMT SOURCE STATEMENT ASM51 V1.9 07.09 05/09/86

```
                        229 ********************************************************************************
                        230 ********************************************************************************
                        231 *                                                                              *
                        232 * THE FOLLOWING DEFINE THE BIT ADDRESSABLE AREA OF INTERNAL RAM                *
                        233 *                                                                              *
                        234 ********************************************************************************
                        235 ********************************************************************************

                        237 ***                             MASTER STATUS BYTE

00000020                239 MSB         EQU     X'20'               MASTER STATUS BYTE
07  20.7                240 ASCFLAG     EQUB    X'20'.7             ASYNC INTERRUPT FLAG IN MSB
05  20.5                241 CMDCMPFL    EQUB    X'20'.5             NON ASYNC: COMMAND COMPLETE FLAG
05  20.5                242 ADDSTAT     EQUB    X'20'.5             ASYNC: ADDITIONAL STATUS FLAG
03  20.3                243 MBYTEFL     EQUB    X'20'.3             MB INDICATE FLAG
02  20.2                244 MDMCHGFL    EQUB    X'20'.2             NON ASYNC:MODEM INPUT TRANSITION
02  20.2                245 XMITCOMP    EQUB    X'20'.2             ASYNC: TRANSMIT COMPLETE FLAG
01  20.1                246 RECERRFL    EQUB    X'20'.1             RECEIVE ERROR FLAG
00  20.0                247 RCVCOMP     EQUB    X'20'.0             RECEIVE COMPLETE FLAG

                        249 ***                             Spare data byte (position X'21')

00000021                251 SPARE21     EQU     X'21'               Spare byte position

                        253 ***                             BYTE X'22' OPERATING MODE FLAG BYTE 0

17  22.7                255 CMDOVFLO    EQUB    X'22'.7             COMMAND STACK OVERFLOW FLAG
14  22.4                256 STINPROG    EQUB    X'22'.4             STATUS PASS IN PROGRESS FLAG
11  22.1                257 P2CMD       EQUB    X'22'.1             P2 CMD FLAG: 1=P2/0=P1 CMD

                        259 ***                             BYTE X'23' PORT 1 FLAGS

00000023                261 P2FLAGS2    EQU     X'23'               PORT 2 FLAGS BYTE 2

1F  23.7                263 HIVALIDB    EQUB    X'23'.7             HI DATA BYTE VALID FLAG CHAN B
1D  23.5                264 XMITBTC     EQUB    X'23'.5             XMIT CHAN B TC FLAG

                        266 ***                             BYTE X'24' PORT 1 FLAG BYTE 1

00000024                268 ASCFL1P1    EQU     X'24'               FLAG BYTE 1 PORT 1
23  24.3                269 MSPAREN1    EQUB    X'24'.3             MARK/SPACE PARITY ENABLE P1
22  24.2                270 MARKPAR1    EQUB    X'24'.2             +MARK/-SPACE PARITY P1
21  24.1                271 XONEN1      EQUB    X'24'.1             ENABLE XON CHECKING P1
20  24.0                272 ENXONOF1    EQUB    X'24'.0             ENABLE XON/XOFF HANDLING P1

                        274 ***                             BYTE X'25' PORT 2 FLAG BYTE 1

00000025                276 ASCFL1P2    EQU     X'25'               ASC FLAG BYTE 1 PORT 2
2B  25.3                277 MSPAREN2    EQUB    X'25'.3             MARK/SPACE PARITY ENABLE P2
2A  25.2                278 MARKPAR2    EQUB    X'25'.2             +MARK/-SPACE PARITY P2
29  25.1                279 XONEN2      EQUB    X'25'.1             ENABLE XON CHECKING P2
28  25.0                280 ENXONOF2    EQUB    X'25'.0             ENABLE XON/XOFF HANDLING P2
```

LOC OBJECT CODE ADDR1 ADDR2 STMT SOURCE STATEMENT ASM51 V1.9 07.09 05/09/86

```
                                282 ***                         BYTE X'26' OPERATING MODE ERROR BYTE 0

37  26.7                        284 TERMCNT     EQUB    X'26'.7             TEMP TERMINAL COUNT FLAG
31  26.1                        285 XSPECFL1    EQUB    X'26'.1             TEMP XMIT SPECIAL FLAG
30  26.0                        286 XSPECFL2    EQUB    X'26'.0             TEMP XMIT SPECIAL FLAG

                                288 ***                         BYTE X'27' P2 ASYNC UNIQUE FLAGS

00000027                        290 P2FLAGS1    EQU     X'27'               ASC UNIQUE FLAGS

3B  27.3                        292 STOPXMT2    EQUB    X'27'.3             ASC STOP XMIT FLAG
39  27.1                        293 SNDXON2     EQUB    X'27'.1             ASC SEND XON FLAG
38  27.0                        294 SNDXOFF2    EQUB    X'27'.0             ASC SEND XOFF FLAG

                                296 ***                         BYTE X'28' OPERATING MODE POLL ENABLES

00000028                        298 POLLEN      EQU     X'28'               POLL ENABLE BYTE
47  28.7                        299 P1ENXMIT    EQUB    X'28'.7             ENABLE PORT 1 XMIT POLL
46  28.6                        300 P1ENRCVR    EQUB    X'28'.6             ENABLE PORT 1 RECEIVE POLL
45  28.5                        301 P1ENMODM    EQUB    X'28'.5             ENABLE PORT 1 MODEM INTERRUPTS
43  28.3                        302 P2ENXMIT    EQUB    X'28'.3             ENABLE PORT 2 XMIT POLL
42  28.2                        303 P2ENRCVR    EQUB    X'28'.2             ENABLE PORT 2 RECEIVE POLL
41  28.1                        304 P2ENMODM    EQUB    X'28'.1             ENABLE PORT 2 MODEM INTERRUPTS

                                307 ***                         BYTE X'29' P1 ASYNC UNIQUE FLAGS

00000029                        309 P1FLAGS1    EQU     X'29'               PORT 1 FLAG BYTE 1

4B  29.3                        311 STOPXMT1    EQUB    X'29'.3             ASC STOP XMIT FLAG
49  29.1                        312 SNDXON1     EQUB    X'29'.1             ASC SEND XON FLAG
48  29.0                        313 SNDXOFF1    EQUB    X'29'.0             ASC SEND XOFF FLAG

                                315 ***                         BYTE X'2A' BIT ADDRESSABLE BYTE

0000002A                        317 P1FLAGS2    EQU     X'2A'               PORT 1 FLAG BYTE 2

57  2A.7                        319 HIVALIDA    EQUB    X'2A'.7             HI DATA BYTE VALID FLAG CHAN A
55  2A.5                        320 XMITATC     EQUB    X'2A'.5             XMIT CHAN A TC FLAG

                                322 ***                         BYTE X'2B' 8530 REG 0 SAVE BUFFER

0000002B                        324 REG08530    EQU     X'2B'               8530 REG 0 SAVE BUFFER
58  2B.0                        325 RXCHARIN    EQUB    X'2B'.0             RXCHAR IN FLAG
5A  2B.2                        326 TXBUFEMP    EQUB    X'2B'.2             TX BUFFER EMPTY FLAG
5F  2B.7                        327 BRKDET      EQUB    X'2B'.7             ASYNC BREAK DETECTED FLAG

                                329 ***                         BYTE X'2C' 8530 REG 1 SAVE BUFFER

0000002C                        331 REG18530    EQU     X'2C'               8530 REG 1 SAVE BUFFER
64  2C.4                        332 RPARERR     EQUB    X'2C'.4             PARITY ERROR DETECTED FLAG
65  2C.5                        333 ROVRUN      EQUB    X'2C'.5             RECV OVERRUN FLAG
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
66  2C.6                          334 RFRMERR    EQUB    X'2C'.6             RECV FRAMING ERROR FLAG

                                  336 ***                        BYTE X'2D' BIT ADDRESSABLE BYTE

6E  2D.6                          338 BRKFLG1    EQUB    X'2D'.6             RECV BREAK DETECTED FLAG
6D  2D.5                          339 BRKFLG2    EQUB    X'2D'.5             RECV BREAK DETECTED FLAG

                                  341 ***                        BYTE X'2E' XMIT CHAN A COMMAND BUFFER

0000002E                          343 XMITACMD   EQU     X'2E'               XMIT CHAN A CMD BUFFER
75  2E.5                          344 TRASHFA    EQUB    X'2E'.5             DISCARD FIRST BYTE
74  2E.4                          345 TRASHLA    EQUB    X'2E'.4             DISCARD LAST BYTE

                                  347 ***                        BYTE X'2F' XMIT CHAN B COMMAND BUFFER

0000002F                          349 XMITBCMD   EQU     X'2F'               XMIT CHAN B CMD BUFFER
7D  2F.5                          350 TRASHFB    EQUB    X'2F'.5             DISCARD FIRST BYTE
7C  2F.4                          351 TRASHLB    EQUB    X'2F'.4             DISCARD LAST BYTE

000020                            354 BITADDR    DS      16X                 16 BYTES OF BIT ADDR'B RAM
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                    356 ************************************************************************
                                    357 ************************************************************************
                                    358 **                                                                    **
                                    359 **                BYTE ADDRESSABLE 8051 INTERNAL RAM                  **
                                    360 **                                                                    **
                                    361 ************************************************************************
                                    362 ************************************************************************

                                    364 *                              RAM BYTES 48-63 (X'30' - X'3F')
000030                              365 LODMA       DS      1X                 DMA DATA PASSING BUFFER
000031                              366 HIDMA       DS      1X                 DMA DATA PASSING BUFFER
000032                              367 HIXBYTEA    DS      1X                 CHAN A HI DMA DATA BUFFER
000033                              368 HIXBYTEB    DS      1X                 CHAN B HI DMA DATA BUFFER
000034                              369 XMTMSK1     DS      1X                 ASYNC XMIT BIT SET MASK (P1)
000035                              370 XMTMSK2     DS      1X                 ASYNC XMIT BIT SET MASK (P2)
000036                              371 RSTPMSK1    DS      1X                 ASYNC RECV NON DATA BIT MSK 1
000037                              372 RSTPMSK2    DS      1X                 ASYNC RECV NON DATA BIT MSK 2
000038                              373 ASCFL2P1    DS      1X                 ASC PARMS SAVE BUFFER
000039                              374 ASCFL2P2    DS      1X                 ASC PARMS SAVE BUFFER
00003A                              375 STAT0       DS      1X                 STATUS PASSING BYTE 0
00003B                              376 STAT1       DS      1X                 STATUS PASSING BYTE 1
00003C                              377 STATCNT     DS      1X                 STATUS PASS BRANCH CTL BYTE
00003D                              378 MBYTBUF     DS      1X                 MB CMD SAVE BUFFER
00003E                              379 SPARE3E     DS      1X                 Spare byte position
00003F                              380 RAMEND      DS      1X                 Hi byte of addr of end of RAM

                                    382 *                              RAM BYTES 64-71 (X'40' - X'47')
                                    383 *                                MODEM INTERFACE VALUES AND MASKS
000040                              384 MDMREG1A    DS      1X                 PORT 1 NEWEST MODEM VALUE
000041                              385 MDMREG1B    DS      1X                 P1 MODEM REG NEXT OLDEST VALUE
000042                              386 MDMREG1C    DS      1X                 P1 MODEM REG OLDEST VALUE
000043                              387 MDMREG2A    DS      1X                 PORT 2 NEWEST MODEM VALUE
000044                              388 MDMREG2B    DS      1X                 P2 MODEM REG NEXT OLDEST VALUE
000045                              389 MDMREG2C    DS      1X                 P2 MODEM REG OLDEST VALUE
000046                              390 MODMMSK1    DS      1X                 PORT 1 MODEM INPUT MASK BUFFER
000047                              391 MODMMSK2    DS      1X                 PORT 2 MODEM INPUT MASK BUFFER

                                    393 *                              RAM BYTES 72-79 (X'48' - X'4F')
                                    394 *                                XON / XOFF CODES
000048                              395 XOFFRCV1    DS      1X                 XOFF COMPARE VALUE
000049                              396 XONRCV1     DS      1X                 XON COMPARE VALUE
00004A                              397 XOFFXMT1    DS      1X                 XOFF XMIT VALUE
00004B                              398 XONXMT1     DS      1X                 XON XMIT VALUE
00004C                              399 XOFFRCV2    DS      1X                 XOFF COMPARE VALUE
00004D                              400 XONRCV2     DS      1X                 XON COMPARE VALUE
00004E                              401 XOFFXMT2    DS      1X                 XOFF XMIT VALUE
00004F                              402 XONXMT2     DS      1X                 XON XMIT VALUE
```

```
SASC     Sample MP ASC Microcode                                                                    PAGE   12

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86

                                   405 *                                 RAM BYTES 80-85 (X'50' - X'55')
000050                             406 R3A8530S   DS      1X                      REGISTER SAVE BUFFER
000051                             407 R5A8530S   DS      1X                      REGISTER SAVE BUFFER
000052                             408 RAA8530S   DS      1X                      REGISTER SAVE BUFFER
000053                             409 R3B8530S   DS      1X                      REGISTER SAVE BUFFER
000054                             410 R5B8530S   DS      1X                      REGISTER SAVE BUFFER
000055                             411 RAB8530S   DS      1X                      REGISTER SAVE BUFFER

                                   413 *                                 RAM BYTES 56-7F

000056                             415 STACKBEG   DS     42X                      STACK AREA
```

```
SASC     Sample MP ASC Microcode                                                                    PAGE   13

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86

                                   419 * ENTRY POINTS INTO RAM MICROCODE FROM ROM

00002001                           421 POLLOOP    EQU     X'2001'                 POLL LOOP STARTING ADDRESS
00002003                           422 HNDLINT0   EQU     X'2003'                 INT0 SERV RTN START ADDRESS
00002006                           423 HNDLINT1   EQU     X'2006'                 INT1 SERV RTN START ADDRESS
00002009                           424 HNDLTIM0   EQU     X'2009'                 TIM0 SERV RTN START ADDRESS
0000200C                           425 HNDLTIM1   EQU     X'200C'                 TIM1 SERV RTN START ADDRESS
```

```
SASC     Sample MP ASC Microcode                                                                    PAGE   14

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86

                                   428 ********************************************************************************
                                   429 **                                                                            **
                                   430 **  ROUTINE NAME:  POLL                                                       **
                                   431 **                                                                            **
                                   432 **  DESCRIPTIVE NAME:  POLL LOOP                                              **
                                   433 **                                                                            **
                                   434 ********************************************************************************
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                    436 ************************************************************************
                                    437 **                                                                    **
                                    438 **         Definition of Entry Points from ROM                        **
                                    439 **                                                                    **
                                    440 ************************************************************************
000000                              441 SASC        CSECT


                                    444 *                   Pad byte to align first entry point at RAM addr.
                                    445 *                    X'2001' after IPL completion.

000000 00                           447             NOP                         PAD BYTE FOR ALIGNMENT

                                    449 *                   St_ex Entry Point.  This is the address that will
                                    450 *                    receive control when the ROM 'Start Execution'
                                    451 *                    command is executed. (Must be at absolute addr.
                                    452 *                    '20A1'H after program IPL).

000001 800C         000F            454             SJMP    POLLINIT            JUMP TO POLL LOOP INITIALIZATION

                                    456 *                   INT 0 Entry Point.  This is the address that will
                                    457 *                    receive control when an interrupt occurs on the
                                    458 *                    8051's interrupt level 0 (Absolute addr. '2003'H).

000003 0206B6       06B6            460             LJMP    SERVINT0            JUMP TO HW INTR 0 SER. ROUTINE

                                    462 *                   INT 1 Entry Point.  This is the address that will
                                    463 *                    receive control when an interrupt occurs on the
                                    464 *                    8051's interrupt level 1 (Absolute addr. '2006'H).

000006 0206D5       06D5            466             LJMP    SERVINT1            JUMP TO HW INTR 1 SER. ROUTINE

                                    468 *                   TMR 0 Entry Point.  This is the address that will
                                    469 *                    receive control when the 8051's internal timer 0
                                    470 *                    expires (Absolute addr. '2009'H).

000009 22                           472             RET                         RETURN, HW TMR 0 NOT USED
00000A 00                           473             NOP                         PAD FOR ALIGNMENT
00000B 00                           474             NOP                         PAD FOR ALIGNMENT

                                    476 *                   TMR 1 Entry Point.  This is the address that will
                                    477 *                    receive control when the 8051's internal timer 1
                                    478 *                    expires (Absolute addr. '200C'H).

00000C 22                           480             RET                         RETURN, HW TMR 1 NOT USED
00000D 00                           481             NOP                         PAD FOR ALIGNMENT
00000E 00                           482             NOP                         PAD FOR ALIGNMENT
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                    484 ************************************************************************
                                    485 **                                                                    **
                                    486 **          OPERATING MODE INITIALIZATION AFTER LEAVING ROM MODE      **
                                    487 **                                                                    **
                                    488 ************************************************************************

00000F 7808                   08    490 POLLINIT    MOV     R0,#CMDST0          INIT COMMAND STACK POINTER
000011 7908                   08    491             MOV     R1,#CMDST0          INIT COMMAND EXEC POINTER
000013 7A00                   00    492             MOV     CMDCNT,#0           INIT CMD COUNT VALUE TO 0
000015 752800                 28    00  493             MOV     POLLEN,#0           INIT POLL ENABLE TO ALL OFF
000018 752900                 29    00  494             MOV     P1FLAGS1,#0         INIT P1 FLAGS 1 TO ALL OFF
00001B 752A00                 2A    00  495             MOV     P1FLAGS2,#0         INIT P1 FLAGS 2 TO ALL OFF
00001E 752700                 27    00  496             MOV     P2FLAGS1,#0         INIT P2 FLAGS 1 TO ALL OFF
000021 752300                 23    00  497             MOV     P2FLAGS2,#0         INIT P2 FLAGS 2 TO ALL OFF
000024 758155                 81    55  498             MOV     SP,#STACK           INITIALIZE STACK POINTER
000027 C214                 22.4        499             CLR     STINPROG            CLEAR STATUS PASS IN PROG FLAG
000029 7583A0                 83    A0  500             MOV     DPH,#ADRMDM1        SET UP TO READ MODEM INPUTS, P1
00002C E0                             501             MOVX    A,@DPTR             EXECUTE THE I/O READ
00002D F540                   40      502             MOV     MDMREG1A,A          INITIALIZE P1 MDMREGA
00002F F541                   41      503             MOV     MDMREG1B,A          INITIALIZE P1 MDMREGB
000031 F542                   42      504             MOV     MDMREG1C,A          INITIALIZE P1 MDMREGC
000033 7583C0                 83    C0  505             MOV     DPH,#ADRMDM2        SET UP TO READ MODEM INPUTS, P2
000036 E0                             506             MOVX    A,@DPTR             EXECUTE THE I/O READ
000037 F543                   43      507             MOV     MDMREG2A,A          INITIALIZE P2 MDMREGA
000039 F544                   44      508             MOV     MDMREG2B,A          INITIALIZE P2 MDMREGB
00003B F545                   45      509             MOV     MDMREG2C,A          INITIALIZE P2 MDMREGC
00003D D2A8                 A8.0      510             SETBIT  EX0                 ENABLE INT0 INTERRUPTS
00003F D2AF                 A8.7      511             SETBIT  EA                  ENABLE INTERRUPTS (GLOBAL)

                                    513 *                           The following bit set asserts a status
                                    514 *                            bit that is visable to the system pro-
                                    515 *                            cessor (via I/O read).  This bit is used
                                    516 *                            to indicate that the adapter processor
                                    517 *                            has completed its initialization and
                                    518 *                            is ready to accept additional commands
                                    519 *                            that will be executed by the RAM pro-
                                    520 *                            gram.

000041 D295                 90.5    522             SETBIT  IPLCOMP             SET 'POLL ACTIVE' FLAG TO SYSTEM
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86

                                   524 ************************************************************************
                                   525 **                                                                    **
                                   526 **          POLL 8530 CHAN A TO SEE IF SERVICE IS REQUIRED            **
                                   527 **                                                                    **
                                   528 ************************************************************************

000043 758398          83    98    530 POLLTOP     MOV     DPH,#H8530A          SET UP MOVX HI ADDR 8530
000046 758201          82    01    531             MOV     DPL,#L8530A          SET UP MOVX LO ADDR 8530
000049 E0                          532             MOVX    A,@DPTR              READ 8530 REG A0 INTO ACC
00004A F52B            2B          533             MOV     REG08530,A           STORE 8530 REG 0
00004C 30461B        2B.6  006A    534             JNB     P1ENRCVR,RCOMPA      JMP IF POLL IS DISABLED
00004F 205F0E        2B.7  0060    535             JB      BRKDET,RDREG1        JMP 8530 RCV BRK BIT IS ON
000052 306E08        2D.6  005D    536             JNB     BRKFLG1,CHKCHAR1     JMP IF BRK FLAG NOT ON
000055 C26E          2D.6          537             CLR     BRKFLG1              CLEAR BREAK ACTIVE FLAG
000057 758203          82    03    538             MOV     DPL,#L8530AD         SET UP MOVX LO DATA ADDR 8530
00005A E0                          539             MOVX    A,@DPTR              RD/DISCARD 8530 DATA BYTE
00005B 800D            006A        540             SJMP    RCOMPA               JMP TO CHK XMIT BUF EMPTY
00005D 30580A        2B.0  006A    541 CHKCHAR1    JNB     RXCHARIN,RCOMPA      JMP IF NO RX CHAR IS AVAILABLE

                                   543 * CHAN A HAS A RECV CHAR AVAILABLE, READ 8530 REG 1 FOR STATUS

000060 7401                  01    545 RDREG1      MOV     A,#R1A8530           SET UP MOVX READ PTR ADDR
000062 F0                          546             MOVX    @DPTR,A              SET UP 8530 PTR REGISTER
000063 00                          547             NOP                          DUMMY WAIT FOR 8530
000064 E0                          548             MOVX    A,@DPTR              READ 8530 REG A1 INTO ACC
000065 F52C            2C          549             MOV     REG18530,A           STORE 8530 REG 0

                                   551 * CALL CHANNEL A RECEIVE HANDLER

000067 120138          0138        553             LCALL   RECVA                CALL RTN TO HANDLE RCV'D BYTE
00006A 304706        2B.7  0073    554 RCOMPA      JNB     P1ENXMIT,POLLCHB     JMP IF TX POLL IS DISABLED
00006D 305A03        2B.2  0073    555             JNB     TXBUFEMP,POLLCHB     JMP IF TX BUFFER IS NOT EMPTY

                                   557 * CALL CHANNEL A TRANSMIT HANDLER

000070 1201BA          01BA        559             LCALL   XMITA                CALL RTN TO HNDL XMIT SERVICE
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                    561 ************************************************************************
                                    562 **                                                                    **
                                    563 **          POLL 8530 CHAN B TO SEE IF SERVICE IS REQUIRED            **
                                    564 **                                                                    **
                                    565 ************************************************************************

000073 758398          83    98     567 POLLCHB     MOV     DPH,#H8530B         SET UP MOVX HI ADDR 8530
000076 758200          82    00     568             MOV     DPL,#L8530B         SET UP MOVX LO ADDR 8530
000079 E0                           569             MOVX    A,@DPTR             READ 8530 REG B0 INTO ACC
00007A F52B             2B          570             MOV     REG08530,A          STORE 8530 REG 0
00007C 30421B        28.2  009A     571             JNB     P2ENRCVR,RCOMPB     JMP IF RX POLL IS DISABLED
00007F 205F0E        2B.7  0090     572             JB      BRKDET,RDREG2       JMP 8530 RCV BRK BIT IS ON
000082 306D08        2D.5  008D     573             JNB     BRKFLG2,CHKCHAR2    JMP IF BRK FLAG NOT ON
000085 C26D          2D.5           574             CLR     BRKFLG2             CLEAR BREAK ACTIVE FLAG
000087 758202          82    02     575             MOV     DPL,#L8530BD        SET UP MOVX LO DATA ADDR 8530
00008A E0                           576             MOVX    A,@DPTR             RD/DISCARD 8530 DATA BYTE
00008B 800D             009A        577             SJMP    RCOMPB              JMP TO CHK XMIT BUF EMPTY
00008D 30580A        2B.0  009A     578 CHKCHAR2    JNB     RXCHARIN,RCOMPB     JMP IF NO RX CHAR IS AVAILABLE

                                    580 * CHAN B HAS A RECV CHAR AVAILABLE, CHECK FOR ANY RECV ERRORS

000090 7401                   01    582 RDREG2      MOV     A,#R1B8530          SET UP MOVX READ PTR ADDR
000092 F0                           583             MOVX    @DPTR,A             SET UP 8530 PTR REGISTER
000093 00                           584             NOP                         DUMMY WAIT FOR 8530
000094 E0                           585             MOVX    A,@DPTR             READ 8530 REG B1 INTO ACC
000095 F52C             2C          586             MOV     REG18530,A          STORE 8530 REG 0

                                    588 * CALL CHANNEL B RECEIVE HANDLER

000097 120276           0276        590             LCALL   RECVB               CALL RTN TO HANDLE RCV'D BYTE

                                    592 * CHECK FOR CHAN A TX BUFFER EMPTY

00009A 304306        28.3  00A3     594 RCOMPB      JNB     P2ENXMIT,POLLCMDS   JMP IF TX POLL IS DISABLED
00009D 305A03        2B.2  00A3     595             JNB     TXBUFEMP,POLLCMDS   JMP IF TX BUFFER IS NOT EMPTY

                                    597 * CALL CHANNEL B TRANSMIT HANDLER

0000A0 1202FA           02FA        599             LCALL   XMITB               CALL RTN TO HNDL XMIT SERVICE
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                    601 ************************************************************************
                                    602 **                                                                    **
                                    603 **          CHECK TO SEE IF A SYSTEM COMMAND IS ON THE CMD STACK      **
                                    604 **                                                                    **
                                    605 ************************************************************************

0000A3 BA0003          00   00A9    607 POLLCMDS    CJNE    CMDCNT,#0,HNDLCMD   JMP IF THER IS A COMMAND
0000A6 0200CB        00CB           608             LJMP    CHKMDM1             NO CMD, JMP TO CHK MODEM P1

                                    610 * AT LEAST ONE COMMAND IS ON THE STACK

0000A9 C211          22.1           612 HNDLCMD     CLR     P2CMD               CLEAR P2 INDICATOR FLAG
0000AB C2AF          A8.7           613             CLR     EA                  DISABLE ALL INTERRUPTS

                                    615 * CHECK IF A COMMAND OVERFLOW CONDITION IS ACTIVE

0000AD 301716        22.7   00C6    617             JNB     CMDOVFLO,EXECCMD    JUMP IF CMD OVERFLO NOT ON
0000B0 BA0802          08   00B5    618             CJNE    CMDCNT,#X'08',NOTFULL JMP IF CMD STACK NOT FULL

                                    620 * A COMMAND OVERFLOW IS ACTIVE AND THE CMD STACK IS STILL FULL
                                    621 * SO LEAVE IT IN THE SYSTEM BUFFER

0000B3 8011          00C6           623             SJMP    EXECCMD             JUMP TO HANDLE TOP COMMAND

                                    625 * A COMMAND OVERFLOW IS ACTIVE AND THE CMD STACK IS NOT FULL
                                    626 * SO MOVE THE COMMAND ONTO THE CMD STACK

0000B5 758390          83     90    628 NOTFULL     MOV     DPH,#ADR8255        ELSE RD CMD, SET UP MOVX ADDR
0000B8 E0                          629             MOVX    A,@DPTR             MOVE COMMAND INTO ACC
0000B9 F7                          630             MOV     @R1,A               MOVE COMMAND ONTO CMD STACK
0000BA 09                          631             INC     CMDSTPTR            INCR CMD STACK PTR
0000BB 740F                  0F    632             MOV     A,#CMDST7           MOVE ADDR OF TOP OF STK TO ACC
0000BD 2401                  01    633             ADD     A,#X'01'            ADD 1 TO THE ADDR
0000BF 99                          634             SUBB    A,CMDSTPTR          SUB ST TPR FROM TOP OF STK +1
0000C0 7002          00C4          635             JNZ     END1                JMP IF ROLL OVER NOT TO BE DONE
0000C2 7908                  08    636             MOV     CMDSTPTR,#CMDST0    ROLL CMD PTR BACK TO BOT OF STK
0000C4 C217          22.7          637 END1        CLR     CMDOVFLO            CLEAR CMD OVERFLOW FLAG
0000C6 D2AF          A8.7          638 EXECCMD     SETBIT  EA                  ENABLE INTERRUPTS
0000C8 1203BA        03BA          639             LCALL   OPCMDDCD            CALL OPERATING MODE CMD DECODER
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                    641 ************************************************************************
                                    642 **                                                                    **
                                    643 **  CHECK TO SEE IF AN INTERFACE TRANSITION HAS OCCURRED FOR PORT 1    **
                                    644 **                                                                    **
                                    645 ************************************************************************


                                    648 * Poll the modem interface register for adapter port 1 to see if
                                    649 *   a modem input as changed state.  Interrupt if a stable state
                                    650 *   change is indicated and P1 modem interrupts are enabled.

0000CB 7583A0          83    A0     652 CHKMDM1     MOV     DPH,#ADRMDM1          SET UP TO READ MODEM P1
0000CE E0                           653             MOVX    A,@DPTR               PERFORM THE I/O READ
0000CF F540            40           654             MOV     MDMREG1A,A            SAVE THE DATA IN MDM REG A
0000D1 B54105          41   00D9    655             CJNE    A,MDMREG1B,CHKMDM1A SEE IF REG A = REG B
0000D4 B54207          42   00DE    656             CJNE    A,MDMREG1C,CHKMDM1B SEE IF REG A = REG C
0000D7 8026          00FF          657             SJMP    CHKMDM2               EVERYBODY EQUAL (NO MDM CHANGES)
0000D9 854041          41    40     658 CHKMDM1A    MOV     MDMREG1B,MDMREG1A     A NOT = B, SAVE A TO B
0000DC 8021          00FF          659             SJMP    CHKMDM2               CHECK FOR P2 MODEM CHANGES
0000DE 30451B        28.5  00FC     660 CHKMDM1B    JNB     P1ENMODM,CHKMDM1D     JMP IF P1 MDM INTRS NOT ENABLED
0000E1 E540                 40     661             MOV     A,MDMREG1A            RETRIEVE I/O READ DATA
0000E3 6542                 42     662             XRL     A,MDMREG1C            EX. OR TO ISOLATE CHANGED BITS
0000E5 5546                 46     663             ANL     A,MODMMSK1            AND OFF UNINTERESTING BITS
0000E7 B40002          00   00EC     664             CJNE    A,#X'00',CHKMDM1C     ANYTHING LEFT ?
0000EA 8010          00FC          665             SJMP    CHKMDM1D              NO, PREPARE TO GO ON TO CHK P2
0000EC 2014FD        22.4  00EC     666 CHKMDM1C    JB      STINPROG,CHKMDM1C     WAIT FOR OK TO PASS STATUS
0000EF D202          20.2          667             SETBIT  MDMCHGFL              SET UP MASTER STATUS BYTE
0000F1 85403A          3A    40     668             MOV     STAT0,MDMREG1A        SECOND BYTE GETS CURRENT MDM STS
0000F4 F53B            3B           669             MOV     STAT1,A               THIRD BYTE GETS DELTA BIT MASK
0000F6 753C02          3C    02     670             MOV     STATCNT,#TWOBYTE      MSB PLUS TWO ADD'L STS BYTES
0000F9 1206A6        06A6          671             LCALL   INTRSYS               INTERRUPT THE SYSTEM
0000FC 854042          42    40     672 CHKMDM1D    MOV     MDMREG1C,MDMREG1A     COPY NEW STABLE VALUE TO REG C
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                    674 ********************************************************************************
                                    675 **                                                                            **
                                    676 **  CHECK TO SEE IF AN INTERFACE TRANSITION HAS OCCURRED FOR PORT 2            **
                                    677 **                                                                            **
                                    678 ********************************************************************************

                                    681 * Poll the modem interface register for adapter port 2 to see if
                                    682 *   a modem input as changed state.  Interrupt if a stable state
                                    683 *   change is indicated and P2 modem interrupts are enabled.

0000FF 7583C0         83    C0      685 CHKMDM2     MOV     DPH,#ADRMDM2          SET UP TO READ MODEM P2
000102 E0                           686             MOVX    A,@DPTR               PERFORM THE I/O READ
000103 F543             43          687             MOV     MDMREG2A,A            SAVE THE DATA IN MDM REG A
000105 B54405           44  010D    688             CJNE    A,MDMREG2B,CHKMDM2A   SEE IF REG A = REG B
000108 B54507           45  0112    689             CJNE    A,MDMREG2C,CHKMDM2B   SEE IF REG A = REG C
00010B 8028           0135          690             SJMP    POLLDONE              EVERYBODY EQUAL (NO MDM CHANGES)
00010D 854344           44    43    691 CHKMDM2A    MOV     MDMREG2B,MDMREG2A     A NOT = B, SAVE A TO B
000110 8023           0135          692             SJMP    POLLDONE              GO BACK TO TOP OF POLL LOOP
000112 30411D         28.1  0132    693 CHKMDM2B    JNB     P2ENMODM,CHKMDM2D     JMP IF P2 MDM INTRS NOT ENABLED
000115 E543                 43      694             MOV     A,MDMREG2A            RETRIEVE I/O READ DATA
000117 6545                 45      695             XRL     A,MDMREG2C            EX. OR TO ISOLATE CHANGED BITS
000119 5547                 47      696             ANL     A,MODMM5K2            AND OFF UNINTERESTING BITS
00011B B40002           00  0120    697             CJNE    A,#X'00',CHKMDM2C     ANYTHING LEFT ?
00011E 8012           0132          698             SJMP    CHKMDM2D              NO, PREPARE TO GO ON TO CHK P2
000120 2014FD         22.4  0120    699 CHKMDM2C    JB      STINPROG,CHKMDM2C     WAIT FOR OK TO PASS STATUS
000123 D202           20.2          700             SETBIT  MDMCHGFL              SET UP MASTER STATUS BYTE
000125 D2B4           B0.4          701             SETBIT  P1P2INTR              SET UP MASTER STATUS BYTE
000127 85433A           3A    43    702             MOV     STAT0,MDMREG2A        SECOND BYTE GETS CURRENT MDM STS
00012A F53B             3B          703             MOV     STAT1,A               THIRD BYTE GETS DELTA BIT MASK
00012C 753C02           3C    02    704             MOV     STATCNT,#TWOBYTE      MSB PLUS TWO ADD'L STS BYTES
00012F 1206A6         06A6          705             LCALL   INTRSYS               INTERRUPT THE SYSTEM
000132 854345           45    43    706 CHKMDM2D    MOV     MDMREG2C,MDMREG2A     COPY NEW STABLE VALUE TO REG C

000135 020043         0043          709 POLLDONE    LJMP    POLLTOP               RETURN TO TOP OF POLL LOOP
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                    712 ************************************************************************
                                    713 *                                                                      *
                                    714 *    CHANNEL A ASYNC RECV SERVICE                                      *
                                    715 *                                                                      *
                                    716 ************************************************************************

                                    718 *    CHECK FOR ANY RECEIVE ERRORS

000138 758203          82    03     720 RECVA       MOV     DPL,#L8530AD        SET LO 8530 DATA ADDRESS
                                    721 * 8530 READ REG 1 IS CURRENTLY IN THE ACC, CHECK FOR ERROR BITS ON
00013B 5470                 70     722             ANL     A,#X'70'            ZERO NON-ASC ERROR BITS
00013D 6003          0142           723             JZ      CHKBRK              JUMP IF NO ERROR BITS ARE ON
00013F 020181        0181           724             LJMP    RERROR1             JMP TO ERROR HANDLER
000142 305F03        2B.7  0148     725 CHKBRK      JNB     BRKDET,NOERROR1     JUMP BREAK DETECT FLAG IS NOT ON
000145 020181        0181           726             LJMP    RERROR1             JMP TO ERROR HANDLER

                                    728 *    NO 8530 DETECTED ERRORS SO READ DATA BYTE FROM THE 8530
                                    729 *    THE DATA POINTER VALUE IS ALREADY SET UP

000148 E0                           731 NOERROR1    MOVX    A,@DPTR             READ THE DATA BYTE TO ACC

                                    733 *
                                    734 *
000149 5536                 36     735             ANL     A,RSTPM5K1          STRIP OFF ALL NON DATA BITS
                                    736 *
                                    737 *
                                    738 *    CHECK IF THE XON/XOFF HANDLING IS ENABLED

00014B 302023        24.0  0171     740             JNB     ENXONOF1,WAITLP2    JUMP IF XON/OFF HNDL DISABLED

                                    742 *    CHECK IF THE CHARACTER IS XOFF OR XON

00014E B54A0D          4A  015E     744             CJNE    A,XOFFXMT1,TESTXON1 JUMP IF CHAR IS NOT XOFF

                                    746 *    RECEIVE CHARACTER WAS AN XOFF CHAR
000151 304702        28.7  0156     747             JNB     P1ENXMIT,WAITLP0    JUMP IF TRANSMITTER NOT ENABLED
000154 D24B          29.3           748             SETBIT  STOPXMT1            SET FLAG TO STOP TRANSMITTING
000156 2014FD        22.4  0156     749 WAITLP0     JB      STINPROG,WAITLP0    LOOP UNTIL STAT PASS IS CLEAR
000159 753B10           3B   10     750             MOV     STAT1,#XOFFSTAT     SET XOFF RECV'D FLAG IN STAT1
00015C 800C          016A           751             SJMP    PASSX1              JMP TO PASS STATUS

00015E 302110        24.1  0171     753 TESTXON1    JNB     XONEN1,WAITLP2      JUMP IF XON CHECKING NOT ENABLED
000161 B54B0D          4B  0171     754             CJNE    A,XONXMT1,WAITLP2   JUMP IF CHAR IS NOT XON

                                    756 *    RECEIVE CHARACTER WAS AN XON CHAR

000164 2014FD        22.4  016(     753 WAITLP1     JB      STINPROG,WAITLP1    LOOP UNTIL STAT PASS IS CLEAR
000167 753B20           3B   20     759             MOV     STAT1,#XONSTAT      SET XON RECV'D FLAG IN STAT1
00016A D205          20.5           760 PASSX1      SETBIT  ADDSTAT             SET MSB ADDITIONAL STAT FLAG
00016C 753C02           3C   02     761             MOV     STATCNT,#TWOBYTE    LOAD STATUS CNT FOR TWO BYTES
00016F 8006          0177           762             SJMP    PASSRCV1            JMP TO COMPLETE STAT PASS

                                    764 ************************************************************************
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                   765 **                                                                    **
                                   766 **          RETURN DATA BYTE TO SYSTEM                                **
                                   767 **                                                                    **
                                   768 ************************************************************************

                                   770 *     CHARACTER WAS NOT XOFF OR XON SO JUST PASS IT TO THE SYSTEM

000171 2014FD          22.4  0171  772 WAITLP2     JB       STINPROG,WAITLP2     LOOP UNTIL STAT PASS IS CLEAR
000174 753C01            3C    01  773             MOV      STATCNT,#ONEBYTE     LOAD STATUS CNT FOR ONE BYTE
000177 D200            20.0        774 PASSRCV1    SETBIT   RCVCOMP              SET RECV COMP FLG IN MSB
000179 D207            20.7        775             SETBIT   ASCFLAG              SET MSB ASC FLAG
00017B F53A              3A        776             MOV      STAT0,A              MOVE DATA CHAR TO STAT0 BYTE
                                   777 ************************************************************************
                                   778 **                                                                    **
                                   779 **        WRITE THE MSB INTO THE 8255 AND CAUSE A SYSTEM INTERRUPT    **
                                   780 **                                                                    **
                                   781 ************************************************************************

00017D 1206A6          06A6        783             LCALL    INTRSYS              GENERATE CHAR. RX INTERRUPT
000180 22                          784 ENDRECV1    RET                           RETURN TO CALLING ROUTINE
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86

                                   786 ************************************************************************
                                   787 **                                                                    **
                                   788 **   A RECEIVE ERROR WAS DETECTED BY THE 8530                         **
                                   789 **                                                                    **
                                   790 ************************************************************************

000181 E0                          792 RERROR1     MOVX    A,@DPTR             READ THE DATA BYTE TO ACC
000182 5536                   36   793             ANL     A,RSTPM5K1          STRIP OFF ALL NON DATA BITS
000184 2014FD          22.4   0184  794 WAITLP3     JB      STINPROG,WAITLP3    LOOP TILL STAT PASS IS CLEAR
000187 306505          2C.5   018F  795             JNB     ROVRUN,CHEKBRK1     JUMP IF NOT AN OVERRUN ERROR
00018A 753B01            3B     01  796             MOV     STAT1,#OVRSTAT      RET OVERRUN ERROR STATUS
00018D 8010            01AB         797             SJMP    RASSERR1            JMP TO PASS STATUS
00018F 305F0E          2B.7   01A0  798 CHEKBRK1    JNB     BRKDET,CHKPAR1      JUMP IF NOT A BREAK RECEIVED
000192 306E02          2D.6   0197  799             JNB     BRKFLG1,RPTBRK1     JMP IF BREAK HAS NOT BEEN RPTD
000195 80E9            0180         800             SJMP    ENDRECV1            BRK PREVIOUSLY RPTD, BAILOUT
000197 D26E            2D.6         801 RPTBRK1     SETBIT  BRKFLG1             SET BREAK DETECTED FLAG
000199 7400                   00    802             MOV     A,#BRKDATA          FORCE DATA BYTE TO '00'H
00019B 753B08            3B     08  803             MOV     STAT1,#XBRKSTAT     RET BREAK DETECTED STATUS
00019E 800B            01AB         804             SJMP    PASSERR1            JMP TO PASS STATUS
0001A0 306405          2C.4   01A8  805 CHKPAR1     JNB     RPARERR,FRMERR1     JUMP IF NOT A PARITY ERROR
0001A3 753B02            3B     02  806             MOV     STAT1,#PARESTAT     RET PARITY ERROR STATUS
0001A6 8003            01AB         807             SJMP    PASSERR1            JMP TO PASS STATUS
0001A8 753B04            3B     04  808 FRMERR1     MOV     STAT1,#FRMESTAT     RET FRAMING ERROR STATUS

                                   810 *    ANY RECEIVE ERROR SHOULD JMP TO HERE

0001AB C0E0              E0        812 PASSERR1    PUSH    ACC                 SAVE ACC

0001AD 758201            82     01 814             MOV     DPL,#L8530A         SET LO 8530 DATA ADDRESS

                                   816 *    SEND RESET COMMAND TO 8530

0001B0 7430                   30   818             MOV     A,#X'30'            MOVE ERROR RESET CMD TO ACC
0001B2 F0                         819             MOVX    @DPTR,A             WRITE ERROR RESET TO 8530
0001B3 D0E0              E0       820             POP     ACC                 RESTORE ACC
0001B5 D201            20.1       821             SETBIT  RECERRFL            SET MSB RECEIVE ERROR FLAG
0001B7 02016A          016A       822             LJMP    PASSX1              JMP TO PASS STATUS
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                    825 ************************************************************************
                                    826 **                                                                    **
                                    827 **   CHANNEL A ASYNC XMIT SERVICE                                     **
                                    828 **                                                                    **
                                    829 ************************************************************************

                                    831 * IF HIVALID IS ON, THIS IS NOT THE FIRST TRANSFER

0001BA 758398          83    98     833 XMITA       MOV     DPH,#H8530A         SET UP DATA POINTER
0001BD 758201          82    01     834             MOV     DPL,#L8530A         SET UP DATA POINTER
0001C0 305709        2A.7  01CC     835             JNB     HIVALIDA,INVALID1   JMP IF HI DMA BYTE IS NOT VALID

                                    837 *    THE HI DMA DATA BYTE IS VALID SO PASS IT TO THE 8530            *

0001C3 C257          2A.7           839             CLR     HIVALIDA            CLEAR VALID DATA FLAG
0001C5 C275          2E.5           840             CLR     TRASHFA             CLEAR TRASH FIRST BYTE FLAG
0001C7 E532              32         841             MOV     A,HIXBYTEA          MOV HI DMA DATA BYTE TO XMIT BUF
0001C9 02024C          024C         842             LJMP    SENDBYT1            JMP TO XMIT BYTE OF DATA
                                    843 *    THE HI DMA DATA BYTE IS NOT VALID SO CHECK FOR SPECIAL SITUATIONS
                                    844 *    THERE IS NO DATA FOR THE 8530 ON THE CARD AT THIS TIME

0001CC 304B05        29.3  01D4     846 INVALID1    JNB     STOPXMT1,CHKXON1    JMP IF STOP XMIT FLAG IS OFF
0001CF C24B          29.3           847             CLR     STOPXMT1            CLEAR STOP XMIT FLAG
0001D1 C247          28.7           848             CLR     P1ENXMIT            CLEAR P1 POLL ENABLE FLAG
0001D3 22                           849             RET                         RETURN TO POLL LOOP

0001D4 30490D        29.1  01E4     851 CHKXON1     JNB     SNDXON1,CHKXOFF1    JMP IF SEND XON FLAG IS OFF

                                    853 *    SEND AN XON TO THE 8530

0001D7 C249          29.1           855             CLR     SNDXON1             CLEAR SEND XON FLAG
0001D9 854930          30    49     856             MOV     LODMA,XONRCV1       MOVE XON CHAR TO LODMA BUFFER
0001DC 2014FD        22.4  01DC     857 WAITLP5     JB      STINPROG,WAITLP5    LOOP UNTIL STAT PASS IS CLEAR
0001DF 753A22          3A    22     858             MOV     STAT0,#XON1CMD     MOV XON CMD TO STAT0
0001E2 800E          01F2           859             SJMP    PASSANY1            JMP TO PASS STATUS

0001E4 30481C        29.0  0203     861 CHKXOFF1    JNB     SNDXOFF1,CHKTXTC1   JMP IF SEND XOFF FLAG IS OFF

                                    863 *    SEND AN XOFF TO THE 8530

0001E7 C248          29.0           865             CLR     SNDXOFF1            CLEAR SEND XOFF FLAG
0001E9 2014FD        22.4  01E9     866 WAITLP6     JB      STINPROG,WAITLP6    LOOP UNTIL STAT PASS IS CLEAR
0001EC 753A23          3A    23     867             MOV     STAT0,#XOFF1CMD     MOVE XOFF CMD TO STAT0
0001EF 854830          30    48     868             MOV     LODMA,XOFFRCV1      MOVE XOFF CHAR TO LODMA BUFFER
0001F2 753B00          3B    00     869 PASSANY1    MOV     STAT1,#0            NO BITS ON IN STAT 1
0001F5 753002          3C    02     870             MOV     STATCNT,#TWOBYTE    LOAD STATUS CNT FOR 2 BYTES
0001F8 D206          20.5           871             SETBIT  CMDCMPFL            SET CMD COMPLETE FLAG IN MSB
0001FA 1206A6          06A6         872             LCALL   INTRSYS             CALL INTERRUPT SERV RTN
0001FD 758398          83    98     873             MOV     DPH,#H8530A         SET UP 8530 MOVX ADDRESS
000200 020235          0235         874             LJMP    SEND1               JMP TO SEND BYTE TO 8530

000203 30551D        2A.5  0223     876 CHKTXTC1    JNB     XMITATC,NOTXTC1     JMP IF TC FLAG IS OFF
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                    878 *
                                    879 *    ALL DATA HAS BEEN GIVEN TO THE 8530, LOOK FOR 'ALL SENT'
                                    880 *                INDICATED BY THE 8530
                                    881 *

000206 7401                   01    883           MOV     A,#R1A8530          SET UP 8530 REGISTER
000208 F0                           884           MOVX    @DPTR,A             WRITE OUT REGISTER POINTER
000209 00                           885           NOP                         WAIT FOR 8530
00020A E0                           886           MOVX    A,@DPTR             READ IN R1A DATA
00020B 20E003         E0.0  0211    887           JB      ACC.0,ALLSNTON1     JUMP IF ALL SENT INDICATED
00020E 02025E         025E          888           LJMP    ENDXMIT1            JMP TILL ALL SENT COMES ON

                                    890 *
                                    891 *   'ALL SENT' IS INDICATED... TRANSMIT IS COMPLETE, PASS STATUS
                                    892 *

000211 C247           28.7          894 ALLSNTON1 CLR     P1ENXMIT            CLR POLL ENABLE FLAG
000213 2014FD         22.4  0213    895 XDONE1    JB      STINPROG,XDONE1     JMP IF STAT PASS NOT IN PROG
000216 C255           2A.5          896           CLR     XMITATC             CLEAR DMA TC FLAG FOR CHAN B
000218 D202           20.2          897           SETBIT  XMITCOMP            SET XMIT COMP FLG IN MSB
00021A D207           20.7          898           SETBIT  ASCFLAG             SET ASC FLG IN MSB
00021C 753C00           3C    00    899           MOV     STATCNT,#ZEROBYTE   LOAD STATUS CNT FOR MSB ONLY
00021F 1206A6         06A6          900           LCALL   INTRSYS             CALL INTERRUPT SERV RTN
000222 22                           901           RET                         RETURN TO POLL LOOP
```

```
 LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                   903 ************************************************************************
                                   904 **                                                                    **
                                   905 **          DMA FROM THE SYSTEM TO THE ADAPTER                        **
                                   906 **                                                                    **
                                   907 ************************************************************************

                                   909 *    THIS IS NOT THE END OF THE TRANSMIT, FETCH TWO MORE BYTES

000223 E52E                  2E    911 NOTXTC1    MOV     A,XMITACMD          MOV CMD/DMA CHAN TO ACC

000225 120678          0678        913            LCALL   DMATOADP           CALL ROUTINE TO DMA TO ADPT.

000228 758398            83    98  915            MOV     DPH,#H8530A         SET UP MOVX ADDR=8530

                                   917 *    THE DMA RET CODE IS IN THE ACC

00022B 7014            0241        919            JNZ     TCISON1             JUMP IF TC RET CODE FOUND

                                   921 *    TC DID NOT OCCUR ON THE TRANSFER SO BOTH BYTES ARE GOOD

00022D 853132            32    31  923 BOTHOK1    MOV     HIXBYTEA,HIDMA      MOVE BYTE INTO SAVE BUFFER
000230 D257            2A.7        924            SETBIT  HIVALIDA            SET HI BYTE VALID FLAG
000232 207504          2E.5  0239  925            JB      TRASHFA,FIRSTBAD1   JUMP IF TRASH 1ST BYTE FLG ON
000235 E530                  30    926 SEND1      MOV     A,LODMA             MOV LO DMA DATA BYTE TO ACC
000237 8013            024C        927            SJMP    SENDBYT1            JMP TO XMIT BYTE OF DATA

000239 C275            2E.5        929 FIRSTBAD1  CLR     TRASHFA             CLEAR TRASH BYTE FLAG
00023B C257            2A.7        930            CLR     HIVALIDA            CLEAR VALID DATA FLAG
00023D E532                  32    931            MOV     A,HIXBYTEA          MOV HI DMA DATA BYTE TO XMIT BUF
00023F 800B            0240        932            SJMP    SENDBYT1            JMP TO XMIT BYTE OF DATA

                                   934 *    TC DID OCCUR ON THE TRANSFER SO CHECK IF LAST BYTE IS GARBAGE

000241 D255            2A.5        936 TCISON1    SETBIT  XMITATC             TURN ON XMIT B TC FLAG
000243 3074E7          2E.4  022D  937            JNB     TRASHLA,BOTHOK1     JUMP IF LAST BYTE IS NOT GARBAGE
000246 C274            2E.4        938            CLR     TRASHLA             CLEAR TRASH BYTE FLAG

                                   940 *    THE LAST BYTE IS NOT VALID SO TURN OFF THE VALID BYTE FLAG

000248 C257            2A.7        942            CLR     HIVALIDA            CLR HI BYTE VALID FLAG
00024A E530                  30    943            MOV     A,LODMA             MOVE LO DMA DATA BYTE
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86

                                    945 ************************************************************************
                                    946 **                                                                    **
                                    947 **         WRITE DATA BYTE TO 8530                                    **
                                    948 **                                                                    **
                                    949 ************************************************************************

                                    951 *
                                    952 *    ZERO OUT ALL NON-SIGNIFICANT DATA BYTE BITS.
                                    953 *      NOTE ALSO THAT THE FOLLOWING INSTRUCTION HAS THE
                                    954 *      EFFECT OF GENERATING SPACE PARITY IF THAT IS TO BE
                                    955 *      THE CASE.  THE 8530 WILL OVERRIDE THIS IF IT IS TO
                                    956 *      GENERATE PARITY.  THE ONLY REMAINING CASE IS MARK
                                    957 *      PARITY GENERATION.
                                    958 *
00024C 5536                   36    959 SENDBYT1   ANL     A,RSTPMSK1          CLEARS UNUSED HIGH ORDER BITS
                                    960 *
                                    961 *    CODE TO GENERATE MARK PARITY
                                    962 *
00024E 302202          24.2  0253   963            JNB     MARKPAR1,MS_DONE1   JUMP IF NOT MARK PARITY MODE
000251 4534                   34    964            ORL     A,XMTMSK1           OR ON MARK PARITY BIT
                                    965 *
                                    966 *    END OF MARK PARITY GENERATION CODE
                                    967 *
000253 758203            82   03    968 MS_DONE1   MOV     DPL,#L8530AD        SET LO 8530 DATA ADDRESS
000256 F0                          969            MOVX    @DPTR,A             MOVE DATA BYTE TO 8530
000257 303104          26.1  025E   970            JNB     XSPECFL1,ENDXMIT1   JMP IF XMIT SPEC FLAG IS OFF
00025A C231            26.1        971            CLR     XSPECFL1            CLEAR XSPECIAL FLAG
00025C C247            28.7        972            CLR     P1ENXMIT            CLEAR PORT 2 ENABLE XMIT
00025E 22                          973 ENDXMIT1   RET                         RETURN TO CALLING ROUTINE
```



```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86

                                    975 ************************************************************************
                                    976 **                                                                    **
                                    977 **         START ASYNC TRANSMIT ON ADAPTER PORT 1                     **
                                    978 **                                                                    **
                                    979 ************************************************************************

00025F 758398            83   98    981 STXMITP1   MOV     DPH,#H8530A         SET UP 8530 ADDRESS
000262 758201            82   01    982            MOV     DPL,#L8530A         SET UP 8530 ADDRESS
000265 7405                   05    983            MOV     A,#R5A8530          SET UP PTR VALUE
000267 F0                          984            MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
000268 E551                   51    985            MOV     A,R5A8530S          SET UP PTR VALUE
00026A 4408                   08    986            ORL     A,#EN8530TX         TURN ON THE TX ENABLE BIT
00026C F0                          987            MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
00026D D247            28.7        988            SETBIT  P1ENXMIT            TURN ON POLL ENABLE BIT
00026F C231            26.1        989            CLR     XSPECFL1            CLEAR DISABLE XMIT FLAG
000271 C255            2A.5        990            CLR     XMITATC             CLEAR XMIT TC FLAG
000273 C257            2A.7        991            CLR     HIVALIDA            CLEAR HI BYTE VALID FLAG
000275 22                          992            RET                         RETURN TO CALLING RTN
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86
                                    994 ************************************************************************
                                    995 **                                                                    **
                                    996 **   CHANNEL B ASYNC RECV SERVICE                                     **
                                    997 **                                                                    **
                                    998 ************************************************************************

                                   1000 *    CHECK FOR ANY RECEIVE ERRORS

000276 758202          82    02    1002 RECVB      MOV     DPL,#L8530BD        SET LO 8530 DATA ADDRESS
                                   1003 * 8530 READ REG 1 IS CURRENTLY IN THE ACC, CHECK FOR ERROR BITS ON
000279 5470                  70    1004            ANL     A,#X'70'            ZERO NON-ASC ERROR BITS
00027B 6003          0280          1005            JZ      CHKBRK2             JUMP IF NO ERROR BITS ARE ON
00027D 0202C1        02C1          1006            LJMP    RERROR2             JMP TO ERROR HANDLER
000280 305F03        2B.7  0286    1007 CHKBRK2    JNB     BRKDET,NOERROR2     JUMP BREAK DETECT FLAG IS NOT ON
000283 0202C1        02C1          1008            LJMP    RERROR2             JMP TO ERROR HANDLER

                                   1010 *    NO 8530 DETECTED ERRORS SO READ DATA BYTE FROM THE 8530
                                   1011 *    THE DATA POINTER VALUE IS ALREADY SET UP

000286 E0                          1013 NOERROR2   MOVX    A,@DPTR             READ THE DATA BYTE TO ACC

                                   1015 *
                                   1016 *
000287 5537                  37    1017            ANL     A,RSTPMSK2          STRIP OFF ALL NON DATA BITS
                                   1018 *
                                   1019 *
                                   1020 *    CHECK IF THE XON/XOFF HANDLING IS ENABLED

000289 302823        25.0  02AF    1022            JNB     ENXONOF2,WAITLP22   JUMP IF XON/OFF HNDL DISABLED

                                   1024 *    CHECK IF THE CHARACTER IS XOFF OR XON

00028C B54E0D          4E  029C    1026            CJNE    A,XOFFXMT2,TESTXON2 JUMP IF CHAR IS NOT XOFF

                                   1028 *    RECEIVE CHARACTER WAS AN XOFF CHAR
00028F 304302        28.3  0294    1029            JNB     P2ENXMIT,WAITLP02   JUMP IF TRANSMITTER NOT ENABLED
000292 D23B          27.3          1030            SETBIT  STOPXMT2            SET FLAG TO STOP TRANSMITTING
000294 2014FD        22.4  0294    1031 WAITLP02   JB      STINPROG,WAITLP02   LOOP UNTIL STAT PASS IS CLEAR
000297 753B10          3B    10    1032            MOV     STAT1,#XOFFSTAT     SET XOFF RECV'D FLAG IN STAT1
00029A 800C          02A8          1033            SJMP    PASSX2              JMP TO PASS STATUS

00029C 302910        25.1  02AF    1035 TESTXON2   JNB     XONEN2,WAITLP22     JUMP IF XON CHECKING NOT ENABLED
00029F B54F0D          4F  02AF    1036            CJNE    A,XONXMT2,WAITLP22  JUMP IF CHAR IS NOT XON

                                   1038 *    RECEIVE CHARACTER WAS AN XON CHAR

0002A2 2014FD        22.4  02A2    1040 WAITLPX2   JB      STINPROG,WAITLPX2   LOOP UNTIL STAT PASS IS CLEAR
0002A5 753B20          3B    20    1041            MOV     STAT1,#XONSTAT      SET XON RECV'D FLAG IN STAT1
0002A8 D205          20.5          1042 PASSX2     SETBIT  ADDSTAT             SET MSB ADDITIONAL STAT FLAG
0002AA 753C02          3C    02    1043            MOV     STATCNT,#TWOBYTE    LOAD STATUS CNT FOR TWO BYTES
0002AD 80D6          02B5          1044            SJMP    PASSRCV2            JMP TO COMPLETE STAT PASS

                                   1046 ************************************************************************
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86

                                   1047 **                                                                    **
                                   1048 **   RETURN DATA BYTE TO SYSTEM                                       **
                                   1049 **                                                                    **
                                   1050 ********************************************************************************

                                   1052 *    CHARACTER WAS NOT XOFF OR XON SO JUST PASS IT TO THE SYSTEM

0002AF 2014FD          22.4  02AF  1054 WAITLP22   JB      STINPROG,WAITLP22   LOOP UNTIL STAT PASS IS CLEAR
0002B2 753C01            3C    01  1055           MOV     STATCNT,#ONEBYTE    LOAD STATUS CNT FOR ONE BYTE
0002B5 D200            20.0        1056 PASSRCV2   SETBIT  RCVCOMP             SET RECV COMP FLG IN MSB
0002B7 D207            20.7        1057           SETBIT  ASCFLAG             SET MSB ASC FLAG
0002B9 D2B4            B0.4        1058           SETBIT  P1P2INTR            INDICATE A P2 INTERRUPT
0002BB F53A              3A        1059           MOV     STAT0,A             MOVE DATA CHAR TO STAT0 BYTE
                                   1060 ********************************************************************************
                                   1061 **                                                                    **
                                   1062 **         WRITE THE MSB INTO THE 8255 AND CAUSE A SYSTEM INTERRUPT   **
                                   1063 **                                                                    **
                                   1064 ********************************************************************************

0002BD 1206A6          06A6        1066           LCALL INTRSYS               GENERATE CHAR. RX INTERRUPT
0002C0 22                          1067 ENDRECV2   RET                         RETURN TO CALLING ROUTINE
```



```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86

                                   1069 ********************************************************************************
                                   1070 **                                                                    **
                                   1071 **   A RECEIVE ERROR WAS DETECTED BY THE 8530                         **
                                   1072 **                                                                    **
                                   1073 ********************************************************************************

0002C1 E0                          1075 RERROR2    MOVX    A,@DPTR             READ THE DATA BYTE TO ACC
0002C2 5537              37        1076           ANL     A,RSTPMSK2          STRIP OFF ALL NON DATA BITS
0002C4 2014FD          22.4  02C4  1077 WAITLP32   JB      STINPROG,WAITLP32   LOOP TILL STAT PASS IS CLEAR
0002C7 306505          2C.5  02CF  1078           JNB     ROVRUN,CHEKBRK2     JUMP IF NOT AN OVERRUN ERROR
0002CA 753B01            3B    01  1079           MOV     STAT1,#OVRSTAT      RET OVERRUN ERROR STATUS
0002CD 801C            02EB        1080           SJMP    PASSERR2            JMP TO PASS STATUS
0002CF 305F0E          2B.7  02E0  1081 CHEKBRK2   JNB     BRKDET,CHKPAR2      JUMP IF NOT A BREAK RECEIVED
0002D2 306D02          2D.5  02D7  1082           JNB     BRKFLG2,RPTBRK2     JMP IF BREAK HAS NOT BEEN RPTD
0002D5 80E9            02C0        1083           SJMP    ENDRECV2            BRK PREVIOUSLY RPTD, BAILOUT
0002D7 D26D            2D.5        1084 RPTBRK2    SETBIT  BRKFLG2             SET BREAK DETECTED FLAG
0002D9 7400              00        1085           MOV     A,#BRKDATA          FORCE DATA BYTE TO '00'H
0002DB 753B08            3B    08  1086           MOV     STAT1,#XBRKSTAT     RET BREAK DETECTED STATUS
0002DE 800B            02EB        1087           SJMP    PASSERR2            JMP TO PASS STATUS
0002E0 306405          2C.4  02E8  1088 CHKPAR2    JNB     RPARERR,FRMERR2     JUMP IF NOT A PARITY ERROR
0002E3 753B02            3B    02  1089           MOV     STAT1,#PARESTAT     RET PARITY ERROR STATUS
0002E6 8003            02EB        1090           SJMP    PASSERR2            JMP TO PASS STATUS
0002E8 753B04            3B    04  1091 FRMERR2    MOV     STAT1,#FRMESTAT     RET FRAMING ERROR STATUS

                                   1093 *    ANY RECEIVE ERROR SHOULD JMP TO HERE

0002EB C0E0              E0        1095 PASSERR2   PUSH    ACC                 SAVE ACC

0002ED 758200            82    00  1097           MOV     DPL,#L8530B         SET LO 8530 DATA ADDRESS

                                   1099 *    SEND RESET COMMAND TO 8530

0002F0 7430              30        1101           MOV     A,#X'30'            MOVE ERROR RESET CMD TO ACC
0002F2 F0                          1102           MOVX    @DPTR,A             WRITE ERROR RESET TO 8530
0002F3 D0E0              E0        1103           POP     ACC                 RESTORE ACC
0002F5 D201            20.1        1104           SETBIT  RECERRFL            SET MSB RECEIVE ERROR FLAG
0002F7 0202A8          02A8        1105           LJMP    PASSX2              JMP TO PASS STATUS
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                   1108 ************************************************************************
                                   1109 **                                                                    **
                                   1110 **    CHANNEL B ASYNC XMIT SERVICE                                    **
                                   1111 **                                                                    **
                                   1112 ************************************************************************

                                   1114 * IF HIVALID IS ON, THIS IS NOT THE FIRST TRANSFER

0002FA 758398          83    98    1116 XMITB       MOV     DPH,#H8530B          SET UP DATA POINTER
0002FD 758200          82    00    1117             MOV     DPL,#L8530B          SET UP DATA POINTER
000300 301F09        23.7  030C    1118             JNB     HIVALIDB,INVALID2    JMP IF HI DMA BYTE IS NOT VALID

                                   1120 *    THE HI DMA DATA BYTE IS VALID SO PASS IT TO THE 8530             *

000303 C21F          23.7          1122             CLR     HIVALIDB             CLEAR VALID DATA FLAG
000305 C27D          2F.5          1123             CLR     TRASHFB              CLEAR TRASH FIRST BYTE FLAG
000307 E533                  33    1124             MOV     A,HIXBYTEB           MOV HI DMA DATA BYTE TO XMIT BUF
000309 020390          0390        1125             LJMP    SENDBYT2             JMP TO XMIT BYTE OF DATA
                                   1126 *    THE HI DMA DATA BYTE IS NOT VALID SO CHECK FOR SPECIAL SITUATIONS
                                   1127 *    THERE IS NO DATA FOR THE 8530 ON THE CARD AT THIS TIME

00030C 303B05        27.3  0314    1129 INVALID2    JNB     STOPXMT2,CHKXON2     JMP IF STOP XMIT FLAG IS OFF
00030F C23B          27.3          1130             CLR     STOPXMT2             CLEAR STOP XMIT FLAG
000311 C243          28.3          1131             CLR     P2ENXMIT             CLEAR P2 POLL ENABLE FLAG
000313 22                          1132             RET                          RETURN TO POLL LOOP

000314 30390D        27.1  0324    1134 CHKXON2     JNB     SNDXON2,CHKXOFF2     JMP IF SEND XON FLAG IS OFF

                                   1136 *    SEND AN XON TO THE 8530

000317 C239          27.1          1138             CLR     SNDXON2              CLEAR SEND XON FLAG
000319 854D30          30    4D    1139             MOV     LODMA,XONRCV2        MOVE XON CHAR TO LODMA BUFFER
00031C 2014FD        22.4  031C    1140 WAITLP52    JB      STINPROG,WAITLP52    LOOP UNTIL STAT PASS IS CLEAR
00031F 753A22          3A    22    1141             MOV     STAT0,#XON1CMD      MOV XON CMD TO STAT0
000322 800E          0332        1142             SJMP    PASSANY2             JMP TO PASS STATUS

000324 30381E        27.0  0345    1144 CHKXOFF2    JNB     SNDXOFF2,CHKTXTC2    JMP IF SEND XOFF FLAG IS OFF

                                   1146 *    SEND AN XOFF TO THE 8530

000327 C238          27.0          1148             CLR     SNDXOFF2             CLEAR SEND XOFF FLAG
000329 2014FD        22.4  0329    1149 WAITLP62    JB      STINPROG,WAITLP62    LOOP UNTIL STAT PASS IS CLEAR
00032C 753A23          3A    23    1150             MOV     STAT0,#XOFF1CMD      MOVE XOFF CMD TO STAT0
00032F 854C30          30    4C    1151             MOV     LODMA,XOFFRCV2       MOVE XOFF CHAR TO LODMA BUFFER
000332 753B00          3B    00    1152 PASSANY2    MOV     STAT1,#0             NO BITS ON IN STAT 1
000335 753C02          3C    02    1153             MOV     STATCNT,#TWOBYTE     LOAD STATUS CNT FOR 2 BYTES
000338 D205          20.5          1154             SETBIT  CMDCMPFL             SET CMD COMPLETE FLAG IN MSB
00033A D2B4          B0.4          1155             SETBIT  P1P2INTR             INDICATE PORT 2 INTERRUPT
00033C 1206A6          06A6        1156             LCALL   INTRSYS              CALL INTERRUPT SERV RTN
00033F 758398          83    98    1157             MOV     DPH,#H8530B          SET UP 8530 MOVX ADDRESS
000342 020379          0379        1158             LJMP    SEND2                JMP TO SEND BYTE TO 8530

000345 301D1F        23.5  0367    1160 CHKTXTC2    JNB     XMITBTC,NOTXTC2      JMP IF TC FLAG IS OFF
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    ASM51 V1.9 07.09 05/09/86

                                   1162 *
                                   1163 *    ALL DATA HAS BEEN GIVEN TO THE 8530, LOOK FOR 'ALL SENT'
                                   1164 *                  INDICATED BY THE 8530
                                   1165 *

000348 7401                  01    1167            MOV     A,#R1B8530          SET UP 8530 REGISTER
00034A F0                          1168            MOVX    @DPTR,A             WRITE OUT REGISTER POINTER
00034B 00                          1169            NOP                         WAIT FOR 8530
00034C E0                          1170            MOVX    A,@DPTR             READ IN R1A DATA
00034D 20E0?3          E0.0  0353  1171            JB      ACC.0,ALLSNTON2     JUMP IF ALL SENT INDICATED
000350 0203A2          03A2        1172            LJMP    ENDXMIT2            JMP TILL ALL SENT COMES ON

                                   1174 *
                                   1175 *   'ALL SENT' IS INDICATED... TRANSMIT IS COMPLETE, PASS STATUS
                                   1176 *

000353 C243            28.3        1178 ALLSNTON2  CLR     P2ENXMIT            CLR POLL ENABLE FLAG
000355 2014FD          22.4  0355  1179 XDONE2     JB      STINPROG,XDONE2     JMP IF STAT PASS NOT IN PROG
000358 C21D            23.5        1180            CLR     XMITBTC             CLEAR DMA TC FLAG FOR CHAN B
00035A D202            20.2        1181            SETBIT  XMITCOMP            SET XMIT COMP FLG IN MSB
00035C D207            20.7        1182            SETBIT  ASCFLAG             SET ASC FLG IN MSB
00035E D2B4            B0.4        1183            SETBIT  P1P2INTR            INDICATE PORT 2 INTERRUPT
000360 753C00            3C    00  1184            MOV     STATCNT,#ZEROBYTE   LOAD STATUS CNT FOR MSB ONLY
000363 1206A6          06A6        1185            LCALL   INTRSYS             CALL INTERRUPT SERV RTN
000366 22                          1186            RET                         RETURN TO POLL LOOP
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                   1188 ************************************************************************
                                   1189 **                                                                    **
                                   1190 **          DMA FROM THE SYSTEM TO THE ADAPTER                        **
                                   1191 **                                                                    **
                                   1192 ************************************************************************

                                   1194 *    THIS IS NOT THE END OF THE TRANSMIT, FETCH TWO MORE BYTES

000367 E52F                  2F    1196 NOTXTC2     MOV      A,XMITBCMD          MOV CMD/DMA CHAN TO ACC

000369 120678          0678        1198             LCALL    DMATOADP            CALL ROUTINE TO DMA TO ADPT.

00036C 758398            83    98  1200             MOV      DPH,#H8530B         SET UP MOVX ADDR=8530

                                   1202 *    THE DMA RET CODE IS IN THE ACC

00036F 7014            0385        1204             JNZ      TCISON2             JUMP IF TC RET CODE FOUND

                                   1206 *    TC DID NOT OCCUR ON THE TRANSFER SO BOTH BYTES ARE GOOD

000371 853133            33    31  1208 BOTHOK2     MOV      HIXBYTEB,HIDMA      MOVE BYTE INTO SAVE BUFFER
000374 D21F            23.7        1209             SETBIT   HIVALIDB            SET HI BYTE VALID FLAG
000376 207D04          2F.5  037D  1210             JB       TRASHFB,FIRSTBAD2   JUMP IF TRASH 1ST BYTE FLG ON
000379 E530              30        1211 SEND2       MOV      A,LODMA             MOV LO DMA DATA BYTE TO ACC
00037B 8013            0390        1212             SJMP     SENDBYT2            JMP TO XMIT BYTE OF DATA

00037D C27D            2F.5        1214 FIRSTBAD2   CLR      TRASHFB             CLEAR TRASH BYTE FLAG
00037F C21F            23.7        1215             CLR      HIVALIDB            CLEAR VALID DATA FLAG
000381 E533                  33    1216             MOV      A,HIXBYTEB          MOV HI DMA DATA BYTE TO XMIT BUF
000383 800B            0390        1217             SJMP     SENDBYT2            JMP TO XMIT BYTE OF DATA

                                   1219 *    TC DID OCCUR ON THE TRANSFER SO CHECK IF LAST BYTE IS GARBAGE

000385 D21D            23.5        1221 TCISON2     SETBIT   XMITBTC             TURN ON XMIT B TC FLAG
000387 307CE7          2F.4  0371  1222             JNB      TRASHLB,BOTHOK2     JUMP IF LAST BYTE IS NOT GARBAGE
00038A C27C            2F.4        1223             CLR      TRASHLB             CLEAR TRASH BYTE FLAG

                                   1225 *    THE LAST BYTE IS NOT VALID SO TURN OFF THE VALID BYTE FLAG

00038C C21F            23.7        1227             CLR      HIVALIDB            CLR HI BYTE VALID FLAG
00038E E530                  30    1228             MOV      A,LODMA             MOVE LO DMA DATA BYTE
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86

                                   1230 ************************************************************************
                                   1231 **                                                                    **
                                   1232 **         WRITE DATA BYTE TO 8530                                    **
                                   1233 **                                                                    **
                                   1234 ************************************************************************

                                   1236 *
                                   1237 *    ZERO OUT ALL NON-SIGNIFICANT DATA BYTE BITS.
                                   1238 *      NOTE ALSO THAT THE FOLLOWING INSTRUCTION HAS THE
                                   1239 *      EFFECT OF GENERATING SPACE PARITY IF THAT IS TO BE
                                   1240 *      THE CASE.  THE 8530 WILL OVERRIDE THIS IF IT IS TO
                                   1241 *      GENERATE PARITY.  THE ONLY REMAINING CASE IS MARK
                                   1242 *      PARITY GENERATION.
                                   1243 *
000390 5537                  37    1244 SENDBYT2   ANL     A,RSTPMSK2          CLEARS UNUSED HIGH ORDER BITS
                                   1245 *
                                   1246 *    CODE TO GENERATE MARK PARITY
                                   1247 *
000392 302A02          25.2  0397  1248            JNB     MARKPAR2,MS_DONE2   JUMP IF NOT MARK PARITY MODE
000395 4535                  35    1249            ORL     A,XMTMSK2           OR ON MARK PARITY BIT
                                   1250 *
                                   1251 *    END OF MARK PARITY GENERATION CODE
                                   1252 *
000397 758202            82  02    1253 MS_DONE2   MOV     DPL,#L8530BD        SET LO 8530 DATA ADDRESS
00039A F0                        1254            MOVX    @DPTR,A             MOVE DATA BYTE TO 8530
00039B 303004          26.0  03A2  1255            JNB     XSPECFL2,ENDXMIT2   JMP IF XMIT SPEC FLAG IS OFF
00039E C230            26.0        1256            CLR     XSPECFL2            CLEAR XSPECIAL FLAG
0003A0 C243            28.3        1257            CLR     P2ENXMIT            CLEAR PORT 2 ENABLE XMIT
0003A2 22                          1258 ENDXMIT2   RET                         RETURN TO CALLING ROUTINE
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86

                                   1260 ************************************************************************
                                   1261 **                                                                    **
                                   1262 **          START ASYNC TRANSMIT ON ADAPTER PORT 2                    **
                                   1263 **                                                                    **
                                   1264 ************************************************************************

0003A3 758398           83    98   1266 STXMITP2   MOV     DPH,#H8530B         SET UP 8530 ADDRESS
0003A6 758200           82    00   1267             MOV     DPL,#L8530B         SET UP 8530 ADDRESS
0003A9 7405                 05   1268             MOV     A,#R5B8530          SET UP PTR VALUE
0003AB F0                        1269             MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
0003AC E554                 54   1270             MOV     A,R5B8530S          SET UP PTR VALUE
0003AE 4408                 08   1271             ORL     A,#EN8530TX         TURN ON THE TX ENABLE BIT
0003B0 F0                        1272             MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
0003B1 D243           28.3       1273             SETBIT  P2ENXMIT            TURN ON POLL ENABLE BIT
0003B3 C230           26.0       1274             CLR     X5PECFL2            CLEAR DISABLE XMIT FLAG
0003B5 C21D           23.5       1275             CLR     XMITBTC             CLEAR XMIT TC FLAG
0003B7 C21F           23.7       1276             CLR     HIVALIDB            CLEAR HI BYTE VALID FLAG
0003B9 22                        1277             RET                         RETURN TO CALLING RTN
```

```
LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    ASM51 V1.9 07.09 05/09/86

                                 1279 ********************************************************************************
                                 1280 **                                                                            **
                                 1281 **          OPERATING MODE COMMAND DECODE                                     **
                                 1282 **                                                                            **
                                 1283 ********************************************************************************
                                 1284 **
                                 1285 **  Sample Async Microcode Command Set Definition
                                 1286 **
                                 1287 **       Command Code         Function
                                 1288 **       ============         ========
                                 1289 **
                                 1290 **          '22'H             Send XON on Adapter P1
                                 1291 **          '23'H             Send XOFF on Adapter P1
                                 1292 **          '2A'H             Send XON on Adapter P2
                                 1293 **          '2B'H             Send XOFF on Adapter P2
                                 1294 **
                                 1295 **          '30'H             Disable Transmit for P1
                                 1296 **          '31'H             Enable Transmit for P1
                                 1297 **          '32'H             Disable Recv for P1
                                 1298 **          '33'H             Enable Recv for P1
                                 1299 **          '34'H             Disable Modem Interrupts for P1
                                 1300 **          '35'H             Enable Modem Interrupts for P1
                                 1301 **          '38'H             Disable Transmit for P2
                                 1302 **          '39'H             Enable Transmit for P2
                                 1303 **          '3A'H             Disable Recv for P2
                                 1304 **          '3B'H             Enable Recv for P2
                                 1305 **          '3C'H             Disable Modem Interrupts for P2
                                 1306 **          '3D'H             Enable Modem Interrupts for P2
                                 1307 **
                                 1308 **          '5X'H             DMA Multi-Byte Cmd to Adapter
                                 1309 **            |               ---------------
                                 1310 **             ------------->| 3 | 2 | 1 | 0 | low order bits
                                 1311 **                           ---------------
                                 1312 **                             |   |   |   |
                                 1313 **                             |   |    -------  Adapter DMA Ch.
                                 1314 **                             |    -----------  undefined
                                 1315 **                              ---------------  '1' = P2 cmd
                                 1316 **
                                 1317 **                           Transmit Data command
                                 1318 **           ---------------------------------
                                 1319 **          | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                 1320 **           ---------------------------------
                                 1321 **             |   |   |   |   |   |   |   |
                                 1322 **             |   |   |   |   |   |    -------  Adapter DMA Ch.
                                 1323 **             |   |   |   |   |    -----------  undefined
                                 1324 **             |   |   |   |    ---------------  '1' = P2 cmd
                                 1325 **             |   |   |    -------------------  Discard Last byte DMA'd
                                 1326 **             |   |    -----------------------  Discard First byte
                                 1327 **             |    ---------------------------  undefined
                                 1328 **              -------------------------------  '1' = Transmit Cmd
                                 1329 **
                                 1330 **                                                                            **
                                 1331 ********************************************************************************
```

LOC OBJECT CODE ADDR1 ADDR2 STMT SOURCE STATEMENT ASM51 V1.9 07.09 05/09/86

```
0003BA E6                          1333 OPCMDDCD  MOV     A,@R0              MOVE THE NEXT CMD TO ACC

0003BB 30E302        E0.3  03C0    1335           JNB     ACC.3,P1CMD        JUMP IF THIS IS A P1 CMD
0003BE D211          22.1          1336           SETBIT  D2CMD              SET PORT 2 CMD FLAG
0003C0 54F0                  F0    1337 P1CMD     ANL     A,#X'F0'           ZERO LO NIBBLE OF CMD CODE
0003C2 30E712        E0.7  03D7    1338           JNB     ACC.7,DJMP2        JUMP IF NOT START XMIT CMD
0003C5 30110d        22.1  03D0    1339           JNB     P2CMD,P1SXMT       JUMP IF NOT PORT 2 COMMAND
0003C8 862F            2F          1340           MOV     XMITBCMD,@R0       MOVE CMD CODE TO XMIT CMD BUFFER
0003CA 1203A3        03A3          1341           LCALL   STXMITP2           CALL START XMIT P2 RTN
0003CD 020401        0401          1342           LJMP    UPSTACK            JUMP TO CMD COMPLETE HANDLER
0003D0 862E            2E          1343 P1SXMT    MOV     XMITACMD,@R0       MOVE CMD CODE TO XMIT CMD BUFFER
0003D2 12025F        025F          1344           LCALL   STXMITP1           CALL START XMIT P1 RTN
0003D5 802A          0401          1345           SJMP    UPSTACK            JUMP TO CMD COMPLETE HANDLER
0003D7 B42005          20  03DF    1346 DJMP2     CJNE    A,#XSPCMD,DJMP3    JUMP IF NOT XMIT SPEC CMD
0003DA 120405        0405          1347           LCALL   XMITSPEC           CALL XMIT SPECIAL CHAR RTN
0003DD 8025          0404          1348           SJMP    CMDCOMP            JUMP TO CMD COMPLETE HANDLER
0003DF B43005          30  03E7    1349 DJMP3     CJNE    A,#RMCCMD,DJMP7    JUMP IF NOT MODE CNTL CMD
0003E2 120435        0435          1350           LCALL   SETMODE            CALL RECEIVE MODE CTL RTN
0003E5 8008          03EF          1351           SJMP    WAIT_LP1           JUMP TO COMPLETE STATUS PASS
0003E7 B45005          50  03EF    1352 DJMP7     CJNE    A,#SDMACMD,WAIT_LP1 JUMP IF NOT START DMA CMD
0003EA 1204E0        04E0          1353           LCALL   MBYTCMDS           CALL START DMA RTN
0003ED 8015          0404          1354           SJMP    CMDCOMP            JUMP TO CMD COMPLETE HANDLER
0003EF 2014FD        22.4  03EF    1355 WAIT_LP1  JB      STINPROG,WAIT_LP1  WAIT TILL STATUS PASS IS CLEAR
0003F2 863A            3A          1356           MOV     STAT0,@R0          MOVE CMD CODE INTO STAT0
0003F4 753C02          3C    02    1357           MOV     STATCNT,#TWOBYTE   SET UP STAT BYTE PASS CNT
0003F7 D205          20.5          1358           SETBIT  CMDCMPFL           SET CMD COMPLETE FLAG IN MSB
0003F9 301102        22.1  03FE    1359           JNB     P2CMD,CALLSYS      JUMP IF CMD WAS FOR PORT 1
0003FC D2B4          B0.4          1360           SETBIT  P1P2INTR           SET INTR SRCE TO PORT 2
0003FE 1206A6        06A6          1361 CALLSYS   LCALL   INTRSYS           CALL SYSTEM INTR SERVICE
000401 120698        0698          1362 UPSTACK   LCALL   CMDSTUPD          CALL SYSTEM INTR SERVICE
000404 22                          1363 CMDCOMP   RET                        RETURN TO MAIN POLL LOOP
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                   1365 ************************************************************************
                                   1366 **                                                                    **
                                   1367 **          TRANSMIT SPECIAL CHARACTER (i.e. XON or XOFF)             **
                                   1368 **                                                                    **
                                   1369 ************************************************************************

000405 E6                          1371 XMITSPEC    MOV     A,@R0                 MOVE CMD CODE TO ACC
000406 201117          22.1  0420  1372             JB      P2CMD,P2XSPEC         JUMP IF PORT 2 CMD

                                   1374 * PORT 1 COMMANDS

000409 B42204            22  0410  1376             CJNE    A,#XON1CMD,NOTXON1    JUMP IF NOT XON FOR PORT 1
00040C D249            29.1        1377             SETBIT  SNDXON1               SET SEND XON FLAG FOR PORT 1
00040E 8005            0415        1378             SJMP    CMDDONE0              JUMP TO DO RETURN
000410 B42309            23  041C  1379 NOTXON1     CJNE    A,#XOFF1CMD,OK1       JUMP IF NOT XOFF FOR PORT 1
000413 D248            29.0        1380             SETBIT  SNDXOFF1              SET SEND XOFF FLAG FOR PORT 1
000415 204704          28.7  041C  1381 CMDDONE0     JB      P1ENXMIT,OK1          JMP IF XMIT IS ENABLED
000418 D247            28.7        1382             SETBIT  P1ENXMIT              ENABLE TRANSMITTER
00041A D231            26.1        1383             SETBIT  XSPECFL1              SET XMIT SPECIAL FLAG
00041C 120698          0698        1384 OK1         LCALL   CMDSTUPD              CALL CMD STACK UPDATE ROUTINE
00041F 22                          1385             RET                           RETURN TO CALLING ROUTINE


                                   1388 * PORT 2 COMMANDS

000420 B42A04            2A  0427  1391 P2XSPEC     CJNE    A,#XON2CMD,NOTXON2    JUMP IF NOT XON FOR PORT 2
000423 D239            27.1        1392             SETBIT  SNDXON2               SET SEND XON FLAG FOR PORT 2
000425 8005            042C        1393             SJMP    CMDDONE2              JUMP TO DO RETURN
000427 B42B09            2B  0433  1394 NOTXON2     CJNE    A,#XOFF2CMD,OK2       JUMP IF NOT XOFF FOR PORT 2
00042A D238            27.0        1395             SETBIT  SNDXOFF2              SET SEND XOFF FLAG FOR PORT 2
00042C 204304          28.3  0433  1396 CMDDONE2     JB      P2ENXMIT,OK2          JMP IF XMIT IS ENABLED
00042F D243            28.3        1397             SETBIT  P2ENXMIT              ENABLE TRANSMITTER
000431 D230            26.0        1398             SETBIT  XSPECFL2              SET XMIT SPECIAL FLAG
000433 80E7            041C        1399 OK2         SJMP    OK1                   JMP TO UPDATE STK/DO RETURN
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86
                                   1401 ************************************************************************
                                   1402 **                                                                    **
                                   1403 **          SET ADAPTER MODE COMMAND                                  **
                                   1404 **                                                                    **
                                   1405 ************************************************************************

000435 E6                          1407 SETMODE     MOV     A,@R0               MOVE CMD CODE TO ACC
000436 201154          22.1  048D  1408              JB      P2CMD,ADPMODE2      JUMP IF THIS IS A PORT 2 CMD

                                   1410 *           SET ADAPTER MODE COMMAND PORT 1                           *

000439 758398            83    98  1412              MOV     DPH,#H8530A         SET UP 8530 ADDRESS
00043C 758201            82    01  1413              MOV     DPL,#L8530A         SET UP 8530 ADDRESS
00043F B43008            30  044A  1414              CJNE    A,#X'30',NOT1       JUMP IF NOT DISABLE TX P1
000442 304702          28.7  0447  1415              JNB     P1ENXMIT,DONE1      JUMP IF XMIT NOT ACTIVE
000445 D24B            29.3        1416              SETBIT  STOPXMT1            SET STOP XMIT FLAG
000447 0204CF          04CF        1417 DONE1       LJMP    CMDDONE1            JUMP TO DO RETURN
00044A B43106            31  0453  1418 NOT1        CJNE    A,#X'31',NOT2       JUMP IF NOT ENABLE TX P1
00044D E0                          1419              MOVX    A,@DPTR             READ 8530 REG 0 VALUE
00044E D247            28.7        1420              SETBIT  P1ENXMIT            ENABLE PORT 1 XMIT
000450 0204CF          04CF        1421              LJMP    CMDDONE1            JUMP TO DO RETURN
000453 B4320D            32  0463  1422 NOT2        CJNE    A,#X'32',NOT3       JUMP IF NOT DISABLE RX P1
000456 7403                03      1423              MOV     A,#R3A8530          SET UP PTR VALUE
000458 F0                          1424              MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
000459 E550                  50    1425              MOV     A,R3A8530S          SET UP PTR VALUE
00045B 54FE                  FE    1426              ANL     A,#X'FE'            TURN OFF THE RX ENABLE BIT
00045D F0                          1427              MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
00045E C246            28.6        1428              CLR     P1ENRCVR            DISABLE POR1 RCVR
000460 0204CF          04CF        1429              LJMP    CMDDONE1            JUMP TO DO RETURN
000463 B43313            33  0479  1430 NOT3        CJNE    A,#X'33',NOT4       JUMP IF NOT ENABLE RX P1
000466 758203            82    03  1431              MOV     DPL,#L8530AD        SET UP 8530 ADDRESS
000469 E0                          1432              MOVX    A,@DPTR             DO DUMMY READ OF RCV FIFO
00046A 758201            82    01  1433              MOV     DPL,#L8530A         SET UP 8530 ADDRESS
00046D 7403                03      1434              MOV     A,#R3A8530          SET UP PTR VALUE
00046F F0                          1435              MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
000470 E550                  50    1436              MOV     A,R3A8530S          SET UP PTR VALUE
000472 4401                  01    1437              ORL     A,#EN8530RX         TURN ON THE RX ENABLE BIT
000474 F0                          1438              MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
000475 D246            28.6        1439              SETBIT  P1ENRCVR            ENABLE POR1 RCVR
000477 8056            04CF        1440              SJMP    CMDDONE1            JUMP TO DO RETURN
000479 B43404            34  0480  1441 NOT4        CJNE    A,#X'34',NOT5       JUMP IF NOT DISABLE P1 MODM
00047C C245            28.5        1442              CLR     P1ENMODM            DISABLE POR1 MODEM INTR
00047E 804F            04CF        1443              SJMP    CMDDONE1            JUMP TO DO RETURN
000480 B4354C            35  04CF  1444 NOT5        CJNE    A,#X'35',CMDDONE1   JUMP IF NOT ENABLE P1 MODM
000483 D245            28.5        1445              SETBIT  P1ENMODM            ENABLE POR1 MODEM INTR
000485 2014FD          22.4  0485  1446 SPIN_1      JB      STINPROG,SPIN_1     WAIT FOR OK TO PASS STS
000488 85423B            3B    42  1447              MOV     STAT1,MDMREG1C      RETN MDM STATUS AS BYTE 2
00048B 8045            04D2        1448              SJMP    STPASS2             JMP TO ROUTINE EXIT

                                   1451 *           SET ADAPTER MODE COMMAND PORT 2                           *
```

LOC OBJECT CODE ADDR1 ADDR2 STMT SOURCE STATEMENT ASM51 V1.9 07.09 05/09/86

```
00048D 758398          83    98  1454 ADPMODE2   MOV     DPH #H8530B         SET UP 8530 ADDRESS
000490 758200          82    00  1455             MOV     DPL #L8530B         SET UP 8530 ADDRESS
000493 B43807          38  049D  1456             CJNE    A,#X'38',NOT11      JUMP IF NOT DISABLE TX P2
000496 304302       28.3  049B  1457             JNB     P2ENXMIT,DONE2      JUMP IF XMIT NOT ACTIVE
000499 D23B         27.3        1458             SETBIT  STOPXMT2            SET STOP XMIT FLAG
00049B 8032            04CF     1459 DONE2      SJMP    CMDDONE1            JUMP TO DO RETURN
00049D B43905          39  04A5  1460 NOT11      CJNE    A,#X'39',NOT21      JUMP IF NOT ENABLE TX P2
0004A0 E0                       1461             MOVX    A,@DPTR             READ 8530 REG 0 VALUE
0004A1 D243         28.3        1462             SETBIT  P2ENXMIT            ENABLE POR1 XMIT
0004A3 802A            04CF     1463             SJMP    CMDDONE1            JUMP TO DO RETURN
0004A5 B43A0C          3A  04B4  1464 NOT21      CJNE    A,#X'3A',NOT31      JUMP IF NOT DISABLE RX P2
0004A8 7403                 03  1465             MOV     A,#R3B8530          SET UP PTR VALUE
0004AA F0                       1466             MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
0004AB E553                 53  1467             MOV     A,R3B8530S          SET UP PTR VALUE
0004AD 54FE                 FE  1468             ANL     A,#X'FE'            TURN OFF THE RX ENABLE BIT
0004AF F0                       1469             MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
0004B0 C242         28.2        1470             CLR     P2ENRCVR            DISABLE P2 RCVR
0004B2 801B            04CF     1471             SJMP    CMDDONE1            JUMP TO DO RETURN
0004B4 B43B13          3B  04CA  1472 NOT31      CJNE    A,#X'3B',NOT41      JUMP IF NOT ENABLE RX P2
0004B7 758202          82    02  1473             MOV     DPL,#L8530BD        SET UP 8530 ADDRESS
0004BA E0                       1474             MOVX    A,@DPTR             DO DUMMY READ OF RCV FIFO
0004BB 758200          82    00  1475             MOV     DPL,#L8530B         SET UP 8530 ADDRESS
0004BE 7403                 03  1476             MOV     A,#R3B8530          SET UP PTR VALUE
0004C0 F0                       1477             MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
0004C1 E553                 53  1478             MOV     A,R3B8530S          SET UP PTR VALUE
0004C3 4401                 01  1479             ORL     A,#EN8530RX         TURN ON THE RX ENABLE BIT
0004C5 F0                       1480             MOVX    @DPTR,A             WRITE PTR VALUE TO REG 0
0004C6 D242         28.2        1481             SETBIT  P2ENRCVR            ENABLE P2 RCVR
0004C8 8005            04CF     1482             SJMP    CMDDONE1            JUMP TO DO RETURN
0004CA B43C06          3C  04D3  1483 NOT41      CJNE    A,#X'3C',NOT51      JUMP IF NOT DISABLE P2 MODM
0004CD C241         28.1        1484             CLR     P2ENMODM            DISABLE P2 MODEM INTR

                                1486 *           COMMAND COMPLETE

0004CF 2014FD       22.4  04CF  1488 CMDDONE1    JB      STINPROG,CMDDONE1   WAIT TILL STATUS PASS IS CLEAR
0004D2 22                       1489 STPASS2     RET                         RETURN TO PASS STATUS
0004D3 B43DF9          3D  04CF  1490 NOT51      CJNE    A,#X'3D',CMDDONE1   JUMP IF NOT ENABLE P2 MODM
0004D6 D241         28.1        1491             SETBIT  P2ENMODM            ENABLE P2 MODEM INTR
0004D8 2014FD       22.4  04D8  1492 SPIN_2      JB      STINPROG,SPIN_2     WAIT FOR OK TO PASS STS
0004DB 85453B          3B    45  1493             MOV     STAT1,MDMREG2C      RETN MDM STATUS AS BYTE 2
0004DE 80F2         04D2        1494             SJMP    STPASS2             JMP TO ROUTINE EXIT
```

```
LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    ASM51 V1.9 07.09 05/09/86
                                 1497 ;*****************************************************************************
                                 1498 ;**                                                                         **
                                 1499 ;**          MULTI-BYTE COMMAND DECODE                                      **
                                 1500 ;**                                                                         **
                                 1501 ;*****************************************************************************
                                 1502 ;**
                                 1503 ;**
                                 1504 ;**  Sample Async Microcode Multi-Byte Command Set Definition
                                 1505 ;**
                                 1506 ;**       Command Code         Function
                                 1507 ;**       ============         ========
                                 1508 ;**
                                 1509 ;**           '00'H            Initialize Port 1
                                 1510 ;**           '01'H            Initialize Port 2
                                 1511 ;**
                                 1512 ;**             Initialization Data Structure
                                 1513 ;**
                                 1514 ;**            ---------------------------------
                                 1515 ;**           | MB Command Code ('00' or '01')|
                                 1516 ;**            ---------------------------------
                                 1517 ;**           | Pad byte                      |
                                 1518 ;**            ---------------------------------
                                 1519 ;**           | 8530 Register Data            |
                                 1520 ;**            ---------------------------------
                                 1521 ;**           | 8530 Register Addr (00 - 0F)  |
                                 1522 ;**            ---------------------------------
                                 1523 ;**                          .
                                 1524 ;**                          .  (repeat as rq'd)
                                 1525 ;**                          .
                                 1526 ;**            ---------------------------------
                                 1527 ;**           | Pad byte                      |
                                 1528 ;**            ---------------------------------
                                 1529 ;**           | Transition flag ('FF'H)       |
                                 1530 ;**            ---------------------------------
                                 1531 ;**           | Pad byte                      |
                                 1532 ;**            ---------------------------------
                                 1533 ;**           | Modem interrupt en. mask      |
                                 1534 ;**            ---------------------------------
                                 1535 ;**           | Async Flags 1                 |
                                 1536 ;**            ---------------------------------
                                 1537 ;**           | Async Flags 2 (byte length)   |
                                 1538 ;**            ---------------------------------
                                 1539 ;**           | XON byte to Transmit          |
                                 1540 ;**            ---------------------------------
                                 1541 ;**           | XOFF byte to Transmit         |
                                 1542 ;**            ---------------------------------
                                 1543 ;**           | XON byte to look for in Rx    |
                                 1544 ;**            ---------------------------------
                                 1545 ;**           | XOFF byte to look for in Rx   |
                                 1546 ;**            ---------------------------------
                                 1547 ;**
                                 1548 ;**                                                                         **
                                 1549 ;*****************************************************************************
```

LOC OBJECT CODE ADDR1 ADDR2 STMT SOURCE STATEMENT ASM51 V1.9 07.09 05/09/86

```
0004E0 C237           26.7          1551 MBYTCMDS   CLR     TERMCNT              CLEAR TEMP. TERMCNT FLAG
0004E2 E6                           1552            MOV     A,@R0                MOVE CMD CODE/DMA CHAN TO ACC
0004E3 120678         0678          1553            LCALL   DMATOADP             CALL DMA TO ADAPTER RTN
0004E6 E530                 30      1554            MOV     A,LODMA              MOVE LO DMA VALUE TO ACC
0004E8 F53D             3D          1555            MOV     MBYTBUF,A            SAVE THE MBYTE CMD CODE

0004EA B40005           00  04F2    1557            CJNE    A,#INL8530A,DJMP1    JUMP IF NOT INIT 8530 CH. A
0004ED 120516         0516          1558            LCALL   IN8530A              CALL 8530 INIT CHAN A RTN
0004F0 8008           04FA          1559            SJMP    STATPASS             JUMP TO SET UP STATUS PASS

0004F2 B40105           01  04FA    1561 DJMP1      CJNE    A,#INL8530B,STATPASS JUMP IF NOT INIT 8530 CH. B
0004F5 1205C7         05C7          1562            LCALL   IN8530B              CALL 8530 INIT CHAN B RTN
0004F8 8000           04FA          1563            SJMP    STATPASS             JUMP TO SET UP STATUS PASS

0004FA 2014FD         22.4  04FA    1565 STATPASS   JB      STINPROG,STATPASS    WAIT TILL STAT PASS IS CLEAR
0004FD D205           20.5          1566            SETBIT  CMDCMPFL             SET COMMAND COMPLETE FLAG
0004FF D203           20.3          1567            SETBIT  MBYTEFL              SET MULTI-BYTE FLAG IN MSB
000501 853D3A            3A    3D   1568            MOV     STAT0,MBYTBUF        MOVE MBYT CMD TO STAT0
000504 753B01            3B    01   1569            MOV     STAT1,#DMATCST       INDICATE DMA TC OCCURRED
000507 753C02            3C    02   1570            MOV     STATCNT,#TWOBYTE     SET UP STAT BYTE CNT
00050A 301102         22.1  050F    1571            JNB     P2CMD,CALLINT        JMP IF NOT A P2 CMD
00050D D2B4           20.4          1572            SETBIT  P1P2INTR             SET INTR SOURCE TO P2
00050F 1206A6         06A6          1573 CALLINT    LCALL   INTRSYS              CALL SYSTEM INTERRUPT ROUTINE
000512 120698         0698          1574            LCALL   CMDSTUPD             CALL CMD STACK UPDATE ROUTINE
000515 22                           1575            RET                          RETURN TO CALLER
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                   1577 ********************************************************************
                                   1578 **                                                                **
                                   1579 **          INITIALIZE 8530 CHANNEL A REGISTERS                   **
                                   1580 **                                                                **
                                   1581 ********************************************************************

000516 E6                          1583 IN8530A     MOV      A,@R0               MOVE CMD CODE/DMA CHAN TO ACC

                                   1585 *  FETCH ADDRESS/DATA PAIR FROM SYSTEM MEMORY

000517 120678          0678        1587             LCALL    DMATOADP            CALL DMA TO ADP RTN

                                   1589 *  THE ACC HAS THE DMA RETURN CODE

00051A 6002            051E        1591             JZ       NOTC1               JUMP IF TC IS NOT RETURNED

                                   1593 *  CHECK IF A TERM COUNT OCCURRED ON THE DMA TRANSFER

00051C D237            26.7        1595             SETBIT   TERMCNT             SET GENERAL TERM CNT FLAG

00051E E531                  31    1597 NOTC1       MOV      A,HIDMA             LOOK AT THE 8530 REG. POINTER
000520 B4FF02          FF    0525  1598             CJNE     A,#X'FF',I_O_8530A  IF NO 'ESCAPE', CONTINUE INIT.
000523 8024            0549        1599             SJMP     S_PARMS_1           JUMP IF 'ESCAPE' INDICATED

000525 758398            83    98  1601 I_O_8530A   MOV      DPH,#H8530A         SET UP HI 8530 ADDRESS
000528 758201            82    01  1602             MOV      DPL,#L8530A         SET UP LO 8530 ADDRESS
00052B E531                  31    1603             MOV      A,HIDMA             GET 8530 ADDR PTR VALUE
00052D F0                          1604             MOVX     @DPTR,A             SET UP 8530 ADDR POINTER
00052E FC                          1605             MOV      WORK4,A             SAVE 8530 ADDR POINTER
00052F E530                  30    1606             MOV      A,LODMA             FETCH DATA BYTE
000531 F0                          1607             MOVX     @DPTR,A             WRITE DATA VALUE TO 8530

                                   1609 *  CHECK IF THE REG TO BE WRITTEN IS A SAVE REGISTER

000532 BC0304            03  0539  1611             CJNE     WORK4,#R3A8530,J11  JMP IF SAVE NOT REQUIRED
000535 F550              50        1612             MOV      R3A8530S,A          SAVE REG VALUE
000537 800C            0545        1613             SJMP     CHKTC1              JMP TO CHK FOR TERMINAL CNT
000539 BC0504            05  0540  1614 J11          CJNE     WORK4,#R5A8530,J12  JMP IF SAVE NOT REQUIRED
00053C F551              51        1615             MOV      R5A8530S,A          SAVE REG VALUE
00053E 8005            0545        1616             SJMP     CHKTC1              JMP TO CHK FOR TERMINAL CNT
000540 BC0A02            0A  0545  1617 J12          CJNE     WORK4,#RAA8530,CHKTC1  JMP IF SAVE NOT REQ'D
000543 F552              52        1618             MOV      RAA8530S,A          SAVE REG VALUE
000545 3037CE          26.7  0516  1619 CHKTC1      JNB      TERMCNT,IN8530A     JUMP IF TC WAS WAS NOT SET
000548 22                          1620             RET                          RETURN TO CALLING RTN
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86
                                   1622 ********************************************************************************
                                   1623 **                                                                            **
                                   1624 **          SET UP ASYNC UNIQUE PARAMETERS FOR PORT 1                         **
                                   1625 **                                                                            **
                                   1626 ********************************************************************************

                                   1628 *  FETCH DATA PAIR FROM SYSTEM MEMORY

000549 E6                          1630 S_PARMS_1  MOV     A,@R0               MOV CMD CODE/DMA CHAN TO ACC
00054A 120678          0678        1631            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1633 * 1ST BYTE IS JUNK
                                   1634 * 2ND BYTE IS MODEM INTERRUPT MASK

00054D 853146            46    31 1636            MOV     MODMMSK1,HIDMA      SAVE VALUE IN INTERNAL RAM

                                   1638 *  FETCH DATA PAIR FROM SYSTEM MEMORY

000550 E6                          1640            MOV     A,@R0               MOV CMD CODE/DMA CHAN TO ACC
000551 120678          0678        1641            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1643 * 1ST BYTE IS ASC FLAG 1
                                   1644 * 2ND BYTE IS ASC FLAG 2

000554 853024            24    30 1646            MOV     ASCFL1P1,LODMA      SAVE VALUE IN BUFFER AREA
000557 853138            38    31 1647            MOV     ASCFL2P1,HIDMA      SAVE VALUE IN BUFFER AREA

                                   1649 *  FETCH DATA PAIR FROM SYSTEM MEMORY

00055A E6                          1651            MOV     A,@R0               MOVE CMD CODE/DMA CHAN TO ACC
00055B 120678          0678        1652            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1654 *  STORE RECEIVE XOFF AND XON COMPARE VALUES IN THEIR SAVE BUFFERS

00055E 853049            49    30 1656            MOV     XONRCV1,LODMA       SAVE XON COMP CHAR
000561 853148            48    31 1657            MOV     XOFFRCV1,HIDMA      SAVE XOFF COMP CHAR

                                   1659 *  FETCH DATA PAIR FROM SYSTEM MEMORY

000564 E6                          1661            MOV     A,@R0               MOVE CMD CODE/DMA CHAN TO ACC
000565 120678          0678        1662            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1664 *  STORE XMIT XOFF AND XON VALUES IN THEIR SAVE BUFFERS

000568 85304B            4B    30 1666            MOV     XONXMT1,LODMA       SAVE XON COMP CHAR
00056B 85314A            4A    31 1667            MOV     XOFFXMT1,HIDMA      SAVE XOFF COMP CHAR

                                   1669 *
                                   1670 *
                                   1671 *        BEGINNING OF CODE TO SETUP MARK/SPACE PARITY PARMS.
                                   1672 *
                                   1673 *
00056E E538                  38    1674            MOV     A,ASCFL2P1          RETRIEVE FLAG 2
```

```
  LOC  OBJECT CODE     ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86

000570 5403                  03   1675            ANL     A,#X'03'            MASK ALL BUT CHAR. LENGTH FIELD
000572 302336          24.3  05AB   1676            JNB     MSPAREN1,NOMSPTY1   JUMP IF NOT MARK OR SPACE PTY.
000575 30221E          24.2  0596   1677            JNB     MARKPAR1,P1SPACE    JUMP IF NOT MARK PARITY
000578 B40108            01  0583   1678            CJNE    A,#X'01',CK6MARK1   JUMP IF NOT 7 BITS (TOTAL)
                                    1679 *
                                    1680 *      CHARACTER IS 6 DATA BITS PLUS MARK PARITY BIT
                                    1681 *
00057B 753440            34    40   1682            MOV     XMTMSK1,#X'40'      OR MASK TO SET MARK PARITY BIT
00057E 75363F            36    3F   1683            MOV     RSTPMSK1,#X'3F'     AND MASK TO STRIP NON DATA BITS
000581 8043            05C6         1684            SJMP    PASSTAT             JUMP TO CONSOLIDATE PROCESSING
000583 B40208            02  058E   1685 CK6MARK1   CJNE    A,#X'02',CK8MARK1   JUMP IF NOT 6 BITS (TOTAL)
                                    1686 *
                                    1687 *      CHARACTER IS 5 DATA BITS PLUS MARK PARITY BIT
                                    1688 *
000586 753420            34    20   1689            MOV     XMTMSK1,#X'20'      OR MASK TO SET MARK PARITY BIT
000589 75361F            36    1F   1690            MOV     RSTPMSK1,#X'1F'     AND MASK TO STRIP NON DATA BITS
00058C 8038            05C6         1691            SJMP    PASSTAT             JUMP TO CONSOLIDATE PROCESSING
                                    1692 *
                                    1693 *      CHARACTER IS 7 DATA BITS PLUS MARK PARITY BIT
                                    1694 *
00058E 753480            34    80   1695 CK8MARK1   MOV     XMTMSK1,#X'80'      OR MASK TO SET MARK PARITY BIT
000591 75367F            36    7F   1696            MOV     RSTPMSK1,#X'7F'     AND MASK TO STRIP NON DATA BITS
000594 8030            05C6         1697            SJMP    PASSTAT             RESUME PRIOR PROCESSING
                                    1698 *
                                    1699 *      SPACE PARITY PARAMETERS
                                    1700 *
000596 B40105            01  059E   1701 P1SPACE    CJNE    A,#X'01',CK6SPC1    JUMP IF NOT 7 BITS (TOTAL)
                                    1702 *
                                    1703 *      CHARACTER IS 6 DATA BITS PLUS SPACE PARITY BIT
                                    1704 *
000599 75363F            36    3F   1705            MOV     RSTPMSK1,#X'3F'     AND MASK TO CLR SPACE PARITY BIT
00059C 8028            05C6         1706            SJMP    PASSTAT             JUMP TO CONSOLIDATE PROCESSING
00059E B40205            02  05A6   1707 CK6SPC1    CJNE    A,#X'02',CK8SPC1    JUMP IF NOT 6 BITS (TOTAL)
                                    1708 *
                                    1709 *      CHARACTER IS 5 DATA BITS PLUS SPACE PARITY BIT
                                    1710 *
0005A1 75361F            36    1F   1711            MOV     RSTPMSK1,#X'1F'     AND MASK TO CLR SPACE PARITY BIT
0005A4 8020            05C6         1712            SJMP    PASSTAT             JUMP TO CONSOLIDATE PROCESSING
                                    1713 *
                                    1714 *      CHARACTER IS 7 DATA BITS PLUS SPACE PARITY BIT
                                    1715 *
0005A6 75367F            36    7F   1716 CK8SPC1    MOV     RSTPMSK1,#X'7F'     AND MASK TO CLR SPACE PARITY BIT
0005A9 801B            05C6         1717            SJMP    PASSTAT             RESUME PRIOR PROCESSING
                                    1718 *
                                    1719 *      NEITHER MARK OR SPACE IS ACTIVE, SETUP STRIP MASK ONLY
                                    1720 *
0005AB B40005            00  05B3   1721 NOMSPTY1   CJNE    A,#X'00',CK6NMS1    JUMP IF NOT 5 DATA BITS
                                    1722 *
                                    1723 *      CHARACTER IS 5 DATA BITS
                                    1724 *
0005AE 75361F            36    1F   1725            MOV     RSTPMSK1,#X'1F'     SET STRIP MASK FOR 7 DATA BITS
0005B1 8013            05C6         1726            SJMP    PASSTAT             RESUME PRIOR PROCESSING
0005B3 B40205            02  05BB   1727 CK6NMS1    CJNE    A,#X'02',CK7NMS1    JUMP IF NOT 6 DATA BITS
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                   1723 *
                                   1729 *      CHARACTER IS 6 DATA BITS
                                   1730 *
0005B6 75363F            36    3F  1731              MOV     RSTPMSK1,#X'3F'     SET STRIP MASK FOR 6 DATA BITS
0005B9 800B            05C6        1732              SJMP    PASSTAT             RESUME PRIOR PROCESSING
0005BB B40105            01  05C3  1733 CK7NMS1      CJNE    A,#X'01',CK8NMS1    JUMP IF NOT 7 DATA BITS
                                   1734 *
                                   1735 *      CHARACTER IS 7 DATA BITS
                                   1736 *
0005BE 75367F            36    7F  1737              MOV     RSTPMSK1,#X'7F'     SET STRIP MASK FOR 7 DATA BITS
0005C1 8003            05C6        1738              SJMP    PASSTAT             RESUME PRIOR PROCESSING
                                   1739 *
                                   1740 *      CHARACTER IS 8 DATA BITS
                                   1741 *
0005C3 7536FF            36    FF  1742 CK8NMS1      MOV     RSTPMSK1,#X'FF'     SET STRIP MASK FOR 7 DATA BITS
                                   1743 *                                        RESUME PRIOR PROCESSING
                                   1744 *                                        (FALL THRU TO PASSTAT)
                                   1745 *
                                   1746 *
                                   1747 *         END OF CODE TO SET UP MARK/SPACE PARITY PARMS.
                                   1748 *
                                   1749 *

                                   1751 *  COMMAND IS COMPLETE SO PASS STATUS

0005C6 22                          1753 PASSTAT      RET                         RETURN TO CALLING ROUTINE
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86
                                   1755 ********************************************************************************
                                   1756 **                                                                            **
                                   1757 **          INITIALIZE 8530 CHANNEL B REGISTERS                               **
                                   1758 **                                                                            **
                                   1759 ********************************************************************************

0005C7 E6                          1761 IN8530B     MOV     A,@R0              MOVE CMD CODE/DMA CHAN TO ACC

                                   1763 *  FETCH ADDRESS/DATA PAIR FROM SYSTEM MEMORY

0005C8 120678          0678        1765             LCALL   DMATOADP           CALL DMA TO ADP RTN

                                   1767 *  THE ACC HAS THE DMA RETURN CODE

0005CB 6002            05CF        1769             JZ      NOTC2              JUMP IF TC IS NOT RETURNED

                                   1771 *  CHECK IF A TERM COUNT OCCURRED ON THE DMA TRANSFER

0005CD D237            26.7        1773             SETBIT  TERMCNT            SET GENERAL TERM CNT FLAG

0005CF E531                  31    1775 NOTC2       MOV     A,HIDMA            LOOK AT THE 8530 REG. POINTER
0005D1 B4FF02          FF    05D6  1776             CJNE    A,#X'FF',I_O_8530B IF NO 'ESCAPE', CONTINUE INIT.
0005D4 8024            05FA        1777             SJMP    S_PARMS_2          JUMP IF 'ESCAPE' INDICATED

0005D6 758398            83    98  1779 I_O_8530B  MOV     DPH,#H8530B        SET UP HI 8530 ADDRESS
0005D9 758200            82    00  1780             MOV     DPL,#L8530B        SET UP LO 8530 ADDRESS
0005DC E531                  31    1781             MOV     A,HIDMA            GET 8530 ADDR PTR VALUE
0005DE F0                          1782             MOVX    @DPTR,A            SET UP 8530 ADDR POINTER
0005DF FC                          1783             MOV     WORK4,A            SAVE 8530 ADDR POINTER
0005E0 E530                  30    1784             MOV     A,LODMA            GET 8530 DATA VALUE
0005E2 F0                          1785             MOVX    @DPTR,A            WRITE DATA VALUE TO 8530

                                   1787 *  CHECK IF THE REG TO BE WRITTEN IS A SAVE REGISTER

0005E3 BC0304            03    05EA  1789             CJNE    WORK4,#R3B8530,J21 JMP IF SAVE NOT REQUIRED
0005E6 F553              53        1790             MOV     R3B8530S,A         SAVE REG VALUE
0005E8 800C            05F6        1791             SJMP    CHKTC2             JMP TO CHK FOR TERMINAL CNT
0005EA BC0504            05    05F1  1792 J21        CJNE    WORK4,#R5B8530,J22 JMP IF SAVE NOT REQUIRED
0005ED F554              54        1793             MOV     R5B8530S,A         SAVE REG VALUE
0005EF 8005            05F6        1794             SJMP    CHKTC2             JMP TO CHK FOR TERMINAL CNT
0005F1 BC0A02            0A    05F6  1795 J22        CJNE    WORK4,#RAB8530,CHKTC2  JMP IF SAVE NOT REQUIRED
0005F4 F555              55        1796             MOV     RAB8530S,A         SAVE REG VALUE
0005F6 3037CE          26.7  05C7  1797 CHKTC2     JNB     TERMCNT,IN8530B    JUMP IF TC WAS NOT SET ON
0005F9 22                          1798             RET                        RETURN TO CMD DECODER
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                    ASM51 V1.9 07.09 05/09/86
                                   1800 ************************************************************************
                                   1801 **                                                                     **
                                   1802 **         SET UP ASYNC UNIQUE PARAMETERS FOR PORT 2                   **
                                   1803 **                                                                     **
                                   1804 ************************************************************************

                                   1806 *  FETCH DATA PAIR FROM SYSTEM MEMORY

0005FA E6                          1808 S_PARMS_2  MOV     A,@R0               MOV CMD CODE/DMA CHAN TO ACC
0005FB 120678          0678        1809            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1811 * 1ST BYTE IS JUNK
                                   1812 * 2ND BYTE IS MODEM INTERRUPT MASK

0005FE 853147            47    31  1814            MOV     MODMMSK2,HIDMA      SAVE VALUE IN INTERNAL RAM

                                   1816 *  FETCH DATA PAIR FROM SYSTEM MEMORY

000601 E6                          1818            MOV     A,@R0               MOV CMD CODE/DMA CHAN TO ACC
000602 120678          0678        1819            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1821 * 1ST BYTE IS ASC FLAG 1
                                   1822 * 2ND BYTE IS ASC FLAG 2

000605 853025            25    30  1824            MOV     ASCFL1P2,LODMA      SAVE VALUE IN BUFFER AREA
000608 853139            39    31  1825            MOV     ASCFL2P2,HIDMA      SAVE VALUE IN BUFFER AREA

                                   1827 *  FETCH DATA PAIR FROM SYSTEM MEMORY

00060B E6                          1829            MOV     A,@R0               MOVE CMD CODE/DMA CHAN TO ACC
00060C 120678          0678        1830            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1832 *  STORE RECEIVE XOFF AND XON COMPARE VALUES IN THEIR SAVE BUFFERS

00060F 85304D            4D    30  1834            MOV     XONRCV2,LODMA       SAVE XON COMP CHAR
000612 85314C            4C    31  1835            MOV     XOFFRCV2,HIDMA      SAVE XOFF COMP CHAR

                                   1837 *  FETCH DATA PAIR FROM SYSTEM MEMORY

000615 E6                          1839            MOV     A,@R0               MOVE CMD CODE/DMA CHAN TO ACC
000616 120678          0678        1840            LCALL   DMATOADP            CALL DMA TO ADP RTN

                                   1842 *  STORE XMIT XOFF AND XON VALUES IN THEIR SAVE BUFFERS

000619 85304F            4F    30  1844            MOV     XONXMT2,LODMA       SAVE XON COMP CHAR
00061C 85314E            4E    31  1845            MOV     XOFFXMT2,HIDMA      SAVE XOFF COMP CHAR

                                   1847 *
                                   1848 *
                                   1849 *        BEGINNING OF CODE TO SETUP MARK/SPACE PARITY PARMS.
                                   1850 *
                                   1851 *
00061F E539                  39    1852            MOV     A,ASCFL2P2          RETRIEVE FLAG 2
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
000621 5403                 03    1853            ANL     A,#X'03'            MASK ALL BUT CHAR. LENGTH FIELD
000623 302B36           25.3  065C  1854            JNB     MSPAREN2,NOMSPTY2   JUMP IF NOT MARK OR SPACE PTY.
000626 302A1E           25.2  0647  1855            JNB     MARKPAR2,P2SPACE    JUMP IF NOT MARK PARITY
000629 B40108             01  0634  1856            CJNE    A,#X'01',CK6MARK2   JUMP IF NOT 7 BITS (TOTAL)
                                    1857 *
                                    1858 *      CHARACTER IS 6 DATA BITS PLUS MARK PARITY BIT
                                    1859 *
00062C 753540             35    40  1860            MOV     XMTMSK2,#X'40'      OR MASK TO SET MARK PARITY BIT
00062F 75373F             37    3F  1861            MOV     RSTPMSK2,#X'3F'     AND MASK TO STRIP NON DATA BITS
000632 8043             0677        1862            SJMP    PASSTAT_2           JUMP TO CONSOLIDATE PROCESSING
000634 B40208             02  063F  1863 CK6MARK2    CJNE    A,#X'02',CK8MARK2   JUMP IF NOT 6 BITS (TOTAL)
                                    1864 *
                                    1865 *      CHARACTER IS 5 DATA BITS PLUS MARK PARITY BIT
                                    1866 *
000637 753520             35    20  1867            MOV     XMTMSK2,#X'20'      OR MASK TO SET MARK PARITY BIT
00063A 75371F             37    1F  1868            MOV     RSTPMSK2,#X'1F'     AND MASK TO STRIP NON DATA BITS
00063D 8038             0677        1869            SJMP    PASSTAT_2           JUMP TO CONSOLIDATE PROCESSING
                                    1870 *
                                    1871 *      CHARACTER IS 7 DATA BITS PLUS MARK PARITY BIT
                                    1872 *
00063F 753580             35    80  1873 CK8MARK2   MOV     XMTMSK2,#X'80'      OR MASK TO SET MARK PARITY BIT
000642 75377F             37    7F  1874            MOV     RSTPMSK2,#X'7F'     AND MASK TO STRIP NON DATA BITS
000645 8030             0677        1875            SJMP    PASSTAT_2           RESUME PRIOR PROCESSING
                                    1876 *
                                    1877 *      SPACE PARITY PARAMETERS
                                    1878 *
000647 B40105             01  064F  1879 P2SPACE     CJNE    A,#X'01',CK6SPC2    JUMP IF NOT 7 BITS (TOTAL)
                                    1880 *
                                    1881 *      CHARACTER IS 6 DATA BITS PLUS SPACE PARITY BIT
                                    1882 *
00064A 75373F             37    3F  1883            MOV     RSTPMSK2,#X'3F'     AND MASK TO CLR SPACE PARITY BIT
00064D 8028             0677        1884            SJMP    PASSTAT_2           JUMP TO CONSOLIDATE PROCESSING
00064F B40205             02  0657  1885 CK6SPC2    CJNE    A,#X'02',CK8SPC2    JUMP IF NOT 6 BITS (TOTAL)
                                    1886 *
                                    1887 *      CHARACTER IS 5 DATA BITS PLUS SPACE PARITY BIT
                                    1888 *
000652 75371F             37    1F  1889            MOV     RSTPMSK2,#X'1F'     AND MASK TO CLR SPACE PARITY BIT
000655 8020             0677        1890            SJMP    PASSTAT_2           JUMP TO CONSOLIDATE PROCESSING
                                    1891 *
                                    1892 *      CHARACTER IS 7 DATA BITS PLUS SPACE PARITY BIT
                                    1893 *
000657 75377F             37    7F  1894 CK8SPC2    MOV     RSTPMSK2,#X'7F'     AND MASK TO CLR SPACE PARITY BIT
00065A 801B             0677        1895            SJMP    PASSTAT_2           RESUME PRIOR PROCESSING
                                    1896 *
                                    1897 *      NEITHER MARK OR SPACE IS ACTIVE, SETUP STRIP MASK ONLY
                                    1898 *
00065C B40005             00  0664  1899 NOMSPTY2   CJNE    A,#X'00',CK6NMS2    JUMP IF NOT 5 DATA BITS
                                    1900 *
                                    1901 *      CHARACTER IS 5 DATA BITS
                                    1902 *
00065F 75371F             37    1F  1903            MOV     RSTPMSK2,#X'1F'     SET STRIP MASK FOR 7 DATA BITS
000662 8013             0677        1904            SJMP    PASSTAT_2           RESUME PRIOR PROCESSING
000664 B40205             02  066C  1905 CK6NMS2    CJNE    A,#X'02',CK7NMS2    JUMP IF NOT 6 DATA BITS
```

```
SASC     Sample MP ASC Microcode                                                    PAGE   52

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                          ASM51 V1.9 07.09 05/09/86

                                   1906 *
                                   1907 *      CHARACTER IS 6 DATA BITS
                                   1908 *
000667 75373F            37    3F  1909            MOV     RSTPMSK2,#X'3F'     SET STRIP MASK FOR 6 DATA BITS
00066A 800B            0677        1910            SJMP    PASSTAT_2           RESUME PRIOR PROCESSING
00066C B40105            01  0674  1911 CK7NMS2     CJNE    A,#X'01',CK8NMS2    JUMP IF NOT 7 DATA BITS
                                   1912 *
                                   1913 *      CHARACTER IS 7 DATA BITS
                                   1914 *
00066F 75377F            37    7F  1915            MOV     RSTPMSK2,#X'7F'     SET STRIP MASK FOR 7 DATA BITS
000672 8003            0677        1916            SJMP    PASSTAT_2           RESUME PRIOR PROCESSING
                                   1917 *
                                   1918 *      CHARACTER IS 8 DATA BITS
                                   1919 *
000674 7537FF            37    FF  1920 CK8NMS2     MOV     RSTPMSK2,#X'FF'     SET STRIP MASK FOR 7 DATA BITS
                                   1921 *                                      RESUME PRIOR PROCESSING
                                   1922 *                                      (FALL THRU TO PASSTAT)
                                   1923 *
                                   1924 *
                                   1925 *         END OF CODE TO SET UP MARK/SPACE PARITY PARMS.
                                   1926 *
                                   1927 *

                                   1929 *  COMMAND IS COMPLETE SO PASS STATUS

000677 22                          1931 PASSTAT_2  RET                         RETURN TO CALLING ROUTINE
```

```
SASC     Sample MP ASC Microcode                                                    PAGE   53

  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                          ASM51 V1.9 07.09 05/09/86

                                   1933 ********************************************************************************
                                   1934 **                                                                            **
                                   1935 **          DMA FROM THE SYSTEM TO THE ADAPTER                                **
                                   1936 **                                                                            **
                                   1937 ********************************************************************************

                                   1939 *  THE DMA CHANNEL IS IN LOW 2 BITS OF ACCUMULATOR

000678 5403                  03    1941 DMATOADP   ANL     A,#X'03'            AND OFF NON-DMA ENCODE BITS
00067A 4290              90        1942            ORL     P1,A                OR DMA ENCODE BITS TO P1
00067C D292            90.2        1943            SETBIT  DMAREQEN            ENABLE DMA REQUEST
00067E 00                          1944            NOP                         WAIT FOR DREQ TO OCCUR
00067F 2094FD          90.4  067F  1945 WAITDACK   JB      DACKBACK,WAITDACK   WAIT TILL DMA IS COMPLETE
000682 758388            83    88  1946            MOV     DPH,#ADRHIDMA       SET UP MOVX ADDR=HI DMA DATA REG
000685 E0                          1947            MOVX    A,@DPTR             READ HI DMA DATA BYTE
000686 F531              31        1948            MOV     HIDMA,A             MOVE HI DMA BYTE TO PASS BUFF
000688 758380            83    80  1949            MOV     DPH,#ADRLODMA       SET UP MOVX ADDR=LO DMA DATA REG
00068B E0                          1950            MOVX    A,@DPTR             READ LO DMA DATA BYTE
00068C F530              30        1951            MOV     LODMA,A             MOVE LO DMA BYTE TO PASS BUFF
00068E E4                          1952            CLR     A                   MOVE NO TC RET CODE TO ACC
00068F 20B002          B0.0  0694  1953            JB      TC,NO_TC            JMP IF TC FROM 8237 IS NOT ON
000692 74FF                  FF    1954            MOV     A,#X'FF'            MOVE TC RETURN CODE TO ACC
000694 5390F8            90    F8  1955 NO_TC      ANL     P1,#X'F8'           AND OFF DMA ENABLE/ENCODE BITS
000697 22                          1956            RET                         RETURN TO CALLING ROUTINE
```

```
LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86

                                 1958 ************************************************************************
                                 1959 **                                                                    **
                                 1960 **          DMA FROM THE ADAPTER TO THE SYSTEM                        **
                                 1961 **                                                                    **
                                 1962 **           (This routine commented out because it is not used       **
                                 1963 **            by this program, and is included for illustration       **
                                 1964 **            purposes only).                                         **
                                 1965 **                                                                    **
                                 1966 ************************************************************************

                                 1968 *  THE DMA CHANNEL IS IN LOW 2 BITS OF ACCUMULATOR

                                 1970 *DMAFRADP  ANL     A,#X'03'            AND OFF NON-DMA ENCODE BITS
                                 1971 *          ORL     P1,A                OR DMA ENCODE BITS TO P1
                                 1972 *          MOV     A,HIDMA             MOVE HI DMA BYTE FROM PASS BUFF
                                 1973 *          MOV     DPH,#ADRHIDMA       SET UP MOVX ADDR=HI DMA DATA REG
                                 1974 *          MOVX    @DPTR,A             WR HI DMA DATA BYTE TO DMA REG
                                 1975 *          MOV     DPH,#ADRLODMA       SET UP MOVX ADDR=LO DMA DATA REG
                                 1976 *          MOV     A,LODMA             MOVE LO DMA BYTE FROM PASS BUFF
                                 1977 *          MOVX    @DPTR,A             WR LO DMA DATA BYTE TO DMA REG
                                 1978 *          SETBIT  DMAREQEN            ENABLE DMA REQUEST
                                 1979 *          NOP                         WAIT FOR DREQ TO OCCUR
                                 1980 *WTDACK    JB      DACKBACK,WTDACK     WAIT TILL DMA IS COMPLETE
                                 1981 *          CLR     A                   MOVE NO TC RET CODE TO ACC
                                 1982 *          JB      TC,NOTC2            JUMP IF NO TC WAS RETURNED
                                 1983 *          MOV     A,#X'FF'            MOVE RETURN CODE TO ACC
                                 1984 *NOTC2     ANL     P1,#X'F8'           AND OFF DMA ENABLE/ENCODE BITS
                                 1985 *          RET                         RETURN TO CALLING ROUTINE
```



```
LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86

                                 1987 ************************************************************************
                                 1988 **                                                                    **
                                 1989 **          UPDATE THE COMMAND STACK EXECUTION PTR AND COUNT VALUE     **
                                 1990 **                                                                    **
                                 1991 ************************************************************************

000698 C2AF          A8.7        1993 CMDSTUPD   CLR     EA                  DISABLE ALL INTERRUPTS
00069A 1A                        1994             DEC     CMDCNT              DECREMENT THE CMD COUNT
00069B 08                        1995             INC     CMDEXPTR            INC CMD EXEC PTR
00069C 7410                10    1996             MOV     A,#ENDSTACK         MOVE END OF STK + 1 TO ACC
00069E B50002        00    06A3  1997             CJNE    A,RB0R0,ENDUPDT     JMP IF PTR IS NOT TO BE ROLLED
0006A1 7808                08    1998             MOV     CMDEXPTR,#CMDST0    MOVE PTR TO BOTTOM OF STACK
0006A3 D2AF          A8.7        1999 ENDUPDT    SETBIT  EA                  ENABLE ALL INTERRUPTS
0006A5 22                        2000             RET                         RETURN TO CALLING RTN
```

```
  LOC  OBJECT CODE     ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                    2002 ************************************************************************
                                    2003 **                                                                    **
                                    2004 **         WRITE THE MASTER STATUS BYTE (MSB) TO THE 8255 TO CAUSE    **
                                    2005 **         A SYSTEM INTERRUPT.                                        **
                                    2006 **                                                                    **
                                    2007 ************************************************************************

0006A6 20B3FD          B0.3  06A6  2009 INTRSYS     JB      IBF,INTRSYS          WAIT IF SYST HASN'T COMPLETED RD
0006A9 D214            22.4        2010             SETBIT  STINPROG             SET STATUS PASS IN PROGRESS FLAG

0006AB C28B            88.3        2012             CLR     IE1                  CLEAR PREVIOUS INT1 INTERRUPTS
0006AD D2AA            A8.2        2013             SETBIT  EX1                  ENABLE INT1'S ON MSB READ
0006AF 758390            83    90  2014             MOV     DPH,#ADR8255         SET UP 8255 ADDRESS
0006B2 E520                    20  2015             MOV     A,MSB                MOVE MSB TO ACC
0006B4 F0                          2016             MOVX    @DPTR,A              MOVE MSB TO SYSTEM BUFFER
0006B5 22                          2017             RET                          RETURN TO CALLING RTN
```



```
  LOC  OBJECT CODE     ADDR1 ADDR2  STMT SOURCE STATEMENT                                  ASM51 V1.9 07.09 05/09/86
                                    2019 ************************************************************************
                                    2020 **                                                                    **
                                    2021 **  INT 0 INTERRUPT HANDLER, CHECK FOR OBF AS SOURCE                   **
                                    2022 **                                                                    **
                                    2023 ************************************************************************

0006B6 C083              83        2025 SERVINT0    PUSH    DPH                  SAVE DATA PTR VALUE
0006B8 30B503          B0.5  06BE  2026              JNB     OBF,HNDLOBF          JUMP IF OBF INTERRUPT
0006BB D083              83        2027 INT0DONE    POP     DPH                  RESTORE DATA PTR VALUE
0006BD 22                          2028             RET                          RETURN IMMEDIATELY IF NOT OBF



                                    2033 ************************************************************************
                                    2034 **                                                                    **
                                    2035 **  OBF INTERRUPT HANDLER ROUTINE                                     **
                                    2036 **  IF CMD STACK FULL, LEAVE CMD IN OB; ELSE MOVE CMD ONTO CMD STACK  **
                                    2037 **                                                                    **
                                    2038 ************************************************************************

0006BE 0A                          2040 HNDLOBF     INC     CMDCNT               INCR THE CMD COUNT
0006BF BA0804            08  06C6  2041              CJNE    CMDCNT,#X'08',CMDOK  JUMP IF CMD OVFLO DIDN'T OCCUR
0006C2 D217            22.7        2042              SETBIT  CMDOVFLO             SET CMD OVERFLO FLAG
0006C4 80F5            06BB        2043              SJMP    INT0DONE             JUMP TO RESTORE DPH & RETURN
0006C6 758390            83    90  2044 CMDOK       MOV     DPH,#ADR8255         ELSE RD CMD, SET UP MOVX ADDR
0006C9 E0                          2045             MOVX    A,@DPTR              MOVE COMMAND INTO ACC
0006CA F7                          2046             MOV     @R1,A                MOVE COMMAND ONTO CMD STACK
0006CB 09                          2047             INC     CMDSTPTR             INCR CMD STACK PTR
0006CC 7410                  10    2048             MOV     A,#ENDSTACK          MOVE ADDR OF TOP OF STK TO ACC
0006CE B501EA            01  06BB  2049             CJNE    A,RB0R1,INT0DONE     JMP IF PTR NOT TO BE ROLLED OVER
0006D1 7908                  08    2050             MOV     CMDSTPTR,#CMDST0     ROLL CMD PTR BACK TO BOT OF STK
0006D3 80E6            06BB        2051             SJMP    INT0DONE             JMP TO RESTORE DPH & RETURN
```

```
LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                    ASM51 V1.9 07.09 05/09/86
                                 2053 ************************************************************************
                                 2054 **                                                                    **
                                 2055 **  IBF INTERRUPT HANDLER ROUTINE                                     **
                                 2056 **    MASTER STATUS BYTE HAS BEEN READ BY SYSTEM PROCESSOR,           **
                                 2057 **    PASS 0, 1, OR 2 ADDITIONAL BYTES AS REQUIRED BY THE             **
                                 2058 **    TYPE OF STATUS PASS.                                            **
                                 2059 **                                                                    **
                                 2060 ************************************************************************
                                 2061 **
                                 2062 **
                                 2063 **  Sample Async Microcode Status Byte Definition
                                 2064 **
                                 2065 **
                                 2066 **       Event                Status Returned
                                 2067 **       =====                ===============
                                 2068 **
                                 2069 **  1) General Command        3 Bytes Returned:
                                 2070 **       Completion
                                 2071 **                            ---------------------------------
                                 2072 **                           | Master Status Byte (20 or 30) |
                                 2073 **                            ---------------------------------
                                 2074 **                           | Command Code Byte             |
                                 2075 **                            ---------------------------------
                                 2076 **                           | Addl Cmd Status Byte          |
                                 2077 **                            ---------------------------------
                                 2078 **
                                 2079 **
                                 2080 **  2) Enable Modem           3 Bytes Returned:
                                 2081 **       Intrs. Cmd
                                 2082 **                            ---------------------------------
                                 2083 **                           | Master Status Byte ('20'H)    |
                                 2084 **                            ---------------------------------
                                 2085 **                           | Command Code Byte (35 or 3D)  |
                                 2086 **                            ---------------------------------
                                 2087 **                           | Current Ifc Inputs            |
                                 2088 **                            ---------------------------------
                                 2089 **
                                 2090 **
                                 2091 **  3) Transmit Complete      1 Byte Returned:
                                 2092 **       Intrs. Cmd
                                 2093 **                            ---------------------------------
                                 2094 **                           | Master Status Byte ('84'H)    |
                                 2095 **                            ---------------------------------
                                 2096 **
                                 2097 **
                                 2098 **  4) Rx without Error       2 Bytes Returned:
                                 2099 **
                                 2100 **                            ---------------------------------
                                 2101 **                           | Master Status Byte ('81'H)    |
                                 2102 **                            ---------------------------------
                                 2103 **                           | Receive Data byte             |
                                 2104 **                            ---------------------------------
                                 2105 **
```

```
  LOC  OBJECT CODE    ADDR1 ADDR2  STMT SOURCE STATEMENT                                ASM51 V1.9 07.09 05/09/86
                                   2106 **
                                   2107 **  5) Rx with 'Error'      3 Bytes Returned:
                                   2108 **
                                   2109 **                          ---------------------------------
                                   2110 **                         | Master Status Byte ('83'H)    |
                                   2111 **                          ---------------------------------
                                   2112 **                         | Receive Data byte             |
                                   2113 **                          ---------------------------------
                                   2114 **                         | Error Code byte               |
                                   2115 **                          ---------------------------------
                                   2116 **
                                   2117 **
                                   2118 **  6) Modem Interrupt      3 Bytes Returned:
                                   2119 **
                                   2120 **                          ---------------------------------
                                   2121 **                         | Master Status Byte ('08'H)    |
                                   2122 **                          ---------------------------------
                                   2123 **                         | Modem Inputs Value            |
                                   2124 **                          ---------------------------------
                                   2125 **                         | Delta Bits Mask               |
                                   2126 **                          ---------------------------------
                                   2127 **
                                   2128 **                                                            **
                                   2129 ************************************************************************

0006D5 C083           83           2131 SERVINT1   PUSH    DPH                     SAVE DATA PTR VALUE
0006D7 758390         83    90     2132            MOV     DPH,#ADR8255            IBF INTR,SET UP ADDRESS FOR MOV
0006DA E53C                 3C     2133            MOV     A,STATCNT               MOV JMP TABLE OFFSET +1 TO ACC
0006DC B40208         02    06EA   2134            CJNE    A,#TWOBYTE,CHK_ONE      CHECK FOR TWO ADD'L BYTES
0006DF E53A                 3A     2135            MOV     A,STAT0
0006E1 F0                          2136            MOVX    @DPTR,A                 WRITE STATUS BYTE TO SYSTEM BUF
0006E2 20B3FD         B0.3  06E2   2137 WAIT_0     JB      IBF,WAIT_0              WAIT FOR SYSTEM TO READ IT
0006E5 E53B                 3B     2138            MOV     A,STAT1
0006E7 F0                          2139            MOVX    @DPTR,A                 WRITE STATUS BYTE TO SYSTEM BUF
0006E8 8006           06F0         2140            SJMP    ENDSTAT                 JUMP TO END STAT PASS
0006EA B40103         01    06F0   2141 CHK_ONE    CJNE    A,#ONEBYTE,ENDSTAT      NOT ONE, MUST BE ZERO, EXIT
0006ED E53A                 3A     2142            MOV     A,STAT0                 MOVE STATUS BYTE 0 TO ACC
0006EF F0                          2143            MOVX    @DPTR,A                 WRITE STATUS BYTE TO SYSTEM BUF
0006F0 E4                          2144 ENDSTAT    CLR     A                       ZERO ACCUMULATOR
0006F1 F520           20           2145            MOV     MSB,A                   CLEAR MASTER STATUS
0006F3 F53A           3A           2146            MOV     STAT0,A                 CLEAR STATUS BYTE 0
0006F5 F53B           3B           2147            MOV     STAT1,A                 CLEAR STATUS BYTE 1
0006F7 F53C           3C           2148            MOV     STATCNT,A               CLEAR STATUS BYTE COUNT
0006F9 C214         22.4           2149            CLR     STINPROG                CLEAR STAT PASS IN PROGRESS FLAG
0006FB C2B4         B0.4           2150            CLR     P1P2INTR                SET DEFAULT INTR SRCE TO PORT 1
0006FD C2AA         A8.2           2151            CLR     EX1                     DISABLE IBF INTERRUPTS
0006FF D083           83           2152            POP     DPH                     RESTORE DATA PTR VALUE
000701 22                          2153            RET                             RETURN TO CALLING ROUTINE
                                   2154            END
```

POS.ID	REL.ID	FLAGS	ADDRESS
0001	0001	04	00 00004
0001	0001	04	00 00007
0001	0001	04	00 00068
0001	0001	04	00 00071
0001	0001	04	00 00098
0001	0001	04	00 000A1
0001	0001	04	00 000A7
0001	0001	04	00 000C9
0001	0001	04	00 000FA
0001	0001	04	00 00130
0001	0001	04	00 00136
0001	0001	04	00 00140
0001	0001	04	00 00146
0001	0001	04	00 0017E
0001	0001	04	00 001B8
0001	0001	04	00 001CA
0001	0001	04	00 001FB
0001	0001	04	00 00201
0001	0001	04	00 0020F
0001	0001	04	00 00220
0001	0001	04	00 00226
0001	0001	04	00 0027E
0001	0001	04	00 00284
0001	0001	04	00 002BE
0001	0001	04	00 002F8
0001	0001	04	00 0030A
0001	0001	04	00 0033D
0001	0001	04	00 00343
0001	0001	04	00 00351
0001	0001	04	00 00364
0001	0001	04	00 0036A
0001	0001	04	00 003CB
0001	0001	04	00 003CE
0001	0001	04	00 003D3
0001	0001	04	00 003DB
0001	0001	04	00 003E3
0001	0001	04	00 003EB
0001	0001	04	00 003FF
0001	0001	04	00 00402
0001	0001	04	00 0041D
0001	0001	04	00 00448
0001	0001	04	00 00451
0001	0001	04	00 00461
0001	0001	04	00 004E4
0001	0001	04	00 004EE
0001	0001	04	00 004F6
0001	0001	04	00 00510
0001	0001	04	00 00513
0001	0001	04	00 00518
0001	0001	04	00 0054B
0001	0001	04	00 00552
0001	0001	04	00 0055C
0001	0001	04	00 00566

POS.ID	REL.ID	FLAGS	ADDRESS
0001	0001	04	00 005C9
0001	0001	04	00 005FC
0001	0001	04	00 00603
0001	0001	04	00 0060D
0001	0001	04	00 00617

SYMBOL LEN VALUE DEFN REFERENCES ASM51 V1.9 07.09 05/09/86

```
A               1 00000008      0   501   502   503   504   506   507   508   509   532   533   539   545
                                    546   548   549   569   570   576   582   583   585   586   629   630
                                    632   633   634   653   654   655   656   661   662   663   664   669
                                    686   687   688   689   694   695   696   697   703   722   731   735
                                    744   754   776   792   793   802   818   819   841   883   884   886
                                    911   926   931   943   959   964   969   983   984   985   986   987
                                   1004  1013  1017  1026  1036  1059  1075  1076  1085  1101  1102  1124
                                   1167  1168  1170  1196  1211  1216  1228  1244  1249  1254  1268  1269
                                   1270  1271  1272  1333  1337  1346  1349  1352  1371  1376  1379  1391
                                   1394  1407  1414  1418  1419  1422  1423  1424  1425  1426  1427  1430
                                   1432  1434  1435  1436  1437  1438  1441  1444  1456  1460  1461  1464
                                   1465  1466  1467  1468  1469  1472  1474  1476  1477  1478  1479  1480
                                   1483  1490  1552  1554  1555  1557  1561  1583  1597  1598  1603  1604
                                   1605  1606  1607  1612  1615  1618  1630  1640  1651  1661  1674  1675
                                   1678  1685  1701  1707  1721  1727  1733  1761  1775  1776  1781  1782
                                   1783  1784  1785  1790  1793  1796  1808  1818  1829  1839  1852  1853
                                   1856  1863  1879  1885  1899  1905  1911  1941  1942  1947  1948  1950
                                   1951  1952  1954  1996  1997  2015  2016  2045  2046  2048  2049  2133
                                   2134  2135  2136  2138  2139  2141  2142  2143  2144  2145  2146  2147
                                   2148
AB              2 0000000C      0
AC              1 000000D6      0
ACC             1 000000E0      0   812   820   887  1095  1103  1171  1335  1338
ADDSTAT         1 00000005    242   760  1042
ADPMODE2        3   00048D   1454  1408
ADRHIDMA        1 00000088    135  1946
ADRLODMA        1 00000080    134  1949
ADRMDM1         1 000000A0    132   500   652
ADRMDM2         1 000000C0    133   505   685
ADR8255         1 00000090    131   628  2014  2046  2132
ALLSNTON1
                2   000211    894   887
ALLSNTON2
                2   000353   1178  1171
ASCFLAG         1 00000007    240   775   898  1057  1182
ASCFL1P1        1 00000024    268  1646
ASCFL1P2        1 00000025    276  1824
ASCFL2P1        1   000038    373  1647  1674
ASCFL2P2        1   000039    374  1825  1852
B               1 000000F0      0
BGEN            1 000000CB      0
BITADDR         1   000020    354
BOTHOK1         3   00022D    923   937
BOTHOK2         3   000371   1208  1222
BRKDATA         1 00000000    147   802  1085
BRKDET          1 0000005F    327   535   572   725   798  1007  1081
BRKFLG1         1 0000006E    338   536   537   799   801
BRKFLG2         1 0000006D    339   573   574  1082  1084
C               1 0000000B      0
CALLINT         3   00050F   1573  1571
CALLSYS         3   0003FE   1361  1359
CHEKBRK1        3   00018F    798   795
CHEKBRK2        3   0002CF   1081  1078
```

SYMBOL LEN VALUE DEFN REFERENCES ASM51 V1.9 07.09 05/09/86

```
CHK_ONE          3   0006EA  2141  2134
CHKBRK           3   000142   725   723
CHKBRK2          3   000280  1007  1005
CHKCHAR1         3   00005D   541   536
CHKCHAR2         3   00008D   578   573
CHKMDM1          3   0000CB   652   608
CHKMDM1A         3   0000D9   658   655
CHKMDM1B         3   0000DE   660   656
CHKMDM1C         3   0000EC   666   664   666
CHKMDM1D         3   0000FC   672   660   665
CHKMDM2          3   0000FF   685   657   659
CHKMDM2A         3   00010D   691   688
CHKMDM2B         3   000112   693   689
CHKMDM2C         3   000120   699   697   699
CHKMDM2D         3   000132   706   693   698
CHKPAR1          3   0001A0   805   798
CHKPAR2          3   0002E0  1088  1081
CHKTC1           3   000545  1619  1613  1616  1617
CHKTC2           3   0005F6  1797  1791  1794  1795
CHKTXTC1         3   000203   876   861
CHKTXTC2         3   000345  1160  1144
CHKXOFF1         3   0001E4   861   851
CHKXOFF2         3   000324  1144  1134
CHKXON1          3   0001D4   851   846
CHKXON2          3   000314  1134  1129
CK6MARK1         3   000583  1685  1678
CK6MARK2         3   000634  1863  1856
CK6NMS1          3   0005B3  1727  1721
CK6NMS2          3   000664  1905  1899
CK6SPC1          3   00059E  1707  1701
CK6SPC2          3   00064F  1885  1879
CK7NMS1          3   0005BB  1733  1727
CK7NMS2          3   00066C  1911  1905
CK8MARK1         3   00058E  1695  1685
CK8MARK2         3   00063F  1873  1863
CK8NMS1          3   0005C3  1742  1733
CK8NMS2          3   000674  1926  1911
CK8SPC1          3   0005A6  1716  1707
CK8SPC2          3   000657  1894  1885
CMDCMPFL         1 00000005   241   671  1154  1358  1566
CMDCNT           1 00000002   195   492   607   618  1994  2040  2041
CMDCUMP          1   000404  1363  1348  1354
CMDDONE0         3   000415  1381  1378
CMDDONE1         3   0004CF  1488  1417  1421  1429  1440  1443  1444  1459  1463  1471  1482  1488  1490
CMDDONE2         3   00042C  1396  1393
CMDEXPTR         1 00000000   193  1995  1998
CMDOK            3   000606  2044  2041
CMDOVFLO         1 00000017   255   617   637  2042
CMDSTPTR         1 00000001   194   631   634   636  2047  2050
CMDSTUPD         2   000698  1993  1362  1384  1574
CMDST0           1   000008   199   490   491   636  1998  2050
CMDST1           1   000009   200
CMDST2           1   00000A   201
```

SYMBOL LEN VALUE DEFN REFERENCES ASM51 V1.9 07.09 05/09/86

```
CMDST3          1   00000B   202
CMDST4          1   00000C   203
CMDST5          1   00000D   204
CMDST6          1   00000E   205
CMDST7          1   00000F   206    159    632
CY              1 000000D7     0
DACKBACK        1 00000094    81   1945
DJMP1           3   0004F2  1561   1557
DJMP2           3   0003D7  1346   1338
DJMP3           3   0003DF  1349   1346
DJMP7           3   0003E7  1352   1349
DMAREQEN        1 00000092    79   1943
DMATCST         1 00000001   143   1569
DMATOADP        2   000678  1941    913   1198   1553   1587   1631   1641   1652   1662   1765   1809   1819   1830
                                   1840
DONE1           3   000447  1417   1415
DONE2           2   00049B  1459   1457
DPH             1 00000083     0    500    505    530    567    628    652    685    833    873    915    981   1116
                                   1157   1200   1266   1412   1454   1601   1779   1946   1949   2014   2025   2027
                                   2044   2131   2132   2152
DPL             1 00000082     0    531    538    568    575    720    814    834    968    982   1002   1097   1117
                                   1253   1267   1413   1431   1433   1455   1473   1475   1602   1780
DPTR            2 00000009     0    501    506    532    539    546    548    569    576    583    585    629    653
                                   686    731    792    819    884    886    969    984    987   1013   1075   1102
                                   1168   1170   1254   1269   1272   1419   1424   1427   1432   1435   1438   1461
                                   1466   1469   1474   1477   1480   1604   1607   1782   1785   1947   1950   2016
                                   2045   2136   2139   2143
DREQ0           1 00000090    77
DREQ1           1 00000091    78
EA              1 000000AF     0    511    613    638   1993   1999
ENDRECV1        1   000180   784    800
ENDRECV2        1   0002C0  1067   1083
ENDSTACK        1 00000010   159   1996   2048
ENDSTAT         1   0006F0  2144   2140   2141
ENDUPDT         2   0006A3  1999   1997
ENDXMIT1        1   00025E   973    888    970
ENDXMIT2        1   0003A2  1258   1172   1255
END1            2   0000C4   637    635
ENXONOF1        1 00000020   272    740
ENXONOF2        1 00000028   280   1022
EN8530RX        1 00000001   158   1437   1479
EN8530TX        1 00000008   157    986   1271
ES              1 000000AC     0
ET0             1 000000A9     0
ET1             1 000000AB     0
EXECCMD         2   0000C6   638    617    623
EXTI0           3 00000003     0
EXTI1           3 00000013     0
EX0             1 000000A8     0    510
EX1             1 000000AA     0   2013   2151
FIRSTBAD1
                2   000239   929    925
FIRSTBAD2
```

SYMBOL LEN VALUE DEFN REFERENCES ASM51 V1.9 07.09 05/09/86

```
                2   00037D  1214   1210
FRMERR1         3   0001A8   808    805
FRMERR2         3   0002E8  1091   1088
FRMESTAT        1 00000004   141    808   1091
F0              1 000000D5     0
HIDMA           1   000031   366    923   1208   1597   1603   1636   1647   1657   1667   1775   1781   1814   1825
                                   1835   1845   1948
HIVALIDA        1 00000057   319    835    839    924    930    942    991
HIVALIDB        1 0000001F   263   1118   1122   1209   1215   1227   1276
HIXBYTEA        1   000032   367    841    923    931
HIXBYTEB        1   000033   368   1124   1208   1216
HNDLCMD         2   0000A9   612    607
HNDLINT0        1 00002003   422
HNDLINT1        1 00002006   423
HNDLOBF         1   0006BE  2040   2026
HNDLTIM0        1 00002009   424
HNDLTIM1        1 0000200C   425
H8530A          1 00000098   125    530    833    873    915    981   1412   1601
H8530B          1 00000098   128    567   1116   1157   1200   1266   1454   1779
I_O_8530A
                3   000525  1601   1598
I_O_8530B
                3   0005D6  1779   1776
IBF             1 000000B3    90   2009   2137
IE              1 000000A8     0
IE0             1 00000089     0
IE1             1 0000008B     0   2012
INL8530A        1 00000000   120   1557
INL8530B        1 00000001   121   1561
INTRSYS         3   0006A6  2009    671    705    783    872    900   1066   1156   1185   1361   1573   2009
INTR0           1 000000B2    89
INT0            1 000000B2     0
INT0DONE        2   0006BB  2027   2043   2049   2051
INT1            1 000000B3     0
INVALID1        3   0001CC   846    835
INVALID2        3   00030C  1129   1118
IN8530A         1   000516  1583   1558   1619
IN8530B         1   0005C7  1761   1562   1797
IP              1 000000B8     0
IPLCOMP         1 00000095    82    522
IT0             1 00000088     0
IT1             1 0000008A     0
J11             3   000539  1614   1611
J12             3   000540  1617   1614
J21             3   0005EA  1792   1789
J22             3   0005F1  1795   1792
LODMA           1   000030   365    856    868    926    943   1139   1151   1211   1228   1554   1606   1646   1656
                                   1666   1784   1824   1834   1844   1951
L8530A          1 00000001   126    531    814    834    982   1413   1433   1602
L8530AD         1 00000003   127    538    720    968   1431
L8530B          1 00000000   129    568   1097   1117   1267   1455   1475   1780
L8530BD         1 00000002   130    575   1002   1253   1473
MARKPAR1        1 00000022   270    963   1677
```

SYMBOL	LEN	VALUE	DEFN	REFERENCES				
MARKPAR2	1	0000002A	278	1248	1855			
MBYTBUF	1	00003D	378	1555	1568			
MBYTCMDS	2	0004E0	1551	1353				
MBYTEFL	1	00000003	243	1567				
MDMCHGFL	1	00000002	244	667	700			
MDMREG1A	1	000040	384	502	654	658	661	668	672
MDMREG1B	1	000041	385	503	655	658			
MDMREG1C	1	000042	386	504	656	662	672	1447	
MDMREG2A	1	000043	387	507	687	691	694	702	706
MDMREG2B	1	000044	388	508	688	691			
MDMREG2C	1	000045	389	509	689	695	706	1493	
MODMMSK1	1	000046	390	663	1636				
MODMMSK2	1	000047	391	696	1814				
MS_DONE1	3	000253	968	963					
MS_DONE2	3	000397	1253	1248					
MSB	1	00000020	239	2015	2145				
MSPAREN1	1	00000023	269	1676					
MSPAREN2	1	0000002B	277	1854					
NO_TC	3	000694	1955	1953					
NOERROR1	1	000148	731	725					
NOERROR2	1	000286	1013	1007					
NOMSPTY1	3	0005AB	1721	1676					
NOMSPTY2	3	00065C	1899	1854					
NOTC1	2	00051E	1597	1591					
NOTC2	2	0005CF	1775	1769					
NOTFULL	3	0000B5	628	618					
NOTT	1	000000C9	0						
NOTXON1	3	000410	1379	1376					
NOTXON2	3	000427	1394	1391					
NOTXTC1	2	000223	911	876					
NOTXTC2	2	000367	1196	1160					
NOT1	3	00044A	1418	1414					
NOT11	3	00049D	1460	1456					
NOT2	3	000453	1422	1418					
NOT21	3	0004A5	1464	1460					
NOT3	3	000463	1430	1422					
NOT31	3	0004B4	1472	1464					
NOT4	3	000479	1441	1430					
NOT41	3	0004CA	1483	1472					
NOT5	3	000480	1444	1441					
NOT51	3	0004D3	1490	1483					
OBF	1	000000B5	92	2026					
OK1	3	00041C	1384	1379	1381	1399			
OK2	2	000433	1399	1394	1396				
ONEBYTE	1	00000001	152	773	1055	2141			
OPCMDDCD	1	0003BA	1333	639					
OV	1	000000D2	0						
OVRSTAT	1	00000001	139	796	1079				
P	1	000000D0	0						
PARESTAT	1	00000002	140	806	1089				
PASSANY1	3	0001F2	869	859					
PASSANY2	3	000332	1152	1142					
PASSERR1	2	0001AB	812	797	804	807			

IBM

Personal Computer Hardware Reference Library

Diskette and Hard Disk Adapter

Contents

Notes:

Description

The IBM Personal Computer AT Fixed Disk and Diskette Drive Adapter connects to the system board using one of the system expansion slots. The adapter controls the 5-1/4 inch diskette drives and fixed disk drives. Connectors on the adapter supply all the signals necessary to operate up to two fixed drives and one diskette drive or one fixed drive and two diskette drives. The adapter will allow concurrent data operations on one diskette and one fixed disk drive.

The adapter operates when connected to a system board expansion slot. This channel is described in the "System Board" section of the IBM Personal Computer AT Technical Reference Manual.

Fixed Disk Function

The fixed disk function features 512-byte sectors; high-speed, PIO data transfers; ECC correction of up to five bits on data fields; multiple sector operations across track and cylinder boundaries; and on-board diagnostic tests. The adapter will support two fixed disks with up to 16 read/write heads and 1024 cylinders.

Task File

A task file, which contains eight registers, controls fixed-disk operations. The following figure shows the addresses and functions of these registers.

I/O Address			
Primary	Secondary	Read	Write
1F0	170	Data register	Data register
1F1	171	Error register	Write precomp
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder low	Cylinder low
1F5	175	Cylinder high	Cylinder high
1F6	176	Drive/head	Drive/head
1F7	177	Status register	Command register

Task File

Task File Registers

Data Register

The data register provides access to the sector buffer for read and write operations in the PIO mode. This register must not be accessed unless a Read or Write command is being executed. The register provides a 16-bit path into the sector buffer for normal Read and Write commands. When a R/W Long is issued, the 4 ECC bytes are transferred by byte with at least 2 microseconds between transfers. 'Data Request' (DRQ) must be active before the transferring of the ECC bytes.

Error Register

The error register is a read-only register that contains specific information related to the previous command. The data is valid only when the error bit in the status register is set, unless the adapter is in diagnostic mode. Diagnostic mode is the state immediately after power is switched on or after a Diagnose command. In these cases, the register must be checked regardless of the status register indicator. The following are bit values for the diagnostic mode.

Diagnostic Mode

01 No errors

02 Controller error

03 Sector buffer error

04 ECC device error

05 Control processor error

The following are bit definitions for the operational mode.

Operational Mode

Bit 0 Data Address Mark (DAM) Not Found—This bit indicates that DAM could not be found within 16 bytes of the ID field.

Bit 1 TR 000 Error—This bit will be set if, during a Restore command, the track 000 line from the fixed disk is not true within 1023 step pulses to the drive.

Bit 2 Aborted Command—A command is aborted based on the drive status (Write Fault, Not Seek Complete, Drive Not Ready, or an invalid command). The status and error registers may be decoded to determine the cause.

Bit 3 Not used.

Bit 4 ID Not Found—The ID field with the specified cylinder, head, and sector number could not be found. If retries are enabled, the controller attempts to read the ID 16 times before indicating the error. If retries are disabled, the track is scanned a maximum of two times before setting this error bit.

Bit 5 Not used

Bit 6 Data ECC Error—This bit indicates that an uncorrectable ECC error occurred in the target's data field during a read command.

Bit 7 Bad Block Detect—This bit indicates that the bad block mark was detected in the target's ID field. No Read or Write commands will be executed in any data fields marked bad.

Write Precompensation Register

The value in this register is the starting cylinder divided by 4. The 'reduced write current' signal to the drive is activated and the adapter's Write Precompensation logic is turned on.

Sector Count Register

The sector count register defines the number of sectors to be transferred during a Verify, Read, Write, or Format command. During a multi-sector operation, the sector count is decremented and the sector number is incremented. When the disk is being formatted, the number of sectors per track must be loaded into the register prior to each Format command. The adapter supports multi-sector transfers across track and cylinder boundaries. The drive characteristics must be set up by the Set Parameters command before initiating a multi-sector transfer. The sector count register must be loaded with the number of sectors to be transferred for any data-related command.

Note: A 0 in the sector count register specifies a 256-sector transfer.

Sector Number Register

The target's logical sector number for Read, Write, and Verify commands is loaded into this register. The starting sector number is loaded into this register for multi-sector operations.

Cylinder Number Registers

The target number for Read, Write, Seek, and Verify commands is loaded into these registers as shown in the following figure. The cylinder-number registers address up to 1024 cylinders.

	Cylinder High	Cylinder Low
Register bits	76543210	76543210
Cylinder bits	———98	76543210

Cylinder Number Registers

Drive/Head Register

Bit 7 Set to 1

Bit 6 Set to 0

Bit 5 Set to 1

Bit 4 Drive Select—This bit selects the drive. A 0 indicates the first fixed disk drive, and a 1 indicates the second.

Bit 3–Bit 0 Head Select Bits—Bits 3 through 0 specify the desired read/write head. Bit 0 is the least-significant (0101 selects head 5). The adapter supports up to 16 read/write heads. For access to heads 8 through 15, bit 3 of the fixed disk register (address hex 3F6) must be set to 1.

Note: This register must be loaded with the maximum number of heads for each drive before a Set Parameters command is issued.

Status Register

The controller sets up the status register with the command status after execution. The program must look at this register to determine the result of any operation. If the busy bit is set, no other bits are valid. A read of the status register clears interrupt request 14. If 'write fault' or 'error' is active, or if 'seek complete' or 'ready' is inactive, a multi-sector operation is aborted.

The following defines the bits of the status register.

Bit 7 Busy—This bit indicates the controller's status. A 1 indicates the controller is executing a command. If this bit is set, no other status register bit is valid, and the other registers reflect the status register's contents; therefore, the busy bit must examined before any fixed disk register is read.

Bit 6 Drive Ready—A 1 on this bit together with a 1 on seek complete bit (bit 4) indicates that the fixed disk drive is ready to read, write, or seek. A 0 indicates that read, write, and seek are inhibited.

Bit 5 Write Fault—A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.

Bit 4 Seek Complete—A 1 on this bit indicates that the read/write heads have completed a seek operation.

Bit 3 Data Request—This bit indicates that the sector buffer requires servicing during a Read or Write command. If either bit 7 (busy) or this bit is active, a command is being executed. Upon receipt of any command, this bit is reset.

Bit 2 Corrected Data—A 1 on this bit indicates that the data read from the disk was successfully corrected by the ECC algorithm. Soft errors will not end multi-sector operations.

Bit 1 Index—This bit is set to 1 each revolution of the disk.

Bit 0 Error—A 1 on this bit indicates that the previous command ended in an error, and that one or more bits are set in the error register. The next command from the controller resets the error bit. This bit, when set, halts multi-sector operations.

Command Register

The command register accepts eight commands to perform fixed disk operations. Commands are executed by loading the task file and writing in the command register while the controller status is not busy. If '-write fault' is active or if '-drive ready' or '-seek complete' are inactive, the controller will not execute any command. Any code not defined in the following causes an Aborted Command error. Interrupt request 14 is reset when any command is written. The following are acceptable commands to the command register.

Command	Bits 7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read Sector	0	0	1	0	0	0	L	T
Write Sector	0	0	1	1	0	0	L	T
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1

Valid Command-Register Commands

The following figure shows the stepping rate as defined by R3 through R0.

R3	R2	R1	R0	Stepping Rate
0	0	0	0	35 us
0	0	0	1	0.5 ms
0	0	1	0	1.0 ms
0	0	1	1	1.5 ms
0	1	0	0	2.0 ms
0	1	0	1	2.5 ms
0	1	1	0	3.0 ms
0	1	1	1	3.5 ms
1	0	0	0	4.0 ms
1	0	0	1	4.5 ms
1	0	1	0	5.0 ms
1	0	1	1	5.5 ms
1	1	0	0	6.0 ms
1	1	0	1	6.5 ms
1	1	1	0	7.0 ms
1	1	1	1	7.5 ms

Stepping Rate

Note: After a Diagnose or Reset Command, the stepping rate is set to 7.5 milliseconds.

The following figure shows the bit definitions for bits L and T.

Bit	Definition	0	1
L	Data Mode	Data Only	Data plus 4 byte ECC
T	Retry Mode	Retries Enabled	Retries Disabled

L and T Bit Definitions

Note: The system verifies the operation of ECC by reading and writing with the ECC bytes. When retries are disabled, ECC and ID field retries are limited to less than two complete revolutions.

Following are descriptions of the valid command-register commands.

Restore: The controller issues step pulses to the drive at 3 milliseconds per step until the track 000 indicator from the drive is active. If track 000 is not active within 1023 steps, the error bit in the status register is set, and a track 000 error is placed in the error register. The implied seek step rate is set by this command.

Seek: The Seek command moves the R/W heads to the cylinder specified in the task files. The adapter supports overlapped seeking on two drives or setup of the buffered seek stepping rate for the implied seek during a Read/Write command. An interrupt is generated at the completion of the command.

Read Sector: A number of sectors (1–256) may be read from the fixed disk with or without the ECC field appended in the Programmed I/O (PIO) mode. If the heads are not over the target track, the controller issues step pulses to the drive and checks for the proper ID field before reading any data. The stepping rate used during the implied seek is the value specified during the previous Seek or Restore command. Data errors, up to 5 bits in length, are automatically corrected on Read Short commands. If an uncorrectable error occurs, the data transfer still takes place; however, a multi-sector read ends after the

system reads the sector in error. Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command, after the lost sector is read by the system.

Write Sector: A number of sectors (1–256) may be written to the fixed disk with or without the ECC field appended in the PIO mode. The Write Sector command also supports implied seeks. Interrupts for the Write command occur before each sector is transferred to the buffer (except the first) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and 'data request' is active.

Format Track: The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table is composed of two bytes per sector as follows: 00, Physical Sector 1, 00, Physical Sector 2, ... 00,Physical Sector 17. The table for 2-to-1 interleave is: 00, 01, 00, 0A, 00, 02, 00, 0B, 00, 03, 00, 0C, 00, 04, 00, 0D, 00, 05, 00, 0E, 00, 06, 00, 0F, 00, 07, 00, 10, 00, 08, 00, 11, 00, 09. The data transfer must be 512 bytes even though the table may be only 34 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. An interrupt is generated at the completion of the command; the Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80. When switching between drives, a restore command must be executed prior to attempting a format.

Read Verify: This command is similar to to a Read command except that no data is sent to the host. This allows the system to verify the integrity of the fixed disk drive. A single interrupt is generated upon completion of the command or in the event of an error.

Diagnose: This command causes the adapter to execute its self-test code and return the results to the error register. An interrupt is generated at the completion of this command.

Set Parameters: This command sets up the drive parameters (maximum number of heads and sectors per track). The drive/head register specifies the drive affected. The sector count

and drive/head registers must be set up before this command is issued. The adapter uses the values specified for track and cylinder crossing during multi-sector operations. An interrupt is generated at the completion of this command. This command must be issued before any multi-sector operations are attempted. The adapter supports two fixed disk drives with different characteristics, as defined by this command.

Miscellaneous Information

The following is miscellaneous information about the fixed disk drive function.

- The adapter performs normal read/write operations on a data field only after a successful match of that sector's ID with the targeted ID.
- ID fields are checked for errors when read from the disk.
- The adapter supports only ECC on data fields and only CRC on ID fields. The CRC polynomial is X16 + X12 + X5 + 1; the ECC polynomial is X32 + X28 + X26 + X19 + X17 + X10 + X6 + X2 + 1. All shift registers are preset to hex F before calculating the checksums, which begin with the respective address marks.

Diskette Function

The 5-1/4 inch diskette drive function is an integral part of the IBM Personal Computer AT Fixed Disk and Diskette Drive Adapter. One or two diskette drives are attached to the adapter through an internal, daisy-chained, flat cable. The attachment will support 160K.-, 320K.-, and 1.2M.-byte diskette drives.

The adapter is designed for a double-density, MFM-coded, diskette drive and uses write precompensation with an analog circuit for clock and data recovery. The diskette-drive parameters are programmable, and the diskette drive's write-protect feature is supported. The adapter is buffered on the I/O bus and uses the

system board's direct memory access (DMA) for record data transfers. An interrupt level also is used to indicate when an operation is complete and that a status condition requires microprocessor attention.

Digital Output Register (Hex 3F2)

The digital output register (DOR) is an output-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions follow.

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Drive B Motor Enable

Bit 4 Drive A Motor Enable

Bit 3 Enable Diskette Interrupts and DMA

Bit 2 Diskette Function Reset

Bit 1 Reserved

Bit 0 Drive Select—A 0 on this bit indicates that drive A is selected.

Note: A channel reset clears all bits.

Digital Input Register

The digital input register is an 8-bit, read- only register used for diagnostic purposes. The following are bit definitions for this register.

Bit 7 Diskette Change

Bit 6 Write Gate

Bit 5 Head Select 3/Reduced Write Current

Bit 4 Head Select 2

Bit 3 Head Select 1

Bit 2 Head Select 0

Bit 1 Drive Select 1

Bit 0 Drive Select 0

Note: Bits 0 through 6 apply to the currently selected fixed disk drive.

Data Rates

The diskette function will support three data rates: 250,000, 300,000 and 500,000 bits per second. The 300,000-and 500,000-bps incoming data pulse widths will be those associated with a 500,000-bps data signal.

Diskette Controller

The diskette controller has two registers to which the main system processor has access: a status register and a data register. The 8-bit status register has the status information about the diskette and may be accessed at any time. The 8-bit data register (hex 3F5), which actually consists of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, and parameters, and provides diskette-drive status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command. The main status register may only be read and is used to facilitate the transfer of data between the processor and diskette controller.

The bits in the main status register (hex 34F) are defined as follows:

Bit 7	Request for Master (RQM)— The data register is ready to send or receive data to or from the processor.
Bit 6	Data Input/Output (DIO)—The direction of data transfer between the diskette controller and the processor. If this bit is a 1, transfer is from the diskette controller's data register to the processor; if it is a 0, the opposite is true.
Bit 5	Non-DMA Mode (NDM)—The diskette controller is in the non-DMA mode.
Bit 4	Diskette Controller Busy (CB)— A Read or Write command is being executed.
Bit 3	Reserved
Bit 2	Reserved
Bit 1	Diskette Drive B Busy (DBB)— Diskette drive B is in the seek mode.
Bit 0	Diskette Drive A Busy (DAB)— Diskette drive A is in the seek mode.

The diskette controller can perform 11 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the diskette controller and the processor, each command can be considered to consist of three phases:

Command Phase: The processor issues a sequence of Write commands to the diskette controller that direct the controller to perform a specific operation.

Execution Phase: The diskette controller performs the specified operation

Result Phase: After completion of the operation, status and other housekeeping information is made available to the processor through a sequence of Read commands to the processor.

Diskette Controller Commands

The following is a list of commands that may be issued to the diskette controller.

- Read Data
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek
- Invalid

Symbol Descriptions

The following are descriptions of the symbols used in the "Command Definitions" later in this section.

A0 Address Line 0—A 0 selects the main status register, and a 1 selects the data register.

C Cylinder Number—Contains the current or selected cylinder number in binary notation.

D Data—Contains the data pattern to be written to a sector.

D7-D0 Data Bus—An 8-bit data bus in which D7 is the most-significant bit and D0 is the least- significant.

DTL Data Length—When N is 00, DTL is the data length to be read from or written to a sector.

EOT End of Track—The final sector number on a cylinder.

GPL Gap Length—The length of gap 3 (spacing between sectors excluding the VCO synchronous field).

H Head Address—The head number, either 0 or 1, as specified in the ID field.

HD Head—The selected head number, 0 or 1. (H = HD in all command words.)

HLT Head Load Time—The head load time in the selected drive (2 to 256 milliseconds in 2- millisecond increments for the 1.2M-byte drive and 4 to 512 milliseconds in 4 millisecond increments for the 320K-byte drive).

HUT Head Unload Time—The head unload time after a read or write operation (0 to 240 milliseconds in 16-millisecond increments for the 1.2M-byte drive and 0 to 480 milliseconds in 32- millisecond increments for the 320K-byte drive.

MF FM or MFM Mode—A 0 selects FM mode and a 1 selects MFM (MFM is selected only if it is implemented.)

MT Multitrack—A 1 selects multitrack operation. (Both HD0 and HD1 will be read or written.)

N Number—The number of data bytes written in a sector.

NCN New Cylinder—The new cylinder number for a seek operation

ND Non-Data Mode— This indicates an operation in the non-data mode.

PCN Present Cylinder Number—The cylinder number at the completion of a Sense interrupt status command (present position of the head).

R Record—The sector number to be read or written.

R/W Read/Write—This stands for either a 'read' or 'write' signal.

SC Sector—The number of sectors per cylinder.

SK Skip—This stands for skip deleted-data address mark.

SRT This 4 bit byte indicates the stepping rate for the diskette drive as follows:

1.2M-Byte Diskette Drive
1111 1 millisecond
1110 2 milliseconds
1101 3 milliseconds

320K-Byte Diskette Drive
1111 2 milliseconds
1110 4 milliseconds
1101 6 milliseconds

ST 0—ST 1 Status 0—Status 3—One of the four registers that stores status information after a command is executed.

STP Scan Test—If STP is 1, the data in contiguous sectors is compared with the data sent by the processor during a scan operation. If STP is 2, then alternate sections are read and compared.

US0–US1 Unit Select—The selected driver number encoded the same as bits 0 and 1 of the digital output register (DOR).

Controller Commands

The following are commands that may be issued to the controller.

Note: An X is used to indicate a don't-care condition.

Read Data

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	0	0	1	1	0
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
DTL							

Result Phase: The following bytes are issued by the controller in the result phase:

ST0

ST1

ST2

C

H

R

N

Format a Track

Command Phase: The following bytes are issued by the processor in the command phase:

0	MF	0	0	1	1	0	0
X	X	X	X	X	HD	US1	US0

N

SC

GPL

D

Result Phase: The following bytes are issued by the controller in the result phase:

ST0

ST1

ST2

C

H

R

N

Scan Equal

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	0	0	0	1
X	X	X	X	X	HD	US1	US0

C

H

R

N

EOT

GPL

STP

Result Phase: The following bytes are issued by the controller in the result phase:

ST0

ST1

ST2

C

H

R

N

Scan Low or Equal

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	1	0	0	1
X	X	X	X	X	HD	US1	US0

C

H

R

N

EOT

GPL

STP

Result Phase: The following bytes are issued by the controller in the result phase:

ST0

ST1

ST2

C

H

R

N

Scan High or Equal

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	1	1	0	1
X	X	X	X	X	HD	US1	US0

C

H

R

N

EOT

GPL

STP

Result Phase: The following bytes are issued by the controller in the result phase:

ST0

ST1

ST2

C

H

R

N

Recalibrate

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	0	1	1	1
X	X	X	X	X	0	US1	US0

Result Phase: This command has no result phase.

Sense Interrupt Status

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	1	0	0	0

Result Phase: The following bytes are issued by the controller in the result phase:

```
ST0

PCN
```

Specify

Command Phase: The following bytes are issued by the processor in the command phase:

```
 0  0  0  0  0  0  1  1

(  SRT     )(   HUT    )

(      HLT          ) ND
```

Result Phase: This command has no result phase.

Sense Driver Status

Command Phase: The following bytes are issued by the processor in the command phase:

```
0  0  0  0  0  0    1    0

X  X  X  X  X  HD  US1  US0
```

Result Phase: The following bytes are issued by the controller in the result phase:

```
ST3
```

Seek

Command Phase: The following bytes are issued by the processor in the command phase:

```
 0  0  0  0  1  1    1    1

 X  X  X  X  X  HD  US1  US0

NCN
```

Result Phase: This command has no result phase.

Invalid

Command Phase: The following bytes are issued by the processor in the command phase:

```
Invalid Codes

 X  X  X  X  X  HD  US1  US0
```

Result Phase: The following bytes are issued by the controller in the result phase:

```
ST0
```

Command Status Registers

The following is information about the command status registers ST0 through ST3.

Command Status Register 0 (ST0)

The following are bit definitions for command status register 0.

Bit 7–Bit 6 Interrupt Code (IC)

00 Normal Termination of Command (NT)—The command was completed and properly executed.

01 Abrupt Termination of Command (AT)—The execution of the command was started but not successfully completed.

10 Invalid Command Issue (IC)—The issued command was never started.

11 Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.

Bit 5 Seek End (SE)—Set to 1 when the controller completes the Seek command.

Bit 4 Equipment Check (EC)—Set if a 'fault' signal is received from the diskette drive, or if the 'track–0' signal fails to occur after 77 step pulses (Recalibrate Command).

Bit 3 Not Ready (NR)—This flag is set when the diskette drive is in the not-ready state and a Read or Write command is issued. It is also set if a Read or Write command is issued to side 1 of a single-sided diskette drive.

Bit 2 Head Address (HD)—Indicates the state of the head at interrupt.

Bit 1–Bit 0 Unit select 1 and 2 (US 1 and 2)—Indicate a drive's unit number at interrupt.

Command Status Register 1 (ST1)

The following are bit definitions for command status register 1.

Bit 7 End of Cylinder (EC)—Set when the controller tries to gain access to a sector beyond the final sector of a cylinder.

Bit 6 Not Used—Always 0.

Bit 5 Data Error (DE)—Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 Overrun (OR)—Set if the controller is not serviced by the main system within a certain time limit during data transfers.

Bit 3 Not Used—This bit is always set to 0.

Bit 2 No Data (ND)—Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan Command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or if the starting sector cannot be found during the execution of a Read Cylinder commnd.

Bit 1 Not Writable (NW)—Set if the controller detects a 'write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.

Bit 0 Missing Address Mark (MA)—Set if the controller cannot detect the ID address mark. At the same time, the MD of status register 2 is set.

Command Status Register 2 (ST2)

Bit 7 Not Used—Always 0.

Bit 6 Control Mark (CM)—This flag is set if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.

Bit 5 Data Error in Data Field (DD)—Set if the controller detects an error in the data.

Bit 4 Wrong Cylinder (WC)—This flag is related to ND (no data) and when the contents of C on the medium are different from that stored in the ID register, this flag is set.

Bit 3 Scan Equal Hit (SH)—Set if the contiguous sector data equals the processor data during the execution of a Scan command.

Bit 2 Scan Not Satisfied (SN)—Set if the controller cannot find a sector on the cylinder that meets the condition during a Scan command.

Bit 1 Bad Cylinder (BC)—Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set.

Bit 0 Missing Address Mark in Data Field (MD)— Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

Command Status Register 3 (ST3)

The following are bit definitions for command status register 3.

Bit 7 Fault (FT)—Status of the 'fault' signal from the diskette drive.

Bit 6 Write Protect (WP)—Status of the 'write-protect' signal from the diskette drive.

Bit 5 Ready (RY)—Status of the 'ready' signal from the diskette drive.

Bit 4 Track 0 (T0)—Status of the 'track 0' signal from the diskette drive.

Bit 3 Two Side (TS)—Status of the 'two side' signal from the diskette drive.

Bit 2 Head Address (HD)—Status of the 'side-select' signal from the diskette drive.

Bit 1 Unit Select 1 (US 1)—Status of the 'unit-select-1' signal from the diskette drive.

Bit 0 Unit Select 0 (US 0)—Status of the 'unit select 0' signal from the diskette drive.

Interfaces

The system interface is through the I/O channel. The address, DMA, and interrupt assignments are shown in the following figures.

I/O Address			
Primary	Secondary	Read	Write
3F2	372		Digital output register
3F4	374	Main status register	Main status register
3F5	375	Diskette data register	Diskette data register
3F6	376		Fixed disk register
3F7	377	Digital input register	Diskette control register

Diskette Function

Note: DMA request is level 2 and interrupt request is level 6.

I/O Address			
Primary	Secondary	Read	Write
1F0	170	Data register	Data register
1F1	171	Error register	Write precomp
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder low	Cylinder low
1F5	175	Cylinder high	Cylinder high
1F6	176	Drive/head register	Drive/head register
1F7	177	Status register	Command register

Fixed Disk Function

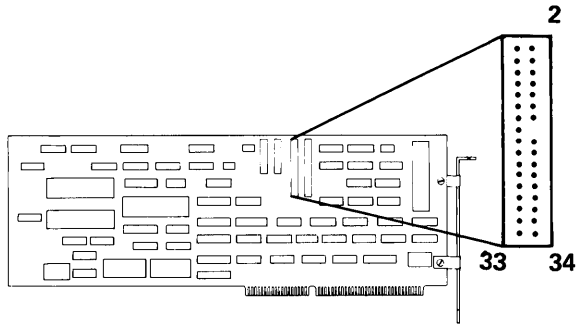
Note: Interrupt request is level 14.

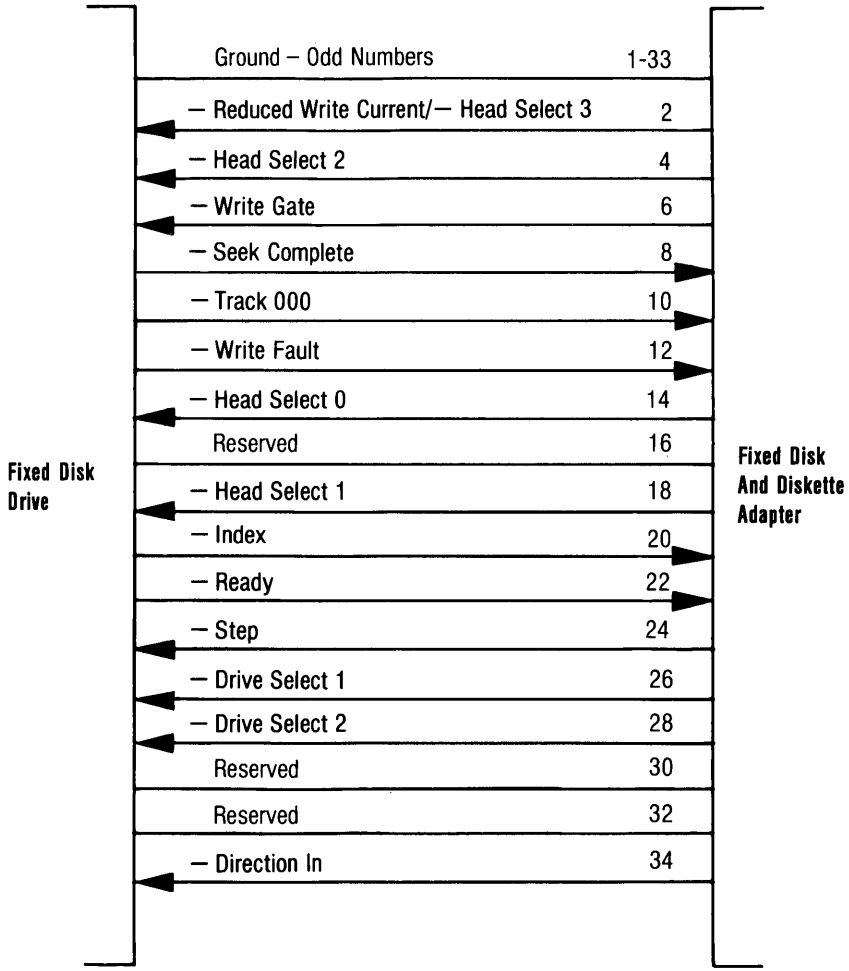
The following operations are supported by this adapter:

- 16 bit programmed I/O (PIO), data transfers to the fixed disk. All other transfers must be 8 bits wide.
- The I/O addresses, recognized by the adapter for either the fixed disk or the diskette function, are independently selected by jumpers.

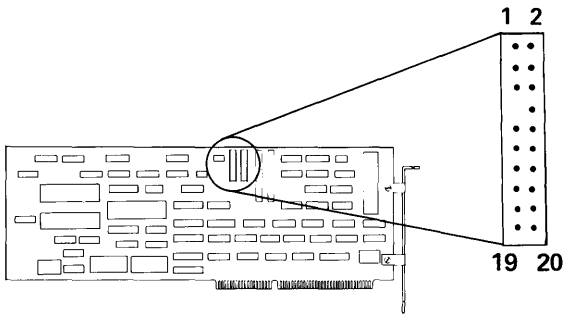
Interface Lines

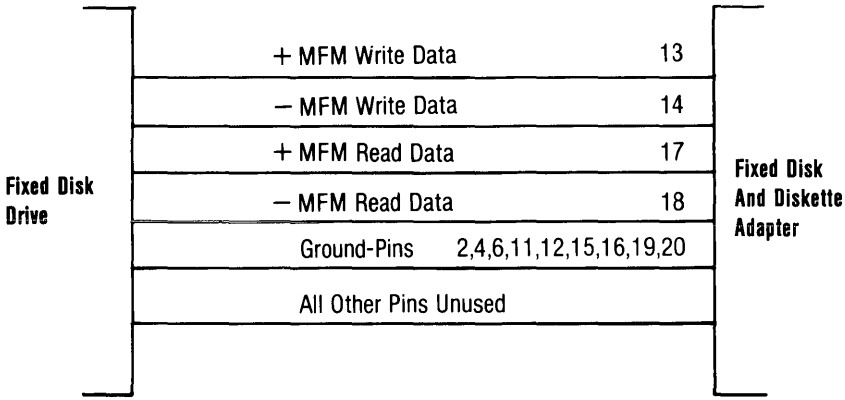
The interface to the fixed disk drive consists of two cables: 'control' and 'data'. The following figures show signals and pin assignments for these cables.





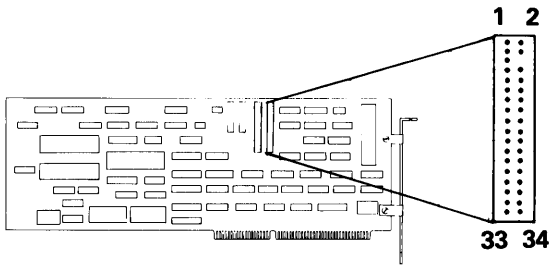
Note: Connection is through a 2-by-17 Berg connector. Pin 15 is reserved to polarize the connector.

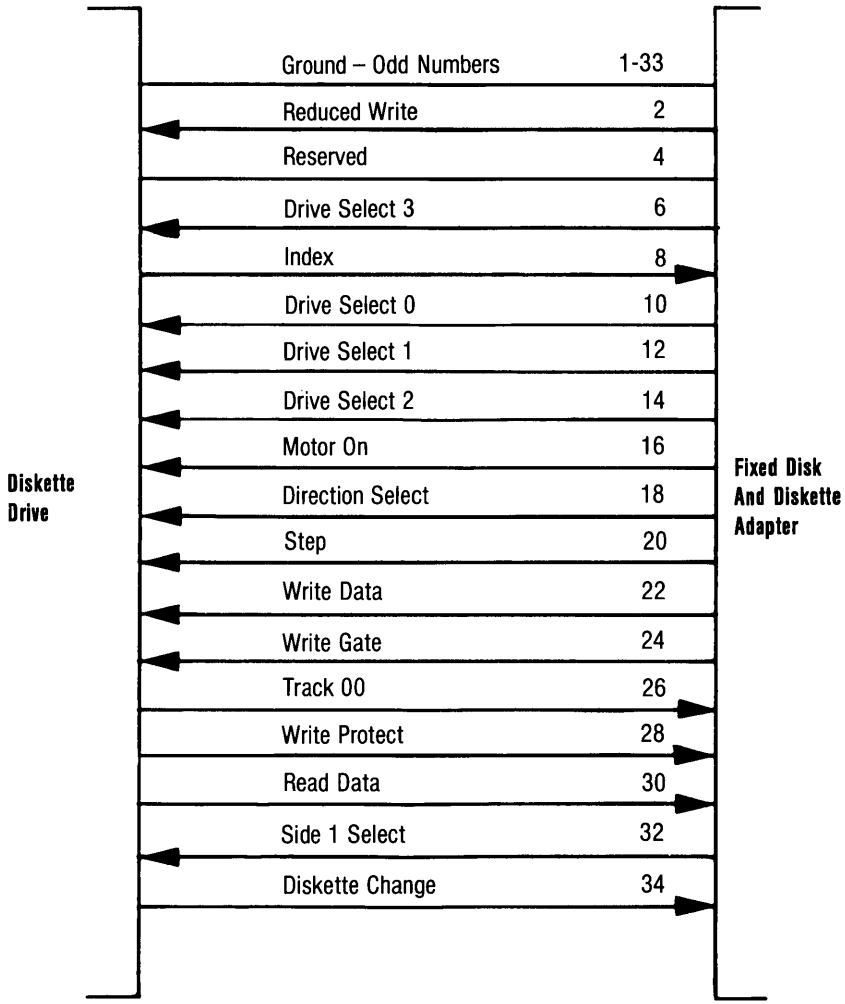




Note: Connection is through a 2-by-10 Berg connector. Pin 8 is reserved to polarize the connector.

The interface to the diskette drives is a single cable that carries both data and control signals. The signals and pin assignments as follows.

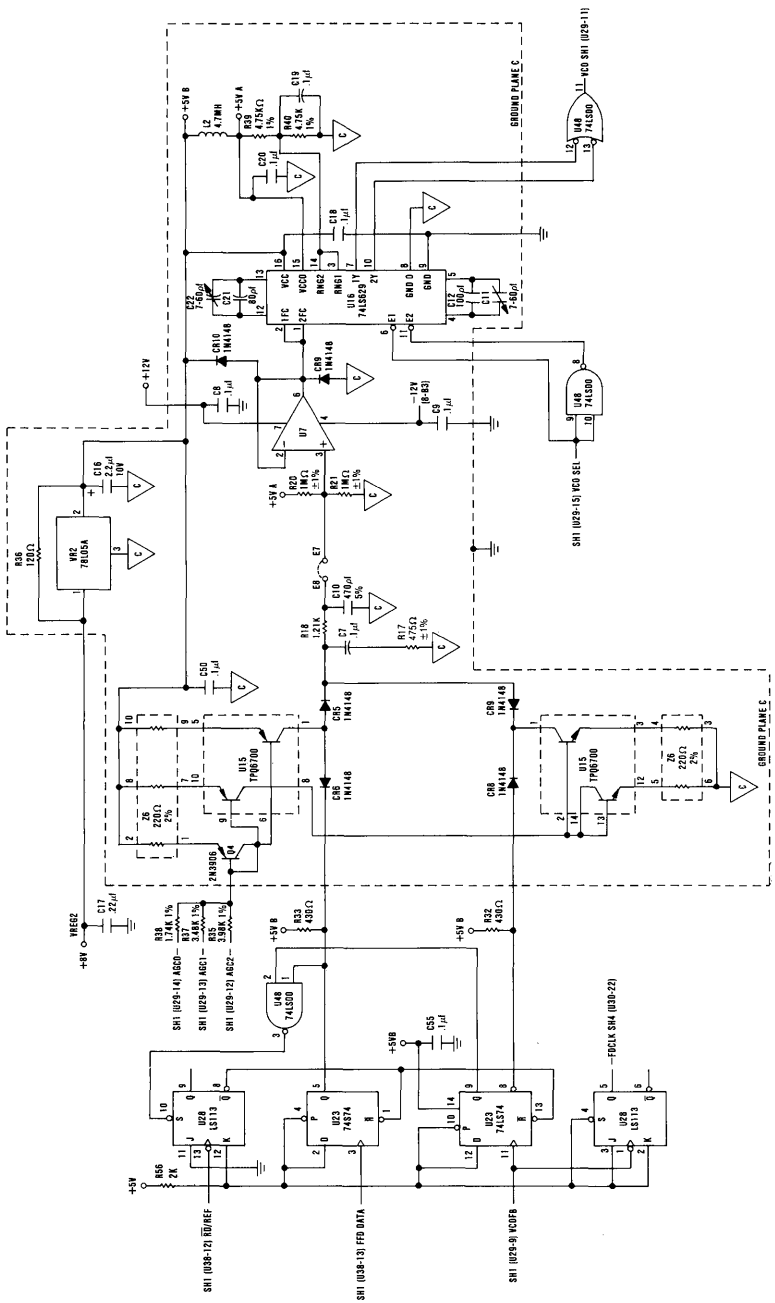




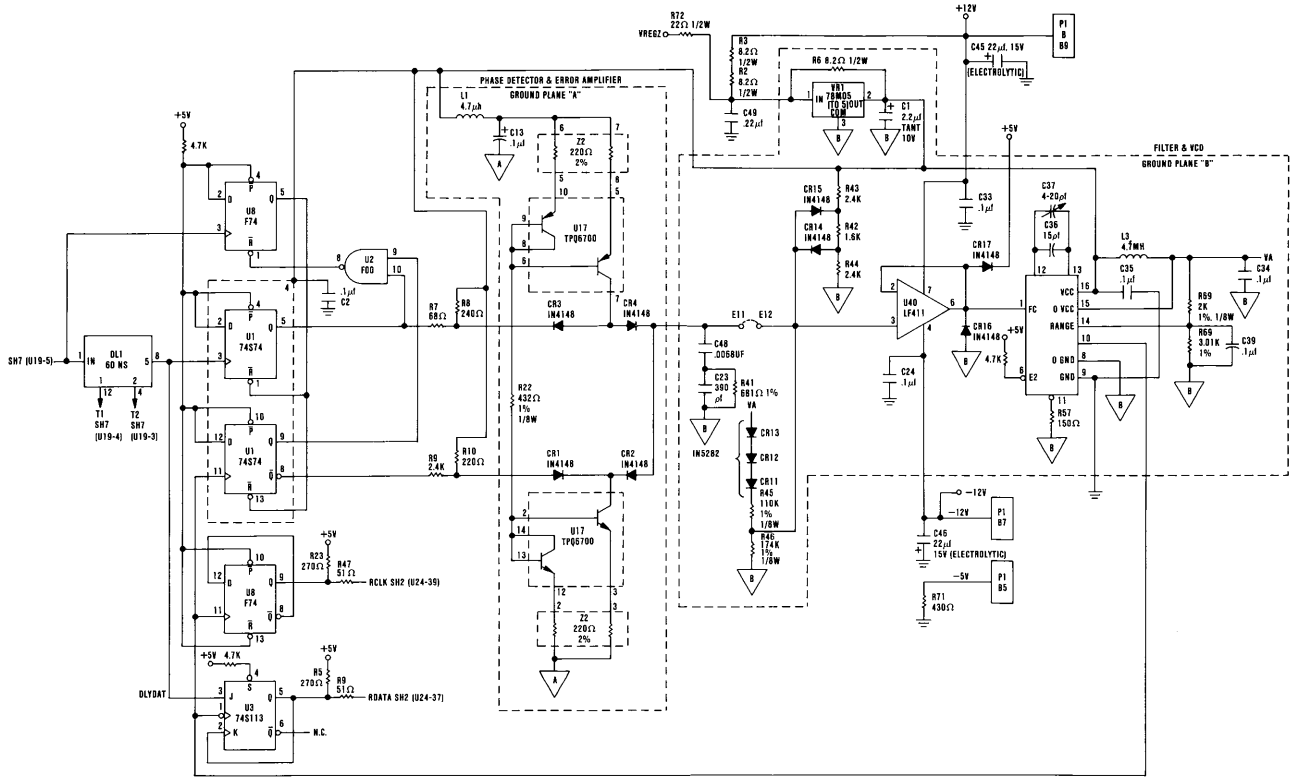
Note: Connection is through a 2-by-17 Berg connector. Pin 5 is reserved to polarize the connector.

Notes:

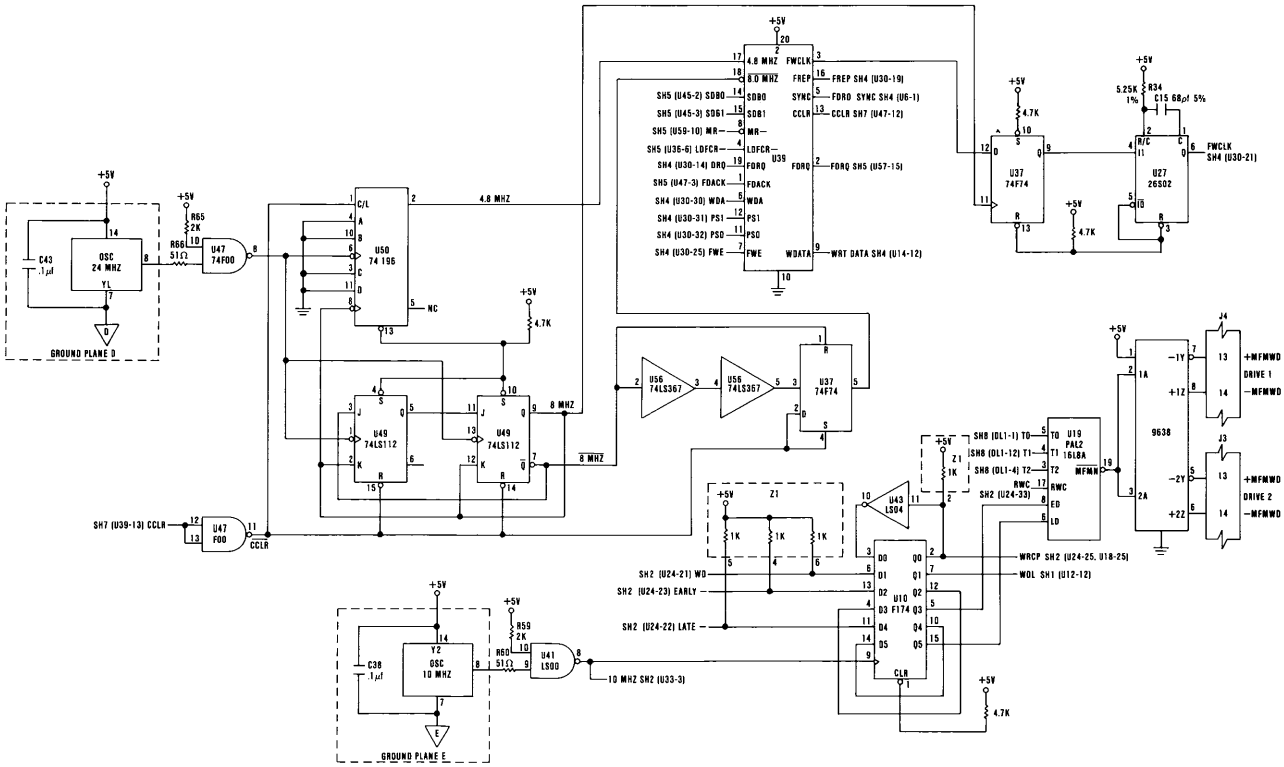
Logic Diagrams



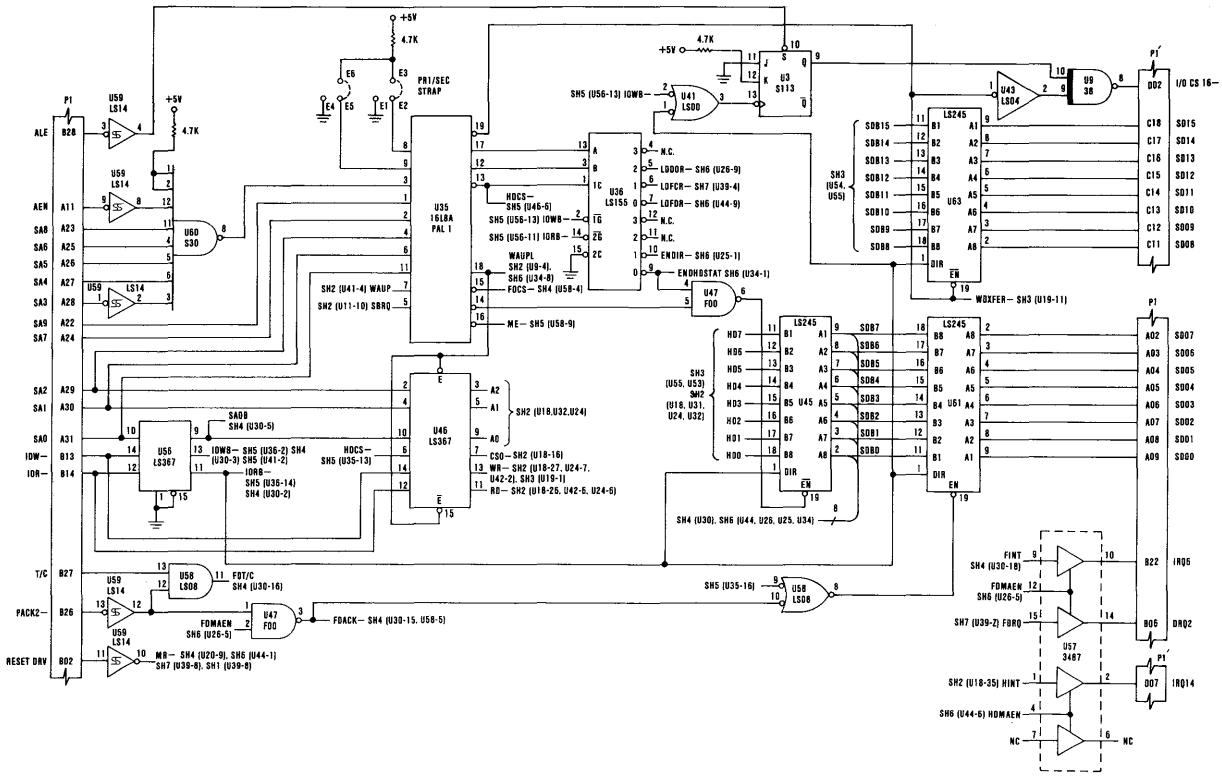
Fixed Disk and Diskette Adapter (Sheet 1 of 8)



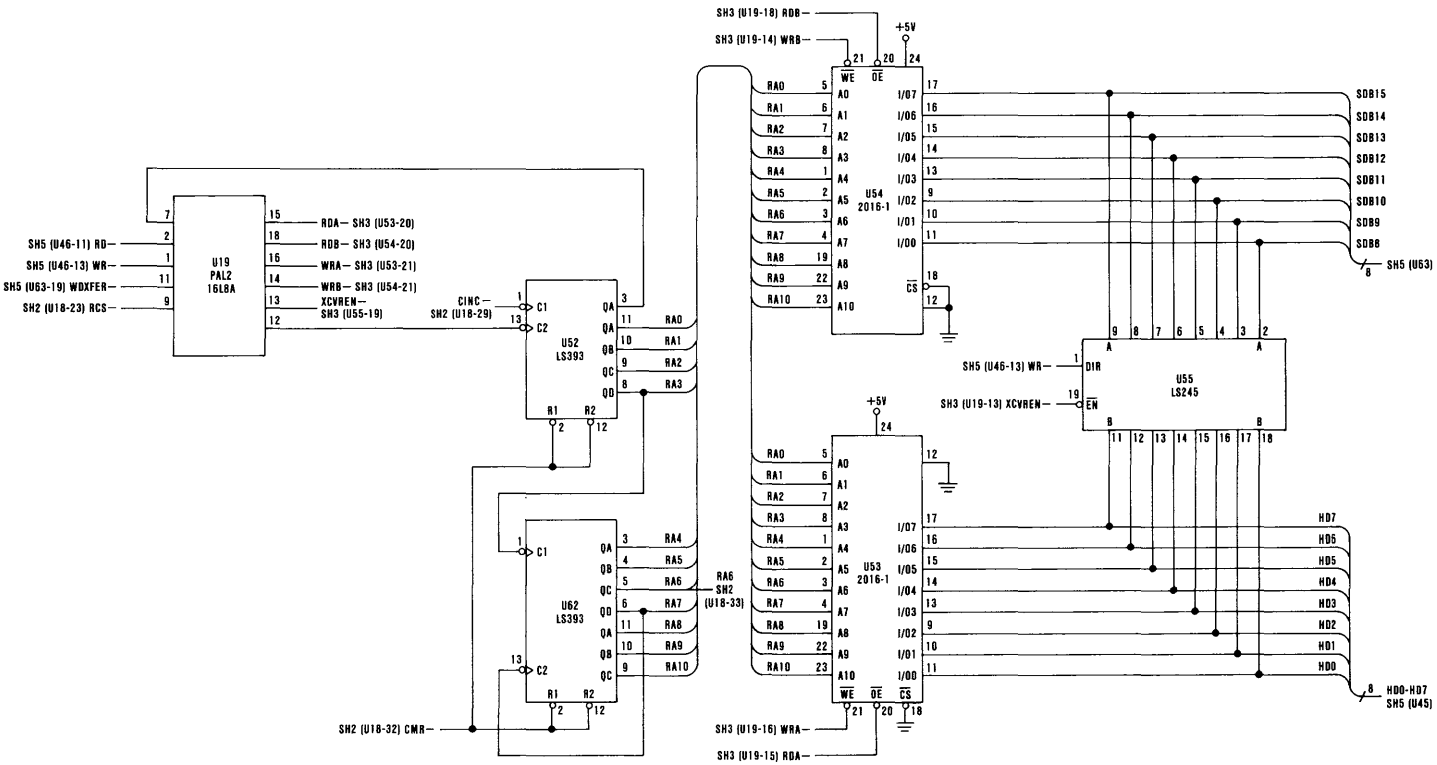
Fixed Disk and Diskette Adapter (Sheet 2 of 8)



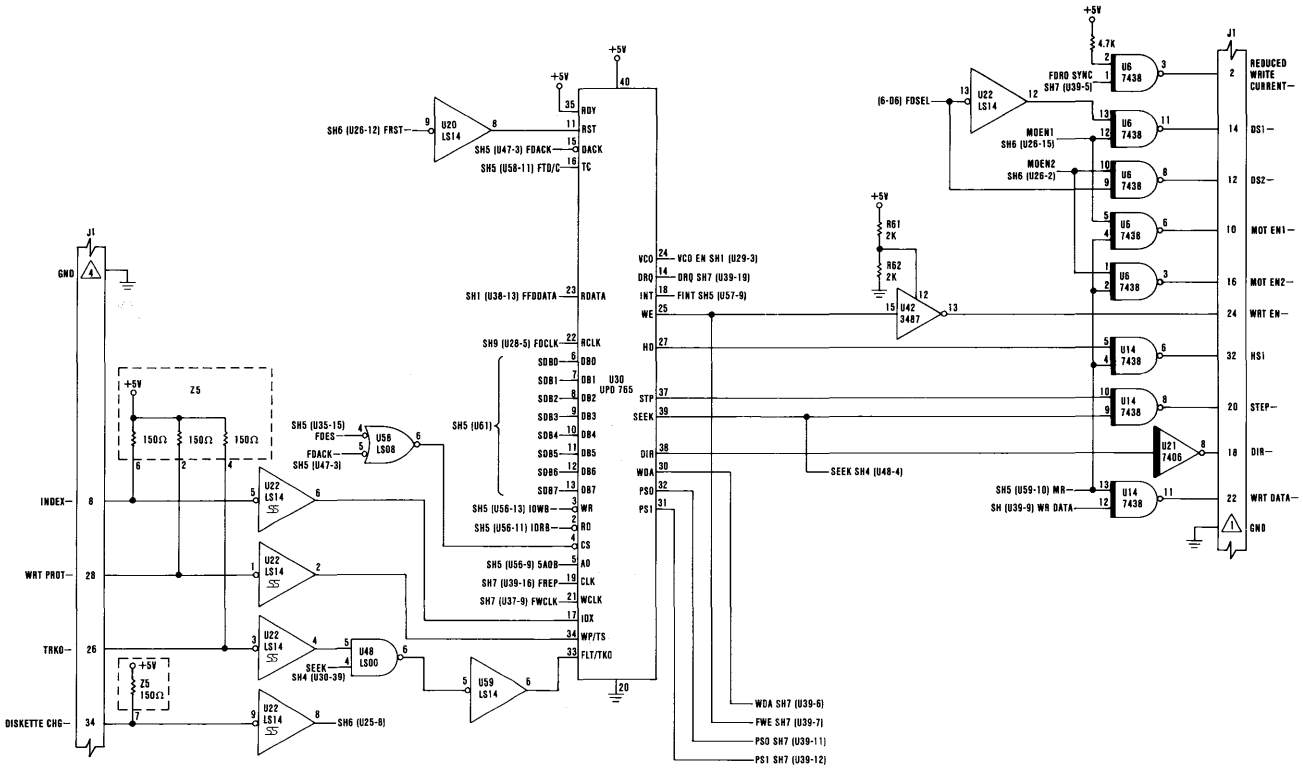
Fixed Disk and Diskette Adapter (Sheet 3 of 8)



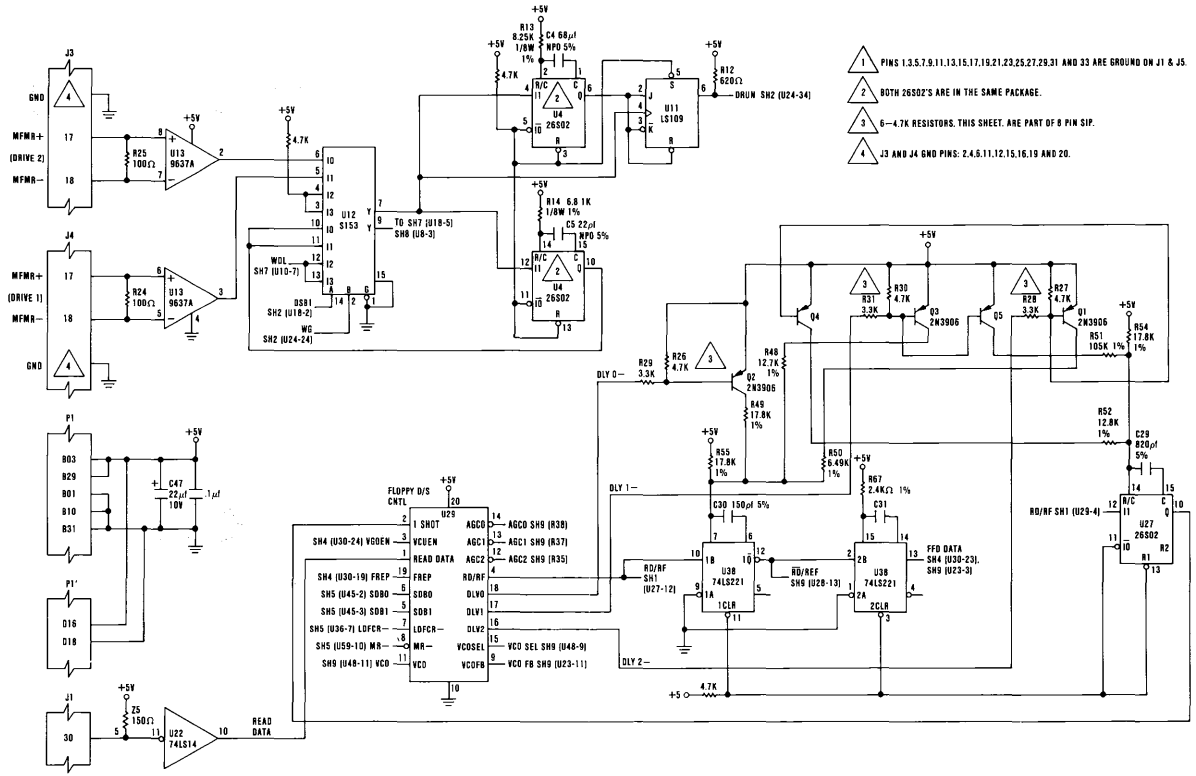
Fixed Disk and Diskette Adapter (Sheet 4 of 8)



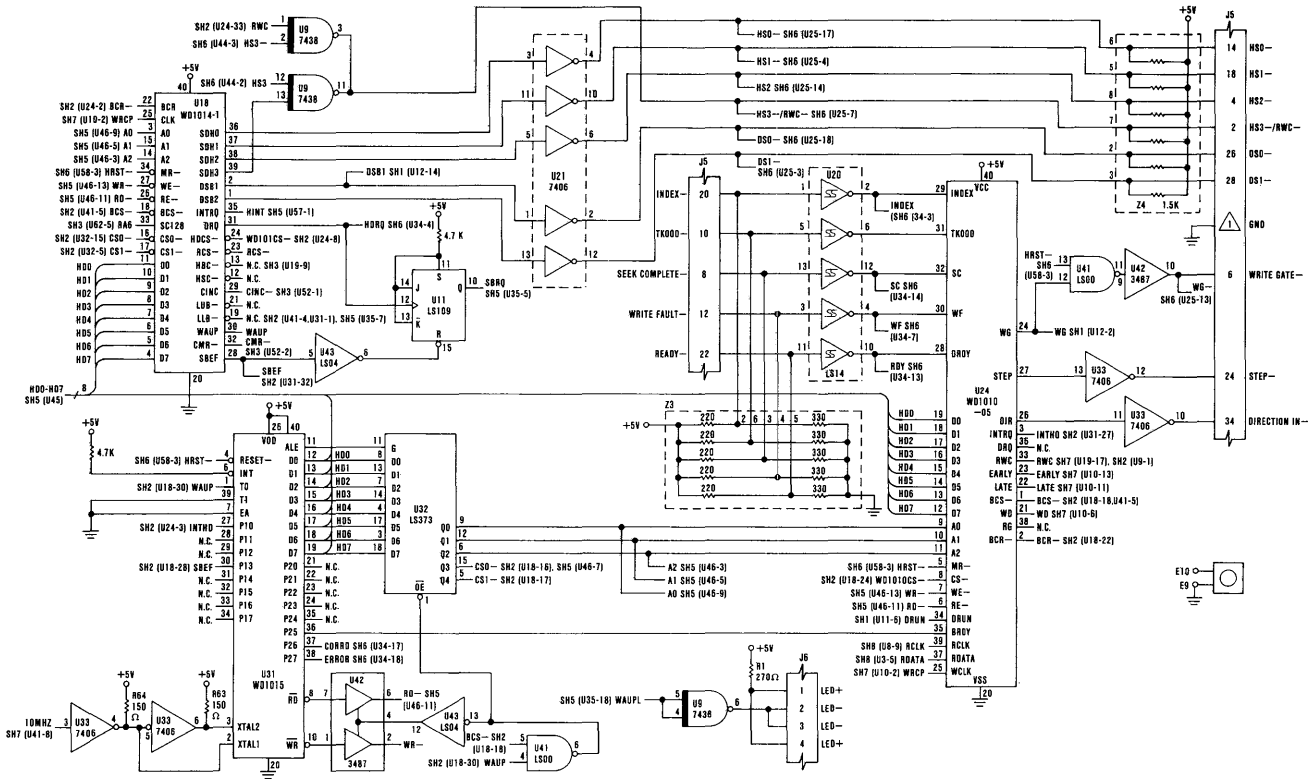
Fixed Disk and Diskette Adapter (Sheet 5 of 8)



Fixed Disk and Diskette Adapter (Sheet 6 of 8)



Fixed Disk and Diskette Adapter (Sheet 7 of 8)



Fixed Disk and Diskette Adapter (Sheet 8 of 8)

IBM

Personal Computer Hardware Reference Library

ESDI Magnetic Media Adapter

Contents

Description

The ESDI Magnetic Media Adapter connects to the system board using one of the I/O slots. The adapter controls the 5-1/4 inch diskette drives and fixed- disk drives. Connectors on the adapter supply all the signals necessary to operate up to two fixed drives and two diskette drives. The adapter allows concurrent data operations on one diskette and one fixed-disk drive.

The adapter operates when connected to a channel I/O slot. This channel is described in the "I/O Channel" section of the RT PC Technical Reference Manual.

Fixed Disk Function

The fixed disk function features 512-byte sectors; high-speed, PIO data transfers; ECC correction of up to 12 bits on data fields; multiple sector operations across track and cylinder boundaries; and on-board diagnostic tests. The adapter supports two fixed disks with up to 16 read/write heads and 2048 cylinders.

Task File

A task file, which contains eight registers, controls fixed-disk operations. The following figure shows the addresses and functions of these registers:

I/O Address			
Primary	**Secondary**	**Read**	**Write**
1F0	170	Data register	Data register
1F1	171	Error register	Not used
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder low	Cylinder low
1F5	175	Cylinder high	Cylinder high
1F6	176	Drive/head register	Drive/head register
1F7	177	Status register	Command register

Figure 1. Task File

Task File Registers

Data Register

The data register provides access to the sector buffer for read/write operations in the PIO mode. This register must not be accessed unless a Read/Write command is being executed. The register provides a 16-bit path into the sector buffer for normal Read/Write commands. When a R/W Long is issued, the 7 ECC bytes are transferred by byte with at least 2 microseconds between transfers. Data Request (DRQ) must be active before the transferring of the ECC bytes.

Error Register

The error register is a read-only register that contains specific information related to the previous command. The data is valid only when the error bit in the status register is set, unless the adapter is in diagnostic mode. Diagnostic mode is the state immediately after power is switched on or after a **Diagnose** command. In these cases, the register must be checked regardless of the status register indicator. The following are bit values for the diagnostic mode:

Diagnostic Mode

01 No errors

02 Adapter device error

03 Disk error

04 Sector buffer error

05 ECC device error

06 Logic support device error

07 Control processor error.

The following are bit definitions for the operational mode:

Operational Mode

Bit 0 Data Address Mark (DAM) Not Found—This bit indicates that DAM could not be found within 16 bytes of the ID field.

Bit 1 TR 000 Error—This bit will be set if, during a Restore command, the track 000 line from the fixed disk is not true within 1023 step pulses to the drive.

Bit 2 Aborted Command—A command is aborted based on the drive status (Write Fault, Not Seek Complete, Drive Not Ready, or an invalid command). The status and error registers may be decoded to determine the cause.

Bit 3 Not used.

Bit 4 ID Not Found—The ID field with the specified cylinder, head, and sector number could not be found. If retries are enabled, the controller attempts to read the ID 16 times before indicating the error. If retries are disabled, the track is scanned a maximum of two times before setting this error bit.

Bit 5 Not used.

Bit 6 Data ECC Error—This bit indicates that an uncorrectable ECC error occurred in the target's data field during a read command.

Bit 7 Bad Block Detect—This bit indicates that the bad block mark was detected in the target's ID field. No Read or Write commands will be executed in any data fields marked bad.

Sector Count Register

The sector count register defines the number of sectors transferred during a Verify, Read, Write, or Format command. During a multisector operation, the sector count is decremented and the sector number is incremented. When the disk is being formatted, the number of sectors per track must be loaded into the register prior to each Format command. The adapter supports multisector transfers across track and cylinder boundaries. The drive characteristics must be set up by the Set Parameters command before initiating a multisector transfer. The sector count register must be loaded with the number of sectors to be transferred for any data-related command.

Note: A 0 in the sector count register specifies a 256-sector transfer.

Sector Number Register

The target's logical sector number for Read, Write, and Verify commands is loaded into this register. The starting sector number is loaded into this register for multisector operations.

Cylinder Number Registers

The target number for Read, Write, Seek, and Verify commands is loaded into these registers as shown in the following figure. The cylinder-number registers address up to 2048 cylinders.

	Cylinder High	Cylinder Low
Register bits Cylinder bits	76543210 ------A98	76543210 76543210

Figure 2. Cylinder Number Registers

Drive/Head Register

Bit 7 Set to 1

Bit 6 Set to 0

Bit 5 Set to 1

Bit 4 Drive Select—This bit selects the drive. An 0 indicates the first fixed disk drive, and a 1 indicates the second.

Bit 3–Bit 0 Head Select Bits—Bits 3 through 0 specify the desired read/write head. Bit 0 is the least significant (0101 selects head 5). The adapter supports up to 16 read/write heads.

Note: This register must be loaded with the maximum number of heads for each drive before a Set Parameters command is issued.

Status Register

The controller sets up the status register with the command status after execution. The program must look at this register to determine the result of any operation. If the busy bit is set, no other bits are valid. A read of the status register clears interrupt request 14. If 'write fault' or 'error' is active, or if 'seek complete' or 'ready' is inactive, a multisector operation is aborted.

The following defines the bits of the status register:

Bit 7 Busy—This bit indicates the controller status. A 1 indicates the controller is executing a command. If this bit is set, no other status register bit is valid, and the other registers reflect the status register's contents; therefore, the busy bit must be examined before any fixed disk register is read.

Bit 6 Drive Ready—A 1 on this bit together with a 1 on seek complete bit (bit 4) indicates that the fixed disk drive is ready to read, write, or seek. A 0 indicates that read, write, and seek are inhibited.

Bit 5 Write Fault—A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.

Bit 4 Seek Complete—A 1 on this bit indicates that the read/write heads have completed a seek operation.

Bit 3 Data Request—This bit indicates that the sector buffer requires servicing during a Read or Write command. If either bit 7 (busy) or this bit is active, a command is being executed. Upon receipt of any command, this bit is reset.

Bit 2 Corrected Data—A 1 on this bit indicates that the data read from the disk was successfully corrected by the ECC algorithm. Soft errors will not end multisector operations.

Bit 1 Index—This bit is set to 1 each revolution of the disk.

Bit 0 Error—A 1 on this bit indicates that the previous command ended in an error, and that one or more bits are set in the error register. The next command from the controller resets the error bit. This bit, when set, halts multisector operations.

Command Register

The command register accepts twelve commands to perform fixed disk operations. Commands are executed by loading the task file and writing in the command register while the controller status is not busy. If '-write fault' is active or if '-drive ready' or '-seek complete' are inactive, the controller will not execute any command. Any code not defined in the following table causes an Aborted Command error. Interrupt request 14 is reset when any command is written. Interrupt level 14 is not shared. The following are acceptable commands to the command register:

Command	Bits 7 6 5 4 3 2 1 0
Restore	0 0 0 1 x x x x
Seek	0 1 1 1 x x x x
Read Sector	0 0 1 0 0 0 L T
Write Sector	0 0 1 1 0 0 L T
Format Track	0 1 0 1 0 0 0 0
Read Verify	0 1 0 0 0 0 0 T
Diagnose	1 0 0 1 0 0 0 0
Set Parameters	1 0 0 1 0 0 0 1
Reserved	0 0 1 1 1 1 0 0
Init ESDI	1 1 1 0 0 0 0 0
Write Stack	1 1 1 0 1 0 0 0
Read Stack	1 1 1 0 0 1 0 0

Figure 3. Valid Command-Register Commands

The following figure shows the bit definitions for bits L and T:

Bit	Definition	0	1
L	Data Mode	Data Only	Data 7 byte ECC
T	Retry Mode	Retries Enabled	Retries Disabled

Figure 4. L and T Bit Definitions

Note: The system verifies the operation of ECC by reading and writing with the ECC bytes. When retries are disabled, ECC and ID field retries are limited to less than two complete revolutions.

The following are descriptions of the valid command-register commands:

Restore

A seek to cylinder 0 command is sent to the selected drive. The drive heads seek to cylinder 0 and any track offsets are cleared. The command terminates if the drive cannot accept the command, a transfer protocol or a transfer parity error is detected. When the command is terminated, error bits are set in the status register and the error register. An interrupt is generated at the end of the command.

Seek

The Seek command moves the read/write heads to the cylinder specified in the task files. The adapter supports overlapped seeking on two drives. An interrupt is generated at the completion of the command.

Read Sector

A number of sectors (1–256) may be read from the fixed disk with or without the ECC field appended in the Programmed I/O (PIO) mode. If the heads are not over the target track, an implied seek occurs. Data errors, up to 12 bits in length, are automatically corrected on Read Short commands. If an uncorrectable error occurs, the data transfer still takes place; however, a multisector read ends after the system reads the sector in error. Interrupts occur as each sector is read by the system. No interrupt is generated at the end of the command, after the last sector is read by the system.

Write Sector

A number of sectors (1–256) may be written to the fixed disk with or without the ECC field appended in the PIO mode. The Write Sector command also supports implied seeks. Interrupts for the Write command occur before each sector is transferred to the buffer (except the first) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and 'data request' is active.

Format Track

The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table is composed of two bytes per sector as follows: 00, Physical Sector 1, 00, Physical Sector 2, ... 00,Physical Sector 17. The table for 4-to-1 interleave is: 00, 01, 00, 0A, 00, 13, 00, 1C, 00, 02, 00, 0B, 00, 14, 00, 1D, 00, 08, 00, 11, 00, 1A, 00, 23, 00, 09, 00, 12, 00, 1B, 00, 24. The data transfer must be 512 bytes even though the table may be only 72 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. An interrupt is generated at the completion of the command; the Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80. When switching between drives, a restore command must be executed prior to attempting a format.

Read Verify

This command is similar to a Read command except that no data is sent to the host. This allows the system to verify the integrity of the fixed disk drive. A single interrupt is generated upon completion of the command or in the event of an error.

Initialize ESDI

This command allows the system to instruct a selected drive by direct command communication. The system must load the transfer data registers (high and low data bytes) prior to issuing the command. The controller serializes the data, adds parity and sends the command to the drive. The drive executes the command and returns status to the transfer data registers for system interpretation.

Diagnose

This command causes the adapter to execute its self-test code and return the results to the error register. An interrupt is generated at the completion of this command.

Write Data Stack

This system diagnostic command verifies the I/O channel to controller data path and control logic. The data sector buffer must be filled with 512 data bytes. The data is not examined by the control processor for correct information. The controller requests data using the normal data request status bit. Command completion will not generate a completion interrupt. A fixed-disk drive does not need to be present for command execution.

Read Data Stack

This system diagnostic command transfers the sector data buffer to system memory. The sector buffer data is not altered (from any previous read or write operation). A command completion interrupt is not generated nor is any drive activity required.

Set Parameters

This command sets up the drive parameters (maximum number of heads and sectors per track). The drive/head register specifies the drive affected. The sector count and drive/head registers must be set up before this command is issued. The adapter uses the values specified for track and cylinder crossing during multisector operations. An interrupt is generated at the completion of this command. This command must be issued before any multisector operations are attempted.

Miscellaneous Information

The following is miscellaneous information about the fixed disk drive function:

- The adapter performs normal read/write operations on a data field only after a successful match of that sector's ID with the targeted ID.
- ID fields are checked for errors when read from the disk.
- The adapter supports only ECC on data fields and only CRC on ID fields. The CRC polynomial is X16 + X12 + X5 + 1; the ECC polynomial is X56 + X52 + X50 + X43 + X41 + X34 + X30 + X26 + X24 + X8 + 1. All shift registers are preset to hex F before calculating the checksums, which begin with the respective address marks.

Diskette Function

One or two diskette drives are attached to the adapter through an internal, daisy-chained, flat cable. The attachment supports 160K.-, 320K.-, 360K.-,and 1.2M.-byte diskette drives.

The adapter is designed for a double-density, MFM-coded, diskette drive and uses write precompensation with an analog circuit for clock and data recovery. The diskette-drive parameters are programmable, and the diskette drive's write-protect feature is supported. The adapter is buffered on the I/O bus and uses the system board direct memory access (DMA) for record data transfers. An interrupt level 6 indicates when an operation is complete or when a status condition requires microprocessor attention.

Digital Output Register (Hex 3F2)

The digital output register (DOR) is an output-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions follow:

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Drive B Motor Enable

Bit 4 Drive A Motor Enable

Bit 3 Enable Diskette Interrupts and DMA

Bit 2 Diskette Function Reset

Bit 1 Reserved

Bit 0 Drive Select—A 0 on this bit indicates that drive A is selected.

Note: A channel reset clears all bits.

Digital Input Register

The digital input register is an 8-bit, read-only register used for diagnostic purposes. The following are bit definitions for this register:

Bit 7 Diskette Change

Bit 6 Write Gate

Bit 5 Head Select 3/Reduced Write Current

Bit 4 Head Select 2

Bit 3 Head Select 1

Bit 2 Head Select 0

Bit 1 Drive Select 1

Bit 0 Drive Select 0.

Note: Bits 0 through 6 apply to the currently selected fixed disk drive.

Data Rates

The diskette function will support three data rates: 250,000, 300,000 and 500,000 bits per second. The 300,000-and 500,000-bps incoming data pulse widths will be those associated with a 500,000-bps data signal.

Diskette Controller

The diskette controller has two registers to which the main system processor has access: a status register and a data register. The 8-bit status register has the status information about the diskette and may be accessed at any time. The 8-bit data register (hex 3F5), which actually consists of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, and parameters, and provides diskette-drive status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command. The main status register may only be read and is used to facilitate the transfer of data between the processor and diskette controller.

The bits in the main status register (hex 34F) are defined as follows:

Bit 7 Request for Master (RQM)— The data register is ready to send or receive data to or from the processor.

Bit 6 Data Input/Output (DIO)—The direction of data transfer between the diskette controller and the processor. If this bit is a 1, transfer is from the diskette controller data register to the processor; if it is a 0, the opposite is true.

Bit 5 Non-DMA Mode (NDM)—The diskette controller is in the non-DMA mode.

Bit 4 Diskette Controller Busy (CB)— A Read or Write command is being executed.

Bit 3 Reserved.

Bit 2 Reserved.

Bit 1 Diskette Drive B Busy (DBB)— Diskette drive B is in the seek mode.

Bit 0 Diskette Drive A Busy (DAB)— Diskette drive A is in the seek mode.

The diskette controller can perform 11 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a

multibyte transfer back to the processor. Because of this multibyte interchange of information between the diskette controller and the processor, each command can be considered to consist of three phases:

Command Phase

The processor issues a sequence of Write commands to the diskette controller that direct the controller to perform a specific operation.

Execution Phase

The diskette controller performs the specified operation.

Result Phase

After completion of the operation, status and other housekeeping information is made available to the processor through a sequence of Read commands to the processor.

Diskette Controller Commands

The following is a list of commands that may be issued to the diskette controller:

- **Read Data**
- **Format a Track**
- **Scan Equal**
- **Scan Low or Equal**
- **Scan High or Equal**
- **Recalibrate**
- **Sense Interrupt Status**
- **Specify**
- **Sense Drive Status**
- **Seek**
- **Invalid.**

Symbol Descriptions

The following are descriptions of the symbols used in the Command Definitions later in this section:

A0 Address Line 0—A 0 selects the main status register, and a 1 selects the data register.

C Cylinder Number—Contains the current or selected cylinder number in binary notation.

D Data—Contains the data pattern to be written to a sector.

D7-D0 Data Bus—An 8-bit data bus in which D7 is the most-significant bit and D0 is the least-significant.

DTL Data Length—When N is 00, DTL is the data length read from or written to a sector.

EOT End of Track—The final sector number on a cylinder.

GPL Gap Length—The length of gap 3 (spacing between sectors excluding the VCO synchronous field).

H Head Address—The head number, either 0 or 1, as specified in the ID field.

HD Head—The selected head number, 0 or 1. (H = HD in all command words.)

HLT Head Load Time—The head load time in the selected drive (2 to 256 milliseconds in 2-millisecond increments for the 1.2M-byte drive and 4 to 512 milliseconds in 4 millisecond increments for the 320K-byte drive).

HUT Head Unload Time—The head unload time after a read or write operation (0 to 240 milliseconds in 16-millisecond increments for the 1.2M-byte drive and 0 to 480 milliseconds in 32- millisecond increments for the 320K-byte drive.

MF FM or MFM Mode—A 0 selects FM mode and a 1 selects MFM (MFM is selected only if it is implemented.)

MT Multitrack—A 1 selects multitrack operation. (Both HD0 and HD1 will be read or written.)

N Number—The number of data bytes written in a sector.

NCN New Cylinder—The new cylinder number for a seek operation

ND Non-Data Mode— This indicates an operation in the nondata mode.

PCN Present Cylinder Number—The cylinder number at the completion of a Sense interrupt status command (present position of the head).

R Record—The sector number to be read or written.

R/W Read/Write—This stands for either a 'read' or 'write' signal.

SC Sector—The number of sectors per cylinder.

SK Skip—This stands for skip deleted-data address mark.

SRT This 4 bit byte indicates the stepping rate for the diskette drive as follows:

1.2M-Byte Diskette Drive
1111 1 millisecond
1110 2 milliseconds
1101 3 milliseconds

320K-Byte Diskette Drive
1111 2 milliseconds
1110 4 milliseconds
1101 6 milliseconds

ST 0—ST 1 Status 0—Status 3—One of the four registers that stores status information after a command is executed.

STP Scan Test—If STP is 1, the data in contiguous sectors is compared with the data sent by the processor during a scan operation. If STP is 2, then alternate sections are read and compared.

US0—US1 Unit Select—The selected driver number encoded the same as bits 0 and 1 of the digital output register (DOR).

Controller Commands

The following are commands that may be issued to the controller:

Note: An X is used to indicate a don't-care condition.

Read Data

Command Phase

The following bytes are issued by the processor in the command phase:

MT	MF	SK	0	0	1	1	0
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
DTL.							

Result Phase

The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N.

Format a Track

Command Phase

The following bytes are issued by the processor in the command phase:

0	MF	0	0	1	1	0	0
X	X	X	X	X	HD	US1	US0
N							
SC							
GPL							
D.							

Result Phase

The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N.

Scan Equal

Command Phase

The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	0	0	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP.							

Result Phase

The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N.

Scan Low or Equal

Command Phase

The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	1	0	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP.							

Result Phase

The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N.

Scan High or Equal

Command Phase

The following bytes are issued by the processor in the command phase:

```
MT  MF  SK  1  1  1   0   1
X   X   X   X  X  HD  US1 US0
C
H
R
N
EOT
GPL
STP.
```

Result Phase

The following bytes are issued by the controller in the result phase:

```
ST0
ST1
ST2
C
H
R
N.
```

Recalibrate

Command Phase

The following bytes are issued by the processor in the command phase:

```
0  0  0  0  0  1   1    1
X  X  X  X  X  0  US1  US0
```

Result Phase

This command has no result phase.

Sense Interrupt Status

Command Phase

The following bytes are issued by the processor in the command phase:

```
0  0  0  0  1  0  0  0
```

Result Phase

The following bytes are issued by the controller in the result phase:

```
STO
PCN.
```

Specify

Command Phase

The following bytes are issued by the processor in the command phase:

```
 0  0  0  0  0  0  1  1
(  SRT     )(   HUT    )
(      HLT          ) ND.
```

Result Phase

This command has no result phase.

Sense Driver Status

Command Phase

The following bytes are issued by the processor in the command phase:

```
0  0  0  0  0  0    1    0
X  X  X  X  X  HD  US1  US0
```

Result Phase

The following bytes are issued by the controller in the result phase:

```
ST3
```

Seek

Command Phase

The following bytes are issued by the processor in the command phase:

```
 0  0  0  0  1  1    1    1
 X  X  X  X  X  HD  US1  US0
NCN.
```

Result Phase

This command has no result phase.

Invalid

Command Phase

The following bytes are issued by the processor in the command phase:

```
Invalid Codes
 X  X  X  X  X  HD  US1  US0
```

Result Phase

The following bytes are issued by the controller in the result phase:

```
STO
```

Command Status Registers

The following is information about the command status registers ST0 through ST3.

Command Status Register 0 (ST0)

The following are bit definitions for command status register 0:

Bit 7–Bit 6 Interrupt Code (IC)

- **00** Normal Termination of Command (NT)—The command was completed and properly executed.
- **01** Abrupt Termination of Command (AT)—The execution of the command was started but not successfully completed.
- **10** Invalid Command Issue (IC)—The issued command was never started.
- **11** Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.

Bit 5 Seek End (SE)—Set to 1 when the controller completes the Seek command.

Bit 4 Equipment Check (EC)—Set if a 'fault' signal is received from the diskette drive, or if the 'track–0' signal fails to occur after 77 step pulses (Recalibrate Command).

Bit 3 Not Ready (NR)—This flag is set when the diskette drive is in the not-ready state and a Read or Write command is issued. It is also set if a Read or Write command is issued to side 1 of a single-sided diskette drive.

Bit 2 Head Address (HD)—Indicates the state of the head at interrupt.

Bit 1–Bit 0 Unit select 1 and 2 (US 1 and 2)—Indicate a drive unit number at interrupt.

Command Status Register 1 (ST1)

The following are bit definitions for command status register 1:

Bit 7 End of Cylinder (EC)—Set when the controller tries to gain access to a sector beyond the final sector of a cylinder.

Bit 6 Not Used—Always 0.

Bit 5 Data Error (DE)—Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 Overrun (OR)—Set if the controller is not serviced by the main system within a certain time limit during data transfers.

Bit 3 Not Used—This bit is always set to 0.

Bit 2 No Data (ND)—Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan Command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or, if the starting sector cannot be found during the execution of a Read Cylinder command.

Bit 1 Not Writable (NW)—Set if the controller detects a 'write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.

Bit 0 Missing Address Mark (MA)—Set if the controller cannot detect the ID address mark. At the same time, the MD of status register 2 is set.

Command Status Register 2 (ST2)

The following are bit definitions for command status register 2:

Bit 7 Not Used—Always 0.

Bit 6 Control Mark (CM)—This flag is set if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.

Bit 5 Data Error in Data Field (DD)—Set if the controller detects an error in the data.

Bit 4 Wrong Cylinder (WC)—This flag is related to ND (no data) and when the contents of C on the medium are different from that stored in the ID register, this flag is set.

Bit 3 Scan Equal Hit (SH)—Set if the contiguous sector data equals the processor data during the execution of a Scan command.

Bit 2 Scan Not Satisfied (SN)—Set if the controller cannot find a sector on the cylinder that meets the condition during a Scan command.

Bit 1 Bad Cylinder (BC)—Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set.

Bit 0 Missing Address Mark in Data Field (MD)— Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

Command Status Register 3 (ST3)

The following are bit definitions for command status register 3:

Bit 7 Fault (FT)—Status of the 'fault' signal from the diskette drive.

Bit 6 Write Protect (WP)—Status of the 'write-protect' signal from the diskette drive.

Bit 5 Ready (RY)—Status of the 'ready' signal from the diskette drive.

Bit 4 Track 0 (T0)—Status of the 'track 0' signal from the diskette drive.

Bit 3 Two Side (TS)—Status of the 'two side' signal from the diskette drive.

Bit 2 Head Address (HD)—Status of the 'side-select' signal from the diskette drive.

Bit 1 Unit Select 1 (US 1)—Status of the 'unit-select-1' signal from the diskette drive.

Bit 0 Unit Select 0 (US 0)—Status of the 'unit select 0' signal from the diskette drive.

Interfaces

The system interface is through the I/O channel. The address, DMA, and interrupt assignments are shown in the following figures:

I/O Address			
Primary	**Secondary**	**Read**	**Write**
3F2	372		Digital output register
3F4	374	Main status register	Main status register
3F5	375	Diskette data register	Diskette data register
3F6	376		Fixed disk register
3F7	377	Digital input register	Diskette control register

Figure 5. Diskette Function

Note: DMA request is level 2 and interrupt request is level 6. Interrupt level 6 is a nonshared interrupt.

I/O Address			
Primary	**Secondary**	**Read**	**Write**
1F0	170	Data register	Data register
1F1	171	Error register	Not used
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder low	Cylinder low
1F5	175	Cylinder high	Cylinder high
1F6	176	Drive/head register	Drive/head register
1F7	177	Status register	Command register

Figure 6. Fixed Disk Function

Note: Interrupt request is level 14. Interrupt level 14 is a nonshared interrupt.

The following operations are supported by this adapter:

- Sixteen bit programmed I/O (PIO) data transfers to the fixed disk. All other transfers must be 8 bits wide.
- The I/O addresses, recognized by the adapter for either the fixed disk or the diskette function, are independently selected by jumpers.

Interface Lines

The interface to the fixed disk drive consists of two cables: 'control' and 'data'. The following figures show signals and pin assignments for these cables:

Signal Name	Signal Pin	Gnd Pin
- Head Select 2^3	2	1
- Head Select 2^2	4	3
- Write Gate	6	5
- Configuration/Status Data	8	7
- Transfer Acknowledge	10	9
- Attention	12	11
- Head Select 2^0	14	13
- Sector	16	15
- Head Select 2^1	18	17
- Index	20	19
- Ready	22	21
- Transfer Request	24	23
- Drive Select 1	26	25
- Drive Select 2	28	27
- Drive Select 3	30	29
- Read Gate	32	31
- Command Data	34	33

Figure 7. Control Signal Lines (J1/P1)

Note: Connection is through a 2-by-17 Berg connector. Pin 15 is reserved to polarize the connector.

Signal Name	Signal Pin	Gnd Pin
- Drive Selected	1	
- Sector	2	
- Command Complete	3	
Reserved	4	
Reserved	5	6
+ Write Clock	7	
- Write Clock	8	
Reserved	9	
+ Read/Reference Clock	10	
- Read/Reference Clock	11	12
+ NRZ Write Data	13	15
- NRZ Write Data	14	16.
+ NRZ Read Data	17	
- NRZ Read Data	18	19
- Index	20	

Figure 8. Data Transfer Signal Lines (J2/P2)

Note: Connection is through a 2-by-10 Berg connector. Pin 8 is reserved to polarize the connector.

The interface to the diskette drives is a single cable that carries both data and control signals. The signals and pin assignments are as follows:

Signal Name	Signal Pin	Gnd Pin
- Reduced Write	2	1
- Reserved	4	3
- Reserved	6	5
- Index	8	7
- Motor Enable Drive 1	10	9
- Drive Select 2	12	11
- Drive Select 1	14	13
- Motor Enable Drive 2	16	15
- Direction Select	18	17
- Step	20	19
- Write Data	22	21
- Write Gate	24	23
- Track 00	26	25
- Write Protect	28	27
- Read Data	30	29
- Side 1 Select	32	31
- Diskette Change	34	33

Figure 9. Control Signal Lines (J1/P1)

Note: Connection is through a 2-by-17 Berg connector. Pin 15 is reserved to polarize the connector.

IBM

Personal Computer Hardware Reference Library

ENHANCED SMALL DEVICE INTERFACE (ESDI) ADAPTER

Enhanced Small Device Interface (ESDI) Adapter

Contents

Description

The Enhanced Small Device Interface (ESDI) Adapter connects to the system board using one of the I/O slots. The adapter controls the 5-1/4 inch diskette drives and fixed-disk drives. Connectors on the adapter supply all the signals necessary to operate up to two fixed-disk drives and two diskette drives. The adapter allows concurrent data operations on one diskette and one fixed-disk drive.

The adapter operates when connected to a channel I/O slot. This channel is described in the "I/O Channel" section of the RT PC Technical Reference Manual.

Fixed Disk Function

The fixed disk function features 512-byte sectors; high-speed, Programmed I/O (PIO) data transfers; Error Correcting Code (ECC) correction of up to 12 bits on data fields; multiple sector operations across track and cylinder boundaries; and on-board diagnostic tests. The adapter supports two fixed disks with up to 16 read/write heads and 2048 cylinders.

Task File

A task file, which contains eight registers, controls fixed-disk operations. The following figure shows the addresses and functions of these registers:

I/O Address			
Primary	**Secondary**	**Read**	**Write**
1F0	170	Data register	Data register
1F1	171	Error register	Not used
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder low	Cylinder low
1F5	175	Cylinder high	Cylinder high
1F6	176	Drive/head register	Drive/head register
1F7	177	Status register	Command register

Figure 1. Task File

Task File Registers

Data Register

The data register provides access to the sector buffer for read/write operations in the PIO mode. This register must not be accessed unless a Read/Write command is being executed. The register provides a 16-bit path into the sector buffer for normal Read/Write commands. When a R/W Long is issued, the 7 ECC bytes are transferred by byte with at least 2 microseconds between transfers. Data Request (DRQ) must be active before the transferring of the ECC bytes.

Error Register

The error register is a read-only register that contains specific information related to the previous command. The data is valid only when the error bit in the status register is set, unless the adapter is in diagnostic mode. Diagnostic mode is the state immediately after power is switched on or after a **Diagnose** command. In these cases, the register must be checked regardless of the status register indicator. The following are bit values for the diagnostic mode:

Diagnostic Mode

01 No errors

02 ESDI adapter device error

03 Disk controller error

04 Sector buffer error

05 ECC device error

06 Logic support device error

07 Control processor error.

The following are bit definitions for the operational mode:

Operational Mode

Bit 0 Data Address Mark (DAM) Not Found—This bit indicates that DAM could not be found within 16 bytes of the ID field.

Bit 1 TR 000 Error—This bit will be set if, during a Restore command, the track 000 line from the fixed disk is not true within 2047 step pulses to the drive.

Bit 2 Aborted Command—A command is aborted based on the drive status (Write Fault, Not Seek Complete, Drive Not Ready, or an invalid command). The status and error registers may be decoded to determine the cause.

Bit 3 Not used.

Bit 4 ID Not Found—The ID field with the specified cylinder, head, and sector number could not be found. If retries are enabled, the controller attempts to read the ID 160 times before indicating the error. If retries are disabled, the track is scanned a maximum of 20 times before setting this error bit.

Bit 5 Not used.

Bit 6 Data ECC Error—This bit indicates that an uncorrectable ECC error occurred in the target's data field during a read command.

Bit 7 Bad Block Detect—This bit indicates that the bad block mark was detected in the target's ID field. No Read or Write commands will be executed in any data fields marked bad.

Sector Count Register

The sector count register defines the number of sectors transferred during a Verify, Read, Write, or Format command. During a multisector operation, the sector count is decremented and the sector number is incremented. When the disk is being formatted, the number of sectors per track must be loaded into the register prior to each Format command. The adapter supports multisector transfers across track and cylinder boundaries. The drive characteristics must be set up by the Set Parameters command before initiating a multisector transfer. The sector count register must be loaded with the number of sectors to be transferred for any data-related command.

Note: A 0 in the sector count register specifies a 256-sector transfer.

Sector Number Register

The target's logical sector number for Read, Write, and Verify commands is loaded into this register. The starting sector number is loaded into this register for multisector operations.

Cylinder Number Registers

The target number for Read, Write, Seek, and Verify commands is loaded into these registers as shown in the following figure. The cylinder-number registers address up to 2048 cylinders.

	Cylinder High	**Cylinder Low**
Register bits Cylinder bits	76543210 ------A98	76543210 76543210

Figure 2. Cylinder Number Registers

Drive/Head Register

Bit 7 Set to 1

Bit 6 Set to 0

Bit 5 Set to 1

Bit 4 Drive Select—This bit selects the drive. A 0 indicates the first fixed-disk drive, and a 1 indicates the second.

Bit 3–Bit 0 Head Select Bits—Bits 3 through 0 specify the desired read/write head. Bit 0 is the least significant (0101 selects head 5). The adapter supports up to 16 read/write heads. Note: This register must be loaded with the maximum number of heads for each drive before a Set Parameters command is issued.

Status Register

The controller sets up the status register with the command status after execution. The program must look at this register to determine the result of any operation. If the busy bit is set, no other bits are valid. A read of the status register clears interrupt request 14. If 'write fault' or 'error' is active, or if 'seek complete' or 'ready' is inactive, a multisector operation is aborted.

The following defines the bits of the status register:

Bit 7 Busy—This bit indicates the controller status. A 1 indicates the controller is executing a command. If this bit is set, no other status register bit is valid, and the other registers reflect the status register's contents; therefore, the busy bit must be examined before any fixed disk register is read.

Bit 6 Drive Ready—A 1 on this bit together with a 1 on seek complete bit (bit 4) indicates that the fixed-disk drive is ready to read, write, or seek. A 0 indicates that read, write, and seek are inhibited.

Bit 5 Write Fault—A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.

Bit 4 Seek Complete—A 1 on this bit indicates that the read/write heads have completed a seek operation.

Bit 3 Data Request—This bit indicates that the sector buffer requires servicing during a Read or Write command. If either bit 7 (busy) or this bit is active, a command is being executed. Upon receipt of any command, this bit is reset.

Bit 2 Corrected Data—A 1 on this bit indicates that the data read from the disk was successfully corrected by the ECC algorithm. Soft errors will not end multisector operations.

Bit 1 Command in progress.

Bit 0 Error—A 1 on this bit indicates that the previous command ended in an error, and that one or more bits are set in the error register. The next command from the controller resets the error bit. This bit, when set, halts multisector operations.

Command Register

The command register accepts twelve commands to perform fixed disk operations. Commands are executed by loading the task file and writing in the command register while the controller status is not busy. If '-write fault' is active or if '-drive ready' or '-seek complete' are inactive, the controller will not execute any command. Any code not defined in the following table causes an Aborted Command error. Interrupt request 14 is reset when any command is written. Interrupt level 14 is not shared. The following are acceptable commands to the command register:

Command	Bits 7	6	5	4	3	2	1	0
Restore	0	0	0	1	x	x	x	x
Seek	0	1	1	1	x	x	x	x
Read Sector	0	0	1	0	0	0	L	T
Write Sector	0	0	1	1	0	0	L	T
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1
Reserved	0	0	1	1	1	1	0	0
Init ESDI	1	1	1	0	0	0	0	0
Write Stack	1	1	1	0	1	0	0	0
Read Stack	1	1	1	0	0	1	0	0

Figure 3. Valid Command-Register Commands

The following figure shows the bit definitions for bits L and T:

Bit	Definition	0	1
L	Data Mode	Data Only	Data + 7 byte ECC
T	Retry Mode	Retries Enabled	Retries Disabled

Figure 4. L and T Bit Definitions

Note: The system verifies the operation of ECC by reading and writing with the ECC bytes. When retries are disabled, ECC and ID field retries are limited to less than two complete revolutions.

The following are descriptions of the valid command-register commands:

Restore

A seek to cylinder 0 command is sent to the selected drive. The drive heads seek to cylinder 0 and any track offsets are cleared. The command terminates if the drive cannot accept the command, a transfer protocol or a transfer parity error is detected. When the command is terminated, error bits are set in the status register and the error register. An interrupt is generated at the end of the command.

Seek

The Seek command moves the read/write heads to the cylinder specified in the task files. The adapter supports overlapped seeking on two drives. An interrupt is generated at the completion of the command.

Read Sector

A number of sectors (1–256) may be read from the fixed disk with or without the ECC field appended in the (PIO) mode. If the heads are not over the target track, an implied seek occurs. Data errors, up to 12 bits in length, are automatically corrected on Read Short commands. If an uncorrectable error occurs, the data transfer still takes place; however, a multisector read ends after the system reads the sector in error. Interrupts occur as each sector is read by the system. No interrupt is generated at the end of the command, after the last sector is read by the system.

Write Sector

A number of sectors (1–256) may be written to the fixed disk with or without the ECC field appended in the PIO mode. The Write Sector command also supports implied seeks. Interrupts for the Write command occur before each sector is transferred to the buffer (except the first) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and 'data request' is active.

Format Track

The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table is composed of two bytes per sector as follows: 00, Physical Sector 01, 00, Physical Sector 02, ... 00,Physical Sector 24. The hexadecimal table for 4-to-1 interleave is: 00, 01, 00, 0A, 00, 13, 00, 1C, 00, 02, 00, 0B, 00, 14, 00, 1D, 00, 03, 00, 0C, 00, 15, 00, 1E, 00, 04, 00, 0D, 00, 16, 00, 1F, 00, 05, 00, 0E, 00, 17, 00, 20, 00, 06, 00, 0F, 00, 18, 00, 21, 00, 07, 00, 10, 00, 19, 00, 22, 00, 08, 00, 11, 00, 1A, 00, 23, 00, 09, 00, 12, 00, 1B, 00, 24. The data transfer must be 512 bytes even though the table may be only 72 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. An interrupt is generated at the completion of the command; the Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80. When switching between drives, a restore command must be executed prior to attempting a format.

Read Verify

This command is similar to a Read command except that no data is sent to the host. This allows the system to verify the integrity of the fixed-disk drive. A single interrupt is generated upon completion of the command or in the event of an error.

Diagnose

This command causes the adapter to execute its self-test code and return the results to the error register. An interrupt is generated at the completion of this command.

Write Data Stack

This system diagnostic command verifies the I/O channel to controller data path and control logic. The data sector buffer must be filled with 512 data bytes. The data is not examined by the control processor for correct information. The controller requests data using the normal data request status bit. Command completion will not generate a completion interrupt. A fixed-disk drive does not need to be present for command execution.

Read Data Stack

This system diagnostic command transfers the sector data buffer to system memory. The sector buffer data is not altered (from any previous read or write operation). A command completion interrupt is not generated nor is any drive activity required.

Set Parameters

This command sets up the drive parameters (maximum number of heads and sectors per track). The drive/head register specifies the drive affected. The sector count and drive/head registers must be set up before this command is issued. The adapter uses the values specified for track and cylinder crossing during multisector operations. An interrupt is generated at the completion of this command. This command must be issued before any multisector operations are attempted.

Miscellaneous Information

The following is miscellaneous information about the fixed-disk drive function:

- The adapter performs normal read/write operations on a data field only after a successful match of that sector's ID with the targeted ID.
- ID fields are checked for errors when read from the disk.
- The adapter supports only ECC on data fields and only Cycle Redundancy Check (CRC) on ID fields. The CRC polynomial is X16 + X12 + X5 + 1; the ECC polynomial is X56 + X52 + X50 + X43 + X41 + X34 + X30 + X26 + X24 + X8 + 1. All shift registers are preset to hex F before calculating the checksums, which begin with the respective address marks.

Diskette Function

One or two diskette drives are attached to the adapter through an internal, daisy-chained, flat cable. The attachment supports 360K- and 1.2M-byte diskette drives.

The adapter is designed for a double-density, MFM-coded, diskette drive and uses write precompensation with an analog circuit for clock and data recovery. The diskette-drive parameters are programmable, and the diskette drive's write-protect feature is supported. The adapter is buffered on the I/O bus and uses the system board direct memory access (DMA) for record data transfers. An interrupt level 6 indicates when an operation is complete or when a status condition requires microprocessor attention. Interrupt level 6 does not support interrupt sharing.

Digital Output Register (Hex 3F2)

The digital output register (DOR) is a write-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions follow:

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Drive B Motor Enable (Active high)

Bit 4 Drive A Motor Enable (Active high)

Bit 3 Enable Diskette Interrupts and DMA (Active high)

Bit 2 Diskette Function Reset (Active low)

Bit 1 Reserved

Bit 0 Drive Select—A 0 on this bit indicates that drive A is selected.

Drive Select—A 1 on this bit indicates that drive B is selected.

Note: A channel reset clears all bits.

Digital Input Register

The digital input register is an 8-bit, read-only register used for diagnostic purposes. All bits are active high. The following are bit definitions for this register:

Bit 7 Diskette Change

Bit 6 Write Gate

Bit 5 Head Select 3/Reduced Write Current

Bit 4 Head Select 2

Bit 3 Head Select 1

Bit 2 Head Select 0

Bit 1 Drive Select 1

Bit 0 Drive Select 0.

Note: Bits 0 through 6 apply to the currently selected fixed-disk drive.

Diskette Control Register (Hex 3F7)

Bits 7 - 2 Reserved.

Bits 1 - 0 Selects read/write data rate.

00	500K-bps
01	300K-bps
10	250K-bps
11	Reserved

Data Rates

The diskette function will support three data rates: 250,000, 300,000 and 500,000 bits per second. The 300,000- and 500,000-bps incoming data pulse widths will be those associated with a 500,000-bps data signal.

Diskette Controller

The diskette controller has two registers to which the main system processor has access: a status register and a data register. The 8-bit status register has the status information about the diskette and may be accessed at any time. The 8-bit data register (hex 3F5), which actually consists of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, and parameters, and provides diskette-drive status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command. The main status register may only be read and is used to facilitate the transfer of data between the processor and diskette controller.

The bits in the main status register (hex 3F4) are active high and are defined as follows:

Bit 7 Request for Master (RQM)—The data register is ready to send or receive data to or from the processor.

Bit 6 Data Input/Output (DIO)—The direction of data transfer between the diskette controller and the processor. If this bit is a 1, transfer is from the diskette controller data register to the processor; if it is a 0, the opposite is true.

Bit 5 Non-DMA Mode (NDM)—The diskette controller is in the non-DMA mode.

Bit 4 Diskette Controller Busy (CB)—A Read or Write command is being executed.

Bit 3 Reserved.

Bit 2 Reserved.

Bit 1 Diskette Drive B Busy (DBB)—Diskette drive B is in the seek mode.

Bit 0 Diskette Drive A Busy (DAB)—Diskette drive A is in the seek mode.

The diskette controller can perform 7 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the diskette controller and the processor, each command can be considered to consist of three phases:

Command Phase

The processor issues a sequence of Write commands to the diskette controller that direct the controller to perform a specific operation.

Execution Phase

The diskette controller performs the specified operation.

Result Phase

After completion of the operation, status and other housekeeping information is made available to the processor through a sequence of Read commands to the processor. An interrupt (level 6) occurs at the beginning of the result phase.

During command or result phases the main status register must be read by the processor before each byte of information is written or read from the data register. Bits six and seven in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word can be written into the data register.

Diskette Controller Commands

The following is a list of commands that may be issued to the diskette controller:

- **Read Data**
- **Format a Track**
- **Recalibrate**
- **Sense Interrupt Status**
- **Specify**
- **Seek**
- **Invalid.**

Symbol Descriptions

The following are descriptions of the symbols used in the Command Definitions later in this section:

A0 Address Line 0—A 0 selects the main status register, and a 1 selects the data register.

C Cylinder Number—Contains the current or selected cylinder number in binary notation.

D Data—Contains the data pattern to be written to a sector.

D7-D0 Data Bus—An 8-bit data bus in which D7 is the most-significant bit and D0 is the least-significant.

DTL Data Length—When N is 00, DTL is the data length read from or written to a sector.

EOT End of Track—The final sector number on a cylinder.

GPL Gap Length—The length of gap 3 (spacing between sectors excluding the VCO synchronous field).

H Head Address—The head number, either 0 or 1, as specified in the ID field.

HD Head—The selected head number, 0 or 1. (H = HD in all command words.)

HLT Head Load Time—The head load time in the selected drive (2 to 256 milliseconds in 2-millisecond increments for the 1.2M-byte drive and 4 to 512 milliseconds in 4 millisecond increments for the 320K-byte drive).

HUT Head Unload Time—The head unload time after a read or write operation (0 to 240 milliseconds in 16-millisecond increments for the 1.2M-byte drive and 0 to 480 milliseconds in 32-millisecond increments for the 320K-byte drive.

MF MFM Mode—A 0 is reserved and a 1 selects MFM.

MT Multitrack—A 1 selects multitrack operation. (Both HD0 and HD1 will be read or written.)

N Number—The number of data bytes written in a sector. Number of bytes = 128 × 2*N.

NCN New Cylinder—The new cylinder number for a seek operation

ND No-Data—This indicates no data in status register 0.

PCN Present Cylinder Number—The cylinder number at the completion of a Sense interrupt status command (present position of the head).

R Record—The sector number to be read or written.

R/W Read/Write—This stands for either a 'read' or 'write' signal.

SC Sector—The number of sectors per cylinder.

SK Skip—This stands for skip deleted-data address mark.

SRT This 4 bit byte indicates the stepping rate for the diskette drive as follows:

1.2M-Byte Diskette Drive
1111 1 millisecond
1110 2 milliseconds
1101 3 milliseconds

320K-Byte Diskette Drive
1111 2 milliseconds
1110 4 milliseconds
1101 6 milliseconds

ST 0—ST 1 Status 0—Status 3—One of the four registers that stores status information after a command is executed.

US0 Drive A selected.

US1 Drive B selected.

Controller Commands

The following are commands that may be issued to the controller:

Note: An X is used to indicate a don't care condition.

Read Data

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	**Bits 7 - 0**
Byte 0	MT MF SK 0 0 1 1 0
Byte 1	X X X X X HD US1 US0
Byte 2	Cylinder Number
Byte 3	Head Address
Byte 4	Record
Byte 5	Number
Byte 6	End of Track
Byte 7	Gap Length
Byte 8	Data Length

Result Phase

The following bytes are issued by the controller in the result phase:

Byte	**Bits 7 - 0**
Byte 0	Status 0
Byte 1	Status 1
Byte 2	Status 2
Byte 3	Cylinder Number
Byte 4	Head Address
Byte 5	Record
Byte 6	Number

Format a Track

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 – 0
Byte 0	0 MF 0 0 1 1 0 1
Byte 1	X X X X X HD US1 US0
Byte 2	Number
Byte 3	Sector
Byte 4	Gap Length
Byte 5	Data

Result Phase

The following bytes are issued by the controller in the result phase:

Byte	Bits 7 – 0
Byte 0	Status 0
Byte 1	Status 1
Byte 2	Status 2
Byte 3	Cylinder Number
Byte 4	Head Address
Byte 5	Record
Byte 6	Number

Recalibrate

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 0 1 1 1
Byte 1	X X X X X 0 US1 US0

Result Phase

This command has no result phase.

Sense Interrupt Status

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 1 0 0 0

Result Phase

The following bytes are issued by the controller in the result phase:

Byte	Bits 7 - 0
Byte 0	Status 0
Byte 1	Present Cylinder Number

Specify

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 0 0 1 1
Byte 1	(SRT)(HUT)
Byte 2	(HLT) ND

Result Phase

This command has no result phase.

Seek

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 1 1 1 1
Byte 1	X X X X X HD US1 US0
Byte 2	New Cylinder

Result Phase

This command has no result phase.

Invalid

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	Invalid Codes

Result Phase

The following bytes are issued by the controller in the result phase:

Byte	Bits 7 - 0
Byte 0	Status 0

Command Status Registers

The following is information about the command status registers ST0 through ST3. All bits are active high.

Command Status Register 0 (ST0)

The following are bit definitions for command status register 0:

Bit 7–Bit 6 Interrupt Code (IC)

- **00** Normal Termination of Command (NT)—The command was completed and properly executed.
- **01** Abrupt Termination of Command (AT)—The execution of the command was started but not successfully completed.
- **10** Invalid Command Issue (IC)—The issued command was never started.
- **11** Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.

Bit 5 Seek End (SE)—Set to 1 when the controller completes the Seek command.

Bit 4 Equipment Check (EC)—Set if a 'fault' signal is received from the diskette drive, or if the 'track–0' signal fails to occur after 77 step pulses (Recalibrate Command).

Bit 3 Not Ready (NR)—This flag is set when the diskette drive is in the not-ready state and a Read or Write command is issued. It is also set if a Read or Write command is issued to side 1 of a single-sided diskette drive.

Bit 2 Head Address (HD)—Indicates the state of the head at interrupt.

Bit 1 Unit select 2 (US 2)—Indicates drive B at interrupt.

Bit 0 Unit select 1 (US 1)—Indicates drive A at interrupt.

Command Status Register 1 (ST1)

The following are bit definitions for command status register 1:

Bit 7 End of Cylinder (EC)—Set when the controller tries to gain access to a sector beyond the final sector of a cylinder.

Bit 6 Not Used—Always 0.

Bit 5 Data Error (DE)—Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 Overrun (OR)—Set if the controller is not serviced by the main system within a certain time limit during data transfers. The time limits are 11 microseconds for the 500K-bps data rate, 17.5 microseconds for the 300K-bps, and 24 microseconds for the 250K-bps data rate.

Bit 3 Not Used—This bit is always set to 0.

Bit 2 No Data (ND)—Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan Command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or, if the starting sector cannot be found during the execution of a Read Cylinder command.

Bit 1 Not Writable (NW)—Set if the controller detects a 'write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.

Bit 0 Missing Address Mark (MA)—Set if the controller cannot detect the ID address mark. At the same time, the MD of status register 2 is set.

Command Status Register 2 (ST2)

The following are bit definitions for command status register 2:

Bit 7 Not Used—Always 0.

Bit 6 Control Mark (CM)—This flag is set if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.

Bit 5 Data Error in Data Field (DD)—Set if the controller detects an error in the data.

Bit 4 Wrong Cylinder (WC)—This flag is related to ND (no data) and when the contents of C on the medium are different from that stored in the ID register, this flag is set.

Bit 3 Reserved

Bit 2 Reserved

Bit 1 Bad Cylinder (BC)—Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set.

Bit 0 Missing Address Mark in Data Field (MD)—Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

Command Status Register 3 (ST3)

The following are bit definitions for command status register 3:

Bit 7 Fault (FT)—Status of the 'fault' signal from the diskette drive.

Bit 6 Write Protect (WP)—Status of the 'write-protect' signal from the diskette drive.

Bit 5 Ready (RY)—Status of the 'ready' signal from the diskette drive.

Bit 4 Track 0 (T0)—Status of the 'track 0' signal from the diskette drive.

Bit 3 Two Side (TS)—Status of the 'two side' signal from the diskette drive.

Bit 2 Head Address (HD)—Status of the 'side-select' signal from the diskette drive.

Bit 1 Unit Select 1 (US 1)—Status of the 'unit-select-1' signal from the diskette drive.

Bit 0 Unit Select 0 (US 0)—Status of the 'unit select 0' signal from the diskette drive.

Interfaces

The system interface is through the I/O channel. The address, DMA, and interrupt assignments are shown in the following figures:

I/O Address			
Primary	**Secondary**	**Read**	**Write**
3F2	372		Digital output register
3F4	374	Main status register	
3F5	375	Diskette data register	Diskette data register
3F6	376	Disk alternate status reg.	Disk control register
3F7	377	Digital input register	Diskette control register

Figure 5. Diskette Function

Note: DMA request is level 2 and interrupt request is level 6. Interrupt level 6 is a nonshared interrupt.

I/O Address			
Primary	**Secondary**	**Read**	**Write**
1F0	170	Data register	Data register
1F1	171	Error register	Not used
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder low	Cylinder low
1F5	175	Cylinder high	Cylinder high
1F6	176	Drive/head register	Drive head register
1F7	177	Status register	Command register

Figure 6. Fixed Disk Function

Note: Interrupt request is level 14. Interrupt level 14 is a nonshared interrupt.

The following operations are supported by this adapter:

- Sixteen bit programmed I/O (PIO) data transfers to the fixed disk. All other transfers must be 8 bits wide.
- The I/O addresses, recognized by the adapter for the fixed disk and the diskette function, are selected by a jumper. Jumper insertion on pins 1 and 2 defines the secondary addresses.

Interface Lines

The interface to the fixed-disk drive consists of two cables: 'control' and 'data'. The following figures show signals and pin assignments for these cables:

Signal Name	Signal Pin	Gnd Pin
- Head Select 2^3	2	1
- Head Select 2^2	4	3
- Write Gate	6	5
- Configuration/Status Data	8	7
- Transfer Acknowledge	10	9
- Attention	12	11
- Head Select 2^0	14	13
- Sector	16	15
- Head Select 2^1	18	17
- Index	20	19
- Ready	22	21
- Transfer Request	24	23
- Drive Select 1	26	25
- Drive Select 2	28	27
- Drive Select 3	30	29
- Read Gate	32	31
- Command Data	34	33

Figure 7. Control Signal Lines (J1/P1)

Note: Connection is through a 2-by-17 Berg connector. Pin 15 is reserved to polarize the connector.

Signal Name	Signal Pin	Gnd Pin
- Drive Selected	1	
- Sector	2	
- Command Complete	3	
Reserved	4	
Reserved	5	6
+ Write Clock	7	
- Write Clock	8	
Reserved	9	
+ Read/Reference Clock	10	
- Read/Reference Clock	11	12
+ NRZ Write Data	13	15
- NRZ Write Data	14	16
+ NRZ Read Data	17	
- NRZ Read Data	18	19
- Index	20	

Figure 8. Data Transfer Signal Lines (J2/P2)

Note: Connection is through a 2-by-10 Berg connector. Pin 5 is reserved to polarize the connector.

The interface to the diskette drives is a single cable that carries both data and control signals. The signals and pin assignments are as follows:

Signal Name	Signal Pin	Gnd Pin
- Reduced Write	2	1
- Reserved	4	3
- Reserved	6	5
- Index	8	7
- Motor Enable Drive 1	10	9
- Drive Select 2	12	11
- Drive Select 1	14	13
- Motor Enable Drive 2	16	15
- Direction Select	18	17
- Step	20	19
- Write Data	22	21
- Write Gate	24	23
- Track 00	26	25
- Write Protect	28	27
- Read Data	30	29
- Side 1 Select	32	31
- Diskette Change	34	33

Figure 9. Control Signal Lines (J1/P1)

Note: Connection is through a 2-by-17 Berg connector. Pin 5 is reserved to polarize the connector.

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Personal Computer Hardware Reference Library

EXTENDED ENHANCED SMALL DEVICE INTERFACE (ESDI) ADAPTER

Extended Enhanced Small Device Interface (ESDI) Adapter

Contents

Description

The Extended Enhanced Small Device Interface (ESDI) Adapter connects to the system board using one of the 16-bit I/O slots. The adapter controls the 5-1/4 inch diskette drives and fixed-disk drives. Connectors on the adapter supply all the signals necessary to operate up to three fixed-disk drives and two diskette drives. The adapter allows concurrent data operations on one diskette and one fixed-disk drive as well as overlapped seeks on the fixed-disk drives.

The adapter supports 16 bit data transfers to the fixed disk in both Programmed Input/Output (PIO) and system Direct Memory Access (DMA) modes. Status and command PIO transfers to the fixed disk must be 8 bit or 16 bit in PIO mode, but command transfers must be 16 bit in DMA mode. All diskette transfers are 8 bit.

The adapter operates when connected to a channel I/O slot. This channel is described in the "I/O Channel" section of the RT PC Technical Reference Manual.

Fixed-Disk PIO Mode

In PIO mode the adapter accepts commands, returns status, and transfers data with PIO operations. The commands are written to a task file, the status is read from status registers, and the data is transferred to or from a data stack.

The task file registers are loaded with the appropriate information. The last register loaded is the command register. When the command register is loaded, the adapter executes the defined command using the other registers where appropriate.

When a Seek command is issued to the adapter, it selects the appropriate drive and sends the correct command data to the selected drive. Then the adapter resets the busy bit in the status register. When the previous Seek command is completed, the system sends either a Read or Write command to the drive. During a Write operation, the adapter sets Data Request when it is ready to accept write data into the data stack. After the data is transferred into the stack, the adapter remains busy until the data transfer to the selected drive is complete.

During a Read operation, the adapter sets the busy bit in the status register. After the first sector of data is read from the disk into the data stack, the adapter resets the busy bit and sets the Data Request bit to signal the system that a sector of data is ready for transferring to the system. The system will PIO the data (2 bytes at a time) and the adapter resets Data Request after the last data transfer occurs.

Task File Registers

PIO fixed-disk operations are controlled by a task file which is a set of 8-bit registers. PIO data transfers are done by a 16-bit data stack. The I/O addresses and register definitions are shown in the table below.

PIO Mode Address			
Primary	**Secondary**	**Read**	**Write**
01F0	0170	Data stack	Data stack
01F1	0171	Error register	Not used
01F2	0172	Sector count	Sector count
01F3	0173	Sector number	Sector number
01F4	0174	Cylinder low	Cylinder low
01F5	0175	Cylinder high	Cylinder high
01F6	0176	Drive/head register	Drive/head register
01F7	0177	Status register	Command register
03F6	0376	Interrupt status	Fixed disk register
05F3	0573	Mode control register	Mode control register

Figure 1. Task File

Note: The I/O addresses are selectable by a jumper on J6. P is for primary and S is for secondary.

PIO Data Stack

The data stack is a 16-bit wide stack providing access to an adapter buffer for read, write, format, and other operations which require data transfer. This stack should only be accessed during data transfer operations when Data Request is on and busy is off. The host may read or write from this stack for diagnostic purposes by means of the Read/Write Buffer command.

Error Register

The error register contains specific information related to the previous command. The data is valid only when the error bit in the status register is set, unless the adapter is in diagnostic mode. Diagnostic mode is defined as the time immediately after a adapter reset or after a Diagnose Command has been issued. In these cases the register must be checked regardless of the status register indication.

Diagnostic Mode

X'E1' No errors

X'E2' Control buffer error

X'E3' Data buffer error

X'E6' Gate array error

X'E8' AIC 010 error

X'EA' 8031 error

X'EC' Read Only Memory (ROM) error

X'EE' Stuck attention error

X'F0' Device error bit stuck on

Operational Mode

The following are bit definitions for the PIO operational mode:

X'C0' Bad block detected alternate

X'80' Bad block detected—The bad block mark is detected in the target ID field. No Read or Write commands are executed on any data fields marked bad.

X'40' Data Error Correcting Code (ECC) error—This indicates that an uncorrectable ECC error has occurred in the data field during a Read command. If retries are enabled, the controller attempts to read the sector 48 times before posting this error, otherwise no retries are attempted.

X'20' Reserved

X'10' ID Not Found—The ID field with the specified cylinder, head, and sector number could not be found. If retries are enabled, the controller attempts to read the ID up to 40 times prior to indicating the error.

X'08' Adapter failure—This bit indicates an adapter malfunction.

X'04' Terminated command—A command is aborted based on drive status such as Attention, Not Seek Complete, Drive Not Ready, or an Invalid command. The status and error registers may be decoded to determine the cause.

X'02' Track 0 error—This bit is set if, during a Restore command, the adapter was not able to complete a recalibrate.

X'01' Data Address Mark (DAM) not found—This indicates that the Data Address Mark (DAM) could not be found within 16 bytes of the ID field. With retries enabled, the adapter attempts to locate the DAM up to 48 times. If retries are disabled, only one attempt is made.

Sector Count Register

The sector count register defines the number of sectors transferred during a Verify, Read, Write, or Format command. During a multisector operation, the sector count is decremented and the sector number is incremented. When the disk is being formatted, the number of sectors per track must be loaded into the register prior to each Format command. The adapter supports multisector transfers across track and cylinder boundaries. The drive characteristics must be set up by the Set Parameters command before initiating a multisector transfer. The sector count register must be loaded with the number of sectors to be transferred for any data-related command.

Notes:

1. A 0 in the sector count register specifies a 256-sector transfer.
2. For multisector operations involving hard errors, sector count is not decremented after the hard error.
3. During single sector operations, the sector number is always decremented after the operation, regardless of errors.

Sector Number Register

The starting sector number for Read, Write, and Verify operations is loaded into this register. During multisector operations, the sector number increments after each sector is read unless a hard error occurs. In this case, the sector is not incremented after the error. For single sector operations the sector number is always incremented regardless of errors.

Cylinder Number Registers

The starting cylinder number for Read, Write, Seek, and Verify is loaded into these registers as shown below. Up to 2048 cylinders are addressed by the cylinder number registers.

	Cylinder High	Cylinder Low
Register bits Cylinder bits	76543210 ------A98	76543210 76543210

Figure 2. Cylinder Number Registers

Drive/Head Register

Bit 7 Drive enable

Bit 6 Drive select bit 1—Select drive 2.

Bit 5 Reserved

Bit 4 Drive select bit 0—Selects drive 0 or 1.

Bit 3 - Bit 0 Head select bits—Bits 3 through 0 specify the desired read/write head. Bit 0 is the least significant (0101 selects head 5). The adapter supports up to 16 read/write heads.

Note: This register must be loaded with the maximum number of heads for each drive before a Set Parameters command is issued.

The desired drive is specified by bits 7, 6 and 4 in the following way:

Bit 7	Bit 6	Bit 4	Drive
1	0	0	0
1	0	1	1
1	1	0	2
1	1	1	Reserved
0	X	X	No file selected

PIO Status Register

The controller sets up the status register with the command status after execution. The program must look at this register to determine the result of any PIO operation. If the busy bit is set, no other bits are valid. A read of the status register clears the active interrupt request. If 'write fault' or 'error' is active, or if 'command complete' or 'drive ready' is inactive, a multisector operation is aborted.

The following defines the bits of the status register:

Bit 7 Busy—This bit indicates the controller status. A 1 indicates the controller is executing a command. If this bit is set, no other status register bit is valid, therefore, the busy bit must be examined before any fixed disk register is read.

Bit 6 Drive Ready—A 1 on this bit together with a 1 on command complete bit (bit 4) indicates that the fixed-disk drive is ready to read, write, or seek. A 0 indicates that read, write, and seek are inhibited.

Bit 5 Write Fault—A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.

Bit 4 Command Complete—indicates that all commands to the file that is selected are complete.

Bit 3 Data Request—This bit indicates that the sector buffer requires servicing during a Read or Write command. If either bit 7 (busy) or this bit is active, a command is being executed. Upon receipt of any command, this bit is reset.

Bit 2 Corrected Data—A 1 on this bit indicates that the data read from the disk was successfully corrected by the ECC algorithm. Soft errors will not end multisector operations.

Bit 1 Reserved

Bit 0 Error—A 1 on this bit indicates that the previous command ended in an error, and that one or more bits are set in the error register. The next command from the controller resets the error bit. This bit, when set, halts multisector operations.

Notes:

1. Programmers must allow for the possibility that an interrupt could be present and automatically reset when reading the status register.
2. After any reset pulse or Diagnose command, busy must be activated within one millisecond and kept active until the self-diagnostics are complete. This time must be at least 10 milliseconds and not more than 1.4 seconds.

PIO Command Register

The command register accepts commands to perform fixed disk operations. Commands are executed by loading the task file and writing in the command register while the controller status is not busy. Any code not defined in the following table may cause an Aborted Command error.

Command	Bits 7	6	5	4	3	2	1	0
Restore	0	0	0	1	0	0	0	0
Seek	0	1	1	1	0	0	0	0
Read Sector	0	0	1	0	0	0	L	R
Write Sector	0	0	1	1	0	0	L	R
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	R
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1
Init ESDI	1	1	1	0	0	0	0	0
Read Data Buffer	1	1	1	0	0	0	0	1
Write Data Buffer	1	1	1	0	0	0	1	0

Figure 3. Valid Command-Register Commands

The following figure shows the bit definitions for bits L and R:

Bit	Definition	0	1
L	Data Mode	Data Only	Data + 4 byte ECC
R	Retry Mode	Retries Enabled	Retries Disabled

Figure 4. L and R Bit Definitions

Notes:

1. The system verifies the operation of ECC by reading and writing with the ECC bytes directly to the drive. This is done by setting bit L to 1. If the L bit is a 1, then the sector count must be a 1.
2. After a adapter reset, the data transfer mode is set to PIO.

The following are descriptions of the valid command-register commands:

Restore

A seek to cylinder 0 command is sent to the selected drive. The drive heads seek to cylinder 0 and any track offsets are cleared. The seek is retried up to six times before a Recalibrate command is sent. If the Recalibrate command fails, a track 0 error is returned. An interrupt is generated at the completion of the command.

Seek

The Seek command moves the read/write heads to the cylinder specified in the task files. The adapter supports overlapped seeking on all drives. An interrupt is generated when the command has been sent to the file. The system must monitor command complete before sending another command to that drive.

Read Sector

A number of sectors (1–256) may be read from the fixed disk with or without the ECC field appended in the Programmed I/O (PIO) mode. If the heads are not positioned over the target track, an implied seek occurs. Data errors, up to nine bits in length, are corrected if retries are enabled. If an uncorrectable error occurs, the adapter will not transfer the data, returns an uncorrectable error and an interrupt occurs. Interrupts occur as each sector is read by the system. No interrupt is generated at the end of the command, after the last sector is read by the system.

Note: If the *L* bit is a one, the sector count must be a one.

Write Sector

A number of sectors (1–256) may be written to the fixed disk with or without the ECC field appended in the PIO mode. The Write Sector command also supports implied seeks. Interrupts for the Write command occur before each sector is transferred to the buffer (except the first) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and 'data request' is active. If retries are enabled the adapter makes eight attempts at writing the data before reporting an error.

Note: If the *L* bit is a one, the sector count must be a one.

Format Track

The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The 1-to-1 interleave table is composed of two hexadecimal bytes per sector as follows: 00, 01, 00, 02, 00, 03, 00, 04, 00, 05, 00, 06, 00, 07, 00, 08, 00, 09, 00, 0A, 00, 0B, 00, 0C, 00, 0D, 00, 0E, 00, 0F, 00, 10, 00, 11, 00, 12, 00, 13, 00, 14, 00, 15, 00, 16, 00, 17, 00, 18, 00, 19, 00, 1A, 00, 1B, 00, 1C, 00, 1D, 00, 1E, 00, 1F, 00, 20, 00, 21, 00, 22, 00, 23, 00, 24. The data transfer must be 512 bytes even though the table may be only 72 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. An interrupt is generated at the completion of the command; the Format Track command supports no error reporting. A bad block may be specified by replacing a X'00' table entry with an X'80' or X'C0'. When switching between drives, a restore command must be executed prior to attempting a format.

Read Verify

This command is similar to a Read command except that no data is sent to the host. This allows the system to verify the integrity of the fixed-disk drive. A single interrupt is generated upon completion of the command or in the event of an error. If retries are enabled, 40 retries are attempted before posting an error in the error register.

Initialize ESDI

This command allows the system to instruct a selected drive by direct command communication. The system must load the command into the cylinder high and cylinder low registers (high and low data bytes) prior to issuing the command. The controller serializes the data, adds parity and sends the command to the drive. The drive executes the command and returns any status to the cylinder high and cylinder low registers for system interpretation. The following ESDI file commands are examples of some commands that may be passed to the drives using this host command.

- Initiate File Diagnostics
- Request Configuration
- Stop/Start Spindle Motor
- Offset Data Strobe
- Offset Track.

For further information refer to *Enhanced Small Device Interface Specification* revision F or later.

Diagnose

This command causes the adapter to execute its self test code and return the results to the error register. An interrupt is generated at the completion of this command.

Write Data Buffer

Upon receiving this command, the adapter sets up a 16K-byte buffer. When busy is off and data request is on, the system writes to this buffer. Command completion will not generate a completion interrupt. All 16K-bytes must be written before issuing another command. This is primarily a diagnostic command.

Read Data Buffer

Upon receiving this command, the adapter sets up a 16K-byte buffer. When busy is off and data request is on, the system reads this buffer. Command completion will not generate a completion interrupt. All 16K-bytes must be read before issuing another command. This is primarily a diagnostic command.

Set Parameters

This command sets up the drive parameters (maximum number of heads and sectors per track). The drive/head register specifies the drive affected. The sector count and drive/head registers must be set up before this command is issued. The adapter uses the values specified for track and cylinder crossing during multisector operations. An interrupt is not generated at the completion of this command. This command must be issued before any multisector operations are attempted.

Mode Control Register

This register switches the adapter between the PIO and DMA mode. In DMA mode, this register also selects the DMA burst length.

Bit 3	Bit 2	Bit 1	Bit 0	Definition
X	0	0	0	PIO Mode Normal
X	X	1	0	PIO Mode Reserved
X	1	X	0	PIO Mode Reserved
0	0	0	1	DMA Mode

See "Fixed-Disk DMA Mode" on page 13 for definition of DMA mode bits.

Fixed Disk Register

The fixed disk register is an eight-bit write only register whose bits are defined below.

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Reserved

Bit 4 Reserved

Bit 3 Alternate DMA channel—When bit 3 is set to 0, the fixed disk primary adapter uses DMA channel 0 and the secondary adapter uses DMA channel 3. When this bit is set to 1, the adapter uses DMA channel 1.

Bit 2 Reset adapter—When bit 2 is set to 0, the adapter is reset and the adapter is set to PIO mode.

Bit 1 Enable hard file interrupts—When bit is 1 set to 0, hard file interrupts are enabled.

Bit 0 Alternate interrupt level

0 = Fixed disk uses interrupt sharing on level 14
1 = Fixed disk uses interrupt sharing on level 12.

Interrupt Status Register

This eight-bit register is used to interrupt status of the fixed disk and the diskette.

Bit 7 Fixed disk interrupt

Bit 6 Diskette interrupt

Bits 5 - 0 Reserved

Reset and Initial Power On

Applying a pulse to the + Reset line, or toggling the Reset bit in the fixed disk register resets the adapter and enables interrupts on level 14. All registers are set to zero except for the following:

- Error register
- Drive/Head Register (X'A0')

The adapter is put into diagnostic mode and the self diagnostics are run.

If a Write operation is in progress when the Reset occurs, bad data may be written onto the file.

Fixed-Disk DMA Mode

In DMA Mode commands and status are transferred by PIO operations, but data is transferred by alternate controller DMA. The commands are written into a command stack and a command register. Adapter status is read from the status register. Setting bit 0 of the mode control register to 1 places the adapter in DMA mode. The burst length must also be set.

In DMA mode the adapter has a two element command queue for each of three files plus a buffer queue. A command can be sent to the adapter whenever the busy bit is off. The adapter interrupts the host when a command completes.

Status and Command Registers

The addresses of the DMA status and command registers are shown in the following table. The mode control register and the fixed disk register are the same in DMA and PIO modes.

DMA Mode Address			
Primary	**Secondary**	**Read**	**Write**
03F6	0376	Interrupt status	Fixed disk register
05F0	0570	Error A register	Command stack
05F3	0573	Mode control register	Mode control register
05F4	0574	Error B register	Reserved
05F6	0576	Status register	Command register

DMA Status Register

The DMA status register is a 16 bit register that the system uses to sense the adapter status.

Bit 15 Busy bit—The busy bit is set by a write to the command register and is reset when the adapter can accept another command. All writes to the command register, command stack, and the mode control register are ignored when this bit is set.

Bit 14 Status Valid—This bit indicates valid status in the status and error registers. This bit is reset when the system does an 8 bit read on the low byte of the status register (5F6 or 576). If disk interrupts are enabled then this bit also controls interrupts.

Bit 13 Corrected Data—This bit is set whenever the adapter has corrected a hard error in a read or read verify with retries on.

Bit 12 Reserved

Bit 11 Reserved

Bits 10 - 8 File Queue Position—These 3 bits define which file queue position the status is for:

000	File 0 queue A
001	File 0 queue B
010	File 1 queue A
011	File 1 queue B
100	File 2 queue A
101	File 2 queue B
110	Buffer transfer queue A
111	Buffer transfer queue B

Bits 7 - 0 Error code—The error type reported is encoded in an 8 bit error code. The following is a summary of the error codes returned.

Error Code (hex)	**Definition**
00	No error detected (command completed)
01	No data address mark
02	Track 0 error
04	Aborted command
08	Adapter error
10	ID not found
20	Write fault error
40	Uncorrectable data ECC error
80	Bad block detected
C0	Bad block detected alternate
21	Write parity error
24	Invalid command

Command Register

The command register is a 16-bit register containing the command and file queue. Writing to the command register sets the busy bit and resets the adapter command stack pointer for the next command.

DMA mode supports the following commands.

Command	Bits 15 - 8	Bits 7 - 0
Read File	0 0 1 0 T 0 0 R	0 0 0 0 0 F F F
Write File	0 0 1 1 0 0 0 R	0 0 0 0 0 F F F
Read Verify	0 1 0 0 0 0 0 R	0 0 0 0 0 F F F
Read Buffer	0 1 1 1 0 0 0 1	0 0 0 0 0 1 1 Q
Write Buffer	0 1 1 1 0 0 1 0	0 0 0 0 0 1 1 Q
Restore	0 0 0 1 0 0 0 0	0 0 0 0 0 F F F
Shutdown	1 1 1 1 0 0 0 0	0 0 0 0 0 0 0 0

Figure 5. Valid Command-Register Commands

The following figure shows the bit definitions for bits T, R and Q.

Bit	Bit = 0	Bit = 1
T	Transfer to system	Transfer to buffer
R	Retries enabled	Retries disabled
Q	Buffer transfer queue A	Buffer transfer queue B

Figure 6. T, R and Q Bit Definitions

The following table shows the bit definitions for bits FFF.

FFF	File and Queue Position
000	File queue 0 position A
001	File queue 0 position B
010	File queue 1 position A
011	File queue 1 position B
100	File queue 2 position A
101	File queue 2 position B
110	Reserved
111	Reserved

Command Stack

The command stack is a 10 byte stack organized 16 bits wide by 5 deep. All writes to the stack must be 16 bits wide. Command parameters must be written to the command stack before the command is written to the command register. Writing to the command register resets the adapter stack pointer for the next command.

Error A Register

This 16-bit register is used for error reporting. If the error was a bad command error this register contains the rejected command. If the error was a file error this register contains the head and sector that had an error.

Error B Register

This 16 bit register is used for reporting file errors. If there was a file error this register contains the cylinder that had an error.

Interrupt Status register

This 8 bit register is used to interrupt status of the fixed disk and the diskette.

Bit 7 Fixed disk interrupt

Bit 6 Diskette interrupt

Bits 5 - 0 Reserved

Mode Control Register

This register switches the adapter between PIO and DMA mode. In DMA mode this register also selects the DMA burst length. This register is set to 0 at power on time. For normal AIX/RT PC system operation it is recommended that the DMA burst length not be set to more than 16 bytes.

Bit 3	Bit 2	Bit 1	Bit 0	Definition
X	0	0	0	PIO Mode Normal
X	X	1	0	PIO Mode Reserved
X	1	X	0	PIO Mode Reserved
0	0	0	1	DMA Mode - 4 Byte Burst
0	0	1	1	DMA Mode - 8 Byte Burst
0	1	0	1	DMA Mode - 16 Byte Burst
0	1	1	1	DMA Mode - 32 Byte Burst
1	0	0	1	DMA Mode - 64 Byte Burst
1	0	1	1	DMA Mode - 128 Byte Burst
1	1	0	1	DMA Mode - 256 Byte Burst
1	1	1	1	DMA Mode - 512 Byte Burst

Fixed Disk Register

The fixed disk register is an 8-bit write-only register whose bits are defined as follows:

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Reserved

Bit 4 Reserved

Bit 3 Alternate DMA channel—When bit 3 is set to 0, the fixed disk primary adapter uses DMA channel 0 and the secondary adapter uses DMA channel 3. When this bit is set to 1, the adapter uses DMA channel 1.

Bit 2 Reset adapter—When bit 2 is set to 0, the adapter is reset and set to PIO mode.

Bit 1 Enable hard file interrupts—When bit 1 set to 0, interrupt level 14 is enabled.

Bit 0 Alternate interrupt level

0 = Fixed disk uses interrupt sharing on level 14
1 = Fixed disk uses interrupt sharing on level 12.

Command Protocol

Initial Adapter Setup

After the initial power on sequence, the adapter is in PIO mode. To switch to DMA mode the host sets the mode control register to DMA mode with the desired burst length. The host must then wait 100ms before sending any commands. After this operation, all data transfers from the files are done in DMA mode. Resetting the DMA mode register to zero, or a Shutdown command will put the adapter in PIO mode.

Normal Command Execution

Whenever the busy bit is off, the host may issue a new command. To do this, the host sends DMA command parameters to the DMA command stack and then loads the DMA command op-code and file queue position into the DMA command register. The adapter empties the command block area and clears the busy bit that was set by the write to the command register. The adapter interrupts the host when a command has completed. This provides a method of issuing new commands to the adapter during time periods when the adapter is transferring data to or from the host using DMA, as well as at all other times.

As explained in the command queuing section below, two commands, A and B can be entered into each queue. The host must never send a new command to position A (or B) of any queue until the previous
A (or B) command has completed for that queue. Up to two commands can be queued for each drive by sending commands A and B to each of the four queues, with each queue being used for a single file.

Command Queuing

After issuing a command to a file by filling the DMA command block stock and issuing a command to queue position 1 A (or B), another command can be issued to the same file before the first command is completed. This is done by waiting for the busy bit to be turned off and issuing a new command block for the same file to queue position 1 B (or A).

The adapter continues with the first command and interrupts the host when it is complete. The adapter will then automatically continue with the next command. After the host has responded to the first interrupt for that queue, it can then issue another command to the file by sending a new command with a target of the same file or path combination as the command just completed.

Up to two commands can be queued for each fixed disk by issuing four pairs of A and B commands, with each queue used for a single file.

Command Queue Execution Order

If commands have been sent by the host to more than one queue before the first command completes, the order of execution of queued commands is as follows:

- When the queues are empty, the adapter begins by accessing the queue which is addressed by the first command received.
- When this command completes, the other command (such as, the A or B command) for the same queue is executed if it has been sent by the host.
- After this command completes, the adapter continues to execute all commands in the same queue until it completes all commands which the host has sent for that queue (that is, as long as the host continues alternately sending Commands A and B to a queue the adapter continues executing these commands alternately until the host stops sending them).
- After completing all commands for a particular queue and finding no more available, the adapter executes commands for the next queue.
- It will then continue executing commands for that queue until no more are available.
- Finally, it will execute all commands for the third queue before checking the first queue again.
- To summarize, the order of execution of commands can be seen as a ring from queue 0 to queue 1 to queue 2 with an indefinite number of operations performed on queue before moving to queue n + 1.

For commands which require seek operations at the start, the seek command is issued to the addressed file, and the A or B command for the next queue is examined. If there is a command that does not require a seek or has completed a seek, then it is executed while the seek operation for the previous queue is occurring. If all files have seek operations in progress, the adapter executes the command for the queue whose seek operation completes first, and continues executing the commands for that queue until the queue is empty.

When the adapter is waiting seeks to complete before starting commands it will start DMA transfers for Write commands, Read Buffer commands, and Write Buffer commands.

When the adapter is executing commands in a file queue, Read buffer and Write buffer commands are started under the following condition:

- The adapter is doing a seek in a read command.
- The command is a Read File to Buffer command.
- The command is a Read Verify command.
- The adapter has finished the DMA data transfer for a write command and there is no other Write DMA data to be transferred.

DMA Command Register

The DMA command register is a 16-bit register that is written to by the host to notify the adapter that a command has been sent. Writing to this register sets the busy bit in the status register and resets the command stack pointer for the the next command. This register should be written after any command stack parameters are written. This register can only be written when the busy bit is off.

DMA Command Stack

The DMA command stack is a 10-byte stack that is used on any command that is more than two bytes long. The host can write to the stack using 16-bit writes or 32-bit writes. The command stack pointer (a counter on the adapter) is reset to the stack beginning by a write to the DMA command register. The command stack can only be written when the busy bit is off.

DMA Commands

In DMA mode the adapter executes the following commands: Read File Read Buffer Read Verify Write File Restore Shutdown.

The host issues a command to the adapter by loading all of the command parameters into the command stack and then writing into the command register. The adapter interrupts the host when each command has completed.

Read File

This command reads 1 to 4 sectors from the file to the command buffer location. The read starts at the cylinder, head, and sector in the command. If the transfer bit is on, the adapter will DMA the data to the host starting at the address specified in the command. If the retries are enabled, the adapter attempts to recover from error conditions before reporting an error. (Refer to "Error Recovery" on page 24 for error recovery procedures.) The adapter interrupts and returns status to the host when this command is complete.

Stack	Bits 15 - 8	Bits 7 - 0
Stack 0	Cylinder Low	Cylinder High
Stack 1	Sector Address	Head Address
Stack 2	Buffer Address	Sector Count
Stack 3	DMA Address 17-23	X X X X X X X X

Stack	Bits 15 - 8	Bits 7 - 0
Stack 4	DMA Address 1-8	DMA Address 9-16

Write File

This command writes 1 to 4 sectors from the host to the file. The buffer location contained in the command will be used. The write starts at the cylinder, head, and sector in the command. The adapter will DMA the data from the host starting at the address specified in the command. If the retries are enabled the adapter attempts to recover from error conditions before reporting an error. (See "Error Recovery" on page 24 for error recovery procedures.) The adapter interrupts and returns status to the host when this command is complete.

Stack	Bits 15 - 8	Bits 7 - 0
Stack 0	Cylinder Low	Cylinder High
Stack 1	Sector Address	Head Address
Stack 2	Buffer Address	Sector Count
Stack 3	DMA Address 17-23	X X X X X X X X
Stack 4	DMA Address 1-8	DMA Address 9-16

Read Verify

This command reads 1 to 4 sectors from the file and verifies that the data is valid. No data is transferred to the buffer or to the system. The read starts at the cylinder, head, and sector in the command. If retries are enabled, the adapter attempts to recover from error conditions before reporting an error. (See "Error Recovery" on page 24 for error recovery procedures.) The adapter interrupts and returns status to the host when this command is complete.

Stack	Bits 15 - 8	Bits 7 - 0
Stack 0	Cylinder Low	Cylinder High
Stack 1	Sector Address	Head Address
Stack 2	Buffer Address	Sector Count

Read Buffer

This command transfers 1 to 32 sectors from the buffer location contained in the command to host. The adapter will DMA the data to the host starting at the address specified in the command. The adapter interrupts and returns status to the host when this command is complete.

Stack	Bits 15 - 8	Bits 7 - 0
Stack 0	X X X X X X X X	X X X X X X X X
Stack 1	X X X X X X X X	X X X X X X X X
Stack 2	Buffer Address	Sector Count
Stack 3	DMA Address 17-23	X X X X X X X X
Stack 4	DMA Address 1-8	DMA Address 9-16

Write Buffer

This command transfers 1 to 32 sectors to the buffer location contained in the command to host. The adapter will DMA the data from the host starting at the address specified in the command. The adapter interrupts and returns status to the host when this command is complete.

Stack	Bits 15 - 8	Bits 7 - 0
Stack 0	X X X X X X X X	X X X X X X X X
Stack 1	X X X X X X X X	X X X X X X X X
Stack 2	Buffer Address	Sector Count
Stack 3	DMA Address 17-23	X X X X X X X X
Stack 4	DMA Address 1-8	DMA Address 9-16

Restore

The Restore command issues a seek to track zero on the specified file. If there is a seek error the adapter issues the seek up to five more times. If an error still remains, a recalibrate command will be sent. An interrupt and status is returned to the system when the command is completed.

Shutdown

The Shutdown command halts all commands at a sector boundary and then:

- Flushes all queues
- Returns the adapter to PIO mode
- Starts a diagnose command.

This command is used at early power off warning and at soft Initial Program Load (IPL) times. An interrupt is returned when the diagnose command completes.

Note: The data buffers are managed by the system. The adapter starts the data buffer where it is told and wraps from the last buffer to the first if that is required.

Error Recovery

Bad Block ID

All IDs that have good ECC are checked for a bad block flag (bit 7 in the head ID field). If there is a bad block flag, then the cylinder, head, and sector of the ID is compared to the cylinder, head, and sector of the ID being searched for. If the IDs are the same, then the read or write operation is stopped and a bad block error is returned.

ID Not Found

The adapter searches for the ID for two times the number of sectors per track (this value is set by a set parameter command). If the ID is not found and retries are disabled, then the read or write is stopped and an ID not found error is returned.

If retries are enabled for a write, the adapter searches for the ID for eight times the number of sectors per track. For a read, the adapter searches 40 times the number of sectors per track using offsets. During this search the IDs are checked for the correct cylinder value. If the cylinder value is not correct, the adapter tries to seek to the correct cylinder up to three times. If the correct ID is not found in the retries, an ID not found is returned.

Read Data Errors

If the adapter finds a data field with bad ECC or a data address mark error and retries are disabled the read is stopped and an uncorrectable ECC error or a data address mark error is returned.

If retries are enabled then the following retries will be attempted to read correct data.

8 retries with Track offset = 0 and Data Strobe offset = 0
8 retries with Track offset = + 1 and Data Strobe offset = 0
8 retries with Track offset = − 1 and Data Strobe offset = 0
8 retries with Track offset = 0 and Data Strobe offset = + 1
8 retries with Track offset = 0 and Data Strobe offset = − 1

If these retries fail, an additional eight retries are attempted with track and data offsets set to 0. The adapter attempts to find two consecutive syndromes that match. If the syndromes match and the data is correctable, the adapter corrects the data and returns a corrected data flag with the data. If the data is uncorrectable or no two consecutive syndromes match, the adapter stops the read and returns an uncorrectable error.

Write Fault Errors

If a write fault is detected, the adapter attempts to clear the fault condition. With retries enabled, the adapter attempts to write the sector seven more times before stopping the write and returning a write fault error. If retries are disabled, the adapter stops the write on the first error and return a write fault error.

ESDI Command Errors

If a PIO ESDI command, PIO Seek command, implied Seek (PIO or DMA mode), or a device Recalibrate command (issued during execution of the adapter Restore command) is sent to the file, the adapter will check for a device error only once, immediately after sending the command. If a parity error or interface error is detected at this time, the adapter will try to resend the command up to two more times. If the two retries fail, the adapter will clear busy and return an terminated command interrupt.

If, however, the device returns an error at a later time, the adapter will not report an error and the next command must handle the device attention.

If attention is detected at the start of a command, the adapter issues ESDI commands to read the file status and to reset attention. If the error returned is a write gate with offset, then a track offset = 0 command and a data strobe offset = 0 command will be sent. If the error returned is motor off, then a start motor command will be issued. If these commands are not able to clear attention, an aborted command is returned.

If an invalid head or cylinder is selected, the adapter will set attention and cause all commands to be aborted until a valid head and cylinder are selected.

DMA Parity Error

If the I/O CH CK line goes low while the adapter has control of the bus during a DMA transfer, the adapter will terminate the command and return a DMA parity error (X'21') in the low byte of the status register. If the command that was terminated was a read or write to the file, the adapter will also abort any other command on that file queue.

File Data Format

The Extended ESDI Adapter works with hard sectored ESDI drives that have unformatted sectors of 575 bytes or more. The adapter formats and uses the sectors as follows.

Format

The adapter writes hex '00' data for one revolution of the file. The file then writes each sector as follows:

Index or Sector pulse	
Write gate on	
12 bytes	'00' PLL sync
1 byte	'FE' ID sync
4 bytes	ID
4 bytes	ID CRC
3 bytes	'00' write pad
Write gate off	
1 byte	Write splice
Write gate on	
12 bytes	'00' PLL sync
1 byte	'FE' data sync
512 bytes	'00' data
4 bytes	Data ECC
3 bytes	'00' write pad
Write gate off	

Read

Index or Sector pulse	
Read gate on	
6 bytes	'XX' PLL sync minimum
1 byte	'FE' ID sync
4 bytes	ID
4 bytes	ID CRC
Read gate off	
4 bytes	Write splice
Read gate on	
6 bytes	'XX' PLL sync minimum
1 byte	'FE' data sync
512 bytes	Data
4 bytes	Data ECC
Read gate off	

Write

Index or Sector pulse	
Read gate on	
6 bytes	'XX' PLL sync minimum
1 byte	'FE' ID sync
4 bytes	ID
4 bytes	ID CRC
Read gate off	
1 byte	Write splice
Write gate on	
12 bytes	'00' PLL sync
1 byte	'FE' data sync
512 bytes	Data
4 bytes	Data ECC
3 bytes	'00' write pad
Write gate off	

ID Format

The ID field has the following format:

Byte 1 0 0 0 0 C11 C10 C9 C8

Byte 2 C7 C6 C5 C4 C3 C2 C1 C0

Byte 3 BB BH 0 0 H3 H2 H1 H0

Byte 4 S7 S6 S5 S4 S3 S2 S1 S0

C0-C11	12-bit cylinder address	
H0-H3	4-bit head address	
S0-S7	8-bit sector address	
BB	Bad block flag	1 = bad block 0 = good block
BH	Hidden bad block flag	1 = hidden 0 = relocated

CRC/ECC Polynomial

The polynomial used for both ID CRC and DATA ECC is
X30 + X24 + X18 + X14 + X8 + X7 + X2 + 1. The polynomial is preloaded with '0's and the sync byte is included.

Diskette Function

One or two diskette drives are attached to the adapter through an internal, daisy-chained, flat cable. The attachment supports 360K- and 1.2M-byte diskette drives.

The adapter is designed for a double-density, MFM-coded, diskette drive and uses write precompensation with an analog circuit for clock and data recovery. The diskette-drive parameters are programmable, and the diskette drive write-protect feature is supported. The adapter is buffered on the I/O channel and uses the system board direct memory access (DMA) for record data transfers. An interrupt level 6 indicates when an operation is complete or when a status condition requires microprocessor attention. Interrupt level 6 does not support interrupt sharing.

The diskette address registers are shown below.

I/O Address			
Primary	**Secondary**	**Read**	**Write**
03F2	0372	Reserved	Digital output register
03F4	0374	Main status register	
03F5	0375	Diskette data register	Diskette data register
03F7	0377	Digital input register	Diskette control register

Digital Output Register

The digital output register (DOR) is a write-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions follow:

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Drive B Motor Enable (Active high)

Bit 4 Drive A Motor Enable (Active high)

Bit 3 Enable Diskette Interrupts and DMA (Active high)

Bit 2 Diskette Function Reset (Active low)

Bit 1 Reserved

Bit 0 Drive Select—A 0 on this bit indicates that drive A is selected.

Drive Select—A 1 on this bit indicates that drive B is selected.

Note: A channel reset clears all bits.

Digital Input Register

The digital input register is an 8-bit, read-only register used for diagnostic purposes. All bits are active high. The following are bit definitions for this register:

Bit 7 Diskette Change

Bit 6 Head Select 3

Bit 5 Head Select 2

Bit 4 Head Select 1

Bit 3 Head Select 0

Bit 2 Drive Select 1

Bit 1 Drive Select 2

Bit 0 Drive Select 3.

Note: Bits 0 through 6 apply to the currently selected fixed-disk drive.

Diskette Control Register

Bits 7 - 2 Reserved.

Bits 1 - 0 Selects read/write data rate.

00	500K-bps
01	300K-bps
10	250K-bps
11	Reserved

The 300K- and 500K-bps incoming data pulse widths will be those associated with a 500K-bps data signal.

Diskette Controller

The diskette controller has two registers
to which the main system processor has access: a status register and a data register. The 8-bit status register has the status information about the diskette and may be accessed at any time. The 8-bit data register (hex 3F5), which actually consists of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, and parameters, and provides diskette-drive status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command.

Main Status Register

The main status register may only be read and is used to facilitate the transfer of data between the processor and diskette controller.
The bits in the main status register (hex 3F4) are active high and are defined as follows:

Bit 7 Request for Master (RQM)— The data register is ready to send or receive data to or from the processor.

Bit 6 Data Input/Output (DIO)—The direction of data transfer between the diskette controller and the processor. If this bit is a 1, transfer is from the diskette controller data register to the processor; if it is a 0, the opposite is true.

Bit 5 Non-DMA Mode (NDM)—The diskette controller is in the non-DMA mode.

Bit 4 Diskette Controller Busy (CB)— A Read or Write command is being executed.

Bit 3 Reserved.

Bit 2 Reserved.

Bit 1 Diskette Drive B Busy (DBB)— Diskette drive B is in the seek mode.

Bit 0 Diskette Drive A Busy (DAB)— Diskette drive A is in the seek mode.

Diskette Command Phases

The diskette controller can perform 7 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the diskette controller and the processor, each command can be considered to consist of three phases:

Command Phase

The processor issues a sequence of Write commands to the diskette controller that direct the controller to perform a specific operation.

Execution Phase

The diskette controller performs the specified operation.

Result Phase

After completion of the operation, status and other housekeeping information is made available to the processor through a sequence of Read commands to the processor. An interrupt (level 6) occurs at the beginning of the result phase.

During command or result phases the main status register must be read by the processor before each byte of information is written or read from the data register. Bits 6 and 7 in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word can be written into the data register.

Diskette Controller Commands

The following is a list of commands that may be issued to the diskette controller:

- **Read Data**
- **Format a Track**
- **Recalibrate**
- **Sense Interrupt Status**
- **Specify**
- **Seek**

Symbol Descriptions

The following are descriptions of the symbols used in the Command Definitions later in this section:

A0	Address Line 0—A 0 selects the main status register, and a 1 selects the data register.
C	Cylinder Number—Contains the current or selected cylinder number in binary notation.
D	Data—Contains the data pattern to be written to a sector.
D7-D0	Data Bus—An 8-bit data bus in which D7 is the most-significant bit and D0 is the least- significant.
DTL	Data Length—When N is 00, DTL is the data length read from or written to a sector.
EOT	End of Track—The final sector number on a cylinder.
GPL	Gap Length—The length of gap 3 (spacing between sectors excluding the VCO synchronous field).

H Head Address—The head number, either 0 or 1, as specified in the ID field.

HD Head—The selected head number, 0 or 1. (H = HD in all command words.)

HLT Head Load Time—The head load time in the selected drive (2 to 256 milliseconds in 2-millisecond increments for the 1.2M-byte drive and 4 to 512 milliseconds in 4-millisecond increments for the 320K-byte drive).

HUT Head Unload Time—The head unload time after a read or write operation (0 to 240 milliseconds in 16-millisecond increments for the 1.2M-byte drive and 0 to 480 milliseconds in 32-millisecond increments for the 320K-byte drive).

MF MFM Mode—A 0 is reserved and a 1 selects MFM.

MT Multitrack—A 1 selects multitrack operation. (Both HD0 and HD1 will be read or written.)

N Number—The number of data bytes written in a sector. Number of bytes = 128 x 2 * N.

NCN New Cylinder—The new cylinder number for a seek operation

ND No-Data—This indicates no data in status register 0.

PCN Present Cylinder Number—The cylinder number at the completion of a Sense interrupt status command (present position of the head).

R Record—The sector number to be read or written.

R/W Read/Write—This stands for either a 'read' or 'write' signal.

SC Sector—The number of sectors per cylinder.

SK Skip—This stands for skip deleted-data address mark.

SRT This 4 bit byte indicates the stepping rate for the diskette drive as follows:

1.2M-Byte Diskette Drive
1111 1 millisecond
1110 2 milliseconds
1101 3 milliseconds

320K-Byte Diskette Drive
1111 2 milliseconds
1110 4 milliseconds
1101 6 milliseconds

ST 0—ST 1 Status 0—Status 3—One of the four registers that stores status information after a command is executed.

US0 Drive A selected.

US1 Drive B selected.

Controller Commands

The following are commands that may be issued to the controller:

Note: An X is used to indicate a do not care condition.

Read Data

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	MT MF SK 0 0 1 1 0
Byte 1	X X X X X HD US1 US0
Byte 2	Cylinder Number
Byte 3	Head Address
Byte 4	Record
Byte 5	Number
Byte 6	End of Track
Byte 7	Gap Length
Byte 8	Data Length

Result Phase

The following bytes are issued by the controller in the result phase:

Byte	**Bits 7 - 0**
Byte 0	Status 0
Byte 1	Status 1
Byte 2	Status 2
Byte 3	Cylinder Number
Byte 4	Head Address
Byte 5	Record
Byte 6	Number

Format a Track

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	**Bits 7 - 0**
Byte 0	0 MF 0 0 1 1 0 1
Byte 1	X X X X X HD US1 US0
Byte 2	Number
Byte 3	Sector
Byte 4	Gap Length
Byte 5	Data

Result Phase

The following bytes are issued by the controller in the result phase:

Byte	**Bits 7 - 0**
Byte 0	Status 0
Byte 1	Status 1
Byte 2	Status 2
Byte 3	Cylinder Number
Byte 4	Head Address
Byte 5	Record
Byte 6	Number

Recalibrate

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 0 1 1 1
Byte 1	X X X X X 0 US1 US0

Result Phase

This command has no result phase.

Sense Interrupt Status

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 1 0 0 0

Result Phase

The following bytes are issued by the controller in the result phase:

Byte	Bits 7 - 0
Byte 0	Status 0
Byte 1	Present Cylinder Number

Specify

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 0 0 1 1
Byte 1	(SRT)(HUT)
Byte 2	(HLT) ND.

Result Phase

This command has no result phase.

Seek

Command Phase

The following bytes are issued by the processor in the command phase:

Byte	Bits 7 - 0
Byte 0	0 0 0 0 1 1 1 1
Byte 1	X X X X X HD US1 US0
Byte 2	New Cylinder

Result Phase

This command has no result phase.

Command Status Registers

The following is information about the command status registers ST0 through ST3. All bits are active high.

Command Status Register 0 (ST0)

The following are bit definitions for command status register 0:

Bit 7–Bit 6 Interrupt Code (IC)

- **00** Normal Termination of Command (NT)—The command was completed and properly executed.
- **01** Abrupt Termination of Command (AT)—The execution of the command was started but not successfully completed.
- **10** Invalid Command Issue (IC)—The issued command was never started.
- **11** Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.

Bit 5 Seek End (SE)—Set to 1 when the controller completes the Seek command.

Bit 4 Equipment Check (EC)—Set if a 'fault' signal is received from the diskette drive, or if the 'track–0' signal fails to occur after 77 step pulses (Recalibrate Command).

Bit 3 Not Ready (NR)—This flag is set when the diskette drive is in the not-ready state and a Read or Write command is issued. It is also set if a Read or Write command is issued to side 1 of a single-sided diskette drive.

Bit 2 Head Address (HD)—Indicates the state of the head at interrupt.

Bit 1 Unit select 2 (US 2)—Indicates drive B at interrupt.

Bit 0 Unit select 1 (US 1) —Indicates drive A at interrupt.

Command Status Register 1 (ST1)

The following are bit definitions for command status register 1:

Bit 7 End of Cylinder (EC)—Set when the controller tries to gain access to a sector beyond the final sector of a cylinder.

Bit 6 Not Used—Always 0.

Bit 5 Data Error (DE)—Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 Overrun (OR)—Set if the controller is not serviced by the main system within a certain time limit during data transfers. The time limits are 11 microseconds for the 500K-bps data rate, 17.5 microseconds for the 300K-bps, and 24 microseconds for the 250K-bps data rate.

Bit 3 Not Used—This bit is always set to 0.

Bit 2 No Data (ND)—Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan Command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or, if the starting sector cannot be found during the execution of a Read Cylinder command.

Bit 1 Not Writable (NW)—Set if the controller detects a 'write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.

Bit 0 Missing Address Mark (MA)—Set if the controller cannot detect the ID address mark. At the same time, the MD of status register 2 is set.

Command Status Register 2 (ST2)

The following are bit definitions for command status register 2:

Bit 7 Not Used—Always 0.

Bit 6 Control Mark (CM)—This flag is set if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.

Bit 5 Data Error in Data Field (DD)—Set if the controller detects an error in the data.

Bit 4 Wrong Cylinder (WC)—This flag is related to ND (no data) and when the contents of C on the medium are different from that stored in the ID register, this flag is set.

Bit 3 Reserved

Bit 2 Reserved

Bit 1 Bad Cylinder (BC)—Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set.

Bit 0 Missing Address Mark in Data Field (MD)— Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

Command Status Register 3 (ST3)

The following are bit definitions for command status register 3:

Bit 7 Fault (FT)—Status of the 'fault' signal from the diskette drive.

Bit 6 Write Protect (WP)—Status of the 'write-protect' signal from the diskette drive.

Bit 5 Ready (RY)—Status of the 'ready' signal from the diskette drive.

Bit 4 Track 0 (T0)—Status of the 'track 0' signal from the diskette drive.

Bit 3 Two Side (TS)—Status of the 'two side' signal from the diskette drive.

Bit 2 Head Address (HD)—Status of the 'side-select' signal from the diskette drive.

Bit 1 Unit Select 1 (US 1)—Status of the 'unit-select-1' signal from the diskette drive.

Bit 0 Unit Select 0 (US 0)—Status of the 'unit select 0' signal from the diskette drive.

Interfaces

The system interface is through the I/O channel. The address, DMA, and interrupt assignments are shown in the following figures:

I/O Address			
Primary	**Secondary**	**Read**	**Write**
03F2	0372	Reserved	Digital output register
03F4	0374	Main status register	
03F5	0375	Diskette data register	Diskette data register
03F7	0377	Digital input register	Diskette control register

Figure 7. Diskette Function

Note: DMA request is on level 2. The diskette uses interrupt level 6 and does not support interrupt sharing.

PIO Mode Address			
Primary	**Secondary**	**Read**	**Write**
01F0	0170	Data register	Data register
01F1	0171	Error register	Not used
01F2	0172	Sector count	Sector count
01F3	0173	Sector number	Sector number
01F4	0174	Cylinder low	Cylinder low
01F5	0175	Cylinder high	Cylinder high
01F6	0176	Drive/head register	Drive/head register
01F7	0177	Status register	Command register
03F6	0376	Interrupt status	Fixed-disk register
05F3	0573	Mode control register	Mode control register

Figure 8. Fixed Disk Function

DMA Mode Address			
Primary	**Secondary**	**Read**	**Write**
03F6	0376	Interrupt status	Fixed disk register
05F0	0570	Error A register	Command stack
05F3	0573	Mode control register	Mode control register
05F4	0574	Error B register	Reserved
05F6	0576	Status register	Command register

Figure 9. Fixed Disk Function

Note: Interrupt request is level 12 or level 14. Both levels are shared interrupts. DMA channels 0, 1, or 3 are supported.

The following operations are supported by this adapter:

- Sixteen bit programmed I/O (PIO) data transfers to the fixed disk. All other transfers must be 8 bits wide.
- The I/O addresses are selected by a jumper on J6. P is for primary and S is for secondary.

Miscellaneous Information

- The diskette interface signal - WC Control is the logical inverse of Bit 0, that is, when 300K-bps is selected the - WC CONTROL is active.
- The attachment must support up to 80 tracks and up to fifteen 512-byte sectors per track.
- The table below details the relationship between the data rate and the diskette adapter clocks.

Data Rate	Clock Frequency	Data Encoding	Write Precompensation
250K bps	4.0 MHz	MFM	250 ns.
300K bps	4.8 MHz	MFM	208.3 ns.
500K bps	8.0 MHz	MFM	125 ns.

- When changing data rates the minimum high and low clock times (40 ns) for the NEC 765 (or equivalent) must not be violated.

Interface Lines

The interface to the fixed disk drive consists of two cables: 'control' and 'data'. One common control cable is used for all drives. A separate data cable is used for each drive. The following figures show signals and pin assignments for these cables:

Signal Name	Signal Pin	Gnd Pin
- Head Select 3	2	1
- Head Select 2	4	3
- Write Gate	6	5
- Configuration/Status Data	8	7
- Transfer Acknowledge	10	9
- Attention	12	11
- Head Select 0	14	13
- Sector	16	-
- Head Select 1	18	17
- Index	20	19
- Ready	22	21
- Transfer Request	24	23
- Drive Select 0	26	25
- Drive Select 1	28	27
- Drive Select 2	30	29
- Read Gate	32	31
- Command Data	34	33

Figure 10. Control Signal Lines (J1/P1)

Note: Connection is through a 2-by-17 Berg connector. Pin 15 is reserved to polarize the connector.

Signal Name	Signal Pin	Gnd Pin
- Drive Selected	1	
- Sector	2	
- Command Complete	3	
Reserved	4	
Polarizer	5	6
+ Write Clock	7	
- Write Clock	8	
Reserved	9	
+ Read/Reference Clock	10	
- Read/Reference Clock	11	12
+ NRZ Write Data	13	15
- NRZ Write Data	14	16.
+ NRZ Read Data	17	
- NRZ Read Data	18	19
- Index	20	

Figure 11. Data Transfer Signal Lines (J2/P2)

Note: Connection is through a 2-by-10 Berg connector. Pin 5 is reserved to polarize the connector.

The interface to the diskette drives is a single cable that carries both data and control signals. The signals and pin assignments are as follows:

Signal Name	Signal Pin	Gnd Pin
- Reduced Write	2	1
- Reserved	4	3
- Reserved	6	5
- Index	8	7
- Motor Enable Drive 1	10	9
- Drive Select 2	12	11
- Drive Select 1	14	13
- Motor Enable Drive 2	16	15
- Direction Select	18	17
- Step	20	19
- Write Data	22	21
- Write Gate	24	23
- Track 00	26	25
- Write Protect	28	27
- Read Data	30	29
- Side 1 Select	32	31
- Diskette Change	34	33

Figure 12. Control Signal Lines (J1/P1)

Note: Connection is through a 2-by-17 Berg connector. Pin 5 is reserved to polarize the connector.

IBM

Personal Computer Hardware Reference Library

SMALL COMPUTER SYSTEM INTERFACE (SCSI) ADAPTER

Small Computer System Interface (SCSI) Adapter

Contents

Description

The Small Computer System Interface (SCSI) Adapter connects to the system board using one of the I/O slots. This adapter board provides a host computer with the capability of controlling selected SCSI[1] devices by means of a 62-pin connector on the rear of the adapter. Connector pin definitions and details of the signal protocol used by this adapter are described in this manual.

The adapter uses 16 bit data transfers and acts as an alternate controller during Direct Memory Access (DMA) operations. All other transfers are 8- or 16-bit programmed input/output (PIO) transfers unless otherwise noted. The DMA channel used is selected by software.

The adapter interrupts on interrupt level 11 or 12. The interrupt level used is selected by software. Both interrupt levels are sharable.

The adapter operates when connected to a channel I/O slot. This channel is described in the "I/O Channel" section of the RT PC Technical Reference Manual. Diagnostic functions including an adapter self-test and wrap are also provided.

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[1] SCSI is used in this manual to represent Small Computer System Interface

Software Interface

Host Reset and Initial Power On

After a pulse to the RESET host bus pin, the host must write the value X'44' into the auxiliary register at 0D5C (095C) before the adapter can continue with its normal internal initialization process. At the completion of this process:

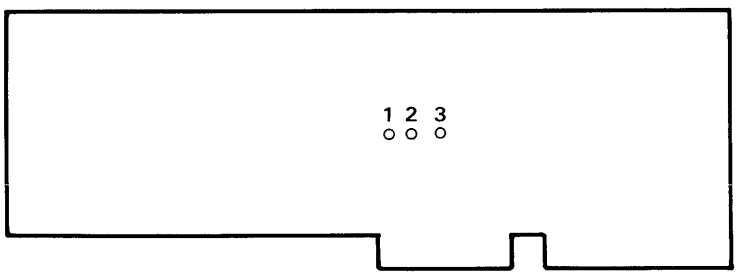
- The adapter Basic Assurance Tests (BATs) have been run
- The adapter hardware has been initialized
- The configuration register has been cleared
- The adapter is ready to report the result of the BATs.

All commands issued to the command register before the auxiliary register is written as described above will be ignored.

At the completion of the initialization process, the user must read the status registers for the BATs status. This causes the busy bit in the low byte of the status register to be turned off to allow adapter commands to be issued and normal operation to continue. See "Perform Basic Assurance Tests - BATs (Op code 4)" on page 13 for more information on clearing BATs status.

I/O Addresses

The SCSI adapter can be configured to respond to two sets of register addresses, primary and alternate, depending on the position of the jumper. Jumper insertion on pins 2 and 3 defines the alternate addresses.



These I/O addresses are defined in the table below:

I/O Address				
Primary	**Alternate**	**Read**	**Write**	**Length**
0D5E	095E	Status	Command	16 Bits
0D5C	095C	Auxiliary	Auxiliary	16 Bits
0D5B	095B	Reserved	DMA Mode	8 Bits
0D58	0958	Status Extension	Parameter Stack	16 Bits
0D52	0952	Configuration (12 Bits)	Configuration (8 Bits)	8/12 Bits

Figure 1. SCSI Adapter I/O Addresses

Register Definitions

The register definitions are defined with respect to I/O instructions on the IBM RT PC. Notice that during 16 bit I/O operations, a low for high byte swap occurs between the processor channel and the I/O channel. See the "I/O Channel" section in RT PC Technical Reference Manual for details.

Status Register

The status register returns command completion status. It is read after an interrupt occurs and before sending a new command (see bit 7). An 8-bit read operation to 0D5E/095E clears interrupts and allows subsequent interrupts to occur. Sixteen bit reads of 0D5E/095E or 8 bit reads of 0D5F/095F will not result in interrupts being cleared.

Bits 15-8 These bits contain the completion status codes for adapter operation as described in "Status Code Table" on page 31. For SCSI commands, these bits contain the SCSI status byte returned by the SCSI device.

Bit 7 This bit indicates that the adapter is busy processing commands and has not emptied the parameter stack. The host must not attempt any write operations to the command register or the parameter stack until this bit is a zero. This bit is set immediately after a write operation to the command register, and is cleared by the adapter as soon as it has emptied the stack. (Usually within 100 microseconds unless its unsent SCSI command staging area is full.)

Bit 6 When set to a one by the adapter, this bit indicates other bits in the register are valid. It is automatically reset by reading the 8 low order bits of this register, and all other bits are no longer valid until it is set once again by the adapter. An 8-bit read operation of the low order byte (address 0D5F/095F) or any 16 bit read operation will not clear this bit, and will not clear the interrupts.

Bit 5

1 = Status register bits 15-8 contain the SCSI command status
0 = Other completion status codes. See "Status Code Table" on page 31.

Bits 4-0 Command tag number originally passed by host with the command block. (Tag hex '1F' = unexpected condition, nonhost initiated operation.) See "Status Code Table" on page 31.

Command Register

The command register alerts the adapter that the parameter stack has been filled. It contains the operation code and other parameters defined below. A 16 bit write operation to this register sets the busy bit in the status register, and the host should not send another command block until the adapter empties the stack.

Note: Eight bit write operations to 0D5E/095E should not be done by the host, unpredictable results may occur if this is attempted.

Bits 15-12 These bits contain the adapter operation code for the command to be performed. See "Commands" on page 8 for a description of the operation codes.

Bits 11-8 Number of bytes of parameters in the SCSI command Block. (Used for the 'Send SCSI Command' operation only.)

Bits 7-5 Reserved

Bits 4-0 These bits assign an SCSI command tag number to the SCSI command block currently in the parameter stack. For op codes 0 and 1, only tags X'00' through X'0F' are allowed. Other op codes can also use tag X'10'. These bits are returned by the adapter in the status register upon SCSI command completion. (See the status register error code definitions in "Completion Status Codes" on page 27.)

Auxiliary Register

The auxiliary register contains additional status information which is sent to the host after certain adapter operations. The contents are defined in the command definitions.

DMA Mode Register

The DMA mode register defines the burst length used by the adapter hardware during DMA data transfers. It should be set up at initialization time.

Bit 7 Should be set to 0.

Bits 6-4 Reserved

Bits 3-1 The DMA burst size is encoded as follows:

Configuration Bits 3-1	DMA Burst Length
0 0 0	4 bytes
0 0 1	8 bytes
0 1 0	16 bytes
0 1 1	32 bytes
1 0 0	64 bytes
1 0 1	128 bytes
1 1 0	256 bytes
1 1 1	512 bytes

Bit 0 Must be set to 1.

For normal AIX/RT PC system operation it is recommended that the DMA burst length not be set to more than 8 bytes.

Status Extension Register

This status extension register contains additional status which the adapter can communicate to the host. Details can be found in "Completion Status Codes" on page 27.

Parameter Stack

This parameter stack is a 16-byte stack used by the host to pass SCSI commands and other information to the adapter. It must never be written into by the host without first checking the busy bit of the status register. It must only be written by a 16-bit output operations.

The parameter stack must be loaded by 16-bit write operations as follows:

16-Bit I/O Operation	I/O Instruction Bits 15-8	I/O Instruction Bits 7-0
1	Stack byte 0	Stack byte 1
2	Stack byte 2	Stack byte 3

Notice that when performing 16-bit I/O operations on the RT PC, a byte swap occurs between the processor channel and the I/O instruction.

Configuration Register

The configuration register sets up adapter parameters to be used during its operation. This register can only be addressed by 16 bit I/O operations. Bits 7-0 are read only.

Bits 15-13 DMA channel select bits are encoded as follows:

Bit 15	Bit 14	Bit 13	Channel
0	0	0	0
0	0	1	1
0	1	0	—
0	1	1	3
1	0	0	—
1	0	1	5
1	1	0	6
1	1	1	7

Note: Notice that DMA channels 2 and 4 will not be enabled even if selected.

Bit 12 DMA Enable. No DMA requests are issued to the system until this bit is set.

Bit 11 Reserved

Bit 10 Reserved

Bit 9 Interrupt Enable

Bit 8 Interrupt Level

0 = Interrupt level 11
1 = Interrupt level 12

Bits 7-4 Reserved

Bits 3-0 Read Only bits used for E.C. level of the adapter board. The initial level is E. C. level 15. Note that this is not the same as the firmware ROM (read only memory) E.C. level. Subsequent levels are sequentially numbered from zero.

Command Interface

Command Protocol

Whenever the adapter is not busy, the host may issue a new op code. To do so, the host fills the parameter stack. The host then loads the operation code and other information into the command register and is free to continue other processes. Another command may be sent as soon as the host detects that bit 7 in the status register has been cleared. All command transfers are accomplished with programmed I/O operations.

After the host has loaded the command register, the adapter empties the stack and command register, and clears the status register busy bit. The adapter can then accept another command from the host. The maximum number of unfinished commands which the adapter can store is 16. If the host attempts to send another command when the adapter already has 16 unfinished commands stored, it will not clear busy until it finishes one of its stored commands. This method of command transfer allows the host to issue new commands to the adapter while the adapter is transferring data or processing other host commands. It also allows the adapter to prevent the host from overloading it with too many commands when the SCSI bus and bus devices are busy processing multiple commands. If all 16 commands have been sent and the SCSI bus is hung with an error condition, diagnostic commands and the Clear Tag command can be sent by using tag X'10'. This clears the SCSI bus and allows recovery operations to proceed.

If the adapter command requires use of the SCSI bus, the adapter arbitrates for bus use and sends the SCSI command block which it received from the host via the command stack. It will process all routine SCSI messages which may be required for command completion without host involvement. (This includes responding to SCSI device requests, disconnections due to data accesses, storing buffer pointers, and obtaining the SCSI completion status byte.) When the SCSI device has completed the command and sent its status byte to the adapter, the adapter will:

- Fill bits 8-15 of the status register with the SCSI device status
- Fill the low order status byte with the command tag
- Set the SCSI completion bit and system interrupt bit, and interrupt the host.

If the command requires a DMA operation to host memory, the adapter sets up the DMA hardware and transfers the requested data from its buffer to host memory or vice versa. It then fills the status register and interrupts the host.

After the command completion interrupt to the host, the host performs a 16-bit read operation from the status register. A subsequent 8-bit read operation to the status register (address 0D5E/095E) high order byte is then required. This operation resets the interrupt bus signal and allows subsequent interrupts to occur.

Commands

The parameter stack contents and register contents for each adapter operation code are defined below. The valid operation codes are as follows:

Op Code 0	Send SCSI Command
Op Code 1	Read/Write Buffer RAM Commands
Op Code 2	Reserved
Op Code 3	Reserved
Op Code 4	Diagnose - run Basic Assurance Tests (BATs)
Op Code 5	Diagnose - run Wraps
Op Code 6	Clear tag
Op Code 7	Continue SCSI data transfer
Op Code 8	Miscellaneous adapter information
Op code 9	Reset SCSI bus
Op Codes 10-15	Reserved

Send SCSI Command (Op code 0)

This command alerts the adapter that an SCSI command block and associated parameters are in the parameter stack, and that the command should be sent as soon as the bus is free.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved		StopXfr	DataXfr	Dir'n	SCSI ID		
1	Buffer Number							
2	Reserved							
3	Interrupt Granularity							
4								
5		LUN						
6 7 8								
9								
10 11 12								
13								
14								
15								

Figure 2. Stack Usage for Send SCSI Command

Stack Contents

Byte 0

Bits 0-2 Encoded SCSI ID of the target SCSI device.

Bit 3 The data transfer direction during the SCSI data phase. This bit must match the data transfer direction of the SCSI command.

0 Data output to SCSI bus
1 Data input from SCSI bus

Bit 4 SCSI data transfer control bit. A 1 indicates that there is a data transfer for this command and bytes 1 and 3 of the stack are valid.

Bit 5 Stop data transfer. This bit forces the adapter to use the asynchronous data mode during SCSI data transfers, and to inhibit SCSI data transfers within 512 bytes after each intermediate interrupt (See byte 3) until a 'Continue SCSI Data Transfer' command is issued.

Bits 6, 7 Reserved.

Byte 1 The starting buffer block number to read from or write to. The 64 K-byte data buffer on the adapter is divided into one hundred twenty eight 512-byte sections. The host must indicate which of these 128 buffers to use during the data phase of the SCSI command by inserting a starting buffer number from 0 to 127 in byte 1 of the stack. The number of bytes in the length parameter of the SCSI command block divided by 512 bytes is the number of buffer blocks which will be used by the command. If this number plus the buffer start location (byte 1) is greater than 127, then after buffer number 127 is used, buffer zero is accessed and a wrap around of the buffer occurs.

Byte 2 Reserved

Byte 3 This byte is the interrupt granularity. A zero in this byte position causes the adapter to issue a single command completion interrupt upon SCSI command completion (that is, after all the data from the SCSI device is in the buffer upon completion of a SCSI read command or after all the data has been sent to the device during a SCSI write command.) Notice, however, that if the SCSI command returned an error status, the read data may not be valid or the data to be written may not have been correctly received by the SCSI device.

A nonzero number in this byte position causes the adapter to issue intermediate interrupts during the data transfers to or from the SCSI bus. The period at which these intermediate interrupts are issued is every (512*interrupt granularity) bytes since the last reconnection. (See note below.) If (512*interrupt granularity) is greater than the length parameter of the SCSI command block, no intermediate interrupts are issued. See "Status Code Table" on page 31 for the contents of the status and other registers after an intermediate interrupt.

Note: Since intermediate interrupts are issued after each (512*interrupt granularity) bytes have been transferred **since the last reconnection**, SCSI devices which disconnect on other than 512 byte boundaries may not always receive granularity interrupts on exact buffer boundaries.

Bytes 4-15 For six, ten and twelve byte SCSI commands, the SCSI command descriptor block is placed in bytes 4-9, 4-13, and 4-15 respectively. The unused bytes for the shorter commands need not be written to.

The only field in the SCSI command block that the adapter uses is the logical unit (LUN) field. The remaining fields contain information for the target device only. Linked commands must not be used with this adapter. This requires bits 0 and 1 of the last SCSI command parameter byte to be zero. Once a command to a given LUN of a SCSI device has been issued, the next command to that LUN should not be issued until the previous command completes.

Command Register

See "Command Register" on page 4 for definition.

Status Register

If bit 5 is set to a 1, the SCSI command completed and the high byte of the status register contains the SCSI status byte returned by the SCSI device. If bit 5 is a 0, the SCSI command was not executed successfully and the high byte contains an error code instead of the SCSI status. The error codes are defined in "Completion Status Codes" on page 27.

Status Extension Register

If the status register contains error completion codes 41, 42, or 44, then this register contains the SCSI status byte. See "Status Code Table" on page 31. Otherwise, this register contains the ending buffer pointer value. This value is the next buffer address to be accessed and can be adjusted to determine the Last Address (LA) of data transferred as follows:

LA = S - 1 (read operation)

LA = S - 3 (write operation)

Notes:

1. S = Status extension register contents
2. Each buffer address contains 2 bytes.

Read/Write Adapter Data Buffer (Op code 1)

This command transfers a specified number of 512-byte data buffers to or from host memory. Data transfers are done by DMA operations. A single interrupt is issued by the adapter after all DMA data transfers have been completed.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved				Dir'n	ByteXfr	Reserved	
1	Reserved (Residual DMA Address)							
2	DMA Address - High Byte							
3	DMA Address - Middle Byte							
4	DMA Address - Low Byte							
5	Buffer Number							
6	Block Count/Byte Count							

Figure 3. Stack Usage for Read/Write Adapter Data Buffer Command

Stack Contents

Byte 0 Bits 0-1 Reserved

Bit 2 = Indicates if this transfer is in blocks or bytes.

0 Block transfer, stack byte six contains block count
1 Byte transfer, stack byte six contains byte count

Bit 3 = The data transfer direction during the DMA for this command.

0 Write adapter buffer
1 Read adapter buffer

Bits 4-7 Reserved

Byte 1 Residual DMA address. This byte is reserved to allow the system to load the full 32-bit address it has for the DMA address so there is no need to parse it out. This byte is always ignored by the adapter.

Byte 2 Host DMA data address, high byte divided by 2.

Byte 3 Host DMA data address, middle byte divided by 2.

Byte 4 Host DMA data address, low byte divided by 2.

Byte 5 Starting Buffer Number.

Byte 6 If bit 2 of byte zero is a 1, this field contains the number of transfer bytes divided by 2. If bit 2 of byte zero is a 0, this field contains the number of 512-byte blocks to transfer minus one.

Command Register

See "Command Register" on page 4 for definition.

Status Register

See "Status Register" on page 3 for definition.

Perform Basic Assurance Tests - BATs (Op code 4)

This command causes the adapter to reset the SCSI bus and run tests on adapter registers and memory, including RAM. This command is an immediate command so it is executed as soon as the adapter receives it. During execution, the buffer and registers are cleared, therefore the host should make sure that no other commands are in progress before this operation code is used.

During command execution, more than one test is performed. If any test fails, a status other than X'0F' is reported. If status is read again, a X'0F' is reported to indicate BATs have completed. If no errors are detected only the X'0F' status is reported and normal operation can begin.

Stack Contents

Reserved

Command Register

See "Command Register" on page 4 for definition. Tag bits are ignored for BATs; the tag field is loaded with a X'1F' value.

Auxiliary Register

If BATs completed successfully, then this register and the status extension register contain zeros, otherwise each register is reserved.

Status Register

Bits 15-8 If these bits contain the code X'0F', then all tests have been executed. Otherwise error status needs to be read. (See "Status Code Table" on page 31).

Bits 7-0 See status register definition. (Bit 7 is set to a one until command completion.)

Status Extension Register

See auxiliary register above.

Perform Wrap Tests - Wraps (Op code 5)

This command starts a wrap test which tests the SCSI bus line drivers, receivers, and enable logic. The external SCSI cable should be removed or all SCSI devices which are attached to the SCSI bus must be turned off before attempting a wrap test. This command is an immediate command so it is executed as soon as the adapter receives it. During execution, the buffer and registers are cleared, therefore the host should make sure that no other commands are in progress before this operation code is used.

Stack Contents

Reserved

Command Register

See command register definition.

Auxiliary Register

If the WRAPS completed successfully, then this register and the status extension register contain a zero, otherwise each register may be nonzero.

Status Register

If the high byte of the status register (address 0D5E or 095E) contains a zero completion code then the WRAPS completed successfully. Otherwise, if the failing wrap number in bits 8 through 12 in the high byte is a nine, then check the fuse on the board. If the failing wrap number is other than zero, check the cables. See "Completion Status Codes" on page 27.

Status Extension Register

See auxiliary register above.

Clear Tag (Op code 6)

This command clears a tag for an adapter command. If the tag was for a SCSI command and the adapter is connected to the LUN referenced by the SCSI command, the SCSI Reset line is pulsed. (See "Reset Condition" on page 34.)

Stack Contents

Byte 0

Bits 7-5 Reserved

Bits 4-0 Tag number to be cleared.

Command Register

See "Command Register" on page 4 for definition.

Status Register

See "Status Register" on page 3 for definition.

Continue SCSI Data Transfer (Op code 7)

This command is used in conjunction with the 'Send SCSI Command' operation to allow SCSI data transfer operations to continue after they have been inhibited after an intermediate interrupt. See the Send SCSI Command description for the method of specifying intermediate interrupts and inhibiting SCSI transfers after them. The tag used for this operation must be the same as the tag for the 'Send SCSI Command' operation which is being resumed. No interrupts or completion status is returned to the host.

Stack Contents

Reserved

Command Register

See "Command Register" on page 4 for definition.

Status Register

Reserved

Miscellaneous Adapter Information (Op code 8)

This command is used to get certain available information about the adapter that may be needed for diagnostics or configuration purposes. Currently the only byte defined is a ROM E.C. level and version numbers. See the register definitions below. This command is an immediate command and is executed as soon as the adapter receives it.

Stack Contents

Reserved

Command Register

See "Command Register" on page 4 for definition.

Status Register

If the high byte of the status register contains a zero completion code, then the status extension registers and auxiliary registers contain valid information.

Status Extension Register

This high byte of the status extension register (address 0D58 or 0958) contains the ROM E.C. version number. The low byte contains the ROM E.C. level number. The ROM level is a subdivision of the ROM version. Each time the version number is changed, the level numbers restart at zero.

Auxiliary Register

Reserved

Reset SCSI Bus (Op code 9)

This command causes the adapter to pulse the SCSI reset line. All outstanding commands are cleared.

Stack Contents

Reserved

Command Register

See "Command Register" on page 4 for definition. The tag bits are ignored.

Status Register

Bits 15-8 = X'83' (See "Status Code Table" on page 31).

Bits 7-0 = X'1F'

Status Extension Register

Reserved

Auxiliary Register

Reserved

Command Staging and Buffer Data Pointer Storage

Two command storage capabilities are provided by the adapter:

- Unsent SCSI command storage
- Data pointer storage for commands in process.

Unsent SCSI Command Staging

After receiving any SCSI command from the host, the adapter immediately attempts to arbitrate for the SCSI bus and send the command to the addressed device. If the bus is not free it stores the command, clears the status register busy bit and continues trying to obtain the SCSI bus and send the command. If the host sends another SCSI command to a different device before the adapter has sent the first command to the first SCSI device, the adapter will accept the command and again clear the status register busy bit. If the SCSI bus is very busy and the adapter has accepted 16 commands without executing any of them, it will not clear the busy bit until it has sent the first command. This storage capability allows the adapter to hold off the host during periods of intense SCSI bus activity and to issue new commands once it becomes free. Unsent SCSI commands are sent according to an algorithm which gives priority to commands with low tag numbers.

Because the time required for the adapter to establish an SCSI connection and send a command is unknown, the busy bit is set for an indeterminate length of time in the case where 16 unsent commands have been stored.

Tag Management and Execution Order

This section describes the algorithm used for the execution order of SCSI and buffer commands (op codes 0 and 1). These commands are not executed in FIFO order. SCSI command tags and buffer command tags are handled separately but use the same algorithm. All other op codes are immediate op codes and are executed as they are received by the adapter. For this description, op code 1 (buffer commands) will be used in the examples.

The host supplies a unique tag for each command issued to the adapter. Several buffer commands (and SCSI commands) can be issued before status is received by the host. All of the outstanding commands can be in various stages of execution and the firmware must maintain the progress of each one. This is done in an array indexed by the tag number. Each element of the tagged array has a state field which describes the execution state for the command with that tag number.

When a read/write buffer op code is received into the tagged array, the array is searched and if no other buffer op codes are present, this state field is set to *executing* and the command execution is begun. If a buffer command is already being processed, then this one is labelled as the *next to execute*. If there already is a *next* then it is labelled as *ready*. As soon as the executing command is complete, the command whose tag state is *next* is executed and the whole array is searched from low to high tag. The first tag found whose state is *ready* becomes the *next* command to execute.

This algorithm allows a high priority command to be executed before a command that was sent previously if that is desired. This is accomplished by placing a command at a lower tag number than all of the other outstanding commands.

Example of Execution Order Algorithm

The host sends four buffer commands to the adapter as fast as it can. Each command goes to successive tag numbers. Assuming no other buffer commands are outstanding, when the adapter receives the first one it will set its state to *executing* and begin running it. When the adapter receives the second one, the state is set to *next* since only one other buffer command is present. The next two commands will receive states of *ready*. Tag example 1 illustrates the result of receiving these four commands.

Tag	Command	State
0	- - - - -	
1	- - - - -	
2	- - - - -	
3	Buffer A	Executing
4	Buffer B	Next
5	Buffer C	Ready
6	Buffer D	Ready
7	- - - - -	
8	- - - - -	
9	- - - - -	
10	- - - - -	
11	- - - - -	
12	- - - - -	
13	- - - - -	
14	- - - - -	
15	- - - - -	

Figure 4. Tag Example 1

When the first command is completed, status is returned to the host and this tag is now free to use again. The tag found whose state is *next* will be changed to *executing*. The array will be searched from tag 0 to the end until a tag is found whose state is *ready*. This tag state will be changed to *next*. Tag example 2 shows this result.

Tag	Command	State
0	- - - - -	
1	- - - - -	
2	- - - - -	
3	- - - - -	
4	Buffer B	Executing
5	Buffer C	Next
6	Buffer D	Ready
7	- - - - -	
8	- - - - -	
9	- - - - -	
10	- - - - -	
11	- - - - -	
12	- - - - -	
13	- - - - -	
14	- - - - -	
15	- - - - -	

Figure 5. Tag Example 2

If two more buffer commands are added, one to tag 1 and one to tag 9, their states will be *ready* as before because tags already exist with states of *executing* and *next*. The implied priority of the algorithm now shows its effect when tag 4, the executing tag, is completed. As before, the tag whose state is *next* begins executing. When the array is searched for the first *ready* tag, it is tag 1 that is labelled as *next* and not tag 6. These results are shown in tag example 3.

Tag	Command	State
0	- - - - -	
1	Buffer E	Next
2	- - - - -	
3	- - - - -	
4	- - - - -	
5	Buffer C	Executing
6	Buffer D	Ready
7	- - - - -	
8	- - - - -	
9	Buffer F	Ready
10	- - - - -	
11	- - - - -	
12	- - - - -	
13	- - - - -	
14	- - - - -	
15	- - - - -	

Figure 6. Tag Example 3

Notice that the command at the highest used tag will not be executed until the one previous to it changes state from *next* to *executing* and no other tags containing buffer commands are in *ready* state. This means that in order to execute the highest tag used, no more than three buffer commands can be outstanding. The host should not send another command until status is received from one of the three outstanding commands.

During normal operation, both SCSI commands and buffer commands may be intermixed in the array as in tag example 4, or the host may decide to use the first half of the tags for buffer commands and the second half for SCSI commands. In either case, the algorithm is applied separately to each of the two command types. Again, other op codes cause a tag to be busy while the command is being executed but the execution algorithm is not used on them.

Tag	Command	State
0	- - - - -	
1	- - - - -	
2	SCSI	Ready
3	Buffer A	Executing
4	SCSI D	Ready
5	- - - - -	
6	- - - - -	
7	Buffer E	Ready
8	Buffer B	Next
9	Buffer C	Ready
10	- - - - -	
11	SCSI A	Executing
12	SCSI B	Next
13	Buffer D	Ready
14	Buffer F	Ready
15	- - - - -	

Figure 7. Tag Example 4

SCSI Command Linking

SCSI command linking is not supported. This requires bits 0 and 1 of the last byte of all SCSI command blocks to be zero.

SCSI Commands in Process

The adapter can store up to 16 sets of DMA pointers and associated intermediate status for SCSI LUN's which have disconnected for command processing. (Each pointer is associated with a unique command tag X'0' - X'F'.) A command reject is returned if the tag is outside the range X'0' - X'F'.

Data Buffer Management

The adapter data buffer consists of 64K-bytes of RAM divided into one hundred twenty eight 512-byte buffers. As described in the 'Send SCSI Command' definition, the host specifies which buffers to use during the data phase of each SCSI command. When the host wishes to transfer the SCSI data to or from its memory, it then can issue a Read/Write Buffer command to initiate the desired data transfer. In order to utilize the data buffer's dual port capability during data read operations, the host can issue a SCSI command which will result in a data phase, and immediately issue a Read/Write Buffer command to transfer the data to or from its memory. The following typical sequences of operations that the host would follow are:

Read

The host first issues a Send SCSI command operation which calls for a read operation of 8K-bytes to adapter memory from the SCSI device. An interrupt granularity of 2K-bytes is specified. The adapter then sends the SCSI command to the SCSI device and begins transferring data into the adapter buffer as soon as the SCSI device begins its data transfer. As soon as 2K-bytes are transferred, the adapter issues an intermediate interrupt to the host. The host then issues a Read Adapter Buffer operation to read the first 2K-bytes of data into host memory. As the first 2K-bytes of data is being transferred to the host, the SCSI device may finish sending the second 2K-bytes of data to the adapter buffer, and the adapter may issue another intermediate interrupt to the host. As long as the host has received more intermediate interrupts than it has given 2K-byte Read Adapter Buffer commands, it continues to issue Read Buffer Commands until all 8K-bytes of SCSI data has been transferred. Notice that unless the SCSI device terminates the Read command immediately upon the occurrence of a hard error, the integrity of the data received cannot be guaranteed until the total 8K-byte command completes. Also notice that the actual number of data bytes transferred for any command is under control of the target.

Write

The host adapter first issues enough Write Adapter Buffer commands to fill the adapter buffer with 4K-bytes of data. The adapter then issues a Send SCSI Command operation to transfer the 4K-bytes of data from the adapter memory that it just wrote. As the SCSI device transfers these 4K-bytes, the adapter can begin transferring another block to be written to that SCSI device so that when the device finishes writing the 4K-bytes, another Send SCSI Command operation can be issued to the SCSI device. Notice that unless the SCSI device terminates the Write command immediately upon the occurrence of a hard error, the successful storage by the SCSI device of the adapter buffer data cannot be guaranteed until the SCSI command completes. Also notice that the actual number of data bytes transferred for any command is under control of the target.

The data buffer may contain both read and write data simultaneously and it can simultaneously read from the SCSI bus into the buffer and read from host memory into the buffer. Likewise, it can simultaneously write to the SCSI bus and write to host memory. Therefore, if a write data buffer command is received during the time the adapter is connected to an SCSI device in a *data-in* phase, the Write Data Buffer command will not be delayed until the *data-in* phase is completed. Likewise, if a read data buffer command is received during the time when the adapter is connected to an SCSI device is in a *data-out* phase, the Read Data Buffer command will not be delayed until the *data-out* phase is completed.

SCSI commands involving data phase block lengths of larger than 64K-bytes should not be sent unless the complete 64K-byte buffer is used. In this case, the adapter will use the complete buffer as a wraparound buffer. There are two options for handling this type of data transfer. The first is where the host is responsible for ensuring that buffer overruns do not occur. The host does this by choosing an interrupt granularity of sufficient size and responding to intermediate data interrupts with Read/Write Buffer commands such that buffer overruns do not occur. When this option is chosen, the timing for interrupts and commands may result in data loss.

The second option requires that the host set bit 5 in the first byte of the stack during the Send SCSI command operation and to load the interrupt granularity field with an appropriate value. (Larger values of interrupt granularity will result in better performance.) The adapter forces the data transfer to be asynchronous and will stop the data transfer after the requested interrupt granularity. This option ensures against underruns and overruns, but the SCSI bus will be hung after intermediate interrupts until a Continue SCSI Data Transfer command is received. For details about this option, see "Send SCSI Command (Op code 0)" on page 9.

Odd Byte Data Transfers

All DMA transfers begin and end on even byte boundaries, and the SCSI transfer lengths will always be an even number of bytes. SCSI devices which return an odd number of bytes at command completion cause the adapter to insert a dummy byte into host memory to provide the even number of bytes for the DMA transfer. Any time a disconnect message is received by the adapter and an odd number of data bytes have been transferred for that command, error code X'45' is flagged. Therefore, SCSI devices which disconnect before giving the command complete message and which later reconnect to complete the command *must* disconnect on *even* byte boundaries.

Completion Status Codes

This section describes the completion codes returned to the host when errors occur and for normal completion. The completion code itself is returned in the high byte of the status register at address 0D5E or 095E. Based on the value of the code, other status registers may contain valid information. Details of these codes are defined below and summarized in "Status Code Table" on page 31.

Adapter Ready Status

Code (Hex)	Description
0F	This code indicates that the adapter is ready to initialize and begin running after a hardware reset or after BATs (op code 4) is run. In both cases basic assurance tests (BATs) have been run and other errorstatus may have been already returned to the host. See "Perform Basic Assurance Tests - BATs (Op Code 4)" on page 13 and "Reset Condition" on page 34 for more information.

Adapter Detected Fault Condition

Code (Hex)	Description
81	The firmware has detected a differential sense fault. This could be due to a single-ended device or wrong cable inadvertently attached to the SCSI connector on the adapter. After this status is read by the host, firmware will abort all current operations, reset the SCSI bus, and reset the adapter by branching to BATs.
82	The firmware has detected bad terminator power. This could be due to a blown fuse or cable termination. After this status is read by the host, firmware will abort all current operations, reset the SCSI bus, and reset the board by branching to BATs.
83	The firmware has detected that the SCSI bus has been reset. The firmware has aborted all SCSI commands in progress and cleared the tagged array of any outstanding commands. Read/write buffer commands as well as all other op codes will not be affected.
84	This code is returned when a firmware timer has expired indicating a code hang or timeout situation. This may be due to a SCSI bus error or timing problem.

88	This status will be returned as a result of a firmware wild branch condition. In other words, if the firmware can detect that an area of the ROM is being executed that has no defined code in it, this status code will be returned. The status extension register will contain the address at which the wild branch was discovered. This error should not occur unless something has gone wrong, and BATs should be run to determine the error.

Normal Completion Response

Code (Hex)	Description
00	A zero code is the status received when op codes 5, 6, 7, and 8 have completed without errors. (Notice that at this time for op code 8 only, the status extension register contains additional information.)
XX (SCSI)	If bit 5 in the low byte of the status register is a one, then the completion code is the actual status byte received from the target device on the SCSI bus. See "Status Code Table" on page 31 for details of this byte.

Abnormal Completion Response

- Command Rejected

Code (Hex)	Description
21	The command tag requested in the command register is already being used by a previous command. Either change the tag and issue the command again or clear the tag using op code 6 and then reissue the command.
22	The tag requested in the command register is not in the '0' to 'F' valid range for op codes 0 or 1 and not in the '0' to '10' valid range for other op codes.
23	The op code requested in the command register is a reserved number and not executable.
24	The parameter count requested in the command register is not valid. This should be the byte count of the SCSI command block and can only be 6, 10 or 12. This field is only used for op code 0.
25	The SCSI id in the stack parameters is invalid. The id cannot be the same as this adapter, which is 7. All other values for this field (0 to 6) are accepted.
27	The buffer number or block count information in the stack parameters is too large for the buffer RAM size on the adapter.

- Command Execution Fault

Code (Hex)	Description
41	The SCSI device tried to restore the data pointers to an area of the buffer that may already be used for another command. The firmware will have rejected the restore data pointers message and the target will come back with non zero status. The host should reissue the command. This code is returned at the command completion interrupt. The SCSI command completion status byte is placed in the status extension register high byte. The status extension register low byte contains pthe hex value 20.
42	The SCSI device tried to modify the data pointer to an area of the buffer that may already be used for another command. The firmware will have rejected the modify data pointers message and the target will come back with non-zero status. The host should reissue the command. This code is returned at the command completion interrupt. The SCSI command completion status byte is placed in the status extension register high byte. The status extension register low byte contains the hex value 20.
43	There was a parity error on a DMA transfer. The host should reissue the buffer command (op code 1).
44	A parity error was detected on data being read from the SCSI bus. The host should reissue the SCSI command (op code 0). This code is returned at the command completion interrupt. No grandularity interrupts are sent after the parity error was detected. The SCSI command completion status byte is placed in the status extension register high byte and the status extension register low byte contains the hex value 20 if good SCSI status is received. If good status is not received, the status extension register high byte contains hex 48.
45	The SCSI device disconnected during a data transfer on an odd byte boundary. The firmware will abort the SCSI command and the host should try and reissue the command.
46	A clear tag command was received for a tag that was already cleared.
47	The microcode has tried unsuccessfully three times to select a target and has been unable to do so.
48	The adapter never received a parity free status byte for the command.

- Informational

  Code (Hex) **Description**

  A1 The required interrupt granularity time requested has passed. This indicates to the host that the next block of data has been written to or read from the buffer and the host can reuse that block as necessary.

  The interrupt granularity requested can be small enough and the adapter busy enough that more than one status interrupt of this type can be pending for a command. To avoid having to read status twice or more for the information, the high byte of the status extension register will be incremented by the firmware to indicate the number of blocks available.

  - Diagnostic op - BATs

    See "Perform Basic Assurance Tests - BATs (Op Code 4)" on page 13 for details.

  - Diagnostic op - WRAPS

    See "Perform Wrap Tests - Wraps (Op code 5)" on page 14 for details.

Status Code Table

Status High Completion Code	Status Low * Tag	Status Ext Register Usage	Meaning
0000 1111 (0F)	xx 0 1 1111	N/A	Adapter ready after hardware reset or BATs op code completed
100x xxxx			Adapter detected fault condition during normal operation:
1000 0001 (81)	xx 0 1 1111	N/A	SCSI differential sense error
1000 0010 (82)	xx 0 1 1111	N/A	SCSI terminator power error
1000 0011 (83)	xx 0 1 1111	N/A	SCSI bus reset occurred
1000 0100 (84)	xx 0 1 1111	8031 Addr	Watch dog timeout
1000 1000 (85)	xx 0 1 1111	8031 Addr	Firmware 'wild branch'
			Normal completion response to adapter op codes
SCSI Stat	xx 1 t tttt	Note 5	for OP 0
0000 0000 (00)	xx 0 t tttt	Note 4	for OPs 1,5,6,7,8

Figure 8 (Part 1 of 2). Status Code Table

Status High Completion Code	Status Low * Tag	Status Ext Register Usage	Meaning
			Abnormal completion response
001x xxxx			Command Rejected - Reason
0010 0001 (21)	xx 0 t tttt	Command Reg	Command tag in use
0010 0010 (22)	xx 0 t tttt	Command Reg	Command tag out of range
0010 0011 (23)	xx 0 t tttt	Command Reg	Invalid operation code
0010 0100 (24)	xx 0 t tttt	Command Reg	Invalid stack parameter count
0010 0101 (25)	xx 0 t tttt	Command Reg	Invalid SCSI ID
0010 0111 (27)	xx 0 t tttt	Command Reg	Bad buffer block info.
010x xxxx			Command Exec Fault - Reason
0100 0001 (41)	xx 0 t tttt	SCSI status	SCSI Restore Pntrs
0100 0010 (42)	xx 0 t tttt	SCSI status	SCSI Modify Data Pointer
0100 0011 (43)	xx 0 t tttt	N/A	DMA transfer parity error
0100 0100 (44)	xx 0 t tttt	SCSI status	SCSI transfer parity error
0100 0101 (45)	xx 0 t tttt	N/A	SCSI odd byte xfer
0100 0110 (46)	xx 0 t tttt	N/A	Tag already cleared
0100 0111 (47)	xx 0 t tttt	N/A	Unable to select target
0100 1000 (48)	xx 0 t tttt	Note 5	Bad Status
001x xxxx			Informational - Reason
1010 0001 (A1)	xx 0 t tttt	# of ints	Intermediate xfer interrupt
110n nnnn	xx 0 1 1111	Note 3	Diagnostic Op - BATs failed
111n nnnn	xx 0 t tttt	Note 3	Diagnostic Op - Wraps failed

Figure 8 (Part 2 of 2). Status Code Table

Notes:

1. t = tag number used; n = failing BAT or WRAP number
2. * 1 = SCSI status from target
3. See BATs/WRAPs sections for details.
4. See "Miscellaneous Adapter Information (Op code 8)" on page 16 for details; N/A for all other op codes.
5. Buffer address (See "Send SCSI Command (Op code 0)" on page 9 for details).

SCSI Implementation

The following table summarizes the SCSI design point chosen.

Data Rate	3.6 M Bytes/sec (maximum–synchronous)
Data Protocol	Synchronous or Asynchronous
SCSI Bus Phases	Arbitration, Selection, Command, Message, Data, Status, Reselection
SCSI Bus Priority	Seven (fixed at highest level)
SCSI Device Type	Initiator Only
Electrical Interface	Differential Mode signals
	Internal Terminator Network
	Terminator Power Supplied and Fused (1 Amp.)
	Shielded connector
	Parity required of all devices on bus
Cable Length	25 meters (maximum)
SCSI Command Sets	Groups 0 through 7

Note: Only one host adapter of the type described in this specification may be present on the SCSI bus at a time. Other initiators with lower priorities may be connected but may not directly communicate with this adapter; this adapter does not function as a target.

The following sections outline more specifically how this adapter has implemented the requirements of the American National Standards Institute (ANSI) standard.

Reset Condition

Incoming Reset Pulses

Whenever the RST line is pulsed, all adapter commands are cleared. Any device (such as a device which has implemented the soft reset option) which reselects the adapter to continue a command after the RST pulse will be issued a Bus Device (BDR) Message. See "Bus Device Reset (BDR) Message (Reset Procedure)" on page 38.

Note: The first device attempting a reselection after a reset may be unable to reconnect on its first reselection attempt.

Outgoing Reset Pulses

The host can direct the adapter to issue a pulse on the RST line by issuing a Perform BATs operation (Op code 4). The RST line may also be pulsed during a 'Clear Tag' command. The adapter will also issue a pulse on the RST line after an unsuccessful attempt to send a Message Parity Error (MPE) or BDR message. A reset pulse is also generated if any device takes longer than 65 milliseconds to complete any non-data phase.

SCSI ATN Line

The adapter raises the ATN line whenever it has a message for the target. The target may or may not respond with the message out (MO) phase. If a parity error occurs during any message in (MI) phase, the ATN line is asserted and a MO phase must occur in response to the ATN signal or a reset pulse will occur. (In this case, the ATN line is asserted prior to the release of ACK during the REQ/ACK handshake of the message byte in error.) For erroneous multibyte messages ATN is asserted prior to the release of ACK for the last REQ/ACK handshake of the message.

Once an MO phase is begun, the target must stay in the MO phase until the ATN line has been released by the adapter unless an error occurs. The ATN line will be released while REQ is active and ACK is inactive during the last REQ/ACK handshake of the MO phase.

Message Phase Implementation

The table below summarizes the messages implemented by this adapter.

Message	Direction
Command Complete (CC)	In
Save Data Pointer (SDP)	In
Restore Pointers (RP)	In
Disconnect (DSC)	In
Initiator Detected Error (IDE)	Out
Message Reject (MR)	In Out
No Operation (NOP)	Out
Message Parity Error (MPE)	Out
Bus Device Reset (BDR)	Out
Identify (IDF)	In Out
Extended Messages:	
Synchronous Data Transfer	In Out

All other messages will be rejected. SCSI devices that take more than 65 milliseconds to complete any non-data phase are not supported.

Command Complete Message

This message must be received by the adapter to successfully complete a command.

Save Data Pointer

This message is always accepted and the saved buffer location is stored.

Restore Pointer

If a nonzero granularity interrupt value was specified when the Send SCSI command was issued by the host, then the restore pointers message is accepted only if the current pointers equal the saved pointers, such as after a reconnection to continue a command. Otherwise it is rejected. If zero was specified for the granularity interrupt value, then the restore pointers message is accepted and it causes the adapter to restore the current data pointers to the location previously saved by the SCSI device.

Disconnect

This message or the command complete message should be received by the adapter between any phase and the bus free phase. If one of these messages is not received just before the bus free phase, the adapter clears all records of the command in process. Subsequent attempts to reconnect by the logical unit (LUN) will result in an BDR message being sent to the reconnecting device.

SCSI data transfers cannot be interrupted by a disconnection after transferring an odd number of bytes. If an SCSI device disconnects after transferring an odd number of bytes without sending the command complete message, then the adapter will clear all record of the current command and interrupt the host to inform it of this occurrence.

Note: Data transfers of an odd number of bytes are possible and can be interrupted by disconnections, but only the last block of data transferred just before command completion may contain an odd number of bytes.

Initiator Detected Error (IDE)

The adapter attempts to send this message if a parity error is detected during a status phase. It does this by asserting the SCSI ATN line prior to its release of ACK for the status phase. If the IDE message is either rejected or is not accepted and the device sends the command complete message before the adapter receives an error free status byte, then the host is interrupted with a completion code indicating bad status. Parity errors which occur during data input phases are reported to the host. The adapter does not send the initiator detected error message for these errors.

Message Reject

This message is sent in response to an incoming message which is not implemented by the adapter. For single byte messages, the adapter raises the ATN line prior to its release of ACK for the message to be rejected. For extended messages, ATN is asserted prior to releasing ACK for the last byte of the extended message. Subsequent extended message bytes are read and ignored and the next bus phase must be the message out phase. This message is also sent when a restore pointers message is received, when the current pointers do not equal the saved pointers, and the interrupt granularity for the command is nonzero. In the case of incoming MR messages, no action is taken except in the following circumstances:

- During the synchronous data transfer negotiations
- After IDE, BDR, or MPE messages.

No Operation

This message is sent by the adapter when the target enters a MO phase and the adapter has no messages to send.

Identify

The adapter attempts to send identify messages after any selection phase. If they are accepted by the SCSI device, then disconnection will be enabled by setting bit 6 of the message byte to a 1. An incoming identify message must be received by the adapter in the first bus phase following a reselection by any multiple LUN target.

Message Parity Error

The adapter attempts to send this message when a parity error is detected during a MI phase. It does this by asserting the SCSI ATN line prior to its release of the ACK signal for the last byte of the MI phase with the error. If the next phase is not the MO phase, then the adapter will pulse the RST line.

The message parity error message must be accepted (if it is rejected, the bus is reset). After it is received by the target, the next bus phase must be either a retry of the preceding MI phase, a retry of the MO phase, or the bus free phase.

Synchronous Data Transfer

This message is used in negotiations for data transfer mode. Synchronous data transfers will be used whenever possible.

Bus Device Reset (BDR) Message (Reset Procedure)

The BDR message will be issued if the adapter is reselected by a LUN for which the adapter has no outstanding command. See incoming reset pulses under "Reset Condition" on page 34.

If the target does not enter the MO phase when ATN is raised after the above condition or if the BDR message is accepted, the adapter will clear its memory of the command records to all LUNS of the SCSI device. The next bus phase must be the bus free phase.

If the BDR message is rejected, a hard reset pulse is issued to the SCSI bus and the host is interrupted to inform it of this action.

Bus Free Phase

The target should not go to the bus free phase except after either sending one of the command complete messages or a disconnect message.

If the target disconnects without sending one of these messages, the adapter clears all records of the current command. Subsequent attempts to reconnect by the LUN results in a BDR message being sent to that LUN. As required by the ANSI specification, the target must go to the bus free phase under any of the following conditions:

- After a Bus Device Reset message was received and not rejected
- After a pulse to the RST line.

Connector

The connector signals and pin assignments are as follows:

Signal Name	+ Signal Pin	- Signal Pin
SHIELD GND	1	2
DB0	3	4
DB1	5	6
DB2	7	8
DB3	9	10
DB4	11	12
DB5	13	14
DB6	15	16
DB7	17	18
DBP	19	20
DIFFSENS	21, 62	22
GND	23	24
TERMPWR	25	26
GND	27	28
ATN	29	30
GND	31	32
BUSY	33	34
ACK	35	36
RST	37	38
MSG	39	40

Figure 9 (Part 1 of 2). SCSI Connector Pins

Signal Name	+ Signal Pin	- Signal Pin
SEL	41	42
C/D	43	44
REQ	45	46
I/O	47	48
GND	49	50

Figure 9 (Part 2 of 2). SCSI Connector Pins

Note: Pins 51 through 61 are not used.

IBM

Personal Computer Hardware Reference Library

Streaming Tape Drive Adapter

Contents

Description

The IBM RT PC Streaming Tape Drive Adapter provides a QIC-02 (Quarter Inch Cartridge) tape interface to the IBM RT PC System. The adapter uses programmed I/O for the 16 bit data transfers to and from its 512 byte sector buffer. It uses interrupt sharing on level 12 and decodes 16 bits for the I/O address. The adapter provides all of its own clocking and does not require any system clocking support.

The card design is centered around a 8042 microcontroller which contains 2K of ROM, 128 bytes of RAM, an 8-bit timer or counter and 18 programmable I/O pins. Commands from the system are interpreted by the controller and output to the tape drive in accordance with the streaming tape interface. Prior to issuing a command, the controller will verify that the drive is ready and has no pending errors. The 8042 will also present status to the system as the result of a status read from the drive. The status bits may then be decoded to indicate various drive conditions, such as beginning of media, over and underruns, and file mark found. A pair of registers are available to the system for commands and data.

During command execution or data transfers the system does not have access to the control processor registers. Two registers are available during these times to provide status information and allow system control functions. The read only status register provides various attachment indications (such as busy) and several signals directly from the tape drive interface. The control register allows the system to disable interrupts or parity checking and also provides reset capability to the attachment.

To initiate a command the system must output to the 8042 command port, this sets input buffer full (IBF) in the status port. IBF resets when the 8042 reads the command. The microcode will then decode and execute the command. If a read command is issued, the controller sends the QIC-02 tape read command to the drive and enables the sector buffer through the programmable logic sequencer (PLS). Once the drive has come up to speed and starts to read, the PLS transfers data into the buffer according to the handshake sequence detailed in the QIC-02 specifications. When the buffer is full, the PLS signals the 8042, which raises the hardware interrupt signal to the system. The 8042 then resets the PLS in preparation for the system data read. The system executes a programmed I/O move and transfers the data from the adapter to the system. A similar chain of events occurs during a write command, except the data moves in the opposite direction.

A read status command starts in the same way as a read but the PLS is not required since the data (6 bytes) is transferred directly into the 8042 data port from the drive. In this case, when the status data is presented to the attachment, the 8042 forces a write to its own data port and then completes the handshake operation. The command then reads the data register and stores it in internal RAM. This is repeated until the six status bytes are read and the 8042 interrupts the system and transfers the stored data to the system via its data port.

The remaining commands fit into the basic architecture described above.

Figure 1 on page 2 is a block diagram of the IBM RT PC Streaming Tape Drive Adapter.

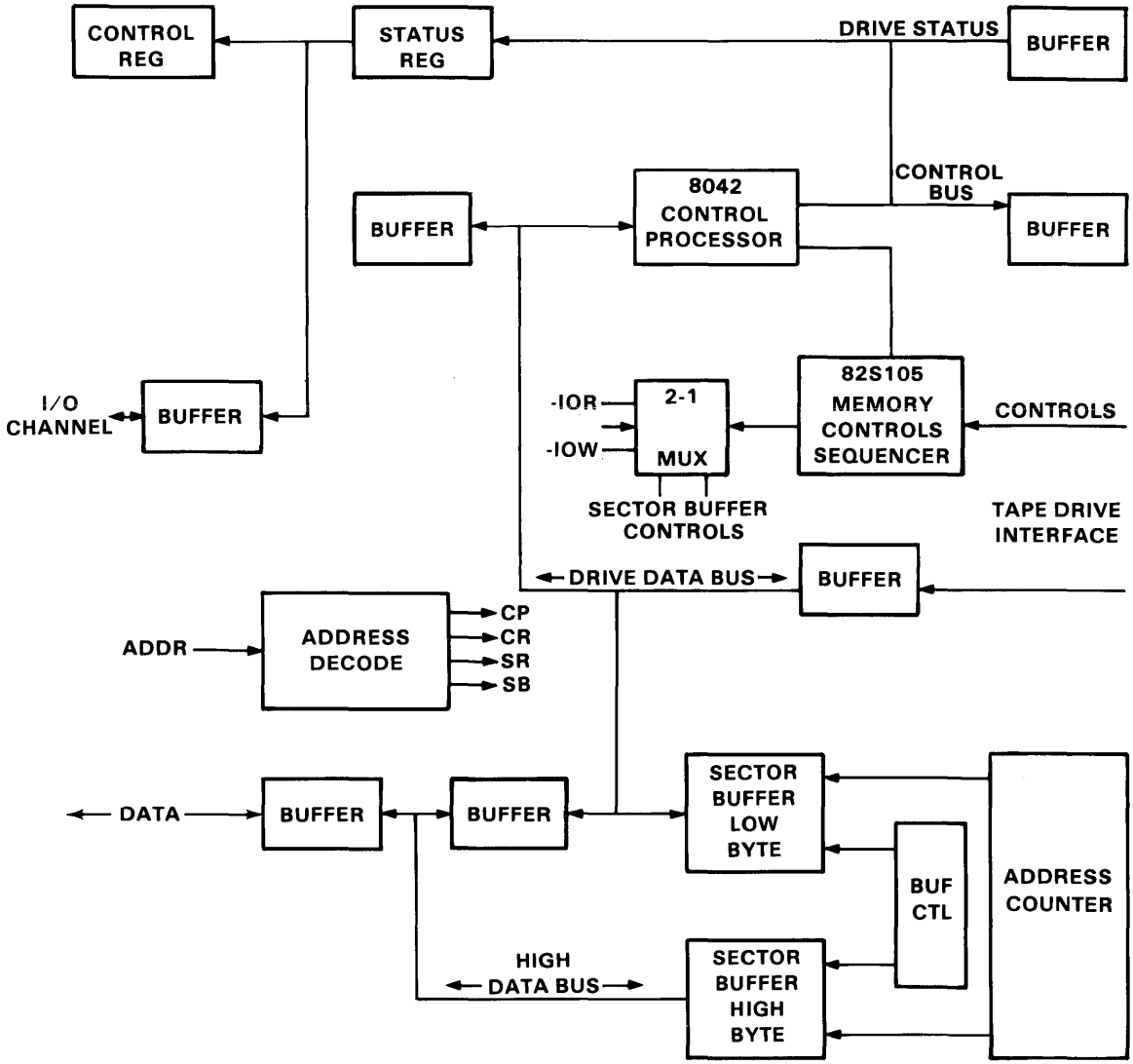


Figure 1. Streaming Tape Adapter Block Diagram

System I/O Channel

The following lines connect the IBM RT PC Streaming Tape Drive Adapter card to the I/O channel.

+ SA00-SA15 (Input)

System address bits 0 to 15: These lines address memory and I/O devices within the system. SA00 is the least significant bit (LSB) while SA15 is the most significant bit (MSB).

+ Reset DRV (Input)

Reset Driver: This line resets or initializes system logic upon power-up or during a low line voltage outage. This signal is active high.

+ SD00-SD15 (Input/Output)

Data bits 0 to 15: These lines provide data bus bits 0 to 15 for the processor, memory, and I/O devices. SD00 is the least significant bit.

+ IRQ3-IRQ7,IRQ9-IRQ12, IRQ14-15 (Output)

The IBM RT PC Streaming Tape Drive Adapter uses interrupt level 12 which is a shared interrupt level. All other levels are not used by the adapter.

- IOR (Input)

I/O Read Command: If the IBM RT PC Streaming Tape Drive Adapter card is being addressed, the adapter drives its data on to the data bus and holds the data on the data bus as long as IOR is active. This signal is active low.

- IOW (Input)

I/O Write Command: If the IBM RT PC Streaming Tape Drive Adapter card is being addressed, the adapter reads the data on the data bus. The data is latched at the trailing edge of IOW. This signal is active low.

+ AEN (Input)

Address Enable: This line degates the processor and other devices from the I/O channel to allow DMA. This line must be low to decode a valid address for an I/O channel transfer.

- IOS16 (Output)

I/O Chip Select 16: This line is active when a 16-bit I/O transfer takes place between the adapter and the system.

IBM RT PC Streaming Tape Drive Adapter Signal Line Descriptions

Online

'Online' is an adapter generated control that activates prior to transferring a Read or Write command. Deactivation terminates the Read or Write command.

Request

'Request' is an adapter generated control that indicates command data has been placed on the data bus while in command mode, or status has been taken from the data bus while in status input mode. The system asserts request only when the drive asserts ready or execute.

Parity

'Parity' is a bidirectional line which is odd parity of the 8-bit data bus.

Data Bus

'Data Bus' is the 8-bit bidirectional data bus. Bit 7 is the most significant bit.

Reset

'Reset' causes the drive initialization to perform and sets default selection to drive 0. Exception asserts.

Transfer

'Transfer' is an adapter generated control that indicates command data has been placed on the data bus when in write mode, or data has been taken from the data bus in read mode.

Acknowledge

'Acknowledge' is a drive generated control that indicates command data has been taken from the data bus when in write mode, or data has been placed on the data bus in read mode.

Ready

'Ready' is drive generated and indicates one of the following:

- Data has been taken from the data bus in command transfer mode
- Data has been placed on the data bus in the status input mode
- A Beginning of Tape (BOT), Retension, or Erase command is complete
- The drive is ready to receive the next block, a Write command, or a Write File Mark (WFM) command from the system when in write mode.
- The drive is ready to transmit the next block to the system or ready to receive a Read or Read File Mark (RFM) command when in read mode

- The drive is ready to receive a new command.

Exception

'Exception' is drive generated and indicates an exception condition has occurred. The system must issue a Read Status command and perform a status input to determine the cause.

Direction

'Direction' is drive generated. When false, the adapter data bus drivers assert their data bus levels and the drive data bus drivers assume a high impedance state. If true, the adapter assumes the high impedance state and the drive asserts its bus level.

IBM RT PC Streaming Tape Drive Adapter Signal Levels

All signals between the adapter and the tape drive are standard TTL levels and are active low.

IBM RT PC Streaming Tape Drive Adapter Signal Termination

The standard signal termination is 220 ohms to 5 Vdc and 330 ohms to ground. The bidirectional data bus and the four control signals from the adapter terminate at the drive. The bidirectional data bus and the drive control signals terminate at the adapter.

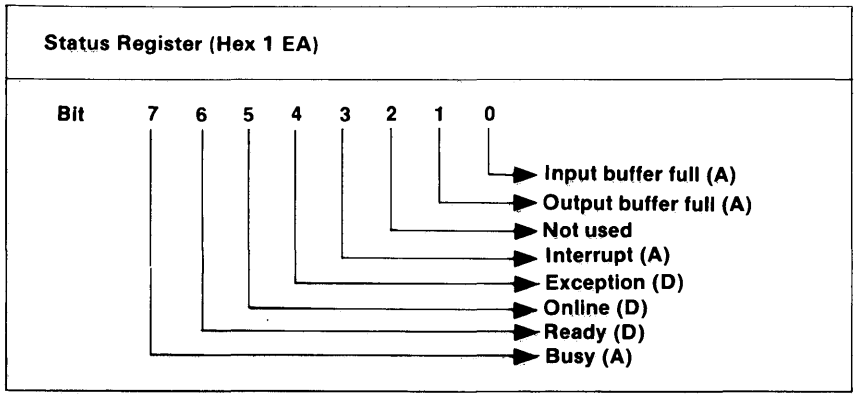
Programming Considerations

The following information describes the I/O addresses and commands used by the IBM RT PC Streaming Tape Drive Adapter.

I/O Address Assignments

Address	Read Mode	Write Mode
1E8	Sector Buffer	Sector Buffer
1EA	Status Register	Control Register
1EC	8042 Data Port	8042 Data Port
1EE	Reserved	8042 Command Port
6F4	Reserved	Interrupt Reset

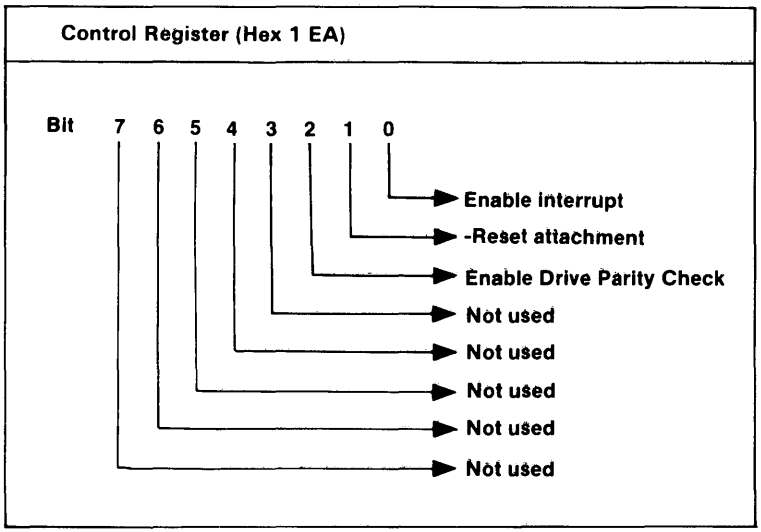
Status Register



Note: D = Drive Indicator; A = Attachment Generated

Input buffer full (IBF)	When data is sent to the 8042 the IBF signal is asserted indicating that the command or data register was loaded. When the register is read by the 8042, IBF goes false.
Output buffer full (OBF)	This signals the system that the 8042 loaded its register and is ready to transfer the data. Once the system reads the data OBF goes false.
Interrupt	The hardware interrupt signal is replicated here. After each command completes and when the sector buffer service is required, the 8042 interrupts the system.
Exception, Online, Ready	These signals are tape drive interface signals as seen by the attachment card.
Busy	Busy is asserted any time the 8042 has control of the internal data bus on the attachment card.

Control Register



Enable Interrupt This interrupt enables the tri-state driver for the hardware interrupt to the system.

- Reset Attachment This reset forces a hardware reset on the 8042. This causes the 8042 to execute its power-on diagnostics (PODs) and initiate handshake sequence with the system. Busy is on until the PODs are completed.

Enable Drive Parity Check
If the attached tape drive supports odd parity generation and checking on the data bus, the attachment also operates with parity when this bit is set.

Commands

The following is a list of commands supported by the streaming tape adapter board. The command port value (CPV) is written to the command port when giving the command.

Reset (hex 00)

This command resets the 8042 and starts the power-on diagnostics.

Drive Select (hex 01)

This command selects the drive to be used.

Rewind (hex 02)

This command positions the tape at the beginning of tape.

Erase (hex 03)

This command erases the entire tape.

Retension (hex 04)

This command cycles the tape from beginning of tape to the end and back again. This command should be performed when a new tape cartridge is inserted in the drive.

Read Status (hex 05)

This command reads status from the tape drive and presents it to the system.

Write Data (hex 06)

This command writes data on the tape.

Write File Mark (hex 07)

This command writes file marks on the tape.

Read Data (hex 08)

This command reads data from the tape.

Read File Mark (hex 09)

This command reads file marks from the tape.

Skip (hex 0C)

This command is used to skip blocks of data on the tape.

Terminate (hex 0D)

This command terminates a series of read or write commands.

Drive Self Test 1 (hex 0E)

This command causes the drive to perform a checksum calculation on its internal memory.

Drive Self Test 2 (hex 0F)

This command causes the drive to perform three checks:

1. Verifies capstan speed
2. Verifies beginning of tape, end of tape, and safe sensors
3. Writes worst case pattern on the tape and verifies it.

IBM RT PC Streaming Tape Drive Adapter Interface Specifications

The IBM RT PC Streaming Tape Drive Adapter has a 37-pin, D-shell connector at the rear of the adapter. The following figure shows the signals and their pin assignments.

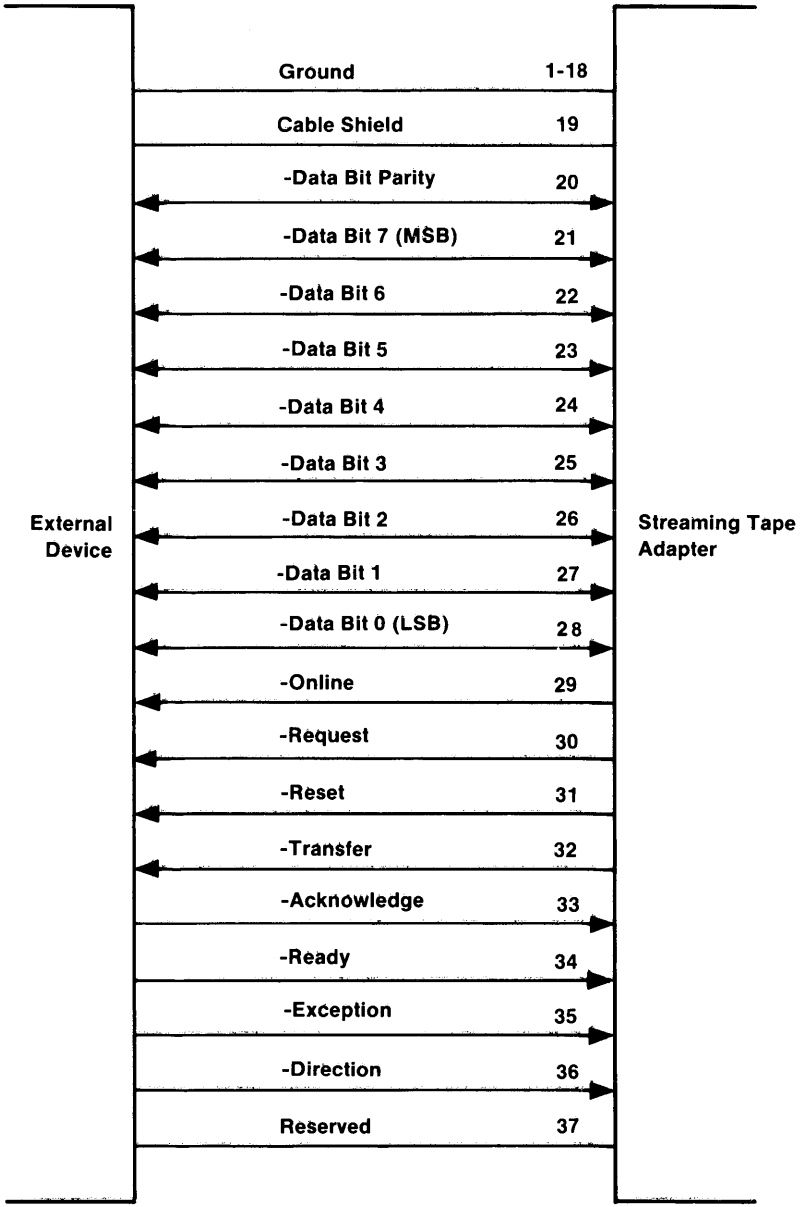
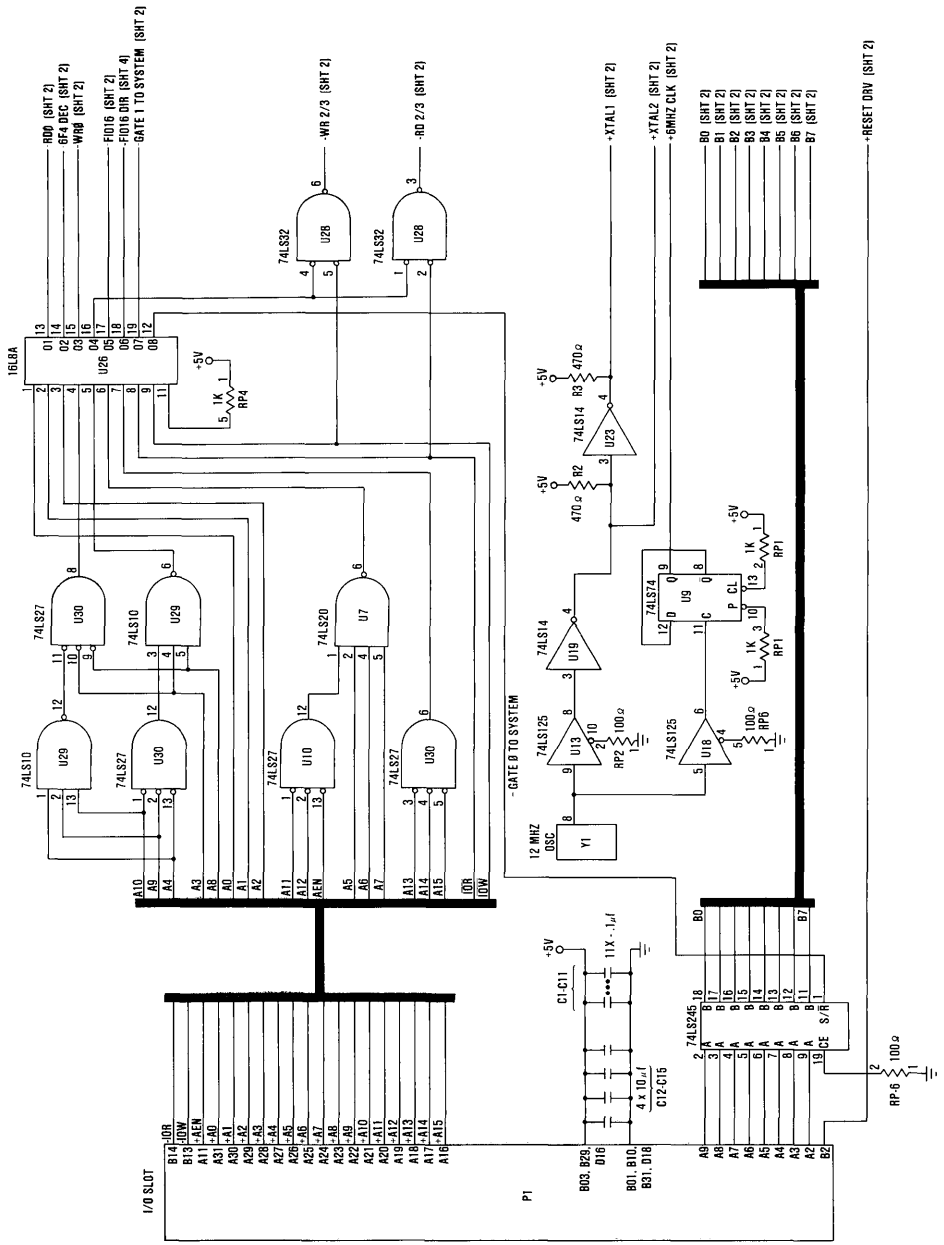


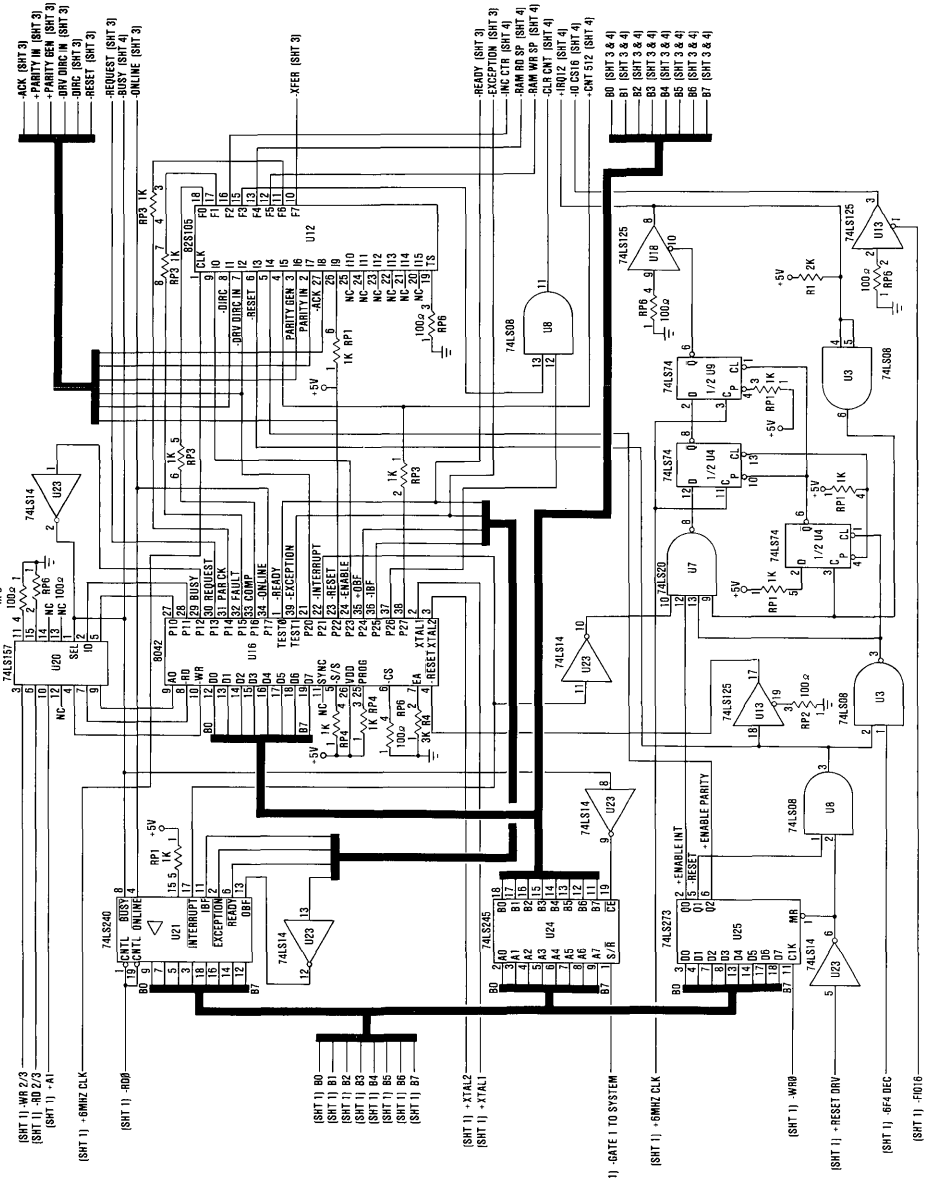
Figure 2. IBM RT PC Streaming Tape Drive Adapter Interface Specifications

Logic Diagrams

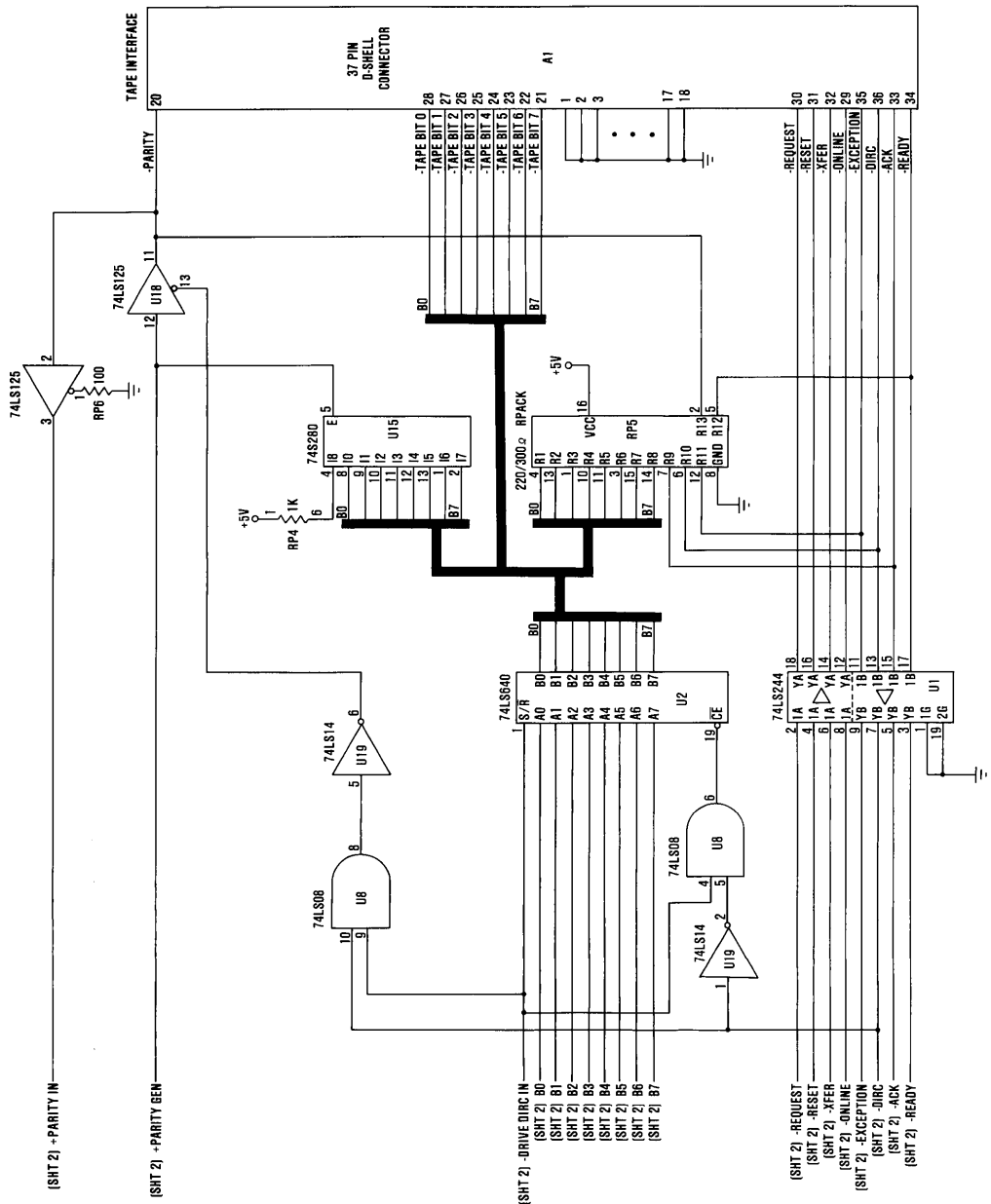
Sheet 1 of 4



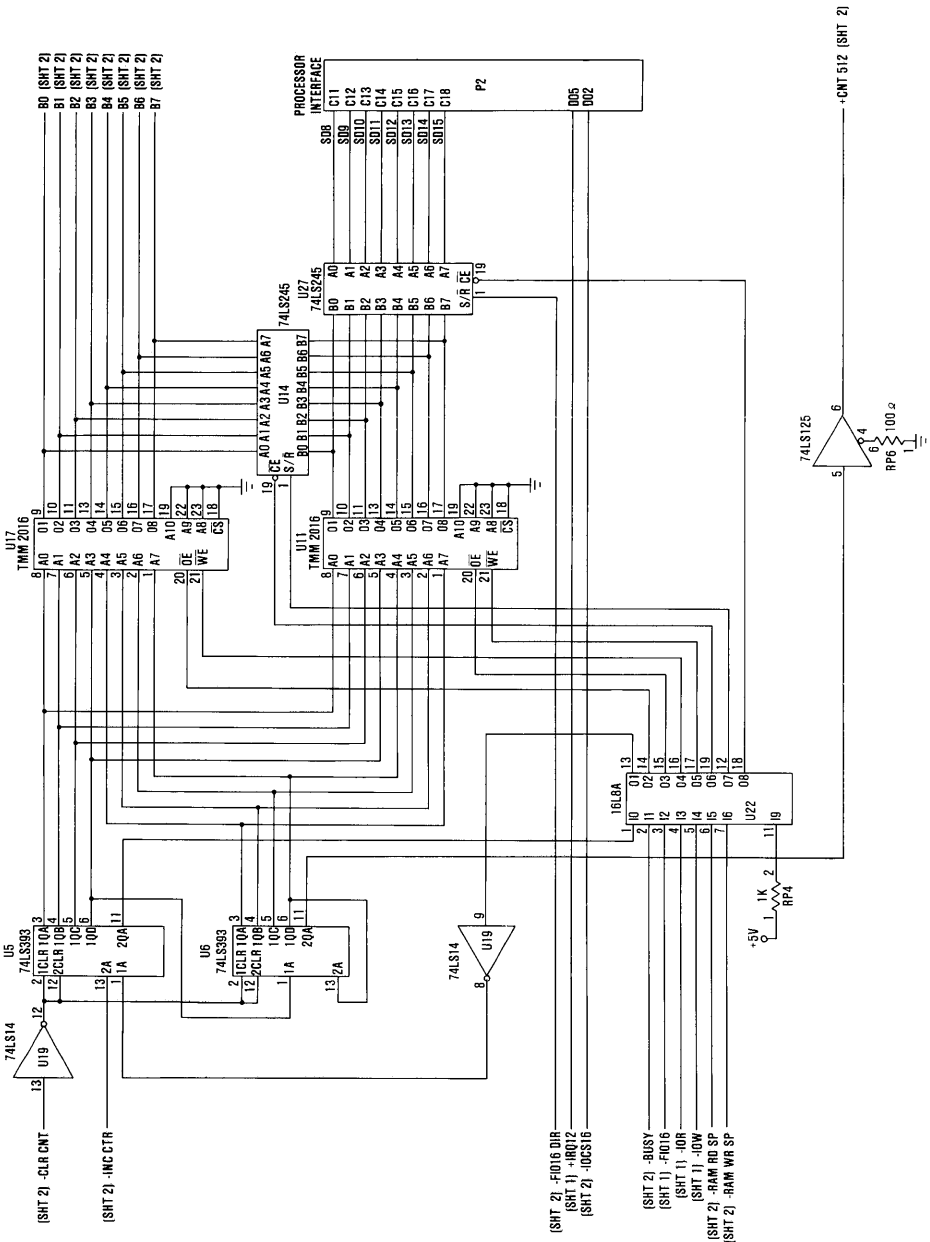
Sheet 2 of 4



Sheet 3 of 4


TAPE INTERFACE
37 PIN D-SHELL CONNECTOR
-PARITY
-TAPE BIT 0
-TAPE BIT 1
-TAPE BIT 2
-TAPE BIT 3
-TAPE BIT 4
-TAPE BIT 5
-TAPE BIT 6
-TAPE BIT 7
-REQUEST
-RESET
-XFER
-ONLINE
-EXCEPTION
-DIRC
-ACK
-READY
74LS125
74LS14
74LS08
74LS640
74LS244
74S280
RPACK
220/300Ω
RP4 1K
RP6 100
+5V
[SHT 2] +PARITY IN
[SHT 2] +PARITY GEN
[SHT 2] -DRIVE DIRC IN
[SHT 2] B0
[SHT 2] B1
[SHT 2] B2
[SHT 2] B3
[SHT 2] B4
[SHT 2] B5
[SHT 2] B6
[SHT 2] B7
[SHT 2] -REQUEST
[SHT 2] -RESET
[SHT 2] -XFER
[SHT 2] -ONLINE
[SHT 2] -EXCEPTION
[SHT 2] -DIRC
[SHT 2] -ACK
[SHT 2] -READY

Sheet 4 of 4


PROCESSOR INTERFACE
P2
U27 74LS245
U14 74LS245
U11 TMM 2016
U17 TMM 2016
U5 74LS393
U6 74LS393
U19 74LS14
U22 16L8A
74LS125
RP6 100Ω
RP4 1K
+5V
+CNT 512 [SHT 2]
[SHT 2] -CLR CNT
[SHT 2] -INC CTR
[SHT 2] -FIO16 DIR
[SHT 1] +IRQ12
[SHT 2] -IOCS16
[SHT 2] -BUSY
[SHT 1] -FIO16
[SHT 1] -IOR
[SHT 1] -IOW
[SHT 2] -RAM RD SP
[SHT 2] -RAM WR SP

IBM

Personal Computer Hardware Reference Library

40 MB Fixed Disk Drive

Contents

Description

The 40MB Fixed-Disk Drive is a direct access storage device using nonremovable 5.25-inch rigid disks. The drive uses a rotary voice-coil positioner that has a 40-millisecond average access time. The read/write heads automatically retract to a dedicated landing zone when power is turned off.

Interfaces

The interfaces of this drive are divided into three categories:

- Data transfer
- Control
- DC power.

The data transfer interface is a 20-pin printed circuit board (PCB) edge connector. The signals and pin assignments are as follows:

Signal Name	Pin
-Drive selected	1
+Write data	13
-Write data	14
+Read data	17
-Read data	18
Ground	2, 4, 6, 11, 12, 15, 16, 19, 20

Figure 1. Data Transfer Interface

The control interface is a 34-pin PCB connector. Figure 2 shows the signals and pin assignments.

Signal Name	Signal Pin	Gnd Pin
Head select 3	2	1
Head select 2	4	3
Write gate	6	5
Seek complete	8	7
Track 000	10	9
Write fault	12	11
Head Select 0	14	13
- Reserved -	16	15
Head select 1	18	17
Index	20	19
Ready	22	21
Step	24	23
Drive select 1	26	25
Drive select 2	28	27
Drive select 3	30	29
Drive select 4	32	31
Direction in	34	33

Figure 2. Control Interface

The dc power interface is a 4-pin female connector. The signals and pin assignments follow.

Signal Name	Pin
+12 Volts DC	1
+12 Volts Return	2
+5 Volts Return	3
+5 Volts DC	4

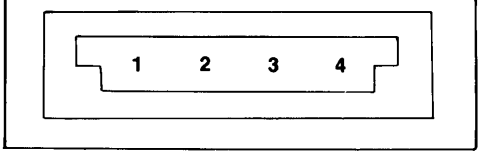


Figure 3. DC Power Interface

Input Control Signals

The control input signals have a removable terminator that can be unplugged when multiple drives operate multiplexed on the same control cable. These input signals have the following specifications.

- Active: 0.0 to 0.4 Vdc at 40 mA.
- Inactive: 2.5 to 5.25 Vdc at 0 mA.

The following are descriptions of the control input signals.

-Write Gate

When active, this signal allows writing of data on the disk. The inactive level allows reading of data from the disk, and allows the step pulse to move the heads.

-Head Select 0, 1, 2, and 3

These four signals enable the selection of each read/write head in a binary-coded sequence. 'Head Select 0' is the least significant. Heads are numbered 0 through F. When all head select signals are inactive, head 0 is selected.

-Direction In

This signal defines the direction the read/write heads move when 'Step' is pulsed. An inactive level defines the direction as out, and if a pulse is applied to '-Step', the read/write heads move away from the center of the disk. An active level defines the direction as in, and the read/write heads move toward the center of the disk.

-Step

This signal causes the read/write heads to move in the direction defined by the '-Direction In' signal. Any change in 'Direction In' is made at least 100 nanoseconds before the leading edge of the step pulse.

The adapter's controller may burst step pulses to the drive until the time after the last pulse exceeds 200 microseconds or the maximum number of step pulses is received (1 for each track). The drive starts motion of the heads after receiving the first step pulse. Step pulses are sent to the drive every 20 microseconds.

Two drives multiplexed on the same control cable may overlap seeking. An overlapped seek occurs when the first drive is deselected after the final step pulse is sent. The other drive is then selected and the '-Step' and '-Direction In' signals are set for the operation desired.

-Drive Select 2

When this signal is active, it multiplexes all data transfer and control signals of the interface cables. Only '-Drive Select 2' should be jumpered on a drive with multiple drive select capability.

Output Control Signals

An open-collector output stage, which is capable of sinking a maximum of 48 mA. at logical 0 to an active state with a maximum voltage of 0.4 Vdc at the driver, drives the output control signals. When the driver is at the inactive level, the driver's transistor is off and the collector's cutoff current is a maximum of 250 microamperes.

-Seek Complete

The '-seek complete' signal becomes active when the read/write heads settle on the final track at the end of a seek. Reading or writing is not attempted when '-Seek Complete' is inactive. '-Seek Complete' is inactive during:

- Seeking
- The power-on recalibration
- The time a drive problem makes the drive unready.

-Track 000

The '-track 000' signal is active when the drive's read/write heads are at the outermost track.

-Write Fault

The '-write fault' signal indicates that a condition at the drive is causing improper operation of the disk. An active level of this signal prevents further writing and seeking until the condition is reset.

-Index

The drive provides this output signal once each revolution to indicate the beginning of a track. This signal normally is inactive and goes active to indicate '-Index'. Only the change from inactive to active is valid (leading edge of the pulse).

-Ready

When the 'Ready' and '-Seek Complete' signals are active, the drive is ready to read, write, or seek, and the I/O signals are valid. An inactive level of this signal prevents all writing and seeking.

Data-Transfer Signals

All signals associated with the transfer of data between the drive and the system are differential (pairs of balanced signals) and are not multiplexed. Data is transferred at a rate of 5 million bits per second using MFM recording.

Two pairs of signals are used for the transfer of data: write data and read data. The following describes the data-transfer signals.

Write Data

'Write Data' is a differential pair that defines signal transitions written on the track. When '+ Write Data' goes more positive than '- Write Data', flux reverses on the track, provided that 'Write Gate' is active. The system drives '- Write Data' to an active level ('+ Write Data' more negative than '- Write Data') when in the read mode.

Read Data

'Read Data' is sent to the system through the differential pair of Read Data lines. The transition of '+ Read Data' going more positive than '- Read Data' represents a flux reversal on the track of the selected head.

Fixed Disk Requirements for Diagnostics

Diagnostics reserve the right to use portions of each installed fixed disk independent of the user installed operating system or hardware device drivers. The cylinder 0 format as described in the IBM RT PC Virtual Resource Manager Technical Reference must be honored. Also, the CE cylinder should never be used for customer data. It will be overwritten during diagnostic testing. The CE cylinder is the innermost cylinder of each fixed disk. Honoring these reservations avoids the destruction of data and allows the hardware to be serviced.

Specifications

The following figures list the internal and performance specifications of this drive.

Rotational speed	3600 rpm
Index	1
Start time	25 seconds (max.)

Figure 4. Internal Specifications

Formatted capacity	40M-bytes
Bytes per sector	512
Sectors per track	17
Transfer rate	5M bits per second
Latency (average)	8.3 ms
Access time: Track to track Average Maximum	 8 ms 40 ms 80 ms

Figure 5. Performance Specifications

Power Dissipation	30 Watts Average
Operating limits	Ambient temperature 10 to 50°C (50 to 122°F) Relative humidity 8 to 80 % Maximum wet bulb 26.7°C (80°F)
Non-operating limits	Ambient temperature -40 to 60°C (-40 to 140°F) Humidity no condensation
Mechanical dimensions	Width 146.0 mm (5.8 in) Height 82.5 mm (3.25 in) Depth 203.2 mm (8 in)
Weight	3.4 kg (7.5 lbs.)

Figure 6. Physical Specifications

IBM

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70MB Fixed Disk Drive

Contents

Description

The 70MB Fixed-Disk Drive is a direct access storage device using nonremovable 5.25-inch rigid disks. The drive uses a rotary voice-coil positioner that has a 40-millisecond average access time. The read/write heads automatically retract to a dedicated landing zone when power is turned off.

Interfaces

The interfaces of this drive are divided into three categories:

- DC power
- Data transfer
- Control.

The dc power interface is a 4-pin female connector. The signals and pin assignments follow:

Signal Name	Pin
+12 Volts DC	1
+12 Volts Return	2
+5 Volts Return	3
+5 Volts DC	4

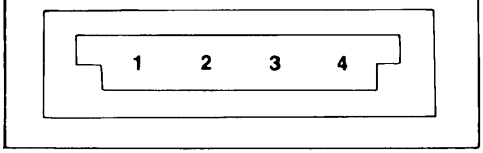

Figure 1. DC Power Interface

The data transfer interface is a 20-pin printed circuit board (PCB) edge connector. The signals and pin assignments are as follows:

Signal Name	Signal Pin	Gnd Pin
- Drive Selected	1	
- Sector	2	
- Command Complete	3	
Reserved	4	
Reserved	5	6
+ Write Clock	7	
- Write Clock	8	
Reserved	9	
+ Read/Reference Clock	10	
- Read/Reference Clock	11	12
+ NRZ Write Data	13	15
- NRZ Write Data	14	16
+ NRZ Read Data	17	
- NRZ Read Data	18	19
- Index	20	

Figure 2. Data Transfer Signal Lines (J2/P2)

The control interface is a 34-pin PCB connector. The table below shows the signals and pin assignments:

Signal Name	Signal Pin	Gnd Pin
- Head Select 2^3	2	1
- Head Select 2^2	4	3
- Write Gate	6	5
- Configuration/Status Data	8	7
- Transfer Acknowledge	10	9
- Attention	12	11
- Head Select 2^0	14	13
- Sector	16	15
- Head Select 2^1	18	17
- Index	20	19
- Ready	22	21
- Transfer Request	24	23
- Drive Select 1	26	25
- Drive Select 2	28	27
- Drive Select 3	30	29
- Read Gate	32	31
- Command Data	34	33

Figure 3. Control Signal Lines (J1/P1)

Input Control Signals

The input control signals have a removable terminator that can be unplugged when multiple drives operate multiplexed on the same control cable. The input signals are received by 74LS14 circuits. The following are descriptions of the input control signals.

Drive Select

'Drive Select' consists of three output lines from the controller which are decoded to select a single drive. When the drive select lines are all zero (inactive), no drive is selected. The decoding of these lines is shown below:

Drive Select 3	2	1	Drive Selected
0	0	0	None
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The drive address is set using option switches on the drive. Switches should be set to select drive 2.

Head Select

There are four head select lines (Head select 2^0, 2^1, 2^2, 2^3) which are decoded to select one of up to 16 heads. Head 2^0 is the least significant line. When all head select lines are inactive, head 0 is selected.

Since the file has a maximum of seven heads, the head select 2^3 line is not used internally, but it is properly terminated.

Transfer Request

Transfer Request is used as a handshake signal during command and configuration or status transfers.

Read Gate

The active level of this signal allows data to be read from the disk.

Write Clock

Write Clock is provided by the controller and must be at the bit data rate. This clock frequency is dictated by the Read/Reference Clock during the write operation.

NRZ Write Data

NRZ Write Data is a differential pair that writes data on the disk. The data is clocked by the Write Clock signal.

Command Data

When presenting a command, 16 information bits of serial data, plus parity is presented on this line. This data is controlled by the handshake protocol with the 'Transfer Request' and 'Transfer Acknowledge' signals. Data is transferred most significant bit first and utilizes odd parity.

The following table lists the drive commands:

Command	15 - 12	11 - 8	7 0
Request Status	0010	0000	xxxxxxxx
Request Unique Status	0010	xxxx	xxxxxxxx
Request Configuration	0011	0000	xxxxxxxx
Request Number of Fixed Cylinders	0011	0001	xxxxxxxx
Request Number of Heads	0011	0011	xxxxxxxx
Request Number of Bytes per Track	0011	0100	xxxxxxxx
Request Number of Bytes per Sector	0011	0101	xxxxxxxx
Request Number of Sectors per Track	0011	0110	xxxxxxxx
Request Number of ISG Bytes	0011	0111	xxxxxxxx
Request Number of PLO Sync Bytes	0011	1000	xxxxxxxx
Request Number of Unique Status Words	0011	1001	xxxxxxxx
Reset Attention and Status	0101	0000	xxxxxxxx
Stop Spindle Motor	0101	0010	xxxxxxxx
Start Spindle Motor	0101	0011	xxxxxxxx
Data Strobe Offset 0	0110	000x	xxxxxxxx
Data Strobe Offset 1 Early	0110	0010	xxxxxxxx
Data Strobe Offset 1 Late	0110	0011	xxxxxxxx
Data Strobe Offset 2 Early	0110	0100	xxxxxxxx

Figure 4 (Part 1 of 2). Commands

Command	15 - 12	11 - 8	7 0
Data Strobe Offset 2 Late	0110	0101	xxxxxxxx
Data Strobe Offset 3 Early	0110	0110	xxxxxxxx
Data Strobe Offset 3 Late	0110	0111	xxxxxxxx
Track Offset 0	0111	000x	xxxxxxxx
Track Offset +1	0111	0010	xxxxxxxx
Track Offset -1	0111	0011	xxxxxxxx
Track Offset +2	0111	0100	xxxxxxxx
Track Offset -2	0111	0101	xxxxxxxx
Track Offset +3	0111	0110	xxxxxxxx
Track Offset -3	0111	0111	xxxxxxxx
Seek	0000	Cylinder	
Recalibrate	0001	xxxx	xxxxxxxx
Initiate Diagnostics	1000	xxxx	xxxxxxxx

Figure 4 (Part 2 of 2). Commands

Output Control Signals

The output signals have the following specifications:

- Active: 0.0 to 0.4 Vdc at 48mA.
- Inactive: 2.5 to 5.25 Vdc at 250 uA.

The following are descriptions of the output control signals:

Drive Selected

Drive Selected indicates the selection status of the drive. This line goes active only when the Drive Select lines match the drive address.

Transfer Acknowledge

Transfer Acknowledge is a response to the 'Transfer Request' signal during command and configuration or status transfers.

Configuration/Status Data

Configuration or status data is presented to the interface and transferred using the handshake protocol with the 'Transfer Request' and 'Transfer Acknowledge' signals. The 16 bits of configuration data is shown in Figure 5 on page 9.

Bit	Value	Description
15	0	Tape Drive
14	1	Format Speed Tolerance Gap Required
13	1	Track Offset Option Available
12	1	Data Strobe Offset Option Available
11	0	Rotational Speed Tolerance is >0.5%
10	0	Transfer Rate >10 Mhz
9	1	Transfer Rate >5 Mhz <10 Mhz
8	0	Transfer Rate <5 Mhz
7	0	Removable Cartridge Drive
6	1	Fixed Drive
5	0	Spindle Motor Control Option Implemented
4	0	Head Switch Time >15usec.
3	1	RLL Encoded (Not MFM)
2	0	Controller Soft Sectored (Address Mark)
1	1	Drive Hard Sectored (Sector Pulses)
0	0	Controller Hard Sectored (Byte Clock)

Figure 5. Configuration Data Bits

The 16 bits of status data is shown in Figure 6.

Bit	Value	Description
15	0	Reserved
14	0	Removable Media Not Present
13	0	Write Protected, Removable Media
12	0	Write Protected, Fixed Media
11	0	Reserved
10	0	Reserved
9	X	Spindle Motor Stopped
8	X	Power On Reset Conditions Exist
7	X	Command Data Parity Fault
6	X	Interface Fault
5	X	Invalid or Unimplemented Command Fault
4	X	Seek Fault
3	X	Write Gate with Track Offset Fault
2	X	Unique Status Available
1	X	Write Fault
0	0	Removable Media Changed

Figure 6. Status Data Bits

Command Complete

Command Complete allows the controller to monitor the drive's command complete status, during overlapped commands, without selecting the drive. This signal is inactive during the following cases:

- At power on
- Upon receipt of the first command data bit. Command Complete stays inactive during the entire command sequence.

Ready

Ready indicates that the spindle is up to speed. When this signal and Command Complete are active, and Attention is inactive the file is ready to read, write, or seek. When Ready is inactive, all writing and seeking is inhibited.

Attention

Attention signals the controller when the drive has a fault condition or a change in status. Writing is inhibited when Attention is active. Attention is deactivated by the Reset Interface Attention command.

Index

The drive provides this output signal once each revolution to indicate the beginning of a track. This signal normally is inactive and goes active to indicate -Index. Only the change from inactive to active is valid (leading edge of the pulse). The nominal period of this signal is 16.7 milliseconds.

Sector

The drive provides this output signal to indicate the start of a sector. This signal normally is inactive and goes active to indicate -Sector. Only the change from inactive to active is valid (leading edge of the pulse).

Read/Reference Clock

Read/Reference Clock provides the read clock when Read Gate is active and a reference clock when Read Gate is inactive. After Read Gate is activated, Read Clock may not be within tolerance until PLO synchronization is established. The transitions between Read Clock and Reference Clock are performed without glitches, but up to two missing clock cycles may occur.

NRZ Read Data

NRZ Read Data is a differential pair that reads previously written data from the disk. This data is clocked by the Read Clock signal. These lines are held inactive until PLO synchronization is established and data is valid.

Fixed Disk Requirements for Diagnostics

Diagnostics reserve the right to use portions of each installed fixed disk independent of the user installed operating system or hardware device drivers. The cylinder 0 format as described in the IBM RT PC Virtual Resource Manager Technical Reference must be honored. Also, the CE cylinder should never be used for customer data. It will be overwritten during diagnostic testing. The CE cylinder is the innermost cylinder of each fixed disk. Honoring these reservations avoids the destruction of data and allows the hardware to be serviced.

Specifications

The following figures list the internal and performance specifications of this drive:

Rotational speed	3600 rpm
Index	1
Start time	50 seconds (max)

Figure 7. Internal Specifications

Formatted capacity	70M-bytes
Bytes per sector	512
Cylinders	566
Heads	7
Sectors per track	36
Transfer rate	10M bits per second
Latency (average)	8.3 ms
Access time: Track to track Average Maximum	 8 ms 40 ms 70 ms

Figure 8. Performance Specifications

Power dissipation	30 watts average
Operating limits	Ambient temperature 10 to 50°C (50 to 122°F) Relative humidity 8 to 80% Maximum wet bulb 26.7°C (80°F)
Non-operating limits	Ambient temperature -40 to 60°C (-40 to 140°F) Humidity no condensation
Mechanical dimensions	Width 146.0 mm (5.8 in) Height 82.5 mm (3.25 in) Depth 203.2 mm (8 in)
Weight	3.4 kg (7.5 lbs.)

Figure 9. Physical Specifications

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Double Sided Diskette Drive

Contents

Notes:

Description

The Double Sided Diskette Drive is a direct-access device that can store 320/360Kb of data on a dual-sided 5-1/4 inch diskette. All data format and access control is in the system. The following figure describes the type of diskette required by this drive.

Characteristic	Requirement
Certification	Double sided 48 TPI 40 tracks per surface Soft Sector
Recording density	5,876 bits per inch
Media coercivity	300 to 350 Oersteds
Jacket	Standard 5-1/4 inch

Diskette Requirements

The signals for operating the diskette drive are generated through the IBM Personal Computer AT Fixed Disk and Diskette Drive Adapter.

Interfaces

The diskette drive has two types of interface: control and dc power. The following figure shows the signals and pin assignments for the control interface.

Signal Name	I/O	Signal Pin	Ground Pin
Reserved	-	2	1
Reserved	-	4	3
-Drive Select 3	I	6	5
-Index	O	8	7
-Drive select 0	I	10	9
-Drive select 1	I	12	11
-Drive select 2	I	14	13
-Motor On	I	16	15
-Direction Select	I	18	17
-Step	I	20	19
-Write Data	I	22	21
-Write Gate	I	24	23
-Track 00	O	26	25
-Write Protect	O	28	27
-Read Data	O	30	29
-Side 1 Select	I	32	31
Reserved	-	34	33

Control Interface (P1/J1)

Following are the signals and pin assignments for the dc power interface.

Signal Name	Pin
+ 12 Vdc	1
+ 12 Vdc Return	2
+ 5 Vdc Return	3
+ 5 Vdc	4

Power Interface (P2/J2)

All signals operate between +5 Vdc and ground with the following definitions:

Inactive Level: +2.5 to +5.25 Vdc

Active Level: 0.0 to +0.4 Vdc

All outputs from the drive can sink 40 mA at the active level. The system provides pull-up registers.

Input Signals

All input signals are active when low.

Drive Select 0 through 3

These 'drive select' signals enable or disable all other drive interface signals, except 'motor on'. When 'drive select' is at the active level, the drive is enabled. When it is at the inactive level, all controlled inputs are ignored, and all drive outputs are disabled. The enabled or disabled condition of the drive is established within 500 nanoseconds after a change to the select input, excluding head-load time and settling times.

-Motor On

An active level of this signal starts the drive motor. There must be a 750 millisecond delay after '-motor on' becomes active before any read or write operation starts.

-Direction Select

This signal determines the direction the read/write head moves when the step signal is pulsed. An active level indicates away from the center of the diskette (out); an inactive level indicates toward the center of the diskette (in). Any change in the 'direction select' signal must be made at least 1 microsecond before the leading edge of the step pulse, and at least 1 microsecond after the trailing edge of the step pulse.

-Step

This signal causes the read/write heads to move in the direction determined by the 'direction select' signal. Motion is started each time the signal changes from an active to inactive level (at the trailing edge of the pulse).

-Write Data

Each time this signal changes from the inactive to inactive level, the current through the read/write heads reverses, thereby writing

a data bit. This signal is enabled when 'write gate' is at the active level.

-Write Gate

A 250-nanosecond active pulse of this signal causes a bit to be written on the diskette. These pulses may occur with either a 4, 6, or 8-microsecond spacing (±0.5%). After deactivating 'write gate', deactivation of 'drive select' and 'motor on', and changing 'side select' must be delayed 1 millisecond, because the erase head is active for this period.

-Side 1 Select

This signal determines which side of the two-sided diskette will be used for reading or writing. An inactive level of this signal selects the read/write head on the 0 side of the diskette; an active level selects the 1 side. A 100-microsecond delay must be allowed after switching from one head to the other before starting to read or write.

Output Signals

-Index

When the drive senses the index hole in the diskette, it generates a 1- to 8-microsecond active pulse on this line.

-Track 00

An active level of this signal means that the read/write heads are at Track 0 (the outermost track).

-Write Protect

An active level of this signal means that a diskette without a write-protect notch is in the drive. The drive will not write when a protected diskette is loaded.

-Read Data

A 250-nanosecond active pulse is provided on this line for each bit detected on the diskette. These pulses may occur with either 4, 6, or 8-microsecond spacing.

Specifications

The following figures show the physical, and performance specifications for this drive.

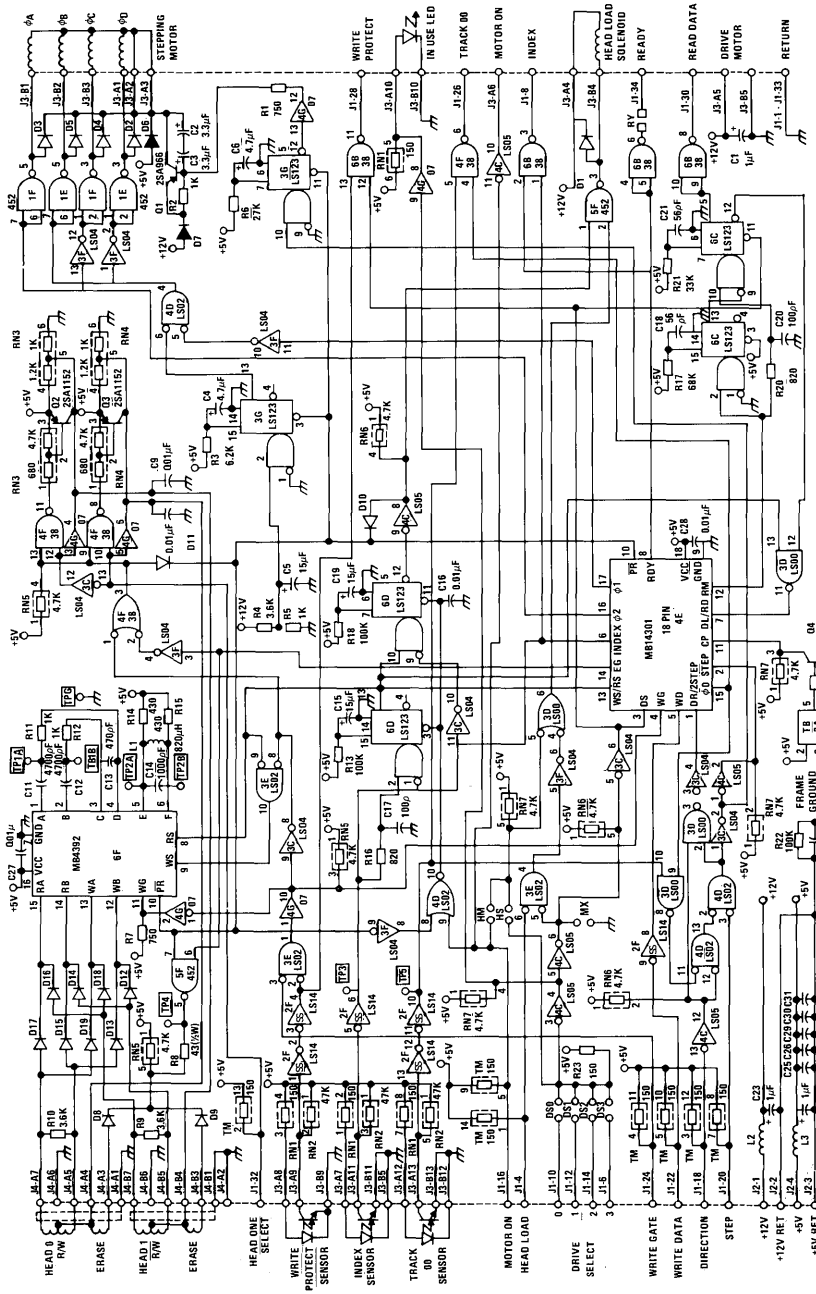
Power Dissipation	11 W (Typical)
Operating Limits	
Ambient Temperature	10 to 50 Degrees C (41 to 114.8 Degress F)
Relative Humidity	8 to 80%
Maximum Wet Bulb	26.7 Degrees C (84 Degrees F)
Non-Operating Limits	
Ambient Temperature	-40 to 60 Degrees C (-40 to 140 Degrees F)
Humidity	No Condensation
Mechanical Dimensions	
Width	146.0 mm (5.8 in.)
Height	41.0 mm (1.6 in.)
Depth	203.2 mm (8.0 in.)
Weight	1.6 kg (3.52 pounds)

Physical Specifications

Capacity Unformatted	500 Kb
Capacity Formatted	
9 Sectors Per Track	368.6Kb
8 Sectors Per Track	320.0Kb
Recording density	5,876 bits per inch
Track Density	48 TPI(tracks per inch)
Cylinders	40
Tracks	80
Encoding Method	MFM
Rotational Speed	300 RPM ± 1.5%
Transfer Rate	250K bits per second
Latency (Average)	100 ms
Access Time:	
Average	81 ms
Track to Track	6 ms
Settling Time	15 ms
Head Load Time	0 ms
Motor Start Time	500 ms

Performance Specifications

Logic Diagrams



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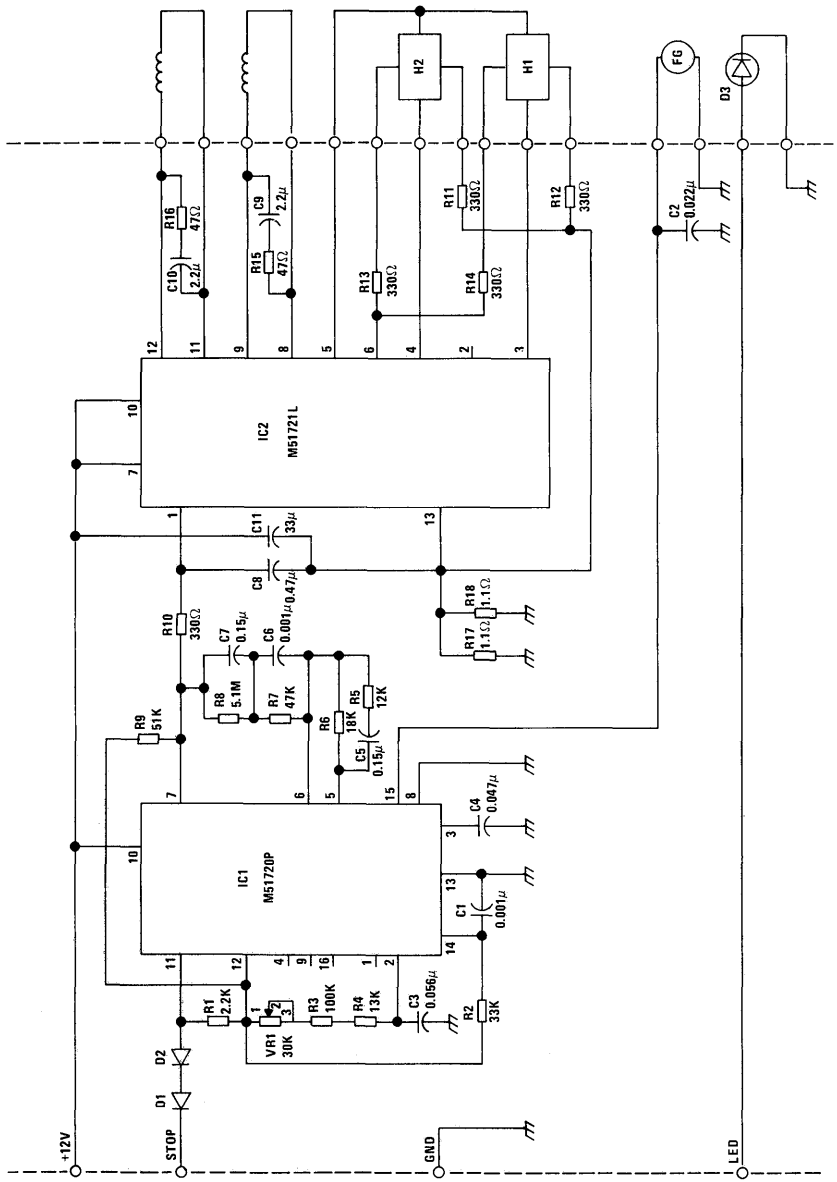

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8 Double Sided Diskette Drive

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High Capacity Diskette Drive

Contents

Notes:

Description

The IBM Personal Computer AT High Capacity Diskette Drive is a direct-access device that can store 1.2Mb of data on a dual-sided 5-1/4 inch diskette. All data format and access control is in the system. The following figure describes the type of high-density diskette required by this drive. Diskettes, which meet these specifications may not be used in either a 160/180Kb or a 320/360Kb diskette drive.

Characteristic	Requirement
Certification	Double sided 96 TPI 80 tracks/surface Soft sector
Recording density	9,646 bits per inch
Media coercivity	600 to 650 Oersteds
Jacket	Standard 5-1/4 inch

Diskette Requirements

The signals for operating the diskette drive are generated through the IBM Personal Computer AT Fixed Disk and Diskette Drive Adapter.

> **Note:** This drive also can read diskettes formatted for a 320/360Kb dual-sided drive or a 160/180Kb single-sided drive.

Interfaces

The diskette drive has two types of interface: control and dc power. The following show the signals and pin assignments for the control interface.

Signal Name	I/O	Signal Pin	Ground Pin
-Reduced write	I	2	1
Reserved	-	4	3
-Drive select 3	I	6	5
-Index	O	8	7
-Drive select 0	I	10	9
-Drive select 1	I	12	11
-Drive select 2	I	14	13
-Motor on	I	16	15
-Direction select	I	18	17
-Step	I	20	19
-Write data	I	22	21
-Write gate	I	24	23
-Track 00	O	26	25
-Write protect	O	28	27
-Read data	O	30	29
-Side 1 select	I	32	31
-Diskette change	O	34	33

Control Interface (P1/J1)

The signals and pin assignments for the dc power interface are as follows:

Signal Name	Pin
+12 Vdc	1
+12 Vdc return	2
+5 Vdc return	3
+5 Vdc	4

DC Power Interface (P2/J2)

All signals operate between +5 Vdc and ground with the following definitions:

Inactive Level: +2.5 to +5.25 Vdc

Active Level: 0.0 to +0.4 Vdc

All outputs from the drive can sink 40 mA at the active level. The system provides pull-up registers.

Input Signals

Following are descriptions of the input signals.

-Reduced Write

The inactive state of this signal indicates that high-density media is present requiring normal write currents, and the active state indicates low-density media is present, requiring a reduced write current.

-Drive Select 0, 1, 2, and 3

The Drive Select signals enable or disable all other drive interface signals, except 'motor on'. When 'drive select' is at the active level, the drive is enabled. When it is at the inactive level, all controlled inputs are ignored, and all drive outputs are disabled. The enabled or disabled condition of the drive is established within 500 nanoseconds after a change to the select input, excluding head-load time and settling time.

-Motor On

The spindle motor runs when this input is active. The drive requires a 1 second delay after '-motor on' becomes active before a read or write operation.

-Direction Select

If this input is at a inactive level the 'step' input signal moves the heads away from the drive spindle. An active level causes the opposite. This input is stable for a minimum of 1 microsecond before and after the trailing edge of the step pulse.

-Step

A 1-microsecond active pulse on this input causes the read/write heads to move one track. The state of '-Direction Select' at the trailing edge of the Step pulse determines the direction of motion.

-Write Data

A 150-nanosecond pulse on this input causes a bit to be written on the disk if Write Gate is active. These pulses may occur with either a 2, 3, 3.3, 4, 5, or 6.67-microsecond spacing ±0.5 %. When Write Gate is inactive, pulses do not appear on this input.

-Write Gate

An active level of this input enables the write current circuits, and the Write Data input controls the writing of information. Transitions of this line occur 4 to 8 microseconds before the first significant data bit, and 4 to 8 microseconds after the last significant data bit. Making this input inactive removes all current from the read/write heads and allows the read circuits to operate within 590 microseconds All motor-start, head-settle, and head-load times are complied with before the line becomes active.

-Side 1 Select

Making this input active selects the upper head; otherwise the lower head is selected.

Output Signals

Following are descriptions of the output signals.

-Index

When a diskette's index hole aligns with the hole in the diskette jacket, a 1- to 8-microsecond active pulse is generated on this line.

-Track 00

This signal is active when the upper head is on Track 00.

-Write Protect

This output is active when a diskette without a write-protect notch is inserted. It prevents the erasing or writing of data.

-Read Data

Each bit detected provides a 150-nanosecond active pulse on this line. These pulses may occur with either a 2, 3, 3.33, 4, 5, or 6.67-microsecond spacing ±0.5%.

-Diskette Change

This output is active unless a diskette is present and a step pulse is received when the drive is selected.

Power Sequencing

The 'write gate' signal is turned off and is kept off before power is switched on or off. The read/write heads return to Track 00 when the system power is switched on.

Drive-in-Use Indicator

The Drive-in-Use indicator lights when the drive is selected.

Specifications

The following figures show the performance, physical, and performance specifications for this drive.

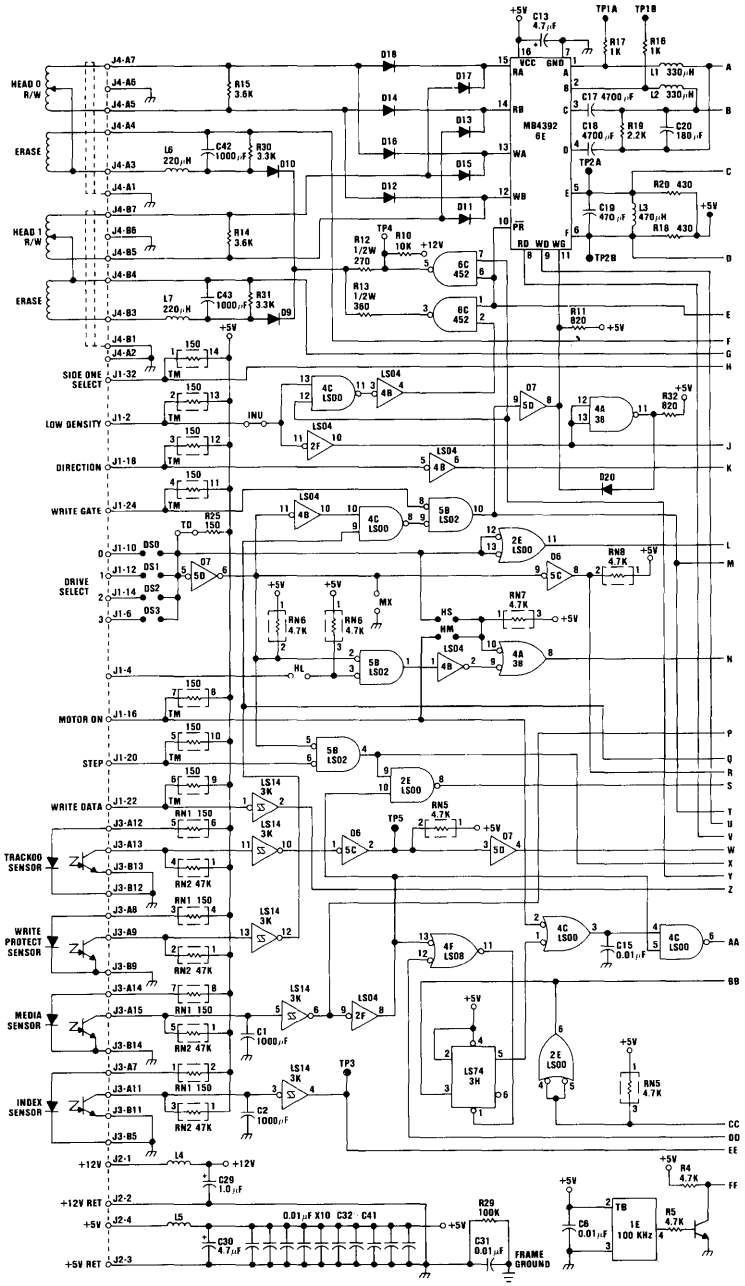
Power dissipation	11 W (TYP)
Operating limits	Ambient temperature 5 to 46 degrees Celsius (41 to 114.8 degrees Farenheit) Relative humidity 20 to 80 % Maximum wet bulb 29 degrees Celsius (84 degrees Farenheit)
Non-operating limits	Ambient temperature -40 to 60 degrees Celcius (-40 to 140 degrees Farenheit) Humidity no condensation
Mechanical dimensions	Width 146.0 mm (5.8 in) Height 41.0 mm (1.6 in) Depth 203.2 mm (8 in)
Weight	1.6 kg

Physical Specifications

Capacity unformatted	1604Kb
Capacity formatted	
15 sectors per track	1.2Mb
Recording density	9646 bits per inch
Track density	96 TPI
Cylinders	80
Tracks	160
Encoding method	MFM
Rotational speed	360 RPM
Transfer rate	500K bits/second
Latency (average)	83 ms
Access time	
Average	91 ms
Track to track	3 ms
Settling time	18 ms
Head load time	50 ms
Motor start time	750 milliseconds

Performance Specifications

Logic Diagrams



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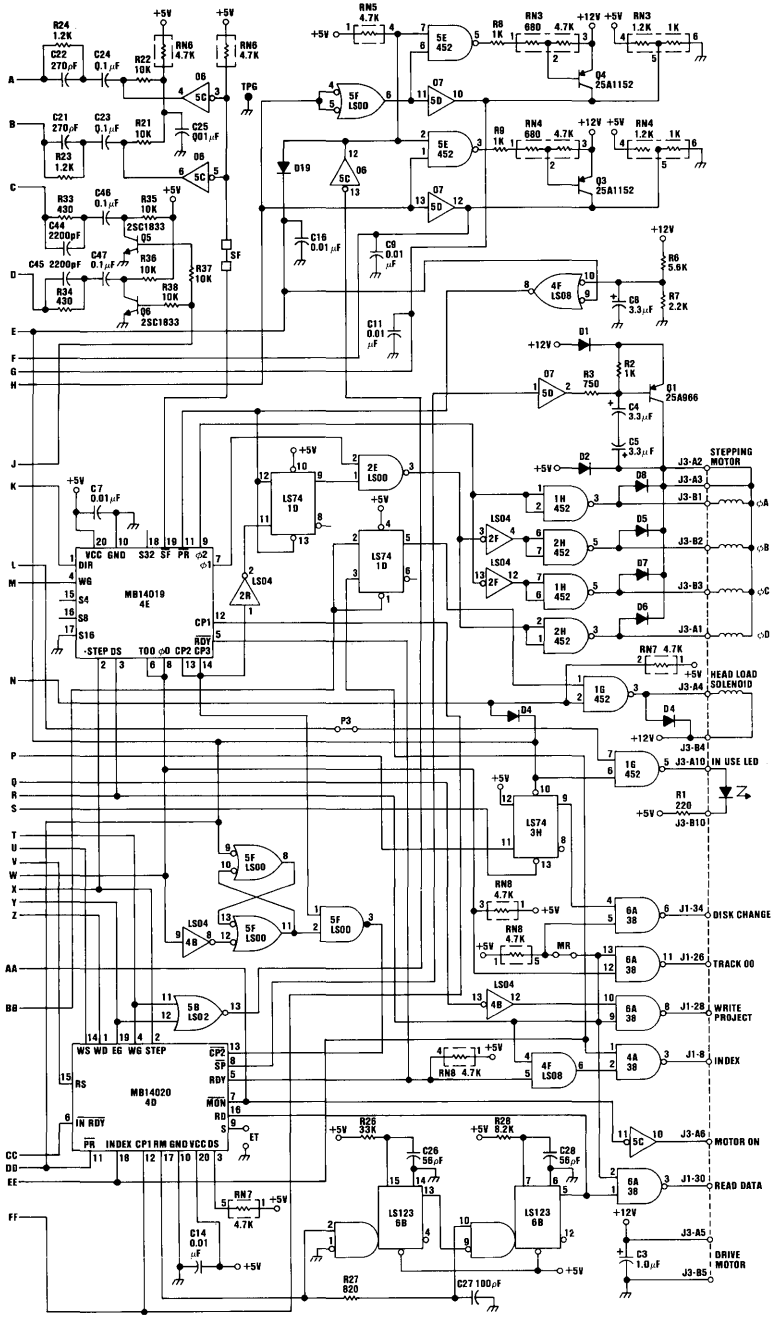

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Streaming Tape Drive

Contents

Description

The tape subsystem contains a 1/4-inch streaming cartridge tape drive, a power supply, and associated components. The streaming tape drive consists of read/write, control and motor drive electronics, a tape transport mechanism, and head stepping assembly. These components perform the following functions:

- Interpret and generate interface control signals
- Automatically position the read/write head to the proper track
- Format, read, and write data
- Monitor and control tape speed
- Provide data error detection and correction.

The IBM RT PC Streaming Tape Drive Adapter board controls the subsystem. All commands from the system pass through the adapter board.

Control Interface

The control interface lines for the tape subsystem are carried by a 6 foot black signal cable which enters the rear of the subsystem. The cable attaches to the IBM RT PC Streaming Tape Drive Adapter card with the 37-pin D-shell connector on the end of the cable. The cable pin assignments are shown in Figure 1 on page 2.

Signal Name	Signal Pin	Gnd Pin
Cable shield	19	1
Parity Bit (Odd)	20	2
Bit 7	21	3
Bit 6	22	4
Bit 5	23	5
Bit 4	24	6
Bit 3	25	7
Bit 2	26	8
Bit 1	27	9
Bit 0	28	10
On line	29	11
Request	30	12
Reset	31	13
Transfer	32	14
Acknowledge	33	15
Ready	34	16
Exception	35	17
Direction	36	18
Reserved	37	

Figure 1. Control Interface Lines

Power

The subsystem has its own AC line cord that must be plugged into an electrical wall outlet.

Specifications

The following figures show the physical and performance specifications for the subsystem.

Signal interface	QIC-02 industry standard
Data format	QIC-24 industry standard
Capacity	55M-bytes
Recording density	10000 flux changes per inch
Transfer rate	86.7K bits per second
Tape speed	90 inches per second
Internal data buffer	2K-bytes

Figure 2. Performance Specifications

AC power	50-60 Hz, 90-137 Volts RMS 100 watts
Operating limits	Ambient temperature 5 to 40°C (41 to 104°F) Relative humidity 20 to 80 %
Nonoperating limits	Ambient temperature -10 to 60°C (-40 to 140°F) Relative humidity 8 to 80%
Mechanical dimensions	Width 144.0 mm (5.75 in) Height 221.2 mm (8.75 in) Depth 387.3 mm (15.25 in)

Figure 3. Physical Specifications

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