82365SL
PC CARD INTERFACE CONTROLLER (PCIC)

- **Designed for Use in Notebooks which Implement either an 8-Bit or 16-Bit External System Bus.**
  - **— ExCA™ Implementation of ISA Bus to PCMCIA 2.0 /JEIDA 4.1 Interface**
- **Each PCIC Supports Two PCMCIA 2.0 / JEIDA 4.1 68-pin Standard PC Card Sockets**
  - **— Cascadable up to Eight Sockets**
  - **— Each Socket Interchangeably Supports either Memory or I/O PC Cards**
- **System Bus Timings Compatible with Intel386™ SL Microprocessor SuperSet**
  - **— Direct Support for Most Integrated EISA/ISA Chipsets**
  - **— Easily Configured to Support Other Standard Architectures**
- **Power Management Support**
  - **— Individual Socket Power Control**
  - **— Insertion/Removal Capability**
- **Eliminates Need for System Configuration Jumpers**
  - **— Address Mapping Support for PCMCIA 2.0 /JEIDA 4.1 PC Card Memory and Address Windowing Support for I/O Space**
  - **— Selectable Interrupt Steering from PC Card to System Bus**
- **160-Pin JEDEC QFP Package**
  (See Packaging Specifications Order Number 240800-001.)

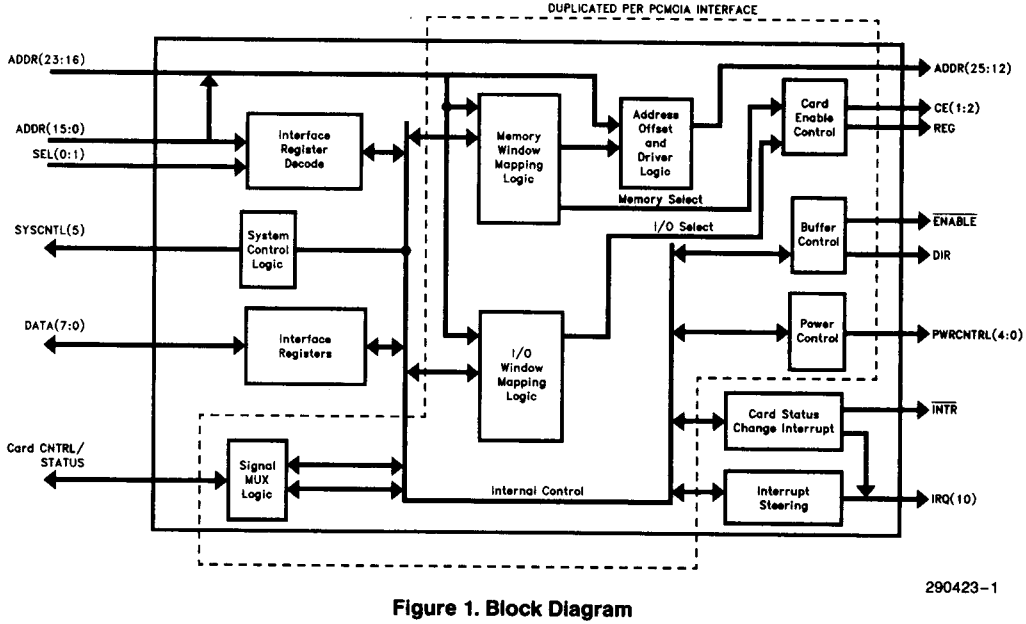

Figure 1. Block Diagram

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Order Number: 290423-001

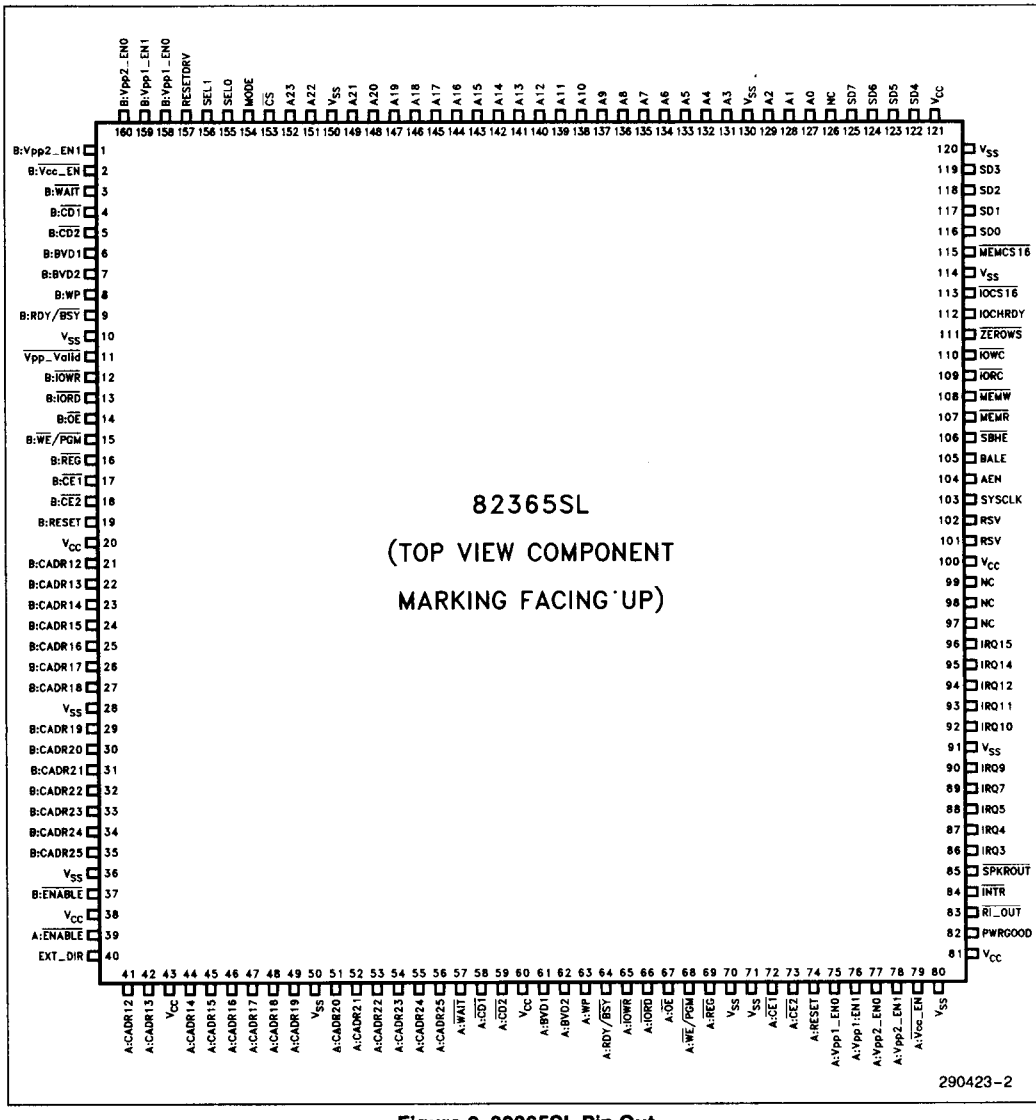

Figure 2. 82365SL Pin Out

PIN ASSIGNMENT

Pin Cross Reference by Pin Name

1	B: V_{PP2}_EN1
2	B: $\overline{V_{CC}}$_$\overline{EN}$
3	B: $\overline{WAIT}$
4	B: $\overline{CD1}$
5	B: $\overline{CD2}$
6	B: BVD1 (B: $\overline{STSCHG}$/ B: $\overline{RI}$)
7	B: BVD2 (B: $\overline{SPKR}$)
8	B: WP (B: $\overline{IOIS16}$)
9	B: RDY/$\overline{BSY}$ (B: $\overline{IREQ}$)
10	V_{SS}
11	$\overline{V_{PP}}$_Valid
12	B: $\overline{IOWR}$
13	B: $\overline{IORD}$
14	B: $\overline{OE}$
15	B: $\overline{WE}$/$\overline{PGM}$
16	B: $\overline{REG}$
17	B: $\overline{CE1}$

18	B: $\overline{CE2}$
19	B: RESET
20	V_{CC}
21	B: CADR12
22	B: CADR13
23	B: CADR14
24	B: CADR15
25	B: CADR16
26	B: CADR17
27	B: CADR18
28	V_{SS}
29	B: CADR19
30	B: CADR20
31	B: CADR21
32	B: CADR22
33	B: CADR23
34	B: CADR24
35	B: CADR25
36	V_{SS}
37	B: $\overline{ENABLE}$
38	V_{CC}

39	A: $\overline{ENABLE}$
40	EXT_DIR
41	A: CADR12
42	A: CADR13
43	V_{CC}
44	A: CADR14
45	A: CADR15
46	A: CADR16
47	A: CADR17
48	A: CADR18
49	A: CADR19
50	V_{SS}
51	A: CADR20
52	A: CADR21
53	A: CADR22
54	A: CADR23
55	A: CADR24
56	A: CADR25
57	A: $\overline{WAIT}$
58	A: $\overline{CD1}$
59	A: $\overline{CD2}$

60	V_{CC}
61	A: BVD1 (A: $\overline{STSCHG}$/ A: $\overline{RI}$)
62	A: BVD2 (A: $\overline{SPKR}$)
63	A: WP (A: $\overline{IOIS16}$)
64	A: RDY/$\overline{BSY}$ (A: $\overline{IREQ}$)
65	A: $\overline{IOWR}$
66	A: $\overline{IORD}$
67	A: $\overline{OE}$
68	A: $\overline{WE}$/$\overline{PGM}$
69	A: $\overline{REG}$
70	V_{SS}
71	V_{SS}
72	A: $\overline{CE1}$
73	A: $\overline{CE2}$
74	A: RESET
75	A: V_{PP1}_EN0
76	A: V_{PP1}_EN1

PIN ASSIGNMENT (Continued)

Pin Cross Reference by Pin Name (Continued)

77	A: V_{PP2}_EN0	98	NC	119	SD3	140	A12
78	A: V_{PP2}_EN1	99	NC	120	V_{SS}	141	A13
79	A: $\overline{V_{CC}}$_$\overline{EN}$	100	V_{CC}	121	V_{CC}	142	A14
80	V_{SS}	101	Reserved	122	SD4	143	A15
81	V_{CC}	102	Reserved	123	SD5	144	A16
82	PWRGOOD	103	SYSCLK	124	SD6	145	A17
83	$\overline{RI\ OUT}$	104	AEN	125	SD7	146	A18
84	$\overline{INTR}$	105	BALE	126	NC	147	A19
85	$\overline{SPKROUT}$	106	$\overline{SBHE}$	127	A0	148	A20
86	IRQ3	107	$\overline{MEMR}$	128	A1	149	A21
87	IRQ4	108	$\overline{MEMW}$	129	A2	150	V_{SS}
88	IRQ5	109	$\overline{IORC}$	130	V_{SS}	151	A22
89	IRQ7	110	$\overline{IOWC}$	131	A3	152	A23
90	IRQ9	111	$\overline{ZEROWS}$	132	A4	153	$\overline{CS}$
91	V_{SS}	112	IOCHRDY	133	A5	154	MODE
92	IRQ10	113	$\overline{IOCS16}$	134	A6	155	SEL0
93	IRQ11	114	V_{SS}	135	A7	156	SEL1
94	IRQ12	115	$\overline{MEMCS16}$	136	A8	157	RESETDRV
95	IRQ14	116	SD0	137	A9	158	B: V_{PP1}_EN0
96	IRQ15	117	SD1	138	A10	159	B: V_{PP1}_EN1
97	NC	118	SD2	139	A11	160	B: V_{PP2}_EN0

NOTE:
Pins 102 (RSV) and 101 (RSV) must be pulled up. A 10 KΩ is recommended.

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QUICK PIN REFERENCE

Symbol	Type	Name and Function
System Interface Pin Descriptions		
A0:A23	I	**ADDRESS BUS** lines driven by the host system which enable direct addressing of up to 16 Mbytes of memory on a card. Signal A0 is not used in word access mode. Signal A23 is the most significant bit. In a 16-bit ISA system, LA<23:17> should be connected to A<23:17> and SA<16:00> should be connected to A<16:00>.
AEN	I	**SYSTEM ADDRESS ENABLE**
BALE	I	**BUS ADDRESS LATCH ENABLE:** This active HIGH input is used to latch A23-A17 at the beginning of any bus cycle.
$\overline{CS}$	I	**CHIP SELECT:** This signal is driven from an address decode if Mode = 1, or is tied low. For internal chip select, Mode = 0.
SD0:SD7	I/O	**DATA INPUT/OUTPUT** lines constitute a bidirectional bus. D0 through D7 are used to access the PCIC internal registers.
V_{SS}		**GROUND:** Provides the 0V connection from which all inputs and outputs are referenced.
$\overline{INTR}$	O	**INTERRUPT REQUEST:** This active LOW output requests a standard maskable interrupt to the CPU. $\overline{INTR}$ is intended to be connected to the $\overline{EXTSMI}$ of the Intel386 SL CPU.
IOCHRDY	O	**I/O CHANNEL READY:** This active HIGH signal is issued as an indication that the current I/O bus cycle is completed. When a PC Card peripheral needs to extend a READ or WRITE cycle, the PCIC pulls IOCHRDY LOW. IOCHRDY can be deasserted by either the PCMCIA signal $\overline{WAIT}$, or by programming the PCIC to add wait states for 16-bit memory and I/O cycles. If $\overline{Wait}$ is used in 16-bit mode, the wait state generator has to be set to 1 wait state.
$\overline{IOCS16}$	O	**16-BIT I/O TRANSFER MODE CHIP SELECT:** This signal is used by the host system to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System Controller requests a 16-bit I/O cycle and $\overline{IOCS16}$ is sampled high.
$\overline{IORC}$	I	**I/O PORT READ:** Driven to an active state (low) indicates to the PCIC that an I/O read cycle is occurring on the system bus.
$\overline{IOWC}$	I	**I/O PORT WRITE:** Driven to an active state (low) indicates to the PCIC that an I/O write cycle is occurring on the system bus.
IRQs	O	**SYSTEM INTERRUPT BACKPLANE REQUESTS:** These active high signals are used to request interrupt service.
$\overline{MEMCS16}$	O	**16-BIT MEMORY TRANSFER MODE CHIP SELECT:** This signal is used by the host system to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System Controller requests a 16-bit memory cycle and $\overline{MEMCS16}$ is sampled high.
$\overline{MEMR}$	I	**SYSTEM MEMORY READ:** Active LOW signal indicates a read cycle.
$\overline{MEMW}$	I	**SYSTEM MEMORY WRITE:** Active LOW signal indicates a write cycle.
MODE	I	**DECODE MODE:** Used to determine if the Port Address Chip Select will be decoded internally (Mode = 0), or with external logic (Mode = 1).
PWRGOOD	I	**POWER GOOD:** Active high signal indicates that power to the system is stable. Implementations not using the POWER GOOD signal should tie this signal low.

QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
System Interface Pin Descriptions (Continued)		
RESETDRV	I	**RESET DRIVE:** Active HIGH signal indicates a main system cold reset, generated by the Intel386 SL CPU as a combination of POWERGOOD and the Intel 386 SL CPU resume.
RSV		**RESERVED:** Must be pulled high by an external resistor. A recommended value is 10K.
$\overline{RI\_OUT}$	O	**RING INDICATE OUTPUT:** Pass through of Ring Indicate output from I/O PC Card.
$\overline{SBHE}$	I	**SYSTEM BUS HIGH ENABLE:** When this signal is LOW, it indicates that data is valid on the upper byte of the 16-bit data bus.
SEL0, SEL1	I	**SELECT PCIC BASE I/O ADDRESS:** Strapping options that determine the PCIC registers base I/O address. All PCIC registers are accessed indirectly using an offset from the base I/O address. These signals allow chaining several PCICs together.
$\overline{SPKROUT}$	O	**SPEAKER OUT:** Digital audio signal used to provide a single amplitude (digital) audio waveform intended to be driven to the system's speaker. Pass through of $\overline{SPKR}$ from I/O PC Card. When no audio signal is present, this signal shall be held high.
SYSCLK	I	**SYSTEM CLOCK:** 4.77 MHz–8.33 MHz. The value of the clock will effect the following: $\overline{INTR}$ Timing characteristic $\overline{INTR}$ pulse width is 3 SYSCLKs in length 16 bit $\overline{MEMR}$ Delay 16 bit $\overline{MEMW}$ Delay
V_{CC}		**DEVICE POWER SUPPLY:** 5V ±10%.
$\overline{ZEROWS}$	O	**ZERO WAIT STATE:** This active LOW output indicates that a PC Card wishes to execute an 8-bit zero wait state bus cycle. This signal will not be driven during a 16-bit access.

QUICK PIN REFERENCE (Continued)

NOTE:
The I/O PC Card Functions are listed below the Memory PC Card functions and in ().

Symbol	Type	Name and Function
PCMCIA/JEIDA PC Card Socket Interface Pin Descriptions		
BVD1, BVD2	I	**BATTERY VOLTAGE DETECT:** Generated by memory PC Cards that include batteries. The signals are an indication of the condition of the battery on the memory PC Card. Both BVD1 and BVD2 are kept asserted (high) when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. If BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. Signal status available by reading the Interface Status Register.
($\overline{STSCHG}$/$\overline{RI}$)	I	**CHANGED STATUS:** Signal is held high when either or both the "Signal on Change" bit and "Changed" bit in the Card Status Register on the PC Card are set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical or of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. **Ring Indicate.** Signal is qualified by the Ring Indicate Enable bit (Interrupt and General Control Register bit 7). If enabled the input signal is passed on to the RI_$\overline{OUT}$ output pin.
($\overline{SPKR}$)	I	**DIGITAL AUDIO:** Is used to provide a single amplitude (digital) audio waveform intended to be driven to the system's speaker.
CADR<25:12>	O	**CARD ADDRESS:** Used with the lower 11 bits of Address Bus to generate Card Address.
$\overline{CD1}$, $\overline{CD2}$	I	**CARD DETECT:** Provides for proper card insertion detection. The signals have been positioned at opposite ends of the connector to facilitate the detection process. The signals are connected to ground internally on the PC Card; thus they will be forced low whenever a card is placed in a host socket. Signal status is available by reading Interface Status Register.
$\overline{CE1}$, $\overline{CE2}$	O	**CARD ENABLE:** Active low card enable signals driven by the PCIC. $\overline{CE1}$ is used to enable even bytes, $\overline{CE2}$ for odd bytes. A multiplexing scheme based on A0, $\overline{CE1}$, $\overline{CE2}$ allows 8-bit hosts to access all data on D0-D7 if desired.
$\overline{ENABLE}$	O	**ENABLE:** Signal used to select PC Card socket to activate. This signal controls the external address buffer logic.
EXT_DIR	O	**EXTERNAL TRANSCEIVER DIRECTION CONTROL:** This signal is high during a read, and is low during a write. The default power up condition is write (low.)
$\overline{IORD}$	O	**I/O READ:** Active low signal driven by the host system. It is used with the $\overline{REG}$ line to gate I/O Read data from the PC Card. $\overline{IORD}$ gates I/O Read data from a memory PC Card only when the $\overline{REG}$ line is also asserted.
$\overline{IOWR}$	O	**I/O WRITE:** Signal is driven by the host system and used together with the $\overline{REG}$ line for gating I/O Write data to the memory PC Card. $\overline{IOWR}$ gates the I/O Write data to the PC Card only when the $\overline{REG}$ line is also asserted.
$\overline{OE}$	O	**OUTPUT ENABLE:** The $\overline{OE}$ line is an active low signal driven by the host system which is used to gate Memory Read data from memory PC Cards.
V_{CC}_$\overline{EN}$ $V_{PP}1$_EN0 $V_{PP}1$_EN1 $V_{PP}2$_EN0 $V_{PP}2$_EN1	O	**POWER CONTROL:** Five signals used to control voltages ($V_{PP}1$, $V_{PP}2$ and V_{CC}) for PCMICA/JEIDA socket interface. Logic is detailed in Power and RESETDRV Control Register.

QUICK PIN REFERENCE (Continued)

NOTE:
The I/O PC Card Functions are listed below the Memory PC Card functions and in (). (Continued)

Symbol	Type	Name and Function
PCMCIA/JEIDA PC Card Socket Interface Pin Descriptions (Continued)		
$\overline{V_{PP}\_VALID}$	I	**V_{PP} VALID:** This active Low input indicates that the V_{PP} power lines have reached the user specified range. Signal status is available by reading Interface Status Register.
RDY/$\overline{BSY}$	I	**READY/BUSY:** Driven low by memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY/BUSY is set high when memory PC Cards are ready to accept a new data transfer command. READY/BUSY is used as an interrupt request for I/O PC Cards. Signal status is available by reading Interface Status Register.
($\overline{IREQ}$)	I	**INTERRUPT REQUEST:** Signal is asserted by an I/O PC Card to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested.
$\overline{REG}$	O	**ATTRIBUTE MEMORY SELECT:** Inactive (high) for all normal accesses to what is known as Main Memory of the PC Card. I/O PC Cards will not respond to $\overline{IORD}$ or $\overline{IOWR}$ when the $\overline{REG}$ signal is kept inactive. During DMA operations the $\overline{REG}$ signal must be kept inactive to ensure that PC cards do not respond to the I/O portion of a DMA transfer and to ensure that DMA accesses to the memory portion of a PC Card takes place to the Common Memory of the PC Card. This may be accomplished on an ISA compatible signal by forcing $\overline{REG}$ inactive whenever the ISA bus signal AEN (Address Enable) is inactive. When this signal is active (low), access is limited to Attribute Memory when $\overline{WE}$ or $\overline{OE}$ are active, and to I/O ports when $\overline{IORD}$ or $\overline{IOWR}$ are active. For configurable memory PC Cards and I/O PC Cards, the PC Cards contain configuration and status registers in the Attribute Memory Space.
RESET	O	**CARD RESET:** Forces a hard reset to a PC card.
$\overline{WAIT}$	I	**BUS CYCLE WAIT:** Signal driven by the PC card to delay completion of the memory or I/O cycle which is in progress.
$\overline{WE}$/$\overline{PRGM}$	O	**WRITE ENABLE:** $\overline{WE}$ is used by the host for gating Memory Write data. $\overline{WE}$ is also used for memory PC Cards that employ programmable memory technologies.
WP	I	**WRITE PROTECT:** Reflects the status of the Write Protect switch on memory PC Cards. If the memory PC Card switch is present, this signal will be asserted by the memory PC Card when the switch is enabled, and deasserted when the switch is disabled. If the memory PC Card has no Write Protect switch, the card will connect this line to ground or V_{CC}, depending on the condition of the card memory. If the memory PC Card can always be written, the pin will be connected to ground. If the memory PC Card is permanently Write Protected, the pin will be connected to V_{CC}. For I/O PC Cards, WP is used for the Card is 16-Bit Port ($\overline{IOIS16}$) function. Signal status is available by reading the Interface Status Register.
($\overline{IOIS16}$)	I	**CARD IS 16-BIT PORT:** Signal is asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16-bit accesses. If this signal is not asserted during a 16-bit I/O access, the system will generate a second, 8-bit reference to the odd byte of the 16-bit word which is accessed by the initial cycle. If 8-bit window size is selected, $\overline{IOIS16}$ is ignored.

NOTE:
PCMCIA Input Acknowledge ($\overline{INPACK}$) signal is not supported by the PCIC.

OVERVIEW

Intel's PC Card Interface Controller (PCIC) — is the ExCA™ interface solution for notebook PCs. Currently, the PCIC allows OEMs to design their systems to provide the PC user with a wide range of connectivity options (Modem, Twisted Pair Ethernet, etc.) as well as eliminating rotating electro-mechanical media (via Intel Flash Memory Cards). Through the use of the ExCA standard interface, the PCIC will provide access to an even broader range of functions in the future.

The PCIC is the heart of the Intel ExCA implementation of the PCMCIA/JEIDA standard. ExCA and the PCIC provide an open standard system interface for PC Cards at the hardware and data interchange level. The PCIC insures that PC Card compatibility is maintained across manufacturers of PC Cards, as well as between systems from multiple notebook PC vendors.

The PCIC simplifies designing the PC Card socket to the ISA bus interface in a notebook PC. To fulfill this requirement, there were two main criteria which had to be met:

1. Minimize chip count between an ISA bus and PC Card socket(s).
2. Maximize flexibility by providing benefits such as programmable PC Card select decoding, multiple memory address translation maps, power management and I/O Interrupt steering.

In addition, the PCIC supports a jumperless configuration mechanism which allows the system manufacturer to support PC Card setup either through a configuration (CONFIG.SYS) driver or through an extension to the BIOS called "System Socket Services".

ARCHITECTURAL OVERVIEW

The PCIC functional blocks include the ISA interface, PCMCIA/JEIDA PC Card socket interface, Memory and I/O Window mapping, Power Management Support, Interrupt Steering, Configuration Registers and Digital Audio Signal.

ISA Interface

The PCIC interfaces directly to the ISA bus, such as that found on the Intel386 SL Microprocessor SuperSet and most other integrated ISA chipsets. For systems based on the Intel386 SL Microprocessor SuperSet, the PCIC provides additional signals such as **PowerGood, SPKROUT, INTR** and **RI_OUT.**

PCMCIA/JEIDA PC Card Socket Interface

The PCMCIA/JEIDA interface consists of 60 signals and 8 power connections that interface to PC Cards through a 68 pin socket. A single PCIC can be configured to support either one or two PC Cards sockets directly, with the provision to allow up to eight PC Card sockets in multiples of two. The PCIC supports two PC Card types (either memory or I/O) interchangeably. It accomplishes this by multiplexing some of the static signals that are defined differently for memory and I/O PC Cards. These signals are configured appropriately by accessing the PC Card's card configuration registers.

Memory and I/O Window Mapping

As with standard PC add-in cards, multiple PC Cards in a system can conflict if they try to utilize the same system memory and I/O range. The PCIC allows the Operating System to map each PC Card into a separate memory range, and a separate I/O range, thus avoiding system configuration conflicts.

The PCIC provides memory paging, memory address mapping for both PC Card attribute and common memory, and I/O address mapping. The PCIC includes registers to allow access to the card information structure and card configuration registers within the attribute memory described by the PCMCIA/JEIDA PC Card Standard.

Power Management

The PCIC implements power management for each PC Card socket. Socket power management is controlled through programming the **Power** and **RESETDRV** control register (Base + 02/42h). Additionally, each socket can be independently buffered to allow for insertion and removal of PC Cards. The system designer can add external buffer(s) and transceiver(s) to the system to provide electrical isolation between the PCMCIA sockets and the system bus.

Buffering system examples are included in this data sheet.

Interrupt Steering

The PCIC steers the one interrupt from the PC Card to one of ten system bus interrupts. Multiple PC Cards in a system can conflict if they try to utilize the same interrupt level (i.e., $\overline{IRQ7}$). The PCIC can be programmed to eliminate this conflict by steering each PC Card interrupt request to a different system interrupt.

Configuration Registers

The PCIC provides a register containing interface identity and revision information for each socket.

Digital Audio Signals

The PCIC supports special signals such as digital audio ($\overline{SPKR}$). These signals are passed through to the system bus without signal conditioning.

PC Card Interface I/O Register Addressing

All PCIC control registers are byte wide and accessed using an indirect indexing scheme. Two I/O addresses, are used to access the PCIC's control registers. The first I/O address is the PCIC's index register. The second I/O address is the PCIC's data register. Each PC Card socket can have up to 64 indirectly addressed registers. This allows for the support of two separate PC card sockets using only two I/O addresses. In order to support up to eight sockets in a system, another 2 I/O addresses are used which are selected by input lines (**SEL0** and **SEL1**). Any system conflicts with the default I/O addresses can be overcome (setting the mode line) by using external address decode logic to map to another I/O address.

The PCIC index register and data register I/O address for the interface registers support both Intel386 SL CPU and ISA system configurations. The index register and the data register are read/write registers. *The PCIC will not respond to a data register read or write operation or to an index register read operation unless the index register has first been written to with a valid index.*

The **SEL1** and **SEL0** lines are strapping options for the PCIC, which determine the starting base for the index register values. **SEL1** and **SEL0** determine the mapping of socket A and socket B to one of four groups.

Index Base Values for Group 0 thru Group 3

Mode	$\overline{CS}$	SEL1	SEL0	Base	Index I/O Add	Data I/O Add
0	0	0	0	00h	3E0h	3E1h
0	0	0	1	80h	3E0h	3E1h
0	0	1	0	00h	3E2h	3E3h
0	0	1	1	80h	3E2h	3E3h
1	0	X	X	00h	A0 = 0	A0 = 1
1	0	X	X	80h	A0 = 0	A0 = 1
X	1	X	X	XXh	PCIC Not Selected	

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REGISTER SET

The following is a list of PCIC registers and their offset values. Each register is byte wide and can be read only or read/write.

PCIC Registers Table

Socket A Offset	Socket B Offset	Register Name
+ 00h	+ 40h	Identification and Revision
+ 01h	+ 41h	Interface Status
+ 02h	+ 42h	Power and RESETDRV Control
+ 03h	+ 43h	Interrupt and General Control
+ 04h	+ 44h	Card Status Change
+ 05h	+ 45h	Card Status Change Interrupt Configuration
+ 06h	+ 46h	Address Window Enable
+ 07h	+ 47h	I/O Control
+ 08h	+ 48h	I/O Address 0 Start Low Byte
+ 09h	+ 49h	I/O Address 0 Start High Byte
+ 0Ah	+ 4Ah	I/O Address 0 Stop Low Byte
+ 0Bh	+ 4Bh	I/O Address 0 Stop High Byte
+ 0Ch	+ 4Ch	I/O Address 1 Start Low Byte
+ 0Dh	+ 4Dh	I/O Address 1 Start High Byte
+ 0Eh	+ 4Eh	I/O Address 1 Stop Low Byte

REGISTER SET (Continued)

PCIC Registers Table (Continued)

Socket A Offset	Socket B Offset	Register Name
+ 0Fh	+ 4Fh	I/O Address 1 Stop High Byte
+ 10h	+ 50h	System Memory Address 0 Mapping Start Low Byte
+ 11h	+ 51h	System Memory Address 0 Mapping Start High Byte
+ 12h	+ 52h	System Memory Address 0 Mapping Stop Low Byte
+ 13h	+ 53h	System Memory Address 0 Mapping Stop High Byte
+ 14h	+ 54h	Card Memory Offset Address 0 Low Byte
+ 15h	+ 55h	Card Memory Offset Address 0 High Byte
+ 16h	+ 56h	Reserved
+ 17h	+ 57h	Reserved
+ 18h	+ 58h	System Memory Address 1 Mapping Start Low Byte
+ 19h	+ 59h	System Memory Address 1 Mapping Start High Byte
+ 1Ah	+ 5Ah	System Memory Address 1 Mapping Stop Low Byte
+ 1Bh	+ 5Bh	System Memory Address 1 Mapping Stop High Byte
+ 1Ch	+ 5Ch	Card Memory Offset Address 1 Low Byte
+ 1Dh	+ 5Dh	Card Memory Offset Address 1 High Byte
+ 1Eh	+ 5Eh	Reserved
+ 1Fh	+ 5Fh	Reserved
+ 20h	+ 60h	System Memory Address 2 Mapping Start Low Byte
+ 21h	+ 61h	System Memory Address 2 Mapping Start High Byte
+ 22h	+ 62h	System Memory Address 2 Mapping Stop Low Byte
+ 23h	+ 63h	System Memory Address 2 Mapping Stop High Byte
+ 24h	+ 64h	Card Memory Offset Address 2 Low Byte
+ 25h	+ 65h	Card Memory Offset Address 2 High Byte
+ 26h	+ 66h	Reserved
+ 27h	+ 67h	Reserved
+ 28h	+ 68h	System Memory Address 3 Mapping Start Low Byte
+ 29h	+ 69h	System Memory Address 3 Mapping Start High Byte
+ 2Ah	+ 6Ah	System Memory Address 3 Mapping Stop Low Byte
+ 2Bh	+ 6Bh	System Memory Address 3 Mapping Stop High Byte
+ 2Ch	+ 6Ch	Card Memory Offset Address 3 Low Byte
+ 2Dh	+ 6Dh	Card Memory Offset Address 3 High Byte
+ 2Eh	+ 6Eh	Reserved
+ 2Fh	+ 6Fh	Reserved
+ 30h	+ 70h	System Memory Address 4 Mapping Start Low Byte
+ 31h	+ 71h	System Memory Address 4 Mapping Start High Byte
+ 32h	+ 72h	System Memory Address 4 Mapping Stop Low Byte
+ 33h	+ 73h	System Memory Address 4 Mapping Stop High Byte
+ 34h	+ 74h	Card Memory Offset Address 4 Low Byte
+ 35h	+ 75h	Card Memory Offset Address 4 High Byte
+ 36h	+ 76h	Reserved
+ 37h	+ 77h	Reserved
+ 38h	+ 78h	Reserved
+ 39h	+ 79h	Reserved
+ 3Ah	+ 7Ah	Reserved
+ 3Bh	+ 7Bh	Reserved
+ 3Ch	+ 7Ch	Reserved
+ 3Dh	+ 7Dh	Reserved
+ 3Eh	+ 7Eh	Reserved
+ 3Fh	+ 7Fh	Reserved

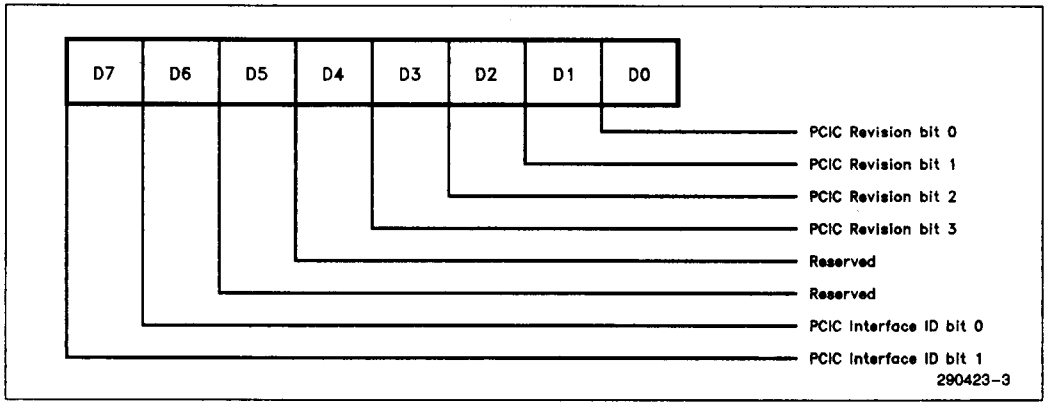
General Setup Registers

Identification and Revision Register (Read Only)

Socket A: Index Value (Base + 00h)

Socket B: Index Value (Base + 40h)

The Identification and Revision Register is used by the system software to determine the type of PC Cards supported, and to identify what version of a PCIC is present. System software reads the Identification and Revision Register and then compares the result value against existing revision numbers (82h for Rev. 0 PCIC silicon ID code).



Bit 7 and Bit 6: PCIC Interface Type

These bits indicate the type of PC Cards supported by the PCIC at the particular socket. These bits do not identify the type of card that is present at the socket.

ID 1	ID 0	Interface
0	0	I/O Only
0	1	Memory Only
1	0	Memory & I/O
1	1	Reserved

NOTE:
These bits will read back as 10.

Bit 5 and Bit 4: Reserved

These bits will be read back as zero.

Bit 3 thru Bit 0: PCIC Revision

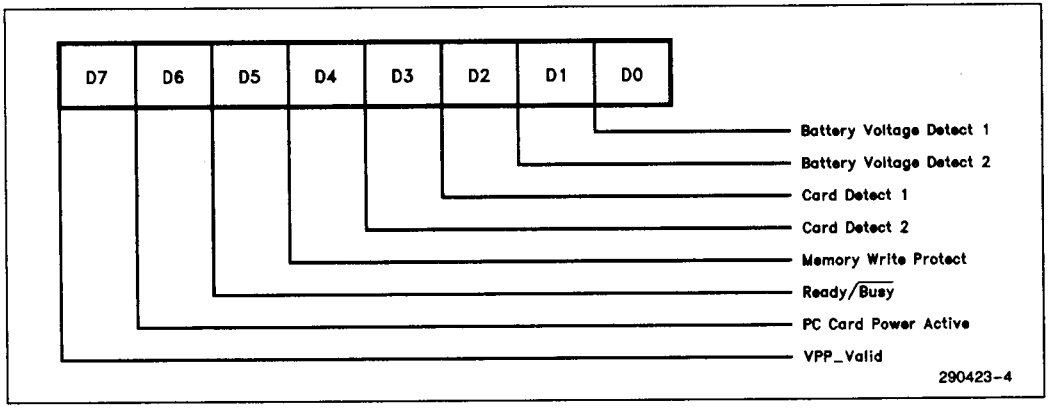
These four bits indicate the current revision level of the PCIC.

The initial revision code will be 0010.

Interface Status Register (Read Only)

Socket A: Index Value (Base + 01h)
Socket B: Index Value (Base + 41h)

The Interface Status Register provides the current status of the PC Card socket interface signals.



Bit 7: V_{PP}_Valid.

Indicates the state of the $\overline{V_{PP}\_Valid}$ pin. If this bit is set to a one, the $\overline{V_{PP}\_Valid}$ pin is active ($\overline{V_{PP}\_Valid}$ = 0). If this bit is set to zero, the $\overline{V_{PP}\_Valid}$ pin is inactive ($\overline{V_{PP}\_Valid}$ = 1).

NOTE:
The logic level of this bit is the reverse of the $\overline{V_{PP}\_VALID}$ pin.

Bit 6: PC Card Power Active

Indicates the current power status of the socket. If bit is set to zero, power to the socket is turned off (V_{CC}, $V_{PP}1$, and $V_{PP}2$ are all no connects). If bit is set to one, power is provided to the socket (V_{CC} = 5V and $V_{PP}1$ and $V_{PP}2$ are set according to bits 3–0 in the power control register).

Bit 5: Ready/$\overline{Busy}$

Indicates the ready condition of the PC Card. If bit is set to one, the PC Card is ready. If bit is zero the PC Card is busy.

Bit 4: Memory Write Protect

Bit value is the logic level of the **WP** signal on the memory PC Card interface. When bit is set to zero the PC Card is not write protected. When bit is set to one the PC Card is write protected, and the card enable signals to the PC Card are not enabled during a memory write cycle to common or attribute memory.

Bit 3: Card Detect 2

Together with card detect 1 indicates a card is present at the socket and fully seated. Bit is set to one if the **$\overline{CD2}$** signal on the PC Card interface is active. Bit is set to zero if the **$\overline{CD2}$** signal on the PC Card interface is inactive.

Bit 2: Card Detect 1

Together with card detect 2 indicates a card is present at the socket and fully seated. Bit is set to one if the **$\overline{CD1}$** signal on the PC Card interface is active. Bit is set to zero if the **$\overline{CD1}$** signal on the PC Card interface is inactive.

Bit 1 and Bit 0: Battery Voltage Detect 2 and 1

BVD1	BVD2	Status
0	0	Battery Dead
0	1	Battery Dead
1	0	Warning
1	1	Battery Good

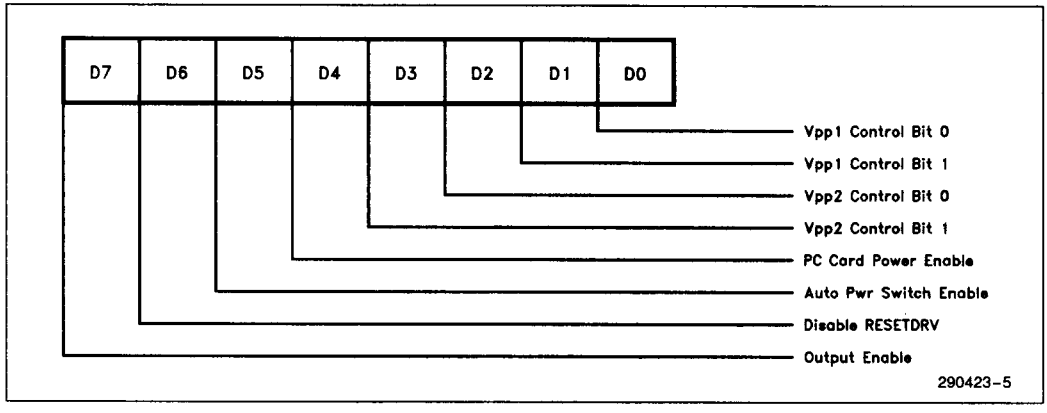
For I/O PC Cards, bit 0 indicates the current status of the ($\overline{\text{STSCHG}}$/$\overline{\text{RI}}$) signal from the PC Card when the ring indicate enable bit in the Interrupt and General control register is set to zero.

Power and RESETDRV Control Register (Read/Write)

Socket A: Index Value (Base + 02h)

Socket B: Index Value (Base + 42h)

This register controls the PC Card power and resetting of the PCIC registers. A **RESETDRV** clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one. *Output Enable should not be set until the register has been previously written setting PC Card Power Enable.*



Bit 7: Output Enable

If this bit is set to zero, the PC Card outputs listed below are tri-stated and the $\overline{\text{ENABLE}}$ pin to the corresponding socket is inactive.

CADR<25:12>, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{OE}}$, $\overline{\text{REG}}$, RESET, $\overline{\text{WE}}$

Refer to the Slot Power Control Table for the functionality of the Output Enable bit.

Bit 6: Disable Resume RESETDRV

If bit is set to one and the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1), the resetable registers of the PCIC will remain intact and will not be reset. If bit is set to zero and the **RESETDRV** is a result of a Intel386 SL CPU resume, the resetable registers of the PCIC will be reset. If the **RESETDRV** is a result of a system reset, the resetable registers of the PCIC will be reset regardless of the setting of bit.

Bit 5: Auto Power Switch Enable

If bit is set to zero, automatic socket power switching based on card detects is disabled. If bit is set to one, automatic socket power switching based on card detects is enabled.

Bit 4: PC Card Power Enable

If bit is set to zero, all power to the PC Card is disabled (V_{CC}, $V_{PP}1$ and $V_{PP}2$ = no connect). When bit is set to one, V_{CC} = 5V and $V_{PP}1$ and $V_{PP}2$ are set according to bit 3 through bit 0 in this register.

Bit 3 and Bit 2: PC Card $V_{PP}2$ Power Control

00 - no connect 01 - V_{CC} 10 - V_{PP} 11 - reserved

NOTE:
The 11 combination is reserved and should not be used, but if these bits are set to 11 then $V_{PP}2$ will be a no connect.

Bit 1 and Bit 0: PC Card $V_{PP}1$ Power Control

00 - no connect 01 - V_{CC} 10 - V_{PP} 11 - reserved

NOTE:
The 11 combination is reserved and should not be used, but if these bits are set to 11 then $V_{PP}1$ will be a no connect.

Power Control

The PCIC provides each socket with 5 power control pins.

Ctrl Bit	Name	Description
0	$V_{PP}1\_EN0$	$V_{PP}1$ control pin, bit 0
1	$V_{PP}1\_EN1$	$V_{PP}1$ control pin, bit 1
2	$V_{PP}2\_EN0$	$V_{PP}2$ control pin, bit 0
3	$V_{PP}2\_EN1$	$V_{PP}2$ control pin, bit 1
4	$\overline{V_{CC}\_EN}$	Master enable pin

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	$\overline{V_{CC}\_EN}$	$V_{PP}x\_EN1$	$V_{PP}x\_EN0$
1	0	0	0	0	0	0	0
1	0	1	0	1	0	0	1
1	1	0	1	0	0	1	0
1	1	1	1	1	0	0	0
0	X	X	X	X	1	0	0
0	X	X	X	X	1	0	0
0	X	X	X	X	1	0	0
0	X	X	X	X	1	0	0

These pins allow the designer to control two unique voltage levels to each socket V_{PP} pin.

A PC card is considered detected when: $\overline{CD2}$ = 0 and $\overline{CD1}$ = 0.

The PC Card Active Power bit of the Interface Status Register indicates the current power status of the socket. If bit is set to zero, power to the socket is turned off ($\overline{V_{CC}EN}$, $V_{PP}1\_EN0$, $V_{PP}1\_EN1$, $V_{PP}2\_EN0$, and $V_{PP}2\_EN1$ are all inactive). If this bit is set to one, power is provided to the socket ($\overline{V_{CC}EN}$ = 0V and $V_{PP}1$ and $V_{PP}2$ are set according to bits 3-0 in the power control register).

The following table describes the slot power control function.

Power Cntrl Reg			PC Card Pins		Tri-state Outputs	IF Stat Reg
Output	PC Card Power Enable	Auto Power Switch Enable	$\overline{CD1}$	$\overline{CD2}$		PC Card Power Active
X	0	X	X	X	OFF	0
0	1	0	0	0	OFF	1
1	1	0	0	0	ON	1
X	1	0	X	1	OFF	1
X	1	0	1	X	OFF	1
0	1	1	0	0	OFF	1
1	1	1	0	0	ON	1
X	1	1	X	1	OFF	0
X	1	1	1	X	OFF	0

NOTE:
PC Card Power Active = 0 → V_{CC}, $V_{PP}1$, and $V_{PP}2$ are no connects

The power control register also contains control bits in which to independently and separately select 5V, 12V, or no connect for $V_{PP}1$ and $V_{PP}2$.

The power control circuitry only switches the applicable voltages and does not provide voltage generation.

It is recommmended that on all designs using the PCIC, a 1 Amp 125V fuse be installed on each PCMCIA socket voltage line to comply IEC 950 and UL 1950.

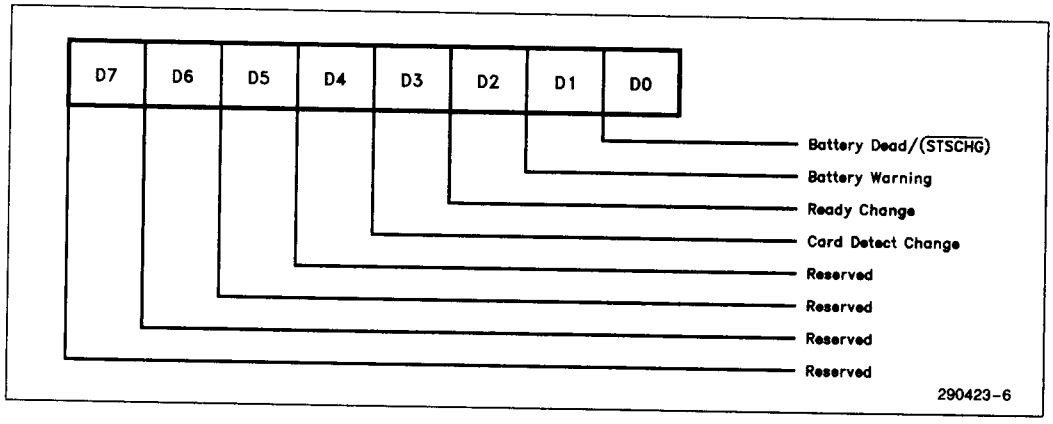
Card Status Change Register (Read Only)

Socket A: Index Value (Base + 04h)
Socket B: Index Value (Base + 44h)

The Card Status Change Register contains the status for sources of the card status change interrupt. These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the card status change interrupt configuration register. Reading the Card Status Change Register causes the register bits to be reset to zero.

If the card status change interrupt is enabled to one of the system bus interrupt request lines, the corresponding IRQ signal remains active high until this register is read.

A **RESETDRV** clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



NOTE:
Bit descriptions in parenthesis indicate valid signals after the interface is configured for I/O PC Cards.

Bit 7 thru Bit 4: Reserved

These reserved bits always read zero.

Bit 3: Card Detect Change

Bit is set to one when a change has been detected on either the **CD1** or **CD2** signals.

Bit 2: Ready Change

Bit is set to one when a low to high has been detected on the **Ready/Busy** signal indicating that the memory PC Card is ready to accept a new data transfer. Bit reads zero for I/O PC Cards.

Bit 1: Battery Warning

Bit is set to one when a battery warning condition has been detected. Bit reads zero for I/O PC Cards.

Bit 0: Battery Dead (STSCHG)

For memory PC Cards, bit is set to one when a battery dead condition has been detected.

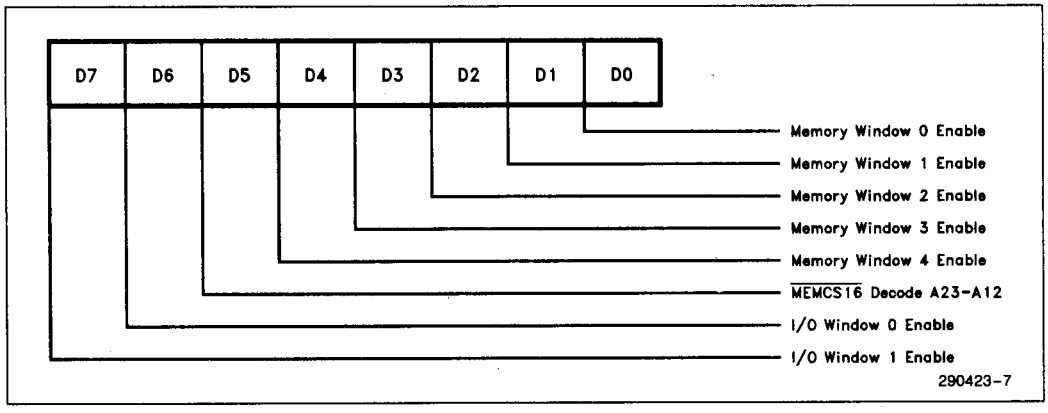
For I/O PC Cards, bit is set to one if ring indicate enable bit in the interrupt and general control register is set to zero and the (**STSCHG/RI**) signal from the I/O PC Card has been pulled low. The system software then has to read the status change register in the PC Card to determine the cause of the status change signal (**STSCHG**). This bit reads zero for I/O PC Cards if the ring indicate enable bit in the interrupt and general control register is set to one.

Address Window Enable Register (Read/Write)

Socket A: Index Value (Base + 06h)

Socket B: Index Value (Base + 46h)

This register controls the enabling of the memory and I/O mapping windows to the PC Card memory or I/O space. **RESETDRV** clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7: I/O Window 1 Enable

If bit is set to zero, an I/O access within the I/O address 1 window will inhibit the card enable signals to the PC Card. If bit is set to one, an I/O access within the I/O address 1 window will generate the card enables to the PC Card. I/O accesses pass addresses from the system bus directly through to the PC Card. *The start and stop register pairs must all be set to the desired window values before setting bit to one.*

Bit 6: I/O Window 0 Enable

If bit is set to zero, an I/O access within the I/O address 0 window will inhibit the card enable signals to the PC Card. If bit is set to one, an I/O access within the I/O address 0 window will generate the card enables to the PC Card. I/O accesses pass addresses from the system bus directly through to the PC Card. *The start and stop register pairs must all be set to the desired window values before setting bit to one.*

Bit 5: $\overline{\text{MEMCS16}}$ Decode A23-A12

If this bit is set to zero, **$\overline{\text{MEMCS16}}$** is generated from a decode of the system (ISA) address lines **A23–A17** only. This means that at a minimum, a 128K block of system (ISA) memory address space is set aside as 16-bit memory only. If this bit is set to a one, **$\overline{\text{MEMCS16}}$** is generated from decode of the system (ISA address lines **A23–A12**).

When decoding in the first 128K block of address space, full line address decode should be used.

Bit 4: Memory Window 4 Enable

If bit is set to zero, a memory access within the system memory address 4 window will inhibit the card enable signals to the PC Card. If bit is set to one, a memory access within the system memory address 4 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to one.* When bit is set to one and the system address is within the window, the computed address will be generated to the PC Card.

Bit 3: Memory Window 3 Enable

If bit is set to zero, a memory access within the system memory address 3 window will inhibit the card enable signals to the PC Card. If bit is set to one, a memory access within the system memory address 3 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to one.* When bit is set to one and the system address is within the window, the computed address will be generated to the PC Card.

Bit 2: Memory Window 2 Enable

If bit is set to zero, a memory access within the system memory address 2 window will inhibit the card enable signals to the PC Card. If bit is set to one, a memory access within the system memory address 2 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to one.* When bit is set to one and the system address is within the window, the computed address will be generated to the PC Card.

Bit 1: Memory Window 1 Enable

If bit is set to zero, a memory access within the system memory address 1 window will inhibit the card enable signals to the PC Card. If bit is set to one, a memory access within the system memory address 1 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to one.* When bit is set to one and the system address is within the window, the computed address will be generated to the PC Card.

Bit 0: Memory Window 0 Enable

If bit is set to zero, a memory access within the system memory address 0 window will inhibit the card enable signals to the PC Card. If bit is set to one, a memory access within the system memory address 0 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to one.* When bit is set to one and the system address is within the window, the computed address will be generated to the PC Card.

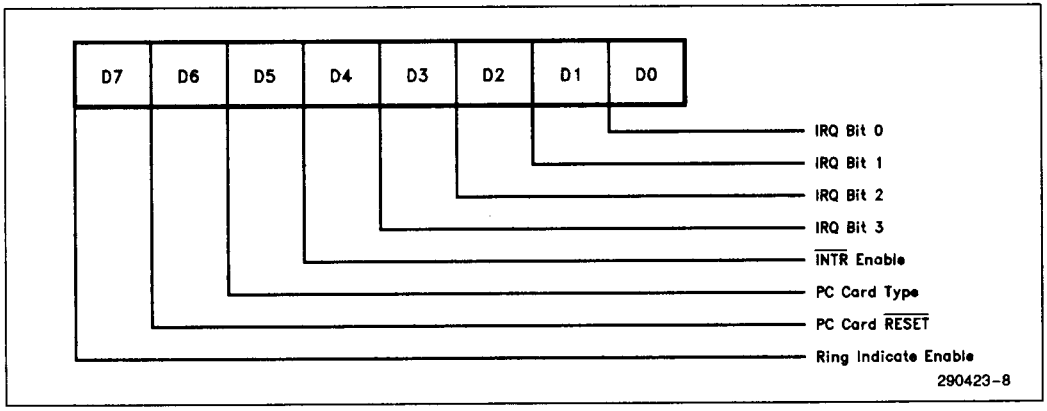
Interrupt Registers

Interrupt and General Control Register (Read/Write)

Socket A: Index Value (Base + 03h)

Socket B: Index Value (Base + 43h)

The Interrupt and General Control Register controls the interrupt steering for the PC Card I/O interrupt as well as general control of the PCIC. A **RESETDRV** clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7: Ring Indicate Enable

If bit is set to one and the PC Card type bit is set to one (I/O PC Card), the (**STSCHG/RI**) signal from the I/O PC Card is used as a ring indicator signal and is passed through to the **RI_OUT** output pin of the PCIC. If bit is set to zero and the PC Card type bit is set to one (I/O PC Card), the (**STSCHG/RI**) signal from the I/O PC Card is used as the status change signal (STSCHG). The current status of the signal is then available to be read from the interface status register and this signal can be configured as a source for the card status change interrupt. The ring indicate enable bit has no function when the PC Card type bit is set to zero (memory PC Card).

Bit 6: PC Card Reset

This is a software reset to the PC Card. Setting bit to zero activates the **RESET** signal to the PC Card. The **RESET** signal will be active until bit is set to one.

Bit 5: PC Card Type (**Memory** or **I/O**)

Setting bit to one selects an I/O PC Card which enables the PC Card interface multiplexer for routing of PC Card I/O signals. Setting bit to zero selects a Memory PC Card.

Bit 4: INTR Enable

Setting bit to one enables the card status change interrupt on the **INTR** signal. If bit is set to zero, the **INTR** signal does not indicate a card status change interrupt and the card status change interrupt is steered to one of the IRQ lines according to bits 7 through 4 in the card status change interrupt configuration register.

Bit 3 thru Bit 0: IRQ Level Selection (**I/O Cards Only**)

These bits select the redirection of the PC Card interrupt.

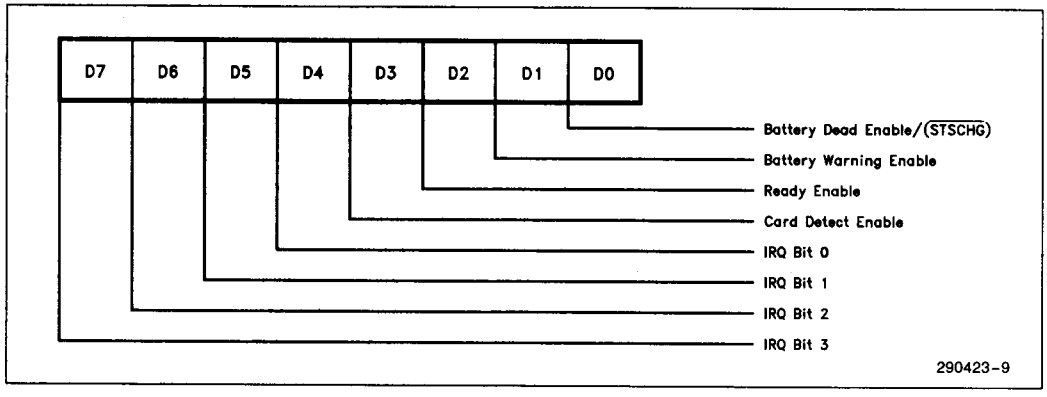
IRQ Bit 3	IRQ Bit 2	IRQ Bit 1	IRQ Bit 0	Interrupt Request Level
0	0	0	0	IRQ Not Selected
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	IRQ3 Enabled
0	1	0	0	IRQ4 Enabled
0	1	0	1	IRQ5 Enabled
0	1	1	0	Reserved
0	1	1	1	IRQ7 Enabled
1	0	0	0	Reserved
1	0	0	1	IRQ9 Enabled
1	0	1	0	IRQ10 Enabled
1	0	1	1	IRQ11 Enabled
1	1	0	0	IRQ12 Enabled
1	1	0	1	Reserved
1	1	1	0	IRQ14 Enabled
1	1	1	1	IRQ15 Enabled

Card Status Change Interrupt Configuration Register (Read/Write)

Socket A: Index Value (Base + 05h)

Socket B: Index Value (Base + 45h)

This register controls interrupt steering of the card status change interrupt and the card status change interrupt enables. A **RESETDRV** clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7 thru Bit 4: Interrupt Steering for the Card Status Change Interrupt

These bits select the redirection of the card status change interrupt if the interrupt is not selected to the output on the **INTR** pin.

$\overline{\text{INTR}}$ Enable Bit (Interrupt & Gen Cntrl Reg)	IRQ Bit 3	IRQ Bit 2	IRQ Bit 1	IRQ Bit 0	Interrupt Request Level
0	0	0	0	0	IRQ Not Selected
0	0	0	0	1	Reserved
0	0	0	1	0	Reserved
0	0	0	1	1	IRQ3 Enabled
0	0	1	0	0	IRQ4 Enabled
0	0	1	0	1	IRQ5 Enabled
0	0	1	1	0	Reserved
0	0	1	1	1	IRQ7 Enabled
0	1	0	0	0	Reserved
0	1	0	0	1	IRQ9 Enabled
0	1	0	1	0	IRQ10 Enabled
0	1	0	1	1	IRQ11 Enabled
0	1	1	0	0	IRQ12 Enabled
0	1	1	0	1	Reserved
0	1	1	1	0	IRQ14 Enabled
0	1	1	1	1	IRQ15 Enabled
1	X	X	X	X	Card Status Change Interrupt on $\overline{\text{INTR}}$ pin

Bit 3: Card Detect Enable

Setting bit to one enables a card status change interrupt when a change has been detected on the $\overline{\text{CD1}}$ or $\overline{\text{CD2}}$ signals. Setting bit to zero disables the generation of a card status change interrupt when the card detect signals change state.

Bit 2: Ready Enable

Setting bit to one enables a card status change interrupt when a low to high transition has been detected on the **Ready/$\overline{\text{Busy}}$** signal. Setting bit to zero disables the generation of a card status change interrupt when a low to high transition has been detected on the **Ready/$\overline{\text{Busy}}$** signal.

Bit is ignored when the interface is configured for I/O PC Cards.

Bit 1: Battery Warning Enable

Setting bit to one enables a card status change interrupt when a battery warning condition has been detected. Setting bit to zero disables the generation of a card status change interrupt when a battery warning condition has been detected.

Bit is ignored when the interface is configured for I/O PC Cards.

Bit 0: Battery Dead Enable ($\overline{\text{STSCHG}}$)

For memory PC Cards, setting bit to one enables a card status change interrupt when a battery dead condition has been detected.

For I/O PC Cards, setting bit to one enables the PCIC to generate a card status change interrupt if the ($\overline{\text{STSCHG}}$/$\overline{\text{RI}}$) signal has been pulled low by I/O PC Card, assuming that the ring indicate enable bit in the interrupt and general control register is set to zero. Setting bit to zero disables the generation of a card status change interrupt. Bit is ignored when the interface is configured for I/O PC Cards and the ring indicate enable bit in the interrupt and general control register is set to one.

Memory and I/O Mapping

PC Card Memory Addressing

The PCIC provides access mechanisms to map portions of the 64 Mbyte common memory and/or 64 Mbyte attribute memory spaces on the PC Card into the smaller 16 Mbyte system (ISA) address space. The PCIC mapping functions provide for extension of the system side address space up to the full 64 Mbyte PC Card capability.

The PCIC has 5 independently enabled and controlled system memory address mapping windows. Each system memory window maps into either the common or attribute memory space of the PC Card. Each system memory window has independent control of memory data bus width, system bus wait states, software write protect, and enable.

Mapping of each system memory window can start and stop on any 4 Kbyte boundary of (ISA) system memory above 64 Kbyte. The PCIC does not allow mapping of a system memory window between 0 and 64 Kbyte in the (ISA) system address space. Only I/O address windows are allowed to be mapped between 0 and 64 Kbyte in the (ISA) system address space. This limitation allows the PCIC to resolve conflicts in accesses to I/O PC cards that contain memory.

For example, if a system memory window is mapped between 0 and 64 Kbyte in the (ISA) system address space, any accesses to this window will not access the memory PC Card.

To open a window, the system memory start address (FIRST), system memory stop address (LAST), and PC Card memory offset are set under software control. The PC Card memory offset address is added to the (ISA) system address to generate the address for the PC Card. The figure above shows an example of mapping a 1.4 Mbyte system memory window. The system memory window maps the memory range from 2.2 Mbyte to 3.6 Mbyte on to the PC Card memory range 320 Kbyte to 1.72 Mbyte. The PC Card memory offset address (3E18h in this example) is set by software to be equal to the 2's complement of the difference between the system memory start address (FIRST) and the start address of the PC Card.

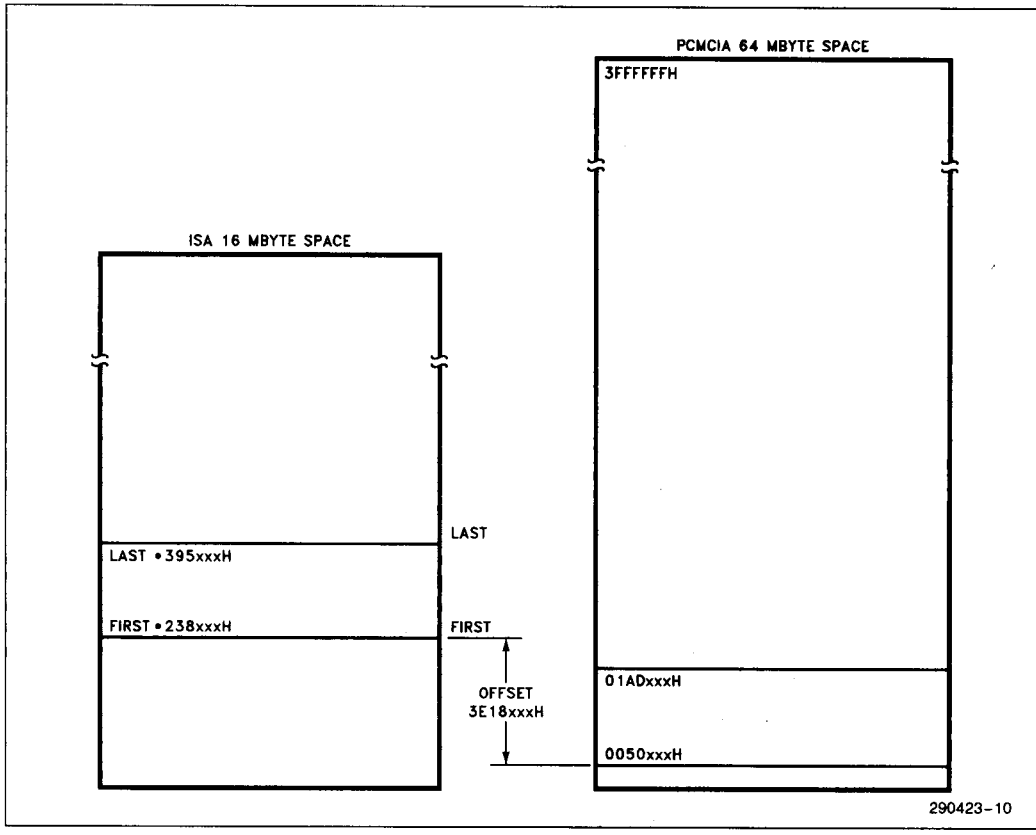
A memory PC Card is accessed when the following conditions are satisfied:

1. The system memory address mapping window is enabled;
2. The (ISA) system memory address is greater than or equal to the system memory address mapping start register A23:A12 (high and low byte);
3. The (ISA) system memory address is less than or equal to the system memory address mapping stop register A23:A12 (high and low byte).

The system memory address mapping windows can all be configured by software to be independently used, or used in concert to perform mapping for special memory mapping requirements, like LIM/EMS (Lotus-Intel-Microsoft/Extended Memory Specification) or XIP (Execute in Place).

The system memory address mapping windows allow for the placement of multiple ROM executable images on a single PC Card. These images can be aligned to start on any 4 Kbyte boundary on the memory PC Card. Access to these ROM executable images is achieved by setting the size of a system memory address mapping window to the size of the executable image (minimum 4 Kbyte block), and setting the PC Card memory offset from the system memory start address (FIRST) to generate the address of the first byte of the executable image on the PC Card.

The PC Card memory offset allows for either positive or negative (2's complement) values from the (ISA) system address. The PCIC does no checking for a window whose size and offset allow it to wrap from the last PC Card address to the first PC Card address. Software has the full responsibility for preventing the occurrence of address wrapping.



PC Card I/O Addressing

The (ISA) system bus is limited to 768 bytes of common I/O address space between the I/O address 100h and 3FFh. The PCIC supports system I/O address decode from 0 to 64 Kbytes. I/O addressing on PC Cards is very similar to memory addressing. The PC Card can request certain common I/O address locations or can request only the size of the I/O space required. When only the size of I/O space required is requested, the system is free to locate the PC Card anywhere in the 64 Kbyte system I/O address space. The PC Card will decode the **$\overline{CE2}$**, **$\overline{CE1}$**, **$\overline{IORD}$**, and **$\overline{IOWR}$** signals to respond to an I/O access.

The PCIC has two independently enabled and controlled I/O address windows which define a 16-bit address decode to achieve a 1 byte resolution. This allows for two noncontiguous I/O address windows for each PCMCIA socket. Each window has independent control of I/O data bus width, zero wait state system bus access, and generation of **$\overline{IOCS16}$**.

An I/O PC Card is accessed when the following conditions are satisfied:

1. The I/O address window is enabled;
2. The (ISA) system address is greater than or equal to the I/O address start register A15:A0 (high and low byte);
3. The (ISA) system address is less than or equal to the I/O address stop register A15:A0 (high and low byte).
4. The access is not a DMA transfer. AEN = 0 to access the I/O PC Card.

It is the responsibility of the system software to account for each I/O address range assigned to a particular PC Card. The reservation of a particular I/O address range for each PC Card can reduce card power consumption since only one PC Card is enabled during each I/O access.

The PCIC can directly map the system I/O address space to the PC Card I/O ports with single byte

granularity. Each PC Card is guaranteed a reserved system I/O address space, and an I/O cycle will be generated to the PC Card only within the assigned space. Therefore, the PCIC does not rely on the PC Card to decode the I/O address space and respond with the acknowledge signal. The PCMCIA Input Acknowledge (INPACK) signal would be required for systems that generate card enables to the PC Card over a wide range of I/O address space and rely on the PC Card acknowledge signal to enable any data transceivers between the PC Slot and the system data bus. On a read from the PC Card with an I/O address window enabled, the PCIC will qualify the data transceiver direction line and the card enables with a valid access to the PC Card I/O address space. The PCIC does not allow overlapping I/O address windows to be enabled concurrently.

Memory Paging

The paging of system memory is supported in the PCIC through the use of multiple system memory address mapping windows. When using LIM or XIP, the software assigns a window to each page required to support the LIM/XIP function. Software has the responsibility to set up the system memory address mapping windows to be in one contiguous system address space with each window controlling a single page in the PC Card memory. When changing the page pointer only the PC Card memory offset address value needs to be altered to change the mapping.

As an example, consider the use of one 64 Kbyte (ISA) system address memory space at 0D0000H-0DFFFFH with four 16 Kbyte pages (see table below). Four system memory address mapping windows would be assigned having the following system memory start and system memory stop addresses assigned to map the LIM data into system address space.

System Memory Start	System Memory Stop	Window
0D0xxxh	0D3xxxh	0
0D4xxxh	0D7xxxh	1
0D8xxxh	0DBxxxh	2
0DCxxxh	0DFxxxh	3

The PC Card memory offset address would direct the access to the correct address on the PC Card.

Attribute Memory Address Mapping

Attribute memory on the PC Card can be accessed through any of the system memory address mapping windows. This is accomplished by setting the "REG active bit" in the card memory offset address register to one. The system memory window to attribute memory can be mapped from any ISA address to any PC Card address.

Multiple system memory address mapping windows to separate attribute memory address spaces can be opened simultaneously. Each of these windows can be configured to use a different number of wait states, software write protect, and data width.

Common Memory Address Mapping

Common memory on the PC Card can be accessed through any of the system memory address mapping windows. This is accomplished by setting the "REG active bit" in the card memory offset address register to zero. The system memory window to PC Card common memory can be mapped from any ISA memory address to any PC Card memory address.

Multiple system memory address mapping windows to separate PC Card common memory address spaces can be opened simultaneously. Each of these windows can be configured to use a different number of wait states, software write protect, and data width.

I/O Registers

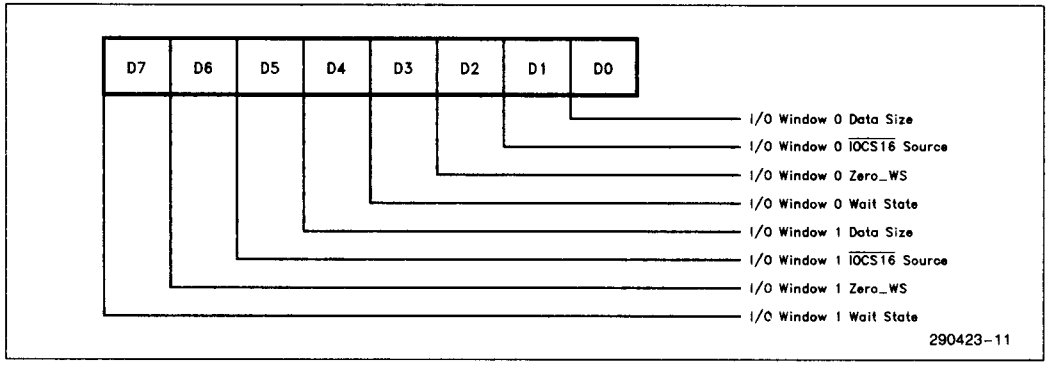
I/O Control Register (Read/Write)

Socket A: Index Value (Base + 07h)

Socket B: Index Value (Base + 47h)

This register indicates the I/O configuration for I/O window 0 and I/O window 1. This information is read from the PC Card's card information structure. Dynamic bus sizing on a cycle by cycle basis is implemented to the PC Card interface if the source of the **IOCS16** signal is the PC Card as determined by the IOCS16 source bit. In order to be compatible with some software and hardware implementations such as an IDE interface, it is necessary for the PC Card to decode two consecutive I/O addresses to determine the cycle data width. In order to meet the system bus timings, this type of PC Card must decode the address lines A9-A0 prior to the card enable signal becoming active at the interface. The card decodes the address and responds to a 16-bit cycle by enabling **IOIS16 (PCMCIA socket pin 33)**. The PCIC qualifies **IOIS16** with the card enable signals to generate **IOCS16** to the system bus.

These bits set the data path size and select zero wait states for the appropriate bus access, and are used to determine system bus signal **IOCS16**.



RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.

Bit 7: I/O Window 1 Wait State

If this bit is set to one, 16-bit system accesses occur with 1 additional wait state (4 SYSCLKs).

Bit 6: I/O Window 1 Zero Wait State

If bit is set to one, 8-bit system I/O accesses occur with zero additional wait states and the **ZEROWS** signal will be returned to the system bus. If bit is set to zero, the system I/O access will occur with additional wait states. Bit has no meaning for 16-bit I/O accesses since 16-bit system I/O accesses always occur with additional wait states.

Bit 5: I/O Window 1 IOCS16 Source

If bit is set to zero, the PCIC generates **IOCS16** based on the value of the data size bit. If bit is set to one, the PCIC generates **IOCS16** based on the **IOIS16** signal from the PC Card.

Bit 4: I/O Window 1 Data Size

A zero selects an 8-bit I/O data path to the PC Card, and a one selects a 16-bit I/O data path to the PC Card.

Bit 3: I/O Window 0 Wait State

If this bit is set to one, 16-bit system accesses occur with 1 additional wait state (4 SYSCLKs).

Bit 2: I/O Window 0 Zero Wait State

If bit is set to one, 8-bit system I/O accesses occur with zero additional wait states and the **ZEROWS** signal will be returned to the system bus. If bit is set to zero, the system I/O access will occur with additional wait states. Bit has no meaning for 16-bit I/O accesses since 16-bit system I/O accesses always occur with additional wait states.

Bit 1: I/O Window 0 IOCS16 Source

If bit is set to zero, the PCIC generates **IOCS16** based on the value of the data size bit. If bit is set to one, the PCIC generates **IOCS16** based on the **IOIS16** signal from the PC Card.

Bit 0: I/O Window 0 Data Size

A zero selects an 8-bit I/O data path to the PC Card, and a one selects a 16-bit I/O data path to the PC Card.

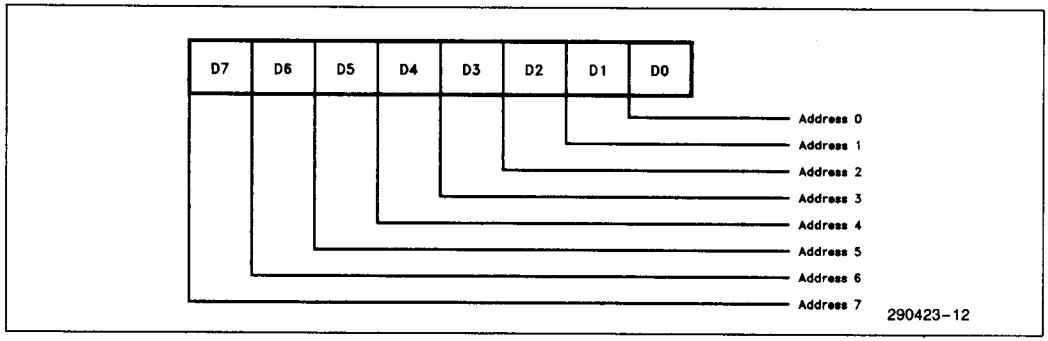
I/O Address 0 Start Register Low Byte (Read/Write)

Socket A: Index (Base + 08h)

Socket B: Index (Base + 48h)

This register contains the low order address bits used to determine the start address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



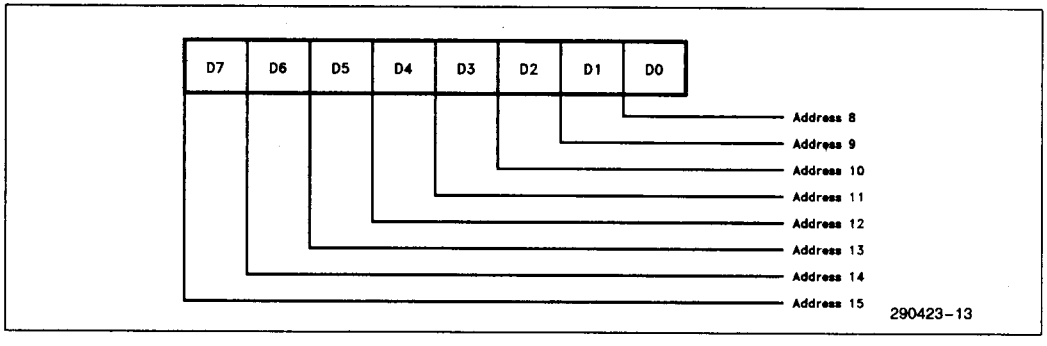
Bit 7 thru Bit 0: I/O Window 0 Start Address A7:A0

I/O Address 0 Start Register High Byte (Read/Write)

Socket A: Index (Base + 09h)
Socket B: Index (Base + 49h)

This register contains the high order address bits used to determine the start address of I/O address window 0.

RESETDRV clears all bits in this register, unless the RESETDRV is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7 thru Bit 0: I/O Window 0 Start Address A15:A8

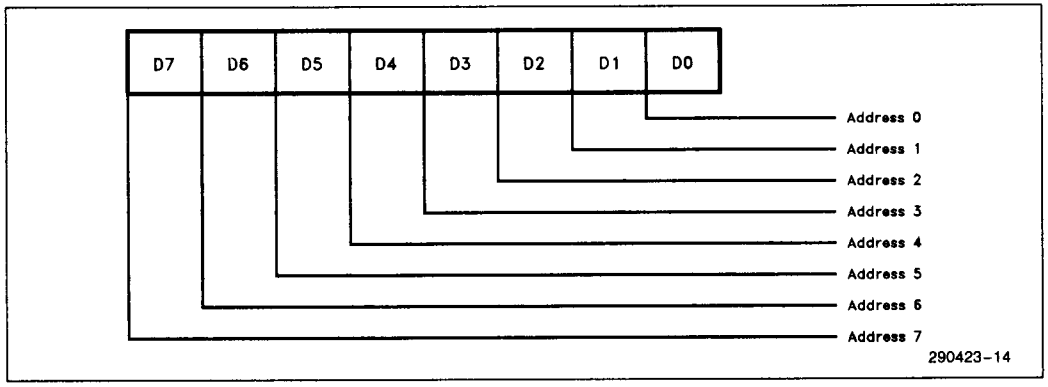
I/O Address 0 Stop Register Low Byte (Read/Write)

Socket A: Index (Base + 0Ah)
Socket B: Index (Base + 4Ah)

This register contains the low order address bits used to determine the stop address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0.

NOTE:
Do not attempt to overlay the I/O window over the top of the PCIC registers. This will cause the PCIC access type to change.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



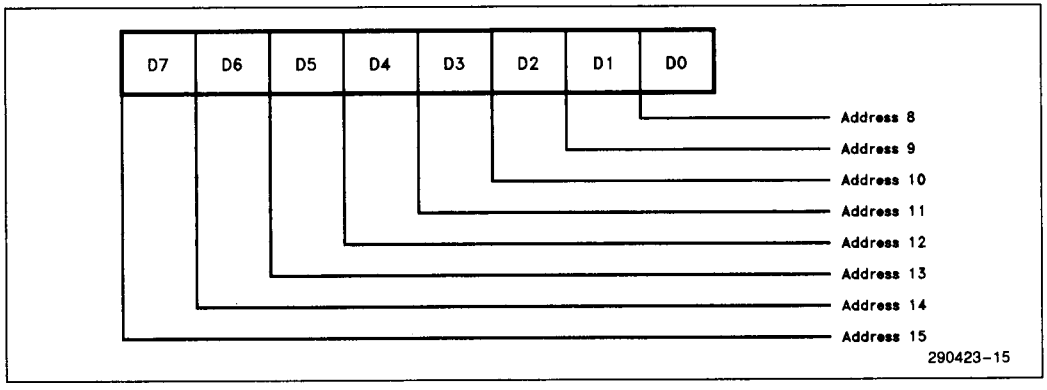
Bit 7 thru Bit 0: I/O Window 0 Stop Address A7:A0

I/O Address 0 Stop Register High Byte (Read/Write)

Socket A: Index (Base + 0Bh)
Socket B: Index (Base + 4Bh)

This register contains the high order address bits used to determine the stop address of I/O address window 0.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



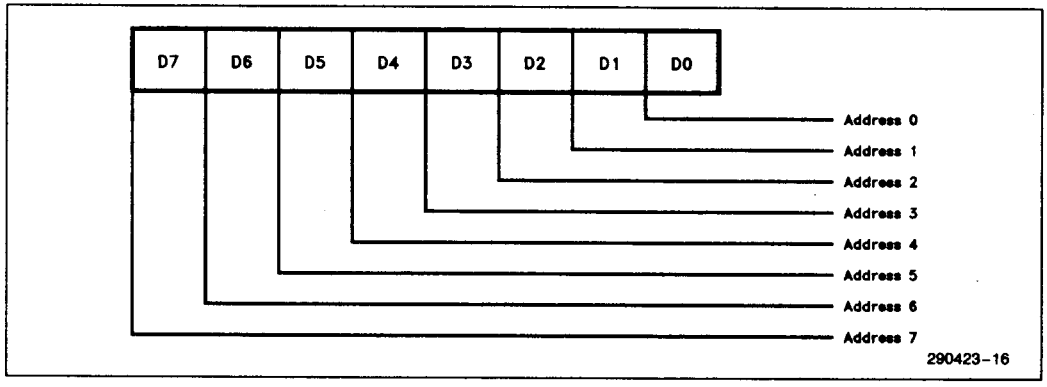
Bit 7 thru Bit 0: I/O Window 0 Stop Address A15:A8

I/O Address 1 Start Register Low Byte (Read/Write)

Socket A: Index (Base + 0Ch)
Socket B: Index (Base + 4Ch)

This register contains the low order address bits used to determine the start address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 1.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



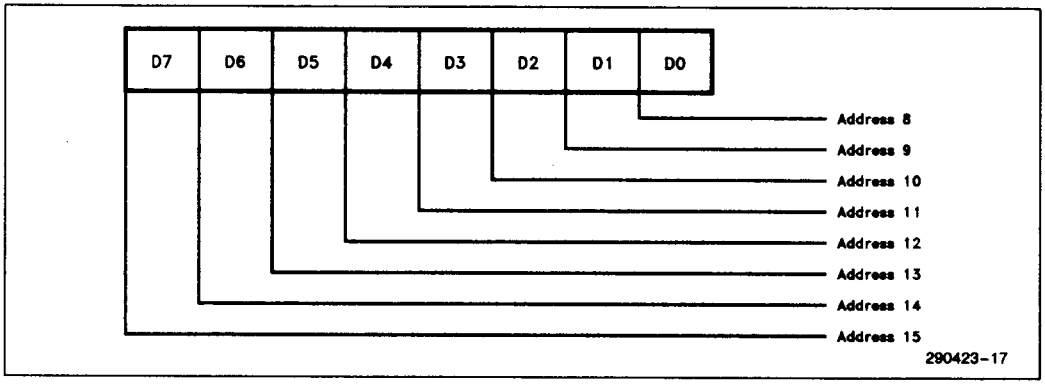
Bit 7 thru Bit 0: I/O Window 1 Start Address A7:A0

I/O Address 1 Start Register High Byte (Read/Write)

Socket A: Index (Base + 0Dh)
Socket B: Index (Base + 4Dh)

This register contains the high order address bits used to determine the start address of I/O address window 1.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



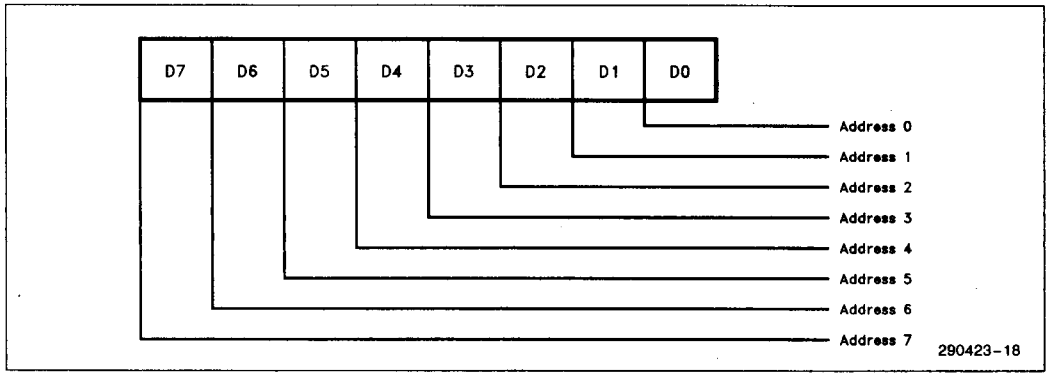
Bit 7 thru Bit 0: I/O Window 1 Start Address A15:A8

I/O Address 1 Stop Register Low Byte (Read/Write)

Socket A: Index (Base + 0Eh)
Socket B: Index (Base + 4Eh)

This register contains the low order address bits used to determine the stop address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 1.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



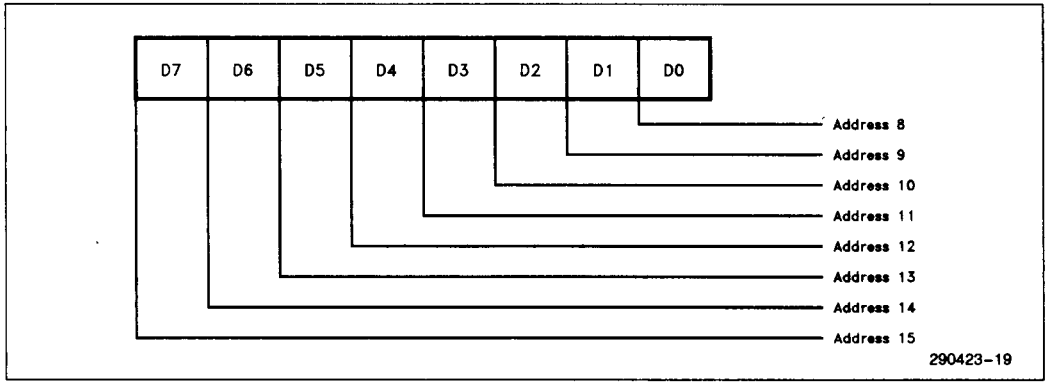
Bit 7 thru Bit 0: I/O Window 1 Stop Address A7:A0

I/O Address 1 Stop Register High Byte (Read/Write)

Socket A: Index (Base + 0Fh)
Socket B: Index (Base + 4Fh)

This register contains the high order address bits used to determine the stop address of I/O address window 1.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7 thru Bit 0: I/O Window 1 Stop Address A15:A8

Memory Registers

System Memory Address 0 Mapping Start Low Byte Register (Read/Write)

Socket A: Index (Base + 10h)
Socket B: Index (Base + 50h)

These registers contain the low order address bits used to determine the start address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4 Kbytes.

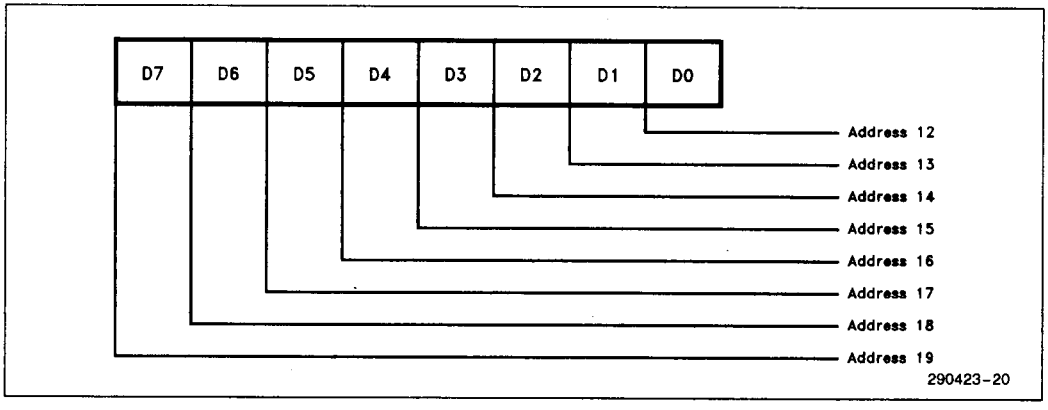
A memory PC Card is selected when the following conditions are satisfied:

1. The system memory address mapping window is enabled;
2. The (ISA) system memory address is greater than or equal to the system memory address mapping start register A23:A12 (high and low byte);
3. The (ISA) system memory address is less than or equal to the system memory address mapping stop register A23:A12 (high and low byte).

The system memory address mapping windows can all be configured by software to be independently used, or used in concert to perform mapping for special memory mapping requirements, like LIM/EMS (Lotus-Intel-Microsoft/Extended Memory Specification) or XIP (Execute in Place).

NOTE:
A memory window can not be set up below the first 64K of address space.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



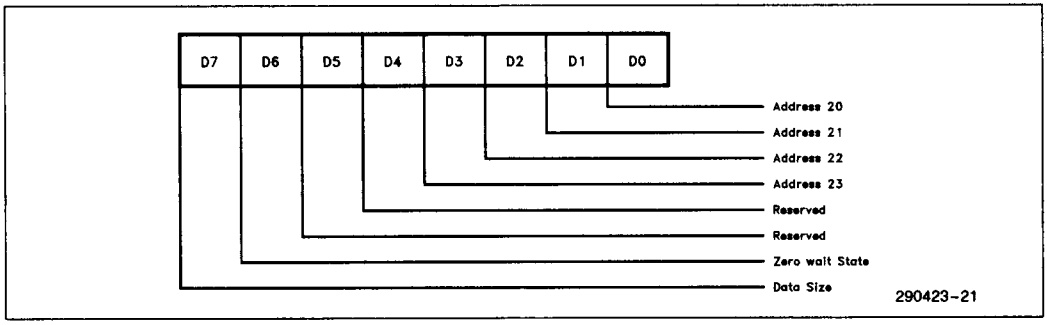
Bit 7 thru Bit 0: System Memory Window Start Address A19:A12

System Memory Address 0 Mapping Start High Byte Register (Read/Write)

Socket A: Index (Base + 11h)
Socket B: Index (Base + 51h)

These registers contain the high order address bits used to determine the start address of the corresponding system memory address mapping window. Each system memory window has a data path size associated with it which is controlled by a bit in this register. Accesses to each system memory window have the potential to occur with zero additional states which is also controlled by a bit in this register.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7: Data Size

A zero selects an 8-bit memory data path to the PC Card, and a one selects a 16-bit memory data path to the PC Card.

Bit 6: Zero Wait State

If bit is set to one, an 8-bit system memory accesses occur with zero additional wait states and the **ZEROWS** signal will be returned to the system bus. If bit is set to zero, system memory accesses will occur with additional wait states. The **Wait** signal will override this bit.

3

Bit 5 and Bit 4: Reserved

Bit 3 thru Bit 0: System Memory Window Start Address A23:A20

High order address bits used to determine the start address of the corresponding system memory address mapping window.

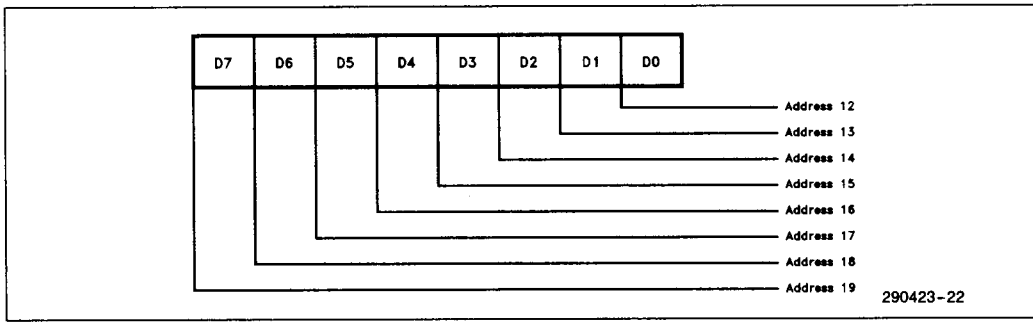
System Memory Address 0 Mapping Stop Low Byte Register (Read/Write)

Socket A: Index (Base + 12h)

Socket B: Index (Base + 52h)

These registers contain the low order address bits used to determine the stop address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4 Kbytes.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7 thru Bit 0: System Memory Window Stop Address A19:A12

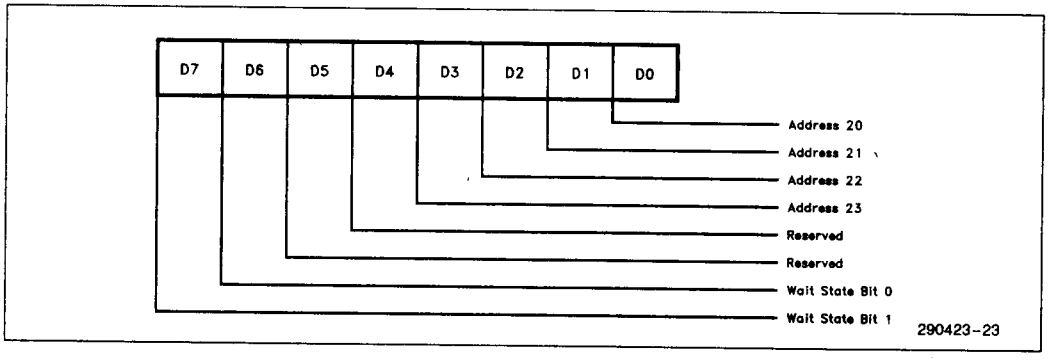
System Memory Address 0 Mapping Stop High Byte Register (Read/Write)

Socket A: Index (Base + 13h)

Socket B: Index (Base + 53h)

These registers contain the high order address bits used to determine the stop address of the corresponding system memory address mapping window. Each system memory window has the ability to extend a 16-bit system bus cycle by inserting wait states. Two bits in each of these register selects the number of wait states for a 16-bit access to the system memory window.

RESETDRV clears all bits in this register, unless the **RESETDRV** is a result of a Intel386 SL CPU resume (PWRGOOD = 1) and the disable resume RESETDRV bit is set to one in the power and RESETDRV control register.



Bit 7 and Bit 6: Wait State(s) Select

These bits determine the number of additional wait states for a 16-bit access to the system memory window. The internal wait state generator will not cause additional wait states to be inserted for an 8-bit system access even if both bits are set to one because **IOCHRDY** will be pulled high by the PCIC before the system samples **IOCHRDY**. If the PC Card supports the $\overline{\text{WAIT}}$ signal, wait states will be generated by the PC Card asserting the $\overline{\text{WAIT}}$ signal. Bits 6 and 5 should be set to zero to disable the internal wait state generator from generating wait states.

Wait State Bit 1	Wait State Bit 0	Number of Additional Wait States	# of SYSCLKs per Access
0	0	Standard 16-bit Cycle	3
0	1	1	4
1	0	2	5
1	1	3	6

Bit 5 and Bit 4: Reserved

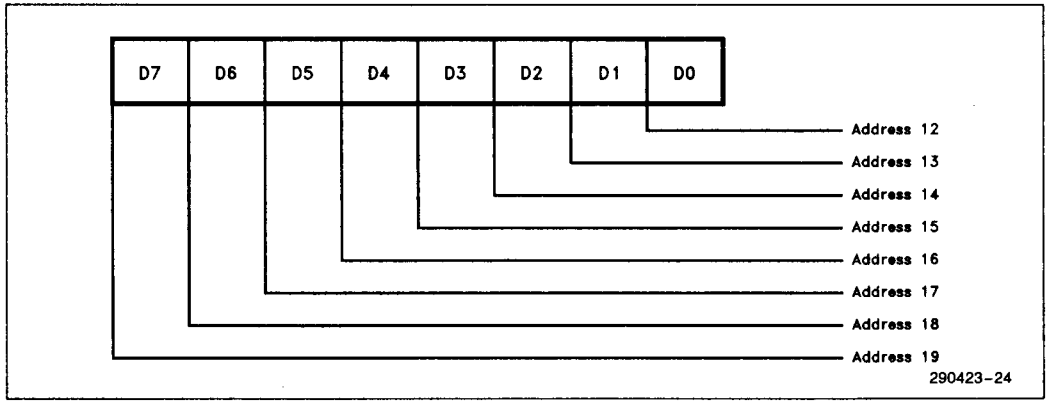
Bit 3 thru Bit 0: System Memory Window Stop Address A23:A20

High order address bits used to determine the stop address of the corresponding system memory address mapping window.

Card Memory Offset Address 0 Low Byte Register (Read/Write)

Socket A: Index (Base + 14h)
Socket B: Index (Base + 54h)

These registers contain the low order address bits which are added to the system address bits **A19:A12** to generate the memory address for the PC Card.

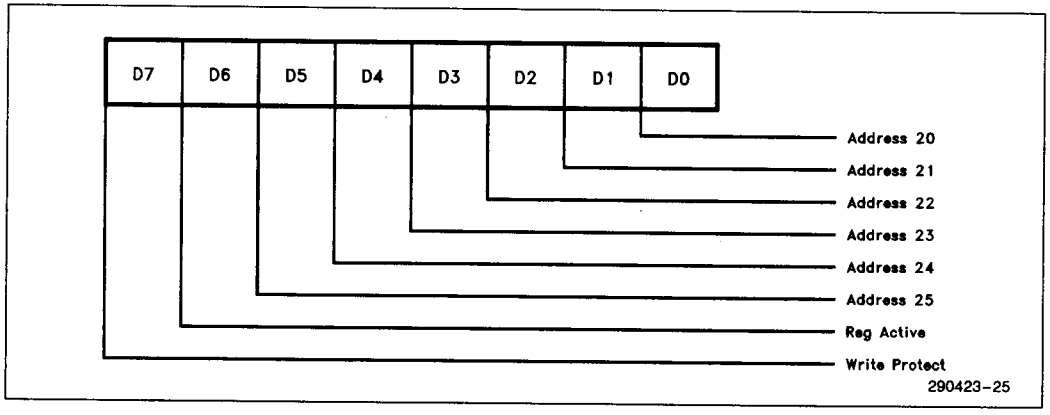


Bit 7 thru Bit 0: Card Memory Offset Address A19:A12

Card Memory Offset Address 0 High Byte Register (Read/Write)

Socket A: Index (Base + 15h)
Socket B: Index (Base + 55h)

These registers contain the high order address bits which are added to the system address bits (A23:A20) to generate the memory address for the PC Card. The software write protect of the PC Card memory for the corresponding system memory window is controlled by this register. This register also controls if the corresponding system memory window is mapped to attribute or common memory on the PC Card.



Bit 7: Write Protect

If bit is set to one, write operations to the PC Card through the corresponding system memory window are inhibited. If bit is set to zero, write operations to the PC Card through the corresponding system memory window are allowed.

Bit 6: Reg Active

If bit is set to one, accesses to the system memory window will result in attribute memory on the PC Card being accessed. If bit is set to zero, accesses to the system memory will result in common memory on the PC Card being accessed.

Bit 5 thru Bit 0: Card Memory Offset Address A25:A20

Bits A25 and A24 will be added to the system address bits A23:A20 to generate the memory address for the PC Card.

System Memory Addresses 1–4 Mapping Registers (Read/Write)

System Memory Addresses 1–4 register functions duplicate Address 0. Below are the register addresses of each of the registers.

System Memory Address 1 Mapping Start Register Low Byte

Socket A: Index (Base + 18h)
Socket B: Index (Base + 58h)

System Memory Address 1 Mapping Start Register High Byte

Socket A: Index (Base + 19h)
Socket B: Index (Base + 59h)

System Memory Address 1 Mapping Stop Register Low Byte

Socket A: Index (Base + 1Ah)
Socket B: Index (Base + 5Ah)

System Memory Address 1 Mapping Stop Register High Byte

Socket A: Index (Base + 1Bh)
Socket B: Index (Base + 5Bh)

Card Memory Offset Address 1 Low Byte

Socket A: Index (Base + 1Ch)
Socket B: Index (Base + 5Ch)

Card Memory Offset Address 1 High Byte

Socket A: Index (Base + 1Dh)
Socket B: Index (Base + 5Dh)

System Memory Address 2 Mapping Start Register Low Byte

Socket A: Index (Base + 20h)
Socket B: Index (Base + 60h)

System Memory Address 2 Mapping Start Register High Byte

Socket A: Index (Base + 21h)
Socket B: Index (Base + 61h)

System Memory Address 2 Mapping Stop Register Low Byte

Socket A: Index (Base + 22h)
Socket B: Index (Base + 62h)

System Memory Address 2 Mapping Stop Register High Byte

Socket A: Index (Base + 23h)
Socket B: Index (Base + 63h)

Card Memory Offset Address 2 Low Byte

Socket A: Index (Base + 24h)
Socket B: Index (Base + 64h)

Card Memory Offset Address 2 High Byte

Socket A: Index (Base + 25h)
Socket B: Index (Base + 65h)

System Memory Address 3 Mapping Start Register Low Byte

Socket A: Index (Base + 28h)
Socket B: Index (Base + 68h)

System Memory Address 3 Mapping Start Register High Byte

Socket A: Index (Base + 29h)
Socket B: Index (Base + 69h)

System Memory Address 3 Mapping Stop Register Low Byte

Socket A: Index (Base + 2Ah)
Socket B: Index (Base + 6Ah)

System Memory Address 3 Mapping Stop Register High Byte

Socket A: Index (Base + 2Bh)
Socket B: Index (Base + 6Bh)

Card Memory Offset Address 3 Low Byte

Socket A: Index (Base + 2Ch)
Socket B: Index (Base + 6Ch)

Card Memory Offset Address 3 High Byte

Socket A: Index (Base + 2Dh)
Socket B: Index (Base + 6Dh)

System Memory Address 4 Mapping Start Register Low Byte

Socket A: Index (Base + 30h)
Socket B: Index (Base + 70h)

System Memory Address 4 Mapping Start Register High Byte

Socket A: Index (Base + 31h)
Socket B: Index (Base + 71h)

System Memory Address 4 Mapping Stop Register Low Byte

Socket A: Index (Base + 32h)
Socket B: Index (Base + 72h)

System Memory Address 4 Mapping Stop Register High Byte

Socket A: Index (Base + 33h)
Socket B: Index (Base + 73h)

Card Memory Offset Address 4 Low Byte

Socket A: Index (Base + 34h)
Socket B: Index (Base + 74h)

Card Memory Offset Address 4 High Byte

Socket A: Index (Base + 35h)
Socket B: Index (Base + 75h)

ISA INTERFACE

The PCIC interfaces directly to a clocked ISA bus. It is fully compatible with the Intel 386SL Microprocessor SuperSet and most integrated ISA chipsets.

External Buffer and Transceiver Control

The PCIC provides control of external data transceivers and external address to provide electrical isolation between the two PC Card sockets and the (ISA) system bus. The following sections demonstrate three buffering solutions: one socket, two sockets with shared buffering and two sockets with individual socket buffering.

PCIC One Socket Solution With Socket Buffering

The solution shows the PCIC configured to support a single PC Card socket. The socket is buffered to allow for insertion and removal of PC Cards as well as power management.

PCIC Two Socket Solution With Shared Socket Buffering

The solution shows the PCIC configured to support two PC Card sockets. This configuration provides minimal chip count and board space. Power management is restricted since both sockets must be controlled together.

PCIC Two Socket Solution With Individual Socket Buffering

The solution shows the PCIC configured to individually support two PC Card sockets. While similar to the shared socket solution above, this configuration requires an additional buffer and transceiver. The benefit is that power management can now be accomplished on a socket by socket basis.

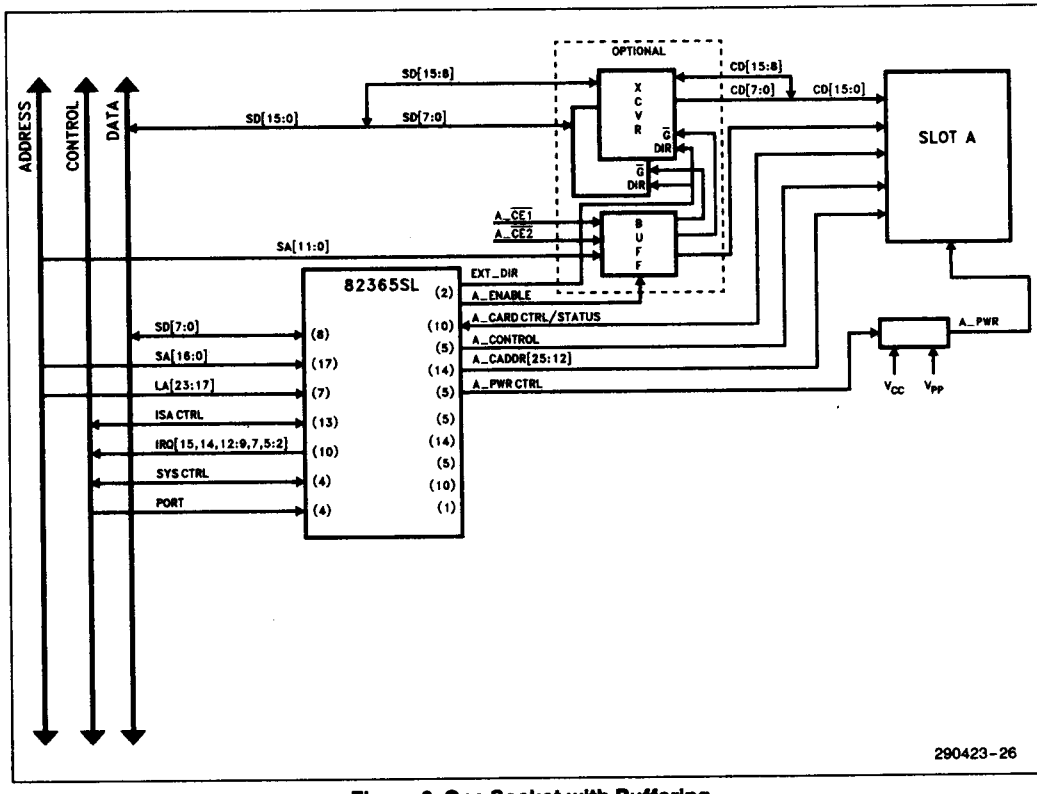


Figure 3. One Socket with Buffering

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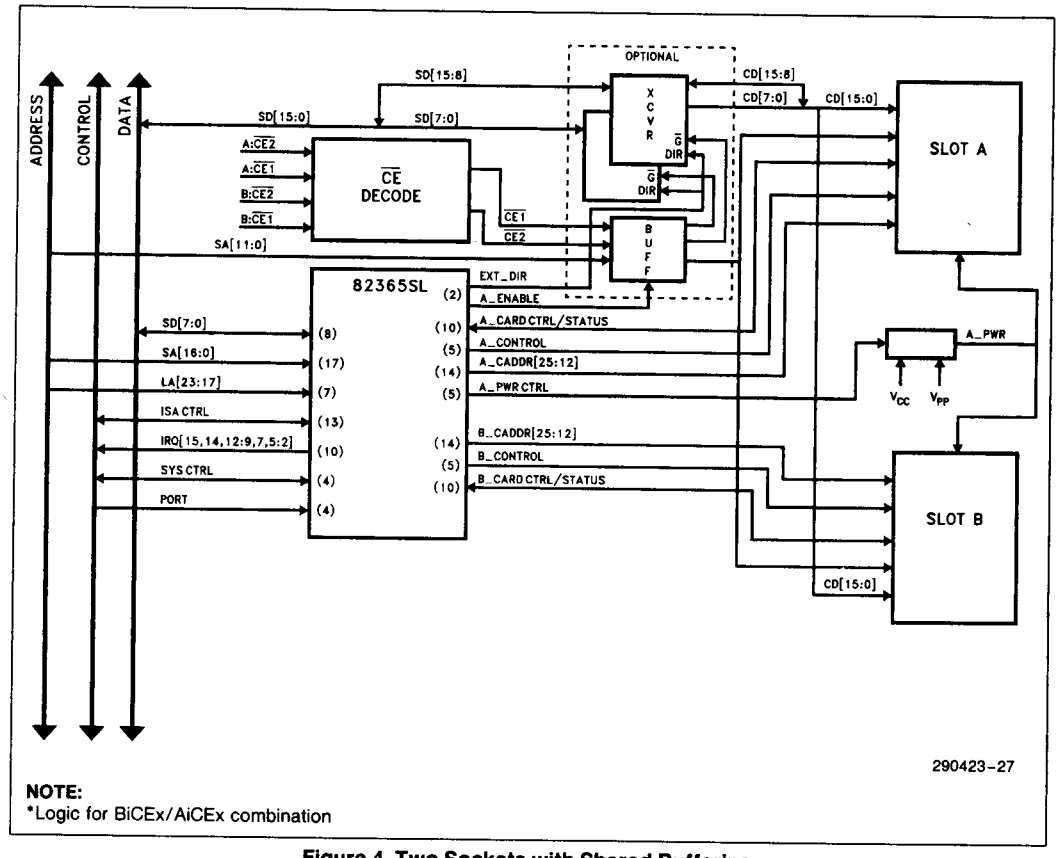


NOTE:
*Logic for BiCEx/AiCEx combination

Figure 4. Two Sockets with Shared Buffering

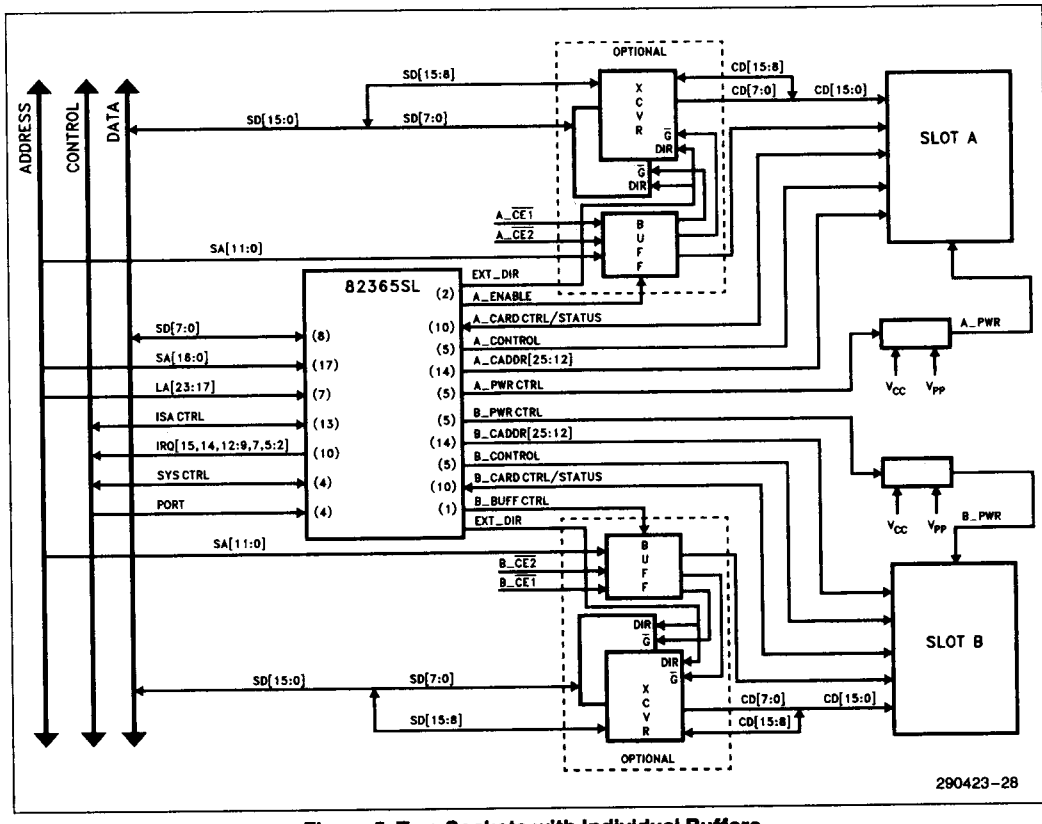


Figure 5. Two Sockets with Individual Buffers

PCMCIA/JEIDA PC Card Socket INTERFACE

The PCIC directly supports 1 or 2 PC Card sockets (designated Socket A and Socket B). Up to eight sockets can be directly supported by cascading PCICs (maximum of four supported directly), with each PCIC supporting a pair of PC Card sockets (designated Socket A and Socket B for each pair). Each PCIC is uniquely selected using the PCICs select input lines (**SEL0** and **SEL1**). This socket selection mapping is shown in the PCIC Socket Selection Mapping Table.

Each PC Card socket interface has its own compliment of memory address mapping, I/O address mapping, configuration, and status registers. The ID and revision registers are logically repeated for both interface register pairs.

All PCIC control registers are byte wide and accessed using an indirect indexing scheme. Two I/O addresses, are used to access the PCIC's control registers. The first I/O address is the PCIC's index register. The second I/O address is the PCIC's data register. Each PC Card socket can have up to 64 indirectly addressed registers. This allows for the support of two separate PC card sockets using only two I/O addresses. In order to support up to eight sockets in a system, another 2 I/O addresses are used which are selected by input lines (**SEL0** and **SEL1**). Any system conflicts with the default I/O addresses can be overcome (setting the mode bit) by using external address decode logic to map to another I/O address.

Interface Decode Logic

The interface decoding logic decodes the I/O address 3E0h and 3E1h as the address of the PCIC index and data registers respectively for sockets 0 through 3. For sockets 4 through 7, the PCIC decodes I/O addresses 3E2h and 3E3h for the index and data registers. To access one of the PCIC registers the system must first write the index value to the index register and then either read from or write to the data register. The PCIC maps Socket A and Socket B to one of four groups as defined in the PCIC Socket Selection Table. The value of the index register determines an access to the Socket A or Socket B set of interface registers as described in the Index Register Mapping Table. The index register and the data register are read/write registers. The PCIC will not respond to a data register read or write operation or to a index register read operation unless the index register has first been written to with a valid index. The index is considered valid if it is within the range determined by the **SEL1** and **SEL0** signals, which are strapping options for the PCIC.

A mismatch in the address decode will cause a clearing of all 4 of the index registers in the PCIC. This gives the designer the ability to cascade PCICs without having bus contention.

PCIC Socket Selection Mapping

SEL1	SEL0	Description
0	0	Group 0, A/B are mapped to slots 0 & 1
0	1	Group 1, A/B are mapped to slots 2 & 3
1	0	Group 2, A/B are mapped to slots 4 & 5
1	1	Group 3, A/B are mapped to slots 6 & 7

Index Register Mapping

Group	Slot A	Slot B	Base Address	Index Range
0	Slot 0		3E0h	Index = 00h to 3fh
0		Slot 1	3E0h	Index = 40h to 7Fh
1	Slot 2		3E0h	Index = 80h to BFh
1		Slot 3	3E0h	Index = C0h to FFh
2	Slot 4		3E2h	Index = 00h to 3Fh
2		Slot 5	3E2h	Index = 40h to 7Fh
3	Slot 6		3E2h	Index = 80h to BFh
3		Slot 7	3E2h	Index = C0h to FFh

PC Card Status

The status of the PC Card including PC Card detection, memory write protect status, battery voltage detect, PC Card power, and ready/busy are accessible through the interface status register. A change in PC Card status can cause a card status change interrupt (such as when a PC card is inserted or removed). The source of the interrupt is configurable.

Control/Status Signal Multiplexers

A number of the PC Card signals have different signal designations based on whether the PC Card is memory or I/O. Multiplexers are incorporated within the PCIC to redirect the appropriate signals based upon the setting of the PC Card type bit in the interrupt and general control register.

INTERRUPT STEERING

Based upon four bits in the interrupt and general control register, the interrupt request signal (**IREQ**) from an I/O PC Card will be directed to one of ten interrupt request lines on the system bus. The PCIC inverts the I/O PC Card interrupt (**IREQ**) and steers the interrupt request line to the selected system bus interrupt. The active low interrupt request of the PC Card is thus mapped to an active high system interrupt request.

The PCIC provides a card status change interrupt which can notify the system of a change in the battery voltage detects, card detects, ready/busy condition, and status change (I/O PC Cards: **STSCHG**). If this interrupt is configured as the **INTR** signal, it should be used as the **EXTSMI** input to the Intel386 SL microprocessor, or it can be directed to one of the ten interrupt request lines on the system bus based upon four bits in the card status change interrupt configuration register.

CONFIGURATION REGISTERS

Interface Configuration/Control

The PCIC provides control of the PC Card. Functions provided include bit programmable memory write protect for the attribute and common memory, **V_{CC}** power control of no connect or 5V, independent **$V_{PP}1$** and **$V_{PP}2$** power control of no connect, 5V, or 12V, and interrupt steering. The PCIC implements 10 interrupt request levels (**IRQ15**, **IRQ14**, **IRQ12:IRQ9**, **IRQ7**, **IRQ5:IRQ3**) to which the card status change interrupt and the I/O PC Card interrupt (**$\overline{IREQ}$**) can be routed.

Control of the signal multiplexers for directing the appropriate memory or I/O signals to a given socket is also provided, as well as control bits to set memory and I/O data path size.

DIGITAL AUDIO SUPPORT

The PCIC supports special signals such as digital audio. These signals are passed through to the system bus without signal conditioning. The digital audio signal (**$\overline{SPKR}$**) from each socket is logically 'OR'd to the speaker output pin (**$\overline{SPKROUT}$**) of the PCIC.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} Max	0°C to +70°C	Units
V_{IH} (TTL)	Minimum High Level Input Voltage	5.5	2.0	V
V_{IL} (TTL)	Maximum Low Level Input Voltage	5.5	0.8	V
V_{OH}	Minimum High Level Output Voltage 4 mA Buffer, I_{OH} = −4 mA 8 mA Buffer, I_{OH} = −8 mA 16 mA Buffer, I_{OH} = −16 mA	5.5	2.4	V
V_{OL}	Maximum High Level Output Voltage 4 mA Buffer, I_{OL} = 4 mA 8 mA Buffer, I_{OL} = 8 mA 16 mA Buffer, I_{OL} = 16 mA	5.5	0.4	V
I_{IL}	Maximum Input Leakage Current	5.5	±10	μA
I_{OL}	Maximum Output Leakage Current	5.5	±10	μA

3

Capacitance

Symbol	Parameter	0°C to +70°C	Units
C_{IN}	Maximum Input Capacitance	10	pF
C_{OUT}	Maximum Output Capacitance	10	pF
C_{IO}	Maximum I/O Capacitance	10	pF

Absolute Maximum Ratings*

Symbol	Parameter	Value	Units
V_{CC}	DC Power Supply Voltage	−0.5 to +7.0	V
V_{IN}, V_{OUT}	DC Input, Output Voltage	−0.5 to V_{DD} + 0.5	V
I	DC Current Drain V_{DD} and V_{SS} Pins	100	mA
T_{STG}	Storage Temperature	−55 to +150	°C
T_L	Lead Temperature	250	°C
T_{OPER}	Operating Temperature	0 to +70	°C

NOTE:
* Stress beyond those listed in this table may cause physical damage to a device and should be avoided. This table does not imply that operations at conditions above those listed in AC Timings is possible. This is a stress rating and operation of a device at or above this rating for an extended period of time may cause failure or affect reliability.

I_{CC} Specifications

Symbol	Parameter	Max	Unit
I_{CC}	Supply Current	45	mA
I_{CC1}	Supply Current/Suspend Mode Outputs Tri-stated/No Clock/Inputs Not Toggling	100	μA

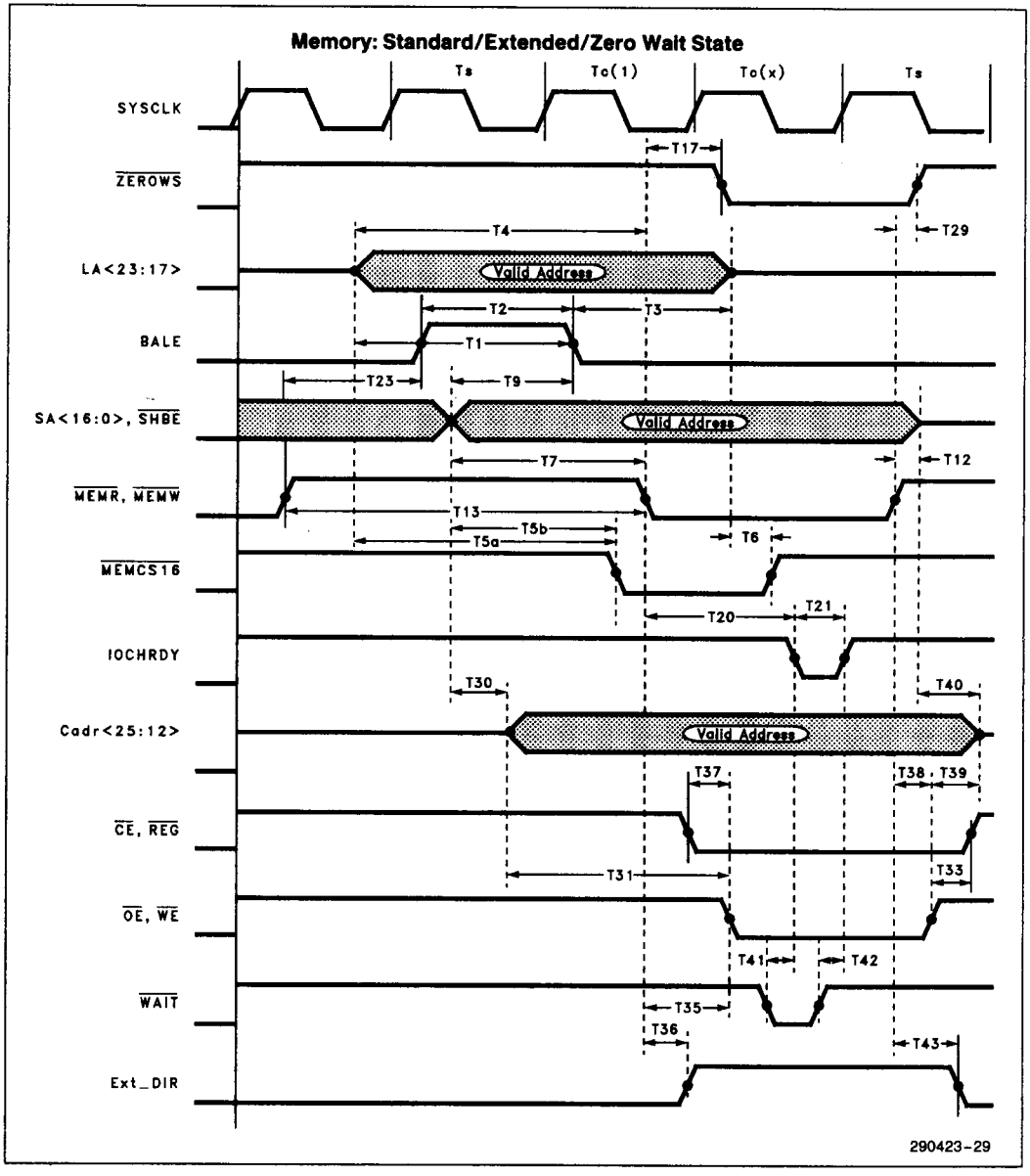
AC CHARACTERISTICS T = 0°C to +70°C, SYSCLK = 8.33 MHz, V_{CC} = 4.5V to 5.5V, T in ns

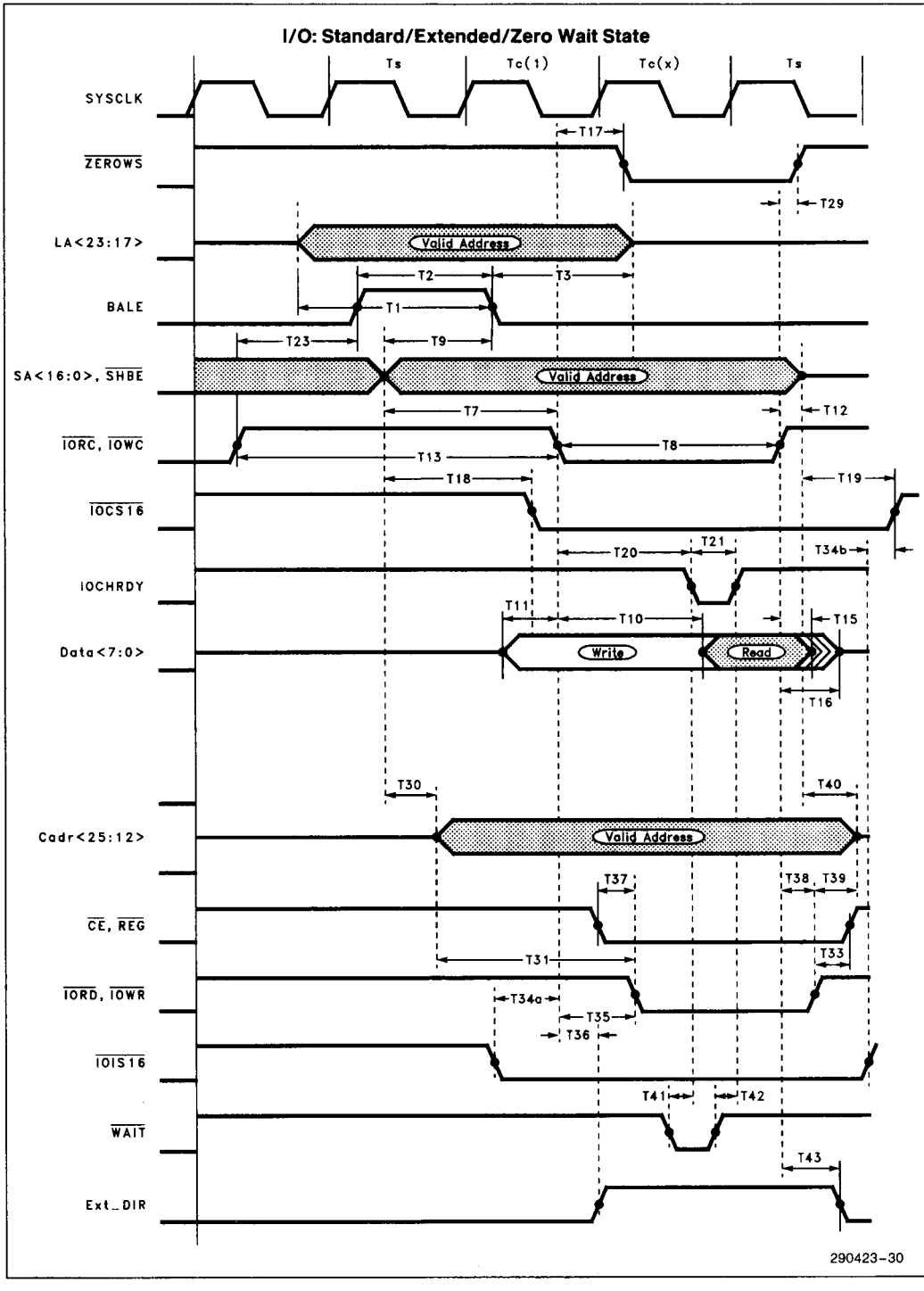
Parameter	Description	Min	Max
T1	A<23:17> Setup to BALE	93	
T2	BALE Pulse Width	48	
T3	A<23:17> Hold from BALE	15	
T4A	A<23:17> Setup to 16-Bit Memory Command	102	
T4B	A<23:17> Setup to 8-Bit Memory Command	162	
T5A	$\overline{\text{MEMCS16}}$ Valid from A<23:17>		58
T5B	$\overline{\text{MEMCS16}}$ Valid from A<16:00>		24(1) 26(2)
T6	$\overline{\text{MEMCS16}}$ Hold from A<23:17>	0	
T7A	A<16:12> and $\overline{\text{SBHE}}$ to 16-Bit Memory Command	23	
T7B	A<16:12> and $\overline{\text{SBHE}}$ to 8-Bit Memory Command	89	
T7C	A<15:00> and $\overline{\text{SBHE}}$ Setup to I/O Command	89	
T8	PCIC Register Access Command Width	480	
T9	A<16:00> and $\overline{\text{SBHE}}$ Setup to BALE Falling	26	
T10	PCIC Register Read Data Access		433
T11	PCIC Register Write Data Setup	−61	
T12	A<16:00> and $\overline{\text{SBHE}}$ Hold from Command	25	
T13	PCIC Register Access Command Off Time	159	
T15A	PCIC Register Read Data Hold	0	
T15B	PCIC Register Write Data Hold	25	
T16	PCIC Register Access Command Off to D<7:00> Tri-State		30
T17	$\overline{\text{ZEROWS}}$ Valid from A<15:00>		67
T18	$\overline{\text{IOCS16}}$ Valid from A<15:00>		67
T19	$\overline{\text{IOCS16}}$ Hold from A<15:00>	0	
T20	IOCHRDY Low from 16-Bit Command (Internal Wait State Generation)		65
T21A	IOCHRDY Active Pulse Width (Memory Cycle) (Internal Wait State Generation)	135	415
T21B	IOCHRDY Active Pulse Width (I/O Cycle) (Internal Wait State Generation)	75	115
T23	BALE Active from Command Hold	33	
T29	$\overline{\text{ZEROWS}}$ Hold from 8-Bit Command	0	
T30A	A<15:12> to CA<25:12> Valid Delay, Memory Cycles		50
T30B	A<15:12> to CA<15:12> Valid Delay, I/O Cycles		25
T31A	CA<15:12> to Socket I/O CMD Setup	70	
T31B	CA<15:12> to Socket Memory CMD Setup	30	
T33A	Socket CMD to $\overline{\text{CE}}$ Hold Time	20	

AC CHARACTERISTICS T = 0°C to +70°C, SYSCLK = 8.33 MHz, V_{CC} = 4.5V to 5.5V, T in ns (Continued)

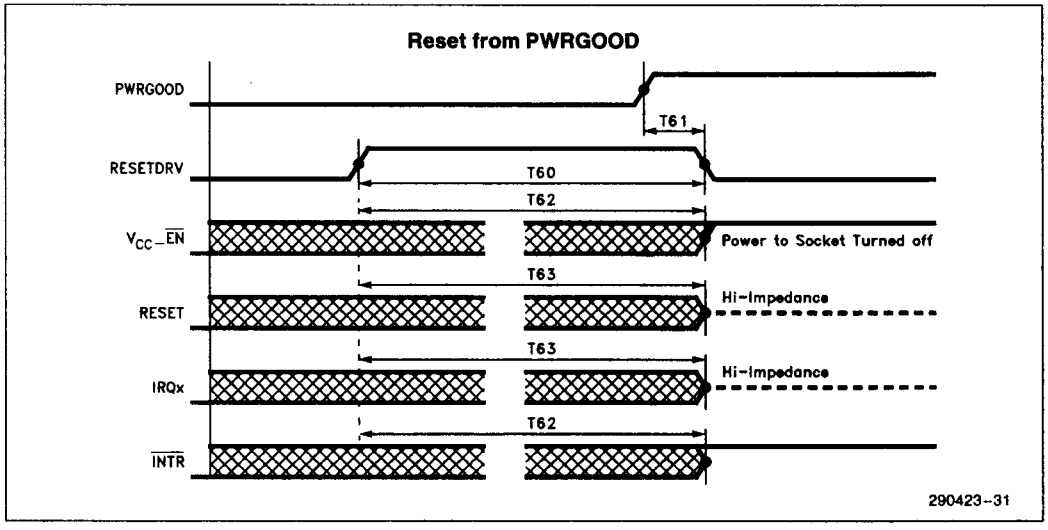
Parameter	Description	Min	Max
T33B	Socket CMD to $\overline{REG}$ Hold Time	0	
T34A	$\overline{IOIS16}$ to $\overline{IOCS16}$ Valid Delay		45
T34B	$\overline{IOCS16}$ Hold from $\overline{IOIS16}$ Valid	−30	
T35A	ISA CMD to SKT CMD Valid Delay for 8-Bit Memory, 8/16 I/O		20
T35B	ISA CMD to SKT CMD Valid for 16-Bit Memory		100
T36	ISA Read CMD Falling to EXT__DIR Rising		25
T37	$\overline{CE}$, $\overline{REG}$ Setup to Socket CMD Setup	5	
T38	ISA CMD Inactive to Socket CMD Inactive Valid Delay	0	20
T39	Socket CMD Inactive to CADR<25:12> Hold Time	20	
T40A	CA<15:12> Hold from A<15:12> Memory	0	
T40B	CA<15:12> Hold from A<15:12> I/O	0	
T41	$\overline{WAIT}$ Active to IOCHRDY Inactive		20
T42	$\overline{WAIT}$ Inactive to IOCHRDY Active	0	20
T43	EXT__DIR Hold from ISA Read Inactive	0	
T45	AEN Valid to ISA CMD Active Setup	100	
T46	AEN Hold from ISA Command Inactive	30	
T47	$\overline{CS}$ Active to PCIC Register Access CMD Active	30	
T48	$\overline{CS}$ Hold from PCIC Register Access CMD Inactive	0	
T49A	ISA Read CMD Active to $\overline{ENABLE}$ Inactive		20
T49B	$\overline{ENABLE}$ Inactive Hold Time from IS Read CMD Inactive	0	
T50	RI__ to RI__OUT Delay, SPKR__ to SPKR__OUT Delay		30
T51	Card Status Change to $\overline{INTR}$ Valid Delay		2 × BUSCLK + 50
T52	Card Status Change to $\overline{IRQ}$ Valid		BUSCLK + 50
T53	$\overline{INTR}$ Pulse Width	3 × BUSCLK	
T54	PCMCIA $\overline{IREQ}$ to IRQx Delay		50
T60	RESETDRV Pulse Width	1 μs	
T61	PWRGOOD Rising to RESETDRV Falling	5	
T62	Signal Inactive from RESETDRV Rising		200
T63	Signal Tri-State from RESETDRV Rising		200

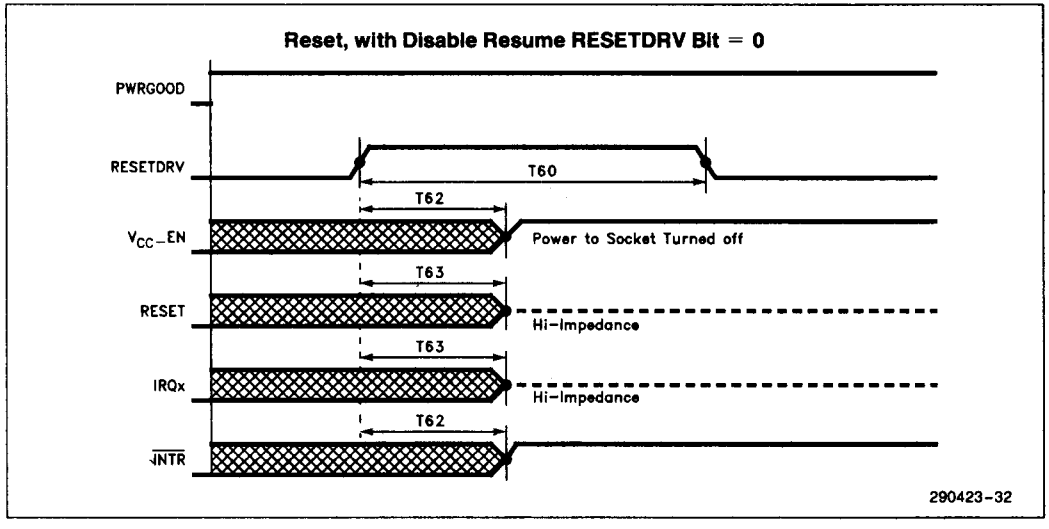
NOTES:
1. $\overline{MEMCS16}$ value based on 30 pF load.
2. $\overline{MEMCS16}$ value based on 80 pF load.

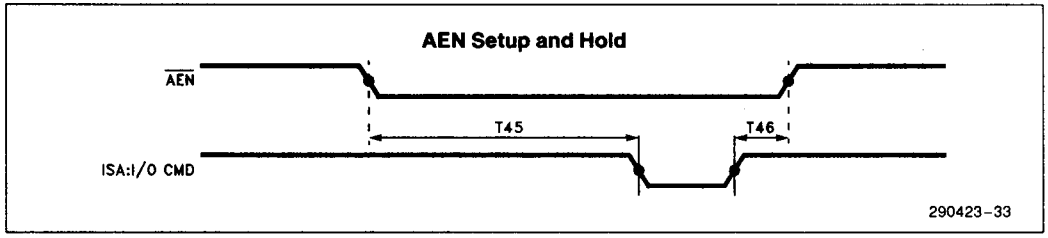

Memory: Standard/Extended/Zero Wait State
Ts
Tc(1)
Tc(x)
Ts
SYSCLK
ZEROWS
LA<23:17>
BALE
SA<16:0>, SHBE
MEMR, MEMW
MEMCS16
IOCHRDY
Cadr<25:12>
CE, REG
OE, WE
WAIT
Ext_DIR
Valid Address
T1
T2
T3
T4
T5a
T5b
T6
T7
T9
T12
T13
T17
T20
T21
T23
T29
T30
T31
T33
T35
T36
T37
T38, T39
T40
T41
T42
T43
290423-29

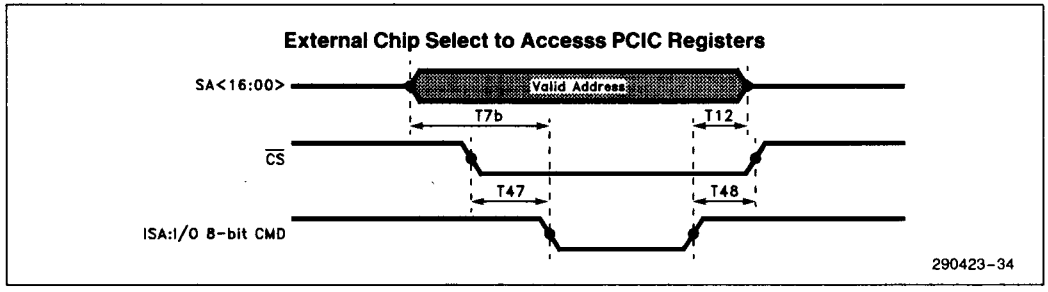

I/O: Standard/Extended/Zero Wait State
Ts
Tc(1)
Tc(x)
Ts
SYSCLK
ZEROWS
LA<23:17>
BALE
SA<16:0>, SHBE
IORC, IOWC
IOCS16
IOCHRDY
Data<7:0>
Cadr<25:12>
CE, REG
IORD, IOWR
IOIS16
WAIT
Ext_DIR
T17
T29
Valid Address
T2
T3
T1
T23
T9
Valid Address
T7
T12
T13
T8
T18
T19
T20
T21
T34b
T11
T10
T15
Write
Read
T16
T30
T40
Valid Address
T37
T38, T39
T31
T33
T34a
T35
T36
T41
T42
T43
290423-30

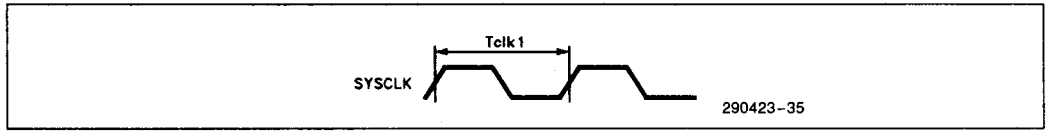
RESET


Reset from PWRGOOD
PWRGOOD
T61
RESETDRV
T60
T62
VCC–EN
Power to Socket Turned off
T63
RESET
Hi-Impedance
T63
IRQx
Hi-Impedance
T62
INTR
290423-31


Reset, with Disable Resume RESETDRV Bit = 0
PWRGOOD
RESETDRV
T60
T62
VCC–EN
Power to Socket Turned off
T63
RESET
Hi-Impedance
T63
IRQx
Hi-Impedance
T62
INTR
290423-32

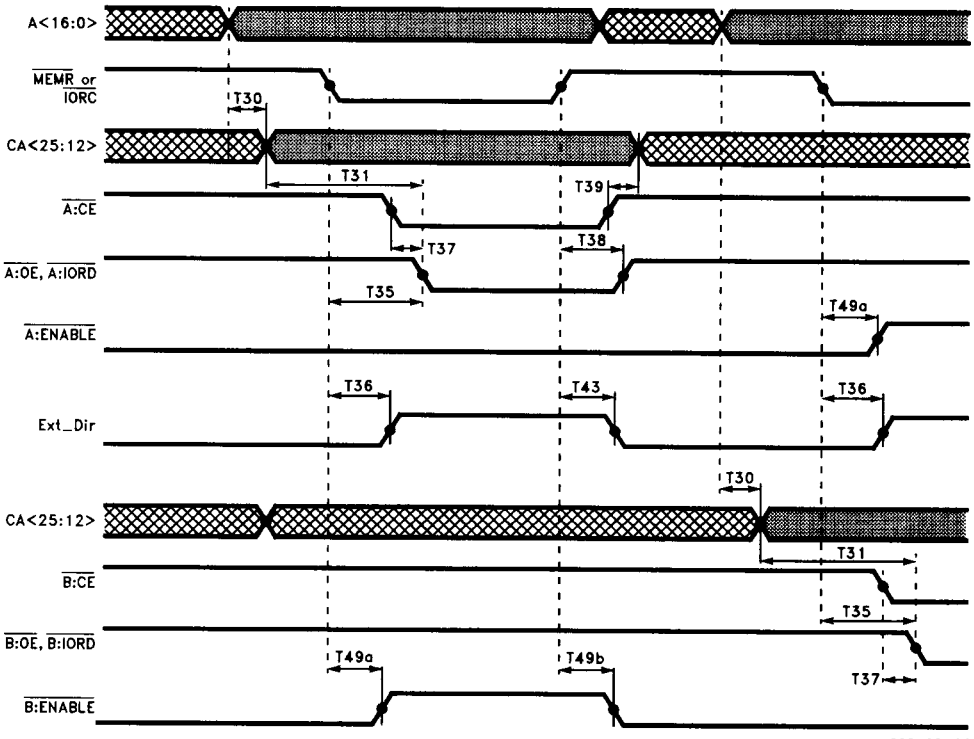






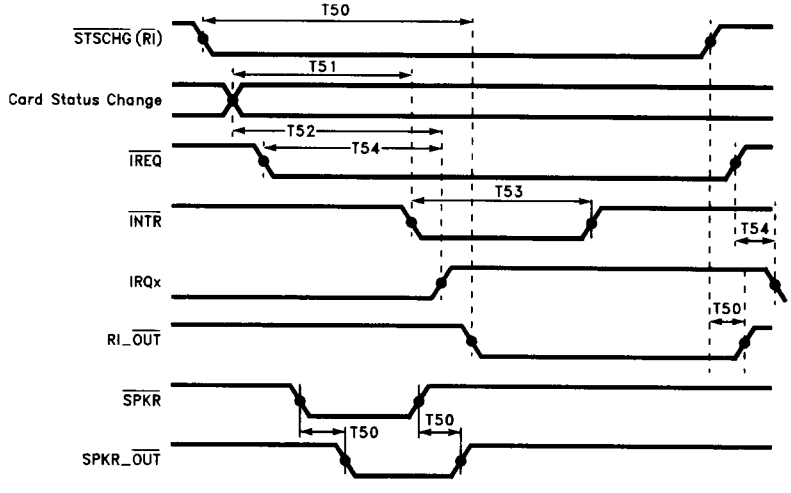
Parameter	Description	Min	Max
T_{CLK1}	SYSCLK Period	120	210

Consecutive Read Cycles to Different Sockets



290423-36

Interrupt, Ring Indicate, Speaker Timings



290423-37

PCIC PIN CHARACTERISTICS

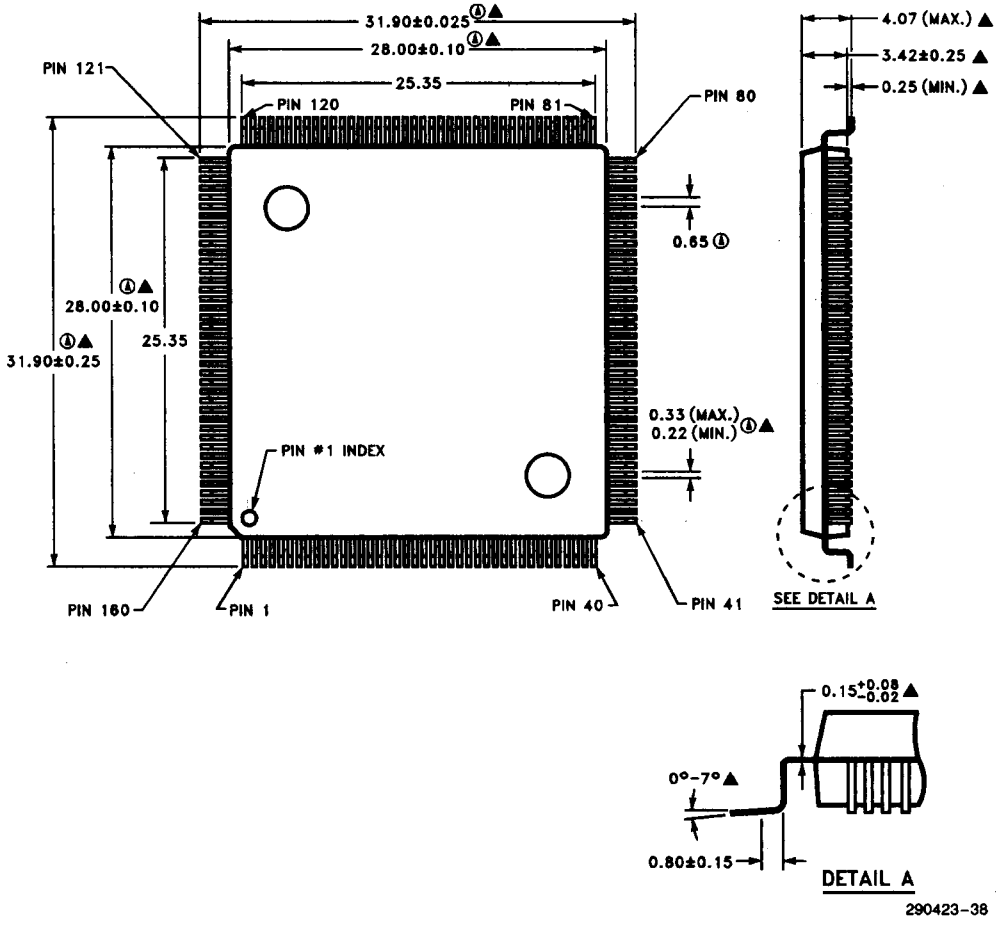
Direction	Signal Name	Characteristics
Input	A:BVD1	Schmitt Trigger 100 μA Pull Up
Input	A:BVD2	Schmitt Trigger 100 μA Pull Up
Input	A:$\overline{WAIT}$	TTL Compatible
Input	A:RDY/$\overline{BSY}$	TTL Compatible
Input	A:WP	TTL Compatible
Input	A:$\overline{CD1}$	Schmitt Trigger
Input	A:$\overline{CD2}$	Schmitt Trigger
Input	$\overline{V_{PP}\_VALID}$	TTL Compatible 25 μA Pull Up
Input	B:BVD1	Schmitt Trigger 100 μA Pull Up
Input	B:BVD2	Schmitt Trigger 100 μA Pull Up
Input	B:$\overline{WAIT}$	TTL Compatible
Input	B:RDY/$\overline{BSY}$	TTL Compatible
Input	B:WP	TTL Compatible
Input	B:$\overline{CD1}$	Schmitt Trigger
Input	B:$\overline{CD2}$	Schmitt Trigger
Input	PWRGOOD	Schmitt Trigger 100 μA Pull Up
Input	SEL0	TTL Compatible
Input	SEL1	TTL Compatible
Input	$\overline{CS}$	TTL Compatible
Input	MODE	TTL Compatible
Input	A0	TTL Compatible
Input	A1	TTL Compatible
Input	A2	TTL Compatible
Input	A3	TTL Compatible
Input	A4	TTL Compatible
Input	A5	TTL Compatible
Input	A6	TTL Compatible
Input	A7	TTL Compatible
Input	A8	TTL Compatible
Input	A9	TTL Compatible
Input	A10	TTL Compatible
Input	A11	TTL Compatible

Direction	Signal Name	Characteristics
Input	A12	TTL Compatible
Input	A13	TTL Compatible
Input	A14	TTL Compatible
Input	A15	TTL Compatible
Input	A16	TTL Compatible
Input	A17	TTL Compatible
Input	A18	TTL Compatible
Input	A19	TTL Compatible
Input	A20	TTL Compatible
Input	A21	TTL Compatible
Input	A22	TTL Compatible
Input	A23	TTL Compatible
Input	BALE	TTL Compatible
Input	RESETDRV	Schmitt Trigger 25 μA Pull Down
Input	SYSCLK	TTL Compatible
Input	$\overline{MEMW}$	TTL Compatible
Input	$\overline{MEMR}$	TTL Compatible
Input	$\overline{IOWC}$	TTL Compatible
Input	$\overline{IORC}$	TTL Compatible
Input	AEN	TTL Compatible
Input	$\overline{SBHE}$	TTL Compatible
Output	A:$\overline{OE}$	4 mA Tri-State
Output	A:$\overline{IORD}$	4 mA Tri-State
Output	A:$\overline{CE2}$	4 mA Tri-State
Output	A:RESET	4 mA Tri-State
Output	A:$\overline{WE}$	4 mA Tri-State
Output	A:$\overline{IOWR}$	4 mA Tri-State
Output	A:$\overline{CE1}$	4 mA Tri-State
Output	A:$\overline{REG}$	4 mA Tri-State
Output	A:CA12	8 mA Tri-State
Output	A:CA14	8 mA Tri-State
Output	A:CA16	8 mA Tri-State
Output	A:CA18	8 mA Tri-State
Output	A:CA20	8 mA Tri-State
Output	A:CA22	8 mA Tri-State
Output	A:CA24	8 mA Tri-State

PCIC PIN CHARACTERISTICS (Continued)

Direction	Signal Name	Characteristics
Output	A:CA13	8 mA Tri-State
Output	A:CA15	8 mA Tri-State
Output	A:CA17	8 mA Tri-State
Output	A:CA19	8 mA Tri-State
Output	A:CA21	8 mA Tri-State
Output	A:CA23	8 mA Tri-State
Output	A:CA25	8 mA Tri-State
Output	A:V_{PP}1_EN0	4 mA Output
Output	A:V_{PP}1_EN1	4 mA Output
Output	A:V_{PP}2_EN0	4 mA Output
Output	A:V_{PP}2_EN1	4 mA Output
Output	A:V_{CC}_EN	4 mA Output
Output	B:$\overline{WE}$	4 mA Tri-State
Output	B:$\overline{OE}$	4 mA Tri-State
Output	B:$\overline{IOWR}$	4 mA Tri-State
Output	B:$\overline{IORD}$	4 mA Tri-State
Output	B:$\overline{CE1}$	4 mA Tri-State
Output	B:$\overline{CE2}$	4 mA Tri-State
Output	B:$\overline{REG}$	4 mA Tri-State
Output	B:RESET	4 mA Tri-State
Output	B:CA12	8 mA Tri-State
Output	B:CA14	8 mA Tri-State
Output	B:CA16	8 mA Tri-State
Output	B:CA18	8 mA Tri-State
Output	B:CA20	8 mA Tri-State
Output	B:CA22	8 mA Tri-State
Output	B:CA24	8 mA Tri-State
Output	B:CA13	8 mA Tri-State
Output	B:CA15	8 mA Tri-State
Output	B:CA17	8 mA Tri-State
Output	B:CA19	8 mA Tri-State
Output	B:CA21	8 mA Tri-State
Output	B:CA23	8 mA Tri-State
Output	B:CA25	8 mA Tri-State
Output	B:V_{PP}1_EN0	4 mA Output
Output	B:V_{PP}1_EN1	4 mA Output

Direction	Signal Name	Characteristics
Output	B:V_{PP}2_EN0	4 mA Output
Output	B:V_{PP}2_EN1	4 mA Output
Output	B:V_{CC}_$\overline{EN}$	4 mA Output
Output	IRQ3	8 mA Tri-State
Output	IRQ4	8 mA Tri-State
Output	IRQ5	8 mA Tri-State
Output	IRQ7	8 mA Tri-State
Output	IRQ9	8 mA Tri-State
Output	IRQ10	8 mA Tri-State
Output	IRQ11	8 mA Tri-State
Output	IRQ12	8 mA Tri-State
Output	IRQ14	8 mA Tri-State
Output	IRQ15	8 mA Tri-State
Output	$\overline{ZEROWS}$	16 mA 5V Open Drain
Output	$\overline{MEMCS16}$	16 mA 5V Open Drain
Output	$\overline{IOCS16}$	16 mA 5V Open Drain
Output	IOCRCRDY	16 mA 5V Open Drain
Output	EXT_DIR	4 mA Output
Output	B:$\overline{ENABLE}$	4 mA Output
Output	A:$\overline{ENABLE}$	4 mA Output
Output	$\overline{SPKROUT}$	4 mA Output
Output	RI_$\overline{OUT}$	4 mA Output
Output	$\overline{INTR}$	4 mA Output
I/O	SD0	I = TTL Compatible, O = 8 mA
I/O	SD1	I = TTL Compatible, O = 8 mA
I/O	SD2	I = TTL Compatible, O = 8 mA
I/O	SD3	I = TTL Compatible, O = 8 mA
I/O	SD4	I = TTL Compatible, O = 8 mA
I/O	SD5	I = TTL Compatible, O = 8 mA
I/O	SD6	I = TTL Compatible, O = 8 mA
I/O	SD7	I = TTL Compatible, O = 8 mA



NOTES:
1. All dimensions are in millimeters.
A 2. Unless otherwise specified, all dimensions are nominal.
A 3. When converting from millimeters to inches, four significant digits to the right of the decimal point are necessary.

3