# Hiacms Technical Newsletter 

IBM 5415 Processing Unit
Models A and B
Theory-Maintenance Diagrams
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This Technical Newsletter provides an Appendix B for the subject publication. This TNL is for World Trade distribution anly and is not to be obsoleted with the next revision to the base manual. Pages to be inserted are:

## Appendix B

## Summary of Amendments

This TNL provides a description of the 5203 World Trade only RPQ Y91479.

Note: Please file this cover letter at the back of the manual to provide a record of changes.

## Appendix B. 5203 World Trade Only RPQ Y91479

## CONTENTS

5203 Printer Attachment Changes

| General Description | B-2 |
| :---: | :---: |
| SIO Interrupt Control | B-2 |
| Test I/O on Interrupt Pending | B-2 |
| Interrupt Control Instructions | . B-2 |
| Interrupt Request (Circuit Objectives) | . . B.3 |
| Cycle Steal Request | . . B.3 |
| Interrupt Request Diagram | . . B-4 |
| AC Control Box |  |
| AC Control Box Wiring Diag |  |


| ntroduction |  |
| :---: | :---: |
| AC/DC Voitage | B.7 |
| Basic Unit | B-8 |
| Input Power Requirements | B-8 |
| Parts Replacement | B-8 |
| Checks and Adjustments |  |
| Power Supplies and Cooling | B-10 |
| DC Bulk Supplies | B-12 |
| Power Sequence |  |
| Power Up Sequence | B. 14 |
| Normal Power Down Sequence |  |
| Thermal and Power Checks |  |
| Abnormal Power Indications |  |
| Power Check and Thermal Check Indicators | B. 18 |
| System Sequencing and Sensing Relays |  |
| Power On Sequence | B-19 |
| Abnormal Power Off |  |
| Overvoltage and Overcurrent Power Off |  |
| Sequence | B-19 |
| Undervoltage Power Off Sequence | B-19 |
| Thermal Power Off Sequence | B-19 |
| Emergency Power Off | B-19 |
| Coil/Relay Functional Descriptions |  |

## General Description

The 5203 attachment in 5415 WT RPQ works exactly as the 5203 attachment in 5410 except OP END interrupt (interrupt level 5) and Unit Record Restart feature (interrupt level 6) which are added to fit the capability of 5415 .

Notice that the Dual Feed Carriage feature is not supported by this RPQ.

The interrupt request occurs as a result of the following conditions:

1. Printing is accomplished - PRINT FL is turning off.
2. Carriage movement is finished - CARRIAGE BUSY is turned off.
3. NO OP condition is set by SIO instruction because of the error check in previous print cycle. Note that Interrupt sio error check in previous print cycle
4. The SIO skip or SIO space command is issued but carriage movement is inhibited; i.e. space $=0$, space more than Iines, skip to the line which is already in alignment.
The following two instructions are implemented by this RPQ.
1.) SIO Interrupt Control

Start $I / O$ ( $n$ code=011) is available for enabling, disabling, and/or resetting interrupt requests. This instruction is accepted unconditionally; i.e. during busy, not ready con ditions. The instruction format is shown below.

| Function | Op Code | DA | M | N | Control Code |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIO Interrupt Control | F3 | 1110 | 0 | 011 | See | Be | w |
| Control Code |  |  |  |  |  |  |  |
| Function | O | 12 | $\underline{3}$ | 4 | 5 | $\underline{6}$ | 7 |
| Enable Interrupt | 1 | Y Y | X | X | X | X | X |
| Disable Interrupt | 0 | $\mathbf{Y} \quad \mathbf{Y}$ | X | X | X | X | X |
| Reset Interrupt (Buffer Busy) | Y | Y | X | X | X | X | X |
| Reset Interrupt <br> (Carriage Busy) | Y | Y | X | X | X | X | X |

X - Don't Care - should be zero.
Y - Can be one if multiple interrupt control functions are desired, otherwise must be zero.

## 2.) Test I/O on Interrupt Pending

Operation End Interrupt Pending condition can be tested by use of a TIO ( $n$ code=011) instruction. The instruction format is shown below.
$\frac{\text { Function }}{\text { TIO Interrupt Pending }} \frac{O p \text { Code }}{21} \quad \frac{D A}{1110} \frac{M}{0} \frac{N}{011}$ Branch to Addr.

Note that additional information as to causes of interrupt requests by the 5203 attachment may be tested with existing instructions.
$\begin{array}{lll}\text { TIO } & 21 & E 2 \\ \text { TIO } & 21 & E 4\end{array}$
Printer Busy
TIO 21 E4 Carriage Busy
SNS YO E3 No Op (Byte 2, Bit 7)

Interrupt Control Instructions

|  |  | Cond <br> A | Cond <br> B |  |
| :--- | :--- | :--- | :---: | :---: |
| $\mathrm{N} \neq 3$ | Determined by 5410 attachment $\log \mathrm{ic}$ |  |  |  |
|  | SIO | Unconditionally <br> Accepted | 0 | 1 |
|  | TIOInterrupt <br> Pending | 1 | 0 |  |
|  | Interrupt not <br> Pending | 0 | 1 |  |

[^0] controI latches.

## INTEPRUPT REQUEST - CIRCUIT OBJECTIVES

All logic is assembled on one MST card placed on printer attachment board O1A-B1 in position Q2. The data flow s shown below.

Be aware that the interrupt logic is added to the logic of the 5203 attachment. If you unplug the card 02, the attachment works in the same mode as on the System $/ 3$ Model 10 except for the cycle steal priority and cycle steal assignment.

The decoder register is set every $1 / 0$ cycle at 'sample DPJ cl 5 time. The outputs of the register are decoded to determine the channel condition A or B for SIO and TIO with $\mathrm{N}=3$ code.


The Interrupt-card presents Operation End request on level 5.
This request occurs as a result of the following conditions
1.) Printing is accomplished - PRINT FL is turning off
3.) Carriage movement is finished. - Carriaqe Busy is turning off. error check in previous print cycle. Note that Interrupt sio does not set the NO-OP condition lat
4.) The SIO-skip or SIO-space issued but carriage movement is inhibited. (Example: Space $=0$, space 3 , skip to the line which is already aligned).

## CYCLE STEAL REOUEST

The Cycle Steal Request and Assignment is changed according to the table shown below.

|  |  | 5203 on M10 | 5203 on M15 |
| :--- | :--- | :---: | :---: |
| CYCLE STEAL REQUEST | CSR | 5 | 7 |
|  | CUS LINE | 5 | 7 |
|  | DBO BIF | 6 | 6 |

## UNIT RECORD RESTART (URR)

Urit record restart feature is added to 5410 printer attachment logic. If enabled the interrupt in level 6 occured when 5203 printer is going from not ready to ready.


## AC Control Box (YB 099)

The ac control box serves as an entry point for the ac line
cord it houses line filters, a master circuit breaker, and
cord it houses line filters, a master
two contactors for ac sequencing.

This AC Box is located in 5203 Printer
Power Distribution and Supply frame


K 22 5203 AC supply
K 22 distributes ac power to the +60 V printer power supply and all 5203 motor contactors.
It is picked by CPU I/O power on signal
K 212560 AC supply
K 21 distributes ac power to the 2560 MFCM for 60 Hz machines only. It is picked by CPU I/O power on signal.

## Phase Sense Relay (PSR)

PSR monitors the ac line cord at the output of the master circuit breaker. The PSR has two funcitons: 1 lsense that
voltage is present on each phase of the customers power source and 2)that they are in the correct phase sequence. The PSR will not pick if the above conditions do not exist. The System/3 emergency power off(EPO)circuit is fed through the PSR points. When this circuit is not completed the system will not power up. The ac power fault indicator is turned on.


5415 POWER SUPPLY CHANGES FOR WORLD TRADE ONLY RPQ Y91479

## POWER SUPPLY <br> ViLID FOR 5203 INSTALLATION)

 INTRODUCTION (Part 1 of 2)AC/DC Voltage
AC POWER
A The 5415 CPU supplies primary ac input power to the following devices:

1442 Card Read/Punch
2501 Card Reader
2560 MFCM ( $50 \mathrm{~Hz}-220 \mathrm{Vac}$ and above)
3277 Display
5415 Po wer Supplies
5422 Diik Drive Enclosure
5424 MFCU
5444 Disk Drives
B The RPQ Y91479 supplies primary ac powe to the 5203. It also supplies primary ac power for the 2560 when the input power is 60 hertz or 50 hertz ( 200 Vac ).

## DC POWER

A The following dc voltages are used by the 5415 A The
CPU:

- Voltages (dc) developed within the CPU:
-4 Vdc (A gate basic)
$-4 \mathrm{Vdc}(\mathrm{A}$ gate basic)
-4 Vdc (B gate feature)
+6 Vdc (basic)
+8.5 Vdc and +3.4 Vdc (basic storage)
+24 Vdc (EPO and sequencing)
-12 Vdc (BSCA feature)
$\pm 12 \mathrm{Vdc}$ (MLTA and BSCA features)
$\pm 3 \mathrm{Vdc}(1442,2501,2560$ features)
$+5 \mathrm{Vdc}(3277$ Attachment)
-30 Vdc (5444 Attachment)
- Voltages (dc) supplied by $1 / O$ devices for use by the CPU:
$\pm 3 \mathrm{Vdc}$
+6 Vdc
+12 Vcc
Voltages developed by 5444

| +6 Vdc | Voltages developed by 5444 |
| :--- | :--- |
| +12 Vdc | drive 0 for 5444 Attachment |


| $\begin{array}{l}+12 \mathrm{Vdc} \\ -36 \mathrm{Vdc}\end{array}$ |
| :--- |

+18 Vdc - Voltage developed by the 5444 for the 5444 Attachment

Note: See manual of individual I/C device for dc voltage requirements.



## INTRODUCTION (Part 2 of 2) FOR 5203 INSTALLATION) <br> Basic Unit

The primary power input (ac) is distributed to bulk supplies located in the CPU. The bulk supplies supply unregulated filtered dc to the regulator assen blies. The regulators provide the voltage regula-
 ted dc output is distributed to gates $A$ and $B$ and the appropriate $1 / O$ devices.

## Input Power Requirements

The input power requirements for System/3 are three-phase power at 30A. Domestic and World Trade input voltage requirements are

- 60 Hertz: $200 \mathrm{Vac}, 208 \mathrm{Vac}$, and 230 Vac ( $\pm 10 \%$ )

50 Hertz: $200 \mathrm{Vac}, 220 \mathrm{Vac}, 235 \mathrm{Vac}, 380$ Vac, $408 \mathrm{Vac}( \pm 10 \%)$

## Parts Replacement

The power system is designed for replacement of power supply subassemblies rather than discrete components. The exceptions include fuses, voltage regulator cards, and relays. However, in large assemblies like the primary control box or bulk to replace com ponets (filter capacitors, eta).

## Checks and Adjustments

DANGER: After the emergency power switch is opened, power is available at K1 is opened, power is available at K1 at transformer (T1) terminat.

All voltage measurements should be made in a normal enviromment (temperature between 68 degrees and 86 degrees F) with a recently calibrated Weston ${ }^{*}$ 901 meter or its equivalent.
*Trademark of Weston, Inc.


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POWER SUPPLIES AND COOLING
(Part 1 of 2)
(FOR 5203 INSTALLATION)


POWER SUPPLIES AND COOLING (Part 2 of 2)
(FOR 5203 INSTALLATION)
Notes:

1. If the primary power input is 235 Vac or $\mathbf{4 0}$ Vac an autotransformer is required to sup ply power to the 2560,2501 , or 1442 (if these features are installed).
2. Primary power for the $\mathbf{2 5 6 0}$ is supplied by the RPQ 5203 Printer on 60 Hz and 200 V ac 50 Hz Systems.
3. Resistor assembly is used to load the No. 1 bulk supply when the 6 Vdc expansion feaure is installed. Power to the 6 V regulator is supplied by the 6 Vdc expansion supply.


Each bulk power supply contains a ferro-resonant transformer with multiple secondary windings.
The transformer outputs are rectified, filtered, and
made available to dc regulators for additional regu
lation. The No. 1 bulk supply is shown in the
example. The No. 2 and No. 3 butks are similar
but contain dc bulk and bias voltages for the 4 V
regulators only.
Note: All outputs (dc bulk and bias voltages) are
floating. The outputs are referenced to ground
via external wiring.


## POWER SEQUENCE (Part 1 of 3)

These pages describe the sequential action of the system power supplies and their functional units. The purpose of the relays and coils are described n page 8-24. Reference logic pages YA102 through YA103

## Power Up Sequence

Normal conditions with system POWER switch set OFF, main CB on, line source on, and no power faults:
. K13 and K14 are not energized (EPO must not be pulled and no point to ground fault).
a. K13-1 is not picked (allows +24 V to be passed to K14-2).
b. $\mathrm{K} 14-2$ is not picked (allows +24 V to be passed through power switch section $A$ in the off position to the thermal switches to energize K2).
2. +24 Vdc control voltage is available (TP2 $=24 \mathrm{Vdc})$.
3. K1 is energized (convenience outlet on).
4. K2 is energized if:
a. No thermal switch is open.
b. +24 Vdc control is available (main CB on).

Note: Abnormal power down conditions are described on page 8-21.

Lamp test switch is active (only TH CHK and PWR CHK lights will light with lamp test).
${ }_{3}^{2}-$
we the system POWER switch to ON.
Sections $A, B$, and $C$ of the power switch transter.
Section C turns on PWP. CHK light (turns Off wher K12-2 picks) Section C is also off when, K12-2 picks). Section C is als reset while the POWER switch is set ON
. Section $B$ provides $+24 V$ control to the 5445 (if installed), 24 V control to the main storage supply, and +24 V to the n/o K6-2 contacts.
3. Section $A$ energizes K 3 coil through $\mathrm{K} 2-4$ n/o points. (The thermal relay (K2) is now held through $\mathrm{K} 2.3 \mathrm{n} / \mathrm{o}$ points.)

## K3 relay picks:

. Power (ac) is applied to all fans.
2. Power (ac) is applied to No. 1, 2, and 3 bulk power supplies and to the +6 V expansion power supply.
3. Power (ac) is applied to the main storage supply.
4. Power (ac) is applied to $\pm 3 \mathrm{~V}$ supply for 2560 (when installed).

## (2)

Eulk logic supply voltage energizes regulators:
Bras voltage ( $20 \mathrm{Vdc} \pm 10 \%$ ) is applied to -4 V (No. 1, 2, and 3) and +6 V regu lators (terminals E9 anc' E10 of each).

Bulk voltages are applied to each regula tor (terminals E1 and E2 of each)
a. 9.37 V to 11.3 Vdc to -4 V regulator b. 10.77 V to 13.5 Vdc to +6 Vdc regula tor
$46 \mathrm{Vdc}( \pm 10 \%)$ is applied to the resistor box assembly ( 30 V section).
4. Approximately 25 Vac is applied to the 12 V supply (BSCA/MLTA feature)
5. K30 is energized (senses BSCA -12V sup ply) or K 2 is energized (senses $\pm 12 \mathrm{~V}$ sup ply).
6. $\mathrm{K} 30-1$ or $\mathrm{K} 2-1$ picks (TP9 $=0 \mathrm{Vdc}$ )

Note: The $\pm 12 \mathrm{~V}$ power supply relay K2 should not be confused with K2 in the system (mounted on relay panel).

V regulators power up
Main storage supply powers up (when -4 V No. 1 output reaches -3 V ).
2. K5 is energized ( -4 V No. 1 regulator out put sense).
3. K 17 is energized $(-4 \vee \mathrm{No}$. 2 regulator output sense).
4. K19 is energized ( -4 V No. 3 feature regu lator output sense).
5. K5-1 picks (TP2 $=0$ Vdc)
6. K17-2 picks (TP3 $=0 \mathrm{Vdc})$.

K19.2 picks (TP4 $=0 \mathrm{Vdc}$ ) --4 V No. 3 feature must be installed.
8. K5-2, K17-1, and K19-1 pick (all three picked apply the start-up voltage to ter minal E 12 of the +6 V regulator)

Main storage power supply powers up:
. K8 is energized ( +8.5 V sense).
2. K8-1 picks plus $\mathrm{K} 6-2$ picked (energizes K9, K9A, and K9B; and passes +24 V to the 5203 RPQ K 21 and K 22 )
+6V reguiator powers up:
$K 6$ is energized $(+6 \mathrm{~V}$ regulator output sense).
2. K6. 1 picks (passes -30 Vac to the 5444 )
3. K6-2 picks lalong with K8-1 picked, ener gizes K9, K9A, and K9B and also passes +24 V to the 5203 RPQ K21 and K22)
4. K6-3 picks lactivates -4 V UV detection sircuit).
5. $\mathrm{K} 6-4$ picks $(\mathrm{TP5}=0 \mathrm{Vdc})$

K9, K9A, and K9B relays pick:
K9B. 1 picks (passes 7.25 Vac to tamp dis tribution TB). Clock 9 is forced on.
2. K98-2 picks (passes 41 Vac to usage meter control card).
3. K9A-1 and 3 pick (passes ac voltage to 3277).
4. K9-1, 2 and 3 pick (passes ac voltage to 1/O devices).

## (5)

+24 V supply in $5424 / 5422$ and +60 V P/S in 5203 wer up:
$K 10$ and $K 11$ are energized $1+24 V$ and +60 V sense).
2. $\mathrm{K} 10-2$ picks (TP7 $=0 \mathrm{Vdc})$
$\mathrm{K} 11-2$ picks (TP8 $=0 \mathrm{Vdc})$. K 12 is energized.
4. K 12.1 picks (passes power sequence com plete signal to the 5203 and passes +24 V plete signal to the
to 2560 feature).
5. K12-2 picks (PWR CHK light goes off).
6. K12-3 picks (inhibits K 15 from being energized during a normal power on and off sequence).
7. K12-4 picks ('power on reset' is deacti vated and clock 9 goes off).

## Power On Sequence

System is ready for processing.

NOTE 1: 24 Vdc supply is located in 5415 frame for systems without 5424/5422 installed.

Main CB On (power switch OFF)
+24 Vdc control voltage
K 1 (convenience outlets)
K2 (TH CHK light turns off)
Turn Power switch ON
K3 (ac voltage to logic supplies and fans)
K5 (-4V power on)
K5-2, K17-1 (+6V power on
K6 ( 6 V sensed)
(-30V to 5444 file)
11. (+3.4V power on)
12. ( 8.5 V power on)
13. $\mathrm{K} 8(8.5 \mathrm{~V}$ sensed
14. K9-B (lamp and meter voitage)
16. K9-A (ac volage 103277
16. K9 (ac voltage to I/O devices)
17. (+24V power on in 5424/5422) Note 1

AC Box (5203)
19. +60 V in 5203
20. $\mathrm{K} 10(+24 \mathrm{~V}$ sensed)
21. K11 ( +60 V sensed)
22. K12 (remove POR)


## POWER SEQUENCE (Part 3 of 3

## Normal Power Down Sequence

Move POWER swith to OFF.
Sections $A, B$, and $C$ of the power switch transfer.

1. Section $\mathbf{C}$ deactivates the $-4 V \cup V$ detec tion circuit. (Applies 'Ax inhibit' to $-4 V$ UV detection circuit.)
2. Section $A$ opens. K10-1 and K11-1 hold $K 3$ energized until both the +24 V supply $K 3$ energized until both the +24 V supply and +60 V supply are powered
3. Section $\mathbf{B}$ deenergizes: K9, K9A, and K9B (1/O supplies). $+3.4 / 8.5 \mathrm{~V}$ main storage supply. 5444 supplies

Main storage supply powers down.

## 1. K8 is de-nergized.

2. K8-1 drops (used in power on sequence).
3. K - 2 drops ( $\mathrm{TPG}=\mathbf{2 4} \mathrm{Vdc}$
4. K 12 is de energized
5. K12-2 drops (PWR CHK light comes on).
6. K12-3 drops (inhibits K15 from being ener gized).
7. K12-4 drops lactivates 'power on reset' to the CPU).
+60 V and +24 V supplies power down. (1/O sup plies cie energize slower than the main storage supp:y.)

K 10 and K11 are de-energized.
2. K10.2 and K 11.2 drop (TPs).
3. K10-1 and K11-1 ideenergize K3:.

## Power Off Sequence

## 1. Main CB

2. +24 Vdc control voltage

K 1 (convenience outlet) K2 (thermal interlock) K9 (a) K9A (ac volage to 3277 ) K9A (ac voltage to 3277 )
$K 22$ in $5203(+60)$
10. K 11 ( +60 Vdc sensed)
10. K11 (+60 Vdc sensed)
11. K10 $(+24 \mathrm{Vdc}$ sensed)
11. K10 +24 Vdc sensed)
12. K 12 (turn on POR)
12. K12 (turn o
13. $K 7$ in 5421
14. $K 8(+8.5 \mathrm{Va})$
14. $\mathrm{K} 8(+8.5 \mathrm{Vd}$
15. $(+3.4 \mathrm{Vdc})$
15. +3.4 Vdc )
16. K (ac voltage to logic supplies and fans)
16. K K 6 (ac voltage to to sensed)
18. $\mathrm{K} 5(-4$ Vac sensed


THERMAL AND POWER CHECKS (Part 1 of 3 )

Abnormal Power Indications
An abnormal power down can be caused by a power check or a thermal check.

A PWR CHK light indicates that one of the following has occurred:

- An abnormsl sequence down A
- An abnormal sequence up $\mathbb{B}$
- An overvoltage, overcurrent, or an undervolt An overvortage, overcu
- A thermal condition exists (TH CHK light will be on alsol D.

A thermal check indicates that one of the following areas hes overheated:

- A or B gate logic
- Bulk supply
- Regulator stack
- Main storage supply
- 5203 and 2560 supplies
- 5203 logic gate

A An abnormal power down sequence occurs only when the POWER switch is moved to OFF (the operator intends to power down the system). If all system power supplies power down as expected, no power check occurs. If they do not, the PWR CHK light stays on lcomes on during normal power down sequence) and +24 Vdc may or may not be available on one of the test points.

Any one of the following faults could cause an abnormal power down sequence.

1. Section $A, B$, or $C$ of the power switch failed to open.
2. K3 relay did not drop.
3. K9 relay did not drop.
4. K5-1 relay did not drop.


One failure is examined to show how the power supply elements react: With the POWER switch OFF, and if relay K3 fails to drop ac power con tinues to be supplied to the -4 V and +6 V regulators. Since K5, K17, and K6 are never de-energized K5-1, K17-2, and K6-4 never drop. +24 Vdc is measured on TP6. The PWR CHK light is on be cause +24 V is available through $\mathrm{K} 5-1, \mathrm{CR13}$ and K12-2.

An abnormal power doun sequence should not be confused with an overvoltage (OV) or overcurrent. (OC) fault occurring during a power down. If an OV or OC occurs during a power down sequence, the system powers down as expected and the PWR CHK light does not stay on but goes off as soon as all supplies are down. However, a fault relay (K13, K14, K16, or K18) latches so when the POWER switch is moved to ON , an immediate power check occurs with no power supply sequencing. (Normally an OV/OC causes the system to immediately power down at some point in the sequence up state or a fter all supplies are up.

B An abnormal power up sequence can occur after the POWER switch is moved to ON. This power iabilure can occur if any one of the system the sense relays fail to sense an ascociated powe supoly output. The system doss not abruptly supply aupl. The ss in moes nof abruply complete or stops sequencing up it the point of failure for some supplies +24 Vdc is measured on the TP of the suoply that failed to power up. For Example: If the main storage power supply For Example. Fine main storage power supply has an internal failure and its output never reaches
+8.5 V . K8 is not energized and relays K 8.1 and K8-2 are not transferred. With K8-1 not picked, K9, K9A, and K9B are not energized (1/O supplies). With K8-2 not picked, +24 Vdc appears at TP6. K12 is not energized and the PWR CHK light stays on.
$\mathrm{A}-4 \mathrm{~V}$ or +6 V overwoltage, overcurrent, or undervoltage power failure can be detected during normal power on. With this type of fallure tault is detected +24 V is measured on the TP of turk is deeche. 24 V is measured O IP failure, The respective regulators sense voltage and current load drain and if preset limits are exceeded a point-to-ground signal is presented on pin E8 of the respective regulator. This point-to-ground signal (ground potential) is used to energize the appropriate OV/OC sense relay which, in turn, immediately drops all system power. Undervoltage power failures also cause abrupt system power down. Two special UV detection circuits are used to sense the output of the -4 V and +6 V regulators. If either regulator's output drops below criteria, $\mathrm{K} 6 / \mathrm{K} 15$ ( +6 V UV) or K 14 ( -4 V UV) is energized and powers down the system. However, a +6 V UV does not power down the system abruptly but causes a power check with all CPU logic supplies up.

Overcurrent (OC) Power Failure Example: System is in a normal power up state.

1. A -4 V short-to-ground fault occurs (can be anywhere on the system where -4 V from the No. 1 bulk is used)
2. The fault causes excessive current drain on the $-A V$ regulator.
3. $\mathrm{A}-4 \mathrm{~V} O \mathrm{C}$ falt is sensed by the -4 V regu lator card.
4. A point-to-ground signal is presented to K13. (The ground side of K13 is normally open to ground.)
5. K 13 is energized.
6. K13-2 picks (latches K13 on)
7. K13-1 picks (TP12 = +24 Vdc). When this relay transfers, +24 Vdc control voitage is K9 in particular).
8. System powers down abruptly.
9. PWR CHK comes on as soon as K12 drops and the POWER switch stays ON

If the POWER switch is moved to OFF the PWR CHK light goes off, but comes on again each tim the swith is moved to on. The system stay latched in tail state und fle frelay

The fault relay can be reset by setting the POWER The fauk relay can be reset by seKing the PO With the POWER switch set OFF, +24 V energizes K13 coil through the closed check reset switch. With check reset open, K13 de-energizes and K13-2 drops (latch) and K13-1 drops. K2 is now energized by the +24 V control voitage and the system is ready for a normal power uo sequence.

The above description can be used similarly for -4 V OV/OC, -4 V UV , and +6 V OV/OC power failures. Only different supplies and relays are involved.

A +6 V UV power failure does not cause abrupt system power down. Instead, special solid state circuits sense the +6 V regulator output and, if +5.7 Vdc or lower is sensed, coil K6A is energized. Relay K6A-1 picks and causes K15 to energize. Then K15-4 picks and de energizes K9, K9A, and K9B. This relay drops ac power to the I/O devices, which ceuses K10 and K11 to drop. The PWR CHK light comes on, but the system does not power down since +24 V control is not interrupted to K 3 or K2.
Undervoltage control circuits are used to ensure that:
a) +6 V is always present when -30 and +24 Vdc are present in the 5444 and when +24 and +48 Vdc are present in the 2560 .
b) -4 V is always present when +6 V is present in the 5424, or CPU logic gate.

If the above is not controiled, damage results in I/O device control circuits and electro-magnetic components.

Normally a power supply itself cannot cause an OC failure. If an OC condition prevails, an I/O devica, logic circuits, or cables have caused the failure. If the supply is abnormally overioaded, an OC condition prevais over an UV condition. Even though the regulated supply voitage may drop, normaily the OC sensing by tre regulator has powered the system down before UV can be detected.

A thermal check, caused by one of the folA therma check, caused by one of the for power down in a sequencial manner rather than abruptly.

Thermal check example: System is in a normal power on state.

1. A thermal switch opens from an overheating condition.
2. $\mathbf{+ 2 4 V}$ is interrupted to K 2 coil, K 2 de-energizes.
3. $\mathrm{K} 2-3$ and $\mathrm{K} 2-4$ transfor.
4. K2-3 interrupts +24 V to K9, K9A, and K9B ( $1 / \mathrm{O}$ supplies power down) and passes +24 V to the thermal light.
5. K2-4 transfers, and $K 3$ is held energized through K10-1 and K11-1 until both the +24V power supply and the +60 V power supply are down.
6. System powers down as a normal power down sequence, except that the TH CHK light is on.
If the POWER switch is set OFF, the TH CHK light stays on if the thermal fault still exists. If the fault is corrected, moving the switch to OFF allows K2 to be energized again and the TH CHK light goes off.

## THERMAL AND POWER CHECKS

(Part 2 of 3)

## Power Check and Thermal Check Indicators

The PWR CHK light comes on during the power on sequence and goes off when the power on sequence is completed It also lights with the TH CHK light (see chart below) when an overtemps:ature condition occurs or whenever ariy power trouble is present.

A 'power on reset' occurs every time the PWR CHK lights. PWR CHK stays off if the 24 Vdc output of the control transformer/rectifier pack ( $T / R \mathrm{Pac}$ ) is missing

| Fault | POWER ON/ OFF Switch | Power Check Ind | Thermal Ind | Action |
| :---: | :---: | :---: | :---: | :---: |
| Internal Power <br> Supply Malfunction | On | On | Off | 1. Turn power off. <br> 2. Correct problem. <br> 3. Press check reset. <br> 4. Turn power on. |
| Thermal Condition | On | On | On | 1. Turn power off. <br> 2. Power check indicator goes off. <br> 3. Thermal light stays on until condition is removed. |
| Customer Power Source Loss | On | On | On | 1. Turn power off. <br> 2. All indicators turn off. <br> 3. Turn power on and continue operation. |
| Emergency Power Off (EPC) Activated | On | Off | Off | 1. Turn power off. <br> 2. Correct problem. <br> 3. Restore EPO interlock. <br> 4. Turn power on. |

## Test Points (TPs)

Test points ( $T P_{s}$ ) are on the power control box When a voltage failure occurs, check these rest points in numerical sequence to determine the voltage that failed.

If the power on sequence is not completed the PWR CHK light remains on and the TPs from TP2 to TP9 indicate where the sequence stopped.

For example, $\mathrm{a}+6 \mathrm{~V}$ regulator sequencing failure is indicated if TPs $2-4$ were zero volts and +24 V appeared at TP5.

The machine powers down in any of the conditions detected in TP10-14. Twenty-four volts is readable in TP10-14 until CHECK RESET is pressed. Loss of either the -4 V or +6 V while the machine is running powers down the system and +24 V is present at TP10-14. Loss of +24 V white the machine is running does not cause power down but activates 'power on reset' stopping operation of the machine.

For example, an overvoltage/overcurrent failure in the -4 V No. 1 regulator occurred if +24 V ap peared at TP12.


## HERMAL AND POWER CHECKS Part 3 of 3)

System Sequencing and Sensing Relays
This is a simplified diagrain of the system sequenc ing anc sensing relays. This diagram intends to how more simply how the system is powered up: K1. K2, K3, etc.

## Power On Sequence

$K 1$ picks if the 24 V control voltage is present through the EPO switch. A quick service check for this 24 V supply can be made by pressing LAMP TEST while power is off and observing the TH CHK and PWR CHK lights. If they light, the 24 V supply is present.
K2 picks if the CPU, 2560 (if installed), and 5203 thermals are closed, and all fault relays are denergized.

Note: K1 and K2 pick with the POWER switch on or off
$K 3$ picks when the POWER switch is turned ON.
K12 picks when the power on sequence is com plete.

## Abnormal Power Off

The five causes for an abnormal power off sequence are:

1. Overvoltage (OV)
2. Overcurrent (OC)
3. Undervoltage (UV)
4. Thermal loverheating - normal power off sequence)
5. Emergency power off (EPO) switch opened

Overvoltage and Overcurrent Power Off Sequence

Whenever an overvoitage or an overcurrent condition is sensed, one of the OV/OC relays, K13, K14 K 16 , or K 18 is picked. Energızing an OV/OC relay resuits in de-energizing contactor K3. De-energizing contactor K3 removes power from the logic and main storage supply.

On an abnormal power off, the power check indicator turns on to indicate a failure. Test points indicate the power supply that failed. The ener gized OV/OC relay contacts hold the relay ener gized until CHECK RESET is pressed with the POWER switch OFF.

After an overvoltage, overcurrent, or an undervoltage failure, CHECK RESET must be pressed with the POWER switch set OFF to de-energize the OV/OC/UV relay and to allow a power on sequence.

## Undervoltage Power Off Sequence

Only the -4 V and the +6 V outputs sense for undervoltage conditions. If the -4 V No. 1 regulator UV circuit senses an undervoltage condition, the -4 V UV circuit (a separate card) immediately signals the +6 V requatar to short via the SCR across the +6 V regulator output This is a +6 V simulated overcurrent condition and the OV/OC/UV relay overcurrent condition and the OV/OC/UV relay
K 14 energizes. The K14-2 contacts remove +24 V from contactor K3. Contactor K3, in turn, removes power to the logic and main storage bulk supply. This results in an immediate system power off.

Because $\mathrm{K} 14 \mathrm{OV} / \mathrm{OC} / \mathrm{UV}$ relay energizes, +24 V is present at TP 13 to indicate a +6 V power failure. However, $\mathrm{a}+6 \mathrm{~V}$ overvoltage, $\mathrm{a}+6 \mathrm{~V}$ overcurrent or a -4 V undervoltage could cause the failure condition (see MAPs, Maintenance Analysis Procedures).


## Thermal Power Off Sequence

A thermal condition causes relay $K 2$ to be denergized. The K2-3 contacts turn on the TH CHK light to indicate overheating. Power then sequences off the same as a normal power off sequence by opening the power switch circuit.

The TH CHK light and the PWR CHK light are on when the system power off sequence ends. Turning the POWER switch OFF turns off the PWR CHK light. The TH CHK light remains on until the over-temperature condition has been FF. Pow by turning the POWER switch ON.

## Emergency Power Off

Pulling the emergency power off switch removes +24 V to $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 3$, etc. causing system power to drop immediately.

Note: In a normal systemi power off state, TP2 will read +24 Vdc . Because of a system power failure (power check), +24 Vdc measured on TP2 indicates the -4 Vdc failed to sequence on

COIL/RELAY FUNCTIONAL DESCRIP TIONS (Part 1 of 3)

The coils/relays described below are classified into two groups: sequence relays or fault relays. Sequence relays allow the system to sequentially power up or power down. Fault relays identify a failing power supply and in some cases, cause the system to abruptly power down to avoid circuit/ component damage.

Sequence Relays
Fault Relays
K1 (I/OP/S)
*K2** ( $\pm 12 \mathrm{~V}$ sense)
MLTA/BSCA
K3 (bulk power)
*K5 (-4V No. 1 sense) *K6 (+6V sense)
*K8 (main storage sup.
ply sense)
K9 (1/O supply)
K9A (115 Vac distribu tion)
K9B (41 Vac and 7.25
Vac distribution)
A ${ }^{*} 10(+24 \mathrm{~V}$ sense K11 (+60V
52031
K12 (pow
sense)
*K17 (-4V No. 2 sense) *K19 (-4V No. 3 sense) *K30 (-12V sense) with medium speed BSCA and not MLTA
*These relays are also fault relays because they identify the failing power supply.

This $K 2$ is located in $\pm 12 \mathrm{~V}$ supply, and not in the sequence control box.
$\Delta$ These relays cause an abrupi system power off; all others do not.

Note: K4 and K7 are not used
24 Vdc supply is located in 5415 frame for systems without 5422/5424 installed.

## K1 Convenience Outlet (YA102)

- Pick
-24 V sequence power up - EPO switch closed (pushed in)
- Drop
- EPO switch opened (pulled out) - Loss of 24 V sequence power

Function
K1-1, 2 provides control of 115 Vac to system convenience outlets.

K2: Thermal Relay, Relay Panel (YA102)

- Pick
- System in normal power off state
- All thermal switches closed
- Drop

Any system thermal open

- Function

Function

- K2.2 not used

K2.3
a. Provides hold
POWER is $O N$.
. Interrupts hold current to K9 K9A K9 coils and drops power-on signals to 5203 and 5445 devices on a thermal fault.
Provides power to the TH CHK indicator
light when a thermal fault is detected.
d. Provides input voltage to main storage supply sequence card.

- K24
. On normal sequence on, provides a path to allow K3 to pick if no thermal fault is present.
b. Provides for sequential shutdown of K 3 on a power fault condition.
c. Inhibits -4 V UV sense after a thermal fault.
d. Drops power-up signal to main storag supply.


K2 $\pm 12 \mathrm{~V}$ Supply Sense, Located on Powe Supply (MLTA/BSCA-YA140)

- Pick
- When the MLTA $\pm 12 \mathrm{~V}$ supply output is approximately $\pm 12 \mathrm{Vdc}$.

Drop
Loss of either +12 V or -12 V output.

- Function

K2-2
a. Provides a path for +24 V to $\mathrm{TP9}$ when $\pm 12 \mathrm{~V}$ supply is not up.
b. Provides the $\pm 12 \mathrm{~V}$ link in the power com plete sequence chain.

Note: The $\pm 12$ Vdc supply is required when the MLTA feature is instalied. This suppiy is aiso used with BSCA and not MLTA if the BSCA feature contains the 1200 bps integrated mo feature contains the 1200 bps integrated moout 1200 bps modem is installed (BSCA without this modem uses -12 Vdc only).

K3 AC Voltage to Bulk Power Supply (YA102)

Pick
Transferring the power switch (section A) after being in a normal power off state.

Drop
A-4V OV/OC power fault

- A -4V UV or +6 V OV/OC power fault
- Loss of +24 V . +60 V levels after a thermat
fault.
- Loss of +24 V . +60 V levels after transferring the power switch to the "OFF" position.
- Function
- K3-1, 2, 3 controls ac distríbution to all

CPU bulk supplies:
. No. 1 logic $-4 \mathrm{~V} /+6 \mathrm{~V} /-30 \mathrm{~V}$ and 25 Vac
to $-1 \pm 12 \mathrm{~V}$ supply
. No. 2 logic -4V
d. Main storage $+8.5 \mathrm{~V} /+3.4 \mathrm{~V}$
e. -6 V expansion +6 V
f. $\pm 3 \mathrm{~V} 2560 \pm 3 \mathrm{~V}$

Note: The outputs of the +6 V regulator, +8.5 V regulator, and +3.4 V regulator have additional controlling functions.

- Provides ac voltage to all CPU cooling fans.

OIL/RELAY FUNCTIONAL DESCRIP. IIONS (Part 2 of 3)
K.5. - 4 V No. 1 (A gate) Sense (YA102A)

- Pick $\quad-\quad$ V No. 1 (A gate) output at approximately $-4 \mathrm{Vdc}$

Drop

- Loss of -4V No. 1 (A gate) output
- Function
- K5.1
a. Provides path for +24 V to TP 2 when -4 V No. 1 ( $A$ gate) level is not up.
b. Provides control of the PWR CHK light during power down sequence.
c. Provides the -4 V No. 1 (A gate) link in the power complete (K12) sequence chain. - K5.2
a. Provides the -4 V No. 1 (A gate) link in the start up control for the +6 V regul tor.


## K6. +6V Sense (YA 102A)

- Pick
-+6 V output ar aporoximately +6 Vdc
- Drop
- Loss of +6 V output
- Function

K6.1 controls distribution from -30 V di vider network to 5444 file

- K6-2 provides the +6 V up-link of the chain required to energize K9, K9A, and K9B re. lays that provide ac voltage to $1 / O$ devices attached to the system
- K6-3 provides voltage to -4 V UV sense circuit. This line ensures that a -4 V UV fault will not be sensed before the +6 V supply is up.
a. Provides a path for +24 V to TP5 when +6 V level is not up. For +24 V to appear on TP5, all -4 V supplies, -12 V or $\pm 12 \mathrm{~V}$ supply, and $\pm 3 \mathrm{~V} 2560$ supply (if installed) must be up.
b. Provides the +6 V link in the power complete sequence chain.
+6 V UV Detect (YA 102B)
- Loss of +6 V output while system is in a normal power on state.
- Drop
+6 V power restored
- Function
- K6A-1 provides path for picking the +6 UV fault relay (K15) when system is in a normal power on state, and a +6 V undervoltage is detected.

Note: K6A is energized with +24 V only when the ground side of this coil is connected ground. Transistors Q1 and Q2 sample the +6 V regulator output and if +6 V is avail ble, Q1 and Q2 do not conduct and Q2 pre sents an open circuit to the ground side of K6A and inhibits this coil from being enerized. If +6 V is not available, transistors $\mathrm{Q}^{\prime}$ and Q 2 conduct and the ground side of K6A at ground potential and allows K6A to be nergized. This causes K15 fault relay to pick which, in turn, causes a power chect (K9 drops, K10 drops, K12 drops, PWR CHK light on).

K8 Main Storage Supply Sense (YA 102A)

- Pick
_ +8.5 V output at approximately 8.5 Vdc
- Drop
- Loss of +8.5 V output
- Function
- K 8.1 provides the +8.5 V required to energize K9, K9A, and K9B relays that provide ac voltage to the I/O devices attached to the K8.2
a. Provides a path for +24 V to TP6 when +8.5 V level is not up. For +24 V to ap pear on TP6. all -4 V supplies, -12 V or $\pm 12 \mathrm{~V}$ supply, $\pm 3 \mathrm{~V} 2560$ supply lif installed) and +6 V supply must be up.
b. Provides the +8.5 V link in the power complete sequence chain.

Note: The +8.5 V supply depends on the +3.4 V supply being up. The +3.4 V supply is not associated with any reiay coil. How ever, the availability of this voltage provides a start-up to the +8.5 V supply. Hence, both must be up before K8 can pick.

K9. I/O AC Power 208/230V AC (YA102)

- Pick
-+6 V power up and +8.5 V power up
- Drop
- Any OV/UV/OC fault on -4V or +6 V
- Thermal fault
- POWER switch being set OF
- Loss of the +8.5 V level when in a normal power up state
- Function

K9-1, 2,3 controls ac voltage distribution to the following I/O devices
a. 2560
b. 2501
c. 2501
e. 5422

Note: Primary power for the 2560 is supplied by the 5203 RPQ on 60 Hz and 200 Vac 50 Hz systems.

## K9A I/O AC Power (YA102)

- Pick
- +6 V power up and +8.5 V power up

Drop

- Any OV/UV/OC fault on -4 V or +6 V Thermal fault
- POWER switch being set OFF
- Loss of the +8.5 V level when in a normal power up state
- Function

K9A-1, 3 controls ac power distribution to the 3277.

K9B 725 Vac and 41 Vac Distribution
(Lamp and Meter - YA102)

- Pick
-+6 V power up and +8.5 V power up
- Drop
- Any OV/UV/OC fault on -4 V or +6 V
- Thermal fault
- POWER switch being set OFF
- Loss of the +8.5 V level when in a normal power up state
- Function

K98-1 controls distribution of the 7.25 Vac power to the indicator lamp bus.

- K98-2 controls distribution of the 41 Vac power to the meter control card.

K10 I/O Power Sense (YA 102A)

- Pick
- $5424 / 5422+24 \mathrm{~V}$ power supplies are up
- Drop
- Loss of $5424 / 5422+24 \mathrm{~V}$ power supoly.
- Function

K10.1
a. Provides path to hold K 3 energized after a thermal fault or setting the POWER switch OFF.
b. Provides path to supply +24 V to regula tor for main storage supply sequence sense circuits.
K10-2
a. Provides a path for +24 V to TP7 when +24 V in $5424 / 5422$ is not up. For +24 V to appear on TP7, all - 4 V supolies, -12 V or $\pm 12 \mathrm{~V}$ supply, $\pm 3 \mathrm{~V} 2560$ supply (if installed). +6 V supply, and +8.5 V sup ply must be up.
b. Provides the +24 V supplies link in the power complete sequence chain.
NOTE : 24 Vdc supply is located in 5415 frame for sys tems without $5422 / 5424$ installed.

K11 +60V Sense (YA102A)

- Pick
+60 V suppiy in 5202 RPQ up to approximately $+60 \mathrm{~V}$
- Drop

Loss of +60 V output

- Function
a. Provides a path to hold K3 energized after a thermal fault or setting the POWER switch OFF.
b. Provides a path to supply +24 V to regulator for main storage supply sequence/ sense circuits.
KI. 2
a. Provides a path for +24 V to TP8 when 60 V in 5203 is not up. For +24 V to ppear on TP8, all -4 V supplies, -12 V . $\pm 12 \mathrm{~V}$ supply, $\pm 3 \mathrm{~V} 2560$ supply (if in stalled) +6 V supply, +8.5 V supply, +24 V in $5424 / 5422$
b. Provides the +60 V link in the power com piete sequence chain.

Note: While it appears that K10 and K11 have duplicate functions, the holding on of $K 3$ until +60 V to the MFCU is down (K11-1 ol is sufficient justification for K11 being present.

COIL RELAY FUNCTIONA: EESCRIP TIONS (Part 3 of 3)
$K 12$ Power Sequence Compleie
Pick
All -4 V power supplies sensed up (K.5, K17 K19). -12 V or $\pm 12 \mathrm{~V}$ power supply sensed up ( $\mathrm{K} 30, \mathrm{~K} 2$ in MLTA supply), $\pm 3 \mathrm{~V}$ power supoly sensed up ( $K 12$ ), +6 V power supply sensed up (K6), +8.5 V power supply sensed supply in 5203 sensed up (K11).

Drop

- Loss of any of the above supply outputs OV/OC fault on - 4 V or +6 V leveis - UV fault on - $4 V$ levei
- Function

K12.1
a. Provides power sequence complete to 5203 and 5424
b. Provides +24 V to 2560 switch lines (2) c. Provides control line to 341

- K12-2

3. Provides +24 V to PWR CHK light with POWER switch ON and K12 not picked, or with POWER switch OFF though K12 not picked and -4 V No. 1 supply (K5) still up
K12-3
a.
a. Enabies picking of +6 V UV fault relay ( K 15 ) but oniy after power seauence is complete (inhibits a +6 V UV fault during a normal power up and power down sequence).
a. Disables 'power on reset' signal to CPU (clock 9 no loneer on).

K13 - 4 V No. 1 (A gate) OV/OC Fault
Pick
An overvoltage or overcurrent condition de tected by -4 V No. 1 (A gate) regulato

- Drop

Pressing CHECK RESET with the POWER switch OFF
K.13-1
a. Frovides a path for +24 V to TP12.
b. Provides control of distribution of +24 V to ali sequence control circuits.

- K13-2
a. Provides a hold path for K13 requiring a manual reset to clear the fault indicator. 4 V No. 1 (A gate) UV or +6 V OV/OC Fault
- Pick

An overvoltage or overcurrent condition detected by the +6 V requiator

- An undervoltage condition dotected by the 4 V No. 1 (A-gate) UV sense circuit.
- Dro

Pressing CHECK RESET with the POWER switch OFF

- Drop
- Pressing CHECK RESET with the POWER switch OFF.
- Function

K14.?
a. Provides a hold path for K 14 requiring a manual reset to ciear the fault indica tor.
$\mathrm{K} 14-2$
a. Provides a path for +24 V to TP13
b. Provides control of distribution of +24 V to all sequence control circuits.

## - K14.3 not used.

a. Inhibits picking of K15 when K 14 picked.

Note: K14-4 and K15-1 are used to prevent picking twe fault relays when a power fault (OV/OC) occurs. When the system abruptly powers dowri and K3 is dropped, a race condition (to power down) exists for the -4 V and +6 V supplies. $\mathrm{K} 14-4$ and K 15.1 elimir ate erroneous test point indications.


## K15 +6V UV Fault

$K 15$ is used as a +6 V UV detection sense relay and as a $\pm 3 \mathrm{~V}$ sequence sense ( 2560 feature) relay.

- Pick

A UV condition causing K6A. $1 \mathrm{n} / \mathrm{o}$ points to close with power complet (K12.3 n/o points closed) and no -4 V UV fault or +6 V OV/OC fault (K $14-4 \mathrm{n} / \mathrm{c}$ points closed).

- Drop
- Pressing CHECK RESET with the POWER switch OFF
- Function
- K15-1
a. Inhibit +24 V to TP7 on +6 V UV condition
$\mathrm{K} 15-2$
a. Provides a path for +24 V to TP14
K.
$K$
$15-3$
a. Provides a hold path for K 15 requiring a manuat !ese: to clear the fault indicato K 15.4
a. Provides control of +24 V to K9. K9A. and K9B coil's and power up signal to 5203 RPG


## K16 - 4 V No. 2 OV/OC Faul

- Pick

An overvoltage or overcurrent conditior id tected bv $-4 \vee$ No. 2 requlator.

- Drop

Pressing CHECK RESET with PCWER switch

- Function
- K16-1
a. Provides a path for +24 V to $T P 1$
b. Provides control of distribution of +24 V to all sequence control circuits.
K16-2
a. Provides a hold path for K 16 requiring a manual reset to clear the fault indicator.


## $K 17$

- Pick
$-4 \vee \mathrm{No}$. 2 output at approximately -4 Vd
- Drop

Loss of -4V No. 2 output

- Function
- K17.1
a. Provides the -4 V No. 2 link in the start up control for the +6 V requlator
- K17.2
a. Provides a path for $+24 V$ to TP3 when -4 V No. 2 level is not up. For +24 V to appear on TP3, -4V No. 1 (A gate) and $-4 \vee$ No. 3 supplies must be up.
b. Provides the -4 VNo .2 link in the power complete sequence chain.


## K18 -4V No. 3 OV/OC Fault

- Pick
- An overvoltage or overcurrent condition de tected by -4 V No. 3 regulator.
- Drop
- Pressing CHECK RESET switch with POWER switch OFF.
- Furction

K18-1
a. Provides a path for +24 V to TP10.
b. Provides control of distribution of +24 V to all sequence control circuits.
K .18 .2
a. Proviciss a hold path for K 18 requiring a manuè reset to clear the fault indicator

K19 - AV No. $\Xi$ Sense

- Pick
$-4 V$ No. 3 output at approximately -4 Vdc
- Drop
- Loss of -4 V No. 3 output
- Function

K19.1
a. Provides the -4 V No. 3 link in the start up control for the +6 V regulator

- K19-2
a. Provides a path for +24 V to TP4 when -4 V No. 3 level is not up. For +24 V to appear on TP4, -4V No. 1 (A gate) sup ply must be up.
b. Provides the -4 V No. 3 link in the power complete sequence chain.


## K30 -12V Supply Sense (BSCA)

- Pick RSCA -12V supply output is at approx imately -12 Vdc .
- Loss of -12 V supply output
- Function
- K30-1
a. Provides a path for +24 V to TP9 when the -12 V supply is not up.
b. Provides the -12 V link in the power complete sequence chan.

Note: If MLTA and BSCA features are in stalied. a $\pm 12 \mathrm{~V}$ supply is instalied instead of the -12 V suppiy in that case, K2 is used to sense its output.


[^0]:    The decoded SIO N3 signal is used to inhibit setting of NO OP latch in attachment and as a set-reset signal of interrupt

