IBM System/36

IBM System/36
Processing Unit and Channel Maintenance Information Manual
Stage 3

Order Number
SY31-9035-0

Section 10

First Edition (October 1986)

IBM has prepared this maintenance manual for use by hardware service representatives in the maintenance or repair of the specific machines indicated. IBM makes no representations that it is suitable for any other purpose.

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Preface

This manual contains the maintenance information necessary to service the System/36 processing unit and channel. This manual includes maintenance procedures, FRU descriptions, interface descriptions, and sequence of events sections to aid in diagnosing machine failures not found by the MAPs.

This manual uses a specific range of words so that the text can be understood by customer engineers in countries where English is not the normal language.

It is assumed that the hardware service representative using this manual has been trained on System/36, as described in the *System/36-5360 New Product Planning Technical Service Letter*.

About This Manual

The service procedures in this manual are numbered.

- The MAPs can send you to a specific procedure in this manual.
- Other System/36 MIMs can send you to a specific procedure in this manual.
- Steps in a procedure in this manual can send you to another procedure in this manual or in other System/36 MIMs.
- The index can send you to procedures where key words can be found.

Related Publications

System/36 Hardware Publications

- *General Maintenance Information Manual*, SY31-8999
- *Data Storage Attachment Maintenance Information Manual*, SY31-9001
- *51TD Diskette Drive and Adapter Maintenance Information Manual*, SY31-9003
- *Work Station Attachment Maintenance Information Manual*, SY31-9004
- *10SR Disk Drive and Adapter Maintenance Information Manual*, SY31-9005
- *72MD Diskette Magazine Drive and Adapter Maintenance Information Manual*, SY31-9006
- *Data Communications Attachment Maintenance Information Manual*, SY31-9007
- *3262 Printer Attachment Maintenance Information Manual*, SY31-9008
- *Power Maintenance Information Manual*, SY31-9009
- *8809 Tape Adapter Maintenance Information Manual*, SY31-9010
- *Single-Line Communications Attachment Maintenance Information Manual*, SY31-9017
- *Eight-Line Communications Attachment Maintenance Information Manual*, SY31-9018
- *1255 MCR Attachment Maintenance Information Manual*, SY09-1026
- *Local Area Network Attachment Maintenance Information Manual*, SY31-9021
- *6157 Tape Adapter Maintenance Information Manual*, SY31-9037

Other System Publications

- *Control Storage Service Information Manual*, LY31-0650

Safety

Danger and Caution Notices

In the System/36 maintenance manuals, the word *DANGER* informs you of conditions that could cause personal injury or death. (The word *HAZARDOUS* or *WARNING* may appear on labels on machines and field-supply items.) The word *CAUTION* informs you of an action that could cause damage to a program, to a device or system, or to data.

There are blank lines below each notice. You can translate these notices and write your own words on the blank lines.

Danger Notices

A danger notice appears on page vii of this Safety section under "Electrical Accidents–First Aid."

Danger notices also appear in the following procedures:

10-320 Opening Covers
10-325 Control Panel Removal

Caution Notices

A caution notice appears in the following procedure:

10-325 Control Panel Removal

Rules for Safety

If you know the safety rules for working with electrical and mechanical equipment and you observe the rules, you can work safely with IBM equipment.

Do not fear electricity, but respect it.

While you are maintaining IBM equipment, observe every safety precaution possible and the following safety rules.

Work Environment

- Do not work alone in hazardous conditions or near equipment that has dangerous voltage. Always inform your manager if the conditions or voltages are a possible problem.
- Always look for possible hazards in your work environment. Examples of hazards are: moist floors, nongrounded extension cables, power surges, and missing grounds.
- Do not perform any action that makes the product unsafe or that causes hazards for customer personnel.
- Before you start the equipment, ensure that other personnal are not in a hazardous position.
- Do not wear loose clothing that can be trapped in the moving parts of a machine. Ensure that the sleeves of your clothing are fastened or are rolled above the elbow.
- Insert your necktie into your clothing or fasten it with a clip (preferably nonconductive) at approximately 8 centimeters (3 inches) from its end.
- Lift the equipment or parts by standing or pushing up with your stronger leg muscles; this action removes the strain from the muscles in your back. Do not lift any equipment or parts that are too heavy for you.
- Put removed machine covers in a safe place while you are servicing the machine. Reinstall the covers before returning the machine to the customer.
- Always keep your tool kit away from walk areas so that other persons cannot trip over it. For example, keep the kit under a desk or table.
- Observe good housekeeping practices in the area of the machines while you are performing maintenance and after completing it.
- After maintenance, reinstall all safety devices, such as guards, shields, labels, and grounding devices. Exchange safety devices that are worn or defective. Remember, the safety devices protect you from a hazard. You destroy their purpose if you do not reinstall them when you have completed the service call.

Electrical Safety

- If possible, always disconnect the power-supply cables before you work on a machine. When you switch off power at the wall box, lock the switch in the off position or attach a DO NOT OPERATE tag (Z229-0237) to the switch.

  Note: *A non-IBM attachment to an IBM machine may be powered from another source and may be controlled by a different switch or circuit breaker.*

- Switch off all power before:
  - Removing or assembling the main units of the equipment
  - Working near power supplies
  - Inspecting power supplies
  - Installing changes in machine circuits
- If you really need to work on equipment that has exposed live electrical circuits, observe the following precautions:
  - Ensure that another person who understands the power off controls, is near you. Another person must be there to switch off the power, if necessary.
  - Do not wear jewelry, chains, metal-frame eyeglasses, or other personal metal objects. Remember, if the metal touches the machine, the flow of current increases because the metal is a conductor.
  - Use only insulated probe tips or extenders. Remember, worn or cracked insulation is unsafe.
  - Use only one hand while you are working on live equipment. Keep the other hand in your pocket or behind your back. Remember, there must be a complete circuit for an electrical shock to occur. This precaution prevents your body from completing the circuit.
  - When you use a tester, set its controls correctly and use insulated probes that have the correct electrical specification.
  - Do not touch objects that are grounded, such as metal floor strips, machine frames, or other conductors. Use suitable rubber mats obtained locally, if necessary.
- When you are working with machines having voltages more than 30 Vac or 42 Vdc, observe the special safety instructions given in customer engineering memorandums (CEMs).
- Never assume that power has been removed from a circuit. First, ensure that power has been removed.
- Do not touch live circuits with the surface of a plastic dental mirror. Remember, the surface of the dental mirror is conductive and can cause damage or personal injury.
- If an electrical accident occurs:
  - Use caution. Do not be a victim yourself.
  - Switch off the power.
  - Instruct another person to get medical aid.
  - If the victim is not breathing, perform mouth-to-mouth rescue breathing. See "Electrical Accidents—First Aid."

Mechanical Safety

Do not touch moving mechanical parts when you are lubricating a part, checking for play, or doing other similar work.

Safety Glasses

Wear safety glasses when:

- Using a hammer to drive pins or other similar parts
- Using a power drill
- Using a spring hook to attach or remove a spring
- Soldering parts
- Cutting wire or removing steel bands
- Using solvents, chemicals, or cleaners to clean parts
- Working in any other conditions that could injure your eyes

Tools, Testers, and Field-Use Materials

- Do not use tools or testers that have not been approved by IBM. Ensure that electrical hand tools, such as Wire-Wrap[1] tools and power drills, are inspected regularly.
- Exchange worn or broken tools or testers.
- Do not use solvents, cleaners, or lubricants that have not been approved by IBM.

Summary

Prevention is the main aid to electrical safety. Always think about electrical safety and use good practice; for example:

- Ensure that the customer's power receptacle matches the IBM equipment specifications.
- Inspect power cables and plugs; check for loose, damaged, or worn parts.
- Review the procedures in the maintenance documents before you remove a part that can hold an electrical charge from the machine. Carefully discharge the necessary parts exactly as instructed by the procedure.

Never assume that a machine or a circuit is safe. No machine is always completely safe. You may not know the exact condition of a machine because, for example:

- The power receptacles could be wrongly wired.
- Safety devices or features could be missing or defective.
- The maintenance or machine level change history could be wrong or not complete.
- The design could have a problem.
- The machine could have been damaged when it was shipped.
- The machine could have an unsafe change or attachment.
- An engineering change or a sales change could be wrongly installed.
- The machine could be deteriorated because it is old, or because it operates in an extreme environment.
- A part could be defective, therefore causing a hazard.
- A part could be wrongly assembled.

These are some of the ways that the condition of the machine could affect safety. Before you start a service call or procedure, have good judgment and use caution.

Electrical Accidents—First Aid

When performing rescue procedures for an electrical accident, do as follows:

- *Use Caution:* If the victim is touching the electrical-current source, remove the power. To do this, you may need to operate the room emergency power-off switch or the disconnecting switch. If you cannot find the switch, use a dry wooden rod or other nonconductive object to pull or push the victim away so he or she is not touching the electrical-current source.
- *Work Quickly:* If the victim is unconscious, he or she may need mouth-to-mouth rescue breathing and possibly external cardiac compression if the heart is not beating.
- *Get Medical Aid:* Instruct another person to dial the rescue service (such as the ambulance or the hospital).

Determine if the victim needs mouth-to-mouth rescue breathing. If he or she does, perform the following steps:

DANGER

Use extreme care when you perform rescue breathing for a victim who may have breathed in toxic fumes. Do not breathe in air that the victim has breathed out.

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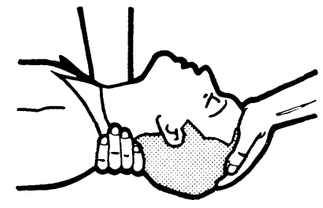
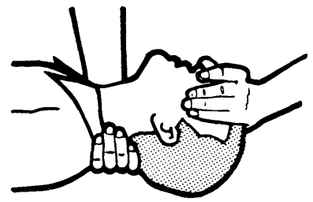
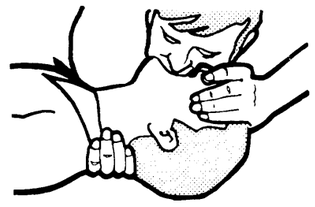
1. Prepare for rescue breathing:
   a. Ensure that the victim's airway is open and that it is not obstructed; check the mouth for objects that may be obstructing the airway, such as chewing gum, food, dentures, or the tongue.
   b. Place the victim on his or her back, put one hand behind the victim's neck, and put the other hand on his or her forehead.
   c. Lift the neck with one hand, and tilt the head backward by pressing on the forehead with the other hand.



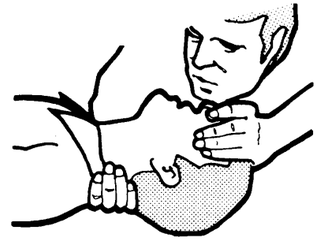
2. Look, listen, and feel to determine if the victim is breathing freely.
   a. Put your cheek near the victim's mouth and nose.
   b. Listen and feel for the breathing out of air. At the same time, look at the victim's chest and upper abdomen to see if they move up and down.
3. If the victim is not breathing correctly:
   a. Keep the victim's head tilted backward. Continue to press on the forehead with your hand; at the same time, position the same hand so that you can pinch together the victim's nostrils with your thumb and finger.



   b. Open your mouth wide and take a deep breath. Make a tight seal with your mouth around the victim's and blow into the victim's mouth.



   c. Remove your mouth to let the victim breathe out, and check that the victim's chest moves down.



   d. Repeat steps b and c once every 5 seconds either until the victim breathes for himself or herself, or until medical aid comes.

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1 Trademark of the Gardner-Denver Co.

Reporting Accidents

Report, to your field manager, all electrical accidents, possible electrical hazards, and accidents that nearly occurred. Remember, an accident that nearly occurs might be caused by a design problem; your immediate reporting ensures that the problem will be solved quickly.

Also report all small electrical shocks. Remember, a condition that causes a small shock need only differ slightly to cause serious injury.

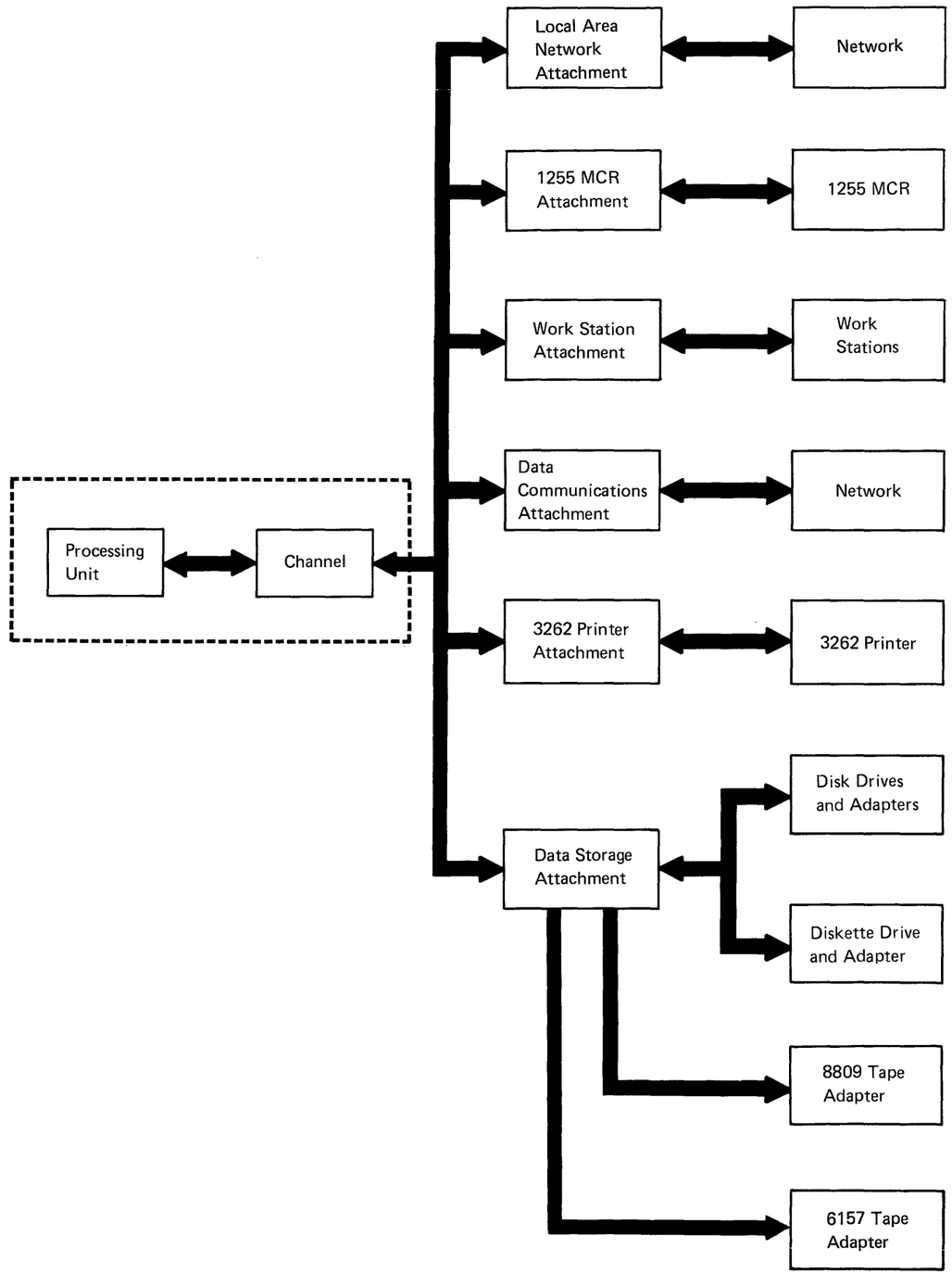
Contents

Overview

10-100
Introduction

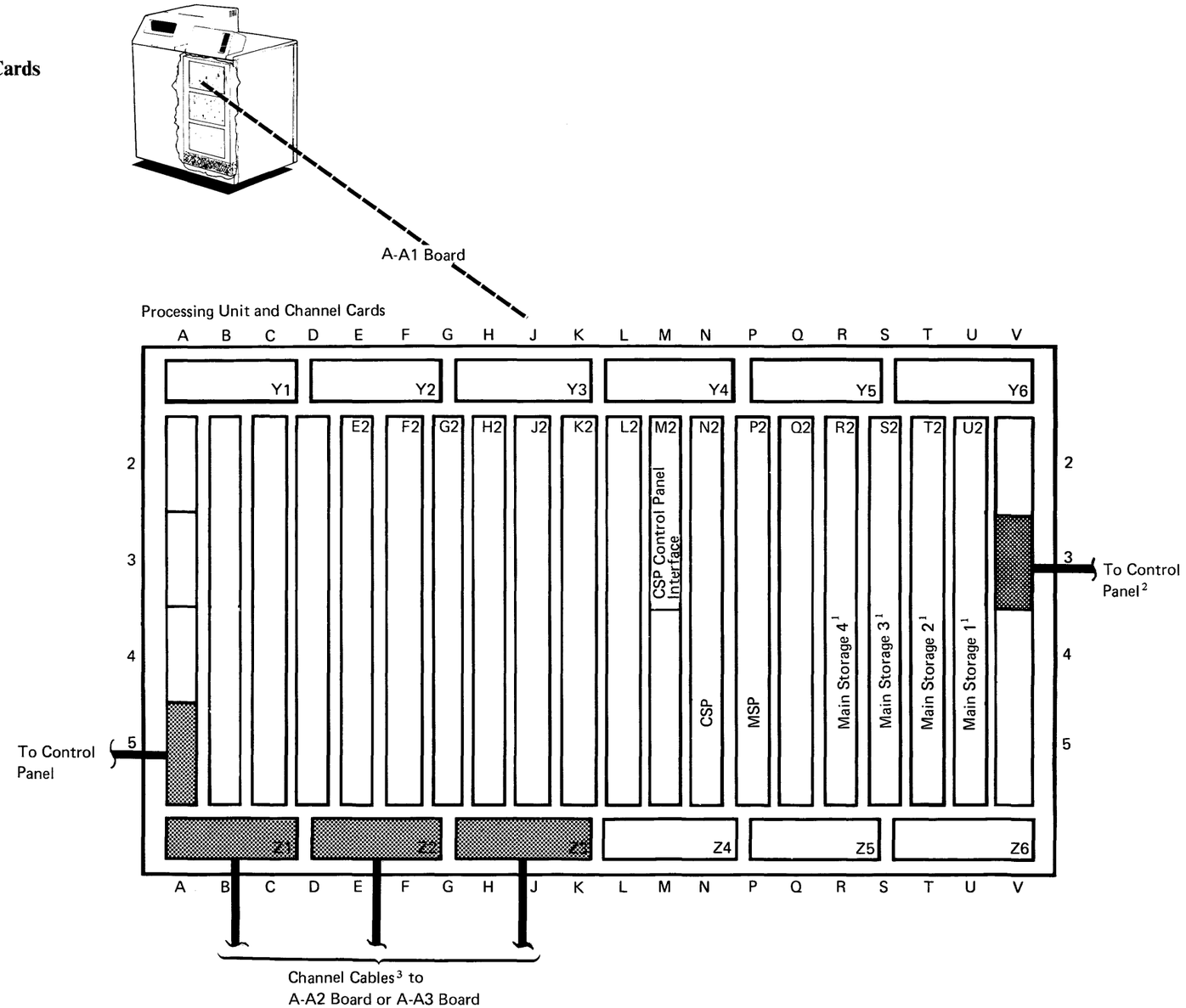
The IBM System/36 is made up of the following parts:

- Processing unit: The processing unit includes:
  - The main storage processor (MSP) for user programs
  - Main storage
  - The control storage processor (CSP) for system control
  - Control storage
  - The control panel
- Channel: The channel is the link between the processing unit and the I/O attachments. It supplies a data path and control circuits to transfer data between the I/O attachments and any part of the processing unit.
- Work station attachment: The work station attachment connects the channel to up to 72 work station devices (display stations or printers). The attachment supplies control circuits for data transfer between the devices and the channel.
- Data communications attachment: The data communications attachment can be a single-line communications attachment (SLCA), a multiline communications attachment (MLCA), or an eight-line communications attachment (ELCA). The SLCA connects one data communications line to the channel; the MLCA connects up to four data communications lines to the channel; the ELCA connects up to eight data communications lines to the channel. Each communications line can be controlled by either binary synchronous communication (BSC) or synchronous data link control (SDLC) line protocols.
- Data storage attachment: The data storage attachment connects the channel to the following:
  - Disk drive adapters, for storage of large blocks of data such as user programs, large data files, and the System Support Program Product (SSP).
  - A diskette drive adapter (or a diskette magazine drive adapter), for offline storage of data and to save and restore data from the system disk files.
  - A tape adapter, for offline storage of data and to save and restore data from the system disk files.
- Printer attachment: The printer attachment connects a system-controlled printer to the channel for printed output.
- 1255 MCR attachment: The 1255 magnetic character reader (MCR) attachment connects the channel to a 1255 MCR for input of data that is read from source documents.
- Local area network attachment: The local area network attachment connects the channel to an IBM PERSONAL COMPUTER AT®. The Personal Computer AT connects to the local area network.



Locations

10-200
Processing Unit Cards

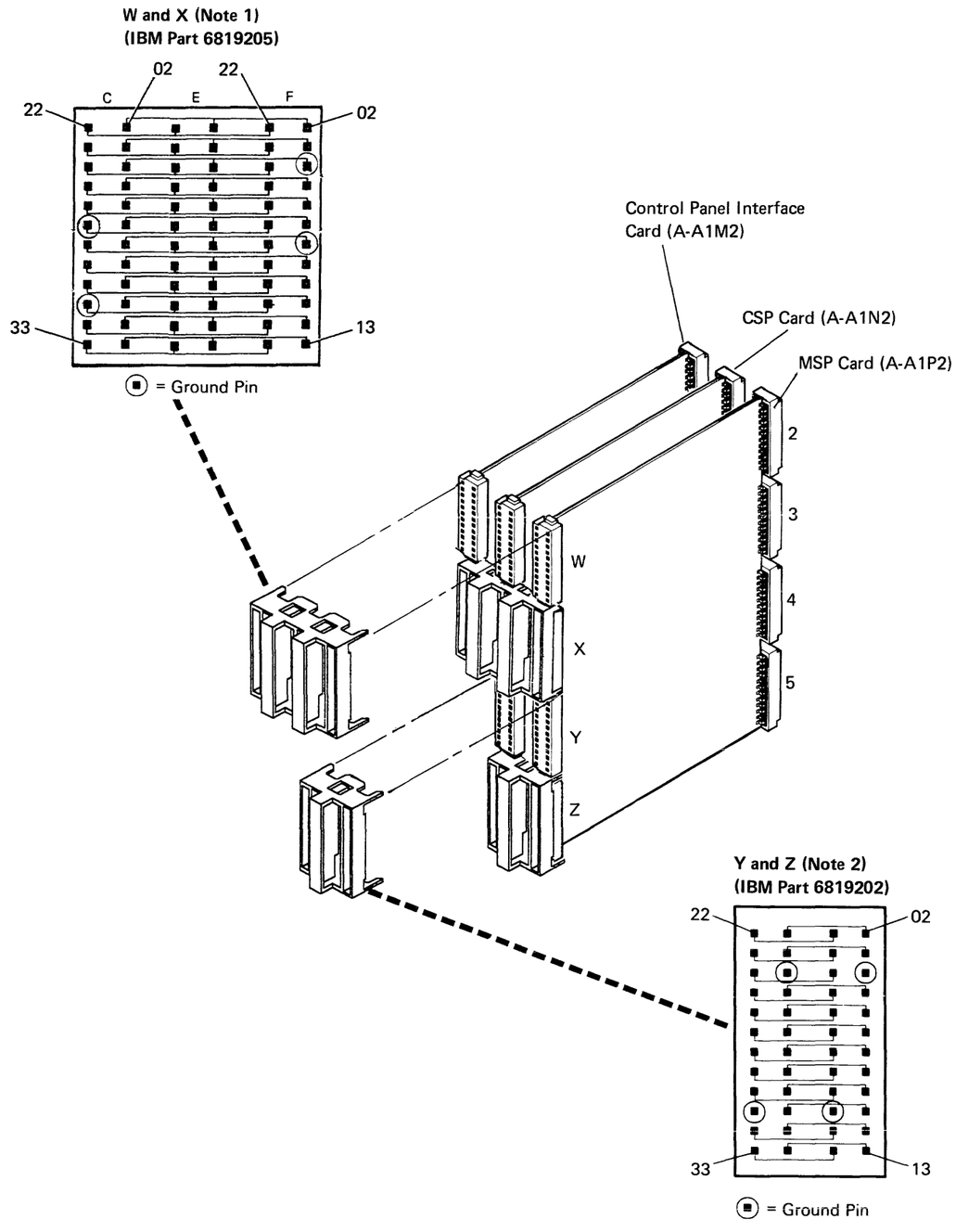


[1] If you add or remove any main storage cards, you must reconfigure main storage. A-A1U2 must contain a 1024K-byte main storage card.
[2] A-A1V3 contains this cable only if SLCA is installed.
[3] If the channel crossover cables are IBM part 2595676, they are installed on the pin side only. See the labels for correct installation.

10-205
Top Card Connectors

Notes:

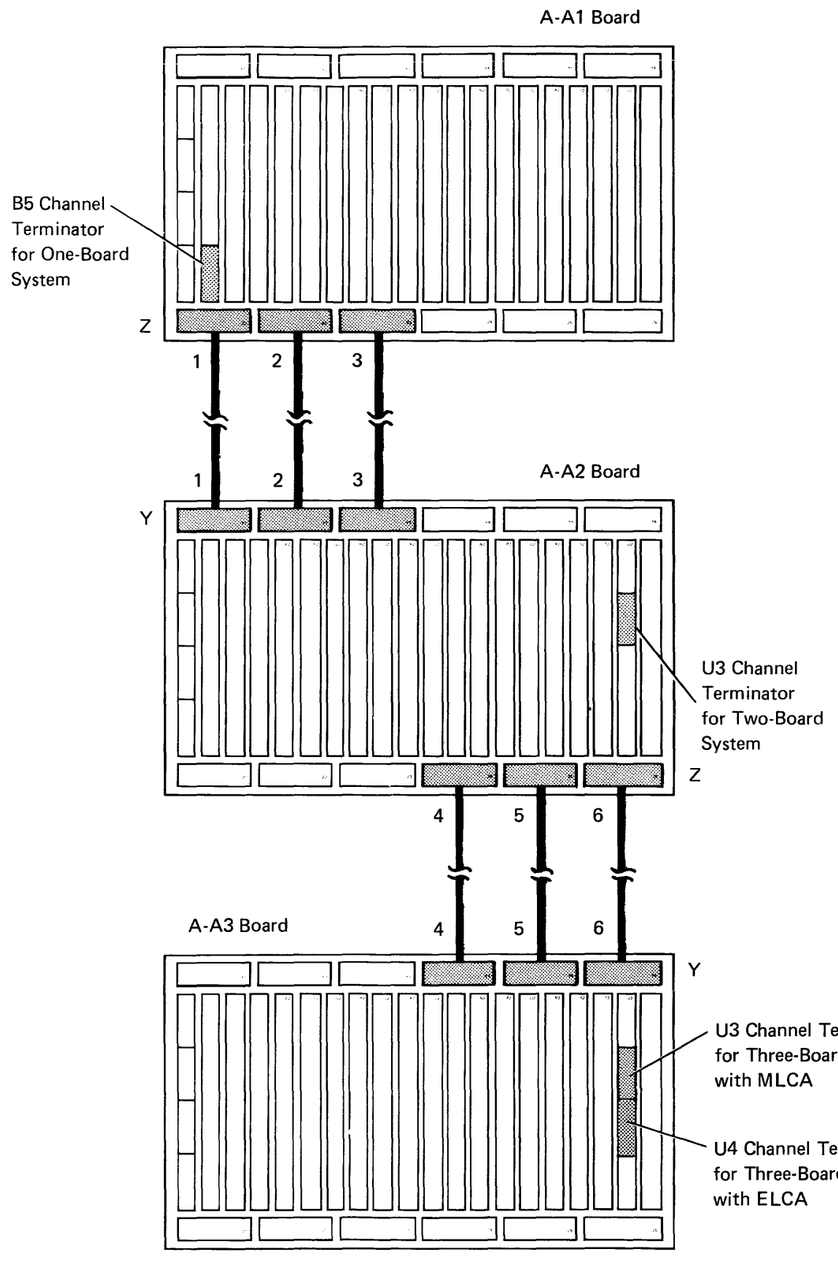
1. *Top card connectors W and X:*
   - *Have the same part number (IBM Part 6819205)*
   - *Can be swapped with each other, but not with the top card connectors Y and Z.*
   - *Can be installed only so that the housing of the top card connector matches the pin connectors of the cards.*
2. *Top card connectors Y and Z:*
   - *Have the same part number (IBM Part 6819202)*
   - *Can be swapped with each other, but not with the top card connectors W and X.*
   - *Can be installed only so that the housing of the top card connector matches the pin connectors of the cards.*



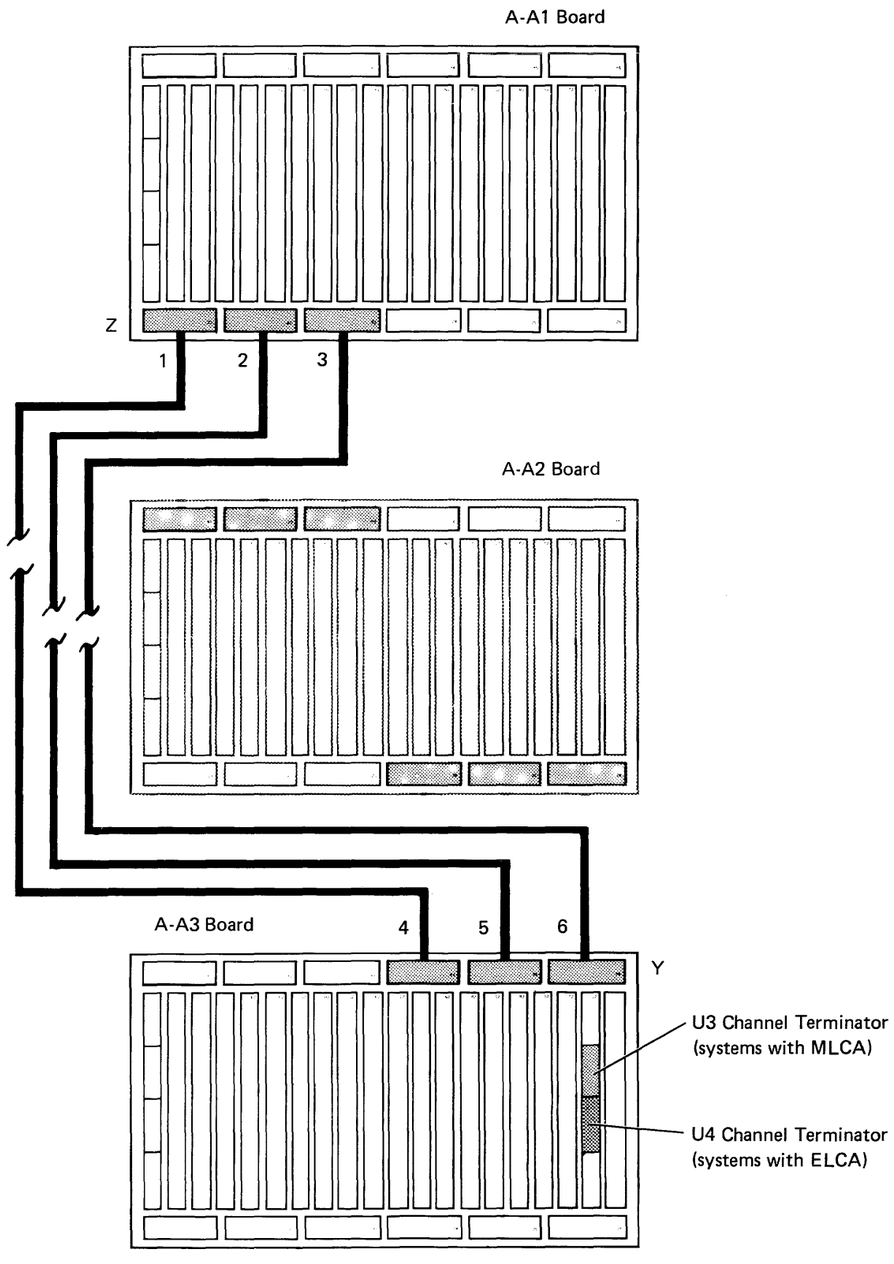
10-210
Channel Cables

One-Board Systems, or Two- or Three-Board Systems with A2 Board Installed

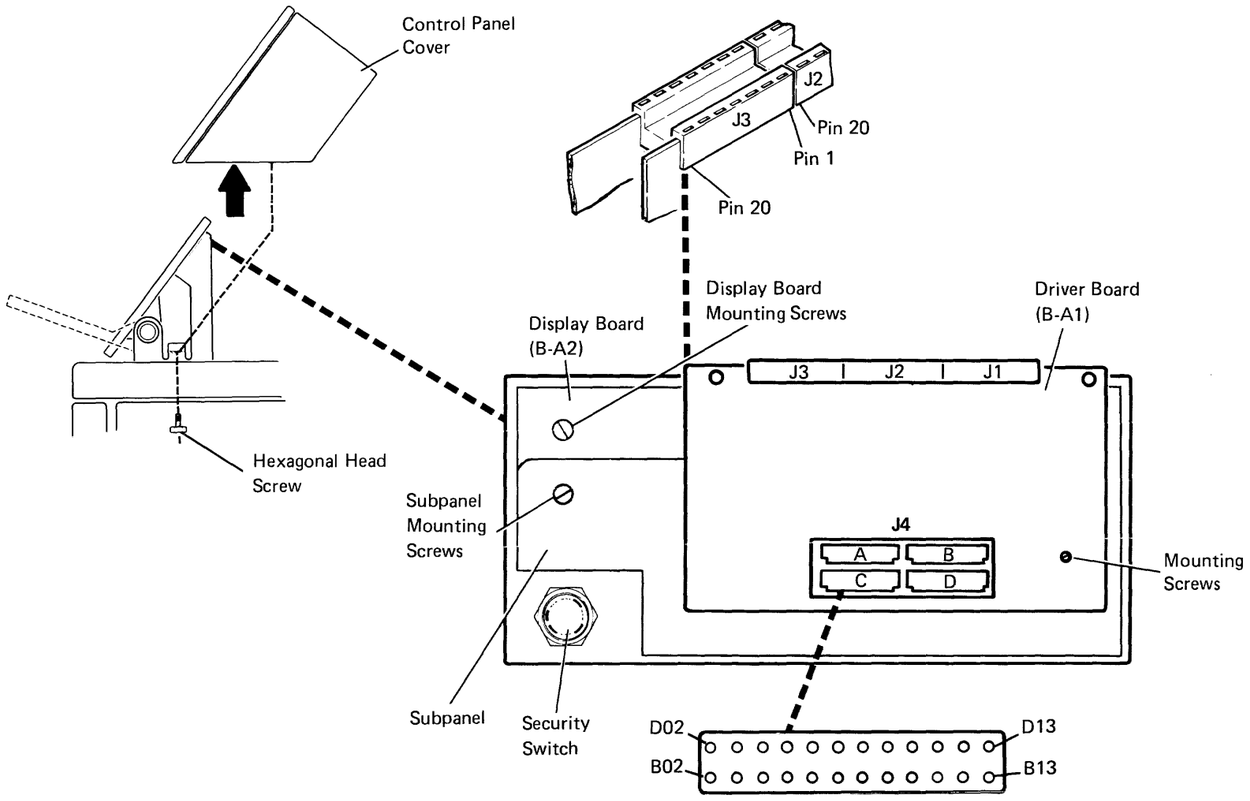
Note: *If the channel crossover cables are IBM part 2595676, they are installed on the pin side only. See the labels for correct installation.*

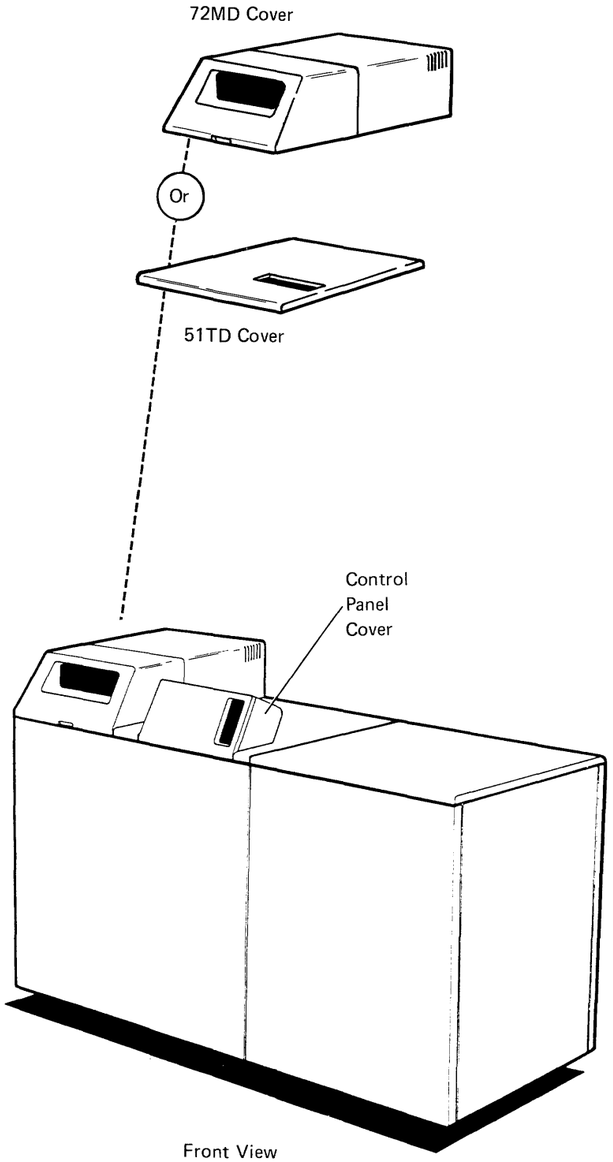


Two-Board Systems without A2 Board Installed

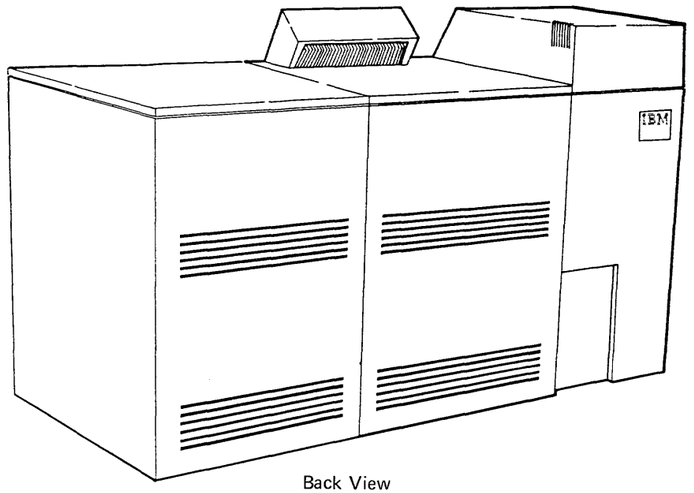


10-215
Control Panel FRUs

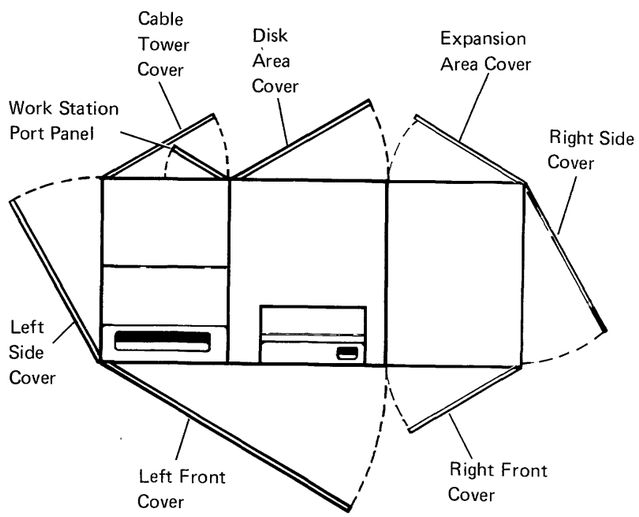




Front View



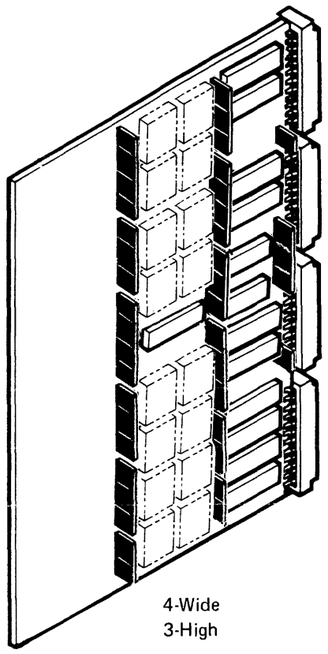
Back View



Top View

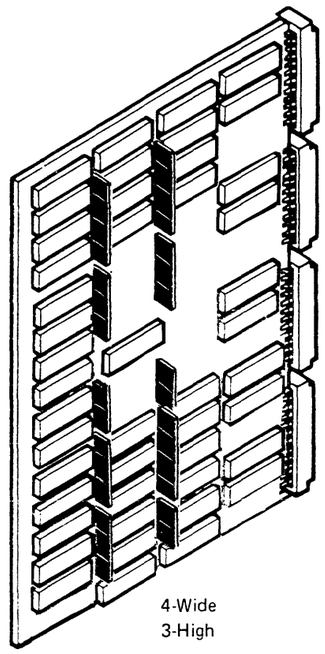
10-230
Main Storage Card Types

1024K Bytes with ECC



Used for Main Storage (A-A1U2, A-A1T2, A-A1S2, and A-A1R2)

2048K Bytes with ECC



Used for Main Storage (A-A1T2, A-A1S2, and A-A1R2)

Maintenance Procedures

SERVICE CHECKS AND REMOVAL PROCEDURES

10-320
Opening Covers

A latch inside each System/36 cover holds the cover closed. To open the cover:

1. Insert a spring hook (IBM part 154230 or a similar spring hook) into the access slot in the cover.

   DANGER
   You can injure your hand when opening or closing the logic gate.

   You can jam your hand between the top of the gate and the frame. Pull on the rear of the gate to open it, and push on the front of the gate to close it.

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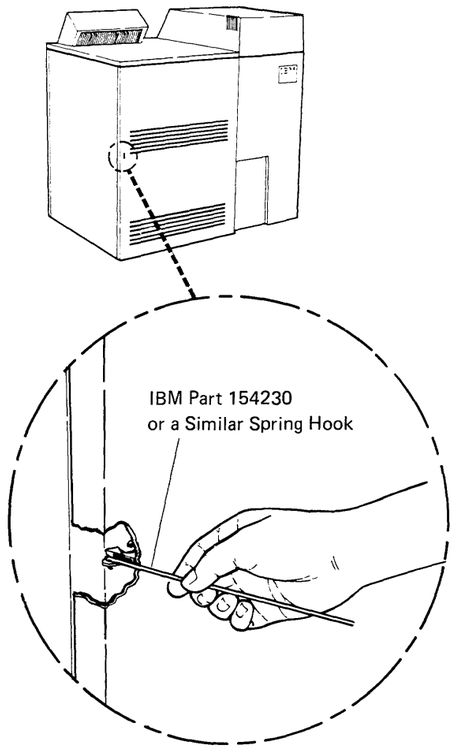

2. Pull out on the latch with the spring hook to open the cover.

10-325
Control Panel Removal

Perform the following steps to remove a control panel FRU:

1. Power off (01-115).
2. Set CB1 to off.
3. Disconnect the line cord.

DANGER
You can injure your hand when opening or closing the logic gate.

You can jam your hand between the top of the gate and the frame. Pull on the rear of the gate to open it, and push on the front of the gate to close it.

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4. Open the front cover and open the logic gate.
5. Locate and remove two control panel cover mounting screws (under the control panel).
6. Lift the cover off the control panel.
7. Tilt the control panel forward to access the rear of the panel.
8. Remove and label the cables from connectors J4-A, B, C, and D.

   Note: *In the following steps, keep the panel in a horizontal position to prevent losing small parts.*

9. Remove the driver board mounting screws and the driver board.

CAUTION
When you remove the two subpanel mounting screws that are behind the communications display, the communications display comes off.

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10. While supporting the communications display from the bottom of the panel, remove the subpanel mounting screws, the communications display, and the subpanel.

CAUTION
Panel switch keybuttons are pulled loose when you remove the display board. Be careful not to lose or damage them.

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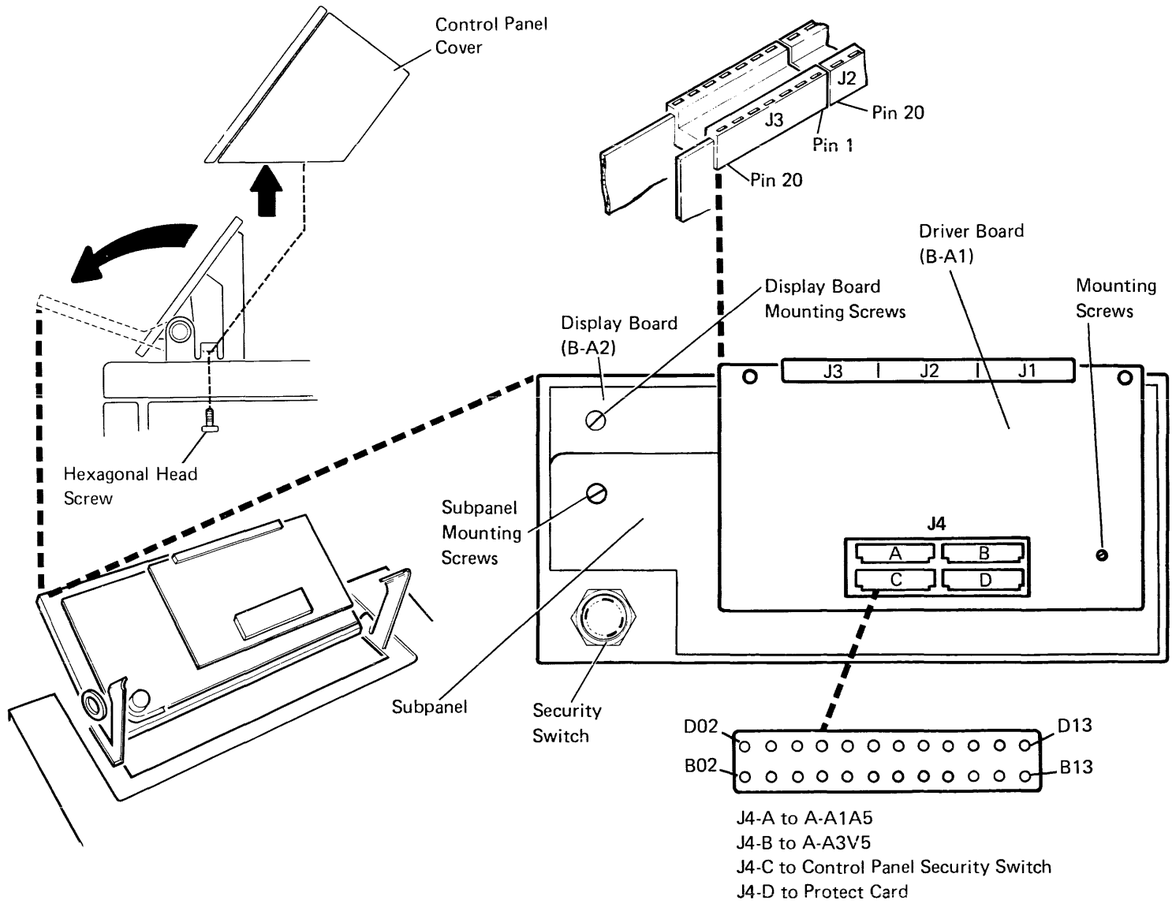
11. Remove the display board mounting screws and the display board.



12. Remove the rubber cover from the display board if it is still attached.

Perform the steps in reverse order to assemble. Top connectors must be on the display board before you reinstall the display board.

10-360
How to Identify a Failing Main Storage Card

If exchanging the card indicated by the system reference code (see MAP 0113, MAP 0114, MAP 0115, and MAP 0116) does not repair a main storage problem, use the following procedure to identify the failing main storage card:

1. Check the MSP error history table (10-550) to determine if any of the following bits of status byte 4 (10-558) are on:

Bit(s)	Description
4	Single-bit storage error
5	Multiple-bit storage error

2. If any of the bits in step 1 are on, use the entry labeled "Fail 2K" in the MSP error history table (10-550) to determine the Fail 2K Value. Find this Fail 2K Value in the first column of the table below. Then, read across to the failing card in the column that matches the largest main storage card installed on the system. See 10-230 to determine card types.

	Main Storage Card Types	
	Only 1024 Kb Cards	**Largest Card is 2048 Kb**
Fail 2K Value	**Failing Card**	**Failing Card**
0000 to 01FF	A-A1U2	A-A1U2
0200 to 03FF	A-A1T2	A-A1T2
0400 to 05FF	A-A1S2	A-A1S2
0600 to 07FF	A-A1R2	A-A1R2
0800 to 09FF	–	A-A1U2
0A00 to 0BFF	–	A-A1T2
0C00 to 0DFF	–	A-A1S2
0E00 to 0FFF	–	A-A1R2

DIAGNOSTIC INFORMATION

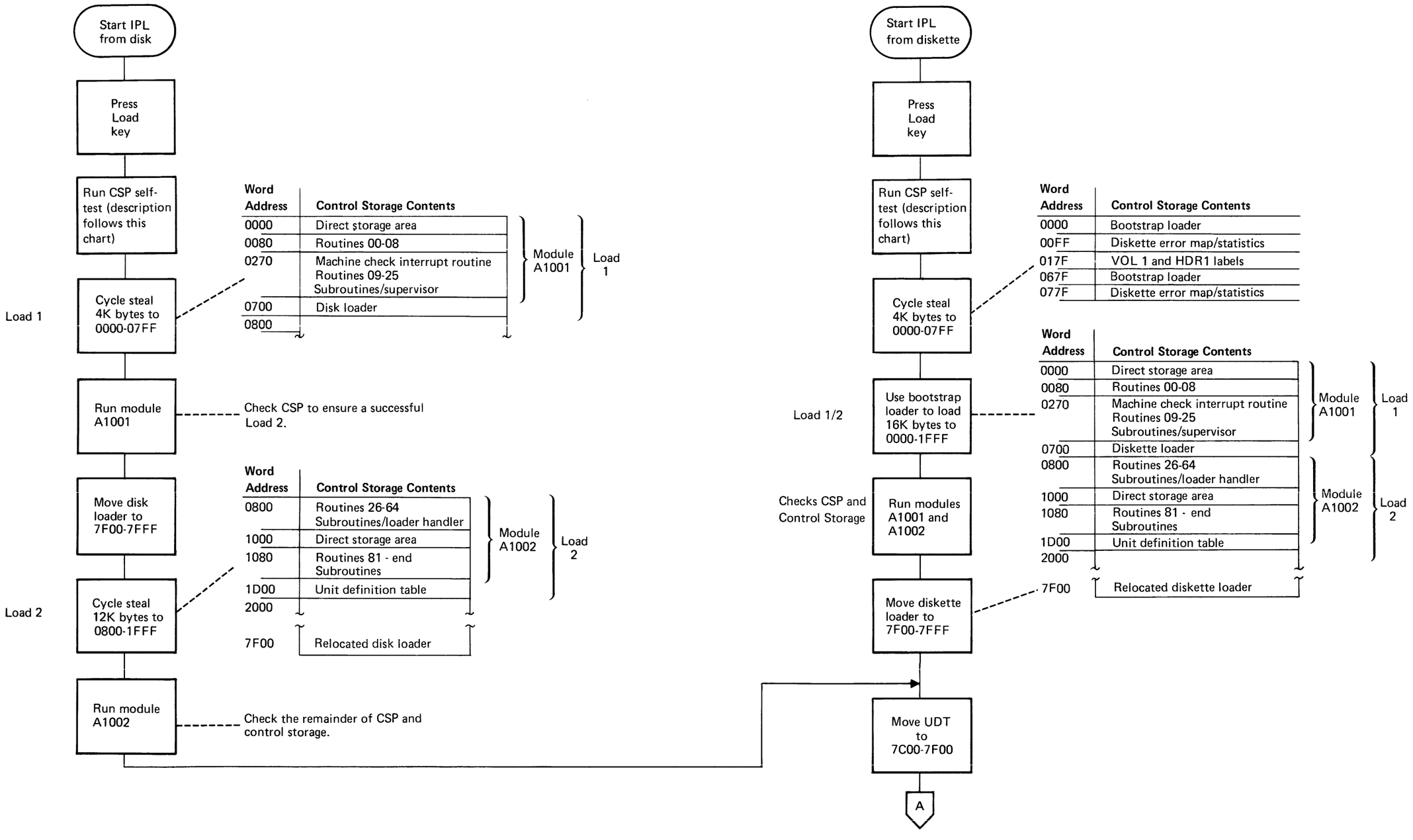
10-400
IPL Good Machine Path

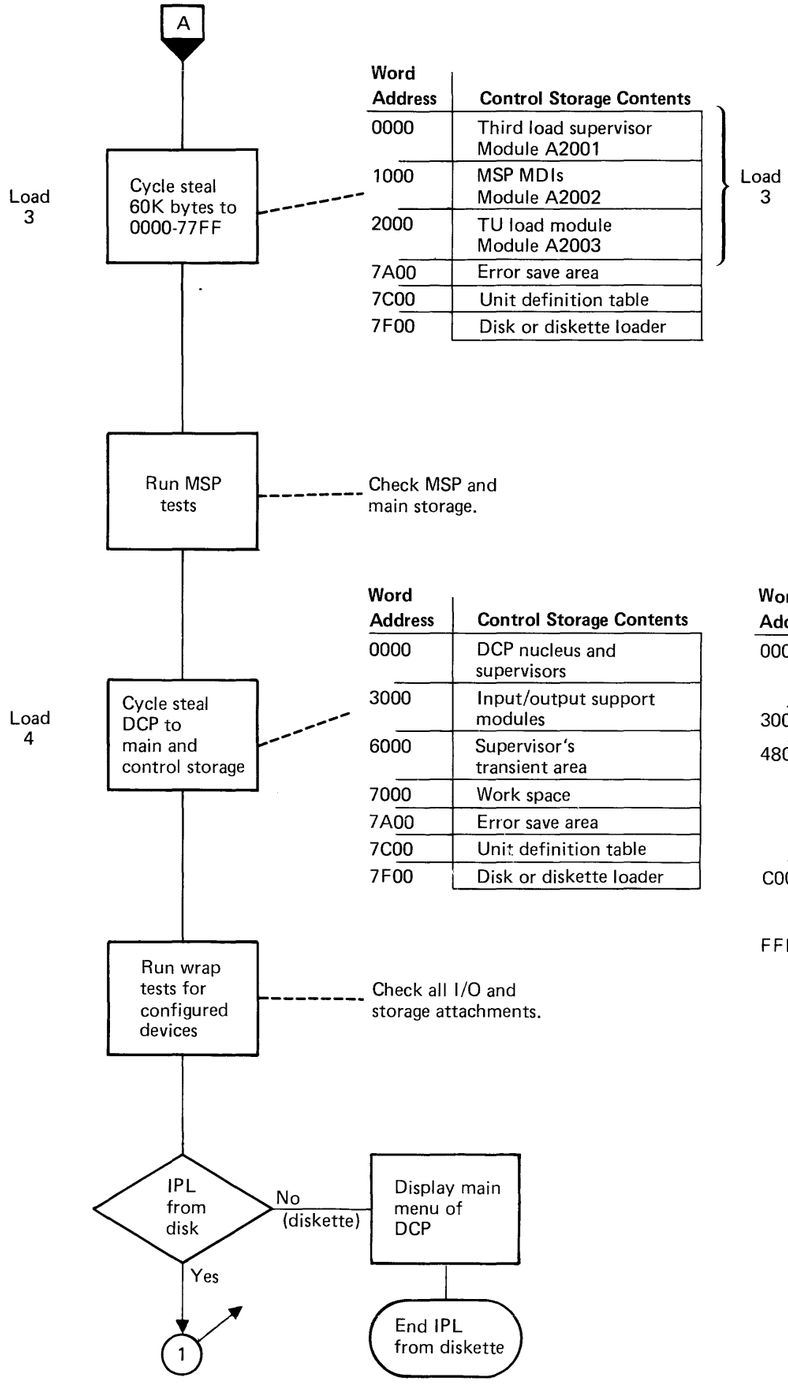
When the Load key on the control panel is pressed (01-140), the system automatically runs diagnostic tests that check the operation of the CSP and control storage, the channel, the MSP and main storage, and wrap tests with all configured I/O devices. When these tests complete without error, the System Support Program Product (SSP) can be loaded.

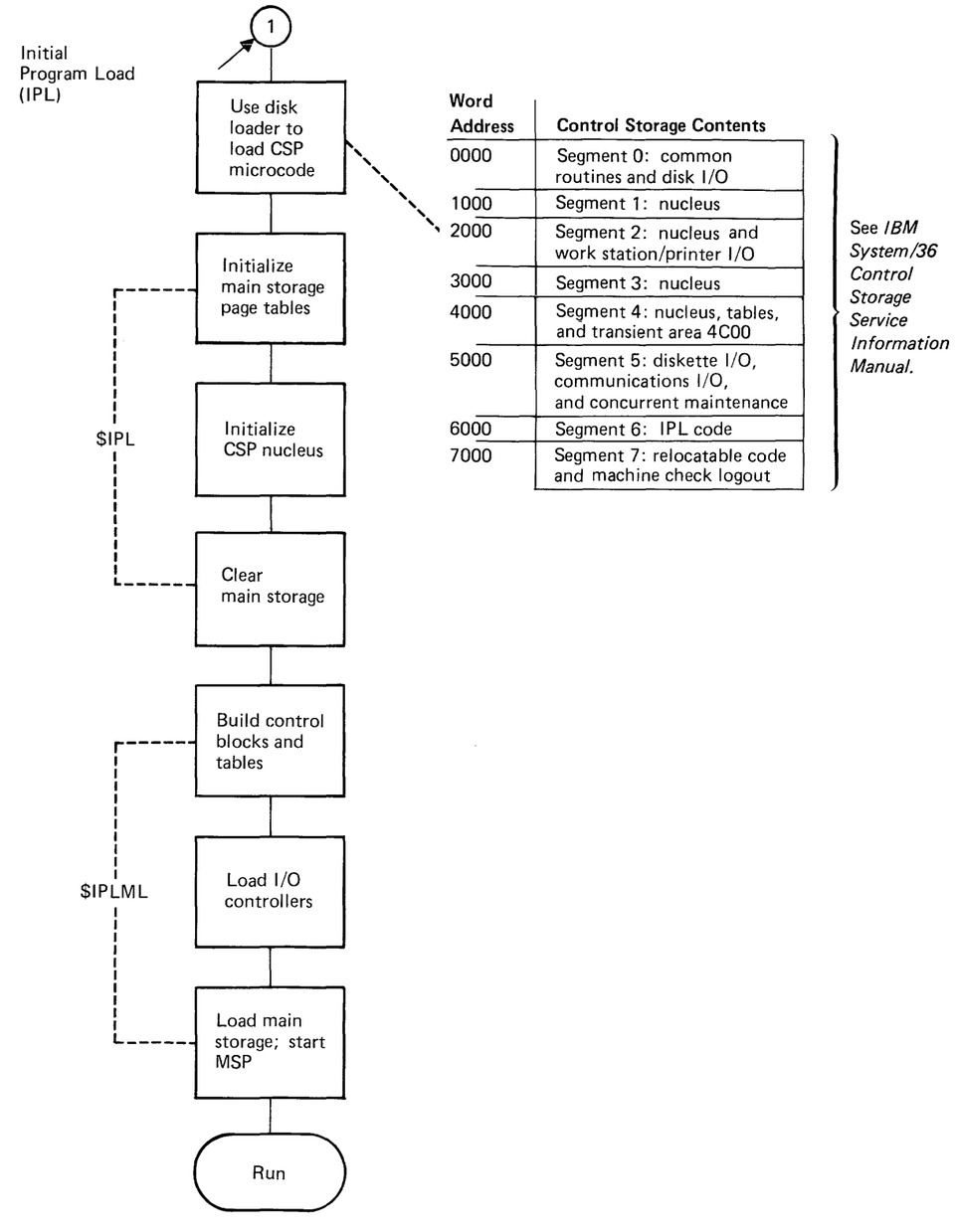
The IPL diagnostics are stored on the load device (either disk or diskette). The load process is different for each device, as shown in the following charts. However, in each case, the IPL diagnostics run as follows:

- CSP Self-Test: Basic check of CSP and control storage, and partial check of channel
- Load 1: Initial check of CSP, control storage, and channel
- Load 2: Complete check of CSP, control storage, and channel
- Load 3: Complete check of MSP and main storage
- Load 4: I/O wrap tests

10-400 (continued)
IPL Good Machine Path




A
Load 3
Cycle steal 60K bytes to 0000-77FF
Word Address
Control Storage Contents
0000
Third load supervisor Module A2001
1000
MSP MDIs Module A2002
2000
TU load module Module A2003
7A00
Error save area
7C00
Unit definition table
7F00
Disk or diskette loader
Load 3
Run MSP tests
Check MSP and main storage.
Load 4
Cycle steal DCP to main and control storage
Word Address
Control Storage Contents
0000
DCP nucleus and supervisors
3000
Input/output support modules
6000
Supervisor's transient area
7000
Work space
7A00
Error save area
7C00
Unit definition table
7F00
Disk or diskette loader
Word Address
Main Storage Contents
0000
DCP main storage nucleus
3000
Transient area
4800
Transient area or utility/exerciser program
C000
Utility/exerciser supervisor
FFFF
Run wrap tests for configured devices
Check all I/O and storage attachments.
IPL from disk
No (diskette)
Display main menu of DCP
End IPL from diskette
Yes
1


Initial Program Load (IPL)
1
Use disk loader to load CSP microcode
Word Address
Control Storage Contents
0000
Segment 0: common routines and disk I/O
1000
Segment 1: nucleus
2000
Segment 2: nucleus and work station/printer I/O
3000
Segment 3: nucleus
4000
Segment 4: nucleus, tables, and transient area 4C00
5000
Segment 5: diskette I/O, communications I/O, and concurrent maintenance
6000
Segment 6: IPL code
7000
Segment 7: relocatable code and machine check logout
See IBM System/36 Control Storage Service Information Manual.
Initialize main storage page tables
$IPL
Initialize CSP nucleus
Clear main storage
Build control blocks and tables
$IPLML
Load I/O controllers
Load main storage; start MSP
Run

10-400 (continued)
IPL Good Machine Path

CSP Self-Test

The CSP self-test consists of modules 0 through 21. These modules check the basic operation of the CSP and control storage and perform a partial check of the channel. The modules are loaded from the control panel interface card to control storage when the Load key is pressed. CSP self-test modules do not use result bytes. If an error occurs, the system reference code (SRC) appears on the control panel display. The CSP self-test modules run in the following sequence.

Self-Test Module	Description	System Reference Code
0	Initialize the machine check MAB to E880.	FFFF
1	Test unconditional branching.	E880
2	Test conditional branch by setting the PCR.	E881
3	Test the subroutine linkage.	E882
4	Test the test mask instruction.	E883
5	Test for the correct selection of bytes in work registers.	E884
6	Test the compare immediate instruction.	E885
7	Test the subtract immediate instruction.	E886
8	Test all 1-byte logical instructions.	E887
9	Test all 1-byte arithmetic instructions.	E888
10	Test all 2-byte logical instructions.	E889
11	Test all 2-byte, and 2-byte with 1-byte, arithmetic instructions.	E88A
12	Test all hexadecimal branch instructions.	E88C
13	Test all hexadecimal move instructions.	E88E
14	Initialize the low 32K words of control storage.	E88F
15	Test storage data and ECC check bits.	E890 E893
16	Test base + displacement instructions.	E894
17	Test full-word and half-word load and store instructions. Test load from a direct area.	E895 E896 E897
18	Test the following: 1. Channel register 2. Channel DBO and DBI bus 3. Set machine check level 4. Sensing a not valid device address 5. Sensing a CPC bus parity check 6. Sensing a parity check in OUT1 gate 7. Sensing a channel check 8. Sensing a parity check in OUT2 gate 9. Channel bits 10. LSR exception check	 E898 E899 E89C E89F E8A0 E8A2 E8A6 E8A8 E8AA E8AD
19	Test the following: 1. Enable interrupts 2. Interrupt level 5	 E8AE E8AF
20	Test the following: 1. Enable and disable interrupts using the 8-millisecond timer 2. Interrupt levels 1 through 4 using the 8-millisecond timer	 E8B0 E8B1
21	Test load and sense of the run control byte.	E8B2
	Update SRC on exit from the self-test.	E8B3

Load 1 Diagnostic Routines

Load 1 consists of diagnostic routines 00 through 25, the needed supervisor functions for running the routines, and a loader. The routines check the basic operation of the CSP and control storage to ensure that the remaining tests can be loaded. Load 1 routines do not use result bytes. If an error occurs, the system reference code (SRC) appears on the control panel display. Load 1 routines run in the following sequence.

Routine	Description	System Reference Code
00	Test unconditional branching to some addresses.	E900
01	Test conditional branching. The CSP must have been reset when the Load key was pressed.	
02	Test conditional branching by setting the condition register. This routine uses the SBN, SBF, and load PCR instructions.	
03	Test the test mask instruction. This routine uses SBN, SBF, and branch on condition (BOC) instructions to test mask the low byte of work register 1.	
04	Test the test mask instruction. This routine uses SBN, SBF, and BOC instructions to test mask the high byte of work register 1.	
05	Test the load immediate instruction. This routine uses the TM and conditional branch instructions.	
06	Test the compare immediate instruction. This routine uses the LI and conditional branch instructions.	
07	Test the branch and link instruction and the return instruction. This routine uses the LI, CI, MVR, and conditional branch instructions.	
08	Test the sense input register instruction. This routine performs the sense and checks that no error occurs.	
09	Test the subtract 1 from a register instruction (1 byte minus 1). This routine uses the LI, CI, and BOC instructions.	E909
10	Test the add 1 to a register instruction (1 byte plus 1). This routine uses the LI, CI, and BOC instructions.	E910
11	Test the subtract 1 from a register instruction (2 bytes minus 1). This routine uses the LI, CI, and BOC instructions.	E911
12	Test the add registers instruction (2 bytes plus 1 byte). This routine uses the LI, CI, branch on condition, and MPLF reset carry instructions.	E912
13	Test the add registers instruction (2 bytes plus 2 bytes). This routine uses the LI, CI, branch on condition, and MPLF reset carry instructions.	E913
14	Test the subtract registers instruction (2 bytes minus 2 bytes). This routine uses the LI, CI, branch on condition, and MPLF reset carry instructions.	E914
15	Test the load register from a direct area of control storage instruction. This routine uses the LI, CI, and BOC instructions and performs multiple tests of this instruction.	E915
16	Test the store register to a direct area of control storage instruction. This routine uses the LI, L, CI, and BOC instructions and performs multiple tests of this instruction.	E916
17	Test the load register from control storage instruction. This routine uses the LI, CI, and BOC instructions and performs multiple tests of this instruction.	E917
18	Test the store register to control storage instruction. This routine uses the LI, LC, CI, and BOC instructions and performs multiple tests of this instruction.	E918
19	Test the channel. This routine uses I/O immediate instructions to load and sense the channel register and compares the value sensed to the value loaded. The routine also senses the channel error byte and checks its value.	E919
20	Load and sense the processor condition register.	E920
21	Test the subtract immediate instruction.	E921
22	Test the add 1 to a register instruction (2 bytes plus 1). This routine uses the LI, CI, BOC, and reset carry/set equal instructions.	E922
23	Test the OR registers instruction (1 byte with 1 byte).	E923
24	Test the AND registers instruction (1 byte with 1 byte).	E924
25	Test the shift left logical instruction. This routine shifts left 1 bit of a selected byte in a register.	E925

10-400 (continued)
IPL Good Machine Path

Load 2 Diagnostic Routines

Load 2 consists of the remaining diagnostic routines for the CSP and control storage. The routines check the complete operation of the CSP and control storage. Load 2 routines do not use result bytes. If an error occurs, the system reference code (SRC) appears on the control panel display. Load 2 routines run in the following sequence.

Routine	Description	System Reference Code
–	Load module A1002.	E990
26	Test the exclusive OR registers instruction (1 byte with 1 byte).	EA26
27	Test the AND complement registers instruction (1 byte with 1 byte).	EA27
28	Test the OR complement registers instruction (1 byte with 1 byte).	EA28
29	Test the add registers instruction (1 byte plus 1 byte).	EA29
30	Test the subtract registers instruction (1 byte minus 1 byte).	EA30
31	Test the add registers with carry instruction (1 byte plus 1 byte).	EA31
32	Test the subtract registers with borrow instruction (1 byte minus 1 byte).	EA32
36	Test the exclusive OR registers instruction (2 bytes with 2 bytes).	EA36
37	Test the OR registers instruction (2 bytes with 2 bytes).	EA37
38	Test the AND registers instruction (2 bytes with 2 bytes).	EA38
39	Test the AND complement registers instruction (2 bytes with 2 bytes).	EA39
40	Test the OR complement registers instruction (2 bytes with 2 bytes).	EA40
41	Test the shift left logical double instruction. This routine shifts left 1 bit of both bytes in a register.	EA41
42	Test the subtract registers instruction (2 bytes minus 1 byte).	EA42
43	Test the subtract registers with borrow instruction (2 bytes minus 2 bytes).	EA43
44	Test the add registers with carry instruction (2 bytes plus 2 bytes).	EA44
45	Test the move zone instruction.	EA45
46	Test the hexadecimal branch instruction.	EA46
47	Test the shift right logical and the shift right logical double instructions.	EA47
48	Test the direct storage areas of control storage.	EA48
49	Test the move register instruction.	EA49
50	Test the zero and add registers instruction (1 byte with 1 byte).	EA50
51	Test the 'I/O service request' latch.	EA51
53	Sense the processor control byte and the processor error byte and test the 'flag' latch in the processor condition register.	EA53
55	Test the I/O clocks.	EA55
60	Force a storage data register parity check, an X-register parity check, and a microinstruction operation register parity check.	EA60
61	Force, detect, and reset the following: device address not valid check and system bus parity check.	EA61
63	Perform the control storage block tests.	EA63
64	Test all control storage locations.	EA64
81	Test the load high byte of a register from control storage instruction and the store high byte of a register to control storage instruction.	EA81
82	Test the add n to a register instruction (n = 1 through 16) (1 byte plus n and 2 bytes plus n)	EA82
83	Test the branch extended instruction.	EA83
84	Test the branch and link instruction.	EA84
85	Test the compare registers instruction (1 byte with 1 byte and 2 bytes with 2 bytes).	EA85
86	Test the subtract n from a register instruction (n = 1 through 16) (1 byte minus n and 2 bytes minus n).	EA86
88	Test the control storage base-plus-displacement instructions.	EA88
89	Test control storage ECC logic.	EA89
A1	Test the level 5 interrupt.	EAA1
A2	Test the fixed-interval timer at interrupt levels 1, 2, 3, and 4.	EAA2
–	Load MSP diagnostics.	EA90

Load 3 Diagnostic Routines

Load 3 diagnostic routines consist of test units (TUs) that test the complete operation of the MSP and main storage. The TUs run in the following sequence for a good machine path (if test option 0000 is selected). If errors occur, the test may branch to other tests not included here, or a system reference code (SRC) may appear on the control panel display (see MAP 0113, MAP 0114, MAP 0115, and MAP 0116). See 10-420 for a complete list of the MSP test units, a description of each TU, and the result bytes that each TU generates.

TU Sequence	Area Tested
T20B1	Check test options
T20EE	PATR and MCR load/sense
T20DA	Task 0 ATR data
T20DB	Task 0 ATR parity check
T20E2	Load and store configuration control register (CCR)
T20EF	Address compare register 2
T20F0	Address compare register 1
T20F1	Address compare register 0
T20E5	MSP register load/sense
T20F2	CSP read/write MSP register immediate instructions
T20E4	LSR addressing
T20E3	Reset MSP, sense status bytes, PSR, OP register, Q-register
T207F	Sense main storage and load MCR
T2082	Sense bad main storage bits
T20F5	Auto configure
T20E6	CCR and storage-not-valid check
T20E8	Storage exception generation
T20E9	Single storage cell
T20EA	Single storage cell addressing
T20EB	Single storage cell addressing
T20E0	Main storage refresh
T20B5	Analyze results of main storage tests
T20EC	Main storage real and translated addressing
T20ED	Main storage real and translated addressing
T20E1	2-byte and base-plus-displacement main storage accesses
T20DF	Reset interrupt level 5
T20E7	Address translation registers
T20DE	ATR main storage access
T20DD	Main storage card ECC logic test

TU Sequence	Area Tested
T20B6	Supervisor call instruction using PACT, ATR task group 0, and ATR task group 1
T20BB	Load register instruction
T20B7	Branch on condition instruction
T20BC	Store register instruction
T20C5	Load address instruction
T20B8	Jump on condition instruction
T20B9	Jump backward instruction
T20C6	Compare logical characters instruction
T20BA	Load program mode register instruction
T20BF	Branch on ARR instruction
T20BD	Compare logical immediate instruction
T20BE	Move immediate instruction
T20C2	Add to register instruction
T20CE	Add logical characters instruction
T20C0	Set bits on, set bits off instructions
T20C1	Test bits on, test bits off instructions
T20C3	Subtract from register instruction
T20C4	Subtract logical immediate instruction
T20C7	Zero and add zoned decimal instruction
T20C8	Add zoned decimal instruction
T20C9	Subtract zoned decimal instruction
T20CA	Move hexadecimal character instruction
T20CB	Edit instruction
T20CC	Insert and test characters instruction
T20CD	Move characters instruction
T20CF	Subtract logical characters instruction

TU Sequence	Area Tested
T20D2	Shift right character instruction
T20D4	Many instructions, using both PACT and ATR address translation modes
T20D0	MSP temporary suspend
T20D6	MSP instruction step
T20D1	X-register parity check
T20D5	MSP soft stop
T20D7	Address compare stop
T20F3	Force storage exception on not valid address
T20F4	Fast task load function
T20D9	Fast task save
T20DC	Storage extend cycle
T20D8	Not valid operation code
T20B1	Check for normal IPL
T20B4	Set up MSP, using system UDT information

10-420
MSP Test Unit Descriptions

In addition to running as part of the IPL testing, the MSP test units (TUs) can be loaded and run separately to check an area of the MSP operation (01-450). For most I/O devices, descriptions of the tests and their result bytes appear on the system console when the test is selected. However, when MSP tests are run, the system console may not be working. For that reason, this section contains a short description of each test and its result bytes to aid in interpreting results from the tests. The tests appear in numeric order by their TU number (T20xx). Some tests included here are not run during the IPL good machine path.

Result byte 1 is in WR7 high; result byte 2 is in WR7 low. See 01-225 to display WR7. Unless indicated differently, a good machine generates a result byte value of 00.

T207F
Main Storage Size Determination and MCR Load

This TU senses each main storage card to determine the number and size of storage cards in the system. This TU then loads the memory configuration register (MCR) with the correct value.

Result Byte 1

Bit(s)	Description
0	There is no card in A-A2U2 or there is an empty location between cards.
1	A machine check interrupt occurred.
2-7	Not used.

Result Byte 2

Not used.

T2082
Sense and Replace Bad Main Storage Bit

This TU senses each main storage location and determines if a bad bit is present. If so, this TU replaces the bad bit with the redundant bit in the main storage logic.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The TU did not find a bad bit.
2	The TU failed.
3	The TU did not find a bad ECC bit.
4	The TU did not correct an ECC problem.
5	More than one ECC bit is bad.
6, 7	Not used.

Result Byte 2

Not used.

T20B1
TU Supervisor

This TU checks the action control word bit that records the test options.

Result Byte 1

Bit(s)	Description
0	Bypass the MSP tests was selected (mode E).
1	Bypass the MSP tests was selected (mode 0 or mode F).
2-7	Not used.

Result Byte 2

Not used.

T20B2
FF00 Initialization—Mode E

This TU sets the MSP control registers, the LSRs, and main storage to known values. The values are the results of storage accesses to main storage. Values are set for storage with ECC, and 128K bytes of storage are set to FF. The address translation registers are set as if there were no bad pages in main storage.

Result Byte 1

Bit(s)	Description
0	The TU could set main storage to FF.
1	The TU could not access MSP registers.
2-7	Not used.

Result Byte 2

Not used.

T20B3
FF00 Initialization—Mode 0 or Mode F

This TU sets the MSP control registers, the LSRs, and main storage to known values. The values are from the unit definition table (UDT). The address translation registers are set as if there were no bad pages in main storage.

Result Byte 1

Bit(s)	Description
0	The TU could not set main storage to FF.
1-7	Not used.

Result Byte 2

Not used.

T20B4
0000 Initialization

This TU sets the MSP control registers, the LSRs, and main storage to known values. The values are from the unit definition table (UDT). The address translation registers are set using the information in the bad page table area.

Result Byte 1

Bit(s)	Description
0	The TU could not set main storage to FF.
1-7	Not used.

Result Byte 2

Not used.

T20B5
Analysis of Main Storage Bad Page Table

This TU checks the bad page table to determine if there are enough good storage pages to continue with the tests. The TU uses the following rules:

- The number of bad pages cannot be more than a maximum value.
- There can be no bad pages if the FC03 test option was selected.
- The area from 0-16K bytes must have no bad pages.

Result Byte 1

Bit(s)	Description
0	The number of bad pages is more than the maximum number.
1	There are bad pages in the first 16K-byte area.
2	A machine check interrupt occurred.
3-7	Not used.

Result Byte 2

Not used.

T20B6
SVC Instruction and ATR Selection Test

This TU tests the SVC instruction. It performs SVC operations in aligned and non-aligned modes.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	No SVC occurred.
3	An MSP check occurred as indicated in SB4 and SB5.
4	A Q-code error occurred.
5-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20B7
Branch On Condition Instruction Test

This TU tests the branch on condition instruction for all valid Q-codes and with many PSR values.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20B8
Jump On Condition Instruction Test

This TU tests the jump on condition instruction for all valid Q-codes and with many PSR values.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20B9
Jump Backward Instruction Test

This TU tests the jump backward instruction.

Result Byte 1

Bit(s)	Description
0	The test results were not correct.
1	A machine check interrupt occurred.
2	Interrupt level 5 did not occur.
3	An error SVC was received.
4-7	Not used.

Result Byte 2

Not used.

T20BA
Load PMR Instruction Test

This TU tests the load PMR instruction for many valid Q-codes and with many PSR values.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	The results of the load PMR instruction were not correct.
3	No storage exception occurred at the end of the test.
4	An MSP check occurred as indicated in SB2.
5-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20BB
Load Register Instruction Test

This TU tests the load register instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20BC
Store Register Instruction Test

This TU tests the store register instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3-7	Not used.

Result Byte 2

Not used.

T20BD
Compare Logical Immediate Instruction Test

This TU tests the compare logical immediate instruction.

Result Byte 1

Bit(s)	Description
0	The test results were not correct.
1	A machine check interrupt occurred.
2	Interrupt level 5 did not occur.
3	An error SVC was received.
4-7	Not used.

Result Byte 2

Not used.

T20BE
Move Immediate Instruction Test

This TU tests the move immediate instruction.

Result Byte 1

Bit(s)	Description
0	The test results were not correct.
1	A machine check interrupt occurred.
2	Interrupt level 5 did not occur.
3	An error SVC was received.
4-7	Not used.

Result Byte 2

Not used.

T20BF
Branch on ARR Instruction Test

This TU tests the branch on ARR instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C0
Set Bits On/Off Instructions Test

This TU tests the set bits on and the set bits off instructions.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C1
Test Bits On/Off Instructions Test

This TU tests the test bits on and the test bits off instructions.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C2
Add to Register Instruction Test

This TU tests the add to register instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C3
Subtract from Register Instruction Test

This TU tests the subtract from register instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C4
Subtract Logical Immediate Instruction Test

This TU tests the subtract logical immediate instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C5
Load Address Instruction Test

This TU tests the load address instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C6
Compare Logical Characters Instruction Test

This TU tests the compare logical characters instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C7
Zero and Add Zoned Decimal Instruction Test

This TU tests the zero and add zoned decimal instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C8
Add Zoned Decimal Instruction Test

This TU tests the add zoned decimal instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20C9
Subtract Zoned Decimal Instruction Test

This TU tests the subtract zoned decimal instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20CA
Move Hexadecimal Character Instruction Test

This TU tests the move hexadecimal character instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20CB
Edit Instruction Test

This TU tests the edit instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20CC
Insert and Test Characters Instruction Test

This TU tests the insert and test characters instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20CD
Move Characters Instruction Test

This TU tests the move characters instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

10-420 (continued)
MSP Test Unit Descriptions

T20CE
Add Logical Characters Instruction Test

This TU tests the add logical characters instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20CF
Subtract Logical Characters Instruction Test

This TU tests the subtract logical characters instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20D0
MSP Temporary Suspend Test

This TU tests the ability of the MSP to run while the CSP reads and writes to main storage and reads from MSP registers. The TU runs a combination of MSP instructions, including storage accesses, while the CSP generates temporary suspends to the MSP.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Not used.

T20D1
X-Register Parity Check Test

This TU forces an X-register parity check to verify that the MSP can sense an X-register parity check.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	The checks were not stored in the CSP.
2	The checks were not stored in SB2.
3	The checks were not reset by SB6.
4	An error SVC was received.
5	A machine check interrupt occurred.
6	The check stored in SB4 is not correct.
7	The check stored in SB5 is not correct.

Result Byte 2

Not used.

T20D2
Shift Right Character Instruction Test

This TU tests the shift right character instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	An MSP check occurred as indicated in SB2.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20D4
Combined Mode Address Translation Test

This TU runs a combination of instructions and translated addressing modes.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	SB2, bit 6 is on.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if result byte 1, bit 3 is on. If bit 3 is off, result byte 2 is not used.

T20D5
MSP Soft Stop Test

This TU runs a set of instructions to test if a soft stop occurs when the instructions are performed under the specified conditions. The instructions and conditions tested are:

- A branch condition is met.
- A jump condition is met.
- A load address is performed to the IAR.
- A load register is performed to the IAR.
- An add register is performed to the IAR.
- A subtract register is performed to the IAR.

The test also includes instructions that do not cause a soft stop. At the end of the test, the CSP counts the number of soft stops that occurred and compares it with the number that was expected.

Result Byte 1

Bit(s)	Description
0	Too many soft stops occurred.
1	Too few soft stops occurred.
2	The test failed for other reasons, such as a machine check interrupt, a time-out, or an MSP error.
3-7	Not used.

Result Byte 2

If the test fails, result byte 2 contains the number of soft stops that occurred during the test.

T20D6
MSP Instruction Step Mode Test

This TU runs a combination of MSP instructions, including storage changes, with the MSP in instruction step mode. The test counts the number of instructions that are performed to verify that the MSP generates an interrupt level 5 request after each instruction.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	An MSP stop occurred that was not expected.
2	A machine check interrupt occurred.
3	The number of instructions that was counted is wrong.
4-7	Not used.

Result Byte 2

Not used.

T20D7
MSP Address Compare Stop Test

This TU runs a combination of MSP instructions and verifies that an address stop occurs for some values of the CCR. The test also verifies that the address compare stop function operates correctly during a CSP access of MSP registers or main storage.

Result Byte 1

Bit(s)	Description
0	An error occurred that was not expected.
1	The address comparison failed.
2-7	Not used.

Result Byte 2

When the address comparison fails (result byte 1 is set), result byte 2 contains the value in the CCR.

10-420 (continued)
MSP Test Unit Descriptions

T20D8
Not Valid Operation Code Test

This TU runs various instructions that result in one of three types of not valid operation codes.

Result Byte 1

Bit(s)	Description
0	The MSP stopped too many times.
1	The MSP stopped too few times.
2	The test failed for other reasons, such as interrupt level 5 did not occur, an MSP error occurred, or the not valid operation latch was not set.
3	Not used.
4	A machine check interrupt occurred.
5-7	Not used.

Result Byte 2

Result byte 2 contains the counter value of the number of interrupt level 5 requests if the test fails.

T20D9
Fast Task Save Test

This TU runs various sets of instructions that result in different ways to get a fast task save.

Result Byte 1

Bit(s)	Description
0	The register save data did not match the expected data.
1	Checks occurred that were not expected.
2	The test failed for other reasons, such as an error during interrupt level 5, a machine check interrupt, or a time-out.
3	The IAR value was not correct.
4-7	Not used.

Result Byte 2

Result byte 2 contains the counter value of the number of interrupt level 5 requests if the test fails.

T20DA
Task 0 ATR Data Test

This TU loads and senses test data in all of the task 0 ATRs. The test uses data patterns A7, 00, 55, AA, and FF.

Result Byte 1

Bit(s)	Description
0	The A7 test failed.
1-3	Not used.
4	The 00 test failed.
5	The 55 test failed.
6	The AA test failed.
7	The FF test failed.

Result Byte 2

If result byte 1, bit 0, 4, 5, 6, or 7 is on, result byte 2 contains the ATR address where the failure occurred.

T20DB
Task 0 ATR Parity Check Test

This TU tests the parity checking logic for the task 0 ATRs.

Result Byte 1

Bit(s)	Description
0	The test failed.
1	A machine check interrupt occurred.
2-5	Not used.
6	A CPC bus parity check did not occur.
7	A task 0 parity check did not occur.

Result Byte 2

Not used.

T20DC
Storage Extend Cycle Test

This TU sets the storage extend cycle bit. The test then runs various instructions and checks to ensure that the data is correct.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error SVC was received.
3	SB2, bit 6 is on.
4-7	Not used.

Result Byte 2

Result byte 2 holds the contents of SB4 if SB2, bit 6 is on. If SB2, bit 6 is off, result byte 2 is not used.

T20DD
Main Storage Card ECC Test

This TU tests the error checking and correcting logic on each main storage card. The test forces single-bit and multiple-bit errors.

Result Byte 1

For a good machine, result byte 1 contains a value of 01, 02, or 03.

Bit(s)	Description
0	The test did not correct the single-bit error.
1	The test did not sense the single-bit error.
2	The test did not sense the multiple-bit error.
3	The test sensed an error in the storage configuration data.
4	A machine check interrupt occurred.
5	Not used.
6	One or more of the main storage cards passed the test.
7	One or more of the main storage cards was not tested because of a single-bit error in the first 2K-byte page.

Result Byte 2

Bit(s)	Description
0-3	Not used.
4	Card A-A1R2 failed.
5	Card A-A1S2 failed.
6	Card A-A1T2 failed.
7	Card A-A1U2 failed.

T20DE
ATR Access of Main Storage

This TU performs accesses of main storage using all eight of the ATR banks.

Result Byte 1

Bit(s)	Description
0	Task group 0 failed.
1	I/O group 0 failed.
2	Task group 1 failed.
3	I/O group 1 failed.
4	I/O group 2 failed.
5	I/O group 3 failed.
6	I/O group 4 failed.
7	I/O group 5 failed.

Result Byte 2

Not used.

T20DF
Reset MSP Interrupt Level 5 Request Test

This TU verifies that the MSP can generate and reset an interrupt level 5 request to the CSP.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	SB1 did not reset interrupt level 5.
3-7	Not used.

Result Byte 2

Not used.

T20E0
Main Storage Refresh Test

This TU verifies that main storage is being refreshed. The test writes a data pattern into all configured storage, waits 2 seconds, and then reads all storage locations and compares the data read with the expected data. If a storage error occurs, the test writes the address of the 2K-byte page in the bad page table, and records the error type, the failing test ID, and the failing storage card.

Result Byte 1

Not used.

Result Byte 2

Not used.

T20E1
2-Byte Load and Store Main Storage Instruction Test

This TU verifies that the CSP load main storage byte (LM) and store main storage byte (STM) instructions operate correctly. The test uses both direct addressing and base-plus-displacement addressing methods.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	An MSP check occurred.
2	The test failed.
3-7	Not used.

Result Byte 2

Not used.

T20E2
Ripple CCR Test

This TU tests the configuration control register (CCR) by loading and sensing a changing bit pattern.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The data read did not match the data expected.
2-7	Not used.

Result Byte 2

Not used.

10-420 (continued)
MSP Test Unit Descriptions

T20E3
Sense Status Bytes, PSR, OP Register, and Q-Register Test

This TU resets the MSP and then verifies that the values in the status bytes, the program status register (PSR), the operation (OP) register, and the Q-register are correct.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	SB2 is not correct.
2	SB0 is not correct.
3	The PSR is not correct.
4	SB6 is not correct.
5	SB5 is not correct.
6	SB4 is not correct.
7	SB8 is not correct.

Result Byte 2

Bit(s)	Description
0	The OP register is not correct.
1	The Q-register is not correct.
2-7	Not used.

T20E4
MSP LSR Stack Test

This TU tests the ability of the MSP to address the LSR stack and to write and read data into the LSRs. The test uses data patterns A7, 00, and FF.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The data read did not match the data expected.
2-7	Not used.

Result Byte 2

If result byte 1, bit 1 is on, result byte 2 contains the address of the LSR where the data read did not match the data expected. If bit 1 is off, result byte 2 is not used.

T20E5
MSP Register Load/Sense Test

This TU loads and senses all MSP registers that can be loaded and sensed. The test uses data patterns A7, 55, and 00.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The A7 test failed.
2	The 55 test failed.
3	The 00 test failed.
4-7	Not used.

Result Byte 2

If result byte 1, bit 1, 2, or 3 is on, result byte 2 contains the address of the register where the test failed. If bits 1, 2, and 3 are off, result byte 2 is not used.

T20E6
Storage-Not-Valid Check Test

This TU sets the configuration control register (CCR) with the correct value for the system. The test then verifies that the system can access the correct areas in storage and that a storage check is generated if accesses are attempted outside the permitted area.

Result Byte 1

Bit(s)	Description
0	The test failed.
1-7	Not used.

Result Byte 2

Not used.

T20E7
ATR Stack Test

This TU tests the ability of the CSP to address the ATR stack and to write and read data into the ATRs.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The data read did not match the data expected.
2-7	Not used.

Result Byte 2

Not used.

T20E8
Storage Exception Test

This TU verifies that the storage exception check can be generated during a CSP address translation (using ATRs) storage access. The test uses SB6 to rest the checks that occur.

Result Byte 1

Bit(s)	Description
0	A storage exception did not occur during a write operation.
1	A storage exception did not occur during a read operation.
2	An error was not indicated the the CSP error byte.
3	The error indicated by SB4 is not the expected error.
4	The error indicated by SB2 is not the expected error.
5	SB2 was not reset by SB6.
6	SB4 was not reset by SB6.
7	Not used.

Result Byte 2

Not used.

T20E9
Main Storage Write and Read Test

This TU verifies that data can be written to and read from main storage. The test sets all configured storage locations to FF. It then writes a data pattern and reads it back to verify the operation of all storage locations from the lowest address to the highest address. The test uses data patterns FF, 00, 55, AA, FED1, and FFF4.

If a storage error occurs, the test writes the address of the 2K-byte page in the bad page table and records the error type, the failing test ID, and the failing storage card.

Result Byte 1

Not used.

Result Byte 2

Not used.

T20EA
Main Storage Addressing Test (Address + 1)

This TU verifies that the MSP can address all locations in main storage. The test sets all of main storage to FF. It then writes and reads alternate locations starting at the lowest address through the highest address. The test uses data patterns 00 and 77.

If a storage error occurs, the test writes the address of the 2K-byte page in the bad page table and records the error type, the failing test ID, and the failing storage card.

Result Byte 1

Not used.

Result Byte 2

Not used.

T20EB
Main Storage Addressing Test (Address - 1)

This TU verifies that the MSP can address all locations in main storage. The test sets all of main storage to FF. It then writes and reads alternate locations starting at the highest address through the lowest address. The test uses data patterns 00 and 77.

If a storage error occurs, the test writes the address of the 2K-byte page in the bad page table and records the error type, the failing test ID, and the failing storage card.

Result Byte 1

Not used.

Result Byte 2

Not used.

T20EC
2K-Byte Addressing Test
(Address + 2K)

This TU verifies that the PCSP register (a PACT register) is being used to access main storage. The test sets the first location of each 2K-byte page to a value of FF. It then writes a new pattern in the first location of the lowest page and reads the first location of the next page. The test continues in this way through all pages in main storage (except those pages that are recorded in the bad page table) from the lowest to the highest address. The test uses data patterns 55 and AA.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The data read did not match the data expected.
2-7	Not used.

Result Byte 2

Not used.

T20ED
2K-Byte Addressing Test
(Address - 2K)

This TU verifies that the PCSP register (a PACT register) is being used to access main storage. The test sets the last location of each 2K-byte page to a value of FF. It then writes a new pattern in the last location of the highest page and reads the last location of the next lower page. The test continues in this way through all pages in main storage (except those pages that are recorded in the bad page table) from the highest to the lowest address. The test uses data patterns 55 and AA.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The data read did not match the data expected.
2-7	Not used.

Result Byte 2

Not used.

10-420 (continued)
MSP Test Unit Descriptions

T20EE
PATR and MCR Load/Sense Test

This TU loads and senses the PATR and the MCR. The test uses data patterns A7, FF, AA, 55, and 00.

Result Byte 1

Bit(s)	Description
0	The A7 test failed.
1	The FF test failed.
2	The AA test failed.
3	The 55 test failed.
4	The 00 test failed.
5, 6	Not used.
7	A machine check interrupt occurred.

Result Byte 2

If result byte 1, bit 0, 1, 2, 3, or 4 is on, result byte 2 contains the address of the register where the test failed. If bits 0, 1, 2, 3, and 4 are off, result byte 2 is not used.

T20EF
ACR 2 Test

This TU ensures that address compare register 2 (ACR 2) can be loaded and sensed.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The value in ACR 2 is not correct.
2-7	Not used.

Result Byte 2

If an error was sensed in ACR 2 (result byte 1, bit 1 is on), then result byte 2 contains the data value that was being loaded and sensed when the error occurred. If no error was sensed, result byte 2 is not used.

T20F0
ACR 1 Test

This TU ensures that address compare register 1 (ACR 1) can be loaded and sensed.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The value in ACR 1 is not correct.
2-7	Not used.

Result Byte 2

If an error was sensed in ACR 1 (result byte 1, bit 1 is on), then result byte 2 contains the data value that was being loaded and sensed when the error occurred. If no error was sensed, result byte 2 is not used.

T20F1
ACR 0 Test

This TU ensures that address compare register 0 (ACR 0) can be loaded and sensed.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The value in ACR 0 is not correct.
2-7	Not used.

Result Byte 2

If an error was sensed in ACR 0 (result byte 1, bit 1 is on), then result byte 2 contains the data value that was being loaded and sensed when the error occurred. If no error was sensed, result byte 2 is not used.

T20F2
CSP Load and Sense PSR Test

This TU verifies that the CSP can correctly load and sense the PSR using the write MSP register immediate and read MSP register immediate instructions. The test uses the following patterns for the PSR:

- Load FF and sense 39.
- Load 00 and sense 02.
- Load 3C and sense 3C.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt occurred.
1	The FF/39 test failed.
2	The 00/02 test failed.
3	The 3C/3C test failed.
4-7	Not used.

Result Byte 2

Not used.

T20F3
Main Storage Exception Test–Address Not Valid

This TU verifies that a storage exception check occurs when the ATRs or PACT registers are loaded with an address that is more than 8 million bytes.

Result Byte 1

Bit(s)	Description
0	A machine check interrupt did not occur.
1	A machine check interrupt occurred but was not expected.
2	The MSP did not sense a storage exception condition.
3-7	Not used.

Result Byte 2

Not used.

T20F4
Fast Task Load Function Test

This TU tests the fast task load function.

Result Byte 1

Bit(s)	Description
0	Interrupt level 5 did not occur.
1	A machine check interrupt occurred.
2	An error occurred in one of the PACT registers.
3	An error occurred in one of the following registers: OP, Q, LCRR, PSR, or PMR.
4	An error occurred in one of the registers between index register 1 (XR1) and work register 7 (WR7).
5	The test did not end correctly.
6	The ATR value contains an error.
7	SB1, bit 6 was not reset.

Result Byte 2

Bit(s)	Description
0	The PSREG was not initialized correctly.
1	An error occurred while reading the high byte of the ATR.
2-7	Not used.

T20F5
Auto Configure Test

This TU determines the number and size of each main storage card installed. Then, the test updates the unit definition table.

Result Byte 1

Bit(s)	Description
0, 1	0,0 = A-A1R2 is empty. 0,1 = A-A1R2 is 1024 Kb. 1,0 = A-A1R2 is 2048 Kb.
2, 3	0,0 = A-A1S2 is empty. 0,1 = A-A1S2 is 1024 Kb. 1,0 = A-A1S2 is 2048 Kb.
4, 5	0,0 = A-A1T2 is empty. 0,1 = A-A1T2 is 1024 Kb. 1,0 = A-A1T2 is 2048 Kb.
6, 7	0,0 = A-A1U2 is empty. 0,1 = A-A1U2 is 1024 Kb. 1,0 = A-A1U2 is 2048 Kb.

Result Byte 2

Bit(s)	Description
0-2	Not used.
3	The test failed.
4-7	Number of cards configured; contains all zeros if the test is omitted.

T20F6
Main Storage Write Test

This TU writes to the first four addresses on each main storage card.

Result Byte 1

Bit(s)	Description
0	Not used.
1	Could not write to addresses 1 and 3.
2	Could not write to addresses 2 and 4.
3	Storage parity error on write.
4	Not used.
5	Sensed only FF from main storage bytes.
6	A multiple-bit storage error was indicated but the correct data was received.
7	Not used.

Result Byte 2

Bit(s)	Description
0-2	Not used.
3	All configured main storage cards failed.
4	Card A-A1R2 failed.
5	Card A-A1S2 failed.
6	Card A-A1T2 failed.
7	Card A-A1U2 failed.

10-420 (continued)
MSP Test Unit Descriptions

T20F7
Main Storage Write Test Increase Address

This TU writes to the first four addresses on each main storage card. The test performs a write, increases the address, and then performs a read. The test ignores checks.

Result Byte 1

Not used.

Result Byte 2

Bit(s)	Description
0-2	Not used.
3	All configured main storage cards failed.
4	Card A-A1R2 failed.
5	Card A-A1S2 failed.
6	Card A-A1T2 failed.
7	Card A-A1U2 failed.

T20F8
Main Storage Write Test Decrease Address

This TU writes to the first four addresses on each main storage card. The test performs a write, decreases the address, and then performs a read. The test ignores checks.

Result Byte 1

Not used.

Result Byte 2

Bit(s)	Description
0-2	Not used.
3	All configured main storage cards failed.
4	Card A-A1R2 failed.
5	Card A-A1S2 failed.
6	Card A-A1T2 failed.
7	Card A-A1U2 failed.

T20F9
Main Storage Test–Card Error Analysis

This TU formats the data collected in TUs T20E9, T20EA, T20EB, and T20E0 and displays the results in the result bytes.

Result Byte 1

For a good machine, result byte 1 contains a value of either 00 or 40.

Bit(s)	Description
0	Not used.
1	The system has more than one main storage card.
2	Not used.
3	A storage error occurred that had more than one bad bit (multiple-bit storage error).
4	Not used.
5	A data compare error and a multiple-bit storage error occurred.
6, 7	Not used.

Result Byte 2

Bit(s)	Description
0-2	Not used.
3	All configured main storage cards failed.
4	Card A-A1R2 failed.
5	Card A-A1S2 failed.
6	Card A-A1T2 failed.
7	Card A-A1U2 failed.

T20FA
Main Storage Test–Failing Test Analysis

This TU collects the TU IDs of the tests that failed during TUs T20E9, T20EA, T20EB, and T20E0 and displays the results by card in the result bytes.

Result Byte 1

Bit(s)	Description
0	T20E9 failed.
1	T20EA failed.
2	T20EB failed.
3	T20E0 failed.
4-7	Not used.

Result Byte 2

Bit(s)	Description
0-2	Not used.
3	All configured main storage cards failed.
4	Card A-A1R2 failed.
5	Card A-A1S2 failed.
6	Card A-A1T2 failed.
7	Card A-A1U2 failed.

T20FB
Main Storage Card Type Determination

This TU reads the unit definition table and determines the number of main storage cards installed.

Result Byte 1

Bit(s)	Description
0	Not used.
1-3	The number of main storage cards installed.
4, 5	Not used.
6	A-A1U2 is 2048 Kb.
7	A-A1U2 is 1024 Kb.

Result Byte 2

Bit(s)	Description
0, 1	Not used.
2	1 = 1024 Kb and 2048 Kb main storage cards are installed.
3-5	Not used.
6	Only 2048-Kb main storage cards are installed.
7	Only 1024-Kb main storage cards are installed.

T20FC
Main Storage Data Bit Fault Test

This TU checks the first 2K page in main storage to determine if one data bit is failing. This 2K page is written and read one address at a time starting at the lowest address. The test uses data patterns 55 and AA.

Result Byte 1

Bit(s)	Description
0	All bits failed.
1	One bit failed.
2	Half of the bits failed.
3	More than one bit failed.
4-7	Not used.

Result Byte 2

Not used.

T20FD
Main Storage Address Bit Fault Test

This TU determines which address bit is failing. Main storage is first initialized to FF. Then, at address 0000, the test writes data pattern 55. Next, the test reads address 0000 and compares the data read with the data written. The test continues through the highest address bit configured. This TU ignores checks.

Result Byte 1

Bit(s)	Description
0	Not used.
1	One address bit failed.
2-7	Not used.

Result Byte 2

Bit(s)	Description
0-7	Hexadecimal address of the failing address bit.

T20FE
Main Storage Card Type Determination

This TU reads the unit definition table and determines the card type in each main storage card location.

Result Byte 1

Bit(s)	Description
0, 1	Not used.
2	A-A1R2 is 2048 Kb.
3	A-A1R2 is 1024 Kb.
4, 5	Not used.
6	A-A1S2 is 2048 Kb.
7	A-A1S2 is 1024 Kb.

Result Byte 2

Bit(s)	Description
0, 1	Not used.
2	A-A1T2 is 2048 Kb.
3	A-A1T2 is 1024 Kb.
4, 5	Not used.
6	A-A1U2 is 2048 Kb.
7	A-A1U2 is 1024 Kb.

10-430
Identifying MSP Instructions in Hexadecimal Format

Use the following tables to interpret the hexadecimal format of MSP instructions. The op code determines the function of the instruction; it also determines the number of bytes of addressing and control information that are used before the next op code is found. See 01-246 or 01-248 to display main storage on the control panel. See 10-660 for a list of MSP instructions in alphabetic sequence by mnemonic.

MSP Instructions and Formats (Op Code Sequence)

Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	Byte 6	
Op Code	Q-Code		Operand Addresses				Instruction
04	L1	L2	Direct address of operand 1		Direct address of operand 2		Zero and add zoned decimal (ZAZ)
06	L1	L2					Add zoned decimal (AZ)
07	L1	L2					Subtract zoned decimal (SZ)
08	Select half byte						Move hex character (MVX)
0A	L1						Edit (ED)
0b							Insert and test characters (ITC)
0C	L3						Move characters (MVC)
0d							Compare logical characters (CLC)
0E							Add logical characters (ALC)
0F							Subtract logical characters (SLC)

Legend
L1 = Length-1 of operand 1 (in bytes)
L2 = Length-1 of operand 2 (in bytes)
L3 = Length-1 of both operands (in bytes)

Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	
Op Code	Q-Code		Operand Addresses			Instruction
14	L1	L2	Direct address of operand 1		Operand 2 displacement for indexing with XR1	Zero and add zoned decimal (ZAZ)
16	L1	L2				Add zoned decimal (AZ)
17	L1	L2				Subtract zoned decimal (SZ)
18	Select half byte					Move hex character (MVX)
1A	L1					Edit (ED)
1b						Insert and test characters (ITC)
1C	L3					Move characters (MVC)
1d						Compare logical characters (CLC)
1E						Add logical characters (ALC)
1F						Subtract logical characters (SLC)
24	L1	L2	Direct address of operand 1		Operand 2 displacement for indexing with XR2	Zero and add zoned decimal (ZAZ)
26	L1	L2				Add zoned decimal (AZ)
27	L1	L2				Subtract zoned decimal (SZ)
28	Select half byte					Move hex character (MVX)
2A	L1					Edit (ED)
2b						Insert and test characters (ITC)
2C	L3					Move characters (MVC)
2d						Compare logical characters (CLC)
2E						Add logical characters (ALC)
2F						Subtract logical characters (SLC)

Byte 1	Byte 2	Byte 3	Byte 4	
Op Code	**Q-Code**	**Operand Addresses**		**Instruction**
34	Register select	Direct address of operand		Store register (ST)
35				Load register (L)
36				Add to register (A)
37				Subtract from register (S)
38	Mask			Test bits on masked (TBN)
39				Test bits off masked (TBF)
3A				Set bits on masked (SBN)
3b				Set bits off masked (SBF)
3C	Immediate data			Move logical immediate (MVI)
3d				Compare logical immediate (CLI)
3E	SC L1			Shift right character (SRC)
3F	Immediate data			Subtract logical immediate (SLI)

Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	
Op Code	**Q-Code**		**Operand Addresses**			**Instruction**
44	L1	L2	Operand 1 displace-ment for indexing	Direct address of operand 2 with XR1		Zero and add zoned decimal (ZAZ)
46	L1	L2				Add zoned decimal (AZ)
47	L1	L2				Subtract zoned decimal (SZ)
48	Select half byte					Move hex character (MVX)
4A	L1					Edit (ED)
4b						Insert and test characters (ITC)
4C	L3					Move characters (MVC)
4d						Compare logical characters (CLC)
4E						Add logical characters (ALC)
4F						Subtract logical characters (SLC)

Byte 1	Byte 2		Byte 3	Byte 4	
Op Code	**Q-Code**		**Operand Addresses**		**Instruction**
54	L1	L2	Operand 1 displace-ment for indexing with XR1	Operand 2 displace-ment for indexing with XR1	Zero and add zoned decimal (ZAZ)
56	L1	L2			Add zoned decimal (AZ)
57	L1	L2			Subtract zoned decimal (SZ)
58	Select half byte				Move hex character (MVX)
5A	L1				Edit (ED)
5b					Insert and test characters (ITC)
5C	L3				Move characters (MVC)
5d					Compare logical characters (CLC)
5E					Add logical characters (ALC)
5F					Subtract logical characters (SLC)
64	L1	L2		Operand 2 displace-ment for indexing with XR2	Zero and add zoned decimal (ZAZ)
66	L1	L2			Add zoned decimal (AZ)
67	L1	L2			Subtract zoned decimal (SZ)
68	Select half byte				Move hex character (MVX)
6A	L1				Edit (ED)
6b					Insert and test characters (ITC)
6C	L3				Move characters (MVC)
6d					Compare logical characters (CLC)
6E					Add logical characters (ALC)
6F					Subtract logical characters (SLC)

Legend
L1 = Length-1 of operand 1 (in bytes)
L2 = Length-1 of operand 2 (in bytes)
L3 = Length-1 of both operands (in bytes)
SC = Shift count-1 (in bits)

10-430 (continued)
Identifying MSP Instructions in Hexadecimal Format

Byte 1	Byte 2	Byte 3	
Op Code	**Q-Code**	**Operand Address**	**Instruction**
74	Register select	Displacement for indexing with XR1	Store register (ST)
75			Load register (L)
76			Add to register (A)
77			Subtract from register (S)
78	Mask		Test bits on masked (TBN)
79			Test bits off masked (TBF)
7A			Set bits on masked (SBN)
7b			Set bits off masked (SBF)
7C	Immediate data		Move logical immediate (MVI)
7d			Compare logical immediate (CLI)
7E	SC L1		Shift right characters (SRC)
7F	Immediate data		Subtract logical immediate (SLI)

Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	
Op Code	**Q-Code**		**Operand Addresses**			**Instruction**
84	L1	L2	Operand 1 displacement for indexing	Direct address of operand 2 with XR2		Zero and add zoned decimal (ZAZ)
86	L1	L2				Add zoned decimal (AZ)
87	L1	L2				Subtract zoned decimal (SZ)
88	Select half byte					Move hex character (MVX)
8A	L1					Edit (ED)
8b						Insert and test characters (ITC)
8C	L3					Move characters (MVC)
8d						Compare logical characters (CLC)
8E						Add logical characters (ALC)
8F						Subtract logical characters (SLC)

Byte 1	Byte 2		Byte 3	Byte 4	
Op Code	**Q-Code**		**Operand Addresses**		**Instruction**
94	L1	L2	Operand 1 displacement for indexing with XR1	Operand 2 displacement for indexing with XR1	Zero and add zoned decimal (ZAZ)
96	L1	L2			Add zoned decimal (AZ)
97	L1	L2			Subtract zoned decimal (SZ)
98	Select half byte				Move hex character (MVX)
9A	L1				Edit (ED)
9b					Insert and test characters (ITC)
9C	L3				Move characters (MVC)
9d					Compare logical characters (CLC)
9E					Add logical characters (ALC)
9F					Subtract logical characters (SLC)
A4	L1	L2		Operand 2 displacement for indexing with XR2	Zero and add zoned decimal (ZAZ)
A6	L1	L2			Add zoned decimal (AZ)
A7	L1	L2			Subtract zoned decimal (SZ)
A8	Select half byte				Move hex character (MVX)
AA	L1				Edit (ED)
Ab					Insert and test characters (ITC)
AC	L3				Move characters (MVC)
Ad					Compare logical characters (CLC)
AE					Add logical characters (ALC)
AF					Subtract logical characters (SLC)

Legend
L1 = Length-1 of operand 1 (in bytes)
L2 = Length-1 of operand 2 (in bytes)
L3 = Length-1 of both operands (in bytes)
SC = Shift count-1 (in bits)

Byte 1	Byte 2	Byte 3	
Op Code	**Q-Code**	**Operand Address**	**Instruction**
b4	Register select	Displacement for indexing with XR2	Store register (ST)
b5			Load register (L)
b6			Add to register (A)
b7			Subtract from register (S)
b8	Mask		Test bits on masked (TBN)
b9			Test bits off masked (TBF)
bA			Set bits on masked (SBN)
bb			Set bits off masked (SBF)
bC	Immediate data		Move logical immediate (MVI)
bd			Compare logical immediate (CLI)
bE	SC L1		Shift right characters (SRC)
bF	Immediate data		Subtract logical immediate (SLI)

Byte 1	Byte 2	Byte 3	Byte 4	
Op Code	**Q-Code**	**Operand or Address**		**Instruction**
C0	Branch condition	Direct target address		Branch on condition (BC)
C2 select	Register	Immediate operand		Load address (LA)

Byte 1	Byte 2	Byte 3	
Op Code	**Q-Code**	**Operand or Address**	**Instruction**
d0	Branch condition	Displacement (+ XR1)	Branch on condition (BC)
d2	Register select	Value (+ XR1)	Load address (LA)
E0	Branch condition	Displacement (+ XR2)	Branch on condition (BC)
E2	Register select	Value (+ XR2)	Load address (LA)
F0	Branch	Displacement (+ ARR)	Branch on ARR (BC)
F1		Displacement (+ IAR)	Jump backward (JC)
F2		Displacement (+ IAR)	Jump on condition (JC)
F4	SVC function select		Supervisor call (SVC)
F5	Control information		Transfer control (XFER)
F6	PMR bit select	Immediate data	Load program mode register (LPMR)

Legend
L1 = Length-1 of operand 1 (in bytes)
L2 = Length-1 of operand 2 (in bytes)
L3 = Length-1 of both operands (in bytes)
SC = Shift count-1 (in bits)

10-440
Identifying CSP Instructions in Hexadecimal Format

When displaying control storage on the control panel display (01-242) or when reading a hexadecimal dump of control storage, you must know what type of information is being displayed: CSP instructions or data used by the CSP. See the *Control Storage Service Information Manual* for details of the control storage arrangement, or see 10-400 ("IPL Good Machine Path") for a general description of the control storage arrangement. The following chart describes the function of each valid hexadecimal representation of a CSP instruction.

Note: *For CSP I/O instructions, see 10-450.*

Machine Code				Function
0 1 2 3	4 5 6 7	8 9 A B	C D E F	
0	Branch address			Branch
1				Branch and link Branch and store address
2	0	Branch address		Branch on carry
	1			Branch high
	2			Branch low
	3			Branch equal
	4			Branch positive, or branch all ones
	5			Branch negative, or branch on a combination of ones and zeros
	6			Branch on zero
	7			Branch on flag
	9			Branch not high
	A			Branch not low
	b			Branch not equal
	C			Branch not positive, or branch not all ones
	d			Branch not negative, or branch on not a combination of ones and zeros
	E			Branch not zero
	F	0	0	Return (to address in MAB)
	F	8	0	Branch extended
Branch address				
2	F	C	0	Branch and link extended
Branch address				
b	F	A	b	Branch on I/O condition (see 10-450) (bFAb instruction disables base + displacement instruction)
3	M	Branch address		

Machine Code								Function
0 1 2 3	4 5 6 7			8 9 A B			C D E F	
3	S	Base		Displacement				Base + displacement: Storage to or from register move
4	X	WR1		Operation			WR2	
3	S	Base		Displacement				Base + displacement: Storage test mask
5	X	WR1		Mask				
3	S	Base		Displacement				Base + displacement: Logical/arithmetic 1 storage to register
6	X	WR1		Operation	X		WR2	
3	S	Base		Displacement				Base + displacement: Logical/arithmetic 2 storage to register
7	0	WR1		Operation	X		WR2	
3	S	Base		Displacement				Base + displacement: Storage set bits off
8	X	WR1		Mask				
3	S	Base		Displacement				Base + displacement: Storage set bits on
9	X	WR1		Mask				
3	S	Base		Displacement				Base + displacement: Load immediate storage
9	X	WR1		Data				
3	S	Base		Displacement				Base + displacement: Storage compare immediate
C	X	WR1		Data				
3	S	Base		Displacement				Base + displacement: Storage subject immediate
D	X	WR1		Data				
3	S	Base		Displacement				Base + displacement: Load address
E	WR1			1	1		WR2	

Legend
M = 4-bit control field (see 10-450)
S = Storage select: 1 = control storage, 0 = main storage
X = Register byte select: 1 = high, 0 = low
WR1 = Work register select for operand 1 (0 through 7)
WR2 = Work register select for operand 2: 2 = WR42, 3 = WR43

10-440 (continued)
Identifying CSP Instructions in Hexadecimal Format

Machine Code						
0 1 2 3	**4**	**5 6 7**	**8 9 A B**	**C**	**D E F**	**Function**
4	X	R1 LSR select	8	0	R2 LSR select	Load 1 byte of main storage to R1
				1		Load 1 byte of main storage to R1; increase R2
			9	0		Read 1 byte of MSP register to R1; decrease R2
				1		Load 1 byte of main storage to R1; decrease R2
	0		A	0		Load 2-byte control storage word to R1
				1		Load 2-byte control storage word to R1; increase R2
	1			0		Load 1 byte of control storage to high byte of R1
				1		Load 1 byte of control storage to high byte of R1; increase R2
	0		b	0		Read 2-byte MSP register to R1; decrease R2
				1		Load 2-byte control storage word to R1; decrease R2
	1			0		Read 2 bytes of main storage to R1; increase R2 by 2
				1		Load 1 byte of control storage to high byte of R1; decrease R2
	X		C	0		Store 1 byte of main storage from R1
				1		Store 1 byte of main storage from R1; increase R2
	0		d	0		Write 1 byte of MSP register from low byte of R1; decrease R2
				1		Store 1 byte of main storage from low byte of R1; decrease R2
	1			0		Write 1 byte of MSP register from high byte of R1; decrease R2
				1		Store 1 byte of main storage from high byte of R1; decrease R2
	0		E	0		Store 2 bytes of control storage from R1
				1		Store 2 bytes of control storage from R1; decrease R2
	1			0		Store 1 byte of control storage from high byte of R1
				1		Store 1 byte of control storage from high byte of R1; increase R2
	0		F	0		Write 2-byte MSP register from R1; decrease R2
				1		Store 2 bytes of control storage from R1; decrease R2
	1			0		Store 2-bytes of main storage from R1; increase R2 by 2
				1		Store 1 byte of control storage from high byte of R1; decrease R2

Legend
M = Control field for I/O devices
X = Register byte select: 1 = high, 0 = low
Y = Register byte select: 1 = high, 0 = low
n = Increase value
R = Register select: 0 = WR0, 1 = WR1
R1 = Data register (LSRs) select
R2 = Address register (in LSRs) select

Machine Code						Function
0 1 2 3	4	5 6 7	8 9 A B	C D E F		
5	0	R1	Mask value			Test low byte of R1 using mask
	1					Test high byte of R1 using mask
6	X		0	n - 1		Add n to R1 (increase by n)
			1	Y	R2	Exclusive OR registers
			2			Zero and add registers
			3			OR registers
			4			Compare registers
			5			AND complement
			6			AND registers
			7			OR complement
			8	n - 1		Subtract n from R1 (decrease by n)
			9	Y	R2	Add registers with carry
			b			Add registers
			b	X	R1	Shift left logical
			C	Y	R2	Subtract registers
			E			Subtract registers with borrow
7	0		0	n - 1		Add n to R1 (increase by n)
			1	0	R2	Exclusive OR registers
			2			Zero and add registers
			3			OR registers
			4			Compare registers
			5			AND complement
			6			AND registers
			7			OR complement
			8	n - 1		Subtract n from R1 (decrease by n)
			9	0		Add registers with carry
			A	Y	R2	Subtract registers (2 bytes minus 1 byte)
			b	0		Add registers
			b	0	R1	Shift left logical double
			C	0		Subtract registers
			d	Y	R2	Add registers (2 bytes plus 1 byte)
			E	0		Subtract registers with borrow
	1	R X 0	MSP register address			Read from MSP register immediate to CSP WR0 or WR1[1]
	1	R X 1	00-FF			Write to MSP register immediate from CSP WR0 or WR1[1]

Machine Code					Function
0 1 2 3	4 5 6 7	8 9 A B			C D E F Function
8	X R1	Immediate data			Set bits off
					AND complement immediate
					AND immediate
9					Set bits on
					OR immediate
					OR complement immediate
A					Load immediate
b	M	0	X	R1	I/O load (see 10-450)
	M	4			I/O sense (see 10-450)
	0	5			Sense interrupt level status byte
	0	6			Processor sense: Storage error byte
	1				Storage control byte
	2				I/O clocks low
	3				Interrupt level backup byte
	4				Run control byte
	5				Control panel display low byte[2]
	6				I/O clocks high and low
	7				IPL status byte[2]
	8				Control mode register
	9				Control panel display high byte[2]
	A				Processor error byte
	b				Processor condition register
	C				Bank address register
	E				Processor sense: PACT CSP register

Legend

M = Control field for I/O devices
X = Register byte select: 1 = high, 0 = low
Y = Register byte select: 1 = high, 0 = low
n = Increase value
R = Register select: 0 = WR0, 1 = WR1
R1 = Data register (LSRs) select
R2 = Address register (in LSRs) select

[1] R = 0, WR0 is used.
R = 1, WR1 is used.
[2] The control panel interface card performs these instructions.

10-440 (continued)
Identifying CSP Instructions in Hexadecimal Format

Machine Code					Function	
0123	4567	89AB	CDEF			
b	M	8	X	R1	I/O control load (see 10-450)	
	0	A	X	R1	Processor load:	Load processor condition register (PCR)
	1		F			Reset carry–set equal
	2		X	R1		Load storage control byte
	6					Load PACT CSP register
	8		F			Set PCR flag bit
	9		X	R1		Load control mode register
	A					Load 8-ms timer interrupt level
	b		F			Reset PCR flag bit
	C		X	R1		Load bank address register
	d		0			Disable interrupt level 5 interrupt
			1			Enable interrupt level 5 interrupt
			2			Reset interrupt level 5 request
			3			Set interrupt level 5 request
			4			Disable external interrupt level 5 request
			5			Enable external interrupt level 5 request
			6			Reset CSP interrupt level 5 request latch
			7			Set CSP interrupt level 5 request latch
			8			Reset bank address register
			9			Set bank address register
			A			Disable 8-ms timer
			B			Enable 8-ms timer
			C			Reset 8-ms timer interrupt
			D			Reset I/O clocks
	E		0			Turn on Program Check light[3]
			1			Set I/O service request
			2			Reset I/O service request
			3			Processor check halt[3]
			4			Disable checks
			5			Enable interrupts
			6			Disable interrupts
			7			Enable checks
			8		Processor load:	Reset MSP

Legend
M = Control field for I/O devices
X = Register byte select: 1 = high, 0 = low
Y = Register byte select: 1 = high, 0 = low
n = Increase value
R = Register select: 0 = WR0, 1 = WR1
R1 = Data register (LSRs) select
R2 = Address register (in LSRs) select

[3] The control panel interface card performs these instructions.

Machine Code				Function	
0 1 2 3	4 5 6 7	8 9 A B	C D E F		
b	E	A	9	Processor load:	Turn on the System in Use light[3]
			A		Turn off the System in Use light[3]
			b		Start the MSP
			C		Turn on the Console Check light[3]
			d		Turn off the Console Check light[3]
			F		Reset the MSP 'temporary stop request' latch
	F		0		Disable the 3-second time-out
			1		Reset the 'MSP stop' latch
			2		Reset the 'machine check' latch
			3		Set the 'MSP temporary stop request' latch
			4		Enable the 3-second time-out
			5		Set the 'MSP stop' latch
			6		Reset the 'retry' latch and the 3-second time-out
			7		Set the 'retry' latch
			9		Set the 'machine check' latch
			C		Hardware IPL command[3]
			E		Processor wait[3]
			F	Processor load:	Power-off request[3]
	M	C	X R1	I/O control sense (see 10-450)	
b	M	d	0	Branch on I/O condition	
0	Branch address				

Machine Code				Function
0 1 2 3	4 5 6 7	8 9 A B	C D E F	
C	X R1	Immediate data		Compare immediate data with R1
d				Add or subtract immediate data from R1 (data is negative for add)
E	0	0	Direct address	Load R1 from direct word in control storage
	1			Store R1 in direct word in control storage
	LSR on active interrupt level 0-B	1 1 X X	LSR on active interrupt level 0-B	Move LSR to LSR
F	X R1	Branch address 8-11	0	Hex branch numeric; 4 bits of R1 → MAR 12-15
			1	Hex branch zone; 4 bits of R1 → MAR 12-15
		0	8	Shift right logical (1-bit right shift of selected byte)
		2	8	Shift right logical double (1-bit right shift of selected 2 bytes)
		0 1 0	Y 1 R2	Move zone to numeric; [R1 (zone) → R1 (numeric); R2 (zone) → R1 (zone)]
		0 1 1		Move zone to zone; [R2 (zone) → R1 (zone)]

Legend
M = Control field for I/O devices
X = Register byte select: 1 = high, 0 = low
Y = Register byte select: 1 = high, 0 = low
n = Increase value
R = Register select: 0 = WR0, 1 = WR1
R1 = Data register (LSRs) select
R2 = Address register (in LSRs) select

[3] The control panel interface card performs these instructions.

10-450
Identifying CSP I/O Instructions in Hexadecimal Format

CSP instructions that start with the digits Bxxx can be I/O instructions (see 10-440).

Perform the following steps to determine the function of a CSP I/O instruction:

1. Display WR0 low for the present interrupt level on the control panel display (01-225).

2. Determine from WR0 low which device is being used by the present I/O instruction:

   00 = Channel
   40 = ELCA
   50 = 1255 MCR attachment
   80 = SLCA and MLCA
   90 = Work station attachment 2
   A0 = Data storage attachment
   C0 = Work station attachment 1
   E0 = System printer
   F0 = I/O controller initialization

3. Use the following charts to determine the function of the hexadecimal I/O instruction for the selected attachment.

Channel I/O Instructions

WR0 Low = 00

Machine Code					Function
0123	4567	89AB	C	DEF	
b	M	0	X	R1	I/O load (X,R1 not used)
	M	4	X	R1	I/O sense
	0 1	4			Sense channel register Sense channel error byte
	M	8	X	R1	I/O control load
	1 2 5 6	8			Load channel register from R1 Reset channel error byte Set channel odd parity Set channel even parity
	M	C	X	R1	I/O control sense
	4 5	C			Sense data bus out and data bus in Sense tag bus in and address register select

Legend
X = Register byte select: 1 = high, 0 = low
R1 = Data register (in LSRs) select

I/O Controller Instructions

WR0 Low = 40 (ELCA), 80 (MLCA), 90 (work station 2), A0 (tape), C0 (work station 1)

Machine Code					Function
0 1 2 3	**4 5 6 7**	**8 9 A B**	**C**	**D E F**	
b	M	0	X	R1	I/O load
	0	0			Load system tag bus in buffer and select op end interrupt
	1				Load data buffer 1
	2				Load data buffer 2
	3				Reset system interrupt request
	4				Load cycle steal pacer and cycle steal block length
	5				Load controller tag bus in buffer and system tag bus in 3/cycle steal counter high
	6				Enable system interrupt request
	7				Disable system interrupt request
	E				Reset transparent mode
	M	4	X	R1	I/O sense
	0	4			Sense data buffer 2
	1				Sense data buffer 1
	2				Sense system interrupt status
	3				Sense controller status
	4				Sense bus coupler configuration
	E				Diagnostic sense data buffer 1
	M	8	X	R1	I/O control load
	0	8			Reset bus coupler
	1				Load processor control bits
	2				Load cycle steal counter low
	3				Load cycle steal and SILSB response bits
	5				Set system interrupt level, initial address load, transparent
	6				Reset system interrupt conditions
	7				Set controller interrupt conditions
	E				Diagnostic load bus coupler

Legend
X = Register byte select: 1 = high, 0 = low
R1 = Data register (in LSRs) select

10-450 (continued)
Identifying CSP I/O Instructions in Hexadecimal Format

1255 MCR I/O Instructions

WR0 Low = 50

Machine Code					
0 1 2 3	4 5 6 7	8 9 A B	C	D E F	Function
b	M	d		0	Branch on I/O condition
0	Branch address				
	0 1 4 6				Controller unit check No controller unit check Diagnostic valid Diagnostic not valid
	M	0	X	R1	I/O load
	0 1 3 4 5 6 7	0			Set diagnostic mode Reset diagnostic mode Reset system interrupt request Set system interrupt request Load data to controller DBI buffer Disable system interrupt request Enable system interrupt request
	M	4	X	R1	I/O sense
	0 1 2 3	4			Controller data byte Controller status byte 1 Controller status byte 2 Controller status byte 3
b	M	8	X	R1	I/O control load
	0 1 2 3 4 5 6 7 8 C	8			Set service needed Set command waiting Reset controller load Set controller load Reset controller single cycle Set controller single cycle Set controller reset Reset controller reset Start controller Reset adapter

Legend
X = Register byte select: 1 = high, 0 = low
R1 = Data register (in LSRs) select

SLCA I/O Instructions

WR0 Low = 80

Machine Code					
0 1 2 3	4 5 6 7	8 9 A B	C	D E F	Function
b	M	0	X	R1	Branch on I/O condition.
	2 3 5 6 7 9	0			Reset time-out interrupt Reset interrupts (not timer) Disable time-out interrupt Enable interrupts (not timer) Enable time-out interrupt Load buffer
	M	4	X	R1	I/O sense
	1 3 6 9	4			Sense byte status register Sense modem status register Sense adapter status register Sense buffer
	M	8	X	R1	I/O control load
	1 2 3 6 9 E F	8			Reset byte status register Load control out register Diskette interrupts Reset disable interrupts Load diagnostic control register Load hardware timer Load adapter control register

Legend
X = Register byte select: 1 = high, 0 = low
R1 = Data register (in LSRs) select

Data Storage Attachment I/O Instructions

WR0 Low = A0

Machine Code					Function
0123	4567	89AB	C	DEF	
b	M	0	X	R1	I/O load
	0	0			Set the number of 128-byte blocks to move between the system and the storage device
	1				Set the number of bytes in the first block to move between the system and the storage device
	2				Set the number of bytes in the first block to move to or from the storage device
	3				Reset interrupt level 4
	6				Enable or disable interrupts to system
	7				Reset all storage devices
	8				Set buffer control
	9				Set buffer mode
	A				Load scan delimiter to buffer
	b				Set continuous transfers
	M	0	X	R1	I/O sense
	0	4			Sense the number of 128-byte blocks to move between the system and the storage device
	1				Sense the number of bytes in the first block to move to or from the system device
	2				Sense the number of bytes in the first block to move to or from the storage device
	3				Sense the number of 128-byte blocks to move to or from the storage device
	8				Sense buffer status
	9				Sense buffer mode
	A				Sense scan hit pointer

Legend
X = Register byte select: 1 = high, 0 = low
R1 = Data register (in LSRs) select

Machine Code					Function
0123	4567	89AB	C	DEF	
b	M	8	X	R1	I/O control load
	0	8			Select storage device and one of its registers
	1				Storage device command
	3				Reset interrupt level 1
	4				Assign storage device to a buffer
	6				Reset checks
	8				Enable or disable storage device interrupts
	9				Assign storage device interrupt to IL1 or IL4
	A				Enable or disable timer
	b				Select buffer
	C				Set cycle steal control bits
	d				Set diagnostic interrupts
	F				Set diagnostic storage device reads and writes
	M	C	X	R1	I/O control sense
	0	C			Sense which storage device and register are selected
	1				Storage device status information
	4				Sense which storage device is assigned to which buffer
	8				Sense storage device interrupts for IL4
	9				Sense storage device interrupts for IL1
	b				Sense channel interface status

10-450 (continued)
Identifying CSP I/O Instructions in Hexadecimal Format

System Printer I/O Instructions

WR0 Low = E0

Machine Code					Function
0 1 2 3	4 5 6 7	8 9 A B	C	D E F	
b	M	d	0		Branch on I/O condition
0	Branch address				
	0				Controller unit check
	4				Interrupt enabled
	5				Diagnostic valid
	6				Diagnostic not valid
	7				3262 attachment installed
	8				Data not ready
	b				Command reject
	d				No checks waiting
	E				Send not ready
4	M	0	X	R2	I/O storage
	2		0	R2	Data transfer (1 byte) from system to printer controller storage
			1		Data transfer (1 byte) from system to printer controller storage; increase R2
b	M	0	X	R1	I/O load
	1				Activate controller start
	3				Reset interrupt request
	5				Enable interrupts
	6				Disable interrupts
	9				Load system data register
	M	4	X	R1	I/O sense
	1				Sense system data register
	2				Sense system data register
	9				Sense system data register
	M	8	X	R1	I/O control load
	3				Set controller mode
	5				Adapter reset
	b				Start of transaction
	C				End of transaction
	M	C	X	R1	I/O control sense
	3				Sense status

HOW TO INTERPRET ERAP REPORTS

See 01-360 for information on how to run the error recording analysis procedure (ERAP).

ERAP error information aids in determining the cause of failures in the processing unit. These failures may be intermittent failures or continuous failures that the MAPs do not find.

Run the ERAP for the area of the processing unit that is failing and look at the error information that has been recorded. If a specific error occurs frequently in the latest entries of the table, suspect an intermittent failure.

If there is no frequent pattern associated with the error history information, use the following information to aid in determining the cause of the error. The information recorded was present when the error occurred.

10-500
CSP Error History Table

```
         ERROR HISTORY TABLE FOR CONTROL STORAGE PROCESSOR


      FROM: XX/XX/XX  XX:XX:XX           TO: XX/XX/XX  XX:XX:XX
                                        CHAN  ECC                     MSP  SB   FAIL
 DATE   TIME  SRC      PCR  IL    PEB  CEB  REG   CHK  MAR    MAB      4   5    2KMS WR0  WR1   WR2    WR3   WR4   WR5   WR6   WR7
YYMMDD HHMMSS . . . . . . . . . . . . . . . . . . . .HEX . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
XXXXXX XXXXXX XXXX     XX   X     XX   XX   XX    XX   XXXX   XXXX    XX  XX    XXXX XXXX XXXX  XXXX   XXXX  XXXX  XXXX  XXXX  XXXX
XXXXXX XXXXXX XXXX     XX   X     XX   XX   XX    XX   XXXX   XXXX    XX  XX    XXXX XXXX XXXX  XXXX   XXXX  XXXX  XXXX  XXXX  XXXX
XXXXXX XXXXXX XXXX     XX   X     XX   XX   XX    XX   XXXX   XXXX    XX  XX    XXXX XXXX XXXX  XXXX   XXXX  XXXX  XXXX  XXXX  XXXX
XXXXXX XXXXXX XXXX     XX   X     XX   XX   XX    XX   XXXX   XXXX    XX  XX    XXXX XXXX XXXX  XXXX   XXXX  XXXX  XXXX  XXXX  XXXX

              10-502     10-506     10-510     10-514     10-518      10-522               10-526
                    10-504     10-508     10-512     10-516      10-520     10-524
```

10-502
System Reference Code

This column contains the system reference code (SRC) that was recorded at the time of the error. See MAP 0113, MAP 0114, MAP 0115, and MAP 0116 for all valid system reference codes and their meanings.

10-504
Processor Condition Register

The processor condition register (PCR) contains information about the status of the last operation (of the type that affects of PCR) performed in the CSP.

Bit(s)	Description
0	Flag This bit is a flag bit controlled completely by the microcode running in the CSP.
1	Positive Result This bit indicates that an instruction generated a positive result from the ALU.
2	Negative Result This bit indicates that an instruction generated a negative result from the ALU.
3	Zero This bit indicates that an instruction generated a result of zero from the ALU.
4	Carry This bit indicates that an add instruction generated a carry out from the high-order position, or that a subtract instruction ran without a borrow to the high-order.
5	High This bit indicates that an add or subtract instruction generated a positive result (the first operand is higher than the second operand).
6	Low This bit indicates that an add or subtract instruction generated a negative result (the first operand is lower than the second operand).
7	Equal This bit indicates that an instruction generated a result of zero.

10-506
Interrupt Level Backup Byte

The interrupt level backup byte (ILBB) indicates on which hardware interrupt level the CSP was running when the error occurred. The contents of the interrupt level (IL) field in the error history table have the following meanings.

IL Field	Controller Interrupt Level
5	5
4	4
3	3
2	2
1	1
Blank	Main program level

10-508
Processor Error Byte

The processor error byte (PEB) indicates the type of error detected by the CSP during an I-cycle, an E-cycle, or during a cycle steal operation. If one of these bits is set during a cycle steal operation, bit 6 of the channel error byte (10-510) is also set.

Bit(s)	Description
0	Storage Check One of the following caused an error: • An uncorrectable ECC error • Bad parity from control storage
1	System Bus Parity Check The CSP read bad parity on the system bus.
2	4-Second Time-out The program failed to recover from a loop within 1 second after a 3-second time-out.
3	Data Flow Parity Check The CSP detected bad parity in the internal data flow.
4	Processor Check One of the following sets this bit: • A processor error or a channel error • A 4-second time-out • A processor check halt instruction
5	3-Second Microcode or 8-Millisecond Hardware Time-out If bits 6 and 7 are off, this bit indicates a 3-second microcode time-out. If bit 6 or 7 is on, this bit indicates an 8-millisecond hardware time-out. The time-out was caused by the device indicated by bit 6 or 7.
6	Channel Check
7	MSP Check An error occurred during a CSP access to the MSP registers or storage. See MSP status bytes 4 and 5 to determine the type of error (10-558 and 10-560).

10-510
Channel Error Byte

When the channel senses an error, it sets a bit in the channel error byte (CEB) to indicate the type of error that occurred. This error checking occurs even if error checking is disabled for the CSP.

Bit(s)	Description
0	DBO Parity Check This bit indicates that an I/O attachment sensed a parity error in the data it received from the channel. The I/O attachment sends the '-tag bus in 5' signal to the channel. The channel sets this bit on and sends a channel check to the CSP.
1	Not Valid Device Address This bit indicates that the channel sent a device address on the output data bus ('bi-di 8-15') but received no answer in the time permitted (a time-out occurred). The channel generates a blast condition (10-830) to clear the channel and sends a channel check to the CSP.
2	DBI Parity Check This bit indicates that the channel sensed a parity error on data coming from an attachment. The channel generates a blast condition (10-830) to clear the channel and sends a channel check to the CSP.
3	I/O Time-out Check This bit indicates that an I/O attachment did not deactivate the '-service in' signal in the specified time following the '-service out' signal. The channel generates a blast condition (10-830) to clear the channel and sends a channel check to the CSP.
4	This bit indicates that the channel received bad parity on the system bus from either the CSP or the MSP.
5	Not used.
6	Cycle Steal Is Active This bit indicates that the channel performed a cycle steal operation. The channel resets this bit when the operation is complete, unless a machine check occurs. When a machine check is present, this bit does not change. The CSP can then use this bit to determine which operation (instruction processing or cycle steal) the channel was doing when the machine check occurred.
7	Sense Interrupt Level Status Bits Operation This bit indicates that a processor check or a channel check occurred during an SILSB instruction.

10-512
Channel Register

The channel register stores information about the type of operation that the channel last performed. The status of bits 6 and 7 in the channel error byte (CEB) determines the contents of bits 0 through 3 in the channel register. Bits 4 through 7 in this register are not used.

CEB Bit(s)		
6	7	Channel Register Bits 0-3 Contents
0	0	Bits 0-3 contain the device address that the CSP used for the last I/O instruction performed (10-615).
0	1	Bits 0-3 contain the interrupt level that the SILSB instruction last polled (10-615).
1	0	When bit 0 = 0, bits 1-3 contain the encoded cycle steal ID bit for the I/O device that received the cycle steal (10-615). When bit 0 = 1, if bits 1-3 = 000, no device responded. When bit 0 = 1, if bits 1-3 = 000 through 111, they are not used.

10-514
Storage Error Byte

The storage error byte stores flags for errors that occur during accesses to control storage. This byte is not recorded in ERAP. However, this byte can be displayed on the control panel (01-330).

Bit(s)	Description
0-4	ECC single-bit error log
5	LSR Write Exception Check This bit indicates that an instruction wrote to a CSP LSR when it was not permitted.
6	Storage Control Not Correctable Error This bit indicates that one of the following occurred: • An ECC error during a control storage read in ECC mode • A parity error during a control storage read in parity mode
7	Not used.

10-516
Microinstruction Address Register

This field contains the MAR of the interrupt level indicated by the interrupt level backup byte. The value in the MAR represents the address plus 1 of the microinstruction that the CSP was performing when the error occurred.

10-518
Microinstruction Address Backup Register

This field contains the address that the MAB (of the interrupt level indicated by the interrupt level backup byte) contained at the time of the check. The address is of the next microinstruction to be performed after the next return microinstruction performed on the interrupt level. Usually, the MAB contains the address of the next microinstruction after the last branch and link microinstruction performed on the interrupt level.

10-520
MSP Status Byte 4

MSP status byte 4 (SB4) contains flags for errors that occur during MSP operations or during CSP or channel accesses to MSP registers or main storage. Following a reset instruction, the register is cleared to zero. See 10-558 for a description of the bits in SB4.

10-522
MSP Status Byte 5

MSP status byte 5 (SB5) contains flags for errors that occur during MSP operations or during CSP or channel accesses to MSP registers or main storage. Following a reset instruction, the register is cleared to zero. See 10-560 for a description of the bits in SB5.

10-524
Failing 2K Page of Main Storage

If main storage caused the error, this field contains the page address of the failing 2K page in main storage. If main storage did not cause the error, this field is not valid.

To determine if main storage may have caused the error, check for any of the following conditions:

- Bit 4 or 5 of MSP status byte 4 (SB4) is on (10-558).
- SRC is 120x (10-552).

See 10-360 to identify a failing main storage card.

10-526
Work Registers 0 through 7

These values represent the contents of work registers 0 through 7 of the interrupt level indicated by the interrupt level backup byte.

10-550
MSP Error History Table

```
        ERROR HISTORY TABLE FOR MAIN STORAGE PROCESSOR


    FROM:  XX/XX/XX  XX:XX:XX          TO: XX/XX/XX  XX:XX:XX
                        STATUS   FAIL                                                          ATRS . .               . PACT REGS . .
 DATE   TIME    SRC    0  2  4  5   2K  OP  Q  PMR  IAR  ARR   XR1    XR2    OP1    OP2  PSREG  IR    01    02   RQ BMR
YYMMDD HHMMSS    . . . . . . . . . . . . . . HEX . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
XXXXXX XXXXXX  XXXX   XX XX XX XX XXXX XX  XX XX   XXXX XXXX  XXXX   XXXX   XXXX   XXXX XXXX   XXXX XXXX XXXX XX XX  XXXXXXXXXXXXXXXX
XXXXXX XXXXXX  XXXX   XX XX XX XX XXXX XX  XX XX   XXXX XXXX  XXXX   XXXX   XXXX   XXXX XXXX   XXXX XXXX XXXX XX XX  XXXXXXXXXXXXXXXX
XXXXXX XXXXXX  XXXX   XX XX XX XX XXXX XX  XX XX   XXXX XXXX  XXXX   XXXX   XXXX   XXXX XXXX   XXXX XXXX XXXX XX XX  XXXXXXXXXXXXXXXX
XXXXXX XXXXXX  XXXX   XX XX XX XX XXXX XX  XX XX   XXXX XXXX  XXXX   XXXX   XXXX   XXXX XXXX   XXXX XXXX XXXX XX XX  XXXXXXXXXXXXXXXX
```

10-552 10-558 10-564 10-570 10-576 10-582 10-588 10-594

10-554 10-5560 10-566 10-572 10-578 10-584 10-590

10-556 10-562 10-568 10-574 10-580 10-586 10-592

10-552
System Reference Code

This column contains the system reference code (SRC) that was recorded at the time of the error. If the SRC is 120x, IPL diagnostics detected the error, and only the date, time, SRC, and fail 2K entries are valid. See MAP 0113, MAP 0114, MAP 0115, and MAP 0116 for all valid system reference codes and their meanings.

10-554
MSP Status Byte 0

MSP status byte 0 (SB0) is a sense-only byte that the CSP senses. The control logic updates status byte 0 to indicate the present state of the logic as it drives the data flow. The sequencer bits define the step of the I- or E-cycle in which the MSP is operating.

Bit(s)	Description
0	When set, this bit indicates that a fast task operation is occurring.
1-3	Not used.
4	Sequencer 0
5	Sequencer 1
6	Sequencer 2
7	Sequencer 3; this sequencer drives the MSP during instruction operation.

10-556
MSP Status Byte 2

MSP status byte 2 (SB2) contains check and control information for the main storage processor. The following chart describes the bits in this status byte.

Bit(s)	Description
0	When set, this bit indicates that the MSP has sensed an instruction that it cannot perform.
1	Not used.
2	MS Address Compare Stop When set, this bit indicates that the MSP or the CSP made a main storage access to the address specified for an address compare stop.
3	Not used.
4	First Cycle When set during an E-cycle, this bit indicates that the MSP is using the first byte of an operand.
5	Recomplement Cycle Used as a diagnostic bit.
6	MSP Checks When set, this bit indicates that at least 1 bit in either status byte 4 or status byte 5 is set.
7	Carry In Used as a diagnostic bit.

10-558
MSP Status Byte 4

MSP status byte 4 (SB4) contains flags for errors that occur during MSP operations or during CSP or channel accesses to MSP registers or main storage. Following a reset instruction, status byte 4 is cleared to zero.

Bit(s)	Description
0	Not used.
1	Task 0 Parity Check The MSP or CSP accessed the Task 0 buffer, which had bad parity on its data out bus.
2	0 = The MSP has not accessed the first 2K page of main storage. 1 = The MSP has accessed the first 2K page of main storage.
3	Not Valid Main Storage Address The MSP or CSP accessed a main storage address larger than the amount of main storage installed.
4	Single-Bit Storage Error A main storage location had 1 bad bit, which was corrected.
5	Multiple-Bit Storage Error A main storage location had more than 1 bad bit, which was corrected.
6	Not used.
7	Storage Exception Check The CSP accessed Task 0, Task 1, or I/O ATRs, and one or more of the three most significant bits is set.

10-560
MSP Status Byte 5

MSP status byte 5 (SB5) contains flags for errors that occur during MSP operations or during CSP or channel accesses to MSP registers or main storage. Following a reset instruction, status byte 5 is cleared to zero.

Bit(s)	Description
0	X-register parity check
1	Y-register parity check
2	Not used.
3	MSP bus parity check
4-6	Not used.
7	MSP Storage Exception Check One of the following occurred: • The MSP accessed Task 0, and one or more of the three most significant bits in the ATR is set. • The MSP attempted to load the PMR or the PACT registers when in the not-privileged mode.

10-562
Failing 2K Page of Main Storage

If main storage caused the error, this field contains the page address of the failing 2K page in main storage. If all other fields except this field and the date, time, and SRC fields are zero, the failing 2K page was detected during IPL and caused the IPL to fail.

If main storage did not cause the error, this field is not valid.

To determine if main storage could have caused the error, check for any of the following conditions:

- Bit 4 or 5 of MSP status byte 4 (SB4) is on (10-558).
- SRC is 120x (10-552).

See 10-360 to identify a failing main storage card.

10-564
OP Register

The OP (operation) register contains the control byte of an MSP instruction when the instruction is fetched from main storage.

10-566
Q-Byte

This field is the contents of the Q-byte in the MSP local storage registers. This byte is loaded with the Q-byte of an instruction at the start of the instruction and is not changed while the instruction is running.

10-568
Program Mode Register

The program mode register (PMR) controls address translation for MSP accesses to main storage. The PMR also protects the ATRs and PACT registers from change by programs that are not privileged. The bits of the PMR have the following meanings.

Bit(s)	Description
0	Disable Task Switching Bit This bit can be set by the system software to prevent a task switch.
1,2	Not used; must be zero.
3	When off, this bit selects PACT register PXR1 to make operand addresses that are indexed by XR1 (10-670).
4	When off, this bit selects PACT register PIAR to make addresses for instruction fetches (10-670).
5	When off, this bit selects PACT register PXR2 to make operand addresses that are indexed by XR2 (10-670).
6	When off, this bit selects PACT register PDIR for address translation of direct operand addresses.
7	Not Privileged Mode 1 = The MSP is not operating in privileged mode. If any MSP instruction attempts to change a PACT register or the PMR, a storage exception check occurs. 0 = The PACT registers and the PMR can be changed without generating a storage exception check.

10-570
Instruction Address Register

This field contains the logical address (before translation) of the next instruction to be performed in normal sequence by the MSP.

10-572
Address Recall Register

The address recall register (ARR) is a general work register that can contain the address of an earlier instruction.

10-574
XR1

XR1 is a general-purpose index register.

10-576
XR2

XR2 is a general-purpose index register.

10-578
OP1

The OP1 register contains the logical address of operand 1 (before translation).

10-580
OP2

The OP2 register contains the logical address of operand 2 (before translation).

10-582
PSREG

This field contains the 2 low bytes of the storage address for the data to be loaded into the MSP registers, or for the MSP registers to be stored in during a fast task switch. The high byte of this address is in PREG (one of the PACT registers).

10-584
ATRS IR

This field is the contents of the address translation register that would be used to translate addresses for an instruction if translation is specified. See 10-568 to determine if translation is specified.

10-586
ATRS 01

This field is the contents of the address translation register that would be used to translate addresses for operand 1 if translation is specified. See 10-568 to determine if translation is specified.

10-588
ATRS 02

This field is the contents of the address translation register that would be used to translate addresses for operand 2 if translation is specified. See 10-568 to determine if translation is specified.

10-590
Q-Register

This field is the contents of the Q-register. This register is loaded with the Q-byte of an instruction, but can be changed while the instruction is running.

10-592
Backup Mode Register

The backup mode register (BMR) is not used and always contains a value of 00.

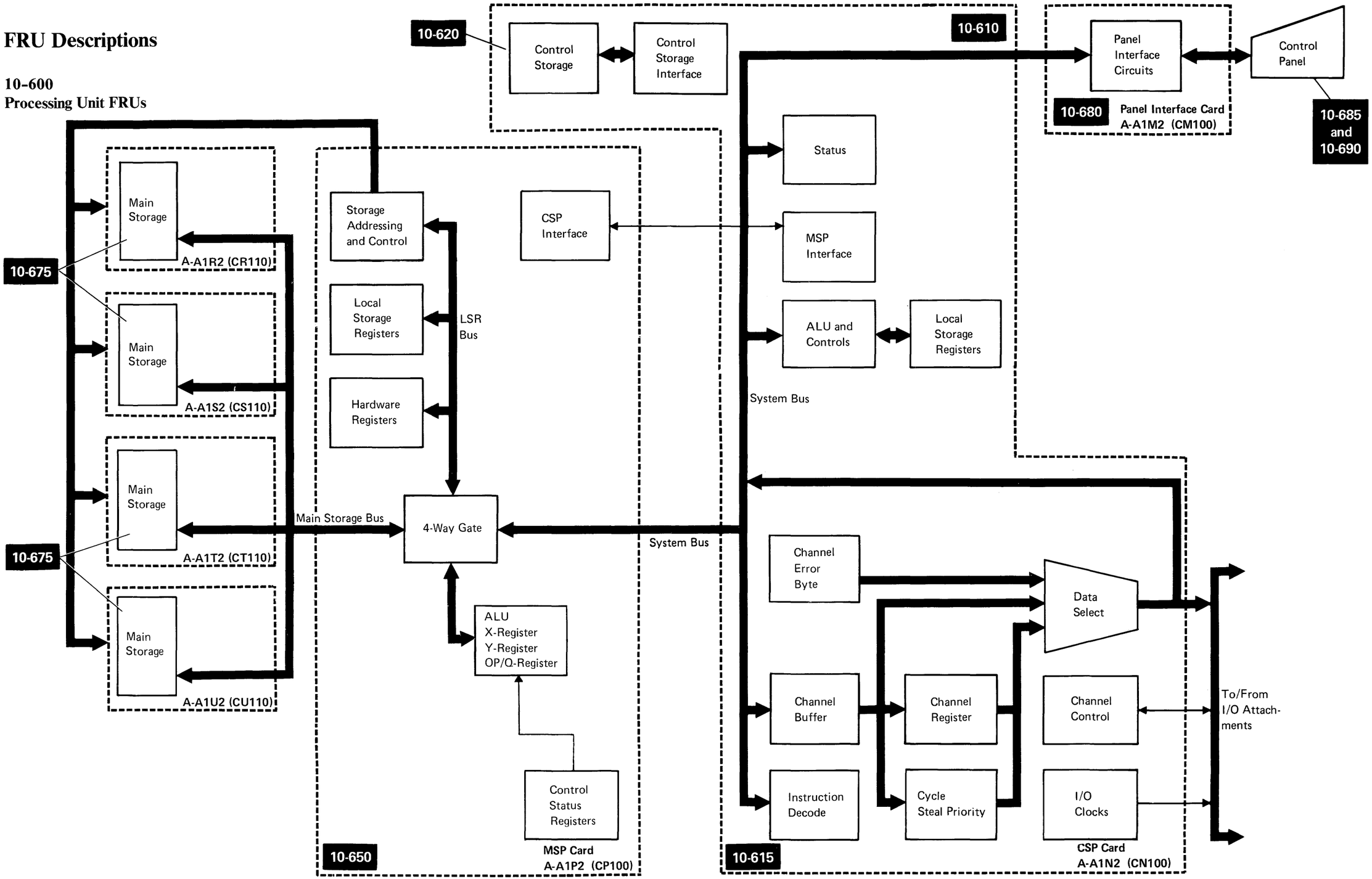
10-594
PACT Registers

This 16-character field is the contents of the eight PACT registers (10-670). The values are run together on the printout with 2 characters representing the contents of each register. Reading the field from left to right, the registers are in the following sequence:

- PDIR
- PXR1
- PXR2
- PIAR
- PREG
- PATR
- Pxxx (not used)
- Pxxx (not used)

FRU Descriptions

10-600
Processing Unit FRUs



CONTROL STORAGE PROCESSOR

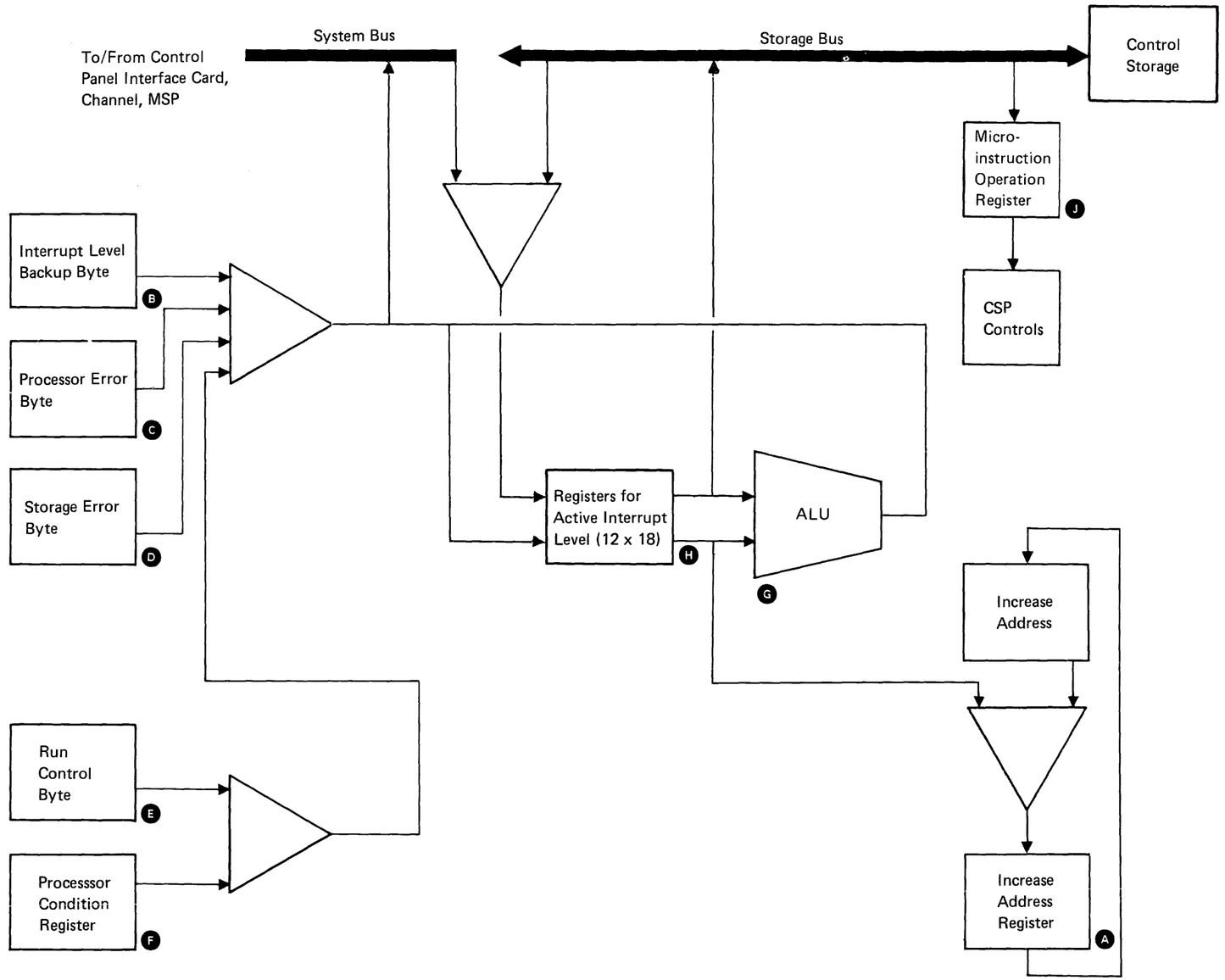
10-610
CSP Card

The CSP card controls the actions of the system that support the System Support Program Product (SSP) and the user programs, such as:

- Loading the SSP into the main storage processor
- Controlling input/output operations
- Sensing machine status
- Recording errors
- Recovering from errors

See the Sequence of Events sections (starting at 10-810) for the actions that occur during these operations.

The circuits that perform the functions of the control storage processor are contained on one card in location A-A1N2.



Increase Address Register (A)

The increase address register holds the address of the next instruction to be performed in the CSP.

Interrupt Level Backup Byte (B)

The interrupt level backup byte (ILBB) indicates in which the CSP is operating. When an error occurs, the contents of this byte are stored in the error table to aid in determining the conditions at the time of the error. The CSP can sense this byte by using a sense CSP control register instruction or a sense ILBB instruction. Because some of the values are the same for different operation levels, the CSP control program uses this byte together with the channel error byte (10-510) and the channel register (10-512) to completely determine error conditions. Only bits 4 through 7 of the ILBB are used; bits 0 through 3 are not used. See 01-325 to display this byte on the control panel.

The following table shows the operation levels for the possible values in bits 4 through 7 of the ILBB.

ILBB Bit(s) 4 5 6 7	CSP Operation Level
1 x x x	Machine Check Level Bits 5 through 7 contain the code for the operation level that was active when the machine check occurred.
x 1 0 1	Interrupt level 1
x 1 0 0	Interrupt level 2
x 0 1 1	Interrupt level 3
x 0 0 1	Interrupt level 4
x 0 0 0	Interrupt level 5
x 1 1 1	Main program level
x 0 1 0	Cycle steal

Processor Error Byte (C)

The processor error byte stores indicators of error conditions that occur in the CSP. These error conditions normally cause a machine check interrupt unless checks have been disabled by:

- Performing a CPU immediate instruction
- Pressing the Force CSP Run key on the control panel (01-317)
- Installing a board jumper to disable checks (01-317)

Even if checks are disabled, the bits in this byte are set when the error occurs. Therefore, you must clear this byte before running the CSP with checks enabled.

The following conditions clear the processor error byte:

- Performing a CPU immediate command (reset machine check interrupt)
- Starting a power-on reset
- Pressing the System Reset key on the control panel

The processor error byte is not reset by a load operation, so that you can load the processing unit following a machine check without destroying the information in the processor error byte. This byte can be sensed with a CPU immediate instruction and can also be displayed on the control panel (01-330). See 10-508 for a list of the error conditions represented in the processor error byte.

Storage Error Byte (D)

The storage error byte stores flags for errors that occur during accesses to control storage. These errors cause a machine check interrupt unless checks have been disabled by:

- Performing a CPU immediate instruction
- Pressing the Force CSP Run key on the control panel (01-317)
- Installing a board jumper to disable checks (01-317)

Even if checks are disabled, the bits in this byte are set when the error occurs. Therefore, you must clear this byte before running the CSP with checks enabled.

The following conditions clear the storage error byte:

- Performing a CPU immediate command (reset machine check interrupt)
- Starting a power-on reset
- Pressing the System Reset key on the control panel

A load operation does not reset the storage error byte; you can load the processing unit following a machine check without destroying the information in the storage error byte. This byte can be sensed with a CPU immediate instruction. See 10-514 for the meaning of the bits in this byte. See 01-330 to display the storage error byte on the control panel.

10-610 (continued)
CSP Card

Run Control Byte (E)

The run control byte (RCB) contains processor control information. The CSP can sense this byte by using a sense CSP control register instruction or a sense RCB instruction. The following table shows the meaning of each bit in the RCB.

Bit(s)	Description
0	MSP Stop This bit stops the MSP after the MSP completes its present instruction. A set MSP stop latch instruction sets this bit. Either a reset MSP stop latch instruction or a PCB reset instruction resets this bit.
1	Address Compare Enable This bit permits the CSP to stop during either main storage address compare or control storage address compare operations.
2	Control Storage Address Compare This bit indicates to the CSP the type of address compare on which to stop. 1 = Stop on control storage address compare. 0 = Stop on main storage address compare.
3	Address Compare This bit indicates that the CSP stopped because of an address compare.
4	I/O Service Request This bit stops the MSP after its present instruction. A set service request instruction sets this bit. Either a reset service request instruction or a PCB reset instruction resets this bit.
5	Always on.
6	Control Panel Instruction This bit indicates that the CSP stopped because of an instruction that uses the control panel.
7	Always on.

Processor Condition Register (F)

The processor condition register contains indicators for the conditions that are tested by the jump on condition (JC) instruction. The bits in the register are set by instructions that run in the CSP. See 10-504 for the bits and their meanings. See 01-325 to display this register on the control panel.

Arithmetic and Logic Unit (G)

The arithmetic and logic unit (ALU) is a 2-byte wide processor that performs arithmetic and logic operations on data from the LSR set or control storage to generate the signals and addresses needed to control system operation. The ALU can operate on either 2-byte or 1-byte data. When operating in 1-byte mode, only bits 8 through 15 of the internal data are used in the ALU. Input data to the ALU comes from the two outputs of the register set during normal instruction processing. The output from the ALU is stored in the local storage registers (H) under control of the present microinstruction.

Local Storage Registers (H)

The CSP local storage registers (LSRs) are a set of seventy-two 2-byte registers. These registers are assigned as follows:

- Ten registers to each of the six CSP operation levels (main program level and interrupt levels 1 through 5)
- Ten registers for machine check interrupts
- Two registers used by the CSP for base-plus-displacement instructions

Each operation level of the CSP has the following registers in the LSRs:

- Microinstruction address register (MAR): This register contains an address that is one more than the control storage address of the microcode instruction that is running in the CSP.
- Microinstruction address backup (MAB) register: When a branch and link or a branch and link long instruction is performed, this register contains an address that is one more than the control storage address of the microcode instruction that was just completed (the return address) in the CSP.
- Work registers 0 through 7 (WR0-WR7): These eight registers can be used for:
  - Data buffers
  - Address registers
  - Operand registers for the ALU to use for its internal calculations
  - Input/output control registers for transfer to or from the channel and the attachments.

The address registers that are used during cycle steal operations are separate from the CSP LSRs. These registers are selected by control lines from the channel ('ARS bits 4-7') and contain the address of the area in the processing unit that will be used in the cycle steal operation (MSP registers, main storage, CSP registers, or control storage).

The following table shows the locations of the registers for each operation level in the CSP. While the CSP is stopped, the control storage locations shown in the table contain copies of all CSP LSRs. See 01-225 for a procedure to display on the control panel those registers in the table that have associated register addresses.

Microinstruction Operation Register (J)

The microinstruction operation register (MOR) contains the microinstruction that has been read from control storage. The microinstruction that is in the MOR controls the operation of the CSP.

	Main Level		Machine Check		Interrupt Level 1		Interrupt Level 2		Interrupt Level 3		Interrupt Level 4		Interrupt Level 5		Cycle Steal	
	Local Storage Register Number															
Register	Register Address	Storage Location	Register Address	Storage Location	Register Address	Storage Location	Register Address	Storage Location	Register Address	Storage Location	Register Address	Storage Location	Register Address	Storage Location	Register Adress	Storage
MAR	8	FF11	A	FFd1	C	FF31	E	FF51	28	FF71	2C	FF91	2E	FFb1		
MAB	9	FF13	b	FFD3	d	FF33	F	FF53	29	FF73	2d	FF92	2F	FFb3		
WR 0 or CS 0	0	FF01		FFC1	10	FF21	18	FF41	20	FF61	30	FF81	38	FFA1		FFE0
WR 1 or CS 1	1	FF03		FFC3	11	FF23	19	FF43	21	FF63	31	FF83	39	FFA3		FFE1
WR 2 or CS 2	2	FF05		FFC5	12	FF25	1A	FF45	22	FF65	32	FF85	3A	FFA5		FFE2
WR 3 or CS 3	3	FF07		FFC7	13	FF27	1b	FF47	23	FF67	33	FF87	3b	FFA7		FFE3
WR 4 or CS 4	4	FF09		FFC9	14	FF29	1C	FF49	24	FF69	34	FF89	3C	FFA9		FFE4
WR 5 or CS 5	5	FF0b		FFCb	15	FF2b	1d	FF4b	25	FF6b	35	FF8b	3d	FFAb		FFE5
WR 6 or CS 6	6	FF0d		FFCd	16	FF2d	1E	FF4d	26	FF6d	36	FF8d	3E	FFAd		FFE6
WR 7 or CS 7	7	FF0F		FFCF	17	FF2F	1F	FF4F	27	FF6F	37	FF8F	3F	FFAF		FFE7
CS 8																FFE8
CS 9																FFE9
CS A																FFEA
CS B																FFEb
CS C																FFEC
CS D																FFEd
CS E																FFEE
CS F																FFEF

Legend
CS = cycle steal register
WR = work register

10-615
Channel

The channel, which is part of the CSP card, is the data path between the processing unit (including storage) and the I/O attachments of the system. The channel buffers the data and supplies control and timing functions for the data transfer operations. The data path of the channel interface is a 2-byte bidirectional bus (bi-di 0-7, P, 8-15, P) that is normally used as two single-byte buses, one for input (bi-di 0-7, P) and one for output (bi-di 8-15, P).

The channel is the data path for the following functions in the system:

- Moving data between control storage or main storage and the I/O attachments
- Moving data between the CSP local storage registers or the MSP registers and the I/O attachments
- Transferring control information from the CSP to the I/O attachments
- Transferring status information from the I/O attachments to the CSP

See the Sequence of Events sections (starting at 10-810) for the actions that occur during these data transfer operations.

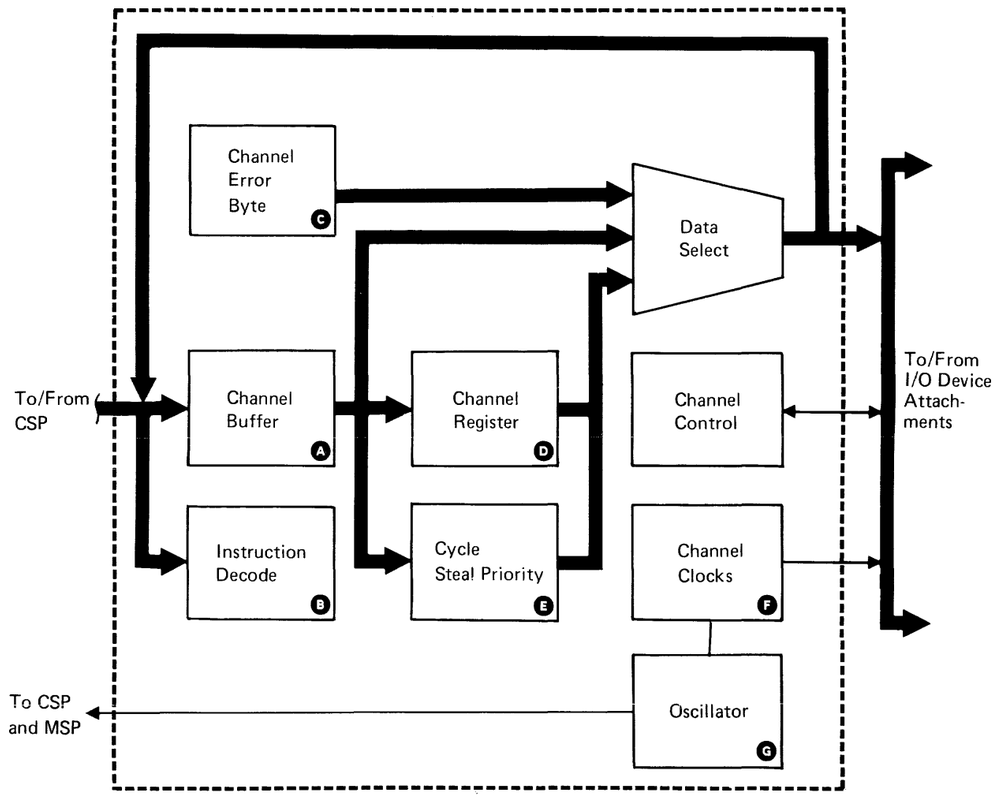
Channel Buffer A

The channel buffer is an intermediate storage register for all data that passes through the channel. This buffer permits the channel to synchronize with the attachments and the processing unit.

Instruction Decode B

The instruction decode receives I/O instructions from the CSP and generates the necessary timing and control signals for the requested function.

The instructions come from the CSP on the internal system bus. Each instruction is 2 bytes wide. The contents of work register zero low (WR0 low) in the CSP are used to determine the address of the requested I/O device. When the CSP sends the command to the channel, it also sends WR0 low. The channel then combines the information from WR0 low with the command modifier field of the instruction and sends this information to the attachment on the bi-di 8-15 bus.



When an instruction is for a specific device, the format of WR0 low is:

Bit(s) 0-3	Bit(s) 4-7
Device address	0

The device address is an encoded address that selects the attachment that the transfer operation is for. The device addresses are:

Address (WR0 Low) 0-3	Assigned Device
0	Channel (used for channel sense information and initialization)
2	Local area network attachment
4	ELCA
5	1255 MCR attachment
8	SLCA or MLCA
9	Work station attachment 2
A	Data storage attachment
B	6157 tape adapter
C	Work station attachment 1
E	System printer
F	I/O controller initialization

When an instruction is for more than one device (sense interrupt level status byte), the format of WR0 low is:

Bit(s) 0-3	Bit(s) 4-7
Interrupt address	0

The interrupt address selects all attachments on an interrupt level. All devices with an active interrupt on that interrupt level will return their interrupt ID bit on the bi-di 0-7 bus in response to this command. Interrupt address hex 0 cannot be assigned to any I/O interrupt. The device assigned to each bit is:

Interrupt level 2
- bi-di bit 0 = Data communications
- no bit set = IL2 8-millisecond timer

Interrupt level 4
- bi-di bit 0 = Work station attachment 2
- bi-di bit 1 = 1255 MCR attachment
- bi-di bit 2 = Work station attachment 1
- bi-di bit 3 = System printer
- bi-di bit 6 = Data storage attachment

Input/Output (I/O) Instructions

The channel responds to two types of I/O instructions from the CSP:

- I/O immediate
- I/O branch on condition

See 10-821 for the sequences for processing these instructions. See 10-450 for a list of the I/O instructions used by each device.

I/O Immediate Instructions

Format (2 Bytes)	Function
1011 mmmm ffff hrrr	Loads and gets data directly between channel and attachments, and the CSP. The fields have the following meanings: • 1011 is the op code for I/O immediate instructions. • mmmm is a modifier that is defined for each attachment. • ffff is a function field that identifies the type of instruction: – 0 is I/O load. – 4 is I/O sense. – 5 is sense interrupt level status byte. – 6 is processor sense. – 8 is I/O control load. – A is processor load. – C is I/O control sense. – D is I/O branch on condition. • h selects the byte of the register selected by rrr: 1 = high byte, 0 = low byte. • rrr selects one of eight local storage registers, except during a processor load when it is a modifier for the mmmm value.

I/O Branch On Condition Instructions

Format (4 Bytes)	Function
1011 mmmm 1101 0000 0000 @@@@ @@@@ @@@@	This instruction is a type of I/O immediate instruction. This instruction tests a condition on the selected attachment. If the condition is met, the instruction causes a branch in the CSP microcode. The branch goes to an area of microcode that permits the CSP to respond to the condition. If the condition is not met, the CSP continues with the normal sequence of microcode. The fields have the following meanings: • 1011 is the op code for the I/O immediate instructions. • mmmm is a modifier that is defined for each attachment. • 1101 is the function code that indicates this is an I/O branch on condition instruction. • @@@@@@@@@@@@ is a 12-bit address that supplies part of the address in control storage to which the microcode will branch if the condition tested is met.

10-615 (continued)
Channel

Channel Error Byte C

When the channel senses an error, it sets a bit in the channel error byte to indicate the type of error that occurred. This error checking occurs even if error checking is disabled for the CSP. During error recovery procedures, the CSP control program can get this information from the channel to determine the type of error that occurred. The contents of the channel error byte can be displayed on the control panel (01-335). See 10-510 for a description of each bit in the channel error byte.

Channel Register D

The channel register stores information about the type of operation that the channel last performed. The CSP can sense the contents of the channel register; the CSP can also load the channel register. The status of bits 6 and 7 in the channel error byte (CEB) determines the contents of bits 0 through 3 in the channel register. Bits 4 through 7 in this register are not used. The contents of the channel register can be displayed on the control panel (01-335). See 10-512 for a description of each bit in the channel register.

Cycle Steal Priority E

There are two levels of priority when performing a cycle steal operation: system interrupt priority and priority of the attachment compared with all attachments that are attempting to do a cycle steal.

Once the channel has been recognized for a cycle steal operation, it generates sense cycle steal ID command to the attachments. Those attachments that need a cycle steal operation respond by setting their assigned bit on the bidirectional data bus, bi-di 0-7. The bits are assigned to each attachment using a fixed priority (bit 0 is the highest priority, bit 7 is the lowest priority), so that the channel only searches for the highest priority bit that is set to determine which attachment is permitted to start the cycle steal. For example, if the channel register contains hex 4x, the cycle steal ID bit is bi-di bit 4. The following table describes the bits for cycle steal ID.

Bi-Di Bit(s)	Attachment
0	Not used
1	MLCA or ELCA controller
2	Local area network attachment
3	Not used
4	Data storage attachment
5	6157 tape adapter
6	Work station attachment 2
7	Work station attachment 1

Channel Clocks F

The channel sends five separate clock signals to the attachments for timing of data transfer operations. These signals are pulses that occur at the following rates:

- 100 nanoseconds
- 512 microseconds
- 1024 microseconds
- 131 milliseconds
- 1048 milliseconds (1 second)

During normal operations, these clocks are always working and are not stopped by a processor check condition. However, they can be stopped during diagnostic testing.

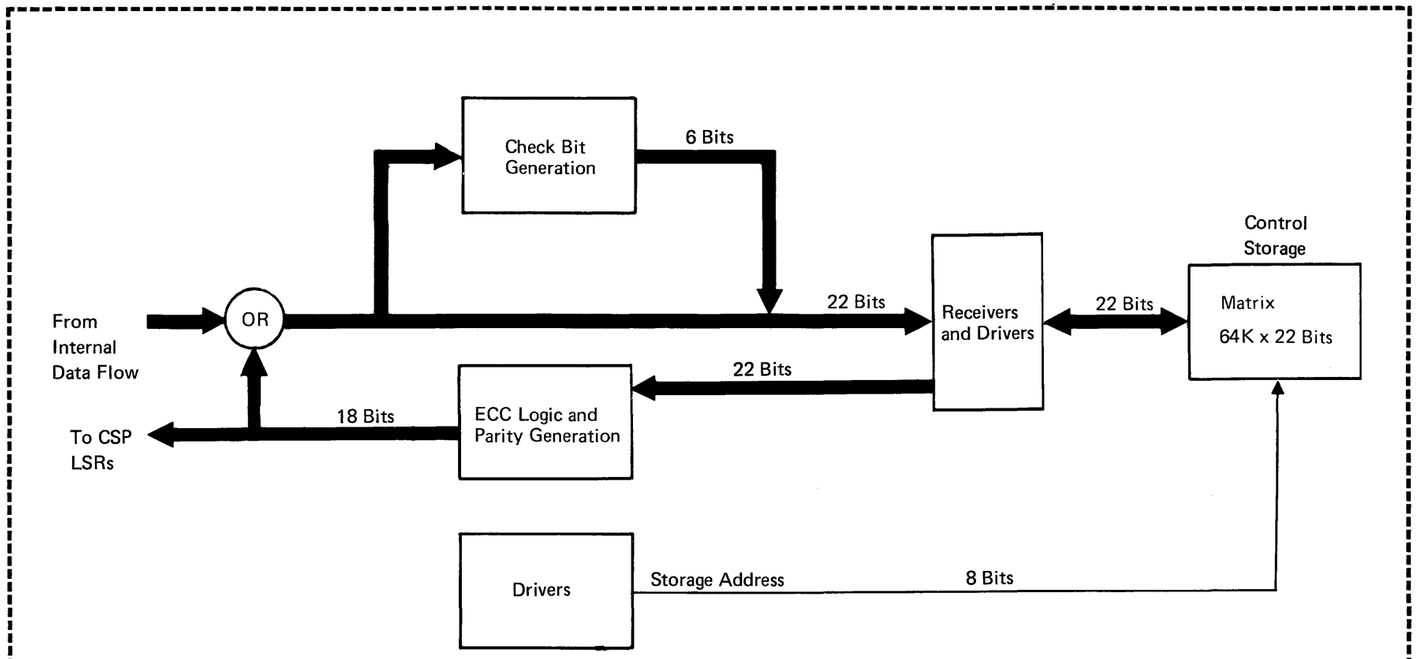
Oscillator G

The oscillator generates timing pulses used to generate the channel clocks.

10-620
Control Storage

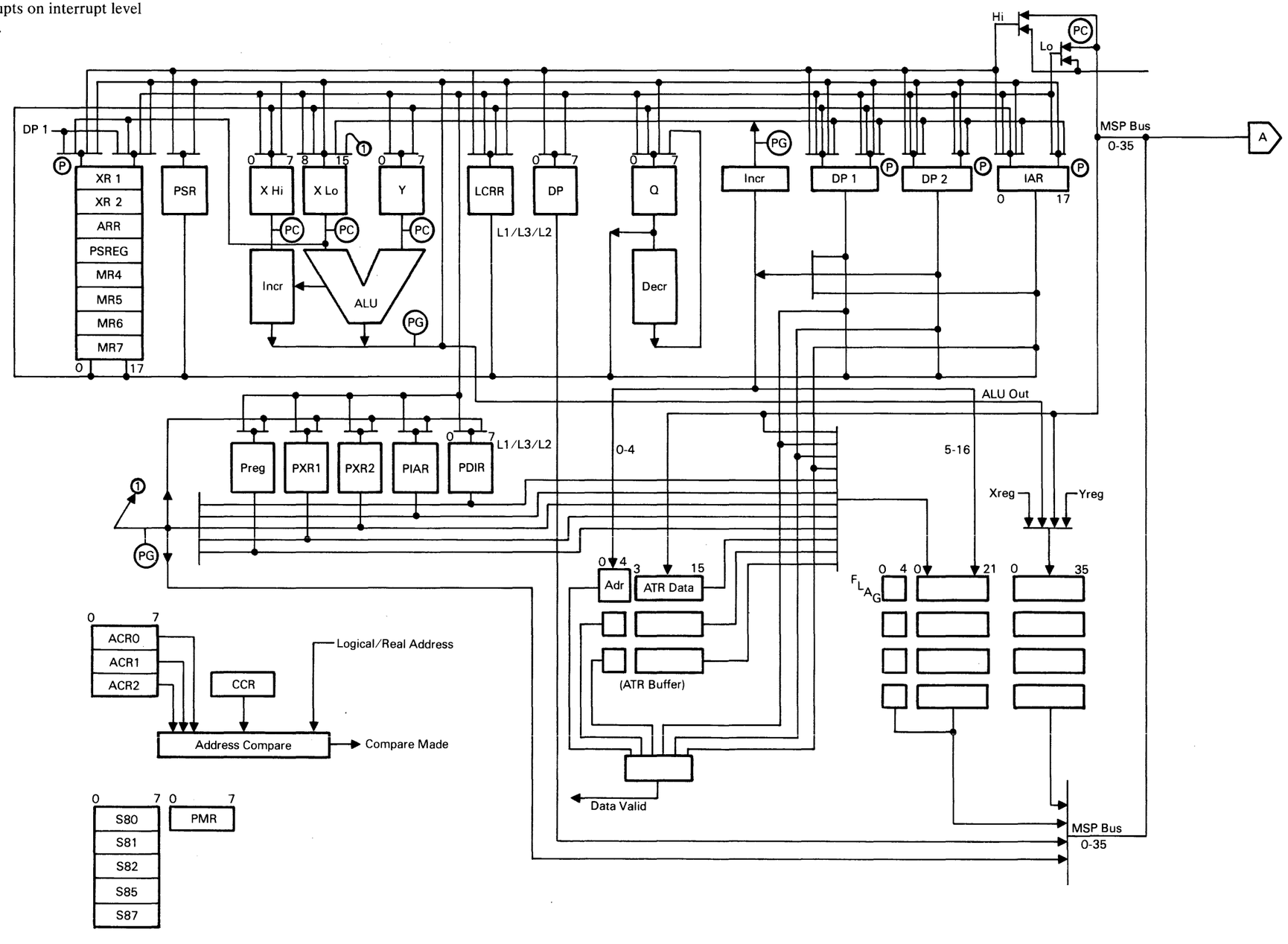
Control storage, which is part of the CSP card, contains logic to perform the following functions:

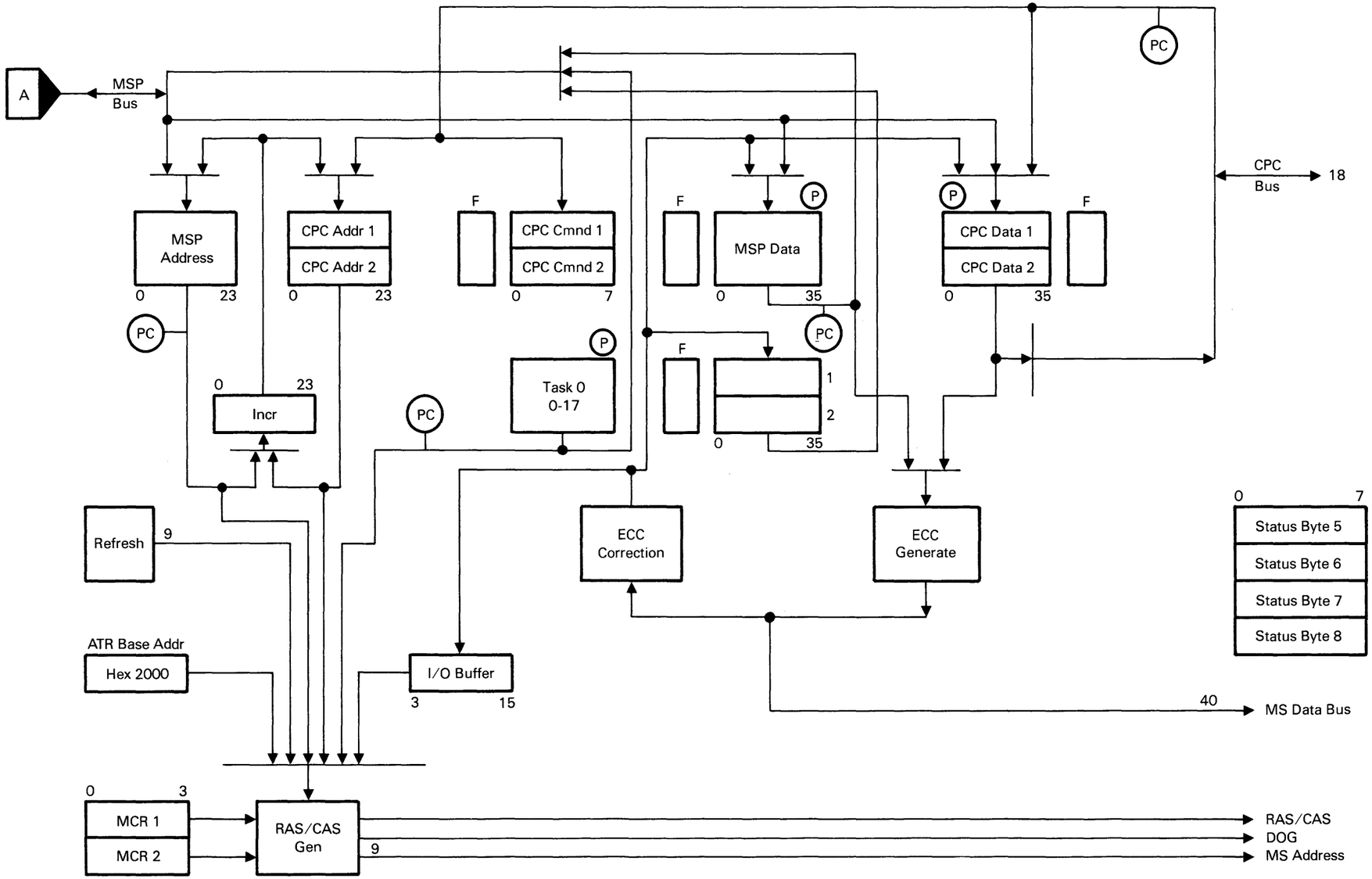
- Store up to 128K bytes of data plus the error correction code (ECC) in a matrix of 64K 22-bit words. Control storage stores 22 bits (16 data bits plus 6 ECC bits) during one write operation.
- Fetch data from the matrix as indicated by the CSP. Control storage fetches 22 bits (16 data bits plus 6 ECC bits) during one read operation.
- Generate a 6-bit error correction code and store it with the data in the 64K x 22-bit matrix.
- Use the 6-bit error correction code to detect and correct single-bit errors in any 16-bit word read from control storage.
- Use the 6-bit error correction code to detect multiple-bit errors in any 16-bit word read from control storage.



MAIN STORAGE PROCESSOR

The main storage processor (MSP) runs SSP routines and customer programs that are stored in main storage as indicated by the control programs running in the control storage processor (CSP). direct control over the CSP and must generate interrupts on interrupt level 5 to request service from the CSP.




A
MSP Bus
PC
CPC Bus
18
MSP Address
0
23
CPC Addr 1
CPC Addr 2
0
23
F
CPC Cmnd 1
CPC Cmnd 2
0
7
F
MSP Data
P
0
35
P
CPC Data 1
CPC Data 2
0
35
F
PC
PC
P
Task 0
0-17
F
1
2
0
35
0
23
Incr
PC
Refresh
9
ECC Correction
ECC Generate
0
7
Status Byte 5
Status Byte 6
Status Byte 7
Status Byte 8
ATR Base Addr
Hex 2000
I/O Buffer
3
15
40
MS Data Bus
0
3
MCR 1
MCR 2
RAS/CAS Gen
9
RAS/CAS
DOG
MS Address

10-650
MSP Card

ALU and Gating

The arithmetic and logic unit (ALU) can perform binary arithmetic, logic operations, and decimal addition and subtraction on operands in zoned decimal format. The ALU can operate on 1 byte of an operand at one time. Input data to the ALU comes from the X- and Y-registers. Output from the ALU can be sent back to the X-register, to main storage, or to any of the internal MSP registers. Gating circuits associated with the ALU also permit an increase or a decrease of a 2-byte address, or the addition of a 1-byte value (displacement) to a 2-byte address.

X-Register

The X-register is a 16-bit register that temporarily stores data or addresses for the ALU to operate on, or for transfer into the local storage registers or main storage. Input to the X-register is from the local storage registers or directly from main storage.

Y-Register

The Y-register is an 8-bit register that temporarily stores data for the ALU to operate on, or for transfer into the local storage registers or main storage. Input to the Y-register is from the local storage registers or directly from main storage.

OP Register

The OP (operation) register is an 8-bit register that holds the control byte of an MSP instruction when the instruction is fetched from main storage. The MSP control card uses the output from the OP register to control:

- Gate selection
- ALU functions
- Program status register (PSR) contents
- Local storage register address selection
- Processing unit clocks

A copy of the original contents of the OP register is stored in the OP byte in the local storage registers.

Q-Register

The Q-register is an 8-bit register. Its function is controlled by the contents of the OP register. The Q-register performs the following functions:

- Specifies the length of operands used in ALU operations
- Controls operations together with the OP register
- Selects registers to be changed or to be stored in main storage
- Selects the conditions in the program status register to be tested
- Holds register addresses or data to be loaded during MSP register sense and load operations

Because the contents of the Q-register can be changed when performing an instruction, a copy of the original contents of the Q-register is stored in the Q-byte in the LSRs.

Local Storage Registers

The local storage registers (LSRs) are a group of sixteen 2-byte registers that the MSP uses for data buffers and address registers. The values of these registers change with the program being performed in the MSP. The following chart describes the contents of each of the local storage registers.

Register	Contents
OP1	Operand 1 Address The logical address of operand 1 (before translation).
OP2	Operand 2 Address The logical address of operand 2 (before translation).
IAR	Instruction Address Register The logical address (before translation) of the next instruction to be performed in normal sequence by the MSP.
OP	Operation Byte A copy of the OP register (instruction control field) at the start of performing an instruction.
Q	Q-Byte A copy of the Q-register at the start of performing an instruction.
XR1	Index Register 1 A general-purpose index register.
XR2	Index Register 2 A general-purpose index register.
ARR	Address Recall Register A general work register that may contain the address of an earlier instruction.
LCRR	Length Count Recall Register An 8-bit register that contains the R-byte (third byte) of an operation that could not be performed.

Register	Contents
WR4	Work Register 4 A general-purpose work register.
WR5	Work Register 5 A general-purpose work register.
WR6	Work Register 6 A general-purpose work register.
WR7	Work Register 7 A general-purpose work register.
PSATR	ATR Storage Address The two low bytes of the storage address for the data to be loaded into the MSP registers, or for the MSP ATRs. The high byte of this address is in PATR.
PSREG	MSP Registers Storage Address The two low bytes of the storage address for the data to be loaded into the MSP registers, or for the MSP registers to be stored in. The high byte of this address is in PREG (one of the PACT registers).

Address Translation Registers

The address translation registers (ATRs) are a group of 248 registers. The MSP uses the ATRs to map storage addresses to different areas of storage for jobs running in the MSP. Eight PACT registers are used for real addressing of main storage (see 10-670). These registers are divided into groups, as follows:

System Address	Register Group
80-9F	Task address translation (group 1)
A0-A7	PACT registers
A8-BF	I/O ATR (group 1)
C0-DF	Task address translation (group 0)
E0-FF	I/O ATR (group 0)
100-11F	I/O ATR (group 2)
120-13F	I/O ATR (group 3)
140-15F	I/O ATR (group 4)
160-17F	I/O ATR (group 5)

The registers contain values that, when combined with the address in the MSAR, send the address to the area in storage assigned to the job now running in the MSP. If an ATR is loaded with a value of all 1's, the storage address is protected and no access can be made.

Main Storage Address Register

The main storage address register (MSAR) holds storage addresses during accesses to main storage. This register cannot be changed during a storage access. The MSAR can also select MSP registers for sensing and loading operations when it is loaded with the internal MSP address for the selected register. The contents of the MSAR cannot be sensed.

Buffer Compare Registers

The buffer compare registers (BCR) contain the storage address of the data contained in the data buffer on the storage card. These registers are loaded when a new block of data is loaded into the buffer. When the MSP makes an access to main storage, it compares the address with the contents of the buffer compare registers to determine if the data in the buffer can be used (to speed up the storage access). The address is divided into two buffer compare registers, as follows.

Bit(s)	Buffer Compare Register
13-15	BCR High Buffer compare register high
16-21	BCR Low Buffer compare register low

10-650 (continued)
MSP Card

Address Compare Registers

The address compare registers (ACR) contain a storage address of a location in storage. When the MSP makes a storage access, the MSP compares the storage address with the contents of the address compare registers and generates an address compare signal when the two addresses are the same. The address is divided into three address compare registers, as follows.

Bit(s)	Address Compare Register
0-7	ACR 0 Address compare register 0
8-15	ACR 1 Address compare register 1
16-23	ACR 2 Address compare register 2

Configuration Control Register

The configuration control register (CCR) contains information that defines how the address compare logic is used. The values in this register are controlled by the CSP.

Address Compare: Bits 0 through 3 determine when the address compare logic generates a compare pulse to the MSP control logic and to the CSP. These bits specify the processing unit operations during which the address compare logic can operate. The valid contents of bits 0 through 3 of the CCR and their meanings are as follows. Bits 4 through 7 of the CCR are not used.

Value (Hex)	Address Compare For
0	Real addressing (bits sent to storage cards) during MSP E- or I-cycle, or during CSP operation
1	Real addressing during MSP E- or I-cycle
2	Real addressing during MSP E-cycle or during CSP operation
3	Real addressing during MSP E-cycle
4	Real addressing during MSP I-cycle or during CSP operation
5	Real addressing during MSP I-cycle
6	Real addressing during CSP operation
7	Not used
8	Logical addressing during MSP E- or I-cycle, or during CSP operation
9	Logical addressing during MSP E- or I-cycle
A	Logical addressing during MSP E-cycle or during CSP operation
B	Logical addressing during MSP E-cycle
C	Logical addressing during MSP I-cycle or during CSP operation
D	Logical addressing during MSP I-cycle
E	Logical addressing during CSP operation
F	Not used

Note: *Logical address compare is done only when address translation is done. The comparison is done on the contents of the MSAR before translation.*

Program Mode Register

The program mode register (PMR) controls address translation for MSP accesses to main storage, and also protects the ATRs and PACT registers from change by programs that are not privileged. The PMR can be loaded by the CSP and also by the MSP when it is in privileged mode. See 10-568 for a description of the bits in the PMR.

MSP Status Registers

Status Byte 0

Status byte 0 (SB0) indicates the present condition of the MSP control logic. See 10-554 for a description of the bits in SB0.

Status Byte 1

The CSP loads status byte 1 (SB1) with a value that supplies control information to the MSP. The information in SB1 cannot be sensed.

Bit(s)	Description
0, 1	Not used
2	Reset not valid instruction latch
3	Reset MSP interrupt level 5 request
4	0 = Disable fast task save 1 = Enable fast task save
5	0 = Disable soft stop 1 = Enable soft stop
6	0 = Disable fast task load 1 = Enable fast task load
7	0 = Disable parity check run 1 = Enable parity check run

Status Byte 2

Status byte 2 (SB2) contains check and control information for the MSP. See 10-556 for a description of the bits in SB2.

Status Byte 4

Status byte 4 (SB4) contains flags for errors that occur during MSP operations or during CSP or channel accesses to MSP registers or main storage. Following a reset instruction or a system reset operation, SB4 is cleared to zero. See 10-558 for a description of the bits in SB4.

Status Byte 5

Status byte 5 (SB5) contains flags for errors that occur during MSP operations or during CSP or channel accesses to MSP registers or main storage. Following a reset instruction or a system reset operation, SB5 is cleared to zero. See 10-560 for a description of the bits in SB5.

Status Byte 6

Status byte 6 (SB6) controls some check and stop conditions of the MSP. The CSP sets or resets the bits in SB6. Following a reset instruction or a system reset operation, SB6 contains zero. The following chart describes the bits in SB6.

Bit(s)	Description
0	0 = Disable main storage address compare stop 1 = Enable main storage address compare stop
1	Reset main storage address compare stop
2	Check reset
3	0 = ECC mode not active 1 = ECC mode active
4	Enable single-bit storage error detection
5	Enable multiple-bit storage error detection
6	MSP parity check
7	CSP parity check

Status Byte 7

Status byte 7 (SB7) contains control information for the MSP. The following chart describes the bits in SB7.

Bit(s)	Description
0,1	Not used
2	0 = 2K page trap is not active 1 = 2K page trap is active
3	0 = Refresh rate is 7.0 μs 0 = Refresh rate is 15.0 μs
4	0 = Normal storage cycle 0 = Extend storage cycle
5	0 = Disable 256–512 register addressing 1 = Enable extended register addressing
6	0 = ECC bits from PATR (diagnostics) 1 = ECC bits from B 0000000 (diagnostics) This bit is used only when SB6, bit 3 is not active.
7	Not used

Status Byte 8

Status byte 8 (SB8) contains check information for the main storage processor. The following chart describes the bits in SB8.

Bit(s)	Description
0-4	Not used
5	MSP check
6	CSP check
7	SBA check

10-650 (continued)
MSP Card

Program Status Register

The program status register (PSR) is an 8-bit register that contains the conditions that are tested by branch on condition and jump on condition instructions. The contents of the PSR can be changed by:

- A system reset or power-on reset
- A reset MSP instruction from the CSP
- A load register instruction
- A register load from the CSP
- An add to register instruction
- An instruction that changes bits in the register

The following chart describes the bits in the register for instructions that use the PSR.

Instruction	PSR Bit	Description
Zero and add zoned decimal	7 6 5	Result is zero. Result is negative. Result is positive.
Add and subtract zoned decimal	7 6 5 4	Result is zero. Result is negative. Result is positive. Result overflow.
Edit	7 6 5	Operand 2 is zero. Operand 2 is negative. Operand 2 is positive (see note).
Compare logical characters	7 6 5	Operand 1 is equal to operand 2. Operand 1 is less than operand 2. Operand 1 is more than operand 2.
Compare or subtract logical immediate	7 6 5	Operand 1 is equal to immediate operand. Operand 1 is less than immediate operand. Operand 1 is more than immediate operand.
Add logical characters	7 6 5 2	Result is zero. Result is not zero with no carry. Result is not zero with a carry. Carry.
Subtract logical characters	7 6 5	Result is zero. Operand 1 is less than operand 2. Operand 1 is more than operand 2.
Subtract from register	7 6 5	Result is zero. Register is less than operand 1. Register is more than operand 1.
Add to register	7 6 5 2	Result is zero. Result is not zero with no carry. Result is not zero with a carry. Carry.
Test bits on	3	Test bits are not all ones.
Test bits off	3	Test bits are not all zeros.
Shift right character	7 6 5 2	Result is zero. Result is even and not zero. Result is odd-numbered. A 1-bit was moved out.
Branch or jump on condition		These instructions clear (set to zero) the bit tested (bit 3 or 4).
Load register (load PSR)	 7 6 5 4 3 2	Instruction bits 10-15 are: Bit 15 = 1 Bit 15 = 0 and bit 14 = 1 Bit 15 = 0 and bit 14 = 0 Bit 12 = 1 Bit 11 = 1 Bit 10 = 1
Reset MSP or system reset		This instruction sets the PSR to a value of hex 01.

Note: *PSR values for the edit instruction occur only under one of the following conditions:*

- *PSR bit 7 was set before the edit instruction was performed.*
- *The low-order byte of operand 1 is hex 20.*
- *Operand 2 is not zero.*

10-655
MSP Use of Addressing

Most addresses given in the instruction are for the location of the low-order (rightmost) byte of the field. Therefore, as the instruction is performed, the operand address register (OP1 or OP2 in LSR stack) is decreased to lower the main storage address. An exception is the ITC (insert and test characters) instruction, which is performed from the high-order byte to the low-order byte. In this case, the operand address register is increased in the same way that the instruction address register is increased during instruction fetch cycles.

The MSP uses one of two types of addressing when performing instructions: direct addressing or indexing.

Direct Addressing

Direct addressing needs a 2-byte address for each field selected by the instruction. This 2-byte address is loaded directly into the main storage address register (MSAR) to develop the address sent to the main storage cards (see 10-670).

Indexing

Indexing is a method for changing addresses in a program without changing the instruction. An indexed address is a single byte in the instruction. This single byte (displacement byte) is added to the contents of a 2-byte index register to form the operand address. This operand address is stored in the operand address register and is loaded into the MSAR to develop the address sent to the main storage cards (see 10-670).

Indexing is used to:

- Perform an instruction with an indexed address
- Add the index register to a constant
- Branch to an address to perform the instruction at a different storage location
- Perform an instruction or a series of instructions many times without using too many storage locations

Either of two index registers (XR1 or XR2) can be selected for indexing.

Sequential Instruction Operation

The MSP works step by step. Because of this, the instructions are stored in main storage using increasing addresses. The instruction address register stores the address of the storage location of the next instruction to maintain the sequence of the instructions. The MSP increases the instruction address register by 1 (or by 2 if the MSP reads 2 bytes at a time) as each instruction byte is read from storage to address the next higher storage location. This process continues until all the instruction bytes have been addressed. The instruction is then performed. After the instruction has been completed, the MSP uses the instruction address register to address the next instruction from storage.

Branching

Branching permits the MSP to change the instruction sequence under specific conditions. If the branch condition is met, the MSP places the address of the branch-to location (the target address) in the instruction address register. The target address then becomes the location of the next instruction to be performed. By branching to a different storage location and skipping some instructions, the operating sequence of the stored program is changed.

10-660
Instruction Formats

Each MSP instruction has an operation code (1 byte) and a Q-code (1 byte). These codes are followed either by a control code or by one or two addresses. The length of the instruction is from 3 bytes, for a control instruction or a one-address instruction with an indexed address, to 6 bytes, for a two-address instruction using direct addressing. The MSP performs three types of instructions:

- Two-address instructions
- One-address instructions
- Control instructions

Two-address instructions have two separate addresses that follow the Q-code in the instruction. The first address is the address of either the result field or the first operand. The second address is the address of the second operand. The first operand can be used as both a source field and a result field so that the first operand source field is changed when the result is written into it. The second operand is not changed except when the two operands overlap.

Most one-address instructions have only one field in main storage that contains an address (the load address instruction contains the needed data instead of an address).

Control instructions do not need main storage data fields and do not contain addresses.

The op code for each instruction changes with the type of addressing used. The following chart shows how the op code changes with the different types of addressing for each valid mnemonic of the MSP instruction set. See 10-430 for the MSP instruction set (in sequence by machine code) that shows the length of each instruction and the meaning of the Q-code. See 01-246 or 01-248 to display main storage.

		Op Code												
		Two-Address Instructions (Operand 1/Operand 2)									One Address			Control
Mnemonic	Function	Direct/ Direct	Direct/ XR1	Direct/ XR2	XR1/ Direct	XR1/ XR1	XR1/ XR2	XR2/ Direct	XR2/ XR1	XR2/ XR2	Direct	XR1	XR2	
A	Add to register										36	76	B6	
ALC	Add logical characters	0E	1E	2E	4E	5E	6E	8E	9E	AE				
AZ	Add zoned decimal	06	16	26	46	56	66	86	96	A6				
BC	Branch on condition										C0	D0	E0	
BC	Branch on ARR													F0
CLC	Compare logical characters	0D	1D	2D	4D	5D	6D	8D	9D	AD				
CLI	Compare logical immediate										3D	7D	BD	
ED	Edit	0A	1A	2A	4A	5A	6A	8A	9A	AA				
ITC JC	Insert and test characters Jump backward	0B	1B	2B	4B	5B	6B	8B	9B	AB				F1
JC	Jump on condition													F2
L	Load register										35	75	B5	
LA	Load address										C2	D2	E2	
LPMR	Load program mode register													F6
MVC	Move characters	0C	1C	2C	4C	5C	6C	8C	9C	AC				
MVI	Move logical immediate										3C	7C	BC	
MVX	Move hex characters	08	18	28	48	58	68	88	98	A8				
S	Subtract from register										37	77	B7	
SBF	Set bits off masked										3B	7B	BB	
SBN	Set bits on masked										3A	7A	BA	
SLC	Subtract logical characters	0F	1F	2F	4F	5F	6F	8F	9F	AF				
SLI	Subtract logical immediate										3F	7F	BF	
SRC	Shift right character										3E	7E	BE	
ST	Store register										34	74	B4	
SVC	Supervisor call													F4
SZ	Subtract zoned decimal	07	17	27	47	57	67	87	97	A7				
TBF	Test bits off masked										39	79	B9	
TBN	Test bits on masked										38	78	B8	
XFER	Transfer control													F5
ZAZ	Zero and add zoned decimal	04	14	24	44	54	64	84	94	A4				

10-670
Main Storage Addressing

The MSP uses two types of main storage addressing: translated addressing and real addressing. The methods that the MSP uses to perform translated and real addressing are the same whether the CSP, MSP, or SBA is making the main storage access. However, the MSP must determine whether to perform translation or not. So, the MSP performs main storage addressing in three steps:

1. Determines the type of addressing to use (translated or real)
2. Generates the address
3. Sends the address bits to the main storage card

Type of Addressing

During CSP accesses to main storage, all I/O cycle steals are done using translated addressing. I/O devices may cycle steal only to or from I/O address translation registers (ATRs) and main storage. When the MSP performs address translation, bit 3 of the command byte is on.

During MSP accesses to main storage, bits 3 through 6 of the program mode register (PMR) control address translation. The status of these bits is based on the type of MSP cycle being performed.

During SBA accesses to main storage, the MSP uses real addressing. When the MSP performs real addressing, bit 3 of the command byte is off.

Translated Addressing Mode

To use translated addressing for MSP operations, the most significant bit of the PACT registers is on. Bit 3 of the command byte is on for CSP operations. For both of these types of operations, the ATRs are used to generate the translated address.

The ATRs contain information that permits main storage address translation by 2K address blocks. Each ATR has 16 bits, but bits 0 through 2 are not valid. If one or more of bits 0 through 2 are on when the ATR is used, a storage exception check occurs.

Real Addressing Mode

Prefix address contained translation (PACT) registers store the most significant bit of an address. When this bit is off, the MSP uses the PACT registers to form the real address.

Bit 0 of PACT registers PIAR, PDIR, PXR1, and PXR2 is set into the program mode register. This bit controls whether the address will be translated or not. If the address will not be translated, the PACT registers are mapped directly into the real storage address. They are ignored in translated mode.

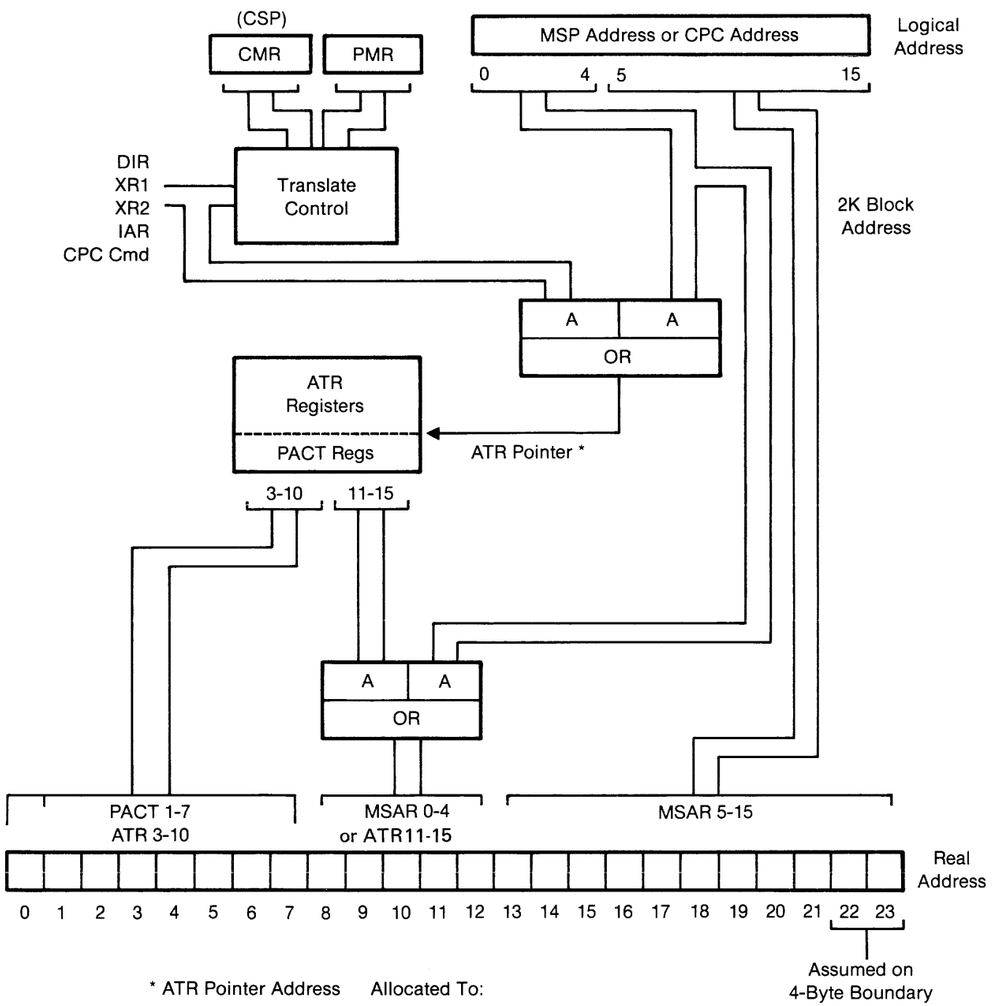
The MSP fast task switching logic uses PACT registers PATR and PREG to determine one of the following:

- The 64K section of real storage in which to save the present task registers
- The 64K section of real storage from which to fetch the next task registers

These registers have no translate bit, and when they are used, real addressing is used.

MSP Addressing of Main Storage

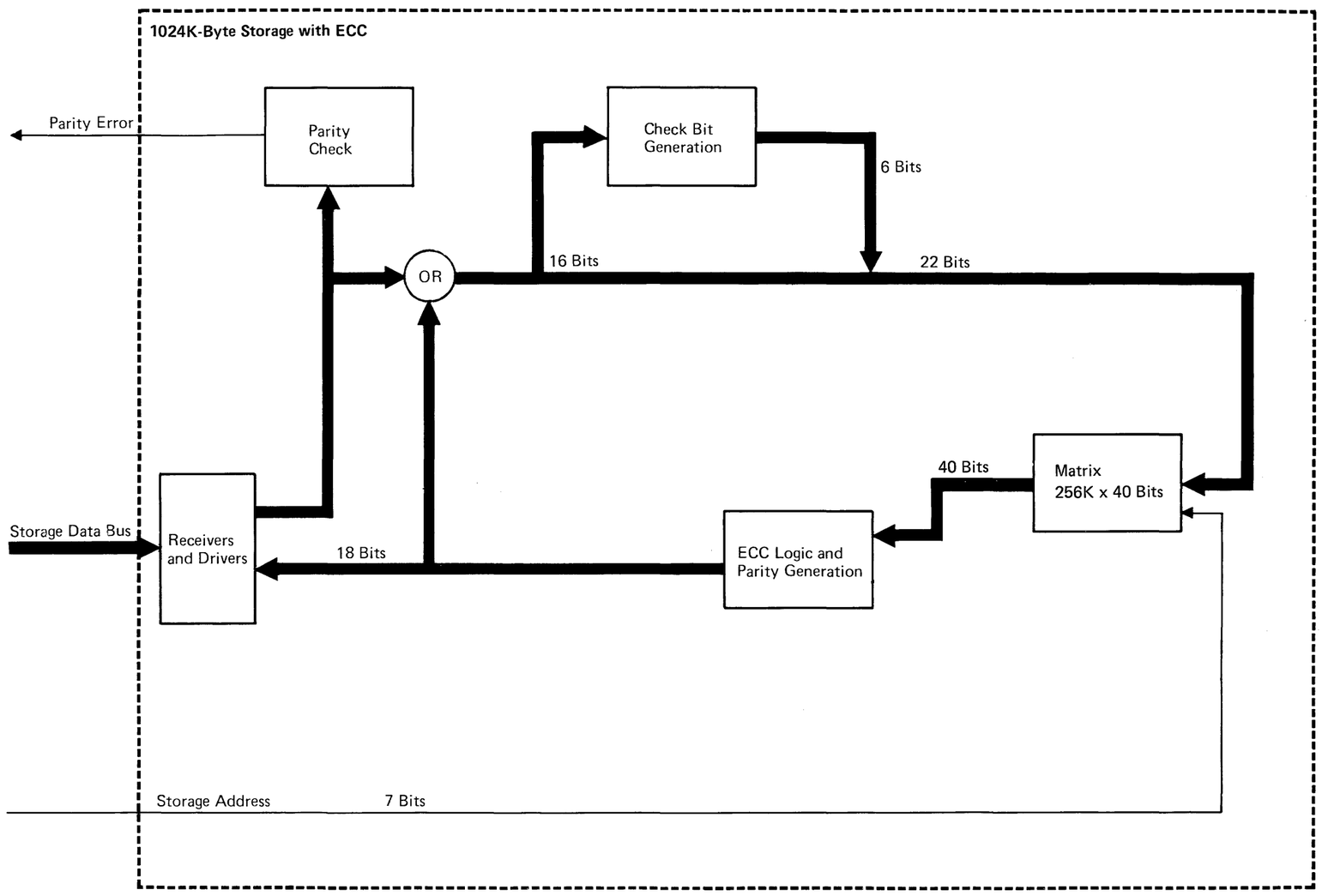
Note: *When main storage cards of different types are installed, they are addressed as if each was equal to the largest.*



* ATR Pointer Address	Allocated To:
80 - 9F	Task ATR (Group 1)
A0 - A7	PACT Registers
	A0 PDIR
	A1 PXR1
	A2 PXR2
	A3 PIAR
	A4 PREG
	A5 PATR
	A6 RSVD
	A7 PCSP
A8 - BF	I-0 ATRs 40-63
C0 - DF	Task ATR (Group 0)
E0 - FF	I-0 ATRs 0-31

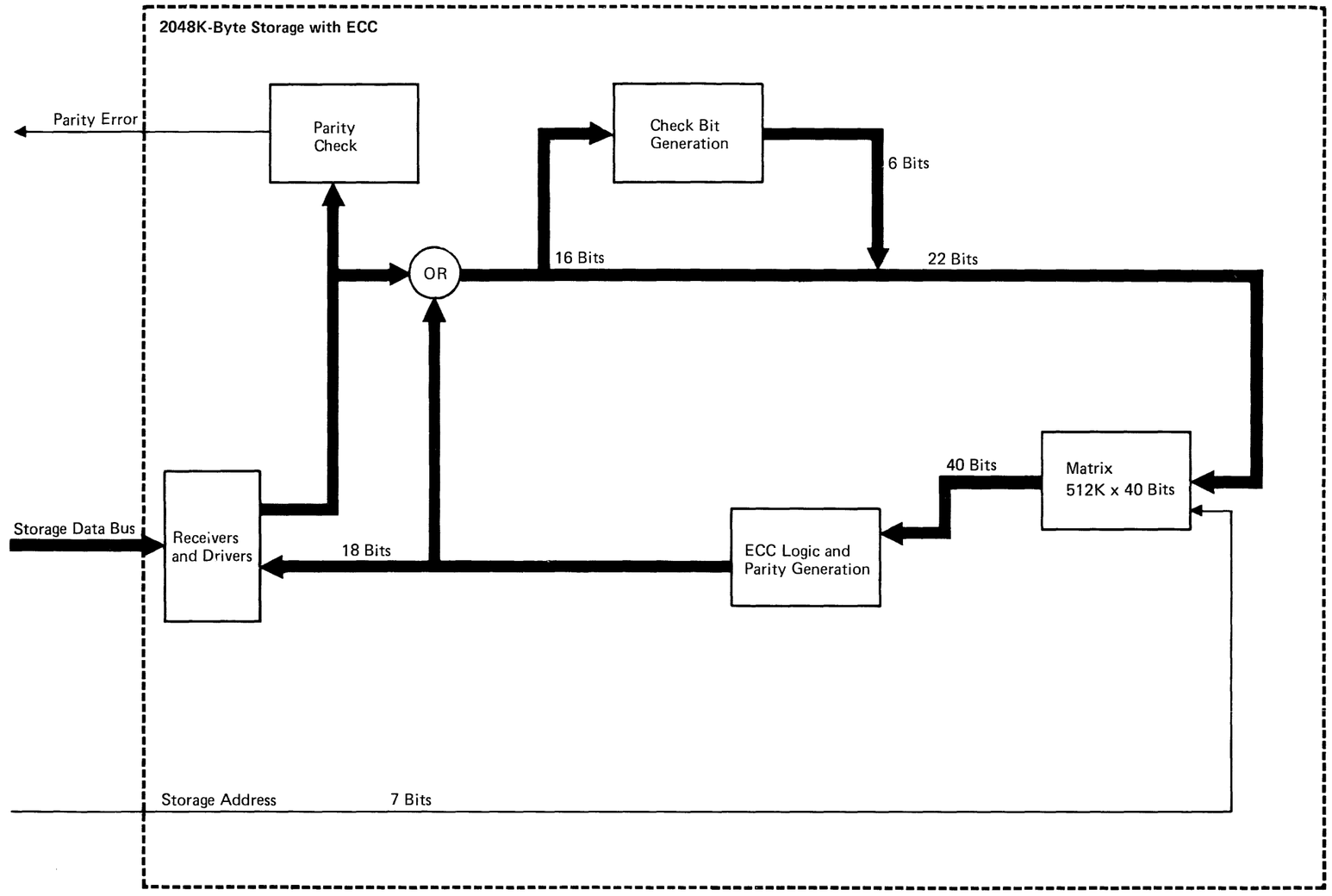
1024K-Byte Storage Card with ECC

The 1024K-byte storage card with ECC is a 4-wide, 3-high card that contains no logic to perform data storage. This storage card receives an RAS address, a CAS address, a write/read control line, and data. It can store up to 1024K bytes of data (plus error correction code) in a matrix that has 512K 40-bit words. The card writes or reads 40 bits (32 data bits plus 7 ECC bits and 1 redundant bit) during one operation.



2048K-Byte Storage Card with ECC

The 2048K-byte storage card with ECC is a 4-wide, 3-high card that contains no logic to perform data storage. This storage card receives an RAS address, a CAS address, a write/read control line, and data. It can store up to 2048K bytes of data (plus error correction code) in a matrix that has 1024K 40-bit words. The card writes or reads 40 bits (32 data bits plus 7 ECC bits and 1 redundant bit) during one operation.



10-680
Control Panel Interface Card

The control panel interface card is a 2-wide, 3-high card in the A-A1 board that connects to the control panel through a flat cable, and to the CSP through two top card connectors. The logic on this card is the interface between the CSP and the control panel; it also controls most of the functions of the panel. The functions of the control panel interface card include:

- Sensing when a key is pressed
- Removing the key contact bounce from the signal
- Interpreting the functions of the keys
- Passing data to and from the CSP
- Passing data, status, and operations to and from the control panel
- Controlling the hexadecimal display
- Controlling the LEDs on the control panel (except power check, temperature check, power on, and the eight communications and power LEDs)
- Receiving and driving the signals that enter and leave the card
- Performing the following each time the system is powered on:
  - A self-test
  - A test of its interface with the CSP
- Performing the following each time the Load key is pressed:
  - Error recording, if needed (to save the status of the CSP registers and control storage LSRs)
  - A test of its interface with the CSP
  - Loading the CSP self-test into control storage and starting the CSP
  - A hardware IPL from the correct load device (when the CSP self-test ends correctly) and starting the CSP
- Performing CSP instructions that use the control panel
- Performing parity checking on data it receives from the CSP

10-685
Control Panel Driver Board

The control panel driver board is behind the control panel. The board has four cables that connect it to:

- The control panel interface card (through the A-A1 board)
- The A-A1 board if SLCA is installed, or the A-A3 board if MLCA is installed
- The protect card
- The Security switch

Also, three edge connectors connect the driver board to the display board.

The driver board contains logic to perform the following functions:

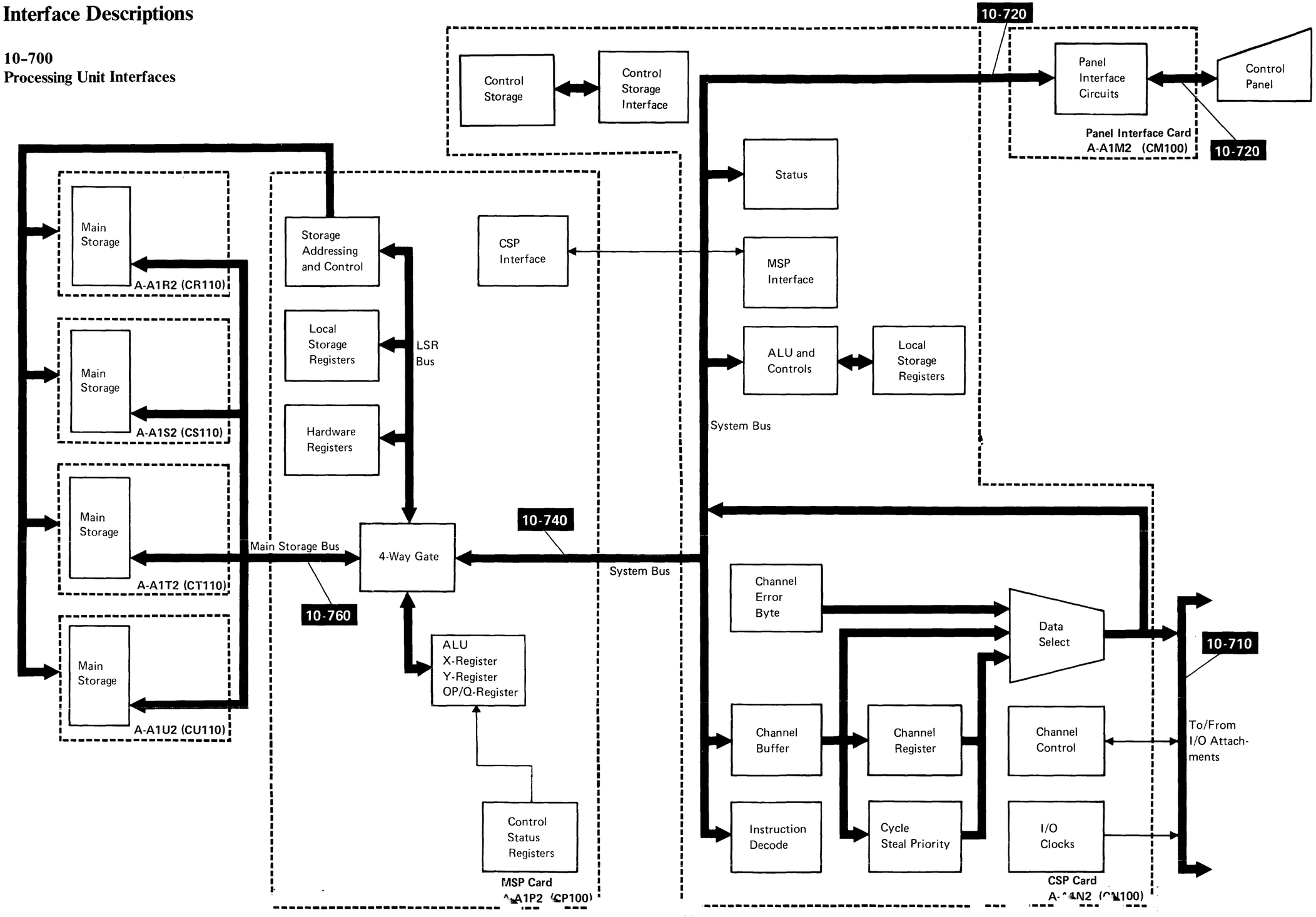
- Drive the LEDs and displays on the control panel
- Store data to be displayed on the control panel
- Control circuits to gate the data to the correct area for display on the control panel

10-690
Control Panel Display Board

The control panel display board contains the input keys, the output displays, and the LEDs that let the user enter and read data on the control panel. The board contains no control logic.

Interface Descriptions

10-700
Processing Unit Interfaces



Channel Interface Output Signals

Signal Name	Description
−Bi-di DBI/DBO hi byte (PH, 0-7)	This bus contains data from the attachment to the channel interface during I/O sense and I/O control sense instructions, and during single-byte base cycle steal operations. During 2-byte data transfers, this bus combines with the bi-di lo byte bus to form a bidirectional data path that is 18 bits wide.
−Bi-di DBI/DBO lo byte (PL, 8-15)	This bus contains data from the channel interface to the attachment during I/O load and I/O control load instructions, and during single-byte base cycle steal operations. During 2-byte data transfers, this bus combines with the bi-di hi byte bus to form a bidirectional data path that is 18 bits wide.
−Burst or I/O strobe	This signal supplies timing for synchronous data transfer between the channel interface and the attachment controller.
−Busy to cycle steal	This signal indicates to the attachment controller that the system is operating at a higher priority than the priority assigned to steal (machine check).
−Chan CSIPL diskette (from control panel)	When active, this signal selects the diskette for use during system initial program load. When not active, this signal selects the disk.
−Encoded comm select bits (0-3) (from control panel)	These four signals select one of the four possible communication lines to be displayed on the control panel. Only one of these signals can be active at any one time. • Bit 0 selects line 1 • Bit 1 selects line 2 • Bit 2 selects line 3 • Bit 3 selects line 4
−Control out	When active, this signal indicates to the attachment that the CBO bus contains information to specify either a cycle steal or an I/O instruction. This signal can also be activated together with the '−service out' signal to force all attachments off the channel.
−CBO bits (chan) (0-2) (command bus out)	These signals, together with the '−control out' and '−service out' signals, indicate the type of data that is on data bus out. The decode for these signals is as follows: 0 0 0 = Sense cycle steal identification Requests the attachment that is requesting a cycle steal operation to put its device ID on the bi-di data bus. 0 0 1 = Sense interrupt status Requests the attachment that is requesting service on an interrupt level to put its device ID on the bi-di data bus. 0 1 0 = Cycle steal acknowledge Indicates that the channel is permitting an attachment request for a cycle steal. 0 1 1 = JIO branch The CSP microcode branches if the attachment responds with tag bus in, bit 4. 1 0 0 = IOL (load) The bi-di output bus contains data from the CSP local storage registers or from control storage or main storage for the attachment. 1 0 1 = IOS (sense) Data is taken from the bi-di input bus and placed in one of the CSP local storage registers, in control storage, or in main storage. 1 1 0 = IOCL (control load) The bi-di output bus contains data from the CSP local storage registers to be used as control information by the attachment. 1 1 1 = IOCS (control sense) The bi-di input bus contains control or status information to be placed in the CSP local storage registers.
−Data protect (from protect card)	This signal is active during power-on and power-off operations. Attachments can use this signal to protect data or hardware during unstable power conditions.
−IMPL cycle to I/O (chan) (from CSP)	This signal starts a control storage initial program load sequence. The condition of the '−chan CSIPL diskette' signal determines if the disk or the diskette supplies the information for the load.

Signal Name	Description
+Mach chk to I/O (chan) (from CSP)	This signal indicates to the attachment that the CSP detected a processor check or channel check condition.
+Power on reset and −power on reset (from protect card)	These signals are active as long as the system is powered off. When the system is powered on, these signals remain active for approximately 2 seconds to set the channel and attachment circuits to an initial condition.
−Service out	Input Operation (data from the attachment to the channel) This signal indicates to the attachment that the data on the bi-di input bus has been recognized and the attachment can either present new data or terminate the transfer. Output Operation (data from the channel to the attachment) This signal indicates to the attachment that the data on the bi-di output bus is valid and can be sensed. This signal remains active as long as the data on the output bus is valid. Cycle Steal This signal remains active during all of the operation. Each data byte is transferred by activating the '−burst or I/O strobe' signal.
+System reset (chan) from control panel interface card	When active, this signal indicates to the attachment that it should set its circuits to an initial condition. This signal is generated by pressing either the System Reset key or the Load key on the control panel, or during a power-on operation.
+Wait state (from CSP)	This signal indicates that the CSP is in a wait condition during cycle steal operations.
+100 ns clock	100-nanosecond clock to attachments.
+512 μs clock	512-microsecond clock to attachments.
+1.02 ms clock	1024-microsecond clock to attachments.
+131.1 ms clock	131 072-microsecond clock to attachments.
+1 sec clock	1 048 000-microsecond clock to attachments.

Channel Interface Input Signals

Signal Name	Description
−ARS bus 3, 4, 5, 6, 7 (address register select)	These five signals are encoded with a value that selects the interrupt level work register that contains the base address to be used during a cycle steal operation.
−Communications indicators (9 signals)	These signals permit the communications attachment to display status information on the control panel.
−Cycle steal burst data request	This signal is activated by the attachment to start a multiple-byte cycle steal operation.
−Cycle steal req (new)	This signal is activated by an attachment to request a cycle steal operation. It turns off during '−service in' of the cycle steal.
−Microinterrupt req (2, 3, 4)	These signals carry interrupt requests from the attachments to the indicated interrupt levels of the CSP (2, 3 or 4). An active interrupt request indicates to the CSP that an attachment on that level needs service. The CSP resets the interrupt request with an I/O immediate command after it responds to the interrupting attachment.
+Multidevice response	When active, this signal indicates that all attachments have responded to a multidevice command (CBO = 001).
−Printer on (remote on)	The line printer activates this signal to the channel to turn on +24 Vdc to the line printer hammer drivers.
−Service in	This signal indicates to the channel that the attachment has received a command byte from the channel. If a response is needed from the attachment, this signal also indicates that the response will be available at the correct time.
−Tag bus in 0	This signal controls the selection of either a high or low byte during 1-byte base cycle steal operations that transfer data into either control storage or the CSP local storage registers. This signal is ignored for 2-byte transfers, or for transfers to main storage. When active, this signal selects the low byte and adds one to the storage address; when not active, this signal selects the high byte and the storage address is not changed.
−Tag bus in 1	This signal determines the direction of the data transfer during all cycle steal operations. When this signal is active, the transfer is from the channel to the attachment; when this signal is not active, the transfer is from the attachment to the channel.

Note: *The −ARS bus 5, 6, and 7 and −tag bus in 1 signals can be tested with IPL diagnostic routines (10-400). Other channel signals cannot be checked using the diagnostic routines.*

Signal Name	Description
−Tag bus in 3	This signal, together with '−tag bus bit 4', determines the register to be used in a transfer to or from one of the processing unit registers. If this signal is not active, the transfer uses a storage location. If this signal is active, the transfer uses a register in either the CSP or the MSP as determined by bit 4.
−Tag bus in 4	Cycle Steal This signal determines the destination of the data transfer. When this signal is active, a CSP register or control storage is used; when this signal is not active, an MSP register or main storage is used. I/O Sense When active, this signal indicates that the attachment did not supply good parity on the bi-di input bus. Jump I/O When active, this signal indicates that the attachment found the tested condition (the CSP will take the jump in the control program).
−Tag bus in 5	When active, this signal indicates that the attachment sensed bad parity on the bi-di output bus.
−Tag bus in 6	When active, this signal indicates that the attachment is using the 2-byte wide transfer mode of the channel (both bytes of the bi-di bus carry data in the same direction).

10-720
CSP to Control Panel

CSP to/from Control Panel Interface Card

Signal Name	Description
−System bus	This signal is an 18-bit bidirectional bus that carries data and addresses between the CSP and the control panel interface card.
−PCB (processor control bus)	This is a 4-signal bus that controls start, stop, and reset functions of the CSP.
−PCB strobe	This signal synchronizes PCB commands to the CSP.
−OLB (operating level bits)	These bits are a 3-bit bus that indicates the present operating (interrupt) level of the CSP.
−Processor check	This signal indicates the present operating condition of the CSP.
−CSP active	This signal indicates the present state of the CSP.
−CSP check	This signal indicates that the CSP detected a check; the signal is active for a minimum of 100 nanoseconds.

10-720

Control Panel Interface Card to/from Control Panel

Signal Name	Description
−Addressed key pressed	When active, this signal indicates that the key that is being addressed is in the active state (is pressed).
−Bi-di panel interface bus (0-3)	This bidirectional bus carries data for one of three functions: • Data to drive the hexadecimal display • Data to turn the LEDs on or off • Communications line select data from the control panel
+Degate display segments	When active, this signal inhibits the hexadecimal display from receiving data, so that the '+panel adr/data bits' signal can be used to control the LEDs.
+Key address bits (0-4)	These bits select a key on the control panel. When that key is addressed, the control panel logic checks to see if the key is pressed.
−Lamp test	When active, this signal turns on all LEDs and shows all 8s in the hexadecimal display.
−Power key	When active, this signal indicates that the Power key on the control panel has been pressed. If mode 6 is selected (enable power off), the panel interface card generates the '−power off' signal to the protect card.
−Power off	When active, this signal requests the protect card to turn off system power. This signal can be generated by: • An I/O immediate instruction from the CSP • Pressing the Power key on the control panel when in mode 6 (enable power off)
−Panel strobe	This signal clocks data into the panel data latches when the data is not changing.
+Select bus bits (0-2)	This 3-bit bus carries data for one of two functions: • To select one of the 4 hexadecimal display characters to receive data • To select one of two groups of eight LEDs to receive data
−Storage unlock	This signal enables control panel operations that permit the user to display or change storage.

10-740
CSP to MSP

The following tables describe the signals between the CSP and the MSP. The reference column contains a diagnostic test unit (TU) number that you can loop on while checking the signal.

Bidirectional Signals

Signal Name	Description	Reference
+Bi-di system bus hi byte	+External System Bus High This is an 8-bit bidirectional bus (plus parity/bit) that is the high-byte path (bits 0-7) for the following data: • The 2-byte main storage address when using main storage (CSP or cycle steal to main storage) • A 2-byte data transfer to/from main storage or an MSP register (from either CSP or cycle steal) • The address of an MSP register when the CSP is using an MSP register; this byte is not used but must have good parity (only the low byte is used)	T20E9*
+Bi-di system bus lo byte	+External System Bus Low This is an 8-bit bidirectional bus (plus parity bit) that is the low-byte path (bits 8-15) for the following data: • The 2-byte main storage address when using main storage (CSP or cycle steal to main storage) • A 2-byte data transfer to/from main storage or an MSP register (from either CSP or cycle steal) • The address of an MSP register when the CSP is using an MSP register • The data path during all 1-byte operations between main storage or an MSP register and the CSP	T20E9*

* A failure in this signal can cause a system failure during IPL, so that you cannot load the diagnostic control program.

CSP to MSP Interface Signals

Signal Name	Description	Reference
–Allow MSP run	When active, this signal permits the MSP clocks to run unless they are interrupted by the '–temp stop request' signal. This signal is activated by the CSP when it performs a start MSP instruction; it is removed when: • The 'stop' latch in the CSP is activated. • The system is in MSP instruction step mode. • The CSP sets the 'I/O service request' latch. The signal is also removed when the MSP stops and activates the '–interrupt level 5 request' signal because of an MSP check, an address compare stop, or a supervisor call.	T20B6
–Clock MSAR/-Stg function from CSP	These two signals define the parts of an MSP/main storage access by the CSP as follows: • When both signals are not active, no access is occurring. • When the '–clock MSAR' signal is active and the '–stg function from CSP' signal is not active, the command/PCSP part of the access is occurring. • When both signals are active, the address part of the access is occurring. • When the '–clock MSAR' signal is not active and the '–stg function from CSP' signal is active, the data part of the access is occurring.	T20E9
–Reset MSP	This signal stops the MSP clocks and resets the MSP registers. It is activated during power-on reset, when the System Reset key is pressed, or if the CSP performs a reset MSP command. The MSP clocks are active during the reset operation. At the end of the operation, the clocks are stopped until the CSP activates the '–allow MSP run' signal.	T20E3
–Temp stop request	This signal stops the MSP at a point that will not affect the result of its instruction sequence. This signal is activated for the following operations: • Machine check interrupt in the CSP • CSP is stopped • At the direction of the CSP microcode program	T20E9
–Two-byte op to MSP	When active, this signal indicates that the present data transfer to or from main storage (or MSP registers) is a 2-byte wide transfer.	T20E9

MSP to CSP Interface Signals

Signal Name	Description	Reference
–Interrupt level 5 request	When active, this signal indicates to the CSP that the MSP needs service from the CSP. This signal occurs when the '–reset MSP' signal is active or when an MSP check condition occurs. It can also occur when one of the following internal conditions occurs in the MSP while the MSP is performing an instruction: • Instruction step mode • An operation that cannot be performed • Main storage address compare stop The CSP can reset this signal either by activating the '–allow MSP run' signal, or by resetting the interrupt level 5 request bit by loading MSP status byte 1.	T20B6
–MS address compare	This signal indicates that a main storage address compare has occurred. When in main storage address compare stop mode, this signal sets the main storage address compare bit in MSP status byte 2 when the address compare occurs.	T20D7
–MSP check	This signal indicates that a check condition has occurred during the present data transfer. The type of check can be determined from MSP status bytes 4 (10-558) and 5 (10-560).	T20E9
–MSP buffer ready	For a write operation, this signal indicates that data has been received from the CSP. For a read operation, this signal indicates that data is ready to be transferred to the CSP.	T20E9

1024K-Byte Storage Card with ECC

The following tables describe the signals between the MSP and main storage. The reference column contains a diagnostic test unit (TU) number that you can loop on while checking the signal.

MSP to Main Storage

Signal Name	Description	Reference
−MS address bit 0-8	This address bus selects one of the locations on the main storage card to be used for the present operation.	T20E9
−MS read/+write	When minus, this signal indicates that the present main storage operation is a read operation. When plus, this signal indicates that the present main storage operation is a write operation.	T20E9
−RAS	When this signal is active, the storage modules contain the RAS address.	T20E9
−CAS	When this signal is active, the storage modules contain the CAS address.	T20E9
−Data out gate	When this signal is active, the output drivers of the storage card are activated.	T20E9
−Bank select	This signal controls the '-RAS' and '-data out gate' signals. When this signal is active, the '-RAS' and '-data out gate' signals control the storage card.	T20E9
−Data latch	When this signal is active, data at the storage card input drivers will be latched during a write operation.	None

Bidirectional MSP/Main Storage Signals

Signal Name	Description	Reference
+Bi-di MS bus 0-39	This is a 40-bit bidirectional data bus (32 data bits, 7 ECC bits, and 1 redundant bit) that transfers data between the MSP and main storage during main storage read and write operations.	T20E9

2048K-Byte Storage Card with ECC

The following tables describe the signals between the MSP and main storage. The reference column contains a diagnostic test unit (TU) number that you can loop on while checking the signal.

MSP to Main Storage

Signal Name	Description	Reference
−MS address bit 0-8	This address bus selects one of the locations on the main storage card to be used for the present operation.	T20E9
−MS read/+write	When minus, this signal indicates that the present main storage operation is a read operation. When plus, this signal indicates that the present main storage operation is a write operation.	T20E9
−RAS	When this signal is active, the storage modules contain the RAS address.	T20E9
−CAS	When this signal is active, the storage modules contain the CAS address.	T20E9
−Data out gate	When this signal is active, the output drivers of the storage card are activated.	T20E9
−Bank select	This signal controls the '-RAS' and '-data out gate' signals. When this signal is active, the '-RAS' and '-data out gate' signals control the storage card.	T20E9
−Data latch	When this signal is active, data at the storage card input drivers will be latched during a write operation.	None

Bidirectional MSP/Main Storage Signals

Signal Name	Description	Reference
+Bi-di MS bus 0-39	This is a 40-bit bidirectional data bus (32 data bits, 7 ECC bits, and 1 redundant bit) that transfers data between the MSP and main storage during main storage read and write operations.	T20E9

Sequence of Events

10-810
Initial Program Load

During the initial program load (IPL), the channel can load the CSP microcode and the MSP support programs from either disk or diskette as determined by the mode selected on the control panel, as follows:

- Mode 0: Loads the system from disk.
- Mode E: Loads the system from diskette. This mode is used for loading diagnostic programs from diskette.
- Mode F: Loads the system from disk or diskette. A selected load option determines the load function (see 01-140).

Loading control storage (CSIPL) is a hardware-controlled function that is started by pressing the Load key on the control panel. Loading main storage (MSIPL) and attachment controller microcode storage is controlled by the CSP and starts immediately following CSIPL. The following table shows the major events that occur during the initial starting of the system.

Control Panel Interface Card	Control Storage Processor	Data Storage Attachment
1 The operator presses the Load key (control panel). Hex FFFF appears on the display.		
	2 Turns off the '–CSP active' signal and disables cycle steals.	
3 Performs error recording, if needed.		
4 Performs a processor control bit (PCB) reset. This resets the main level MAR, ILBB, PEB, CEB, channel register, and ECC error byte.		
5 Loads control storage with the CSP self-test routines.		
6 Sends a CSP start command to the CSP.		
	7 Performs the CSP self-test.	
	8 Sends the hardware IPL command to the control panel interface card when the self-test ends successfully.	
9 Performs a system reset.		
10 Sends the '–IMPL cycle' signal to the data storage attachment.		
		11 Starts the B and C clocks.
		12 Load from disk: Generates the '–IPL disk A' signal to the first disk drive. Load from diskette: Generates the '–IPL dskt' signal to the diskette drive.
		13 The storage device performs its IPL sequence: • 10SR (10-811) • 51TD (10-813) • 72MD (10-814)

Control Panel Interface Card	Control Storage Processor	Data Storage Attachment
		14 Performs a read data operation.
		15 Starts a cycle steal to transfer data from the data storage attachment to control storage starting at location 0000.
16 Senses that 4096 bytes have been transferred to control storage.		
17 Deactivates the '−IMPL cycle' signal.		
		18 Deactivates either the '−IPL disk A' signal or the '−IPL dskt' signal.
19 Sends a PCB reset CSP command to the CSP.		
20 Sends a PCB start command to the CSP.		
21 Removes hex FFFF from the control panel display.		
	22 Starts operating from control storage location 0000 (see 10-400).	
	23 Control storage microcode loads main storage with the support programs to permit the operator to communicate with the system.	

10-811
10SR Attachment IPL

Adapter Card	10SR Disk Drive
1 Senses an active level on the '–disk/dskt reset' signal.	
2 Senses an active level on the '–IPL disk A' signal.	
3 Generates a read data command for 16 records starting with logical record 0 (cylinder 0, head 0).	
	4 Accesses cylinder 0 (97-820).
	5 Selects head 0 (97-824).
	6 Reads 16 records, starting with logical record 0, and sends them to the system (see 90-835, starting with step 4).
7 Return to the channel IPL sequence (10-810).	

10-813
51TD Attachment IPL

Adapter Card	51TD Diskette Drive
1 Senses an active level on the '–power-on reset' signal.	
2 Senses an active level on the '–IPL dskt' signal.	
3 Issues a sequence of commands to perform an IPL read operation.	
	4 Performs a recalibrate (91-861).
	5 Performs a load heads command (91-851).
	6 Reads data starting at cylinder 0, head 0, sector 1.
7 Return to the channel IPL sequence (10-810).	

10-814
72MD Attachment IPL

Adapter Card	72MD Diskette Magazine Drive
1 Senses an active level on the '–power-on reset' signal.	
2 Senses an active level on the '–IPL dskt' signal.	
3 Issues a sequence of commands to perform an IPL read operation.	
	4 Performs an orient command (93-852).
	5 Performs a select magazine 1, slot 1 command. If no diskette is present, a select I/O slot 1 command is performed (93-853).
	6 Performs a recalibrate (93-861).
	7 Performs a load heads command (93-854).
	8 Reads data starting at cylinder 0, head 0, sector 1.
9 Stops the read operation when the '–IPL dskt' signal goes not active.	
10 Return to the channel IPL sequence (10-810).	

10-820
General I/O Operation

Input/output (I/O) operations are started by a program running in the MSP. These operations are used to:

- Write data to disk or diskette storage
- Read data from disk or diskette storage
- Print data on a printer
- Display data on a display
- Transfer data over the data communications line(s)

For the program to operate, it must be loaded into main storage. The following chart shows the major events that occur during a sample I/O operation. See the attachment Maintenance Information Manuals for details concerning I/O operations.

MSP CSP/Channel	Attachment	
1 Customer program calls SSP to read or write data.		
2 SSP issues SVC for I/O service to CSP.		
	3 CSP calls its I/O control handler routine (IOCH).	
	4 IOCH analyzes the operation and sets up data addresses.	
	5 IOCH uses I/O load commands to transfer control to the attachment.	
		6 Uses cycle steal to transfer data between storage and the device.
		7 Issues interrupt request to indicate to the CSP that the transfer is complete.
	8 CSP senses device interrupt.	
	9 Resets the interrupt.	
	10 IOCH senses the status of the attachment.	
	11 Returns control to the SSP.	
12 SSP tests the status of the attachment.		
13 SSP performs error recovery and error recording.		
14 SSP returns control to the customer program.		

10-821
I/O Instruction Transfer

Input/output (I/O) instructions permit the CSP to control the attachments by starting I/O operations and by requesting status information from the attachments. The CSP can also use I/O instructions to transfer data to or from attachments that have a slow data transfer rate.

The CSP has two I/O instructions that communicate through the channel to the attachments:

- I/O immediate
- I/O branch on condition

The I/O immediate instruction is 2 bytes long; the I/O branch on condition instruction is 4 bytes long. The low byte of work register 0 (WR0 low) contains the device address for each I/O instruction. When the instruction is performed, the CSP sends WR0 low to the channel. The channel then combines bits 0-3 of WR0 low with the modifier field and sends the result over the bi-di bus to the attachment when the '−control out' signal is active. The following table shows the major events that occur during an I/O instruction transfer.

Channel	Attachment
1 Sets command bus out to command value.	
2 Activates the '−control out' signal.	
3 Sets bi-di 0-7 to device address (0-3) and CBO modifier (4-7).	
4 Activates the 'channel strobe' signal.	
	5 Activates the '−service in' signal.
	6 Sets bi-di 0-7 to requested data (if needed).
	7 Tag bit 4 valid.
8 Deactivates the '−control out' signal.	
9 Activates the '−service out' signal (data and tag buses need not be valid any more).	
10 Sets bi-di 8-15 to data (if needed).	
	11 Deactivates the '−service in' signal.
12 Deactivates the '−channel strobe' signal.	
13 Deactivates the '−service out' signal.	
14 CBO and bi-di 0-7 no longer valid (end of operation).	

10-822
Cycle Steal Read from Main Storage

CSP	MSP
1 Activates the '−clock MSAR' signal and puts the command byte on system bus bits 0-7 and the PCSP on system bus bits 8-15.	
	2 Storage control unit clocks command/PCSP.
3 Activates the '−storage function' signal and puts the main storage address on system bus bits 0-15.	
	4 Storage control unit clocks main storage address.
5 Deactivates the '−clock MSAR' signal.	
	6 Reads data from main storage.
	7 Data valid on system bus.
	8 Generates the '−buffer ready' signal.
9 Clocks data into channel buffer.	
	10 Repeats steps 6 through 9 for multiple-byte transfers.
11 Deactivates the '−storage function' signal.	
12 Operation complete; returns to normal processing.	

10-823
Cycle Steal Write to Main Storage

CSP	MSP
1 Activates the '−clock MSAR' signal and puts the command byte on system bus bits 0-7 and the PCSP on system bus bits 8-15.	
	2 Storage control unit clocks command/PCSP.
3 Activates the '−storage function' signal and puts the main storage address on system bus bits 0-15.	
	4 Storage control unit clocks main storage address.
5 Deactivates the '−clock MSAR' signal.	
6 Channel puts data on system bus.	
	7 Storage control unit clocks data from system bus.
	8 Generates the '−buffer ready' signal.
	9 Storage control unit writes data to main storage.
	10 Repeats steps 6 through 9 for multiple-byte transfers.
11 Deactivates the '−storage function' signal.	
12 Operation complete; returns to normal processing.	

10-824
Single Read from Main Storage

CSP	MSP
1 Activates the '–clock MSAR' signal and puts the command byte on system bus bits 0-7 and the PCSP on system bus bits 8-15.	
	2 Storage control unit clocks command/PCSP.
3 Activates the '–storage function' signal and puts the main storage address on system bus bits 0-15.	
	4 Storage control unit clocks main storage address.
5 Deactivates the '–clock MSAR' signal.	
	6 Reads data from main storage.
	7 Data valid on system bus.
	8 Generates the '–buffer ready' signal.
9 Clocks data into CSP buffer.	
10 Deactivates the '–storage function' signal.	
11 Operation complete; returns to normal processing.	

10-825
Single Write to Main Storage

CSP	MSP
1 Activates the '–clock MSAR' signal and puts the command byte on system bus bits 0-7 and the PCSP on system bus bits 8-15.	
	2 Storage control unit clocks command/PCSP.
3 Activates the '–storage function' signal and puts the main storage address on system bus bits 0-15.	
	4 Storage control unit clocks main storage address.
5 Deactivates the '–clock MSAR' signal.	
6 Puts data on system bus.	
	7 Storage control unit clocks data from system bus.
	8 Generates the '–buffer ready' signal.
	9 Storage control unit writes data to main storage.
10 Deactivates the '–storage function' signal.	
11 Operation complete; returns to normal processing.	

10-826
Multiple-Byte Cycle Steal

Multiple-byte cycle steal is a mode of operation that permits an attachment to write or read data to or from storage without affecting the actions of the MSP. Each operation can transfer up to 256 bytes of data when the bi-di bus is being used as a 2-byte wide bus. To start a multiple-byte cycle steal, the attachment generates a cycle steal request to the channel. The priority of this request is the same as a normal cycle steal; that is, it is higher than any other interrupt except machine check.

When the channel services the request, it senses the device IDs on the bi-di bus and permits the cycle steal from the attachment with the highest priority. If the transfer is for main storage, the storage control unit of the MSP controls main storage priorities between the channel and the MSP.

The attachment can then use main storage cycles to transfer its data as long as the channel keeps the '–service out' signal active. The attachment can transfer 1 or 2 bytes of data for each '–channel strobe' signal. The following table shows the major events that occur during a multiple-byte cycle steal operation.

Channel	Attachment
	1 Sends the '–burst' signal to the channel.
2 CSP stops.	
3 Generates a sense ID command (CBO = 000).	
4 Activates the '–control out' signal.	
5 Pulses the '–channel strobe' signal.	
	6 Bi-di 0-7 set to device ID bit: 0 = Not used 1 = Data communications 2 = Not used 3 = Not used 4 = Data storage attachment 5 = Not used 6 = Not used 7 = Work station attachment
7 Generates a cycle steal command (CBO = 010).	
8 Puts the highest priority ID bit from bi-di 0-7 on bi-di 8-15 (out).	
9 Pulses the '–channel strobe' signal.	
	10 Activates the '–service in' signal.
	11 Activates the '–cycle steal request' signal.
12 Deactivates the '–control out' signal.	
	13 Address register select lines valid.
	14 Tag bus bits valid.
	15 Bi-di 0-7 (-15) valid for input data.
16 Activates the '–service out' signal.	
17 Reads or writes data (10-827 or 10-828).	
18 Bi-di 0-7 (-15) valid for output data.	
	19 Repeats steps 15 through 17 for each transfer.
	20 Deactivates the '–service in' signal.
	21 Deactivates the '–cycle steal request' signal.
22 Deactivates the '–service out' signal (operation complete).	
23 CSP returns to its operations.	

10-830
Channel Errors

When the channel finds an error, it sets flags in the channel error byte and generates a channel check to the CSP. The CSP microcode can then attempt the operation again, record the error in the error table, or run without the failing device. The channel can perform no more data transfers until the CSP recognizes the channel check and completes its error recording procedure. The channel error byte and the channel register remain constant, as a record of the conditions at the time of the error, until:

- The system is powered off.
- The CSP clears both registers.
- The System Reset key on the control panel is pressed. If the system is started again without being powered off, the CSP stores the channel information in control storage during initial program load (IPL), and records it on disk when IPL is complete.

If the CSP cannot run because of the error, a processor check occurs and the system stops with the Processor Check light on (control panel).

Channel Error Recovery

CSP	Channel
	1 Senses an error condition and records it in the channel error byte.
	2 Generates a channel check to the CSP.
3 Generates a machine check interrupt and activates the machine check servicing routine.	
4 Reads the channel error byte and the channel register and places the information in the error table.	
5 Resets the machine check interrupt and the channel error condition.	
6 Attempts the I/O operation again.	
7 If multiple attempts fail, places the attachment offline.	
	8 Returns to normal operation.

Blast Condition

For critical errors, the CSP clears all attachments from the channel by activating both the '−control out' and '−service out' signals at the same time that the '−channel strobe' signal is not active. This operation is a blast condition. A blast condition is generated because of one of the following:

- Channel parity errors.
- Device address not valid.
- Time-out error.
- A device has constant control of the channel (caused by a machine check during a multiple-byte cycle steal operation).
- An I/O instruction or cycle steal operation did not complete normally.

The blast condition is at least 800 nanoseconds long.

CSP	Channel
1 Senses a critical error condition on the channel.	
2 Generates the '−service out' signal.	
3 Generates the '−control out' signal.	
	4 Removes information from the '−tag bus in' and the '−ARS bus' signals.
	5 Removes information from bi-di 0-15.
	6 Deactivates the '−service in' and '+multidevice response' signals.
	7 Deactivates the '−burst cycle steal request' signal (during cycle steal).
	8 Keeps the '−interrupt request' and '−cycle steal request' signals active.
9 Deactivates the '−service out' and '−control out' signals.	
10 Returns to normal operations.	
	11 Starts the I/O operation again.

10-840
CSP or Cycle Steal Sense of MSP Register

CSP	MSP
1 Activates the '–clock MSAR' signal and puts the command byte on system bus bits 0-7 and the PCSP on system bus bits 8-15.	
	2 Storage control unit clocks command/PCSP.
3 Activates the '–storage function' signal and puts the MSP register address on system bus bits 0-15.	
	4 Storage control unit clocks MSP register address.
5 Deactivates the '–clock MSAR' signal.	
	6 Reads data from MSP register.
	7 Data valid on system bus.
	8 Generates the '–buffer ready' signal.
9 Clocks data into CSP buffer.	
10 Deactivates the '–storage function' signal.	
11 Operation complete; returns to normal processing.	

10-841
CSP or Cycle Steal Load of MSP Register

CSP	MSP
1 Activates the '–clock MSAR' signal and puts the command byte on system bus bits 0-7 and the PCSP on system bus bits 8-15.	
	2 Storage control unit clocks command/PCSP.
3 Activates the '–storage function' signal and puts the MSP register address on system bus bits 0-15.	
	4 Storage control unit clocks MSP register address.
5 Deactivates the '–clock MSAR' signal.	
6 Puts data on system bus.	
	7 Storage control unit clocks data from system bus.
	8 Generates the '–buffer ready' signal.
	9 Storage control unit writes data to MSP register.
10 Deactivates the '–storage function' signal.	
11 Operation complete; returns to normal processing.	

10-850
Main Storage Read

MSP	Main Storage
1 Places the RAS address on the MS address bus. Activates the '−RAS' signal. Places the CAS address on the MS address bus. Activates the '−CAS' signal.	
2 The '−MS read/+MS write' signal is valid.	
	3 Latches the status of the address and the '−MS read/+MS write' signal.
4 Activates the '−data out gate' signal.	
	5 Puts data on the main storage bus.
6 The address is no longer valid. Deactivates the '−MS read/+MS write' signal.	
7 Deactivates the '−data out gate' signal.	
	8 Removes data from the main storage bus.

10-852
Main Storage Refresh

MSP	Main Storage
1 Places the refresh address on the MS address bus. Activates the '−RAS' signal.	
2 Deactivates the '−RAS' signal.	

10-853
Main Storage Write

MSP	Main Storage
1 Places the RAS address on the MS address bus. Activates the '−RAS' signal.	
2 Places the CAS address on the MS address bus. Activates the '−CAS' signal.	
3 Activates the '−MS read/+MS write' signal.	
	4 Latches the status of the address and '−MS read/+MS write' signals.
5 Puts data on the main storage bus.	
6 Latches data into main storage.	
7 Address is no longer valid. The '−MS read/+MS write' signal is no longer valid.	

10-860
MSP Instruction Fetch

The MSP can fetch instructions from main storage as long as the CSP holds the '−allow MSP run' signal active, and there are instructions to be operated on. The MSP performs the following actions during an instruction fetch sequence:

1. Leaves the alternate mode condition (10-870).
2. Checks SB1 bit 6. If this bit is set, the MSP starts a fast task load (10-866).
3. Uses the contents of the IAR to form a real address. Uses this real address to perform a main storage read (10-850).
4. Increases the address in the IAR to get the remaining bytes of the instruction from main storage.
5. When all of the instruction has been read from main storage, the MSP increases the address in the IAR.
6. Starts to perform the instruction (10-861 through 10-863).

10-861
MSP Instruction Operation for Two-Address Instructions

MVC and ZAZ Instructions

The MSP card performs the following functions to perform either an MVC or a ZAZ instruction:

1. During instruction fetch (10-860), the MSP gets two addresses from main storage, puts them in either the X- or Y-register, adds an index value (if needed), and stores the indexed addresses in the OP1 and OP2 registers.
2. Makes a real address using the contents of the OP2 register.
3. Reads operand 2 from main storage, using the real address, and stores operand 2 in either the X- or Y-register (the Q-byte is used to keep track of the length of the operand).
4. Performs the operation on operand 2.
5. Sets values in the PSR (except MVC).
6. Makes a real address using the contents of the OP1 register.
7. Uses the real address to write the result into the operand 1 location in main storage.
8. Starts another instruction fetch (10-860).

ALC, SLC, AZ, SZ, ITC, MVX, and ED Instructions

The MSP card performs the following functions to perform the ALC, SLC, AZ, SZ, ITC, MVX, and ED instructions:

1. During instruction fetch (10-860), the MSP gets two addresses from main storage, puts them in either the X- or Y-register, adds an index value (if needed), and stores the indexed addresses in the OP1 and OP2 registers.
2. Makes a real address using the contents of the OP2 register.
3. Reads operand 2 from main storage, using the real address, and stores operand 2 in either the X- or Y-register (the Q-byte is used to keep track of the length of the operand, except for MVX).
4. Makes a real address using the contents of the OP1 register.
5. Reads operand 1 from main storage, using the real address, and stores operand 1 in either the X- or Y-register (the Q-byte is used to keep track of the length of the operand, except for MVX).
6. Performs the operation on operands 1 and 2.
7. Sets values in the PSR (except ITC and MVX).
8. Makes a real address using the contents of the OP1 register.
9. Uses the real address to write the result in the operand 1 location in main storage.
10. Starts another instruction fetch (10-860).

CLC Instruction

The MSP card performs the following functions to perform a CLC instruction:

1. During instruction fetch (10-860), the MSP gets two addresses from main storage, puts them in either the X- or Y-register, adds an index value (if needed), and stores the indexed addresses in the OP1 and OP2 registers.
2. Makes a real address using the contents of the OP2 register.
3. Reads operand 2 from main storage, using the real address, and stores operand 2 in either the X- or Y-register (the Q-byte is used to keep track of the length of the operand).
4. Makes a real address using the contents of the OP1 register.
5. Reads operand 1 from main storage, using the real address, and stores operand 1 in either the X- or Y-register (the Q-byte is used to keep track of the length of the operand).
6. Performs the operation on operands 1 and 2.
7. Sets values in the PSR.
8. Starts another instruction fetch (10-860).

10-862
MSP Instruction Operation for One-Address Instructions

The MSP card performs the following actions to perform a one-address instruction:

1. During instruction fetch (10-860), the MSP gets one address from main storage, puts it in either the X- or Y-register, adds an index value (if needed), and stores the indexed address in the OP1 register.
2. If the instruction uses an operand from storage (L, A, S, TBN, TBF, CLI, SRC, SLI, SBN, and SBF):
   a. Makes a real address using the contents of the OP1 register.
   b. Reads operand 1 from main storage, using the real address, and stores operand 1 in either the X- or Y-register (the Q-byte is used to keep track of the length of the operand for SRC only).
3. Performs the operation on operand 1. The PSR and LSR registers may be changed by the instruction.
4. If the result is to be written to storage (S, SBN, SBF, MVI, and SRC):
   a. Makes a real address using the contents of the OP1 register.
   b. Uses the real address to write the result in the operand 1 location in main storage.
5. Starts another instruction fetch (10-860).

10-863
MSP Instruction Operation for Control Instructions

The MSP performs all operations on control format instructions during the instruction fetch cycle (10-860).

Branch Instructions

For branch instructions, the MSP performs the following actions:

1. Tests the PSR with the mask value in the Q-byte.
2. If the PSR matches the mask, the MSP:
   a. Loads the contents of the IAR into the ARR
   b. Puts a new address into the IAR
   c. Starts a new instruction fetch (10-860).

Load Address and Load PMR Instructions

The MSP performs the following actions:

1. Loads the specified register with the value from the instruction.
2. Starts another instruction fetch (10-860).

SVC Instructions and Operations That Cannot Be Performed

The MSP performs the following actions:

1. Loads the R-byte (third byte of the instruction) into the LCRR in the LSR stack.
2. Generates an interrupt level 5 request to the CSP.
3. Performs a fast task save operation (10-865).

10-865
MSP Fast Task Save

The MSP performs the following actions:

1. The MSP is performing instructions, and SB1 bit 4 is on (permits fast task save).
2. An MSP stop condition occurs (except a check):
   a. Address compare stop.
   b. Soft stop (SB1 bit 5 is active when a specified type of instruction is performed).
   c. An SVC (or any operation that cannot be performed) is found.
   d. The CSP deactivates the '–allow MSP run' signal.
   e. The MSP Stop key on the control panel is pressed.
   f. Instruction step mode.
3. Generates an interrupt level 5 request to the CSP.
4. Sets SB0 bit 0 on.
5. Reads values from PREG and PSREG to determine the ending address of the task save area in main storage.
6. Stores task values in the save area in main storage starting at the end and counting backward.
7. Switches to alternate mode (10-870).

When the MSP enters alternate mode, the CSP reads main storage to find out why the MSP stopped.

10-866
MSP Fast Task Load

MSP	Other Processing Unit Cards
1 The MSP is in alternate mode, and SB1 bit 6 is on (permits fast task load).	
	2 The CSP activates the '–allow MSP run' signal.
3 Checks SB1 bit 6 (if this bit is not on, the MSP will perform the task that is already in the MSP).	
4 Reads values from PREG and PSREG to determine the ending address of the task load area in main storage.	
5 Loads task values from the load area in main storage starting at the end and counting backward.	
6 Reads values from PATR and PSATR to determine the ending address of the ATR load area in main storage.	
7 Loads ATR values from the load area in main storage starting at the end and counting backward.	
8 Starts performing instructions using the new task values.	

10-870
MSP Alternate Mode

The alternate mode of the MSP is a not active condition that the MSP enters to wait for instructions from the CSP. The MSP enters alternate mode for one of the following reasons:

- A fast task save operation completes (10-865).
- A check condition occurs.
- The CSP activates the '–temp stop request' signal (for a cycle steal).

The MSP leaves the alternate mode when the CSP activates the '–allow MSP run' signal. When this occurs, the MSP starts another instruction fetch (10-860).

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Numerics

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Processing Unit and Channel
Maintenance Information Manual
Stage 3

SY31-9035-0

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