## TECHNICAL PUBLICATIONS CHANGE NOTICE

### 1.0 Purpose

Document FS 002 "Field Engineering Technical Manual SPD 10/20 Stored Program.Display" is currently being evaluated for changes and/or revisions. Promulgated information outdated since the original printing, which could present a hazzard to personnel, or result in faulty machine operation will receive immediate attention, using the change notice as a distribution vehicle.

### 2.0 Effectivity

Model 005 and 006 power supply voltages. The supply voltages +14 and +25 are set in the factory using proper load currents and a thermistor simulator where $R=347$ ohms. The simulation value corresponds to the thermistor resistance value when connected to the memory stack at an ambient temperature of $25^{\circ} \mathrm{C}\left(77^{\circ} \mathrm{F}\right)$. Under this controlled condition, the +14 volts is set to +14.0 and the +25 volts is set to +22.0 . The indicating instrument can be a Digital voltmeter or calibrated voltmeter.

Since the ambient temperature in the field varies, the only true reference is the factory procedure. On terms of measurement accuracy, the DVM is best, however, not always available. Use of a voltage droping device allows measurement with a VOM on a more sensitive range than otherwise. Figure 1 illustrates the voltage adjustment fixture. The following is a procedure for on site measurement and adjustment.

| STEP | PROCEDURE | RESULTS |
| :---: | :--- | :--- |
| A | Disconnect the thermistor leads (brown power <br> supply terminals) attach the simulator resistor <br> to the supply (347 ohms +15 ohms) and power <br> up the unit. |  |
| B | Connect black clip lead (gnd) to chassis ground. <br> Connect orange clip lead to +14 V (top end of <br> C22 or C29 memory electronics board) Leave <br> red clip open. |  |



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TCPN \#001
10/12/71
R. Moore

Page 2

| STEP | PROCEDURE | RESULTS |
| :---: | :--- | :--- |
| D | Set VOM on 2.5 Volt scale and connect probes <br> to the + and - terminals of the fixture, observing <br> correct meter polarity. | +14 should be <br> adjusted to 14.0 V <br> which will indicate <br> 2.0 on the VOM. |
| F. | Remove the orange clip lead and attach the red <br> clip lead to +25 volts. (t25 is accessable on the <br> top ends of R64 or R83 on the memory electronics <br> board). Leave orange lead open. <br> Power down, remove simulator and reattach <br> thermistor leads. | +25 should be <br> adjusted to +22.0 <br> which will indicate <br> 2.0 on the VOM. |

With respect to the above data, the nominal voltage of +25 VDC referenced in the Technical Manual FS002 pages:

| $2-5$ | $5-73$ |
| :--- | :--- |
| $5-56$ | $5-75$ |
| $5-57$ | $7-3$ |
| $5-71$ | $7-7$ |

should be changed to +22 volts $D$. C.



Figure 1 Memory Voltage Adjustment Fixture

# FIELD ENGINEERING 

TECHNICAL MANUAL

$S P D^{T M} 10 / 20$

## PERIPHERALS

VOLUME I SPD-L Program Loader
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## FOREWORD

This manual provides the installation, theory of operation and maintenance procedures for the SPD -L Program Loader. Field repair is accomplished by on-site replacement of a faulty module. Module repair is performed off-site by a technical staff with appropriate test equipment. An understanding of the theory provided in this manual and a familiarization with the logic diagrams provided in support document FS 003 will provide the required background for technical proficiency.


Figure 1-1. SPD-L Program Loader

## CHAPTER I

 INTRODUCTION
### 1.1 GENERAL DESCRIPTION

The SPD-L Program Loader is a perforated paper tape reader with associated controller logic designed to input data to the SPD 10/20 Stored Program Display. As illustrated in Figure l-1, the SPD-L is a compact, portable device with the following physical characteristics:
12 inches wide $\quad$ Weight: 7 pounds
7 inches deep
5 inches high

Data and instructions are inputted to the TPU (Terminal Processing Unit) at a rate of 30 characters per second. When a test console is used to aid in program debugging, all SPD-L operations can be performed in the single cycle mode. Data input can be initiated from the Program Loader via a "bootstrap" mode or from the TPU in response to Read Input/ Output instructions.

## CHAPTER II

INSTALLATION

## 2. 1 INSTALLATION PROCEDURE

Since the SPD-L is a self-contained unit, installation, as such, requires no special ability or complex procedure. When it is desired to load a perforated tape program, the following steps should be observed:

1. Locate the Loader physically close to the Master Display (data input cable is approximately five feet long).
2. Turn OFF the Master Display a. c. power.
3. Plug the female end of the 50 -pin data cable connector into the Loader recepticle.
4. Plug the male end into the Terminal I/O connector panel recepticle number 9 or other designated connector.
5. Raise starwheels by rotating the lever illustrated in Figure l-l.
6. Depress the mechanical release knob located in the center of the tape supply reel (see Figure l-1).
7. Insert the tape leader under the starwheels with tape guide holes lined up on the tape sprocket.
8. Lower starwheels into operating position.
9. Turn ON a.c. power to the Master Display.

The above installation instructions are all that is necessary to prepare the SPD-L for operation.

## CHAPTER III

## SPD-L OPERATIONAL DESCRIPTION

### 3.1 DESCRIPTION

After following the procedure outlined in Chapter II, the unit will input coded data to the TPU when the RED pushbutton is momentarily depressed. Note that there were two previously defined modes of operation; the input load initiated at the Loader has been prescribed first. This approach is taken because the BOOT mode must be first when one assumes the memory contents upon initial load are zero. If, however, some prior information was residing in memory, the W I/O mode may have been selected. Also, the placement of the tape under the starwheels must allow at least four non-punched (non-zero) character spaces prior to the program perforations. Another operating restriction is that the RED 'Boot' button must not be held depressed past the leader or proper loading will not be accomplished.

For the purpose of program loading, the plexiglass front protective cover is lifted, which exposes the internal circuitry as illustrated in Figure 3-1. Figure 3-2 provides a component view of both boards $A$ and $B$ with the test points identified. The test point notation is found in Chapter IV.

The programmed instructions associated with the SPD-L Program Loader are summarized below:


Figure 3-1. Program Loader, Internal View
3-2


| Type <br> Bit <br> Decode | Function <br> Bit <br> Decode | Description |
| :--- | :--- | :--- |
| CIO | 0 | Leader Search-commands the SPD-L to advance <br> the tape to a valid leader (four or more consecutive <br> null characters followed by a non-null character). |
| CIO | 2 | Boot Search - commands the SPD-L to advance the <br> tape to the boot leader (four or more consecutive <br> null characters followed by the ASCII '\#' character) <br> and then to transfer data. |
| CIO | 5 | Mask Interrupt - sets the interrupt mask, inhibiting <br> interrupts to the TPU. |
| RIO | 0 | Unmask Interrupt - resets the inter rupt mask, <br> enabling interrupts to the TPU. |
| RIO | Input Unit Online - is acknowledged when the SPD-L <br> is online. |  |

### 3.2 PROGRAMMED EVENTS ON TAPE

Figure 3-3 is a physical representation of a typical Program Loader instruction tape. The tape illustrated has been foreshortened by elimination of the two large areas of data, but illustrates the start and end of the BOOT and operating programs. From left to right, the leader is the first data to pass through the starwheel sensors. The signal resulting from this portion of tape indicates no data present. The only hole in the tape at this point is the tape sprocket hole. The first actual data encountered is the enter BOOT character. The next series of data is the BOOT loader. This data is characterized by the continuous punching of bit 6. The last character in this series is the END BOOT code, after which control for further operation is signaled from the TPU. After the BOOT loader, another portion of clear leader is positioned between the BOOT loader and the start of the operating program. At the end of the operating program there are a few blank leader positions, followed by the last data character which stops the program loader.


## CHAPTER IV

## THEORY OF OPERATION

## 4. 1 INTRODUCTION

The Program Loader control electronics is located on two logic boards within the Loader. The schematic 003-01-01 contains both Board A and Board B. Figure $4-1$ is a simplified block diagram of the Program Loader controller. Program Loader interface with the TPU does not require an I/O controller. Direct access to the TPU I/O Bus is available at a 50 -pin I/O connector.

### 4.2 THEORY

Sheet 2 includes two data latches, M21 and M22, which store eight bits of inputted tape data for presentation to the TPU. Storage is provided so that switch bounce will not cause false data. The two latches accept paper tape data, PTD00 through 07; the latches are strobed at a time when the data under the head is reliable for presentation to the TPU. The data can be enabled to the TPU in either the Boot mode or by a Read I/O command from the TPU. Inverters M3 feed gate M9 with the two bit TYPE I/O decode, for decoding TIO commands. The output of M9 is fed to MIl on sheet 4 for making up an acknowledge signal. Gate M10 is enabled by the TYPEI/O controller address and clock pulse CPT02N, and is used for clocking CIO commands.


Figure 4-1. Program Loader Block Diagram

In operation, leader search or Boot search is always necessary prior to data entry. After the leader search command, four or more blank codes ( 0 's) must be found, then the first non-blank (non-zero) character is presented to the TPU. In Boot search the first zero character after the Boot character is presented. The system will enter boot if the Boot character is found and has been preceded by four blanks. Because of these prior stipulations, when a tape is loaded on the head of the reader at least four zero characters must be allowed. On sheet 3 the counter M1 and M2 counts the decoded blank characters. Gate M20 is labeled PTZDETI, paper tape 0 detector, which decodes four zeros. The output of M20 is ANDed with PTZDET0 at gate M18, which is equivalent to the other four bits and again decodes all zeros. The total combination indicates eight zeros detected and enables the clock into the counter, and counting starts when the first zero character is detected. If a non-zero character is detected, the counter is reset. When a zero character is detected, LCIDET at M7 is a low; if the character is nonzero, that point is high, which feeds into gate LCGCLF, allowing a clock pulse through to reset the counter. The counter continues to count until four zero counts are detected. At that time a non-zero character will reset the counter, but the first non-zero character after the count of four (MOD flops set) indicates a valid mode with leader detected, which acknowledges the TPU and sets the LDFF (leader detected) flip flop M15 before resetting the counter. The fact that leader detect occured is remembered at M15. After detecting four zeros in a row, the output from the MOD detect flip flop, pin 11, is combined with the leader search mode signal and a non-zero character signal. The signal out of gate M14 sets flip flop M15.

The BOOT detector flip flop, M15, is much the same. It is set by a specific character. After the MOD DET flip flop is set, a valid decode in the boot character is available and the controller is in the boot mode, the BOOT flip flop is set and the BOOT mode is entered. On the bottom of sheet 3 are located two bow tie latches, M5 and M17. One is the leader search latch flip flop (LSL), which sets on a programmed command C I/O which dictates a leader search. The boot latch sets under two conditions:
one is depressing the RED button on the paper tape chassis, the other is when under TPU control via CIO \#2. When performing a search, the leader search flip flop puts out a command signal which advances the tape but does not acknowledge TPU. The Boot flip flop M15 on sheet 3 is called BDFF01. There is another flip flop called BDFF02, M2 on sheet 4 , which follows BDFF01 by a one character delay. It is utilized because the first BDFF0l will set on the boot character. But that character is not presented to the TPU, so there is a one character delay. The character after the boot character sets BDFF02, which is used for acknowledging the TPU. This delay assures that the boot character is not presented to the TPU as the first character of the program.

Sheet 4 schematically illustrates the free-running oscillator, composed of discrete components Q1 and Q2, which operate at a 30 Hz rate. The oscillator is free-running in design, but is also controlled. The output of the oscillator sets a flip flop called OSFF (M12) once every character and that signal advances the paper tape on the reader. Once the OSFF flip flop is set, it sets another flip flop called data available (DAFFA) and the output of DAFFA (low side) is fed to inverter M6 pin 1, which disables transistor Q1 and oscillation stops. This condition is provided for operation in the single cycle mode when attached to a test console. The sequence of events which occur after getting a character are: the one shot flip flop is set, which sets the data available flip flop, and causes an inhibit of the oscillator. The flip flop DAFFA is reset in the following conditions: if in the READ mode, and the detected command is a READ I/O, if in the Leader Search mode, or the BOOT Search mode. In the BOOT mode the TPU can accept characters as fast as the reader detects them. A signal from the BOOT flip flop M2 is ANDed with data available flop at M10. On the next clock pulse, Data Available is reset and operation continues to the next character.

In the READ mode the Program Loader waits until the TPU reads the character because the TPU may be performing some other data handling and may not be ready for the next character. In the BOOT mode the Loader is the only device capable of inputting data and, in terms of cycle time, is much slower than the TPU. The moment the Data Available flip flop is set,
an advance to the next character is automatic. The same conditions hold for the BOOT search mode. The period of waiting until the character is read is accomplished by holding the oscillator until the Data Available flip flop is set.

The only other logic on sheet 4 is the mask flip flop which is set by function 02, and cleared by function 03. The gates M10 and M11 are on sheet 4. The T I/O is present if the controller is plugged in. The Read I/O acknowledge occurs only when there is data available which comes from gate M9, which signals 'data available' after the leader has been detected. The BOOT mode acknowledge goes out one character after the boot character, determined by the BDFF flip flop. Every time there is Boot data available, an acknowledge is sent. Flip flop M2 on sheet 2 sets on the positive going edge of the one shot flip flop and is ANDed with the timing signal from TURT4, a square wave from the TPU. The reason for using TURT4 is that it is the only clock available when the TPU is in clock stop.

## CHAPTER V

MAINTENANCE AND REPAIR

### 5.1 GENERAL

The actual data reading is accomplished with a vendor supplied electro-mechanical starwheel sensing device. The eight starwheels can sense up to eight bits of data. The eight corresponding contacts are composed of two silver contacts and a stainless steel pressure wire. The contacts can switch 0.1 amperes (resistive load) for a life of 100 million cycles. The rate of character reading is variable from 0 to 30 characters per second, asynchronously, when operated at rated power ( 0.4 watts) with appropriate suppression. The speed is a function of solenoid operate and release time.

The tape reader reads all standard five, six, seven or eight channel tapes. In addition, all grades of paper or plastic tapes can be read. The reader mechanism is warranted by the vendor for a period of one year. Figure 5-1 illustrates the top and front view of the reader mechanism.

### 5.2 SIGNAL AND CABLE DATA

Figure $5-2$ is a top view of the Program Loader, illustrating the connector locations. The A and B connectors are for circuit boards A and B respectively. The connector designated ' $C$ ' is for the reader data and control signal interface cable to the controller electronics. Connector $D$ is the $50-\mathrm{pin}$ cable socket for the TPU interface cable. Connectors A and B include two rows


Figure 5-1. SPD-L Tape Reader Mechanism


Figure 5-2. Program Loader Illustrating Connector Locations
of pins which mate with the two sides of the circuit board when installed. The row positioned at the rear of each connector is numerically numbered 1 through 22. The front row is alphabetical, A through Z. D is a 50 -pin connector and C is a 15-pin connector. Table 5-1 provides signal nmemonics with definition and complete chassis wiring. The wiring is called out by first referencing the appropriate connector, then the assigned pin.

Table 5-2 lists the wiring of the external 50-pin connector. Due to the drive necessary from TPU to Reader, this cable is generally kept as short as practical (not to exceed 5 feet). Table 5-3 lists the test points located on the circuit cards with applicable logic levels.

Table 5-1. Program Loader Connector Wiring and Nmemonic Definition

| Nmemonic | Definition | WIRED |  |
| :---: | :---: | :---: | :---: |
|  |  | FROM | TO |
| TURT4 | Timing Unit Register Time 4 | D-37 | A-21 |
| PTOS CL | Paper Tape Oscillator Enable/Disable | B-L | A-6 |
| FUNC 02 | Programmed Function Code Bit 2 | D-24 | A-15 |
| FUNC 03 | Programmed Function Code Bit 3 | D-26 | A-X |
| INT SEL IN | TPU Interrupt Selector Signal | D-31 | A-C |
| ACK | Acknowledge Signal | A-W | D-27 |
| INT SEL OUT | Daisy Chain Interrupt Signal | A-B | D-32 |
| INTX | Interrupt By Controller | A-H | D-30 |
| DAFF | Data Flip Flop | A-P | B-E |
| CLIPT | Leader Clock Pulse | A-S | B-11 |
| RSPT | Reset Paper Tape | A-19 | B- 5 |
| RESET | Initializing Signal For Flip Flops | D-25 | B-4 |
| DSCIICL | Program Decode Mask Flop Clock | A-20 | B-8 |
| FUNC00 | Programmed Function Code Bit D | D-20 | B-7 |
| FUNCIO1 | C I/O Boot | A-L | B-C |
| FUNC01 | Programmed Function Code Bit 1 | D-22 | B-D |
| ENT BOOT | Boot Switch Signal | C-12 | B-J |
| PWR | Power Up Reset | B-R | A-T |
| BOOT | Forced Mode for Data Loading | B-2 | D-29 |
| OSGCL | ¢9 Clock for Leader and Boot Detect Flops | B-6 | A-E |
| DAGLD | Leader Detected Data Available | B-10 | A-F |
| BDFF02 | Boot Flip Flop Number 2 | B-3 | A-2 |
|  | From Boot Flop $1 \bar{Q}$ To Boot 2 K | B-9 | A-3 |
| TYPI01 | Type 01 Inverted | A-U | B-F |
|  | Function of ADDXX | A-R | B-H |
| RIOAC | Read I/ O Acknowledge | A-V | B-B |
|  | Reader Drive Signal | A-Y | B-Y |
| +14V | Reader Mechanism Power | D-38 | A-16 |
| $+5 \mathrm{~V}$ | Logic Power | D-1 | A-1 |
|  | $+5 \mathrm{~V}$ | A-1 | A-A |
|  | $+5 \mathrm{~V}$ | A-A | B-1 |
|  | $+5 \mathrm{~V}$ | B-1 | B-A |
| GND | Ground | D-2 | A-22 |
| GND | Ground | A-22 | A-Z |
| GND | Ground | A-Z | B-22 |
| GND | Ground | B-22 | B-Z |
| GND | Ground | D-40 | A-22 |
| GND | Ground | D-41 | B-22 |
| CONT 07 | Controller Priority Address | D-28 | A-N |

Table 5-1. Program Loader Connector Wiring and Nmemonic Definition Cont'd.

| Nmemonic | Definition | WIRED |  |
| :---: | :---: | :---: | :---: |
|  |  | FROM | TO |
| CPTø2 | Clock Pulse Time ( $\varnothing$ ) 2 | D-34 | A-M |
| TYP00 | Programmed Type Code Bit 0 | D-19 | A-J |
| TYP01 | Programmed Type Code Bit 1 | D-21 | A-K |
| INB00 | Input Bus To TPU Bit 0 | D-4 | B-W |
| INB01 | Input Bus to TPU Bit 1 | D-6 | B-T |
| INB02 | Input Bus To TPU Bit 2 | D-8 | B-U |
| INB03 | Input Bus To TPU Bit 3 | D-10 | B-V |
| INB04 | Input Bus To TPU Bit 4 | D-12 | B-P |
| INB05 | Input Bus To TPU Bit 5 | D-14 | B-M |
| INB06 | Input Bus To TPU Bit 6 | D-16 | B-12 |
| INB07 | Input Bus To TPU Bit 7 | D-18 | $\mathrm{B}-\mathrm{N}$ |
|  | +14V | A-17 | C-13 |
| CMC | Tape Reader Clock | A-18 | C-11 |
| CPTø8 | Clock Pulse Time ( $\varnothing$ ) 8 | D-36 | A-D |
| Ground |  | B-22 | B-Z |
| PTD00 | Tape Data Bit 0 | C-1 | B-14 |
| PTD01 | Tape Data Bit 1 | C-2 | B-15 |
| PTD02 | Tape Data Bit 2 | C-3 | B-17 |
| PTD03 | Tape Data Bit 3 | C-4 | B-16 |
| PTD04 | Tape Data Bit 4 | C-5 | B-18 |
| PTD05 | Tape Data Bit 5 | C-6 | B-19 |
| PTD06 | Tape Data Bit 6 | C-7 | B-21 |
| PTD07 | Tape Data Bit 7 | C-8 | B-20 |
| Ground |  | C-15 | B-Z |
| DLFF | 4 LSB's Clock | A-4 | B-S |
| DLFF* | 4 MSB 's Clock | A-5 | B-K |
| -- | Not Used | B-X | C-9 |
| $\phi 18$ | Reset Clock | B-13 | D-35 |

Table 5-2. Program Loader Cable 50 Wire 50 Pin Connector
INCOTERM CB 1632
WIRING TABLE

| Color | Signal | $\begin{aligned} & \text { Cinch } \\ & \text { DD } 50 \mathrm{P} \end{aligned}$ | $\begin{aligned} & \text { Cinch } \\ & \text { DD } 50 \mathrm{~S} \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| BLK | +5 VDC | 1 | 1 |
| BROWN | GND | 2 | 2 |
| RED | OTB 00 | 3 | 3 |
| ORANGE | INB 00 | 4 | 4 |
| YELLOW | OTB 01 | 5 | 5 |
| GREEN | INB 01 | 6 | 6 |
| BLUE | OTB 02 | 7 | 7 |
| VIOLET | INB 02 | 8 | 8 |
| GRAY | OTB 03 | 9 | 9 |
| WHITE | INB 03 | 10 | 10 |
| PINK | OTB 04 | 11 | 11 |
| TAN | INB 04 | 12 | 12 |
| W HT-BLK | OTB 05 | 13 | 13 |
| WHT-BRN | INB 05 | 14 | 14 |
| WHT-RED | OTB 06 | 15 | 15 |
| WHT-ORG | INB 06 | 16 | 16 |
| WHT-YEL | OTB 07 | 17 | 17 |
| WHT-GRN | INB 07 | 18 | 18 |
| WHT-BLU | TYP 00 | 19 | 19 |
| WHT-VIO | FUNC 00 | 20 | 20 |
| WHT-GRY | TYP 01 | 21 | 21 |
| RED-BLK | FUNC 01 | 22 | 22 |
| RED-YEL | ATTENTION | 23 | 23 |
| RED-GRN | FUNC 02 | 24 | 24 |
| WHT-BLK-BLK | RESET | 25 | 25 |
| WHT-BLK-BRN | FUNC 03 | 26 | 26 |
| WHT-BLK-RED | ACK | 27 | 27 |
| WHT-BLK-ORG | CONT 07 | 28 | 28 |
| WHT-BLK-YEL | BOOT | 29 | 29 |
| WHT-BLK-GRN | INT XX | 30 | 30 |
| WHT-BLK-BLU | INT SEL IN | 31 | 31 |
| WHT-BLK-VIO | INT SEL OUT | 32 | 32 |
| WHT-BLK-GRY | CPT 13 N | 33 | 33 |
| WHT-RED-BLK | CPT $\varnothing 2 \mathrm{~N}$ | 34 | 34 |
| WHT-RED-BRN | CPT 18 N | 35 | 35 |
| WHT-RED-RED | CPT ø8 N | 36 | 36 |
| WHT-RED-GRN | TURT 4 | 37 | 37 |
| WHT-RED-BLU | +14 V | 38 | 38 |
| WHT-RED-VIO | -14 V | 39 | 39 |
| W HT-GRN-BLK | GND | 40 | 40 |

Table 5-2. Program Loader Cable 50 Wire 50 Pin Connector (Cont.) INCOTERM CB 1632

## WIRING TABLE

|  |  |  |  |
| :---: | :---: | :---: | :---: |
| Color | Cignal | Cinch | Cinch |
| WHT-GRN-BRN | GND | DD | D 50 |
| WHT-GRN-RED |  | 41 | 41 |
| WHT-GRN-GRN | 42 | 42 |  |
| WHT-GRN-BLU | 43 | 43 |  |
| WHT-GRN-VIO | 44 | 44 |  |
| WHT-BLU-BLK |  | 45 | 45 |
| WHT-BLU-BRN | 46 | 46 |  |
| WHT-BLU-RED | 47 | 47 |  |
| WHT-BLU-GRN | 48 | 48 |  |
| WHT-BLU-BLU | 49 | 49 |  |

Table 5-3. Test Points

| TB 7 Board A |  |  |
| :---: | :--- | :--- |
| PIN | Signal | Level |
| 1 | DAFFA | $\mathrm{H}=$ Tape Advance |
| 2 | BDFF02 | $\mathrm{H}=$ BOOT and Data Detected |
| 3 | MASK | $\mathrm{H}=$ Unmask Interrupt |
| 4 | DASMA | $\mathrm{H}=$ Mask Interrupt |
| 5 | INT | $\mathrm{H}=$ Interrupt |
| 6 | BOOAC | $\mathrm{L}=$ BOOT Acknowledge |
| 7 | RIOAC | $\mathrm{L}=$ Read I/O Acknowledge |
| 8 | MASK | $\mathrm{H}=$ Clock Mask Flop |
| 9 | OSC | $\mathrm{H}=$ Set J Input OSFF |
| 10 | TIOAC | $\mathrm{L}=$ Test I/O Acknowledge |
| 11 | FATCL | $\mathrm{L}=$ Timing Pulse |
| 12 | PTCLG0 | $\mathrm{H}=$ Tape Go |
| 13 | DAFF | $\mathrm{L}=$ Boot Reset |
| 14 | PTOSCL | $\mathrm{L}=$ Clear Data Flop A |


| TB 13 |  |  |
| :---: | :---: | :--- |
| PIN | Signal | Leard B |
| 1 | LCIDET | L $=$ Zeros Detected |
| 2 | LSL00 | $\mathrm{H}=$ Leader Search |
| 3 |  |  |
| 4 | LSIBS | $\mathrm{L}=$ Clear Leader Detect Flip Flop |
| 5 | LSICT | $\mathrm{H}=$ Set Data Mode |
| 6 | BTRES | $\mathrm{H}=$ Boot Reset |
| 7 | BDFF01 | $\mathrm{L}=$ Bit 7 Is Zetected |
| 8 | PTIO7 |  |
| 9 |  |  |
| 10 |  | Mode Counter Clock |
| 11 |  | H = Clear Mode Detect Counter |
| 12 | LSBSCL |  |
| 13 | LCIFOR |  |
| 14 | MOD DET |  |

Table 5-3. Test Points Cont'd.

| TB 19 |  | Board B |
| :---: | :--- | :--- |
| PIN | Signal | Level |
| 1 | BCIDET | $\mathrm{H}=$ Boot Code Detected |
| 2 |  |  |
| 3 | DLFF | $\mathrm{H}=$ Clock Bits 0-3 |
| 4 | L04 | Latch Output Bit 4 |
| 5 | L00 | Latch Output Bit 0 |
| 6 | L07 | Latch Output Bit 7 |
| 7 | BIADLD | L = Read Signa1 |
| 8 | PTI04 | Paper Tape Latch Input Bit 4 |
| 9 | PTI00 | Paper Tape Latch Input Bit 0 |
| 10 | DLIFF | $\mathrm{H}=$ Clock Bits 4-7 |
| 11 | FU9CI00 | L = Leader Search Command |
| 12 | BSL00 | I+= BOOT |
| 13 | BSCSW | L = BOOT Command |
| 14 |  |  |

The following wave form taken at TB7 pin 9 is the oscillator rate for driving the tape advance mechanism.


| Volts/Div | $0.2 \times 10$ |
| :--- | :--- |
| Time/Div | 10 ms |

Table 5-4 presents a listing of possible problems which can cause malfunctions to occur at the Program Loader. However, depending on the failure, the actual cause may be at the Terminal because the Loader is dependent on the Terminal for its power source. The program tape must also be correct; therefore, when troubleshooting, a known good program should be used. This precaution will eliminate the posibility of a software problem looking like a hardware problem.

Table 5-4. Problem - Probable Cause

| Trouble | Probable Cause | Corrective Action |
| :---: | :---: | :---: |
| No reader response when Boot button is depressed | +5 or +14 volts missing or low. <br> Loose PC Board A or B Faulty one-shot Reader driving circuit Connector C disconnected Defective Memory Stack, Data Flow, Data Control, Memory Electronics or RMTU. | Check cable connections. <br> Replace fuses or otherwise restore operating voltages. <br> Reseat Power Supply boards A and B. Replace Power Supply. Check thermistor on Memory Stack. <br> Reseat both boards. <br> Check TB7-9 for oscillator waveform. <br> Check Q4, check connector C. Substitute - as required. |
| Reader mechanism starts operating when TPU is powered up. | Power up malfunction. | Substitute board B. <br> Substitute TPU Control Board. |
| Tape feeding rate irregular | Tape wound too tite. Irratic +14 volts. | Loosen tape on spool. <br> Repair as required to restore proper +14 volts. |
| Will not load past last BOOT character. | Bad Load. | Reload Program. |

Table 5-4. Problem - Probable Cause Cont'd.

|  | Probable Cause | Corrective Action |
| :--- | :--- | :--- |
|  | TPU Problem | Substitute Data Control, <br> Keyboard Controller, <br> Memory Electronics, <br> Memory Stack or Data Flow |
| Tape runs com- <br> pletely through <br> loader and sole- <br> noid operates <br> continuously. | Reader oscillator not <br> being inhibited. | Substitute Data Control, RMTU, <br> Memory Electronics, |
| Will not load <br> past first leader <br> character after <br> Boot. | Memory Sta ck or Data Flow. |  |
|  | Substitute reader Boards A interrupt select <br> and/or B. |  |

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MODEL 18 TAPE READER

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### 1.0 DESCRIPTION

1.1 The CMC Model 18 Tape reader reads data in the form of holes in paper tape and presents this data as contact closures to connected equipment. The device uses starwheels to sense the holes and steps the tape by means of a solenoid.
1.2 The simplicity of design and value-engineered manufacture make the CMC Tape Reader exceptionally reliable and unusually low in cost. It is as easy to use as an ordinary relay and as trouble-free.
1.3 Applications of the CMC Model 18 Tape Reader include numerical control of machine tools, data communications, automation of production equipment, automatic typewriters and printers, process control, automatic testing and an input device to digital computers.
1.4 Key features of the CMC Model 18 Tape Reader are: starwheel sensing, solenoid tape feed, mechanical simplicity, reliability and low cost.

### 2.0 SPECIFICATIONS

2.1 SOLENOID DRIVE - Approximately 14 watts of power is required to operate the drive coil at the rated voltages. Standard readers are available for 12, 24 and 48 volt D. C. operation. Readers for operation at other voltages are available upon special request.

Drive Voltage

| 12 V. D. C. | $8 \Omega$ | $1 \Omega$ |
| :--- | ---: | ---: |
| 24 V. D. C. | $32 \Omega$ | $4 \Omega$ |
| 48 V. D. C. | $120 \Omega$ | $33 \Omega$ |

Coil Resistance
$120 \Omega$

Series Resistor

$$
1 \Omega
$$

$4 \Omega$
$33 \Omega$
2.2 The duration of the drive pulse necessary to operate the reader is approximately 17 milliseconds. The release time is a function of the suppression circuit used. When a diode-zener series combination (with the zener voltage $1 / 2$ of the drive voltage) is placed across the drive coil, release time is approximately 25 milliseconds. We recommend a General Electric IN5059 diode (or equivalent) and an appropriate value 1 watt zener diode.
2.3 The reading rate of the reader is 0 to 30 characters per second, asynchronously, when operated at the rated power with the appropriate suppression circuit. The speed is a function of the solenoid operate and release times.
2.4 READING DIRECTION - The tape transport is unidirectional, from right to left.
2.5 TAPE - The Model 18 Tape Reader reads all standard perforated 5, 6, 7 or 8 channel tapes. All grades of paper, mylar and aluminized tapes can be read. Readers capable of reading typesetter (TTS) 'advanced feed' tape are available upon special request.
2.6 STARWHEEL SENSING CONTACTS - 8 starwheels, sensing 8 tape channels, actuate 8 corresponding contacts. Each sensing contact consists of two silver contact wires and one stainless steel pressure wire. The contact wires close to a common silver plate. The contacts can switch .100 amperes, resistive load, for a life of 100 million cycles. The maximum contact 'make' bounce is 1 millisecond.
2.7 TAPE LOADING CONTACT - The tape loading contact is open during the tape loading operation and closed when the starwheels are in the read position.
2.8 INTERRUPTER CONTACTS - Normally closed at rest, the interrupter contacts open when the armature is pulled in and reclose during the latter part of the feed stroke. The contact material is tungsten and can switch 1 ampere, resistive load for a life of 100 million cycles.
2.9 MECHANICAL LIFE - Under laboratory conditions at our factory, the Model 18 has been life tested over 100 million cycles. The read error rate is not more than 1 character in 24 million ( $2.4 \times 10^{7}$ ) characters read.
2.10 ENVIRONMENT - The Model 18 Tape Reader will operate continuously in a temperature range of $0^{\circ}$ to $70^{\circ}$ centigrade at 20 to 85 percent relative humidity providing that no temperature/humidity combination produces condensation. All metal surfaces of the reader have been treated to retard corrosion.
2.11 SIZE - The panel size is $1 / 8$ inch thick, by $31 / 2$ inches high by 7 inches wide. The front panel clearance is $21 / 4$ inches and the rear panel clearance is $11 / 2$ inches.
2.12 WEIGHT - The shipping weight of the Model 18 Tape Reader is 2 lbs.

### 3.0 THEORY OF OPERATION

3.1 STARWHEEL SENSING - Starwheels are used to sense the holes in the tape. The sensing action is illustrated in Figures 1 and 2.


FIGURE 1 Starwheel Sensing No Hole


FIGURE 2 Starwheel Sensing Hole
3.2 In Figure 1, the starwheel (1) is held against the tape (3) by the sensing arm lever (2) under the urging of the wire contacts (5) and the pressure wire (4). As the tape is advanced, the starwheel slides along the surface of the tape on two of its five points.
3.3 When a hole in the tape is encountered, the starwheel rolls into the hole and the resulting motion allows the wire contacts to close against the common plate (6) as shown in figure 2. The electrical connection is thus established between the common plate and the terminal pin (7).
3.4 The primary function of the pressure wire is to isolate the starwheel arm from the contact wires during the 'read' mode so that minor variations in the tape do not cause contact 'hash'.
3.5 A unique feature of starwheel sensing is that in the case of consecutive holes in the tape, the starwheel actuated contact remains closed and can be used as a holding circuit.
3.6 Starwheel sensing is easy on the tape. Paper program loops can be passed through the Model 18 Tape Reader thousands of times.
3.7 TAPE DRIVE - The tape drive mechanism is illustrated in figure 3.


FIGURE 3 Tape Drive Mechanism
3.8 When the drive coil (6) is energized, the armature (5) is attracted and moves about the pivot point (4). This action causes the pawl (8) to engage the next tooth on the ratchet (9). When the drive coil is de-energized, the spring (3) returns the armature and steps the ratchet. The ratchet is fixed to the tape sprocket shaft.
3.9 An extension (2) of the armature operates an actuator (1) which opens the interrupter contacts (7) when the drive coil is energized. By connecting the interrupter contacts in series with the drive coil, the device can be caused to self-step continuously. Self-step operation generally exceeds 30 C.P.S. The diode suppression should be used without zener. The interrupter switch also provides an inter-lock signal to connected equipment.
3.10 An important feature of this type of tape drive is that the tape is advanced by the spring-urged return stroke of the armature. The circuitry and control logic is considerably simplified. For example, if a command to step the tape is initiated by the character being sensed, that command is not wiped out by the energization of the coil.
3.11 The reference chart below shows the reader drive pulse and where the functions of the reader occur in respect to the drive pulse.

DRIVE PULSE VOLTAGE

TRANSPORT SHAFT
SPEED
(REV/SEC)


Open (no hole)


FIGURE 4 Reference Chart

### 4.0 INSTALLATION

4.1 The CMC Model 18 Tape Reader is designed to be mounted with four (4) number 6 screws on hole centers as shown in figure 5.


FIGURE 5 Mounting Diagram
4.2 TO REMOVE THE FRONT COVER - Remove the white plastic knob by pulling it straight out. Next, remove the button-head screw located in the center of the cover. The cover will come off if it is pulled straight out.
4.3 TO CONNECT TO READ HEAD TERMINALS - Refer to figure 6. The contact terminals are eutectic silver with a. 045 hole to accommodate the contact wiring. When soldering wires to the terminals, a low wattage instrument soldering iron is suggested in the 47 1/2 watt range.

## CAUTION

EXCESSIVE APPLICATION OF HEAT WILL MELT THE CELCON TERMINAL BLOCK.

CHANNEL 1 HOLD-DOWN ARM


FIGURE 6 Read Head Wiring .

TO CONNECT THE DRIVE COIL AND INTERRUPTER SWITCH - Refer to Figure 7.


FIGURE 7 Reader Drive Wiring Connections
4.4 ARC SUPPRESSION - The recommended suppression (not supplied) is a diode and zener diode, back-to-back, as shown in Figure 7. The suppression is necessary for 30 CPS operation. For lower speeds, the zener may be omitted.

### 5.0 READ HEAD ADJUSTMENTS

5.1 READ HEAD POSITIONING - Ordinarily, the only time that a positioning adjustment is necessary is when a new read head is to be installed. During normal maintenance, all that is required is a visual inspection.

To adjust the read head position, refer to Figure 8. Adjust all "E" screws so that they do not limit the starwheel arms. Position the read head assembly so that the radius of the hold-down arm matches the radius of the sprocket wheel. Load a tape with a hole, no-hole pattern on the sprocket wheel with the no-hole character under the starwheels. Center the read head so that the starwheel is centered on the no-hole code. The two bottom teeth of the starwheel should be equidistant from the adjacent holes. The read head is fastened to the panel with three screws ("S" in Figure 8).


SAMPLE: Hole - No Hole Tape
5.2 STARWHEEL ARM TENSION - To adjust the starwheel arm tension, refer to Figure 8. With the read head in the proper position, measure the tension at point " $A$ " in the direction indicated by the arrow. With no tape under the starwheels, a force of 40-45 grams should be necessary, at point "A" to lift a starwheel arm so that the starwheel axle is above the adjacent starwheel arm.

Plate " $B$ " on Figure 8 is used to change the starwheel arm tension. Adjust plate " $B$ " so that the tension on starwheel arms one (1) and eight (8) are both equal.

### 5.3 COMMON BAR ADJUSTMENT - After aligning the read head and setting

 the starwheel arm tension, the next step is to set the gap between the contact wires and the common bar.With a blank tape (No-Hole pattern) under the starwheels, set the gap between the common bar and the contact wires ("C" in Figure 8) to . 010 using adjustment screws "D".
5.4 CONTACT BOUNCE ADJUSTMENT - Using a test tape with a hole, nohole pattern and an oscilloscope to observe the contact wave forms, adjust screw "E" for a minimum bounce condition. The maximum bounce allowable is 1 millisecond. Be sure to coat all adjustment screws with "Glyptal" to prevent them from losing the adjustment.


FIGURE 8 Read Head

### 6.0 REGISTRATION AND TAPE DRIVE ADJUSTMENTS

6.1 With a strip of "hole-no hole" tape (see sample) positioned over sprocket adjust the detent spring to position the sprocket wheel and tape under the starwheels so that the starwheels are centered equally between the two "hole" patterns.
6.2 Reverse movement of the ratchet wheel is prevented by the detent spring. Check that the detent spring engages with the drive face of the seventh tooth from the pawl hook. It must be adjusted as closely as possible but still be able to fall freely into its locking position. Spring pressure of the detent spring against the ratchet should be $3.5 \mathrm{oz} . \pm .5 \mathrm{oz}$. See Figure 9.
6.3 ARMATURE AND ARMATURE ARM BACK STOP - check that the armature operates freely without the armature arm riding on any part of the heel piece or the upper surface of the base plate. Adjust the back stop so that the pawl hook fully locates into the tooth of the ratchet without causing rotation of the ratchet away from its detented position. Check that the armature rests against the entire slanted surface of the armature back stop. Insert. 002 shim between armature and core and manually operate the armature. The pawl hook should engage the next tooth of the ratchet and, upon release of armature, istep the ratchet one tooth. With a . 006 shim the pawl hook should not engage the tooth. If manual operation does not result in stepping with .002 shim or permits stepping with .006 shim correct by supporting armature and adjusting armature arm accordingly.
6.4 PAWL HOOK - the tooth edge of the pawl hook must be parallel with the teeth on the ratchet wheel. Make adjustment if necessary by forming the armature arm where the pawl hook spring is assembled to the armature. The pawl hook must rest at the bottom of the engaged ratchet tooth and along entire width of the tooth. Spring pressure of the pawl hook against the ratchet should be 25-30 grams.
6.5 PAWL STOP - check that the pawl hookfits firmly between the pawl stop and the ratchet wheel with armature in non-operated position, to prevent overtravel of ratchet in excess of .002 . Arm of pawl stop must be parallel to pawl hook.
6.6 ARMATURE RETURN SPRING - adjust armature return spring tension for $14 \mathrm{oz} . \pm .5 \mathrm{oz}$. See Figure 9 for spring guage application. Measure at point where the tension of the spring guage causes motion of the armature.

NOTE: Approximately 18-22 oz. are required to lift the pawl hook over the


Adj. screw armature spring


FIGURE 9 Drive Mechanism Adjustments

### 6.7 INTERRUPTER SWITCH - CHECK FOR THE FOLLOWING CONDITIONS

 6.7.1 Interrupter pressure spring should be adjusted for $3.5 \mathrm{oz} . \pm .5 \mathrm{oz}$. Form spring as required.6.7.2 Contact force should be adjusted for 40-50 grams for contact break. Form the spring contact blade to adjust.
6.7.3 Contact centers within .020 .
6.7.4 The interrupter switch should open at approximately $80 \%$ of the upward stroke of the pawl.
6.7.5 The interrupter switch contacts should open $.010 \pm .002$ as shown in Figure 10.
6.7.6 The interrupter switch should be adjusted to maintain its memory. The armature extension arm fits through the rectangular hole in the actuator. The phenolic slide should open the interrupter switch with a sufficient amount of over-travel so that the switch will remain "open" when armature is energized. Check to assure switch closes when armature is released and phenolic slide is restored. Form armature extension arm to reposition actuator.

NOTE: Spring tension adjustments are illustrated in Figure 9. Note that arrows indicate the direction in which measurements are to be made.


FIGURE 10 Interrupter Switch Gap Adjustment
7.0 TAPE DRUM ASSEMBLY - To remove the tape drum assembly from the reader, use the following procedure:
7.1 Place the starwheels in the load or raised position.
7.2 Remove the Tape guide plates.
7.3 Remove the bearing plate and carefully pull the drum assembly forward.
7.4 Using a \#. 048 Bristol wrench, loosen the 3-48 Nylock socket screws located inside the shaft bearings.
7.5 Carefully replace the drum assembly.
7.6 Replace the bearing plate.
7.7 Using a \#. 048 Bristol wrench, adjust the 3-48 Nylock socket set screws to align the tape drum with the starwheel arms. The sprocket wheel should be centered on the hold-down arm of the read head. The tape drum shaft should have approximately .002 inches end play.
7.8 Replace the guide plates.
8.0 PREVENTIVE MAINTENANCE - Lubricate all points marked "L" on Figure 11 using CMC \#5 grease.
8.1 Keep the reader generally clean and free from paper dust. Use a fine burnishing tool to clean all electrical contacts. DO NOT BEND THE CONTACT WIRES IN THE READ HEAD. Avoid a heavy build-up of grease and dust on lubricated surfaces.


FIGURE 11 Lubrication Points

## IMPORTANT NOTE

COMPUTER MECHANISMS CORPORATION uses two drive systems on the Model 18 Tape Reader. These units appear identical but the PARTS ARE NOT INTERCHANGABLE. In order to identify the drive system on your reader, locate the part number on the drive coil. If this number has an."RCE"prefix, the reader has an " $E$ " type drive. If there is no prefix, the reader has an " $N$ ": type drive.

All spare or replacement parts are available from COMPUTER MECHANISMS CORPORATION, 493 Washington Avenue, Carlstadt, New Jersey 07072. Phone Area Code 201-438-1770. TWX \# 710-989-0111

| DESCRIPTION | PART <br> NUMBER | NUMBER REQUIRED |
| :---: | :---: | :---: |
| FULL READER HEAD ASSEMBLY | 18105 | 1 |
| Back Plate | 18067 | 1 |
| Adjustable cross block | 18070 | 1 |
| Cross bar | 18084 | 1 |
| Starwheel arm comb | 18071 | 1 |
| Contact bar | 18072 | 1 |
| Contact wire comb | 18085 | 1 |
| Spring wire comb | 18086 | 1 |
| Contact block | 18087 | 1 |
| Guard | 18074 | 1 |
| Front plate | 18068 | 1 |
| Eccentric shaft | 18078 | 1 |
| Spacer | 18060-1 | 1 |
| Starwheel arm | 18065 | 8 |
| Starwheel | 18053 | 8 |
| Hold-down arm | 18064 | 1 |
| Spacer | 18060-2 | 1 |
| Starwheel arm shaft. | 18066 | 1 |
| Knob | 18079 | 1 |
| Contact wire (Silver) | 18075 | 17 |
| Wire spring S/S . 015 Dia. | 18076 | 8 |
| Wire spring S/S . 028 Dia. | 18077 | 1 |
| Eccentric shaft limit guide | 18106 | 1 |
| Eccentric shaft limit | 18107 | 1 |
| Eccentric shaft limit spring | 18108 | 1 |
| Shims | 18109 | As Req'd |
| 4-40 X 1/4 Socket head cap screw |  | 2 |
| 4-40 X 3/8 Socket head cap screw |  | 4 |
| 4-40 X $5 / 8$ Socket head cap screw |  | 1 |
| 4-40 X 3/8 Button head cap screw |  | 2 |
| 4-40 X $1 / 4$ Flat head cap screw |  | 2 |
| 4-40 X 1/4 Socket set screw |  | 2 |
| \#4 Flat washer |  | 7 |


| DESCRIPTION | TYPE | PART \# | \# REQ'D |
| :---: | :---: | :---: | :---: |
| Main panel | - | 18056 | 1 |
| Groov-pin 5/64 X 3/8 Type 3 | - | - | 1 |
| Bearing block | - | 18092 | 1 |
| 6-32 X 3/8 Flat head socket cap screw | - | - | 1 |
| Insulation plate | - | 18059 | 1 |
| Base plate | N | 18102-N | 1 |
| Base plate | E | 18102-E | 1 |
| 4-40 X 5/16 Socket head cap screws | - | - | 2 |
| \#4 Flat washers | - | - | 11 |
| Heel piece, sub assembly | N | 531478 | 1 |
| Heel piece, sub assembly | E | 419002 | 1 |
| Back stop | N | 504218 | 1 |
| Back stop washer | N | 504250 | 1 |
| 4-40 X 1/4 Fillister head screw | N | 504261 | 1 |
| Back stop | E | 419017 | 1 |
| Back stop washer | E | 430507 | 1 |
| Back stop screw | E | EC5 3X6MO5 | 1 |
| Spring holder | N | 504221 | 1 |
| Spring holder screw | N | 504242 | 1 |
| Spring holder | E | 419008 | 1 |
| Spring holder screw | E | 420205 | 1 |
| Guide plate | - | 18098 | 2 |
| Drum and shaft assembly | - | 18103 | 1 |
| Front bearing plate assembly | - | 18104 | 1 |
| 6-32 X 3/8 Button head socket screw | - | - | 2 |
| 1/16 X . 410 Dowel pin | - | - | 2 |
| 3-48 X 5/32 Nyloc set screw | - | - | 2 |
| Detent spring | N | 504263 | 1 |
| Detent spring screw | N | 575926 | 1 |
| Detent spring washer | N | 562470 | 1 |
| Detent spring | E | 419009 | 1 |
| Detent spring screw | E | EC5 2.3X3 MO5 | 1 |
| Detent spring washer | E | \#3 washer | 1 |
| Armature | N | 504201 | 1 |
| Armature | E | 419051 | 1 |
| Spring | N | 504270 | 1 |
| Spring | E | 230931 | 1 |
| Pawl stop | N | 504224 | 1 |
| Pawl stop screw (4-40 X l/4 pan head) | N | - | 1 |
| Pawl stop | E | 419016 | 1 |
| Pawl stop screw | E | EC5 3X4.5 MO5 | 1 |
| Hex nut | N | 586947 | 1 |
| Hex nut | E | BGM-45-503 | 1 |
| Coil, 12 volt | N | 563921 | 1 |
| Coil, 24 volt | N | 563919 | 1 |
| Coil, 48 volt | N | 563918 | 1 |

DESCRIPTION
Coil, 12 volt
Coil, 24 volt
Coil, 48 volt
1 ohm resistor ( 12 volt)
4 ohm resistor ( 24 volt)
33 ohm resistor ( 48 volt)
Terminal strip
3-48 X 3/16 Pan head screw
4-40 X 3/8 Socket head screw
\#4 Internal star washer
Interrupter switch
Interrupter switch
Cover latch
4-40 X 3/16 Pan head screw
3/16 Cable clamp
4-40 Hex nut
Plastic cover
Cover spacer
Knob
Cover

TYPE PART \#
E RCE86107
E RCE86105
E RCE86104

-     - 
-     - 
-     - 
- 18110
-     - 
-     - 
-     - 

N 504378
E RBG2F601

- 18058 2
- $18058 \quad 2$
-     - 
-     - 
-     - 
- 18089
- 18101
- 18079
- 18090 1 1 1.

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TOOL
Hex Driver 3/32
Hex Driver 1/16
Hex Driver . 050
Hex Driver . 035

Bristol Driver . 096
Bristol Driver . 048

Gram Guage 10-80 Grams

Spring Scale 0-8 Ounces
Spring Scale 0-32 Ounces

Feeler Guage Set No. 66

Wrench, Open end, $1 / 4$ inch
Wrench, Open end, $3 / 8$ inch
Screwdriver, Common, $21 / 4 \mathrm{X} 1 / 8$
Screwdriver, Common, 3 X 7/32

## MANUFACTURER

Allen Manufacturing Co. Hartford, Connecticut

American Chain and Cable Co. Waterbury, Connecticut

Imtra Corp.
Cambridge, Massaschusetts

Chatillon Co.
New York, New York
L. S. Starrett Co.

Athol, Massachusetts
J. H. Williams and Co. Buffalo, New York
"

FIELD ENGINEERING
TECHNICAL MANUAL

$$
S P D^{T M} 10 / 20
$$

PERIPHERALS

## VOLUME II SPD-M MULTIPLEXER

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## FOREWORD

This manual provides the installation, theory of operation and maintenance procedures for the SPD-M Multiplexer. Field repair is accomplished by on-site replacement of a faulty module. Module repair is performed off-site by a technical staff with appropriate test equipment. An understanding of the theory provided in this manual and a familiarization with the logic diagrams provided in support document FS 003 will provide the required background for technical proficiency.


## CHAPTER I

## INTRODUCTION

### 1.1 GENERAL

The SPD-M Multiplexer is an INCOTERM product that complements the SPD 10/20 Stored Program Display. It provides the convenience and economy of interfacing a maximum of 16 Display Terminals with one communications modem. The appearance of the Multiplexer, shown in Figure 1-1, indicates a similar motif for this product as with the SPD 10/20 Terminal; namely, the absence of operator controls due to the stored program feature.

System expansion beyond 16 Display Terminals is possible by using cascaded multiplexers. This configuration is referred to as Master Multiplexer operation. Four multiplexers, servicing 16 Displays each, are connected to one Multiplexer called the Master. In this configuration, a total of 64 Displays can be interfaced.

### 1.2 INTERFACES

The SPD-M Multiplexer interfaces directly to modems such as the Bell Series 103, 202 and 201; CODEX AE-96; MILGO 440/48, or equivalent; or to any EIA RS 232-C compatible modems for all transmission speeds from 50 Baud to 4800 Baud. It operates in full or half duplex configurations, synchronously or asynchronously, and is transparent to all code patterns in both the transmit and receive modes. A Display Terminal may be placed up to

300 feet from the Multiplexer. The distance may be extended to 1000 feet by the use of an optional Communications Controller in the SPD 10/20

Display Terminal. Maximum separation between Multiplexers in the Master configuration is 50 feet.

The following standard EIA RS 232-C signals are included in the interface as required.

## Circuit - Description

AA - Protect<br>BA - Transmitted Data<br>BB - Received Data<br>CA - Request to Send<br>CB - Clear to Send<br>CC - Data Set Ready<br>AB - Signal Ground<br>DB - Transmitter Signal Timing Element<br>DD - Receiver Signal Timing Element<br>CD - Data Terminal Ready<br>CF - Received Line Signal Detector

### 1.3 OPERATION

The SPD-M Multiplexer is designed to operate in a single or multiple drop system environment with communication traffic controlled by a Central Processing Unit (CPU) oriented polling system. Data incoming to the site is supplied to all connected Terminals for address identification by the specific unit addressed. Site polling may be accomplished by use of a common address word assigned to all Terminals.

Message flow is controlled by both the CPU and the SPD-M. All messages originating from a Terminal await CPU authorization for transmission. Also, the Clear to Send lines connecting each Terminal and the SPD-M enable only one SPD 10/20 at a time.

The Multiplexer handles full duplex communication traffic. Usually, individual SPD 10/20 units will be connected to the SPD-M by half duplex lines, but full duplex operation of a single SPD $10 / 20$ is permitted if the SPD 10/20 is equipped with dual Communication Controllers.

## CHAPTER II

## INSTALLATION

2. 1 CABLING AND TESTING MULTIPLEXER INSTALLATIONS
2.1.1 Cabling the SPD-M Multiplexer

The Multiplexer installation which allows communication access for up to 16 Terminals, utilizing only one communication line, is illustrated in Figure 2-1, a simplified diagram.


Figure 2-1. Multiplexer Cabling

Observe that there is not a one-to-one correspondence between the Terminal 1 cable and the number of the Multiplexer jack it plugs into. Multiplexer jack 1 is cabled to the communications line; therefore, Multiplexer jacks 2 through 17 correspond to Terminals I through 16 for the purpose of cabling to ordered Terminals.

### 2.1.2 General Requirements for Multiplexer Testing

Equipment required for testing is listed below.

1. One Multiplexer (4, 8, 12 or 16 channels).
2. Three SPD $10 / 20$ Display Terminals (containing synchronous and keyboard controllers).
3. Modem Eliminator (set at 2400 Baud). See Appendix A.

Resident programs required for testing are listed below.

1. SPD Terminal A program requires that the Terminal is able to:
a. Initiate General Poll
b. Receive and display ASCII characters
c. Transmit displayed messages via Synchronous Controller.
2. SPD Terminal B programs assure that Terminal B's are able to:
a. Receive Poll/General Poll
b. Upon receiving Poll/General Poll, transmit message displayed on screen
c. Receive and display message via Synchronous Controller.

### 2.2 PROCEDURE



Test Set-Up

1. Load Terminal A Program
2. Modem Eliminator optioned to 2400 Baud. (Modem Eliminator will supply the proper Data Set interface signals to Terminal A and the MUX. ) Connect Modem Eliminator to Terminal A and JI of MUX.
3. Load Terminal B Programs.
4. Connect B Terminals to J2 and J3 of MUX.

### 2.2.1 Test l

1. Multiplexer optioned as follows:
a. For MUX operation (as opposed to Master MUX operation)
b. Synchronous operation
c. Non-priority sequencing
d. Cancels incorporated
e. Multiple transmission.
2. Write messages on the two $B$ Terminals and initialize transmit.
3. Enable the Polling sequence of Terminal A.
4. The two messages of the B Terminals will be displayed on screen of Terminal A.
5. Write message on screen of Terminal $A$ and transmit it to the two B Terminals. Both screens will display the message.
6. Repeat Steps 2 through 5, using all of the active MUX channels.

### 2.2.2 Test 2

1. Multiplexer optioned as follows:
a. MUX operation
b. Synchronous operation
c. Priority sequencing
d. Cancels incorporated
e. Multiple transmissions.
2. Repeat 2.2.1 Test 1, Steps 2 through 5. The results will be identical.

### 2.2.3 Test 3

1. Multiplexer optioned as follows:
a. MUX operation
b. Synchronous operation
c. Non-priority sequencing
d. Cancels incorporated
e. Single transmission.
2. Again repeat Steps 2. 2. 1 Test 1, Steps 2 through 5. In this case, only one message will be displayed when the poll is sent. Reenable the poll and the second message will be displayed.

## 2. 3 MASTER MULTIPLEXER CABLING

The following illustration (Figure 2-2) is a simplified diagram of Master Multiplexer cabling.


Figure 2-2. Master Multiplexer Cabling

## CHAPTER III

OPERATIONAL DESCRIPTION

### 3.1 PHYSICAL DESCRIPTION

The SPD-M Multiplexer measures 17 inches wide, 9 inches high, and 14 inches deep, and weighs 30 pounds. The bottom of the Multiplexer is a single piece of heavy gage sheet metal that serves as the chassis and structural member. Mounted on the chassis are the power supply, rear panel and printed circuit card rack (see Figure 3-1). The cover, which is removed in one piece, is an assembly consisting of the top, front panel and two side panels that are held together with screws and nuts. The cover is removed by loosening the three captive screws at the top of the rear panel and lifting it forward and upward to clear the front panel Power On indicator. The top of the cover is louvered and the front panel has a hole through which the blue lens of the indicator projects. When the cover is removed, an interlock switch deactivates the Multiplexer by cutting off the 115 V a.c. power.

The printed circuit card rack is mounted directly on the chassis and consists of a holder for eight printed circuit cards and an associated connector plate. Card-to-card wiring and card-to-I/O connector wiring is accomplished on the back plane of the connector plate. The interlock switch and indicator are mounted on the side of the card rack.

Spacers are used to mount the Power Supply to the chassis, which provides an air space between them.


B2114-22

Figure 3-1. Multiplexer With Top Cover Removed

The rear panel is mounted on two brackets which are attached to the chassis (see Figure 3-2). Mounted on the panel are a power switch, a. c. power receptacle, four fuses and I/O connectors (maximum of 17). In the minimum configuration, the Multiplexer contains five I/O connectors: No. 1 connects to the modem and Nos. 2 through 5 connect to the Terminals. System expansion is handled in increments of four; therefore, additional I/O connectors are provided on plates that contain four connectors each. The plates are installed in slots in the rear panel. Unused slots are filled with blank plates.

Depressing the Power switch to the ON position applies $115 \mathrm{~V}, 60 \mathrm{~Hz}$ power to the Multiplexer and illuminates the blue ( +5 VDC ) indicator on the front panel. A 2.5 A fuse is contained in the a. c. power line. The power supply d.c. outputs are fused as follows: 3A for the +5 output and 1.5A each for the +12 V and -12 V outputs.

### 3.2 FUNCTIONAL DESCRIPTION

### 3.2.1 General Operation

The SPD-M Multiplexer operates with a group of SPD 10/20 Terminals in a system that utilizes polling under control of the Central Processing Unit (CPU). The communication traffic is controlled by the CPU but message flow is controlled by both the Multiplexer and the CPU. All messages received by the Multiplexer from the CPU are transmitted to all Terminals via their Communications Controllers. The polling message envelope contains a functional double address: site address and Terminal address. The received site address must match the programmed site address; otherwise, no Terminals will respond. If the site address is verified, then the Terminal address is examined. It is usually in the form of a specific poll (specific Terminal address) or a general poll (all Terminals address). If a specific Terminal is addressed, only the selected Terminal will respond to the polling message. Three choices are possible in response to a general poll.


Figure 3-2. Multiplexer, Rear View

1. A No Data signal must be sent to the CPU from the site if no Terminal has data.
2. A Data signal or the data itself is sent by one Terminal only.
3. A Data signal or the data itself is sent by all Terminals that have data.
The polling speed is a function of the number of Terminals serviced and the speed of the modem. The polling operation is flexible and many variations are possible because of the programmable feature of the SPD 10/20 Terminal.

In addition to the features that allow Single or Master Multiplexer configuration with from 4 to 16 Terminals per multiplexer, several other options are available. Some options are the function of the number and type of Communications Controllers that are installed in the Terminal and some are the function of the hard-wired configuration of the option blocks installed in the Multiplexer Data Flow board. For details concerning these option blocks, refer to Appendix B in the Technical Manual for the SPD 10/20 Stored Program Display Terminal. The basic options are listed below.

1. Data can be synchronous or asynchronous.
2. Data word format can be 6, 7 or 8 -bits.
3. Transmission can be half or full duplex.
4. Data message transmission can be single or multiple mode.
5. Individual display transmissions can be synchronous or asynchronous (with synchronous system only).
6. Data can be priority or non-priority sequenced.

### 3.2.2 Functional Units

All the Multiplexer circuitry is contained on printed circuit boards. The basic configuration that interfaces four Terminals requires only four boards: one each Input Line Driver/Receiver, Data Flow, Summation and Output Line Driver/Receiver. These boards are shown in Figure 3-3. The maximum configuration that interfaces 16 Terminals requires one additional Summation board and three additional Line Driver/Receiver Output boards for a total of eight boards. Table 3-1 summarizes the board requirements for various configurations.


Line Driver Receiver Input


Summation


Data Flow


Line Driver Receiver Output

Figure 3-3. Multiplexer Circuit Board Complement

Table 3-1. Boards Required for Number of Terminals Used

| Board Type | 4 | $5-8$ | $9-12$ | $13-16$ |
| :--- | :---: | :---: | :---: | :---: |
|  | Terminals | Terminals | Terminals | Terminals |
| Input Line Driver/Receiver | 1 | 1 | 1 | 1 |
| Data Flow | 1 | 1 | 1 | 1 |
| Summation | 1 | 1 | 2 | 2 |
| Output Line Driver/Receiver | 1 | 2 | 3 | 4 |

A brief functional description of each unique board is given below. Figure
3-4 is a simplified block diagram of the Multiplexer.
Input Line Driver/Receiver - This board basically functions as a standard interface for the modem. It contains seven line receivers and three line drivers. One each of these circuits is used only in the Master Multiplexer configuration; therefore, only six line receivers and two line drivers are used in a single Multiplexer configuration. The line receiver translates the bipolar line levels $(+12 \mathrm{~V})$ used in the modem to the conventional logic levels ( 0 V and +5 V ) used in the Multiplexer. The line driver performs the translation in the other direction ( 0 V and +5 V to $\pm 12 \mathrm{~V}$ ). Both the drivers and receivers are dual-in-line IC packages. The inputs to the six line receivers come from the modem. Two receiver outputs are sent to the Data Flow board and four are sent to the Output Line Driver/Receiver board and then directly to the Terminal. The inputs to both line drivers come from the Data Flow board and their outputs go directly to the modem.

Data Flow - This board contains the Multiplexer timing and selection logic necessary to sequence the message handling associated with up to 16 Terminals. Basically, this board scans the Terminals and picks the first one that is requesting to transmit data. It returns a signal to the Terminal that allows it to transmit its message. When transmission is complete, this board again scans the Terminals to find the next one with data to transmit.

Summation - The data and the signal requesting transmission from each Terminal are sent to this board. Two boards are required to handle a full complement of 16 Terminals. All these signals are summed on this


Figure 3-4. Multiplexer Block Diagram
board and in conjunction with control signals from the Data Flow board allows communication between the modem and the selected Terminal.

Output Line Driver/Receiver - This board basically functions as an interface between the Multiplexer and Communications Controller in the Terminal. It has four identical sections: one for each Terminal. Each section contains seven line drivers and three line receivers. Two line drivers and one line receiver are used only in the Master Multiplexer configuration; therefore, only five line drivers and two line receivers are used in a single Multiplexer configuration. The line driver/receivers are the same type used in the Input board to perform bilateral signal translation between logic levels ( 0 V and +5 V to $\pm 12 \mathrm{~V}$ and vice versa).

## CHAPTER IV

## THEORY OF OPERATION

### 4.1 GENERAL

The theory of operation discussion is referenced to four schematic drawings which are logic diagrams for the four unique printed circuit boards. They are listed below.

Drawing Number
007-04-01, Sheet 2 Input Line Driver/Receiver Board
007-02-01, Sheet 2
007-01-01, Sheet 2 007-03-01, Sheet 2

Title

Data Flow Board
Summation Board
Output Line Driver/Receiver Board

The basic discussion deals with a single Multiplexer configuration. Any unique signals or circuits associated with Master Multiplexer operation are specifically mentioned in the discussion.

### 4.2 RECEIVE MODE

In the receive mode, four signals from the modem are sent to the Multiplexer and on to all Terminals with very little processing other than level translations. The signals enter the Input board (drawing 007-04-01) where they are given a level translation, double inversion and are sent to the Output board (drawing 007-03-01). The level translation ( +12 V to 0 V and +5 V ) is performed by a Cermetek type CM1160 Line Receiver which also
inverts the signal. The second inversion is performed by a type 7404 inverter. The signals and their paths through the Input board (drawing 007-04-01) are as follows:

1. RECEIVED DATA enters pin 9 of Line Receiver M6 and leaves via pin 4 of inverter M5 as the REC DATA signal.
2. RECEIVED LINE SIGNAL DETECTOR enters pin 6 of Line Receiver M6 and leaves via pin 6 of inverter M5 as the Carrier Detect (CD) signal. The signal is also picked off prior to entering M5 and is sent to the Data Flow board as CARRIER.
3. RECEIVER SIGNAL TIMING ELEMENT enters pin 6 of Line Receiver M7 and leaves via pin 8 of inverter M5 as the Serial Receive Clock signal (SRC).
4. TRANSMITTER SIGNAL TIMING ELEMENT enters pin 9 of Line Receiver M7 and leaves via pin 10 of inverter M5 as the Serial Transmit Clock (STC). The signal is also picked off prior to entering M5 and is sent to the Data Flow board as SERIAL CLOCK. These signals are used only in Master Multiplexer operation.
The four signals mentioned above, REC DATA, CD, SRC and STC are sent to the Output board (drawing 007-03-01) where each one is inverted and given a level translation ( 0 V and +5 V to $\pm 12 \mathrm{~V}$ ) by a Cermetek type CM1150 Line Driver and sent to the Terminal. Actually, after the first inversion, each signal is sent to four Line Drivers to provide a signal for the four Terminals serviced by the Output board. As an example, refer to drawing 007-03-01 to trace the path of the REC DATA signal. It enters pin 5 of inverter M9 and is sent to four Line Drivers: M18 pin 10, M18 pin 4, M20 pin 10 and M20 pin 4. The outputs of the Line Drivers go to four Terminals and are identified as REC DATA 1 through 4.

## 4. 3 TRANSMIT MODE

The communication traffic in a typical multiplexed Terminal configuration is controlled by a Central Processing Unit (CPU) using a polling system. The Terminals do not initiate any action on their own; they respond, positively or negatively, only to interrogation by the CPU.

The sequence of events starts with the transmission of a polling message by the CPU. The message path is from the CPU through the Modem to the Multiplexer and finally to all Terminals. Assume that the CPU transmits a general polling message. It is received by all Terminals and each one responds by transmitting a Request to Send (RTS) signal. Terminals that have no data to send indicate this fact by attempting to send an End of Transmission (EOT) signal which, in effect, is a No Data message. Terminals that have data to send provide a Transmit Data (XMIT DATA) signal to indicate this fact. These signals are sent to the Multiplexer to be processed so that the sequence of response by the Terminals can be determined and controlled.

A more detailed discussion of the Transmit mode is discussed in the following paragraphs.

Upon receipt of the general polling message from the CPU, all Terminals on line send a Request to Send (RTS) signal. All RTS signals are sent to a line receiver on the Output board. Each signal is inverted and translated to the conventional logic used in the Multiplexer (logic zero $=0 \mathrm{~V}$ and logic one $=+5 \mathrm{~V}$ ). All the enabled (low) RTS signals are sent to the Summation board (drawing 007-01-01). One board handles eight inputs; therefore, two boards are required for servicing nine to 16 Terminals. All eight RTS inputs, labeled RTSA through RTSH, are applied to the 8 -input gate M1. In any, or all, RTS inputs are enabled (low), Ml is enabled and its high output, $₹ R T S$, is sent to the Data Flow board (drawing 007-02-01). This signal enters the Data Flow board on pin 44 as $\sum$ RTSl and on pin 46 as \&RTS2 (if a second Summation board is used). The numerals 1 and 2 in the signal designation differentiate between the two Summation boards used if the system has more than eight Terminals. The ₹RTS is sent out as RTS via gate M4, pin 8 to line driver M2, pin 10 on the Input board (drawing 007-04-01). Line driver M2 inverts the signal and converts the level from convential logic $(0 \mathrm{~V}$ and +5 V ) to the ELA RS $232 \mathrm{~B} / \mathrm{C}$ levels ( $\pm 12 \mathrm{~V}$ ) used in the modem. The signal is sent to the modem as REQUEST TO SEND. The ₹RTS input to the Data Flow board also passes through a delay circuit ( $Q_{1}, C 1$ and $R 2$ ) and sets
latch M13 (pin 8 low) so that gate M16, pin 1 is enabled high. The output of M16 is inverted at Mll which provides the enabling signal (low) to Selector M3. Signal $\leqslant R T S$ is delayed approximately one character time to allow all Terminals to become operational (send an RTS) and insure that no Terminal that has data to send is skipped.

Selector M3 is a type 74154 four-line-to-16-1ine decoder. It decodes four binary-coded inputs (A, B, C and D) into one of 16 mutually exclusive outputs when both strobe inputs G1 (pin 18) and G2 (pin 19) are low. Outputs 1 through 8 are sent to one Summation board and are labeled SELA through SELH; outputs 9 through 16 are sent to the other Summation board (if used) and are labeled SELA ${ }^{1}$ through SELH ${ }^{1}$. The inputs are provided from the Qoutputs of the Asynchronous Divide By 16 Up Counter that is constructed with two type 7476 dual J-K flip flops M2 and M7. The counter is clocked by the high speed clock (M14 and discrete components C3, C4, R8 and R9) shown in the bottom left section of drawing 007-02-01. The counter is enabled and disabled by inverter M14, pin 12; it can be reset to a zero count (cleared) by the $\leqslant$ RTS input signal. These functions are discussed in detail in subsequent paragraphs.

As a simple example, assume that an eight Terminal configuration has been polled and that Terminal $D$ is the first detected to have data to send. Signal $£ R T S$ is detected and selector $M 3$ is enabled. The counter ( $M 2$ and M7) is enabled and is counting. When the counter state reaches the unique condition corresponding to selector output 3 (pin 4 of M3), that output (SEL D) is enabled (low). Signal SEL D is sent to pin 3 of gate M5 on the Summation board where it is ANDed with RTS D to enable M5, pin 1. The other gates in this group are not enabled at this time because none of the other SEL signals are enabled. The high output from pin 1 of M5 is sent directly to four gates. It is sent to M6 pin 1 where it is ANDed with a high GOXMIT signal from inverter M7 pin 12. The gate is enabled and produces a low CTSD signal, which is the Clear to Send signal for Terminal D. This signal is sent to a line driver on the Output board and on to Terminal D. The out-
put of M5 pin 1 is also sent to pin 5 of M17 where it is inverted and sent as low signal (RTS) (SELECTED) to the Data Flow board. The third destination for the output of M5 pin 1 is pin 9 of gate M18. Terminal D has data to send so signal DATA D is enabled (low). It is inverted by M15 and applied to pin 10 of gate M18. Gate M18 is enabled and produces a low (RTS) (SELECTED) (DATA) signal which is sent to the Data Flow board. The DATA D signal is also sent to pin 5 of gate M3 prior to being inverted. This low input enables gate M3 and sends the $£$ DATA signal to the Data Flow board which indicates that at least one Terminal has data to send. The non-inverted (low) DATA D signal is also sent to pin 4 of gate M16 via option block STBll. This gate is a 3-input NAND. The fourth destination for the output of M5 pin 1 is pin 9 of inverter M19 where it is inverted and sent (as a low signal) to pin 3 of gate M16. Pin 5 of gate M16 is connected to pin 12 of M20 which inverts the CANCEL B signal from the Data Flow board. This signal is a function of all Terminals that have data and the Terminal selected. It is enabled low so that after inversion it is applied as a high signal to pin 5 of M16 (and all other gates in this group). The low inputs to pins 3 and 4 of M16 disable it; therefore, the output (pin 6) is high. This signal is sent to pin 1 of gate M8 where it is ORed with a high on pin 2 to disable M18 and inhibit generation of the Cancel signal CAN D. The high signal on pin 2, which is sent to all other gates in this group, is the inversion of CANCEL A from pin 2 of M7. Signal CANCEL A is generated on the Data Flow board only when the last Terminal with data has been detected. When enabled, it enters M7 pin 1 as a high signal. At this time, it is not enabled and a Cancel signal is not generated which is the case for a Terminal that has data to send. If all jumpers are installed in option block STBll, the DATA signals can be used to inhibit the Cancel signals. If no jumpers are installed, the (RTS) (SELECTED) signals are used to inhibit the Cancel signals.

After a transmit sequence has been executed, the selector (M3) is disabled if no RTS signals are present. It is disabled via high conditions at M13 pin 8 and a low from option block STBIO, resulting in a high signal to its
strobe input G2. In this condition, all selector outputs are high which is the disable state for all Select (SEL) signals. The selector inputs are a function of the counter (M2 and M7) and when it is enabled again it will select whatever Terminal is represented by the existing counter state. An option is provided via option block STB12, pins 3 and 14, to allow random selection or priority selection. Without the jumper, the counter is disabled via the $J$ and K -inputs of its first flip flop M2. This action is initiated by the dropping of RTS which also disables the selector which is now waiting to select the next Terminal in sequence when it is enabled again. This is considered random selection. In priority selection, the STB12 jumper is installed and the RTS signal (low) is used to clear the counter to the zero state. When the next sequence starts, the selector picks up at output 0 which is priority 1 and continues down the line to the last output (15).

In normal operation, the CPU is polling continuously so that RTS signals from the Terminals are generated at frequent intervals. Under these conditions, procedures other than dropping the RTS signals are used to stop the selector at the proper time during the sequencing operation. One method is used when no Terminal has data to send. This situation results in a low §DATAl signal on pin 62 of the Data Flow board (drawing 007-02-01). A Terminal has been selected but no data is available so (RTS) (SELECTED) 1 on pin 61 is enabled (low) and (RTS) (SELECTED) (DATA) 1 on pin 65 is disabled (high). The £DATAl signal is inverted by M8 and applied to pin 13 of gate M5. The (RTS) (SELECTED) l signal is inverted by M4 and applied to the other input (pin 12) of gate M5. Both these signals are high and M5 is enabled. The low output ( pin 11 ) of M5 is applied to pin 10 of M5 which is another gate in this IC. The high (RTS) (SELECTED) (DATA) 1 signal is sent to pin 9 of M5. The gate is enabled and the high output is sent to pin 3 of inverter M4. The inverted isgnal from pin 4 of M 4 is sent to pin 2 of gate M19. This disables M19 and the resulting high output is inverted by MIl and the J and K inputs of flip flop M2 are both held low. This disables the flip flop which in turn inhibits the counter and effectively stops the selector (M3). The operational sequence is completed by sending a GOXMIT
signal to the selected Terminal. The Terminal responds with an EOT that is essentially a No Data signal.

The other method used to stop the selector (M3) at the proper time is applicable when a Terminal has data to send. The desired result is to stop the selector right after selecting the Terminal that has data to send. In response to a polling message, all Displays send an RTS and those having data also generate an XMIT DATA signal which is sent to the Summation board and on to the Data Flow board as the ミDATA signal. At the start of the sequence, the £DATA 1 signal is enabled (high) but the (RTS) (SELECTED) 1 and (RTS) (SELECTED) (DATA) 1 signals are not yet enabled because the Terminal has not been selected; therefore, both signals are high. The enabled DATA 1 signal is inverted by M8 (low) and sent to pin 13 of gate M5. The (RTS) (SELECTED) 1 signal, which is high, is inverted by M4 and sent to pin 12 of gate M5. The enabled (high) output of M5 (pin 11) is sent to pin 10 of OR gate M5. The high (RTS) (SELECTED) (DATA) l signal is sent to the other input (pin 9) of this gate. The output (pin 8) is low and is sent to pin 3 of inverter M4. After inversion, it is sent to pin 2 of gate M19. This same M5 output (pin 8) is also sent to pin 4 of M19 which is another gate in this IC. Being a low signal, it disables M19 and its high output (pin 6) is sent to pin 8 of M15. The other input (pin 9) of M15 is the high (RTS) (SELECTED) 1 signal which also is connected to the K -input (pin 16) of lip flop M20. The two high inputs at M15 enable it and the low output (pin 10) is sent to the J-input (pin 4) of flip flop M20. The inputs of flip flop M20 are $\mathrm{J}=0$ and $\mathrm{K}=1$, which keep it in the reset condition (pin $15=0$ and pin $14=1$ ). The high signal from pin 14 is sent to pin 13 of gate M19, which along with the high inputs on pins 1 and 2, enable the gate. The output of M19 (pin 12) enables the counter via inverter M11. The selector is enabled by the ₹RTS 1 signal so it selects the Terminal that has data to send. Via the logic on the Summation board, (RTS) (SELECTED) 1 and (RTS) (SELECTED) (DATA) 1 are enabled (low). These signals now enable gate M5. Its high output (pin 8) is inverted by M4 and sent to pin 2 of gate M19. The high output (pin 12) of M19 inhibits the counter.

The output of M5 (pin 8) is also sent to pin 4 of M19. The other two inputs to this gate are also high: pin 3 from the $\bar{Q}$ output of M20 in the reset state; and pin 5 which is the inverted Clear to Send (CTS) from board pin 58. These three high signals enable M19 and its low output (pin 10) is sent to pin 8 of M15. The other input (pin 9) to this gate is the low (RTS) (SELECTED) 1 signal. These two low signals force the output (pin 10) high and it is sent to the K-input of M20. Now, with the J-input high and the K-input low, the next clock pulse sets flip flop $M 20(Q=1$ and $\bar{Q}=0)$. The $\bar{Q}$ output (pin 14) of M20 is fed to pin 13 of gate M19 which represents an inhibiting input. The $\bar{Q}$ output is also fed to pin 3 of gate M19 which forces its output high and that in turn forces the output of M15 low. Both the J and K inputs of M20 are now zero so subsequent clock pulses have no effect on its state. With the counter inhibited, the selector is effectively stopped and the selected Terminal transmits its data and drops its RTS which forces (RTS) (SELECTED) 1 and (RTS) (SELECTED) (DATA) 1 high and DATA low. These signals now force the output (pin 8) of OR gate M5 low which re-establishes an enabling input at pin 2 of M19. The output ( pin 6 ) of M19 is now high and along with the high (RTS) (SELECTED) 1 signal enables M15. The inputs to flip flop are now $J=0$ and $K=1$ so that the next clock pulse reset it ( $Q=0$ and $\bar{Q}=1$ ). The $\bar{Q}$ output (pin 14) is sent to pin 13 of M19. With the arrival of the next RTS signal, this gate is enabled via OR gate M13 which starts the counter. The $\bar{Q}$ output (pin 14) is also sent to pin 3 of M19 which does not change its output; therefore, M20 remains in the reset condition. The selection logic (M5, M19, M13, etc.) is now conditioned to process another sequence that starts with the raising of a RTS signal.

The CANCEL A and CANCEL B signals used on the Summation board are generated on the Data Flow board. CANCEL $A$ is generated only when the last Terminal to transmit is detected. In all other cases, CANCEL B is used. A CANCEL signal and a CLEAR TO SEND signal are both required by a Terminal to condition it for sending an EOT signal at the end of a data message or immediately after the Multiplexer responds to its RTS if no data is to be transmitted. In operation, CANCEL B generates a Cancel signal (CAN)
for all Terminals except the selected one. If the selected Terminal is the last one, CANCEL B cannot generate a CAN signal but CANCEL A can, if it is enabled.

CANCEL A is generated at gate M15 on the Data Flow board (drawing 007-02-01). It is inverted by M4 and sent to the Summation board: it is enabled in the high state. The selection circuitry, M5, M15, M19 and M20, and latch M18 control the generation of CANCEL A. CANCEL B is enabled low and is picked off the $\bar{Q}$ output (pin 14) of flip flop M20.

Another signal, GOXMIT, is generated on the Data Flow board and is sent to the Summation board to enable the Clear To Send (CTS) signals. The logic for generating the GOXMIT signal is shown on the lower right section of drawing 007-02-01. The GOXMIT signal is generated after the SEL and (RTS) (SELECTED) signals are enabled. Pin 8 of gate M26 is enabled (low) when its three input signals are high. The signals are: high speed clock ( pin 9 ); RTS after delay ( pin 12 ); and Time Zero from the sync counter (M1 and M6). When these inputs are all high, M26 is enabled (low) and its output is inverted by M11 and sent to pin 4 of AND gate M25 and pin 3 of AND gate M24. With (RTS) (SELECTED) enabled, pin 5 of M25 is low and the gate output (pin 6) is high. This output signal (pin 6) is fed to pin 5 of gate M24 where it is ANDed with the high signal from inverter Mll and the high (Q) output (pin 15) from flip flop M20. Gate M24 is enabled (low) and its output is inverted by M11 (pins 8 and 9) and is used to clock flip flop M17 which has fired inputs ( $\mathrm{J}=1$ and $\mathrm{K}=0$ ). The next clock pulse sets flip flop M17 and its Q output (pin 15) is sent through STB 10 to pin 13 of gate M24, where it is ANDed with the SERIAL CLOCK and $\overline{C T S}$ signal to generate the GOXMIT signal.

Some of the logic used to generate the GOXMIT signal is as sociated with the synchronizing logic which consists basically of gates M16, M23, M24 and M25, and the sync counter (M1 and M6). When the data set is of the synchronous type, the Multiplexer generates a pulse derivative of the high speed internal clock (approximately 2 MHz ). The pulse is produced on either the
leading or trailing edge, depending on whether operation is synchronous or asynchronous. If the data and transmission is synchronous, the Multiplexer provides the clock. If the data is synchronous but transmission is not, the clock is not needed. In the case of asynchronous data, the clock must be supplied.

In synchronous operation, data is transmitted at a specific rate, as is asynchronous data. However, no breaks in the data train are allowed. This operation then requires the transmission of some coding at the beginning and end of a synchronous data message so the receiving station can set its circuits (synchronize) in preparation for data reception. The transmitting Terminal message is an 8 -bit data train. On the trailing edge of the eighth bit, the Request to Send drops, which provides the signal to the Synchronous Counter (M1 through M6) and the fill-in character is generated. The counter sequentially produces seven l-bits and one zero bit until the next message block is ready. The fill-in pattern thus maintains ODD parity. When the next message is available, the sync counter stops after the seventh bit, resets itself, and enables the data path. The counting operation of the circuit can be altered for 6,7 and 8 bit data by specific jumper wires at STB10. Gates M23, 24, 25 and 26 are interconnected to provide a latch flip flop function which toggles the operation of either providing data or fill-in characters at M23, pins 8 or 11. Either M23 pin 6 enables M23 pin 9 or M24 pin 8 enables M23 pin 12. Control of the toggling action is dependent on the three input signals at AND gate M26, pins 9, 10 and 12. Pin 9 is enabled by the internal clock. The clock feed can be optioned at STB2l for the normal high speed output or a subdivision of this rate provided as a decode of flip flops M27, performed at M25. The signal at pin 12 , M26 is the delayed RTS and the pin 10 input is the sync counter decode of zero. With the inputs Conditioned, the output (pin 8) is fed through a 7404 inverter, M11, and two AND gates, M25 and M24. Gate M25 pin 5 is enabled only when a Request to Send is enabled. The low at M25 pin 6 inhibits M24 pin 5 and resets the Clear to Send (GOXMIT) flip flops M17. The same ANDing situation is pre-
sent at M26 for fill-in characters generation. However, the path is now gate M24. M25 pin 6 goes high when (RTS) (SELECTED) drops. This signal enables pin 5 M24. The third input (pin 4) is supplied by control flip flop \#1 (M20 pin 15) going true. The conditions at M24 result in the starting of turn of circuits M17 in preparation for transmitting synchronizing data. The toggling circuit must be controlled by a specific timing so that actual Terminal data is not random or asynchronous with respect to the fill-in data. The proper control is a function of the clock pulse and Request to Send. At the proper time the RTS with data produces a signal at pin 6, M24, which is one clock pulse wide. The pulse is tied to the clock input of M17 and sets the first flip flop. Only when the $Q$ side (M17 pin 15) is set will the selected Terminal be sent a Clear to Send (GOXMIT). Options available at the STB10 input to AND gate M24 provide for synchronous or asynchronous operation. At STB10 the serial clock can be ANDed with the XMIT clock and Clear to Send signal. This ability provides a major difference between normal data set operation and operation with a Multiplexer. Effectively, two of the basic signals in the data set are ANDed, resulting in the synchronous clocks and Clear to Send being transmitted on the same line. The option is not wired in for asynchronous operation.

The next full character time after setting M17 \#1, the counter is again 0, (RTS) and ( RST) (DATA) are present and M17 \#2 is strobed. One character time later the same events occur and the latch is reset, allowing an open data line. The above sequence is a specific example of synchronous operation. Normal synchronous transmitted data is preceeded by three or more sync characters which set the receiver to accept the data.

When asynchronous data is transmitted, two different source clocks are involved and the requirement is that they be very closely matched. The transmission of asynchronous data through synchronous data sets requires that one character follow another. Synchronous characters (front and back) are not required, but breaks in data are not allowed.

### 4.4 POWER SUPPLY OPERATION

The SPD-M obtains operating voltages from a Trygon Model TP3E transistorized power supply. The suceeding paragraphs reference the schematic Figure 4-1.

The a. c. - input voltage applied to Terminal strip lugs 1 and 2 can range from 105 to 125 volts a.c. Input voltage frequency can be from 47 to over 62 HHz . The power transformer Tlll primarily feeds three separate secondary windings. Each secondary is full wave rectified to obtain the three d. c. outputs:

> +A is +3.5 to $+5.5 @ 0$ to 6.0 amperes
> +B is +10 to +25 @ 0 to 1.8 amperes
> -C is -5 to -16 @ to 1.5 amperes.

The + A output circuit utilizes a series pass transistor Q101, which is controlled by circuit A.2, a solid state error sensing amplifier. The error signal is developed by a comparison voltage and the actual A2 output dropped across variable divider R40, R41 and R42. Short circuit protection is provided by sensing a voltage drop across R23/R33. The voltage drop, in combination with variable resistor R32, biases Q10 and in case of overload will limit the drive available from circuit A2.

The $+B$ output circuit path is through series pass transistor Q102. The control circuit is an operational amplifier designated A1. The operational amplifier compares a reference voltage level with the output level by means of variable voltage divider R16, R13 and R15. The amplifier output biases Q3, which, in turn, controls the pass transistor. Short circuit protection is provided by sensing the voltage drop across R7/R8. The voltage developed in event of a short circuit or overload biases Q4, which cuts off driver Q3.

Output C is routed through series pass transistor Q103. This regulating circuit is entirely composed of discrete components. Voltage comparisons are made with reference and output voltages through the variable divider network consisting of R61, R62 and R63. Short circuit protection is provided by detecting the voltage drop across current sensing resistor R55/R66. *This supply can operate at 400 Hz with a $15 \%$ power derating.

The resulting voltage operates $Q 15$, which diverts the drive current from the amplifier.


CHAPTER V<br>MAINTENANCE AND REPAIR

### 5.1 GENERAL

The physical layout of the Multiplexer, as illustrated in Figure 3-1, is somewhat modified if operation is contemplated with a 230 Volt a c line input. Figure 5-1 relates the physical orientation of the 230 Volt input transformer. The input leads can be selected to accomodate a wide range of input voltages. The input voltages are transformed to the operating voltage for the power supply (115 Volts). Figure 5-1 also relates the position of jacks on the connector panel. Since there can be up to 17 connectors on the panel, the card cage designations start with the number 18 and proceed through 25. Table 5-1 lists the internal connector wiring and signal designations. When viewed from the wire wraped side of the PC connectors, the even pins are on the right of each connector and odd pins are on the left. Pin \#1 then, is on the top right of each circuit card connector. Table 5-2 lists the Power distribution wiring.


Figure 5-1 Multiplexer, 230 Volt Operation And

Table 5-1. Internal Signal Wiring

|  | WIRED |  |  |
| :---: | :---: | :---: | :---: |
| Nmemonic | Definition | From | To |
| D/ND | Data/No Data | Jack 18 Pin 22 | Jack 19 Pin 48 |
| XMIT DATA | Transmit Data | Jack 18 Pin 16 | Jack 19 Pin 8 |
| RTS | Request to Send | Jack 18 Pin 32 | Jack 19 Pin 56 |
| CAN \& DSR | Cancel and |  |  |
|  | Data Set Ready | Jack 18 Pin 52 | Jack 19 Pin 80 |
| LTS | Last to Send | Jack 18 Pin 62 | Jack 19 Pin 67 |
| CTS | Clear to Send | Jack 18 Pin 68 | Jack 19 Pin 58 |
| STC | Serial Transmit |  |  |
|  | Clock | Jack 18 Pin 30 | Jack 22 Pin 4 |
| CD | Carrier Detect | Jack 18 Pin 34 | Jack 22 Pin 8 |
|  |  | Jack 22 Pin 8 | Jack 23 Pin 8 |
|  |  | Jack 23 Pin 8 | Jack 24 Pin 8 |
|  |  | Jack 24 Pin 8 | Jack 25 Pin 8 |
| REC DATA | Received Data | Jack 18 Pin 36 | Jack 22 Pin 6 |
|  |  | Jack 22 Pin 6 | Jack 23 Pin 6 |
|  |  | Jack 23 Pin 6 | Jack 24 Pin 6 |
|  |  | Jack 24 Pin 6 | Jack 25 Pin 6 |
| SRC | Serial Receive |  |  |
|  | Clock | Jack 18 Pin 28 <br> Jack 22 Pin 10 | Jack 22 Pin 10 <br> Jack 23 Pin 10 |
|  |  | Jack 23 Pin 10 | Jack 24 Pin 10 |
|  |  | Jack 24 Pin 10 | Jack 25 Pin 10 |
| SERIAL CLOCK | Serial Clock | Jack 18 Pin 67 | Jack 19 Pin 73 |
| CARRIER | Carrier | Jack 18 Pin 44 | Jack 19 Pin 10 |
| £ RTS | Summation of Request to Send | Jack 19 Pin 44 |  |
| RTS SELECTED 1 | Request to Send Selected (not more than eight Terminals) | Jack 19 Pin 61 | Jack 20 Pin 4 |
| £ DATA 1 | Summation of Data (not more than eight Terminals) | Jack 19 Pin 52 | Jack 20 Pin 41 |
| (RTS)(SEL)(DATA) 1 | Request to Send Selected with Data (not more than eight Terminals) | Jack 19 Pin 65 | Jack 20 Pin 60 |
| CANCEL Bl | Cancel B (not last Terminal and not more than eight Te | Jack 19 Pin 69 erminals) | Jack 20 Pin 79 |
| CANCEL Al | Cancel A (last to send in group of Terminals not mor | Jack 19 Pin 63 <br> e than eight) | Jack 20 Pin 59 |

Table 5-1. Internal Signal Wiring Cont'd.

| Nmemonic | WIRED |  |  |
| :---: | :---: | :---: | :---: |
|  | Definition | From | To |
| GO XMIT 1 | Go Transmit (not more than eight Terminals) | Jack 19 Pin 77 | Jack 20 Pin 39 |
| SEL H | Select Terminal H (eighth Terminal) | Jack 19 Pin 28 | Jack 20 Pin 28 |
| SEL A | Select Terminal <br> A (first Terminal) | Jack 19 Pin 30 | Jack 20 Pin 7 |
| SEL B |  | Jack 19 Pin 32 | Jack 20 Pin 26 |
| SEL C |  | Jack 19 Pin 34 | Jack 20 Pin 9 |
| SEL D |  | Jack 19 Pin 36 | Jack 20 Pin 24 |
| SEL E |  | Jack 19 Pin 38 | Jack 20 Pin 5 |
| SEL F |  | Jack 19 Pin 40 | Jack 20 Pin 3 |
| SEL G |  | Jack 19 Pin 42 | Jack 20 Pin 30 |
| RTS A | Request to Send (Terminal A) | Jack 19 Pin 68 Jack 20 Pin 13 | Jack 20 Pin 13 Jack 22 Pin 30 |
| RTS B | Request to Send (Terminal B) | Jack 19 Pin 70 Jack 20 Pin 21 | Jack 20 Pin 21 Jack 22 Pin 44 |
| RTS C | Request to Send (Terminal C) | Jack 19 Pin 72 <br> Jack 20 Pin 10 | Jack 20 Pin 10 Jack 22 Pin 64 |
| RTS D | Request to Send (Terminal D) | Jack 19 Pin 74 Jack 20 Pin 23 | Jack 20 Pin 23 <br> Jack 22 Pin 72 |
| £ RTS 2 | Summation of Request to Send (more than eight Terminals) | Jack 19 Pin 46 | Jack 21 Pin 11 |
| (RTS) SELECTED 2 | Request to Send Selected (more than eight Termina | Jack 19 Pin 62 ls) | Jack 21 Pin 4 |
| £ DATA 2 | Summation of Data (greater than eight Terminals) | Jack 19 Pin 50 | Jack 21 Pin 41 |
| (RTS)(SELECTED) <br> (DATA) 2 | Request to Send Selected with Data | Jack 19 Pin 66 | Jack 21 Pin 60 |
| CANCEL B2 | Terminal Cancel | Jack 19 Pin 71 | Jack 21 Pin 79 |
| CANCEL A2 | Last Terminal Cancel | Jack 16 Pin 64 | Jack 21 Pin 59 |
| GO XMIT 2 | Go Transmit (more than eight Terminals) | Jack 19 Pin 79 | Jack 21 Pin 39 |
| SEL A' | Select First <br> Terminal in second group of eig ie. the ninth Term | Jack 19 Pin 26 <br> hht, <br> inal | Jack 21 Pin 7 |

Table 5-1. Internal Signal Wiring Cont'd.

| Nmemonic | WIRED |  |  |
| :---: | :---: | :---: | :---: |
|  | Definition | From | To |
| SEL B' |  | Jack 19 Pin 24 | Jack 21 Pin 26 |
| SEL C' |  | Jack 19 Pin 22 | Jack 21 Pin 9 |
| SEL ${ }^{\prime}$ |  | Jack 19 Pin 12 | Jack 21 Pin 24 |
| SEL E' |  | Jack 19 Pin 14 | Jack 21 Pin 5 |
| SEL $\mathrm{F}^{\prime}$ |  | Jack 19 Pin 16 | Jack 21 Pin 3 |
| SEL G' |  | Jack 19 Pin 18 | Jack 21 Pin 30 |
| SEL H ${ }^{\prime}$ |  | Jack 19 Pin 20 | Jack 21 Pin 28 |
| 1 RTS | One Request to Send | Jack 19 Pin 78 | Jack 22 Pin 26 |
| RTS E | Request to Send Terminal E | Jack 20 Pin 8 | Jack 23 Pin 30 |
| RTS F |  | Jack 20 Pin 6 | Jack 23 Pin 44 |
| RTS G |  | Jack 20 Pin 22 | Jack 23 Pin 64 |
| RTS H |  | Jack 20 Pin 16 | Jack 23 Pin 72 |
| CTS A | Clear to Send Terminal A | Jack 20 Pin 38 | Jack 22 Pin 18 |
| CTS B |  | Jack 20 Pin 34 | Jack 22 Pin 13 |
| CTS C |  | Jack 20 Pin 44 | Jack 22 Pin 27 |
| CTS D |  | Jack 20 Pin 48 | Jack 22 Pin 61 |
| CTS E |  | Jack 20 Pin 36 | Jack 23 Pin 18 |
| CTS F |  | Jack 20 Pin 46 | Jack 23 Pin 13 |
| CTS G |  | Jack 20 Pin 50 | Jack 23 Pin 37 |
| CTS H |  | Jack 20 Pin 32 | Jack 23 Pin 61 |
| CAN A | Cancel Terminal A | Jack 20 Pin 67 | Jack 22 Pin 12 |
| CAN B |  | Jack 20 Pin 69 | Jack 22 Pin 07 |
| CAN C |  | Jack 20 Pin 71 | Jack 22 Pin 27 |
| CAN D |  | Jack 20 Pin 73 | Jack 22 Pin 55 |
| CAN E |  | Jack 20 Pin 77 | Jack 23 Pin 12 |
| CAN F |  | Jack 20 Pin 63 | Jack 23 Pin 7 |
| CAN 9 |  | Jack 20 Pin 65 | Jack 23 Pin 27 |
| CAN H |  | Jack 20 Pin 61 | Jack 23 Pin 55 |
| DATA A | Data Detected A | Jack 20 Pin 45 | Jack 22 Pin 34 |
| DATA B |  | Jack 20 Pin 43 | Jack 22 Pin 50 |
| DATA C |  | Jack 20 Pin 57 | Jack 22 Pin 68 |
| DATA D |  | Jack 20 Pin 55 | Jack 22 Pin 78 |
| DATA E |  | Jack 20 Pin 53 | Jack 23 Pin 34 |
| DATA F |  | Jack 20 Pin 51 | Jack 23 Pin 50 |
| DATA G |  | Jack 20 Pin 49 | Jack 23 Pin 68 |
| DATA H |  | Jack 20 Pin 47 | Jack 23 Pin 78 |

Table 5-1. Internal Signal Wiring Cont'd.

|  | WIRED |  |  |
| :---: | :---: | :---: | :---: |
| Nmemonic | Definition | From | To |
| TDA DATA/NO DATA 1 | Transmitted Data/ No Data (master MUX operation) | Jack 20 Pin 52 | Jack 22 Pin 9 |
| TDB DATA/NO DATA 2 | Transmitted Data/ No Data (master MUX operation) | Jack 20 Pin 54 | Jack 22 Pin 5 |
| TDC DATA/NO DATA 3 | Transmitted Data/ <br> No Data (master <br> MUX operation) | Jack 20 Pin 56 | Jack 22 Pin 57 |
| TDD DATA/NO DATA 4 | Transmitted Data/ No Data (master MUX operation) | Jack 20 Pin 58 | Jack 22 Pin 53 |
| RTS A' | Request to Send (first Terminal over eight, ie. Terminal \#9) | Jack 21 Pin 13 | Jack 24 Pin 42 |
| RTS $\mathrm{B}^{\prime}$ |  | Jack 21 Pin 21 | Jack 24 Pin 44 |
| RTS C' |  | Jack 21 Pin 10 | Jack 24 Pin 64 |
| RTS ${ }^{\prime}$ |  | Jack 21 Pin 23 | Jack 24 Pin 72 |
| RTS E' |  | Jack 21 Pin 8 | Jack 25 Pin 30 |
| RTS $\mathrm{F}^{\prime}$ |  | Jack 21 Pin 6 | Jack 25 Pin 44 |
| RTS G ${ }^{\prime}$ |  | Jack 21 Pin 22 | Jack 25 Pin 64 |
| RTS H' |  | Jack 21 Pin 16 | Jack 25 Pin 72 |
| CTS A' | Clear to Send (first Terminal over eight, ie. Terminal \#9) | Jack 21 Pin 38 | Jack 24 Pin 18 |
| CTS B' |  | Jack 21 Pin 34 | Jack 24 Pin 13 |
| CTS C ${ }^{\prime}$ |  | Jack 21 Pin 44 | Jack 24 Pin 37 |
| CTS ${ }^{\prime}$ |  | Jack 21 Pin 48 | Jack 24 Pin 61 |
| CTS E' |  | Jack 21 Pin 36 | Jack 25 Pin 18 |
| CTS $\mathrm{F}^{\prime}$ |  | Jack 21 Pin 46 | Jack 25 Pin 13 |
| CTS G ${ }^{\prime}$ |  | Jack 21 Pin 50 | Jack 25 Pin 37 |
| CTS H ${ }^{\prime}$ |  | Jack 21 Pin 32 | Jack 25 Pin 61 |
| CAN A' | First Terminal over eight, ie. \#9 | Jack 21 Pin 67 | Jack 24 Pin 12 |
| CAN B' |  | Jack 21 Pin 69 | Jack 24 Pin 7 |
| CAN C ${ }^{\text {' }}$ |  | Jack 21 Pin 71 | Jack 24 Pin 27 |
| CAN ${ }^{\prime}$ |  | Jack 21 Pin 73 | Jack 24 Pin 55 |
| CAN E' |  | Jack 21 Pin 77 | Jack 25 Pin 12 |

Table 5-1. Internal Signal Wiring Cont'd.

| Nmemonic | WIRED |  |  |
| :---: | :---: | :---: | :---: |
|  | Definition | From | To |
| CAN F' |  | Jack 21 Pin 63 | Jack 25 Pin 7 |
| CAN G' |  | Jack 21 Pin 65 | Jack 25 Pin 27 |
| CAN H ${ }^{\prime}$ |  | Jack 21 Pin 61 | Jack 25 Pin 55 |
| DATA A' | Data Detected | Jack 21 Pin 45 | Jack 24 Pin 34 |
| DATA B' |  | Jack 21 Pin 43 | Jack 24 Pin 50 |
| DATA C' |  | Jack 21 Pin 57 | Jack 24 Pin 68 |
| DATA D' |  | Jack 21 Pin 55 | Jack 24 Pin 78 |
| DATA E' |  | Jack 21 Pin 53 | Jack 25 Pin 34 |
| DATA $\mathrm{F}^{\prime}$ |  | Jack 21 Pin 51 | Jack 25 Pin 50 |
| DATA G ${ }^{\prime}$ |  | Jack 21 Pin 49 | Jack 25 Pin 68 |
| DATA H' |  | Jack 21 Pin 47 | Jack 25 Pin 78 |
| 1 RTS | One Request to | Jack 22 Pin 26 | Jack 22 Pin 20 |
|  | Send | Jack 22 Pin 20 | Jack 22 Pin 31 |
|  |  | Jack 22 Pin 31 | Jack 22 Pin 29 |
| GROUND |  | Jack 18 Pin 85 | Jack 19 Pin 85 |
|  |  | Jack 19 Pin 85 | Jack 20 Pin 85 |
|  |  | Jack 20 Pin 85 | Jack 21 Pin 85 |
|  |  | Jack 21 Pin 85 | Jack 22 Pin 85 |
|  |  | Jack 22 Pin 85 | Jack 23 Pin 85 |
|  |  | Jack 23 Pin 85 | Jack 24 Pin 85 |
|  |  | Jack 24 Pin 85 | Jack 25 Pin 85 |
|  |  | Jack 18 Pin 86 | Jack 19 Pin 86 |
|  |  | Jack 19 Pin 86 | Jack 20 Pin 86 |
|  |  | Jack 20 Pin 86 | Jack 21 Pin 86 |
|  |  | Jack 21 Pin 86 | Jack 22 Pin 86 |
|  |  | Jack 22 Pin 86 | Jack 23 Pin 86 |
|  |  | Jack 23 Pin 86 | Jack 24 Pin 86 |
|  |  | Jack 24 Pin 86 | Jack 25 Pin 86 |
|  |  | Jack 22 Pin 83 | Jack 23 Pin 83 |
|  |  | Jack 23 Pin 83 | Jack 24 Pin 83 |
|  |  | Jack 24 Pin 83 | Jack 25 Pin 83 |
|  |  | Jack 22 Pin 84 | Jack 23 Pin 84 |
|  |  | Jack 23 Pin 84 | Jack 24 Pin 84 |
|  |  | Jack 24 Pin 84 | Jack 25 Pin 84 |
|  |  | Jack 25 Pin 83 | Jack 25 Pin 85 |
|  |  | Jack 25 Pin 84 | Jack 25 Pin 86 |
| $+5 \mathrm{~V}$ |  | Jack 18 Pin 1 | Jack 19 Pin 1 |
|  |  | Jack 19 Pin 1 | Jack 20 Pin 1 |
|  |  | Jack 20 Pin 1 | Jack 21 Pin 1 |
|  |  | Jack 21 Pin 1 | Jack 22 Pin 1 |
|  |  | Jack 22 Pin 1 | Jack 23 Pin 1 |

Table 5-1. Internal Signal Wiring Cont'd.

| Nmemonic | WIRED |  |  |
| :---: | :---: | :---: | :---: |
|  | Definition | From | To |
| $+5 \mathrm{~V}$ |  | Jack 23 Pin 1 | Jack 24 Pin 1 |
|  |  | Jack 24 Pin 1 | Jack 25 Pin 1 |
|  |  | Jack 18 Pin 2 | Jack 19 Pin 2 |
|  |  | Jack 19 Pin 2 | Jack 20 Pin 2 |
|  |  | Jack 20 Pin 2 | Jack 21 Pin 2 |
|  |  | Jack 21 Pin 2 | Jack 22 Pin 2 |
|  |  | Jack 22 Pin 2 | Jack 23 Pin 2 |
|  |  | Jack 23 Pin 2 | Jack 24 Pin 2 |
|  |  | Jack 24 Pin 2 | Jack 25 Pin 2 |
|  |  | Jack 25 Pin 2 | Jack 25 Pin 1 |
| -12V |  | Jack 18 Pin 81 | Jack 22 Pin 81 |
|  |  | Jack 22 Pin 81 | Jack 23 Pin 81 |
|  |  | Jack 23 Pin 81 | Jack 24 Pin 81 |
|  |  | Jack 24 Pin 81 | Jack 25 Pin 81 |
|  |  | Jack 18 Pin 82 | Jack 22 Pin 82 |
|  |  | Jack 22 Pin 82 | Jack 23 Pin 82 |
|  |  | Jack 23 Pin 82 | Jack 24 Pin 82 |
|  |  | Jack 24 Pin 82 | Jack 25 Pin 82 |
|  |  | Jack 25 Pin 82 | Jack 25 Pin 81 |
| $+12 \mathrm{~V}$ |  | Jack 18 Pin 75 | Jack 22 Pin 75 |
|  |  | Jack 22 Pin 75 | Jack 23 Pin 75 |
|  |  | Jack 23 Pin 75 | Jack 24 Pin 75 |
|  |  | Jack 24 Pin 75 | Jack 25 Pin 75 |
|  |  | Jack 18 Pin 76 | Jack 22 Pin 76 |
|  |  | Jack 22 Pin 76 | Jack 23 Pin 76 |
|  |  | Jack 23 Pin 76 | Jack 24 Pin 76 |
|  |  | Jack 24 Pin 76 | Jack 25 Pin 76 |
|  |  | Jack 25 Pin 76 | Jack 25 Pin 75 |

Table 5-2. Power Distribution Wiring

| Voltage | From | To |
| :---: | :---: | :---: |
| +5 | Power Supply Pin 10 | +5 Volt Fuse (2) |
|  | +5 Volt fuse | Jack 18 Pin 1 |
|  | +5 Volt fuse | Jack 18 Pin 2 |
| $-12$ | Power Supply Pin 4 | - 12 Volt Fuse (4) |
|  | -12V fuse | Jack 18 Pin 81 |
|  |  | Jack 18 Pin 82 |
| +12 | Power Supply Pin 13 | +12 Volt Fuse (3) |
|  | +12 Volt fuse | Jack 18 Pin 75 |
|  | +12 Volt fuse | Jack 18 Pin 76 |
| +5 Volt lamp* | +5 Volt fuse | lamp |
|  | lamp | ground (PS pin 9) |
| AC (Hot) | Power Supply Pin 1 | AC fuse (1) |
|  | AC fuse (1) | Interlock Switch |
|  | Interlock Switch | ON/OFF Switch |
|  | ON/OFF Switch | AC receptacle |
| DC ground | Power Supply pin 7 | Ground (Chassis) |
| AC ground | Power Supply pin 3 | Ground (Chassis) |
|  | Receptacle Ground | Chassis Ground |
| AC (Common) | Receptacle Common | ON/OFF Switch |
|  | ON/OFF Switch | Interlock Switch |
|  | Interlock Switch | Power Supply Pin 2 |

Figures 5-2 and 5-3 relate the input power wiring for the two specific ac power environments. Table 5-3 provides input/output cabling data for the communications cables.

### 5.2 TROUBLESHOOTING

The SPD-M Multiplexer can be quickly repaired by circuit board replacement. The only immediate visual failure indication is the Power ON lamp. This indicator signals a power disruption which completely disables the Multiplexer so that communications cannot be transacted with


Figure 5-2. Power Wiring 230 Volt Operation


Figure 5-3 Power Wiring 115 Volt Operation No Input Transformer

Table 5-3. I/O Cable 15 Wire Conductor, 25 Pin Connector

| Belden 8458 |  |  | E/A RS 232B Standard Interfacing |  |
| :---: | :---: | :---: | :---: | :---: |
| Color | $\begin{gathered} \text { Cinch } \\ \text { DB } 25 \mathrm{P} \end{gathered}$ | $\begin{gathered} \text { Cinch } \\ \text { DB } 25 \mathrm{P} \end{gathered}$ | Circuit | Description |
| Black | 1 | 1 | AA | Protective Ground |
| White | 2 | 2 | BA | Transmitted Data |
| Red | 3 | 3 | BB | Received Data |
| Green | 4 | 4 | CA | Request to Send |
| Orange | . 5 | 5 | CB | Clear to Send |
| Blue | 6 | 6 | CC | Data Set Ready |
| White/Black | 7 | 7 | $A B$ | Signal Ground |
| Red/Black | 8 | 8 | CF | Data Carrier Detector |
| Green/Black | 13 | 13 |  |  |
| Orange/Black | 14 | 14 |  |  |
| Blue/Black | 15 | 15 | DB | Transmitter Signal Element |
|  | 17 | 17 |  | Timing |
| Black/White | 17 | 17 | DD | Receiver Signal Element |
|  | -- | - |  | Timing |
| Red/White | 19 | 19 |  |  |
| Green/White | 20 | 20 | CD | Data Terminal Ready |
| Blue/White | 21 | 21 |  |  |

associated Terminals. The loss of dc operating voltages will also cause catastrophic failure. This fault can be isolated by observing the condition of the dc current fuses.

Because of the expansion capability and the modularity of circuit boards, some fault conditions will be selective. Observing the following relationships, note that a faulty Output Line Driver/Receiver causes one of a specific group of four Terminals to fail while a faulty Summation board causes one of a group of eight Terminals to fail. Assuming a total of 16 Terminals are connected, and they all fail, with the exception of power failure, the Data Flow board would be suspect.

| 4 | $5-8$ | $9-12$ | $13-16$ |
| :---: | :---: | :---: | :---: |
| Terminals | Terminals | Terminals | Terminals |


| Input Line Driver/Receiver | 1 | 1 | 1 | 1 |
| :--- | :--- | :--- | :--- | :--- |
| Data Flow | 1 | 1 | 1 | 1 |
| Summation | 1 | 1 | 2 | 2 |
| Output Line Driver/Receiver | 1 | 2 | 3 | 4 |

A problem existing in the Output Line Driver/Receiver will most likely effect only one Terminal. Verification that a given probelm exists at the Multiplexer, rather than at the Terminal, can be performed by cable switching at the Multiplexer connector panel.

Prior to performing any tests such as the off line installation test (Paragraph 2.2), the Terminal circuit board configuration should be reviewed. Headers should be checked and the software program verified, ie., Multiplexer testing is dynamic and the test vehicles are properly operating Display Terminals.

### 5.3 OPTION BLOCKS

As illustrated in Figure 3-3, the Multiplexer has three single position option blocks on the Data Flow circuit board (STB 10, 12 and 21) and one dual position block on the Summation board (STB 10/11). The locations are determined by counting the IC locations from the bottom row of logic, left to right, with the package side facing front. The following is a list of possible option blocks.

## MULTIPLEXER



Part NO.

001-11-01-723
STB NO.

10

12

$$
001-11-01-724
$$



001-1:1-01-725


001-11-01-742
21
Async Data Sync Data Sets 2400 Baud 8 Port MUX


Async Data - Async Data Sets. 1200 Baud 8 Port MUX.


21
Async Data - Async Data Sets. 1200 Baud 16 Port MUX.


10
Async Data
Async Modem


12
Async Data - Async Modem Non Priority Poll
Single Xmitt Poll


Part NO.

001-11-01-777


001-11-01-803


21
8 port - Synchronous Modem and Controller
STB NO.

21

12 Non Priority Polling - Single Transmit Poll

8 port - No New Sync Non Priority Multiple Transmissions

## Function

Async Data-Async Modem -



## MULTIPLEXER (Cont.)



Pert NO. STB NO.

001-11-02-709 10/11


001-11-02-766
10/11
Master Mux - Multiple Transmission
$\left[\begin{array}{llll}0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0\end{array}\right]$

## APPENDIX A

## MODEM ELIMINATOR

The Modem Eliminator is used to connect one Display to another through a synchronous or asynchronous communications controller and to allow operation of the transmit and receive functions without a data set. The Eliminator generates the data set signals required for a particular operation, whether half duplex or full duplex (see Figure A-1). In addition, the eliminator is also useful when used between a Multiplexer and Display. Figure A-2 is a Modem Eliminator block diagram. The 13.2 MHz clock provides an accuracy of $0.1 \%$ at 2400 Baud. At slower speeds, it is more accurate. The clock feeds into a synchronous binary counter, of which several phases are decoded. The first decode is B in any (1000) which is fed into the 7493 as the clock. Then two other decodes are taken. One is the count seven, which is used as a strobe and provides the actual clock for the 7476. On the right side of the schematic the data being clocked is a decode of all the 7493's and is applied to the $J$ and $K$ inputs. When setting up the data set speed, the counter counts up to a certain point which is equivalent to a predetermined number of milliseconds. The 7476 J and K inputs are tied so each time the count comes in, the output toggles. As stated before, a count of seven from the synchronous binary counter strobes the 7476. On a count of nine all the registers are reset. So the decoded count does three things. Every synchronous count of one sets the 7493 counter. On a count of seven the left side 7476 flip flop is strobed


Figure A-1. Modem Eliminator


Figure A-2. Modem Eliminator Block Diagram
and at a count of nine the registers are cleared and the up count repeats. There are two ways of starting the operation. Either the Request to Send from the A Display or the B Display will start the counter up. The two 1160 line receivers are also inverters. When RTS is not true, the counters and flip flops are held reset. When RTS A is high on pin 1, the output of the line receiver is negative. As soon as the RTS comes in true, the resets are lifted and counting begins. At least one of the RTS's has to be true to enable the count. The output signals being generated are a simulation of the data set signals and are a function of the incoming Request to Send and timing count. The outgoing signals are: transmit and receive clock and the Clear to Send. When RTS A starts, several things happen. First, a transmit clock is required for the particular display (A) and a receive clock is required for the other display (B). (Display A is transmitting and Display B is receiving.) Display A has generated RTS which resulted in enabling the serial transmit clock (STC) and the serial receive clock (SRC). A1so, the RTS has resulted in a carrier detect for B and CTS (Clear to Send) for A. The eliminator thus has effectively generated the substitutes replacing the data set.

# FIELD ENGINEERING 

TECHNICAL MANUAL

$$
\text { SPD }^{\text {TM }} 10 / 20
$$

PERIPHERALS

## VOLUME III SPD-P PRINTER

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## Appendix A

Interface With Incremental Printer

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## FOREWORD

This manual provides the installation, theory of operation and maintenance procedures for the SPD-P Printer. Field repair is accomplished by on-site replacement of a faulty module. Module repair is performed off-site by a technical staff with appropriate test equipment. An understanding of the theory provided in this manual and a familiarization with the logic diagrams provided in support document FS 003 will provide the required background for technical proficiency.


Figure 1-1 SPD-P Printer

## CHAPTER I

## INTRODUCTION

### 1.1 SCOPE

The purpose of this manual is to provide Field Engineers and other qualified personnel with information concerning the theory of operation and maintenance of the SPD-P Printer.

The remainder of this section contains a general discussion of the Printer. Chapter II contains installation information. Operational information is covered in Chapter III and the detailed theory of operation is discussed in Chapter IV. Maintenance and repair information is presented in Chapter V.

The SPD-P Printer consists of a Univac incremental printer mechanism and operating electronics installed in a cabinet along with interface logic and operator controls designed by INCOTERM. This manual covers the Printer in general and the interface logic and operator controls in detail.

### 1.2 GENERAL DESCRIPTION

The SPD-P is a hard copy output device that prints out messages sent to it by SPD 10/20 Display Terminals. It accepts six-part, edge-sprocketed forms 3-5/8 inches (minimum) to 14-7/8 inches (maximum) in width. The form length must be 11 inches to prevent printing on the perforated dividing line.

The physical characteristics of the SPD-P are listed below.

| Height: | 13 inches |
| :--- | :--- |
| Width: | 28 inches |
| Depth: | 23 inches |
| Weight: | 90 pounds |
| Operating Temperature: 5 to $40^{\circ} \mathrm{C}$ |  |

The SPD-P Printer is shown in Figure 1-1.

### 1.3 INTERFACE

The SPD-P Printer has self-contained input/output and control electronics which has a designed-in multiplexing capability. A maximum of 16 SPD 10/20 Terminals can be connected to one SPD-P Printer. However, each Terminal must contain an Asynchronous Controller specifically to interface with the Printer.

Data from the Terminal to the Printer conforms to the American Standard Code for Information Interchange (ASCII).

### 1.4 OPERATION

The Printer operates automatically under control of the SPD 10/20 Terminal's stored program. The SPD-P is controlled by the Asynchronous Controller. All Write, Command and Test Input/Output instructions issued to the Printer are the same as those issued to the Asynchronous Controller.

When several Terminals are connected to a Printer, the Multiplexer allows the Terminals to be serviced in a round-robin fashion. Once the Printer receives a request for service from a Terminal, it is reserved for the exclusive use of the requesting Terminal until it is released by that Terminal. When released, the Printer scans all other Terminals for service requests before it scans the releasing Terminal again.

Switches are provided to allow the operator to start and stop the Printer and to initiate single spacing and form feeding. Indicators are provided to alert the operator that the Printer is out of paper or that a fuse is blown.

## CHAPTER II

SPD-P INSTALLATION

## 2. 1 UNPACKING AND INSPECTION

The SPD-P is factory packed in two separate containers. One package contains the complete OEM printer mechanism and the other is composed of the INCOTERM housing with power supplies, interface electronics, internal wiring and the ac power cable. Visual inspections should be performed prior to opening the container, and again after opening the container, to determine what items are part of the particular installation. Some data which can be visually checked are, that the serial numbers of both printer mechanism and housing agree with the summary listing. If the application is in a 50 Hz environment, the printer motor will be stamped 50 Hz . In a 230 volt environment, a multi-tap input ac transformer is used to convert the input ac to the 115 Vac operating voltage.

### 2.2 ASSEMBLING THE PRINTER

Remove the shipping base and packing material from both the mechanism and housing. Due to the bulk and lack of handling surfaces on the printer mechanism, obtain assistance when lifting the mechanism into the housing. When lifting, handle by the cast portion of the base only and be careful not to grip the circuit board which is exposed across the entire bottom of the mechanism. Figure 2-1 is a rear view of the printer mechanism, illus-


Figure 2-1 UNIVAC Printer Mechanism
trating the motor, motor starting circuit and electronics connector. The printer rear panel is hinged on the bottom and by releasing the top holding screws, the panel and attached power supplies can be removed from interfering with the mechanism during installation. When ready for installation, a protective cover is positioned over the motor and associated circuits; this portion is placed to the rear of the housing. With the housing cover raised, as in Figure 3-1, observe the four shock absorbent mounting pads. Lift the mechanism into the housing and position the mechanism base studs into the shock mounts. With the printer rear screen removed (as illustrated in Figure 3-3), the interface cable can be inserted into the mechanism electronics socket.

### 2.3 CABLING

The ac input power cable supplied with the Printer is generally an eight foot cable with a twist lock socket for the Printer connection, and a plug specified by the customer on the line connection.

## CAUTION

Check the ac line prior to applying power. Readings should be:
$115 \mathrm{~V} \pm 2.5 \%$ or
$220 V+5 \%$
The communications cables supplied for a given installation are packed with the SPD 10/20 Terminal. Figure 2-2 illustrates the one-to-one correspondance for the purpose of cabling ordered Terminals. The jacks Jl through J16 are located on the rear of the Printer in four multiples of four jacks in a row. Since all installations will not have 16 Terminals, the Printer connector panel can be one of four configurations as follows:

> 1. Four Terminals: JI through J4
2. Eight Terminals: J1 through J8
3. Twelve Terminals: J1 through J12
4. Sixteen Terminals: J1 through J16

The illustration, Figure 3-3, is an eight Terminal Printer. Obviously, not more than eight Terminals could be connected to this Printer; however, it will function if less than the full complement of Terminals are connected.
SPD 10/20 Communications

Figure 2-2. Sixteen Terminal Installation Cabling

### 2.4 TESTING THE PRINTER

The assembled Printer can be exercised to provide a level of confidence before connecting to on-line Terminals. The following procedure provides that if the Printer mechanics and interface controller are operating properly, the mechanism will print out a series of E's.

| STEP | PROCEDURE |  | RESULT |
| :---: | :---: | :---: | :---: |
| 1 Load Form | a) b) c) | Position Printer form supply behind and slightly lower than the base of the Printer. <br> Enter the edge of first form into form feed slot as illustrated in Figure 3-3 and push the form forward. <br> Place the paper form on the drive sprockets in a manner that locates the perforated line between the color coded (black) teeth on the sprocket. The sprocket can be manually positioned by applying an outward force to the outer knob and rotating. | Continuous form will feed properly. <br> Form slides through and is positioned between sprocket tractors (Figure 3-1). Automatic form spacing occurs so printing on the perforation does not occur. |
| 2 Power ON | a) | Connect the ac power cable to the line source and position rear panel power ON/OFF switch to ON. | All power systems operate and mechanism motor runs. |
| 3 Test | a) | Locate Logic IC designated A16 (Card A package 16) and short pin 2 to ground. | Mechanism prints all $\mathrm{E}^{\prime}$ s. |

Upon successful completion of the test for E's, printing operator controls can be exercised for proper function. See controls and indicators, Table 3-1. The final installation test is on-line (TFU data input) printing. As a prerequisite to the actual data transfer and print out, the software program with Printer handler must be loaded and the key which will cause data transfer must be specified.

## CHAPTER III

## OPERATIONAL DESCRIPTION

### 3.1 PHYSICAL DESCRIPTION

### 3.1.1 SPD-P Printer Major Components

The SPD-P Printer consists of a Univac incremental printer mechanism, three dc power supplies and control electronics housed in an INCOTERM custom cabinet (see Figure 3-1).

The incremental printer mechanism is a Univac Type 0769-06 with associated control electronics. It requires $120 \mathrm{~V}, 60 \mathrm{~Hz}$, ac power and three levels of dc power: $+48 \mathrm{~V},+5 \mathrm{~V}$ and $\overline{+} 12 \mathrm{~V}$.

The dc power supplies are listed below.
Faratron Corp. Model FR-1031-C supplies +48V
ACDC Electronics Model IC5N2. 7 supplies +5 V
ACDC Electronics Model 0A15D1.1-3 supplies +12 V
The control electronics (printer controller) consists of two plug-in circuit boards (A and B) with wire-wrap sockets for dual in-line IC's. The boards have handles to assist in removal and installation (see Figure 3-1).

### 3.1.2 Cabinet (See Figures 3-1 through 3-3)

The cabinet houses and provides structural support for the printer mechanism, power supplies, printer controller and electrical components such as switches, connectors and fuses. It has six main parts: bottom, bottom cover, printer mechanism mounting frame, components mounting


B 2114-27

Figure 3-1 SPD-P With Cover Raised


Figure 3-2 SPD-P Printer, Cover Closed


Controller Inspection Port Holding Bracket Controller Controller
Card A

Form Feed Slot


Figure 3-3 Rear Of Printer With Protective Screen Removed
frame, top cover and rear screen.
The bottom is a rectangular shaped sheetmetal piece formed so that it has a front, two sides, no back and a partially open underside.

The protective bottom cover is a sheetmetal piece with an integral paper guide.

The mounting frame for the printer mechanism is a heavy gage metal frame using welded square-tubular construction. It is basically rectangular with the sides extending rearward approximately three inches and then vertically to form two posts, six inches high. Each corner of the horizontal rectangular section contains an integral web to which a shock mount is secured. The printer mechanism is mounted on these shock mounts.

The printer mechanism mounting frame rests on the inside of the bottom section of the cabinet. The bottom protective cover is installed on the outside of the bottom section using eight screws and spacers to provide a $1 / 4$ inch space between the cover and the bottom. Each screw passes through the cover, a spacer and the bottom and is screwed into a tapped hole in the printer mechanism mounting frame. In this manner, the bottom section, bottom cover and printer mechanism mounting frame are securely held together.

The components mounting frame is a sturdy rectangular metal frame using welded angle iron construction. It contains one horizontal and one vertical cross member to facilitate the mounting of components. This frame is attached to the rear of the integral posts on the printer mechanism mounting frame with four screws. The ac panel and I/O connector panel are mounted on the outside of the frame. Mounted on the inside of the frame are the card holder for the printer controller; mounting bracket for the +48 V power supply and $\overline{+12 V}$ power supply; and the mounting plate for the +5 V power supply.

The top cover assembly is a sheet-metal piece that forms the top half of the cabinet. The front section is slanted and contains a printer viewing port, approximately 17 inches wide by 6 inches high. A hinged plexiglass window is installed in this opening with space at the top for paper ejection. The cover is pivoted at the rear and opens upward. Travel is limited to a
little over $90^{\circ}$ by stops that contact the components mounting frame. When fully opened, the cover center of gravity holds it firmly against the stops without a locking device.

The rear protective screen is attached to the outsideof the components mounting frame (see Figure 3-4). It encloses the back of the Printer except for the ac panel and I/O connector panel.

### 3.1.3 Printer Controller

The printer controller circuitry is contained on two plug-in circuit boards (see Figure 3-5). The boards utilize wire-wrap sockets which accept dual in-line IC's with a maximum of 16 leads. The sockets also accept plugin discrete component units. The board connector consists of 70 gold plated finger contacts arranged 35 per side. The fingers connect with two rows of feed-through wire-wrap pins to effect the conversion of wire-wrap connections to plated finger connections.

The cards are inserted into wire-wrap edge type connectors. Plastic guide strips on the card holder and handles on the card provide accurate and convenient insertion and removal. Looking at the card holder from the front of the Printer, Card A is at the rear.

Card A contains 64 sockets arranged in eight rows of eight each. Three sockets contain discrete component units; the remainder (61) contain IC's.* Card B contains 56 sockets arranged in seven rows of eight each. Two sockets contain discrete component units and three are unused; the remainder (51) contain IC's. A small area at the top of Card B contains discrete components soldered to wire-wrap terminals. Each card contains a ground plane on the wire-wrap side and a +5 V plane on the component side.

The first and last socket location in each row is identified by a number etched on the board. These numbers, along with the card identification (A and B), are used on the symbols in the logic diagrams.

### 3.1.4 Electrical System

The Printer contains an electrical system which serves primarily as a power distribution system. It also interfaces the operator's control

3-6 * Depending on intended number of terminals


Figure 3-4 Rear Of Printer With Protective Screen Installed


Figure 3-5 Printer Controller Circuit Cards


Figure 3-5a Printer Controller Circuit Cards
switches and indicators with the printer control electronics.
The operator's switches (4) and indicators (2) are mounted in a cluster in the lower right corner of the top cover. The wiring from the switches and indicators can be disconnected at a plastic connector mounted inside the top cover.

The ac power panel is a removable subassembly that contains the 115 V ac input receptacle, ac power switch and five fuses (one for the ac power and one for each of the four dc supply voltages, $+5,+12,-12$ and +48 V ). The switch, receptacle and fuses are accessible from the rear of the Printer. A relay and terminal block are mounted on the inside of the panel. The terminal block distributes 115 V ac to the power supplies and to the relay contacts. When the relay is energized, the 115 V ac is sent to the printer motor contained on a large printed circuit board mounted on the printer mechanism (see Figure 3-6). The relay coil is energized by the output of the +5 V power supply. If the +5 V output is not present, 115 V ac power will not be sent to the printer motor.

An interlock switch is located electrically between the ac power switch and the ac terminal block. Physically, the switch is located under the rim of the cabinet bottom section near the left front corner (see Figure $3-1$ ). It is actuated when the top cover is closed. Opening the cover opens the switch and cuts off the 115 V ac power.

Edge type connectors are provided for printer controller cards A and $B$. They are mounted on the bottom of the card holder. An edge type connector is provided on a wiring harness to interface with the printer mechanism pc board.

An I/O connector panel subassembly is mounted on the frame at the rear of the Print er (see Figure 3-3). The panel contains 16 slots for installing I/O connectors. The number of connectors depends on the number of SPD 10/20 Terminals interfacing with the Printer; however, connectors are added in groups of four. Covers are installed over unused slots.

## Connector



Figure 3-6 Printer Mechanism Operating Electronics
*On UNIVAC parts list IC's of the same type have the same identification
ie, 2 IC 16 etc.

### 3.2 CONTROLS AND INDICATORS

With one exception, the operator's controls and indicators are located on the lower right section of the top cover (see Figure 3-2). The exception is the ac power switch which is located on the rear of the Printer. The name, type and function of each control and indicator is listed in Table 3-1.

Two fuses are associated with the FUSE indicator. They are the print actuator fuse and the line feed fuse which are installed in fuse holders located on the printer mechanism frame (see Figure 3-1). The FUSE indicator does not illuminate if any of the fuses on the rear of the Printer are blown.

### 3.3 FUNCTIONAL DESCRIPTION

The Printer operates automatically but it can be stopped by the operator to initiate single line spacing and form spacing. When using the maximum form width (14-7/8 inches), a maximum of 132 characters can be printed on a line. Lines are spaced vertically, six per inch.

The basic speed of the Printer is 330 Baud, asynchronous, which provides an operating speed of 30 characters per second $\frac{330 \mathrm{Baud}}{11 \mathrm{Bits}}=30$ characters per second. An 11-bit code is used to transmit data to the Printer: one start bit, eight data bits and two stop bits. Transmission is serial by bit, with the least significant bit first.

The Printer is controller by an Asynchronous Controller in the Terminal. All Write I/O, Control I/O and Test I/O commands issued to the Printer are the same as those issued to the Asynchronous Controller Data Set Ready lines to indicate a Ready status. If a TIO Data Set On-Line does not acknowledge, the Printer is off, out of paper or has malfunctioned.

The control characters for the Printer are tabulated below.

| Signal | Hex | Binary | Function |
| :--- | :--- | :--- | :--- |
| Carriage Return | OD | 00001101 | Returns carriage to left margin |
| Carriage Return/ | OE | 00001110 | Returns carriage to left margin <br> and spaces paper up one line |
| Line Feed | OA | 00001010 | Spaces paper up one line |
| Form Feed | OC | 00001100 | Spaces paper to the top of the next <br> form and returns carriage to the <br> left margin |

Table 3-1. Controls and Indicators

| Control/Indicator | Type | Function |
| :---: | :---: | :---: |
| POWER switch | Two position rocker action switch labeled ON and OFF | Applies ac power to the Printer |
| START switch | Illuminated (green) momentary action, pushbutton switch | When momentarily depressed, starts Printer. Illuminates when activated. |
| STOP switch | Illuminated (red) momentary action, pushbutton switch | When momentarily depressed, stops Printer. Illuminates when activated. |
| FORM SPACE switch | Momentary action, pushbutton switch. White face, nonilluminated | When momentarily depressed, spaces paper to top of next form. Printer must be stopped before activating this switch. |
| SINGLE SPACE switch | Momentary action, pushbutton switch. White face, nonilluminated | When momentarily depressed, spaces paper up one line. Printer must be stopped before activating this switch. |
| OUT OF PAPER indicator | Red indicator | Illuminates when Printer is out of paper. |
| FUSE indicator | Red indicator | Illuminates when fuse has blown in Printer. |

The Printer character set is described in Table 3-2. The Printer responds only to the printable character codes and the control codes.

Table 3-2. Printer Character Set

| Printed <br> Character | Keyboard Character | Internal <br> Code | Printed <br> Character | Keyboard Character | Internal <br> Code |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $!$ | X (ETX) | 0100001 | @ | @ | 1000000 |
| " | (CHECK) | 0100010 | A | A | 1000001 |
| \# | \# | 0100011 | B | B | 1000010 |
| \$ | \$ | 0100100 | C | C | 1000011 |
| \% | \% | 0100101 | D | D | 1000100 |
| \& | \& | 0100110 | E | E | 1000101 |
| 1 | ' | 0100111 | F | F | 1000110 |
| 1 | $($ | 0101000 | G | G | 1000111 |
| ) | ) | 0101001 | H | H | 1001000 |
| * | * | 0101010 | I | I | 1001001 |
| + | + | 0101011 | J | J | 1001010 |
| , | , | 0101100 | K | K | 1001011 |
| - | - | 0101101 | L | L | 1001100 |
| . | . | 0101110 | M | M | 1001101 |
| 1 | 1 | 0101111 | N | N | 1001110 |
| 0 | 0 | 0110000 | 0 | 0 | 1001111 |
| 1 | 1 | 0110001 | P | P | 1010000 |
| 2 | 2 | 0110010 | Q | Q | 1010001 |
| 3 | 3 | 0110011 | R | R | 1010010 |
| 4 | 4 | 0110100 | S | S | 1010011 |
| 5 | 5 | 0110101 | T | T | 1010100 |
| 6 | 6 | 0110110 | U | U | 1010101 |
| 7 | 7 | 0110111 | V | V | 1010110 |
| 8 | 8 | 0111000 | W | W | 1010111 |
| 9 | 9 | 0111001 | X | x | 1011000 |
| : | : | 0111010 | Y | Y | 1011001 |
| ; |  | 0111011 | Z | Z | 1011010 |
| $<$ | $<$ | 0111100 | [ | $\Delta$ | 1011011 |
| $=$ | $=$ | 0111101 | $\checkmark$ | 1 | 1011100 |
| $>$ | $>$ | 0111110 | $\sqsupset$ | D | 1011101 |
| ? | ? | 0111111 | 1 | 7 | 1011110 |
| SPACE | SPACE | 0100000 | - | - | 1011111 |

## CHAPTER IV

## THEORY OF OPERATION

### 4.1 INTRODUCTION

The theory of operation discussion deals primarily with the Printer Controller electronics designed and built by INCOTERM. The Printer Controller electronics consists of two cards of digital circuits that interface the printer operating electronics (supplied by Univac) with the Asynchronous Controller in the SPD 10/20 Display Terminal.

The printer operating electronics, which are supplied by Univac, basically convert low power digital signals that represent requests for specific printer operations to higher power electrical control signals. These signals operate a motor, relay and solenoids which control the mechanical portion of the Printer.

### 4.2 PRINTER CONTROLLER

The Printer Controller circuit boards are described physically in Paragraph 3.1.3. This discussion deals with the theory of operation and is referenced to schematic drawing 008-01-01, sheets 2 through 9. Figure 4-1 is a simplified block diagram of the Printer Controller.


Figure 4-1. Simplified Block Diagram, Printer Controller

### 4.2.1 Timing

The basic timing is generated by the oscillator shown in the upper left section of sheet 2. The oscillator is composed of a 13.2 MHz crystal, B8 gates PROSC1, $-2,-3$, capacitor C1 and resistors R1 and R2. The operating frequency is divided by 40,000 to produce 330 Baud which is the basic speed of the Printer. Using an ll-bit data word (one start bit, eight data bits, two stop bits) the Printer operating speed is 30 characters per second.

Four 4-bit binary counters (B4, B5, B6, B7) are cascaded to produce a system clock. Each unit is a TI type SN 7493 4-bit binary counter connected as a 4-bit ripple-through counter. Pin 14 is the input and the four outputs are taken at pins 8, 9, 11 and 12. The first two stages, B7 (PRCL1) and B6 (PRCL2), are free running. The last two stages, B5 (PRCL3) and B4 (PRCL4), contain active reset inputs (pins 2 and 3) that are connected to the input data via a logic network. In stages B4 and B5, pins 2 and 3 are connected to the output of OR gate B13 (PRCLG). A high signal at both pin 2 and pin 3 of B4 and 5 resets all the stage outputs to logical 0. A low signal to these inputs is required to count. Resets occur for each half character.

The Printer Data input signal PRDATA enters sheet 2 at the input of inverter A38 (PRDIN). Physically, the input data enters the Printer Controller at one of 16 line receivers on Card B. The line receiver translates the bipolar line levels $(+12 \mathrm{~V})$ to the conventional logic levels ( 0 V and +5 V ) used in the Printer Controller. The outputs of the 16 line receivers are multiplexed and a single output is fed to inverter A38 on sheet 2. The sixteen line receivers in the Printer are used to accomodate a maximum of 16 Display Terminals with one Printer. These circuits are discussed in detail in subsequent paragraphs.

The PRDATA signal is also sent directly to the J-input of JK flip flop A36 (PRSI00). The Q-output of A36 is connected to the input of the serial/ parallel register A34 and A35. The register consists of two TI type SN 7495 4-bit shift registers connected in series. Each unit has a serial input (pin 1), four outputs (pins 10-13), mode control input (pin 6) and two clock inputs (pin

8 for shift left and pin 9 for shift right). The mode control must be logical 0 to effect a right shift; and logical 1 to effect a left shift. The mode control signal is generated at the output (pin 2) of inverter B24 (Parallel Enable PRPENI). The shift left clock signal is generated at the output (pin 8) of gate B16 (Parallel clock PRPCL). This signal is also sent to the preset input of flip flop A36. The shift right clock signal is generated at the output (pin 3) of gate B16 (PRCD1). This signal is also used to clock flip flop A36.

Assume that a character is being sent to the Printer Controller. Its arrival is indicated by a start bit (logical 0) on the PRDATA line. This low signal is inverted by A38 (PRDIN) and applied to the K-input of flip flop A36. It is also applied directly (non-inverted) to the J-input of A36. The inputs to A 36 are now conditioned $\mathrm{J}=0$ and $\mathrm{K}=1$ and when clocked will shift the first zero bit into register A36. The first zero bit is also applied to pin 12, B22. Flip flop B2, being initially cleared, provides a $\bar{Q}$ high to pin 13 gate B22, resulting in a true ANDing situation. The output of B22 (pin 11) is inverted (low to high) and applied to the J input of flip flop B2, which is not clocked until the first zero bit has been evaluated as being valid.

Gates B13 (PRCLGB, PRCLGA) are conditioned to produce a signal at B13 pin 3 which lifts the reset from counters B4 and B5 and counting begins. If the detected zero bit does not stay low for a count equal to one half a bit time, the logical assumption is that noise was present and the loss of a high signal at B2l creates a counter reset through B13 (pin 3). If the zero bit is valid when the counter output B4 pin 9 goes high, the condition is logically ANDed at gate B16 pins 12 and 13 which produces a parallel enable at the input register mode pins. B4 pin 12 goes high, causing B16 pin 8 to go low, clocking all ones into the register. The one half bit time is decoded at gate B14 which produces a clock for flip flops B3. The flip flops are decoded at PRCDI (Bl6 pin 3) which clock the true zero bit condition into clock enable flip flop B2. The zero bit condition is latched and counting continues for the remainder of the bit time. The next time B14 is true, flip flops B3 change state as decoded at B15 pins 1 and 2.

The character bits are gated each time by gate B16 and are shifted into register A34/35 until the zero bit reaches position 08, at which time the register contains a full character.

The enabler PRSCl from inverter A38 pin 8 strobes the four MSB's into buffer register A27/A28 on sheet 4. The enabler PRSC2 (A38 pin 10) strobes the four LSB's. The low signal present at A42 pin 3 is fed to pin 9 OR gate B13, where it enables a clock reset. The logical conotation is that the character data has been serially received and parallel enabled to the buffer at which time resets occur in preparation for the next character. Resets also occur on Power UP. The Power UP is detected at input pin A33 when it is fed through inverter A41. The output of inverter A41 resets the move carriage circuits and is applied to another inverter. The output of A38 (pin 6) resets the buffer register and through OR gate B13 and inverter B24, resets the character enable flip flop B2 and the character clocks 5 and 6 (flip flop B3).

Sheet 3 is the character counter which operates in conjunction with the reluctance pick up head in the Printer. The reluctance pick up produces a signal related to the printer character wheel, and sends out a stream of 65 pulses, followed by a gap of about 3.5 milliseconds, which indicates a return to the first character (see Figure 4-2). The circuit takes the character pulse from the Printer and feeds it through inverter A38, pin 13, and A29, pins 1 and 2 , which establish a clean waveform before clocking the synchronous counter. The counter (A18, 1920 and 21) is decoded at AND gate A22 to provide a count of 34, and at gate A30 for a count of one. A count of 64 is decoded to inhibit print hammer firing.

The print wheel sprocket data stream is also used to time the print hammer pulse. The necessary signal is a low of $926 \mu \mathrm{~s}$ duration. Flip flops A17 count two sprocket pulses of $463 \mu \mathrm{~s}$ each, decoded at AND gate A33 and fed to the print actuator flip flop A09 on sheet 5.

After the last sprocket tooth and prior to the first tooth is a gap area which produces a 3.7 ms pulse. This lull allows recovery time for the actuator should the last and first characters of a print wheel cycle be printed


Figure 4-2. Reluctance Coil, Print Sprocket Wheel Relationship
in succession. The gap is also a convenient reference point for separating print wheel cycles as is necessary since carriage movement is performed on one cycle and compare/print on the next. Flip flop Al8 (PRCCR) separates the two cycles. The period of the gap is detected by the decay time of the $22 \mathrm{~K} \Omega / .1 \mu \mathrm{~F}$ RC network at the output of inverter A39 (pin 6). The resulting signal presets flip flop Al8 at pin. 7. When the gap passes the pickup head the level change conditions pin 1 of AND gate A33. Pin 2 is enabled by a basic timing derivative and feeds from pin 3 a clock signal which toggles the outputs of flip flop Al8.

The character bits in the storage buffer on sheet 4 are sensed, and if the character is printable, either bit 5 or bit 6 is high. This condition (valid character) is decoded at gate A24. Assuming a printable character, the first operation required is to start moving the printer carriage. This operation occurs at a sprocket wheel count of 34 , decoded at A10 along with a signal indicating the carriage is not on the right margin. The carriage continues to move until the character is printed; if another character is immediately present, gate A24 (valid character) stays conditioned until no more valid characters appear in the register.

### 4.2.2 Printable Character

When the character in the buffer register (sheet 4) is a printable character, and the carriage starts moving, a compare operation is performed to find out where the character is on the wheel and then the hammer is fired. The carriage starts moving on the count of 34 , but the compare must wait until the next revolution of the print wheel. With the valid character decode from A24, the move carriage flip flop A11 is set through gate A10. Flip flop A09 (PRTTC) provides the Time To Compare signal. When conditioned by PRVCH (valid character) the output is fed back through inverter A23 and enables the compare gate A31. The compare circuit uses an exclusive ORing of the character in the buffer and the count on the wheel. When they match, PRCG 0 through 5 (A24 and A32) all go high and that high is a true compare signal. After the compare, the valid character and the $\bar{Q}$ side of A 18 (PRCC 6, sheet 3) produce a signal at gate A33 pin 8, which allows Al7 (sheet 3) to start counting. Two successive sprocket wheel pulses are decoded at A17 (sheet 3) which provide the timed signal (PRPFP) of 926 microseconds used to fire the printer hammer, after which the input buffer is reset. Figure 4-2 summarizes the printable character timing. If only one character is to be printed or if it is the last character of a series, flip flop A03 and A15 set after compare and reset after the next count of one to stop carriage motion.

### 4.2.3 Control Characters

Control character commands are decoded from bits 3, 5, and 6 of the character register at gate Al5 (PRCCL). A 100 combination of bits 3, 5 and 6 respectively conform to the USASCII set which is used for control characters. With a control character available the specific decodes for carriage return (A13, pin 6), line feed (A14, pin 6), and form feed (A14, pin 8) are ANDed with the control character enabler from pin 6, A15. The gated control functions have to be true simultaneously with the count of 34. Both coded and mechanical carriage returns are also provided. When the carriage is at the right side, a switch is activated and forces an automatic carriage return. The coded Carriage Return is gated with the count of 34 and sets flip


Figure 4-3. Printable Character Timing
flops B9 and B10, pin 12 (sheet 4), which provides the carriage return. The Carriage Return flip flop stays set until the carriage returns to the left margin where another microswitch is mechanically activated and causes the controller to drop the carriage return signal to the Printer itself. There are a number of ways to accomplish Line Feed, such as control codes coming from the Terminal, manual single space from a pushbutton on the Printer panel, or when the paper is positioned three lines from the bottom of the form, in which case another microswitch makes automatic spaces to the third line down on the next form. This action prevents printing over the perforation. The Line Feed decode is ANDed with a character count of 34 for the width of the line feed signal. The flip flop B9 and B10 (pin 6) is conditioned for one character time at a count of 34 . When Form Feed is sent to the Printer, the Univac electronics sends back a signal at input pin B11 to inverter B21, High Signal Equals Home Paper. With the Form Feed flop set, the High Home Paper signal resets it, but the condition is latched in the logic on the Univac mother board. That condition remains until the skip perforation switch is activated. At that point it single spaces six lines to the top of the next form and is ready to go again.

### 4.2.4 Built In Test And Error Detect

The series of gates on the left side, sheet 6(A05, A06 and A07), are provided to print out special characters under Error or Test conditions. The data from the Asynchronous Controller is checked for parity at gate A02, a 74180 , 8 -bit parity checker. After the data is in the storage buffer, it is examined for even parity. Device A02 decodes the parity condition just before the time to compare. If bad parity is detected, either an asterisk or a question mark can be printed in place of the faulty character. Gates A05, A06 and A07 force the storage buffer to a code for a question mark or an asterisk. A test is performed by enabling AND gate A16 ${ }^{*}$ which results in an output of all E's, croping the page and clearing the buffer.

When the Asynchronous Controller sends out requests for service, such as Request to Send, Clear to Send, etc., the Printer must be energized
before printing.
There are two output paths for Clear to Send. One is for a valid character, the other is for a control character. When performing a print operation, if there is another character available, the data is shifted out of the input register and into the storage buffer, which allows the input buffer to receive the next character. The control character is different as far as the time frame involved. The carriage return must travel from the left margin, which requires 385 milliseconds. So the Clear to Send must be held longer. Upon detection of any control character, Clear to Send shuts off and remains off until the carriage is all the way back. Line Feed takes only one character time and occurs right after the character count of 34 and allows another character in. The Form Feed must wait until completion; the form feed time is approximately one half second.

The Printer can interface with up to 16 Terminals and the means for selecting which Terminal is going to be enabled is on sheets 7,8 and 9 . First, the counter on sheet 8 operates as a sequencer. When a Terminal sends out a Request to Send, it is received onsheet 7 (line receivers), and is sent to sheet 8 for summation and selection. When the Request to Send and the count match (B39, 40, 47 and 48), the sequencer stops and a Clear to Send is sent to the Terminal, which enables the data into the Printer Controller.

If the Printer runs out of paper or blows a fuse, a signal is sent to the Terminal to test for the presence of the Data Set Ready signal.

## CHAPTER V

MAINTENANCE AND REPAIR

### 5.1 GENERAL

The SPD-P operation is dependent upon the TPU, its electronic interface and the electro-mechanical printer mechanism. Some problems which appear as an inoperative or partially operative Printer can be traced back to the Terminal. The electronic printer controller at the Printer can be repaired by circuit board replacement. Faulty power supplies are also repaired by replacement. The only item housed in the Printer which is not repaired by replacement is the power cabling. Detailed parts breakdown of the Univac mechanism are contained in Univac manual MH 2307 and adjustments are contained in MH 2308. Some of the more useful data relative to Univac adjustments are contained in this chapter.

### 5.2 SIGNAL AND CABLE DATA

Table 5-1 summarizes the nmemonic signal as it is found in the Printer Controller logic diagrams. The points of wiring identified in the Table can be accessed with an oscilloscope probe, preferably with the circuit card (A or B) on an extender. The signal input cabling is illustrated in Figure 5-1. As illustrated, the I/O connector is for a four Terminal input, but similar cabling would be used for expanded input operation. The external cables are the standard 1:1 cable, however, the Printer cable is generally much longer than other communi-

Table 5-1. Printer Signal Summary

| Nmemonic | WIRED |  |
| :---: | :---: | :---: |
|  | Definition | From To |
| PRPENI | Printer Parallel Enable (Inverted) | Plug A pin 39 Plug B pin 39 |
| PRPCL | Printer Parallel Clock | Plug A pin 40 Plug B pin 40 |
| PR SEL 2 | Summation of Selected <br> Terminals (9 through 16) | Plug A pin 46 Plug B pin 46 |
| PRPURI | Power Up Reset (Inverted) | Plug A pin 42 Plug B pin 42 |
| PRSCL | Shift Clock | Plug A pin 43 Plug B pin 43 |
| PRCDI | Clock Decode First <br> Half Bit Time | Plug A pin 44 Plug B pin 44 |
| PRCD2 | Clock Decode Second Half Bit Time | Plug A pin 45 Plug B pin 45 |
| PRCL24 | Timing Clock Pulse | Plug A pin 47 Plug B pin 47 |
| PR DATA 1 | Summation Data From Terminals 1 through 8 | Plug A pin 48 Plug B pin 48 |
| PRCD1 | Terminal Mux Scan Clock Stage 1 | Plug A pin 49 Plug B pin 49 |
| PRDC2 | Terminal Mux Scan Clock Stage 2 | Plug A pin 50 Plug B pin 50 |
| PRDC3 | Terminal Mux Scan Clock Stage 3 | Plug A pin 51 Plug B pin 51 |
| PRDC4* | Terminal Mux Scan Clock Stage 4 (Q) | Plug A pin 52 Plug B pin 52 |
| PRFCRI |  | Plug A pin 53 Plug B pin 53 |
| PRCRD | Carriage Return Decode | Plug A pin 56 Plug B pin 56 |
| PRCRLFD | Carriage Return, Line Feed Decode | Plug A pin 57 Plug B pin 57 |
| PRLFD | Printer Line Feed | Plug A pin 58 Plug B pin 58 |
| PRFFD | Printer Form Feed | Plug A pin 59 Plug B pin 59 |
| PRI34 | Sprocket Wheel Count of 34 | Plug A pin 60 Plug B pin 60 |
| PRCCH | Printer Control <br> Character | Plug A pin 61 Plug B pin 61 |

Table 5-1. Printer Signal Summary Cont'd.

| Nmemonic |  | WIRED |
| :---: | :---: | :---: |
|  | Definition | From To |
| PRRRD | Printer Reset Ready | Plug A pin 62 Plug B pin 62 |
| PRGRD | Printer Ready Gate | Plug A pin 63 Plug B pin 63 |
| PRIRDX | Strobe Clear To Send Terminals 9 through 16 | Plug A pin 67 Plug B pin 54 |
| PRDIN | Serial Data Input To Serial/Parallel Register | Plug A pin 41 Plug B pin 41 |
| PRDATAl | Data Line For Terminal 1 | Plug B pin 4 Conn 1 pin 2 |
| PRRTS 1 | TPU Request to Send Terminal 1 Data | Plug B pin 5 Conn 1 pin 4 |
| PRCTS 1 | Printer to TPU Clear to Send | Plug B pin 6 Conn 1 pin 5 |
| PRDATA2 | Data Line Terminal 2 | Plug B pin 8 Conn 2 pin 2 |
| PRRTS2 | Request to Send Terminal 2 | Plug B pin 9 Conn 2 pin 4 |
| PRCTS2 | Clear to Send Terminal 2 | Plug B pin 10 Conn 2 pin 5 |
| PRCOl | Sprocket Wheel Count of 1 | Plug A pin 38 Plug B pin 38 |

The Printer power wiring can be either 220 V 50 Hz or 115 V 60 Hz , depending on customer selection. Figures 5-2 and 5-3 are simplified power wiring diagrams for both versions. Always verify that the power supplied (measure) corresponds with the SPD-P and Univac identification plates.


Connector

Figure 5-1. Input Output Wiring Schematic


Figure 5-2. Printer Power Wiring Simplified, 220 V 50 Hz Operation


Figure 5-3. Printer Power Wiring Simplified, 115 V 60 Hz Operation
cations cables. The standard length is 50 feet. See Table 5-2 for I/O cable data.

### 5.3 PRINTER ADJUSTMENTS

The only operating control provided with the Printer mechanism is a phasing control located on the left hand side of the mechanism. The phasing control tab is located on the front side of the sprocket wheel housing and is positioned so it can be rotated through a $180^{\circ}$ arc. The purpose of the control is to adjust the time of print hammer impact so that characters are not clipped at the top or bottom. Since impact time is a function of paper thickness, the adjustment is made when different paper stock is used.

The three main items which if properly set result in good print operation are:

1. Code wheel adjustment
2. Mounting screws on the actuator and incrementing rack must be tight
3. Timing adjustment as discussed above.

When Printer adjustments are made, the phase adjustment should be performed first, which establishes good character presentation as a reference for other adjustments.

### 5.3.1 Lubrication

The actuator carriage shaft and code wheel shaft should never be greased. Cleaning can be done with a non-linting cloth moistened with freon. The lead screw, lead screw pawl pivot point and teeth on the incrementing bar can be greased after being cleaned. Anderol grease L-757 or an equivalent is recommended.

### 5.3.2 Miscellaneous Adjustment Notes

The pully cord has a tendency to stretch over a period of time. When replacing the cord, a carriage return measurement should be conducted to assure proper operation of the Printer. The test requires an oscilloscope to observe the 385 ms carriage return time. The oscilloscope is connected with the trigger probe to $P 1$ pin 8 and the input probe to Terminal board 1

Table 5-2. I/O Cable 15 Wire Conductor, 25 Pin Connector

| Belden 8458 |  |  | E/A RS 232B Standard Interfacing |  |
| :---: | :---: | :---: | :---: | :---: |
| Color | $\begin{aligned} & \text { Cinch } \\ & \text { DB } 25 \mathrm{P} \end{aligned}$ | Cinch DB 25 P | Circuit | Description |
| Black | 1 | 1 | AA | Protective Ground |
| White | 2 | 2 | BA | Transmitted Data |
| Red | 3 | 3 | BB | Received Data |
| Green | 4 | 4 | CA | Request to Send |
| Orange | . 5 | 5 | CB | Clear to Send |
| Blue | 6 | 6 | CC | Data Set Ready |
| White/Black | 7 | 7 | AB | Signal Ground |
| Red/Black | 8 | 8 | CF | Dața Carrier Detector |
| Green/Black | 13 | 13 |  |  |
| Orange/Black | 14 | 14 |  |  |
| Blue/Black | 15 | 15 | DB | Transmitter Signal Element |
|  | -- | -- |  | Timing |
| Black/White | 17 | 17 | DD | Receiver Signal Element |
|  | -- |  |  | Timing |
| Red/White | 19 | 19 |  |  |
| Green/White | 20 | 20 | CD | Data Terminal Ready |
| Blue/White | 21 | 21 |  |  |
|  | -- | -- |  |  |

Terminal 1. The measured time can be varied by rotating the spring tension nut.

When performing realignment of the code wheel to print wheel relationship, place a mark on the print wheel to indicate where the first character is located (note that the diamonds are not characters). The adjustment called for in the Univac manual can be one tooth off either way and still function properly.

The signal detected at the reluctance pick up head should be 600 mv . The spacing required for this output is 0.017 inches.

Tearing of paper, no character printed or poor character printing can result from improper print hammer flight time. Approach hammer adjustments with caution as they are interrelated.

The print wheel rotation is in close proximity to the paper and can cause smudges and paper jamming if the guide is not properly set. Clearance between the guide and print hammer should be $0.022 \pm 0.002$ inches.

Motor belt tension can be made without the use of a spring scale. If the belt can be turned on edge on the pully, the belt must be readjusted. If the belt can be turned up only about $1 / 4$ of an inch, the adjustment is operational (the same quick test can be performed on the drive belt).

FIELD SERVICE CHECK LIST

Customer name $\qquad$ Location $\qquad$
Field Eng. $\qquad$
SPD-P Preventive Maintenance Every Two Months

Date $\qquad$

Initials ${ }^{\text {' }}$

1. Clean the print wheel
2. Clean the actuator carriage shaft .
3. Check the drive belt tension and wear
(if belt can twist l/2 turn - too loose, l/4 turn - OK $\qquad$
4. Check print wheel shaft for binding, clean if necessary $\qquad$
5. Check the nylon pulley cord for fraying and replace if necessary
6. Check all pulley for loose mounting nuts and screws $\qquad$
7. Check lead screw and pawl for foreign matter, clean if necessary
8. Check incrementing rack and pawl for foreign matter, clean and lubricate if necessary
9. Check for varying line spacing
10. Check all printable characters for completeness .
11. Check for proper number of characters per line .

Measure and record the voltages (DO NOT adjust)
Input AC $\qquad$ $+5$ $\qquad$ $+48$ $\qquad$ $+12$ $\qquad$ $-12$ $\qquad$

## APPENDIX A

INTERFACE WITH INCREMENTAL PRINTER

The criteria for OEM interface are quite useful as a starting point when learning how the SPD-P works. To this end, the appropriate section from Univac's OEM Manual \#GD 0004 is presented verbatum.

SECTION 5. INTERFACE REQUIREMENTS FOR INCREMENTAL PRINTER MECHANISM WITH INTIMATE ELECTRONICS (TYPES 0769-00, -01, -06, -07)
5.1
5.1.1

### 5.2 LOGIC LEVELS

5.2.1 Unless otherwise specified, the logic levels for interface signals of the Incremental Printer Mechanism Types 0769-00 and 0769-01 are as follows:

$$
\begin{array}{ll}
\text { a. Low level: } \quad 0<\mathrm{V}_{\mathrm{L}}<0.5 ; \mathrm{I}_{\mathrm{L}} \leq 12 \mathrm{MA} \\
\text { b. High level: } & +5<\mathrm{V}_{\mathrm{H}}<+7 ; \mathrm{I}_{\mathrm{H}} \approx 0 \mathrm{MA}
\end{array}
$$

5.2.2 Unless otherwise specified, the logic levels for interface signals of the Incremental Printer Mechanism Types 0769-06 and 0769-07 are as follows:

$$
\begin{array}{ll}
\text { a. Low level: } \quad 0<V_{L}<0.5 ; I_{L} \text { (input) } \leq 13 \mathrm{MA} ; \\
& I_{\mathrm{L}} \text { (output) } \leq 34 \mathrm{MA} \\
\text { b. High level: } & +2.5<\mathrm{V}_{\mathrm{H}}<+5.0 ; \mathrm{I}_{\mathrm{H}} \approx 0 \mathrm{MA}
\end{array}
$$

### 5.3 INPUT SIGNALS

5.3.1 MOVE-CARRIAGE SIGNAL. The signal necessary to "move the carriage" is a low-level signal that must remain low for the duration of the carriage travel time desired. The
leading edge of this signal should be synchronized with the signal generated by simultaneous detection of the following two conditions:
a. A printable character in the data register.
b. A sprocket count of 34 .

The termination of the signal should be controlled by the following two conditions:
a. $N_{0}$ character in the data register.
b. A sprocket count of 1 .
5.3.2 PRINT SIGNAL. The signal necessary to "print" a character is a low-level signal with a duration equal to the interval between three sprocket pulses (926 microseconds).
5.3.3 LINE-FEED SIGNAL. To feed paper one line, a low-level signal with a maximum duration of 20 milliseconds is needed. The minimum duration required is 25 microseconds for the +6 V logic (Types 0769-00, -01) and 100 nanoseconds for the +5 V logic (Types 0769-06, -07). The minimum time between two successive line feed signals is one character time ( 33.3 milliseconds). The time required to advance the paper one line and be in position to print on the next line is also one character time.
5.3.3.1 In order to protect the line feed clutch, a fuse is connected in series with the +48 V level to the line feed (paper feed) solenoid. The fuse, which is a slow-blow type fuse (0.2A; 250V) mounted next to the clutch, limits the time of continuous line feed voltage to a maximum of 19.6 seconds.
5.3.4 CARRIAGE-RETURN SIGNAL. A low-level signal (initiated at a sprocket count of 34) is needed to initiate a carriage return operation. This signal must be terminated when the carriage assembly returns to the left margin. To allow time for the carriage to settle down, a minimum of 33.3 milliseconds is required between the closure of the leftmargin switch and the initiation of a move-carriage signal. The first character may be printed during the move-carriage signal.
5.3.5 INHIBIT-SOLENOIDS SIGNAL. In order to inhibit spurious line feed and print operations when DC power is turned on or off, the L-inhibit-solenoids signal is applied to the solenoid drive transistors. When turning on DC power, the L-inhibit-solenoid signal (a DC ground level at a maximum current of 350 milliamperes) is applied until the DC operating voltages reach $90 \%$ of rated value. This signal is also applied when turning off DC power and may be removed when the DC operating voltages have dropped to $10 \%$ of rated value.
5.3.6 HOME-PAPER SIGNAL. The home paper function is initiated either by a logic function or manually by means of a switch on the operator's panel. (The control unit circuitry and switch necessary to implement the home paper function must be supplied by the OEM customer.) When the L-home-paper signal is generated, the paper advances continuously at a rate of 12 inches ( 72 lines) per second for the duration of the signal and the H-set-home-paper signal goes high.
5.3.6.1 The H-set-home-paper signal goes low and the paper advance stops at the fourth line from the bottom of the form when the home-paper signal is removed. The paper is then advanced to the top of the next form (page) under control of the skipperforation function. Note that the duration of continuous paper travel (line feed or home paper) cannot exceed a maximum of 19.6 seconds (see paragraph 5.3.3.1).
5.4 OUTPUT-SIGNALS
5.4.1 PRINT-SPROCKET SIGNAL. The Incremental Printer Mechanism generates and presents to the interface amplified printsprocket signals (low pulses). The leading edge of each of these pulses should be used to step an external sprocket counter (character counter) supplied by the OEM customer. The output signals from this counter, when compared with the print data, should generate a print signal timed so that the correct character is printed. The output of this counter should also be used to time the move-carriage and carriagereturn signals.
5.4.1.1 There are 65 sprocket pulses generated during each revolution of the printwheel ( 33.3 milliseconds per revolution). The pulse width is approximately 220 microseconds, and the other time parameters of the print-sprocket signal are illustrated below.


The 3.70 millisecond time period between the last pulse of one group and the first pulse of the following group provides the print actuator recovery time required when the last and first characters on the printwheel are printed in succession.
5.4.1.2 The sprocket pulses may be synchronized with the characters on the printwheel by use of the mechanical phasing adjustment. It is necessary to correct this adjustment only when the form thickness is changed.
5.4.2 LEFT-MARGIN SIGNAL. The NO. contacts of the left-margin switch close and the signal is generated when the carriage returns to the extreme left position. In order to provide time for the carriage to stabilize, a minimum of one printwheel revolution ( 33.3 milliseconds) is required between the closing of the leftmargin switch and the initiation of an L-move-carriage signal.

The NO. contacts of the switch will open during the printing of the first column; therefore, a carriage return can be initiated after one character is printed (or spaced).
5.4.3 RIGHT-LIMIT SIGNAL. The right-limit switch closes and the signal is generated when the carriage moves to column $\mathrm{N}+1$ (where N is the maximum number of printable columns on the selected paper stock). The L-right-limit signal should be used to initiate an automatic L-carriage-return signal, which must be initiated at a sprocket count of 34 , as illustrated:


Note that, normally the carriage return function should be controlled by using an external sprocket counter (character counter) to determine the carriage position; the right-limit switch merely provides a safeguard for this function. A linefeed signal can be generated concurrently with the carriagereturn signal, in which case the line-feed function is completed before the carriage return operation.
5.4.4 OUT-OF-PAPER SIGNAL. The out-of-paper signal is derived from a switch used to sense the presence of paper. The NC contacts of the switch open (and the NO. contacts close) when the bottom edge of the last sheet of paper is approximately 2 inches from the line of print. This action causes the H-out-of-paper signal to be generated. It should be noted that the NO. contacts of this switch are available to energize an out-of-forms indicator (L-out-of-paper signal).
5.4.5 SKIP-PERFORATION SIGNAL. The skip-perforation (skip-line) signal normally is used when printing on ll-inch perforated forms. When the perforation line in the forms is approximately $1 / 2$-inch below the print line, the NO. contacts of the skip-perforation switch close and the signal is generated. The NO. contacts open when the perforation line advances approximately $1 / 2$-inch above the print line.
5.4.5.1 If continuous line-feed signals (L-line-feed) are generated during the time the NO. contacts of this switch are closed, the skip-perforation function can be performed. When this switch is adjusted properly (to provide $1 / 2$-inch margins at the top and bottom of an ll-inch form), there is space on the form for 60 lines of print.
5.4.6 FUSE-FAULT SIGNAL. The fuse-fault signal is normally low. When this signal goes high, it indicates that either the print actuator fuse or the line feed fuse is blown. Also, a set of relay contacts is provided to energize an indicator (L-print-check indicator) when a fuse fault occurs. It should be noted that if paper feeds continuously for more than 19.6 seconds, the line feed fuse will blow.

INTIMATE PRINTED CIRCUIT ELECTRONICS

L MOVE CARRIAGE
L CARRIAGE RETURN
L PRINT
L LINE FEED
L INHIBIT SOLENOIDS
L HONE PAPER


FIGURE 5-1. INTERFACE, SIMPLIFIED DIAGRAM

TABLE 5-1. Interface Signal List - Connector IJI

| Pin | Signal | Pin | Signal |
| :---: | :---: | :---: | :---: |
| 1 | L Left Margin | 19 | $+48 \mathrm{~V}$ |
| 2 | L Carriage Return | 20 | Not Used |
| 3 | L Move Carriage | 21 | DC Ground |
| 4 | L Print Sprocket | 22 | DC Ground |
| 5 | H Out of Paper | 23 | +48 V Return |
| 6 | L Inhibit Solenoid | 24 | +48 V Return |
| 7 | -12 V | 25 | Protective Ground |
| 8 | L Right Limit | 26 | Not Used |
| 9 | L Line Feed | 27 | AC Neutral (ACN) |
| 10 | L Home Paper | 28 | Not Used |
| 11 | H Set Home Paper | 29 | AC Hot; thru Cover Interlock (Not Supplied) |
| 12 | L Skip Lines | 30 | Not Used |
| 13 | L Print | 31 | H Fuse Fault |
| 14 | +6 V or +5 V | 32 | Not Used |
| 15 | Not Used | 33 | Forms Out Indicator <br> (Not Supplied) |
| 16 | Not Used | 34 | Home Paper Switch <br> (Not Supplied) |
| 17 | +48 V Actuator | 35 | $\begin{aligned} & \text { Print Check Indicator } \\ & \text { (Not Supplied) } \end{aligned}$ |
| 18 | +48 V Actuator |  |  |

TABLE 5-2. Component Assembly to Mechanism
Terminal Board Interface Connections

| Terminal | Mechanism Connection |
| :---: | :---: |
| TB1-1 | Left Margin Switch IS2-NO. |
| TB1-2 | Left Margin Switch IS2-C |
| TB1-3 | Reluctance Head 1PU1 |
| TB1-4 | Reluctance Head 1PUI |
| TB2-1 | Paper Feed Fuse F2 |
| TB2-2 | Paper Feed Solenoid 1L3 |
| TB2-3 | Paper Feed Solenoid IL3 |
| TB3-1 | Motor 18l (yellow) |
| TB3-2 | Motor Start Relay 1Kl-4 |
| TB3-3 | Frame Ground |
| TB4-1 | Out of Paper Switch 1S3-C |
| TB4-2 | Skip Line Switch 1S4-NC |
| TB4-3 | Skip Line Switch 1S4-NO. |
| TB4-4 | Skip Line Switch 1S4-C |
| TB4-5 | Out of Paper Switch 1S3-NC |
| TB4-6 | Out of Paper Switch 1S3-NO. |
| TB5-1 | Right Margin Switch 1Sl-NO. |
| TB5-2 | Right Margin Switch 1Sl-C |
| TB5-3 | Carriage Increment Solenoid IL2 |
| TB5-4 | Carriage Increment Solenoid IL2, and Carriage Pawl Solenoid ILI |
| TB5-5 | Carriage Pawl Solenoid 1 LI |
| TB5-6 | Print Actuator Solenoid 1L4 |
| TB5-7 | Print Actuator Solenoid 1L4 |

## FIELD ENGINEERING

TECHNICAL MANUAL

$$
S P D^{T M} 10 / 20
$$

PERIPHERALS

VOLUME IV SPD-T MAGNETIC TAPE UNIT
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## FOREWORD

This manual provides the installation, theory of operation and maintenance procedures for the SPD-T Magnetic Tape Unit. Field repair is accomplished by on-site replacement of a faulty module. Module repair is performed off-site by a technical staff with appropriate test equipment. An understanding of the theory provided in this manual and a familiarization with the logic diagrams provided in support document FS 003 will provide the required background for technical proficiency.


Figure 1-1. SPD-T Magnetic Tape Unit

## CHAPTER I

## INTRODUCTION

### 1.1 SCOPE

The purpose of this manual is to provide Field Engineers and other qualified personnel with information concerning installation, operation and maintenance of the SPD-T Magnetic Tape Unit, illustrated in Figure 1-1.

The SPD-T consists of a TT100 OEM tape transport manufactured by Sykes Datatronics Inc. The tape transport is purchased with read/write and motor control electronics to which the INCOTERM electronic controller is added. This manual deals with the INCOTERM and Sykes electronics in detail and the Tape Transport mechanical function in general.

### 1.2 GENERAL DESCRIPTION

The SPD-T Magnetic Tape Unit provides an auxiliary storage capacity for local use with an SPD 10/20 Display Terminal. Digital data is stored on computer grade magnetic tape that is contained in reel-to-reel cassettes which are conveniently loaded into the SPD-T.

The unit provides Read and Write operation in the sequential and direct access modes. Rapid data retrieval is possible in the direct access mode through the use of pre-recorded tape addresses. The SPD-T contains control electronics which allow interaction with the Display Terminal as defined by the system software program.

The SPD-T Magnetic Tape Unit is a self-contained unit which does not require a special controller in the Terminal. It is connected by cable to the connector on the left side of the Display Terminal, which is, in effect, an extension of the TPU I/O bus.

Physical characteristics of the SPD-T are listed below.

| Height: | 7 Inches |
| :--- | :--- |
| Width: | $8-5 / 16$ Inches |
| Depth: | $19-1 / 4$ Inches |
| Weight: | 43 Pounds |
| Mounting: | Desk Top |

## 1. 3 INTERFACE

The SPD-T has a self-contained controller which is operated on an I/O basis with both the TPU externally and the Tape Transport internally. The Terminal-to-Magnetic Tape Unit connection is made at connector J11 on the rear of the SPD-T (see Figure 1-2). Connector J12 is utilized only if an additional SPD-T or SPD-L is used. The interface cable is generally the same 50 -conductor cable used for paper tape program loading and is attached to the TPU at the 50 -pin program loading connector.


Figure 1-2. SPD-T, Rear View

### 1.4 OPERATION

The SPD-T can be operated in an automatic mode under control of the SPD 10/20 stored program or in a manual mode under operator control. The manual mode provides limited functions such as positioning the MANUAL/ AUTO switch, positioning the BOOT/REWIND switch or depressing the START switch. The common operator mode application is for BOOT loading of programs from tape to TPU. When under program control, data can be input from or output to the Magnetic Tape Unit sequentially or by direct access. The position of data on the tape can be calculated with respect to a prerecorded tape address.

### 1.5 GENERAL SPECIFICATIONS

Recording Density
Recording Technique
Read/Write Tape Speed

Data Transfer Rate

Characters Per Cassette
Between Message Gap
Start Time (5ips)
Stop Time (5 ips)
Jitter
Search or Rewind Speed
High Speed Stop Time
Stop Distance @ 100 ips
Voltage Input

Frequency AC

800 Bits Per Inch
Phase Encoding (Single Track)
5 Inches Per Second $60 \mathrm{~Hz}= \pm 5 \%$ @ $\pm 3 \mathrm{~Hz}$ $50 \mathrm{~Hz}= \pm 6 \%$ @ $\pm 3 \mathrm{~Hz}$
400 Characters/Second
10 Bits Per Character
( 8 Data, Double With Parity)
288, 000 - Gaps
80 Characters
200 msec Max. (0.8 inch)
100 msec Max. (0.2 inch)
$\pm 1.4 \%$ RMS/Bit
100 ips Average
260 msec Max.
16 Inches
Multi-Tap
105, 110, 115, 120, 125 V Nominal $+10-15 \%$
210, 220, 230, 240, 250 V Nominal +10-15\%
$60 \mathrm{~Hz} \pm 3 \mathrm{~Hz}$
$50 \mathrm{~Hz} \pm 2 \mathrm{~Hz}$

### 1.5.1 Tape Cassette Specification

General Description - The tape cassette is a reel-to-reel type with external dimensions which conform to the Phillips standard. The magnetic tape contained is high output computer grade, certified, and is preceeded and followed by 20 inches of transparent tape for BOT and EOT sensing. Cassettes have two track protect openings with removable closure tabs (replaceable by plugs) and a pressure pad to uniformly hold the magnetic tape against the Read/Write head.

Physical Properties - Tape
BASE

Material
Thickness
Width
Length

## OXIDE

| Thickness | 0.0002 Inch Nominal |
| :---: | :---: |
| Coercivity (hci) | $330 \begin{aligned} & +10 \\ & -35\end{aligned}$ oerstad |
| Retentivity ( Br ) | $1100 \pm 100$ gauss |
| Squareness (Br/Bs) | 0.80 |
| COATING ROUGHNESS | 1 to 6 microinches |
| PRINT-THROUGH | $2 \%$ max |
| EASE OF ERASURE | $3 \%$ max |
| SURFACE RESISTANCE | 1000 megohms max |
| LOGITUDINAL CURVATURE | less than $1 / 8$ inch in 36 inches |
| LEADER/TRAILER |  |
| Material | Polyester |
| Thickness | 0.0015 inch nominal |
| Width | $0.150_{-.002}^{+0} \text { inch }$ |
| Length | 20 inches minimum |
| Color | Clear |

Tensilized Polyester
0.0005 Inch Nominal
$0.150{ }_{-0}^{+0}$ Inch
$300_{-0}^{+3}$ Feet
0.0002 Inch Nominal
$330 \begin{aligned} & +10 \\ & -35\end{aligned}$ oerstad
$1100 \pm 100$ gauss
0.80

1 to 6 microinches
$2 \%$ max
$3 \% \max$
1000 megohms max
less than $1 / 8$ inch in 36 inches

Polyester
0.0015 inch nominal
$0.150_{-.002}^{+0}$ inch
20 inches minimum
Clear

## Pressure Pad

Pressure
When the Read/Write head is activated to the cassette, the pressure of the pad upon it shall be 0.005 to $0.015 \mathrm{~N} / \mathrm{mm}^{2}$. The pressure pad is symetrically positioned.

Dimensions
0.20 to 0.24 inch
0.20 inch minimum

In the direction of tape travel In the direction of tape width

## Certification

Tape must be certified end to end in cassette after loading for zero (0) drop-outs at 1600 fci measured at $50 \%$ detection level over two tracks.

## Operational

Read/Write Speed 15 IPS
(Heads in Contact)
Search \& Rewind Speed
110 IPS Average
(Heads not in contact)
Friction torque of the $2 \times 10^{-3} \mathrm{Nm}$ Max. full Hub in the Cassette
Friction torque of both
$2.7 \times 10^{-3} \mathrm{Nm}$ Max. hubs measured in the cassette itself at the nearly full Hub

Friction torque of both
$5.5 \times 10^{-3} \mathrm{Nm}$ Max.
Hubs measured in the Cassette itself at the nearly full Hub with a Hold-back torque of $0.8 \times 10^{-3} \mathrm{Nm}$

The tape shall be suitable for use with instruments applying a maximum continuous load of 2 N .

## Environmental Conditions

Operating

Temperature
Relative Humidity

## Storage

Temperature
Relative Humidity

Shipping
Temperature

## Suppliers

Information Terminals Corp. 1160 Terra Bella Aven. Mountain View, California 94040

Sykes Datatronics, Inc. 375 Orchard Street
Rochester, New York 14606
$40^{\circ} \mathrm{F}$ to $100^{\circ} \mathrm{F}$
$20 \%$ to $90 \%$ without condensation

400 F to 1200 F
$20 \%$ to $90 \%$ without condensation
$-4^{\circ} \mathrm{F}$ to $150^{\circ} \mathrm{F}$

P/N T-300 certified data cassette Sykes configuration

P/N 1001A0171A

## CHAPTER II

INSTALLATION

## 2. 1 SHIPPING AND INSTALLATION ENVIRONMENT

The SPD-T will function satisfactorily in temperature and humidity conditions suitable for operation in a computer system. The unit will withstand shipping temperatures varying between $-4^{\circ}$ and $150^{\circ} \mathrm{F}$. Normal operating range is $40^{\circ}$ to $100^{\circ} \mathrm{F}\left(40\right.$ to $38^{\circ} \mathrm{C}$ ) at 20 to $90 \%$ relative humidity without condensation.

Compared with open-reel tapes, magnetic tape cassettes provide superior protection against physical tape damage and collection of dust.

## 2. 2 UNPACKING AND INSPECTION

The SPD-T is shipped in a single container. When received, the outer extremities should be observed for obvious shipping damage. Upon opening the shipping container, an inner, edge protected carton is exposed. The inner carton contains the SPD-T and, depending on whether it is a single item shipment or part of a larger system shipment, the cables and Product Summary will also be included. However, in the case of a larger shipment, the cables and Product Summary may not be in the same container as the SPD-T. After removing the shipping base, place the SPD-T in its operating location and verify all markings against the Product Summary. Pay particular attention to the input voltage straping table, line cord recepticle markings and fuse rating.

## 2. 3 PREPARATION FOR OPERATIONAL CHECK OUT

Prepare an SPD 10/20 Display Terminal for operation with the SPD-T Magnetic Tape Unit by performing the Terminal installation and checkout, if the Terminal is a new installation or if verifying operational readyness of an existing Terminal. Locate the $50-$ pin program loading cable and a.c. power cable.

## CAUTION

Check the a.c. line voltage prior to connecting power cable. The reading must agree with the intended input voltage strapping table located on the underside of the unit.

### 2.4 OPERATING PROCEDURE FOR SPD-T CHECK OUT

1. Place the Magnetic Tape Unit physically close to the Display Terminal.
2. Place the Terminal and Magnetic Tape Unit to an OFF condition prior to connecting the signal cable.
3. Insert the female $50-$ pin plug into $J 17$ (top) on the rear panel of the SPD-T. Insert male end at the program loading connector on the Terminal.
4. Turn ON the Magnetic Tape Unit a.c. power switch on the rear of the unit and observe that the POWER ON and OPERATOR indicators (see Figure 2-1) are illuminated. The POWER ON indicator remains illuminated as long as power is applied.
5. Open the cassette receiver (see Figure 2-2) and insert the Magnetic Tape Cassette, with desired BOOT data, positioned so the front label can be seen through the receiver viewing port.
6. Close the cassette receiver firmly.
7. Turn the Terminal a.c. power ON and observe that the SPD-T OPERATOR indicator is extinguished.
8. Position the MANUAL/AUTO switch to MANUAL.
9. Position the BOOT/REWIND switch to BOOT.


Figure 2-1. SPD-T Operator Controls And Indicators
10. Momentarily depress START button. Observe that the TAPE MOTION indicator is illuminated. If tape motion starts on clear leader (BOT), it is automatically advanced to the oxide portion of tape. When the tape stops the TAPE MOTION indicator is extinguished. Depression of the START button again results in the TAPE MOTION and BOOT indicators illuminating. When the 'BOOT' program is loaded, the tape stops and the BOOT and TAPE MOTION indicators are extinguished. If an error is detected during program loading, the tape motion stops but the BOOT indicator remains lighted. Restart by depressing the START button.
11. When program loading is complete, position the MANUAL/AUTO switch to AUTO. Only the POWER ON lamp remains illuminated and the SPD-T operation is defined by the program software.

## NOTE

In the AUTO mode, the BOOT/REWIND and START switches have no effect on the operation of the Tape Unit.
12. To rewind the tape, place the MANUAL/AUTO switch to the MANUAL position and BOOT/REWIND switch to REWIND. Momentarily depress the START button and observe that the TAPE MOTION indicator is illuminated. When rewind reaches clear leader, motion stops and the TAPE MOTION indicator is extinguished.
13. When powering OFF or removing the signal cable, turn the Terminal OFF first, then turn OFF the SPD-T.

### 2.5 INSTALLATION TEST SOFTWARE

One tape cassette is included in all SPD-T customer shipments. Unless special consideration has been negotiated, the tape may be blank (void of data). Field personnel do not totally depend on the customer's tape to verify an installation; however, if the Field Engineer's tape proves the cassette unit is functioning properly, but the customer's tape does not work, a gain adjustment may be required (see Paragraph 5.5). Each Field Engineer carries at least


Figure 2-2. SPD-T With Cassette In Receiver
three tape cassettes:

1) a system diagnostic test cassette with both tracks protected to prevent erronious erase,
2) a blank tape (scratch pad) without protection, and
3) a tape cassette exerciser with both tracks protected.

### 2.5.1 Hardware Elements

The diagnostic test program requires:

1. An operational SPD $10 / 20$ with 2 K memory,
2. An SPD 10/20 Keyboard Model Kl1-01, and
3. Keyboard controller addressed 2 and SPD-T addressed 1.

Although the diagnostic was designed to a specific configuration, as listed above, the Field Engineer need only cross correlate the code produced by a specific key depression with the code position of another keyboard type to obtain the same results. The remainder of this chapter will reference the key conforming to the Model Mil-0l Keyboard.

### 2.5.2 Functional Description

Operation of the diagnostic test program is divided into four phases. The first two phases require manual manipulations necessary for Tape Transport operation, such as Power Up, loading the cassette, and setting switches. During the third phase (Boot Mode) the program is loaded into the TPU. The program starts automatically by displaying the information in Figure 2-3. (the grid is representative of each position on the CRT where a character can be placed). During phase four, the operator may select from the Test Menu any test from 2 through 8 listed in Figure 2-3. After choosing a test by typing the appropriate key number, that test is entered and information as in Figure 2-4 is displayed. If an error is detected, the appropriate error code is inserted, along with track and address information, during error processing (see Figure 2-5). If the test completes successfully, Figure 2-6 is displayed.

Phase 1 is the Power Up and Operator Intervention Required Test. This test is a written series of operator instructions on the physical use of the Magnetic Tape Unit. The control switches and indicator lamp functions




are described. The operator is instructed to position specific switches and verify appropriate indications. Instructions are then given for proper placement of the cassette into the unit.

Phase 2 is the Manual Motion Test. This test is similar to Test 1. The operator is instructed to perform manual actions and to monitor the appropriate indicators. The test performs the Manual mode rewind and forward-to-oxide functions.

Phase 3 is Verify BOOT. This test requires operator manual action to verify the BOOT function. The verification is by visual inspection of the display monitor to assure that operating programs have been loaded. The monitor should appear as in Figure 2-3.

Phase 4 consists of seven tests. The tests and Debug Program result from successful BOOT operation in Phase 3 and are under program control. They are randomly selectable by depressing the keyboard key (l through 8) appearing at the left of the displayed Test Menu (see Figure 2-3).

### 2.5.3 Operating Instructions

The following instructions are described for the operator. The first three phases should be completed in sequence to produce the proper operating environment for the fourth. Cassette No. 2 (blank with both tracks unprotected) should be loaded after the completion of Phase 3.

Operating Sequence:
Phase l-Power Up and Operator Intervention Required

1. Turn power on by depressing the white, two-position rocker switch on the rear of the SPD-T.
2. Observe the indicator lamps on the front of the SPD-T. The POWER ON and OPER lamps should be illuminated.
3. Power on the SPD $10 / 20$ Display.
4. Place the "Tape Cassette Diagnostic Test" cassette into the SPD-T by opening the receiver and inserting the cassette. Loading is accomplished by holding the cassette in the upper left corner with the recording tape up and the side marked 'OTHER SIDE OUTWARD' away from the operator.
5. Close the door. The OPER indicator lamp should go off.


Figure 2-7. Example of One Tape Address Segment

Phase 2 - Manual Motion Test

1. Position the AUTO/MANUAL switch to the MANUAL position.
2. Position the REWIND/BOOT switch to the REWIND position.
3. Depress the START button. If the magnetic tape was at the clear leader portion, nothing should happen. If the tape was over the oxide portion, the TAPE MOTION lamp will illuminate and the tape will rewind to clear leader. At clear leader, the tape will stop and the TAPE MOTION lamp will extinguish. Inspection can be made by opening the door of the SPD-T and observing the tape.
4. Place the REWIND/BOOT switch to the BOOT position. Depress the START switch. The TAPE MOTION lamp will go on and the tape will be moved to oxide. When motion stops, the TAPE MOTION lamp will extinguish. Inspect as in above paragraph.

Phase 3 - Verify BOOT Test

1. After Phase 1 and 2 have been completed, depress the START switch. The TAPE MOTION and BOOT indicator lamps should both illuminate as the tape moves forward.
2. Successful completion of this test will cause the **TAPE CASSETTE DIAGNOSTIC TEST** and other information to be displayed on the monitor screen as depicted in Figure 2-3.
3. If tape motion stops and the BOOT lamp remains illuminated, a bad BOOT record has been read. To recover, depress the START switch again and continue until successful completion.
4. Upon successful completion, remove the system test cassette and insert a blank cassette.

Phase 4 - Selectable Tests
Any of the eight tests in the listed Test Menu may now be selected. If the DEBUG program* is selected, the NEW LINE key performs the CARRIAGE RETURN function of earlier versions. Exit from DEBUG by typing J: 0800 (NEWLINE). To select a test from the displayed Test Menu, depress the corresponding number of the keyboard.

## NOTE

Tests 2 and 3 are complementary and it is wise to follow 2 with 3 . Tests 4 and 5 are also complementary and, as such, 4 should precede 5 .

* The DEBUG program is generally used by the programmer when testing new programs for further details (see the Programmer's Reference Manual).

Test 2
This test formats the address track as in Figure 2-7. Addresses are written from 0 to $383910^{\circ}$ Approximate length of the test is 12 minutes.

Test 3
This test reads the primary address and its complement to verify the accuracy of Test 2. All $3840{ }_{10}$ primary addresses are read if the test completes successfully. Approximate length is 12 minutes. If an error occurs, a display similar to Figure 2-5 will appear. The address of the error will appear in the message.

Test 4
This test writes a l000-character data block. The data, in hex, is AA, an alternating bit pattern (10101010). Approximate length is five seconds.

Test 5
This test searches for the data block created by Test 4. All 1000characters are read and inspected. Approximate length is five seconds.

Test 6
This test writes six records in BOOT format. The first record is intentionally bad. The tape is rewound and BOOT is entered under program control. The display monitor should go blank and the BOOT lamp should remain on. To recover, set the AUTO/MANUAL switch to MANUAL and the REWIND/BOOT switch to BOOT. Depress the START button. The display monitor should be restored to its previous condition i.e. **TAPE CASSETTE DIAGNOSTIC TEST**, etc. It is allowable to depress the START switch four more times for test purposes. Upon completion, reset the AUTO/MANUAL switch to AUTO.

Test 7
This test performs high speed motion testing. Data check characters are written at specific addresses and then a high speed search is made. The tape is rewound, followed by a forward and backward search. Verification of the check characters is performed. The test is approximately 30 sec onds in length.

Test 8
This test verifies the erase capability by erasing a 256-character block and then writing a check record. The tape is rewound and then read. Dropout and Parity status bits are allowed and tested for. Upon reading the check record, the test is completed. Length is approximately 15 seconds.

### 2.5.4 Test Interpretation

Upon successful completion of Tests 2, 3, 4, 5, 7, and 8, the message 'TEST OX ENDED' is displayed along with recovery instructions, as depicted in Figure 2-6. Errors encountered are displayed in the ${ }^{\prime} E R R O R=000 '$ message. The error codes and their meanings, as well as the test number or subroutine from which they come, are listed below.

| Code | Meaning <br> 001 | Bad erase, tape stop <br> 002 |
| :--- | :--- | :--- |
| Protected track, bad address, tape <br> stop | Test No. |  |
| 003 | Protected track, tape stop | 8 |
| 004 | Tape stop | 2,3 |
| 005 | Tape stop | 4 |
| 006 | Bad data, tape stop | Subroutine |
| 007 | Read/Write error | Subroutine |
| 008 | Boot error, tape stop | 5 |
| 009 | Tape stop, operator intervention | Subroutine |
| 010 | Address overrun | 6 |
| 011 | Bad data, tape stop | Subroutine |

Visual inspection of the status word at the bottom of the display should provide additional information. A one (l) above the description indicates the presence of that condition.

### 2.6 TAPE CASSETTE EXERCISE PROGRAM

The cassette exercise program produces the desired code pattern to allow critical calibrations adjustment. The adjustments and operation required are discussed in Paragraph 5.4 and 5.5.

## CHAPTER III

## OPERATIONAL DESCRIPTION

### 3.1 PHYSICAL DESCRIPTION

### 3.1.1 SPD-T Major Components

The SPD-T Magnetic Tape Unit consists of a Sykes tape deck with appropriate Read/Write and motor control electronics, a Crane multiple voltage power supply and an INCOTERM electronic controller (see Figure 3-1). The above components are housed in a cabinet suitable for desk top or shelf mounting.

The SPD-T will operate over a variable range of input ac voltages, as specified in Paragraph 1.5. Figure 3-1 illustrates the line input transformer which is tap adjustable to accomodate the input voltage while maintaining the proper secondary voltage for power supply and tape deck requirements. The power supply input is 120 Volts ac nominal at 50/60 Hz. The dc outputs are:

$$
\begin{aligned}
& +5 \mathrm{Vdc} \\
& \pm 12 \mathrm{~V} \mathrm{dc} \\
& +24 \mathrm{~V} \mathrm{dc}
\end{aligned}
$$

The tape deck capstan drive can be operated with 50 OR 60 Hz . The frequency of operation governs the synchronous capstan motor which must maintain capstan speed at 763 rpm . The proper capstan drive pulley is installed at the factory to provide a tape speed of five ips (capstan speed $=763$ ) in the Read and Write modes.
$2-\varepsilon$ INIERLOCK SPD-TCONTROLLER CARD CAGE

### 3.1.2 Tape Deck

Figure 3-2 illustrates the tape deck as it looks from the rear. The three motors are arranged across the bottom of the unit with the capstan drive motor on the right. The capstan motor is synchronous in operation and provides uni-directional rotation of the capstan and fly wheel. The method of mounting to the deck plate allows belt tension adjustments as required (see Maintenance Section).

The reel drive system utilizes two identical induction motors; one drives the cassette take up reel and the other the drive reel. The motors provide high speed tape movement at an average speed of 110 ips at 60 Hz , which is reduced to 90 ips at 50 Hz . During tape operation, proper application of voltage to the motor windings creates the proper tape tension and dynamic braking.


Figure 3-2. Rear View Of Tape Deck

### 3.1.3 SPD-T Controller

The electronic controller is physically located within the SPD-T Magnetic Tape Unit. The circuit is composed of five circuit cards, 6-1/4 by 6-1/2 inches. The card cage (see Figure 3-3) is a six position cage designed for horizontal card mounting and has large openings between runners for air flow. As illustrated, the cards are designated A through E and are inserted with A being the lowest position in the cage. Figure 3-4 illustrates each card. Note that the cards are keyed into the respective connector and the alpha designator is etched on the component side of each board.

### 3.2 INTERFACE WIRING

Figure 3-5 illustrates the connector side of the controller card cage. Input/Output signals in the TPU interface are taken from the wire wrap terminals and connected to I/O connectors J1l and J12. The tape deck commands and responses are routed through the connectors at the lower pins on the card cage. As the cable harness passes the power supply leads, they are picked up for routing to Jl through Pl . The remaining signals are distributed to the Read/Write electronics at J2 (P2) and motor control electronics at J4, 5 and 6 (P4, 5 and 6).

### 3.3 CONTROLS AND INDICATORS

With one exception, the controls and indicators for the SPD-T Magnetic Tape Unit are located on the front panel. The exception is the Power On switch which is located on the rear panel. The front panel controls and indicators are described below.

MANUAL/AUTO Switch

BOOT/REWIND Switch

START Switch

A two position toggle switch that selects whether or not tape is to be under program control (AUTO).

A two position toggle switch that selects the Bootstrap function or the Rewind function.

A pushbutton switch that initializes the Bootstrap function or the Rewind function in the Manual mode.


Figure 3-3 Side View SPD-T With Controller Boards Installed.
B2126-6


B2126-22

CONNECTOR

$$
\begin{aligned}
& \text { Filustrating Care 3-5. SPD-T Side View } \\
& \text { Cage Connector And I/O Wiring }
\end{aligned}
$$

### 3.4 FUNCTIONAL DESCRIPTION

The SPD-T Magnetic Tape Unit provides the terminal user with a local peripheral device with removeable cassette storage for both programming and data Input/Output. The controller associated with the tape unit can perform initial Bootstrap program loads to the Terminal by simple operator initiation. After the initial BOOT load, the TPU program controls SPD-T operation and can issue programmed commands to re-enter BOOT or Read/Write functions on either of the two tracks.

### 3.4.1 Magnetic Tape and Cassette

The operating magnetic tape supplied with the SPD-T is a certified computer grade tape contained in a cassette which conforms to Phillips standards. After data has been written on the tape, the user can elect to protect that information from being accidentally changed. This is accomplished on either track by removing a tract protect tab on the cassette. If it is desired to remove the protection, a means of filling the void where the tab was removed can be devised (tape, plug, etc.) which allows re-use of the cassette for Read/Write operations.

### 3.4.2 Controller Status Indicator

The SPD-T Controller has an 8-bit Input/Output Data Register, the contents of which are fed to an 8-bit Input bus buffer which can be strobed for data or status bits. When operating under program control, status bit zero is set by the following conditions which require operator intervention.

## Condition

a. Cassette not in place.
b. Malfunction of tape address change optical sensor unit.
c. Malfunction of the clear leader optical sensor unit.
d. Improper connection between TPU and SPD-T.
e. Tape stalls after motion was started.

## Action

a. Open door and position cassette.
b. Replace faulty lamp or light detector.
c. Replace faulty lamp or light detector.
d. Check connections.
e. Open door to clear the condition. If caused by faulty tape address change detector, repair as required.

Status bit one is set to indicate a program error caused by an illegal command sequence, data overrun or forward motion beyond the end of tape. Bit two is set in the Read mode if a parity error is detected and bit three is set if a dropout occurs. Bit four is a motion indicator and is set whenever the tape is in motion. Bit five sets to indicate a Manual mode operation. Bit six is wired to be continuously set and bit seven is not used.

### 3.4.3 Priority Conditions

Depending on how the SPD-T is being operated and the status of the unit, certain commands will not be executed by the controller. Hardware protection is provided to detect any illegal sequence of commands or failure within the unit that could possibly damage the transport mechanism. This protection will stop or prevent motion until the problem is rectified. The following conditions will cause commands to be rejected.
a. Once tape motion has been started, any command that would change speed or direction is ignored. Tape motion is not stopped.
b. Slow speed motion commands are ignored if clear leader is under the optical sensor.
c. Tape motion will be stopped and all motion commands (manual or automatic) ignored if operator intervention is required.
d. All TPU commands are ignored if the controller is in the Bootstrap Mode.
e. When the cassette controller is powered up and clear leader is under the optical sensor, the Fast Forward command is the only command that will be executed. Also, if the cassette is in place when power is turned on, an "artificial" stall will be generated to force the operator to open the door and insure that the cassette is mounted properly, i.e. at the beginning of tape.
f. If the controller is in the manual mode, all CIO commands will be ignored. However, all TIO and RIO Status Commands will function normally. If the RIO Data, WIO Data or Erase commands are issued, the controller causes the Auto-EXEC to transfer program control to background processing.
g. Write Track A/B Command will be rejected if Track A/B is protected. If these commands are issued while the tape is in motion, the tape is stopped and Status Bit 1, program error
is set. Further tape motion is inhibited until the flag is cleared by issuing an RIO Status Command.
The Enable-TAC-Interrupts command allows the controller to interrupt the TPU each time a TAC is detected. This command is valid for both slow and fast speed operation. TAC inter rupts may occur only when the tape motion is up to speed and clear leader is not detected. The Disable-TACInterrupts Command prevents the controller from interrupting the TPU when a TAC is detected. This command may be issued while either slow or fast speed operation is taking place or when motion is stopped.

The Read-Track-A and Read-Track-B commands cause the tape to begin slow speed motion in the forward direction, initialize sync search, and prepare the contraller to read data from the appropriate track. When sync is established, the first character sent to the TPU is the character immediately after the sync code. The Write-Track-A and Write-Track-B commands cause the tape to start slow speed forward motion and prepare the controller to write data on Track A or Track B respectively. No Read-Track or Write-Track commands should be issued over clear leader, and if issued, are rejected.

The Fast-Forward command causes the tape to begin high speed motion in the forward direction. If this command is issued over clear leader, the tape will move until oxide is detected and stop. If the command is given when clear leader is at the end of tape, an automatic rewind to oxide will occur. The Rewind command causes the tape to move at high speed in the reverse direction.

The Enter-Boot command moves the tape in the forward direction at slow speed, places the TPU into Bootstrap mode and causes the controller to search Track B for a boot record. If a BOOT record is not found, an automatic rewind will be performed and the tape will stop over clear leader at the beginning of the tape. In this case, operator intervention will be required.

The Unmask-Interrupt command allows the cassette controller to interrupt the TPU. The Mask-Interrupt command inhibits the controller from interrupting the TPU.

The controller generates an Inter rupt in four ways, listed below.

1. A character is read from the tape after a Read Track A/B command has been issued, the tape is moving at the correct speed, and sync has been established and an RIO has been issued.
2. The controller is ready to accept a write character after a Write Track A/B Command has been issued.
3. Tape motion stops for any reason after it had started, in which case an acknowledge signal will be given once by the controller to a RIO Data WIO Data or WIO Erase Command. An exception occurs if the cassette unit is switched to Manual Mode while the tape is in motion.

The Stop Command causes tape motion to stop. This command may be issued during either slow or fast speed operation. When this command is used while in the Write mode, a one inch inter-record gap will be created. This command must be issued before any command which would require the tape to change speed or direction. To switch from a Write to a Read operation, a CIO Stop is issued and a period of waiting is incurred before the motion signal becomes false, after which the CIO Read is sent.

The two WIO commands accepted by the controller are Data and Erase. The Data command causes data to be transferred from the ACR to the controller for storage on the tape.

If the controller cannot accept the data, normal Auto-Exec action occurs. The controller then generates an interrupt when it is ready to accept data. When a Write operation is terminated via a Stop command, the last character received by the controller is written on the tape before the controller actually executes the STOP. The Data and Erase commands should not be issued alternately.

Two RIO commands are accepted by the controller: Data and Status. The Data Command causes the controller to send an acknowledge signal to the TPU when it has data to transfer to the ACR. If no acknowledge signal is received, normal Auto-Exec action occurs.

The Status command causes the controller to transfer the byte of status information to the ACR. The controller always responds with an acknowledge signal to this command. The Status Command also clears the
parity, dropout, and program error bits in the status register.
The TIO commands accepted by the SPD-T controller are tests for Controller-Present, Beginning of Tape, Data Transferred, or TAC, ClearLeader, Read-Error, Tape-Stop-Condition, and Read-Error (or) Tape-Stop. The Controller Present command causes the controller to respond with an acknowledge if clear leader is under the optical sensor.

The Data-Transferred or TAC command provides the program with the capability of determining which type of interrupt came from the controller: If the controller responds with an acknowledge signal to this test, the last interrupt was due to TAC detection. If there is no acknowledgement, the last interrupt was due to a valid data transfer or a tape stopped condition. If TAC interrupts are enabled and a cassette interrupt has occurred, this command must be issued to clear the controller for further interrupts. (This command should not be given if TAC interrupts are not enabled.) TAC' inter rupts are mutually exclusive to Data Transfer and Tape Stop Interrupts.

The Read Error command tests status bits 2 (parity error) and 3 (drop out) to determine if the last character read from tape was in error. If no error is detected, the controller will respond with an acknowledge signal. The Tape Stop command tests status bit 0 , operator intervention required; bit l, program error; bit 4, tape in motion; and bit 5, manual mode. The controller will acknowledge if none of these status bits are set. The Read-Error or Tape Stop Condition command tests the status bits zero through five. If any bit is on the controller will not acknowledge.

### 3.4.5 Photo Detectors

The SPD-T tape deck uses photo sensitive transistors for two different applications. Figure 3-6 illustrates the basic principle used to signal tape address changes using a five-vane chopper wheel. The signal changes generated by the interrupted light beam provide the programmer with a reference point which can be used to access random areas of tape. When the TAC interrupt occurs, the address is stored into the TPU. After some subsequent time, that address can be recalled by computing the direction
of drive necessary to arrive at the specified address, i. e. forward or reverse. The tape is driven in a fast mode until the relative proximity of the address is arrived at as counted up to or down to by the program and corresponding TAC interrupts. The second use for a photo sensitive device is to detect whether the tape is on clear leader. Figure 3-7 illustrates the principle by showing graphically that the light beam from the source does not penetrate the oxide coated portion of the tape. As illustrated, there are two sections of tape which do allow light to fall on the photo sensor. The beginning of tape and end of tape are therefore both signalled by a single detector.

### 3.4.6 Tape Format

Figure 3-8' represents a typical section of two track magnetic tape. For practical purposes only a small number of addresses are illustrated. The layout above the fifth address illustrates the address format and that below the data track illustrates the data format. Notice that there are two portions of tape which fall in the magnetic oxide area that are unusable. The reason is that the process in which the clear leader is bonded to the oxide section degrades the oxide and is not reliable.

The topmost drawing illustrates one complete address occuring between two successive TAC interrupts. As soon as the TAC is detected, the program writes two leader characters followed by a sync character. Then two characters which define the address ( $16 \mathrm{bits} / 2 \mathrm{~K}$ memory) are written immediately, followed by the address complement. Two spare characters are then written, followed by a completely redundant address pattern. After the last character in the second pattern fill characters are written until the next TAC is encountered.

The two lower blocks illustrate the data pattern (the lowest is for BOOT data). Both the data record and BOOT record begin with 35 leader characters followed by a sync character. The data records illustrated exaggerate the fact that data is somewhat offset from the TAC. In reality, the 35 leader characters accomplish the offset which allows the tape to search for a TAC, read the address on Track A, then switch tracks for a Read or Write operation on Track B. Also note that due to the mechanical generation


Figure 3-6. Chopper Vane Tape Address Change Detector


Figure 3-7. Beginning And End of Tape Sensor


Figure 3-8. Address and Data Track Format
of TAC signals and in the peripheral change as tape is taken from one spool and placed on another the distance between TAC's changes. The first tape address interval is approximately 0.57 inches in length, while the last is approximately 1.24 inches in length. When data is written to $N$ characters length, as that illustrated under address 3, it can consume adjacent address areas and when the data ends, a void area occurs since the next data block will not be written until the next TAC inter rupt and address segment occur.

## CHAPTER IV

## THEORY OF OPERATION

### 4.1 INTRODUCTION

The SPD-T Magnetic Tape Unit control electronics is located on five INCOTERM circuit boards which function together as a single controller and two Sykes Datatronics, Inc. tape deck control circuit boards. All boards are located within the SPD-T unit. As previously mentioned, the INCOTERM controller boards are letter designated A through E. The corresponding schematics are numbered:

$$
\begin{aligned}
& 013-01-01=A \\
& 013-04-01=B \\
& 013-02-01=C \\
& 013-03-01=D \\
& 013-05-01=E
\end{aligned}
$$

The logic schematics are found in the Field Service Technical Manual, FS 003 (a book of reduced schematics). The Sykes logic will be presented in the next paragraph.

### 4.2 SYKES TAPE DECK CIRCUITRY

The Read/Write assembly operates in either a Read mode or Write mode. In the Write mode the write circuit converts digital logic levels to currents which produce flux patterns in the tape head. A "1" is represented by a positive flux and a " 0 " by a negative flux. As the tape moves past the
head, the magnetic flux polarizes the magnetic oxide on the tape, creating a magnetic record. In the Read mode the tape moves past the head and causes a voltage to be induced in the head which is representative of the flux polarity originally applied to the tape. The signal from the head is a relatively low level. The signal is amplified and converted to the proper logic levels. In addition to the Read/Write operation, the circuit also selects either of two tracks for the operating mode.

### 4.2.1 Functional Description (Tape Deck Electronics)

The following description is accompanied by Figure 4-1, a block diagram of the Read/Write assembly.

The track and mode select circuit selects one (and only one) of the two tracks and determines whether data will be written on, or read from that track. If the Write operation has been chosen, then the write data at the input of the write amplifier will be converted to a push-pull current in the appropriate track of the magnetic tape head. If the Read operation has been chosen, then the output signal of the selected track of the tape head will be transmitted to the read amplifier. This amplifier will then amplify and band limit the signal. It should be noted that during the Write operation, extraneous signals may be processed by the read circuitry due to its high gain characteristics. These signals are ignored.

The output of the read amplifier is passed on to the threshold detector where it is rectified, amplified, and the signal components below a pre-set level are removed. The last operation removes noise at zero crossings while preserving the signal peaks. This signal is then presented to the peak detector, which produces a pulse for each signal peak. Each pulse corresponds to a flux reversal. The pulses are then shaped and amplified in a schmitt trigger and passed to the output buffer where they are used to strobe the data.

In addition to knowing the point at which a transition occurs, the sense (level) of the data must also be determined. This is accomplished by taking a sample of the output of the read amplifier and converting it to a two-level signal in the level detector. This signal is then gated at data


Figure 4-1. SYKES Read/Write Assembly, Block Diagram
transitions in the output buffer and stored until the next transition occurs. This stored signal is the desired read data.

### 4.2.2 SYKES Tape Deck Logic

Figure 4-2 is an overall diagram covering mainly the motor control logic. The power switch applies 115 VAC to the motor circuits. In addition, 115 volts ac isolated and +5 VDC are wired to this circuit. The control signals, direction, speed, and run are fed from the controller to this motor control circuit. The control signals are decoded at Logic Ul, U2, U3, U4 and U5, and provide the operating commands of:

| Fast Reverse | U2 Pin | 11 |
| :--- | :--- | ---: |
| Fast Forward | U2 Pin | 8 |
| Slow Forward | U5 Pin | 6 |
| Slow Reverse | U5 Pin | 2 |
| Solonoid-1 | U1 Pin | 8 |
| MOTION | U1 Pin | 10 |
| Brake Forward | U5 Pin | 12 |
| Brake Reverse | U5 Pin | 4 |

The application of these signals to the forward and reverse motor so that the desired effect is accomplished by the six triac elements. The triac allows bi-directional current with controller gate signals.

Although not physically attached to the circuit board, the photo sensors and micro switches are wired back to the board as illustrated in Figure 4-2.

The Read/Write assembly logic is illustrated in Figure 4-3. The logical flow in this figure is quite similar to the block diagram previously described. The Write data enters the logic at component Ul Pin 13. The signal is amplified and sent to the appropriate head. The head selected (track) can be only one track at a given time. The gain potentiometers R39 and R67 are only active for the track selected. If data is read, the head signal is routed to the read amplifier. The amplified read signal enters the data recovery section with a sample routed through the peak detector for processing and conversion into a suitable read data strobe.

### 4.3 INCOTERM SPD-T ELECTRONIC CONTROLLER

The INCOTERM controller handles the input/output interface between the SPD-T and the SPD 10/20 Display Terminal. Figure $4-4$ is a block diagram of the controller with the interface signals graphically separated. The Bold lines are tape deck signals and the smaller lines are the TPU signals. In operation, the TPU program code is decoded at the controller and action signals are fed to the control section for routing. Some actions are looped back to the TPU (such as status indications, ACK, ect.) while others direct tape deck operation. The sensors located at the tape deck also feed signals to the controller. In the case of data, there is an input data path for data read from tape and an output data path for data to be written on tape. The data register is parallel accessed by,


Figure 4-2. Overall Diagram



TPU Clocks
From Tape Deck)
Figure 4-4. Simplified Block Diagram, SPD-T Controller
and has access to the TPU input/output bus lines (INB/OTB 00-07). The data transfer is parallel between the TPU and controller and serial between the controller and tape deck.

### 4.3.1 Controller Timing (Print 013-01-01)

Table 4-1 and 4-2 illustrate the timing relationship for the Read and Write mode of operation. The timing is effective for one eight bit character with double width parity. The arbitrary digital character is 01111010 . Cassette controller board A, Print 013-01-01, includes the majority of the timing generation. $\emptyset 1, \emptyset 2, \emptyset 1 \mathrm{~A}$ and $\emptyset 1 \mathrm{~B}$ are derivatives of the internal crystal oscillator. The oscillator provides a raw frequency of 2.048 MHz which is available for use as a high speed clock and input to the frequency divider M28. The element M28 is an SN 7493 which functions as a four bit binary counter. The output A is looped back to input B to provide a divide by 16 count as decoded at M27, pins 1, 2, 4 and 5. The frequency of the output (M27, Pin 6) is 128 kHz . This signal is fed as the input to a second 7493, M22. The output of M22 provides a true input to AND gate M21, Pins 3, 4 and 5 on a count of eight and a count of 16. At the count of eight, M22 output D is low and M21 Pin 6 is low which enables M23, Pins 8 and 9 and produces the $\emptyset 1$ signal. At the count of 16 output D (M22) is high and M27 Pin 6 is again true (low). The D output is inverted and the inputs to M23 (pins 11 and 12) are now true, producing a shifted clock called $\emptyset 2$.

Phase 1 is further sub-divided by applying the signal to the clock input of flip flops M16 (Pin 1 and 6). The $\bar{Q}$ output is gated by $\phi 1$ at AND gate M17 (Pins 9 and 10). The resulting signal (low) is inverted at M15 and is called $\emptyset 1 \mathrm{~A}$. The $Q$ output is gated at M17, Pins 12 and 13, producing the $\emptyset 1 \mathrm{~B}$ clock. The result is that $\emptyset 1$ is divided by two and two outputs exist which are phase shifted by 180 degrees.

The above clock signals are illustrated in Table 4-1. When the Read operation is performed, the signal which synchronizes the data transfer is the Read clock. The character is formatted by phase encoding, which results in two transitions occurring for each data bit. This method is simply illu strated in Figure 4-5.

TABLE 4-1. READ TIMING DIAGRAM (CHARACTER=01111010) (All Signals Located On Board A)


TABLE 4-2. WRITE TIMING DIAGRAM (CHARACTER=01111010)
(All Signals Located On Board A)



Figure 4-5. Example Of A Phase Encoded Character (01111010)

The Read Clock creates a pulse at a rate equal to twice the actual bit time. The signal enters the controller at pin 39 where it is processed for the appropriate logic level (inverted) and applied to flip flops M12. The flip flops present true conditions at AND gate M11, pins 1 and 2 after one full bit time has occurred (count of 3). The resulting low at pin 3 AND gate MII feeds through OR gate M11, pin 12 to clock the sync flip flop and to AND gate M9 where the output (pin 4) is in sync with the data and allows the counter to operate. The waveform illustrated in Figure 4-1 for M10 pin 11 indicates the phase 1 B reset of this flip flop. The Read Data waveform at flip flop Ml0 pin 14 is processed through the gating (M4, M14 and M26) and fed serial by bit into flip flop M1, pins 4 and 16. This flip flop is clocked by $S R$ SCK, the shift register shift clock which shifts the eight data bits from M1 pin 15 and into the serial/parallel register (Schematic 013-02-01, Board C). During the second half of T9 the data bits are parallel enabled by the clock signal SR PCK (Shift Register Parallel Clock Enable). The remaining double width parity is decoded at flip flop M13 and M1, resulting in the final clock for this character. The 10 bit times are decoded at the four bit serial/parallel register M24.

In the Write mode (Table 4-2) the same character bit sequence is presented. The parallel data (eight bits) are loaded into the serial/parallel registers M14 and M16 on Board C. The data is shifted out in serial (S DATA

OUT) and fed into Board A on Pin 33. The data then has parity added and is sent to the Sykes logic to be written on tape.

### 4.3.2 Controller Data Register (Print 013-02-01)

This schematic presents the logic located on controller Board C. The data registers perform both the eight bit parallel data interface to the TPU input and output bus and parallel-to-serial, serial-to-parallel data handling to and from the tape deck logic. The parallel register is composed of two four bit flip flop registers, M13 and M15. On the input side there is select gating which allows data entry from two sources. One is from the TPU output bus, bits 00-07, the other is from the parallel output of the serial/parallel register. On the output side there is also gating which allows the program to select eight data bits or six status bits on the input bus line to the Terminal.

The parallel/serial register is composed of two (4 bit) 7495's connected in eight bit operation. The register accepts both parallel and serial inputs and provides parallel and serial outputs, depending on the mode of operation. The parallel inputs are fed from the output of the data register and the serial input is effectively the taped data. The outputs are fed in parallel to the data register select input gates and in the appropriate combination to the prime condition decoders. The serial output is effectively the data to be written on tape.

The decoders are wired to the data bits such that three prime conditions are detected when they occur. The program command for Start of BOOT/End of BOOT, Sync and Leader are detected by AND gates M9, 10 and 8 respectively. The results of the detected conditions are logically processed to produce the mode control and clocking for the state registers M24. The outputs provide operating status commands which signal normal operation, leader, BOOT and reset run circuits.

### 4.3.3 Control Circuitry (013-04-01)

The various control signals dealing with both the data and operation of the tape deck are found on the remainder of the circuit boards. Board B (Print 013-04-01) and Board D (Print 013-03-01) decode the program commands
and produce the resultant control signals. Circuit board E (Print 013-05-01) performs a rather miscellaneous control dealing with a wide variety of signals.

The programmed TYPE code is a two bit code which comes from the TPU output bus (low truth) and is decoded on Board B to provide the test, control, Read and Write commands. The FUNC code is a four bit function code which is decoded to provide the TYPE code with 16 possible command signals (Hex). The following table summarizes the controller commands.

| TABLE 4-3. SPD-T CONTROLLER COMMANDS |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { TYPE bits } \end{aligned}$ |  | FUNC bits (Hex) |  |  |  |  | Command |
| TIO | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Acknowledge if Controller is present. |
|  | 0 | 0 | 1 | 0 | 1 | 0 | A | Acknowledge if at Beginning of Tape. |
|  | 0 | 0 | 1 | 0 | 1 | 1 | B | Acknowledge if Tape Address Changes. |
|  | 0 | 0 | 1 | 1 | 0 | 0 | C | Acknowledge if on Clear Leader |
|  | 0 | 0 | 1 | 1 | 0 | 1 | D | Acknowledge if no Read Error |
|  | 0 | 0 | 1 | 1 | 1 | 0 | E | Acknowledge if no Tape Stop |
|  | 0 | 0 | 1 | 1 | 1 | 1 | F | Acknowledge if no Read Error or Tape Stop. |
| CIO | 0 | 1 | 0 | 1 | 0 | 0 | 4 | Enable TAC Interrupts |
|  | 0 | 1 | 0 | 1 | 0 | 1 | 5 | Disable TAC Interrupts |
|  | 0 | 1 | 0 | 1 | 1 | 0 | 6 | Read Track A |
|  | 0 | 1 | 0 | 1 | 1 | 1 | 7 | Read Track B |
|  | 0 | 1 | 1 | 0 | 0 | 0 | 8 | Write Track A |
|  | 0 | 1 | 1 | 0 | 0 | 1 | 9 | Write Track B |
|  | 0 | 1 |  | 0 | 1 | 0 | A | Fast Forward |
|  | 0 | 1 | 1 | 0 | 1 | 1 | B | Rewind |
|  | 0 | 1 | 1 | 1 | 0 | 0 | C | Enter BOOT |
|  | 0 | 1 | 1 | 1 | 0 | 1 | D | Unmask Interrupt |
|  | 0 | 1 | 1 | 1 | 1 | 0 | E | Mask Interrupt |
|  | 0 | 1 | 1 | 1 | 1 | 1 | F | Stop |
| RIO | 1 | 0 | 0 |  | 1 |  | C | Read Data |
|  | 1 | 0 |  | 0 | 1 | 0 | A | Read Status |
| WIO | 1 | 1 | 0 |  | 1 |  | 6 | Write Data |
|  | 1 | 1 | 1 | 0 | 0 | 0 | 8 | Erase |

The TPU TYP code enters controller board B (Print 013-04-01) on Pins 20 and 28. The TIO is decoded at AND gate M7, Pins 2 and 3 . The signal is then fed to AND gates M14, Pins 4 and 13, where the function and address requirements are detected. The resulting commands are distributed to to appropriate circuits and acknowledges through OR gate M16. The Read and Write IO code is detected with address at AND gate M20, Pins 9 and 10. As indicated in Table 4-3, there are only two command functions for each mode. The R/W TYPE signal is routed to AND gates M21, pin 4, and M22, Pins 3 and 11, where the various function bits enter the circuit from Card D. The Read data is enabled through M22 (Pin 8) M26 (Pin 5) and finally to M26 (Pin 11) which causes the data buffer transfer to the INPUT BUS. The Read status signal is enabled at M21, Pin 6. The CIO is decoded at AND gate M7. Depending on the function, there are some 12 different actions caused by the CIO.

Also located on Board B are the acknowledge and interrupt circuits. Most of the test I/O's (TIO) are signals which detect specified conditions and signal that condition to the TPU via the acknowledge ACK line, Pin 84 Board B. The group of AND gates M15, Pins 8 and 11, M9, Pins 8 and 11, and OR gates M19, pin 10, M8, Pin 6, M20, Pin 3, and M11, Pin 10, feed M16, through M14 to produce a signal at the ACK flip flop M30, Pin 14, producing an ACK signal through M6 at Pin 6.

The TPU inter rupt select IN is present on pin 77, Board B. If the controller is not conditioned to inter rupt the select is passed out on Pin 79. If the controller does require service and the inter rupt is enabled ( Pin 44 ), an interrupt is generated at $\operatorname{Pin} 81$.

The function decoder is located on Board D (Schematic 013-03-01). The four bits enter M3, a 4 to 16 decoder, from which they are applied as illustrated in Table 4-3. A large portion of the action signals to and from the tape deck originate or end at the circuitry on Board D. Dual flip flops M8 are strobed by a CIO derivative to produce the Enable/Disable TAC signal on output Pin 38 (flip flop pin 10) and mask/unmask interrupts on output pin 40 (flip flop pin 15). Dual flip flops M14, similarly, are clocked by a TYPE

CIO signal. Pin 10 and 11 produce the track select outputs with Track $A$ on output Pin 22 and B on 16 . The Read/Write select is output on Pin 26 (Read) and Pin 28 (Write). Dual flip flop M1l produces the tape deck motion signal Fast/Slow from one flop and Forward/Reverse from the other. Both flip flops are clocked by a CIO derivative CK B. The last two flip flops in this series of outputs are M5 which produce the Run/Stop and BOOT select signals. The Run/Stop flip flop is clocked with the same signal as the Mll flip flops. The BOOT flop is clocked by a different derivative of the CIO, in this case CK A is used.

The various switches associated with the tape deck provide manual operating signals to Board D. The conditions, AUTO and MANUAL are routed to the controller from opposite poles of the same switch. The MANUAL signal is found on input pin 13 where it is ANDed with the MOTION signal. The switch signal for AUTO is entered at pin 7 with pin 9 serving as the common for both 7 and 13. Drawing a line between pins 7 and 9 simulates the setting for the AUTO mode. Following the signals through, bow tie flip flop M1, Pin 8 is low, resulting in a not manual signal at output Pin 8. Simulating the opposite switch setting results in a high signal on Pin 8 and a high on Pin 6, which is the truth for the MANUAL mode.

A similar action occurs at Pins 42,50 and 25 , which are connected to the START switch at the front panel. When the switch is activated (Pin 50 and 42 shorted), a high signal is present on Pin 6, M2. Pin 3 is low to Pin 4 and Pin 6 is high to Pin 1 of one shot M7. M7 is enabled by the ANDing of the MANUAL mode signal and produces a MANUAL START pulse on Pin 21 when the Start switch is released.

The third front panel switch is the BOOT/REWIND switch. The switch wiring is to Pins 32, 48 and 34 with Pin 48 the common (ground). When the switch is positioned to REWIND, a low signal is present on Pin 9, M2. Pin 8 is latched high and is fed to M29, Pin 4, where an ANDing condition occurs with a true manual signal on Pin 5 (high). OR gate M29 is conditioned and feeds a low to Pin 2, M23, which in turn enables a high to the J input Pin 4, flip flop M11. This flop produces a fast signal. The output of M29 (Pin 6) is inverted
and fed to the J input of the FWD/REV flip flop, creating a Reverse signal. The same signal applied to the FWD/REV flop (Pin 9) is gated through M30 to produce a RUN condition at flip flop M5.

When the BOOT/REWIND switch is placed to the BOOT position a low signal is present on Pin 2, M2. The low is latched at Pin 8 and enables Pin 8 of AND gate M22. Assuming the tape is not on clear leader, the EOT/ BOT signal is true at Pin 9, the output; Pin 10 is ANDed with the manual signal and output from M29, Pin 8 through inverter M8 and to the J input of the BOOT flip flop. Table 4-4 represents the timing for the BOOT mode with an expanded time representation of the ACK and data transfer timing. The manual start pulse initiates the BOOT mode as previously discussed. The Speed signal produces a 200 ms delay to get the tape up to speed before any operation is performed as dictated by the State 0 . When State 1 occurs, a TPU BOOT signal is sent to the display. The TPU BOOT stays high through the remaining states data transfer and End BOOT. State 2 is Start of BOOT, followed by State 3 which is Read BOOT. State 3 stays high for the duration of the BOOT data. The RDY clock and BOOT acknowledges enable the Boot data to the TPU. At the end of the BOOT record, State 4 is enabled and provides an End BOOT and resets the running condition. The time expanded diagram at the bottom of Table 4-4 provides a more in-depth view of the circuit outputs involved in generating the BOOT ACK and data transfer.

Schematic 013-05-01, in addition to the BOOT circuits, contains tape deck interface wiring to light particular lamps, accept and discriminate lamp sensor signals and miscellaneous other functions. The tape address sensor inputs a signal at Pin 37 where the one shot M21 shapes the signal for application to AND gate M7, Pin 11. The TAC signal is enabled or disabled at Pin 12 by the programmed command. The Power ON lamp signal is a 5 volt signal level from the cassette +5 volt supply. The level is inverted at M1, Pin 8 and wired to the front panel. The BOOT lamp is triggered by the BOOT mode signal. The high signal is inverted at M1, Pin 6 and wired to the front panel. If operator intervention is required, the conditions that require intervention are output from OR gate M14, Pin 12. The high is inverted at M2, Pin 8 and

TABLE 4-4. BOOT MODE TIMING

wired to the lamp on the front panel. The MOTION lamp is fed from M2 Pin 6.
Flip flops MII provide a logical delay of one character so that the last character is not lost vhen a mode change occurs. Flip flop M5 similarly delays a mode change from Read/Write to Erase so the last good data character is not erased.

### 4.4 TPU 50 PIN I/O BUS PLUG - CONTROLLER INTERFACE

### 4.4.1 Description

This paragraph described the method for interfacing controllers to the $50-$ pin I/O plug on the SPD 10/20 (J9 on 005 and 006 units and J15 on 010 units). The standard SPD 10/20 is wired to allow the interfacing of one SPD-L Program Loader. To interface an SPD-T Magnetic Tape Unit to the I/O plug requires modifications to the SPD 10/20.

### 4.4.2 Standard SPD 10/20 Configuration

Figure 4-6 is a simplified block diagram of the wiring to the I/O plug, for the standard configuration. The only device that can connect to J9 or J15 with this configuration is the SPD-L Program Loader. Referring to Figure 4-6, observe that the I/O plug contains only one address and one interrupt line. Also the interrupt select line to the plug is wired in parallel with the inter rupt select line to controller Cl.

### 4.4.3 Special SPD 10/20 Configuration

Figure 4-7 is a simplified block diagram of the I/O plug wiring for use with the SPD-T. With this wiring configuration it is possible to connect one or two Magnetic Tape Units, or one Magnetic Tape Unit and one Program Loader to the I/O bus. (This configuration is also usable for new controllers that are designed to connect to the 50 -pin I/O bus plug.) Comparing Figure $4-7$ to Figure 4-6, the following differences should be noted.

1. The special configuration has two address and two interrupt lines wired to the I/O plug,
2. In the special configuration the interrupt select line to the I/O plug is connected from the output of the last active controller,

* on 010 units these signals are routed from Cl

| C | C 1 | C 2 | C 3 | C 4 |
| :---: | :--- | :--- | :--- | :--- | :--- |

Pin 31


CA Pin 32


Interrupt Select


Co


Address, Interrupt. I/O Signals


Pins on I/O plug J9 or
J 15
Remaining pins
30
28
$\square 2,40,41$

Figure 4-6. Standard Configuration I/O Plug Wiring

3. The special configuration has four additional ground wires added to the I/O plug.

### 4.4.4 Conversion From Standard <br> Configuration To The Special Configuration

Table 4-5 shows the wiring changes required to convert the standard configuration to the special configuration for using magnetic tape cassettes. The wire for the interrupt select line may be routed from one of two points. The wire may be connected to Pin 32 of the last active controller, or it may be connected to Pin 32 of C8 and looping (jumper) boards (part number 001-15-07-702) placed in all unused slots.

### 4.4.5 Option Block Wiring

Option blocks STB-4 and STB-13/14 on the TPU Control Board must be modified as follows to generate the required address and interrupts:

STB-4 (Interrupt)
Delete the present wire from Pin 2 and use the following table to rewire the interrupt lines:

| I/O Device | Option Pin \# |  | Interrupt \# |
| :--- | :---: | :---: | :---: |

STB-13/14 Address
Delete wire from Pin 9 and use the following table to rewire the address lines:

| I/O Device | Option Pin \# | Interrupt \# |  |
| :--- | :---: | :---: | :---: |
| Cassette \#1 | 9 | 0 |  |
|  |  | 1 | 8 |
| Cassette \#2 or | 26 | 2 | 7 |
| Program Loader |  | 3 | 6 |
| (If Present) |  | 4 | 5 |
|  |  | 5 | 4 |
|  |  | 6 | 3 |
|  |  | 7 | 2 |
|  |  |  | 1 |

TABLE 4-5. WIRING CHANGES TO CONVERT STANDARD CONFIGURATION TO SPECIAL CONFIGURATION

| Change Number | Purpose of Change | Method of Achieving Change |
| :---: | :---: | :---: |
| 1 | To add additional address line. | Add wire: A13 Pin 55 to J9 or J15 Pin 43. |
| 2 | To delete interrupt line to C7 for useage by the I/O plug. | Delete wire: Bl3 Pin 31 to C7 Pin 30. |
| 3 | To add additional interrupt line. | Add wire: B13 Pin 31 to J9 or J15 Pin 44. |
| 4 | To rewire inter rupt select line. | Delete wire: Bl3 Pin 16 to J9 Pin 31 (005 and 006 units) or |
|  |  | Delete wire: C1 Pin 31 to J15 Pin 31 (010 unit) |
|  |  | Add wire: <br> From Pin 32 of the last active controller to J9 or Jl5 Pin 31 <br> (See Section 4 for a more detailed description.) |
| 5 | To add additional ground wires if not installed at the factory. | Add wires: J9 or J15 Pins 47, 48 49 , 50 , to a lug and connect to chassis ground. <br> (NOTE: This change may have been installed at the factory.) |

### 4.4.6 Special Considerations

Figure 4-8 is included to illustrate how the address and interrupt lines are distributed between two devices. The first SPD-T uses the address and inter rupt signals present at Pins 28 and 30 respectively. The first cassette also takes the address and inter rupt signals present on Pins 43 and 44 and routes them to the second device on Pins 28 and 30.

The maximum allowable cable length from the SPD 10/20 to the first SPD-T is three feet. The maximum allowable cable length between the first SPD-T and the second SPD-T (or SPD-L) is two feet.

It should be noted that as a result of these modifications, controller slot C7 cannot contain an interruptable controller because the interrupt line has been rerouted for use by the second controller on the I/O plug. Controller slot C7, however, can contain a non-interrupting controller for example a BOOT Controller or a Cyclic Check Controller.


Figure 4-8. Signal Distribution Between I/O Devices

## CHAPTER V

MAINTENANCE AND REPAIR

### 5.1 TIME PHASED MAINTENANCE

### 5.1.1 Daily Maintenance

The parts of the tape transport mechanism that touch the tape should be kept very clean. Dust and lint contamination can prevent proper contact between the tape and the tape head which results in error or data dropouts.

The pressure roller, tape guide and tape head should be cleaned periodically: once a day, or after approximately eight hours of tape operation, whichever comes first. The cleaning procedure is described below.

## NOTE

Pinch roller and capstan must not be flooded with cleaner. Sharp objects should not come in contact with the tape path as permanent damage may result.

1. Turn off the Tape Unit power switch. The POWER ON indicator should be extinguished.
2. Open the receiver and remove the cassette, if one is installed.
3. With the receiver open to the normal stop, depress the detent and open the receiver fully. Use a mechanical pencil or similar device to depress the detent as shown in Figure 5-1.
4. Moisten a 'kimwipe" (or equivalent) or a small piece of lint free cloth or lint free absorbent paper with tape head cleaner.

### 5.1.1 Daily Maintenance (Continued)

5. Insert the end of a small rod or similar device into the hole in the tape head bar (see Figure 5-2) and pull downward and hold to expose the pressure roller, tape head and tape guide (see Figure 5-3). Wipe the tape head, tape guide and pressure roller clean.
6. The receiver catch must be positioned as shown in Figures 5-2 and 5-3; otherwise, the receiver will not close properly. If inadvertantly tripped, return the catch to the position shown.


Figure 5-1. Releasing the Receiver Detent


Figure 5-2. Method Used to Expose Parts for Cleaning


Figure 5-3. Tape Head Exposed

### 5.1.2 Quarterly Maintenance

A self-contained fan is used to cool the Magnetic Tape Unit. Air enters through the foam plastic filter on the rear of the unit. The filter prevents the entry of air borne dust and lint through the cooling fan and should be cleaned or replaced every 90 days. The following procedure should be used.

1. Turn off the Tape Unit power switch. The POWER ON indicator should be out.
2. Pull the filter from its frame.
3. Vacuum clean the frame to remove any dust dislodged by the filter removal.
4. Wash the filter in a detergent solution, rinse, wring out and dry thoroughly.
5. Replace the filter in its frame and carefully tuck in the edges.

### 5.1.3 Semi-annual Maintenance

1. Clean the tape head carriage solenoid as follows:
a. Remove the front panel of the unit.
b. Pull the solenoid plunger pin out and remove the plunger.
c. Using a foam or cotton swab (such as a "Q-tip") saturated with a cleaner (Tape head cleaner such as MS200 Magnetic Tape Head Cleaner can be used), thoroughly clean out the solenoid cavity.
d. Clean and replace the solenoid plunger and pin.
2. Adjust the tape head carriage solenoid as follows:
a. Remove the Read/Write circuit board by disconnecting the tape head wires and removing the screws in the four corners of the board.
b. Loosen the solenoid mounting screws and push the plunger firmly into the solenoid. The tape head carriage moves to the tape head engaged position.
c. Move the solenoid assembly to the left until the plunger bottoms within the solenoid.
d. Scribe a reference mark on the plunger, flush with the front of the solenoid, to indicate the plunger seal position.
e. Move the solenoid to the right 0.02 to 0.03 inches, and tighten the mounting screws.

### 5.1.3 Semi-annual Maintenance (Continued)

3. Check the capstan drive belt tension. The drive belt tension should allow approximately $1 / 16$ inch deflection on the belt midway between pulleys when a one-pound pressure is applied. If this is not the case, proceed as follows:
a. Remove the front panel from the unit.
b. Loosen the capstan drive motor mounting bracket screw lo cated approximately one inch below the power switch.
c. Reposition capstan drive motor until the conditions stated above are met.
d. Tighten the mounting bracket screw securely.
4. Check the adjustment of the pinch roller. The pinch roller should be compressed 0.013 inches when the tape head carriage is in low position. To test and/or adjust for proper pinch roller/capstan contact, proceed as follows:
a. Remove the front panel from the unit.
b. Place a 0.013 inch guage or shim on the top surface of the lower tape head carriage stop.
c. Depress tape head carriage cam until the tape head carriage is firmly contacting the shim.
d. The pinch roller should now be in light contact with the capstan. If not, loosen the pinch roller housing screw and position the pinch roller housing so the pinch roller lightly contacts the capstan as step c is performed.
e. Repeat steps c and d using a 0.014 inch guage or shim. The pinch roller should not contact the capstan.
f. Make sure the pinch roller house is vertical.
g. Tighten the pinch roller housing retaining screw securely.

### 5.2 CASSETTE PREVENTATIVE MAINTENANCE

The cassettes are loaded with magnetic tape which must be protected against physical damage, exposure to magnetic fields and contamination from dust and lint. These conditions cause errors or permanent loss of data stored on the tape.

The following handling and storing practices should be adhered to.

### 5.2 CASSETTE PREVENTATIVE MAINTENANCE (Continued)

l. Keep cassettes in the protective containers.
2. The insides of the protective container should be kept clean. Close the cover when the cassette is removed for use.
3. Rewind the cassette before removal from the Tape Unit. This exposes the clear leader at the cassette openings instead of the oxide-coated tape which reduces the chance of physical damage to the tape. The transparent leader and tape must be given equal protection from fingerprints and dirt because dirt can be transferred between wraps of tape on the reel.
4. When handling the cassettes, avoid touching the tape or leader surfaces. Fingerprints may cause data drop-outs and lead to dirt accumulation.
5. Protect the cassettes from direct sunlight, moisture and solvents. These could deform the tape or soften the tape binder.
6. Do not expose the cassettes to high temperature.
7. Do not expose the tape to magnetic fields such as those from magnets, motors, transformers or TV sets.
8. Store cassettes in protective containers at normal room temperature and average humidity.
9. Cassettes shipped during very cold weather should be allowed eight hours to reach normal environmental temperature before use. Very cold tape may be physically distorted if it is subjected to the start and stop conditions performed by the Magnetic Tape Unit.

### 5.3 LAMP ADJUSTMENTS

### 5.3.1 BOT/EOT Sense Lamp Position

Should it become necessary to replace a BOT/EOT sense lamp, the following adjustment is required:

1. Adjust the EOT lamp depth (retained by friction) until the output of the phototransistor is at a minimum. The minimum on voltage should not exceed 500 mv .
2. Secure the bulb.
3. Completely cover the photosensor and verify that the sensor output voltage is 1.05 volts or greater.

### 5.3.2 TA Sense Lamp Position

The following adjustment is required when a Tape Address sense lamp is replaced.

1. Rotate the shaft encoder until the lamp is centered between vanes (open).
2. Adjust the lamp position for minimum output from the TA phototransistor. Minimum ON voltage should not exceed 500 mv .
3. Secure the lamp by trapping the lead wires in the wire slot.

### 5.4 CONTROLLER CALIBRATION

The controller board E contains a potentiometer (R2) which sets the time of a one shot multivibrator. The potentiometer should be set to obtain a 200 ms positive pulse at TPl (see Figure 3-4, page 3-8). The following procedure allows observation and adjustment of this signal.

1. Load the SPD-T exercise program (\#C-7113-0-1-2).
2. Remove program tape and replace with a scratch tape.
3. Place AUTO/MANUAL switch to AUTO.
4. Type $J=0800$ CR and execute test $1 B N$ by typing same. (Tape starts and stops repeatedly.)
5. With oscilloscope probe on Board E, TPl, adjust potentiometer R2 to obtain a 200 ms positive pulse.
6. Type 4 to terminate test.

### 5.5 TAPE DECK CALIBRATION

Should it become necessary to adjust for customer tape, or to replace either a tape head or Read/Write electronics board, the following procedure must be followed to reset the proper circuit gain.

1. Install the circuit board or tape head and make all operating connections.
2. Reload cassette exercise program and insert scratch tape.
3. Clean the tape head and tape path.
4. Type $J=0800$ CR.
5. Execute test lAN by typing lAN. With tape in motion, place MANUAL/AUTO switch in MANUAL and tape will stop near end of tape.
6. Place MANUAL/AUTO switch in AUTO.
7. Type 4 to reinitiate program.
8. Repeat 5, 6 and 7 above except for Track B (Type in IBN).
9. Power down (TPU before cassette), extend Board A and power up (cassette before TPU).
10. Read Track B (type in 2BN). With scope probe on Read/Write Electronics TP-1 (Figure 3-2) and triggering scope from signal at M25-13 on Board A, adjust R39 (Figure 3-3) for the maximum undistorted signal (Figure 5-4). This is the point just before the negative peak shows signs of clipping.
11. Terminate 10 above by typing 4.
12. Read Track A (type in 2AN). With probes connected as in 10 above, adjust R14 until waveform in 10 above is obtained.
13. Terminate 12 above.
14. Repeat 10 and 11 above, note the output, then read Track A and compare. If the signals are identical, end test. If they are not identical, repeat step 12 and subsequent steps.

## NOTE

Constant use of a given cassette results in two occurances: oxide is worn from the tape and some oxide particles penetrate or cause a film build up on the tape head. Either of these conditions can cause reduced output voltages at TPl. When performing this test, use a relatively new tape and clean the head. When in the field and TPl looks like it requires an adjustment, clean the head and use a known good (not extremely used) tape before making an adjustment.


Figure 5-4. Read/Write Signal A) Point Before Clipping B) Clipped

### 5.6 SPD-T 60/50 HZ CONVERSION PROCEDURE

Conversion of the operating characteristics are performed in the factory. However, upon installation, in order to verify that an SPD-T is properly configured, the following information is provided.

Parts Used:
50 Hz Pulley Sykes \#1001 A1712
Serial Number Sticker
Special Tools:
1 pound scale
. 050 inch Hex Key Wrench
11/32 Box Wrench
Procedure:
(Refer to Figure 3-1, Page 3-2 for an illustration of the gene ral area.)

1. Locate the capstan mounting bracket and loosen the bolt.
2. Position the capstand drive motor so that the capstan belt can be removed from the pulley.
3. Exchange the capstan pulley. Small diameter end of pulley faces capstan motor. ( 50 Hz is larger than 60 Hz pulley.) The set screw seats on the flat portion of the motor shaft.
4. Replace the belt and position the capstan drive motor to allow approximately $1 / 16$ inch deflection of the belt at the mid point when a one pound pressure is applied.
5. Tighten the mounting bracket bolt securely.
6. Change transformer taps to operate at the 50 Hz input voltage.
7. Replace the Serial Number sticker to reflect 50 Hz operation.

### 5.7 POWER SUPPLY ADJUSTMENTS

The SPD-T uses a crane multivoltage power supply, as illustrated in Figure 5-5. The $+5, \pm 12$ and +24 volts are potentiometer adjustable. The power supply is internally fused such that an inoperative voltage may require removal of the supply for access to the faulty fuse. Figure 5-6 illustrates the power supply interwiring with the other subassemblies.



Figure 5-6. Simplified Internal Wiring Diagram

## APPENDIX A

SIGNAL NMEMONICS AND
POINT TO POINT WIRING

## A. 1 GENERAL

This section is presented to provide the Field Engineer with a brief description of the signal nmemonics and point to point wiring for any given signal in the SPD-T. Table A-1 provides a controller signal summary, Table A-2 is the power and interelectronics cabling, and Table A-3 is the Input/Output signals.

Table A-1. SPD-T Controller Signal Summary

| Nmemonic | Definition | WIRED |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | From |  | To |  |
|  |  | Board | Pin | Board | Pin |
| H S CK | High Speed Clock | A | 77 | C | 77 |
| T9 | Parity Timing Pulse Inverted | A | 27 | C | 70 |
| T9 | Parity Timing Pulse | A | 41 | C | 63 |
|  |  | C | 63 | E | 42 |
| $\overline{\text { (READ)(STATE 0) }}$ | Programmed Read In- | A | 69 | C | 73 |
|  | struction ANDed with State Zero. Both Inverted | C | 73 | E | 73 |
| W MODE STROBE | Write Mode Clock | A | 19 | E | 65 |
| W MODE | Write Mode | A | 21 | E | 67 |
| ERASE TAPE | Erase Tape Signal | A | 37 | E | 81 |
| SR MODE | Mode Control I/O Data Register. Low = Serial Shift Enable | A | 7 | C | 67 |
| RDY CK | Ready Clock for Buffer | A | 3 | B | 42 |
|  | Register R/W | B | 42 | E | 44 |
| D. O. CK | Drop Out Clock | A | 31 | C | 83 |
|  |  | C | 83 | E | 40 |
| SR PCK | Shift Register Parallel | A | 20 | C | 26 |
|  | Clock | C | 26 | E | 49 |
| W MODE | Not Write Mode. <br> Part of Tape Erase Ckt. | A | 53 | D | 73 |
| PARITY ERROR | Bit 2 of Status Word Indicative Parity Error | A | 8 | C | 38 |
| $\overline{\text { PARITY ERROR }}$ | Not Parity Error | A | 4 | B | 31 |
| D.O. ERROR | Drop Out Error | A | 25 | C | 76 |
|  |  | C | 76 | E | 47 |
| CLR STATUS | Program Initial Clear | A | 22 | B | 56 |
|  | Status Flip Flops | B | 56 | E | 46 |
| PAR DET | Parity Detect | A | 26 | E | 51 |

Table A-1. SPD-T Controller Signal Summary Cont'd.

| Nmemonic | Definition | WIRED |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | From |  | To |  |
|  |  | Board | Pin | Board | Pin |
| $\overline{\text { STATE } 2+\text { STATE } 3}$ | Boot State Error | A | 15 | E | 13 |
| SR SCK | I/O Shift Register Serial Mode Clock | A | 16 | C | 28 |
| 9th BIT | Not 9th Parity Bit | A | 14 | C | 69 |
| S DATA OUT | Serial Data Out | A | 33 | C | 22 |
| $S$ DATA IN | Serial Data In | A | 10 | C | 57 |
| BOOT MODE | Bootstrap Operation | B | 10 | C | 74 |
|  |  | D | 60 | E | 10 |
|  |  | C | 74 | D | 60 |
| MANUAL MODE | Manual Operation | B | 14 | C | 8 |
|  |  | C | 8 | D | 4 |
| CK C | TAC and Mask Flop Clock Signal | B | 51 | D | 31 |
| CK D | Track and Mode Clock | B | 9 | D | 46 |
| CK A | Motion and Boot Mode Clock | B | 15 | D | 67 |
| MAN START PULS* | Manual Start Pulse | B | 54 | D | 21 |
| $\overline{\text { MOTION }}$ | Not Motion | B | 32 | D | 10 |
| $\overline{\text { EOT/BOT SENS }}$ | End of Tape/Begining | B | 63 | D | 59 |
|  | of Tape Sensor | D | 59 | E | 53 |
|  |  | E | 53 | Jack | 10 pin 79 |
| RESET FWD LP |  | B | 80 | E | 19 |
| CK B | Inverted Clock A | B | 76 | D | 70 |
| FWD LP |  | B | 78 | D | 61 |
| RESET RUN | Reset Run/Stop Flip Flop | B | 49 | D | 74 |
|  |  | D | 74 | E | 61 |
| START REWIND | Rewind Command | B | 71 | D | 44 |
|  |  | D | 44 | E | 25 |
| EOT/BOT | End of Tape, Beginning of Tape | B | 48 | D | 37 |

Table A-1. SPD-T Controller Signal Summary Cont'd.

| Nmemonic | Definition B | WIRED |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | From |  | To |  |
|  |  | Board | Pin | Board | Pin |
| READ | Enable A Read Data | B | 34 | D | 26 |
|  | Operation | D | 26 | C | 71 |
| BUFFER STROBE | Enable Data Register | B | 40 | C | 75 |
| $\overline{\text { CPT 02 }}$ | Inverted System Clock 2 | B | 22 | D | 33 |
|  |  | D | 33 | E | 71 |
| FN B | Programmed Decode Function B | B | 39 | D | 51 |
| FN A | Programmed Decode Function A | B | 53 | D | 49 |
| (FN6 + FN8) | Programmed Function (6 or 8) | B | 65 | D | 14 |
| STATUS INB | Enable Status On Input Bus | B | 59 | C | 15 |
| BOOT MODE | Enables Buffer To Input Bus | s B | 19 | D | 66 |
| TAC ENB | Not Tape Address Change | B | 21 | D | 38 |
|  | Enable - | D | 38 | E | 3 |
| BUFFER INB | Buffer Enable To Input Bus | B | 67 | C | 13 |
| INITIAL | Initialize | B | 55 | D | 69 |
|  |  | D | 69 | E | 60 |
| STATE 2 | Decode Data State 2 | B | 74 | C | 72 |
|  |  | C | 72 | E | 15 |
| GO WRITE | Controller Write Data | B | 72 | D | 19 |
|  | Enable | D | 19 | E | 56 |
| SET DATA SER | Set Data Service Flip Flop | B | 83 | E | 45 |
| TAC* | Tape Address Change | B | 61 | E | 7 |
| SR BUFFER | Serial Register Data Enabled To Buffer Programmed | B | 60 | C | 65 |
| ENB INT | Enable Interrupt From Mask/Unmask Flip Flop | B | 44 | D | 40 |
| BOOT ACK | Boot Acknowledge | B | 52 | E | 66 |
| BOT | Not Beginning of Tape | B | 37 | D | 79 |

A-4

Table A-1. SPD-T Controller Signal Summary Cont'd.

| Nmemonic | Definition | WI RED |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | From |  | To |  |
|  |  | Board | Pin | Board | Pin |
| FN C | Program Decode <br> Function C | B | 41 | D | 57 |
| FN D | Program Decode Function D | B | 43 | D | 27 |
| FNE | Program Decode Function E | B | 47 | D | 55 |
| FN F | Program Decode Function F | B | 45 | D | 53 |
| MOTION ALLOW | Not Motion Allowed | B | 7 | D | 76 |
| OP INTER REQ |  | B | 69 | C | 56 |
|  | Required | C | 56 | E | 20 |
| DROPOUT | No Dropout | B | 33 | E | 32 |
| MANUAL MODE | Not Manual Mode | B | 25 | D | 8 |
| PROGRAM ERR | Program Error | B | 57 | C | 34 |
| MOTION | Tape Motion | E | 22 | C | 14 |
|  |  | B | 27 | Jack | 10 pin 69 |
|  |  | C | 14 | B | 27 |
| WRITE ERROR | Write Error | B | 3 | D | 43 |
| R/W STRB | Read Write Strobe | B | 38 | E | 63 |
| DROPOUT | Dropout Error Status | C | 54 | E | 28 |
| STATE 3 | State Bit Decode 3 | C | 81 | E | 57 |
| STATE 4 | State Bit Decode 4 | C | 79 | D | 80 |
| MODE CHANGE | Operating Mode Change | C | 82 | D | 15 |
| POWER UP | Operating Power Applied +5 Volts | D | 68 | E | 58 |
| FN 6 | Program Function Decode 6 | D | 45 | E | 62 |
| FN 8 | Program Function Decode 8 | D | 47 | E | 64 |
| START REWIND | Set Run Flop $=$ RUN | D | 72 | E | 43 |

Table A-1. SPD-T Controller Signal Summary Cont'd.

| Nmemonic | Definition | WIRED |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | From |  | To |  |
|  |  | Board | Pin | Board | Pin |
| STOP STRB | Strobe Boot Flip Flop | D | 81 | E | 27 |
| BOOT ERROR | Status Enabler | C | 78 | E | 69 |
| $\overline{\text { EOT }}$ | Not End of Tape | D | 83 | E | 41 |
| POWER UP +IOR | Power Up Or Input Output Circuit Reset | D | 82 | E | 21 |
| READ CLOCK | Read Data Clock | A | 39 | Jack | 10 pin 59 |
| SPEED CONTROL | Tape Deck Control Signal (H=Slow, Low=Fast) | Jack | 10 pin | 65 D | 75 |
| SPEED | Tape Speed | A | 67 | B | 46 |
|  |  | B | 46 | E | 9 |
| RECVD DATA | Received Tape Data | A | 45 |  | 10 pin 61 |
| WRITE DATA | Operation In Write Mode | A | 13 | Jack | 10 pin 49 |
| WRITE DATA | Not Write Mode | A | 9 | Jack | 10 pin 51 |
| RUN* | Not Running | Jack | 10 pin | 67 B | 75 |
|  |  | B | 75 | D | 71 |
|  |  | D | 71 | E | 50 |
| MAN BOOT | Manual Boot Operation | Jack | 10 pin | 5 D | 32 |
| MAN REWIND | Operator Manual Rewind | Jack | 10 pin | 7 D | 34 |
| AUTO | Automatic Operator Mode Select | Jack | 10 pin | 9 D | 7 |
| MANUAL | Manual Operator <br> Mode Select | Jack | 10 pin | 11 D | 13 |
| $\overline{\text { START }}$ | Operator Select Not Start | Jack | 10 pin | 13 D | 42 |
| START | Start Operation | Jack | 10 pin | 15 D | 25 |
| TRACK B PROT | Protect Track B (Read Only) | Jack | 10 pin | 71 D | 65 |
| TRACK A PROT | Protect Track A (Read Only) | Jack | 10 pin | 73 D | 63 |
| SELECT A | Select Track A | Jack | 10 pin | 53 D | 22 |
| SELECT B | Select Track B | Jack | 10 pin | 55 D | 16 |
| SELECT WRITE | Select Write Mode | Jack | 10 pin | 57 D | 28 |
| DIRECTION | Select Direction of Tape Movement | Jack | 10 pin | 63 D | 77 |

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Table A-1. SPD-T Controller Signal Summary Cont'd.

| Nmemonic | Description | WIRED |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | From |  | To |  |
|  |  | Board | Pin | Board | Pin |
| TA SENSOR | Tape Address Sensor | Jack | 10 pin | 77 E | 37 |
| CASSETTE IN | Cassette In Place Micro Switch Signal | Jack | 10 pin | 75 E | 33 |
| OP INT REQ LAMP | Operator Visual Signal Lamp for Intervention Required | Jack | 10 pin | 17 E | 16 |
| BOOT LAMP | Indicator of Boot Operation | Jack | 10 pin | 19 E | 14 |
| MOTION LAMP | Tape Motion Indicator | Jack | 10 pin | 21 E | 26 |
| POWER ON LAMP | Indicate Presence of +5 V | Jack | 10 pin | 23 E | 55 |
| EOT/BOT LAMP | Indicator of Tape Begin or End of Tape | Jack | 10 pin | 25 E | 4 |
| TAC LAMP | Photo Sensor Lamp For Address Change |  | 10 pin | 27 E | 59 |
| $+5 \mathrm{~V}-\mathrm{B}$ | Cassette +5 Volt Power | Jack | 10 pi | 1 Jac | 10 p |
| GROUND | Ground Return To Tape D | ck Jack | 10 pin | 85 Jack | 10 pin |
| $+5 \mathrm{~V}-\mathrm{A}$ | TPU +5 Volt Power | B | 82 | C | 51 |
|  |  | D |  | E | 77 |
|  |  | C | 51 | D | 41 |
| GROUND | Return to TPU Ground | Jack | 10 pin | 81 Jack | 10 pin |

Table A-2. Power And Inter-Electronics Cable Wiring

| WIRED |  |  |  |
| :---: | :---: | :---: | :---: |
| Signal | Description | From | To |
| POWER ON LAMP | Operator Indicator | Lamp 4 cathode | Plug 10 pin 23 |
| $+5 \mathrm{~V}$ | +5Volts | Lamp 2, 3 and 4 Anode | Terminal block 2 lug 3 |
| MOTION LAMP | Operator Indicator | Lamp 3 Cathode | Plug 10 pin 21 |
| OPER INT LMP | Operator Intervention Lamp | Lamp 2 Cathode | Plug 10 pin 17 |
| MANUAL | Operator Switch | Switch 3 | Plug 10 pin 11 |
| GND | Ground | Switch 3 Common | Term Block 2 lug 6 |
| AUTO | Operator Selected Operating Mode Switch | Switch 3 | Plug 10 pin 9 |
| +14 VOLTS | Tape Deck +14 V | Jack 7 pin 20 | Plug 10 pin 29 |
| TAC | Tape Address Change | Jack 7 pin 21 | Plug 10 pin 27 |
| EOT/BOT | End/Beginning of Tape | Jack 7 pin 22 | Plug 10 pin 25 |
| AC IN BLK | AC Input Black Lead | AC Input (Black) | Rear Panel Interlock Switch, Normal Open |
|  |  | Interlock Switch Common | Fuse 1 |
|  |  | Fuse 1 <br> Switch 2 Common Contact | Switch 2, Normal Open Term Block 1 lug 7 |
| AC NET WHT | AC Input Neutral (White) | White Lead Sw 2 Common | AC Switch 2 (ON/OFF) Term Block 1 lug 12 |
| AC GND GRN | AC Input Ground (Green) | AC Ground | Ground Lug |
| WRITE DATA | Command to Tape Deck | Plug 2 pin 7 | Plug 10 pin 49 |
| $\overline{\text { WRITE DATA }}$ | Complement of Write Data | Plug 2 pin 1 | Plug 10 pin 51 |
| SELECT A | Track A Selected | Plug 2 pin 2 | Plug 10 pin 53 |
| SELECT B | Track B Selected | Plug 2 pin 6 | Plug 10 pin 55 |

Table A-2. Power And Inter-Electronics Cable Wiring Cont'd.

| Signal | WIRED |  |  |
| :---: | :---: | :---: | :---: |
|  | Description | From | To |
| SELECT WRITE | Write Mode Selected | Plug 2 pin 9 | Plug 10 pin 57 |
| READ CLOCK | Read Data Strobe | Plug 1 pin 10 | Plug 10 pin 59 |
| RECVD DATA | Received Data | Plug 1 pin 7 | Plug 10 pin 61 |
| DIRECTION | Direction of Tape Motion | Plug 6 pin 13 | Plug 10 pin 63 |
| SPEED CONTROL | Fast or Slow <br> Speed Control | Plug 6 pin 10 | Plug 10 pin 65 |
| RUN* | Results of Logical Tests For Run or Not Run | Plug 6 pin 14 | Plug 10 pin 67 |
| MOTION | Signal For Tape In Motion Lights Operation Lamp | Plug 6 pin 12 | Plug 10 pin 69 |
| TRACK B PROT | Micro Switch Sense for Presence of Protect Tape on Cassette Track B | Plug 6 pin 6 | Plug 10 pin 71 |
| TRACK A PROT | As Above For Track A | Plug 6 pin 5 | Plug 10 pin 73 |
| CASSETTE IN | Verifying Signal <br> for Cassette <br> Presence | Plug 6 pin 4 | Plug 10 pin 75 |
| TAC SENSOR | Chopper Vain <br> Signal for Track <br> Address Change, <br> Twisted With <br> Ground Lead | Plug 6 pin 7 <br> (Gnd) 6 pin 3 | Plug 10 pin 77 <br> (Gnd) 10 pin 81 |
| $\overline{\text { EOT/BOT SENS }}$ | Photo Electric Pick Up Through Clear Beginning or End of Tape Leade Twist With Ground | Plug 6 pin 8 <br> (Gnd) 6 pin 3 | Plug 10 pin 79 <br> (Gnd) 10 pin 83 |
| $+5 \mathrm{~V}$ | +5 Volt dc Power | Term block Term block 2 Term block 2 | 9 Term block 2 lug 3 <br> 4 Plug 10 pin 1 <br> Plug 1 pin 8 |

Table A-2. Power And Inter-Electronics Cable Wiring Cont'd.


Table A-3. Input/Output Cable, SPD-T

| Signal | From Electronics |  | To I/O |  | I/O Cable (External) |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Board | Pin | Jack | Pin | Plug | Pin |
| INB 07 | C | 27 | J11 | 18 | Pl1 | 18 |
|  |  |  | J12 | 18 |  |  |
| TYP 00 | B | 20 | J11 | 19 | Pll | 19 |
|  |  |  | J12 | 19 |  |  |
| FUNC 00 | D | 52 | J11 | 20 | P11 | 20 |
|  |  |  | J12 | 20 |  |  |
| TYP 01 | B | 28 | J11 | 21 | P11 | 21 |
|  |  |  | J12 | 21 |  |  |
| FUNC 01 | D | 54 | J11 | 22 | Pl1 | 22 |
|  |  |  | J12 | 22 |  |  |
| FUNC 02 | D | 56 | J11 | 24 | Pl1 | 24 |
|  |  |  | J12 | 24 |  |  |
| RESET | D | 39 | J11 | 25 | Pl1 | 25 |
|  |  |  | J12 | 25 |  |  |
| FUNC 03 | D | 58 | J11 | 26 | Pl1 | 26 |
|  |  |  | J12 | 26 |  |  |
| ACK N | B | 84 | J11 | 27 | P11 | 27 |
|  |  |  | J12 | 27 |  |  |
| ADD XX C | B | 8 | J11 | 28 | P11 | 28 |
| ADD XX O | 11 (jack) | 43 | J12 | 28 |  |  |
| TPU BOOT | E | 79 | J11 | 29 | Pll | 29 |
|  |  |  | J12 | 29 |  |  |
| INT XX C | B | 81 | J11 | 30 | Pl1 | 30 |
| INT XX O | 11 (jack) | 44 | J12 | 30 |  |  |
| SELECT IN | B | 77 | J11 | 31 | Pl1 | 31 |
| SELECT OUT | B | 79 | J12 | 31 |  |  |
| CPT 13 | B | 13 | J11 | 33 | Pl1 | 33 |
|  |  |  | J12 | 33 |  |  |
| CPT 02 | B | 26 | J11 | 34 | Pl1 | 34 |
|  |  |  | J12 | 34 |  |  |
| CPT 18 | B | 16 | J11 | 35 | Pl1 | 35 |
|  |  |  | J12 | 35 |  |  |

Table A-3. Input/Output Cable, SPD-T

| Signal | From Electronics |  | To I/O |  | I/ O Cable (External) |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Board | Pin | Jack | Pin | Plug | Pin |
| $+5 \mathrm{~V}$ | E | 77 | J11 | 1 | P11 | 1 |
|  | B | 82 | J12 | 1 |  |  |
| +5V Return (Ground) | C | 60 | J11 | 2 | P11 | 2 |
| OTB 00 | C | 43 | J11 | 3 | Pl1 | 3 |
|  |  |  | J12 | 3 |  |  |
| INB 00 | C | 55 | J11 | 4 | Pl1 | 4 |
|  |  |  | J12 | 4 |  |  |
| OTB 01 | C | 45 | J11 | 5 | Pl1 | 5 |
|  |  |  | J12 | 5 |  |  |
| INB 01 | C | 39 | J11 | 6 | Pl1 | 6 |
|  |  |  | J12 | 6 |  |  |
| OTB 02 | C | 61 | J11 | 7 | Pl1 | 7 |
|  |  |  | J12 | 7 |  |  |
| INB 02 | C | 41 | J11 | 8 | Pl 1 | 8 |
|  |  |  | J12 | 8 |  |  |
| OTB 03 | C | 59 | J11 | 9 | Pll | 9 |
|  |  |  | J12 | 9 |  |  |
| INB 03 | C | 49 | J1I | 10 | P11 | 10 |
|  |  |  | J12 | 10 |  |  |
| OTB 04 | C | 19 | J11 | 11 | Pl1 | 11 |
|  |  |  | J12 | 11 |  |  |
| INB 04 | C | 31 | J11 | 12 | P11 | 12 |
|  |  |  | J12 | 12 |  |  |
| OTB 05 | C | 21 | J11 | 13 | P11 | 13 |
|  |  |  | $\mathrm{J} 12$ | 13 |  |  |
| INB 05 | C | 7 | J11 | 14 | P11 | 14 |
|  |  |  | J12 | 14 |  |  |
| OTB 06 | C | 33 | J11 | 15 | Pl1 | 15 |
|  |  |  | J12 | 15 |  |  |
| INB 06 | C | 9 | J11 | 16 | Pl1 | 16 |
|  |  |  | J12 | 16 |  |  |
| OTB 07 | C | 37 | J11 | 17 | Pl1 | 17 |
|  |  |  | J12 | 17 |  |  |

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Table A-3. Input/Output Cable, SPD-T

| Signal | From Electronics |  | To I/O |  | I/O Cable (External) |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Board | Pin | Jack | Pin | Plug | Pin |
| CPT 09 | B | 73 | J11 | 36 | P11 | 36 |
|  |  |  | J12 | 36 |  |  |
| TURT 4 | B | 4 | J11 | 37 | P11 | 37 |
|  |  |  | J12 | 37 |  |  |
| +14V | 10 (jack) | 29 | J11 | 38 | P11 | 38 |
| $+14 \mathrm{~V}$ |  |  | J12 | 38 |  |  |
| $-14 \mathrm{~V}$ | 11 (jack) | 39 | J12 | 39 |  |  |
|  |  |  |  |  | J11 Pin 40 and 41 Grounded |  |

# FIELD ENGINEERING <br> TECHNICAL MANUAL 

$$
\text { SPD } 10 / 20
$$

## PERIPHERALS

## VOLUME V SPD-P15 Printer

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## FOREWORD

This maintenance volume provides a basic description of and maintenance procedures for the SPD-P15 Printer. Field maintenance and repair are accomplished by on-site one-for-one replacement of faulty modules. Module repair is performed off-site at the Repair Facility. This maintenance volume consists of three chapters. Chapter 1 consists of a general description, reference documents, specifications, and functional and physical characteristics. Chapter 2 contains a description of the printer controls and indicators; and procedures for paper, feed pin, and ribbon removal and replacement. Chapter 3 consists of maintenance procedures for the SPD-P15 Printer; including required tools and test equipment; preventive and corrective maintenance procedures; fault isolation and troubleshooting; checks and adjustments and a description of the printer test program.


Figure l-1 SPD-P15 Printer, Electronics Box, and Controller

## CHAPTER 1 INTRODUC TION

### 1.1 BASIC DESCRIPTION

The SPD-P15 is a small, lightweight printer that receives and prints data derived from the SPD 10/20 Display Terminal, via an asynchronous printer controller, to provide a hard copy output. The SPD-P15 Printer consists of the Printer mechanism installed in a Case (table top configuration). The printer controller and an electronics box are related components that are required and supplied with the printer (see Figure 1-1).

The printer accepts single and multiple sprocket feed, or ordinary paper. It can accept an original and two carbons or up to five copies can be produced, depending on paper thickness. Printing action is typographic and a standard (reversible) typewriter type ribbon is used. Printing speeds are variable up to 15 characters per second (maximum) depending on the transmitting source. The SPD-P15 prints all 64 characters of the ASCII dense subset; the type face used is Gothic.

The printer controller must be plugged into the slot defined by the Product Summary. The power supply in the Electronics Box contains a tapped transformer to allow operation at 105 VRMS $+10 \%,-20 \%$ to 125 VRMS $+10 \%,-20 \%$, at 5 V increments, or $210 \mathrm{VRMS}+10 \%,-20 \%$ to 250 VRMS $+10 \%,-20 \%$, at 10 V increments, by selecting the appropriate taps.


Figure 1-2 SPD-Pl5 Basic Block Diagram

Printer interfacing is shown in Figure 1-2; a cable of up to 10 feet in length is used to connect the printer to the electronics box and a cable of up to 20 feet in length is used to connect the electronics box to the SPD 10/20 Display Terminal. Additional interfacing information is contained in Drawing 014-10-08-002.

### 1.2 REFERENCE DOCUMENTS

Reference documents related to SPD-P15 Printer operation and maintenance are listed in Table 1-1.

| Table 1-1 <br> Reference Documents |  |  |
| :---: | :---: | :--- |
| Focument Number | Title | Publisher |
| FS002* | SPD 10/20 Field Engi - <br> neering Technical <br> Manual <br> SPD 10/20 Field Engi - <br> neering Technical <br> Manual Logic Diagrams | INCOTERM |
| P/N41859** | Installation and Main- <br> tenance of Model 123P <br> Printer | Mite Corp. |
| P/N42171** | Illustrated Parts List <br> For The Model 123P <br> Printer | Mite Corp. |

Related drawings for the Printer, Printer Controller, and Electronics Box are listed in Table 3-5.

### 1.3 DIAGNOSTIC PROGRAM

A diagnostic program designated the "Multi-Printer Diagnostic" is supplied with the Printer for initial checkout, maintenance, and troubleshooting purposes. A description of Multi-Printer Diagnostic Program usage is provided in Paragraph 3.7.

### 1.4 SPECIFICATIONS

Following are the operating and physical specifications for the SPD-P15 Printer:
1.4.1 Environmental Requirements

Operating Temperature Range
Operating Humidity Range

### 1.4.2 Operating Requirements

Power Requirements

Inking Medium

Maximum Paper Thickness
1.4.3 Operating Characteristics

Electronics Box Power Supply Outputs
Printing Speed
Print Code
$10^{\circ}$ to $32^{\circ} \mathrm{C}$
to $95 \%$ (relative)

105, 110, 115, 120, or 125 VRMS $+10 \%,-20 \%$, or $210,220,230$, 240 , or 250 VRMS $+10 \%,-20 \%$ 215 VA total

Standard 0.5 inch typewriter type ribbon
Multicopy*-0.014in., maximum Single copy-0.005in., maximum

| Print Line Width | 80 characters (7.5 in.) |
| :---: | :---: |
| Character Spacing | 3/32 in. nominal (approximately <br> 10.8 character spaces per inch) |
| Line Spacing | 6 lines per inch. |
| Character Size | Height - 0. 107 inch <br> Width - 0.062 inch |
| Line Feed | Single |
| Paper-Sprocket Feed | Width - 8.5 inch, single or multicopy, fully chadded holes along each edge. |
| Paper - Prick Pin Feed | Width - 8.5 inch, single or multicopy. No chadded holes. |
| Paper - Friction Feed | Width - 5.0 to 8.5 inch, single sheets |
| Life of Mechanism** | 1500 hours at 10 cps between major overhauls. |
| Mechanism Reliability | 500 hours at 100 cps . minimum |

### 1.4.4 Physical Specifications

The following physical specifications are for the complete assembled printer and printer case.

| Height: | 6.5 inches |
| :--- | ---: |
| Width: | 18.0 inches |
| Depth: | 18.0 inches |
| Total Weight: | 31.5 pounds |

The following physical specifications are for the printer electronics box.

| Height: | 5.5 inches |
| :--- | ---: |
| Width: | 11.0 inches |
| Depth: | 10.0 inches |
| Total Weight: | 14.5 pounds |

### 1.5 FUNCTIONAL DESCRIPTION

The SPD-Pl 5 Printer consists of the Printer, Printer case, Electronics Box, and Printer Controller. The Printer Controller contains communications and control circuitry required to interface the SPD-P15 Printer with the SPD $10 / 20$ Display Terminal. The Electronics Box contains the power supply, and solenoid driver circuitry.

### 1.5.1 SPD-P15 Printer

The printer circuitry is subdivided into the print cylinder printer system, and control system. The print cylinder printing system positions the print cylinder and print hammer, and the control system performs all the related control functions necessary during printer operation; i.e., carriage return, line feed, character advance, line feed, ribbon feed, and print command. For more detailed infor mation, refer to Section 4 of the Mite Printer Installation and Maintenance Manual.

### 1.5.2 Electronics Box

The Electronics Box contains the power supply and solenoid driver circuitry. The power supply provides the +5 Vdc and +115 Vdc outputs required for the printer and the solenoid driver circuitry. The solenoid driver circuitry drives the 115 Vdc solenoids contained in the printer, controlled by pulses (using normal logic levels) received from the SPD 10/20 via the Printer Controller.

### 1.5.3 Printer Controller

The Printer Controller must be plugged into the slot defined by the Product Summary. The Printer Controller provides the necessary interfacing and communications control required between the SPD 10/20 Display Terminal, and the Electronics Box and SPD-Pl5 Printer (see Figures 1-1 and 1-3).


Figure 1-3 SPD-Pl5 Printer Controller

CHAPTER 2
OPERA TING INSTRUCTIONS

## 2. 1 GENERAL

This chapter contains the necessary information required for SPD-P15 Printer operation such as; controls and indicators, special considerations, etc.

## 2. 2 CONTROLS AND INDICATORS

The SPD-Pl5 Printer has three switches (see Figure 2-1), all of which are located on the printer case. The ac power ON/OFF switch serves as both a switch and an indicator. The switches and their functions are as follows:
\(\left.\left.$$
\begin{array}{lll}\text { Power ON/OFF Switch } & \text { Left-Front } & \begin{array}{l}\text { Switches ac power to } \\
\text { and Indicator }\end{array}
$$ <br>
Printer and Electronics <br>

Box. When power is on,\end{array}\right\} $$
\begin{array}{l}\text { switch will be lit. }\end{array}
$$\right\}\)| Depressing this switch |
| :--- |
| initiates a manual car - |
| riage return cycle. |

## 2. 3 PAPER INSTALLATION

The printer is capable of three types of paper feed: sprocket, prick pin and friction feed. Sprocket feed is used with 8.5 inches wide paper


Figure 2-1 SPD-P15 Controls and Indicators
with chadded (punched) holes along both edges. Prick pin feed is used with 8.5 inches wide paper without punched holes along the edges. Friction feed is used with single sheets, narrower than 8.5 inches. For examples of the sprocket and prick pin feed pins, see Figure 2-2.

## NOTE

> Before installing paper, ensure that the correct feed pins are installed in the platen. There should be four feed pins at each end of the platen. If the wrong pins are installed, refer to Steps 1 through 5 of Paragraph 2.5 , and install the correct pins before installing the paper.

To make the sprocket teeth engage the holes more easily when inserting the paper, the platen should first be positioned as follows:

Step
Procedure
1 Turn the paper roller shaft so that the flat side of the shaft is horizontal. Then turn the shaft two clicks in the counter clockwise direction (as viewed from the left side).

2 Pull the paper (from the rear) up over the top of the printer, with the side to be typed on facing down.

NOTE
If sprocket feed or pin prick feed type paper is used, the pressure rollers must be released by moving the release lever to the rear of the printer before inserting the paper. If friction feed paper is used, and the sprocket or pin prick teeth are installed in the platen, they must be engaged by moving the release level fully forward to the front of the printer. When using sprocket feed or pin prick feed paper, perform Steps 3 and 5. When using friction feed paper, refer to Steps 4 and 5. To remove the teeth, refer to Paragraph 2.5.

Step

## Procedure

Carefully guide the sprocket (or pin prick) feed paper into the paper receiving throat, with the side to be printed on facing down, until it bottoms. Slowly turn the paper advance knob until the teeth correctly engage the holes in the paper. In the case of pin prick feed, ensure that the paper is straight and the prick pins penetrate the paper easily and without resistance.

## 2. 4 FEED PIN REMOVAL AND REPLACEMENT

Normally, either the sprocket pins or prick pins will be installed in the printer prior to shipment. The eight alternate feed pins and installation tool are contained in the accessory kit that is shipped with the printer. To remove one type of pin and replace them with the alternate type, refer to Figure 2.1, and perform the following procedure.

Step
1
2 Rotate the paper roller shaft until the pins are accessible through the openings in the paper pan. There are four pins at each end.
3
Procedure
Open the printer cover. pins at each
To remove the pins, unscrew each counterclockwise.

NOTE
Care should be taken to avoid dropping the pins into the printer mechanism.


Sprocket Feed


Figure 2-1 Paper Feed Pins


1. Ribbon Spool - Right Hand
2. Ribbon Spool Spindle
3. Reversing Fork
4. Ribbon Gulde - Right Rear
5. Ribbon Guide - Right Front
6. Ribbon Hammer Guides
7. Print Cylinder
8. Ribbon Guide - Left Front
9. Ribbon Guide - Left Rear
10. Ribbon Guide
11. Reversing Fork
12. Reversing Eyelet
13. Ribbon Spool - Left Hand
14. Ribbon Spool Sprindle

Figure 2-2 Ribbon Threading Diagram

Step
4 Install the alternate feed pins.
5 Close the printer cover.

### 2.5 RIBBON REPLACEMENT

The following procedure is provided to facilitate removal and replacement of the ribbon.

Step
Procedure
1 Open the printer cover.
2 Wind the ribbon onto the fullest spool until the small reversing eyelet is exposed at the end of the ribbon (see Figure 2-3).
3 Remove the spools and ribbon from the ribbon guides. Retain the empty spools.

4 Hook the end of the new ribbon to the smpty spool. Wind the ribbon on the spool and continue to wind until the reversing eyelet has been wound onto the spool. The spool is not installed at this time.

6 Grasp the empty spool and thread the ribbon through the reversing fork (next to the full spool) and hook it onto the ribbon guide. Hook the ribbon to the ribbon guide on the right-front and in front of the print cylinder, ensuring that it passes between the hammer face and the print cylinder.

7 Hook the ribbon onto the ribbon guide on the left-front, then the ribbon guide on the left-rear corner. Pull it in back of the large ribbon guide in the rear, thread it through the adjacent reversing fork, and place the spool onto the spindle. The reversing eyelet should be exposed at this time.

Step

## CAUTION

The exposed reversing eyelet must be on the spool side of the reversing fork, between the spool and reversing fork. If the reversing eyelet is on the outside of the fork, the ribbon will not automatically reverse when the end of the ribbon is reached and damage could occur to the mechanism.

Manually actuate the ribbon mechanism, including actuation of the reversing forks several times, to ensure the ribbon advance system is working correctly.

$$
2-7
$$

## CHAPTER 3

MAINTENANCE

### 3.1 INTRODUCTION

This chapter contains troubleshooting, preventive maintenance, and corrective maintenance instructions and procedures for the SPD-P15 Printer Controller and Printer Electronics Box. General troubleshooting and preventive maintenance instructions are also included for the SPD-P15 Printer.

Troubleshooting and corrective maintenance procedures are directed to the site-level. The objective of site level maintenance is to repair the equipment with minimum down-time by locating the faulty electronics board, or assembly within the particular piece of equipment, and removing and replacing the non-working board or assembly with a working board or assembly.

### 3.2 TEST EQUIPMENT

The tools and test equipment (or equivalent), lubricants, and cleaning materials that are required for maintenance of the SPD-P15 Printer are listed in Tables 3-1, and 3-2. Tools required for maintenance of the Mite Printer Controller, and Printer Electronics Box are included in the Field Service Tool Kit.

Table 3-1
Test Equipment and Tools Required

| Equipment | Manufacturer | Designation | Required Use |
| :--- | :--- | :--- | :--- |
| Multimeter | Simpson | 160 | To perform voltage <br> and solenoid resis - <br> tance measurements. |
| Sprocket Tooth and <br> Prick Tooth Wrench* | Mite Corp. | 41615 | To remove and install <br> sprocket and prick <br> teeth. |
| Multi-Printer <br> Diagnostic Program | INCOTERM | E-7111-1 | To test the SPD-P15 <br> Printer. |
| *NOTE: Supplied with SPD-P15 Printer. |  |  |  |

In addition to the required test equipment and tools listed in Table 3-1, the following lubricants and cleaning materials are required and/or recommended.

Table 3-2
Lubricants and Cleaning Materials
Grease, High Temperature* Non-flammable Chlorinated Solvent
(e. g. , triclorethylene) $* *$

Oil, High Temperature
(Polyester Base)*
Merix Anti-Static No. 79\%*
Typewriter Brush*
*NOTE: Required for preventive maintenance.
**NOTE: Recommended but not required.

### 3.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically to prevent failures caused by minor damage or progressive deterioration. A preventive maintenance $\log$ book should be established, or if one already exists, a section should be added to make the necessary entries according to a regular preventive maintenance schedule. This data, compiled over an extended period of time, is useful in anticipating possible component failures on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks, lubrication, and cleaning. All maintenance schedules should be established according to conditions at the particular site which are particularly influenced by environmental conditions. Mechanical checks should be performed as often as required. All other preventive maintenance should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 250 operating hours or every six months, whichever occurs first. However, lubrication may be required on a more frequent basis depending on the operating environment.

The following are tasks which should be performed as part of the preventive maintenance procedure.
a. Clean both the exterior and interior of the Printer Electronics Box and printer case and copy windown, using a vacuum cleaner and/or clean cloth moistened in a mild detergent or non-flammable chlorinated solvent (e.g., triclorethylene).
b. Clean all air vents using a vacuum cleaner or small brush and moist cloth.
c. Clean the print cylinder and shaft with a dry typewriter brush.

## WARNING

Never use any cleaning solutions or lubricants on the print cylinder and shaft, hammer and shaft, or solenoid plungers. The components must run dry.
d. If the copy window becomes electrostatic, it may be treated with Merix Anti-Static No. 79, diluted 1 to 1 with water.
e. Inspect all wiring, cables, and harnesses for cuts, breaks, fraying, deterioration, kinks, strains, and mechanical security. Replace or repair any defects found.
f. Inspect all lamps, switches, knobs, connectors, and fuses for proper operation and/or mechanical security. Repair, replace or tighten as required.
g. Inspect all modules to ensure that all are firmly seated in their sockets. Remove and clean any modules that may have collected excess dirt or dust.
h. Inspect the power supply for leaky capacitors, overheated resis tors, relay operation, etc.; replace or repair, if any defective items are found.
i. Check the voltage outputs of all voltage regulators and make any necessary adjustments of the regulators in accordance with Paragraph 3.6.1, to bring the voltages into specification. If the voltage cannot be adjusted to meet the specification, corrective maintenance must be performed.
j. Load and run the Multi-Printer Diagnostic Test, described in Paragraph 3.7, and allow to run for one hour. No errors should occur.

## 3. 4 CORRECTIVE MAINTENANCE

The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Personnel responsible for maintenance should be familiar with the system concept, the drawings listed in Table 3-5, and the location of mechanical and electrical components.

The first step in correcting a reported malfunction is to isolate the problem, using the flow chart in Figure 3-1, and determine whether the problem is in the hardware, software, or both. If the malfunction is determined to be of a hardware type, it should be further isolated to the unit or board level. Once the problem has been isolated to a specific PC board,subassembly, etc., it should be replaced with a PC board, subassembly, or unit of known quality on a one -for -one basis. When a defective board or subassembly is replaced with a spare, tag the defective board or unit, and note on the tag the location from which it was taken and the nature of the failure.

Corrective maintenance is not complete until all activities are recorded in the log book. Record all data, indicating the symptoms displayed by the fault, the method of fault detection, the board or unit at fault, and any comments that would be helpful in the future. The log should be maintained on a daily basis, recording all preventive and corrective maintenance results.

### 3.5 SPD-Pl5 FAULT ISOLATION AND TROUBLESHOOTING

The flow chart contained in Figure 3-1 is supplied to be used for fault isolation and troubleshooting, in conjunction with the accompanying procedure contained in this paragraph. The flow chart must be followed in the exact sequential order in which it appears. Do not skip or ignore any of the steps; all steps must be accomplished in the order that they appear.

SPD-P15 Printer "checks and adjustments" are contained under Paragraphs 3.6 through 3.6 .2 , and will be referenced in the flow chart as required. A description and procedures for the SPD-P15 Printer Test Program are provided in Paragraphs 3.7 through 3.7.6, and will be referenced as required in the flow chart.


Figure 3-1 Fault Isolation Flow Chart (Sheet 1)


Figure 3-1 Fault Isolation Flow Chart (Sheet 2)

### 3.6 CHECKS AND ADJUSTMENTS

The following procedures are provided for checkout and adjustment of the SPD-P15 Printer, printer controller, decoding logic and solenoid drivers, and the printer power supply.

### 3.6.1 Power Supply Check and Adjustments

This procedure is performed to verify that the correct dc operating voltages are supplied by the printer power supply contained in the Printer Electronics Box. To check the power supply output voltages, perform the following steps:

| Step | Procedure |
| :---: | :---: |
| 1 | Plug a connector, with pins 35 and 37 jumpered, into into electronics box connector Jl. |
|  | CAUTION |
|  | Use care when performing this step. There are high voltages on this connector. |
| 2 | Refer to Table 1 on Drawing 014-13-001 and ensure that the transformer strapping is connected correctly. |
| 3 | Ensure that connectors J1 and J2 on the electronics box are disconnected, and power -up the electronics box (power supply). |
| 4 | Monitor the +5 Vdc supply at the ( + ) side of C5. Adjust at $R 60$ as required to obtain the required +5 Vdc output. |
| 5 | Monitor the +115 Vdc supply at the ( + ) side of C6. Adjust at $R 59$ as required to obtain the required +115 Vdc output. |
| 6 | Power down the unit and remove the jumper connected between pins 35 and 37 of Jl. |

### 3.6.2 Printer Controller Static Check

This procedure is performed to verify that the potentiometers that are used to adjust the various delays in the SPD-P15 Printer Controller are
set for the correct resistance values.
Step
1 Refer to Drawings 001-22-01-001, Sheet 2, and 001-22-02-701.

2 Connect an ohmmeter across the arm and one end of each of the following potentiometers and set each for the following resistance values:

| Potentiometer |  | Value |
| :---: | :---: | :---: |
| R11 |  | 5 K |
| R16 |  | 5 K |
| R17 |  | 5 K |
| R12 |  | 10 K |
| R13 |  | 10 K |
| R14 |  | 10 K |
| R15 |  | 10 K |

### 3.6.3 Printer Adjustments

Procedures for adjustments to the SPD-P15 Printer are provided in Paragraph 5-6 of the Mite Printer Installation and Maintenance Manual (refer to Table 1-1) one of which is shipped with each printer. The procedures contained under 5-6; a., and b., are not to be performed. The remaining adjustment procedures in 5-6, c., through 5-6, 1., may be performed.

## 3. 7 PRINTER TEST PROGRAM

The test program that is used to test the SPD-P15 Printer is the MultiPrinter Diagnostic, Program No. E-71ll-1. This test program is designed to test all of the printer electro-mechanical operating functions, the data interfacing with the SPD $10 / 20$ (via the Mite Printer Controller), and the printer printing quality. The various functions may be executed in any desired sequence. The various functions and conditions that may be tested using this test program are listed below:
a. Data Interface Functions
b. Printing Quality
c. Error Conditions
d. Keyboard Lights (on SPD 10/20)
e. Operating Instructions

### 3.7.1 Program Description

The various program functions may be executed and tested individually in any desired sequence.

Operating Functions - Operating functions that are tested by the test program are: carriage return, line feed, combined carriage return/ line feed, and reset.

Data Interface Functions - Two tests contained in Paragraphs 3.7.6, and 3. 7. 7 are provided to test the data interface (printer controller and electronics box) between the SPD 10/20 and the SPD-P15 Printer.

The first test permits all characters that can be input from the keyboard to be printed in any desired print position. This test prints static information (i.e., information already formatted on the screen) which is initiated by pressing the PRINT SCREEN key. This function may be terminated by pressing the PROGRAM RESET or DISCONTINUE keys (see Figure 3-2).

The second test is a continuous -loop test that uses a "regressive" carriage return function and prints the dense subset (printable characters) of the ASCII character set. This test is initiated by pressing the PRINT ASCII key and the ASCII dense subset is printed continually. The first line will be a full line of characters and each successive line will be shorter by one character until only a single character is printed on the
last line. The printing cycle then resumes, beginning again with a full line and the cycle is repeated. This function may be terminated by pressing the PROGRAM RESET key.

Printing Quality - The quality of the printed information; i. e., uniformity of coloration (dark or light characters), accuracy of horizontal and vertical spacing, and reliability of the printer mechanism may be verified between functions and/or tests.

### 3.7.2 Considerations and Constraints

The following are considerations and/or constraints that should be remembered when using the Multi-Printer Test Program:
a. Since the "DOUBLE WIDTH" print key causes an adjustment of the number of characters inserted on the screen by the "line builder" routine, this key, when used, should be pressed before test data is entered from the keyboard.
b. The "REPEAT" and "DISCONTINUE" keys may be pressed either before printing begins, or during printing.
c. When a Time-Out condition occurs, the "PROGRAM RESET" key must be pressed to re-initialize the program.
d. Since the keyboard remains enabled during printing, most keys that are pressed are considered "data" keys and are entered on the screen. Thus, no function keys are recognized by the program with the exception of "PROGRAM RESET", "PRINTER RESET" (if valid), "LINE BUILDER", "REPEAT", "DISCONTINUE" and all cursor functions.

$* 1$


Figure 3-2 Keyboard Function Keys

INCOTERM STANDARD KEYBOARD


Figure 3-3 SPD 10/20 Standard Keyboard

### 3.7.3 Keyboard Indicators

The keyboard lights (shown in Figure 3-3) and their respective functions are listed in Table 3-3.

Table 3-3
Keyboard Indicators and Functions

| Indicator | Function |
| :---: | :---: |
| KEY ERROR | Lighted when a Type 4 error has been detected. Once lighted, any subsequent valid use of a key will cause the light to be turned off. |
| $\begin{aligned} & \text { TIME -OU T } \\ & \text { ERROR } \end{aligned}$ | Lighted when a Type 3 error exists. |
| REPEAT | Lighted when program is operating in continuous mode (i.e., after the "REPEAT" key has been depressed to place a function into continuous operating mode. Light is turned off when "DISCONTINUE" key is depressed. |
| PRINTER NOT READY | Lighted when Type 2 error exists. |
| CONTROLLER <br> NOT READY | Lighted when Type 1 error exists. |
| SELECT | Lighted after selection of a valid printer using "PRINTER SELECT" key. |

### 3.7.4 Error Conditions

The error conditions listed in Table 3-4 will be detected and brought to the attention of the operator via the keyboard lights (see Figure 3-3) and/or Sonalert.

Table 3-4
Error Conditions and Indications

| Type | Indication | Description |
| :---: | :---: | :---: |
| 1 | CONTR NOT PRESENT Indicator lights. | Printer controller not present in TPU. |
| 2 | PRINTER NOT READY Indicator lights. | Printer power off or in power up sequence, printer not connected correctly, printer not selected, etc. |
| 3 | TIME-OUT ERROR Indicator lights |  |
| 4 | KEY ERROR <br> Indicator lights | The following may cause the indicator to light: a non-exis tent printer is selected, an invalid controller address is typed in during a "Change Address" request, a function is initiated before a printer is selected (PRINTER SELECTED light is off), a function is initiated that is not available in the printer (i.e., "page eject" function for the SPD-P15 Printer). |

### 3.7.5 Operating Instructions

The following are the operating instructions required for the MultiPrinter Test Program (E-7111-1).

Step
1
2 Before using this program, ensure that all cabling between the printer and the TPU is complete, and power to the printer is on, press the LF switch to advance the paper.

When the program is completely loaded, operating infor mation will appear on the screen (see Figure 3-4). The data displayed on the screen is for information purposes only, and is not to be used as a procedure.

If alphanumeric characters do appear, this indicates a "faulty load". Reload the program. If a faulty load again occurs, refer to Paragraph 4. 5.

If the cursor does not appear in the upper left-hand corner of the screen, depress the "CURSOR TO HOME" key. Enter " $M$ ", then depress the "SELECT PRINTER" key. If a correct printer ID has been typed, the cursor will return to the HOME position. If it has not returned to HOME position, repeat this step.

The printer controller address default value used by the program is 5. If the actual controller address contained in the Product Summary is different (must be either $\emptyset$ or 2 through 7) it must be initiated by typing it at the HOME position of the screen, and pressing the "CHANGE ADDRESS" key. Acceptance of a correct address by the program will cause the cursor to return to the HOME position. If the address is not accepted, repeat this step.

Any function that can be executed by the printer selected may now be initiated. Pressing an invalid function key will cause the "KEY ERROR" indicator to be turned on, and/or (if present in the TPU being used) the SONALERT to be sounded. Press the DOUBLE WIDTH and PAGE EJECT keys, the KEY ERROR indicator should light or the SONALERT should sound.


Figure 3-4 Initial Operating Information

Step
Procedure

8
To cause any function to be repeated continually, first depress the "REPEAT" key, then the desired function key. To stop continuous mode execution, depress the "DISCONTINUE" key. Since the "PRINT SCREEN" function always prints the entire screen before determining whether a repetition is necessary, the "RESET PROGRAM" key may be used if a quick termination of this function is desired. This key is also used to terminate the "PRINT ASCII' function.

9 To assist in the generation of lines of characters on the screen, based on printed line length, a "Line-Builder" function has been incorporated into the program. To activate the "LINE BUILDER" function, depress the "LINE BUILDER" key. To generate, for example, a full line of $R^{\prime}$ s for the printer selected, merely press "R" key and hold it down. This enables the keyboard interrupt repeat function and $R^{\prime}$ s will begin to fill the screen. When this automatic fill action stops, a full (printer) line of $R^{\prime}$ s has been entered. Additional lines may be generated by releasing the $R$ key and pressing any other key (or the "R" key again, if additional lines of R's are desired). To revert to normal keyboard operation, use the "PROGRAM RESET" key.

### 3.7.6 Keyboard Input Test

This procedure is used to test the data interface (printer controller and electronics box) between the SPD 10/20 and the SPD-P15 Printer, and permits all characters that can be input from the keyboard to be printed.

Step

## Procedure

Press the CR and LF keys and type the following information on the screen followed by a CR and LF.

$$
\begin{array}{llllllllll}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & \emptyset
\end{array}
$$

2 Press the PRINT SCREEN key. The information on the screen should be printed by the printer (see Figure 3-5).

3 Press the CR and LF switches on the printer to ensure they are operable.

4 Press the CR and LF keys, then press the REPEAT key and PRINT SCREEN key. The printer should print the displayed information repeatedly with a carriage return and line feed after each line. Press the PROGRAM RESET key to terminate the function.

5 Press the ERASE SCREEN key to clear the screen.
6 Press the CR and LF keys and type the characters A through $Z$ on the screen and repeat steps 2,4 , and 5 .

7
Press the CR and LF keys and type the remaining lower case characters and shifted (upper case) characters. Press the CR and LF keys and repeat steps 2, 4, and 5.

### 3.7.7 Continuous Loop Test

This test procedure is used to test the data interface (printer controller and electronics box) between the SPD 10/20 and the SPD-P15 Printer. It is a continuous loop test that uses a "regressive" carriage return function (lines are progressively shorter) and prints the dense subset (printable characters) of the ASCII character set (see Figure 3-6).

Step
Procedure

1
Press the CR and LF keys.
2 To initiate the test, press the PRINT ASCII key.
3 Observe the information printed by the printer. The first line will be a full line of characters and each successive line will be shorter by one character until only

1234567890
1234567894
1234567899
1? 34567890
1234567894

ABCDEFGHI JKL MNOPORSTIVWXYZ AGCDEFGHI JKLMNOPIRS TIVVXYZ ABCDEFGHIJKL MNOPDRS TIVWXYZ ABCDEFGWI JKLMNOOORSTIVWXYZ ABCOEFGHIJKLMNOPORST!IVWXYZ ABCDEFGHI JKI MNOPDRS TIIVWXYZ




```
-&1*\;:[../日#क%R'()=+*<>?
-&10\::[0./n#$&%'()=+*<>?
-&1, \::[0./*;*%q!()=+*<>?
```

Figure 3-5 Keyboard Input Test Printout












Figure 3-6 Continuous Loop Test Printout
a single character is printed on the last line. The printing cycle then resumes, beginning with a full line and the cycle is repeated.

4 The test may be terminated by pressing the PROGRAM RESET key.

## 3. 8 SPD-P15 PRINTER

The drawings and logic diagrams that are supplied with the SPD-P15 Printer are listed in Table 3-5.

Table 3-5
SPD-P15 Printer Drawing Package

| Drawing Number | Title |
| :---: | :---: |
| SPD-P15 Drawing Package |  |
| 014-10-08-002 | SPD-P15 Cabling, Mite Printer |
| 001-22-01-001 | Mite Printer Controller |
| 001-22-02-701 | P. C. Board Assy., Mite Printer Controller |
| 014-13-01-001 | Mite Printer Power Supply |
| 014-13-02-701 | P. C. Board Assy., Mite Printer Power Supply |
| Mite Corp. Installation and Maintenance Manual |  |
| 9380 | Outline Drawing, Model 123 Printer |
| 41411 | Timing Diagram for Model 123 Printer |
| 41613 | Schematic Diagram, Model 123 Printer |
| 41860 | Electrical Connections, Model 123 Printer |












