iSBC 094
4K BYTE CMOS
RAM/BATTERY BACKUP BOARD
HARDWARE REFERENCE MANUAL

Manual Order Number: 9800449B

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Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

PREFACE

This manual provides general information, principles of operation, and service information for the iSBC 094 4K Byte CMOS RAM/Battery Backup Board. Additional information is available in the following document: *Intel MULTIBUS Interfacing*, Application Note AP-28.

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ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 094 is a member of a complete line of Intel iSBC 80 and iSBC 86 system expansion modules. The iSBC 094 provides 4K bytes or 2K words of static read/ write memory and includes power fail interface logic and an on-board rechargeable battery. The iSBC 094 performs as a slave module on the Multibus.

1-2. DESCRIPTION

The iSBC 094 (figure 1-1) is designed to be plugged into a standard iSBC 604/614 Modular Backplane and Cardcage to interface directly with an Intel iSBC 80 Single Board Computer or with an Intel Intellec Microcomputer Development System.

The iSBC 094 contains 4K bytes (2K words) of static random access memory (RAM) implemented with 32 Intel 5101 CMOS RAM chips. Jumpers are provided to allow the selection of a continuous 4K byte segment that begins on any 4K memory address boundry (0000H, 1000H, 2000H, etc.). 16-bit data may be stored in 2K segments in a similar fashion. An on-board rechargeable battery and battery charging circuit insures the integrity of the on-board RAM for at least 96 hours after system power (+5V) is removed. Thus, critical system parameters can be stored in the iSBC 094 memory during temporary primary power failures. Power fail interface logic is included that will generate a CPU interrupt when a power failure is detected by the system power supply. An orderly system shutdown procedure may than be executed to save critical system parameters for subsequent retrieval.

The battery charging circuit includes overcharge and short-circuit protection. Switches are provided for connecting and disconnecting the on-board battery during maintenance and storage and for enabling and disabling the power fail circuit.

All electrical connections are implemented via edge connectors P1 and P2. Connector P1 connects to the Multibus and accommodates all of the major power and signal lines including the address and data buses. The data lines terminate at a memory buffer composed of Intel 8226 Parallel Bidirectional Bus Drivers. Connector P2 accommodates the lines pertaining to the ac power fail feature.

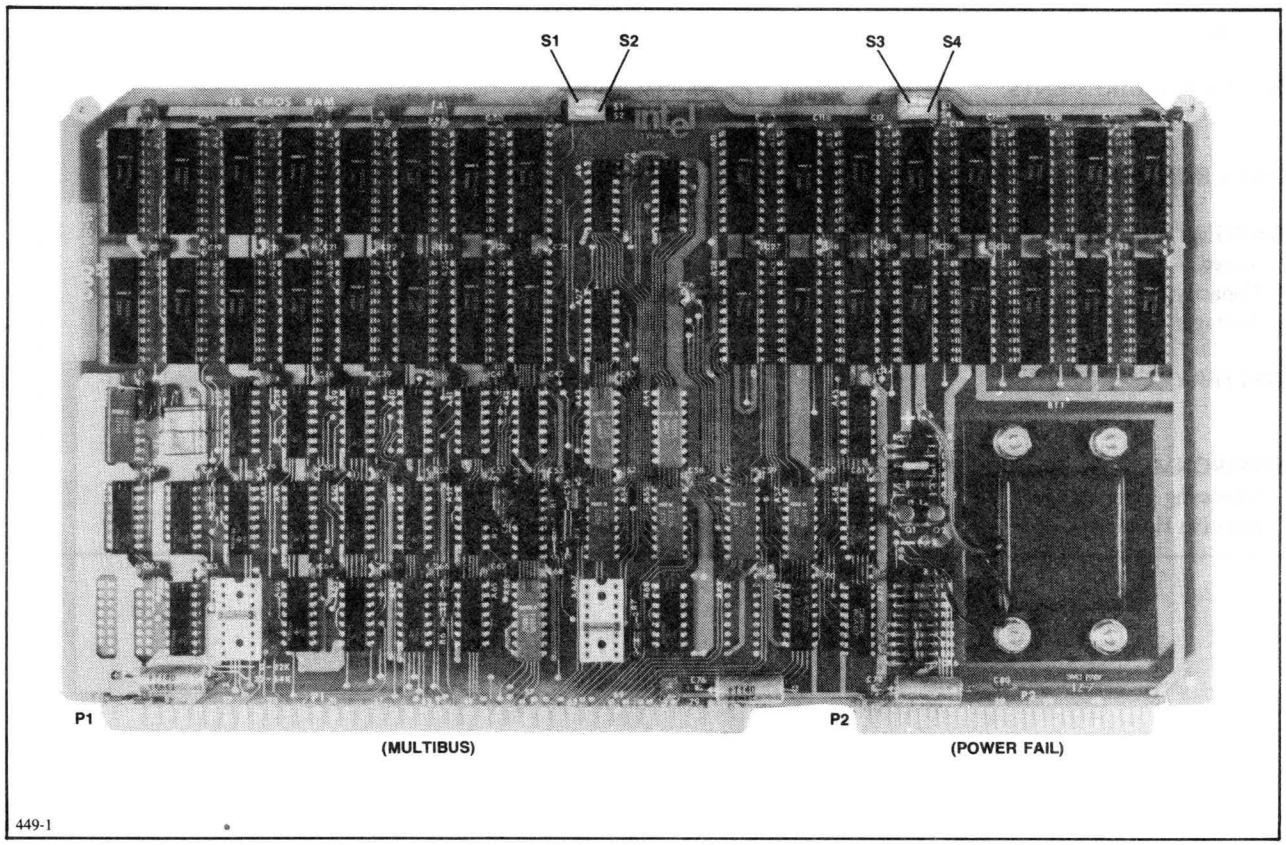


Figure 1-1. iSBC 094 4K Byte CMOS RAM/Battery Backup Board

1-3. DOCUMENTATION SUPPLIED

The following documentation is supplied with the iSBC 094 board:

a. Schematic Diagram, dwg. no. 01-0652-000
b. Assembly Diagram, dwg. no. 05-0652-000

1-4. SPECIFICATIONS

Specifications for the iSBC 094 are listed in table 1-1.

Table 1-1. Specifications

CAPACITY:	4096 bytes (2048 words).
BUS COMPATIBILITY	
Interface:	TTL compatible.
Connector:	86-pin, double-sided, PC edge connector with a 3.96-mm (0.156-inch) contact centers. (Refer to paragraph 2-7).
ADDRESS SELECTION:	4K 8-bit segment starting at any jumper selectable base address on a 4K byte boundary or 2K 16-bit segment.
MEMORY RESPONSE TIME	
Read Access:	750 nsec (maximum).
Read Cycle:	900 nsec (maximum).
PHYSICAL CHARACTERISTICS	
Width:	30.48 cm (12.00 inches).
Height:	17.15 cm (6.75 inches).
Thickness:	1.27 cm (0.50 inch).
Weight:	340.2 gm (12 ounces).
POWER REQUIREMENTS:	V_{CC} = +5V ±5%. I_{CC} = 0.80A typical; 1.7A maximum.
DATA RETENTION:	96 hours following removal of +5V bus power.
BATTERY CHARACTERISTICS	
Type:	Eveready #CH150 (or equivalent), nickel-cadmium, rechargeable.
Capacity:	150 mA hours.
Voltage:	3.6V nominal.
BATTERY CHARGE TIME:	14 hours for full charge (150 mA hours) (full overcharge and short-circuit protection).
ENVIRONMENTAL REQUIREMENTS	
Operating Temperature:	0° to 55°C (32° to 131°F)
Relative Humidity:	To 90%, without condensation.

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBC 0944 RAM Board. These instructions include unpacking and inspection; installation considerations such as power and cooling requirements, physical dimensions, and bus interface requirements; jumper configurations; power fail connections; board installation; and programming considerations.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel MCSD Technical Support Center (see paragraph 4-3) to obtain a Repair Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The iSBC 094 is designed for interface with an Intel iSBC 80/86 Single Board Computer based system or an Intel Intellec Microcomputer Development System. Important installation and interfacing criteria are presented in the following paragraphs.

2-4. POWER REQUIREMENT

The iSBC 094 requires +5V (+0.25V) at 1.7A maximum. For installation in an iSBC Single Board Computer based system, ensure that the system power supply has sufficient +5V current capacity to accommodate the additional requirement. For installation in an Intellec System, calculate the total +5V current requirement for the standard modules and all installed optional modules. Ensure that the additional 1.7A (maximum) current requirement will not exceed the capacity of the +5V supply.

2-5. COOLING REQUIREMENT

The iSBC 094 dissipates 121 gram-calories/minute (0.49 Btu/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The System 80/86 enclosures and the Intellec System include fans to provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

Physical dimensions of the iSBC 094 are as follows:

a. Width: 30.48 cm (12.00 inches)
b. Height: 17.15 cm (6.75 inches)
c. Thickness: 1.27 cm (0.50 inch)

2-7. BUS INTERFACE REQUIREMENTS

The iSBC 094 is designed for installation into a standard Intel iSBC 604/614 Cardcage or in the Intellec System motherboard. As shown in figure 1-1, edge connector P1 provides interface to the Multibus. Connector P1 pin assignments are listed in table 2-1 and descriptions of the signal functions are given in table 2-2. Edge connector P2 is the battery backup and power fail input connector as described in paragraph 2-14. Alternative mating connectors for P1 and P2 are listed in table 2-3.

The ac and dc characteristics of the iSBC 094 are present in tables 2-4 and 2-5, respectively. The bus exchange timing for memory read and write operations is shown in figure 2-1.

2-8. JUMPER AND SWITCH CONFIGURATIONS

Instructions for configuring jumpers to select the 4K memory address block and implement the on-board Initialize (INIT/) and Advanced Acknowledge (AACK/) functions are provided in following paragraphs. Also included are instructions for configuring the power fail and battery backup switches.

2-9. MEMORY ADDRESS BLOCK ASSIGNMENT

Jumper pads XA61 and XA67 provide the means for selecting the iSBC 094 RAM address block. Install one jumper at XA61 to assign the 4K block of locations to the upper or lower half of the 64K byte system memory space. Install a second jumper between one of the eight pin pairs on XA67 to select the starting address of the desired 4K block locations. Table 2-6 lists the base addresses selected by the various jumper configurations.

2-10. INITIALIZE SIGNAL OPTION

The Initialize (INIT/) signal initializes the iSBC 094 control logic by resetting various latches and counters to a known state. There are two sources of the INIT/ signal: the CPU and the iSBC 094. The CPU generates INIT/ (1) during a start-up sequence when power is initially applied to the system and (2) whenever an external "reset" signal is activated. The iSBC 094 ac power fail logic generates INIT/ when the externally supplied ACLO signal is activated. If it is desired to use the INIT/ signal generated by the iSBC 094, connect a jumper between pins 2 and 15 of jumper pad XA61.

Table 2-1. Multibus Connector P1 Pin Assignments

PIN*	SIGNAL	FUNCTION	PIN*	SIGNAL	FUNCTION
1	GND	Ground	44	ADRF/	Address Bus
2	GND		45	ADRC/	
3	+5 VDC	Power Input	46	ADRD/	
4	+5 VDC		47	ADRA/	
5	+5 VDC		48	ADRB/	
6	+5 VDC		49	ADR8/	
7			50	ADR9/	
8			51	ADR6/	
9			52	ADR7/	
10			53	ADR4/	
11	GND	Ground	54	ADR5/	
12	GND		55	ADR2/	
13			56	ADR3/	
14	INIT/	System Initialize	57	ADR0/	
15			58	ADR1/	
16			59	DATE/	Data Bus
17			60	DATF/	
18			61	DATC/	
19	MRDC/	Memory Read Command	62	DATD/	
20	MWTC/	Memory Write Command	63	DATA/	
21			64	DATB/	
22			65	DAT8/	
23	XACK/	Transfer Acknowledge	66	DAT9/	
24	INH1/	Inhibit RAM	67	DAT6/	
25	AACK/	Advanced Acknowledge	68	DAT7/	
26			69	DAT4/	
27	BHEN/	Byte High Enable	70	DAT5/	
28			71	DAT2/	
29			72	DAT3/	
30			73	DAT0/	
31			74	DAT1/	
32			75	GND	Ground
33			76	GND	
34			77		
35			78		
36			79		
37			80		
38			81	+5 VDC	Power Input
39			82	+5 VDC	
40			83	+5 VDC	
41			84	+5 VDC	
42			85	GND	Ground
43	ADRE/	Address Bus	86	GND	

*All unassigned pins are reserved.

Table 2-2. Multibus Signal Functions

SIGNAL	FUNCTIONAL DESCRIPTION
AACK/	*Advanced Acknowledge.* An early indication to the bus master that the iSBC 094 has accepted the command and is executing the specified Memory Read or Memory Write operation.
ADR0/-ADRF/	*Address.* These 16 lines transmit the address of the specific RAM location to be accessed. ADRF/ is the most significant bit.
BHEN/	*Byte High Enable.* Enables the proper data path between RAM and the data buffers.
DAT0/-DATF/	*Data.* These sixteen bidirectional lines transmit and receive data to and from the specified RAM location.
INH1/	*Inhibit RAM.* Prevents the iSBC 094 from responding when the bus master addresses a higher priority device that has the same address as the iSBC 094.
INIT/	*Initialize.* Resets the iSBC 094 circuits to a known internal state.
MRDC/	*Memory Read Command.* Initiates the reading of data from the RAM location specified on the Multibus address lines onto the Multibus data lines.
MWTC/	*Memory Write Command.* Initiates the writing of data from the Multibus data lines into the RAM location specified on the Multibus address lines.
XACK/	*Transfer Acknowlege.* Indicates to the bus master that the iSBC 094 has completed the specified Memory Read or Memory Write operation. That is, data has been placed onto or accepted from the Multibus data lines.

Table 2-3. Mating Connectors

INTERFACE	NO. OF PAIRS/PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR PART NO.
Multibus (P1)	43/86	0.156 in.	Soldered	CDC Micro Plastics ARCO Viking	VPB01E43D00A1[2] MP-0156-43-BW-4 AE443WP1 Less Ears 2VH43/1AV5
Multibus (P1)	43/86	0.156 in.	Wirewrap	CDC CDC Viking	VFB01E43D00A1[2] VPB01E43A00A1 2VH43/1AV5
Auxiliary[1] (P2)	30/60	0.1 in.	Soldered	Viking TI	3VH30/1JN5 H312130
Auxiliary[1] (P2)	30/60	0.1 in.	Wirewrap	CDC TI	VPB01B30A00A2[2] H311130

NOTES:
1. Connector dimensions vary from vendor to vendor. Review vendor specifications to ensure that connector heights and wirewrap pin lengths conform to your system packaging requirements.
2. CDC VPB01 . . . , VPB02 . . . , VPB04 . . . , etc., are identical connectors with different electroplating thickness or metal surfaces.

Table 2-4. iSBC 094 AC Characteristics

PARAMETER	MINIMUM (nsec)	MAXIMUM (nsec)	DESCRIPTION	REMARKS
t_{AS}	50		Address setup to command	From data to command
t_{DS}	50		Write data setup to command	Normal write
t_{AAK}	215	295	Command to advanced acknowledge time	
t_{ACK}	750	819	Command to transfer acknowledge time	
t_{AH}	0		Address hold time	
t_{DH}	0		Write data hold time	
t_{DRH}	0		Read data hold time	
t_{TO}		65	Acknowledge turnoff delay	
t_{ACC}		720	Access time to read data	
$t_{CY(D)}$		819	Minimum cycle time	
t_{IS}	+50	−50	Inhibit setup to command	Blocks RAM cycle and t_{ACK}
t_{IH}	150		Inhibit hold time from command	Blocks AAK if $t_{IS} < t_{IS}$ minimum
t_{IPW}	100		Inhibit pulse width	

Table 2-5. iSBC 094 DC Characteristics

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN.	MAX.	UNITS
ADR0/-	V_{IL}	Input Low Voltage			0.8	V
ADRF/	V_{IH}	Input High Voltage		2.0		V
INIT/ (input)	I_{IL}	Input Current at Low V	V_{IN}=0.4V		−0.40	mA
	I_{IH}	Input Current at High V	V_{IN}=2.7V		20	μA
INH1/	*C_L	Capacitive Load			18	pF
AACK/	V_{OL}	Output Low Voltage	I_{OL}=32 mA		0.4	V
XACK/	V_{OH}	Output High Voltage	I_{OH}=−5.2 mA	2.4		V
	I_{LH}	Output Leakage High	V_O=2.4V		40	μA
	I_{LL}	Output Leakage Low	V_O=0.4V		−40	μA
	*C_L	Capacitive Load			15	pF
DAT0/	V_{OL}	Output Low Voltage	I_{OL}=50 mA		0.6	V
DATF/	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.45V		−0.25	mA
	I_{LH}	Output Leakage High	V_O=5.25V		100	μA
	*C_L	Capacitive Load			18	pF
PFSN/	V_{OL}	Output Low Voltage	I_{OL}=16 mA		0.4	V
PFIN/	V_{OH}	Output High Voltage	OPEN COLLECTOR			
INIT/ (output)	*C_L	Capacitive Load			18	pF
ACLO	I_{IL}	Input Current at Low V	V_{IN}=0.4V		0.01	mA
PFIN/	I_{IH}	Input Current at High V	V_{IN}=5.0V		0.01	mA
PFSR/	V_{IL}	Input Low Voltage		2.5		V
	V_{IH}	Input High Voltage		2.5		V
	*C_L	Capacitive Load			18	pF
MRDC/	V_{IL}	Input Low Voltage			0.8	V
MWTC/	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.4V		−1.6	mA
	I_{IH}	Input Current at High V	V_{IN}=5.5V		1	mA
	*C_L	Capacitive Load			18	pF

*Capacitance values are approximations.

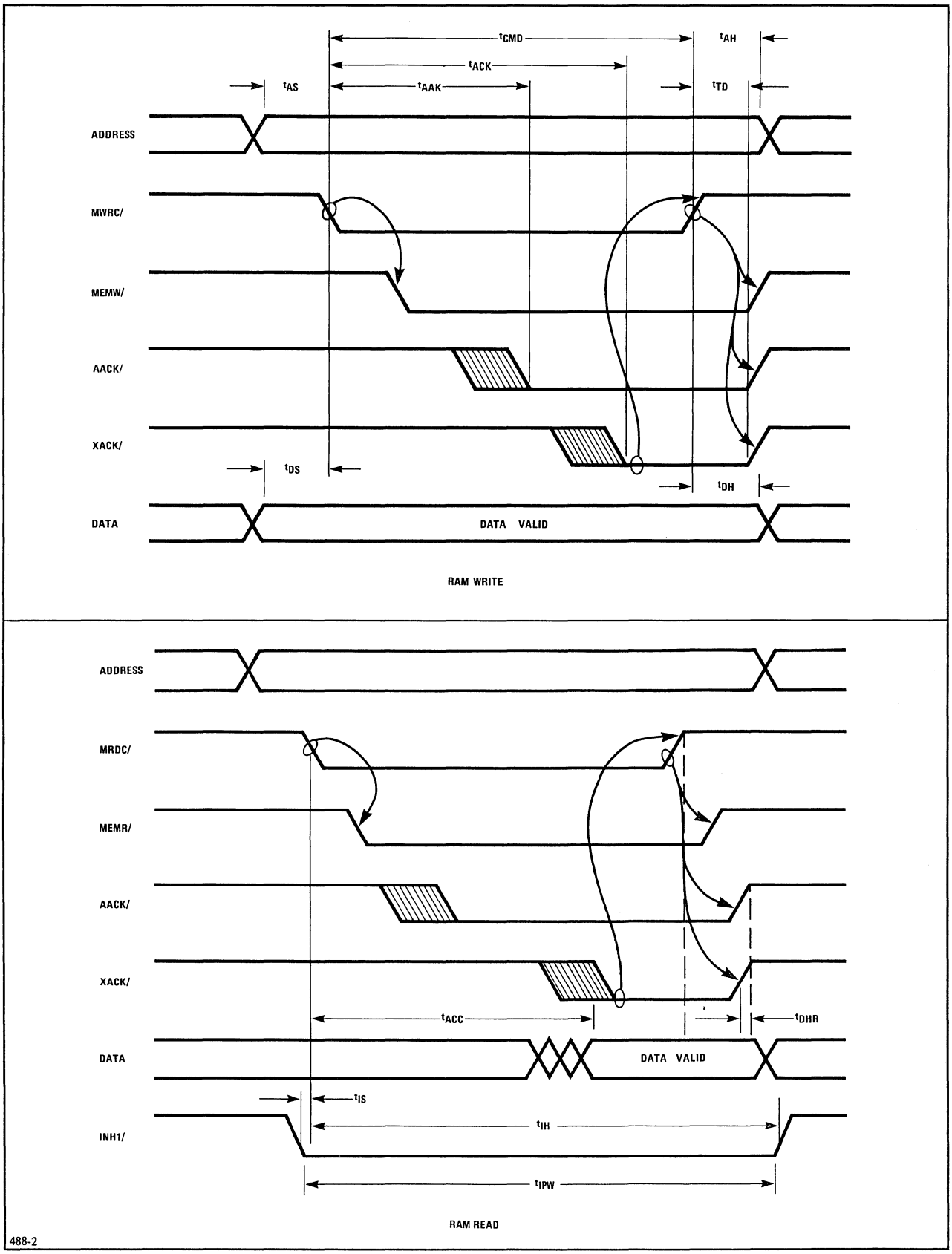


Figure 2-1. Bus Exchange Timing

Table 2-6. Memory Address Block Assignment Jumpers

2K X 16 bit MEMORY BLOCK	4K X 8 bit MEMORY BLOCK	JUMPER XA61	JUMPER XA67
0-2K	0-4K		1-16
2-4K	4-8K		2-15
4-6K	8-12K		3-14
6-8K	12-16K		4-13
8-10K	16-20K	4-13	5-12
10-12K	20-24K		6-11
12-14K	24-28K		7-10
14-16K	28-32K		8-9
16-18K	32-36K		1-16
18-20K	36-40K		2-15
20-22K	40-44K		3-14
22-24K	44-48K	3-14	4-13
24-26K	48-52K		5-12
26-28K	52-56K		6-11
28-30K	56-60K		7-10
30-32K	60-64K		8-9

2-11. ADVANCED ACKNOWLEDGE SIGNAL OPTION

After the bus master has issued a Read or Write Command, it requires a Transfer Acknowledge (XACK/) or an Advanced Acknowledge (AACK/) signal response from the iSBC 094. (Refer to table 2-2 for a functional description of the XACK/ and AACK/ signals.)

All systems can operate using the XACK/ signal. However, in some systems the XACK/ signal occurs so long after the command is issued that the bus master must idle in one or more wait states before proceeding with the sequence that completes the data transfer. In such systems, the access time can be enhanced by employing the AACK/ signal. The AACK/ signal occurs approximately 500 nanoseconds before the XACK/ signal and, when employed, may eliminate the need for bus master wait states.

The AACK/ signal can only be used in systems in which the timing cycle of the bus master makes its use feasible. In systems in which there is more than one bus master, the AACK/ signal can be employed only if its timing is compatible with the cycle of the fastest bus master in the system.

If the AACK/ signal is to be used, connect a jumper between pins 5 and 12 of jumper pad XA61; otherwise, disable the AACK/ signal by connecting a jumper between pins 6 and 11 of jumper pad XA61.

2-12. POWER FAIL SWITCHES

Switches S1 and S2 shown in figure 1-1 are connected in parallel and are used to enable or disable the ac power fail circuit. Close both S1 and S2 when the iSBC 094 is being installed in or removed from the cardcage. After the board is seated into the backplane, set both S1 and S2 to the OPEN position.

2-13. BACKUP BATTERY SWITCHES

Switches S3 and S4 shown in figure 1-1 are connected in parallel to enable or disable the backup battery. Set both S3 and S4 to the OPEN position when the iSBC 094 is being installed in or removed from the cardcage, and whenever the iSBC 094 is being stored with the battery in place. After the board is seated into the backplane and power has been applied to the system, set both S3 and S4 to the closed position.

2-14. POWER FAIL CONNECTIONS

A mating connector must be installed in the Intellec System chassis, iSBC 604, or iSBC 614 to accommodate power fail connector P2. (Refer to figure 1-1.) Table 2-3 lists and describes some 60-pin connectors that may be used for this purpose; both solder and wirewrap connectors are listed. Table 2-7 correlates the signals and pins on the connector.

Table 2-7. Power Fail Connector P2 Pin Assignments

PIN	SIGNAL	FUNCTION
1 and 2	GND	Signal ground.
3 and 4	+VB	Battery test point.
13	PFSR/	Power Fail Sense Reset. Resets latch in ac power fail logic that generates PFSN/ signal. PFSR/ is generated as a result of an external switch closure.
17	PFSN/	Power Fail Sense. Indicates to the CPU that an ac power failure has occurred.
18	ACLO	AC Low. Triggers ac power fail circuit when ac power to the system power supply drops below 103/206V ac.
19	PFIN/	Power Fail Interrupt. Informs CPU that ac power fail circuit has been activated by ACLO signal.

Procure the appropriate mating connector for P2 and secure it in place as follows:

a. Position holes in P2 mating connector over mounting holes that are in line with corresponding P1 mating connector.

b. From top of connector, insert two 0.5-inch #4-40 pan head screws down through connector and mounting holes.

c. Install a flat washer, lock washer, and star-type nut on each screw; then tighten the nuts.

When the mating connector for P2 is in place, wire the power fail signals to the appropriate pins of the connector as listed in table 2-7. In a typical system, these signals would be wired as follows:

a. System power supply ground connected to P2 pins 1 and 2.

b. ACLO signal from system power supply connected to P2 pin 18.

c. PFSN/ signal from P2 pin 17 connected to Power Fail Status (PFS) input of CPU.

d. PFIN/ signal from P2 pin 19 connected to Power Fail Interrupt (PFI) input of CPU.

The PFSR/ signal is input to the iSBC 094 at connector P2 pin 13. The PFSR/ signal is generated by an off-board switch that must be attached to a convenient location on the Intellec chassis or iSBC 604 or 614 Cardcage. When the switch has been secured mechanically, wire it so that ground is applied to P2-13 when the switch is actuated. Grounding P2-13 resets the PFSN/ signal to the CPU.

2-15. BOARD INSTALLATION

Always turn off the computer power before installing or removing the iSBC 094 board. Also refer to paragraphs 2-12 and 2-13 and configure switches S1 through S4 properly before installing or removing the iSBC 094 board. Failure to take this precaution can result in damage to the board.

In an iSBC Single Board Computer based system, install the board in any slot that has not been wired for a dedicated function. In an Intellec Microcomputer Development System, install the board in any slot except slots 1 and 2. Ensure that power fail connector P2 mates with the user-installed mating connector.

2-16. PROGRAMMING CONSIDERATIONS

The iSBC 094 presents two areas of concern to the programmer: 1) memory addressing and 2) processing the power fail interrupt (PFIN/) and the other signals associated with the ac power fail feature.

2-17. MEMORY ADDRESSING

Because the iSBC 094 represents a portion of system memory, the addresses assigned to the iSBC 094 must not overlap addresses assigned to other blocks of system memory. For example, if the iSBC 094 and an iSBC 104 Combination Memory and I/O Board were assigned the same 4K byte or 2K word segment of addresses, both boards will respond when the addresses are called. If the iSBC 094 is assigned the same addresses as PROM or other higher-priority device in the system, the higher-priority device will activate the Multibus inhibit (INH1/) line when the addresses are called. When active, INH1/ essentially disconnects the iSBC 094 from the system by disabling the iSBC 094 board's memory buffers and XACK/ and AACK/ signals. Consequently, the higher-priority device will function normally, but the iSBC 094 will not respond to the bus master command.

There are certain instances in which the latter situation can be used advantageously. For example, a PROM board equipped with RAM inhibit (e.g., iSBC 416 PROM) and having the same addresses as the iSBC 094 can be connected to the Multibus for maintenance purposes. When the maintenance tasks have been performed and the PROM board is removed from the Multibus, the iSBC 094 will function again as an extension of system memory.

Paragraph 2-9 explains how the iSBC 094 memory address boundaries are established.

2-18. AC POWER FAIL

The ac power fail circuit, in conjunction with the on-board backup battery, enhances the use of the iSBC 094 as a storage area for data such as the program stack, critical data, and other program information that must be protected. Connector P2 pin locations of all signals relating to the ac power fail feature are given in table 2-7.

When the ac power line voltage drops below 103/203V ac (rms), the system power supply activates the ACLO signal. In response to ACLO, the ac power fail circuit generates the power fail interrupt (PFIN/). This signal indicates the start of a 3.6-msec period during which the CPU may transfer machine status and other critical parameters to the iSBC 094 RAM Board. When this 3.6-msec period has elapsed, the ac power fail circuit denies access to RAM until system power is restored. The integrity of these RAM protect functions can only be ensured if the system power supply generates ACLO at least 7 milliseconds before the dc power source output falls below the prescribed operating limits.

The on-board backup battery ensures the integrity of the RAM contents for a minimum of 96 hours after the loss of main power. Any subroutine intended to service the PFIN/ interrupt must reflect the fact that RAM accessibility is limited to a specific time period following the interrupt.

The ACLO/ signal that is generated by the system power supply prior to a power loss also sets the power sense latch in the ac power fail circuit. When set, the power sense latch activates the power fail sense (PFSN/) signal. During a system power up, the PFSN/ signal can be sensed by the CPU to determine if the previous removal of power occurred as the result of a power failure or a normal power shutdown.

The power fail sense latch is reset by the power fail sense reset (PFSR/) signal. This signal is generated by an off-board switch that must be wired to the ac power fail circuits during installation of the iSBC 094. The procedure for installing and wiring the power fail sense reset switch is given in paragraph 2-14.

Procedures for powering up the system must take into account the power fail sense (PFSN/) signal, the power fail sense reset (PFSR/) signal and, if a power loss has occurred, the power fail interrupt service routine. The following steps must be included in any initial power-up sequence; i.e., power is off due to a normal power shutdown sequence.

a. Activate the off-board power fail sense reset switch and keep it actuated through step c below.

b. Turn on system power. (This will force a power-up reset.)

c. Sense the PFSN/ input from the iSBC 094. The PFSN/ signal will be false because the switch is actuated. Deactuate the switch.

d. Initialize the system and begin execution of the program.

The following steps must be included in any system power-up procedure following a system power loss.

a. When power is restored, a power-up reset is generated.

b. Sense the PFSN/ input from the iSBC 094. The PFSN/ signal will be true.

c. Activate the PFSN/ switch and initialize the system hardware.

d. Restore the software state of the machine from the data saved by the power fail interrupt service routine.

e. Terminate the power fail interrupt service routine and return to the interrupted program.

CHAPTER 3
PRINCIPLES OF OPERATION

3-1. INTRODUCTION

This chapter details the operation of the iSBC 094 with reference to block and logic diagrams that are interspersed with the text, and to the iSBC 094 schematic diagram located at the end of chapter 4.

Both active-high (positive-true) and active-low (ground-true) signals appear on the schematics and drawings. To avoid confusion when referring to these signals, the following convention is used. The mnemonic for each active-low signal is terminated by a slash (e.g., SEL/). Such references indicate that the signal level is low when the condition is true (active). A mnemonic without a slash (e.g., ESB) refers to an active-high signal. These references indicate that the signal level is high when the condition is true (active).

3-2. FUNCTIONAL DESCRIPTION

The iSBC 094 (figure 3-1) is divided into five functional areas: address decoders, RAM array, memory buffers, control logic, and power fail circuits. All data is transferred between the iSBC 094 and the bus master over the bidirectional data bus (DAT0/ through DATF/). Data is channeled between the data bus and RAM via the memory buffers.

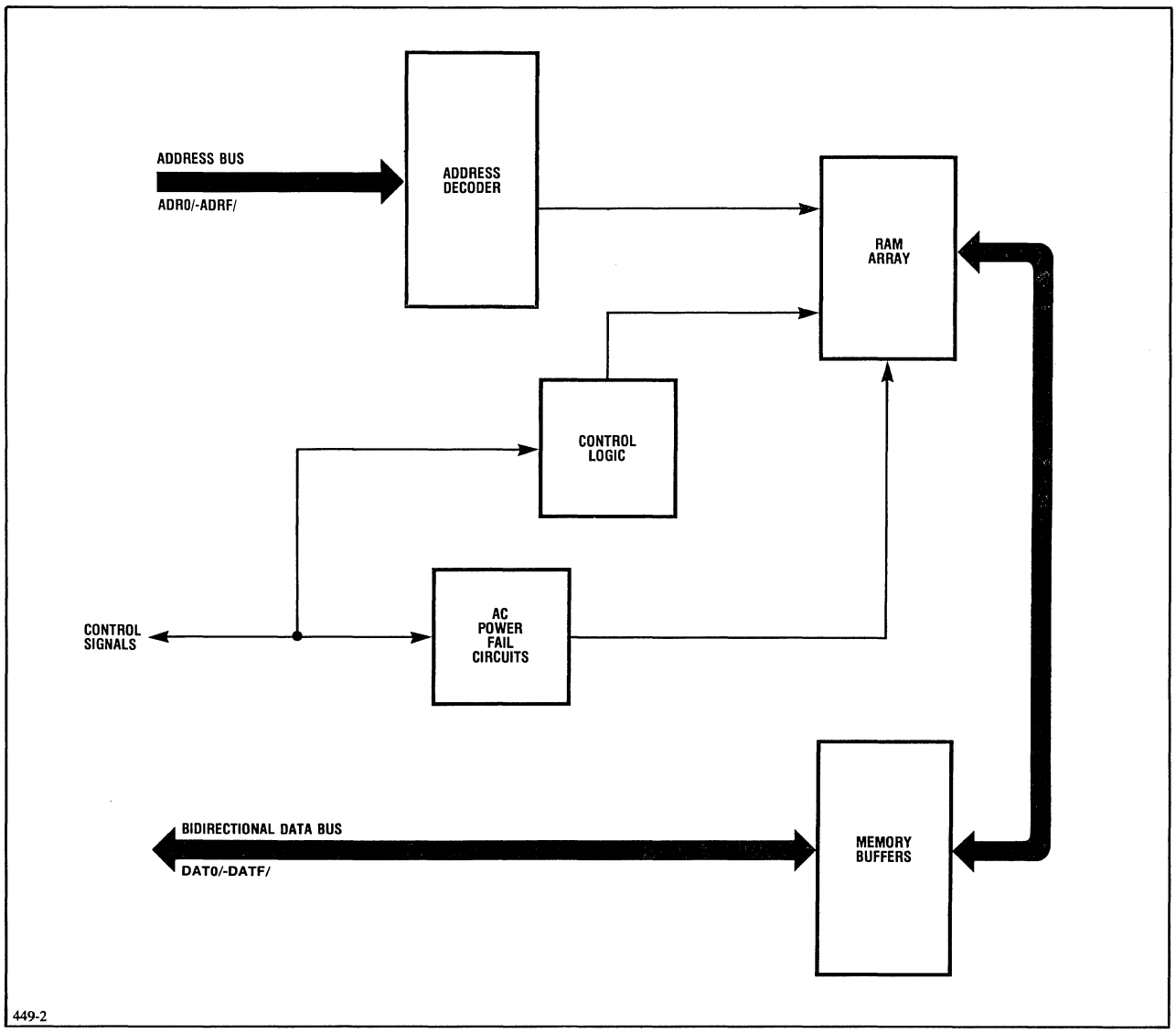


Figure 3-1. iSBC 094 Functional Block Diagram

These buffers are composed of line receivers and line drivers to maintain compatibility between the Multibus and the iSBC 094 logic. Timed signals from the control logic activate the drivers in the memory buffer during read operations, and activate the receivers in the memory buffer during write operations. When the iSBC 094 is not selected, the memory buffers are essentially disconnected from the data bus.

The RAM location used in a data transfer is specified by a 16-bit system address. This address is transmitted over the address bus that connects to all of the system devices. From the system address the iSBC 094 decoders generate the signals required to select a specific byte or word location in the RAM array of the addressed board.

All timing and control signals required for data transfers are generated by the iSBC 094 control logic. The control sequences that produce these signals are initiated by Read and Write Commands from the bus master.

The ac power fail circuits flag the CPU in the event of a power failure. The power fail circuits then provide a period during which the CPU can store critical data in RAM. When this period has elapsed, the ac power fail circuits deny access to RAM until main power is restored.

3-3. BOARD SELECTION

The iSBC 094 board address is decoded from the four most-significant bits (ADRC/ through ADRF/) of the address. The decoding is accomplished by Intel 8205 one-of-eight decoder A66. (See chart 3 of the schematic.) ADRF/, the most-significant bit, is applied to the high-true enable input of A66 in either its true or false state. When ADRF/ is true, the RAM address occupies an area in the upper half of the system memory space. When ADRF/ is false, the RAM address occupies an area in the lower half of the system memory space. The true or false state of ADRF/ is applied to the 8205 decoder as a function of a jumper connected between pins 4 and 13 or pins 3 and 14 of XA61.

Address bits ADRC/ through ADRE/ are decoded by A66 into one of eight low-true outputs. Each output represents the starting location of a 4K block of memory. The decoder output representing the desired RAM starting address is jumpered to the SEL/ line. The SEL/ line represents the board select level in that it must be true to allow the control logic to respond to the bus master Read and Write Commands.

3-4. RAM CHIP ADDRESSING

Logically, the 4K of RAM is divided into two 2K by 8-bit arrays. (Refer to figure 3-2.) They are referred to as the odd and even, or upper and lower, arrays.

Consecutive bytes of a data transfer are not stored in contiguous locations of the same array. Rather, bytes with odd addresses are stored in the odd array, and bytes with even addresses are stored in the even array. The function of selecting the alternate arrays is accomplished by the Enable Swap Byte (ESB) logic. This logic, in turn, is controlled by ADR0/ (the least significant address bit) and by the Byte High Enable (BHEN/) signal.

During a write operation, all data is transferred to the iSBC 094 via the Multibus. Data is routed through the line receivers in Memory Data Buffers A54, 55, 56 & 57 to the RAM arrays. If BHEN/ and ADR0/ are false, the ESB logic enables chip decoder A44. When enabled, A44 decodes address lines ADR9/ through ADRB/, and raises one of the eight chip enable lines CE1 through CE8. The enabled CE line selects a specific pair of chips in the upper RAM array. Address lines ADR1/ through ADR8/ are decoded to select a specific 8-bit byte within the selected chip pair (four bits in each chip). When the Write Command arrives from the bus master, the data byte is written into the addressed 8-bit location.

When the bus master sends the next consecutive address to write the next 8-bit byte, ADR0/ is true. Consequently, the ESB logic enables chip decoder A43. This decoder samples address bits ADR9/ through ADRB/, and raises one of the eight lines CE9 through CE16 to the lower array. Because ADR0/ is true and BHEN/ is false, the ESB logic generates a signal that gates the data from Memory Data Buffer A56/57 through a set of 3-state drivers to the lower array. As successive bytes of a block of data arrive, the iSBC 094 acts in this manner to store alternate bytes in the upper and lower arrays.

To write a 16-bit word, BHEN/ must be true, and ADR0/ false.

Addressing for a read operation is accomplished in the same manner as for a write operation. However, the flow of data is in the opposite direction. During a read operation, data is channeled from the selected array through the memory line drivers to the Multibus. When a byte is read out of the upper array, it is channeled through the line drivers in Memory Data Buffer A56/57 to data lines DAT0/ through DAT7/. When data is read out of the lower array, the ESB logic generates a signal that gates the data through a set of 3-state drivers to Memory Data Buffer A56/57. The drivers in A56/A57 channel the data onto data lines DAT0/ through DAT7. As in a write operation, the ESB logic generates the gating signal as a function of ADR0/ (false) and BHEN/ (false).

Each RAM chip has a secondary enabling input (CE2). If main power is lost, the ac power fail logic (paragraph 3-9) prohibits access to the RAM array by applying CBAR/ to these inputs.

3-5. READ/WRITE CONTROL TIMING

Upon receiving a Read or Write Command from the bus master, the iSBC 094 initiates a sequence of operations that effects the transfer of data into or out of the RAM array. The basic timing for the sequence is provided by a 16-stage shift register (A47/A46) that is stepped by a 20-MHz clock (A36-12). (See sheet 4 of the schematic.) When stepped, the shift register generates timing segments T0 through T15.

3-6. BASIC READ/WRITE CONTROL CYCLE

As explained previously, address selection is accomplished prior to the arrival of a Read or Write Command from the bus master. The select operation forces SEL/ true (low). (See sheet 4 of the schematic.) With SEL/ true, the signal MRD/ (A37-12)

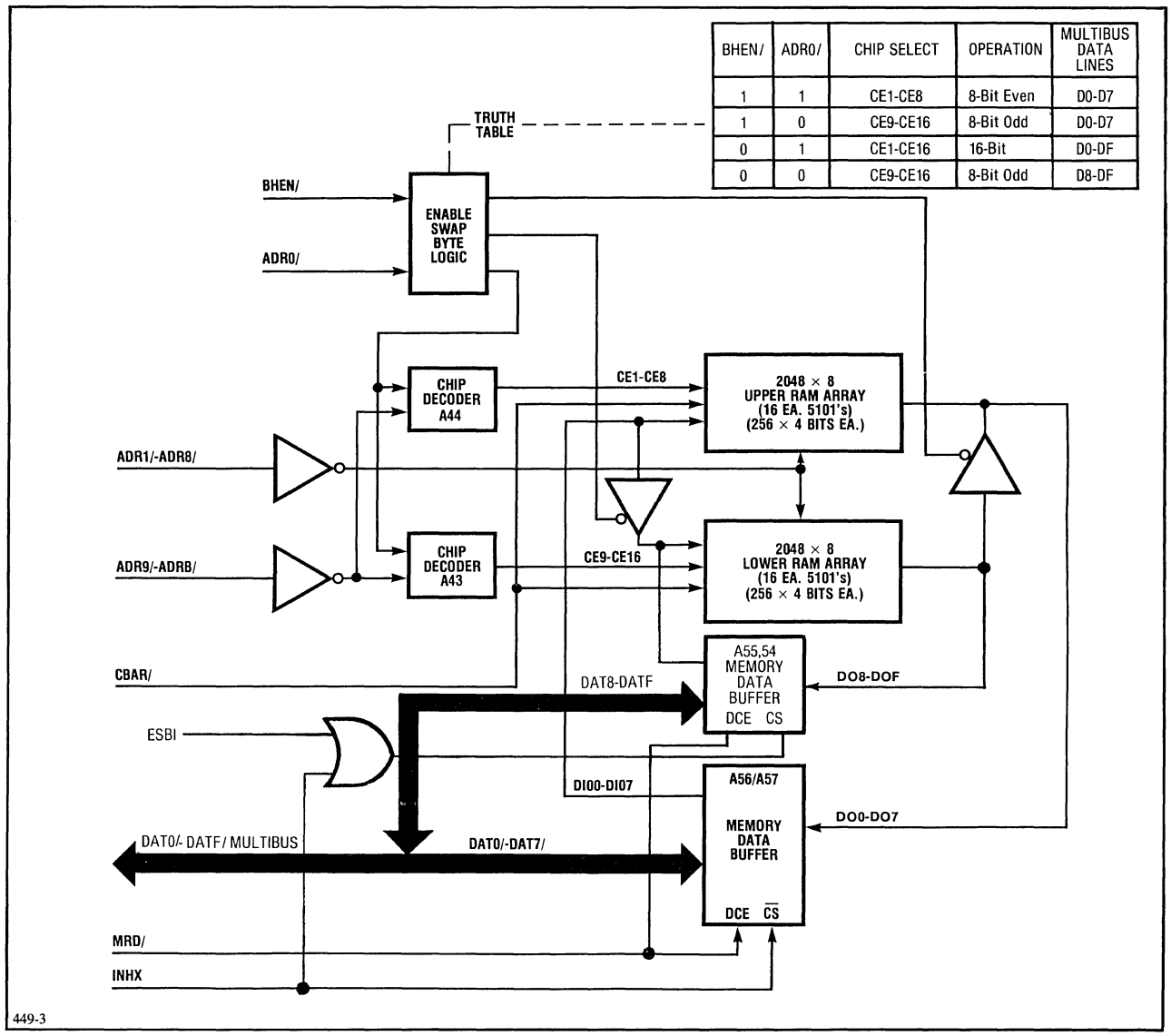


Figure 3-2. RAM Chip/Byte Selection and Memory Buffer

is driven true if the subsequent command is a read, or false if the subsequent command is a write. Depending upon its state, MRD/ enables the memory buffer receivers (write) or drivers (read).

In addition, because SEL/ is true, the arrival of a read (MRDC/) or write (MWTC/) command sets latch A48-5. With A48-5 set, timing pulses from A36-12 begin shifting ones through shift register A47/A46.

If the operation is a write, outputs from the shift register set latches A51-9 and A39-5 at T1 and T4, respectively. With these latches set, A38-8 generates the write enable levels (WE1/ and WE2/) that write the data into the selected RAM locations. The WE levels remain active until T13, at which time latch A51-9 is reset.

At T14, the shift register output at A46-12 is converted to the XACK/ level and is sent to the bus master. If the operation is a write, XACK/ informs the bus master that the data on the data bus has been written into the addressed RAM location. If the operation is a read, XACK/ informs the bus master that the data requested from RAM is available on the data bus.

In response to XACK/, the bus master deactivates the command (MRDC/ or MWTC/ goes high), setting latch A48-9. Setting this latch triggers one-shot A53-6 which, in turn, resets the shift register and latches A48-5 and -9. This represents the end of the basic transfer cycle.

3-7. ADVANCED ACKNOWLEDGE

The QE output from shift register A47 is inverted and can be sent to the bus master as the Advanced Acknowledge (AACK/) signal (sheet 4 of the schematic). This signal is generated approximately 500 nanoseconds before Transfer Acknowledge signal XACK/. The AACK/ signal informs the bus master that the read or write transfer will be completed early enough so that the bus master can proceed with its basic timing sequence. Were it not for AACK/, the bus master would not be informed of the status of the data transfer until the arrival of XACK/.

In some systems the XACK/ signal occurs so late in the current bus master timing state that the bus master would enter a wait state before proceeding to the next timing state. In such systems, the access time of the system is enhanced by employing the AACK/ signal, thereby eliminating the need for a bus master wait state.

The AACK/ signal is generated by the iSBC 094 and is routed to the bus master only if a jumper is installed between pins 5 and 12 of XA61.

3-8. INHIBIT CIRCUITS

If the bus master issues an iSBC 094 address, and if there is a higher-priority device with the same address, the other device can issue an inhibit (INH1/) signal. Essentially, the INH1/ signal disconnects the iSBC 094 from the system by disabling its memory buffers and its XACK/ and AACK/ signals.

When INH1/ is activated, it disables gate A40-12 (sheet 4 of the schematic). The resultant INHX signal disconnects the memory buffers from the system bus. Disabling gate A40-12 also disables the drivers that route the XACK/ and AACK/ signals to the bus master.

If at this time the iSBC 094 board is selected and a Read or Write Command is issued, latch A48-5 is set. With the setting of A48-5, the control logic proceeds to generate the timing and control signals that execute the operations of the command. However, the iSBC 094 is isolated from the Multibus because gate A40-12 is disabling the memory buffers and the XACK/ and AACK/ drivers. When the command is removed, the control logic is reset by the triggering of one-shot A53-6 in the same manner as during the execution of a normal command. (Refer to paragraph 3-6.)

At the same time that the Read or Write Command initiated the setting of latch A48-5, inhibit latch A39-8 was also set because INH1/ is true. If INH1/ becomes false while the control logic is processing the invalid command, the reset output from A48-5 keeps gate A40-12 disabled. As a result, the memory buffers and the XACK/ and AACK/ drivers are kept disabled until the processing is complete and the control logic is reset in the normal manner. Inhibit latch A39-8 is reset (via A40-8) at the same time that the other control logic latches are reset.

If a command intended for the iSBC 094 is issued between the time that INH1/ is activated and deactivated, the inhibit logic ensures that the command is executed. It is executed after the sequence initiated by the invalid (inhibited) command has been completed. In this instance, the valid command will still be present after the control logic (including inhibit latch A39-8) is reset. With the resetting of A39-8, INHX goes false, enabling the memory buffers and the XACK/ and AACK/ drivers.

At the end of the invalid sequence, the negative level that resets inhibit latch A39-8 is inverted and applied to latch A48-5. This level is a function of one-shot A53-6 that initiates the final resetting of the control logic. When the one-shot delay times out, latch A48-5 is set. The control logic responds to the setting of this latch as if a command were issued from the bus master. That is, it executes the sequence dictated by the current command.

3-9. AC POWER FAIL CIRCUIT

The ac power fail circuits are shown on sheet 4 of the schematic. In the event of a power failure, these circuits: (1) send an interrupt to the CPU, (2) set a latch to remember that a power failure occurred, and (3) inhibit access to RAM and clear the control logic after a 3.6-msec delay.

When ac power falls below a prescribed limit, the system power supply activates the ACLO signal. ACLO triggers one-shot A53-10, and the power fail interrupt (PFIN/) is sent immediately to the CPU.

ALCO also sets power fail sense (PFSN) latch A70-12. This latch stores the fact that a power failure has occurred. It can be sensed during the next power-up sequence to inform the CPU of the cause of the power shutdown. The PFSN latch can only be reset by PFSR/ which is generated by an off-board switch.

When the A53-10 one-shot delay times out, it sets latch A70-1. When set, A70-1 generates CBAR/ and INIT/. CBAR/ disables the CE2 input to all of the RAM chips on the board. This prevents memory from being accessed until the ACLO signal is removed. Note that the CPU is allowed the 3.6 milliseconds from the generation of PFIN/ until the generation of CBAR/ to retrieve critical data from memory.

When a jumper is installed between pins 2 and 15 of XA61, INIT/ undergoes a double inversion and becomes the INITX/ signal; INITX/ drives the output of gate A50-8 low, resetting the control logic.

Latch A70-1 is reset when the A53-10 one-shot delay has timed out and ACLO goes false (power restored). When reset, A70-1 drives CBAR/ and INIT/ false.

Most of the ac power fail circuits are powered by the back-up battery circuit during a power failure. For this reason, these circuits are implemented using low-powered CMOS devices.

3-10. BATTERY CHARGING CIRCUIT

This circuit is shown on sheet 1 of the schematic. It consists of transistors Q1 and Q2, diodes CR2 through CR6, and switches S3 and S4. The switches connect the charging circuit to the nickel-cadmium backup batteries.

The battery charging circuit is powered by the system +5V supply via connector P1. The battery is in the charge mode as long as the +5V supply remains valid and battery switches S3 and S4 are closed. In this mode, the charging circuit performs as a constant current source and charges the battery at a 10- to 20-mAH. A minimum 14-hour charging period is required to ensure a full charge.

The loss of the system +5V supply places the battery circuit in the discharge mode. When discharging, the battery supplies power to the RAM array to maintain data integrity for a minimum of 96 hours after main power is lost. It also supplies power to the ac power fail circuits to ensure generation of the PFIN/, PFSN/, INIT/, and CBAR/ signals.

CHAPTER 4
SERVICE INFORMATION

4-1. INTRODUCTION

This chapter provides service diagrams and service and repair assistance instructions for the iSBC 094.

4-2. SERVICE DIAGRAMS

The iSBC 094 parts location and schematic diagrams are given in figure 4-1 and 4-2, respectively. The schematic diagram consists of four sheets, each marked with grid coordinates. Signals that transverse from one sheet to another are assigned grid coordinates at both the signal source and destination. For example, the grid coordinates 2ZD8 locate a signal source or destination on sheet 2 in Zone D8.

Both active-high (positive-true) and active-low (ground-true) signals appear on the schematics. To avoid confusion as to the meaning of these signals, the following convention is used. The mnemonic for each active-low signal is terminated by a slash (e.g., SEL/). Such references indicate that the signal level is low when the condition is true (active). A mnemonic without a slash (e.g., ESB) refers to an active-high signal. These references indicate that the signal level is high when the condition is true (active).

4-3. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCSD Technical Support Center in Santa Clara, California at one of the following numbers:

Telephone:
From Alaska or Hawaii call –
(408) 987-8080
From locations within California call toll free –
(800) 672-3507
From all other U.S. locations call toll free –
(800) 538-8014
TWX: 910-338-0026
TELEX: 34-6372

Always contact the MCSD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCSD Technical Support Center to initiate the repair.

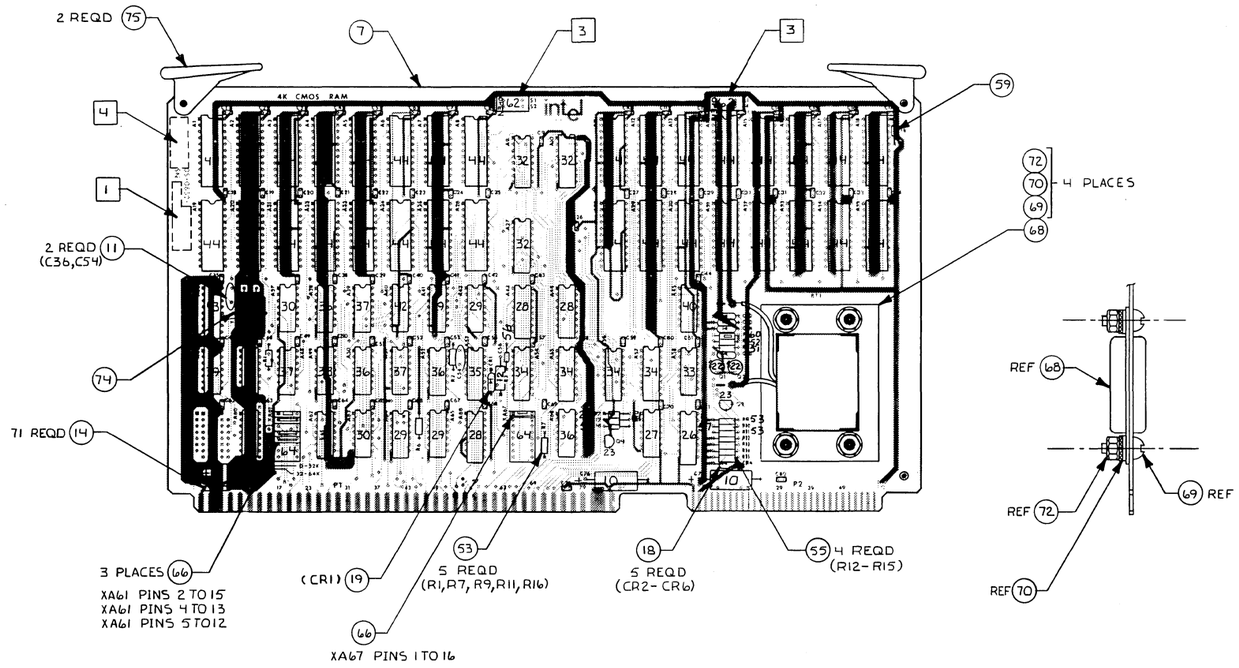
In preparing the product for shipment to the MCSD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCSD Technical Support Center personnel.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

NOTES: UNLESS OTHERWISE SPECIFIED

1. STAMP ASSEMBLY DASH NO., REV LEVEL AND SERIAL NO. APPROXIMATELY WHERE SHOWN WITH BLACK INDELIBLE INK.
2. ASSEMBLE PER INTEL SPECIFICATION 99-0007-001.
3. DIP SWITCHES S1 THRU S4 (ITEM 62) MUST BE SWITCHED TO THE OPEN POSITION AFTER ASSEMBLY.
4. STAMP MCD P/N "PWA460138B-01" APROX WHERE SHOWN WITH CONTRASTING INDELIBLE INK.



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01	7259		2-7-79	001		
00	4810		9-13-77	000	SBC-094/IN-8100	

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PCB ASSEMBLY
4K CMOS RAM
SBC-094/IN-8100

SIZE	DRAWING NO.	REV
D	05-0652-002	00

SCALE 1/1 SHEET 1 OF 1

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05-0652-002

Figure 4-1. SBC 094 Parts Location Diagram

DEVICE TABLE					
TYPE	GND	+5.0V	+VB	REF DES	UNUSED OUTPUT PINS
4049	8		1	A71	
4013	7		14	A70	
3205	8	16		A43, A44, A66	
74LS04	7	14		A41, A42, A64, A65	A65-2,4,8,10,12
74S04	7	14		A37, A63	
7402	7	14		A62	A62-10
74367	8	16		A9, A10, A27	
7405	7	14		A58	A58-2,4,12
3226	8	16		A54-A57	
9602	8	16		A53	
74S00	7	14		A38, A50, A52, A68	A38-6, A68-11
74S74	7	14		A39, A48, A51	A51-5
74S02	7	14		A49	
74164	7	14		A46, A47	A46-3,4,5,6,13, A47-3,5,11,12
4001	7		14	A45	A45-3,10,11
74366	8	16		A60	A60-3, 5, 7, 9
74S10	7	14		A40	A40-6
8224	8	16		A36	
5101	8		22	A1-A8, A11-A26, A28-A35	
SPARE	8	16		A59, A69	

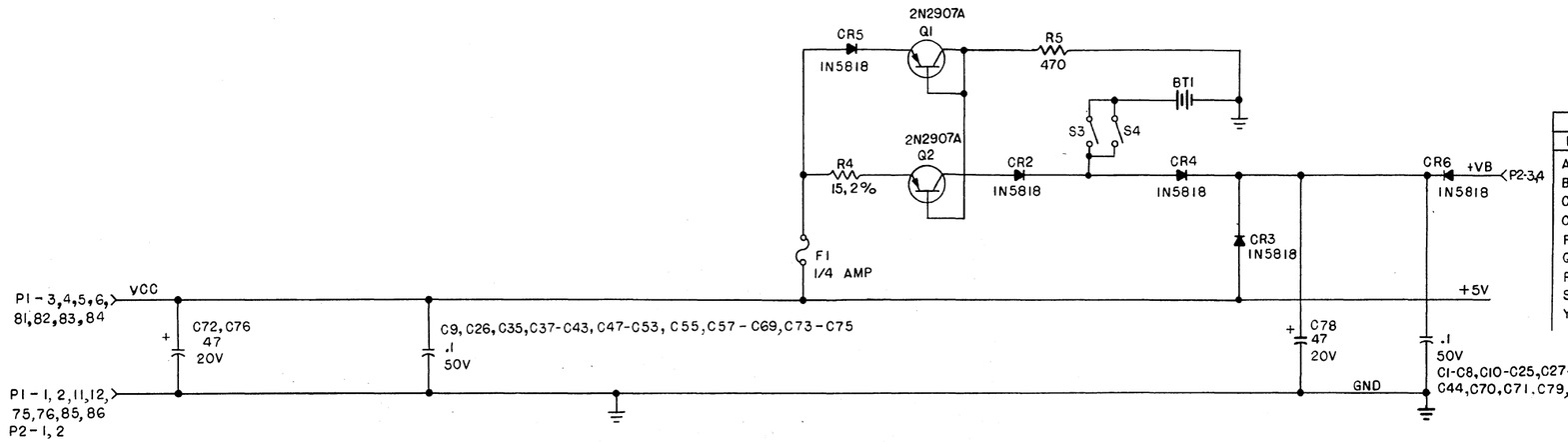
A61 / AACK	12-5	11-6
ENABLE AACK	S	O
DISABLE AACK	O	S

JUMPER FIELD CONFIGURATION:

S = SHORT
O = OPEN

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, 1/4 WATT
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS
3. ALL DIODES ARE IN5818

MEMORY RANGE	OPERATION	8 BIT / 16 BIT	0-4K / 0-2K	4K-8K / 2K-4K	8K-12K / 4K-6K	12K-16K / 6K-8K	16K-20K / 8K-10K	20K-24K / 10K-12K	24K-28K / 12K-14K	28K-32K / 14K-16K	32K-36K / 16K-18K	36K-40K / 18K-20K	40K-44K / 20K-22K	44K-48K / 22K-24K	46K-50K / 24K-26K	50K-54K / 26K-28K	54K-60K / 28K-30K	60K-64K / 30K-32K
JUMPER FIELD	CHIP A61	4-13	S	S	S	S	S	S	S	S	O	O	O	O	O	O	O	O
		3-14	O	O	O	O	O	O	O	O	S	S	S	S	S	S	S	S
	CHIP A67	1-16	S	O	O	O	O	O	O	O	S	O	O	O	O	O	O	O
		2-15	O	S	O	O	O	O	O	O	O	S	O	O	O	O	O	O
		3-14	O	O	S	O	O	O	O	O	O	O	S	O	O	O	O	O
		4-13	O	O	O	S	O	O	O	O	O	O	O	S	O	O	O	O
		5-12	O	O	O	O	S	O	O	O	O	O	O	O	S	O	O	O
		6-11	O	O	O	O	O	S	O	O	O	O	O	O	O	S	O	O
		7-10	O	O	O	O	O	O	S	O	O	O	O	O	O	O	S	O
		8-9	O	O	O	O	O	O	O	S	O	O	O	O	O	O	O	S



REFERENCE DESIGNATIONS	
HIGHEST USED	NOT USED
A71	C45
BT1	C46
C80	C77
CR7	
F1	
Q4	
R18	R8
S4	
Y1	

REV	E.O. NO.	REL	DATE	DASH NO.	MODEL NO.	USED ON
00	7438			002		
00	7259			001		
00	4910			000	SBC-094 IN-8100	05-0652-XXX

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4K CMOS RAM
SBC-094/IN-8100

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SCALE: NONE | SHEET 1 OF 4

DWG NO. 01-0652-002

98-0047-000

Figure 4-2. SBC 094 Schematic Diagram (Sheet 1 of 4)

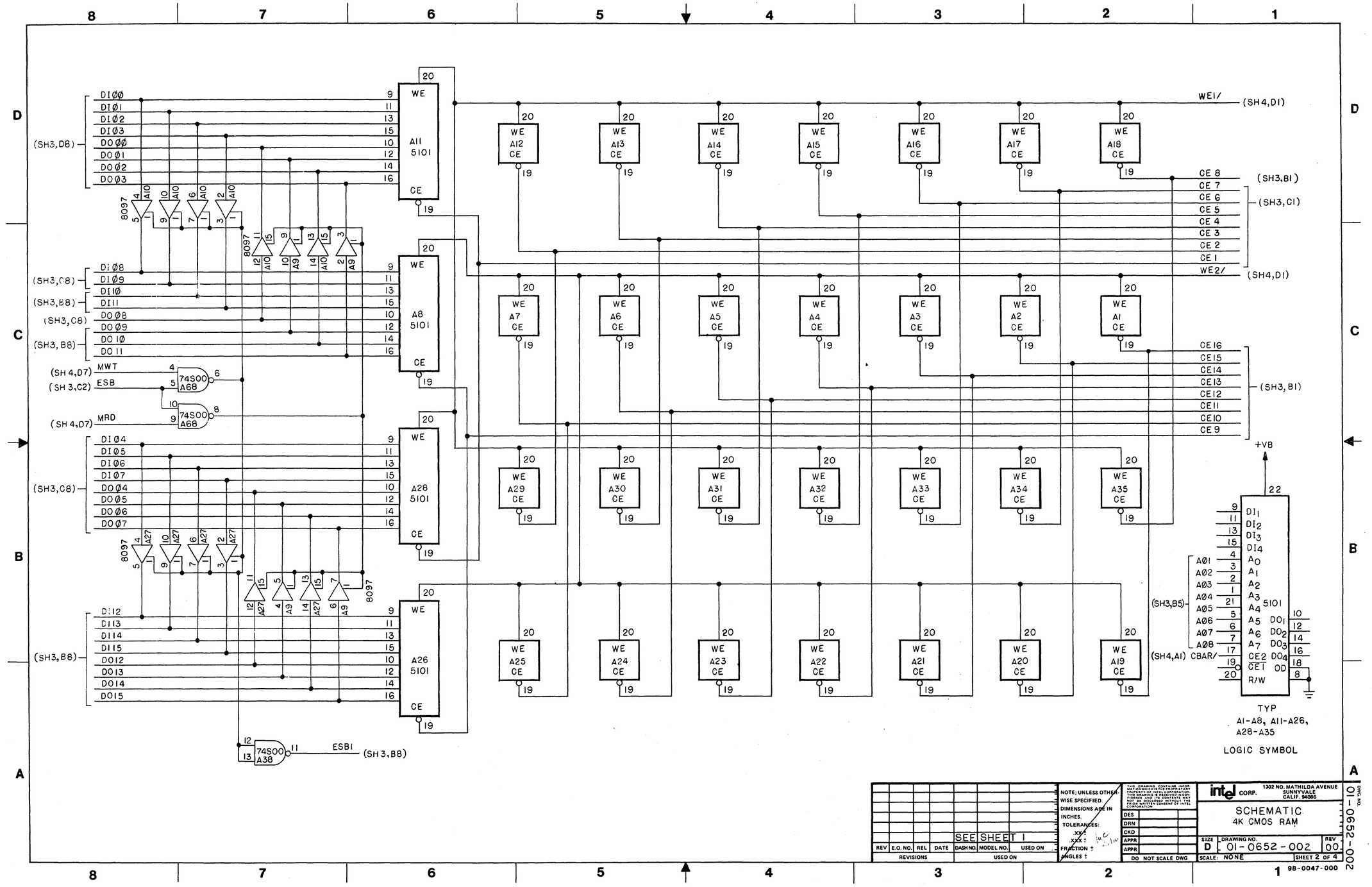

Figure 4-2. SBC 094 Schematic Diagram (Sheet 2 of 4)

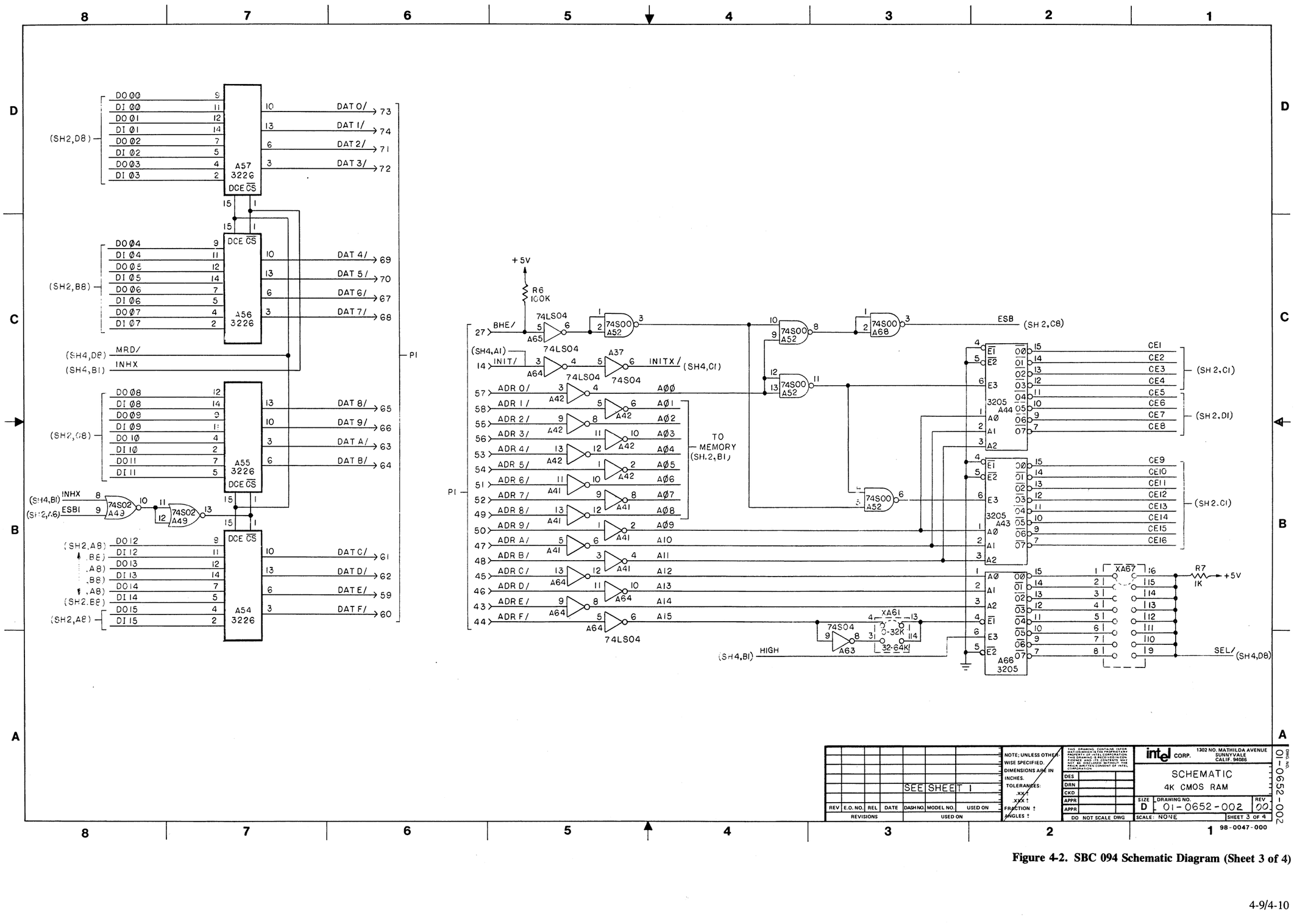

Figure 4-2. SBC 094 Schematic Diagram (Sheet 3 of 4)

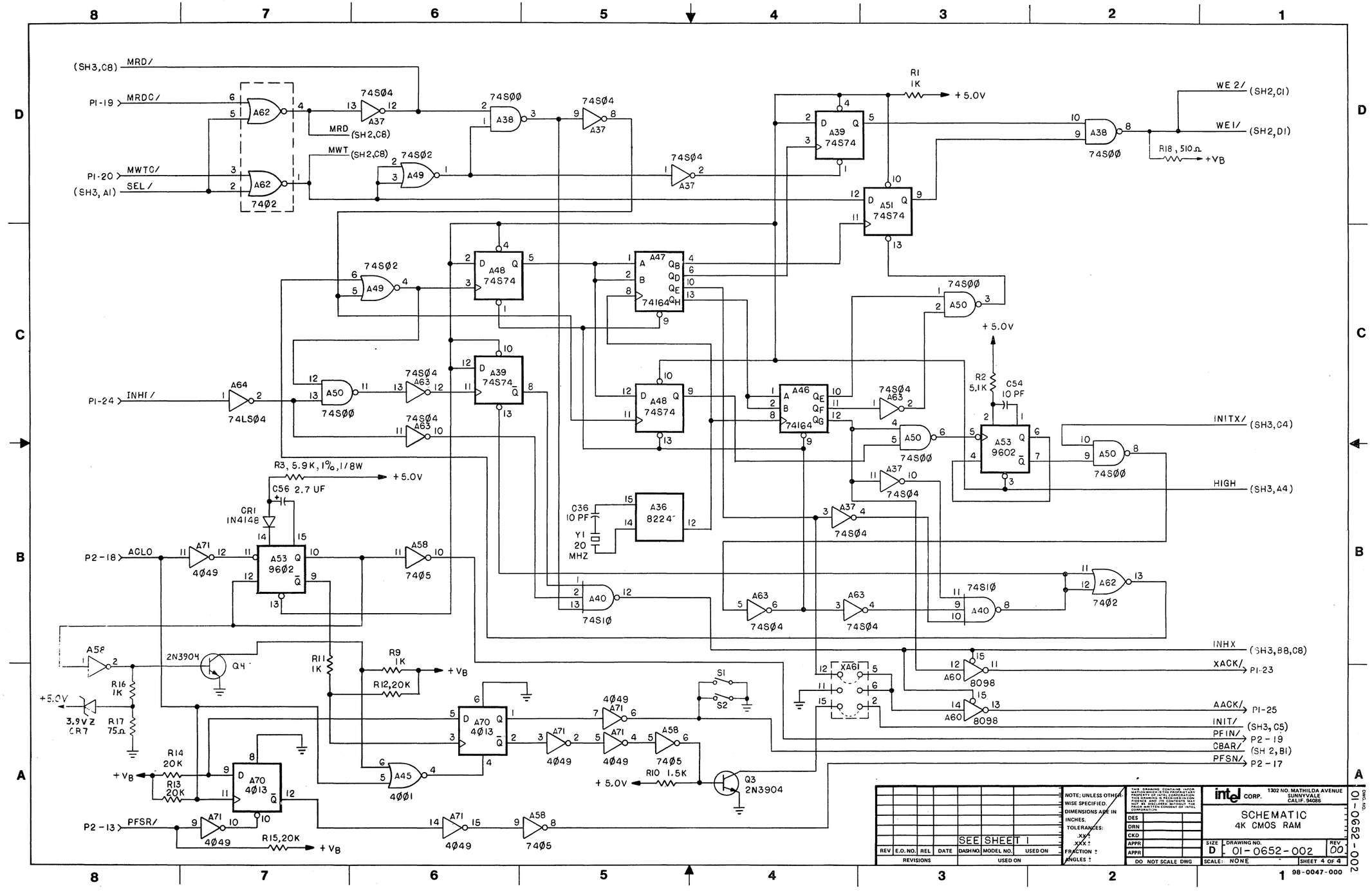

Figure 4-2. SBC 094 Schematic Diagram (Sheet 4 of 4)

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