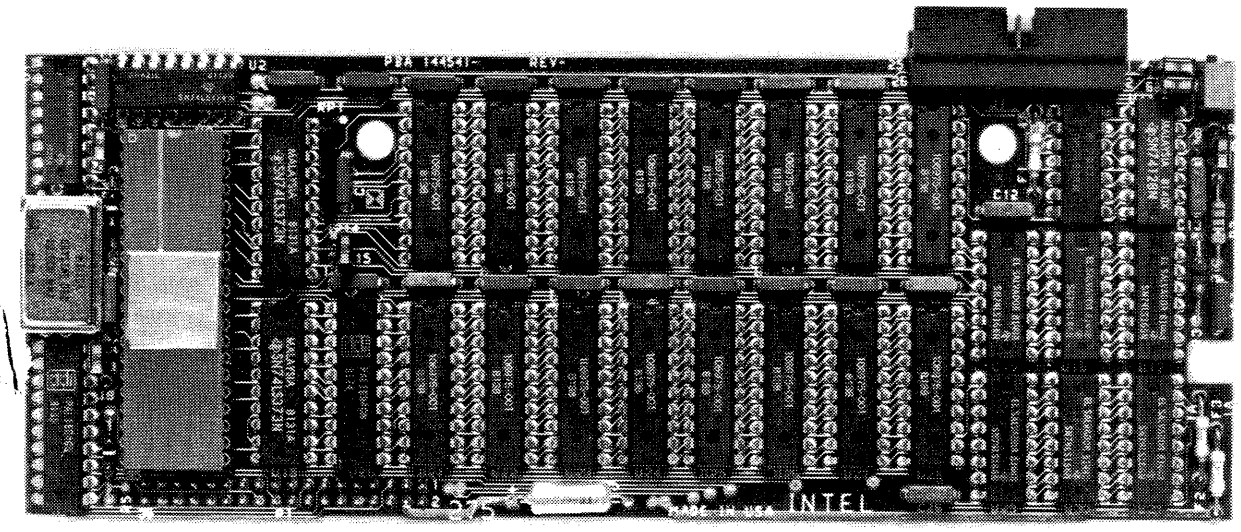
iSBX™ 275 VIDEO GRAPHICS CONTROLLER MULTIMODULE™ BOARD REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 144829-001

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PREFACE

This manual contains descriptive information concerning the iSBX 275 Video Graphics Display Controller Multimodule. It also contains the information necessary to install the iSBX 275 Video Graphics Display Controller Multimodule board onto a host processor board that has an iSBX Bus connector and the programming information required for displaying figures on the user-attached monitor. Appendix A contains a glossary of terms used within this manual. Appendix B contains the hexadecimal code for generating the 8 x 8 ASCII character set.

LIST OF SAFETY PRECAUTIONS

Never attempt to service any sub-assembly within a chassis with the AC power cord connected. Hazardous voltages are present within the chassis with the AC cord connected to a power source.

Damage to some monitors may occur whenever power is applied to the monitor without supplying the sync signals or using the wrong frequency for the sync signals.

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CHAPTER 1. DESCRIPTION

1-1. INTRODUCTION

The iSBX 275 Video Graphics Controller (VGC) Multimodule board is a double-wide Multimodule expansion board, shown in Figure 1-1. It is a graphic/character controller that adds bit-mapped raster-scan graphic drawing and display functions to the Intel line of CPU boards. The iSBX 275 Video Graphics Controller Multimodule board is designed for installation onto any iSBC microcomputer board having an iSBX connector.

The iSBX 275 Video Graphics Controller Multimodule board interfaces between a host microcomputer board and either a black-and-white or a color monitor. When connected to a color monitor, the iSBX 275 VGC board allows selection of up to eight colors each for display and background.

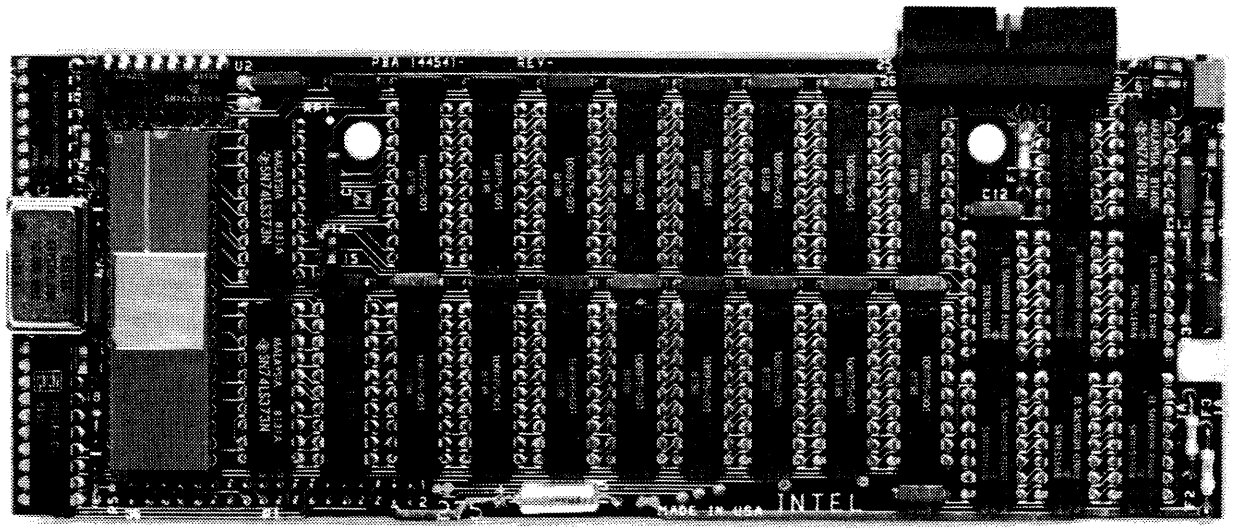


Figure 1-1. iSBX™ 275 Video Graphics Controller Board

1-2. GENERAL DESCRIPTION

The iSBX 275 Video Graphics Controller (VGC) board is designed to work with a general purpose microprocessor in order to implement a computer graphics system.

The iSBX 275 VGC board is attached to the user-selected host processor board via the standard eight-bit iSBX bus (36-pin or 44-pin) connector and is used to generate the basic video signals to the user-attached video display monitor.

The host processor board passes commands and data to the iSBX 275 VGC board via the iSBX bus. The iSBX 275 VGC board, upon receipt of the commands, performs all of the tasks needed to manage the display memory. In addition to the display function, the iSBX 275 VGC board implements high-speed, vector-to-raster scan conversion.

The commands sent to the iSBX 275 VGC board consists of a series of instructions and their associated parameters. These commands and their associated parameters are used to construct a geometric figure or graphic character into the display memory bit-by-bit. This geometric figure or graphic character drawn in the display memory can then be displayed on the monitor. The monitor is a window into the display memory. This window may be panned or scrolled across that image without changing it. The drawing commands which define the elements of the figure include lines, arcs, circles, rectangles, character/symbol painting, and area fills. The commands also allow user-selected line styles and patterns with which to draw and display figures on the monitor.

The host processor (under control of the user's graphic software program) performs the preliminary calculations to prepare the drawing parameters, provides the starting point into the display memory and other associated parameters of the figure to be drawn. The iSBX 275 VGC calculates the display memory addresses bit-by-bit for the graphic figure to be drawn and completes the drawing without further intervention from the host processor.

For example, if a rectangle is to be drawn on the attached monitor, the iSBX 275 VGC board is given a command which defines the type of drawing followed by the starting address and several other parameters that define the length and height of the rectangle. The iSBX 275 VGC board is then given the start drawing command to draw the rectangle. The iSBX 275 VGC board takes the command and draws the figure in the display memory.

1-3. FUNCTIONAL DESCRIPTION

The iSBX 275 Video Graphics Controller (VGC) board consists of five logical blocks as shown in Figure 1-2. These five logic blocks of the iSBX 275 VGC board are as follows:

- Graphic Display Controller
- Control Logic
- Clock Generator
- Display Memory (16K x 16-bit static RAM array)
- Shift Register and Output Buffer

1-4. GRAPHIC DISPLAY CONTROLLER

The heart of the iSBX 275 VGC board is the Intel 82720 Graphic Display Controller (GDC) chip. The Graphics Display Controller (GDC) chip is an intelligent microprocessor peripheral chip designed as a raster-scan computer graphics controller. Control of the GDC by the host microprocessor is achieved via the standard eight-bit bi-directional iSBX bus interface. This bi-directional bus interface allows the host processor to send command and parameter bytes to start the drawing process. The host processor begins the process by retrieving status information from the iSBX 275 VGC board concerning the drawing process. This status information from the iSBX 275 VGC board is readable at any time by the host processor. Access to the GDC is coordinated via flags in the status register.

The First In First Out (FIFO) buffer is integral to the GDC and is the GDC's interface to the iSBX connector through which all commands and data pass. Access to the 16-byte FIFO is controlled by the host processor via the GDC's command set. The host processor coordinates the transfers by checking the appropriate status register bits. Commands and parameter bytes are sent to the GDC's FIFO and are differentiated based on the state of the address bit 0. All commands are written to the GDC. When the write control line is activated, the GDC configures the FIFO as an input buffer to receive the command and the parameter bytes. If a read command is issued to the GDC, the GDC interprets the command, configures the FIFO as an output buffer and places the requested data into the FIFO. The status register indicates that the data is ready to retrieve. The host processor can then retrieve the requested information by activating the read control line.

When the host processor sends a command byte and activates the write control line (IOWR) to the GDC, the GDC interprets the contents written into the FIFO, decodes the command, distributes the succeeding parameter bytes to the proper registers within the GDC, and then initiates the required operation. Any parameter byte following a command is truncated by the receipt of the next command.

The host processor (under control of the user's software) programs the GDC sync logic during initialization with either a reset command or a sync command and the associated parameters. The GDC generates the sync signals (horizontal and vertical) as well as the blanking signals to the CRT monitor for any interlaced or non-interlaced video format.

1-5. CLOCK GENERATOR

The Clock Generator consists of a crystal oscillator and the Clock Programmable Array Logic (PAL) chip. Together, they provide the timing signals used. The iSBX 275 VGC board is supplied with a crystal oscillator, but if you desire, you may replace it with another under the following restraints on frequency. The dot clock may be the oscillator frequency or the frequency divided by two (jumper selectable). The frequency selected must provide a dot clock of at least 4 MHz and less than 13 MHz for a monochrome monitor or 10 MHz for a color monitor due to the external support circuits.

The Clock PAL contains the latch LX and LY which is used for switching of graphics display or monitor power. These two signals (LY and LX) are provided for CRT control on systems which use the same CRT as both a graphics and a data terminal. Upon power up, signal LX is set low and signal LY is set high to give control of the CRT to the data terminal controller. Control of the CRT is passed to the iSBX 275 VGC board simply by executing a write command (data is ignored) to any odd I/O address within the range of MCS1/ of the iSBX bus which sets LX high and LY low. See Table 3-1 for addresses. A write to any even address in the same range will return LY and LX to their original power up states, returning control of the CRT to the data terminal controller. Refer to Optional Circuits in Chapter 2 for an example of an external circuit which may be used to implement this feature. These two signals may also be used to turn on the monitor after sync initialization.

The clock PAL (A19) decodes the control lines IORD/, IOWR/, and MCS0/ sent by the host processor, and in turn, generates RD or WR to the GDC. The iSBX 275 VGC board does not support DMA transfers.

1-6. CONTROL LOGIC

The control logic consists of the Control PAL which aids the GDC in controlling access to the display memory. There are two types of accesses to the display memory; Display cycles and Read-Modify-Write (RMW) cycles. During display cycles, the data at the addressed location is read and sent to the shift register for subsequent display on the monitor. During a RMW cycle, data is accessed from display memory, modified, and written back into the display memory. The modifications done to the data at the addressed location are: complement, set, clear, or replace.

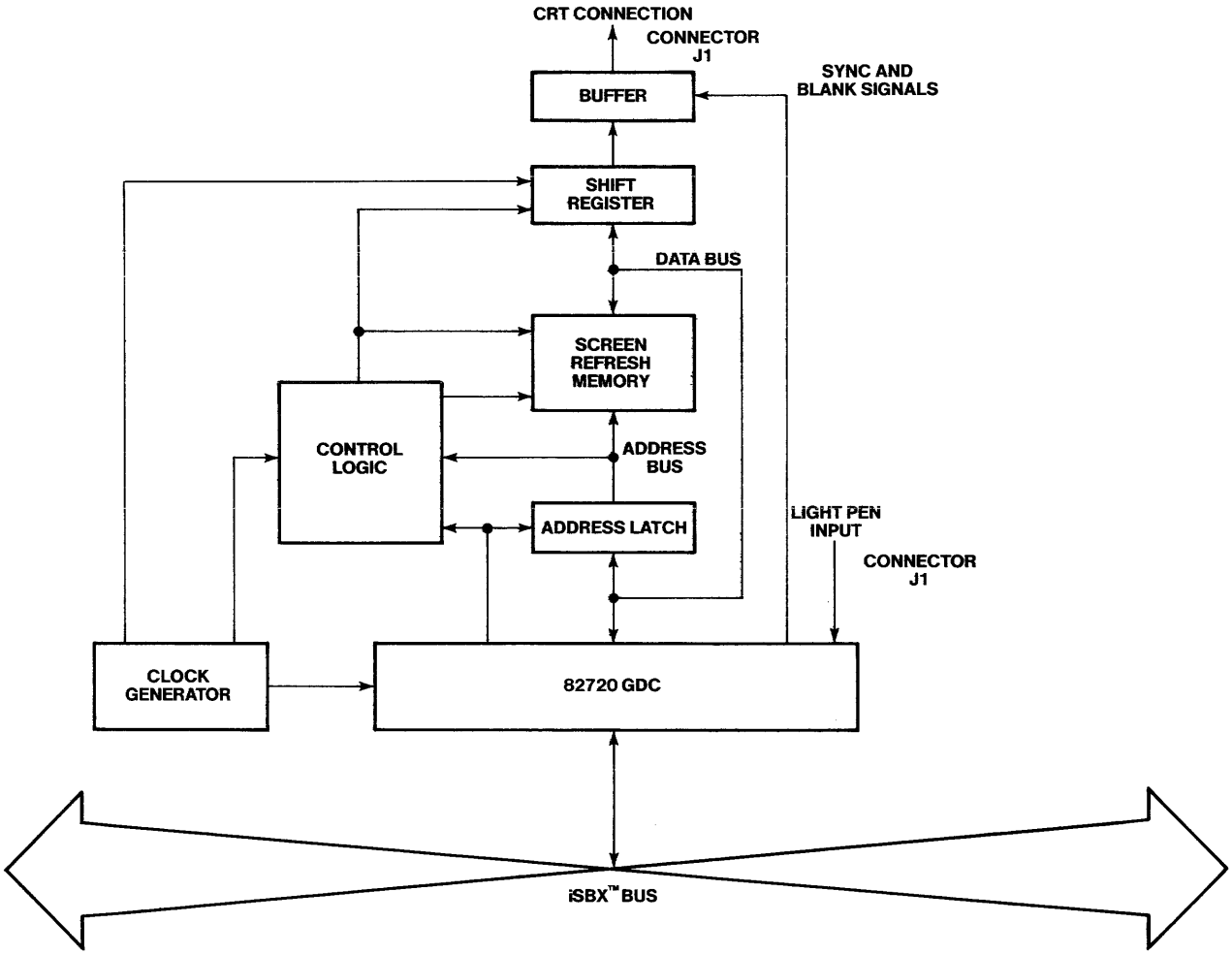


Figure 1-2. Functional Block Diagram

1-7. DISPLAY MEMORY

The display memory consists of sixteen 16K x 1 static RAMs which provide 256K bits of memory arranged as 16K sixteen-bit words. The address of the display memory access is calculated by the GDC and latched in the address latch. The data stored at the addressed location may be modified by the GDC, passed back to the host processor, or displayed on the attached monitor. When using a black-and-white monitor interface, all of the display memory are accessible. When using a color monitor interface, one block (1/4) of the display memory is available for each color (or 3/4 of the total memory).

When the data stored at the addressed RAM location is to be displayed, the data is parallel loaded into the shift register.

1-8. SHIFT REGISTER AND BUFFER LOGIC

The Shift Register logic consists of three 16-bit registers (one for each color) and a series of D flip-flops. Each shift register performs the parallel-to-serial conversion that produces the video bit stream sent to the attached monitor. Additional D-type flip-flops are used to resynchronize the video data with the synchronizing signals and blanking signals out to the connector. In the black and white mode, only one shift register is used.

1-9. EQUIPMENT SUPPLIED

The following hardware is supplied to attach the iSBX 275 VGC board to an iSBC host processor board:

Three nylon spacers
Six nylon screws

The schematic diagram is also supplied with the iSBX 275 VGC board for reference only.

1-10. COMPATIBLE EQUIPMENT

The iSBX 275 VGC Multimodule board can be used with any board supporting the iSBX Bus structure.

Signals from the iSBX 275 VGC board are accessible to the video terminal by means of the interface connector J1 and the user-fabricated cable.

1-11. SPECIFICATIONS

Specifications for the iSBX 275 VGC board are listed in Table 1-1.

Table 1-1. Specifications

PHYSICAL CHARACTERISTICS:	
Width:	7.82 cm (3.08 inches)
Length:	19.05 cm (7.50 inches)
Height:	2.05 cm (0.80 inches) iSBX 275 VGC board only 2.90 cm (1.14 inches) iSBC board plus the iSBX 275 VGC board
Weight:	127 gm (4.5 oz.)
ENVIRONMENTAL CHARACTERISTICS:	
Operating Temperature:	0° to 55°C (32° to 131°F)
Relative Humidity:	To 95% without condensation
POWER REQUIREMENTS:	
Vcc = +5 ± 5% at 1.5 AMP	

***

CHAPTER 2. PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBX 275 Video Graphic Controller (VGC) board onto an Intel Single Board Computer with an iSBX Bus connector. These instructions include unpacking and inspection, installation considerations such as physical dimensions, power requirements, cooling and mounting requirements, optional design considerations, jumper configurations, connector pin assignments and an installation procedure.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt of the equipment for evidence of mishandling during transit. If the shipping carton is severly damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Marketing Administation to obtain a return authorization number and further instructions (see chapter 4). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2-3. PREPARATION FOR INSTALLATION

The iSBX 275 VGC board is designed to mount onto any board that supports the iSBX Bus interface. Installation considerations such as power, cooling, mounting and physical size requirements are outlined in the following paragraphs.

2-4. POWER REQUIREMENTS

The iSBX 275 VGC board requires +5V ($\pm$0.25V) at 1.5A maximum for operation. In addition, $\pm$12.0V are routed through the board but not used. All three voltages are routed through 1 AMP fuses to the video connector J1. These voltages are supplied to the iSBX 275 VGC board from the host microcomputer board via the iSBX Bus connector. Total the power requirements of the iSBX 275 VGC board and the other system components. Ensure that the power supply is capable of supplying the additional power requirements for the iSBX 275 VGC board.

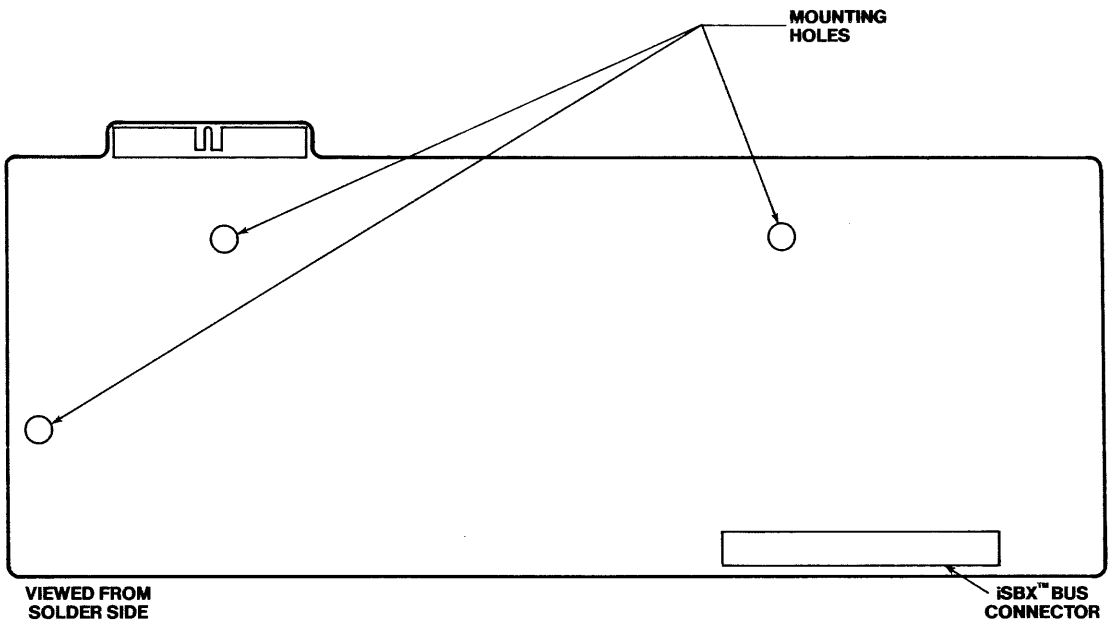
2-5. COOLING REQUIREMENTS

The iSBX 275 VGC board dissipates approximately 112 gram calories/minute (0.454 BTU/minute) and adequate circulation of air must be provided to prevent the ambient temperature from exceeding 55°C (131°F). The iSBC system enclosures include fans to provide adequate intake and exhaust of ventilating air.

2-6. MOUNTING REQUIREMENTS

Figure 2-1 shows the iSBX bus connector and standoff locations of the iSBX 275 VGC board. The Multimodule board mounts onto any iSBC microcomputer containing an iSBX connector and the required standoff holes. The mounting hardware supplied as part of the Multimodule board includes:

1. 6 nylon screws, 1/4-inch x 6/32
2. 3 nylon standoffs, 1/2-inch x 6/32



Viewed from bottom

1108

Figure 2-1. Connector and Standoff Locations

NOTE

The Multimodule board, when installed onto a host microcomputer iSBC board, may intrude on the adjoining card slot adjacent to the component side of the host microcomputer in some iSBC cardcages.

2-/. PHYSICAL DIMENSIONS

Figure 2-2 shows the physical dimensions and Figure 2-3 shows the clearances for an iSBX 275 VGC board mounted on a host iSBC microcomputer board. The dimensions shown in Figure 2-3 are maximum heights.

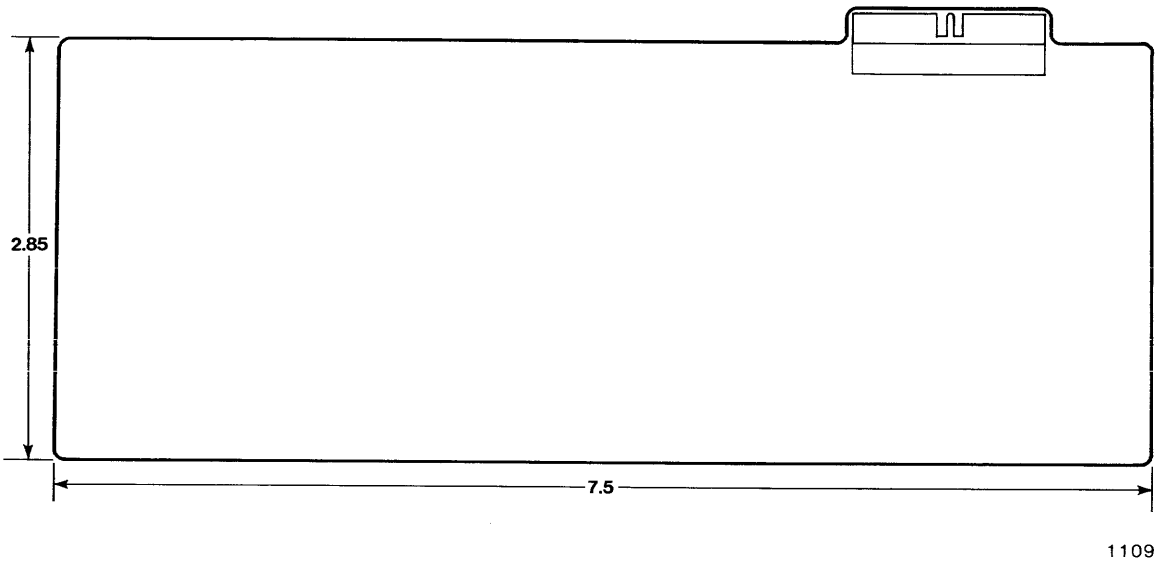


Figure 2-2. Board Dimensions (Inches)

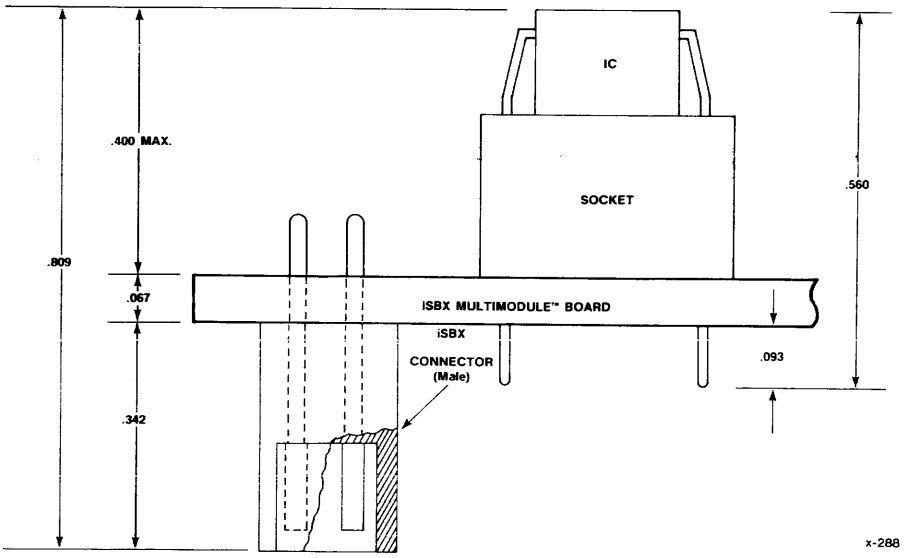


Figure 2-3. Mounting Clearances (Inches)

2-8. SYSTEM CONSIDERATIONS

Before installing your iSBX 275 VGC board into your graphic system, there are several options you need to consider. The first consideration is the selection of the type of video monitor you want to attach to your graphic system. Once that decision is made, you need to consider the jumper options on the iSBX 275 VGC board to make. You also may want to consider adding external optional circuits to your graphic system. The following sections are provided to help you select your options.

2-9. MONITOR SELECTION

Table 2-1 lists those monitor manufacturers whose specifications have been reviewed by Intel for compatibility with the iSBX 275 VGC board. This information is for reference only and does not constitute an endorsement by Intel Corporation. Refer to the manufacturer's documentation for specific details for the synchronization requirements, dc drive capability, etc.

Table 2-1. CRT Monitors

CRT TYPE	MANUFACTURER
Black and White	MOTOROLA M3570
Black and White	BALL BROTHERS TTL 120
Color	BALL BROTHERS 7 - 015 -0131
Color	INDUSTRIAL DATA TERMINALS 19AC
Color	CONRAC 5711C13
Color	Mitsubishi C - 3419
Color	NEC 1202DH

2-10. HARDWARE OPTIONS

The iSBX 275 board has several operating modes which are selectable by hardware jumpers and software programming. This section deals with the hardware jumper options. Table 2-2 is a numerical listing of all the jumpers on the iSBX 275 VGC board with a short description of each jumper. Refer to Chapter 3 for programming options and information.

Table 2-2. Jumper Configuration

Jumper Number	Function
E1 to E2	This is used for testing purposes only.
E3 to E4	This jumper routes the active high vertical sync (VSYNC) signal to the attached monitor.
E4 to E5	This jumper routes an active low vertical sync (VSYNC/) signal to the attached monitor.
E6 to E7	This jumper provides an external contrast adjustment (R1) to the attached black and white monitor.
E8 to E10	This jumper routes combined sync (CSYNC/) to the attached monitor.
E9 to E10	This jumper routes an active low horizontal sync (HSYNC/) signal to the attached monitor.
E11 to E10	This jumper routes an active high horizontal sync (HSYNC) signal to the attached monitor.
E12 to E13	This jumper selects the color mode for the Control circuitry. It should be removed for B/W mode.
E14 to E15	This is used for testing purposes only.
E16 to E17	This is used to select the non-divided clock.
E17 to E18	This jumper selects the divide-by-two mode for the CLOCK circuitry. It is typically used for color mode.

2-11. CLOCK FREQUENCY SELECTION

The video dot clock is supplied by a socketed TTL crystal oscillator module. The factory default is a 12.6 MHz clock, but the user may replace this crystal oscillator with any value up to 16 MHz to provide a maximum dot clock rate of 10 MHz for color monitors and 13 MHz for black and white monitors. Consult Chapter 3 for information on the relationship between the dot rate, the horizontal scan rate, and the vertical frame rate.

In addition to changing the oscillator frequency, there is a jumper option that allows the clock signal from the oscillator to be divided by two. This allows the iSBX 275 VGC board to interface to either a black and white monitor or a color monitor with the same basic frequency. Typically, black and white monitors use a non-divided clock; while color monitors use a clock that is divided by two because the color resolution is less; thus, a slower dot clock. Table 2-3 lists the optional jumpers, their numbers, and their respective functions.

2-12. MODE SELECTION

The two modes of operation for the Control PAL (black and white or color) are selected by jumper E12 to E13. The iSBX 275 VGC board is shipped from the factory without jumper E12 to E13 (for use with black and white monitors). If a color monitor is used, jumper E12 to E13 must be installed.

2-13. VIDEO OUTPUT SIGNALS

The iSBX 275 VGC board is shipped from the factory with jumper E6 to E7 installed to enable interfacing a black and white monitor which requires an external contrast adjustment. If an external contrast adjustment is required for the black and white monitor type being used, jumper E6 to E7 routes the variable contrast video signal (A VIDEO) as an output. The contrast adjustment (R1) is provided on the iSBX 275 VGC board.

If G Video is used and this adjustment is not required (if the black and white monitor has its own contrast adjustment or if the color mode is used), jumper E6 to E7 should be removed to avoid loading the output driver.

2-14. Horizontal Sync

Horizontal sync is normally active high with jumper E10 to E11 installed (factory default). It may be inverted to an active low by removing jumper E10 to E11 and installing jumper E9 to E10. An active low combined sync signal CSYNC/ (VSYNC NORed with HSYNC), may be obtained by adding jumper E8 to E10. This jumper is typically used for color monitors. Refer to the vendor manual for your monitor type to determine these requirements. Then, refer to Table 2-3 for the optional jumper configurations.

2-15. Vertical Sync

The vertical sync (VSYNC/) signal is normally active low with jumper E5 to E4. It may be inverted to an active high by removing jumper E4 to E5 and installing jumper E3 to E4. Refer to Table 2-3 for optional jumper configurations.

Table 2-3. Optional Jumper Configurations

Default Jumper	Default Function	Remove Jumper	Install Jumper	Optional Function
E10 - E11	HSYNC	E10 - E11 E10 - E11	E8-E10 E9 - E10	CSYNC/ HSYNC/
E4 - E5	VSYNC/	E4 - E5	E3 - E4	VSYNC
E16 -E17	Non-divide by 2	E16 - E17	E18 - E17	Divide by 2
	Black & white		E12 - E13	Color mode
E6 - E7	A Video contrast adjustment for attached monitor	E6 - E7		G video

2-16. OPTIONAL DESIGN CONSIDERATIONS

Two optional circuit designs that you may want to consider adding to your microcomputer graphic system are: a composite sync circuit and a monitor multiplexer circuit.

A sample of a composite video circuit is shown in Figure 2-4. Figure 2-5 shows a sample of a multiplexer circuit to enable the use of one monitor with two controllers.

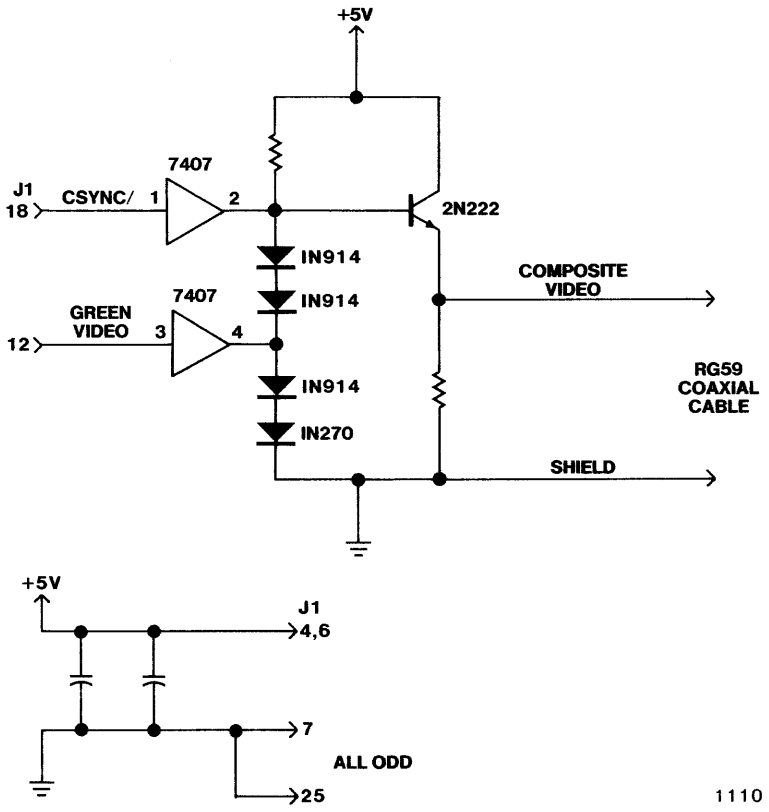


Figure 2-4. Sample Design of Black and White Composite Sync Circuit

2-17. iSBX™ BUS INTERFACE CONNECTOR

Connector P1 is the standard eight-bit iSBX Bus connector which interfaces all data and control signals between the host iSBC microcomputer board and the iSBX 275 VGC board. There must be 32 dot clock pulses between the leading edges of the commands. Much of this time is taken up by the CPU overhead. Refer to the iSBX Bus Specification if additional information is needed.

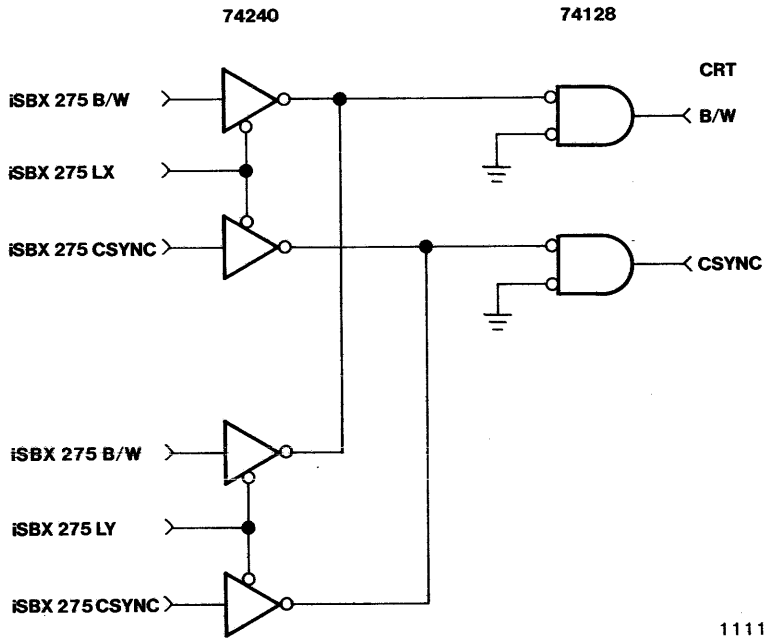


Figure 2-5. Sample Design of a Multiplexer Circuit

2-18. SYSTEM INSTALLATION PROCEDURE

The following is the recommended procedure for preparing the iSBX 275 Video Graphic Controller (VGC) board for installation into your chassis. The jumper configuration section of this chapter provides the necessary information for the jumper options and the instructions for making the desired jumper changes.

The iSBX 275 VGC board mounts onto the host iSBC board (having a Multimodule connector) as follows:

1. Disconnect system power. Power down the system chassis and any attached peripherals. Disconnect the system power cord from the ac source.

CAUTION

Remove power from the system before inserting or removing iSBC or iSBX boards into/from a cardcage. Failure to do so could result in damage to the boards.

Do not remove or install board cables with power applied. Removing or installing cables with power supplied may cause damage to the boards.

2. Gain access to the cardcage. Refer to the applicable chassis or card cage hardware reference manual for the procedures on adding new boards to the system. Perform the required procedure to gain access to the card cage and remove the host processor board from the card cage.

3. Install the iSBX 275 VGC board onto the host processor board in accordance with the Multimodule board installation procedure contained in paragraph 2-19.

4. Fabricate the CRT Interface cable in accordance with the CRT interface cable fabrication procedure contained in paragraph 2-21.

5. Complete system assembly. Refer to the applicable chassis or card cage hardware reference manual. Perform the required procedure to route any cables exiting the chassis and complete the system assembly.

CAUTION

Do not turn on ac power to the monitor without first initializing the GDC. Failure to comply may damage the monitor.

6. Restore ac power and check for proper system operation.

2-19. MULTIMODULE™ BOARD INSTALLATION PROCEDURE

1. Configure the iSBX 275 VGC board by making the necessary jumper changes to suit your specific application.

2. With the nylon 1/4-inch x 6/32 screws, secure the 1/2-inch plastic spacers (3) to the host iSBC board as shown in Figure 2-6.

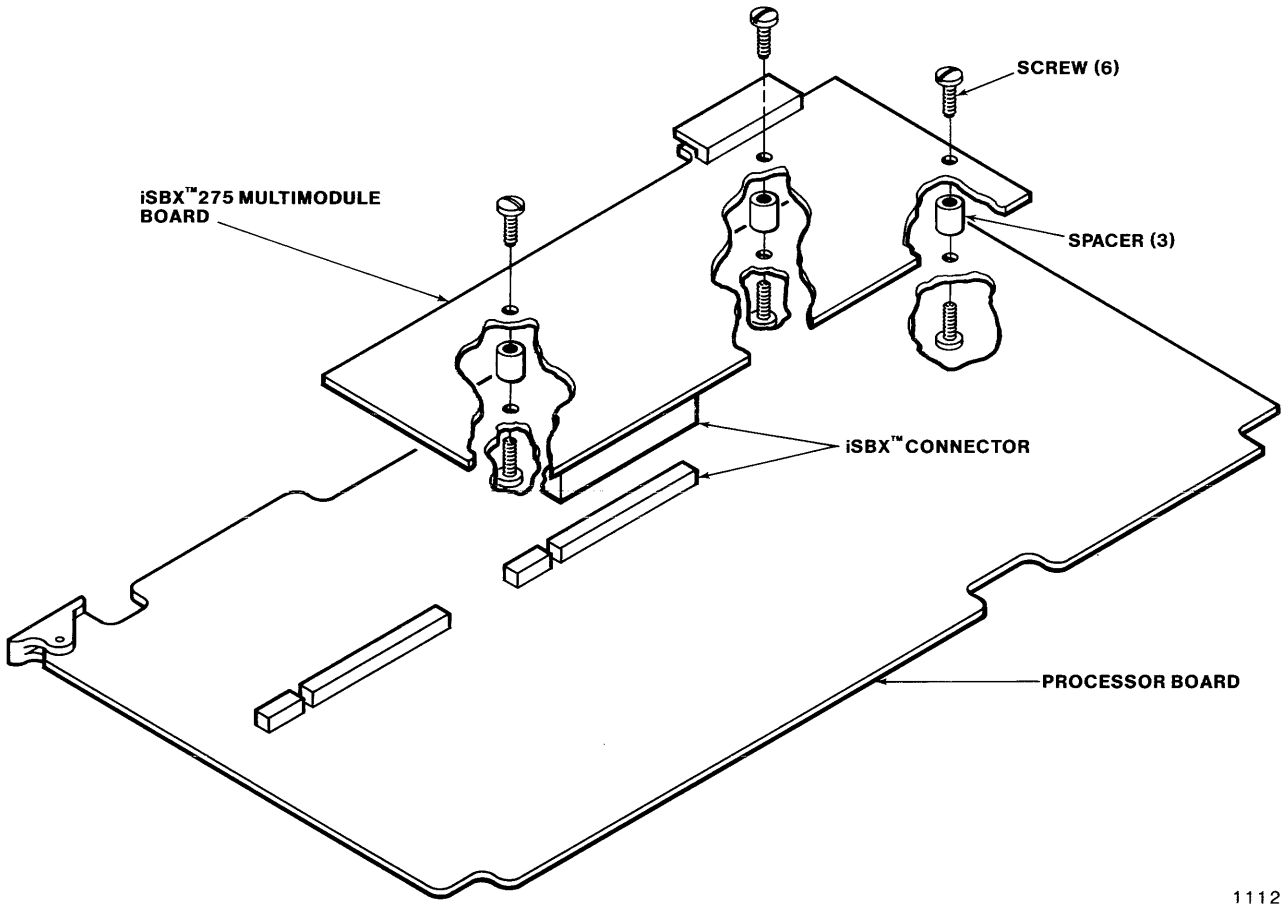


Figure 2-6. Installation of the iSBX™ 275 VGC board

3. Locate the center iSBX bus connector on the host iSBC board and align it the iSBX bus connector of the iSBX 275 VGC board.

4. Align the iSBX 275 VGC board mounting holes with the spacers on the host iSBC board.

5. Gently press the two boards together until the connector seats.

6. Secure the Multimodule board to the top of the spacers with the three 6/32 nylon screws.

2-20. CRT INTERFACE

Connector J1 is a 26-pin connector used to interface your selected CRT monitor. It is recommended that keyed connectors be used to ensure proper cable installation. Table 2-4 lists some part numbers and vendors of compatible connectors which mate with connector J1 on the iSBX 275 VGC board. The signals for each pin of the J1 connector are listed in Table 2-5 and the descriptions of the signal functions are listed in Table 2-6. Table 2-7 list the dc characteristics and Table 2-8 lists the ac characteristics.

Table 2-4. J1 Compatible Connector

VENDOR	Part Number	Connector Type	Pins
BERG	65043	Wire type	13/26
BERG	65846-819	Wire type (keyed)	13/26
BERG	65485-011	Flat cable	13/26
BERG	65847-027	Flat cable (keyed)	13/26
3M	3399	Flat cable	13/26

Table 2-5. Connector J1 Pin Assignments

Pin Number	Name	Function
1	DOT CLK/	Active low - Dot clock
10	A Video	Adjustable video for B/W monitors
12	G Video	Green Video for Color or video for B/W
14	B Video	Blue Video for color monitors
16	R Video	Red Video for color monitors
18	HSYNC	Active high - horizontal sync
20	LY	CRT Multiplexer control signal-(Reset high)
22	LPEN	Rising edge-triggered light pen input
24	VSYNC/	Active low - vertical sync
26	LX	CRT Multiplexer control signal-(Reset low)
All odd pins 7 through 25 are grounded. Pins not listed are reserved.		

Table 2-6. CRT Interface Signal Definitions

Signal	Function
Dot Clk:	Dot Shift Clock - clock signal to video output for test purposes.
A Video:	Adjustable Video - this is the adjustable-contrast video fed to most B&W monitors. The output signal is developed across a 500 ohm trim pot.
G Video:	Green Video - a TTL Signal capable of driving a 75 ohm line. This is the Green Video gun driver signal. This signal may also be used for black and white video. (See Table 2-3)
R Video:	Red Video - a TTL signal capable of driving a 75 ohm line. This is the Red Video gun driver signal.
B Video:	Blue Video - a TTL signal capable of driving a 75 ohm line. This is the Blue Video gun driver signal.
VSYNC/:	Vertical Sync - an active-low TTL signal indicating vertical retrace. This signal may optionally be inverted to active-high. (See Table 2-3)
HSYNC:	Horizontal Sync - an active high TTL signal that indicates horizontal retrace. (See Table 2-3) Options allow Combined Sync - an active-low TTL Signal capable of driving a 75 ohm line that indicates a combined sync (CSYNC/ = HSYNC/ AND VSYNC/) for use on RGB monitors or a composite video combiner.
LPEN:	Light Pen - a rising edge triggered TTL input signal which informs the GDC that a light pulse has been detected.
LX, LY:	CRT Multiplexer Control - These signals control a CRT shared with a Data Terminal Controller. On reset LX is low and LY is high.

Table 2-7. CRT Interface Signal DC Characteristics

Signal	Parameter Note	Min	Max	Unit	
R, G, B Video, CCYNC/	Output Low Voltage		0.5	V	IOL = 48mA
	Output High Voltage	2.4		V	IOH = -2.4mA
	Output High Voltage	2.0			IOH = -42.4mA
VSYNC	Output Low Voltage		0.5	V	IOL = 14.4mA
	Output High Voltage	2.4		V	IOH = -.75mA
A Video	Output High Voltage*	0	3.0	V	RL = 120 ohm
HSYNC	Output Low Voltage		0.5	V	IOL = 16.4mA
	Output High Voltage	2.4		V	IOH = -.91mA
Dot Clock, VSYNC/, HSYNC/	Output Low Voltage		0.5	V	IOL = 20mA
	Output High Voltage	2.4		V	IOH = -1mA
LPEN	Input Low Voltage		0.8		IIL = 485uA
	Input High Voltage	2.0			IIH = 10uA
LY, LX	Output Low Voltage		0.5	V	IOL = 24mA
	Output High Voltage	2.4		V	IOH = -3.2mA

*The high-level output voltage is adjustable over the range shown with the 500 ohm Contrast trim pot.

Table 2-8. CRT Interface AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
t_1	Dot Pulse Width	100		ns	(Divided Mode)
		77		ns	(Non-divided mode
t_2	Horiz Sync Width	(Determined by the Initialization commands)			
t_3	Vert Sync Width	(Determined by the Initialization commands)			

2-21. CABLE FABRICATION

The fabrication of the CRT monitor interface cable depends on the type of monitor selected. If the monitor selected is a black and white, fabricate your CRT Interface cable in accordance with paragraph 2-22. If the monitor selected is a color monitor, fabricate your CRT Interface cable in accordance with the paragraph 2-23.

2-22. INTERFACING BLACK AND WHITE MONITORS

When interfacing a black and white monitor that is compatible with those listed in Table 2-1 to the iSBX 275 VGC board, use the 10-pin edge connector Cinch 251-10-90-160 or equivalent. Table 2-9 lists the pin assignments.

Table 2-9. Black and White Monitor Pin Assignments

iSBX 275 Connector	CRT Connector	Function	iSBX 275 Connector	CRT Connector	Function
1		Reserved	2		-12V
3		Reserved	4		+5V
5		Reserved	6		+5V
7		Ground	8		+12V
9	1	Ground	10	8	A Video
11		Ground	12		G Video
13		Ground	14		B Video
15		Ground	16		R Video
17	5	Ground	18	6	HSYNC
19		Ground	20		LY
21		Ground	22		
23	10	Ground	24	9	VSYNC
25		Ground	26		LX

Use twisted pair wire between ground and pins 8, 6 9. For some monitors, external dc power must be supplied to pins 1 and 7 of the monitor. External brightness control is optional (user-supplied and installed on CRT connectors pins 2, 3, and 4). See the applicable CRT manual for details.

2-23. INTERFACING COLOR MONITORS

When fabricating a cable to interface most color monitors to the iSBX 275 VGC board, use Coax BNC connectors. Table 2-10 lists the pin assignments. When using the NEC Model 1202DH Color Monitor, use Table 2-11 to obtain the proper pin assignments for fabricating the interface cable.

Table 2-10. Color Monitor Pin Assignments

iSBX 275 Connector J1	Function	iSBX 275 Connector J1	Function
12	G Video	14	B Video
16	R Video	18	CSYNC/
Use 75 ohm coax for all connections.			

Table 2-11. NEC Monitor Cable Fabrication Data

iSBX 275 Connector Pin	CRT Connector Pin	Function
11	1	Ground
12	3*	G Video
13	5	Ground
14	4*	B Video
15	6	Ground
16	2*	R Video
18	7 and 8	CSYNC/
* Use a 75 ohm, 1/4 Watt resistor from the indicated pin to ground for termination.		

***

CHAPTER 3. PROGRAMMING INFORMATION

3-1. INTRODUCTION

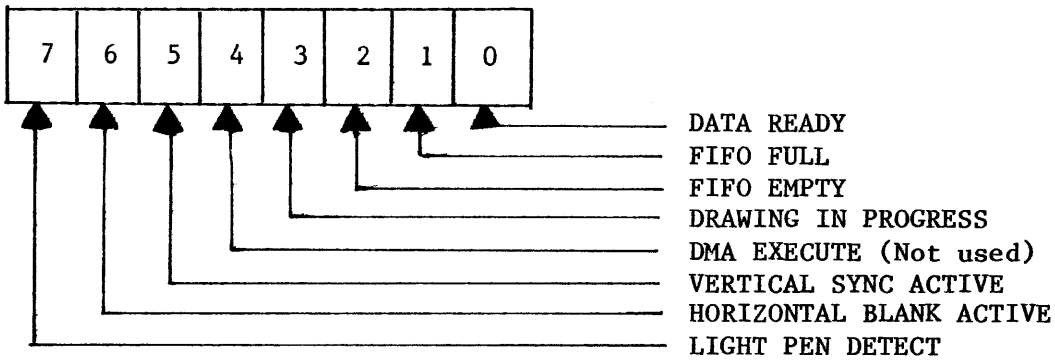
This chapter provides programming information for the iSBX 275 Video Graphics Controller (VGC) board. All on-board functions are controlled by the Graphics Display Controller (GDC) chip.

3-2. ADDRESSING

The iSBX 275 VGC board is accessed in the I/O space of the host processor board using read and write commands. Consult the hardware reference manual for the host processor board to find the address associated with the iSBX bus connector used to mount the iSBX 275 VGC board. Table 3-1 gives the addresses of the Command, Status, and Data ports used by the iSBX 275 VGC board. Before data or commands are written from the host processor board to the iSBX 275 VGC board, the host processor should check the status register to ensure that the command/data FIFO is not full. Figure 3-1 defines each bit of the Status Register.

Table 3-1. I/O Port Address Locations

8 Bit Hostboard	16-Bit Hostboard	READ (IN) TO CPU	WRITE (OUT) FROM CPU
X0, X2 X4, or X6	X0, X4, X8, or XC	status	Data, (Parameters)
X1, X3, X5, or X7	X2, X6, XA, or XE	Data	Command
X8, XA, XC, XE	Y0, Y4,Y8, YC		CRT Multiplexer LX=HIGH, LY=LOW
X9, XB, XD, XF	Y2, Y6, YA, YE		CRT Multiplexer LX=HIGH, LY=LOW
X,Y = any hexadecimal digit, set by the host processor board decoding logic.			



Light Pen Detect. When this bit is set to 1, the light pen address (LAD) register contains a value (word address) that the system microprocessor can read. This flag is reset after the three bytes of Light Pen Address (LAD) is moved into the FIFO in response to the light pen read command.

Horizontal Blank Active. A value of 1 for this flag signifies that horizontal retrace blanking is currently underway.

Vertical Sync Active. This flag is a 1 during vertical retrace. The vertical sync flag coordinates display-format-modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

DMA Execute. This bit is a 0 since DMA is not supported.

Drawing in Progress. This status flag is set to a 1 while the GDC is drawing a graphics figure.

FIFO Empty. This flag and the FIFO full flag coordinate system microprocessor accesses with the GDC's FIFO. When it contains a 1, the empty flag ensures that all the commands and parameters previously sent to the GDC have been processed.

FIFO Full. When this flag is contains a 1, it indicates a full FIFO in the GDC. A value of 0 ensures that there is room for at least one more byte. This flag must be checked before each write into the GDC.

Data Ready. When this flag is set to 1, it indicates that a byte is available to be read by the microprocessor. The data-ready bit must be tested before each read operation by the system microprocessor. The flag is reset after the data is transferred from the FIFO into the microprocessor.

Figure 3-1. Status Register Bit Definition

3-3. INTERRUPTS

The iSBX 275 VGC board provides one interrupt (MINTR0) which is active (high) during vertical sync time. This allows the synchronization of the display update with the vertical blanking period and provides a field-rate time tick.

3-4. DISPLAY MEMORY ORGANIZATION

The on-board bit-map display memory consists of 16K words of 16 bits each beginning at address 0 relative to the Graphics Display Controller (GDC) chip. This memory is read out 16 bits at a time by the GDC and displayed on the screen starting at the top, left corner of the screen and sequences down toward the bottom right corner of the screen. Because the display is read a word at a time, the display resolution in the horizontal direction must always be an even multiple of 16. The least significant bit of the word is displayed first. The GDC chip has a total of 18 address bits, but the iSBX 275 VGC board uses the 14 least significant bits. The additional upper bits are ignored, but should be set to zero to avoid complicated memory address calculations and to ensure software compatibility with future products.

While in black and white mode, all 16K words of the display memory are in a contiguous block which may be written to and displayed. A value of 1 written into the bit map is displayed as an illuminated dot.

When in the color mode, three color planes exist sequentially in memory for purposes of writing, but are displayed simultaneously. The planes are each 4K words long and are in the order of Red, Blue, and Green. The Red plane starts at memory address 0; the Blue plane starts at memory address 1000H; and the Green plane at memory address 2000H. A value of 1 written into a given plane illuminates that color dot. Table 3-2 lists the color plane combinations for the various colors. If a figure is to be drawn in a color that is composed of two or more primary colors, the GDC chip must be instructed to draw the figure separately for each color plane. This is done by changing the cursor base address and repeating the drawing command and parameters.

Table 3-2. Color Plane Combinations

COLOR PLANE GREEN	BLUE	RED	DISPLAYED COLOR
0	0	0	BLACK
0	0	1	RED
0	1	0	BLUE
0	1	1	MAGENTA
1	0	0	GREEN
1	0	1	YELLOW
1	1	0	CYAN
1	1	1	WHITE

3-5. COMMAND SUMMARY

The following is a summary of all the commands available with the iSBX 275 VGC board. These commands are organized into four categories: Video Control commands, Display Control commands, Drawing Control commands, and Data Read commands and are described in subsequent paragraphs.

RESET COMMAND	Resets the GDC to its idle state.
VSYNC	Specifies the video display format.
SYNC	Specifies the cursor and character row heights.
PITCH	Specifies the width of the horizontal dimension of display memory.
ZOOM	Specifies the zoom factors for graphics character writing.
PRAM	Defines the starting addresses and lengths of the display areas and specifies the eight bytes for the graphic character.
CURS	Sets the position of the cursor in display memory.
START	Ends the idle mode and unblanks the display.
BCTRL	Controls the blanking and unblanking of the display.
MASK	Sets the mask register contents.
FIGS	Specifies the parameters for the drawing processor.
FIGD	Draws the figure specified into the display memory.
GCHRD	Draws the graphics character into the display memory.
WDAT	Writes data words or bytes into the display memory.
RDAT	Reads data words or bytes from the display memory.
CURD	Reads the cursor position.
LPRD	Reads the light pen address.

3-6. VIDEO CONTROL COMMANDS

The Video Control commands are used to initialize the iSBX 275 VGC board after a power up sequence. Normally, these commands do not need to be repeated after being executed once; however, executing these commands puts the GDC in a known state. The commands are listed in the sequence in which they are normally executed.

3-7. RESET Command (00H). The Reset command (Figure 3-2) is used to initialize the operation and display modes of the GDC. It resets the GDC to its idle state and specifies the video display formats when executed with the appropriate parameters. When executed without parameters, it simply causes the display to blank and the GDC chip to remain idle; no previous parameters are changed. To ensure that this command is received by the iSBX 275 VGC board, ignore the status of the First In/First Out (FIFO) register. This command clears the FIFO and terminates any previous command. Table 3-3 defines the eight parameter bytes following this command.

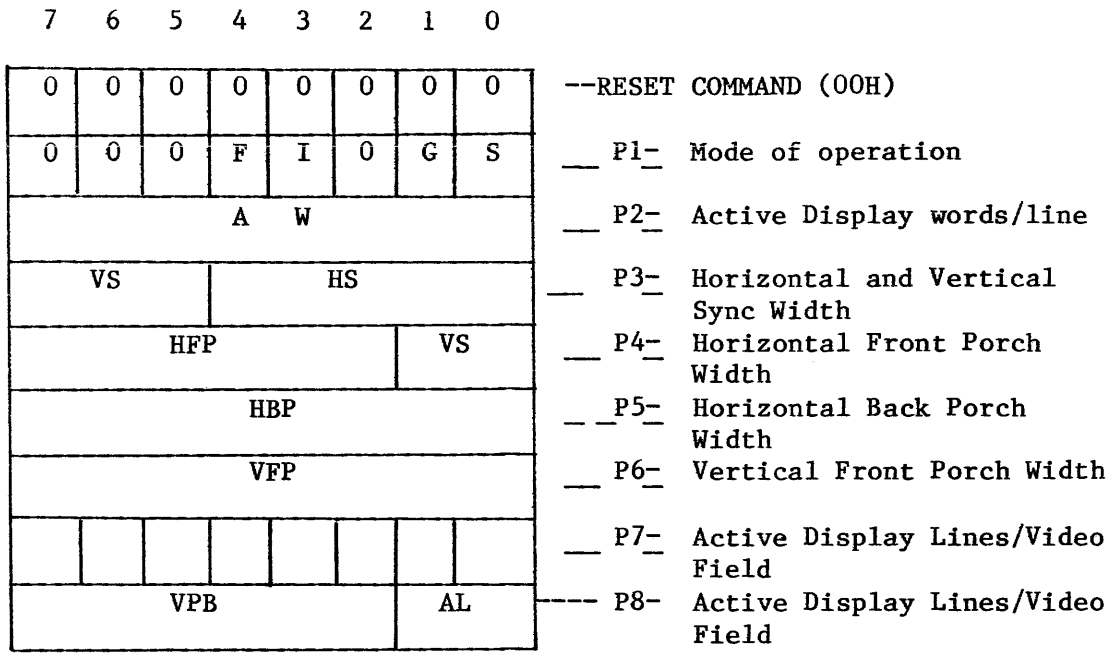


Figure 3-2. Reset Command and Parameter Bytes

Table 3-3. Definition of Reset Parameter Bytes

Byte	Function
1	This byte defines the mode of the iSBX 275 VGC board as follows:

0	0	0	F	I	0	G	S

I S
0 0 = Non- Interlaced
0 1 = Invalid
1 0 = Interlaced Repeat Field for Character Displays
1 1 = Interlaced

G
0 = Mixed graphics and character mode
1 = Graphics mode

F
0 = Drawing during active display time and retrace blanking
1 - Drawing only during retrace blanking

2 The value of this parameter byte specifies the number of active words per line (the horizontal dot resolution divided by 16). It must be an even number and two less than the value desired; if a resolution of 256 dots is required, the value given for this parameter = 14 decimal or 0EH (256 divided by 16 equals 16; 16 minus 2 equals 14).

3 The value for the upper portion of this parameter byte specifies the horizontal sync width in words. (With a crystal oscillator of 12.6 MHz, one word time is 1.27 microseconds for black and white or 2.54 microseconds for color.) The value must be programmed to one less than the desired value, i.e., if a horizontal sync width of 5 microseconds is required in color mode, the parameter value is 5/2.54 = 2; 2 minus 1 = 1.

4 The value for the upper portion of parameter 3 and the lower portion of parameter 4 is the vertical sync pulse width in lines. This value specifies the number of lines that the VSYNC signal is active. The time period of a line is calculated as LT = WT x (AW + HFP + HBP + HS). Where: LT = line time, WT = word time, AW = Active display words/line, HFP = horizontal front porch width (in words), HBP = horizontal back porch (in words), and HS = horizontal sync width (in words).

The value for the lower portion of parameter 4 is the horizontal front porch width in words. This value must be one less than the desired value. If a light pen is to be used, the minimum horizontal front porch width must be six words. This results in a minimum parameter value of five words.

Table 3-3. Definition of Reset Parameter Bytes (continued)

Byte	Function
5	The value for parameter 5 specifies the horizontal back porch width in words. It must be one less than the desired value. The minimum horizontal back porch width is 3 words, resulting in a minimum parameter value of 2 words.
6	The value for parameter 6 specifies the vertical front porch width in lines.
7	The value for parameter 7 and the lower portion of parameter 8 specifies the number of lines displayed (the Y resolution) if in the non-interlace mode of operation. If the interlace mode of operation is used, this value is YRES/2.
8	The value for the lower portion of this parameter along with the upper portion of parameter 7 specifies the number of lines displayed (the Y resolution). The upper portion of this parameter specifies the vertical back porch width in lines.

Consult the vendor manual for the information for your monitor. The Horizontal rate of your monitor is one piece of information that you will need. The typical horizontal rate of a video monitor is 15.75 KHz or 63.5us. The typical frame rate of a monitor is 60 Hz or 16.7 ms. Next, consider the type of display you want; either interlace or non-interlaced. Your option may be the interlaced mode of operation which provides a frame rate of 30 Hz or 33.33 ms. Some monitors provide faster horizontal scan rates up to 35 KHz. The maximum horizontal rate which the iSBX 275 VGC board supports depends on the horizontal resolution and the horizontal blanking time. Next, you want to consider the horizontal resolution which depends on the selected memory size. The iSBX 275 VGC board provides 512 x 512 (which for a 15.75 KHz frame rate and a 60 Hz field rate forces you to use the interlaced mode). An example of the calculations involved in determining the initialization parameters for the iSBX 275 VGC board is as follows:

Given: From a black and white monitor vendor manual:

Horizontal Pulse width = 2.5 us (MIN) to 30 us (MAX)
Vertical Pulse Width = 75 us (MIN) to 1.2 ms (MAX)
Horizontal rate = 15750 Hz
Field rate = 60 Hz

Given: From the 82720 GDC chip specifications:

Horizontal Back Porch (in words must be equal to or greater than 3 words).
Horizontal Front Porch (in words must be equal to or greater than 2 words).
Number of active words per line must be an even integer from 2 to 256 and a multiple of 16.

In the following example, a memory size of 256 by 256 using the non-interlaced mode is selected to be displayed on a monitor with a 4:3 aspect ratio.

First, find the active words per line that best utilizes memory by:

$(256)^2 = (16 \times AW) \times (16 \times 3/4\ AW)$
$(256)^2 = 3/4 \times (16 \times AW)^2$
taking the square root of both sides: (256) = SQRT of 3/2 16 x AW
AW = 16 x 2/SQRT of 3
AW = 32/SQRT of 3 = 18.5 (rounded down) = 18 active words/line

Next, find the total number of lines per field by:

15750/60 = 262 total lines per field.

Third, find the horizontal resolution by:

Since there are 18 active words per line 16 times that will give the number of dots per line or the horizontal resolution. Thus,

18 x 16 = 288 dots/active line or the horizontal resolution.

Due to the 4:3 aspect ratio of the monitor selected for this example, the number of bits displayed in the Y or vertical direction is equal to 3/4 of the number displayed in the X or horizontal direction. Therefore, the number of dots/display line = 288 x 3/4 = 216.

Fourth, find the number of lines to be blanked by:

262 -216 = 46 lines to be blanked.

Because one horizontal line time is equal to 63.5 us, initially assign four for the Vertical Sync pulse width.

63.5 us x 4 = 254us which is within the rated specification for the vertical sync pulse.

Lets evenly space the VFP and VBP in front and in back of the Vertical sync pulse, make VBP and VFP = 21 lines each.

Therefore the total = 21 plus 21 plus 4 = 46. 46 plus 216 = 262.

CAUTION

Damage will result to some monitors if power is supplied to the monitor without sync signals or if the sync signals are at the wrong frequency.

The dot time is equal to the reciprocal of 12.6 MHz times 2 = 158 ns.

Find the active word time by;
16 times 158ns = 2.5 us.

The time of one horizontal line = 63.5 us. Therefore,

63.5 us/2.5us = 25 words/line.

Since 18 of the 25 words per line are the displayed words, 25 - 18 (displayed words/line) = 7 words/line which are to be used for blanking.

The total number of words to be blanked are 7 which includes (HS + HFP + HBP). Since the minimum number of words that the GDC chip requires is 3 for HBP, assign 3 words for HBP, plus 2 words for HFP, leaves 2 words left to assign for Horizontal Sync.

With this information empirically derived, the initialization parameters can now be assigned as follows:

X resolution (bits) = 288 or 120H
Y resolution (bits) = 216 or D8H
Horizontal sync width (words) = 2
Vertical sync width (lines) = 4
Horizontal Front Porch (words) = 2
Horizontal Back Porch (words) = 3
Vertical Front Porch (lines) = 21 or 15H
Vertical Back Porch (lines) = 21 or 15H
Operation Mode = 00010001 (binary)

3-8. VSYNC (6FH). This command is used to set the GDC on the board as the master sync generator. Figure 3-3 shows the VSYNC command.

0	1	1	0	1	1	1	1

Figure 3-3. VSYNC Command

3-9. SYNC (0FH or 0EH). The SYNC command is used to enable (0F) or blank (0E) the display. This command is also used to control the video display with the same parameters allowed as that for the Reset command. The difference being that this command does not reset the GDC nor does it place the GDC in a idle state. This command and associated parameters are shown in Figure 3-4. Table 3-3 defines each of the associated parameter bytes.

0	0	0	0	I	1	1	X	__ SYNC
0	0	0	F	I	0	G	S	__ P1- Mode of operation
A W								__ P2- Active Display words/line
VS			HS					__ P3- Horizontal and Vertical Sync Width
HFP						VS		__ P4- Horizontal Front Porch Width
HBP								__ P5- Horizontal Back Porch Width
VFP								__ P6- Vertical Front Porch Width
								__ P7- Active Display Lines/Video Field
VPB						AL		---- P8- Active Display Lines/Video Field

Figure 3-4. SYNC Command and Associated Parameter Bytes

3-9. DISPLAY CONTROL COMMANDS

There are six Display Control commands which are used to control the manner in which an image drawn in the display memory is accessed and displayed on the attached screen of the monitor. These six Display Control commands are as follows:

3-11. PITCH (47H). This command specifies the width of the display memory in the horizontal dimension. It sets the number of words between vertically adjacent pixels. If the bit map and the display window are the same size, the pitch should be the same as the Active Words per line parameter programmed as part of the Reset or SYNC command (a horizontal resolution of 256 dots results in a pitch of 16) or 256/16 = 16. Note that the value entered for the pitch parameter is not decremented by one as in the parameter value entered for the horizontal resolution parameter for the Reset command. If a Reset command is executed and parameter 2 of the Reset command is sent, the Pitch command must be executed to properly reload the Pitch register within the GDC.

By specifying a pitch parameter which is greater than the Active Words per line, a bit map can be created that is wider than the display surface. Changing the starting address of the display (with the PRAM command) allows the display window to be panned across the bit map. If a wider bit map is used, care must be taken to avoid drawing figures which exceed the available memory or inadvertantly cross from one color plane to another. Figure 3-5 shows the PITCH command and associated parameter byte. Note that the Active Word (AW) parameter value is two less than the display window width. The Pitch command must be used to set the proper memory width larger than the window width.

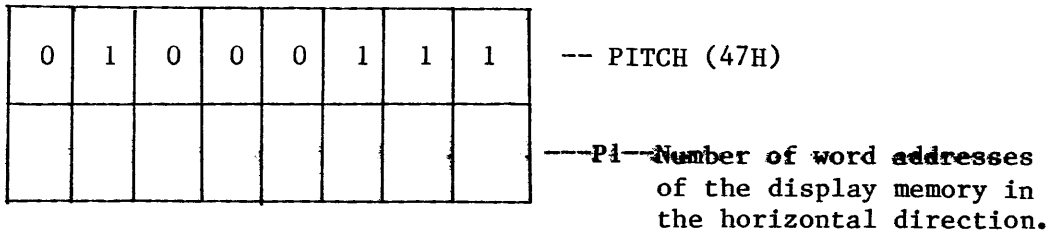


Figure 3-5. PITCH Command and Associated Parameter Byte

3-10. ZOOM (46H). This command is used to specify the multiplier factors used during display and character drawing and rectangle filling. The board does not support display zooming; therefore, the upper four bits (nibble) of the parameter must be zero. The zoom magnification factor for a graphic character is set by the lower nibble in integer multiples. A value of 0 sets the multiplication factor to 1; a value of 15 sets the multiplication factor to 16. Figure 3-6 shows the Zoom command and associated parameter byte.

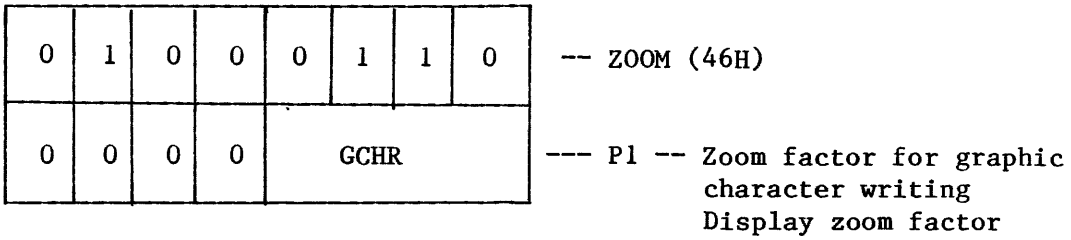


Figure 3-6. ZOOM Command and Associated Parameter Byte

3-11. PRAM (7XH). This command is used for loading the internal 16-byte RAM area of the GDC chip. The lower four bits of this command determine the starting address in the parameter RAM area. The succeeding bytes are stored in predefined locations. The host processor can write into any location of the PRAM and load up to 16 bytes into the parameter RAM at incrementing addresses. The parameter RAM area within the GDC chip is used to store two types of information. It is used to specify the details of the display area partitions, or used to supply the bit pattern for either figure drawing or the graphic character. The sequence of the byte transfers is terminated by the next command byte entered into the FIFO. Figure 3-7 shows the PRAM command and associated parameter bytes. Table 3-4 defines the parameter bytes associated with the PRAM command. This command may be used to modify the contents of any byte or sequence of bytes starting with the byte specified within the least significant four bits of the command byte. The starting address is used in panning and scrolling. To pan, your PITCH must be greater than the active words per line. To scroll, your starting address is incremented in multiples of your PITCH setting. In color mode, scrolling tends to shift your displayed screen and therefore is not useful. The black and white mode affords a 256 x 256 non-interlaced mode which is useful for panning and scrolling. The 512 x 512 interlaced mode does not lend itself very well to panning and scrolling due to the memory constraints.

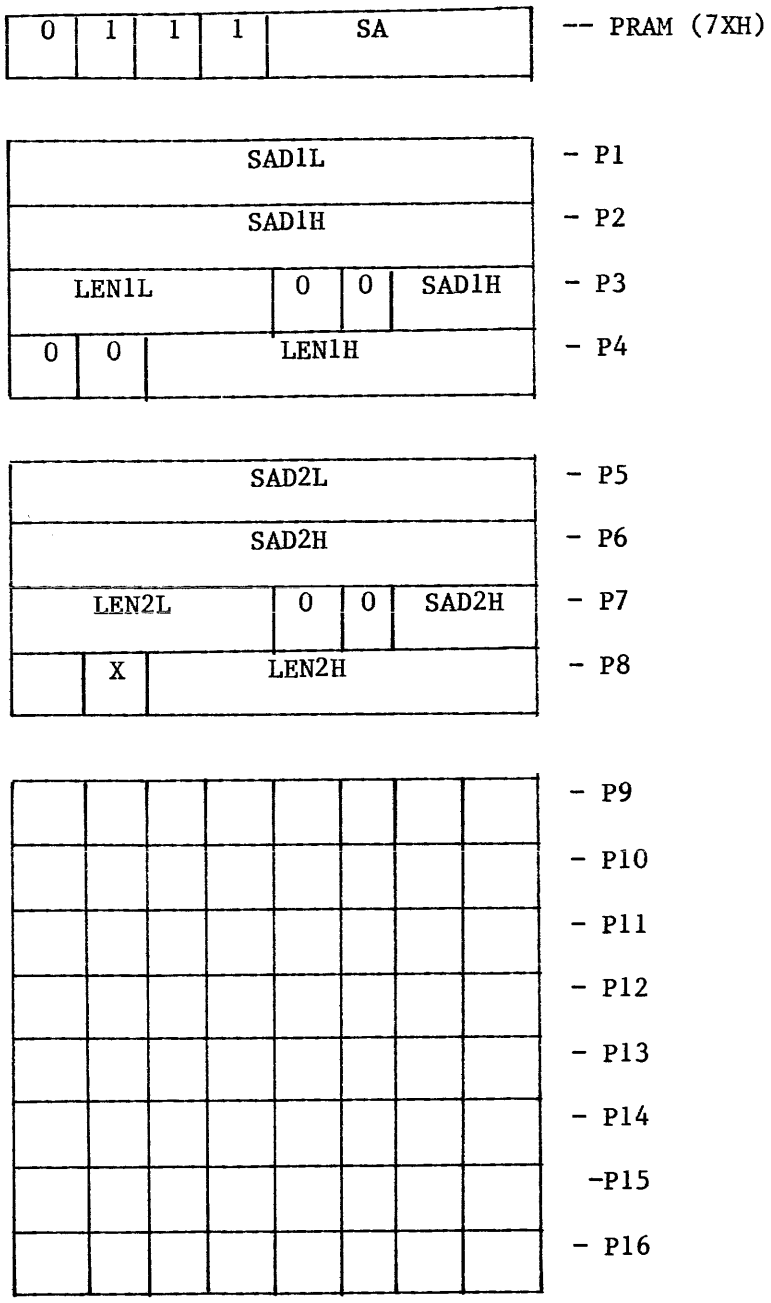


Figure 3-7. PRAM Command and Associated Parameter Bytes

Table 3-4. Definition of PRAM Parameter Bytes

Byte	Function
	The command byte specifies the starting address in the parameter RAM. From the starting address, any number of bytes may be loaded into the parameter RAM at incrememting addresses up to 15.
1 - 4	The first 4 bytes specify the starting address and the length of the top portion of the first display area. The starting address uses an 18-bit value, but the board only uses the least significant 14 bits. Normally, a starting address of 0 is used. The length portion of the parameter RAM block is a 10-bit value used to specify the length (in words) of the first (top) display window. When only one display window is used, the length should be set to its maximum value (3FFH). Note that the top two bits of the fourth byte must be 0.
5 - 7	If two display windows are used, these bytes specify the starting address and the length of the bottom display area (or second window) following the same guidelines as listed above.
8 - 9	Bytes 8 through 9 specify the 16 bit pattern information when in the bit-mapped graphics mode. When drawing a line, arc, or rectangle (linear figures), bytes 8 and 9 are used to specify the line style (dotted or dashed).
8 - 15	Bytes 8 through 15 are used to specify the character font bit pattern when drawing a graphics character. A value of 1 enables the corresponding pixel, while a value of 0 suppresses it. Again, a value of 1 in a given bit position enables drawing, while a value of 0 suppresses it.

3-12. CURS (49H). This command sets the position of the graphics cursor by specifying the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word. The memory address is an 18-bit value, while the dot address within the word is a 4-bit value. This results in a total of 22 bits of pixel address. Figure 3-8 shows the CURS command and associated parameter bytes.

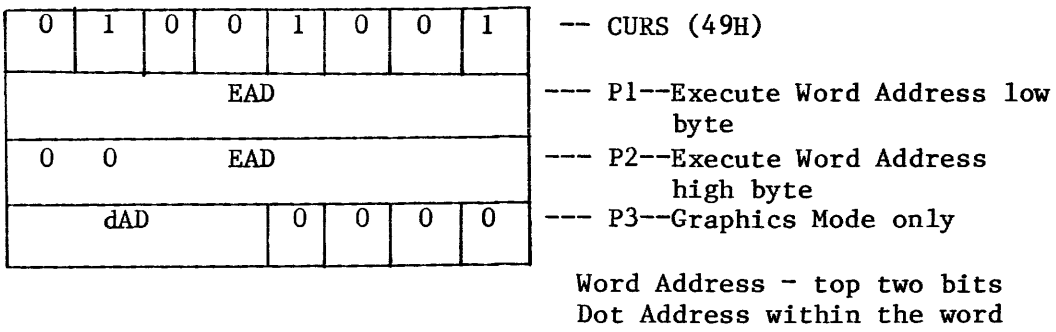


Figure 3-8. CURS Command and Associated Parameter Bytes

Normally, graphic coordinates are specified by the X and Y coordinates of the Cartesian coordinate system with the origin (X = 0, and Y = 0) at the bottom left corner of the screen. The device driver software must convert these X and Y values to an absolute memory address. Note that the memory address starts at the top of the display and increments toward the bottom of the screen, while the Y coordinate starts at the bottom and increases toward the top of the screen. This direction reversal means the Y coordinates must be inverted before the memory address is calculated.

In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word. The following equations show the calculation for the absolute memory address:

X = X coordinate. It must be in the range $0 \leq X \leq XRES$

Y = Y coordinate. It must be in the range $0 \leq Y \leq YRES$

Where: XRES = horizontal resolution in dots
YRES = vertical resolution in dots
Y' = inverted Y coordinate
MA = memory address

$$Y' = (YRES - 1) - Y$$

$$MA = Y' * XRES + X$$

If color mode is used, the base address of the color plane must be added in the equation. Note that the color plane size must be converted from words into bits. The color plane base address constants are:

RED = 0
BLUE = 1000H words, 10000H bits
GREEN = 2000H words, 20000H bits

Once the 22-bit memory address is calculated, it must be formatted by the driver software into the form required by the CURS command.

Memory Address (MA) = ZAABBC

B	B	- Parameter 1 EAD
0 0 A*	A	- Parameter 2 EAD
C	0 0 0 0	- Parameter 3 dAD

A, B and C are 4-bit nibbles
* set the upper two bits of this nibble to 0.

3-13. START (6BH). This command starts the display process with the previously defined display conditions. Figure 3-9 shows the START command.

0	1	1	0	1	0	1	1	--START (6BH)

Figure 3-9. START Command

3-14. BCTRL (0CH or 0DH). The blanking control command (0DH) enables and (0CH) disables the display process, blanking the screen. Figure 3-10 shows the BCTRL command.

0	0	0	0	1	1	0	X	--BCTRL (0CH, 0DH)

Figure 3-10. BCTRL Command

3-15. DRAWING CONTROL COMMANDS

The Drawing Control commands are used to perform bit-map manipulation and to draw figures. These commands are used repeatedly as figures are drawn.

3-16. MASK (4AH). The Mask command loads the 16-bit Mask register which specifies the bit or bits within the currently addressed display memory that are to be modified. The Mask register can be modified using the CURS command to reposition the cursor or modify the drawing. Two parameters associated with the Mask command are used to load a 16-bit value into the Mask register. If normal single pixel at a time graphics figure drawing is desired, there is no need to use this command because the CURS command sets up the proper pattern to address the proper pixels as the drawing progresses. The Mask register should be set to all ones for any word-at-a-time operation. Figure 3-11 shows the Mask command and assoicated parameter bytes. Table 3-5 defines the parameter bytes associated with the Mask command.

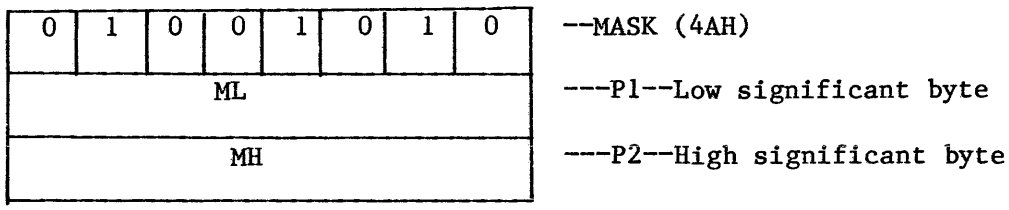


Figure 3-11. MASK Command and Associated Parameter Bytes

Table 3-5. Definition of MASK Command Bytes

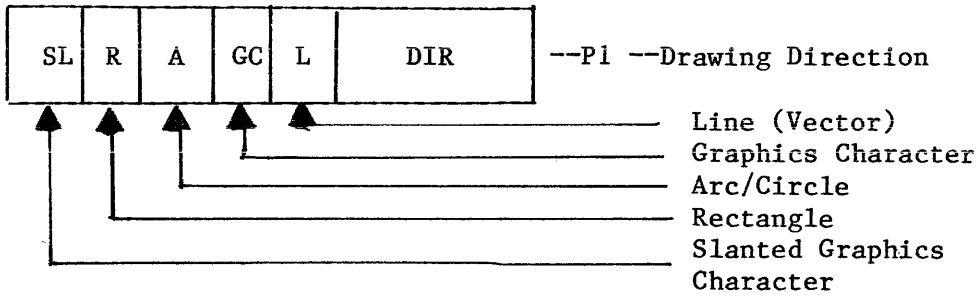
Byte	Function
1	The value of 1 for each bit defines the bits of the least significant byte in display memory that can be modified.
2	The value of 1 for each bit defines the bits of the most significant byte in display memory that can be modified.

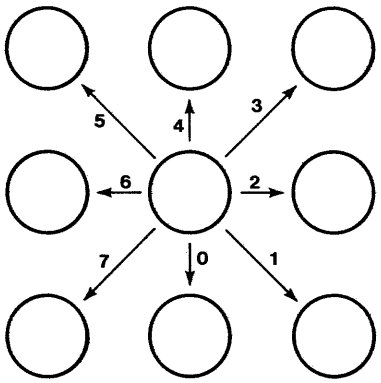
3-17. FIGS (4CH). The FIGS command specifies the geometric figure or graphic character to be drawn and is used to set up the parameters needed to modify the bit map. Up to 11 parameters may follow this command. To prepare for graphics drawing, the GDC requires the figure type, the direction, and drawing parameters, the starting pixel address, and the pattern. Once these are stored within the GDC, the Figure Draw (FIGD) command initiates the drawing operation. Figure 3-12 shows the FIGS command and associated parameter bytes. Table 3-6 defines the parameter bytes associated with the FIGS command.

0	1	0	0	1	1	0	0	--FIGS (4CH)
SL	R	A	GC	L	DIR			-- P1 Drawing Direction
DC								-- P2 DC Drawing Character
0	GD	DC						-- P3 DC Drawing Character (high bits)
DL								-- P4 D Drawing Parameter
0	0	DH						-- P5 D Drawing Parameter
D2L								-- P6 D2 Drawing Parameter (Low byte)
0	0	D2H						-- P7 D2 Drawing Parameter (High byte)
D1L								-- P8 D1 Drawing Parameter (Low byte)
0	0	D1H						-- P9 D1 Drawing Parameter (High byte)
DML								-- P10 DM Drawing Parameter (Low byte)
0	0	DMH						-- P11 DM Drawing Parameter (High byte)

Figure 3-12. FIGS Command and Associated Parameter Bytes

Table 3-6. Definition of FIGS Parameter Bytes

Byte	Function
1	The three least significant bits of this byte specify the direction that the figure is drawn, while the next 5 bits select the drawing type. The GDC uses the successful approximation technique to find the next pixel of the figure. This pixel is one of the eight nearest neighbors to the last pixel drawn. The GDC assigns each of these eight directions a number from 0 to 7 as shown in Figure 3-13. Figure 3-14 shows the result of the direction parameter on the various figure types. 
2 and 3	These two bytes specify the Drawing Count (DC) parameter. The value specified should be one less than the number of RMW cycles to be executed. Byte 2 defines the least significant address; byte 3 defines the most significant address.
4 and 5	These two bytes specify the D parameter which is the number of words to be accessed in the direction specified.
6 and 7	These two bytes specify the D2 parameter which takes on different meanings depending on the type of figure to be drawn. Note that the upper two bits of these bytes are zero. Table 3-7 defines each of the parameters for a given drawing type. When drawing a line with a negative slope, you must swap the X and Y coordinates so that the absolute value of delta X (dX) is equal to or greater than the absolute value of delta Y (dY). The direction that the line is drawn depends on the polarity (sign) of three values: delta X (dX), delta Y (dY) and the difference of the absolute value of dX minus the absolute value of dY. Table 3-8 shows the relationships.
8 and 9	These two parameter bytes specify the D1 drawing parameter and take on a different meaning depending on the figure to be drawn.
10 and 11	These two parameter bytes specify the DM drawing parameter which is the dots to be masked from the figure to be drawn.



1113

Figure 3-13. Drawing Direction

DIR	LINE	ARC	CHARACTER	SLANT CHAR	RECTANGLE
000					
001					
010					
011					
100					
101					
110					
111					

1114

Figure 3-14. Drawing Direction Resulting from Direction Parameter

Table 3-7. Graphics Figure Drawing Parameters

DRAWING TYPE	DC	D	D2	D1	DM
Initial Value*	0	8	8	−1	−1
Line	$\lvert\Delta I\rvert$	$2\lvert\Delta D\rvert-\lvert\Delta I\rvert$	$2(\lvert\Delta D\rvert-\lvert\Delta I\rvert)$	$2\lvert\Delta D\rvert$	—
ARC**	r sine$\Phi\uparrow$	r−1	2(r−1)	−1	r sine θ
Rectangle	3	A−1	B−1	−1	A−1
Area Fill	B−1	A	A	—	—
Graphic Character***	B−1	A	A	—	—
Read & Write data	W−1	—	—	—	—

* Initial values for the various parameters remain as each drawing process ends.

** Circles are drawn with 8 arcs, each of which span 45° so that the sine $\Phi = 1/\sqrt{2}$ and sine $\theta = 0$.

*** Graphic characters are a special case of bit-map area filling in which B and A ≤ 8. If A = 8 there is no need to load D and D2 parameters.

Where:
−1 = all ONES value

All numbers are shown in base 10 for convenience. The GDC accepts base 2 numbers (2's complement notation where appropriate).

— = no parameter bytes sent to the GDC for this parameter.

ΔI = The larger of ΔX or ΔY.

ΔD = The smaller of ΔX or ΔY.

r = The radius of curvature, in pixels.

Φ = Angle from the major axis to the end of the arc, $\Phi \leq 45°$.

θ = Angle from major axis to the start of the arc, $\theta \leq 45°$.

$\uparrow$ = Round up to next higher integer.

$\downarrow$ = Round down to next lower integer.

A = Number of pixels in the initially specified direction.

B = Number of pixels in the direction at right angles to the initially specified direction.

W = Number of words to be accessed.

C = Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected.)

D = Number of words to be accessed in the direction at right angles to the initially specified direction.

DC = Drawing count parameter which is one less than the number of RMW cycles to be executed.

DM = Dots masked from drawing during arc drawing.

Table 3-8. Relationship of Line Drawing Direction

dX	dY	dX - dY	Direction	L	D
+	+	+	2	X	Y
+	+	-	3	Y	X
+	-	+	1	X	Y
+	-	-	0	Y	X
-	+	+	5	X	Y
-	+	-	4	Y	X
-	-	+	6	X	Y
-	-	-	7	Y	X

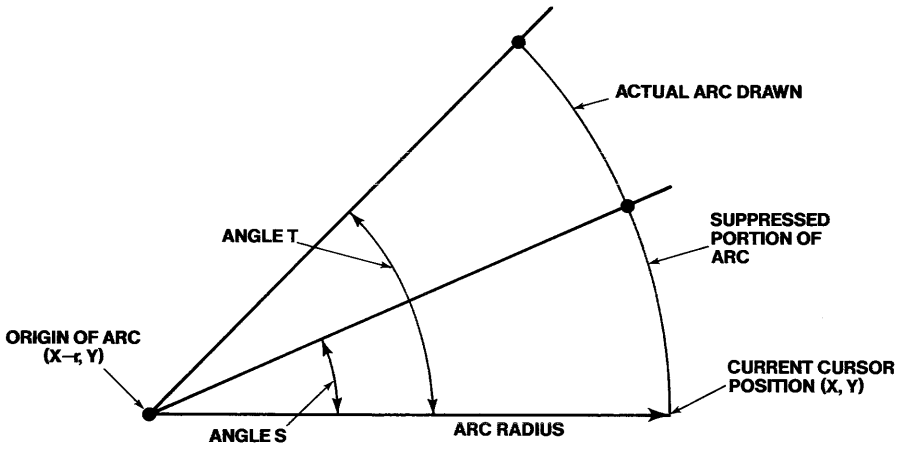
When drawing an arc, several points must be kept in mind. First, the maximum arc angle is 45°, starting on a coordinate axis intercept. The current cursor position is used as the coordinate intercept point, and the contents specified by the DIR parameter indicate the direction that the arc is drawn. Two angles are used to specify the arc. Figure 3-15 shows an example of drawing an arc with a DIR of 4. Angle "T" specifies the total angle from the coordinate axis of the arc (up to 45°). Angle "S" specifies the angle from the coordinate axis of the suppressed (not displayed) portion of the arc. It also shows the drawing parameters definition.

A circle is drawn as eight 45° arcs, each starting at a coordinate axis intersection, the origin being at the center of the circle. If (X,Y) is the position at the center of the arc, the starting points are: X+r, Y (right edge), X-r, Y (left edge), X, Y + r (top edge), and X, Y-r (bottom edge). Two arcs are drawn in opposite directions beginning at the starting point.

When drawing a rectangle, the length and height parameters (D and D2) specify the number of pixels on each side of the box, not including the starting point. Figure 3-16 shows a box drawn with a starting point of (0,0), a length of 4 (D = length minus one or 3) and a height of 6 (D2 = height minus one or 5). The result would actually be a box 5 pixels by 7 pixels.

When filling a rectanglar area, you must change the parameter definition. Parameters D and D2 are set to length + 1, while the parameter DC is set to the height. For example, if the rectangle shown in Figure 3-16 were completely filled (including the borders), the cursor would be positioned at (0,0), parameters D and D2 would be set to 5 (length + 1), and parameter DC would be set to 6 (height).

If only the interior of the rectangle is to be filled (assuming the borders were previously drawn and are to be left intact), the cursor would be positioned at (1,1), parameters D and D2 would be set at 3 ([length +1] -2). Two must be substracted to compensate for the left and right borders, and parameter DC would be set to 4 (height minus 2). Two is subtracted to compensate for the top and bottom borders.



PARAMETER	CONTENTS	
DC	r * sin (T)	ROUNDED UP
D	r – 1	
D2	2 * (r–1)	
D1	-1	
DM	r * sin (S)	ROUNDED DOWN

NOTE: ANGLE T MUST BE GREATER THAN 0 AND LESS THAN OR EQUAL TO 45°
ANGLE S MUST BE GREATER THAN OR EQUAL TO 0 AND LESS THAN 45°

1115

Figure 3-15. ARC Drawing

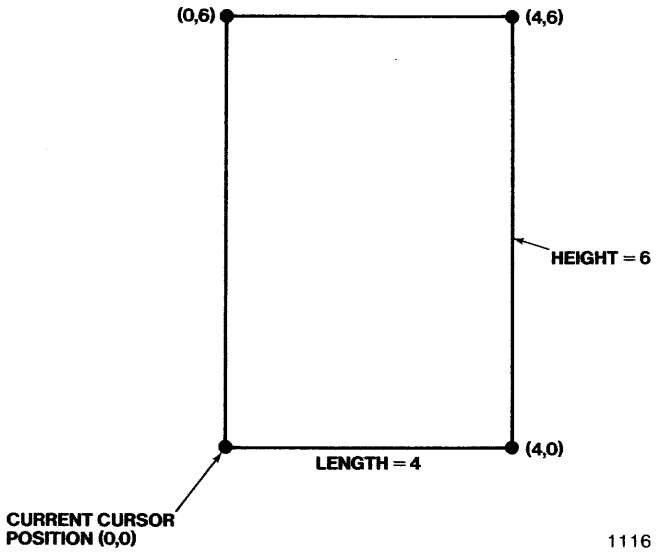


Figure 3-16. Rectangle Drawing

All figures are drawn from the current cursor position. Typically, a CURS command is given prior to each figure drawing (FIGD) command to position the cursor at the starting point of the figure. The drawing parameters loaded into the GDC are modified as drawing progresses; therefore, they must be reloaded when another figure is to be drawn, even if it is the same figure.

3-18. FIGD (6CH). The FIGD command loads the previously loaded drawing parameters from the Parameter RAM into the drawing processor and starts the drawing process at the pixel address pointed to by the cursor. Figure 3-17 shows the FIGD command.

0	1	1	0	1	1	0	0	--FIGD (6CH)

Figure 3-17. FIGD Command

3-19. GCHRD (68H). The GCHRD command is used to start drawing a graphics character or begin filling an area with the pattern stored in the Parameter RAM. The parameters are loaded with the FIGS command. Drawing begins at the address in display memory pointed to by the EAD and dAD values. Prior to executing this command, you must load the Drawing Parameter Registers with the appropriate values and load the parameter RAM with the character font or fill pattern. Note that the loading of the Parameter RAM changes the line drawing pattern for later drawings; hence, you must remember to reload the line pattern before doing another figure drawing. Figure 3-18 shows the GCHRD command.

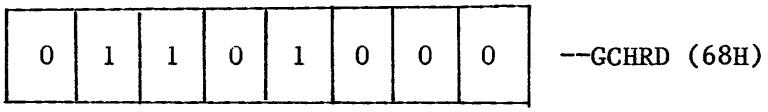


Figure 3-18. GCHRD Command

3-20. WDAT (base code = 20H). The WDAT command initiates the RMW activity and writes data directly to the display memory. This command requires parameters to set the pattern register within the GDC while other commands use the stored value in the parameter RAM. The WDAT command must be preceeded by a FIGS command and its associated parameters. The first three parameters of the FIGS command are needed to set the type of drawing to take place, the direction of the drawing, and the DC value. The DC value of the DC parameter plus one is the number of RMW cycles performed by the GDC. The one RMW cycle is executed at the address pointed to by the cursor address. The EAD pointer is incremented to the next word as specified by the direction parameter. Additional parameters can then be accepted. For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle. Only the LSB of the parameter byte is used as the pattern during the RMW memory cycle. In addition, it may be used to set the type of drawing with other commands.

Three types of bit map modifications can take place; the lower two bits of this command specify the type. Once set, this modification mode is retained until another WDAT command is given. The WDAT command is given without parameters if setting the modification mode is all that is required.

If it is desired to write data directly to the bit map, the GDC must be placed in the mixed character/graphic mode. The cursor must then be positioned to the correct place and the mask register loaded with all ones (0FFFFH). The Direction and DC parameters must then be loaded with the desired direction code and a value equal to one less than the number of words to be written. A direction of 2 is typically used. The WDAT command is then given one set of parameters (either one or two bytes, depending on whether bytes or words are to be written). The GDC repeatedly writes the same data pattern to memory the number of times specified by the DC parameter.

While the GDC is writing to the display memory, the "Drawing-IN-Progress" bit is not set. In order to determine when the WDAT command is completed, send the GDC another command (such as Display Start) and check the FIFO Empty status bit. When the value for this bit goes to a 1, both commands are complete.

Remember, the modification mode set by the last WDAT command is used for all subsequent drawings. Finally, the GDC should be placed back into the graphics mode for normal operation. Figure 3-19 shows the WDAT command and associated parameter bytes. Table 3-9 lists the modes and command codes.

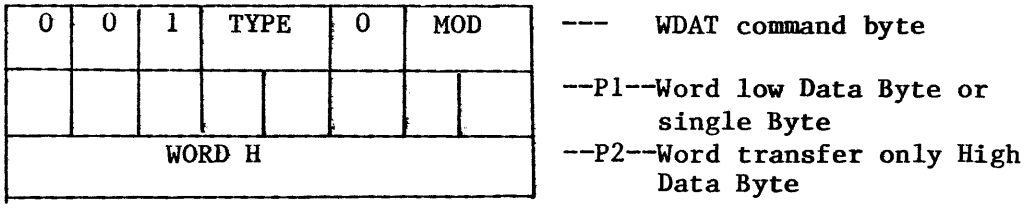
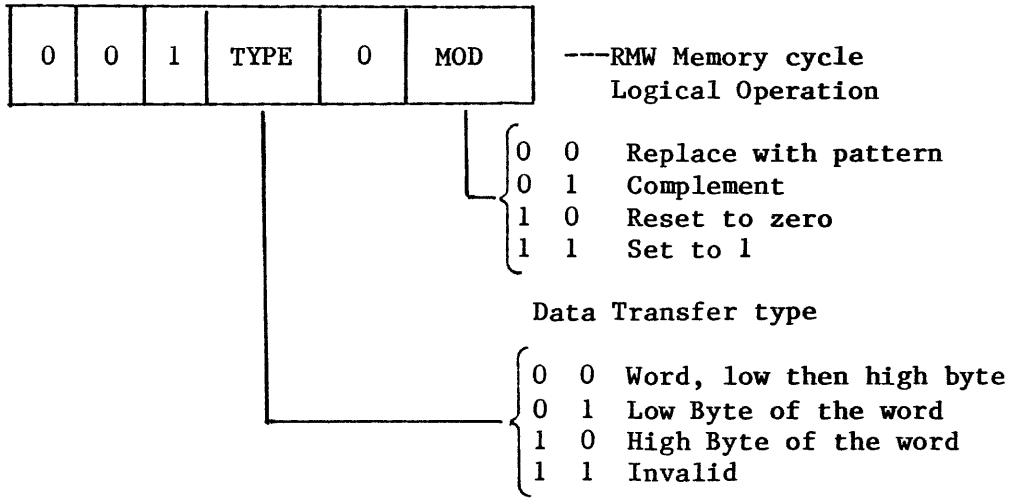


Figure 3-19. WDAT Command and Associated Parameter Bytes

Table 3-9. Definition of WDAT Parameter Bytes

Byte	Function
	The three least significant bits of this command byte specify the



1 This parameter byte is either the least significant byte of a word transfer or the single data byte.

2 This parameter byte is the most significant byte of a word transfer.

3-21. DATA READ COMMANDS

The Data Read commands allow the host processor to recover data from the GDC. This data is in addition to the status information always available via the status input port. After a Data Read command is given, the GDC's FIFO is cleared and is configured as an output buffer. Data is then passed back to the host processor with an input instruction. The presence of data is indicated by the setting of the Data Ready bit. A Data Read command may be aborted before all of the data is read by writing a new command to the GDC (ignore the FIFO Full Status bit). This terminates the Data Read command, clears the FIFO, and reverses the direction of data.

The Read Data Commands consists of RDAT, CURD, and LPRD.

3-22. RDAT (Base Code = 0A0H). The RDAT command reads data directly from the bit map display memory. Either bytes or words can be read. The sequence to use is as follows:

First, the cursor must be positioned to the correct location. Next, the mask register should be loaded with all ones (FFFFH). The direction and DC parameters should then be loaded using the same format as that used with the WDAT command with one exception. The exception being that the DC value is the actual number of either bytes or words to be read (not one less). The RDAT command can then be loaded. The data is then read a byte at a time from the data port.

The two least significant bits of the RDAT command byte also set the modification mode in the same manner as that used with the WDAT command. If the code "0A0H is used, the mode is set for a replace operation. Make sure that the correct mode is reloaded before other operations are started. Figure 3-20 shows the RDAT command.

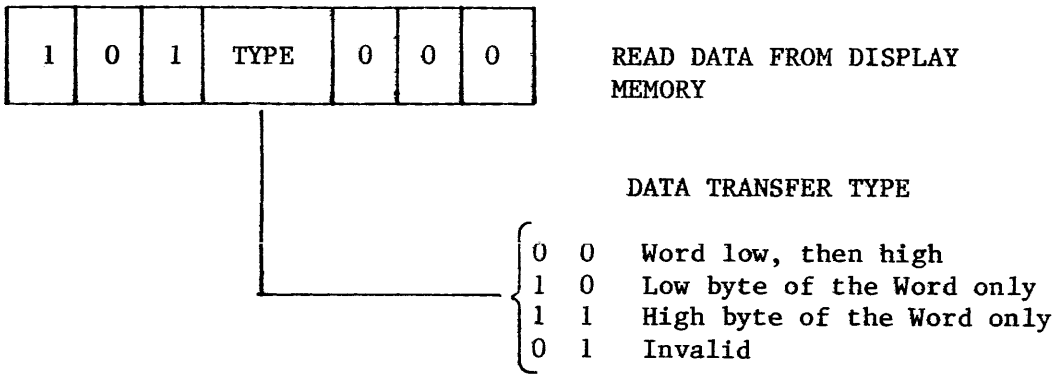


Figure 3-20. RDAT Command

3-23. CURD (0E0H). The CURD command reads the current cursor position. The first three bytes read are the 18 bits of absolute memory address (only the least significant 14 bits are used). The next two bytes are the 16-bit contents of the Mask Register. If the mask register was not directly loaded, the returned contents of the Mask register will be the one of 16 codes for the dot address. A value of 1 in the least significant bit corresponds to a dot address of 0; a value of 1 in the most significant bit corresponds to a dot address of 0FH. Figure 3-21 shows the CURD command and the bytes returned.

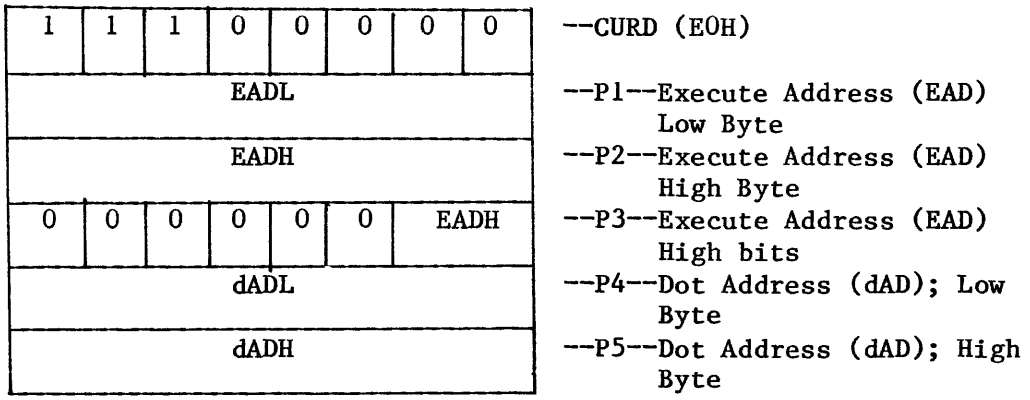


Figure 3-21. CURD Command and Returned Bytes

3-24. LPRD (0C0H). The LPRD command reads the address of a light pen "hit" after indication is posted in the status register. For a light pen to register, two consecutive "hits" at the same address must be detected. The address returned reflects a word level (not a dot level); thus, the returned address is 18 bits (3 bytes) in length. There is a position error of several words due to internal and external delays. The user software must correct the position by subtracting an empirically-determined value. Figure 3-22 shows the LPRD command and returned bytes.

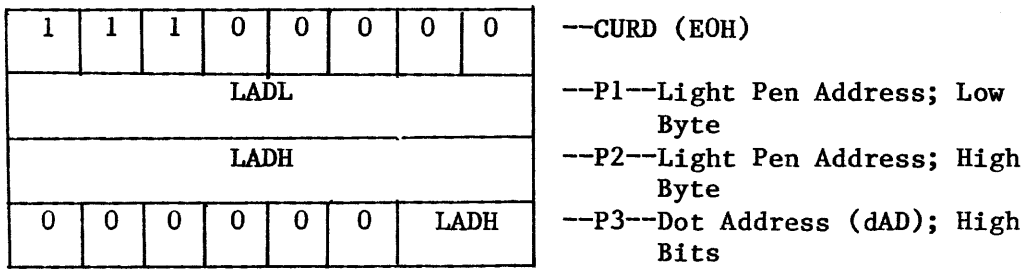


Figure 3-22. LPRD Command and Returned Parameter Bytes

3-25. OPERATION SEQUENCE

The following sequences are recommended. Following these sequences ensures that all registers are in the proper state.

After power up, the first operation should be the initialization operation. Once initialized, the GDC may be given an indefinite number of drawing and display commands without further operator intervention.

CAUTION

Do not apply power to the monitor until after the GDC initialization is complete. Turn off power to the display monitor before or at the same time that power is removed from the iSBX 275 VGC board. Some monitors may be damaged when operated without sync signals or with sync signals of the wrong frequency.

3-26. INITIALIZATION

The following operation should be performed to prepare the iSBX 275 VGC board for operation. Two key variables are used repeatedly and should be initialized here. These variables are the X resolution in dots (XRES) and the Y resolution in dots (YRES). The term "AR" refers to values selected "As Required" for the display monitor and for the particular system in use.

1. Issue Reset
   a. Operation Mode = AR
   b. Active Words/Line = (XRES/16) - 2
   c. Horizontal Sync = AR
   d. Vertical Sync = AR
   e. Horizontal Front Porch = AR
   f. Horizontal Back Porch = AR
   g. Vertical Front Porch = AR
   h. Active Lines/Frame = YRES or [(YRES - 1)/2 for interlace operation]
   i. Vertical Back Porch = AR
2. Set Pitch = XRES/16
3. Set Zoom = 0

4. Set Cursor Characteristics
   a. Lines/Row = 1
   b. Disable cursor

5. Set Starting Address in PRAM
   a. Address = 0
   b. Block Length = 3FFH

6. Set Vertical Sync Mode to Master

7. Clear Screen with WDAT command
   a. Set Mixed Character/Graphics Mode
   b. Set cursor address to 0
   c. Set Mask to 0FFFFH
   d. Set Direction to 2, set DC to 3FFFH
   e. Issue WDAT command with word operation, replace pattern (code 20H). Data = 00,00
   f. Set graphics mode

8. Begin Display

3-27. SYMBOL Drawing

The following steps should be followed when drawing characters or symbols to the screen:

1. Store character or symbol bit pattern into the parameter RAM.

2. Set modification mode.

3. Set Zoom as required.

4. Position cursor as required.

5. Set up drawing parameters.
   a. Select graphics character drawing
   b. Set Direction as required
   c. Set DC to 7

6. Issue Draw Graphics Character command.

7. To repeat (as for multiple color planes), go back to step 4.

3-28. FIGURE DRAWING

1. Set line pattern in bytes 8 and 9 of the parameter RAM.
2. Set modification mode.
3. Position cursor as required.
4. Set up drawing parameters.
   a. Select appropriate figure type and direction
   b. Load parameters DC, D, D2, D1, and DM as required
5. Issue Draw Figure command.
6. To repeat, go back to step 3.

3-29. RECTANGLE FILLING

The following steps should be followed when filling rectangular areas.

1. Store fill pattern into parameter RAM.
2. Set modification mode.
3. Set Zoom to 0.
4. Position cursor as required.
5. Set up Drawing parameters.
   a. Select Graphics Character Drawing
   b. Set Direction as required
   c. Set DC to height
   d. Set D and D2 to length + 1
6. Issue Draw Graphics Character command.
7. To repeat, go back to step 4.

3-30. EXAMPLE

In this example, the calculations are derived from a particular monitor. If you attempt to do this example, your calculations might be different depending on the type of monitor you are using. Using this as an example of how to derive the values for the different parameters, an arc will be created in display memory and displayed on the screen of your monitor.

Using the formulas given in paragraph 3-7, calculate the initialization parameters associated with the Reset command for your specific application. Send the Reset command and associated parameters required to initialize the iSBX 275 VGC board. Then send the Start command to the iSBX VGC board to display the image written in the display memory onto

the monitor. For calculation purposes in this example, lets use a horizontal resolution of 12H (18 words) and a vertical resoultion of D8H (216 lines). We now have to calculate the EAD. Assume that we want to display a 45 degree arc starting at an X coordinate of 45H and at a Y coordinate of 50H on the screen with a radius of 255 bits from the center of the arc. Therefore,

EAD = (Y MAX - Y)(xres words) + (x words)

EAD = (D8 -50)(12H) + (4)

EAD = (88)(12) + 4

EAD =990 + 4

EAD = 994

dAD = 5

Now that the EAD and dAD are calculated, lets enter these values as the parameter bytes associated with the CURS command.

Output the byte 49H (CURS command) to the command port of the GDC.

Output the byte 94H as the value for the least significant byte of the cursor position (as calculated) to the data port of the GDC.

Output the byte 09 as the value for the most significant byte of the cursor position (as calculated) to the data port of the GDC.

Output the byte 50 as the value for the top address bits of the cursor position and as the dot address

Now lets use the FIGS command to set up the drawing parameters for a 45° arc with a radius of 255 bits.

Output the byte 4C (FIGS command) to the command port of the GDC.

The code to specify Parameter 1 for drawing an arc with a DIR of 2 is 22H. Therefore, output the byte 22 to the data port of the GDC.

The code to specify the DC parameter 2 for an arc specifies a value calculated by multiplying the radius times the sine of angle theta rounded up to the next even integer. The sine of a 45 degree angle is .707. Therefore, .707 x 255 = 180.28; rounded up gives 181. The hexadecimal value of 181 = B4H. Therefore, output the byte B4 to the data port of the GDC.

Parameter 3 is the most significant byte of the DC parameter. Because B4 is the number of bits with which to draw the arc and because that value can be defined in the least significant byte, this byte should be set to 00.

Parameter 4 is the D parameter. This parameter for an arc specifies r minus 1. The radius desired is 255; therefore, 255 minus 1 = 254. The hexadeciamal value for 254 = FEH. Therefore, output the byte FE to the data port of the GDC.

Parameter 5 is the most significant byte of the D parameter. Because the value can be defined in the least significant byte, this byte should be set to 00. Therefore, output the byte 00 to the data port of the GDC.

Parameter 6 is the D2 parameter. This parameter for an arc specifies 2(r - 1). The desired radius is 255. Thus, 2 (255 - 1) = 508. The hexadecimal value for 508 = 1FCH. Therefore, output the byte FC to the data port of the GDC.

Parameter 7 is the most significant byte for the D2 parameter. Because the value for this byte exceeds FF, set this byte to 01.

Parameter 8 is the D1 parameter byte and for an arc is equal to - 1. Thus, as specified in Table 3-8, this byte is set to all ones or FFH. Therefore, output the byte FF to the data port of the GDC.

Parameter 9 is the most significant byte of the D1 parameter and is also set to all ones or FFH. Therefore, output the byte FF to the data port of the GDC.

Parameter 10 is the least significant byte of the DM parameter and for an arc is specified as the radius times the sine of angle theta rounded down. This parameter asks for the number of bits to be masked from the drawing. Because no bits are to be masked from the drawing the value entered should be zero. Therefore, output the byte 00 to the data port of the GDC.

The value for this byte is also zero for the same reason. Therefore, output the byte 00 to the data port of the GDC.

Now lets output the byte 6C (FIGD command) to the command port of the GDC to cause the GDC to draw the arc in memory and because of the initialization and start commands already given, the drawing of the arc will appear on the screen at the coordinates given. Figure 3-23 shows the relative position of the arc displayed on the screen.

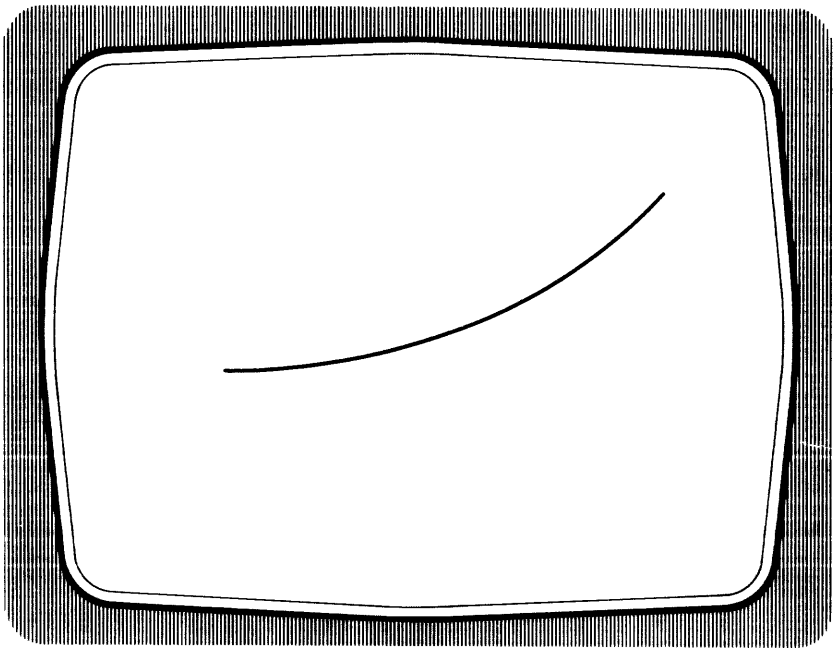


Figure 3-23. Arc Displayed on the Monitor

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CHAPTER 4. SERVICE INFORMATION

4-1. INTRODUCTION

This chapter provides service and repair assistance information. For personnel safety and system component protection, refer all servicing to qualified personnel only.

4-2. SERVICE AND REPAIR ASSISTANCE

The best service for your Intel product is provided by an Intel Customer Engineer. These trained professionals will provide prompt, efficient on-site installation, preventive maintenance, or corrective maintenance services that will keep your equipment in the best possible operating condition.

Your Intel Customer Engineer can provide the service you need through a prepaid service contract or on an hourly charge basis. For further information, contact your local Intel office.

When an Intel Customer Engineer is is not available in your local area, you may contact the Intel Marketing Administration directly at one of the following numbers:

Telephone:

From Western Region call 602 - 869-4951
Midwest Region call 602 - 869-4392
Eastern Region call 602 - 869-4045
International call 602 - 869-4391

Before calling the Intel Marketing Administration, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other Intel products it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other Intel products the serial number is usually stamped on a label.

d. Shipping and billing address.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Intel Marketing Administration personnel of this aggreement.

g. Product Service Maintenance Agreements are available through the local Product Service Sales Office.

Never return equipment to Intel for service or repair until after you contact a local field office or the Intel Marketing Administration.

If return of your equipment is necessary, you will be given a Repair Authorization Number, shipping instructions, and other important information that will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment, or if the product is out of warranty, a purchase order is necessary in order for the Intel Repair Center to make the repair.

When preparing the product for shipment to the Repair Center, use the original factory packaging material if available. If the original packaging material is not available, wrap the product in a cushioning material such as Air Cap SD-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. (or equivalent) and securely enclose it in a heavy-duty corrugated shipping carton. Mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by the Intel Repair Center.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

4-3. REPLACEMENT PARTS LIST

Refer to Table 4-1 for the Replacement Parts List. Figure 4-1 is a schematic diagram of the iSBX 275 Video Graphics Controller board.

Table 4-1. Replacement Parts Lists

Ref. Desg.	Description	Intel Part No.	Qty/ Assy.
C1 thru C24, C26	Cap. 0.1UF, 50 V, +80% -20%,	104324-049	25
C25	Cap. 22UF 15V, ±10%	101772-041	1
E1 thru E18	Jumper plug	102480-001	6
F1 thru F3	Fuse 1 AMP	102057-008	3
G1	Oscillator, 12.6 MHz	101582-013	1
J1	26-pin Video connector	104262-026 or 106891-013	1
P1	iSBX Bus connector	103109-001	1
R1	Potentiometer,500 ,1/2 W,10%	104239-006	1
R2	Resistor, 120,1/4W,5%	101655-017	1
R3	Resistor,10K,1/4W, 5%	101655-004	1
R4,R5	Resistor,390,1/4W,5%	101656-006	2
RP1	Resistor Pak,10K,6 pin,SIP	101726-038	1
U1	IC 74S174	100655-021	1
U2	IC 74LS174	100655-031	1
U3	IC 82720	107865-001	1
U4, U19	IC 74LS373	100697-031	2
U5, U6, U7, U8, U9, U10, U11, U12, U21, U22, U23, U24, U25, U26, U27, U28	IC 16K x 1 SRAM (2167)	106868-001	16
U13	IC 74S04	100604-021	1
U14	IC 74128	100626-001	1
U15, U16, U17, U29, U30, U31	IC 74LS166	100651-031	6
U18	IC PAL 16R4A	144633-001	1
U20	Control PAL	144634-001	1

***

APPENDIX A. GLOSSARY

The following is a glossary of terms used within this manual.

FIELD - A field consists of a continuous series of horizontal lines scanned from the top to the bottom of the screen at a 60 Hz rate.

For the interlaced mode, each field contains every other horizontal line. Thus, two fields are required for each complete picture or frame.

For the non-interlaced mode, each field contains the complete picture and is equal to a frame.

FRAME - For the non-interlaced mode, a frame is scanned at 60 Hz (U.S. manufacturers have 262 lines).

For the interlaced mode, a frame consists of two fields each of which is scanned at a 60 Hz for a frame rate of 30 Hz (U.S. manufacturers of television sets have 525 lines per frame).

HORIZONTAL BACK PORCH - The horizontal back porch signals the start of the non-displayed area at the left edge of a horizontal sweep.

HORIZONTAL BLANKING - Horizontal blanking is the non-displayed time of every scan line. It consists of the sum of the horizontal sync, the horizontal front porch and the horizontal back porch.

HORIZONTAL FRONT PORCH - The horizontal front porch signals the start of the non-displayed area at the right edge of a horizontal sweep.

HORIZONTAL RESOLUTION - The number of discernable dots displayed along a horizontal scan line of a monitor.

HORIZONTAL SYNC - Horizontal sync indicates the horizontal retrace period and initiate the start of a new horizontal scan line. For typical monitors, a horizontal sync pulse takes place every 63.5 us.

PIXEL - A pixel is one dot or picture element on a raster scan line.

VERTICAL BACK PORCH - The vertical back porch signals the non-displayed area at the top edge of the screen.

VERTICAL BLANKING - Vertical blanking is the time it takes from the bottom of a field to the top of the next field and consists of the vertical sync, the vertical front porch and the vertical back porch.

VERTICAL FRONT PORCH -The vertical front porch signals the non-displayed area at the bottom edge of the screen.

VERTICAL RESOLUTION - The number of discernable lines displayed on the monitor.

VERTICAL SYNC - Vertical sync indicates the vertical retrace period and the start of the next frame.

***

APPENDIX B

This appendix contains the code for an 8 x 8 matrix for generation of an ASCII character set available on a typical typewriter type keyboard.

CODE	CHAR	LINE 0	1	2	3	4	5	6	7
00	GC1	BF	DF	DF	EF	F7	F7	FB	FD
01	GC2	FE	FD	FD	FB	F7	F7	EB	DD
02	GC3	BE	DD	DD	EB	F7	F7	EB	DD
03	GC4	F7	F7	F7	F7	F7	F7	F7	F7
04	GC5	F7	F7	F7	F7	F7	87	FF	FF
05	GC6	FF	FF	FF	FF	FF	87	F7	F7
06	GC7	FF	FF	FF	FF	FF	F0	F7	F7
07	GC8	F7	F7	F7	F7	F7	F0	FF	FF
08	GC9	FF	FF	FF	FF	FF	80	FF	FF
09	GC10	F7	F7	F7	F7	F7	80	FF	FF
0A	GC11	F7	F7	F7	F7	F7	87	F7	F7
0B	GC12	F7	F7	F7	F7	F7	F0	F7	F7
0C	GC13	FF	FF	FF	FF	FF	80	F7	F7
0D	GC14	F7	F7	F7	F7	F7	80	F7	F7
0E	GC15	F0	F0	F0	F0	F0	FF	FF	FF
0F	GC16	87	87	87	87	87	FF	FF	FF
10	GC17	FF	FF	FF	FF	FF	F0	F0	F0
11	GC18	FF	FF	FF	FF	FF	87	87	87
12	GC19	F0	F0	F0	F0	F0	87	87	87
13	GC20	87	87	87	87	87	F0	F0	F0
14	GC21	80	80	80	80	80	F0	F0	F0
15	GC22	80	80	80	80	80	87	87	87
16	GC23	80	80	80	80	80	FF	FF	FF
17	GC24	FF	FF	FF	FF	FF	80	80	80
18	GC25	F0	F0	F0	F0	F0	F0	F0	F0
19	GC26	87	87	87	87	87	87	87	87
1A	GC27	F0	F0	F0	F0	F0	80	80	80
1B	GC28	87	87	87	87	87	80	80	80
1C	GC29	FF	FF	FF	E3	E3	E3	E3	FF
1D	GC30	BF	DF	EF	EF	EF	E0	EF	EF
1E	GC31	FE	FD	FB	FB	FB	03	FB	FB
1F	32	F7	F7	F7	F7	F7	FF	FF	FF
20	SP	FF	FF	FF	FF	FF	FF	FF	FF
21	!	F7	F7	F7	F7	F7	FF	F7	FF
22	"	EB	EB	EB	FF	FF	FF	FF	FF
23	#	EB	EB	C1	EB	C1	EB	EB	FF
24	$	F7	C3	F5	E3	D7	E1	F7	FF

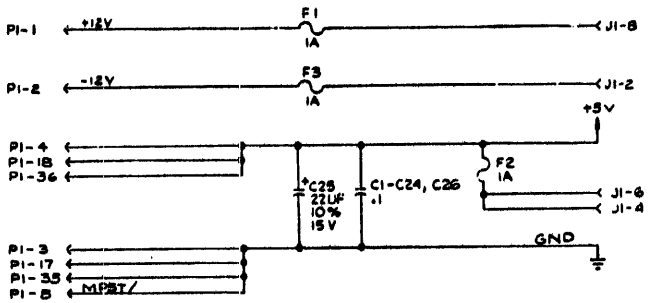
CODE	CHAR	LINE 0	1	2	3	4	5	6	7
25	%	F9	D9	EF	F7	FB	CD	CF	FF
26	&	F7	EB	EB	F3	C5	ED	D3	FF
27	'	F7	FB	FD	FF	FF	FF	FF	FF
28	(	EF	F7	FB	FB	FB	F7	EF	FF
29	)	FB	F7	EF	EF	EF	F7	FB	FF
2A	*	F7	D5	E3	F7	E3	D5	F7	FF
2B	+	FF	F7	F7	C1	F7	F7	FF	FF
2C		FF	FF	FF	FF	FF	F9	F9	FB
2D	-	FF	FF	FF	C1	FF	FF	FF	FF
2E	.	FF	FF	FF	FF	FF	EF	E7	FF
2F	/	FF	DF	EF	F7	FB	FD	FF	FF
30	0	E3	DD	CD	D5	D9	DD	E3	FF
31	1	F7	F3	F7	F7	F7	F7	E3	FF
32	2	E3	DD	EF	F7	FB	FD	C1	FF
33	3	E3	DD	DF	E3	DF	DD	E3	FF
34	4	ED	ED	ED	C1	EF	EF	EF	FF
35	5	C1	FD	FD	E1	DF	DD	E3	FF
36	6	E3	FD	FD	E1	DD	DD	E3	FF
37	7	C1	DD	EF	F7	FB	FB	FB	FF
38	8	E3	DD	DD	E3	DD	DD	E3	FF
39	9	E3	DD	DD	C3	EF	F7	FB	FF
3A	:	FF	FF	E7	E7	FF	E7	E7	FF
3B	;	FF	FF	E7	E7	FF	E7	E7	EF
3C		DF	EF	F7	FB	F7	EF	DF	FF
3D	=	FF	FF	C1	FF	C1	FF	FF	FF
3E		FB	F7	EF	DF	EF	F7	FB	FF
3F	?	E3	DD	EF	F7	F7	FF	F7	FF
40	@	E3	DD	D5	C5	E5	FD	C3	FF

8 x 8 CHARACTER TABLE

CODE	CHAR	LINE 0	1	2	3	4	5	6	7
41	A	F7	EB	DD	DD	C1	DD	DD	FF
42	B	E1	DD	DD	E1	DD	DD	E1	FF
43	C	E3	DD	FD	FD	FD	DD	E3	FF
44	D	E1	DB	DB	DB	DB	DB	E1	FF
45	E	C1	FD	FD	F1	FD	FD	C1	FF
46	F	C1	FD	FD	F1	FD	FD	FD	FF
47	G	E3	DD	FD	FD	C5	DD	E3	FF
48	H	DD	DD	DD	C1	DD	DD	DD	FF
49	I	E3	F7	F7	F7	F7	F7	E3	FF
4A	J	C7	EF	EF	EF	EF	ED	F3	FF
4B	K	DD	ED	F5	F9	F5	ED	DD	FF
4C	L	FD	FD	FD	FD	FD	FD	C1	FF
4D	M	DD	C9	D5	DD	DD	DD	DD	FF
4E	N	DD	DD	D9	D5	CD	DD	DD	FF
4F	O	E3	DD	DD	DD	DD	DD	E3	FF
50	P	E1	DD	DD	E1	FD	FD	FD	FF
51	Q	E3	DD	DD	DD	D5	CD	C3	FF
52	R	E1	DD	DD	E1	F5	ED	DD	FF
53	S	E3	DD	FD	E3	DF	DD	E3	FF
54	T	C1	F7	F7	F7	F7	F7	F7	FF
55	U	DD	DD	DD	DD	DD	DD	E3	FF
56	V	DD	DD	DD	DD	DD	EB	F7	FF
57	W	DD	DD	DD	DD	D5	C9	DD	GG
58	X	DD	DD	EB	F7	EB	DD	DD	FF
59	Y	DD	DD	EB	F7	F7	F7	F7	FF
5A	Z	C1	DF	EF	F7	FB	FD	C1	FF
5B		F1	FD	FD	FD	FD	FD	F1	FF
5C		FF	FD	FB	F7	EF	DF	FF	FF
5D		C7	DF	DF	DF	DF	DF	C7	FF
5E		F7	EB	DD	FF	FF	FF	FF	FF
5F	_	FF	FF	FF	FF	C1	FF	FF	FF
60		FD	FB	F7	FF	FF	FF	FF	FF

CODE	CHAR	LINE 0	1	2	3	4	5	6	7
61	a	FF	FF	F1	EF	E3	ED	E1	FF
62	b	FD	FD	FD	F1	ED	ED	F1	FF
63	c	FF	FF	F3	ED	FD	ED	F3	FF
64	d	EF	EF	EF	E3	ED	ED	E3	FF
65	e	FF	FF	F3	ED	F1	FD	E3	FF
66	f	F7	EB	FB	FB	F1	FB	FB	FF
67	g	FF	FF	E3	ED	ED	E3	EF	EF
68	h	FD	FD	F5	E9	ED	ED	ED	FF
69	i	FF	F7	FF	F7	F7	F7	F7	FF
6A	j	FF	EF	FF	EF	EF	EF	EF	ED
6B	k	FD	F5	F9	FD	F9	F5	ED	FF
6C	l	F7	F7	F7	F7	F7	F7	EF	FF
6D	m	FF	FF	EB	D5	D5	D5	D5	FF
6E	n	FF	FF	F5	E9	ED	ED	ED	FF
6F	o	FF	FF	F3	ED	ED	ED	F3	FF
70	p	FF	FF	F1	ED	ED	F1	FD	FD
71	q	FF	FF	E3	ED	ED	E3	EF	EF
72	r	FF	FF	E5	F9	FD	FD	FD	FF
73	s	FF	FF	E3	FD	F3	EF	F1	FF
74	t	FB	FB	F1	FB	FB	EB	F7	FF
75	u	FF	FF	ED	ED	ED	ED	F3	FF
76	v	FF	FF	DD	DD	DD	EB	F7	FF
77	w	FF	FF	DD	D5	D5	D5	EB	FF
78	x	FF	FF	DD	EB	F7	EB	DD	FF
79	y	FF	FF	ED	ED	ED	E3	EF	EF
7A	z	FF	FF	C1	EF	F7	FB	C1	FF
7B		E7	FB	FB	FD	FB	FB	E7	FF
7C		F7	F7	F7	FF	F7	F7	F7	FF
7D		F3	EF	EF	DF	EF	EF	F3	FF
7E		FF	FF	FB	D5	EF	FF	FF	FF
7F		80	80	80	80	80	80	80	80

***



DEVICE TABLE						
REFERENCE DESIGNATION	DEVICE TYPE	POWER PINS				UNUSED LOGIC ELEMENT OUTPUT PINS
		GND	+5V	+12V	-12V	
U13	74804	7	14			
U14	74128	7	14			
U15-17, U29-31	74LS166	8	16			
U2	74LS174	8	16			
U4, U19	74LS373	10	20			
U1	7451 74	8	16			
U5-12, U21-28	2167	10	20			
U3	82720	20	40			
U18, U20	PAL 16R4A	10	20			
G1	XTAL OSC	7	14			

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE VALUES ARE IN MICROFARADS, +80% -20%, 50V.
2. RESISTANCE VALUES ARE IN OHMS, 1/4W, ±5%.
3. THESE PARTS ARE PROGRAMMED.
4. ODD NUMBERED PINS 7 THRU 25 OF J1 ARE CONNECTED TO GROUND.

REF DESIGNATION	
LAST USED	NOT USED
U31	
C26	
E18	
J1	
P1	
R5	
RP1	
G1	

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ±; .X ±; .XXX ±

ITEM NO. | DESCRIPTION: PARTS LIST

	SIGNATURE	DATE
DRN BY	Ed Turner	7/8/82
CHK BY	V. Engel	9/10/82
ENGR	Dave Hammond	9/10/82
APVD		
APVD		

intel® 3065 BOWERS AVE SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC DIAGRAM
iSBX 275

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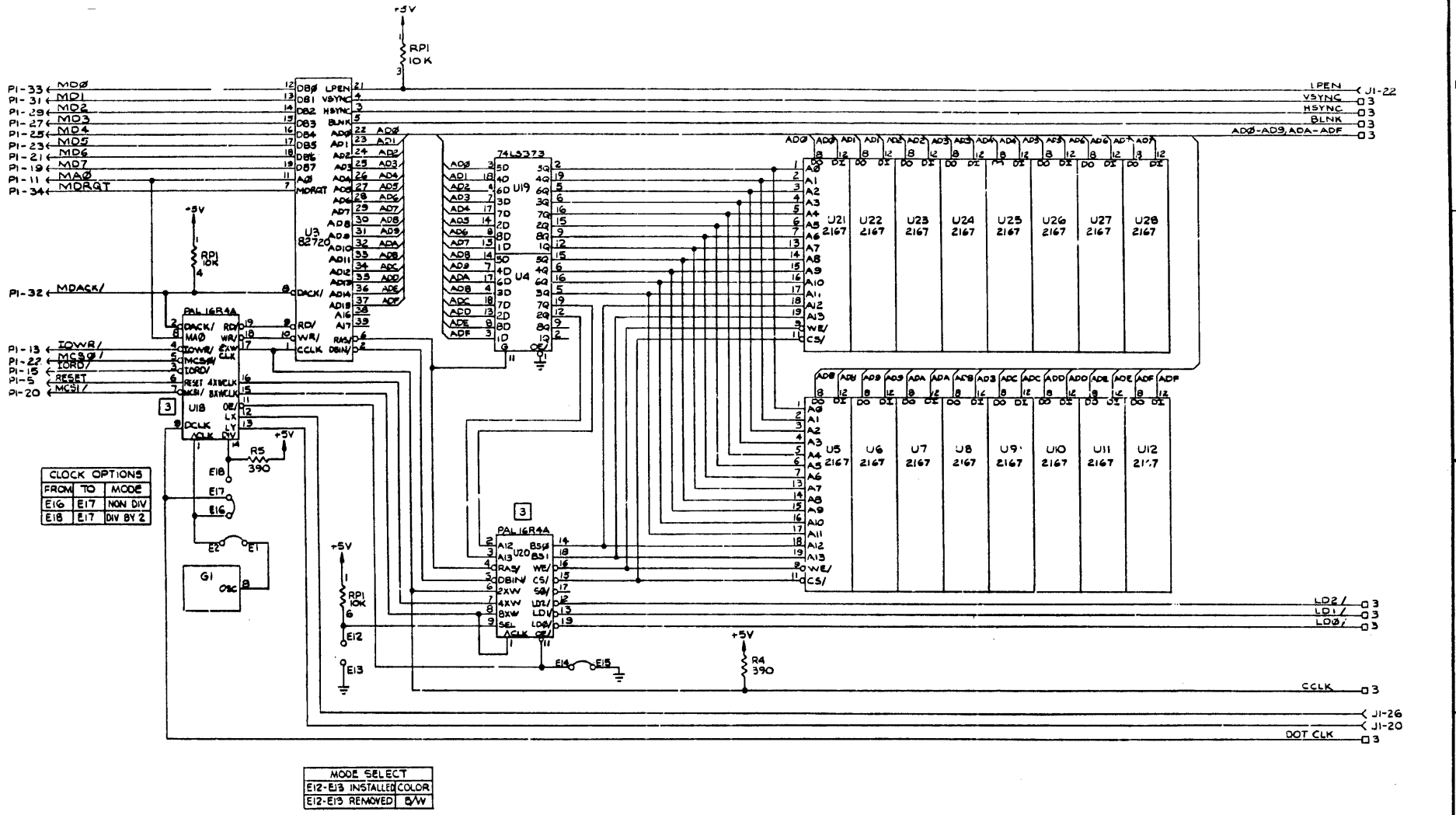

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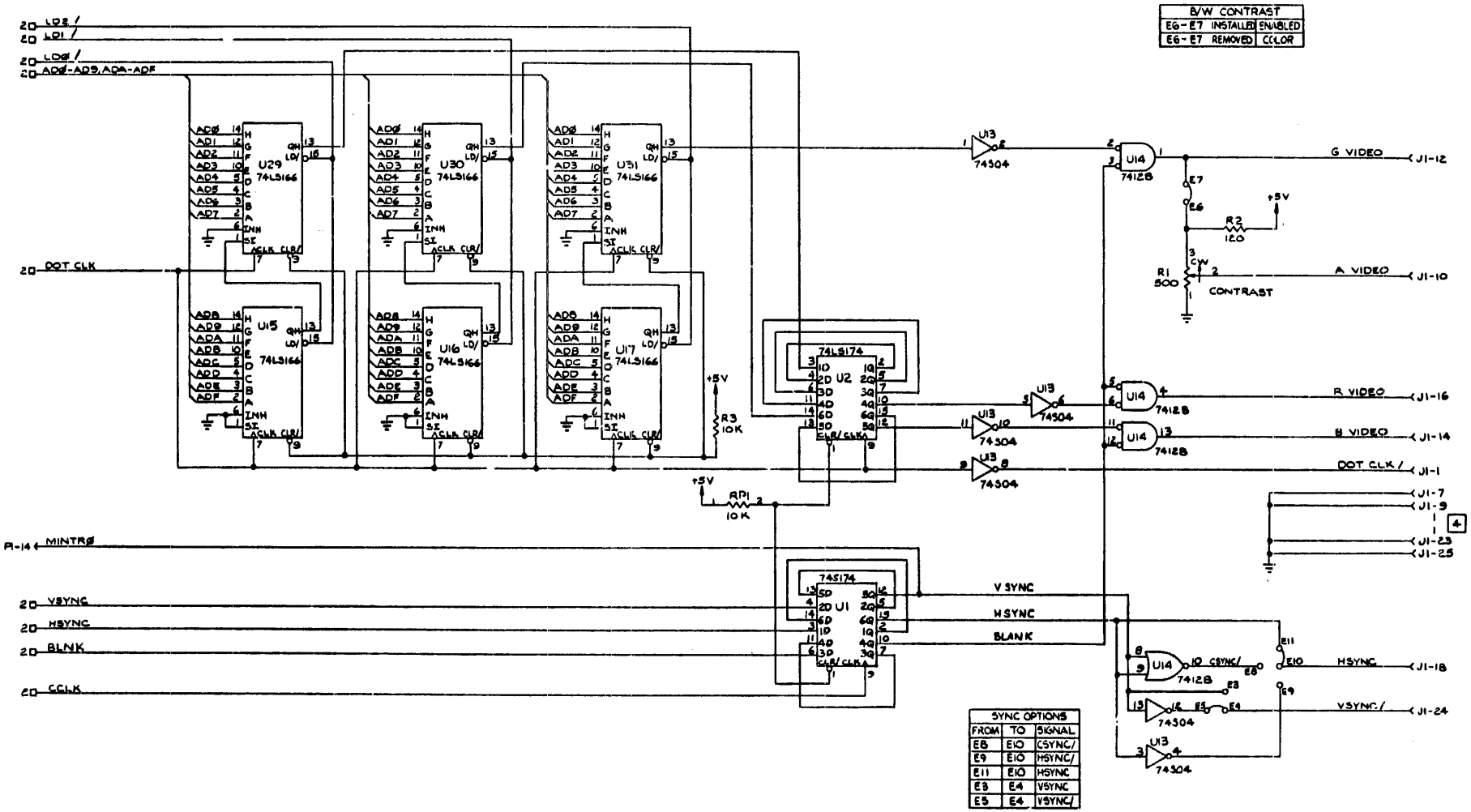

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