M71-304/305

M73-306/307

32KB MEMORY

MAINTENANCE MANUAL

This manual covers the 32KB Memory Modules
used with the Model 7/16 and 7/32 systems.

CONSISTS OF:

INSTALLATION SPECIFICATION	02-340R01A20
MAINTENANCE SPECIFICATION	02-340R01A21
SCHEMATIC	35-473R09D08
SCHEMATIC	35-475R01D08
COMPONENT LOCATOR	35-473M01R09E03

●
INTERDATA®

Subsidiary of PERKIN-ELMER
Oceanport, New Jersey 07757, U.S.A.

M71-304/305

M73-306/307

32KB MEMORY

INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-340 (for 1.0 micro-second operation) and 02-341 (for 750 nanosecond operation) 32KB Memory Modules in INTERDATA Model 7/16 Basic, 7/16 (with HSALU), and 7/32 systems.

Product Numbers M71-304 and M71-305 designate 1.0 microsecond cycle 32KB Memory Modules without parity and with parity respectively for the Model 7/16 Basic, 7/16 (with HSALU), and 7/32 systems. Product Number M73-306 and M73-307 designate 750 nanosecond 32KB Memory Modules without parity and with parity respectively for the Model 7/16 (with HSALU) and 7/32 systems. Refer to the 02-340A21 32KB Memory Maintenance Specification, for details.

2. PHYSICAL CHARACTERISTICS

The 32KB Memory Module consists of one mother-board (approximately 15" x 15") which contains a plug on core stack of 16K words x 17 bits (32K bytes with parity) or 16K words x 16 bits (32K bytes without parity).

3. POWER REQUIREMENTS (MAXIMUM)

Operating	(P15)	2.4 Amperes @ 0°C
	(N15)	2.0 Amperes @ 0°C
	(P5)	3.0 Amperes @ 5.25V
Stand By	(P15)	0.0 Amperes @ 0°C
(each module)	(N15)	0.2 Amperes @ 0°C
	(P5)	2.0 Amperes @ 5.25V

The (N15) and (P15) voltages must be temperature compensated and track within 1%.

4. UNPACKING

When the 32KB Memory Module is shipped with a system, it is installed at the factory and requires no special unpacking procedure. If the module assembly is purchased separately, it should be unpacked carefully and inspected for damage prior to installation.

5. CONFIGURATIONS

5.1 Model 7/16 Basic, 7/16 HSALU, and 7/32

5.1.1 32KB Memory Module Configurations.

The 32KB Memory Module requires on board wiring for address decoding. Address coding and parity strapping options (locations called out on component locator 35-473M01E03) for the 02-340 32KB Memory Module are shown in Functional Schematic 35-473D08, sheet 11. The first 32KB Memory Module (Module 0) in the 7/16 Basic Processor is installed in Slot 5 of the CPU chassis, refer to Table 1. The first 32KB Memory Module (Module 0) in the 7/16 HSALU and 7/32 Processor is installed in Slot 3 of the CPU chassis, refer to Table 4.

The 32KB Memory Module is only installed in 7/16 Basic Processors that have a 35-446R02 (CPU-HI) or higher revision level.

The 32KB Memory Modules can be installed in place of, or with, 8KB (Series 5) Memory Modules and 16KB (Series 6) Memory Modules in the 7/16 Basic and the 7/16 HSALU Processor Systems.

5.1.2 8KB (Series 5), 16KB (Series 6), and 32KB Combination Configurations.

The 8KB (Series 5) and 16KB (Series 6) can be combined with a 32KB Memory Module to add 8KB and/or 16KB to a 32KB boundary. If the total memory configuration will exceed 64KB (two 32KB Memory Modules), 8KB (Series 5) Memory Modules may not be used in that configuration.

On the 7/16 Basic Processor, Slot 5 in the CPU chassis is used for the first 32KB Memory Module. Slot 7 in the Expansion chassis, if required, must be used for the first memory module.

On the 7/16 HSALU and 7/32 Processors, Slot 3 in the CPU chassis is used for the first 32KB Memory Module. Slot 7 in the Expansion chassis, if required, must be used for the first Memory Module.

Memory must be configured in adjacent descending slots on the Model 7/32 Processor system.

The 8KB (Series 5), 16KB (Series 6), and 32KB Memory Modules are configured at the factory per user requirements. Refer to Table 2 for the 7/16 Basic Processor system, and Table 5 for the 7/16 HSALU Processor system.

If the 32KB Memory Module is the expansion to a system already configured, all memory modules that are not 32KB Memory Modules are reconfigured such that they become the top of available memory. Note that if the final memory configuration exceeds 64KB, 8KB (Series 5) Memory Modules may not be used.

Refer to Table 3 for the appropriate slot in which to install 8KB (Series 5) Memory Modules relative to memory address boundaries for the 7/16 Basic Processor system.

Refer to Table 6 for the appropriate slot in which to install 8KB (Series 5) Memory Modules relative to memory address boundaries for the 7/16 HSALU Processor system.

For 7/32 Processor system 8KB (Series 5) Memory Module variations, refer to the 01-087A20 Installation Specification of Model 7/32 Maintenance Manual, Publication Number 29-403 for details.

6. PARITY

Refer to Maintenance Specification 02-340A21. The 02-340F02 denotes a 32KB unit without parity. In this unit all of Bit 17 components are deleted and PAR0 is deactivated by connecting A150-12 to ground. In the 02-340F01 unit, parity (PAR0) is activated by connecting A150-12 to A158-05 and deactivated by connecting A150-12 to ground. PAR0 strapping is done on the solder side.

MODEL 7/16 BASIC, 7/16 (WITH HI-ALU), AND 7/32

TABLE 1
32KB MEMORY MODULE CONFIGURATIONS

MEMORY	MEMORY MODULE	CPU SLOT (S)
32KB	0	5
64KB	1	4 SLOT 5 AND ANY REMAINING SLOT 4:0
—	—	3
—	—	2
—	—	1
—	—	0

NOTES:
1. THE 32KB MEMORY MODULE CAN BE INSTALLED IN MODELS 7/16 AND 7/32 WITH 35-446R02 (CPU-HI) OR HIGHER PRINTED PRINTED CIRCUIT BOARDS

2. THE FIRST 32KB MEMORY MODULE MUST BE INSTALLED IN SLOT 5

3. THE MODEL 7/16 AND 7/32 CPU CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS ARE SHOWN IN TABLE 3

TABLE 2
8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULE COMBINATIONS CONFIGURATIONS

MEMORY	MEMORY MODULE	SLOTS	CPU OR EXPANSION
32KB	1 32KB	5	CPU
40KB	1 32KB 1 SERIES 5	5 1	CPU
48KB	1 32KB 1 SERIES 6	5 4,3,2,1,0	CPU
	1 32KB 2 SERIES 5	5 0-1	CPU
56KB	1 32KB 1 SERIES 6 1 SERIES 5	5 7 5 OR 2	CPU EXPANSION EXPANSION
	1 32KB 3 SERIES 5	5 7-6-5 OR 7-1-2	CPU EXPANSION
64KB	2 32KB	5-4,5-3,5-2,5-1, 5-0	CPU
	1 32KB 2 SERIES 6	5 4-3,3-2,2-1,1-0	CPU
	1 32KB 1 SERIES 6 2 SERIES 5	5 7 5-4 OR 2-3	CPU EXPANSION EXPANSION
	1 32KB 4 SERIES 5	5 7,6,5,4 OR 7,1,2,3	CPU EXPANSION

NOTES:
1. 8KB (SERIES 5), 16KB, (SERIES 6), AND 32KB MEMORY MODULES CONFIGURED AT THE FACTORY PER USER REQUIREMENT

2. SLOT 5 IN THE CPU CHASSIS MUST BE USED FOR THE FIRST MEMORY MODULE

3. SLOT 7 IN THE EXPANSION CHASSIS MUST BE USED FOR THE FIRST MEMORY MODULE, UNLESS THE CPU CHASSIS AND EXPANSION CHASSIS ARE POWERED BY A BULK POWER SUPPLY, INTERDATA PART NUMBER 34-020

TABLE 3
8KB (SERIES 5) MEMORY MODULE BOUNDARIES

SLOT	MEMORY ADDRESS	MEMORY	
5	0000 - 1FFE	8KB	MODEL 7/16
4	2000 - 3FFE	16KB	AND 7/32
3	4000 - 5FFE	24KB	MEMORY ADDRESS
2	6000 - 7FFE	32KB	BOUNDARY SLOT
1	8000 - 9FFE	40KB	DESIGNATIONS
0	A000 - BFFE	48KB	

SLOT	MEMORY ADDRESS	MEMORY	
7	8000 - 9FFE	40KB	
6	A000 - BFFE	48KB	UNIVERSAL
5	C000 - DFFE	56KB	EXPANSION CHASSIS
4	E000 - FFFE	64KB	MEMORY ADDRESS
3	E000 - FFFE	64KB	BOUNDARY SLOT
2	C000 - DFFE	56KB	DESIGNATIONS
1	A000 - BFFE	48KB	
0	8000 - 9FFE	40KB	

NOTES:

1. IF THE 32KB MEMORY IS THE EXPANSION TO A SYSTEM ALREADY CONFIGURED, THE 32KB MEMORY MUST BE IN SLOT 5, THE FIRST 32KB OF CORE ADDRESS, 0000 - 7FFE, IN THE MODEL 7/16 OR 7/32 CPU CHASSIS.

2. SLOT MEMORY ADDRESS BOUNDARY DESIGNATIONS PERTAIN TO 8KB (SERIES 5) MEMORY MODULES ONLY (TABLE 3)

3. REFER TO TABLE 3 FOR THE APPROPRIATE SLOT IN WHICH TO INSTALL 8KB (SERIES 5) MEMORY MODULES RELATIVE TO MEMORY ADDRESS BOUNDARIES. FOR EXAMPLE; FOR 40KB OF MEMORY, ONE 32KB MUST BE INSTALLED IN SLOT 5 AND ONE 8KB (SERIES 5) MUST MUST BE INSTALLED IN SLOT 1 OF THE CPU CHASSIS

3

3A

M71-304/305

M73-306/307

32KB MEMORY

MAINTENANCE SPECIFICATION

1. INTRODUCTION

This specification applies to the INTERDATA 32KB Memories listed in Table 1.

TABLE 1. 32KB MEMORIES

INTERDATA PART NUMBER	PRODUCT NUMBER	SPEED	SIZE	CONFIGURATION
02-340F01 (35-473F03)	M71-305	1.0 us	32KB	16K x 17*
02-340F02 (35-473F04)	M71-304	1.0 us	32KB	16K x 16
02-341F01 (35-473F01)	M73-307	750 ns	32KB	16K x 17*
02-341F02 (35-473F02)	M73-306	750 ns	32KB	16K x 16

*The seventeenth bit is a parity bit.

2. SCOPE

This specification describes the operation of the 32KB Memory, the inputs necessary to operate the memory, and the resultant outputs provided by the memory. A brief review of core memory theory precedes the detailed circuit description. This specification also provides a block diagram analysis, timing information, troubleshooting and maintenance information, and a mnemonic list.

3. PHYSICAL DESCRIPTION

The 32KB Memory consists of one mother-board (approximately 15" x 15") that can be installed in a card file on 0.75 inch centers. The 35-473M01E03 32KB Memory Component Locator shows address, parity and cycle time strapping locations, test points, etc. A back panel map is shown in Functional Schematic 35-473D08, Sheet 1.

4. BASIC CORE MEMORY THEORY

This memory is wired in a coincident current, 3D, 3 wire configuration. The core orientation and wiring is illustrated in Figures 1 and 2. Figure 1 shows the X and Y wiring for the 16K x 17 bit stack. Figure 2 shows how the inhibit winding is strung on a set of 64 Y lines to obtain an 8K matrix (64 Y by 128 X lines). Each bit has two inhibit windings.

As shown in Figure 1, the direction of X read current is always from the X drive (X00:127) to the X sink (XC00:127). The direction of Y Write current is always from the Y drive (Y00:127) to the Y sink (YC00: 127). The orientation of the core is changed from bit to bit to arrange coincidence in the core. In Figure 2, the direction of inhibit current is from the inhibit end (IA or IB) to the sense end (SA and $\overline{SA}$ or SB and $\overline{SB}$). Inhibit current is in the same direction as Y Write current.

A core is switched by applying one-half the current necessary to switch the core, to each of the selected X and Y drive lines. One core in each bit plane is thereby addressed. During a Read operation, current in the drive lines is such as to force the cores to the ZERO state. Nothing occurs in any core which is already in the ZERO state. However, if a core is in the ONE state, the core switches. When the core changes state, a signal is induced in the sense winding of that bit plane. The induced signal is used to generate a ONE indication for that bit position. During a Write operation, current flow is in the opposite direction in the drive lines, which tends to force the cores to the ONE state. An opposing current to the Y axis current is applied to the inhibit winding for each bit plane which is to remain at ZERO.
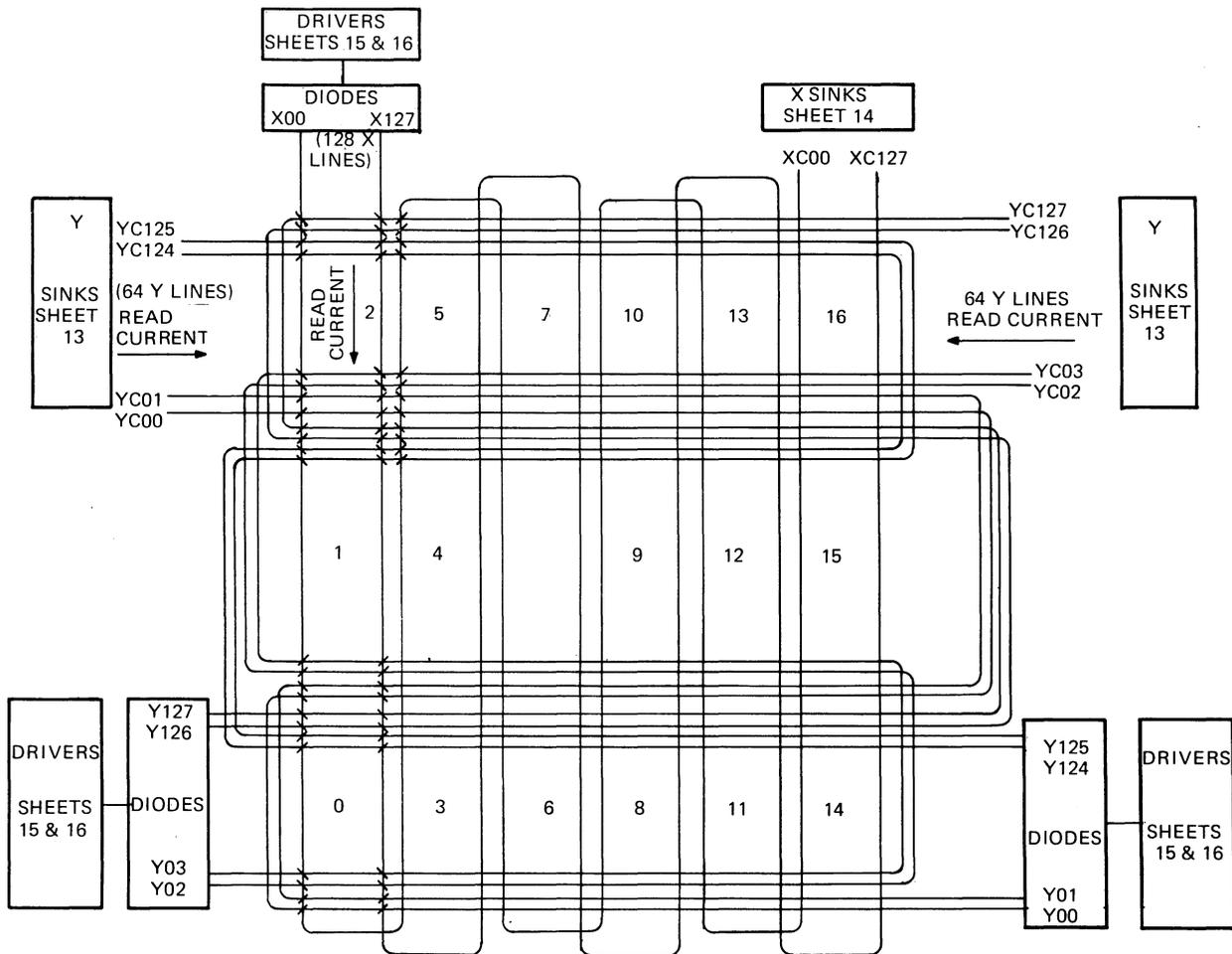
CORE ORIENTATION SHOWN FOR BIT 0
IS TYPICAL FOR 0, 2, 4, 6, 7, 8, 10, 12, 14, 16,

CORE ORIENTATION SHOWN FOR BIT 1
IS TYPICAL FOR 1,3,5,9,11,13,15

Figure 1. X and Y Core Plane Wiring
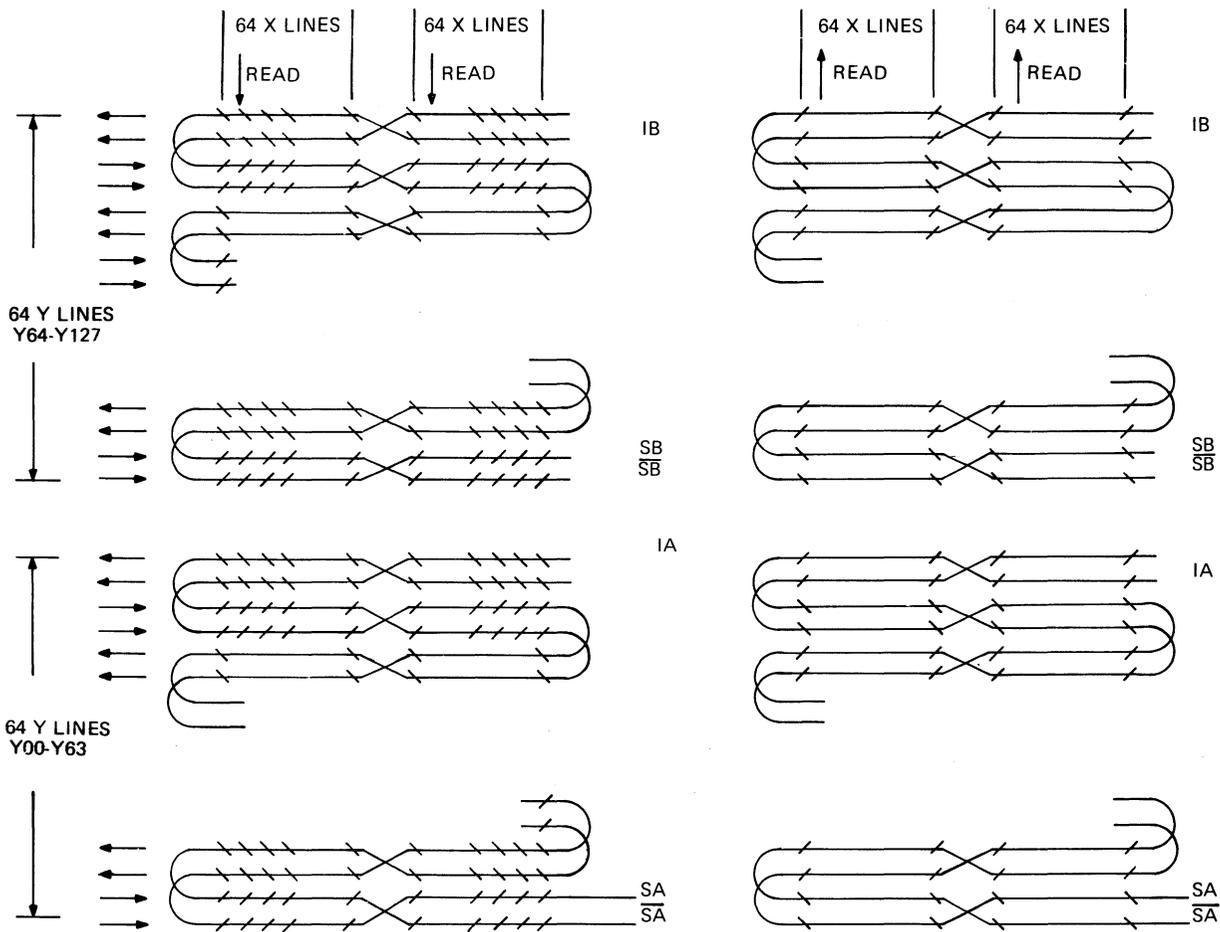
Figure 2. Sense-Inhibit Wiring

5. MEMORY CONFIGURATION

Eight bi-polar X sink switches and eight bi-polar Y sink switches share 16 bi-polar drive switches such that an 8 x 16 decode matrix controls read and write current in 128 X lines and an 8 x 16 decode matrix controls read and write current in 128 Y lines. The shared drive switch scheme is illustrated in Figure 3. The 32 drive switches are controlled by memory addresses and the Read/Write control lines such that the appropriate polarity switch is used for a given operation. For any memory operation, six switches must be turned on; an X sink switch, a Y sink switch, a positive drive switch (X or Y, emitter connected to diodes), and a negative drive switch (X or Y, collector connected to diodes). The X sink is negative for read and positive for write. The Y sink is positive for read and negative for write. Once the selected sink and drive switches are activated the X and Y current sources are then turned on. This is repeated for both the read and write phases of a memory cycle.

6. BLOCK DIAGRAM ANALYSIS

6.1 Timing and Control

Figure 4, the block diagram of the memory, illustrates that the timing and control section contains many inter-related circuits which are used to control the timing of the stack currents. A strap option of addresses MA000, MAX070, and MAX060 and their complement provides for a one out of eight module select. Refer to Functional Schematic 35-473D08, Sheet 11. Early Read (ER0) initiates the memory read phase and Inhibit (INH0) initiates the memory write phase of a memory cycle. The timing is independent of the width of ER0 and INH0. Some addresses are combined with timing pulses in the timing and control section to provide an additional level of decode. For example, the stack is wired such that one 8K bit sense-inhibit is strung on the first set of 64 Y lines, and the other 8K bit sense-inhibit is strung on the second set of 64 Y lines. MA010 and MA011 are used to select the sense strobe and inhibit timing pulses for the first and second 8K bit respectively and to control the selection of the first 64 Y lines and the last 64 Y lines respectively.

Y SINKS

TO 13 MORE EMITTERS   TO 13 MORE COLLECTORS

X SINKS

A

X READ OR Y WRITE DRIVE SWITCHES

①

Y READ OR X WRITE DRIVE SWITCHES

B

A

②

B

A

YRC0 OR XWC0

③

B

XRC1 OR YWC1

+SKV

P15

−SKV

N15

① ② ③

THESE SWITCHES ARE TURNED ON IN PAIRS
IF 1A IS ON FOR READ, 1B IS ON FOR WRITE
IF 1B IS ON FOR READ, 1A IS ON FOR WRITE
THIS APPLIES FOR 2, 3, ETC.

NOTE THAT FOR ANY READ, AN "A" SWITCH
IS ON FOR X AND A B SWITCH IS ON FOR Y.

Y READ   X WRITE   X READ   Y WRITE

5W   5W   5W   5W

N15

P15

Figure 3. Shared Drive Switches

4

Figure 4. System Block Diagram

6.2 Drive Switch Sharing and Sink Switches

The mechanics of switch sharing is accomplished by OR-tying the outputs of the X and Y drive switch decoders (Sheets 15 and 16). Positive switch decoders (emitter connected to diodes) serve both X Read drive and Y Write drive switches. Negative switch decoders (collector connected to diodes) serve both X Write drive and Y Read drive switches.

For example, MA070:090 and RXDTA0 or RXDTB0, produced by MA100 ANDed with the Read Timing signal (RT1), controls the selection of the one of 16 positive switches for X read. MA110:130 and WYDTA0 or WYDTB0, produced by MA010 ANDed with the Write Timing signal (WT1), controls the selection of the same switch for Y Write. The same switch is used for both X Read and Y Write during a cycle. The Write Timing signal (WT1) selects a negative X switch that complements the positive Read switch. Figure 3 illustrates the switch sharing. The X sink uses MA020 and 140; Write Timing signal (WT0); and XSTA0 or XSTB0, produced by MA030 ANDed with Sink Timing signal (SKTA), to select one of eight bi-polar X sink switch pairs. The Y sink uses MA040 and 050; Write Timing signal (WT1); and YSTA0 or YSBT0, produced by MA060 ANDed with SKTA, to select one of eight Y sink switch pairs.

6.3 Drive Current Timing and Amplitude

The X and Y current switches Q65, Q66, Q67, and Q68 (Sheet 17) are controlled by RT1 and $\overline{Q5}$, Q1, XRCT1, and Q1 respectively which are generated by the timing and control section. These signals control the width of the X and Y currents, while four 5 watt resistors determine their amplitude. Y Read current (YRCS0) (17E1) with X Write current (XWCS0) (17E1), and X Read current (XRCS1) (17L1) with Y Write current (YWCS1) (17L1) are switched through separate balun transformers.

6.4 Inhibit

Each bit is write controlled by two separate inhibit windings, one for each 8K bit section. The selection of the inhibit winding is controlled by MA010. The 17 Memory Data (MD) lines determine whether a ONE or a ZERO is to be written into each bit.

6.5 Sense

The sense section contains 17 dual sense amplifiers. Each dual amplifier senses one bit. The strobe timing signals SAS11 or SAS21 select one of two amplifiers as dictated by MA010.

7. CIRCUIT DESCRIPTION

7.1 Introduction

This section describes the circuits shown in Functional Schematic 35-473D08. The zone location of components referenced in the following descriptions are provided in parentheses after the circuit designation of signal mnemonic. Throughout the following discussion, signals on the memory interface bus are considered positive true (i.e., logical 1 = high $\geq$ +2.5V and logical 0 = low $\leq$ +0.4V. However, as indicated by the mnemonics, the signals on the bus are inverted.

7.2 Timing and Control Circuits

Timing is shown in Figure 5. ER0 initiates the Read phase and INH0 initiates the Write phase of a memory cycle. A counter, driven by a delay line oscillator, is used to generate the timing intervals during which the X and Y drive, as well as the sink and current switches are activated. Other timing such as Inhibit pulse width (INHT11 and INHT21) (11L6) and sense strobe pulse width (SAS11 and SAS21) (11L7) are controlled by one-shots. The timing diagram shown in Figure 5 is for both the 750 and 1000 nanosecond cycle options. INH0 for 750 nanosecond cycle occurs no later than To +350 nanoseconds, while for 1 microsecond operation, INH0 occurs no later than To +420 nanoseconds. In either case, during a Read-Restore operation, the MS Bus is valid from To +275 nanoseconds to To +420 nanoseconds, and during a Clear-Write operation, the MD Bus is valid at the start of INH0 and thereafter for a minimum of 300 nanoseconds.

Refer to Sheet 11 of Functional Schematic 35-473D08 and Figure 5. The Read phase is initiated when the unit select line at Gate A138-2 (11D7) is high and ER0 (11A2) is set true.

.750 US CYCLE SCALE

| T$_0$ | 100 | 200 | 300 | 325 | 400 | 500 | 600 | 700 | 800 |

MAXXX   0

VALID

ER0   300/80*

RT1   20/15   260/250

CLK

Q1   55/45   100/80

235/220   280/260

Q2   95/85   145/125

Q3

Q4   275/260   325/305

$\overline{Q5}$

0

INH0   350/330   350/80

RBSY1   65/55   310/95

WBSY1   110/90   360/95

WT1   20/15   300/285

SKTA   30/25   270/260   30/25   310/295

XRCT1   105/95   245/235

SAS   240/230

CLR0   **   420/390

MS BUS   275/250   420/400   MD BUS

MS BUS VALID   MD BUS VALID

420 MAX.

NOTES:
* MAXIMUM/MINIMUM
** SEE SECTION 12.5

0
1 US CYCLE SCALE

| T$_0$ | 100 | 200 | 300 | 420 | 500 | 600 | 700 | 800 | 900 |

Figure 5. Timing Diagram

RT1 (11H2) is generated for a period determined by Resistor R110 and Capacitor C59 (11F4). The counter (A142, A143, and A146) is incremented for an interval determined by the width of RT1, and at a frequency controlled by delay line A140 (11L4) and driver A147 (11L4). The two flip-flops at 11C3 and 11C5 inhibit re-triggering of the Read and Write timing circuits should ER0 or INH0 extend beyond the time to complete a cycle. In addition, a Memory Busy signal (MBSY1) (11R7) is set at the beginning of Read and reset at the end of Write, indicating that a memory cycle is in process. The subsequent Write phase is initiated by INH0. When INH0 is set true, WT1 is generated for a period determined by Resistor R109 and Capacitor C58 (11F2). RT1 and WT1 circuits are interlocked to prevent sink switch burn out. INHR1, INHT11, and INHT21 (11K6) are inhibit timing signals and are discussed in Section 9.

7.2.1 Read Timing (RT1). RT1, which controls the Read phase of the memory cycle, generates the timing signals which control the sequence of switch turn on and turn off and also the timing and width of the sense strobe as follows:

1. Generates RXDTA0 (12F2) or RXDTB0 (12D2) and XSTA0 (12F6) or XSTB0 (12F6). These determine the timing of the X current drivers and X current sink switches respectively. Simultaneously RYDTA0 (12G4) or RYDTB0 and YSTA0 (12G7) or YSTB0 (12G7) are also generated which determine the timing of the Y current drivers and Y current sink switches respectively.

2. During the interval that the decoded current driver (Sheets 15 and 16) and sink switches (Sheets 13 and 14) are on, the current sources are turned on and off by signals from RT1 and from the timing counter (Q1, XRCT1, and Q5) (Sheet 11). Refer to Sheet 17.

3. Generates CLR0 (12N4) and SAT (12R6). CLR0 determines the width of the data pulse on the MS Bus, while SAT generates one of two sense strobes SAS11 or SAS21 (Sheet 11) as determined by address MA010.

7.2.2 Write Timing (WT1). WT1, which controls the Write phase of the memory cycle, generates the timing signals which control the sequence of switch turn on and turn off and also the timing and width of the sense inhibit as follows:

1. Generates WXDTA0 (12G3) or WXDTB0 (12G3) and XSTA0 (12G6) or XSTB0 (12G6). These determine the timing of the X current drivers and X current sinks respectively. Simultaneously WYDTA0 (12G5) or WYDTB0 (12G5) and XSTA0 (12G6) or YSTB0 (12E7), are also generated, which determine the timing of the Y current drivers and Y current sinks switches respectively.

2. During the interval the decoded current driver (Sheets 15 and 16) and sink switches (Sheets 13 and 14) are on, the current sources are turned on and off by signals from the timing counter (Q1) (Sheet 11). Refer to Sheet 17.

3. Generates Inhibit control pulses INHT11 or INHT21 as determined by MA010, and also the Inhibit rise time (INHR1) control whose width is determined by Resistor R108 and Capacitor C57.

8. DECODE AND DRIVE CIRCUITS

The timing and control circuits, already described, provide a series of timing delays and sequences which perform the required core switching function. The following section describes this function.

When timing signals are applied to decoded switches they are activated and provide a pair of closed paths through one X wire and one Y wire. Current is then passed from the drive current sources to the selected lines and back to the current sources. The organization of the X and Y matrices is shown in Figures 6 and 7 in simplified form. Since the two matrices (X and Y) are identically organized the following description is limited to the operation of the X matrix.

Memory Addresses MA071:090 together with RXDTA0 (Read X Driver Timing A) for read and WXDTA0 for Write are inputs to the two one-out-of-eight Read/Write drive switch decoders A95 and A90. Address MA021, MA141, XSTA0 together with WT0 for Read and WT1 for Write are inputs to a one-out-of-four Read/Write sink switch pair decoder. During the Read phase, RXDTA0 and XSTA0 are supplied simultaneously to turn on drive switch QM93 and sink switch QM126. Approximately 40 nanoseconds later XRCT1 (X Read) Current Timing) is applied to A125 (17J4) to turn on current source switch Q67 (17L5). At this point Read current, whose amplitude is determined by Resistor R128 (17L5), is switched from P15 through the Read balun T48 (17M2) and drive switch QM93 (15J2) into line X000 and back through sink switch QM126 (14E2) and balun T48 to N15. The Read current is later terminated by XRCT1 followed in 40 nanoseconds by the end of RXDTA0 which turns off switches QM93 and QM126. Once all Read currents and voltage transients have settled the Write phase can begin. Write current, in the opposite direction through line X000, is generated and steered as a result of applying WXDTA0, XSTA0 and Q1 to operate drive switch QM87 (15R1), sink switch Q126 (14E2) and current switch Q66 (17L5) respectively, in the same relative time sequence described for the Read phase. Damaged cores or drive lines may be located with the use of tables on Figures 6 and 7 once the failing addresses are determined.
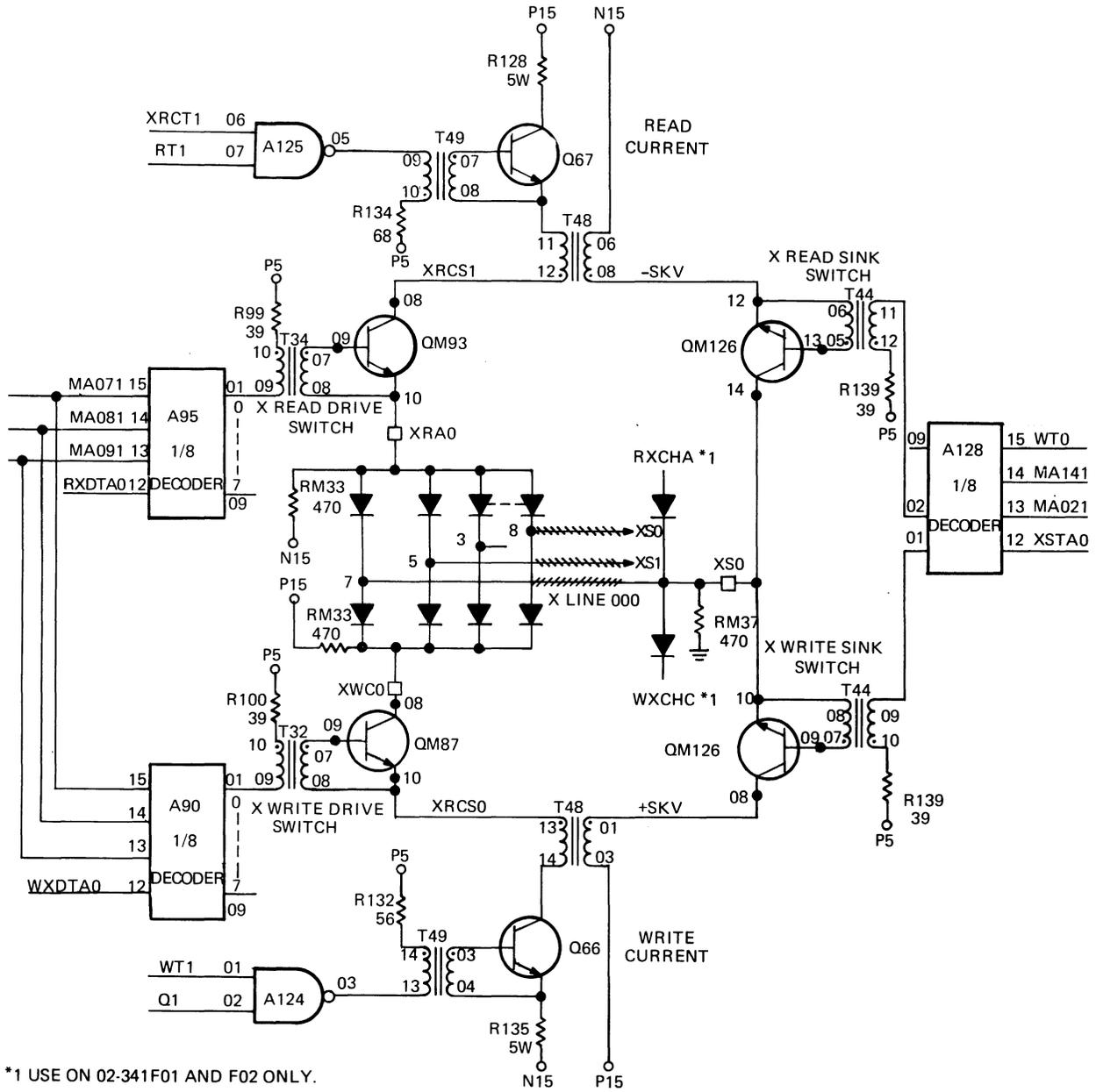
*1 USE ON 02-341F01 AND F02 ONLY.

32KB CORE MEMORY X LINE DECODE

XSTA0 - MA030 = 0
XSTB0 - MA030 = 1
RXDTB0 + WXDTB0 - MA100 = 0
RXDTA0 + WXDTA0 - MA100 = 1

					MA020	0	0	0	0	1	1	1	1
					MA030	0	0	1	1	0	0	1	1
					MA140	0	1	0	1	0	1	0	1
MA070	MA080	MA090	MA100	XWC/XRA		XS4	XS5	XS0	XS1	XS6	XS7	XS2	XS3
1	1	1	1	15		119	117	126	124	115	113	122	120
1	1	1	0	7		55	53	62	60	51	49	58	56
1	1	0	1	11		87	85	94	92	83	81	90	88
1	1	0	0	3		23	21	30	28	19	17	26	24
1	0	1	1	13		104	106	97	99	108	110	101	103
1	0	1	0	5		40	42	33	35	44	46	37	39
1	0	0	1	9		72	74	65	67	76	78	69	71
1	0	0	1	1		8	10	1	3	12	14	5	7
0	1	1	1	14		118	116	127	125	114	112	123	121
0	1	1	0	6		54	52	63	61	50	48	59	57
0	1	0	1	10		86	84	95	93	82	80	91	89
0	1	0	0	2		22	20	31	29	18	16	27	25
0	0	1	1	12		105	107	96	98	109	111	100	102
0	0	1	0	4		41	43	32	34	45	47	36	38
0	0	0	1	8		73	75	64	66	77	79	68	70
0	0	0	0	0		9	11	0	2	13	15	4	6

Figure 6X. Drive Line Table and Selection Scheme

YSTA0 - MA060 = 1
YSTB0 - MA060 = 0
RYDTB0 + WYDTB0 - MA010 = 0
RYDTA0 + WYDTA0 - MA010 = 1

32KB CORE MEMORY Y LINE DECODE

					MA040	0	0	0	0	1	1	1	1
					MA050	0	0	1	1	0	0	1	1
					MA060	0	1	0	1	0	1	0	1
MA010	MA110	MA120	MA130	YWA/YRC		YS0	YS4	YS2	YS6	YS1	YS5	YS3	YS7
1	1	1	1	15		126	111	118	103	122	107	114	99
1	1	1	0	11		67	32	75	90	71	86	79	94
1	1	0	1	13		124	109	116	101	120	105	112	97
1	1	0	0	9		65	80	73	88	69	84	77	92
1	0	1	1	14		127	110	119	102	123	106	115	98
1	0	1	0	10		66	83	74	91	70	87	78	95
1	0	0	1	12		125	108	117	100	121	104	113	96
1	0	0	0	8		64	81	72	89	68	85	76	93
0	1	1	1	7		62	47	54	39	58	43	50	35
0	1	1	0	3		3	18	11	26	7	22	15	30
0	1	0	1	5		60	45	52	37	56	41	48	33
0	1	0	0	1		1	16	9	24	5	20	13	28
0	0	1	1	6		63	46	55	38	59	42	51	34
0	0	1	0	2		2	19	10	27	6	23	14	31
0	0	0	1	4		61	44	53	36	57	40	49	32
0	0	0	0	0		0	17	8	25	4	21	12	29

Figure 7. Y Drive Line Table and Selection Scheme

10

9. DATA LOOP CIRCUITS

The data loop section includes the circuits used to control the inhibit current, the inhibit current drivers, the sense amplifier, and the MS Bus drivers. The data loop section is shown on Sheets 2 through 10. The inhibit circuits employ the same circuit for all bits, however, Bits 0:8 are driven from N15 while Bits 9:16 are driven from P15. The Inhibit current is generated by two timing pulses INHT11 or INHT21 and INHR1 which control its duration and amplitude respectively. INHR1 (2B4), a 60 nanosecond pulse, is generated by the leading edge of INH0. This pulse causes T10 (Sheet 2) to operate as a 1:1 transformer. As in the case of Bit 16 (Sheet 2) Transistors Q5, Q6, Q7 and Q8 are turned on. INHT11 and INHT21, the Inhibit duration timing pulses, are controlled by MA010 and MA011 (11A8) respectively. Note that INHT11 selects the first 8K sense/inhibit and INHT21 selects the second 8K sense/inhibit. The "Inhibit Shut Down" circuit contains three transistor clamps which are activated by the System Clear signal (SCLR0) (Sheet 11). The clamps are applied to the INHT11, INHT21, and WT1 signals during the power turn ON/OFF periods to prevent spurious triggering of the Inhibit Transistor Drivers.

9.1 Write Phase

Assume that MA010 is false and a ZERO is to be written into Bit 16. MD160 (2C1) is high so Gate A4-5 (2E1) goes low and current flows through Resistor R14 (2F1) and T1-16 and 15 (2F1), turning on Q22 (2G1). Current now flows from P15 (2G1) through T15-13 and 14, Diode D2, and Transistor Q5 to ground. No current flows in T15 (2G2) Terminals 15 and 16 because the current through Terminals 13 and 14 causes a positive voltage at Terminal 15 with respect to Terminal 16 and Diode D1 is reverse-biased. As current develops through Terminals 13 and 14, current is also induced in the secondary winding. The direction of current flow is from Terminal 3 to Terminal 1, through the inhibit winding, to $\overline{SB16}$ and SB16, Diodes D104 and D105 and back to Terminal 3. The transformer turns ratio at this time is 1:1 (see Figure 8). After 60 nanoseconds the current has reached the required amplitude and Transistor Q5 is turned off. Current must now flow from P15 through Q22, and through both Primary windings of T15 and Diode D1 to ground. The effective turns ratio on T15 is now 3:1 and the applied voltage to the secondary is reduced accordingly, but the current present when Transistor Q5 turned off is maintained for the duration of INHT11. After INHT11 times out, Q22 is turned off and the Inhibit current drops to zero. Diode D3 (2G2) clamps the recovery voltage to protect Q22. The secondary winding (Terminals 1 and 3) recovers into P5 and the inhibit line recovers through Resistor R25 (2H2) and the 100 ohm inhibit termination resistor in module RM1 (2J3).

N2 = 16 TURNS
N1 = 8 TURNS
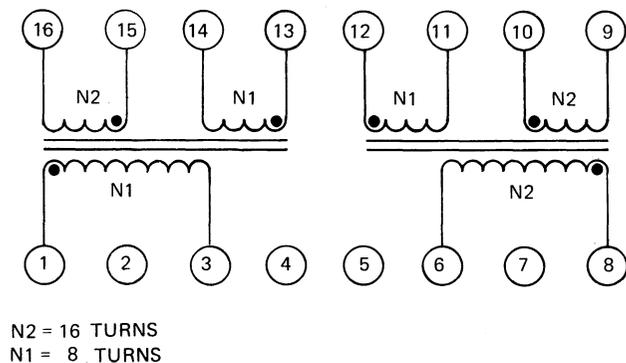
Figure 8. Inhibit Drive Transformer

9.2 Read Phase

During a Read time, a signal on the sense line is terminated by the 120 ohm resistors. The signal is amplified to a TTL level by the sense amplifier. The state of MA010 determines which 8K section of the bit plane is to be read out and SAS11 or SAS21 is generated accordingly. CLR0 is raised to a logic ONE level during strobe time and is held for 130 nanoseconds. If a ONE is read from the stack the sense amplifier latches for the duration of CLR0.

The Data Out Gate (DOG1) is normally high and is forced low whenever the Processor asserts WRT0 thereby preventing Read data from appearing on the MS Bus when a Clear-Write cycle is performed on the 02-341F01 and F02 (this function is not strapped in the 1.0 microsecond cycle option, 02-340F01 and F02). The 2.15K resistor in parallel with the 2K resistor in each resistor module establishes an approximate 100:1 ratio between V_T and the actual voltage at the input of the threshold amplifier. Provisions are made to monitor and adjust V_T.

10. TEMPERATURE TRACKING

The memory has a Thermistor (Rt1) mounted between back panel Terminals 128-1 and 227-1. The Thermistor is a temperature sensitive resistor which connects to the -16.5 volt power supply. The +16.5V supplies vary inversly as the temperature varies. At 0°C the supply voltages are approximately 18.00 volts; at 50°C the supply voltages are approximately 15.00 volts.

11. TESTPOINTS

Table 2 lists the test points and their corresponding location on the functional schematic.

TABLE 2. TEST POINT LOCATIONS

Test Point	Function	Location
TP1 INHR0	Inhibit pulse rise time	2D3
TP2 INHT11	Inhibit pulse duration timing	3D6
TP3 V_{TH}	Relative threshold voltage	2L1
TP4	Sense threshold auxiliary circuit	2L1
TP5	Sense threshold auxiliary circuit	2L1
TP6 GRD	Sense threshold auxiliary circuit	2B7
TP7 GRD	Sense threshold auxiliary circuit	2B7
TP8 GRD	Sense threshold auxiliary circuit	2B7
TP10 SAS11	Sense amplifier strobe (for sense strobe presence only)	2N5

12. TESTS AND ADJUSTMENTS

The timing of the sense amplifier strobe, the setting of the sense threshold voltage (V_{TH}), and the basic memory timing are adjustable. They are all set to exact standards at the factory. These setting or adjustments are not likely to change except for a circuit malfunction. However, a memory suspected of being marginal may be checked in the following manner:

1. Ensure that +5V is within the range of 4.9 to 5.1 volts.

2. Ensure that P15 and N15 are tracking according to the graph in Figure 9.

3. Compare the timing of RT1, WT1, INHT11, INHT21, INHR1 and XRCT1 with the timing diagram, Figure 5. If it is not the same (± 10 nanoseconds), their respective one-shots are defective. If XRCT1 is incorrect the problem may be with delay line driver A147 (11K4) or receivers A159 and A154 (Sheet 12).

4. Check the timing of the leading and trailing edges of Q1 with respect to the leading edge of ER0 at A162-3. These should be 50 nanoseconds and 230 nanoseconds respectively ±5 nanoseconds, adjust jumper W1 (11L4) until it is within this range. If it can't be met, the oscillator circuit is defective.

5. Check the timing of SAS11 or SAS21 with respect to the leading edge of XRCS1 at the -15 V level. If it is not 110 nanoseconds (±3 nanoseconds), adjust Resistor R10 using an extender board. (Sense strobe is measured on A75-11 with respect to XRCS1 at T48-12.) Also check the timing of CLR0 with respect to SAS11 or SAS21. This should be high during SAS and low again at 420 nanoseconds following ER0.

6. While running the memory test, vary Resistor R88 so that V_{TH} at TP3 is adjusted over the range of 1.15 to 2.65 volts. If the memory passes this test the problem is not in the sense circuits. If memory fails the test, troubleshoot the device circuits.

12 B
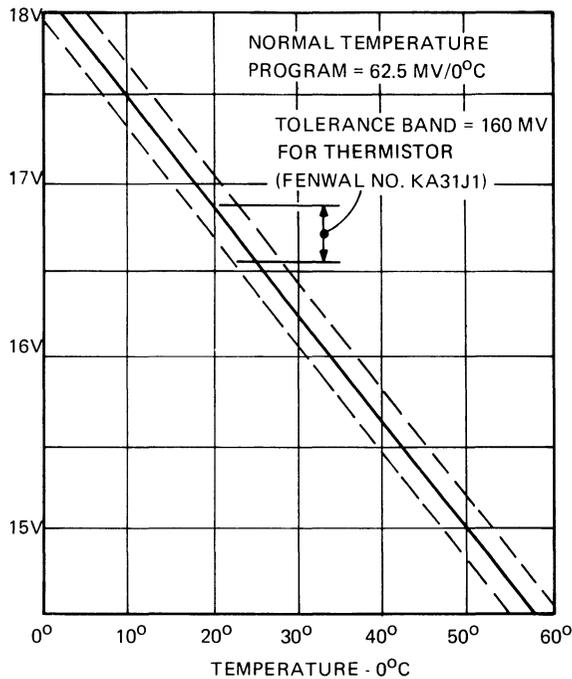
Figure 9. Thermistor Temperature Program

13. TROUBLESHOOTING

Because of the many types of failures possible, a careful diagnosis is important. First determine whether or not the memory can be written into and read from. The problem should fall into one of four main categories:

1. Fails all bits, all addresses.

    a. Will not read "ones".
    b. Will not read "zeros".

2. Fails all bits, some addresses.

3. Fails one or more bits, all addresses.

4. Fails some bits, some addresses.

Of the four categories, 1, 2, and 3 are classified as failures where the faulty circuit can be found by referring to the troubleshooting chart. Category 4 may require analysis of waveforms and failure conditions. The troubleshooting analysis chart should be used as an aid in diagnosing the problem and isolating the faulty circuit in any of the four categories.

A preliminary check should include the following steps:

1. Verify that P5, V_T, P15, and N15 are within limits.

2. Write all ONES into an address.

3. Read this address. If all ones are read, go to Step 4. If all bits are ZEROS, look for something such as the memory not being selected or a broken connection at one of the four 5W resistors or the associated transistor (Q65:Q68). Also examine the timing to determine if the timing pulses are occurring in the proper sequence. If some bits are ZEROS, note them and troubleshoot the associated circuits using the troubleshooting chart.

4. Write all ZEROS into an address.

5. Read the data at this address. If all bits are ZEROS, go to Step 6. If all bits are ONES, it indicates that the inhibit timing circuits are not functioning. If some bits are ONES, note them and troubleshoot the associated circuits using the troubleshooting chart.

6. Write all ONES at all addresses.

7. Read all addresses. If all ONES are read at all addresses, go to Step 8. If not, notice the type of failure:

    a. All bits fail, some addresses.
    b. Some bits fail, some addresses.
Select the proper section of the chart.

8. Write all ZEROS at all addresses.

9. Read all addresses. If all ZEROS are read go to Section 12. If some bits are ONES at some addresses, it indicates that the sense amplifier strobe is misadjusted, or V_T is misadjusted, or there is too much drive current because of a short, or P15 and/or N15 are too high. It is also possible that one sense amplifier or the associated circuit is marginal, but do not suspect this if more than one bit is failing in this manner.

10. Go to Section 12.

TROUBLESHOOTING ANALYSIS CHART

SYMPTOM	POSSIBLE TROUBLE	POSSIBLE SOLUTION
Fails all bits, all addresses Does not read ones	P5, P15, N15 or V_T not present or misadjusted.	Refer to Section 12.
	Unit selected, memory timing, Write Busy or Read Busy circuits malfunctioning, or sense amplifier strobe timing misadjusted.	Check TP1 and TP10 (see schematic, Sheets 2 and 11).
	No drive current. One of the circuits on Sheet 17 or Functional Schematic 35-473D08 has failed.	See Section 12. Check the waveforms "YRCS0 or XWCS0" and "XRCS1 or YWCS1" and compare with Figures 10 and 11.
Does not read zeros.	Inhibit circuits malfunctioning.	Check TP2 while the memory is addressed and MA010 is reset. If no signal is present, see schematic Sheet 11 and Section 9.
Fails all bits, some addresses	Drive circuits malfunctioning.	Try to spot a commonality of addresses (see Figures 6 and 7). Monitor the voltage at XRCS1 or YWCS1 (17L1) and compare it with Figure 11.
Fails some bits, all addresses. Does not read ones	Sense circuits malfunctioning (rarely more than one circuit). V_T misadjusted. Sense amplifier strobe maladjusted. MA driver chip bad.	Note which bits are failing and compare waveforms with Figures 21:23.
Does not read zeros	Inhibit circuit malfunctioning.	Troubleshoot the bad bit comparing waveforms with Figures 22:23.
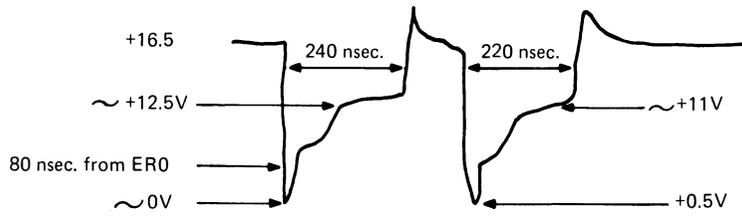
Figure 10. YRCS0 or XWCS0
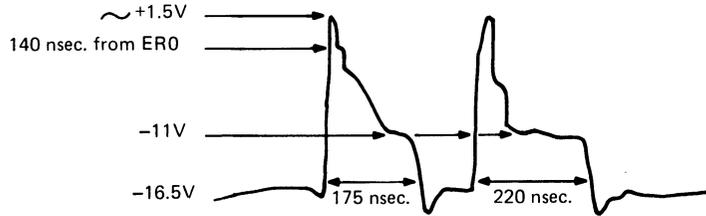
Figure 11. XRCS1 or YWCS1
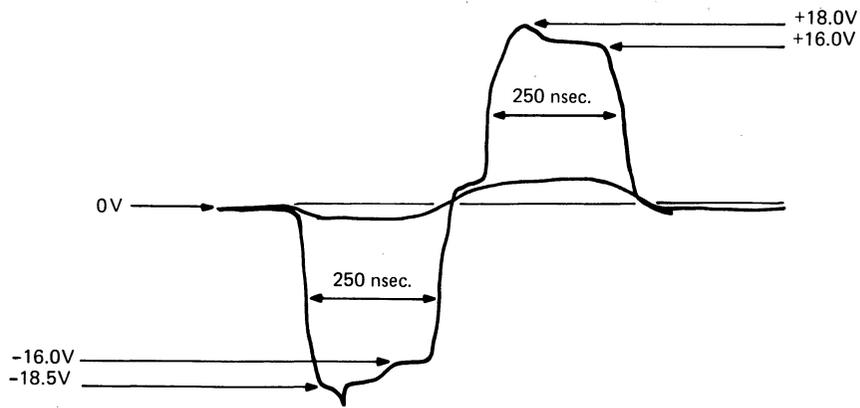
Figure 12. X Sink

Figure 13. Y Sink

15
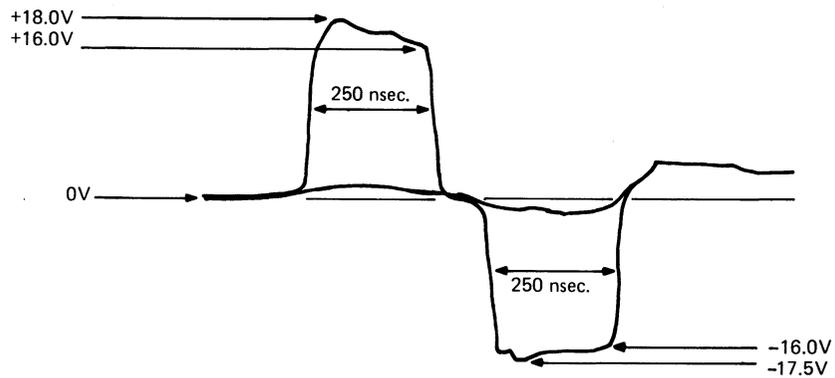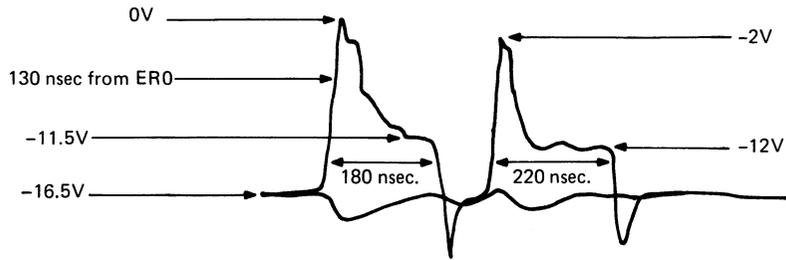
Figure 14. XRA0 + YWA0
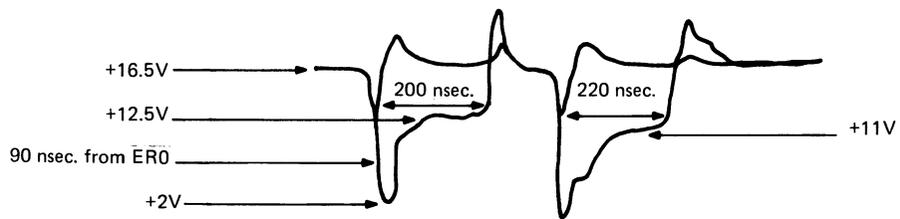
Figure 15. XWC0 + YRC0
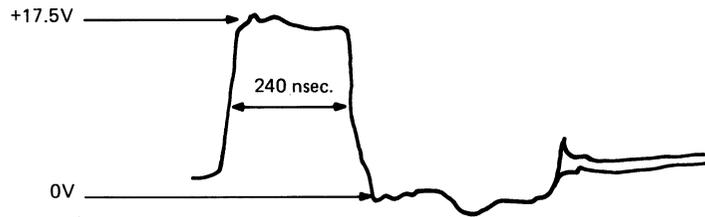
Figure 16. RYCHC
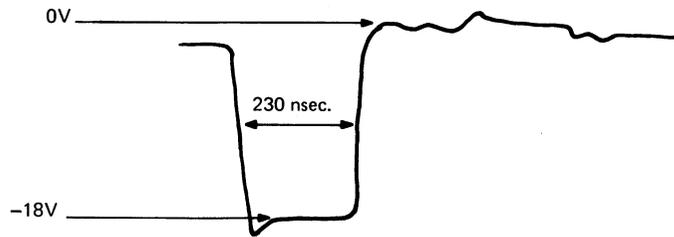
Figure 17. RXCHA
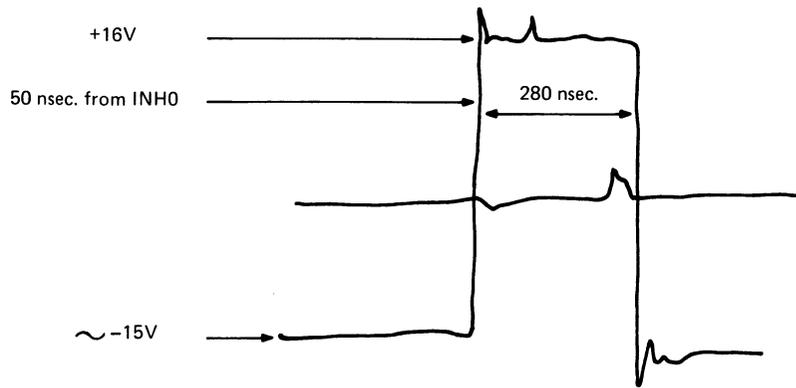
Figure 18. Q22 Emitter
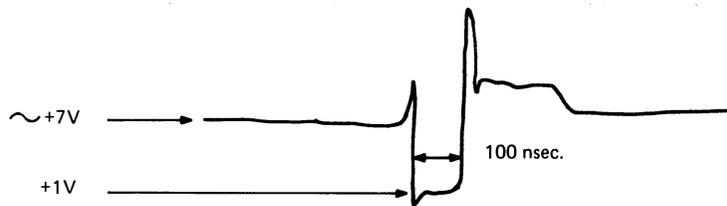
Figure 19. Q5 Collector
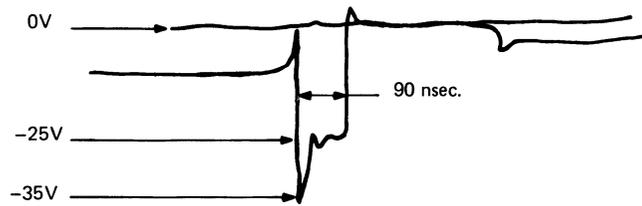
Figure 20. CR1 Anode
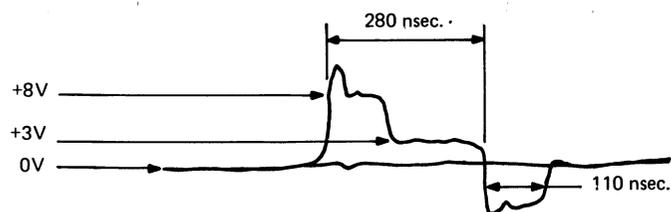
Figure 21. IB 16
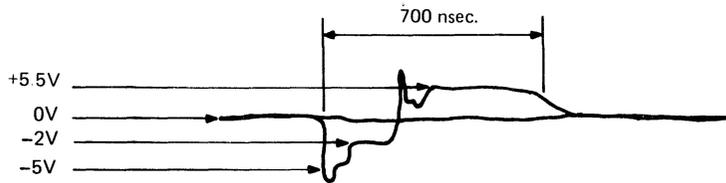
Figure 22. T15-3
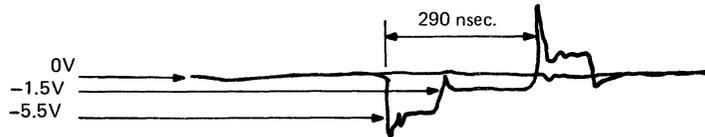
Figure 23. SB 16

Failing Address and Sink Switch Cross Reference

        (X=Don't Care)

X SINK

XS	0	Every Other Location from 1000 to 1FFE	(MA14=0)
XS	1	Every Other Location from 1000 to 1FFE	(MA14=1)
XS	2	Every Other Location from 3000 to 3FFE	(MA14=0)
XS	3	Every Other Location from 3000 to 3FFE	(MA14=1)
XS	4	Every Other Location from 0000 to 0FFE	(MA14=0)
XS	5	Every Other Location from 0000 to 0FFE	(MA14=1)
XS	6	Every Other Location from 2000 to 2FFE	(MA14=0)
XS	7	Every Other Location from 2000 to 2FFE	(MA14=1)

Y SINK

YS	0	256	Consecutive Loc. from X000 to X1FE
YS	1	256	Consecutive Loc. from X800 to X9FE
YS	2	256	Consecutive Loc. from X400 to X5FE
YS	3	256	Consecutive Loc. from XC00 to XDFE
YS	4	256	Consecutive Loc. from X200 to X3FE
YS	5	256	Consecutive Loc. from XA00 to XBFE
YS	6	256	Consecutive Loc. from X600 to X7FE
YS	7	256	Consecutive Loc. from XE00 to XFFE

Failing Address and X Drive Switch Cross Reference

XRA/XWC		(MA 4, 5, 6 can be a 0 or 1, but are shown as 0)
XRA/XWC	0	16 Consecutive Loc. from X000 to X01E
XRA/XWC	1	16 Consecutive Loc. from X100 to X11E
XRA/XWC	2	16 Consecutive Loc. from X080 to X09E
XRA/XWC	3	16 Consecutive Loc. from X180 to X19E
XRA/XWC	4	16 Consecutive Loc. from X040 to X05E
XRA/XWC	5	16 Consecutive Loc. from X140 to X15E
XRA/XWC	6	16 Consecutive Loc. from X0C0 to X0DE
XRA/XWC	7	16 Consecutive Loc. from X1C0 to X1DE
XRA/XWC	8	16 Consecutive Loc. from X020 to X03E
XRA/XWC	9	16 Consecutive Loc. from X120 to X13E
XRA/XWC	10	16 Consecutive Loc. from X0A0 to X0BE
XRA/XWC	11	16 Consecutive Loc. from X1A0 to X1BE
XRA/XWC	12	16 Consecutive Loc. from X060 to X07E
XRA/XWC	13	16 Consecutive Loc. from X160 to X17E
XRA/XWC	14	16 Consecutive Loc. from X0E0 to X0FE
XRA/XWC	15	16 Consecutive Loc. from X1E0 to X1FE

Failing Address and Y Drive Switch Cross Reference

YWA/YRC		(MA8, 9 can be a Ø or a 1, but are shown as Ø)
YWA/YRC	Ø	2 Consecutive Loc. from XX00 to XX02
YWA/YRC	1	2 Consecutive Loc. from XX10 to XX12
YWA/YRC	2	2 Consecutive Loc. from XX08 to XX0A
YWA/YRC	3	2 Consecutive Loc. from XX18 to XX1A
YWA/YRC	4	2 Consecutive Loc. from XX04 to XX06
YWA/YRC	5	2 Consecutive Loc. from XX14 to XX16
YWA/YRC	6	2 Consecutive Loc. from XX0C to XX0E
YWA/YRC	7	2 Consecutive Loc. from XX1C to XX1E
YWA/YRC	8	2 Consecutive Loc. from XX20 to XX22
YWA/YRC	9	2 Consecutive Loc. from XX30 to XX32
YWA/YRC	10	2 Consecutive Loc. from XX28 to XX2A
YWA/YRC	11	2 Consecutive Loc. from XX38 to XX3A
YWA/YRC	12	2 Consecutive Loc. from XX24 to XX26
YWA/YRC	13	2 Consecutive Loc. from XX34 to XX36
YWA/YRC	14	2 Consecutive Loc. from XX2C to XX2E
YWA/YRC	15	2 Consecutive Loc. from XX3C to XX3E

The following is a breakdown of groups of failing addresses and
which circuit to trouble-shoot. An X symbolizes either a 1 or a Ø.

Failing locations	Failing circuit
1. 0XX2, 0XX4, 0XX6, 0XX8	XS5 SH.14M4
2. XX0C to XX0E	YWA6 SH.15K6
XX4C to XX4E	YRC6 SH.15R6
XX8C to XX8E, etc.	
3. XX20 to XX22	YWA8 SH.16K2
XX60 to XX62	YRC8 SH.16R2
XXA0 to XXA2, etc.	
4. X0C0 to X0CE	
X2C0 to X2CE	XWC6 SH.15R6
X4C0 to X4CE	XRA6 SH.15K6
5. 0600 to 0800	
1600 to 1800	YS6 SH.13N6
2600 to 2800, etc.	

OPEN LINE OR BAD DIODE SYMPTOMS

EXAMPLES:

Failing Locations

1.	10C0	These bits decoded would point to XSØ and
	10C4	XRA/XWC 6, which points to X line 63.
	10C8	
	10CC	
	10D0	
	10D4	
	10D8	
	10DC	
2.	0C18	These bits decoded would indicate that YS3 and
	0C1A	YWA/YRC3, which points to Y line 15.
	0C58	
	0C5A	
	0C98	
	0C9A	
	0CD8	
	0CDA, etc.	

14. MNEMONICS LIST

The following list provides a brief description of each mnemonic found in the 32KB Memory. The source of each signal on Schematic Drawing 35-473D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLR0	Clear	12S3
DOG1	Data Out Gate	11D9
DUA0	Data Unavailable	12S3
ER0	Early Read (initiate read timing)	11A2
IA0:IA16	8K Inhibit A, Bits 0:16	2H5 and 9H5 2H9 and 9H9 10H5
IB0:IB16	8K Inhibit B, Bits 0:16	2H2 and 9H2 2H7 and 9H7 10H3
INH0	Inhibit (initiate write timing)	11A4
INHR1	Inhibit rise timing	11L4
INHT11	Inhibit flat top timing, circuit 1	11K6
INHT21	Inhibit flat top timing, circuit 2	11K6
IRTTA-IRTTE	Inhibit rise time transformer A-E	6C6 8C6 9C6
MA000	Memory Address Bus	11A6
MA010	Memory Address Bus	11A8
MA020	Memory Address Bus	14G
MA030	Memory Address Bus	12A6
MA040	Memory Address Bus	13G5
MA050	Memory Address Bus	13G5
MA060	Memory Address Bus	12A7
MA070:MA090	Memory Address Bus	15A3
MA100	Memory Address Bus	12B2
MA110:MA130	Memory Address Bus	15A4 15A5
MA140	Memory Address Bus	14G5
MAX060	Extended Memory Address Bus	11A7
MAX070	Extended Memory Address Bus	11A8

MNEMONIC	MEANING	SCHEMATIC LOCATION
MBSY1	Memory Busy Bus	11E6
MBZ0	Memory Busy Bus	11F8
MD000:MD160	Memory Data Bus	2C1 and 5C1 2C5 and 5C5 6A3 and 10A3 6A7 and 9A7
MS000:MS160	Memory Sense Bus	2R3 and 10R3 2R7 and 9H7
PAR0	Parity	11F7
RT0	Read Timing	11F5
RT1	Read Timing	11H2
RXCHA	Read X Sink Discharge	17G7
RXDTA0	Read X Drive Timing A	12F2
RXDTB0	Read X Drive Timing B	12F4
RYCHC	Read Y Sink Discharge Circuit	17G8
RYDTA0	Read Y Drive Timing A	12F4
RYDTB0	Read Y Drive Timing B	12F4
$\overline{SA0}:\overline{SA16}$	First side of 8K sense line A, Bits 0:16	2H4 and 9H4 2H9 and 9H9
SA0:SA16	The second side of 8K sense line A, Bits 0:16	10H5
SAS11	Sense Amplifier Strobe, Circuit 1	11K6
SAS21	Sense Amplifier Strobe, Circuit 2	11K7
SB0:SB16	First side of 8K sense line B, Bits 0:16	2H2 and 9H2 2H6 and 9H6
SB0:SB16	The second side of 8K sense line B, Bits 0:16	10H3
SCLR0A	System Clear	11A6
SKTA	Sink Timing A	11J4
+SKV	Positive Sink Voltage	17F1
-SKV	Negative Sink Voltage	17N1
V_T	Threshold Voltage	2H1
WT0	Write Timing	11E3
WT1	Write Timing	11H4
WXCHC	Write X Sink Discharge	17R7

MNEMONIC	MEANING	SCHEMATIC LOCATION
WXDTA0	Write X Drive Timing A	12G3
WXDTB0	Write X Drive Timing B	12G3
WYCHA	Write Y Sink Discharge Circuit	17R8
WYDTA0	Write Y Drive Timing A	12G5
WYDTB0	Write Y Drive Timing B	12G5
XRA0-YWA0 through XRA15-YWA15	X Read Anode 0 or Y Write Anode 0 through X Read Anode 15 or Y Write Anode 15	Sheets 15 and 16
XRCT1	X Read Current Timing	12F9
XRCS1 or YWCS1	X Read Current or Y Write Current	17L1
XS0:XS7	X Sink 0:7	Sheet 14 Sheet 15
XSTA0	X Sink Timing A	12F6
XSTB0	X Sink Timing B	12F6
XWC0 + YRC0 through XWC15 + YRC15	X Write Cathode 0 or Y Read Cathode 0 through X Write Cathode 15 or Y Read Cathode 15	Sheet 15 Sheet 16
YRCS0 or XWCS0	Y Read Current or X Write Current	17E1
YS0:YS7	Y Sink 0:7	Sheet 12 Sheet 12
YSTA0	Y Sink Timing A	12F7
YSTB0	Y Sink Timing B	12F7