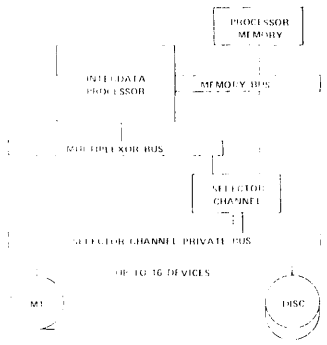
INTERDATA®

Product Bulletin

Selector Channel



- **2,000,000 Data Transfer Rate**
- **Byte and Halfword Data Transfer Modes**
- **Simultaneous Data Processing**
- **True Cycle Stealing Direct Memory Access**

GENERAL DESCRIPTION

The SELECTOR CHANNEL provides a completely independent high-speed direct memory data transfer interface between INTERDATA processor memory and selected device controllers. Up to 16 device controllers may be connected to the Selector Channel.

Data transfer rates of up to 2,000,000 bytes per second are possible with the Selector Channel. The chief advantage of a Selector Channel is the capability to transfer data simultaneously with data transfer over the multiplexor bus and other processing functions.

The Selector Channel is capable of operating in a block transfer mode or a transparent mode and allows device data transfer in a byte or halfword data format.

OPERATIONAL CHARACTERISTICS

The Selector Channel transfers data by employing a true cycle-stealing operation directly to processor memory. Once initiated, the Selector Channel functions in a completely autonomous fashion. One device may be active at any one time.

Data transfer is initiated by loading a starting address and an ending address which specify the memory start and end addresses for the specific data to be transferred. After address loading, the processor issues a GO command to the Selector Channel and the data transfer proceeds without further direction from, or interaction with the processor. The GO command also inhibits activity between the processor and any other device on the Selector Channel private bus. All Selector Channel set-up commands are transferred over the processor multiplexor bus.

The Selector Channel responds to three commands: READ, GO and STOP.

The READ command causes the Selector Channel to set the particular device controller in a read mode and the internal memory interface logic to a memory write mode. This allows data transfer from the Selector Channel connected device to memory. In the absence of a READ command the Selector Channel automatically assumes a WRITE mode which sets the memory interface logic to transfer data from memory to a Selector Channel connected device.

The GO command releases the internal Selector Channel circuitry which allows the direct memory access operations to take place and the autonomous transfer of data to proceed until the block specified by the start and end addresses has been completed.

Upon receipt of a STOP command the Selector Channel completes the current access cycle (if in progress), clears the busy signal which will allow the processor access and terminates direct memory access operations.

Upon termination of a data transfer block, the Selector may interrupt the processor to signal activity completion or change the status to return the Selector Channel to idle mode without processor interrupt.

When not activated, the Selector Channel private bus is connected directly to the multiplexor bus and acts as a bus buffer. Communication between the multiplexor and private bus devices takes place in the normal I/O bus manner using standard I/O programming conventions.

SPECIFICATIONS

Maximum I/O Data Rate:	2,000,000 bytes per second
Maximum Number of Devices:	16
Data Transfer Format:	Byte (8bit) or Halfword (16bit)
Direct Memory Access Method:	Cycle Steal
Dimensions:	15" x 15"
Weight:	2.5 pounds
Power Requirement:	+ 5.0 VDC ± 5%, 2.5 Amperes

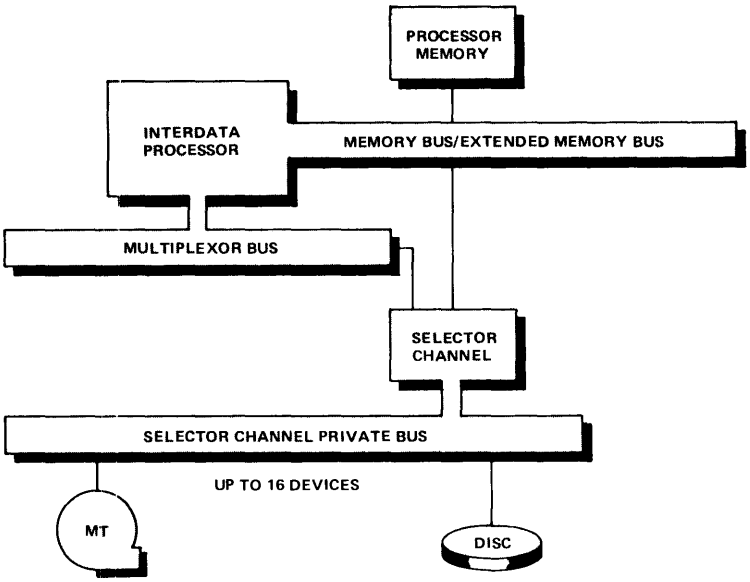
INTERDATA PRODUCT NUMBER

M70-103 Selector Channel, provides true cycle-stealing to memory for 8 or 16-bit transfers at rates up to 2MB/sec. Includes hardware byte assembly and automatic control of variable length records.

INTERDATA® 2 Crescent Place, Oceanport, New Jersey 07757 (201) 229-4040 Printed in U.S.A. 55473

INTERDATA®

SYSTEM MODULES



Selector Channel

PRODUCT DESCRIPTION

The Selector Channel provides a completely independent high-speed direct memory data transfer interface between Interdata processor memory and selected device controllers. Up to 16 device controllers can be connected to the Selector Channel.

Data transfer rates of up to 2,000,000 bytes per second are possible. The Selector Channel provides the capability to transfer data simultaneously with data transfer over the multiplexor bus and other processing functions.

The Selector Channel can operate in a block-transfer mode or a transparent mode and allows device data transfer in a byte or halfword data format.

FEATURES

- 2,000,000 Bytes Per Second Transfer Rate
- Simultaneous Data Processing
- Byte and Halfword Data Transfer Modes
- True Cycle Stealing Direct Memory Access

OPERATIONAL CHARACTERISTICS

The Selector Channel transfers data by employing a true cycle-stealing operation directly to processor memory. Once initiated, the Selector Channel functions in a completely autonomous fashion. One device can be active at any one time.

Data transfer is initiated by loading a starting address and an ending address which specify the memory start and end addresses for the specific data to be transferred. After address loading, the processor issues a GO command to the Selector Channel and the data transfer proceeds without further direction from, or interaction with the processor. The GO command also inhibits activity between the processor and any other device on the Selector Channel private bus. All Selector Channel set-up commands are transferred over the processor multiplexor bus.

The M70-103 Selector Channel is designed to function with Interdata 16-bit processors with a memory address range of 64 K bytes. The M73-105 Extended Selector Channel is used with the 7/32 series processors and is capable of addressing 1 million bytes of memory.

COMMANDS

The Selector Channel responds to three commands: READ, GO and STOP.

The READ command causes the Selector Channel to set the particular device controller in a read mode and the internal memory interface logic to a memory write mode. This allows data to transfer from the Selector Channel connected device to memory. In the absence of a READ command, the Selector Channel automatically assumes a WRITE mode which sets the memory interface logic to transfer data from memory to a Selector Channel connected device.

The GO command releases the internal Selector Channel circuitry which allows the direct memory access operations to take place and the autonomous transfer of data to proceed until the block specified by the start and end addresses has been completed.

On receipt of a STOP command, the Selector Channel completes the current access cycle, clears the busy signal which will allow the processor access, and terminates direct memory access operations.

On termination of a data transfer block, the Selector Channel may interrupt the processor to signal activity completion or change the status to return the Selector Channel to idle mode without processor interrupt.

When not activated, the Selector Channel private bus is connected directly to the multiplexor bus and acts as a bus buffer. Communication between the multiplexor and private bus devices takes place in the normal I/O bus manner using standard I/O programming conventions.

SPECIFICATIONS

Maximum I/O Data Rate:
2,000,000 bytes per second

Maximum Number of Devices:
16

Data Transfer Format:
Byte (8 bit) or Halfword (16 bit)

Direct Memory Access Method:
Cycle Steal

Address Range:

Selector Channel	64 K Bytes
Extended Selector Channel	1 M Bytes

Dimensions:
15" x 15"

Weight:
2.5 pounds

Power Requirement:
+ 5.0 VDC ± 5%, 2.5 Amperes

Interdata Product Number

M70-103 – Selector Channel. Provides true cycle-stealing to memory for 8 or 16-bit transfers at rates up to 2MB/sec. Includes hardware byte/halfword assembly and automatic control of variable length records.

M73-105 – Extended Memory Selector Channel. Provides a true cycle stealing access to up to 1,000,000 bytes of main memory for 8 or 16 bit transfers at rates up to 2 MB/sec.

INTERDATA®
Subsidiary of PERKIN ELMER • Oceanport New Jersey 07757
Printed in U.S.A.
8761021