VME-68K10

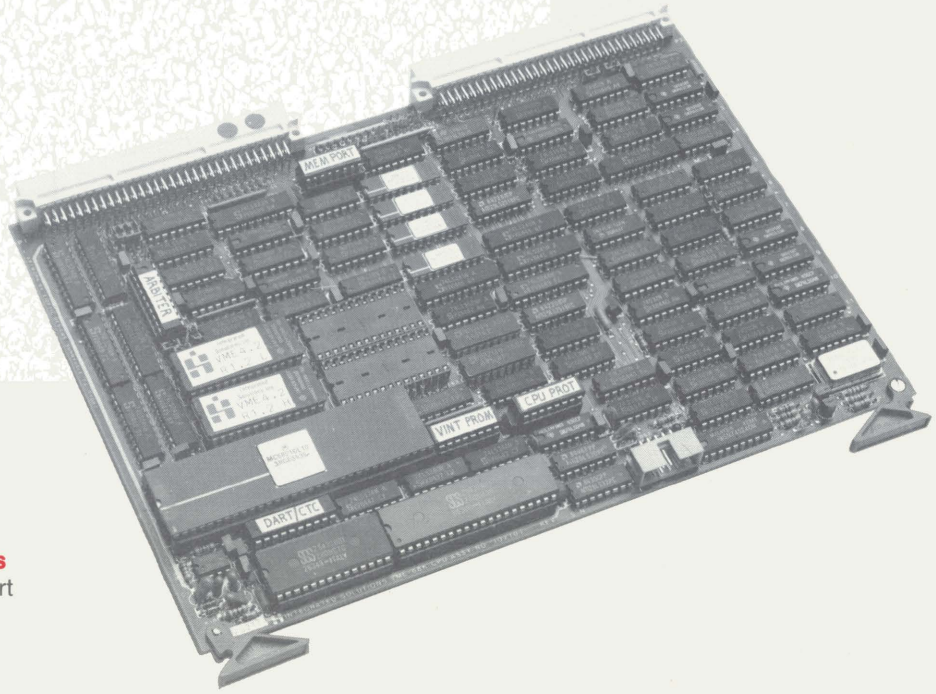
Product Specifications

Features

- 10 MHz 68010 CPU or 11.2 MHz 68010 CPU
- Dual 32-bit buses (VME bus and HSMEM bus)
- High speed memory management unit (MMU)
- Programmable interrupt timer
- Two serial ports
- Four on-board sockets for up to 128 Kb of EPROM or ROM; or up to 64 Kb of EPROM or ROM and 16 Kb of static RAM

The *VME-68K10* is a high-performance systems-oriented CPU on a standard double-size VME card. It is designed to combine the processing speed, large instruction space and powerful instruction set of the MC68010 processor with the well-defined and well-documented second generation VME bus.

The *VME-68K10* maximizes the performance available from the MC68010 processor. With the addition of one or more *VME-HSMEM (MEG/2MEG)*, dual-ported memory cards, the processor can have no wait state access to up to the full 16 Mb of physical memory present on the VME bus.



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Processor

The *VME-68K10* is available with either a 10 MHz 68010 processor or a 11.2 MHz 68010 processor.

Buses

The *VME-68K10* supports two buses, the VME bus and the HSMEM bus, that function together to allow the 68010 to run at maximum speed.

HSMEM Bus

The HSMEM bus is a 32-bit semisynchronous memory bus implemented on the user-defined pins (outside two rows) of the P2 connector. It provides access to up to 16 Mb of physical memory with no wait states even with a 11.2 MHz 68010 processor.

23 Address Lines:
HSADD23—HSADD1

32 Data Lines:
HSDAT31—HSDAT0

9 Control Lines:

HSCYC*	Used to start a HSMEM cycle
HSUDS*	Used as upper and lower data
HSLDS*	Strobes on the HSMEM bus
HSRW*	Read/write control line
HSLW*	Used to signal 32 bit transfers
HSREF*	Used to signal the start of a refresh cycle
HSVMEK*	Used to signal the start of a VME access cycle
HSPARERR*	Parity error signal returned by the memory board to the CPU if parity error occurs
HSDTACK*	Used as the handshake to allow the completion of high-speed memory cycles

VME Bus

The VME bus is a complete implementation that supports 24-bit addresses and 16-bit data transfers. It includes an interrupt handler for all seven interrupt levels and a four-level prioritized bus arbiter.

The board is configurable to run with all dual-ported HSMEM memory, all standard VME memory or a combination of the two. All I/O devices other than the on-board serial ports and countertime channels are normally accessed over the VME bus. For those users who want to design high-speed I/O interfaces to the HSMEM bus, full specifications are provided with the *VME-68K10.*

Prioritized Arbiter

The *VME-68K10* supports a full four-level prioritized arbiter as defined in the VME specification. The CPU itself can be placed at any of the four levels and the arbiter can be disabled allowing the CPU to function with the arbiter on some other card. A jumper allows the CPU itself to function as either a *RELEASE ON REQUEST* or a *RELEASE WHEN DONE* master. The arbiter is very fast, arbitrating requests in 120ns average with the 11.2 MHz board or 150ns average with the 10 MHz board.

Memory Management Unit (MMU)

The *VME-68K10* memory management unit (MMU) is based on a two-level translation system that consists of a segmentation front end followed by a paged back end. The segmentation unit takes bits 22-17 of the 68010 logical address and uses these bits as an index into the segment register bank along with four bits of the context register. The segment register array consists of 1024 registers, each 8 bits wide. The combination of 6 logical address bits and 4 context register bits selects one unique segment register on each memory access. Out of the segment register bank come 8 bits: the upper two bits are used for protection and the bottom six bits are used as an index into the page table. The two protection bits are encoded as follows:

00—no access
01—read and execute access only
10—read/write access
11—system mode-read/write access user mode-execute access only

Page Map

The six segment number bits coming out of the segment register are concatenated with bits 16-12 of the logical address to form an eleven bit entry into the page table. The page table is 2 Kb x 16 bits. Out of the page table comes a 12-bit physical page number that is concatenated with the 12 low-order address bits (actually address bits 11-1 plus UDS* and LDS*) to form a 24-bit physical address. In addition, the output of the page register bank has three additional bits: a non-existent page bit that is set by the software to mark the page as non-resident in physical memory, a page accessed bit that is automatically updated by the hardware on any access to that page, and a page written bit that is automatically updated by the hardware on any write access to that page. In addition, there is a spare bit that can be read and written by the software for house-keeping purposes if necessary.

Programmer's View of Memory Management Structure

From the programmer's point of view, each process consists of up to 64 segments, each segment containing up to 32 four Kb pages.

Context Register

To minimize context switching overhead, there are actually 16 sets of 64 segments present in the segment map. A 4-bit context register, settable only by the system, selects which user context is employed when a user program is running. Whenever the 68010 is in supervisor mode, the system context (context 0) is used automatically. The user context, however, is preserved when a switch is made from user mode to system mode and back to user mode such as when servicing interrupts. Thus, when 15 or fewer processes are simultaneously memory resident, context switching only requires modifying the context register while in supervisor mode.

Software

The *VME-68K10* is available with UNIX 4.2 BSD (Berkeley Software Distribution). UNIX 4.2 BSD is the operating system of choice for those users who want a full virtual implementation plus a high level of performance in the file system. UNIX 4.2 BSD runs on most Digital Equipment Corporation VAX systems that run UNIX. The Integrated Solutions 4.2 BSD implementation is complete and provides the same operating environment as on a VAX.

EPROM Options

Two EPROM options are available with the VME-68K10:

MACS The MACS set of two 2732 EPROMs contains self-test diagnostics, MMU initialization logic, and the Motorola Macsbug debugger/monitor. As a debugger, Macsbug supports low-level software debugging, including the ability to set breakpoints and to trace instruction execution. As a monitor, Macsbug has a rich command set for examining and modifying registers and memory locations.

UNIPS The UNIPS set of two 27128 EPROMs contains self-test diagnostics, MMU initialization logic, and UNIX bootstrap loaders. This set is required for running UNIX 4.2 BSD.

Specifications

Processor

Motorola 68010.

Versions

VME-68K10-10:
10 MHz 68010.
VME-68K10-11:
11.2 MHz 68010.

Form Factor

Standard double-size VME board, 160mm by 233.33mm.

I/O Connections

Two Serial ports:
One with full modem control-10 pin ribbon cable connector.

Buses

VME bus:
P1 connector. Full support for the VME bus including all seven interrupt levels and full four level bus arbitration logic.

HSMEM bus:
P2 connector (user defined I/O pins). Full 32-bit semi-synchronous bus allows 68010 to run with no wait states.

PROM Sockets

Four on-board PROM sockets for up to 128 Kb of EPROM or ROM; or two sockets for 64 Kb of EPROM or ROM and two sockets for up to 16 Kb of static RAM.

Programmable Interrupt Timer

This timer can be set to interrupt at either a 60Hz or 50Hz rate as required for UNIX operation or can be used as a programmable timer for real-time applications.

Power Requirements

+5 volts, 4.5 amps.
+12 volts, .05 amps.

Environmental Requirements

Temperature:
0 to 50 degrees centigrade (operating)
−40 to 65 degrees centigrade (non-operating)
Humidity:
10 to 95 percent (non-condensing)

1. UNIX is a trademark of Bell Laboratories.
2. VAX is a trademark of Digital Equipment Corporation.
3. Macsbug is a trademark of Motorola.
4. 4.2 BSD is a trademark of the Board of Regents, University of California, Berkeley.

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