VME-TC50

Tape Controller

Hardware Reference Manual

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PREFACE

This manual describes the Integrated Solutions (IS) VME-TC50 Tape Controller Board. The text provided in this manual includes a product overview, specifications, configuration information, and software interface information. The manual is divided into five sections which include the following:

Section 1 describes the general features and architecture of the VME-TC50.

Section 2 lists the board specifications.

Section 3 provides information regarding VME-TC50 configuration.

Section 4 describes the VME-TC50 tape controller software interface.

Section 5 describes the VME-TC50 Real Time Clock software interface.

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SECTION 1: INTRODUCTION

1.1 Features

Integrated Solutions' VME-TC50 is a half-inch nine-track tape controller with an industry standard (Pertec) interface. The VME-TC50 is implemented on a single double-wide VME-compatible printed circuit board and offers the following features:

- Forty-eight Kbytes of on-board data buffer for sustained high data transfer rates
- Full 24-bit memory addressing (16 Mbytes)
- Supports both streaming and start/stop nine-track tape drives
- Handles tape drives that support 800, 1600, 3200, and 6250 BPI
- Supports dual speed and/or dual density tape drives
- Supports NRZI, PE, and/or GCR tape drives
- Burst transfer rate up to 500 Kbytes per second
- On-board diagnostics with LED indicator
- Real Time Calendar/Clock (RTC)
- Programming interface that employs packet processing

1.2 Architecture

As shown in Figure 1-1, the major functional elements of the VME-TC50 board are

- Control microprocessor (Z8002)
- Forty-eight Kbyte RAM buffer
- EPROM-resident firmware and diagnostics
- VME interface logic (Bus Request/Grant, Address Decode, Interrupt Request)
- CMOS Real Time Calendar/Clock with battery backup

1.2.1 Control Microprocessor

The high-speed 16-bit microprocessor controls all communications across the VME bus and all operations of the tape unit. Use of a 16-bit microprocessor gives the VME-TC50 a high level of functionality.

1.2.2 Data Buffer

The VME-TC50 Tape Controller features a RAM buffer that maximizes the throughput of the tape unit by minimizing data read overruns and data write underruns. Overruns and underruns occur due to the mismatch between the data transfer rates of the tape unit (high) and the operating system (much lower).

All information is transferred between the peripheral devices and the VME bus memory through the on-board 48 Kbyte buffer which is implemented in 8K x 8 static RAMs.

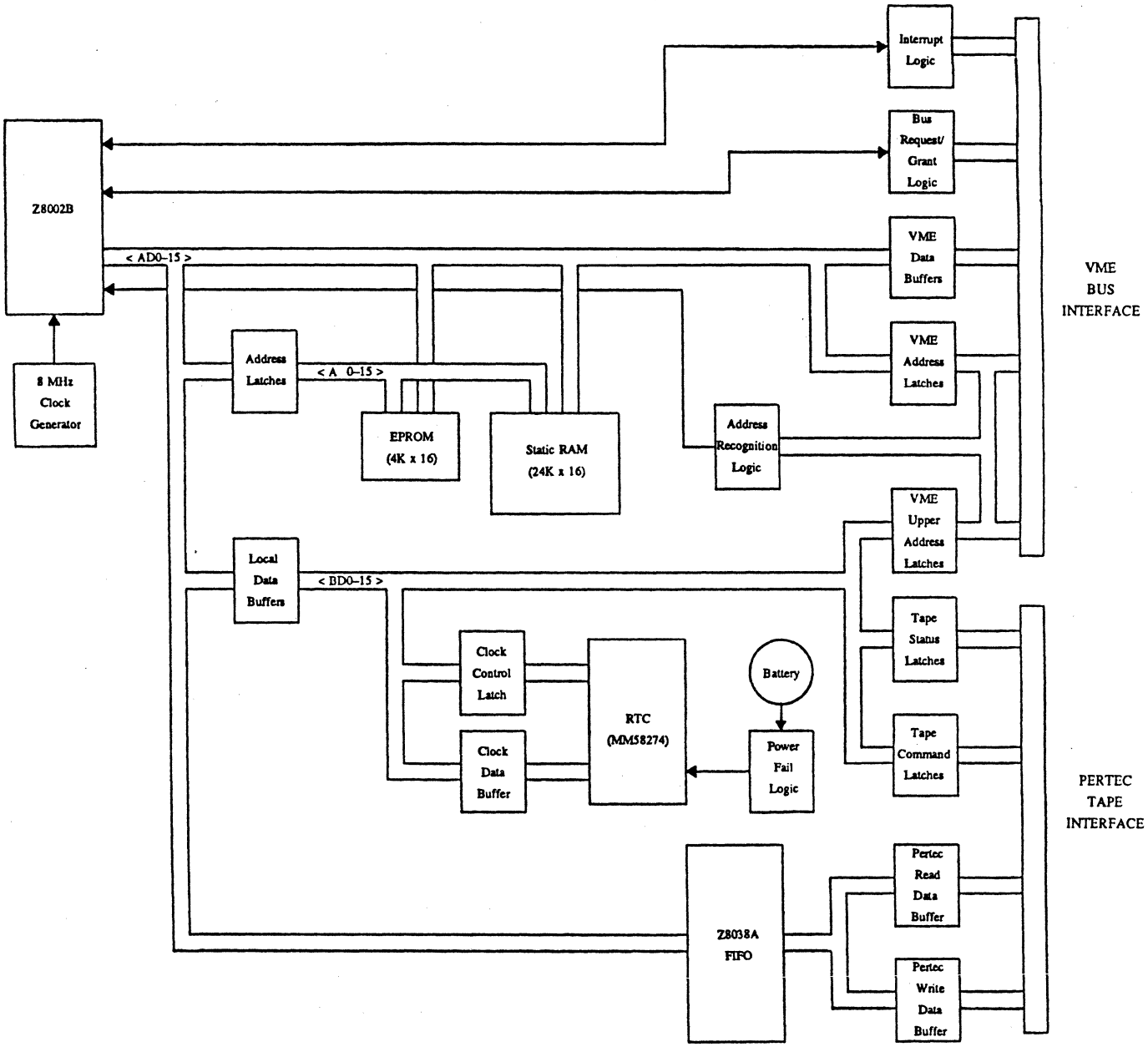


Figure 1-1. VME-TC50 Block Diagram

1.2.3 EPROMs

All VME-TC50 operations are controlled and monitored by the firmware which resides in two 2732A EPROMs. These EPROMs can easily be changed in the field if firmware upgrades are necessary.

1.2.4 VME Interface Logic

The VME-TC50 interfaces with the VME bus as a 24 address bit, 16 data bit master; and a 24 address bit, 16 data bit slave (as defined in the *VMEbus Specification Manual*, Motorola part number MVMEBS/D1). The VME interface logic on the VME-TC50 board provides interfacing capability consistent with the VME specification for the following VME-defined functional modules:

- Data Transfer Bus Requester—This is the bus acquisition interface based on a Bus Request/Bus Grant protocol. There are actually four separate sets (0-3) of these lines defined by VME. Each set supports a *daisy chain propagation* priority scheme among multiple requesters within the set. Prioritization also exists between sets, with highest priority going to Request 3. Any one of these can be selected on the VME-TC50.
- Data Transfer Bus Master—This is the ability to initiate data transfer cycles across the data transfer bus. Once acquisition of the bus has been granted, the VME-TC50 may directly access the host memory independent of the host CPU.
- Interrupter—The interrupter performs three tasks. It asserts the interrupt request line, supplies a status/ID (vector) byte to the data bus when its request has been acknowledged, and propagates the interrupt acknowledge daisy chain signal if it is not requesting that level of interrupt. There are seven levels (1-7) of interrupt request priority supported by VME, with Level 7 being the highest. The VME-TC50 can select one level from Levels 4 through 7; Levels 1 through 3 are not selectable.
- Slave—This is the ability to respond to an access attempt by a master. Determination of an attempt to access is based on recognition of a certain address within a particular address range. The VME-TC50 can exist on any eight-word boundary within the address range of FFF000 to FFFFF0 (hex).

1.2.5 Real Time Calendar/Clock

The Real Time Calendar/Clock (RTC) consists of a CMOS real time clock/calendar chip, lithium battery, micropower crystal oscillator, and power failure detection and cutover circuits. The battery should power the RTC for approximately five years.

1.3 Programming Interface

The VME-TC50 tape controller software interface corresponds very closely to the DEC TS11 interface (a DEC half-inch start/stop tape interface). Consequently, UNIX or other operating system TS11 drivers can be easily used with the VME-TC50.

The VME-TC50 communicates with the host CPU via three VME bus word locations that function as device registers. These device registers are the first three words on an eight-word boundary. The first two word locations function as device registers for the tape control function, while the third word supports the RTC (Sections 4 and 5 of this manual provide more detailed software interface information regarding the tape control function and RTC function respectively).

The VME-TC50 Tape Controller uses a mechanism called *packet processing* in order to receive commands from the host CPU as well as to provide tape transport status to the host CPU. With packet processing, the host CPU creates command packets in system memory that supply the VME-TC50 with commands and their associated parameters. The CPU then writes the 24-bit address of a particular command packet into the VME-TC50 tape controller device registers. When the VME-TC50 receives a command packet address, it retrieves the command packet from system memory via DMA transfer and executes the command. Upon completion of the command, tape transport status is written to the Status

Register which can be read by the host CPU. Additional status information in the form of a message packet is also provided via DMA transfer from the VME-TC50 to a predefined system memory location called the message buffer.

The commands and subcommands directly supported by the VME-TC50 Tape Controller include the following:

- Write Characteristics
- Read
  - Read Next (Forward)
  - Reread Previous (Space Reverse, Read Forward)
- Write
  - Write Data
  - Write Data Retry (Space Reverse, Erase, Write Data)
- Position
  - Space Records Forward
  - Space Records Reverse
  - Skip Tape Marks Forward
  - Skip Tape Marks Reverse
  - Rewind
- Format
  - Write Tape Mark
  - Erase
  - Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)
- Control
  - Message Buffer Release
  - Rewind and Unload
  - Clean Tape (handled as NO-OP)
- Get Status
- Subsystem Initialize

SECTION 2: SPECIFICATIONS

This section provides performance specifications and operating requirements for the VME-TC50.

2.1 Form Factor

The VME-TC50 form factor is standard double-sized VME - 160mm x 233.33mm.

2.2 Compatibility

The VME-TC50 plugs into a VME bus-based system and supports half-inch nine-track tape drives and contains a Real Time Calendar/Clock (RTC). The VME-TC50 interfaces with the VME bus as a 24 address bit, 16 data bit master; and a 24 address bit, 16 data bit slave (as defined in the *VMEbus Specification Manual*, Motorola part number MVMEBS/D1). Table 2-1 provides the pin assignments and signal mnemonics for the VME-TC50 VME bus connector, P1.

The VME-TC50 supports numerous tape drives that conform to the Pertec interface standard including the Cipher Microstreamer and the CDC Keystone. The tape controller input/output is implemented on two 50-pin flat ribbon cable connectors (J1 and J2) that conform to the Pertec interface standard. The I/O signal mnemonics and pin assignments are provided in Table 2-2.

2.3 Addressing

The VME-TC50 board uses three one-word VME bus address locations to support tape units and the RTC. The addressing may be set on any eight-word boundary within the address range of FFF000 to FFFFF0 (hex). Since the VME-TC50 actually responds to eight one-word VME bus addresses, the five remaining words within the eight word boundary may not be assigned to other functions.

2.4 Address Modifiers

The VME-TC50 responds to all standard (non-sequential) supervisory and non-privileged accesses. It does not respond to short I/O or extended (32-bit address) accesses.

2.5 Interrupt Vector

The VME-TC50 interrupt vector is switch-selectable from 94 or 98 (hex). By changing one of the on-board EPROMs, other vectors can be selected.

2.6 Electrical Requirements

The VME-TC50 power requirements are +5 volts at 2.0 amps typical (3.6 amps maximum).

2.7 Environmental Requirements

The VME-TC50 environmental requirements are as follows:

Temperature:

0 to 50 degrees centigrade (operating)
-40 to 65 degrees centigrade (non-operating)

Humidity:

10 to 95 percent (non-condensing)

Table 2-1. VME Bus Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	VMED0	BBUSY*	VMED8
2	VMED1	BCLR*	VMED9
3	VMED2	ACFAIL*	VMED10
4	VMED3	BG0IN*	VMED11
5	VMED4	BG0OUT*	VMED12
6	VMED5	BG1IN*	VMED13
7	VMED6	BG1OUT*	VMED14
8	VMED7	BG2IN*	VMED15
9	GND	BG2OUT*	GND
10	SYSCLK†	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	VMEBERR*
12	VMEDS1*	BR0*	SYSRESET*
13	VMEDS0*	BR1*	LWRD*
14	VMEWR*	BR2*	VMEAM5
15	GND	BR3*	VADD23
16	VMEDTACK*	VMEAM0	VADD22
17	GND	VMEAM1	VADD21
18	VMEAS*	VMEAM2	VADD20
19	GND	VMEAM3	VADD19
20	VMEIACK*	GND	VADD18
21	IACKIN*	SERCLK†	VADD17
22	IACKOUT*	SERDAT†	VADD16
23	VMEAM4	GND	VADD15
24	VADD7	IRQ7*	VADD14
25	VADD6	IRQ6*	VADD13
26	VADD5	IRQ5*	VADD12
27	VADD4	IRQ4*	VADD11
28	VADD3	IRQ3*†	VADD10
29	VADD2	IRQ2*†	VADD9
30	VADD1	IRQ1*†	VADD8
31	-12V†	+5V STDBY†	+12V†
32	+5V	+5V	+5V

† *VME bus signals, but no connection on VME-TC50 board.*

Table 2-2. I/O Connector Pin Assignments

Connector	Signal Pin Number	Return Pin Number	Signal Mnemonic	Signal Name
J1	2	1	IFBY	Formatter Busy
	4	3	ILWD	Last Word
	10,12,30,26	9,11,29,25	IW0-7	Write Data 0-7
	6,32,28,24	5,31,27,23		
	8	7	IGO	Initiate Command
	14	-	-	Spare
	16	15	ILOL	Load/On Line
	18	17	IREV	Reverse
	20	19	IREW	Rewind
	22	21	IWP	Write Data Parity
	34	33	IWRT	Write
	36	35	ILGAP	Long Gap
	38	37	IEDIT	Edit
	40	39	IERASE	Erase
	42	41	IWFM	Write File Mark
	44	43	IRTH1	Read Threshold 1
	46	45	ITAD0	Transport Address 0
	48,50	47,49	IR2-3	Read Data 2-3
J2	1	-	IRP	Read Data Parity
	2,3	-	IR0-1	Read Data 0-1
	4	-	ILDP	Load Point
	6,20,10,8	5,19,9,7	IR4-7	Read Data 4-7
	12	11	IHER	Hard Error
	14	13	IFMK	File Mark
	16	15	IDENT	PE Identification Burst
	18	17	IFEN	Formatter Enable
	22	21	IEOT	End of Tape
	24	23	IRWU	Rewind/Unload
	26	25	INRZ	NRZI Mode
	28	27	IRDY	Ready
	30	29	IRWD	Rewinding
	32	31	IFPT	File Protect
	34	33	IRSTR	Read Strobe
	36	35	IWSTR	Write Strobe
	38	37	IDBSY	Data Busy
	40	39	ISPEED	High-Speed Status
	42	41	ICER	Corrected Error
	44	43	IONL	On Line
	46	45	ITAD1	Transport Address 1
	48	47	IFAD	Formatter Address
	50	49	IHISP	High-Speed Select

2.8 Diagnostics

The VME-TC50 has an automatic self test at power-on or system reset. Normally, at power-on or reset the diagnostic LED on the VME-TC50 board lights, indicating that the self diagnostic is executing. After approximately two seconds the LED goes off and remains off, signifying successful completion of the test. The only time the LED again lights is if a fatal error is detected. In such cases, a four-bit error code is continuously blinked on the LED (most significant bit first) with a two to three second pause between each code signal.

With a long blink representing a 1 and short blink representing 0, the VME-TC50 fatal error codes are given in Table 2-3.

Table 2-3. VME-TC50 Fatal Error Codes

Code	Description
0000	Error in RAM Bank 0
0001	Error in RAM Bank 1
0010	Error in RAM Bank 2
0011	No RAM in Bank 0
0100	NMI error (hardware or firmware related problem)
0101	Write command stop error indicating a Write command stopped with data still in the FIFO
0110	Read command stop error indicating a Read command stopped with data still in the FIFO
0111	Not used
1000	Interrupt error indicating an invalid interrupt vector on vectored interrupt from the FIFO

SECTION 3: CONFIGURATION

The VME-TC50 board has jumpers and switches which provide considerable configuration flexibility. This section describes how to configure the VME-TC50 board. Figure 3-1 is a layout of the VME-TC50 board that shows the jumper and switch locations. The functions and configuration of these jumpers and switches are discussed in the paragraphs that follow.

3.1 Jumper Configurations

There are 62 jumpers on the VME-TC50. Their functions and setting are discussed in the following paragraphs.

3.1.1 VME Bus Requestor Jumper Settings (E1–E24)

Jumpers E1–E24 control the VME bus request/grant level of the VME-TC50 requester. There are four levels of bus request/grant, Levels 0 through 3. The jumper configurations for each request/grant level are shown in Table 3-1. The ISI factory default setting is for Level 2.

Table 3-1. Bus Request/Grant Level Jumper Settings

Level 0	Level 1	Level 2	Level 3
E7 to E8	E5 to E6	E3 to E4	E1 to E2
E11 to E12	E11 to E12	E11 to E12	E9 to E11
E15 to E16	E15 to E16	E13 to E15	E10 to E12
E19 to E20	E17 to E19	E14 to E16	E15 to E16
E21 to E23	E18 to E20	E19 to E20	E19 to E20
E22 to E24	E23 to E24	E23 to E24	E23 to E24

3.1.2 RAM Socket Configuration (E41–E43 and E47–E49)

Jumpers E41–E43 and E47–E49 configure the static RAM sockets to accommodate either 2K x 8 or 8K x 8 static RAMs (see Table 3-2). When using 2K x 8 RAMs, the RAM chips must be positioned in the sockets so that Pin 1 of the chip resides in Pin 3 of the socket.

At system power on, the on-board firmware automatically determines which size RAMs are present and adjusts itself accordingly. The VME-TC50 default setting is for 8K x 8 RAMs.

Table 3-2. Static RAM Jumper Settings

RAM	Jumper Setting
2K x 8	E41 to E42 E47 to E48
8K x 8	E42 to E43 E48 to E49

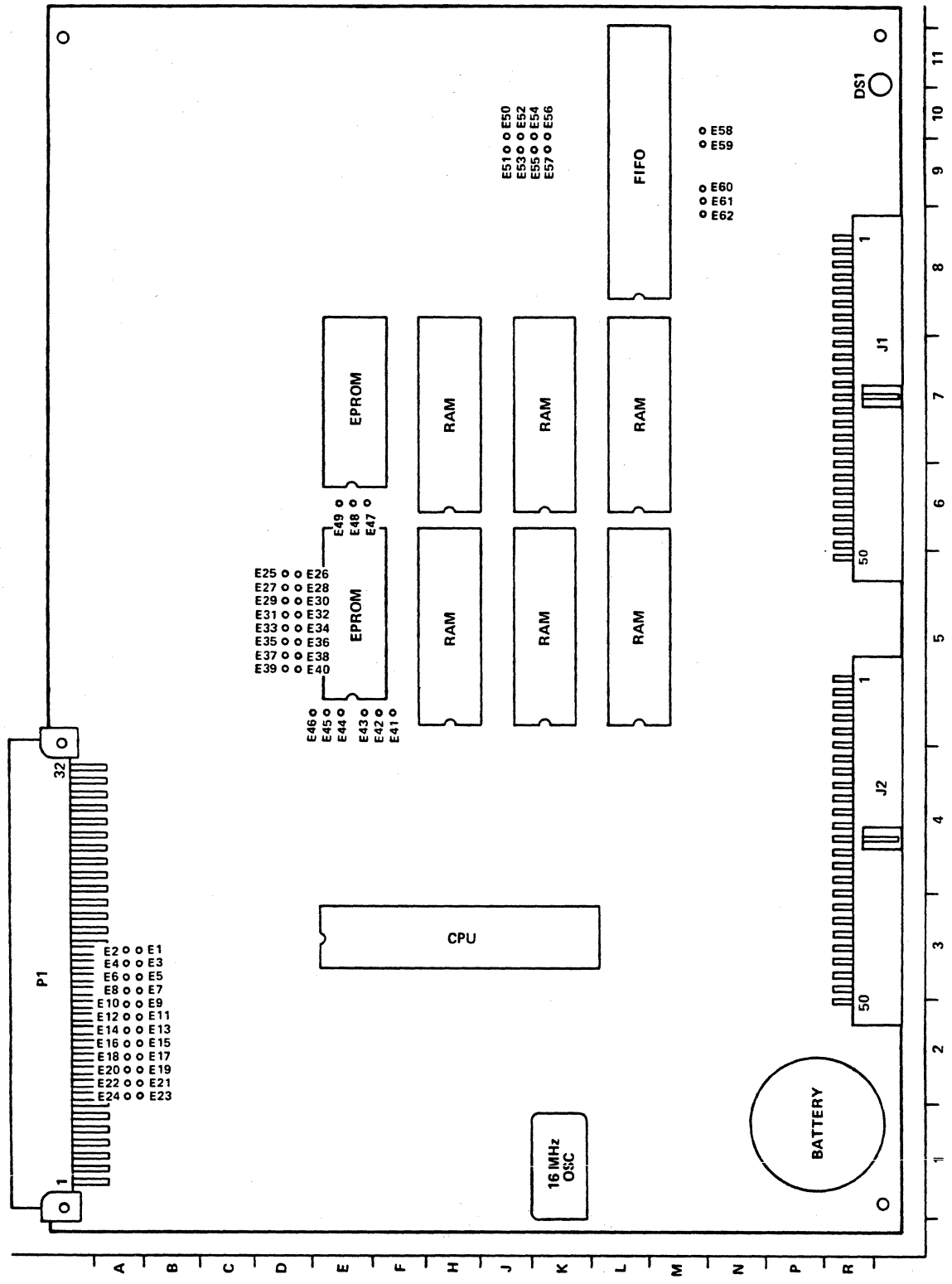
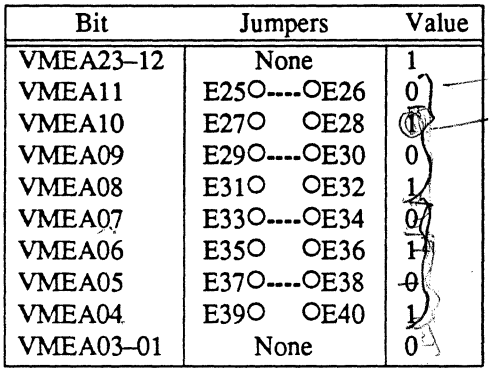


Figure 3-1. VME-TC50 Board Layout

3.1.3 Address Jumpers (E25–E40)

Jumpers E25–E40 set the VME-TC50 address location on the VME bus within the address range of FFF000 and FFFFF0 (hex).

Jumper posts E25–E40 are grouped as eight jumper pairs that correspond to the VME bus address bits as shown in Figure 3-2. The address bits may be set to 1 (no jumper) or 0 (jumper installed). As an example, the jumper configuration shown in the figure is the factory default, FFF550.



Bit	Jumpers	Value
VMEA23–12	None	1
VMEA11	E25O----OE26	0
VMEA10	E27O OE28	1
VMEA09	E29O----OE30	0
VMEA08	E31O OE32	1
VMEA07	E33O----OE34	0
VMEA06	E35O OE36	1
VMEA05	E37O----OE38	0
VMEA04	E39O OE40	1
VMEA03–01	None	0

Figure 3-2. VME-TC50 Address Jumpers

3.1.4 EPROM Socket Configuration Jumpers (E44–E46)

Jumpers E44–E46 configure the EPROM sockets to accommodate either 2K x 8 (2716) or 4K x 8 (2732) EPROMs. Integrated Solutions' firmware is resident on 4K x 8 EPROMs so the factory default setting is E44 to E45. The jumper settings are summarized in Table 3-3.

Table 3-3. EPROM Jumper Settings

EPROM	Jumper Setting
2716	E45 to E46
2732	E44 to E45

3.1.5 Timeout Jumpers (E50–E57)

The VME-TC50 has a timer that monitors the duration of the VME bus cycles. The timer can be set to send a timeout to the on-board microprocessor if the VME cycle exceeds 16, 32, 64, or 128 microseconds. The factory default is set for 16 microseconds. Table 3-4 summarizes the timer jumper configurations.

Table 3-4. Timeout Jumper Settings

Duration	Jumper Setting
16 microseconds	E50 to E51
32 microseconds	E52 to E53
64 microseconds	E54 to E55
128 microseconds	E56 to E57

3.1.6 Odd/Even Parity Select Jumpers (E58–E62)

Jumpers E58–E62 enable you to select odd or even parity. The factory default for the VME-TC50 is for odd parity with the appropriate jumper configuration as shown in Table 3-5.

Table 3-5. Parity Jumper Settings

Parity	Jumper Settings
Odd	E58 to E59 E61 to E62
Even	E60 to E61

3.2 Switch Settings (SW1)

There is one four-bit switch bank located on the VME-TC50 board. The switch settings select base interrupt vector, tape transport operation mode, and interrupt level.

3.2.1 Interrupt Vector

Switch 1 (SW1-1) on the switch bank selects the base interrupt vector. If the switch is open, Vector 0 (94) is selected; if closed, Vector 1 (98) is selected.

3.2.2 Tape Transport Mode

SW1-2 on the switch bank selects the tape transport mode. If the switch is open, start/stop mode is selected; if closed, streaming mode is selected.

In streaming mode, a command can be issued to the transport whenever Data Busy (IDBSY) is inactive, as long as the command is the same mode (Read or Write) and the same direction, independent of the state of Formatter Busy. If buffering is disabled, the transfers to/from the tape transport and to/from the host memory take place concurrently. (With very high transfer rate drives, this could cause overruns.)

3.2.3 Interrupt Level

The VME bus supports seven levels of interrupts, 1–7, with Level 7 being the highest priority. The VME-TC50 can select any one interrupt level from Levels 4–7. Levels 1–3 are not selectable. The VME-TC50 interrupt level is selected via Bits 3 and 4 on the switch bank in accordance with the information given in Table 3-6. The VME-TC50 factory default setting is for interrupt Level 4.

Table 3-6. Interrupt Level Switch Settings

Level	SW-3	SW-4
7	open	open
6	open	closed
5	closed	open
4	closed	closed

SECTION 4: TAPE CONTROL SOFTWARE INTERFACE

4.1 Overview

The VME-TC50 utilizes command packets, stored in system memory, to receive commands from a host. Some commands have various subcommands called modes. A set of device interface registers are used to initiate command packet processing and to retrieve basic status. This section describes register manipulation and provides an overview of the packet protocols (the format used to transfer commands, data, and extended status). Table 4-1 provides a command summary. A detailed description of each command is contained in Section 4.4.

Table 4-1. VME-TC50 Command Summary

Command Name	Mode Name/Description
GET STATUS	Get Status (update the extended status registers in the message buffer in memory)
READ	Read Next (Forward) Reread Previous (Space Reverse, Read Forward)
WRITE CHARACTERISTICS	Load Message Buffer Address and Set Device Characteristics
WRITE	Write Data Write Data Retry (Space Reverse, Erase, Write Data)
POSITION	Space Records Forward Space Records Reverse Skip Tape Marks Forward Skip Tape Marks Reverse Rewind
FORMAT	Write Tape Mark Erase Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)
CONTROL	Message Buffer Release Rewind and Unload Clean Tape (handled as NO-OP)
INITIALIZE	Controller Initialize

The VME-TC50 tape subsystem uses three device registers to support tape control functions. These registers occupy two VME bus word locations. The device registers are

- Status Register (TSSR)
- Command Pointer Register (TCPR)
- Extended Command Pointer Register (TXCPR)

The TCPR and TXCPR form a 24-bit register that is loaded from the VME bus to initiate an operation. The TCPR is a read/write register; the TXCPR is a write-only register. To initiate a command, the TXCPR should be loaded by a word (16-bit) VME bus write with the high-order eight-bit portion of a 24-bit command pointer. Subsequently, the TCPR should be loaded by a word (16-bit) VME bus write with the low-order portion of the command pointer. The command pointer is then used by the VME-TC50 to retrieve the command packet from system memory. The contents of the command packet instruct the controller regarding the operations that are to be performed. The command packet also defines any function parameters such as a data buffer address, a byte count, a record count, and modifier flags.

The TSSR is a 16-bit read-only register maintained by the VME-TC50. Major tape controller and drive status are contained in this register.

When a command is to be processed, a command packet must first be assembled in system main memory. The command packet ranges in length from one word (two bytes) to four words (eight bytes) long. All command packets must begin on a word boundary. The words in the command packet can be thought of as the contents of three registers:

- Command Register (CMDR)
- Data Pointer Register (DPR)
- Positive Byte Count Register (BPCR)

The CMDR contains the code for one of the commands listed in Table 4-1. The DPR contains the address of the data buffer to be processed. The DPR is a two word (32-bit) field. It consists of a low-order address word containing the low order 16 bits of the data pointer, followed by a high-order address word containing the high order eight bits of the data pointer. When the command being used does not involve a data buffer, the two DPR words are not used in the data packet, and the BPCR immediately follows the CMDR.

When the command is processed by the VME-TC50, a message buffer located in system memory is built to return information to the host. The VME-TC50 requires that a message buffer address be supplied via a Write Characteristics command. The Write Characteristics command must be the first command issued following an initialize. Until a Write Characteristics command is issued, all other commands will be rejected.

The BPCR is used to indicate the number of bytes to be read or written during a data transfer. It is also used to specify the number of records in a Space Records command or the number of filemarks in a Skip Tape Marks command. The CMDR specifies the function to be executed by the VME-TC50.

4.2 Register Definitions

The VME-TC50 tape subsystem maintains three registers on the VME bus and five more remote registers in the message buffer area of system memory. The VME bus registers are

- TCPR
- TXCPR
- TSSR

The remote registers in the message buffer are Extended Status Registers 0-4 (XST0 - XST4). Register formats and bit definitions for all of these registers are contained in the sections that follow.

4.2.1 Command Pointer Register (TCPR)

The TCPR is a 16-bit write-only VME bus register located at the first VME bus address (VMEbase). This register should be written only with a 16-bit VME bus operation to specify the low-order 16 bits of the command pointer. (The high-order eight bits of the command pointer should have previously been written to the TXCPR register.) The VME-TC50 responds whenever the TCPR location is written, but the controller is only activated when the SSR bit in the TSSR is set. If SSR is not set, the Register Modification Refused (RMR) bit in the TSSR is set, and the new command pointer is ignored.

The TCPR register is illustrated in Figure 4-1; the bits are defined in Table 4-2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

Figure 4-1. TCPR Register Format

Table 4-2. TCPR Register Bit Definitions

Bit	Name	Definition
15	P15	Command Pointer Bit 15
14	P14	Command Pointer Bit 14
13	P13	Command Pointer Bit 13
12	P12	Command Pointer Bit 12
11	P11	Command Pointer Bit 11
10	P10	Command Pointer Bit 10
9	P09	Command Pointer Bit 9
8	P08	Command Pointer Bit 8
7	P07	Command Pointer Bit 7
6	P06	Command Pointer Bit 6
5	P05	Command Pointer Bit 5
4	P04	Command Pointer Bit 4
3	P03	Command Pointer Bit 3
2	P02	Command Pointer Bit 2
1	P01	Command Pointer Bit 1
0	P00	Command Pointer Bit 0

4.2.2 Extended Command Pointer Register (TXCPR)

The TXCPR is a 16-bit write-only VME bus register located at the VME bus base address + 2 (VMEbase + 2). This register should be written with a 16-bit VME bus operation to specify the high-order eight bits of the 24-bit command pointer. The low-order 16 bits of the command pointer should subsequently be written to the TCPR register. The TXCPR need not be reloaded for subsequent command pointers, unless the contents must be altered. (When changed, it must be loaded prior to loading the TCPR.) The TXCPR is cleared by an initialize.

Writing into the TXCPR with the high order data bit set to 1 causes an initialize, while writing with the high order data bit set to 0 loads the TXCPR. The VME-TC50 responds whenever the TXCPR location is loaded. However, data is only accepted when the SSR bit in the TSSR is set. If SSR is not set, the Register Modification Refused (RMR) bit in the TSSR is set, and the new command pointer is ignored.

The TXCPR register is illustrated in Figure 4-2 and the bits are defined in Table 4-3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	0	0	0	0	0	0	0	P23	P22	P21	P20	P19	P18	P17	P16

Figure 4-2. TXCPR Register Format

Table 4-3. TXCPR Register Bit Definitions

Bit	Name	Definition
15	RST	This bit causes an initialize†
14-8	-	Set to 0 (bits are not used)
7	P23	Command Pointer Bit 23
6	P22	Command Pointer Bit 22
5	P21	Command Pointer Bit 21
4	P20	Command Pointer Bit 20
3	P19	Command Pointer Bit 19
2	P18	Command Pointer Bit 18
1	P17	Command Pointer Bit 17
0	P16	Command Pointer Bit 16

† *If Reset is set to one*

4.2.3 Status Register (TSSR)

The TSSR is a sixteen bit read-only VME bus register located at the VMEbase address +2. The TSSR contains the major status of the drive and controller.

The TSSR register format is illustrated in Figure 4-3 and the bit definitions are contained in Table 4-4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC	-	SCE	RMR	NXM	NBA	-	-	SSR	OFL	FC1	FC0	TC2	TC1	TC0	-

Figure 4-3. TSSR Register Format

Table 4-4. TSSR Register Bit Definitions

Bit	Name	Definition
15	SC	Special Condition — When set, indicates that the last command was not completed without incident: either an error was detected or an exception condition (e.g., tape mark on read, reverse motion at BOT) occurred. Also set by the error bits in TSSR: RMR and NXM. Indicates that the Termination Class (TC) bits are nonzero (unless RMR is the only error — see RMR). SC is cleared by initialize.
14	—	Not used; always set to 0.
13	SCE	Sanity Check Error — Set when the controller detects an internal error. This is considered serious enough that a message buffer is not sent out. (Causes TC7.)
12	RMR	Register Modification Refused — Set when the TCPR or the TXCPR is written from the VME bus and Subsystem Ready (SSR) is not set. Causes the SC bit to be set, but no TC (the VME-TC50 never sees the data written) because on a system with no bugs, RMR can be set if TSDB is written while an ATTN message is being output. If ATTNs are not enabled, RMR setting indicates a fatal controller or software bug.
11	NXM	Non-existent memory — Set when trying to do a DMA transfer to/from memory and a VME bus error occurs (BERR* is asserted). May occur when fetching a command packet, fetching or storing data, or storing the message packet.

Table 4-4. (Continued)

Bit	Name	Definition
10	NBA	Need Buffer Address — When set, indicates that the VME-TC50 needs a message buffer address. Set by initialize. Cleared during the Write Characteristics command (if a valid address was given). If NBA is set and any command other than Write Characteristics is given, the operation is terminated with function reject.
9-8	—	Not used; always set to 0.
7	SSR	Subsystem Ready — When set, indicates that the VME-TC50 is not busy and is ready to accept a new command pointer. Cleared by writing the TCPR with a new command pointer. Also cleared by initialize, then set if the internal diagnostics are passed.
6	OFL	Off-Line — When set, indicates that the tape transport is off-line and unavailable for any commands requiring tape motion. This bit can cause a TC of 1 (on an ATTN interrupt) or 3 (results in Nonexecutable Function (NEF) status). This bit does not indicate the current status of the transport; it is updated only upon command completions.
5-4	FC<1:0>	Fatal Termination Class Code — Used to indicate the type of fatal error that occurred on the VME-TC50. The code is valid only when the SC bit is set and the TC code bits are all set (111); they are clear otherwise. The FCs are as follows: 0 Internal diagnostic error. Initialize must be issued for the controller to accept further commands. 1–3 Reserved.

Table 4-4. (Continued)

Bit	Name	Definition
3-1	TC<2:0>	Termination Class Code — Each of the eight possible values of this three-bit field represents a particular class of errors or exceptions. The conditions in each class have similar significance and recovery procedures (where applicable). The codes are 0 Normal Termination. 1 Attention Condition. 2 Tape Status Alert. 3 Function Reject. 4 Recoverable Error — Tape position is one record down tape from start of function. 5 Recoverable Error — Tape has not moved. 6 Unrecoverable Error — Tape position lost. 7 Fatal Controller Error — (see fatal class codes).

4.2.4 Extended Status Register 0 (XST0)

XST0 appears as the fourth word in the message buffer returned by the VME-TC50 upon completion of a command or on an ATTN.

The XST0 register is illustrated in Figure 4-4. Bits are defined in Table 4-5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	-	WLK	BOT	EOT

Figure 4-4. XST0 Register Format

Table 4-5. XST0 Register Bit Definitions

Bit	Name	Definition
15	TMK	Tape Mark Detected — Set whenever a tape mark is detected during a Read, Space or Skip command, and also as a result of the Write Tape Mark or Write Tape Mark Retry commands.
14	RLS	Record Length Short — This bit indicates that either the record length was shorter than the byte count on read operations, a space record operation encountered a tape mark or BOT before the position count was exhausted, or a Skip Tape Marks command was terminated by encountering BOT or a double tape mark (if that operational mode is enabled, see LET and ESS) prior to exhausting the position counter.
13	LET	Logical End of Tape — Set only on the Skip Tape Marks command when either two contiguous tape marks are detected, or when moving off of BOT and the first record encountered is a tape mark. The setting of this bit does not occur unless this mode of termination is enabled through use of the Write Characteristics command.
12	RLL	Record Length Long — When set, indicates that the record read was longer than the byte count specified.
11	WLE	Write Lock Error — When set, indicates that a write operation was issued, but the mounted tape did not contain a write enable ring.
10	NEF	Nonexecutable Function — When set, indicates that a command could not be executed due to one of the following conditions: • The command specified reverse tape direction, but the tape was already at BOT. • The issuing of any motion command when the Volume Check (VCK) bit is set. • Any command, except Get Status or Initialize, when the transport is off-line. • Any Write command when the tape does not contain a write enable ring (also causes write lock status - WLE).

Table 4-5 (Continued)

Bit	Name	Definition
9	ILC	Illegal Command — Set when a command is issued and either its command field or its mode field contains codes that are not supported by the VME-TC50.
8	ILA	Illegal Address — Set when a command specifies an odd address where an even one is required.
7	MOT	Motion — Tape is moving. Indicates that the transport is asserting formatter busy or rewinding status.
6	ONL	On Line — When set, indicates that the attached tape transport is on line and operable. A change in this bit can cause a termination class of 1 (ATTN interrupt, if ATTNs are enabled). When clear and a command requiring motion is issued, causes NEF (TC 3).
5	IE	Interrupt Enable — Reflects the state of the IE bit supplied on the last command.
4	VCK	Volume Check — When set, indicates that the attached tape transport is either off-line or powered down. Cleared by the Clear Volume Check (CVC) bit in the command header word. This bit can cause a termination class of 3 (TC 3).
3	—	Not used; always set to 0.
2	WLK	Write Locked — When set, indicates that the mounted tape does not contain a write ring. The tape is, therefore, write protected.
1	BOT	Beginning of Tape — When set, indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape.
0	EOT	End of Tape — This bit is set whenever the tape is positioned at or beyond the EOT reflective strip. Does not reset until the tape passes over the detector in the reverse direction under program control. If the controller is read buffering (prereading records from tape automatically) and the EOT strip is seen, this bit is not set until the program actually requests the record associated with the EOT.

4.2.5 Extended Status Register 1 (XST1)

XST1 appears as the fifth word in the message buffer returned by the VME-TC50 upon completion of a command or on an ATTN. The XST1 register is shown in Figure 4-5. Bits are defined in Table 4-6.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLT	-	COR	-	-	-	-	RBP	-	-	-	-	-	-	UNC	-

Figure 4-5. XST1 Register Format

Table 4-6. XST1 Register Bit Definitions

Bit	Name	Definition
15	DLT†	Data Late — Set whenever the internal FIFO buffer is full on a read and the tape transport attempts to enter another byte, or when it is empty on a write and the transport requests another byte. These conditions occur whenever the bus registers are being polled so often as to not allow the controller time to transfer sufficient data to/from the FIFO or if the drive transfer rate exceeds the throughput of the controller.
14	—	Not used; always set to 0.
13	COR	Correctable Data — When set, indicates that a correctable data error has been encountered while reading or writing. On a write, this bit causes a termination class of 4. On a read, the termination class is 0 (no corrective action required).
12-9	—	Not used; always set to 0.
8	RBP	Read Bus Parity Error — Set when the controller detects a parity error on the read data lines of the transport bus (during a read or a write). If this parity error is also detected by the tape transport, the UNC bit is also set. The problem is most likely in the bus drivers in the tape transport, the bus receivers in the controller, or in the tape transport bus cable.
7-2	—	Not used; always set to 0.
1	UNC	Uncorrectable Data or Hard Error — Set in response to the tape transport assertion of Hard Error during a read or a write to indicate that an uncorrectable data error has occurred.
0	-	Not used; always set to 0.

† *Instances of Data Late may be experienced under certain conditions when the VME-TC50 is supporting tape drives with higher data transfer rates (e.g., 6250 bpi tape drives). These data overruns can occur under the following conditions: the VME-TC50 is set for streaming mode, byte swapping is turned on for the read/write command, data transfer block size is greater than 512 bytes per block, and the data transfer rate is greater than 200 Kbytes/second. The recommended solution for such DLT problems is to operate the VME-TC50 in start/stop mode (turn VME-TC50 switch SW1-2 off).*

4.2.6 Extended Status Register 2 (XST2)

XST2 appears as the sixth word in the message buffer returned by the VME-TC50 upon completion of a command or on an ATTN.

The XST2 register is illustrated in Figure 4-6; the bits are defined in Table 4-7. Note that the low-order eight bits of this register have special meaning for the Write Characteristics command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPM	-	-	-	-	WCF	-	-	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0

Figure 4-6. XST2 Register Format

Table 4-7. XST2 Register Bit Definitions

Bit	Name	Definition
15	OPM	Operation in Progress — Tape Moving.
14-11	—	Not used; always set to 0.
10	WCF	Write Clock Failure — Set during a write to indicate that the internal FIFO is not being emptied by the transport.
9-8	—	Not used; always set to 0.
7-0	RL<7:0>	Revision Level — On a Write Characteristics command, this field displays the firmware revision level. On all other commands, Bits 2-0 show the unit number of the currently selected transport.

4.2.7 Extended Status Register 3 (XST3)

XST3 appears as the seventh word in the message buffer returned by the VME-TC50 upon completion of a command or on an ATTN.

The XST3 register is illustrated in Figure 4-7; the bits are defined in Table 4-8.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	OPI	REV	-	-	-	-	RIB

Figure 4-7. XST3 Register Format

Table 4-8. XST3 Register Bit Definitions

Bit	Name	Definition
15-7	-	Not used; always set to 0.
6	OPI	Operation Incomplete — Set when read, space, or skip operation runs for approximately 120 seconds without detecting any data on the tape.
5	REV	Reverse — Set when the current operation causes reverse tape motion (includes the Retry commands as well as simply Reverse Read, Space, etc.); clear when operation is forward or rewind.
4-1	-	Not used; always set to 0.
0	RIB	Reverse into BOT — When set, indicates that a Read, Space, Skip, or Retry command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion halts at BOT.

4.2.8 Extended Status Register 4 (XST4)

XST4 appears as the eighth word in the message buffer returned by the VME-TC50 upon completion of a command or on an ATTN. The XST4 register is illustrated in Figure 4-8; the bits are defined in Table 4-9.

NOTE

For XST4 to be stored, the message buffer extent parameter specified in the Write Characteristics command must be 16 bytes instead of the minimum 14 bytes.

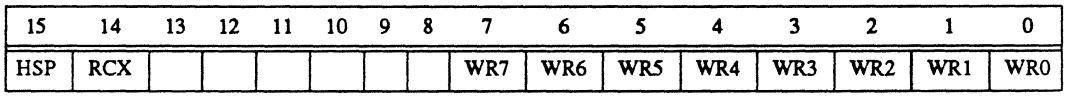


Figure 4-8. XST4 Register Format

Table 4-9. XST4 Register Bit Definitions

Bit	Name	Definition
15	HSP	High Speed — When set, indicates that a dual-speed transport is operating in high-speed mode. When clear, a dual-speed transport is operating in low speed mode.
14	RCX	Retry Count Exceeded — When set, indicates that the controller is buffering write data and cannot successfully output the buffered record within the specified number of retries. Causes tape position lost termination.
13-8	-	Not used; always set to 0.
7-0	WR<7:0>	Write Retry Count Statistic — When the controller is buffering write data records, this field indicates the total number of controller-initiated retries performed in order to write the previous buffered record. This count is cleared after it is displayed. For example, consider the situation in which (1) buffering is in operation and record N is in VME-TC50 RAM (the controller has given success- ful termination for record N), (2) the Write command for record N+1 has been issued to the controller, but the controller has not yet returned termination status for the command, and (3) the controller must perform M retries to finally write record N successfully. In this situation, M appears in the WR field when termination of record N+1 is finally returned.

4.3 Packet Processing

The CPU passes control information to the VME-TC50 via a command packet located in system main memory. Similarly, the controller returns status information to the host via a message packet located in system main memory. A command is initiated by the CPU writing the location of the command buffer into the TXCPR and TCPR registers. The controller then becomes busy, fetches the command and associated parameters from the command buffer, executes the command, stores the status into the message buffer, interrupts the host (if so programmed), and becomes idle. The CPU then examines the TSSR and the extended status in the message buffer to determine the success or failure of the command. Every command is handled in this basic manner. The following sections discuss buffer control, message buffer format, and attention handling.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACK	Device Dependent			Mode Code				Format Code			Command Code				
Low-Order Data Pointer Address A<15:0>															
High-Order Data Pointer Address A<23:16>															
Count Parameter															

Note: Not all words are required for all commands.

Figure 4-9. Command Packet Format

4.3.1 Buffer Ownership and Control

To prevent the controller from updating the message buffer while the CPU is reading it, or the CPU from updating the command buffer while the controller is reading it, the concept of ownership is defined. Each buffer may be owned by either the controller or the CPU. A buffer can only be modified by the current owner. Ownership of a buffer may only be transferred by its current owner.

There are four different combinations of transferring the two buffers in the two directions:

- Command Buffer: CPU to controller (by the CPU)
- Command Buffer: controller to CPU (by the controller)
- Message Buffer: CPU to controller (by the CPU)
- Message Buffer: controller to CPU (by the controller)

Table 4-10 describes the buffer transfer operations.

An initialize aborts any current operation and gives ownership of both the command buffer and the message buffer to the CPU.

Table 4-10. Buffer Ownership Transfers

Buffer	Direction	Transfer Method
Command Buffer	CPU to the Controller	The CPU transfers ownership of the command buffer to the controller by writing the address of the command buffer into the TCPR register. This clears the SSR bit in the TSSR.
Command Buffer	Controller to the CPU	The controller transfers ownership of the command buffer back to the CPU by depositing a message packet (in the message buffer) that has the Acknowledge (ACK) bit set in the message header word. After the message is deposited by the controller, it sets the SSR bit in the TSSR to indicate that the message is in the message buffer. If the message does not contain the ACK bit set, the CPU knows that the controller did not see the last command buffer and that the CPU still owns the command buffer. The command may be re-issued by the CPU.
Message Buffer	CPU to the Controller	The CPU transfers ownership of the message buffer to the controller by setting the ACK bit in the command buffer and then initiating the command by writing the command buffer address into the TCPR. If the command buffer does not contain the ACK bit, the controller knows that the CPU did not see the last message buffer and the controller still owns it. In this case, the controller, in response to the CPU writing into TCPR sets SSR and performs an interrupt (if the Interrupt Enable (IE) is set) without sending out a message.

Table 4-10. (Continued)

Buffer	Direction	Transfer Method
Message Buffer	Controller to the CPU	The controller transfers ownership of the message buffer to the CPU by writing the message buffer, setting the SSR bit and interrupting if IE is set. This happens at the following two times: • At the end of a command. • By outputting an ATTN message. In this case, SSR is already set because ATTN only happens when the controller is inactive. Therefore, the controller clears SSR, outputs the message, and then sets SSR again (and interrupts if the IE bit was set on the message buffer release command that gave control of the message buffer to the controller). Note that for an ATTN to occur, the Enable Attention Interrupt (EAI) bit must have been set in the previous Write Characteristics command.

During normal command processing, the ownership of both buffers passes simultaneously, first from CPU to controller (at the start of command processing, when the CPU writes a command pointer into the TSDB register), and then from controller to CPU (upon completion of the command).

4.3.2 Buffer Control on Attentions

An Attention (ATTN) is enabled by the CPU setting up the appropriate characteristics mode word on the Write Characteristics command (EAI = 1). It allows the controller to flag exceptional conditions (e.g, a change in transport on-line/off-line status, or diagnostic self-test errors) when the controller is in the idle state (not executing a command).

If an ATTN condition occurs and the controller does not own the message buffer, the controller queues the ATTN internally. Then, when the CPU releases the message buffer on the next command (with the ACK bit set), the controller outputs the ATTN message with the ACK bit clear in the message header word to indicate that the command was lost (except for the transfer of ownership of the message buffer to the controller). In this case, the controller refuses to accept ownership of the command buffer. The CPU, then, still owns the command buffer (because the controller did not accept the command) and also owns the message buffer now filled with an ATTN message. If the CPU still wants to execute the ignored command, the command must be re-issued (with the ACK bit set).

An exception to this procedure is the Write Characteristics command, which is executed regardless of a pending ATTN. This exception is necessary to allow the software to specify a message buffer address and control enabling of ATTNs.

Consider the case where the CPU wants to be notified of a change in status while the controller is inactive for a long period of time. To accomplish this, the controller must own the message buffer for that entire period of time. Normally, the controller gives up ownership of the message buffer at the end of a command. However, for enabling ATTN messages, ownership of the message buffer is transferred to the controller via the Message Buffer Release command. This is a special command that tells the controller not to give ownership of the message buffer back to the CPU at the end of the command.

The controller does not output a message at the end of this command, but just updates the TSSR register (with the SSR bit set) and interrupts (if the IE bit was set in the command and such an interrupt was enabled by the Enable Release Interrupt (ERI) bit) in the previous Write Characteristics command. The controller maintains ownership of the message buffer until an ATTN condition is seen, and then immediately clears SSR, outputs the ATTN message (with the ACK bit not set since the controller is not responding to a command), and then sets SSR and interrupts the CPU (if the IE bit was set on the Message Buffer Release command).

During this process, the CPU owns the command buffer and the controller owns the message buffer. If the controller outputs an ATTN message, ownership of the message buffer is passed back to the CPU. At that time, the system is back to the state of the CPU owning both buffers. Another ATTN is not done until the CPU does a command with the ACK bit set to release ownership of the message buffer containing the ATTN message.

If the CPU has done a Message Buffer Release command and wants to issue another command, but has not received an ATTN from the controller (so that the controller still owns the message buffer from the Message Buffer Release command), the CPU can issue a command without the ACK bit set in the command buffer. (At the time the command is issued, the CPU does not own the message buffer, so the CPU cannot release the message buffer.) If the CPU does set the ACK bit, nothing happens except the CPU might miss an ATTN if the controller was sending out an ATTN message at the same time that the CPU was issuing the command.

It is possible that the CPU may attempt to initiate a new command at or near the same time that the controller attempts to output an ATTN message. (The command must not have the ACK bit set since the CPU does not own the message buffer.)

If the CPU writes the TCPR register while SSR is clear during an ATTN, the RMR error bit is set and that command is ignored. The ATTN message does not have the ACK bit set since the controller does not own the command buffer. Note that RMR may get set in this way on a bug-free system. All other settings of RMR indicate a software bug (the CPU tried to issue a command before the previous command was completed).

If the CPU command is lost because the controller is outputting an ATTN message, VCK and IE are not updated. If the CPU command is rejected (illegal command, etc.) and not ignored, VCK and IE are updated to the start of the rejected command.

4.3.3 Message Packet Format

Figure 4-10 illustrates the format of the message packet. This format is used for all messages, whether at an end of a command or for an ATTN. The message consists of a header word, a data field length word, a residual byte/record/tape-mark count word, and either four or five extended status registers. Normally, only four extended status registers are provided. The fifth one (XST4) is available only when enabled by the appropriate Write Characteristics command. Table 4-11 describes the message packet. Tables 4-12 and 4-13 provide the message code and termination class code descriptions, respectively.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Reserved			Class Code				Format 1			Message Type				
ACK	0	0	0	0	0	C	C	0	0	0	m	m	m	m	m
Reserved								Data Field Length							
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0
RBCPR															
XST0															
XST1															
XST2															
XST3															
XST4†															

Figure 4-10. Message Packet Format

† *Note: XST4 is available only when enabled via the Write Characteristics command.*

Table 4-11. Message Packet Field Definitions

Word	Bit	Description
1	15	ACK (Acknowledge) — This bit is set by the VME-TC50 to inform the CPU that the command buffer is now available for subsequent command packets. On an ATTN message, this bit is not set since the controller does not own the command buffer.
1	14-12	Reserved — These bits are reserved for future enhancements. They always appear as zero.
1	11-8	Class Code Field — These bits define the class of failure determined for the rest of the message buffer when the message type field is not indicating a normal END message. The codes are described in Table 4-12:
1	7-5	Packet Format 1 Field — The only value supported by the VME-TC50 is 000, which specifies a one-word message header.
1	4-0	Message Type Code — This field, together with the format field, indicates the format and length of message packets. For the VME-TC50, the message type is of the form 10xxx, which indicates that the message contains a header word, and then xxx data/status words. This field indicates the general type of message contained in the buffer and is related to the termination class code appearing in the TSSR register (see Table 4-13):
2	15-8	Not used; always set to 0.
2	7-0	Data Field Length — This field specifies how many bytes of information follow this word in the message packet. Normally, with the extended features mode of the VME-TC50 disabled, this field contains a value of 10 (00001010), indicating that the packet contains the RBPCR plus four extended status registers. With the extended features mode enabled, this field contains a value of 12 (00001100) to indicate that an additional extended status register (XST4) is supplied.

Table 4-11. (Continued)

Word	Bit	Description
3	15-0	Residual Byte/Record/File Count Register — After a Read command, this word contains the difference between the number of bytes specified in the command and the number of bytes actually transferred from tape. In other words, this register indicates by how much the tape record fell short of the expected length. After a Space Records or Skip Tape Marks command, this register contains the difference between the number of records or tape marks specified in the count word of the command and the number of records or files actually skipped. Note that spacing and skipping operations can terminate before the count is exhausted for a variety of reasons (e.g, tape mark, BOT).
4	15-0	Extended Status Register 0 — See Section 4.2.4 for a description of this register.
5	15-0	Extended Status Register 1 — See Section 4.2.5 for a description of this register.
6	15-0	Extended Status Register 2 — See Section 4.2.6 for a description of this register.
7	15-0	Extended Status Register 3 — See Section 4.2.7 for a description of this register.
8	15-0	Extended Status Register 4 — See Section 4.2.8 for a description of this register.

Table 4-12. Termination Class Code Description

Message Type	Class Code	Definition
ATTN	0000	On line or off line.
FAIL	0000	Not used.
FAIL	0001	Illegal Command (ILC), Illegal Address (ILA), or NBA on a tape motion command.
FAIL	0010	Write-lock error on nonexecutable function.
FAIL	0011	Diagnostic error.

Table 4-13. Message Code Descriptions

Termination Class Code	Message Type	Definition
0,2	10000	End
3	10001	Fail
4,5,6,7	10010	Error
1,7	10011	Attention

4.3.4 General Status Handling Information

Table 4-14 summarizes the relationship between the termination class code (appearing in the TSSR register) and the message type code (appearing in the header word of the message buffer after a message packet has been deposited by the controller).

Table 4-14. Termination Class/Message Type Relationship

TC2-0 Value	Message Type	Meaning
0	END	Normal Termination — The operation completed without incident.
1	ATTN	Attention Condition — This code indicates that the drive has undergone a status change, such as going off-line or coming on line.
2	END	Tape Status Alert — A status condition is encountered that may have significance to the program. Bits of interest in the extended status registers include TMK, EOT, RLS, and RLL.
3	FAIL	Function Reject — The specified function was not initiated. Bits of interest include OFL, VCK, BOT, WLE, ILC, and ILA.

Table 4-14. (Continued)

TC2-0 Value	Message Type	Meaning
4	ERROR	Recoverable Error — Tape position is one record beyond what its position was when the function was initiated. Suggested recovery procedure is to log the error and issue the appropriate Retry command.
5	—	Not used.
6	ERROR	Unrecoverable Error — Tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers. Recovery is handled by the specific application program.
7	ATTN	Fatal Subsystem Error — The subsystem is incapable of properly performing commands, or at least its integrity is seriously questionable. Refer to the fatal class code field in the TSSR register for additional information on the type of fatal error.

The following points should be noted in reference to status and error handling:

1. Error bits in the TSSR register (SC and RMR) are cleared by successfully loading a command pointer into the TCPR register and by successfully depositing an END message.
2. All commands (even the Get Status command) clear the internal copy of each error bit in the extended status registers. Therefore a Get Status command does not return the error bits as set up by a previous tape operation.
3. A read operation that encounters a TMK does not transfer any data and gives a Tape Status Alert termination. The TMK and RLS status bits are set, and the RBPCR word in the message buffer contains the original byte count as specified in the command.
4. A space records operation automatically terminates when a tape mark is traversed, and the TMK status bit is set. Also, RLS is set if the record count is not decremented to zero.
5. A skip tape marks operation automatically terminates when two consecutive tape marks are encountered and the Enable Skip Stop (ESS) mode is enabled via the Write Characteristics command. RLS is set if the count is not decremented to zero. The same is also true if a tape mark is the first record of BOT and both the ESS and ENB bits were set in the previous Write Characteristics data word.
6. Every Write, Write Retry, Write Tape Mark, Write Tape Mark Retry, and Erase command that is executed with the transport EOT signal active results in a Tape Status Alert termination.
7. A Read Reverse, Space Reverse, Reverse, or Skip Tape Marks Reverse command that encounters BOT after the operation is underway results in a tape status alert termination (the RIB status bit is set).
8. If a Read Reverse, Space Records Reverse, or Skip Tape Marks Reverse command is issued while the tape is already at BOT, a function reject (nonexecutable function) status is returned.
9. When a Rewind command is issued, the termination message and interrupt does not occur until the tape reaches BOT and has stopped. If the tape is already at BOT when the command is

issued, the transport is still commanded to rewind to ensure proper tape positioning.

10. Certain failures can result in no interrupt even though the specified command had IE set. These failures include Nonexistent Memory Error (NXM), since the failure could have occurred before the IE bit was fetched from the command packet.

11. The following are notes concerning interrupts:

    a. When record buffering for writes is in operation, the controller issues normal termination messages and interrupts immediately after the data to be written has been stored in the controller's RAM and before the data is actually written on tape. The possibility exists that the record cannot successfully be written on tape with the first attempt, in which case a retry algorithm is executed to attempt to successfully write the data. If the data is eventually successfully written, the CPU will not know that any problem occurred unless the extended features mode is enabled, in which case the write retry count field in XST4 may be examined in the message termination of the next command.

    b. If record buffering for writes is in operation and the controller cannot write a stored record successfully from its RAM (retry count exhausted), the next command following the Write command associated with the failed record is terminated with Termination Class 6 (tape position lost) and the RCX bit in XST4 is set.

4.4 Commands

The following sections describe the general command format. Then, each command is described in detail.

4.4.1 Command Packet Definitions

Logically, a command packet can be composed of one to four 16-bit words, depending on the type of command and the amount of information the controller needs to proceed with execution. All command packets begin with a command packet header word (see Figure 4-11). The format of this word is the same for all commands; the encoding of the various fields within the word distinguishes one command from another. Table 4-15 defines the fields within the header word. The following sections describe each command in detail, along with its specific command packet format.

Certain bits of the header word and other words within the command packet are not defined for all commands. When building the command packet, all undefined bits should be set to 0. If any undefined bit is not 0 for a specific command, the command is not executed, and is terminated with a Function Reject (Termination Class 3).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	SWB	0	m	m	m	IE	0	0	0	c	c	c	c

Figure 4-11. Command Packet Header Word

Table 4-15. Command Packet Header Word Bit Definitions

Bit	Name	Function
15	Acknowledge (ACK)	This bit should be set when issuing a command and the CPU owns the message buffer. Its function is to inform the VME-TC50 that the message buffer is now available for any pending or subsequent message packets. This passes ownership of the message buffer to the controller. If the CPU has released ownership of the message buffer to the controller for ATTNs and has not yet received an ATTN message, the ACK bit should be 0.
14-12	Device Dependent Bits	These three bits perform functions applicable to particular commands. The bit definitions are defined in Table 4-16.
11-8	Command Mode Field	This field acts as an extension to the command code field and allows further specification of device commands.
7-5	Packet Format #1 Field	This field defines the state of interrupt enable. The only two valid configurations are 000 = interrupt disable 100 = interrupt enable
4-0	Command Code	This field defines the major command category. It is used together with the command mode field to specify the command.

Table 4-16. Device Dependent Bit Definitions

Bit	Name	Definition
14	CVC	Clear Volume Check — When set, the volume check condition, set when the transport goes from off-line to on line, will be cleared, thereby allowing tape operations to be executed on the transport.
13	—	This bit is not used and should be set to 0.
12	SWB	Swap Bytes — When set, instructs the VME-TC50 to alter the sequence of storing and retrieving tape data bytes from the CPU memory. When SWB is 0, the *first* byte in a word is the least significant byte (bits 7–0). When SWB is 1, the industry standard method is specified in which the first byte of a word is considered to be the most significant byte (bits 15–8). Figure 4-12 shows the positions of the bytes in the case of a Forward Read or Write and Reverse Read with even byte count. Figure 4-13 shows the positions of the bytes in the case of a Forward or Reverse Read with odd byte count.

Swap Bytes = 0
Buffer Address = 1000 hex
Byte Count = 8 bytes

1000	1	0
1002	3	2
1004	5	4
1006	7	6

Swap Bytes = 1
Buffer Address = 1000 hex
Byte Count = 8 bytes

1000	0	1
1002	2	3
1004	4	5
1006	6	7

Swap Bytes = 0
Buffer Address = 1001 hex
Byte Count = 8 bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5
1008		7

Swap Bytes = 1
Buffer Address = 1001 hex
Byte Count = 8 bytes

1000		0
1002	1	2
1004	3	4
1006	5	6
1008	7	

Note: Byte 0 indicates the byte nearest to BOT.

Figure 4-12. Memory/Tape Data Byte Positioning (Case 1)

Swap Bytes = 0
Buffer Address = 1000 hex
Byte Count = 7 bytes

1000	1	0
1002	3	2
1004	5	4
1006		6

Swap Bytes = 1
Buffer Address = 1000 hex
Byte Count = 7 bytes

1000	0	1
1002	2	3
1004	4	5
1006	6	

Swap Bytes = 0
Buffer Address = 1001 hex
Byte Count = 7 bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5

Swap Bytes = 1
Buffer Address = 1001 hex
Byte Count = 7 bytes

1000		0
1002	1	2
1004	3	4
1006	5	6

Note: Byte 0 indicates the byte nearest to BOT.

Figure 4-13. Memory/Tape Data Byte Positioning (Case 2)

4.4.2 Get Status Command

Figure 4-14 illustrates the Get Status command packet. This command causes a message packet to be deposited in the message buffer area in order to update the extended status registers. However, after the end of any command except message buffer release, the VME-TC50 automatically updates the extended status registers. Therefore, the Get Status command is generally only used when a status register update is desired with no tape motion.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	0	0	m	m	m	IE	0	0	0	1	1	1	1
Not Used															

Figure 4-14. Get Status Command Packet

4.4.3 Read Command

Figure 4-15 illustrates the command packet for a read operation. There are two normal modes of operation, Read Forward and Reread Previous (see Table 4-17). Reread Previous is further controlled by the state of the OPP bit in the command packet header word.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	SWB	m	m	m	m	IE	0	0	0	0	0	0	1
Low-Order Data Pointer Address															
A15															A0
High-Order Data Pointer Address															
0	0	0	0	0	0	0	0	A23							A16
Buffer Extent (byte count) (16-bit unsigned value)															

Figure 4-15. Read Command Packet

Table 4-17. Read Modes

Mode	Function
0000	Read Next (Forward)
0010	Reread Previous (Space Reverse, Read Forward)

The command packet for a read contains four words: a header word, two words specifying the memory address of the buffer where the data will be stored, and a buffer extent (byte count) word specifying the number of bytes in the data buffer and the number of bytes to be read. A byte count of 0 specifies that 65,536 (64K) bytes are to be read.

The third word in the packet specifies the high order address bits of the data buffer pointer. If any of Bits 15-8 in this word are nonzero, the command is aborted with function reject termination and ILA error status.

The read operation is assumed to be for a record of known length. Therefore, the correct record byte count (fourth word of the packet) must be known. If the byte count exactly equals the record length, normal termination occurs. If the record is shorter than the specified byte count, the RLS error bit in XST0 is set and a Tape Status Alert termination occurs. If the record on tape is larger than the byte count the RLL error bit in XST0 is set and a Tape Status Alert termination again occurs. However, in this case, only the number of bytes specified in the byte count field is transferred to the data buffer. Also, any read operation that encounters a tape mark does not transfer any data. In this case, the TMK and RLS bits are set and a Tape Status Alert termination is returned.

Reread Previous operations that encounter BOT cause the RIB bit in XST3 to be set and a Tape Status Alert termination to be given. If the tape is already positioned at BOT when a Reread Previous command is issued, there is no tape motion and Function Reject termination occurs, with the NEF error bit set in XST0.

4.4.4 Write Characteristics Command

Figures 4-16 and 4-17 illustrate the Write Characteristics command packet format and characteristics data format, respectively. The objective of this command is to inform the VME-TC50 of the location and size of the message buffer. The message buffer must be at least seven contiguous words long (eight for Extended Features mode) and it must be located on a word boundary.

The Write Characteristics command also transfers a characteristics mode word to the controller and an additional control word. The characteristics mode word causes specific actions for certain operational modes. The bits for this word are defined in Table 4-18. Table 4-19 defines the bits in the additional control word.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
Low-Order Characteristic Data Address															
A15															A0
High-Order Characteristic Data Address															
0	0	0	0	0	0	0	0	A23							A16
Buffer Extent (byte count) (16-bit unsigned value)															

Figure 4-16. Write Characteristics Command Format — Command Packet

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Low-Order Message Buffer Address															
A15															A0
High-Order Message Buffer Address															
0	0	0	0	0	0	0	0	A23							A16
Message Buffer Extent (byte count) (16-bit unsigned value >= 14)															
0	0	0	0	0	0	0	0	ESS	ENB	EAI	ERI	0	0	0	0
XIRG Retry Limit				NO-XIRG Retry Limit				RTY		HSP	Buffer Control		Unit Select		

Figure 4-17. Write Characteristics Command Format — Characteristic Data

Table 4-18. Characteristics Mode Data Word Bit Definitions

Bit	Name	Definition
15-8	—	Not used. These bits are not checked by the VME-TC50. Their state does not affect operation but they should be set to 0.
7	ESS	Enable Skip Tape Marks Stop — When set, this bit instructs the controller to stop and set the LET status bit during a Skip Tape Marks command when a double tape mark (two contiguous tape marks) is detected. Setting this bit also enables operation of the ENB bit. When set to 0, the Skip Tape Marks command terminates only on tape mark count exhausted or if it runs into BOT.
6	ENB	Enable Tape Mark Stop Off BOT — This bit is meaningful only if the ESS bit is set. When both bits are set, the tape is at BOT, a Skip Tape Marks command is issued, and the first record seen is a tape mark, the controller halts the operation and sets the LET status bit in XST0. If this bit is clear under the same conditions, the controller merely counts the tape mark and continues.
5	EAI	Enable Attention Interrupts — When this bit is 0, attention conditions (e.g, on-line transitions) do not result in interrupts to the CPU. Rather, these conditions are not reported until the next command is issued; at this time, the command is rejected, and an ATTN message is returned. With this bit set, attention conditions cause an ATTN message to be generated (and an interrupt, if the IE bit was set on the last command) as soon as the controller owns the message buffer.
4	ERI	Enable Message Buffer Release Interrupts — If clear, interrupts are not generated upon completion of a Message Buffer Release command. Upon recognition of the command, only SSR is reasserted. If ERI is set, an interrupt is generated (without a message packet).
3-0	-	Not used and should be set to 0.

Table 4-19. Extended Characteristics Data Word Bit Defintions

Bit	Name	Description
15-12	XGRL	Extended Interrecord Gap (XIRG) Retry Limit — The value in this field, taken as a four-bit unsigned integer, specifies the number of times the VME-TC50 attempts to write a buffered record before aborting buffered write operation. A retry with XIRG consists of a backspace over the faulty record, a fixed length erase, and a write of the buffered record. An XIRG retry is attempted once after the non-XIRG retry limit is reached; then, if still not successful, another series of non-XIRG retries is attempted. The total number of retries allowed on any record is therefore the non-XIRG limit times the XIRG limit. This field has meaning only if write buffering is enabled and Retry Algorithm Control (RTY) is set.
11-8	NXGRL	Nonextended Interrecord Gap Retry Limit — The value in this field, taken as a four-bit unsigned integer, specifies the number of times the VME-TC50 attempts to write a buffered record without generating an extended IRG before attempting a retry with an extended IRG. A retry without an XIRG consists of a backspace over the faulty record and a write of the buffered record; no erase is performed. This field has meaning only if write buffering is enabled and RTY is set.
7	RTY	Retry Algorithm Control — When this bit is 0 and the controller is write buffering, the default retry algorithm (backspace and write with extended IRG up to ten times) is used when a record cannot be successfully written onto tape. When this bit is set, the retry limits specified in Bits 15-8 are used.
5	HSP	High-Speed Select — When this bit is clear, a dual-speed transport is commanded to operate at low speed. When set, a dual-speed transport is commanded to operate at high speed.
4-3	BUF CTL	Buffering Mode Control — This two-bit field controls the read and write buffering capabilities of the controller. The codes are defined as follows: Bit 4 Bit 3 Function 0 0 Buffering is disabled 1 0 Enable read buffering only 0 1 Enable write buffering only 1 1 Enable both read and write buffering
2-0	USEL	Unit Select — This field selects a transport for subsequent tape operations. Initialize always sets the unit select to 0.

The characteristic data buffer must begin on an even address. If Bit 0 of the second packet word, or

Bits 15-8 of the third packet word are nonzero, the function is not executed, but is terminated with a Function Reject. In this case, no message packet is stored, but an interrupt is generated if the IE bit is set. The fifth characteristics data word can optionally be specified to invoke special functions. In addition, a message buffer extent of 16 bytes can be specified so that extended status register 4 (XST4) can be output.

The fifth characteristic data word is used to specify parameters for the record buffering mode of operation and is also used to select a tape unit in a multidrive system.

The Write Characteristics command clears the NBA bit in the TSSR register, indicating that a valid message buffer has been specified, if all the following conditions are met:

- The command was not rejected because of nonzero bits in reserved or unused fields within the first three command packet words.
- The fourth packet word (byte count) contains at least a count of six to allow the first three characteristic data words to be fetched.
- The first two data words specify a valid even address (word boundary).
- The third data word contains a value of 14 or greater (specifying the length of the message buffer).

If any of the above conditions are not met, then the NBA bit is set (even if it was already clear from a previous valid Write Characteristics command) and no further message packets are deposited.

Note that if the byte count word in the command packet is less than seven, the characteristic mode data word is not fetched, causing the current values of the characteristic mode bits stored in the controller to be retained. Similarly, if the byte count is less than 10, the additional extended features control word is not fetched and the default values are used. The default values are no buffering, low speed, and transport 0.

4.4.5 Write Command

Figure 4-18 illustrates the command packet for a Write. There are two normal modes of operation: Write Data and Write Data Retry.

The allowable mode field codes and their functions are shown in Table 4-20.

Table 4-20. Valid Mode Field Codes

Mode	Function
0000	Write Data
0010	Write Data Retry (Space Reverse, Erase, Write Data)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	0	0	m	m	m	IE	0	0	0	0	1	0	1
Low-Order Data Buffer Address															
A15															A0
High-Order Data Buffer Address															
0	0	0	0	0	0	0	0	A23							A16
Buffer Extent (byte count) (16-bit unsigned value)															

Figure 4-18. Write Command Packet

The command packet for a Write contains four words: a header word, two words specifying the address of the buffer in memory where the data to be written onto tape is stored, and a buffer extent (byte count) word specifying the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of 0 specifies that 65,536 (64K) bytes are to be written.

If any of Bits 15-8 in the third word (high-order data buffer address) are nonzero, the command is aborted with Function Reject termination and ILA error status.

If a Write command is executed at or beyond the EOT marker, the data is written, but a Tape Status Alert (TSA) termination occurs. EOT remains set until passed in the reverse direction.

If a Write Retry command is issued while the tape is positioned at BOT, a Function Reject termination occurs with the NEF bit set in XST0.

During writes, the controller generates a parity bit for each data byte sent to the transport; the transport then writes this bit along with the data byte onto tape. During the write, the transport also reads the written bytes from tape and checks the parity. Two types of data errors can arise during a write: a correctable error or an uncorrectable error. In either case, the CPU should immediately issue a Write Retry command to rewrite the data correctly.

4.4.6 Position Command

Figure 4-19 illustrates the Position command packet. This command causes the tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to BOT. The tape mark/record count is the second word of the command packet. This word is ignored for a Rewind command.

The allowable mode field codes and their functions are described in Table 4-21.

Table 4-21. Functions of the Mode Field Codes (Position Command)

Mode	Function
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Record Count Ignored)

1514	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	0	0	m	m	m	IE	0	0	0	1	0	0	0
Tape Mark/Record Count (16-bit unsigned value)															

Figure 4-19. Position Command Packet

The Space Records operation skips over the number of records specified in the record count word of the command packet. However, the operation automatically terminates, with a TSA termination code, when a tape mark is traversed. (The tape mark is included in the record count.) Also, the RLS status bit in XST0 is set if the record count is not decremented to zero.

A Skip Tape Marks command skips over the number of tape marks specified in the tape mark count word of the command packet. However, the operation automatically terminates if a double tape mark (two contiguous tape marks) is encountered and the ESS bit was set in the previous Write Characteristics command. Termination also occurs if a tape mark is the first record off of BOT and the ESS and ENB bits were both set in the previous Write Characteristics command. RLS is set if the tape mark count is not decremented to zero.

A Space Records Reverse or Skip Tape Marks Reverse, which runs into BOT, sets the Reverse into BOT (RIB) status bit and causes a TSA termination. If one of these reverse commands is issued while the tape is already positioned at BOT, the NEF error bit is set and Function Reject termination returned; in this case, the tape does not move.

When a Rewind command is issued, the interrupt (if enabled) does not occur until the tape reaches BOT and has stopped.

4.4.7 Format Command

Figure 4-20 illustrates the Format command packet. Note that the second word is present, but it is not used in the command. This command can write a tape mark, rewrite a tape mark, or erase tape.

The allowable mode field codes and their functions are described in Table 4-22.

15	14	13	2	11	10	9	8	7	6	5	4	3	2	1	0
Cll	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	0	0	m	m	m	IE	0	0	0	1	0	0	1
(Not Used)															

Figure 4-20. Format Command Packet

Table 4-22. Functions of the Mode Field Codes (Format Command)

Mode	Function
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)

In all cases, executing a Format command at or beyond EOT causes a TSA termination. The EOT bit remains set until the EOT marker is passed in the reverse direction.

The Write Tape Mark command causes a transport dependent fixed length of tape to be erased and a file mark to be written. The Erase command merely causes a fixed length of tape to be erased. Successive Erase commands should be used to erase more than the transport dependent fixed length of tape.

The Write Tape Mark Retry command causes a Space Reverse (over the previous record), followed by a Fixed Length Erase, followed by a Write Tape Mark (which erases more tape before writing the file mark). If the tape is positioned at BOT when the Write Tape Mark Retry command is issued, the operation is aborted with Function Reject termination and the NEF error bit is set.

4.4.8 Control Command

Figure 4-21 illustrates the Control command packet. There are three modes: Message Buffer Release, Rewind and Unload, and NO-OP. The Control command is characterized by the fact that termination (and an interrupt if IE is set) occurs immediately at the start of the command.

The allowable mode field codes and their functions are provided in Table 4-23.

Table 4-23. Valid Mode Field Codes (Control Command)

Mode	Function
0000	Message Buffer Release
0001	Rewind and Unload
0010	NO-OP (Clean Tape)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	0	0	m	m	m	IE	0	0	0	1	0	1	0
(Not Used)															

Figure 4-21. Control Command Packet

The Message Buffer Release command, when executed with the ACK bit set, allows the controller to own the message buffer so it can update the status in the message buffer in case of an ATTN.

The Rewind and Unload command rewinds the tape completely onto the supply reel and places the transport in the off-line state. When this command is executed, termination (and an interrupt if IE is set) occurs immediately.

When the NO-OP command is issued, normal termination occurs immediately and no tape motion results.

4.4.9 Initialize Command

Figure 4-22 illustrates the Initialize command packet. This command performs the same as a write into the TXCPR register with Data Bit 15 set to 1. Note that IFEN to the tape transport is pulsed to stop runaway commands.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode				Format 1			Command				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	0	1	1
(Not Used)															

Figure 4-22. Initialize Command Packet

4.5 Record Buffering

The Record Buffering mode of operation can be invoked to optimize system performance when performing read and/or write operations to a streaming tape transport. The technique causes tape records to be buffered in the controller in order to speed tape throughput, by avoiding tape repositioning delays. The effect of buffering is to lengthen the apparent re-instruct period (as seen from the CPU) since tape data transfers can be overlapped with the CPU operations required to prepare for issuing the next command to the tape subsystem.

Read buffering causes an additional record to be read from the tape in response to a program requesting one. Typically, a program requests several records in succession, so a record stored in the controller is available for immediate transfer to the CPU. Only the Read Next (e.g, a forward read) causes the buffering algorithm to be invoked.

Write buffering allows one record to be accumulated in the controller and subsequently written to tape, allowing transfer of data from CPU memory to controller to be overlapped with tape repositioning. This also allows the CPU to prepare and issue the next Write command while the previous record is being physically written to tape. Therefore, there can be two records ready for consecutive transfers: one in the controller, and one in main memory.

Record Buffering is enabled by issuing the Write Characteristics command with the fifth characteristics data word properly configured.

SECTION 5: RTC SOFTWARE INTERFACE

The Clock register which is used for RTC programming is located at VME-TC50 base address+4. The structure of this one-word register is shown in Figure 5-1. The clock functions supported are

- Read clock register from buffer
- Write clock register to buffer
- Update clock buffer from clock hardware
- Update clock hardware from clock buffer

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC	CLK	HW	RW	CREG				Value							

Figure 5-1. Clock Register Format

For clock operations both MC and CLK are set. Programming is accomplished by commands to read and write elements of a clock buffer along with commands to update the buffer and clock hardware. The clock hardware is implemented with an MM58274 clock chip and the software interface buffer is an array of bytes organized as follows:

Byte 0 Ten thousandths of seconds (2 BCD digits)

Byte 1 Hundredths and tenths of seconds (2 BCD digits)

Byte 2 Seconds (2 BCD digits)

Byte 3 Minutes (2 BCD digits)

Byte 4 Hours (2 BCD digits)

Byte 5 Day of week (1 BCD digits)

Byte 6 Day of month (2 BCD digits)

Byte 7 Month (2 BCD digits)

Byte 8 Year (2 BCD digits)

Byte 9 Leap year (lower nibble matches the MM58274 leap year register format)

In order to read the clock buffer the HW and RW bits must be clear. The index of the quantity desired should be written to the CREG field of the Clock register. For example, if you want to read *hours*, you should write a value of four to the CREG. When the MC bit is clear, indicating the completion of the operation, the value in the lower byte of the Clock register is the value at the given index of the clock buffer.

NOTE

Ten thousandths and hundredths of seconds always read as 0.

In order to write the clock buffer, the HW bit must be clear and the RW bit set. The index and value of the time unit which is to be modified should be in the CREG and the lower byte of the Clock register. For example, in order to write 41 minutes, the CREG should be 0011 (minutes byte) and the value should be 01000001 (41).

To program the hardware clock or update the clock buffer with the current time, the HW bit should be set. With HW set, RW set to 1 programs the clock hardware with the values in the clock buffer; RW as 0 updates the clock buffer from the hardware.

The lower nibble of Byte 9 (leap year) matches the MM58274 leap year register format (see Table 5-1). The leap year counter (Bits 2 and 3) should be loaded with the number of years since the last leap year. For example, if 1980 were the last leap year, a clock programmed in 1982 should have a value of two stored in the leap year counter.

Bit 1 of Byte 9 sets the time as AM or PM when 12-hour mode is used. Bit 1 should be 0 if 24-hour mode is used.

Table 5-1. Leap Year Byte Format

	Byte 9 (lower nibble)				
Function	Bit 3	Bit 2	Bit 1	Bit 0	Comments
Leap year counter	X	X			A value of 0 = a leap year
AM/PM (12-hour mode)			X		0=AM 1=PM
12/24-hour select bit				X	0=12-hour mode 1=24-hour mode