JE610 KEYBOARD KIT

JE610 ASCII KEYBOARD ENCODER

DESCRIPTION: THE JE610 ASCII ENCODED KEYBOARD KIT CAN BE INTERFACED INTO MOST ANY COMPUTER SYSTEM. THE KEYBOARD ASSEMBLY REQUIRES +5V @ 150MA AND –12V @ 10MA FOR OPERATION. INTERFACE WIRING CAN BE MADE WITH EITHER A 16 PIN DIP JUMPER PLUG OR AN 18 PIN (.156 SPACING) EDGE CONNECTOR.

FEATURES:

- 60 KEYS GENERATE THE FULL 128 CHARACTERS, UPPER AND LOWER CASE ASCII SET
- 2 USER DEFINE KEYS PROVIDED FOR CUSTOM APPLICATIONS
- OUTPUTS DIRECTLY COMPATIBLE WITH TTL/DTL OR MOS LOGIC ARRAYS
- UTILIZES A 2376 (40 PIN) ENCODER MEMORY CHIP
- FULLY BUFFERED
- CAPS LOCK FOR UPPER CASE ONLY ALPHA CHARACTERS

PARTS LIST:

REF	DESCRIPTION	QTY
IC1	556 DUAL TIMER	1
IC2	74LS02 QUAD GATE	1
IC3	74LS00 QUAD GATE	1
IC4	7425 DUAL GATE	1
IC5	AY-5-2376 ENCODER OR EQ	1
IC6,7	74LS05 HEX BUFFER	2
C1	CAPACITOR, ELEC, 1MF, 25V	1
C2,5,7,8, 10,11,13-16	CAPACITOR, DISC, .1MF, 50V	10
C3,4,6	CAPACITOR, DISC, .01MF, 50V	3
C9	CAPACITOR, DISC, 100PF, 50V or EQ	1
C12	CAPACITOR, ELEC, 47MF, 16V	1
CR1,2	DIODE IN4148 OR EQ	2

REF	DESCRIPTION	QTY
KB1	KEYBOARD, 62 KEYS, HI-TEK	1
R1-3	RESISTOR, 560 OHMS, 1/4W	3
R4,6,13-23	RESISTOR, 2.2K, 1/4W	13
R5	RESISTOR, 150K, 1/4W	1
R7,8,11	RESISTOR, 27K, 1/4W	3
R9	RESISTOR, 100K, 1/4W	1
R10	RESISTOR, 270K, 1/4W	1
R12	RESISTOR, 10K, 1/4W	1
J1	CONNECTOR, 16 PIN, ST STD	1
JW1	CONDUCTOR, INSULATED 26AWG	5"
	SOCKET, 14 PIN, ST STD OR EQ	6
	SOCKET, 40 PIN, ST STD OR EQ	1
	PRINTED WIRING BOARD JE610	1
	JE610 KIT INSTRUCTIONS	2 SHTS

ASSEMBLY PREPARATION AND PROCEDURES:

1. IMPORTANT: IDENTIFY ALL PARTS ON PARTS LIST BEFORE PROCEEDING.

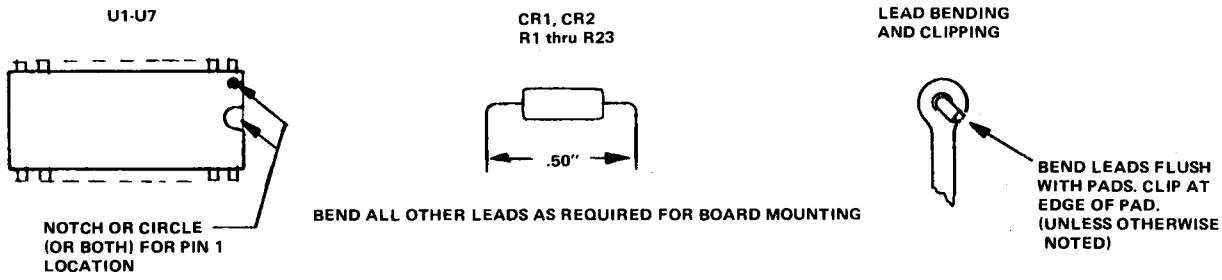
2. SUGGESTION: SIMULATE PRINTED WIRING BOARD ASSEMBLY BY PLACING THE COMPONENTS IN THEIR ACTUAL PLACE ON THE PICTURE ASSEMBLY. TRANSFER COMPONENTS TO THE BOARD DURING ASSEMBLY.

3. TOOLS REQUIRED:
   - SMALL SOLDERING IRON OR GUN (27W TO 35W).
   - RESIN CORE SOLDER .03 DIA. (DO NOT USE ACID CORE TYPE).
   - SMALL LONG NOSE PLIER.
   - SMALL WIRE CUTTER.
   - SMALL SPONGE FOR CLEANING SOLDER TIP.

4. SOLDERING TIPS:
   - FEED SOLDER TO THE CRACK BETWEEN THE PAD AND THE IRON TIP.
   - LEAVING THE IRON TIP TOO LONG ON A PAD WILL LIFT THE PAD. ALLOW APPROXIMATELY 2 SECONDS PER SOLDER JOINT.
   - USING TOO MUCH SOLDER WILL CAUSE THE SOLDER TO BRIDGE ACROSS TRACES.
   - KEEP IRON TIP CLEAN BY WIPING THE TIP ACROSS A WATER-DAMPENED SPONGE.

ASSEMBLY PREPARATION AND PROCEDURES: (CONT'D)

5. COMPONENT WIRE IDENTIFICATION, LEAD BENDING AND CLIPPING:



ASSEMBLY INSTRUCTIONS:

1. PRINTED WIRING BOARD ASSEMBLY: SEE ASSEMBLY PICTURE. (PAGE 5).

   1.1 START BOARD ASSEMBLY BY PLACING THE BOARD IN THE POSITION SHOWN ON THE ASSEMBLY PICTURE. THE EDGE CONNECTOR (P1) WILL BE AT THE UPPER LEFT CORNER.

   1.2 INSERT RESISTORS R1 THRU R23 AS SHOWN. TAKE CARE THAT THE COLORS ARE CORRECT. BEND AND CLIP LEADS. DO NOT SOLDER.

   1.3 INSERT DIODES CR1 AND CR2. NOTE POLARITY BAND POSITION. BEND AND CLIP LEADS. DO NOT SOLDER.

   1.4 INSERT CAPACITORS C1 THRU C16. BE SURE THAT THE CAPACITANCE VALUES ARE CORRECT FOR EACH CAPACITOR LOCATION. NOTE LOCATION OF (+) LEAD FOR C1 AND C12 . BEND AND CLIP LEADS. DO NOT SOLDER.

   1.5 INSERT J1 CONNECTOR (16 PIN SOCKET), IC1,2,3,4,6 AND 7 SOCKETS (14 PIN) AND IC5 SOCKET (40 PIN) FLUSH ON BOARD. NOTE ANGLE (OR MARKINGS) ON THE UPPER RIGHT CORNER OF THE SOCKET TO IDENTIFY PIN 1 (ALL 8 SOCKETS) LOCATION. PIN 1 IS ALSO DESIGNATED BY A SQUARE PAD ON THE BOARD. TO PREVENT THE SOCKETS FROM FALLING OFF, BEND 2 LEADS AT OPPOSITE CORNERS ON EACH SOCKET. DO NOT BEND OTHER LEADS. DO NOT SOLDER.

   1.6 INSERT KEYBOARD (KB1) FLUSH ON BOARD. BE SURE THAT ALL THE PINS ARE STRAIGHT BEFORE INSTALLING. THERE ARE 3 LOCATING PINS ON THE BOTTOM OF THE KEYBOARD TO HELP ALIGN THE PINS THRU THE BOARD. ANY UNNECESSARY FORCING MEANS PIN MISALIGNMENT. PINS WILL BREAK WHEN BENT MORE THAN A COUPLE OF TIMES. MAKE SURE EACH KEY SWITCH HAS 2 PINS THRU THE BOARD. EACH OF THE KEY PADS CAN BE REMOVED BY PULLING IT STRAIGHT UP FROM THE SQUARE SHAFT. DO NOT BEND LEADS. DO NOT SOLDER.

   1.7 DOUBLE CHECK FOR CORRECT COMPONENT INSERTION BY PLACING A CHECK MARK (✓) IN EACH OF THE CIRCLES PROVIDED ON THE ASSEMBLY DRAWING.

   1.8 TURN COMPONENT BOARD ASSEMBLY OVER BY RESTING IT ON THE KEYBOARD, AND SOLDER ALL COMPONENT LEADS. APPLY AS LITTLE HEAT AS POSSIBLE, FOR A GOOD SOLDER JOINT, TO CR1 AND CR2 AS THEY ARE MORE HEAT SENSITIVE THAN THE OTHER COMPONENTS. CHECK CAREFULLY FOR SOLDER BRIDGES ACROSS PADS AND TRACES. REMOVE ALL SOLDER BRIDGES IF ANY.

   1.9 INSTALL JUMPER WIRE (JW1) TO SOCKET LEADS BETWEEN IC4 PIN 6 AND IC5 PIN 6 (NON-COMPONENT SIDE). CHECK CAREFULLY FOR SOLDER BRIDGES AROUND LEADS. PLACE (✓) IN CIRCLE.

2. BOARD VOLTAGE CHECK: (NO IC'S IN SOCKETS)

   2.1 ATTACH GROUND TO J1-8 DIP SOCKET OR P1-18 EDGE CONNECTOR.
   ATTACH +5VDC TO J1-16 DIP SOCKET OR P1-1 EDGE CONNECTOR.
   ATTACH −12VDC TO J1-9 DIP SOCKET OR P1-16 EDGE CONNECTOR.

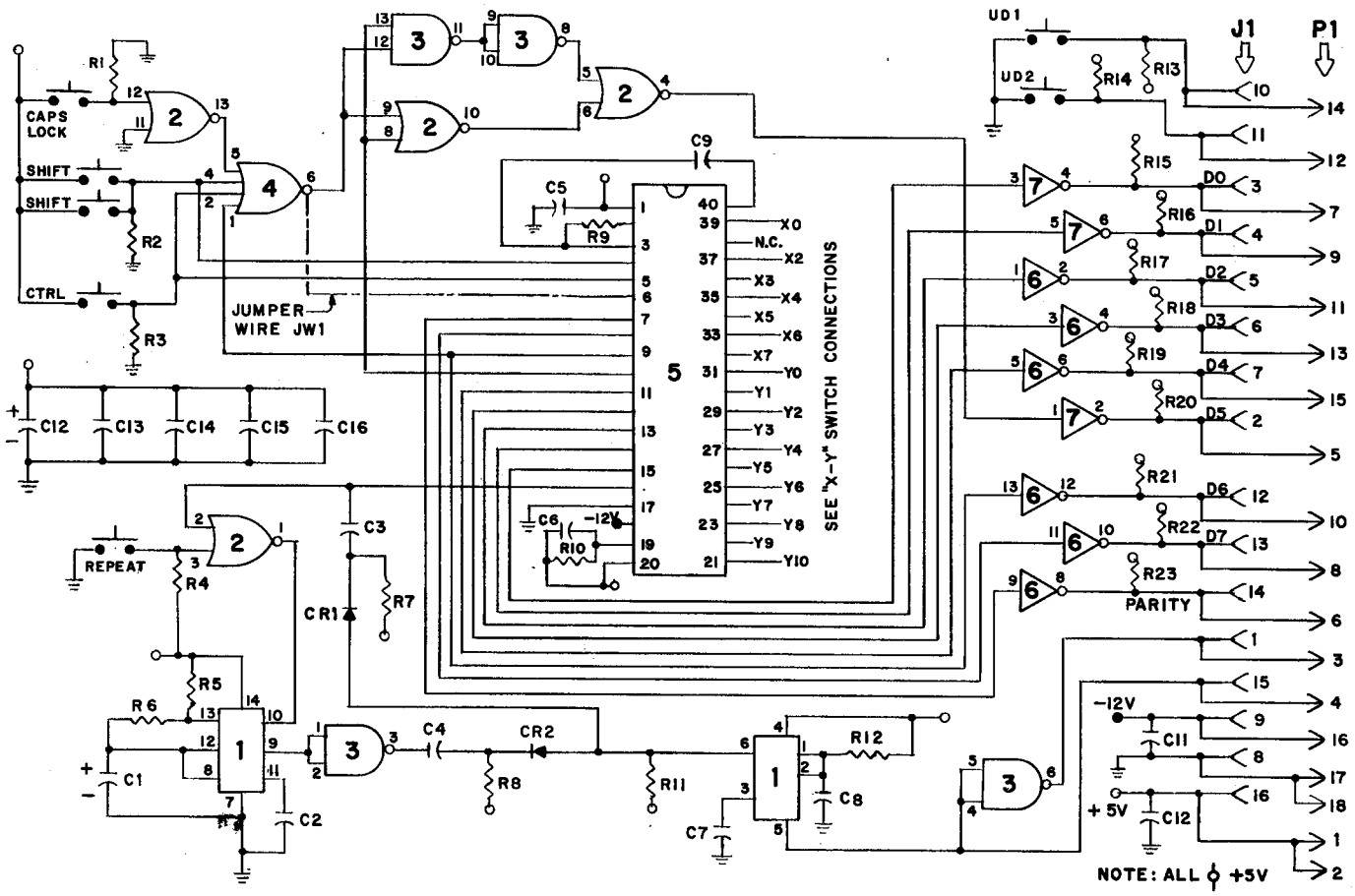
   2.2 CHECK FOR +5V *BETWEEN GROUND* AND IC SOCKET #1 PIN 14, IC SOCKET #5 PIN 1, AND IC SOCKET #7 PIN 14. ALSO CHECK FOR −12 V BETWEEN GROUND AND IC SOCKET #5 PIN 18.

   2.3 IF THERE IS NO VOLTAGE ON THE PIN(S) CHECK FOR IMPROPER HOOK-UP AT THE CONNECTORS.
   IF THE +5V APPEARS ONLY AT CERTAIN PINS, CHECK FOR UNSOLDERED PADS OR COLD SOLDER JOINTS. ALSO CHECK FOR SOLDER BRIDGED TRACES AND PADS. WHEN BOTH VOLTAGES ARE PROPERLY CHECKED, DISCONNECT POWER SUPPLIES.

3. I.C. ASSEMBLY

   3.1 INSERT IC'S 1 THRU 7 INTO THEIR RESPECTIVE SOCKETS. NOTE THAT THE NOTCH TO LOCATE PIN #1 ON ALL THE IC'S ARE ON THE RIGHT SIDE. TO PREVENT DAMAGES FROM STATIC ELECTRICAL DISCHARGE TO IC 5, DO NOT REMOVE THE BLACK CONDUCTIVE FOAM FROM THE IC LEADS UNTIL READY TO PUT INTO THE 40 PIN SOCKET. BE SURE THE PINS ON ALL THE IC'S ARE STRAIGHT BEFORE INSERTION. FIRST LINE UP ONE SIDE OF THE LEADS INTO THE SOCKET AND THEN CAREFULLY WORK THE LEADS FROM THE OPPOSITE SIDE INTO THE SOCKET BEFORE PUSHING IT IN. RECHECK FOR PROPER PLACEMENT OF EACH IC AS WELL AS THE PIN #1 LOCATION.
   PLACE A (✓) MARK IN THE CIRCLE.

JE610 SCHEMATIC DIAGRAM



KEYBOARD SWITCH PAD "X-Y" CONNECTIONS

KEY → X-Y →	ESC X5 Y10	! 1 X7 Y8	" 2 X7 Y7	# 3 X7 Y6	$ 4 X7 Y5	% 5 X7 Y4	& 6 X7 Y3	/ 7 X7 Y2	(8 X7 Y1	) 9 X7 YO	Ø X3 YO	= – X2 YO	: \ X7 Y10	~ ^ X7 Y9	BACK SPACE X3 Y5	BREAK XO YO
KEY → X-Y →	TAB X6 Y9	Q X6 Y8	W X6 Y7	E X6 Y6	R X6 Y5	T X6 Y4	Y X6 Y3	U X6 Y2	I X6 Y1	O X6 YO	P X3 Y2	{ [X3 Y6	\ @ X3 Y4	LINE FEED X3Y9	DELETE X3 Y10	
KEY → X-Y →	CTRL ---	CAPS LK ---	A X5 Y8	S X5 Y7	D X5 Y6	F X5 Y5	G X5 Y4	H X5 Y3	J X5 Y2	K X5 Y1	L X5 YO	+; X4 YO	*; X3 Y1	}] X3 Y7	RETURN X3 Y8	
KEY → X-Y →	UD1 ---	SHIFT ---	Z X4 Y10	X X4 Y9	C X4 Y8	V X4 Y7	B X4 Y6	N X4 Y5	M X4 Y4	< , X4 Y3	> . X4 Y2	? / X4 Y1	SHIFT ---	REPEAT ---	UD2 ---	SPACE BAR X2Y8

KEYBOARD OPERATION:

THE JE610 KEYBOARD CONNECTS TO THE COMPUTER BY MEANS OF AN 18 PIN EDGE CONNECTOR (.156 SPACING) TO "P1" OR A 16 PIN DIP JUMPER PLUG TO "J1" SOCKET. THE DATA IS PARALLEL CONSISTING OF 8 ASCII DATA BITS AND 1 EVEN PARITY BIT. ALSO PROVIDED ARE POSITIVE AND NEGATIVE-GOING STROBES TO SIGNAL THE PRESENCE OF DATA. WHEN A KEY IS PRESSED, THE NORMALLY RANDOM-MOVING BIT PATTERN AT THE OUTPUTS STABILIZES TO THE ASCII CHARACTER REPRESENTING THE DEPRESSED KEY AND PRODUCING THE STROBE'S OUTPUTS. THE OUTPUTS WILL THEN GO INTO THE COMPUTER. THE USER-DEFINED KEYS HAVE A HIGH LEVEL OUTPUT (PULLED UP TO +5VDC) WHEN THE KEYS ARE NOT PRESSED. THE OUTPUT(S) BECOME ZERO VOLTS WHEN THE KEYS ARE PRESSED.

ADAPTING TO NON-STANDARD DATA INPUT POLARITY:

THE KEYBOARD SENDS ITS DATA OUT USING POSITIVE LOGIC AS CORRESPONDING TO THE CODE ASSIGNMENT CHART ON PAGE 6 (EXCEPT WITH EVEN PARITY). THE ENCODER CHIP IS WIRED TO PRODUCE THE CORRECT LOGIC OUTPUT BUT MAY BE CHANGED, IF NECESSARY, BY REPLACING BOTH 74LS05 IC'S (IC6 AND IC7) WITH 7407 TYPES. THIS WOULD CAUSE THE **DATA** AND **PARITY** TO BE **INVERTED.** NOTE THAT THERE ARE TWO STROBE LINES, ONE FOR DEVICES REQUIRING A POSITIVE-GOING EDGE TO SIGNAL DATA AVAILABLE AND THE OTHER FOR DEVICES NEEDING NEGATIVE EDGE TRIGGERING.

CONNECTOR TERMINALS AND DATA BIT IDENTIFICATIONS

DATA BITS:

DATA BIT NO. (D)	8*	D7**	D6	D5	D4	D3	D2	D1	D0	*PARITY
J1 CONNECTOR PIN NO.	14	13	12	2	7	6	5	4	3	**Not used in some systems.
P1 CONNECTOR PIN NO.	6	8	10	5	15	13	11	9	7	
DATA BIT VALUE	—	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	

STROBES:

POSITIVE-GOING EDGE: J1 PIN 15, P1 PIN 4
NEGATIVE-GOING EDGE: J1 PIN 1, P1 PIN 3

POWER CONNECTIONS:

+5VDC @ 150MA: J1 PIN 16, P1 PINS 1 & 2
−12VDC @ 10 MA: J1 PIN 9, P1 PIN 16
GROUND: J1 PIN 8, P1 PIN 17 & 18

USER-DEFINED KEYS:

UD1: BOTTOM ROW LEFT CORNER KEY. J1 PIN 10, P1 PIN 14.
UD2: BOTTOM ROW RIGHT CORNER KEY. J1 PIN 11, P1 PIN 12.

KEYBOARD SWITCH AND CONNECTOR(S) PIN TEST

A VOLTMETER OR LOGIC PROBE WILL BE REQUIRED FOR THIS TEST. CONNECT BOTH POWER SUPPLIES (+5V, −12V AND GROUND) TO THEIR RESPECTIVE PINS ON J1 OR P1. TEST MEASUREMENTS WILL BE MADE BETWEEN GROUND AND THE DESIGNATED PIN NO.(S) OF J1 OR P1. PRESS THE FOLLOWING KEYS BY HOLDING EACH DOWN ONE AT A TIME. ANY OUTPUT BELOW 0.5V (APPROX.) TO COMMON, IS CONSIDERED LOW OR ZERO (0) OR OFF. ANY OUTPUT ABOVE 4.5V (APPROX.) TO COMMON IS CONSIDERED HIGH OR ONE (1) OR ON. THIS TEST SHOULD CHECK OUT THE PROPER FUNCTION OF THE KEYBOARD.

	J1-14 OR P1-6	J1-13 OR P1-8	J1-12 OR P1-10	J1-2 OR P1-5	J1-7 OR P1-15	J1-6 OR P1-13	J1-5 OR P1-11	J1-4 OR P1-9	J1-3 OR P1-7
KEY* (PRESS)	PARITY	D7** (B8)	D6 (B7)	D5 (B6)	D4 (B5)	D3 (B4)	D2 (B3)	D1 . (B2)	D0 (B1)
SPACE BAR	1	1	0	1	0	0	0	0	0
!	0	1	0	1	0	0	0	0	1
"	0	1	0	1	0	0	0	1	0
$	0	1	0	1	0	0	1	0	0
(	0	1	0	1	0	1	0	0	0
Ø	0	1	0	1	1	0	0	0	0
0 (upper)	1	0	1	0	0	1	1	1	1

** Not used in parity check

*CHECK HORIZONTAL COLUMN ACROSS CHART FOR EACH KEY PRESSED

TIPS FOR ISOLATING COMMON KEYBOARD PROBLEMS:

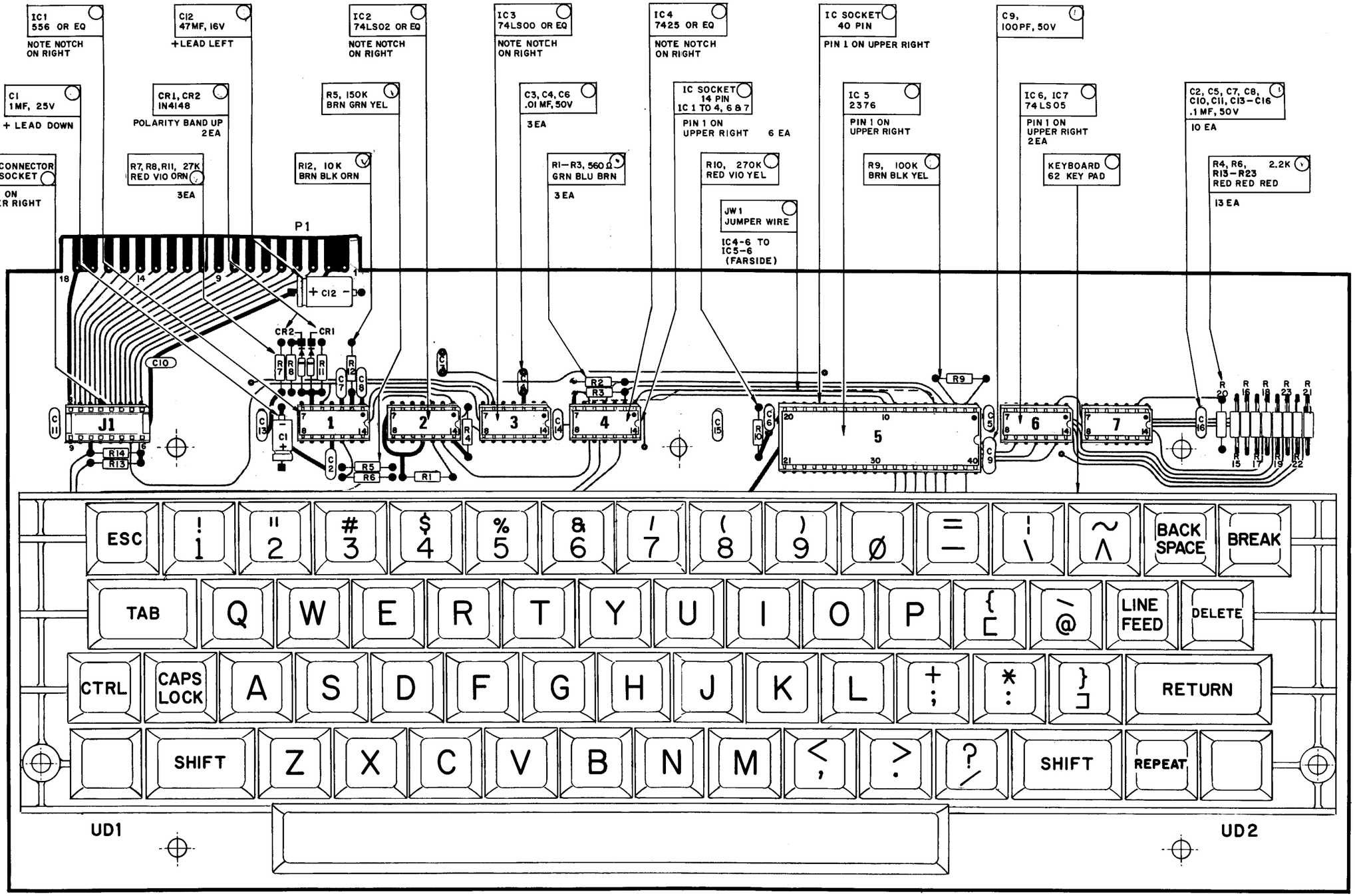
1. IMPROPER COMPONENT ASSEMBLY: RECHECK ALL COMPONENTS FOR PROPER INSERTION. CHECK ALL IC'S FOR PROPER PIN 1 LOCATION. CHECK FOR CORRECT POLARITY LEAD PLACEMENT OF CR1, CR2, C1 AND C12.
2. BECAUSE OF NON-CORRESPONDING PIN NUMBERS BETWEEN J1 AND P1 CHECK FOR CORRECT TERMINATIONS TO RESPECTIVE CONNECTORS.
3. RECHECK FOR PROPER POWER SUPPLY(S) HOOK-UP.
4. GENERAL AND INTERMITTENT PROBLEMS: IMPROPER COMPONENT VALUE PLACEMENT. COLD SOLDER JOINTS, UNSOLDER PADS AND SOLDER BRIDGES ACROSS TRACES AND PADS.
5. CAUTION: A COMMON MISTAKE IS TO INSERT CONNECTORS J1 OR P1 BACKWARDS. THIS COULD CAUSE IRREPARABLE DAMAGES.

IMPORTANT:
IF REPAIRS ARE REQUIRED, FORWARD KIT ALONG WITH EXPLANATION TO JAMECO ELECTRONICS REPAIR CENTER, 1021 HOWARD AVENUE, SAN CARLOS, CA 94070 – **THIS KIT WILL NOT BE REPAIRED BY JIM-PAK DEALERS.**

WARRANTY:
A $10.00 minimum service fee will be charged on each kit returned for repairs. We will replace, free of charge, all components which are defective due to manufacturer defects within 90 days from date of purchase. Customer will be subject to charges for misuse or damage to the printed wiring board or components during assembly.

Jameco ELECTRONICS

JE610 ASCII KEYBOARD — PRINTED WIRING BOARD ASSEMBLY



Keyboard Encoder

FEATURES

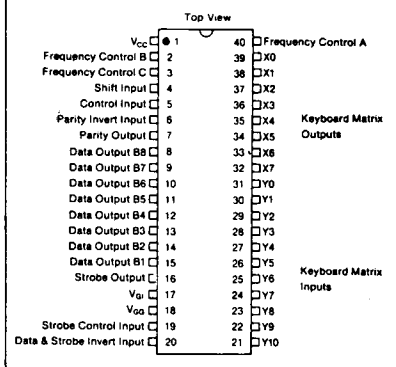
- One integrated circuit required for complete keyboard assembly.
- Outputs directly compatible with TTL/DTL or MOS logic arrays.
- External control provided for output polarity selection.
- External control provided for selection of odd or even parity.
- Two key roll-over operation.
- N-key lockout.
- Programmable coding with a single mask change.
- Self-contained oscillator circuit.
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Static charge protection on all input and output terminals.
- Entire circuit protected by a layer of glass passivation.

DESCRIPTION

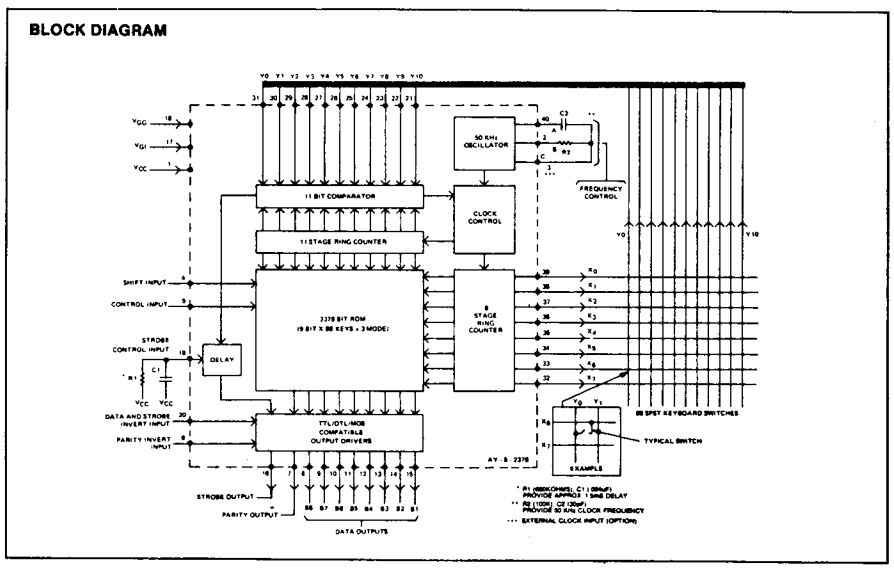
The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ± 0.5 Volts, V_{GG} = −12 Volts ± 1.0 Volts, V_{GI} = GND. | (V_{CC} = Substrate Voltage) Operating Temperature (T_A) = 0°C to +70°C

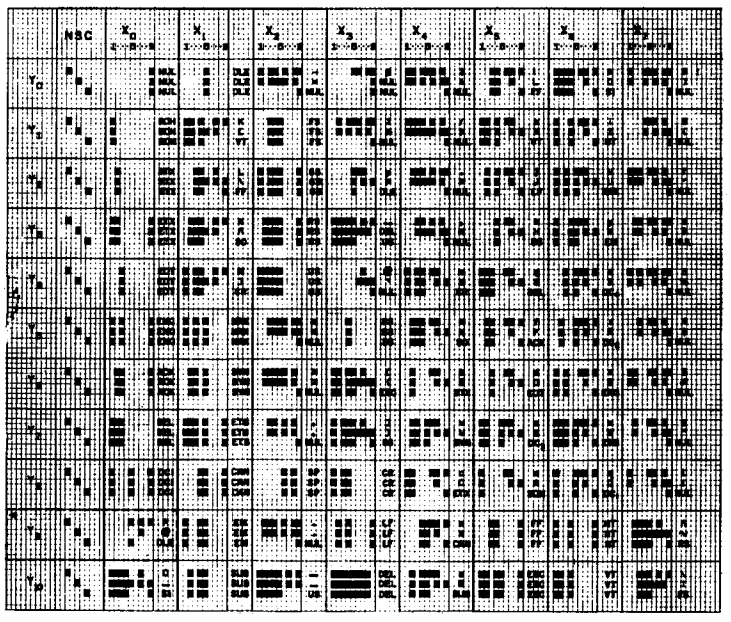
Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote** for typical R - C values
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
			—			
Shift & Control Input Current	$I_{INS,C}$	15	36	60	μA	V_I=+5V
		8	16	30	μA	V_I= 0V
Data, Parity Invert Input Current	$I_{IND,P}$	—	.01	1	μA	V_I=−5V to +5V
X Output (X_0-X_7)						
Logic "1" Output Current	I_{X1}	—	0	—	μA	V_{OUT} = V_{CC}
		80	150	400	μA	V_{OUT} = V_{CC} −1.3V
		140	300	800	μA	V_{OUT} = V_{CC} −2.0V
		250	700	1500	μA	V_{OUT} = V_{CC} −5V
		500	1500	3000	μA	V_{OUT} = V_{CC} − 10V
Logic "0" Output Current	I_{XO}	15	30	80	μA	V_{OUT} = V_{CC}
		13	27	65	μA	V_{OUT} = V_{CC} −1.3V
		12	25	60	μA	V_{OUT} = V_{CC} −2.0V
		5	10	40	μA	V_{OUT} = V_{CC} −5V
		—	1	20	μA	V_{OUT} = V_{CC} −10V
Y Input (Y_0-Y_{10})						
Trip Level	V_Y	V_{CC} −5	V_{CC} −3	V_{CC}−2	V	Y Input Going Positive
Hysteresis	ΔV_Y	.5	.9	1.4	V	Note 1
						Note 2
Selected Y Input Current	I_{YS}	30	60	160	μA	V_{IN} = V_{CC}
		26	54	130	μA	V_{IN} = V_{CC} −1.3V
		24	50	120	μA	V_{IN} = V_{CC} −2.0V
		10	20	80	μA	V_{IN} = V_{CC} −5V
		—	2	20	μA	V_{IN} = V_{CC} −10V
Unselected Y Input Current	I_{YU}	15	30	80	μA	V_{IN} = V_{CC}
		13	27	65	μA	V_{IN} = V_{CC} −1.3V
		12	25	60	μA	V_{IN} = V_{CC} −2.0V
		5	10	40	μA	V_{IN} = V_{CC} −10V
Input Capacitance	C_{IN}	—	3	10	pf	at 0V
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10⁷	—	—	Ω	
Strobe Delay						
Trip Level (Pin 19)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	.5	.9	1.4	V	See Note 1
Quiescent Voltage (Pin 19)		−3	−5	−8	V	With 680KΩ to V_{SS}
Data Output (B_1-B_8)						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6ma
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH}−100μa
Power						
I_{CC}	—	—	5	10	mA	V_{CC} = +5V
I_{GG}	—	—	5	10	mA	V_{GG} = −12V

**Typical values at +25°C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = **eleven.**

STANDARD CODE ASSIGNMENT CHART

8 Bit ASCII, odd parity



OPERATION

The AY-5-2376 contains (see Block Diagram), a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

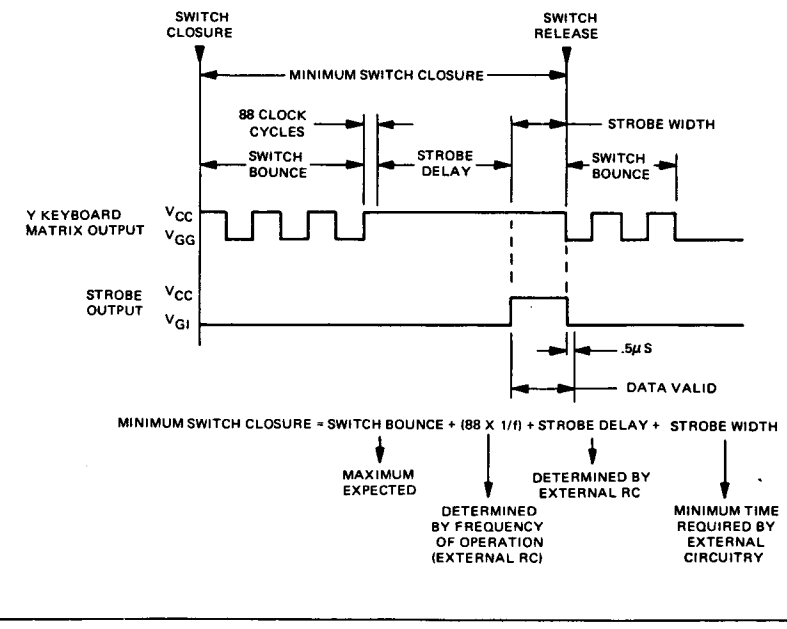
When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and to the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

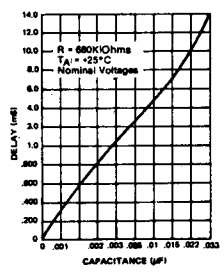
SPECIAL PATTERNS

Since the selected coding of each key is defined during the manufacture of the chip, the coding can be changed to fit any particular application of the keyboard. Up to 264 codes of up to 8 bits (plus one parity bit) can be programmed into the AY-5-2376 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code is available as a standard pattern.

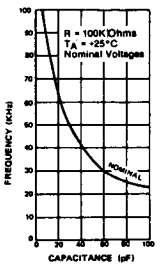
TIMING DIAGRAM



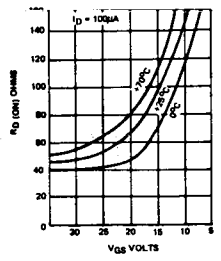
TYPICAL CHARACTERISTIC CURVES



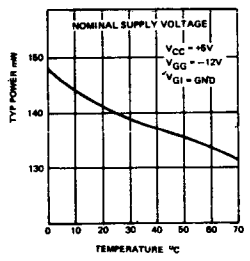
STROBE DELAY VS. C1



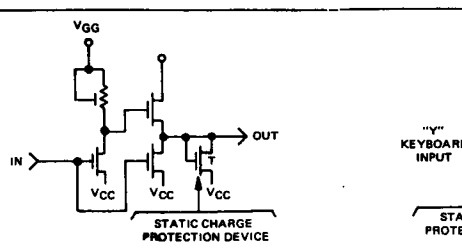
OSCILLATOR FREQUENCY VS. C2



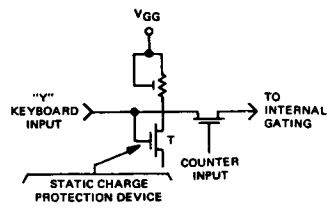
TYPICAL OUTPUT ON RESISTANCE (R_{DON}) VS. GATE BIAS VOLTAGE (V_{GS})



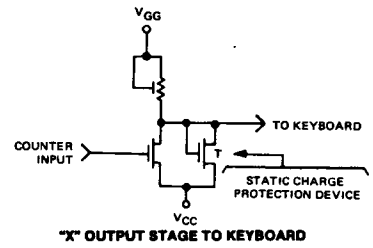
TYPICAL POWER CONSUMPTION (mW) VS. TEMP (C°)



OUTPUT DRIVER

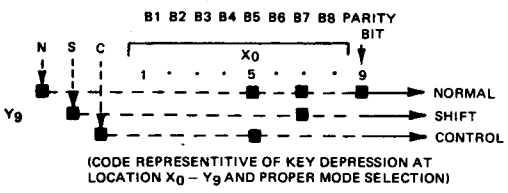


"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

*EXAMPLE



N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1". (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = GND

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

MODE SELECTION

S	C	= N
C	C	= S
S	S	= C
S	C	= C