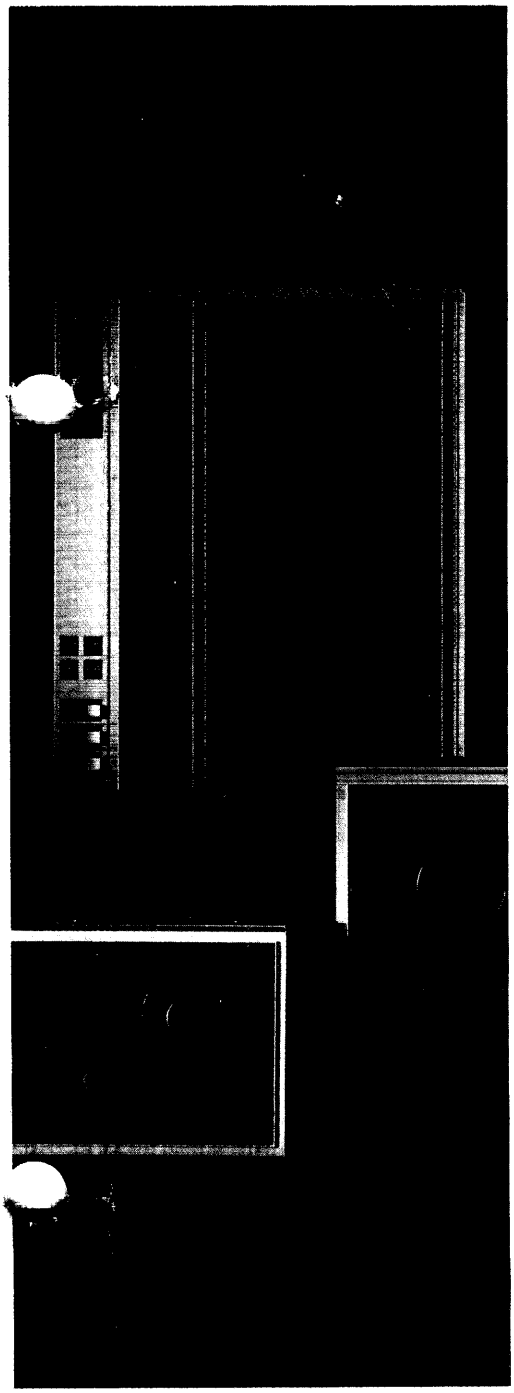
Operation and Maintenance Manual

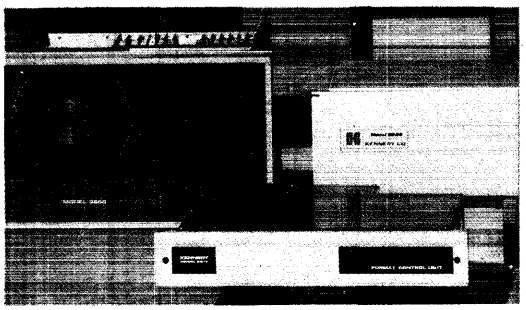
Model 9100

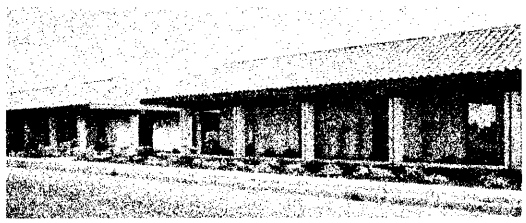
Digital Tape Transport

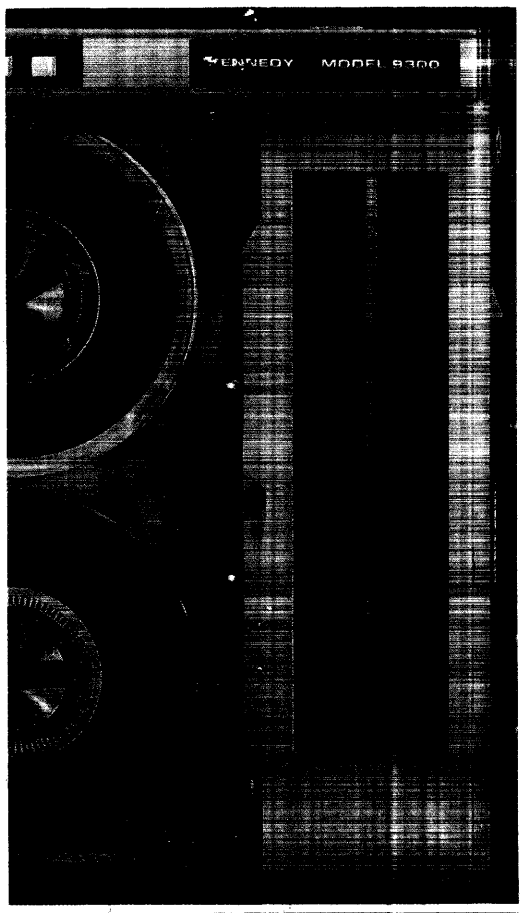
KENNEDY

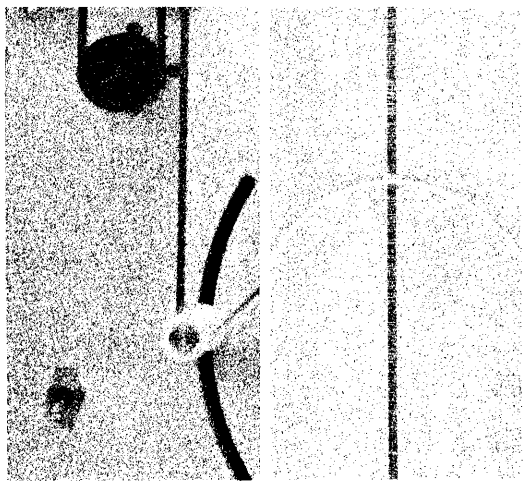
MODEL	PART NO.	INTERFACE
9100	192-9100-003	STD
SPEED	DENSITY	TRACKS
75 IPS	800/1600 CPI	9
MODIFICATIONS		

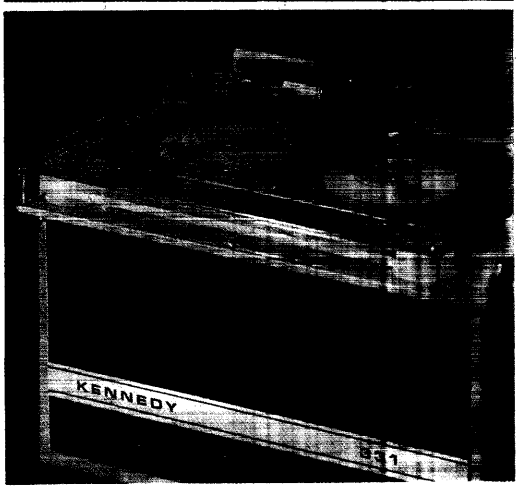












CONTENTS

SECTION V — PARTS IDENTIFICATION

SECTION VI — WIRING AND SCHEMATIC DIAGRAMS

SECTION VII — GENERAL INFORMATION AND APPENDIX

ILLUSTRATIONS

TABLES

FCC NONCERTIFIED EQUIPMENT

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

SECTION I
APPLICATION DATA

SECTION I

APPLICATION DATA

1.1 INTRODUCTION

The Kennedy Model 9100 is a synchronous digital magnetic tape unit that with proper external formatting control is capable of reading and writing IBM compatible tapes, and is used in applications requiring high reliability at moderate tape speeds. Typical applications include operation with mini computers as peripherals and high speed data collection systems.

The Model 9100 is equipped with the electronics necessary for reading and writing tapes and for controlling the tape motion. The head specifications and the mechanical and electrical tolerances of the Model 9100 meet the requirements for IBM compatibility. However, the formatting electronics, parity generator, cyclic redundancy check character (CRCC) generator, gap control, etc., are not included and must be provided by the tape control and formatter in order to generate properly formatted IBM compatible tapes.

The standard Model 9100 is available in 7 or 9 track NRZI recording configurations, as well as the 9 track phase encoded configuration. Standard data recording densities are: 200/556 cpi or 556/800 cpi 7 track NRZI, 800 cpi 9 track NRZI, 1600 cpi 9 track phase encoded, 800/1600 cpi 9 track NRZI/ phase encoded, or 800/1600 cpi NRZI. A tape unit select switch is standard on 7 and 9 track models. A dual density switch is standard on 9 track dual density units.

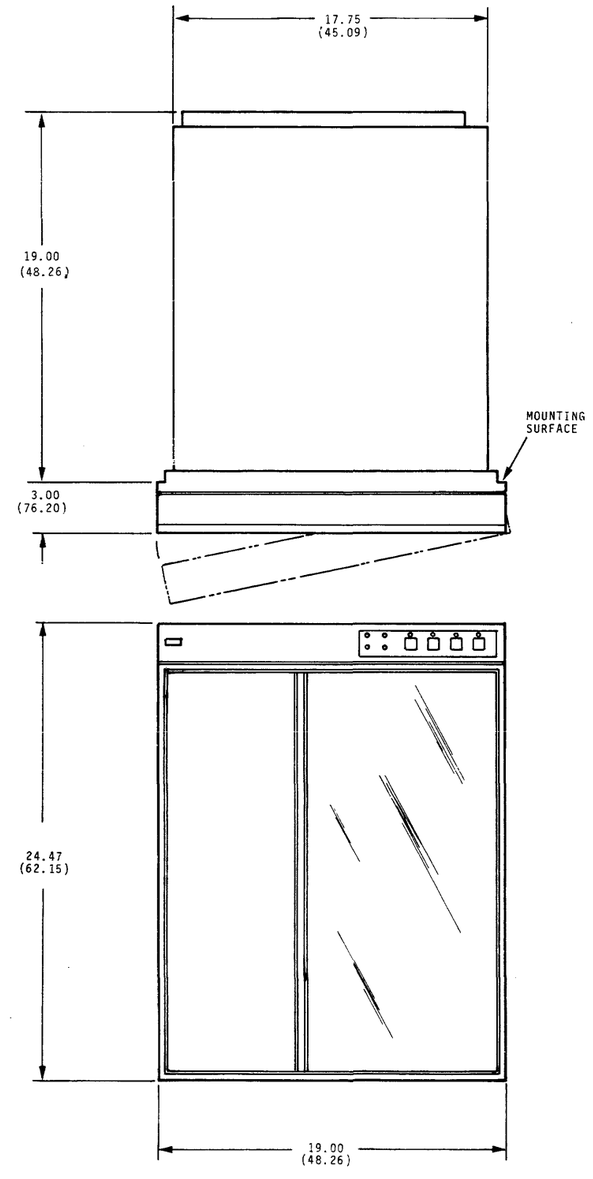
The standard tape speed is 75 ips; however, tape speeds from 25-75 ips are available. The data transfer rate at 75 ips, 800 cpi is 60 kHz, or 120 kHz at 75 ips, 1600 cpi. Other options include power supply modification to accommodate foreign or dc line voltages, auto power restart, etc.

1.2 ELECTRICAL AND MECHANICAL SPECIFICATIONS

Tape (computer grade)	
Width	0.5 inch (1.27 cm)
Thickness	1.5 mil (0.038 mm)
Tension	8.0 ounces (227 gm)
Reel diameter	to 10.5 inches (26.6 cm)
Capacity	2400 feet (731.5 meters)
Reel hub	3.69 inches (9.37 cm) dia per IBM standards
Reel braking	Dynamic
Recording mode (IBM compatible)	NRZ1/PE
Tape drive	Single capstan
Tape speed	45-75 ips (114-190 cm/sec)
Instantaneous speed variation	±1%
Long term speed variation	±1%
Start/stop displacement	0.19 inch (0.476 cm)
Start/stop time @ 75 ips	5.0 ms
Rewind speed	200 ips (508 cm) nominal
Magnetic head assembly	
(Write to read gap displacement)	
Dual gap 7 track read after write	0.30 inch (0.76 cm)
Dual gap 9 track read after write	0.15 inch (0.38 cm)
Interchannel displacement error ... (measured with IBM master skew tape PN 432362)	
Write (maximum)	100 μinches (2.5 μm)
Read (maximum)	100 μinches (2.5 μm)
Erase head	Full width
Load point and end of tape reflective strip detection (IBM compatible)	Infrared
Broken tape detection	Infrared
Dimensions (see Figure 1-1)	
Transport mounting (horizontal)	Standard 19-inch (48.26 cm) RETMA rack
Height	24.47 inches (62.15 cm)
Width	19.00 inches (48.26 cm)
Depth (from mounting surface)	19.0 inches (48.26 cm)
Depth (overall)	21.62 inches (54.91 cm)
Weight	150 pounds (67.95 kgm)
Shipping weight	200 pounds (75.43 kgm)
Operating environment	
Ambient temperature	+2° to +50°C
Relative humidity (noncondensing)	15% to 95%
Power requirements	115 vac, 60 Hz 220/240 vac, 50 Hz single phase
Volt amps nominal	400
Volt amps maximum	800

Table 1-1. Electrical and Mechanical Specifications

410-4018



DUST COVER OPENS TO APPROX 120 DEGREES
FOR ACCESS TO TAPE REELS

DECK ASSEMBLY EXTENDS ON SLIDES
FOR ACCESS TO TRANSPORT & ELECTRONICS

FIRST DIMENSIONS ARE SHOWN IN INCHES
DIMENSIONS IN PARENTHESES ARE IN CENTIMETERS

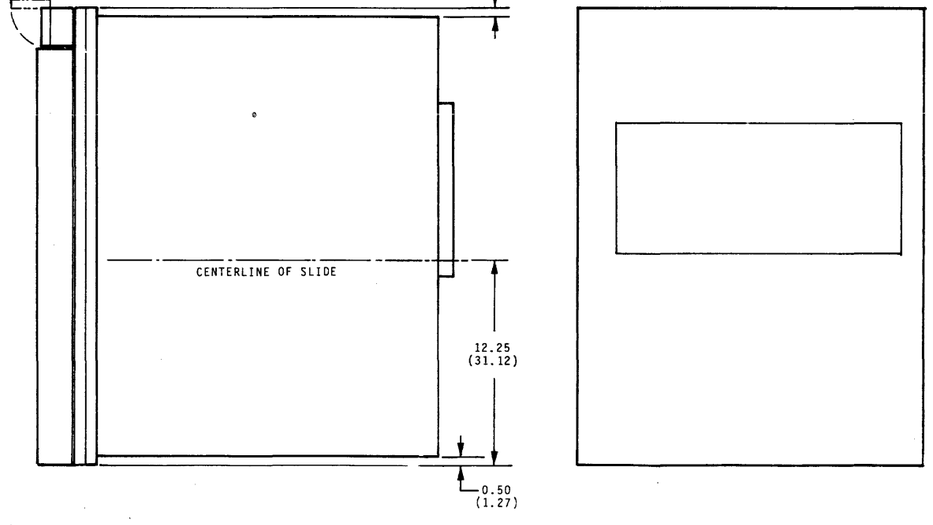
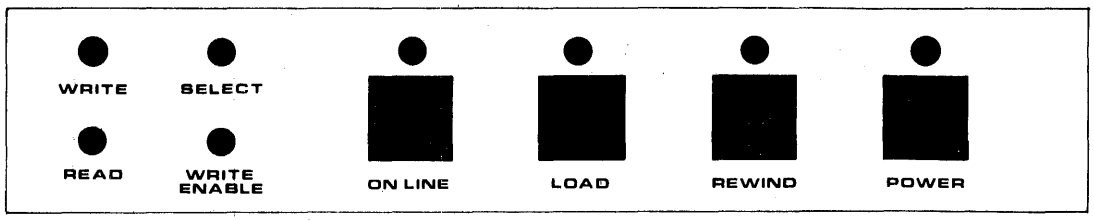


Figure 1-1.
Model 9100 Outline and Installation Drawing

1.3 CONTROLS AND INDICATORS



WRITE INDICATOR. Illuminated when write status is selected.

READ INDICATOR. Illuminated when read status is selected.

SELECT INDICATOR. Illuminated when tape unit is on line and selected.

WRITE ENABLE INDICATOR. Illuminated whenever a reel with a write enable ring is mounted on the supply hub.

ON LINE. A momentary pushbutton, which functions as alternate action. When first activated the tape unit is placed in an on-line condition; when the tape unit is on line it can be remotely selected and will be ready if tape is loaded to or past the load point. When activated again it takes the tape unit off line. The indicator is illuminated in the on-line condition.

LOAD. The momentary pushbutton activates the reel servos (tensions tape) and starts the load sequence. The indicator is illuminated when the reel servos are activated and tape is tensioned.

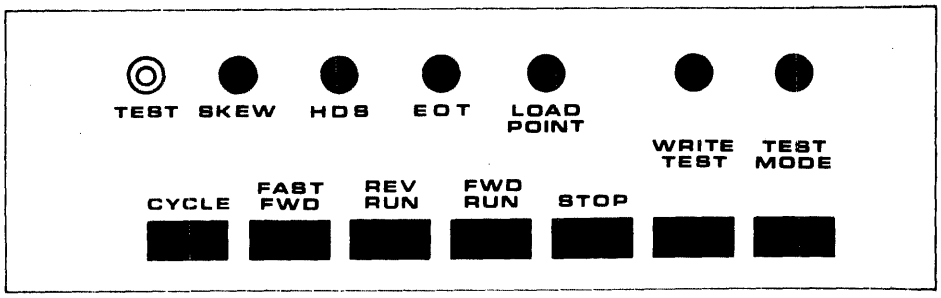
REWIND. The momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and unit is off line. The indicator is illuminated during either a local or remote rewind operation. Pressing the REWIND pushbutton at load point initiates the unload sequence.

NOTE

LOAD and REWIND pushbuttons are disabled when the tape unit is on line.

POWER. The ON/OFF switch applies power to the tape transport.

Figure 1-2. Control Panel Controls and Indicators



NOTE

Tape transport must be off line and STOP pushbutton depressed before test panel can become functional.

TEST point and SKEW indicator. Indicator lights if tape skew exceeds the appropriate skew (read or write) gate setting. An oscilloscope test point is available for monitoring skew gate timing.

HDS indicator. Indicates that high density mode has been selected.

EOT indicator. Indicates when tape has reached or passed end of tape.

LOAD POINT indicator. Indicates when tape is at load point.

CYCLE pushbutton. An interlocked pushbutton which runs tape in alternating forward and reverse modes. Useful for making ramp or vacuum sensor adjustments. Depressing STOP pushbutton terminates this operation.

FAST FORWARD pushbutton. An interlocked pushbutton switch that allows tape unit to run forward at fast speed. Depressing STOP pushbutton or EOT marker terminates this operation.

REVERSE RUN pushbutton. An interlocked pushbutton switch that allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton or load point marker terminates this operation.

FORWARD RUN pushbutton. An interlocked pushbutton switch that allows tape unit to proceed forward at normal speed. Depressing STOP pushbutton or EOT marker terminates this operation.

STOP pushbutton. An interlocked pushbutton switch that terminates all tape motion.

WRITE TEST pushbutton and indicator. A momentary pushbutton which programs 1's to be written on all channels to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator remains illuminated while unit is in this mode.

TEST MODE pushbutton and indicator. A momentary pushbutton selects test mode and activates test panel. When indicator is illuminated, test panel is active. (Tape unit must be off line and STOP pushbutton depressed before test panel will function.)

Test Panel Controls and Indicators

1.4 INTERFACE CONNECTIONS

The interface connectors on the Model 9100 are designed for twisted pair inputs and outputs. For each active pin there is a ground pin. The mating interface connectors, three 36-pin edge connectors (PN 121-0096) are supplied with the tape unit.

1.5 INTERFACE SIGNAL CHARACTERISTICS

The tape unit responds to zero true inputs and provides zero true outputs. Each signal input is terminated in such a manner as to provide matching for twisted pair cables. See Figure 1-3. Each output line is driven with an open collector driver. For best results the typical interfacing circuit configurations shown in Figure 1-4 should be used. The recommended twisted pair cable will reduce the magnitude of intercable crosstalk. Unless otherwise specified all wires should be 24 AWG minimum, with a minimum insulation thickness of 0.01 inch. Each pair should have not less than one twist per inch and the input-output cables should not exceed 20 feet in length.

1.6 INPUT SIGNAL DESCRIPTION

The input receiver circuits, due to zero true current sinking logic design, will interpret a disconnected wire or removal of power at the transmitter as a logic 0 or false condition. The logic 1 or true state requires 25 ma current sink with less than 0.4v.

The logic 0 or false state will be 3v due to the input matching resistors (see Figure 1-3). The recommended input pulse width is 2 microseconds. The rise and fall times for pulses and levels must be less than 0.5 microsecond. Each input is enabled when the tape transport is on line and selected.

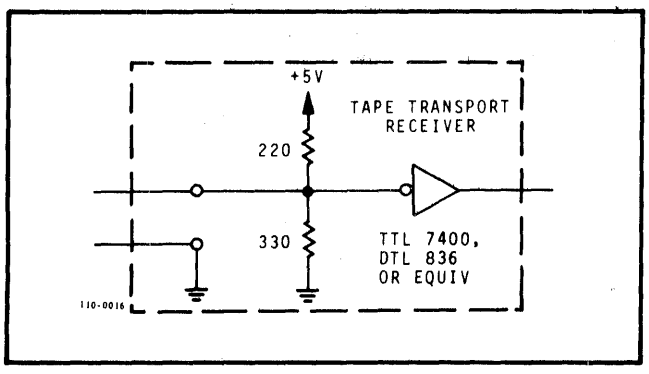


Figure 1-3. Typical Receiver Circuit

1.7 OUTPUT SIGNAL DESCRIPTION

Each output line is driven with an open collector current sinking logic driver which is capable of sinking up to 40 ma in the true state. All outputs are disabled (false) when the tape unit is not on line or not selected.

1.8 TAPE MOTION COMMANDS

For maximum interface convenience, Model 9100 is configured to control tape motion and direction using the SYNCHRONOUS FORWARD command and SYNCHRONOUS REVERSE command. The tape transport capstan servo accelerates the tape to the required speed with a linear ramp. The tape is also decelerated to a stop with a linear ramp. Start and stop occurs within the interrecord gaps. The ramp time is **5 ms for 75 ips** and varies inversely with tape speed. The amount of tape travel during the ramp up or ramp down is always **0.19 inch.**

These two factors are to be taken into consideration when writing and gapping. A delay is required before writing to insure that tape is up to speed and to allow read after write. Timing diagrams for pertinent commands to provide properly formatted tapes are shown in Figures 1-5 through 1-7.

Figure 1-5 shows the timing requirements for writing a block in a read after write system (dual gap head) in the write mode with read occurring immediately after writing. Figure 1-6 shows the timing requirements for reading a block in the forward direction. Figure 1-7 shows the timing requirements for reading a block on a read after write system in the reverse direction.

1.9 INTERFACE INPUT SIGNALS

All commands from and to the input/output connector are preconditioned by loading tape and placing the tape unit on line using the front panel controls. The next commands set up the recorder.

1.9.1 SETUP COMMANDS

TRANSPORT SELECT

SLT	Level	P1-J

A level that when true enables all the interface drivers and receivers in the transport, thus connecting the transport to the controller. Transport must also be on line, and SLT must be true for entire sequence (until tape motion stops). The SLT level may be removed to disconnect the machine from the system. The read or write status will remain in the last established condition.

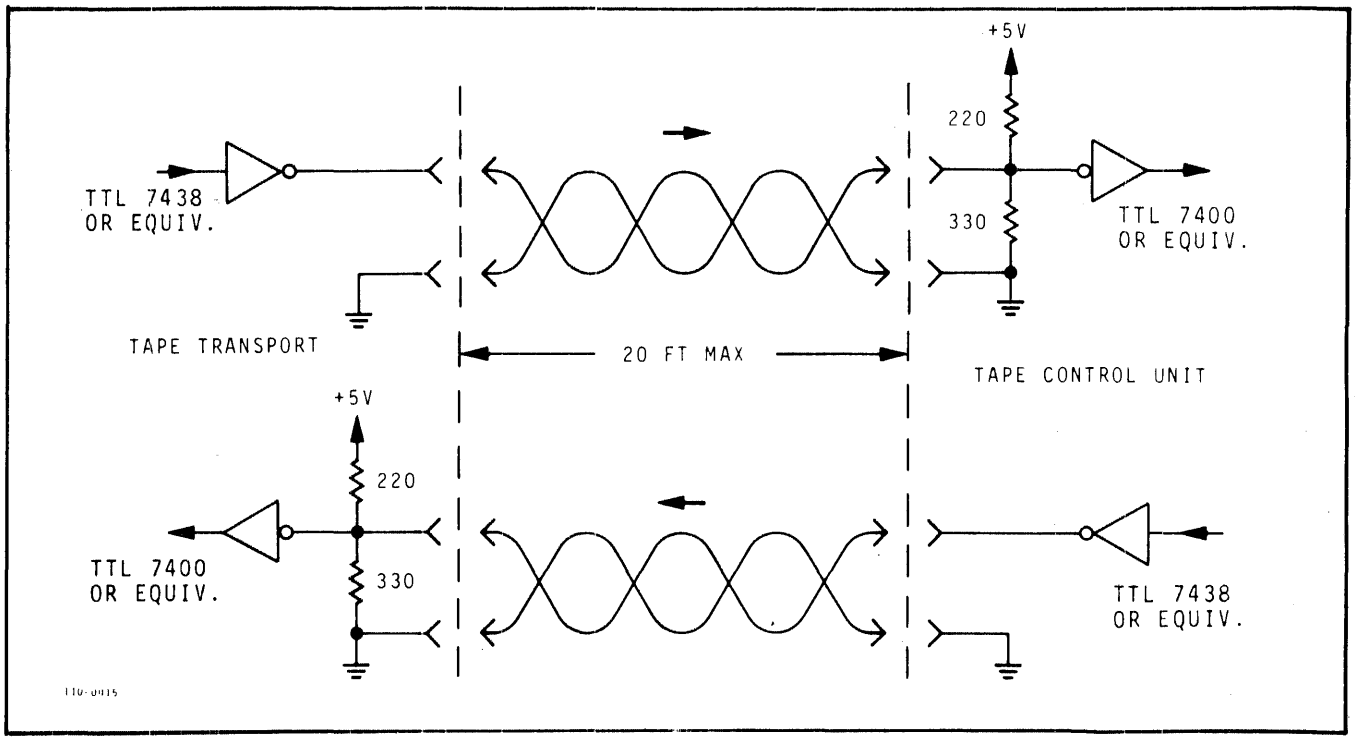


Figure 1-4. Typical Interface Configuration

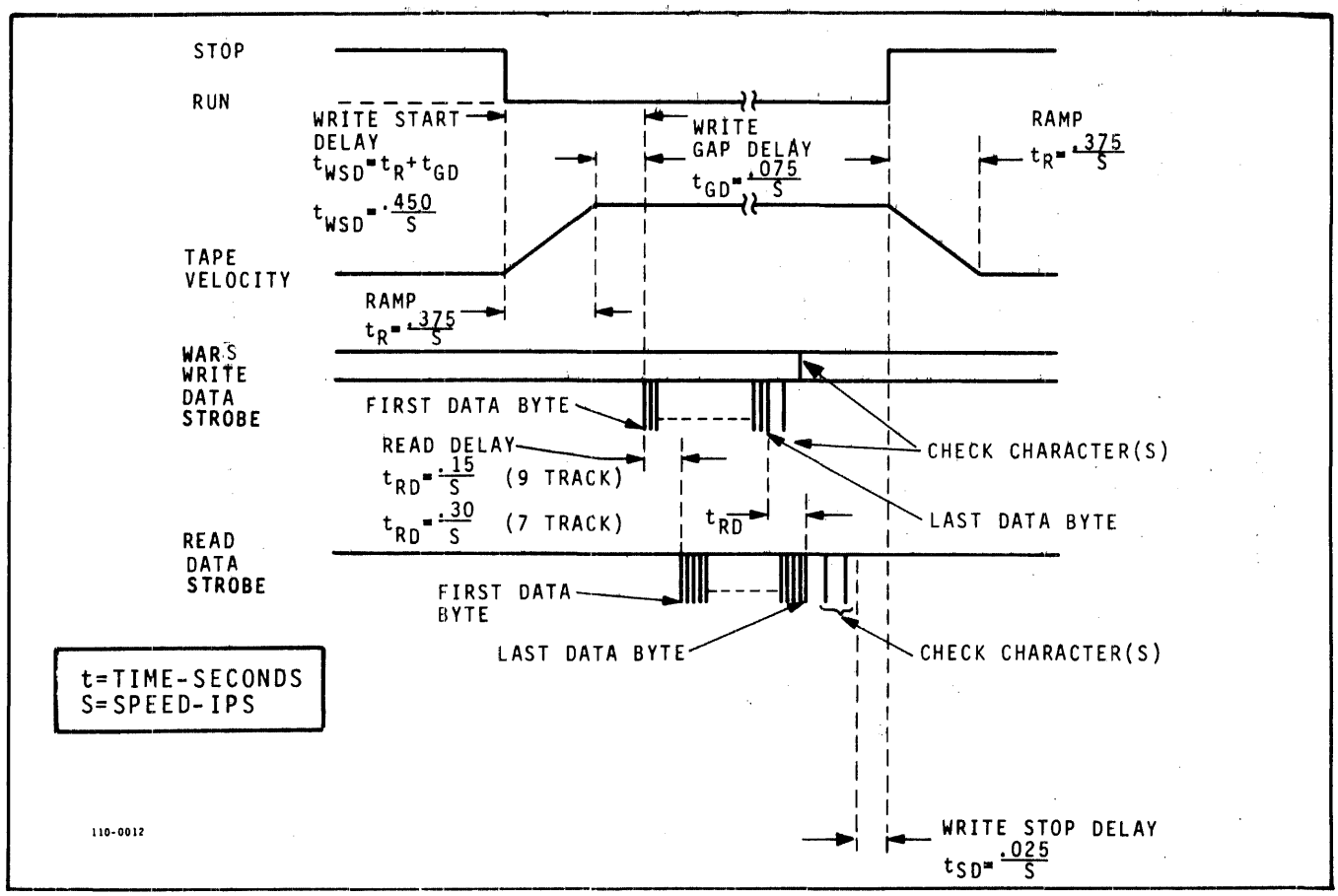


Figure 1-5. Write Timing

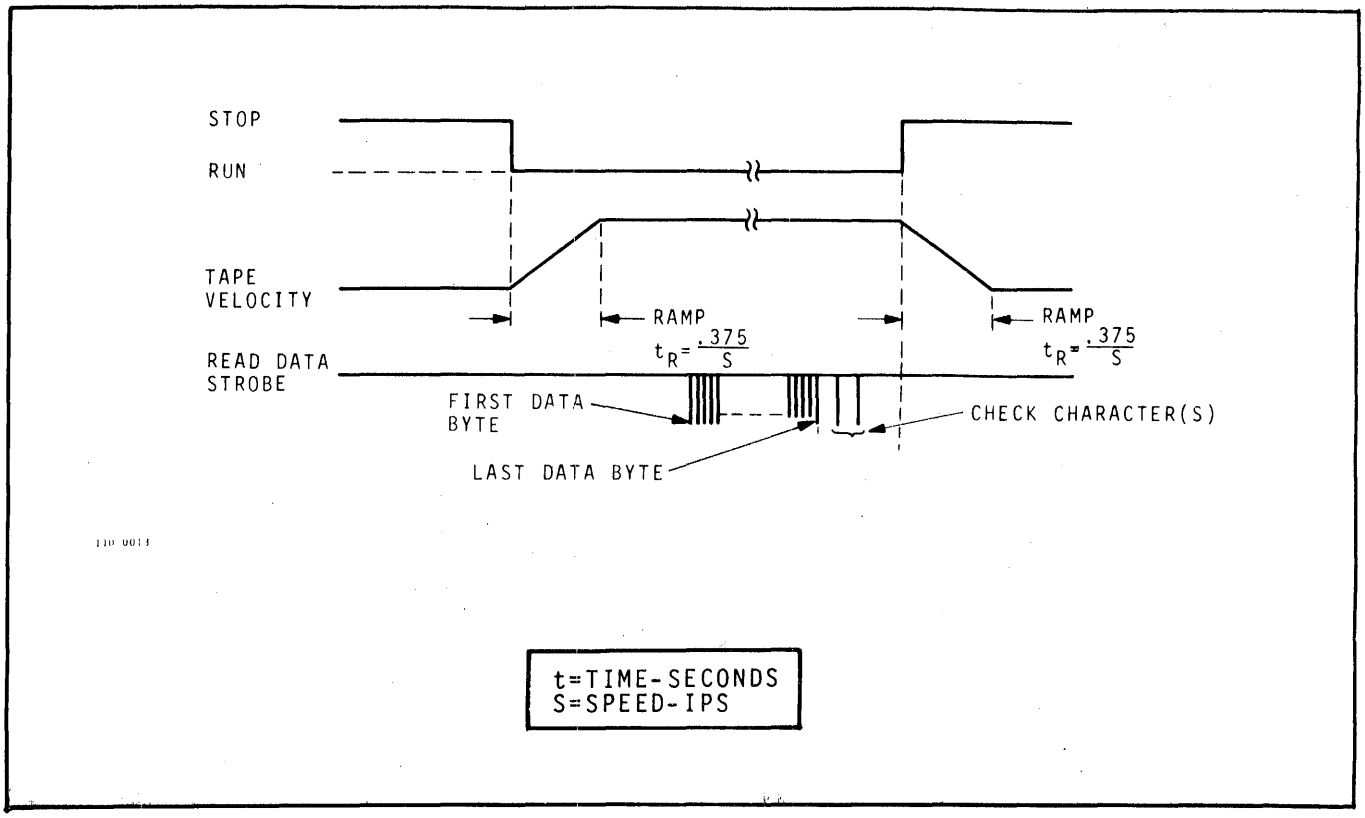


Figure 1-6. Read Forward Timing

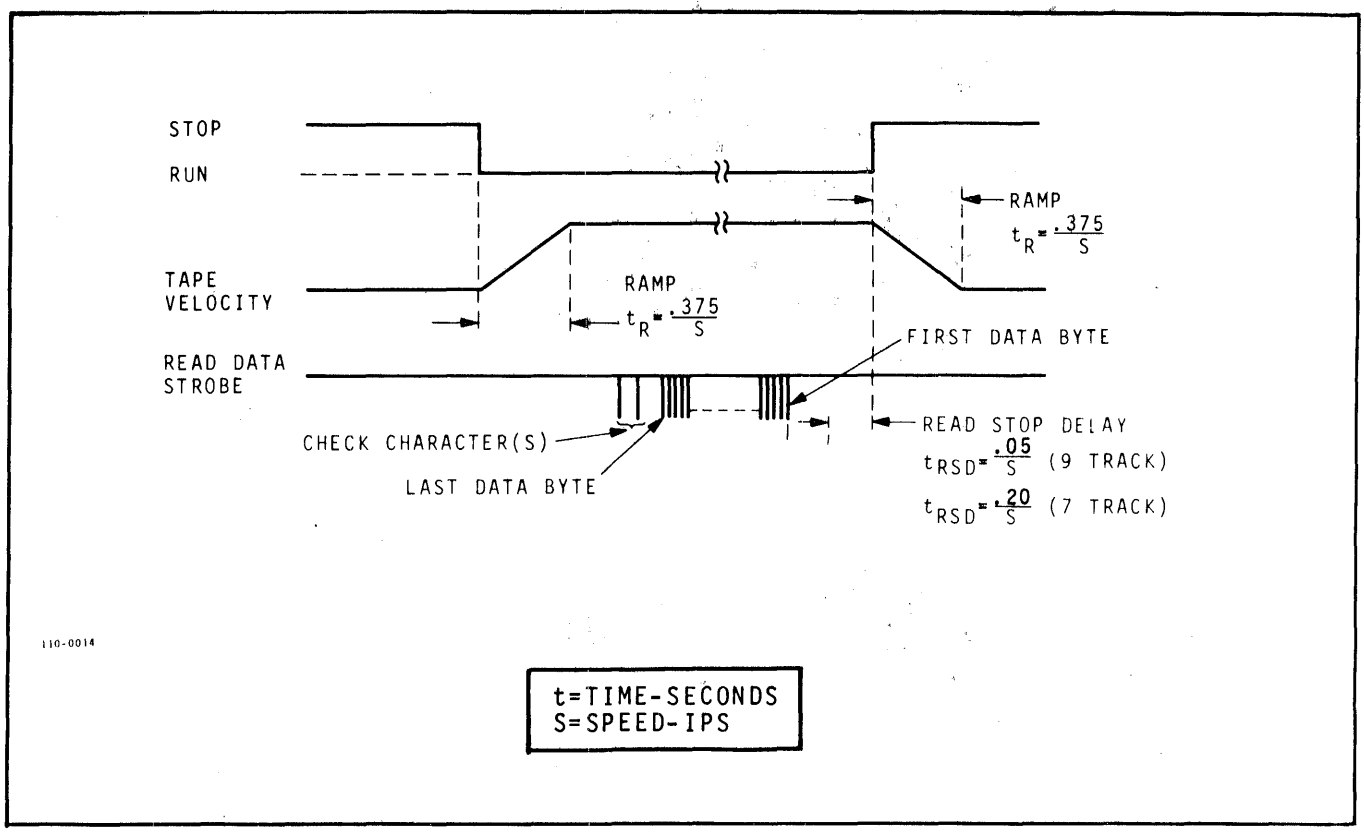


Figure 1-7. Read Reverse Timing

DATA DENSITY SELECT
(Dual Density only)

DDS	Level	P1-D

Used when the TRANSPORT DENSITY SELECT switch is in the remote position. When true, this level selects the high read density (dual density).

1.9.2 TAPE MOTION COMMANDS

OVERWRITE (OPTIONAL)

OVW	Level	P1-B

A level that when true conditions appropriate circuitry in the transport to allow updating (rewriting) of a selected record. The transport must be in the write mode of operation to utilize the OVW feature.

SYNCHRONOUS FORWARD COMMAND

SFC	Level	P1-C

A level that when true, and the transport is ready and on line, causes tape to move forward at the specified speed. When the level goes false, tape motion ramps down and ceases.

SYNCHRONOUS REVERSE COMMAND

SRC	Level	P1-E

A level that when true, and the transport is ready and on line, causes tape to move in a reverse direction at the specified speed. When the level goes false, tape motion ramps down and ceases. If the load point marker is detected during a SRC, the SRC will be terminated. If a SRC is given when the tape is at load point, it will be ignored.

REWIND COMMAND

RWC	Pulse	P1-H

A pulse input will rewind the tape past the load point and stop. The transport will then initiate a load forward sequence and return the tape to the load point marker. This input will be accepted only if the load point output is false. The transport may be taken off line while rewind is still in process. Rewind will continue normally.

1.9.3 WRITE COMMANDS

SET WRITE STATUS

SWS	Level	P1-K

A level that must be true at the leading edge of a SFC (or RUN and FWD) when the write mode of operation is required, and must remain true for a minimum of 10 μsec after the leading edge of the SFC (or RUN and FWD). SWS is sampled at the leading edge of the SFC (or RUN and FWD), toggling the read/write flip-flop to the appropriate state. Internal interlocks in the tape unit will prevent writing in the reverse direction, when the write enable ring is missing, when the tape unit is off line, when loading to load point, and during a rewind.

WRITE DATA INPUTS

Nine Track	Seven Track	
WDP	WDC	P2-L
WD0		P2-M
WD1		P2-N
WD2	WDB	P2-P
WD3	WDA	P2-R
WD4	WD8	P2-S
WD5	WD4	P2-T
WD6	WD2	P2-U
WD7	WD1	P2-V

Nine lines for nine-track operation, seven lines for seven-track operation. These are levels that if true at WDS time will result in a flux transition being recorded on tape (transport is in the write mode). Inputs must remain quiescent 0.1 μsec beyond the trailing edge of the WDS pulse. The CRCC is written by providing the correct data character together with a WDS four character times after the last data character of the record.

The LRCC is written using the WARS signal. The LRCC can also be written by providing the correct data character together with a WDS. If the LRCC is written (DATA-WDS) in this manner a WARS should be given one character time after the LRCC to insure proper IRG erasure in case of data input error.

WRITE DATA STROBE

WDS	Pulse	P2-A

A pulse of 1 μsec nominal width for each character to be written. Writing occurs on the trailing edge of the WDS. WDS may be a 1 μsec minimum, 1.5 μsec maximum pulse. Data inputs must have settled for at least 0.1 μsec before the leading edge of WDS and remain quiescent for at least 0.1 μsec beyond the trailing edge.

WRITE AMPLIFIER RESET

WARS	Pulse	P2-C

A pulse of 1 μsec nominal width that, when true, resets the write amplifier circuits on the leading edge which is delayed internally by the write deskewing network. The purpose of this line is to enable writing of the longitudinal redundancy check character (LRCC) at the end of a record. This insures that all tracks are properly erased in an interrecord gap (IRG).

In a seven-track system, the leading edge of the WARS pulse should be four character times after the leading edge of the WDS associated with the last data character in the block. In a nine-track system, the leading edge of the WARS pulse should be eight character times after the leading edge of the WDS associated with the last data character in the block (four character times after the CRCC is written).

1.9.4 READ COMMANDS

The tape unit will always have read selected. When write is selected (SWS) the data just written will be read back using a high threshold level on the read amplifiers. When SWS is false the normal threshold is applied to the read amplifiers.

AUTOMATIC CLIPPING LEVEL DISABLE
ACLD Level P3-6

When true this level overrides the automatic clipping level electronics and holds the read electronics in the normal clipping level. The switching between read and write clipping levels is not affected.

1.9.5 SHUTDOWN COMMANDS

The use of a given magnetic tape unit may be terminated by an OFF LINE command. Once this command is given the tape unit may be returned to an interface command only by operating the front panel ON LINE switch.

OFF LINE COMMAND
OFFC Pulse P1-L

A level or pulse (minimum width 1 μsec) that resets the on-line flip-flop to the zero state, placing the transport under manual control. It is gated only by SELECT in the transport logic, allowing an OFFC to be given while a rewind is in progress. An OFFC should be separated from a rewind command by at least 2 μsec.

1.10 INTERFACE OUTPUT SIGNALS

All output signals are enabled only when the tape transport is ON LINE and SELECTED.

1.10.1 STATUS OUTPUTS

ON LINE
ONL Level P1-M

A level that is true when the on-line flip-flop is set. When true, the transport is under remote control. When false, the transport is under local control.

TRANSPORT READY
RDY Level P1-T

A level that is true when the tape transport is on tape; that is, when the initial load sequence is complete and the transport is not rewinding. When true, the transport is ready to receive a remote command.

HIGH DENSITY INDICATOR
(Dual Density only)
HDI Level P1-F

A level that is true only when the high-density mode of operation is selected.

FILE PROTECT
FPT Level P1-P

A level that is true when a reel of tape without a write-enable ring is mounted on the transport supply (or file) hub.

WRITE ENABLE
WEN Level P1-S

A level that is true when a reel of tape with a write-enable ring is mounted on the transport supply (or file) hub. Opposite of file protect.

LOAD POINT
LDP Level P1-R

A level that is true when the load point marker is under the photosensor and the transport is not rewinding. After receipt of a SFC the signal will remain true until the load point marker leaves the photosense area.

TAPE RUNNING
RNG Level P1-V

This is a level that is true when tape is being moved under capstan control and remains true until tape motion has ceased. (Includes forward, reverse, and rewind tape motion.)

END OF TAPE
EOT Level P1-U

A level that is true when the EOT marker is detected in the forward direction. Goes false when the EOT marker is detected in reverse (SRC or REWIND).

REWINDING
RWD Level P1-N

A level that is true when the transport is engaged in a rewind operation or returning to the load point at the end of the rewind operation.

1.10.2 READ OUTPUTS

Read outputs are present at all times. The high threshold level is selected internally when SWS is selected.

READ DATA STROBE

RDS Pulse P3-2
(Not used in phase encoded operation)

A pulse for each data character read from tape in NRZ1. The average time (τ_1) between two read data strobes is

$$\tau_1 \text{ (sec)} = \frac{1}{s \cdot d}$$

Read clock pulse width (t_w) is

$$t_w = \frac{1}{s \cdot d \cdot 32} = \frac{\tau_1}{32}$$

where

s = tape speed in inches per second
d = density characters per inch

The minimum time between consecutive read data strobes is less than this figure owing to skew and bit crowding effects. A guaranteed safe value for the minimum time is 1/2 τ_1.

READ GAP DETECT

RGAP Level P3-12
(Not used for phase encoded operation)

A level that is true approximately 20 character spacings after the last data byte (16 character spacings on seven-channel), and remains true until the first data byte of the subsequent data block. Note: This level will be true whenever tape motion is at rest.

READ DATA LEVEL (NRZ1 MODE)

Nine Track	Seven Track	
RDP	RDC	P3-1
RD0		P3-3
RD1		P3-4
RD2	RDB	P3-8
RD3	RDA	P3-9
RD4	RD8	P3-14
RD5	RD4	P3-15
RD6	RD2	P3-17
RD7	RD1	P3-18

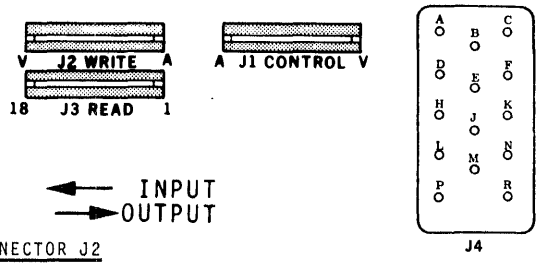
Nine lines, nine track; seven lines, seven track. These lines may be strobed by either edge of the read clock and remain true for 1/64 of a character time following the trailing edge of the read clock. Note: A CRC character may be all zeros, which will not cause a read clock.

1.11 STATION SELECT SWITCH

The station select unit on the front panel of the Model 9100 is wired as shown in Figure 1-8. When using the station select switch, disconnect the SELECT line connected to J1-J of the Model 9100.

1.12 SUMMARY OF CHARACTERISTICS

Figure 1-8 shows the location of connectors and pin numbers with signal names.



WRITE CONNECTOR J2

ACTIVE	GROUND		SIGNAL	MNEMONIC
A	1	←	WRITE DATA STROBE	WDS
B	2	←	N.C.	
C	3		WRITE AMPLIFIER RESET	WARS
D	4		NOT USED	
E	5		NOT USED	
F	6		NOT USED	
H	7		NOT USED	
J	8		NOT USED	
K	9		NOT USED	
L	10	←	WRITE DATA CHANNEL P	WDP
M	11	←	WRITE DATA CHANNEL 0	WD0
N	12	←	WRITE DATA CHANNEL 1	WD1
P	13	←	WRITE DATA CHANNEL 2	WD2
R	14	←	WRITE DATA CHANNEL 3	WD3
S	15	←	WRITE DATA CHANNEL 4	WD4
T	16	←	WRITE DATA CHANNEL 5	WD5
U	17	←	WRITE DATA CHANNEL 6	WD6
V	18	←	WRITE DATA CHANNEL 7	WD7

CONTROL CONNECTOR J1

ACTIVE	GROUND		SIGNAL	MNEMONIC
A	1	←	LOAD ON LINE (OPTIONAL)	LOL
B	2	←	OVERWRITE	OVW
C	3	←	SYNCHRONOUS FORWARD	SFC
D	4	←	HIGH DENSITY SELECT	HDS
E	5	←	SYNCHRONOUS REVERSE	SRC
F	6	→	HIGH DENSITY INDICATOR	HDI
H	7	←	REWIND COMMAND	RWC
J	8	←	SELECT	SLT
K	9	←	SET WRITE STATUS	SWS
L	10	←	OFF LINE COMMAND	OFFC
M	11	→	ON LINE	ONL
N	12	→	REWINDING	RWD
P	13	→	FILE PROTECT	FPT
R	14	→	LOAD POINT	LP
S	15	→	WRITE ENABLE	WEN
T	16	→	TRANSPORT READY	RDY
U	17	→	END OF TAPE	EOT
V	18	→	TAPE RUNNING	TRNG

READ CONNECTOR J3

ACTIVE	GROUND		SIGNAL	MNEMONIC
1	A	→	READ DATA CHANNEL P	RDP
2	B	→	READ DATA STROBE	RDS
3	C	→	READ DATA CHANNEL 0	RD0
4	D	→	READ DATA CHANNEL 1	RD1
5	E		NOT USED	
6	F	→	AUTO DISABLE	
7	H		NOT USED	
8	J	→	READ DATA CHANNEL 2	RD2
9	K	→	READ DATA CHANNEL 3	RD3
10	L		NOT USED	
11	M		NOT USED	
12	N	→	GAP DETECT	
13	P		NOT USED	
14	R	→	READ DATA CHANNEL 4	RD4
15	S	→	READ DATA CHANNEL 5	RD5
16	T		NOT USED	
17	U	→	READ DATA CHANNEL 6	RD6
18	V	→	READ DATA CHANNEL 7	RD7

STATION SELECT CONNECTOR J4

ACTIVE	GROUND		SIGNAL	MNEMONIC
A,C	B	←	SELECTS STATION 1	SLT1
D,F	E	←	SELECTS STATION 2	SLT2
H,K	J	←	SELECTS STATION 3	SLT3
P,R	M	←	SELECTS STATION 4	SLT4

Figure 1-8. Summary of Interface Characteristics

SECTION II
INSTALLATION AND OPERATION

SECTION II
INSTALLATION AND OPERATION

2.1 INSTALLATION

2.1.1 INSPECTION

Prior to installation, inspect thoroughly for foreign material that may have become lodged in the vacuum columns, reel hubs, and other moving parts.

2.1.2 MOUNTING

Physical dimensions and outline of the tape transport are shown in Figure 1-1. The transport requires 24.5 inches vertical mounting space on the standard 19 inch rack. The transport is mounted on a pair of slides which are attached to the rack. The slides are equipped with a lockout mechanism, shown in Figure 2-1, that prevents their overextension. The lockout mechanism is gravity activated, requiring each slide to be mounted on the side of the cabinet for which it was designed, as indicated on the slide. To ascertain that the slides are mounted correctly, open one slide (of the pair) and look for the letters RH (right hand) or LH (left hand) stamped directly above the lockout lever on the forward portion of the intermediate channel, as shown in Figure 2-1. The slide designated RH should be mounted on the right hand side of the cabinet when facing the unit. With the right and left hand slides securely fastened to the cabinet and in extended position, align the quick disconnect strips attached to the sides of the transport with the center track of the slides, as shown in Figure 2-2. Push transport towards cabinet until fully engaged.

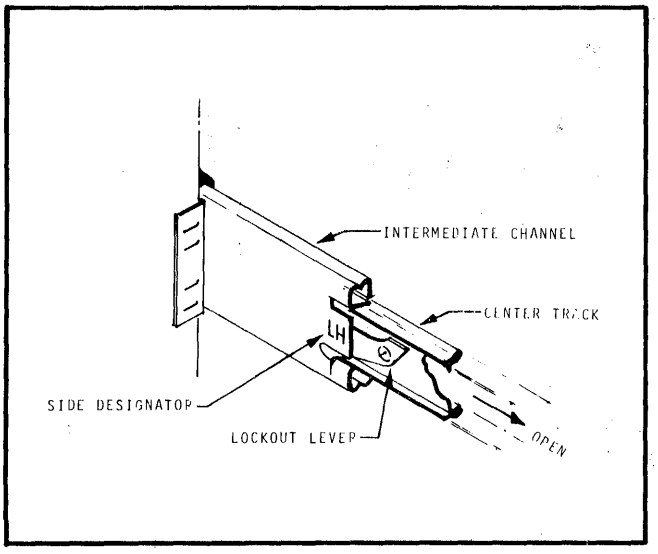


Figure 2-1. Slide Identification

CAUTION

To avoid personal injury and/or transport damage due to dropping of unit, secure transport in place by aligning captive screws on each slide with the respective threaded holes in the disconnect strips and tighten, as shown in Figure 2-2.

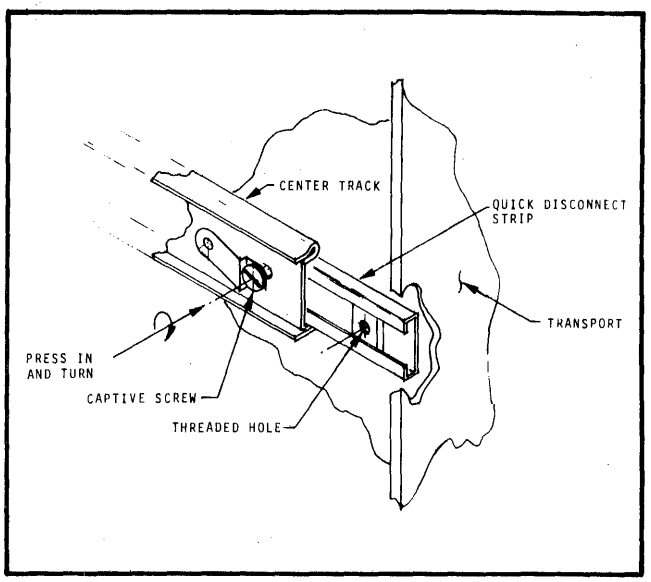


Figure 2-2. Captive Screw Location

2.1.3 SERVICE ACCESS

Access to the plug-in cards and control electronics is available with the unit extended on slides from the sides. The voltage regulator and the servo power assembly are mounted on the inside of the heatsink on the side of the transport. The fuses, power connector, and interface connectors are also accessible from the rear of the unit. For servicing electronics, test points are provided by standoff pins on circuit boards and are identified by upper case letters near each test point.

2.1.4 SUPPLIED ITEMS/REQUIRED ITEMS

All required items except the twisted pair interface cables are supplied with the unit. These required items and their part numbers include:

Empty 10.5 inch reel (113-0008-001)

Three 36 pin interface connectors (order three 121-0082-002)

Winchester Address Select Connector w/pin (121-0108-001; 121-0082-002)

Power Cord (121-9000-003)

Shipping Brace (291-4768-001)
(Shipping brace should be removed before use and saved in case the machine is to be shipped in the future.)

Set of rack mount slides (128-0151-003)

2.1.5 INTERCABLING

Installation of the tape transport requires fabrication of interconnection cables between the tape controller and the tape transport. The three 36 pin cable connectors that mate with the connectors on the units are supplied with the system.

The connector pin assignments are shown in Figure 1-8. Twisted pair cabling should be used to reduce intercable crosstalk. All wires should be 24 AWG minimum insulation thickness of 0.01 inch. Each pair should have no less than one twist per inch, and maximum cable length should not exceed 20 feet.

2.1.6 POWER CONNECTIONS

CAUTION

Before connecting the unit to the power source, make certain the line voltage is correct (115 or 230 vac) and that proper fuses have been installed.

A detachable power cord is supplied with the tape unit. The power cord is 7.5 feet long and has a NEMA three-prong (two power, one chassis ground) plug for connection to the power source.

2.2 OPERATION

2.2.1 INTERFACE

Before placing the unit in operation, make certain that the interface connection procedures outlined in Section I have been performed.

2.2.2 CONTROLS AND INDICATORS

Paragraph 1.3 lists the controls and indicators for the tape transport and describes the functions of each. The test panel controls are described in Section IV.

2.2.3 PRELIMINARY PROCEDURES

Before placing the unit in operation, proceed as follows:

a. Check the tape transport read/write head, erase head, capstan and idlers for any foreign material.

b. Check for correct line voltage and make sure that correct fuses are installed (paragraph 2.1.5).

c. Push primary power switch on control panel to ON position.

2.2.4 TAPE THREADING

To thread the tape on the transport, proceed as follows:

a. Raise the latch of the quick-release hub and place the tape file reel to be used on the supply hub (Figure 2-3) with the write enable ring side next to the transport deck.

b. Hold the reel flush against the hub flange and secure it by pressing the hub latch down.

c. Thread the tape along the path as shown on the threading diagram (Figure 2-3).

d. Holding the end of the tape, wrap a few clockwise turns around the takeup reel hub.

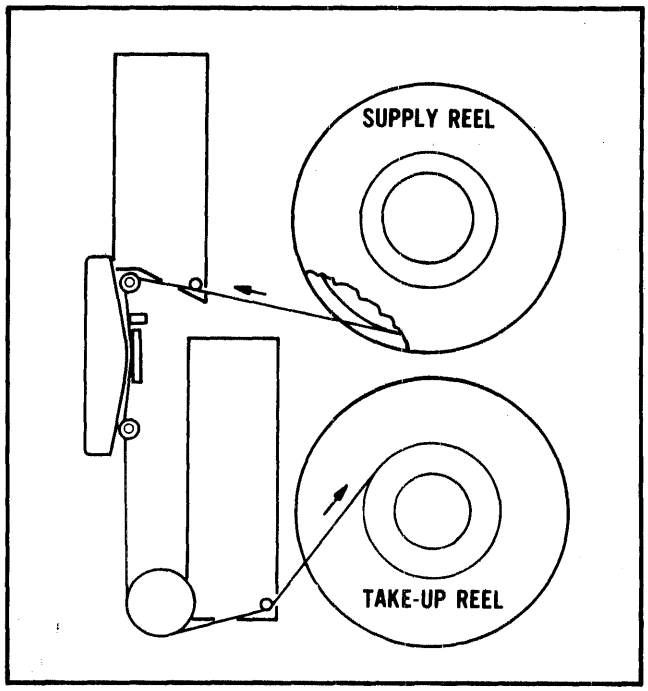


Figure 2-3. Tape Threading Diagram

2.2.5 TAPE LOADING

Pressing the LOAD pushbutton energizes the reel servos and initiates a load sequence. Tape advances to the load point marker and stops. If for some reason the load point marker is already past the sensor as, for example, when restoring power after a shutdown, tape continues to move for approximately 6 seconds and then initiates rewind automatically.

Once pressed, the LOAD switch is illuminated and remains illuminated until power has been turned off or tape is removed from the machine.

2.2.6 PLACING TAPE UNIT ON LINE

After the tape is properly threaded and has been loaded and brought to the load point, press the ON LINE pushbutton and make certain the ON LINE indicator illuminates. (The REWIND pushbutton is disabled when the tape unit is on line.) On-line status enables the tape unit to be remotely selected and to perform all normal operations under remote control.

2.2.7 TAPE UNLOADING AND REWIND

Provision is made in the 9000 series transports for rewinding a tape to load point under remote control. However, this operation may also be performed manually. Proceed as follows:

a. If the ON LINE indicator is illuminated, press the ON LINE pushbutton. The ON LINE indicator should extinguish when pressure is removed.

b. Press the REWIND pushbutton. The tape will now rewind to the load point marker.

c. After the tape has been positioned at the load point under remote or local control, press the REWIND pushbutton to rewind the tape past load point to the physical beginning of the tape.

NOTE

The rewind sequence cannot be stopped until the tape has rewound either to load point or until tape is rewound onto the supply reel after an unload sequence.

2.2.8 POWER SHUTDOWN

A tape transport should not be turned off when tape is loaded and is past the load point marker. Kennedy 9000 series transports are designed to prevent physical damage to the tape in the event of power failure, and to minimize operator error which could destroy recorded data. In the event of power failure during tape unit operation, manually wind the tape forward several feet before restoring power. When power has been restored, press the LOAD pushbutton. If load point is not reached within 36 feet, the tape will rewind, searching for load point. If desired, the tape can then be advanced to the data block nearest the point at which the power failure occurred by initiating the appropriate control commands.

Although it is possible to develop procedures which would allow power shutdown between tape files and tape records this is not recommended. Where data files are short, it is preferable to use smaller tape reels.

SECTION III
THEORY OF OPERATION

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the Model 9100 tape transport at the functional block level. The description applies to the standard dual density 800/1600 cpi, nine track, 75 ips version. Detailed circuit descriptions are included in the schematic section of the manual.

3.2 TAPE TRANSPORT CONTROL

The circuit boards in the control section of the card cage control the tape transport by generating internal tape transport commands which are based upon commands from the interface, as well as status signals from the tape transport.

In the Model 9100, the following circuit boards control the tape transport:

Type 3841 Line Terminator
Type 3842 Interface Control
Type 3843 Pushbutton Control
Type 5719 Sensor Amplifier/Driver
Type 6667 Sequence Control
Type 5733 Ramp Generator
Type 6666 Servo Control

Figure 3-1 is a block diagram of the Model 9100. Tape commands from the interface connector are supplied to the interface control board which will generate internal tape transport commands if certain interlocks are satisfied. These tape transport commands are then supplied to the Pushbutton Control board. The Sequence Control and the Pushbutton Control also contain several interlocks which must be satisfied before the Pushbutton Control can encode the tape motion commands onto one of three command lines: RUN NORMAL (RNN1), RUN FAST (RNF1), and REVERSE SELECT (RVS1). These three command lines are supplied to the Ramp Generator, which provides linear ramp-up to speed and linear ramp-down to standstill in order to minimize tape stress and maintain accurate tape speeds. The output of the Ramp Generator is supplied to the capstan servo preamplifier on the Type 5666 Servo Preamplifier board. The capstan servo uses the Ramp Generator output to control capstan motor current, while the capstan tachometer supplies a stabilizing feedback voltage to the capstan servo based on capstan motor speed.

The Type 5719 Sensor Amplifier/Driver receives input from the file protect switch, load point sensor, and end of tape sensor. These signals are amplified and gated, then supplied to the Pushbutton Control and Sequence Control as tape transport status signals for controlling their interlocks.

The Type 3844 Sensor Amplifier/Driver module also contains the drivers for the WRITE, READ, and SELECT indicators on the main control panel.

3.2.1 SEQUENCE CONTROL

Due to certain special sequencing requirements involved in controlling the tape transport, a special Sequence Control module has been developed for the Model 9100. Transport control pushbuttons on the main control panel connect directly to this board. In addition, broken tape, vacuum switch, and load point status signals are input to the Sequence Control board. Thus, when tape breaks or vacuum pressure drops, the Sequence Control will initiate the appropriate tape transport command to stop reel movement. Also, the sequencer will condition the actions caused by pressing the REWIND pushbutton dependent upon whether tape is in front of or past the load point marker.

Four sequences are discussed: the POWER ON sequence, which occurs after the POWER pushbutton is pressed, the LOAD sequence, which follows the POWER ON sequence after the LOAD pushbutton is pressed, the UNLOAD sequence, which occurs when REWIND command is given and the tape is on the load point marker, and the POWER OFF sequence, when unit is loaded and power is turned off from the front panel.

3.2.1.1 POWER ON Sequence

When the POWER pushbutton is pressed, the low power transformer and various regulated voltages are generated. The vacuum blower and high power transformer are enabled through main relay K4.

3.2.1.2 LOAD Sequence

During this sequence, the vacuum blower motor is turned on, +24 vdc and -24 vdc is supplied to the electronics, servo relay K1 is actuated to enable reel motors and power latch, tape is tensioned and

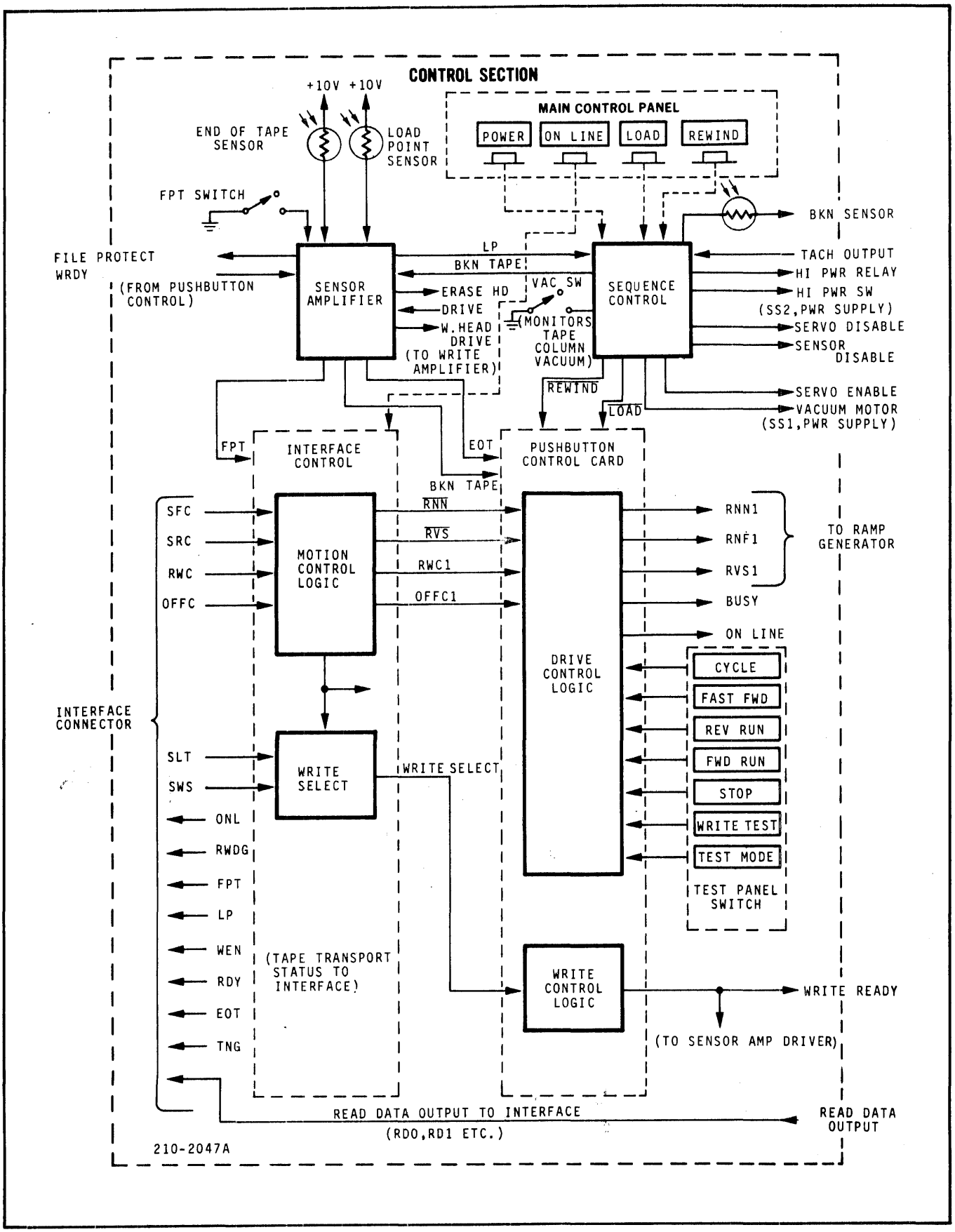


Figure 3-1. Control Logic Block Diagram

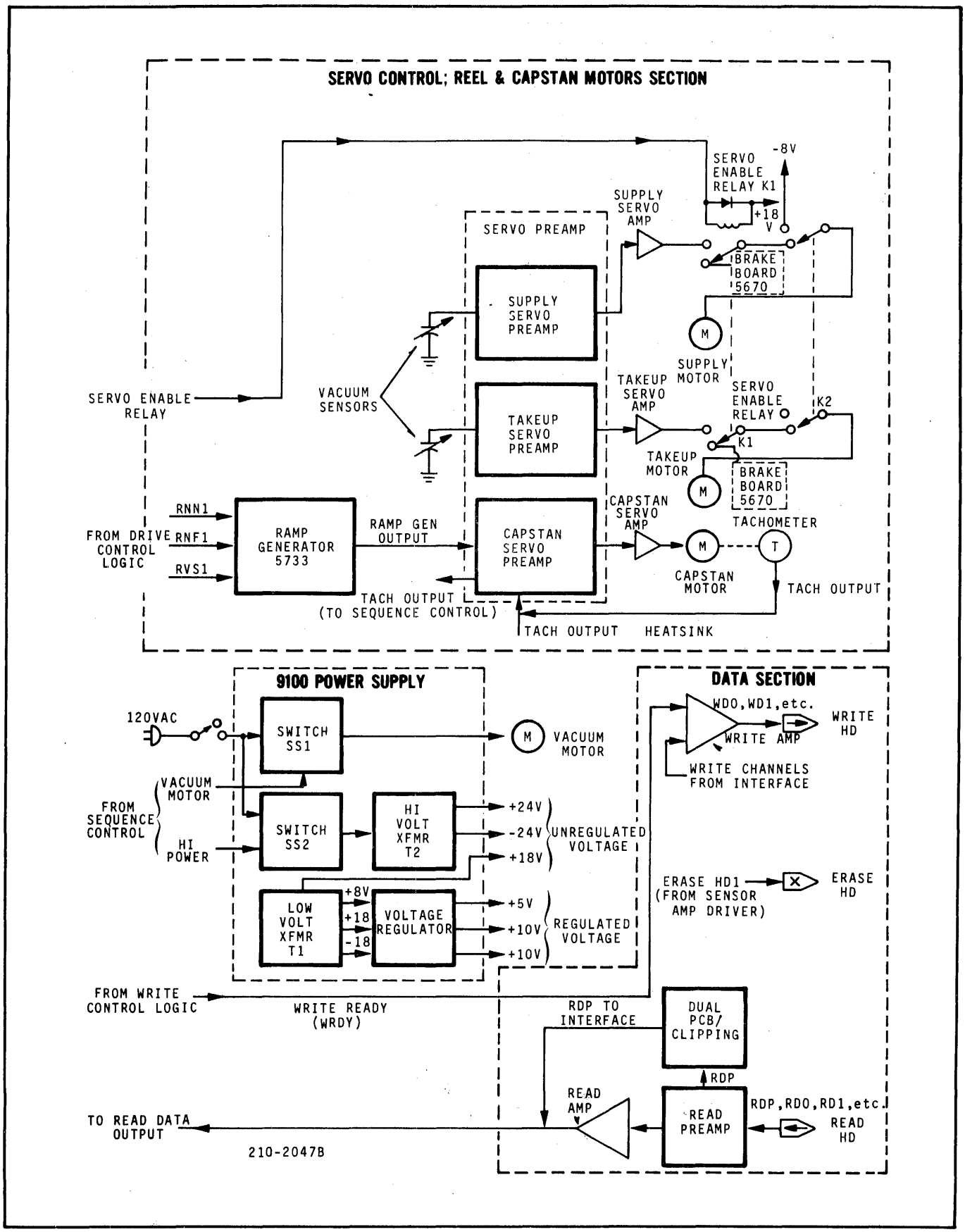


Figure 3-1. Control Logic Block Diagram

drawn into the vacuum columns, and the reel servo loop is closed. At the completion of this sequence, the tape is properly tensioned. The capstan servo now receives the command to advance at normal speed to load point and then stops. If load point is not reached within 6 seconds after pressing the LOAD pushbutton, the sequencer will command the transport to rewind the tape, searching for load point. All operation is interrupted in case of broken tape or loss of vacuum as determined by the vacuum switch. In this instance BROKEN TAPE true signal will be supplied from the Sequence Control and all servos will be disabled immediately. An END OF TAPE true signal from the END OF TAPE sensor will not terminate a write operation. Instead, an EOT status is given to the interface, which should be used to generate a proper sequence to terminate writing.

3.2.1.3 UNLOAD Sequence

During an unload operation, the tape is slowly and completely rewound onto the supply reel after it stops at load point during a normal rewind sequence.

To initiate the unload operation, the transport must be taken off line, either through an OFF LINE interface command or by pressing the ON LINE pushbutton. Next the REWIND pushbutton is pressed. This sets the unload flip-flop on the Sequence Control board, causing UNLOAD true to be output.

This connects the supply reel motor to -8 vdc instead of +24 vdc, opening the tape position servo loop. The takeup and supply reels now slowly rotate in reverse until the tape is completely rewound. When the physical end of tape is reached, BKN tape goes true and the unload sequence is terminated. Note that the POWER pushbutton is disabled during the entire unload operation.

3.2.1.4 POWER OFF Sequence

When the POWER switch is shut off, the vacuum motor turns off immediately. The sequence is: vacuum switch off, sensor disable true (enabling the reels to remove tape from the vacuum chamber), servo disable true (applying braking signals to reels), all power then turned off.

3.3 WRITE OPERATION

(Occurs after LOAD sequence is completed)
The main pushbutton panel on the front of the tape deck is used to prepare the transport for operation. After power is turned on and the tape is properly threaded, the front panel LOAD pushbutton is pressed and the machine goes through the load sequence described above. Pressing the front panel ON LINE pushbutton now places the transport on line, preparing the transport to respond to interface commands as soon as they are available. When the transport is selected by a SLT true command from the interface, the Interface Control board's gates are enabled, allowing the transport to accept interface commands and return transport status signals to the interface.

Interlocks ensure that the transport writes data on tape only when the tape is properly loaded, the reel has a write enable ring, and the tape is moving forward at normal running speed. When SET WRITE STATUS from the interface goes true under these conditions, WRITE READY true is supplied to the Sensor Amplifier/Driver module. Here it turns on the write and erase head current drivers and illuminates the WRITE indicator on the front panel. WRITE READY and SELECT1 (combining ON LINE true and SELECT true) are also supplied to the data electronics card cage where they enable the write and read amplifier stages. With WRITE READY true, the interface supplies the properly formatted data to be written on tape.

3.4 READ OPERATION

When the tape is properly loaded, not rewinding, and WRITE READY is false, a read operation is selected and the Sensor Amplifier/Driver module illuminates the front panel READ indicator. The read preamplifier and amplifier are now enabled to generate read signals back to the interface.

3.5 TEST PANEL

The test panel is standard equipment in the Model 9100. Located next to the control panel, it is used to perform tests and adjustments on the tape transport while it is off line. This eliminates the need for many external test fixtures as well as saving valuable computer time.

The panel becomes operational only when the transport is off line, and the test panel STOP pushbutton is pressed. If these conditions are satisfied the test panel pushbuttons are enabled when the TEST MODE pushbutton is pressed. (The function of each test panel control and indicator is provided in Figure 4-2 of the maintenance section.)

Basically, the test panel is used for making skew, speed, ramp time, and servo system adjustments. Besides providing complete control over tape speed and direction, it can initiate a write test by generating a crystal controlled all-1 test pattern on the tape.

The test panel also contains indicator lamps which illuminate when there is excessive skew, high density is selected, end of tape or load point is reached, or a write test is being performed. (The skew test indicates proper alignment of the read/write head.)

The test panel also contains a CYCLE pushbutton, which runs the tape forward and reverse continuously for making ramp time and reel servo adjustments.

The logic circuitry required to translate test panel commands into tape transport commands is located on the Pushbutton Control card. The skew detect network for making skew tests is located on the Dual Density Control contained in the data section of the card cage.

3.6 TAPE TRANSPORT CONTROL ADJUSTMENTS

The Kennedy tape transport requires few adjustments. These are preset at the factory and should not be changed unless there is strong reason to believe adjustment is required. The following adjustments are made on the control logic modules:

Adjustment	Location
Normal running speed	R14, Ramp Generator
Ramp-up time	R3, Ramp Generator
Ramp-down time	R4, Ramp Generator
End of tape/beginning of tape	R16, Sensor/Amplifier Driver

The adjustment procedures are outlined in the maintenance section of the manual and in the circuit descriptions of the individual schematics.

3.7 SERVO SYSTEM

3.7.1 INTRODUCTION

The transport servo system advances the tape past the tape heads at a precisely controlled speed while maintaining a constant tape tension. The servo section is composed of three basic blocks: the takeup and supply vacuum sensors, takeup and supply reel servos, and the capstan motor servo.

3.7.2 VACUUM SENSORS AND REEL SERVOS

When the machine is running forward normally, tape loops form approximately half way up the takeup and supply vacuum columns. (This position will vary depending on tape direction and speed. However, tape loop position should not fluctuate once established in any given mode.) Two specially designed tape sensors are positioned behind the tape loops to maintain the tape loop position while the tape is in motion. These sensors are variable capacitors. Each capacitor consists of a plated PC board covered with flexible, metallized mylar. The edges of the board are 5/1000 inch thicker than the copper center, forming a long groove (see Figure 3-2). Several holes are drilled through the board. The grooved area is covered with metallized plastic, mylar side down to form a dielectric. Wires are connected to the metallized covering and the copper plate to form a capacitor. The sensor is then mounted to a hollow metal chamber to form the base of the column.

When the Model 9100 is turned on and forward mode is selected, the vacuum pump attached to the back of the vacuum chamber draws the tape upward into the tape chamber (see Figure 3-3). A high vacuum exists above the tape in the enclosed portion of the chamber. No vacuum exists at the open end of the tape chamber. A partial vacuum is present in the vacuum chamber behind the tape sensor.

Since there are holes drilled in the sensor, the difference in pressure thus created presses the metallized mylar covering against the copper plate over the area below the tape loop. Thus the capacitance of the sensor changes as the tape loop moves in the column.

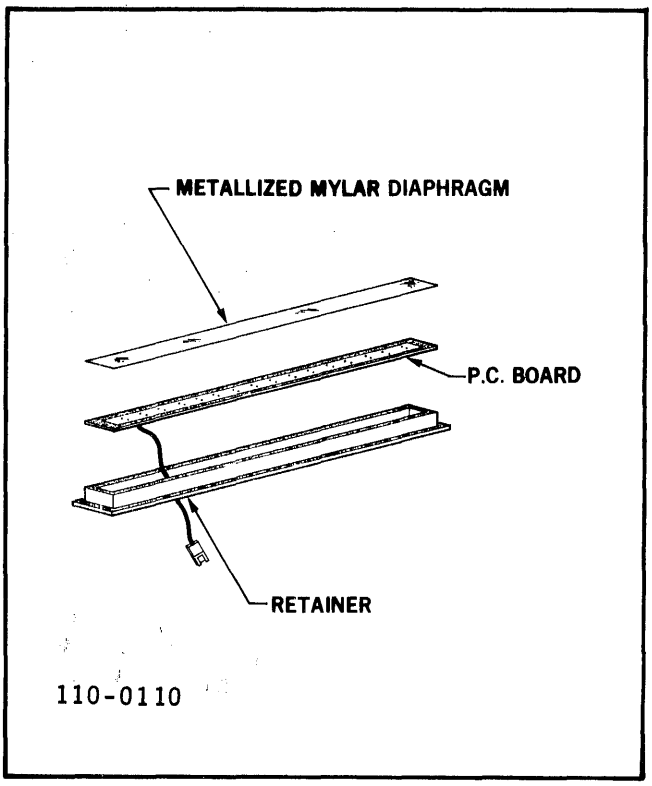


Figure 3-2. Vacuum Sensor Assembly

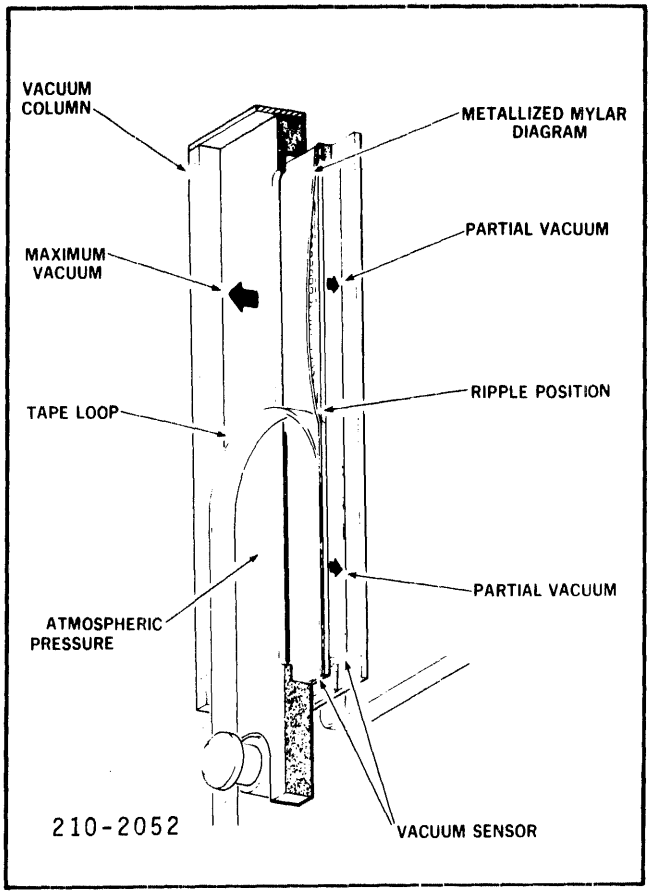


Figure 3-3. Vacuum Sensor Operation: Cross Section View

The tape loop sensors are connected to an oscillator as the frequency control element. Any capacitance increase caused by the tape loop moving up the column decreases the output frequency of the oscillator and vice versa. This output frequency is integrated and filtered, and dc zeroed in to develop a dc motor control voltage. Thus the torque of the reel motors is controlled to centralize the tape loops within the vacuum columns during operation.

3.7.3 CAPSTAN SERVO AMPLIFIER

A RUN NORMAL, RUN FAST, or REVERSE signal from the Ramp Generator is decoded and then supplied to the Capstan Servo Amplifier on the Type 6666 Servo board. This capstan servo can be disabled by SERVO DISABLE true from the Sequence Control. Motor speed is kept constant by feedback from a tachometer mounted to the capstan motor. This feedback is compared to the Ramp Generator input. Any difference voltage caused by motor speed deviation is amplified to develop a corrective voltage for returning the motor to proper speed. A sampling of tachometer output is also directed to the Sequence Control.

3.7.4 SERVO SYSTEM ADJUSTMENTS

These adjustments are preset in the factory and should not be changed unless there is strong reason to believe adjustment is required. Adjustment procedures are outlined in the maintenance section of the manual and in the circuit description of the servo system schematic.

Adjustment: R4, R54 Frequency Controls
Function: varies basic frequency of oscillators to control speed of reel motors
Location: Type 6666 Servo Preamplifier

Adjustment: R17, R65 Gain Potentiometers
Function: eliminates tape loop overshoot when tape direction is changed
Location: Type 6666 Servo Preamplifiers

Adjustment: R115 Capstan Servo Zero
Function: eliminates capstan creep when tape is stopped
Location: Type 6666 Servo Preamplifier

3.8 DATA SECTION

3.8.1 INTRODUCTION

The data section includes read/write amplifiers and interface cards containing output drivers and timing controls. Block diagrams are shown in Figures 3-4 and 3-5.

The data section consists of seven circuit cards that plug into the data masterboard. These include a Dual Density Control, a Dual P Channel/Clipping Control, a pair of Quad Read Amplifier modules, a Four Channel Write Amplifier card, a Five Channel Write Amplifier card, and a Data Terminator card.

3.8.2 WRITE ELECTRONICS (Figure 3-4)

A write amplifier channel is provided for each tape channel. Four of these channels and the circuitry typical of all write amplifiers are contained on Type 4366 Write Amplifier. The five remaining write amplifier stages are located on Type 4368 Write Amplifier. These cards plug into the masterboard, from which the necessary head connections are made. (Two of the channels on the Type 4366 Write Amplifier are not used in seven-track operation.)

Each write amplifier channel consists of an input buffer, a digitally adjustable deskewing circuit, a clocked flip-flop, and a write head driver. The skew characteristics of each read/write head are tested at the factory and the write amplifier switches are

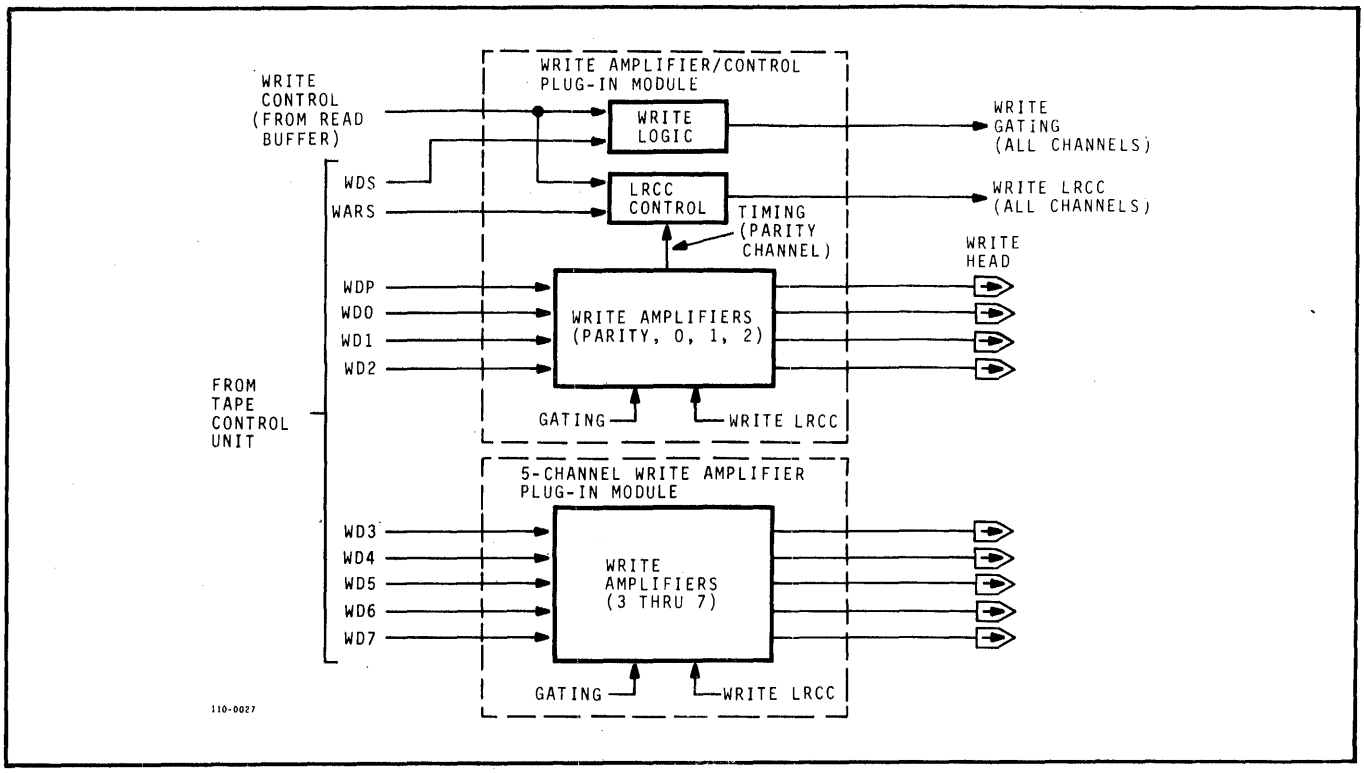


Figure 3-4. Write Data Section

set to compensate for the skew, using channel P as the fixed reference channel. (Normally the write deskew switch settings should never be changed. When a new head is installed the factory furnishes a label displaying the new deskew switch settings required to compensate for the characteristics of the new head.)

The write electronics section also includes the write data strobe buffer which clocks the write amplifier flip-flops, and a write amplifier reset circuit to clear all write amplifier flip-flops. The write amplifier reset is used to write the longitudinal redundancy check character. During a write test mode, initiated by the test panel with the recorder off line, the write electronics generates an all-1 test pattern on tape derived from a crystal controlled reference frequency F_R, supplied from the module in the read electronics. The test pattern can be used to test write deskewing as well as other functions of the data electronics.

3.8.3 READ ELECTRONICS (Figure 3-5)

The function of the read electronics is to convert the data recovered from the tape into digitized wave forms, deskew, and supply it to the interface with its respective read clock. The read electronics also detect the interrecord gap and excessive skew. The components comprising the read section include the magnetic read head, the Read Preamplifier module, Read Amplifier/Clipping Control module, and a pair of Quad Read Amplifier modules. Figure 3-5 is a functional block diagram of the read section, showing the general signal flow between the cards. A detailed circuit description of each circuit card accompanies the schematic of the card.

Low level analog signals on the order of tens of millivolts are supplied from the read head to the Read Preamplifier module. They are linearly amplified to an output voltage (adjusted by a potentiometer for each read preamplifier stage) of approximately 8 volts peak to peak during 800 cpi NRZ1 read operation. The amplified analog signals are then supplied to the nine read amplifier stages, eight of which are located on the Quad Read Amplifiers. (Channel P is directed to the Read Amplifier/Clipping Control module.) Each read amplifier stage includes a peak detection circuit, a filtering network, an output data register, and a pulse generator.

The analog signals from the preamplifier are detected only when they exceed the positive or negative clipping levels provided by the Dual P Channel/Clipping

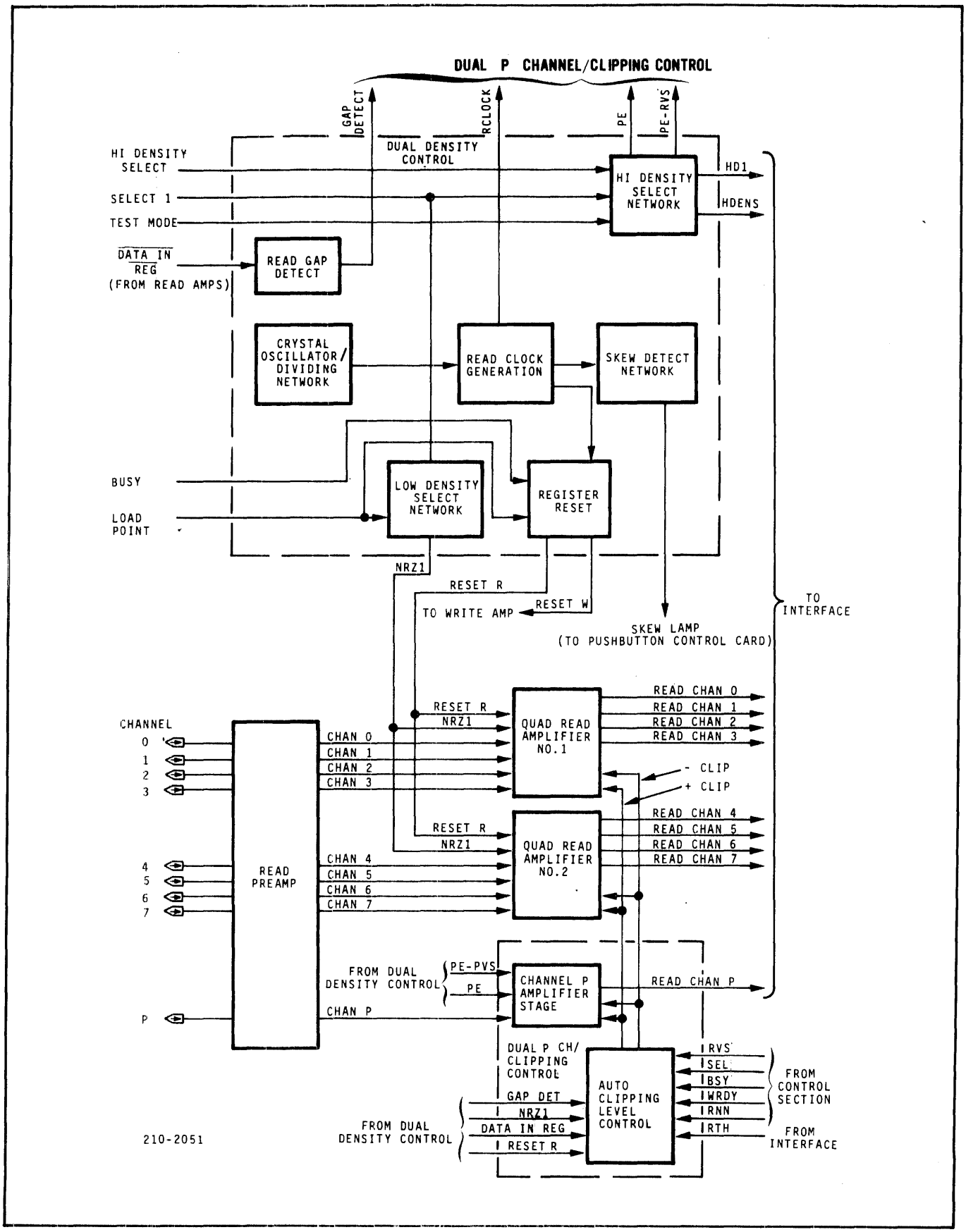


Figure 3-5. Read Data Section

Control module. They are then rectified and peak detected, with the resulting digitized wave forms containing negative-going transitions corresponding to the peaks of the input analog signals, e.g., one bits in the NRZ1 code. The digitized wave forms are supplied to a filtering network which eliminates spurious pulses between transitions. The data of each channel is then stored in a register which generates DATA IN REGISTER to the Dual Density Control.

The Dual Density Control card supplies a READ CLOCK output to clock the data registers of all nine channels simultaneously, supplying the data character to the interface.

When an error is detected, and the transport is commanded by the interface to reread a block, the read amplifier clipping levels are switched automatically by the Dual P Channel/Clipping Control module to maximize the recoverability of marginally recorded data. First the clipping levels are lowered to recover possible partial dropouts. If the block is still in error, the clipping levels are switched to higher levels to eliminate possible baseline spikes.

The Dual Density Control module contains circuitry common to all nine channels. It generates the read clock and detects excessive skew, as well as detecting the interrecord gap and providing the interlocks necessary for 800 or 1600 cpi density selection. The Dual Density Control also supplies reference frequencies to the Write Amplifier modules in order to generate the write test pattern.

In the phase encoded mode, the analog signal with its two main frequency components is amplified, peak detected, and digitized. Threshold detection for PE mode is identical to NRZ1 threshold detection, except for the absence of RCLK and RGAP outputs to the interface. The output of each channel represents its respective flux change.

3.9 DATA SECTION ADJUSTMENTS

The following adjustments are made in the data electronics section:

Adjustment	Location
Read preamplifier amplitude	Type 5728 Read Preamplifier
Skew alignment	Read/write head, write amplifiers

The adjustments are preset at the factory and should not be changed unless there is strong reason to believe that readjustment is required. The adjustment procedures are described in the circuit description of the Read Preamplifier and Write Amplifier schematics.

SECTION IV
MAINTENANCE INSTRUCTIONS

SECTION IV

MAINTENANCE INSTRUCTIONS

4.1 GENERAL

Kennedy Company tape transports are highly reliable precision instruments which will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The units require very few adjustments and these should not be performed unless there is strong reason to believe they are required. All electrical adjustments are preset at the factory and should not require readjustment except after long periods of time.

4.2 PREVENTIVE MAINTENANCE

To assure continuing trouble-free operation a preventive maintenance schedule should be kept. The items involved are few and simple but very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport so a rigid schedule applying to all machines is difficult to define. The recommended periods below apply to units in constant operation in ordinary environments. They should be modified if experience shows other periods are more suitable.

4.2.1 DAILY CHECK

Visually check the machine for cleanliness and obvious misadjustment. If items in the tape path show evidence of dirt or oxide accumulation, clean thoroughly.

4.2.2 CLEANING

All items in the tape path must be kept scrupulously clean. This is particularly true of the head and guides. The inside of the dust cover must not be allowed to accumulate dirt since transfer to the tape will cause malfunction.

In cleaning it is important to be thorough yet gentle and to avoid certain dangerous practices.

4.2.2.1 Head Cleaning

Oxide or dirt accumulations on the head surfaces are removed using a mild organic solvent and a swab. Q tips are convenient for this use but must be used with caution. Be sure the wooden portion does not contact head surfaces.

An ideal solvent is 1.1.1 trichlorothane contained in Kennedy K21 maintenance kit. However, others such as isopropyl alcohol will do. DO NOT USE: acetone or lacquer thinner, aerosol spray cans, or rubbing alcohol.

Do not use an excess of any solvent, and be extremely careful not to allow solvent to penetrate ball bearings of idler rollers, capstan motor, etc., since it will destroy their lubrication.

4.2.2.2 Tape Path Cleaning

CAUTION

Do not attempt to clean the mylar sensors in columns or allow solvent to contact the element. Dirt and oxide will not impede the sensor operation.

Other items in the tape path should be cleaned at the same time as the magnetic head. These include columns, idler rollers, tape guides, capstan, and tape cleaner surface.

The techniques are similar to those outlined above for head cleaning.

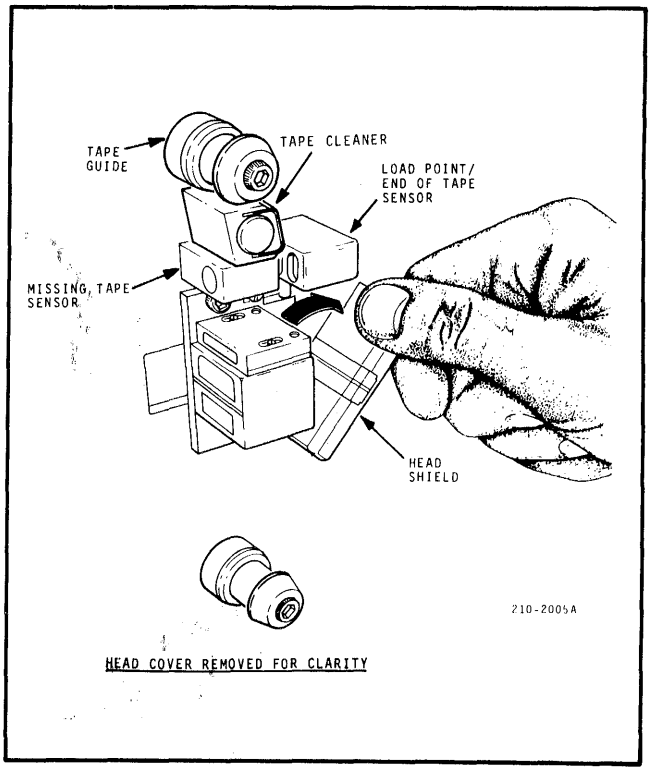


Figure 4-1. Opening of Head Shield

4.2.2.3 Other Cleaning

A vacuum cleaner is recommended for removing accumulations of dust inside the dust cover or elsewhere in the unit. Compressed air may be used if caution is exercised to avoid blowing dirt into bearings. Antistatic cleaners are available for cleaning the plexiglass dust cover window.

4.2.3 VISUAL CHECK

Check visually to determine if all appears to be right with the machine. It is helpful to run tape forward and reverse observing smooth tape motion, proper vacuum operation, etc.

4.3 ROUTINE ADJUSTMENT

There are no routine adjustments. Need for adjustment will be manifest if malfunction occurs. Under normal circumstances adjustment will be more likely to cause trouble than prevent it.

4.4 LUBRICATION

No bearing lubrication is required. All bearings are lubricated for life and introduction of oil may destroy their lubrication.

4.5 WEAR

Magnetic tape is an abrasive and in time wear will be noted on items over which the oxide surface slides.

4.5.1 HEAD WEAR

Head wear is generally signaled by an increase in error rate. Confirmation is a sizable increase in output voltage at the read head as measured at the read preamplifier. When the head becomes worn it must be replaced. Head replacement procedure is described in paragraph 4.24.5.

Worn heads usually can be resurfaced at least once if returned to the factory. This is more economical than replacement with a new head. Consult Section V for details of head return.

4.5.2 GUIDE WEAR

Guides wear principally at the point of contact with the front guide surface. Although guides are ceramic, in time grooves will appear. Since guides are symmetrical it is only necessary to loosen the guide mounting screw, rotate the guide, and tighten to present an unworn surface to the tape.

4.5.3 REEL HUB WEAR

Quick release hubs are adjustable to assure a firm clamping action. They are designed to make it impossible to mount a reel in a wrong or cocked position. If the locking action should become weak, the hub may be adjusted as described in paragraph 4.8. O-ring clamps used in the hub may tend to hang up after long periods of use. This can be corrected as follows:

a. Remove O-ring from hub.

b. Clean thoroughly with mild solvent.

c. Lubricate ring with silicone grease. Wipe off as thoroughly as possible, leaving a light lubricating film.

d. Snap O-ring back in place.

4.6 PERIODIC INSPECTION

At regular intervals, approximately every two months, it is advisable to make a more thorough check of machine operating parameters. This will ensure that no progressive degradation will go unnoticed. The test panel facilitates making these checks, allowing control of tape motion off line for test purposes as well as providing useful indicators and test signals. The test panel connector plugs into a connector on the control electronics. It does not require that interface cables be disconnected. Using the test panel or other appropriate means, the following should be checked periodically.

Tape speed
Ramp times
Read level
Skew
Photosensor adjustment
Capstan and reel servo adjustment

Procedures for checking these and other items are given in this section and a suggested sequence of adjustments is shown in Table 4-1.

4.7 TEST PANEL USE

4.7.1 TEST PANEL USE

The test panel is standard equipment in the Model 9100. Located next to the control panel, it is used to perform tests and adjustments on the tape transport while it is off line. This eliminates the need for many external test fixtures as well as saving valuable computer time.

The function of each test panel control and indicator is provided in Figure 4-2.

Basically, the test panel is used for making skew, ramp time and servo adjustments. Besides providing

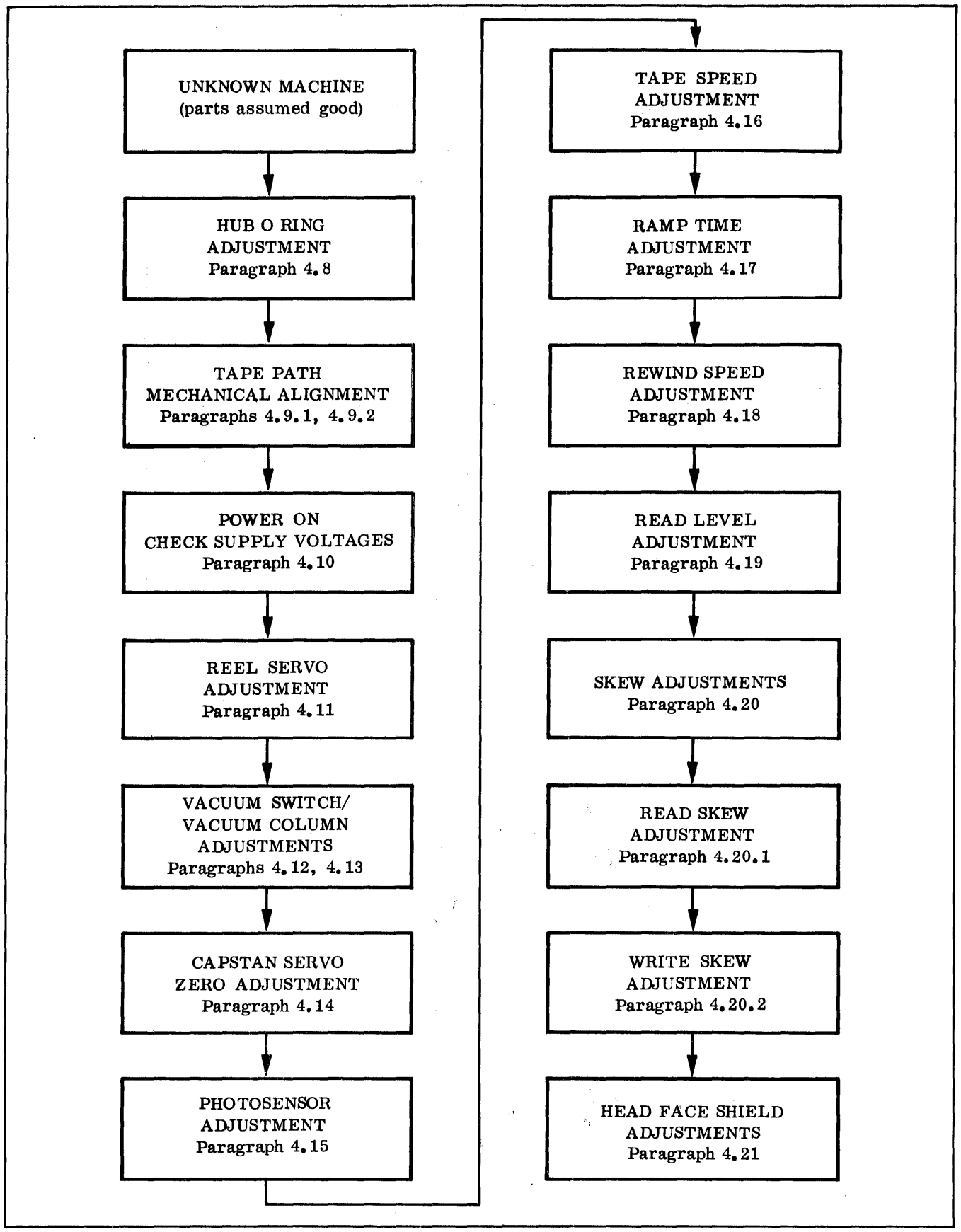
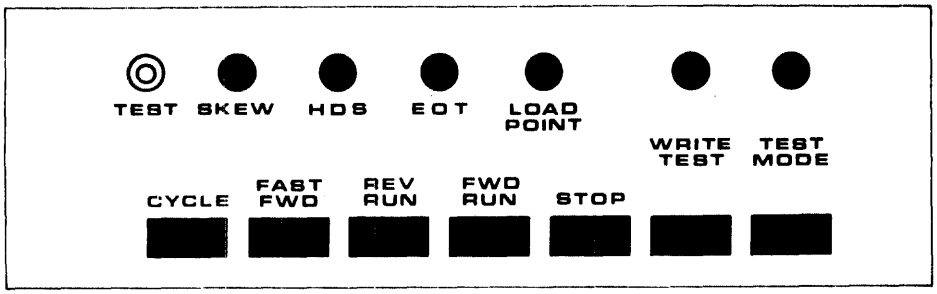


Table 4-1. Adjustment Sequence



NOTE

Tape transport must be off line and STOP pushbutton depressed before test panel can become functional.

TEST point and SKEW indicator. Indicator lights if tape skew exceeds the appropriate skew (read or write) gate setting. An oscilloscope test point is available for monitoring skew gate timing.

HDS indicator. Indicates that high density mode has been selected.

EOT indicator. Indicates when tape has reached or passed end of tape.

LOAD POINT indicator. Indicates when tape is at load point.

CYCLE pushbutton. An interlocked pushbutton which runs tape in alternating forward and reverse modes. Useful for making ramp or vacuum sensor adjustments. Depressing STOP pushbutton terminates this operation.

FAST FORWARD pushbutton. An interlocked pushbutton switch that allows tape unit to run forward at fast speed. Depressing STOP pushbutton or EOT marker terminates this operation.

REVERSE RUN pushbutton. An interlocked pushbutton switch that allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton or load point marker terminates this operation.

FORWARD RUN pushbutton. An interlocked pushbutton switch that allows tape unit to proceed forward at normal speed. Depressing STOP pushbutton or EOT marker terminates this operation.

STOP pushbutton. An interlocked pushbutton switch that terminates all tape motion.

WRITE TEST pushbutton and indicator. A momentary pushbutton which programs 1's to be written on all channels to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator remains illuminated while unit is in this mode.

TEST MODE pushbutton and indicator. A momentary pushbutton selects test mode and activates test panel. When indicator is illuminated, test panel is active. (Tape unit must be off line and STOP pushbutton depressed before test panel will function.)

Figure 4-2. Test Panel Controls and Indicators

complete control over tape speed and direction, it can initiate a write test by generating a crystal controlled all-1 test pattern on the tape. The test panel also contains indicator lamps which illuminate when there is excessive skew, high density is selected, end of tape or load point is reached, or a write test is being performed. (The skew test indicates proper alignment of the read/write head.)

The test panel contains a CYCLE pushbutton. When pressed, it runs the tape forward and reverse continusously to facilitate ramp time and reel servo adjustments.

4.7.2 OPERATION

Pressing the TEST MODE pushbutton activates the test panel if the Model 9100 is off line with the STOP pushbutton on the control panel depressed. The test panel is turned off by either pressing the TEST MODE pushbutton to release it or by pressing the ON LINE pushbutton on the control panel.

4.8 HUB O RING ADJUSTMENT (FIG. 4-3.)

Object: to lock tape reel firmly to the hub.

If the tape reel is loose with hub locked, check the condition of the neoprene O-ring. This O-ring expands when the locking latch is depressed to secure reel to hub.

4.8.1 If the O-ring is not worn, but the reel won't seat firmly:

a. Loosen hub setscrew until the inner hub turns freely.

b. With hub latch up, rotate inner hub clockwise while restraining the outer hub. This will exert more pressure on the O-ring when the latch is depressed.

c. Place reel on hub and lock latch to determine whether more or less tightening is required.

NOTE

There are several holes in the bottom of the outer hub to accommodate the hub setscrew. Therefore, after adjustent is correct, the hub must be turned slightly until the setscrew fits into one of these holes.

d. After the correct setting is found, retighten the hub setscrew.

4.8.2 If O-ring requires replacement:

a. Loosen setscrew until inner hub turns freely.

b. Unscrew inner hub from hub assembly.

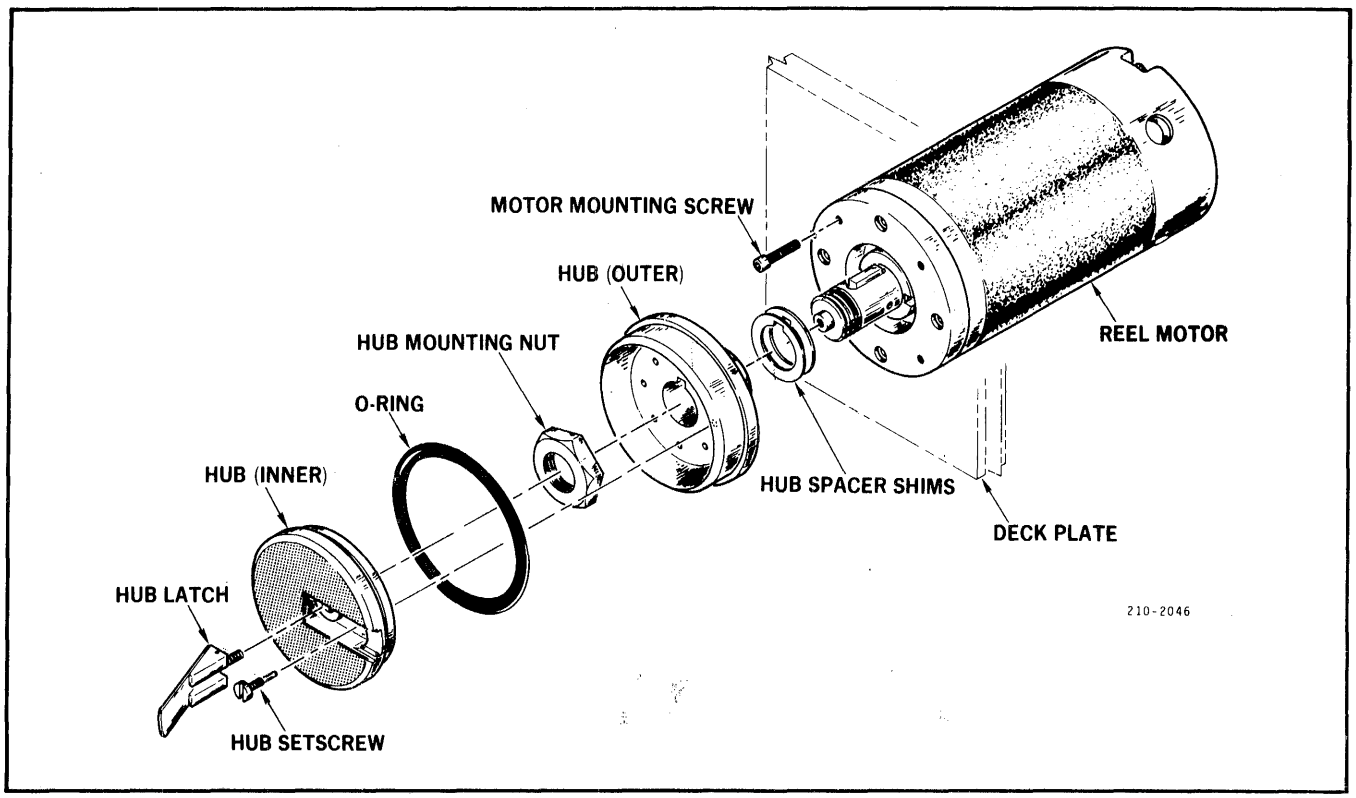


Figure 4-3. Hub O-Ring Adjustment

c. Replace worn O-ring with new O-ring (Kennedy PN 125-0030-006). Prior to installation the new O-ring should be lubricated with silicone grease and wiped, leaving a light lubricating film.

d. Replace inner hub and readjust O-ring pressure according to paragraph 4.8.1.

4.9 TAPE PATH MECHANICAL ALIGNMENT

4.9.1 REEL CLEARANCE ADJUSTMENT/ HUB REPLACEMENT (Figures 4-3, 4-4)

Object: To maintain the proper tape path across the top of the hub reel mounting flange and the unpainted area on the deck plate (see Figure 4-3). This measurement should be made with a vernier caliper. A special shim kit, Kennedy PN 198-0100-001) is available for spacing the hub assembly properly.

Procedure:

a. Loosen hub setscrew and unscrew inner hub.

b. Insert special spanner wrench (Kennedy PN 154-0042-001) into setscrew holes to stabilize hub. Then remove the hub mounting nut with a socket wrench. Slide remaining portion of the hub assembly off the motor shaft.

c. Add or remove shims as required to obtain 0.328 inch distance from reel flange to the unpainted portion of the deck plate.

d. Reassemble hub assembly. Tighten nut to 20 +/-5 in./lb torque.

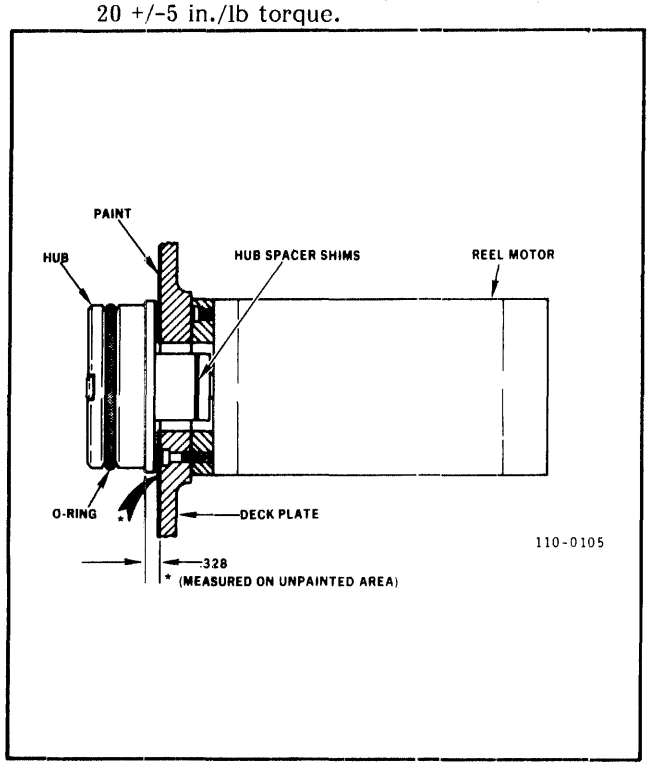


Figure 4-4. Reel Hub Assembly

4.9.2 CAPSTAN PARALLELISM

The tape should not travel laterally (ride in or out) on the capstan in the forward or reverse mode. To check, observe the tape on the capstan while the machine is in CYCLE mode.

Adjustment Procedure

Object: to eliminate any lateral tape movement on the capstan during operation.

a. With tape stopped, loosen capstan screws (see Figure 4-5).

b. Back off both capstan adjustment setscrews until they no longer touch the capstan motor mounting plate.

c. Retighten both capstan adjustment setscrews until they press lightly against the capstan motor mounting plate.

d. Place machine in CYCLE test mode. Observe tape position on the capstan. If tape moves OUTWARD, tighten both adjustment screws equally until OUTWARD lateral movement ceases. If tape moves INWARD, loosen both adjustment screws equally until inward lateral movement ceases.

e. Retighten capstan setscrews and recheck. If lateral tape movement has been eliminated, adjustment is complete. Otherwise, repeat adjustment procedure.

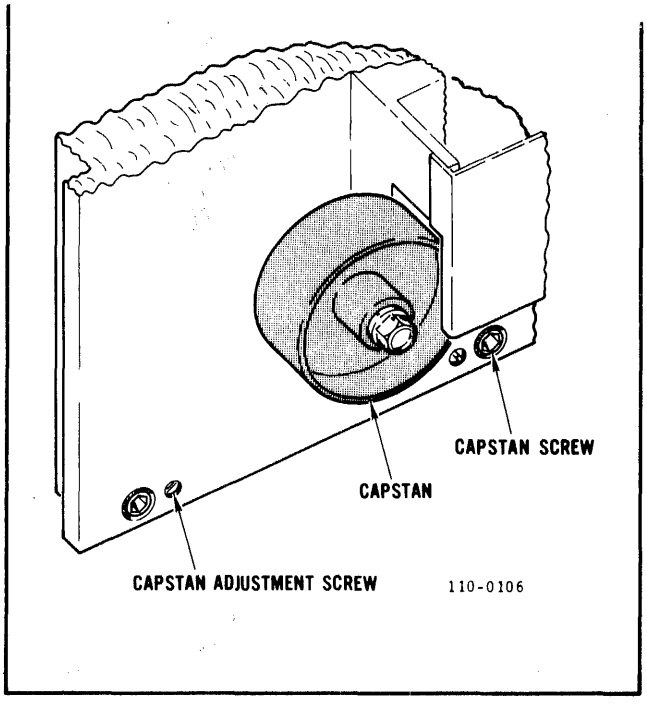


Figure 4-5. Capstan Parallelism Adjustment

4.10 CHECKING SUPPLY VOLTAGES

Here is a list of supply voltages and their test points in the Model 9100.

+24v - case of Q27, Q28, Q31, Q32, Q35 (MJ802), heatsink (+26v under light load)

-24v - case of Q29, Q30, Q33, Q34, Q36 (MJ4502), heatsink (-26v under light load)

+10v (+0.5,-0.2v) Sensor Amplifier/Driver, test point A

-10v (+/-0.8) Sensor Amplifier/Driver, test point B

+5v (+/-0.25) Sensor Amplifier/Driver, test point C

NOTE

(1) Use chassis ground when making voltage measurements.

(2) Make certain power is switched OFF when removing or replacing circuit boards.

If the voltages are not correct, the trouble is either in the power supply or due to an overload on the power supply. Removing each circuit board while monitoring supply voltage can help isolate the cause of any overload. Also, be sure to check the power supply for burned, open, or shorted components. The power supply is protected against short circuits in its regulated voltage circuitry.

4.11 REEL SERVO ADJUSTMENT

4.11.1 CENTERING ADJUSTMENT
(R10, Supply Servo; R69, Takeup Servo)

Object: to center tape in both vacuum columns when tape is stopped.

NOTE

Tape loops must be in both vacuum columns during adjustment.

Procedure:

a. Load tape and advance it to load point.

b. Adjust R10 on the servo preamp until tape loop is center in the supply vacuum column. (Note: While adjusting, make certain tape loops remain within both vacuum columns.)

c. Repeat steps a and b to adjust R69, the takeup servo zero adjustment. When completed, both reels should be stationary, with the tape centered in both vacuum columns.

4.11.2 GAIN ADJUSTMENTS
(R24, Supply; R83, Takeup)

Object: to eliminate any overshoot of the tape loop in the vacuum column when tape changes direction.

Procedure:

a. Connect a zero-centered voltmeter to test point A on the Servo Preamplifier board. Use chassis ground.

b. Turn power on; advance tape to load point.

c. Rotate supply reel to permit tape to rise to top of the supply vacuum column. Voltage at test point A should be approximately +2 vdc.

d. Rotate supply reel to pull tape almost out of the supply vacuum column. Voltage at test point A should be nominally -2 vdc.

e. Press TEST MODE and CYCLE pushbuttons on test panel. Tape will continuously alternate between forward and reverse. Check for overshoot when the tape loop changes position as the tape changes direction. If overshoot occurs, adjust R24 until it is eliminated.

f. Repeat steps b, c, and d to check and adjust R83, the takeup reel servo gain control.

4.12 VACUUM SWITCH

The vacuum switch is located in the rear of the deck assembly in the upper right hand corner on the column plenum cover. This switch is a safety device to prevent possible tape breakage. It will operate to shut off the tape transport whenever the vacuum pressure within either vacuum column drops below a predetermined level. The objective of adjustment is to determine and set the pressure level at which the vacuum switch will actuate.

Equipment required: Kennedy Vacuum Test Box, Kennedy Part No. 154-0041-001 or equivalent.

a. Connect vacuum gauge and ohmmeter to the vacuum switch as shown in Figure 4-6. To do this, one end of the vacuum switch hose must be detached and connected to the vacuum test box "T" fitting. Then the hose on the opposite end of the "T" fitting is attached to the vacated hose fitting on the vacuum switch. Also, detach the green/white (+) wire from its terminal on the vacuum switch. Connect it to chassis ground prior to attaching the ohmmeter to the positive terminal on the vacuum switch.

b. With machine on and a tape at load point, cover the bleed hole (see Figure 4-6). This gives maximum vacuum pressure, which should measure between 17 and 21 inches of water at sea level, or 15 to 19 inches of water at 4000 feet altitude.

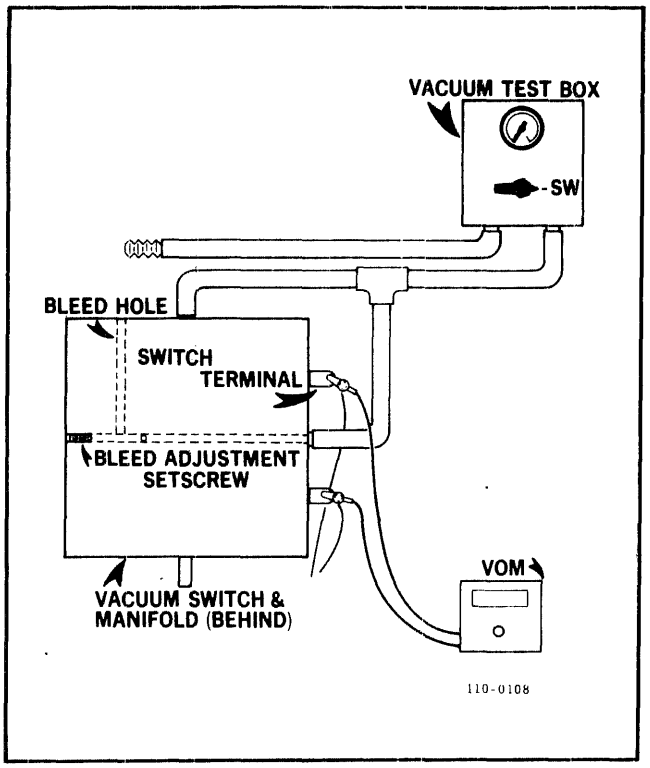


Figure 4-6. Vacuum Switch Adjustment

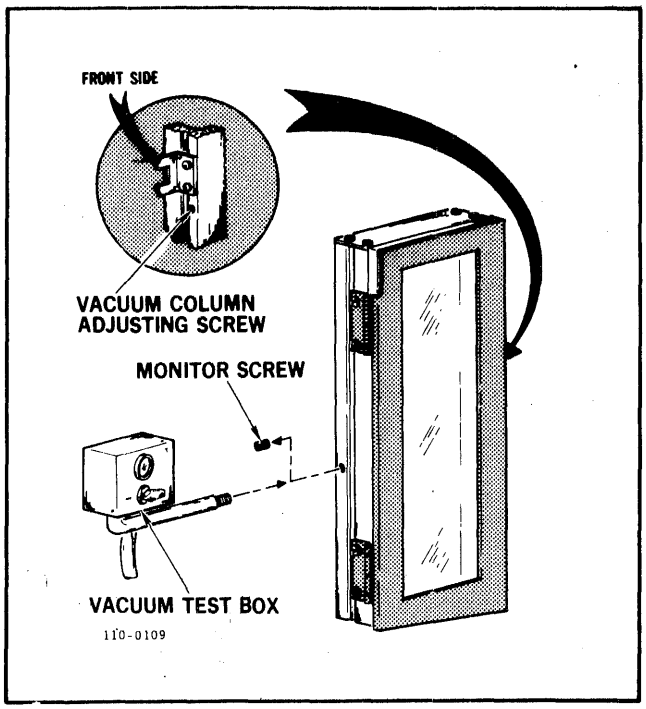


Figure 4-7. Vacuum Column Adjustment

c. Uncover bleed hole. Adjust bleed adjustment screw until switch closes. (Ohmmeter will indicate 0 ohm). Pressure should be between 10 inches and 14 inches of water.

d. Tighten bleed adjustment screw to obtain pressure reading which is 4 inches higher than pressure obtained in step c. Adjustment is complete.

4.13 VACUUM COLUMN ADJUSTMENT

Equipment required: Kennedy Vacuum Test Box, Kennedy Part No. 154-0041-001 or equivalent.

Objective: to develop one-half to two-thirds of vacuum present at the vacuum sensor. This adjustment should follow, not precede,the vacuum switch adjustment.

Using an Allen wrench, unscrew the 6/32 Allen screw from the left hand side of the supply vacuum column. Install the threaded vacuum hose fitting and vacuum guage in the monitor screw hole (see Figure 4-7).

b. With the machine turned on and a tape at load point, measure the vacuum. (Tape loops must be present in both vacuum columns to obtain accurate readings). Vacuum should be one-half to two-thirds of the final measurement obtained in step b of the vacuum switch adjustment. (At sea level, pressure should measure between 10 inches and 14 inches of water. At 4000 feet, pressure should measure between 9 inches and 12.5 inches of water.)

c. If a correct vacuum reading is not obtained, adjust the appropriate vacuum column adjustment screw shown in Figure 4-7 as required.

d. Detach the vacuum test box and replace the monitor screw. Repeat adjustment procedure on the takeup vacuum column.

4.14 CAPSTAN ZERO ADJUSTMENT

The capstan should not move when the tape is stopped. A zero adjustment is provided on the servo preamplifier to remove the effects of component tolerances.

Procedure:

a. If capstan rotates slowly when tape is stopped, grasp capstan with tape loaded and turn first clockwise, then counterclockwise. Capstan will show a reluctance to turn. If turned gently a small dead zone can be detected. This dead zone should be approximately the same for either direction of motion. If adjustment is required, connect a voltmeter or scope probe to test point D of the servo module.

b. Advance tape to load point.

c. Rotate zero adjust pot R139 to bring measured voltage to zero.

4.15 EOT/BOT SENSOR ADJUSTMENT

Infrared emitting diodes and sensor transistors are used to detect the EOT and BOT markers. These semiconductor elements display long term stability and high resistance to ambient light conditions. The sensor amplifier bias has to be initially adjusted to balance the input to the amplifier stages. Once this adjustment is performed in the factory there is usually no need for readjustment unless the amplifier module or the sensing elements are replaced. When readjustment is required, follow the procedure outlined below.

a. Place blank tape over the sensors.

b. Connect a dc voltmeter between test points E and F on the Sensor Amplifier/Driver module.

NOTE

These test points are both off ground. If an oscilloscope is used to measure the voltage instead of a voltmeter, it must be isolated from ground, or the two inputs should be added with one channel inverted.

c. Adjust potentiometer R16 for 0v between test points E and F.

4.16 TAPE SPEED ADJUSTMENT

Normal tape speed is controlled by R14 on the ramp generator. This control is set at the factory and normally will not require adjustment. There are two methods for checking speed.

Strobe disk method

a. Mount strobe disk on the capstan (Kennedy PN 291-5572-001, -69 Hz type; 291-5572-002, -50 Hz type). Position a fluorescent light a few feet from the capstan.

b. With tape running at normal speed, adjust R14 on ramp generator for a steady strobe disk pattern if necessary. If R14 must be adjusted, check read preamplifier gain settings (paragraph 4.19).

Skewmaster Tape Method

a. Mount skewmaster tape on machine as described in read skew adjustment.

b. Observe waveform at one preamplifier test point.

c. Set the time for one complete sine wave cycle (two bits) at a value determined by

$$\text{time in ms} = 100x \frac{25}{\text{speed (ips)}}$$

by adjusting R14. Note that the waveform will not be entirely stationary on the scope owing to small rapid speed variations. These should be visually averaged.

d. If speed adjustment was made check read preamp gain settings (paragraph 4.19).

4.17 START/STOP RAMP TIME ADJUSTMENT

To assure accurate tape gap generation, tape must linearly accelerate to normal running speed and linearly decelerate to stop. The start and stop ramp voltages required for this linear movement are controlled by ramp generator potentiometers R3 and R4, respectively. Ramp timing is the same for both forward and reverse modes.

To adjust start and stop ramp timing:

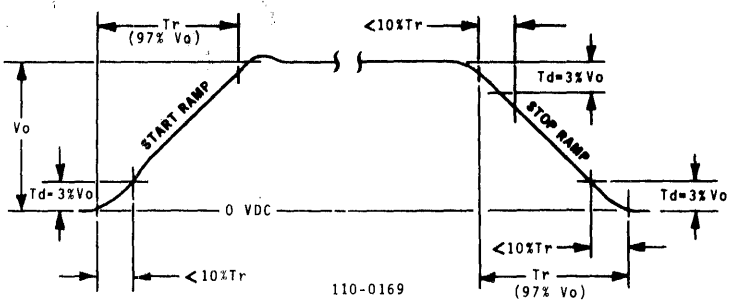
Procedure

a. Connect channel 1 of oscilloscope to output of the Ramp Generator board at test point A.

b. Connect oscilloscope's external trigger input to pin C (SFC/) of the Interface PC board, using an extender board.

c. From computer or tape transport exerciser issue a series of Synchronous Forward Commands (SFC/) to the transport. Each SFC/ transition should last approximately two ramp times. (Compute ramp time Tr formula below, then multiply results by two.) Tr is measured in milliseconds and its tolerance equals +0%, -5%, where:

$$\text{Tr } (-5\% \ +0\%) = \frac{375}{\text{tape speed}}$$



NOTES

1. Tr equals 97% of the total ramp voltage, Vo.

2. Ramp voltage should be at ground at beginning of ramp.

d. To adjust start ramp, sync oscilloscope on leading edge of SFC/ input signal and observe waveform.

e. Compare values from use of formula with those read from oscilloscope presentation.

f. Adjust R3 to obtain correct start ramp. Use a nonmetallic adjustment tool.

g. After start ramp adjustment, make certain Td, which is defined as 3% of ramp voltage Vo, is less than 10% of ramp time Tr.

h. Perform steps d through g to adjust stop ramp time. Adjust R4 and sync oscilloscope on trailing edge of SFC/.

i. After start ramp adjustment, make certain Td is less than 10% of ramp time Tr. Adjustment is complete.

4.18 REWIND SPEED

Rewind speed is not adjustable. It is determined by fixed values on the Ramp Generator card.

4.19 READ LEVEL ADJUSTMENT

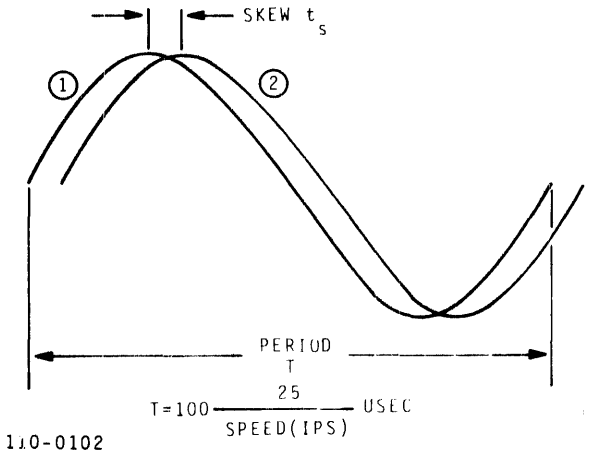
This adjustment sets gain of the Read Preamplifiers to the correct level. Too much gain will introduce noise and too little will aggravate dropouts.

a. Load a reel of scratch tape on the transport, write enable ring in place.

b. Select TEST MODE.

c. Select WRITE TEST, FORWARD RUN.

d. Observe waveforms at test point for each channel on Read Preamplifier.



Skew Adjustment Waveforms

e. Measure peak-to-peak amplitude and set for 8 +/-0.5 volts using channel gain control on Read Preamplifier. Repeat for each channel. Note that the read level is about 10 percent higher when the machine is operating in read-after-write mode than when in the read mode. This effect is caused by small unavoidable magnetic remanence in the write head and the erase head. Skewmaster tapes should NOT be used as amplitude reference for this reason.

4.20 SKEW ADJUSTMENT

Skew is one of the most important parameters in reading NRZ1 data. Since, in a read-after-write head, data is read with one gap and written with a second gap, read and write skews are in general different and must be compensated separately. Only when both are properly set can the machine be said to be deskewed. In the Model 9100 the read gap is deskewed mechanically while digitally controlled delays are used to deskew the write gap.

4.20.1 READ SKEW ADJUSTMENT

When deskewing the read gap, the head is mechanically tilted to have its gap at an exact right angle to the tape. This is accomplished using a skewmaster tape (see maintenance tools).

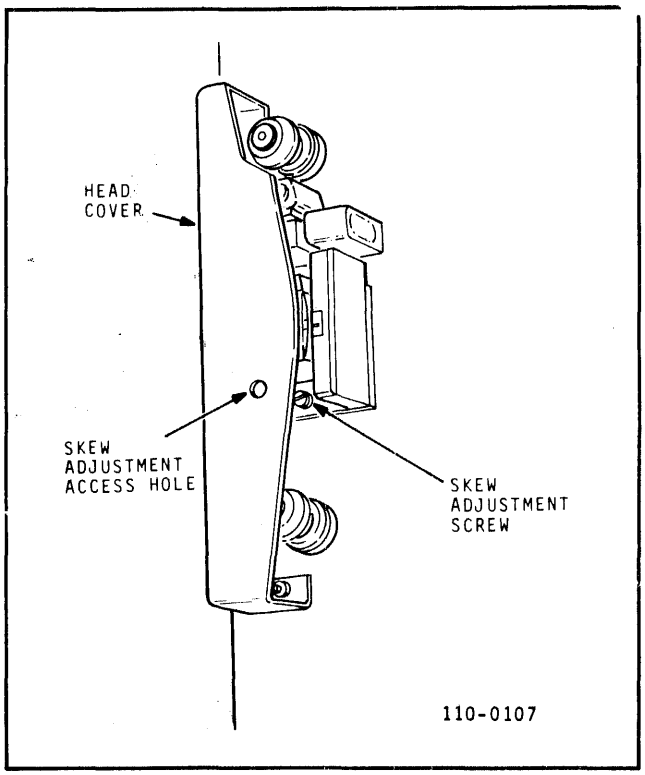


Figure 4-8. Head Skew Adjustment

a. Load skewmaster on transport. Be sure write enable ring is missing.

b. Press TEST MODE button.

c. Press FORWARD RUN.

d. Observe SKEW indicator and adjust skew adjusting screw on the head mounting plate (Figure 4-8) until indicator does not come on.

For greater precision, a scope probe may be connected to the TEST terminal on the test panel. At this point the pattern will be a grouping of nine pulses as each channel "reports in." At optimum skew setting, these pulses occupy the minimum spread.

4.20.2 WRITE SKEW ADJUSTMENT

The Model 9100 features a unique digital deskewing arrangement for deskewing the write head. Since write-read skew is a function of head geometry and does not change, write deskewing delays are determined at the factory and each head has a deskewing chart showing the appropriate write amplifier deskew switch settings for that head. All channels are referenced to the P channel (or C in seven-track units).

If for some reason it is necessary to deskew the write head in the field the procedure is as follows:

a. Proceed as in read level adjustment, paragraph 4.19.

b. Connect a dual channel scope channel 1 to the P channel test point on the Read Preamplifier. Set alternate sweep, trigger channel 1 internal.

c. Connect scope channel 2 to test point for tape channel 5 and observe pattern. Set sweep speed to display one half sine wave cycle.

d. Observe separation of peaks displayed. Note that because of small variations in speed and skew the pattern will not be entirely stationary.

e. Set skew switch for channel 5 for minimum peak separation.

f. Repeat for each of the remaining seven channels.

4.21 HEAD FACE SHIELD ADJUSTMENT

A shield is located over the magnetic head surface to reduce write-read crosstalk. Its spacing, determined by a spring stop, is important. The spring stop is adjustable as follows:

a. Loosen stop screw with tape removed from machine.

b. Insert three thicknesses of tape (0.006 inch) between shield surface and top surface of head. Do not use feeler gauges, since they may scratch the head surface.

c. Press shield against tape firmly and tighten stop screw.

d. Remove tape pieces by lifting shield.

4.22 BLOWER MOTOR BELT TENSION ADJUSTMENT

Objective: To adjust tension of blower motor belt to approximately 1/4 inch (approximately 6 mm) of deflection. (See Figure 4-9.)

Equipment needed: Spring scale (0-1000 gm), 150 mm (6 inch) ruler.

Procedure:

a. Secure primary power to unit.

b. Remove rear access cover located above primary input power connection.

c. Using a pencil, mark vertical position of drive belt midpoint.

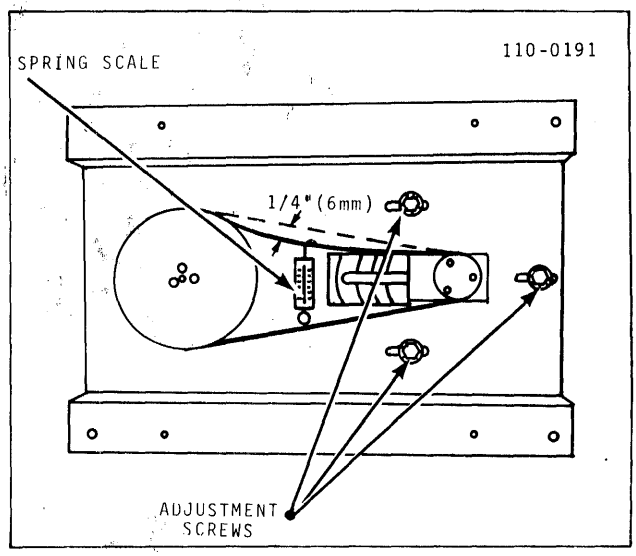


Figure 4-9. Blower Motor Belt Adjustment

d. Attach spring scale to drive belt midpoint and apply 1000 gm tension.

e. Again mark vertical position of drive belt midpoint.

f. Using the ruler, measure the distance between the two midpoint positions. Measurement should be approximately 1/4 inch (6 mm).

g. If deflection is incorrect, loosen adjustment nuts and move blower to the right to increase tension or to the left to decrease tension. Retighten nuts and repeat steps e through f.

h. After adjustment is completed and verified, replace access cover.

4.23 TROUBLESHOOTING

Troubles that can arise in the Model 9100 can usually by classified as either mechanical or electrical but often the classification may be confusing because a basically mechanical problem can cause what appears to be an electronic malfunction and vice versa. In any case the problem should be thoroughly analyzed before adjustments are made.

Electronic troubleshooting is greatly facilitated by the modular construction: a new card may be substituted and the effect observed. Most difficult, of course, are subtle problems and those of an intermittent nature.

Visualizing solution (Magnasee) is useful under certain conditions for troubleshooting. At high densities the data cannot be satisfactorily resolved but such problems as a dead track, improper gap length, etc., can be isolated rapidly by its use.

If a tape has had visualizing solution applied to it DO NOT reuse that portion of the tape as it will contaminate the head. Cut the visualized portion off and discard.

To use visualizing solution, shake the can thoroughly, remove top and pass portion to be visualized through the solution. Snap the tape vigorously to remove excess solution and let dry. Iron powder will be left in magnetized areas. This can be picked off using Scotch tape and applied to a sheet of paper for permanent record.

4.23.1 HIGH ERROR RATE

Usually the more difficult problems involve a higher than permissible error rate for which, at first glance, there is no obvious reason. If operating properly with good tape the transport should make very few errors in writing and if rewriting is included in the program it should make no read errors.

Useful clues are:

a. In what mode - read or write - are many errors occurring?

b. At what point in the block does the error occur?

c. What is the nature of the error: VRC, CRC, LRC?

d. Are the errors pattern related?

e. Do errors occur only on certain sets of commands?

The first thing to be done is to inspect head and other items in the tape path for dirt accumulations. Be sure everything is clean. Check the tape being used and try a new reel if tape is doubtful. Check interface connections for broken wires or bad contracts. Table 4-2 is a troubleshooting chart concerned with high error rate.

4.23.2 COMPATABILITY

Model 9100 accepts and produces tapes conforming to the ANSI standards. Occasionally compatibility problems can arise:

a. Tapes written by and acceptable to the 9100 are not acceptable to another transport.

b. Foreign tapes cannot be read by the 9100 but its own tapes can be.

Three items may be involved: skew, speed, ramp times. These should be checked as described in the adjustment procedures.

4.23.3 OTHER MALFUNCTIONS

Normal trouble shooting procedures are involved in finding electronic malfunctions. The first things to check are the supply voltages:

+/-24 volts nominal unregulated will normally be about +/-26 volts under light load.

+/-10 volts +/-0.5 volt

+5 volts +/-0.25 volt

Convenient test points for measuring supply voltages are:

+24v - case of Q9 (MJ802) on heatsink
-24v - case of Q10 (MJ4502) on heatsink
+10v - Sensor Amplifier/Driver TPA
-10v - Sensor Amplifier/Driver TPB
+5v - Sensor Amplifier/Driver TPC

Observed: High error rate — clean machine, good tape

Symptom	Possible Cause	Indication	Action	Reference
Continuous errors, every block (read mode)	Broken connection to interface or internally	Continuity	Correct connection.	
	Bad preamp channel	No output at test point on write test	Replace preamp.	
	Bad quad read amp channel	No data at test point	Replace quad read amplifier.	
	Tape speed grossly wrong	Visual or skewmaster	Adjust speed.	4.16
	Bad head channel	No output at preamp test point on write test	Replace head.	4.23.5
Continuous errors, write mode only	Broken connection on write data or WDS lines	Continuity	Correct connection.	
	Bad write amp channel	No signal in write test mode	Replace write amp.	
Frequent write errors, few or no read errors	Write-read crosstalk	Noisy signal at preamp test point	Check preamp gain. Check face shield spacing.	4.19 4.21
Frequent CRC, LRC errors, no VRC errors	Wrong CRC generation in interface	Wrong data at input	Correct interface.	
Read or write errors only at start of block	Ramp time wrong	Read signals appear before ramp is complete	Adjust ramp time.	4.17
Read errors on long blocks only	Tape path misaligned	Tape bears heavily on one guide surface	Mechanical alignment.	4.9
Pattern related errors	Write-read crosstalk	Noisy signal at preamp test point	Check preamp gain. Check face shield spacing.	4.19

Table 4-2. Troubleshooting

Control Malfunctions

Symptom	Possible Cause	Location	Action	Reference
Tape breakage or aborted load	Misadjusted reel servo(s) on Servo Preamplifier module	Side panel	Readjust.	4.11
LOAD pushbutton activates servos when pressed but does not hold	Broken tape signal clears LOAD flip-flop			
	a. Sensor Amplifier/Driver module	Card cage	Replace module.	
	b. Pushbutton Control module	Card cage	Replace module.	
	c. Photosensor (BKN) malfunction	Deck	Replace sensor.	4.23.6
	d. Sequencer module	Panel	Replace module.	
	e. Vacuum switch and/or vacuum blower	Deck, blower	Fix.	
Tape feeds forward after load point marker should be sensed and is rewound to physical end of tape	a. Marker strip missing from tape	Tape	Apply reflective strip.	
	b. Misadjustment of photosensor on Sensor Amplifier/Driver module	Card cage	Adjust photosensor.	4.15
No EOT signal	Same as load point above but for EOT			4.15
REWIND pushbutton inoperative	Logic malfunction, Pushbutton Control module, Sequence module	Card cage, side panel	Replace module.	
Rewind does not stop at LP but continues until tape is wound off reel	a. Same as above			
	b. Photosensor adjustment wrong, Sensor Amplifier/Driver module	Card cage	Adjust photosensor.	4.15
Reels rotate uncontrolled when power is turned on with tape in both vacuum columns	a. Servo preamplifier malfunction	Side panel	Remove preamp. If reels stop, replace preamplifier module.	
	b. Servo power amplifier (bad power transistors)	Heatsink	Replace heatsink assembly or locate and replace bad power transistors.	
Tape moves erratically, slips on capstan	Head face shield touching tape	Deck	Adjust face shield setting.	4.21
Capstan turns slowly when it should be stopped	Capstan zero adjustment, Servo Preamplifier module	Side panel	Adjust for zero.	4.14

Table 4-3. Troubleshooting

Voltages are measured to chassis (ground). Plus or minus 24 volts will increase to +/-32 volts when speed is greater than 150 ips.

NOTE

TURN POWER OFF WHEN REMOVING OR INSERTING CARDS.

If the voltages are not correct the trouble is either in the power supply or in the fact that the malfunction is loading the supply excessively. Pulling cards from their sockets can help isolate an overloaded condition. The power supply is short-circuit protected on the regulated voltages. Assuming the voltages are correct, Table 4-3 should help in isolating malfunctions.

4.24 PARTS REPLACEMENT

In most instances assembly methods for parts replacement are obvious. Electronic parts are nearly all on plug-in modules. Items in the tape path may require machine realignment if replaced. If only one item is replaced at a time the complete alignment procedure usually may be avoided. Examples follow.

4.24.1 HUB REPLACEMENT
(Refer to paragraph 4.9.1)

4.24.2 O-RING REPLACEMENT
(Refer to paragraph 4.8.2)

4.24.3 REEL MOTOR REPLACEMENT
(Kennedy PN 190-5698-001)

a. To expose motor mounting screws, remove the hub assembly as described in paragraph 4.9.1.

b. Using a 5/32 inch Allen wrench, unscrew the four motor mounting screws and lift the reel motor out of the chassis.

4.24.4 CAPSTAN MOTOR REPLACEMENT
(Kennedy Part No. 198-5823-001)

Procedure:

a. Detach capstan connecting cable.

b. After removing mounting nut, detach capstan with capstan puller (Kennedy Part No. 154-0043-001).

c. Using a 5/32 inch Allen wrench, remove the four capstan motor mounting screws and lift the capstan motor out of the chassis.

4.24.5 MAGNETIC HEAD REPLACEMENT

Replacement heads are supplied as complete assemblies together with mounting plate. A write deskewing chart is supplied with each head.

a. Remove head cover.

b. Unplug head connectors.

c. Remove head mounting screw and remove head, passing connectors through the panel hole provided.

d. Be sure adjusting screw on replacement head is almost completely unscrewed.

e. Mount new head with mounting screw fairly loose. Screw in adjusting screw until point protrudes enough to engage its conical locating hole. Tighten mounting screw.

f. Plug in head.

g. Deskew the read head as described in the deskew adjustment procedure.

h. Set deskewing switches on write amplifiers to correspond to chart supplied.

i. Stick chart over old chart to record switch settings.

4.24.6 EOT/BOT SENSOR REPLACEMENT

a. Remove EOT/BOT sensor assembly by unplugging and removing mounting screws. Since it will not pass through the hole provided, the connector must be removed by cutting the cable. Retain the connector.

b. Replacement sensors are provided with connector pins crimped to wires but with connector shell not installed.

c. Replace assembly, passing wires through hole provided. Replace screws.

d. Snap pins into connector shell in same color sequence as in the shell removed and plug in.

e. Adjust as described in adjustment procedure.

4.24.7 TAPE CLEANER REPLACEMENT

a. Remove head cover.

b. Remove circular snap-in plug cover.

c. Remove mounting screw and tape cleaner.

d. Mount new cleaner assembly with mounting screw finger tight.

e. Adjust cleaner surface so that it just touches the tape and is parallel to the tape surface.

f. Tighten mounting screw and install snap-in plug cover.

4.25 MODULE REPAIR

If the difficulty is traced to a plug-in module during troubleshooting, it will usually not be too difficult to find the component at fault and repair the module. All parts used in the electronics are standard commercially available units and may be replaced by others of like type and rating. Normal good practice and workmanship should be exercised.

4.26 MAINTENANCE TOOLS

In addition to normal electronic tools and test gear (an oscilloscope, voltohmmeter, etc.) the following items should be available for service and repair.

Vacuum gauge, Kennedy PN 154-0067-001
Spanner wrench, Kennedy PN 154-0042-001
Set of nut drivers or open end wrenches
Phillips and standard screwdrivers
Capstan puller, Kennedy PN 154-0043-001
Skewmaster tape, Kennedy PN 154-0036-001

Maintenance kit, Kennedy PN 190-2324-001, containing:

Head cleaner
Hex socket keys - 7/64, 5/32, 1/8, 3/32
Lint-free swabs
Reflective marker strips
Magnasee visualizing solution
Loctite grade H
Card extender, Kennedy PN 190-2224-001
Belt Tensiometer, Kennedy PN 154-0568-001
Strobe Disk, Kennedy PN 291-5572-001

Optional maintenance tools:

Extension hose set, Kennedy PN 154-0044-001
Blower extension cord, Kennedy PN 154-0045-001

SECTION V
PARTS IDENTIFICATION

SECTION V

PARTS IDENTIFICATION

5.1 SPARE PARTS ORDERING INFORMATION

This section describes the replaceable parts in your unit which are available only from Kennedy Company. Many parts of the unit are common commercial parts and can be obtained locally from the manufacturer. These parts are marked with the manufacturer's name and part number and are not listed herein.

The serial number and part number are the keys to numerous engineering details applying to your unit. These numbers are on the serial number tag located on the rear panel of the unit.

Changes to Kennedy units are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements developed in our Engineering Department. If a part you have ordered has been replaced by a new part, a Kennedy representative will advise you concerning any change in part number.

All parts orders should be addressed directly to Kennedy Company, Spare Parts Order Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (213) 357-8831 or (213) 681-9314, TWX 910-585-3249.

5.2 IN-WARRANTY REPAIR PARTS ORDERING INFORMATION

Repair parts for in-warranty units are made available on an exchange basis through the Kennedy Company Spare Parts Department. The serial number and part number of the tape unit are necessary to insure shipment of the proper replacement parts.

All inquiries should be directed to Kennedy Company, Spare Parts Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (213) 357-8831 or (213) 681-9314, TWX 910-585-3249.

5.3 EXPORT ORDERS

Customers outside the United States and Canada are served by Kennedy Company international sales agents. All correspondence regarding your unit should be directed to your sales agent. If you prefer, correspondence may be addressed directly to Kennedy Company, Spare Parts Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (213) 357-8831 or (213) 681-9314, TWX 910-585-3249, cable KENNEDYCO.

5.4 ILLUSTRATED PARTS LIST

To assist in parts identification, an illustrated parts list is included in this section with references to photographs of the machine. Part numbers beginning with 198 are listed again in the Recommended Spare Parts list at the end of this section. Kennedy Company recommends that these parts be ordered as spares to minimize machine downtime due to equipment failure. Certain parts on this list have no quantity indicated. We recommend ordering one of each such parts for remote installations where delivery is time consuming.

5.5 FIELD KITS

Some replacement components may be supplied in the form of repair or field change kits. The repair kits contain parts that are matched or assembled and adjusted at the factory because of complexity or to aid the field technician. The components ordered as field kits either by correspondence with Kennedy service engineers or by direct order will be supplied with complete installation instructions. The change kits are intended for standard or special options not originally included in the unit.

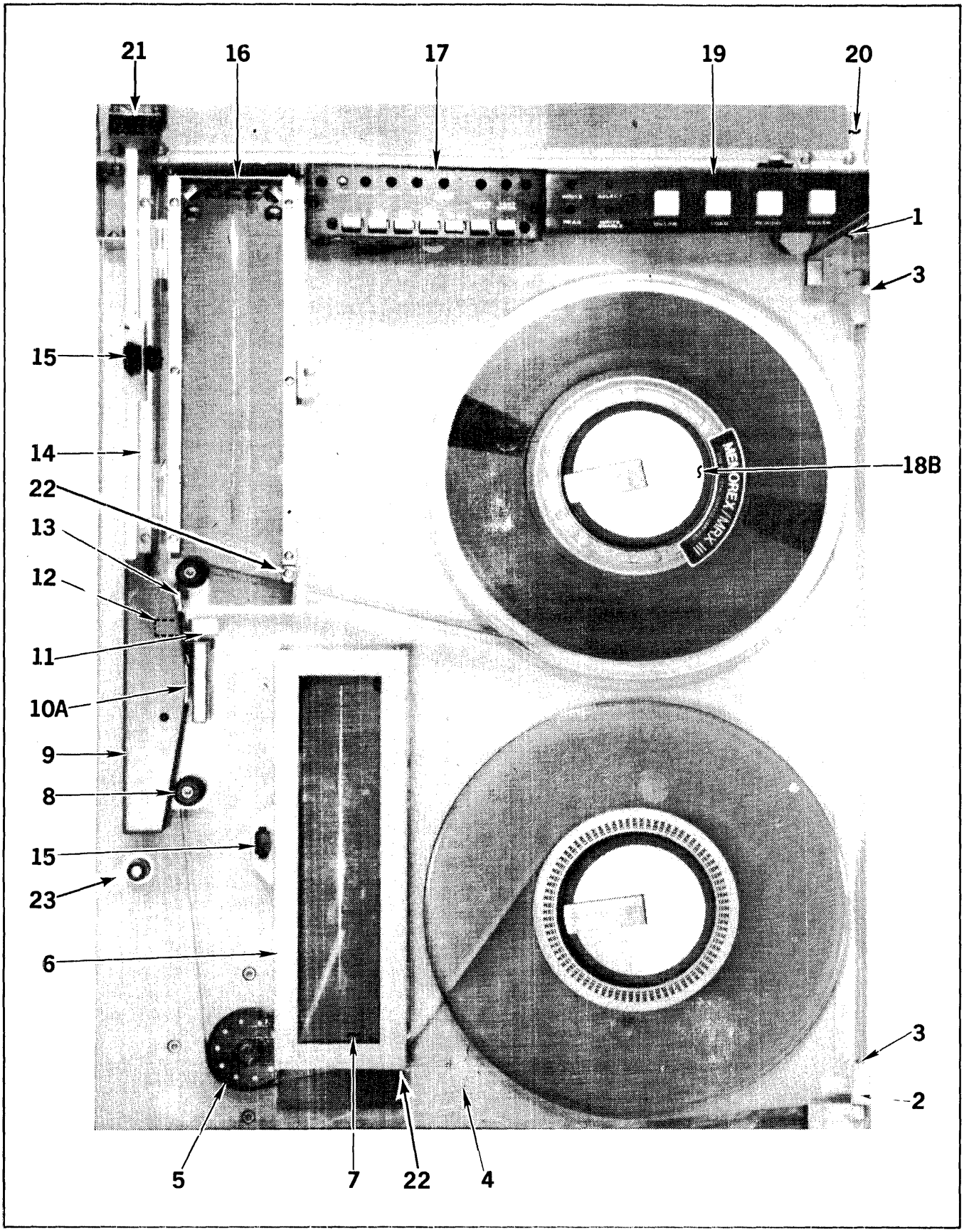


Figure 5-1. Model 9100 Tape Transport: Front View

PARTS LIST

Item No.	Part No.	Description	Notes
1-1	190-5654-001	Door Assy	
1-2	391-5736-001	Dust Cover Hinge	
1-3	191-2939-001	Hinge Pin	
1-4	404-5662-001	Deck Assy	
1-5	198-5699-001	Capstan Wheel	
1-6	198-0018-001	Takeup Vacuum Column Cover	
1-7	198-5675-001	Takeup Vacuum Column Assy	
1-8	190-5732-001	Split Tape Guide Assy, Ceramic	
1-9	291-2775-009	Magnetic Head Cover	
1-10A	198-2399-025	Head and Head Mount Assy, 9 track	1
	198-2399-026	Head and Head Mount Assy, 7 track	1
1-11	*198-5906-002	IR Sensor EOT/BOT	
1-13	190-5750-001	Tape Cleaner Assy	
1-14	198-0017-001	Supply Vacuum Column Cover	
1-15	128-0156-001	Catch, Vacuum Column Cover	
1-16	198-5674-001	Supply Vacuum Column Assy	
1-17	190-5371-002	Test Panel Assy, Dual Density	
1-17	190-5371-003	Test Panel Assy, Dual Density, 45 ips	
1-18B	198-0110-001	Reel Hub Assy, Quick Release	1,2
1-19	198-5687-002	Pushbutton Control Panel Assy	
1-20	190-5658-001	Control Panel Cover Assy	
1-20	190-5658-002	Control Panel Cover Assy with Density Select Switch	
1-21	151-0034-001	Thumbwheel Switch, 1 to 4 (parallel)	
1-22	125-0085-001	Tape Guide	
1-23	128-0153-001	Adjustable Grip Latch	

*Replaces 198-1138-001, LP/EOT Photosensor, and 198-1139-001 BT Photosensor, after SN 5262. (198-5906-002 includes 190-5303-002 Connector board.)

NOTES

1. These parts have detailed parts views on following page.

2. Assembly includes shims for setting hub clearance. Refer to paragraph 4.9.1 of O/M manual for adjustment procedure.

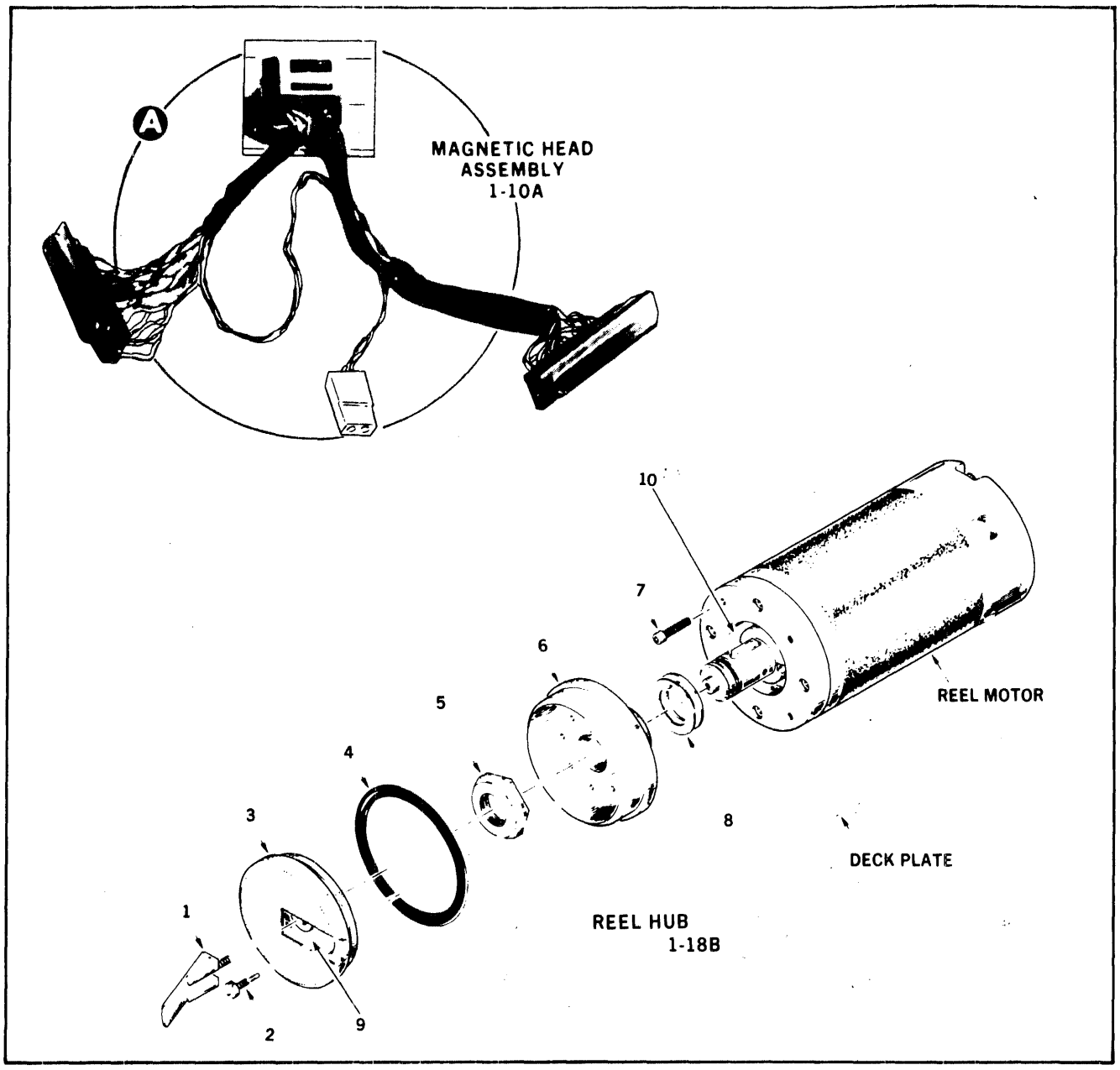


Figure 5-2

PARTS LIST FOR FIGURE 5-2

Item No.	Part No.	Description	Qty	Notes
2-1	190-4778-002	Hub Latch Assy		
2-2	191-4709-001	Index Screw		
2-3	190-4704-001	Outer Hub Assy		
2-4	125-0030-006	O Ring, 3.645" OD		
2-5	191-4708-001	Hub Nut		
2-6	291-4705-002	Inner Hub		
2-7	128-1000-095	Screw, 8-32 x .875", Hex Hd, Stl Cad Plate II		
2-8	198-0082-001	Shim Set Assy		
2-9	191-3451-001	Thrust Washer		
2-10	191-4710-001	Key (3/16" x 3/16" x 3/4")		

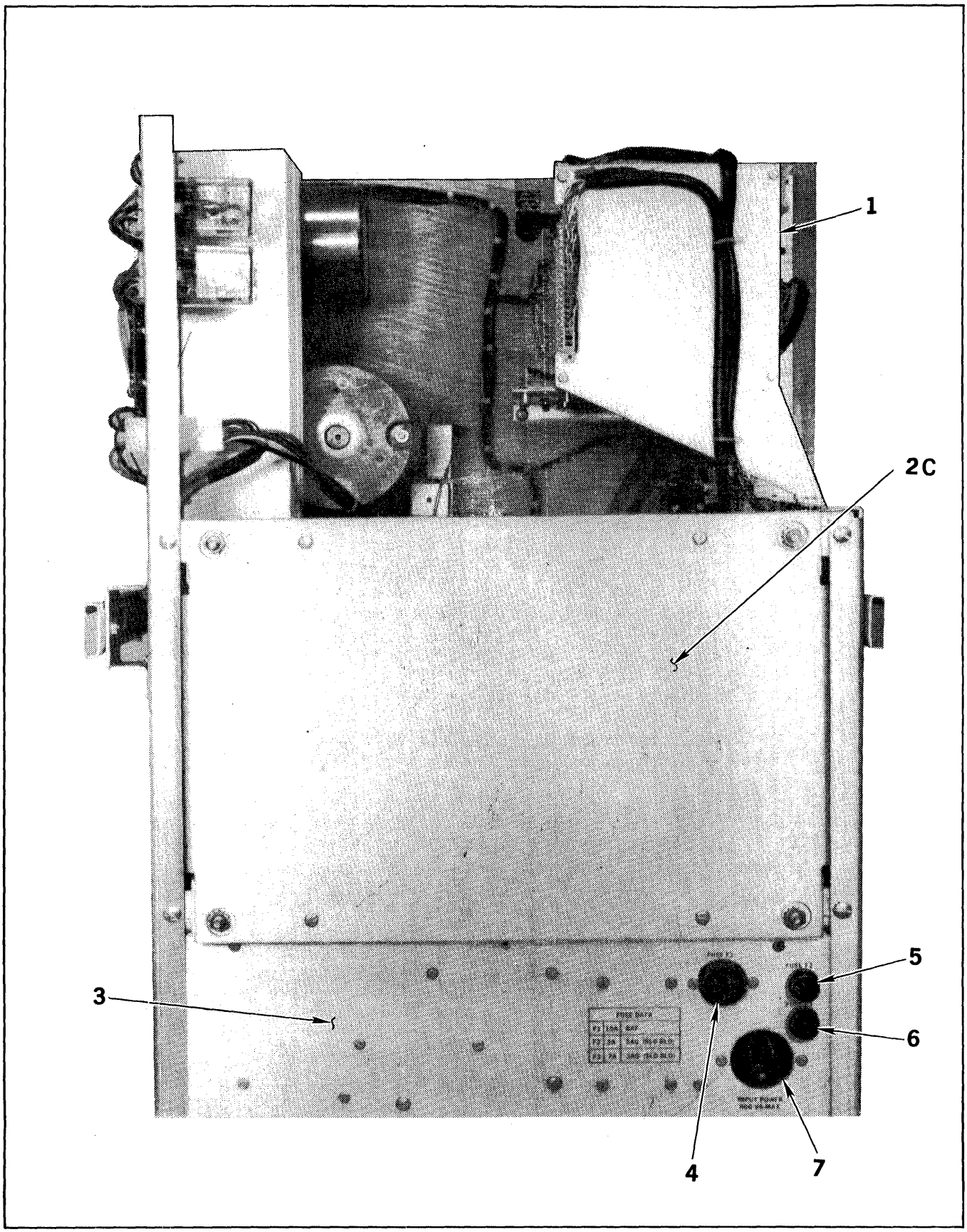
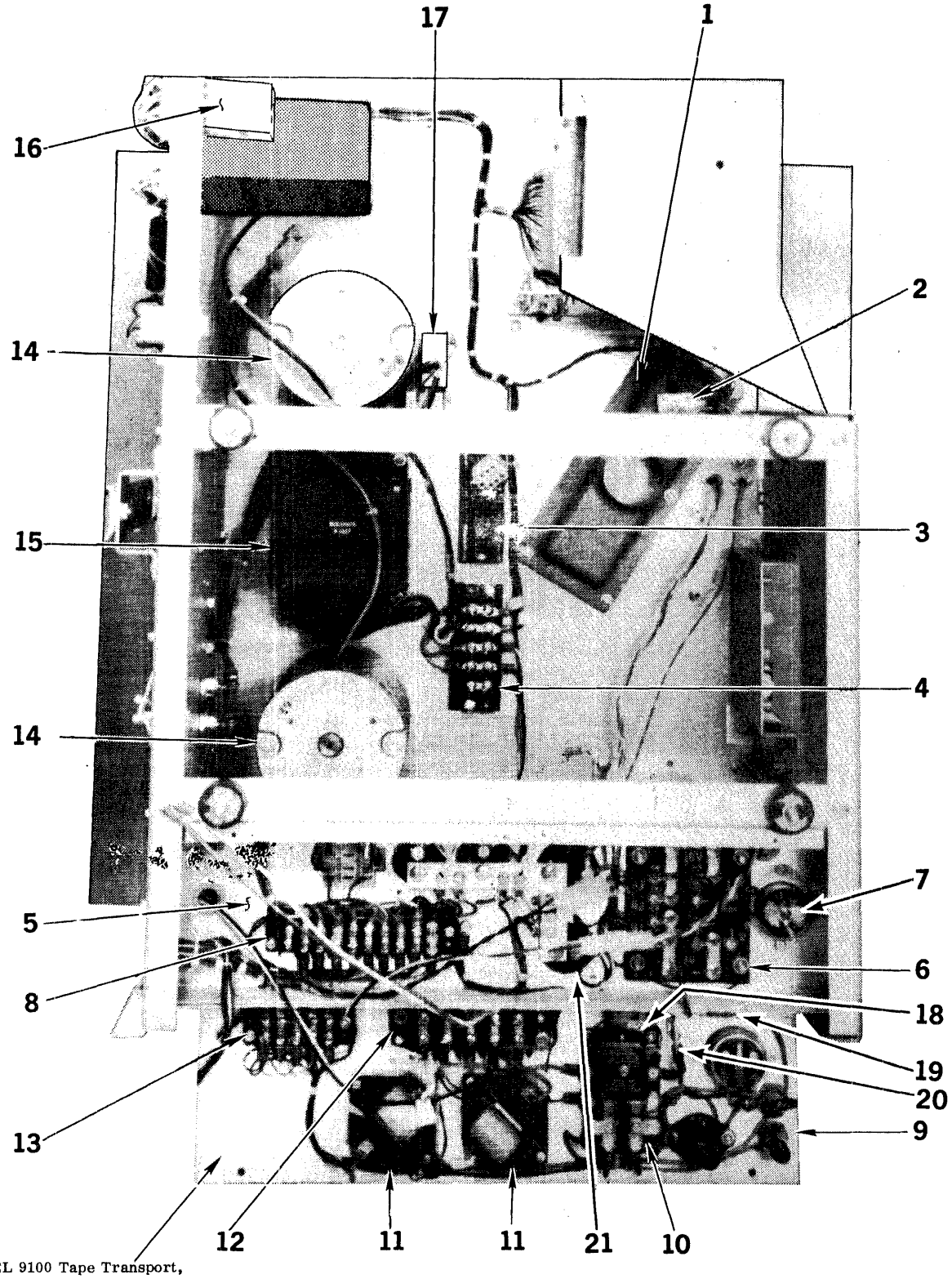


Figure 5-3. Rear View: With Panel



MODEL 9100 Tape Transport,
Vacuum Blower Assy Removed,
Power Panel Cover Open.

Figure 5-4. Rear View: Without Panel

PARTS LIST

Item No.	Part No.	Description
3-1	190-5657-001	Card Cage Assy, Dual Density (w/o modules)
3-2C	190-5659-001	Vacuum Blower Assy, 110 vac, 60 Hz, 0' to 4K' alt
	190-5659-002	Vacuum Blower Assy, 220 vac, 50 Hz, 0' to 4K' alt
	190-5659-003	Vacuum Blower Assy, 110 vac, 60 Hz, 4K' to 8K' alt
	190-5659-004	Vacuum Blower Assy, 110 vac, 60 Hz, 8K' to 12K' alt
	190-5659-005	Vacuum Blower Assy, 220 vac, 60 Hz, 0' to 4K' alt
	190-5659-006	Vacuum Blower Assy, 240 vac, 50 Hz, 0' to 4K' alt
	190-5659-007	Vacuum Blower Assy, 110 vac, 50 Hz, 0' to 4K' alt
	190-5659-008	Vacuum Blower Assy, 220 vac, 50 Hz, 4K' to 8K' alt
	190-5659-009	Vacuum Blower Assy, 110 vac, 50 Hz, 4K' to 8K' alt
	190-5659-010	Vacuum Blower Assy, 100 vac, 50 Hz, 0' to 4K' alt
	190-5659-011	Vacuum Blower Assy, 100 vac, 60 Hz, 0' to 4K' alt
3-3	190-5686-001	Power Panel Cover Assy
3-4	151-0066-001	F1 Fuseholder, 30A Bus
	198-0067-150	Fuse, 15A 125v (110 vac use)
	198-0067-080	Fuse, 8A 250v (220 vac use)
3-5	151-0802-001	F2 Fuseholder, 15A
	198-0133-030	Fuse, 3A 250v
3-6	151-0802-001	F3 Fuseholder, 15A
	198-0133-080	Fuse, 8A 250v (110 vac use)
	198-0133-050	Fuse, 5A 250v (220 vac use)
3-7	121-9001-003	Power Input Socket
4-1	198-5683-001	Intake Plenum Cover
4-2	198-0064-001	Vacuum Switch
4-3	*190-5303-002	Connector Board Assy
4-4	121-0172-005	Terminal Strip, 5 Circuit
4-5	190-5656-001	Power Panel Chassis Assy
4-6	190-5584-001	Rectifier PC Board Assy
4-7	121-0171-001	Twist-On Outlet Receptacle
4-8	121-0140-010	Terminal Strip, 10 Circuit
4-9	190-5686-001	Power Panel Cover Assy
4-10	145-0016-001	Relay
4-11	190-5707-001	Solid State Switch Assy
4-12	121-0172-005	Terminal Strip, 5 Circuit
4-13	121-0140-005	Terminal Strip, 5 Circuit
4-14	190-5698-001	Reel Motor Assy
4-15	190-5725-001	T2 High Power Transformer Assy
4-16	145-0005-001	Relay, 12 vdc
	145-0005-002	Relay, 6 vdc
4-17	190-2641-004	File Protect Switch Assy
4-18	115-0019-001	Capacitor, 0.47 mfd, 400 vdc
4-19	147-1520-050	Resistor, Wire Wound, 5 ohm, 20w, 10%
4-20	147-1520-101	Resistor, Wire Wound, 100 ohm, 20w, 5%
4-21	115-3610-449	Capacitor, Elect, 35K mfd, 10v
	191-5705-001	Filter

*Replaces 190-4013-001, Connector board, after SN 5262.

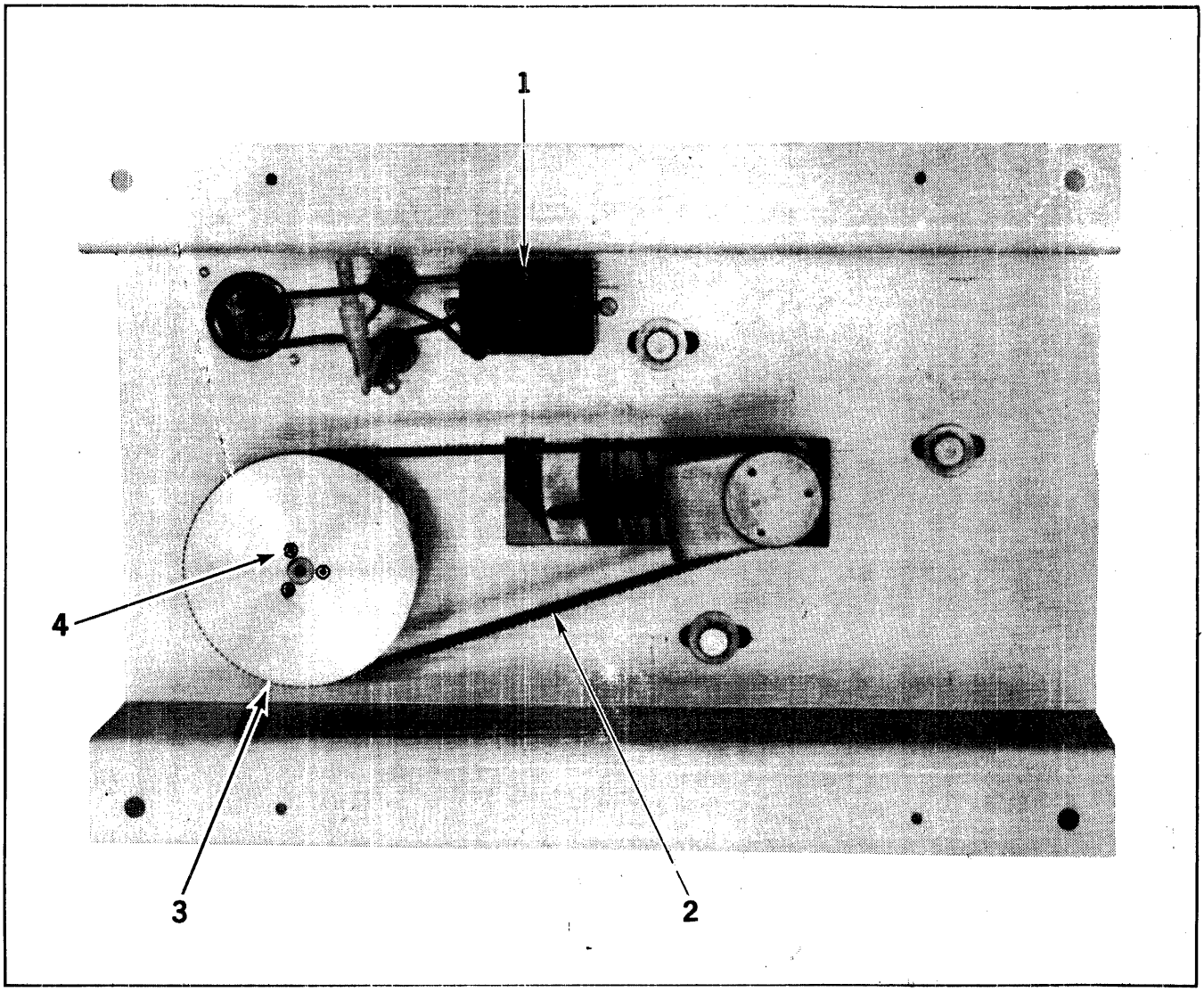


Figure 5-5. Vacuum Blower Assembly: Bottom View

PARTS LIST FOR FIGURE 5-5

Item No.	Part No.	Description
5-1	145-0017-001	Motor Starting Relay, 110 vac, 60 Hz
	145-0017-002	Motor Starting Relay, 220 vac, 50 Hz
5-2	135-0056-001	Flat Belt, 60 Hz, 0' to 8K' alt
	135-0056-002	Flat Belt, 60 Hz, 8K' to 12K' alt/50 Hz, 0' to 4K' alt
	135-0056-008	Flat Belt, 50 Hz, 4K' to 8K' alt
5-3	291-5845-101	Pulley, 110/220 vac, 60 Hz, 0' to 4K' alt
	291-5845-102	Pulley, 110 vac, 60 Hz, 4K' to 8K' alt
	291-5845-103	Pulley, 220 vac, 50 Hz, 0' to 4K' alt/100 vac, 60 Hz 8K' to 12K' alt
	291-5845-104	Pulley, 220 vac, 50 Hz, 4K' to 8K' alt/110 vac, 60 Hz
	291-5845-105	Pulley, 220 vac, 50 Hz, 8K' to 12K' alt
	291-5572-001	Strobe Disk, 75 ips, 60 Hz
	291-5572-002	Strobe Disk, 75 ips, 50 Hz
	291-5572-003	Strobe Disk, 45 ips, 60 Hz
5-4	128-1000-064	Machine Screw, Hex Socket Head, 6-32 x 5, Stl Cad

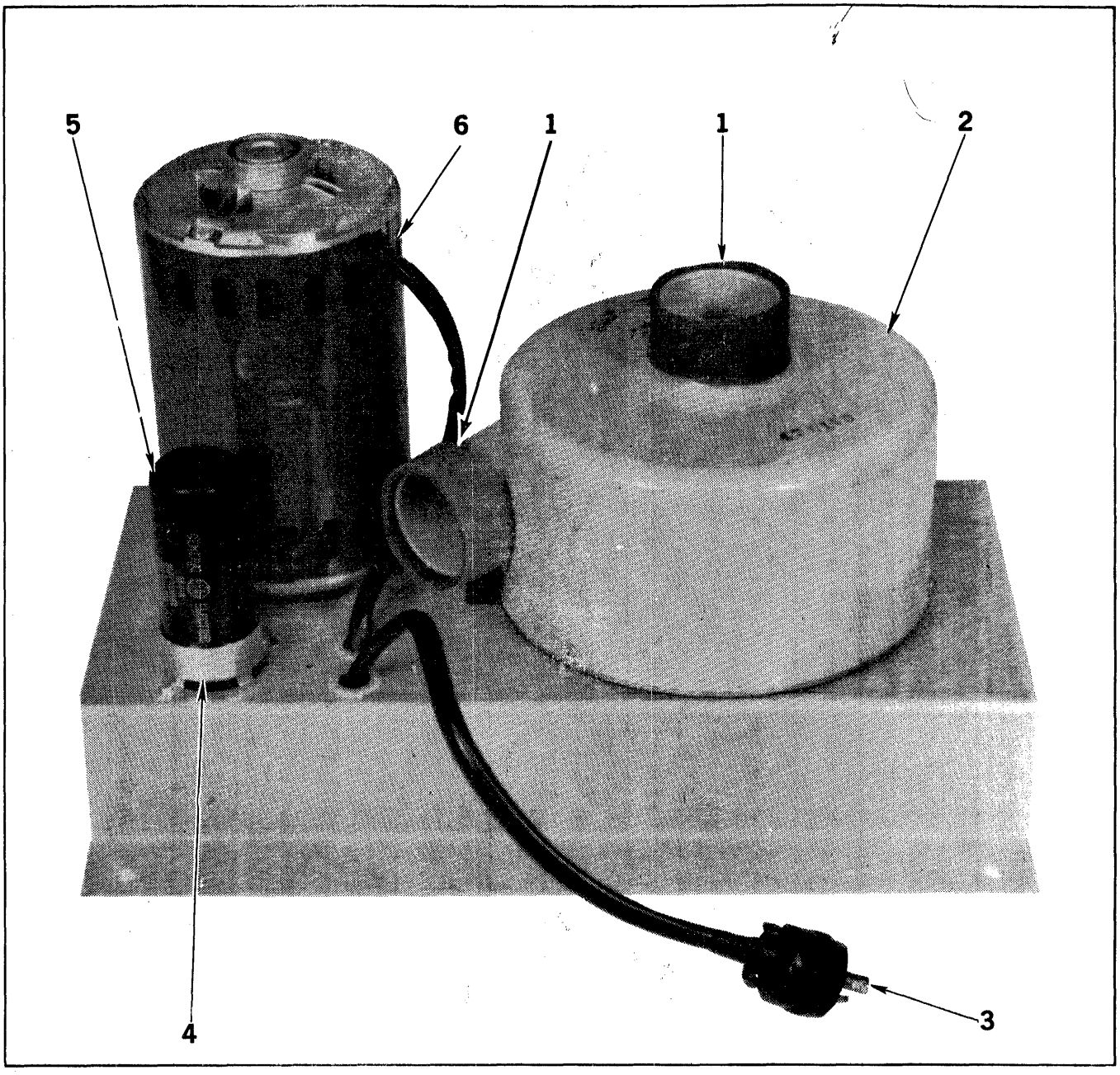


Figure 5-6. Vacuum Blower Assembly: Top View

PARTS LIST FOR FIGURE 5-6

Item No.	Part No.	Description
6-1	191-5668-001	Sleeve
6-2	126-0001-003	Blower, Belt Drive
6-3	121-0171-002	AC Plug
6-4	115-0003-001	Capacitor Mounting Clamp, 100 vac, 60 Hz
	115-0003-005	Capacitor Mounting Clamp, 220 vac, 50 Hz
6-5	115-0018-001	AC Motor Starting Capacitor, 270-324 mfd, 110 vac, 60 Hz
	115-0018-002	AC Motor Starting Capacitor, 72-88 mfd, 250 vac, 50/60 Hz
6-6	190-5846-003	Blower Motor/Hub Assy, 110 vac, 50/60 Hz
	190-5846-004	Blower Motor/Hub Assy, 220 vac, 50/60 Hz
	190-5846-005	Blower Motor/Hub Assy, 240 vac, 50/60 Hz
	190-5846-006	Blower Motor/Hub Assy, 100 vac, 50/60 Hz

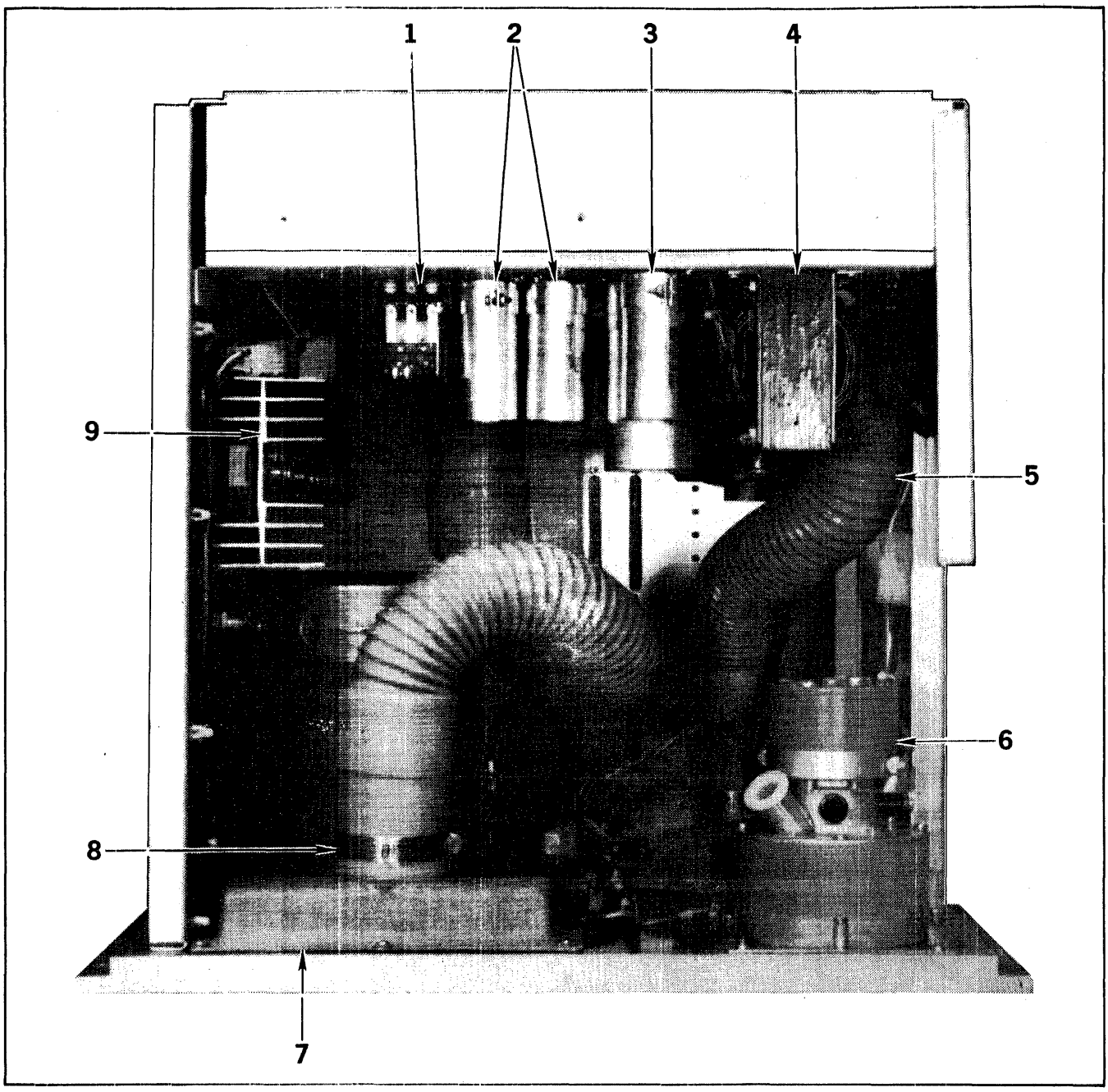


Figure 5-7. Model 9100 Tape Transport: Bottom View

PARTS LIST FOR FIGURE 5-7

Item No.	Part No.	Description
7-1	145-0005-001	Relay, 12 vdc
	145-0005-002	Relay, 6 vdc
7-2	115-3625-798	Capacitor, Electrolytic, 7,900 mfd, 25 vdc
7-3	115-3610-449	Capacitor, Electrolytic, 40,000 mfd, 10 vdc
7-4	198-4163-001	T1 Transformer
7-5	198-0046-001	Hose Assy, Supply
7-6	190-4721-001	Capstan Motor Assy
7-7	198-5683-002	Exhaust Plenum Cover
7-8	190-5848-001	Hose Assy, Blower to Plenum Cover
7-9	190-5671-001	Regulator and Servo Assy

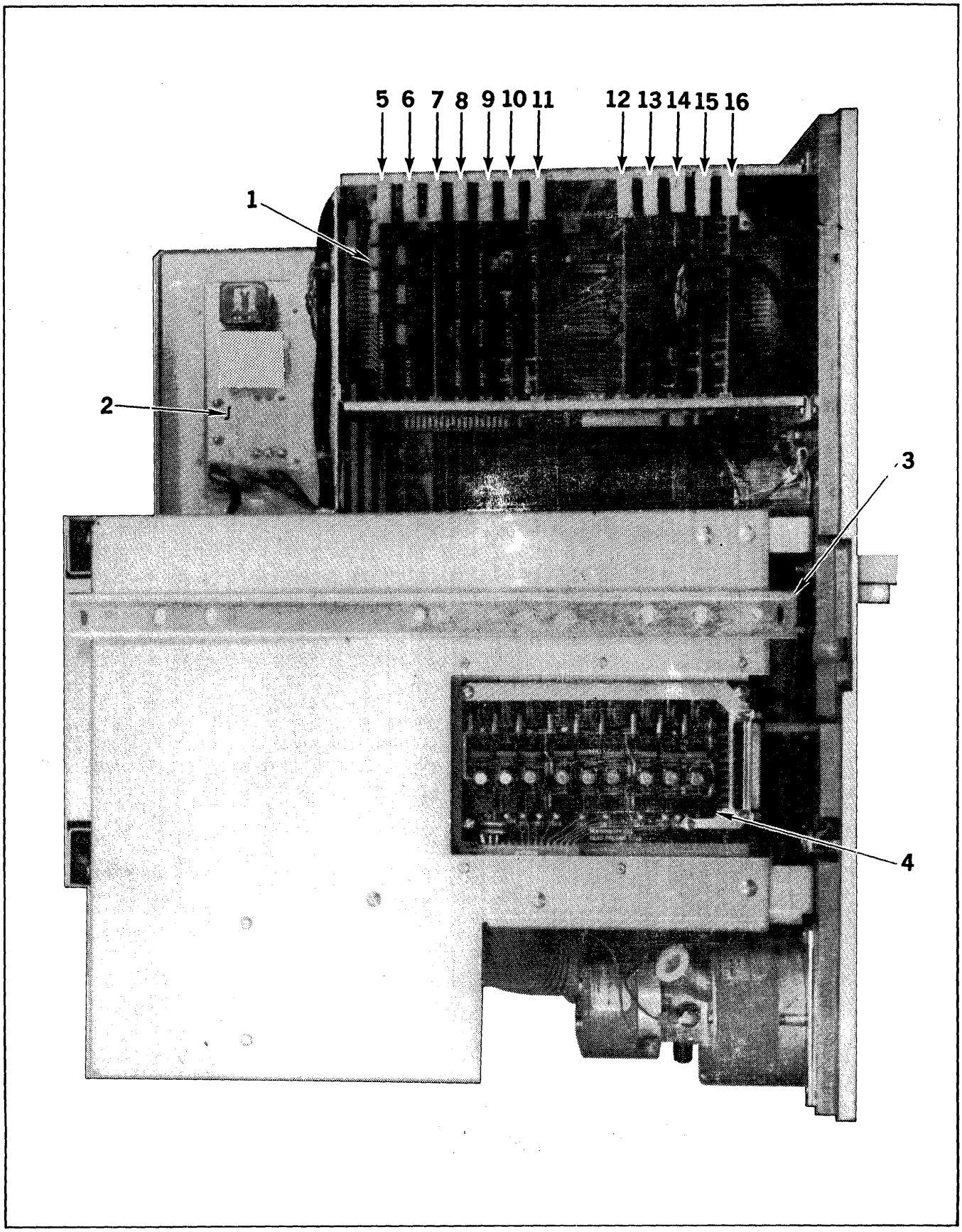


Figure 5-8. Model 9100 Tape Transport: Left Side

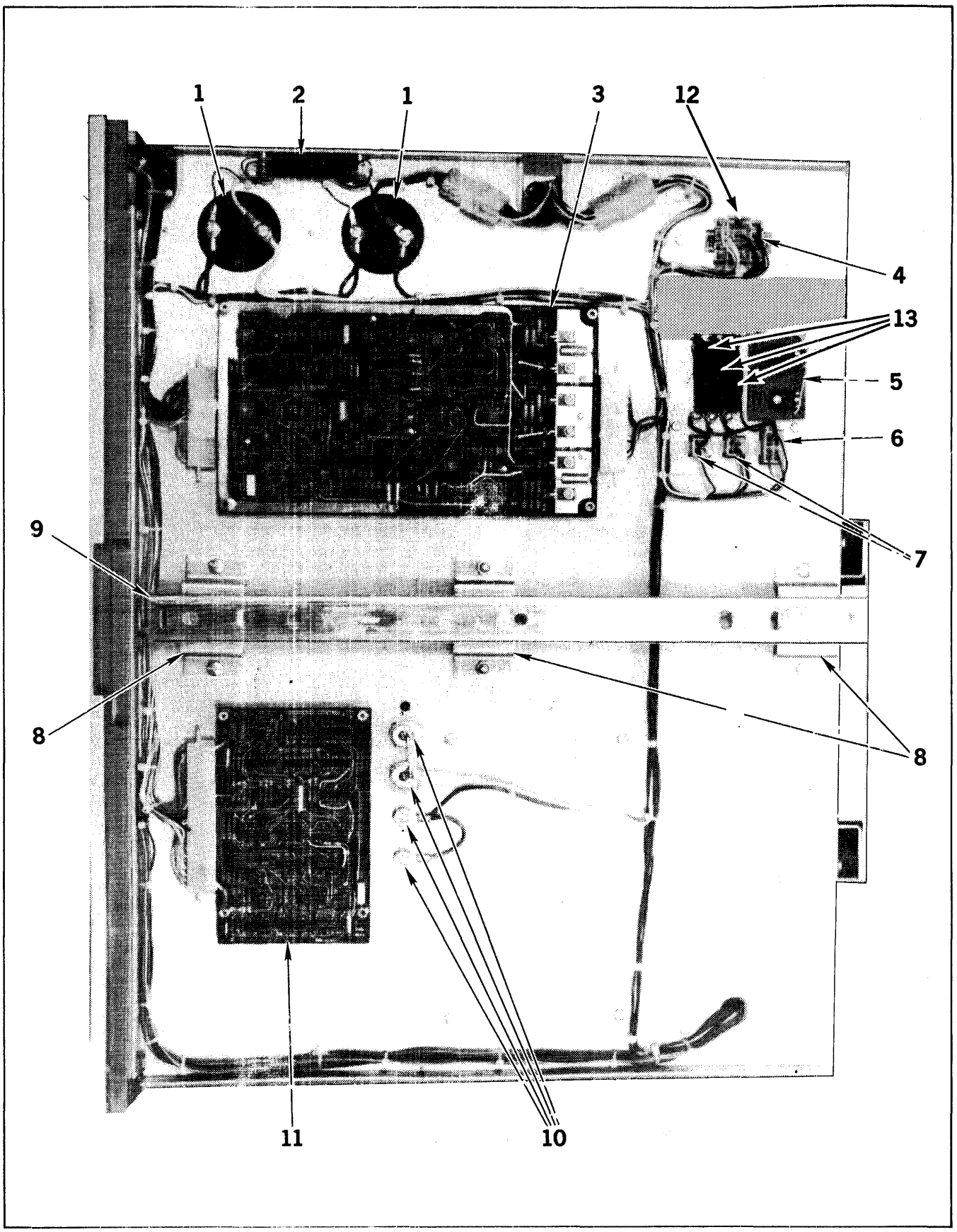


Figure 5-9. Model 9100 Tape Transport: Right Side

PARTS LIST

Item No.	Part No.	Description	Notes
8-1	190-5664-002	Masterboard, Dual Density	
8-2	190-5840-001	Reel Plate Assy	
8-3	128-0151-003	Slide Set, Heavy Duty	
8-4	190-5728-xxx	Read Preamplifier Assy	1
8-5	190-5368-xxx	Five Channel Write Amplifier	1
8-6	190-5366-xxx	Four Channel Write Amplifier	1
8-7	190-3860-xxx	Data Terminator	1
8-8	190-4385-xxx	This PC board replaced by:	
	190-6385-xxx	Quad Read Amplifier	1
8-9	190-4385-xxx	This PC board replaced by:	
	190-6385-xxx	Quad Read Amplifier	1
8-10	190-4367-xxx	This PC board replaced by:	
	190-6367-xxx	Dual P Channel/Clipping	1
8-11	190-4365-xxx	Replaced by:	
	190-6365-xxx	Dual Density Control (800/1600 cpi models)	1
	190-5771-xxx	Delay Timing (200, 556, 800 cpi models)	1
8-12	190-3841-xxx	Control Terminator	1
8-13	190-3842-xxx	Interface Control	1
8-14	190-3843-xxx	Pushbutton Control	1
8-15	190-5733-xxx	Ramp Generator	1
8-16	190-5719-001	Sensor Amplifier Driver	
9-1	115-3625-479	Capacitor, Electrolytic, 47,000 mfd, 25 vdc	
9-2	147-1520-101	Resistor, WW, 100 ohm, 20w	
9-3	190-6666-xxx	Servo Preamplifier Assy	1
9-4	121-0175-001	Relay II Circuit Connector	
9-5	190-5770-001	Braking Board Assy	
9-6	121-0173-005	Molex Flat Blade Connector, 4 circuit	
9-7	121-0173-001	Molex Flat Blade Connector, 2 circuit	
9-8	191-5681-001	Spacer	
9-9	*190-5507-001	Slide Set, Heavy Duty	
9-10	148-0085-001	Rectifier, Silicon, High Power, 1N1184	
9-11	190-6667-xxx	Sequence Control Assy	1
9-12	148-0015-001	Rectifier, Silicon 1N2069	
9-13	147-0028-001	Resistor 0.1 ohm, 10w, 1%	

*For serial numbers prior to 5263, please consult factory.

NOTES

1. The last 3 dash numbers of these modules vary, depending on machine specifications. These dash numbers are stamped on the module, or may be found on the circuit card identification strip.

RECOMMENDED SPARE PARTS LIST

(Certain parts in this list have no quantity indicated. For remote installations where parts delivery is time consuming, we recommend ordering one of each of these parts as required for your machine in addition to the recommended quantities of the regular spares.)

Item No.	Part No.	Description	Qty	Notes
1-20	198-5665-001	Assy PC Board Display Panel		
1-5	198-5699-001	Capstan	1	
1-7	198-5675-001	Takeup Vacuum Column Assy	1	
1-8	190-5732-001	Split Tape Guide Assy, Ceramic	2	
1-10A	198-2399-025	Head and Head Mount Assy, 9 track	1	2
	198-2399-026	Head and Head Mount Assy, 7 track	1	2
1-11	*198-5906-002	IR Sensor EOT/BOT	1	
1-13	190-5750-001	Tape Cleaner Assy	1	
1-15	128-0156-001	Catch, Vacuum Column Cover	1	
1-16	198-5674-001	Supply Vacuum Column Assy	1	
1-17	190-5655-002	Replaced by:		
	190-5371-002	Test Panel Assy, Dual Density	1	
	190-5655-003	Replaced by:		
	190-5371-003	Test Panel Assy, Dual Density	1	
1-19	198-5687-002	Pushbutton Control Panel Assy	1	1
1-22	125-0085-001	Tape Guide	1	
3-2C	190-5659-001	Vacuum Blower Assy, 110 vac, 60 Hz, 0' to 4K' alt		
	190-5659-002	Vacuum Blower Assy, 220 vac, 50 Hz, 0' to 4K' alt		
	190-5659-003	Vacuum Blower Assy, 110 vac, 60 Hz, 4K' to 8K' alt		
	190-5659-004	Vacuum Blower Assy, 110 vac, 60 Hz, 8K' to 12K' alt		
	190-5659-005	Vacuum Blower Assy, 220 vac, 60 Hz, 0' to 4K' alt		
	190-5659-006	Vacuum Blower Assy, 240 vac, 50 Hz, 0' to 4K' alt		
	190-5659-007	Vacuum Blower Assy, 110 vac, 50 Hz, 0' to 4K' alt		
	190-5659-008	Vacuum Blower Assy, 220 vac, 50 Hz, 4K' to 8K' alt		
	190-5659-009	Vacuum Blower Assy, 110 vac, 50 Hz, 4K' to 8K' alt		
	190-5659-010	Vacuum Blower Assy, 100 vac, 50 Hz, 0' to 4K' alt		
	190-5659-011	Vacuum Blower Assy, 100 vac, 60 Hz, 0' to 4K' alt		
	151-0066-001	F1 Fuseholder, 30A Bus		
	198-0067-150	Fuse, 15A (110 vac use) (5 per box)	1 box	
	198-0067-080	Fuse, 8A (220 vac use) (5 per box)	1 box	
3-5	151-0802-001	F2 Fuseholder, 15A		
	198-0133-030	Fuse, 3A 3AG (5 per box)	1 box	
3-6	151-0802-001	F3 Fuseholder, 15A		
	198-0133-080	Fuse, 8A 3AG (110 vac use) (5 per box)	1 box	
	198-0133-050	Fuse, 5A 3AG (220 vac use) (5 per box)	1 box	
4-1	198-5683-001	Intake Plenum Cover		
4-2	198-0064-001	Vacuum Switch	1	
4-5	190-5656-001	Power Panel Assy		
4-6	190-5584-001	Rectifier PC Board	1	
4-9	190-5686-001	Power Panel Cover Assy		
4-10	145-0016-001	Relay	1	
4-11	190-5707-001	Solid State Switch	1	
4-14	190-5698-001	Reel Motor Assy	1	
4-15	190-5725-001	High Power Transformer Assy		
4-17	190-2641-004	File Protect Switch Assy	1	
4-20	147-1520-101	Resistor, Wire Wound, 100 ohm, 20w, 5%		
5-1	145-0017-001	Motor Starting Relay, 110 vac, 60 Hz	1	
	145-0017-002	Motor Starting Relay, 220 vac, 50 Hz	1	

*Replaces 198-1138-001, LP/EOT Photosensor, and 198-1139-001 BT Photosensor, after SN 5262. (198-5906-002 includes 190-5303-002 Connector board.)

(NOTES (see last page)

RECOMMENDED SPARE PARTS LIST

Item No.	Part No.	Description	Qty	Notes
5-2	135-0056-001	Flat Belt, 60 Hz, 0' to 8K' alt	1	
	135-0056-002	Flat Belt, 60 Hz, 8K' to 12K' alt/50 Hz, 0' to 4K' alt	1	
	135-0056-008	Flat Belt, 50 Hz, 4K' to 8K' alt	1	
5-3	291-5845-101	Pulley, 110/220 vac, 60 Hz, 0' to 4K' alt		
	291-5845-102	Pulley, 110 vac, 60 Hz, 4K' to 8K' alt		
	291-5845-103	Pulley, 110 vac, 60 Hz, 8K' to 12K' alt/220 vac, 50 Hz 0' to 4K' alt		
	291-5845-104	Pulley, 220 vac, 50 Hz, 4K' to 8K' alt		
	291-5845-105	Pulley, 220 vac, 50 Hz, 8K' to 12K' alt		
	291-5572-001	Strobe Disk, 75 ips, 60 Hz	1	
	291-5572-002	Strobe Disk, 75 ips, 50 Hz	1	
	291-5572-003	Strobe Disk, 45 ips, 60 Hz	1	
6-2	126-0001-003	Blower Belt Drive	1	
6-5	115-0018-001	Motor Starting Capacitor, 270-324 mfd, 110 vac, 60 Hz		
	115-0018-002	Motor Starting Capacitor, 72-88 mfd, 250 vac, 50/60 Hz		
6-6	190-5846-003	Blower Motor/Hub Assy, 110 vac, 60 Hz	1	
	190-5846-004	Blower Motor/Hub Assy, 220 vac, 50/60 Hz	1	
	190-5846-005	Blower Motor/Hub Assy, 240 vac, 50/60 Hz	1	
	190-5846-006	Blower Motor/Hub Assy, 100 vac, 50/60 Hz	1	
7-1	145-0005-001	Relay, 12 vdc	1	
	145-0005-002	Relay, 6 vdc	1	
7-2	115-3625-798	Capacitor, Electrolytic, 7,900 mfd, 25 vdc		
7-3	115-3610-449	Capacitor, Electrolytic, 40,000 mfd, 10 vdc		
7-4	198-4163-001	T1 Low Power Transformer		
7-5	198-0046-001	Hose Assy, Supply		
7-6	190-4721-001	Capstan Motor Assy	1	3
7-7	198-5683-002	Exhaust Plenum Cover		
7-8	198-0047-001	Hose Assy, Exhaust		
7-9	190-5671-001	Regulator and Servo Assy	1	4
8-1	190-5664-002	Masterboard, Dual Density		
8-4	190-5728-xxx	Read Preamplifier	1	
8-5	190-4368-xxx	Five Channel Write Amplifier (45 ips)	1	6
8-5	190-5368-xxx	Five Channel Write Amplifier (75 ips)	1	6
8-6	190-4366-xxx	Four Channel Write Amplifier (45 ips)	1	6
8-6	190-5366-xxx	Four Channel Write Amplifier (75 ips)	1	6
8-7	190-3860-xxx	Data Terminator		6
8-8	190-4385-xxx	Replaced by:		
	190-6385-xxx	Quad Read Amplifier	1	6
8-9	190-4385-xxx	Replaced by:		
	190-6385-xxx	Quad Read Amplifier	1	6
8-10	190-4367-xxx	Replaced by:		
	190-6367-xxx	Dual P Channel/Clipping	1	6
8-11	190-4365-xxx	Replaced by:		
	190-6365-xxx	Dual Density Control (800, 1600 cpi models)	1	6
8-12	190-5771-xxx	Delay Timing (200,556,800 cpi models)	1	6
	190-3841-001	Control Terminator		6
8-13	190-3842-xxx	Interface Control	1	6
8-14	190-3843-xxx	Pushbutton Control	1	6
8-15	190-5733-xxx	Ramp Generator	1	6
8-16	190-5719-001	Sensor Amplifier Driver	1	6
9-1	115-3625-479	C1, C2 Capacitor, Electrolytic, 48,000 mfd, 25 vdc		
9-3	190-6666-101	Servo Preamplifier	1	6

NOTES (see last page)

RECOMMENDED SPARE PARTS LIST

Item No.	Part No.	Description	Qty	Notes
9-11	190-6667-xxx	Sequence Control Module	1	6
	121-0198-004	Power Cord, 10A		
	198-0100-002	Hub Repair Kit, Model 9100	2	5
	198-0021-001	Brush Replacement Kit, Capstan Motor (2 brushes)	1	

NOTES

1. Unless specified, door assemblies and control panels will be shipped with standard paint colors. Please specify if special paint or logo is required.
2. Head is supplied on mounting plate and with face shield and connector. Specify number of tracks. All heads are read after write with side mounted erase. Deskew chart is furnished with each head.
3. Capstan motor/tachometer assembly is supplied with capstan wheel in case of damage to capstan during removal.
4. Heatsink assembly includes Power Supply Regulator module 190-4352-001. This module is not readily replaceable without replacing heatsink.
5. Repair kit contains those items subject to wear.
6. The last three dash numbers of this module will vary according to machine specifications. These dash numbers are stamped on the module, or may be found on the circuit card identification strip in the machine. The complete module part number should be specified during ordering.

MAINTENANCE TOOLS

In addition to normal electronic tools and test gear (an oscilloscope, voltohmmeter, etc.) the following items should be available for service and repair.

Kennedy Part No.	Description
154-0067-001	Vacuum Gauge
154-0042-001	Spanner Wrench
	Set of Nut Drivers or Open End Wrenches
	Phillips and Standard Screwdrivers
154-0043-001	Capstan Puller
154-0036-001	Skewmaster Tape
190-2324-001	Maintenance Kit
	Containing:
	Head cleaner
	Hex socket keys - 7/64,5/32,1/8,3/32
	Lint-free swabs
	Reflective marker strips
	Magnasee visualizing solution
	Loctite grade H
190-2224-001	Card Extender

Optional Maintenance Tools

154-0044-001	Extension Hose Set
154-0045-001	Blower Extension Cord
154-0063-001	Hub/File Protect Height Gauge
154-0568-001	Tensiometer

SECTION VI

WIRING AND SCHEMATIC DIAGRAMS

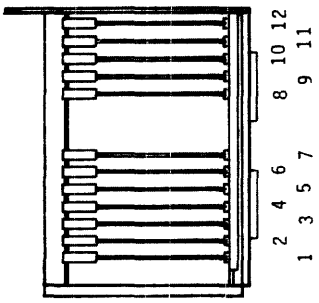
SECTION VI

WIRING AND SCHEMATIC DIAGRAMS

This section contains the wiring diagrams, schematic diagrams, and circuit descriptions for the individual circuit cards used in the transport. The schematics are arranged by functional group as shown below.

Electronics symbols used in the drawings conform to MIL-STD-15. Abbreviations conform to MIL-STD-12 unless otherwise specified. Logic diagrams conform to MIL-STD-806C.

Overall	Model 9100 Wiring Diagram Model 9100 Power Supply Type 5664 Masterboard
Control Electronics	Type 3842 Interface Control Model 9100 Tape Motion Controls (includes Type 5665 Main Control Panel Type 3843 Pushbutton Control Type 5655 Test Panel Switch) Type 3841 Control Terminator Type 6667 Sequence Control Type 5733 Ramp Generator Type 5719 Sensor Amplifier/Driver Type 5655 Test Panel Switch (includes Type 3864 LED Panel Type 4568 Cycler Type 4865 Test Panel) Type 4013 Connector Board
Servo	Type 6666 Servo Preamplifier Type 5670 Braking Board Type 5672 Resistor Board
Read Section	Type 3935 Read Preamplifier (45 ips models) Type 5728 Read Preamplifier (75 ips models) Type 4385 Quad Read Amplifier Type 6385 Quad Read Amplifier Type 4365 Dual Density Control Type 5771 Delay Timing (7 track models) Type 4367 Dual Density P Channel/Clipping Control Type 6367 Dual Density P Channel/Clipping Control
Write Section	Dual Density Write Section Type 4366A/4368A Write Amplifiers (45 ips models) Type 5366/5368 Write Amplifiers (75 ips models) Type 3860 Data Terminator



CIRCUIT CARD IDENTIFICATION		
LOC	TYPE	FUNCTION
	READ/WRITE SECTION	
1	5368-001	5 CHANNEL WRITE AMPLIFIER
2	5366-002	4 CHANNEL WRITE AMPLIFIER
3	3860-001	DATA TERMINATOR
4	6385-006	QUAD READ AMPLIFIER
5	6385-006	QUAD READ AMPLIFIER
6	6367-006	DUAL P CHANNEL/CLIPPING
7	4365-006	DUAL DENSITY CONTROL
	CONTROL SECTION	
8	3841-001	CONTROL TERMINATOR
9	3842-001	INTERFACE CONTROL
10	3843-001	PUSHBUTTON CONTROL
11	5733-001	RAMP GENERATOR
12	5719-001	SENSOR AMPLIFIER/DRIVER

MODEL	PART NO.	INTERFACE
9100	192-9100-003	STD

SPEED	DENSITY	TRACKS
75 IPS	800/1600 CPI	9

MODIFICATIONS

NOTES TO SCHEMATIC SECTION

Certain conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified the resistor may be either 1/4 or 1/2 watt.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5v) and 7 (ground) for 14 pin packages, and 16 (+5v) and 8 (ground) for 16 pin packages. Some ICs -- 7476, 7492, 7493 for example -- have power connections on pin 5 (+5v) and pin 10 (ground). Operational amplifiers in the 8 pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

7. Abbreviations used in from and to designations are as follows:

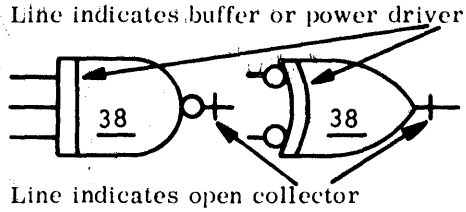
CI	Control Interface
PBC	Pushbutton Control
RG	Ramp Generator
SA	Sensor Amplifier/Driver
DT	Delay Timing
RA/CL	Read Amplifier/Clipping Level
RA	Quad Read Amplifier
WA1	Four Channel Write Amplifier
WA2	Five Channel Write Amplifier

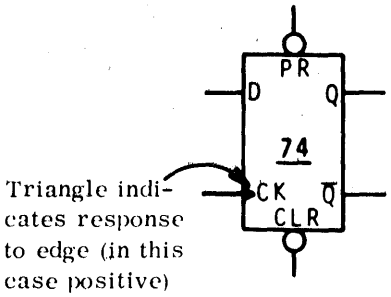
8. Positive logic is shown for all internal connections. Interface connections are zero true but the bar is omitted.

9. Integrated circuit symbols contain a circuit designator that corresponds to the number silkscreened onto the circuit module above an underlined number representing the IC type.

   The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a 00 designation indicates a 7400 quad two input NAND gate. T.I.'s complete part number is SN7400N. In multifunctional units in close proximity to each other the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

   Military Standard 806C is the base for logic symbols. Additional conventions are shown below.



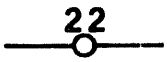


10. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

11. Unless otherwise specified, light emitting diodes are FLV102 or equivalent.

12. Module connector pins are shown as

where no further connection is shown on the schematic, and as



when there is a connection shown.

13. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown their destinations may not be shown.

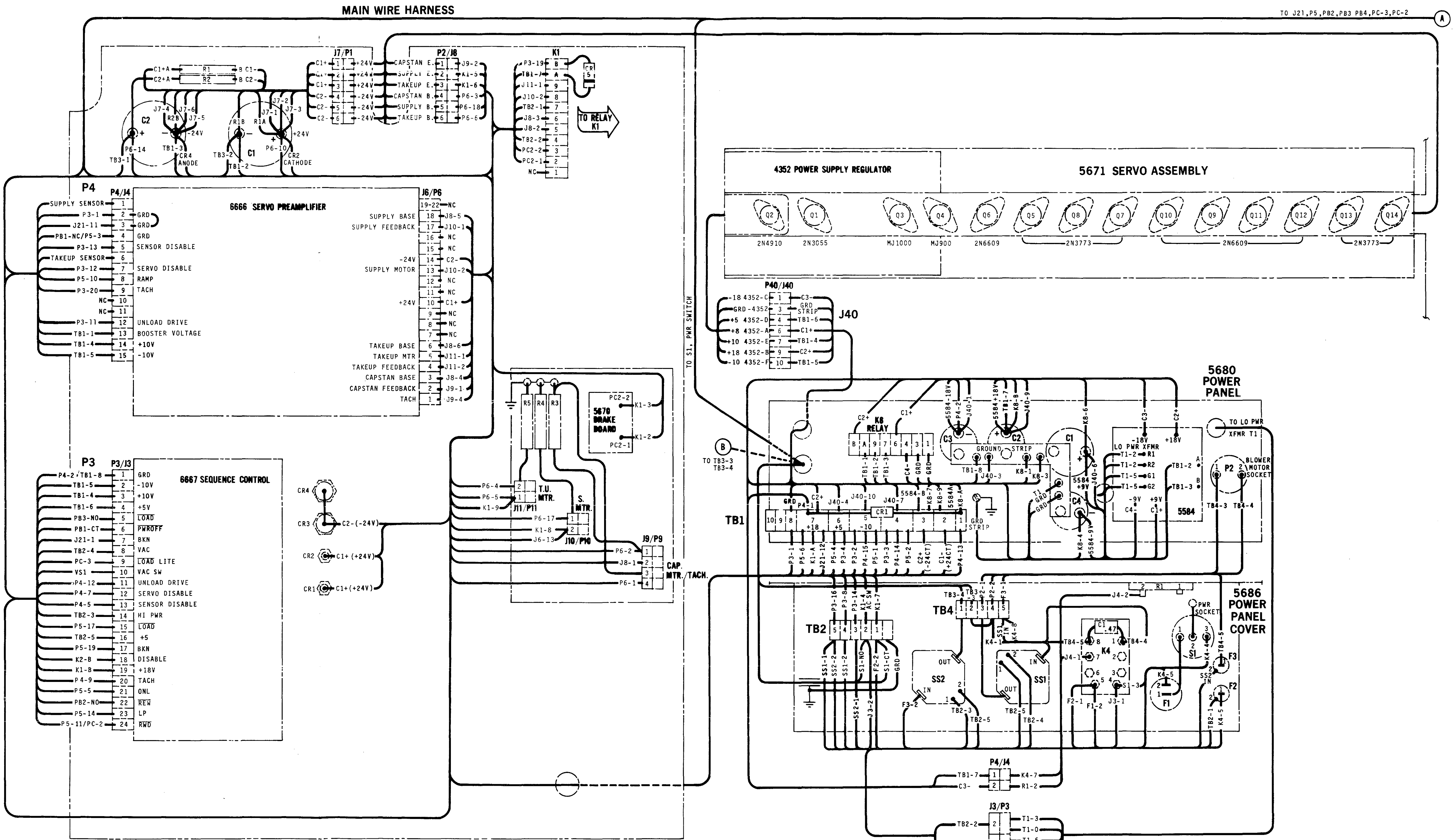
14. Some schematics of modules include certain external elements which aid in understanding the circuit function. In this case all the connections to the element may not be shown in the interest of clarity.

15. 

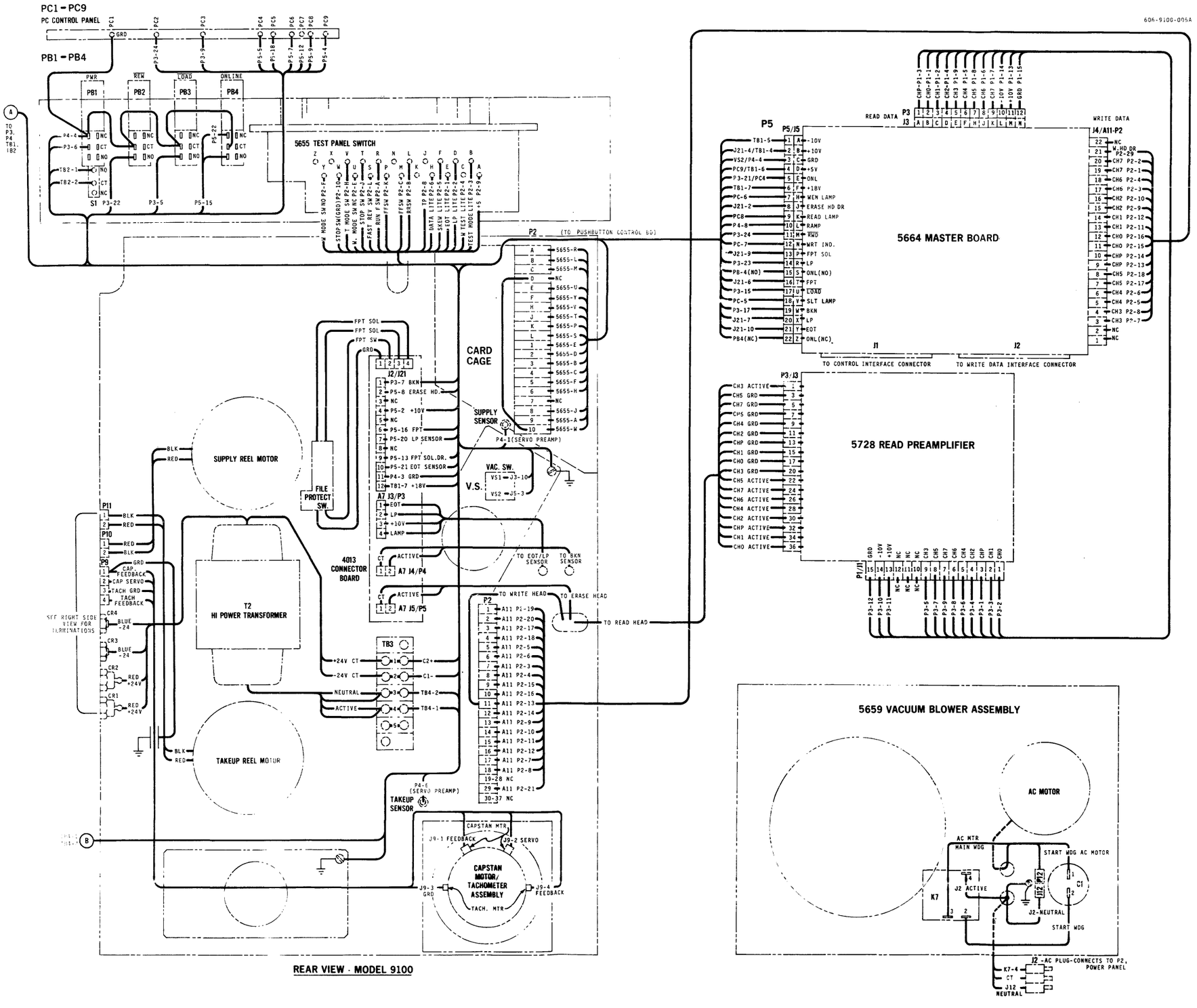
designates a test point provided on the module. Letters proceed from top to bottom of card with the ground test point, if present, as the bottommost terminal.

16. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. These are the designations on the socket. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

606-9100-004B

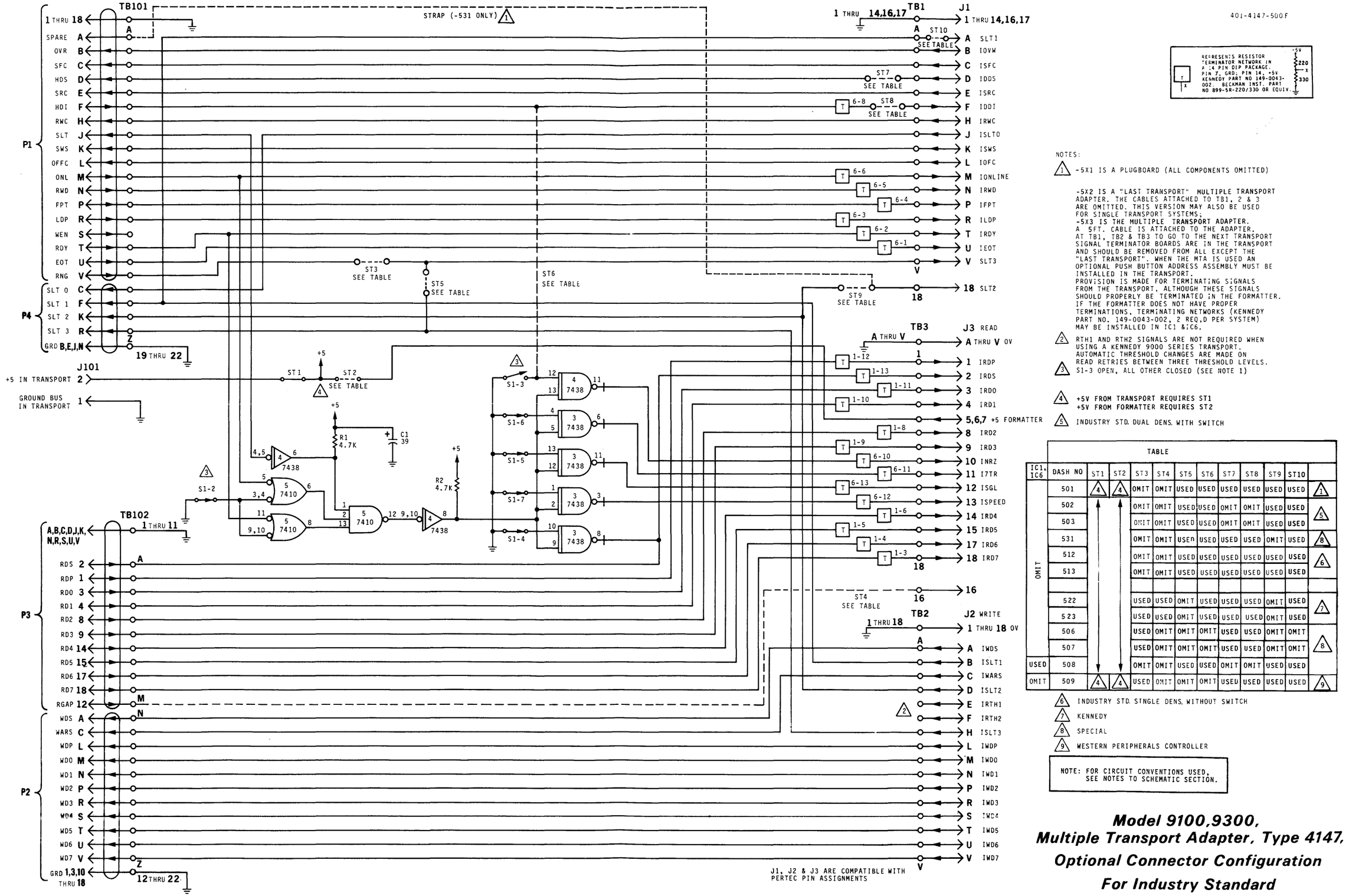


RIGHT SIDE VIEW - MODEL 9100



REAR VIEW - MODEL 9100

401-4147-500F



REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V. KENNEDY PART NO 149-0043-002. BECKMAN INST. PART NO 899-5R-220/330 OR EQUIV.

NOTES:

1. -5X1 IS A PLUGBOARD (ALL COMPONENTS OMITTED)

   -5X2 IS A "LAST TRANSPORT" MULTIPLE TRANSPORT ADAPTER. THE CABLES ATTACHED TO TB1, 2 & 3 ARE OMITTED. THIS VERSION MAY ALSO BE USED FOR SINGLE TRANSPORT SYSTEMS;
   -5X3 IS THE MULTIPLE TRANSPORT ADAPTER. A 5FT. CABLE IS ATTACHED TO THE ADAPTER. AT TB1, TB2 & TB3 TO GO TO THE NEXT TRANSPORT SIGNAL TERMINATOR BOARDS ARE IN THE TRANSPORT AND SHOULD BE REMOVED FROM ALL EXCEPT THE "LAST TRANSPORT". WHEN THE MTA IS USED AN OPTIONAL PUSH BUTTON ADDRESS ASSEMBLY MUST BE INSTALLED IN THE TRANSPORT.
   PROVISION IS MADE FOR TERMINATING SIGNALS FROM THE TRANSPORT, ALTHOUGH THESE SIGNALS SHOULD PROPERLY BE TERMINATED IN THE FORMATTER. IF THE FORMATTER DOES NOT HAVE PROPER TERMINATIONS, TERMINATING NETWORKS (KENNEDY PART NO. 149-0043-002, 2 REQ,D PER SYSTEM) MAY BE INSTALLED IN IC1 &IC6.

2. RTH1 AND RTH2 SIGNALS ARE NOT REQUIRED WHEN USING A KENNEDY 9000 SERIES TRANSPORT. AUTOMATIC THRESHOLD CHANGES ARE MADE ON READ RETRIES BETWEEN THREE THRESHOLD LEVELS.
3. S1-3 OPEN, ALL OTHER CLOSED (SEE NOTE 1)
4. +5V FROM TRANSPORT REQUIRES ST1
   +5V FROM FORMATTER REQUIRES ST2
5. INDUSTRY STD. DUAL DENS. WITH SWITCH

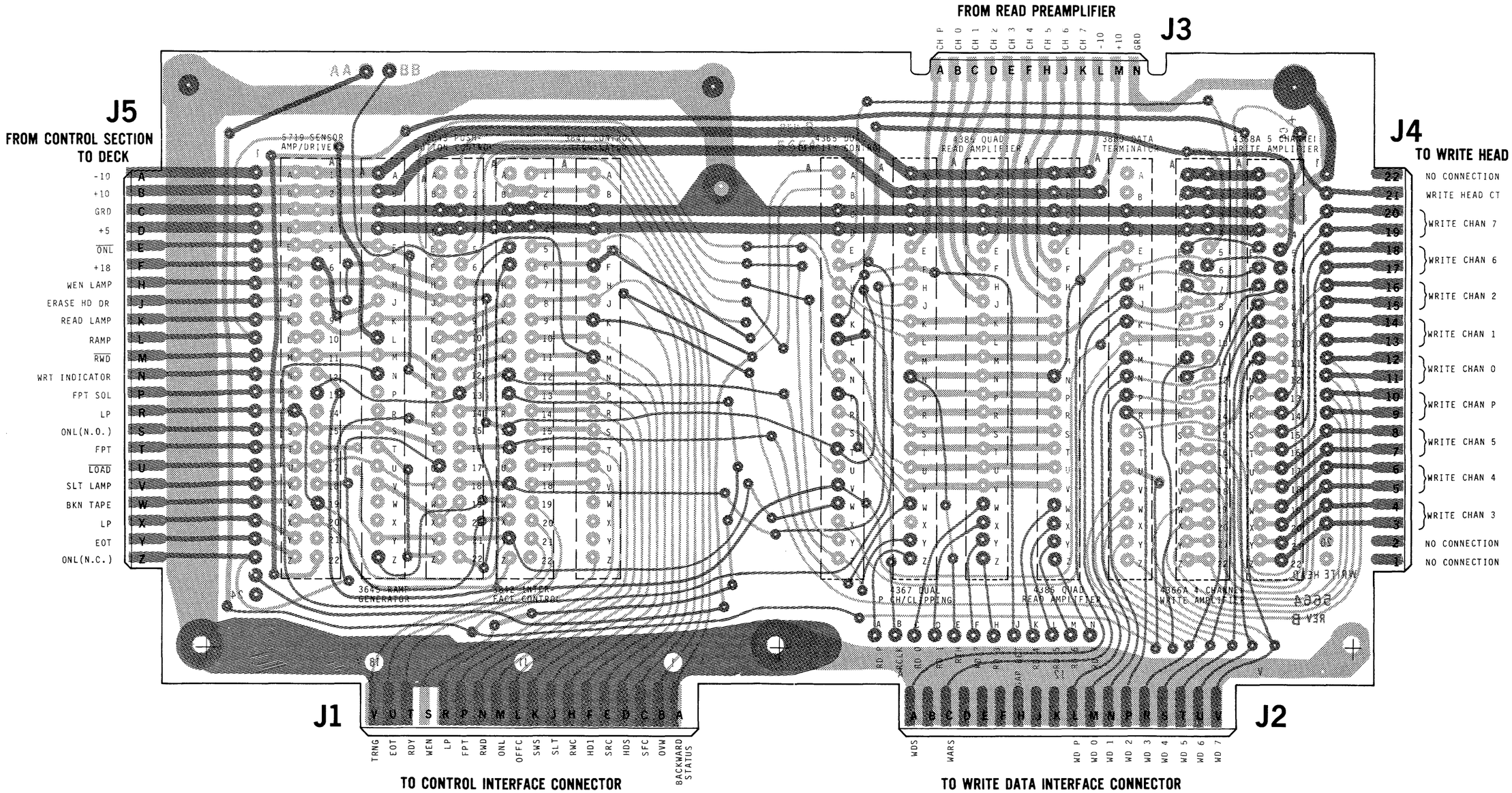
TABLE

IC1, IC6	DASH NO	ST1	ST2	ST3	ST4	ST5	ST6	ST7	ST8	ST9	ST10	
OMIT	501	4	4	OMIT	OMIT	USED	USED	USED	USED	USED	USED	1
	502			OMIT	OMIT	USED	USED	OMIT	OMIT	USED	USED	5
	503			OMIT	OMIT	USED	USED	OMIT	OMIT	USED	USED	
	531			OMIT	OMIT	USED	USED	USED	USED	OMIT	USED	8
	512			OMIT	OMIT	USED	USED	USED	USED	USED	USED	6
	513			OMIT	OMIT	USED	USED	USED	USED	USED	USED	
	522			USED	USED	OMIT	USED	USED	USED	OMIT	USED	7
	523			USED	USED	OMIT	USED	USED	USED	OMIT	USED	
	506			USED	OMIT	OMIT	OMIT	USED	USED	OMIT	OMIT	8
	507			USED	OMIT	OMIT	OMIT	USED	USED	OMIT	OMIT	
USED	508			OMIT	OMIT	USED	USED	OMIT	OMIT	USED	USED	
OMIT	509	4	4	USED	OMIT	OMIT	OMIT	USED	USED	USED	USED	9

6. INDUSTRY STD. SINGLE DENS. WITHOUT SWITCH
7. KENNEDY
8. SPECIAL
9. WESTERN PERIPHERALS CONTROLLER

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Model 9100,9300, Multiple Transport Adapter, Type 4147, Optional Connector Configuration For Industry Standard



410-4019

INDICATES NEAR SIDE OF CIRCUIT BOARD AS VIEWED FROM REAR OF TRANSPORT

INDICATES FAR SIDE OF CIRCUIT BOARD AS VIEWED FROM REAR OF TRANSPORT

Masterboard Assembly, Type 5664,

MODEL 9100 POWER SUPPLY

CIRCUIT DESCRIPTION

Besides providing the regulated and unregulated voltages required to operate the tape transport electronics, the power supply contains several switches and relays required for controlling the sequence of operation. Separate low voltage and high voltage power transformers are used. All regulated voltages are derived from the low power transformer. Output from the high voltage transformer is supplied to the reel servos and capstan servos.

SEQUENCE OF OPERATION

When the power switch pushbutton on the front panel is pressed, plus and minus 18 vdc from transformer T1's full wave bridge actuates relay K4, switching ac to solid state switches SS1 and SS2. However, no ac can reach the vacuum blower motor until relays K5 and K6 are actuated to make the switch Triacs conductive. This happens when the LOAD pushbutton is pressed. SS1 will now provide power to the vacuum blower motor, while SS2 supplies ac to the high voltage transformer, T2.

HIGH SPEED RELAY K8

During fast forward or rewind modes, plus and minus 32 vdc is required to run the reel motors for 200 ips high speed operation. To develop this voltage, high speed relay K8 is closed by amplified output from the capstan tachometer whenever motor speed exceeds 130 ips. (See high speed relay output signal on the Servo System schematic.)

Plus 8 vdc and minus 8 vdc is now applied to the secondary center taps of the high voltage transformer. This transformer's output voltage now increases from plus and minus 24 vdc to plus and minus 32 vdc for high speed operation.

SERVO ENABLE RELAY K1

Connected in parallel with power switch SW1, this relay remains closed for some time after power is shut off. This permits the sequence control to finish the command sequence required for shutting down the tape transport.

TYPE 4352 POWER SUPPLY REGULATOR

This circuit develops +10 vdc, -10 vdc, and +5 vdc regulated voltage from the +18 vdc, -18 vdc, and +8 vdc unregulated voltages developed by transformer T1's two full wave bridges.

+10 VOLT REGULATOR

Pass transistor Q3 is fed from +18v and its base is driven by a monolithic regulator IC2. Voltage output is determined by R8 and R9. Q7 and Q8 control power supply tracking when powering down. As +18v drops owing to discharge of C1, Q8 cuts off at approximately 13 volts on the +18v line. When this happens Q7 is turned on shorting out R9 and dropping the regulator reference voltage to zero. The +10v output is cut off and drops to zero. Since +10v is the reference for -10v, -10v also drops to zero. This action occurs before the +5v supply has dropped sufficiently to cause indeterminate logic states; turn-off transient motions are prevented.

-10 VOLT REGULATOR

The -10v supply is regulated by pass transistor Q4 driven by Q6. Its reference is +10v as determined by R13, R14. In this way the two regulated voltages are made to track each other.

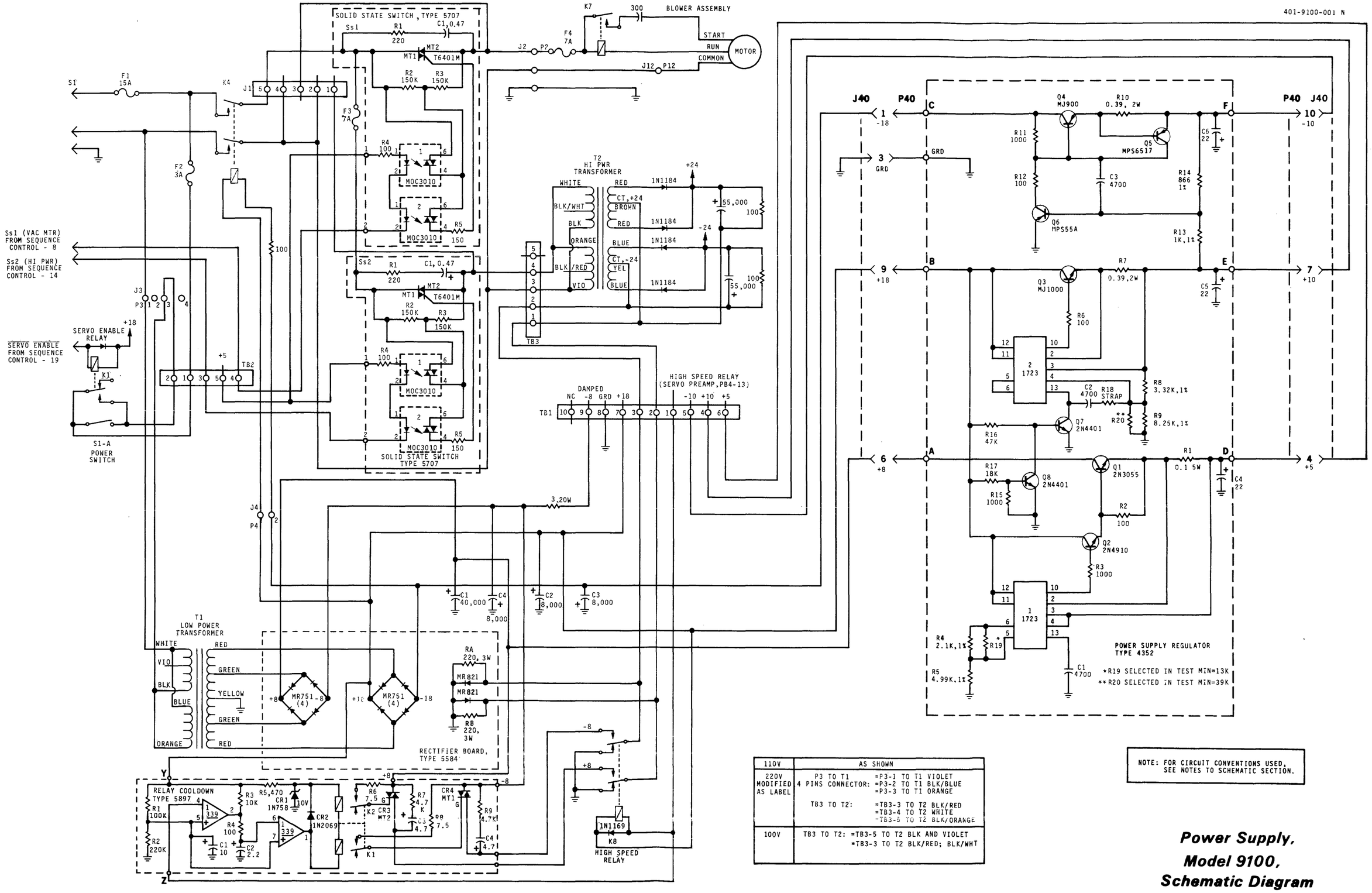
+5 VOLT REGULATOR

An integrated circuit regulator IC1 controls +5v output in conjunction with pass transistor Q1 and driver Q2. Output voltage is set by R4, R5. The internal circuitry of IC1, IC2 consists of a differential amplifier with built-in zener reference, together with facilities for short circuit protection. Q2 assures that sufficient base drive is available for Q1.

SHORT CIRCUIT PROTECTION

Drop-through series resistors, for example R10 in the -10v supply, provide short circuit protection. If the drop across R10 exceeds approximately 0.6v, Q5 is turned on, connecting Q4 base to emitter and cutting off Q4. This corresponds to approximately 1.5 amperes under short circuit conditions. Similar circuits are provided in IC1 and IC2.

401-9100-001 N



110V	AS SHOWN
220V MODIFIED AS LABEL	P3 TO T1 4 PINS CONNECTOR: =P3-1 TO T1 VIOLET =P3-2 TO T1 BLK/BLUE =P3-3 TO T1 ORANGE TB3 TO T2: =TB3-3 TO T2 BLK/RED =TB3-4 TO T2 WHITE =TB3-5 TO T2 BLK/ORANGE
100V	TB3 TO T2: =TB3-5 TO T2 BLK AND VIOLET =TB3-3 TO T2 BLK/RED; BLK/WHT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Power Supply, Model 9100, Schematic Diagram

TYPE 3842 INTERFACE CONTROL

CIRCUIT DESCRIPTION

This module contains a set of receivers for the interface control commands:

SYNCHRONOUS FORWARD SFC
SYNCHRONOUS REVERSE SRC
OVERWRITE OVW
REWIND RWC
SELECT SLT
SET WRITE STATUS SWS
OFF LINE OFFC

It also contains drivers that return the recorder status outputs to the interface:

ON LINE ONL
REWINDING RWDG
FILE PROTECT FPT
LOAD POINT LP
WRITE ENABLE WEN
READY RDY
END OF TAPE EOT
TAPE RUNNING TNG

Certain controls and delays are also provided to ensure proper tape motion and transport operation.

TAPE MOTION CONTROLS

The motion control commands from the interface, SFC and SRC, are translated on this card into the internal motion commands of the transport — RUN NORMAL $\overline{\text{RNN}}$, FORWARD $\overline{\text{FWD}}$, and REVERSE $\overline{\text{RVS}}$. These internal motion commands are supplied to the Pushbutton Control module, where they are combined with commands supplied from the transport pushbuttons and internal interlocks to generate the commands that initiate actual tape motion on the Ramp Generator module.

On this module SFC and SRC are supplied to an interlocking network that ensures that the tape comes to a stop before its direction of motion is reversed. The interlocking network includes flip-flop IC1-3, edge circuits IC2-6 and IC2-8, NAND gate IC3-6, and interlocking flip-flop IC3-10. Whenever flip-flop IC1 changes states due to a change in the direction of motion, for example from a reverse command SRC to a forward command SFC, its output generates a pulse through the edge circuits consisting of inverters IC2 and the associated capacitors. The pulse is gated through IC3-6 to the set input of interlocking flip-flop IC3-10. The flip-flop can be set only if TAPE RUNNING $\overline{\text{TNG}}$ is true, indicating that the tape is still moving. In this case $\overline{\text{TNG}}$ low at input pin W is inverted by IC18-12 and supplies a high input to the clear of IC3. The flip-flop can then be set by the pulse on its set input, its 0 output going low. The 0 output of IC3 then inhibits the RUN NORMAL gate IC15 at pin 2, setting RUN NORMAL $\overline{\text{RNN}}$ false. After the tape has ramped down to a stop, TAPE RUNNING $\overline{\text{TNG}}$ goes false, clearing interlocking flip-flop IC3, whose output then enables the RUN NORMAL gate. RUN NORMAL $\overline{\text{RNN}}$ then goes true if the following conditions are satisfied: SELECT SLT1 is true, indicating that the transport is on line and selected by the interface; BUSY $\overline{\text{BSY}}$ is false, indicating the transport is not rewinding or searching for load point; and SRC command is not given at load point. (This would activate NAND gate IC15-8 and would disable the RUN NORMAL gate at IC15-1.) If the above conditions are satisfied, RUN NORMAL $\overline{\text{RNN}}$ goes true at output pin V, and is supplied to the Pushbutton Control module where it initiates tape motion at the normal running speed. The direction of motion is determined by the state of flip-flop IC1. If a forward command SFC has been given, the flip-flop is set and its 1-output enables NAND gate IC14-8, provided that SLT1 is true and $\overline{\text{BSY}}$ is false. This generates FORWARD $\overline{\text{FWD}}$ true at output pin U. If a reverse command SRC has been given, flip-flop IC1 is cleared and enables NAND gate IC14-6, generating REVERSE $\overline{\text{RVS}}$ true, providing SLT1 is true, $\overline{\text{BSY}}$ is false, and LOAD POINT LP is false. No interface reverse command is acknowledged by the transport when the load point is detected.

WRITE SELECT

During a write operation the interface supplies SET WRITE STATUS SWS true at pin K; SWS is inverted by IC9-4 and is supplied to the D input of flip-flop IC7. The flip-flop is toggled provided that the transport is selected and on line, after NOR gate IC1-11 is activated by a synchronous motion command. This would activate NAND gate IC1-8 and trigger one-shot IC4-1, generating a 2 μsec pulse. On the trailing edge of the pulse the $\overline{\text{Q}}$ output of the one-shot toggles IC7-3, the Q output of the flip-flop going high and activating NAND gate IC10-11, generating WRITE SELECT WSEL true at output pin H. During an overwrite operation OVERWRITE OVW true is inverted by IC18-8 and sets the D input of flip-flop IC7-12

high. On the trailing edge of the pulse generated by one-shot IC4-4 the flip-flop is set and enables NAND gate IC8-12. One-shot IC4-4 also direct-sets flip-flop IC11, whose Q output enables the overwrite gate at IC8-9. If write status is true, the gate is enabled at IC8-13 and it is kept activated as long as a synchronous motion command is activating NAND gate IC1-8. IC8-8 then goes low and supplies $\overline{\text{WSEL}}$ for the duration of the motion command only. When a WRITE AMPLIFIER RESET pulse is given at pin P, it toggles flip-flop IC11 to the cleared state and disables the overwrite gate.

REWIND FLIP-FLOP

When a REWIND COMMAND RWC is given by the interface, it sets the rewind flip-flop IC5-3, provided that the transport is selected, on line, and not at load point. The 1-output of the flip-flop then goes high, generating REWINDING RWDG true to the interface, and a rewind command $\overline{\text{RWC1}}$ through an edge circuit consisting of inverter IC6-6, NAND gate IC6-8, and capacitor C5. $\overline{\text{RWC1}}$ is supplied to the Pushbutton Control module. The flip-flop is cleared when the tape returns to and stops at load point, or when BROKEN TAPE BKN is detected.

END OF TAPE

An end of tape indication is set when the EOT marker is encountered in forward direction and remains set until the marker is passed in the reverse direction.

A true EOT signal at pin Z if machine status is $\overline{\text{RWDG}}$ (IC10-5, 8) and $\overline{\text{RVS}}$ (IC14-6) causes IC11 to be preset by IC19-8. An EOT status is then signaled at the interface by IC16-3.

Upon passing the EOT marker in the reverse direction IC13-3 is high and the EOT signal clocks IC11 clear on the trailing edge of the EOT signal dropping the EOT signal at the interface. IC11 is preset to the clear state by BKN signal at pin X.

OUTPUT STATUS

Most status gates on this module are preconditioned by SELECT and ON LINE being true; consequently, the transport returns status indications only when it is selected and on line. The READY status is generated when BUSY $\overline{\text{BSY}}$ supplied from the Pushbutton Control module is false and the transport is not rewinding. The LOAD POINT output is also preconditioned by the rewinding status being false. The only status gate not preconditioned is the rewind via the REWIND pushbutton. If the pushbutton is used to rewind, that status is made available to the interface without being selected and on line.

401-3842-001K

CONTROL TERMINATOR CARD, 3841

WARS1 (FROM WA1-M)

CONTROL INTERFACE CONNECTOR J1

OVW B — OVW (IC 7-12)

SFC C — SRC E

RWC H — SLT J — SWS K

OFFC L — ONL M — RWDG N — FPT P — LDP R — WEN S — RDY T — EOT U — TNG V

BACKWARD STATUS

WRITE STATUS

ST1 STRAP — ST2 OMIT — ST3 OMIT — ST4 OMIT

ST5 — SEE TABLE — ST6 — SEE TABLE — CT1 SEE TABLE

LP (IC18-6) — TNG (PIN W) — LP (PIN Y) — ONL (PIN R) — BSY (PIN N) — TNG (PIN W)

R1 4.7K — R2 4.7K — R3 4.7K — R4 220 — R5 330

C1 100 — C2 100 — C3 2000 — C4 1000 — C5 2000 — C6 100

CR1 OMIT — CR2 1N270

OVW (IC18-8)

CONTROL TERMINATOR CARD HAS TERMINATORS (T) 220-330 OHM AND PULL-UPS (P) 4.7K AS SHOWN

DASH NO.	CT1	ST5	ST6
001H	NO CUT	OMIT	OMIT
004	SEE SEPARATE SCHEM.		
005	SEE SEPARATE SCHEM.		
006A	CUT	OMIT	ADD

D +5V

C GRD

W TNG (FROM RAMP GENERATOR-Z)

V RNN (TO PUSHBUTTON CONTROL-18)

U FWD (NOT USED)

T RVS (TO PUSHBUTTON CONTROL-16)

N BSY (FROM PUSHBUTTON CONTROL -13)

S WRDY (FROM PUSHBUTTON CONTROL-J)

F SLT1 (TO (A10J4-W CONTROL MB; SENSOR AMPL DRIVER-Z)

K REWIND LAMP (FROM PUSHBUTTON CONTROL-L)

Y LP (FROM SENSOR AMP/DRIVER-19)

L RWC1 (TO PUSHBUTTON CONTROL-M)

M OFFC1 (TO PUSHBUTTON CONTROL-12)

H WSEL (TO PUSHBUTTON CONTROL-7)

R ONL (FROM PUSHBUTTON CONTROL-14)

X BKN (FROM SENSOR AMP/DRIVER-18)

Z EOT1 (FROM SENSOR AMP/DRIVER-X)

J FPT (FROM SENSOR AMP/DRIVER-9)

E EOT2 (TO PUSHBUTTON CONTROL-22)

Interface Control, Type 3842, Schematic Diagram

TYPE 4842 INTERFACE PC BOARD
CIRCUIT DESCRIPTION

This board contains receivers and gating circuits for developing tape transport commands from incoming controller commands. It also contains line drivers for outputting tape transport status commands to the controller. In addition, type D flip-flop IC10 outputs EBDIS/, the Erase Bar Disable signal required during tape editing.

Tape Motion Control Circuitry

SFC, SRC, FAST tape motion commands from the controller are translated into internal tape transport motion commands RNN/, RNF/ and RVS/ by quad 2x1 multiplexer IC15. These internal commands are supplied to the Pushbutton Control module where they are combined with commands from the transport pushbuttons and the internal interlocks to develop the actual tape motion commands issued to the transport's Ramp Generator PC board.

SRC, SFC and FAST are supplied to an interlocking network on this PC board to insure that tape motion ceases prior to accepting a new direction command. The interlock network consists of a high frequency sampling oscillator (IC11 and related components), and a directional interlock flip-flop (IC14 and related components) to select and generate the appropriate RUN NORMAL, RUN FAST and REVERSE signals required by the transport. The oscillator monitors the state of TNG/ (Turning) signal. This signal disables oscillator output when the capstan is turning and enables oscillator output when tape and capstan motion ceases.

Table 1 indicates the controller inputs and interface board outputs required to initiate a given tape motion.

To generate RNN true for forward tape motion, SFC (Synchronous Forward Command) from the controller must be true. This is supplied to the D input of interlock flip-flop IC14 and pin 3 of multiplexer IC15. After capstan motion ceases, TNG/ goes false, enabling the high frequency oscillator at IC11, pin 3 to clock out Q high at IC14-5. This is applied to multiplexer IC15-1 to select its B inputs. Since SFC high is applied to the 1B input of the multiplexer, the output at IC15-4 goes high. This is inverted low at inverter IC16-11 to produce RNN/ (Run Normal) true at pin V.

Should the Synchronous Reverse Command (SRC) be issued to the transport, it will not be able to produce a RVS/ transport command until capstan rotation ceases. SRC true is gated with LP/ false to enable IC6-6. IC6-6 high is applied to inputs 1A and 2A of the multiplexer. After tape motion stops, TNG/ false enables the sampling oscillator, clocking the Q output of IC15-5 low, since SFC would now be low false after inversion at IC14. IC15-1 of the multiplexer goes low, selecting the A multiplexer inputs. IC15-4 again goes high to issue RNN/ true at pin V IC15-7 also goes high and is inverted low at IC16-3 to produce RVS/ true.

Fast forward tape motion does not require a stopped tape, if a direction change is not required since the requisite RNN true is routed back to pin 11 of the multiplexer IC and output whenever the A inputs are selected by IC14-5 low. IC15-9 goes high at this point, making NAND gate IC16-10 high. FAST true from the interface will enable IC16, which outputs RNF/ true at pin U. RNN/ at pin V will also be true as required by the ramp generator for fast forward tape motion. When the End of Tape mark is reached, EOT/, connected to pin 10 of the multiplexer, will go low true, causing IC15-9 to go low to disable a run fast operation (now being interpreted as normal run).

Fast reverse tape operation is initiated by generating RNN/ true, RNF/ true and RVS/ true. Thus, the controller must issue SRC true and FAST true. After capstan rotation ceases and TNG/ goes false, Q low is clocked out of IC14-5, selecting the B multiplexer inputs. Then RNN/, RNF/ and RVS/ at pins V,U and T all go low true.

Tape motion will be disabled whenever BSY true or SLT/ false signals are issued. This would disable NAND gate IC3-6, resulting in a high false STROBE signal at IC15-15, which disables all multiplexer outputs.

Tape Mode		Controller Command	Interface PCB Output
Forward	=	SFC true	RNN/true
Reverse	=	SRC true	RNN/true + RVS/true
Fast Forward	=	SFC true + FAST true	RNN/true + RNF/true
Fast Reverse	=	SRC true + FAST true	RNN/true + RNF/true + RVS/true

Table 1

Write Select

Control of the write amplifier is performed by SWS (Set Write Status), OVW (Overwrite) and internally generated WARS1 (Write After Read Strobe) signals which generate WSEL/ (Write Select) and EBDIS/ (Erase Bar Disable). WSEL/ and EBDIS/ are output to the sensor amplifier and pushbutton control cards.

A sampling scheme is employed to permit the interface to issue tape motion and WSEL commands simultaneously. RNN/ true and RNN true are delayed 16 and 8 usec respectively by RC networks R8/C1 and R9/C2 prior to being applied to Schmitt trigger NAND gate IC13. As a result, IC13-8 outputs an approximate 8 usec low clockpulse to the sampling flip-flops and the preset of IC8. Thus the write commands are sampled 15 to 20 usec after the leading edges of the tape motion commands, allowing the controller to output tape motion and write amplifier commands simultaneously.

Set Write Status (SWS) true is loaded into the D input at IC10-12 from 15 to 20 usec after RNN goes true. SWS high true and EBDIS high false are applied to AND/OR inverter IC9 at pins 9,10 and 11, producing WSEL/ true at IC9-8. OVW will be false during a normal write operation.

Note that WSEL/ is not reset on termination of a motion command; instead it is only sampled at the beginning of a motion command. This avoids potential glitches from being written while writing consecutive blocks, since the write amplifier is not being constantly turned on and off during this operation.

Overwrite

Overwriting or editing is performed by backspacing over the block to be rewritten to determine its exact length then presenting OVW true and SWS true concurrent with the beginning of a run command. This sets the Q outputs at IC10-9 low false and IC10-5 true. Reset flip-flop IC8-9 is also set high true. AND/OR inverter 9 is enabled, outputting WSEL/ true for the duration of the overwrite operation. Note that Erase Bar Disable (EBDIS/) true is output to the sensor amplifier from pin 18 during an overwrite operation which disables (turns off) the upstream erase bar.

After a block is written in NRZI format, WARS goes true at the write amplifier to produce an LRC character; then WARS1 true is issued to the interface, toggling IC8-9 false to disable Write Select and turn off the write current before writing can continue into the next data block.

Rewind and Unload

The rewind status flip-flop is a SR flip-flop IC7 and related circuitry. A Rewind Command (RWC) is accepted whenever the tape is not at load point (LP false). IC7-8,2 go high, causing RWDG true status signal to be output to the interface through driver IC5-6. Simultaneously a 5 usec RWC1/ true pulse is output from Schmitt trigger NAND gate IC11-11. RWC1 is output to the Pushbutton Control PC board to set the REWIND flip-flop. The pushbutton control card then issues a RWDG1 true level which is applied to IC7-10 to keep the rewind status flip-flop set.

When the tape rewinds to loadpoint (LP true) and capstan motion ceases (TNG/ true), or a broken tape is detected (BKN true), the rewind status flip-flop is cleared. IC7-11,12 goes high, which is applied to AND gate IC6-12. If the unit is selected, online, and not busy, IC6 and IC13 will be enabled to return a RDY true status signal to inform the interface that the transport is ready for the next data and/or tape motion command.

During an unload operation, the tape is slowly rewound off the takeup reel. To accomplish this, UNLD/ true is issued from the controller. UNLD/ true is inverted high at IC4-12; then gated with SLT SLT and ONL, or just UNLD/ itself. (This is determined by the strapping of ST1/ST2: See table on schematic.) The high output at IC6-8 is inverted low by IC4, then used to set unload flip-flop IC8 at pin 4. IC8-5 high is gated at IC11 with IC7-11,12 high, which indicates the transport is not rewinding. IC11-6 outputs UNLOAD/ true for vacuum column 9100/9300 transports. Strap ST5 is connected on interface PC boards used in 9100/9300 transports to output UNLOAD/ true to the Sequence Control PC board through pin 7.

With strap ST3 installed, RVS and RNN/ true signals are output to the Pushbutton Control PC board on 9000/9700 transport through pins V and T. A BKN true status signal will clear both the rewind status and unload flip-flops, when the tape completely unloads.

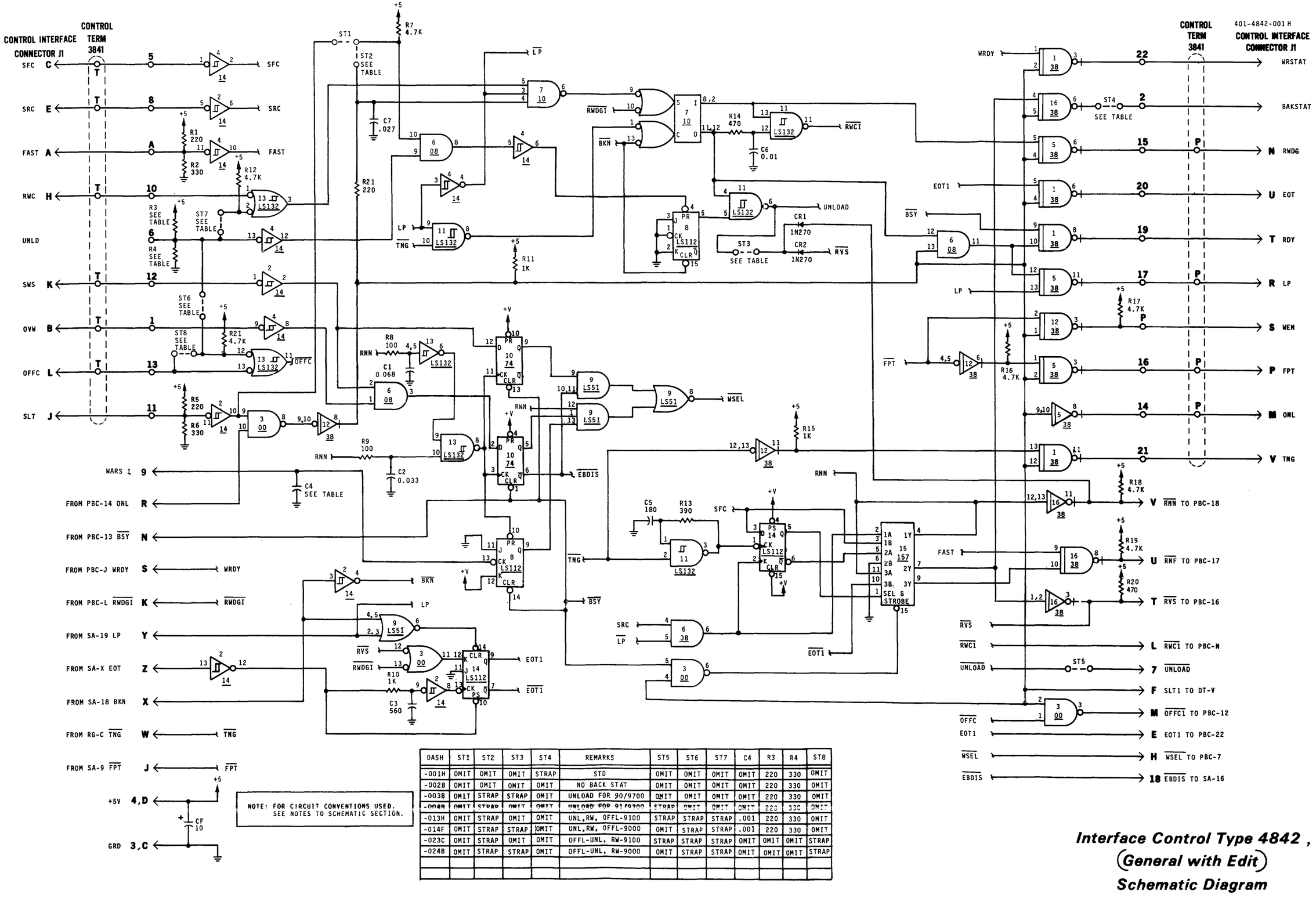
Diodes CR3/CR4 at pins 10 and 12 cause UNLD/ true from the interface to initiate a rewind operation if the tape was not already at load point. The tape drive will also be taken offline (OFFC true). RC network R21/C7 delays SLT and ONL true signals 4 to 6 usec to insure correct timing during this combination unload-rewind-offline operation.

EOT Flip-Flop

IC14 is the EOT flip-flop which outputs EOT1 high true status signal to the Pushbutton Control PC board whenever the EOT tab has been detected. EOT true also is gated with SLT and ONL true at IC1, then returned to the interface via pin U as EOT. EOT low false trailing edge from the Sensor Amplifier clears IC14 by clocking the flip-flop if and only if a reverse motion command is initiated. (EOT is delayed by R10/C3 for TTL timing considerations.) EOT1 at IC14-8 now goes false. Load Point true or Broken Tape true, which are applied to preset pin 10, will also clear the EOT flip-flop.

Status Gates

All status gates on this PC board are preconditioned by SLT and ONL being true. The gating of these signals is self-explanatory.



DASH	ST1	ST2	ST3	ST4	REMARKS	ST5	ST6	ST7	C4	R3	R4	ST8
-001H	OMIT	OMIT	OMIT	STRAP	STD	OMIT	OMIT	OMIT	OMIT	220	330	OMIT
-002B	OMIT	OMIT	OMIT	OMIT	NO BACK STAT	OMIT	OMIT	OMIT	OMIT	220	330	OMIT
-003B	OMIT	STRAP	STRAP	OMIT	UNLOAD FOR 90/9700	OMIT	OMIT	OMIT	OMIT	220	330	OMIT
-004B	OMIT	STRAP	OMIT	OMIT	UNLOAD FOR 91/9300	STRAP	OMIT	OMIT	OMIT	220	330	OMIT
-013H	OMIT	STRAP	OMIT	OMIT	UNL,RW, OFFL-9100	STRAP	STRAP	STRAP	.001	220	330	OMIT
-014F	OMIT	STRAP	STRAP	OMIT	UNL,RW, OFFL-9000	OMIT	STRAP	STRAP	.001	220	330	OMIT
-023C	OMIT	STRAP	OMIT	OMIT	OFFL-UNL, RW-9100	STRAP	STRAP	STRAP	OMIT	OMIT	OMIT	STRAP
-024B	OMIT	STRAP	STRAP	OMIT	OFFL-UNL, RW-9000	OMIT	STRAP	STRAP	OMIT	OMIT	OMIT	STRAP

Interface Control Type 4842 ,
(General with Edit)
Schematic Diagram

MODEL 9100 TAPE MOTION CONTROLS

CIRCUIT DESCRIPTION

This schematic shows the Type 5665 Main Control Panel and the Type 3843 Pushbutton Control card, as well as blocks of the Sequence Control, Interface Control and Test Panel Switch to illustrate the interconnections between these modules and the other tape motion control circuitry.

The Pushbutton Control card and the Sequence Control contain the circuitry required to perform the motion commands issued from the Interface Connector or by the Main Control Panel pushbuttons. The Pushbutton Control card generates RUN NORMAL RNN1, RUN FAST, RNF1, and REVERSE (RVS1) which are supplied to the Ramp Generator. Here the tape motion signal from the Pushbutton Control card is converted to an analog voltage for controlling the capstan servo on the Type 5666 Servo Preamplifier module.

The ON LINE pushbutton on the Main Control Panel is connected to the ON LINE flip-flop on the Pushbutton Control card. The LOAD and REWIND pushbuttons are processed by the Sequence Control prior to being applied to their respective flip-flops on the Pushbutton Control board as negative true signals.

LOADING

When LOAD true is output from the Sequence Control, it grounds the input to inverter IC12-1, setting the LOAD flip-flop consisting of NOR gate IC13-6 and inverter IC12-1. Once the LOAD flip-flop is set IC13-6 goes low. This signal is inverted at IC12-4 to remove the direct-clear from ON LINE flip-flop IC10-3. Thus the ON LINE flip-flop can be set only after the transport has been loaded. When the ON LINE pushbutton is activated the first time, it toggles IC10-1 to the set, or ON LINE, position. The ON LINE flip-flop can be cleared by pressing the front panel pushbutton a second time, or by an interface OFF LINE COMMAND (OFFC1) supplied from the interface control module.

The REWIND pushbutton can be activated only when the transport is off line. When activated, the REWIND pushbutton sets the flip-flop consisting of gates IC8-8 and IC8-6, provided that the transport is loaded at the time and test mode is not selected. Consequently the transport cannot be rewound by the pushbutton during test mode, or when on line, or when LOAD is false.

When the transport is on line the REWIND flip-flop can be set by interface REWIND COMMAND ($\overline{\text{RWC1}}$) true, supplied from the interface control module.

The output of the REWIND flip-flop, REWINDING (RWDG1), activates NOR gates IC15-8 and IC14-6, generating RNF1 and RVS1 true to the ramp generator module to initiate a fast reverse motion to load point. When load point is detected the photosensor amp driver module supplies LPPULSE true to input pin H of the Pushbutton Control module, clearing the REWIND flip-flop.

ADVANCING TAPE TO LOAD POINT

The ON TAPE flip-flop, IC10, locates tape position. Before the tape is loaded, the flip-flop is cleared by $\overline{\text{LOAD}}$ false, which is inverted low by IC12-2 at IC10-8. When the transport is loaded the direct-clear is removed and NAND gate IC14-11 goes high. Since the ON TAPE flip-flop is still cleared, its $\overline{Q}$ output high activates NAND gate IC14-8, generating RUN NORMAL (RNN1) at output pin Y to advance tape to load point. When the load point marker is detected, LP true from the photosensor module is gated through IC16-3 and direct-sets flip-flop IC10-7 to the ON TAPE state, terminating the tape motion. Similarly, when load point is detected during reverse tape motion, the ON TAPE flip-flop is toggled by NAND gate IC16-11 to the clear state, initiating forward tape motion back to load point.

BUSY

This module generates a BUSY output when the tape is not loaded, when it is advancing to load point, or when the transport is off line and not in test mode. In any of these cases NOR gate IC4-8 is activated and supplies BSY true through IC5-2 to the Interface Control module.

WRITE READY

WRITE READY true is generated in two different cases: when the interface supplies WRITE SELECT true and the transport is not in test mode ($\overline{\text{TM}}$ false), or when the transport is in the write test mode and flip-flop IC6-14 is set. In either case NOR gate IC1-8 is activated, enabling NAND gate IC4-5. The gate is activated provided that BUSY ($\overline{\text{BSY}}$) is false, FILE PROTECT ($\overline{\text{FPT}}$) is false, and the transport is not in reverse motion (RVS1 is false). IC4-6 then

goes low, is inverted by IC5-12 and generates WRDY true at output pin J to the Write Amplifier module.

TEST PANEL CONTROL

In order to activate the test panel the transport must be off line, and the test panel STOP pushbutton must be depressed. In that case the TEST MODE pushbutton on the test panel can be activated, setting the flip-flop consisting of inverters IC11-8 and IC11-10, which in turn toggles the test mode flip-flop IC6-6 to the test mode state, generating TM and $\overline{TM}$ true. The test mode flip-flop is direct-cleared when the transport is placed on line, or when the TEST MODE pushbutton is activated a second time. After the test mode flip-flop has been set the other test panel pushbuttons are enabled. The WRITE TEST pushbutton may then be activated, setting the protective flip-flop consisting of inverters IC11-4 and IC11-6. This toggles the write test flip-flop IC6-1 to the write test mode, provided that forward motion is selected. The $\overline{Q}$ output of the write test flip-flop then activates NOR gate IC1-8, which in turn activates write ready gate IC4-5, provided that FILE PROTECT (FPT), REVERSE (RVS1), and BUSY ($\overline{BSY}$) are all false. WRITE READY (WRDY) true is then generated at output pin J to the Write Amplifier module, where it enables the write data strobe circuitry. During the write test the write amplifiers generate consecutive all-1 characters which may be used to adjust the skew.

Additional test panel pushbuttons are FWD RUN (a forward run normal button), FAST FWD (a high speed forward button), REV RUN, and CYCLE. The reverse run button can be activated only if ON TAPE flip-flop IC10 is set and the tape is not at load point. NAND gate IC3-3 is activated, which in turn activates NAND gate IC7-6 (when the TEST MODE flip-flop is set) and sets the common of the reverse buttons low. The forward motion commands are terminated when either the STOP pushbutton is activated, clearing the TEST MODE flip-flop, or end of tape is detected, in which case EOT1 true is inverted by IC17-4, disabling NAND gate IC7-3 and setting the common of both forward motion buttons high. Similarly reverse motion can be terminated by activating the STOP pushbutton, which terminates all test mode operations, or when load point is detected, in which case LP true is inverted by IC17-3 and disables NAND gates IC3-3 and IC7-6. This sets the common of the reverse buttons high. The Pushbutton Control module also drives the test panel indicators, lighting the data lamp when any data is being processed by the write/read electronics, illuminating the skew indicator when the skew is out of adjustment, illuminating the EOT indicator when the transport is at end of tape, and illuminating the LOAD POINT indicator when the transport is at the beginning of tape.

The CYCLE function is fully discussed in the Type 5655 Test Panel Switch circuit description.

TYPE 4843 AUTO POWER RESTART PC BOARD
CIRCUIT DESCRIPTION
(OPTIONAL PC BOARD)

Introduction

When incorporated in any of the Kennedy Model 9000, 9100, 9300, 9700, 9800, or 9832 recorders, the type 4843 Pushbutton Control module allows use of several factory optional features. These functions are determined by optional straps and the use of components in the APR field. Not all functions and/or combinations of such are available with every 9000 series recorder. Refer to schematic 401-4843-001 and the dash number of your particular 4843 module for features that have been incorporated and tested at the time your unit was built. Due to the interaction of several of these options the user is advised to consult the factory in writing if he desires to incorporate any additional optional features through field modification. Failure to do so invites the possibility of voiding the warranty of the particular recorder involved.

The major optional features along with suggested usage are outlined below. (Reference is made to schematic 401-4843-001.)

ON TAPE (OT)

Determined by the placement of option strap 1. If this option is specified at the time of factory order, the operator cannot place the tape unit on line until a reel of tape is loaded and positioned at or past the BOT tab.

ONLINE LOCK (ONLL)

Determined by the placement of option strap 2. When specified at the time of factory order, this feature prevents the operator from manually taking the tape unit off line via the front panel switch, unless the tape controller has allowed him to do so. This signal is not normally gated with select and is an input signal line on interface connector J1-A.

FAST (FST)

Determined by diode CR2 and a special control interface module. When specified at the time of factory order, this feature allows interface control of high speed forward and high speed reverse motion of tape. It is used in conjunction with the Synchronous Forward, Synchronous Reverse, and the optional Fast line at the control interface connector of the deck. High speed forward and reverse commands will be accepted when the tape is on line and selected. The high speed reverse command will be implemented at any time when tape is positioned past the BOT tab and the high speed forward command will be carried out only when tape is positioned at or between the BOT and EOT tabs (past EOT, a fast forward command will cause tape to advance at the normal synchronous forward speed). Note: This feature should be used only for purposes of high speed search, as writing cannot be done at high speeds.

AUTO POWER RESTART (APR)

Determined by the configuration of components in the APR field and external assemblies (in some models) driven by this module. When specified at the time of factory order, this option will protect the tape unit against "brownout" and will automatically power up, load, and set the deck on line under certain conditions. With the standard APR option this circuitry continually monitors the line voltage and whether the tape unit is on line or off line. If the external line voltage falls below a minimum value required by the tape deck, this option will force the deck into an off-line state along with issuing a BROKEN TAPE command (i.e., the reel and capstan servos will be disabled and any write current is inhibited). When the input power level returns to an acceptable value, the APR circuitry will do one of two things, depending on whether the deck was on line before the power fell: (1) nothing, if the deck was in an off-line state, or (2) load, advance tape several inches and place the deck on line if it was previously in an on-line state. Additionally, if APR circuitry is used in the Model 9832 buffer, it will issue an INITIALIZE signal (i.e., clear the buffer memory) when power is returned.

OPTIONAL LOAD ON LINE FEATURE

A factory variation (to be specified at time of order) of the standard APR option is the LOAD ON LINE (LOL) feature. If specified, this allows the user, through a control interface signal, to load and place the tape deck on line. The LOL signal is acknowledged only after external power has dropped and returned to an acceptable level and the deck is in an unloaded state. If the LOL feature is used, it is the user's responsibility to provide a TTL logic low-going pulse (minimal pulse duration 500 milliseconds) after power is returned to an acceptable level. The LOL signal is not gated with SELECT and appears as an input signal on interface connector J1A.

SUGGESTED USAGE OF APR FEATURE

The standard APR circuitry is activated only when the deck is placed on line and is deactivated when the deck is placed off line. (In the case of the LOL variation, circuitry is activated only when power has failed and then returned when the deck is in an unloaded state.) Thus, when manually loading a reel of tape on the deck, the APR feature is transparent to the operator and only comes into play when

external power has failed with the tape deck in an on-line state. The tape deck must be mounted in a vertical positon to avoid spilling of tape in the case of power failure. Proper positioning of commands after the APR circuitry has repowered the deck depends on the particular mode of operation and should be determined by the application. If a rewind was in process at the time of power failure, the tape may stop and become repositioned up to 5 feet before load point. For proper operation in this case, tape should be spaced forward 6 feet and then rewound. For any other mode of operation, it is suggested that a REWIND command be issued immediately after an APR power-up. The LOL signal is not gated with SELECT and appears as an input signal on interface connector J1A.

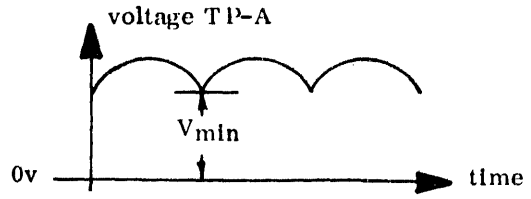
The APR circuitry is designed to operate under conditions of power failure external to the tape deck. Power failure simulations made via the front panel power switch do not come under the above category since this power switch is located between an input power RFI filter and the power transformer.

AUTO POWER RESTART ADJUSTMENT

Normal field adjustment of the Auto Power Restart board is not required unless a new APR board is placed in a machine or an existing board has been refurbished. If this is the case, the following field procedure is recommended:

1. Power up machine and adjust R18 fully CW.

2. Monitor TP-A and TP-B with a scope. TP-B is a logic level and will be high. TP-A is the preregulated +5 vdc and will appear on the scope as illustrated below:



3. Adjust the input power voltage to the machine so that the value of V_{min} (as shown above) equals the value stated on schematic 401-4843-001 of the APR PC board.

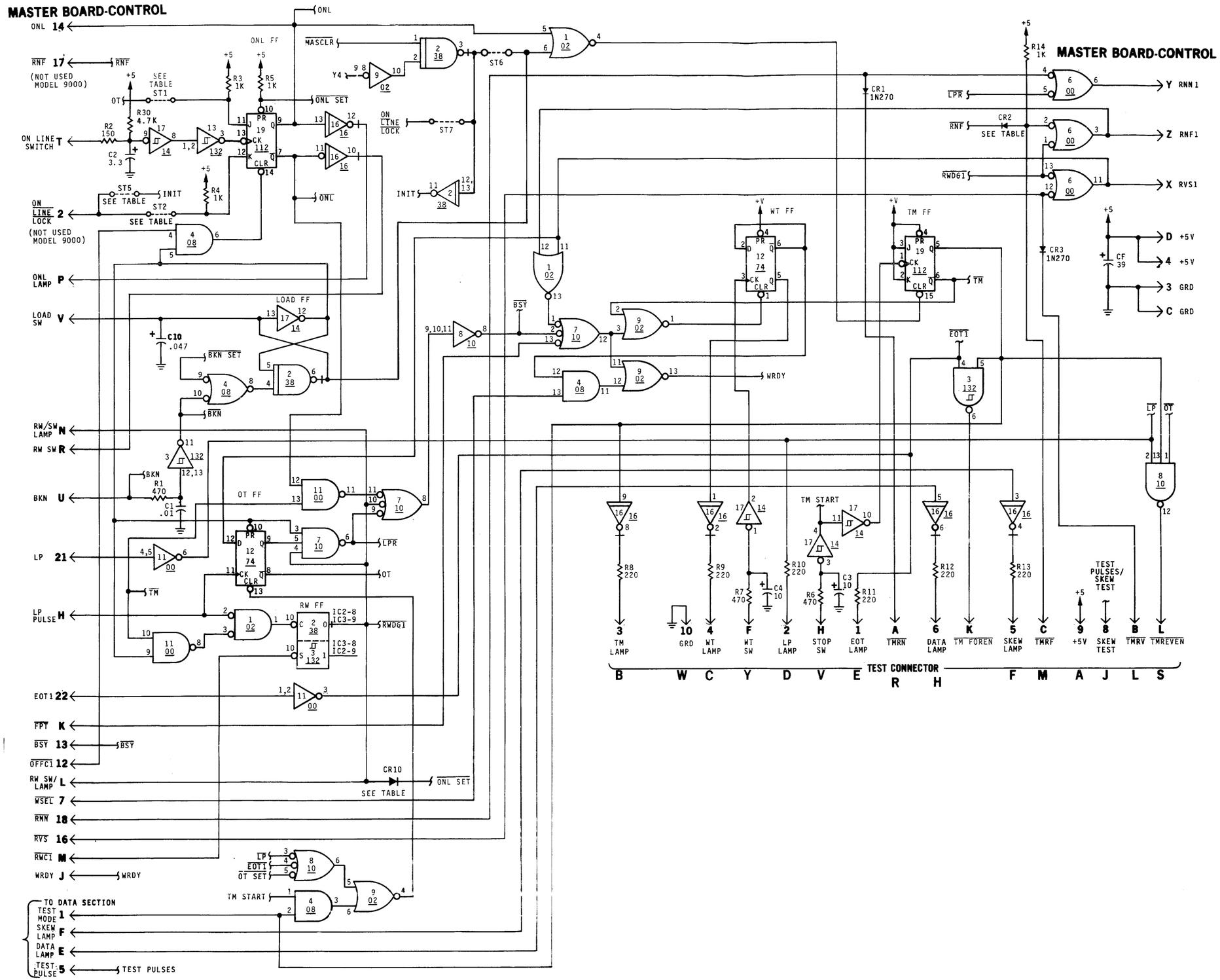
4. Turn R18 CCW until the voltage appearing at TP-B goes low.

APR OPERATION IN MODELS 9100/9300

APR operation in these vacuum column tape transports is identical to the above description with the following exceptions:

a) Manual and power failure initiated load sequences take approximately twice as long due to the increased tape tensioning time required to prevent oversized tape loops from forming in the vacuum columns during a power failure.

b) The manual and APR load sequences are now as follows: Tension Tape; Load Columns, Search forward to load point; if load point is not found after a given time out period, rewind to load point; then place unit online.



APR Pushbutton Control, Type 4843, Schematic Diagram Sheet 1 of 2

401-4843-001 V/

STATE	FUNCTION	NEXT (JUMP)	JUMP CONDITION
0	$\overline{\text{BKN SET}}$	1 (0)	$\overline{\text{MAS CLR}}$
1	$\overline{\text{BKN SET}}$	2 (0)	$\overline{\text{MAS CLR}}$
2		3	
3		4	
4		F (7)	$\overline{\text{LOL}}$
5		6	
6		7	
7		8	
8	$\overline{\text{LDSET}}$	9	
9	$\overline{\text{LDSET}}$	A	
A	$\overline{\text{OTSET}}$	B	
B	$\overline{\text{OTSET}}$	C	
C	$\overline{\text{ONLSET}}$	D	
D	$\overline{\text{ONLSET}}$	E	
E	ENABLE	E (0)	$\overline{\text{MAS CLR}}$
F	ENABLE	F (0)	BKN

X TABLE

DASH NO.	-0YZ	-1YZ	-2YZ	-3YZ	-4YZ	-5YZ	-6YZ	-7YZ	-8YZ	-9YZ
SPEED(IPS)	-	10	12.5	15	18.75	25	37.5	45	75+	—
R25	OMIT	180K	150K	100K	82K	68K	47K	39K	2.2M	3.3M

Y TABLE

DASH NO.	-X0Z	-X1Z	-X2Z	-X3Z	-X4Z	-X5Z	-X6Z	-X7Z	-X8Z
FIRST USED ON	9000	9100/9300	9000/9700/9800		9832		9700/9800	9100/9300	9100/9300
FUNCTION	STD	LOL	LOL	AUTO	LOL	AUTO	AUTO RW	AUTO	AUTO/OT
APR CIRCUIT		●	●	●	●	●	●	●	●
ST3, RELAY K1				●		●	●	●	●
ST4			●	●	●	●	●		●
ST5					●	●			
ST6	●		●	●	●	●	●		
ST7		●						●	●
ST8	●		●	●	●	●	●		
ST9		●						●	●
DIODE CR10							1N270		

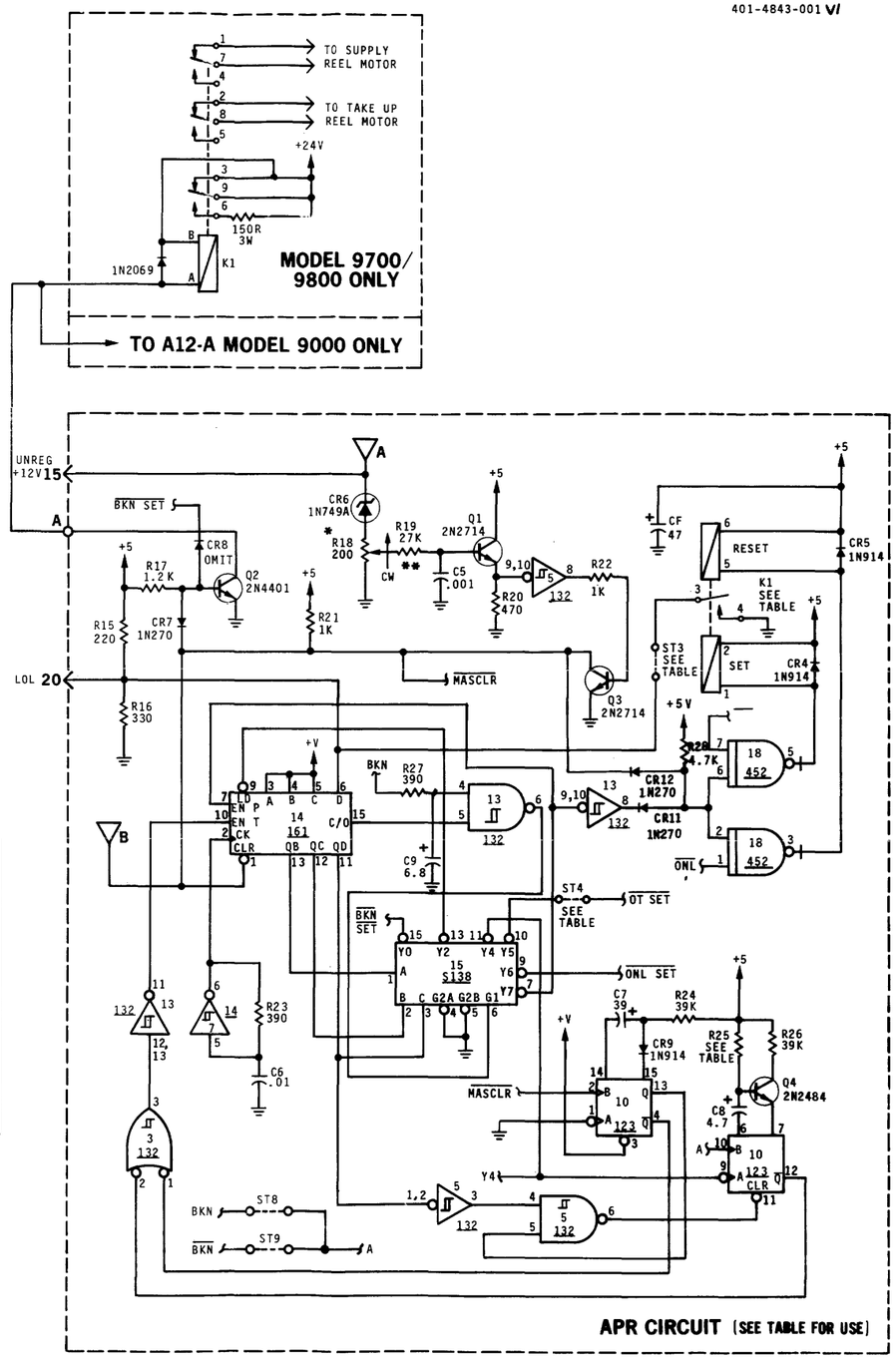
Z TABLE

DASH NO.	-XY1	-XY2	-XY3	-XY4	-XY5	-XY6	-XY7	-XY8
FUNCTION	STD	OT	ONLL	OT/ONLL	FAST	OT/FAST	ONLL/FAST	OT/ONLL/FAST
ST1 (OT)		●		●		●		●
ST2 (ONLL)			●	●			●	●
CR2 (FAST)					1N270	1N270	1N270	1N270

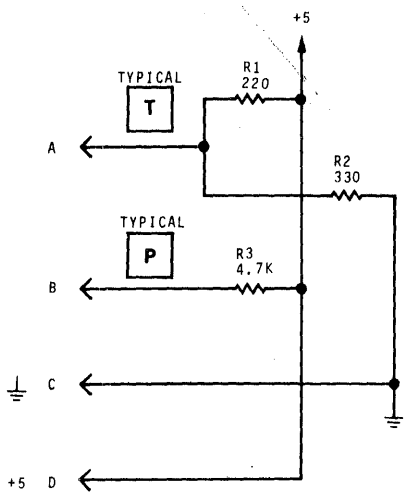
●=USED

*ADJUST R18 SUCH THAT SIGNAL AT TEST POINT B GOES LOW WHEN VOLTAGE FALLS BELOW 6.25 ±.15V MIN AT TEST POINT A (NOTE SCHMITT ACTION OF IC5-3)
**FACTORY SELECT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.



APR Pushbutton Control, Type 4843, Schematic Diagram Sheet 2 of 2



E ← T

F ← T

J ← T

L ← T

M ← OMIT

N ← T

P ← T

R ← P

S ← P

T ← P

U ← P

V ← P

W ← P

X ← P

Y ← P

Z ← P

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Control Terminator, Type 3841-001C, Schematic Diagram

TYPE 6667 SEQUENCE CONTROL

CIRCUIT DESCRIPTION

This module contains circuitry for implementing the following sequences: LOAD, when tape is loaded into the column after the LOAD pushbutton is pressed; UNLOAD, when tape is rewound onto the supply reel after the REWIND pushbutton is pressed at load point, and POWER OFF, when tape is removed from the column and tensioned after power is turned off from the front panel POWER pushbutton. In addition, the broken tape sensor detector circuitry (Q2 and related components), the rewind pushbutton control circuitry (IC13, IC7 and related components), the automatic load point search circuitry (IC3 pin 12, C6, R24) are all located on this board.

Sequences are controlled through the use of a low frequency clock (IC15) with a period of approximately 0.5 second, and an eight-stage shift register (IC16, IC17). When power is first turned on, a power preset pulse (IC6 pin 4, Q1 and related components) presets the shift register to all zeros, resets the load flip-flop (IC9 pin 6), and the unload flip-flop (IC9 pin 8). By the same token the load point search flip-flop (IC1 pin 6) is being set.

Note that a broken tape sensor output or a loss of vacuum detected after loading will generate the same preset status mentioned above. Under these conditions no power is applied to the vacuum blower motor and the high power transformer (for the servos). In addition, a broken tape signal and an unload command are sent to the control logic, and a sensor dsable and servo disable true signal are sent to the servo preamplifier.

LOAD SEQUENCE

When the LOAD pushbutton is pressed after a low frequency clock time, the load flip-flop is set, enabling the shift register to shift 1 to the right. (The low frequency clock is also the clock to the shift register.) The load flip-flop also starts the vacuum motor through a command from SS1 (capacitive start). At stage 1 the LOAD light on the front panel is turned on and so is the high power transformer, generating +24v rectified (SS2). This delay avoids a high surge of ac input current which could overload the line.

At stage 2, the servo disable to the servo preamplifier is set false, allowing the power amplifiers of the reel and capstan servo to operate. At the same time, the load relay is energized, connecting the reel motors to their respective amplifier and latching the ac power pushbutton. (Prior to this, the motors were being braked.)

At stage 7, sensor disable goes false. During the time from stage 2 through stage 6, the reels motors were operating on an open loop mode, tensioning the tape on its threading path and allowing the vacuum to reach its nominal level. When the servo disable goes false, the tape is fed into each column through a measured "kick" (this circuit is implemented in the Type 6666 Servo Preamplifier) and the position servo mechanism of each column is closed through its respective sensor. The tape is now loaded.

At stage 8, a load signal (with a false broken sensor signal) is fed to the control electronics, which in turn enables the capstan to run forward. If load point is not found within 6 seconds (60 feet), the load point search flip-flop is still set and IC16 will force a rewind to load point. At the same time, the vacuum switch is enabled.

POWER OFF SEQUENCE

When power is turned off from the front panel, switch S1 will close and reset the load flip-flop, enabling the shift register to shift 0 to the left, turning off the vacuum blower and immediately setting SENSOR DISABLE true. The sequence is now opposite to the load sequence. Up to stage 2 the tape is being pulled out of the column and tensioned properly. At the end of the sequence all power is turned off (load relay false).

UNLOAD SEQUENCE

When the REWIND pushbutton is pressed at load point and the tape is standing still as detected by IC13, CR5, CR6, R20, R22 and R21, the unload flip-flop is set and the power off sequence is initiated (IC5, pin 12). However, the power remains on at the end of the power off sequence and after tape has been pulled out of the column, an UNLOAD/ true signal is sent to the 6666 Servo Preamplifier, disabling the takeup servo and applying voltage to the supply reel to unload the tape. The unload sequence is terminated when end of tape is detected by the broken tape sensor, which results in BKN true at the sequence control.

REMOTE UNLOAD

Certain APR modified units permit remote unloading from the interface. UNLOAD/ true at pin 18 sets the UNLOAD flip-flop (IC9-8,12) resulting in UNLOAD/ true at output pin 11.

401-6667-001 K

DASH NO.	USED ON	R1	R9	1C12
001K	9300STD	1M	150,3W	INSTALL
002H	9100STD	680K	56,3W	
003C	9300APR	3M	150,3W	OMIT
004C	9100APR	2.2M	56,3W	

GRD 1
-10 2 → -10
+10 3 → +10
+5 4 → +5
+5 16 TO SS
CF 10
LOAD 9
LOAD 5
S1-B 6
POWER OFF
STANDARD TACH 20 (FROM SERVO PREAMP)
UNLOAD 18
LOAD POINT 23 (FROM CARD CAGE)
7 BKN FROM CONNECTOR BD.
10 VACUUM SWITCH
22 REWIND
ON LINE 21
STRAP ST1
PRESET
R1 SEE TABLE
R2 470
C1 .68
C2 0.01
CR12
R3 6.2K
R4 3.3K
R5 2.2K
R6 1K
R7 2K
R8 2K
R9 SEE TABLE 3W
R10 4.7K
R11 10K
R12 2.2K
R13 4.7K
R14 330
R15 4.7K
R16 4.7K
R17 22
R18 220
R19 2K
R20 470K
R21 10K
R22 10K
R23 1K
R24 470K
R25 100
R26 220
R27 4.7K
R28 4.7K
R29 22
R30 1000
R31 4.7K
R32 100
C3 39
C4 0.47
C5 0.39
C6 10
C7 0.01
C8 .01
CR1
CR2 1N753A
CR3 1N753A
CR4
CR5
CR6
CR7
CR8
CR9 1N270
CR10
CR11 1N270
Q1 2N4990
Q2 2N4401
L1 4.7 MH
L2 4.7 MH
K1 +24
1N2069
SERVO ENABLE
14 SS2 HI POWER (TB2-3, POWER SUPPLY)
12 SERVO DISABLE (TO SERVO PREAMP)
19
13 SENSOR DISABLE (TO SERVO PREAMP)
8 SSI VACUUM MOTOR (TB2-4, POWER SUPPLY)
15 LOAD (TO CARD CAGE)
17 BROKEN TAPE (TO CARD CAGE)
11 UNLOAD (TO SERVO PREAMP)
24 REWIND (TO CARD CAGE)
PRESET

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Sequence Control, Type 6667, Schematic Diagram

TYPE 5733 RAMP GENERATOR

CIRCUIT DESCRIPTION

The ramp generator produces the proper analog signal inputs to the capstan servo system to control the direction and velocity of tape motion. The outputs are voltages that rise and fall linearly at controlled rates to highly stable levels. These analog signals are controlled by digital logic outputs from the control section.

Two similar ramp generator circuits are provided: one for normal speed operation and one for high speed operation. IC4 is an operational amplifier in the RUN NORMAL SPEED circuit. The amplifier output is normally saturated in the negative direction. When its positive input at pin 3 is high, the output saturates at +10 volts. This occurs when the RUN NORMAL input sets flip-flop IC7. IC4 feeds FETs Q1, Q2 which are connected in a constant-current circuit. The magnitude of current flow in the circuit is controlled by R3 and R4. R3 controls current in the positive-going direction, or start ramp, while R4 controls the negative-going stop ramp.

Since C1 is charged by a constant current, its voltage rises linearly until clamped by CR1 to a value one diode drop below +5 volts. The emitter of Q11 is connected to RUN FAST voltage through diode CR9. Since Q11 is controlled by unregulated power supply voltage at pin W, it pulls down the +5 volt RUN FAST signal whenever the line voltage drops below its rated level. Q3 is an emitter follower whose output rises to a value of +5 volts, since the emitter can rise one diode drop higher than the base. When the input from IC7 to IC4 drops, the voltage fed to Q1, Q2 goes to -10 volts and C1 is discharged linearly until clamped by the base-collector diode of Q3. Since Q3 base goes one diode drop negative, and the emitter is at zero, a positive-going ramp has been generated.

The ramp voltage output from Q3 is fed to the FET switches Q4 and Q5. If forward direction has been selected, Q4 is on and Q5 is off. The ramp is then amplified by unity gain operational amplifier IC3, without inversion, and appears as a positive-going ramp at test point A. If reverse is selected, Q5 is on and Q4 is off. The ramp is then fed to the inverting input of IC3 and appears as a negative-going ramp at test point A. Forward/reverse selection is controlled by flip-flop IC6 and Q9, Q10.

Ramp amplitude and, therefore, tape speed are controlled by normal speed control R14 and output summing resistor R15. The fast forward and reverse ramps are produced by a similar circuit involving amplifiers IC1 and IC2. However, since rewind speed and ramp time need not be precisely controlled, resistors are used instead of FETs to charge and discharge C4 and produce an approximate 0.5 sec rise/fall time. CR9 and CR10 isolate the ramp output from any small offsets that may be present in IC2. Rewind speed is controlled by summing resistor R16. Operational amplifier IC5 at zero ramp output has a slight bias produced by R37 and R38, keeping its output negative. When the ramp rises above the bias, IC5 switches to positive output, indicating that the tape is running. This output is used to gate off the input circuits through IC10 and IC9. Flip-flops IC7 and IC8 may be reset by run normal or run fast inputs going false, but cannot be set again until the tape comes to a stop. This prevents damage from illegal commands and reduces timing requirements.

Resistor R44, capacitor C10, emitter follower Q11, and diode CR8 comprise a voltage tracking circuit for RUN FAST signal. The +18 vdc unregulated reference voltage is derived from power supply transformer T1.

Type 5733 Ramp Generator includes an additional flip-flop, IC11-8, whose function is to enable consecutive RUN NORMAL commands to be received without requiring the tape to ramp down to a stop following each normal speed operation. Following a RUN FAST command, however, flip-flop IC11 is set by IC8, inhibiting any RUN NORMAL commands until the tape comes to a stop, at which point IC9-6 clears IC11-9, and the 0 output at IC11-8 enables IC7-2.

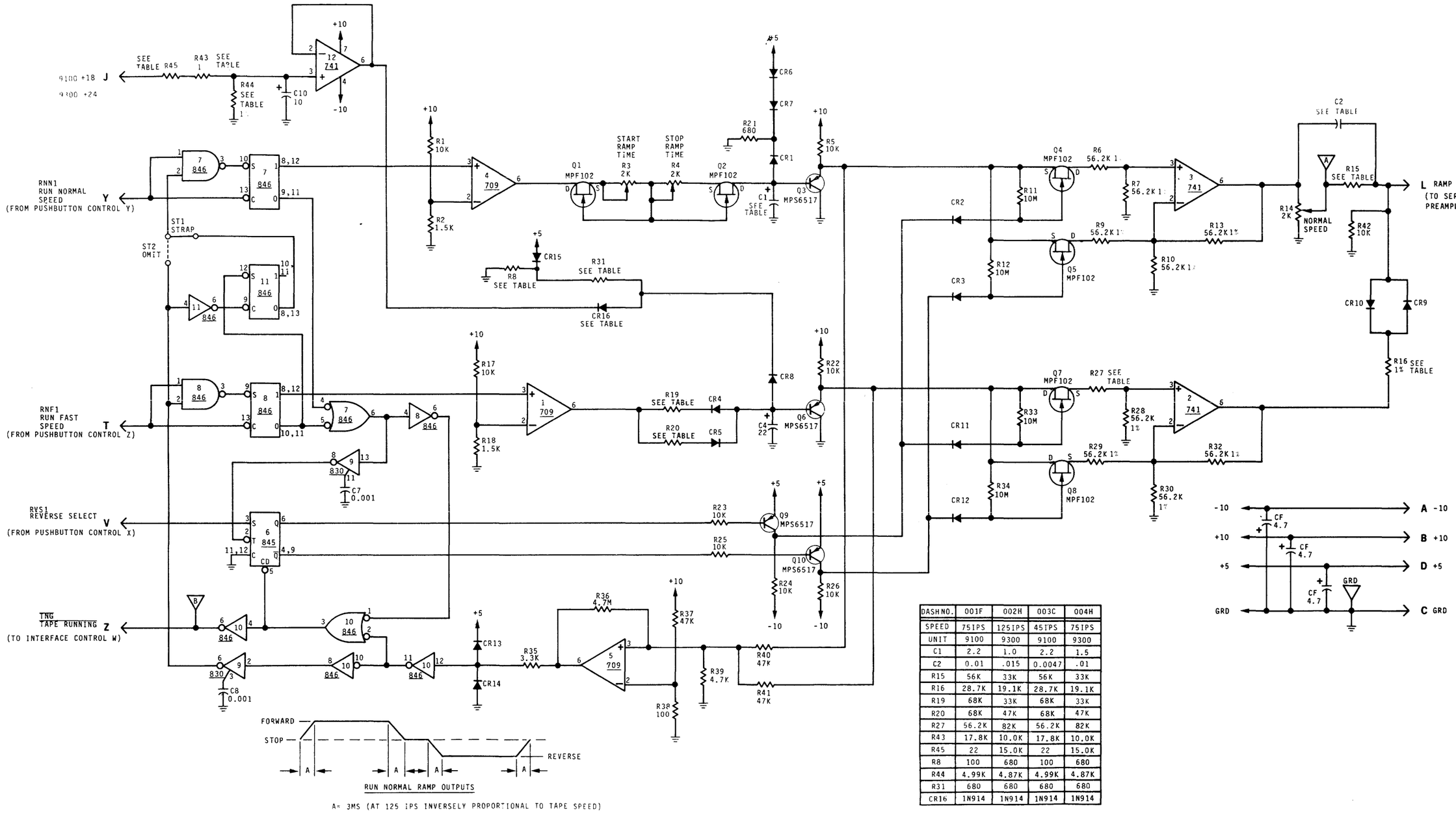
ADJUSTMENT PROCEDURE

Start/stop time adjustment:

a. Arrange input signals to the tape transport to start and stop machine. Rate must be such as to allow full ramp time.
b. Adjust start ramp (R3) for required time, observing with oscilloscope at test point A.
c. Adjust stop ramp (R4) for required time. Time is measured from maximum volts to zero volt.

Speed adjustment:

a. Using a masterskew tape, drive the transport in a forward direction at normal speed.
b. Observe data rate at read amplifiers and adjust R14 for correct timing.



DASH NO.	001F	002H	003C	004H
SPEED	75IPS	125IPS	45IPS	75IPS
UNIT	9100	9300	9100	9300
C1	2.2	1.0	2.2	1.5
C2	0.01	.015	0.0047	.01
R15	56K	33K	56K	33K
R16	28.7K	19.1K	28.7K	19.1K
R19	68K	33K	68K	33K
R20	68K	47K	68K	47K
R27	56.2K	82K	56.2K	82K
R43	17.8K	10.0K	17.8K	10.0K
R45	22	15.0K	22	15.0K
R8	100	680	100	680
R44	4.99K	4.87K	4.99K	4.87K
R31	680	680	680	680
CR16	1N914	1N914	1N914	1N914

NOTE. FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Ramp Generator-Model 9100/9300, Type 5733, Schematic Diagram

TYPE 5719 SENSOR AMPLIFIER DRIVER CIRCUIT DESCRIPTION

This module responds to signals from infrared detecting transistors which sense load point and end of tape reflective strips, and broken tape. In addition, this module contains the file protect circuitry, the write drives, and the erase head drives.

EOT, BOT, AND BKN SENSOR AMPLIFIERS

The load point sensor amplifier and the end of tape sensor amplifier operate interdependently to detect the load point and the end of tape markers. The active components in detecting EOT and load point are two operational amplifiers, IC6 and IC8, and two transistors, Q1 and Q2, in conjunction with associated components. Transistors Q1 and Q2 act as current sources; potentiometer R16 is used to adjust the transistor base currents to equalize the voltage at the inputs of IC8, the load point sensor amplifier, and IC6, the end of tape sensor amplifier. Resistors R18, R19, R20, and R21 are used to bias the amplifiers' inputs when plain tape is in front of the sensors. When either load point marker or the end of tape marker is detected, the infrared detecting transistor of the particular sensor is turned off, and a high level is supplied from Connector Board Type 5303 at either pin Y or Z, switching the output of the respective operational amplifier. Resistors R17 and R22 serve as feedback loops for noise protection. Thus when load point is detected, the load point sensor supplied at input pin Y of this module saturates IC8, causing its output to go high, and is inverted twice by IC7 to generate LOAD POINT (LP) true at output pin 19 to the Pushbutton Control module. The output of inverter IC7-8 is also supplied to an edge circuit which produces a 1 microsecond pulse on the trailing edge of LP. This pulse is output at pin 8 to the Pushbutton Control module. The EOT sensor amplifier operates in the same manner, generating a high output when the EOT marker is detected, and supplying EOT true at output pin X to the Pushbutton Control and Control Interface modules.

BROKEN TAPE signal from the Sequence Control enters the board at pin W. When BROKEN TAPE goes true, positive voltage turns on transistor Q3. The collector of the transistor goes to ground, generating BKN true at output pin 18. When power is initially turned on capacitor C9 will cause the BKN output to be high which presets the LOAD flip-flop on the Interface Control module.

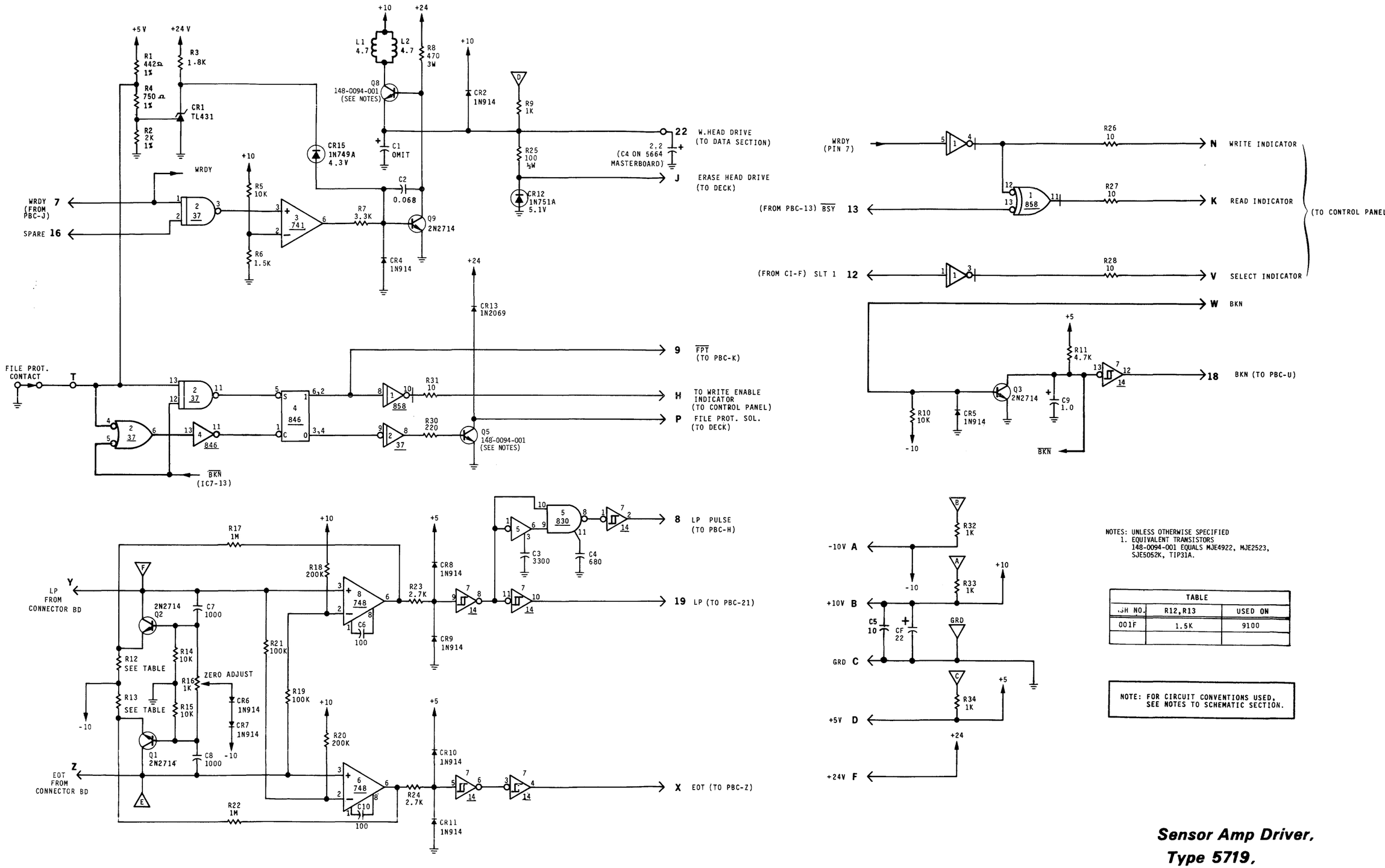
FILE PROTECT CIRCUITS

The file protect switch output is supplied to this module at pin T from Connector Board Type 5303. When a reel is loaded without a write enable ring, the switch contact remains grounded. During the load sequence, BKN is held true by the sequence control to facilitate certain operations and the tape must be reloaded to change the state of the file protect flip-flop (IC4-5). When BKN is made false, the circuit looks at the state of the file protect contacts. FPT true at pin K of the pushbutton control makes WRITE READY (WRDY) false.

WRITE, ERASE DRIVES

When the file protect switch is grounded, it also turns off transistor Q7, in turn shutting off the current at the base of Q8. This cuts off the write head and erase head drive currents supplied by transistor Q8. In order for the write and erase drives to be turned on, the file protect switch must be opened and WRITE READY must be true at input pin 2. This will activate NAND gate IC2-3, causing op amp IC3 to turn off transistor Q9, in turn enabling transistor Q8 to turn on and supply the write and erase head drives at pins 22 and J.

The zener diode into the base of Q7 detects when power is being dropped. This turns off Q7 early enough in the power down sequence to turn on Q9 and remove the head voltage supplied by Q8. This avoids putting unwanted flux changes on tape during a power failure.



NOTES: UNLESS OTHERWISE SPECIFIED
1. EQUIVALENT TRANSISTORS
148-0094-001 EQUALS MJE4922, MJE2523, SJE5052K, TIP31A.

TABLE		
ISH NO.	R12,R13	USED ON
001F	1.5K	9100

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Sensor Amp Driver, Type 5719, Schematic Diagram

TYPE 5655 TEST PANEL SWITCH

CIRCUIT DESCRIPTION

Located on the front of the tape transport, this module contains the Type 4865 Test Panel, Type 4568 Cycler, and the Type 3864 LED Display Panel. The test panel switch is connected to the Pushbutton Control card, which contains most of the logic circuitry required to deliver appropriate commands to the ramp generator when the machine is off line and one of the test modes has been selected. (Refer to Model 9100 Tape Motion Control circuit description for a detailed explanation of this process.) Continuous forward and reverse tape motion circuitry for adjusting skew and aligning the tape path is contained in the Type 4568 Cycler circuit board.

CYCLER OPERATION

When the CYCLE pushbutton is pressed with the machine in test mode and at load point, the cycler generates alternating negative true $\overline{\text{TRVS}}$ and $\overline{\text{TRNN}}$ commands to the Pushbutton Control module. The tape will move forward and reverse continuously until the STOP pushbutton is pressed or END OF TAPE is reached (Note: Tape will not move in reverse when positioned at LOAD POINT.)

The basic operation of the cycler is as follows: If the cycle switch is not activated, the low true $\overline{\text{RVS}}$ and $\overline{\text{RNN}}$ signals from IC3 are "gated out" of the Pushbutton Control board via the S1 cycle switch. When the cycle switch is activated, the low frequency oscillator IC2-5 is enabled and $\overline{\text{RVS}}$ and $\overline{\text{RNN}}$ are switched into the Pushbutton Control board. Forward tape motion is produced by the application of a $\overline{\text{RNN}}$ and $\overline{\text{RVS}}$ command, whereas reverse tape motion takes place when $\overline{\text{RNN}}$ and $\overline{\text{RVS}}$ commands are applied. The duty cycle of IC2-5 is approximately 60% and is gated at IC3 so that 40% of the time $\overline{\text{RVS}}$ is enabled, contributing to a net forward motion of tape in the cycle mode. IC1, R4 and C3 act as a bidirectional edge detection circuit. IC1-8 triggers monostable IC2-9, which disables any $\overline{\text{RNN}}$ command during the ramp as required for proper operation.

401-9100-003BI

PUSHBUTTON CONTROL CARD TYPE 3843

MAIN CONTROL PANEL 5665

SEQUENCE CONTROL 5667

CONTROL INTERFACE 3842

PHOTO-SENSOR AMP/DRIVER

DUAL DENSITY CONTROL 4365

LED PANEL 3864

TEST PANEL 4865

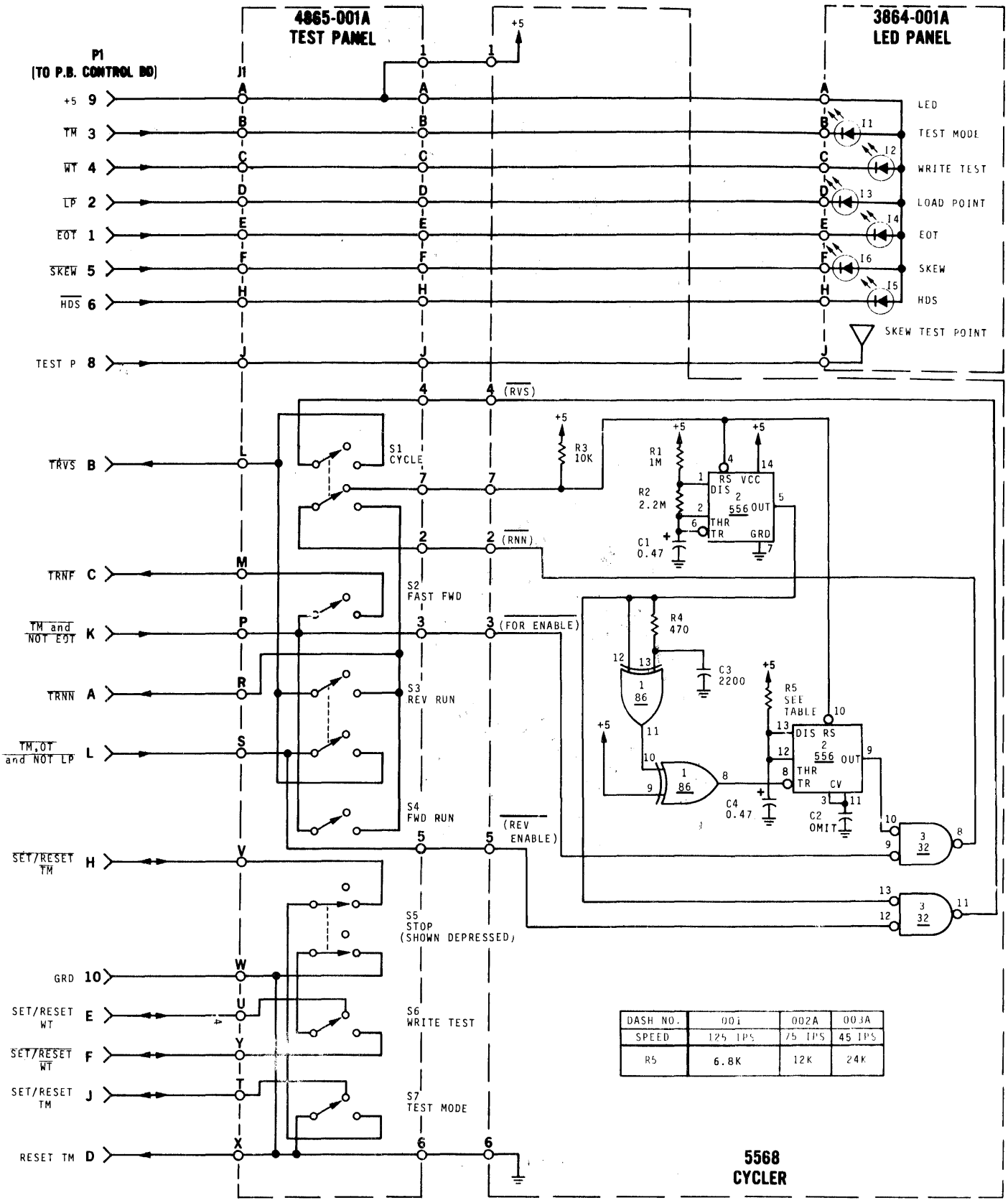
CYCLER 5568

TEST PANEL SWITCH 5655

	STD	TMZ
3843	001F	002C
ST1	STRAP	OMIT
ST2	OMIT	STRAP
C6	OMIT	220
ST3	OMIT	OMIT
ST4	OMIT	OMIT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

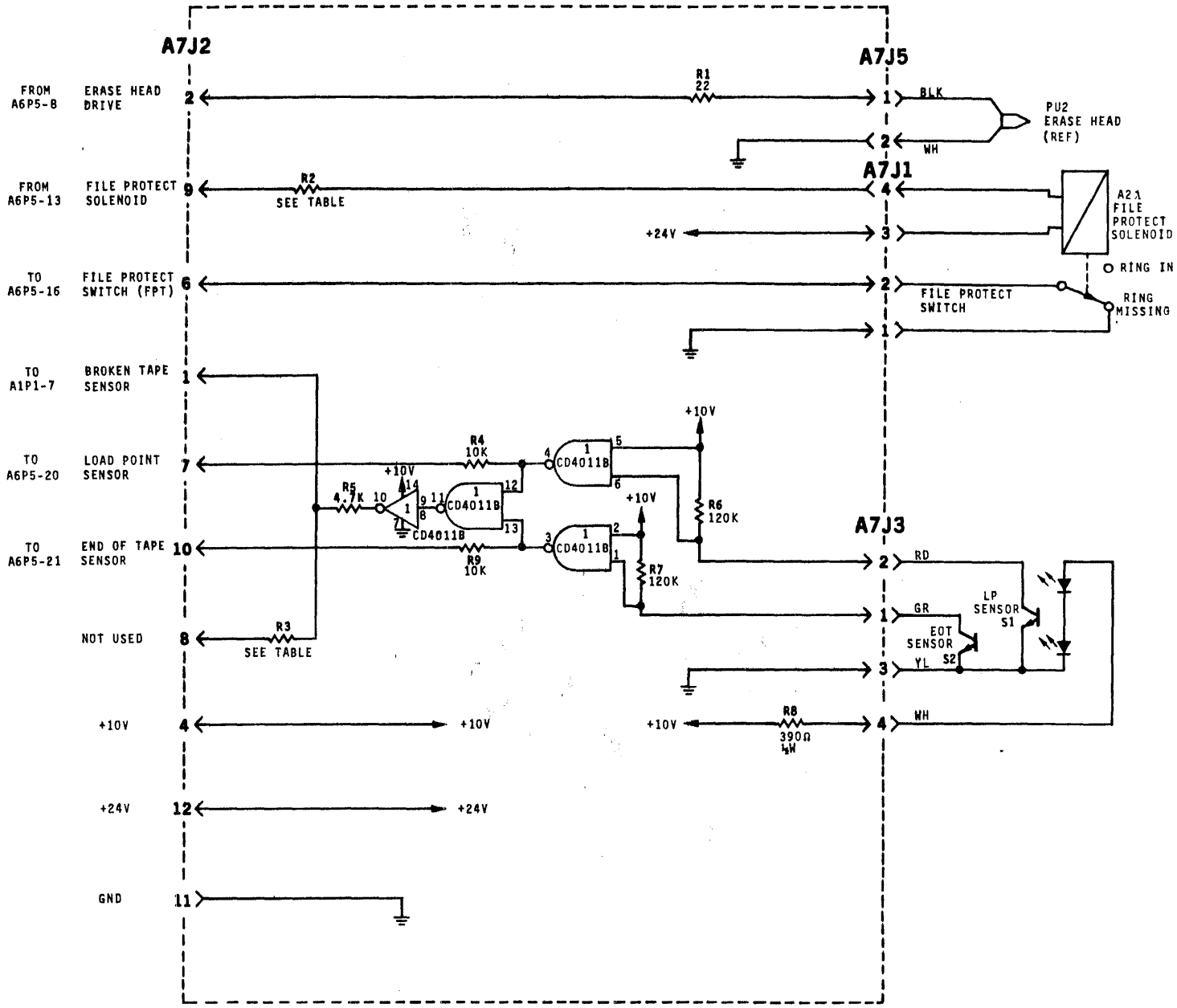
Tape Motion Control-Model 9100, Type 3843, 5665, 5655, Schematic Diagram



DASH NO.	001	002A	003A
SPEED	125 IPS	75 IPS	45 IPS
R5	6.8K	12K	24K

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Test Panel Switch-Model 9100, Type 3864, 4568, 4865, Schematic Diagram



DASH NO.	R2	R3
001	STRAP	2.2K
002	15, 3W	2.2K
003	STRAP	OMIT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Connector Board Type 5303
Schematic Diagram

MODEL 9100/9300 SERVO SYSTEM

CIRCUIT DESCRIPTION

The Servo System consists of the servo preamplifier circuits, the servo amplifier circuits and the braking circuits. There are separate servo preamp circuits for the reels and the capstan. Each reel servo preamplifier circuit is connected to its own servo amplifier circuit. The composite schematic of the servo system should be used along with the circuit description.

TAKEUP AND SUPPLY REEL SERVOS

Both circuits are identical; therefore we will concentrate on the supply reel servo, discussing control signals common to both reel servos as applicable. Each reel servo contains a sensor detector circuit, which converts the position of the tape loop into dc voltage, an operational amplifier for position servo control (IC18, Q6, Q7, Q8, Q9), and the amplifier stages (four transistors each).

Resistor R10 and the supply vacuum column sensor control the nominal output frequency of the sensor detector, IC21. (Refer to paragraph 4.11 of the maintenance section if adjustment of resistor R10 is required.)

After the servo signal oscillation is rectified and integrated, it is fed to operational amplifier IC19. Gain adjustment pot R24 is set to adjust proper position of the tape loop in the column when speed is 125 ips forward and reverse. (Refer to paragraph 4.11 of the maintenance section.) N type FET Q2 is the sensor disable control. SENSOR DISABLE true (high) signal from the Sequence Control will turn off the FET, preventing the sensor signal from actuating the motors. Thus, when tape is not in the column or vacuum is lost, SENSOR DISABLE goes true to turn off the signal from the column sensor. During the POWER ON sequence, the Sequence Control generates SENSOR DISABLE true, opening the position servo loop and positioning the reels until the tape is properly tensioned in the vacuum columns.

SERVO DISABLE true from the sequencer will disable motor current by reverse biasing reel servo control FET Q5. FET Q15 and Q32 are also reverse biased, opening the takeup reel and capstan servo loops.

Capacitors C2 and C15 on the reel servos perform a special function. During discharging, the capacitors will produce a forced sensor output equivalent to the tape sitting at the open end of the column.

A signal from the capstan tachometer is fed into the reel servo system to bias the null position of the tape loop as conditioned by the speed and direction of tape movement. This has the effect of optimizing the position of the tape in the column. The signal is amplified and conditioned by IC4, 3, and 2 so that (a) there is no output when tape is standing still (b) there is an output proportional to speed and direction during ramp-up and ramp-down, and (c) there is a fixed voltage while running (IC4 saturated).

BRAKING CIRCUIT BOARD

For safety reasons (broken tape) it is desirable to place braking tension on the tape after it has been threaded and secured to both reels. To accomplish this, two thyristors on the Braking Circuit board are connected to the motor windings when SERVO DISABLE is true. When the reels turn rapidly enough for the motor windings to generate more than 3 vac, the voltage at the gates of both thyristors will exceed 0.5 vac. The thyristors now short out, producing a counter EMF voltage through the motor windings and a 1 ohm resistor, for braking.

When they are turning slowly the reels will spin freely because the voltage produced by the motor windings is insufficient to turn on the thyristors. This removes all braking effect when the reels are loaded manually.

CAPSTAN SERVO/CAPSTAN TACHOMETER

During a RUN NORMAL operation, a RAMP INPUT signal from the ramp generator is combined with dc feedback signal from the capstan tachometer to produce an extremely stable capstan speed. The ramp input to the Capstan Servo Amplifier is summed with the tachometer output at the source of Q32. (The STANDARD TACH output at P4-9 becomes TACH input on the Sequence Control.) R159 is the tachometer summing resistor, while the ramp summing resistor is located on the ramp generator. Any error voltage -- the difference voltage produced by summing ramp generator and tachometer input signals -- is fed to operational amplifier IC1. Output from IC1 is applied to complementary drivers Q27, Q28, Q29 and Q30. These transistors drive the output amplifiers stage to develop a dc voltage across the capstan motor. The motor then increases or reduces speed to produce a tachometer output voltage equal to that produced by the ramp generator.

Capstan amplifier gain is determined by the negative feedback loop around operational amplifier IC1. This consists of R143, R144, C31 and ZERO adjustment potentiometer R139. If the capstan turns when the tape is stopped, R139 requires adjustment. This procedure is covered in paragraph 4.14 of the maintenance section.

FET Q32 controls passage of the servo control output to the capstan op amps, drivers and amplifiers. This

FET is controlled by SERVO DISABLE input from Sequence Control. When the tape is tensioned normally (i.e., with all sensors false), SERVO DISABLE false (low) is applied to pnp transistor Q1 in the upper left hand corner of the schematic. It conducts, grounding the -10v supply connected to its collector. The gate of FET Q32 is enabled and it passes any available error voltage to the capstan servo drivers and amplifiers.

When SERVO DISABLE true is generated by the Sequence Control, the -10 volt supply connected to the collector of Q1 passes through diode CR1, disabling FET Q32 to disable the capstan servo signal as well as capstan motor current.

HIGH SPEED RELAY OUTPUT SIGNAL (P4-13)

A sampling of capstan tachometer output is amplified by operational amplifiers IC8 and 7. When tape speed exceeds 150 ips in the fast forward or rewind mode, the output produced by these op amps becomes sufficient to make Q31 conductive. This grounds and closes high speed relay K8 in the power supply which is connected to P4-13 through the wire harness. The relay will change the reference voltage of the center taps of the high voltage transformer, allowing the reel motors to smoothly accelerate the tape to 300 ips in either fast wind mode.

SUPPLY VOLTAGE SWITCHING

In order to decrease transistor power consumption and to lower their operating range, the supply voltage of the power transistors for the reel servos is switched on and off, depending on the voltage required to operate the servos. Comparator IC's 22 through 25 are connected as a Schmidtt trigger to detect the motor voltage and switch on and off transistors Q33, 34, 35 and 36. This, in turn, switches the supply path Darlington transistors on and off. These transistors are mounted on the heat sink. For example, the positive supply voltage for each servo is turned off when the motor voltage for the corresponding servo reaches -6v. The positive supply voltage is turned on when motor voltage reaches -3v. A diode mounted in the heat sink assembly references the supply to ground when the supply path Darlington transistor is turned off.

401-6666-101R

DASH NO.	101N	102M
SPEED	75 IPS	45 IPS
Q25	MPF161	OMIT

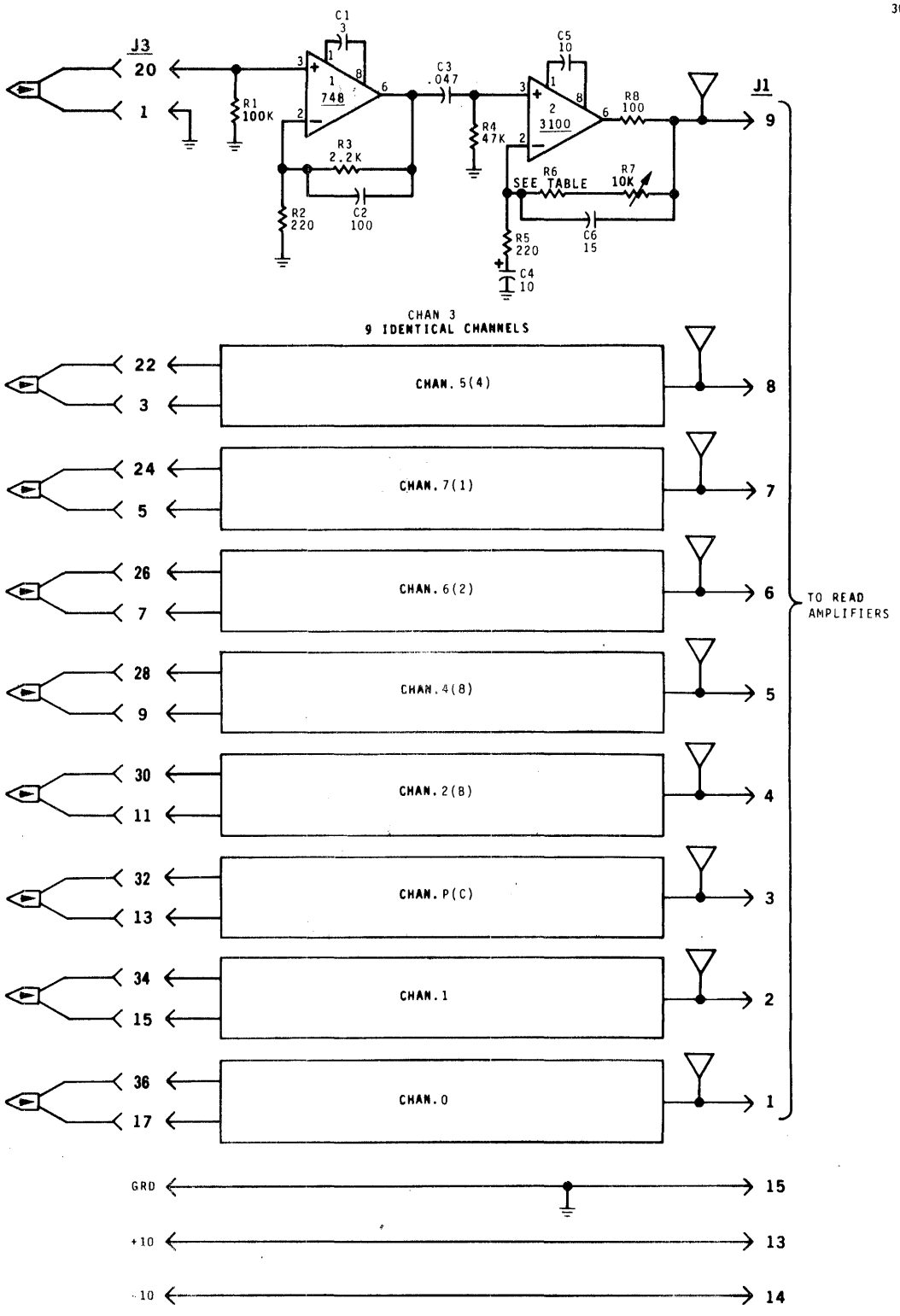
** DENOTES FACTORY SELECTED VALUE.

Servo Preamp - Model 9100
Type 6666,
Schematic Diagram

TYPE 5728 READ PREAMPLIFIER

CIRCUIT DESCRIPTION

This module contains nine identical high gain amplifiers which amplify the input signal from the read head and supply it to the read amplifier cards. Each amplifier stage consists of two operational amplifiers with negative feedback loops. Overall gain of each amplifier stage is controlled by its variable potentiometer, R7. It should be adjusted for 8 vdc (p-p) at the output.



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

DASH NO.	-001	-002	-003
HEAD	STANDARD	FERRITE	7 TRK
R1	100K	1.5K	100K
R6	3.3K	3.3K	1.8K

Read Preamp-Model 9100, TYPE 5728, Schematic Diagram

TYPE 6385 QUAD READ AMPLIFIER

CIRCUIT DESCRIPTION

This module contains four identical read amplifiers which detect, filter and digitize both 800 cpi NRZI and 1600 cpi PE read data. Two of the boards are employed in dual density transports to process the eight read data channels. The read amplifier for channel P is located on the Dual Density P Channel Clipping PC board. The operation of read amplifier channel A is explained below; the other read amplifiers operate identically.

NRZI Operation

Analog read data from the read preamplifier is input at pin E as SIG. Part of the signal is differentiated by resistor R2 and capacitor C1, then applied to the NRZI peak detectors IC10-9 and IC10-5. Part of the SIG input remains undifferentiated and is applied to the positive and negative clipper comparators at IC5-9 and IC5-5. Note that the output of all these comparators will be positive, since negative signal excursions are inverted at the comparator inputs.

The peak of the differentiated signal waveform exhibits a 90 degree phase advance with respect to the peak of the undifferentiated signal waveform at the clipper comparator outputs. This phase difference defines the length of the negative-going clock pulse applied to the NRZI read register, J-K flip-flop IC6.

During positive signal excursions, IC10-7 and IC10-12 go high, causing IC15-8 to go low. To eliminate spurious noise pulses, capacitor C6 delays the read signal. When the differentiated signal at IC10-9 passes the 0v reference point, IC15-8 goes high to eliminate spurious noise pulses. Capacitor C6 delays the signal slightly. Since this delay is a function of tape speed, the value of C6 varies accordingly. (See table on schematic.)

The low output pulse from inverter IC19-2 clocks NRZI Read Register IC6. The Q output at IC6-3 goes high, enabling NAND gate IC1 at pin 4. (NRZI signal at IC1-5 input remains true as long as the transport is selected, the tape is past load point and BUSY is false.) The low true digitized NRZI read data is output to the interface from pin Z.

When the NRZI read register is set, its Q/ output goes low, causing a low true DATA IN REGISTER/ pulse to be output to the Dual Density Control board. After an appropriate interval, a Reset Read Register (RESETR/) pulse will be clear the NRZI Read Register, making DATA IN REG/ false until the next NRZI read data bit is applied to the Read Register's clock input.

RESETR also pulses true to clear the NRZI Read Register when: LOAD POINT goes true, BUSY goes true, high density recording (PE mode) is selected, or the tape transport is deselected.

Incidentally, positive or negative NRZI excursions must exceed their respective clipping thresholds at IC10-10 and IC10-4. The purpose of the clipping levels is to eliminate spurious baseline noise pulses, requiring the analog signal supplied from the read preamplifier to exceed a certain amplitude before it is detected by the read amplifier stages. Different clipping levels are used during different modes of operation. The clipping level during a read only NRZI mode is 20 percent of the maximum peak-to-peak signal. During a read-after-write operation the clipping levels are raised to 33 percent of the maximum signal. During the interrecord gap the clipping levels are raised 7 percent higher than their values during the data block to reduce the probability of detecting random noise. When an error is detected in a read only mode and the transport is commanded to backspace over the erroneous block and reread it, the clipping levels are switched automatically to maximize the recoverability of marginally recorded data. First, the clipping levels are lowered to recover possible partial dropouts, and if the error is still detected the clipping levels are raised to eliminate possible high baseline noise spikes.

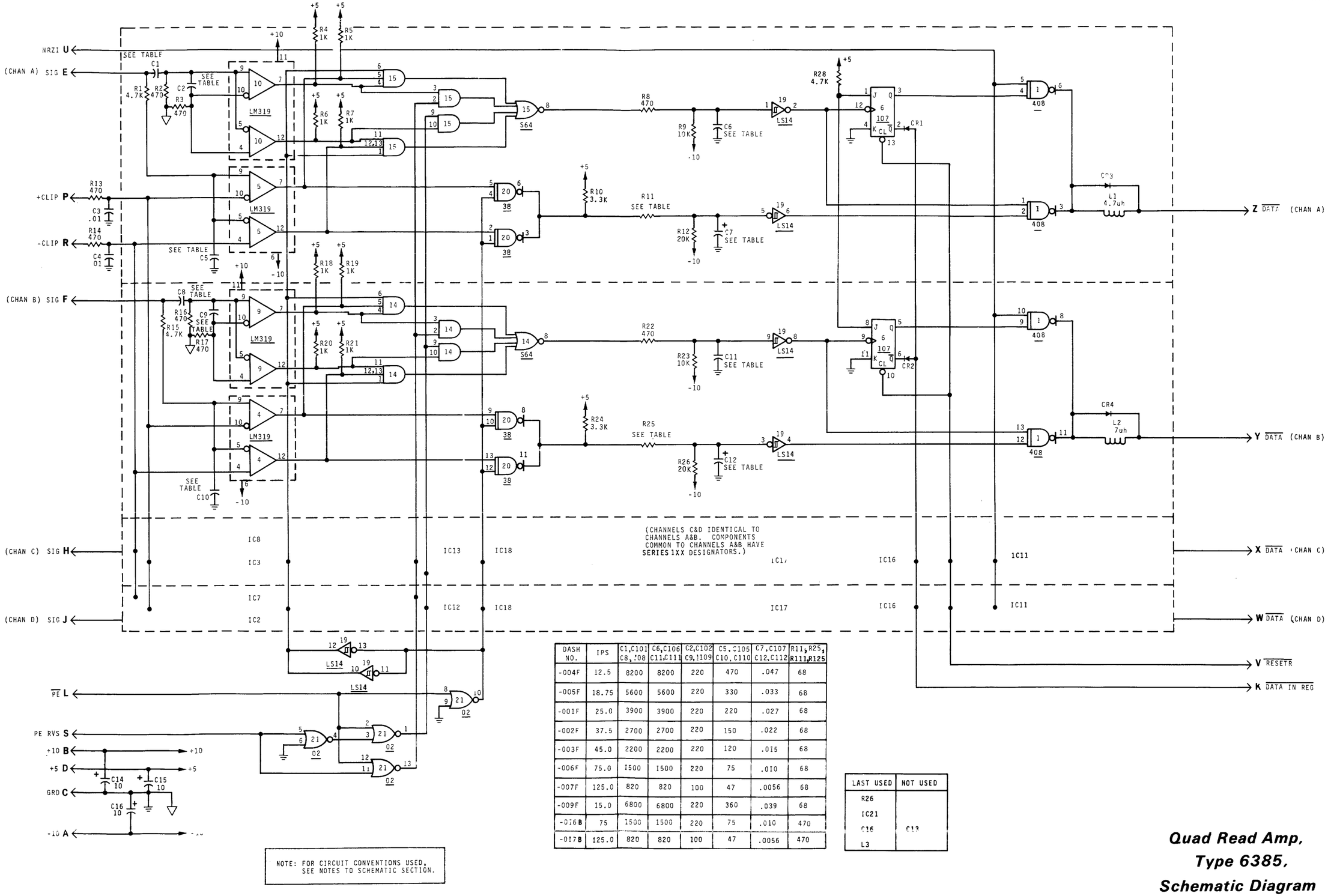
PE Operation

When High Density Status (HDS) true is output from the controller, PE true is generated on the Dual Density Control board and input on the Quad Read Amplifier at pin L. NRZI signal goes false, disabling the Q output of NRZI read register IC6 at NAND gate IC1-5.

To conform to the PE format, only positive PE read data excursions will be peak and threshold detected during a PE read forward operation. To accomplish this, AND gates IC15-9 is disabled by low signal from NOR gate IC21-1 to disable negative signal processing. Simultaneously, IC15-2 is enabled to pass any positive-going PE read data. During a read reverse PE operation, PE RVS goes true, enabling the negative transition processing gates and disabling the positive ones.

Note that the PE signal path to the DATA output now passes through NAND gate IC1-3. This gate is enabled at pin 1 because inverter IC19-2 goes high during each PE read data transition.

401-6385-001H



DASH NO.	IPS	C1,C101 C8,C108	C6,C106 C11,C111	C2,C102 C9,C109	C5,C105 C10,C110	C7,C107 C12,C112	R11,R25, R111,R125
-004F	12.5	8200	8200	220	470	.047	68
-005F	18.75	5600	5600	220	330	.033	68
-001F	25.0	3900	3900	220	220	.027	68
-002F	37.5	2700	2700	220	150	.022	68
-003F	45.0	2200	2200	220	120	.015	68
-006F	75.0	1500	1500	220	75	.010	68
-007F	125.0	820	820	100	47	.0056	68
-009F	15.0	6800	6800	220	360	.039	68
-016B	75	1500	1500	220	75	.010	470
-017B	125.0	820	820	100	47	.0056	470

LAST USED	NOT USED
R26	
IC21	
C16	C13
L3	

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Quad Read Amp, Type 6385, Schematic Diagram

TYPE 4365 DUAL DENSITY CONTROL

CIRCUIT DESCRIPTION

This module performs the following control functions:

a. Generates the read clock, supplies the READ REGISTER RESET signal to the NRZ1 data registers, and detects excessive skew

b. Detects the interrecord gap

c. Provides the interlocks required for the density selection

d. Supplies the reference frequencies for the write test

These operations are described below.

READ CLOCK, REGISTER RESET, AND SKEW DETECT NETWORK

The read clock and its related functions are performed as a function of a crystal generated master clock. The clock is produced by a master oscillator consisting of crystal Y1, transistors Q1 and Q2, and capacitor C4, connected in a feedback loop. The output clock of the oscillator is a square wave with a frequency equivalent to 64 times the 800 cpi data rate. (The master frequency is divided by two in transports with running speeds slower than 25 ips, by connecting flip-flop IC16 in the network.) The master clock is supplied to a skew counter consisting of two divide-by-16 counters, IC14 and IC17, in tandem. The counter is preset to one of three counts, depending on the mode of operation, and then counts up to its maximum count. During a read mode the skew count is 29, or approximately 45 percent of the character time. During a read-after-write mode the skew count is reduced to 21 (by WRITE READY activating NAND gate IC5-6), or approximately 33 percent of the character, and during the read test mode the count is reduced to 8, or approximately 13 percent of the character space. The skew gate is shortened during the read test mode to enable accurate alignment of the read head with respect to the tape path using an 800 cpi skewmaster tape.

When the leading channel detects data it supplies $\overline{\text{DATA IN REGISTER}}$ true at input pin H, setting the D input of flip-flop IC16 high. The succeeding master clock pulse clocks IC16 to the set state, the Q output going high to enable the skew counter to count. When the counter reaches its maximum count, the CARRY output of IC14 goes high and sets the D input of the first IC9 flip-flop high. The next master clock pulse clocks the flip-flop to the set state, and its Q output goes high to generate the read clock pulse through NAND gate IC5-3 (since the $\overline{Q}$ output of the third IC9 flip-flop is still high). The duration of the read clock is equivalent to two master clock intervals; the third master clock toggles IC9-15 to the set state, its $\overline{Q}$ output going low to terminate the output READ CLOCK pulse. The fourth clock pulse following the completion of the skew count toggles IC9-7 to the set state, its Q output going high to supply a RESET READ REGISTER RESETR pulse. RESETR clears the NRZ1 data register portions of the read amplifier stages, setting the $\overline{\text{DATA IN REGISTER}}$ signals of all nine read amplifier stages false. RESETR is also generated when signal C goes low. This occurs when any one of the following conditions is true: the transport is deselected (SLT1 going false), BUSY goes true, LOAD POINT goes true, or HIGH DENSITY is selected. Any of these conditions would clear the NRZ1 read registers.

The fourth clock pulse following the skew count completion also sets the input of D type flip-flop IC11 high. On the fifth pulse that flip-flop is toggled to the set state, its $\overline{Q}$ output going low to enable one-shot IC12 at pin 9. If one of the channels detects an additional character at this time its $\overline{\text{DATA IN REG}}$ goes true again, is inverted by IC1-6 and triggers the skew one-shot IC12 at pin 10. The $\overline{Q}$ output of the one-shot supplies a pulse through inverter IC2-6 that is used to illuminate the test panel skew indicator.

GAP DETECTION NETWORK

A 12-character delay is provided between the last character of the block and the GAP DETECT indication. The gap detection is performed by a network including flip-flop IC11, divide-by-16 counter IC13, and NAND gate IC7-3. During the data block $\overline{\text{DATA IN REGISTER}}$ (a wire-OR'd signal supplied from the nine read amplifier stages) remains true; it is inverted twice by IC1-6, IC7-6 and keeps counter IC13 cleared until the end of the data block. Following the last character in the block $\overline{\text{DATA IN REG}}$ goes high and the direct-clear is removed from IC13. At this time the $\overline{Q}$ output of flip-flop IC11 is high, the flip-flop having been clocked to the clear state when $\overline{\text{DATA IN REG}}$ first went true at the beginning of the block. Counter IC13 is then clocked by Ct, an 800

cpi data rate clock supplied from the clock dividing network including IC15 and IC18. Twelve clock counts into the gap IC13 activates NAND gate IC7-3; the output of the gate goes low and direct-sets flip-flop IC11, the $\overline{Q}$ output of IC11 going low to lock the counter while the Q output goes high and supplies $\overline{GAP\ DETECT}$ true at output pin K. $\overline{GAP\ DETECT}$ remains true until either the beginning of the next block or until the transport is deselected (SEL A going false).

DENSITY SELECT CIRCUITS

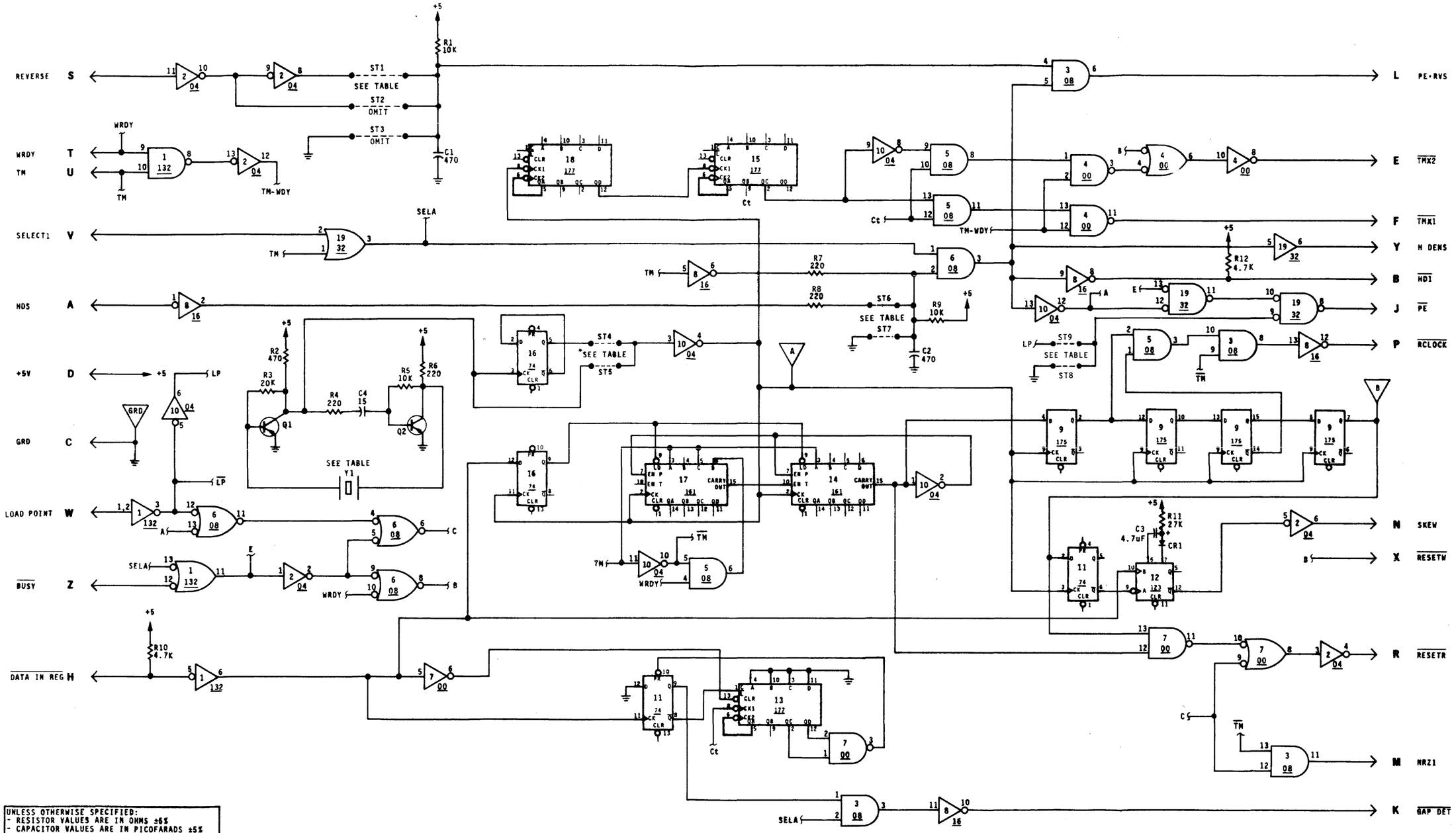
The NRZ1 800 cpi mode is selected either when the transport is selected and on line (SLT1 true, activating OR gate IC19-3) or when the transport is in the test mode (TM true at input pin U), provided that LOAD POINT is false and that HIGH DENSITY SELECTED is also false. If these conditions are satisfied then NAND gate IC3-8 is activated, supplying NRZ1 true at output pin M to enable the NRZ1 portions of the data electronics.

The high density is selected whenever the interface supplies HIGH DENSITY SELECT HDS true at input pin A of this card, the transport is selected and on line (SLT1 true), and not in the test mode (TM false). When these conditions are satisfied NAND gate IC6-3 is activated, supplying HIGH DENSITY true HDENS at pin Y and $\overline{HDI}$ true at pin B. If in addition to the above conditions the $\overline{BUSY}$ and the LOAD POINT status lines are both false, AND gate IC19-8 is activated, supplying PHASE ENCODED $\overline{PE}$ true at output pin J to enable the phase encoded portions of the data electronics.

WRITE TEST FREQUENCIES

The reference frequencies $\overline{TMX1}$ and $\overline{TMX2}$ are 800 cpi data rate square waves, 180 degrees out of phase, used to alternately set and reset the write amplifier flip-flops to generate the NRZ1 write test mode all-1 pattern.

These frequencies are generated by the divider network including IC15 and IC18 counters, which divides the master oscillator frequency into the data rate clock Ct. Ct is then gated through two IC5 NAND gates, with the Qc output of IC15 used to invert the phase of one frequency with respect to the other. The two test frequencies are then gated through the IC4 NAND gates when the write test mode is selected, indicated by both TM and WRITE READY being true. The two frequencies are then output at pins F and E as TMX1 and TMX2 and are supplied to the write amplifier cards.



UNLESS OTHERWISE SPECIFIED:
- RESISTOR VALUES ARE IN OHMS ±5%
- CAPACITOR VALUES ARE IN PICOFARADS ±5%
- NPN TRANSISTORS ARE 2N2714
- PNP TRANSISTORS ARE MPS6517
- DIODES ARE 1N914
- IC ARE TTL, 7400 SERIES
-- NUMBER IN LOGIC SYMBOL IS REFERENCE DESIGNATOR, UNDERLINED NUMBER IS IC TYPE. (IF 7400 SERIES, 74 IS OMITTED)
-- IC PIN 7 IS CONNECTED TO GROUND
-- IC PIN 14 IS CONNECTED TO +5V
-- UNUSED INPUTS OF IC MAY BE TIED TOGETHER OR TO +5V THROUGH RESISTOR (+V)
- (*) DENOTES FACTORY SELECTED VALUE. TYPICAL VALUE IS SHOWN
- FILTER CAPACITORS ARE NOT SHOWN BUT ARE IDENTIFIED BY CF ON PC BOARD

NOTE: DASH NUMBERS 10X ARE THE SAME AS 00X WITH ST6 OMITTED AND ST7 IN. 20X ARE THE SAME AS 00X WITH ST6 AND ST7 OMITTED.

*

DASH NO.	-004F	-005F	-001H	-002F	-003F	-006F	-013C		
IPS	12.5	18.75	25	37.5	45	75	45		
Y1	1.28	1.92	1.28	1.92	2.306	3.840	2.306		
ST4	STRAP	STRAP	OMIT	OMIT	OMIT	OMIT	OMIT		
ST5	OMIT	OMIT	STRAP	STRAP	STRAP	STRAP	STRAP		
ST2	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	STRAP		
ST6	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP		
ST7	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT		
ST8	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP		
ST9	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT		

NOTE: ST1 IS IN FOR READ REVERSE CAPABILITY WITH 9217 ONLY

Dual Density Control, Type 4365A
Schematic Diagram

TYPE 5771 SEVEN-TRACK DELAY TIMING MODULE

CIRCUIT DESCRIPTION

This module performs the following control functions:

a. Generates the read clock, supplies read register reset signal to the NRZI data registers and detects excessive skew.

b. Detects the interrecord gap.

c. Supplies the reference frequencies for the write test.

d. Selects one of the two available densities.

READ SKEW, REGISTER RESET AND SKEW DETECT NETWORK

The read clock and its related functions are performed by the crystal generated master clock. The clock is produced by a master oscillator consisting of crystal Y1 and IC20. The output of the oscillator is a 25.6 kHz squarewave. Signal F1, the master clock output, is inverted at IC12-3 and supplied to IC14, which is a divide-by-16 skew counter. This counter is preset to one of three counts (depending on the mode of operation), and then counts to its maximum count. During a read operation, the skew count is 15, or approximately 45% of the character time. During a read after write operation, the skew count is reduced to 11 (through load input C of IC14) or approximately 34% of the character time. During a read test the count is reduced to 4, or approximately 13% of the character time. The skew gate is shortened during the read test mode in order to enable accurate alignment of the read head with respect to the tape path.

When the leading channel detects data, it supplies $\overline{\text{DATA IN REG}}$ true to input pin H, setting the D input at flip-flop IC10-12 high. Next, a master clock pulse from f1 clocks IC10 to the set state, and the Q output goes high to enable skew counter IC14. When the skew counter reaches its maximum count, the carry out (C/O) output of IC14 goes high and sets the D input at flip-flop IC15-12 high. The next master clock pulse clocks IC15-11 to the set state and its Q output goes high to generate the read clock pulse through NAND gate IC9-3. The next master clock pulse resets IC15-9, since IC14 had been preloaded in the previous state. The duration of the read clock is therefore equivalent to one master clock interval ($\frac{1}{32\text{nd speed x density}}$). The third master clock pulse clocks IC15, pin 5 to the set state to supply reset read register true to the data registers of the read amplifier stages. This clears the data registers, setting the DATA IN REG signals of all nine read amplifiers false. $\overline{\text{RESET R}}$ is also generated when $\overline{\text{BUSY}}$ is true. The fourth clock pulse sets the Q output of IC16-9. If data in register signal is still true at this time (indicating bad skew), one shot IC19 fires and illuminates the skew indicator on the front panel for a fixed time delay.

GAP DETECTION NETWORK

A 12 character delay is provided between the last character of the block and the gap detect indication. Gap detection is performed by a network which includes flip-flop IC10 and counter IC11. During the data block, $\overline{\text{DATA IN REG}}$ (a wire or'd signal supplied from seven of the read amplifier stages) remains true; it is inverted twice by IC9-8 and IC13-11 to keep counter IC11 cleared until the end of the data block. Following the last character in the block, $\overline{\text{DATA IN REG}}$ goes false (high) and the direct clear is removed from IC11. At this time the Q output of flip-flop IC10 is high, since it was clocked to the clear state when DATA IN REG first went true at the beginning of the block. Counter IC11 is then clocked by a clock frequency equivalent to the data rate at the selected density. At count 12, IC12-11 goes low, direct setting IC10-5 and locking the counter. IC10-5 outputs the gap detect (GAP DET) signal, which is gated with LP, SLT1 and BUSY. GAP DET remains true until the beginning of the next block or until the transport is no longer selected.

DENSITY SELECT CIRCUITS

A dual density machine is either 200/556 cpi or 556/800 cpi. Switchable microswitch contacts S1-S4 are used to select either density pair. They are factory set for the density option chosen. Refer to the 5771 schematic table for the correct switch settings.

Within each option, the high or low density clock frequency is selected by the state of the HDS input from the interface. HDS true will select the higher density; HDS false selects the lower density. When HDS is true, HDI true will be returned to the interface, provided the transport is selected, not at load point and

not busy. The HDS LED will also be illuminated. The proper master clock frequency is automatically selected by IC1-8, IC1-6, IC2-6 and IC2-12.

WRITE TEST FREQUENCIES

The reference frequencies $\overline{TMX1}$ and $\overline{TMX2}$ are reverse phased 800 cpi data rate squarewaves. These frequencies alternately set and reset the write amplifier flip-flops to generate an all-1 test pattern for NRZI write testing. $\overline{TMX1}$ and $\overline{TMX2}$ are generated by a divider network consisting of IC4 and IC7. This network divides master oscillator frequency f1 to produce data rate clock fr. Clock fr is then gated with the QD output of IC7. This makes $\overline{TMX1}$ 180 degrees out of phase with respect to $\overline{TMX2}$. $\overline{TMX1}$ and $\overline{TMX2}$ are then buffered and gated through IC3. The $\overline{TMX1}$ and $\overline{TMX2}$ reference frequencies will only be output when the write test mode is selected (WRDY true and TM true).

401-5771-001 L

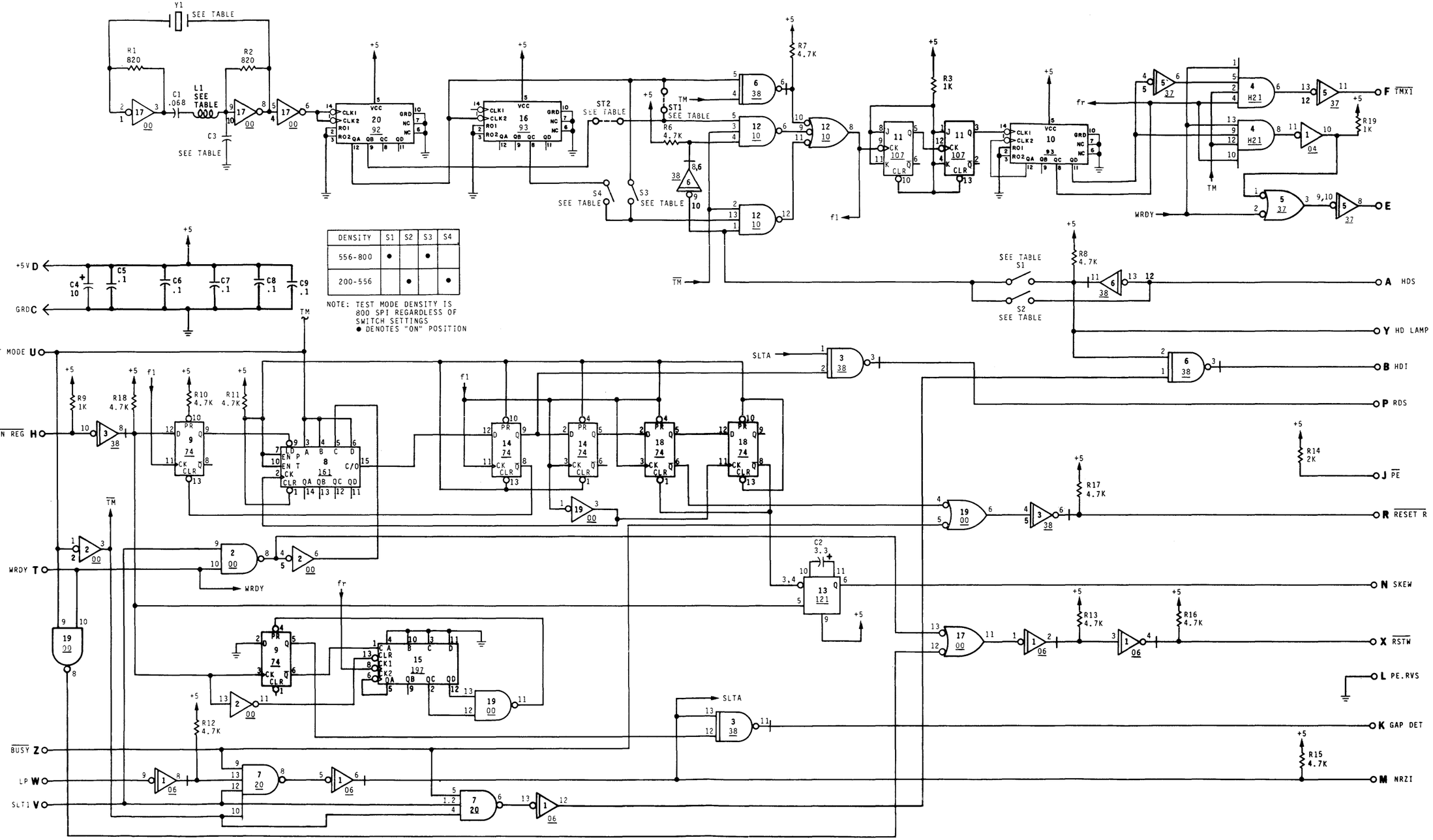
DENSITY	S1	S2	S3	S4
556-800	●		●	
200-556		●		●

NOTE: TEST MODE DENSITY IS 800 SPI REGARDLESS OF SWITCH SETTINGS
● DENOTES "ON" POSITION

DASH NO.	DENSITY	IPS	ST1	ST2	Y1	C3	L1
001	DUAL	125	STRAP	OMIT	6.4 MHz	OMIT	STRAP
101	TRIPLE	125	OMIT	STRAP	6.4MHz	OMIT	STRAP
002	DUAL	75	STRAP	OMIT	3.84MHz	220PF	4.7 uH
102	TRIPLE	75	OMIT	STRAP	3.84MHz	220PF	4.7 uH
003	DUAL	45	STRAP	OMIT	2.304MHz	680PF	4.7 uH
004	DUAL	112.5	STRAP	OMIT	5.76MHz	OMIT	STRAP

7 Track Delay Timing, Type 5771, Schematic Diagram

401-6771-001A



DENSITY	S1	S2	S3	S4
556-800	●		●	
200-556		●		●

NOTE: TEST MODE DENSITY IS 800 SPI REGARDLESS OF SWITCH SETTINGS
● DENOTES "ON" POSITION

DASH NO.	DENSITY	IPS	ST1	ST2	Y1	C3	L1
001A	DUAL	125	STRAP	OMIT	6.4MHz	OMIT	STRAP
101A	TRIPLE	125	OMIT	STRAP	6.4MHz	OMIT	STRAP
002A	DUAL	75	STRAP	OMIT	3.84MHz	220pf	4.7uH
102A	TRIPLE	75	OMIT	STRAP	3.84MHz	220pf	4.7uH
003A	DUAL	45	STRAP	OMIT	2.304MHz	680pf	4.7uH
004A	DUAL	112.5	STRAP	OMIT	5.76MHz	OMIT	STRAP

7 Track Delay Timing, Type 6771, Schematic Diagram

TYPE 6367 DUAL P CHANNEL /CLIPPING PC BOARD

CIRCUIT DESCRIPTION

This module contains the read amplifier stage for channel P as well as the automatic clipping level switching control. The operation of the read amplifier stage is identical to that of the read amplifier stages located on the 6385 Dual Density Quad Read Amplifier, and as described in the circuit description of that card. The generation of the clipping levels and their switching control is explained below.

The purpose of the clipping levels is to eliminate spurious baseline noise pulses, requiring the analog signal supplied from the read preamplifier to exceed a certain amplitude before it is detected by the read amplifier stages. Different clipping levels are used during different modes of operation. The lowest clipping threshold occurs during read only NRZI mode. This level is increased during read after write operations. During the gap the clipping levels are raised even higher to reduce the probability of detecting random noise. When an error is detected in a read only mode and the transport is commanded to backspace over the erroneous block and reread it, the clipping levels are switched automatically to maximize the recoverability of marginally recorded data. First the clipping levels are lowered to recover possible partial dropouts, and if the error is still detected the clipping levels are raised to eliminate possible high baseline noise spikes.

The main component used in producing the clipping level voltages is operational amplifier IC17. The output of IC17 is used as the negative clipping level, and is supplied to the P channel read amplifier stage on this card and to the read amplifier stages of the other channels through output pin R. Operational amplifier IC18 inverts the output of IC13, supplying the positive clipping level.

During the NRZI mode FET Q2 is turned off by Phase Encoded (PE) false. As a result, resistors R14 and R15 are included in the negative feedback loop of operational amplifier IC17. The +10v routed through resistor R11 provides the minimum input voltage to IC17, producing an output clipping level of approximately 0.4 volt. Other voltages are added to the input of IC17 through R16, R17, or R18, increasing the clipping level's amplitude as required by the particular mode of operation. Thus, during a read only operation, the voltage through R17 is combined with R11's voltage.

During a read after write mode, WRDY true at input pin J direct-sets flip-flop IC16-4. The Q output of IC12 then goes high to add the voltage through R18 to that used during the read mode. This increases the read-after-write clipping level.

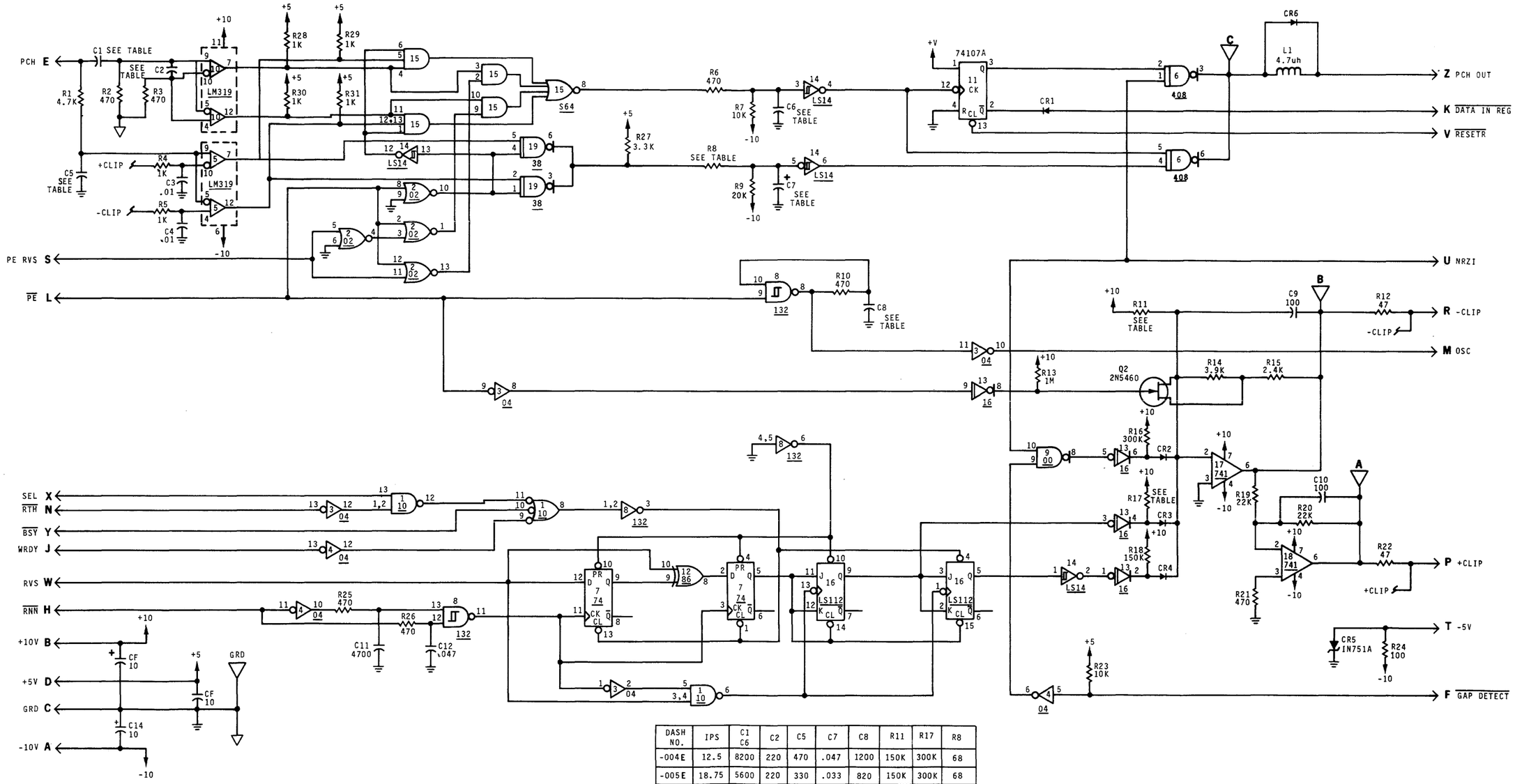
During the NRZI gap, GAP DET true at input pin F supplied from the Dual Density Control module is inverted by IC4-6 to activate NAND gate IC9-8, which adds the voltage through R16 to that used during the read only mode.

During a phase encoded operation, PE/ true (supplied at pin L from the Dual Density Control module) turns FET Q1 on, in effect bypassing R17 in the feedback loop of operational amplifier IC17. This reduces the output levels during PE.

The automatic clipping level switching is provided by the network including flip-flops IC7, IC16, exclusive - OR gate IC12 and associated circuitry. The circuit is used as a direction reversal indicator, the Q output of IC7-5 going high whenever the direction of motion is switched from reverse to forward or forward to reverse. Whenever two RUN NORMAL (RNN/) commands are given in the same direction, the Q output of IC7-5 goes low. The two J-K flip-flops of IC16 are connected as a divide-by-three counter, to count the number of direction reversals. If an error is detected during the read mode and the transport backspaces over the erroneous block, the Q output of IC7-5 goes high, setting the J-K input of IC16-11 high. During the second reread of the block, IC16-9 is toggled to the set state by a pulse formed on the leading edge of the RUN NORMAL (RNN/) command. The Q output of IC16-9 high is inverted at IC13-4, grounding resistor R17. This reduces the clipping levels during the second reread of the block. If an error is still detected, counter IC16 moves to the count of 2, with the Q output of the second IC16 flip-flop going high and that of the first going low. As a result, the voltages through R17 and R18 are added to the clipping levels, to increase the clipping threshold. During the next reread the voltage through R17 would be removed, further reducing the clipping level. The cycle would be repeated on the subsequent reread attempt.

The automatic switching is disabled if the transport interface supplies CLIPPING LEVEL DEFEAT (RTH/) true at input pin N, provided that the transport is selected. This would activate NAND gate IC1-12, to clear the IC7 flip-flops and direct set IC16-4. BUSY (BSY/) true or WRITE READY (WRDY) true would have the same effect.

401-6367-001E



DASH NO.	IPS	C1 C6	C2	C5	C7	C8	R11	R17	R8
-004E	12.5	8200	220	470	.047	1200	150K	300K	68
-005E	18.75	5600	220	330	.033	820	150K	300K	68
-001E	25.0	3900	220	220	.027	560	150K	300K	68
-002E	37.5	2700	220	150	.022	390	150K	300K	68
-003E	45.0	2200	220	120	.015	330	150K	300K	68
-006E	75.0	1500	220	75	.010	180	100K	1M	68
-007E	125.0	820	100	47	.0056	100	100K	1M	68
-009E	15.0	6800	220	360	.039	1000	150K	300K	68
-016B	75	1500	220	75	.010	180	100K	1M	470
-017B	125.0	820	100	47	.0056	100	100K	1M	470

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Dual P Chan/Clipping, Type 6367, Schematic Diagram

DUAL DENSITY WRITE SECTION

CIRCUIT DESCRIPTION

This is a composite schematic of the Type 4366A Four Channel Write Amplifier and the Type 4368A Five Channel Write Amplifier. Write channels P, 0, 1, and 2 are processed by the Type 4366A Write Amplifier, while write channels 3-7 are processed by the Type 4368A Write Amplifier.

WRITE AMPLIFIER OPERATION

Each write amplifier stage consists of two OR gates, an input buffer flip-flop, a delay counter, and a pair of drivers. The operation of the write channel P amplifier stage is explained; the other stages operate similarly.

Write data channel P signal from the transport interface is inverted and supplied to the J input of input buffer flip-flop IC8, as well as one input of OR gate IC7. Write data is processed differently, depending on whether the tape transport is operating in the PE mode or the NRZ1 mode.

In the NRZ1 mode, NRZ1 high from the Dual Density Control module is inverted and supplied to one input of OR gate IC7. During NRZ1 high, this gate will pass the NRZ1 data without inverting it. Each time the input NRZ1 data goes low, both the J and K inputs of the input buffer flip-flop are set high. The WRITE DATA STROBE (WDS) from the interface now toggles the input buffer flip-flop to the opposite state. Thus for each 1 input, a polarity transition is recorded on tape. When the input data is high, containing a logic 0, the J and K inputs of the buffer flip-flop are set low. Thus the flip-flop does not change states when clocked by the WRITE DATA STROBE.

In the PE mode, NRZ1 false is inverted, causing OR gate IC7 to become an inverter. Now the input buffer flip-flop stores the input logic states whenever clocked by the phase encoded 3200 fci WRITE DATA STROBE. In the PE mode the data lines are already encoded in the formatter.

The input buffer flip-flop will store the data until the delay counter of the respective stage reaches its maximum count. The delay counter of each stage digitally deskews the write data, using channel P as a fixed reference. Although the delay counter of channel P is permanently preset to the count of 8, the counters of write data channels 0-7 can be preset to any count, using switches to either ground or open their parallel inputs. These delay counters are clocked by a reference frequency (Cx) at approximately 80 times the 800 cpi data rate, 40 times the 1600 cpi data rate, or 20 times the fci rate. Generated by an oscillator circuit, this clock advances each delay counter from the preset count until it reaches the maximum count of 16. At this point the Q_d output of the delay counter will clock the respective output register flip-flop. This transfers data from the input buffer to the output of the amplifier stage, where a pair of drivers energizes the respective head winding.

Write data deskewing is performed by manually adjusting the switches of one channel at a time until the output of that channel, as displayed on an oscilloscope connected to the Read Preamplifier module, coincides with channel P. The write deskewing compensates for the physical displacement of the channels with respect to each other on the write head. The write deskewing procedure does not correct for the misalignment of the head with respect to the tape path. The delay counter switches are preset in the factory and normally their positions should not be changed unless the write head has to be replaced. In that case the new factory supplied head is provided with a tag showing the new delay counter switch positions, as required to compensate for the new head's characteristics. Should readjustment become necessary, follow the write deskewing procedure outlined in the maintenance section of this manual.

WRITE TEST MODE

When the transport is in the write test mode, input frequencies TMX1 and TMX2 from the Dual Density Control module alternately set and reset the input data buffer flip-flops of each write amplifier stage, generating the required NRZ1 all-1 test pattern on the tape. TMX2 true pulse also fires one-shot IC5. This disables WRITE AMPLIFIER RESET (WARS) from the interface, permitting the tape to be written on during the test mode without disconnecting the Model 9100 from the interface.

TYPE 4368A AMPLIFIER OPERATION

The operation of these write amplifiers is identical to that of the Type 4366A Four Channel Write Amplifier module described above.

DUAL DENSITY WRITE SECTION

CIRCUIT DESCRIPTION

This is a composite schematic of the Type 5366 Four Channel Write Amplifier and the Type 5368 Five Channel Write Amplifier. Write channels P, 0, 1, and 2 are processed by the Type 5366 Write Amplifier, while write channels 3-7 are processed by the Type 5368 Write Amplifier.

WRITE AMPLIFIER OPERATION

Each write amplifier stage consists of two OR gates, an input buffer flip-flop, a delay counter, and a pair of drivers. The operation of the write channel P amplifier stage is explained; the other stages operate similarly.

Write data channel P signal from the transport interface is inverted and supplied to the J input of input buffer flip-flop IC8, as well as one input of OR gate IC7. Write data is processed differently, depending on whether the tape transport is operating in the PE mode or the NRZ1 mode.

In the NRZ1 mode, NRZ1 high from the Dual Density Control module is inverted and supplied to one input of OR gate IC7. During NRZ1 high, this gate will pass the NRZ1 data without inverting it. Each time the input NRZ1 data goes low, both the J and K inputs of the input buffer flip-flop are set high. The WRITE DATA STROBE (WDS) from the interface now toggles the input buffer flip-flop to the opposite state. Thus for each 1 input, a polarity transition is recorded on tape. When the input data is high, containing a logic 0, the J and K inputs of the buffer flip-flop are set low. Thus the flip-flop does not change states when clocked by the WRITE DATA STROBE.

In the PE mode, NRZ1 false is inverted, causing OR gate IC7 to become an inverter. Now the input buffer flip-flop stores the input logic states whenever clocked by the phase encoded 3200 fci WRITE DATA STROBE. In the PE mode the data lines are already encoded in the formatter.

The input buffer flip-flop will store the data until the delay counter of the respective stage reaches its maximum count. The delay counter of each stage digitally deskews the write data, using channel P as a fixed reference. Although the delay counter of channel P is permanently preset to the count of 8, the counters of write data channels 0-7 can be preset to any count, using switches to either ground or open their parallel inputs. These delay counters are clocked by a reference frequency (Cx) at approximately 80 times the 800 cpi data rate, 40 times the 1600 cpi data rate, or 20 times the fci rate. Generated by an oscillator circuit, this clock advances each delay counter from the preset count until it reaches the maximum count of 16. At this point the Q_d output of the delay counter will clock the respective output register flip-flop. This transfers data from the input buffer to the output of the amplifier stage, where a pair of drivers energizes the respective head winding.

Write data deskewing is performed by manually adjusting the switches of one channel at a time until the output of that channel, as displayed on an oscilloscope connected to the Read Preamplifier module, coincides with channel P. The write deskewing compensates for the physical displacement of the channels with respect to each other on the write head. The write deskewing procedure does not correct for the misalignment of the head with respect to the tape path. The delay counter switches are preset in the factory and normally their positions should not be changed unless the write head has to be replaced. In that case the new factory supplied head is provided with a tag showing the new delay counter switch positions, as required to compensate for the new head's characteristics. Should readjustment become necessary, follow the write deskewing procedure outlined in the maintenance section of this manual.

HEAD CURRENT REFERENCE

In the NRZ1 mode, both pairs of drivers are actuated to pass full write current to the head. In the PE mode, IC17 and IC19 are disabled by NRZ2 false. Only IC18 and IC20 are enabled, which decreases write current to the proper level for PE operation.

WRITE TEST MODE

When the transport is in the write test mode, input frequencies TMX1 and TMX2 from the Dual Density Control module alternately set and reset the input data buffer flip-flops of each write amplifier stage, generating the required NRZ1 all-1 test pattern on

the tape. TMX2 true pulse also fires one-shot IC5. This disables WRITE AMPLIFIER RESET (WARS) from the interface, permitting the tape to be written on during the test mode without disconnecting the Model 9300 from the interface.

TYPE 5368 AMPLIFIER OPERATION

The operation of these write amplifiers is identical to that of the Type 5366 Four Channel Write Amplifier module described above.

4-CHANNEL WRITE AMPLIFIER
5366

5-CHANNEL WRITE AMPLIFIER
5368

401-9300-002 H

5366 DASH NO.	MODEL	SPEED A (IPS)	C4	R16,R17 R20,R21 R24,R25 R28,R29	R18,R19 R22,R23 R26,R27 R30,R31	ST1	C*
-001D	9300	125	270	390	330	OMIT	ON CUT
-002B	9100 / 9300	75	470	390	330	OMIT	NO CUT
-003B	9100	45	680	390	330	OMIT	NO CUT
-201B	9000	25	1200	510	470	OMIT	NO CUT
-202B	9000	37.5	820	510	470	OMIT	NO CUT
-203B	9000	45	680	510	470	OMIT	NO CUT
-204B	9000	12.5	2200	510	470	OMIT	NO CUT
-205B	9000	18.75	1500	510	470	OMIT	NO CUT
-501A	9100	75	470	390	330	STRAP	CUT
-502A	9000	37.5	820	510	470	STRAP	CUT

5368 DASH NO.		SPEED A (IPS)		R2,R3,R7 R8,R12 R13,R17 R18,R22	R4,R5,R9 R10,R14 R15,R19 R20,R24	
-001		75 TO 125		390	330	
-201		12.5 TO 45		510	470	

NOTE: ALL CHANNELS IDENTIFIED BY (1) ARE IDENTICAL TO CHAN 2

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Dual Density Write Section
Type 5366, 5368,
Schematic Diagram

4-CHANNEL WRITE AMPLIFIER 4366A

5-CHANNEL WRITE AMPLIFIER 4368A

401-9100-002F1

HEAD DR. FROM SA- 15
WDS FROM INTERFACE 7 (2)
TMX1 FROM DDC-F 5
TMX2 FROM DDC-E K
WARS FROM INTERFACE J (2)
RESETW FROM DDC-X 10
PE FROM DDC-J 6
WDP 11
WD0 12
WD1 13
WD2 14
FROM INTERFACE (2)
TO WRITE HEAD

SEE TABLE
MJE253
-503 ONLY
SKEW SWITCH
CHAN P
CHAN 0
CHAN 1 (IC15,16,17)
CHAN 2 (IC18,19,20)
HEAD CT
WDS1
M WARS
WCLEAR
CLOCK
RESETW
COUNT CD
CHAN P
CHAN 0
CHAN 1
CHAN 2

TMX1 5
PE 6
WD3 J
WD4 K
WD5 L
WD6 11
WD7 12
S1 CHAN 3 (1) (IC2,3,4)
S2 CHAN 4 (1) (IC6,7,8)
S3 CHAN 5 (1) (IC10,11,12)
S4 CHAN 6 (1) (IC13,14,15)
S5 CHAN 7 (1) (IC16,17,18)
CHAN 3
CHAN 4
CHAN 5
CHAN 6
CHAN 7

*SEE CAP @ IC4-8 (IC4 IS 846)

4366A	-001E	-002E	-003E	-004E	-005E	-006D	-103D	-106D	*-503C	-009B
IPS	25	37.5	45	12.5	18.75	75	45	75	45	15
C4	1200	820	680	2200	1500	390	680	390	680	1800
R16,R17 R19,R20 R22,R23 R25,R26	240						180, 1W		240	240
R1,R2,R3	120						100		120	120
R4	180						100		180	180

4368A	-001B	-101A
R2,R3 R5,R6 R8,R9 R11,R12 R14,R15	240	180, 1W

Dual Density Write Sect., Type 4366A, 4368A, Schematic Diagram

SECTION VII
GENERAL INFORMATION AND APPENDIX

DIGITAL RECORDING ON MAGNETIC TAPE USING NRZ1 CONVENTIONS AND FORMAT

1.1 INTRODUCTION

There are many recording techniques that may be employed to record digital information onto magnetic tape. Some of these are: non-return-to-zero (NRZ), return-to-zero, phase-encoded, Manchester coding, and NRZ1. Of these methods the NRZ1, non-return-to-zero change at logic 1, has been most widely accepted for recording parallel data onto multitrack recorders. This method has been used by IBM and other computer manufacturers for many years, and packing densities, formats, and mechanical dimensions have been fairly well standardized by usage throughout the industry.

1.1.1 IBM COMPATIBLE

The term IBM compatible, or more specifically IBM compatible 2400 series, is found frequently in specifications of tape units manufactured by companies other than IBM. This means that a tape written on a machine that is IBM compatible can be successfully entered into an IBM computer utilizing the IBM 2400 series of magnetic tape units. The converse, of course, is also true. Tapes written on an IBM 2400 can be read on IBM compatible tape units equipped with the read function.

This common denominator between systems is important, for often it is the only common point between computer systems and data acquisition systems. The parameters that ensure this compatibility relate to track width, number of tracks, position of the tracks on the width of the tape, form of check characters, spacing of check characters from data, length of interblock gaps, length of file gaps, and the character used to identify a file gap, as well as the mechanical dimensions of reels and hubs. This note describes these factors for the IBM compatible NRZ1 method of recording.

1.1.2 ADVANTAGES OF NRZ1 RECORDING METHOD

In the NRZ1 method of recording, current is flowing in one direction in the magnetic head at all times it is writing. This factor makes it possible to record over old data, erasing the old data as the recording is taking place. Head current also flows in a uniform direction during the interrecord gap. This is useful when it is necessary to rewrite a record or skip a bad area of tape found on re-read and allows the head current to be turned on again in a known direction without causing unwanted spikes.

Another advantage of the NRZ1 system is that the electronics for writing and reading are simpler than those required for other recording techniques, such as phase encoding.

A disadvantage of the NRZ1 system is that it is not self-clocking and is useful only where multiple track recording is employed. A further restriction is that in order to derive a clock from the multiple tracks, at least one of the tracks must have a one in it for each byte or character recorded. This last factor is ensured when a parity check is employed and the parity is odd. If even parity is used, then of course the all-zero character must be declared invalid and not used during the block.

1.2 WRITING NRZ1 TAPES

To record digital data on magnetic tape, it is necessary to magnetize the tape discretely to indicate binary ones and zeros. In the NRZ1 method, current is flowing in the head at all times the magnetic tape unit is in the write mode. As long as the head current does not change, the data will be written such that it will be interpreted as zeros. When a transition occurs between saturation magnetism (plus and minus) on the tape, this will be interpreted as a one. Figure 1-1 shows typical waveforms for data recorded on tape in the pattern 011010. The data is entered together with write clocks as shown, with a write clock for each bit recorded. With tape in continuous motion, a flux pattern corresponding to the tape magnetization will appear on the tape as shown.

NRZ1 recording is implemented by driving current through the head winding in a direction determined by a flip-flop that toggles for each one, gated in by coincidence between data and a write clock.

1.3 READING NRZ1 RECORDINGS

To recover the data written in NRZ1 format, the tape is moved at a constant velocity past the gap in the head. Refer to Figure 1-2. If the same pattern shown above is present on the tape, the head voltage

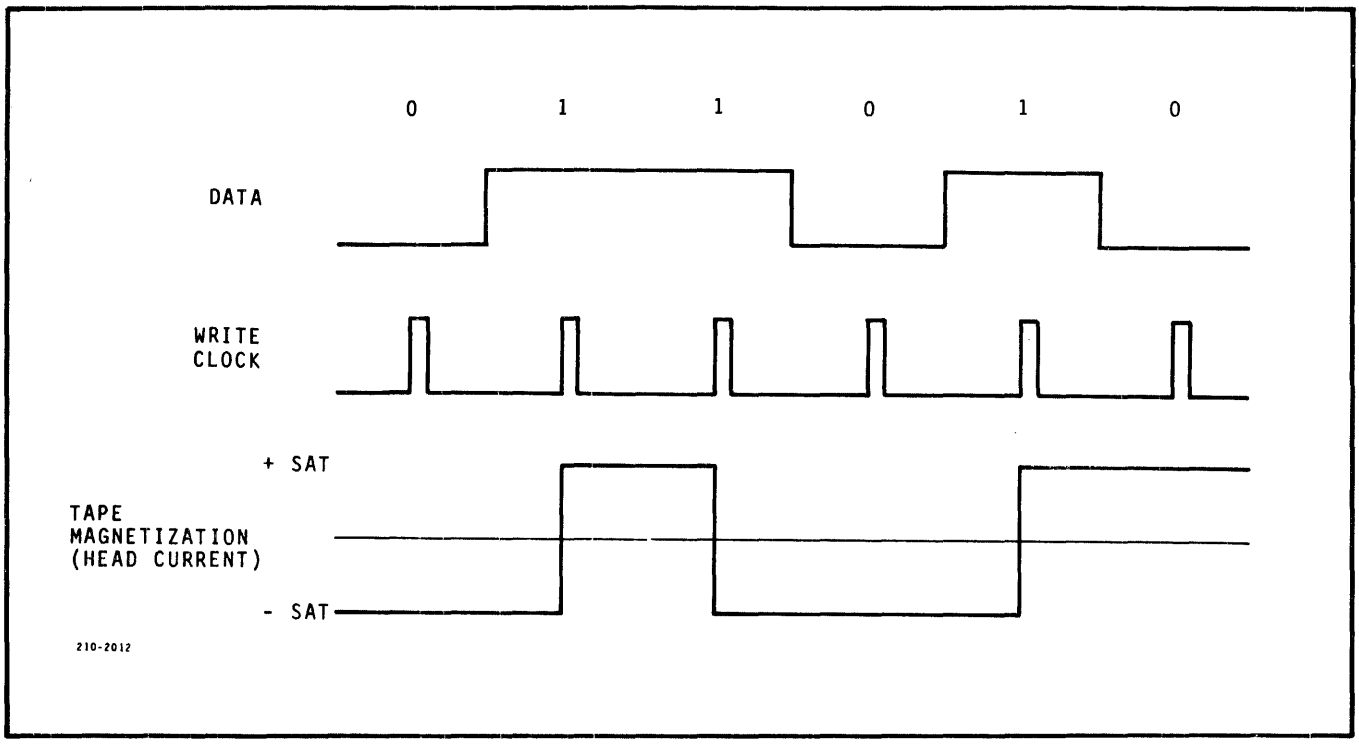


Figure 1-1 NRZ1 Waveforms - Writing

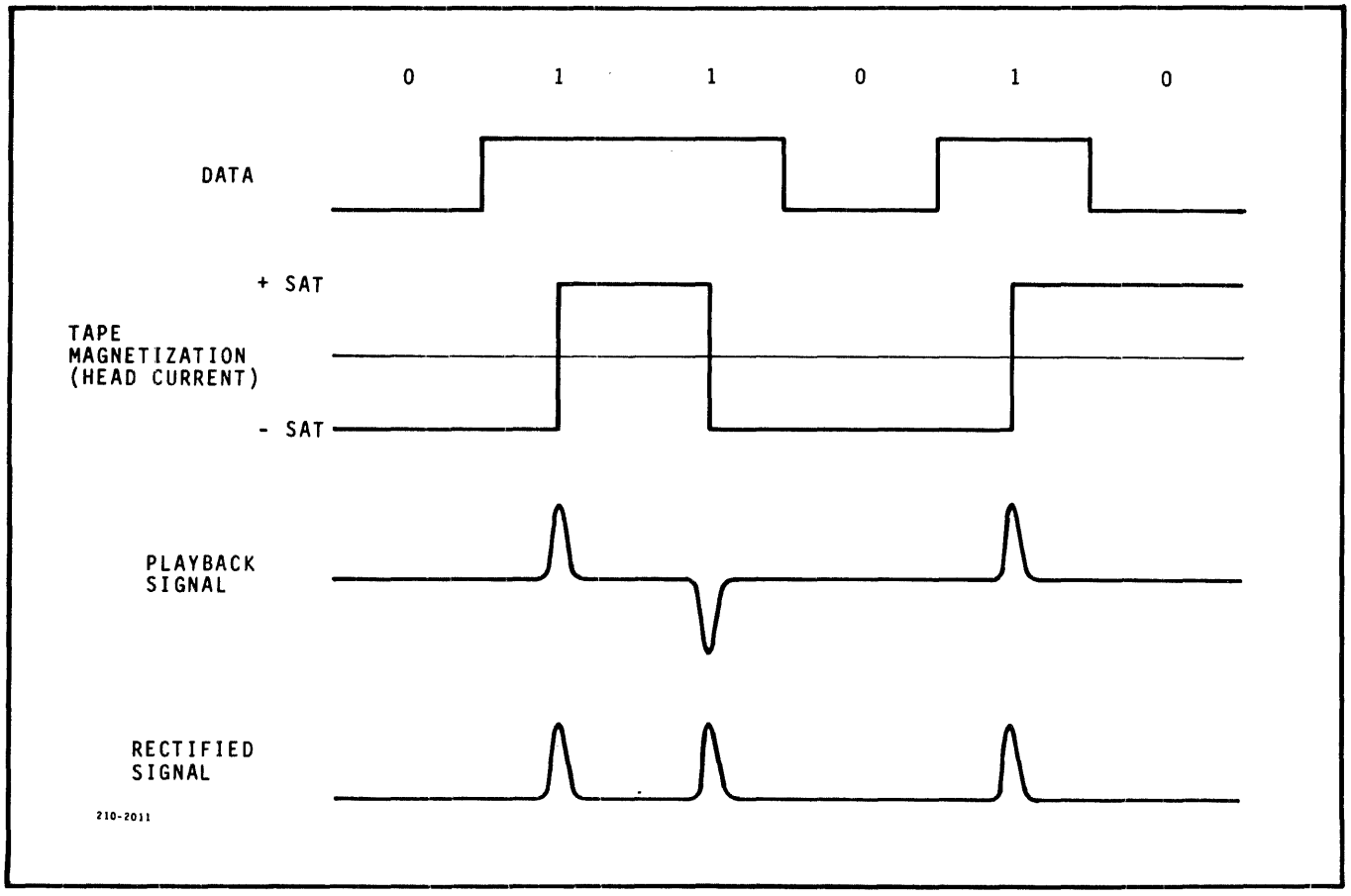


Figure 1-2. NRZ1 Waveforms - Reading

will look like the playback signal since the voltage induced in the head is the differential of the flux pattern on the tape. The characteristic half sine wave results from the fact that the gap on the head has a finite width.

The pattern shown is typical of what would be seen with 200 bits per inch (bpi) recording. As the recording density increases, the mechanical dimensions of the head remain the same, resulting in the same waveform but with the individual waves crowded close together. This ultimately presents a limit beyond which this type of recording is useful with state-of-the-art tapes and magnetic heads. Recording of 800 bpi seems to be a practical limit and is the maximum density utilized in present-day systems.

The playback signal is then rectified and, as can be seen from the figures, a pulse is present for every one recorded and the base line remains stationary for all zeros recorded. Note, however, that it is not practical to derive an accurate clock from the signal on the basis of a single-track recording. However, since this is a multiple track system and employs a parity generator, a data bit will be found on one of the multiple tracks for each character written, assuming that an all-zeros character is not employed in conjunction with even parity.

Considering the above factors, a typical read amplifier consists of an analog amplifier, a rectifier, a peak detector, suitable logic to create a clock, and an output buffer stage to enable interfacing to the customer's unit.

1.3.1 SKEW AND GAP SCATTER

Another major factor that limits the design of an NRZ1 multiple track system is that heads are not perfect because of gap scatter and head mounting to decks is not perfect causing skew. Both these factors have the same effect in that the signals from all the tracks do not occur perfectly in unison. The problem is minimal if the same head and deck are used for reading and writing a given tape, but since interchangeability of tapes between machines is mandatory provisions must be made to cancel out these effects. The allowable tolerances in head manufacture have practical limits and are typically in the ±50 microinch region for high quality heads. Fixed heads without adjustment are practical with 200 bpi and 556 bpi recording, but 800 bpi recording requires adjustments.

All Kennedy recorders are equipped with the necessary deskewing adjustment to enable operation and assure compatibility with other magnetic tape units. These adjustments take the following form.

1.3.1.1 Read Head Alignment

The read head is adjusted so that its gaps are perpendicular to the direction of tape motion using an IBM skewmaster tape. A mechanical adjustment is provided consisting of a spring loaded mounting plate working against a fine pitch adjusting screw. (On incremental and some low density machines this adjustment is either not required or is made by shimming tape guides.)

1.3.1.2 Read Electronic Deskew Register

All Kennedy read amplifiers are provided with a deskewing register. This register allows a total skew of 50 percent for all reasons including write head gap scatter, dynamic read skew, read head misalignment, and speed variation in writing or reading.

1.3.1.3 Write Electronic Deskewing (continuous tape units only)

The mechanical relationship between the read gap and the write gap is fixed in any given read after write head. Since the read head is adjusted perpendicular to tape motion (paragraph 1.3.1.1), the write time for each channel may be delayed selectively so that a character is written on the tape perpendicular to tape motion. In Kennedy continuous tape units a fixed delay is inserted for one channel and individual delays are provided for the remaining channels. This arrangement allows each channel to be adjusted in exact relationship to the fixed channel and allows adjustment for skew and gap scatter as well.

1.4 TAPE FORMATS

There are other factors that affect compatibility in addition to density and recording method:

a. Tape markers
b. Gaps
c. Check characters
d. Codes

1.4.1 TAPE MARKERS

When recording on magnetic tape, care must be taken to avoid physical handling and damage to the recorded surface. A portion of tape — at least 10 feet — at each end is reserved for threading and loading and is not used for storing data. To define the recorded area, pressure sensitive reflective markers are applied to the nonoxide side of the tape as shown in Figure 1-3.

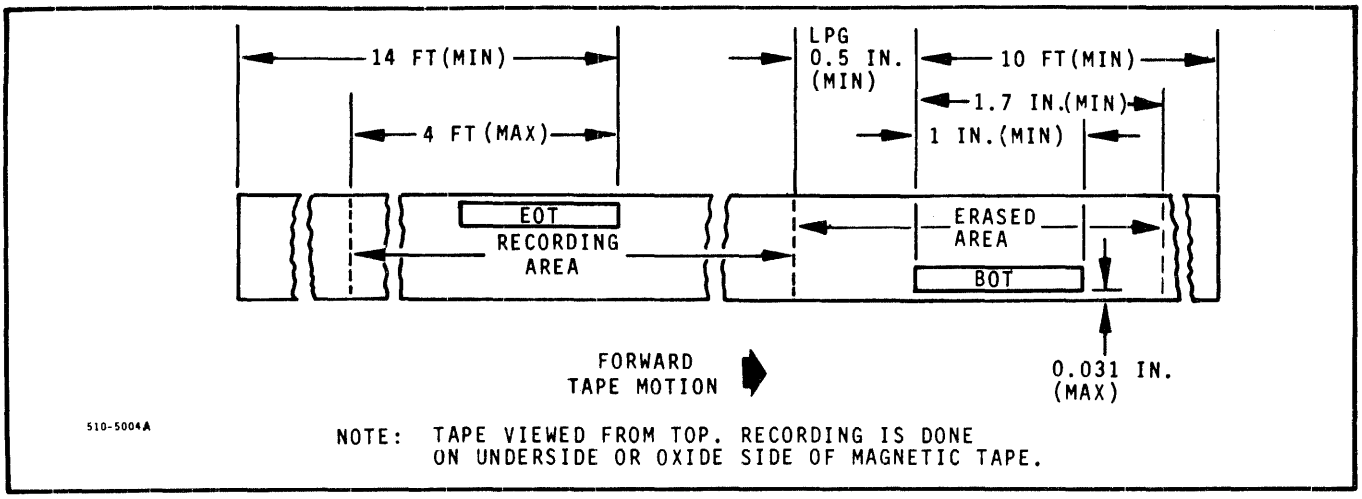


Figure 1-3. Tape Markers

These markers are sensed optically and define the recorded area in a standardized manner.

The BOT marker signal is used internally to define the load point or starting of recording. The EOT marker signal is not used internally but is available to the interface as an end of tape warning signal and should be used by the unit interfaced to the magnetic units to terminate recording within the next 4 feet of tape.

1.4.2 GAPS

Tape reading can only take place reliably when tape is moving at a known speed across the head. To allow tape to start and stop while the computer manipulates data, a section of tape with no data is provided between records or blocks of data and at the beginning and end of tape. This section is recorded with the head current turned on in the direction defined as erased and results in a constant flux in a predetermined direction which is independent of tape speed or motion. The direction of current in the heads defining the erased condition is also controlled to be uniform in all recorders. On readback this flux is constant as the tape accelerates and decelerates. Since a change in flux is required for the read head to sense data, no signal occurs and orderly starts and stops may be made.

Mechanical limitations preclude instantaneous starts and stops, and a distance of tape must be reserved, conditioned by the requirements of the "worst case" machines, to use the standards. While high speed units (IBM 2400 series) set the length of the gaps, Kennedy recorders utilize the full gap length to advantage by providing controlled acceleration and deceleration, resulting in minimum stresses to the tape.

1.4.2.1 Beginning of Tape Gap

An erased section of tape is required surrounding the BOT marker. This serves as a defined area within which data recording or reading can start. To comply with IBM specifications this section extends a minimum of 1.7 inches ahead of the trailing edge of the BOT marker and extends a minimum of 0.5 inch past the trailing edge of the BOT marker. In nearly all systems (including IBM) this erased section totals about 3.5 inches (Figure 1-3).

1.4.2.2 Interrecord Gaps

Interrecord gaps are areas, without data, placed between data blocks or records as shown in Figure 1-4. The length of the gap is 0.75 inch minimum for seven-track systems and 0.60 inch minimum for nine-track

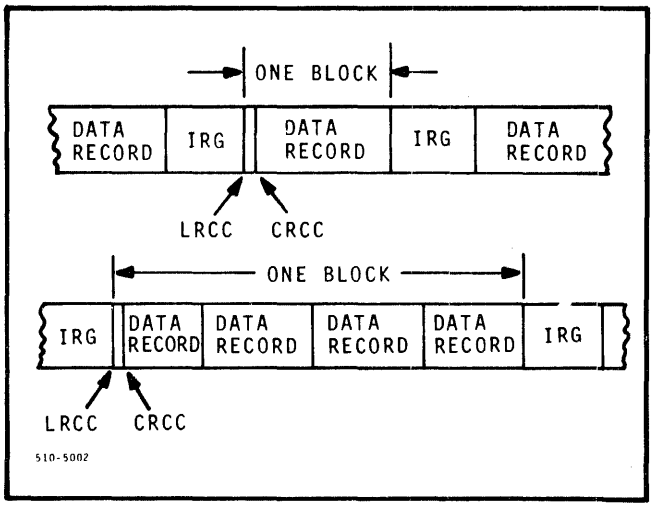


Figure 1-4. Interrecord Gaps

systems. The maximum length is not critical. The USA Standard Institute specifies the maximum length at 25 feet.

If records are short it can be seen that a large portion of the tape is used for interrecord gaps. In many cases computers are programmed to handle records in batches as shown in Figure 1-4. In this case the IRG and check characters are inserted on a block basis.

Figure 1-5 shows the format of the file mark for seven- and nine-track tapes. The distinguishing feature of the block is the fact that it is a single specific character record with a check character. The erased gap itself is nearly always used but IBM standards state that it is optional.

1.4.3 CHECK CHARACTERS

The NRZ1 format provides for both vertical and horizontal parity checks. In the nine-track system an additional check called the cyclic redundancy check character is used. Refer to Figures 1-6 and 1-7 for the location of the check characters.

The check characters define to a very high level of confidence that a block that is read is accurate.

1.4.3.1 Vertical Parity

Seven-track and nine-track systems use six and eight tracks respectively for recording data. The remaining track is redundant and carries the parity information. When the data is written on tape, a parity generator senses the input data and determines if the number of bits in the byte is odd or even. It outputs a "1" or a "0" to the redundant track to make the count odd if odd parity is selected, or even if even parity is selected.

On readback a similar circuit can be used to count the number of bits in each byte and determine if the count is odd or even. Depending on which is defined as correct, it signals the error line if the count is wrong. Thus each byte is checked. However, if an even number of bits is dropped the test will not result in an error signal, so an additional check called longitudinal parity is employed.

Odd or even parity may be selected on seven-track recorders. Nine-track recorders are always odd parity.

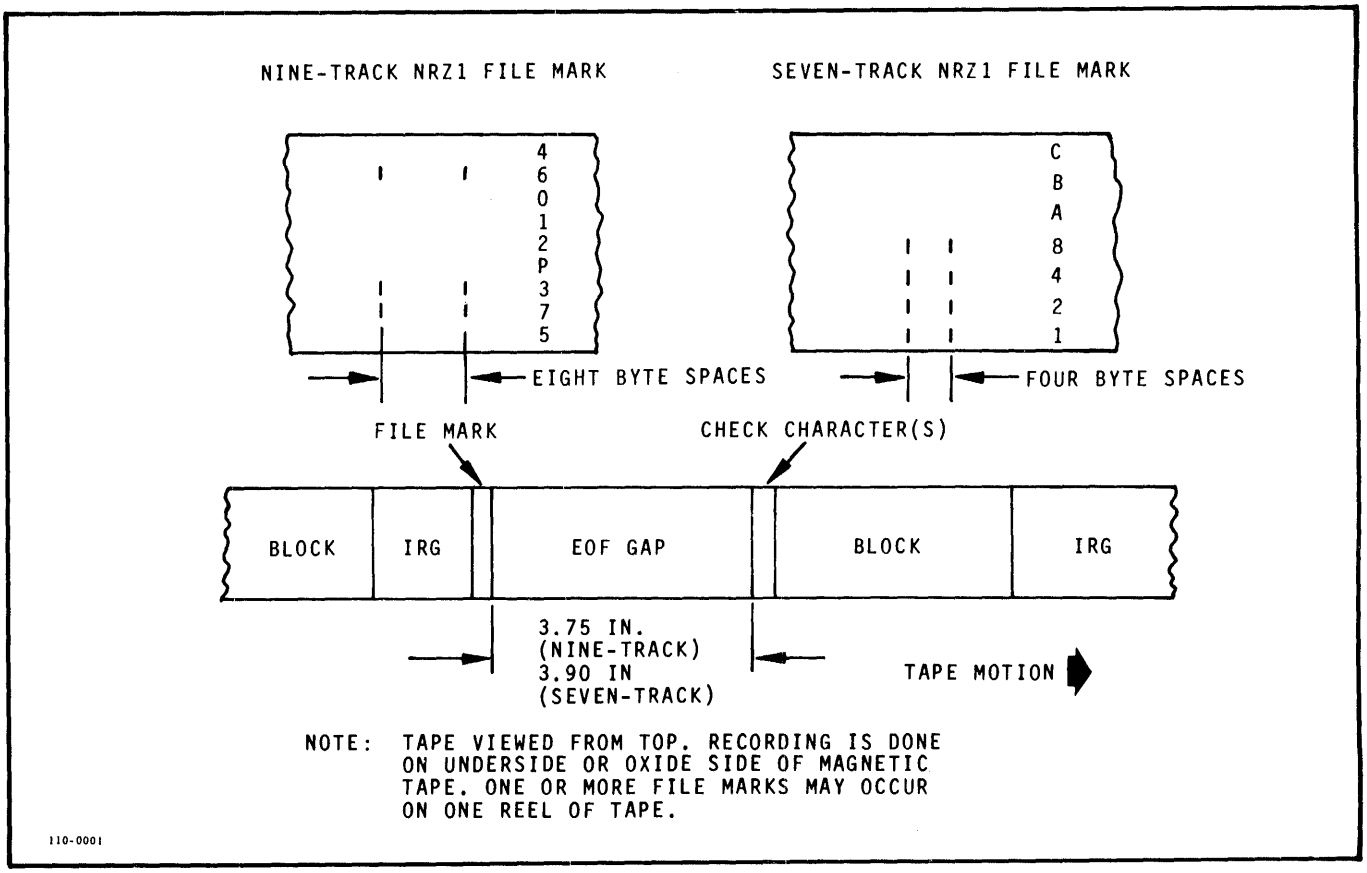
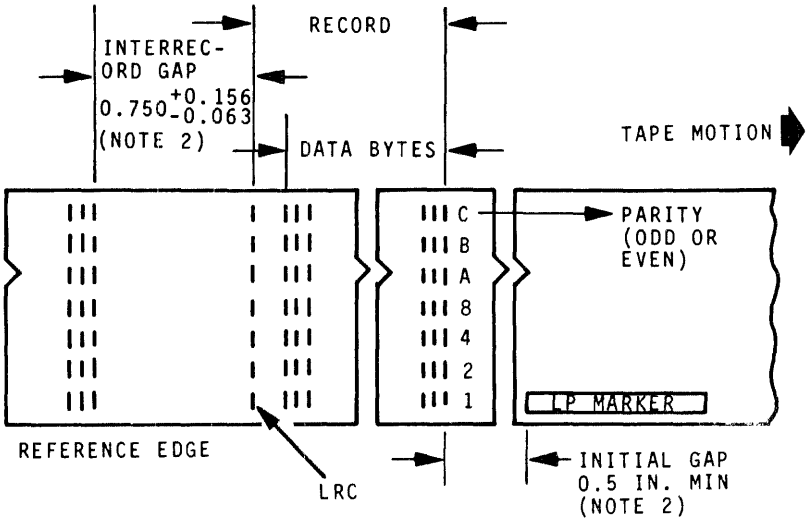


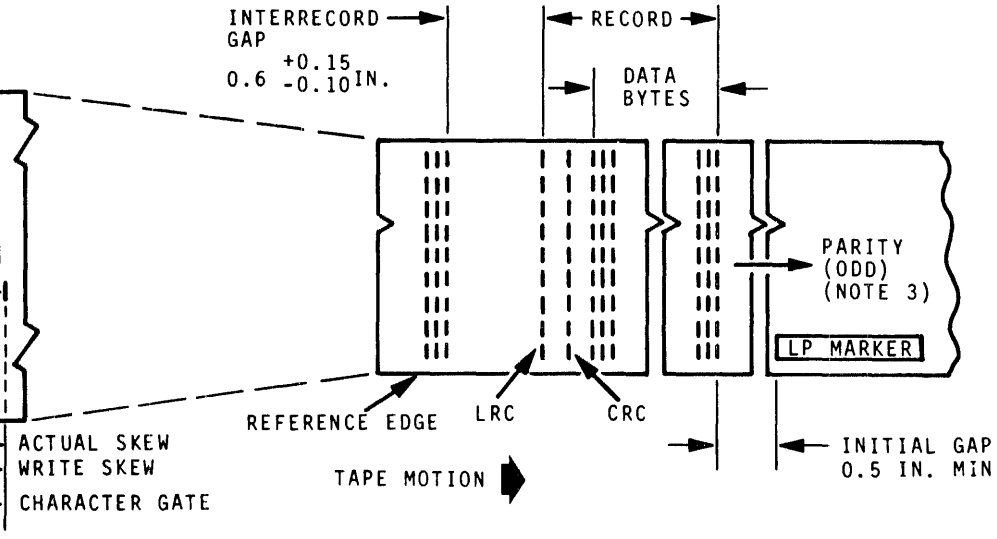
Figure 1-5. NRZ1 File Marks



NOTES:
1. TAPE IS SHOWN WITH OXIDE SIDE DOWN. NRZ1 RECORDING. BIT PRODUCED BY REVERSAL OF FLUX POLARITY.
2. TAPE TO BE FULLY SATURATED IN THE ERASED DIRECTION IN THE INITIAL GAP AND THE INTERRECORD GAP. ERASURE SUCH THAT A NORTH SEEKING END OF COMPASS WILL POINT TO START OF TAPE.
3. LRC (LONGITUDINAL REDUNDANCY CHECK CHARACTER) ODD OR EVEN-SPACED FOUR BITS FROM DATA CHARACTER.
4. PARITY BIT (A VERTICAL PARITY BIT IS WRITTEN FOR EACH BYTE).

110-0017

Figure 1-6. Data Format - Seven Track



NOTE:
1. CRC (CYCLIC REDUNDANCY CHECK CHARACTER). PARITY OF CRC CHARACTER IS DETERMINED BY THE NUMBER OF DATA CHARACTERS IN RECORD. ODD NUMBER OF DATA CHARACTERS-EVEN CRC CHARACTER, ETC. CRC USED ONLY IN IBM SYSTEM SYSTEM/360 800BPI. CRC CHARACTER SPACED FOUR BITS FROM DATA CHARACTERS.
2. LRC (LONGITUDINAL REDUNDANCY CHARACTER) ALWAYS ODD PARITY. SPACED FOUR BITS FROM CRC.
3. PARITY BIT (A VERTICAL PARITY BIT IS WRITTEN FOR EACH CHARACTER CONTAINING AN EVEN NUMBER OF BITS).

110-0018

Figure 1-7. Data Format - Nine Track

1.4.3.2 Longitudinal Parity

A longitudinal redundancy check character is written at the end of each block. It is separated from the end of each block as shown in Figure 1-8. This character is made up on a per-track basis. The number of 1's recorded in a given track of a block is counted and a "1" is written in the track as the LRCC if the count was odd, and, therefore, the number of 1's recorded in each track becomes even for any given block. On readback this is checked and an error is detected if the count is odd in any track. The possibility of not detecting an erroneous block still exists if an even number of bits in a given track of a block is dropped. However, when this test is combined with the vertical parity test the probability of not detecting an error is reduced.

1.4.3.3 Cyclic Redundancy Check Character (CRCC)

In the nine-track system another check character must be written. This character is derived with relatively complex logic, the result of which, in combination with the LRCC and vertical parity information, enables a computer to determine in which track a dropout occurred. If the dropout occurred in only one track in the given block, the computer can then nullify that track and generate the information in that track from the data in the remaining tracks, which includes the parity track.

This check character follows the last data byte by four cell positions, as shown in Figure 1-8.

1.4.3.4 Codes

The recorder will accept and read back any code set applied (six-bit for seven-track, eight-bit for nine-track). The only restriction is that the 000000 character in a seven-track system using even parity must not be used. This is a blank position or missing character, and most IBM systems will register an error condition if it is found in a block.

Two code sets are shown in Figure 1-9. These are the graphic symbols portion of the codes used by IBM for nine-track and seven-track systems. They are shown for reference only. Systems may use different code structures when they are programmed for them.

In the seven-track system the 000000 character may be converted to the 001010 character by use of the "BCD 0 to 10" option which is available for most Kennedy recorders. This senses the 000000 character on the data lines in conjunction with a write clock and converts it internally to record the IBM character for the number 0 (001010).

1.4.4 SUMMARY OF FORMAT

A summary of the above factors is shown in Figure 1-6 for seven-track data format and Figure 1-7 for nine-track data format Record blocks and tape markers are shown in Figure 1-10.

1.4.5 REFERENCES

Additional information may be found in the following publications:

a. IBM 2400-Series Magnetic Tape Units Original Equipment Manufacturers' Information, IBM Form 226862-4

b. USA Standard Recorded Magnetic Tape for Information Interchange (800 cpi, NRZ1), United States of America Standards Institute, 10 East 40th Street, New York 10016

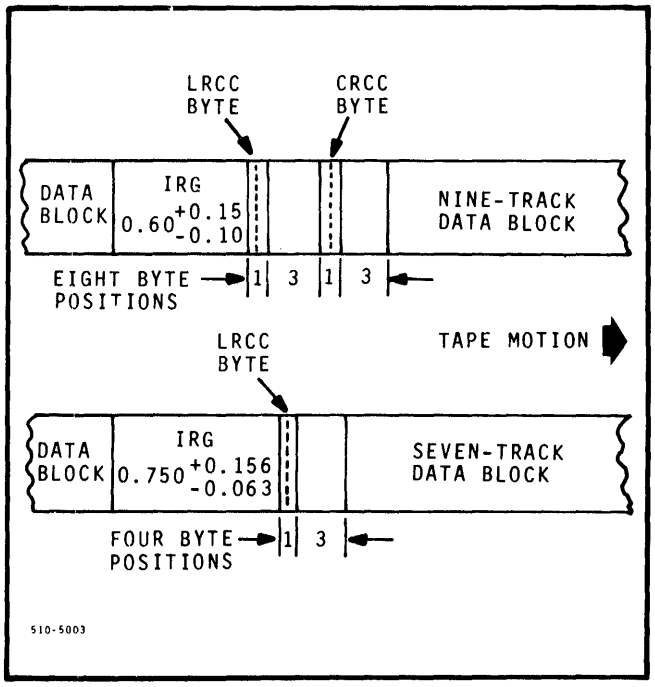
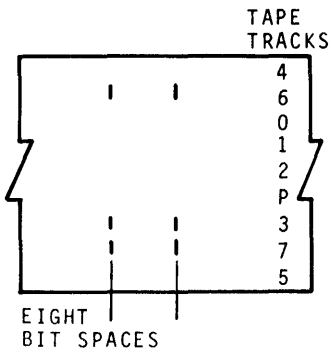


Figure 1-8. Check Characters

COLLATING SEQUENCE	GRAPHICS		EXTENDED BINARY CODED DECIMAL INTERCHANGE CODE (EBCDIC)								BINARY CODED DECIMAL INTERCHANGE CODE (BCD)					
	8 Bit	BCD	0	1	2	3	4	5	6	7	B	A	8	4	2	1
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	0
01	.	.	0	1	0	0	1	0	1	1	1	1	1	0	1	1
02	←	¤)	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	[	0	1	0	0	1	1	0	1	1	1	1	1	0	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	1
06	&	& +	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	$	$	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	]	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	0
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	1
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	% (	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↓	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	ъ	ъ	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	#	# =	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@ '	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	∇	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	1	1	1	1	1	1	1	0	0	1	1	1	1
25	δ	δ	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	0
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	1
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1
33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	ō	ō	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	1	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

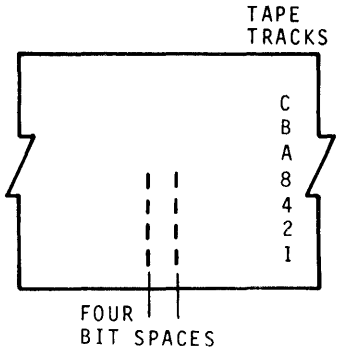
Figure 1-9. Typical IBM Codes

NINE-TRACK NRZ1 TAPE MARK



A NINE-TRACK NRZ1 TAPE MARK IS A SPECIAL CONTROL BLOCK THAT CONSISTS OF A CHARACTER WITH 1-BITS IN DATA TRACKS 3, 6, AND 7, AND AN IDENTICAL LRC CHARACTER EIGHT BIT SPACES FROM IT. NO CRC CHARACTER IS WRITTEN. ALTHOUGH THE TAPE MARK IS PRECEDED BY APPROXIMATELY 3.75 INCHES OF ERASED TAPE, THIS GAP IS NOT A REQUIREMENT.

SEVEN-TRACK NRZ1 TAPE MARK



A SEVEN-TRACK NRZ1 TAPE MARK IS A SPECIAL CONTROL BLOCK THAT CONSISTS OF A CHARACTER WITH 1-BITS IN A DATA TRACKS 8, 4, 2, AND 1, AND AN IDENTICAL LRC CHARACTER FOUR BIT SPACES FROM IT. ALTHOUGH THE TAPE MARK IS PRECEDED BY APPROXIMATELY 3.90 INCHES OF ERASED TAPE, THIS GAP IS NOT A REQUIREMENT.

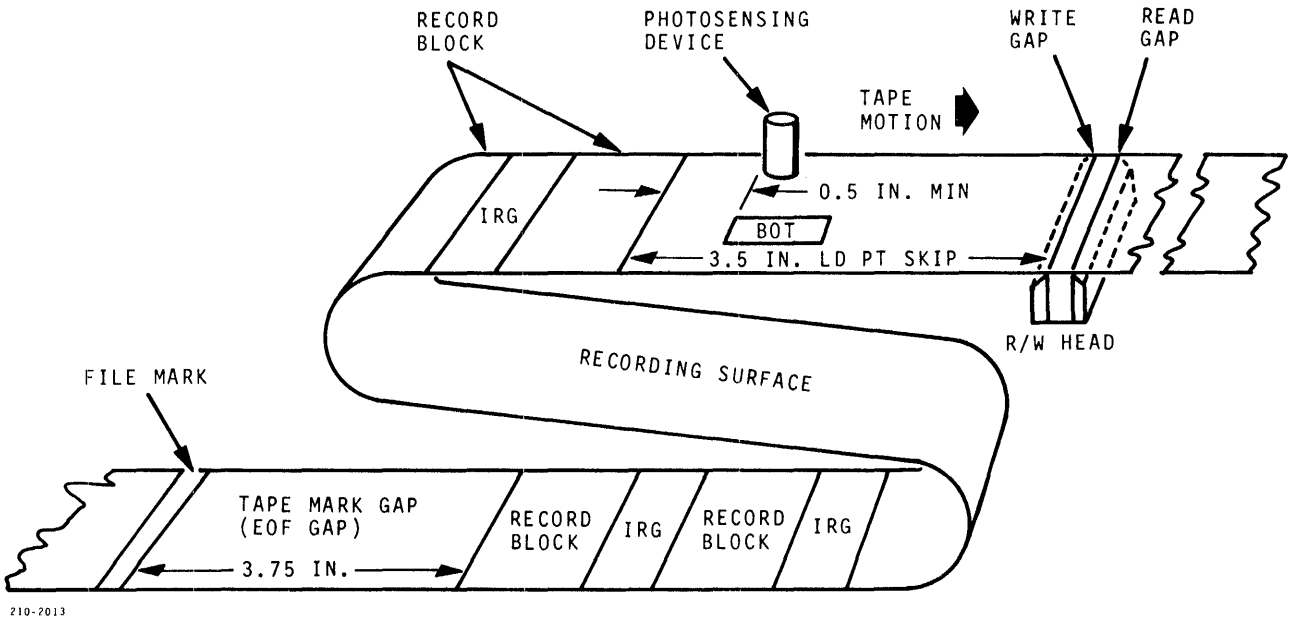


Figure 1-10. Record Blocks and Tape Marks

PHASE ENCODED RECORDING

Introduction

For many years, NRZ1 recording has been used in most computer tape systems. Density has increased from 200 cpi to 556 cpi and 800 cpi in the quest to increase data storage capability of tape and to achieve higher data rates.

With higher densities mechanical tolerances become more and more critical, however, and 800 cpi is probably the practical limit for NRZ1 recording. If higher densities were to be achieved, a new recording method was required.

Phase encoding was chosen. Its advantages were well known from use of similar systems on drums and specialized tape drives. In computer use, tape density of 1600 cpi was selected, and a tape format was established first by IBM and later adopted by ANSI as a proposed American national standard.

Figure 1 shows graphically the effect of density on tape storage capacity as a function of block length.

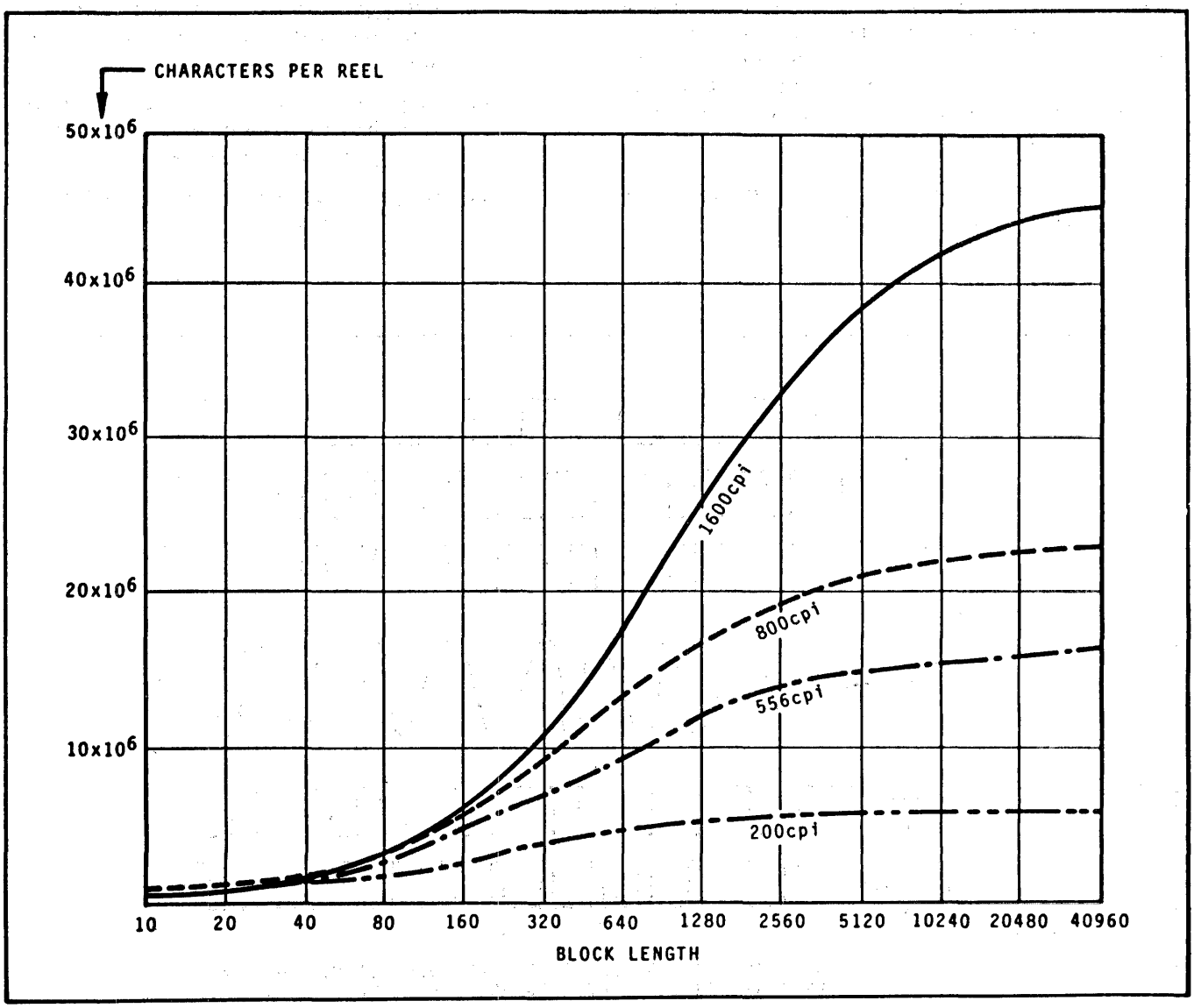


Figure 1. Comparison of Packing Density, Phase Encoded and NRZ1 Formats

Phase Encoded Recording

Each of the nine tracks on a PE tape is recorded in such a manner as to allow recovery of a track clock plus the data. This removes the requirement for close skew alignment as in NRZ1 recording, since clocked data can be assembled in a register to remove the effects of skew.

Saturation recording is used. Tape is dc erased with a polarity such that the rim end of the tape becomes a north seeking pole. A one bit is defined as a flux reversal to the reference polarity. A zero bit is defined as a flux reversal toward the opposite polarity. A "phase flux reversal" is written at the nominal midpoint between successive ones or successive zeros to establish proper polarity.

Figure 2 shows the resulting pattern of reversals on tape. It will be seen that the recording results in two bit densities being recorded, 1600 flux reversals per inch (frpi) and 3200 frpi. Phase shift of these two frequency components is of the utmost importance for decoding after playback.

Figure 3 is a logic diagram of a write amplifier that generates the required waveforms.

Tape Format

For IBM compatibility, tapes must be written in the proper format. This includes conventions on gap-lengths and special marks on tape. These have been chosen to ensure compatibility with nine-track 800 cpi NRZ1 on the same transport but with different electronics.

PE Format Requirement

a. Identification burst. A burst of recording in track 4 (P channel) only starting a minimum of 1.7 inches before the load point marker and extending past load point, but ending at least 0.5 inch before the first data block. Used to identify PE tapes.

b. Initial gap. A gap of at least 3 inches between the load point marker and the beginning of the first data block.

c. Preamble. A burst of 40 zero characters in each track followed by a character containing ones in each track.

d. Data. Nine tracks, channel assignments same as 800 cpi.

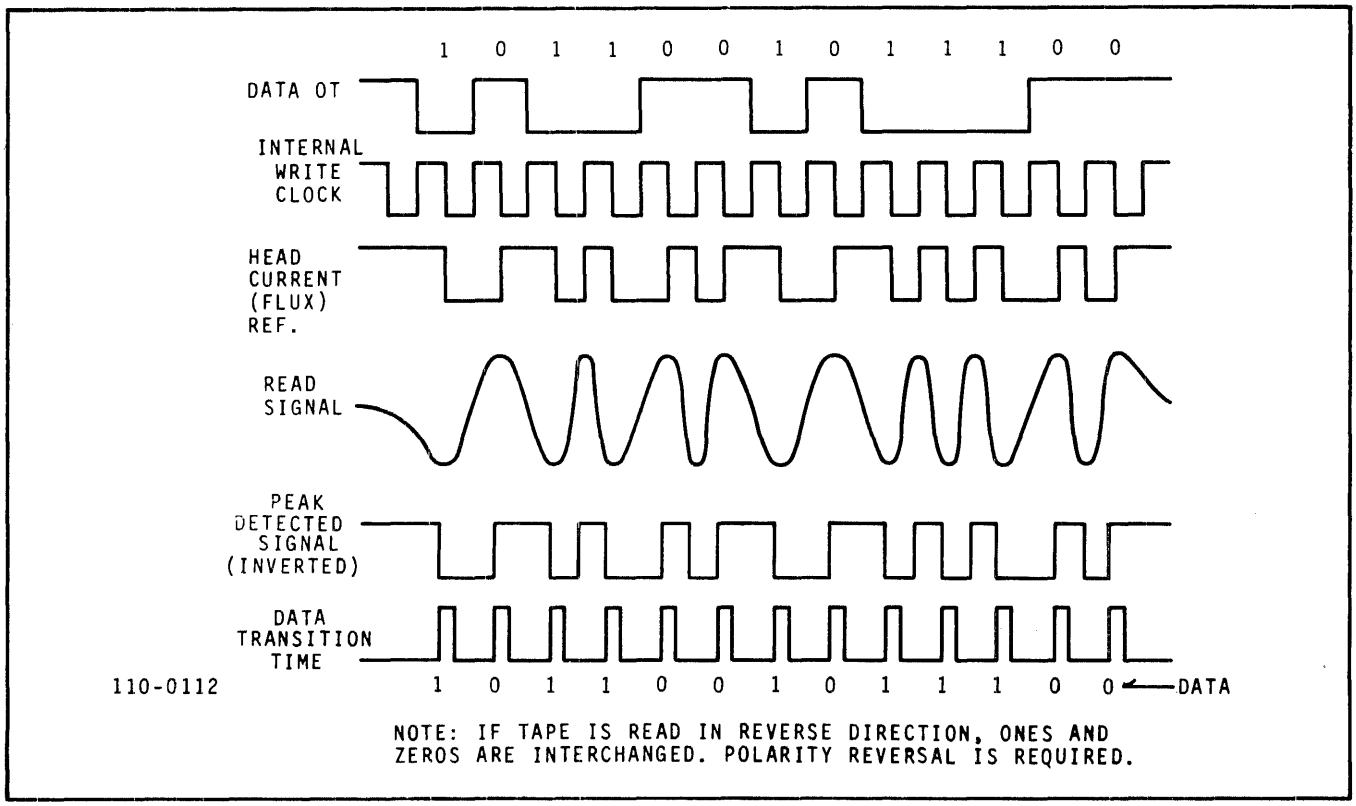


Figure 2. Phase Encoded Waveforms

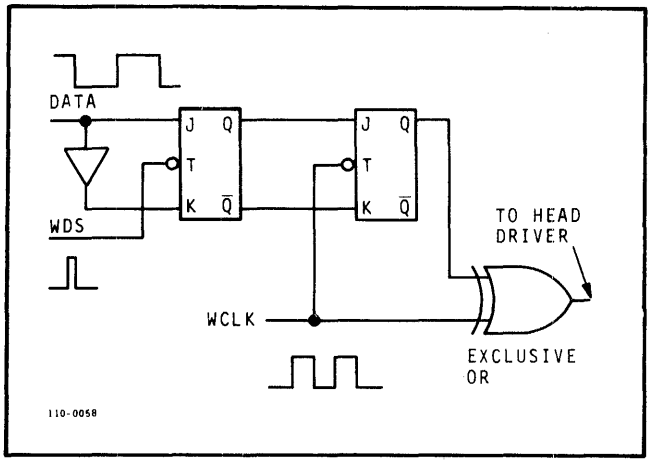


Figure 3. Write Amplifier Logic

e. Postamble. An all ones character followed by 40 all zero characters.

f. Interrecord gap. A gap 0.6 inch long nominal (0.5 inch minimum, 25 feet maximum) erased in the reference direction.

g. Tape marks. Tape marks are special control blocks used to identify portions of the tape. As opposed to NRZ1 format which has only one tape mark, there are eight possible marks in PE format. Tape mark blocks may be from 64 to 256 characters in length and are recorded in the format shown in Table 1.

Reflective Strips

Load point and end-of-tape reflective strips are attached to the tape in the same positions and with the same meaning as in NRZ1 recording.

Check Characters

All PE tapes are written with odd vertical parity. There are no LRC or CRC characters in the PE system. They are not needed since the location of the track in error can be easily detected through the coding system.

Reading Phase Encoded Tapes

Reading methods for PE tapes differ, naturally, from NRZ1 methods. Following is a general discussion of means employed to extract recorded information. More specific circuit descriptions will be found in instruction manuals for Kennedy Company PE units.

Amplified head signal waveforms are shown in Figure 4 for a typical data block. Preamble and postamble are easily identified at the beginning and end of the block. Purpose of the preamble is to allow synchronization with the signal by a phase-locked oscillator before data begins. It is written at 3200 frpi (all zeros).

Because of tape and head response limitations, the high frequency components are of lower amplitude than the low frequency components.

Differentiation of the amplified signal is performed in read electronics. Signal is then crossover detected, and digitized. A new signal envelope detector is used to detect "dropouts" in order to precisely determine defective parts of tape. Up to three characters may be lost at the beginning of the block and some noise can be seen at the end of the block (after the last zero) for up to two characters time.

Two conditions should be met before signals are recognized as valid data: (a) Signals must be present in all tracks; (b) a number of zeros (approximately 25) must be followed by an all ones character preamble detected).

Once detected, the preamble combination of all ones must be treated as a valid character. All zeros is not a valid character unless the single track dropout line is active.

One phase-locked oscillator and associated electronics is recommended for better tolerance to tape deck

TRACK	CHANNEL	1	2	3	4	5	6	7*	8
1	5	X	-	X	-	X	-	X	-
2	7	X	X	X	X	X	X	X	X
3	3	-	-	-	-	-	-	-	-
4	P	-	X	X	-	-	X	X	-
5	2	X	X	X	X	X	X	X	X
6	1	-	-	-	-	-	-	-	-
7	0	-	-	-	X	X	X	X	-
8	6	X	X	X	X	X	X	X	X
9	4	-	-	-	-	-	-	-	-

\- dc erased

x recorded at 3200 frpi

* most frequently used combination

110-0113

Table 1. Tape Mark Combinations

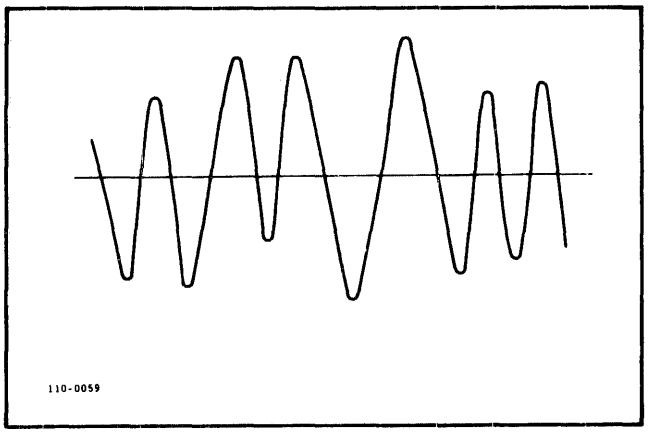


Figure 4. Read Signal

speed variation and write data timing. Two detectors, a one detector and a zero detector, are used to develop data. If, in the required time, neither detector has an output, a single track dropout is signaled and data correction ensues.

Each read channel has three output lines: one, zero, clock. These three lines are fed to a four-stage shift register controlled by an up-down counter. Upon entering the shift register, the 1 or 0 bit is shifted to the right to occupy the last open shift register cell. As data characters are read out, the shift register contents are shifted to the right. This allows up to four characters of skew. An error is posted if the skew register overflows.

Since single track dropouts are detected on a per bit basis and since the track in error is known, the character in the SR output stage can be corrected. This is done by reconstructing the missing bit by placing the remaining bits in a parity generator and adjusting the missing bit so that odd parity is achieved. If more than one track drops out, a multiple track error condition is flagged. In this case correction is not possible.

It can be seen from the preceding discussion that some complexity is required in the PE read electronics. If possible, it is desirable to share read electronics among several tape units as in Kennedy System 9000. If a customer wishes to build his own PE electronics, licenses are available to use Kennedy Company designs, thereby saving a considerable amount of engineering time.

SUMMARY OF SAFETY PRECAUTIONS

Power Connections:

CAUTION

Before connecting the unit to the power source, make certain the line voltage is correct (either 115 vac or 230 vac) and that the proper fuses have been installed. Proper fuse ratings are indicated on the rear of the unit.

Troubleshooting:

CAUTION

Turn power off before removing or installing PC boards.

RECOMMENDED TOOLS/TEST EQUIPMENT

In addition to normal electronic tools and test gear (an oscilloscope, voltohmmeter, etc.), the following items should be available for service and repair.

Vacuum test box, Kennedy PN 154-0041-001
Spanner wrench, Kennedy PN 154-0042-001
Set of nut drivers or open end wrenches, Phillips and standard screwdrivers
Capstan puller, Kennedy PN 154-0043-001
Skewmaster tape, Kennedy PN 154-0036-001
Card extender, Kennedy PN 190-2224-001
Maintenance kit, Kennedy PN 190-2324-001, containing:

- Head cleaner
- Hex socket keys - 7/64, 5/32, 1/8, 3/32
- Lint-free swabs
- Reflective marker strips
- Magnasee visualizing solution
- Loctite grade H

Optional maintenance tools:
Extension hose set, Kennedy PN 154-0044-001
Blower extension cord, Kennedy PN 154-0045-001

Warranty

The Company warrants its devices against faulty workmanship or the use of defective materials (except in those cases where the materials are supplied by OEM) for a period of one year from the date of shipment to OEM, with the exception of ¼" cartridge products which are warranted for a period of ninety (90) days.

The liability of the Company under this warranty is limited to replacing, repairing, or issuing credit (at the Company's discretion) for any devices which are returned by OEM during such period provided that (a) the Company is promptly notified in writing upon discovery of such defects by OEM; (b) the defective unit is returned to the Company, transportation charges prepaid by OEM; and (c) the Company's examination of such unit shall disclose to its satisfaction that such defects have not been caused by misuse, neglect, improper installation, repair alteration or accident.

Kennedy Company is continually striving to provide improved performance, value and reliability in its products and reserves the right to make these changes without being obligated to retrofit delivered equipment.

KENNEDY
Subsidiary Magnetics & Electronics Inc

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