Operation and Maintenance Manual

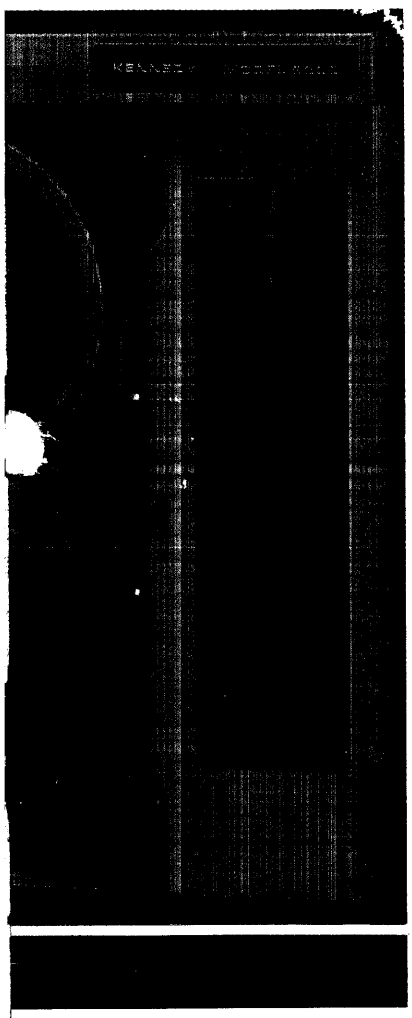
KENNEDY

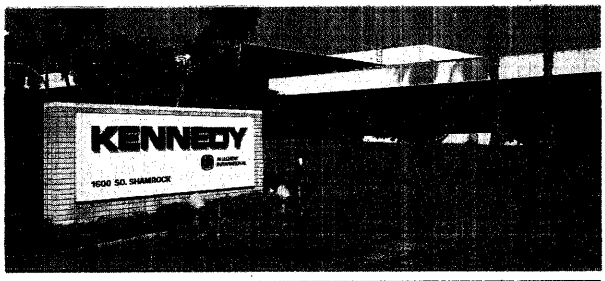
ALLEGHENY INTERNATIONAL

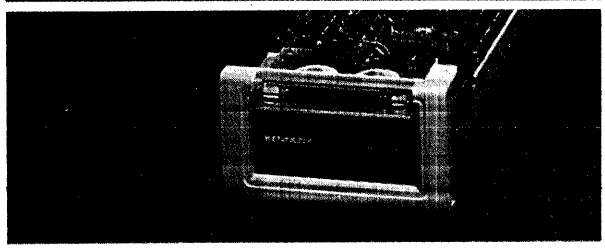
Preliminary

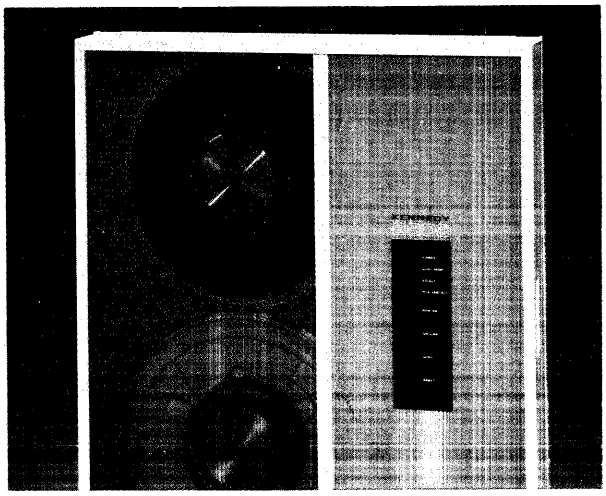
Model 9400

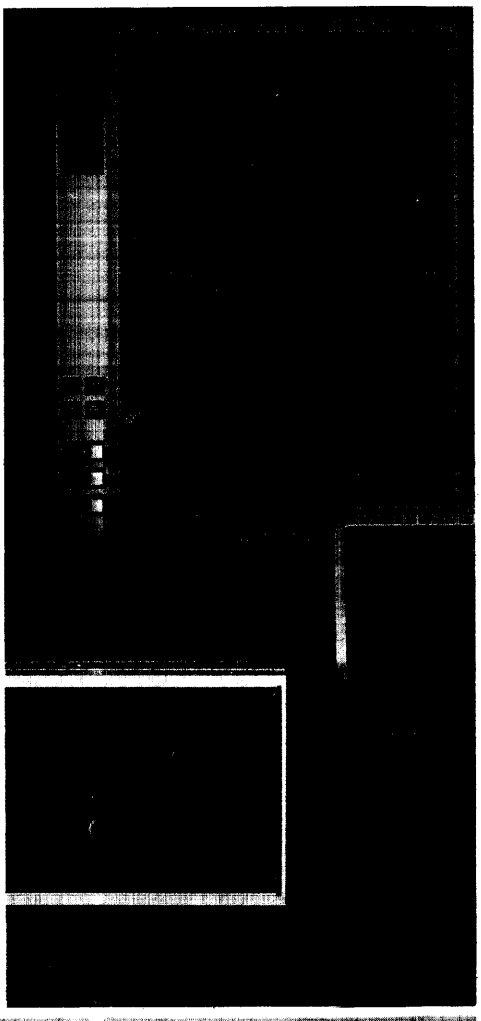
Tri-density Tape System

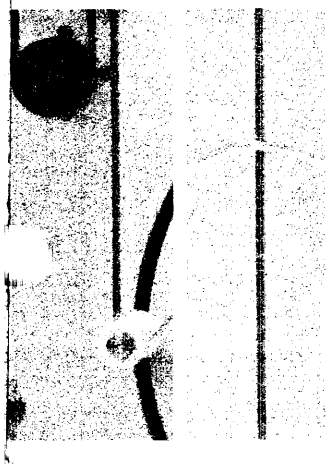


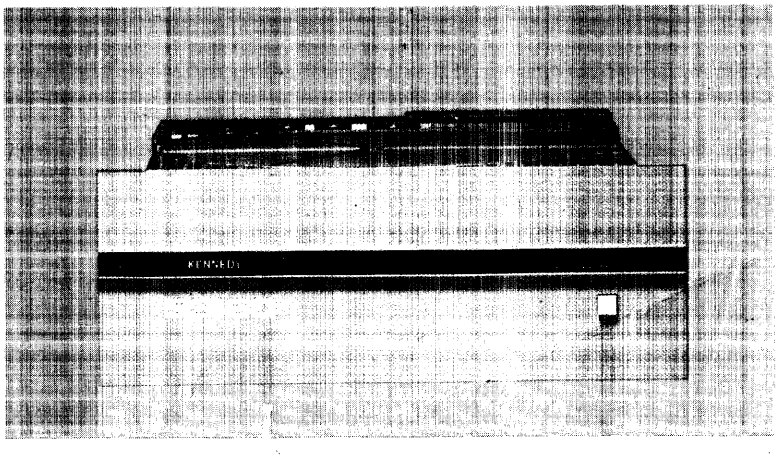


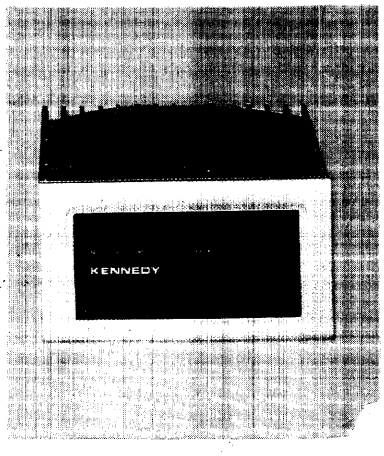












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SECTION I

APPLICATION OF DATA

1.1 INTRODUCTION

1.1.1 GENERAL

The Kennedy Model 9400 is a Tri-Density Tape System (TTS) designed to provide high speed, low cost mass storage, well suited for medium and high end micro/minicomputer systems.

The internal 'intelligence' of the system allows sophisticated error correction and system checks that heighten user confidence in system reliability.

1.1.2 TAPE FORMAT MODES

The following are the three modes of operation which make up the 9400 Tri-Density System:

1. GROUP CODED RECORDING (GCR): The 6250 BPI GCR (45 ips) MODE provides high density storage with very high data reliability. The nominal data rate transfer is 280-312 kilobytes per second, depending on the controller performance capability.

2. PHASE ENCODING (PE): The 1600 BPI PE (75 ips) MODE provides a medium density storage capability suitable for micro/minicomputer systems. The nominal data rate transfer is 120 kilobytes per second.

3. NONRETURN-TO-ZERO (NRZI): The 800 BPI NRZI (75 ips) MODE is provided for Industry Standard interchangeability. The nominal data rate is 60 kilobytes per second.

The 9400 TTS has a nine (9) track recording configuration, and is extremely cost efficient, providing the system integrator with the ability to store up to 180 MBytes of data in a GCR Format while maintaining compatability with PE and NRZI recorded tapes.

1.1.3 AVAILABLE HOST INTERFACE

The 9400 has the optional capabilities to use four different host interfaces with just a simple replacement of the Transfer Adapter board (TAB). The host can be changed to the type of interface needed to interface with outside controllers. The available standard host interfaces for the 9400 are as follows:

PICO

PERTEC

STC

TELEX

All interfaces generate full IBM and ANSI compatible tapes insuring full interchangeability on any other compatible device.

Note

This technical manual is written to accommodate the PERTEC TAB. Information pertaining to PICO, STC and Telex Interface boards can be obtained in future Model 9400 Operation and Maintenance manuals.

1.2 OPERATIONAL SPECIFICATIONS

1.2.1 GENERAL

Table 1-1 illustrates the complete electrical and mechanical specifications for the Model 9400 Tri-Density Tape System (TTS).

The 9400 utilizes convection cooling as one of the means of heat dissipation, and heat sinks are oriented for vertical transport mounting. Fans are provided for heat dissipation.

Note

Care must be taken when enclosing the unit to provide adequate air flow and assure that operating temperature limits (see Table 1-1) will not be exceeded.

1.2.2 MECHANICAL CONFIGURATION

Refer to Figure 1-1 for outline and installation view of the Model 9400 Tri-Density unit.

All assemblies are readily accessible from side or rear and may be removed by releasing jack screws and connectors (see Section II for Installation and Operation).

1.3 FRONT PANEL CONTROLS AND INDICATORS

Figure 1-2 illustrates the 9400 front panel controls and indicators, which include diagnostic controls and indicators, not seen when the front door is closed.

PERFORMANCE SPECIFICATION	
Data Density	800 BPI 1600 BPI 6250 BPI
Format	NRZI ANSI and IBM compatible PE GCR
Tape Speed	45 ips GCR 75 ips NRZI/PE
Rewind Time	500 ips max. 350 ips nominal 1 min 10 sec for 2400'(typical)
Gap Length	GCR 0.3" (RD AND WRT) Nominal NRZI/PE 0.6" (RD and WRT) Nominal
Access Time	GCR 2.7 ms @ 45ips Nominal NRZI/PE 3.7 ms @ 75 ips Nominal
Instantaneous Speed Variation	+/- 3%
Long Term Speed Variation	+/- 1% (GCR), +/-2% (PE,NRZ1)
Data Transfer Rate (Nominal) (GCR rates switch selectable)	GCR 312.5 KB/sec burst 281 KB/sec avg. 205 KB/sec 125 KB/sec PE 120 KB/sec NRZI 60 KB/sec
Density selection	Automatic (Read mode) Manual, from front panel or software selectable under host control.
TAPE	
Width Thickness Tension Reel size	0.498 (+/-.002) inch 1.5 mil's 8.0 +/- 2.0 ounces up to 10.5"
Tape capacity 1.5 mil tape	600,1200 or 2400 feet

TABLE 1-1
ELECTRICAL AND MECHANICAL SPECIFICATIONS

Magnetic Head Assembly	
Surface	Chrome or Triballoy
Number of Tracks	9 Track
Write to read gap	.15"
Erase head	Full Width
Wrap angle	7.5 +/- 5 degrees
Write skew	Less than 75 microinches
Read skew	Less than 75 microinches
Tape cleaner	Sapphire blade, vacuum-assisted
BOT/EOT detection	Infrared
Broken tape detection	Infrared
Motion control	Microprocessor controlled servo
Formatter	Integral, all densities
Tape buffer	Vacuum column
Interface	Pico, Pertec, STC, Telex
Diagnostic	Internal self-test front panel External RS-232 port (for remote testing) Signature analysis
Seismic operation	Supports seismic option
Acoustic noise	60 db(typical,operating,door closed)
MAINTENANCE STATISTICS	
MTBF (Design Goal)	6000 hours
MTTR (Design Goal)	30 minutes
ENVIRONMENTAL SPECS	
Temperature operating	2-45 degrees Celcius (excluding media).
Temperature non-operating	-2/-70 degrees Celcius
Humidity operating	15%-95% (non-condensing)
Humidity non-operating	5%-95% (non-condensing)
Altitude operating	0-4000' (high altitude options available to 12,000')
Altitude non-operating	0-50,000'

TABLE 1-1
ELECTRICAL AND MECHANICAL SPECIFICATIONS

PHYSICAL SPECS (See Figure 1-1)	
Dimensions	Height 24.5" Width 19" depth 22 3/4"
Mounting	Std. EIA Retma Rack, (slides)
Weight	170 lbs.
POWER SPECS	
Power Requirements 60 HZ voltage Input current nominal Power nominal 50 HZ voltage Input current nominal Power nominal	 115VAC 9 AMPS 1000W +/-10% 220/240VAC 4.5 AMPS 1000W
OPTIONS	
Special Paint FiFo Buffers See Table 1-1A for more information on 9400 options.	 4K (STD) 8K 12K 16K
Agency recognition	UL/CSA/FCC

TABLE 1-1
ELECTRICAL AND MECHANICAL SPECIFICATIONS

GENERAL OPTIONS	
Interface:	PICO PERTEC STC TELEX
Voltage:	115V 220V 240V
Frequency:	50 HZ 60 HZ
Parity:	Internal (STD) External
High Altitude Kit:	4000/8000 ft. 8000/12,000 ft.
Special Paint	(10 or more units)
FIFO Buffer:	4K (STD) 8K 12K 16K

NOTE

Larger than 4K FIFO's are needed if the lower GCR transfer rates are going to be used and the block size is greater than 4K. The following is a FIFO size vs record size chart to help determine the FIFO size needed:

LOW SPEED GCR (WRITE) 125 KB/SEC

	FIFO SIZE	PREFILL DELAY	MAX RECORD (IN BYTES)
1.	4096	30.7 ms	6,656
2.	8,192	63.0 ms	14,080
3.	12,288	80.0 ms	17,920
4.	16,384	126.0 ms	28,016

NOTE

Delay cancelled if 'LAST WORD' received.(See above PREFILL DELAY column) PREFILL includes ramp.

TABLE 1-1A
9400 OPTIONS

MEDIUM SPEED GCR (WRITE) 208 KB/SEC			
	FIFO SIZE	PREFILL DELAY	MAX RECORD (IN BYTES)
5.	4,096	18.4 ms	14,336
6.	8,192	38.0 ms	30,464
7.	12,228	51.0 ms	40,192
8.	16,338	72.0 ms	60,784

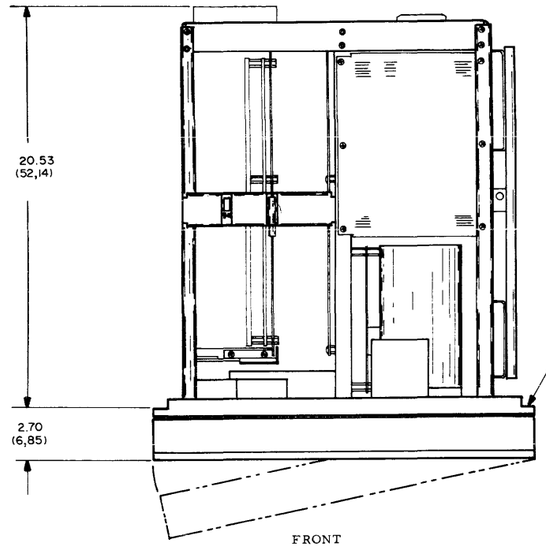
NOTE

Delay cancelled if 'LAST WORD' received.(See above PREFILL DELAY column) PREFILL includes ramp.

Software programs before version 1.9 will only support item 3.

TABLE 1-1A
9400 OPTIONS

TOP

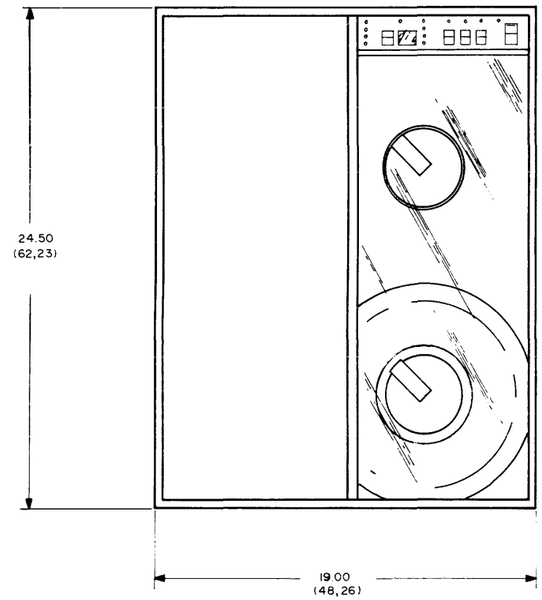


DUST COVER OPENS TO APPROX 120 DEGREES
FOR ACCESS TO TAPE REELS

DECK ASSEMBLY EXTENDS ON SLIDES
FOR ACCESS TO TRANSPORT & ELECTRONICS

FIRST DIMENSIONS ARE SHOWN IN INCHES
DIMENSIONS IN PARENTHESES ARE IN CENTIMETERS

FRONT



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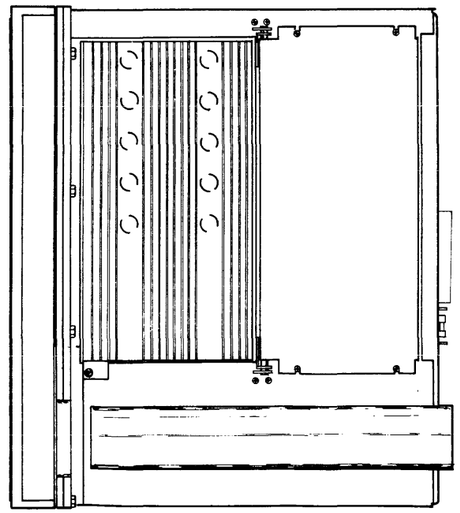


BACK

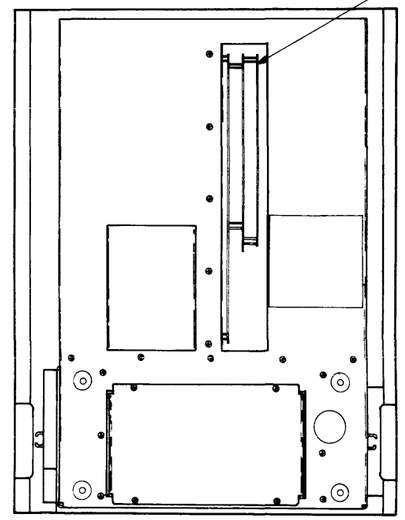
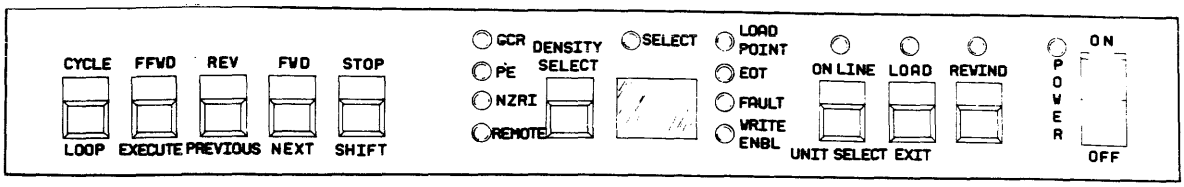


Figure 1-1

Outline and Illustration Drawing

410-4047



Note

Tape transport must be off line (on line indicator extinguished) and at load point before test panel can be functional.

ON LINE CONTROLS

The following controls are used to operate the unit on line with the host controller:

Note

Tape must be at BOT when selecting density.

GCR Indicator: Indicates Group Coded Recording (GCR) density mode has been selected.

PE Indicator: Indicates Phase Encoding (PE) density mode has been selected.

NRZI Indicator: Indicates nonreturn-to-zero (NRZI) density mode has been selected.

Remote Indicator: Indicates that the host may select the operating density.

Density Select: A toggle line switch, which selects density modes (GCR, PE, NRZI, and Remote).

Select Indicator: Illuminated when tape unit is ON LINE and selected.

Digital Read-Out Indicator: This will indicate the tape unit, number and a fault status code number for service information.

Note

By holding down the stop button, and depressing ON LINE SELECT pushbutton, you can change the unit select number (1, 2, 3, 4...). This feature will not be available on initial wire wrap Pertec adapters.

Load Point Indicator: Illuminated when tape is at load point.

EOT Indicator: Illuminated when tape has reached or passed End of Tape.

Figure 1-2

Front Panel Controls and Indicators

Fault Indicator: Will illuminate when a problem exists within the 9400 circuitry.

Write Enable (ENBL) Indicator: Illuminated whenever a reel with a write enable ring is mounted on the supply hub.

On Line Unit Select: A momentary pushbutton, which functions as alternate action. When first activated, the tape unit is placed in an On Line condition, when the tape unit is On Line it can be remotely selected. When activated again it takes the tape unit Off Line. The indicator is illuminated in the On Line condition.

Note

LOAD, REWIND and all off line controls are disabled when the tape unit is On Line.

LOAD: The momentary pushbutton activates the reel servos, tensions tape and starts the load sequence. The load point indicator will illuminate when the reel servos are activated, tape is tensioned and at BOT.

REWIND: The momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and unit is off line. The indicator is illuminated during either a local or remote rewind operation.

POWER: The ON/OFF switch applies power to the tape transport.

OFF LINE CONTROLS

These controls are used in testing and adjusting the unit.

Cycle Control Pushbutton: An interlock pushbutton which runs tape in alternating forward and reverse modes. Helpful in making ramp or vacuum sensor adjustments. Depressing STOP terminates this operation.

Fast Forward (FFWD) Pushbutton: An interlock pushbutton switch that allows tape unit to run forward at fast speeds. Depressing STOP button terminates this operation.

Reverse Pushbutton: An interlock pushbutton switch that allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton will terminate this operation.

Forward (FWD) Pushbutton: An interlock pushbutton switch that allows the tape unit to proceed forward at normal speeds. Depressing STOP button will terminate this operation.

STOP Pushbutton: An interlock pushbutton that terminates all tape motion.

Figure 1-2 (con't.)

Front Panel Controls and Indicators

1.4 INTERFACE DESCRIPTION

The interface connectors on the 9400 are designed for flat ribbon cables. Each live pin has a ground pin. An 8251A Asynchronous Serial Interface provides a means of communication with an external pocket terminal, standard CRT terminal or modem for test box operations. The port is selected by the memory decoders. An MC1488 and MC1489 provide RS232 level translation. A jumper block allows the port to appear as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE).

1.5 PERTEC INTERFACE SIGNAL CHARACTERISTICS

The unit responds to zero true inputs and provides zero true outputs. When interfacing a controller to the Pertec Transfer Adapter board, two 50 lead flat cables (3M 3365-50 or equivalent) are required. Figure 1-3 illustrates the Pertec Interface Driver/Receiver configuration for the Model 9400. Figure 1-4A and 1-4B show the general read and write timing diagrams for the PERTEC Interface. Figures 1-4 through 1-10 provide the sequences of events that occur during writing and reading for the Tri-Density System.

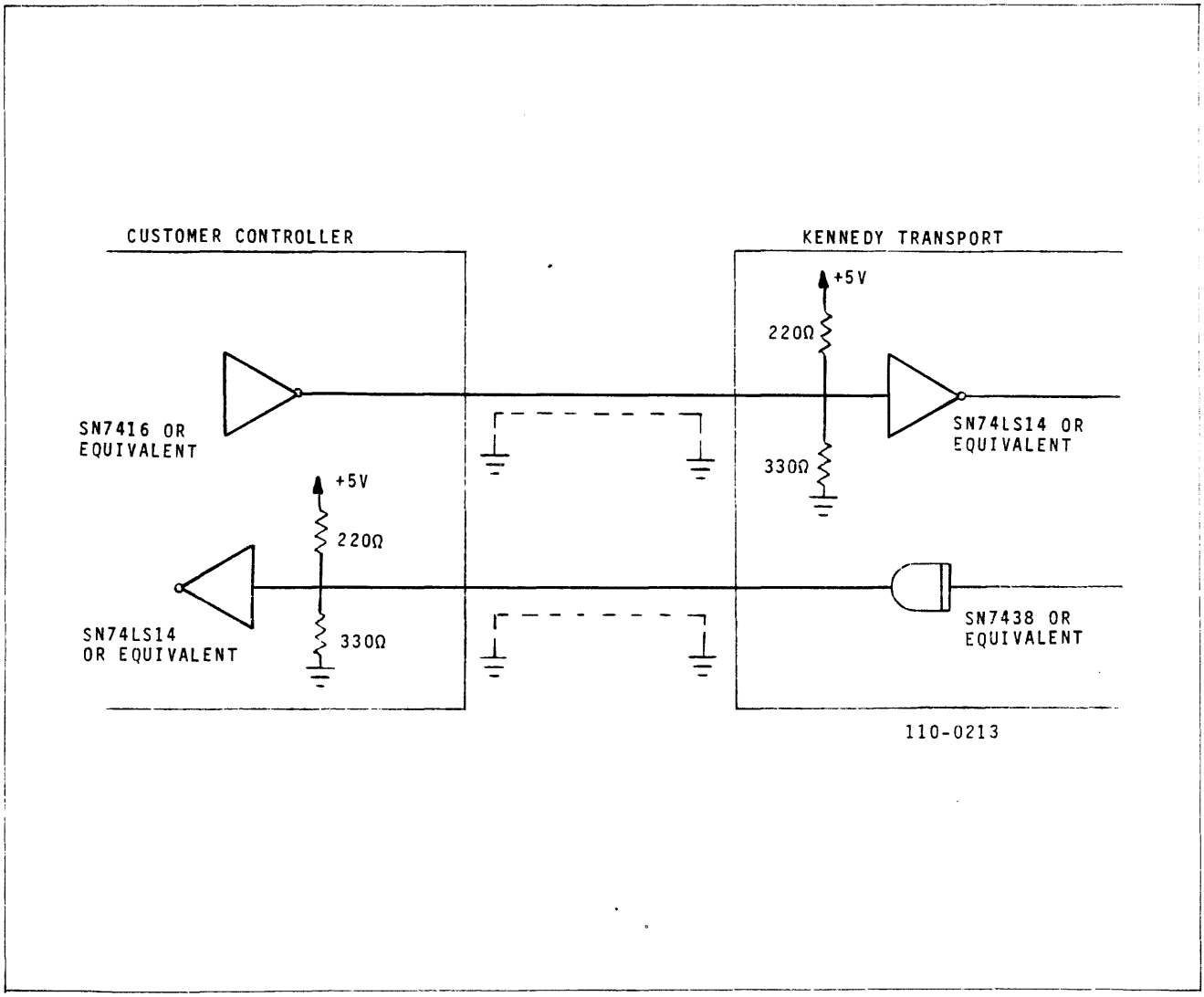
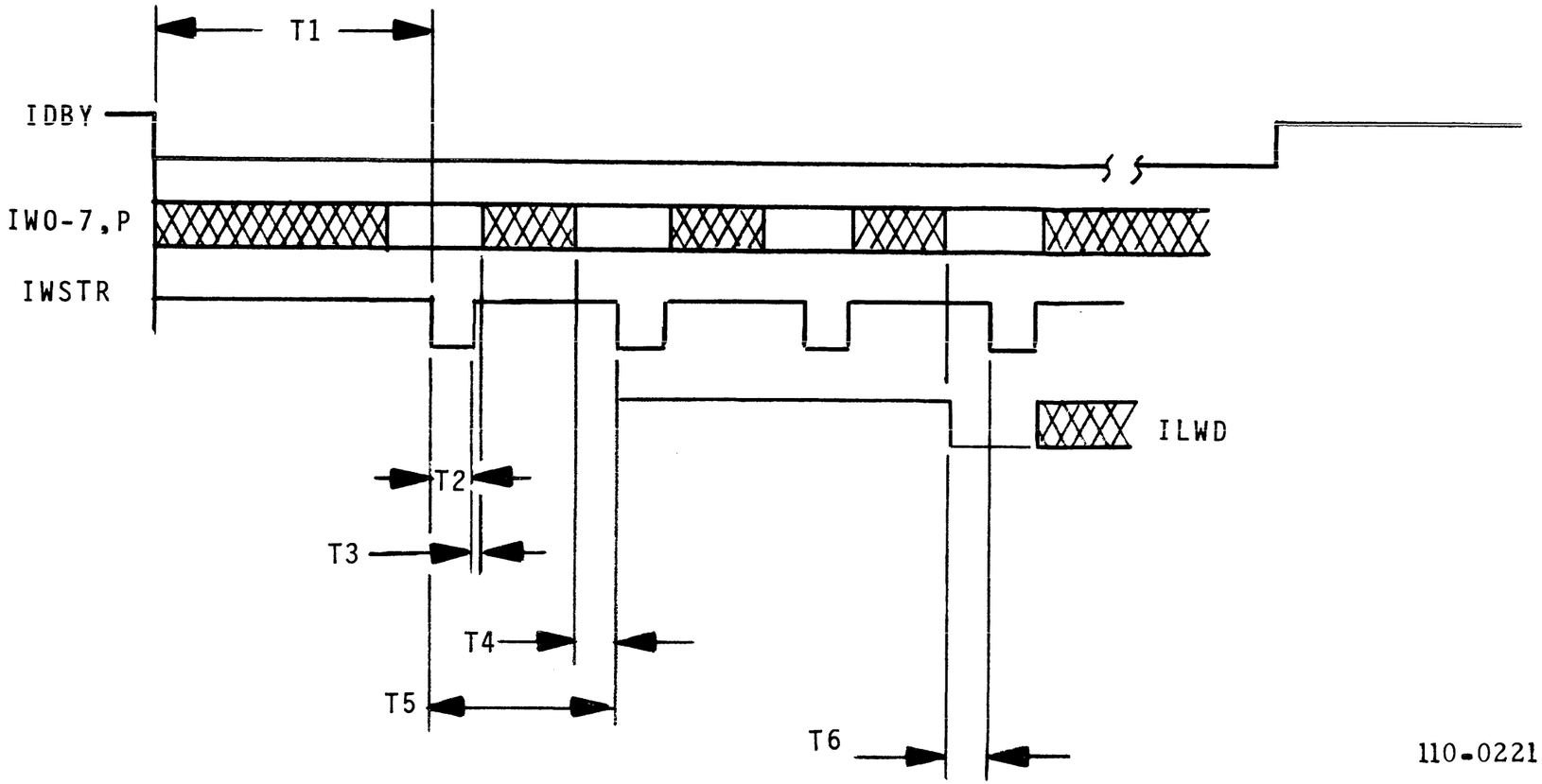


Figure 1-3

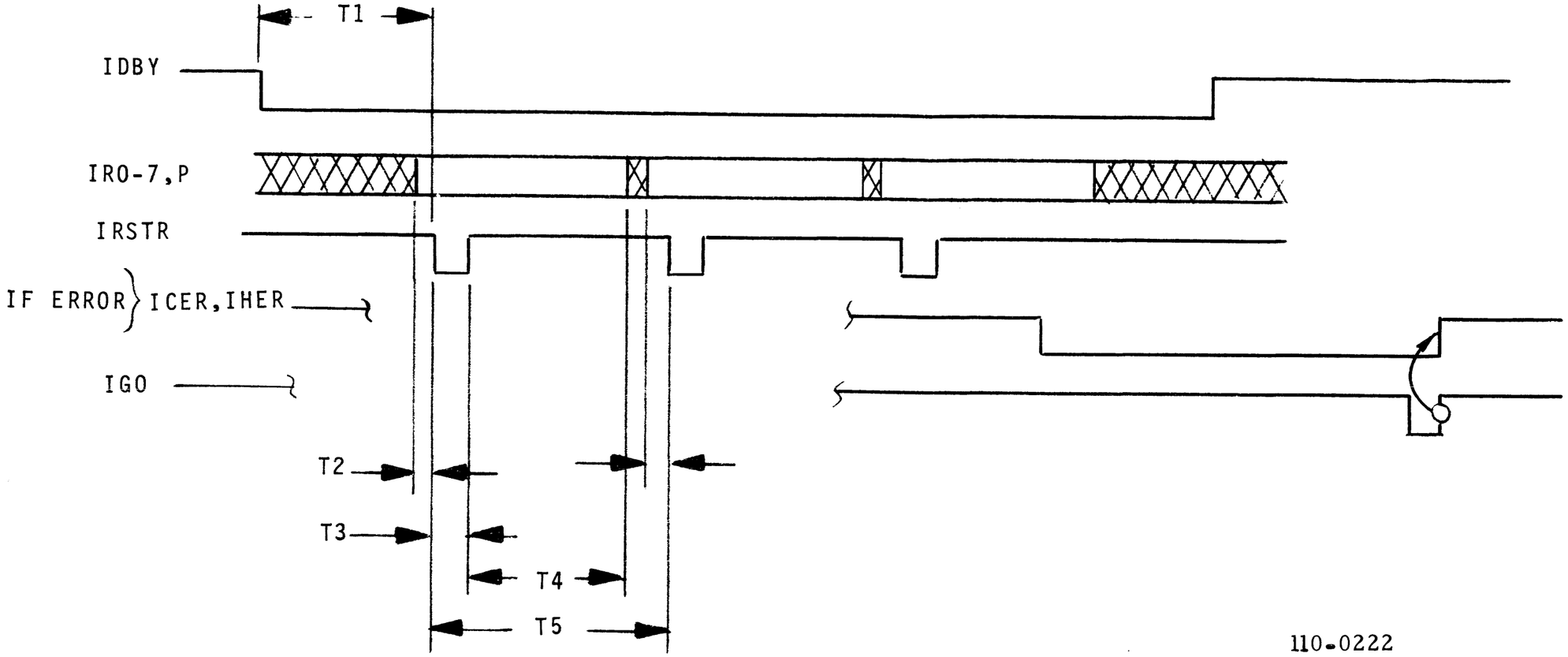
Driver/Receiver Interface Configuration



		NRZI	PE	GCR NORMAL	GCR LO SPEED
T1	DBY TO FIRST WRITE STROBE	≥25µs	≥25µs	≥25µs	≥25µs
T2	WIDTH OF IWSTR(25% OF CELL TIME)	4µs	2µs	800ns	2µs
T3	HOLD TIME FOR THE WRITE DATA LINES AFTER TRAILING EDGE OF WRITE STROBE (IWSTR).	≥0	≥0	≥0	≥0
T4	WRITE DATA SET UP TIME. DATA SHOULD BE SET UP WITHIN HALF A DATA BYTE PERIOD AFTER THE TRAILING EDGE OF EACH WRITE STROBE (IWSTR↑)	≥500ns	≥500ns	≥500ns	≥500ns
T5	PERIOD PER BYTE(@KILOBYTES/SEC)	16µs (62.5KB/s)	8µs (125KB/s)	3.2µs (312KB/s)	8µs (125KB/s)
T6	LAST WORD(ILWD) SET UP TIME. THIS SIGNAL SHOULD COINCIDE WITH THE LAST DATA BYTE.	≥500ns	≥500ns	≥500ns	≥500ns

Figure 1-4A
General Write Timing

106-9400-012D



110-0222

		NRZI	PE	GCR NORMAL	GCR LO SPEED
T1	DBY TO FIRST READ STROBE	>50µs	>320µs	>200µs	>320µs
T2	LEAD TIME OF READ DATA LINES TO LEADING EDGE OF IRSTR	≥500ns	≥500ns	≥500ns	≥500ns
T3	WIDTH OF READ STROBE(IRSTR)	≥1.0µs	≥1.0µs	≥1.0µs	≥1.0µs
T4	HOLD TIME OF READ DATA LINES AFTER TRAILING EDGE OF IRSTR	>2µs	>1µs	≥500ns	>5µs
T5	NOMINAL DATA BYTE PERIOD (KILOBYTES/SEC)	16.6µs (60KB/s)	8.33µs (120KB/s)	3.2→3.5µs (281KB/s) (Burst@312KB/s)	8µs (125KB/s)

Figure 1-4B
General Read Timing

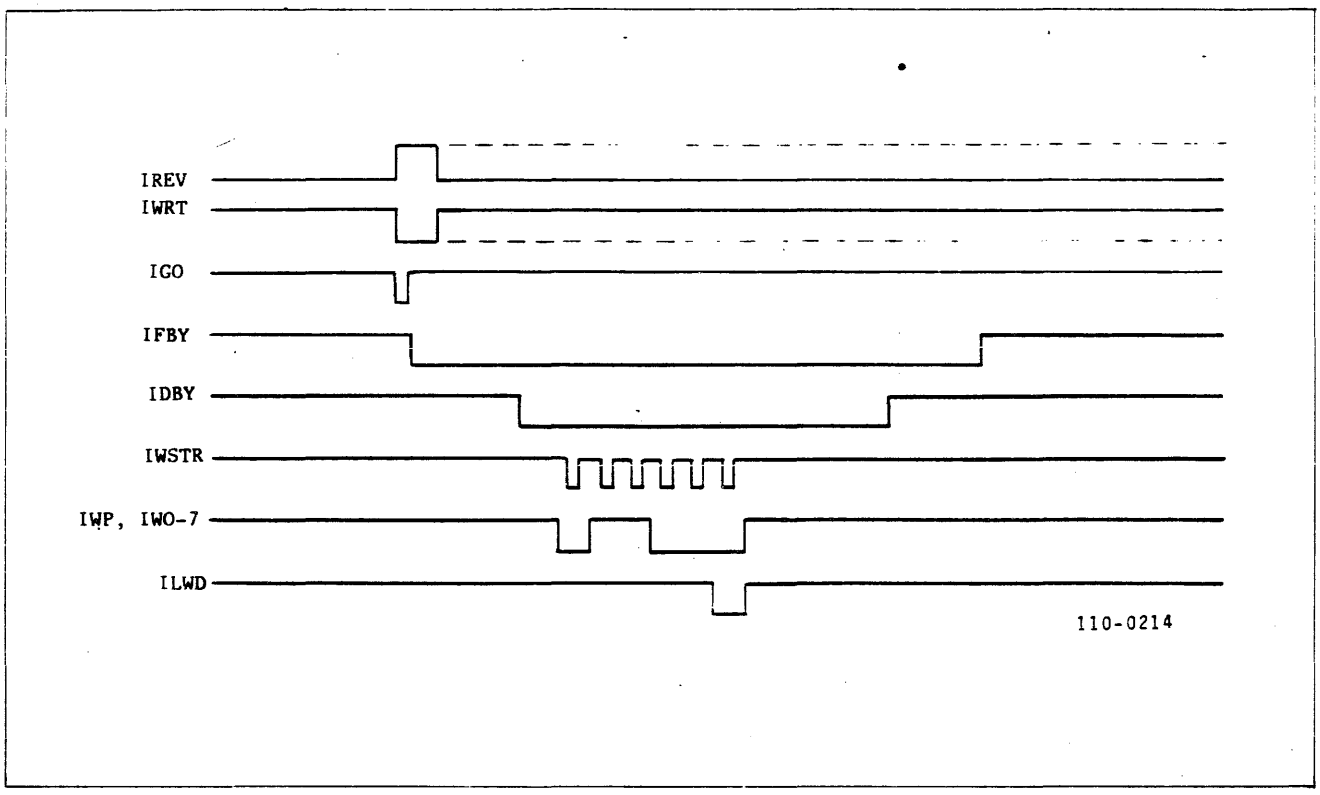


Figure 1-4

GCR Write Timing

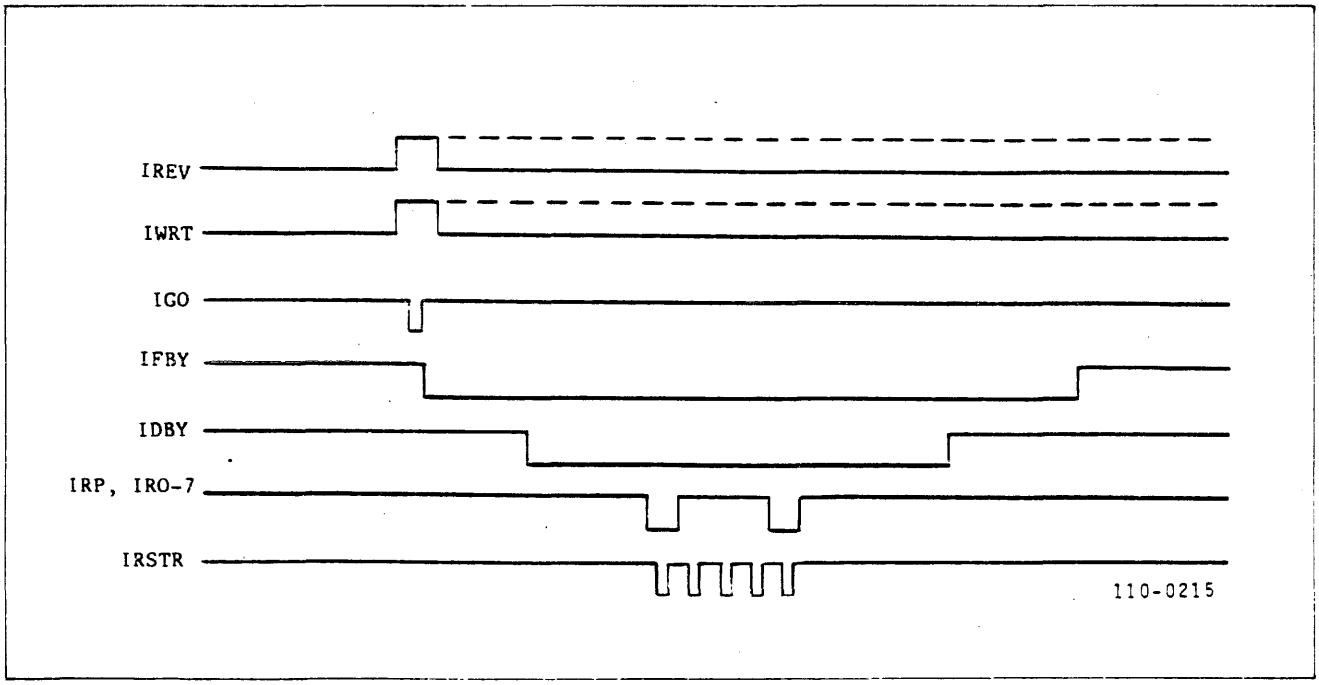


Figure 1-5

GCR Read Timing

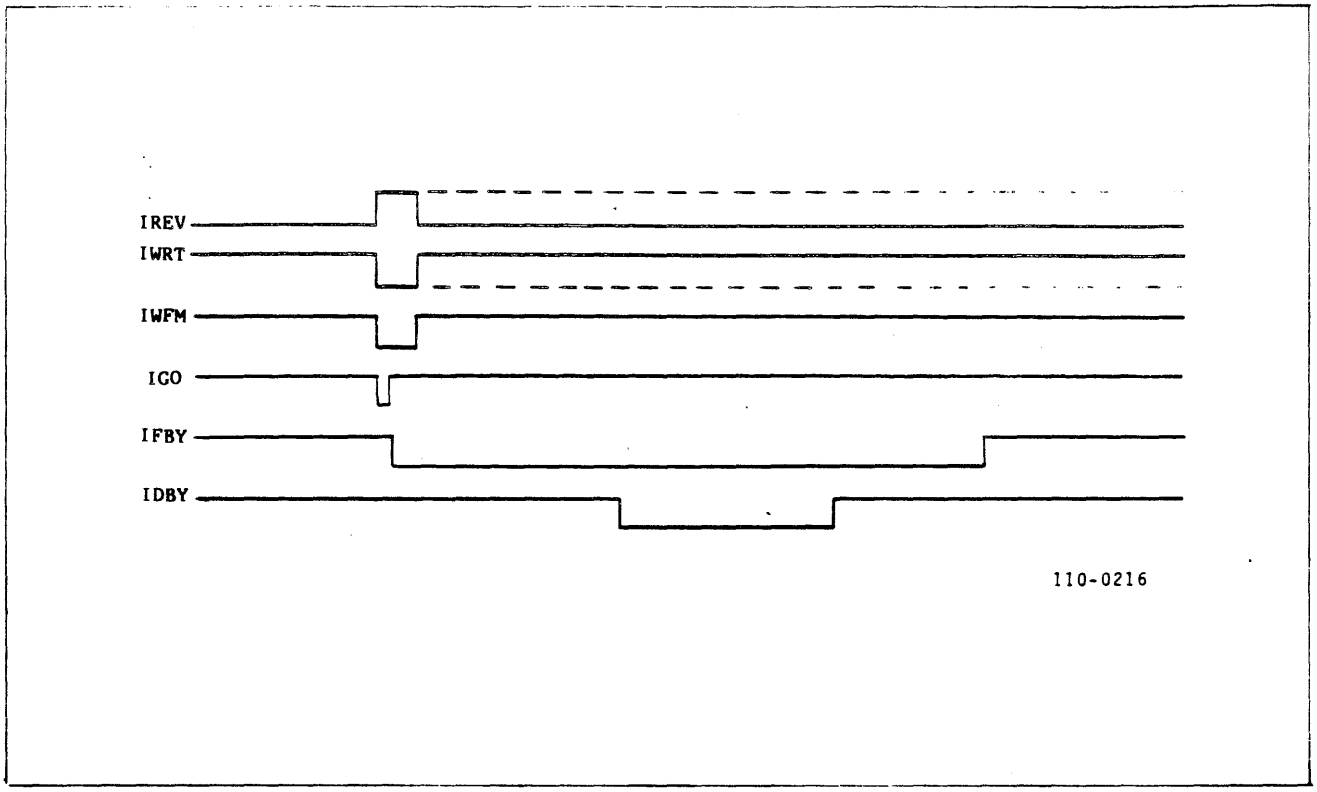


Figure 1-6
NRZI Write File Mark

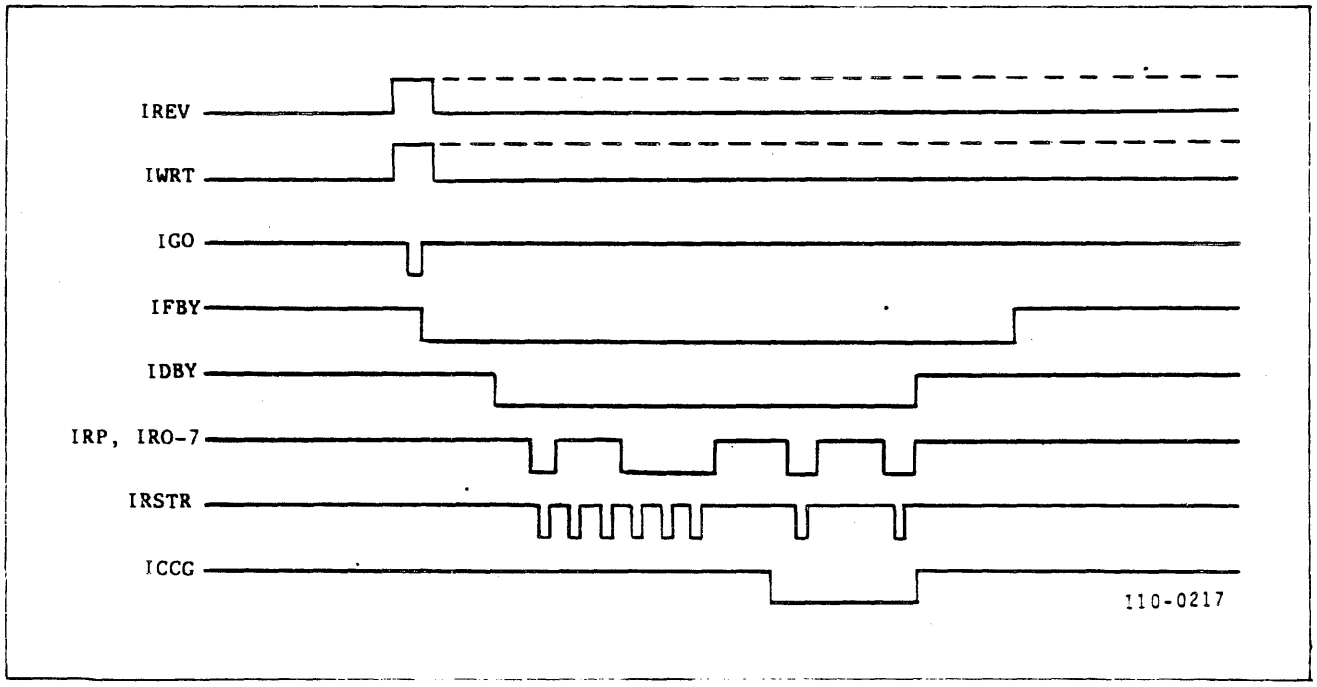


Figure 1-7
NRZI Read Timing

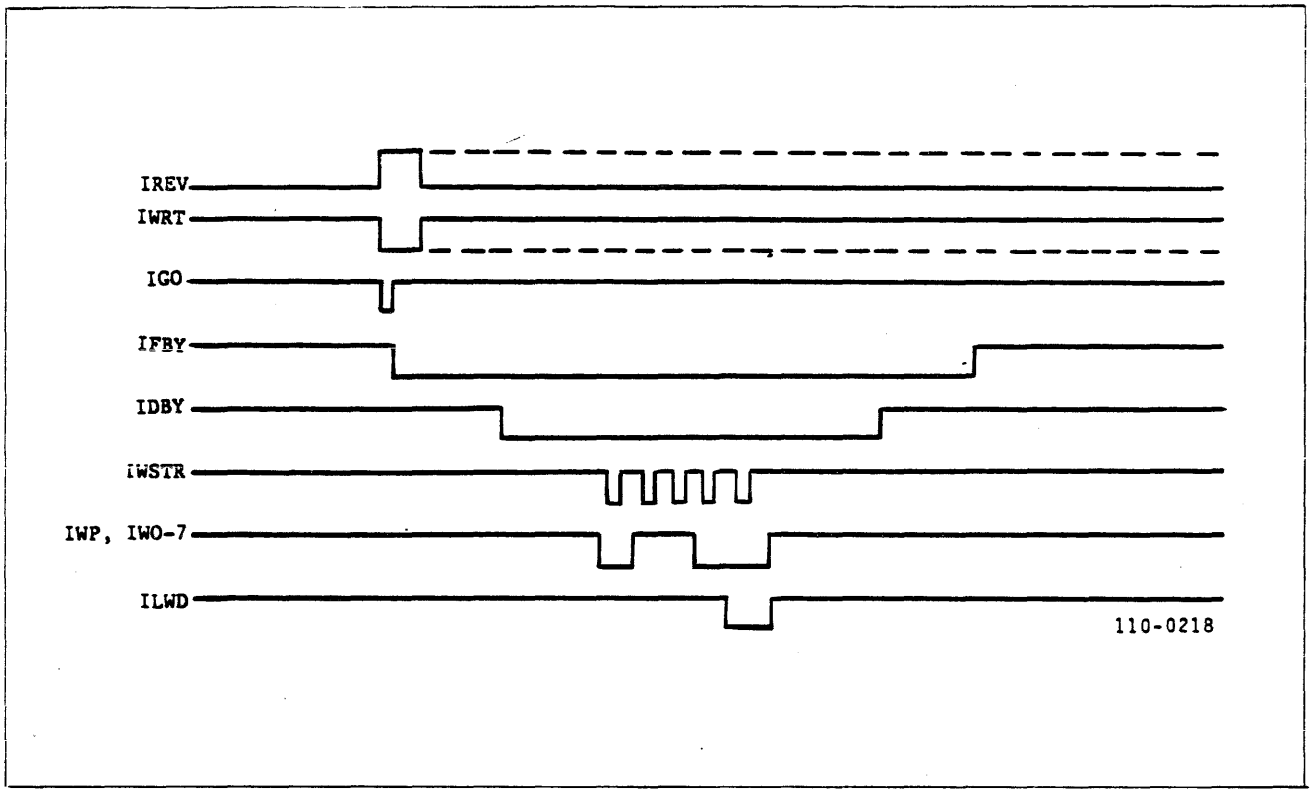


Figure 1-8
NRZI Write Timing

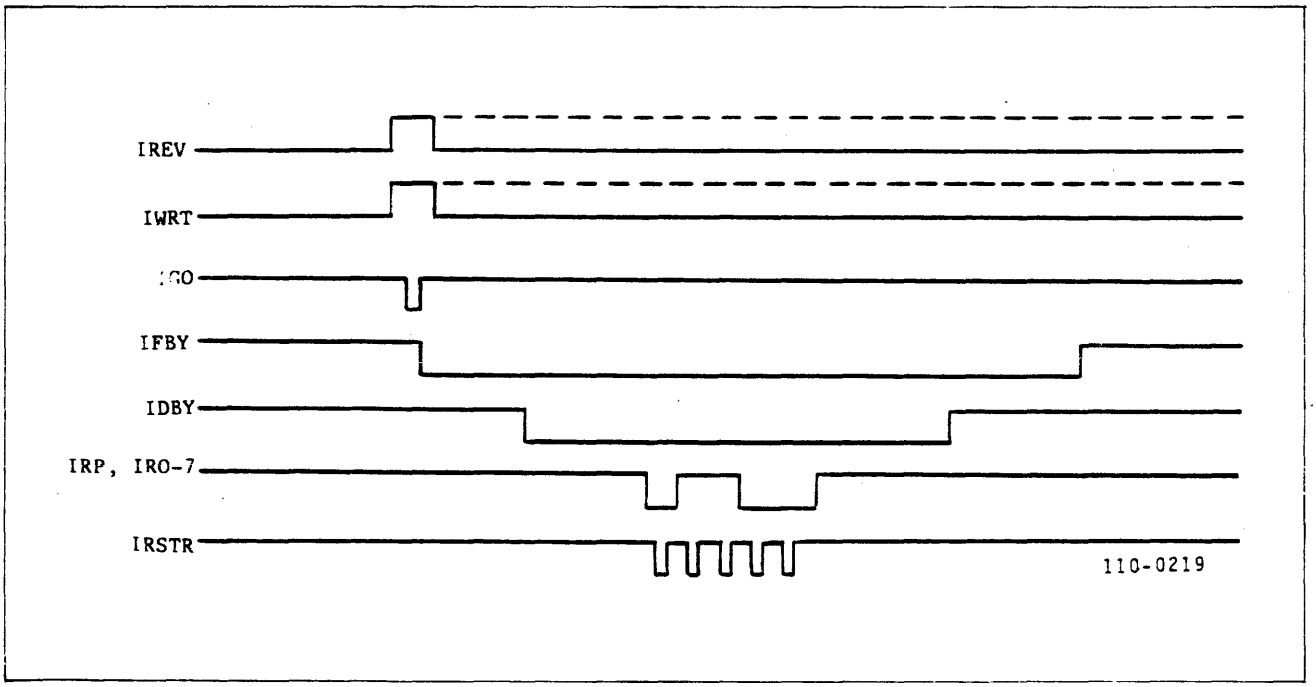


Figure 1-9
PE Read Timing

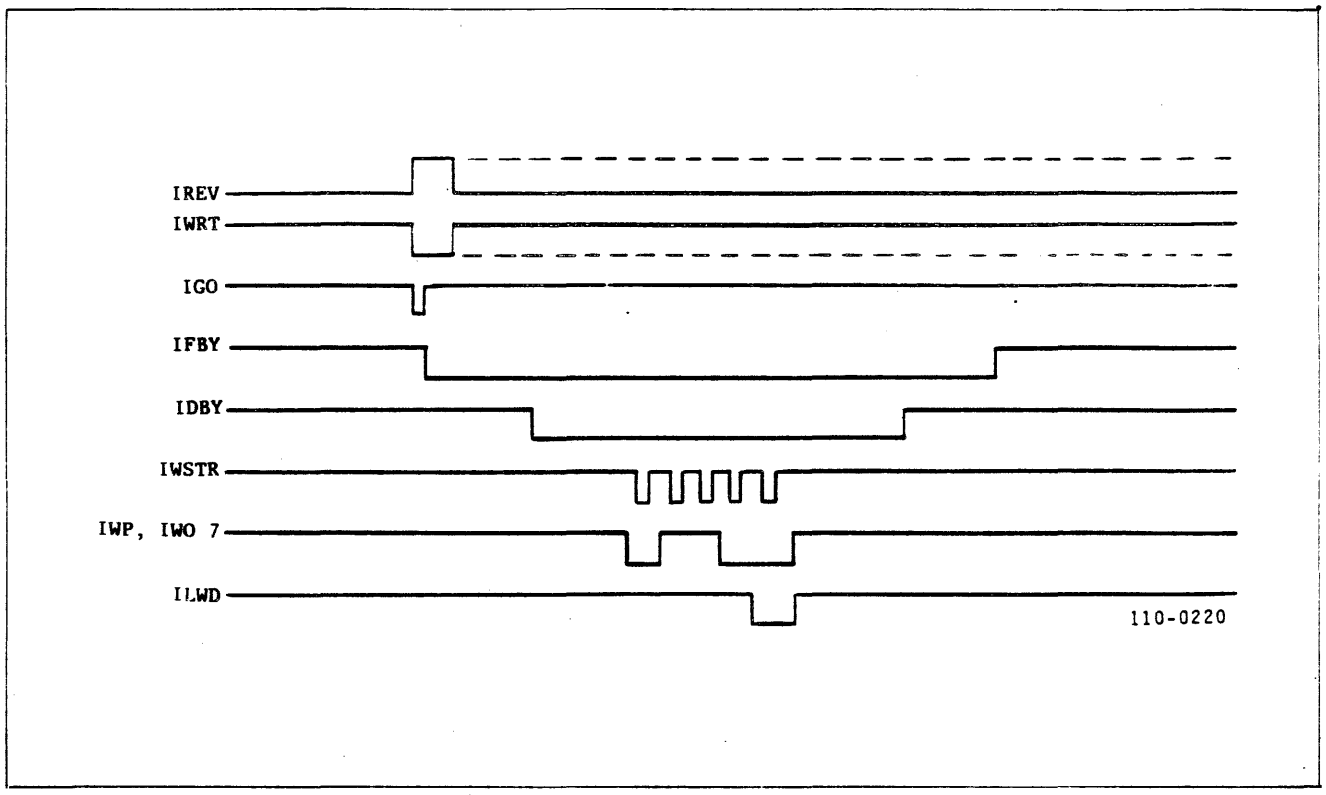


Figure 1-10

PE Write Timing

All interface designs should be based on the following criteria:

LEVELS:	TRUE = LOW = 0v (approx)	
	FALSE = HIGH = +3v	
PULSES:	Minimum pulsewidth is 1 usec	

The circuits are designed so that a disconnected wire or removal of power at the driver results in a false signal being interpreted at the receiver.

The two interface cables connect directly to J100 and J200 on the Pertec TAB as shown in Figure 1-11.

To connect the interface, the following must be considered:

1. When connecting the TAB host I/O interface cable, the length of the cable should be limited to 20 feet (6.1m).
2. Unless otherwise specified all host wires should be 28 AWG minimum, with a minimum insulation thickness of 0.01 inch.

Table 1-2 shows the Pertec Transfer Adapter board pin layout and signal nomenclatures.

1.6 INPUT SIGNALS

The input lines from the tape transport are terminated with a 220 ohm (5%) resistor to plus five volts, and a 330 ohm (5%) resistor to ground (see Figure 1-3). All input circuits have low level input voltage of 0.8v maximum and a high level input voltage of 2.0v minimum. The input receivers are all 74LS type circuits.

1.7 OUTPUT SIGNALS

All output lines must be terminated at the far end of the daisychained cable with a 220 ohm (5%) resistor to plus five volts and a 330 ohm (5%) resistor to ground. Output circuits are 7406 or 7438 TTL open collector drivers as shown in Figure 1-3.

1.8 TAPE MOTION

The tape transport capstan SERVO accelerates the tape to the required speed with a linear ramp. The tape is also decelerated to stop with a linear ramp. Start and Stop occurs within the interrecord gaps. The ramp UP/DOWN time for GCR is 2.7 ms and for PE/NRZI 4.5 ms.

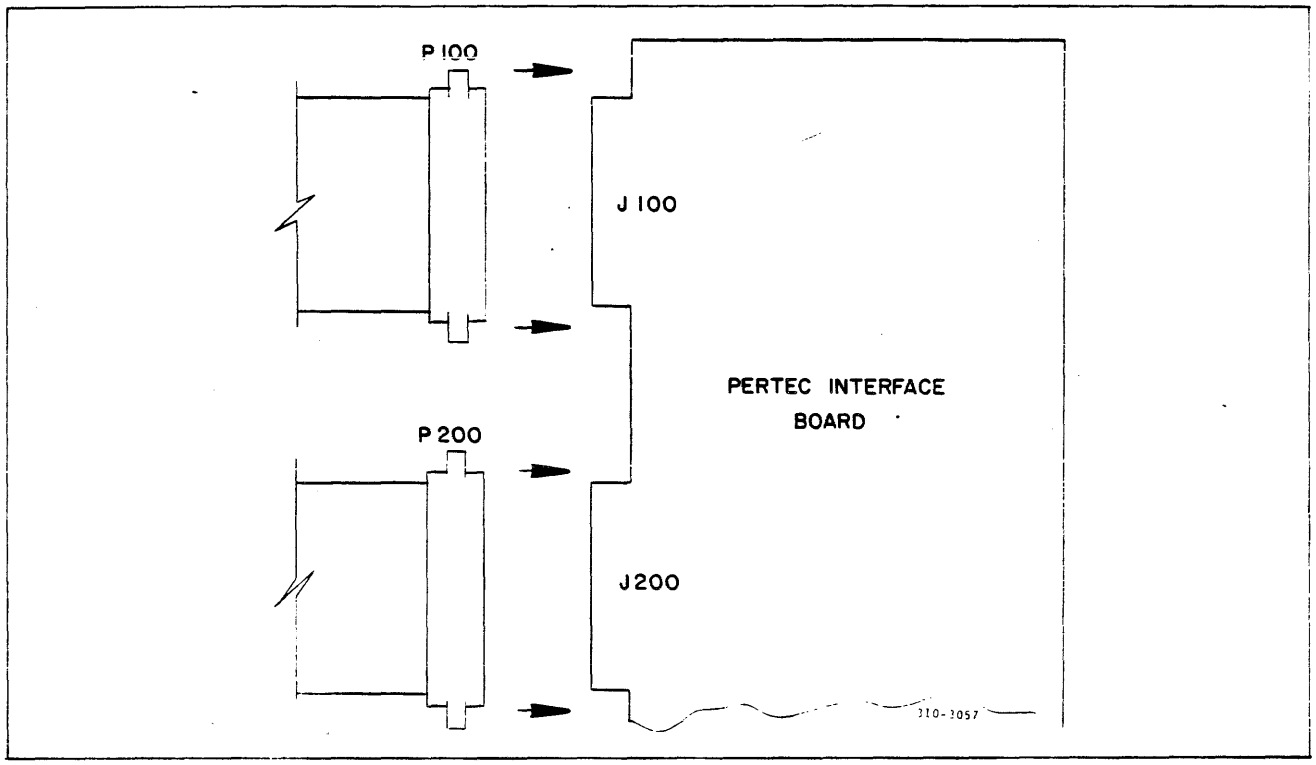


Figure 1-11

Interface Cable Connection

Interface I/O Connection P100/P200		Controller to Interface	
Live Pin	**Ground Pin**	**Signal Name**	**Mnemonic**
P100-			
2	1	FORMATTER BUSY	IFBY
4	3	LAST WORD	ILWD
6	5	WRITE DATA 4	IW4
8	7	INITIATE COMMAND	IGO
10	9	WRITE DATA Ø	IWØ
12	11	WRITE DATA 1	IW1
14	13	SPARE	
16	15	LOAD ON LINE	ILOL
18	17	REVERSE/FORWARD	IREV
20	19	REWIND	IREW
22	21	WRITE DATA PARITY	IWP
24	23	WRITE DATA 7	IW7
26	25	WRITE DATA 3	IW3
28	27	WRITE DATA 6	IW6
30	29	WRITE DATA 2	IW2
32	31	WRITE DATA 5	IW5
34	33	WRITE/READ	IWRT
36	35	NOT USED	
38	37	EDIT	IEDIT

Table 1-2

Pin/Signal Characteristics

Interface I/O Connection P100/P200		Controller to Interface	
Live Pin	**Ground Pin**	**Signal Name**	**Mnemonic**
40	39	ERASE	IERS
42	41	WRITE FILE MARK	IWFM
44	43	READ THRESHOLD 1	ITHR1
46	45	TRANSPORT ADDRESS	ITAD∅
48	47	READ DATA 2	IRD2
50	49	READ DATA 3	IRD3
P200-			
1	5	READ DATA PARITY	IRP
2	5	READ DATA ∅	IRD∅
*3	5	READ DATA 1	IRD1
4	5	BEGINNING OF TAPE	IBOT
6	5	READ DATA 4	IRD4
8	7	READ DATA 7	IRD7
10	9	READ DATA 6	IRD6
12	11	HARD ERROR	IHER
14	13	FILE MARK	IFMK
**16	15	CHECK CHARACTER GATE/IDENTIFICATION	ICCGID
18	17	FORMATTER ENABLE	IFEN
20	19	READ DATA 5	IRD5
22	21	END OF TAPE	IEOT
24	23	OFF LINE	IOFL
26	25	NRZI	INRZI
28	27	READY	IRDY
30	29	REWINDING	IRWD
32	31	FILE PROTECT	IPROT
34	33	READ STROBE	IRSTR
36	35	WRITE STROBE	IWSTR
38	37	DATA BUSY	IDBY
40	39	SPEED	ISPEED
42	41	CORRECT ERROR	ICER
44	43	ON LINE	IONL
46	45	TRANSPORT ADDRESS	ITAD1
48	47	FORMATTER ADDRESS	IFAD
50	49	DENSITY SELECT	IDEN

* All odd pin numbers are ground except pins 1 and 3.
** ICCG and IOCNT line (16) shared by NRZI and PE.
NOTE: REMOTE Tri-Density Selection is optional, in the present configuration only Dual Remote Density is available per controller capability. See dip-switch configuration flow diagram (Figure 1-12) for available remote options.

Table 1-2 (con't.)

Pin/Signal Characteristics

1.9 BASIC SIGNAL DEFINITIONS

The 9400 Tape Drive Unit is capable of executing the commands necessary to enable the modes of operation described in the following paragraphs.

Note

All commands except REWIND (IREW), and OFF LINE (IOFL) are executed by sampling the logic states of the REVERSE/FORWARD (IREV), WRITE/READ (IWRT), WRITE FILE MARK (IWFM), EDIT (IEDIT), and ERASE (IERASE) interface lines, as given in Table 1-3.

REWIND and OFF LINE commands are executed directly from the interface.

1.9.1 READ FORWARD

This command causes tape on the selected transport to be accelerated to the normal transport operating speed. The transport generates the delays necessary for proper positioning of transport read head in the interblock gap (IBG), this is after it reads the first record of data encountered and has decelerated the tape to a stop. The next block can be read by supplying a new read forward command to the transport prior to the completion of the tape deceleration which improves access time to the next block by as much as one ramp time.

1.9.2 READ REVERSE

This command is similar to a read forward command except that tape motion is in the reverse direction. During the reverse operation, the unit always resets to the quiescent state when the BOT signal is present. In this operation the head can be repositioned further back in the gap after reading a record. The change in position of the head is to facilitate the editing of a record, and is done by the transport in response to an EDIT command. See paragraph 1.9.4 for EDIT command.

1.9.3 WRITE

In this operation the unit accelerates tape, and after the appropriate prerecord delay time, begins to transfer data from the controller to the transport. This process continues until a LAST WORD (ILWD) is received from the controller.

The tape will continue to move forward until the record has been read by the read head, then the tape will be decelerated to a stop with the write head properly located in the center of IBG.

1.9.4 EDIT

In this operation the write current is switched OFF slowly at the end of an edit sequence, to minimize the possibility of recording a glitch on tape.

1.9.5 WRITE FILE MARK

The write file mark command causes a file mark to be written on tape.

1.9.5.1 PE File Mark

When a write file mark is executed, the transport unit generates a file mark consisting of 256 flux reversals at 3200 frpi in channels P, 0, 2, 5, 6 and 7. Channels 1, 3, and 4 are dc-erased.

Note

When reading, the unit will recognize a file mark if there are at least 64 flux reversals in channels 2, 6, and 7 with channels 1, 3, and 4 dc-erased. Channels P, 0, and 5 are ignored for this test.

1.9.5.2 NRZI File Mark

A NRZI write file mark command is generated by a unique one-character record. This single data character consists of a 1 bit in channels 3, 6, and 7 and a 0 bit in all other channels. The CRCC contains all 0s. The LRCC is equivalent to the single data character.

The 9400 tape unit tests for the presence of the file mark pattern during every read operation. When this is detected, the file mark (IFMK) interface line, P200-14, is pulsed and the file mark character is transmitted to the controller. ICCG asserts and the LRCC is transmitted.

1.9.5.3 GCR File Mark

Note

The flux reversal rate of 9042 frpi (356 frmm) is equal to the number of bit cells per inch. This accommodates data, encoding, error checking, and other overhead requirements. The data density is 6250 cpi (246 c/mm).

The file mark is specified as 250 to 400 flux reversals, all 1s, at 9042 frpi in channels 7, 2, 6, 5, P, and 0, and dc-erased in channels 3, 1, and 4.

1.9.6 ERASE VARIABLE LENGTH

The erase variable length command causes tape to be moved in the forward direction with erase current on. A LAST WORD (ILWD), P100-4 signal from the controller terminates the erase operation.

Note

In PE/GCR format, the ID burst will not be erased when an erase command is given from BOT.

Command	IREV	IWRT	IWFM	IEDIT	IERASE
Read Forward	H	H	H	H	H
Read Reverse (Normal)	L	H	H	H	H
Read Reverse (Edit)	L	H	H	L	H
Write	H	L	H	H	H
Edit	H	L	H	L	H
Write File Mark	H	L	L	H	H
Erase (Variable Length)	H	L	H	H	L
Erase (Fixed Length)	H	L	L	H	L
Space Forward	H	H	H	H	L
Space Reverse	L	H	H	H	L
File Mark Search Forward	H	H	L	H	H
File Mark Search Reverse	L	H	L	H	H
File Mark Search Forward (Ignore Data)	H	H	L	H	L
File Mark Search Reverse (Ignore Data)	L	H	L	H	L
Security Erase	H	L	L	L	L

L = Low = True
H = High = False

Table 1-3

Transport Commands

1.9.6.1 Erase Fixed Length

This command causes a 4.0 inch (10.16 cm) length of tape to be erased.

1.9.6.2 Security Erase

The security erase command causes tape to be erased from its present position to a point 3 to 5 feet after EOT. Tape is then rewound to BOT.

1.9.7 SPACE FORWARD

This command is similar to a read forward command except that no Read Strobe (IRSTR) signals are supplied to the controller. Error checking is not performed, but a test is made to determine if the record spaced over was a file mark.

1.9.8 SPACE REVERSE

This is similar to a read reverse command except that no (IRSTR) signals are supplied to the controller. Here error checking is not performed. A test is made to determine if the record spaced over was a file mark.

1.9.9 REWIND

The rewind command causes the transport to rewind to BOT. In systems where more than one transport is daisychained, it is possible to rewind several transports while transferring data to or from another transport in the chain.

1.9.10 FILE MARK SEARCH FORWARD/REVERSE

A file mark search foward command causes the transport to execute a series of read forward commands, while the reverse command causes the transport to execute a series of read reverse commands. Both series are terminated by the recognition of either a file mark character or the EOT tab. Tape is stopped following the reading of a file mark in a manner similar to terminating a normal read operation.

If the BOT tab is encountered during a file mark search operation, the operation is terminated. The file mark search forward command may be combined with a space forward command, thereby preventing IRSTR, ICER, and IHER signals from being presented at the transport unit to controller interface. The file mark search reverse command may be combined with a space reverse command, thereby preventing IRSTR, ICER, and IHER signals from being presented at the transport unit to controller interface.

1.9.11 OFF LINE (REWIND AND UNLOAD)

This command places the unit under local control. This also causes the tape transport to perform a rewind/unload operation.

1.10 CONTROLLER TO TRANSPORT INTERFACE SIGNALS

1.10.1 FORMATTER ADDRESS (IFAD)

LEVEL P200-48

This is a level (ex: high = address 0, low = address 1) which selects the formatter transport unit, in which it will address.

Note

The transport addresses are predetermined by switches on the Pertec Interface board. This is also true for the formatter addresses, density select, and variable speed GCR. See dip switch configuration flow diagram (Figure 1-12), for the options available on the I/O lines of the interface. These options are only made available with wire wrapped interface boards.

1.10.2 TRANSPORT ADDRESS (ITAD0/ ITAD1)

LEVEL P100/200-46

This level selects the transports which may be daisychained to each other.

1.10.3 INITIATE COMMAND (IGO)

PULSE P100-8

This pulse initiates the commands given in Table 1-3. On the trailing edge of IGO, the command lines described in paragraphs 1.10.4 through 1.10.8 are copied into the transport formatter and the formatter busy signal (IFBY) is set low. IFBY is described in section 1.11.1.

1.10.4 REVERSE/FORWARD (IREV)

LEVEL P100-18

This signal specifies forward or reverse tape motion. When the signal goes low a reverse is executed; when it goes high a forward command is executed.

1.10.5 WRITE/READ (IWRT)

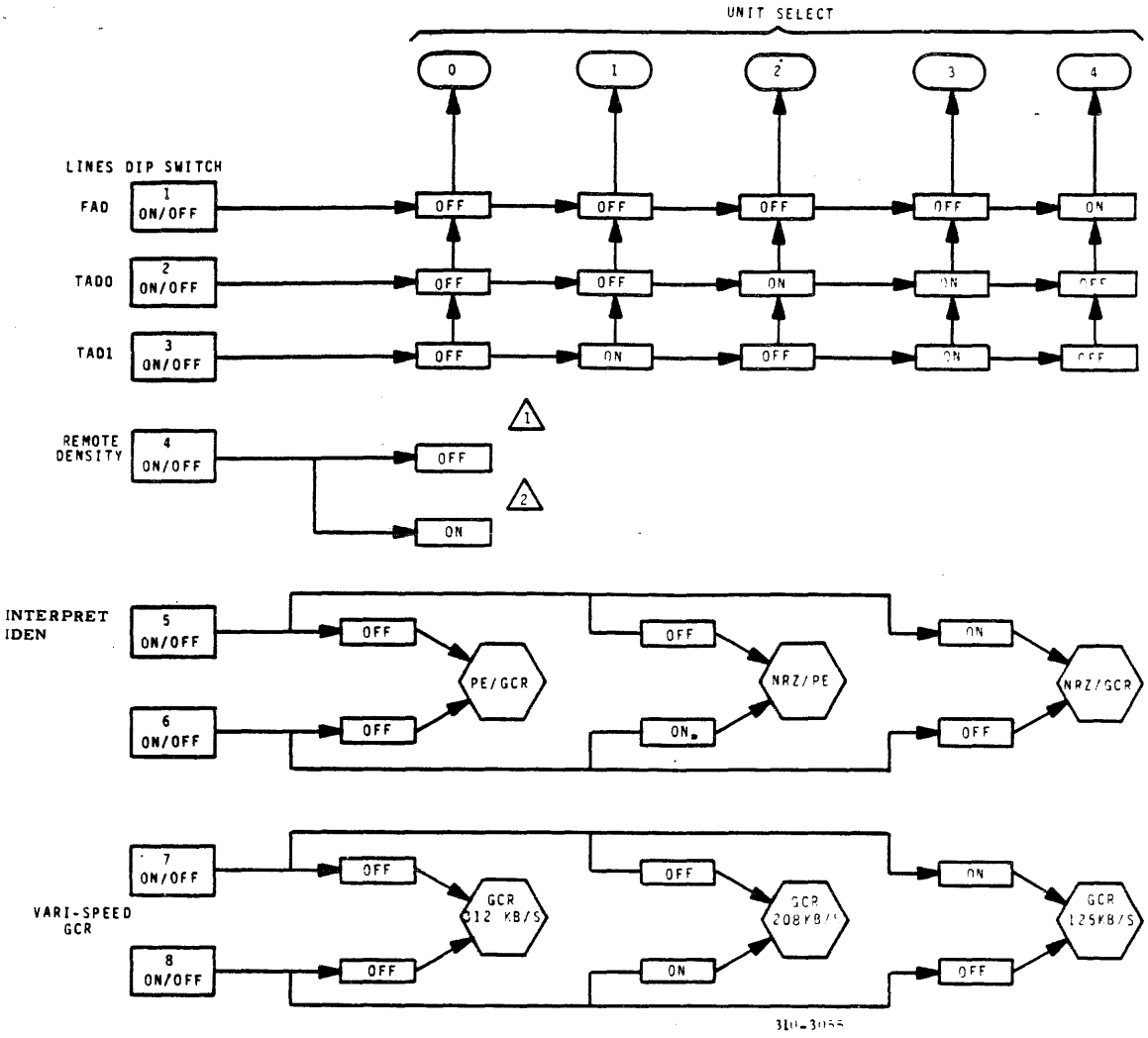
LEVEL P100-34

This signal specifies the operation mode of the system. When the signal is low a write command is executed; when the signal goes high a read command is executed.

1.10.6 WRITE FILE MARK (IWFM)

PULSE P100-42

This pulse causes a write file mark to be written on the tape, if IWRT is also low during this time.



1 REMOTE WILL LOOK AT (DUAL DENSITY) 2 OF THE 3 DENSITIES ONLY. WHICH DENSITY IT LOOKS AT DEPENDS ON THE SETTING OF SWITCHES 5 AND 6.

2 REMOTE HAS TRIDENSITY AVAILABLE, BASED ON OPTDEN LINE AND IDEN.

NOTE:
'IOPTDEN' IS A HARDWARE LINE WHICH MAY OR MAY NOT BE UTILIZED. IF IOPTDEN IS USED, THEN TABLE I IS APPLICABLE. IF IOPTDEN IS NOT USED THEN 'IDEN' TOGETHER WITH SWITCHES 5 AND 6 SELECT THE DENSITY. AS AN EXAMPLE, SWITCHES 5 AND 6 BOTH OFF AND A HIGH 'IDEN' WILL SELECT GCR DENSITY.

IOPTDEN	IDEN	DENSITY
0	0	GCR
0	1	NRZI
1	0	PE
1	1	NRZI

TABLE I

Figure 1-12

PERTEC Interface Dip Switch Configuration

1.10.7 EDIT (IEDIT)

LEVEL P100-38

The edit signal is used in the following two ways:

1. Read Reverse: Modifies the read reverse stop delay to optimize head positioning when editing tapes.

2. Write: The transport write current is turned off gradually at the end of the record, thus preventing an adjacent data record from being erased.

1.10.8 ERASE (IERASE)

LEVEL P100-40

When IERASE and IWRT signals are low, the unit will perform a dummy write command. The transport unit will go through all the functions of a normal write operation, but no data is recorded. The length of tape erase is equivalent to the length of the dummy record as defined by LAST WORD (ILWD) Paragraph 1.10.12.

Alternatively, if the IERASE, IWRT, and IWFM signals are low, the unit will perform a dummy write file mark operation. A fixed length of tape is erased, approximately 4.0 inches (10.16 cm).

The IERASE signal is also used to inhibit Read Strobe (IRSTR) during a space operation (space forward or space reverse NSPC) or file mark search operation.

1.10.9 DENSITY SELECT (IDEN)
(DUAL OR TRI-DENSITY)

SIGNAL P100-50

Note

Consult the dip switch flow diagram (Figure 1-12) for available options in density select. The switch position will determine dual or tri-density operation.

This signal (dual density only) is used when the transport density select switch is in remote position. When true this signal selects the high write density. Density will initially default to that of the mounted tape (in read mode), then it can be manually or remotely selected.

1.10.10 REWIND (IREW)

PULSE P100-20

IREW causes the selected transport to rewind to load point (BOT mark).

Note

This command will be executed only if the transport is ready and on line. This command does not cause the unit to become busy.

1.10.11 OFF LINE (IOFL)

PULSE P200-24

When this line is pulsed the unit will go off line and initiate a rewind command. After reaching BOT it will unload tape. If the unit is already rewinding at the time an off line command is given, the unit will wait for BOT and perform an unload sequence.

1.10.12 LAST WORD (ILWD)

PULSE P100-4

During a write or an erase command, this pulse is used to indicate that the next character to be strobed into the transport unit is the last character of the record.

1.10.13 FORMATTER ENABLE (IFEN)

LEVEL P200-18

When true (low) this line enables the transport. When false (high) it causes the unit to be reset to the quiescent state.

1.10.14 WRITE DATA INPUTS (IW_)

Track	Pin Location
IWP	P100-22
IW0	P100-10
IW1	P100-12
IW2	P100-30
IW3	P100-26
IW4	P100-6
IW5	P100-32
IW6	P100-28
IW7	P100-24

These nine lines transmit write data from the controller to the transport unit, to be written on corresponding channels on tape. IW7 corresponds to the least significant bit of the character.

The first character of the data record should be available on these lines within one character period after IDBY goes true and should remain true until the trailing edge of the first IWSTR pulse issued by the microformatter. The next character must then be set up in less than a half-character period. Subsequent characters will be processed in this way until ILWD is set low, indicating that the last character is being transferred. Table 1-4 identifies these lines with regard to interface identification, track number and IBM/PERTEC channel.

USE WHEN HOST BINARY WEIGHT OF CHANNEL IS KNOWN.									
HOST (BINARY)	P	7 (2)	6 (2)	5 (2)	4 (2)	3 (2)	2 (2)	1 (2)	0 (2)
IBM/PERTEC CHANNEL NO	P	W0	W1	W2	W3	W4	W5	W6	W7
ANALOG READ/WRITE TRACK NO.	4	7	6	5	3	9	1	8	2
WSEQ	Y8	Y7	Y1	Y4	Y0	Y2	Y6	Y5	Y3
DESKEW	Y2	Y3	Y1	Y0	Y4	Y7	Y8	Y5	Y6
ECP	Y8	Y0	Y6	Y3	Y7	Y5	Y1	Y2	Y4
USE WHEN TRACK NO ON TAPE IS KNOWN.									
TRACK	1	2	3	4	5	6	7	8	9
HOST (BINARY)	2 (2)	0 (2)	4 (2)	P	5 (2)	6 (2)	7 (2)	1 (2)	3 (2)
WSEQ	Y6	Y3	Y0	Y8	Y4	Y1	Y7	Y5	Y2
DESKEW	Y8	Y6	Y4	Y2	Y0	Y1	Y3	Y5	Y7
ECP	Y1	Y4	Y7	Y8	Y3	Y6	Y0	Y2	Y5

Table 1-4
Track Identity

1.11 TRANSPORT CONTROLLER INTERFACE SIGNALS

1.11.1 FORMATTER BUSY (IFBY)

LEVEL P100-2

NOTE

This signal may be used by the controller to inhibit further commands.

When this status is issued, the IFBY goes low at the trailing edge of IGO and remains low until tape unit motion stops after execution of command.

1.11.2 DATA BUSY (IDBY)

LEVEL P200-38

The IDBY signal goes low when the transport has reached operating speed, traversed the IRG, and the transport is about to read or write data. IDBY remains low until the data transfer is finished and the appropriate post record delay is completed. IDBY goes high at the same time that the capstan starts to decelerate the tape. A new command may be given when IDBY goes high for an on-the-fly operation. On-the-fly commands must be of the same Read/Write mode and the same tape direction.

1.11.3 CHECK CHARACTER GATE (ICCG) IDENTIFICATION (ID)

LEVEL P200-16

This interface line is shared by NRZI, PE, and GCR format. In the NRZI format, the signal is ICCG and is set low by the transport unit when the read information currently being transmitted to the controller is either a CRCC or an LRCC. The signal is high when data characters are being transmitted. Data and check information can be distinguished by gating READ STROBE (IRSTR) with ICCG or its inverse.

1.11.4 HARD ERROR (IHER)

PULSE P200-12

This signal is set low if an uncorrectable read error is detected by the transport unit.

NOTE

All error information is reported to the controller before DATA BUSY (IDBY) goes false.

1.11.5 CORRECTED ERROR (ICER)

PULSE • P200-42

The ICER is used only in the PE mode. The signal is set low by a single track dropout during a read or read-after-write operation. ICER in a read-after-write operation indicates that the record should be rewritten.

1.11.6 FILE MARK (IFMK)

PULSE P200-14

File mark is pulsed when a file mark is detected during read or read-after-write operations. Error conditions should be ignored when a file mark is detected.

1.11.7 READY (IRDY)

LEVEL P200-28

This is a level which is true only when the transport is ready to receive external commands; the following conditions must exist:

1. All interlocks made
2. Initial load or rewind sequence is complete
3. Transport is on line
4. Transport is not rewinding

.11.8 ON LINE (IOL)

LEVEL P200-44

This level is true when the on line flip-flop is set, indicating the transport is under remote control. When false the transport is under local control.

1.11.9 REWINDING (IRWD)

LEVEL P200-30

This level is true when the transport is rewinding.

1.11.10 FILE PROTECT (IFPT)

LEVEL P200-32

The following will make this level true:

1. Power ON
2. Tape loaded and under tension
3. Supply reel has write enable ring removed

1.11.11 BEGINNING OF TAPE (IBOT)

LEVEL P200-4

When true, this signal indicates that tape is at rest with the BOT tab at the infrared sensor. Level goes false after BOT tab leaves sensor.

1.11.12 END OF TAPE (IEOT)

LEVEL P200-22

When true this signal indicates EOT tab is at infrared sensor.

1.11.13 TAPE SPEED (ISPEED)

LEVEL P200-40

When true this signal indicates that GCR mode is selected.

1.11.14 WRITE STROBE (IWSTR)

PULSE P200-36

The IWSTR line is pulsed for each data character to be written on tape. The pulsewidth of IWSTR is approximately 25 percent of a character time. IWSTR samples the WRITE DATA lines (IWP, IW0-7) from the controller and copies this information, character by character, into the transport unit write logic.

The first character must be available before the first IWSTR is issued, and succeeding characters must be set up within half a character period after the trailing edge of each IWSTR pulse.

This line is also active during Erase (Variable Length) commands; however, the data being copied into the unit will not be written on tape.

For a Write File Mark or Erase (Fixed Length) command, the required pattern is generated internally by the unit and IWSTR is not used.

1.11.15 READ STROBE (IRSTR)

PULSE P200-34

The READ STROBE line (IRSTR) is pulsed (1 usec minimum pulsewidth) for each character of read information (data, CRCC, and LRCC) to be transmitted to the controller. IRSTR is used to sample the READ DATA lines (IRP, IR0-7).

The transmission of check characters (CRCC and LRCC) is flagged by the CHECK CHARACTER GATE line (ICCG) and in the event of an all zeros character, an IRSTR pulse is provided.

Note that although the average time between adjacent IRSTR pulses (for PE and NRZI) is 1/BV where:

B = packing density

V = tape velocity

this time may vary considerably due to the combined effects of bit crowding and skew. The minimum time between adjacent pulses is one half character period.

In GCR read strobe separation does not vary. Refer to read timing diagrams (figures 1-4A through 1-10) for additional timing information.

1.11.16 READ DATA LINES

Track	Pin Location
IRP	P200-1
IRØ	P200-2
IR1	P200-3
IR2	P100-48
IR3	P100-50
IR4	P200-6
IR5	P200-20
IR6	P200-10
IR7	P200-8

These nine lines transmit read data from the transport unit to the controller. Each character read from the tape is available by sampling IRP, IR0-7 in parallel at IRSTR time.

Data remains set on IRP, IR0-7 for a full character period. The corresponding IRSTR pulse is placed centrally during the time that data is available.

1.12 OPTIONAL CONTROLLER REMOTE CONDITIONS

NOTE

The following optional remote conditions are only for the units with a wire wrapped Pertec Interface board.

The dip switch flow diagram (Figure 1-12) is an example of the various options available to the controller (remotely) on the Pertec Interface.

The flow diagram gives all possible switch positions available.

Switches 1, 2, and 3 are for controlling the formatter/transport address lines to the unit desired. Switches 4, 5, and 6 are the switches that can control dual or tri-density selection (remotely).

NOTE

If switch 4 is on the ON position, the controller must be capable of handling tri-density (GCR, NRZI, PE). If the controller cannot handle tri-density mode and the switch is at the ON position, it will only be able to write in a NRZI mode.

Switches 7 and 8 are to vary the GCR speed. Depending on the switch position, the speeds available are:

- 312 KB/sec, average 281 in read mode equivalent to 45 ips
- 208 KB/sec, approximate to PE at 125 ips
- 125 KB/sec, approximate to PE at 75 ips

SECTION II
INSTALLATION AND OPERATION

SECTION II

INSTALLATION AND OPERATION

2.1 INSTALLATION

2.1.1 SHIPPING CONTAINER

With another person's help, lift the 9400 tape drive out of the shipping container. When removing the unit from the shipping container, be careful that the dust cover (door) of the unit is secure to the body of the tape drive by the shipping tape attached. Perform the following steps after removing unit from shipping container. See Figure 2-1 for shipping container configuration.

Note

After removing the 9400 tape drive unit out of the shipping container, save the carton, shipping container, and shipping braces, for possible future use.

1. Place the 9400 unit in its upright position.
2. Remove the shipping braces.
3. Remove attached shipping tape.
4. Prepare for inspection per paragraph 2.1.2.

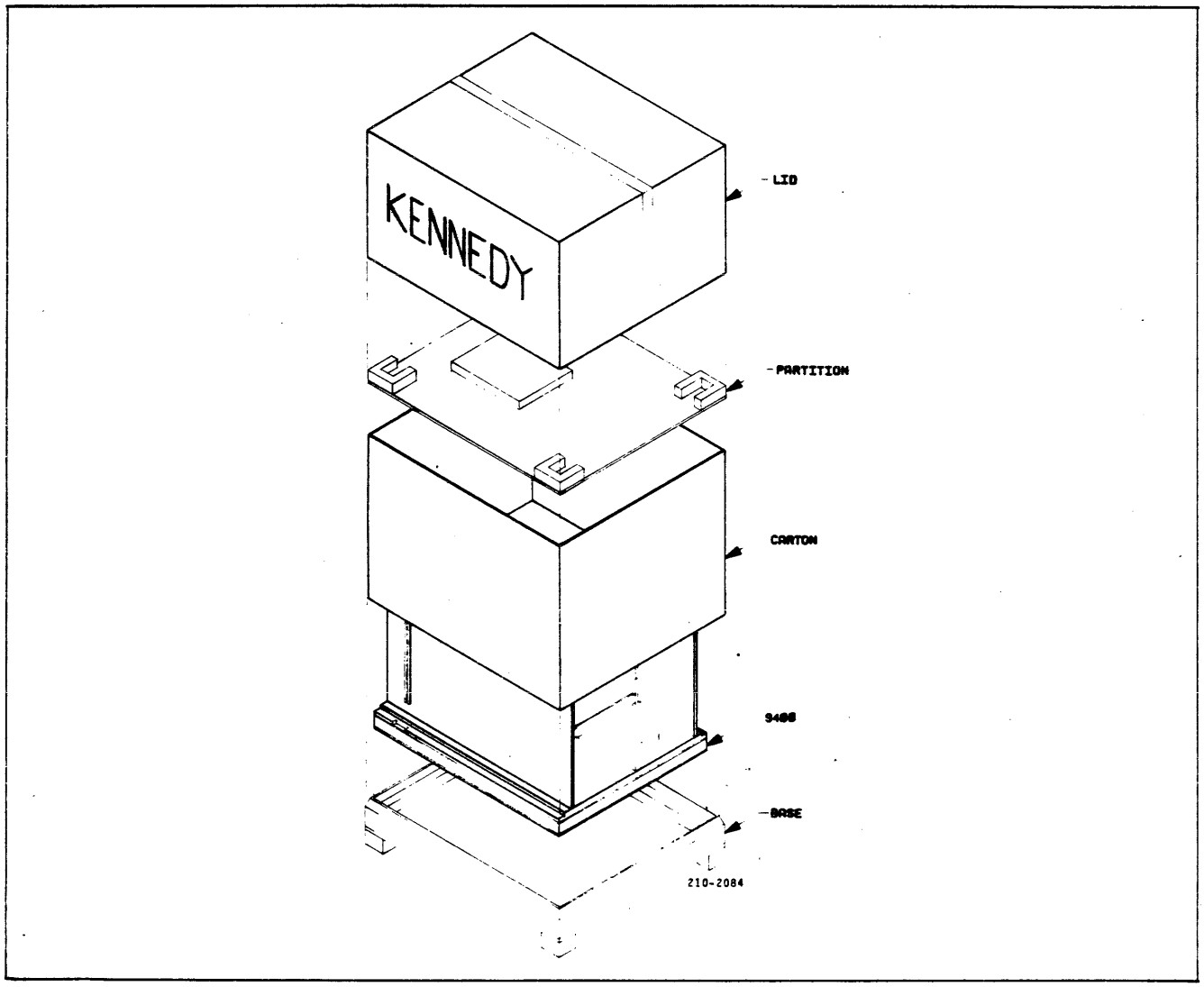


Figure 2-1

Shipping Container

2.1.2 INSPECTION

Prior to installation perform the following steps:

Visually inspect the entire 9400 unit for the following shipping damage:

a. Misaligned parts

b. Cosmetic scratches or dents

c. Foreign material that may have become lodged in drive mechanism (vacuum columns, reel hubs, etc.)

d. If any of the above mentioned (a, b, or c) is found to be true, you should contact your marketing representative.

2.1.3 MOUNTING

The transport unit requires 24.5 inches vertical mounting space on a standard 19 inch rack. The transport is mounted on a pair of slides which are provided in the shipping container. The rack slides must be mounted on customer's rack before unit can be mounted.

WARNING

9400 tape drive unit may cause personal injury when in the extended service position if the mounting rack is not properly secure to the ground and/or other adjacent racks.

The slides are equipped with a lockout mechanism, shown in Figure 2-2, which prevents slide overextension. Each slide has a slide designator which identifies the slide for right-hand or left-hand mounting.

Note

To ascertain that the slides are mounted correctly, open one slide (of the pair) and look for the letters RH (right-hand) or LH (left-hand) stamped directly above the lockout lever, as shown in Figure 2-2.

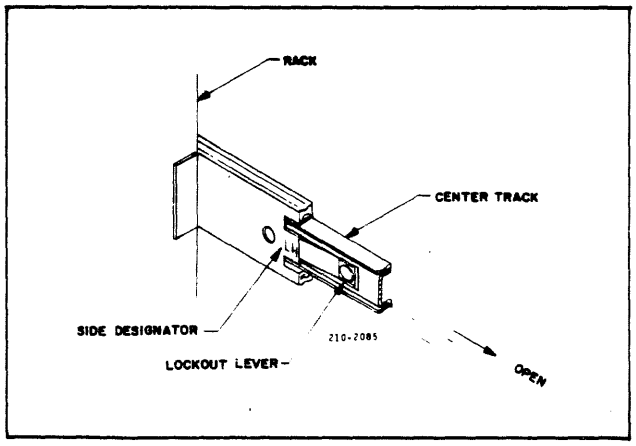


Figure 2-2

Rack Slide Identification

With the right- and left- hand slides securely fastened to the rack (cabinet) and in the extended position, align the quick disconnect strips (attached to the sides of the unit) with the center tracks of the slides, as shown in Figure 2-3.

CAUTION

To avoid personal injury and/or transport damage due to dropping of unit, secure transport in place by aligning captive screws on each side with respective threaded holes in the disconnect strips and tighten, as shown in Figure 2-3.

After securing the transport to the tracks on the cabinet, push unit towards cabinet until fully engaged. It may now be locked by turning a lock screw in front of the lower left-hand side of transport fully clockwise.

To service/test transport's electronics, turn lock screw counterclockwise to unlock unit and extend outward to service position.

2.1.4 SERVICE ACCESS

To obtain access to the plug-in cards and control electronics the unit must be extended forward on its slides. The voltage regulator and servo power assembly are mounted on the inside of the heat sink, on the right-hand side of the transport.

Circuit breakers and power connector are accessible from the rear of the unit. Control electronics are accessible in the left-hand side of the unit.

For servicing, electronics test points are provided by standoff pins on the circuit boards, which are identified by upper case letters near each test point.

2.1.5 SUPPLIED/REQUIRED ITEMS

Table 2-1 shows supplied and required items for the 9400 tape drive unit.

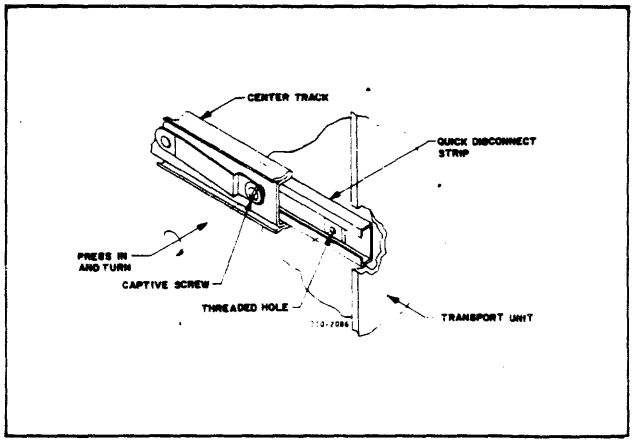


Figure 2-3

Rail/Transport Mounting Assembly

Nomenclature	Part Number	Qty
O&M Manual	9400	1
Empty 10.5" Reel	113-0008-001	1
Power Cord	121-0198-003 (115v)	1
Optional	121-0198-104 (240v)	
Slide & Rail Assy	190-5507-001	1
Shipping Brace	291-4768-001	1

Table 2-1
Supplied/Required Items

2.1.6 INTERCABLING DESCRIPTION (PERTEC)

Two 50-lead flat cables are used for transport-to-controller interface. Interface lines to and from the transport are TTL compatible, single-ended. Pulsewidths are 200 nanoseconds or greater, unless otherwise noted. See Section I for interface configuration.

2.1.6.1 50-Lead Flat Cable

The 50-lead flat cable should be 28 AWG and not exceed a maximum limit of 20 feet (6.1 meters) in length.

2.1.7 POWER-UP CONNECTIONS

CAUTION

Make certain that line voltage is correct before connecting unit to power source. See specification table for correct power source usage.

A detachable power cord is supplied with the tape unit. The power cord is 6.6 feet (115v) or 9.8 feet (240v), and has a NEMA three prong (two power, one chassis ground) plug for connection to power source.

Connect the power cord to the proper line source and push primary power switch on control panel to ON position.

2.2 OPERATION

2.2.1 INTERFACE

Interface operation and characteristics are outlined and performed in Section I.

2.2.2 CONTROLS AND INDICATORS

Figure 1-2 in Section I shows the controls and indicators for the tape transport.

2.2.3 TAPE THREADING

To thread the tape on the transport, proceed as follows (see Figure 2-4):

a. Raise the latch of the quick-release hub and place the tape reel to be used on the supply hub with the write enable ring side facing the transport deck.

b. Hold the reel flush against the hub flange and secure it by pressing the hub latch down.

c. Thread the tape along the path shown on the tape threading diagram (Figure 2-4).

d. Holding the end of the tape, wrap a few clockwise turns around the take-up reel.

2.2.4 TAPE LOADING

After the tape is fully threaded, the unit is in position to load the tape. Depressing the LOAD switch energizes the reel servos and initiates a load sequence including vacuum column power up. The tape advances to load point marker (BOT) and stops.

Note

If for some reason BOT is already past the sensor, for example, when restoring power after shutdown or from over-threading, tape will continue to move forward for a few seconds and initiate rewind command automatically until BOT is found.

Once pressed, the LOAD switch is illuminated and remains illuminated until power is turned off or tape is unloaded from the unit.

If power is turned off the LOAD switch must be depressed to load the tape again.

2.2.5 PLACING TAPE UNIT ON LINE

After unit is loaded and brought to the load point (BOT), press the ON LINE pushbutton and make certain the ON LINE indicator illuminates.

Note

All the front panel controls are disabled when the tape unit is ON LINE, except for the density select switch. The density select must be in the remote position, in order to control the density remotely.

ON LINE status enables the tape unit to be remotely selected and to perform all normal operations under the controller direction.

2.2.6 UNIT OFF LINE

To take the unit OFF LINE, the ON LINE switch must manually be depressed again and the ON LINE LED should go off. With the ON LINE mode off, the unit can now be controlled by the control panel.

Note

When selecting density modes from the front panel, the tape must be at BOT in order to operate the DENSITY SELECT switch.

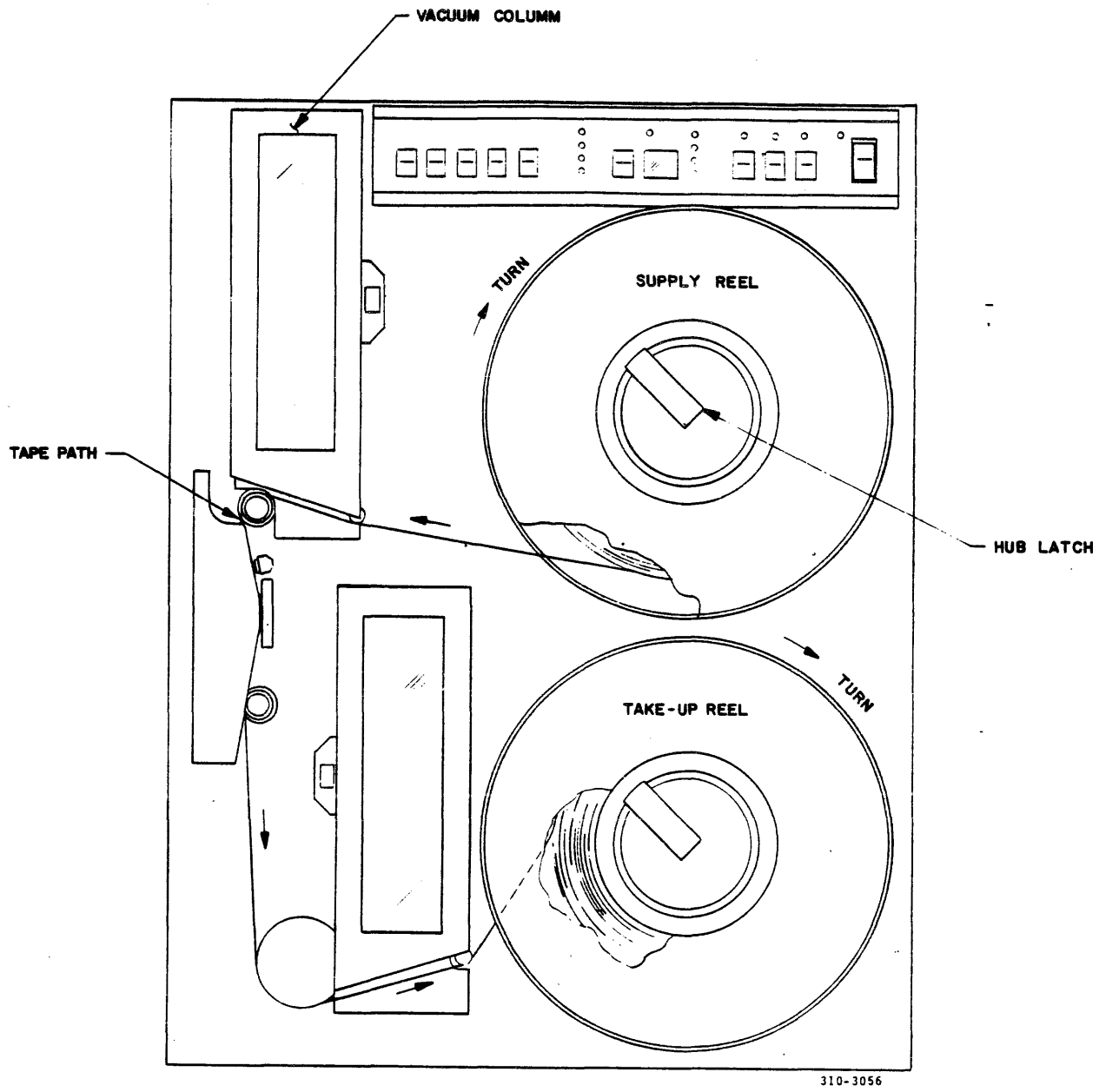


Figure 2-4

Tape Threading Diagram

2.2.7 TAPE UNLOADING AND REWINDING

The 9400 can remotely rewind a tape to BOT however this operation can also be performed manually as follows:

a. If the ON LINE indicator is illuminated, press the ON LINE pushbutton. The ON LINE indicator should turn off.

b. Press the REWIND pushbutton. The tape will now rewind to BOT.

c. Press load switch, LED should turn off. The unit will now go through an unload sequence, turning off the vacuum columns and rewinding tape entirely on to the master reel.

Note

If power source is completely lost when rewinding, the unit will shut down and not rewind or tension tape. If this happens proceed as follows:

1. Reset circuit breaker (change fuses if your unit contains fuses), and restore power source.
2. Depress load switch, (LED will illuminate when on). At this time the tape unit will power up and restore tape to BOT.

d. Now that the tape is at BOT, depress the LOAD button so that the LED will go OFF.

After step d, the vacuum column will shut down and the tape will slowly unthread itself onto the master reel in its unload sequence.

To load another tape onto the unit proceed to paragraphs 2.2.3-2.2.5 and follow exact sequence given.

2.2.8 POWER SHUTDOWN

2.2.8.1 Panel Power Switch

In the event the power switch is turned off during rewind or forward mode, the unit will immediately shut down; it will not take up the tension on the tape. In the event the power source line fails while writing or reading on tape, the unit will immediately shut down. In this shutdown the tape will not rewind or take up tension. On power up tape must be reloaded. After the tape is loaded the controller can now search for the data block on which it was on and continue.

SECTION III
THEORY OF OPERATION

3.0 THEORY OF OPERATION

Sections 3.1 through 3.5.3.8 of this portion of the manual gives a brief description and general overview of the 9400 Tri-density Tape System. The remaining sections of chapter three gives a detailed description of the system and references the schematics in section VI.

3.1 GENERAL INTRODUCTION

The 9400 Tri-density Tape System (TTS) provides high speed, low cost mass storage by providing three modes of operation, the:

1) 800 bpi NRZ1 (75 ips) mode is provided for Industry Standard interchangeability at a nominal data rate of 60 kilobytes per second.

2) 1600 bpi PE (75 ips) mode provides a medium density storage capability at a nominal data rate of 120 kilobytes per second.

3) 6250 bpi GCR (45 ips) mode provides high density storage and high data reliability at a nominal data rate of 280 kilobytes per second.

The formatter for the three modes is embedded in the 9400 system electronics which allows for interfacing through a Host I/O interface. The system utilizes the proven technology of the 9100 mechanical tape path and servo design and combines this technology with the latest state-of-the-art electronic advancements. This includes bit slice microprocessor technology, an 8088 microprocessor, and a RS-232-C diagnostic port.

3.2 SYSTEM CONFIGURATION

The 9400 TTS can be divided into several subsystems consisting of the following:

1) I/O Host Interface

2) System Processor

3) Write Data Handler

4) Front Panel (Keyboard)

5) Analog Read/Write Amps

6) Read Decoders I and II

7) Read Data Handler

8) Servo/Tape Transport/Vacuum System

9) Power Supplies

The various subsystems are illustrated in figure 3.1.

3.2.1 I/O HOST INTERFACE

Because of the modular design of the system a number of Host interfaces can be interchanged with only the replacement of an interface card. The four customized interface cards consist of the following:

1) Pertec

2) Pico

3) STC

4) Telex

All interfaces are field interchangeable, single PC boards. Specific data on each interface will be found in Section I of this manual.

3.2.1.1 PERTEC INTERFACE

The Pertec interface is an Industry Standard which is configured with two 50 pin flat ribbon cable connectors. The interface has 16 Data Lines, 19 Status Lines and 15 Command lines.

3.2.1.2 PICO INTERFACE

The Pico interface is configured with a 34 pin flat cable

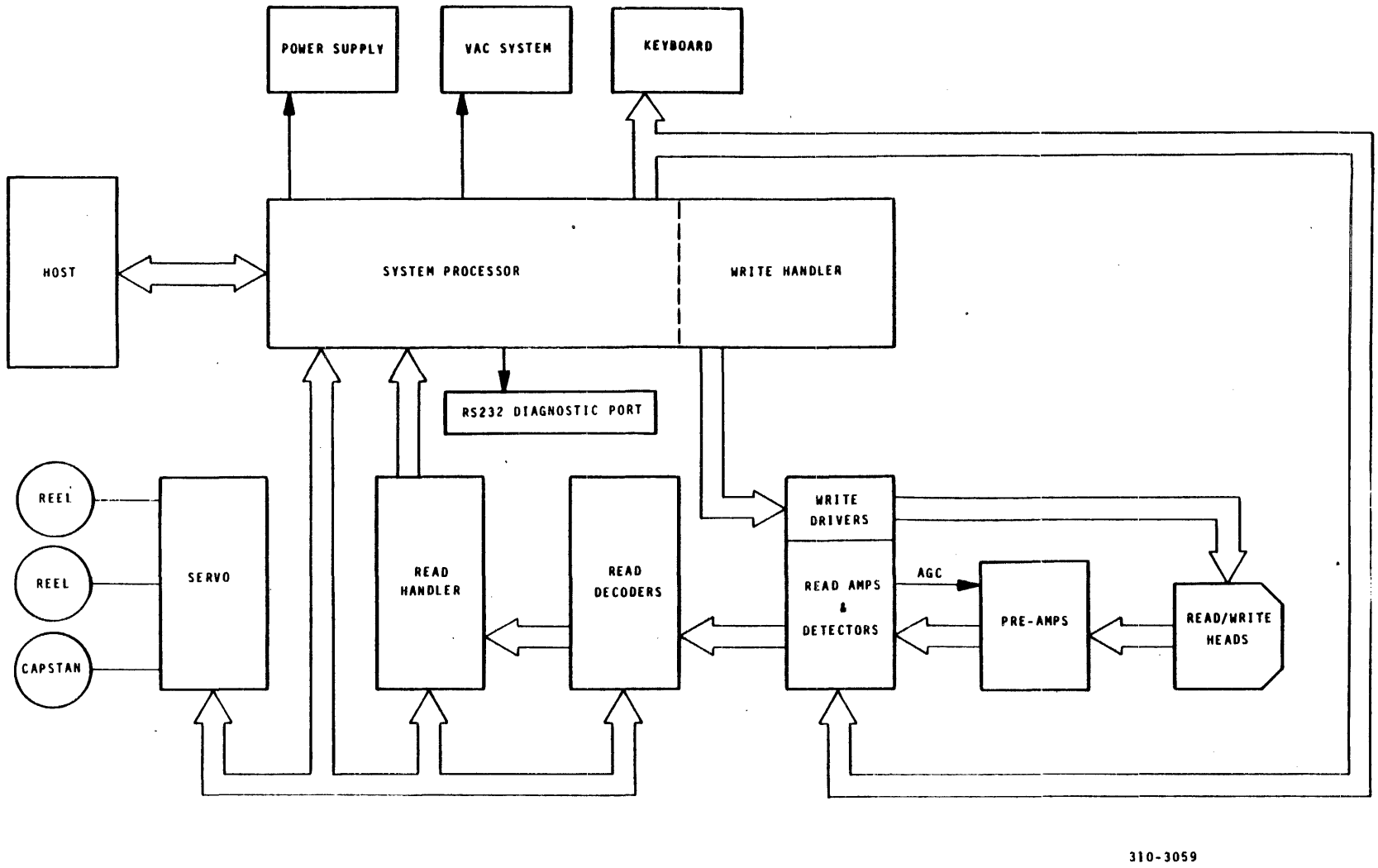


Figure 3-1

9400 System Block Diagram

connector which includes 17 single lines with the following capabilities:

1) 8 bi-directional bus lines

2) 2 uni-directional parity lines

3) 6 uni-directional control lines

4) 1 Cable Monitor

The interface supports transfer rates up to 312 kilobytes per second, and provides Error Status and Configuration information.

3.2.1.3 STC INTERFACE

The STC interface is configured with a 30 conductor twisted pair (input signals) and a 60 conductor flat cable (output signals). The host configuration will control up to 4 tape drives.

3.2.1.4 TELEX INTERFACE

The Telex interface is configured with three 25 pin connectors. The interface has 61 signal lines providing digital information which includes:

1) 3 Addressing lines

2) 2 Density lines

3) 6 Command and Command clock lines

4) 22 Status lines from the formatter

5) 4 Error Status bytes

6) 19 Data Operation lines

The Telex controller may be able to interface with up to 8 model 9400's, depending on the controller and host.

3.2.2 SYSTEM PROCESSOR

The 9400 utilizes an Intel 8088 16 bit CPU with an 8 bit data bus. The System Processor has control over the Keyboard, Read/Write Data Handlers, Servo/Tape transport System, Read Decoders, Analog Read/Write amplifiers, the Power Supplies and Vacuum System. The System Processor circuitry supplies a 5MHz System clock as well as a 2.5MHz Peripheral clock, Reset and Ready lines. The major portion of the operating software is accessed by 15 prioritized interrupts. The System Processor block diagram, is shown in figure 3.2.

3.2.3 WRITE DATA HANDLER

The Write Data Handler (fig. 3.3) encodes data received from the Host Interface or the System Processor FIFO, into GCR, PE, or NRZI format and outputs a real-time encoded data stream to the write amplifiers. The Write handler also writes tape and ID marks depending on the chosen format.

3.2.4 FRONT PANEL

The front panel is an Intel 8279-5 programmable Keyboard/Display I/O Interface configured with a vacuum switch (internal to the system), a Power switch, 9 panel switches, 13 LED indicators, and two LED displays. The Front Panel Keyboard operates in a decoded scan sensor matrix mode with an ISWITCH interrupt generated whenever a switch is pressed or released. Key status (open or closed) is stored in RAM addressable by the CPU. The keyboard allows operator control of the system and diagnostic test routines.

3.2.5 ANALOG READ/WRITE AMPS

The Analog Read/Write circuitry comprises the input Data section of the system. Figure 3.4, a block diagram of the Analog Read/Write board, illustrates the following:

1) WRITE HEAD DRIVERS: Nine write head drivers force a constant current through each track of the write head. A simple square-wave drive is used.

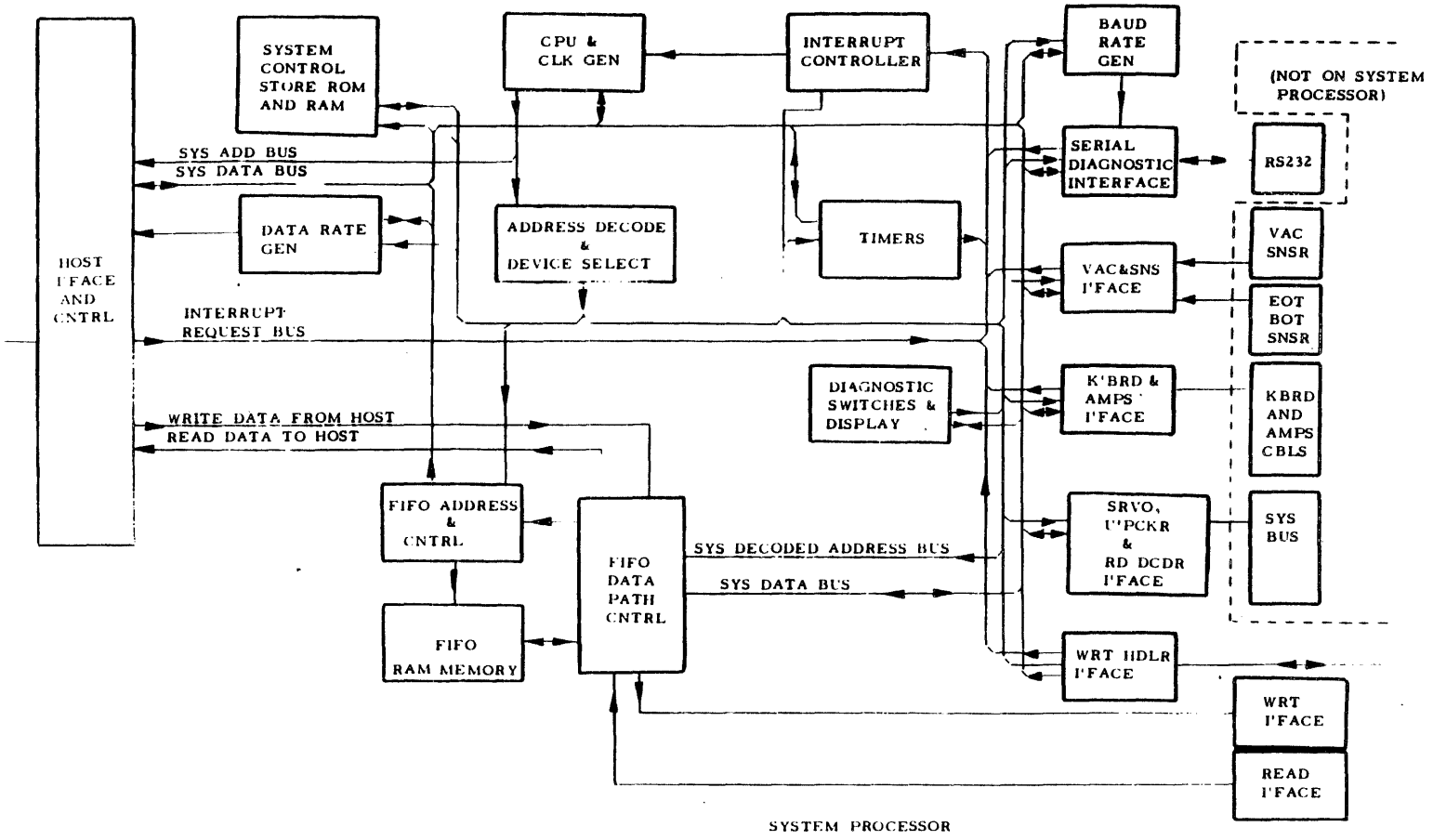


Figure 3-2

System Processor Block Diagram

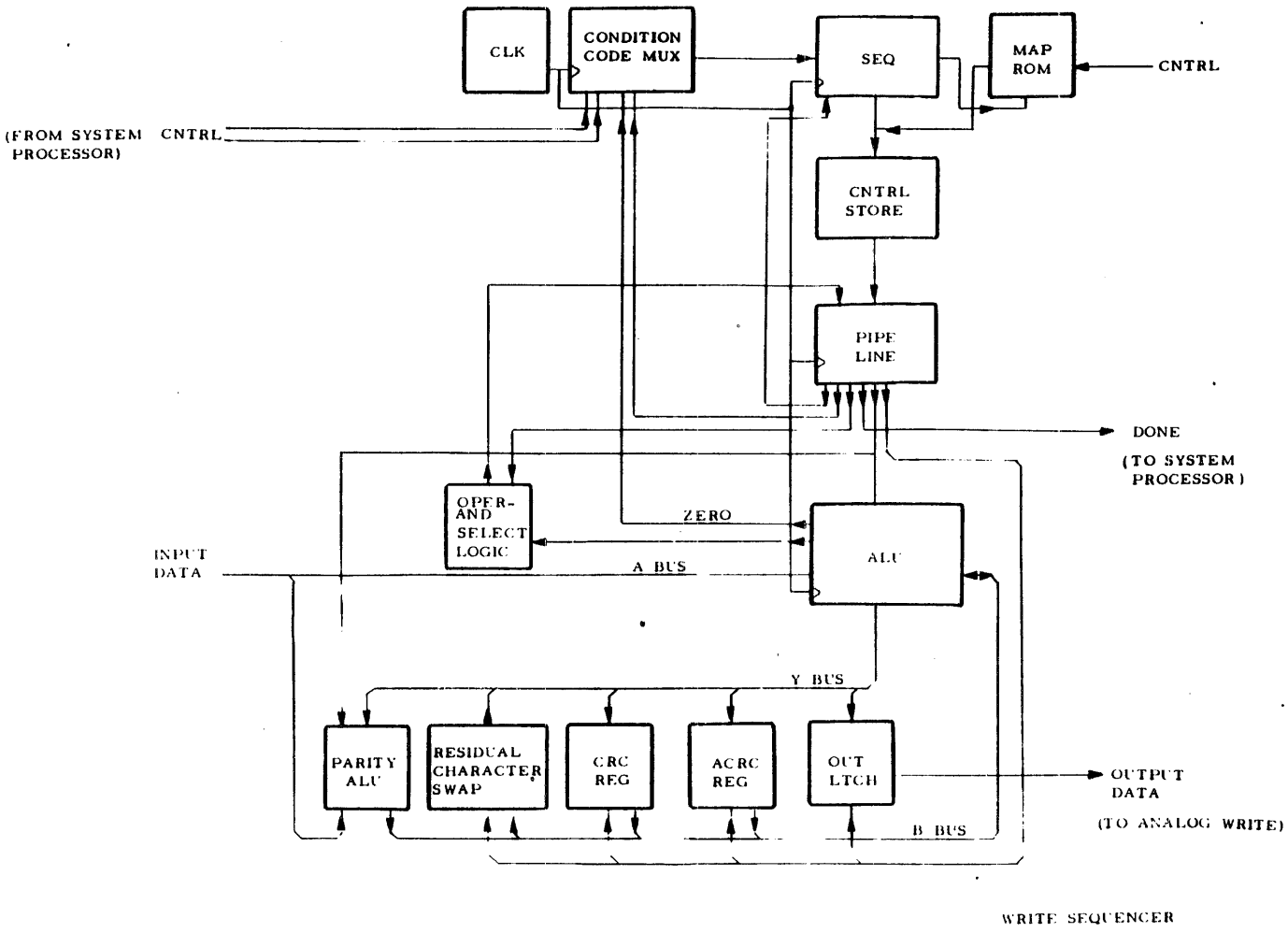


Figure 3-3

Write Data Handler Block Diagram

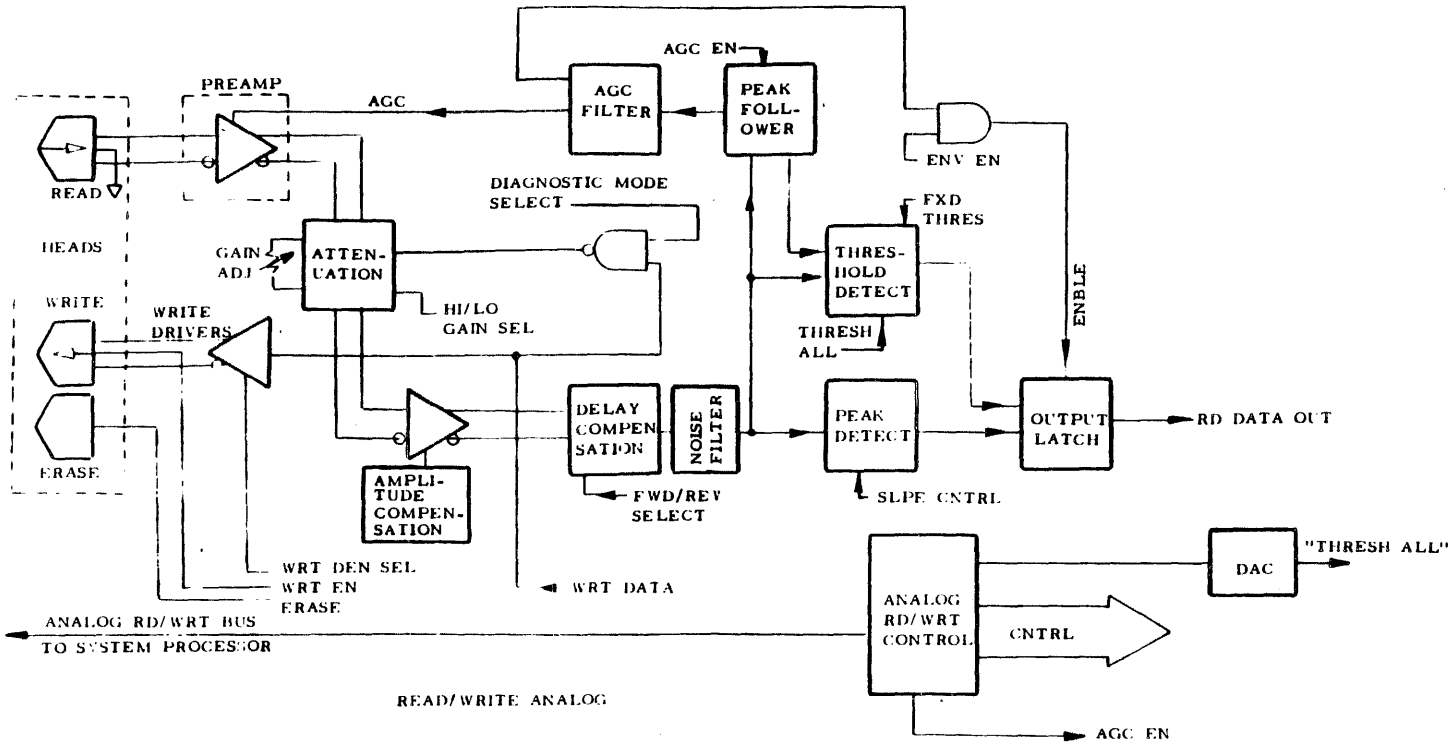


Figure 3-4

Analog Read/Write Block Diagram

2) READ AMPLIFIERS: Nine equalized read amplifiers filter the data pulses from the read head/preamp assembly to minimize "peak-shift" and noise.

3) THRESHOLDING: Each read channel incorporates a programmable threshold detector. The threshold can be set using the onboard DAC, or a variable threshold which is a fixed percentage of the signal. The threshold establishes the minimum signal amplitude that can be detected as a valid signal.

4) PEAK FOLLOWER: Each read channel incorporates circuitry that produces a variable DC voltage roughly equal to the peak-to-peak amplitude of the readback signal. The primary function of this signal is to establish the automatic threshold during read-only operation.

5) AUTOMATIC GAIN CONTROL: The peak follower signal is sampled, filtered and fedback to the preamp board assembly as a form of gain control in the read-only mode.

6) HIGH/LOW GAIN: The gain is a selectable function in which a known degree of attentuation can be introduced ahead of the read amplifiers to normalize all read channels to the same output signal level. The degree of attenuation can be independently adjusted by separate potentiometers for each channel (potentiometers are effective only when low gain is selected).

7) PEAK DETECTOR: The peaks of the analog read waveform are detected and outputted as logic-level transitions after being gated by the thresholding circuitry.

8) DIAGNOSTICS: Three levels of programmable diagnostics are available: direct coupling of the write input to the read output; injection of a filtered portion of the write signal into the read amp input; and crossfeed coupling of the write signal into the read preamp through the head itself.

9) WRITE DIAGNOSTICS: The total write head current can be monitored and compared with the expected normal range for the density selected. Any deviation from this range generates an error signal which can be noted by the System Processor. This test is carried on off line under operator control. The erase head can also be monitored by a status line.

10) SYSTEM INTERFACE: The status and functions of the Read/Write board are interfaced to the System Processor board by an 8255A-5 Programmable Peripheral Interface (PPI) chip.

3.2.6 READ DECODERS I AND II

The Read Decoders (fig. 3.5) track the tape speed and generate

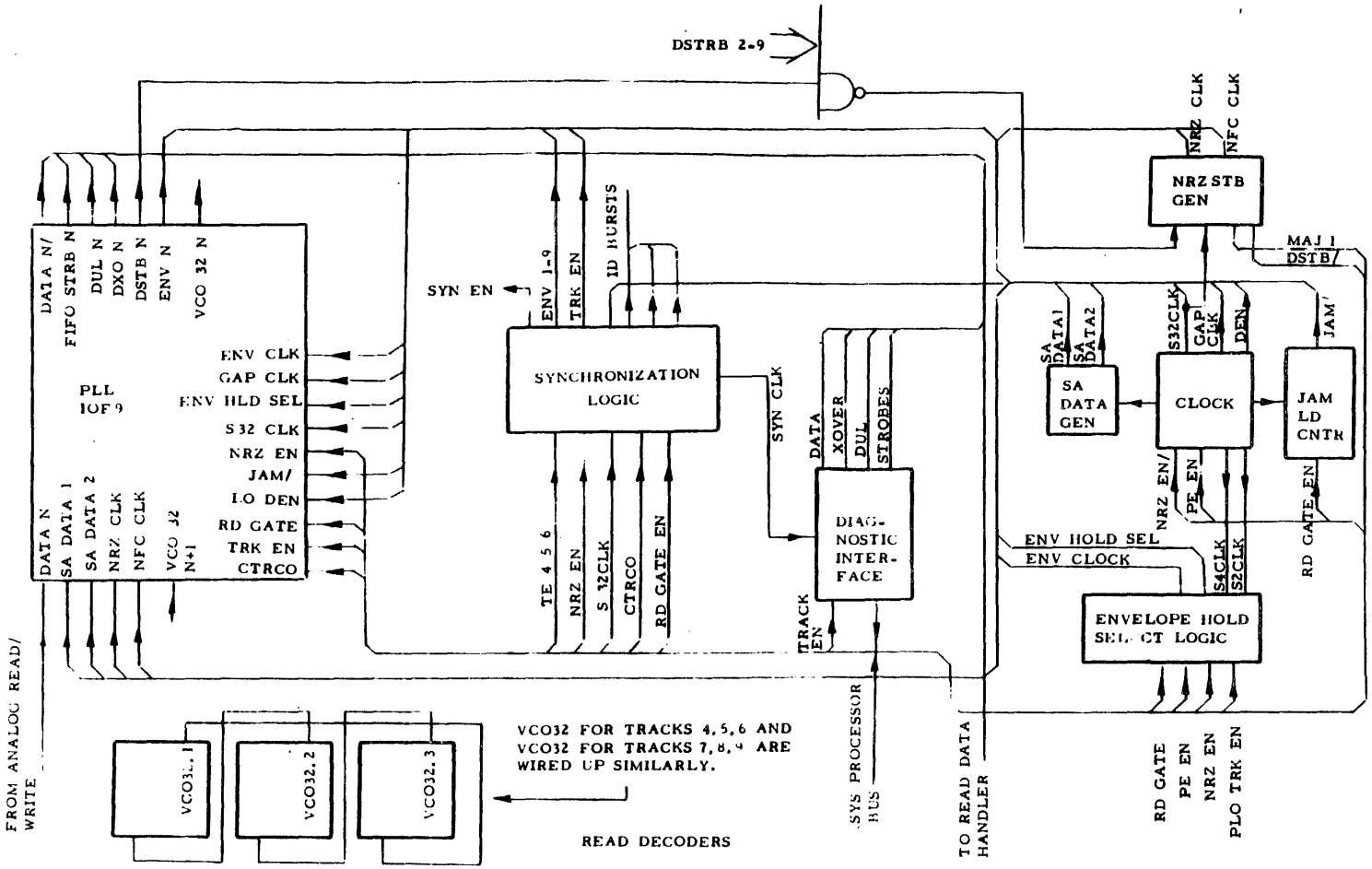


Figure 3-5

Read Decoder I & II Block Diagram
(Sheet 1 of 2)

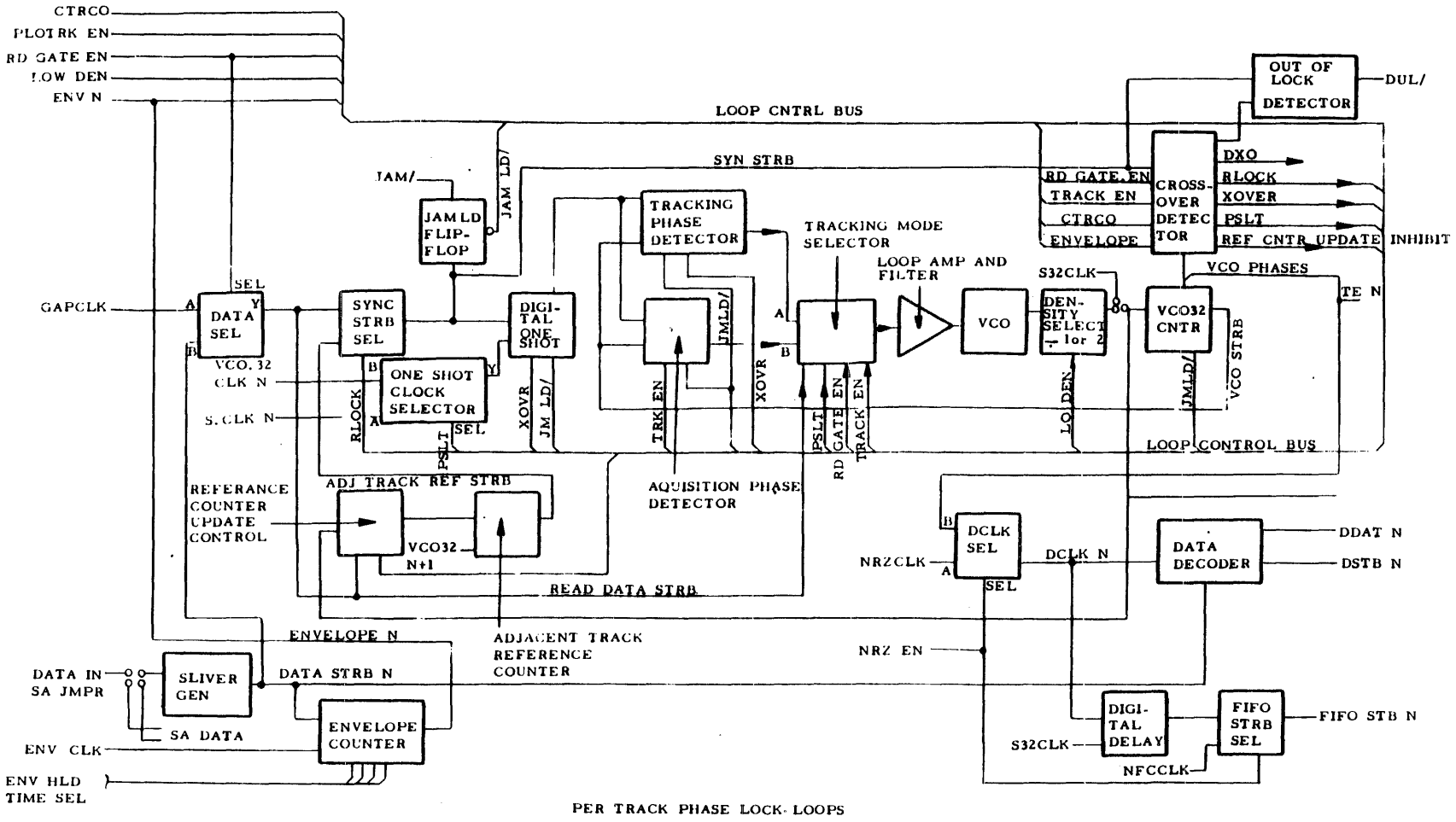


Figure 3-5

Read Decoder I & II Block Diagram

(Sheet 2 of 2)

NRZ1/PE/GCR data with accompanying strobes and error pointers. The decoders utilize separate VCO loops for each track of data eliminating errors due to dynamic skew. VCO loop out-of-lock conditions are indicated when detected and error pointers are generated by crossover detection. The Read Decoders also contain envelope detectors and ID and file mark recognition circuits.

READ DECODER I performs the data decoding of tracks 1-3, generates crystal frequencies for both Read decoders I and II and NRZ1 clocks for decoding NRZ1 data.

READ DECODER II performs the data decoding of tracks 4-9 and contains loop synchronization circuitry and diagnostic interfacing.

3.2.7 READ DATA HANDLER

The Read Data Handler (fig. 3.6) accepts raw data from the Read Decoders and performs deskewing, error detection and correction. The Read Data Handler consists of two bipolar bit-slice processors, the Error Correction Processor (ECP) and the Deskew Processor. The processors communicate with each other through a shared two-port RAM memory. Both processors are mounted on a single PC board.

The ECP implements a two-track error correction algorithm for each rectangular data group, and verifies data integrity over the length of each record by checking the CRC and ACRC error detection characters.

The Deskew Processor aligns the 9 data channels (eliminating any time-wise skew between data channels caused by tape head misalignment), performs group 5-to-4 decoding, checks for dropouts or illegal five-codes in the data stream, and forms an 'error pointer mask' indicating which two channels are most likely to be in error based on illegal characters or crossover pointers from the data decoder. In the event of a failure to achieve or maintain alignment due to dropouts in the preamble or the data stream, the Deskew Processor will attempt a re-alignment procedure during resync bursts.

The Read Data Handler provides three status bytes to the System Processor, indicating various errors which may occur during the unpacking process. The Deskew Processor controls status bits indicating the occurrence of dropouts, illegal characters, uncorrected skew errors, or crossover errors during a record. The ECP has status bits indicating failure to verify the CRC or ACRC charactrers, or output data timing errors. There are two status registers containing Track-In-Error (TIE) pointers on a per record basis.

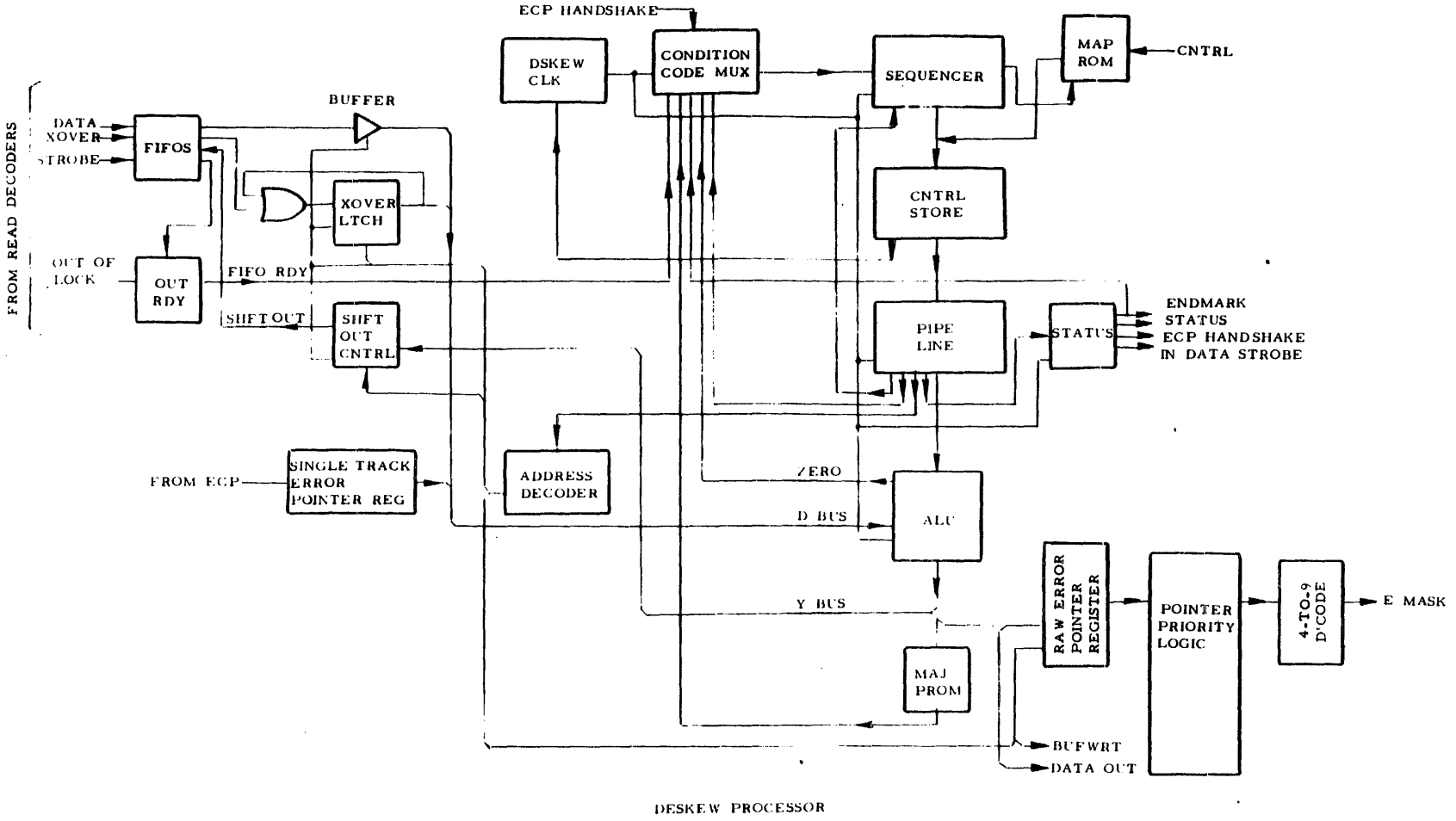


Figure 3-6

Read Data Handler Block Diagram
(Sheet 1 of 2)

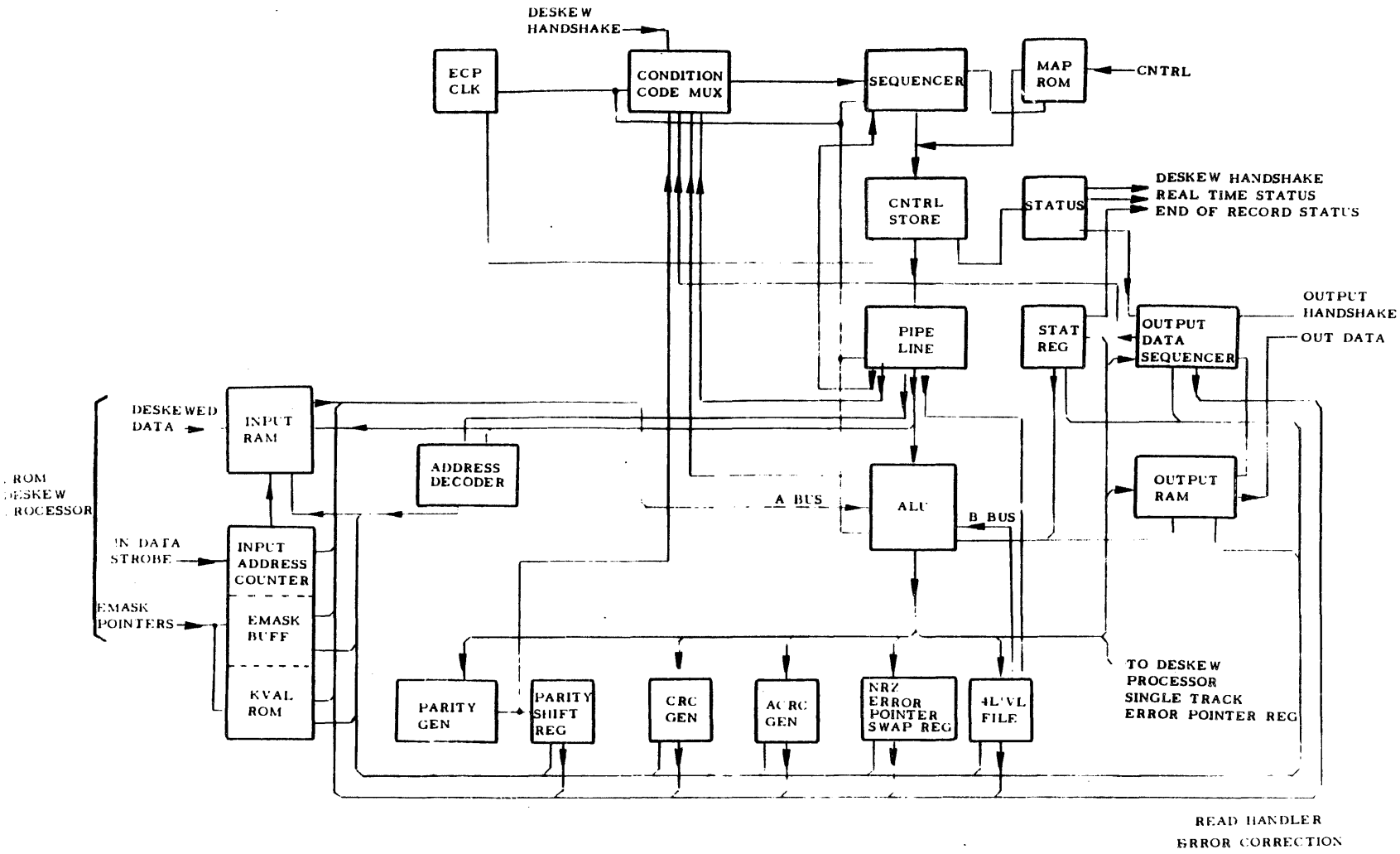


Figure 3-6

Read Data Handler Block Diagram
(Sheet 2 of 2)

3.2.8 SERVO/TAPE TRANSPORT SYSTEM

The Servo/Tape Transport System (fig. 3.7) achieves smooth, precise tape motion over the tape heads at a controlled speed while maintaining a constant tape tension. This task is accomplished by Reel Servos and Servo Amps, Vacuum Columns and Sensors, and a Capstan Motor and Amp.

1) REEL SERVOS & SERVO AMPS: Two permanent magnet, high torque DC motors are directly coupled to the supply and take-up reels. The Servos are driven by a set of amplifiers which receive information on tape ripple position from vacuum column sensors.

2) VACUUM COLUMNS & SENSORS: Supply and take-up vacuum columns are incoporated into the system for tape overshoots and compensate for the reel motors' high inertia, allowing the system to make rapid speed changes. Specially designed pressure-to-electrostatic transducer type sensors are housed in each vacuum column. The sensors are variable capacitors which consist of a perforated, plated PC board covered with flexible, metallized mylar (fig. 3.8). Each sensor is then mounted to a hollow metal chamber to form the base of the vacuum column. When vacuum is applied, tape is drawn upwards into the tape chamber and a high vacuum exists above the tape in the enclosed portion of the chamber. No vacuum exists at the open end of the tape chamber. A partial vacuum is present in the vacuum chamber behind the tape sensor. The metallized mylar diaphragm responds to the differences in pressure and varies the capacitance according to tape loop position.

3) CAPSTAN MOTOR & AMP: The capstan servo controls tape speed and acceleration. A low inertia motor is used to meet the short ramp demand of GCR formatted recordings.

3.2.9 POWER SUPPLY

Four 24 volt supplies are used to drive the Servos, providing +/- 24 volt and +/- 48 volt lines for low and high speed operation respectively. Two relays, K1 and K2, are incorporated into these supplies to select the required servo voltage and are processor controlled. In addition, +5 and +/- 12 volt lines are provided from separate supplies.

3.3 DATA FORMATS (NRZ1, PE, GCR)

3.3.1 NRZ1 FORMAT

Non-return to zero (NRZ1) is one of the basic methods of recording

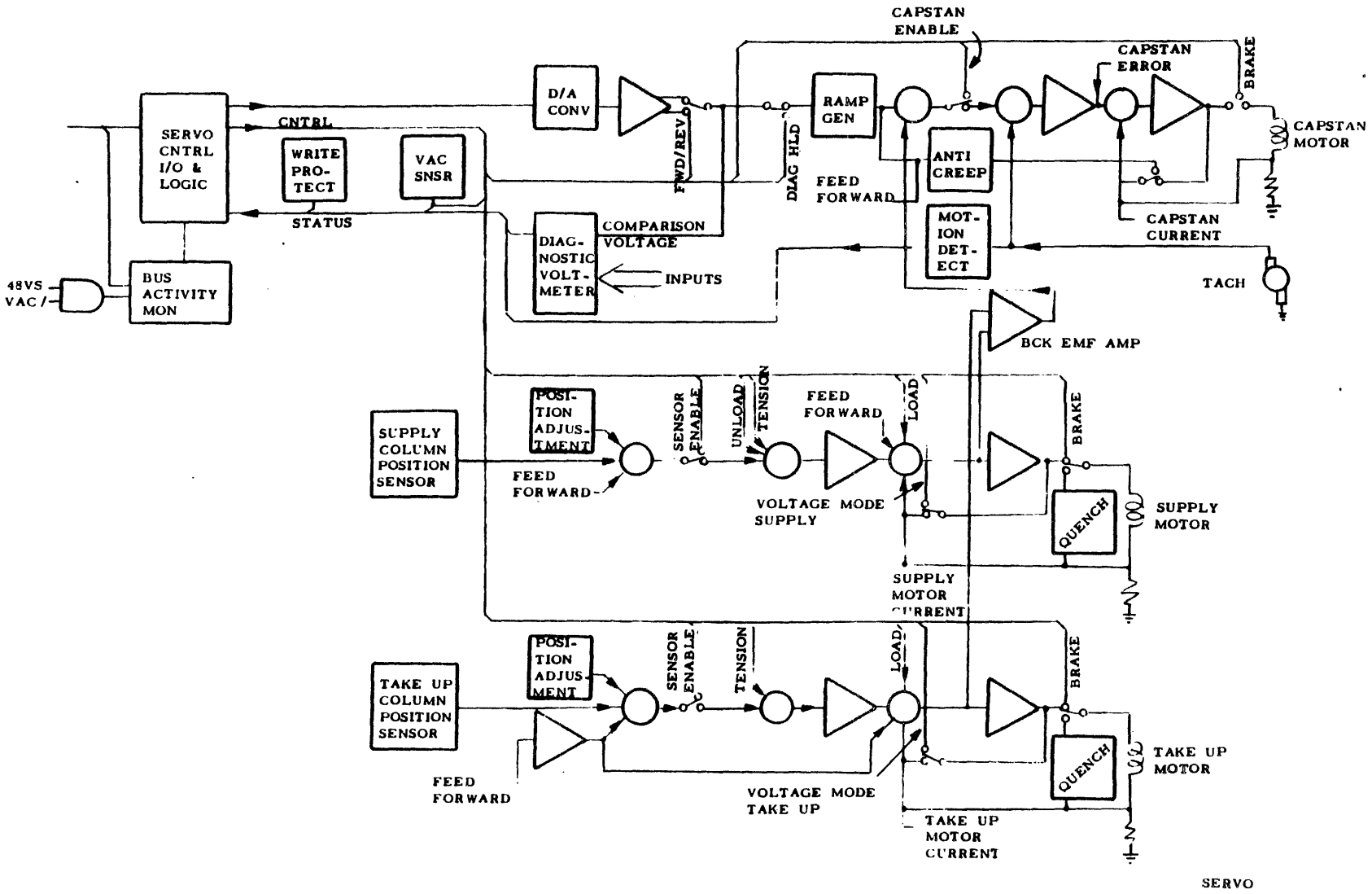
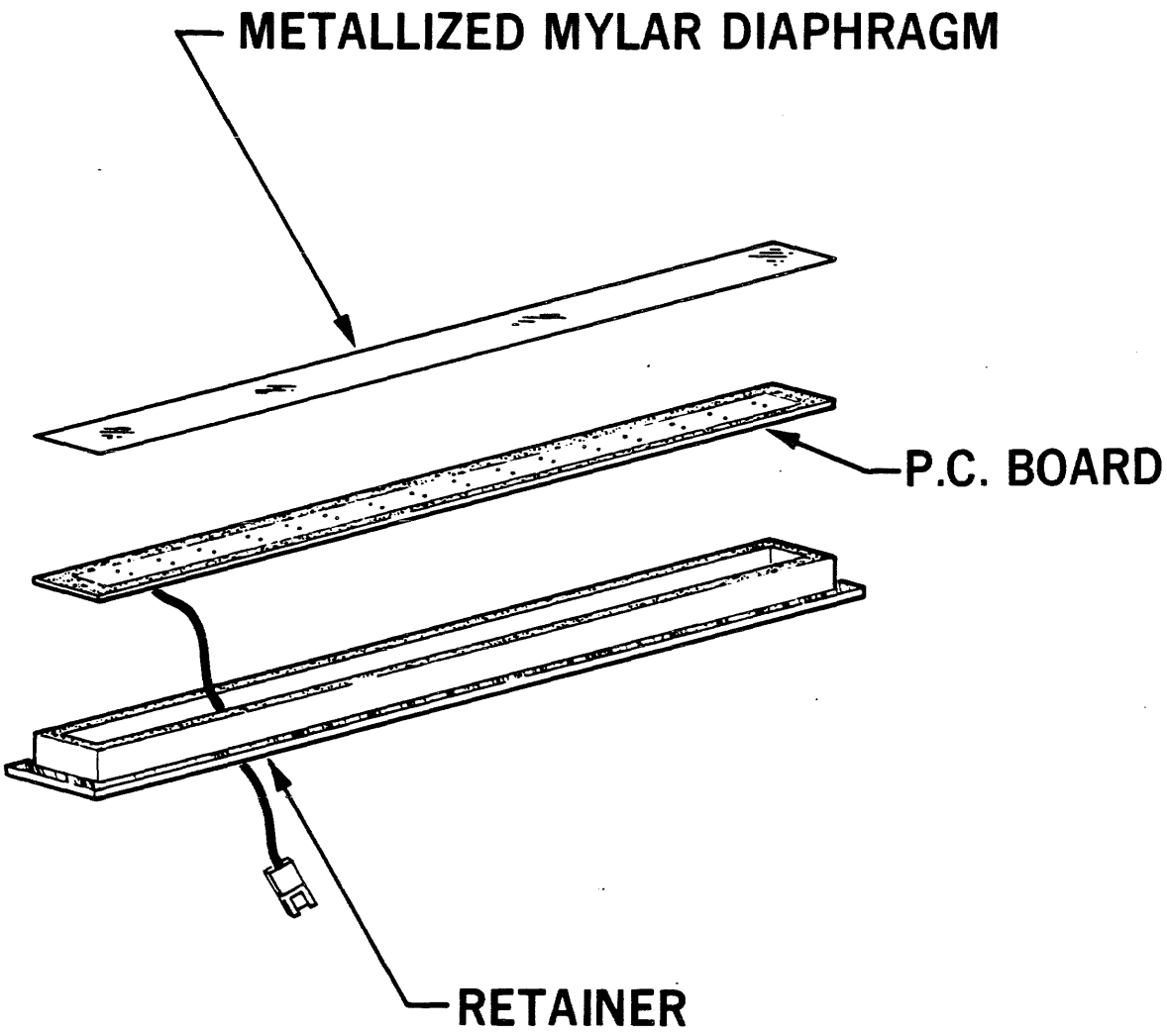


Figure 3-7

Servo/Tape Transport Block Diagram



110-0110

Figure 3-8
Vacuum Sensor Assembly

data. NRZ1 data is 9-track, 800 cpi (32 c/mm), compared to Phase Encoded (PE), which is 9-track, 1600 cpi (63 c/mm). A comparison of PE and NRZ1 formats is shown in figure 3.9.

In 9-track NRZ1 format (fig. 3.10) a Cyclic Redundancy Check Character (CRCC) is used within the block structure to provide error information for subsequent error correction. Vertical parity (excluding CRCC) in the 9-track format is always odd.

3.3.2 DATA

NRZ1 data is characterized as follows:

1) A '1' bit corresponds to a flux transition, of either polarity, in the center of the bit cell on tape. This corresponds to a logic true '1' on the WRITE DATA interface line to the transport during a Write operation.

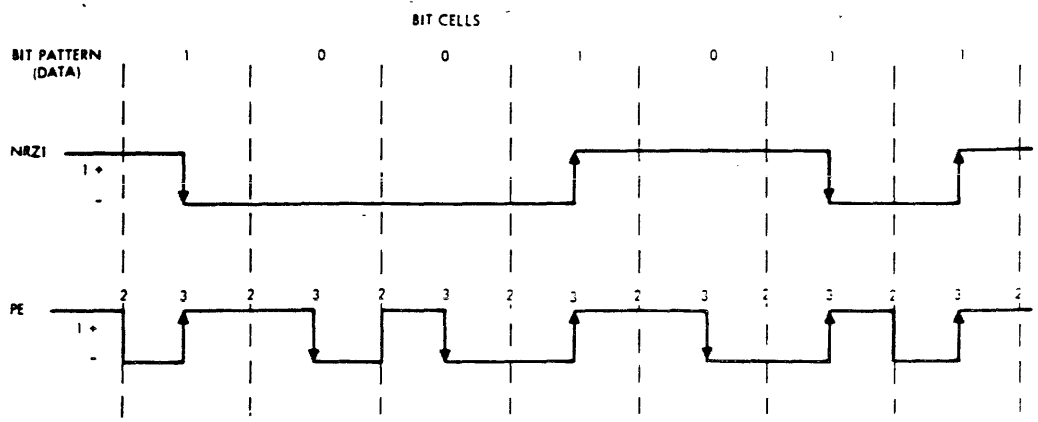
2) A '0' bit corresponds to the lack of a flux transition at the center of the bit cell on tape. This corresponds to a logic false '0' on the WRITE DATA interface line to the transport during a Write operation.

3.3.3 DATA RECORD

A record of NRZ1 data may contain between 18 and 2048 characters. This is in accordance with the ANSI Specification for 800 cpi NRZ1 recording. The 9400 is capable of reading or writing data records containing a minimum of one character (single character blocks are not recommended since a dropout may cause a single character block to be mistaken for a filemark). The firmware limitation to the maximum number of data characters that may be included in a record is 64K. Channel P on tape is written to provide odd parity for all data characters. Nominal spacing between characters is 1250 uinches (3175 um).

3.3.4 CYCLIC REDUNDANCY CHECK CHARACTER

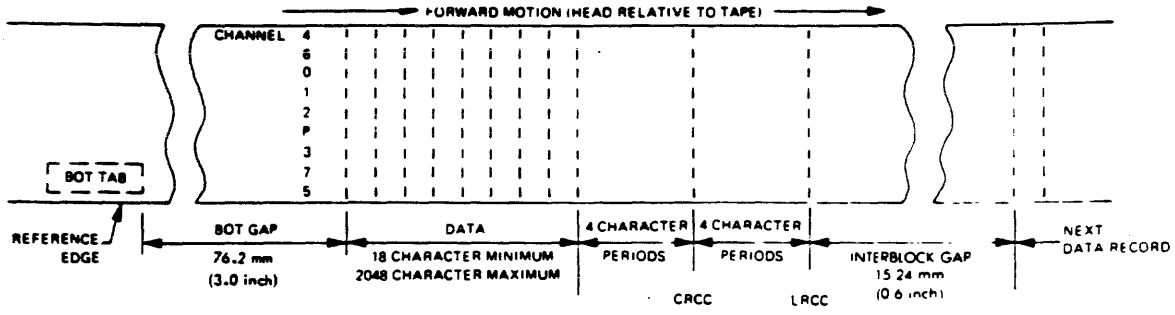
The Cyclic Redundancy Check Character (CRCC) is written on tape after a four character delay from the last data character. The CRCC is



1 FLUX POLARITY OF INTERBLOCK GAP
2 PHASE BIT SHIFT TIME
3 DATA BIT SHIFT TIME

Figure 3-9

NRZ1 & PE Comparison



NOTES:

1 TAPE SHOWN WITH OXIDE SIDE UP
2 CHANNELS 0—7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE
3 CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY (EXCEPT CRCC)
4 EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF 1 BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT, THE LRCC WILL NEVER BE AN ALL-0s CHARACTER
5 IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL 0s, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED
6 A FILE MARK IS A SINGLE CHARACTER RECORD HAVING 1 BITS IN CHANNELS 3, 6 AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL 0s. THIS RECORD IS SEPARATED BY 88.9 mm (3.5 inches) FROM THE PREVIOUS RECORD AND BY A NORMAL IBG (15.24 mm/0.6 inch) FROM THE FOLLOWING RECORD
7 DATA PACKING DENSITY IS FIXED AT 32 c/mm (800 cpi)

Figure 3-10

9-Track NRZ1 Format

generated in accordance with the ANSI Specification for 800 cpi NRZ1 magnetic tape recording.

3.3.5 LONGITUDINAL REDUNDANCY CHECK CHARACTER

The Longitudinal Redundancy Check Character (LRCC) is written on tape after a four character delay from the CRCC. The data in this character is such that the total number of '1' bits in a track (including the CRCC and LRCC) is even. The LRCC will never be an all '0's character. The LRCC is generated by the reset of the write register in the tape transport. The LRCC also serves to set the tape magnetization in the proper direction for the Inter Record Gap (IRG).

3.3.6 FILE MARK

When executing a Write File Mark command, the formatter generates a unique one-character record. This single data character consists of a '1' bit in Channels 3, 6, and 7 and a '0' bit in all other channels. The CRCC contains all '0's. The LRCC is equivalent to the single data character. Figure 3.11 illustrates the NRZ1 formats.

3.3.7 ERROR DETECTION

In the NRZ1 format, all deskewing functions during a read operation are performed in the tape transport. The 9400 receives a 9-bit word from the transport and relays this word to the customer's controller. A HARD ERROR (HER) is generated by the 9400 unit if any of the following read errors occur:

1) A data character is read from tape containing even parity.

2) A CRC error is detected. (The 9400 performs complete CRC checking; the received CRC must be exactly correct in all 9 bits).

3) Longitudinal parity on any track is odd.

4) A track dropout occurs in such a way as to cause more than two check characters, i.e., CRCC and LRCC, to be detected when the 9400 unit interprets the dropout as an end-of-record condition.

All of the foregoing errors except (4) are checked during both Read Forward and Read Reverse operations. The error described in (4) is checked only during Read Forward operations.

3.4 PHASE ENCODED (PE) FORMAT

The PE overall tape format is illustrated in figure 3.12. Portions of this format are discussed in paragraphs 3.4.1 and 3.4.2.

3.4.1 PE MODE DATA BLOCK FORMAT

Figure 3.13 details the format for the data block. The Preamble consists of 40 characters of '0's followed by a '1' character. A character is defined as nine bits in parallel, one bit per track (channel). The Postamble consists of a '1' character followed by 40 characters of '0's.

3.4.2 PE MODE TAPE MARK FORMAT

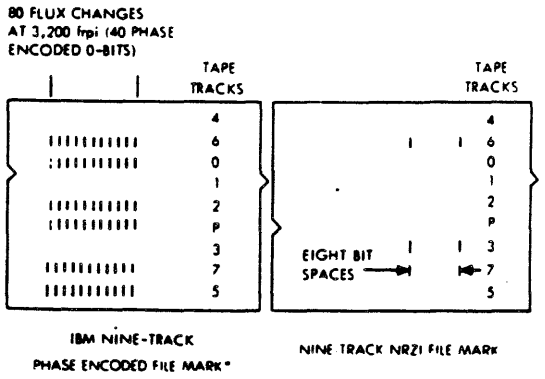
Figure 3.14 details the tape mark format used in PE mode. The tape mark is a special control block consisting of 64 to 256 flux reversals at 3200 flux reversals per inch (frpi) (126 fr/mm) in channels 2, 6, and 7. Channels 1, 3, and 4 are dc-erased. Channels 5, P, and 0, in any combination, may be dc-erased or recorded in the manner stated for channels 2, 6, and 7. The 9400 TTS system uses 80 flux reversals in a tape mark.

3.5 GROUP-CODED RECORDING (GCR) FORMAT

The recording format for GCR, operating at a character density of 6250 bpi, is described in the following text.

3.5.1 GCR OVERALL TAPE FORMAT

The Density Identification Area in the GCR recording format is



* ANSI SPECIFICATIONS DEFINE A FILE MARK AS A SPECIAL CONTROL BLOCK CONSISTING OF 64 TO 256 FLUX REVERSALS (AT 3200 frpi) IN CHANNELS 2, 6 AND 7. CHANNELS 1,3 AND 4 ARE DC ERASED. CHANNELS P, O AND 5 (IN ANY COMBINATION) MAY BE DC ERASED OR RECORDED IN THE MANNER STATED FOR CHANNELS 2, 6 AND 7.

Figure 3-11

NRZ1 File Mark

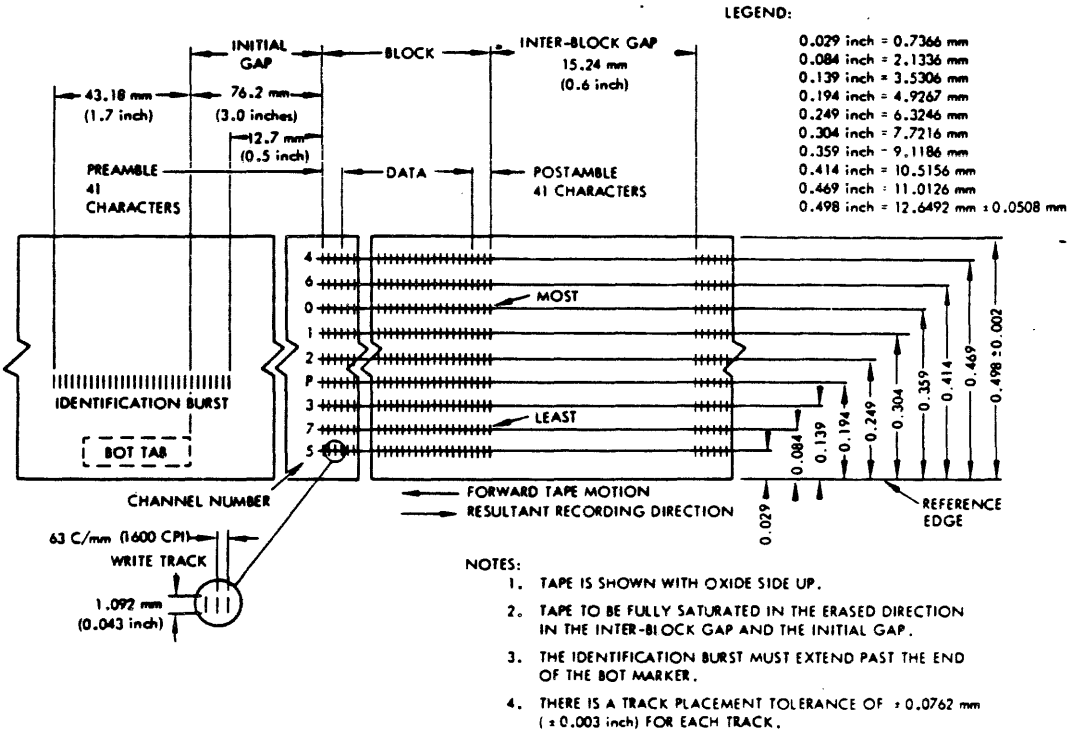


Figure 3-12

PE Tape Format

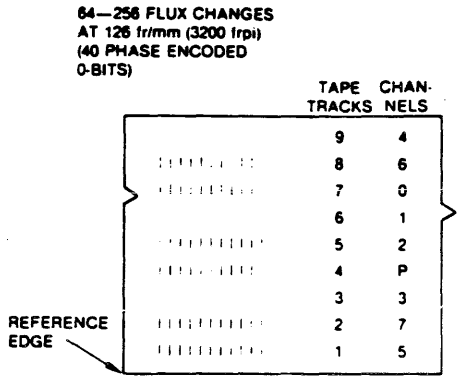
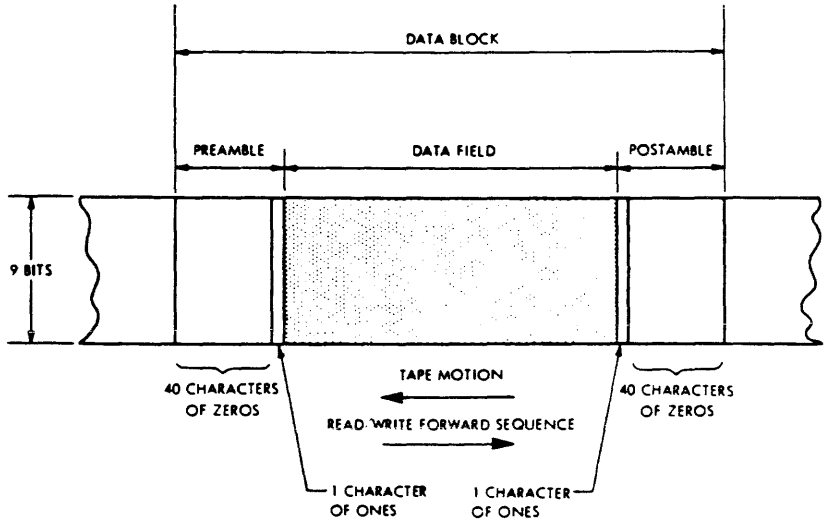


Figure 3-13

PE Data Block Format



NOTE: A CHARACTER IS NINE PARALLEL BITS, ONE BIT ON EACH OF THE TRACKS.

Figure 3-14

PE Tape Mark Format

identified by a burst of the recording at the BOT marker (fig.3.15). This burst is in the PE frequency range on channel 1, with erasure on all other tracks. The ID burst begins 1.7 inches (43.18 mm) minimum before the trailing edge of the BOT marker and continues past the trailing edge of the BOT marker.

The Automatic Read Amplification (ARA) burst, immediately following the ID burst, consists of all tracks, separated from the ID burst by an undefined gap. The burst of '1's is placed as follows: It begins no sooner than 11.5 inches (38.1 mm), as measured from the leading edge of the BOT marker.

Appended to the end of the '1's burst is an ARA ID burst consisting of '1's in channels 7, 3, 2, 1, 6, and 4, and dc-erasure in channels 5, P, and 0. This ID Burst is approximately 2 inches (50.8 mm) long (at least a contiguous 0.25 inch [6.35 mm] of this length must be error-free in all tracks at once). There is a nominal inter-block gap (IBG) between the ARA ID burst and the first data block.

3.5.2 GCR MODE TAPE MARK FORMAT

Figure 3.16 details the tape mark format used in GCR mode to mark the end of a file. The tape mark is a special block generated in response to the Write Tape Mark GCR command.

The tape mark is specified as 250 to 400 flux reversals, all '1's at 9042 frpi (356 fr/mm) in channels 7, 2, 6, 5, P, 0, and dc-erasure in channels 3, 1, and 4.

NOTE: The flux reversal rate of 9042 frpi is equal to the number of bit cells per inch. This accommodates data, encoding, error checking, and other overhead requirements. The data density is 6250 cpi.

3.5.3 GCR DATA BLOCK FORMAT

3.5.3.1 PREAMBLE

Each block of data is preceded by a preamble for synchronization purposes. The preamble, as recorded, consists of 80 characters, divided into five 16-character subgroups, one Terminator Control Subgroup, one Second Control Subgroup, and 14 Sync Control Subgroups (fig. 3.17).

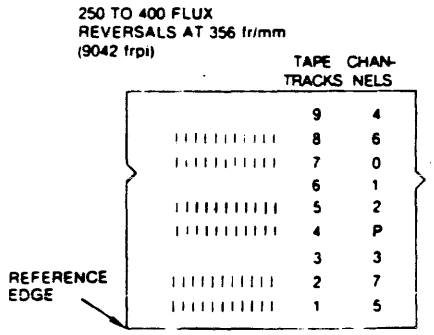
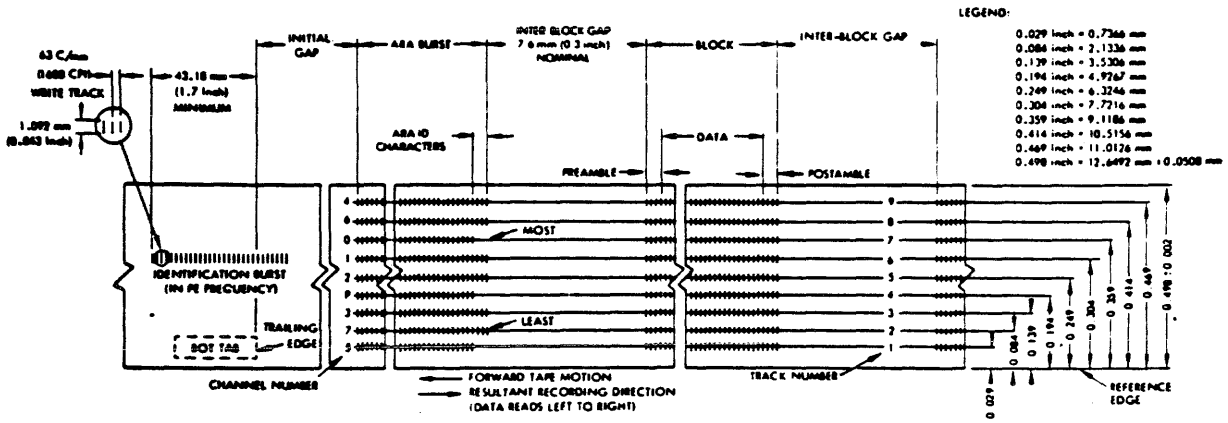


Figure 3-15

GCR Overall Tape Format

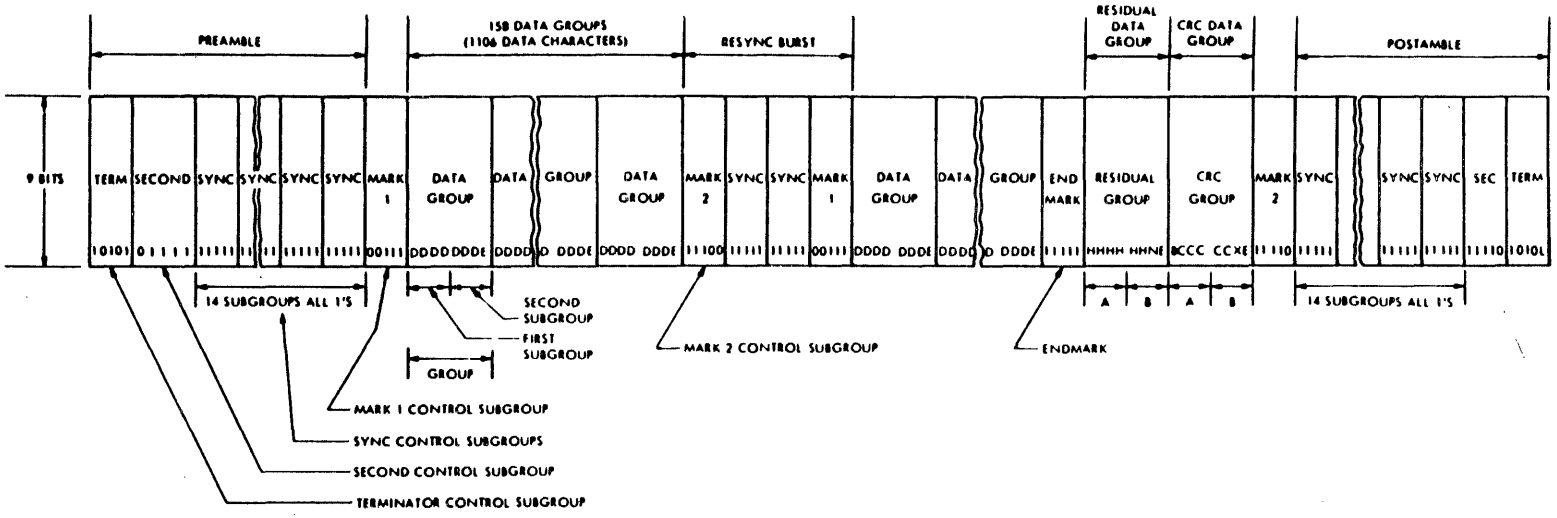


NOTES:

1. TAPE IS SHOWN WITH OXIDE SIDE UP.
2. TAPE TO BE FULLY SATURATED IN THE ERASED DIRECTION IN THE INTER-BLOCK GAP AND THE INITIAL GAP.
3. THE IDENTIFICATION BURST MUST EXTEND PAST THE END OF THE BOT MARKER.
4. THERE IS A TRACK PLACEMENT TOLERANCE OF ±0.0762 mm (±0.003 inch) FOR EACH TRACK.

Figure 3-16

GCR Tape Mark Format



NOTE: DATA, RESIDUAL AND GCR GROUPS ARE TRANSLATED FROM 8-BYTE TO 10-BYTE CODES BEFORE THEY ARE SENT TO THE TRANSPORT FOR RECORDING ON TAPE.

Figure 3-17

GCR Data Block Format

1) The Terminator Control Subgroup (TERM) is one set of nine parallel 8-bit serial values of 1Ø1Ø1 in the respective tracks for the BOT end of each block and 1Ø1ØL, the EOT end of each block, where L represents even logitudinal parity. The L bit of the last character restores the magnetic remanence to the erase state.

2) The Second Control Subgroup is one set of nine parallel 5-bit serial values of Ø1111 in the respective tracks for the BOT end of the block and 11110 for the EOT end of the block interleaved between the respective Terminator Control Subgroups and the Sync Control Subgroups.

3) The Sync Control Subgroup is one set of nine parallel 5-bit serial values, 11111 in the respective tracks. It is used to indicate recorded frequency and phase to allow synchronization of the Variable Frequency Clock (VFC).

3.5.3.2 MARK1 CONTROL SUBGROUP

This subgroup is one set of 5-bit serial values (ØØ111) in each of the nine parallel tracks simultaneously. Mark1 delineates the boundary between control subgroups and data. When the tape moves in the forward direction, Mark1 indicates that data will follow.

3.5.3.3 DATA GROUP

A Data Group is an essential element of Group Code Recording. Before encoding it develops as seven data characters. An error correction character plus a parity channel are mathematically determined and add to the data to form a GCR codeword (fig. 3.18). Each of these codewords are divided into two data subgroups (fig. 3.19) and converted to a storage subgroup according to fig. 3.2Ø. The storage subgroups are then rejoined and written to tape in a 1Ø byte recording group.

3.5.3.4 RESYNCHRONIZATION BURST

After each 158 data groups (11Ø6 data characters as calculated in data-group format), a resync burst, consisting of a Mark2 Control Subgroup, two Sync Control Subgroups and one Mark1 subgroup, is generated. The Sync Control Subgroups are formatted as described in

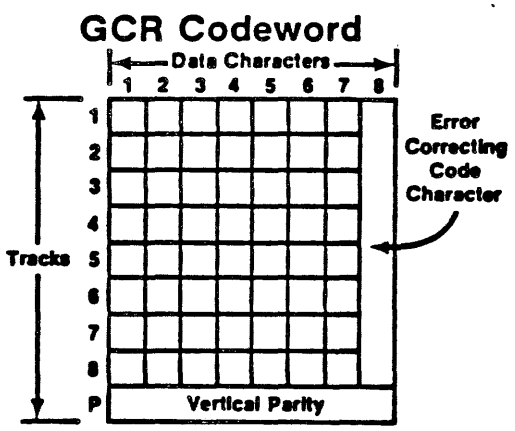


Figure 3-18
GCR Code Word

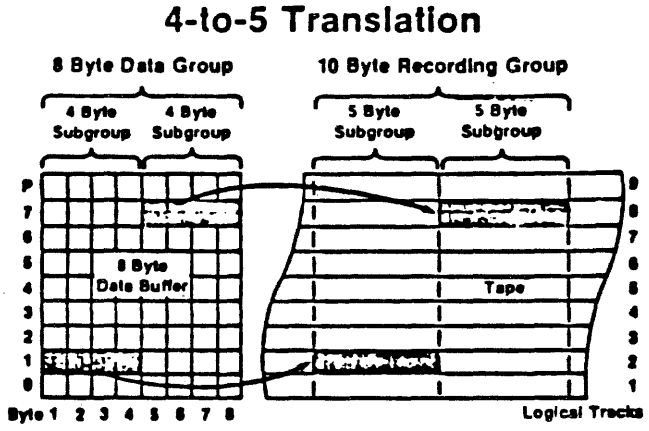


Figure 3-19
4-to-5 Translation

Data Subgroup to Storage Subgroup Conversion

DATA	STORAGE
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

Figure 3-20

Data Subgroup to Storage Subgroup Conversion

paragraphs 3.5.3.1. The Mark2 Subgroup that ends the 158 data group series is the same as Mark1 (refer to 3.5.3.2) except that the 5-bit serial value is 11100. The Mark1 Subgroup indicates the end of the sync burst, as described in 3.5.3.2.

3.5.3.5 END MARK CONTROL SUBGROUP

The End Mark is used to indicate the end of a series of complete data groups, and the beginning of the Residual Data Group. The End Mark is one set of nine parallel 5-bit serial numbers (11111) in each of the tracks.

3.5.3.6 RESIDUAL DATA GROUP

The Residual Data Group positions are as follows:

1) Group positions 1-6 contain residual data characters or padding, i.e., the remainder of the number of characters divided by 7.

2) Group position 7 contains an auxiliary CRC character (N).

3) Group position 8 contains an ECC character (E).

The residual data characters occupy the lower-numbered positions, with the high numbered group positions containing padding characters of all 0s with odd parity. The group positions 1-6 may contain all padding or all data characters in accordance with the number of residual characters modulo 7.

3.5.3.7 CRC DATA GROUP

This specially formatted data group contains the CRC character and the residual character. The group positions are as follows:

1) Group position 1 contains an all '0's character with odd parity or the CRC character (b).

2) Group positions 2-6 each contain the CRC character (C).

3) Group position 7 contains the residual character (X).

4) Group position 8 contains the ECC character (E).

3.5.3.8 POSTAMBLE

The postamble follows the CRC group and a Mark2 Subgroup, which is the same as Mark1, except that the 5-bit serial value is 11100. The postamble consists of 80 characters of which the first 14 subgroups are all '1's in all tracks followed by 11110 and 1010L in all tracks (the L character is the last character, and is recorded to restore the residual magnetism of the tape to the IRG polarity). The postamble is recorded for the purpose of electronic synchronization in reverse reading mode.

3.6 SYSTEM PROCESSOR DETAILED DESCRIPTION

The System Processor is a bus oriented, memory mapped architecture. There is a System Address bus, System Data bus, System Decoded Address bus (MAP) derived from the System Address bus, and an Interrupt Request bus.

IC93 (8088), the main CPU, receives a 5MHZ System Clock from the Clock Generator, IC88 (8284A). The Clock Generator also supplies a 2.5MHZ (PCLK) Peripheral Clock, and a 15MHZ FIFO Input Clock (FIN) as well as controlling the READY and RESET lines of the main CPU. The Clock Generators' RDY1 and RDY2 lines are synchronized to the READY line of the CPU. The lower address/data lines are buffered by octal bus transceiver IC119. Memory mapped address decoding is achieved through Programmable Array Logic (PAL) IC's 75 & 81 and ICs' 55, 63, 64, 69, 70, 76, 104 and 110 which are utilized as decoders.

3.6.1 ROM/RAM

Operating system storage is provided through four 4K-byte EPROMs (ICs' 86,94,106 and 116) beginning at address 0000H. Two 2K by 8 RAMs (ICs' 105 and 115) provide stack and storage space beginning at location 8000H. Additionally, a 2K by 8 CMOS RAM with a battery power supply provides non-volatile storage. Power-up/reset, diagnotics and program initialization is accomplished by a 512 by 8 boot ROM (IC111) located at the upper most memory block. Upon power-up/reset, the internal registers and flags of the CPU are cleared with the exception of the Code Segment (CS) register, which is set to all ones (FFFFH). This

causes program execution to begin at FFFFØH which is occupied by the boot Prom.

3.6.2 TIMING CONTROL

Tape movement timing control is provided by two Programmable Interval Timers (IC74 and IC8Ø, timer Ø and 1 respectively) which prescale the 2.5MHZ PCLK to a usable timing range from 8ØØ nanoseconds to 1718 seconds. Each timer contains three independently programmable counters. Counter 1 is used as a pre-scaler for counter 2. Counter 2 disables counter 1 after the terminal count, until the counter is restarted. Counter 3 provides transmit/receive clock to the Programmmable Communication Interface (IC132) which provides the baud rate to the RS232-C port. Counter 4 acts as a system watchdog counter. Counter 5 is utilized as a host data rate clock and is also tied to the clock of counter 6. Counter 6 is used as a secondary programmable system counter and is also used as interrupt 15.

3.6.3 INTERRUPTS

Two Programmable Interrupt Controllers, IC73 & IC79 (8259A), arbitrate and mask interrupts from various devices. IC79 is a slave to IC73. A maximum of 15 interrupts can be realized from the interrupt controllers. Presently, 13 interrupts are utilized as follows:

1) AC FAIL: The highest priority is given to a Non Maskable Interrupt (NMI) dedicated for power failure. This interrupt is asserted whenever the input AC line from the power supply drops below a preset threshold level. Upon initiation of the NMI, the servo system is disabled, switching the reel servo motors over to the braking circuit which stops the tape if in motion. The processor is then placed in the HALT mode to prevent it from attempting any further action until power is restored. This is the only interrupt which is not prioritized by the interrupt controllers.

2) FAULT: The system FAULT interrupt indicates a possible catastrophic system failure such as a Servo Power, Broken tape or Vacuum failure. A FAULT will cause all tape motion to cease immediately, followed by an indication on the Fault LED. The system is placed off line and any command sequences are terminated. This interrupt is enabled when tape is loaded.

3) RTIME: A watchdog timer interrupt.

4) HOST: A preassigned interrupt dependent upon the host interface.

a) Pertec- Reset for FORMATTER ENABLE/

5) TIMER: This general purpose interrupt resets the Timer Flag which was set by the routine which initiated the timer. The interrupt request is cleared and the timer is disabled. The Timer flag is reset to indicate that the timer is finished.

6) SENSOR: the position sensor interrupt is used to set/reset the Load Point (LPT) and End Of Tape (EOT) flags. If the system is off line, EOT causes tape motion to cease (front panel motion commands are invalid after EOT). If LPT is encountered during a high speed rewind, tape ramps down slowly and then searches forward at 75 ips for the LPT marker. This interrupt is enabled only when tape is loaded.

7) DONE: This interrupt is generated by the Write Data Handler after completion of the command given to it.

8) HOST2: A preassigned interrupt dependent upon the host interface.

a) Pertec- Command other than Rewind or Offline

9) SWITCH: This interrupt is used to set various flags (mode, Unit Address and On Line) and/or to initiate various operations (Rewind, Load/Unload, servo exercise and power shut-down).

10) HOST3: A preassigned interrupt dependent upon the host interface.

a) Pertec- a Rewind or Offline command

11) RXRDY: This interrupt, which is output from the Programmable Communication Interface IC132 (8251A) causes the next location in the 256 byte recirculating transmitter and receiver buffers to be filled with the received byte. If the receiver buffer is full (read pointer just below the write pointer), the byte is not stored and a control 'G' character (BELL) is placed in the transmitter buffer. The interrupt is then disabled until at least one byte is read from the buffer.

12) TXRDY: This is a transmitter empty interrupt from the Programmable Communication Interface. The interrupt causes the next location in the recirculating transmitter buffer to be output. If the buffer is empty (read pointer equals write pointer), the interrupt is disabled until another character is deposited in the buffer.

13) UPDATE: This is a timer interrupt from counter 6.

The NMI address is at location 08H. The other interrupts exist in a vector table starting at location 20H.

3.6.4 SUBSYSTEM MEMORY MAP & SYSTEM CONTROL

Communication between the processor and the subsystems of the 9400 is a function of the commands from the processor and the information on the status lines. Each subsystem lies in a memory mapped block of 32 bytes which the System Processor decodes and sets the corresponding subsystem select line true. Each subsystem then does additional decoding of the address lines to obtain the individual command and status latches it requires. This section defines the commands and status for the block defining the System Control. Command and status definitions for the other subsystems will be found in the individual write-ups of each subsystem. The subsystem blocks along with there absolute memory locations are as follows:

Subsystem Memory Map

Hex Address range	Subsystem
F800 - F81F	Write Data Handler
F820 - F83F	Front Panel
F840 - F85F	Analog Read/Write Amps
F860 - F87F	System Control
F880 - F89F	Reserved
F8A0 - F8BF	Read Decoders
F8C0 - F8DF	Read Data Handler
F8E0 - F8FF	Servo

3.6.4.1 SYSTEM CONTROL

This block contains registers and latches allowing the system processor to control and keep tabs on the First-In-First-Out (FIFO) buffer, power supply, cable monitors, diagnostic control, and the tape markers. These registers are mapped as follows:

HEX ADDRESS	WRITE	READ
0F860	Power Supply Control	Tape Marker Sensors
0F861	FIFO Control	Cable Monitor Check
0F862	Status LEDs	Diagnostic Switches
0F863	Write byte to FIFO	Read byte from FIFO
0F864	Write FIFO count LSB	Read FIFO count LSB
0F865	Write FIFO count MSB	Read FIFO count MSB

1) Write Byte to FIFO: If FIFO in-rdy is true and the FIFO control register is set to allow system data into the FIFO, a write to this address will be put into the FIFO. This is useful for testing the FIFO.

2) Read Byte from FIFO: If FIFO out-rdy is true and the FIFO control register is set to allow data to be read out by the system, a read from this address will read one byte out of the FIFO.

3) FIFO count LSB: A read from this address will give the least significant byte of the 16 bit counter that is monitoring the FIFO. A write will load a value to this counter.

4) FIFO count MSB: A read of this address will give the most significant byte of the FIFO counter. A write will load a value to this counter.

3.6.4.2 POWER SUPPLY CONTROL

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FIFO reset	FIFO clear	FIFO mode		System enable		Vacuum enable	Fast

Fast — Sets servo power supply from 24 volts to 48 volts.

Vacuum enable — Turns on vacuum blower.

System enable — By-passes AC power switch to leave power on while the tape is unloaded.

FIFO mode — When true, data shifted into the FIFO will not increment the byte counter (diagnostic).

FIFO clear — Active low. Clears the FIFO address and byte counters.

FIFO reset — Active low. Initializes handshake flops and holds the phase counter. This bit must be low to load the byte counter.

3.6.4.3 TAPE SENSOR REGISTER

The Tape Sensor Register, the input port to read the tape sensors, gives the System Processor access to the FIFO full and output ready flag.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				FIFO OUTRDY	FIFO FULL	EOT	LDP

3.6.4.4 FIFO CONTROL REGISTER AND BUFFER

The System Processor must have control over which subsystem writes to and reads from the FIFO data buffer. This register handles this function. The least significant nibble is data input to the FIFO; while the most significant nibble is data output from the FIFO. Bit 6 must be set when reading NRZ1 data on systems with the PERTEC interface. This will cause the Read data to by-pass the FIFO and be fed real-time to the host.

LSB

0	System data bus	INPUT
1	Read Data from Read Data Handler	TO
2	Write Data from Host I/0	FIFO
3	Write Data Handler output data	

4	System Data bus	OUTPUT
5	Read Data to Host I/O	FROM
6	Write Data to Write Data Handler	FIFO
7	Loop	

MSB

The FIFO data path control is achieved through line receivers, ICs 51, 52, 53, 59, 60, 61 and octal D-flops ICs 62 and 78. The FIFO buffer itself consists of eight 2kbyte ram chips (ICs 66, 77, 99, 100, 112, 113, 122, 138). Read Data (RD0-RD7) from the Read Data Handler enters the FIFO through IC59. Interface Data (I00-I07) from the Host Interface enters through IC60. Data from the System Processor Bidirectional Data bus (BD0-BD7) enters through IC61. Control latch IC62 determines what type of data enters the FIFO. Address generation is accomplished through three sets of cascaded counters (LS569). ICs 95, 101, 96 and 102 form the content address counter and keeps track of how many bytes are in the FIFO. ICs 130, 123, 117, and 108 form the Read Address counter while ICs 131, 124, 118 and 109 form the Write Address counter. IC107 is used as a wrap around latch and activates the Synchronous Clear (SCLR/) of the Read and Write Address counters.

3.6.4.5 CABLE MONITOR REGISTER

The system has a port to read the cable monitors on all flat cables it uses. Reading a 00H byte from this port indicates all cables are in place.

LSB	0	Interface cable to Analog Read/Write Amps
	1	Interface cable to Front Panel
	2	Read data cable
	3	Interface cable to Power Supply
	4	Write data cable
	5	Interface cable to Servo
	6	Interface cable to Read Data Decoders
MSB	7	Interface cable to Read Data Handler

3.6.4.6 STATUS LEDS

There is a bank of 8 LEDs for use by the System Processor. The lower four LEDs represents the most significant binary weighted hex digit, while the upper four LEDs represents the least significant binary weighted hex digit. The LEDs provide an alternate display for diagnostic codes. The codes displayed on the LEDs are listed in section 4.20.1.

3.6.4.7 DIAGNOSTIC SWITCHES

An 8 position dip switch (SW2) located on the System Processor board is utilized to program certain features of the diagnostic software. The switch configuration is discussed in section 4.19.

3.6.5 SERIAL INTERFACE

IC132 (8251A), a Programmable Communications Interface, provides a means of communication with a standard CRT terminal for diagnostics. ICs 141 and 142 are line receivers and drivers, respectively, providing RS-232-C level translation through a standard 25 pin interface connector. A jumper block (ST37) configures the port to appear as Data Terminal Equipment (DTE).

DATA TERMINAL EQUIPMENT (DTE) TABLE

JUMPER:	J20 PIN:	FUNCTION
17 - 18:	2	RX DATA
1 - 2 :	3	TX DATA
9 - 10:	6	DTR
8 - 11:	20	DSR
13 - 14:	N/A	RTS - CTS (LOOP-BACK)

DATA COMMUNICATIONS EQUIPMENT (DCE) TABLE

JUMPER:	J20 PIN:	FUNCTION
1 - 18:	2	TX DATA
2 - 17:	3	RX DATA
4 - 5 :	4	RTS
14 - 15:	5	CTS
7 - 8 :	20	DTR
11 - 12:	6	DSR

3.6.6 SUBSYSTEM INTERFACING

The System Processor interfaces by cable with the other subsystems through bus transceivers (LS245) or inverter buffer drivers (7406). There are 11 electrical connections on the microprocessor board. All connectors are designated by 'J' with the exception of the two host interface connectors P1 and P2.

System Processor Connector	Interfaces
J11	To Analog Rd/Wrt & Keyboard
J5	From Read Handler
J9	To Analog Rd/Wrt
J21	From Vacuum Switch
J22	From BOT/EOT Sensor Assembly
J13	To Power Supply Interface
J3	From Power Supply
P1 & P2	To Host Interface
J4	To Read Handler & Read Decoder II
J20	RS-232 port

3.6.7 WRITE DATA HANDLER

The Write Data Handler resides on the same board as the System Microprocessor. The command register is mapped at address F800H. The sequential command set is as follows:

Command (Hex)	Description
35	Write file mark, NRZ
34	Write one data block, NRZ
B8	Write ID burst, PE
00	Stop writing ID burst, PE
39	Write file mark, PE
38	Write one data block, PE
BC	Write ID burst, GCR
AC	Write ARA burst, GCR
BC	Write ARA ID burst, GCR
00	Stop Writing ARA ID burst, GCR
3D	Write file mark, GCR
3C	Write one data block, GCR

The Write Handler Processor consists of an Am2910 sequencer (IC21), a 32-bit-wide control store memory, and an Arithmetic/Logic Unit built with two Am2903 four-bit slices (ICs 7 & 18). The ALU also includes a one-bit 'parity ALU'(built from a PROM (IC25) and an Am29705 dual-port RAM (IC1)) and logic for generating CRC and ACRC characters. The parity ALU normally operates in a closed loop. Its only source of input data is the parity output of the 2903's, which is written to the parity ALU by the INPT instruction.

CRC and ACRC generation is accomplished by an algorithm which involves bit swapping and modulo 2 addition. External registers, ICs 6 & 12, accumulate CRC and ACRC data.

The first task performed by the write data generator is the generation of the preamble and MARK1 group. While the MARK1 group is being written the first data group is being input.

Data is input to the write data generator from the system processor FIFO buffer in groups of seven bytes. The time interval between bytes in the group is equal to one data cell, or 2.45 microseconds in GCR mode at 45 ips. Between each burst of seven data strobes, there is a 3 cell interval of no strobes. The Error Correcting Code is computed on the incoming data as well as the Auxiliary CRC, CRCC, Modulo 7 count and Modulo 32 count. Once 7 bytes have collected and the ECC generated, the first 4 bytes are encoded to 5 bytes. Then the last 3 bytes and ECC are encoded as 5 bytes. Data is input until no more data is available from the host. To complete the GCR data block, the processor calculates the number of pad characters required, completes computation of ACRC and CRC, and formats the Modulo 7 and Modulo 32 counts. The END MARK, RESIDUAL, and CRC groups are then written, followed by the MARK2 group and postamble.

3.7 FRONT PANEL KEYBOARD

The Front Panel Keyboard consists of a Keyboard Decoder and Keyboard. The Keyboard Decoder is interfaced with the System Processor through bus transceivers IC1 and IC2 via cable J11. IC2 is configured in a unidirectional mode while IC1 is bidirectional at the processor's command. IC3, a Programmable Keyboard/Display I/O interface, is responsible for decoding switch selection and generating the Keyboard interrupt (Kint/) to the processor. Q1 - Q8 supplies the drive current to all of the LEDs and displays while IC5 and 6 sinks the current.

3.8 ANALOG READ/WRITE AMPS

The Analog Read/Write circuitry interfaces with the System Processor through cable J11, bus transceivers IC9 & IC1Ø, and a Programmable Peripheral Interface IC8. IC1Ø is configured as an A to B bus receiver while IC9 is bidirectional depending on the status of KRD/ & KAMPS/. KAØ & KA1 selects one of the three ports of PPI IC8 while KRD/, KWRT/, and KAMPS/ determines the direction of data flow and whether the PPI is enabled.

3.8.1 PORT DESCRIPTION

Port A of IC8 is programmed as an output and determines the DAC input word. The actual value of the DAC sink current can be determined by the following formula:

$$\text{Total DAC Sink Current (A)} = \frac{(\text{Decimal value of DAC input Word}) * 5.0}{256 * R84(\text{ohms})}$$

Each track of the Read/Write board receives approximately one ninth of this current for use in developing a fixed threshold voltage.

Port B is programmed as a dedicated output port which controls the following functions:

Port

B1: controls the loop write to read diagnostic function. A logic high at this port indicates a loop read to write operation.

B2: Envelope Enable. A logic low forces all read data to appear at the digital output. A logic high permits the envelope detector to determine whether data is output or not for each read channel.

B3: AGC drive enable. A logic low from this port drives darlington pair Q27 and Q28 on to provide 5 volts for use by the peak detectors. Diode CR6 provides a discharge path for filter capacitor C16.

B4: FWD/REV Equalization. This permits compensation of the delay equalizer for changes in tape direction. A logic low at this port permits correct equalization for reading data in reverse.

B5: NRZ1 Select. This modifies the read equalization for NRZ1 operation. A low at this port produces NRZ1 equalization by driving Q25 on, which in turn biases QX09 and QX10 on.

B6: Diagnostic Enable. This is the read data input diagnostic enable. A logic high is coupled through buffer IC11 to gates ICX01 on each of the read channels. Write data present at ICX01 is then permitted to appear at CX09, the diagnostic data injection point.

B7: A logic low signal at this port drives Q26 on, which reverse biases CR1, permitting QX05 to turn on in all tracks. An adjustable divider is formed by RX20, RX21 and RX22, reducing the gain 5-10 times.

Port C is configured with bits C0-C3 as outputs and bits C6-C7 as inputs and control the following:

Ports

C0: Write Enable/. This signal, acting through Q21, turns on write current to the write head. The turn-on and turn-off rates are controlled to prevent extra transitions from being written accidentally.

C1: Phase Encode/. Buffered through IC2, this signal turns Q20 on and provides PE levels of write current.

C2: NRZ/. This signal turns Q19 on via IC2 and provides NRZ1 write current. With NRZ1 enabled, the PE command for write current is disregarded.

C3: ERASE/. This signal enables the full width erase head.

C6: ERASE DIAGNOSTIC. This diagnostic port monitors the erase head. A logic high indicates the erase head is on.

C7: WRITE DIAGNOSTIC. This diagnostic port monitors the write head by noting the state of a comparator sensing the voltage across the write head current sense resistor, R64. A logic low generally indicates a fault in the write or read head.

The remaining ports on IC8 are not utilized. The base address of IC8 is 0F840H.

3.8.2 . WRITE DRIVE CIRCUITRY

The write head is a center-tapped bifilar type with the center tap common to all channels. It connects to the Analog Read/Write board through connector J7 and the read pre-amp. The erase head is also driven through J7.

GCR encoded data is inputted from the processor board through J9. After buffering from IC1 & IC5, the write data is applied to IC2-IC4. IC2-IC4 are low skew gates with complimentary outputs and enable clean transitions to be written at any density. Switched current source pairs Q1-Q2, Q3-Q4, etc., drive the write head directly, with the value of the write current inversely proportional to the value of resistance of the common emitters pulled up to the +5 volt supply. Resistors R1-R2, R7-R8, etc., serve to isolate the logic from the head drive circuit and produce only a slight voltage drop under normal operation. Switches Q19 and Q20 apply 5 volt power to R3-R9-R15 etc. and R4-R10-R16 etc. respectively, thus varying the emitter resistance of the current source pairs and, as a result, the write current. GCR write current is established by R6-R12-R18 etc., and potentiometers R5-R11-R17 etc. The GCR write current is increased to PE levels when switch Q20 is on. PE write current is increased to NRZ1 levels when switch Q19 is on. These switches are controlled by the processor board via IC8 and IC2.

Write drive is enabled by switch Q22 and Q21, which are driven by IC8. Components R62, R63, R64, C3 and CR3 provide a controlled rate of current change during write current disable and enable. This avoids the problem of extraneous transitions being written during write operations. Resistor R64 also provides a voltage drop to the head center tap to prevent overheating of the switched current source pairs during NRZI mode writing.

The voltage across R64 is also applied to window comparator IC13 for write diagnostics. The allowable sense voltage at this point is determined by R6A, R5A, R99, R1A, R2A and switches Q31 and Q32. Q31 and Q32 are driven by the PE and NRZ1 control lines, respectively, thereby producing window voltages appropriate for the different densities. C33 and R94 permit small, rapid variations in the write current (such as that caused by an open head or cable) to be detected at the input of IC13. R7A, R10A and C32 act in conjunction with the open collector output of IC13 to produce the pulse stretcher necessary for the processor board to detect brief faults in write current through the interface chip IC8. Q33 disables the higher write fault threshold with write current off completely to provide "write protect" confirmation through the PPI IC8.

The erase head is driven by switch Q23, which is also monitored by the PPI. R67 and C5 provide controlled erase current rise and fall times to prevent erroneous transitions from being written while switching erase current on or off. CR4 absorbs any erase head flyback voltage.

3.8.3 READ AMPLIFIER AND DETECTOR CIRCUITRY

The basic read amplifier consists of ICX03 and related components. Differential read data from the read head preamp is routed to RX21 and RX20 through connector J6. In the low gain mode, QX05 is on due to the presence of approximately zero volts at the gate through RX23. The divider formed by RX20, RX21 and RX22 attenuates the input signal by a factor of 5 to 10, with RX22 serving to adjust the signal level into ICX03. The gain and frequency response characteristics of ICX03 are set by RX29, RX30, CX10, LX02 and, when switch QX10 is closed, RX43. Due to delay distortion caused by this frequency equalizer and the read/write process itself, a delay equalizer consisting of RX32, CX14 and, with switch QX06 closed, CX15, has been incorporated. The fully compensated signal is present at the junction of RX32 and CX14 and is buffered by QX07. RX33 in the collector of emitter follower QX07 prevents spurious oscillations.

3.8.4 FILTER CIRCUITRY

A Bessel filter consisting of CX16, CX17, RX35 and LX04 removes noise from the read signal without affecting the waveshape. The filter is single ended with unity gain and is buffered by QX08. The output of this emitter follower drives the passive differentiator and the threshold detector and has the test point designation ADATA.N.

3.8.5 PEAK DETECTOR CIRCUITRY

The analog data contains the recorded information at the peaks of the waveform. The analog waveform is thus differentiated by CX19, RX39 and LX05, which puts slope information at the input of comparator ICX04. Since the slope equals zero at any peak and the other input to the comparator is also zero (through RX40), the comparator will change state at all analog data peaks. The comparator output is gated at pins 8 and 13, however, and the signal must be of sufficient amplitude to enable the window detector ICX02 to toggle latch ICX05.

3.8.6 WINDOW DETECTOR CIRCUITRY

The window detector determines if signal amplitude of a certain polarity is sufficiently large to consider as data. ICXØ2 pins 1Ø, 11 and 13 make up the positive signal sensing threshold. The two comparators are buffered and converted to TTL levels by QXØ4 and QXØ3, respectively.

During the write mode, the inputs to the comparators are the analog signal (through CX18 and CX2Ø) and two DC voltage levels determined by DAC IC7. The DAC acts as a current sink creating voltage drops across the nine sets of resistors RX1Ø, RX11, RX12, RX13, RX14, RX15. No current flow occurs through RXØ9 due to diode CRXØ1, which is back biased during write operations. The total threshold voltage is developed across RX12, with the AC coupled read signal centered on the total threshold voltage, due to the equality of resistors RX1Ø and RX14; RX11 and RX13.

When writing, an analog data signal at pin 11 of ICXØ2 more negative than the DC threshold voltage at pin 1Ø will cause the comparator output to swing negative, pinching off QXØ4. This will cause pin 13 of comparator ICXØ5 to go high, thereby opening the threshold window for differentiated data of the correct polarity to pass to latch ICXØ4. For positive going signals, a similar action occurs. Data amplitudes smaller than the threshold voltages do not toggle latch ICXØ5.

When reading, the DAC sink current is zero and the threshold divider is driven through diode CRXØ and resistor RXØ9. The source of drive is capacitor CXØ1 and transistor QXØ2 of the peak follower circuit (see section 3.6.7). The threshold voltage is developed across RX12, with the read signal capacitively coupled to the center of this value. Capacitor CX24 forces the threshold voltage time constant to be equal to the coupling capacitor (CX18) time constant, such that the threshold voltage will tend to track the analog signal baseline with changes in threshold divider voltage.

3.8.7 PEAK FOLLOWER CIRCUIT

The peak follower generates a variable DC voltage instantaneously equal to the peak-to-peak amplitude of the analog data signal across RX11 and RX13. This occurs only in the read mode with the signal AGC ENABLE logic true. Analog data present at pins 6 & 9 of ICXØ2 will force pins 1 or 14 of ICXØ2 to go negative if the DC voltages at pins 7 or 8 are not equal to the analog signal amplitude. This causes current source QXØ2 to turn on, charging capacitor CXØ1. This voltage is fed back to pin 7 of ICXØ2 and the thresholding divider through CRXØ1 and RXØ9. Since QXØ2 is capable of charging CXØ1 relatively rapidly, and CXØ1 discharges fairly slowly; the DC voltage fed back

to pin 7 of the comparators will be nearly equal to the positive peak value of the analog signal applied to pin 6. A similar effect happens at pins 8 and 9 of ICX02 for negative analog signals since RX11 and RX13 are equal. Resistor RX44 aids in the discharge of CX01, while diode CRX03 prevents CX01 voltage from becoming excessively negative with no signal input.

3.8.8 AUTOMATIC GAIN CONTROL CIRCUIT

The peak follower voltage on CX01 is tapped off through RX05 and CRX07. After filtering by CX26 and a capacitor on the preamp board assembly, this voltage is applied to the gain control input of the respective channel on the preamp board to form an AGC control loop. Diode CRX07 isolates the AGC discharge time constant from the peak follower time constant of CX01 and RX44.

3.8.9 DIRECTION CONTROL CIRCUIT

Fet QX06 is turned on when operating in reverse, allowing CX15 to shunt CX14 in the delay equalizer circuit. This adds more delay at low fre-quencies to compensate for basic changes in read characteristics during reverse.

3.8.10 NRZ1 EQUALIZER CIRCUIT

Two FET's, QX09 & QX10, change the response characteristic of each read channel for use with NRZ1 data. QX10 allows RX43 to shunt the frequency equalizer associated with ICX03, thus greatly increasing the gain at low frequencies. QX09 allows CX20 to shunt CX18, which extends the low frequency response of the signal path to comparator ICX02, preventing base line wander at the threshold comparator input.

3.8.11 ENVELOPE DETECTOR

As an overall indication of signal being present during read only mode, the voltage at CX01 is tapped by RX01 and used to drive QX01. When QX01 is driven on, pin 4 of ICX01 is forced high, allowing latch

ICXØ5 to operate. With little or no analog signal present, the voltage at CXØ1 is low, QXØ1 is off and output latch ICXØ5 can be forced to a known state if ENVELOPE ENBL is logic high (ICXØ1 pin 6). Hysteresis is provided through RXØ4, with level shifting provided by RXØ3. If ENVELOPE ENBL is held low, all data coming through the read chain appears at the data outputs.

3.9 READ DECODERS I AND II

The Read decoders consist of two circuit boards I and II which are interconnected to each other through J12. The System Processor interfaces with Read Decoder II through J4. The function of the interface is to provide the communications link between the System Processor and the Read Decoder in order that:

1) The Read Decoder performs its function at the density selected by the System Processor.

2) The System Processor may monitor the activities of the decoders' synchronization and majority/special block recognition circuits.

3) The System Processor may monitor the data in a diagnostic operation.

The following are the input/output ports used in this interface:

Hex Address	Output	Input
ØF8AØ	load 8253-5 counter Ø (not used)	read 8253-5 counter Ø (not used)
ØF8A1	load 8253-5 counter 1	read 8253-5 counter 1
ØF8A2	load 8253-5 counter 2	read 8253-5 counter 2
ØF8A3	load 8253-5 control register	not used
ØF8A4	generate diagnostic FIFO shift out	read diagnostic data and sync status byte
ØF8A5	load decoder density and diagnostic track select	read majority/special block recognition byte

3.9.1 DECODER DENSITY AND DIAGNOSTIC CONTROL

The system processor selects the decoder operation density and the diagnostic track via an octal D flip-flop.

Bits 0-3 Diagnostic Track Selection

Bit 3 2 1 0	Track
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
0 0 1 1	4
0 1 0 0	5
0 1 0 1	6
0 1 1 0	7
0 1 1 1	8
1 x x x	9

Bits 4-5 Density Selection

Bit 5 4	Density
0 0	GCR
0 1	PE
1 0	NRZ1
1 1	ILLEGAL

Bit 6 not used

Bit 7 FIFO enable, resets FIFO when low.

3.9.2 DIAGNOSTIC DATA AND SYNCHRONIZATION STATUS

Decoded data, crossover flags, envelope status, and FIFO strobes from all nine tracks are multiplexed by a network connected as a quadruple 9 to 1 multiplexer. The data is shifted into the diagnostic FIFO by the accompanying FIFO strobes. The System Processor may monitor the data by issuing an input read command to address ØF8A4. FIFO handshaking and synchronization status are also provided in this port.

Bit	Ø	decoded data of the selected track (through FIFO)
	1	crossover flag of the selected track (through FIFO)
	2	envelope status of the selected track (through FIFO)
	3	not used
	4	FIFO output ready
	5	RDGATEEN
	6	PLOTRKEN
	7	SYNCEN

3.9.3 MAJORITY/SPECIAL BLOCK RECOGNITION BYTE

This byte provides the system processor with the envelope activities monitored by the majority prom.

Bit	Ø	MAJ1
	1	MAJ7
	2	MAJ8
	3	MAJ9
	4	ARA ID burst
	5	GCR ID burst
	6	PE ID burst
	7	FILE MARK

3.9.4 CLOCK GENERATOR

Read Decoder I includes cicuitry which generates two clock frequencies of 26.04 MHZ and 15.36 MHZ by utilizing two crystals: Y1 together with its associated components comprises the oscillator for generation of a clock 64 times the PE data rate while Y2 generates a clock for GCR operation. The LOWDEN signal derived from PEEN/ and NRZEN/ is used to select the proper clock frequency for a particular mode of operation.

During normal operation Strap 1 (ST1) pins 2 and 3 are connected and pin 1 is left open. IC3, 4 and 6 divides the S64CLK of IC5 pin 6 in order to generate S2, S4, S8, S32 and GAP clocks. ST1, with pins 1 and 2 jumpered and pin 3 open, in conjunction with IC1, 2, 7 and 9 is a configuration used for Signal Analysis (SA) purposes.

3.9.5 DATA TRANSITION DETECTOR

Data from the read amps, which enters the decoders via J10, are buffered by schmitt triggered inverters (IC33). Data Strobes of S32CLK width are generated by the edge detector circuit of ICs 34 and 29 or ICs 15 and 28. Multiplexers (ICs 28, 29 or 30) are used for every three tracks of data to generate RD DATA STRBs. The purpose of these multiplexers is to substitute the data by GAPCLK during gap and the initial portion of preamble in order to maintain vco loops at the nominal data rate.

3.9.6 ENVELOPE DETECTION

Envelope flags are generated to indicate the detection of data streams. DATASTRB from each incoming data stream sets the envelope flip-flop (LS74) and presets a 4 bit counter (LS191). As long as DATASTRB arrives before the counter overflows, envelope flag stays in a latched state. If DATASTRB is not detected again and the counter overflows, the envelope flip-flop is reset to indicate the loss of data. S4CLK is multiplexed to count up the counters during PE/GCR and S2CLK during NRZ1. The counter preset is determined by the minimum elapsed time required to recognize the loss of data. In GCR, the gaps are up to 2 bit cells in length in the incoming data, representing up to two consecutive zeros permissible in GCR. An elapsed time of three and one half bit cells is necessary before envelope reset. Similarly, in PE, an elapsed time of two and one half bit cells is necessary. Therefore, only one and one half bit cells of elapsed time is required to detect the loss of an envelope. The

following shows the counter preset values and nominal envelope elapsed time after each preset for GCR and PE.

GCR:

PLOTRK EN	RDGATE EN	PRESET D C B A	ELAPSED TIME	EQUIV. CELLS
0	0	0 0 0 0	9.2 usec	3.75
0	1	1 0 0 1	3.7 usec	1.5
1	1	0 0 0 0	9.2 usec	3.75

PE:

PLOTRK EN	RDGATE EN	PRESET D C B A	ELAPSED TIME	EQUIV. CELLS
0	0	1 0 0 1	6.2 usec	1.5
0	1	1 0 0 1	6.2 usec	1.5
1	1	0 1 0 1	10.4 usec	2.5

When MAJ7 is false during PE the preset value on Read Decoder 2 is modified to 0101 instead of 1001 to obtain the proper envelope timing for PE ID burst detection, which requires a minimum elapsed time of 8.3 usec on track 4 before envelope reset. For NRZ1, the preset value is always 0011 with a hold time of 25 usec, which is approximately 1.5 times that of a nominal NRZ1 cell period.

3.9.7 DENSITY IDENTIFICATION AND MAJORITY DETECTION

On Read Decoder II, envelope majorities, identification bursts, and file marks are detected by a majority prom (IC56). The following shows the conditions for detections.

MAJ1 - when any envelope is detected.

MAJ7 - when more than 6 envelopes are detected.

MAJ8 - when more than 7 envelopes are detected.

MAJ9 - when all 9 envelopes are detected.

ARA ID - envelopes detected in tracks 2, 3, 5, 6, 8 and 9 and none in tracks 1 ,4 and 7.

GCR ID - envelope detected in track 6 only.

PE ID - envelope detected in track 4 only.

GCR FILE MARK - envelopes detected in tracks 2, 5, 8 and 1, 4, 7.

PE FILE MARK - envelopes detected in tracks 2,5,8 and any combination of tracks 1, 4, and 7.

3.9.8 LOOP SYNCHRONIZATION

The purpose of loop sychronization is to provide proper timing for the acquiring and tracking loop frequencies. Prior to data blocks all loops are maintained by GAPCLK. When MAJ7 is detected, indicating detection of 7 or more envelopes, a 4 bit counter (IC35), starts counting. The clock input of IC35 is connected to GAPCLK and when it counts to 15, its carry output sets RDGATEEN which, via the multiplexer described in 3.7.5, switches the loop input from GAPCLK to data. RDGATEEN then enables two more 4 bit counters, ICs 36 and 37, which count up and generate PLOTRKEN and SYNCEN, 18 and 34 cell periods respectively, after RDGATEEN is set. Once SYNCEN is set, both ICs 36 and 37 are disabled. SYNCEN is self latching at the third counter's terminal count. PLOTRKEN is used for switching vco loops from high gain acquiring mode to low gain tracking mode. SYNCEN does not affect vco loops, instead it is used to enable the output of FIFO strobe signals. Loop frequencies from tracks 5, 4, or 6 are multiplexed to the clock inputs of ICs 36 and 37.

3.9.9 PHASE LOCK LOOP

The phase lock loop consists of a phase lock oscillator (PLO), phase and frequency discriminators and crossover/out-of-lock detection circuits. Loop coherence is maintained whenever envelope dropout or crossover occurs, by switching the loop input to the reference strobe generated from an adjacent loop frequency.

3.9.9.1 PLL DISCRIMINATOR

All PLLs are in the acquire mode during the interblock gap and the

initial portion of the preamble. The PLLs are switched to the tracking mode by flip-flop IC11Ø pins 5 & 6. When PLOTRKEN is set, IC11Ø switches the mode of operation by enabling the phase discriminator and disabling the frequency discriminator. Inputs B3 and B4 (from the frequency discriminator flip-flop ICXØ6) from multiplexer ICXØ5 are disabled while PMPTRK.N and PMPTRK.N/ are enabled. Additionally, during PE tracking mode, PEEN/ enables PMPTRKPEN and its complement at ICX12 pins 3 & 6, in order to maintain vco gain.

The phase discriminator (ICXØ9 pins 5 & 6 and ICXØ8 pin 9), the frequency discriminator (ICXØ6, ICXØ8 pins 6 & 11, ICX24 pin 4, ICXØ7 pin 11 and ICX22 pin 4), the digital one shot (ICXØ7 pin 3, ICX11 pin 12 and ICXØ9 pin 9), and the vco phase detector counter (ICX17 and ICX18 pins 8 & 9) are initialized and synchronized by JAMLD/ (ICX24 pin 8) whenever RDGATEENs' level change is detected by IC3Ø and IC29 pin 8 (Read Decoder I) in conjunction with S8CLK.

3.9.9.2 DIGITAL ONE SHOT

This circuit provides a timing reference for the phase and frequency discriminators. VCO32.N and S32 clocks, which are multiplexed by ICXØ5 at pin 4, increments ICX11 and ICXØ9, generating a pulse which is half the nominal data cell at ICXØ9 pins 5 & 6. The pulse is generated at the leading edge of DATASTRB.

3.9.9.3 PHASE DISCRIMINATOR

Two corrective pump charge signals are derived from the phase discriminator: PUMPTRK.N & PUMPTRK.N/, which increase and decrease vco frequency respectively. The two signals are produced at flip-flops ICX1Ø pin 9 and ICXØ9 pin 6. When the vco phase lags the data (VCOSTRB/ occurs after one shot trailing edge), the phase discrepancy increases the input voltage to the vco, thus increasing the frequency. Conversely, when the vco phase leads the data (VCOSTRB/ is detected before the trailing edge of the one shot), the phase discrepancy reduces the vco input voltage, thus decreasing the frequency. These two corrective signals cancel each other when the data and vco phases match each other. The corrective pump charge signals are connected to lower gain inputs (as compared to those in the acquire mode) of the vco network to emphasize the correction of tape speed variance, rather than individual magnetic bit drift.

3.9.9.4 FREQUENCY DISCRIMINATOR

The frequency discriminator generates two pump charge signals, PMPAQ.N & PMPAQ.N/, which correct for any static speed deviation before switching to the tracking mode. When the vco phase lags the data, speed-up pump charge signal PMPAQ.N becomes latched at ICX24 pin 4 by the trailing edge of the digital one shot until the detection of VCOSTRB. Conversely, when the vco phase leads the data, VCOSTRB/ latches the slow down pump charge PMPAQ.N/ until the trailing edge of the digital one shot.

3.9.10 PLL MONITOR

3.9.10.1 VCO MULTIPLEXER AND PHASE DETECTION

During operation in GCR, VCOCLK.N is output at ICX14 pin 6 as VCO32.N. During operation in PE, VCOCLK.N is divided by two at ICX18 pin 6 before being multiplexed by LOWDEN/. Loop gain, even though lowered by the division of PE clock, is compensated for by pump charge signals. PMPTRKPE.N and PMPTRKPE.N/, enabled by PE/ at ICX12 pins 3 & 6, doubles the feedback currents to the vco network. Therefore, the vco operates in a linear region eventhough the vco operating center is set in GCR. ICs X17 & X18 count VCO32 CLK, providing vco phase detection with 3.12% resolution. The ripple carry output at ICX17 pin 13 (VCOSTRB/) indicates cell boundary while the QD line generates DCLK for PE/GCR.

3.9.10.2 REFERENCE STROBE GENERATOR

Reference strobes are generated and substituted for data strobes whenever envelope dropout or crossover occurs in the reference tracking mode. The reference strobes are derived by counting the VCO32 CLK from one of three adjacent tracks. For example, track 1 reference strobe is generated from VCO32.2 and track 2 reference strobe is generated from VCO32.3, while track 3 reference strobe is generated from VCO32.1. Therefore, under worst case conditions, reference strobe is derived from frequency information which is only two tracks away. A five bit counter (ICs X13 & X15) synchronizes reference strobe to the middle of a cell boundary when preloaded by VCOSTRB/ preceded by a data strobe.

3.9.10.3 CROSSOVER/OUT-OF-LOCK DETECTION

Crossover, under certain criteria, occurs when a data transition crosses a cell boundary. Thus, data pattern 11 appears as 101, 1010 as 11 or 1001, and 1001 as 101. Since the data strobe together with the vco strobe provides the PLL with frequency information, crossover may result in incorrect feedbacks. The crossover detector is based on the following: the maximum cell expansion or contraction is 56% of one cell period for first order peak shifts and 28% for second order peak shifts. Crossover windows (W1/-W5/), generated by ICX19, are utilized with the following criteria to determine if a data transition has crossed a cell boundary:

1) The prior data transition occurred within 62.5% of its following cell boundary and data up to the transition under test was detected as 101 and the transition occurred within a crossover window immediately behind the preceeding cell boundary.

2) The prior data transition occurred within 31.3% of its preceding cell boundary and data up to the transition under test was detected as 11 and the transition occurred within a crossover window immediately ahead of the following cell boundary.

3) The prior data transition occurred within 31.3% of its following cell boundary and data up to the transition under test was detected as 1001 and the transition occurred within a crossover window immediately behind the preceding cell boundary.

4) The prior data transition occurred within 62.5% of its preceding cell boundary and data up to the transition under test was detected as 101 and the transition occurred within a crossover window immediately ahead of the following cell boundary.

In each of the above cases, the first condition establishes the phase relation between the prior data transition and the data cell, the second condition differentiates data patterns.

In circuit implementation, two flags, DPC and OVS, are tested

according to the following to determine the data pattern:

DPC	OVS	
1	X	The previous data transition occurred within the preceding cell (11 pattern).
Ø	Ø	The previous data transition occurred 2 cells before (1Ø1 pattern).
Ø	1	The previous data transition occurred 3 cells before (1ØØ1 pattern).

Whenever a crossover is detected the circuit disables pump charges temporarily and enters into reference tracking at the immediately following cell boundary.

Reference tracking due to crossover is set to last for a minimum of 16 cell periods and a maximum of 32 cell periods. Dropout also activates reference tracking in order to maintain loop coherence. In such a case it will last until 16 to 32 cell periods after the recovery of the envelope. The crossover flag is synchronized to provide a set up time of one clock period of the S32CLK and a hold time of half a cell period in order to satisfy the FIFO interface requirement.

Early detection of loop blow-up is required to prevent overflow/underflow of the Read Handler FIFO. This is accomplished through the Out-Of-Lock (OOL) flag. The OOL flag is set when crossover is detected while in the reference tracking mode. This indicates a large discrepancy between an adjacent track's loop frequency and causes crossover during a reference lock operation. Once the OOL flag is set, it is latched until the end of a data block.

3.9.11 PHASE LOCK OSCILLATOR

The Phase Lock Oscillator (PLO) circuitry receives corrective feedback signals from the discriminator via high speed CMOS inverter ICXØ3. Several stages of operational amplifiers (ICXØ1) provide gain and integration of these signals before driving an ECL voltage controlled oscillator. The central operating point of the vco is calibrated to produce an output frequency of 13.Ø2 MHZ (GCR nominal S32 clock) while the input voltage is set at -8ØØ millivolts. The ECL output of the vco is then converted to a TTL level by ICXØ4 which outputs VCOCLK.N.

3.9.12 NRZ1 DATA CLOCK GENERATOR

During NRZ1 operation, loop synchronization as well as vco loops are disabled. The loops are maintained in the PE nominal data rate. NRZ1 data clock (Read Decoder I) is directly generated from S32CLK which is 128 times the NRZ1 data rate. S32CLK is divided by 8 by 4 bit counter IC27 to obtain a clock 16 times the NRZ1 data rate which in turn is divided by a second 4 bit counter (IC20) to generate two clocks: one twice the data rate and one equivalent to it. During the interblock gap the counters are free running. Upon arrival of a data byte, the leading data transition synchronizes the counters. Once synchronized, further synchronization is not allowed until 75% of the cell period is past. This prevents synchronization by the same byte of data more than once. The circuit continues to do so for the entire data block, thereby eliminating an accumulation of phase errors. When a data block is detected the majority prom (IC56, Read Decoder II) issues MAJ1/, which is terminated one and one half cell periods after the end of a data block. MAJ1/ is used to enable NRZCLK via IC21 pin 12, IC11 pin 3 and IC31 pin 2. NFCCLK, output at IC31 pin 3, which is generated for the purpose of providing the FIFO strobe during NRZ1, differs from NRZCLK in that it is delayed one cell period. Both NRZCLK and NFCCLK are in phase with the data and terminate at the trailing edge of MAJ1.

3.9.13 DATA CLOCK AND FIFO STROBE

Data clock (DCLK.N), is generated by an inverting multiplexer IC19. In PE or GCR operation, DCLK is derived from VCOCLK via the vco phase detector (ICs X17 and X18 pins 8 & 9). In NRZ1, DCLK is derived from NRZCLK. The inverting multiplexer is used to ensure that DCLK is in phase with the data cell boundary. DCLK.N clocks ICX28 and ICX27, while Data STRB.N clocks ICX28 pin 3. The three flip-flops produce decoded signals DSTB.N/ and DDATA.N/.

3-10 SERVO TAPE/TRANSPORT

The system processor communicates with the servo via connector J4 (sheet 1 servo schematic).

3.10.1 DATA BUFFER

A bidirectional buffer (IC15) controls data flow to and from the servo on lines OBDØ-7, depending on the signals OBRD/ and OBSERVO/, which determine flow direction and output enable respectively.

3.10.1.1 PIO CONTROL BUFFER

Lines OBAØ, OBA1, OBSERVO/, OBRD/, OBWRT/, OBDEAD/ and OBVAC/ are fed into the PIO control buffer (IC16) and are enabled by VAC and 48Vs to protect against a condition where tape might have been pulled out of one or both columns during a rewind or fast forward. The following is a description of the above controls:

OBAØ and OBA1 select the PIO port that data is to be written into or read from. OBSERVO/ enables the data buffer (IC15) outputs and the Programmable Peripheral Interface (PPI--sometimes referred to as a PIO) chip (IC14).

The direction of the data flow is determined by OBRD/. When OBWRT/ is true the system processor can send commands to the servo board, whereas a false OBRD/ enables it to read the servo status.

3.10.1.2 PROGRAMMABLE PERIPHERAL INTERFACE (PPI)

The Programmable Peripheral Interface (IC14) controls the channeling of data into or out of the board. It is initialized from a reset as follows:

	A1	AØ	RD/	WR/	CS/	DATA
1)	1	1	1	Ø	Ø	81HEX
2)	Ø	Ø	1	Ø	Ø	ØØHEX
3)	Ø	1	1	Ø	Ø	3FHEX
4)	1	Ø	1	Ø	Ø	1ØHEX

Step 1) determines the configuration of the PPI which consists of outputs on ports A,B and the most significant nibble of port C, and inputs on the least significant nibble of port C.

Step 2) sets the value of the data on port A to ØØHEX.

Step 3) sets the value of the data on port B to 3FHEX.

Step 4) sets the value of the most significant nibble of port C to 10Hex.

3.10.1.3 PIO PORTS

PORT A:

Port A provides an eight bit word for the DAC chip (IC13) in order to generate a reference for the ramp generator. At low speeds, a change in LSB produces a speed change of .5 ips whereas in FAST it increases to 2.5 ips. Nonlinearity of tach voltage limits the speed accuracy to +/-.5% above 5.2 ips.

PORT B:

The output of PORT B (CONTRL0-6) contains servo controls, which get latched to IC11, allowing diagnostic flexibility to these lines without affecting the servo.

PORT C:

The following servo status are contained on the LS nibble of PORT C:

1) WRTPRO is the file protect switch status.

2) RUNNING, when high, indicates capstan motion.

3) ADC is a diagnostic signal accessed by the processor to determine its next iteration for analog to digital conversions. A number of critical signals have been routed to an analog multiplexer. Under software control, one of these signals can be selected as an input to a comparator; the second comparator input is connected to the DAC. The output of the comparator is fed back to the PPI, where it is named "ADC". Thus the System Processor may use successive approximation techniques to read the actual voltage at the selected node.

4) BRAKE controls the release or application of brake.

3.10.2 DEADMAN TIMER AND RESET

A periodic pulse, OBDEAD/, occurs every 20 ms (max) to update the one-shot (IC17 pin 9) when concurrent with OBWRT/. If not refreshed within 20 ms, the one-shot output forces a PPI reset, which is acknowledged by the processor as a fault condition.

3.10.3 SERVO COMMAND LATCH

When HOLD (IC14 pin 25) goes true, the CONTRL0-6 lines are latched by IC11 which is manipulated by the servo logic to implement the given command. A flip-flop (IC10 pin 6) forces these lines into their default mode during a reset by causing the latch to assume a high-impedance state.

3.10.4 SERVO LOGIC

An auxiliary +5V supply is provided from an on board regulator to maintain proper control during a catastrophic main +5V failure.

3.10.4.1 SERVO ENABLE (SRVENB/)

When false, all internal servo commands are inhibited.

3.10.4.2 TENSION

In the tension mode, TENSION goes true at IC18 pin 3, causing VMODETU/ and VMODESU/ to be asserted, enabling the reel servo loops to operate in voltage mode by switching R97 and R98 into the feedback loop. The take-up reel differs only slightly in its bias from the supply reel. Tape tension builds up slowly and the difference in bias causes a forward tape motion of approximately 1.5 rev/sec.

3.10.4.3 LOAD/

A high to low transition at LOAD/ enables the one-shot (IC17 pin 7) to output a pulse at IC23 pin 4. Thus, when vacuum is established or SERVENB/ goes false, the load pulse is inhibited.

3.10.4.4 FAST/

When FAST/ goes true and tape is not in motion, it latches NORMAL RAMP/ false and HIGAIN/ true providing a high capstan motor gain and lower ramp acceleration.

3.10.4.5 GCR RAMP/

When GCR RAMP/ goes false at IC19 pin 14, IC19 pin 15 goes true which opens switch IC5 pins 2 and 3 (sheet 5 servo schematic), disconnecting the shunt resistor R75 and decreasing the integrator's (IC4 pins 8,9,10) time constant to three times shorter than normal.

3.10.4.6 UNLOAD/

With VAC/ false and SERVENB/ true, UNLOAD is produced at IC18 pin 11 whenever UNLOAD/ goes true. VMODESU/ AT IC23 pin 11 is forced true turning on IC8 pins 10,11,6,and 7, thereby selecting voltage mode servo operation for the supply reel only. The servo takes about .7 seconds to reach its maximum voltage mode speed of 3 rev/sec.

3.10.4.7 VAC/

This signal, sent by the processor after vacuum verification via the vacuum switch, is gated with SRVENB/ to generate SNSENB/ at IC25 pin 15 which is used to enable the column sensors via the analog switches IC8 pins 2, 3, 14,and 15.

VAC/ gated with SRVENB/ (IC23 pins 1,2) and HOLD/ (IC10 pins 12,13) also generates REFENB/ and CAPENB/ (IC20 pin 11) to assure disabling of the capstan motor when tape is not loaded.

3.10.5 48V SENSE

This circuit consists of Q40, R173, R174, R175, CR44 and a high voltage inverter (IC25 pins 3 and 2).

The servo supply voltage is divided down by R173 and R174 and when it exceeds 35 volts, Q40 will turn off forcing 48VS to go high. CR44 will clamp the voltage at the base of Q40 to one diode drop above the +12 volt supply to prevent any damage to the transistor.

3.10.6 WRITE PROTECT SOLENOID

The write protect solenoid (sheet 2 of Servo schematic) is controlled by CNTRL6 input on IC11 pin 3 which, when high forces Q39 on, energizing the relay (the solenoid is shown in the deenergized state). The switch at J23 pins 3 and 4 give WRTPRO status to the processor.

The circuit consisting of the REFERENCE RAMP GENERATOR, VELOCITY ERROR AMP, and CURRENT ERROR AMP along with the PWR AMP and the tachometer controls the capstan motor. Their individual functions are described below (refer to sheet 3 servo schematic).

3.10.7 REF RAMP GENERATOR

The circuit consists of IC4 pins 8, 9, 10, 12, 13, 14 and all related components. The first stage (pin 14) of the amplifier is an error amplifier which swings positive or negative depending on the VREF input and the reference ramp voltage generated by the integrator stage (pin 8). Ramp rail is therefore set by the VREF input and its slope is determined by the input current to the integrator.

3.10.8 VELOCITY ERROR AMP

The reference ramp output from IC4 pin 8 corresponds to the required capstan speed and is input to the error amplifier IC2 pin 1. Whenever VTACH/(R67+R69) equals VREF/(R59+R61) the output of the error amp (pin 1) equals zero, indicating balance between required capstan speed and actual speed. In "HI GAIN/" mode, input current to the error amp is increased by switch IC5 pins 10 and 11 resulting in 5 times greater speeds for the same ramp voltage.

3.10.9 CURRENT ERROR AMP

The VERR voltage from IC4 pin 1 drives a current amplifier which, in turn drives the power amplifier transistors (Q24,25,26,27,15,33), pumping current into the motor and producing acceleration.

When IC4 pin 7 swings positive Q25, 27 and 33 turn on, pumping current from the positive servo supply to the motor. A reverse current flows when pin 7 swings negative, turning on Q24, 26 and 15.

Voltage sensed across the current sense resistor R48 is fed back to the current amplifier closing the loop. Motor currents are limited to 10 amps by the driver, R53, R57 and feedback from R48, which limits base drive to the transistors Q24 and Q25.

3.10.10 ANTICREEP CIRCUIT

Under normal running, the current amplifier (IC4 pins 5,6,7) has an open loop gain which can cause an unpredictable creeping motion when in the STOP mode.

In order to prevent this creeping motion, FET (Q37) is used to close the amplifier's feedback loop when in the STOP mode. The zero value of the reference ramp causes IC9 pin 14 to be less than or equal to 1.2 volts, forcing Q34 and Q38 off and Q37 on, inserting R132 in the feedback loop.

Q37 is pinched off whenever the reference ramp exceeds 30mV of either polarity, returning the servo into normal operation.

3.10.11 MOTION DETECTION

Tachometer voltage is sensed in a similar manner as that of the anticreep circuit when IC9 pin 8 swings positive or negative whenever tach voltage exceeds 20mV of either polarity. Q35 and Q36 are turned on, flagging 'RUNNING'.

3.10.12 REEL SERVOS

Both servos are identical so only the supply reel servo is described. These motors are slaves to the capstan motor and try to maintain the center position of the tape in the vacuum columns. The following are its subsystems:

1) Position sensor

2) Position error amplifier

3) Current amplifier

4) Power amplifier

3.10.13 POSITION SENSORS

A metalized mylar diaphragm mounted on one side of a perforated PC board constitutes a pressure to capacitance transducer. Tape loop position inside the column determines the diaphragm area affected by the vacuum and hence its capacitance.

A one-shot (IC2 pins 1,2 and 6) senses the tape loop position by converting the vacuum capacitance into a pulse when triggered by the clock circuit of IC3 pin 10. The pulse duty cycle therefore varies with tape position. R102 centers the tape position while R24, R101, R188, and C3 filter the pulse and set the loop gain.

3.10.14 POSITION ERROR AMP

When SNSENB/ goes true IC7 (pins 8,9,10) accepts the filtered pulses containing tape position information. R92, R93 and C40 determine the

amp's DC gain, cut-in and cut-out frequencies while C41 rolls off high frequencies.

R99 balances the amp's summing node when tape is positioned in the column. When in motion,tape position in the vacuum column is offset by the reference ramp voltage entering via R100 and R111.

3.10.15 CURRENT AMPLIFIER

The servo current amplifier operation is the same as described for the capstan motor. C34 and R84 provide high frequency roll-off and current is sensed via R46.

3.10.16 FAST FORWARD (FFWD)

In order to compensate for the servo response lags, the FFWD signal from the reference ramp generator couples a spike to the servo amp via R100, R111 and C43 enabling the reel motors to respond quickly and catch up with the capstan motor.

3.10.17 BACK EMF AMP (BEMF)

The BEMF amplifier (IC9 pins 1,2, and 3) limits the capstan speed to the maximum allowable by either of the reel motors. When either of the current amp registers currents are in excess of 40 mA, the BEMF amp generates a voltage at SLOWCAP to add to or subtract from the reference ramp thus limiting the capstan speed.

3.10.18 BRAKE

When braking is desired, relay K1 is deenergized, disconnecting the capstan and the servo amplifiers and shorting the servo motors through an SCR (Q8) and resistor R18. Braking is due to the current caused by the self-induced voltage across the winding.

Braking becomes imperative under the following conditions:

1) +12V supply at the emitter of Q4 or -12V at Q5 emitter fails.

2) When + servo drops, it will force Q1 and Q5 off.

3) Q2 and Q4 turning off due to servo falling off or Q3 turning on due to BREAK command going true.

To prevent relay points from arcing, Q6, C1 and R5 delay the SCR (Q8) operation until the relay's mechanical transients have died. Once K1 is deenergized, IC1 turns ON, latching Q1 and Q5 and assuring a positive stop.

3.11 READ DATA HANDLER Circuit Description

3.11.1 STATUS AND COMMAND REGISTERS

The System Processor interfaces with the Read Data Handler through connectors J4 and J5 (sheets 14 and 15 of the Read Data Handler schematics). Three status registers are available to the System Processor. One register contains information as to the general type of errors encountered during the previous read operation, while the other two registers contain per-track error status information. The status registers are mapped into the System Processor address at 0F8C0H for the general status register, 0F8C1H for the lower track pointer register, and 0F8C2H for the upper track pointer register. The Read Data Handler requires only one command byte.

The processor polls the eight bits of the general status register to determine when the Read Data Handler has finished. Bits 0,1, and 2 represent unrecoverable errors, while bits 4, 5, and 6 may represent soft errors which have not affected the integrity of the recorded data. Bits 3 and 7 should be true at the end of each record. They indicate that the residual group and postamble have been recognized. The status register is accessed by a read of address 0F8C0H. The eight bits of the status register are defined as follows:

7	6	5	4	3	2	1	0
DNORM	SKER	XOVR	ILGL	ENORM	OTE	ACRC	CRC

CRC — If high, the CRC was not found or was not valid.

ACRC — An ACRC error was detected during the last record processed; or, the residual group was not found, or was not correctly identified.

OUTPUT TIMING ERROR — The host or DMA channel failed to take data from the read handler.

ECP NORMAL COMPLETION

The error correction processor recognized the residual & CRC groups, and carried out CRC & ACRC verification checks.

ILLEGAL CHARACTER — An illegal five-code was detected during the last record processed. If no CRC or ACRC error occurred, the ECP was able to correctly restore the lost data.

CROSSOVER — A crossover pointer occurred during the last record processed and was detected by the Read Data Decoders. If no CRC or ACRC error occurred, the data handler was able to recover the data.

SKEW ERROR — The deskew processor was unable to align the data during the preamble, or alignment was lost at some time during the last record processed. If no CRC or ACRC error was detected, the ECP was able to correctly restore the lost data from the misaligned channels.

DESKEW NORMAL COMPLETION

The deskew processor recognized the postamble of the last record processed.

Three bits of the LOWER TRACK POINTER REGISTER contain pointers to 3 of the 9 tape tracks. If any of these bits is high, then some sort of error was detected in that track during the previous read operation.

7	6	5	4	3	2	1	Ø
n/a	n/a	n/a	n/a	n/a	TP3	TP2	TP1

Six bits of the UPPER TRACK POINTER REGISTER contain pointers to 6 of the 9 tape tracks. If any of these bits is high, then some sort of error was detected in that track during the previous read operation.

7	6	5	4	3	2	1	0
n/a	n/a	TP9	TP8	TP7	TP6	TP5	TP4

The System Processor controls the operation of the Read Handler by writing to the command register at 0F8C0H. This register is only written to when the ENORM and DNORM bits in the general status register are true. The bits in the command register are as follows:

7	6	5	4	3	2	1	0
n/a	n/a	RDEN/	CCGEN	COR/	FWD	PE	GCR/

GCR/ When low, the Read Handler expects to process GCR data. When high, the Read Handler examines bit 1 to determine whether to expect PE or NRZ1 data.

PE If GCR/ is high and bit 1 is high, the Read Handler expects PE data. If GCR/ is high and PE is low, the Read Handler expects NRZ1 data.

FWD Direction of tape travel. Necessary for proper data decoding.

COR/ If COR/ is high, the Read Handler's error correction capability is inhibited. This mode is used in read-after-write, when it necessary to certify the tape to be free of dropouts. For NRZ1 single track correction, execute a Space Reverse command, then read the block with this bit set low.

CCGEN In NRZ1 mode, when this bit is set high, the CRC and LRC characters are transmitted over the interface to the host, accompanied by the CCG flag. When low, the CRC and LRC are not transmitted.

RDEN/ This bit is set high by the System Processor between data records. When the bit goes low, the Read Handler starts to look for data at its inputs. When high, the Read Handler is in a reset state.

3.11.2 DESKEW PROCESSOR AND ARCHITECTURE

Architecturally, the Deskew Processor consists of a sequencer, a

control store, a processing unit, a Track In Error (TIE) pointer logic block, and a First-In-First-Out (FIFO) memory for input.

3.11.3 INPUT FIFO

Input data (UDATA.N/, UOOL.N/, USTROBE.N/ and UXOVER.N/) from Read Decoders I and II (See sheets 1 & 2 of Read Data Handler) enters the Read Handler via connectors J1, J2 and straps ST22 and ST23. The input data is buffered by ICs 160-164 and is strobed into 9 separate FIFO memories (ICs 138-147) by BSTROBE.N/. The Deskew Processor waits until data is available from all 9 FIFO's by searching for a MARK1 data pattern (00111) in each channel before shifting data out simultaneously. As soon as the Deskew Processor finds the MARK1 in each channel, it stops shifting data out from that channel's FIFO until it finds a MARK1 character in all 9 channels or until a time-out occurs. All skew is eliminated and byte-wide aligned data emerges from the FIFO's as they are shifted in unison. The FIFO ready logic (IC116) receives the OUTPUT READY (OR.N) byte which generates the FIFO READY term (FREADY/) at IC117 pin 9.

3.11.4 DESKEW SEQUENCER

The sequencer (IC33) is an Am2910 'Microprogram Controller.' Only 9 bits of its 12-bit address field are currently used to select addresses in the ROM microcode control store; the other three bits are available for expansion. The 2910 can step sequentially through all 512 microinstructions in its presently utilized address space, or it can execute conditional or unconditional jumps to any address. It has a stack for storing subroutine return addresses, and a counter for implementing loops. It can also jump to a location specified by a map ROM (IC34) which allows the System Processor to select one of several microcode routines for execution. A condition code multiplexer (IC99) selects among several signals to determine whether a conditional branch will take place. The available condition codes are PARITY (DPARL), ZERO (DZEROC), FIFO DATA READY (FRDY/), INPUT DATA EMPTY (INMTY/), END MARK DETECT (ENDMRKL), and TWOL, THREEL, and FIVEL (true if at least 2, 3, or 5 lines on the Y-bus are high). Clock is supplied by IC92 an Am2925 Clock Generator.

3.11.5 DESKEW CONTROL STORE

The microinstruction word for the Deskew Processor is 32 bits wide.

The control word includes 9 bits to select the 2901 processor function, 4 bits to select the sequencer op-code, 3 bits to select the condition code input, 4 bits to select input or output functions, 2 bits to control the Am2925 programmable cycle length variable speed clock, and 10 bits shared between RAMA & RAMB address fields and sequencer branch address.

3.11.6 DESKEW PROCESSING UNIT

The processing unit is built of three Am2901 four-bit slices. These parts are similar to the 2903's but have a simplified instruction set and do not have the 'hooks' to add external RAM register files.

The processing unit has a single input bus, the 'D' bus. Under microprogram control, the FIFO data and phase TIE registers may be input to the 'D' bus, and used as ALU operands. The unit also has a single output bus, the 'Y' bus, which may be latched to the status register, the ECP input buffer, the FIFO shift-out control register, the majority voter PROM, or the TIE pointer logic block.

3.11.7 TIE POINTER LOGIC BLOCK

The TIE pointer logic block (sheet 6 of Read Data Handler schematics) is a priority encoder which always has two active outputs. The Deskew Processor accumulates several error pointer masks (illegal, dropout, phase TIE) of different priorities. These masks are output to the TIE pointer logic in sequence from lowest to highest priority. After all masks have been input, the output of this logic block is a mask pointing to the two highest priority error pointers. If no pointers are active during the current group, the error mask from the previous group becomes the new error mask.

3.11.8 ERROR CORRECTION PROCESSOR (ECP) SEQUENCER

The sequencer (IC14) is an Am2910 'Microprogram Controller.' Only 9 bits of its 12-bit address field are currently used to select addresses in the ROM microcode control store; the other three bits are available for expansion. The 2910 can step sequentially through all 512 microinstructions in its presently utilized address space, or it can execute conditional or unconditional jumps to any address. It has a stack for storing subroutine return addresses, and a counter for implementing loops. It can also jump to a location specified by a map

ROM (IC15) which allows the System Processor to select one of several microcode routines for execution. A condition code multiplexer (IC42 and 43) selects among several signals to determine whether a conditional branch will take place. The available condition codes are ZERO (EZEROC), CORRECT/, MODULO 32 COUNT 0 (M320), PADCRC/ (determines if a 0 should be added to the CRC group), OUTPUT DATA READY (OUTDRDY), END MARK DETECTED (ENDMRK), RAM DATA.N (RAMDN), INPUT DATA READY (IDRC), VALID HARD POINTER (VHP), and CHECK CHARACTER GATE ENABLE (CCGEN). Clock is supplied by IC59 an Am2925 Clock Generator with a programmable variable cycle length.

3.11.9 ERROR CORRECTION PROCESSOR (ECP) CONTROL STORE

The control store is 512 bytes by 40 bits of bipolar PROM memory (ICs 24, 7, 25, 8, 26, 9, 27, 10, 23 and 6). The 40-bit instruction word is divided into several control fields. Nine bits are used to control the 2903 bit slice ALU functions. Five bits are used to select the 2910 sequencer function. Twelve bits are used for addressing RAM memory, including the 2903's internal RAM, the input and output register files, and other registers (two RAM addresses, RAMA and RAMB, are used independently to address the dual-port RAM. Each address field is 6 bits wide.) The RAM address field is shared with the branch address field.

Counters are included on the outputs of the RAMA and RAMB address fields in order to allow software loops to index through several bytes of data. These counters are transparent for most operations. However, a three-bit field is allocated to control these counters, allowing them to be loaded with an address and then incremented.

Three bits are used to control writing to the CRC and ACRC accumulation registers, three bits control handshaking with the Deskew Processor, and two bits are used to control a 2925 clock generator which allows variable cycle lengths depending on the complexity of a microinstruction. This clock permits the ECP to run at the highest possible speed for each instruction. Finally, a two-bit field controls the operation a a 4-level register file.

The 40-bit microinstruction word is fed from the ROM into a single-level pipeline register. This register allows the instruction fetch cycle to occur simultaneously with the operation of the bit-slice ALU.

3.11.10 ERROR CORRECTION PROCESSOR (ECP) UNIT

The ECP consists of three type 2903 bit-slice chips (ICs 83-85), which form a 9-bit ALU with a 16-byte dual-port RAM memory (ICs 80 & 81) and

a special 'Q' register for storing intermediate results. The ALU can perform 16 different arithmetic and logical functions on two variables, called R and S. The R operand is selected by the RAMA field, while the S operand may be selected by the RAMB field, or it may come from the internal 'Q' register. Depending on the function selected, the output of the ALU may be shifted left or right, and/or written to the register specified by the RAMB field.

In addition to the 2903 internal RAM, the RAMA address field is used to access the input register file, the EMASK register, the KVAL ROM, the vertical parity register, and the CRC and ACRC registers. The RAMB address field is used to write to the 4-level register file, the status byte, the CRC and ACRC accumulation registers, and the output byte count register. It is also used to read and write the output register file.

Look-ahead carry is generated by a 2902 (IC111) for arithmetic operations. The least significant slice's 'carry-in' input is tied high, in order that a '1' may be entered into the processor using an ADD instruction with both operands equal to zero.

The processing unit contains a number of special purpose registers. The EMASK register always contains a 9-bit value with 2 bits set true and the other seven false. The two true bits point to the two tracks judged to be most likely to contain an error. The EMASK value is generated by the deskew processor's TIE pointer logic block, based on phase TIE signals from the data decoder, and its own detection of illegal 5-codes.

The KVAL ROM is used as a look-up table to access a value which is used in the two-track error correction algorithm.

The CRC and ACRC accumulation registers are recirculating shift exclusive-or registers, capable of operating either in forward or reverse mode. They carry out all operations necessary to accumulate the CRC and ACRC charcters, respectively. They are read once at the end of each record, at which time their contents should be zero. The CRC and ACRC registers are implemented using PAL16R6 fuse-programmable logic arrays.

The vertical parity register is a shift register with parallel output and serial input. As each byte of data is input from the Deskew Processor, its parity is calculated and shifted into the parity register. If no errors occur, the vertical parity register will contain zero. If a nonzero value is found, it is used in the error correction algorithm.

The status register is used to communicate status information to the System Processor.

The 4-level register file is used to select an ALU operand from up to 4 values on a conditional basis. The selection is determined based on two bits of data shifted out simultaneously from the 2903's Q register

and ALU shifter. This facility is very useful for syndrome accumulation, multiplication modulo a polynomial and replication.

The input and output register files are used to buffer data coming into and out of the error correction processor. These files are implemented with type 29705 sixteen-byte dual-port RAMs.

The output byte count register is used to control the removal of data from the output register file to the Am2950 output port.

3.11.11 ERROR CORRECTION PROCESSOR OPERATION

3.11.11.1 INPUT DATA

The ECP expects to receive raw GCR data stripped of all preambles, postambles, sync characters, and mark characters. The data input to the ECP must be deskewed -- it must be a sequence of byte-wide data.

The data input handshake protocol is defined as follows: at the beginning of a read operation, the ECP will assert its 'INPUT DATA EMPTY' signal. The input data loader should then set-up the first byte of data on the FDATA input data bus and strobe BUFWRT/ to write the data into the ECP's input data register file, while simultaneously incrementing the data register file address pointer. The second, third...through eighth byte of data may be input to the ECP in the same way. After the entire 8-byte group has been entered to the ECP, the Deskew Processor should create the EMASK and latch it for the ECP's use, and then assert 'INPUT DATA READY' to tell the ECP that it may start to process the data. The ECP removes INPUT DATA EMPTY and the Deskew Processor removes INPUT DATA READY to complete the cycle. A complete group must be processed every 25 microseconds at 45 ips.

When the Deskew Processor detects an END MARK subgroup on the tape, it notifies the ECP by asserting 'END MARK DETECT'. The Deskew Processor does not load any mark or sync subgroup into the ECP. Also, the ECP does not care about resync bursts, and is not notified of their occurrence on the tape.

If the tape is running in reverse, the ECP will output the corrected data to the CRC/ACRC register and the output port in reverse order.

Note that the Deskew Processor needs to look-ahead one subgroup for dropouts, in order to guarantee that all dropouts are detected and flagged in the EMASK of the group in which they first begin. For example, if the original data is: 01010 10111 11110 01010 ..., and a dropout occurs beginning at the 10th bit of the 1st group. The data from 5-to-4 decoding will be: 01010 10110 00000 00000 ...If only the first group is looked at, there is no way to tell that a dropout has

occurred. Thus, to develop a correct EMASK for the first group, it is necessary to 'look-ahead' for dropouts in the second group.

3.11.11.2 READ HANDLER OUTPUT DATA

Output from the ECP is handled by a block of logic called the 'output data sequencer'. When the ECP finishes correcting a group of data, it loads the data into a 29705 buffer RAM, and sends a 'start' command to the output sequencer. The sequencer then sends the first data byte to the output register, and waits for the System Processor or host to take the data. As each byte of data is taken, the next byte is made available at the output port. At 45 ips, a group of seven bytes must be taken every 25 microseconds, or an 'output timing error' will result.

3.12 POWER SUPPLY CONTROL (Circuit Description)

Several voltages are monitored by the System Processor via the Power Supply Control board (located next to the take-up reel motor) in order to detect any voltage failures. The five individual circuits on the power supply board consist of the following:

1) VACUUM BLOWER ENABLE

2) SYSTEM POWER ENABLE

3) 48V ENABLE

4) 24V FAIL

5) 12V FAIL

6) AC FAIL

3.12.1 VACUUM BLOWER ENABLE

The System Processor controls the turn on/turn off function of the vacuum blower motor with PVACEN/, which enters at connector J13 pin 7. PVACEN/ turns on ICs 5 and 7 (photo-triacs) which enables the blower motor by switching on triac Q8.

3.12.2 SYSTEM POWER ENABLE

Power supplied to the system and the cooling fans is switched via triac Q9, which is controlled by both the Front Panel Power Switch and/or the System Processor through PSYSEN/ (Processor System Enable/) at J13 pin 9.

The System Processor can enable system power and fans eventhough the Front Panel Power Switch is turned off. The processor accomplishes this by asserting a logic low PSYSEN/. This signal keeps Q9 gated on via ICs 4 and 6.

3.12.3 ENABLE 48V PROCESSOR

The reel motors on the 9400 are run from two supply voltages, 24V and 48V, as required for low and high speed operations, respectively. The System Processor connects the +/- servo lines to either 24V or 48V by controlling a set of relays, K1 and K2.

During high speed operation the processor asserts a low PFAST/ at J13 pin 5. PFAST/ causes K1 and K2 to energize, these relays connect the 24 volt supplies (J26 pins 26-29) in a series configuration, providing +/- 48 volts to the servos. During low speed operation, the +/- 24 volts are configured by the deenergized state of K1 and K2, which connects the supplies in series.

3.12.4 24V FAIL

The System Processor senses 24 volt failure by monitoring P24VFAIL/ at J13 pin 3. When the 24V line drops below 21.4 volts, Q5, Q6 and Phototransitor IC2 switch off, forcing P24VFAIL/ low which signals a 24 volt failure.

3.12.5 12V FAIL

The System Processor senses 12 volt failure by monitoring P12FAIL/ at J13 pin 1. If the 12 volt line drops below 10.6 volts Q3 switches off and causes Q4 to assert a low P12FAIL/ which signals a 12 volt failure.

3.12.6 AC FAIL

The System Processor senses AC failure by monitoring PACFAIL/ at J13 pin 2. PACFAIL/ originates from the power supply.

SECTION IV
MAINTENANCE INSTRUCTIONS

SECTION V
PARTS IDENTIFICATION

SECTION V

PARTS IDENTIFICATION

5.1 SPARE PARTS ORDERING INFORMATION

This section describes the replaceable parts in your unit which are available only from Kennedy Company. Many parts of the unit are common commercial parts and can be obtained locally from the manufacturer. These parts are marked with the manufacturer's name and part number and are not listed herein.

The serial number and part number are the keys to numerous engineering details applying to your unit. These numbers are on the serial number tag located on the rear panel of the unit.

Changes to Kennedy units are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements developed in our Engineering Department. If a part you have ordered has been replaced by a new part, a Kennedy representative will advise you concerning any change in part number.

All parts orders should be addressed directly to Kennedy Company, Spare Parts Order Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (818) 357-8831 or (818) 681-9314, ITT TELEX 472-0116 KENNEDY.

5.2 IN-WARRANTY REPAIR PARTS ORDERING INFORMATION

Repair parts for in-warranty units are made available on an exchange basis through the Kennedy Company Spare Parts Department. The serial number and part number of the tape unit are necessary to insure shipment of the proper replacement parts.

All inquiries should be directed to Kennedy Company, Spare Parts Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (818) 357-8831 or (818) 681-9314, ITT TELEX 472-0116 KENNEDY.

5.3 EXPORT ORDERS

Customers outside the United States and Canada are served by Kennedy Company international sales agents. All correspondence regarding your unit should be directed to your sales agent. If you prefer, correspondence may be addressed directly to Kennedy Company, Spare Parts Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (818) 357-8831 or (818) 681-9314, ITT TELEX 472-0116 KENNEDY.

5.4 ILLUSTRATED PARTS LIST

To assist in parts identification, an illustrated parts list is included in this section with references to illustrations of the unit. Part numbers beginning with 198 are listed again in the Recommended Spare Parts list at the end of this section. Kennedy Company recommends that these parts be ordered as spares to minimize machine downtime due to equipment failure. Certain parts on this list have no quantity indicated. We recommend ordering one of each such parts for remote installations where delivery is time consuming.

5.5 FIELD KITS

Some replacement components may be supplied in the form of repair or field change kits. The repair kits contain parts that are matched or assembled and adjusted at the factory because of complexity or to aid the field technician. The components ordered as field kits either by correspondence with Kennedy service engineers or by direct order will be supplied with complete installation instructions. The change kits are intended for standard or special options not originally included in the unit.

FRONT VIEW (See FIGURE 5-1)

Item No.	Part No.	Description
1	190-6701-001	Dust Cover Assembly
2	190-6570-001	Control Panel
3	113-0008-001	Take-Up Reel 10.5"

TOP VIEW (See FIGURE 5-2)

Item No.	Part No.	Description
1	190-6569-001	Read/Write Board Assembly
2	190-6576-001	Decoder I, 3 Channel
	190-6577-001	Decoder II, 6 Channel
3	190-6572-001	Read Handler Board Assembly
4	190-6579-001	Microprocessor Board Assembly
5	190-6712-001	Servo Heat Sink Assembly
6	190-6604-001	Power Supply Assembly
7	190-6603-001	I/O Pico Bus
	190-6791-001	I/O Pertec Bus
	190-6792-001	I/O STC Bus
	190-6793-001	I/O Telex Bus
8	190-6709-001	Fan Kit 115v 60 Hz
	190-6719-002	Fan Kit 220/240v 50 Hz

SIDE VIEW (See FIGURE 5-3)

Item No.	Part No.	Description
1	190-6079-001	Servo Board Assembly
2	190-5507-001	Slide and Rail Assembly
3	151-0061-001	Circuit Breaker

Table 5-1
9400 Major Assembly

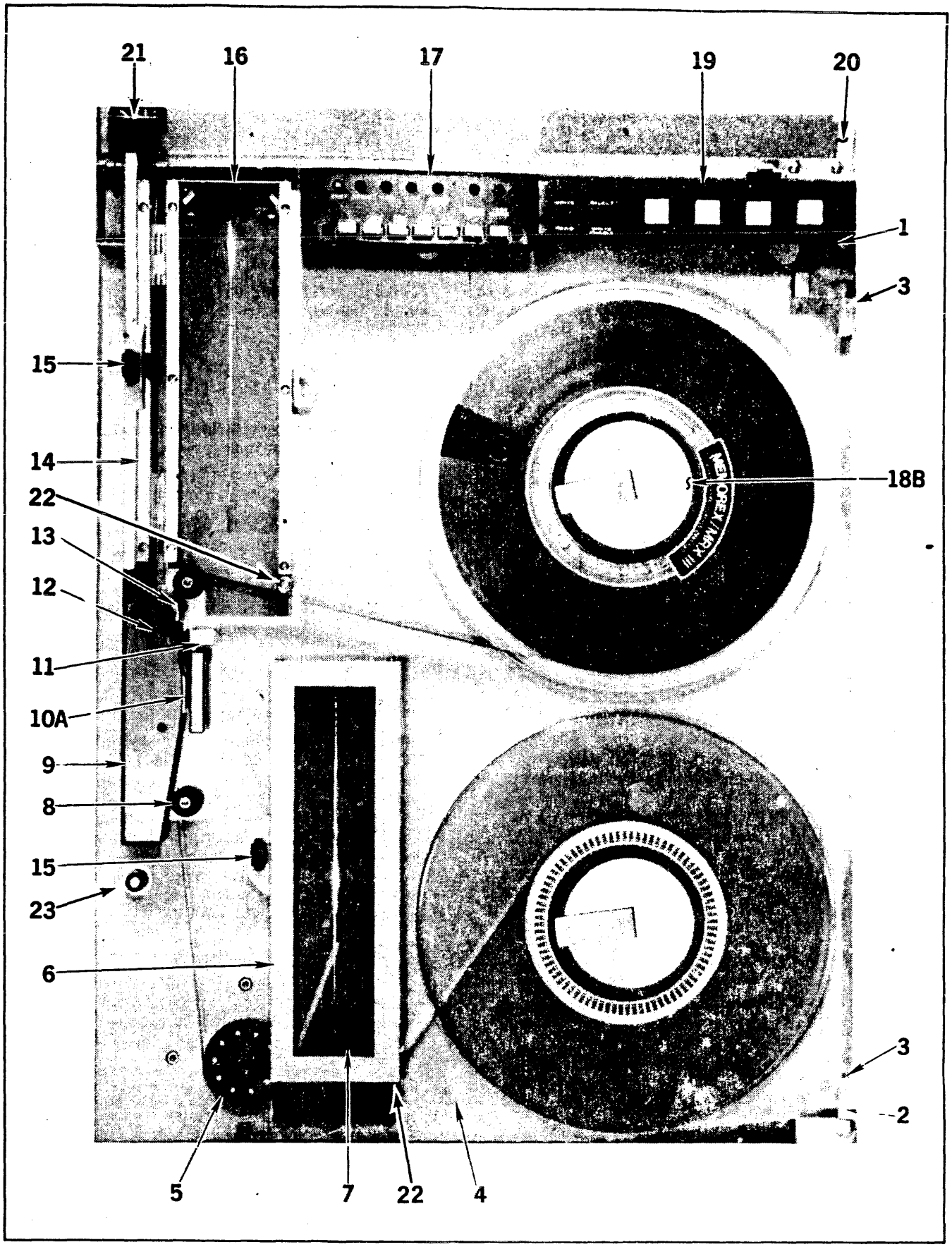


Figure 5-1. Model 9100 Tape Transport: Front View

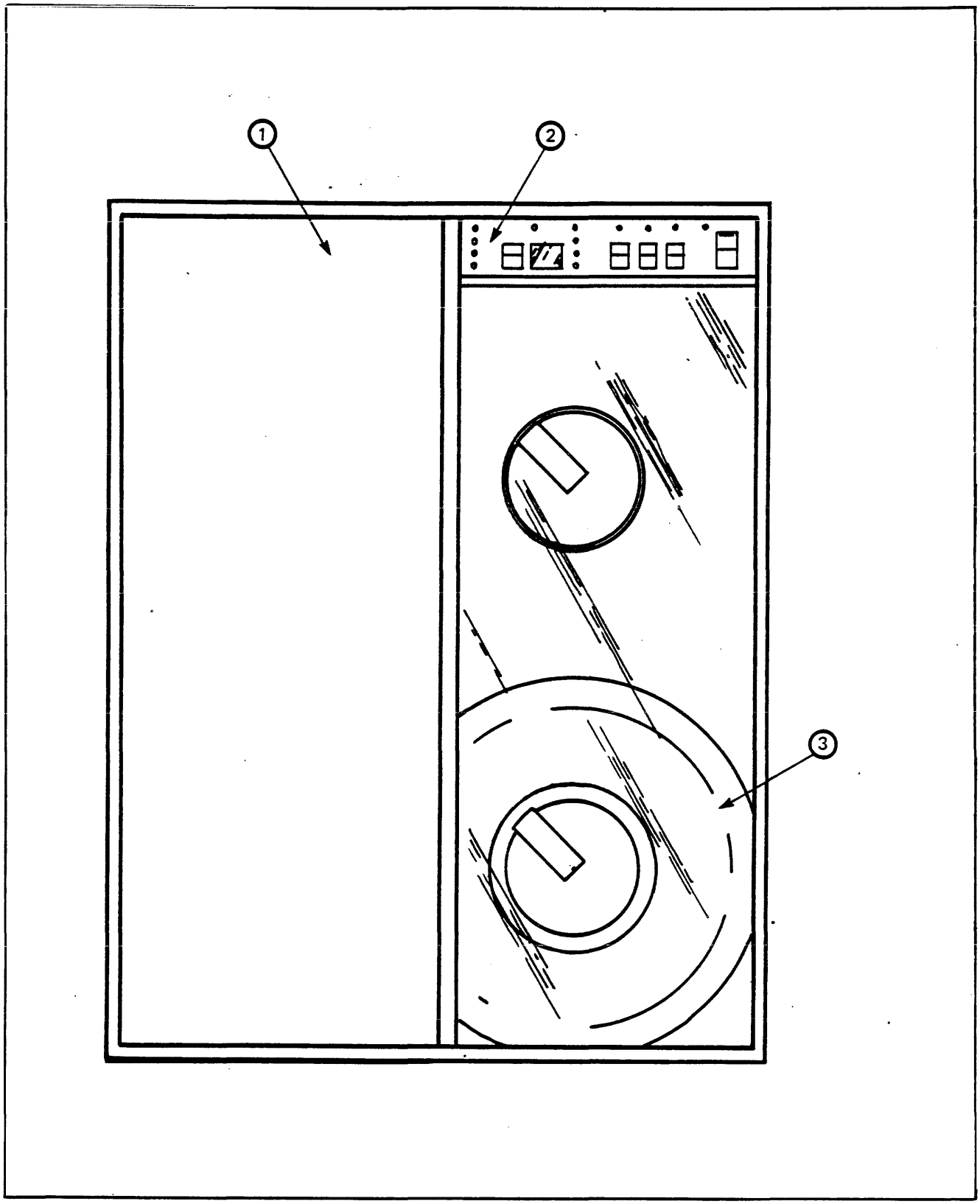


Figure 5-1

Front View 9400

PARTS LIST

Item No.	Part No.	Description	Notes
1-1	190-5654-001	Door Assy	
1-2	391-5736-001	Dust Cover Hinge	
1-3	191-2939-001	Hinge Pin	
1-4	404-5662-001	Deck Assy	
1-5	198-5699-001	Capstan Wheel	
1-6	198-0018-001	Takeup Vacuum Column Cover	
1-7	198-5675-001	Takeup Vacuum Column Assy	
1-8	190-5732-001	Split Tape Guide Assy, Ceramic	
1-9	291-2775-009	Magnetic Head Cover	
1-10A	198-2399-025	Head and Head Mount Assy, 9 track	1
	198-2399-026	Head and Head Mount Assy, 7 track	1
1-11	*198-5906-002	IR Sensor EOT/BOT	
1-13	190-5750-001	Tape Cleaner Assy	
1-14	198-0017-001	Supply Vacuum Column Cover	
1-15	128-0156-001	Catch, Vacuum Column Cover	
1-16	198-5674-001	Supply Vacuum Column Assy	
1-17	190-5655-002	Test Panel Assy, Dual Density	
1-17	190-5655-003	Test Panel Assy, Dual Density, 45 ips	
1-18B	198-0110-001	Reel Hub Assy, Quick Release	1,2
1-19	198-5687-002	Pushbutton Control Panel Assy	
1-20	190-5658-001	Control Panel Cover Assy	
1-20	190-5658-002	Control Panel Cover Assy with Density Select Switch	
1-21	151-0034-001	Thumbwheel Switch, 1 to 4 (parallel)	
1-22	125-0085-001	Tape Guide	
1-23	128-0153-001	Adjustable Grip Latch	

*Replaces 198-1138-001, LP/EOT Photosensor, and 198-1139-001 BT Photosensor, after SN 5262. (198-5906-002 includes 190-5303-002 Connector board.)

NOTES

1. These parts have detailed parts views on following page.

2. Assembly includes shims for setting hub clearance. Refer to paragraph 4.9.1 of O/M manual for adjustment procedure.

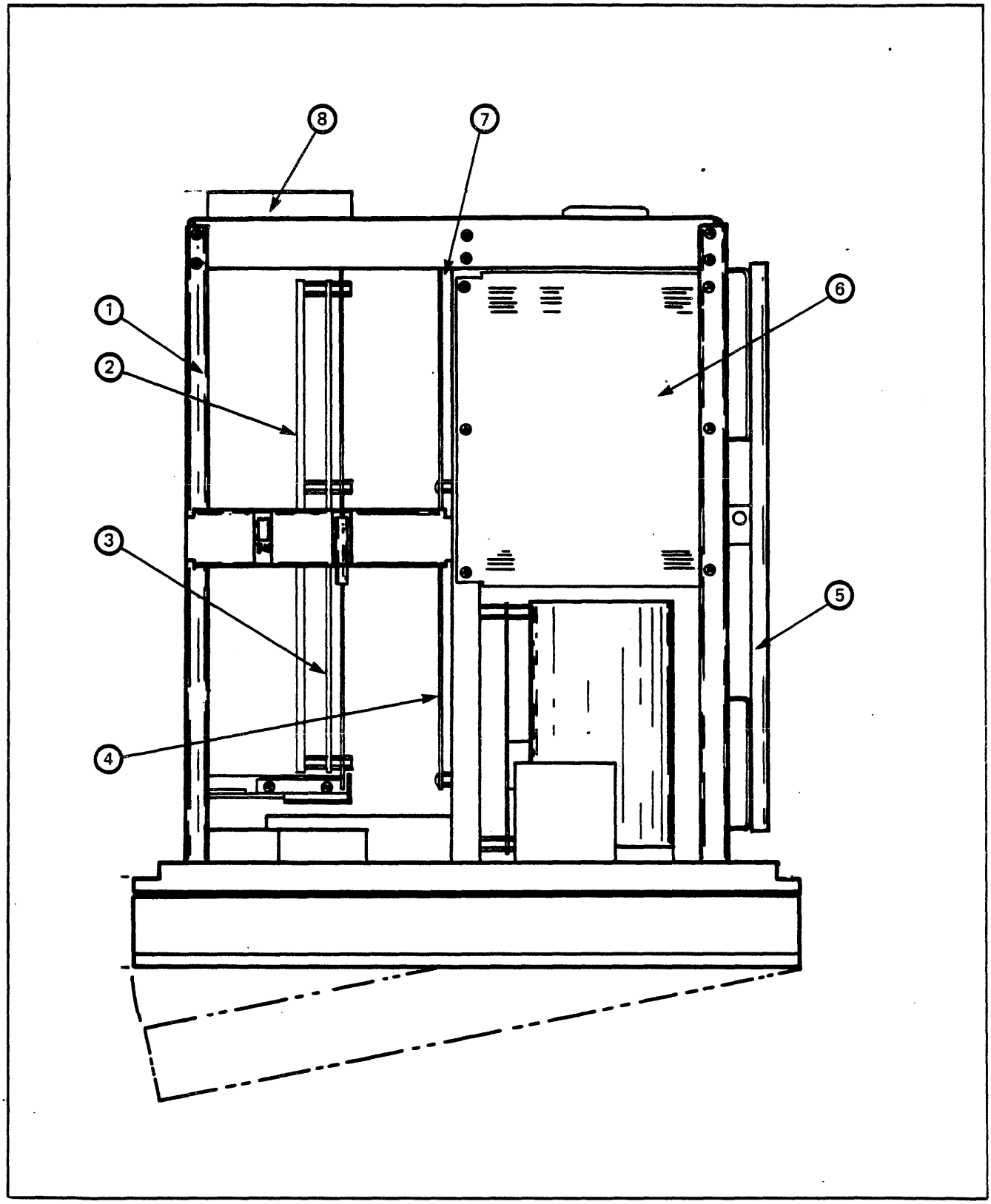


Figure 5-2

Top View 9400

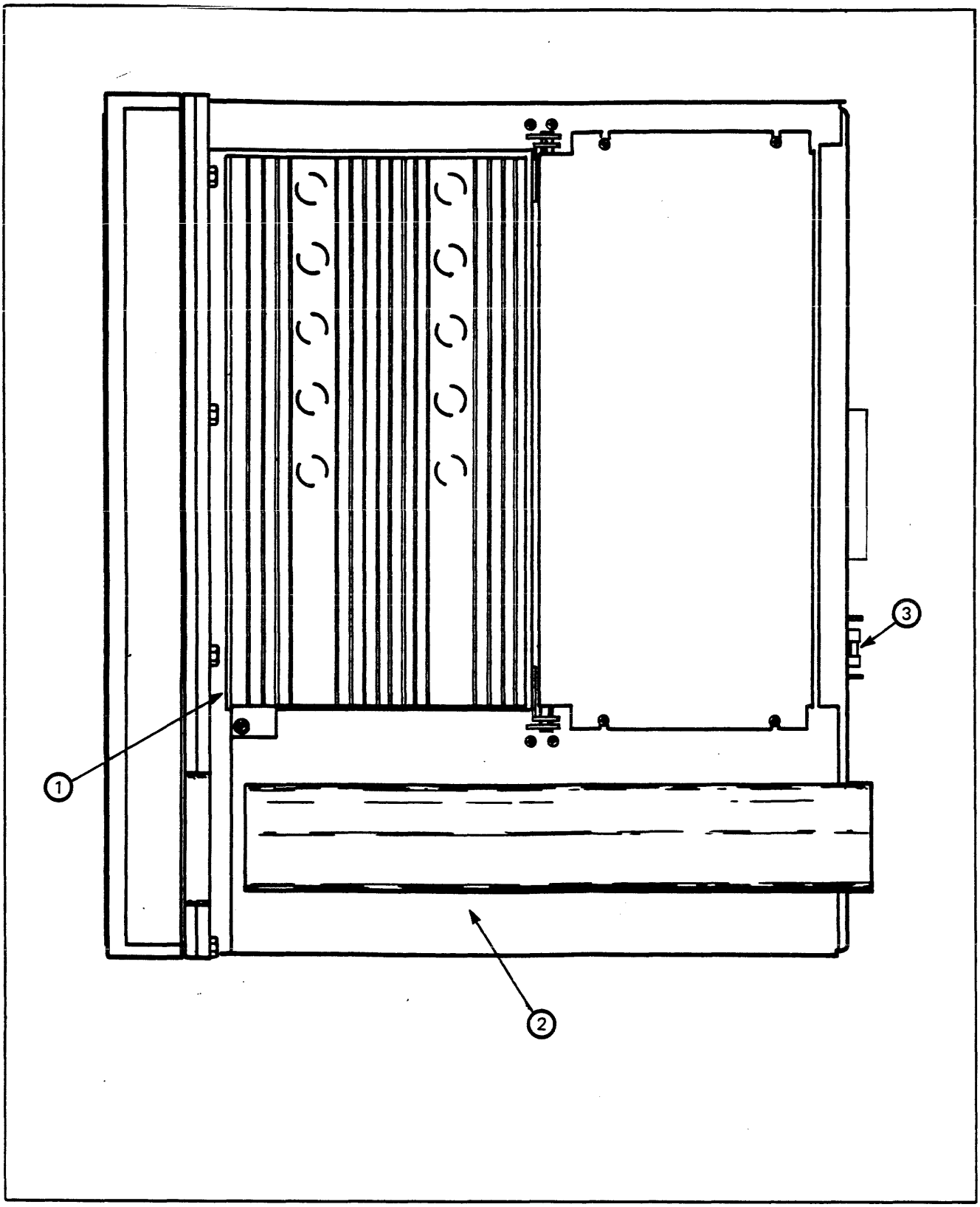


Figure 5-3

Side View 9400

SIDE VIEW (See FIGURE 5-4)

Item No.	Part No.	Description
1	190-5846-003	Assembly, Blower 110 VAC 60 Hz
	190-5846-004	Assembly, Blower 220 VAC 50 Hz
	190-5846-005	Assembly, Blower 240 VAC 50 Hz
2	291-6721-001	Elbow, Blower
3	126-0001-003	Blower, Belt Drive

TOP VIEW (See FIGURE 5-5)

Item No.	Part No.	Description
1	115-0018-001	Capacitor, Motor Start 110 VAC 60 Hz
	115-0018-002	Capacitor, Motor Start 240 VAC 50 Hz
	115-0018-002	Capacitor, Motor Start 220 VAC 50 Hz
2	190-6695-001	Blower Harness
3	148-0131-006	Power Triac
4	145-0017-001	Motor Start Relay 110 VAC 60 Hz
	145-0017-002	Motor Start Relay 220/240 VAC 50 Hz

BOTTOM VIEW (See FIGURE 5-6)

Item No.	Part No.	Description
1	491-6717-001	Blower Deck Assembly
2	291-5845-101	Vacuum Blower Drive Ply Alt, 0-4K;3.02
	291-5845-103	Vacuum Blower Drive Ply Alt, 0-4K;3.63
3	128-1000-064	Screw, Socket Head 6-32 x 0.50 lg, 3 Places
4	135-0056-001	Endless Belt 0.5 w x 20.0 lg
	135-0056-002	Endless Belt 0.5 w x 21.0 lg

Table 5-2
9400 Blower Assembly

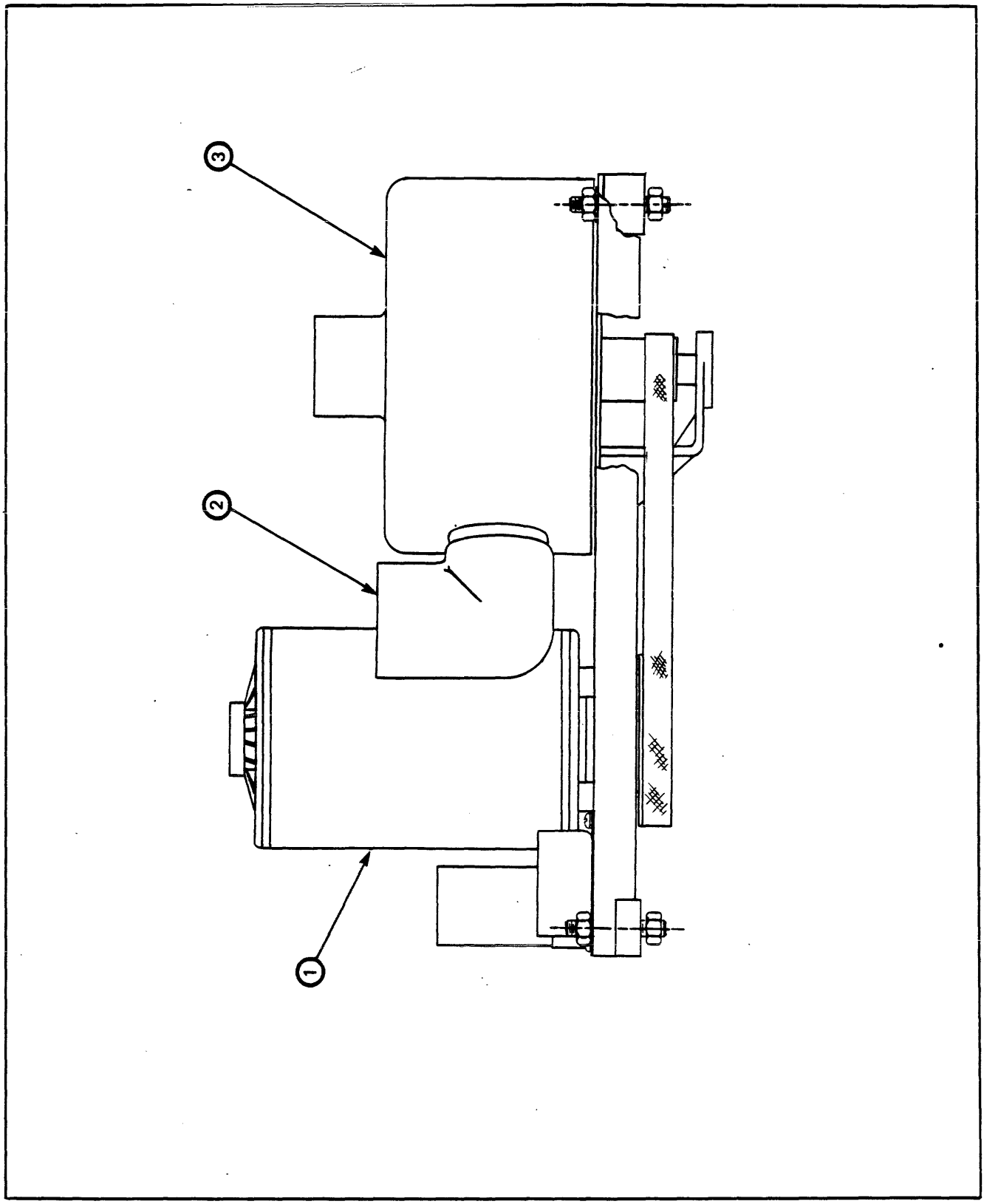


Figure 5-4

Blower Assembly, Side View

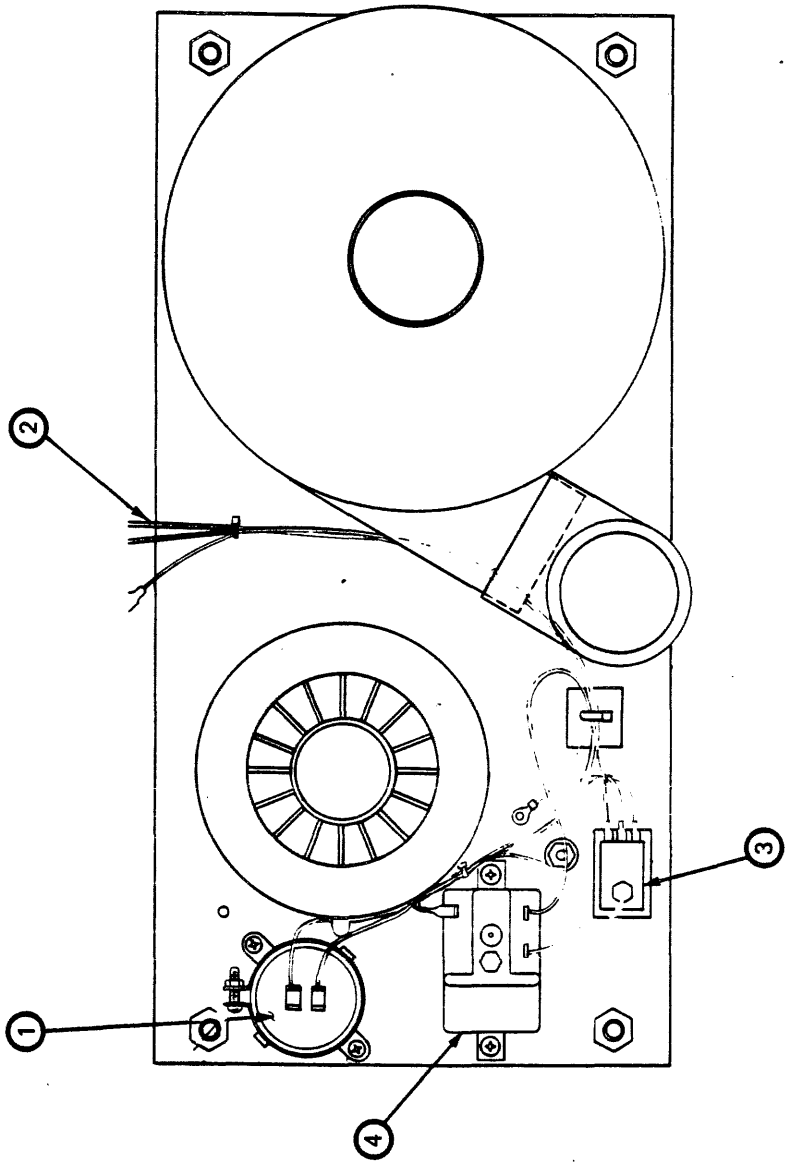


Figure 5-5

Blower Assembly, Top View

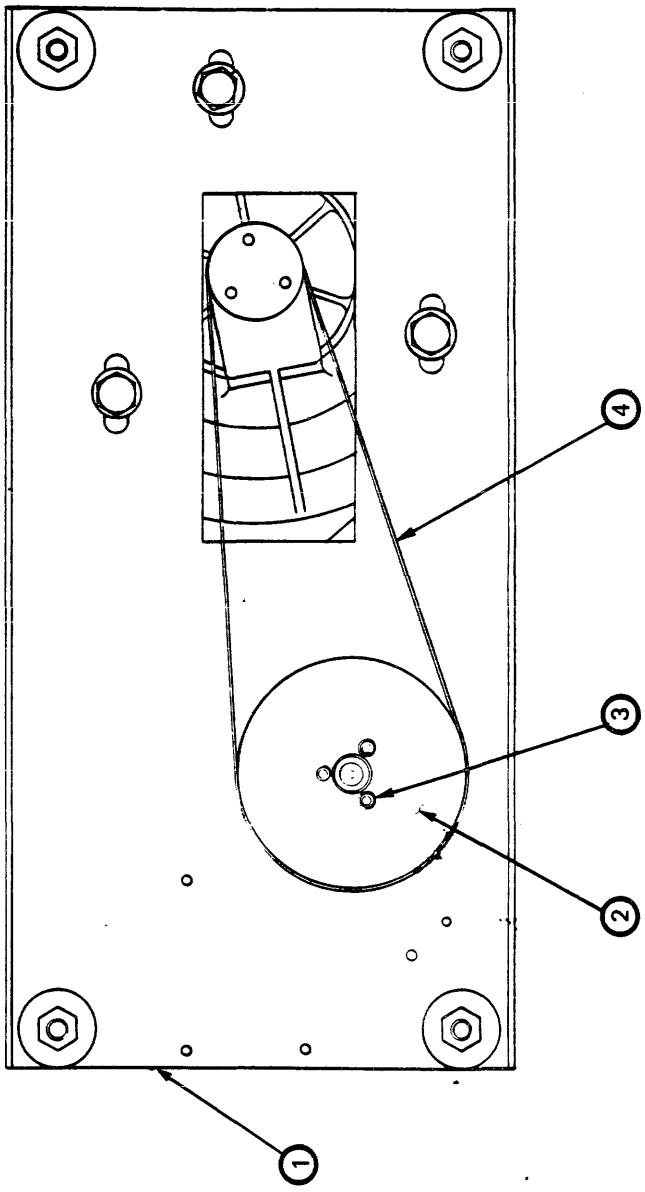


Figure 5-6

Blower Assembly, Bottom View

READ DATA HANDLER ASSEMBLY (See FIGURE 5-7)

Item No.	Part No.	Description
1	121-0211-101	Berg Single Row 1 Pin
2	146-0529-001	Map, ROM
3	149-0182-001	IC, 2910
4	149-2925-001	IC, Clk Gen; 2925
5	149-2903-001	IC, MPU; 4 Bit Slice BPLR
6	149-2705-001	IC, RAM 16 x 4 29705
7	146-0525-001	IC, ROM
8	121-0165-027	Connector, 26 Pin
9	121-0253-005	Connector, 5 Pin
10	121-0213-150	Berg, Double Row 50 Pin
11	121-0165-022	Connector, 50 Pin
12	121-0165-028	Connector, 26 Pin
13	121-0213-124	Berg, Double Row 24 Pin
14	121-0213-106	Berg, Double Row 6 Pin
15	121-0211-103	Berg, Double Row 3 Pin
16	121-0211-102	Berg, Double Row 2 Pin
17	121-0213-120	Berg, Double Row 20 Pin
18	121-0213-122	Berg, Double Row 22 Pin

ASSEMBLY, ANALOG READ/WRITE (See FIGURE 5-8)

Item No.	Part No.	Description
1	121-0165-014	Connector, 24 Pin
2	121-0253-005	Header, 5 Position
3	190-4901-009	Transistor Mtg Kit
4	121-1215-026	Connector, 26 Position
5	121-0165-122	Connector, 20 Position
6	121-0165-026	Connector, 40 Position
7	160-0122-050	Jumper, 84 Places
8	121-0200-001	Terminal, 84 Places

ASSEMBLY, READ PREAMPLIFIER PC BOARD (See FIGURE 5-9)

Item No.	Part No.	Description
1	121-0256-002	Socket Connector, 2 Position
2	121-0213-134	HDR, Connector, 34 Pin
3	118-0003-002	Filter, XMR, Choke
4	160-0084-001	Bus Bar/Shield
5	121-0213-226	HDR, 26 Pin

ASSEMBLY, SERVO BOARD (See FIGURE 5-10)

Item No.	Part No.	Description
1	121-1155-004	Connector, 4 Pin
2	121-0252-009	Connector, 9 Pin
3	160-0122-060	Jumper 4 Places
4	160-0122-050	Jumper 3 Places
5	145-0005-024	Relay
6	121-0252-005	HDR, 5 Position
7	121-0252-005	HDR, 5 Position
8	148-0178-200	XSTR, MCR 72-4
9	148-0143-001	XSTR, Darl
10	121-0265-012	Connector, 50 Pin

Table 5-3
9400 PC Board Assemblies

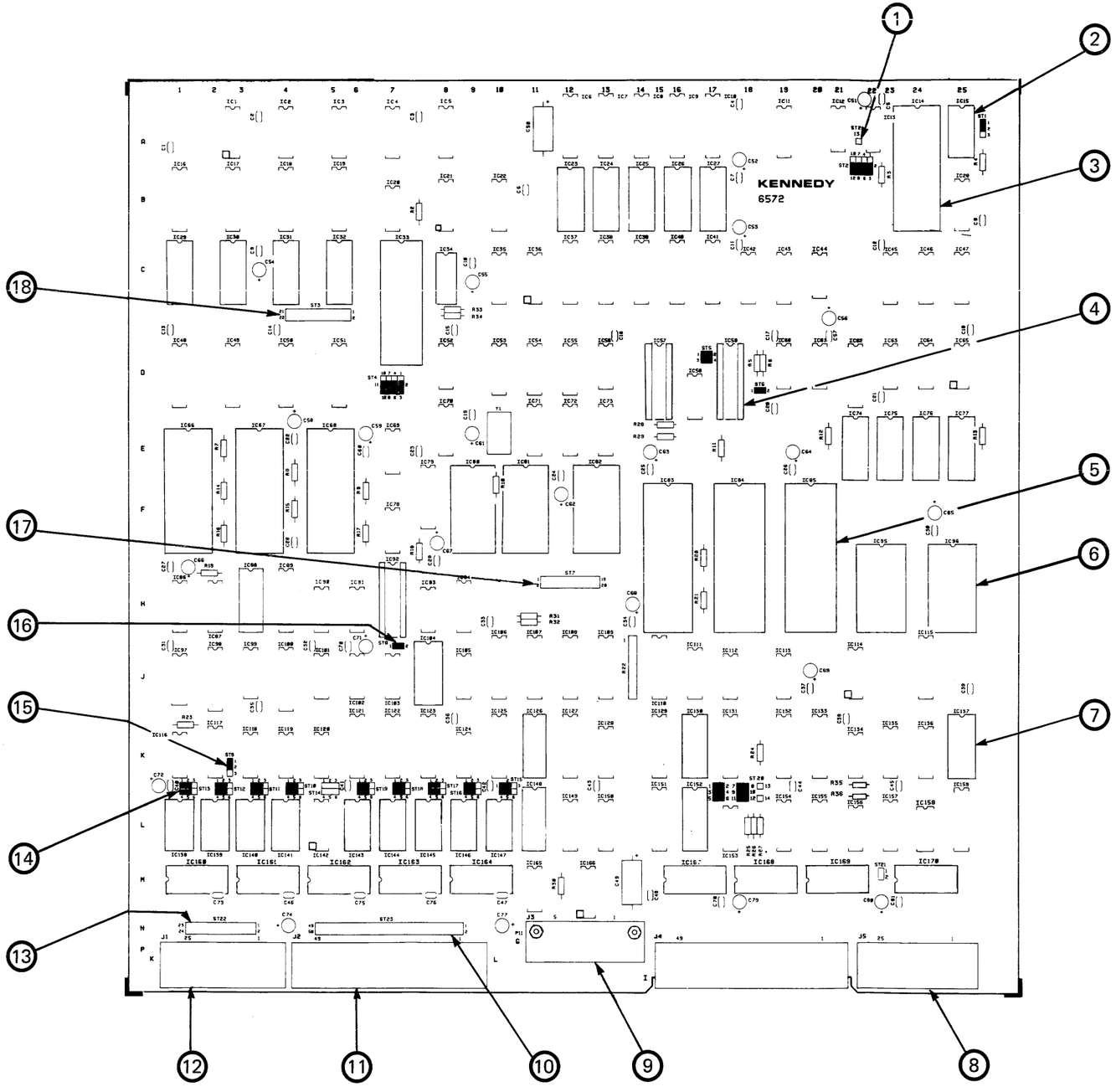


Figure 5-7
Read Handler

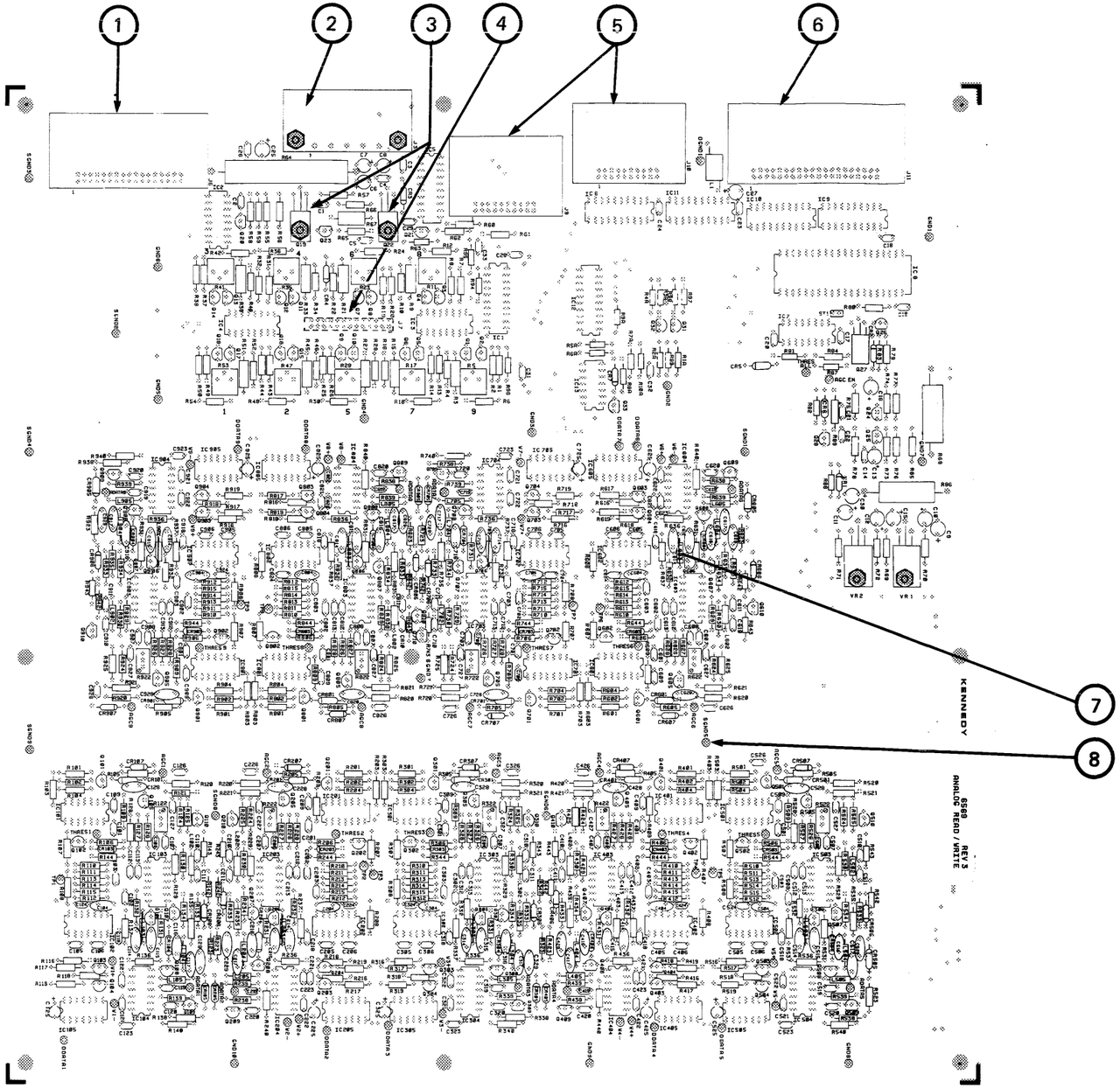


Figure 5-8

Analog Write Board

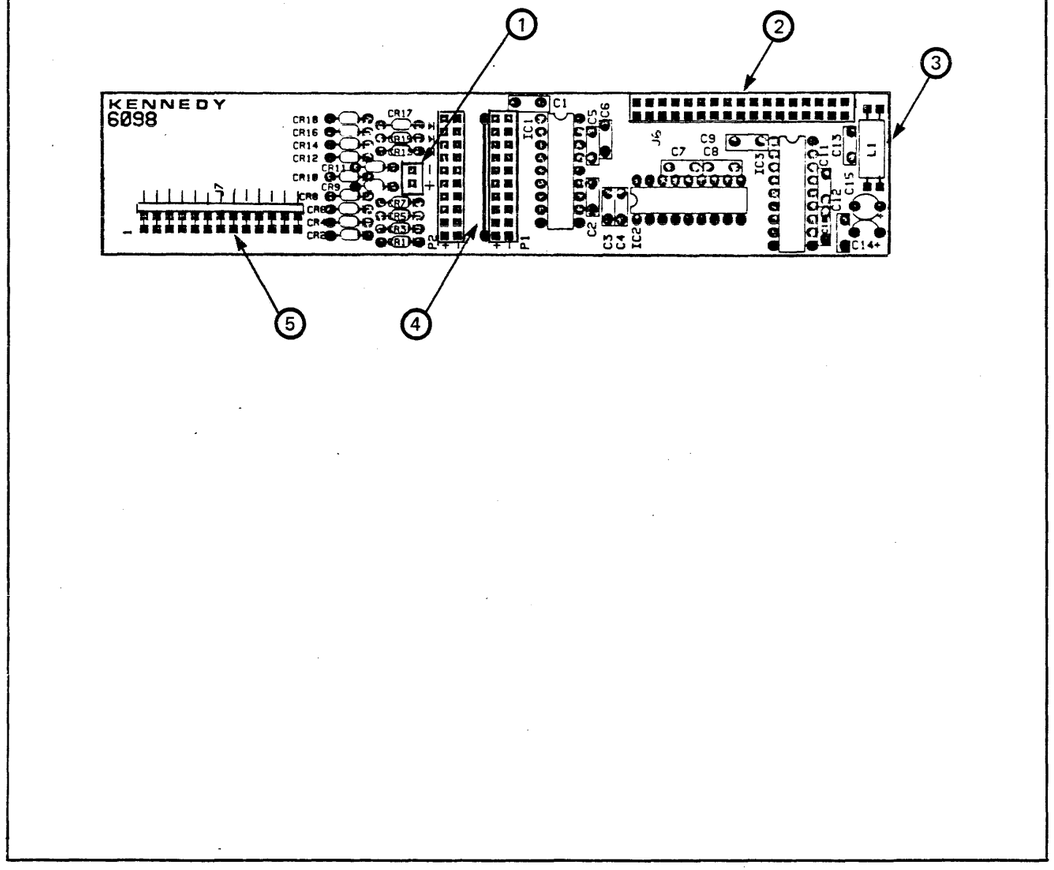


Figure 5-9
Read Pre-Amp

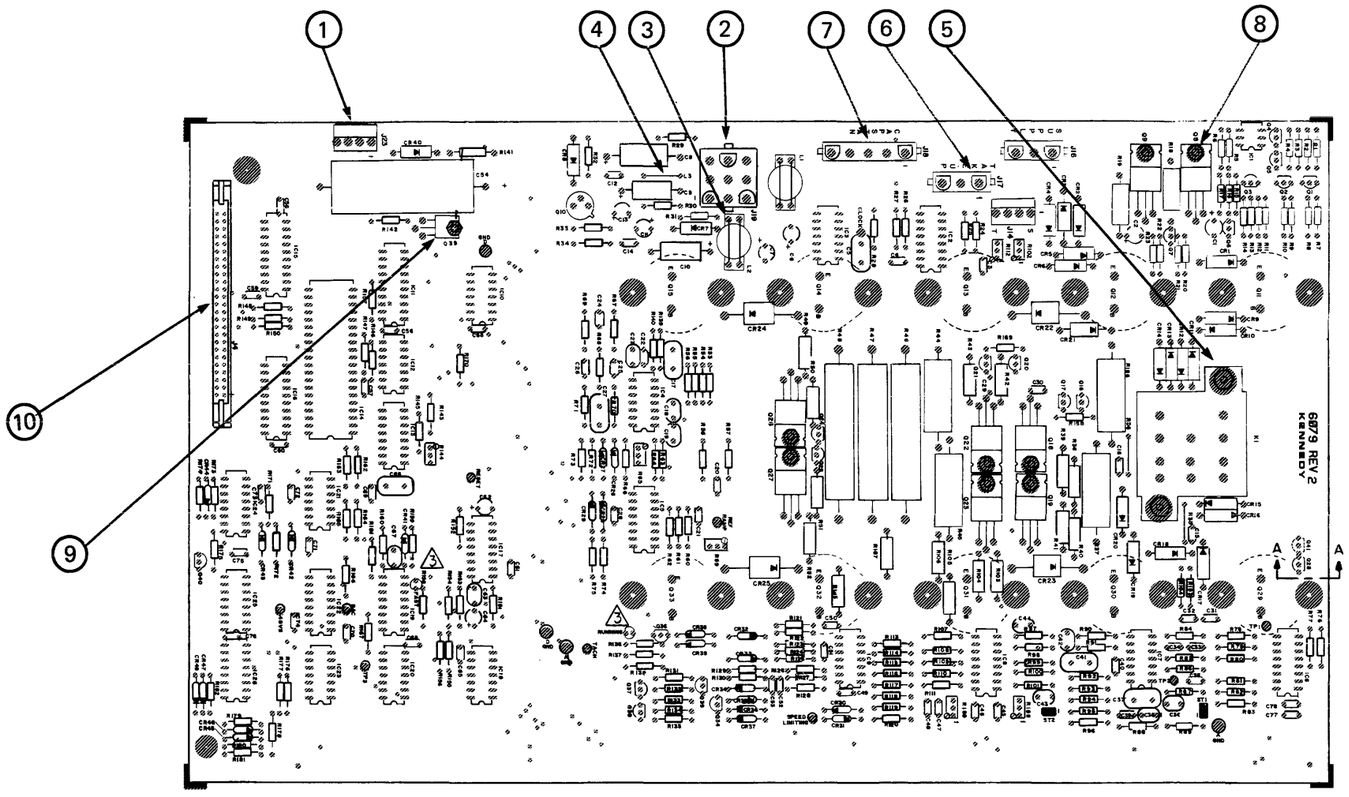


Figure 5-10
Servo Board

ASSEMBLY, POWER SUPPLY CONTROL BOARD (See FIGURE 5-11)

Item No.	Part No.	Description
1	148-0131-006	Transistor, Triac, MAC10-6
2	121-0252-009	Header, 9 Position
3	121-0001-001	Terminal, TP
4	121-0252-005	Connector, 5 Position
5	128-5006-006	Screw, 6-32, Pan Head 4 Places
6	121-0079-001	Terminal, Male 10 Places
7	121-0079-002	Terminal, Female 7 Places
8	121-0165-510	Connector, 10 Pin
9	128-5010-004	Screw, 10-32 Pan Head 4 Places
10	190-4702-001	Assembly, Triac

ASSEMBLY, PROCESSOR/WRITE (See FIGURE 5-12)

Item No.	Part No.	Description
1	121-0206-225	Connector, 25 Position
2	121-0213-108	Berg, 8 Pin 2 Places
3	121-0234-050	Connector, 50 Position 2 Places
4	121-0211-101	Berg, 1 Pin 3 Places
5	121-0165-026	Connector, 40 Pin
6	121-0212-001	Jumper, 1 Position 24 Places
7	121-0213-106	Berg, 6 Pin, 9 Places
8	121-0200-001	Terminal 22 Places
9	121-0165-122	Connector, 20 Pin
10	121-0211-102	Header, 2 Pin
11	190-4901-009	Transistor, Mtg Kit
12	121-0111-102	Header, 2 Pin
13	121-1156-002	Header, 2 Pin
14	121-1156-004	Header, 4 Position
15	121-0165-004	Connector, 26 Pin
16	121-0165-002	Connector, 50 Pin
17	121-0253-005	HDR 5 Position
18	121-0165-510	HDR 10 Position
19	121-0213-118	HDR Double Row 18 Pin

Table 5-3
9400 PC Board Assemblies (continued)

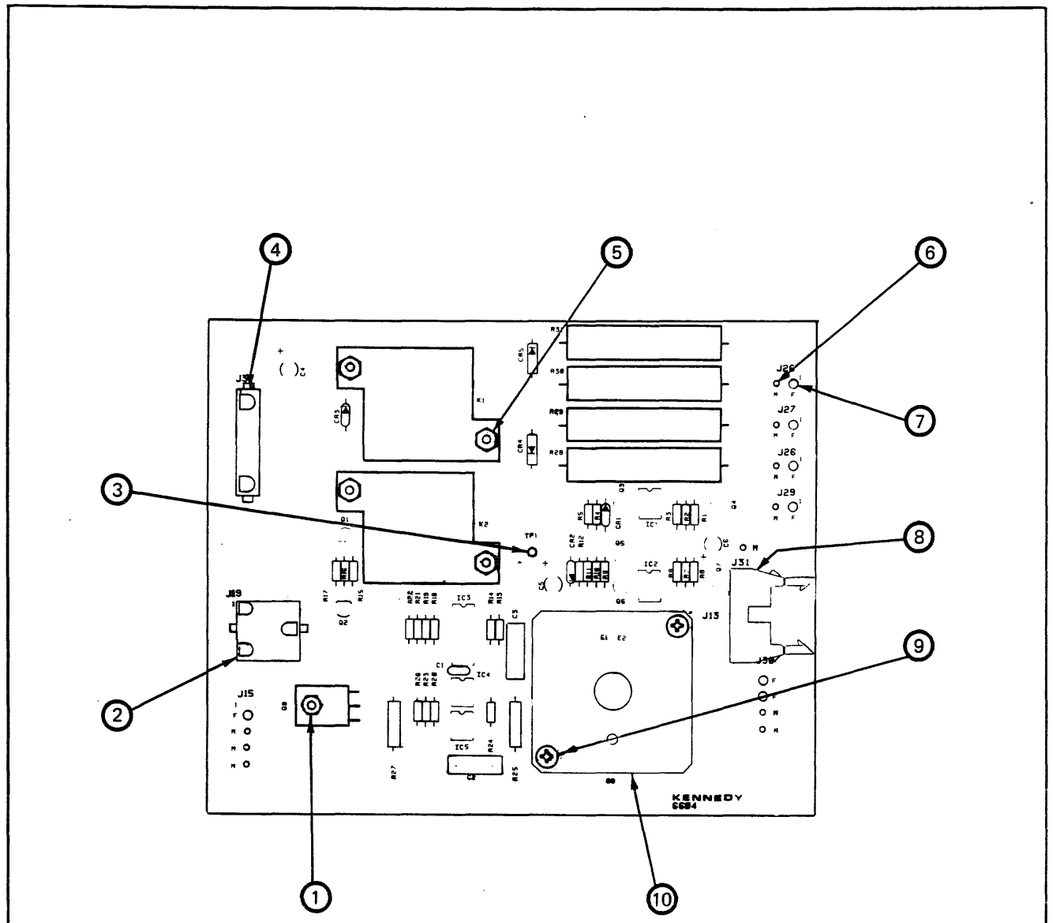


Figure 5-11
Power Supply Control Board

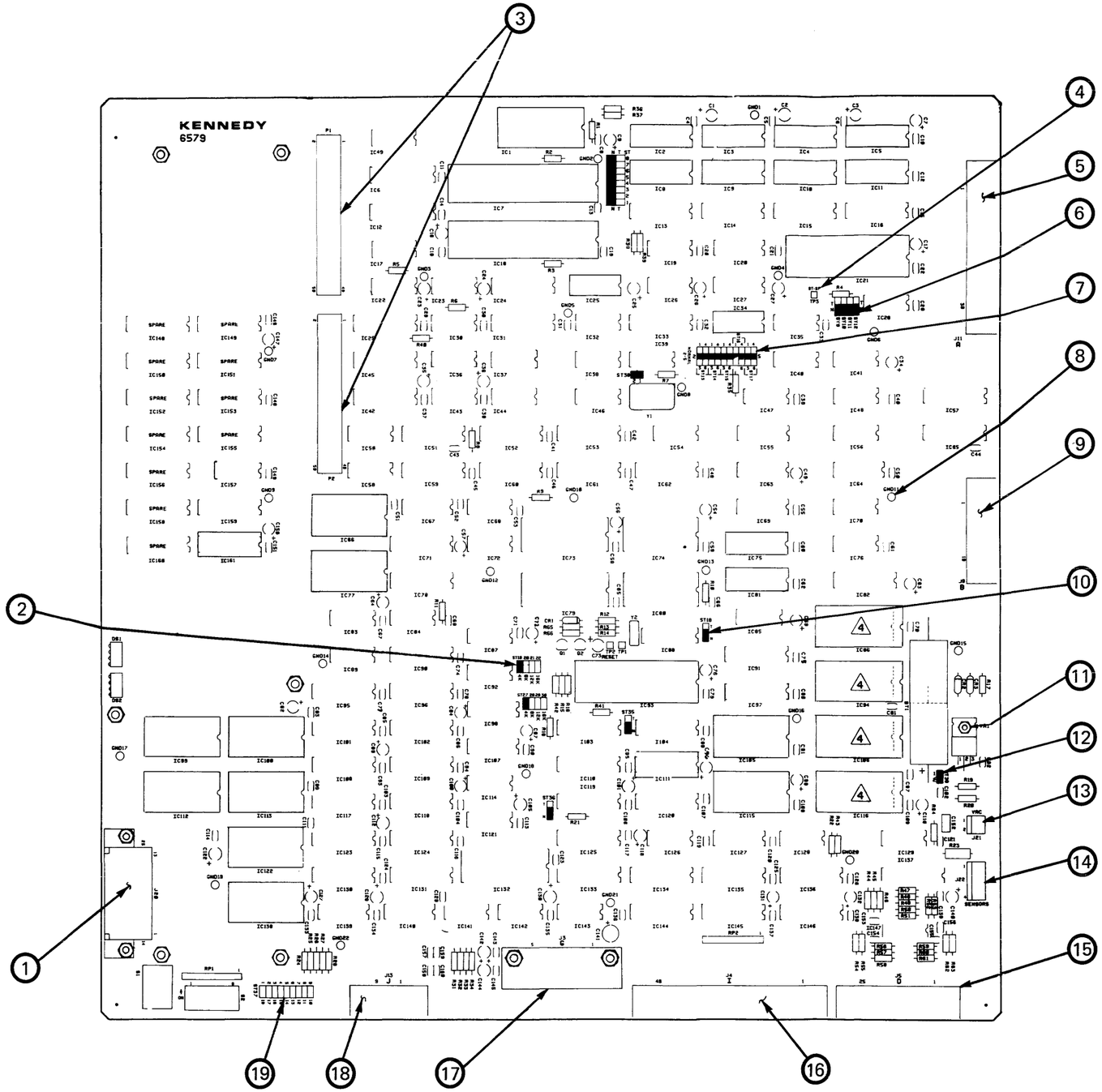


Figure 5-12
Processor Board

READ DECODER I ASSEMBLY (See FIGURE 5-13)

Item No.	Part No.	Description
1	149-0337-220	IC, Regulator-1, LM337
2	121-0211-102	Berg Stik, 2 Pin 6 Places
3	121-0165-102	Connector, 20 Pin
4	121-0212-001	Jumper, 7 Places
5	121-0165-002	Connector 50 Pin
6	121-0211-101	Berg, 5 Position
7	121-0253-005	Header, 5 Position
8	121-0165-028	Connector, 26 Pin

READ DECODER II ASSEMBLY (See FIGURE 5-14)

Item No.	Part No.	Description
1	121-0211-102	Berg, Stik, 2 Pin
2	149-0337-220	IC, Regulator, 37v
3	121-0212-001	Jumper, 14 Places
4	121-0211-101	Berg, Stik, 1 Pin
5	121-0165-028	Connector 26 Pin
6	121-0253-005	Connector 5 Position
7	121-0165-002	Connector 50 Pin
8	121-0165-102	Connector 20 Pin

KEYBOARD PC BOARD ASSEMBLY (See FIGURE 5-15)

Item No.	Part No.	Description
1	151-0084-001	Switch, Button 9 Places
2	121-0237-026	Connector
3	128-0217-002	Spacer, 13 Places
4	148-0181-001	LED, Red, DS7,8,9,10,11
	148-0182-001	LED, Green, DS2,3,12,13
	148-0183-001	LED, Yellow, DS1,4,5,6
5	139-0031-001	Display, LED, MAN-72A

KEYBOARD DECODER ASSEMBLY (See FIGURE 5-16)

Item No.	Part No.	Description
1	121-0265-202	Connector, 40 Pin
2	121-0234-026	Connector, Skt 26 Position
3	121-1155-002	HDR, Connector, 2 Pin
4	121-1158-002	HDR, Connector, 2 Position

Table 5-3
9400 PC Board Assemblies (continued)

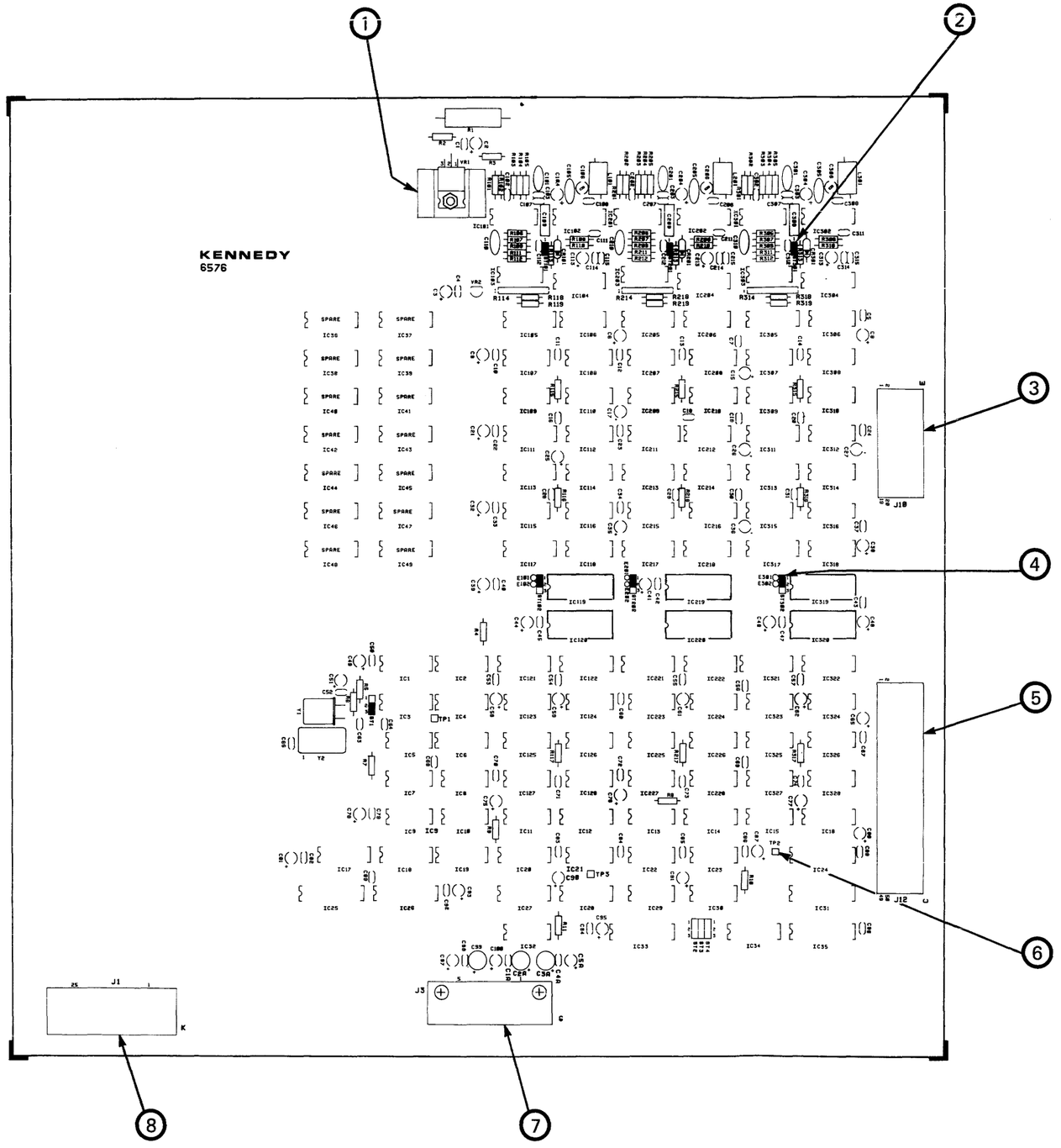


Figure 5-13
Decoder I Board

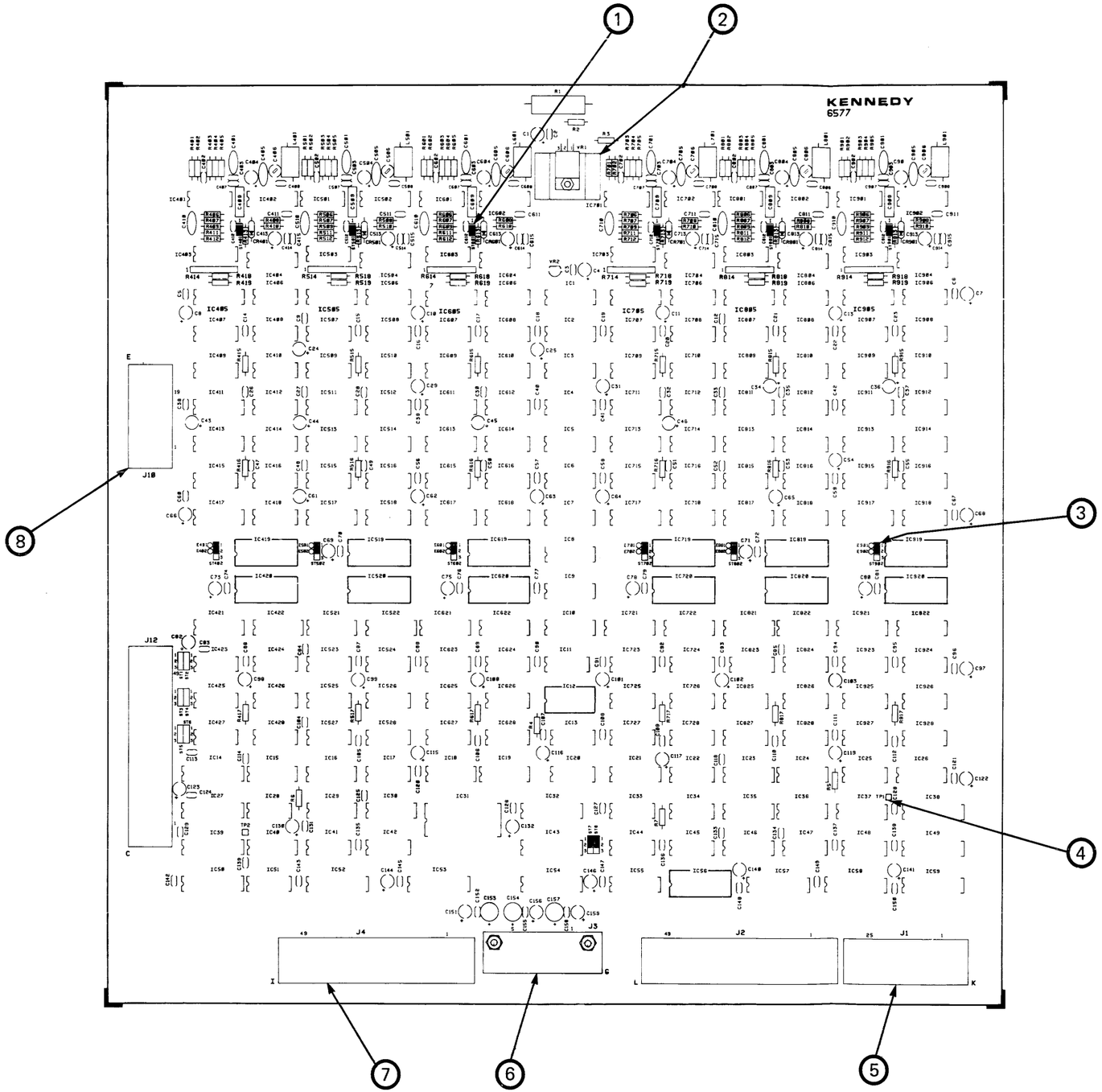


Figure 5-14
Decoder II

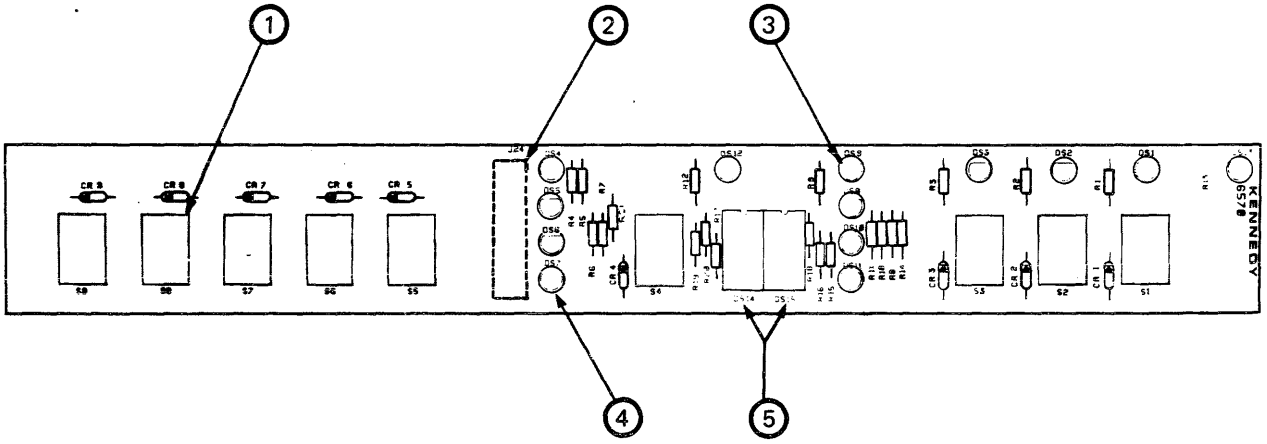


Figure 5-15

Keyboard PCB Assembly

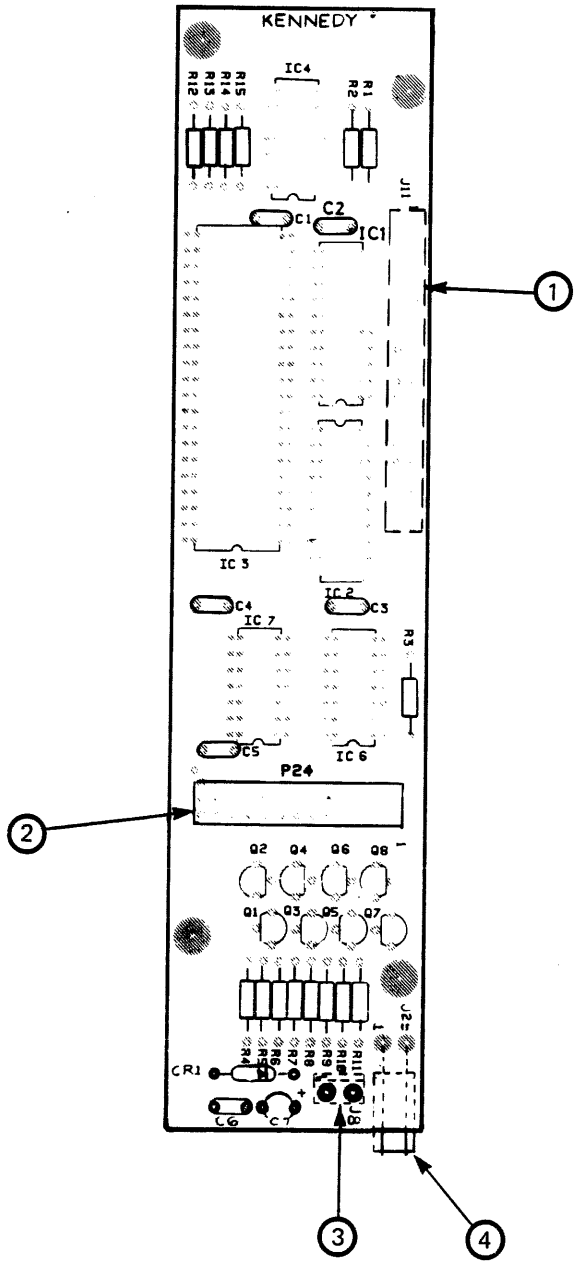


Figure 5-16

Keyboard Decoder

RECOMMENDED SPARE PARTS LIST

Part No.	Description	Qty	Unit Dash No.
135-0056-001	Endless Belt 0.5 w x 20.0 lg	1	001,4,7,10
135-0056-002	Endless Belt 0.5 w x 21.0 lg	1	002,3,5,6,8,9,11,12
121-0198-003	Power Cord 115 VAC 60 Hz	1	001,4,7,10
121-0198-004	Power Cord 240 VAC, 50 Hz	1	003,6,9,12
121-0198-004	Power Cord 220 VAC, 50 Hz	1	002,5,8,11
291-5845-101	Pully, Vacuum Blower Drive Alt 0-4K, 3.20	1	001,4,7,10
291-5845-103	Pully, Vacuum Blower Drive Alt 0-4K, 3.630	1	002,3,5,6,8,9,11,12
190-5675-001	Assembly, Takeup Vacuum Column	1	
190-5720-002	Supply, Cover Frame Assembly	1	
190-5906-003	Assembly, Sensor (EOT/BOT)	1	
190-5674-002	Assembly, Supply Vacuum Column	1	
190-5720-001	Takeup Cover Frame Assembly	1	
151-0064-001	Vacuum Switch	1	
190-6811-001	Assembly, Tape Guide	1	
190-6640-001	Assembly, File Protect	1	
291-6590-001	Capstan Wheel	1	
190-6812-001	Tape Cleaner	1	
145-0017-001	Relay, AC Starter MTR 115 VAC 60 Hz	1	001
145-0017-002	Relay, AC Starter MTR 220/240 VAC 50 Hz	1	002,3
190-4702-001	Triac Assembly	1	
190-6719-001	Fan Kit 115v 60Hz	1	001,4,7,10
190-6719-002	Fan Kit 220/240v 50 Hz	1	002,3,5,6,8,9,11,12
113-0008-001	Reel, Empty 10.5"	1	
198-0100-002	Hub Repair Kit	1	
198-0021-001	Brush Replacement Kit (Capstan Motor, 2 Brushes)	1	
128-0156-001	Catch, Vacuum Column	1	
115-0018-001	Capacitor, Motor Start	1	001
115-0018-002	Capacitor, Motor Start	1	002,3
190-4721-001	Capstan Motor	1	
190-4778-002	Latch Assembly	1	
190-5232-001	Capstan Motor Cable Assembly	1	
190-5698-003	Reel Motor Assembly	1	
190-5906-003	EOT/BOT Sensor	1	
190-5909-003	EOT/BOT Wire Preparation	1	
190-5669-001	Sensor Assembly	1	
190-6260-001	Column Sensor Wire Preparation	1	
190-6711-001	Vacuum Plenum Assembly	1	
190-6640-001	File Protect Assembly	1	
190-6645-001	Servo Harness	1	
190-6657-001	Column Cable	1	
190-6730-001	Mag Head Cover Assembly	1	
190-6701-001	Dust Cover Assembly	1	
190-6571-001	Keyboard Decoder	1	
190-6570-001	Keyboard PC Board Assembly	1	
190-6718-001	Mag Head Assembly	1	

RECOMMENDED SPARE PARTS LIST
(Continued)

190-6098-001 Preamplifier PC Board Assembly

Part No.	Description	Qty	Unit Dash No.
118-0003-002	Chocke	10	
121-0213-134	HDR Double Row	1	
121-0213-226	HDR Right Angle	1	
149-3467-001	IC, Preamplifier 3467	10	

190-6569-001 Assembly, Analog Read/Write

Part No.	Description	Qty	Unit Dash No.
118-0006-104	Inductor, 1 mh	5	
118-0006-153	Inductor, 150 mh	5	
148-0171-001	JFET, J112	10	
148-0258-001	Transistor 2N4258	10	
149-0317-220	Regulator +37v	10	
149-0337-220	Regulator -37v	10	
149-2408-001	DAC 8 Bit, DAC 08	10	
149-8255-005	Peripheral Inter 8255A-5	10	

190-6572-001 Assembly, Read Data Handler

Part No.	Description	Qty	Unit Dash No.
149-0181-002	FIFO, S3341	10	
149-0060-003	74S85 Comparator	10	
149-0121-001	74S133 13 Input Nand	10	
149-0176-002	74S280 Parity Gen/Checker	10	
149-0191-002	74S244 Line Driver	10	
149-0194-002	74S299 SR Bidirectional	10	
149-0200-001	XTL Osc 34 5600 MHz	5	
149-0225-002	JK F-F 741S109	10	
149-0238-002	2 Input NAND 74S38		
149-0377-001	741S377 Flip-Flop	10	
149-0378-001	741S378 HEX-DECI F-F	10	
149-0640-001	741S640 XCVR	10	
149-2125-001	741S125 Buffer	10	
149-2140-001	74S140 NAND	10	
149-2520-001	AM29520 Register	10	
149-2705-001	AM29705 Dual Port RAM	10	
149-2901-001	AM2901 Bit Slice Proc	10	
149-2902-001	AM2902A Look Ahead Carry Gen	10	
149-2903-001	AM2903 Bit Slice Proc	10	
149-2925-001	AM2925 Clock Generator	10	

190-6576-001 Read Decoder I, 3 Channel

Part No.	Description	Qty	Unit Dash No.
128-0219-001	Heat Sink	5	
149-0135-002	741S191 Counter	10	
149-0200-002	XTL Osc 26.04096	5	
149-7404-001	Hex Inv CMOS 74HC04	10	

190-6577-001 Read Decoder II, 6 Channel

Part No.	Description	Qty	Unit Dash No.
149-8253-005	8253-5 Counter/Timer	10	

RECOMMENDED SPARE PARTS LIST
(Continued)

190-6579-001 Processor/Write PC Board

Part No.	Description	Qty	Unit Dash No.
139-0030-001	LED Array	10	
148-0177-001	JFET P Channel	10	
149-0196-001	Counter 74S569	10	
149-0255-001	Decoder 741S255	10	
149-1488-001	RS232 Driver 1488	10	
149-1489-001	RS232 Rec 1489	10	
149-2008-020	SRAM 4016	10	
149-2008-120	SCRAM 4016	10	
149-8088-001	5 MHz 8088 Mu P	10	
149-8251-001	USART 8251	10	
149-8254-001	Counter/Timer 8254-2	10	
149-8254-001	Clock Gen 8284	10	

190-6604-001 Power Supply Control Board

Part No.	Description	Qty	Unit Dash No.
148-0131-006	Triac Mac 10-6	10	
149-1156-001	Triac Moc 3010	10	
149-1157-001	Darlington Opto 4N32	10	
190-5674-002	Supply Vacuum Column Assembly	1	
190-5675-001	Takeup Vacuum Column	1	
190-5698-003	Reel Motor	1	
190-5906-003	EOT/BOT Assembly	1	

190-6079-001 Servo Assembly

Part No.	Description	Qty	Unit Dash No.
145-0005-024	Relay 10a, 24v	2	
147-0040-103	Pot 18 Turn 10K	10	
147-0040-503	Pot 18 Turn 50K	10	
148-0172-024	Suppressor 1N6289	10	
148-0175-001	XSTR NPN 13004	10	
148-0176-001	XSTR PNP 6476	10	
148-0178-200	SCR MCR 72-4	10	
148-0181-001	LED Red	10	
148-0182-001	LED Green	10	
148-0410-001	XSTR 2N4410	10	
149-0179-051	CD 4051 MUX	10	
149-0183-101	Octal Latch 741S373	10	
149-0206-101	Analog Switch HI-201	10	
149-0335-001	Temp Sensor +10 mv/c 1m 335 az	10	
149-4001-001	Quad NOR CD 4001b	10	
149-4047-001	CD 4047	10	
149-4538-001	Oneshot	10	

RECOMMENDED SPARE PARTS LIST
(Continued)

190-6570-001 Keyboard PC Board

Part No.	Description	Qty	Unit Dash No.
139-0031-001	Display MAN72A	5	
148-0183-001	LED Yellow	10	
151-0084-001	PB Switch SPDT	10	
190-6571-001	Keyboard Decoder	1	
149-8279-005	Keyboard/Display	5	
135-0043-001	Motor, Permanent Magnet	1	
113-0094-001	Mag Head, R/W, 9 Track, GCR/PE/NRZI	1	
190-5725-001	Assembly, Transformer	1	
190-6712-001	Heat Sink, Servo	1	
190-6603-001	I/O Pico Bus Assembly	1	
190-6791-001	I/O Pertec Bus Assembly	1	
190-6792-001	I/O STC Bus Assembly	1	
190-6793-001	I/O Telex Bus Assembly	1	

SECTION VI

WIRING AND SCHEMATIC DIAGRAMS

SECTION VI

NOTES TO SCHEMATICS

6.0 GENERAL

6.1 INTRODUCTION

This section contains standards which have been used in preparing schematics for this manual. Electronic symbols used in the schematic diagrams conform to ANSI Y32.2. Abbreviations conform to Mil-Std-12 unless otherwise specified. Logic symbols conform to Mil-Std-806C (ANSI Y32.14). This section also includes TTL and ECL Integrated Circuits.

6.1.1 COMPONENTS

6.1.2 RESISTORS

Resistors are given in ohms, +/-5% 1/4 w unless otherwise specified.

6.1.3 CAPACITORS

Capacitor values are given in microfarads unless otherwise specified. Electrolytic capacitors are always shown with their proper polarization and voltages.

6.2 LOGIC CONVENTIONS AND SYMBOLOGY

6.2.1 TTL LOGIC

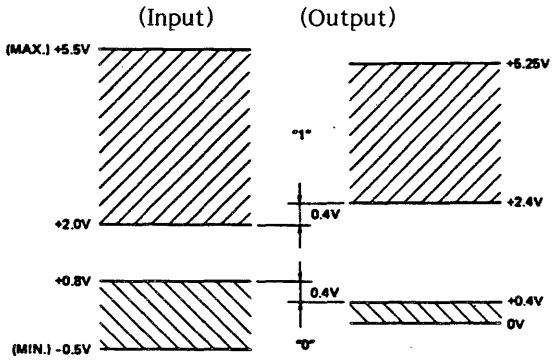
Standard IC power connections on 14 pin packages are on pins 14 (5v) and 7 (ground). For 16 pin packages, power connections are on pins 16 (5v) and 8 (ground). All nonstandard power connections are shown on the first sheet of a schematic, in the reference block.

This unit uses +5v Transistor Transistor Logic (TTL). TTL logic is defined in terms of standard POSITIVE LOGIC using the following definition.

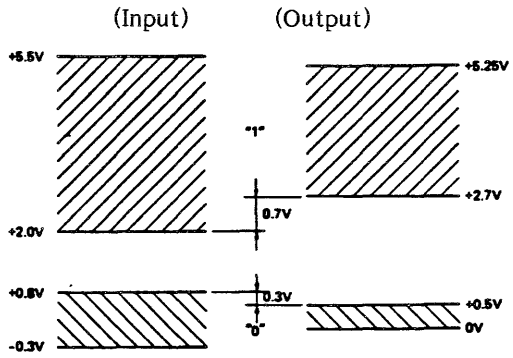
High Voltage = Logical '1'
Low Voltage = Logical '0'

The input/output logic of TTL are defined as follows:

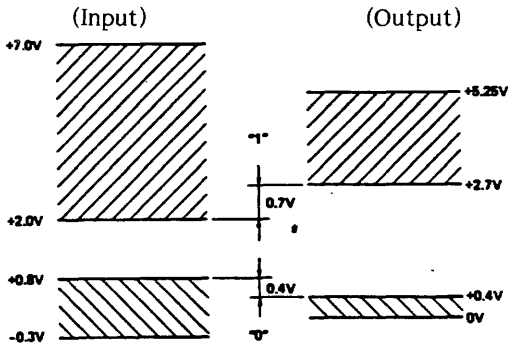
a) TTL MEDIUM SPEED IC



b) TTL SUPER HIGH SPEED IC LEVEL



c) TTL MEDIUM SPEED LOW POWER CONSUMPTION IC



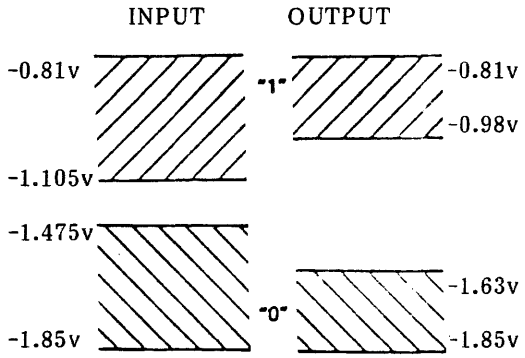
6.2.2 ECL LOGIC

The unit also uses -5.2v Emitter Coupled Logic (ECL). The high impedance of the logic (input to differential amplifier) coupled with the low impedance of the driving source (Emitter Follower Output) allows high DC fanout.

ECL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High	Voltage	=	Logical '1'
Low	Voltage	=	Logical '0'

The input/output logic levels of ECL are defined as follows:

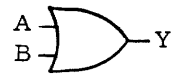


6.2.3 LOGIC SYMBOLOGY

The following conventions are provided to aid in understanding the symbology used in this manual:

1) TTL

This indicates AND gate.
Y = (A) (B)

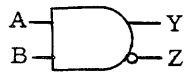


This indicates OR gate.
Y = A+B

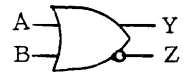
0

A circle on any input line or on the output line indicates that logical '0' is the significant state. The absence of a circle '1' is the significant state.

2) ECL



This indicates AND/NAND gate.
Y = (A) (B)= $\overline{Z}$



This indicates OR/NOR gate.
Y = A+B=$\overline{Z}$

0

This is equal to TTL LOGIC.

6.3 SCHEMATIC FLOW

The schematic diagram shall use a layout which follows the circuit, signal or transmission path, either from input to output, source to load, or in the order of functional sequence.

6.4 TEST POINTS (TP)

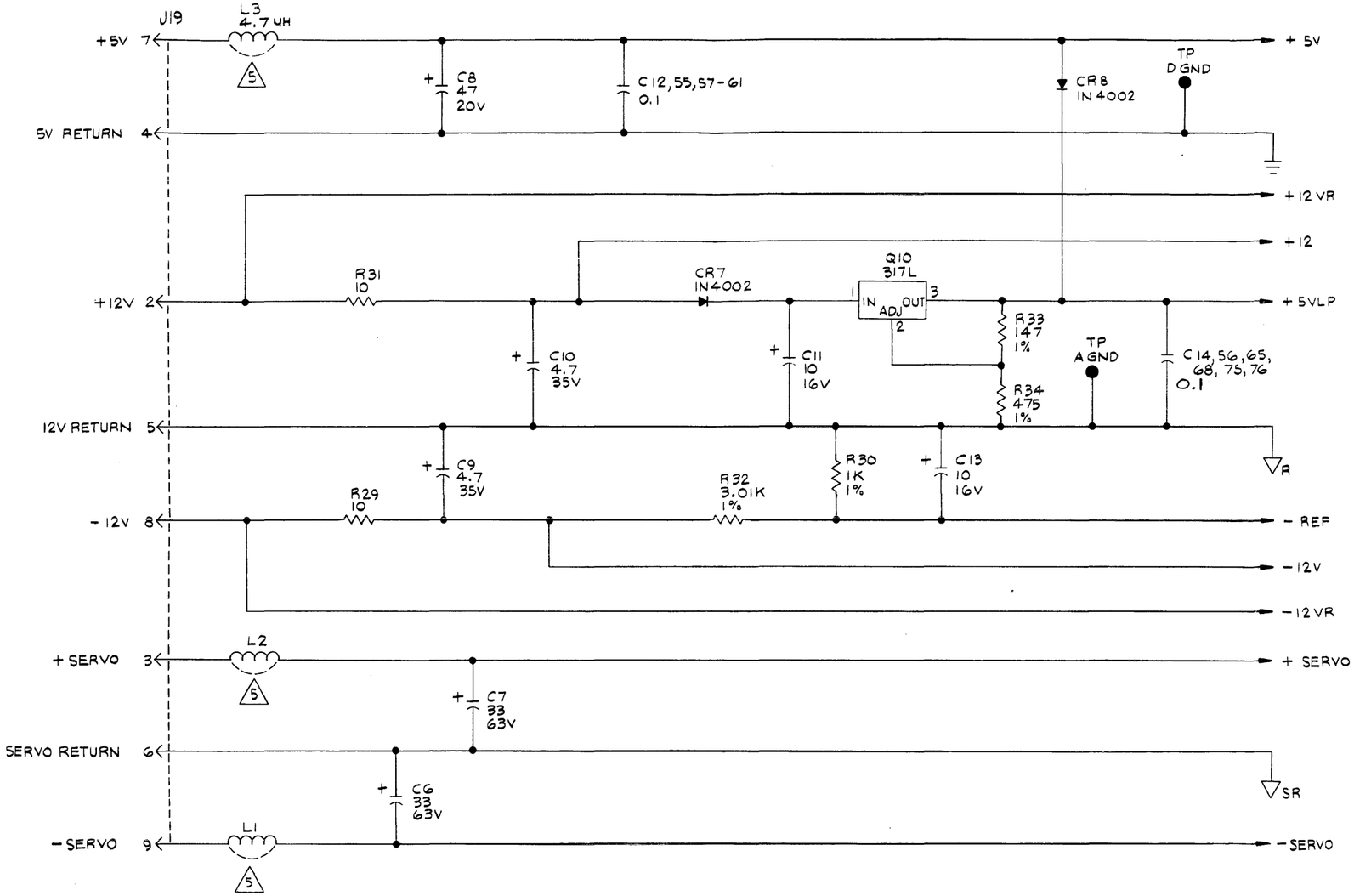
'TP' designates TEST POINTS provided on the circuit board for troubleshooting purposes.

6.5 TERMINALS

Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

6.6 IC DESCRIPTIONS

This section gives a brief description of the integrated circuit devices used throughout the 9400 system. A major portion of this section consists of small scale to large scale TTL integration , followed by Advanced Micro-devices' 2900 family of bit slices and related chips. This is followed by Intel's 8088 microprocessor and related chips. The last section in the end covers any other chips which did not fall under any of the above categories.



5 COMPONENT SHOWN FOR FULL CAPABILITY OF THE BOARD. JUMPERS USED ON THE-001 ASSY

4 TRANSISTORS MOUNTED ON HEAT SINK 404-6712-001.

3. ALL DIODES ARE IN914.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V.
1. ALL RESISTOR VALUES ARE IN OHMS ± 5% 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED.

REFERENCE DESIGNATOR	
LAST USED	NOT USED
C78	—
CR48	—
DS2	—
IC26	—
Q41	—
R189	—
TP14	—
L3	—

REF. DES.	TYPE	+5V	GND
IC10.	74LS00	14	7
IC15,16	74LS245	20	10
IC11	74LS373	20	10
IC18,23	4001B	—	—
IC20	4011	—	—
IC3	4047	—	—
IC19,25	4049	—	—
IC26	4051	—	—
IC24	4053	—	—
IC12	7406	14	7
IC2,17	14538	—	—
IC14	8255A5	26	7

Servo Board
Type 6079-001-11
Schematic Diagram

J4

OBD Ø
OBD 1
OBD 2
OBD 3
OBD 4
OBD 5
OBD 6
OBD 7
OBA Ø
OBA 1
OBA 2
OBA 3
OB VAC
OBUNPKR
OB PLL
OB SERVO
OB DEAD
OB RD
OB WRT
OB RESET

IC15 74LS245
IC16 74LS245
EN G
DIR
OBDØ OBD1 OBD2 OBD3 OBD4 OBD5 OBD6 OBD7
OBAØ OBA1 OB SERVO OBRD OBWRT OB DEAD OB VAC

+5V
R150 10K
R149 10K
R148 10K

VAC(3B2)
(3A6) 48V'S
IC10 74LSØØ
IC12 7406
+5V R145 1K
RESET

DAC Ø-7
CNTRL Ø,1,2,5
DIRECTION
(4B2)

IC14 8255A-5
DØ D1 D2 D3 D4 D5 D6 D7
PAØ PA1 PA2 PA3 PA4 PA5 PA6 PA7
DAC Ø DAC 1 DAC 2 DAC 3 DAC 4 DAC 5 DAC 6 DAC 7
AØ A1 CS RD WR
PBØ PB1 PB2 PB3 PB4 PB5 PB6 PB7
CNTRL Ø CNTRL 1 CNTRL 2 CNTRL 3 DIRECTION CNTRL 5 CNTRL 6 HOLD
PCØ PC1 PC2 PC3 PC4 PC5 PC6 PC7
RUNNING(4C6,5D7)
ADC (4B8)
BRAKE(3D3,6A6)

+5V R146 10K
IC11 74LS373
LE OE
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
SRVENB (3B2)
LOAD (3C2)
UNLOAD (3C2)
FAST (3B2)
GCRRAMP(5A1)

IC12 7406
HOLD (3B4)

TP RESET
IC12 7406
J4 20 OB FAULT

IC10 74LSØØ
IC10 74LSØØ

+5V R153 27K
C64 1.0 35V
IC17 14538
T2 T1 VDD VSS CD
+5V
+5V R152 47K
C62 10 16V

+5VPL
IC18 4001

R141 470 1/2W
C54 500 25V
CR40 IN4002
-12VR
+12VR
IC12 7406
R142 2.7K
Q39 2N6035

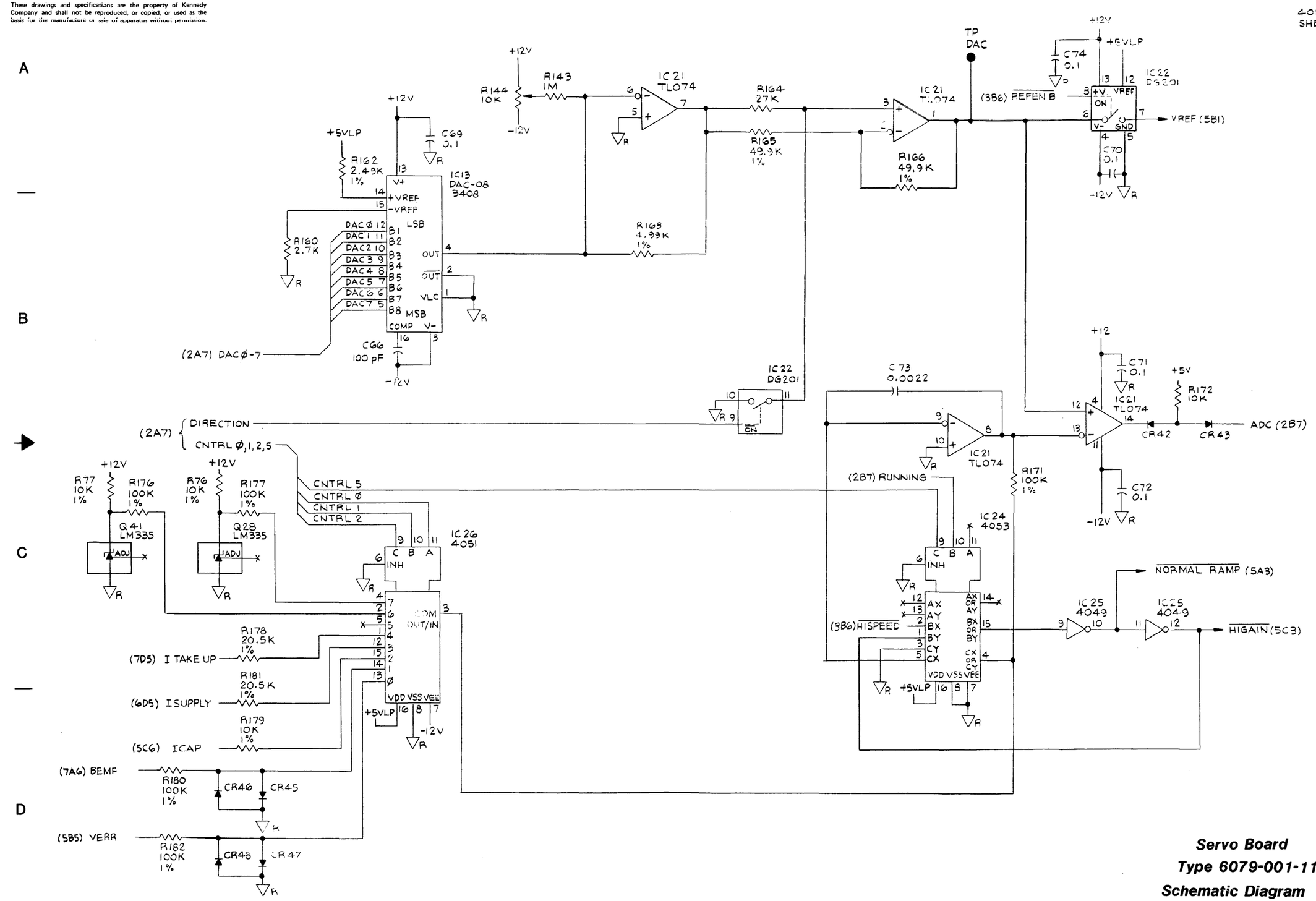
J23
FILE PROTECT ASSEMBLY (190-6640-001)

R147 10K

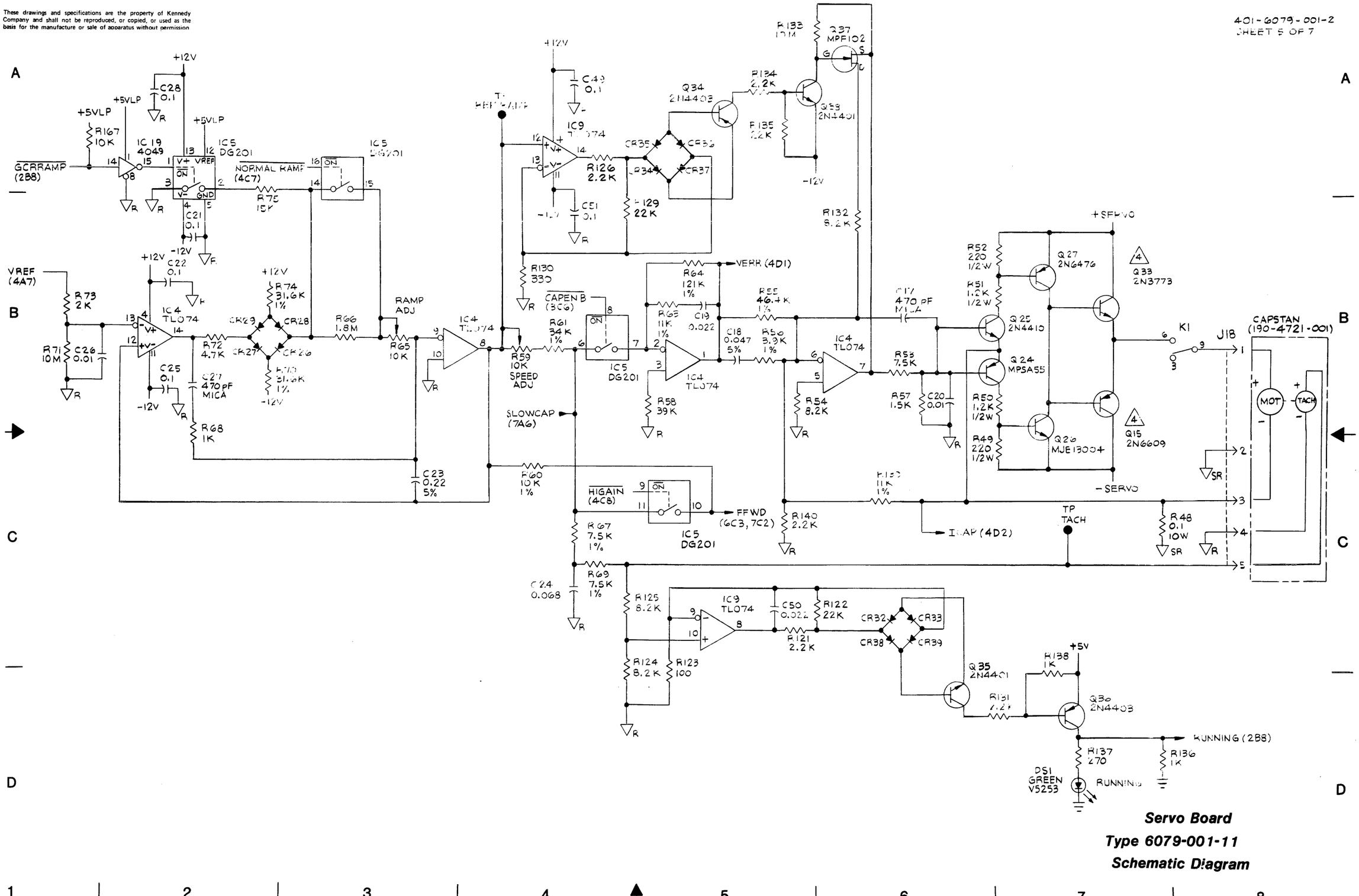
Servo Board
Type 6079-001-11
Schematic Diagram

+SERVO
R174 22K
+12V
CR44
Q40 2N4403
+5VLP
IC25 4049
TP 48VS
48VS (2C4, 6B4, 7B5)
R173 10K
R175 22K
R
+5V
R159 470
FAST
DS2 RED MV5054-1
IC23 4001B
HISPEED (4C6)
(2B8) FAST
IC19 4049
+5VLP
R155 10K
IC12 7406
+5V
R170 10K
IC10 74LS00
+5VLP
R154 10K
+5VLP
R158 10K
VAC (2B4)
(2B7) HOLD
REFENB (4A6)
+5VLP
IC23 4001
(2B8) SRVENB
IC25 4049
SNSENB (6C3, 7C3)
IC20 4011
IC23 4001
+5VLP
IC19 4049
LOAD (6D3, 7A3)
CAPENB (5B4)
IC20 4011
+5VLP
R156 10K
(2B8) UNLOAD
IC18 4001B
UNLOAD (6A2)
+5V
R151 121K 1%
C63 1.5%
+5VLP
R157 10K
TP3
(2B8) LOAD
IC17 14538
IC20 4011
IC18 4001B
TENSION (6B2)
+5V
CR41 +5VLP
R161 620K
IC20 4011
IC19 4049
VMODE TU (7C4)
IC18 4001B
IC19 4049
IC23 4001B
VMODE SU (6C4)
(2B7) BRAKE
IC19 4049
C67 0.15 5%

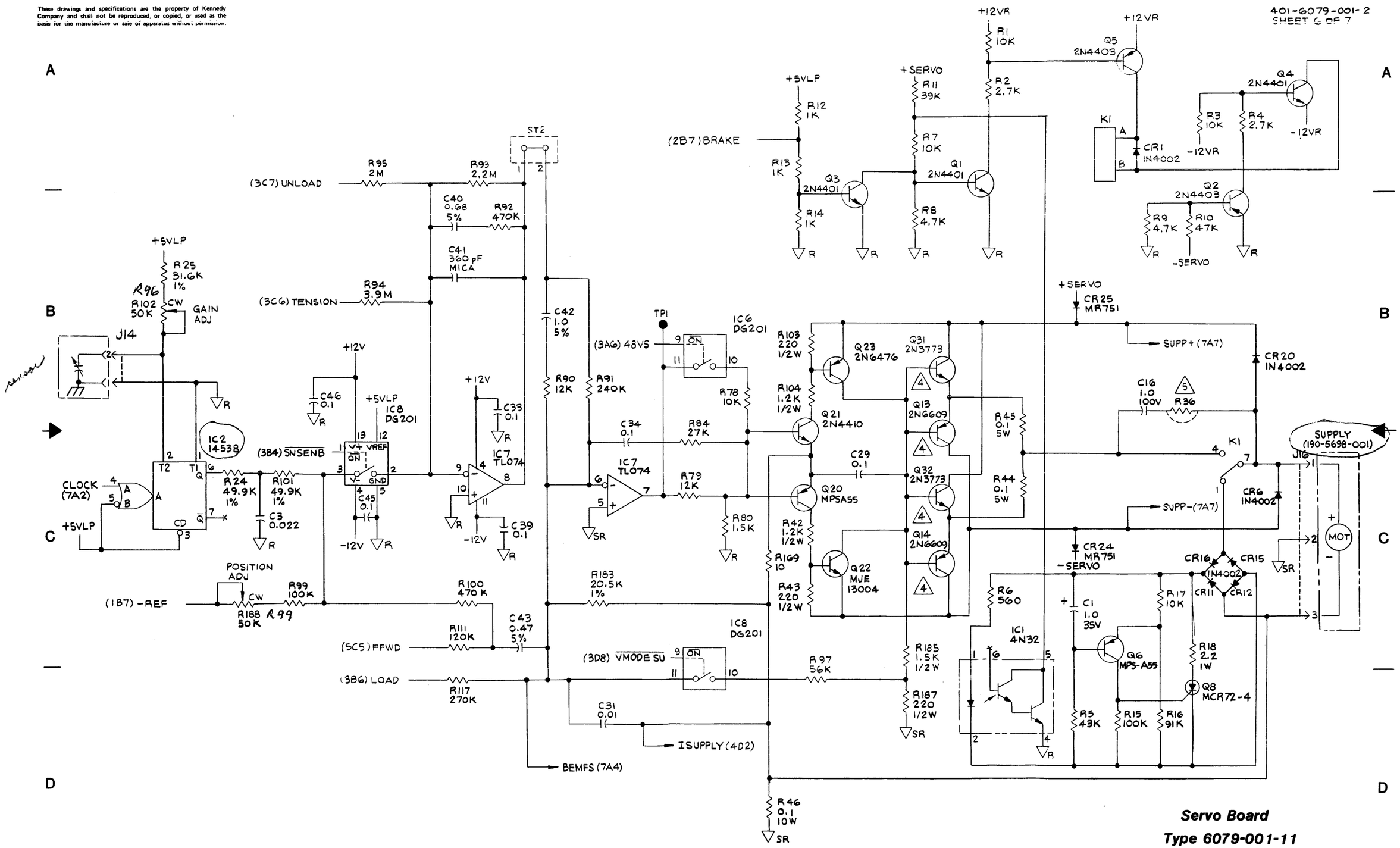
Servo Board
Type 6079-001-11
Schematic Diagram



Servo Board
Type 6079-001-11
Schematic Diagram



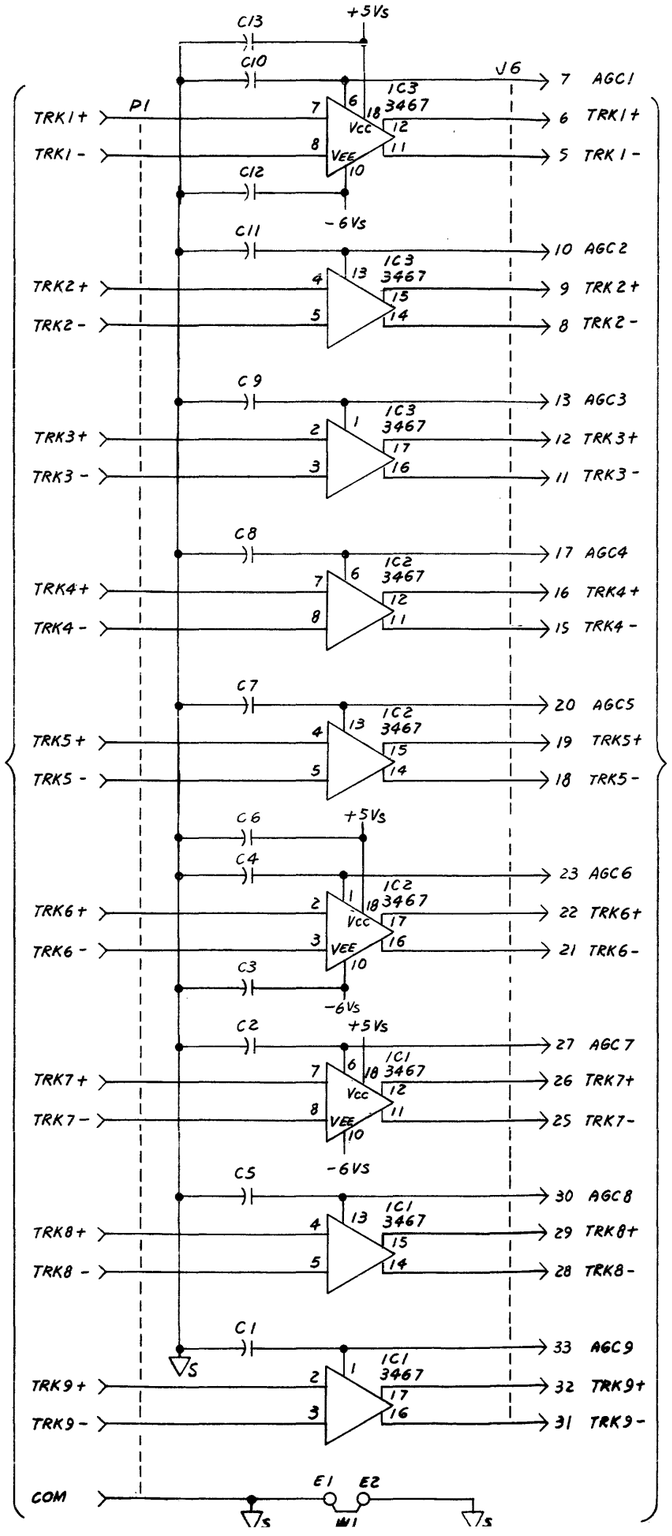
Servo Board
Type 6079-001-11
Schematic Diagram

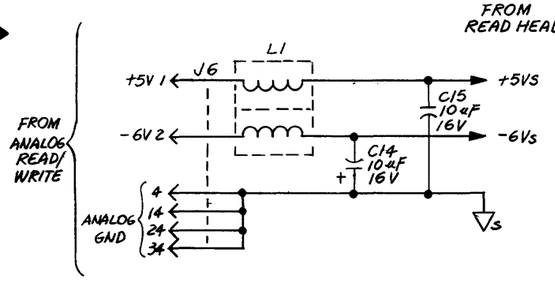


Servo Board
Type 6079-001-11
Schematic Diagram

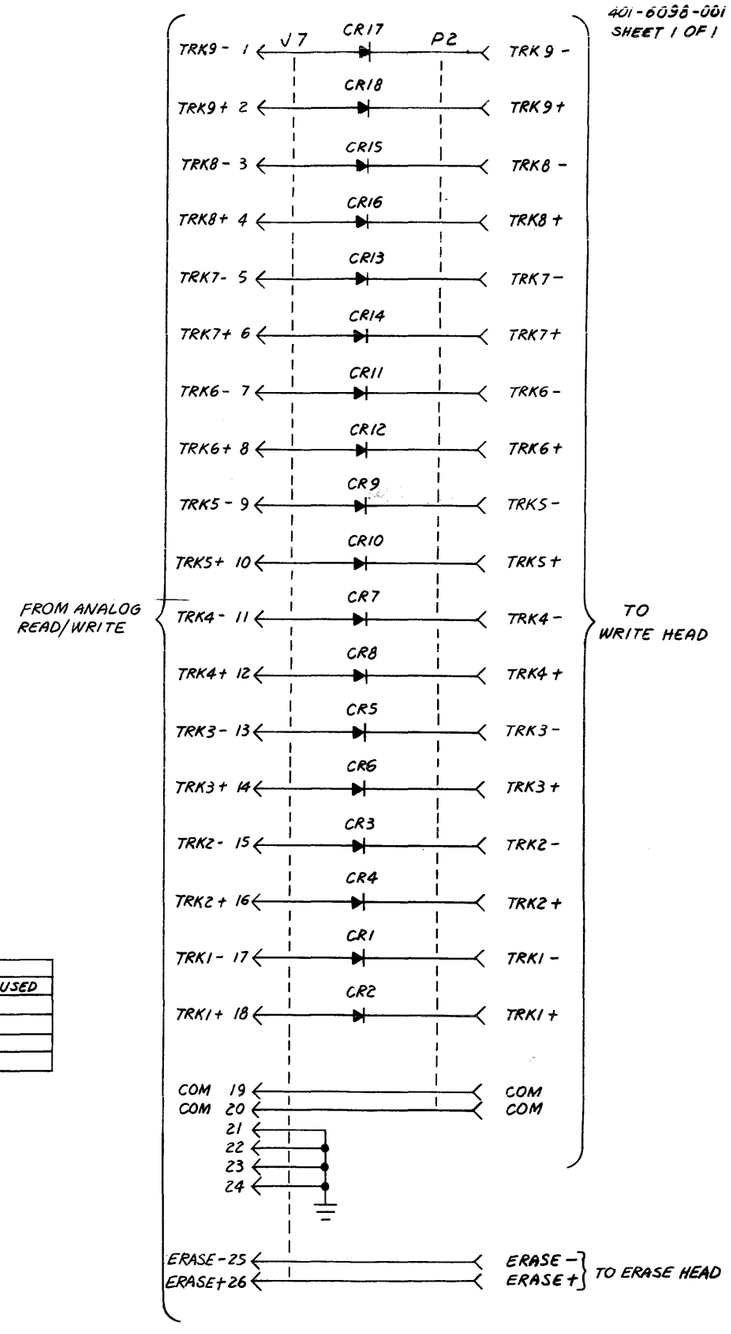
R28 23.7K 1%
C5 0.001
IC3 4047
TP CLK
+5VLP
CLOCK(6C1)
(3B6) LOAD
R118 270K
(6D4)BEMFS
R116 47K
R115 47K
IC9 TL074
R120 1M
CR30
RG2 4.7K
SLOWCAP (5B4)
R119 47K
C48 0.1
CR31
TP SPEED LIMITING BEMF (4D2)
C47 0.01
R127 1M
R128 47K
C53 0.1
C52 0.01
R
(3C8) TENSION
R96 4.7M
R89 2.2M
ST1
C38 0.68 5%
R88 470K
C37 360 PF MICA
R87 240K
C36 1.0 5%
R85 12K
(6C7) SUPP-
(6B7) SUPP+
CR18 IN4002
CR4 IN4002
CR21 IN6289
CR3 IN6289
SR
CR19 IN4002
CR2 IN4002
+SERVO
CR23 MR751
(1B7)-REF
R152 Takeup centering
R189 50K CW
R109 100K
R26 31.6K
CW R112 50K Takeup gain R147
J14
C78 0.1
+12V
TP2
IC6 DG201
(3A6) 48Vs
C77 0.1
R83 10K
-12V
R86 27K
C35 0.1
IC7 TL074
R82 12K
R81 1.5K
R168 10
R184 20.5K 1%
R40 220 1/4W
R38 1.2K 1/2W
Q19 2N6476
Q16 2N4410
Q17 MPS-A55
Q18 MJE 13004
R41 1.2K 1/2W
R39 220 1/2W
Q29 2N3773
Q11 2N6609
Q30 2N3773
Q12 2N6609
C30 0.1
R37 0.1 5W
R186 0.1 5W
C15 1.0 100V
R35
K1
CR5 IN4002
CR22 MR751
-SERVO
CR10 CR9 IN4002 CR13 CR14
C2 1.0 35V
R20 10K
R19 2.2 1W
Q7 MPS-A55
Q9 MCR 72-4
R21 43K
R22 100K
R23 91K
TAKE-UP (190-5698-003)
J17
MOT
IC2 14538
(3B4) SNSEN B
IC8 DG201
IC7 TL074
R27 49.9K 1%
R108 49.9K 1%
C4 0.022
R113 470K
R114 470K
(5C5) FFWD
IC7 TL074
R107 120K
C44 0.47 5%
(3D6) V MODE TU
IC8 DG201
R98 120K
R105 1.5K 1/2W
R106 220 1/2W
C32 0.01
ITAKE UP(4D2)
R47 0.1 10W
SR

Servo Board
Type 6079-001-11
Schematic Diagram



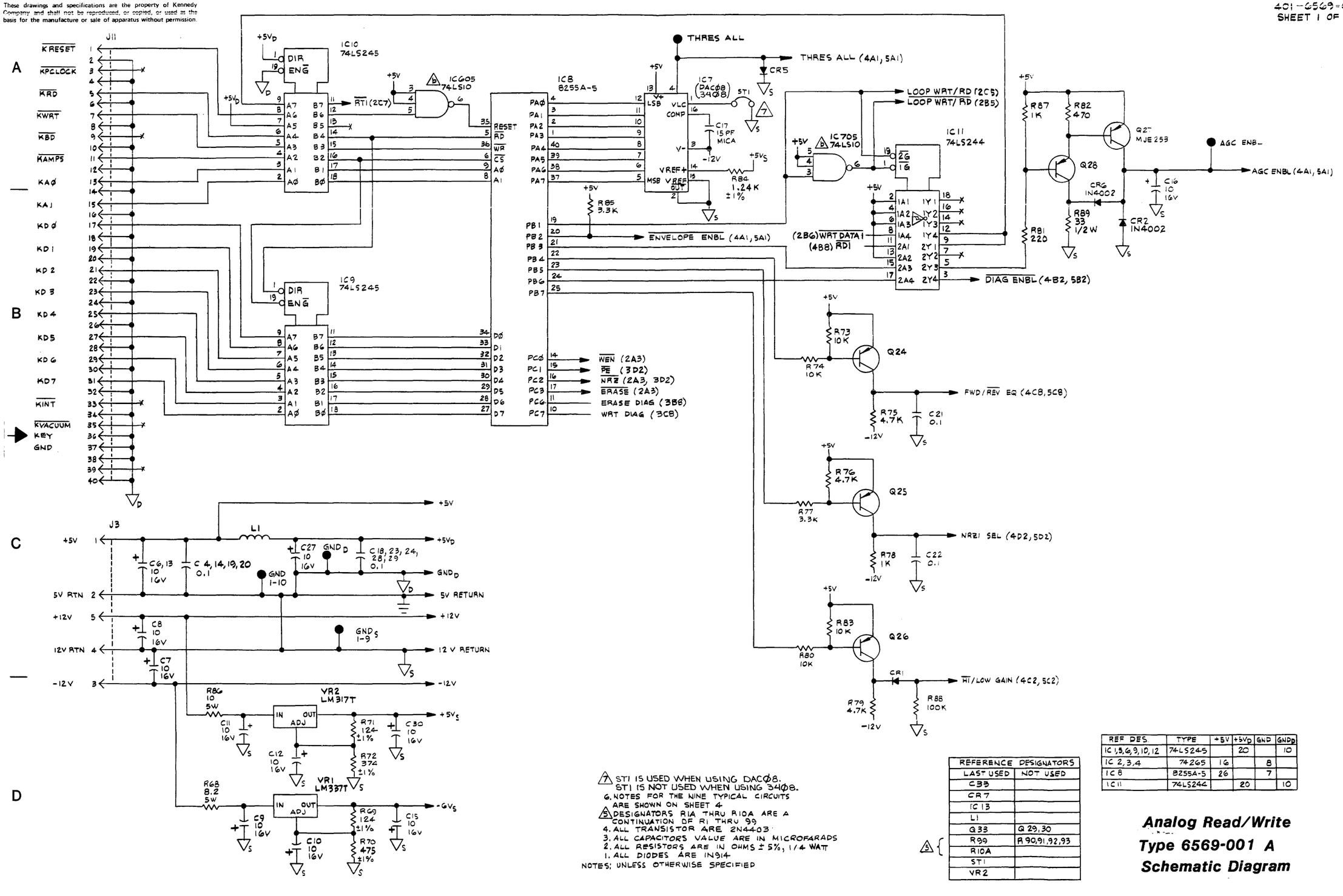


REF. DES	
LAST USED	NOT USED
C15	
L1	
CR18	
IC3	



3. PIN 9 OF IC1 - IC3 IS ANALOG GND.
2. ALL CAPACITOR VALUES ARE IN 0.1 MICROFARADS.
1. ALL DIODES ARE IN914.
NOTE: UNLESS OTHERWISE SPECIFIED.

Read Preamp
Type 6098-001 A
Schematic Diagram



7 ST1 IS USED WHEN USING DACØ8.
ST1 IS NOT USED WHEN USING 34ØB.

6. NOTES FOR THE NINE TYPICAL CIRCUITS ARE SHOWN ON SHEET 4.

5 DESIGNATORS R1A THRU R10A ARE A CONTINUATION OF R1 THRU 99

4. ALL TRANSISTOR ARE 2N4403.
3. ALL CAPACITORS VALUE ARE IN MICROFARADS
2. ALL RESISTORS ARE IN OHMS ± 5%, 1/4 WATT
1. ALL DIODES ARE IN914

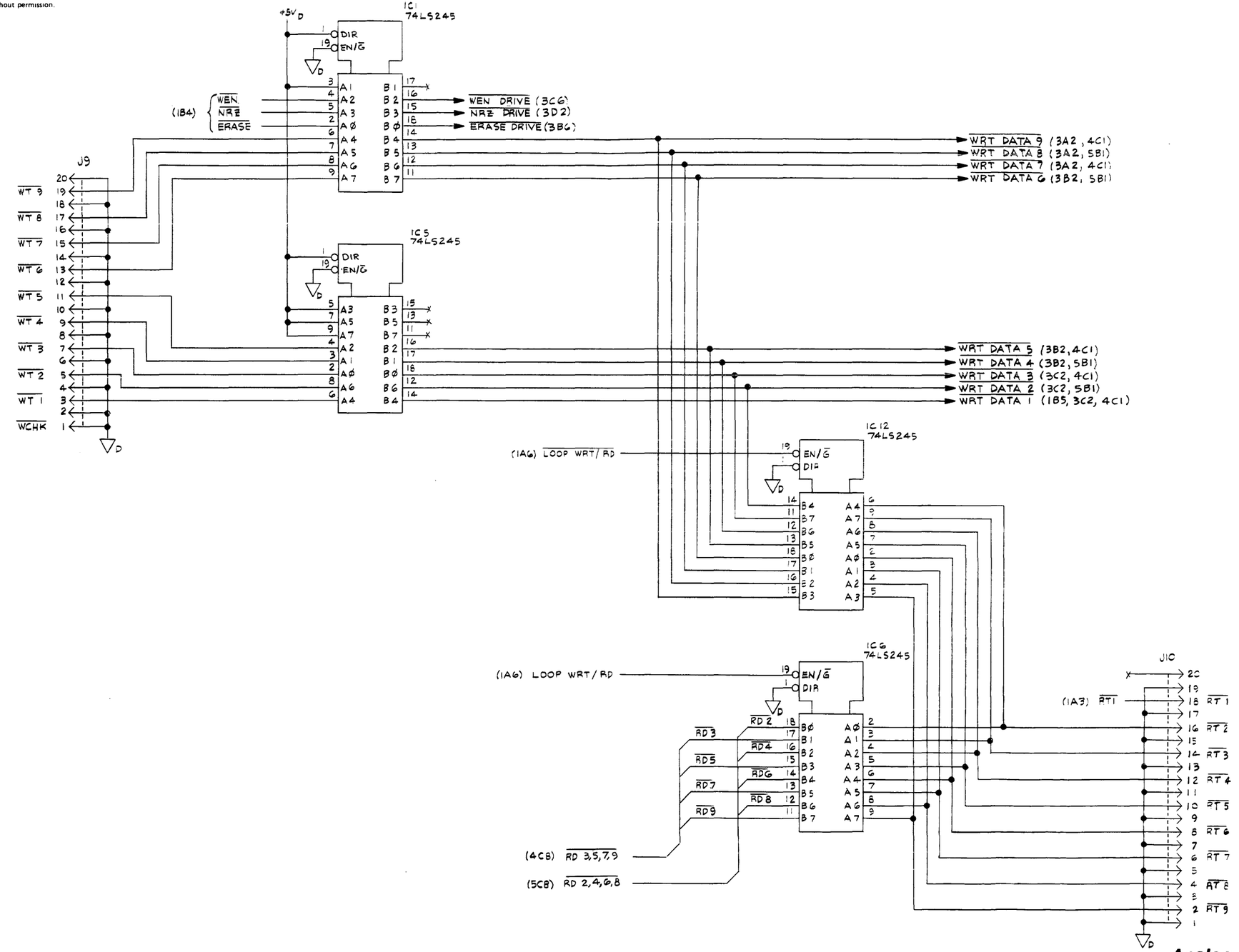
NOTES; UNLESS OTHERWISE SPECIFIED

REFERENCE DESIGNATORS	
LAST USED	NOT USED
C33	
CR7	
IC13	
L1	
Q33	Q29,30
R99	R90,91,92,93
R10A	
ST1	
VR2	

5

REF DES	TYPE	+5V	+5VD	GND	GNDD
IC 1,5,6,9,10,12	74LS245		20		10
IC 2,3,4	7426S	16		8	
IC 8	8255A-5	26		7	
IC 11	74LS244		20		10

Analog Read/Write
Type 6569-001 A
Schematic Diagram



Analog Read/Write
Type 6569-001 A
Schematic Diagram

(2A6) WRT DATA 9 — IC3 74265 — R1 100, R2 100 — Q2 — R3 82 1/2W, R4 220, R5 CW 500, R6 100 — +5V
(2A6) WRT DATA 8 — IC3 74265 — R7 100, R8 100 — Q4 — R9 82 1/2W, R10 220, R11 CW 500, R12 100
(2A6) WRT DATA 7 — IC3 74265 — R13 100, R14 100 — Q6 — R15 82 1/2W, R16 220, R17 CW 500, R18 100
(2A6) WRT DATA 6 — IC3 74265 — R19 100, R20 100 — Q8 — R21 82 1/2W, R22 220, R23 CW 500, R24 100
(2B6) WRT DATA 5 — IC4 74265 — R25 100, R26 100 — Q10 — R27 82 1/2W, R28 220, R29 CW 500, R30 100
(2B6) WRT DATA 4 — IC4 74265 — R31 100, R32 100 — Q12 — R33 82 1/2W, R34 220, R35 CW 500, R36 100
(2B6) WRT DATA 3 — IC2 74265 — R37 100, R38 100 — Q14 — R39 82 1/2W, R40 220, R41 CW 500, R42 100
(2B6) WRT DATA 2 — IC4 74265 — R43 100, R44 100 — Q16 — R45 82 1/2W, R46 220, R47 CW 500, R48 100
(2B6) WRT DATA 1 — IC4 74265 — R49 100, R50 100 — Q18 — R51 82 1/2W, R52 220, R53 CW 500, R54 100

(2B4) NRZ DRIVE — IC2 74265 — R55 220, R56 220, R57 1K — MJE253 Q19 — C1 0.1
Q20 — R58 1K, R59 220 — C2 0.1
Q31 — R98 10K, R97 4.7K, R99 5.6K, R1A 1.40K ±1%
Q32 — R2A 1.5K, R3A 10K, R4A 4.7K
(1B4) PE
(1B4) NRZ

+5V — R65 1K — (2B6) ERASE DRIVE — R66 10K — Q23 — R67 100 1/2W — ERASE DIAG (1B4)
C5 0.1, CR4 IN4002
+5V — R61 4.7K — (2B6) WEN DRIVE — R60 10K — Q21
+5V — R10A 10K — WRT DIAG (1B4)
C32 0.1

IC13 LM319 — +12V, -12V — R7A 1K — Q33 2N4401 — R8A 10K
CR7 — R9A 4.7K — CR3 — R62 2.2K — C3 0.1 — R63 10K — Q22 2N6038
R94 330, C33 .001 — R95 1K ±1% — R96 1K ±1% — R64 10 10W — C25 3.3 35V — C26 0.1 — +5V
IC13 LM319 — C31 100 PF MICA — R5A 93.1 ±1% — R6A 1K ±1% — -12V

1 TRK9 -
2 TRK9 +
3 TRK8 -
4 TRK8 +
5 TRK7 -
6 TRK7 +
7 TRK6 -
8 TRK6 +
9 TRK5 -
10 TRK5 +
11 TRK4 -
12 TRK4 +
13 TRK3 -
14 TRK3 +
15 TRK2 -
16 TRK2 +
17 TRK1 -
18 TRK1 +
19 TRK COM
20 TRK COM
21, 22, 23, 24 GND
25 TRK ERASE —
26 TRK ERASE +

Analog Read/Write
Type 6569-001 A
Schematic Diagram

(1A7) THRES ALL
(1A8) AGC ENBL
(1B5) ENVELOPE ENBL
AGC X
JG
TRK1
AGC 1
TRK 1+
TRK 1-
AGC 3
TRK 3+
TRK 3-
TRK 3
AGC 5
TRK 5+
TRK 5-
TRK 5
AGC 7
TRK 7+
TRK 7-
TRK 7
AGC 9
TRK 9+
TRK 9-
TRK 9
(1B6) DIAG ENBL
(2B6) WRT DATA 1
WRT DATA 9
(1D6) HI/LOW GAIN
(1C6) NRZI SEL
GND
12V RTN
-6V$_S$
+5V$_S$
+12V
-12V
+5V
-6V
THRES X
TPX
A DATA X
DDATAX
WX+
WX-
RD1 (1B5)
RD3
RD5
RD7
RD9 (2D5)
FWD/REV EQ(1B6)
(IC705 USED ON SHEET 1)
ODD TRACKS

RX01 10K
RX02 100K
RX03 39K
RX04 75K
RX05 220
RX06 15
RX07 330
RX08 3.3K
RX09 220
RX10 5.1K
RX11 10K
RX12 10K
RX13 10K
RX14 5.1K
RX15 1.2K
RX16 750
RX17 4.7K
RX18 750
RX19 4.7K
RX20 470
RX21 470
RX22 200
RX23 470K
RX24 4.7K
RX25 220
RX26 4.7K
RX27 220
RX28 2.2K
RX29 2.2K
RX30 120
RX31 100K
RX32 2.21K 1%
RX33 100
RX34 1K
RX35 1.5K
RX36 100
RX37 1K
RX38 100K
RX39 220
RX40 220
RX41
RX42 100K
RX43 470
RX44 2.2K

CX01 0.22 ±5%
CX02 0.01
CX03 100 pF
CX04 100pF MICA
CX05 0.1
CX06 0.1
CX07 0.1
CX08 0.1
CX09 0.1
CX10 0.0033
CX11
CX12 0.1
CX13 0.1
CX14 1000 pF MICA
CX15 470pF MICA
CX16 200pF MICA
CX17 390pF MICA
CX18 0.0047
CX19 0.0015
CX20 0.1
CX21 0.1
CX22 0.1
CX23 0.1
CX24 0.0068
CX25 10 16V
CX26 0.22 ±5%
CX27 0.0001
CX28 220pF MICA
CX29 270pF MICA

LX01
LX02 150μH
LX03
LX04 470μH
LX05 100μH

QX01 2N4401
QX02 2N4258
QX03 J112
QX04 J112
QX05 J112
QX06 J112
QX07 2N4401
QX08 2N4401
QX09 J112
QX10 J112

CRX01
CRX02
CRX03
CRX04
CRX05
CRX06
CRX07

ICX01 MC4011
ICX02 LM339
ICX03 NE592
ICX04 LM361
ICX05 74LS10
ICX05 74LS04

REF DES	TYPE	+5V	+5V$_S$	GND	GND$_S$
ICX01	MC4011		14		7
ICX05	74LS10	14		7	

REFERENCE DES.	
LAST USED	NOT USED
CRX07	CRX02
LX05	LX01
TPX	
RX44	RX41
QX10	
ICX05	
CX29	CX11

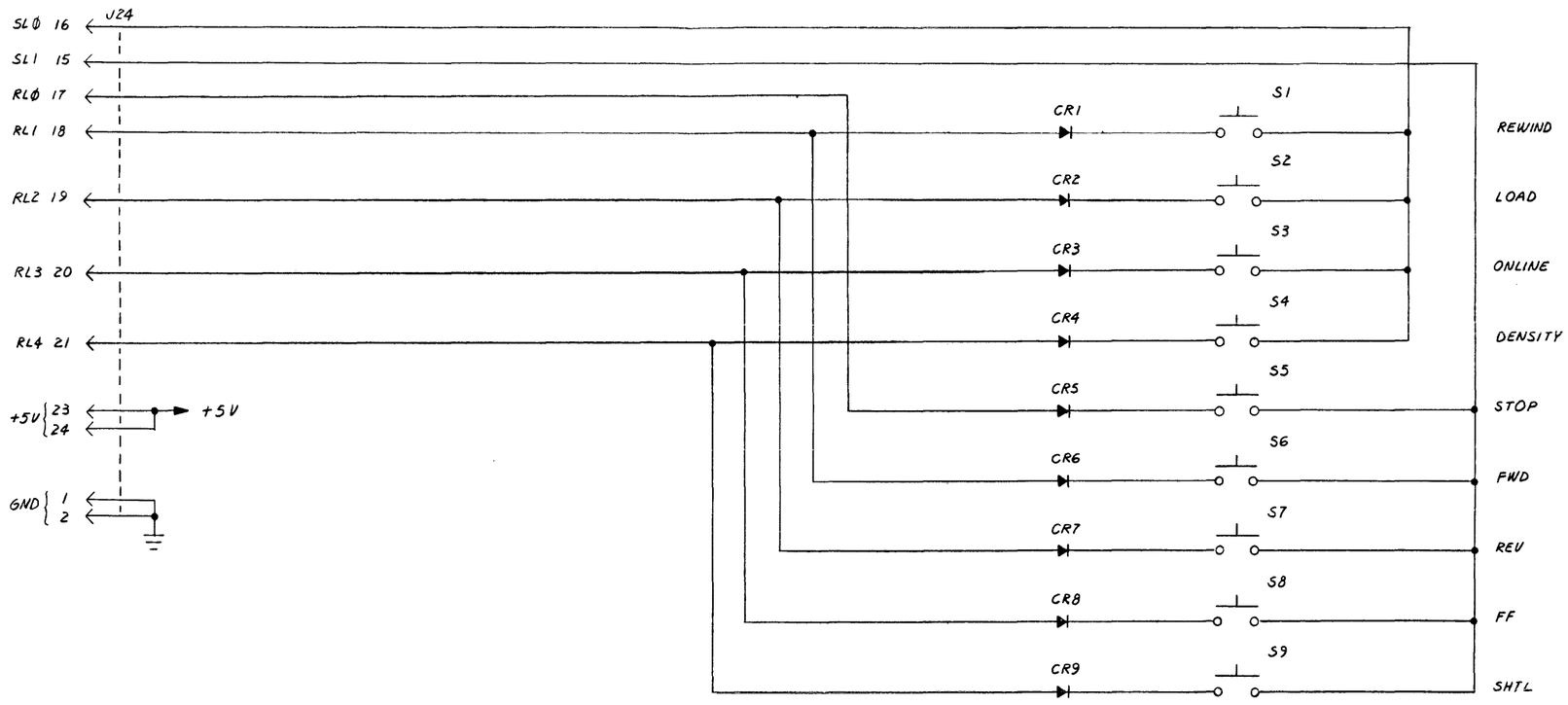
A REFERENCE DESIGNATOR NOTED IS THE ONLY SECTION OF ICX05 USED ELSEWHERE
B PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. THE 'X' INDICATES THE TRACK NUMBER
EXAMPLE: IC 201 = ICX01 OF TRACK 2
R 902 = RX09 OF TRACK 9
AGC3 = AGCX OF TRACK 3

NOTES: UNLESS OTHERWISE SPECIFIED

Analog Read/Write
Type 6569-001 A
Schematic Diagram

(1A7) THRES ALL
(1A8) AGC ENBL
(1B5) ENVELOPE ENBL
AGC X
J6
TRK 2
AGC 2 10
TRK 2+ 9
TRK 2- 8
AGC 4 17
TRK 4+ 16
TRK 4- 15
TRK 4
AGC 6 23
TRK 6+ 22
TRK 6- 21
TRK 6
AGC 8 30
TRK 8+ 29
TRK 8- 28
TRK 8
(1B6) DIAG ENBL
(2B6) WRT DATA 2
WRT DATA 4
(2A6) WRT DATA 6
WRT DATA 8
(1D6) HI/LOW GAIN
(1C6) NRZI SEL
GND
12V RTN
+5VS
-6VS
-12V
RX01 10K
RX02 100K
RX03 39K
RX04 75K
RX05 220
RX06 15
RX07 330
RX08 3.3K
RX09 220
RX10 5.1K
RX11 10K
RX12 10K
RX13 10K
RX14 5.1K
RX15 1.2K
RX16 750
RX17 4.7K
RX18 750
RX19 4.7K
RX20 470
RX21 470
RX22 200
RX23 470K
RX24 4.7K
RX25 220
RX26 4.7K
RX27 220
RX28 2.2K
RX29 2.2K
RX30 120
RX31 100K
RX32 2.21K 1%
RX33 100
RX34 1K
RX35 1.5K
RX36 100
RX37 1K
RX38 100K
RX39 220
RX40 220
RX42 100K
RX43 470
RX44 2.2K
CX01 0.22 ±5%
CX02 0.01
CX03 100PF
CX04 100PF MICA
CX05 0.1
CX06 0.1
CX07 0.1
CX08 0.1
CX09 0.1
CX10 0.0033
CX11
CX12 0.1
CX13 0.1
CX14 1000PF MICA
CX15 470PF MICA
CX16 200PF MICA
CX17 390PF MICA
CX18 0.0047
CX19 0.0015
CX20 0.1
CX21 0.1
CX22 0.1
CX23 0.1
CX24 0.0068
CX25 10 16V
CX26 0.22 ±5%
CX27 0.001
CX28 220PF MICA
CX29 270PF MICA
CW RX22 200
ICX01 MC4011
ICX02 LM339
ICX03 NE592
ICX04 LM361
ICX05 74LS10
ICG05 USED ON SHEET 1
QX01 2N4401
QX02 2N4258
QX03 J112
QX04 J112
QX05 J112
QX06 J112
QX07 2N4401
QX08 2N4401
QX09 J112
QX10 J112
LX02 150μH
LX03
LX04 470μH
LX05 1004H
CRX01
CRX03
CRX04
CRX05
CRX06
CRX07
THRES X
TPX
A DATA X
WX-
WX+
DDATAX
RD2
RD4
RD6
RD8
(2D5)
FWD/REVEQ(1B6)
EVEN TRACKS

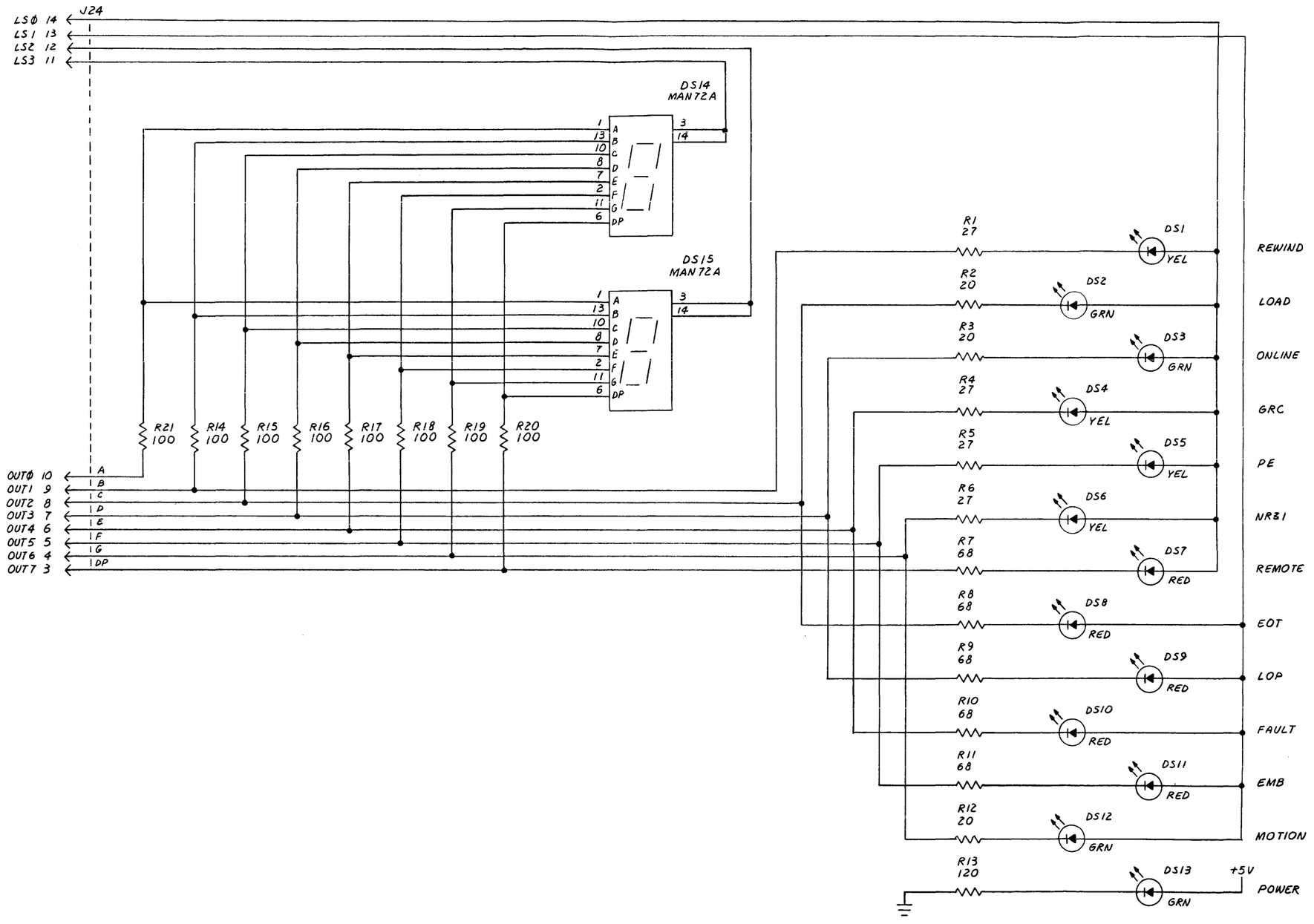
Analog Read/Write
Type 6569-001 A
Schematic Diagram



LAST USED	NOT USED
CR 9	
DS 15	
R 20	
S 9	

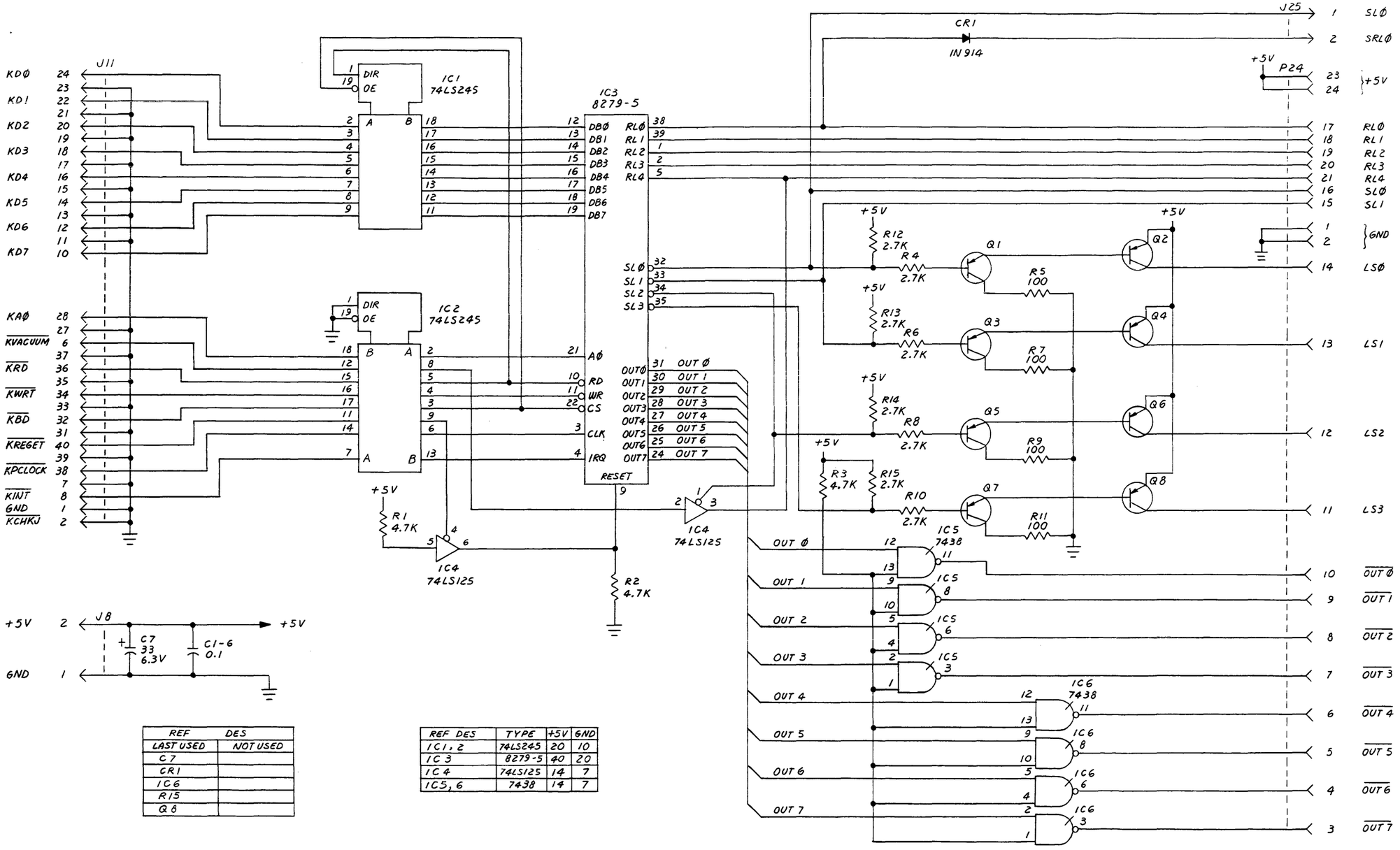
NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.
2. DIODES ARE IN 914.
3. LEDS ARE T1 3/4.

Keyboard
Type 6570-001 B
Schematic Diagram



Keyboard
Type 6570-001 B
Schematic Diagram

401-6571-001 A
SHEET 1 OF 1

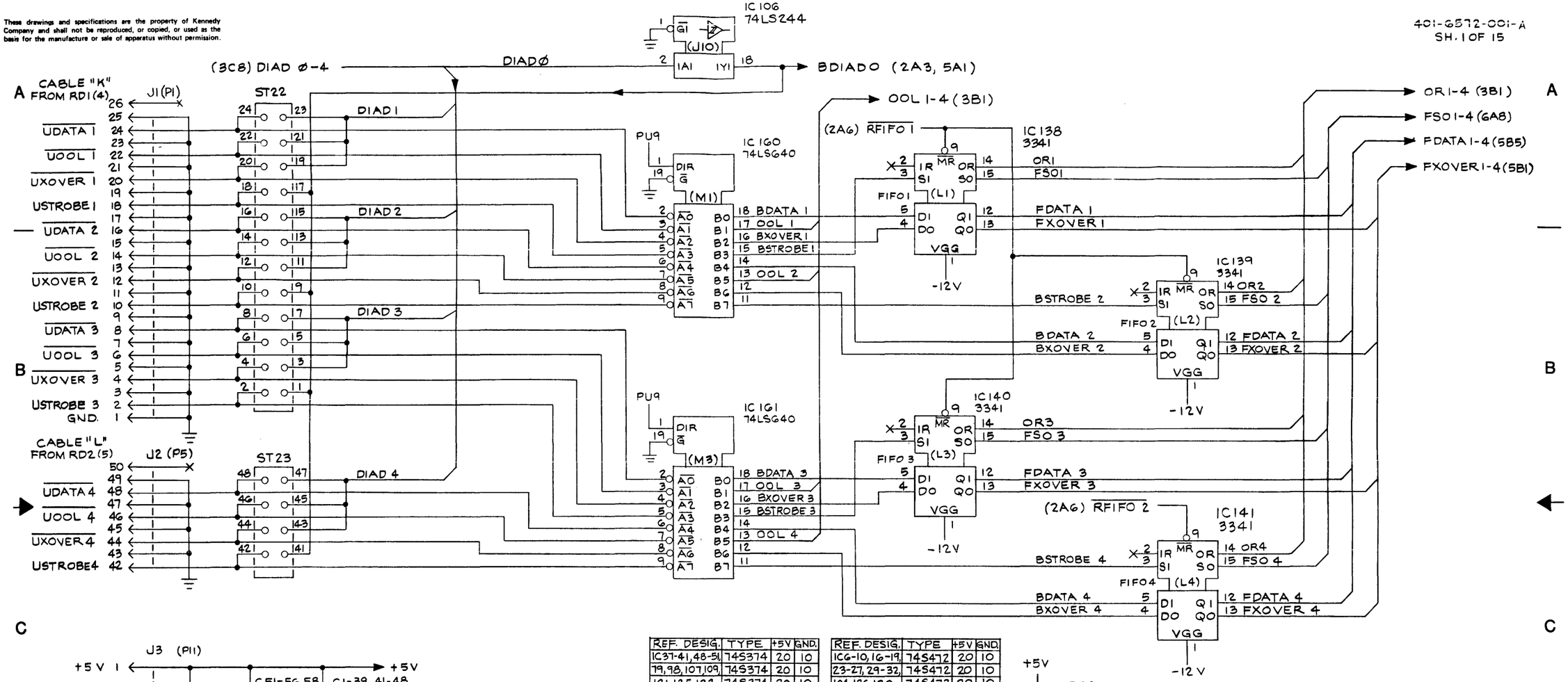


REF DES	
LAST USED	NOT USED
C7	
CR1	
IC6	
R15	
Q8	

REF DES	TYPE	+5V	GND
IC1, 2	74LS245	20	10
IC3	8279-5	40	20
IC4	74LS125	14	7
IC5, 6	7438	14	7

3. ALL RESISTOR VALUES ARE IN OHMS ± 5% 1/4 WATT.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL TRANSISTORS ARE 2N4403.
NOTES: UNLESS OTHERWISE SPECIFIED.

Keyboard Decoder
Type 6571-001 A
Schematic Diagram



REF. DESIGNATORS	
LAST USED	NOT USED
C 81	——
IC 170	IC1-5,11,21, 22,28,36, 45-47,65, 71-73,110, 114,142,166
R 37	——
ST 23	ST 1,14
TP10	——
Y1	——

REF. DESIG.	TYPE	+5V	GND.
IC31-41,48-51	74S374	20	10
79,98,107,109,	74S374	20	10
121,125,132	74S374	20	10
IC118-120,	74LS32	14	7
116, 124, 153	74LS32	14	7
IC 60,69,91	74S04	14	7
IC13,20,105	74S08	14	7
IC 56,64	74S32	14	7
IC 78	74S38	14	7
IC 149	74S85	16	8
IC12,58,93,	74S74	14	7
101,102,165	74S74	14	7
IC44,61,103	74S140	14	7
IC55,86,87	74S138	16	8
IC115	74S244	20	10
IC128,150	7445	16	8
IC66-68	2901B	10	30
IC90, 112	74LS125	14	7
IC 99	74S151	16	8
IC97, 35	74LS259	16	8
IC15, 34	74S288	16	8
IC100,122	74LS273	20	10
IC42,43	74S251	16	8
IC83-85	2903	36	13
IC160-164	74LSG40	20	10
IC14, 33	2910	10	30
IC59, 92	2925	13/24	1/12
IC131, 152	74LS374	20	10
IC 129	74LS240	20	10

REF. DESIG.	TYPE	+5V	GND.
IC6-10,16-19,	74S472	20	10
23-27,29-32,	74S472	20	10
104,126,130,	74S472	20	10
137,148	74S472	20	10
IC 117	74S133	16	8
IC 111	2902A	16	8
IC 94	74S162	16	8
IC 57	29520	24	12
IC53,54	74S139	16	8
IC 63	74S280	14	7
IC 62	74S299	20	10
IC 134	74S86	14	7
IC74-77,88	16R6	20	10
IC 70,113,156	74LS74	14	7
158	74LS74	14	7
IC167-170	74LS245	20	10
IC 154	74LS139	16	8
IC 136	74LS161	16	8
IC 159	74LS377	20	10
IC 135	74LS378	16	8
IC 155	74LS109	16	8
IC80-82,95,96	29705	28	14
IC 138-141	3341	16	8
IC 143-147	3341	16	8
IC 89,106,108,	74LS244	20	10
123,127,133	74LS244	20	10
151	74LS244	20	10
IC 52	74S00	14	7
IC 157	74LS174	16	8

6 X INDICATES NO CONNECTION.

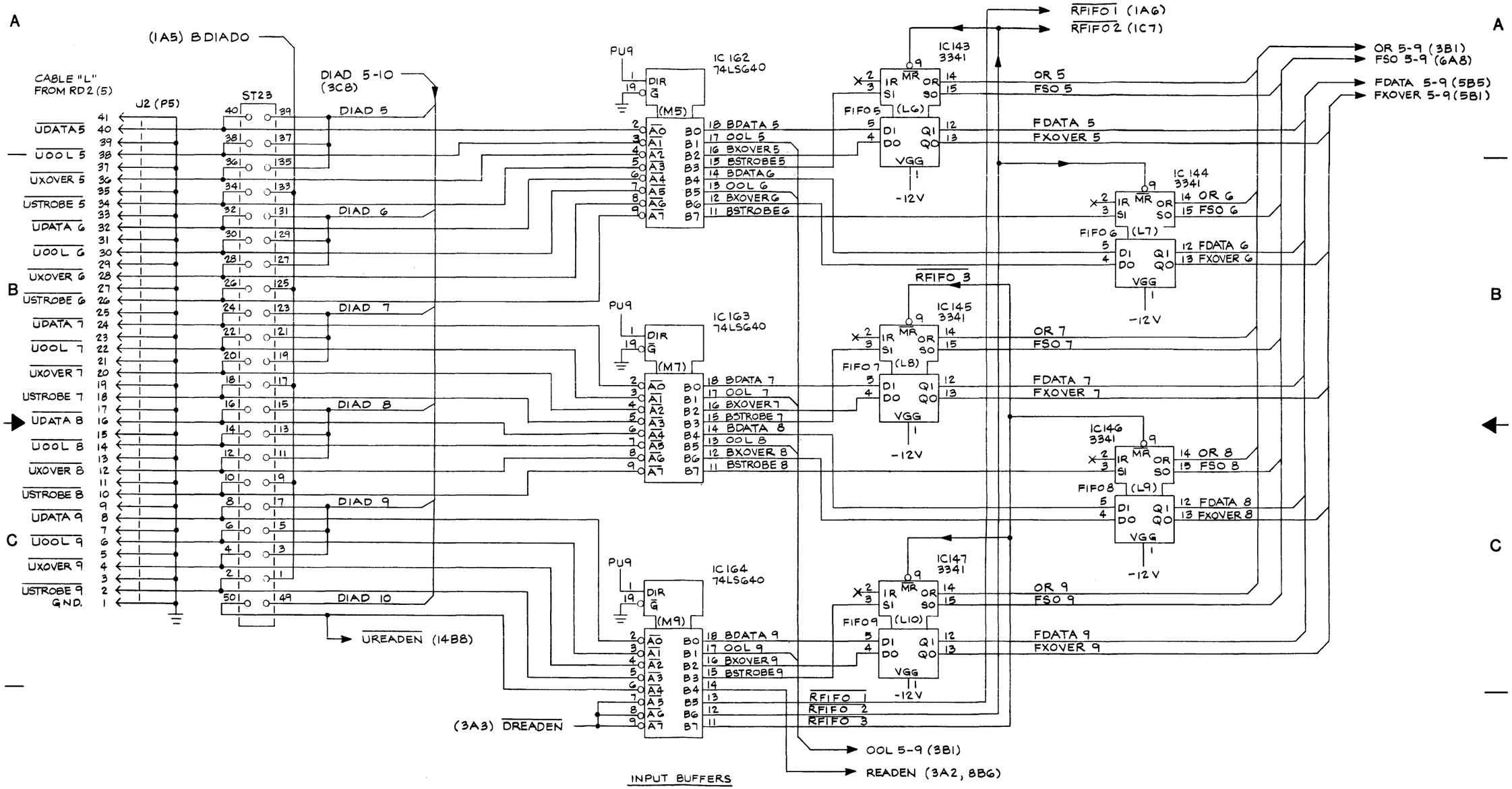
5 COMPONENTS SHOWN FOR FULL CAPABILITY OF THE BOARD.

4 ALL PULL UPS ARE 1K ± 5%, 1/4W.

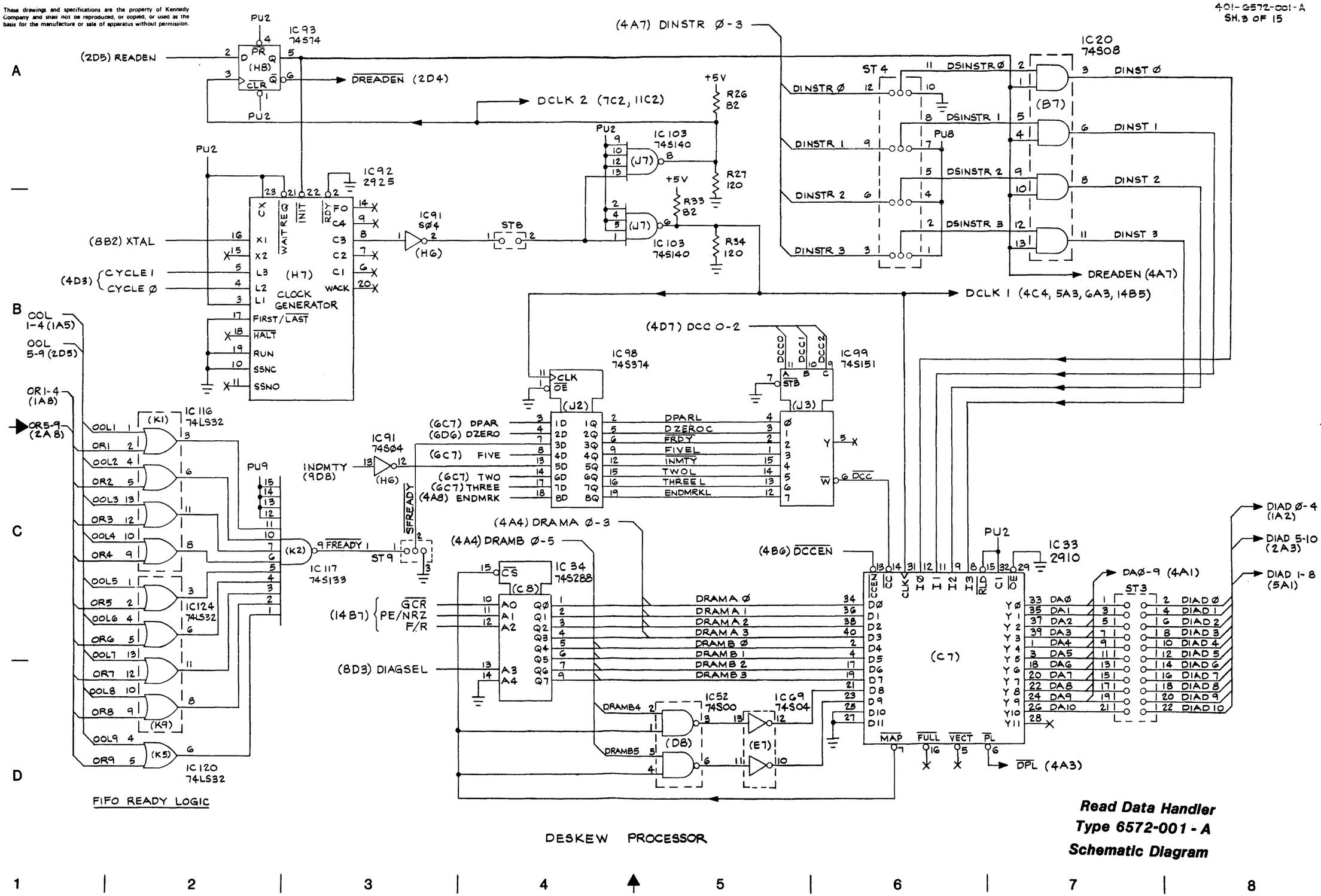
3. DESIGNATORS IN PARENTHESIS ARE BOARD LOCATIONS.
2. RESISTOR VALUES IN OHMS, ± 5%, 1/4 W
1. CAPACITOR VALUES IN MICROFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED.

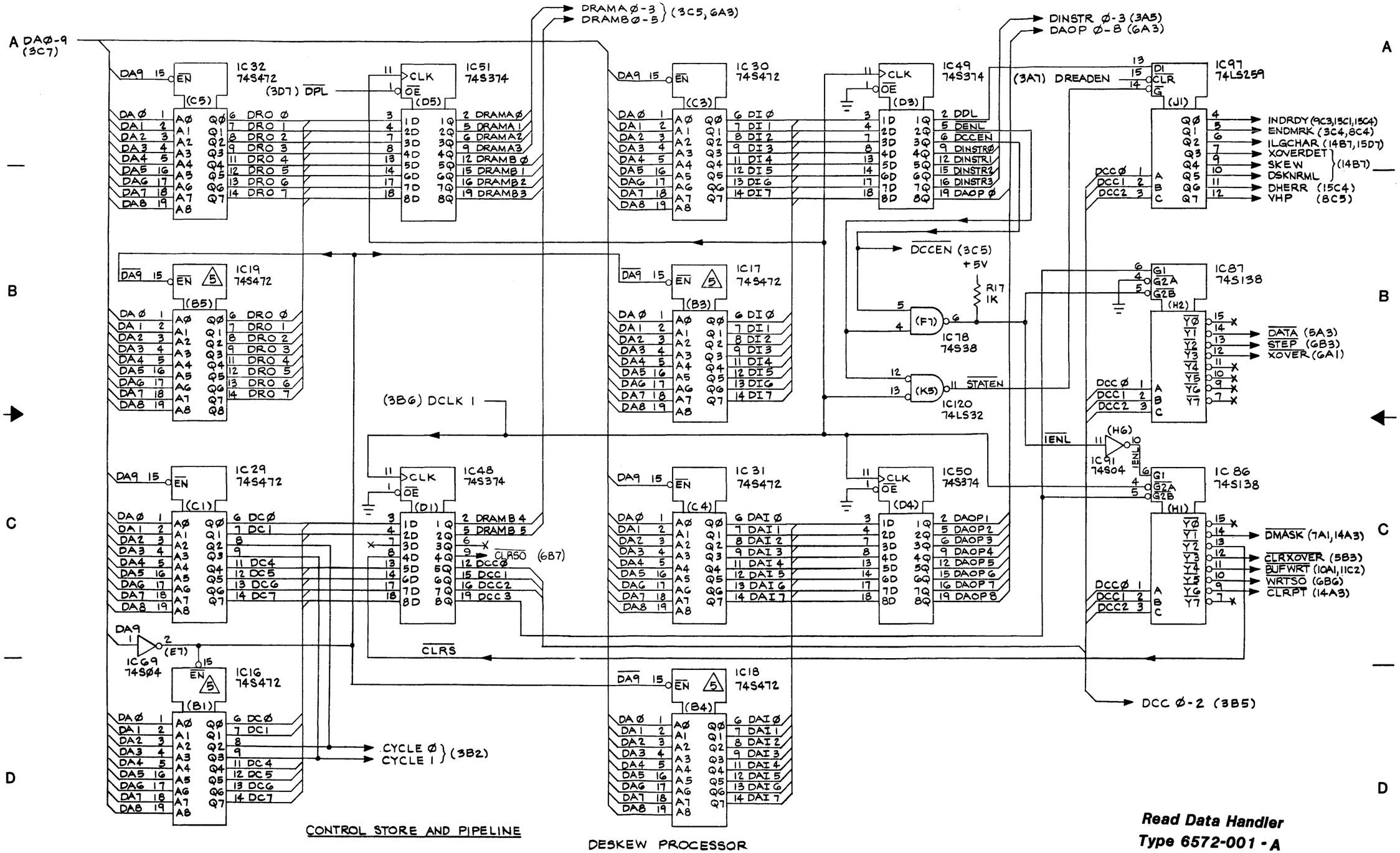
Read Data Handler
Type 6572-001 - A
Schematic Diagram



Read Data Handler
Type 6572-001 - A
Schematic Diagram



Read Data Handler
Type 6572-001 - A
Schematic Diagram



Read Data Handler
Type 6572-001 - A
Schematic Diagram

BDIAD Ø (1A5)

DIAD 1-8 (3C8)

FXOVER 1-4 (1A8)

FXOVER 5-9 (5B5)

(4B8) $\overline{DATA}$

(3B6) DCLK 1

IC120 74LS32 (K5)

$\overline{DATAC}$ (6B7)

XD Ø-8 (6A1)

DD Ø-8 (6A2)

FDATA 1-4 (1A8)

FDATA 5-9 (2A8)

SFDATA1

IC90 74LS125 (H5)

DD8

IC118 74LS32 (K3)

XD8

PU9

IC101 74S74 (J5)

PR D Q CLR

(4C8) $\overline{CLRXOVER}$

IC100 74LS273 (J4)

$\overline{CLR}$ CLK

FIFO DATA BUFFER

IC123 74LS244 (K8)

$\overline{OE}$ $\overline{OE}$

FXOVER1 ST10

FXOVER9 ST19

FXOVER2 ST11

FXOVER8 ST18

FXOVER3 ST12

FXOVER7 ST17

FXOVER4 ST13

FXOVER6 ST16

FXOVER5 ST15

DIAD1

DIAD2

DIAD3

DIAD4

DIAD5

DIAD6

DIAD7

DIAD8

XD7 XD6 XD5 XD4 XD3 XD2 XD1 XDØ

IC119 74LS32 (K4)

IC118 74LS32 (K3)

IC120 74LS32 (K5)

1D 2D 3D 4D 5D 6D 7D 8D

1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q

CROSSOVER LATCH

FDATA1 ST10

FDATA9 ST19

FDATA2 ST11

FDATA8 ST18

FDATA3 ST12

FDATA7 ST17

FDATA4 ST13

FDATA6 ST16

FDATA5 ST15

SFDATA9

SFDATA2

SFDATA8

SFDATA3

SFDATA7

SFDATA4

SFDATA6

SFDATA5

1A1 2A4 1A2 2A3 1A3 2A2 1A4 2A1

1Y1 2Y4 1Y2 2Y3 1Y3 2Y2 1Y4 2Y1

DD7 DD6 DD5 DD4 DD3 DD2 DD1 DDØ

SIGNATURE ANALYSIS JUMPERS

DESKEW PROCESSOR

Read Data Handler
Type 6572-001-A
Schematic Diagram

(5A8) DD Ø-8

(4A4) DRAMA Ø-3
DRAMB Ø-3

(4A7) DAOP Ø-8

(3B6) DCLK 1

XOVER (4B8)

XD 0-8 (5A5)

IC90 74LS125

IC89 74LS244

(4B8) STEP

EY Ø-8 (11A7)

EY Ø-7 (10A8)

WSTEP (12C5)

IC101 74S74

IC79 74S374

SINGLE TRACK ERROR POINTER

IC66 2901

LSNIBBLE (E1)

IC67 2901

(E3)

IC68 2901

MSMIBBLE (E5)

DESKEW PROCESSOR

+5V

R14 1K

R7 470

R16 1K

R37 1K

IC91 74S04

R8 1K

R15 1K

R9 330

DY Ø-8 (7A1, 10D1, 14A3, 11B2)

FIFO SHIFT-OUT CONTROL

IC102 74S74

(4C8) WRTSO

(4C4) CLRSO

(5A5) DATAC

IC121 74S374

IC122 74LS273

FSO 1-4 (1A8)

FSO 5-9 (2A8)

IC104 74S472

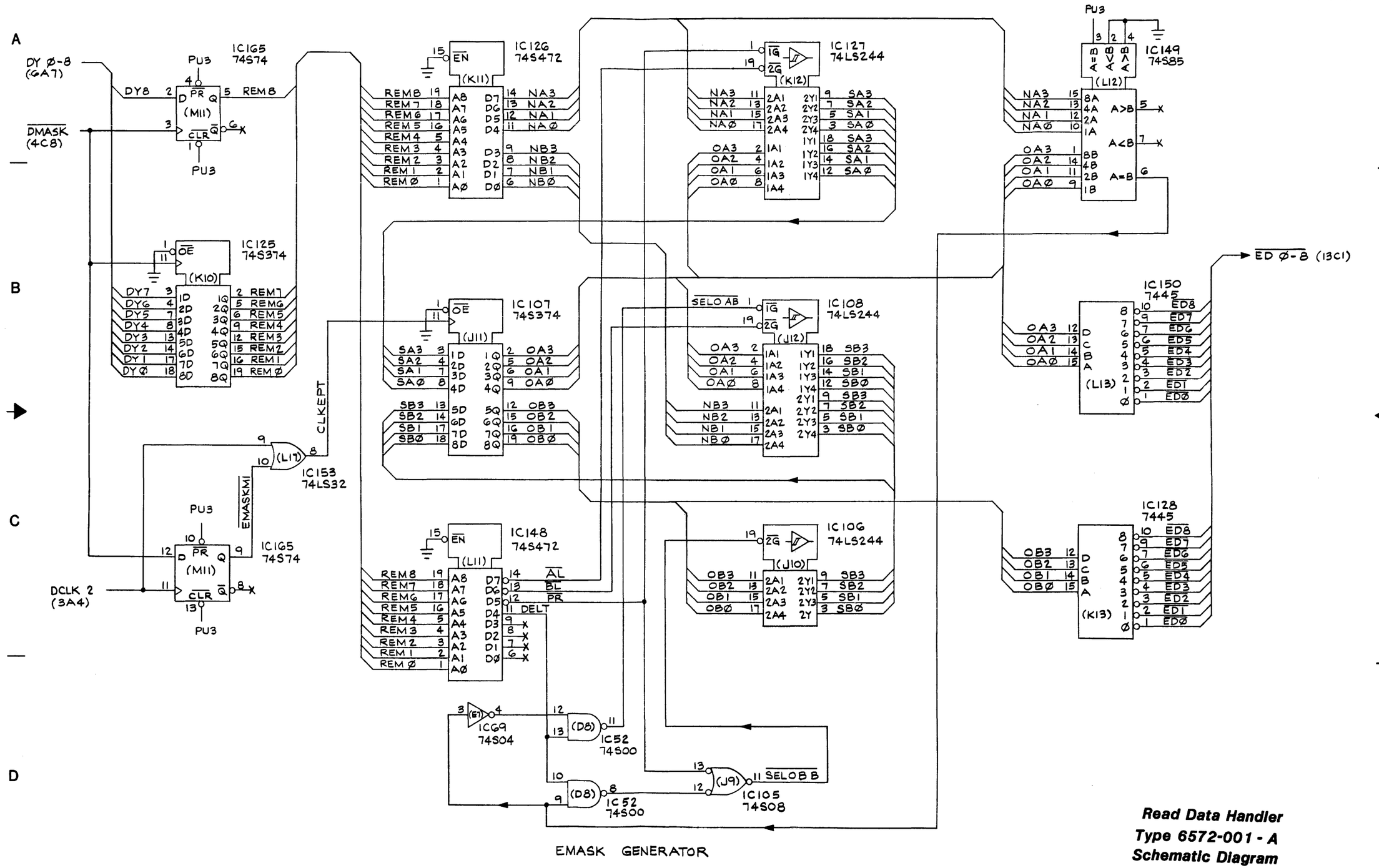
FIVE
TWO
THREE
DPAR
(3C4)

MAJORITY PROM

IC78 74S38

DZERO (3B4)

Read Data Handler
Type 6572-001-A
Schematic Diagram



Read Data Handler
Type 6572-001 - A
Schematic Diagram

(9C4) SEI Ø-3

TP2
(ST2-13)

START SYNCHRONIZER

EREADEN (9D7) (15C6)

PU7

+5V

R6 4.7K

R5 4.7K

ST5

(9A8) ECYC 6

(9B8) ECYC 7

Y1
32.00 MHZ
(E10)

XTAL (3B2)

IC59 2925

VARIABLE CYCLE LENGTH CLOCK

(D17)

WACK

FO

C1

C2

C3

C4

FIRST

HALT

RUN

SSNC

SSNO

IC60 74S04
(D19)

STG

PU6

IC44 74S140
(C20)

R31 82

ECLK 3 (10A1)

IC61 74S140
(D20)

R35 82

R32 120

ECLK 2 (10C3,11B4, 15C2)

IC61 74S140
(D20)

R28 82

R36 120

R29 120

IC13 74S08
(A22)

EINSTR Ø

EINSTR 1

EINSTR 2

EINSTR 3

ST2

EIØ

EI 1

EI 2

EI 3

SEI Ø

SEI 1

SEI 2

SEI 3

PU7

SIGNATURE ANALYSIS JUMPER

CONDITION CODE MUX

ECLK1 (9A3, 11C6, 12B1, 13A5)

(9A7) ERAMA Ø-3

IC43 74S251
(C19)

IC60 74S04
(D19)

IC42 74S251
(C18)

IC37 74S374
(C12)

(10B6) EZEROC

(10A5) RAMDN

EZEROC

(14B8) CORRECT

(15D3) M320

PADCRC

(9C8) OUTDRDY

(4A8) ENDMRK

(9C4) IDRC

(4A8) VHP

(14B8) CCGEN

ECC

PU7

IC12 74S74
(A21)

(2D5) READEN

(9A7) ERAMA 4, 5

(9A7) ERAMB 4, 5

(9C8) EBRADD Ø-3

(9A6) EBRADD 8

EBRADD Ø

EBRADD 1

EBRADD 2

EBRADD 3

ERAMA 4

ERAMA 5

ERAMB 4

ERAMB 5

EBRADD 8

IC15 74S288
(A25)

(14B7) GCR, PE/NRZ, F/R

+5V

R4 1K

ST1

DIAGSEL (3D8)

IC112 74LS125
(J17)

EAOP Ø (9A4, 10D3, 11D2)

PU7

IC14 2910
(A24)

EI4 (9C4)

EROM 0-9 (9A2)

EROM Ø

EROM 1

EROM 2

EROM 3

EROM 4

EROM 5

EROM 6

EROM 7

EROM 8

EROM 9

MAP

FULL

VECT

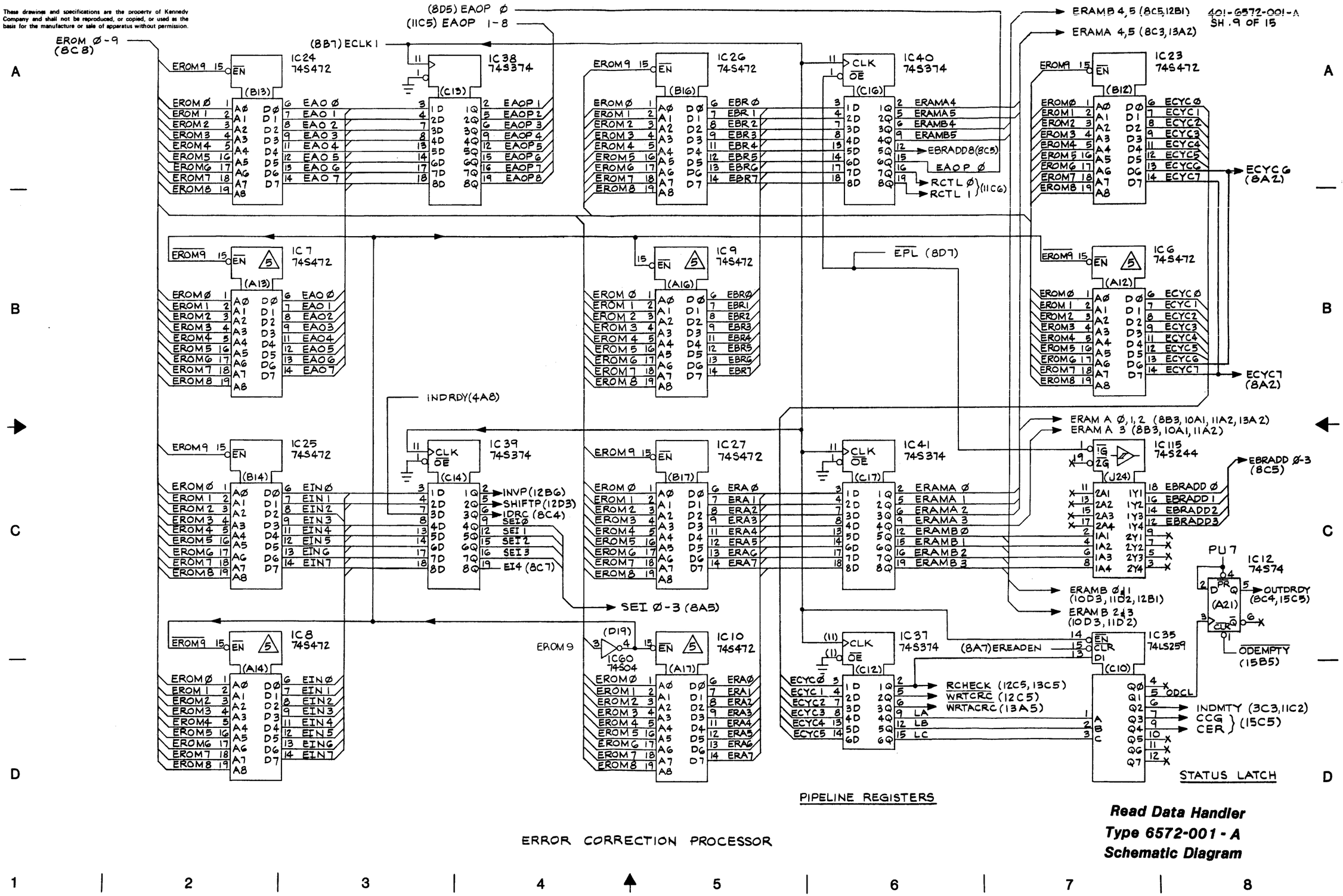
PL

EPL (9C7)

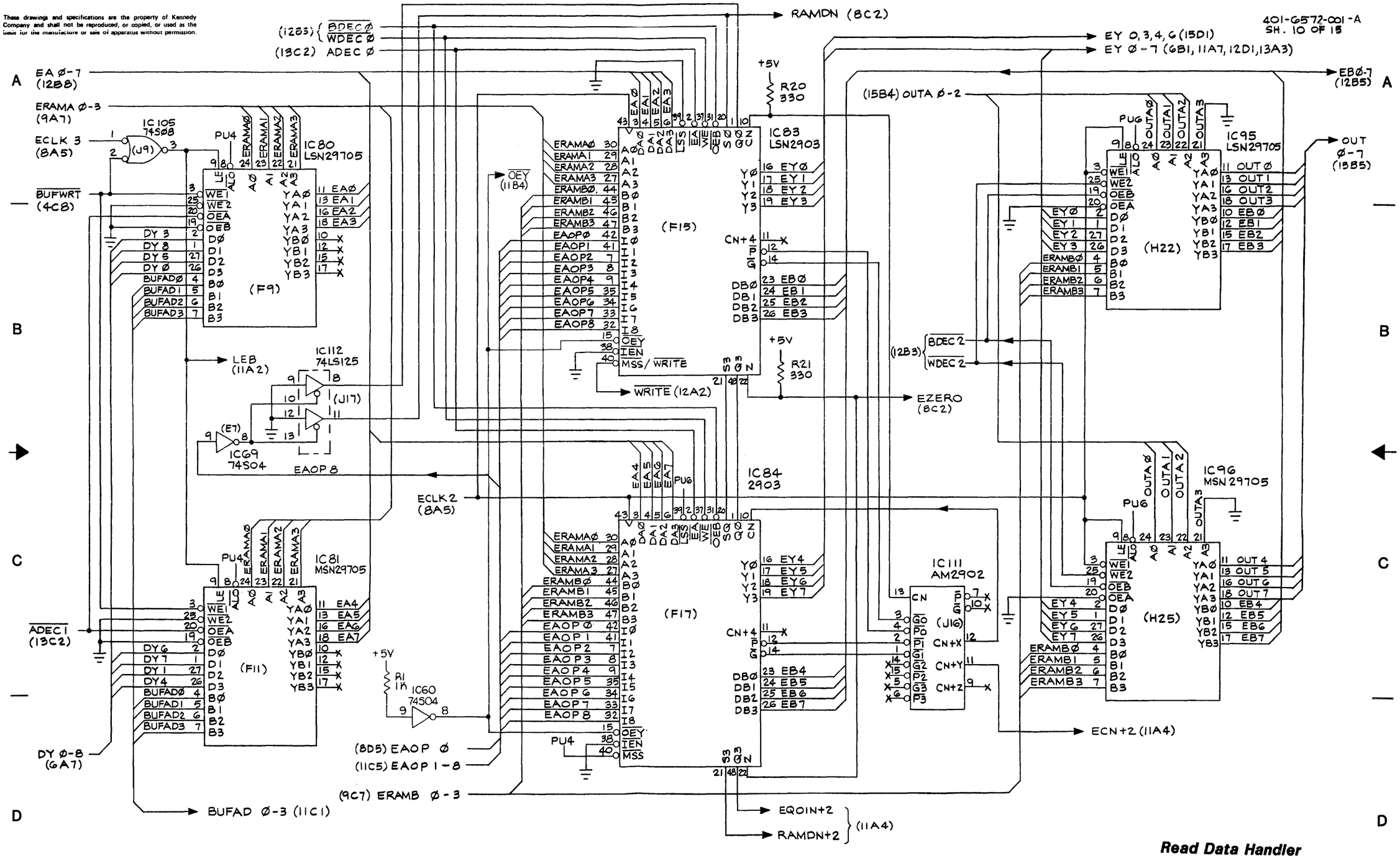
SEQUENCER

ERROR CORRECTION PROCESSOR

Read Data Handler
Type 6572-001 - A
Schematic Diagram

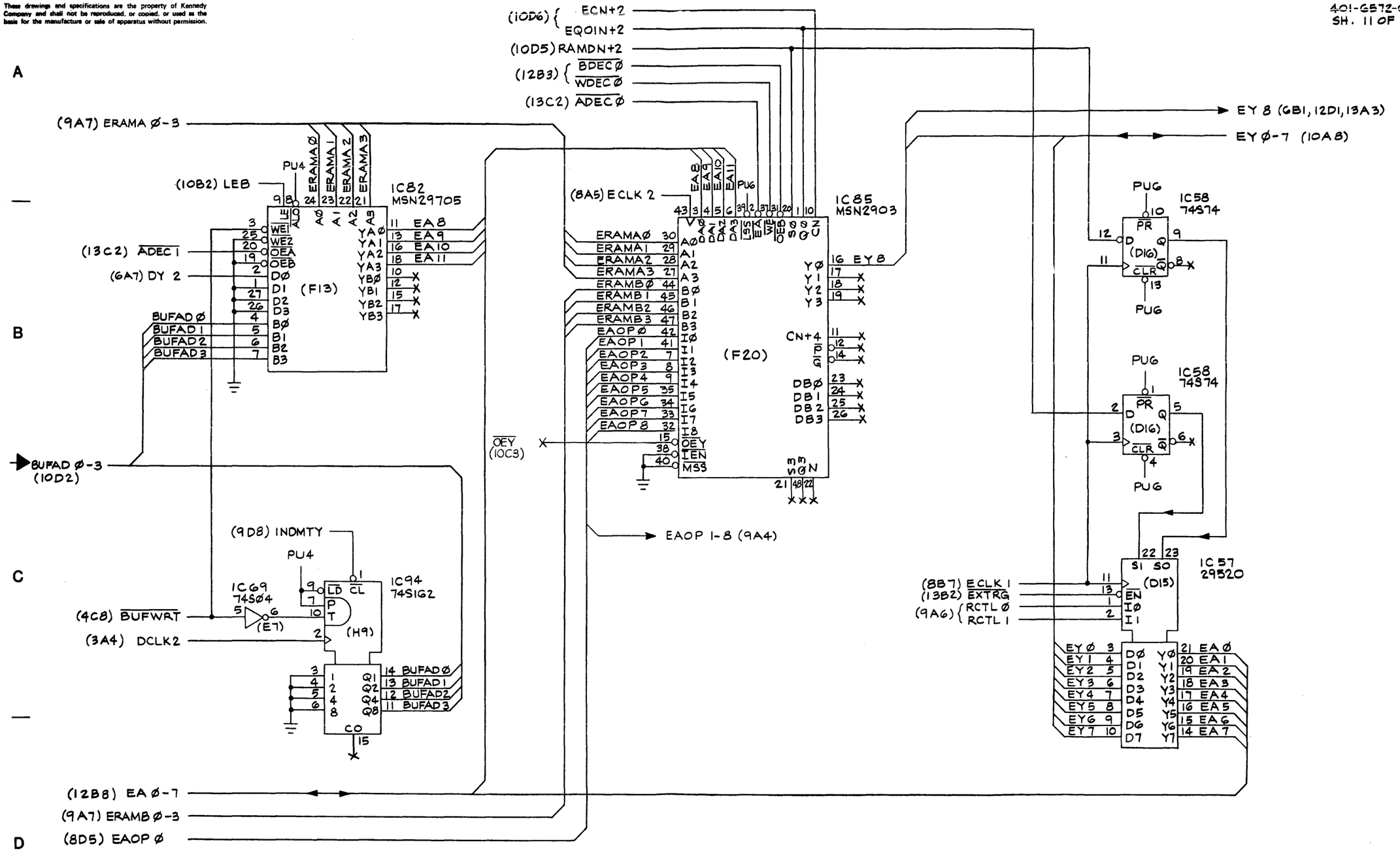


Read Data Handler
Type 6572-001 - A
Schematic Diagram



ERROR CORRECTION PROCESSOR

Read Data Handler
Type 6572-001 - A
Schematic Diagram



ERROR CORRECTION PROCESSOR

Read Data Handler
Type 6572-001 - A
Schematic Diagram

ADDRESS DECODERS

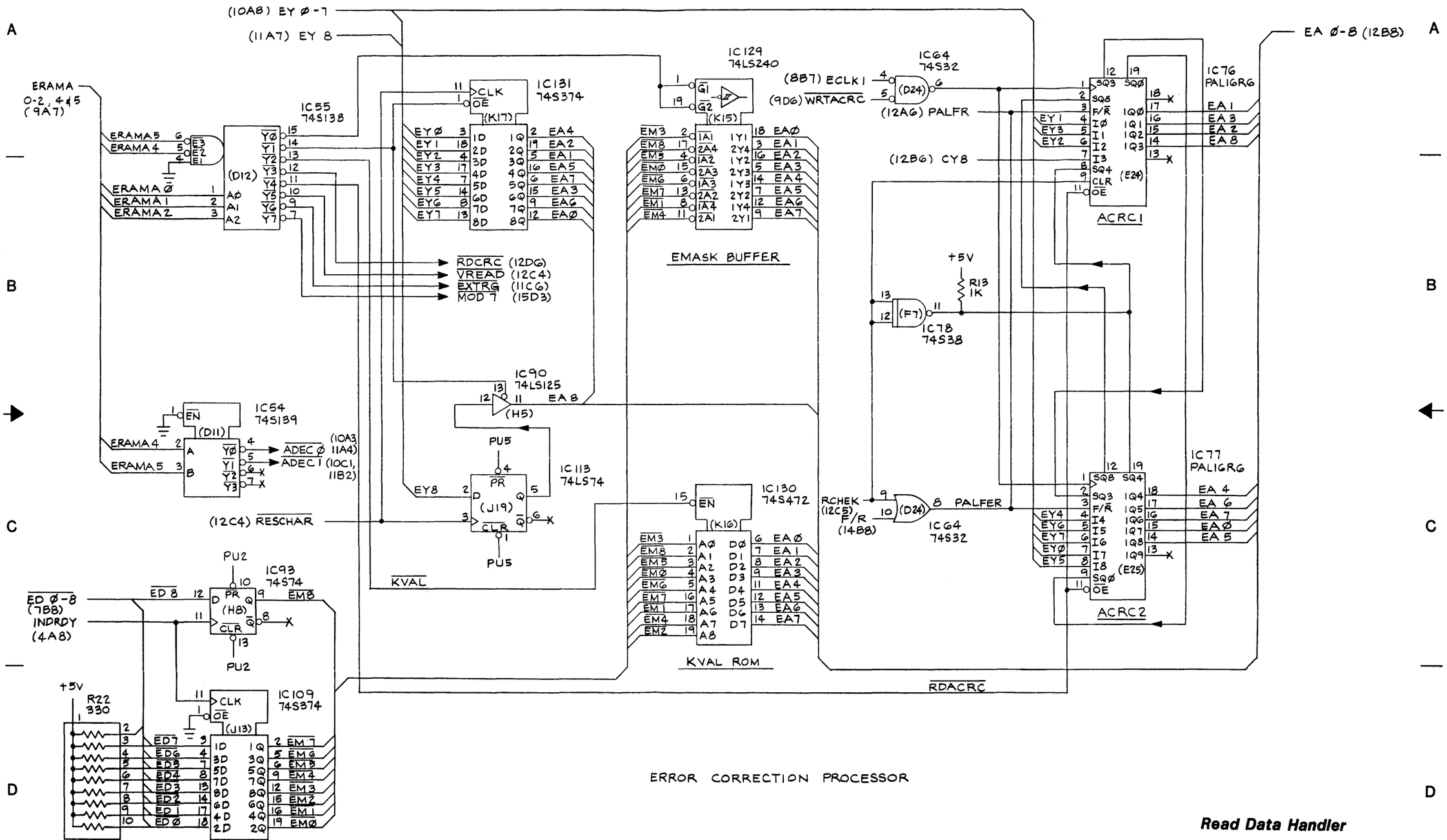
(10B4) WRITE
(8B7) ECLK1
IC56 74S32 (D13)
ENWRT
ERAMB Ø,1,4,5 (9A7)
IC53 74S139 (D10)
ERAMB4
ERAMB5
WDEC Ø (10A3, 11A4)
WDEC 2 (10B7)
BDEC Ø (10A3, 11A4)
BDEC 2 (10B6)
IC54 74S139 (D11)
ERAMBØ
ERAMB1

STATUS
IC56 74S32 (D13)
WSTAT
IC132 74S374 (K19)
EYØ EY1 EY2 EY3 EY4 EY5 EY6 EY7
G STAT 4
STAT 5
STAT G
STAT 7
STATUS LATCH

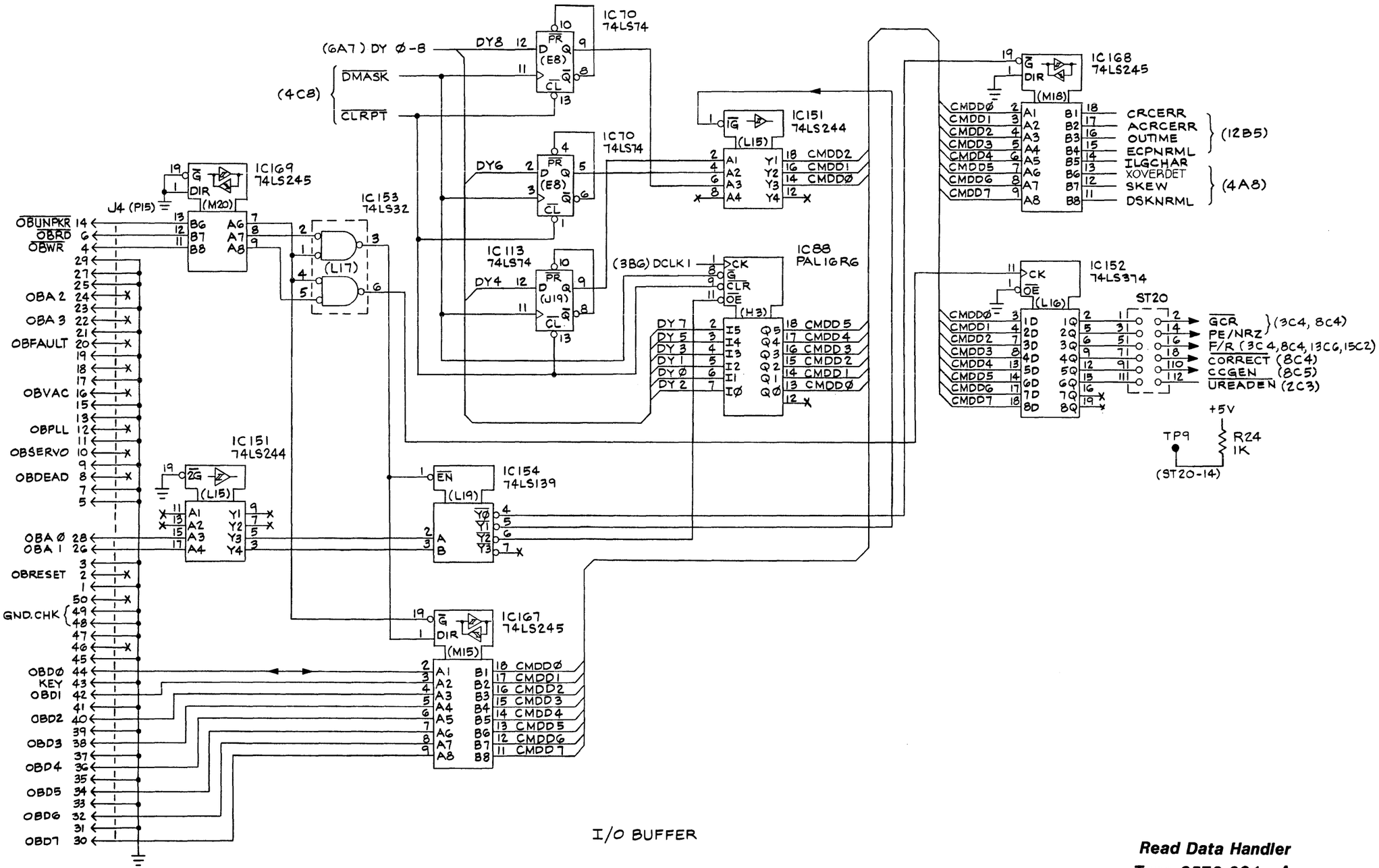
PARITY SHIFT REGISTER
IC133 74LS244 (K20)
EB Ø-7 (10A8)
EBØ EB1 EB2 EB3 EB4 EB5 EB6 EB7
CRCERR
ACRCERR
OUT TIME
ECPNRML
(14A7)

CRC/ACRC CHECKING
CY8 (13BG)
PALFR (13AG)
(9C4) INVP
IC134 74S86 (K21)
IC74 PALIGRG (E21)
SQ3 SQØ SQ8 F/R IØ I1 I2 I3 SQ4 CLR OE
IQØ IQ1 IQ2 IQ3
EAØ EA1 EA2 EA3
CRC1
EA Ø-2 (10A1, 11D2, 13A8, 15D4)
EA 3-7 (10A1, 11D2, 13A8)
EA 8 (11D2, 13A8)
+5V
R12 1K
(9D7) RCHECK
IC78 74S38 (F7)
RESCHAR (13C3, 15C2)
WSTEP (6C1)
IC56 74S32 (D13)
IC64 74S32 (D24)
PUG
WRTCRC (9D6)
IC63 74S280 (D23)
PARITY I
VREAD (13B3)
IC62 74S299 (D21)
SR SL SI SØ
EAØ EA1 EA2 EA3 EA4 EA5 EA6 EA7
IC75 PALIGRG (E23)
SQ8 SQ4 SQ3 F/R I4 I5 I6 I7 I8 SQØ OE
IQ4 IQ5 IQ6 IQ7 IQ8 IQ9
EA7 EA5 EA1 EA2 EA4
(13B3) RDCRC
CRC2
(9C3) SHIFTP
(11A7) EY 8
IC105 74S08 (J9)
EY8
EY Ø-7 (10A8)
ERROR CORRECTION PROCESSOR

Read Data Handler
Type 6572-001 - A
Schematic Diagram

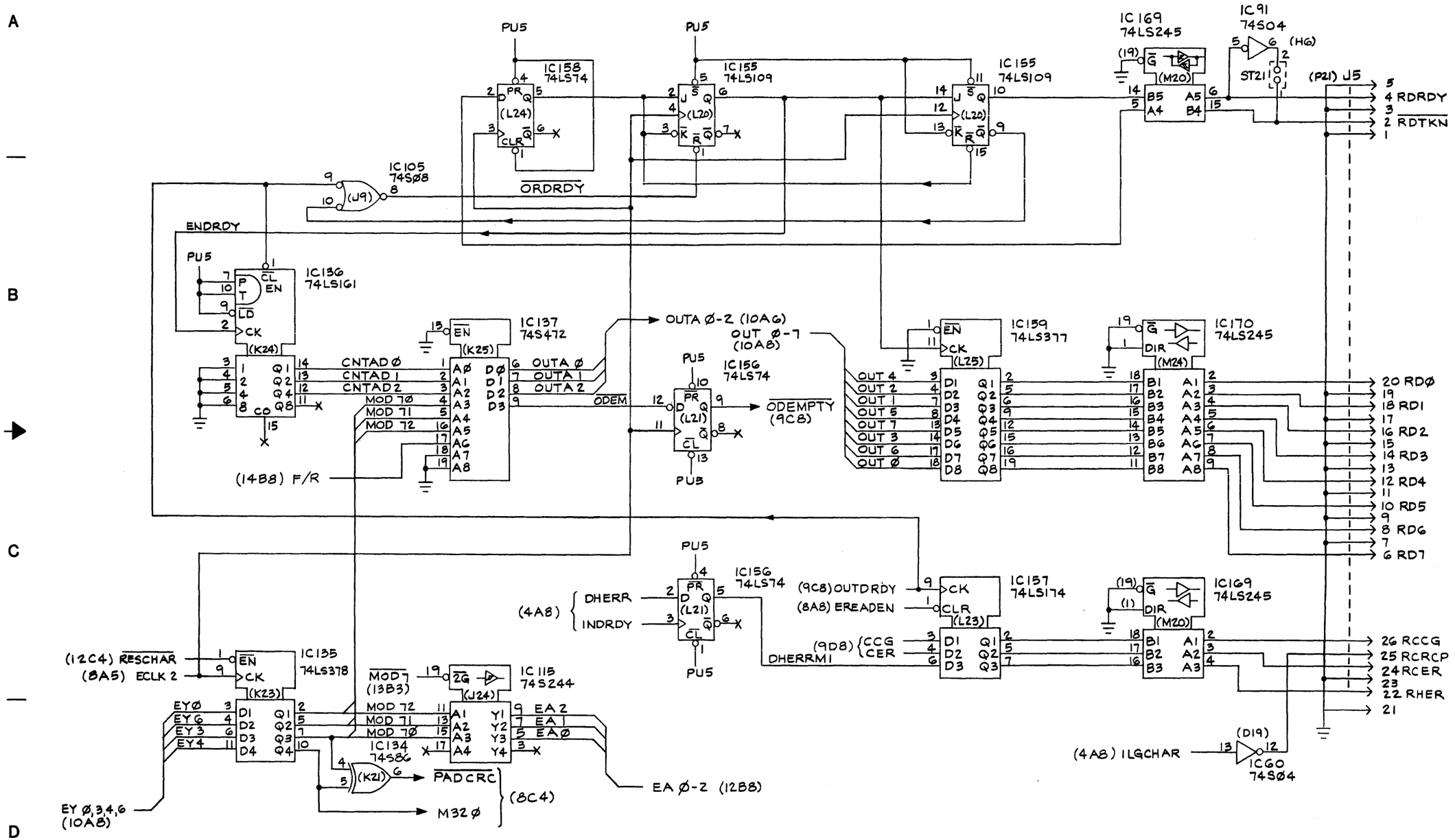


Read Data Handler
Type 6572-001 - A
Schematic Diagram



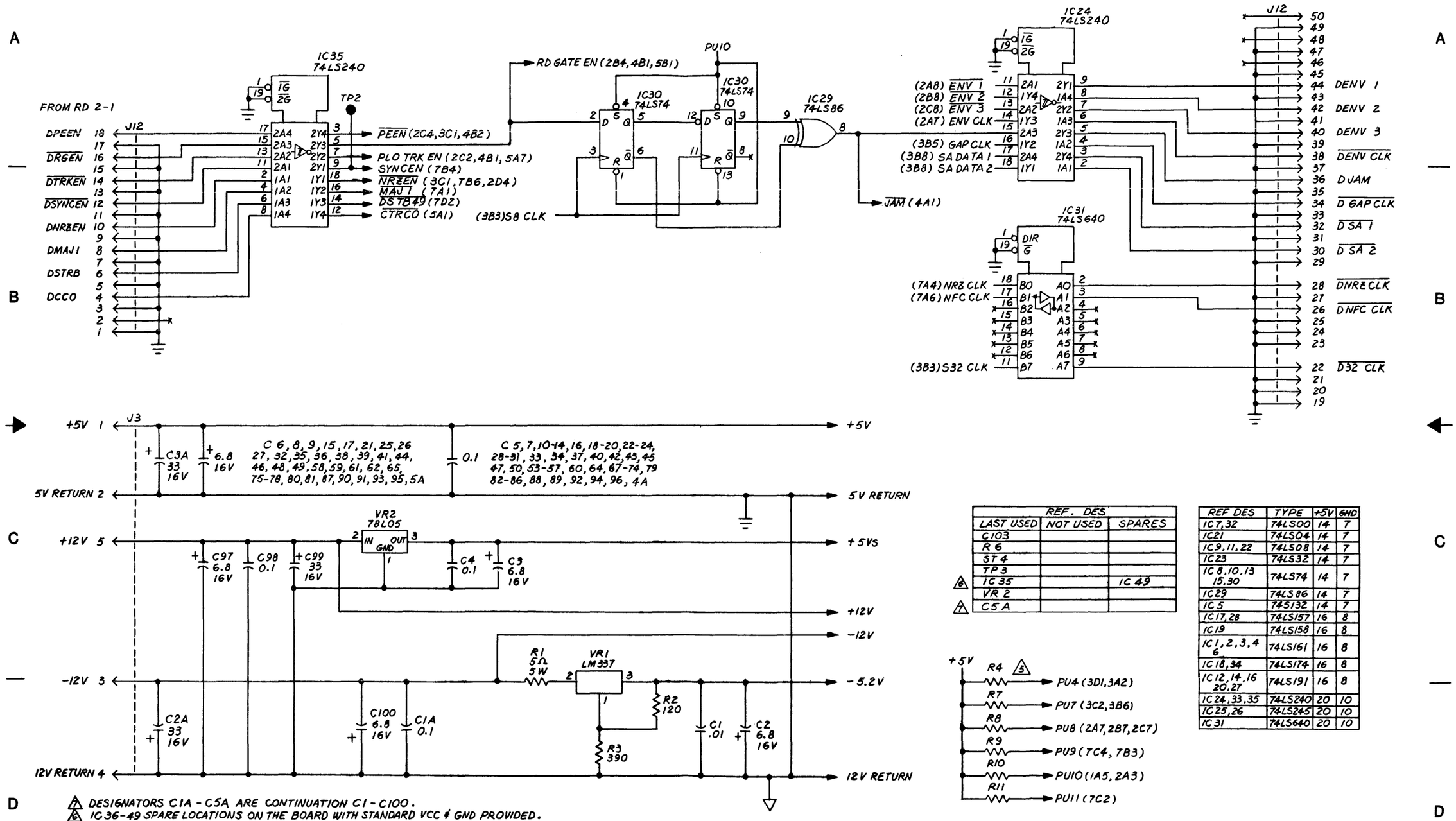
I/O BUFFER

Read Data Handler
Type 6572-001 - A
Schematic Diagram



I/O BUFFER

Read Data Handler
Type 6572-001 - A
Schematic Diagram

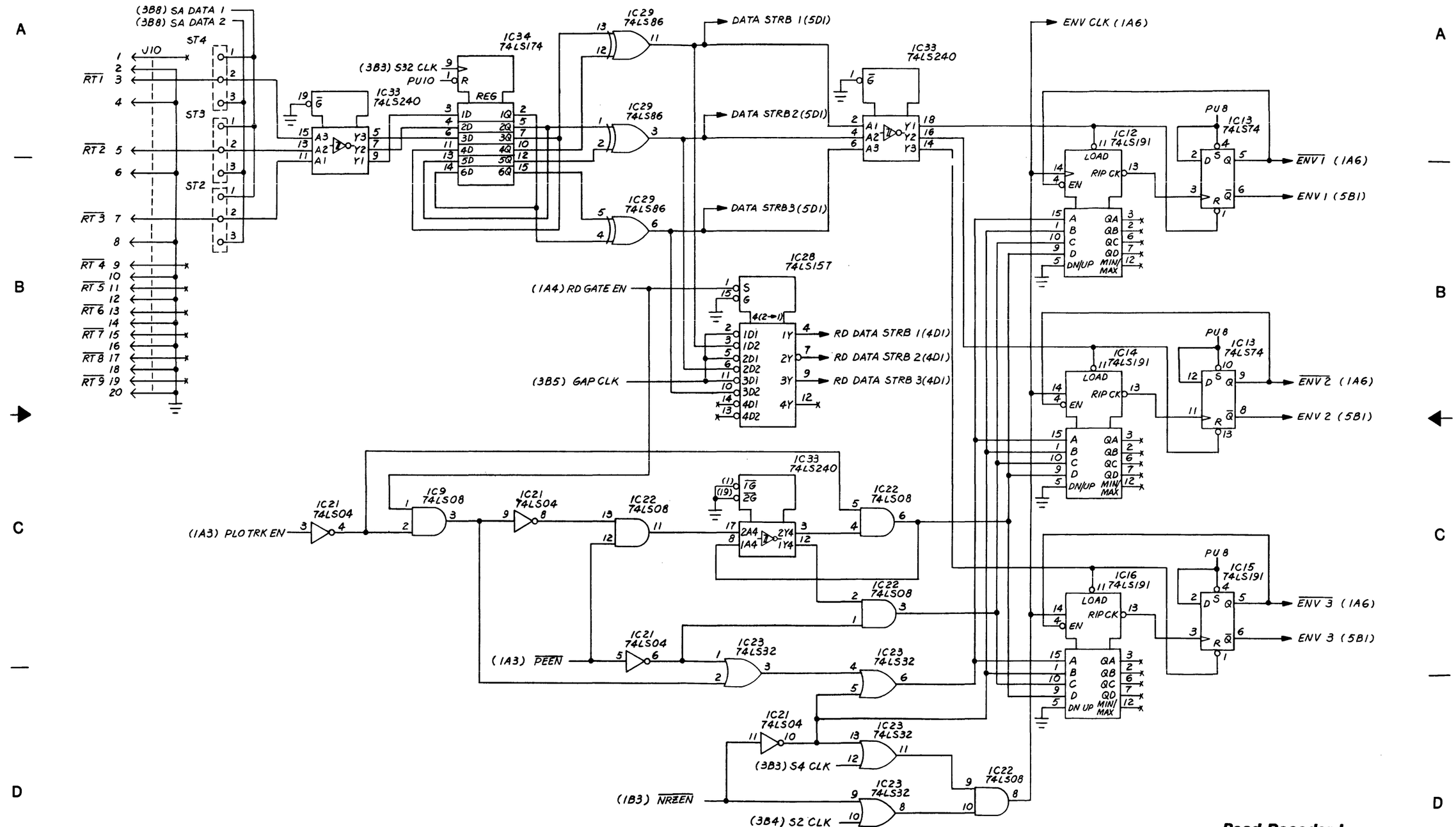


REF. DES		
LAST USED	NOT USED	SPARES
C103		
R6		
ST4		
TP3		
IC35		IC49
VR2		
C5A		

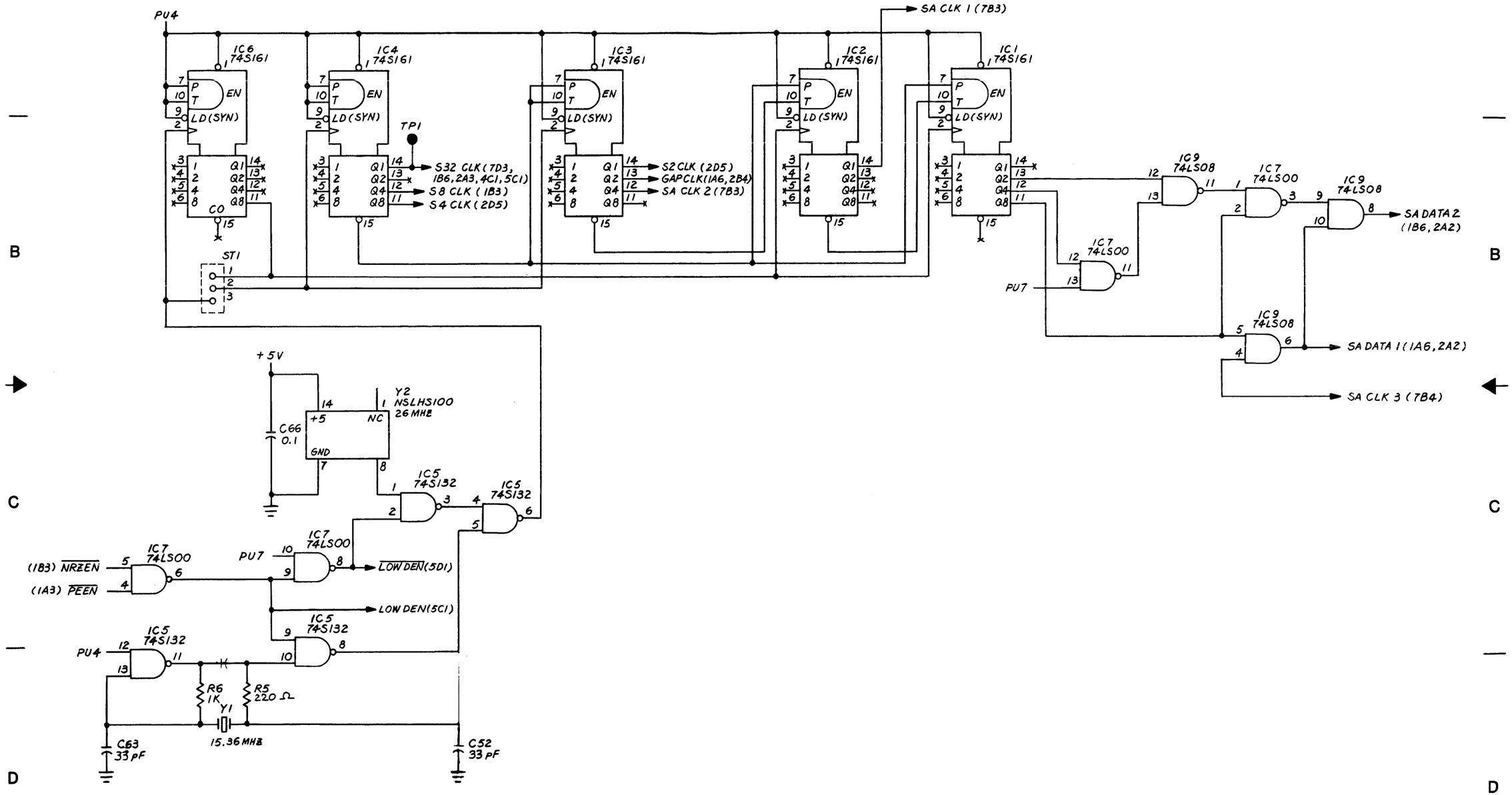
REF DES	TYPE	+5V	GND
IC7,32	74LS00	14	7
IC21	74LS04	14	7
IC9,11,22	74LS08	14	7
IC23	74LS32	14	7
IC 8,10,13 15,30	74LS74	14	7
IC29	74LS86	14	7
IC5	74S132	14	7
IC17,28	74LS157	16	8
IC19	74LS158	16	8
IC1,2,3,4 6	74LS161	16	8
IC18,34	74LS174	16	8
IC12,14,16 20,27	74LS191	16	8
IC24,33,35	74LS240	20	10
IC25,26	74LS245	20	10
IC31	74LS640	20	10

(7) DESIGNATORS C1A - C5A ARE CONTINUATION C1 - C100.
(6) IC 36-49 SPARE LOCATIONS ON THE BOARD WITH STANDARD VCC & GND PROVIDED.
(5) ALL PULL UP RESISTOR VALUES ARE 1K.
4. NOTES FOR THE TYPICAL CIRCUITS ARE SHOWN ON SHEET 6.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.
1. X INDICATES NO CONNECTION.
NOTES: UNLESS OTHERWISE SPECIFIED.

Read Decoder I
Type 6576-001 11
Schematic Diagram



Read Decoder I
Type 6576-001 11
Schematic Diagram



Read Decoder I
Type 6576-001 11
Schematic Diagram

PHASE LOCK LOOP DISCRIMINATOR-CHANNEL 1-3

(1B6) JAM 1-3

(1A3) PEEN 1-3

(1A3) PLO TRK EN 1-3

(1A4) RD GATE EN 1-3

(3B3) S32 CLK 1-3

(5C5) * VCO 32 NO.

THIS * SIGNAL IS CONNECTED TO A SIGNAL FROM AN * * ADJACENT CHANNEL AS NOTED :

*CHAN 1 TO * *CHAN 3
*CHAN 2 TO * *CHAN 1
*CHAN 3 TO * *CHAN 2

(5C5) * * VCO 32 NO. (SEE NOTE ABOVE)

(2A5) RD DATA STRB NO. 1
(2A5) RD DATA STRB 2
(2B5) RD DATA STRB 3

RLCK NO. (5A6)

PH STRB NO. (5C5)

PHSTR NO. (5C7)

JAMLD NO. (5C3)

XOVER NO. (5B6)

PTRK NO. (5B4)

VSTB NO. (5A4)

RL STRB NO. (5A6)

PMP TRK NO. (6B2)

PMP PE NO. (6B2)

PMP PE NO. (6C2)

PMP TRK NO. (6B2)

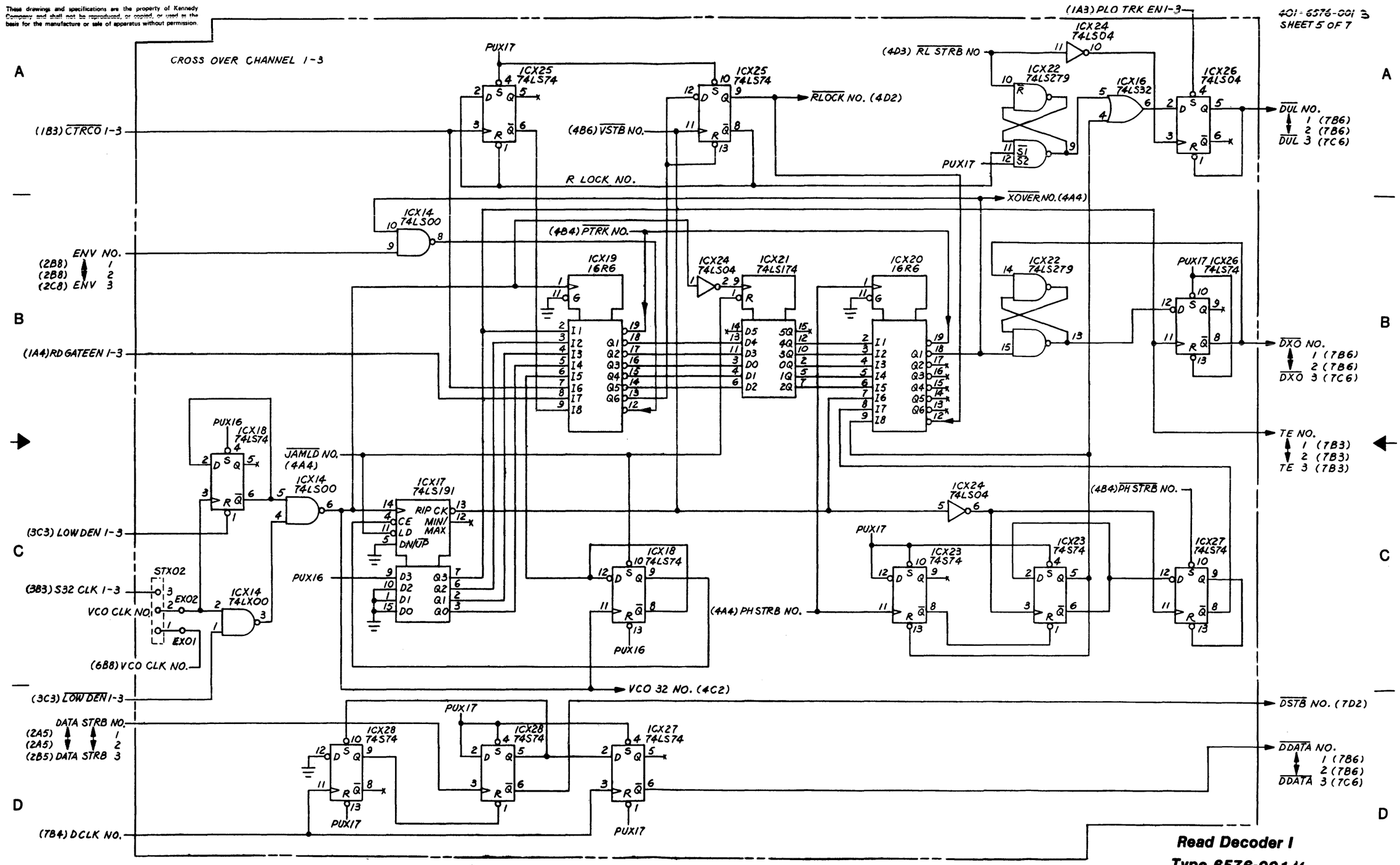
PMP AQ NO. (6B2)

PMP AQ NO. (6C2)

ICX22 74LS274 · ICX24 74LS04 · ICX24 74LS04 · ICX10 74LS74 · ICX06 74LS74 · ICX06 74LS74 · ICX22 74LS279 · ICX07 74LS08 · ICX08 74LS00 · ICX07 74LS08 · ICX24 74LS04 · ICX08 74LS00 · ICX10 74LS74 · ICX07 74LS08 · ICX12 74LS32 · ICX15 74LS74 · ICX16 74LS32 · ICX15 74LS74 · ICX12 74LS32 · ICX08 74LS00 · ICX12 74LS32 · ICX16 74LS32 · ICX05 74LS157 · ICX13 74LS191 · ICX14 74LS00 · ICX08 74LS00 · ICX16 74LS32 · ICX07 74LS08 · ICX11 74LS193 · ICX09 74LS74 · ICX09 74LS74

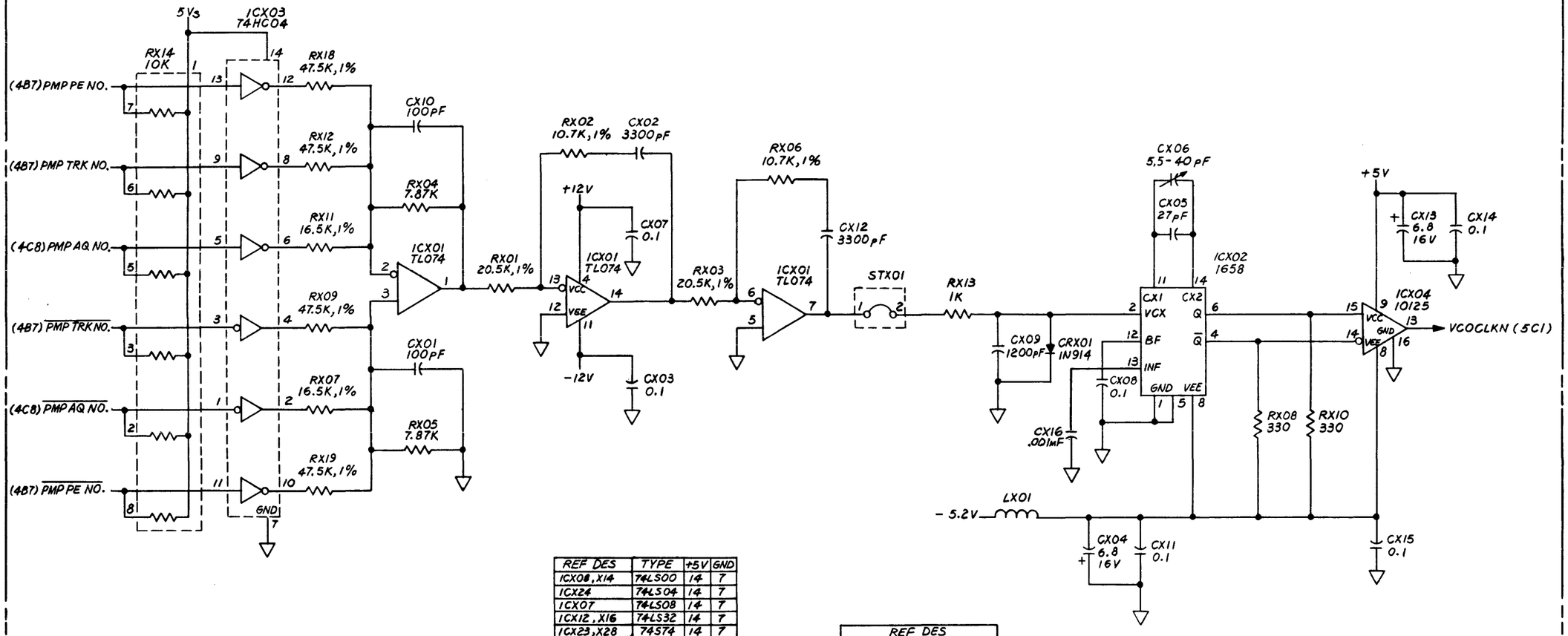
PUX15 · PUX16 · PUX16

Read Decoder I
Type 6576-001 11
Schematic Diagram



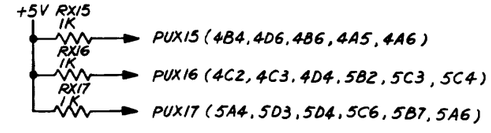
Read Decoder I
Type 6576-0011
Schematic Diagram

VCO PART OF TYPICAL CIRCUITS CHANNEL 1-3



REF DES	TYPE	+5V	GND
1CX08,X14	74LS00	14	7
1CX24	74LS04	14	7
1CX07	74LS08	14	7
1CX12,X16	74LS32	14	7
1CX23,X28	74S74	14	7
1CX06,X09 X10,X15,X18 X25,X26,X27	74LS74	14	7
1CX05	74LS157	16	8
1CX21	74LS174	16	8
1CX13,X17	74LS191	16	8
1CX11	74LS193	16	8
1CX22	74LS279	16	8
1CX19,20	16R6	20	10

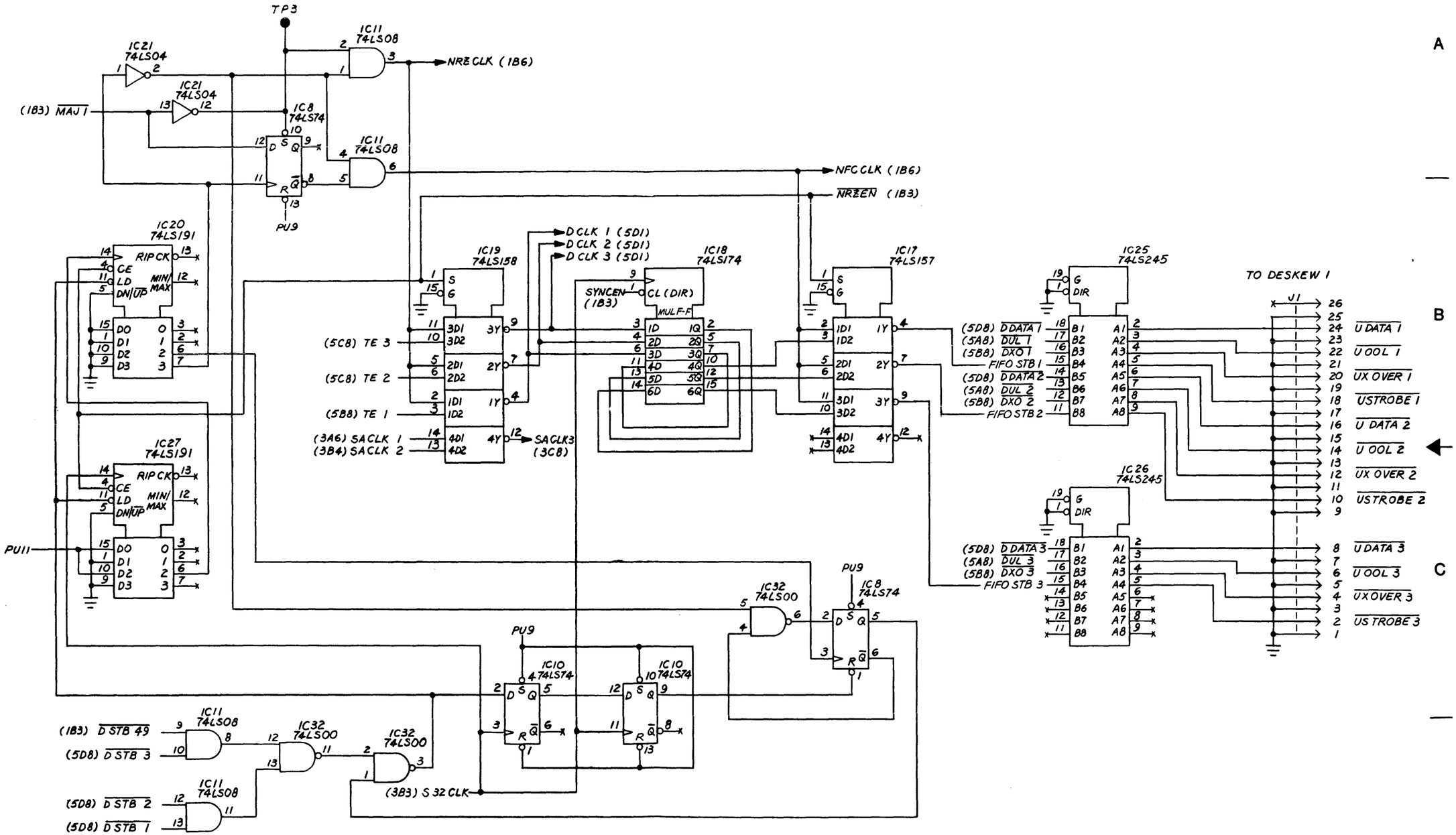
REF DES	
LAST USED	NOT USED
CX16	
CRX01	
1CX28	
LX01	
RX19	
STX01	
EX02	
PUX17	PUX1-14



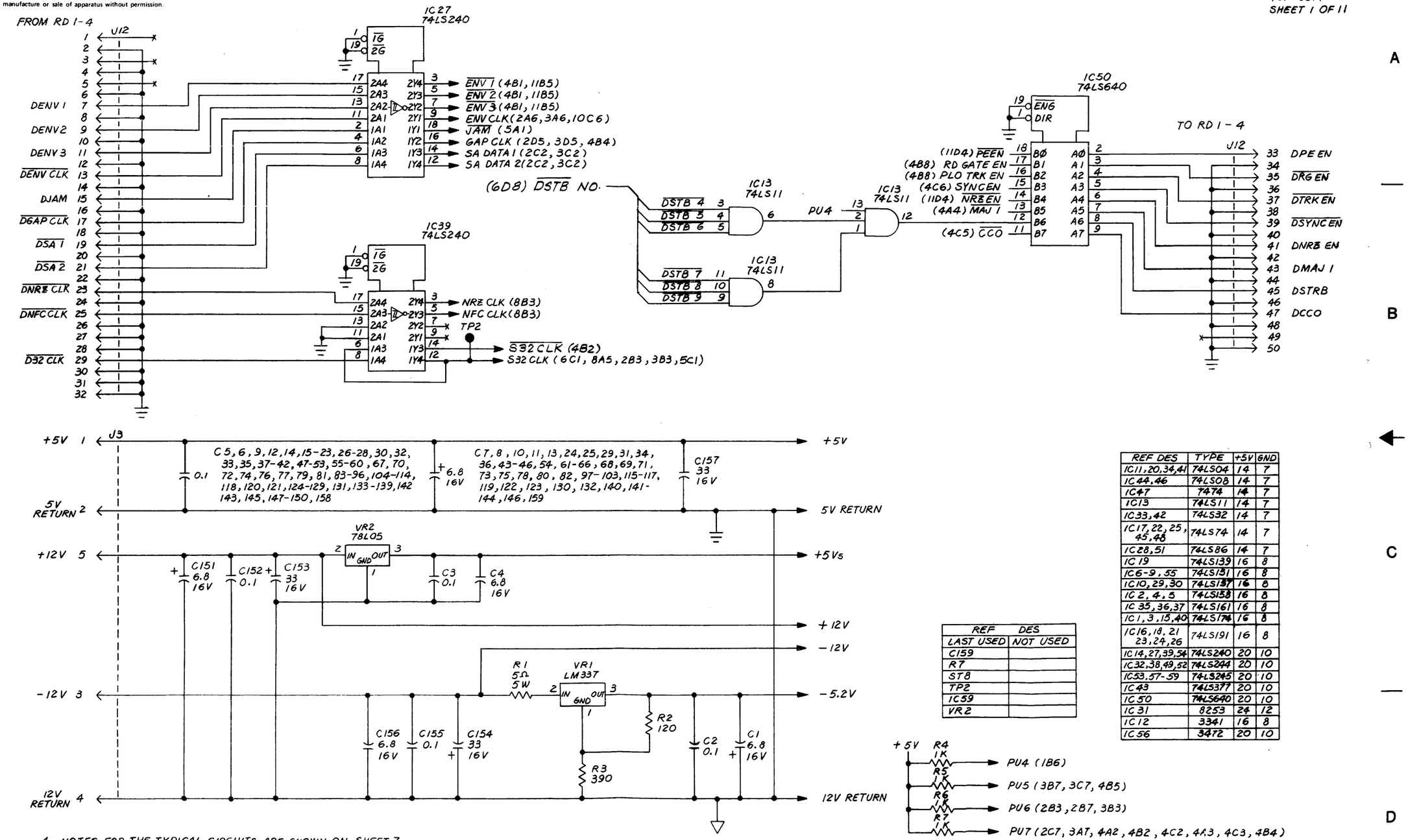
3. A FUNCTION DESIGNATING THE NUMBERS CONNECT ALL CHANNELS IN THAT CKT TOGETHER.
   ie: THE SOURCE TIES TO CHAN 1, 2 & 3.
2. THE ABBREVIATION NO. AFTER A FUNCTION SHALL CONNECT EACH CHANNEL SEPERATERY.
   ie: (CHAN 1 TO 1; 2 TO 2 & ETC).
1. CIRCUITS SHOWN WITHIN PHANTOM LINES IS USED 3 TIMES. CHAN 1 THRU 3. CHAN NUMBER REPLACES THE X IN THE REF DES NUMBER FOR APPROPRIATE CHAN.
   ie: RX01 { SHALL BE R101 FOR CHAN 1. SHALL BE R301 FOR CHAN 3.

NOTES: UNLESS OTHERWISE SPECIFIED.

Read Decoder I
Type 6576-001 11
Schematic Diagram



Read Decoder I
Type 6576-001 11
Schematic Diagram



REF DES	TYPE	+5V	GND
IC11,20,34,41	74LS04	14	7
IC44,46	74LS08	14	7
IC47	7474	14	7
IC13	74LS11	14	7
IC33,42	74LS32	14	7
IC17,22,25, 45,48	74LS74	14	7
IC28,51	74LS86	14	7
IC19	74LS139	16	8
IC6-9,55	74LS151	16	8
IC10,29,30	74LS157	16	8
IC2,4,5	74LS158	16	8
IC35,36,37	74LS161	16	8
IC1,3,15,40	74LS174	16	8
IC16,18,21 23,24,26	74LS191	16	8
IC14,27,39,54	74LS240	20	10
IC32,38,49,52	74LS244	20	10
IC53,57-59	74LS245	20	10
IC43	74LS377	20	10
IC50	74LS640	20	10
IC31	8253	24	12
IC12	3341	16	8
IC56	3472	20	10

REF DES	
LAST USED	NOT USED
C159	
R7	
ST8	
TP2	
IC59	
VR2	

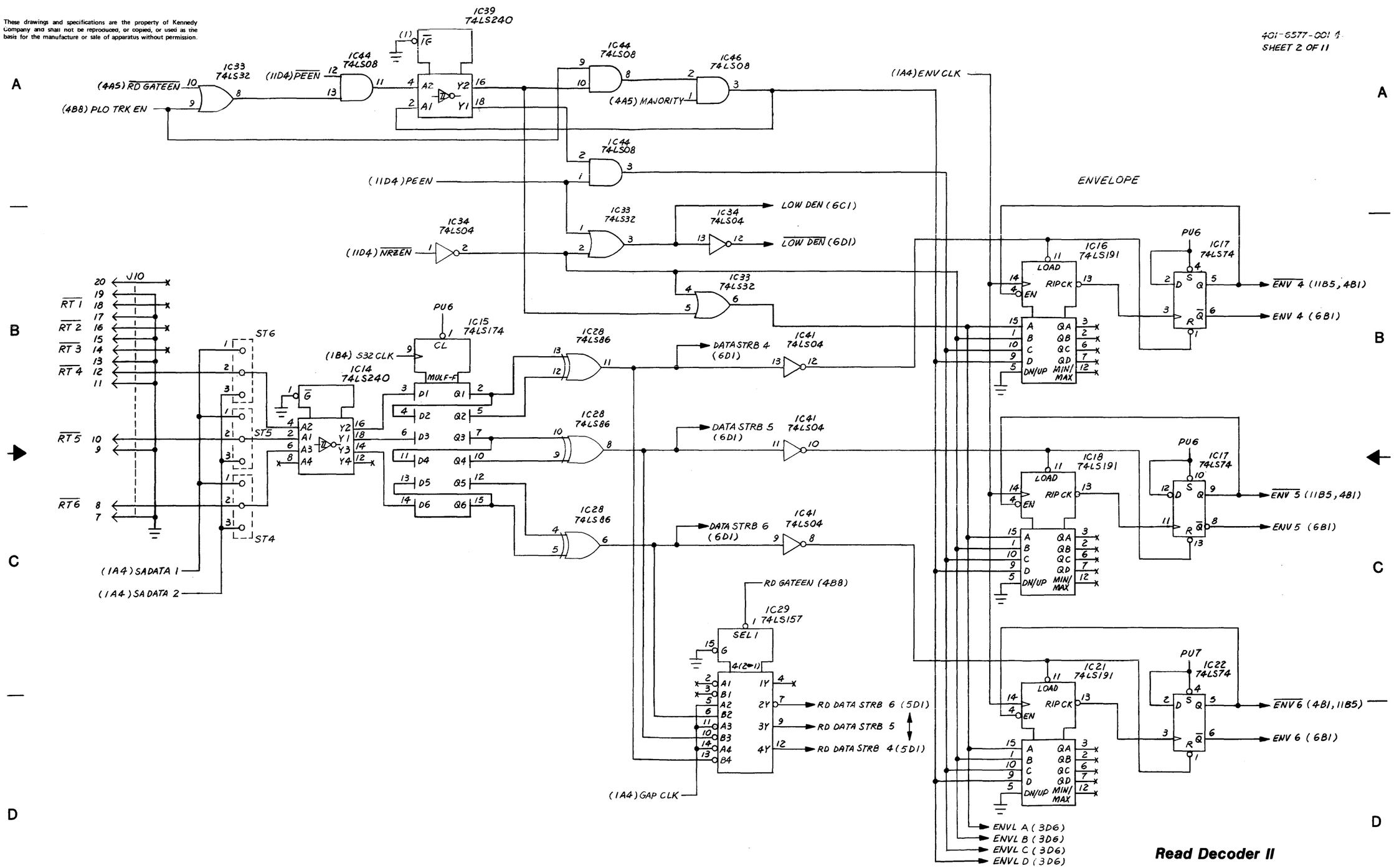
4. NOTES FOR THE TYPICAL CIRCUITS ARE SHOWN ON SHEET 7.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.
1. X INDICATES NO CONNECTION.

NOTES: UNLESS OTHERWISE SPECIFIED.

Read Decoder II

Type 6577-001 12

Schematic Diagram



Read Decoder II
Type 6577-00112
Schematic Diagram

ENVELOPE

(1A4) ENV CLK

(1A4) SA DATA 1

(1A4) SA DATA 2

(1B4) S32 CLK

(1A4) GAP CLK

RD GATE EN (4B8)

DATA STRB 7 (6D1)

DATA STRB 8 (6D1)

DATA STRB 9 (6D1)

RD DATA STRB 7 (5D1)

RD DATA STRB 8

RD DATA STRB 9 (5D1)

(2D7) ENVL D

(2D7) ENVL C

(2D7) ENVL B

(2D7) ENVL A

ENV 7 (4B1, 11B5)

ENV 7 (6B1)

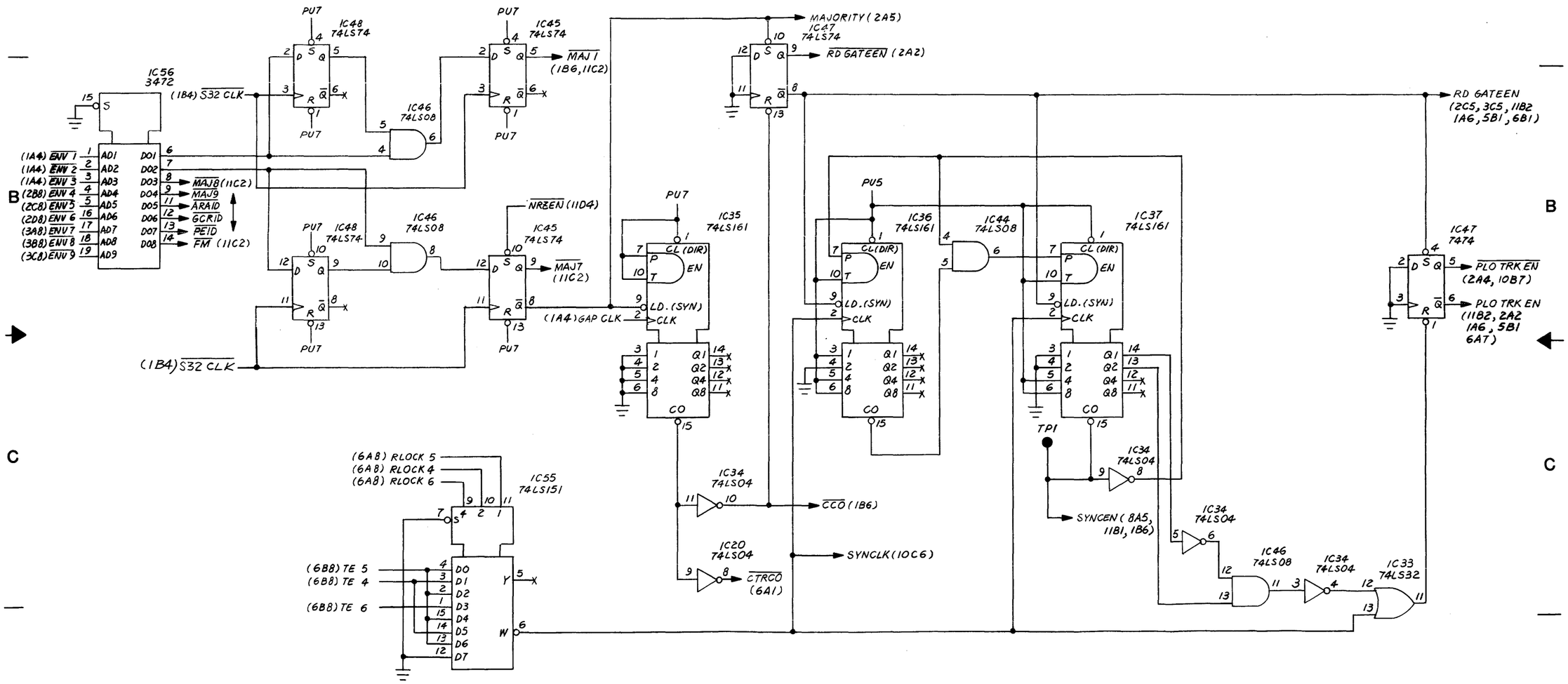
ENV 8 (4B1, 11B5)

ENV 8 (6B1)

ENV 9 (4B1, 11B6)

ENV 9 (6B1)

Read Decoder II
Type 6577-001 12
Schematic Diagram



Read Decoder II
Type 6577-0011 2
Schematic Diagram

PHASE LOCK LOOP DISCRIMINATOR CHANNEL 4-9

(1A4) $\overline{JAM}$ 4-9

(11D4) $\overline{PEEN}$ 4-9

(4B8) PLO TRK EN 4-9

(4B8) RD GATE EN 4-9

(1A4) S32 CLK 4-9

(6C5) * VCO 32 NO.

THIS * SIGNAL IS CONNECTED TO A SIGNAL FROM AN ** ADJACENT CHANNEL AS NOTED :

* CHAN 4 5 6 7 8 TO **CHAN 6 4 5 7 9
* CHAN 9 TO **CHAN 8
** VCO 32 NO. (SEE NOTE ABOVE)

RD DATA STRB NO.

(2D6) 4
(2D6) 5
(2D6) 6
(3D6) 7
(3D6) 8
(3D6) RD DATA STRB 9

PH STRB NO. (6C5)

$\overline{JAMLD}$ NO. (6C3)

$\overline{PHSTR}$ NO. (6C7)

(6B7) $\overline{XOVER}$ NO.

$\overline{PTRK}$ NO. (6B7)

$\overline{RLCK}$ NO. (6A6)

$\overline{RL\ STRB}$ NO. (6A6)

$\overline{RLOCK}$ NO. (6A6)

$\overline{VSTB}$ NO. (6A4)

PMP TRK NO. (7B1)

PMP PE NO. (7B1)

$\overline{PMP\ PE}$ NO. (7C1)

$\overline{PMP\ TRK}$ NO. (7B1)

PMP AQ NO. (7B1)

$\overline{PMP\ AQ}$ NO. (7C1)

ICX22 74LS279
ICX07 74LS08
ICX10 74LS74
ICX06 74LS74
ICX06 74LS74
ICX22 74LS274
ICX24 74LS04
ICX07 74LS08
ICX08 74LS00
ICX24 74LS04
ICX08 74LS00
ICX24 74LS04
ICX07 74LS08
ICX10 74LS74
ICX12 74LS32
ICX15 74LS74
ICX16 74LS32
ICX15 74LS74
ICX12 74LS32
ICX08 74LS00
ICX12 74LS32
ICX16 74LS32
ICX05 74LS157
ICX13 74LS191
ICX07 74LS08
ICX14 74LS00
ICX08 74LS00
ICX16 74LS32
ICX09 74LS74
ICX11 74LS193
ICX09 74LS74

PUX15
PUX16

Read Decoder II
Type 6577-001 12
Schematic Diagram

401-6577-001 4
SHEET 6 OF 11

CROSS OVER CHANNEL 4-9

(6B8) PLO TRK EN NO.

(4C5) $\overline{CTRCO}$ 4-9

(5B6) $\overline{VSTB}$ NO.

$\overline{RLOCK}$ NO. (5D2, 5B5)

(5D3) $\overline{RL\ STRB}$ NO.

PUX17

ICX25 74LS74

ICX24 74LS04

ICX22 74LS279

ICX16 74LS32

ICX26 74LS04

$\overline{DUL}$ NO.
4 (9A5)
5 (9B5)
6 (9B5)
7 (9B5)
8 (9C5)
$\overline{DUL}$ 9 (9C5)

RLOCK NO.
4 (4C3)
5 (4C3)
RLOCK 6 (4C3)

ENV NO.
(2B8) 4
(2C8) 5
(2D8) 6
(3B8) 7
(3B8) 8
(3C8) ENV 9

ICX14 74LS00

ICX19 16R6

ICX24 74LS04

ICX21 74LS174

ICX20 16R6

$\overline{PTRK}$ NO. (5B6)

$\overline{XOVER}$ NO. (5A4)

PUX17 ICX26 74LS74

$\overline{DXO}$ NO.
4 (9A5, 11C4)
5 (9B5
6 (9B5
7 (9B5
8 (9C5, 11C4)
$\overline{DXO}$ 9 (9C5, 11B4)

(4B8) RDGATE EN 4-9

PUX16 ICX18 74LS74

TE NO.
4 (8A3)
5 4D3)
6 4D3)
7 4D3)
8
TE 9 (8A3)

$\overline{JAMLD}$ NO. (5B4)

ICX17 74LS191

ICX14 74LS00

ICX24 74LS04

(5B3) $\overline{PH\ STRB}$ NO.

(2A5) LOWDEN 4-9

STX02

S32 CLK 4-9

VCO CLK NO.

EX02

EX01

(7B8) VCO CLK NO.

ICX18 74LS74

ICX23 74S74

ICX23 74L74

ICX27 74LS74

(5A3) PH STRB NO.

VCO32 NO. (5C2)

(2B5) $\overline{LOWDEN}$ 4-9

$\overline{DSTB}$ NO. (1B4)

DATA STRB NO.
(2B5) 4
(2B5) 5
(2C5) 6
(3B5) 7
(3B5) 8
(3B5) DATA STRB 9

ICX28 74S74

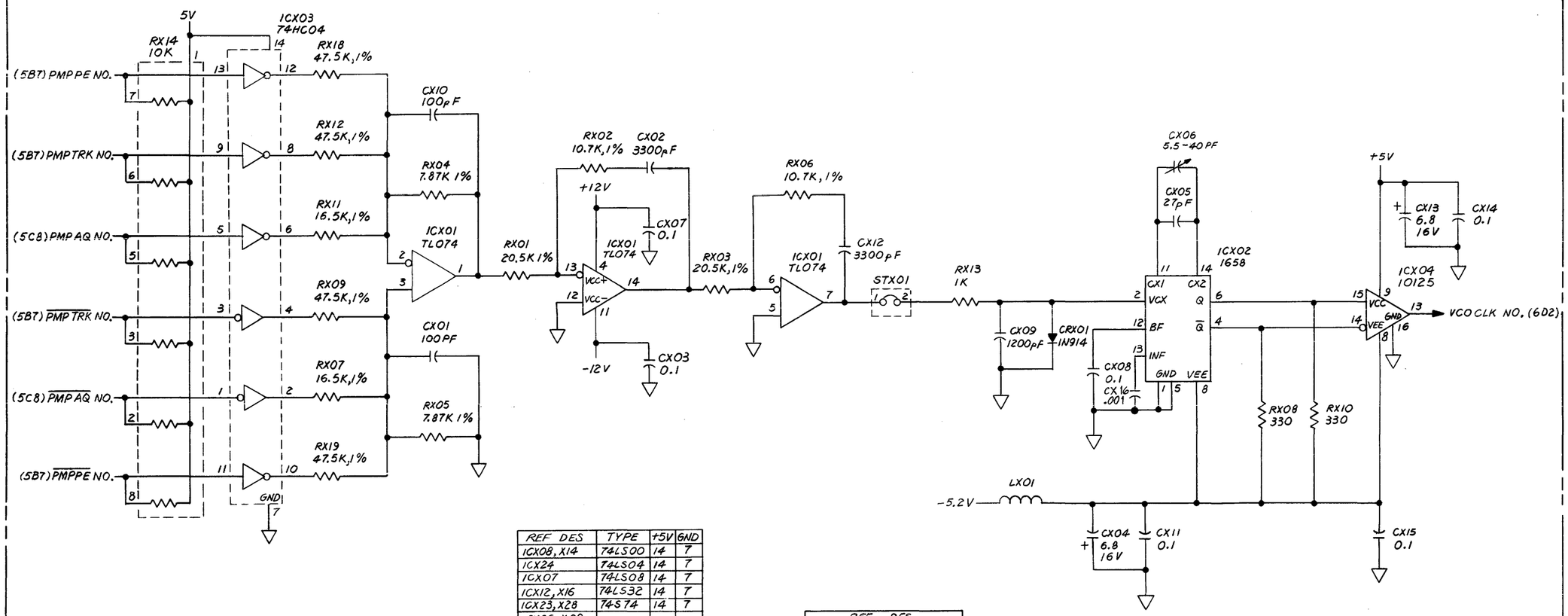
ICX27 74LS74

$\overline{D\ DATA}$ NO.
4 (9B5, 11D5)
5
6
7 (9B5, 11D5)
8 (9C5, 11D5)
$\overline{D\ DATA}$ 9 (9C5, 11B6)

(8A5) DCLK NO.

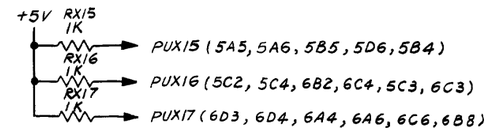
Read Decoder II
Type 6577-001 12
Schematic Diagram

VCO PART OF TYPICAL CIRCUITS CHANNEL 4 - 9



REF DES	TYPE	+5V	GND
ICX08, X14	74LS00	14	7
ICX24	74LS04	14	7
ICX07	74LS08	14	7
ICX12, X16	74LS32	14	7
ICX23, X28	74S74	14	7
ICX06, X09 X10, X15, X18 X25-X27,	74LS74	14	7
ICX05	74LS157	16	8
ICX21	74LS174	16	8
ICX13, X17	74LS191	16	8
ICX11	74LS193	16	8
ICX22	74LS279	16	8
ICX19, 20	16R6	20	10

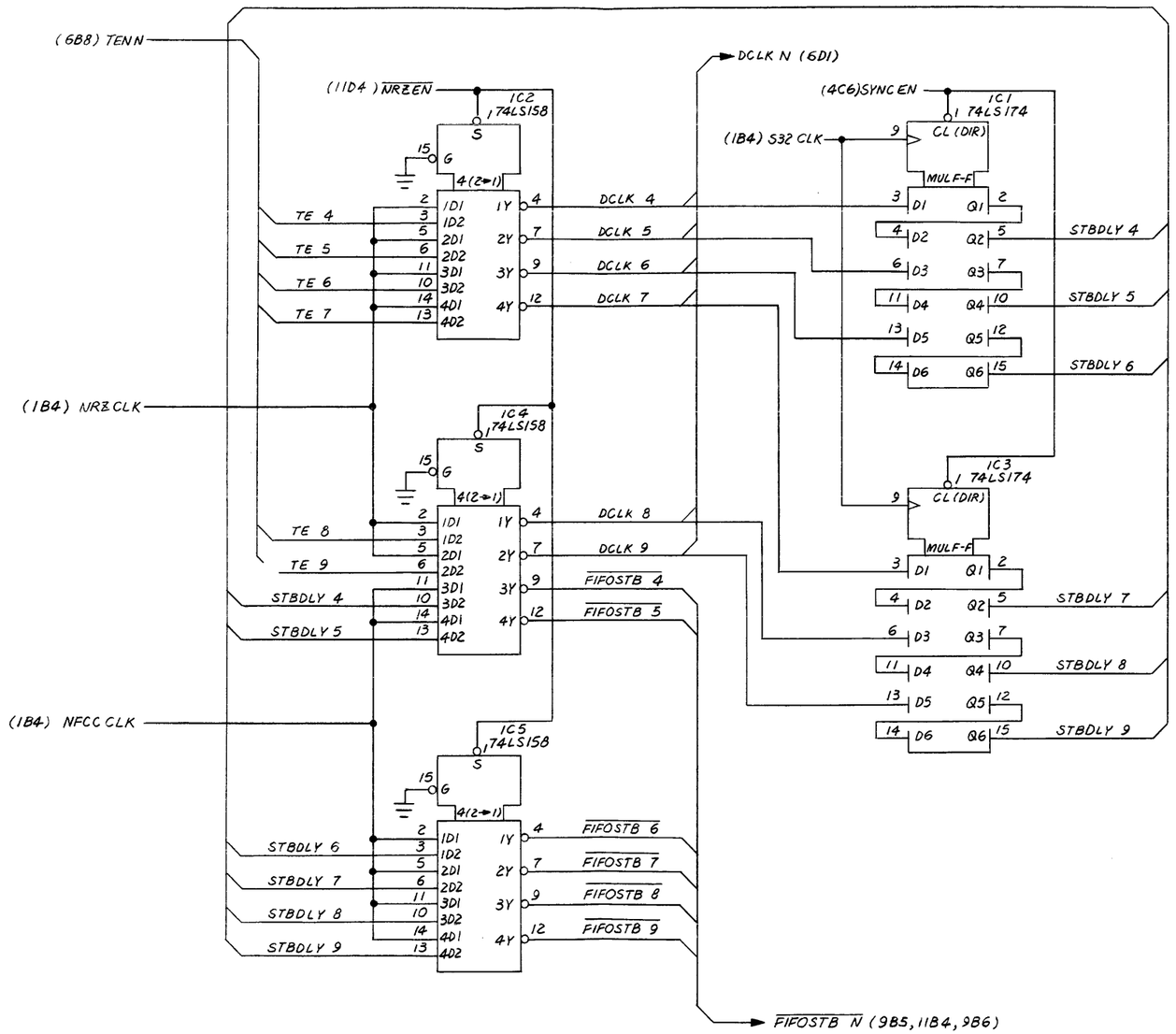
REF DES	
LAST USED	NOT USED
CX16	
CRX01	
ICX 28	
LX01	
RX19	
STX01	
EX02	
PUX17	PUX1-14



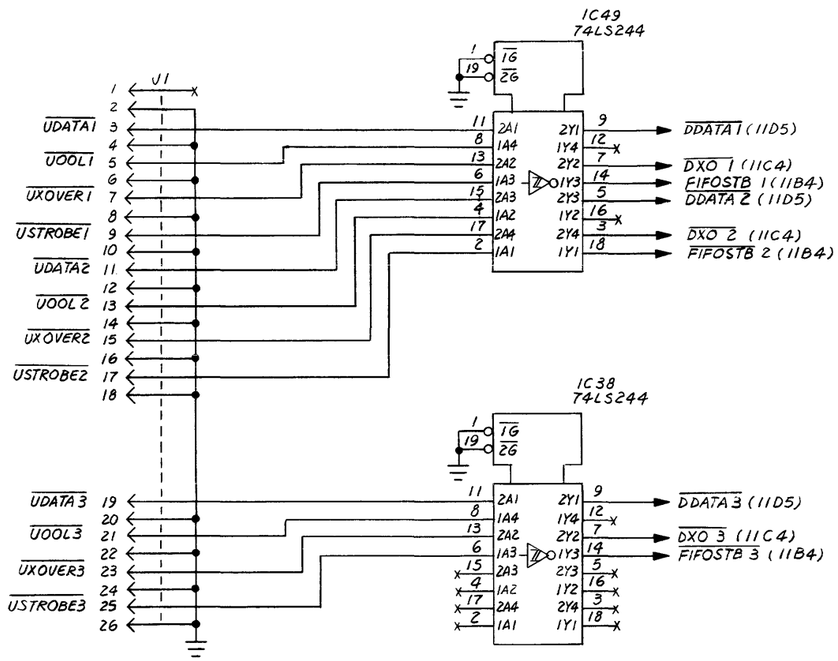
3. A FUNCTION DESIGNATING THE NUMBERS CONNECT ALL CHANNELS IN THAT CKT TOGETHER.
   ie: THE SOURCE TIES TO CHAN 1, 2, 3, 4 ETC.
2. THE ABREVIATION NO. AFTER A FUNCTION SHALL CONNECT EACH CHANNEL SEPERATELY.
   ie: (CHAN 1 TO 1 ; 2 TO 2 & ETC).
1. CIRCUITS SHOWN WITHIN PHANTOM LINES IS USED 6 TIMES. CHAN 4 THRU 9. CHAN NUMBER REPLACES THE X IN THE REF DES NUMBER FOR APPROPRIATE CHAN.
   ie: RX01 { SHALL BE R601 FOR CHAN 6. / SHALL BE R901 FOR CHAN 9.

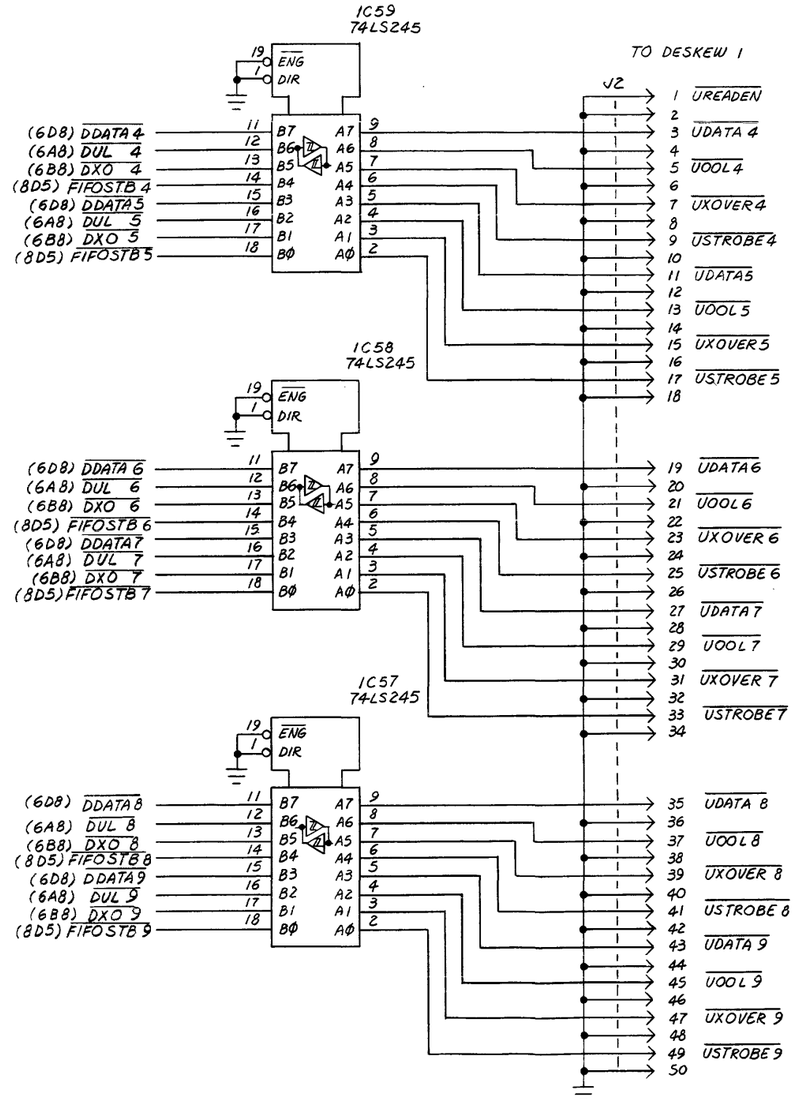
NOTES:

Read Decoder II
Type 6577-001 12
Schematic Diagram

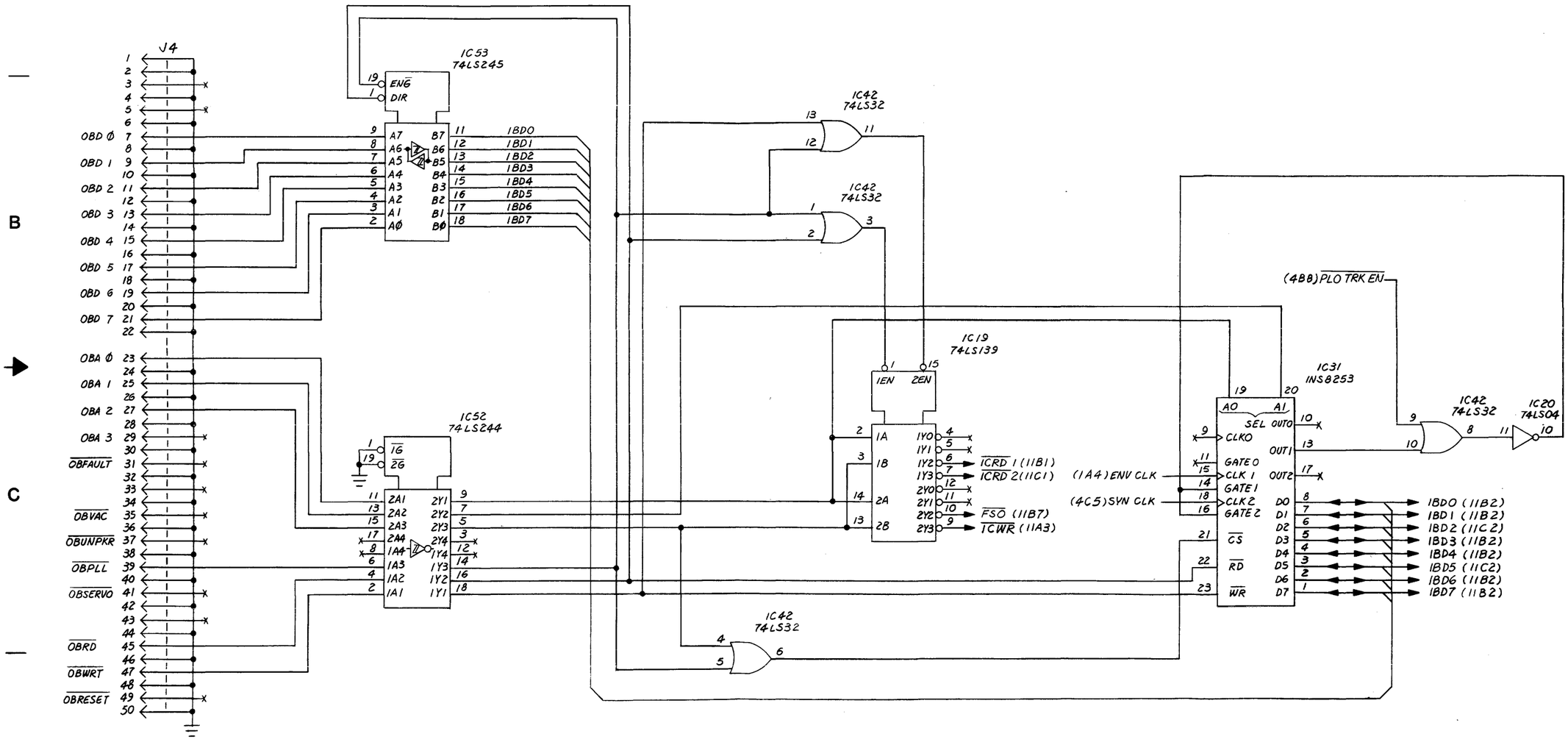


Read Decoder II
Type 6577-001 12
Schematic Diagram

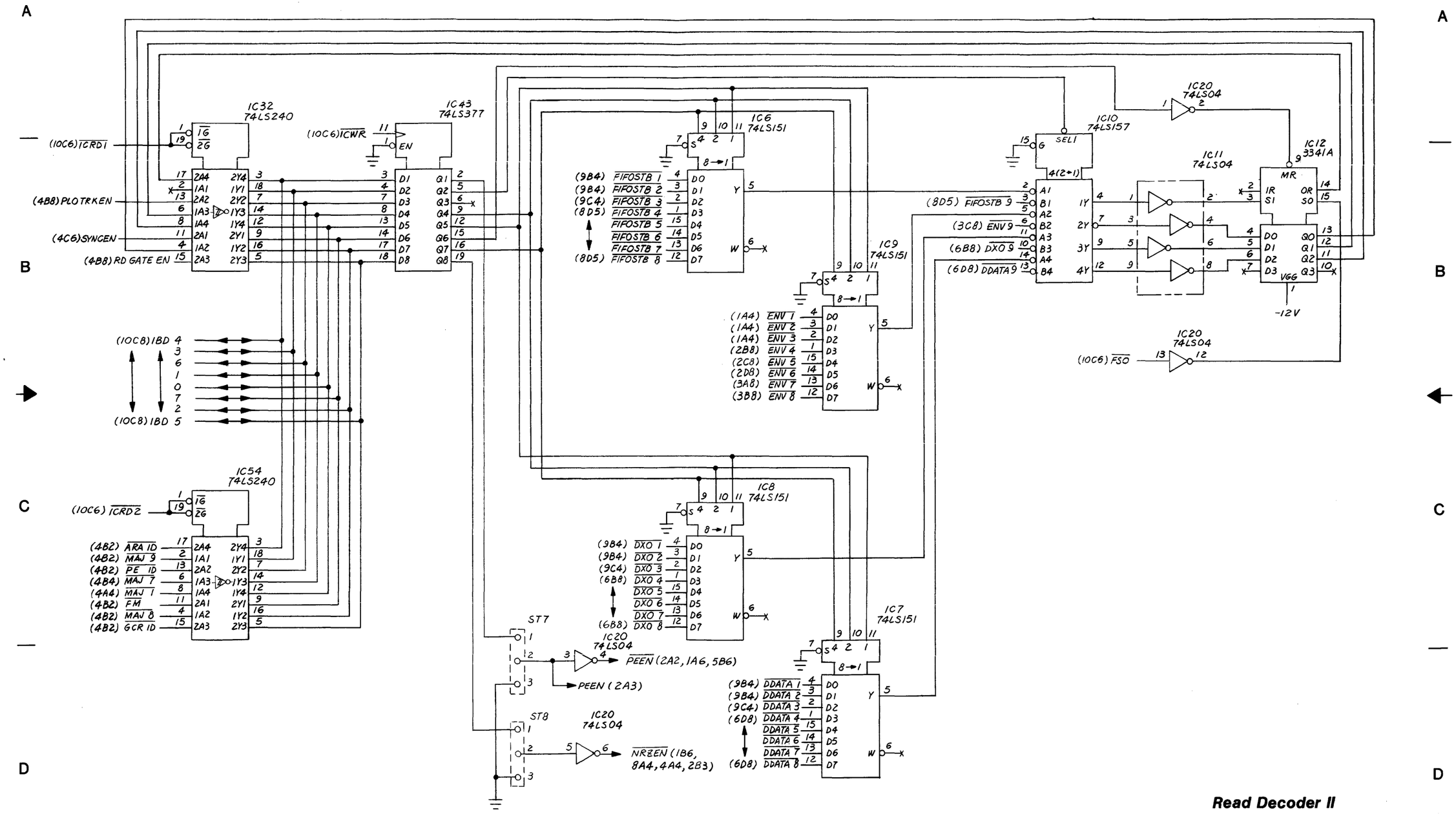




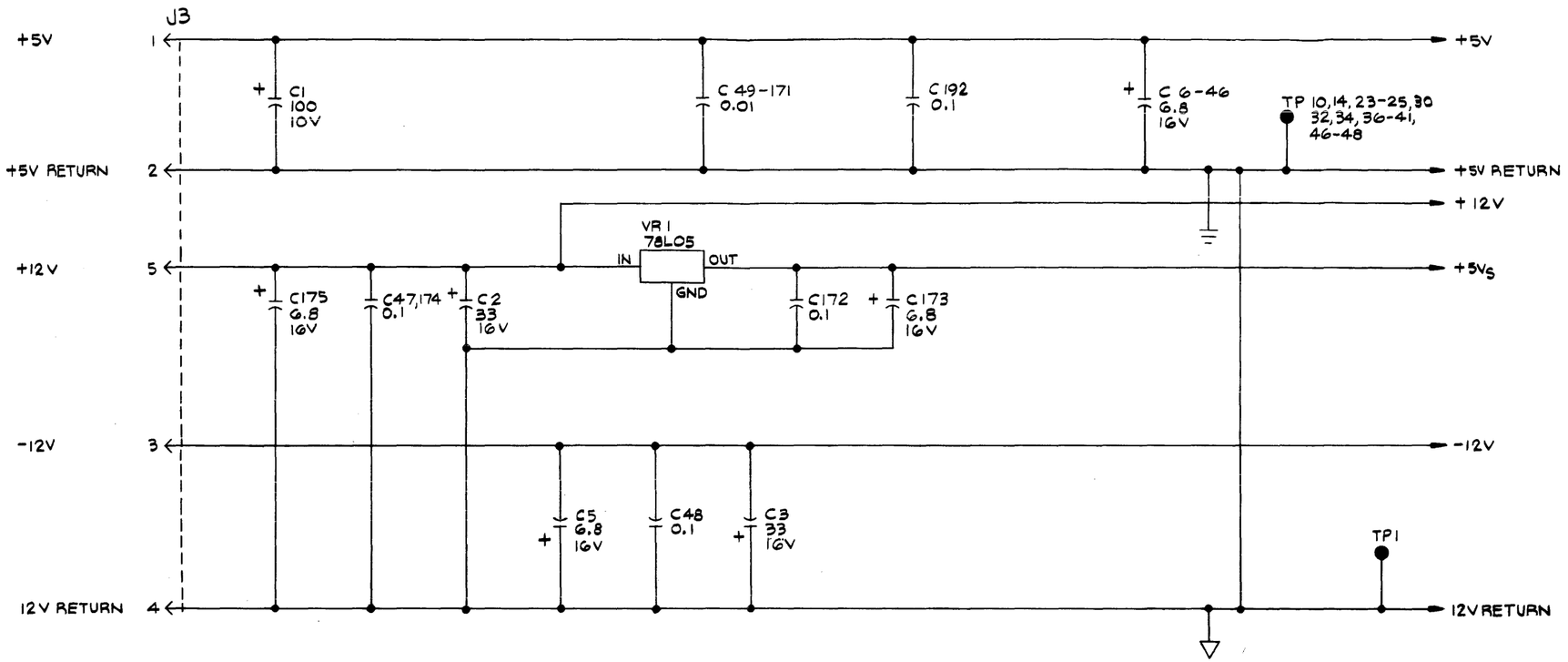
Read Decoder II
Type 6577-001 12
Schematic Diagram



Read Decoder II
Type 6577-001 12
Schematic Diagram



Read Decoder II
Type 6577-001 12
Schematic Diagram



REFERENCE DES.	
LAST USED	NOT USED
C 192	C 4, 184, 191
CR 1	
IC 18A	IC 9
R 29	R 1
ST 14	
TP 48	
VR 1	
Y2	

7 LOCATION IS PROVIDED ON THE BOARD FOR UNUSED IC'S. POWER PINS ARE CONNECTED AS SHOWN IN CHART.

7 DESIGNATORS IC1A-IC18A ARE CONTINUATION IC 1-99

6 TWO LOCATIONS HAVE BEEN PROVIDED ON THE BOARD FOR J10, U35, ST4-12 TO BE USED FOR DIFFERENT UNITS. (IDENTICAL EXCEPT LOCATION)

5 NOTES FOR TYP CIRCUITS ARE SHOWN ON SHEET 5

4 ALL PULL UP RESISTOR VALUES ARE 1K

3. ALL CAPACITOR VALUES ARE IN MICROFARADS
2. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.
1. X INDICATES NO CONNECTION

NOTES: UNLESS OTHERWISE SPECIFIED;

REF. DES	TYPE	+5	GND
IC 28,58,75	74LS00	14	7
IC 45,55,57 96, 5A	74LS04	14	7
IC 11,13,59,65 81,86	74LS08	14	7
IC 76	74LS11	14	7
IC 64	74LS14	14	7
IC 12,54,66 72,93	74LS32	14	7
IC 10,14,21-24,29,32 70,80,82-84,85,90 92	74LS74A	14	7
IC 46	74S132	14	7
IC 2A	74LS139	16	8
IC 44,53 7A-10A	74LS151	16	8
IC 6A	74LS157	16	8
IC 77,79,87, 89,97,99	74LS158	16	8
IC 47,48,68 69,71	74LS161	16	8
IC 36,37,38	74S161	16	8
IC 41,51,62 78,88,98	74LS174	16	8
IC 40,50,61	74S174	16	8
IC 30,73,83	74LS191	16	8
IC 20	74LS193	16	8

REF. DES.	TYPE	+5	GND
IC 35,43,13A	74LS240	20	10
IC 3A, 11A	74LS244	20	10
IC 17A,12A,44 15A, 16A, 18A	74LS245	20	10
IC 95	74LS377	20	10
IC 56, 1A	74S472	20	10
IC 15,25,33	16L8	20	10
IC 16,26,34	16R4	20	10
IC 31	16R6	20	10
IC 4A	3341A	16	8
IC 94	INS8253-5	24	12
IC 39,42,49 52,60,63	74LS86	7	14
IC 5, 6, 7, 17 27, 91	14 PIN LOCATION	14	7
IC 2, 3, 67	16 PIN LOCATION	16	8
IC 1, 4, 74 X01	20 PIN LOCATION	20	10
IC 19	74LS624	9	7

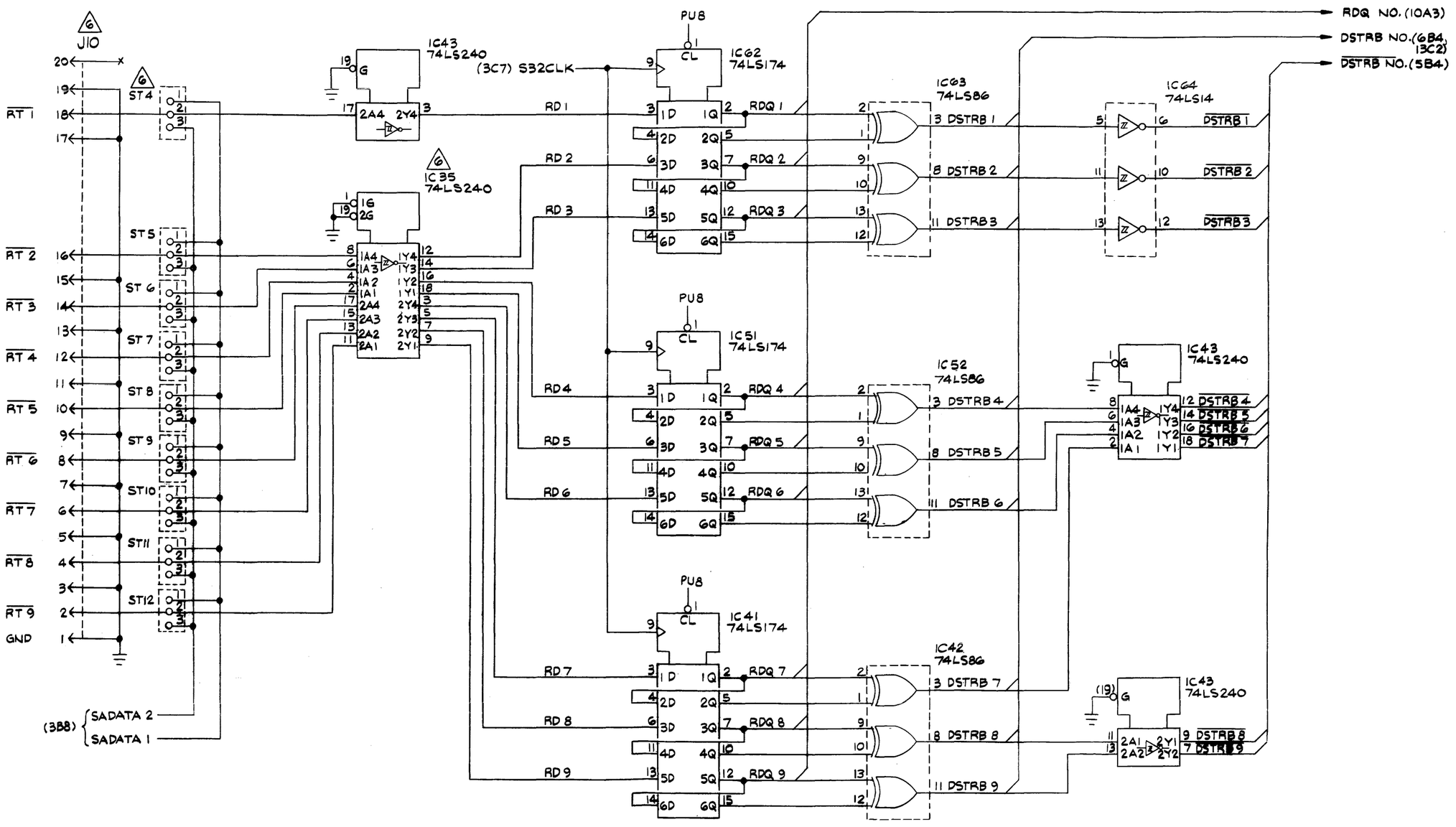
8 8 8

+5V

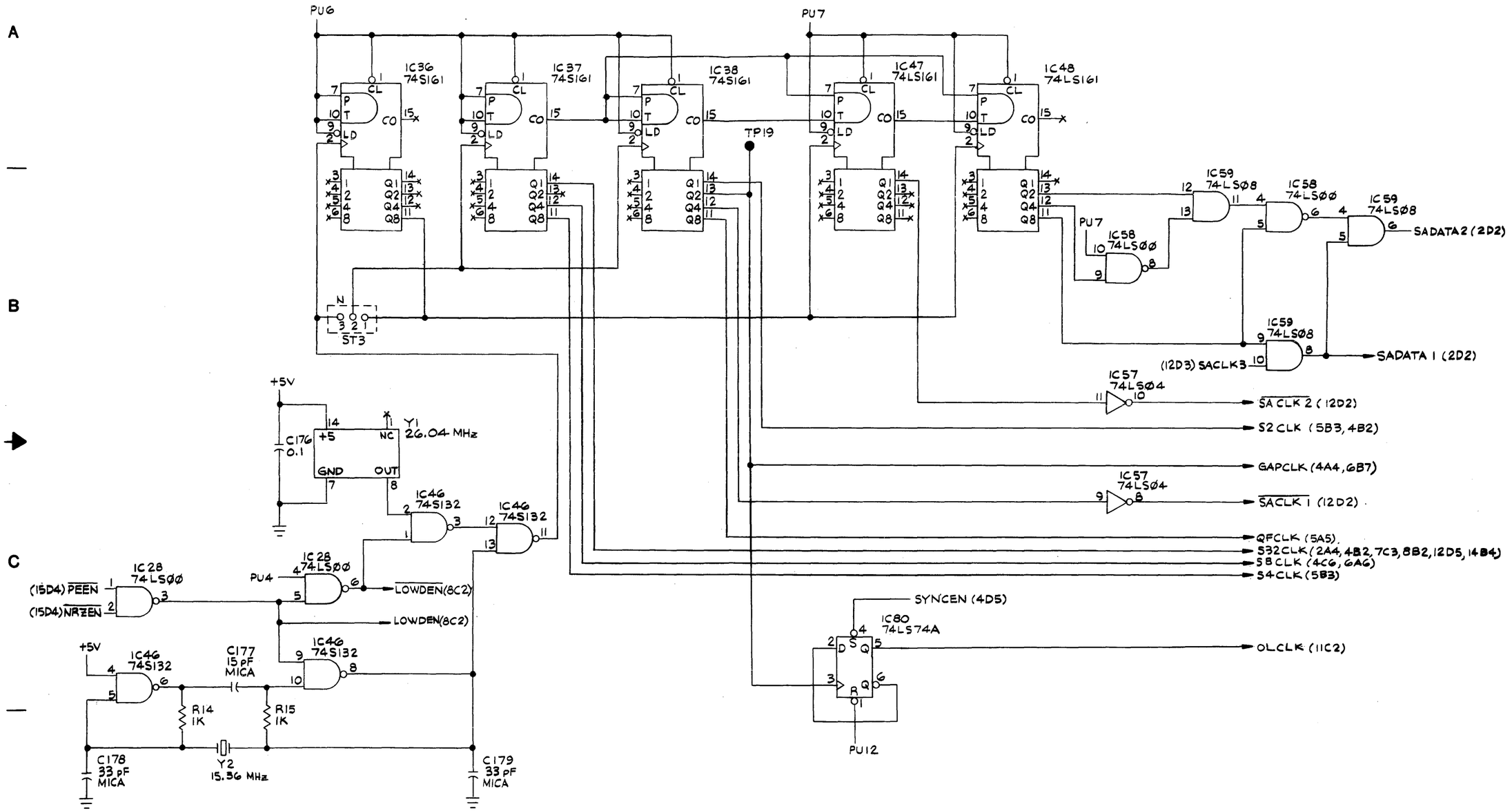
4

R4 PU 4 (3C2, 7C3, 8B3)
R5 PU 5 (4C7, 4D6, 6A7, 7A2, 7B7, 8C4)
R6 PU 6 (3A2, 3B6)
R7 PU 7 (3A5, 3B6)
R8 PU 8 (2A5, 2B5, 2C5, 10A5, 10B5, 10C5)
R9 PU 9 (4B5, 4C5)
R10 PU 10 (4A5)
R11 PU 11 (14B6, 14B4)
R12 PU 12 (4B3, 5A4, 5B4, 11B2, 3D5)
R13 PU 13 (4A3, 4B4)

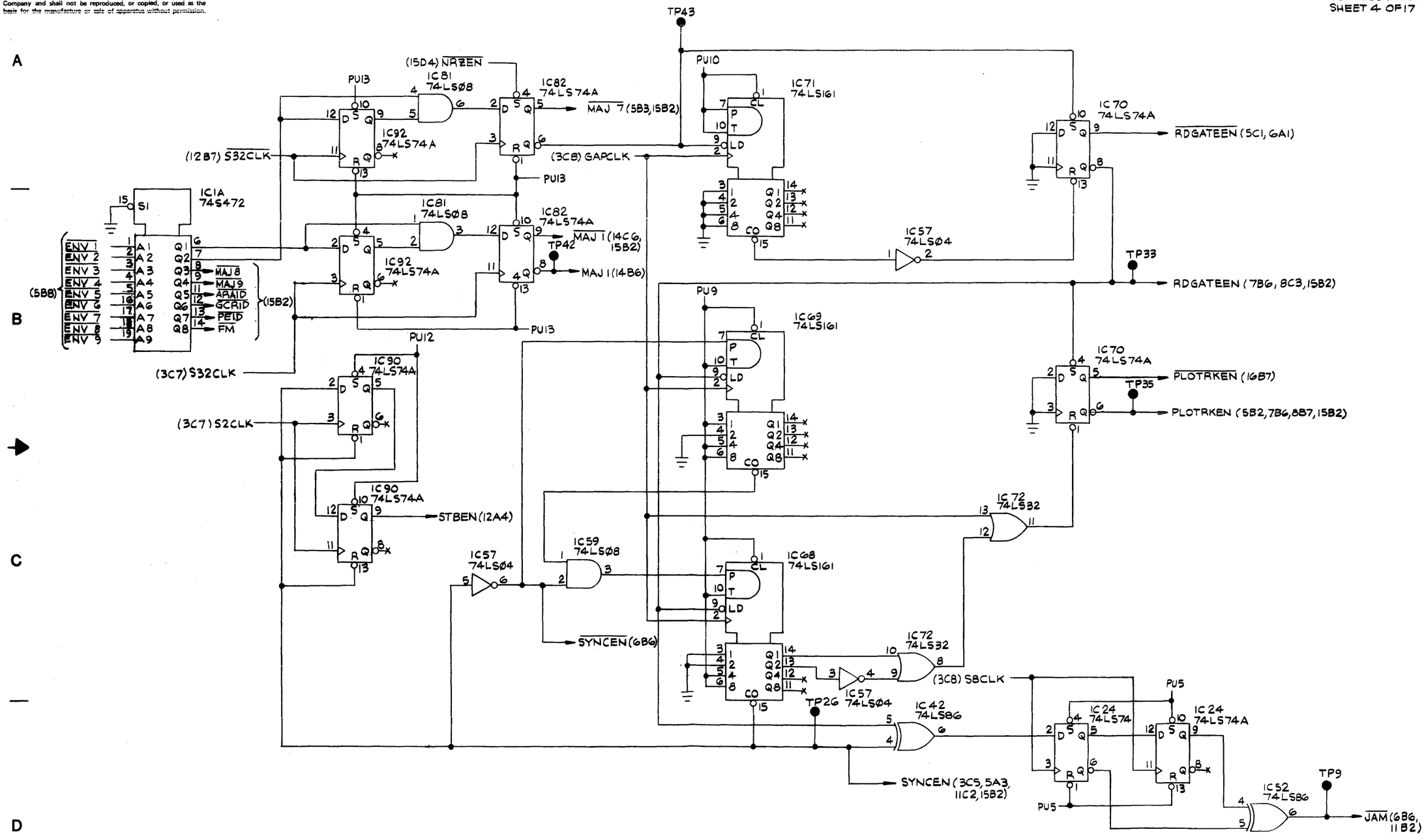
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



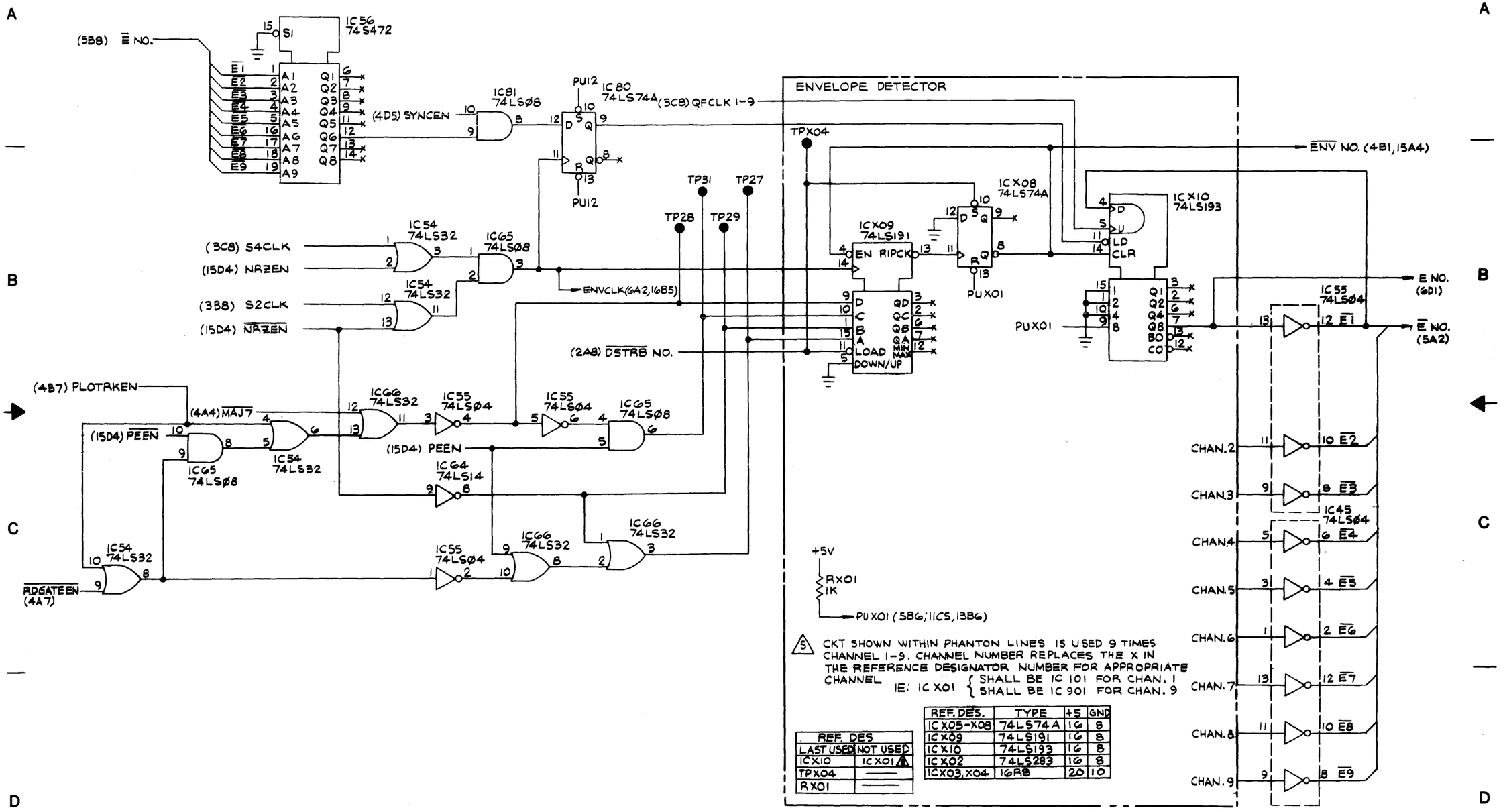
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



Single Loop Decoder
Type 6857-001 A
Schematic Diagram



Single Loop Decoder
Type 6857-001 A
Schematic Diagram

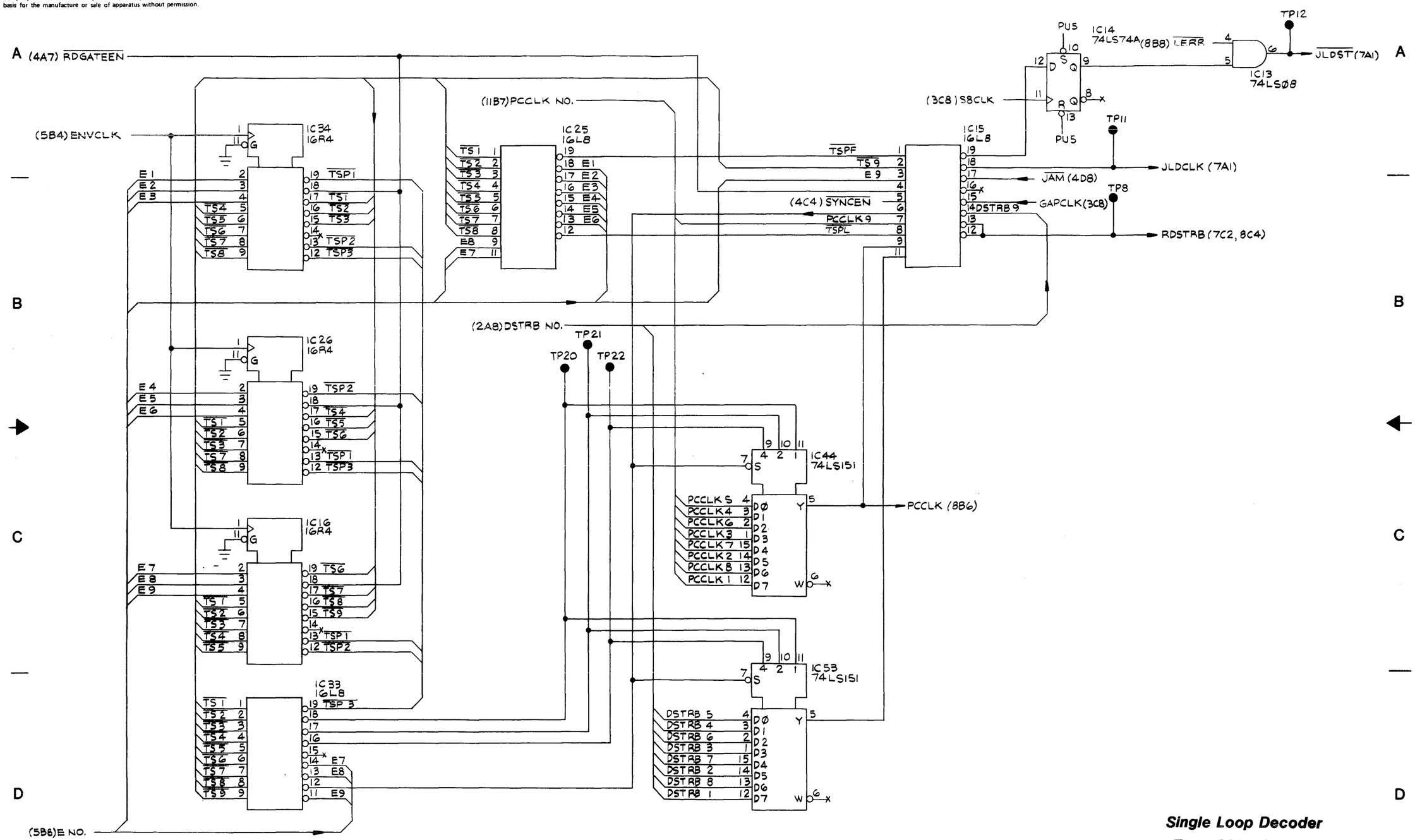


5 CKT SHOWN WITHIN PHANTON LINES IS USED 9 TIMES CHANNEL 1-9. CHANNEL NUMBER REPLACES THE X IN THE REFERENCE DESIGNATOR NUMBER FOR APPROPRIATE CHANNEL
IE: IC X01 { SHALL BE IC 101 FOR CHAN. 1 / SHALL BE IC 901 FOR CHAN. 9

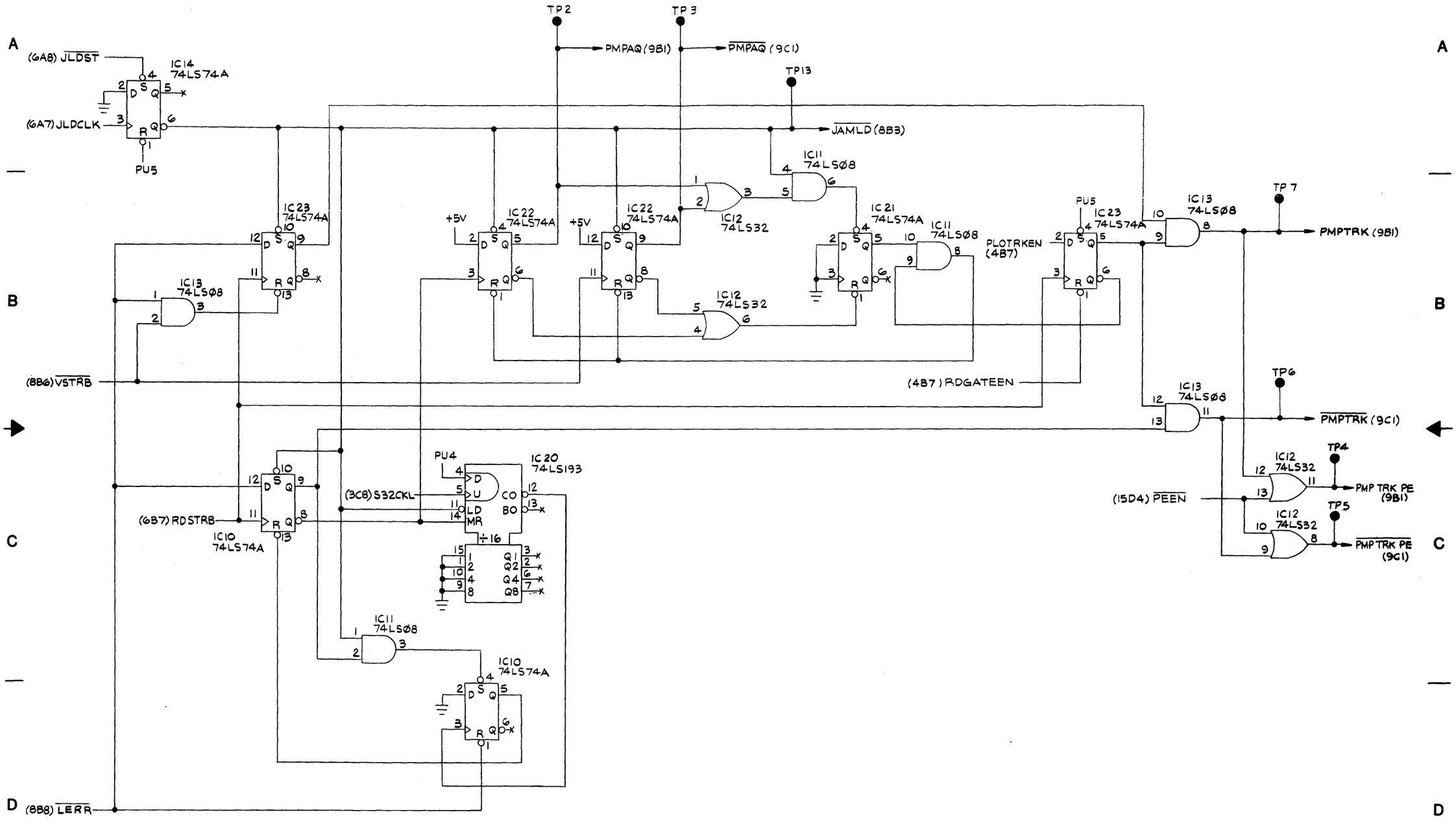
REF. DES	
LAST USED	NOT USED
ICX10	ICX01 ⚠
TPX04	—
RX01	—

REF. DES.	TYPE	+5	GND
ICX05-X08	74LS74A	16	8
ICX09	74LS191	16	8
ICX10	74LS193	16	8
ICX02	74LS283	16	8
ICX03, X04	16R8	20	10

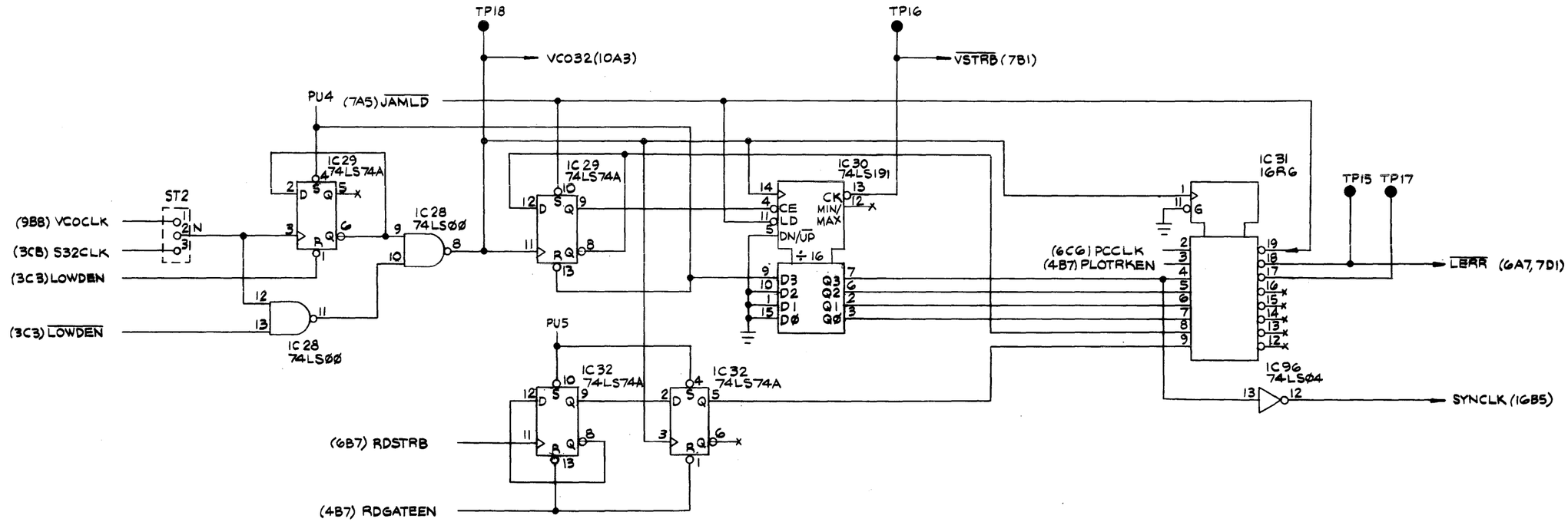
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



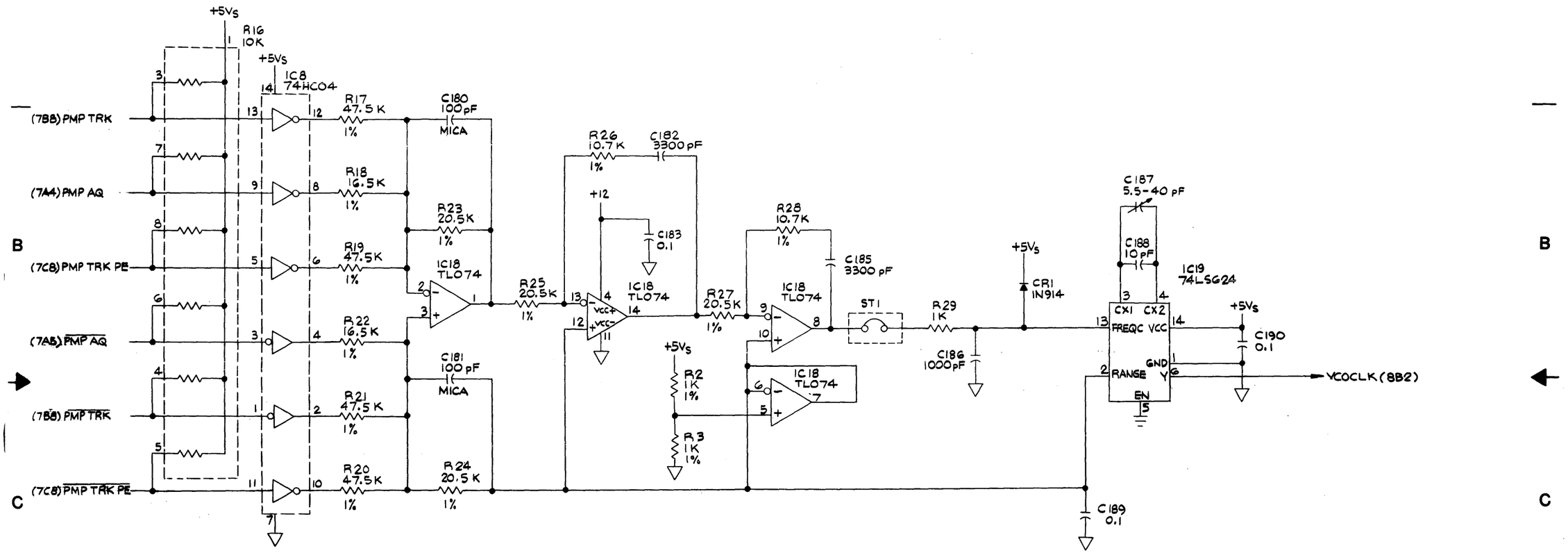
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



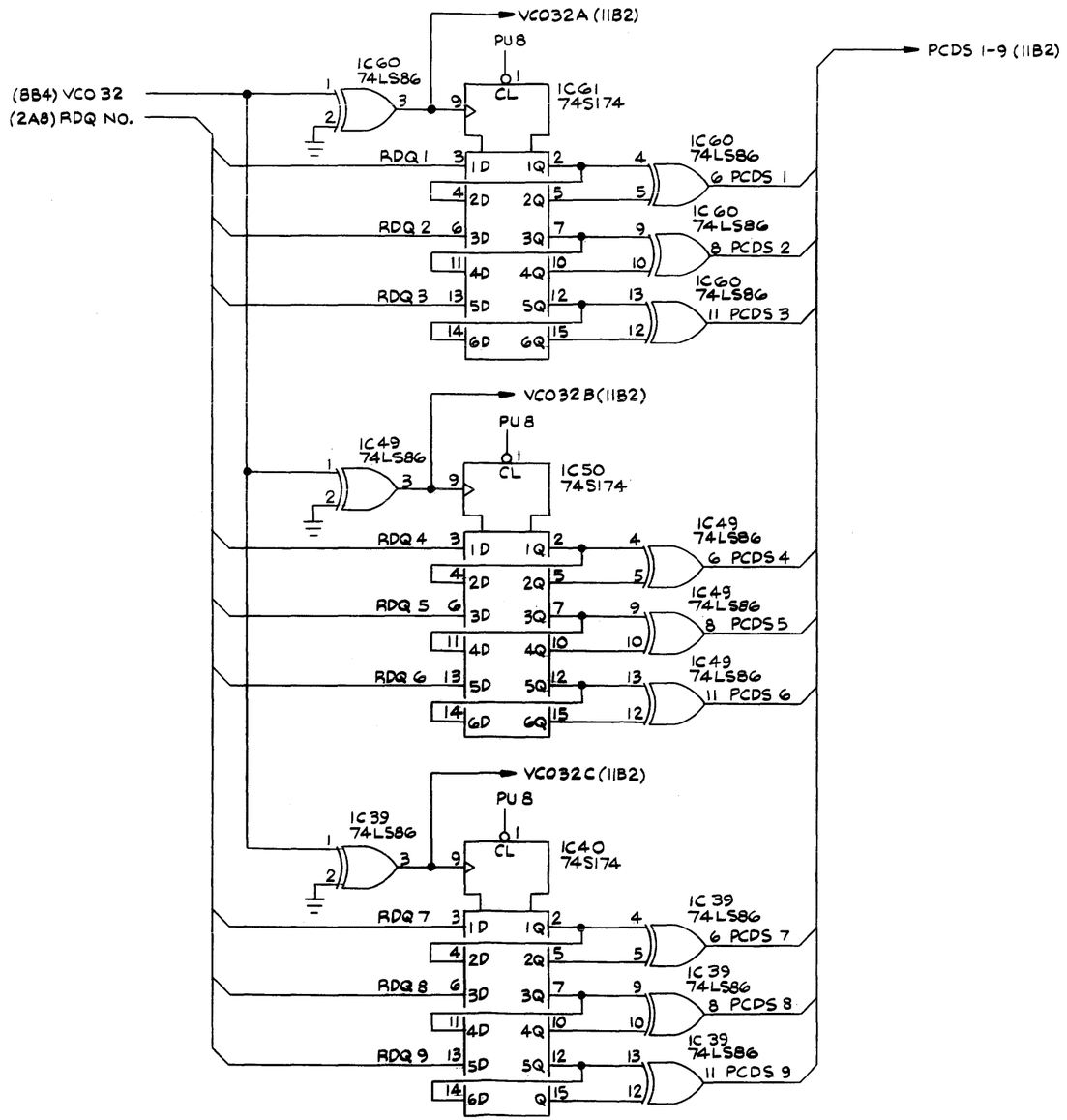
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



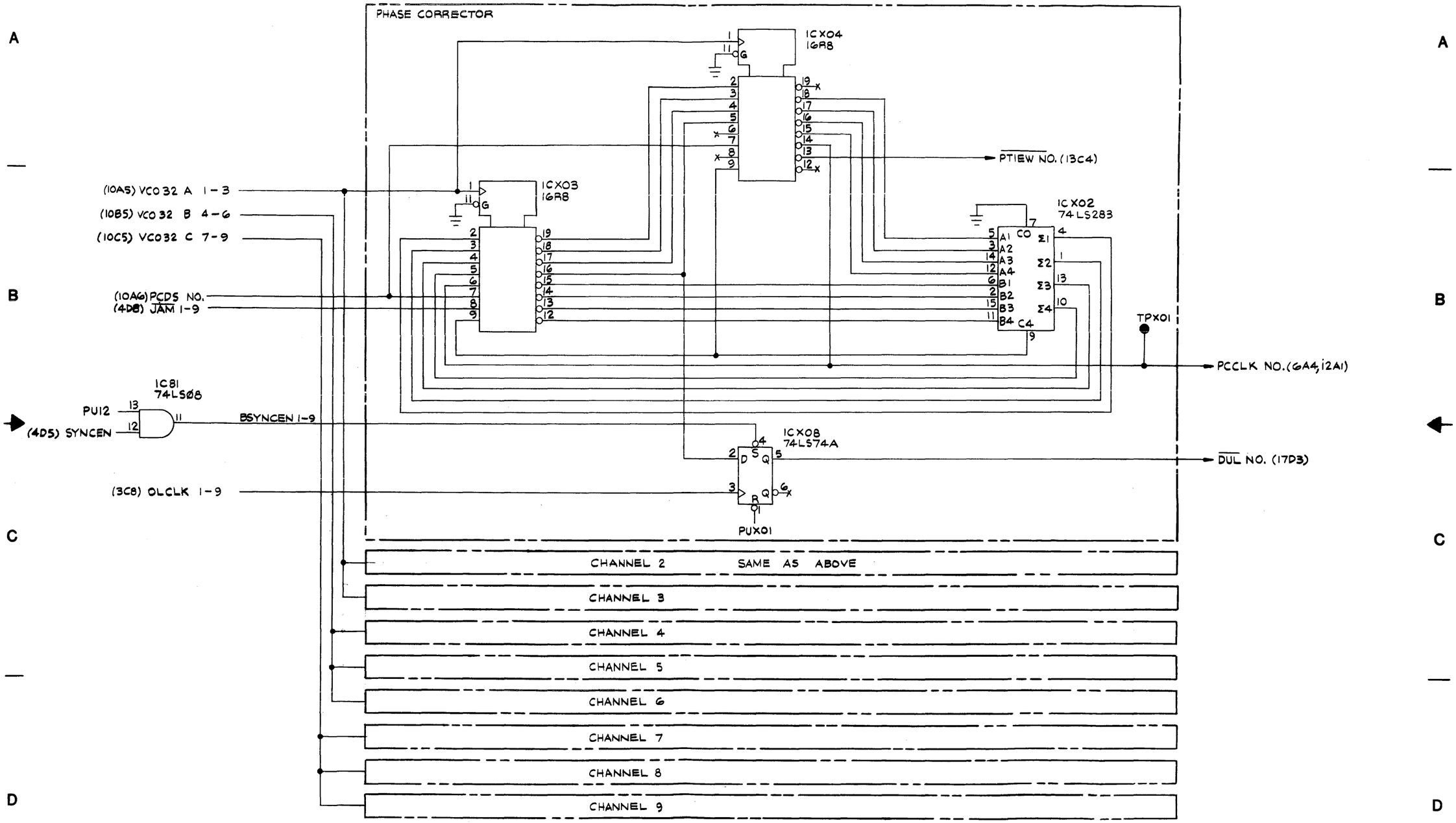
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



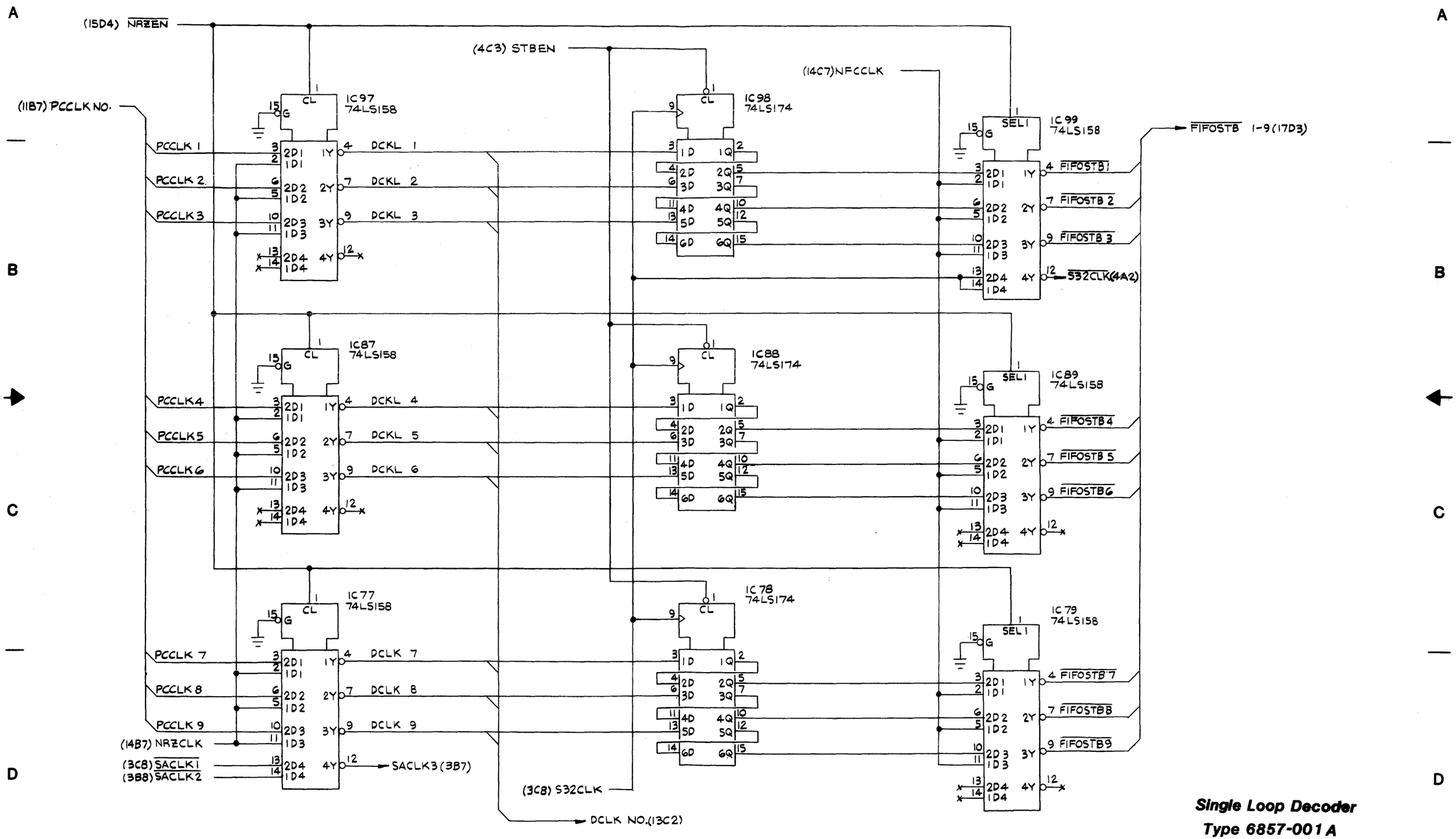
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



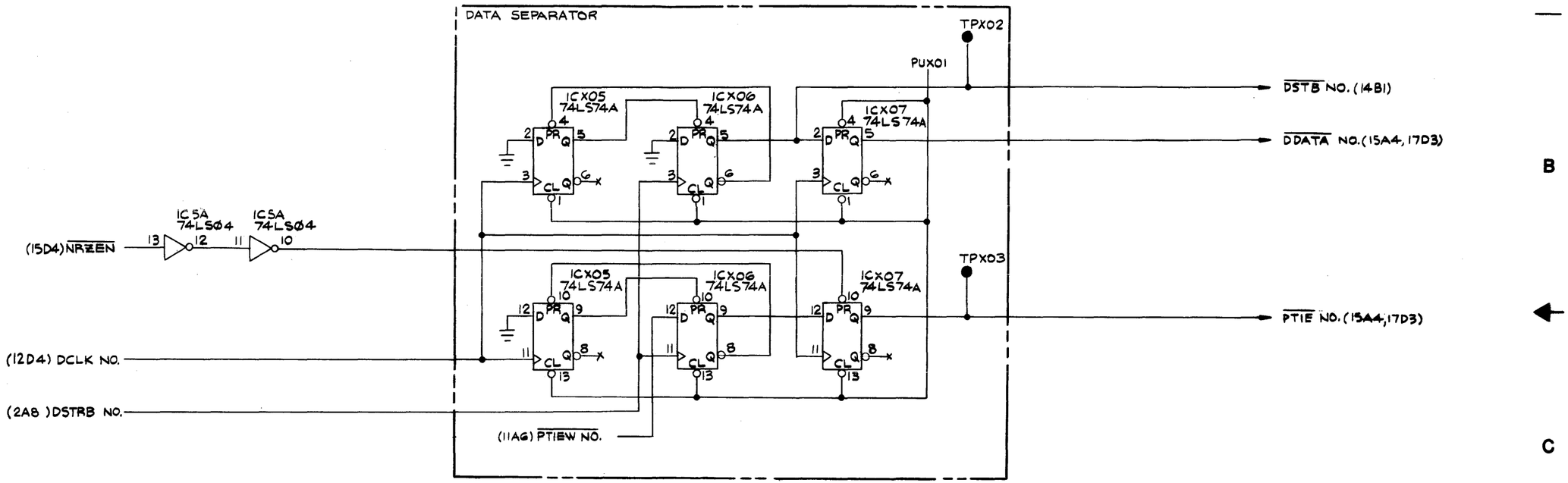
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



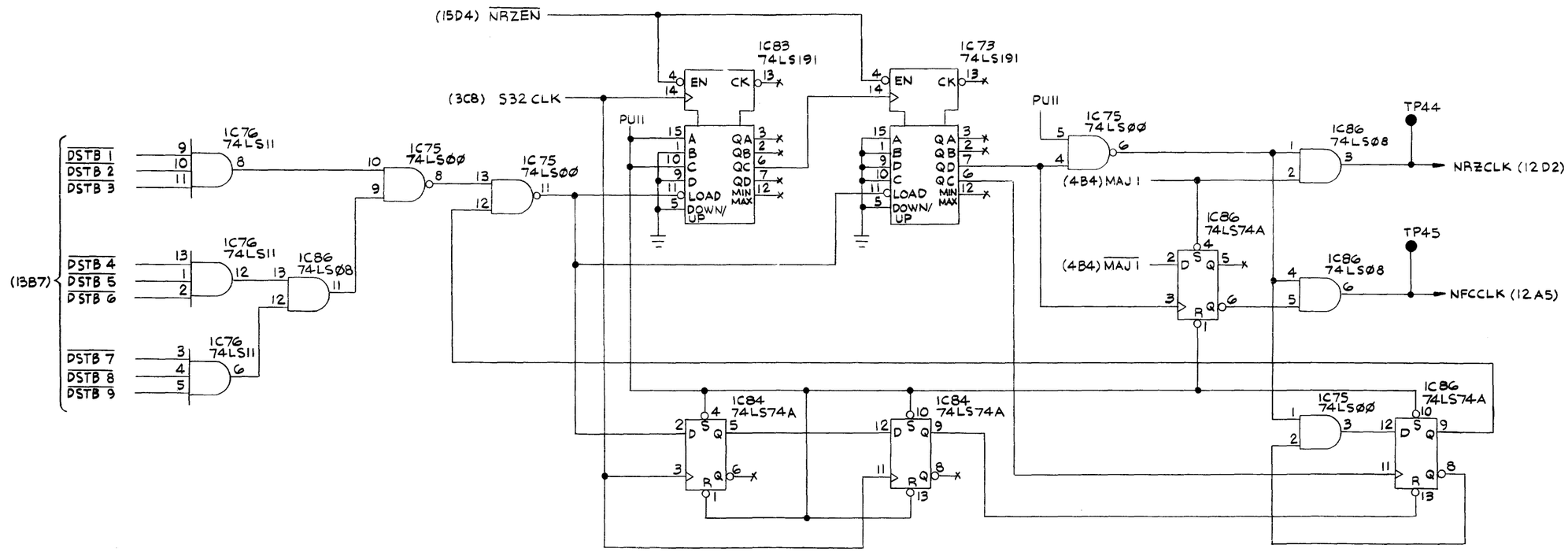
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



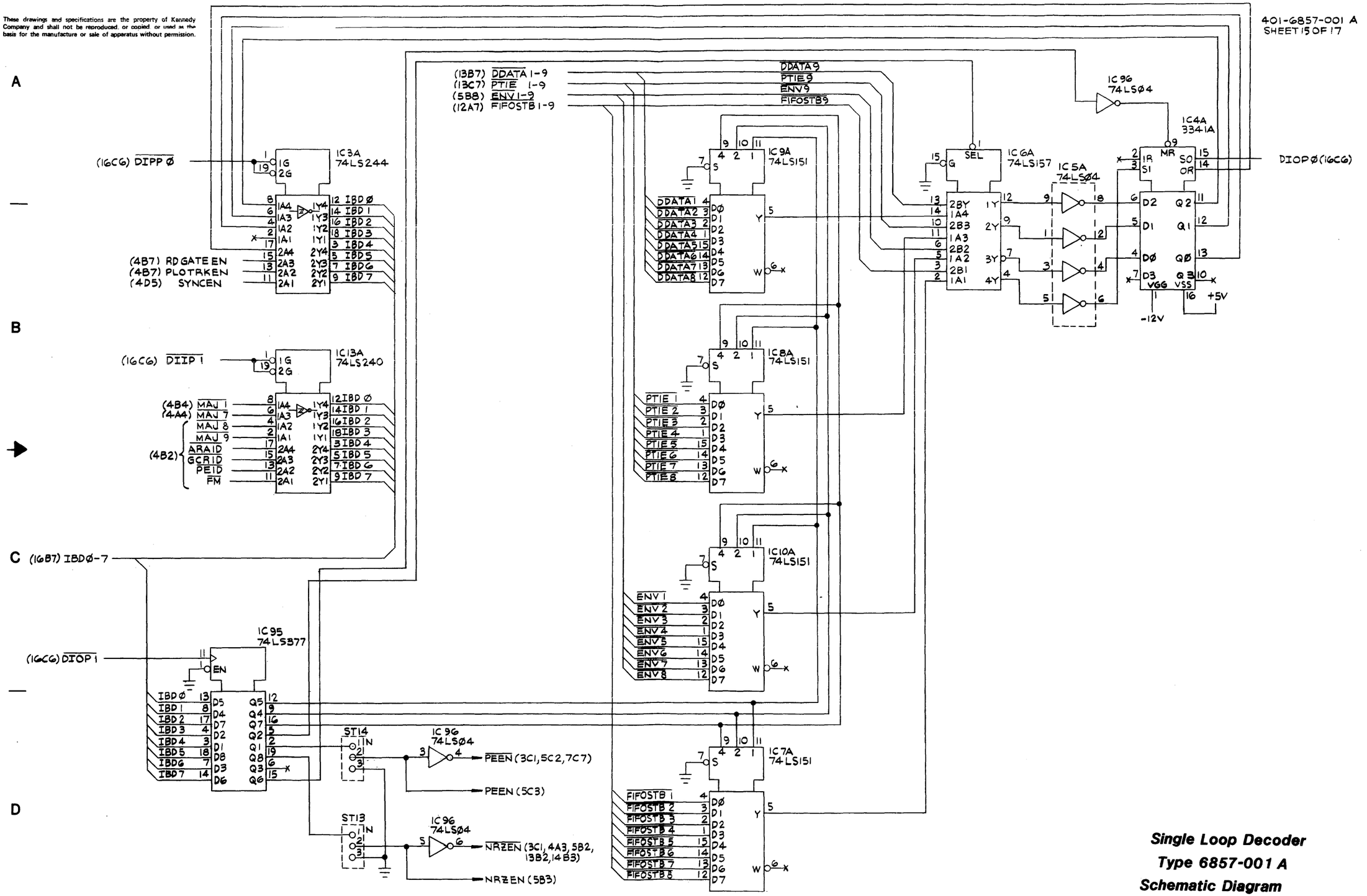
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



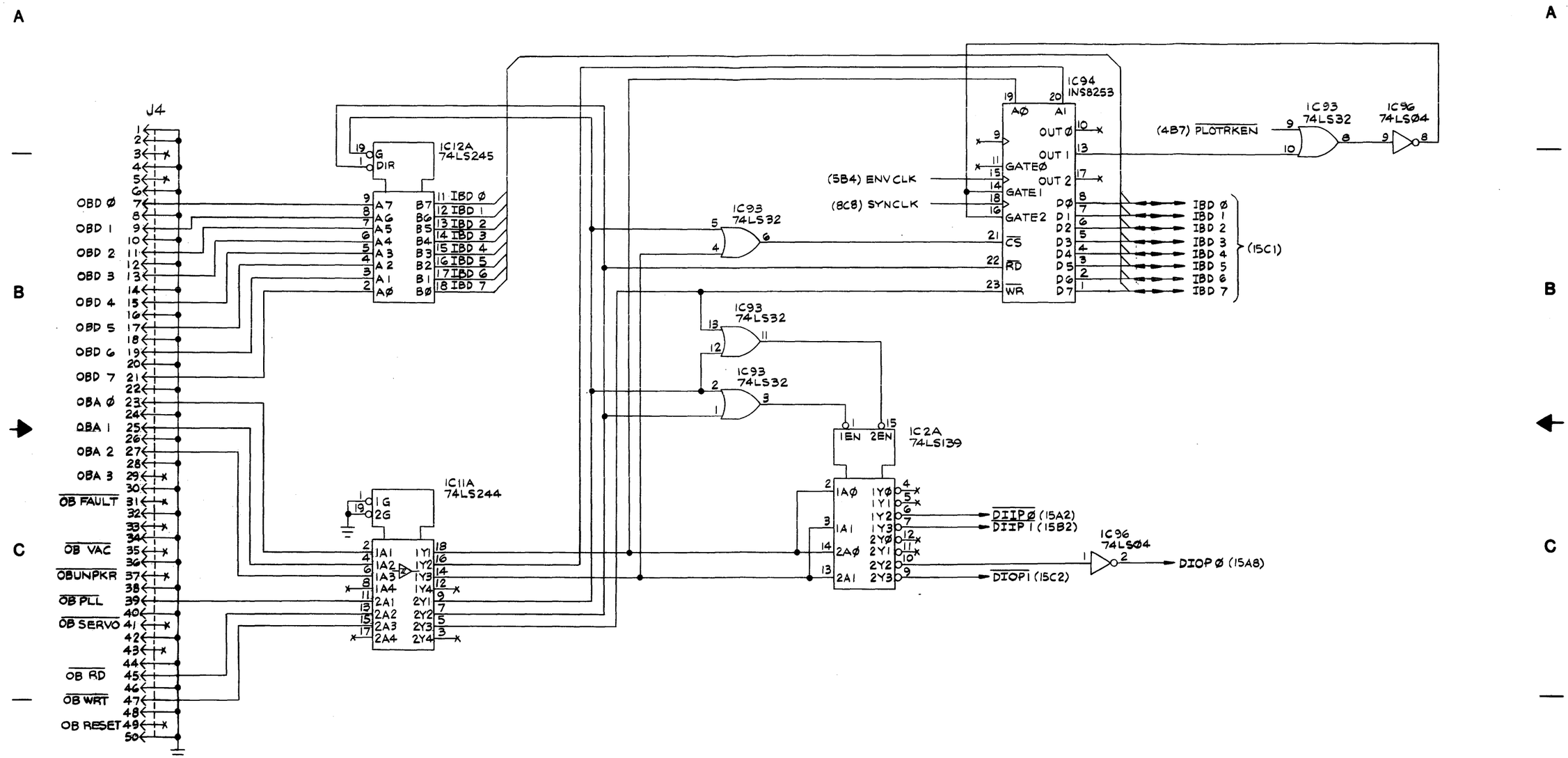
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



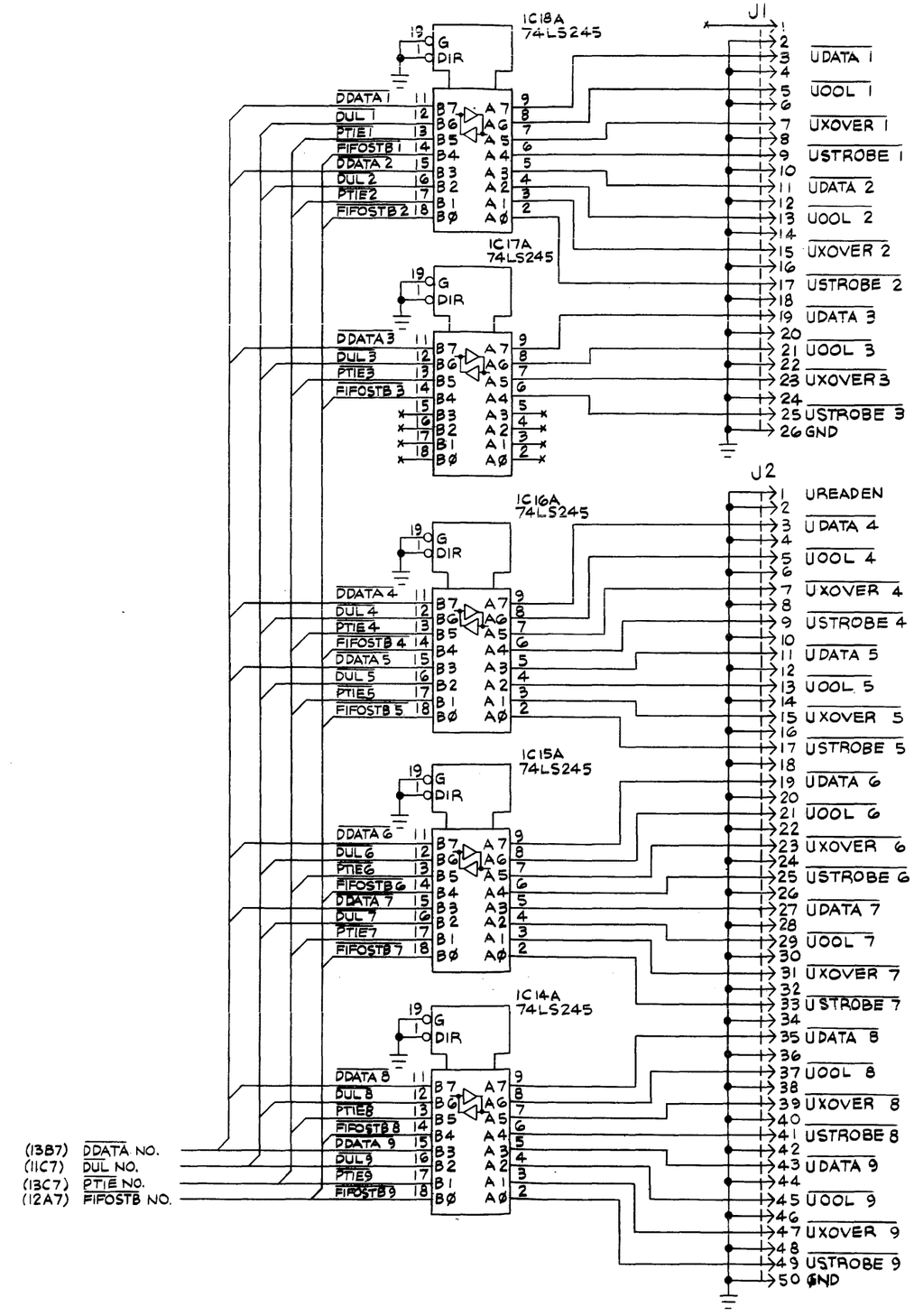
Single Loop Decoder
Type 6857-001 A
Schematic Diagram



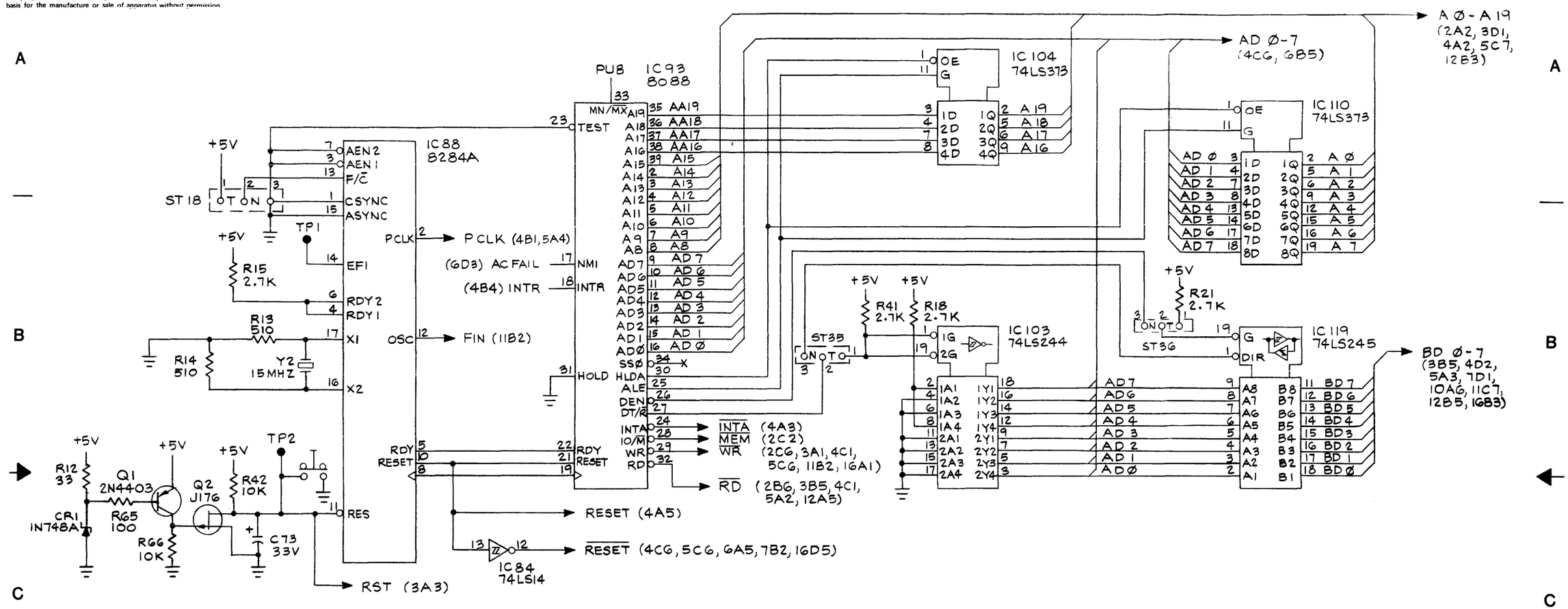
Single Loop Decoder
Type 6857-001 A
Schematic Diagram

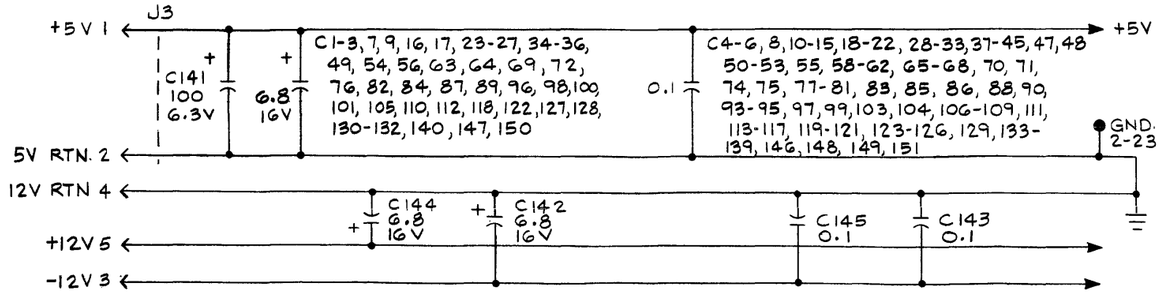


Single Loop Decoder
Type 6857-001 A
Schematic Diagram



Single Loop Decoder
Type 6857-001 A
Schematic Diagram





1. COMPONENT REFERENCE BLOCK, FOR LAST USED AND NOT USED, SHOWN ON SHEET 2.
6. MINIMUM FIFO MEMORY REQUIRED IS 4K. TO ATTAIN DESIRED MEMORY SIZE, CONSULT TABLE ON SHEET 8.
5. COMPONENTS SHOWN FOR FULL CAPABILITY OF THE BOARD.
4. ALL PULL UPS, SHOWN ON SHEET 2 ARE 2.7K.
3. X INDICATES NO CONNECTION.
2. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4W.
1. ALL CAPACITORS ARE IN MICROFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED

REF. DESIG.	TYPE	+5V	GND
IC 47, 83	74LS00	14	7
IC 41, 54, 76	74LS04	14	7
IC 43, 114	74LS08	14	7
IC 40, 87	74LS10	14	7
IC 85	74LS11	14	7
IC 84, 129	74LS14	14	7
IC 70	74LS30	14	7
IC 36, 56, IC 89, 121	74LS32	14	7
IC 22, 30, 35 IC 44, 46, 48 IC 68, 72, 92	74LS74	14	7
IC 128, 157			
IC 126	74LS86	14	7
IC 23, 38, 50, IC 58	74LS125	14	7
IC 67, 69, 98 IC 107, 139	74LS138	16	8
IC 64	74LS139	16	8
IC 55, 63	74LS155	16	8
IC 140	74LS161	16	8
IC 127	74LS175	16	8
IC 57, 133 IC 135, 136 IC 24, 42, 45, IC 51-53, 59, 61 IC 90, 103,	74LS240	20	10
	74LS244	20	10

REF. DESIG.	TYPE	+5V	GND
IC 137, 159	74LS244	20	10
IC 29, 82, 91, IC 97, 119, 120, IC 144-146	74LS245	20	10
IC 33, 62, 125, 134	74LS273	20	10
IC 104 110	74LS373	20	10
IC 31, 71, 78	74LS374	20	10
IC 2-5, 8-11, 111	74S472	20	10
IC 95, 96, 101, IC 102, 108, 109, IC 117, 118, 123 IC 124, 130, 131	74LS569	20	10
IC 65	74LS640	20	10
IC 19	74S00	14	7
IC 26, 32	74S04	14	7
IC 28	74S08	14	7
IC 17, 49	74S86	14	7
IC 27	74S139	16	8
IC 39	74S140	14	7
IC 20	74S153	16	8
IC 37	74S280	14	7
IC 25	74S287	16	8
IC 34	74S288	16	8
IC 6, 12-16	74S374	20	10
IC 86, 94, IC 106, 116	2764	28	14
IC 7, 18	2903	36	13

REF. DESIG.	TYPE	+5V	GND
IC 21	2910	10	30
IC 1	29705	28	14
IC 66, 77, 99, IC 100, 112, 113 IC 115, 122, 138	4016	24	—
IC 143	7406	14	7
IC 93	8088	40	1/20
IC 132	8251A	26	4
IC 74, 80	8254-2	24	12
IC 73, 79	8259-A	28	14
IC 88	8284A	18	9
IC 105	6116E	24	12
IC 75	PAL 10L8	20	10
IC 81, 161	PAL 16L8	20	10
IC 141	1489	14	7
IC 142	1488	—	7

System Processor
Type 6579 21 A
Schematic Diagram

(1A8) A Ø-19

IC 70 74LS30
A 19 1
A 18 2
A 17 3
A 16 4
A 15 5
A 14 6
A 13 11
A 12 12
8 → $\overline{\text{BOOT}}$ (3B6)

PU4
IC 69 74LS138
6 E1
4 E2A
5 E2B
Y Ø 15 → $\overline{\text{WD HAN}}$ (1GA1)
Y 1 14 → $\overline{\text{KEYBRD}}$
Y 2 13 → $\overline{\text{AMPS}}$ } (5C5)
Y 3 12
Y 4 11 X
Y 5 10 → $\overline{\text{PLL}}$
Y 6 9 → $\overline{\text{UNPCKR}}$
Y 7 7 → $\overline{\text{SERVO}}$ } (5A2)
A5 1 AØ
A6 2 A1
A7 3 A2

IC 64 74LS139
1 EN
A2 2 A
A3 3 B
Y Ø 4
Y 1 5
Y 2 6 X
Y 3 7 X

IC 76 74LS04
(1C4) $\overline{\text{RD}}$ 5 → 6

IC 63 74LS155
AØ 13
A1 3
A B SEL
1 1C
2 1G
14 2G
15 2C
1Y Ø 7 → $\overline{\text{LSB READ}}$ (10A6)
1Y 1 6 → $\overline{\text{MSB READ}}$ (11C6)
1Y 2 5 X
1Y 3 4 X
2Y Ø 9 → $\overline{\text{LOAD 1}}$ (10A6, 11B2)
2Y 1 10 → $\overline{\text{LOAD 2}}$ (10C6, 11B2)
2Y 2 11 X
2Y 3 12 X
(6B6) $\overline{\text{FF RESET}}$

IC 81 PAL 16L8
A 17 1
A 16 2
A 3 3
A 4 4
A 11 5
A 12 6
A 13 7
A 14 8
A 15 9
(1B5) $\overline{\text{MEM}}$ 11
19 $\overline{\text{FXXY}}$
18 → $\overline{\text{MEMENB}}$ (3B5)
17 → $\overline{\text{RAM Ø}}$ (3B2)
16 → $\overline{\text{RAM 1}}$ (3A3)
15 ROM Ø
14 ↕ 1
13 ↕ 2
12 $\overline{\text{ROM 3}}$
$\overline{\text{ROM Ø-3}}$ (3C2)

IC 75 PAL 10L8
A 3 1
A 4 2
A 5 3
A 6 4
A 7 5
A 8 6
A 9 7
A 10 8
11
19 → $\overline{\text{INT Ø}}$ (4B3)
18 → $\overline{\text{INT 1}}$ (4C3)
17 → $\overline{\text{TIMER Ø}}$ (4A2)
16 → $\overline{\text{TIMER 1}}$ (4C1)
15 → $\overline{\text{SIO}}$ (4A5)
14 X
13 → $\overline{\text{DEAD MAN}}$ (5B6)
12

IC 55 74LS155
AØ 13
A1 3
A B SEL
1 1C
2 1G
14 2G
15 2C
1Y Ø 7 → $\overline{\text{SENSORS}}$ (5B4)
1Y 1 6 → $\overline{\text{CBLCHK}}$ (5C2)
1Y 2 5 → $\overline{\text{DIAG. SW}}$ (4C5)
1Y 3 4 → $\overline{\text{RD FIFO}}$ (7C7)
2Y Ø 9 → $\overline{\text{PWR. REG}}$ (6A4)
2Y 1 10 → FIFO MODE (7B2)
2Y 2 11 → $\overline{\text{STAT LED}}$ (4C7)
2Y 3 12 → WR FIFO (7A7)
(1B4) $\overline{\text{WR}}$

P2
$\overline{\text{MEM}}$ 32
$\overline{\text{WR}}$ 33

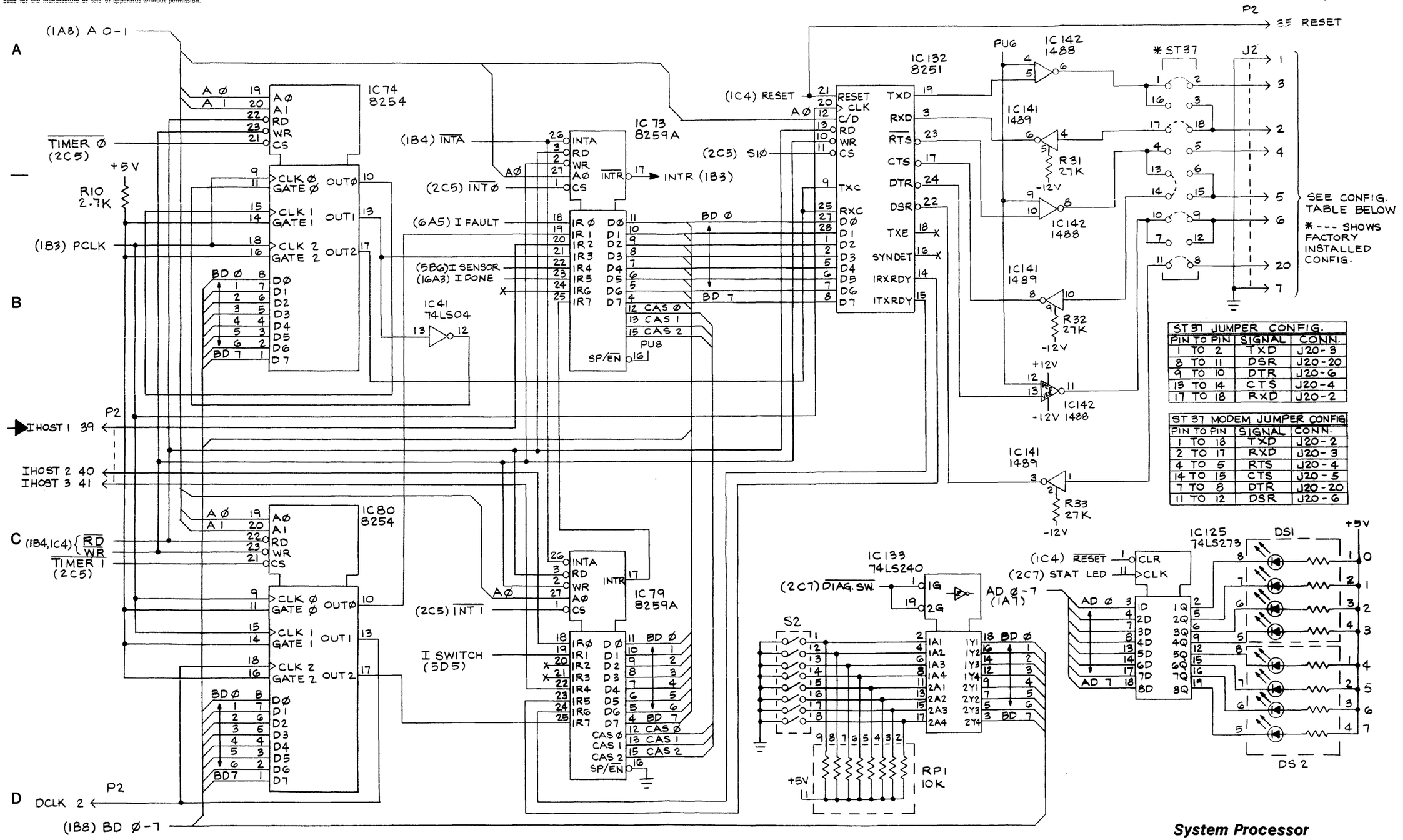
+5V
R16 → PU 8 (1A4, 4B4)
R35 → PU 7 (9C3, 16A5, 16D6)
R34 → PU 6 (4A6, 9B3, 9B4, 9B6, 9D3, 9C4, 9D6, 11A3, 11C4)
R22 → PU 5 (5A4, 5A6)
R8 → PU 4 (2A2, 19A6, 19B7)
R7 → PU 3 (19B3, 19B4, 19C3)
4 R5 → PU 2 (16B2, 16C2, 17B7, 18A3, 18B3, 18C3)
R4 → PU 1 (15B5, 15C6)

REF. DESIGNATORS LAST USED	REF. DESIGNATORS NOT USED	SPARE LCTN ON BOARD
BT 1	—	—
C162	C46, 57, C157, 158	—
CR 3	—	—
DS 2	—	—
IC 161	—	IC148-156, IC158
Q3	—	—
R72	R29, 30, 68-71	—
RP 2	—	—
S2	—	—
ST 39	ST 23-26, ST 31-34	—
VR 1	—	—
Y2	—	—
TP 3	—	—

System Processor
Type 6579 21 A
Schematic Diagram

ST39 R72 270 CR2 1N914 CR3 1N914 VR1 LM317 +12V
BT1 Q3 2N4401 IC160 (MODIFIED LOCATION) RG7 100K R17 100K C102 0.1 R20 240 R19 820 C92 0.1 C91 0.1
(1C3) RST
(2C3) RAM 1 IC89 74LS32
(1B4) WR (2C3) RAM Ø IC115 4016 IC105 6116E
(2C3) MEMENB (1C4) RD IC120 74S245 BD Ø-7 (1B8)
(2A3) BOOT IC111 74S472 BOOT ROM
SYSTEM RAM
ROM Ø-3 (2C4) ROM Ø IC116 2764 ROM 1 IC106 2764 ROM 2 IC94 2764 ROM 3 IC86 2764 +5V
A Ø-12 (1A8)
SYSTEM ROM

System Processor
Type 6579 21 A
Schematic Diagram



ST 37 JUMPER CONFIG.

PIN TO PIN	SIGNAL	CONN.
1 TO 2	TXD	J20-3
8 TO 11	DSR	J20-20
9 TO 10	DTR	J20-6
13 TO 14	CTS	J20-4
17 TO 18	RXD	J20-2

ST 37 MODEM JUMPER CONFIG.

PIN TO PIN	SIGNAL	CONN.
1 TO 18	TXD	J20-2
2 TO 17	RXD	J20-3
4 TO 5	RTS	J20-4
14 TO 15	CTS	J20-5
7 TO 8	DTR	J20-20
11 TO 12	DSR	J20-6

System Processor
Type 6579 21 A
Schematic Diagram

(1B8) DATA BD Ø-7

(2B3) UNPCKR

(1C4) RD

(2B3) PLL / SERVO

IC144 74LS245

IC85 74LS11

J4

OBD Ø 44 … OBD 7 30

VACRT 1

J21

C152 1.0 5%

IC85 74LS11

IC 97 74LS245

J11

KD Ø 24 … KD 7 10

KINT 8

KVAC 6

(2C7) CBLCHK

+5V

RP2 10K

KCHKA 4

KCHKJ 2

RD CHK 1

PCHK 10

WCHK 20

OBCHKS 46

OBCHK P 48

OBCHK U 50

J5 J13 J9 J4

PU5

IC127 74LS175

(1B3) PCLK

(6B3) LDPRT

EOTRT (6B3)

+5V

RG4 2.7K

SENSORS (2C8)

IC136 74LS240

(9A5) NOT FULL

(9D6) OUT RDY

IC82 74LS245

I SWITCH (4C3)

IC126 74LS86

IC89 74LS32

PU5

IC128 74LS74

I SENSOR (4B3)

(2C5) DEADMAN

IC146 74LS245

J4

15 OBVAC
16 OBSERVO
10 OBPLL
11
14 OBUNPCKR
13

IC145 74LS245

1
2 OBRESET
3
4 OBWR
5
6 OBRD
7
8 OBDEAD
9
22 OBA3
21
24 OBA2
23
26 OBA1
27
28 OBAØ
29

RD

PCLK

(2B3) KEYBRD

(2B3) AMPS

(1C4) RESET

(1B4) WR

(1A8) A Ø-3

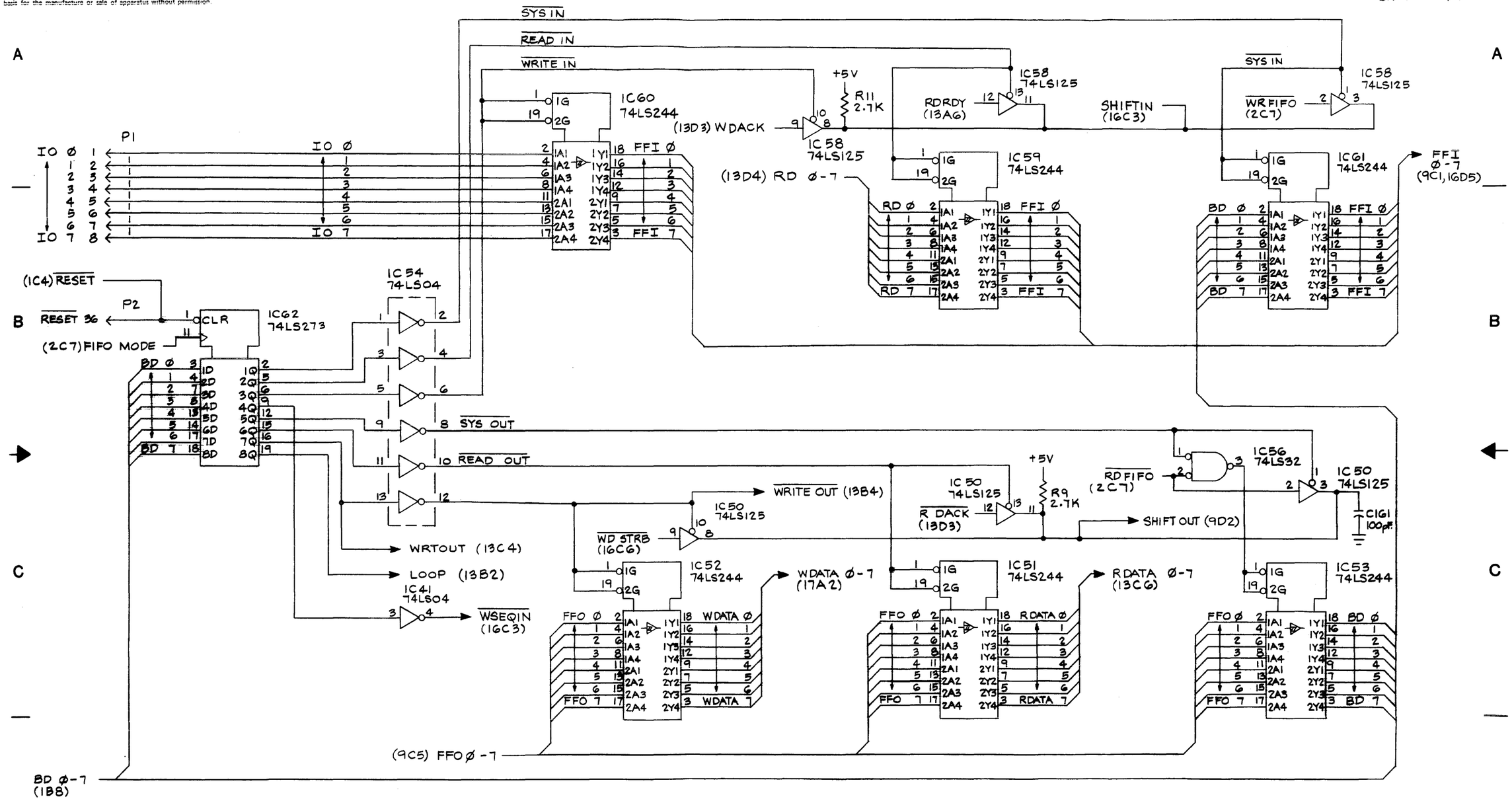
IC91 74LS245

J11

40 KRESET
39
38 KPCLK
37
36 KRD
35
34 KWR
33
32 KKEYBRD
31
30 KAMPS
29
28 KAØ
27
26 KA1
25

System Processor
Type 6579 21 A
Schematic Diagram

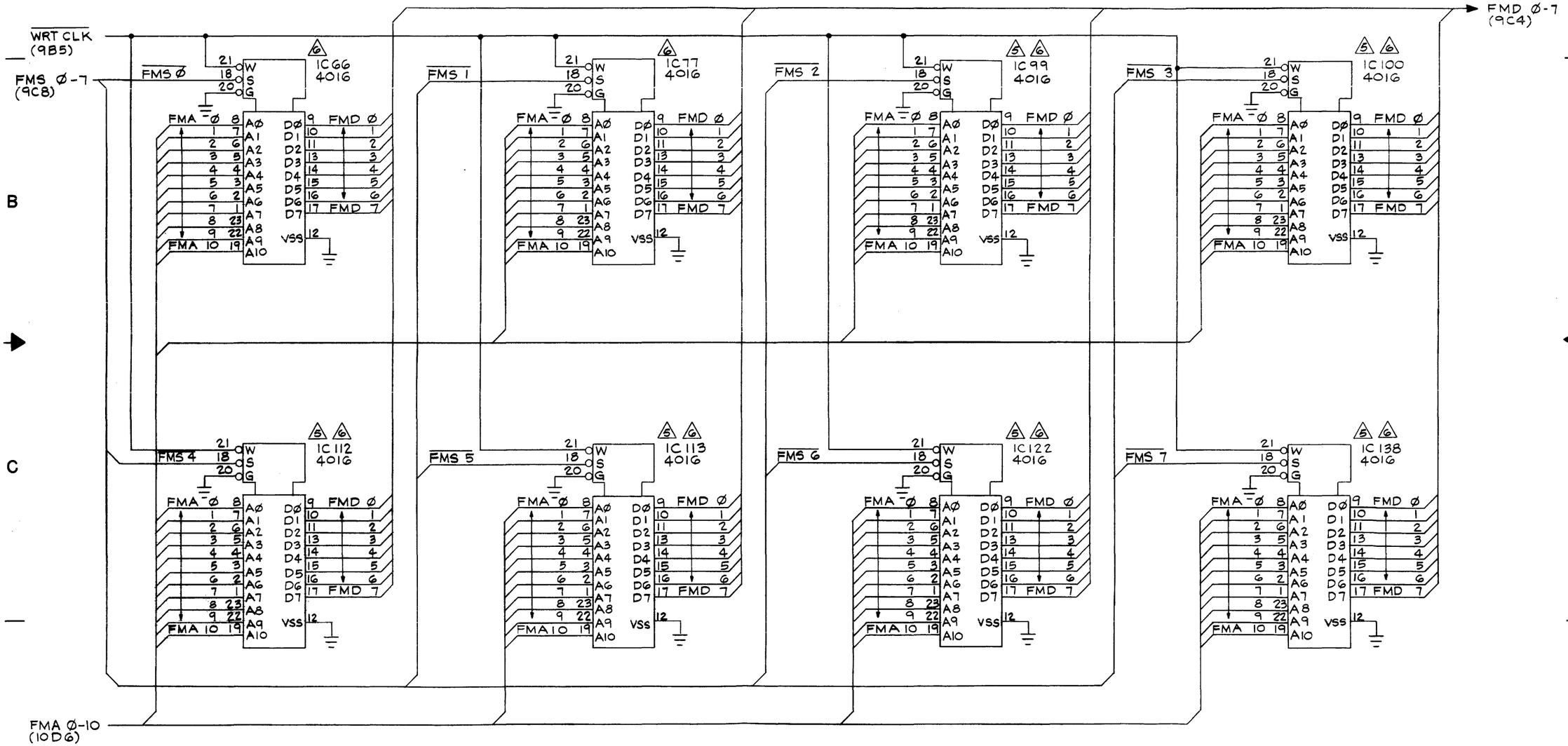
System Processor
Type 6579 21 A
Schematic Diagram



System Processor
Type 6579 21 A
Schematic Diagram

⑥ FIFO MEMORY CONFIGURATION

4K	8K	12K	16K
ST19	ST20	ST21	ST22
ST27	ST28	ST29	ST30
IC66	IC66	IC66	IC66
IC77	IC77	IC77	IC77
	IC99	IC99	IC99
	IC100	IC100	IC100
		IC112	IC112
		IC113	IC113
			IC122
			IC138



System Processor
Type 6579 21 A
Schematic Diagram

C1G2 100pF

IC87 74LS10

IC89 74LS32

$\overline{\text{NOT FULL}}$ (5C4)

$\overline{\text{INRDY}}$ (13C2)

P1 10 $\overline{\text{INRDY}}$

(11A8) $\overline{\text{FULL}}$

(11A5) $\overline{\text{P2}}$

IC84 74LS14

IC83 74LS00

IC43 74LS08

IC72 74LS74

PUG

IC72 74LS74

IC157 74LS74

(11B6) $\overline{\text{P3}}$

IC43 74LS08

$\overline{\text{WRT CLK}}$ (8A1, 10A2, 11B2)

SHIFTIN (1GC3)

IC78 74LS374

IC71 74LS374

FFI Ø-7 (7A8)

FMD Ø-7 (8A8)

FFO Ø-7 (7D3)

(10D6) FMA 11-15

IC67 74LS138

$\overline{\text{FMS}}$ Ø-7 (8B1)

PU7

IC92 74LS574

PUG

IC85 74LS11

(11B5) $\overline{\text{P5}}$ $\overline{\text{P7}}$

$\overline{\text{LSHIFT}}$ (11B4)

$\overline{\text{READCLK}}$ (11B6)

IC68 74LS574

IC68 74LS574

OUTRDY (16C5)

P1 14 OUTRDY

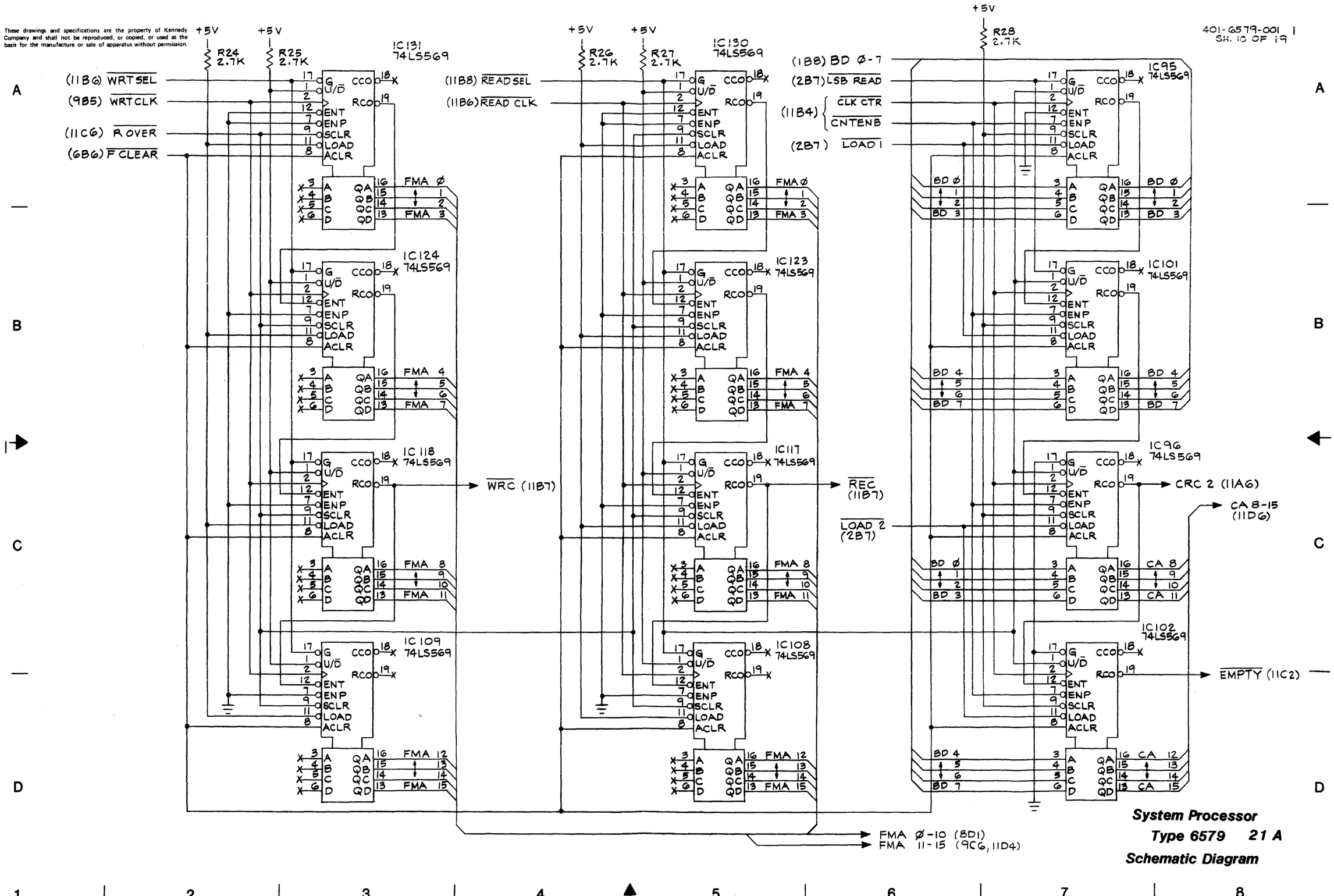
$\overline{\text{OUTRDY}}$ (5C4, 11B4)

$\overline{\text{FF RESET}}$ (6B6)

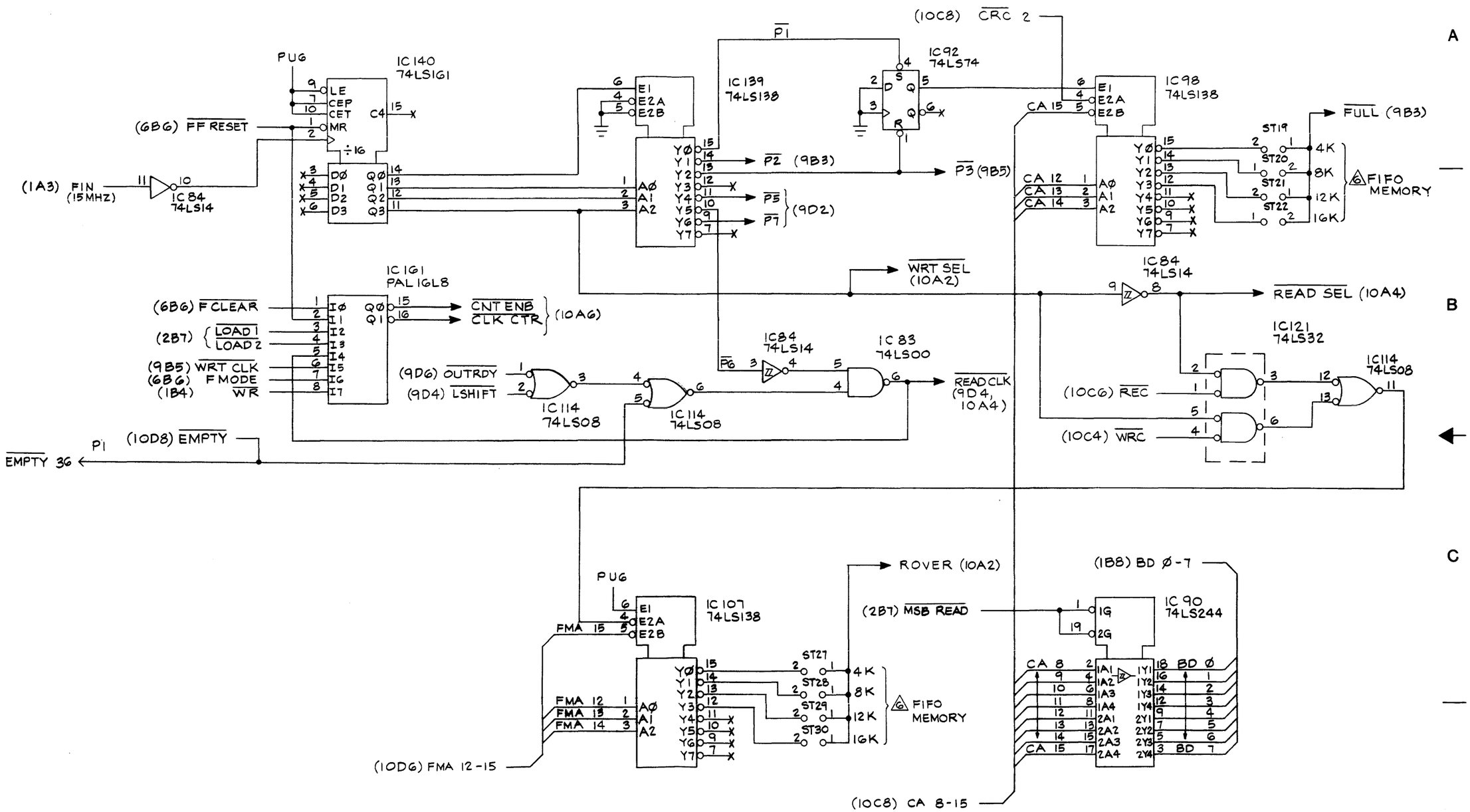
IC43 74LS08

(7C7) SHIFT OUT

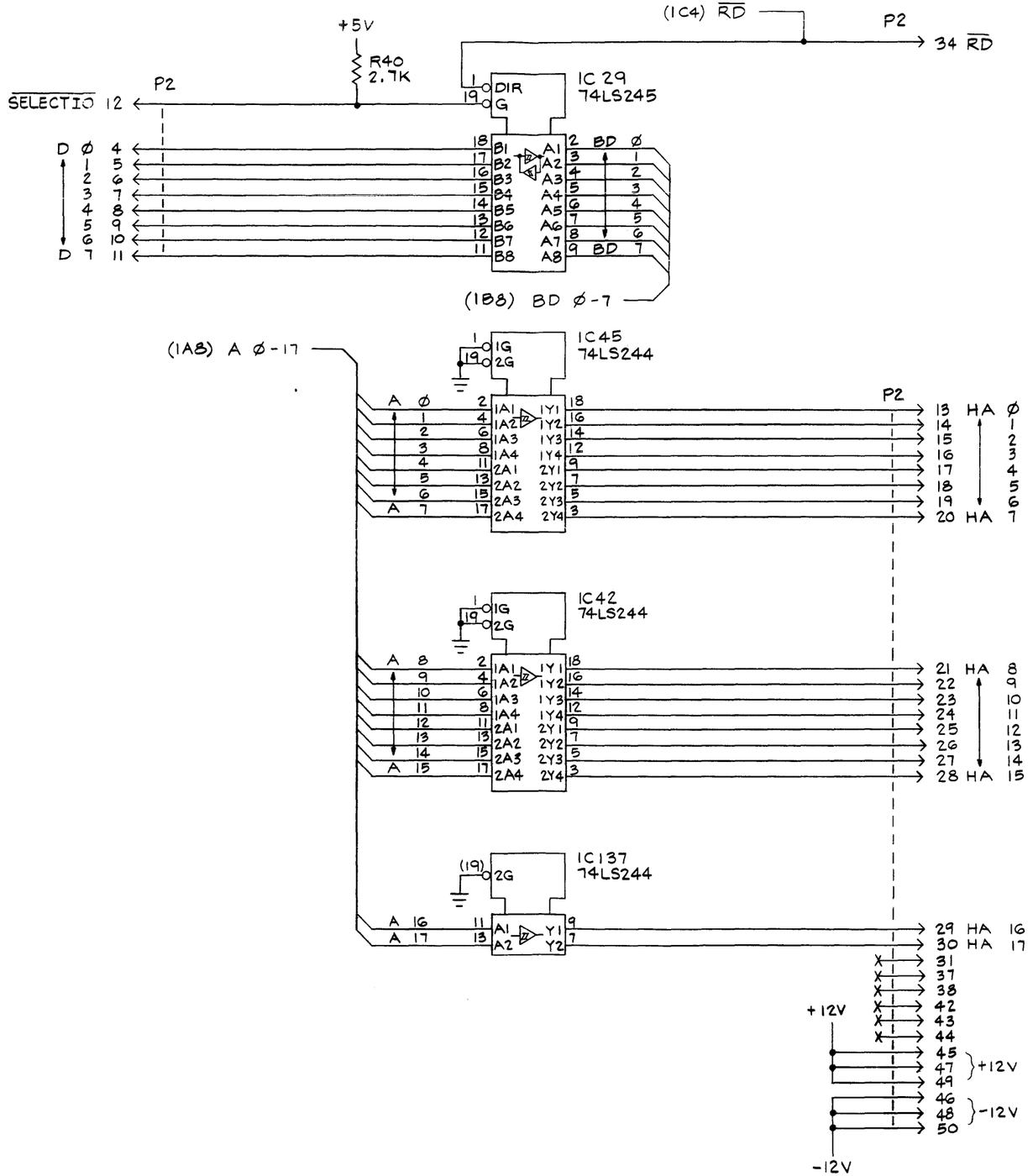
System Processor
Type 6579 21 A
Schematic Diagram



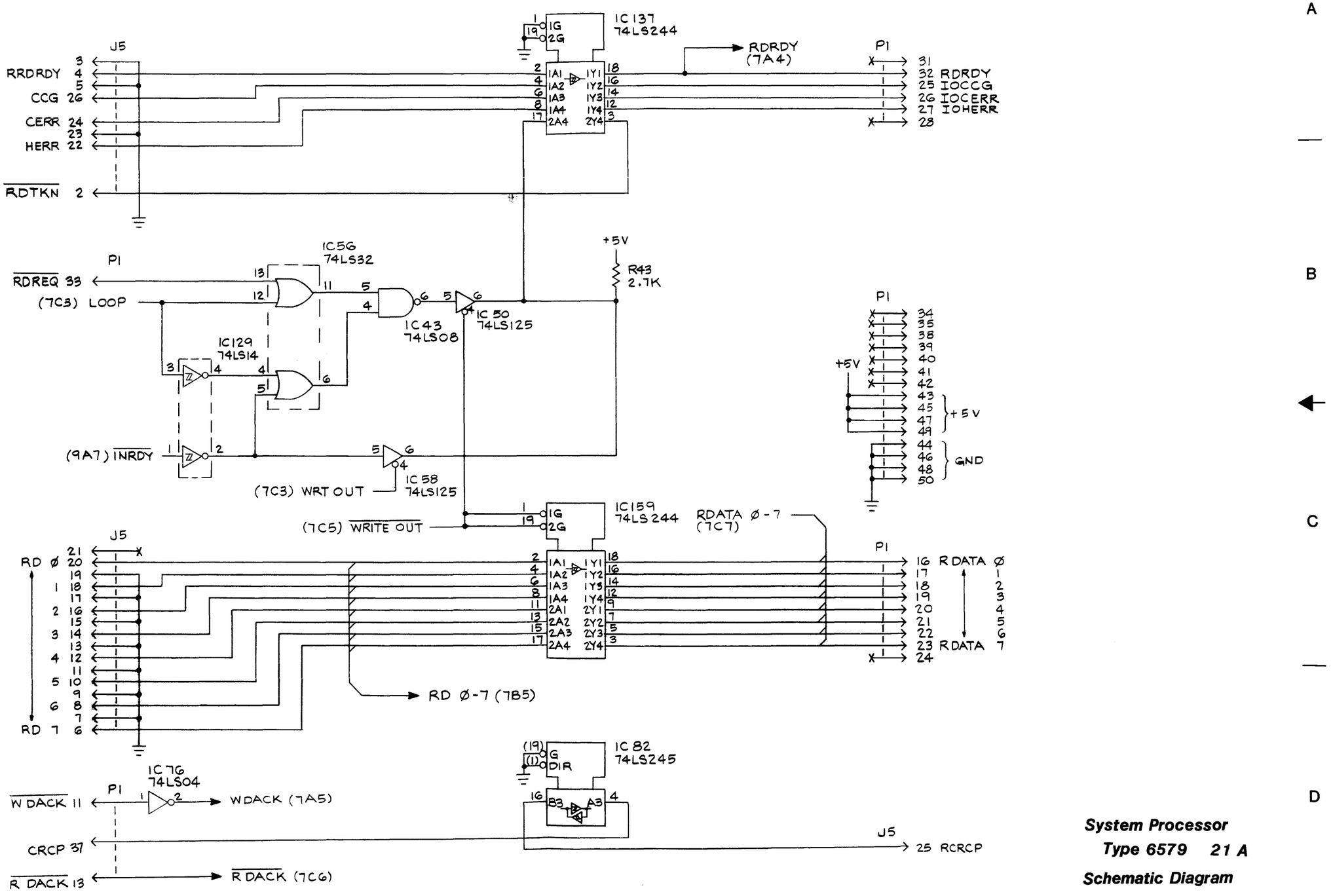
System Processor
Type 6579 21 A
Schematic Diagram



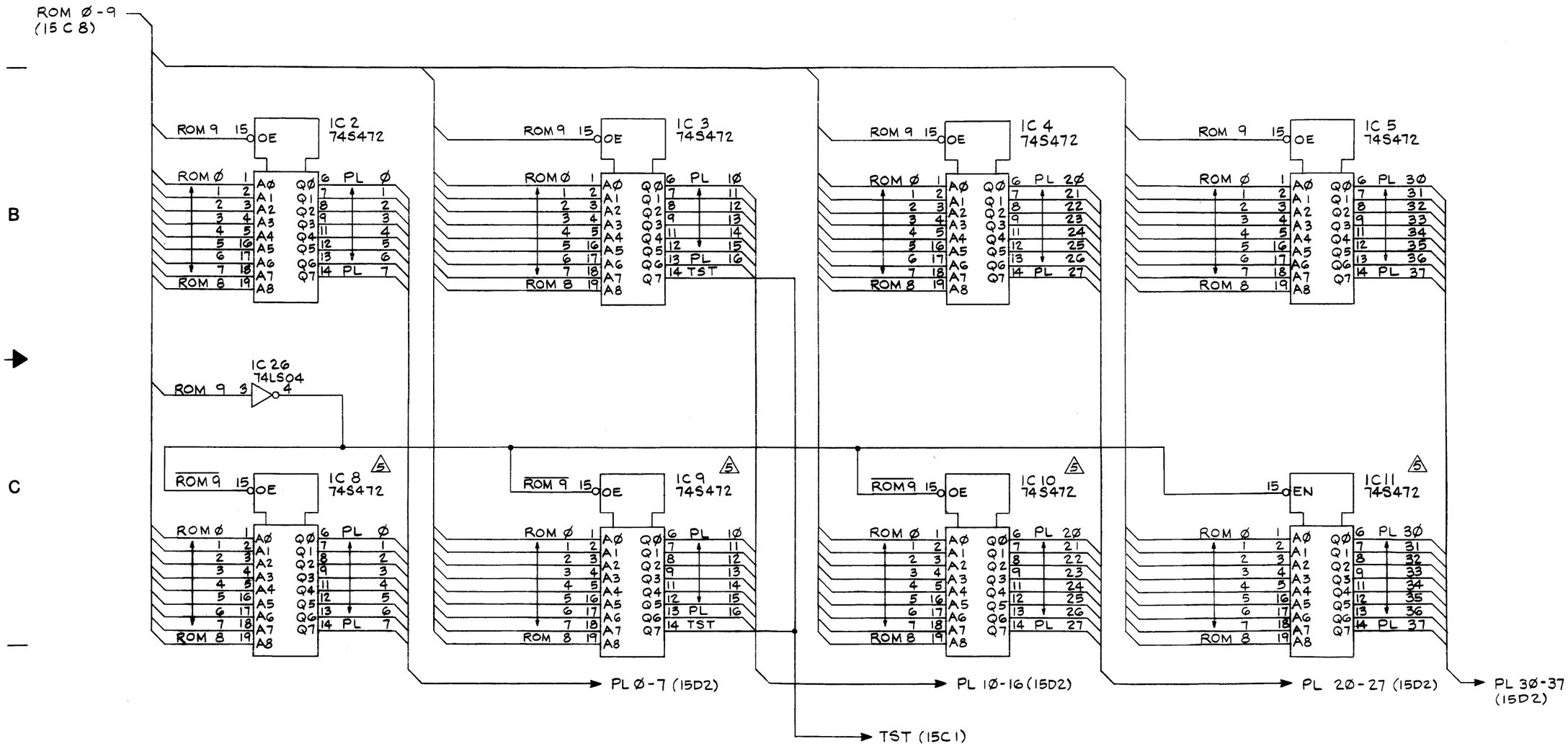
System Processor
Type 6579 21 A
Schematic Diagram



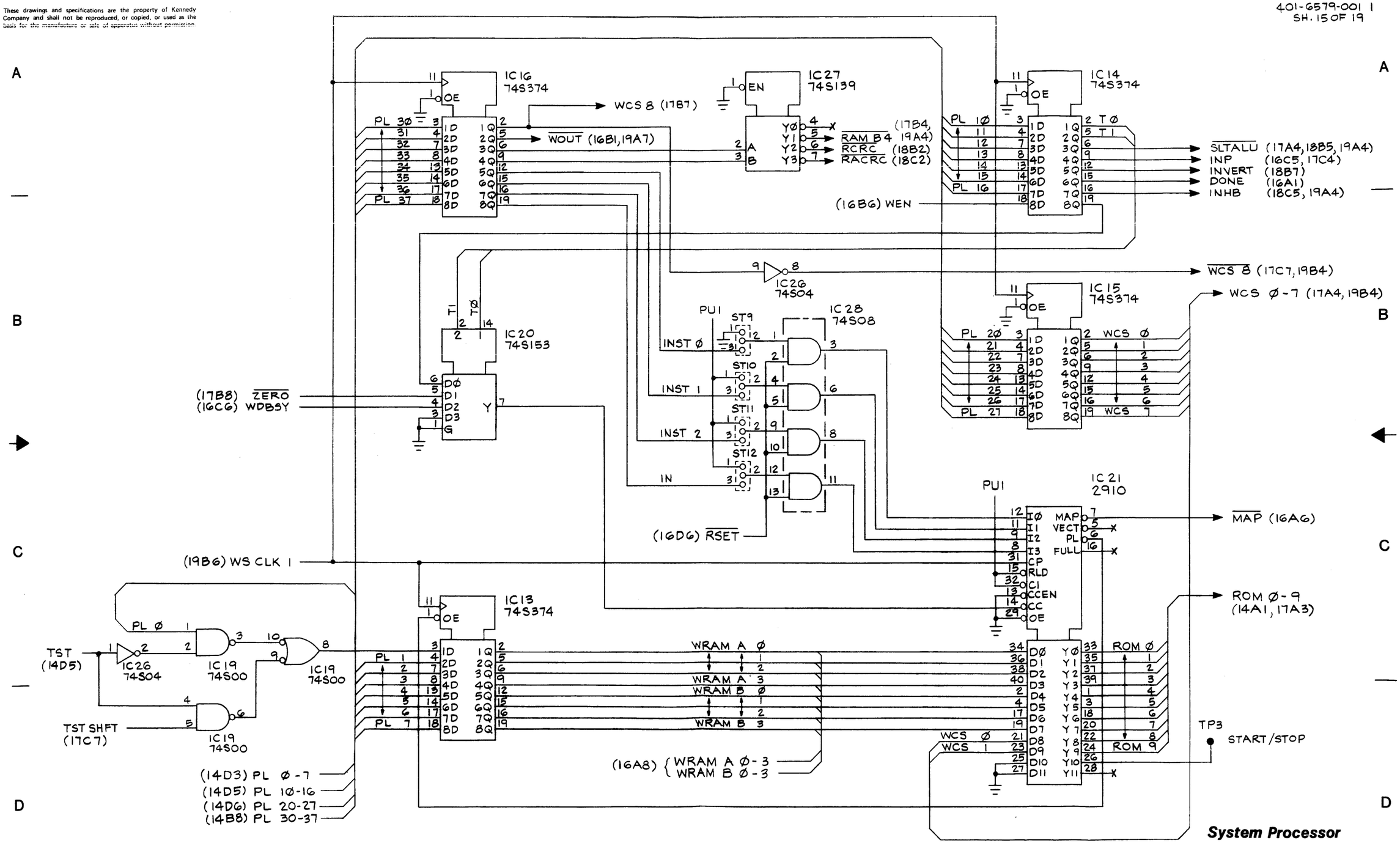
System Processor
Type 6579 21 A
Schematic Diagram



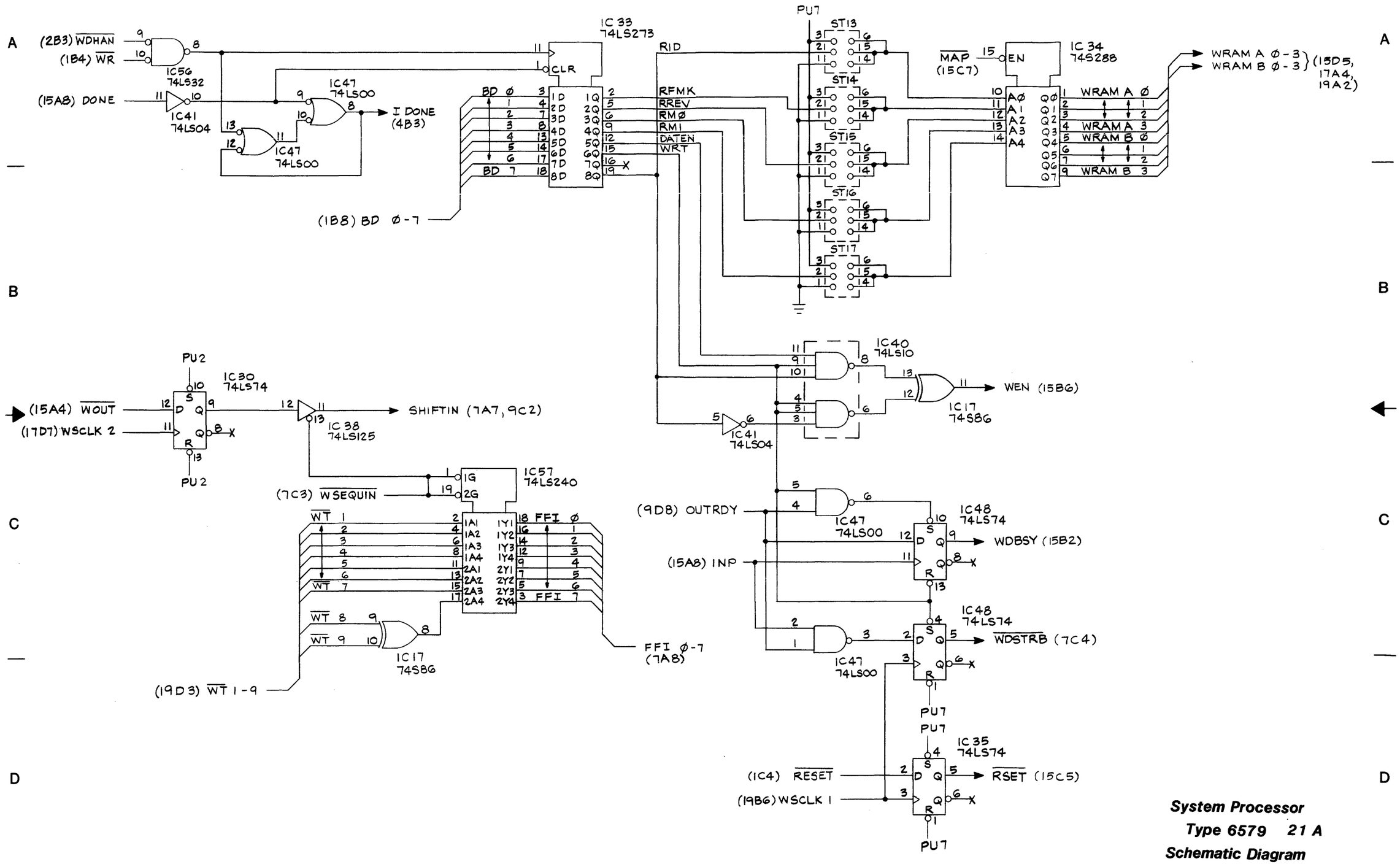
System Processor
Type 6579 21 A
Schematic Diagram



System Processor
Type 6579 21 A
Schematic Diagram



System Processor
Type 6579 21 A
Schematic Diagram



System Processor
Type 6579 21 A
Schematic Diagram

(15B8) WCS Ø-7
(16A8) WRAM A Ø-3 / WRAM B Ø-3
(18D5) WDB Ø-7
(7C5) WDATA Ø-7
(15C8) ROM Ø-7
(15A8) SLTALU
(15A6) RAM B 4
(15A8) INP
WE (19A2)
YB Ø-7 (18A2, 19B6)
WSCLK 2 (16C1, 18A2, 19C5)
TST SHIFT (15D2)
ZERO (15B2)
(15A4) WCS 8
WCS 8 (15B8)

IC 7 2903
IC18 2903
IC 30 74LS74
IC23 74LS125

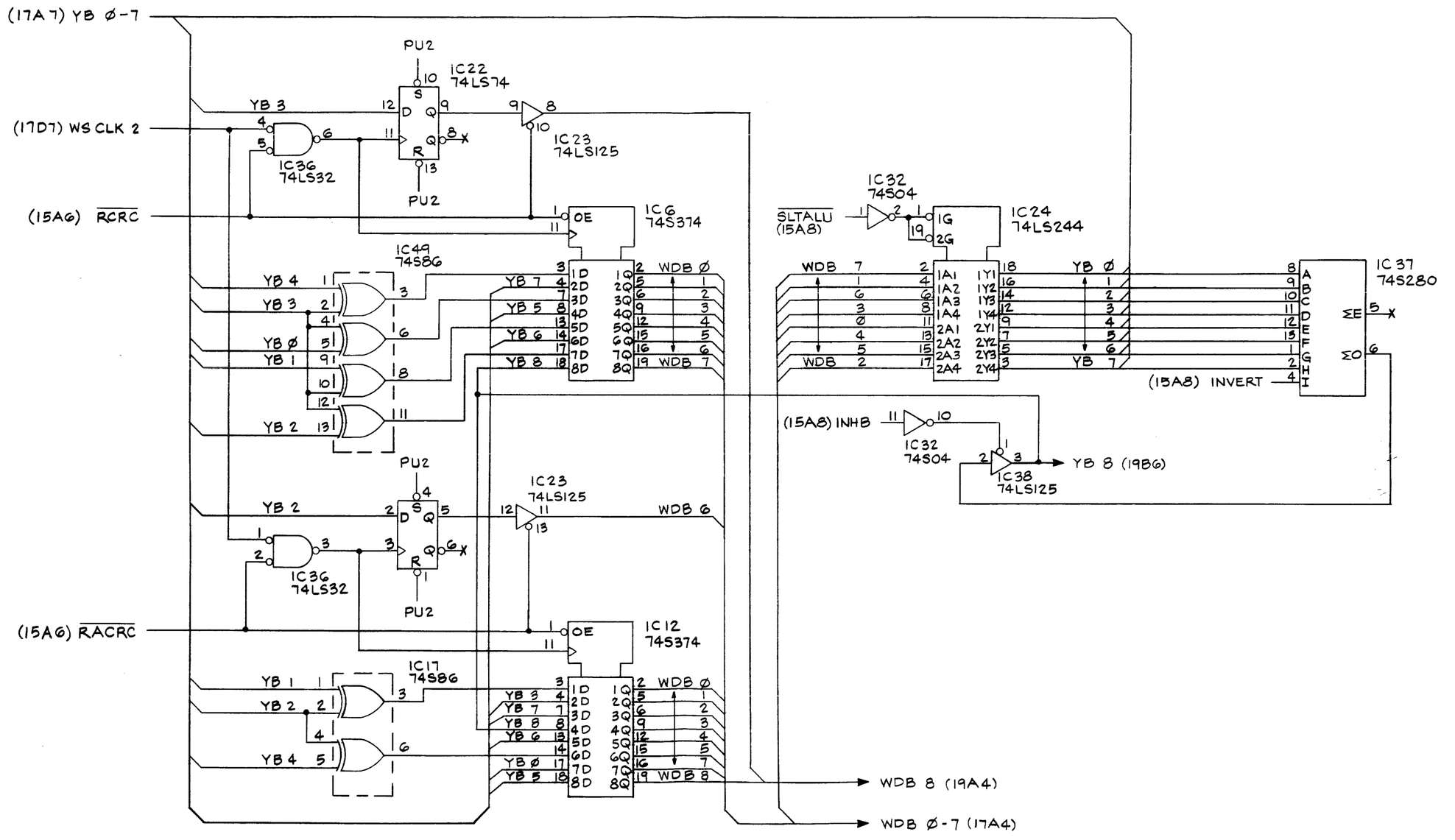
+5V
R2 470
R3 470
R6 470

ST8 ROM 4 / WDA Ø / WDATA 4
ST7 ROM 6 / WDA 1 / WDATA 6
ST6 ROM 3 / WDA 2 / WDATA 3
ST5 ROM Ø / WDA 3 / WDATA Ø
ST1 ROM 5 / WDA 4 / WDATA 5
ST2 ROM 1 / WDA 5 / WDATA 1
ST3 ROM 2 / WDA 6 / WDATA 2
ST4 ROM 7 / WDA 7 / WDATA 7

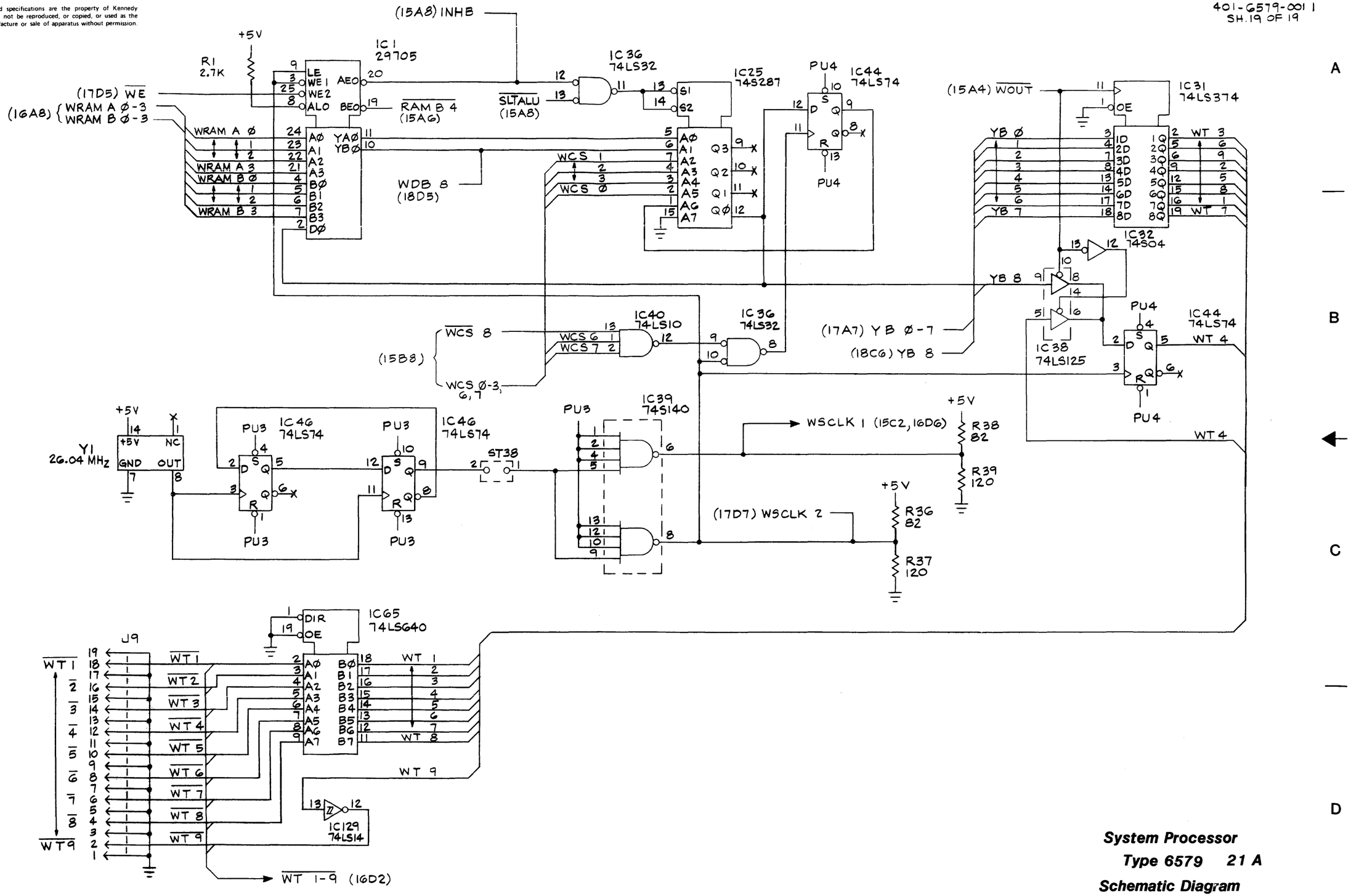
YB Ø
YB 3
YB 4
YB 7

PU2

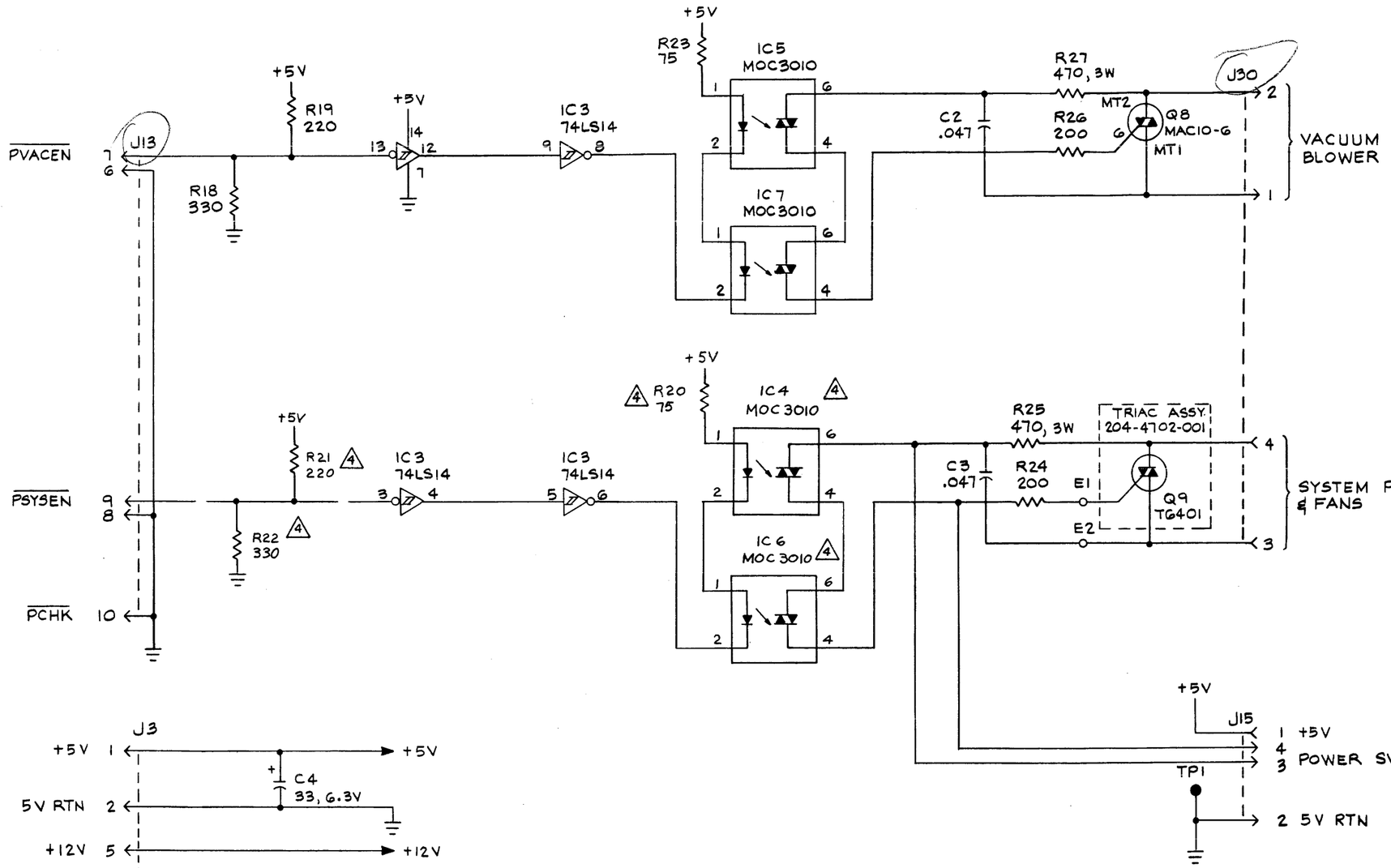
System Processor
Type 6579 21 A
Schematic Diagram



System Processor
Type 6579 21 A
Schematic Diagram



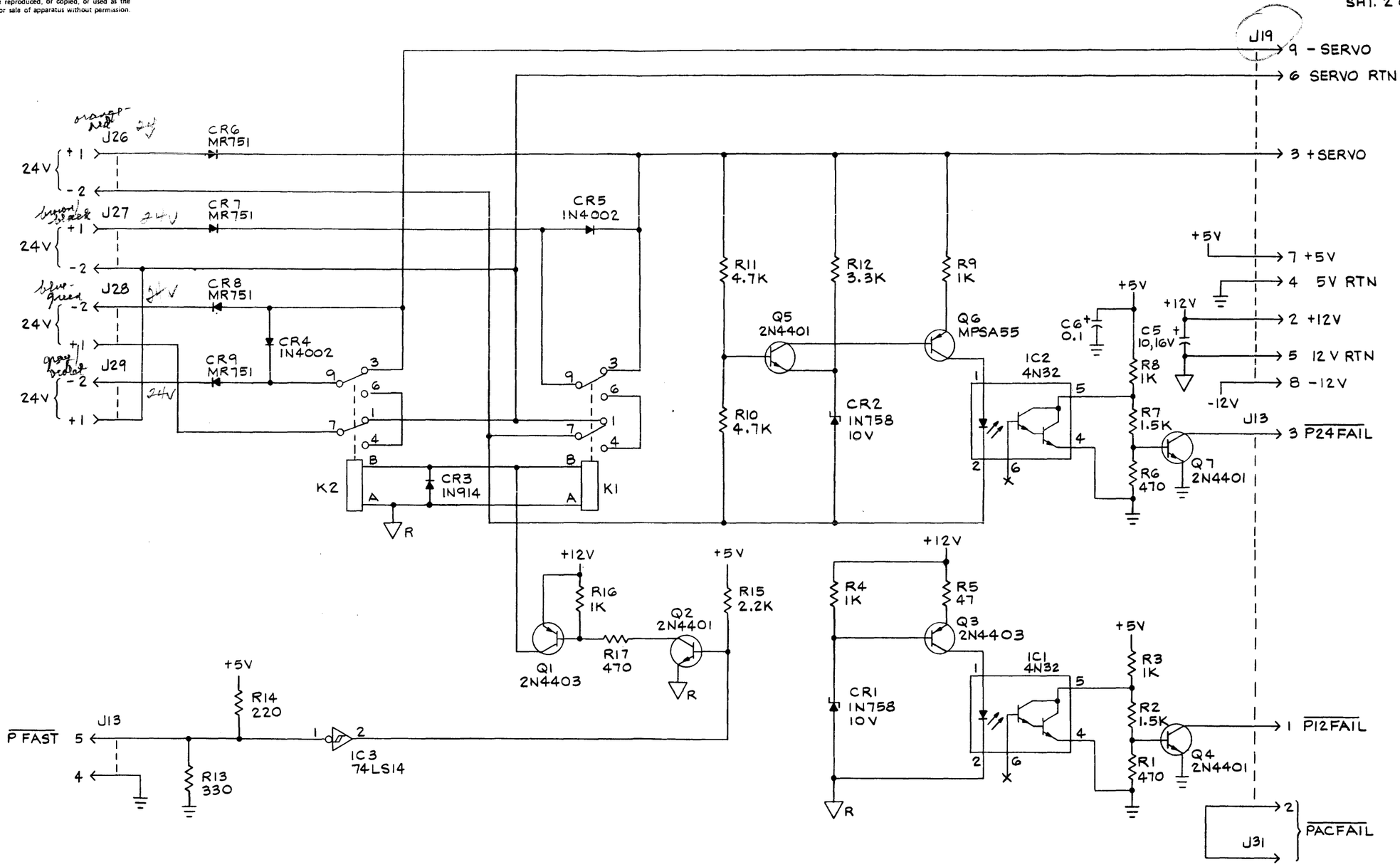
System Processor
Type 6579 21 A
Schematic Diagram



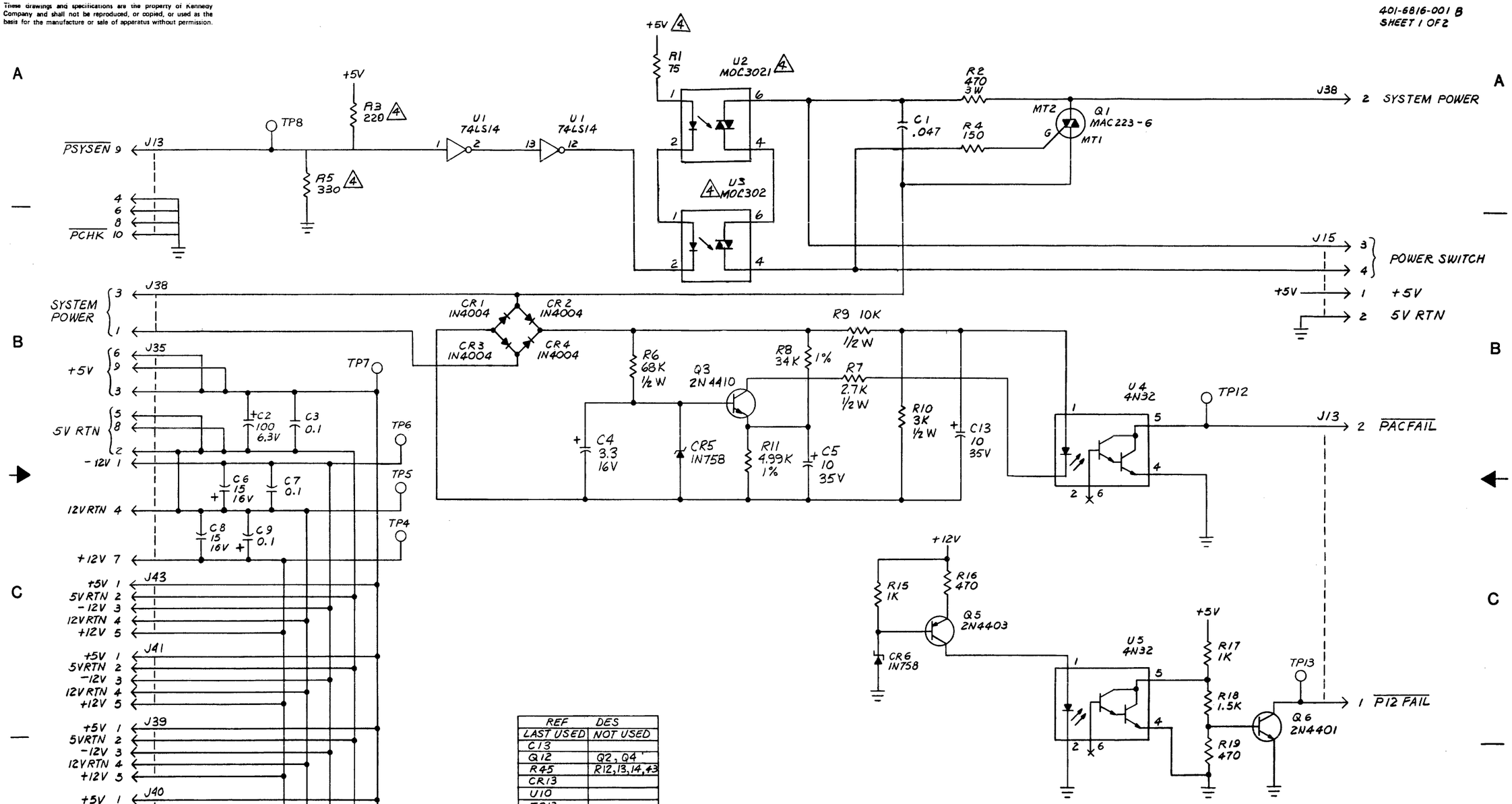
REFERENCE DESIG.	
LAST USED	NOT USED
C6	C1
CR9	—
IC7	
K2	—
Q9	—
R27	R 28-30
TP1	—

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. X INDICATES NO CONNECTION.
4. SHOWN FOR FULL CAPABILITY OF BOARD

Power Supply Control
Type 6604-001 6
Schematic Diagram



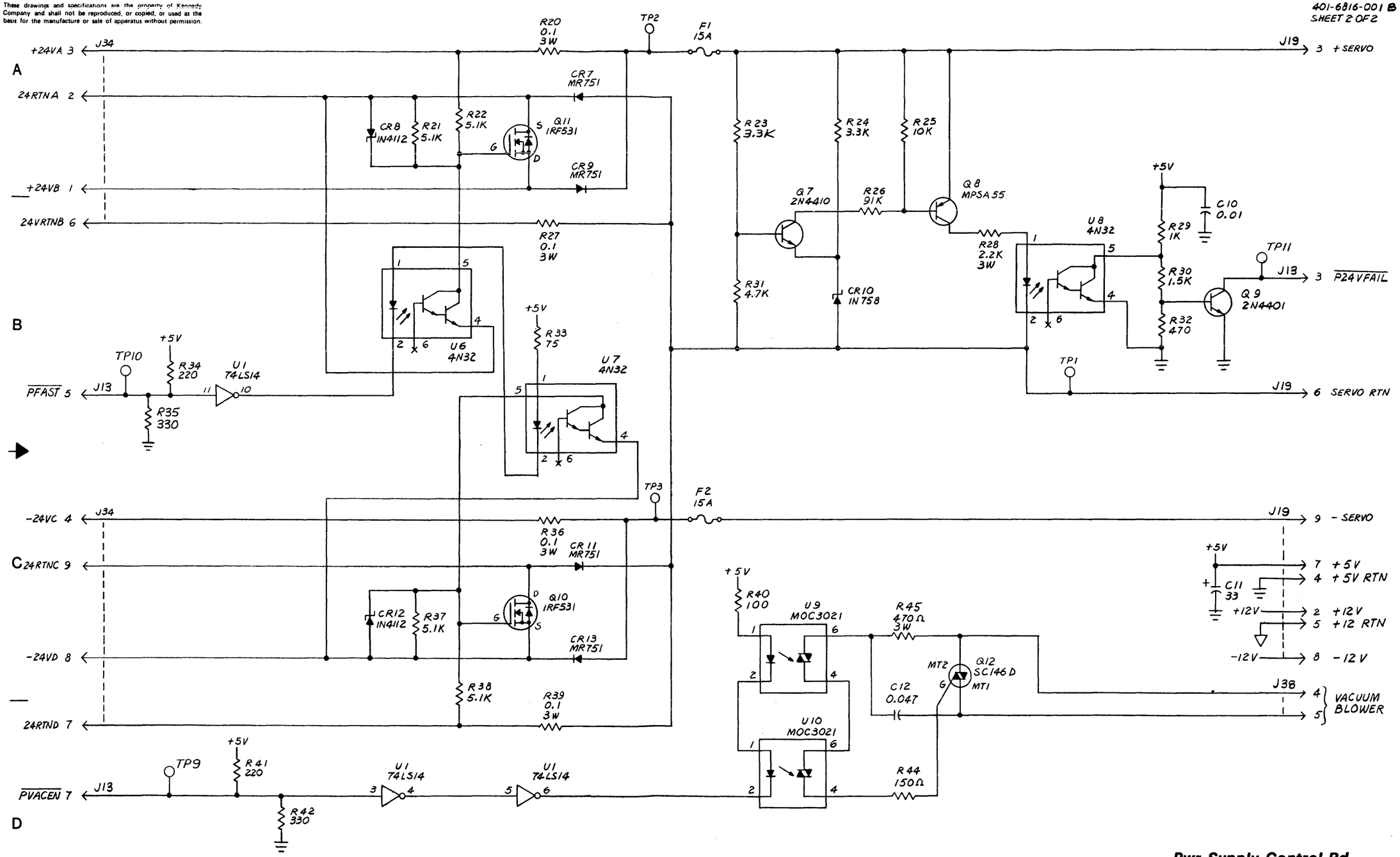
Power Supply Control
Type 6604-001 10
Schematic Diagram



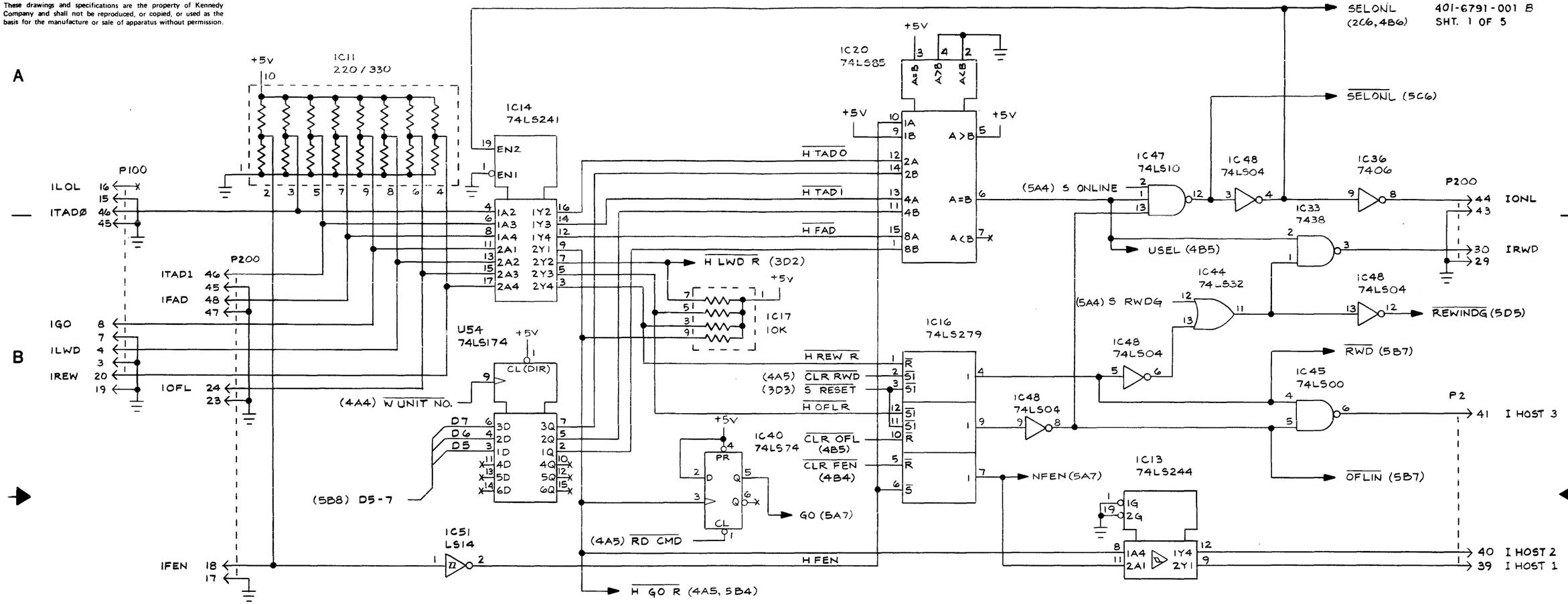
REF DES	
LAST USED	NOT USED
C13	
Q12	Q2, Q4
R45	R12,13,14,43
CR13	
U10	
TP13	
F2	

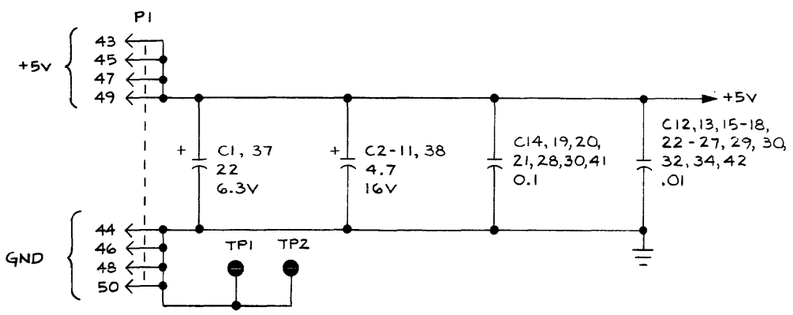
4 SHOWN FOR FULL CAPABILITY OF BOARD.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS ± 5 % 1/4 W.
1. X INDICATES NO CONNECTION.
NOTES: UNLESS OTHERWISE SPECIFIED.

Pwr Supply Control Bd
Type 6816-001 A
Schematic Diagram



Pwr Supply Control Bd
Type 6816-001 A
Schematic Diagram





REF. DESIG	TYPE	+5V	GND
IC45, 50	74LS00	14	7
IC48	74LS04		
IC25, 30, 36	7406		
IC37, 46	74LS08		
IC47	74LS10		
IC51	LS14		
IC44	74LS32		
IC23, 33	7438		
IC38	74LS54		
IC 2, 35, 39	74LS74		
IC40, 41	74LS74	14	7
IC20	74LS85	16	8
IC32	74LS107	14	7
IC24	74LS138	16	8

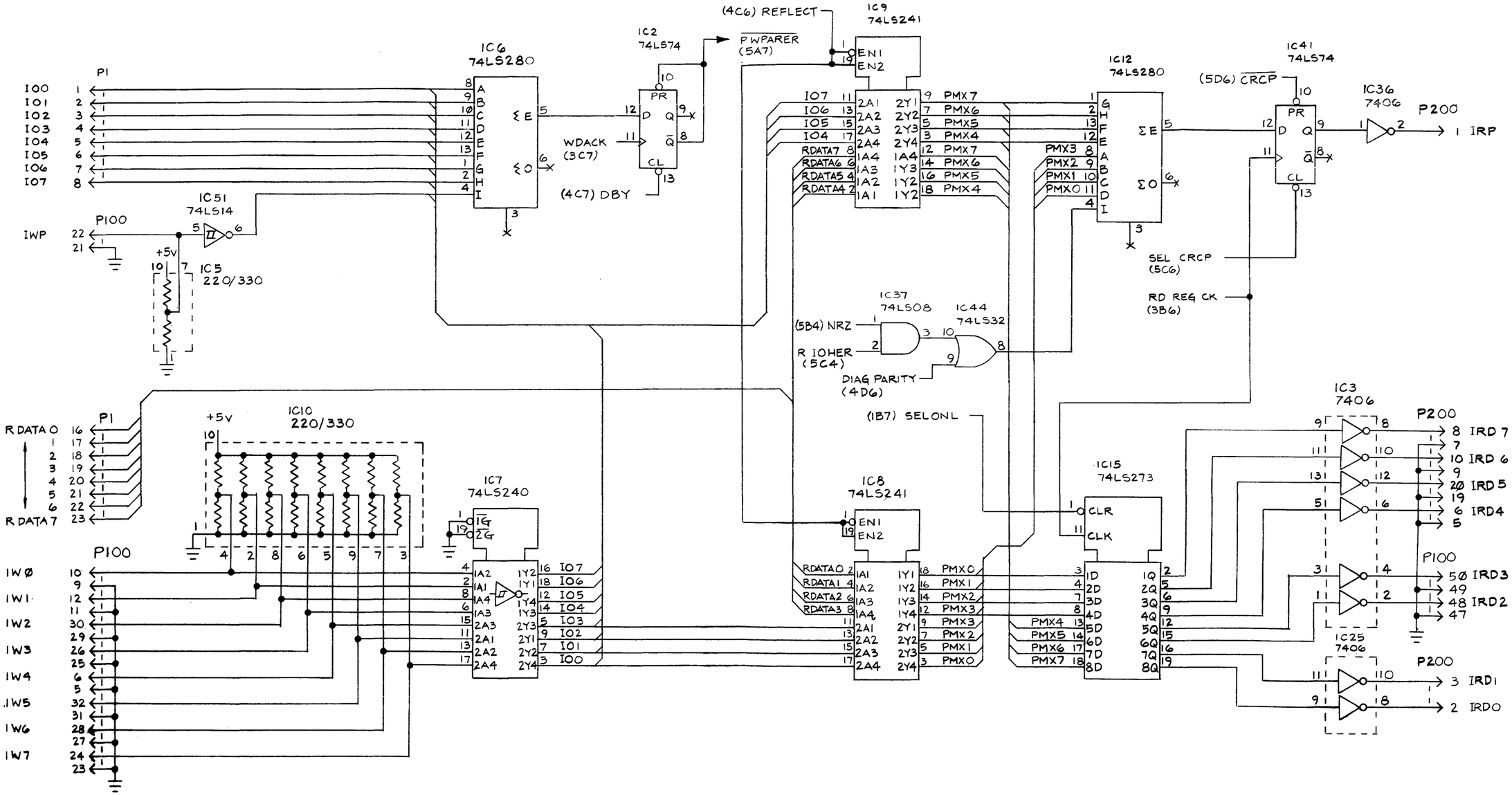
REF. DESIG	TYPE	+5	GND
IC49	74LS157	16	8
IC19, 54	74LS174	16	8
IC43	74LS221	16	8
IC7	74LS240	20	10
IC8, 9, 14	74LS241	20	10
IC1, 13, 18, 28	74LS244	20	10
IC22	74LS259	16	8
IC31	74LS260	14	7
IC15, 21	74LS273	20	10
IC16	74LS279	16	8
IC6, 12	74LS280	14	7
IC3	74LS374	20	10
IC34	16L8	20	10
IC42	74LS193	16	8

REFERENCE DESIG	
LAST USED	NOT USED
C42	C33, 35, 36
R2	
IC54	IC52, 53
S1	
ST9	ST2-5
TP2	

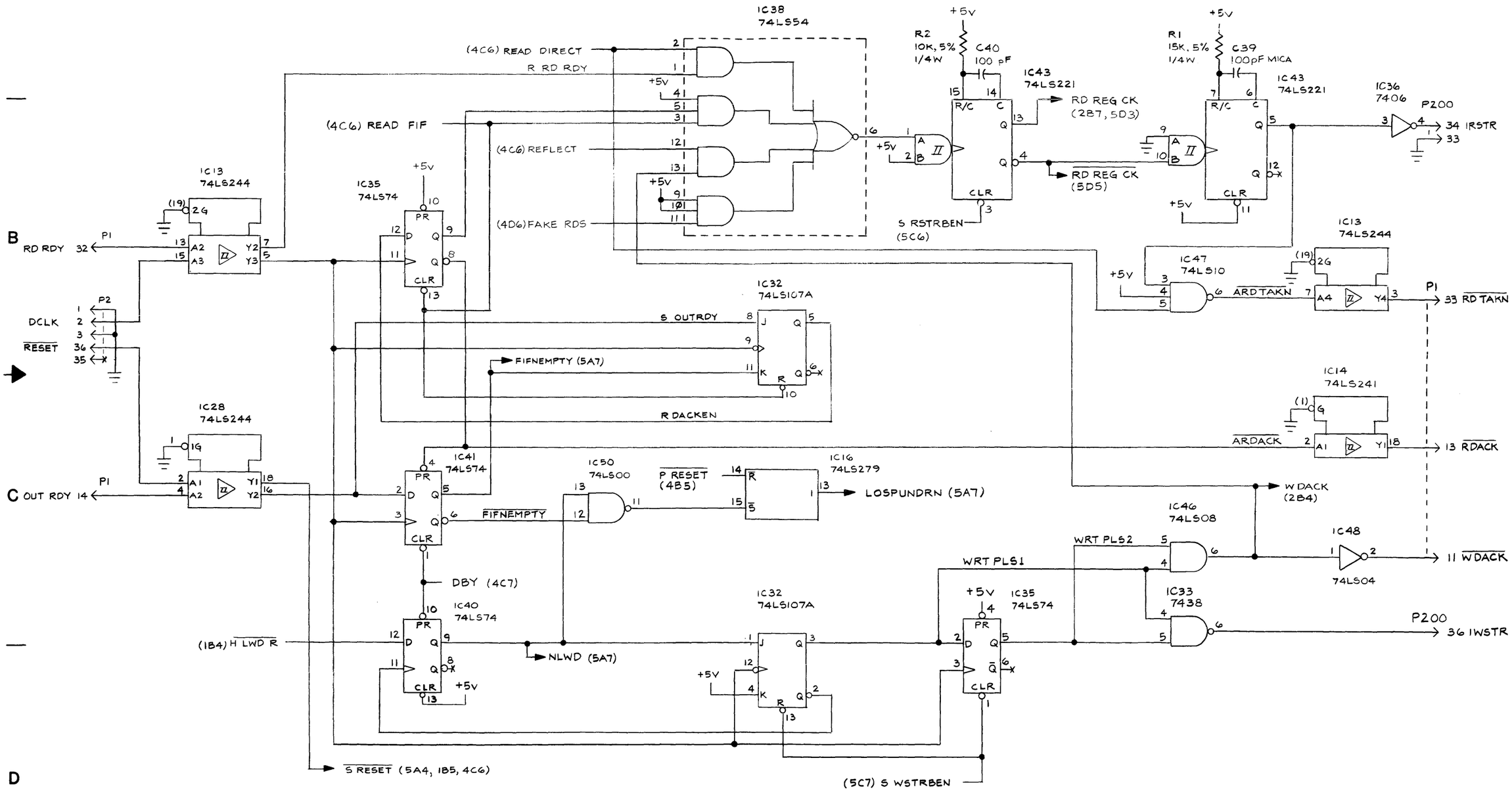
4. IC27 & IC29 ARE A PROVISION FOR TEST USE ONLY. [RESISTOR NETWORK 1.3/3.3K A 10 PIN SIP SUGGESTED BUT NOT SUPPLIED].
3. IC26 HAS THE CAPABILITY OF USING EITHER THE 2764 OR 2732 E PROMS
   2764 - A 28 PIN IC IS SHOWN.
   2732A - A 24 PIN IC IS SHOWN IN PARENTHESIS (SEE ASSY FOR PART USED).
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.

NOTES: UNLESS OTHERWISE SPECIFIED

Pertec Interface
Type 6791-001- B
Schematic Diagram



Pertec Interface
Type 6791-001 B
Schematic Diagram



Pertec Interface
Type 6791-001- B
Schematic Diagram

P2
RD 34
WR 33
MEM 32
SELECTION 12
S HA00 13
S HA01 14
S HA02 15
S HA03 16
S HA04 17
S HA05 18
S HA06 19
S HA07 20
S HA08 21
S HA09 22
S HA10 23
S HA11 24
S HA12 25
S HA13 26
S HA14 27
S HA15 28

IC28 74LS244 (1)
IC51 74LS14
IC37 74LS08
IC34 16L8
IC24 74LS138
IC31 74LS260
IC51 74LS14
IC28 74LS244
IC26 2764 (2732A) 3
IC29 1.3/3.3K 4
IC27 1.3/3.3K 4

W UNIT NO. (1B3)
RS HA00 1
RS HA01 2
RS HA02 3
RD STAT 1 (5A7)
RD OPTION (5A6)
RD CMD (5B4, 1C4)
CLR RWD (1B5)
CLR OFL (1B5)
P RESET (5B5, 3C4)
CLR FEN (1B5)
W STAT 2 (5B6)
W STAT 1 (5A4)
LTCH 1
S RESET (3D3)
DO-7 (5B8)
PROG

IC39 74LS74
P HER (5C6)
(1C4) H GO R
IC46 74LS08
SELONL (1A7)
IC25 7406
P200
42 ICER
41
(1B6) USEL
(5B4) S DENS1
IC45 74LS00
IC47 74LS10
IC48 74LS04
IC36 7406
(5C5) BACK W
(5A4) SBOT
RDY 5
40 ISPEED
39
28 IRDY
27
(5C6) SEL NRW

IC22 74LS259
URDY
DBY (2B4, 3C3)
NRZI + END (5C6)
REFLECT (2A4, 3B4)
READ DIRECT (3A4)
READ FIF (3B3)
FAKE RDS (3B4)
DIAG PARITY (2B5)

IC33 7438
P100
(5C8) FBY
2 IFBY
1
IC23 7438
P200
(5A4) S EOT
22 IEOT
21
IC33 7438
38 IDBY
37
IC23 7438
4
(5A4) S FIL PROT
32 IPROT
33
(5B4) NRZ
26 INRZI
25

Pertec Interface
Type 6791-001- B
Schematic Diagram

1 2 3 4 5 6 7

A B C D

P2
D7 D6 D5 D4 D3 D2 D1 D0

IC21 74LS273
(3D3) S RESET
(4B4) W STAT1
CLR
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
S EOT (4C7)
S BOT (4B5)
S RWDG (1B6)
S FILPROT (4D7)
S ONLINE (1A6)
S DENS1 (4B6)
NRZ (2B5, 4D7)

S1
+5V
IC17 10K

IC4 10K
RD OPTION (4A5)
ST9 ST8 ST7 ST6

IC1 74LS244
1G 2G
TBD3 PAR OPT TBD1 TBDO MEDRATE LO RATE GCR OPT PE OPT
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4 2Y5 2Y6 2Y7 2Y8
D7 D6 D5 D4 D3 D2 D1 D0

IC18 74LS244
(4A5) RD STAT1
(IC5) GO
(3C5) LOSPUNDRN
(3C4) FIFNEMPTY
(3D4) NLWD
(2A4) P WPARER
(1B6) NFEN
(1B7) RWD
(1B7) OFLIN

IC5 220/330
P100
ITHR1 SPARE IDEN IREV IEDIT IERS IWFM IWRT
ST1 S1
P200

IC3 74LS374
(4A5) RD CMD
(IC4) HGO:R
CONTROL
TRI-REMOTE OPT-DENS
D7 D6 D5 D4 D3 D2 D1 D0

IC2 74LS74
P RESET (4B5)
PR D CL Q Q̄

IC19 74LS174
WSTAT 2 (4B4)
CL (DIR)
MUL F-F
S ERROR N/U
S RSTRBEN (3B6)
S WRSTRBEN (3D6)

IC36 7406
FMK
P200 14 13

IC44 74LS32
FBY (4C7)

BACKW (4B5)
(4C6) NRZI + END

IC49 74LS157
SEL
(1A7) SELONL
(4A7) P HER
SEL CRCP (2B7)
SEL NRW (4B6)

IC25 7406
P200 12 11 16 15
I HER
ICCGID

DO-7 (4D5)
D5-7 (IC3)

IC13 74LS244
P1
IOHER IOCCG IOCRCP
R IOHER (2B5)
R IOCCG

IC45 74LS00
IC37 74LS08
RD REG CK (3B6)
REWINDG (1B8)

IC42 74LS193
LD (PIR) CL (PIR)
Q2 Q1 Q4 Q8 BO CO

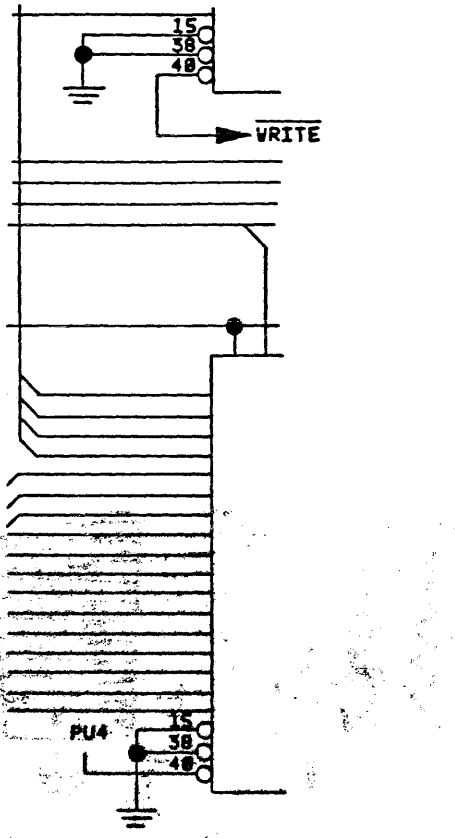
IC51 74LS14
IC45 74LS00
CRCP (2A7)

Pertec Interface
Type 6791-001 B
Schematic Diagram

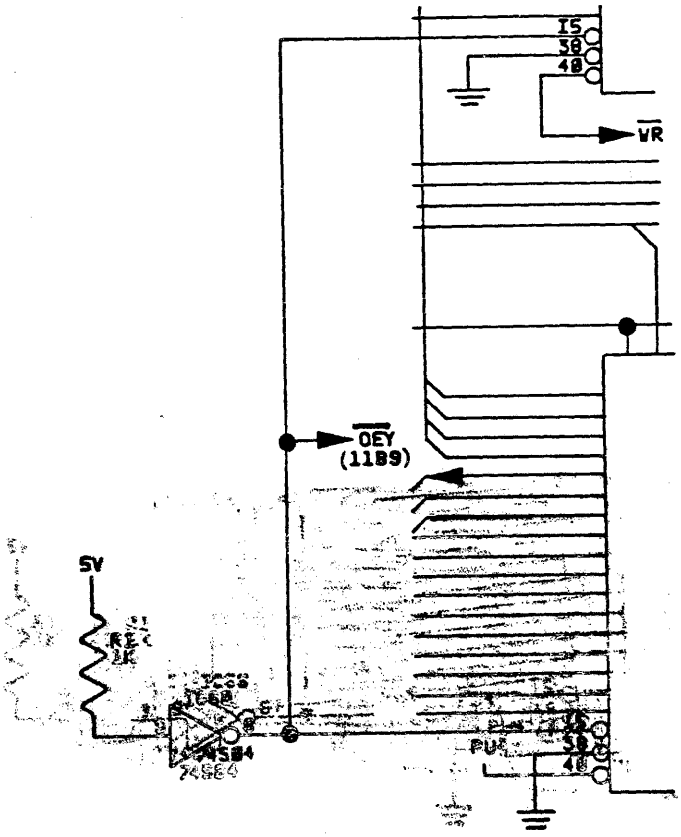
DATE: 7 January 1985
KENNEDY ECN NO: 14240
CODE NO: 18, PCN NO: 18001
PAGE: 3

Schematic Change: Drawing No. 401-6572-001

Sheet 10, WAS:



IS:



Product Information Bulletin

KENNEDY
An Allegheny International Company

PRODUCT	CODE	DATE
9400 MANUAL	9401185	1-11-85

APPROVAL: Engineering	APPROVAL: Marketing	REMARKS
Abdul S. Ali		CORRECTION TO 9400 MANUAL SECTION 4.9 READ/WRITE ADJUSTMENTS

IS

WRITE CURRENT

TRACK	POT
9	R53
8	R47
7	R41
6	R35
5	R29
4	R23
3	R17
2	R11
1	R5

S/B

WRITE CURRENT

TRACK	POT
9	R5
8	R11
7	R17
6	R23
5	R29
4	R35
3	R41
2	R47
1	R53

KENNEDY CO.

DATE: 25 July 1984

PRODUCT CHANGE NOTICE

OEM SERVICE DATA FILE

CHANGE CLASSIFICATION: For Information Only

KENNEDY ECN NO: 13521

MODELS AFFECTED: 9400

CODE NO: 18

PCN NO: 180001

PC BOARD AFFECTED: Pertec Interface, Type 6791

REASON FOR CHANGE/CHANGE DETAILS:

A System Processor Pertec software release kit is presently available for customers experiencing difficulty in reading interchange tapes in PE mode (1600 Bpi) on tapes written on non-Kennedy drives.

The software release kit is provisioned with the latest firmware and includes installation instructions. The kit can be ordered from Kennedy Company under PN 190-7400-001.

ACTION ON UNITS IN SERVICE:

None.

EFFECT ON SPARES:

None.

SERVICE/PARTS TO BE FURNISHED UNDER ASSEMBLIES WARRANTY:

Not applicable.

IDENTIFICATION OF CHANGED ASSEMBLIES:

Assembly 190-6791-001 was raised to revision D. Firmware 190-7400-001 was raised to version 1.D.

DOCUMENTATION CHANGES:

Not applicable.

APPROVAL:

MARKETING

CUSTOMER ENGINEERING

INITIATING ENGINEER

PRODUCT MANAGER

KENNEDY CO.

DATE: 14 October 1984

PRODUCT CHANGE NOTICE

OEM SERVICE DATA FILE

CHANGE CLASSIFICATION: For Information Only

KENNEDY ECN NO: 13585-1

MODELS AFFECTED: 9400

CODE NO: 18

PCN NO: 180002

PC BOARD AFFECTED: Power Supply, Type 6636

REASON FOR CHANGE/CHANGE DETAILS:

The Terminal Block on the Power Supply assembly was modified to meet UL requirements.

ACTION ON UNITS IN SERVICE:

None.

EFFECT ON SPARES:

None.

SERVICE/PARTS TO BE FURNISHED UNDER ASSEMBLIES WARRANTY:

Not applicable.

IDENTIFICATION OF CHANGED ASSEMBLIES:

Assembly #	Revision
190-6636-001	4
190-6636-002	2

DOCUMENTATION CHANGES:

Drawing #	Revision
404-6636-001	3

APPROVAL:

MARKETING

CUSTOMER ENGINEERING

INITIATING ENGINEER

PRODUCT MANAGER

KENNEDY CO.

DATE: 14 October 1984

PRODUCT CHANGE NOTICE

OEM SERVICE DATA FILE

CHANGE CLASSIFICATION: For Information Only

KENNEDY ECN NO: 13879

MODELS AFFECTED: 9400

CODE NO: 18

PCN NO: 180003

PC BOARD AFFECTED: System Processor, Type 6579

REASON FOR CHANGE/CHANGE DETAILS:

The multiwire System Processor Board was upgraded to a printed circuit board, implementing Kennedy Co. latest manufacturing techniques.

ACTION ON UNITS IN SERVICE:

None.

EFFECT ON SPARES:

None.

SERVICE/PARTS TO BE FURNISHED UNDER ASSEMBLIES WARRANTY:

Not applicable.

IDENTIFICATION OF CHANGED ASSEMBLIES:

The multiwire version, 190-6579-001 was changed to 190-7579-001. The top assemblies were revised as follows:

Assembly #	Revision	Assembly #	Revision	Assembly #	Revision
192-9400-001	6	192-9400-007	6	192-9400-016	B
192-9400-002	6	192-9400-008	6	192-9400-020	4
192-9400-003	7	192-9400-009	7	192-9400-021	B
192-9400-004	C	192-9400-013	3	192-9400-501	4
192-9400-005	C	192-9400-014	4	192-9400-502	2
192-9400-006	D				

DOCUMENTATION CHANGES:

Not applicable.

APPROVAL:

_____ MARKETING

_____ CUSTOMER ENGINEERING

_____ INITIATING ENGINEER

_____ PRODUCT MANAGER

KENNEDY CO.

DATE: 14 October 1984

PRODUCT CHANGE NOTICE

OEM SERVICE DATA FILE

CHANGE CLASSIFICATION: For Information Only

KENNEDY ECN NO: 13525, 13580, 13581

MODELS AFFECTED: 9400

PC BOARD AFFECTED: Power Supply, Types 6636 & 6638
Chassis Assembly, Type 6715

CODE NO: 18

PCN NO: 180004

REASON FOR CHANGE/CHANGE DETAILS:

1) Power Supplies, Type 6636 and 6638 were removed from the Deck and Chassis assembly drawings and added to the 9400 (Top Assembly) drawings. This allows the standard Deck and Chassis to be used with all 9400 Models.

2) The assembly drawings for the Deck and Chassis were upgraded to meet UL requirements on the Rear Fan Assembly.

ACTION ON UNITS IN SERVICE:

None.

EFFECT ON SPARES:

None.

SERVICE/PARTS TO BE FURNISHED UNDER ASSEMBLIES WARRANTY:

Not applicable.

IDENTIFICATION OF CHANGED ASSEMBLIES:

The following assemblies were upgraded to the revision levels as indicated:

Assembly	Revision	Assembly	Revision
190-6715-001	B1	192-9400-009	6B
190-6715-002	3	192-9400-010	3A
192-9400-001	5B	192-9400-011	3A
192-9400-002	5B	192-9400-012	3A
192-9400-003	6B	192-9400-013	2B
192-9400-004	B3	192-9400-014	3B
192-9400-005	B3	192-9400-016	A1
192-9400-006	C2	192-9400-020	3C
192-9400-007	5B	192-9400-501	3B
192-9400-008	5B	192-9400-502	1B

DOCUMENTATION CHANGES:

The following documents were upgraded to the revision levels as indicated:

Drawing	Revision
404-6715-001	C
404-6715-002	3

APPROVAL:  MARKETING PRODUCT MANAGER

107508A

Warranty

The Company warrants its devices against faulty workmanship or the use of defective materials (except in those cases where the materials are supplied by OEM) for a period of one year from the date of shipment to OEM, with the exception of ¼" cartridge products which are warranted for a period of ninety (90) days.

The liability of the Company under this warranty is limited to replacing, repairing, or issuing credit (at the Company's discretion) for any devices which are returned by OEM during such period provided that (a) the Company is promptly notified in writing upon discovery of such defects by OEM; (b) the defective unit is returned to the Company, transportation charges prepaid by OEM; and (c) the Company's examination of such unit shall disclose to its satisfaction that such defects have not been caused by misuse, neglect, improper installation, repair alteration or accident.

Kennedy Company is continually striving to provide improved performance, value and reliability in its products and reserves the right to make these changes without being obligated to retrofit delivered equipment.

KENNEDY
ALLEGHENY INTERNATIONAL

KENNEDY

ALLEGHENY INTERNATIONAL

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