Operation and Maintenance Manual

Model 9219

Formatter

FCC CERTIFIED COMPUTER EQUIPMENT

Warning: This equipment generates and uses radio frequency energy and if not installed and used in accordance with the instruction manual may cause harmful interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment.

Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

MODEL 9219 SPECIFICATIONS

1.1 INTRODUCTION

The Kennedy Model 9219 Formatter is designed to format seven and/or nine track NRZI and/or phase encoded tapes. It can be used in conjunction with 10 ips through 125 ips tape transports and contains the electronics required to read or write ANSI and IBM compatible formats. When only the NRZI format is desired, the unused phase encoding electronics may be omitted. Electrical and mechanical specifications are provided in Table 1-1.

The address and control circuits accept input commands from the computer and convert these commands into signals which initiate the desired operations on the selected tape transport.

All timing, as well as data transmission to and from the tape deck and formatter, is controlled by means of a 12 bit bipolar Shottky microprocessor. The time required to complete one instruction is 347 nsec. Several options have been made available through switchable ICs on the 7831 interface board.

The formatter can also operate in any one of four character densities and at any one of eight tape speeds. (Refer to paragraph 2.5.)

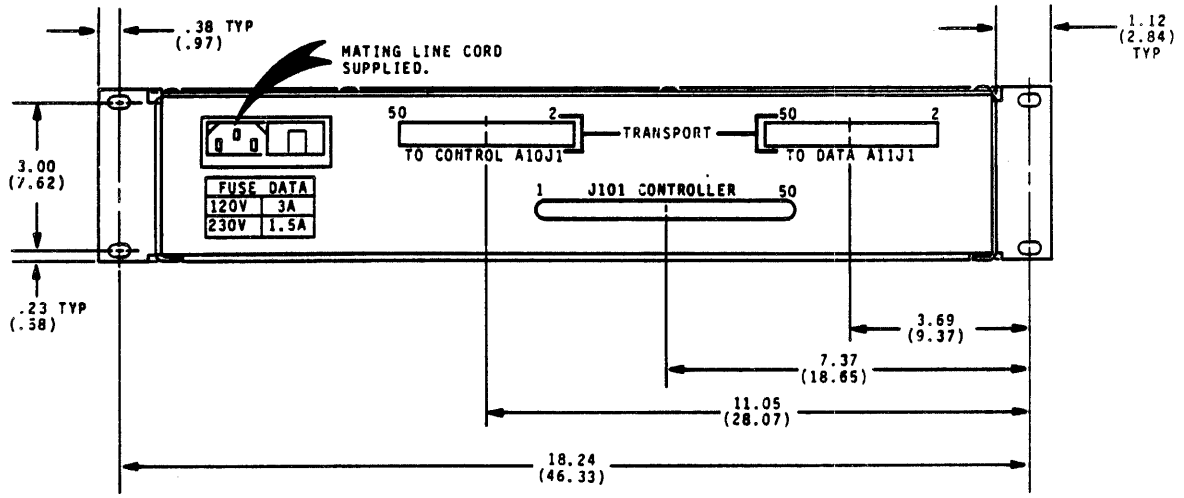
The one-to-one wiring configuration of the masterboard's foil pattern permits the user to interchange the circuit boards. This eliminates the possibility of inserting a circuit board into the wrong slot and possibly overloading the ICs. It also makes the boards easily accessible for troubleshooting.

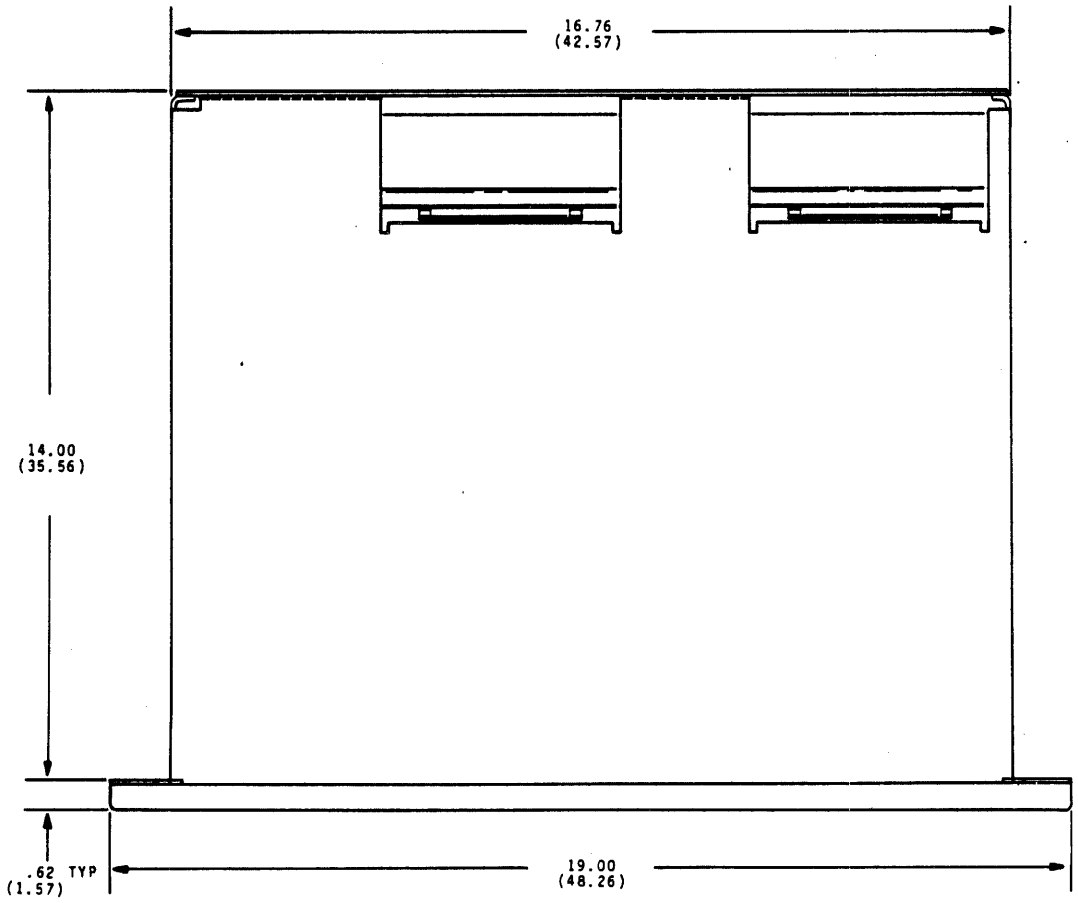
Dimensions*	
Formatter	
Height	4 inches (10.16 cm)
Width	15.6 inches (39.62 cm)
Depth	14 inches (35.56 cm)
Weight	20.6 pounds (9.33 kg)
Operating environment	
Ambient temperature	+2° to 50°C
Relative humidity (noncondensing)	15% to 95%
Altitude	to 30,000 feet (9120m)
Power requirements	
Single density	50 va
NRZI and phase encoded	75 va
Drivers	26LS31 or equivalent
Receivers	26LS32 or equivalent

*Formatter only when not embedded.

Table 1-1. Electrical and Mechanical Specifications

REAR VIEW





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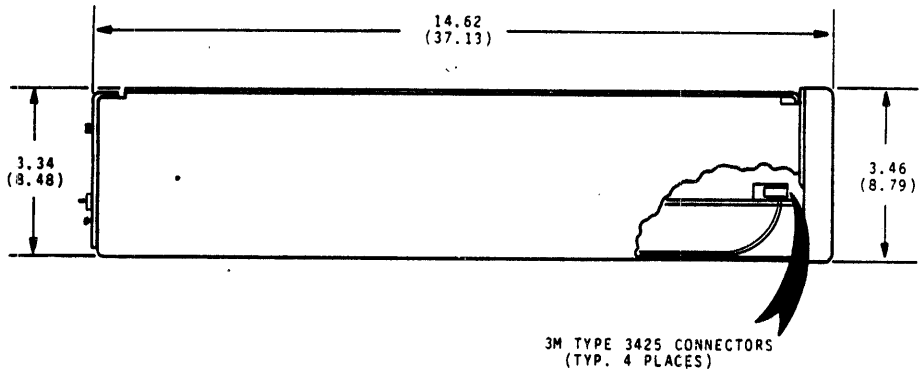
BOTTOM VIEW

SIDE VIEW



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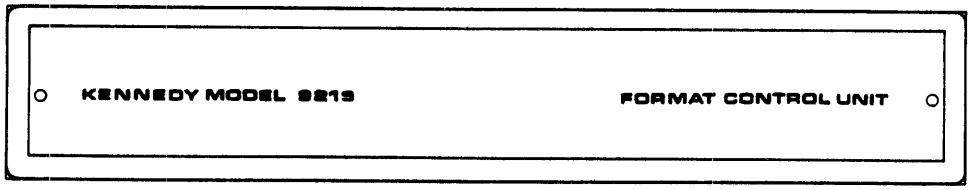


FRONT VIEW

410-4030

Figure 1-1.
Outline and Installation Drawing
Model 9219

MODEL 9219 INTERFACE CHARACTERISTICS

2.1 INTERFACE SIGNAL CHARACTERISTICS

Signals from the controller to the Model 9219 must conform to the following specifications:

Levels	Line A	Line B
	low = true	low = false
	high = false	high = true

Pulses	Line A	Line B
	low = true	low = false
	high = false	high = true.

Minimum pulsewidth = 1 microsecond

Output signals from Model 9219 are driven by differential line driver AM26LS31 or equivalent. Input signals to the 9219 are received by differential line receivers AM26LS32 or equivalent. These input signals are terminated by a parallel-series resistor network, consisting of two 1.5K ohms and one 100 ohm resistors. The interface connector is composed of twisted pairs of wires which transmit input and output signals between the differential line drivers and receivers. The connector pin assignments are provided in Table 2-3.

2.2 INTERFACE INPUT SIGNALS
(Controller to Formatter)

The following paragraphs describe the specifications and functions for each input signal required from the computer interface to the formatter. Under the signal name are listed its mnemonic designation and

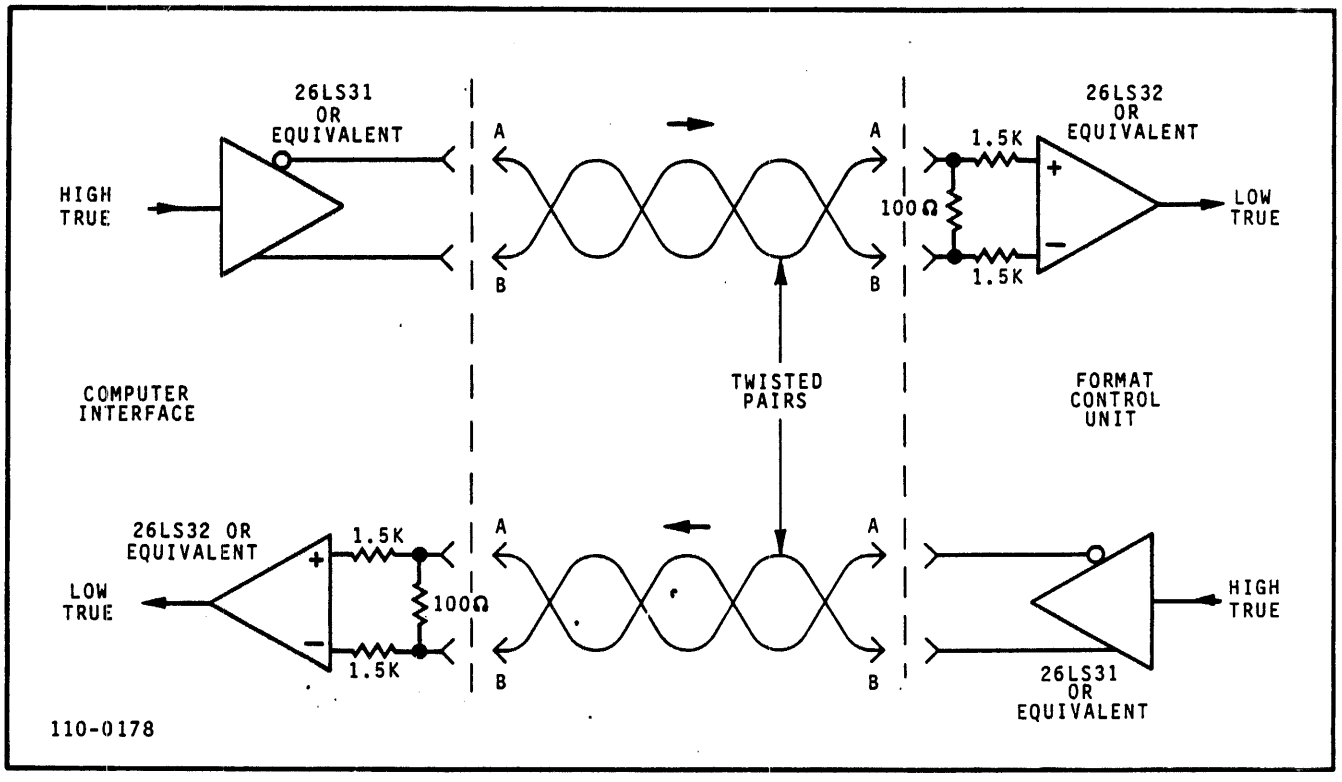


Figure 2-1. Typical Interface Configuration

SIGNAL	MNEMONIC	LEVEL OR PULSE
INTERFACE INPUTS (CONTROLLER TO FORMATTER)		
FORMATTER ADDRESS	FAD	L
TRANSPORT ADDRESS	TAD0,TAD1	L
INITIATE COMMAND	GO	P
REVERSE/FORWARD	REV	L
WRITE/READ	WRT	L
WRITE FILE MARK	WFM	L
EDIT	EDIT	L
ERASE	ERASE	L
REWIND	REW	P
DENSITY SELECT	DEN	L
PARITY SELECT	PAR	L
OFFLINE COMMAND	OFL	P
LAST WORD	LWD	L
FORMATTER ENABLE	FEN	L
WRITE DATA LINES	WP, W0-W7	L
INTERFACE OUTPUTS (FORMATTER TO CONTROLLER)		
FORMATTER BUSY	FBY	L
DATA BUSY	DBY	L
HARD ERROR	HER	P
CHECK CHARACTER GATE	CCG	L
IDENTIFICATION	IDENT	L
CORRECTED ERROR	CER	P
FILE MARK	FMK	P
WRITE STROBE	WRST	P
READ STROBE	RSTR	P
READ DATA LINES	RP, R0-R7	L

Table 2-1 Input/Output Signal List

the connector and active pin designations refer to the interface cable connector that mates with the corresponding card edge connector on the formatter. An I/O signal list is provided in Table 2-1.

FORMATTER ADDRESS

FAD Level J1-A1/B1

A level which selects one of two formatters. FAD false selects formatter address 0; FAD true selects formatter address 1. The formatter addresses are determined by an address switch on the formatter PCBA. Normally, the formatter must be selected in order to perform any formatter operations.

TRANSPORT ADDRESS

TAD0 Levels J1-A24/B24;
TAD1 J1-A23/B23

The states of these lines determine which of up to four transports are selected by the formatter. The following lists defines the tape transport addresses produced as a result of the various TAD0, TAD1.

TAD0	TAD1	ADDRESS
0	0	SLT0
0	1	SLT1
1	0	SLT2
1	1	SLT3

INITIATE COMMAND

GO Pulse J1-A5/B5

A pulse which initiates any command specified by the command lines described in the following paragraphs. Information on the command lines is copied in the corresponding formatter flip-flops on the trailing edge of the GO pulse. FBY is set true when the GO pulse is given with the formatter and the selected transport ready.

COMMAND LINES

The levels on these lines issue a command to the formatter on the trailing edge of the GO pulse. The REV, WRT, WFM, EDIT, ERASE, PAR and DEN levels must be held steady from 0.5 microsecond prior to the trailing edge to 0.5 microsecond following the trailing edge of the GO pulse.

REVERSE

REV Level J1-A6/B6

A level which initiates reverse tape motion when true. When false, this level specifies forward tape motion.

WRITE

WRT Level J1-A7/B7

Write mode is specified when this level is true; read mode is specified when this level is false.

WRITE FILE MARK

WFM Level J1-A8/B8

When this level and WRT are true, the formatter will write a file mark on the tape.

EDIT

EDIT Level J1-A9/B9

EDIT true and REV true modify the read reverse stop delay to optimize head positioning for a subsequent edit operation. When the EDIT level is true and WRT is true, the OVW (overwrite) line is activated and the selected transport operates in the edit mode.

ERASE

ERASE Level J1-A10/B10

ERASE true and WRT true cause the formatter to execute a dummy write command. The formatter

will issue a normal write command but no data will be recorded. A length of tape, as defined by LWD, will be erased. A dummy write file mark command will be issued when ERASE, WRT/READ and the WFM command lines are true. During this operation, approximately 3.75 inches (9.52 cm) of tape will be erased.

DENSITY SELECT

DEN Level J1-A11/B11
(Optional, 7 track NRZI only)

When true, this optional level selects the lower of two possible data transfer packing densities. When this level is false, the higher packing density is selected.

PARITY SELECT

PAR Level J1-A12/B12
(NRZI only)

The levels on this line control the parity mode for write or read data transfer. When true the even (BCD) parity mode is selected; when this level is false, the odd (binary) parity mode is selected.

REWIND

REW Pulse J1-A3/B3

A pulse which causes the selected online transport to rewind to load point. This pulse is directly routed to the transport and does not cause the formatter to go busy.

OFFLINE COMMAND

OFL Pulse J1-A2/B2

This pulse causes the selected transport to go offline without causing the formatter to go busy.

LAST WORD

LWD Level J1-A13/B13

When this level is true during a write or erase command, it indicates that the next character to be strobed into the formatter is the last character of the record. LWD goes true when the last data character is placed on the interface lines.

FORMATTER ENABLE

FEN Level J1A4/B4

When false, this level causes all formatters in the system to revert to the quiescent state. This line may be used to disable the formatters if controller power is lost or to clear formatter logic when illegal commands or unusual conditions occur.

WRITE DATA PARITY & WRITE DATA LINES

WP, W0-W7 Levels (Refer to pin list)

These lines are present in both NRZI and PE formatters and will be defined for each application.

(1) NRZI Formatter

These 9 lines transmit write data from the controller to the formatter. Lines WP, W0-W7 are utilized for 9-channel operation; lines WP, W2-W7 are used for 7-channel operation.

For 9-channel operation the 8 data bits appearing on W0-W7 are written onto the corresponding channels on tape; for 7-channel operation W0 and W1 are not utilized and the remaining 6 data bits are written onto tape. In either case, W7 corresponds to the least significant bit of the character.

Line WP is optional and is utilized only if it is required to write the parity bit specified by the customer. When this option is not employed the formatter generates parity internally on the basis of data contained on W0-W7, together with the current parity mode.

The first character of a record should be available on these lines within one character period after DBY goes true and remain until the trailing edge of the first WSTR is issued by the formatter.

The next character of information must then be placed on these lines within one-half of a character period.

Subsequent characters of a record are processed in this manner until LWD is set true by the controller when the last character is transmitted.

(2) PE Formatter

The 8 write data lines (9 in the case of external parity option) are utilized to transmit write data from the controller to the formatter. W0 corresponds to the most significant bit and W7 to the least significant bit of each character.

The first character of a record should be available on these lines less than 40 character periods after DBY goes true and remain until the trailing edge of the first WSTR is issued by the formatter. The next character of information must then be placed on these lines within one-half of a character period.

Subsequent characters of a record are processed in this manner until LWD is set true by the controller when the last character is transmitted.

2.3 INTERFACE OUTPUTS
(Formatter to Controller)

The 7 track interface output signal is used exclusively in the NRZI formatter; all other interface outputs are common to both NRZI and PE formatters. Pin A33/B33 outputs the CHECK CHARACTER GATE from NRZI formatters or the IDENTIFICATION from PE formatters. The controller must allow for this signal when combination NRZI/PE formatters are used. All pulsewidths must be 1 microsecond wide (min).

FORMATTER BUSY

FBY Level J1-A34/B34

When true, this level inhibits further commands to the formatter. The level goes true on the trailing edge of GO when a command is issued by the controller. FBY will remain true until tape motion ceases.

DATA BUSY

DBY Level J1-A35/B35

This level goes true when the tape is up to speed, has traversed the PBG, and the formatter is about to write data or look for a read signal on the tape. DBY remains true until data transfer is completed and the appropriate post record delay is completed. DBY goes false when the capstan starts to decelerate the tape.

HARD ERROR

HER Pulse J1-A37/B37

When true, this pulse indicates a read error. This line will be true during read operations when one or more of the following occurs:

(1) Longitudinal parity error
(2) Improper record format
(3) CRCC parity error
(4) Vertical parity error on a data character

In all cases except a vertical parity error, HER will be pulsed after the complete record has been read. In the case of a vertical parity error, the HER line will be pulsed when a read strobe (RSTR) pulse is issued for the character in error. DBY goes false after all error information has been transferred to the controller.

CORRECTED ERROR

CER Pulse J1-A38/B38
(PE Mode Only)

When true, this pulse indicates that a single track dropout has been detected and the formatter is performing an error correction.

HARD ERROR

HER Pulse J1-A37/B37
(PE Mode)

When true, this pulse indicates that an uncorrectable read error has occurred and that the record should either be reread or rewritten. Here is a table illustrating the possible HER/CER signal combinations, together with their meaning:

SIGNAL STATES

HER	CER		
0	0	=	No Errors Detected
0	1	=	Single Channel Error
1	0	=	Postamble or VRC ERROR Only All Channels Believed Good
1	1	=	Multiple Channel Errors or: Excessive Skew or: Single Channel Failure w/Postamble VRC Error

This timing chart illustrates the HER/CER minimum pulse widths at various tape speeds:

HER/CER

2 msec min (12.5 ips)
1 msec min (25 ips)
0.67 msec min (37.5 ips)

CHECK CHARACTER GATE

CCG Level J1-A33/B33
(NRZI mode only)

This level is set true by the NRZI formatter when the read information being transmitted to the controller is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). When data characters are transmitted, CCG goes false. Data and check information can be distinguished by gating READ STROBE (RSTR) with CCG or its inverse.

IDENTIFICATION

IDENT Level J1-A33/B33
(PE Mode)

When true, this level identifies PE tapes. PE tapes are detectable in the read forward mode by the presence of an identification burst on the parity channel.

FILE MARK

FMK Pulse J1-A36/B26

File mark is pulsed when a file mark is detected on the tape during a read operation or during a write file mark operation in a read-after-write transport. The FMK line will be pulsed after a complete file mark record has been read. Error conditions should be ignored when a file mark is detected.

TRANSPORT STATUS AND CONFIGURATION LINES

These lines indicate the status and configuration of the selected transport to the controller after being gated with the formatter address signal, FAD. The low true transport status lines are: READY (RDY), ON LINE (ONL), REWINDING (RWD), FILE PROTECT (FPT), LOAD POINT (LP), and END OF TAPE (EOT).

Transport configuration lines are $\overline{\text{NRZ}}$/PE, $\overline{\text{7TK}}$/9TK and LOW/HIGH.

WRITE STROBE

WSTR Pulse J1-A39/B39

This line consists of a pulse for each character of read information to be transmitted to the controller. These signals should be used to sample the read data lines RDP, RD0-RD7.

In NRZI formatters, the transmission of CRC and LRC data characters will be flagged by the check character gate (CCG) signal as described under HARD ERROR (HER).

READ DATA LINES

RP, R0-R7 Levels (See pin list)

In the NRZI formatter, RP and R0-R7 are utilized for 9 channel operation; lines RP and R2-R7 are utilized for 7 channel operation. In PE formatters the 9 PE channels are assigned to RP, R0-R7.

Each character read from tape is made available by parallel sampling the read lines with READ STROBE. Since the data remains on the read data lines for a full character period, the corresponding RSTR pulses are timed to occur after approximately the center of the character period.

2.4 INTERFACE CABLING REQUIREMENTS

The cables connecting the Format Control Unit to the tape transports are normally supplied with the system, and so are the cable connectors that mate with the card edge connectors on the units required for the interface cabling. The intercabling requirements are the same for NRZI or the dual density NRZI/phase encoded systems.

Twisted pair cabling should be used to reduce intercable crosstalk. All wires should be 24 AWG, minimum, with a minimum insulation thickness of 0.1 inch. Each pair should have not less than one twist per inch, and maximum cable length should not exceed 20 feet.

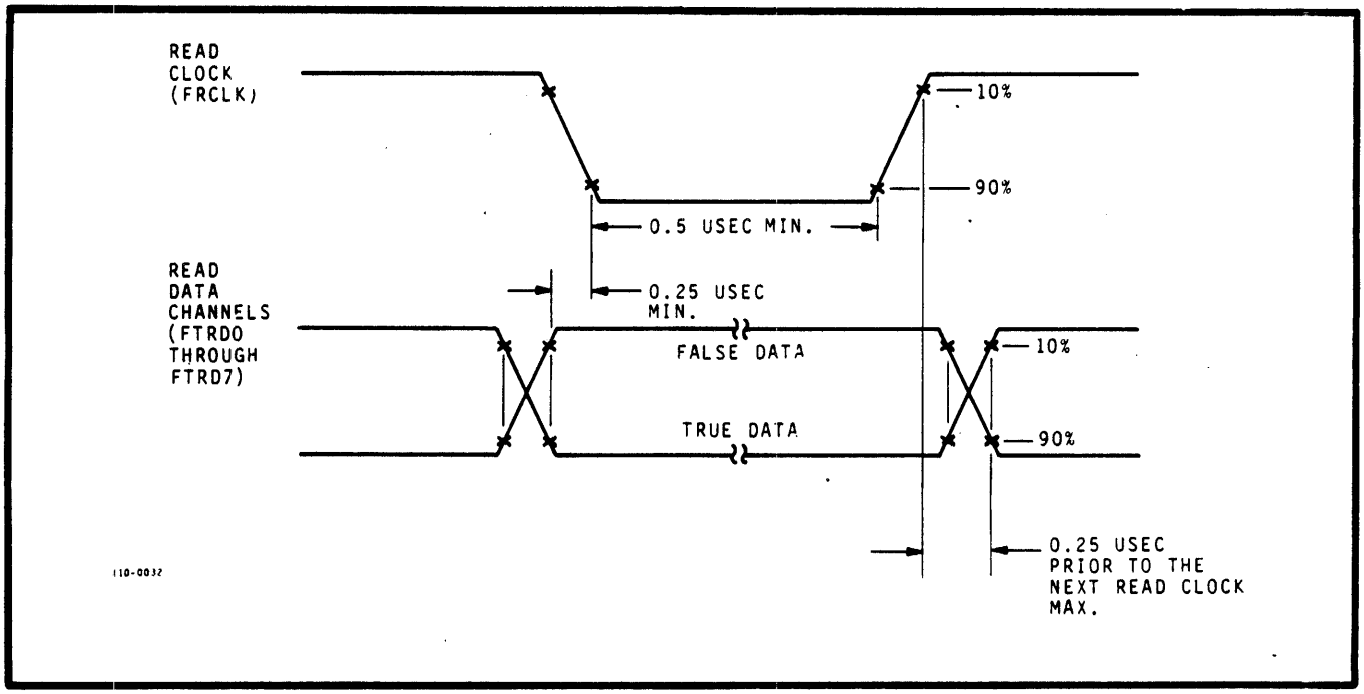
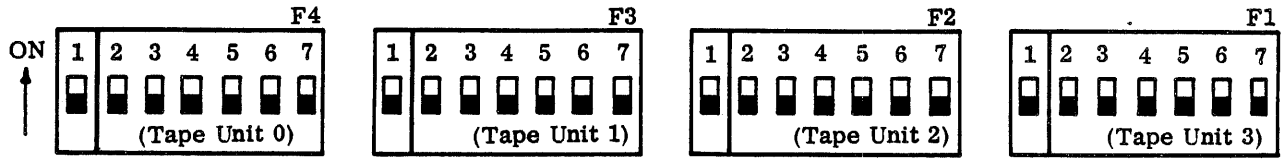


Figure 2-2 Read Data Timing



OPTION SETTINGS[1]

F1-1 ON/F2-1 OFF selects Formatter Address 0 (FAD0)

F1-1 OFF/F2-1 ON selects Formatter Address 1 (FAD1)

F3-1 ON/F4-1 OFF: Selected Tape Unit writes externally generated parity.

F3-1 OFF/F4-1 ON: Selected Tape Unit writes internally generated parity.

DENSITY SELECTION (ON = ✱)

	S2	S3
9 Track 800, 1600[2] CPI		✱
7 Track 556, 800 CPI	✱	
7 Track 200, 556 CPI	✱	✱

	S4
1600 CPI low speed select	✱
1600 CPI high speed select	

SPEED SELECTION (ON = ✱)

		S5	S6	S7
NOT AVAILABLE IN 125 IPS MODELS	10 IPS (125 IPS)	✱	✱	✱
	12.5 IPS		✱	✱
	15 IPS	✱		✱
	18.75 IPS			✱
	25 IPS	✱	✱	
	37.5 IPS		✱	
	45 IPS	✱		
	75 IPS			

NOTES

[1] F1-S1 is reserved.

[2] 1600 cpi density requires PE read recovery board.

Table 2-2 Option, Speed and Density Settings
IC's F1 through F4 located on 4831 Interface Board

2.5 OPTIONS (SPEED AND DENSITY SELECTION)
(Refer to Table 2-1)

Tape speed and density as well as certain options are controlled by means of F1 through F4 on the interface board. Tape unit 0 is controlled by F4; tape unit 1 is controlled by F3, etc.

The options are selectable by switches S1 on F1 through F4. Switches S1 on ICs F1 and F2 determine whether formatter 0 or 1 is addressed. The positions of F3-1 and F4-1 determine whether internal or external parity is written on tape. Switches S2 through S7 on F1 through F4 supply tape unit commands and status signals to and from the individual tape units. Switch S2 on F1 through F4 is turned ON to select a 7 track tape unit, OFF to select a 9 track tape unit.

Switch S3 selects between 556/800 cpi and 200/556 cpi tape densities for 7 track tape units.

Switch S4 is reserved for PE applications and selects between a preset high or low tape speed. Since the PE board can only operate at two speeds, the formatter must be set up so that only two tape speeds are selectable at 1600 cpi. NRZI units have no such limitations.

Switches 5 through 7 can be set to various binary combinations for tape speed selection. Tape speeds possible are: 10 ips, 12.5 ips, 18.75 ips, 25 ips, 37.5 ips, 45 ips and 75 ips.

2.6 DAISYCHAINING

The Model 9219 formatter can be connected to as many as four tape transports of varying tape speeds and character densities.

To connect the Model 9219 to Model 9000 transports, order one 190-4999-001 cable, one 190-4679-001 control adapter and one 190-4479-001 data adapter per transport. Figure 2-3 illustrates the daisychain connection. Note that the 3860 Data Terminator and the 3841 Control Terminator cards are only installed in the last deck of the daisychain.

To connect the Model 9219 to 9100, 9300, 9700 and/or 9800 tape transports, order one 190-4747-001 adapter board per transport and two 190-4999-NLL cables. (When ordering, substitute the number of transports in the daisychain for N; and the total cable length in feet for LL. Twenty feet is the maximum length available.) Figure 2-4 illustrates the daisychain connection. As in Model 9000 daisychain installations, the 3860 Data Terminator and the 3841 Control Terminator cards are installed in the last deck of the chain only. The 4747 adapter board contains a tape unit address select switch. Thus, each deck in the chain can be assigned an address. (SW1 on = tape unit 1 on; SW2 on = tape unit 2 on, etc). The tape unit address can also be controlled by the address select switch on the front panel of each transport. In this instance, all address switches on the adapter boards should be in the OFF position. A 190-4910-001 cable is used to connect the tape unit address switch to the 4747 adapter board.

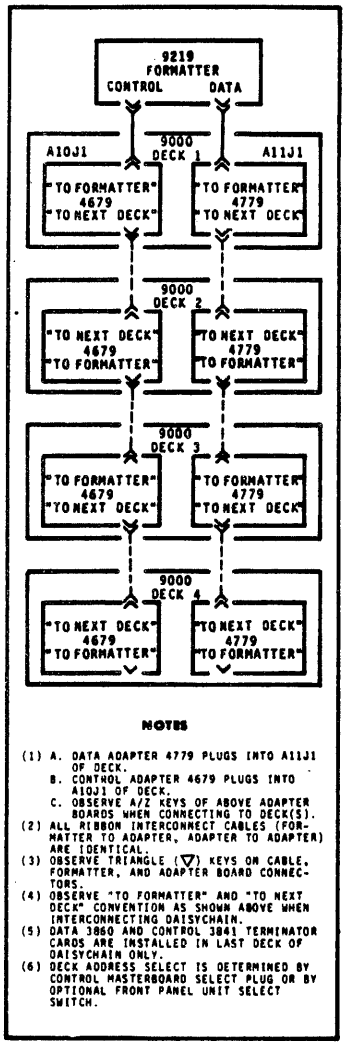


Figure 2-3 Daisychain Connection-9219 to 9000 Transports

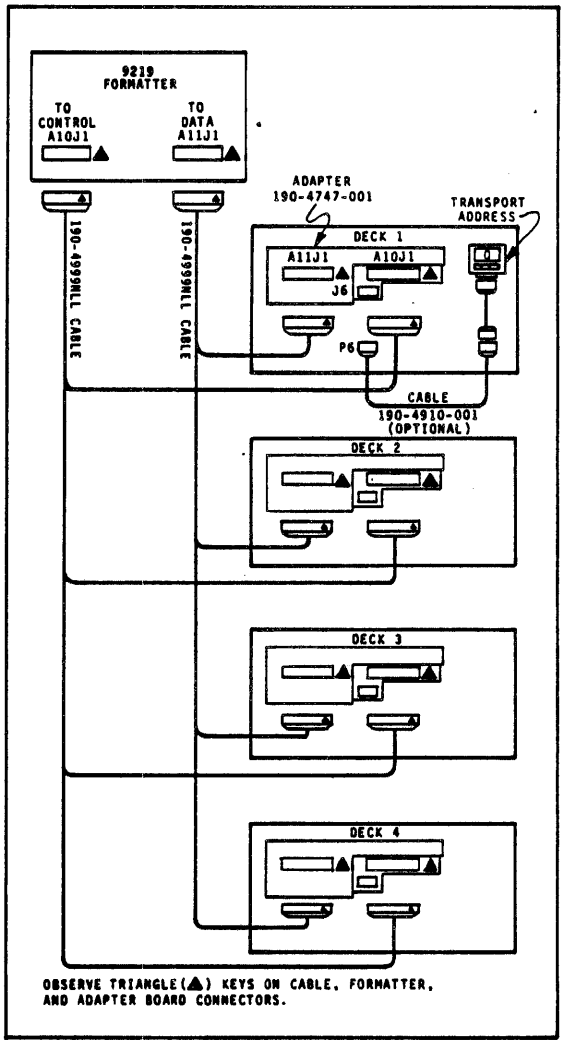


Figure 2-4 Daisychain Connection-9219 to 9100,9300,9700,9800 Transports

J1, Model 9219 Formatter, Mates with P1 from Controller

PIN	MNEMONIC	SIGNAL	IN/OUT
A1/B1	FAD	Formatter Address	IN
A2/B2	OFL	Offline Command	IN
A3/B3	REW	Rewind	IN
A4/B4	FEN	Formatter Enable	IN
A5/B5	GO	Initiate Command	IN
A6/B6	REV	Reverse/Forward	IN
A7/B7	WRT	Write/Read	IN
A8/B8	WFM	Write File Mark	IN
A9/B9	EDIT	Edit	IN
A10/B10	ERASE	Erase	IN
A11/B11	DEN	Density Select (Note 1)	IN
A12/B12	PAR	Parity Select (Note 1)	IN
A13/B13	LWD	Last Word	IN
A14/B14	WP	Write Data Parity	IN
A15/B15	W0	Write Data 0	IN
A16/B16	W1	Write Data 1	IN
A17/B17	W2	Write Data 2	IN
A18/B18	W3	Write Data 3	IN
A19/B19	W4	Write Data 4	IN
A20/B20	W5	Write Data 5	IN
A21/B21	W6	Write Data 6	IN
A22/B22	W7	Write Data 7	IN
A23/B23	TAD1	Transport Address 1	IN
A24/B24	TAD0	Transport Address 0	IN
A25/B25	RDY	Ready	OUT
A26/B26	ONL	On Line	OUT
A27/B27	RWD	Rewinding	OUT
A28/B28	LOP	Load Point	OUT
A29/B29	EOT	End of Tape	OUT

Table 2-3 Interface Pin List

J1, Model 9219 Formatter, Mates with P1 from Controller

(Continued)

PIN	MNEMONIC	SIGNAL	IN/OUT
A30/B30	FPT	File Protect	OUT
A31/B31	NRZ	NRZI	OUT
A32/B32	7TRK	7 Track/9 Track	OUT
A33/B33	IDENT/CCG	Identification/Check Character Gate (Note 2)	OUT
A34/B34	FBY	Formatter Busy	OUT
A35/B35	DBY	Data Busy	OUT
A36/B36	FMK	File Mark	OUT
A37/B37	HER	Hard Error	OUT
A38/B38	CER	Corrected Error	OUT
A39/B39	WRST	Write Strobe	OUT
A40/B40	RSTR	Read Strobe	OUT
A41/B41	RP	Read Data Channel P	OUT
A42/B42	R0	Read Data Channel 0	OUT
A43/B43	R1	Read Data Channel 1	OUT
A44/B44	R2	Read Data Channel 2	OUT
A45/B45	R3	Read Data Channel 3	OUT
A46/B46	R4	Read Data Channel 4	OUT
A47/B47	R5	Read Data Channel 5	OUT
A48/B48	R6	Read Data Channel 6	OUT
A49/B49	R7	Read Data Channel 7	OUT

NOTE 1: Used in NRZI configurations only.
NOTE 2: Used in NRZI/PE configurations only.

Control Connector, Model 9219 Formatter
Mates with 190-4999-XXX Control Cable

PIN SIG/GRD	MNEMONIC	SIGNAL	IN/OUT
1/2	SEL3	Tape Address Select 3	OUT
3/4	SEL2	Tape Address Select 2	OUT
5/6	SEL1	Tape Address Select 1	OUT
7/8	SEL0	Tape Address Select 0	OUT
9/10	RNG	Tape Running	IN
11/12	EOT	End of Tape	IN
13/14	RDY	Ready	IN
15/16		Not Used	
17/18	LDP	Load Point	IN
19/20	FPT	File Protect	IN
21/22	RWD	Rewind	OUT
23/24		Not Used	
25/26		Not Used	
27/28		Not Used	
29/ 30	ONL	Online	
31/32	OFFC	Offline Command	OUT
33/34	SWS	Set Write Status	OUT
35/36	SEL	Tape Unit Select	OUT
37/38	RWC	Rewind Command	OUT
39/40	HDI	High Density Indicator	IN
41/42	SRC	Synchronous Reverse Command	OUT
43/44	HDS	High Density Status	OUT
45/46	SFC	Synchronous Forward Command	OUT
47/48	OVW	Overwrite	OUT

Data Connector, Model 9219 Formatter
Mates with 190-4999-XXX Data Cable

PIN SIG/GRD	MNEMONIC	SIGNAL	IN/OUT
1/2	RDS	Read Data Strobe	IN
3/4	RDP	Read Data Channel P	IN
5/6	RD0	Read Data Channel O	IN
7/8	RD1	Read Data Channel 1	IN
9/10	RD2	Read Data Channel 2	IN
11/12	RD3	Read Data Channel 3	IN
13/14	RD4	Read Data Channel 4	IN
15/16	RD5	Read Data Channel 5	IN
17/18	RD6	Read Data Channel 6	IN
19/20	RD7	Read Data Channel 7	IN
21/22	RGAP	Read Gap Detect	IN
23/24		Not Used	
25/26		Not Used	
27/28		Not Used	
29/30	WDS	Write Data Strobe	OUT
31/32	WARS	Write Amplifier Reset Strobe	OUT
33/34	WDP	Write Data Channel P	OUT
35/36	WD0	Write Data Channel O	OUT
37/38	WD1	Write Data Channel 1	OUT
39/40	WD2	Write Data Channel 2	OUT
41/42	WD3	Write Data Channel 3	OUT
43/44	WD4	Write Data Channel 4	OUT
45/46	WD5	Write Data Channel 5	OUT
47/48	WD6	Write Data Channel 6	OUT
49/50	WD7	Write Data Channel 7	OUT

THEORY OF OPERATION

3.1 GENERAL

The Model 9219 Formatter consists of a microprocessor, an interface board, a masterboard and an optional PE read board required for phase encoded data applications. The one-to-one circuitry configuration of the masterboard makes all tape deck I/O signals available to these boards at the same relative pin positions.

The interface board adapts the Model 9219 to the Pertec controller. All read and write data, computer commands, and tape transport status signals pass through this board. Most tape transport status signals enter the interface board from the masterboard, while write data and computer commands are input on interface board connector J2. Interface board connector J1 outputs read data and transport status signals to the controller.

The microprocessor board is connected to the interface board, the tape unit(s) and the controller through the masterboard. It is capable of driving and selecting tape decks, outputting commands to tape decks and reading status from tape decks. (In normal configurations the interface board selects tape transports, although the microprocessor board may be modified to do this.) In certain applications where responses must be immediate, the microprocessor may be bypassed, or it may look at tape deck signals simultaneously with other formatter boards.

The microprocessor reads and writes at an internally determined data rate which is selectable from 10 to 75 ips in any one of five formats. For seven track tape decks, selectable densities are 200/556 cpi or 556/800 cpi. For nine track machines, 800 or 1600 cpi densities may be selected. The only limitation is that no more than two tape speeds are selectable at 1600 cpi. Selectable speeds include: 10 ips, 12.5 ips, 15 ips, 18.75 ips, 25 ips, 37.5 ips, 45 ips, and 75 ips.

Speed selection, density and certain other options are controlled by switches E1 through E4 on the interface board. (See Table 2-6 for IC switch settings).

3.2 TYPE 4632/4832 MICROPROCESSOR BOARD

This board is microprogramed to control data, transport command and transport status flow between the selected tape transport and the controller. All inputs and outputs to the microprocessor board are made through the A and B busses of the masterboard. Tables 4-1A and 4-1B in the maintenance section list all masterboard connections. The maintenance section also contains the basic, NRZI, and PE programs for the formatter. (The program sequence begins on the basic flow chart, then branches to either the NRZI or PE flow chart, depending on formatter type and recording density.)

The major functional components of the board include: six bipolar Shottky 3002 Central Processing Elements (CPEs), one 3001 Microprogram Control Unit (MCU) and, depending on formatter application, 8 or 16 3601 Programable Read Only Memories (PROMs). Figure 3-1 is a block diagram showing the interrelationship between these major functional elements.

3.2.1 The 3002 Central Processing Elements

There are six of these devices per microprocessor board and all of their input control lines are parallel connected. The Central Processing Elements, or CPEs, are controlled by part of a 32 bit microinstruction word which is output from the programable read only memories during one microinstruction cycle. (Refer to Figure 3.2.) Seven bits of this microinstruction word are output on bus lines F0-F6, the microfunction bus. The F bus controls the six CPEs, but its commands can be altered by the 12 bit K, or masking, bus. This bus can modify the F bus commands by selecting or deselecting the Arithmetic Logic Units (ALUs) within the six CPEs. In fact, the K bus expands the number of functions which may be performed by this masking action.

The remaining 13 bits of the 32 bit microinstruction word are routed back to the 3001 Microprogram Control Unit (MCU). The function of these bits will be discussed under the paragraph entitled 3001 Microprogram Control Unit.

Each central processing element has two input busses, designated I and M, and two output busses, termed D and A. The I bus inputs tape transport commands from the computer and tape transport status information from the selected tape drive. The M bus inputs read or write data to the central processing elements. Since data and command signals are multiplexed on these I/O bus lines, an enabling command is output from the CM and CD busses to select the appropriate signals at a particular point in the formatter program. These commands will be discussed shortly.

Output bus lines A8 through A11 make up the Next Column Address Bus. These lines are connected through quad D flip-flop C9 to the PX4-PX7 inputs on the microprogram control unit (MCU). Data on these

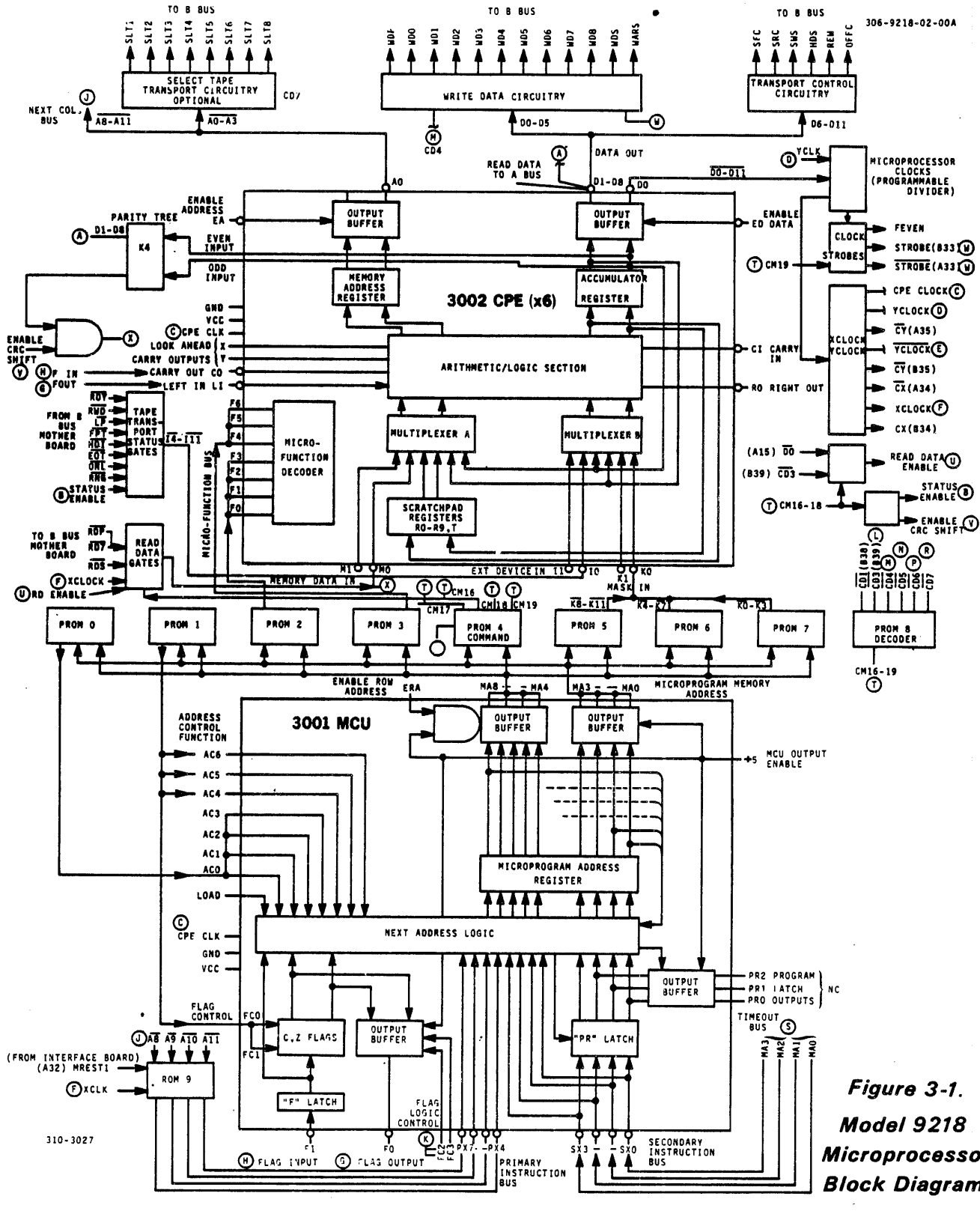


Figure 3-1. Model 9218 Microprocessor, Block Diagram

lines is tested by the MCU to determine the next column address it will output to the PROMs during a JPX (Jump Instruction) command, which will be explained later. Bus lines A0 through A3 are the tape transport select bus. However, since tape transport selection is normally performed by the controller, these lines are not used in the standard 9218 formatter configuration. Bus lines A4 through A7 are unused.

Bus lines D0 through D8 transfer read or write data to the interface. (Write data is clocked out of D latches J7-J8 on the microprocessor to the B bus of the masterboard; read data is transferred through the A bus of the masterboard to the 4831 Interface board.) Bus lines $\overline{D0}$ through $\overline{D8}$, the complements of the D0 through D8 bus lines, load four bit binary counters F7, F8, F9, which determine the read or write data rate. D bus data is also checked for proper parity by parity tree IC K4 and exclusive-OR gates E7.

3.2.2 Command Bus CM16, CM17, CM18

As can be seen, read or write data and tape transport status and command signals are applied to common I/O buses at the CPEs. To organize and synchronize read and write data and the tape transport status and command signals, PROM pair 4 has been programed to output commands 0 through 7 in hex code on command lines CM 16, 17 and 18. Line CM 18 outputs the most significant bit; CM 16 outputs the least significant bit. Additionally, during most command times, a corresponding pulse (CD1-7) is given to enable the appropriate D latches AND/OR gates. Commands 0, 1 and 3 select and transfer data to and from the interface. Commands 2,4,5,6,7 and 8 control the operation of the microprocessor board. Table 3-1 illustrates the bits present on the significant bus lines during a given command time.

Command 0 (0 states on CM 16, 17 and 18) places any available write data on M bus lines 0-8. It also places the selected transport's speed, bit density, parity and the FBY line on the I input bus. This is the normal microprocessor situation until another command is issued.

Command 1 transfers read data out of the CPEs to the interface on D bus lines D0-D8. These lines are input to type D flip-flops B8/B9 on the 4831 Interface board, where they are clocked out on each succeeding read data strobe. Command 1 would necessarily be preceded by command 5, which inputs read data into the M bus of the CPEs for processing.

Command 2 places status information from the selected tape transport on the CPE's I input bus. Command 2 also enables ENABLE CRC SHIFT, which transfers the parity of the least significant nine bits contained in the CPE internal accumulators through the $\overline{D}$ bus onto line 9 of the M input bus. This performs a partial VRC and CRC parity check, reducing the number of instructions required for parity checking later. Incidentally, IC K4 checks parity, while the exclusive-OR gates E7 generate the IBM-compatible CRC character.

Command 3 enables NAND gates F3/H3/H4, applying one read data byte to the M input bus of the CPEs. These NAND gates are connected to the Q outputs of D latches H1/H2, which are clocked by a read data strobe pulse and cleared by a CD5 pulse issued during command 5 time. Thus, CD3 and CD5 must both be true before read data can be input to the central processing elements.

Command 4 parallel-loads write data channels WP through W7 onto CPE output lines D0-D8. It is passed through D latches J7/J8 and out to the tape transport. The WDS and WARS lines are also enabled to insure proper write data timing.

Command 5 transfers one byte of read data onto M input bus lines 0-8 of the CPEs after command 3 is issued. In PE formatters, command 5 also transfers PE read data status information onto I bus lines I0 through I11. If a read data character is present during command 5 time, a carryout is generated from the CPE and applied to the F IN input to the 3001 Microprogram Control Unit. This generates CD5 true from PROM pair 4, clearing D latches H1/H2 and enabling the read data bus to respond to the next read clock. If no read characters are present FIN would be false and the D latches would not be cleared. The read bus is not cleared until command 5 occurs and a carryout exists in the microprocessor. However, read data still won't pass to the controller until command 1 has been issued.

Command 6 parallel loads a programable counter with the bit complement of the D bus. The clock defines the read or write data rate. (Refer to ICs H7, H9, F7, F8, F9 et al on the first page of the microprocessor schematic.) This assures even multiples of tape speeds and results in accurate alignment between tape speed and recording density. The cycle time of the programable counter is 6944x (accumulator +1) microsecond. The number of instructions executed per microinstruction cycle time is defined by the cycle's microinstruction count. This is equal to two times the microinstruction +2. If a hexidecimal 008 were output from the accumulator bus, for example, and command 6 is issued, the number of instructions executed per cycle time would be 2x8+2, or 18. The maximum cycle instruction count is 8192 instructions per cycle time and the minimum cycle instruction count is 4. The 1.02 microsecond STROBE and $\overline{\text{STROBE}}$ pulses are also produced, which are used to develop the WDS and WARS strobe pulses.

In standard formatter configurations, command 7 clocks Hex D flip-flop J6, passing tape transport command(s) available on the A and D busses to the selected tape transport. Commands include: SFC, SRC, SWS, HDS, REW and OFFC. In special formatter configurations, such as buffered tape transports where tape drive selection should be made

COMMAND 0, 1
(Interface Board Data to Microprocessor Board)

I BUS*

11	10	9	8	7	6	5	4	3	2	1	0
0	MSB ← COMMAND → LSB			← SPEED →			PE HIGH SPEED	← DENSITY →		0	BUSY

COMMAND HEXIDECIMAL CODE
- 7 - ERASE VAR
- 6 - ERASE FIXED
- 5 - WFM
- 4 - WRITE EDIT
- 3 - WRITE
- 2 - BACKSPACE EDIT
- 1 - BACKSPACE
- 0 - READ

*When Interface Board is enabled

When D11 = 1: (Read Data, Read Strobe, Hard Error to Controller)

D BUS

11	10	9	8	7	6	5	4	3	2	1	0
1	X	HER	RP	R0	R1	R2	R3	R4	R5	R6	R7

When D11 = 0: (Formatter Status to Controller)

D BUS

11	10	9	8	7	6	5	4	3	2	1	0
0	X	X	IDENT	FBY	DBY	FMK	HER	CER	X	X	X

COMMAND 2

I BUS

11	10	9	8	7	6	5	4	3	2	1	0
RDY	RWD	LDP	FPT	HDI	EOT	ONL	RNG	0	0	0	0

MTU STATUS

M BUS
(Before Enable)

11	10	9	8	7	6	5	4	3	2	1	0
0	0	ODD PARITY BIT	D0	D8	D7	D6⊕D0	D5⊕D0	D4⊕D0	D3⊕D0	D2	D1

M BUS
(After Enabling)

11	10	9	8	7	6	5	4	3	2	1	0
$\overline{LWD}$	0	0	P	0	← WRITE DATA →						
					1	2	3	4	5	6	7

COMMAND 3

D BUS

11	10	9	8	7	6	5	4	3	2	1	0
0 CORR ENAB	PE HIGH SPEED	SEL WRT DATA	FWD	X	X	X	X	0	0	1	ENB READ
TO PE CARD								ENABLES INTERFACE CARD			PE CARD

When D0 = 1: PE Read Card Enabled
When D0 = 0: Interface Card Enabled

Table 3-1A. Command Time Bus Assignments

COMMAND 4
(Microprocessor Card)

D BUS

11	10	9	8	7	6	5	4	3	2	1	0
STRB	0	0	P	0	1	2	3	4	5	6	7

WRITE DATA

WRITE TOGGLES

0 = WDS
1 = WARS

COMMAND 5
*(When Enabled)

CM5 ON UP CARD (NRZI Mode)

M BUS

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	P	0	1	2	3	4	5	6	7

READ DATA

FROM MAG TAPE (FOR NRZI)

CM5 ON PE CARD Microprocessor Board

*I BUS
(PE Mode)

11	10	9	8	7	6	5	4	3	2	1	0
CORR ENAB	BLOCK	D3	FWD SEL	POST DET	1	FM	SKEW	ST ERR	MT ERR	POST ERR	CRC ERR

When D11 = 1:

*M BUS
(PE Mode)

11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	RP	R0	R1	R2	R3	R4	R5	R6	R7

READ DATA

When D11 = 0:

M BUS

11	10	9	8	7	6	5	4	3	2	1	0
0	BLOCK	DE3	P	0	1	2	3	4	5	6	7

ENVELOPES

*WHEN ENABLED
CD3 D0

COMMAND 6

D BUS

11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X

CD6 on Microprocessor Board Loads Contents of $\overline{D11}$ - $\overline{D0}$ into Programable Counter H7/H9/F7/F8/F9.

COMMAND 7

Outputs Transport Commands to Selected Tape Transport

D BUS

11	10	9	8	7	6	5	4	3	2	1	0
SFC	SRC	WSW	HPS	RWC	OFFC	0	0	0	0	0	0

Table 3-1B Command Time Bus Assignments

directly from the formatter, command 7 also enables one of eight transport select signals, SLT1 through SLT8. J5 and K5, the ICs from which these signals would be output, are omitted from standard microprocessor boards.

3.2.3 Time Out Cycle

The microprocessor's clock circuitry includes a programable divider which enables an interrupt. This interrupt permits the microprocessor to test for a time-out cycle while simultaneously executing the next instruction. If a time out is detected, the processor may be forced to branch, i.e., line AC0 will be forced low, and the next location in the memory address register would be an even row or column. Thus the microprocessor can very quickly ascertain whether it should sample the write data registers to determine whether data should be transferred to the formatter, or perform other time-dependent functions.

3.2.4 The 3001 Microprogram Control Unit (MCU)

Through its MA address lines, the 3001 chip determines the microinstruction sequence output to the central processing elements from the programable read only memories. Eleven bits of the microinstruction word output by the PROMs are returned to the 3001 MCU for next address (AC0-AC6) and jump function (FC0-FC3) control. The MA bus lines provide a row and column address to the PROMs, which employ memory matrixes for storing the individual microinstruction word bits. Lines MA0-3 specify the column address; MA4-8 specify the row address. Each PROM matrix can contain up to 32 row addresses and 16 column addresses for a total of 512 microinstruction addresses.

The next address logic in the 3001 MCU makes extensive use of this addressing scheme. For example, from a particular row or address it is possible to jump either unconditionally to any other location in a particular row or column, or conditionally to other specified locations in one operation. For a given address matrix location, there is a fixed subset of microprogram addresses that may be selected as the next address. These are referred to as a jump set and each type of microprogram control unit address control jump function has its associated jump set.

The MCU's jump function logic actually determines the sequence in which microinstruction words are accessed from the microprogram memory by controlling the next address logic within the 3001 MCU. The program memory address is held in the Microprogram Address Register (MAR).

The next address is also influenced by data on bus lines F0-F4. Through flag output line F0, the C and Z flags within the 3001 MCU latch and control the value of the carry and shift inputs to the central processing elements. Under microprogram control the flag logic simultaneously forces the state of this flag output line to 1 or 0 or the value of the C and Z flags in the MCU.

3.2.5 The PROMs

Depending on whether it's a NRZI or NRZI/PE application, there are 8 or 16 socket-connected 3601 PROMs in the microprocessor. They are bipolar Shottky with a 50 nsec access time. Each PROM is 4 x 256, or 256 locations of 4 bits each, and each PROM is specifically programed for use in the Model 9218. The 256 bit locations require lines of addressing (MA bus lines 0-8). The PROMs are paired and parallel-connected. The outputs are common and the chips are wired to have common addresses which are alternately enabled or disabled so that only one chip of a pair operates at any given time. This arrangement can provide up to 512, 32 bit programing words for use in the formatter. However, in applications requiring 256 or less program words, NRZI-only machines for example, one set of PROMs may be omitted. The PROMs output a 32 bit wide microinstruction word during one microinstruction cycle. Here is a breakdown of PROM functions:

PROMs 0 AND 1
(ICs A7, A8, A10, A11)

Output the microinstruction bits which help define the next instruction to the output from the 3001 MCU. These are input on lines AC0-AC6 of the 3001 chip (A12). PROM 0 contains the least significant bits (A0-A3); PROM 1 contains the most significant bits (A4-A6). PROM 1 also outputs FC0-FC1, which control the flags influencing the MCU's next address logic. A true condition on this line results in a conditional branch in the program.

PROM 2
(ICs A5, A6)

Contains the least significant bits of the CPE's microfunction bus. These bits are found on lines F0-F3.

PROM 3
(ICs B7, B8)

Outputs the most significant microfunctions which are on lines F4-F6. PROM 3 also contains a flag control which sets an outgoing carry fed to the 3001 microprocessor. This is F IN, which is transmitted on A12, line 17. FC 3 (A12, pins 12 and 13) controls the holding of an internal storage state in the 3001 chip.

PROM 4
(ICs A2, A3)

Outputs the command bus (CM16, 17 and 18). It also contains CM19 which controls the timing interrupt bit. When true, the interrupt count will be tested to determine whether a timeout has occurred. If it has, AC0 will be forced to 0, causing an unconditional program branch.

PROM 5
(ICs, B10, B11)

Outputs the most significant four bits of the K (masking) bus.

PROM 6
(ICs B5, B6)

Outputs the middle four bits of the K bus.

PROM 7
(ICs B2, B3)

Outputs the least significant four bits of the K bus.

3.3 THE INTERFACE BOARD

All signal flow between the computer, the tape transports and the microprocessor board is processed through this card. The two pages of the interface card schematic can be divided into several functional blocks — Tape Speed/Density Select Switch, Tape Transport Status Gates, Read Data Logic, Address Select Gates, Write Data Gates, and Command Logic, etc.

3.3.1 Tape Speed/Density Select Switches

Tape speed and density as well as certain options are controlled by means of E1 through E4 on the interface board. Tape unit 0 is controlled by E4; tape unit 1 is controlled by E3, etc.

The options are selectable by switches S1 on E1 through E4. Switches S1 on ICs E1 and E2 determine whether formatter 0 or 1 is addressed. The positions of E3-1 and E4-1 determine whether internal or external parity is written on tape. Switches S2 through S7 on E1 through E4 supply tape unit commands and status signals to and from the individual tape units. Switch positions of S2 through S7 are directed to the the microprocessor on corresponding I bus lines I2 through I7. Switch S2 on E1 through E4 is turned ON to select a 7 track tape unit; OFF to select a 9 track tape unit.

Switch S3 selects between 556/800 cpi and 200/556 cpi tape densities for 7 track tape units.

Switch S4 is reserved for PE applications and selects between a preset high or low tape speed. Since the PE board can only operate at two speeds, the formatter must be set up so that only two tape speeds are selectable at 1600 cpi. NRZ1 units have no such limitations.

Switches 5 through 7 can be set to various binary combinations for tape speed selection. Tape speeds possible are: 10 ips, 12.5 ips, 15 ips, 18.75 ips, 25 ips, 37.5 ips, 45 ips and 75 ips.

3.3.2 Tape Transport Status Gates

Tape transport status signals are input to the interface board on the B bus of the motherboard; then gated with FORMATTER ADDRESS and directed to the controller at interface board jack J1. Formatter Address 1 (FAD 1) must be selected (i.e., E2-1 ON/E1-1 OFF) to enable the NAND gates controlling the tape transport status signals. These signals are: High Density Indicator, File Protect, End of Tape, Load Point, Rewind, On Line and Ready.

3.3.3 Read Data Logic

Read data channels P through 7 are assigned to the D output bus of the microprocessor and directed to D latches B8 and B9 on the interface board. They are clocked out to the computer during command 1 (CD1) time when pulses from D11 fire one shot C7. (This one shot also provides the necessary timing delay for the read strobe (RSTR) which is output at J1-31.)

The read data of the D bus is also directed to D latch B5, which outputs any available CER and HER read error signals, as well as IDENT/CCG during command 1 time.

CHECK CHARACTER GATE is set true by a NRZI formatter when the read information contains a CRCC or LRCC check character. The HARD ERROR true signal can either be a pulse or a level. NAND gate B7 will pass a HER true pulse during the read strobe when there is a vertical parity error.

DATA BUSY false will clear D latches B9 and B8 to stop read data transmission when tape speed starts to decelerate. Similarly, INITIALIZE true clears D latch B5.

3.3.4 Address Select

The states of controller signals TAD0 and TAD1 determine which transport is selected. The selected tape deck is addressed through the B bus of the formatter motherboard (B24 through B27). Here is a list of the TAD0-TAD1 combinations with their corresponding addresses:

TAD0	TAD1	ADDRESS
0	0	SLT0
0	1	SLT1
1	1	SLT2
1	1	SLT3

(MSB) J1-1	J1-2 BUSY	J1-3 REVL	J1-4 WRTL	J1-7 WFML	J1-6 EDITL	(LSB) J1-5 ERASEL	Defined Output	Default Output	Output Code
1	1	0	0	0	0	0	RF		7
1	1	0	0	0	0	1		RF	7
1	1	0	0	0	1	0		RF	7
1	1	0	0	0	1	1		RF	7
1	1	0	0	1	0	0		RF	7
1	1	0	0	1	0	1		RF	7
1	1	0	0	1	1	0		RF	7
1	1	0	0	1	1	1		RF	7
1	1	0	1	0	0	0	WRT		4
1	1	0	1	0	0	1	ERV		0
1	1	0	1	0	1	0	WRTE		3
1	1	0	1	0	1	1		ERV	0
1	1	0	1	1	0	0	WFM		2
1	1	0	1	1	1	1	ERF		1
1	1	0	1	1	1	0		WFM	2
1	1	0	1	1	1	1		ERF	1
1	1	1	0	0	0	0	RR		6
1	1	1	0	0	0	1		RR	6
1	1	1	0	0	1	0	RRE		5
1	1	1	0	0	1	1		RRE	5
1	1	1	0	1	0	0		RR	6
1	1	1	0	1	0	1		RR	6
1	1	1	0	1	1	0		RRE	5
1	1	1	0	1	1	1		RRE	5
1	1	1	1	0	0	0		RR	6
1	1	1	1	0	0	1		RR	6
1	1	1	1	0	1	0		RRE	5
1	1	1	1	0	1	1		RRE	5
1	1	1	1	1	0	0		RR	6
1	1	1	1	1	0	1		RR	6
1	1	1	1	1	1	1		RRE	5
1	1	1	1	1	1	1		RRE	5

MSB = Most Significant Bit

LSB = Least Significant Bit

Table 3-2. Input/Output Combinations, Command PROM J1, Interface Board

3.3.5 Write Data Gates

Write data from the computer is inverted; then applied to quad D flip-flops C3 and C4. The write data is clocked out of the flip-flops on the leading edge of each succeeding write strobe. Data Busy must be false and WRITE GATE must be true to enable write data transmission. (DATA BUSY goes true when read data is output from the D bus of the microprocessor. WRITE GATE goes false when strobe pulses no longer clock J-K flip-flop H4.

3.3.6 Command Logic

Computer commands are input at J2-17 of the interface board and gated with load point, file protect and initiate comand signals. LP true, and FPT true will disable the command line AND gates when write or reverse commands are issued. GO false disables the command gates under any condition.

Any available computer command sets its respective J-K flip-flop and is clocked out to J1, a programable read only memory, on the trailing edge of the next GO pulse from the computer.

The command inputs to the PROM are read as two hexidecimal codes which are used to access an output code from the PROM memory. This binary code is output to I bus lines 8, 9, 10, and 0 of the microprocessor. (Table 3-2 lists the various output actions developed as a result of various computer command combinations. Some of these combinations are illegal and will cause the PROM to access the RUN FORWARD code. The microprocessor samples and tests the output of PROM J1 to determine its own operational sequence.

3.4 PHASE ENCODED READ

3.4.1 INTRODUCTION (See Figure 3-2)

The phase encoded read electronics perform the following functions: detect input data transitions from the transport, decode and deskew read data, generate the read clock, detect any formatting or parity errors, correct single track errors, and detect file marks.

While the detection of input data transitions is performed separately for each channel, the data is multiplexed after the initial detection stages and the functions listed above are performed by a single set of electronics for all nine channels. This is accomplished by scanning the nine channels sequentially, processing one channel at a time. The status of the control circuits is updated (UPDATE true) after each nine-channel scanning. When all functions have been performed the decoded data is demultiplexed by the deskew circuitry and supplied to the M bus of the microprocessor and ultimately to the interface.

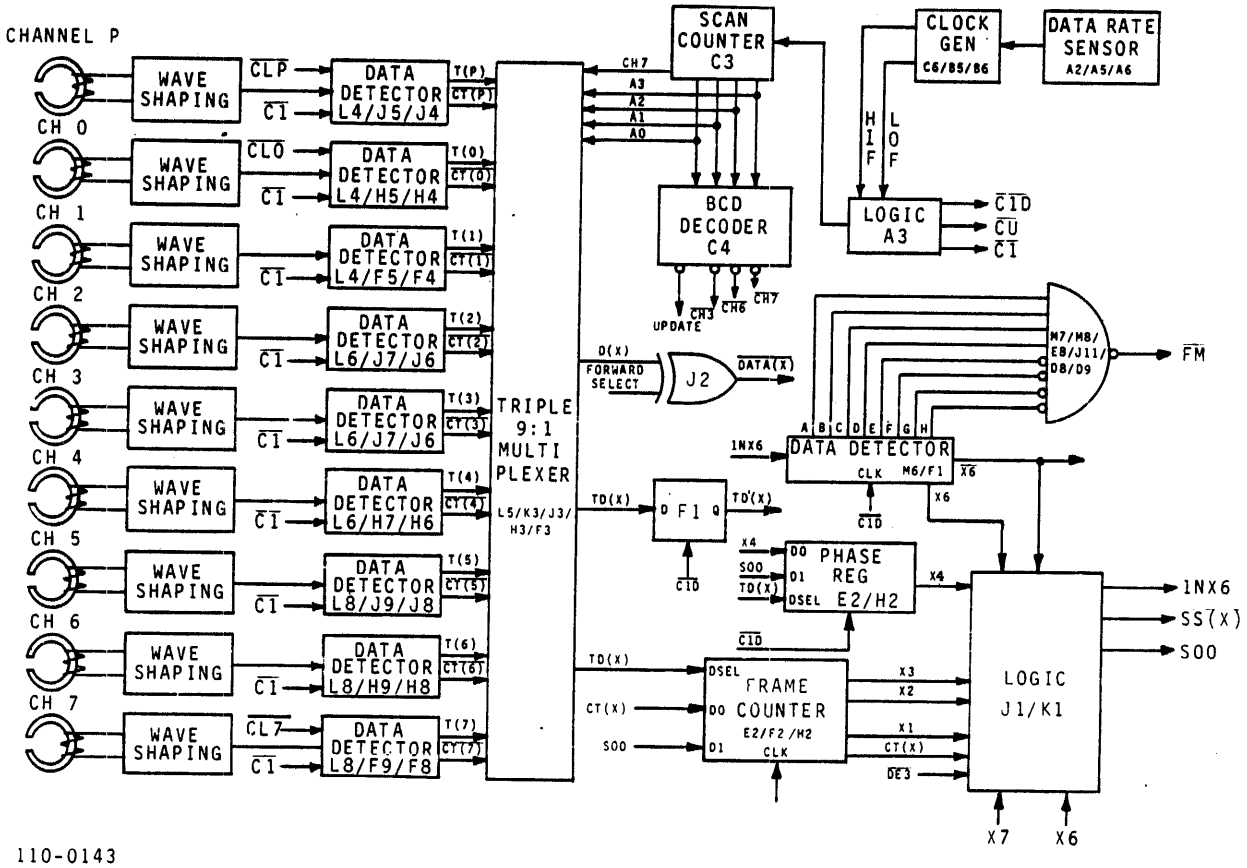


Figure 3-2. Block Diagram, Type 4657 PE Read Board

The various functions performed by the phase encoded read electronics are described in the following paragraphs. The description is divided into several parts, including the timing circuits, data transition detection, data decoding and deskewing, read clock generation, and read data detection.

3.4.2 TRACK ERRORS

The following conditions would cause a track error:

1. Crowded transitions, defined as more than one transition occurring within 25 percent of a character frame. One case is the detection of a transition within 25 percent of the character frame since the previous data transition. Alternately a crowded condition is recognized when an interphase-transition (defined as the midpoint of the character frame) is followed by a transition occurring before the 75 percent point of the frame.

2. Missing transitions, a condition defined as the absence of a transition within 125 percent of a character frame since the last data transition.

3. Inverted transition polarity. This error check samples the polarity of the present input data character, that of the previous data character and the state of the data transition detector.

   The parity of these signals should always be odd: otherwise an error is detected. For example, if the present input character is a 1 and the preceding character is also a 1, the interphase detector output should be true, indicating that the interphase transition was detected between the successive 1's. Similarly, if the input character is a 0 and the previous character was a 1, the output of the interphase-transition detector should be false, since no interphase transition should occur between a 1 and a 0. This error check detects spurious transitions caused by noise.

When any of the above conditions is detected, the DATA signal of the respective track is disabled for the remainder of the block, as is the SHIFT SERIAL Ss(X) signal, which shifts the input character into the deskew shift register. If the error occurs on one track only, it is correctable. However, if an error is detected on more than one track, a MULTIPLE TRACK ERROR (MTR) is indicated, inhibiting the DATA ENABLE (DE3) signal, which in turn inhibits the output data lines.

3.4.3 READ DETECTION CIRCUITRY
'See Schematic 401-4657-001, Page 3).

Read detection circuitry includes a BCD counter (C5), an eight bit binary counter C8/C9, JK flip-flops D7, D10 and several logic gates. This circuitry detects proper read circuit operation as a block of information is being read. Whenever READ ENABLE signal goes true to indicate that data reported in a phase encoded format is to be read, the clear on the BCD counter is disabled to permit it to operate during a sampling cycle to count the number of channels on which error-free data has been detected. The signal INX6 indicates whether or not error free data has been detected on a sampling channel. If error free data has been detected on all channels, the BCD counter will count to nine by $\overline{\text{UPDATE}}$ time and the complement of the single track error signal, $\overline{\text{STR}}$, will go high as the C/O output of the BCD counter goes true on the ninth count. If error-free data is detected on only eight channels as indicated by signal INX6, the BCD counter will only count to eight at the end of a sampling cycle and a logic one single track error signal, $\overline{\text{STR}}$ false, will be generated as the complement of the C/O output of the BCD counter. Output QD will be a logic 1 to indicate a count of 8 and the multiple track error signal, $\overline{\text{MTR}}$, which is generated as the complement of output QD, will be at logic 0.

In the event that data detected signal INX6 falls on two or more channels, the count will be less than eight at $\overline{\text{UPDATE}}$ time and both multiple track error signal $\overline{\text{MTR}}$ and the single track error signal $\overline{\text{STR}}$ will be generated.

3.4.4 INPUT DATA TRANSITION DETECTORS AND MULTIPLEX
(See Schematic 401-4657-00¹, Page 1).

The data lines are input from the B bus of the masterboard; then applied to data input registers M4/M5. Because the data detectors are synchronous systems which operate in response to the master clock pulse signal C1, they are in effect high speed sample data systems which sample the read head data signals (TD X) 48 times during each nominal data frame interval.

The data detectors are sampled at a rate of 256 kHz, which would normally permit a resolution of elapsed time between transitions of no more than 3.9 microseconds, or 1/6.4 of a data frame interval. However, digital timing information provided by the data detector each time it is sampled permits information transitions of a much higher resolution.

Each data detector includes a pair of D input flip-flops, (L4), an exclusive OR gate (K4) an OR gate (K5), a four bit binary counter (J5) and a pair of J-K flips-flops (J4). To understand the operation of the data detector, assume the read data parity (RDP) channel is initially low and has been low for at least 1/4 of a data frame interval period. Flip-flops L4 and the first J4 flip-flop are at a logical zero state; the second J4 flip-flop is at the logical 1 state and counter J5 is counting. Should RDP signal go high, the next low to high transition of clock signal C1 which is generated by the data rate sensor circuitry, sets the first L4 flip-flop. At the following transition

of C1, the second L4 flip-flop is set. During the interval between the setting of flip-flops L4, exclusive OR gate K4 generates an output pulse, setting the second J4 flip-flop. The output pulse from the exclusive OR gate also resets counter J5. The carry output signal from the counter indicates the end of a data frame interval quarter. This carry output pulse toggles the second J4 flip-flop, causing it to output $\overline{CT(P)}$ true signal. $\overline{CT(P)}$ signal is then directed to multiplexer J3, where it indicates whether an even or odd number of quarter data frame intervals have elapsed after the latest information transition.

Three 8 input multiplexers receive the three outputs from each data detector. The multiplexers output D(X), TD(X) and CT(X) signals in accordance with the addressing performed by binary coded decimal counter C3. (Lines A0-A3). This same address output is used to address 1 to 8 demultiplexer L5 which is capable of clearing any of the detector J-K flip-flops handling $\overline{CT}$ signal. $\overline{C1D}$ true enables the demultiplexer, which will clear the flip-flop controlling the data channel currently being processed. $\overline{C1D}$ signal indicates a channel multiplexing sampling interval as opposed to an update multiplexing sampling interval. A TD(X) signal, which indicates the presence or absence of an information transition during the preceding multiplex sampling interval, is also required to enable the multiplexer. When enabled, a clear signal for a given channel is generated during the multiplex sampling interval immediately after the multiplex sampling interval for that channel.

This delay of one clock pulse period insures that the J4 flip-flops are reset as soon as possible to prevent the loss of information without interfering with the sampling of information during a channel sampling interval. However, counter J5 is reset directly in response to a data transition. Flip-flop J4 is then resynchronized with counter J5 as soon as information is taken.

During a multiplex sampling interval, three separate information signals are sampled. A data signal, D (P), generated by the Q output of the second L4 flip-flop, indicates the current data information state and the T (P) signal, generated by the Q output of the second J4 flip-flop, permits transitions in this flip-flop to be counted for determining quarter data frame interval periods. For multiplexing purposes, master clock signals C1 are divided into ten sequential multiplexing intervals. The time multiplex sampling of the outputs from the data detectors thus occurs at an average of 4.8 sample intervals per data frame interval at 125 ips. Because of counter J5 and the second J4 flip-flop, the relatively slow multiplexing rate is sufficient to insure that information cannot be lost from the data detector.

3.4.5 DATA DETECT CIRCUITRY
(See Schematic 401-4657-001, Page 1).

M6, the nine bit data detect shift register, is clocked by the clock input data signal, $\overline{C1D}$, to keep track of whether error-free data has been detected on a given channel. X6 true from type D flip-flop F1 indicates error free data has been detected on a channel corresponding to a current multiplex sampling interval as designated by BCD counter C5. Once an error is detected on a given channel, that channel is disabled by a logical zero in the M6 data detector's storage location for that channel until a block of data has been read successfully. Lines A-H are output to the microprocessor's M bus.

The X6 term in the 1NX6 function permits a logic 1 state to be continued for a channel position once data has been detected unless one of the error conditions is indicated. The TD(X) term indicates that an information transition has been detected by a data detector for a given channel and the data (X) term requires that the information transition be of the logical 0 polarity. X6 and TD(X) permit synchronization of the channel and generation of a logic 1 input to data detector register M6 while a string of zeros is being read from the preamble of a block of information (or postamble when reading backwards).

3.4.6 DATA FRAME COUNTER
(See Schematic 401-4657-001, Page 1).

The function of the Data Frame Counter is to correlate the asynchronous input data transitions and the synchronous functions of the Format Control Unit. The counter identifies the time of each detected transition with respect to the standard character frame. The timing of the transition is used to distinguish between data transitions and phase-reversal transitions occurring between successive identical characters, and is also used to detect bit crowding or missing bits.

The frame counter (E2, F2 and H2) is a three bit counter with the three bit positions for a given channel arranged vertically in three separate nine bit shift registers. (On the schematic, each shift register is made up on one eight bit shift register with its corrresponding type D flip-flop, which adds the ninth bit. During the course of a multiplex sampling cycle, the three bits which correspond to each channel are shifted from left to right by one bit position for each multiplex sampling interval so that the output signals correspond to a current sampling interval. Within the frame counter, the lowermost nine bit shift register F2 stores the second least significant bit and uppermost nine bit shift register E2 stores the most significant bit. Each of these registers responds to one of two inputs in accordance with an address input. The transition detected signal, TD(X), is connected to drive the address input so that the D0 inputs are addressed when a transition is not detected and the D1 inputs are addressed during a sampling interval immediately following the detection of an information transition by data detector M6. The D1 inputs of registers F2 are connected to ground while the D1 input of register F2 is connected to the signal SOD. In this way the phase counter for a given channel is preset to count 0 upon detection of a data

information transition and preset to count 010 upon detection of a phase transition. The frame counter is thus resynchronized with the actual occurence of information transitions upon detection of each information transition. The D0 input to the least significant bit register F2 input is responsive to the multiplex signal CT(X). The D0 inputs of registers F2 have their inputs, 1NX2 and 1NX3 connected to respond to conventional counting circuitry to permit the frame counter to be incremented each time signal CT(X) changes states. The outputs from the frame counter are designated X1, X2, and X3 respectively, and indicate the binary count of the number of at least partially elapsed quarter data frame intervals subsequent to a preceding data information transition for a given channel sampling period during its' multiplex sampling interval.

Logic J1, which generates the 1NX6 data detected signal, also generates the phase transition signal to indicate a phase transition. Logic circuitry J1 also generates shift serially signal SS(X) which serves as a clock signal for deskew circuitry. This signal is generated each time an information transition is detected on a currently sampled channel and the transition is not a phase information transition and no errors are detected.

3.4.7 DATA DESKEWING CIRCUITRY
(See Schematic 401-4657-001, Page 2)

The deskewing circuitry corrects skew variations between the nine input data channels. A maximum of three-character skew can be corrected. In addition, the deskewing circuitry is used to detect the preamble and the postamble, supplying only the valid data to the output with a read clock.

The deskew circuitry consists of six shift registers (B2, C2, D2), and six multiplexers (B1, C1, D1, E3, E4 and E5). Each of the shift registers comprises a stage of the deskew register. The multiplexed input data is shifted into the deskew register by $\overline{C1D}$, whenever a data transition is detected, provided that it is not an interphase transition and that no track error is detected. $\overline{C1D}$ shifts the data along the deskew register, supplying the present input character into the first stage, 1NX7, while the contents of the register are shifted one stage up. Until the first 1 bit of the preamble is input into the deskew register the 40 0's of the preamble are ignored by the output.

As the first one bit is shifted vertically upward, it marks the demarcation between preamble or postamble zero information and data information. (See Table 3-3). Thus, the information stored in a

TYPICAL CHANNEL WRITING ALTERNATE 1S AND 0S

REGISTER CONTENTS	REGISTER STAGE NUMBER					
	1	2	3	4	5	6
DURING PREAMBLE	0	0	0	0	0	0
FIRST 1 BIT	(POINTER) 1	0	0	0	0	0
FIRST DATA BIT	DATA 1	(POINTER) 1	0	0	0	0
SECOND DATA BIT	DATA 0	DATA 1	(POINTER) 1	0	0	0
THIRD DATA BIT, DIR GOING TRUE	DATA 1	DATA 0	DATA 1	(POINTER) 1	0	0
DATA IN ALL CHANNELS, DIRS GOING TRUE, CHARACTER OUTPUT	DATA 0	DATA 1	DATA 0	DATA 1 TO INTERFACE	(POINTER) 1	0
FOLLOWING DIRS, POINTER RETURNED	0	1	0	(POINTER) 1	0	0
OVERFLOW CONDITION, IF SS(X) IS ISSUED	0	1	0	1	0	(POINTER) 1
POSTAMBLE CONDITION IF TRUE FOR ALL CHANNELS	0	0	1	(POINTER) 1		

110-0079

Table 3-3. Deskew Shift Register Operation

vertically extending channel register below the pointer bit is data information. The vertically extending channel registers are operated as first-in-first-out shift registers with data information being output from the register position immediately below the pointer bit. As information is output from a channel register, the pointer bit is shifted vertically downward to the position from which the data information was output and is replaced with a zero at the former position.

The inputs INX7-INX12 to multiplexers E3, E4 and E5 are provided from the outputs of multiplexers, B1, C1 and D1. C1 and D1 are addressed at data inputs SEL A and SEL B. B1 is only addressed at SEL B. The least significant SEL A inputs are responsive to the complement of the shift serially signal, Sx(X). The SEL B, or most significant, address inputs of multiplexers C1 and D1 are connected to data input ready shift signal, DIRS. SEL B on multiplexer B1 is connected to Ss(X). DIRS true is generated when the available data has been detected on all active channels during the preceding multiplex sampling cycle. This causes data to be output from the deskew register.

Usually, DIRS is false because data is not being output and signal Ss(X) is true for the same reason. At this time the C1 inputs to each of the multiplexers are addressed and data is merely circulated from the outputs to the inputs of the shift registers. In the event that signal $\overline{Ss(X)}$ goes low, the 2C1 inputs are addressed. Input 2A to multiplexer B1 is responsive to the $\overline{DATA\ (X)}$ signal and receives the data information state corresponding to a data information transition which caused the generation of the shift serially signal. The CO inputs on each of the other multiplexers is responsive to the output of the shift register which is one bit position below the bit position to which the multiplexer corresponds. Thus, data is shifted vertically upward one bit position as new data is entered into a vertically extending channel register.

The overflow signal, OVF, is output at B1-9 whenever the shift serially signal indicates that a new data transition has been detected while the pointer bit is in the X12, or maximum, position.

Multiplexers E3, E4, and E5 output a serial data signal, RDATA (X), which indicates the contents of the bit position in the deskew register immediately behind the pointer bit when it is at position X10, X11 or X12. These demultiplexers comprise the deskewing network, and also output a postamble (POST (X)) signal whenever data is available for output from the deskew register and a sampled channel has the data content of a logic one followed by two zeros. Although the actual postamble contains a logic one followed by 40 zeros, postamble detection is assumed when a logic one followed by two zeros is detected on all active channels. If the pointer bit is at positions X7, X8 or X9 in the deskew register, the POST (X) signal goes true. However, since the pointer bit is not in one of the deskew register positions which permits outputting data information, these signals are not acted upon by the read system. The POST (X) signal will be generated if position X10 stores a logic one while positions X9 and X8 store logic zeros.

3.4.8 DATA OUTPUT REGISTER (See Schematic 401-4657-001, Page 2).

The serially loaded data output register consists of IC E10 and type D flip-flop J11, which supplies the ninth bit. RDATA (X) from the deskewing network and deskewing buffers supplies the data output register with data bits. These bits are output to the $\overline{M}$ bus of the microprocessor on lines $\overline{M0}$ through $\overline{M8}$ during SHIFT DATA CLOCK true time. The read data output NAND gates are enabled by READ OUTPUT ENABLE true, which in turn is enabled by logic ones on microprocessor command lines CM 16, 17 and 18, as well as DIRS true.

3.4.9 CLOCK GENERATOR, DATA RATE SENSOR & LOGIC (See Schematic 401-4657-001, Page 3).

The data rate sensor consists of track selection circuitry (J-K flip-flops A2, AND gates A5, NOR gate A5) as well a count by five counter A6. Because the phase encoded read system is capable of operating with one of the nine channels disabled after the occurrence of a single track error on the disabled channel, the feedback mechanism for detecting actual data rates must be responsive to two separate channels in case an error is encountered on a selected first channel. The data rate sensor is responsive to either channel 6 or channel 7, depending on which channel first detects a data information transition. Whichever channel first becomes active then remains active until an error is detected on that channel. When an error is detected, the alternate channel becomes activated to provide data rate feedback control.

During the course of reading an interblock gap, both A2 flip-flops are reset by signal $\overline{X6}$ when clocked Resetting these flip-flops disables the clear inputs, which are cross-coupled. As soon as error-free data is detected upon reading the preamble of a data block, as indicated by shift serially signal SS (X), the corresponding flip-flop is clocked to the set state.

In the event that an error is detected on channel 7 during the course of reading a block of data, signal $\overline{X6}$ goes true during the channel 7 sampling interval, causing flip-flop A2-12 to become reset. This enables flip-flop A2-2. During the next channel 6 sampling interval during which a data transition is detected, shift serially signal $\overline{SS\ (X)}$ goes true to set flip-flop A2-2 enables the T input of counter 72 during channel 6 sampling intervals. Four-bit counter A6 now begins counting sequences of five data frame intervals occurring on channel 6.

While counter A6 is counting groups of five data frame intervals, counter C5 begins counting down

from 33 in response to multiplex sampling cycles. With the master clock operating at synchronous speed, there should be 6.4 times 5, or 32 multiplex sampling cycles during each group of five consecutive data frame intervals.

The output of inverter E11 is applied to a voltage controlled oscillator and a pair of LS 124 one shots (A3). The VCO frequency is approximately one to two percent above the synchronous speed as determined by the counters. Optimum accuracy occurs when the clock generator is running slightly fast.

The output of the voltage controller oscillator becomes C1, which is the master clock signal used for interval timing. Its complement, $\overline{C1}$, is used to clock control clock flip-flop B4, concurrent with every tenth master clock pulse.

3.5 SCAN COUNTER

(See Schematic 401-4657- 001, Page 3).

The scan counter consist of clock C3 and demultiplexer C4. The clock divides the basic C1 master clock frequency into specific scanning periods for each channel. A0-A3 from this clock are applied to the 8 to 1 demultiplexers in the data transition detect circuitry. UPDATE output and its complement, $\overline{\text{UPDATE}}$ from the demultiplexers are used extensively throughout the control circuitry.

SECTION IV

MAINTENANCE INSTRUCTIONS

4.1 INTRODUCTION

This section contains several troubleshooting aids which will help pinpoint the faulty component(s) if their use is understood.

Table 4-1 is a pin list of the A and B buses on the masterboard. With the aid of this table, many problems can be isolated to either the interface board, the microprocessor board or the PE read board in formatters having PE read capability.

Tables 4-2 thru 4-7 contain the BASIC NRZI and PE programs of the microprocessor board. (Two sets of programs are provided for the two revision levels of PROMs currently in use.) The programs contain the hexidecimal addresses found on the MA bus lines. These are parallel-connected to the microprocessor PROMs and originate in the 3001 Central Processing Element. (Refer to Figure 4-1 for a simplified block diagram of the 3001 Microprogram Control Unit, the 3002 Central Processing Elements and 3601 Programmable Read Only Memories.) The 3000 ACTION listing indicates actions performed by the 3001 MCU and the 3002 CPE.

The commands from command lines CM16, CM17 and CM18 are also referenced. These commands are defined in Table 4-8, the Microprocessor Command Summary. This list indicates the significant bus line(s) and thus the significant 3002 IC during a given command time.

4.2 TROUBLESHOOTING THE MICROPROCESSOR BOARD

Equipment Required:

Logic Analyzer (Hewlett Packard HP 1607 or equivalent)

Kennedy TB 9219 Test Box

Kennedy PROM Tester PN 190-4780-001

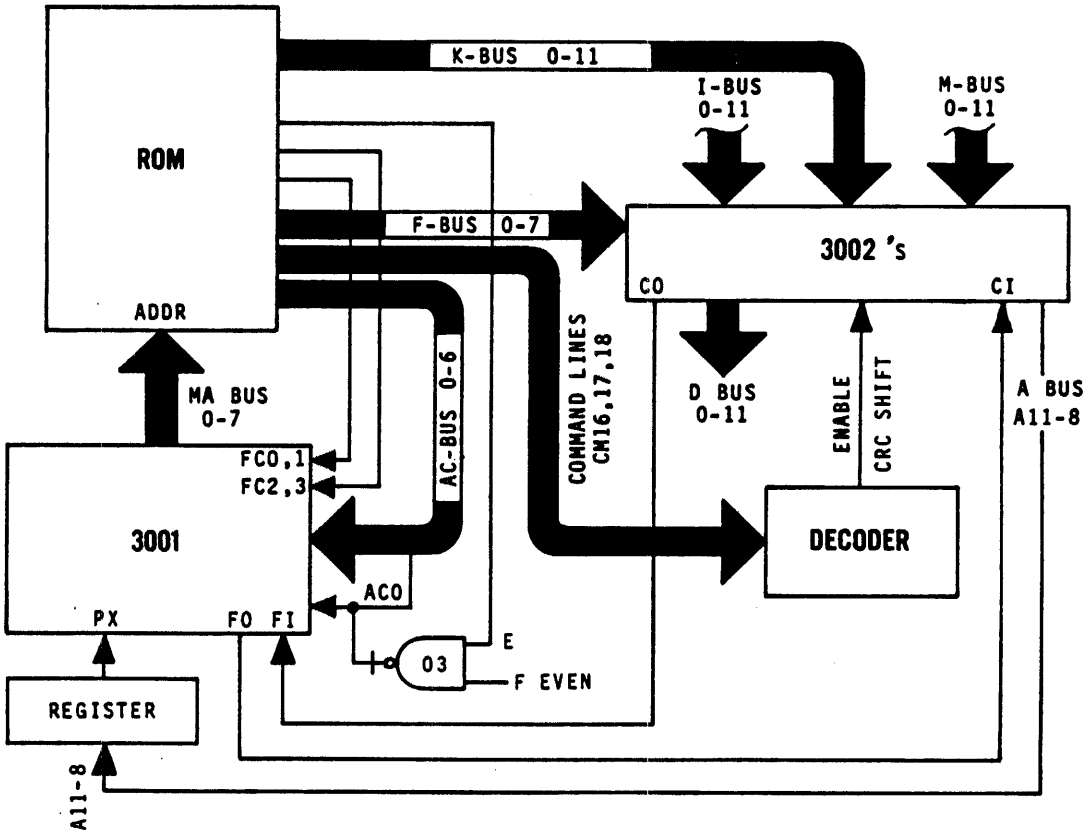


Figure 4-1 Partial Block Diagram, Microprocessor Board

4.2.1 PROM Testing

The PROM's may be tested for the required odd parity with the 190-4780-001 PROM test card. The PROM tester is inserted into one of the card slots of the masterboard; then one PROM at a time is removed from the microprocessor board and inserted into the PROM testing receptacle. A lighted PARITY LED on the test card indicates the PROM has even parity and is therefore defective. The remaining three LED's are numbered 1, 2, and 4, which light to indicate in BCD code the last digit only of the PROM under test. The PROM Locations chart in the schematic section of the manual should be checked to verify that the PROM was inserted in the correct PROM location.

IMPORTANT NOTE

When replacing PROMS, make certain the replacement PROM(s) is/are at the correct revision level. This is marked on the IC. Revision levels must never be mixed, since new and old PROM programs may not be compatible. PROMS with dissimilar revision levels must be replaced as a complete set.

4.2.2 3001 MCU Testing

This IC is most rapidly checked by substitution.

4.2.3 3002 CPE Testing

Operate the formatter in the program section most likely to cause the malfunction. Note the command time currently in operation and compare the state of the significant 3002 bus line(s) with the states indicated in the Microprocessor Command Summary, Table 4-4. Obviously, a mismatch may indicate the 3002 CPE is defective. The outboard components may be tested by comparing the state of the significant bus lines at the masterboard with readings made at the significant 3002 IC.

4.2.4 Type 4657 PE Read PC Board PLO Adjustment

1. Connect oscilloscope test probe to test point DD. Set for AC measurement, using chassis ground reference.
2. Commence PE read operations in high density mode.
3. Adjust HI trimpot connected to one-shot IC A3-3 for AC null.
4. Switch to low density PE read operations. Adjust LO trimpot connected to IC A3-2 for AC null. Adjustment is complete.

MASTERBOARD CONNECTORS "A" SIDE

PIN NO.	MNEMONIC	4657 PE BOARD	4831 INTERFACE BOARD	4632/4832 CONTROL BOARD	TRANSPORT CONNECTOR PIN NO.	DESCRIPTION
01	GRD	GRD	GRD	GRD		GROUND
02	+5 VOLTS	+5 VOLTS	+5 VOLTS	+5 VOLTS		+5 VOLTS
03	$\overline{A0}$			OUTPUT (NC)		TT SELECT (OPTIONAL)
04	$\overline{A1}$			OUTPUT (NC)		TT SELECT (OPTIONAL)
05	$\overline{A2}$			OUTPUT (NC)		TT SELECT (OPTIONAL)
06	$\overline{A3}$			OUTPUT (NC)		TT SELECT (OPTIONAL)
07	$\overline{A4}$			OUTPUT (NC)		NC
08	$\overline{A5}$			OUTPUT (NC)		A BUS NC
09	$\overline{A6}$			OUTPUT (NC)		NC
10	$\overline{A7}$			OUTPUT (NC)		NC
11	$\overline{A8}$			OUTPUT (NC)		
12	$\overline{A9}$			OUTPUT (NC)		NEXT
13	$\overline{A10}$			OUTPUT (NC)		ADDRS
14	$\overline{A11}$			OUTPUT (NC)		BUS
15	$\overline{D0}$	INPUT		OUTPUT		(A8-11)
16	$\overline{D1}$	INPUT		OUTPUT		
17	$\overline{D2}$		INPUT	OUTPUT		
18	$\overline{D3}$		INPUT	OUTPUT		
19	$\overline{D4}$			OUTPUT (NC)		
20	$\overline{D5}$			OUTPUT (NC)		$\overline{\text{D BUS}}$
21	$\overline{D6}$			OUTPUT (NC)		
22	$\overline{D7}$			OUTPUT (NC)		
23	$\overline{D8}$			OUTPUT (NC)		
24	$\overline{D9}$			OUTPUT (NC)		
25	$\overline{D10}$			OUTPUT (NC)		
26	$\overline{D11}$		INPUT	OUTPUT		
27	D0	INPUT	INPUT	OUTPUT		
28	D1	INPUT	INPUT	OUTPUT		D BUS $\overline{R7}$ (CM1) $\overline{R6}$ (CM1)
29	$\overline{CM16}$			OUTPUT		
30	$\overline{CM17}$	INPUT	INPUT	OUTPUT		COMMAND BUS
31	$\overline{CM18}$	INPUT	INPUT	OUTPUT		
32	$\overline{MREST}$	INPUT	OUTPUT	INPUT		MASTER RESET
33	$\overline{STROBE}$			OUTPUT (NC)		STROBE CLOCK
34	$\overline{CX}$			OUTPUT (NC)		$\overline{CX}$ CLOCK
35	$\overline{CY}$	INPUT		OUTPUT		$\overline{CY}$ CLOCK
36	GRD	GRD	GRD	GRD		GRD
37	GRD	GRD	GRD	GRD		GRD
38	$\overline{I0}$	OUTPUT	OUTPUT	INPUT		VRC ERR (CM5)*
39	$\overline{I1}$	OUTPUT		INPUT		$\overline{\text{POST}}$ ERR (CM5)*
40	$\overline{I2}$	OUTPUT	OUTPUT	INPUT		$\overline{9\ TRK}$ (CM3) MTRK (CM5)*
41	$\overline{I3}$	OUTPUT	OUTPUT	INPUT		$\overline{556/800}$ (CM3) STRK (CM5)*
42	$\overline{I4}$	OUTPUT	OUTPUT	INPUT		$\overline{RNG}$ (CM2) 1600 BPI (CM3) SKEW (CM5)*
43	$\overline{I5}$	OUTPUT	OUTPUT	INPUT		$\overline{I\ BUS}$ $\overline{ONL}$ (CM2) FMKD (CM5)*
44	$\overline{I6}$	OUTPUT	OUTPUT	INPUT		$\overline{EOT}$ (CM2) LO SPEED (CM3) READ ENABLE (CM5)*
45	$\overline{I7}$	OUTPUT	OUTPUT	INPUT		HDI (CM2) HI SPEED (CM3) POST DET (CM5)*
46	$\overline{I8}$	OUTPUT	OUTPUT	INPUT		FWD SEL (CM5)*
47	$\overline{I9}$	OUTPUT	OUTPUT	INPUT		LDP (CM2) DE3 (CM5)*
48	$\overline{I10}$	OUTPUT	OUTPUT	INPUT		RWD (CM2) BLOCK (CM5)*
49	$\overline{I11}$	OUTPUT		INPUT		RDY (CM2) CORRECTION ENABLE (CM5)*
50	M0		OUTPUT	INPUT		RD7 (CM5) WD7 (CM3)
51	M1		OUTPUT	INPUT		RD6 (CM5) WD6 (CM3)
52	M2		OUTPUT	INPUT		RD5 (CM5) WD5 (CM3)
53	M3		OUTPUT	INPUT		RD4 (CM5) WD4 (CM3)
54	M4		OUTPUT	INPUT		M BUS RD3 (CM5) WD3 (CM3)
55	M5		OUTPUT	INPUT		RD4 (CM5) WD2 (CM3)
56	M6		OUTPUT	INPUT		RD11 (CM5) WD1 (CM3)
57	M7		OUTPUT	INPUT		RD0 (CM5) WD0 (CM3)
58	M8		OUTPUT	INPUT		RDP (CM5) WDP (CM3)
59	$\overline{M9}$	OUTPUT		INPUT		
60	$\overline{M10}$	OUTPUT		INPUT		
61	$\overline{M11}$	OUTPUT	OUTPUT	INPUT		
62	D4		INPUT	OUTPUT		WD3 (CM3) R3 (CM1)
63	D5			OUTPUT		WD2 (CM3) R2 (CM1)
64	D6			OUTPUT		WD1 (CM3) R1 (CM1)
65	D7			OUTPUT		D BUS WD0 (CM3) R0 (CM5)
66	D8			OUTPUT		WDP (CM3) HDS (CM2)
67	D9		INPUT	OUTPUT		
68	D10			OUTPUT		
69	D11		INPUT	OUTPUT		
70	-12 VOLTS	-12 VOLTS	-12 VOLTS	-12 VOLTS		-12 VOLTS
71	+5 VOLTS	+5 VOLTS	+5 VOLTS	+5 VOLTS		+5 VOLTS
72	GRD	GRD	GRD	GRD		GROUND

* Signal present in PE formatters only. CM stands for command. WDP (CM3) means WDP is present during command 3 time, for example.

Table 4-1A Masterboard Pin List — 'A' Side

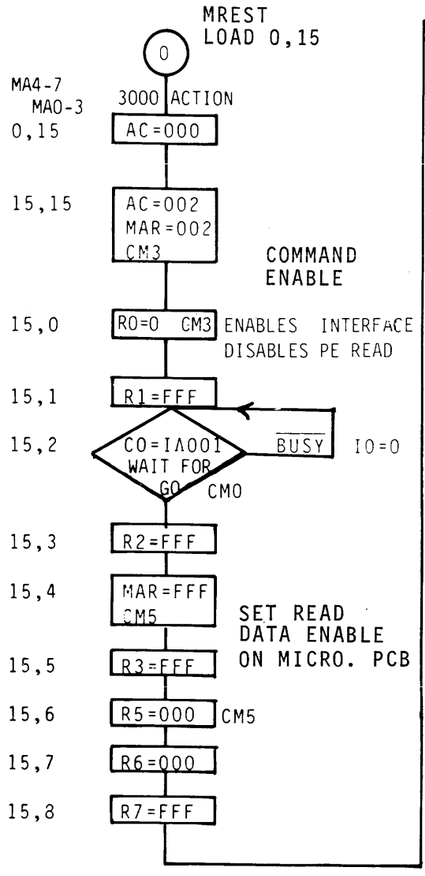
MASTERBOARD CONNECTORS "B" SIDE

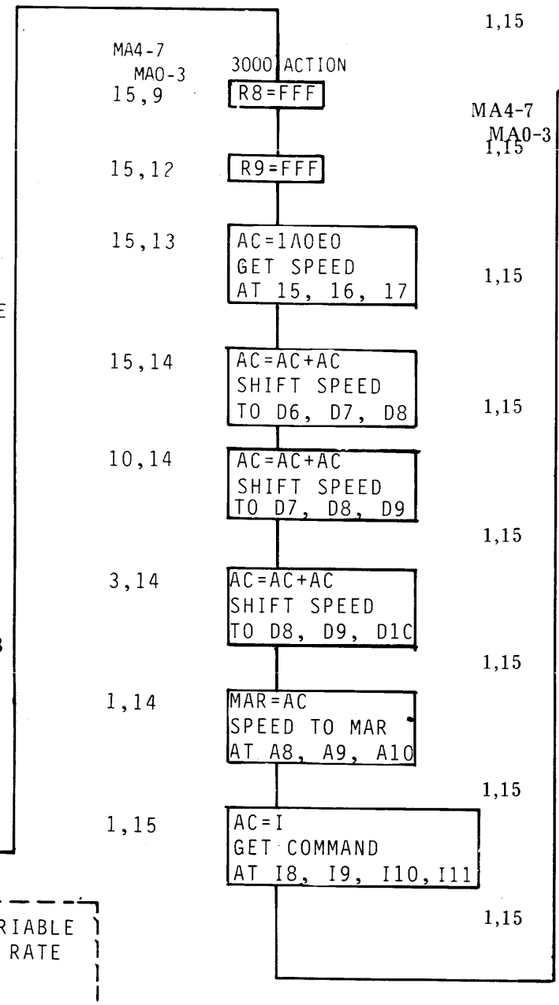
PIN NO.	4632 4832 CONTROL BOARD	4657 PE BOARD	4831 INTERFACE BOARD	MNEMONIC	TRANSPORT	DESCRIPTION	9000 TRANSPORT CONNECTOR PIN NO.	9100/ 9300/ 9700 PIN NO.
01	GRD	GRD	GRD	GRD				
02	+5 VOLTS	+5 VOLTS	+5 VOLTS	+5 VOLTS				
03	INPUT			RDS	OUTPUT	READ DATA STROBE (CD3/5)**	A11J1-A	J3-1
04	INPUT		INPUT	ONL	OUTPUT	ON LINE (CD2)**	A10J1-M	J1-M
05	INPUT		INPUT	LDP	OUTPUT	LOAD POINT (CD2)**	A10J1-R	
06	OUTPUT*			SLT5		SELECT TAPE UNIT 5*		
07	INPUT		INPUT	RWD	OUTPUT	REWINDING (CD2)**	A10J1-N	J1-N
08	INPUT		INPUT	FPT	OUTPUT	FILE PROTECT (CD2)**	A10J1-P	J1-P
09	INPUT	INPUT		RDP	OUTPUT	READ DATA P (7 TRACK C) (CD3/5)**	A11J1-B	J3-1
10	INPUT	INPUT	OUTPUT	RDO	OUTPUT	READ DATA O (CD3/5)**	A11J1-C	J3-3
11	INPUT	INPUT		RD1	OUTPUT	READ DATA 1 (CD3/5)**	A11J1-D	J3-4
12	INPUT	INPUT		RD2	OUTPUT	READ DATA 2 (7 TRACK B) (CD3/5)**	A11J1-E	J3-8
13	INPUT	INPUT		RD3	OUTPUT	READ DATA 3 (7 TRACK A) (CD3/5)**	A11J1-F	J3-9
14	INPUT	INPUT		RD4	OUTPUT	READ DATA 4 (7 TRACK 8) (CD3/5)**	A11J1-H	J3-14
15	INPUT	INPUT		RD5	OUTPUT	READ DATA 5 (7 TRACK 4) (CD3/5)**	A11J1-J	J3-15
16	INPUT	INPUT		RD6	OUTPUT	READ DATA 6 (7 TRACK 2) (CD3/5)**	A11J1-K	J3-17
17	INPUT	INPUT		RD7	OUTPUT	READ DATA 7 (7 TRACK 1) (CD3/5)**	A11J1-L	J3-18
18	INPUT		INPUT	EOT	OUTPUT	END OF TAPE (CD2)**	A10J1-U	J1-U
19	INPUT		INPUT	RDY	OUTPUT	TRANSPORT READY (CD2)**	A10J1-T	J1-T
20	INPUT			RNG	OUTPUT	TAPE RUNNING (CD2)**	A10J1-V	J1-V
21	OUTPUT*			SEL6		SELECT TAPE UNIT 6* (CD7)**		
22	OUTPUT*			SEL7		SELECT TAPE UNIT 7* (CD7)**		
23	OUTPUT*			SEL8		SELECT TAPE UNIT 8* (CD7)**		
24	OUTPUT*		OUTPUT	SEL1	INPUT	SELECT TAPE UNIT 1* (CD7)**	A10J1-W	J4-A,C
25	OUTPUT*		OUTPUT	SEL2	INPUT	SELECT TAPE UNIT 2* (CD7)**	A10J1-X	J4-D,F
26	OUTPUT*		OUTPUT	SEL3	INPUT	SELECT TAPE UNIT 3* (CD7)**	A10J1-Y	J4-H,K
27	OUTPUT*		OUTPUT	SEL4	INPUT	SELECT TAPE UNIT 4* (CD7)**	A10J1-Z	J4-P,R
28		INPUT	INPUT	D2		D BUS		
29	OUTPUT	INPUT		CM16		(LEAST SIGNIFICANT)		
30	OUTPUT	INPUT		CM17		COMMAND BUS		
31	OUTPUT	INPUT		CM18		(MOST SIGNIFICANT)		
32		INPUT	INPUT	D3		D BUS		
33	OUTPUT		INPUT	STROBE		WRITE STROBE		
34	OUTPUT			CX		CX CLOCK		
35	OUTPUT	INPUT		CY		CY CLOCK		
36		GRD	GRD	GRD		GROUND		
37		GRD	GRD	GRD		GROUND		
38	OUTPUT		INPUT	CD1		COMMAND CLOCK 1		
39	OUTPUT		INPUT	CD3		COMMAND CLOCK 3		
40								
41								
42								
43								
44						AC UNREG PWR FAIL (ANALOG SIG)		
45	OUTPUT			SRC	INPUT	SYNCHRONOUS REV COMMAND (CD7)**	A10J1-E	J1-E
46	OUTPUT		OUTPUT	OFFC	INPUT	OFF LINE COMMAND (CD7)**	A10J1-L	J1-L
47	OUTPUT			SFC	INPUT	SYNCHRONOUS FWD COMMAND (CD7)**	A10J1-C	J1-C
48	OUTPUT		OUTPUT	REW	INPUT	REWIND COMMAND (CD7)**	A10J1-H	J1-H
49	OUTPUT			SWS	INPUT	SET WRITE STATUS (CD7)**	A10J1-K	J1-K
50	OUTPUT	INPUT		$\overline{WD7}$	INPUT	WRITE DATA 7 (7 TRACK 1) (CD4)**	A11J1-Z	J2-V
51	OUTPUT	INPUT		$\overline{WD6}$	INPUT	WRITE DATA 6 (7 TRACK 2) (CD4)**	A11J1-Y	J2-U
52	OUTPUT	INPUT		$\overline{WD5}$	INPUT	WRITE DATA 5 (7 TRACK 4) (CD4)**	A11J1-X	J2-T
53	OUTPUT	INPUT		$\overline{WD4}$	INPUT	WRITE DATA 4 (7 TRACK 8) (CD4)**	A11J1-W	J2-S
54	OUTPUT	INPUT		$\overline{WD3}$	INPUT	WRITE DATA 3 (7 TRACK A) (CD4)**	A11J1-V	J2-R
55	OUTPUT	INPUT		$\overline{WD2}$	INPUT	WRITE DATA 2 (7 TRACK B) (CD4)**	A11J1-U	J2-P
56	OUTPUT	INPUT		$\overline{WD1}$	INPUT	WRITE DATA 1 (CD4)**	A11J1-T	J2-N
57	OUTPUT	INPUT		$\overline{WD0}$	INPUT	WRITE DATA 0 (CD4)**	A11J1-S	J2-M
58	OUTPUT	INPUT		$\overline{WDP}$	INPUT	WRITE DATA P (7 TRACK C) (CD4)**	A11J1-R	J2-L
59								
60								
61								
62	INPUT		INPUT	HDI	OUTPUT	HIGH DENSITY INDICATOR (CD2)**	A10J1-F	J1-F
63	OUTPUT		OUTPUT	HDS	INPUT	HIGH DENSITY SELECT (CD7)**	A10J1-D	J1-D
64			OUTPUT	EDIT L	INPUT	EDIT	A10J1-B	J1-B
65	OUTPUT			WDS	INPUT	WRITE DATA STROBE (CD4)**	A11J1-N	J2-A
66	OUTPUT			WARS	INPUT	WRITE AMPLIFIER RESET (CD4)**	A11J1-P	J2-C
67								
68								
69								
70	-12 VOLTS	-12 VOLTS	-12 VOLTS	-12 VOLTS		-12 VOLTS		
71	+5 VOLTS	+5 VOLTS	+5 VOLTS	+5 VOLTS				
72	GRD	GRD	GRD	GRD		GROUND		

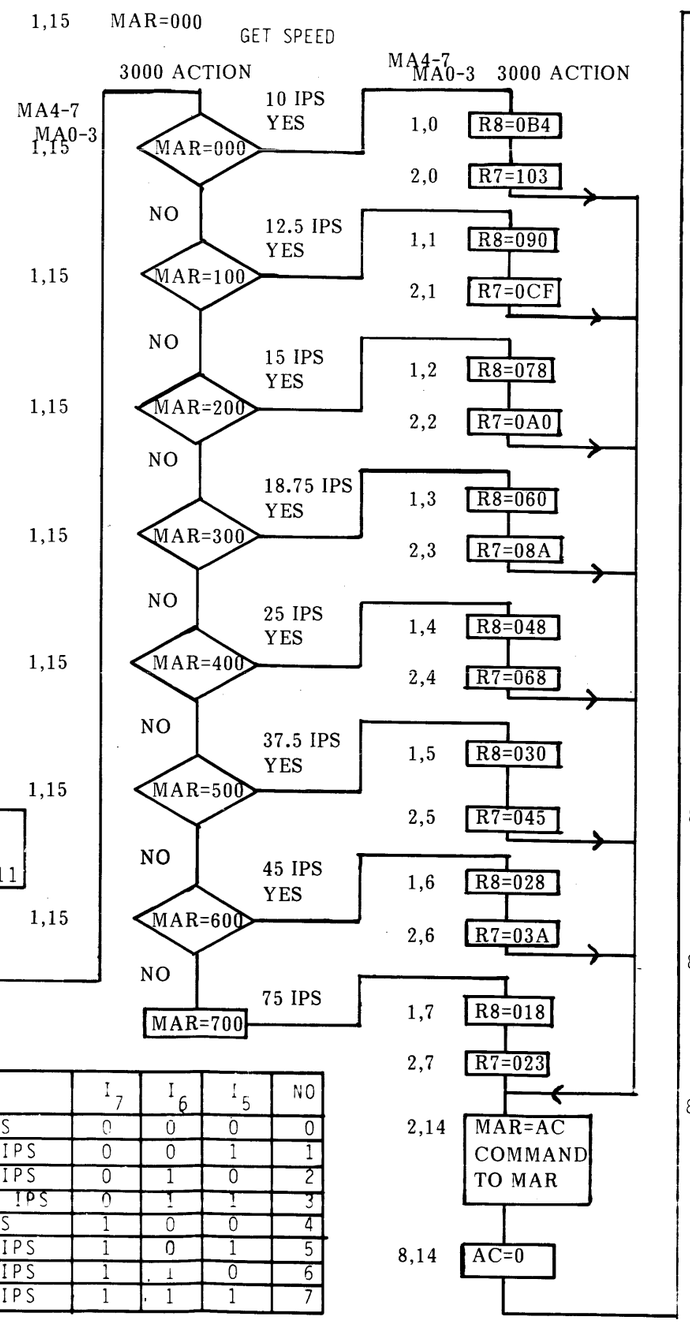
* Not used in normal configuration.

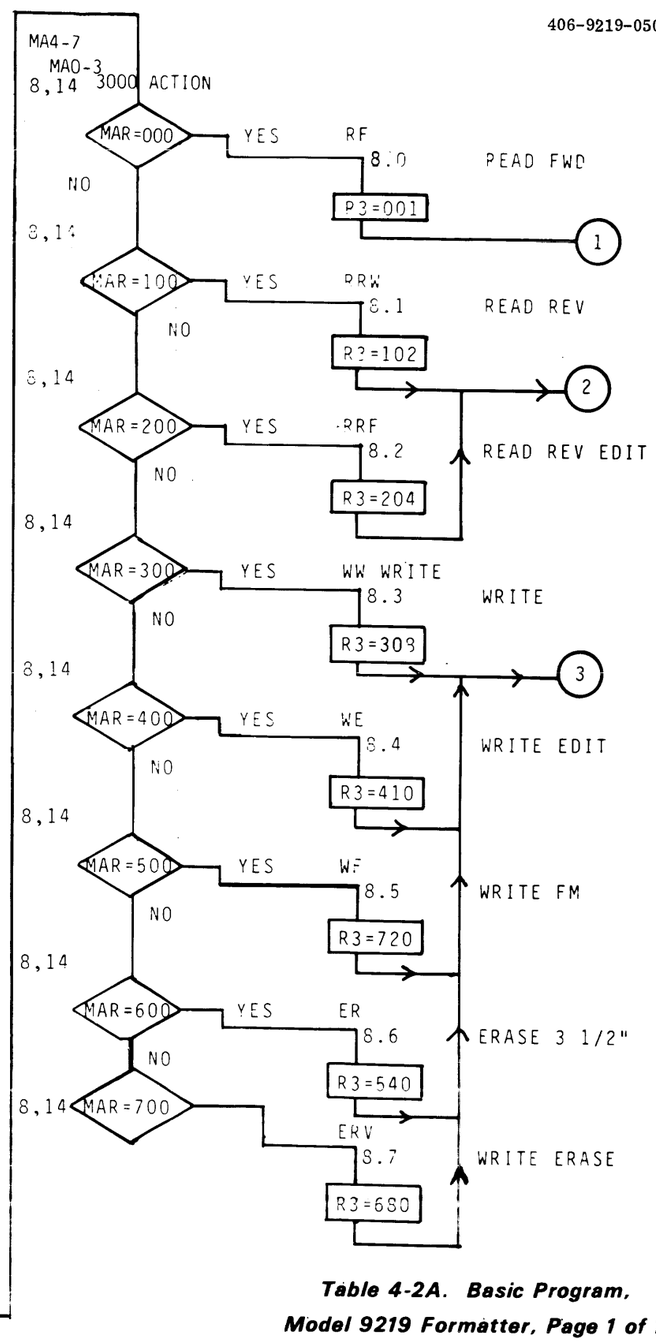
** CD denotes command time when line is enabled, permitting signal to enter or exit micro processor board.

Table 4-1B Masterboard Pin List — 'B' Side









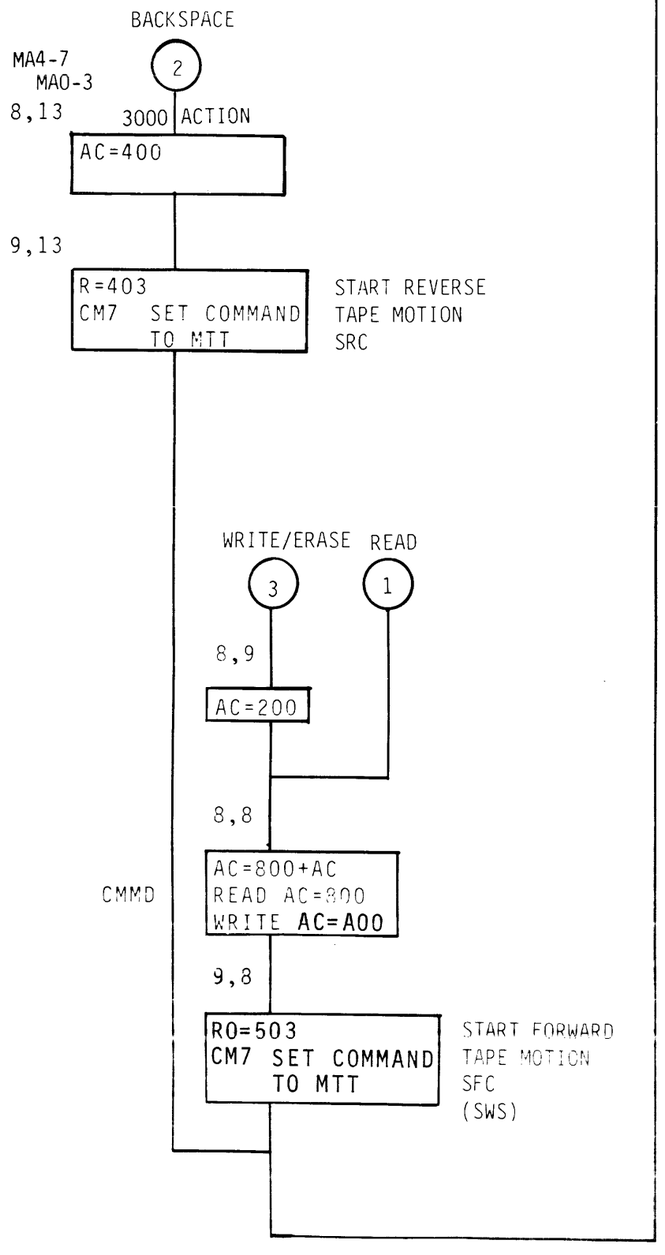
406-9219-050A1

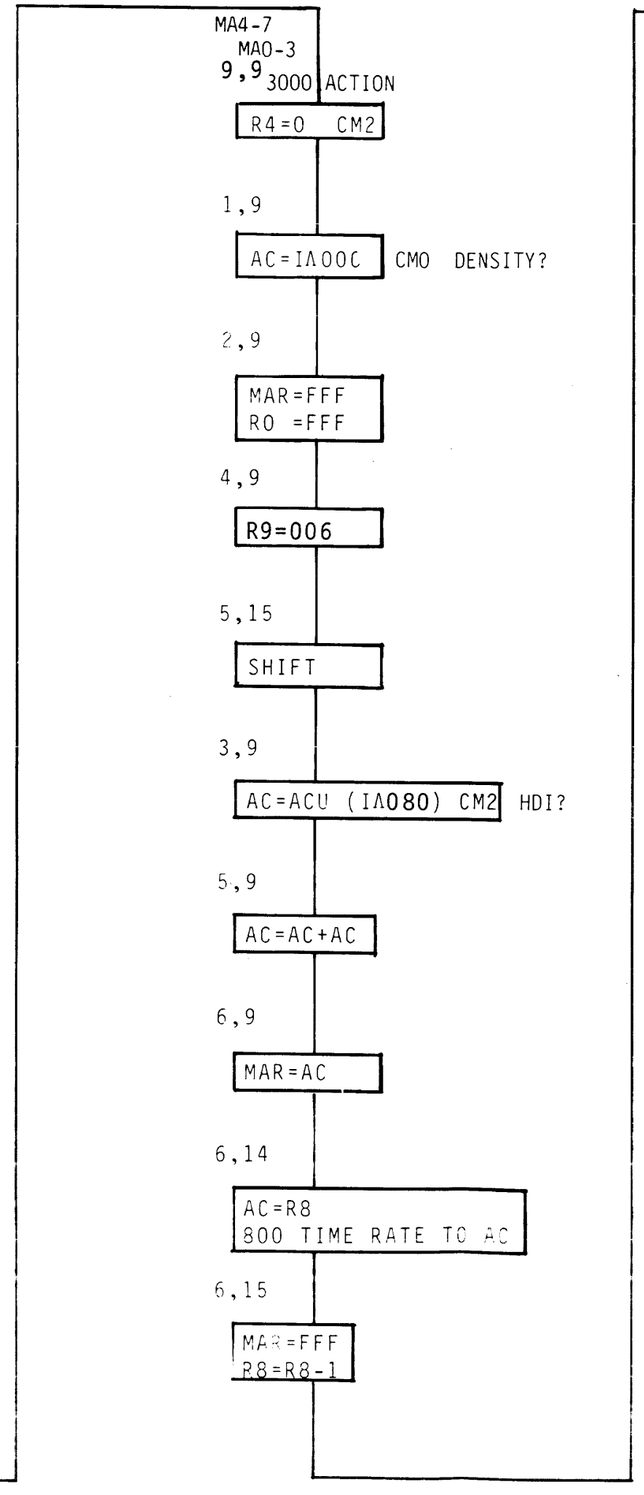
SPEED	I_7	I_6	I_5	NO
10 IPS	0	0	0	0
12.5 IPS	0	0	1	1
15.0 IPS	0	1	0	2
18.75 IPS	0	1	1	3
25 IPS	1	0	0	4
37.5 IPS	1	0	1	5
45.0 IPS	1	1	0	6
75.0 IPS	1	1	1	7

R9 = SUBROUTINE VARIABLE
R8 = 800 BPI TIMER RATE
R7 = DENSITY RATE
R6 = WRITE CRC
R5 = READ CRC NRZI
R4 = READ LRC
R3 = COMMAND
R2 = SCRATCH FFF
R1 = SCRATCH FFF
R0 = SCRATCH FFF

Table 4-2A. Basic Program, Model 9219 Formatter, Page 1 of 2 (For 149-4801-20X PROMs, Rev. E)

COMMAND TO MTT	I_{11}	CM7 I_{10}	I_9	I_8	
READ FWD	1	0	0	0	800
WRITE ERASE	1	0	1	0	900
READ RVS	0	1	0	0	400
	SFC	SRC	SWS		





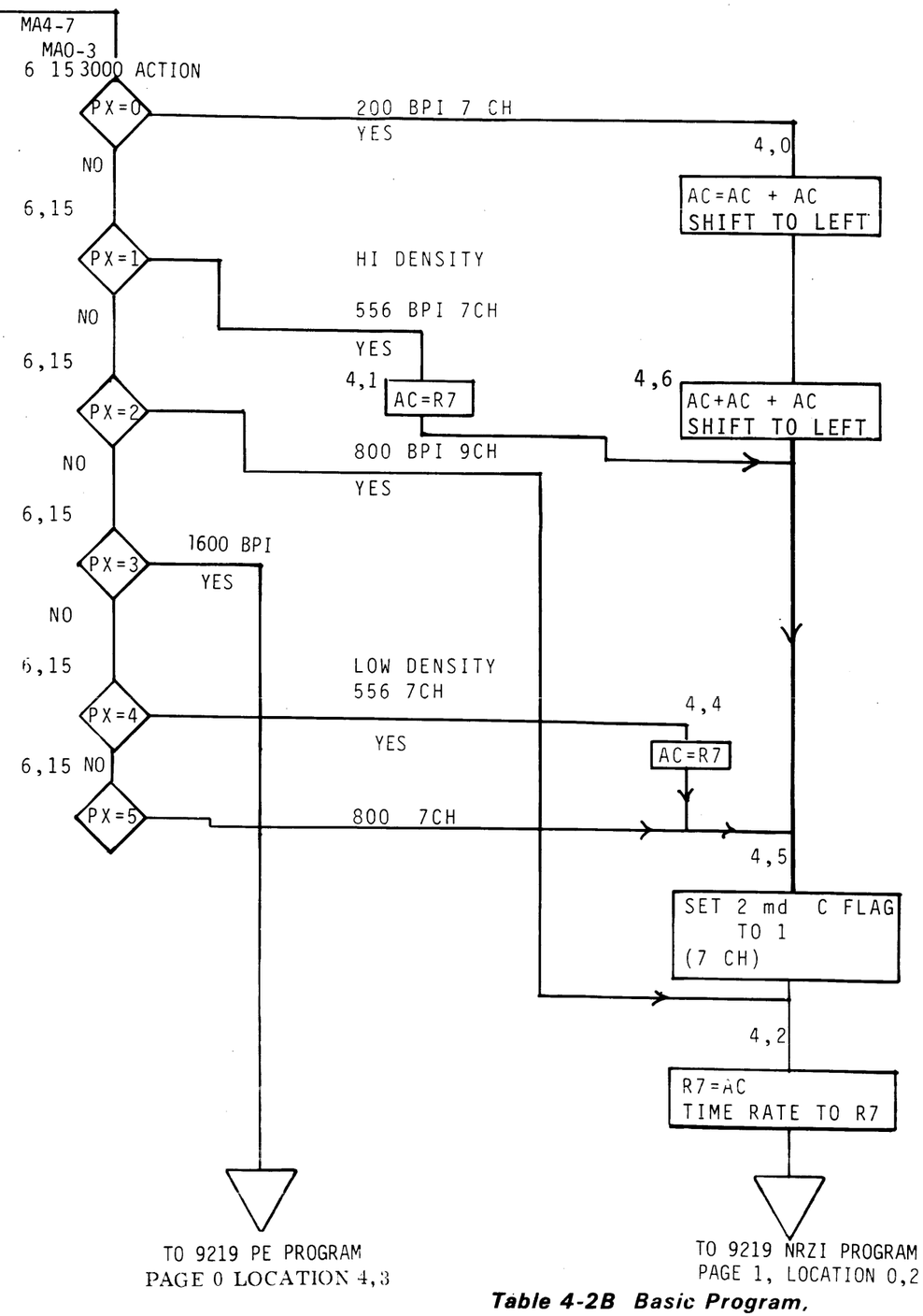
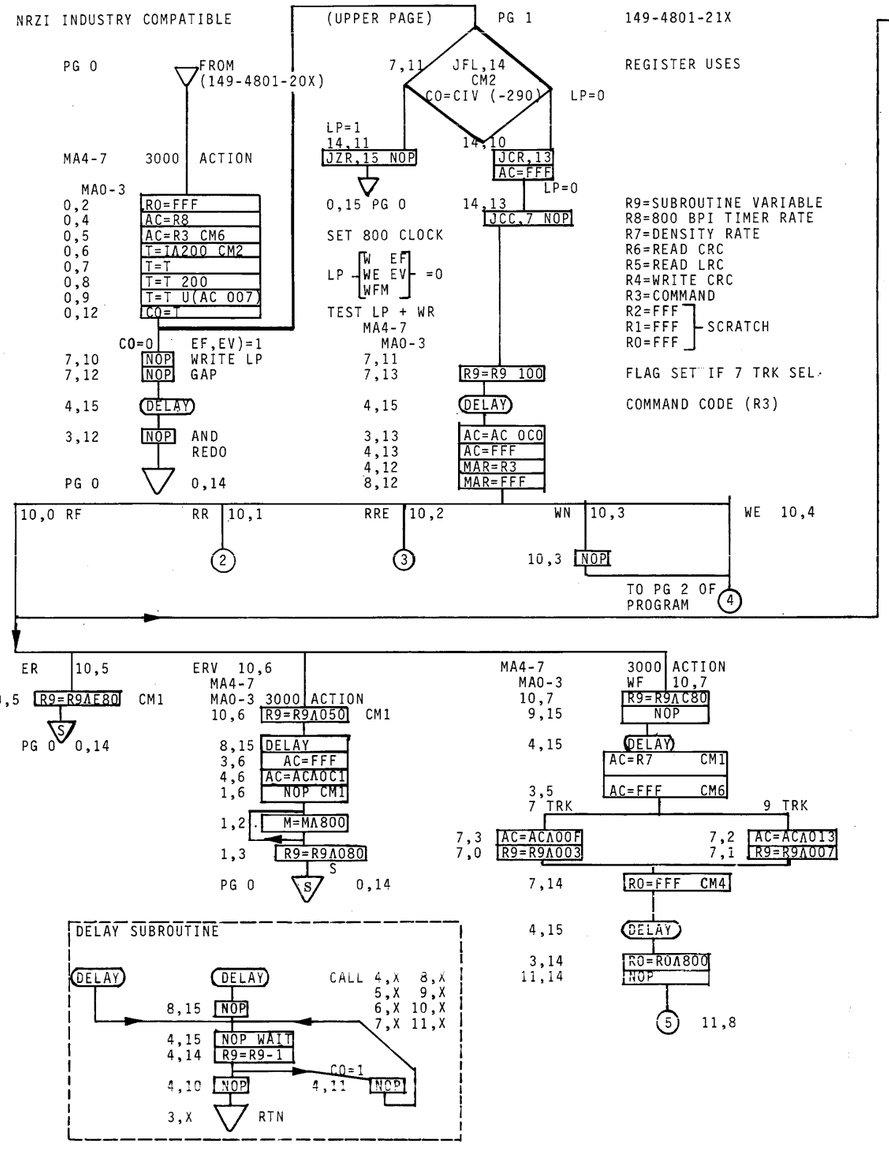
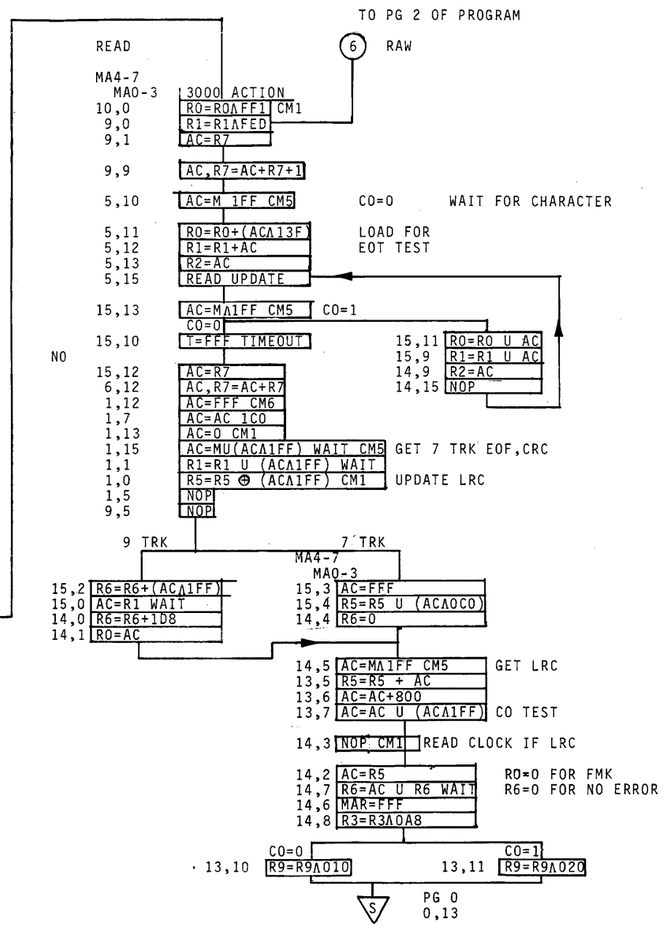


Table 4-2B Basic Program, Model 9219 Formatter Page 2 of 2 (For 149-4801-20X PROMs, Rev. E)





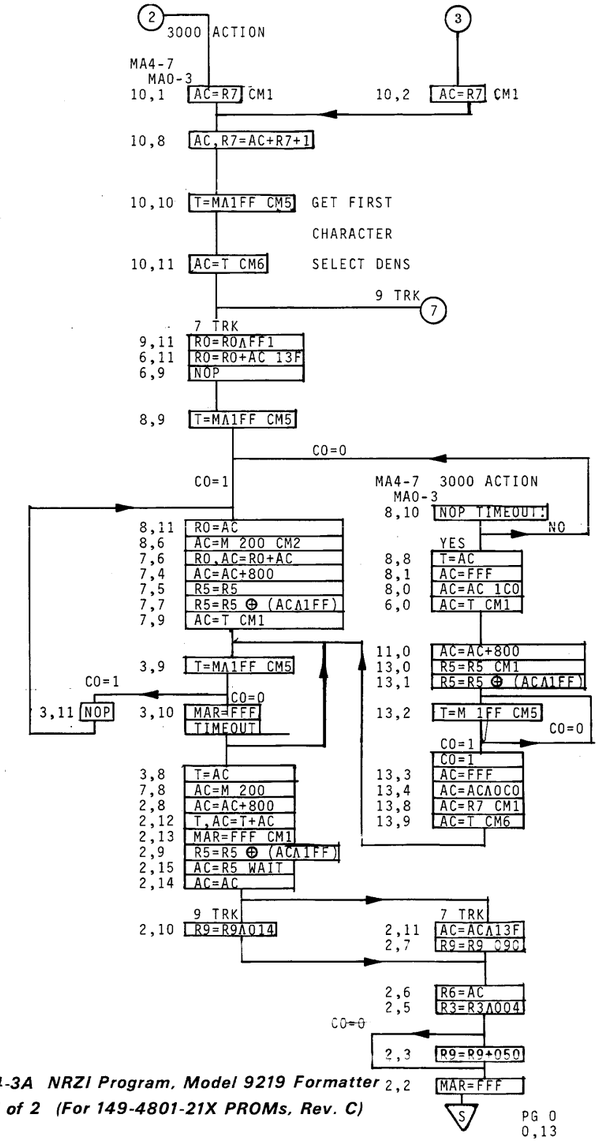


Table 4-3A NRZI Program, Model 9219 Formatter
Page 1 of 2 (For 149-4801-21X PROMs, Rev. C)

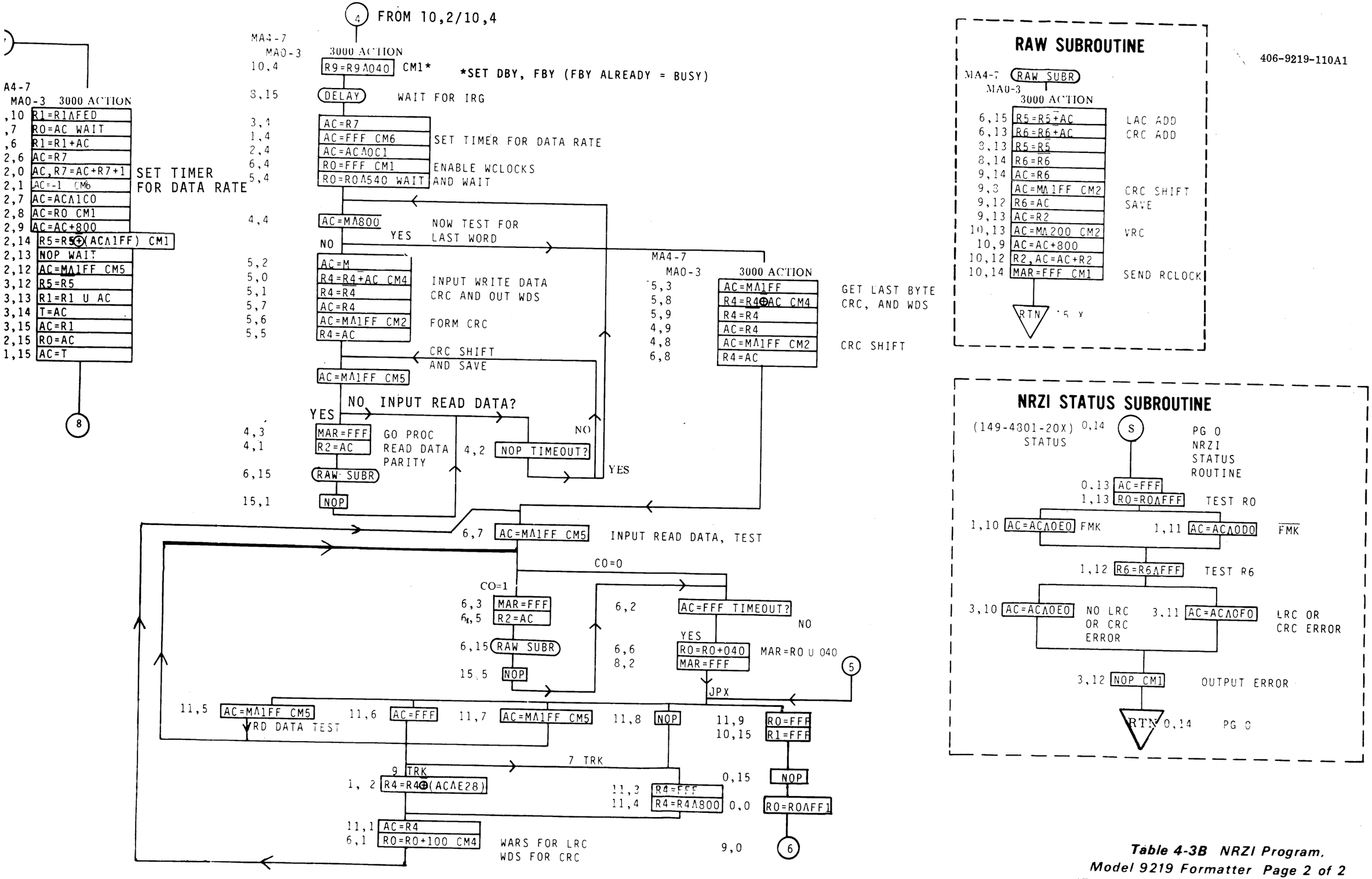


Table 4-3B NRZI Program, Model 9219 Formatter Page 2 of 2 (For 149-4801-21X PROMs, Rev. C)

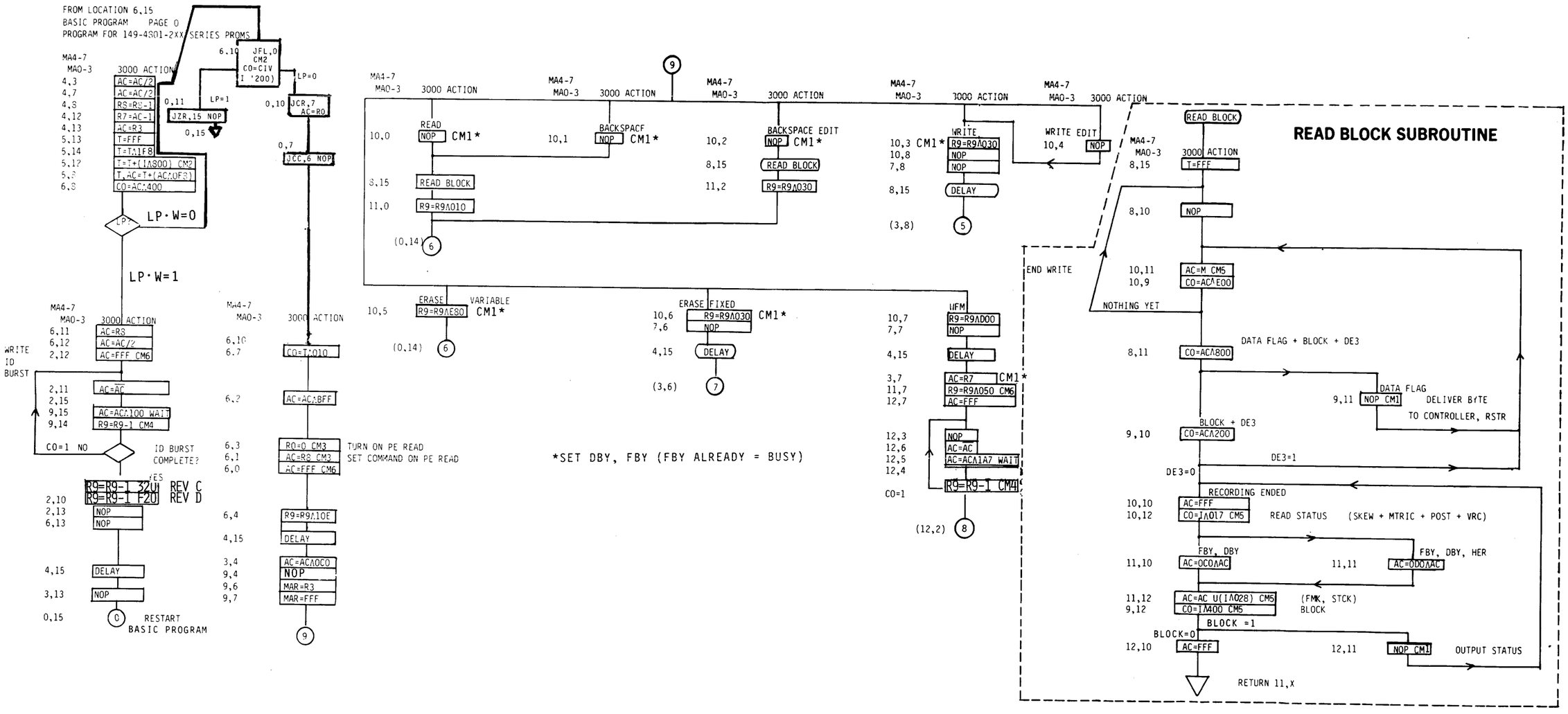


Table 4-4A PE Program, Model 9219 Formatter Page 1 of 2 (For 149-4801-20X PROMS, Rev.E)

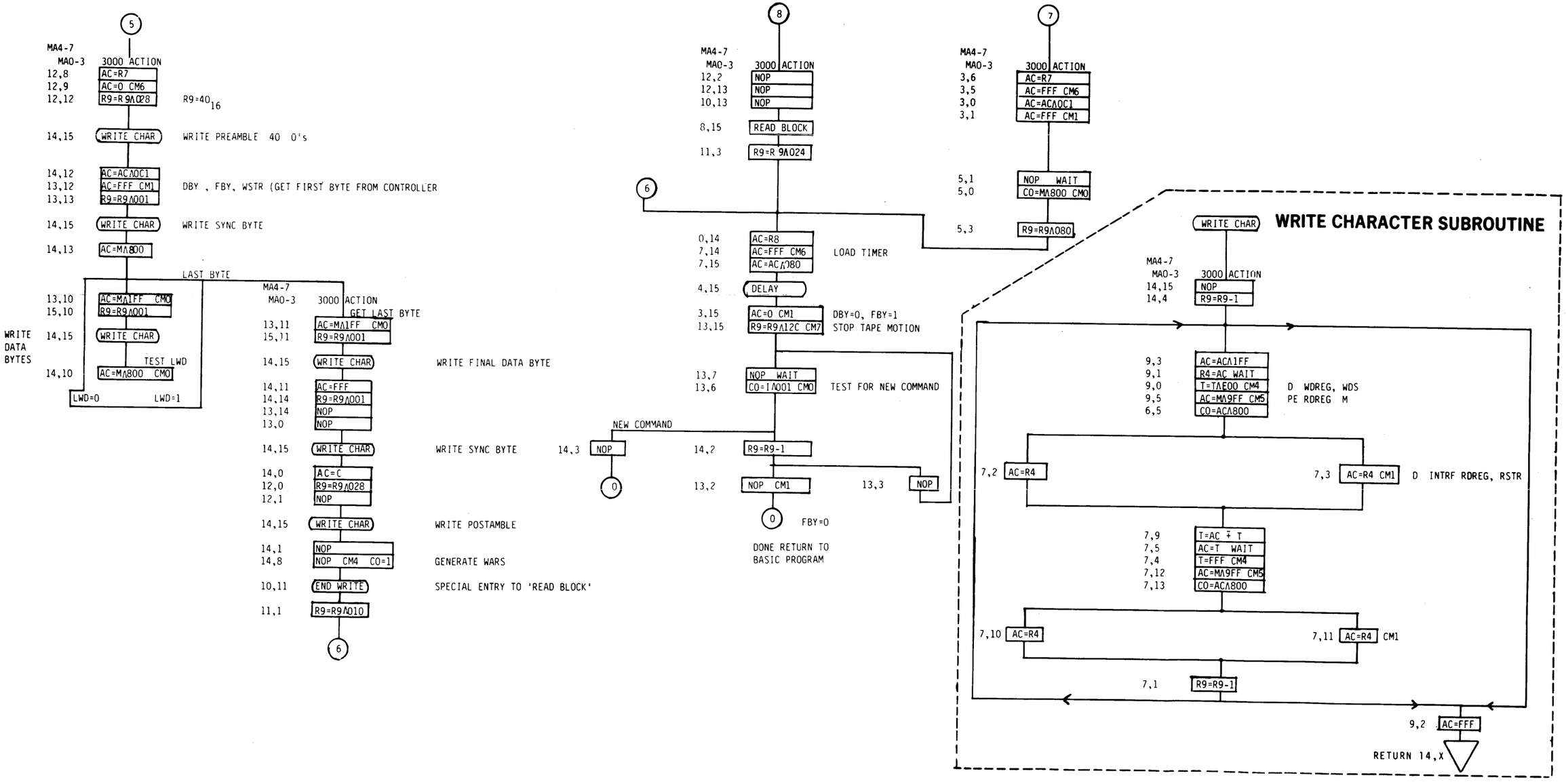


Table 4-4B PE Program, Model 9219 Formatter Page 2 of 2 (For 149-4801-20X PROMs Rev E)

4632/4832 MICROPROCESSOR COMMAND SUMMARY

LINE	CM2 TAPE UNIT STATUS AND PARITY I BUS	M BUS	CM5 READ DATA (NRZI) I BUS	M BUS	
0	0	D1	0	RD CH 7	
1	0	D2	0	RD CH 6	
2	0	D0 + D3	0	RD CH 5	
3	0	D0 + D4	0	RD CH 4	
4	TRNG	D0 + D5	0	RD CH 3	
5	ONL	D0 + D6	0	RD CH 2	
6	EOT	D7	0	RD CH 1	0 IF 7 TRK
7	HDI	D8	0	RD CH 0	0 IF 7 TRK *
8	FPT	D0	0	RD CH P	
9	LDP	1 + (D0+D1+...D8)	0	0	
10	RWD	0	0	0	
11	RDY	0	0	0	

MUST BE ENABLED BY CM3 $\overline{D0}$; DISABLE = CM3 D0. M BUS CLEARED BY CM5 WITH 3002 CARRY MAYBE FORCED TO ONE IF 7 TRK EVEN PARITY BY ASSOCIATED INTERFACE BOARD.

LINE	CM3 DEVICE SELECT D BUS			CM4 WRITE DATA D BUS
0	0 FOR NRZI; 1 FOR 1600 BPI			CH 7 WRITE
1	SEL			CH 6 WRITE
2	SEL	SELECT INTERFACE CODE		CH 5 WRITE
3	SEL			CH 4 WRITE
4	X			CH 3 WRITE
5	X			CH 2 WRITE
6	X			CH 1 WRITE
7	X			CH 0 WRITE
8	IF 1600	FWD SELECT	DEFAULT	CH P WRITE
9	BPI	WRITE DATA IN	1	X
10	SELECTED	HIGH SPEED	0	X
11	AND IF	NO SPEED	0	0: TO ENABLE WCLOCK
	CM3 D0	CORRECTION	0	1: TO OUTPUT WARS

LINE	CM6 SET PROGRAMABLE DIVIDER AND RESET D BUS	D BUS	CM7 SELECT AND SET A BUS	
0	COUNT LSB	CYCLE TIME	X	SELECT UNIT CODE LSB
1	COUNT	.69444 (COUNT+1) usec	X	SELECT UNIT CODE
2	COUNT		X	SELECT UNIT CODE MSB
3	COUNT	CYCLE INSTRUCTION COUNT=2 COUNT + 2	X	ENABLE SELECT
4	COUNT X	X		
5	COUNT	NEXT INTERPRUPT=	X	X
6	COUNT	2 COUNT + 3	OFC	X
7	COUNT RWC	X		
8	COUNT	NEXT STROBE=:	HDS	X
9	COUNT	FROM @ 3 COUNT	SWS	X
10	COUNT	THRU @ 3 COUNT+2	SRC	X
11	COUNT MSB		SFC	X

INTERRUPTS ARE CLEARED BY FORCE EVEN ROM COMMANDS OR BY CM6. STROBES ARE 1 usec WIDE

(FORCE EVEN QUED INTERRUPT) CAUSE ACO (3001 INPUT LSB) TO BE 0, USUALLY CAUSING A JUMP TO AN EVEN ROW OR COLUMN

Table 4-8 Type 4632/4832 Microprocessor Command Summary

SECTION V

PARTS IDENTIFICATION

5.1 SPARE PARTS ORDERING INFORMATION

This section describes the replaceable parts in your tape unit which are available only from Kennedy Company. Many parts of the unit are common commercial parts which can be obtained directly from the manufacturer.

The serial number and part number of the formatter are the keys to numerous engineering details applying to your unit. These numbers are located on the serial number tag located on the rear panel of the unit. When ordering spare parts, accessories, or tools, always specify the serial number and part number of your unit.

Changes to Kennedy units are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. If a part you have ordered has been replaced by a new part, a Kennedy representative will contact you concerning any change in part number.

All parts orders should be addressed directly to Kennedy Company, Parts Order Department, 540 West Woodbury Road, Altadena, Ca 91001, telephone (213) 798-0953, TWX 910-588-3751.

5.2 IN-WARRANTY REPAIR PARTS ORDERING INFORMATION

Repair parts for in-warranty units are made available on an exchange basis through the Kennedy Company Customer Engineering Department.

The serial number and part number of the formatter are necessary in order to insure shipment of the proper replacement parts.

All inquiries should be directed to Kennedy Company, Customer Engineering Department, 540 West Woodbury Road, Altadena, Ca 91001, telephone (213) 798-0953, TWX 910-588-3751.

5.3 EXPORT ORDERS

Customers outside the United States and Canada are served by Kennedy Company international sales agents. All correspondence regarding your formatter should be directed to your sales agent. If you prefer, correspondence may be addressed directly to Kennedy Company, Parts Order Department, 540 West Woodbury Road, Altadena, Ca 91001, TWX 910-588-3751, cable KENNEDYCO.

5.4 ILLUSTRATED PARTS LIST

To assist in parts identification, an illustrated parts list is included with references to photographs of the machine. Part numbers beginning with an 8 or 198 are recommended spare parts. Kennedy Company recommends that these parts be ordered as spares to minimize machine downtime due to equipment failure.

5.5 FIELD KITS

Some replacement components may be supplied in the form of repair or field change kits. The repair kits contain parts that are matched or assembled and adjusted at the factory because of complexity or to aid the field technician. The components ordered as field kits either by correspondence with Kennedy service engineers or by direct order will be supplied with complete installation instructions. The change kits are intended for standard or special options not originally included in the unit.

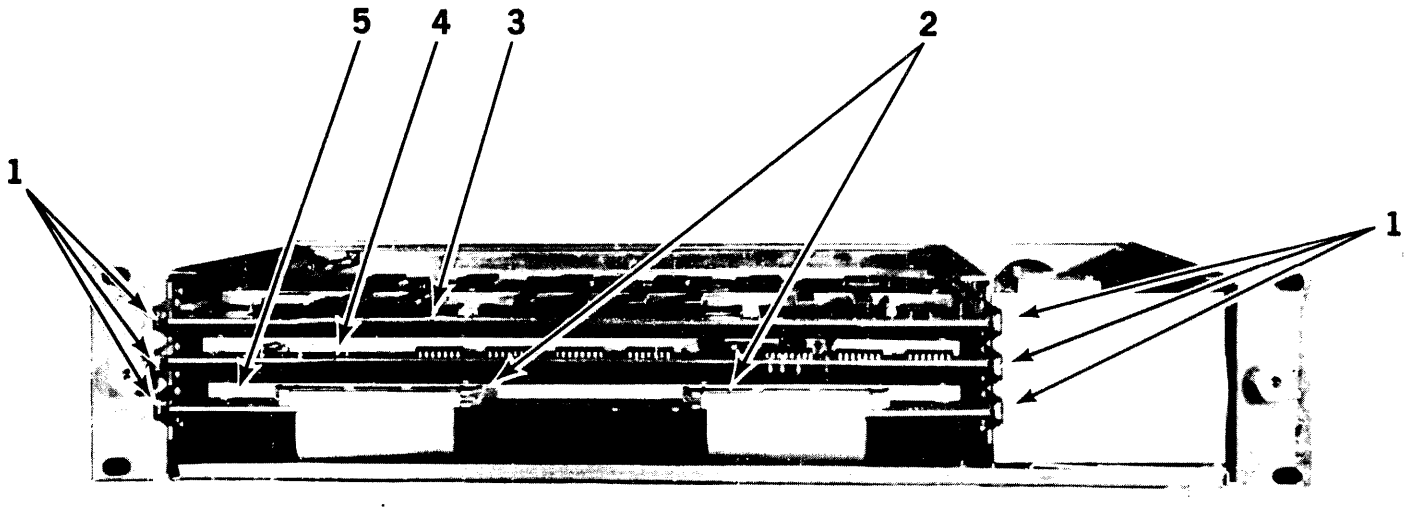


FIGURE 5-1. MODEL 9219 FORMATTER FRONT VIEW (TOP PANEL; FRONT PANEL REMOVED)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-1

Item No.	Part No.	Description	Qty	Notes
5-1-1	125-0083-004	Card Guide	6	
5-1-2	190-4767-501	Cable Connector Assy	2	
5-1-3	190-4657-xxx	PC Read PC Board Assy		1
5-1-4	190-4632-xxx	Microprocessor PC Board Assy		1
5-1-4	190-4832-xxx	Microprocessor PC Board Assy (125 ips models)		1
5-1-5	190-4831-xxx	Formatter Interface Board		1

NOTE

1. Refer to circuit board to determine correct dash number when ordering.

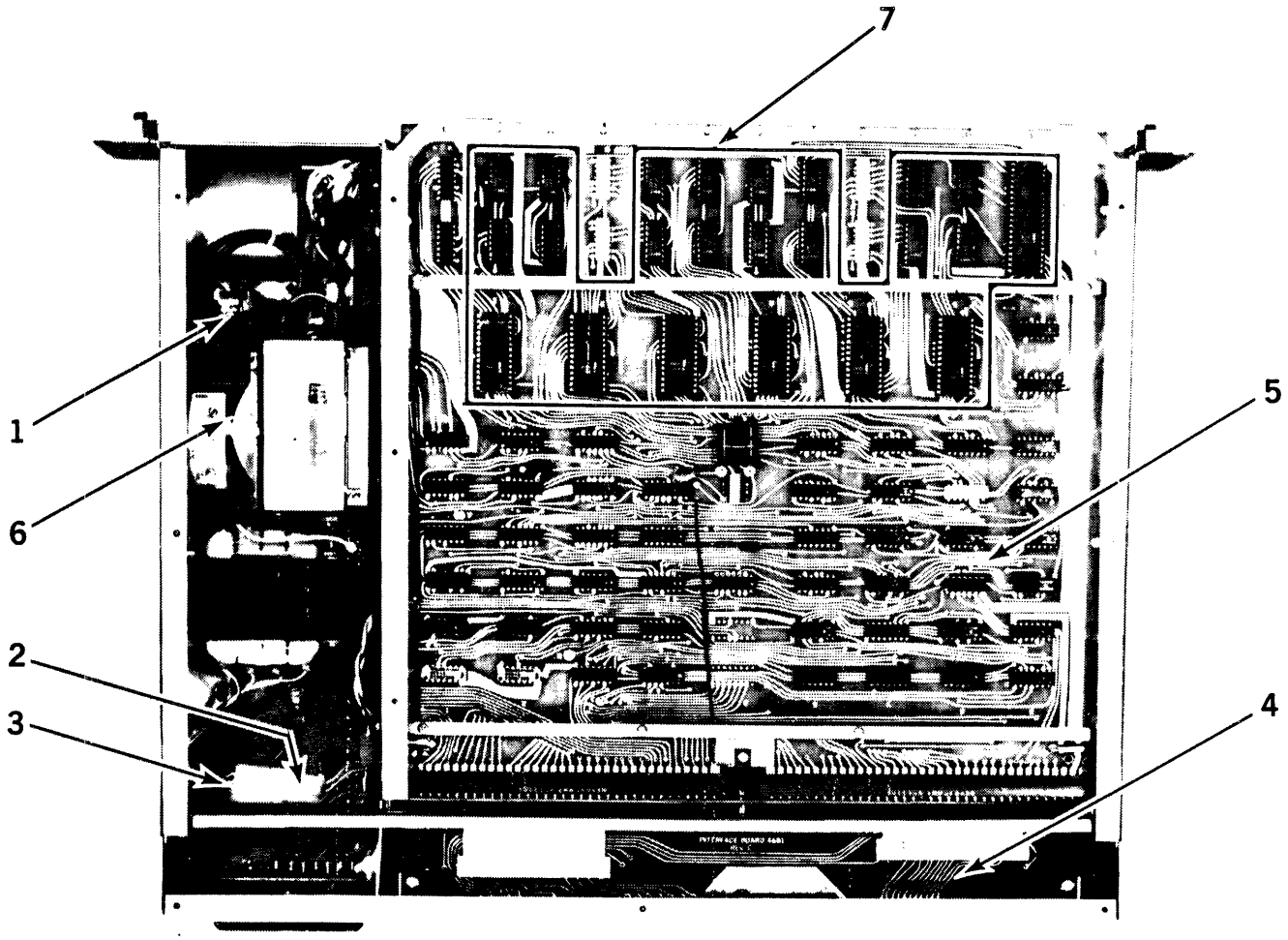


FIGURE 5-2. MODEL 9219 FORMATTER TOP VIEW (TOP COVER REMOVED)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-2

Item No.	Part No.	Description	Notes
5-2-1	140-0006-001	Power Supply - Sawyer	
5-2-2	121-0126-001	Five Pin Molex Receptacle	
5-2-3	121-0126-002	Five Pin Molex Plug	
5-2-4	190-4681-001	Interface PC Board Assy	
5-2-5	190-4611-001	Master PC Board Assy	
5-2-6	125-0032-001	Fan, Rotron PN LY2A1	2
5-2-7	198-0073-001	PROM Repl Kit 4632-007 Microprocessor Board	1
5-2-7	198-0074-001	PROM Repl Kit 4632-008 Microprocessor Board	1
5-2-7	198-0077-001	PROM Repl Kit 4832-007 Microprocessor Board	1
5-2-7	198-0087-001	PROM Repl Kit 4832-008 Microprocessor Board	1

NOTES

1. Each PROM kit contains a complete set of programmed ROMs for the microprocessor board specified.
2. Fan not included in ITT/LMT units.

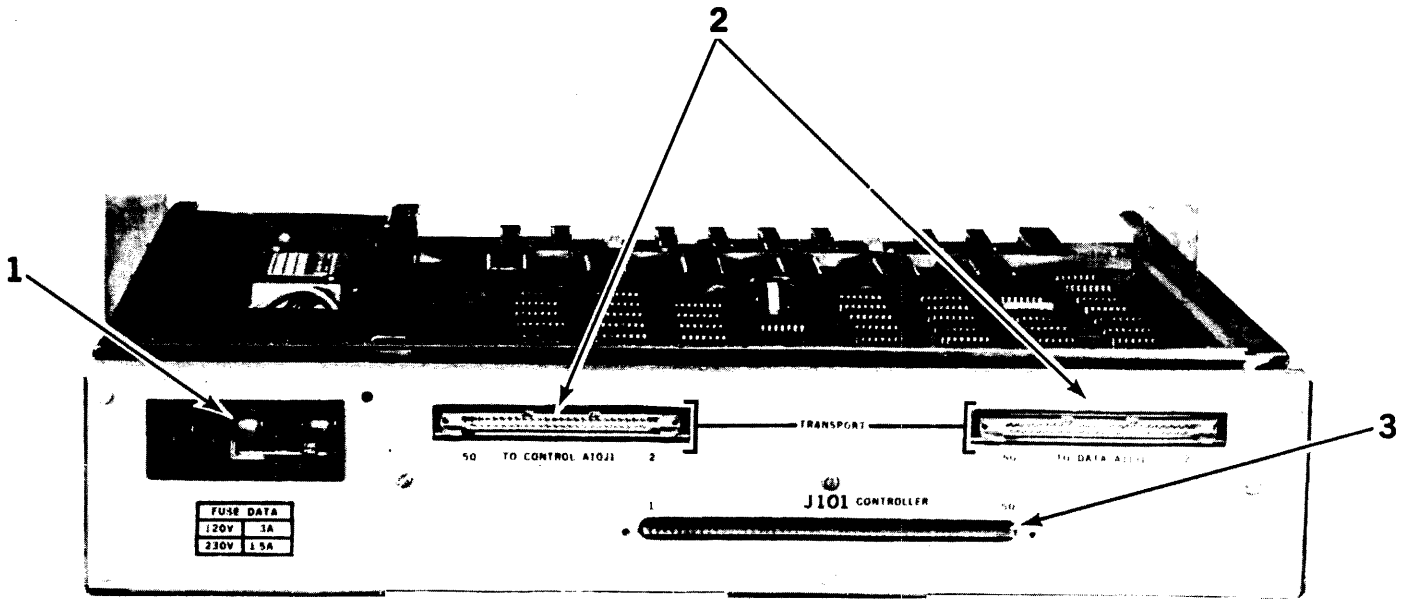


FIGURE 5-3. MODEL 9219 FORMATTER REAR VIEW (TOP COVER REMOVED)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-3

Item No.	Part No.	Description	Qty	Notes
5-3-1	151-0133-030	Fuse, Normal Blo, 3A, 250v (box of 5)	1	
5-3-1	121-0178-001	AC Connector, Voltage Selector, Fuseholder		
5-3-1	125-0068-001	Power Cord		1
5-3-2	190-4900-1xx	Cable, Formatter to Model 9000 Tape Transport		1,2,3
5-3-2	190-4970-1xx	Cable, Formatter to Model 9100, 9300, 9700 or 9800 Tape Transport		1,2,3
5-3-3	121-0159-002	PC Connector, 50 pin	2	1,3
5-3-3	190-4696-001	PEC Interface PC Board		

NOTES

1. Item(s) not shown.
2. Substitute length required for the xx in the dash number. Standard lengths are 4 feet (104) and 10 feet (110).
3. Controller to formatter cables to be fabricated by customer. Refer to Section I for pin assignments.

SECTION VI

WIRING AND SCHEMATIC DIAGRAMS

This section contains the schematic diagrams for the circuit cards used in the Model 9219, which are arranged as shown below. Electronic symbols used in the drawings conform to MIL-STD-15. Abbreviations conform to MIL-STD-12 unless otherwise specified. Logic diagrams conform to MIL-STD-806C.

System Wiring Diagrams

PROM Locations -
Type 4632 Microprocessor Board

Type 4632 Microprocessor
- Page 1, Clocks
- Page 2, Tape Unit I/O
- Page 3, ROM Control
- Page 4, Central Processor

PROM Locations -
Type 4832 Microprocessor Board

Type 4832 Microprocessor
- Page 1, Clocks
- Page 2, Tape Unit I/O
- Page 3, ROM Control
- Page 4, Central Processor

Type 4831 Interface

Type 4657 PE Read

Model 9219 Power Supply

NOTES TO SCHEMATIC SECTION

Certain conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified the resistor may be either 1/4 or 1/2 watt.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5v) and 7 (ground) for 14 pin packages, and 16 (+5v) and 8 (ground) for 16 pin packages. Some ICs — 7476, 7492, 7493 for example — have power connections on pin 5 (+5v) and pin 10 (ground). Operational amplifiers in the 8 pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

7. Abbreviations used in from and to designations are as follows:

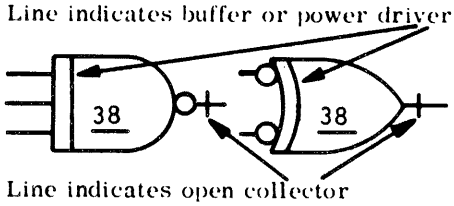
CI	Control Interface
PBC	Pushbutton Control
RG	Ramp Generator
SA	Sensor Amplifier/Driver
DT	Delay Timing
RA/CL	Read Amplifier/Clipping Level
RA	Quad Read Amplifier
WA1	Four Channel Write Amplifier
WA2	Five Channel Write Amplifier

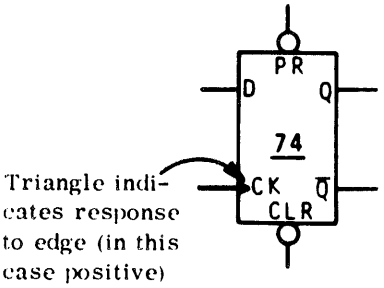
8. Positive logic is shown for all internal connections. Interface connections are zero true but the bar is omitted.

9. Integrated circuit symbols contain a circuit designator that corresponds to the number silkscreened onto the circuit module above an underlined number representing the IC type.

   The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a 00 designation indicates a 7400 quad two input NAND gate. T.I.'s complete part number is SN7400N. In multifunctional units in close proximity to each other the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

   Military Standard 806C is the base for logic symbols. Additional conventions are shown below.



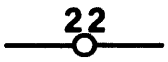


10. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

11. Unless otherwise specified, light emitting diodes are FLV102 or equivalent.

12. Module connector pins are shown as

where no further connection is shown on the schematic, and as



when there is a connection shown.

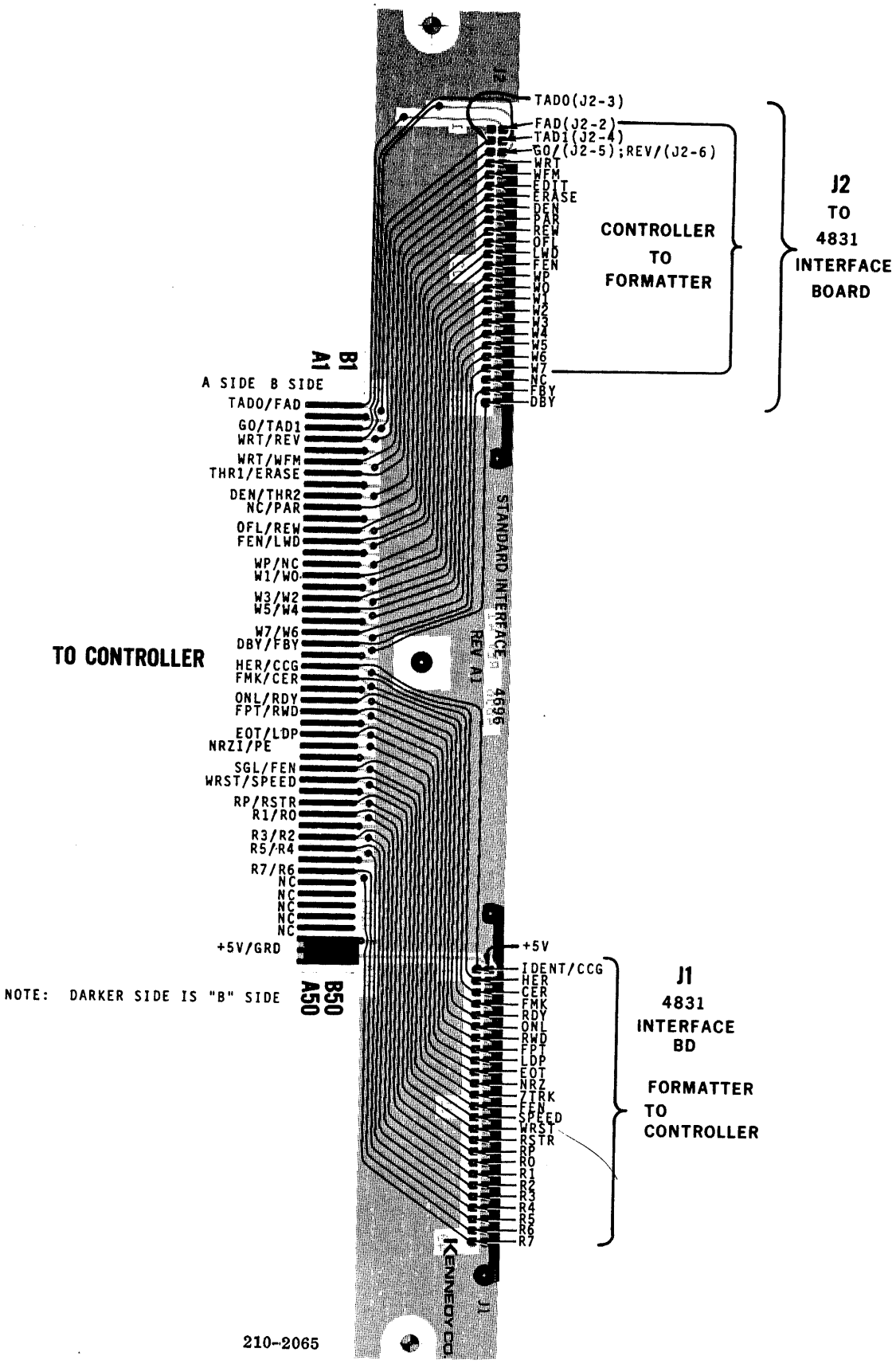
13. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown their destinations may not be shown.

14. Some schematics of modules include certain external elements which aid in understanding the circuit function. In this case all the connections to the element may not be shown in the interest of clarity.

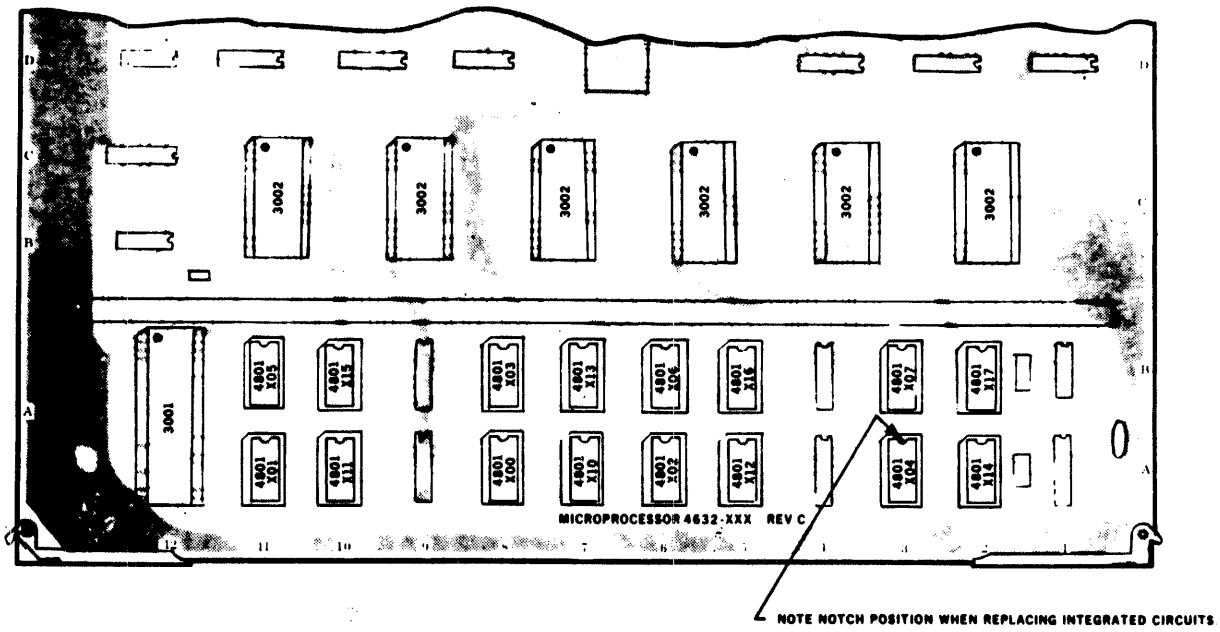
15. 

designates a test point provided on the module. Letters proceed from top to bottom of card with the ground test point, if present, as the bottommost terminal.

16. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. These are the designations on the socket. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.



Type 4696 Interface PC Board



NOTE: The different types of 4632 Microprocessor boards vary according to the programming of the Type 4801 PROM IC's. The PROM locations are indicated by the three digit PROM codes shown above. The "X" in X01, X05, etc. is replaced by a 1, 2, or 3, depending on the application for which a PROM is intended. The Type 4801 PROM dash numbers are organized as follows:

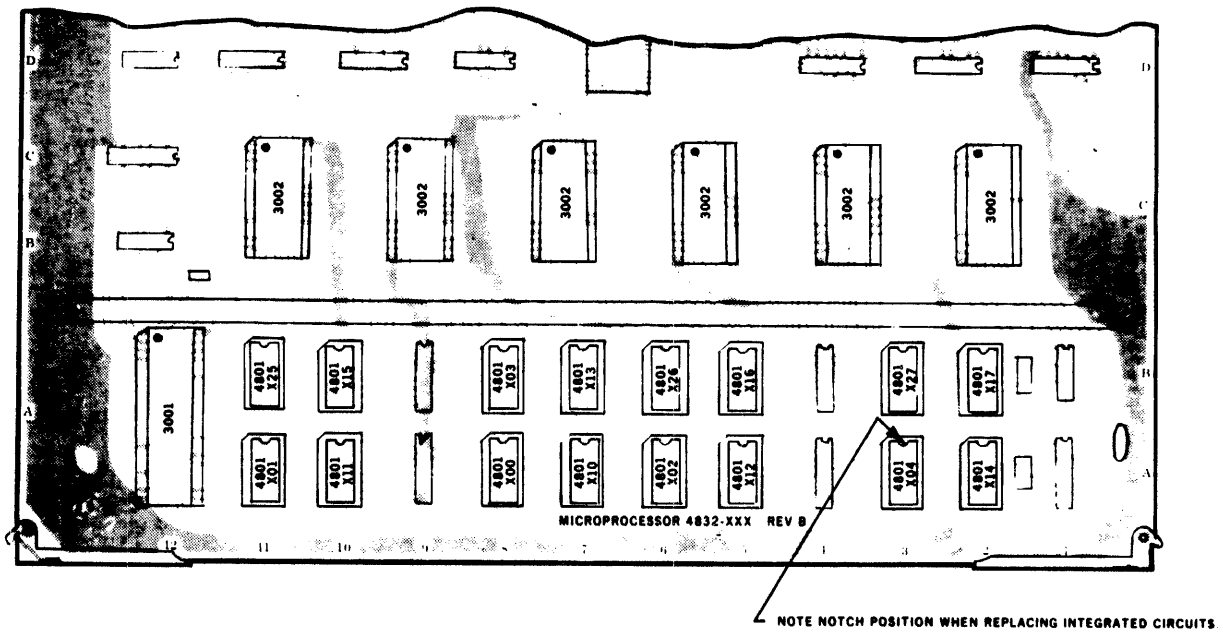
100 through 107: PROM'S used in NRZI only formatters.

100 - 107 plus 110 thru 117: PROM'S used in combination NRZI/PE formatters. (16 PROM'S required).

200 thru 207 plus 210 thru 217: PROM'S used in PEC compatible NRZI and PE formatters. (16 PROM'S required).

300 thru 307 plus 310 thru 317: PROM'S used in Read Reverse and Dead Track Register NRZI and PE formatters only.

PROM Locations - Type 4632 Microprocessor Board



NOTE: The different types of 4832 Microprocessor boards vary according to the programming of the Type 4801 PROM IC's. The PROM locations are indicated by the three digit PROM codes shown above. The "X" in X01, X25, etc. is replaced by a 1 or a 2, depending on the application for which a PROM is intended. The Type 4801 PROM dash numbers are organized as follows:

10X: NRZI PROMs

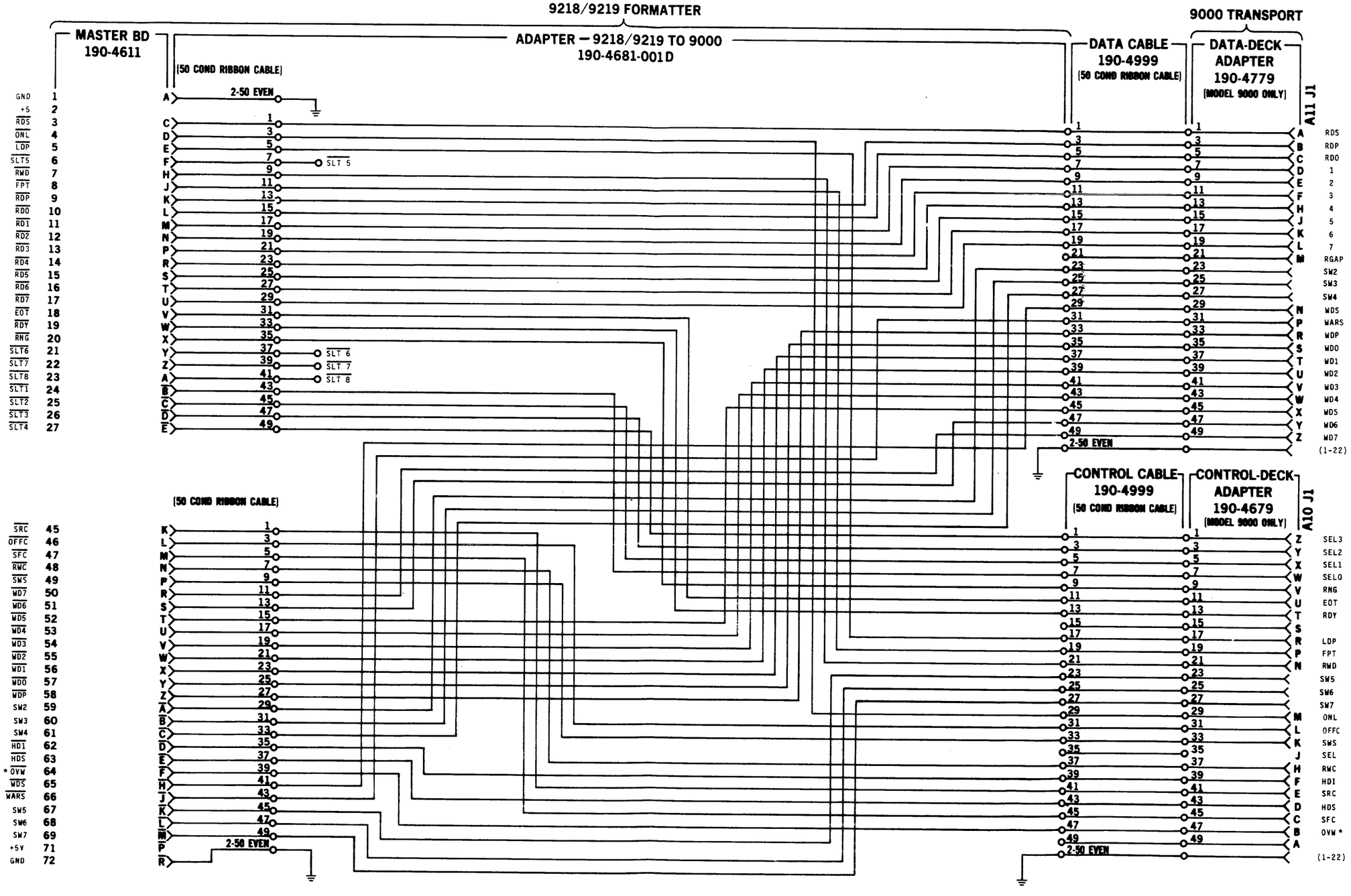
11X: PE PROMs

12X: High Speed NRZI PROMs

2XX: PROMs used in PEC compatible formatters

Eight PROMs are required for NRZI only 4832 boards; 16 PROMs are required for NRZI/PE versions.

PROM Locations - Type 4832 Microprocessor Board



* 9219 FORMATTER ONLY

SYSTEM WIRING,
9218/9219 TO 9000 SERIES
VIA RIBBON CABLE

401-4740-001E

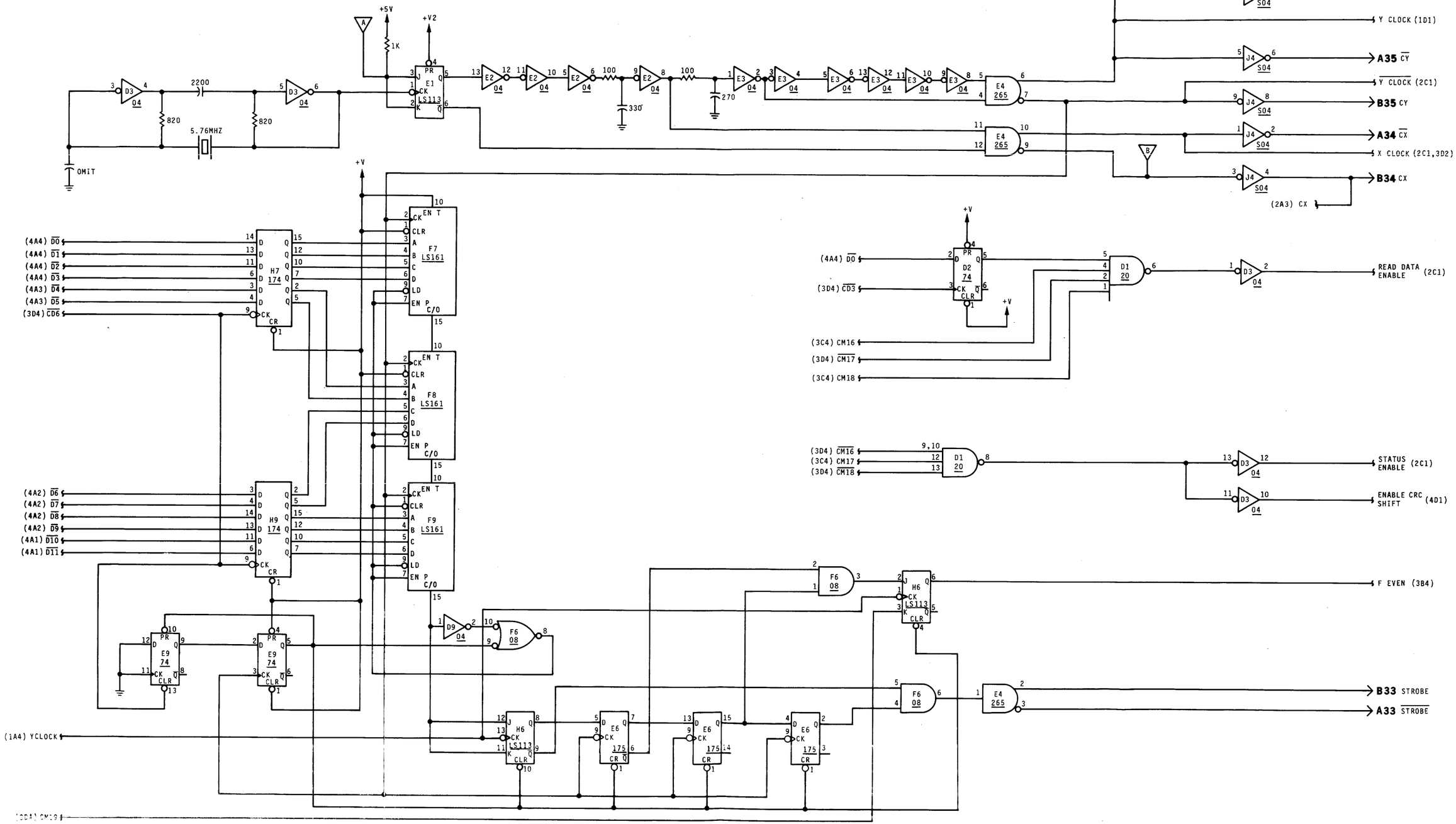
190-4740 ADAPTER PC BOARD CONNECTS 9218/9219 TO 9100/9300/ 9700/9800 INTERFACE (PART OF 190-4747 ASSEMBLY)

DASH NO.	IC1	SW2 THRU SW7	R1	ST1
-001C	OMIT	OMIT	OMIT	USED
-002D	USED	USED	USED	OMIT

* 9219 FORMATTER ONLY

9100,9300,9700 & 9800
To 9218/9219
Ribbon Cable Adapter,
Schematic Diagram

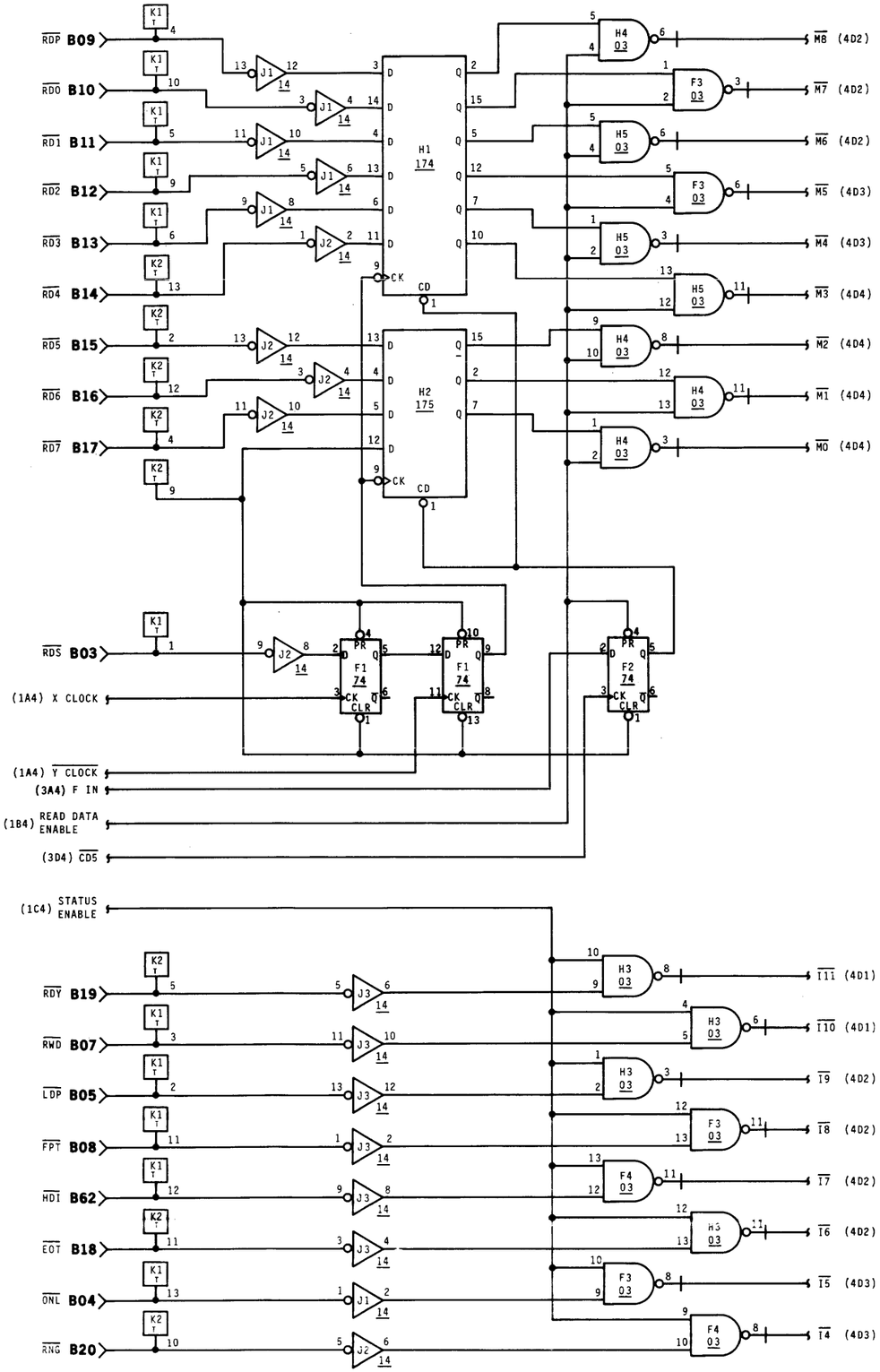
401-4632-001M

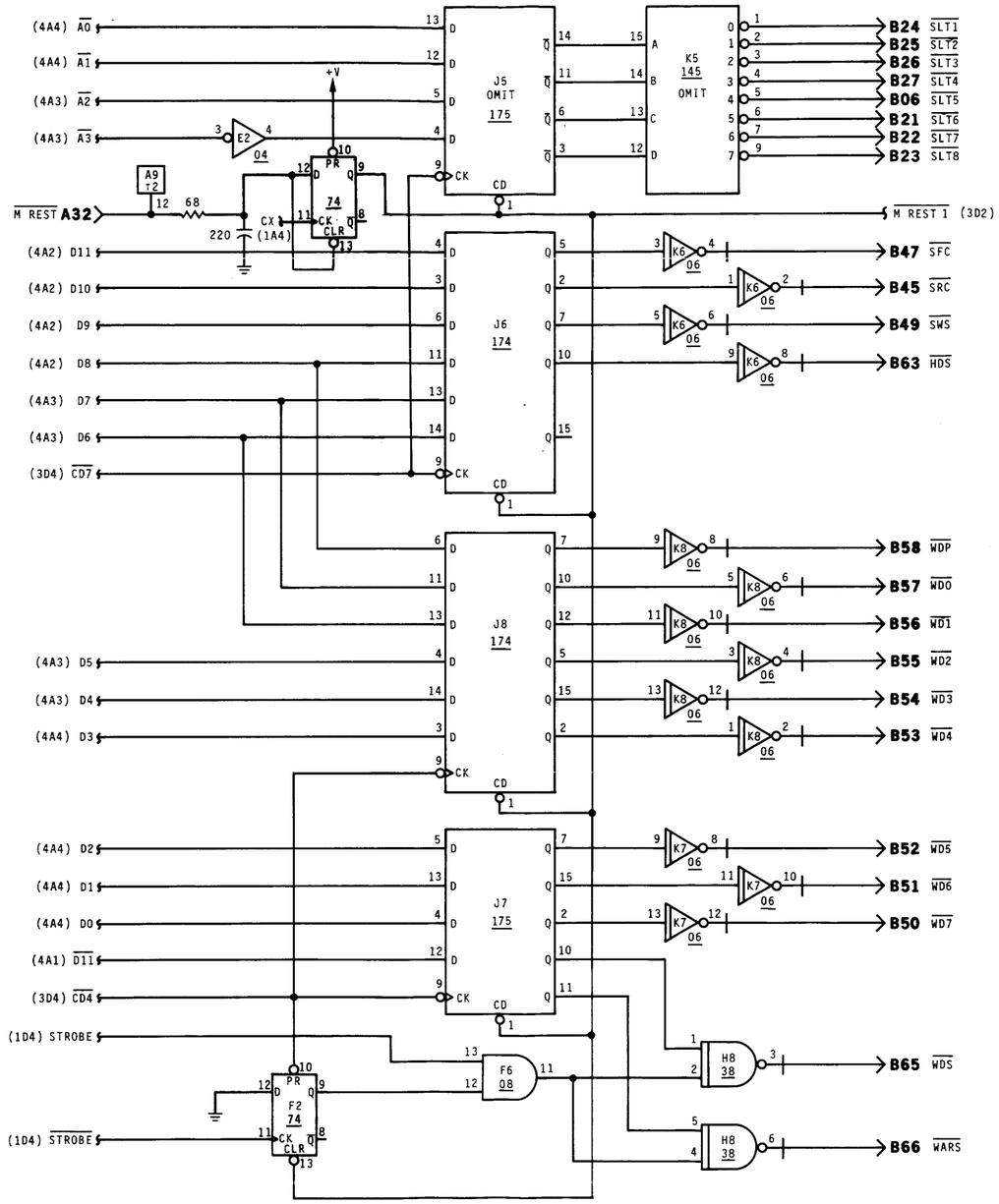


NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Micro Processor, Type 4632-001M,
(Clocks) Page 1 of 4
Schematic Diagram

401-4632-001



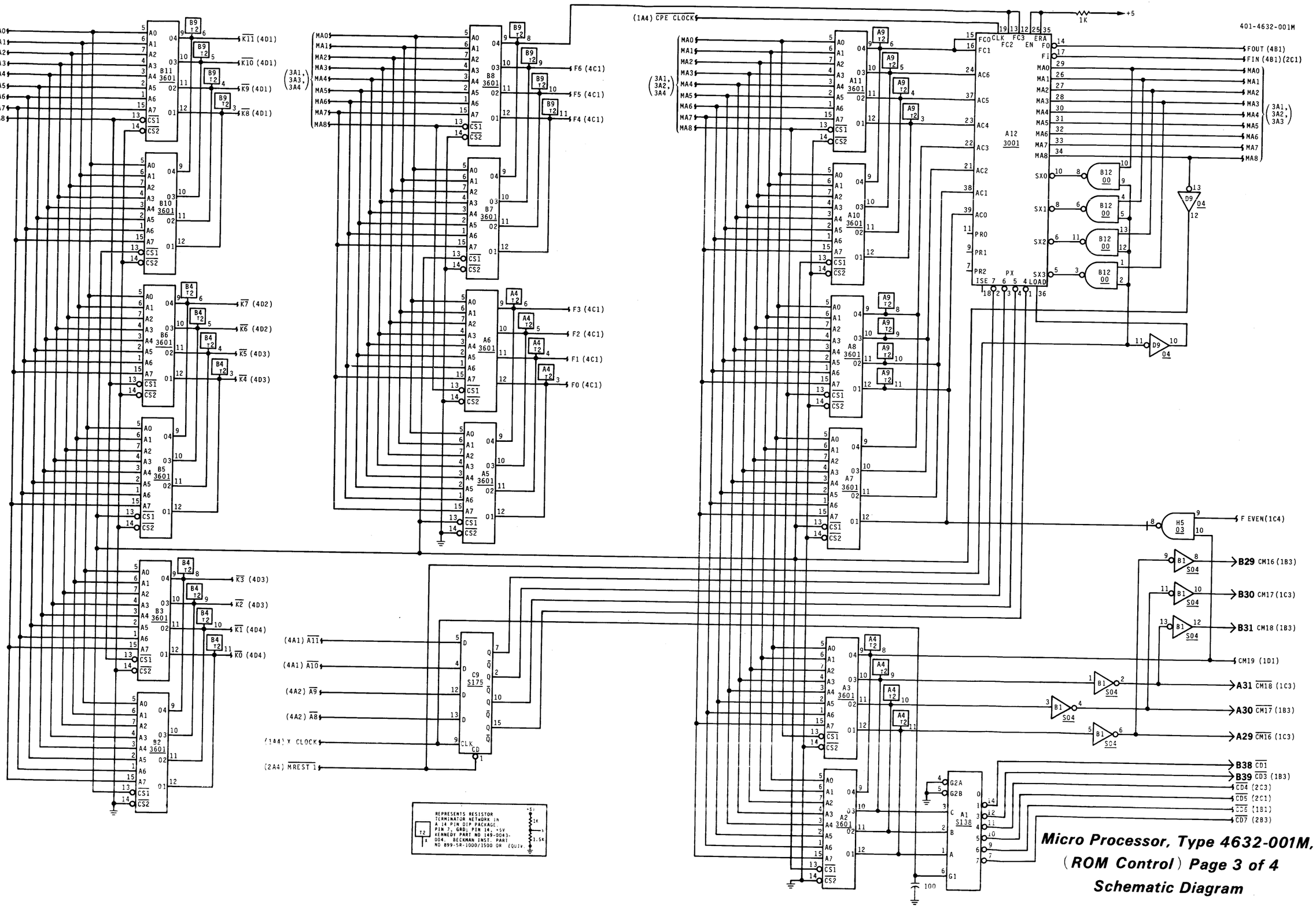


REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V. KENNEDY PART NO 149-0043-002. BECKMAN INST. PART NO 899-5R-220/330 OR EQUIV.

REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V. KENNEDY PART NO 149-0043-004. BECKMAN INST. PART NO 899-5R-1000/1500 OR EQUIV.

Micro Processor, Type 4632-001M, (Tape Unit I/O) Page 2 of 4

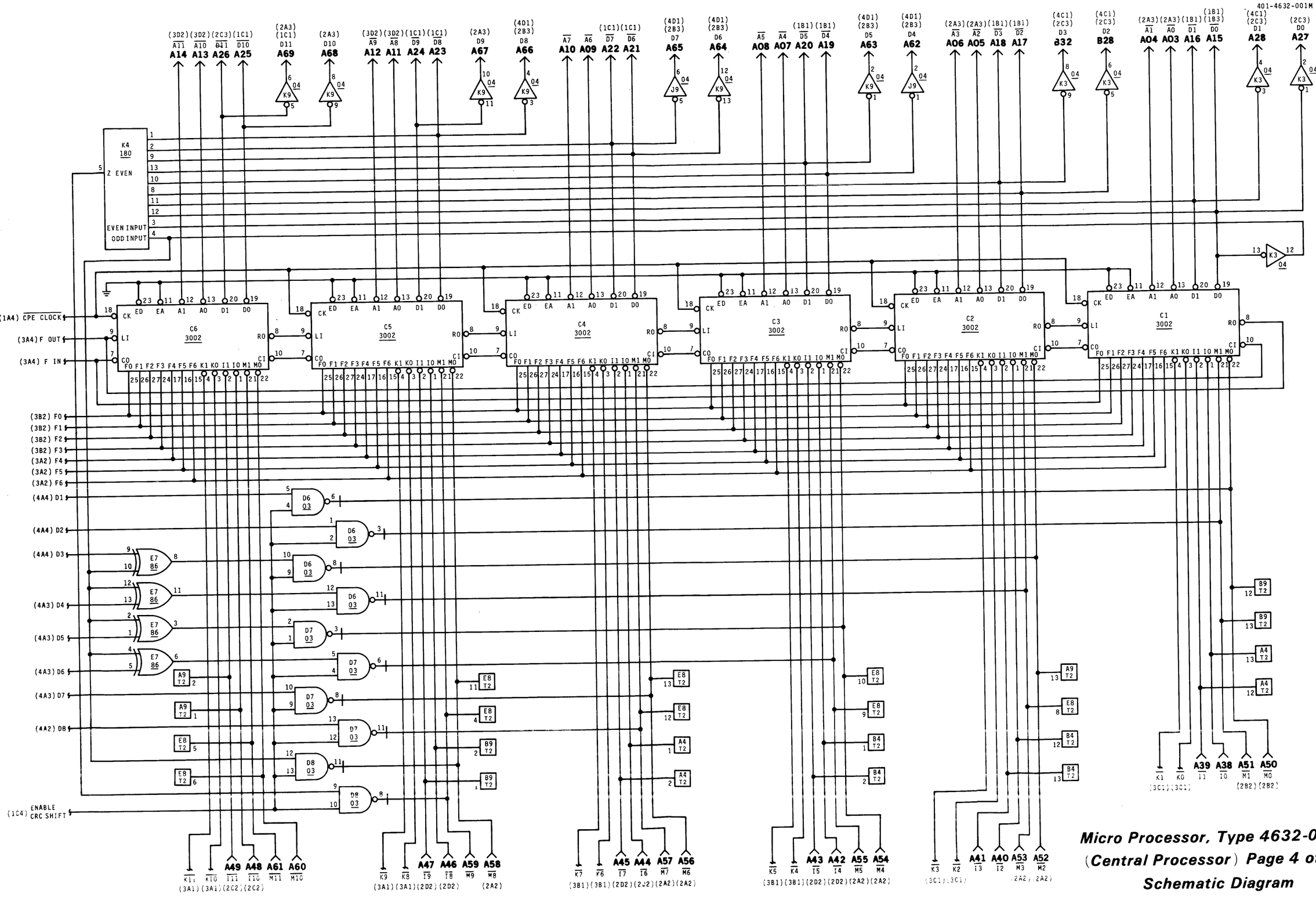
Schematic Diagram



Micro Processor, Type 4632-001M, (ROM Control) Page 3 of 4

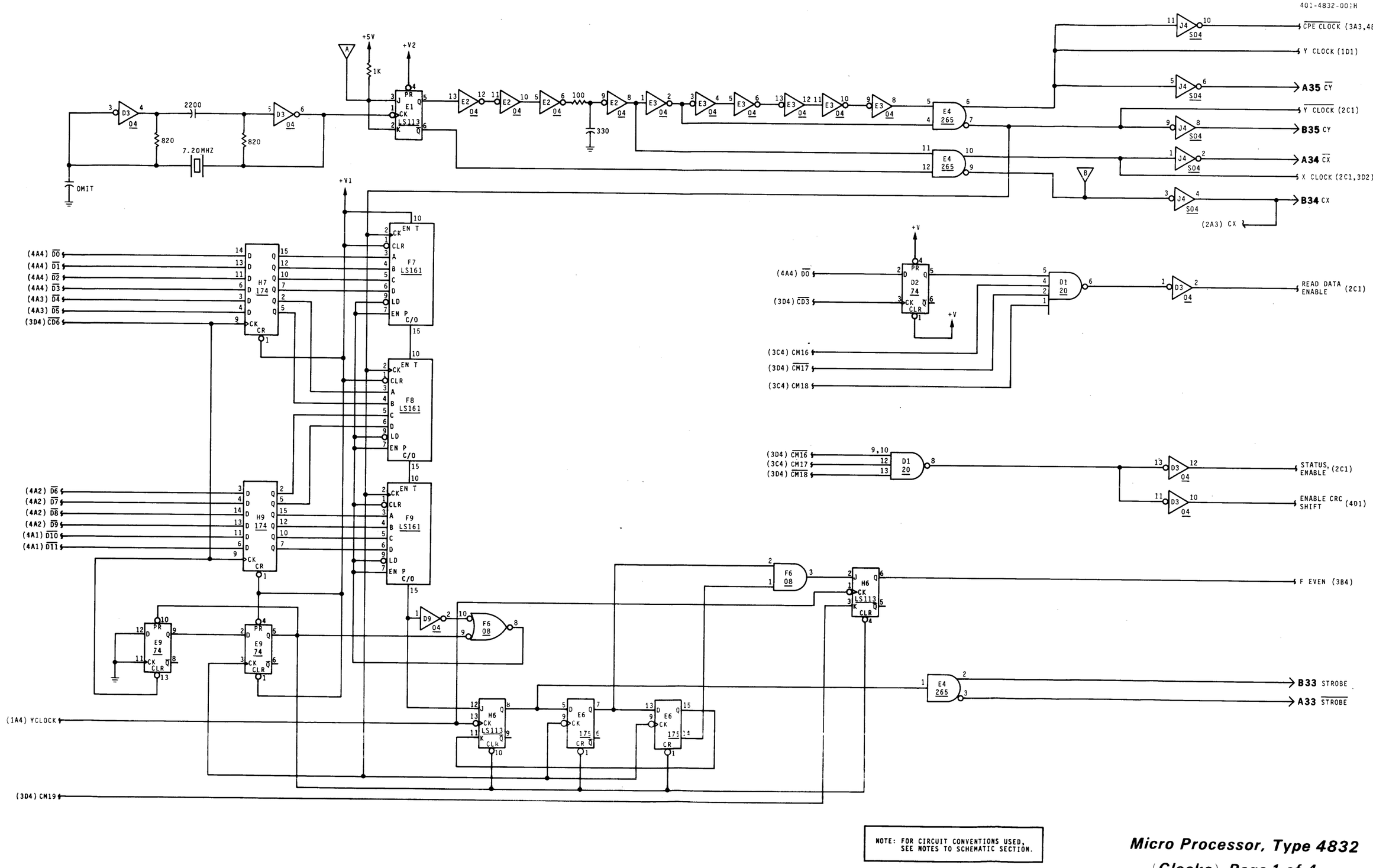
Schematic Diagram

401-4632-001M



Micro Processor, Type 4632-001M,
(Central Processor) Page 4 of 4
Schematic Diagram

401-4832-00:H

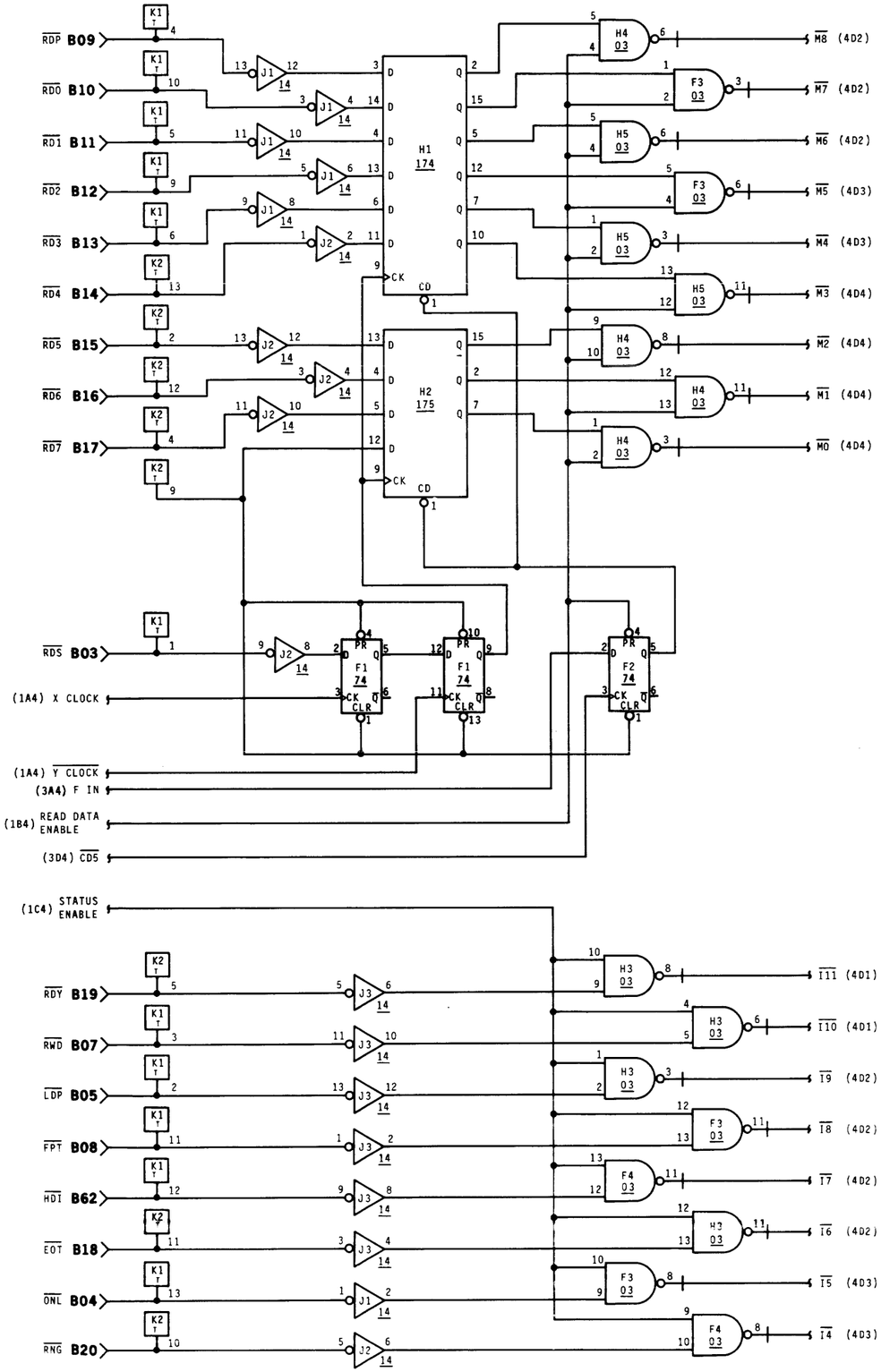


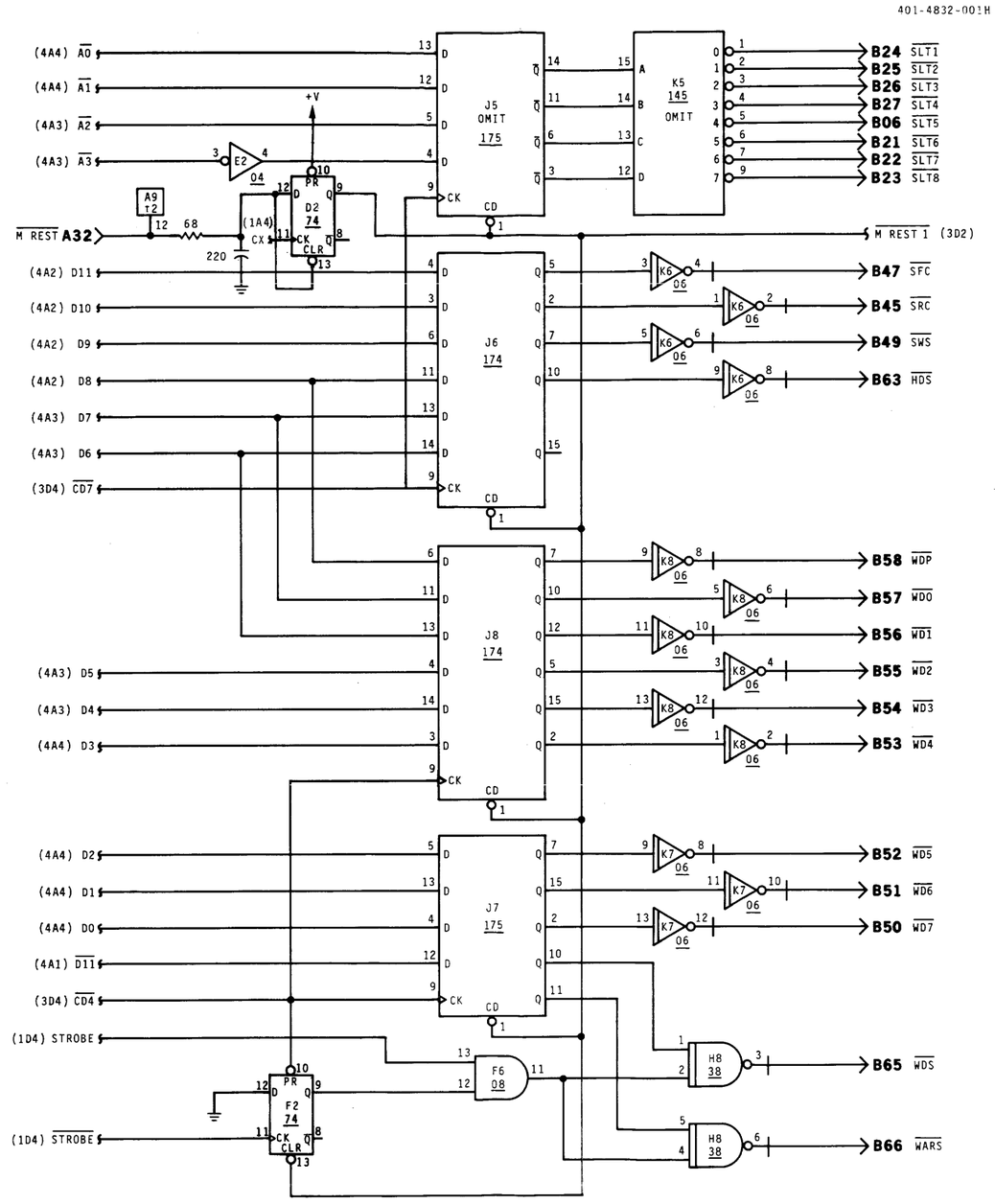
NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Micro Processor, Type 4832

(Clocks) Page 1 of 4,

Schematic Diagram

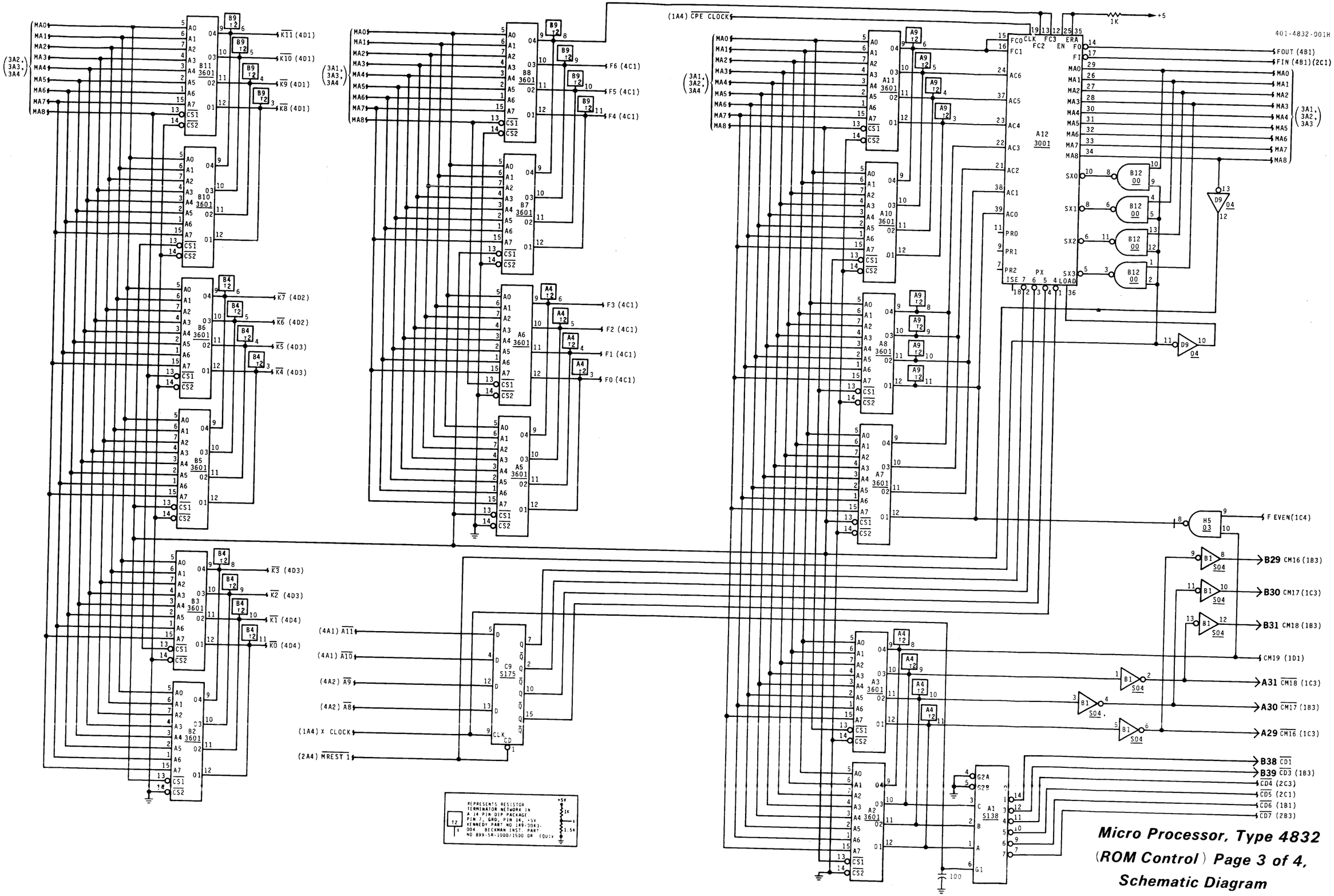




REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V. KENNEDY PART NO 149-0043-002. BECKMAN INST. PART NO 899-5R-220/330 OR EQUIV.

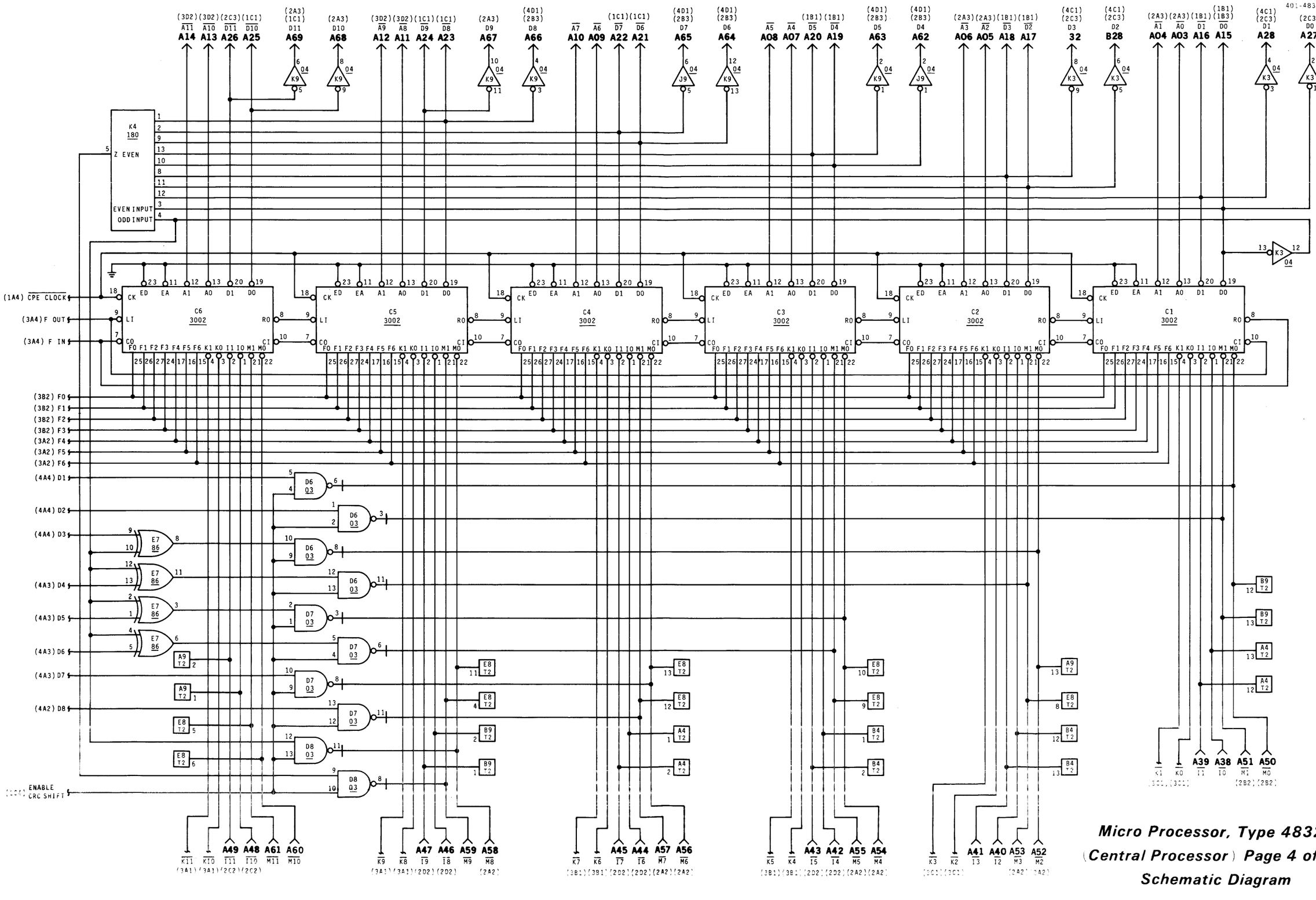
REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V. KENNEDY PART NO 149-0043-004. BECKMAN INST. PART NO 899-5R-1000/1500 OR EQUIV.

Micro Processor, Type 4832 (Tape Unit I/O) Page 2 of 4, Schematic Diagram

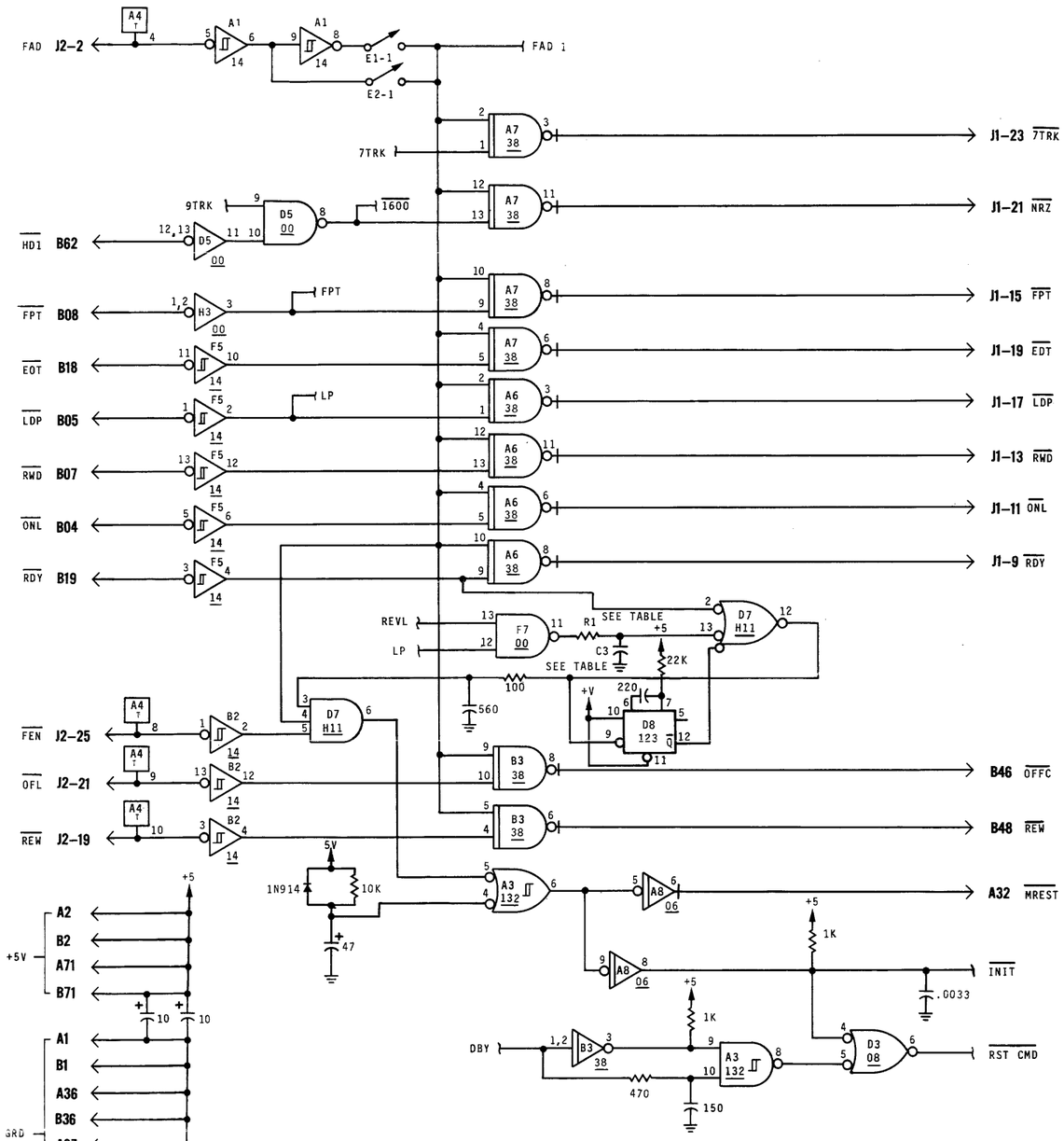


Micro Processor, Type 4832 (ROM Control) Page 3 of 4, Schematic Diagram

401-4832-001H



Micro Processor, Type 4832
(Central Processor) Page 4 of 4
Schematic Diagram



DASH NO.	ST1,ST3,ST5 ST7,ST9,ST11	ST2,ST4,ST6 ST8,ST10,ST12	ST13	ST14	SPEED SELECTED FROM	C3	R1
-001C	OMIT	STRAP	STRAP	OMIT	INTERFACE BD	OMIT	OMIT & STRAP
-002B	STRAP	OMIT	OMIT	STRAP	TAPE DRIVE	OMIT	OMIT & STRAP
-003	OMIT	STRAP	STRAP	OMIT	INTERFACE BD.	.01	220

9219 Interface, Type 4831 Schematic Diagram Sheet 1 of 2

401-4931-001H

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V. KENNEDY PART NO 149-0043-002. BECKMAN INST. PART NO 899-5R-220/330 OR EQUIV.

REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V. KENNEDY PART NO 149-0043-004. BECKMAN INST. PART NO 899-5R-1000/1500 OR EQUIV.

9219 Interface, Type, 4831

Schematic Diagram, Sheet 2of2

Input Data Transition Detectors and Multiplexers

Frame Counter, Phase Detectors, Transition Error Detect Network

401-4657-001H2

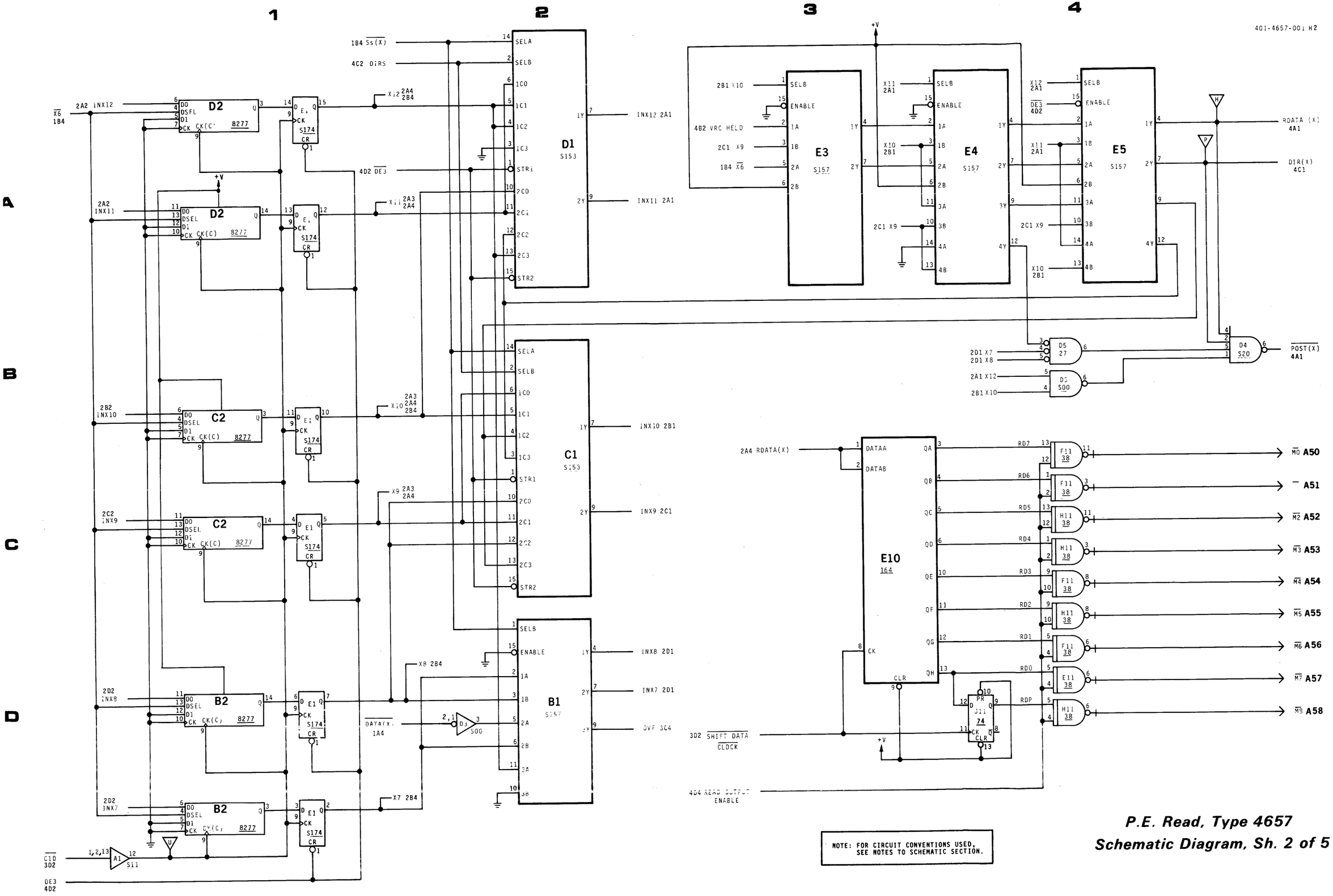
NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

DASH-XUL NOTES
X = 0 FOR STANDARD ASSEMBLY
U = UPPER SPEED, DETERMINED BY DIGIT (SEE TABLE)
L = LOW SPEED, DETERMINED BY DIGIT (SEE TABLE)
C1 = DETERMINED BY L (SEE TABLE)
C2 = SELECTED IN TEST, USE TABLE FOR APPROXIMATE VALUE
C3 = SELECTED IN TEST, USE TABLE FOR APPROXIMATE VALUE

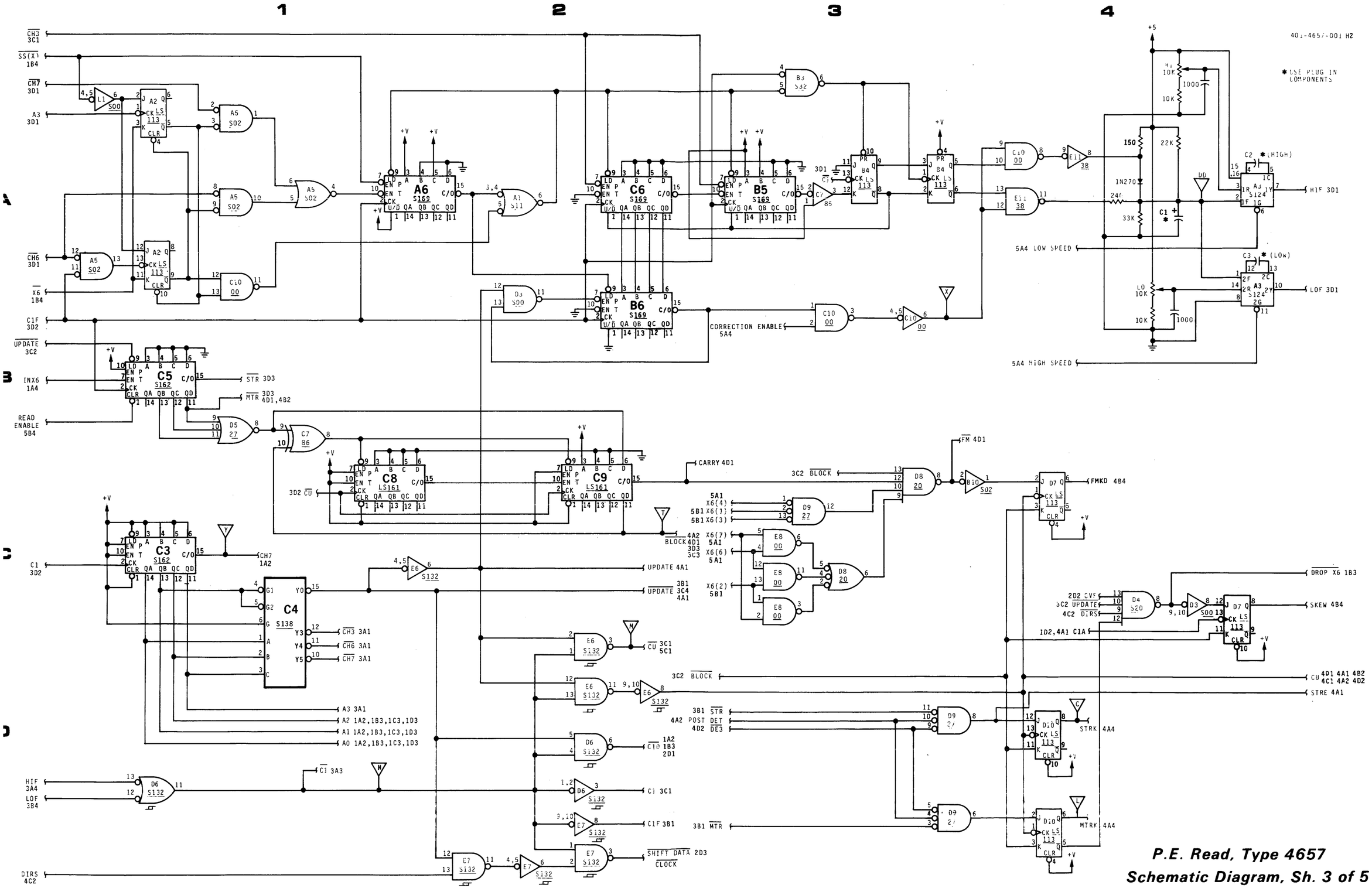
TABLE

DIGIT	SPEED	C1	C2,C3
7	75	.33	68pF
6	45	.33	110pF
5	37.5	.47	150pF
4	25	.68	220pF
3	18.75	1.0	270pF
2	15	1.0	330pF
1	12.5	1.5	430pF
0	10	1.5	510pF

P.E. Read , Type 4657
Schematic Diagram, Sh. 1 of 5

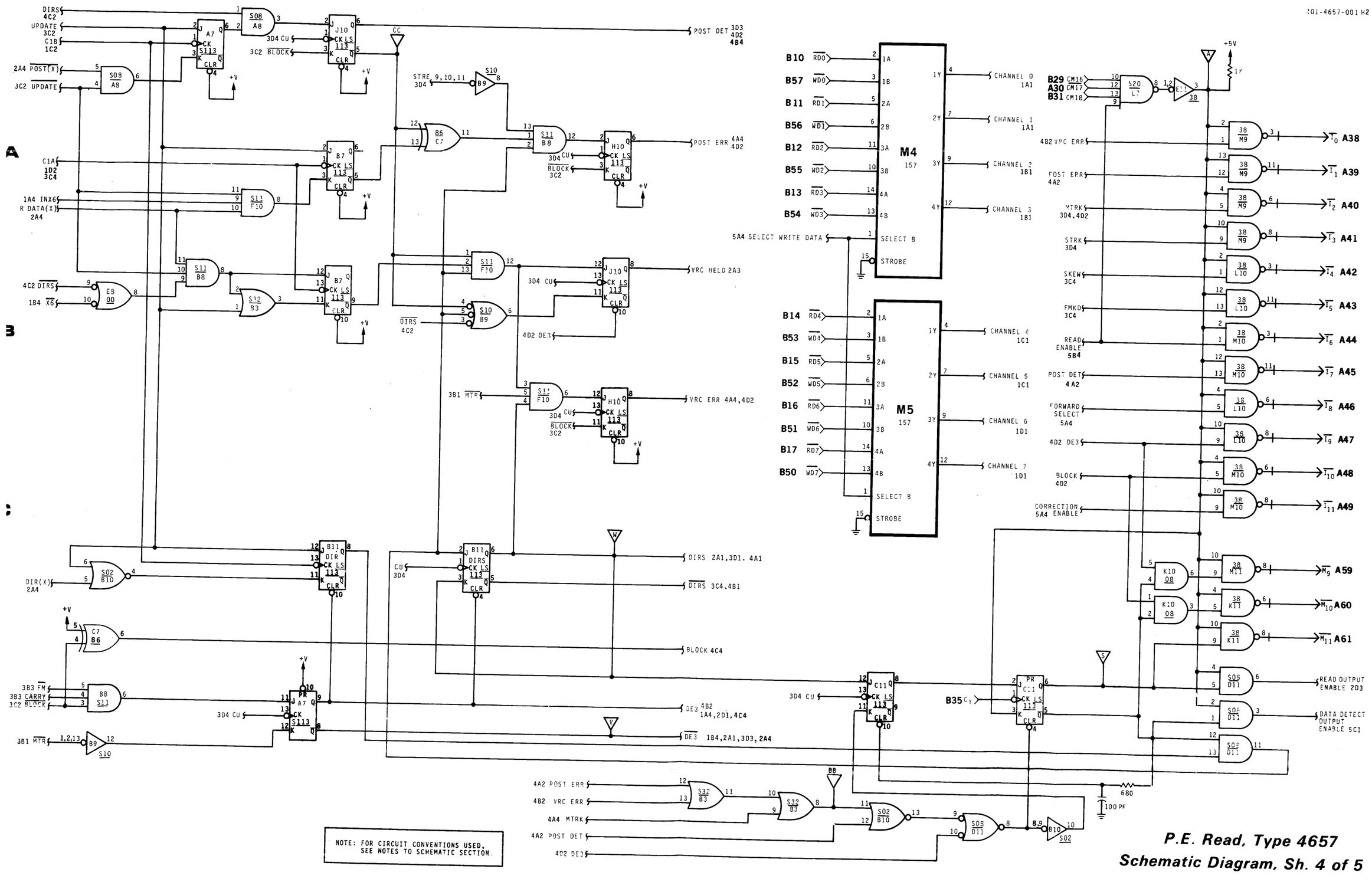


P.E. Read, Type 4657
Schematic Diagram, Sh. 2 of 5

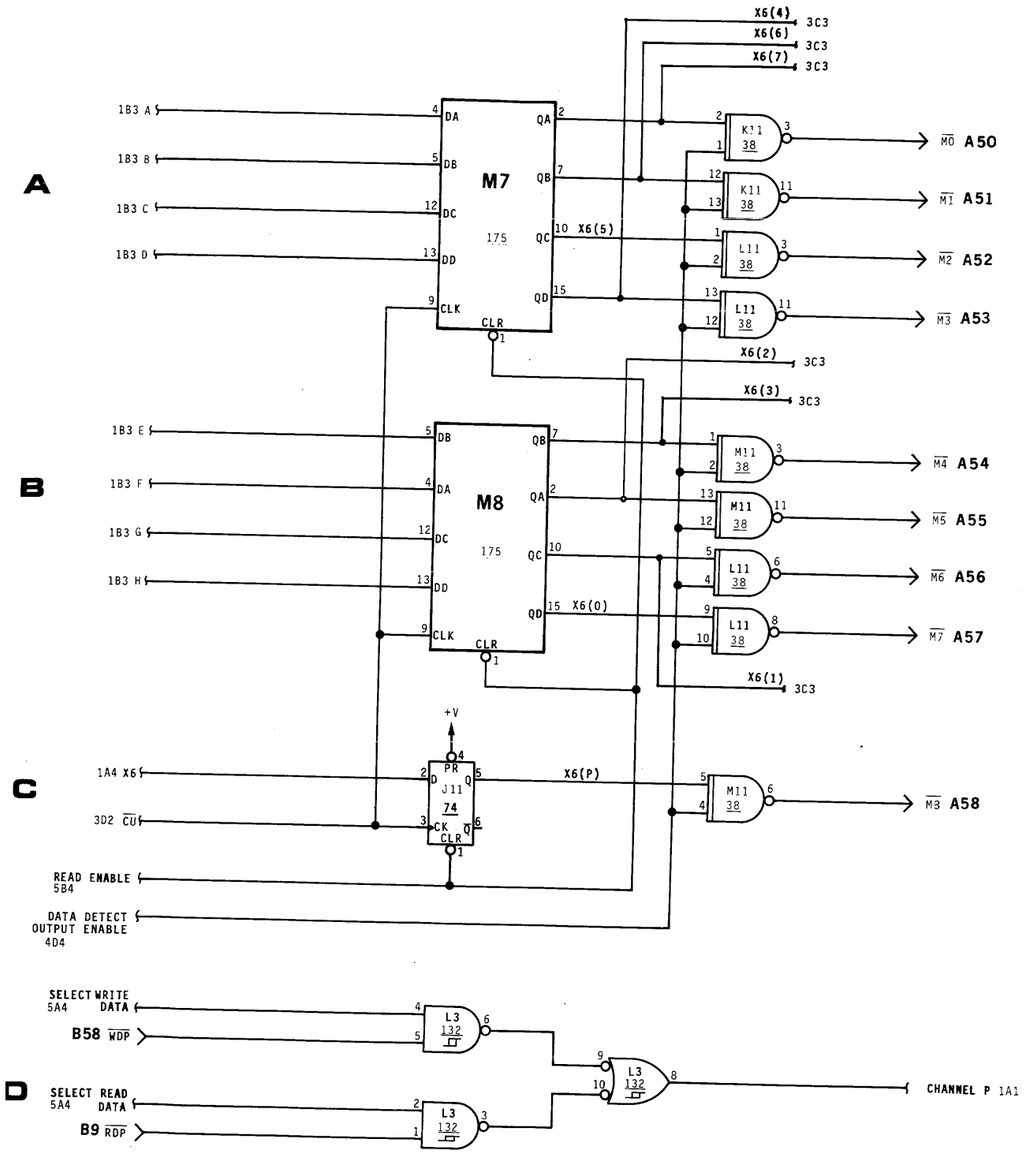


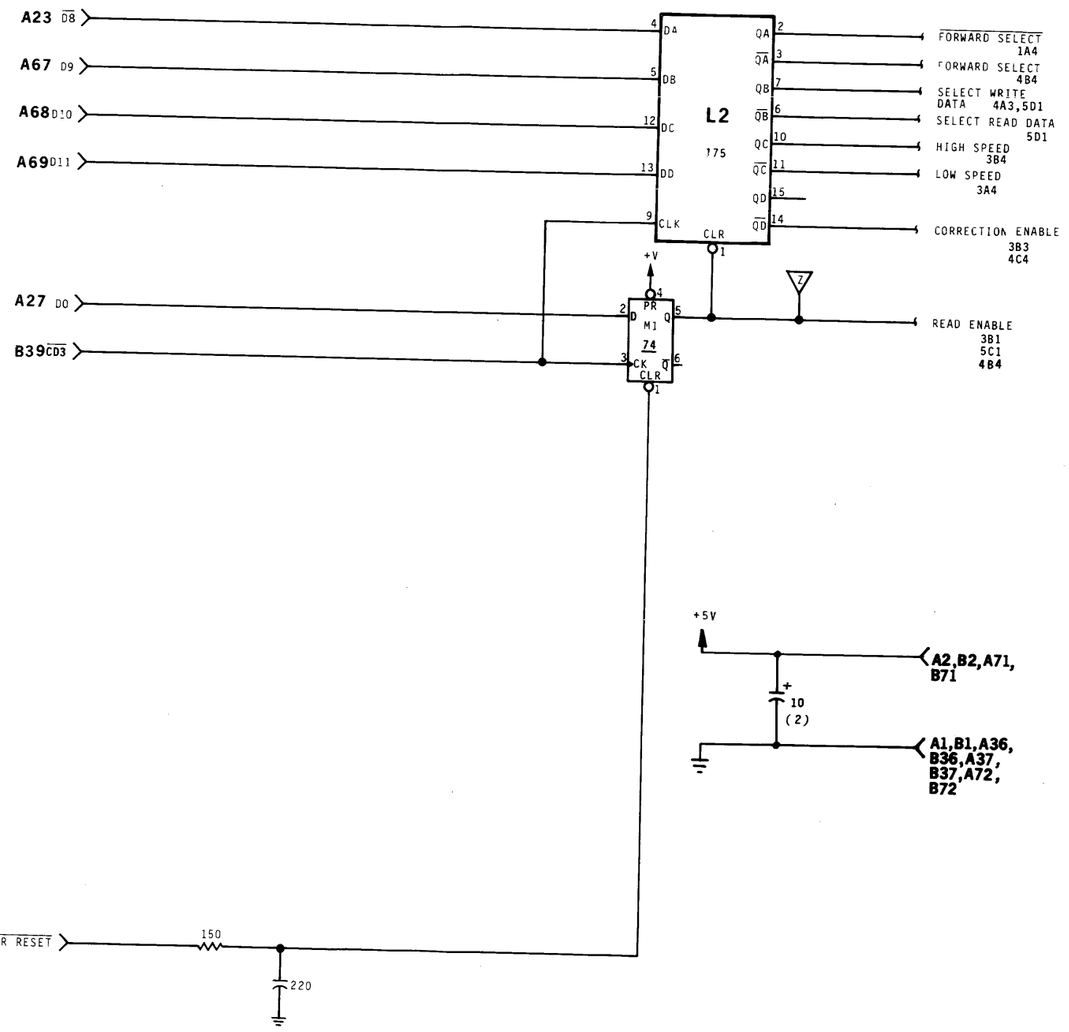
P.E. Read, Type 4657
Schematic Diagram, Sh. 3 of 5

301-4657-001 H2



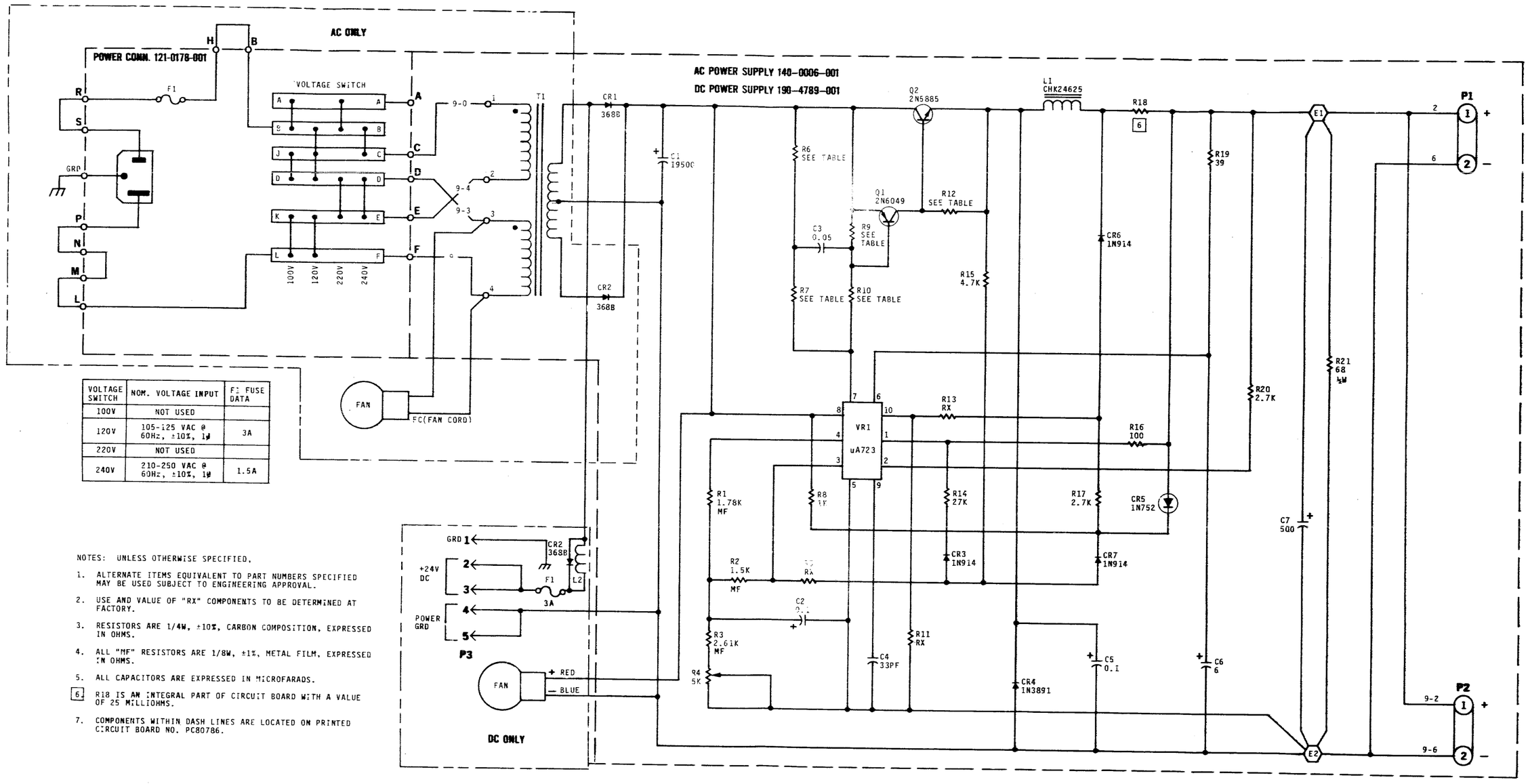
P.E. Read, Type 4657
Schematic Diagram, Sh. 4 of 5





NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

P.E. Read, Type 4657
Schematic Diagram, Sh. 5 of 5



VOLTAGE SWITCH	NOM. VOLTAGE INPUT	F1 FUSE DATA
100V	NOT USED	
120V	105-125 VAC @ 60Hz, ±10%, 1ϕ	3A
220V	NOT USED	
240V	210-250 VAC @ 60Hz, ±10%, 1ϕ	1.5A

NOTES: UNLESS OTHERWISE SPECIFIED,

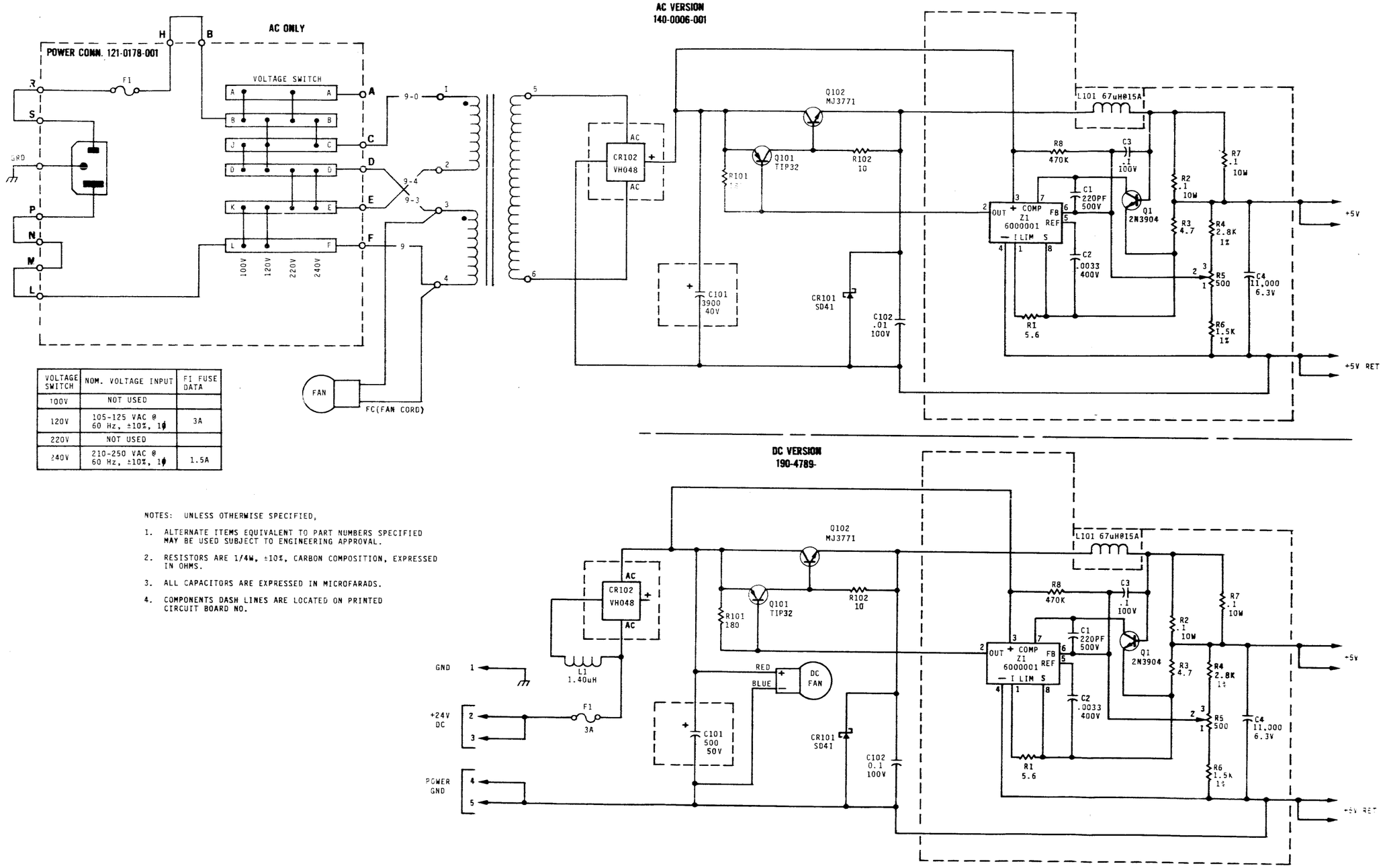
1. ALTERNATE ITEMS EQUIVALENT TO PART NUMBERS SPECIFIED MAY BE USED SUBJECT TO ENGINEERING APPROVAL.
2. USE AND VALUE OF "RX" COMPONENTS TO BE DETERMINED AT FACTORY.
3. RESISTORS ARE 1/4W, ±10%, CARBON COMPOSITION, EXPRESSED IN OHMS.
4. ALL "MF" RESISTORS ARE 1/8W, ±1%, METAL FILM, EXPRESSED IN OHMS.
5. ALL CAPACITORS ARE EXPRESSED IN MICROFARADS.
6. R18 IS AN INTEGRAL PART OF CIRCUIT BOARD WITH A VALUE OF 25 MILLIOHMS.
7. COMPONENTS WITHIN DASH LINES ARE LOCATED ON PRINTED CIRCUIT BOARD NO. PC80786.

USED ON	AC	24VDC
R6	120	150
R7	100	150
R9	330	560
R10	270	470
R12	12	4.7
C1	19500	500

NOM. VOLTAGE OUTPUT

+5 VDC ±0.5V @ 10A

Formatter Power Supply
Schematic Diagram
(Sheet 1 of 2)



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2. RESISTORS ARE 1/4W, ±10%, CARBON COMPOSITION, EXPRESSED IN OHMS.
3. ALL CAPACITORS ARE EXPRESSED IN MICROFARADS.
4. COMPONENTS DASH LINES ARE LOCATED ON PRINTED CIRCUIT BOARD NO.

Formatter Power Supply
Schematic Diagram
(Sheet 2 of 2)

Warranty

The Company warrants its devices against faulty workmanship or the use of defective materials (except in those cases where the materials are supplied by OEM) for a period of one year from the date of shipment to OEM, with the exception of ¼" cartridge products which are warranted for a period of ninety (90) days.

The liability of the Company under this warranty is limited to replacing, repairing, or issuing credit (at the Company's discretion) for any devices which are returned by OEM during such period provided that (a) the Company is promptly notified in writing upon discovery of such defects by OEM; (b) the defective unit is returned to the Company, transportation charges prepaid by OEM; and (c) the Company's examination of such unit shall disclose to its satisfaction that such defects have not been caused by misuse, neglect, improper installation, repair alteration or accident.

Kennedy Company is continually striving to provide improved performance, value and reliability in its products and reserves the right to make these changes without being obligated to retrofit delivered equipment.

KENNEDY
ALLEGHENY INTERNATIONAL

KENNEDY

ALLEGHENY INTERNATIONAL

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TWX 310-472-0116 KENNEDY