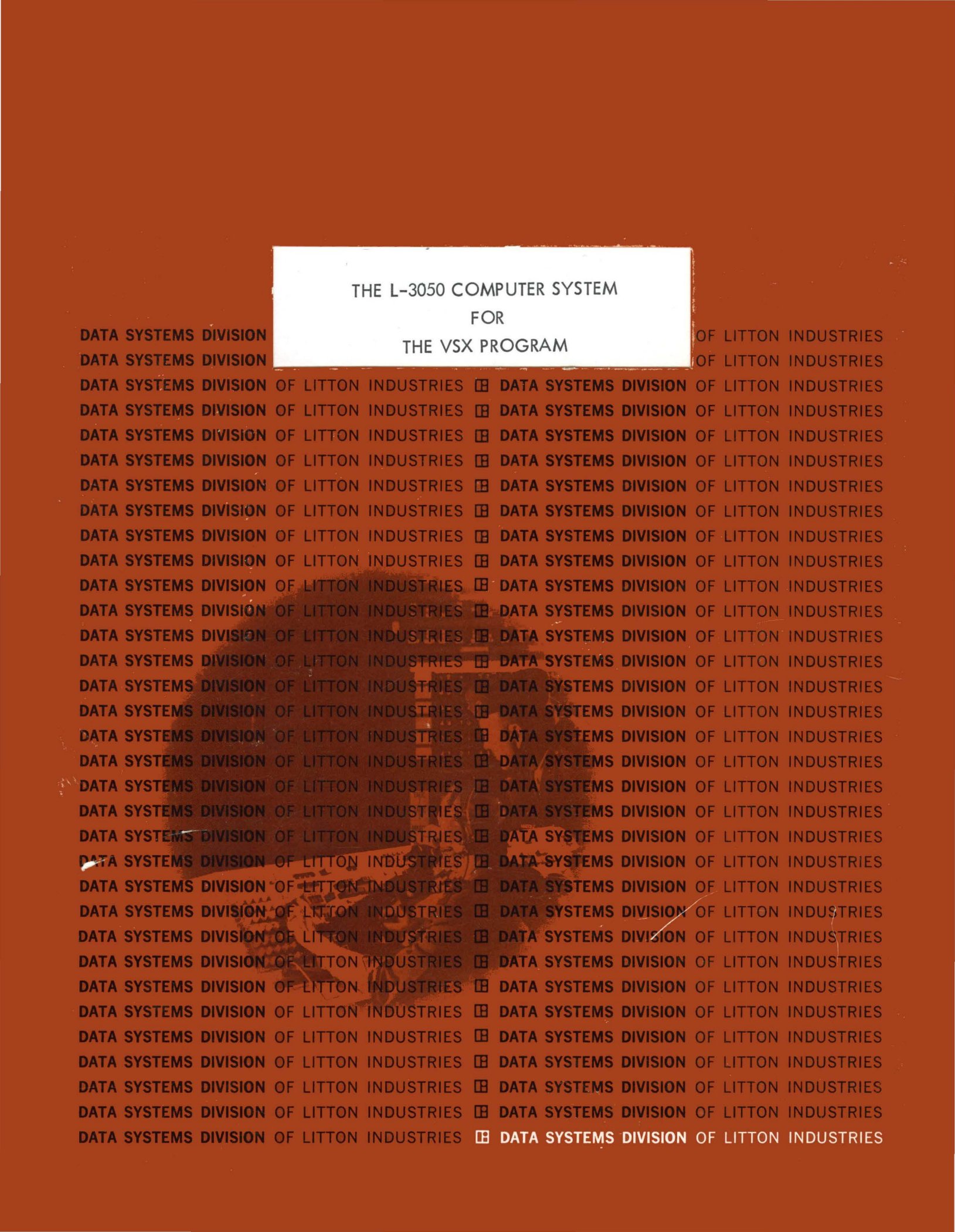
THE L-3050 COMPUTER SYSTEM FOR THE VSX PROGRAM



MS 1771

THE L-3050 COMPUTER SYSTEM
FOR
THE VSX PROGRAM

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Submitted to:

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SECTION I

INTRODUCTION

The L-3050 computer which is described in this proposal has been selected by Litton Data Systems Division as the computer which is ideally suited to solve the data processing problems encountered in the implementation of the VSX Program.

The L-3050 computer, latest member of the Litton Data Systems Division's L-300/L-3000 computer series, couples proven airborne construction techniques with advanced computer circuitry and organization to provide the highest speed, most versatile airborne computer in the industry. The multiple register, multiprogramming, multiprocessor and input/output systems featured by the L-300/L-3000 computer series have already proven effective in several real-time system applications. The implementation of these features in the L-3050 when combined with the timeliness of this computer development makes the L-3050 the ideal computer for the VSX Program.

The L-3050 is a high speed, parallel, binary computer specifically designed to meet the functional requirements of real-time command and control systems, and the environmental requirements of carrier-based airborne applications. The L-304, first member of the family, has been contracted for on three separate programs, one of which, the E2A retrofit development, involved a dual L-304 computer with up to 81,920 32-bit words of memory. The L-3050 uses virtually the identical memory with the exception that a 33rd bit per word has been added for parity. Simplified addressing to up to 131,072 32 bits is provided in all L-300 and L-3000 computers.

The processing capability of the L-3050 has been extended beyond that of the L-304 by increasing the number of instructions to 128, including 32-bit arithmetic as well as 16-bit arithmetic and adding to the number of registers to provide 8 16-bit process registers and 8 32-bit accumulators for each of the 64 program levels. Instruction execution times have been decreased appreciably from those of the L-304 by using "live" process registers and accumulators, taking maximum advantage of memory overlap and allowing instructions to be executed from the process registers or accumulators. The advantage gained by the latter step is shown in the execution times for the integration loop of the sample problem which shows an average execution time of less than 2.5 microseconds per instruction. The advantages of the basic computer organization are made apparent in the same problem where the inner loop of 5 instructions achieves two integrations for each pass through the loop.

The multiprogramming capabilities of the L-3050 are not demonstrated by the sample problems previously submitted to NADC, however, experience in the E2A application has shown that the savings in time and programming complexity in real-time processing is substantial with the L-300/L-3000 multiprogramming implementation. In that dual processor system which performs radar data processing, navigation, data link communication, and display and control processing, only 200 instructions are required for executive control.

The multiprocessing system, which has been proven in the E2A application, is, from the programmer's point of view, merely an extension of the multiprogram system of the single computer. The difference is that instead of one program operating, the highest priority program assigned to each processor is processed simultaneously. The net result is a virtual doubling of computer speed as maximum advantage is taken of each processor's capability.

The input/output system of the L-3050 provides the maximum in speed and flexibility. When the second processor is added to the system, the potential input/output speed and the number of possible system combinations is greatly increased. Each L-3050 is capable of controlling up to 64 input/output devices. Transfers may be either 8 bits in parallel or up to 32 bits in parallel at transfer rates of up to one word or character per memory cycle for each processor. Additional potential combinations are possible which allow input/output to proceed either with or without stealing memory cycles from the processor. It is also possible to arrange the I/O system as was done in the E2A retrofit program, so that peripheral units may be switched to either processor should the other fail.

The packaging used in the airborne L-3050 is the same as that which has successfully passed the rigors of a very extensive step-stress program. The multilayer boards used in the memory and logic portions of the computer makes for an extremely reliable package as well as one which is very compact and lightweight. The latter feature is of utmost importance for the VSX Program as the computer will be very limited in allowable cube and weight.

Finally, the Litton schedule for development of the L-3050 fits exactly the requirements of the NADC-VSX Program (see Section V). A plug-in card version is scheduled for completion in the latter part of 1967 with an airborne high-density version, using proven L-304 packaging, scheduled to follow within six months thereafter. This early development of the L-3050 assures that a proven product with the following unique features will be available for VSX needs:

- Highest speed
- Proven design concepts
- Proven packaging
- Simplified programming
- Proven dual processor design
- High speed, flexible I/O
- Smallest size, lightest weight
- High reliability
- Fail-safe modes
- Early availability of laboratory and airborne models

SECTION II

L-3050 COMPUTER DESCRIPTION

2.1 FUNCTIONAL DESCRIPTION

2.1.1 System Organization

The L-3050 consists of a modular organization of basic system units. These units include: processors, memory modules, power supplies, control consoles, and input/output exchange units. Combinations of these basic units may be organized into systems that will meet the requirements of a wide variety of computer system applications. A typical L-3050 Dual Processor System is shown in Figure 2-1.

2.1.1.1 Processor

A processor consists of the following functional units: arithmetic unit, instruction control unit, memory control unit, program level control unit, and input/output control unit. The arithmetic unit contains a 32-bit, parallel, full adder that is used to execute most instructions. The instruction control unit decodes the instruction and provides control signals to other functional units. It also provides the basic clock frequency to these units. The memory control unit controls traffic on a memory word bus and an address bus. The memory control unit processes requests for memory cycles from the other functional units of the processor and also provides memory parity check and generation functions.

The program level control unit determines which of up to 64 programs has the currently highest priority and provides program level switching control.

The processor contains an input/output control unit that is independent from the other functional units of the processor. This allows data communication to occur simultaneously with instruction computation. Each processor may control and communicate with up to 64 peripheral devices. This may be under instruction control or it may be independent of instruction control and under control of special "key words." Key words are accessed at a rate that is determined by the transmitting or receiving peripheral device. A key word contains block length, memory "running" address, and mode of operation. It is preset by the program prior to data communication.

The input/output control unit connects with peripheral devices via a common set of 33 bidirectional data lines (includes a parity line), control lines and three address lines. Data communication with all devices is controlled on these lines on a

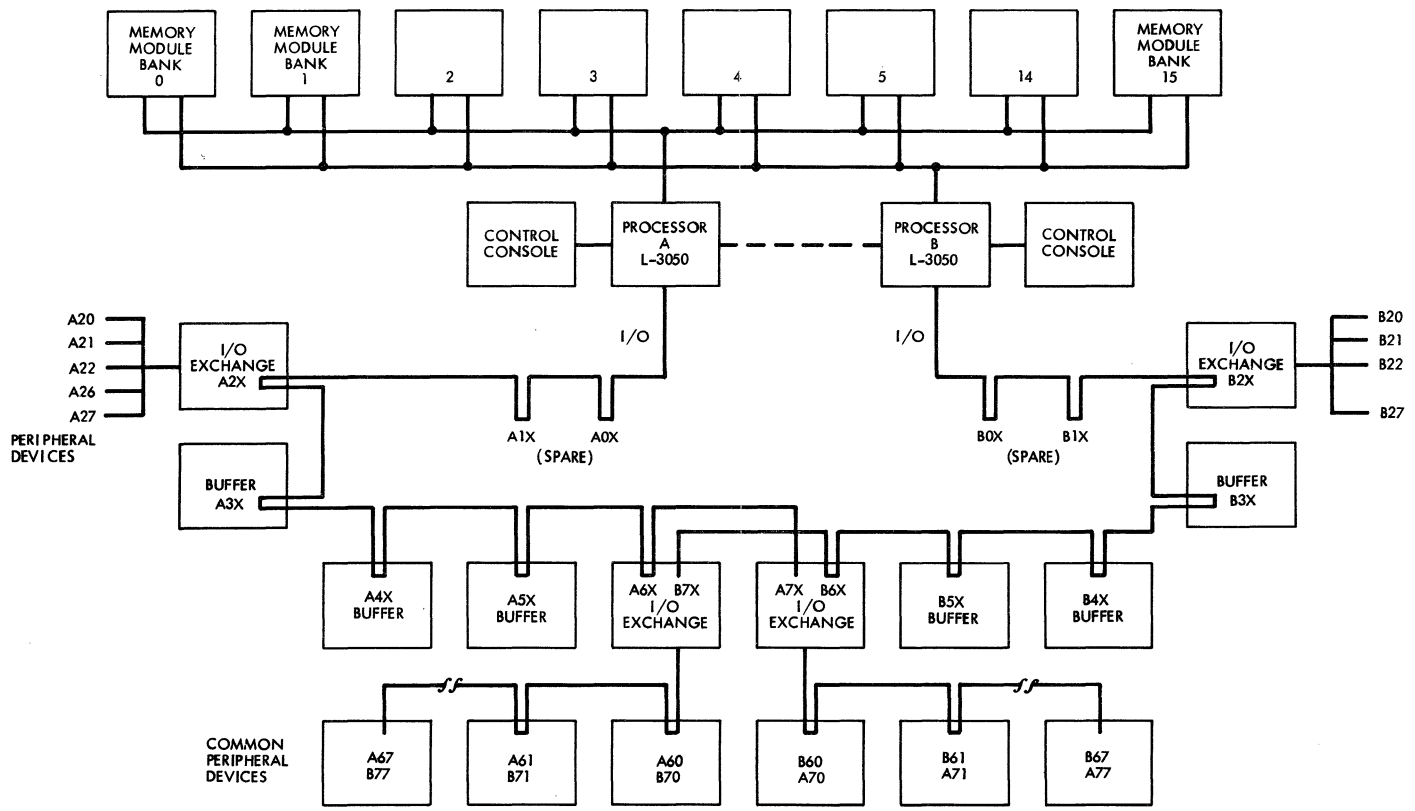

Figure 2-1. L-3050 Data Processor System

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"party line" basis. Eight separate "request" lines and eight separate "acknowledge" lines are provided to signal and respond to requests for data transmission over the common lines. When more than eight devices are required in the system, the three address lines are used to multiplex up to eight devices to a single request line. This is accomplished with an input/output exchange unit or a special buffer that controls more than one device.

2.1.1.2 Memory Modules

Each memory module contains 8192 words and each word is 33 bits in length. Memory modules contain their own logic for the following: processing requests from two processors, memory protection under program control, bank address modification, and self-test. Memory timing is independent of processor timing and, therefore, may be a variable without modification to the processors. The standard L-3050 Memory Module can complete a full cycle in less than two microseconds. A processor can address up to 16 memory modules in one system.

Each memory module may be connected to two processors via independent address buses and word buses. A memory module is selected by the four most significant bits of one of its 17-bit address buses. This is a "bank address." The remaining 13 bits are used for word selection. Logic within a memory module will resolve a simultaneous request from two processors, otherwise, processors are serviced on a first come—first serve basis and the second processor is temporarily suspended if both processors are accessing the same memory module.

Memory protection from programmed modification is provided in 4096-word sizes. Special instructions are used to set one-half or all of the memory into a "non-destructive" mode. This control is provided for both processors and is independent for each processor.

A memory module is given a bank address under program control. A four-bit register in each module is used by both processors to contain a variable bank address. A memory module may also be set active or inactive under program control.

2.1.1.3 Power Supplies

Each basic system unit contains its own microminiature power supply. Each power supply contains its own transient and fault detection hardware. Should a fault or line transient be detected, an automatic interrupt signal is transmitted to one or both of the processors. Action taken is a function of the system organization and which power supply has failed.

2.1.1.4 Control Consoles

A control console is usually provided for each processor. This console contains features for program checkout, maintenance and automatic fault detection indicators. A control console does not normally connect via an input/output channel.

2.1.1.5 Input/Output Exchange Units

An input/output exchange unit provides a multiplexing function for one of the eight main I/O stations. It provides an interface that is identical to the input/output control unit's interface. That is, it resolves priority control over eight request lines and controls sharing of common data and control lines just like the input/output control unit. An input/output exchange unit can be connected to two processors. A command from either processor will switch the I/O exchange unit from one processor to the other.

The I/O exchange unit also provides special long line drive capability for those devices that are located over 100 feet from the processor.

2.1.2 Special Features

2.1.2.1 Multiprogramming

Multiprogramming is a feature that allows the processor to execute up to 64 different programs, one at a time, on a priority demand basis. The control for switching from one program to another is built into the hardware.

2.1.2.1.1 Program Levels. Each of the 64 programs is assigned a program level number. This number corresponds to a bit position within a 64-bit register called the program status register. Bits are set or reset in this register by program or by the input/output control unit of the processor. There is also a second 64-bit register called the program enable register which provides a logical masking on the program status register. Bits in this register are set or reset by programmed instructions. Together, these two 64-bit registers are called the program activity register (PAR). The most significant (highest numbered) one-bit of the program status register which has a corresponding one-bit in the program enable register determines the currently active program.

The PAR is held in four, full word locations of the processor's 16 scratch pad registers. It is made available to the programmer with instructions that use half word, operand addresses: 004000 to 004070_8 (see Table II-1).

OCTAL ADDRESS	PROGRAM ENABLE BITS	OCTAL ADDRESS	PROGRAM STATUS BITS
4000	37_8 TO 16_8	4002	37_8 TO 16_8
4001	15_8 TO 00_8	4003	15_8 TO 00_8
4004	77_8 TO 60_8	4006	77_8 TO 60_8
4005	57_8 TO 40_8	4007	57_8 TO 40_8

Table II-1. Program Activity Register 1616-58

A six-bit number that represents the active program level is logically generated and held in a register called the program level register. The contents of this register are available to the program by execution of normal instructions with special operand address 004030_8.

Program levels 77_8 to 74_8 are reserved for special functions. Program level 77 is used for power-on and power-off functions. This level is automatically entered whenever a power transient is detected or power is initially turned on or off. All active registers of the L-3050 are automatically saved in memory each time a program level change is made: therefore, it is not necessary for the programmer to store these registers when a power transient is detected. During a power-off condition there is sufficient time to execute several instructions in level 77. The contents of the active registers on level 77 are lost when power is turned off. Program level 77 is the only program level that cannot be interrupted by the input/output control unit to process data requests. That is, no I/O communication can take place if the processor is executing a program at level 77. Program level 77 is always "enabled." That is, bit position 77 of the program enable register is wired to a "one."

Program level 76 is reserved for processing detected memory errors. The detection of a memory parity error by the memory control unit or the detection of an attempt to modify a protected area of memory will cause bit 76 of the program status register to be set and, if bit 76 of the program enable register is set, a program level change will occur. The bank address of the memory module that caused the error and the error type indication are automatically stored into the indicator word of program level 76_8.

Program level 75_8 is reserved for a program trace feature. If a console switch is depressed and a program level change occurs, program level 75 is entered (temporarily) in order to execute a program trace program.

Program level 74_8 is reserved for automatic entry due to detection of hardware faults. Special hardware is provided in all functional units to continually monitor for normal operation. Should abnormal operation be detected, program level 74 is entered.

Program level 00 is reserved for execution of a "bootstrap" routine after a program load operation.

2.1.2.1.2 Program Level Registers. A set of fourteen, 32-bit words is assigned to each of the 64 program levels. These 896 words are assigned fixed addresses in the memory module that is selected by the base memory field of the memory extension register. These assigned addresses are shown in Figure 2-2. The set of fourteen words for the currently active program level are held in the processor's active registers. The remaining words are held in their fixed memory locations. Each time a program level change occurs, the old registers are written back into the base memory and the new registers are obtained from memory and are set into the processor's active registers. This operation requires less than 30 microseconds.

The fourteen words associated with each program level are as follows:

Eight Accumulators for full word instructions.

Four words that hold eight 16-bit process registers. These registers are used for index registers or half word accumulators.

Two words designated as the program address file, PAF. The PAF separates into four half words: the instruction location counter, LL; the memory address extension register, LD; the indicator word, IW; and the base address register, LB.

The eight active accumulators and 16 process registers are held in 12 of the processor's 16 scratch pad registers. The PAF is held in flip-flop registers for the currently active program.

These active registers, the program level register and program activity register, PAR, are available to the program by special operand addresses. Operand addresses $004000\text{-}004037_8$ are detected as special register addresses for most L-3050 instructions. Therefore, these memory locations in the processor's base memory are not available for data storage, however, they are available for instruction storage. Table II-2 lists the assigned special operand addresses.

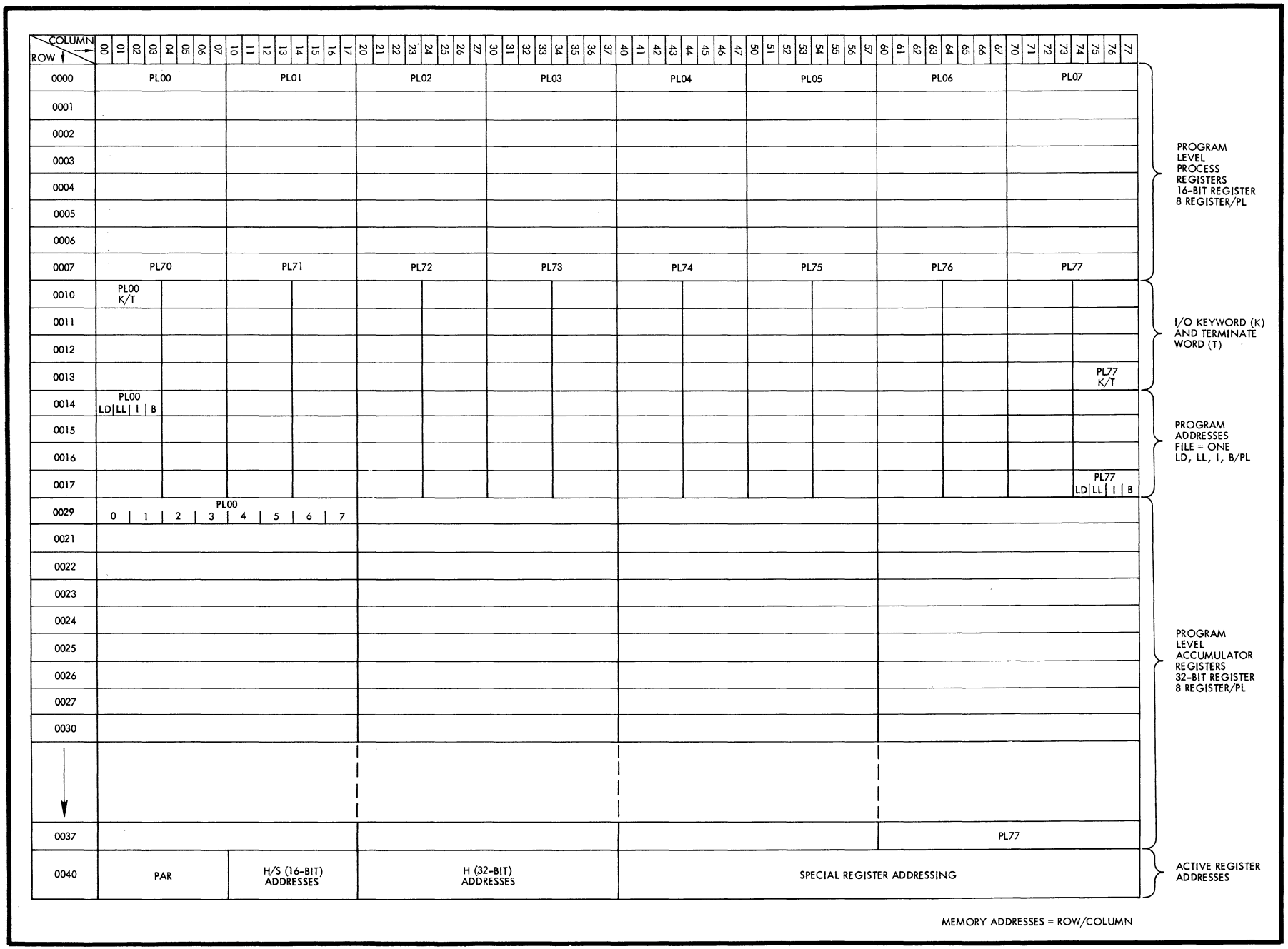


Figure 2-2. Memory Map of Dedicated Locations

1771-2

HALF WORD ADDRESS IN OCTAL	REGISTER NAME	REGISTER SYMBOL
004000	BITS 00-15 OF PROGRAM ENABLE REGISTER, PAR	PE15-00
004001	BITS 16-31 OF PROGRAM ENABLE REGISTER, PAR	PE31-00
004002	BITS 00-15 OF PROGRAM STATUS REGISTER, PAR	PS15-00
004003	BITS 16-31 OF PROGRAM STATUS REGISTER, PAR	PS31-00
004004	BITS 32-47 OF PROGRAM ENABLE REGISTER, PAR	PE47-32
004005	BITS 48-63 OF PROGRAM ENABLE REGISTER, PAR	PE63-48
004006	BITS 32-47 OF PROGRAM STATUS REGISTER, PAR	PS47-32
004007	BITS 48-63 OF PROGRAM STATUS REGISTER, PAR	PS63-48
004010	HALF WORD PROCESS REGISTER, 0 (ACTIVE LEVEL)	H OR S-0
004011	HALF WORD PROCESS REGISTER, 1 (ACTIVE LEVEL)	H OR S-1
004012	HALF WORD PROCESS REGISTER, 2 (ACTIVE LEVEL)	H OR S-2
004013	HALF WORD PROCESS REGISTER, 3 (ACTIVE LEVEL)	H OR S-3
004014	HALF WORD PROCESS REGISTER, 4 (ACTIVE LEVEL)	H OR S-4
004015	HALF WORD PROCESS REGISTER, 5 (ACTIVE LEVEL)	H OR S-5
004016	HALF WORD PROCESS REGISTER, 6 (ACTIVE LEVEL)	H OR S-6
004017	HALF WORD PROCESS REGISTER, 7 (ACTIVE LEVEL)	H OR S-7
004020	FULL WORD ACCUMULATOR, 0 (ACTIVE LEVEL)	H-0
004021	FULL WORD ACCUMULATOR, 1 (ACTIVE LEVEL)	H-1
004022	FULL WORD ACCUMULATOR, 2 (ACTIVE LEVEL)	H-2
004023	FULL WORD ACCUMULATOR, 3 (ACTIVE LEVEL)	H-3
004024	FULL WORD ACCUMULATOR, 4 (ACTIVE LEVEL)	H-4
004025	FULL WORD ACCUMULATOR, 5 (ACTIVE LEVEL)	H-5
004026	FULL WORD ACCUMULATOR, 6 (ACTIVE LEVEL)	H-6
004027	FULL WORD ACCUMULATOR, 7 (ACTIVE LEVEL)	H-7
004030	PROGRAM LEVEL REGISTER, PAF	LP
004031	MEMORY EXTENSION REGISTER, PAF	LD
004032	INDICATOR WORD, PAF	IW
004033	BASE ADDRESS REGISTER, PAF	LB
004034	RESERVED FOR FAULT ISOLATION	
004035	RESERVED FOR FAULT ISOLATION	
004036	RESERVED FOR FAULT ISOLATION	
004037	RESERVED FOR FAULT ISOLATION	

1771-3

Table II-2. Special Operand Addresses 1771-3

Registers of inactive programs are available by addressing their assigned locations in the base memory. The contents of the assigned memory locations of the active program's registers are set to all zeros at the time that the program is active.

The use of special register addresses for operands provide a convenient method of manipulating and controlling these registers. It also provides a method of programming register-to-register operations. Whenever the operand address field of an instruction selects a register as an operand, the instruction execution time is one microsecond less.

If a half word process register is used as an operand with a full word instruction, the 16-bit operand is assumed to be right justified. Sign extension is automatically provided on algebraic, full word instructions. If a full word accumulator is used as an operand with a half word instruction, the left or right half of the accumulator is selected according to the least significant bit of the operand address.

Transfer instructions (and others to be specified) do not use the special register address feature.

2.1.2.1.3 Program Address File. The program address file (PAF) contains four 16-bit fields that provide program address options and conditional status data for sequencing the current program. As stated in Subsection 2.1.2.1.2, there is a PAF for each of the 64 program levels. The four fields are: the instruction location register, LL; the memory extension register, LD; the base address register, LB; and the program indicator word, IW.

The instruction location register holds the address of the next instruction in normal sequence. It is a copy of the processor's instruction counter, LL, as it was when the associated program was last active.

The memory extension register, LD, provides four fields of four bits each for expanded memory addressing. Each four-bit field represents a bank address. The LD register provides a convenient method of directly addressing up to 262,144 16-bit words. Four of any 16 memory banks (16,384 16-bit words per bank) are directly addressable on any program level for any one setting of the LD register (see Subsection 2.1.3.2).

An alternate method of extended memory addressing is also provided in the L-3050. This is provided with the base address register, LB, of the PAF. This 16-bit register may be added to the instruction's operand address or it may be added

to the instruction location register LL, at the option of the programmer. When this register is added to a 16-bit address, it is shifted left by 2-bit positions to yield an 18-bit address. The base address register provides a "dynamic relocatability" feature. It is described in more detail in Subsection 2.1.3.5. The option is controlled by three bits in the indicator word and by the least significant bit (W) of the "operand" address on transfer instructions.

The indicator word of the PAF also contains information bits that indicate the status of certain conditions of the assigned program. Three bit positions signify "less then," "greater than" or "equal to" as a result of compare instructions. These bits may be tested individually or in combination by a special transfer instruction. Two other bits indicate arithmetic overflow and floating point underflow. The remaining bits of the indicator word are used only in program levels 74_8 and 76_8. If a memory error is detected, the bank address of the faulty memory is placed in the indicator word of program level 76. One of two bits are set to indicate a parity error or a protected area violation. If a functional unit is detected as failing, its code number is set into the indicator word of program level 74.

2.1.3 L-3050 Instructions

2.1.3.1 Data Word Formats

The L-3050 utilizes several data word formats depending upon the instruction's requirements. Data words may be logical or algebraic. Logical data words may be 16 bits or 32 bits in length. Algebraic words may be 16 bits or 32 bits in length. Certain algebraic operations may produce a double word result, such as the product on a fixed point multiply instruction. All algebraic words are treated as binary fractions with negative numbers represented in a two's complement form. The sign bit of algebraic numbers is located in the most significant bit position. A "one" represents a negative sign.

Figure 2-3 displays the L-3050 data word formats.

2.1.3.2 Instruction Word Format

The L-3050 uses a 32-bit instruction format as shown in Figure 2-4. The fields of the instruction specify the following functions:

E, bit position 31 — This one-bit field generally specifies a half word (16-bits) operation or a full word operation (32-bits). If this bit is a one, a full word operation (as specified by the instruction's F field) occurs. On a few "interrupt control" type instructions, this bit (when set to a one) allows a program level change.

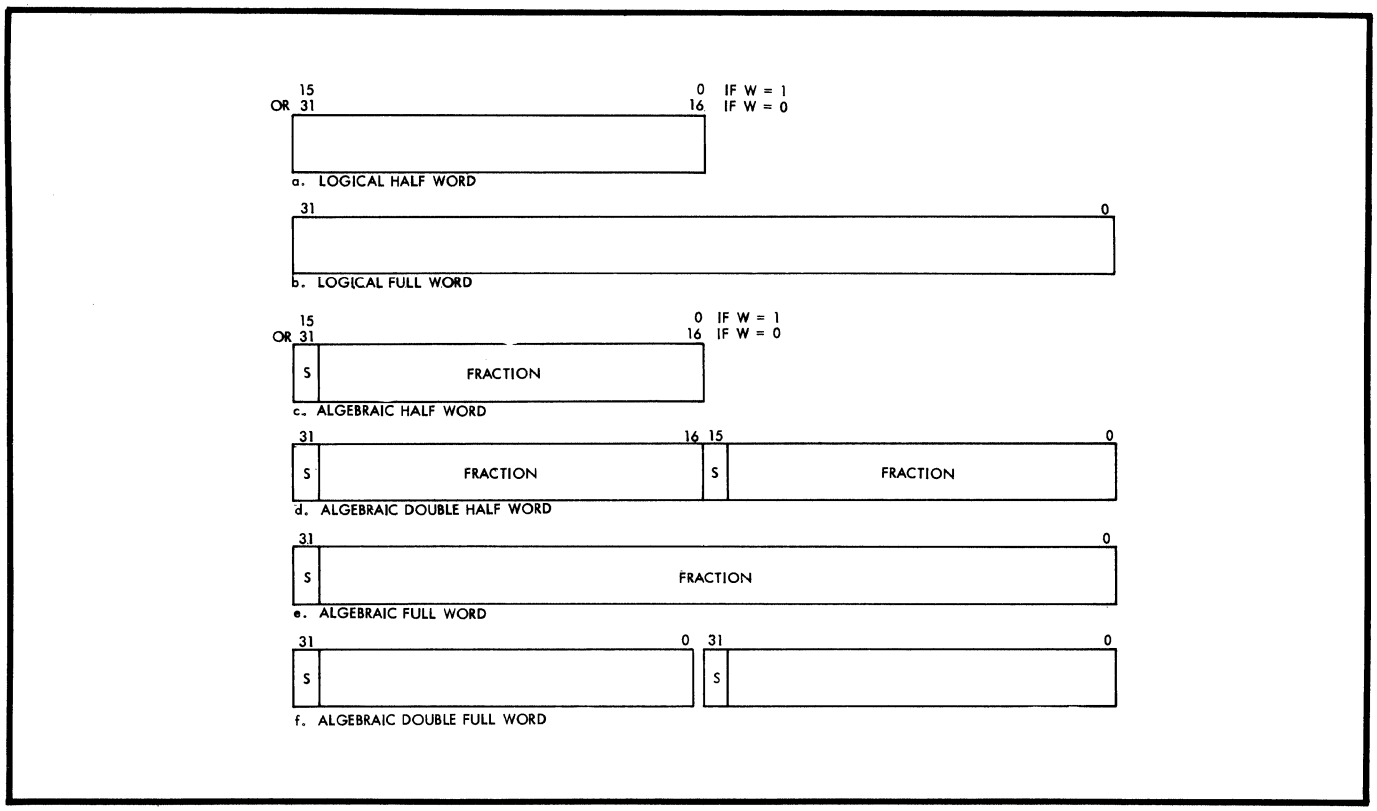


Figure 2-3. L-3050 Data Word Formats 1771-4

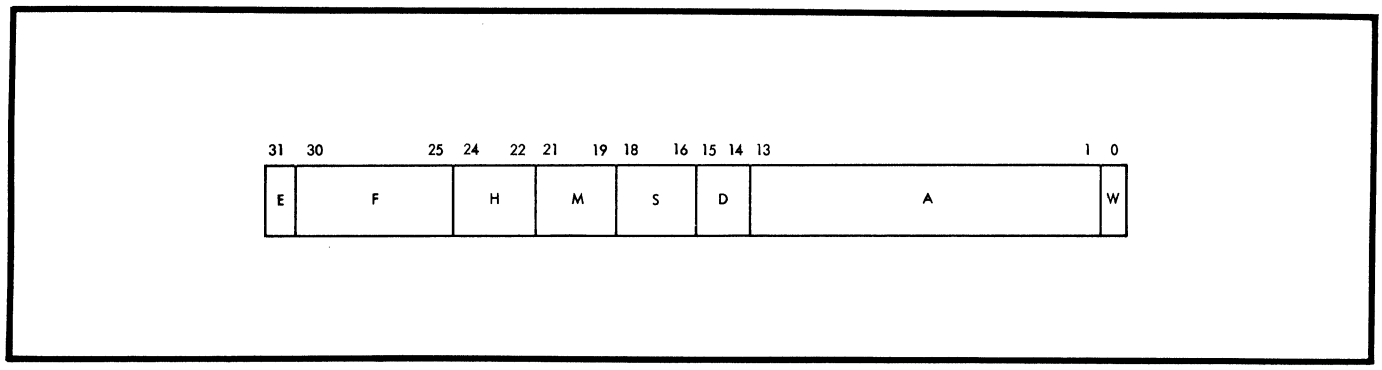


Figure 2-4. L-3050 Instruction Word Format 1616-62

F, bit positions 30 to 25 — This six-bit field specifies the operation to be performed by the instruction. In the following instruction descriptions, a two-character octal number is used to specify this six-bit instruction code.

H, bit positions 24 to 22 — This three-bit field addresses the accumulator to be used with the instruction. If the E bit of the instruction is a one, the H field selects one of eight 32-bit accumulators for the operation. If the E bit is a zero, the H field selects one of eight 16-bit accumulators for the operation. There is a separate set of eight 32-bit accumulators and a separate set of eight 16-bit accumulators (a total of 12 full words) for each of the 64 program

levels. These registers are held in memory for nonactive programs and are held in hardware registers for the active program.

M, bit positions 21 to 19 — This three-bit field provides nine operand addressing modes for the instruction as follows:

M = 0, Direct Address — The D, A, and W fields of the instruction word are not modified. The A and W fields specify an operand address in the memory bank that is indirectly selected by the D field. On full 32-bit operand addresses, W is assumed to be 0.

M = 1, Direct Address with Indexing — The D, A, and W fields of the instruction word are added to the content of the index register selected by the S field. Overflow on this addition is not detected. The sum replaces the D, A, and W fields within the instruction word register and is used as the new instruction address field as in M = 0.

M = 2, Literal — The D, A, and W fields represent a 16-bit word. A memory cycle to obtain this 16-bit word from memory is not required, thereby reducing instruction execution time. This word may be used as: an operand, a mask, an instruction address, a move instruction command, a shift instruction command, etc., depending upon the instruction's operation code. When this mode is used with full word accumulators, the 16-bit word is assumed to be right justified. That is, it is assumed to line up with the right half of the full word.

M = 3, Literal with Indexing — The D, A, and W fields represent a 16-bit half word as in mode 2. However, the process register that is selected by the instruction's S field is arithmetically added to this half word before the instruction operation (that is specified by the F field) takes place. This provides a useful double operation on many instructions. Overflow is detected on this addition, if it occurs the overflow indicator is set.

M = 4, Indirect — The contents of the memory word that is directly addressed by the D, A, and W fields is used as a 16-bit address. This "indirect" address replaces the D, A, and W fields within the instruction word register and is used as in M = 0.

M = 5, Indexed, Indirect — The D, A, and W fields of the instruction word are added to the index register that is selected by the S field. Overflow on this addition is not detected. The sum is used to address a 16-bit

word in memory that replaces the D, A, and W fields of the instruction in the instruction word register. This new address is then used as in M = 0.

M = 6, Indirect, with Indexing – The D, A, and W fields of the instruction select a 16-bit word in memory which is added to the index register selected by the S field of the instruction. No overflow detection occurs. The sum replaces the D, A, and W fields of the instruction in the instruction word register. This new address is then used as in M = 0.

M = 7, Relative with No Indexing – The S field must be all zeros. The content of the current program's instruction location counter is added to the D and A fields of the instruction. The W bit is not modified. Overflow is not detected on this addition. The sum replaces the D and A fields of the instruction within the instruction word register. This operation yields an address that is relative to the address of the next instruction in sequence.

M = 7, Relative with Indexing – The S field must not be all zeros; it selects one of seven process registers. The D, A, and W fields of the instruction word are added to the content of this process register. The content of the current program's instruction location counter is then added to this indexed address. Overflow is not detected on either of the additions. The sum replaces the D and A fields of the instruction within the instruction word register. This operation yields an indexed address that is relative to the address of the next instruction in sequence.

S, bit positions 18 to 16 – This three-bit field selects one of eight 16-bit registers to be used for operand address indexing. These eight registers are the same registers as the 16-bit accumulators that are also selectable by the instruction's H field when the E bit is set to a zero. Because of their dual purpose, these registers are called "process registers." The S field is used on address modes M = 1, 3, 5, 6 and 7 with S $\neq$ 0.

D, bit positions 15 and 14 – These two bits normally select one of four fields in the memory extension register, LD, as shown in Figure 2-5.

The selected four bits are used to select an 8192 word memory bank. Note that four banks, 32, 768 words, are addressable with one setting of the memory extension register. This register is easily loaded with a special instruction or by special address to provide access of up to 131, 072 full words of memory. The contents of this register may be different for each program level.

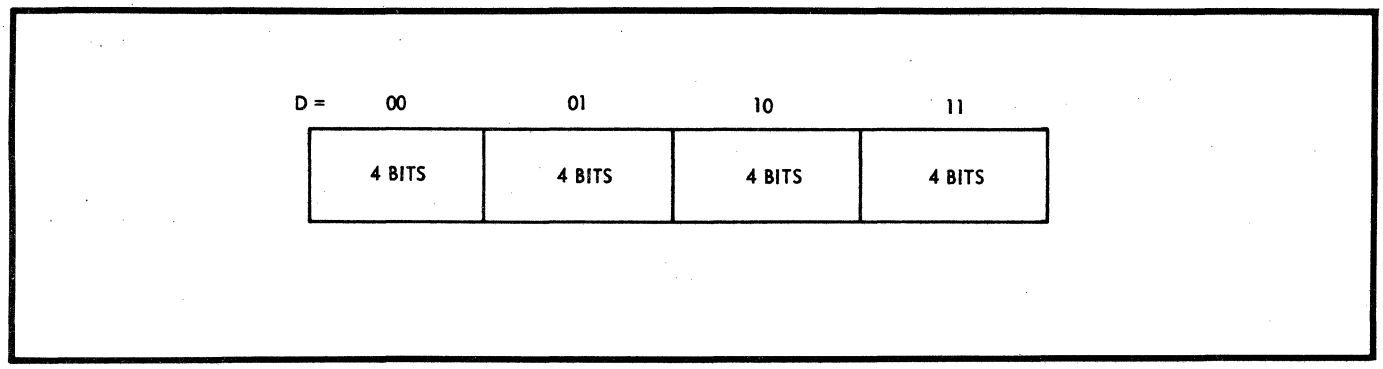


Figure 2-5. Address Extension Register 1616-63

The D bits may also be used as normal memory address bits along with the instruction's A field. The D, A, and W fields represent a 16-bit address that is algebraically added to the contents of the base address register, LB. This option is selected by the program by the setting of two control bits that are located in the indicator word register, IW. The LB register is assumed to be shifted left by two-bit positions with respect to the D, A, and W fields. The algebraic sum yields an 18-bit address that can select up to 131,072 full words. These addresses are relative to the contents of the base address register.

A, bit positions 13 to 1 — These bits represent a full word address in the 8192 word memory bank that was selected either by the instruction's D field and memory extension register or the four most significant bits of the sum of the D and A fields and the base address register.

W, bit position 0 — This bit is used on half word operations (E bit set to 0) to select the left half or right half of the word to be used as the operand. If W is a one the right half of the word is used.

2.1.3.3 Instruction Timing

Instruction execution time in the L-3050 is dependent upon the operant address mode selected by the instruction's M field and the location of instructions and operands in memory. If instructions and operands are located in separate memory banks, advantage of memory cycle overlap is taken.

Table II-3 displays the instruction execution times (in microseconds) for all operand address modes on an add type instruction. The memory overlap column assumes that instructions, indirect addresses and operands are located in different memory banks. The no overlap column displays the instruction timing as if only one memory bank were used for all storage. In addition, it should be noted that a still further reduction in instruction time is possible when the operand is located in the active scratch pad registers.

OPERAND ADDRESS MODE	MEMORY OVERLAP	NO MEMORY OVERLAP
M = 0, DIRECT	2.5 MICROSECONDS	4.0 MICROSECONDS
M = 1, DIRECT, INDEXED	3.0 MICROSECONDS	4.0 MICROSECONDS
M = 2, LITERAL	2.0 MICROSECONDS	2.0 MICROSECONDS
M = 3, LITERAL, INDEXED	2.0 MICROSECONDS	2.0 MICROSECONDS
M = 4, INDIRECT	3.5 MICROSECONDS	6.5 MICROSECONDS
M = 5, INDEXED, INDIRECT	4.0 MICROSECONDS	4.0 MICROSECONDS
M = 6, INDIRECT, INDEXED	4.0 MICROSECONDS	4.0 MICROSECONDS
M = 7, RELATIVE, NO INDEX	3.0 MICROSECONDS	4.0 MICROSECONDS
M = 7, RELATIVE, INDEXED	3.5 MICROSECONDS	4.0 MICROSECONDS

Table II-3. Add Class Instruction Timing 1771-12

The most general case, for those instructions which require an operand, is the direct address mode (M = 0). The most common case for those instructions which use the instruction's address field for other than operand addresses (such as transfer instructions) is the literal mode (M = 2). These are the times that are quoted with the instruction descriptions in Subsection 2.1.3.4. It is also assumed that data and instructions are located in different memory banks in the quoted times of Subsection 2.1.3.4.

There is no difference in instruction timing between half word and full word operations except on multiply, divide and square root instructions.

When the relative address option (see Subsection 2.1.3.5) is used on operand addressing, instruction execution times are increased by one-half microsecond.

All instruction execution times that are shown in this document represent design goals. These times assume that a full memory cycle, including logic propagation times for addressing and control will require 2.0 microseconds. It is also assumed that memory access on a read operation will require 1.0 microseconds.

2.1.3.4 Instruction Descriptions

In describing each L-3050 instruction (see Subsections 2.1.3.4.1 through 2.1.3.4.7) the following notations are used:

E The instruction word's E bit.

F The instruction word's F field.

H The instruction word's H field.

h The contents of the selected accumulator, selected by the instruction's H field. h may be a 16-bit or 32-bit accumulator.

h+1 The contents of the next numbered accumulator that was selected by the instruction's H field.

L Represents the contents of the instruction location register. This number is the address of the next instruction in normal sequence.

n The number of bit positions shifted on a shift type instruction.

Y A general representation for the instruction's operand address.

() Parentheses represent the contents of the memory location that is addressed by the word within the parentheses.

$\|\ \|$ Absolute value.

$\wedge$ Logical AND function.

$\vee$ Logical inclusive OR function.

$\veebar$ Logical exclusive OR function.

$\rightarrow$ "Replaces."

Unless otherwise noted in the instruction descriptions, the interpretation of the instruction's E bit is to select a half or a full word operation, the H field selects an accumulator, the M field selects the operand addressing mode, and the S field selects an index register.

The term "process register" is used in most instruction descriptions. This term is used in place of "accumulators" because the register selected by the instruction's H field may be a 16-bit index register, a 16-bit accumulator or a 32-bit accumulator.

Table II-4 contains a summary of L-3050 instructions.

2.1.3.4.1 Arithmetic Class.

Add	General: h+(Y)→h	2.5 μsec
E = 0, ADH E = 1, ADF F = 10	The operand (Y) is algebraically added to the process register h. If arithmetic overflow occurs, the overflow indicator is set.	

E	F	NAME	MNE	E	F	NAME	MNE
0	00	HALT	HLT	1	00		
0	01	EXECUTE	EXE	1	01		
0	02	EXCHANGE HALF	EXH	1	02	EXCHANGE FULL	EXF
0	03	EXCHANGE DOUBLE HALF	EDH	1	03		
0	04	LOAD HALF	LSH	1	04	LOAD FULL	LSF
0	05	STORE HALF	STH	1	05	STORE FULL	STF
0	06	LOAD DOUBLE, HALF	LDH	1	06	LOAD DOUBLE FULL	LDF
0	07	STORE DOUBLE, HALF	SDH	1	07	STORE DOUBLE FULL	SDF
0	10	ADD HALF	ADH	1	10	ADD FULL	ADF
0	11	SUBTRACT HALF	SBH	1	11	SUBTRACT FULL	SBF
0	12	ADD HALF REPLACE	RAH	1	12	ADD FULL, REPLACE	RAF
0	13	SUBTRACT HALF REPLACE	RSH	1	13	SUBTRACT FULL, REPLACE	RSF
0	14	ADD ABSOLUTE HALF	AAH	1	14	ADD ABSOLUTE FULL	AAF
0	15	SUBTRACT ABSOLUTE HALF	SAH	1	15	SUBTRACT ABSOLUTE FULL	SAF
0	16	LOAD ABSOLUTE HALF	LAH	1	16	LOAD ABSOLUTE, FULL	LAF
0	17	LOAD COMPLEMENT, HALF	LCH	1	17	LOAD COMPLEMENT, FULL	LCF
0	20	EXCLUSIVE OR HALF	EOH	1	20	EXCLUSIVE OR FULL	EOF
0	21	INCLUSIVE OR HALF	IOH	1	21	INCLUSIVE OR FULL	IOF
0	22	LOGICAL AND HALF	ANH	1	22	LOGICAL AND FULL	ANF
0	23	MEMORY BANK DESIGNATE	MBD	1	23	BASE MEMORY DESIGNATE	MBB
0	24	REPLACES EXCLUSIVE OR, HALF	REH	1	24	REPLACES EXCLUSIVE OR, FULL	REF
0	25	REPLACES INCLUSIVE OR, HALF	RIH	1	25	REPLACES INCLUSIVE OR, FULL	RIF
0	26	REPLACE LOGICAL AND, HALF	RNH	1	26	REPLACE LOGICAL AND, FULL	RNF
0	27	MEMORY BANK ASSIGN	MBA	1	27		
0	30	MULTIPLY HALF	MPH	1	30	MULTIPLY FULL	MPF
0	31	DIVIDE HALF	DIH	1	31	DIVIDE FULL	DIF
0	32	DECREMENT H BY TWO	DIX	1	32	INCREMENT H BY TWO	ITX
0	33	DECREMENT H BY ONE	ITX	1	33	INCREMENT H BY ONE	IOX
0	34	TRANSFER ON INDICATORS	XFR	1	34		
0	35	TRANSFER AND STORE LINK	XLK	1	35		
0	36	TRANSFER ON CONSOLE SWITCH	XSW	1	36		
0	37			1	37		
0	40	TRANSFER OF HALF = 0	XZH	1	40	TRANSFER IF FULL = 0	XZF
0	41	TRANSFER IF HALF $\neq$ 0	XNH	1	41	TRANSFER IF FULL $\neq$ 0	XNF
0	42	TRANSFER IF HALF < 0	XLH	1	42	TRANSFER IF FULL < 0	XLF
0	43	TRANSFER IF HALF $\geq$ 0	XPH	1	43	TRANSFER IF FULL $\geq$ 0	XPF
0	44	SHIFT HALF	SHH	1	44	SHIFT FULL	SHF
0	45		DFP	1	45		
0	46		MFP	1	46		
0	47			1	47		
				1	52		
			SFR	1	53		
0	54	GATED COMPARE HALF	GCH	1	54	GATED COMPARE FULL	GCF
0	55	COMPARE HALF	CMH	1	55	COMPARE FULL	CMF
			SFQ	1	56	SQUARE ROOT FIXED	SQP
0	57			1	57		
0	60	SET LOWER BIT OF Y	SBL	1	60	SET LOWER BIT AND INTERRUPT	SLI
0	61	SET UPPER BIT OF Y	SBU	1	61	SET UPPER BIT AND INTERRUPT	SUI
0	62	RESET LOWER BIT OF Y	RBL	1	62	RESET LOWER BIT AND INTERRUPT	RLI
0	63	RESET UPPER BIT OF Y	RBU	1	63	RESET UPPER BIT AND INTERRUPT	RUI
0	64	TEST LOWER BIT FOR ZERO	TLZ	1	64	TEST AND SET LOWER BIT	TLI
0	65	TEST UPPER BIT FOR ZERO	TUZ	1	65	TEST AND SET UPPER BIT	TZI
0	66	TEST LOWER BIT FOR ONE	TLM	1	66	TEST AND RESET LOWER BIT	TNI
0	67	TEST UPPER BIT FOR ONE	TUN	1	67	TEST AND RESET UPPER BIT	TUI
0	70	MOVE AND ZERO, HALF	MZH	1	70	MOVE AND ZERO, FULL	MZF
0	71	MOVE AND INSERT, HALF	MIH	1	71	MOVE AND INSERT, FULL	MIF
0	72	STORE ALL ZEROS, HALF	SZH	1	72	STORE ALL ZEROS, FULL	SZF
0	74	DEVICE COMMAND	DEC	1	74	DEVICE COMMAND, SUICIDE	DES
0	75	INPUT TO REGISTER, HALF	ITH	1	75	INPUT TO REGISTER, FULL	ITF
0	76	OUTPUT FROM REGISTER, HALF	OFH	1	76	OUTPUT FROM REGISTER, FULL	OFF
0	77	NO OPERATION	NOP	1	77	DIAGNOSE	DIG

Table II-4. Summary of L-3050 Instructions 1771-5

Subtract	General: h - (Y)→h	2.5 μsec
E = 0, SBH E = 1, SBF F = 11	The operand (Y) is algebraically subtracted from process register h. If arithmetic overflow occurs, the overflow indicator is set.	
Replace Add	General: (Y) + h→(Y)	3.5 μsec
E = 0, RAH E = 1, RAF F = 12	The process register h is algebraically added to the operand at address Y. h is not changed. If arithmetic overflow occurs, the overflow indicator is set.	
Replace Subtract	General: (Y) - h→(Y)	3.5 μsec
E = 0, RSH E = 1, RSF F = 13	The process register h is algebraically subtracted from the operand at address Y. h is not changed. If arithmetic overflow occurs, the overflow indicator is set.	
Add Absolute	General: h + |(Y)|→h	2.5 μsec
E = 0, AAN E = 1, AAF F = 14	The operand (Y) is algebraically added to process register h, if it is positive or it is algebraically subtracted from process register h if it is negative. If arithmetic overflow occurs, the overflow indicator is set.	
Subtract Absolute	General: h - |(Y)|→h	2.5 μsec
E = 0, SAH E = 1, SAF F = 15	The operand (Y) is algebraically subtracted from process register h if it is positive or it is algebraically added to process register h if it is negative. If arithmetic overflow occurs, the overflow indicator is set.	
Load Absolute	General: |(Y)|→h	2.5 μsec
E = 0, LAH E = 1, LAF F = 16	The operand (Y) replaces the process register h if it is positive. If (Y) is negative it is converted to the equivalent positive number (two's complement) and replaces h. If the operand (Y) is a minus one, the overflow indicator will be set.	

Load Complement	General: $-(Y) \rightarrow h$	2.5 μsec
E = 0, LCH E = 1, LCF F = 17	If the operand (Y) is a negative number, the positive equivalent is loaded into process register h. If the operand (Y) is a positive number, the negative equivalent is loaded into process register h. -(Y) represents the two's complement of (Y). If the operand (Y) is a minus one (-1.0) the overflow indicator will be set.	
Multiply	General: $h \times (Y) \rightarrow h, h+1$	if E = 0:6 μsec if E = 1:10 μsec
E = 0, MPH E = 1, MPF F = 30	The operand (Y) is multiplied by process register h. The result is a double word product that replaces the process register pair, h and h + 1. Overflow may occur on the addition if minus one is multiplied times minus one. If overflow occurs, the overflow indicator is set.	
Divide	General: $h, h+1 \div (Y) \rightarrow h$, REM $\rightarrow h+1$	if E = 0:10 μsec if E = 1:18 μsec
E = 0, DIH E = 1, DIF F = 31	The process register pair, h, h + 1 is divided by the operand (Y). The quotient plus sign is stored into process register h. The remainder is stored into process register, h + 1. The sign of the remainder equals the sign of the dividend. Overflow represents an illegal divide when the divisor (Y) is less than or equal to the dividend.	
Square Root	General: $\sqrt{(Y)} \rightarrow h$	18 μsec
E = 1, SQP F = 56	The square root of the full, fixed point word at address Y is extracted and stored into accumulator h. If the operand is negative, the overflow indicator is set.	

2.1.3.4.2 Logical Class

Exclusive OR E = 0, EON E = 1, EOF F = 20	General: h ⊻ (Y)⟶h The operand (Y) is logically matched with process register h. For every one bit in (Y) and corresponding zero bit in h a one is inserted into that bit position of h. For every one bit in (Y) and corresponding one bit in h a zero is inserted into that bit position of h. Zero bits in (Y) do not modify the corresponding bit positions in h.	2.5 μsec
Inclusive OR E = 0, IOH E = 1, IOF F = 21	General: h ∨ (Y)⟶h The operand (Y) is logically merged with the process register h. For every one bit in (Y) a one is inserted into that bit position of h, regardless of its original state. Zero bits in (Y) do not modify the corresponding bit position in h.	2.5 μsec
Logical AND E = 0, ANH E = 1, ANF F = 22	General: h ∧ (Y)⟶h The operand (Y) is logically masked with the process register h. For each zero bit in (Y) the corresponding bit position in h is reset to a zero. For each one bit in (Y) the corresponding bit position in h remains unchanged.	2.5 μsec
Replace Exclusive OR E = 0, REH E = 1, REF F = 24	General: (Y) ⊻ h⟶(Y) Process register h is logically matched with operand (Y). For every one bit in h the corresponding bit position of (Y) is set to a one if it was a zero or it is reset to a zero if it was a one. Zero bits in h will not change the corresponding bit positions in (Y).	3.5 μsec

Replace Inclusive OR E = 0, RIH E = 1, RIF F = 25	General: (Y) V h⟶(Y) Process register h is logically merged with the operand (Y). For every one bit in h the corresponding bit position of (Y) is set to a one regardless of its original state. For every zero bit in h the corresponding bit position of (Y) is not changed.	3.5 μsec
Replace Logical AND E = 0, RNH E = 1, RNF F = 26	General: (Y) Λ h⟶(Y) Process register h is logically masked with the operand (Y). For every one bit in h the corresponding bit position in (Y) is not changed. For every zero bit in h the corresponding bit position in (Y) is reset to a zero.	3.5 μsec
Move and Zero E = 0, MZH E = 1, MZF F = 70	The address field of this instruction is used to specify the selected register to be used as the mask register and the selected register that will receive the result of the instruction (the destination register). The register to be modified (the source register) is specified by the instruction's h field. This instruction starts with a shift operation; shift options of: left or right, circular or linear shift are provided. Bit positions 5 to 0 specify the number of shifts. Bit positions 11 to 9 select a register that will be logically ANDed with the shifted result. Bit positions 14 to 12 specify the register number that receives this result. The format of this instruction if shown in Figure 2-6.	4.0 + 0.1 μsec

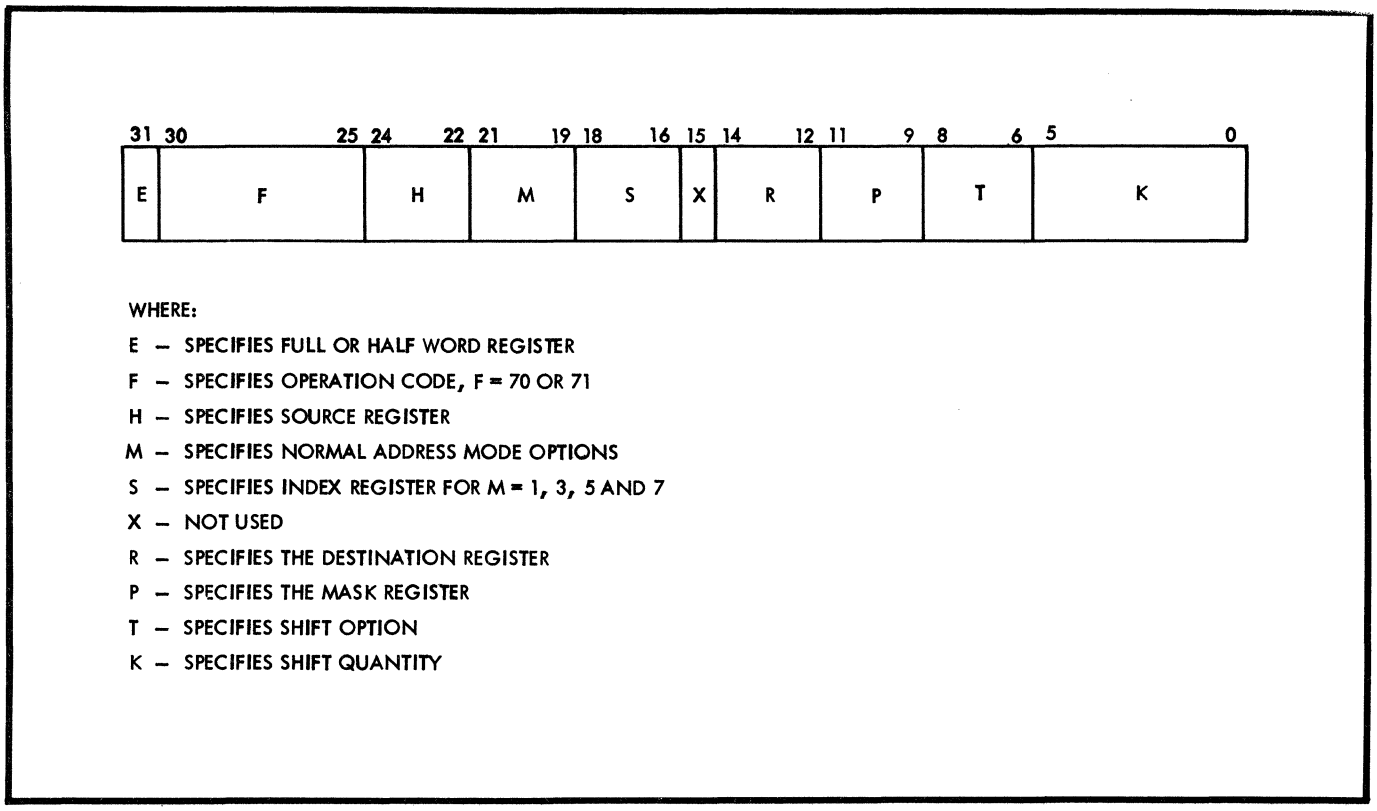


Figure 2-6. Move Instruction Word Format 1771-6

Move and Insert		4.0 + 0.1 μsec
E = 0, MIH E = 1, MIF F = 71	This instruction operates similar to the move and zero instruction described previously, except that the ANDed result of the mask and the shifted source are inserted into the designation register without changing bit positions that correspond to zeros in the mask register.	

2.1.3.4.3 Control Class

Halt	General: Half if H = 0 or SWi = Hi	2.0 μsec
E = 0, HLT F = 00	The half word operand (Y) is stored into the address field of the instruction register and the full word at address Y is stored into the computer's memory register for console display. If H = 0 or if any one of the three conditional halt switches, SW, on the console is "on" and the corresponding bit position of the H field is a one, the computer halts. Manual restart is required.	

Execute E = 0, EXE F = 01	General: (Y)→CR The operand address, Y, is used as the address of the next instruction. This 32-bit word, (Y) is placed into the computer's instruction register, CR. When this instruction is executed, the instruction location register, LL, is not incremented so that the next instruction is obtained in normal sequence.	2.0 μsec
Transfer on Indicators E = 0, XFR F = 34	General: (Y)→L if H = Indicator On A bit-for-bit comparison is made between the instruction's H field and the conditions of the three indicator flip-flops: equal, less than and greater. Only one of these indicators may be set at one time as a result of a compare or gated compare instruction. If any one bit of the H field corresponds to one of the indicators set "ON" a transfer occurs. Otherwise the next instruction in sequence is executed. If the H field if all zeros and the overflow indicator is set ON, a transfer on overflow occurs.	1.5 μsec
Transfer, Unconditional and Store Link E = 0, XLK F = 35	General: L→h, (Y)→L The contents of the instruction location register L which contains the address of the next instruction in sequence is stored into half word, process register h. The half word operand (Y) becomes the address of the next instruction and replaces the original contents of the instruction location register, LL.	1.5 μsec
Transfer On Console Switch E = 0, XSW F = 36	General: (Y)→L if SWi = Hi A bit-for-bit comparison between the On and Off states of three conditional jump switches, SW, on the console and the H field is made. If any switch is "On" and its corresponding bit in the H field is a "one," a transfer to address	1.5 μsec

Transfer On Console Switch (cont'd)	(Y) occurs. Otherwise the next instruction in sequence is executed. h and (Y) are not changed. If H = 0, an unconditional transfer occurs.	
Transfer if Zero E = 0, XZH E = 1, XZF F = 40	General: (Y)→L if h = 0 If process register h is all zeros, a transfer to address (Y) occurs. Otherwise, the next instruction in sequence is executed. h and (Y) are not changed.	1.5 μsec
Transfer if Not Zero E = 0, XNH E = 1, XNF F = 41	General: (Y)→L if h ≠ 0 If process register h is not all zeros, a transfer to address (Y) occurs. Otherwise, the next instruction in sequence is executed. h and (Y) are not changed.	1.5 μsec
Transfer if Negative E = 0, XLH E = 1, XLF F = 42	General: (Y)→L if h < 0 If the sign bit of process register h is a one (negative) a transfer to address (Y) occurs. Otherwise, the next instruction in sequence is executed. h and (Y) are not changed.	1.5 μsec
Transfer if Positive E = 0, XPH E = 1, XPF F = 43	General: (Y)→L if h > 0 If the sign bit of process register h is a zero (positive), a transfer to address (Y) occurs. Otherwise, the next instruction in sequence is executed. h and (Y) are not changed.	1.5 μsec
Gated Compare E = 0, GCH E = 1, GCF F = 54	General: |(Y) - h| is compared with h6 The absolute value of the difference between the operand (Y) and the selected process register h, is compared against the contents of process register number 6. The three indicators—equal, greater and less than—are first reset and then the proper indicator is set according to the results of the comparison. (Y), h and h6 are not changed.	3.5 μsec

Compare	General: (Y) - h is compared with zero	2.5 μsec
E = 0, CMH E = 1, CMF F = 55	The algebraic value of the difference between the operand (Y) and the selected process register h, is compared against all zeros. The three indicators—equal, greater and less than—are first reset and then the proper indicator is set according to the results of the comparison. (Y) and h are not changed.	
Set Lower Bit	General: 1⟶(Y)i, i = 0-7	3.5 μsec
E = 0, SBL E = 1, SLI F = 60	The H field specifies a number, i, from 7 to 0 of a bit position (7-0) within half word operand (Y) that will be set to a one. Other bits of (Y) and h are not changed. If E = 1 and the PAR is addressed, a program level change is attempted. If E = 1, the I/O interrupt lockout flip-flop is reset.	
Set Upper Bit	General: 1⟶(Y)i + 8, i = 0-7	3.5 μsec
E = 0, SBU E = 1, SUI F = 61	The H field specifies a number, i, between 7 and 0, plus eight, that represents a bit position (15-8) within half word operand (Y) that will be set to a one. Other bits of (Y) and h are not changed. If E = 1 and the PAR is addressed, a program level change is attempted. If E = 1, the I/O interrupt lockout flip-flop is reset.	
Reset Lower Bit	General: 0⟶(Y)i, i = 0-7	3.5 μsec
E = 0, RBL E = 1, RLI F = 62	The H field specifies a number, i, between 7 and 0, that represents a bit position (7-0) within half word operand (Y) that will be reset to a zero. Other bits of (Y) and h are not changed. If E = 1 and the PAR is addressed, a program level change is attempted. If E = 1, the I/O interrupt lockout flip-flop is reset.	

Reset Upper Bit E = 0, RBU E = 1, RUI F = 63	General: 0 → (Y)i + 8, i = 0-7 The H field specifies a number, i, between 7 and 0, plus eight, that represents a bit position (15-8) within half word operand (Y) that will be reset to zero. Other bits of (Y) and h are not changed. If E = 1 and the PAR is addressed, a program level change is attempted. If E = 1, the I/O interrupt lockout flip-flop is reset.	3.5 μsec
Test Lower Bit, Jump if Zero E = 0, TLZ E = 1, TLI F = 64	General: L + 1 → L if (Y)i = 0, i = 0-7 The H field specifies a bit position (7-0) within the half word operand (Y) to be tested. If this bit is a zero the instruction location register, LL, is incremented causing the next instruction in sequence to be skipped. h and (Y) are not changed. If E = 1, the I/O interrupt lockout flip-flop is set.	3.5 μsec
Test Upper Bit, Jump if Zero E = 0, TUZ E = 1, TZI F = 65	General: L + 1 → L if (Y)i + 8 = 0, i = 0-7 The H field, plus eight, specifies a bit position (15-8) within half word operand (Y) to be tested. If this bit is a zero, the instruction location register, LL, is incremented causing the next instruction in sequence to be skipped. h and (Y) are not changed. If E = 1, the interrupt lockout flip-flop is set.	3.5 μsec
Test Lower Bit, Jump if One E = 0, TLN E = 1, TNI F = 66	General: L + 1 → L if (Y)i = 1, i = 0-7 The H field specifies a bit position (7-0) within half word operand (Y) to be tested. If this bit is a one, the instruction location register, LL, is incremented causing the next instruction in sequence to be skipped. h and (Y) are not changed. If E = 1, the interrupt lockout flip-flop is set.	3.5 μsec

Test Upper Bit, Jump if One E = 0, TUN E = 1, TUI F = 67	General: L + 1 → L if (Y)i = 8-1, i = 0-7 The H field, plus eight, specifies a bit position (15-8) within half word operand (Y) to be tested. If this bit is a one, the instruction location register, LL, is incremented causing the next instruction in sequence to be skipped. h and (Y) are not changed. If E = 1, the interrupt lockout flip-flop is set.	3.5 μsec

2.1.3.4.4 Indexing Class. In the L-3050 a set of eight 16-bit registers is provided for each of 64 program levels. These registers may be used for either index registers or accumulators. Consequently, all instructions that refer to the contents of one of these registers may be used to modify or test index registers. However, four special instructions which test and modify the 16-bit registers are provided for control on indexing.

Decrement H by Two E = 0, DTX F = 32	General: h - 2 → h, (Y) → L if h ≠ 0 or 1 Process register h is treated as an unsigned 16-bit number. This number is reduced by two until it contains all zeros or all zeros with a one in bit position 0. In this case h is forced to all zeros and the next instruction is taken in sequence. Otherwise, a transfer to address (Y) occurs.	2.0 μsec
Increment H by Two E = 1, ITX F = 32	General: h + 2 → h, (Y) → L if h ≠ 0 or 1 Process register h is treated as an unsigned 16-bit number. A plus 2 is added to this number until it reaches all zeros or all ones with a zero in bit position 0. In this case, h is forced to all zeros and the next instruction is taken in sequence. Otherwise, a transfer to address (Y) occurs.	2.0 μsec

Decrement H by One E = 0, DOX F = 33	General: h - 1⟶h, (Y)⟶L if h ≠ 0 Process register h is treated as an unsigned 16-bit number. This number is reduced by one until it reaches all zeros. When it equals all zeros it is not decremented and the next instruction is taken in sequence. Otherwise, a transfer to address (Y) occurs.	2.0 μsec
Increment H by One E = 1, IOX F = 33	General: h + 1⟶h, (Y)⟶L if h < 0 Process register h is treated as an unsigned 16-bit number. This number is increased by one until it reaches all zeros. When it equals all zeros it is not incremented and the next instruction is taken in sequence. Otherwise, a transfer to address (Y) occurs.	2.0 μsec

2.1.3.4.5 Data Handling Class

Exchange E = 0, EXH F = 02	General: (Y)⟶h, h⟶(Y) The operand (Y) is loaded into the specified process register h. The process register h is stored into address Y.	3.5 μsec
Exchange Double E = 1, EDH F = 02	General: (Y)⟶h, (Y + 1)⟶h + 1 H⟶(Y), H + 1⟶(Y + 1) The double half word operand (Y), (Y + 1) is loaded into the specified process register h, h + 1, and the original contents of the process register pair is stored into address Y and Y + 1.	3.5 μsec
Load H E = 0, LSH E = 1, LSF F = 04	General: (Y)⟶h The operand (Y) replaces the contents of the process register specified by H. (Y) is not changed.	2.5 μsec

Store H	General: h → (Y)	2.5 μsec
E = 0, STH E = 1, STF F = 05	The process register h is stored into address Y. h is not changed.	
Load Double	General: (Y) → h, (Y + 1) → h + 1	2.5 μsec
E = 0, LDH E = 1, LDF F = 06	The double word operand (Y), (Y + 1) replaces the contents of the process register pair, h, h + 1. On modes 2 and 3, a 16-bit operand replaces the specified process register h and the other half of the process register pair is set to all zeros.	
Store Double	General: h → (Y), h + 1 → (Y + 1)	2.5 μsec
E = 0, SDH E = 1, SDF F = 06	The process register pair, h, h + 1, is stored in memory address Y and Y + 1. h, h + 1 are not changed.	
Shift		1.5 + 0.1 μsec
E = 0, SHH E = 1, SHF F = 44	The address field of the instruction is used to specify the type of shift instruction and the number of bits to be shifted. (This address may be modified with the usual address modes if desirable.) Bit positions 10 through 6 of the instruction's address field specify the shift operation as is shown in Figure 2-7. Seventeen different shift operations are provided. Bit positions 5 through 0 specify the number of positions to be shifted. Note that reflect, normalize, shift and count are included with the shift operations.	
Store All Zeros	General: 0 → (Y)	2.5 μsec
E = 0, SZH E = 1, SZF	The contents of address Y is reset to all zeros. The H field is not used. h is not changed.	

SHIFT TYPE OPTIONS							
OCTAL T	DIRECTION T_{10}	END BITS T_9	COMMAND T_8	REGISTERS T_7	WORD TYPE T_6	REGISTERS E = 0, 16 BIT / E = 1, 32 BIT	COMMENT
00	0 RIGHT	0 LINEAR	0 NORMAL	0 SINGLE	0 ALGEBRAIC	S → NOT CHANGED	SIGN EXTENDED
01	0 RIGHT	0 LINEAR	0 NORMAL	0 SINGLE	1 LOGICAL	0 → NOT CHANGED	
02	0 RIGHT	0 LINEAR	0 NORMAL	1 DOUBLE	0 ALGEBRAIC	S → S	SIGN EXTENDED
03	0 RIGHT	0 LINEAR	0 NORMAL	1 DOUBLE	1 LOGICAL	0 →	
11	0 RIGHT	1 CIRCULAR	0 NORMAL	0 SINGLE	1 LOGICAL	NOT CHANGED	
13	0 RIGHT	1 CIRCULAR	0 NORMAL	1 DOUBLE	1 LOGICAL		
20	1 LEFT	0 LINEAR	0 NORMAL	0 SINGLE	0 ALGEBRAIC	S ← 0 NOT CHANGED	
21	1 LEFT	0 LINEAR	0 NORMAL	0 SINGLE	1 LOGICAL	0 NOT CHANGED	
22	1 LEFT	0 LINEAR	0 NORMAL	1 DOUBLE	0 ALGEBRAIC	S ← S ← 0	
23	1 LEFT	0 LINEAR	0 NORMAL	1 DOUBLE	1 LOGICAL	0	
31	1 LEFT	1 CIRCULAR	0 NORMAL	0 SINGLE	1 LOGICAL	NOT CHANGED	
33	1 LEFT	1 CIRCULAR	0 NORMAL	1 DOUBLE	1 LOGICAL		
17	0 RIGHT	1 CIRCULAR	1 REFLECT	1 DOUBLE	1 LOGICAL		
24	1 LEFT	0 LINEAR	1 NORMALIZE	0 SINGLE	0 ALGEBRAIC	0'S IF S = 0, 1'S IF S = 1; S ← 0 NOT CHANGED	RESIDUE → R
25	1 LEFT	0 LINEAR	1 SHIFT AND COUNT	0 SINGLE	1 LOGICAL	0 NOT CHANGED	1'S COUNT → R
26	1 LEFT	0 LINEAR	1 NORMALIZE	1 DOUBLE	0 ALGEBRAIC	S ← S	RESIDUE → R
35	1 LEFT	1 CIRCULAR	1 SHIFT AND COUNT	0 SINGLE	1 LOGICAL	NOT CHANGED	1'S COUNT → R

15	14	12 11	6 5	0
X	R	T	K	

WHERE:

X – NOT USED

R – SPECIFIES DESTINATION REGISTER ON NORMALIZE AND SHIFT AND COUNT

T – SPECIFIES TYPE OF SHIFT

K – SPECIFIES SHIFT QUANTITY

Figure 2-7. L-3050 Shift Instructions

1771-7

2.1.3.4.6 Input/Output Class

External Device Command E = 0, DEC E = 1, DES F = 74	General: (Y)15-8 → I/O Device: (Y)5-0 The operand (Y) is transmitted over the input/output data lines. The I/O device that is assigned the station or substation number specified by bits 5-0 of (Y) accepts bits 15-8 of (Y) as a special command. H is not used. h is not changed. (Y)7-6 are not used. If E = 1 the current program level status bit is reset to zero and a program level change occurs. If E = 1, the I/O interrupt lockout flip-flop is reset.	2.5 μsec
Input to Register E = 0, ITH E = 1, ITF F = 75	General: I/O: (Y)5-0 → h The I/O device at the station or substation number specified by bits 5-0 of (Y) transmits up to 32 bits of information on the I/O data lines. This information is stored into process register h. (Y)15-6 are not used. If E = 0, process register pair h and h + 1 are used. If E = 1, 32-bit accumulator h is used.	2.5 μsec
Output from Register E = 0, OFH E = 1, OFF F = 76	General: h → I/O: (Y)5-0 Process register h is transmitted from the computer over the I/O data lines. Bits 5-0 of (Y) address the I/O station or substation whose device should receive this data. If E = 0, process register pair h and h + 1 are used. If E = 1, 32-bit accumulator h is used.	2.5 μsec

2.1.3.4.7 Miscellaneous Class

Memory Bank Designator E = 0, MBD F = 23	General: (Y)11-00 → LD11-00 The 12 least significant bit positions of the half word operand (Y) replace the 12 least significant bit positions of the memory extension register, LD. This 12-bit word is considered to be three four-bit fields. Each	2.5 μsec

Memory Bank Designator (cont'd)	field provides four most significant address bits when the D field of an address is 01_2, 10_2 or 11_2, in the fixed address option.	
Memory Bank (Base) Designator E = 1, MBB F = 23	General: (Y)15-12 → LD15-12 The four most significant bits of the half word operand (Y) replaces the four most significant bit positions of the memory extension register, LD. These four bits provide memory address extension when the D field of an address in 00_2 in the fixed address option.	2.5 μsec
Memory Bank Assignment E = 0, MBA F = 27	General: (Y) → Memory Bank Number The half word operand (Y) is transmitted to the memory module that is addressed by bit positions 15-12 of (Y). Bit positions 5 and 4 of (Y) command the memory module to use bit positions 9-6 of (Y) as a new bank address and to become active or inactive. Bit positions 3 and 2 of (Y) set or reset two memory protection flip-flops in the selected memory module.	2.5 μsec
Diagnose E = 1, DIG F = 77	The address field of this instruction is decoded to provide a variety of special self-test commands.	
No Operation F = 37 47 57 77	These are nonused operation codes provided for future expansion. At present no operation will occur and the next instruction in sequence will be executed.	

2.1.3.5 Addressing Options

Two addressing options are provided with the L-3050. These are a "fixed" addressing option and a "relative" addressing option. In the fixed option, memory addresses are generated with the memory extension register, LD, as was described previously. In the relative option, addresses are generated by addition of the base address register, LB, to memory addresses. In this addition, the LB register is shifted left by two bits with respect to the 16-bit address that is added. This yields an 18-bit address.

The two addressing options are independent. Either option or both may be used for instruction addressing or operand addressing. Therefore, it is possible to execute instructions which are located in relative positions and refer to fixed data. It is also possible to execute programs from fixed locations that operate on data that is located relative to the base address register.

The relative addressing option is selected by the programmed setting of two control bits. These two bits are located in the indicator word for each program level.

One of these bits is called the program address flag, PF. If PF is set to a one, the program will select instructions from memory addresses that are relative to the contents of the LB register. If PF is set to a zero, the program will select instructions from memory that are directly addressed by the instruction location register, LL, and the LD register.

The second bit is called the data address flag, DF. If DF is set to a one, the contents of the LB register are added to each instruction's operand address. If DF is set to a zero, all operand addresses are formed with the LD register.

The programmed control of PF and DF is conveniently provided because the indicator words are addressable as operands in memory and the active indicator word is addressable as an operand with special address 004032_8. Furthermore, the state of the active program address flag, PF, may be modified by execution of a transfer instruction. Whenever a transfer instruction is executed, the least significant bit of the operand address, the W field, replaces the PF bit of the indicator word, and the LB register is added to the D and A fields of the instruction. If the W field of a transfer instruction is zero, the PF bit is reset and a fixed address is generated for the new instruction address.

The PF is not used in the execution of transfer instructions. The W field specifies the relative or fixed instruction addressing option. PF is examined at the start of all programs to initially cause the sum of the LB register and LL register to

M	ADDRESS MODE	DATA ADDRESS OPTION DF	OPERAND
0	DIRECT	0 1	(A) (A + B)
1	DIRECT, INDEXED	0 1	(A + S) (A + B + S)
2	LITERAL	0 1	A A
3	LITERAL, INDEXED	0 1	A + S A + S
4	INDIRECT	0 1	((A)) ((A + B) + B)
5	INDEXED, INDIRECT	0 1	((A + S)) ((A + B + S) + B)
6	INDIRECT, INDEXED	0 1	((A) + S)) ((A + B) + S) + B)
7	RELATIVE, S = 0	0 1	(A + L) (A + L + B)
7	RELATIVE, S ≠ 0	0 1	(A + S + L) (A + S + L + B)

Table II-5. L-3050 Operand Addresses 1771-8

replace the contents of the LL register. When a program is operating in the relative option for instruction access (PF = 1) is interrupted, the LB register is automatically subtracted from the instruction address register, LL, before LL is returned to its fixed location in memory.

In the execution of a transfer and link instruction with a program that is operating with relative instruction addressing, (PF = 1), the LB register is automatically subtracted from the instruction location register, LL, (this is the "link" address) before LL is stored in the designated process register. A third control bit, the link flag, LF, in the indicator word is set to a one.

The two addressing options may be used with the nine addressing modes of each L-3050 instruction. Addressing modes are selected by the instruction's M field as was described above. Table II-5 summarizes the possible data addresses that can be generated. Table II-6 summarizes the possible instruction addresses that can be generated on transfer instructions. In Tables II-5 and II-6 the following notations are used:

M	ADDRESS MODE	ADDRESS OPTION		ADDRESS
		DF	W	
0	DIRECT	0	0	(A) → L, 0 → PF
		0	1	(A) + B → L, 1 → PF
		1	0	(A + B) → L, 0 → PF
		1	1	(A + B) + B → L, 1 → PF
1	DIRECT, INDEXED	0	0	(A + S) → L, 0 → PF
		0	1	(A + S) + B → L, 1 → PF
		1	0	(A + S + B) → L, 0 → PF
		1	1	(A + S + B) + B → L, 1 → PF
2	LITERAL	0	0	A → L
		0	1	A + B → L, 1 → PF
		1	0	A → L
		1	1	A + B → L, 1 → PF
3	LITERAL, INDEXED	0	0	A + S → L, 0 → PF
		0	1	A + S + B → L, 1 → PF
		1	0	A + S → L, 0 → PF
		1	1	A + S + B → L, 1 → PF
4	INDIRECT	0	0	((A)) → L, 0 → PF
		0	1	((A)) + B → L, 1 → PF
		1	0	((A + B) + B) → L, 0 → PF
		1	1	((A + B) + B) + B → L, 1 → PF
5	INDEXED, INDIRECT	0	0	((A + S)) → L, 0 → PF
		0	1	((A + S)) + B → L, 1 → PF
		1	0	((A + S + B) + B) → L, 0 → PF
		1	1	((A + S + B) + B) + B → L, 1 → PF
6	INDIRECT, INDEXED	0	0	((A) + S) → L, 0 → PF
		0	1	((A) + S) + B → L, 1 → PF
		1	0	((A + B) + S) + B → L, 0 → PF
		1	1	((A + B) + S + B) + B → L, 1 → PF
7	RELATIVE, NOT INDEXED	0	0	A + L → L, 0 → PF
	S = 0	0	1	A + L + B → L, 1 → PF
		1	0	A + L → L, 0 → PF
		1	1	A + L + B → L, 1 → PF
8	RELATIVE, INDEXED	0	0	A + S + L → L, 0 → PF
	S ≠ 0	0	1	A + S + L + B → L, 1 → PF
		1	0	A + S + L → L, 0 → PF
		1	1	A + S + L + B → L, 1 → PF

Table II-6. L-3050 Transfer Instruction Addresses 1771-9

A	The contents of the instruction's address fields D, A, and W
B	The contents of the active LB register
DF	Active data address flag
L	The contents of the active LL register
M	The octal number in the instruction's M field
PF	Active program address flag
S	The contents of the process register selected by the instruction's S field
W	Least significant bit of instruction's operand address field
( )	Contents of the memory location whose address is the sum of the quantities within the parentheses
⟶	"Replaces contents of"

2.1.4 Input/Output

The input/output control (IOC) unit of the L-3050 processor provides control for the execution of data communication with system peripheral devices. This functional unit is designed to perform this communication with two classes of operation. These are: (1) by execution of programmed input/output instructions and, (2) independent of instruction execution at the peripheral device rate.

2.1.4.1 Programmed Input/Output Class

Three input/output instructions: input to register (ITR), output from register (OFS) and device command (DEC) are provided for programmed communication. A description of these instructions was given in Subsection 2.1.3.4.6.

When these instructions are encountered by the instruction control unit of the processor, a special request signal is transmitted to the IOC. When the IOC is not processing I/O requests it will accept the instruction from the instruction control unit and execute it. The instruction control unit waits in the I/O instruction until the IOC signals that it has started to execute the I/O instruction.

The DEC instruction is useful to command a peripheral device to perform its special functions. It is also used to select one of several devices that are sharing a buffer or single I/O address. The ITR instruction is useful to interrogate status messages from the peripheral devices. The OFR instruction is useful to output up to 32 bits in parallel to set indicators or to provide a programmed output operation.

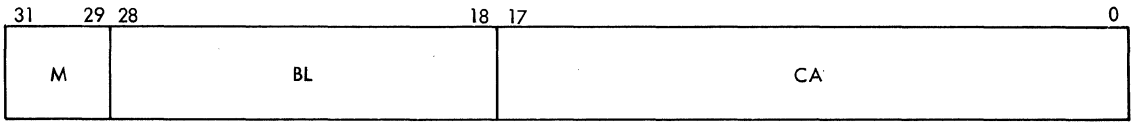


Figure 2-8. Input/Output Key Word Format 1771-10

2.1.4.2 Automatic Input/Output Class

Data communication which is independent of instruction execution is controlled by special I/O key words and termination words. There is a set of 64 key words and 64 termination words for control of up to 64 peripheral devices. The programmer should initialize these words prior to initiating an automatic data communication.

2.1.4.2.1 Key Word. The key word contains a field that specifies the I/O mode of communication, the block length (in words or characters) of the transmission and the address of the word in memory. The key word's address in memory is associated with the peripheral device number that is requesting service. When a request for service is acknowledged by the IOC the associated key word is accessed from the processor's base memory. The word or character is received or transmitted. The block length field of the key word is decremented by one and the current address field is incremented by two for each full word transferred or by one for every two characters transferred. The key word is then returned to memory.

The I/O key word has the format that is shown in Figure 2-8 where:

M = Mode, bit positions 30 to 28 — This 3-bit field specifies one of the following modes of operation:

0 — inactive

1 — alarm

2 — full word input

3 — full word output

4 — character input, no program level change upon block completion

5 — character output, no program level change upon block completion

6 — character input, program level change upon block completion

7 — character output, program level change upon block completion

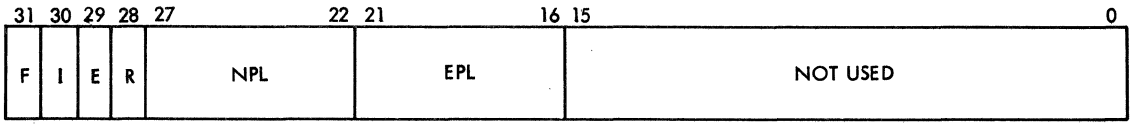


Figure 2-9. Input/Output Termination Word 1771-11

BL = Block Length, bit positions 28 to 18 — This 11-bit field specifies either the number of words or number of characters in a block data transmission or the number of time increments in the alarm mode.

CA = Current Address, bit positions 17 to 0 — This 18-bit field specifies the half word address of the memory location from which the current 32-bit word or two eight-bit characters are accessed in an output mode, or in which they are stored in an input mode.

2.1.4.2.2 Termination Word. The termination word is used to control interrupts from peripheral devices and program level change due to completion of transmission or receipt of a full block of data in character modes 6 and 7. The termination word that is associated with the peripheral device's address is obtained from the processor's base memory whenever: (1) an interrupt request is received, (2) an error is detected and, (3) the key word's block length field has reached zero in I/O modes 6 and 7.

The termination word has the format shown in Figure 2-9 where:

F = Block Complete, bit 31 — The F bit is set following the completion of the transfer of a block of data in character modes 6 or 7. This is detected when the block length field of the associated key word has been decremented to zero. The F bit indicates that no error was detected during transmission or receipt of the characters. The F bit is also set in the "alarm" mode when the block length field is decremented to 0.

I = Indicator, bit 30 — The I bit is set whenever an interrupt request is received from a peripheral device.

E = Device Error, bit 29 — The E bit is set whenever the peripheral device transmits an error signal or data with incorrect parity.

R = IOC Detected Error, bit 28 — The R bit is set whenever the IOC detects a memory parity error on output, a key word with mode zero, or an interrupted "burst" transmission.

NPL = Normal Program Level, bits 27 to 22 — This six-bit field is the binary number of the bit position that will be set in the program status register whenever the F or I bits of the termination word are set.

EPL = Error Program Level, bits 21 to 16 — This six-bit field is the binary number of the bit position that will be set in the program status register whenever the E or R bits of the termination word are set.

2.1.4.2.3 Modes of Operation — The M field of the I/O key word determines the mode of control that the IOC will execute whenever it processes a request from a peripheral device. The modes of operation are as follows:

M = 0, Inactive Mode — If the IOC detects that the mode field is all zeros in the key word, it obtains the corresponding termination word, sets its R bit and transmits an "end of transmission" signal to the peripheral device that was assigned the key word. The EPL field of the termination word is used to specify the status bit in the program activity register that is set to a "one." The key word is not modified.

M = 1, Alarm Mode — In the alarm mode, the block length field, BL, of the key word is used as an event counter. Each time a request from an external source with this key word is serviced the BL field is decremented. The CA field is not modified. No data transmission occurs. The request is usually provided from an interface unit with a real-time clock source.

When the BL field reaches zero, the corresponding termination word is obtained from memory and its F bit is set to a one. The NPL field of this word is used to select a status bit in the program activity register. This status bit is set to a "one." An end of transmission signal is transmitted to the interface unit. Because the BL field is 11 bits, up to 2048 time intervals may be counted. The programmer has normal access to the key words to examine the BL field because they are addressable in memory.

M = 2 or 3, Full Word Input or Output — These modes are the normal modes for transmission of full words. Words can be any size from 1 to 32 bits, but each request for an input or output addresses one word in memory and the address field of the key word, CA, is incremented to the next full word address. The least significant bit position, bit 0, of the CA field is ignored. The block length field, BL, is decremented for each word received or transmitted.

The block length number may be any number from 0 to 2047. The block length may be initially zero to allow more than 2048 words to be transferred with the same key word. Whenever the BL field of the key word is counted from 1 to 0, the IOC transmits an End of Transmission, EOT, signal to the sending or receiving device. The buffer unit for this device may be designed to count EOT signals to control block lengths. When it has reached its maximum, it can signal the IOC via an interrupt request.

The IOC does not access the termination word in modes 2 and 3 each time the block length is counted from 1 to 0. The peripheral device is expected to signa the IOC when it wishes to discontinue communication.

M = 4 or 5, Character Input or Output, No Program Level Change on BL = 0 — Data is received or transmitted as eight-bit characters. This data is unpacked from a 16-bit word on output and packed into a 16-bit word on input from left to right. Each half word is addressed by the key word's CA field. The least significant bit of the key word's BL field selects left or right character within the half word. If BL is even, the left character is selected. If BL is odd, the right character is selected.

Block length may be any number from 0 to 2047. Each time the BL field of the key word is decremented from 1 to 0, an EOT signal is transmitted to the peripheral device. The corresponding termination word is not accessed which is similar to the operation in modes 2 and 3.

M = 6 or 7, Character Input or Output with Program Level Change on BL = 0 — Data is received or transmitted as eight-bit characters as in modes 4 and 5 with the following exception. Each time the key word's BL field is decremented from 1 to 0, the corresponding termination word is accessed. The F bit of the termination word is set to a one if no errors were detected. The NPL field of the termination word is used to specify a bit position within the program status register that is set to a "one." Should this bit position be "enabled" with a one-bit in the same position of the program enable register, and should this bit position represent a higher level program than the current program level, a program level change will occur at the end of the current instruction.

2.1.4.2.4 Types of Operation. The IOC of the L-3050 communicates with external devices in five types of operation. The type of operation is determined by the external device via transmitted control signals. The types of operation are as follows:

(1) Single word or character transmission

(2) Burst of words or characters transmission

(3) Normal interrupt

(4) Error detection

(5) Program load (bootstrap)

2.1.4.2.4.1 Single Word or Character. Normally, the interface buffer of a peripheral device is commanded to transmit or receive data by a programmed Device Command (DEC) instruction. This instruction is executed after the programmer has initialized the key word and termination word that are associated with the device's I/O address. The device then signals the IOC with a request for service at its own rate. Each time a request is acknowledged by the IOC, the proper key word is obtained from memory, the word or character is transferred, and the key word is modified and returned to memory.

This operation is accomplished in 4.0 microseconds.

2.1.4.2.4.2 Burst Transmission. In this type of operation, more than one word or character may be transmitted with each request for service. The peripheral device keeps its request line "true" until it has received or transmitted as many words or characters as it desires.

The first word or character transmission requires 4.0 microseconds and each successive word or character requires 2.0 microseconds.

2.1.4.2.4.3 Normal Interrupt. After being acknowledged by the IOC, a requesting device may signal an interrupt over a common control line. In this case, the IOC obtains a termination word. It posts the I bit of this word and sets a bit in the program status register which is specified by the NPL field of the termination word.

Interrupts received from peripheral devices may be "locked out" at the programmer's option. A special control flip-flop called the interrupt lockout is provided. If this flip-flop is a one, all I/O requests for an interrupt are inhibited by the IOC.

This flip-flop is set by the execution of any test bit instruction (F = 64 to 67) whose E bit is set to a one. This flip-flop is reset by the execution of any set or reset bit instruction (F = 60 - 63) or device command (F = 74) instruction whose E bit is set to a one.

2.1.4.2.4.4 Error Detection. A control line called "device error" is provided for a peripheral device to signal the IOC that it detected an error during normal communication. Should the IOC detect this signal, it will terminate the communication and transmit an "end of transmission" signal to the device. The IOC will obtain the corresponding termination word and set its status bit E to a one, and post the bit of the program status register that is specified by the EPL field of the termination word to a one.

2.1.4.2.4.5 Program Load (Bootstrap). The processor must be in a stopped (reset) configuration prior to this type of operation. A special control line called "program load" will cause the processor to accept data from one of the system's devices. This is the only operation that can occur until the input is complete. The processor then starts to execute the program just received in the program load operation.

The initial program load operation takes place in two steps. The first step is the input of the initial key word from the transmitting device. The second step is the input of the data under control of the initial key word.

The key word is received as four characters. If the transmitting device is a word-oriented device it will transmit four words, but only the eight most significant bits of these words are used for the initial key word input. The first four transmitted characters (or words) form a key word with a normal format.

This key word specifies the length of the block of data to be input and the starting address in memory for storage of this data. The key word's mode field also specifies the input mode (character or full word) for the remaining data. The IOC services the device that is associated with the program load switch only. No other processor operation occurs until the block length field of the key word reaches zero.

When the full block of data is input, the processor automatically assumes program level zero and executes the instruction in the memory address that was initially specified by the key word that controlled the program load. This is the first full word that was input in this operation.

2.1.4.3 Input/Output Interface

All communication between system peripheral devices and the Input/Output Control Unit (IOC) of the L-3050 takes place over 64 interconnecting lines. These lines separate into three groups. Group I consists of 36 lines that are bidirectional. That is, both the IOC and peripheral device buffer units use these lines for the transmission of information. Group II consists of 16 single direction control lines that are used by the IOC for transmission to the peripheral devices. Eight of the lines of Group II are unique to each of eight I/O stations. These lines are called "enable" lines. The remaining eight control lines of Group II are shared by all peripheral buffers. Group III consists of 12 single direction lines that are used by the peripheral device buffers for transmission to the IOC. Four of these lines are shared by all peripheral devices and one of eight are unique to each of eight I/O stations. These eight unique lines are called the "request" lines.

The IOC uses the enable lines to select the desired I/O station, and the peripheral units use the request lines to identify the I/O station to which they are connected.

Each of the lines in the I/O interface transmits signals as described in the following subsections.

2.1.4.3.1 Bidirectional Lines

Data Signals (33) – These signals transfer parallel data, plus odd parity, between the IOC and a peripheral unit.

> NOTE: Data transmission is either in word format or character format. Word transmission may be any length up to 32 bits plus parity; whereas, character transmission may be a maximum of eight bits plus parity. If character format is used, each character is transmitted on the eight most significant lines (left most).

Address Signals (3) – These signals select one of eight substations connected to a particular station. These signals, when required, are transmitted to a station during execution of an I/O instruction, or are received from a station in response to an enable signal.

2.1.4.3.2 From IOC Lines

Enable Signals (8) – These signals, one to a station, acknowledge the receipt of a request from that station.

NOTE: If more than one request is simultaneously received by the IOC the station with the highest priority is acknowledged first.

Sync Signal — This signal is transmitted to a peripheral unit as a request for data.

DEC Control — This control signal is transmitted to the peripheral unit when command data is available to that unit during execution of a device command (DEC) instruction.

OFR Control Signal — This control signal is transmitted to the peripheral unit when data is available during execution of an output from register (OFR) instruction.

ITR Control Signal — This signal is transmitted to the peripheral unit as a request for data during execution of an ITR instruction.

Strobe Signal — This signal is transmitted to a peripheral unit when data ia available during an output.

Mode Signal — This signal is transmitted to the peripheral unit to specify that the communication is due to the execution of an I/O instruction rather than an automatic operation. The activation of this line gives the IOC priority over the peripheral unit for use of the address lines.

End of Transmission Signal — This signal is transmitted to a peripheral unit when a complete block of data has been transferred or upon completion of an interrupt sequence.

Reset Signal — This signal is transmitted to all peripheral units to indicate that the IOC is not prepared to enter into any I/O communications.

2.1.4.3.3 To IOC Lines

Request Signals (3) — These signals, one from each station, are transmitted to the IOC from peripheral units that require servicing.

Ready Signal — This signal is transmitted to the IOC when a peripheral unit has received its acknowledge signal and is prepared to transmit address information (if required); and when a peripheral unit has received a sync signal and has data available.

Interrupt Signal — This signal is transmitted to the IOC as an interrupt signal.

Device Error Signal – This signal is transmitted to the IOC when a peripheral unit has its own error sensing circuits and wants to communicate occurrence of an error to the IOC.

Program Load Signal – This signal is transmitted to the IOC when a peripheral unit wants to initiate a forced memory load.

2.2 PHYSICAL DESCRIPTION OF LABORATORY L-3050 M UNIT

2.2.1 General

The proposed L-3050M laboratory model computer is comprised of highly serviceable, portable modular units. The basic units consist of a processor (see Figure 2-10) and an 8K memory (see Figure 2-11). Memory capacity may be increased incrementally by adding memory units to the system. The units are contained within weathertight aluminum transit cases enabling the units to be readily moved and easily set up for operation. To operate, the units can be located on any work surface, the transit case covers removed by actuating quick-release fasteners and the necessary cables installed to the connectors located on the front panel of the units. The computer is an integral part of the transit case, thereby not requiring case removal during the operational mode.

2.2.2 Processor and Memory Design

The processor and memory units are designed with ease of serviceability and fabrication economy as prime objectives. To service the units, quick-release fasteners secured to the front panel are actuated enabling the unit to be pulled outward on slide rails which are secured to the upper and lower inside surfaces of the transit case (see Figures 2-10 and 2-11). The unit is functional in this position since the external cabling is of sufficient length and is terminated to the front panel. The printed circuit cards are readily removable by actuating the card removal devices shown in Figure 2-12. The processor contains several shelves of cards. The outboard shelves are hinged to enable access to the inboard cards. The printed circuit cards engage with printed circuit card connectors which are secured to the back plane of the card rack. The design enables the utility of automatic wire wrap to interconnect the PC card connectors.

The L-3050M computer uses two basic printed circuit card sizes which are dimensionally 1.20 by 6.60 and 2.20 by 6.60 inches by 0.062 inches in thickness. The cards are fabricated of glass laminate with copper conductor laminate on both surfaces. Monolithic integrated circuit packs as well as discrete components are secured to one side of the PC card only, thereby enabling flow soldering technique to be used in lead termination. A typical PC card assembly is illustrated in Figure 2-12.

The cards are located in an in-line vertical position within the card racks enabling a forced convection method of cooling to be used. The airflow is provided by a fan located in each unit which exhausts the air through an aperture in the upper

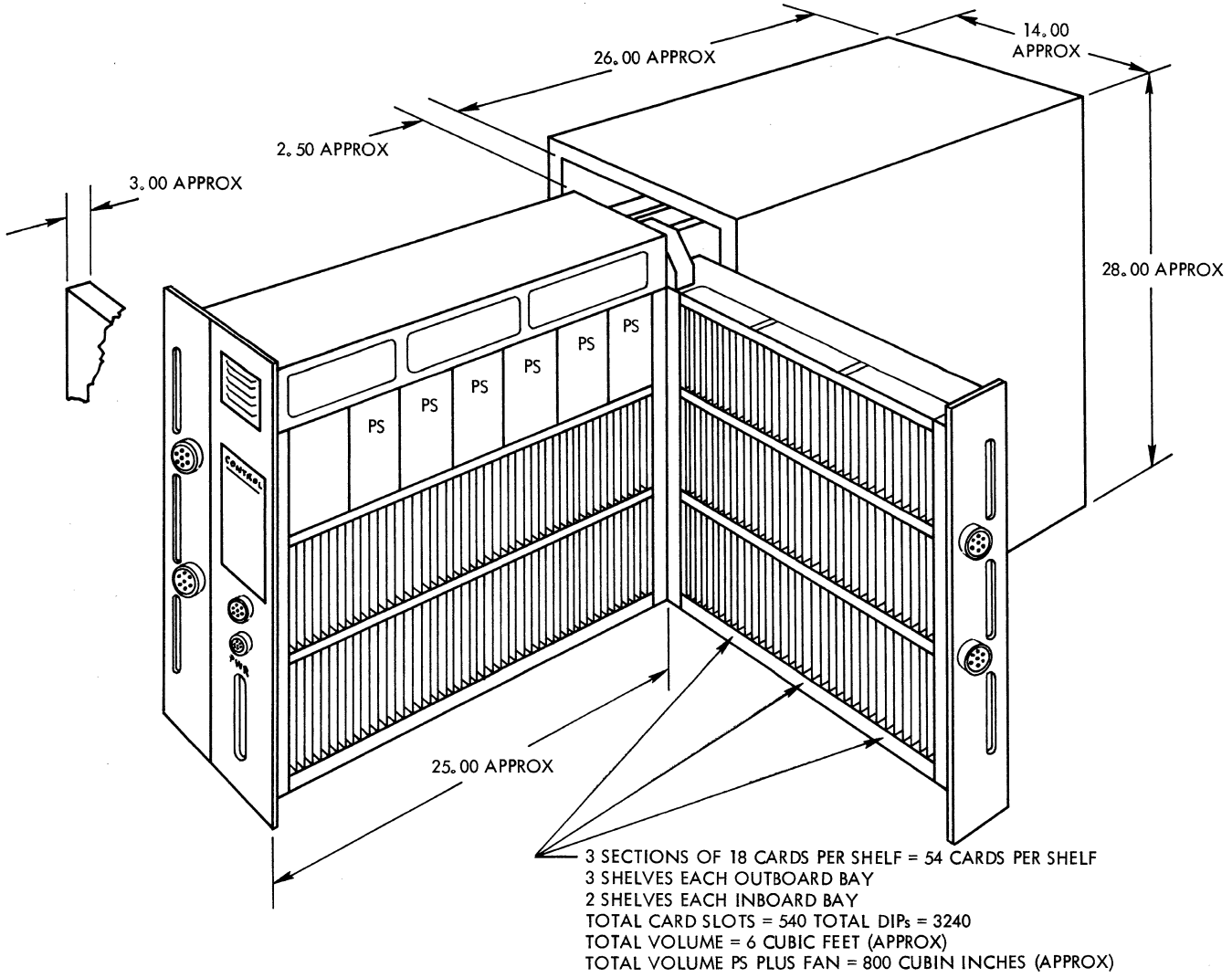


Figure 2-10. Processor Configuration

1771-13

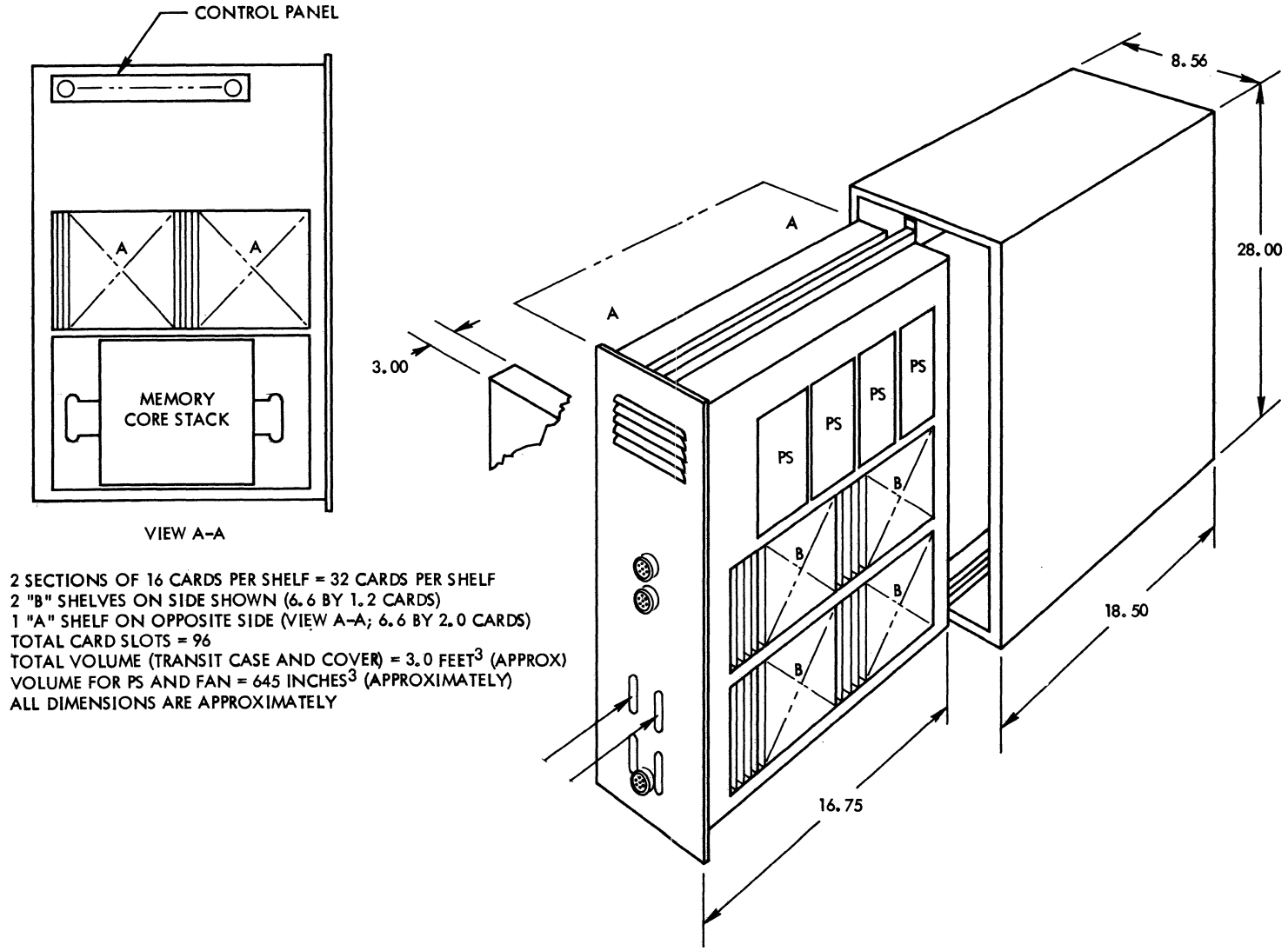


Figure 2-11. Memory Unit

1771-14

COMPONENT / CARD TYPE	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬
545210-100 CARD # 1	860003-70 QUAD-TWO INPUT	←			→	860003-70	SCD40D274M .27µf CAP.	SCD40D274M .27µf CAP.	M22684/01	←		→	M22684/01
545211-100 CARD # 2	TNG3341P TRANSITRON TRIPLE-THREE INPUT	←			→	TNG3341P TRANSITRON	↕	↕	↕				↕
545212-100 CARD # 3	860003-64 DUAL-FOUR INPUT	←			→	860003-64							
545213-100 CARD # 4	860003-6B SINGLE - B INPUT	←			→	860003-68							
545214-100 CARD # 5	860003-52 LAMP/LINE DRIVER	←			→	860003-52							
545215-100 CARD # 6	860003-53 LINE RECEIVER	←			→	860003-53							
545216-100 CARD # 7	SF-130-03 (SYL) DUAL FLIP/FLOP	←			→	SF-130-03 (SYL)	SCD40D274M .27µf CAP	SCD40D274M .27µf CAP.	M22684/01	←		→	M22684/01

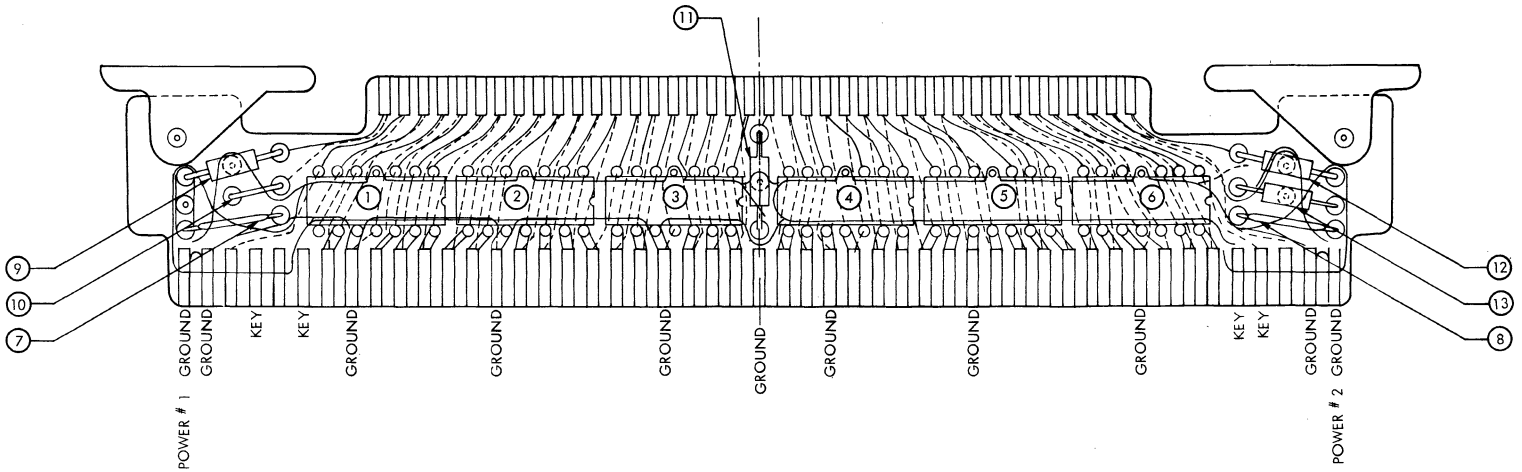


Figure 2-12. Logic Card Assembly Information

1771-15

portion of the panel. The air inlet and outlet openings in the panel are provided with RFI filters. Located in the upper portion of the units are plug-in modular power supplies.

2.3 PHYSICAL DESCRIPTION OF AIRBORNE L-3050 UNIT

2.3.1 General

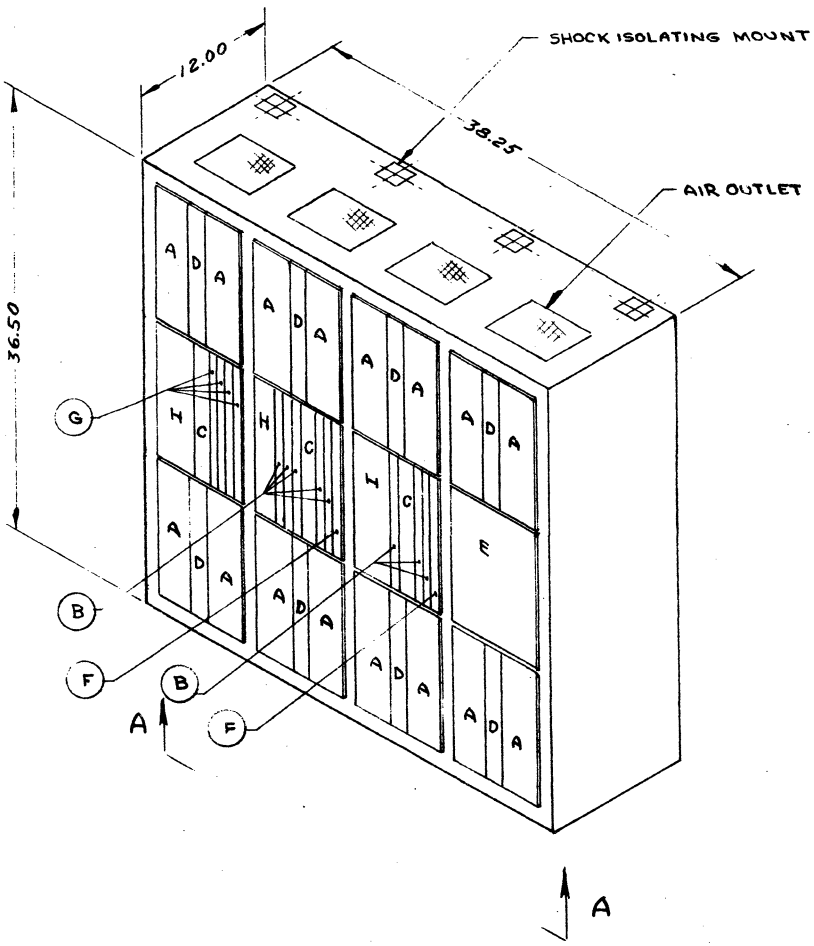
The L-3050 airborne computer system is modularly constructed to meet the requirements of systems ranging from a need for single processor — small memory to multiprocessor — large memory, or any combination thereof. For the VSX multiprocessor system, the form factor proposed is illustrated in Figure 2-13. The calculated weights and physical characteristics are shown in Table II-7.

This form factor is flexible and may be easily changed to fit any configuration of data processing required.

The computer is a fully microelectronic system, utilizing integrated circuits to the maximum extent possible. The design philosophy employs modular functional assemblies having positive lock-in and easy removal capability. The assemblies afford ready access for replacement, testing, and repair, when necessary, and provide excellent physical protection against environments. A proprietary component lead joining technique combines the controllability and general reliability levels usually associated with welding with the reversibility of soldering.

2.3.2 Computer Cabinet

The computer cabinet is fabricated of aluminum alloy and measures 12.00 inches deep, 38.25 inches wide, and 36.50 inches high. The cabinet design utilizes a three-dimensional front shear plate and a similar rear shear plate. These two major parts of the structure are riveted in position using extruded aluminum angles. The complete structure is then enclosed with a 0.062-inch thick aluminum sheet. Three-dimensional front and rear shear planes are made from one-inch thick aluminum plate. The plate design is based around automatic, tape-controlled milling machine fabrication techniques. This machining technique eliminates the cost of special tools and fixtures that would normally be required. With the two principle structural members fabricated in this manner, the assembly can be accomplished without special jigs and assembly fixtures. Notches are located and machined into the edges of the horizontal "TEE" sections of the two structural members to give fast and accurate locators for the module guide rails. The horizontal members are



L-3050 SYSTEM		
CODE	DESCRIPTION	NO. REQ'D
A	8K MEMORY DRAWER	16
B	SETS A/C DRAWERS 1,2,3,4, & 5	2
C	I/O & A/C POWER SUPPLY DRAWER	3
D	MEMORY POWER SUPPLY DRAWER	8
E	AC/DC CONVERTER DRAWER	1
F	I/O CONTROL DRAWER	2
G	I/O EXCHANGE DRAWER	4
H	SPARE	3

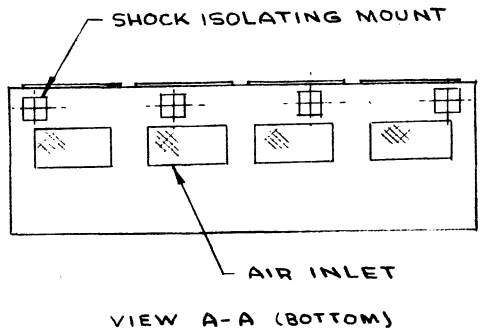


Figure 2-13. L-3050 Computer

1771-16

DRAWER TYPE	QUANTITY	WIDTH (INCHES)	HEIGHT (INCHES)	DEPTH (INCHES)	INDIVIDUAL WEIGHT (POUNDS)	TOTAL WEIGHT (POUNDS)
8K MEMORY	16	3.25	9.68	10.57	15.4	246.4
A/C	10(2 SETS)	0.75	9.68	9.67	4.4	44.0
I/O AND A/C PS	3	1.50	9.68	6.00	8.4	25.2
MEMORY PS	8	1.50	9.68	9.00	6.3	50.4
AC/DC CONVERTER	1	8.00	9.68	9.00	20.0	20.0
I/O CONTROL	2	0.75	9.68	9.67	4.4	8.8
I/O EXCHANGE	4	0.75	9.68	9.67	4.4	17.6
SPARE (BLANK DRAWER)	3	3.50	11.19	9.67	2.5	7.5
CABINET (INCLUDING HARNESS)	1	38.25	36.50	12.00	97.5	97.5
					L-3050 TOTAL WEIGHT	517.14

Table II-7. L-3050 Computer Physical Characteristics 1771-17

fabricated from aluminum extruded angles. These angles are cut to the required length and act as structural members accurately spacing the two shear planes. To complete the structural assembly, the outer aluminum skins are riveted in place.

The vertical air baffles that form four distinct air passages through the unit are bonded in place using an epoxy resin adhesive per MIL-A-8623A Type 1. The functional drawers (modules) are attached to the front shear plane with quick-operating fasteners. The rear shear plane supports the drawers by shear pins. This plane also contains floating electrical connectors that engage with mating drawer connectors. The alignment of the drawers during drawer insertion is facilitated by upper and lower drawer guide rails included in the cabinet design. A positive metal-to-metal stop prevents damage to the mated connectors from overengagement. In addition, the area and pressure characteristics of the metal-to-metal contact provides for grounding and bonding the module to the enclosure.

The computer cabinet is externally mounted on vibration isolators to ensure the assembly will meet the shock and vibration tests of MIL-E-5400 (Curve IV). The shock isolators are located along the lower front edge and the upper rear surface of the cabinet (see Figure 2-13).

2.3.3 Functional Drawers

The computer is constructed in a modular fashion and is comprised of a series of plug-in module "drawers." These drawers are identical in height and the length is controlled to a standard dimension. The width varies according to packaging dictates. Within the drawer configuration are packaged multilaminate boards which may be comprised of up to 15 layers each. Fastened to these multilaminate boards are monolithic integrated circuits. These elements are assembled to the outer surfaces of the multilaminate boards which are attached back to back with an aluminum web sandwiched between. The web serves as a structural and conductive heat transfer member. To minimize temperature gradients, the multilaminate boards are bonded to the web with a silver-filled epoxy. Figure 2-14 illustrates two typical drawers with their covers removed. The screws which retain the covers also provide interface pressure to minimize temperature gradients between the web and covers. These screws fasten into locking inserts thereby minimizing loose hardware.

2.3.4 The Multilaminate Board

A unique multilayer board process interconnects the microelectronic components. It is highly compatible as an interconnection method for "flat pack" types of microelectronic components and circuits. This compatibility derives from several characteristics of these boards. One basic characteristic is the nature of the layer-to-layer interconnection technique employed. Instead of the more conventional plated hole which pierces the board completely, even when only serving to interconnect a few layers, a solid plated post is employed between levels for interlayer communication. Unlike the plated holes, these posts are built up a layer at a time and thus can stop internally, if appropriate, without going all the way through the board. This allows for increased communication ability because the "picket fence" of holes on every layer that would have existed if the plated hole technique were employed is replaced by posts which terminate at various levels, thus providing for increased circuit line routing capability. The net effect is a reduction in the number of layers required to perform a given amount of communication.

Another area of compatibility afforded by this plated post technique is the superior thermal path provided. "Flat packs" have a relatively large surface from which to remove heat considering their overall small volume. The heat is collected in this instance by a surface thermal pad of copper under each "flat pack" and conducted directly through the board by two short, solid copper posts. These posts

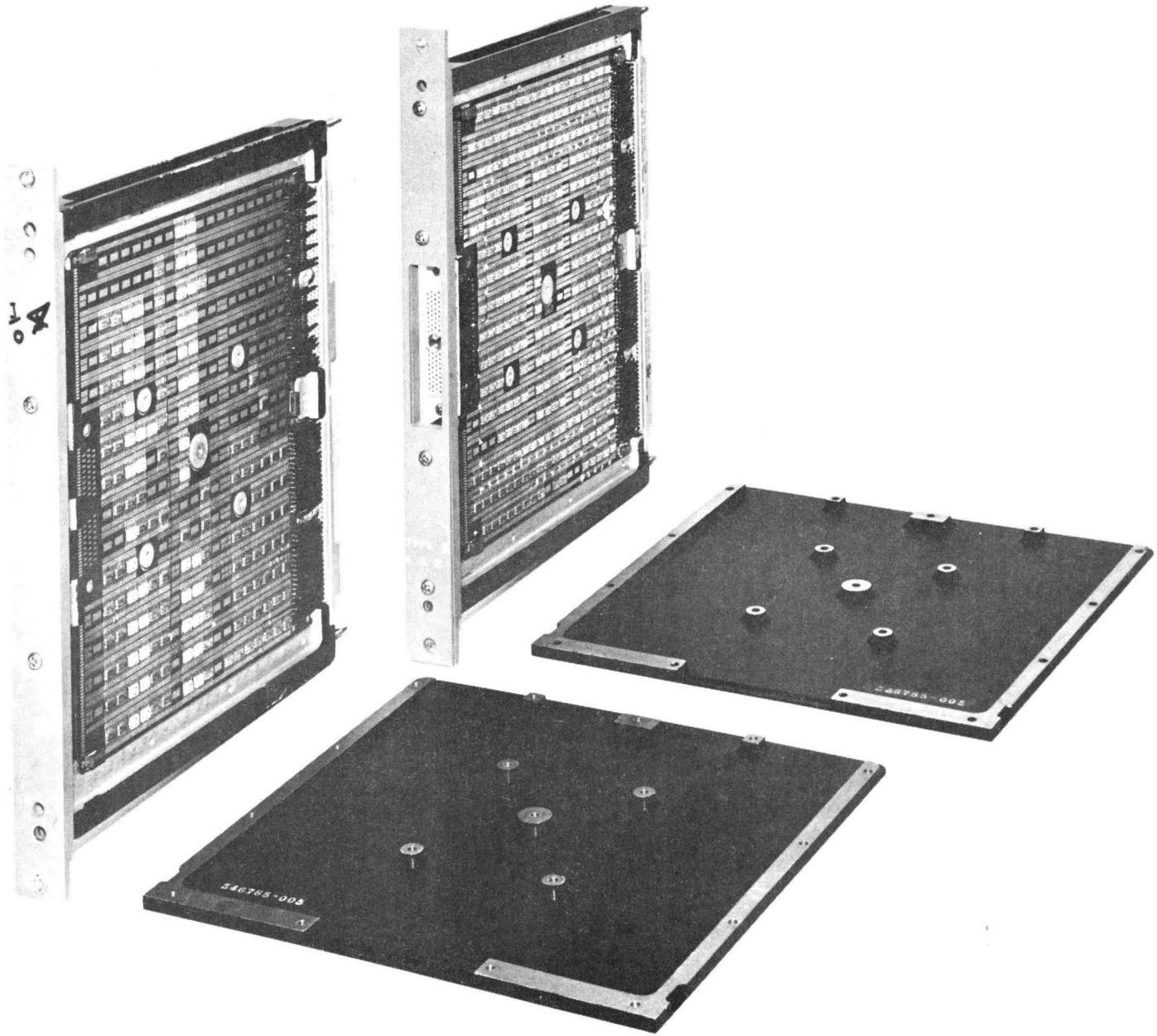


Figure 2-14. Thermal Conductive Path in I/O and A & C Drawers U-10640-24

connect in turn to a copper thermal plane from which the heat is readily removed. A thermally conductive adhesive facilitates the transfer of heat from the flat pack bottom to the thermal pad.

Still another compatibility factor is in the reliability area. The increased reliability afforded by the use of microelectronic integrated circuits should not be dissipated by an interconnection technique of relatively inferior reliability. The solid copper posts employed by the plated post type of laminate is a more rugged means of layer-to-layer interconnection than the shell of copper existing in a plated hole. Also, the area contacted in building up a typical interconnecting post of 0.030-inch diameter is several times greater than the area existing on the exposed ring of copper to which a plated hole connects in a plated hole laminate. The increased reliability implied by this fact appears to be compatible with the higher reliability associated with integrated circuits.

2.3.5 Lead Joining

An extremely important aspect of the employed packaging that enhances both reliability and maintainability is the technique used in making the electromechanical joints between lead wires and the multilayer board circuitry. The two most commonly used methods currently employed in the industry to accomplish this task are soldering and parallel gap resistance welding. Soldering may be accomplished in two basic ways but each of these presents fundamental problems. The method requiring the minimum of equipment, hand soldering, presents the problems of flux removal and possible thermal damage to board, components, or both. If the newer reflow system employing resistance heating is used, the solder-precoated board surfaces are subject to potential storage corrosion because they are not corrosion proof. However, compared to the other commonly employed technique, welding, soldering at least is a reversible process. With welding, component removal becomes a problem.

The method employed by Litton to construct the computer combines the advantages of the foregoing methods while eliminating the major disadvantages. The Litton joining method employs a proprietary surface material which is deposited on all of the surface joining pads of the interconnect multilayer boards. The material has the property of being highly diffusible at certain temperatures which can be readily reached by employing parallel gap resistance welding equipment. These temperatures, while sufficiently high to create a strong diffusion bond between the lead and the pad surface, do not melt either base material. The resultant joints are therefore

provided with a high shear strength because of the relatively large areas involved, but have a low peel strength because of the lack of a weld nugget. The shear strengths obtained in this process are typically equal to or greater than the yield tensile strength of the lead material, while the peel strengths are typically an order of magnitude less. This allows for easy component removal and repeatable replacement. Extensive testing of this process has yielded excellent results for strength and repeatability. Also, it has been demonstrated that rejoining can be accomplished readily many times with the residual material. Six to eight rejoins have been accomplished repeatedly.

Employing the system described, it is possible to remove flat pack integrated circuits by peeling the individual leads from their respective bonding pads without damage to the pads or board. It is then quite simple to rejoin the leads of a new component to the same areas without causing any noticeable degradation of joint strength.

2.3.6 Cooling

Thermal management for the computer is accomplished through the use of controlled conductive heat transfer paths, use of maximum dissipative heat transfer areas where possible, and a series forced convection cooling scheme which allows high unit temperature differences and high subsystem exhaust temperatures. The externally supplied cooling airflow enters the computer through four rectangular holes in the enclosure base (see Figure 2-13, View A-A) and is forced upward and between the module drawers and exhausted through the four rectangular holes in the enclosure top. EMI filters are provided at inlet and outlet apertures. Air ducts and/or baffles are strategically located throughout the enclosure to cool each drawer. Parallel cooling paths are utilized as much as possible to keep the rise in the cooling air temperature and the resulting component temperatures at a minimum.

Modules are constructed with multilaminate boards as the primary electronic interconnecting media containing an integrated, independent, heat transfer system. This heat transfer system takes the form of plated-up solid electrolytic copper posts integrally fastened to the copper surfaces of the multilaminate.

Heat derived from the element fastened to the multilaminate surface passes through an adhesive to a copper pad where it is funneled to the posts. The number of posts per element is dependent on its dissipative characteristics. In no case is there less than two posts per element. The heat is carried down parallel paths to the copper surface on the opposite side of the multilaminate board. These parallel paths are composed of the epoxy portion surrounding the post, the area of which equals the element area minus post areas, and the posts themselves. Once on a

multilaminate far side, it is distributed through the copper surface to approximately a uniform density through the silver-filled epoxy adhesive to the center web or cover (in the case of the memory hybrid circuits). Heat is removed from the web via a number of buses, strategically placed to optimize thermal distributions, and module edges to the cover surfaces. Once on the cover, it is removed by forced convection. Rubber seals are vulcanized to the drawer panel edges thereby preventing a loss of airflow at the panel interfaces.

2.4 CONTROL CONSOLE

The L-3050 Control Console is shown in Figure 2-15 and switch descriptions are presented in the following subsections.

2.4.1 Power and Start Mode Switches (Located Lower Left-Hand Corner of Console Keyboard)

These two switches work together to determine hardware procedure when the hardware is turned on.

Start Mode is "AUTO" – Turn Power "ON"

(1) All control logic is cleared (master reset).

(2) Program level register is set to 77_8.

CAUTION: The program activity registers are not modified. A store cycle in Locations 1606 or 1607 will initiate a program activity register search. If Level 77_8 status and enable bits are not set, the program level will be changed.

(3) Location register is set to 1610_8.

(4) Program begins execution at Location 1610_8.

CAUTION: Levels 74_8 through 77_8 do not allow servicing of input/output requests.

Start Mode is "MANUAL" – Turn Power "ON"

(1) All control logic is cleared (master reset).

(2) Program level register is set to 77_8.

CAUTION: The program activity registers are not modified.

(3) The computer will be in "stopped" mode.

Turn Power "OFF" or if Power Fails

Stopped Mode:

Power goes down.

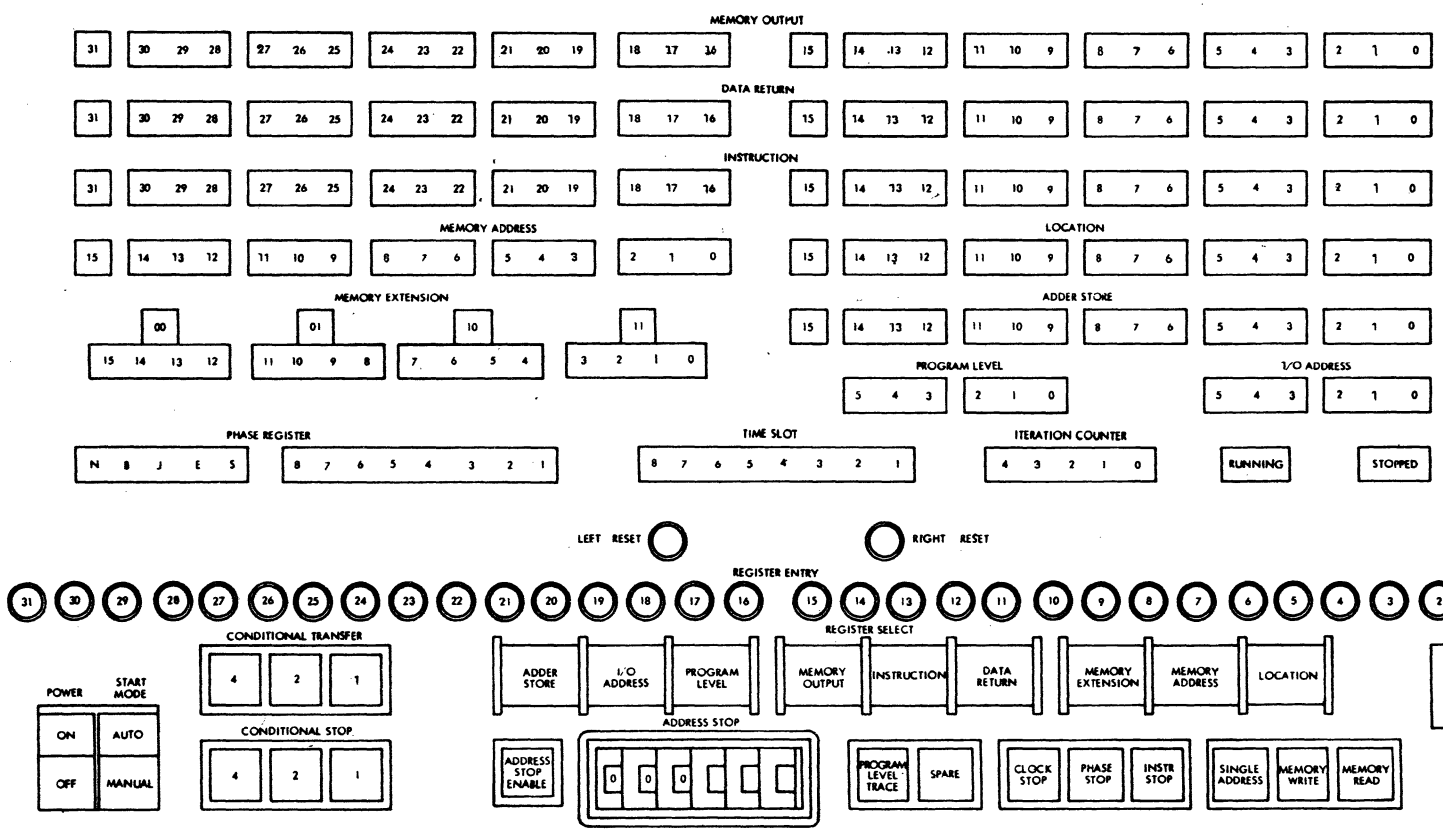


Figure 2-15. Control Console

Running Mode:

(1) The current instruction in process will be completed.

(2) Input/output continuous transmission will be halted if in process. The "F" bit (Bit 31 of terminate word) will not be set to 1. The status bit specified by the terminate word will not be set to 1.

(3) The computer will be changed to program level 77_8.

CAUTION: The program activity registers are not modified. A store cycle in Location 1606 or 1607 will initiate a program activity register search. If Level 77_8 status and enable bits are not set, the program level will be changed.

The power-off routine must execute a halt instruction. This causes the memory to lock up so that it will not be destroyed.

Level 77_8 will not allow the computer to service any input/output request.

2.4.2 Master Reset (Located Middle of Right Side of Console Keyboard)

(1) All control logic is cleared.

(2) The following registers are set to zero:

Memory output

Data return

Instruction

Memory address

Location

Adder store

Input/output address

(3) Program level register will be set to 77_8.

(4) Set MEMORY EXTENSION to 0, 1, 2, 3.

CAUTION: The master reset switch is effective when the computer is in the running mode.

2.4.3 Start (Located Lower Right Corner of Console)

The program begins operating.

2.4.4 Register Entry (Second Row of Buttons)

These buttons are used to enter one bit(s) (light on) into the register selected by the register select switches.

Registers that can be selected:

Memory output

Data return

Instruction

Memory address

Location

Adder store

Input/output address

Memory extension

CAUTION: It is possible to select more than one register at a time. If multiple registers are selected, the "register entry" switches will enter ones into the selected position(s) of every register.

Note that the register display designates the "register entry" button number for every bit. Note, too, that the "memory address" register specifies Bits 0-15, not 16-31.

2.4.5 Register Entry Reset (Two Top Buttons)

The registers affected by these buttons are selected by the register select switches:

Right button zeros positions labeled 0-15

Left button zeros positions labeled 16-31

2.4.6 Register Select (Center of Console)

These switches select the register(s) that are to be modified by the "register entry" and "register entry reset" buttons. Once a register is selected, it cannot receive inputs from any source except the "register entry" and "register entry reset" buttons.

Registers that can be selected:

Memory output

Data return

Instruction

Memory address

Location

Adder store

Input/output address

Program level

Memory extension

CAUTION: It is possible to select more than one register at a time. All selected registers will be modified simultaneously by actions of the "register entry" or "register entry reset" button.

2.4.7 Single Address (Bottom Row, 4th Switch from Right)

Single Address Lighted

The address for a memory read/write operation is taken from the memory address register. The contents of the memory address register will not be changed by the execution of the read/write cycle. This switch should never be actuated while the computer is running, since it may cause program errors.

Single Address Unlighted

The address for a memory read/write operation is taken from the location register. Execution of a read/write cycle will cause the contents of the location register to be incremented by +2.

2.4.8 Memory Read (Bottom Row, 2nd Switch from Right)

Option One

(1) Memory read switch lighted

(2) Single address switch lighted

(3) Depress start switch

The contents of the location specified by the memory address register will be displayed in the memory output register. The contents of the memory address register will not be changed.

Option Two

(1) Memory read switch lighted

(2) Single address switch unlighted

(3) Depress start switch

The contents of the location specified by the location register will be displayed in the memory output register. The contents of the location register will be incremented by +2.

2.4.9 Memory Write (Bottom Row, 3rd Switch from Right)

Option One

(1) Memory write switch lighted

(2) Single address switch lighted

(3) Depress start switch

The contents of the data return register will be stored in the location specified by the memory address register. The contents of the memory address register will not be changed.

Option Two

(1) Memory write switch lighted

(2) Single address switch unlighted

(3) Depress start switch

The contents of the data return register will be stored in the location specified by the location register. The contents of the location register will be incremented by +2.

2.4.10 Instr Stop (Bottom Row, 5th Switch from Right)

This switch halts the computer at completion of instruction currently being executed.

2.4.11 Conditional Transfer (1, 2, 4) (Left End of Middle Row)

These three switches are tested by the Transfer on Console Transfer Switch (XSW) instruction. If the conditional transfer switch tested is lighted the XSW instruction will transfer.

2.4.12 Conditional Stop (1, 2, 4) (Left End of Bottom Row)

These three switches are tested by the Halt (HLT) instruction. If the conditional stop switch tested is lighted, the HLT instruction will halt.

2.4.13 Address Stop (Counter) (Center of Bottom Row)

When the address stop enable switch is lighted, the program will stop at the end of the current instruction when the designated address is accessed. The address may be odd or even; in either case it must be exactly the same as the address accessed. An even double access that includes the odd location specified by the address stop counter will not cause the computer to stop.

2.4.14 Address Stop Enable (Bottom Row, Left of Center)

"ON" Lighted

The program will stop at the end of the current instruction when the address designated by the address stop counter is accessed. The specified address may be the location of an instruction or data referred to by an instruction.

2.4.15 Clock Stop – Phase Stop

These two switches are used by maintenance only.

2.4.16 Program Level Trace (Bottom Row, Right of Center)

Actuation of this switch causes program level 75_8 to be interleaved between each normal program level change.

SECTION III

THE L-3050 INPUT/OUTPUT SYSTEM AS APPLIED TO VSX

3.1 GENERAL

The high speed and flexibility of the L-3050 Input/Output system enables the L-3050 to handle the severe input/output requirements of the VSX system using either two-port or four-port memories. This built-in flexibility allows a choice to be made for the production system based on cost-effectiveness considerations which can be previously proven in the laboratory and flying test systems.

3.2 ALTERNATE INPUT/OUTPUT SYSTEM IMPLEMENTATIONS

The two alternate input/output schemes, either of which may be implemented in the VSX computers, are discussed in the following subsections.

3.2.1 Two-Port Memory System

The two-port memory system requires that each data transfer be interleaved with the execution of the computer program instructions. This slows down the processing of each computer by an amount necessary to process the input/output. An analysis of the percentage of computer time taken by the input/output rates (see Tables III-1 and III-2) for the tactical and sensor processors shows that 26.87 percent of the tactical processor's and 39.58 percent of the sensor processor's time would be taken by input/output if the two-port memory were used and if the severe input/output rates assumed were actually realized.

As shown in Tables III-1 and III-2, the assumptions included the transfer of a total of 32,768 words per second to and from the drum, the display of from 2,000 to 4,000 characters on each of the three displays, and the continual transfer of data to the tape, while at the same time meeting all the other input/output requirements of the system.

3.2.2 Four-Port Memory System

Because of the increase in number of components, the four-port memory is more expensive and less reliable than the two-port. However, the four-port memory has the advantage of completely bypassing the processor, going directly to memory from the input/output device. Thus, no computer time is used by the input/output function.

CHANNEL NUMBER	INPUTS/SECOND	OUTPUTS/SECOND	COMPUTER TIME (MICROSECONDS)	COMPUTER TIME (PERCENT)
15	75	75	600	0.060
14	—	—	—	—
13	5*	5*	40	0.004
12	320	30	1,400	0.140
11	8,192**	8,192**	65,536	6.553
10	—	25,000	100,000	10.000
9	—	25,000	100,000	10.000
8	—	—	—	—
7	—	—	—	—
6	—	—	—	—
5	6	120	504	0.050
4	8.3	125	533.20	0.053
3	5*	5*	40	0.004
2	16.67	—	66.68	0.007
1	—	—	—	—
0	—	—	—	—
TOTALS	8,627.97	58,552	268,719.88	26.87

*ASSUME 5 TRANSFERS/SECOND
**ASSUME 8192 WORDS TRANSFERRED IN AND 8192 WORDS TRANSFERRED OUT PER SECOND

Table III-1. Tactical Processor (Assuming Two-Port Memory) 1771-300

CHANNEL NUMBER	INPUTS/SECOND	OUTPUTS/SECOND	COMPUTER TIME (MICROSECONDS)	COMPUTER TIME (PERCENT)
15	—	2,560	10,240	1.024
14	—	6,000	24,000	2.400
13	—	—	—	—
12	160	110	1,080	0.108
11	8,192***	8,192***	65,536	6.553
10	14,286*	25,000	157,144	15.714
9	—	—	—	—
8	14,286*	—	57,144	5.714
7	—	—	—	—
6	—	—	—	—
5	6	120	504	0.054
4	—	—	—	—
3	5**	5**	40	0.004
2	—	—	—	—
1	5**	5**	40	0.004
0	20,000	5**	80,020	8.002
TOTALS	56,940	42,097	395,748	39.58

*2 16-BIT HALF WORDS ARE TRANSFERRED IN PARALLEL
**ASSUME 5 TRANSFERS/SECOND
***ASSUME 8192 WORDS IN AND 8192 WORDS OUT PER SECOND

Table III-2. Sensor Processor (Assuming Two-Port Memory) 1771-301

3.3 SUMMARY

The entire complement of sensors, displays, storage equipment, etc., is easily handled by the 64 channels available to each of the L-3050 processors. Should either of the processors fail, all input/output devices could be switched to the remaining processor which could then continue to operate in a degraded mode. If the four-port memory were used, all input/output would always bypass the processor and go directly to memory. If the two-port memories are used, failure of one processor would free one of the ports so that the input/output control of the other processor could be switched to the available port with the effect that the input/output transfers would thus be taken completely off-line. This would greatly increase the capability of the degraded mode system.

A determination as to whether the two- or four-port memory will be required could only be made in conjunction with an analysis of the total data processing task. With the L-3050 organization, this processing load could be verified with the laboratory and initial flying model so that the correct choice could be made for the production units without any effect upon programming or input/output interfaces.

SECTION IV

PROGRAMMING CENTER REQUIREMENTS FOR THE VSX L-3050

4.1 GENERAL

Program checkout on most military computers is simplified by the use of high-speed commercial peripheral equipment in conjunction with the military computer. One such programming center is already in operation with the Litton L-304 on the E2A retrofit program, and a second one is being installed for the Canadian Navy as part of the CCS 280 program. It is the latter system which is recommended for VSX.

4.2 PERIPHERAL EQUIPMENT

Program development and checkout for systems involving general-purpose military computers involve the use of assemblers, compilers, operating systems, debugging aids and other standard program tools used in the commercial computer world. To facilitate this type of programming operation commercial peripheral devices are often used in conjunction with the military computer. This approach has already been taken with the Litton L-304 computer in combination with IBM peripherals in establishing its E2A programming center. Litton is currently implementing a second L-304 programming center for the Canadian Navy using UNIVAC peripheral equipment.

The commercial IBM equipment consists of a card reader and punch, two magnetic tape units and a 600 line per minute printer. The UNIVAC equipment consists of a 1005-3 card reader-punch-printer, two magnetic tape units and a disk file. It is the inclusion of the disk file in the CCS 280 programming center which has determined this to be the more advantageous complement of equipment for VSX.

Because the L-304 and L-3050 input/output systems are logically and electrically compatible, the buffering and interface units developed for the L-304 will have direct application to the L-3050. Programming of input and output functions on the L-304 and L-3050 are also directly compatible so that the programs developed for the L-304 programming centers will have direct application to the VSX L-3050 programming center.

CCS 280 PROGRAMMING CENTER
UNIVAC 1005-3-04 WITH CARD READER AND INTEGRATED PRINTER 2010-31
CARD IMAGE CAPABILITY
CARD PUNCH 80 COLUMNS 2009-00
MAGNETIC TAPE UNIT AND CONTROL 0854-04
MAGNETIC TAPE UNIT 0858-01
DISK FILE (1 MILLION CHARACTERS EACH)
MASTER 8400-00
SLAVE F0783-00
ADAPTER FOR COMPUTER E0635-00
DISK-TAPE ADAPTER
E2A RETROFIT PROGRAMMING CENTER
IBM 2540 CARD READER/PUNCH
IBM 1403 HIGH-SPEED PRINTER
IBM 2821 CONTROL UNIT
IBM 2404 MAGNETIC TAPE AND CONTROL
IBM 2401 MAGNETIC TAPE UNIT

Table IV-1. List of Commercial Peripheral Equipments 1771-400

Table IV-1 shows the list of commerical equipments currently being implemented with the L-304 on the CCS 280 and E2A programs. Either sets of equipment tabulated in Table IV-1 could be made available for the L-3050 programming center.

SECTION V

EVOLUTIONARY DELIVERY SCHEDULE FOR LITTON L-304/L-3050 LINE OF MICROELECTRONIC COMPUTERS

5.1 INTRODUCTION

The L-3050 Computer that Litton Data Systems Division is proposing for the VSX Program is an advanced version of the microelectronic L-304 Computer which is currently in production for the Navy's E2A Retrofit Program. The L-304 is made up of modular plug-in units. These use multilaminate boards for circuit interconnection with each laminate capable of interconnecting up to 300 microelectronic integrated circuits. The laminates measure 7.8 by 9.2 inches and are approximately 0.7 inches thick.

Litton is now in the process of developing printed circuit card versions of both the L-304 and the L-3050 Computers for use in shipboard and land environments. The printed circuit cards will contain six integrated circuit modules per card and will measure 1.2 inches wide and 6 inches long. The printed circuit card versions of the computers will be designated as the L-304M and the L-3050M.

The L-304/L-3050 Computer evolutionary schedule in Figure 5-1 shows that both the laboratory version (L-3050M) and the airborne version (L-3050) for VSX will have been proven equipments before implementation into the VSX System.

5.2 DELIVERY SCHEDULE DEVELOPMENT

The following discussion will serve to define the evolutionary processes of the L-304, L-304M, L-3050M and the L-3050 (see Figure 5-1). The process is now in the second stage of development.

Item 1: L-304

The Airborne L-304 is now in production. It has been completely checked out and documented.

Item 2: L-304M

The L-304M (the shipboard and land-based version of the L-304) is scheduled for checkout in April, 1967. The L-304M will use the proven logic of the L-304. Therefore, only those tasks shown for Item 2 will be required to be accomplished for this computer, and they are well on their way to completion as of this date.

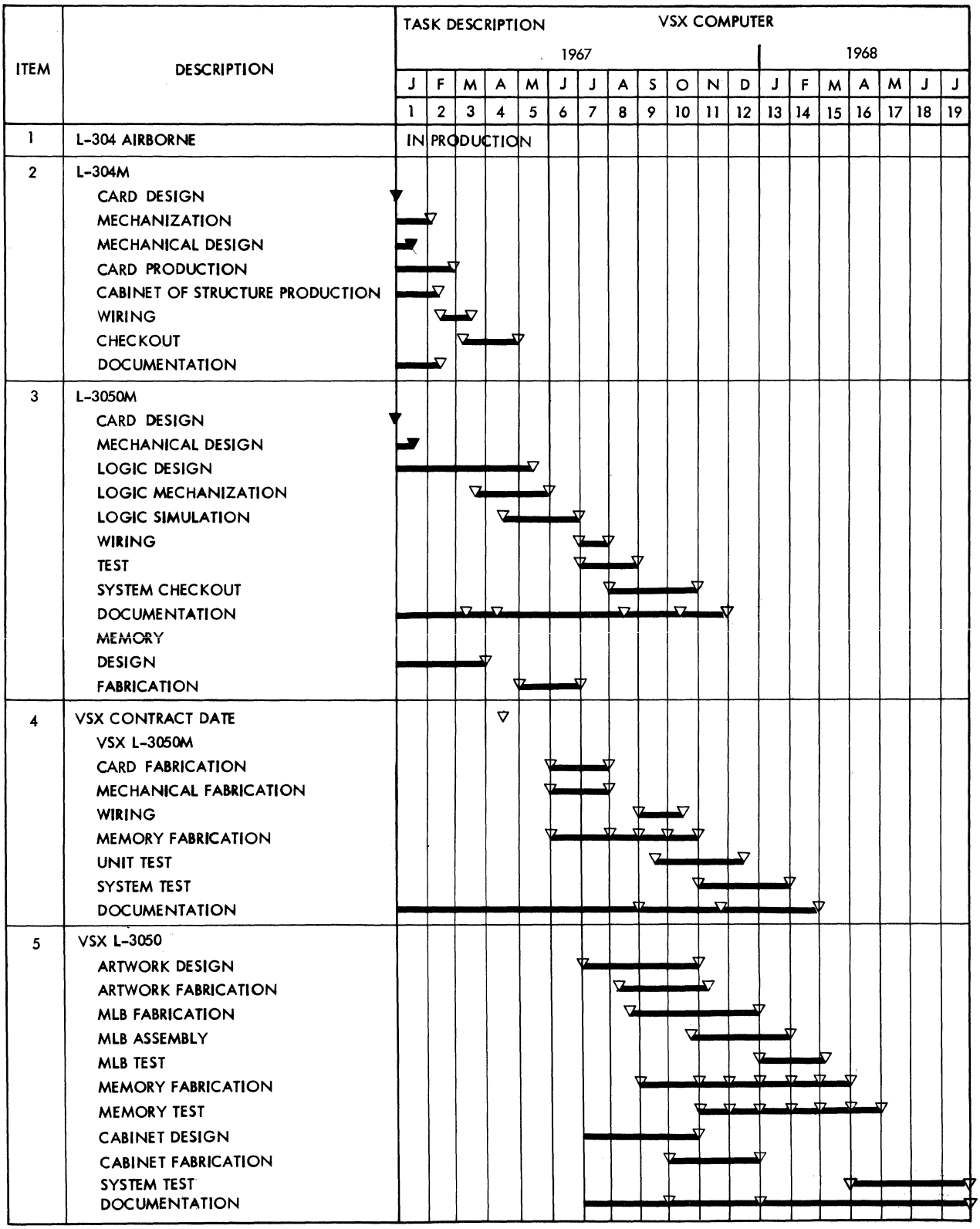


Figure 5-1. Evolutionary Delivery Schedule for Litton L-304/L-3050 Microelectronic Computers 1771-500

Item 3: L-3050M

The L-3050M development is being carried out concurrently with the development of the L-304M (Item 2). The L-3050M is a more powerful, advanced version of the L-304M. Therefore, some logic design is required for the L-3050M to evolve from the L-304M. However, the basic L-304M design will be retained and most of the redesign will consist of implementing the additional capability. The printed circuit card design and the mechanical design of the L-3050M will be identical to the L-304M. The L-3050M Computer is scheduled for completion in October 1967.

Item 4: VSX, L-3050M Laboratory Version

The computer envisioned as the VSX laboratory unit will be the L-3050M. The manufacturing schedule is shown under Item 4. It may be noted from a comparison between the L-3050M development (Item 3) and the VSX proposed L-3050M (Item 4) that if the date of contract for the VSX laboratory unit becomes a reality by April 15, 1967, the design of the L-3050M will be almost complete. Under these conditions, the VSX unit can be delivered in February 1968.

Item 5: VSX L-3050 Airborne Version

The airborne version of the L-3050 will take advantage of the modular techniques for mechanical design now employed in the production of the Airborne L-304. In fact, no basic construction design of the individual modules will be required. The mechanical assemblies as shown in Subsection 2.2 of this proposal are identical to those currently in production.

The logic design will be identical to that of the L-3050M Program. The difference will be a transition from the printed circuit card design to the multilaminate board design now used on the L-304.

New tasks required include design of art work and fabrication of films necessary to produce the multilayered boards. The boards themselves will be produced from those films in a multimillion dollar production facility specifically designed to perform this function. A detailed description of this microelectronic facility is included in Appendix A.

APPENDIX A

FACILITY CAPABILITY

A-1 INTRODUCTION

Litton Systems Incorporated operates approximately 150 plants throughout the world, and procures or develops facilities to maximize each division's ability to achieve contractual objectives. Work under the proposed program will be performed at the Van Nuys, California, and Salt Lake City, Utah, plants of the Data Systems Division (DSD).

A-2 ELECTRONICS DESIGN AND MANUFACTURING FACILITIES

Facilities at Van Nuys are housed in a group of buildings with over 400,000 square feet of floor space. (See Figures A-1 through A-5.) Buildings and basic equipment valued at more than $2.5 million are company-owned or leased. The facilities include engineering, laboratory, clean-room, environmental-simulation, computer, machine shop, sheet metal shop, electrical assembly, and administrative office areas. Electronics equipment and machinery has been acquired during the last five years to support the Division's development and production activities. Government-owned machinery and test equipment are being used only where specifically assigned to contracts. Work in progress is in the areas of computers, data processing equipment, command and control equipment, tactical displays, and recording and reproducing devices. Research and development activities have concentrated on high-reliability microelectronic equipment.

The Salt Lake City plant (Figures A-6 and A-7) is used principally for the fabrication of circuit cards and other subassemblies. The plant is modern and spacious, and equipment includes such items as a 24,000-point wire analyzer for harness and electronics-drawer testing.

A-3 MICROELECTRONIC RESEARCH AND DEVELOPMENT FACILITIES

Recognizing the high-reliability potential of integrated circuits, a microelectronics development program was inaugurated by DSD at a very early stage in the growth of integrated-circuit technology. The microelectronics program utilizes integrated circuits, thin-film techniques, and multilayer boards in equipment construction to the fullest degree permitted by the state of the art. Activities have involved both research and volume production.

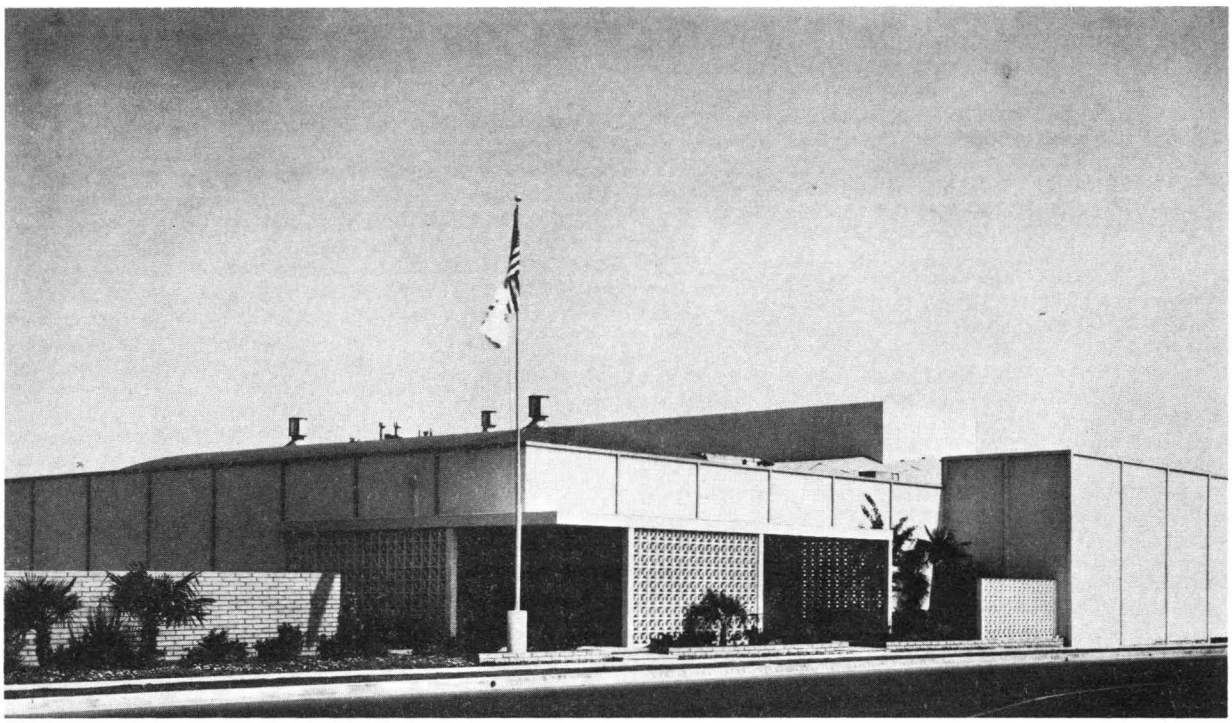


Figure A-1. Building No. 45, Van Nuys 18338-01

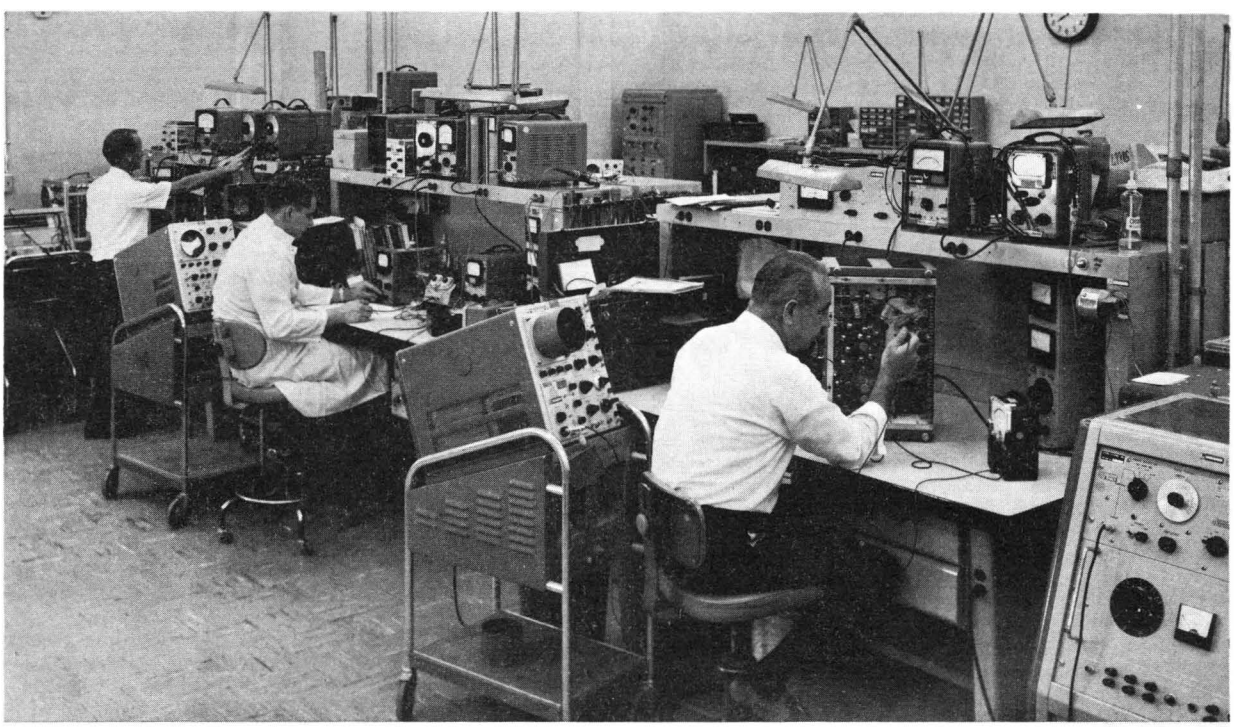


Figure A-2. Typical Engineering Laboratory, Van Nuys 18171-03

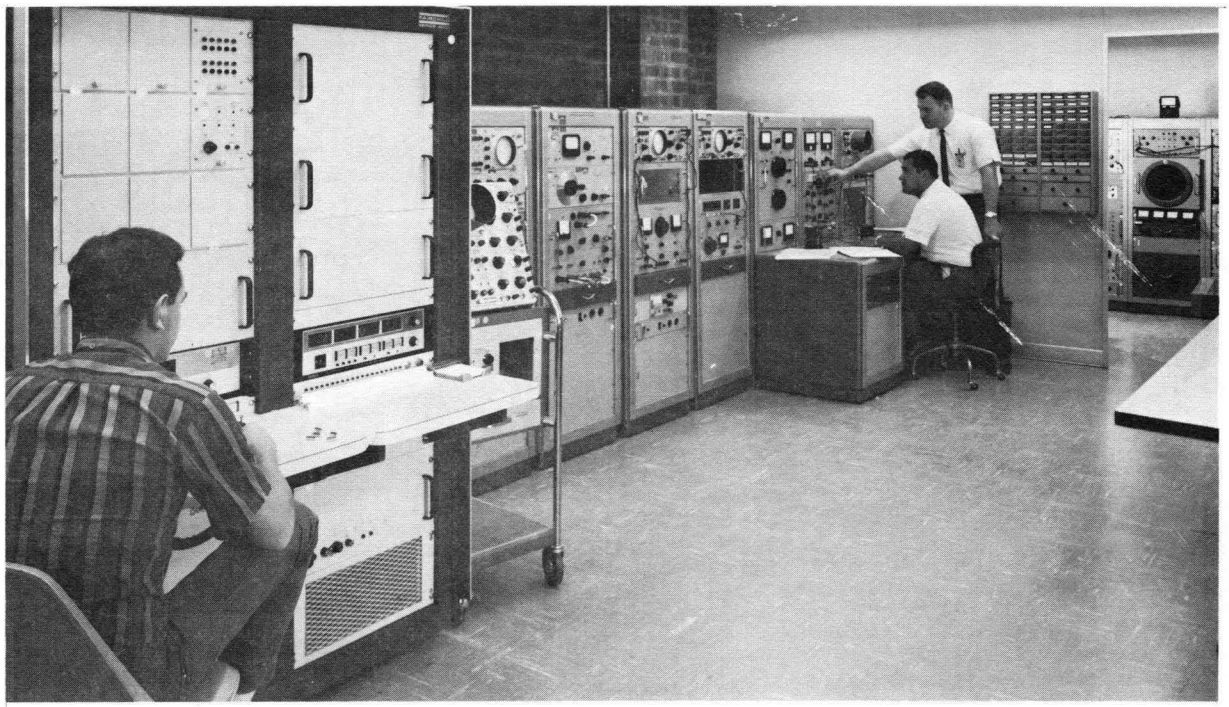


Figure A-3. Receiving Inspection Area, Van Nuys 18171-18

Figure A-4. Electronics Assembly Area, Van Nuys 927-01

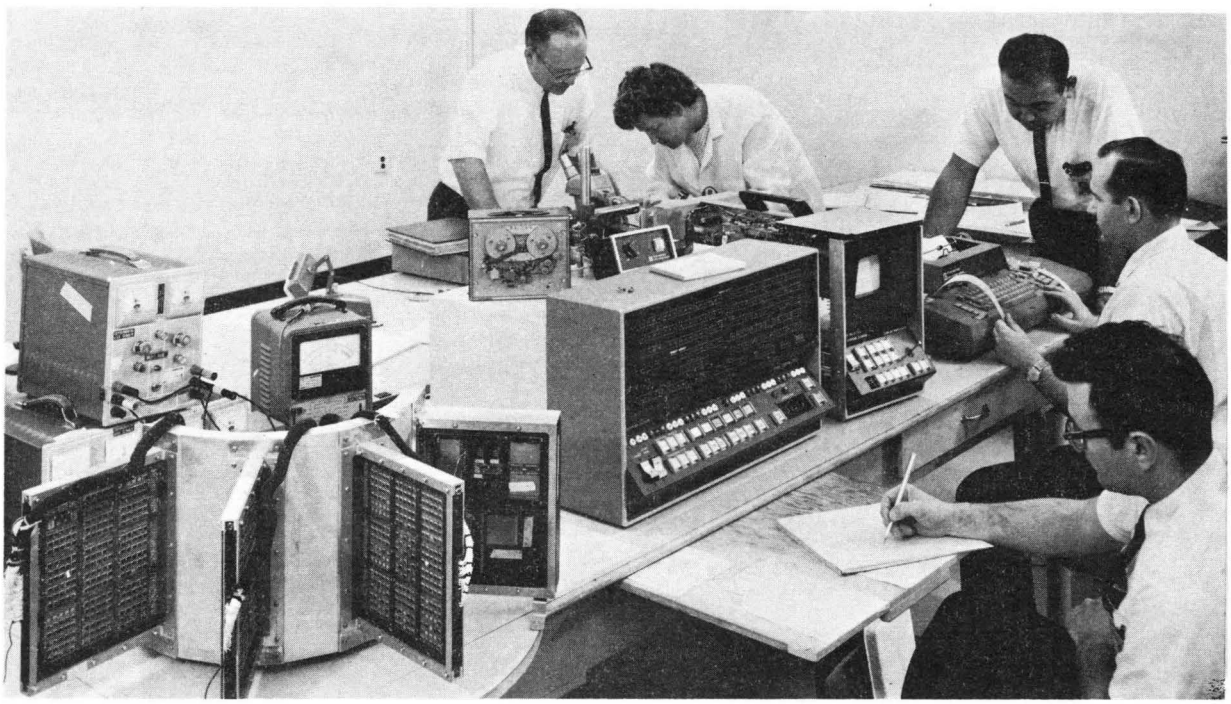


Figure A-5. Microelectronic Cards Undergoing Automated Testing, Van Nuys 5396-02

Figure A-6. Salt Lake City Plant 5370-07

Figure A-7. Electronics Assembly Area, Salt Lake City Plant 5370-06

A 4000-square foot research and development laboratory at Van Nuys is used in the microelectronics program. The laboratory has specialized instruments, chemical process development facilities, analytical research laboratories and electronic test equipment valued at over $700,000.

The research and development facilities are designed to allow technical personnel ready access to production areas, as is required in the rapidly advancing high-technology fields in which DSD operates.

A-4 MICROELECTRONIC EQUIPMENT PRODUCTION FACILITIES

A 10,000-square foot area at Van Nuys is assigned exclusively to the production of subassemblies incorporating integrated circuits. Over 5500 square feet of this floor space is a clean-room complex devoted to the manufacture of multilayer circuit boards, and the mounting of components on these boards. As indicated by the floor plan, Figure A-8, the clean-room area is completely self-contained. This facility was planned specifically for the production of microelectronic subassemblies, and it incorporates the latest advances in manufacturing equipment and line-flow production techniques. Inspection and test facilities are included. Utilizing a special

air-conditioning system, the entire area is maintained at a Class 100,000 clean-room level, with the photoresist room maintained at Class 10,000. Air lock pass-throughs are provided where required, to prevent cross-contamination between rooms.

The multilayer board fabrication line contains custom-designed plating consoles with polyvinylchloride panels. A chemical-mixing room, a photoresist laboratory, and separated rooms for material preparation and laminating are provided. The first stages of multilayer board production are performed in the cleaning and laminating room, and in the material preparation area. From there, materials proceed through a pass-through to the photoresist room. An air lock at the entry door to the photoresist room reduces the possibility of foreign material affecting the precision photographic reproduction of images on board materials.

The next stage is the plating and etching area, shown in Figures A-9 and A-10. The consoles and plating tanks are arranged to accommodate line-flow production. Chemical solutions, from initial chemical etching through copper- and gold-plating, are monitored by a periodic chemical analysis to ensure integrity of the solutions — an essential factor in the production of high quality boards. Room and chemical-solution temperatures are closely controlled.

From the plating area, board layers return to the cleaning and laminating room for application of the next base layer, and return through the photoresist, plating, and etching circuit. After the last layer has been processed, the boards are ready for the attachment of microelectronic components and final inspection. (Refer to Figures A-11 and A-12.)

Inspection stations are located at strategic points throughout the clean-room area to permit in-process inspection. Final inspection takes place in a room specificially assigned to that purpose. A system test area is provided for the electrical test and checkout of completed assemblies.

In addition to the clean-room area, floor space is available for the assembly of panels, main frames, and end-items for microelectronic projects.

The experience of DSD in the application of integrated-circuit technology has shown that techniques and controls applied to the production process and, in addition to the physical aspects of the facility, of vital importance to the quality of the end product. For example, the receiving inspection of all raw materials and integrated-circuit elements must be carefully planned and performed. Having been a large user of integrated circuits for some time, DSD has developed an integrated fabrication facility with an established routine of processing and control. It is DSD's considered

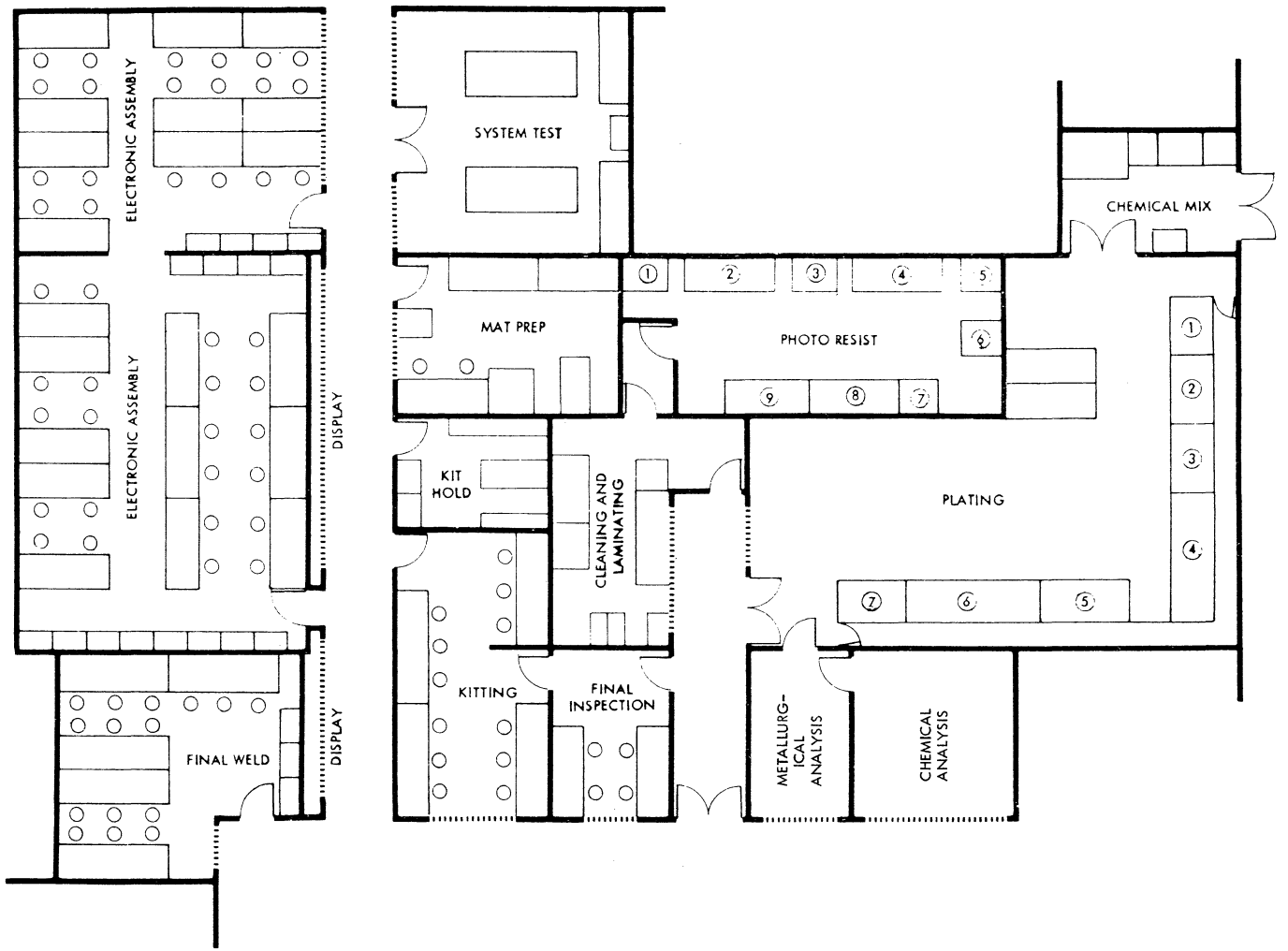


Figure A-8. Floor Plan of Clean-Room Production Area, Van Nuys

1290-7

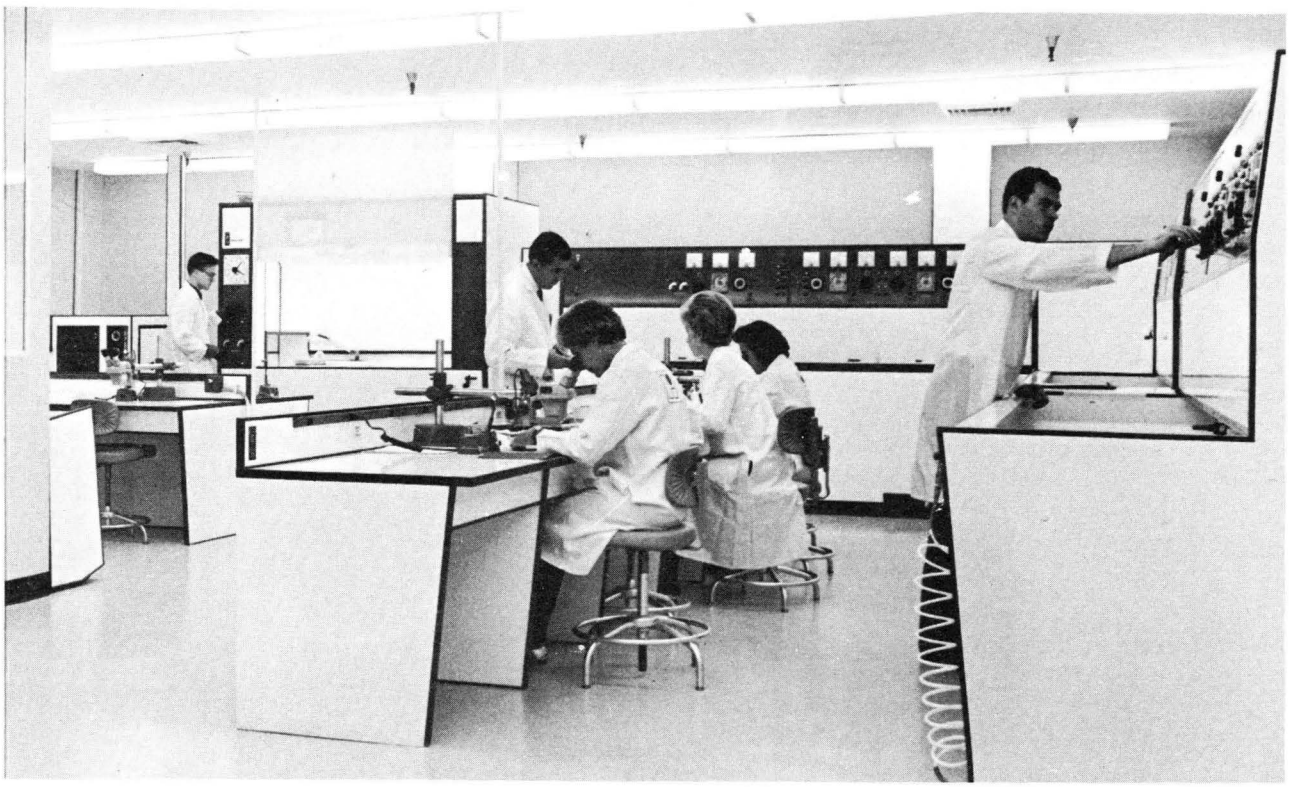


Figure A-9. Plating Room 5437-157

opinion, based on several years experience in the microelectronics field, that the application and development of present-day techniques will continue to yield significant economies in the manufacture of high-quality microelectronic products.

A-5 COMPUTER FACILITIES

Research and development work at DSD is supported by computing and data processing facilities located at the Van Nuys plant. (Refer to Figure A-13.) The computers used are an IBM 360-50 system with 262K storage capacity. Peripheral equipment includes 14 IBM Type 729 and 2400 magnetic tape units, IBM Type 2311 random-access disc storage files (7 each), and a Type 2403 1100 line/minute printer. The computer center activities are supported by a punched card machine section. Should an overload occur, IBM 7094 and IBM 360 computers are available nearby on a standing rental agreement.

A-6 ENVIRONMENTAL TEST FACILITIES

An Environmental Test Laboratory is used regularly by DSD's reliability and quality assurance staffs to support research and development, and to assure conformance with contract requirements. The laboratory has comprehensive facilities

Figure A-10. Etching and Plating Area Designed for Maximum Efficiency

5477-152

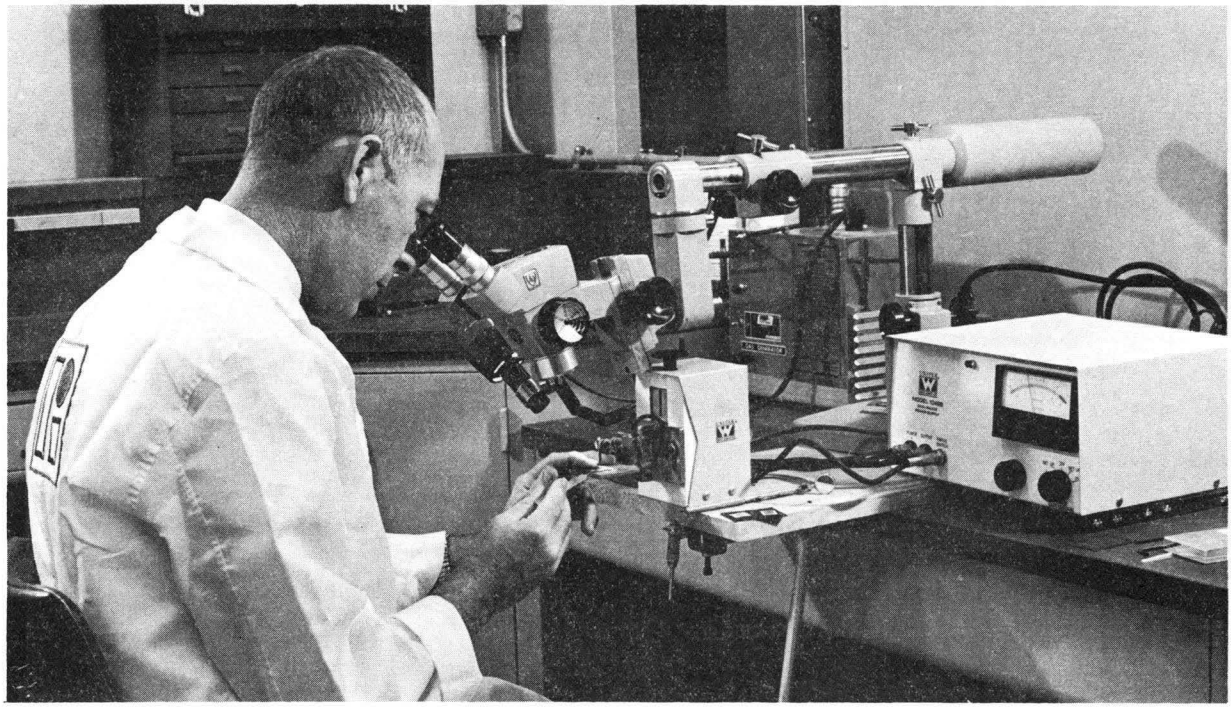


Figure A-11. Attachment of Components to Multilayer Laminated Boards, Using Microwelder 3095-117

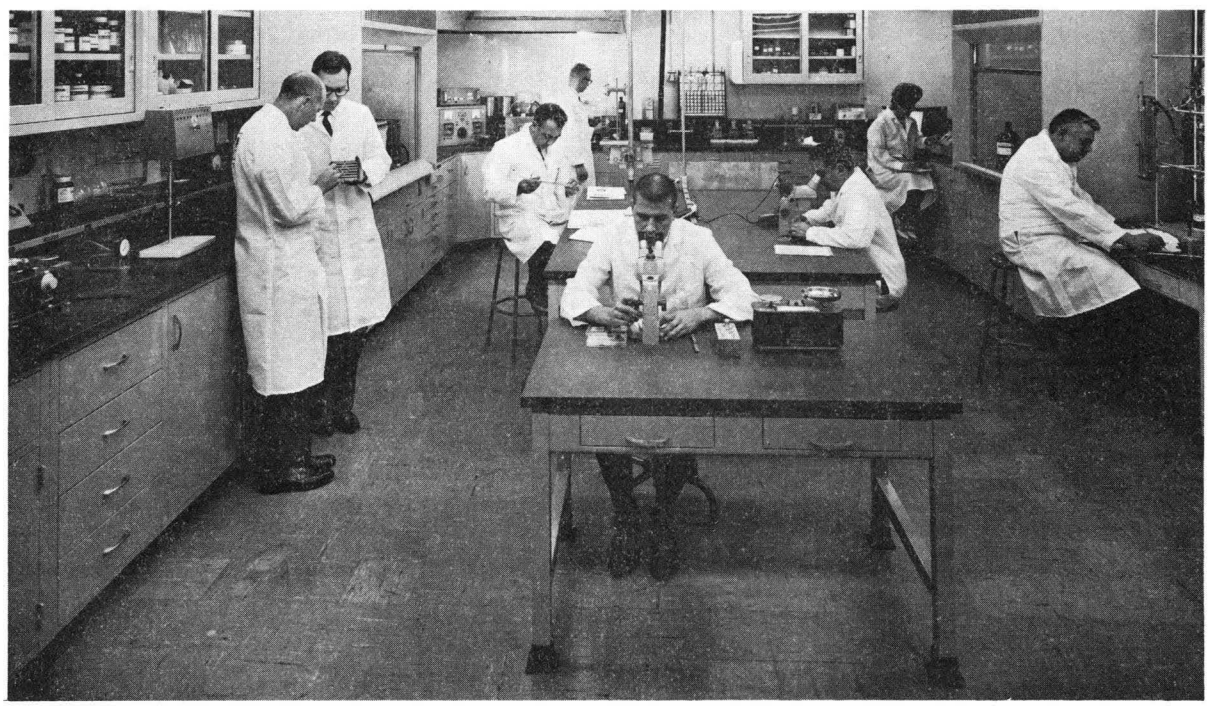


Figure A-12. Inspection Area within the Microelectronic Production Area 3095-06

Figure A-13. Van Nuys Data Processing Facility 5961-02

for the environmental testing of components and assemblies. Table A-I is a list of the testing equipment in the laboratory; measuring equipment and recording devices also are available in the laboratory.

MANUFACTURER	MODEL	DESCRIPTION	
BARRY CONTROLS	150-400VD	SHOCK TEST MACHINE	Test space: 30 inches by 30 inches by 30 inches Maximum specimen weight: 400 pounds Range: 7-77g, depending on shock duration selected (6.5, 11, 24 to 32 milliseconds)
BEMCO	WFA-100-27	TEST CHAMBER, ALTITUDE AND TEMPERATURE	Test space: 3 feet by 3 feet by 3 feet Temperature: -85°C to 150°C Humidity: 20 to 100 percent RH Altitude: site to 150,000 feet
BEMCO	WF-75-27	TEST CHAMBER, TEMPERATURE	Test space: 3 feet by 3 feet by 3 feet Temperature: -75°C to 125°C Humidity: 20 to 100 percent RH
BEMCO	WF-10-36	TEST CHAMBER, TEMPERATURE	Test space: 4 feet by 3 feet by 3 feet Temperature: -10°C to 95°C Humidity: 20 to 100 percent RH
BEMCO	W-36	TEST CHAMBER, HUMIDITY	Test space: 4 feet by 3 feet by 3 feet Temperature: 20°C to 100°C Humidity: ambient to 95 percent RH
BEMCO	SS-30	TEST CHAMBER, SALT SPRAY	Test space: 4 feet by 3 feet by 2-1/2 feet Chamber meets requirements of: MIL-E-5272A, Amendment 1 MIL-STD-202, Method 101
CALIDYNE	A88	VIBRATION TABLE,	5 to 3,000 cps 1.0 inch maximum double amplitude 100 force pound capacity 33g maximum acceleration
CALIDYNE	A174	VIBRATION TABLE, ELECTRONIC	5 to 3,500 cps 1.0 inch maximum double amplitude 1,500 force pound capacity 79g maximum acceleration
GRIEVE-HENDRY	MT	OVEN, ELECTRIC	Test space: 2 feet by 2 feet by 2 feet Temperature: 550°F
LITTON		SPACE CHAMBER	Test space: 700 cubic feet Altitude: above 500,000 feet
STATHAM	TC 4B/S	TEST CHAMBER, TEMPERATURE	Test space: 20 inches by 7 inches by 7 inches Temperature: -90°F to 600°F
WOODMARK	CUSTOM BUILT	VIBRATION TABLE, MECHANICAL	5 to 55 cps 1 inch maximum double amplitude 50 force pound capacity

Table A-I. Environmental Test Equipment 1290-8

DATA SYSTEMS DIVISION OF LITTON INDUSTRIES