# matrox

matrox
electronic systems ltd.

# OEM
# BOARDS AND SYSTEMS
# DATA CATALOG

PRICE: $25

CAT-01-01
JUNE 1983

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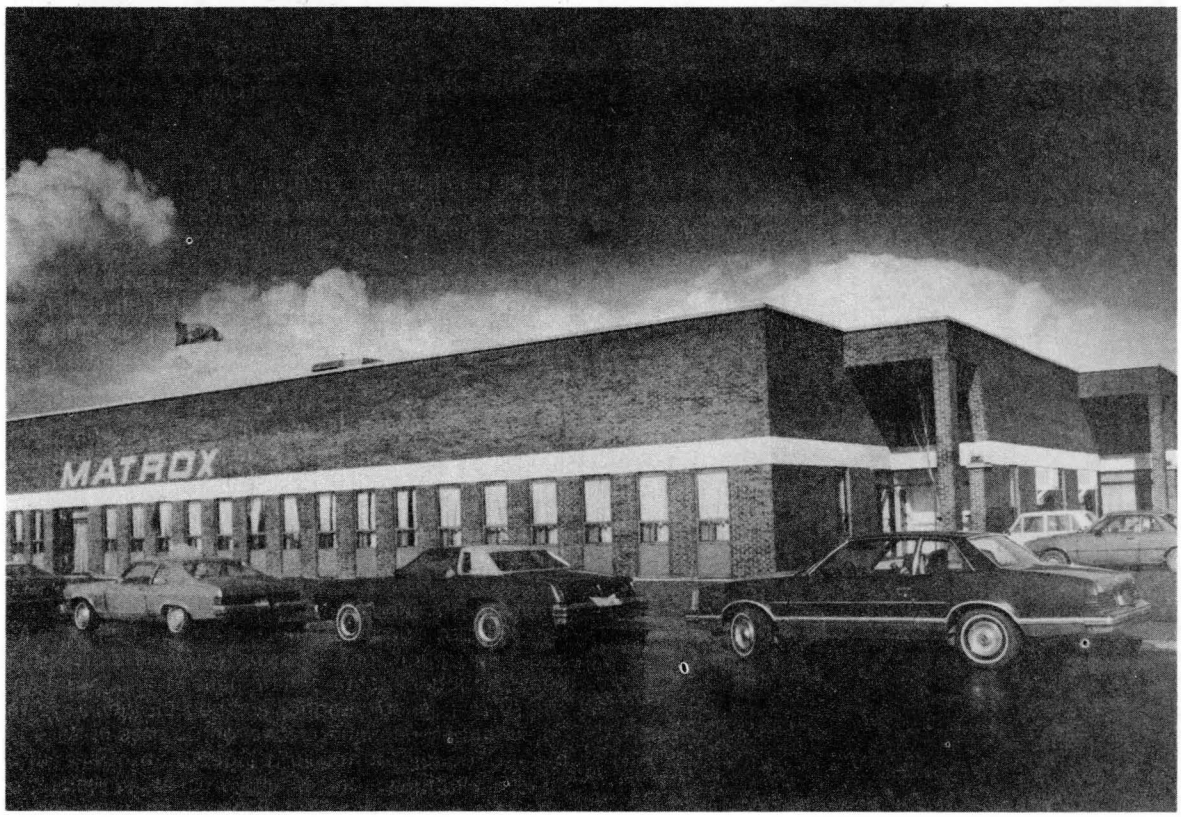



Figure 1. Matrox 27,000 square foot production facility in Montreal, Canada.

# INTRODUCTION

**Matrox is a world leader in the design and manufacture of computer graphics boards and systems. The company is one of the pioneers in raster scan graphics, having been manufacturing video and computer systems for OEM's for over seven years.**

## PRODUCTS

The original Matrox product offering consisted of a series of Video RAM modules providing simple inexpensive displays for OEM applications. These video modules were so successful, that they still remain as viable products today.

With the introduction of standardized bus architectures in the late 70's, the Matrox product line grew to include several "board" level offerings. Matrox video boards are available for a number of industrial buses including Multibus, Q-Bus, Uni-Bus, STD-Bus, S-100 bus and Exorcisor bus.

As the company's expertise in graphics developed, marketing opportunities for complete graphics systems led Matrox to expand the Multibus product line to include CPU boards, memory boards, communication controllers, disk controllers, and Multibus cardcages.

Matrox currently markets a complete line of boards, cardcages, color monitors, keyboards and complete turnkey color graphics terminals and systems.

Future growth for the company will come from new products. Matrox will continue to set the pace in the development of high resolution high performance video boards and systems, and will expand its software and service offerings to support the future needs of a growing base of customers.

## FACILITIES

Matrox was founded in 1976. The company currently employs about 200 people in two Montreal based plants and a New York based distribution centre. A 22,000 square foot facility houses sales, R & D and administration. A second 27,000 square foot plant houses production, and production engineering.

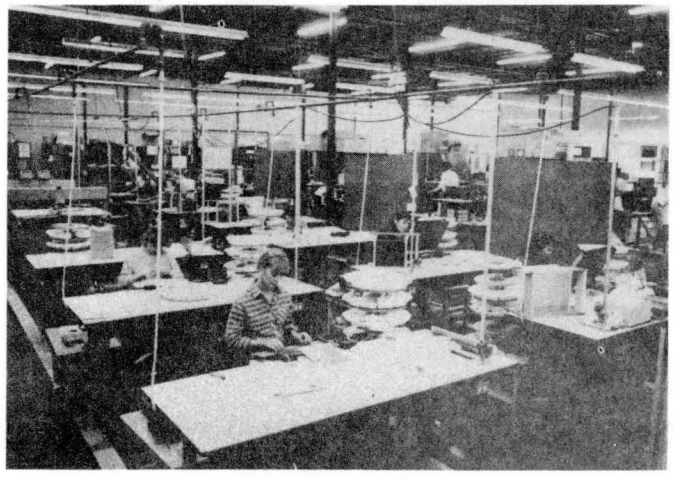
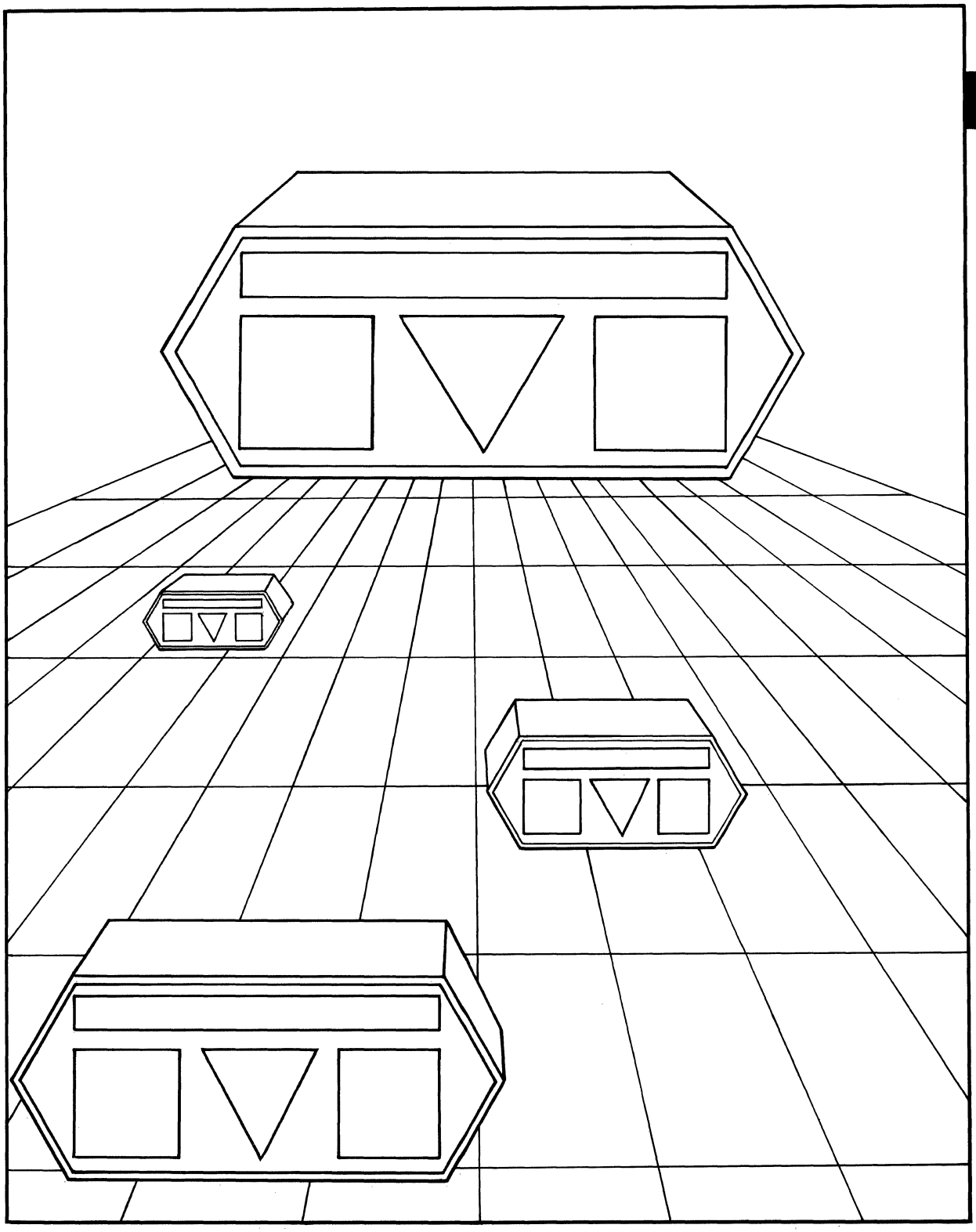


Figure 2. Board assembly area.



# QUALITY ASSURANCE


Figure 3. Matrox 22,000 square foot administration and engineering facility in Montreal, Canada.

## DISTRIBUTION

Matrox products are sold world wide through a network of representatives and distributors. Over 95% of the company's production is shipped to export markets including the United States, Europe, Australia and Japan.

Matrox is dedicated to serving the world marketplace, and will continue to emphasize solid relationships with the company's distributors in order to provide strong local support for its clients.


Figure 4. Matrox MTX-1632 Video RAM is used in the console of this industrial robotics system.
(photo courtesy of Graco Robotics Inc.)

## APPLICATIONS

Matrox products have provided a cost effective solution for a wide and varied number of applications. Some of the larger industries served by the company include:

— Process control

— CAD/CAM

— Medical Electronics

— Robotics

— Computer Aided Instruction

— Financial Displays

— Engineering Work Stations

— Geophysical/Seismic Displays

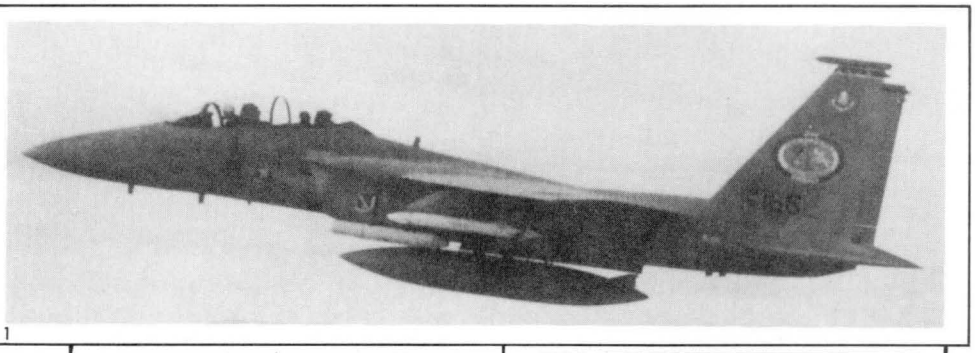
— Military Electronics

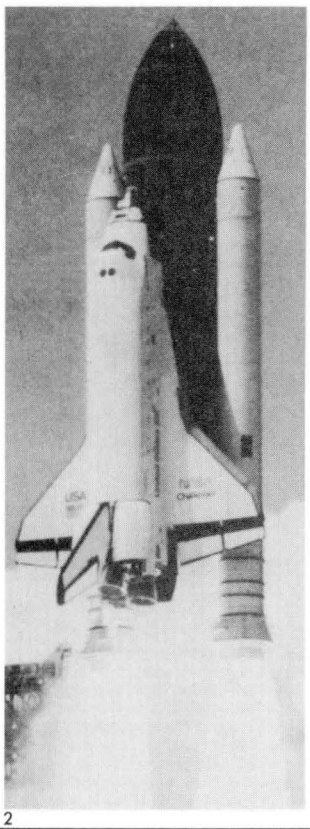
— Presentation Graphics

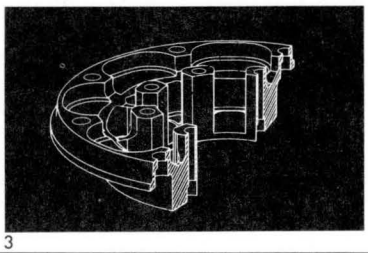
— Business Graphics

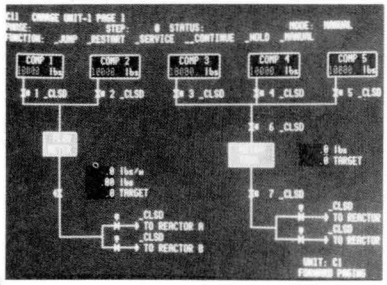
— Public Information Displays

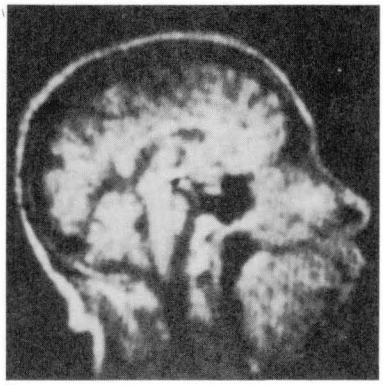
Matrox typically manufactures board or system level products for OEM customers. OEM's incorporate additional hardware and applications software to suit their particular requirements.

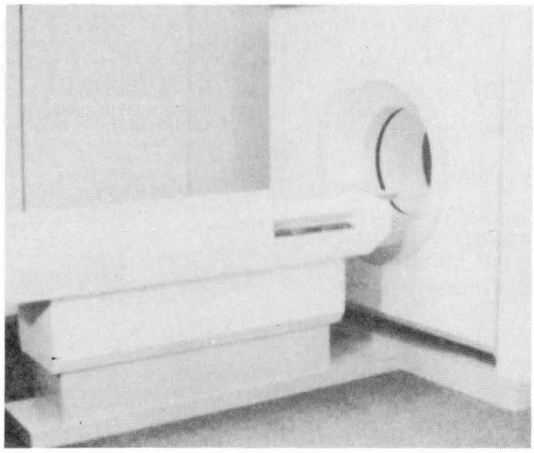


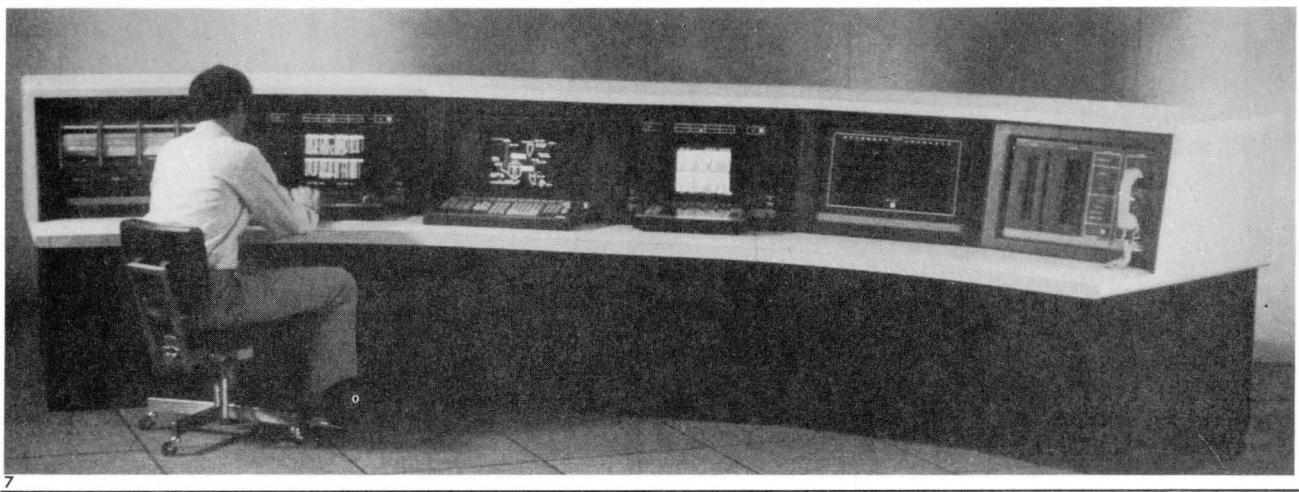






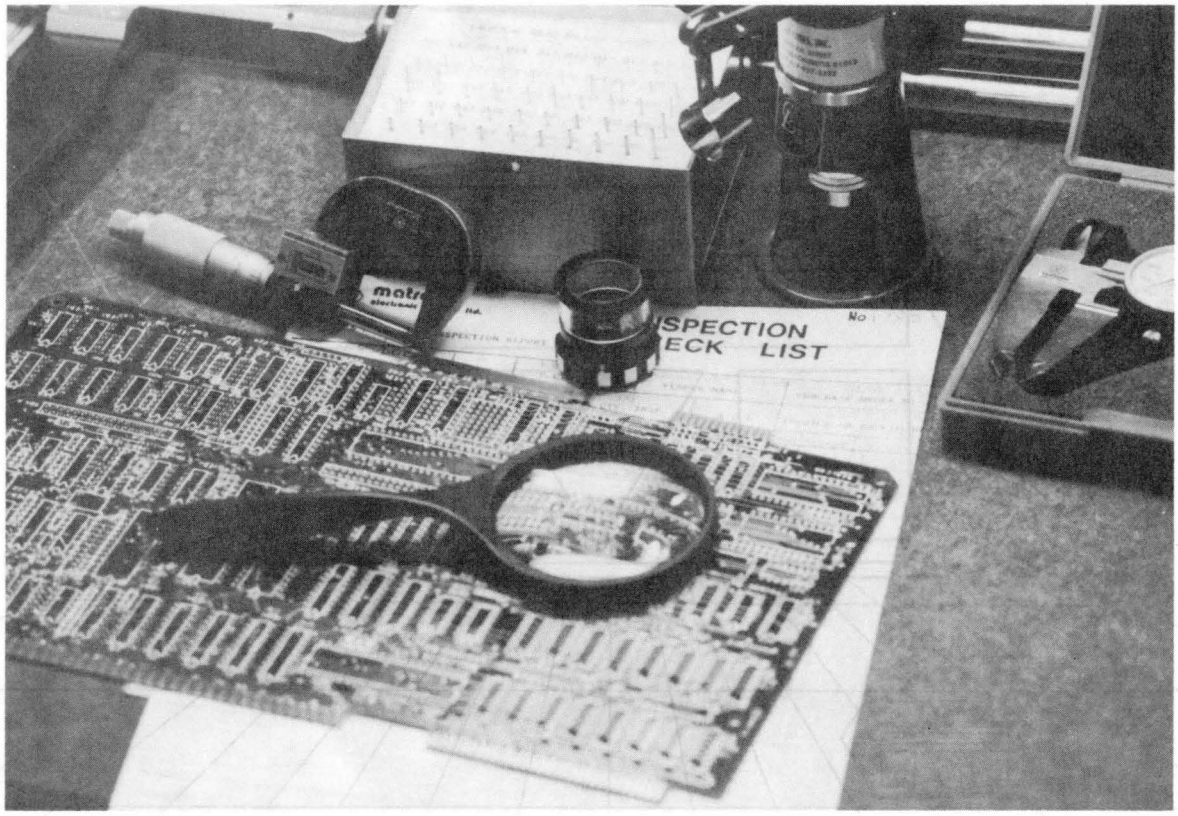







**Matrox OEM customers use Matrox products in a wide range of applications**

1 & 2 — Matrox products are used in a number of applications in the Aerospace Industry.
3 — Matrox display controllers are capable of generating very high resolution color CAD/CAM images.
4 — Process control displays can be generated using high resolution bit-mapped graphics or low cost character graphics with Matrox display controllers.
5 & 6 — Matrox is a major supplier of graphic display controllers to the OEM Medical Electronics Industry.
7 — Process control workstations use several computer controlled graphic displays.




# QUALITY ASSURANCE

**Quality assurance means conforming to specifications.**

## QUALITY IN DESIGN

Performance, reliability, and quality are all important considerations in the design process. Quality must be woven into the design fabric, not added to the finished design. A good designer considers the customer, the service technician, and the manufacturing staff when developing a new product.

At Matrox, we are strongly committed to excellence in design. Our component library lists all Q.A. approved parts and approved sources for those parts. Much emphasis is placed on second source components. All new engineering designs are tested, at the prototype level, with complete sets of integrated circuits from several manufacturers. Engineering prototypes are submitted to an extensive series of tests which include: functional, temperature, and humidity testing, as well as a full 200 hour dynamic burn-in at 60°C.

## QUALITY IN PROCUREMENT

To ensure the reliability of our products, we must demand quality from our suppliers. Matrox works closely with reputable vendors to set up long term stable sources of supply. In the case of critical items, such as multilayer circuit boards, each approved vendor is visited at least once a year to ensure that their quality control measures are up to our standards.

## INCOMING INSPECTION

Occasionally, vendors do slip up. It is the role of the Matrox Incoming Inspection Group to ensure that all supplies entering the manufacturing area do conform to specifications. All items are subjected to thorough electrical and mechanical analysis. Bare circuit boards are 100% checked for warpage, twists, size, registration, revision level, silkscreen, and proper plating before being allowed into the raw materials inventory. All digital integrated circuits are 100% inspected on a go/no-go GENRAD "hot-rail" IC tester which performs a complete electrical test at an elevated temperature.

Any rejected materials are clearly tagged, logged, and turned over to a Management Review Board (MRB) for disposition. If one vendor consistently has rejects, the situation is flagged, and corrective action can be taken.

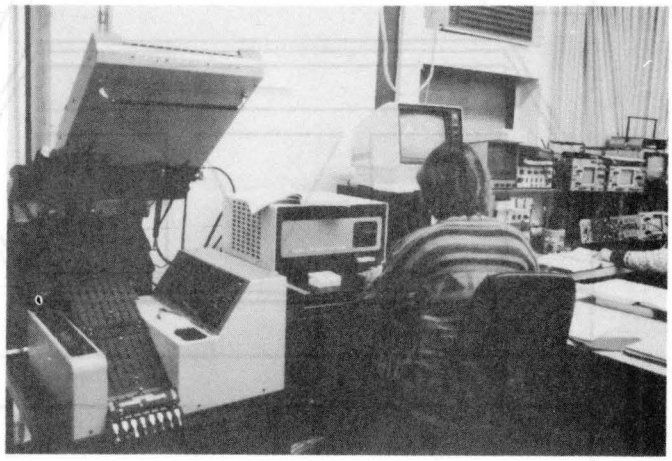


Figure 1. All digital ICs are tested at an elevated temperature on a "hot-rail tester" before entering raw materials inventory.

## QUALITY AS AN ATTITUDE

Quality in a manufacturing environment requires more than a series of inspection stations. Quality starts with people, and their attitude towards their work.

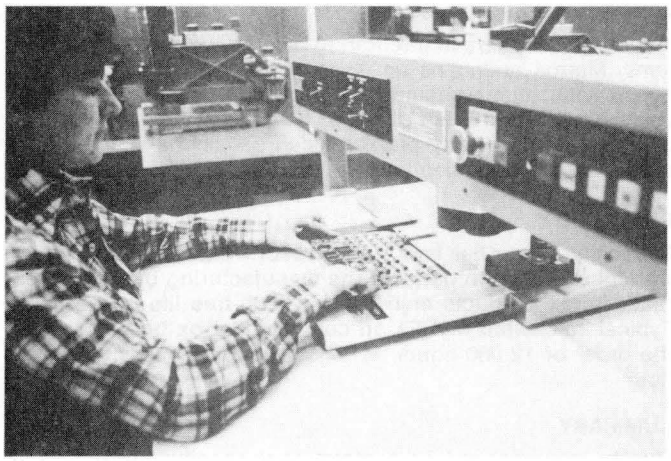


Figure 2. Semi-automatic insertion equipment simplifies assembly and reduces assembly errors.

Taking a lesson from the Japanese, the company has set up a Quality Circles program, whereby every worker has an opportunity to introduce improvements that pertain to his particular job in the manufacturing process.

Quality circles get people involved in their work, and allow them to see tangible results from their efforts. Quality products and pride in workmanship are closely correlated. Attitudes are an important factor in ensuring that products conform to specifications.

**QUALITY IN ASSEMBLY**

Matrox has an enviable production record from the standpoint of quality control. A meticulous set of checks and balances between assembly and inspection has resulted in almost zero reworks, and a defective goods return rate of less than 1%.

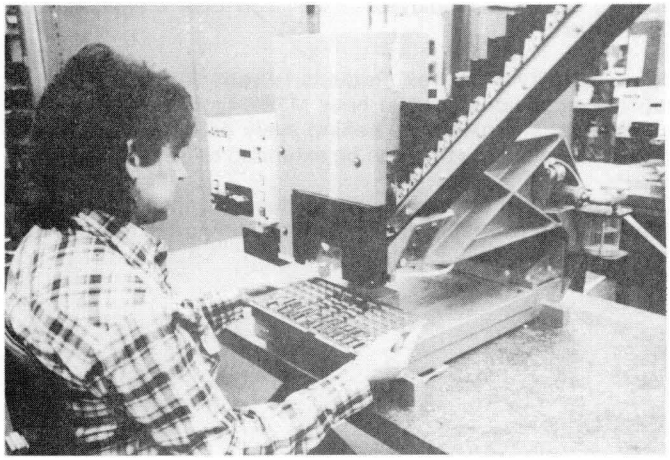


Figure 3; DIP inserter automatically inserts, bends, and clips IC leads to the proper length.

Our excellent quality record is due in part to a substantial investment in automatic assembly equipment including: DIP insertors, component insertors, lead forming equipment, pin insertors and a wave soldering machine. The automatic equipment is ideal for manufacturing large quantities of product.

Soldering is a very important stage in the manufacturing process. Matrox technicians thoroughly inspect the wave solder machine daily and measure solder contaminant levels on a monthly basis. Wave soldering consistently turns out excellent soldering results because every board is preheated to the correct temperature, and passed through a flux bath just prior to entering the wave. After soldering, all boards are cleaned in a freon bath and carefully inspected for flaws.

All of the production personnel involved with soldering are required to attend and pass a comprehensive course on soldering techniques. Also, each assembler is provided with a "workmanship standards" manual which identifies, using large color pictures, what is and is not acceptable for a solder joint. The workmanship manual is based on the Martin Marrietta standards for the aerospace industry.

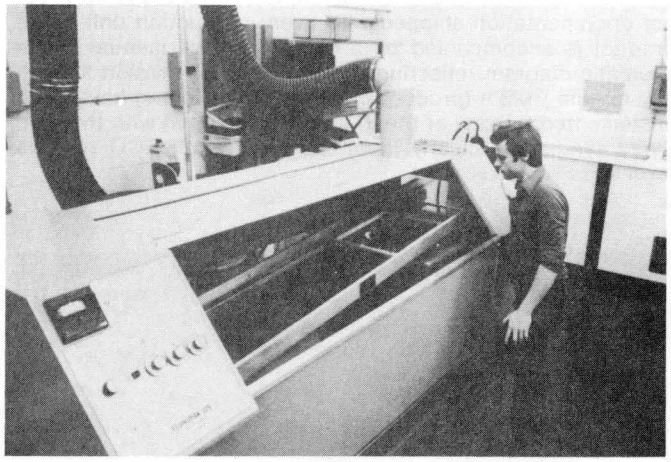


Figure 4: All Matrox boards pass through a wave solder machine which turns out consistent excellent results.

**INSPECTION**

After each step in the assembly procedure, all products are fully inspected by an inspector who must stamp the board and the routing sheet with his unique marker. Boards are 100% inspected after insertion, after wave soldering, after touch-up, after test and after system test. Boards are assigned a serial number immediately after wave soldering, thus allowing complete inspection and test records to be maintained throughout the manufacturing process.

**QUALITY IN TEST**

Every Matrox product undergoes two extensive functional tests and a 48 to 72 hour dynamic burn-in at 60°C. Every board is functionally tested against a comprehensive set of minimal performance specifications, which include normal, low voltage, and high voltage checks.

Initial testing is performed on a Zentehl "bed of nails" tester which provides a diagnostic printout for every board. The Zentehl tester identifies 95% of all faults on all cards. After the initial test, any faults are repaired, the board is retested, and is then sent to burn-in.

After burn-in, a comprehensive systems test is performed to identify any infant mortality problems. If a fault is found, the card is again burned-in and recycled through the systems test.

**DOCUMENTATION AND TRACEABILITY**

Despite an extremely rigorous test and inspection program, some number of products do reach the customer with a problem. It is extremely important that problems discovered both in the field and in the plant be properly identified, so that remedial action can be taken. To ensure traceability of problems, Matrox keeps comprehensive records on each individual product shipped (referenced by serial number). These records provide a log of all of the assemblers, inspectors, and test technicians who worked on the product, as well as a listing of

any faults found in the production of that product. A summary of field repairs its analyzed every month, so that any trends can be identified. If a large number of faults appear to be associated with a particular assembler or a particular test jig, corrective action is taken.

Similarly, for all batches of new materials coming into the plant, records are maintained for the incoming inspection test results. If a problem appears to be associated with a particular batch of components, that batch and the supplier of the parts can be identified.

Another important quality consideration is the standard product documentation shipped with every production unit. Each product is accompanied by a comprehensive manual and a shematic diagram reflecting the proper ECO revision level. If any interim PMB's (product modification bulletins) have been implemented, a copy of the PMB is also shipped with the unit. Every product is clearly identified as to both ECO revision level and PMB level.

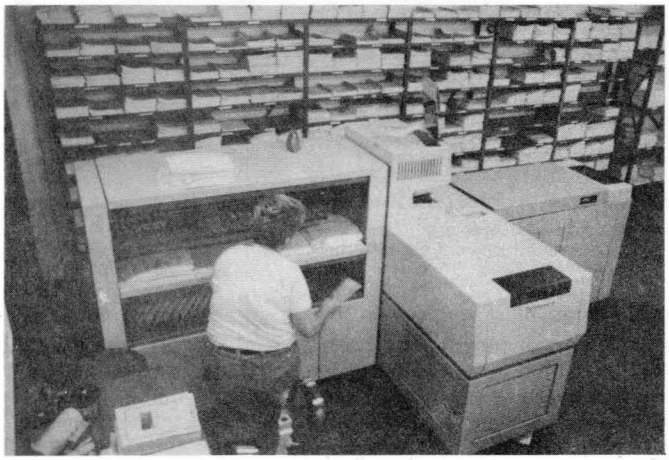


Figure 5: Matrox product documentation is complete and accurate. All documentation is controlled in-house.

## WARRANTY

Matrox guarantees the functionality of every manufactured item with a six month all inclusive parts and labor warranty. This warranty can be extended to one or even two full years for volume OEM customers.

## AFTER SALES SUPPORT

To assist customers in integrating our products into their systems, Matrox maintains an Applications Engineering Group. These applications engineers work with customers in setting up, testing, and trouble shooting Matrox products. Over 50% of all perceived quality problems can usually be isolated and corrected over the telephone.

## RELIABILITY

Reliability is another important aspect of Quality Assurance. Careful attention to detail in the manufacturing cycle assures that Matrox products enjoy a long fault-free life in the field. Typical calculated MTBFs on complex Matrox boards are on the order of 12,000 hours. MTTRs are typically less then one hour.

## SUMMARY

Quality assurance means conforming to specifications.

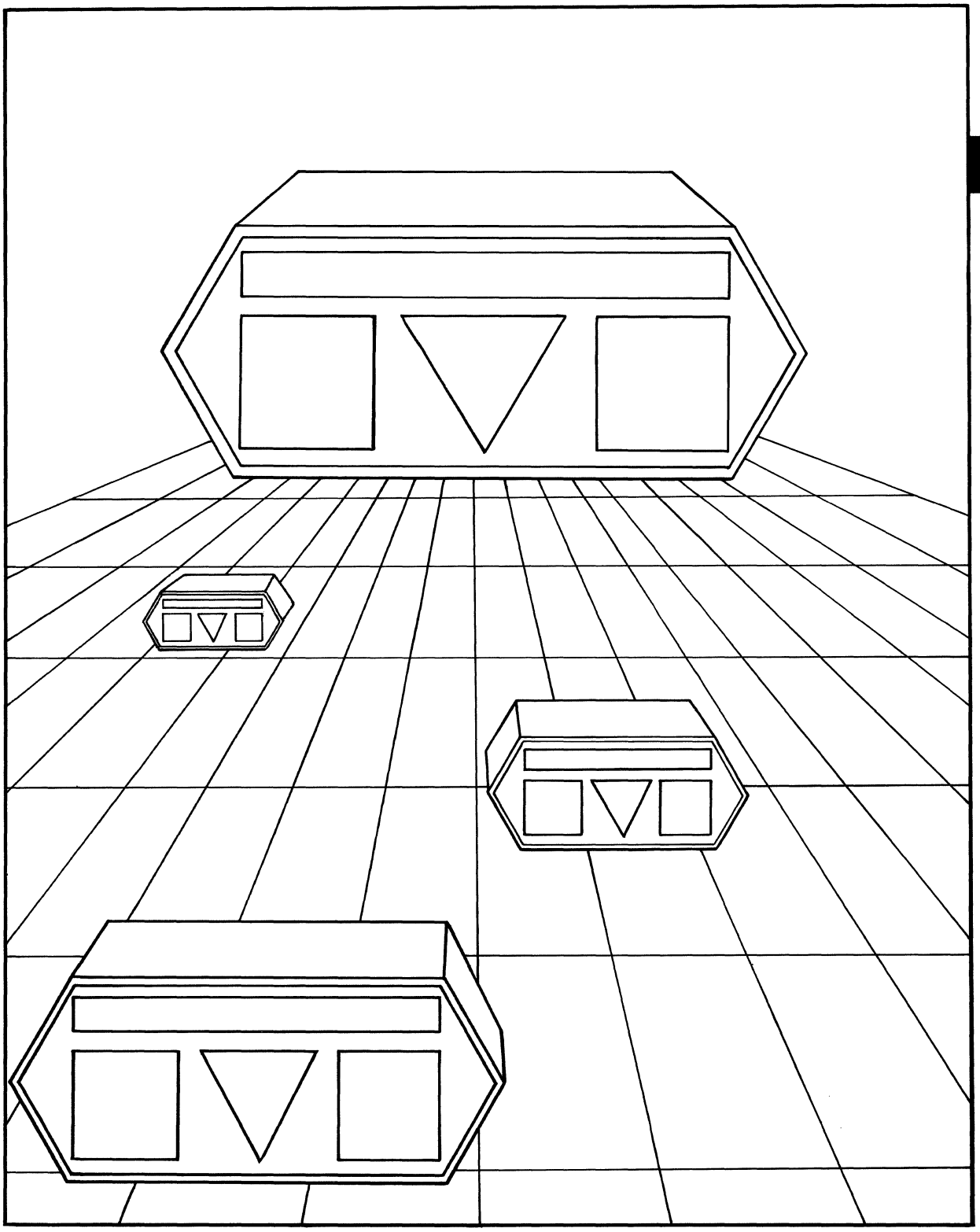
Matrox has an excellent quality record which boasts less than a 1% return rate of defective goods. This performance is achieved by people, who are dedicated to precision and perfection in what they do.

Quality can be achieved only by careful attention to detail at all stages of the manufacturing process. At Matrox, quality is a primary consideration in the design process, in parts procurement, in incoming inspection, in assembly, in inspection, and in test. Every product shipped by Matrox is required to pass two independent comprehensive sets of functional tests and a 48-72 hour burn-in at 60°C. When a product is allowed into finished goods inventory, we guarantee that it fully conforms to specifications.

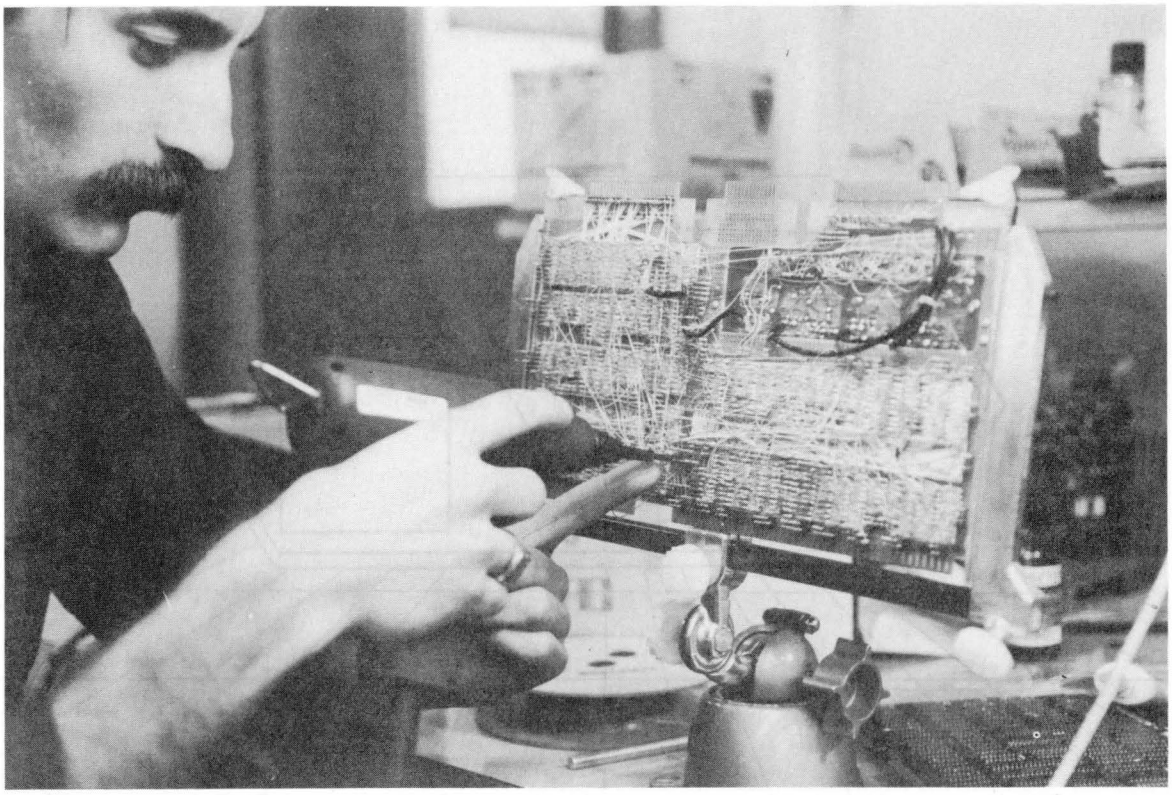
In order to correct problems on that fraction of a per cent of units that do fail in the field, Matrox maintains comprehensive records at all stages of the manufacturing process. These records provide the traceability necessary for proper feedback to the production group. Also, a well staffed Applications Engineering Group is employed to assist in fault diagnosis and field repairs.

The realiability of Matrox products is born out both by theoretical calculations (12,000 hour MTBF typical) and by field experience. Matrox stands behind every product with a comprehensive warranty that can be extended to two full years.

Quality does not stop when the product is shipped. Customer support ensures that Matrox products continue to meet specifications, in the field, for many years.



# CUSTOM CAPABILITY



# CUSTOM CAPABILITY

Matrox has extensive engineering expertise in both hardware and software for computer graphics systems. The company has done custom systems work for several Fortune 500 companies including McDonnell Douglas, General Electric, Philips, and Xerox. Our design ability, our experience, and our solid manufacturing capability permit Matrox to undertake complex projects with tight delivery schedules. Many of the company's standard products were originally developed as custom designs for large customers. Where new designs are undertaken for products with a significant market beyond the immediate requirements of a single customer, Matrox will share the development costs, or forego completely any engineering charges.

An engineering staff of over 80 people are organized by function into 6 engineering groups; Hardware, Software, Systems, Production, Applications and Research & Development (R & D) Groups. Additional engineering support groups include Drafting and Technical Documentation. Matrox's strong committment to R & D has contributed substantially to the company's role as a technological leader in the computer graphics industry.

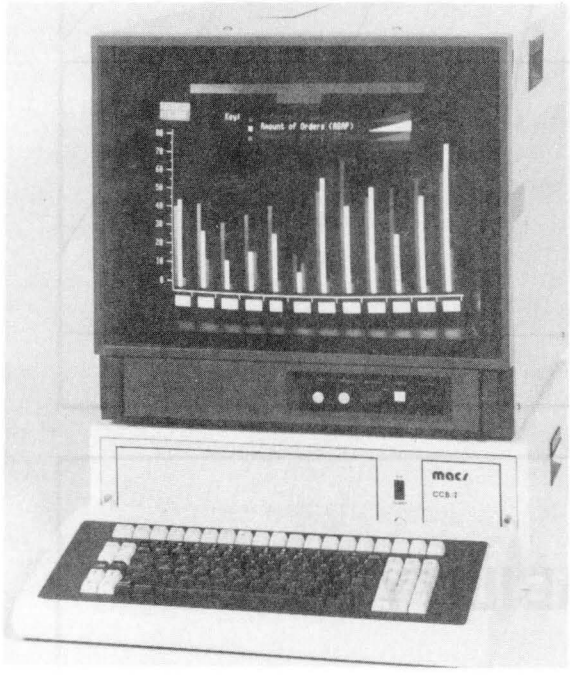


Figure 1. GF-18 graphics terminal is a custom product developed for McDonnell Douglas Corp.

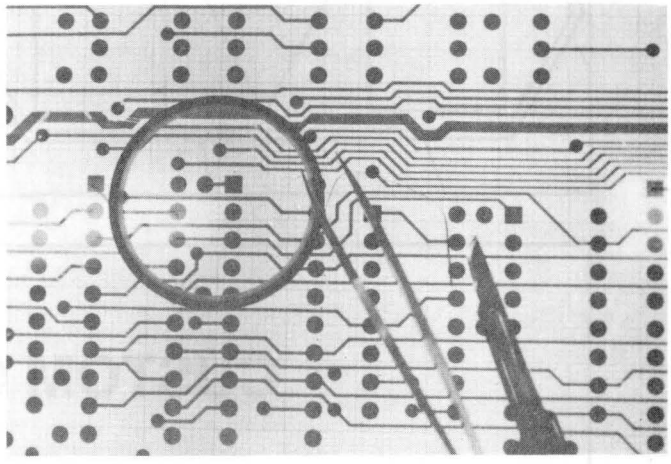


Figure 2. Matrox can generate complex multilayer board designs in 4 to 6 months.

## HARDWARE DESIGN

Matrox has a hardware design staff of over 30 experienced engineers. The company can develop entirely new board designs in about 4 to 6 months for prototypes, and 9 to 12 months for volume production.

For major contracts, a design team headed by a project manager is assigned to develop and maintain a schedule for the system. The schedule, which identifies all significant milestones and critical path items, is reviewed on a weekly basis in order to keep any deviations in check.

Matrox has considerable expertise in graphics design, CPU design, communications, and distributed processing systems.

## SOFTWARE DESIGN

Over ten experienced software engineers are employed in the Matrox Software Engineering Group. The company has extensive experience in assembly language programming for most popular microprocessors, as well as high level language programming in Fortran, C, and Pascal using a variety of operating systems including CP/M, CP/M-86, UNIX, RT-11, and VMS. Over 90% of all program development is done on a VAX-11/750 running under a VMS operating system.

At the heart of the company's new high resolution graphics system is a real-time multi-tasking operating system which supports multiple processors. The ROM-based MRTOS software was developed, in-house, in response to a need for real-time interactive system performance.

Much of the graphics systems work that Matrox has done has required that the software be compatible with the emerging CORE and GKS graphics standards. Matrox has also been involved in the proposed VDI (Virtual Device Interface), VDM (Virtual Device Metafile), and NAPLPS (North American Presentation Level Protocol Syntax) standards.

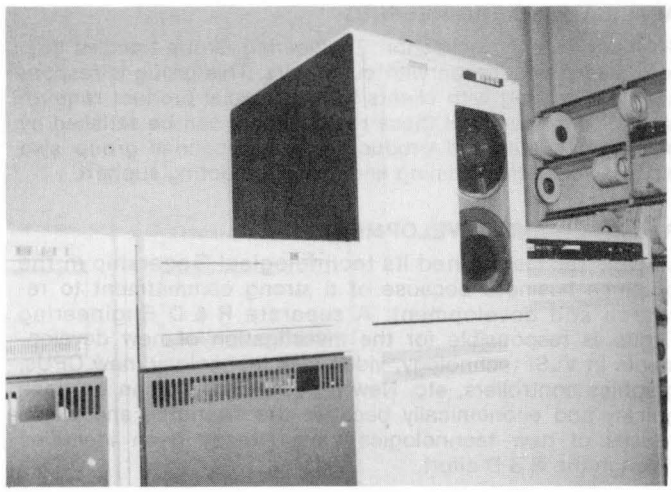


Figure 3. A VAX-11/750 is used for software development for most of the company's ROM and disk based software packages.

## SYSTEMS DESIGN

A separate Systems Engineering Group is responsible for all mechanical design and systems integration work. The systems group is also responsible for securing all regulatory approvals for Matrox products, including UL, CSA, DIN, VDE, and FCC. The systems group provides the experienced project management capabilities required for complex systems products.

## PRODUCTION ENGINEERING

A large well equipped Production Engineering Group is responsible for overseeing the introduction of new engineering designs to the production assembly line. The production engineering group designs all of the test fixtures and test procedures used in assembling, testing, trouble-shooting, and burning-in Matrox products.

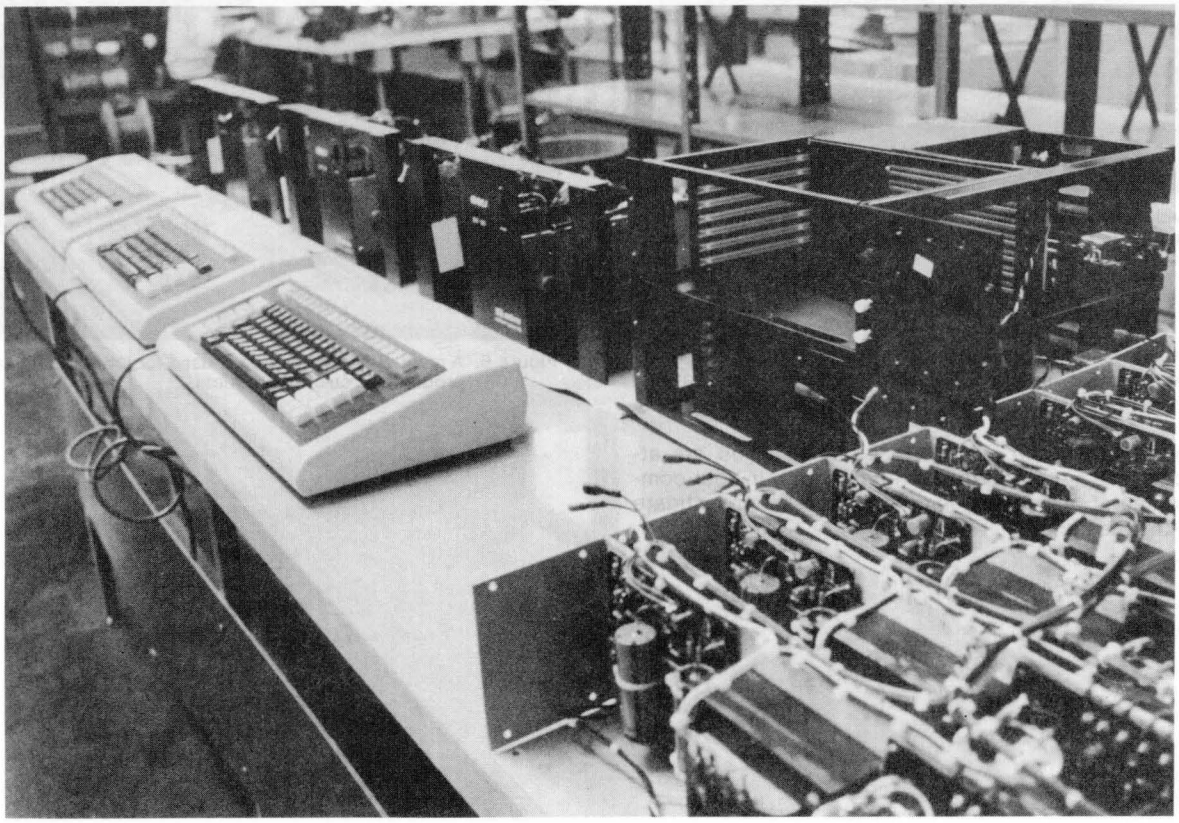


Figure 4. A large mechanical assembly area is used for custom systems work for OEM customers.

## APPLICATIONS ENGINEERING

An independent Application Engineering Group handles day-to-day technical liason with customers. This group is responsible for working with clients having special product requirements, to determine if these requirements can be satisfied by modifying a standard product. The applications group also provides customer training and trouble-shooting support.

## RESEARCH AND DEVELOPMENT

Matrox has maintained its technological leadership in the graphics business because of a strong committment to research and development. A separate R & D Engineering Group is responsible for the investigation of new developments in VLSI technology, video disk technology, new CPUs, graphics controllers, etc. New product designs can be done quickly and economically because the strengths and weaknesses of new technologies have already been identified through the R & D effort.

Figure 5. A video disk research project has produced a commercially viable 1.2 gigabyte archival storage system for picture, text, and audio data.

## MAKE VS. BUY

Many successful companies who have manufacturing capability are eager to build new products "in-house" if they cannot find an existing product that exactly meets their requirements.

The "in-house" approach is not always best. If you are attempting to source a product that is not generally in your company's main line of business, it is probably best to investigate outside custom designs.

Matrox's graphics experience and capability have been built up over a long period of time, and the costs associated with acquiring this expertise have been substantial. Typically the overhead costs associated with in-house designs far outweigh the benefits of lower direct costs, unless significant quantities of the product can be guaranteed.

## SUMMARY

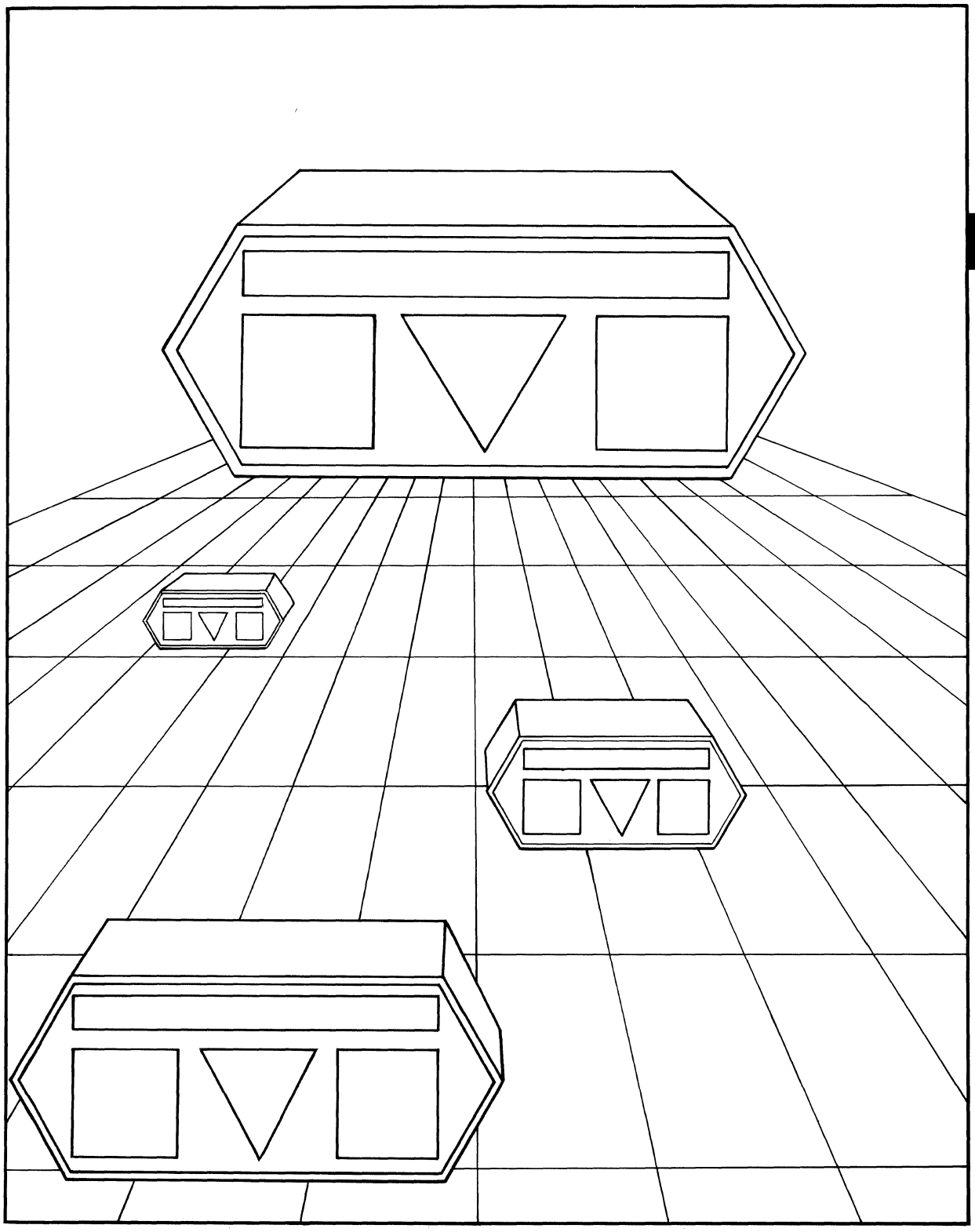
Matrox has extensive experience in custom board and system design. Many Fortune 500 companies have come to Matrox for custom products because of the company's engineering know-how, experience, and manufacturing capability to design, integrate, and produce top quality products in a short amount of time.

Most of the major products introduced by Matrox have originated as custom designs for our customers. This type of approach to product development has several benefits for both parties; the vendor is guaranteed at least one major customer for the product, and the customer is guaranteed a stable source of supply and minimal engineering costs.

Separate engineering groups are employed in hardware design, software design, systems work, production, applications, and R & D. Because of our strong engineering capability and our consistent product excellence, Matrox is regarded as a technological leader in the computer graphics field.

Matrox has the capability, the experience, and the resources to undertake custom graphics and microprocessor products. Talk to us about your special requirements before you commit to a Make/Buy decision.

Figure 6. A manual assembly area is used for low-volume standard products or custom products.



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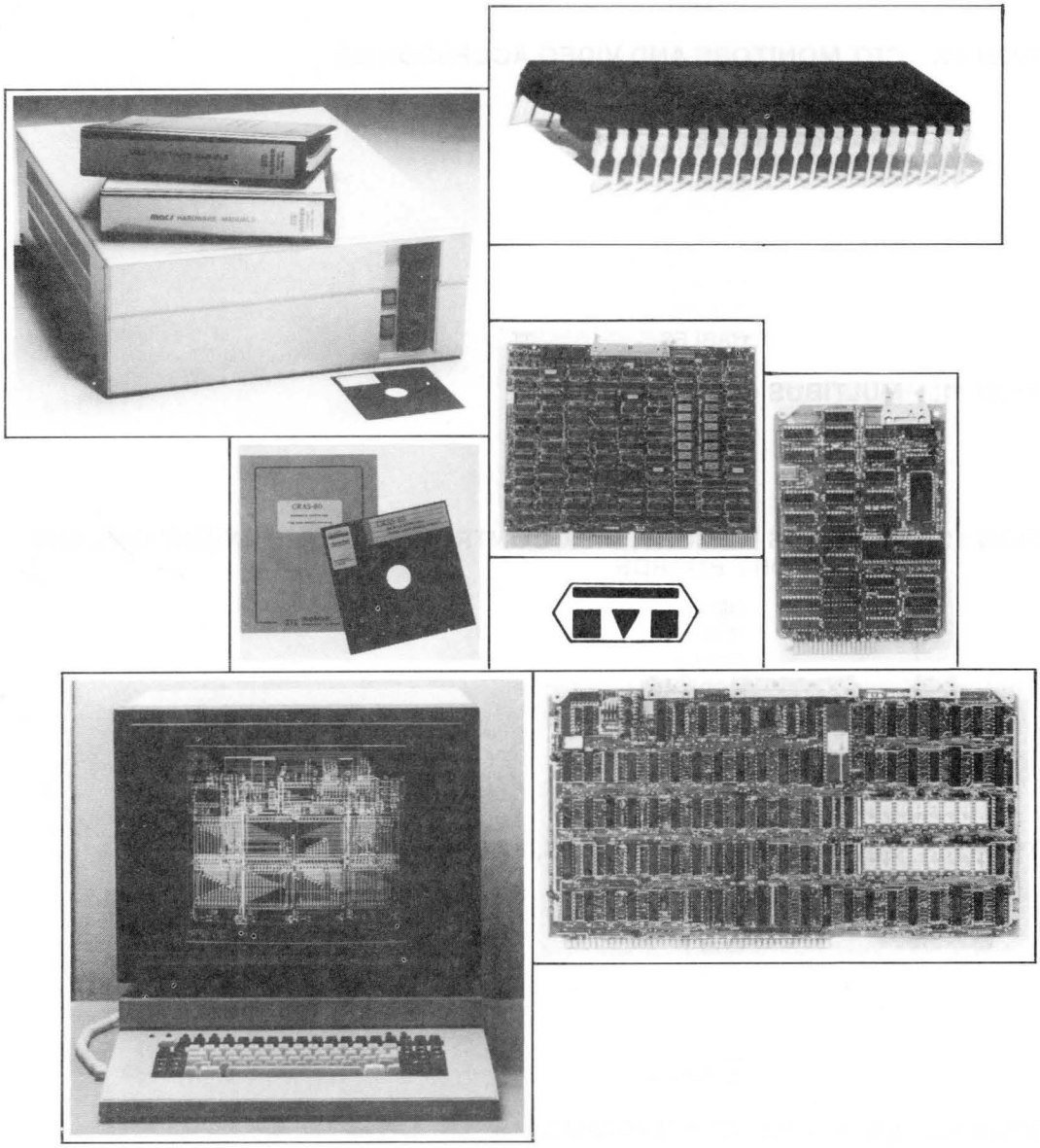
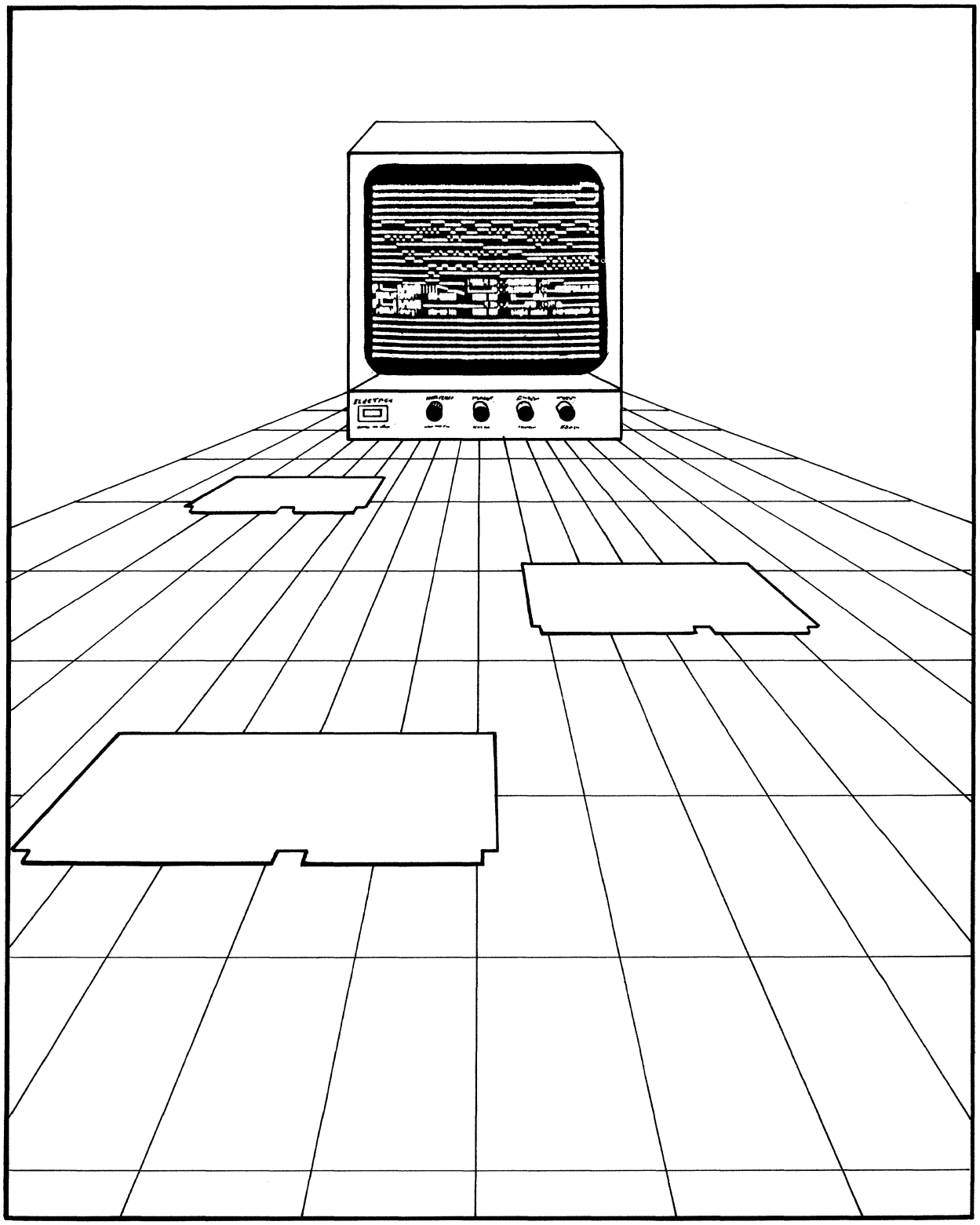




# MULTIBUS VIDEO BOARDS

## SECTION 1 MULTIBUS VIDEO BOARDS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# GXB-1000

## 2K x 2K SUPERHIGH RESOLUTION COLOR GRAPHICS BOARD SYSTEM FOR MULTIBUS

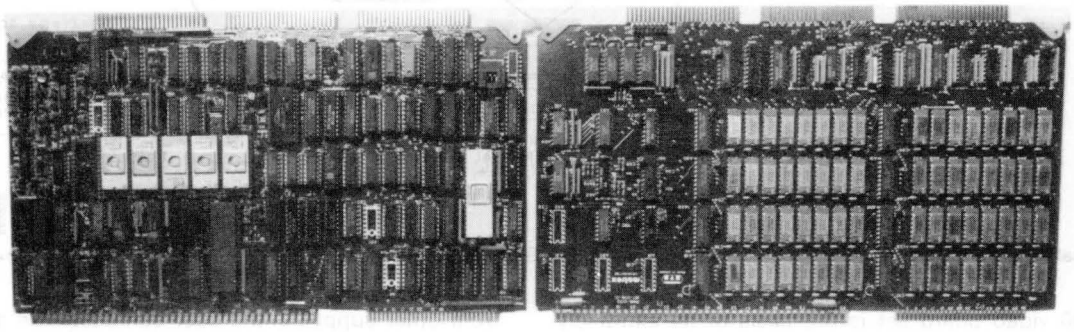


- 2K x 2K read/write area
- 1600 x 1200 and 1024 x 768 display resolution
- 60 Hz noninterlaced/interlaced refresh
- 4, 8, 12, or 16 image planes (bits/pixel)
- Hardware vector generator (800 nsec/pixel)
- 256 color look-up table
- Four pipelined on-board processors
- On-board 16 bit CPU (8088/5MHz)
- 32K byte graphics interpreter
- 2D primitives plus segments
- Flash preset, clear, pan, blink, pixel processor, raster ops, flash load
- Modular design
- Fully Multibus compatible
- Single +5V power supply
- Bus Master or Slave modes

The GXB-1000 is a two board Multibus based graphics system. The GXB-1000 provides the highest performance raster scan color graphics for an extremely low cost. By adding a simple custom software instruction translator in a high level language (C, Pascal, Fortran), the GXB-1000 can be used to build a powerful high resolution color system capable of interpreting any graphics terminal communications protocol. This feature enables the CAD/CAM user to upgrade his existing installation with the GXB-1000 color graphics display controller without changing existing data bases or application software.

Over 6 programmer years of Matrox software effort have gone into the development of the resident graphics interpreter, which recognizes over 256 graphics commands.

The latest state-of-the-art color raster graphics hardware and software are incorporated into the GXB-1000 boards. Advanced features include: 1600 x 1200 resolution, 60 Hz noninterlaced refresh, hardware vector and circle generators (800 nsec/pixel), on-board 16 bit CPU, look-up table, pixel processor, etc. A combination of the highest possible raster display resolution with ultrafast drawing speed yields the top performance required for CAD/CAM applications at the lowest possible cost.



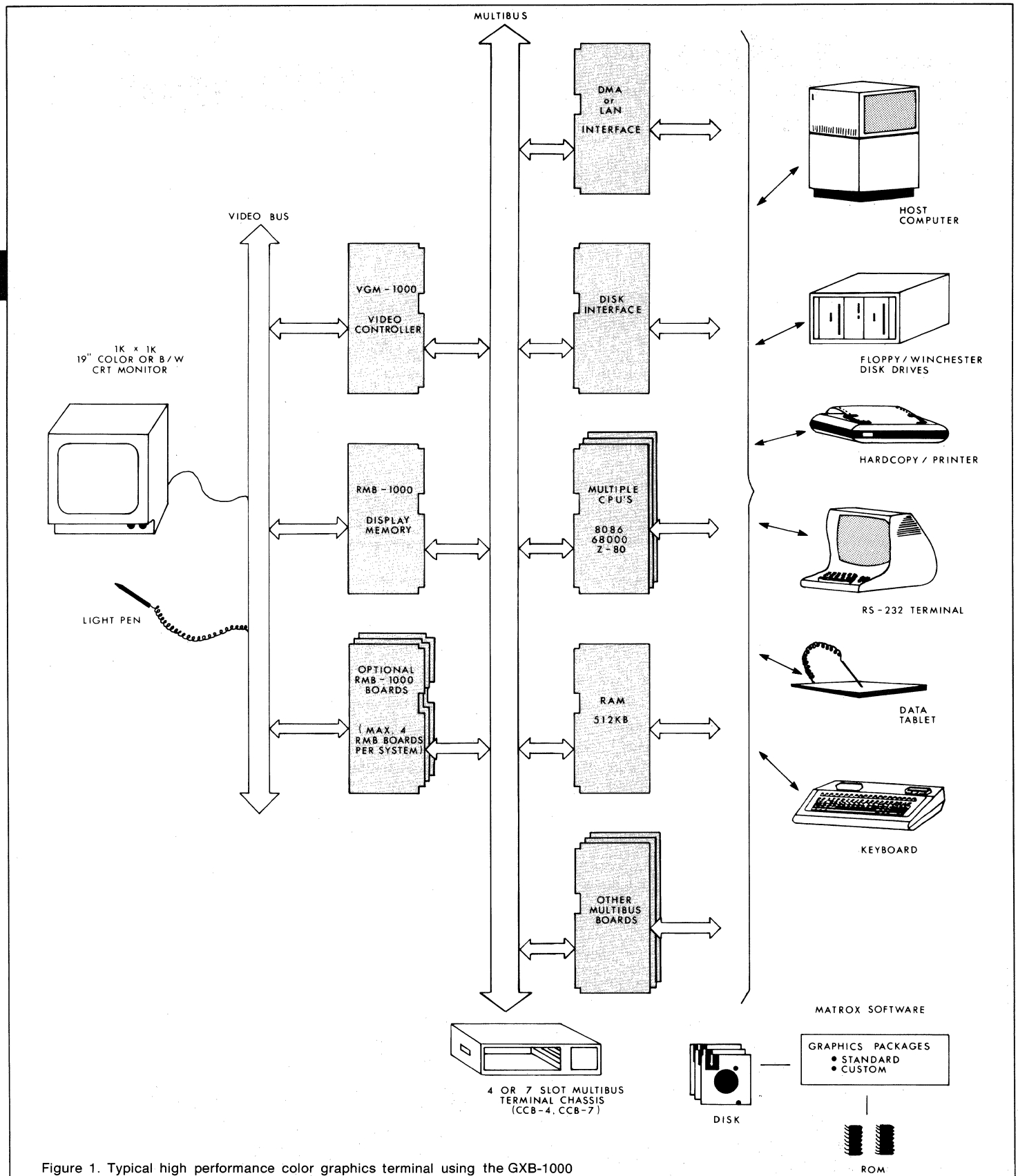



Figure 1. Typical high performance color graphics terminal using the GXB-1000

The GXB-1000 video board set is the basis of an extremely powerful and versatile graphics display system. Using additional boards available off-the-shelf from Matrox such as 8 or 16 bit CPUs (ZBC-80 [Z-80A], MBC-86/12 [8086/87], MRC-68K [68000]), 512K byte RAM (MEGA-4), floppy disk interface (FFD-1), plus DMA, ETHERNET, and other Multibus boards from other suppliers, the user can assemble a high performance graphics system with minimal engineering effort, short development time, and low cost. Matrox supplied graphics software and accessories (CRT monitors, light pen, etc.) enable the OEM user to tailor system performance for a wide range of applications.

# GXB-1000 FEATURES

**Resolution:** 1024 x 768 standard
1600 x 1200 optional
1280 x 1024
1024 x 1024
(other resolutions are user-selectable)

**Bits/Pixel:** 4 bits/pixel standard
8, 12, and 16 bits/pixel optional

**R/W Area:** Read/write memory is 1K x 1K standard
2K x 2K optional

**Refresh Rate:** Noninterlaced or interlaced (50/60 Hz) all resolutions except 1600 x 1200 which is interlaced only.

**Figure Draw Speed:** 800 nsec/pixel min. ("snow")
3.2 μsec/pixel min. (retrace only)
includes vectors, arcs, circles, area fills, and character draws.

**Flash Preset Speed:** 12 nsec/pixel. All pixels (on single or multiple surfaces) are preset to a fixed value in one field (16 msec).

**Slice Draw Speed:** 50 nsec/pixel. 16 pixel horizontal (slices) segments are written in one 800 nsec write cycle. Used in alphanumeric mode for character draws, window clear, fill, marker, etc.

**Flash Load Speed:** 12 nsec/pixel. 16 succesive horizontal pixels in one bit plane are loaded in one 200 nsec memory cycle. Synchronous with the display refresh. Used for high speed load from external sources via Metabus.

**Raster OP Speed:** 6 μsec/pixel for direct raster operations (Bit Blitz) on raster rectangles. 2D transform (translation, rotation, zoom/scale, and reflection) and logic/arithmetic operations between source and destination pixels are supported.

**Preset Mask:** Individual control of each bit plane by plane mask.

**Scroll:** Smooth vertical scroll (by 1 pixel).

**Shift:** Horizontal shift by 4 pixels.

**Pan:** Scroll and Shift can be combined for a smooth two dimensional pan within the 2K x 2K area.

**Look-Up Table:** 256 color look-up table for each 4 bit/pixel surface.

**Overlay Video:** Any bit plane can be used for overlay functions such as blink, alpha, cursors, etc.

**Cursors:** Cross-hair or user-defined cursor for graphics. Underline cursor for alphanumerics and dialog areas.

**Light Pen:** Built-in interface detects the light pen position to one pixel accuracy in 100 msec.

**Video Parameters:** All video parameters including horizontal and vertical syncs, blanks, frequency, and display format are user software programmable.

**Video Outputs:** R,G,B color signals 1Vpp, 75Ω with composite sync on green. Separate video signal connector.

**Multibus Interface:** Memory board takes only +5V power from the Multibus. VGM board fully conforms to Multibus specs.

**Metabus:** The two boards are interconnected via three 50-pin ribbon cables at the top of each board (supplied).

**Pipeline Processors:** Four on-board processors include 16 bit CPU, pixel processor, video ECL processor, and hardware vector generator.

**On-Board CPU:** 5MHz 8088 CPU with 32K of ROM, 4K RAM, and Multibus interface. Interprets off-board display file through on-board ROM interpreter (graphics mode). Can also be used as system CPU executing 8088 code (direct mode).

**Multibus Mode:** On-board CPU executes graphics instructions as either Bus Master or Slave. In Master mode, the 8088 CPU fetches instructions from an off-board RAM display file. In Slave mode, the host transfers the instructions from the display file to the 8088 CPU via an on-board FIFO buffer through an on-board I/O port. Byte by byte or 256 byte block transfers are supported.

**Pixel Processor (PIP):** 100 nsec cycle time processor for processing pixel values. Used for pixel complement, color offset, load, shift, etc. Program for PIP loaded by local 8088 CPU or the user's CPU.

**Video Processor (VIP):** 16 x 8 high speed ECL look-up RAM used for color mapping and video processing. Program for the VIP is loaded by the local 8088 CPU or by the user's CPU.

**Vector Generator:** High speed VLSI graphics processor generates vectors, circles, arcs, rectangles, characters, etc. at 800 nsec/pixel. Program for the graphics generator is loaded by the local 8088 CPU.

## SOFTWARE SUPPORT

**MIG-1 Graphics Package:** Local CPU with resident MIG-1 interpreter recognizes approximately 256 high level graphics commands. Included are various figure draw commands, video effects, pan, clear, control, etc. The MIG-1 interpreter is stored in EPROM and can be accessed either by MACRO commands from a data file or directly by the CPU via a library table. MIG-1 source code is available separately.

## ACCESSORIES

**CRT Monitors:** Matrox supports a full line of 19" color monitors for 1K x 1K resolution displays with noninterlaced or interlaced refresh.

**Light Pen:** High speed ligh pen (LP-600).

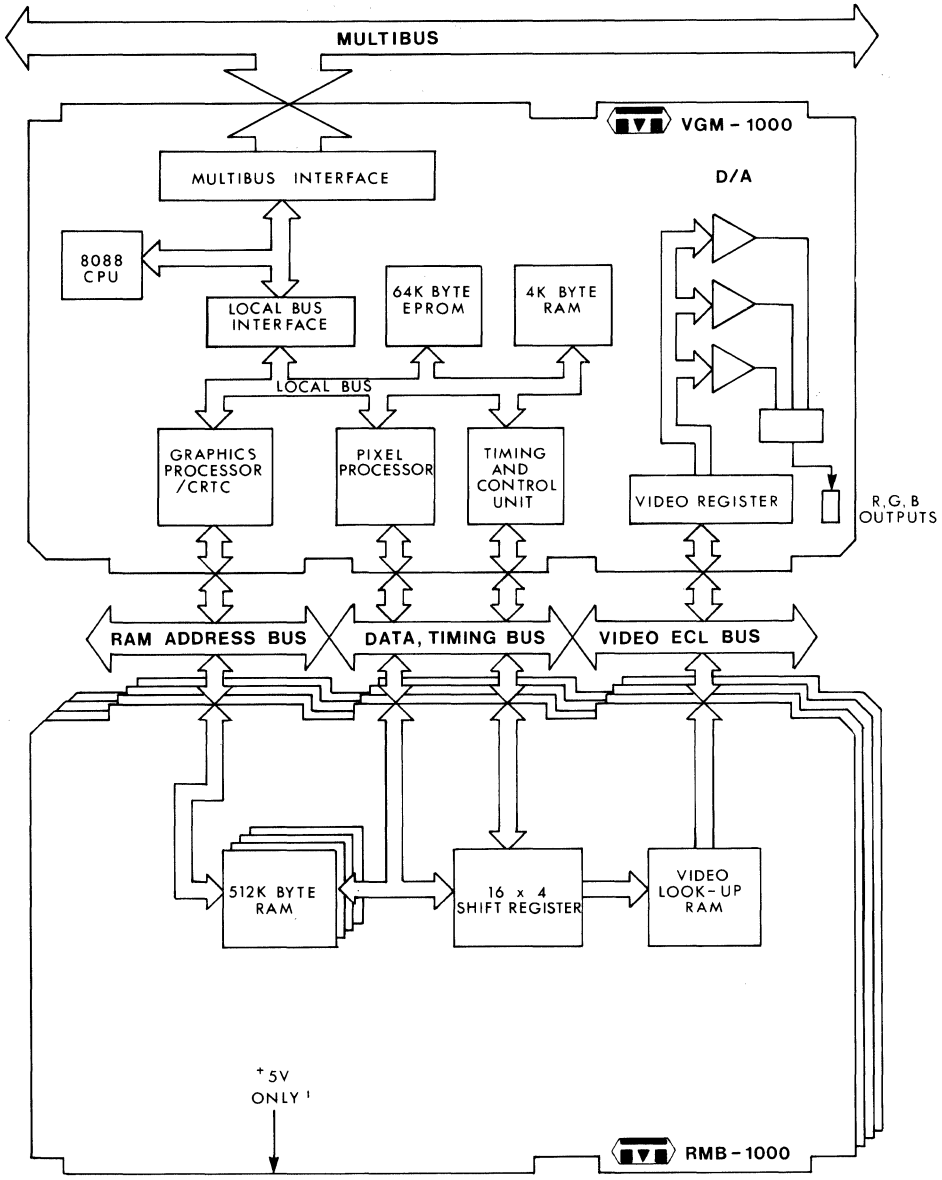



Figure 2. GXB-1000 functional blocks

## FUNCTIONAL DESCRIPTION

The GXB-1000 board set is a complex high speed digital graphics system. By using the latest state-of-the-art VLSI circuits together with high speed ECL logic and advanced software, Matrox can offer the highest performance in color raster graphics. A board level product means lower cost, higher reliability, easier system design, and faster product introduction.

The system consists of two boards; VGM-1000 (Virtual Graphics Machine) and RMB-1000 (Refresh Memory Board). The VGM-1000 generates all of the video timing signals and provides local intelligence with an on-board graphics interpreter executed by an 8088 CPU. The RMB-1000 contains 512K bytes of high speed RAM for four bit plane storage. The memory is organized as 1024 x 1024 x 4 pixels. The system has also been designed to accommodate 256K RAMs. When these parts become available a single RMB-1000 memory board can hold 2M bytes of RAM organized as 2048 x 2048 x 4 pixels.

The VGM-1000 and the RMB-1000 boards are connected via three 50 pin ribbon cables at the top of each board (Metabus). Both boards require only +5V power from the Multibus. The VGM-1000 board appears to the system bus as an 8088 master CPU with full bus arbitration logic.

The user can configure the RMB-1000 memory board for a variety of different display formats and memory configurations through a combination of software programming, jumper changes, and crystal clock changes.

A minimal configuration consists of two boards; one VGM-1000 and one RMB-1000. This system can be structured for any display format within 1 Mega pixels, with each pixel being 4 bits deep. Examples are 1024 x 1024, 1024 x 768, 640 x 480, 800 x 600 landscape and portrait displays.

For displays requiring more bits per pixel (up to 16 bits per pixel) or more resolution (up to 2K x 2K) additional RMB-1000 memory boards can be used. A maximum of four RMB-1000s can be "stacked" together with one VGM-1000. For example, a display of 1600 x 1200 x 4 requires two RMB memory boards configured for serial operation. A display of 1024 x 768 x 16 requires four RMBs configured to operate in parallel.

## VIRTUAL GRAPHICS MACHINE

The GXB-1000 design incorporates the concept of pipelined distributed processors. The four GXB-1000 processors represent the lowest level of the pipeline (as far as the actual picture generation is concerned). The higher level CPU (on-bus or off-bus via a data link) loads a display file containing the picture description (data and instructions) into off-board RAM memory on the Multibus (there can be multiple display files in the off-board RAM). The display file can be up to 16 million bytes long. Multiple display files can also exist anywhere in the 24 bit Multibus address space.

The user can think of the GXB-1000 board set as a graphics processor which executes its own instruction set. The internal CPU together with local resources (ROM, RAM, graphics processor, VIP, PIP, refresh memory, etc.) can be thought of as a single graphics CPU with microcode stored in on-board ROM. A particular graphics instruction is performed by executing microcode (actually 8088 machine language).

The display file containing the graphics instructions can be interpreted by the VGM in either Multibus Master or Slave mode (selected by jumper).

In the Master mode, the host computer has to transfer only the starting address of the display file to the VGM's I/O Command Input Port (3 byte transfer). The host then issues a Run Display File (CONTINUE) command, after which the VGM fetches successive bytes starting from the starting address by becoming the Bus Master for every fetch.

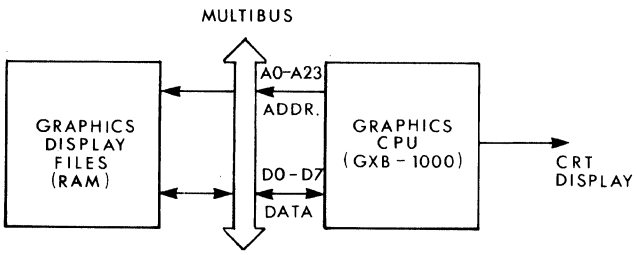



Figure 3. GXB-1000 Bus Master mode configuration.

In the Slave mode, the host must transfer every byte from the display file to the VGM's internal FIFO buffer via the Command Input Port. Up to 256 bytes of the display file commands can be stored in the buffer. Commands can be loaded sequentially or in a single 256 byte block transfer. At the end of a transfer, the VGM's 8088 CPU will fetch instructions from the FIFO buffer until the buffer is empty. At that time the VGM will issue an interrupt to the host. The Slave mode is used for Multibus systems that do not support multimasters.

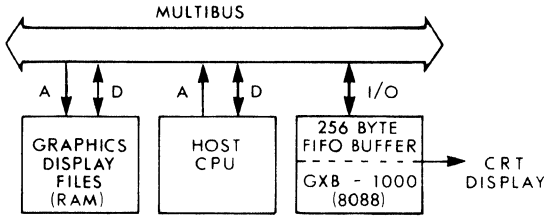



Figure 4. GXB-1000 Bus Slave mode configuration.

The local CPU executes instructions using on-board resources; vector generator, VIP, and PIP. The instruction execution time varies from slow (milliseconds) for long vectors, clear screen, area fills, etc. to very fast (nanoseconds) for control instructions. During execution the Multibus is not used, thereby freeing it for higher level CPU communications. After execution of the complete display file, the local CPU (8088) sends an interrupt signal to the host, notifying it that the display file has been finished. Alternately, multiple display files can be linked so that at the completion of one file the on-board 8088 will jump to the beginning of the next file. Nesting of display files is also supported.

The same byte (fetched from off-board RAM or internal FIFO buffer) can be interpreted by the 8088 as either 8088 instruction opcode or as graphics instruction opcode. The mode is determined by executing the instructions "Switch to Graphics Mode" or "Switch to 8088 Mode". This feature enables the programmer to combine the full 8088 instruction set (at full speed) with Matrox graphics instructions, in the same or different files.

## TYPICAL APPLICATIONS

The GXB-1000 graphics board set is a powerful video display driver that represents the state of the art in raster graphics equipment. The Matrox building block approach to both hardware and software allows the system designer to implement a new graphics terminal, or emulate an existing terminal, with considerable savings in development effort, cost, and time.

By writing the terminal's high level graphics software in a high level language (C, Fortan, Pascal), executed by the in-bus user CPU, any graphics terminal can be designed (Matrox offers both 8086/87 or 68000 based Multibus CPU cards as in-bus host processors). The Matrox graphics commands are treated as user macrocommands and are defined as such to the user's high level language assembler. The programmer does not have to be concerned with the display hardware, and can therefore write high level terminal programs on the CPU of his choice to generate display files. These display files are in turn executed by the Virtual

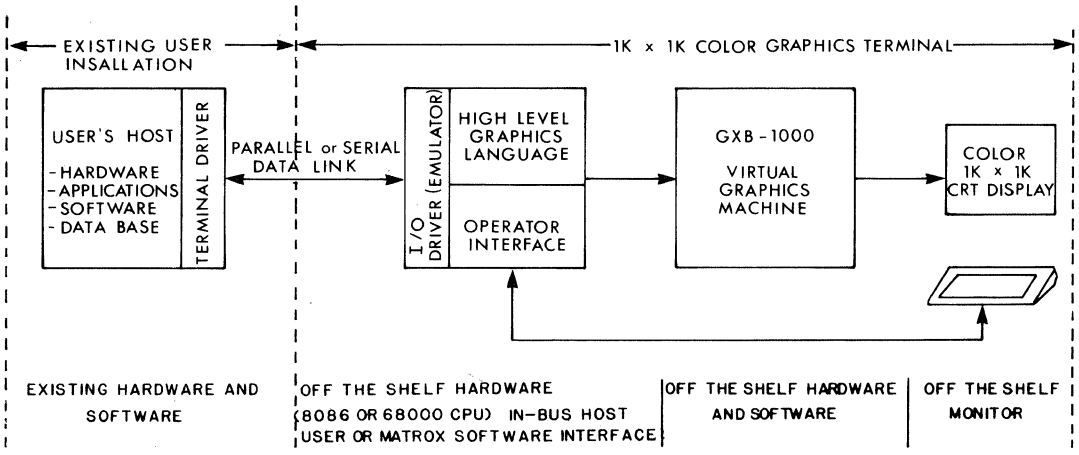



Figure 5. 1K x 1K color graphics terminal implementation.

Graphics Machine in a pipelined fashion, providing the high throughput required for interactive graphics.

This approach significantly simplifies the design of a graphics terminal and enables the user to construct a custom terminal or emulate and upgrade any existing terminal in the shortest possible time. All of the existing user application software and hardware can be used without any change.

As an example of this philosophy, Matrox has developed a Tektronix 4113 emulator software package in "C" which runs on the Matrox MBC-86/12 (8086/87) Multibus CPU board. The package uses a real-time kernel, written in "C", which supports multitasking.

The software is available in "C" source code for the user wanting to add special functions.

## USER MODEL OF THE GXB-1000

The GXB-1000 display appears to the user as a series of 4 plane read/write surfaces. One RMB board represents a single 1K x 1K x 4 bit surface. Up to four RMB boards can be combined serially to provide a larger surface (2K x 2K x 4 bits), or, they can be combined in parallel to provide up to four 1K x 1K x 4 surfaces.

Two bytes are required to define a unique X address, and two bytes are required to define a unique Y address within a read/write surface (64K x 64K addressable area). The graphics interpreter uses only the first 11 address bits (2K x 2K read/write area) and ignores the upper five bits (wrap-around). The actual displayed area may be less than the full read/write area (i.e. 1024 x 768 display area). The display area can be panned to any position within the read/write area.

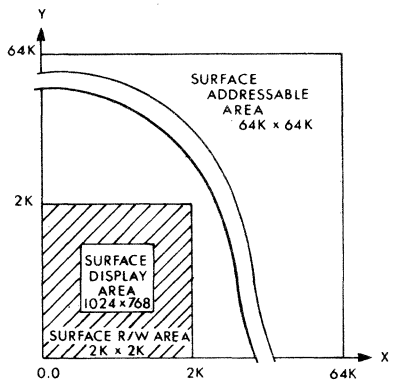



Figure 6. Surface addressable, read/write, and display area definitions.

Each surface can be organized into subsurfaces, with each subsurface consisting of one to four planes. The number of planes used for each subsurface determines the maximum number of colors that can be displayed by that subsurface. Up to 16 one-plane subsurfaces can be defined if four RMB boards are used.

Every surface has its own color look-up table (LUT). As each pixel is displayed, its color index (the four bit binary value stored in the display memory) addresses one of sixteen positions in the look-up table. The output from the look-up table is an 8-bit binary number which, after D/A conversion, defines one of 256 possible display colors. When more than one display surface is used the outputs of the look-up tables can be combined in a "logical OR" or a priority manner (figure 6).

Each subsurface produces its own graphics image. These various images are combined to create a single display, according to the user's overlay and priority commands; "Surface Video Combination", "Set Surface Priority", "Set Surface Visibility", etc. (see GRAPHICS INSTRUCTION SET). If a given subsurface uses a transparent background the next lower priority subsurface will be seen. If, on the other hand, the background is opaque, all other lower priority subsurfaces will be hidden.

Once a subsurface has been specified, the graphics processor can draw various figures, patterns, or characters. The primitives include: point, vector, arc, circle, marker, rectangle, polygon, filled window, and filled character cell. Figures and figure attributes (thickness, texture, addressing and data modes, etc.) are specified by the figure drawing instructions.

There are three possible drawing speeds selectable by the user (Set Drawing Speed instruction). The highest speed is 64 clock cycles per pixel (800 nsec with an 80 MHz clock, or 1.25 million pixels/sec). However, in this mode the display is blanked when accessed by the graphics processor resulting in a "snow" effect on the screen. If the drawing is limited to the retrace period only (i.e. when the display is blanked), to avoid "snow" on the screen, the resulting drawing speed is 3.2 μsec/pixel or over 300,000 pixels/sec. The third speed, obtained by using a wider display blanking signal, is 1.2 μsec/pixel or 830,000 pixels/sec. The user can switch at any time between these drawing speeds depending on the desired effect and the amount of data to be drawn.

A complete surface can be preset to any color by a hardware flash preset command which loads each pixel in the surface at 12.5 nsec/pixel or one field for the complete surface (16 million pixels in 16.6 msec).

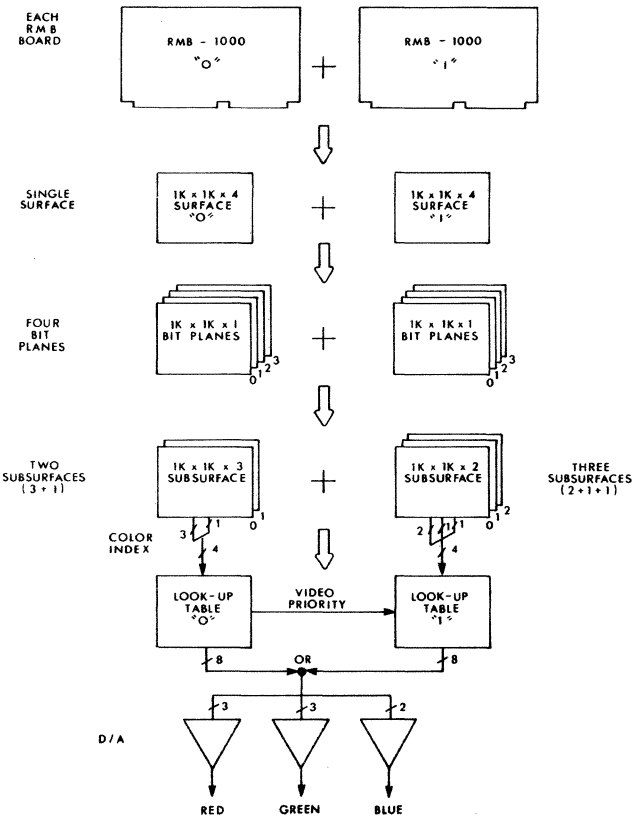



Figure 7. Five subsurface/two surface display example.

In the Alphanumerics display mode, the GXB-1000 works as a color alphanumerics terminal, supporting commands such as carriage return, line feed, back space, etc. Either the full screen or up to four rectangular display areas (Dialog Areas) can be specified for writing text. Alphanumerics Mode and Dialog Area instructions are used for text manipulation.

Any 1-bit subsurface on each surface can be designated for pixel blink control. Setting the pixel bit "on" will result in an on/off blink rate of 4 Hz for all the pixels with the same X,Y address on the same surface. A designated subsurface can also be used as an overlay plane, a graphics cursor plane, or an alphanumerics plane.

## GRAPHICS INSTRUCTION SET

The instruction set has been organized into 10 different functional groups:

1. Flow Control Instructions
2. Context Switching Instructions
3. Configuration and Initialization Instructions
4. Command Instructions
5. Direct Raster Instructions (Raster Op)
6. Figure Drawing Instructions
7. Alphanumeric Terminal Mode Instructions
8. Dialog Area Instructions
9. Miscellaneous Instructions
10. Input Function Support Instructions

The execution times shown in the following tables apply only to the "worst case" mode, where only one instruction is executed at a time. Normally execution times are much shorter (approaching zero) due to the pipelined architechture of the GXB-1000. For example, when drawing polygons, the execution time is a function of the pixel drawing speed only, since the graphics processor and the 8088 CPU operate in the pipelined fashion; i.e. one draws the vector while the other calculates the parameters for the next vector.
The instruction set shown is a superset of all available instructions for the virtual graphics machine. Actual versions of available MIG-XX interpreters execute a subset of the GXB-1000 superset, since not all users require all the instructions. For information on the MIG-XX implementations currently available, consult the factory.

**Flow Control Instructions** — These instructions are used for various housekeeping functions related to the display file and program flow control.

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Go To | 4 | 100 | Loads graphics program counter with address of next instruction (24 bits). |
| Go Sub | 4 | 100 | Loads graphics program counter with address of next instruction and stores the current PC on the stack. |
| Return | 1 | 100 | Return to main program from the subroutine. |
| Stop | 1 | 60 | Stops program execution requires an I/O command to restart. |
| NOP | 1 | 100 | Dummy instruction. No operation. |
| Idle | 1 | 50 | Wait loop, 8088 fetches the same instruction byte, looping conditional on code change. |
| Reset | 1 | 50,000 | Resets and initializes all local resources after executing self-test. |
| Load Status | 1 | 100 | Loads current status of local resources (stored in VGM RAM) to shared buffer. |
| Interrupt | 1 | 60 | Sends interrupt to Host CPU. |
| Fetch Single/Page | 2 | 60 | Sets subsequent fetches from file as single byte or 256 bytes (stored in cache). |

Table 1. Flow Control Instructions.

**Context Switching Instructions** — Data fetched from the display file can be interpreted as direct 8088 op code, or as graphics op code. After a power-up or reset, the VGM defaults to "native 8088 mode". In this mode all instructions are interpreted as 8088 commands. The user can operate in this mode, or can select the "graphics interpreter mode" by executing a CALL instruction to the starting address of the on-board graphics interpreter (switch to graphics mode). The 8088 then interprets all op codes as graphics instructions. When operating in the graphics mode, an instruction is provided to return to the native 8088 mode (Switch to 8088 Mode).

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Switch to 8088 Mode | 5 | 120 | Disengages the graphics interpreter (display file). |
| Switch to Graphics Mode | 5 | 120 | Engages the graphics interpreter. |

Table 2. Command Instructions.

**Configuration and Initializing Instructions** — This group of instructions defines and initializes display parameters such as; number of horizontal and vertical pixels, drawing speed, pan, syncs, blanking, and refresh rate.

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Set Video Format | 2 | 100 | Selects standard video display formats: 1024 x 768, 1024 x 1024, 1600 x 1200. |
| Set Drawing Speed | 2 | 100 | Selects drawing in retrace only (4 μsec/pixel), all the time (800 nsec/pixel), or 50% video (1.2 μsec/pixel). |
| Pan Display | 5 | 100 | Positions display within 2K x 2K area. |
| Surfaces Video Combination | 2 | 100 | Define combination function for multiple surfaces (visibility, priority/OR overlay). |
| Select Surface | 2 | 100 | Selects one of four surfaces for read/write operations. |
| Subsurface Priority Set | 2 | 400 | Define overlay function for multiple subsurfaces on a surface (priority/OR overlay). |
| Select Subsurface | 2 | 400 | Select one of several subsurfaces on a surface for read/write operations. |
| Define Subsurfaces | 2 | 400 | Defines one to four subsurfaces on a four plane surface. |
| Set Subsurface Color | 2 | 400 | Defines foreground color for subsurface write operations. |
| Set Subsurface Combination | 2 | 400 | Defines background color and combined subsurface display color. |
| Set Subsurface Visibility | 2 | 400 | Enables/disables subsurface visibility. |
| Load Surface LUT Directly | 17 | 200 | Loads 16 byte Look-Up Table directly. |
| Load Surface UCS Start Address | 5 | 100 | Loads start address of user character set file (file = 256 x 16 x 16 = 8K bytes). |
| Load Shared Buffer Start Address | 5 | 100 | Loads off-board RAM buffer start address (8 bytes long). |
| Define Video | 9 | 200 | Defines special video display formats (sync, blanks, no. of lines, etc.). |

Table 3. Configuration and Initializing Instructions.

**Commands** — This group of instructions provide the highest priority control of the on-board 8088 by the host. These are the only instructions that are transfered directly to the I/O port on the VGM-1000 board, and are not fetched from external Multibus RAM (Master mode). The I/O port address is hardware selectable by the user.

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Load Start Address | 4 | 200 | Loads internal graphics 24-bit program counter (start address of display file in Multibus RAM). |
| Reset | 1 | 50,000 | Resets and initializes all local resources after executing self-test. |
| Load Status | 4 | 200 | Load current status of local resources (stored in VGM RAM) to Multibus memory. |
| Stop | 1 | 100 | Suspends all 8088 operations, no Multibus access. |
| Continue | 1 | 100 | Resumes program execution after a stop command. |

Table 4. Context Switching Instructions.

**Direct Raster Instructions** — This group of instructions works directly on a rectangular area of the raster. Both run length and bit by bit encoding can be used. Execution speed is a function of the number of pixels in the rectangle, N, and the pixel op speed (3 μsec/pixel).

The instructions; Read Back Raster, Write to Raster, and Set Data Packing Mode, are used for the transfer of raster data to/from off-board RAM.

The Raster Operations work on pixels inside a specified raster rectangle. First a 2D transformation is performed on each "source" pixel, then each transformed pixel is combined with the corresponding pixel at the new destination on the same or different subsurface.

The available 2D transforms and raster operations are described below:

Source/Destination Raster Rectangle — Defines size, initial X/Y position, and destination subsurface of the raster rectangle on the current subsurface.

2D Transform Parameters — Defines the 2D transformation performed on each source pixel before combination with the destination pixel.

- Translation — X, Y translation offset for each pixel.
- Rotation — Rotates each source pixel about the Z-axis with the lower left corner of the rectangle at the origin (8 angles in multiples of 45°).
- Zoom/Scale — Source raster is multiplied by 1, 2, 4, or 8 (zoom by pixel replication) or divided by 1, 2, 4, or 8 (scaling by pseudo random dither sampling).
- Reflection — Source raster can be reflected about any one of four axes (X, Y, Y = X, Y = −X).

Raster Operations — After the 2D transformation, the source raster is combined with the destination raster pixel by pixel. Source pixels can be complemented before the operation. Logic operation (AND, OR, X−OR), arithmetic operations (ADD, SUBTRACT), copy and user-defined pixel functions can also be specified. Operations with a constant are also supported.

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Read Back Raster | 13 | 100 + NX3 | Reads raster rectangle to off-board RAM. |
| Write to Raster | 13 | 100 + NX3 | Write raster rectangle from off-board RAM. |
| Set Data Packing Mode | 2 | 100 | Defines data packing; bit x bit, run length. |
| Raster Op | 14 | 100 + 2NX3 | Moves raster rectangle from one screen location to another with operation. |

Table 5. Direct Raster Instructions.

**Figure Drawing Instructions** — The VGM-1000 draws graphics primitives at a rate of 800 nsec/pixel. The nine primitives include line draw commands (point, vector, arc, circle, marker, rectangle, and polygon) and area draw commands (window and character cell). Several attributes are associated with each figure to be drawn:

Texture — Write/skip pixel pattern (16 x 1 bit). Used to define texture of a line primitive.

Fill Pattern — Write/skip pixel pattern (8 x 8 bits). Used to define the fill pattern of an area primitive.

Thickness — Defines the "pen size" to be used in line drawing operations: 1 x 1 pixels, 2 x 2 pixels, 3 x 3 pixels, up to 16 x 16 pixels.

Chain — Specifies the number of times the figure is to be drawn in succession.

Addressing — The coordinates can be specified in one of three ways:

- Absolute — 2 bytes for each X,Y coordinate. range = 0 — 65,535
- Relative — 2 bytes for each coordinate relative to the cursor. range = ±32,767
- Short Relative — 1 byte for each coordinate relative to the cursor. range = ±127

PIP Function — Specifies the pixel data to be written to the addressed pixel. Five possible functions can be defined:

- Complement Pixel — complements each pixel bit
- Color Index — defines 1 of 16 colors
- Offset to Index — reads value and offsets by 0 — 15
- User PIP Function — user defined truth table used for pixel transformation
- Chromakey Switch — used for user defined chromakey outline fill or hardware clipping (used only with window command).

The texture, fill pattern, thickness, and PIP are each selected through separate explicit instructions. The figure, chain, and addressing mode are selected implicitly by the figure draw instruction op code.

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Set Texture | 3 | 100 | Loads 16 bit write/skip pixel pattern. |
| Set Fill Pattern | 9 | 200 | Loads 8 x 8 bit fill pattern (organized as 8 bytes). |
| Set Thickness | 2 | 100 | Selects 1 of 16 pen sizes from 1 x 1 to 16 x 16. |
| Set Chromakey Index | 2 | 100 | Selects chromakey index 0-15 for fill and clip functions. |
| Select PIP Function | 2 | 100 | Selects 1 of 5 PIP functions (complement, color, offset, chromakey, user). |
| Load User PIP | 9 | 100 | Loads user PIP, pixel in/pixel out table — 16 x 4 organized as 8 bytes. |
| Select Marker | 2 | 100 | Selects 1 of 16 Matrox defined markers. |
| Select User Marker | 4 | 100 | Selects user defined 8 x 8 bit marker located in Multibus RAM. |
| Move (A,R,SR) | 5 | 100 | Moves current position (absolute, relative, or short relative). |
| Point (A,R,SR) | 3 | 100 | Draws point. |
| Vector (A,R,SR) | 3 | 100 + P.8 | Draws vector from current position to endpoint. |
| Arc | 3 | 100 + Px.8 | Draws an arc from point A to Point B with center at current position. |
| Circle | 2 | 100 + 2πRx.8 | Draws a circle of radius R with center at current position. |
| Marker (A,R,SR) | 2 | 100 + MxPx.8 | Draws a marker at current position (dimensions = MxP). |
| Polygon | 4 + 2N | 100 + NxPx.8 | Draws polygon (closed vector chain). |
| Rectangle | 4 | 100 + 4Px.8 | Draws rectangle (outline only) from current position. |
| Window | 4 | 100 + MxPx.8 | Draws rectangle (filled) from current position (dimensions = M x P). |
| Character Cell | 2 | 200 | Draws 8 x 8 filled character cell from current position. |

Table 6. Figure Drawing Instructions.

Note — Bytes and Execution times shown in Table 6 reflect a 1 x 1 pen size and short relative addressing.

**Alphanumeric Terminal Mode Instructions** — In this mode, the GXB-1000 becomes a full screen color alphanumeric terminal. The user can select a character cell size of 8 x 8 or 16 x 16 pixels. The character generator can use either the standard ASCII set (stored in EPROM) or a user defined set (stored in Multibus RAM). The display format is determined by the number of pixels in the X and Y directions.

$$\text{Number of Characters/Line} = \frac{\text{no. of X pixels}}{\text{character X size}} \quad \text{i.e. } \frac{1024}{8} = 128$$

$$\text{Number of Lines/Display} = \frac{\text{no. of Y pixels}}{\text{character Y size}} \quad \text{i.e. } \frac{768}{8} = 96$$

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Enable ATM | 1 | 100 | Enable alphanumeric terminal mode. |
| Define Alpha Mode | 2 | 100 | Defines character size, character generator, format, etc. |
| Define Alpha Surface/ Subsurface | 2 | 100 | Defines surface/subsurface to be used for alpha-numerics. |
| Define Character Color | 3 | 100 | Defines character foreground and background color. |
| Set AT Cursor Position | 3 | 100 | Positions alpha cursor. |
| Enable AT Cursor | 1 | 100 | Enable/disable cursor visibility. |
| Clear Screen | 1 | 16000 | Clears screen and positions cursor to home. |
| Clear to End of Line | 1 | 1000 | Clear to end of line. |
| Character | 2 | 1000 | Draws one character. |
| Character N | 1 + N | Nx1000 | Draws N characters (up to 256 characters). |
| Character Many | 2 + M + 1 | Mx1000 | Draws a string of characters until an SA instruction is received. |
| SA (Stop Alpha) | 1 | 100 | Alpha string terminator. |
| CR | 1 | 100 | Carriage return. Positions cursor to left margin. |
| LF | 1 | 100 | Line Feed. Moves cursor down one line. |
| BS | 1 | 100 | Backspace. Moves cursor left one space. |
| HT | 1 | 100 | Horizontal tab. Moves cursor right one space. |
| VT | 1 | 100 | Vertical Tab. Moves cursor up one line. |

Table 7. Alphanumeric Terminal Mode Instructions.

**Dialog Area Instructions** — A dialog area is a rectangular region of the screen used to display text. Up to four dialog areas of different sizes can be defined on the screen. Instructions for dialog areas are similar to the Alphanumeric Terminal Mode Instructions and use the same character sets and sizes. The number of lines in a dialog area is determined by the number of X and Y pixels and the character size. For example, in a 300 x 200 dialog area using 16 x 16 characters:

$$\text{Number of Characters/Line} = \frac{300}{16} \rightarrow 18$$

$$\text{Number of Lines} = \frac{200}{16} \rightarrow 12$$

The characters are positioned on multiples of 8 or 16 in the X and Y directions. Note that in a dialog area, when the window is complete, the cursor moves to the start position (page mode) whereas in Alpha Terminal Mode the display is moved up one line and the cursor goes to the new bottom line (scroll mode).

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Select Dialog Area | 2 | 100 | Enable/disables one of four dialog areas. |
| Define DA | 6 | 200 | Defines dialog area, size and position. |
| Define DA Character Set | 2 | 100 | Defines character size and font. |
| Define DA Character Color | 3 | 100 | Defines character foreground and background colors. |
| Set DA Cursor Position | 3 | 100 | Positions DA cursor. |
| Enable DA Cursor | 1 | 100 | Enables/disables DA cursor visibility. |
| Clear DA | 1 | MxNx300 | Clear dialog area. (M x N pixels). |
| Clear to End of DA Line | 1 | 1000 | Clear to end of line. |
| DA Character | 2 | 1000 | Draws one character in dialog area. |
| DA Character N | 2 + N | Nx1000 | Draws N characters in dialog area (up to 256). |
| DA Character Many | 2 + M + 1 | Mx1000 | Draws character string until SA instruction is received. |
| SA (Stop Alpha) | 1 | 100 | Alpha string terminator. |
| CR | 1 | 100 | Carriage Return. Moves cursor to left of DA line. |
| LF | 1 | 100 | Line Feed. Moves cursor down one line. |
| BS | 1 | 100 | Backspace. Moves cursor left one space. |
| HT | 1 | 100 | Horizontal Tab. Moves cursor right one space. |
| VT | 1 | 100 | Vertical Tab. Moves cursor up one line. |

Table 8. Dialog Area Instructions.

The characters are positioned on multiples of 8 or 16 in the X and Y directions. Note that in a dialog area, when the window is complete, the cursor moves to the start position (page mode) whereas in Alpha Terminal Mode the display is moved up one line and the cursor goes to the new bottom line (scroll mode).

**Miscellaneous Instructions** — These instructions include surface blink, highlight, preset, and light pen.

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Surface Hardware Blink | 1 | 100 | Enables/disables surface hardware blink (on/off 4 Hz). |
| Surface Software Blink | 1 | 100 | Enables/disables surface software blink (on/off any frequency). |
| Subroutine Highlight | 1 | 100 | Enables/disables subroutine highlight (complements subroutine once/second). |
| Flash Surface Preset | 4 | 16000 | Presets to an affixed color, the entire screen or any rectangular display area, on one surface. |
| Light Pen | 1 | 32000 | Loads the light pen address to the Multibus shared buffer. |
| Blank/Enable Display | 1 | 100 | Blanks (disables)/enables the entire display |

Table 9. Miscellaneous Instructions.

**Input Function Support Instructions** — These instructions generate various graphics cursors and video effects. The user can define a special graphics cursor, stored as a subroutine, which is then used for all graphics cursor operations. Multiple cursors can be defined, but only one is active at a time. The default cursor is a ¼ screen crosshair shown at the cursor position (complement).

| INSTRUCTION | # BYTES | EXECUTION TIME (μs) | DESCRIPTION |
|---|---|---|---|
| Define Graphics Cursor | 4 | 100 | Defines starting address of the display file (subroutine) describing the user's cursor. |
| Define GC Surface | 2 | 100 | Define graphics cursor surface and subsurface. |
| Start Track GC | 5 | — | Positions and displays graphics cursor at X, Y. |
| Track to GC | 5 | — | Moves cursor to new X, Y, displays it, and erases old GC (complement). |
| End Track GC | 1 | — | Sets GC invisible. |
| Start Ink GC | 5 | — | Positions cursor to X, Y, displays GC, and enables ink mode color. |
| Ink to GC | 5 | — | Moves GC to new X, Y, inks trail of movement with color. |
| End Ink GC | 1 | — | Disables ink mode and sets cursor invisible. |
| Start Rubber Band | 5 | — | Positions and displays GC at X, Y and enables "rubber band" mode. |
| Rubber Band to GC | 5 | — | Moves cursor to new X, Y and draws a line from old to new position. |
| End Rubber Band | 2 | — | Disables rubber band mode and sets cursor invisible. |

Table 10. Input Function Support Instructions.

# SPECIFICATIONS

## FUNCTIONAL

## DISPLAY PARAMETERS

| NO. OF RMB BOARDS/SYSTEM | MAXIMUM RESOLUTION |
|---|---|
| 1 | 1K x 1K x 4 |
| 2 | 1K x 1K x 8 or 1600 x 1200 x 4 |
| 3 | 1K x 1K x 12 |
| 4 | 1K x 1K x 16 or 1600 x 1200 x 8 |

## VIDEO TIMING

Display formats and video timing parameters are user software programmable. For a format of 1024 x 768, on a Mitsubishi 8912 monitor, using a 68 MHz crystal, the following timing parameters are programmed:

| SIGNAL | VALUE |
|---|---|
| Active Video | 15.06 $\mu$s |
| Horizontal Sync Frequency | 44.27 KHz |
| Horizontal Sync Width | 1.88 $\mu$s |
| Vertical Sync Frequency | 55.34 Hz |
| Vertical Sync Width | 67.76 $\mu$s |

## INPUT SIGNALS

Light-pen Enable
Light-pen Strobe

## OUTPUT SIGNALS

Red Drive
Blue Drive
Green Drive with composite sync. (Grey Scale Drive)

## BUS INTERFACE

### MULTIBUS

Data, address, and control lines conform to the Intel Multibus Specification No. 9800683 and the IEEE-796 Multibus specification.
Command Input Port — Selectable on any I/O address location 0000 — FFFF

### METABUS (Special Applications)

The three 50-pin buses at the top of each board include: an ECL Video Bus, and Data and Timing Buses for direct access to the refresh RAM. These buses are transparent to the user in normal mode application.

The Metabus can be used for special applications such as: larger color selection look-up RAM (16 million colors), multidisplay/multiuser configurations (one VGM-1000 driving multiple RMB-1000's for up to four different display stations or users), high speed display RAM transparent load (12 nsec/pixel) without tying up the Multibus (used for image dump using high resolution cameras), etc.

For large quantity (100 and up) OEM users, requiring these or similar hardware features, Matrox will design additional custom Multibus boards or will supply all technical information required for the user's own design (subject to certain restrictions — consult the factory).

## CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1 : 86 pin edge connector, 0.156" centers | — Multibus Interface | COMPAR ESM-43-DSRI |
| J1 : 10 pin right angle header, | — R,G,B Video Output | AMP 87922-1 |
| J2 : 10 pin right angle header, | — Light Pen interface | AMP 87922-1 |
| J3 : 50 pin edge connector, 0.1" centers<br>J4 : 50 pin edge connector, 0.1" centers<br>J5 : 50 pin edge connector, 0.1" centres | — Metabus Interface | WINCHESTER 53-50-0<br>(3 required) |

## PHYSICAL

### SIZE

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)

### POWER REQUIREMENTS

VGM-1000 — +5V DC ±5% @ 4.5A
RMB-1000 — +5V DC ±5% @ 3.5A

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0° — 50°C
Relative Humidity: 0 — 95% (non-condensing)

## ORDERING INFORMATION

The standard GXB-1000 consists of two Multibus boards; one VGM-1000 and one RMB-1000. The VGM-1000 board includes the MIG-1 graphics interpreter firmware which executes all of the commands listed in this data sheet. The RMB-1000 board contains 512K bytes of video memory organized as a 1024 x 1024 x 4 bit frame buffer.

| | |
|---|---|
| GXB-1000 | Complete two board graphics controller |

## RESOLUTION/REFRESH RATE AVAILABILITY

| RESOLUTION / REFRESH | 640 x 480 | 1024 x 768 | 1280 x 1024 |
|---|---|---|---|
| 25 Hz | – | X | X |
| 30 Hz | – | X | X |
| 50 Hz | X | X | – |
| 60 Hz | X | X | – |

Note 1: Since the 1280 x 1024 format exceeds the 1K x 1K memory stored on a single RMB, two RMB boards are required for each four bit surface.
Note 2: For refresh rates or resolutions not covered by the above table (i.e. 1600 x 1200) please consult the factory.

## OPTIONS

### Video Memory

| | |
|---|---|
| GXRMB-01 | Adds a second refresh memory board (RMB-1000) for more video planes, or a larger read/write area. |
| GXRMB-02 | Adds two additional refresh memory boards. |
| GXRMB-03 | Adds three additional refresh memory boards. |

### Monitors

| | |
|---|---|
| MCM-1000L | Adds a high resolution 19" RGB color monitor (supports all resolutions except 1024 x 768 @ 50/60 Hz). |
| MCM-1014L | Adds a high resolution 14" RGB color monitor (supports all resolutions except 1024 x 768 @ 50/60 Hz). |
| MCM-2000L | Adds a high bandwidth high resolution 19" RGB color monitor (supports 1024 x 768 @ 50/60 Hz). |

matrox
electronic systems ltd.

*5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA*
*TEL.: 514—735-1182* *TELEX: 05-825651*

# RGB-GRAPH

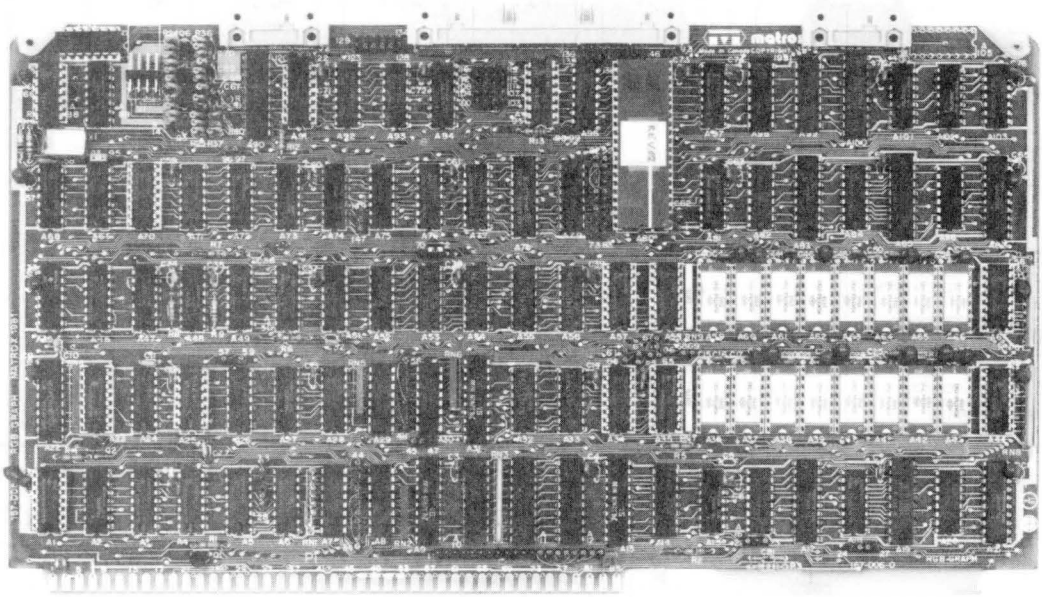
## VECTOR PLOT 512 x 512 COLOR GRAPHICS DISPLAY CONTROLLER FOR MULTIBUS



- **512 x 512 pixel resolution standard**
- **4 bits/pixel expandable to 16 bits/pixel**
- **Writing speed of 800ns/pixel**
- **DMA access to video RAM**
- **Light pen interface built-in**
- **Vector plot**
- **Hardware zoom, pan, scroll, and shift, clear, overlay, clipping, video enable**
- **Works with any 8 or 16 bit Multibus* CPU**
- **Add-on RGB-ALPHA board provides color alphanumeric overlay**
- **Add-on VAF-512 board adds:**
  - **— Real-time 512 x 512 frame grabber**
  - **— 16 million color look-up table**
  - **— Hardware vector generator**

The RGB-GRAPH is a member of Matrox's complete line of modular Multibus* compatible color video boards. By using the latest state of the art LSI and VLSI technology, the RGB-GRAPH provides an economical, self-contained solution for OEM color graphics applications requiring high resolution, top performance, and low cost. The board contains advanced video features such as hardware zoom, scroll, shift, pan, clipping, overlay, video masking, etc. which have previously been available only on the most expensive graphics systems at a much higher cost.

Furthermore, the RGB-GRAPH can be combined with other Matrox color video boards such as the color alphanumerics RGB-ALPHA and video processor board VAF-512 (containing real-time 512 x 512 frame grabber, color look-up tables, and a hardware vector generator). The OEM system designer can now easily incorporate powerful tailor-made graphics into his system at a fraction of the cost of a turn-key system.



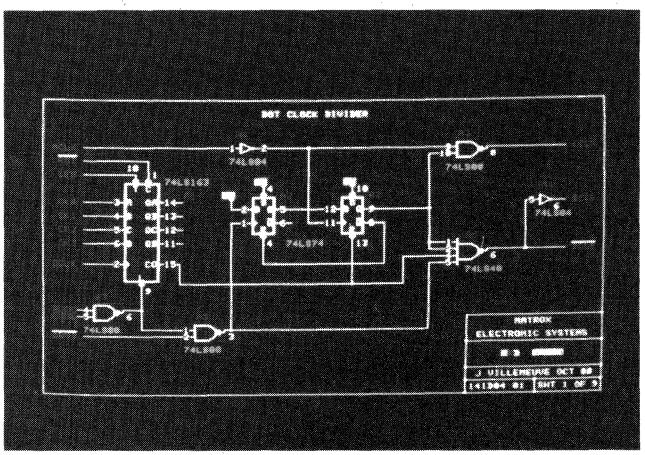


Figure 1. CAD/CAM applications

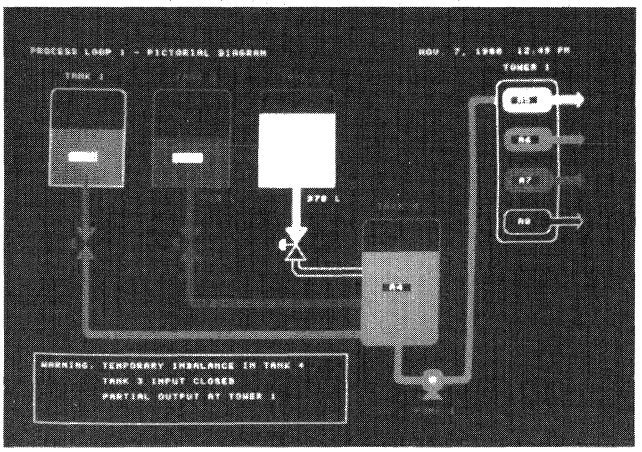


Figure 2. Process Control applications

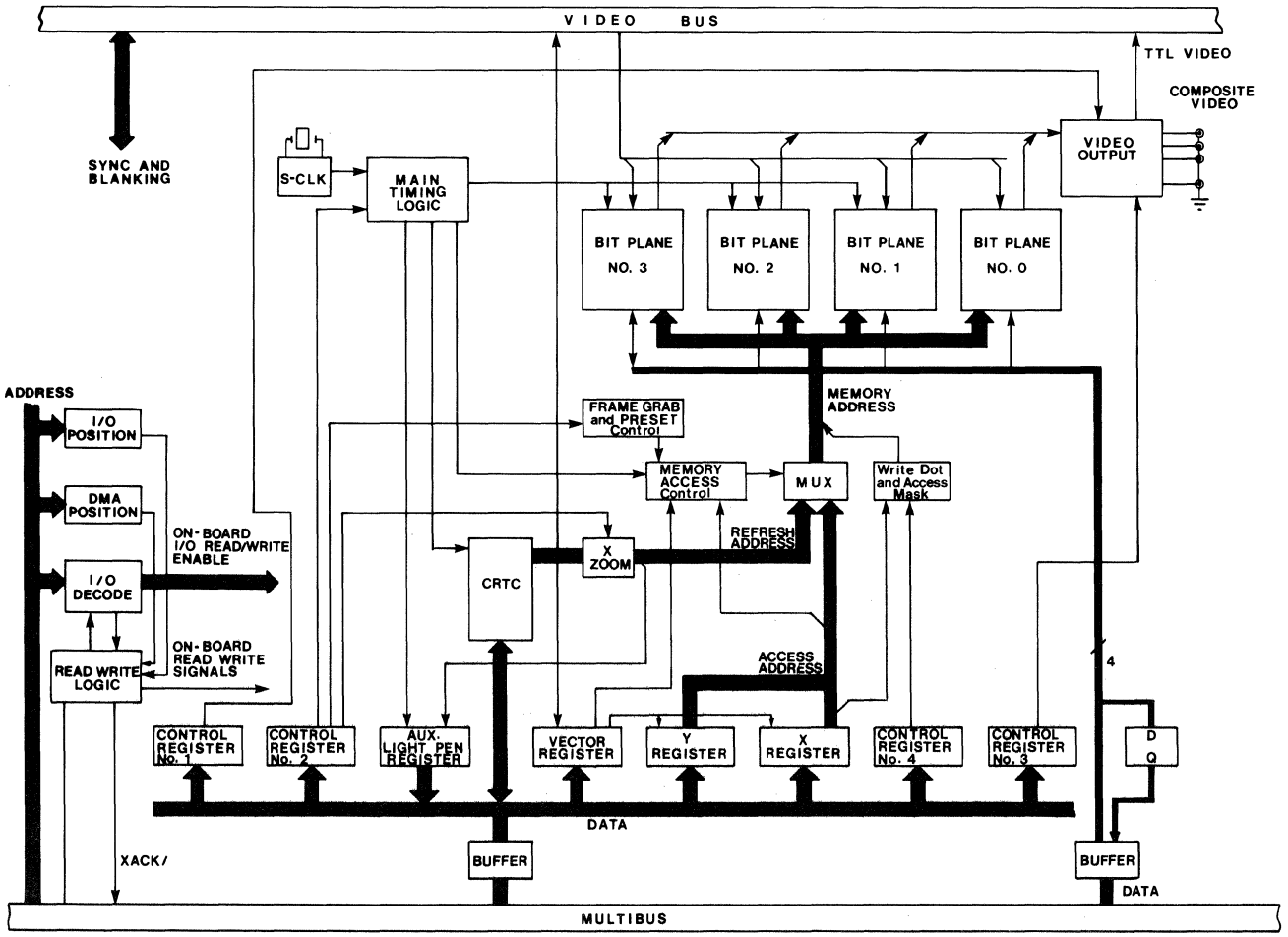



Figure 3. RGB-GRAPH block diagram

## RGB-GRAPH FEATURES

**Resolution:** 512 x 512 or 256 x 256 (special horizontal interlace mode can support 1024 x 512 or 512 x 256)

**Bits/Pixel:** 1-4 bits/pixel, expandable to 16 bits/pixel with additional RGB-GRAPH boards.

**Zoom:** Independent X-zoom by 1, 2, 3, 4, 5, 6, 7, 8
Y-zoom by 1, 2, 4
Zoom works on any segment of the 512 x 512 display

**Scroll:** Up/down scroll (vertical) by multiple of 8 pixels

**Shift:** Left/right (horizontal) by single or multiple dots

**Pan:** Scroll and shift can be combined for full two dimensional pan inside the 512 x 512 area

**Clipping:** 4096 x 4096 addressable area with hardware clip to 512 x 512 for read/write and display

**Clear Display:** Memory hardware clear to zero (black). All pixels cleared in one frame (33 msec.)

**Preset Display:** Memory hardware preset to value (color) in data register. All pixels preset in one frame (33 msec.)

**Preset Mask:** Clear/Preset control of each bit plane by Plane Mask

**Video Mask:** Video on/off control of each bit plane by VIDEO MASK

**Overlay Video:** One bit plane video can be combined with the three others for video effects. Functions available are AND, NAND, OR, X-OR

**Video Parameters:** All video parameters including horizontal and vertical syncs, blanking, frequency, and display format are user software programmable to drive any direct or composite B/W or color CRT monitor

**Video Outputs:** Direct TTL video (4), composite 75Ω R.G.B. color signals and 16-level grey scale signals are available

**Light Pen:** Detects true light pen position within one pixel accuracy. Interface built-in

**Vector Plot:** X-Y registers are auto-increment/decrement

**Display RAM:** Up to 128K byte on-board memory. CPU can read/write with 400ns (min.) and 1.2 μs (max.) access time/pixel. Memory looks like 262,144 x 4 RAM (single RGB-GRAPH), 262,144 x 16 (four RGB-GRAPHs)

**X, Y Pixel Address:** Each pixel can be addressed via X, Y registers (12 bits each). Data registers contain pixel color for read/write (I/O addressing)

**DMA Pixel Address:** 262,144 x 4 (8, 12, 16) display RAM can be accessed in 1K byte blocks (block address in X, Y registers) in DMA mode for image dumping (each pixel is one memory address)

**Double Resolution:** 512 x 512 x 4 display can be switched to 1024 x 512 x 2 under software control by combining two 512 x 512 x 1 planes. Effectively doubles horizontal resolution

**Multibus* Interface:** The RGB-GRAPH looks to the user like 16 I/O locations. All communications including pixel read/write, video functions, etc. are accomplished through I/O R/W (no DMA used). With DMA, 1K additional memory space is used.

**Access Time:** 500ns (max.) for any I/O port; 50ns (min.) — 1.2 μs (max.) for DMA

**Video Bus:** 50 pin connector provides video inputs and outputs for expanded performance using RGB-ALPHA, VAF-512 and additional RGB-GRAPH boards

## ADDITIONAL ADD-ON FEATURES

### RGB-ALPHA

**Alphanumerics:** Color alphanumeric displays can be added by the RGB-ALPHA board (synchronized to the RGB-GRAPH). Formats of up to 132 characters/line and up to 48 lines are user software programmable

### RGB-GRAPH

**16 Bits/Pixel:** By connecting additional RGB-GRAPH boards (max. 4) up to 16 bits/pixel can be obtained (each RGB-GRAPH adds 4 bits/pixel)

### VAF-512

**Color Look-up:** RAM video look-up table increases the number of displayable colors to $2^{24}$ = 16,772,216. CPU can read/write look-up table

**Frame Grabber:** Real-time frame grabber digitizes TV camera outputs with 4 or 8 bits/pixel resolution. Spatial resolution is 512 x 512 or 512 x 256. Single frame grab or continuous frame grab under software control

**Color Frame Grab:** By connecting R.G.B. outputs from a TV camera to the video switcher and grabbing each channel separately, a color picture can be digitized

**External Sync:** Built-in phase-lock loop synchronizes the RGB-GRAPH to an external composite sync (serrated) for broadcast and mixing applications

**Video Switcher:** Four-input video switcher enables the user to digitize four separate TV camera inputs under software control

**Vector Generator:** On-board hardware vector generator with speed of 800ns/pixel. Vector length, slope, and texture are user defined.

## ACCESSORIES

**CRT Monitors:** Matrox supplies a full line of 9" and 14" monochrome monitors, as well as 12", 14", and 19" high resolution (.3 mm pitch) color monitors for interlaced and non-interlaced operations

**Light Pen:** High speed light pen (LP-600)

## SOFTWARE SUPPORT

**GRAS-80:** Library of high-level graphic primitives (subroutines) including points, vectors, arcs, circles, characters, zoom, scroll, video effects, etc. is available (floppy diskette) in CP/M format. Runs under any Z-80 based CP/M system with the RGB-GRAPH plugged in. Subroutines are accessible from Z-80 assembler or "C".

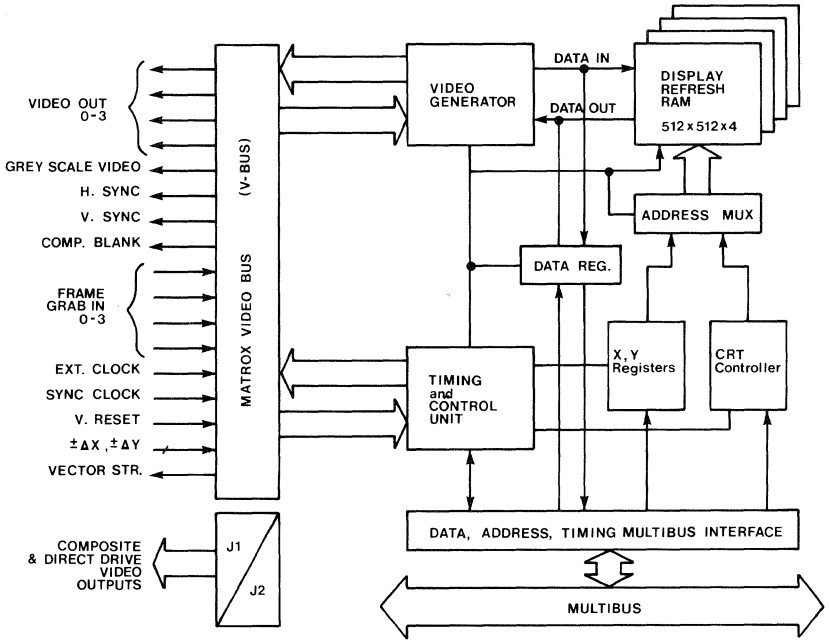



Figure 4. RGB-GRAPH functional blocks

## FUNCTIONAL DESCRIPTION

The RGB-GRAPH is a very complex digital graphics system on a single 6.5" x 12" PC board (figure 3). It consists of six main functional blocks (figure 4): CRT Controller, Video Generator, Display RAM, XY Registers, Timing and Control Unit, and Multibus Interface.

The **CRT Controller (CRTC)** is a VLSI IC which provides all video timing signals including horizontal and vertical sync and blanking, display refresh RAM addresses, as well as various other timing and control signals such as cursor, light pen interface, etc. The CRT Controller is software programmable allowing the user to program parameters such as vertical refresh frequency, width and position of horizontal and vertical sync pulses (important when using non-standard CRT monitors), display resolution, etc. To the Multibus CPU, the CRTC appears as an array of 18 registers which are indirectly addressed via two I/O ports.

The **Display Refresh Memory** is made up of 128K bytes of on-board dynamic RAM (for 512 x 512 x 4 resolution) which contains the binary picture information. Each pixel is identified by a unique address in the 262,144 address space (512 x 512). Each address contains 4 data bits which represent the pixel color. The memory is organized as four independent "planes", each containing one data bit (512 x 512 x 1). The display memory can be expanded to 16 planes through the combination of three additional RGB-GRAPH boards.

The CPU can read/write the display RAM in one of two ways. In the XY mode the CPU loads the X and Y registers with the pixel address and then reads/writes the pixel color information through the Data Register. This mode is normally used when drawing graphics point by point. For high speed read/write operations the CPU can access the refresh memory in DMA mode. The display memory is accessed in 1K byte blocks with the starting address of the desired block loaded into the X and Y registers before executing DMA. This mode is usually used when transferring complete images from/to mass storage devices (floppy, Winchester, etc.) or for hard copies.

In addition to the CPU read/write, the display memory is continually scanned by the CRTC every 16.66ms (60 Hz) to generate video signals or, in the frame grabbing mode, to load digitized TV camera images into memory at speeds of over 100 Megabits/second. Memory access arbitration circuitry on the RGB-GRAPH efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display refresh is "transparent" to the user.

The **X-Y Registers** are 12 bit up/down counter/latches with associated logic containing the address of the pixel being accessed by the graphics cursor (4096 x 4096 addressable area) as shown in figure 5. The CPU can load the X and Y Registers, through programmed I/O, with the pixel's absolute position. Two 8 bit ports are used for each Register. If the contents of either the X or Y Registers exceed the maximum resolution (i.e X > 512, Y > 512) the Clip Circuit will prevent CPU read/write.

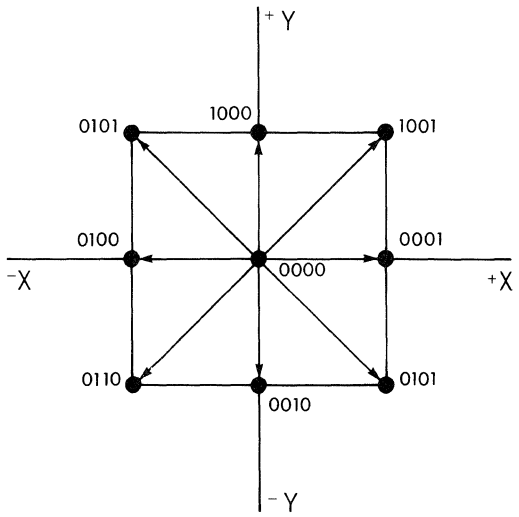



Figure 6. Vector Step Direction

These digital video signals are then passed through double density switches (used for multiplexing two planes to enable the user to double the horizontal resolution, eg. 1024 x 512) and are gated by video mask bits which are stored in the Video Mask Register. The user can, under software control, switch on/off selectively any bit plane enabling a variety of video effects such as animation, multi-page displays, mixing, etc. Overlay logic combines the fourth plane with the other three for various video effects. By plugging the appropriate IC into the overlay socket, the fourth plane can be NANDed (74LS00), ANDed (74LS08), ORed (74LS32), or X-ORed (74LS86) with the other three planes. Video effects such as alphanumerics mixing, multiple windows, graphics cursor, etc. can be accomplished through the use of the overlay feature.

After masking and overlay, the video signals are buffered by high drive buffers (74LS374) with 3-state outputs which are controlled by the video enable signal. The video signals are then placed on the Matrox video bus as TTL video signals (for use by a direct drive TV monitor). The video can alternately be fed to the on-board D/A converter where a composite sync signal is combined with the D/A output to produce a 16 level composite grey scale video signal (75Ω impedance) to drive B/W monitors or hardcopy devices. The TTL level video signals are also combined with a composite sync signal through the composite video buffer to provide composite R,G,B drivers. One of these outputs (normally green) can be intensity controlled by a 2-bit D/A converter connected to planes 2 and 3.

While operating in the frame grabbing mode, the video signals from a TV camera via the VAF-512 board are fed, through a phase lock loop (synchronizes the RGB-GRAPH timing to that of the external sync), to an 8-bit 10 MHz A/D converter. This video signal is then serially input to the 4-bit shift register where it is converted to parallel form and written to the display refresh memory. Note that this is exactly opposite to the generation of video signals during the read operation. Both the read and write video operations are synchronized so that the RGB-GRAPH can operate in a continuous frame grabbing mode (write new pixel data after previous pixel is read).

Various hardware video functions are performed in different sections of the RGB-GRAPH board rather than at one place. Video masking, overlay, D/A conversion, and double density switching are performed in the Video Generator section. Vector plotting and clipping are done through the X, Y Registers, X-zoom, shift, screen clear, and selected plane clear are done in the Timing and Control Unit, and scroll, Y-zoom, user programmable video parameters and light pen interface are handled by the CRT Controller chip.

The **Timing and Control Unit** generates signals for the CRTC as well as all signals required by the display refresh memory (figure 8). It consists of the main oscillator (X-TAL = 10 MHz), variable modulo counters (divide by 1-8) which are controlled by the X-zoom factor to produce the appropriate load and shift signals for the display and a divide by 16 counter which, with a timing PROM, generates a series of timing signals for the memory refresh (RAS, CAS).

The **Multibus* Interface** contains the logic required to interface the RGB-GRAPH to the Multibus*. The RGB-GRAPH looks like 16 consecutive 8-bit wide I/O locations strapped to any 16 address boundary. 8-bit (8085, Z-80A) or 12-bit (8086) I/O addressing can be used. The CPU communicates with the RGB-GRAPH by reading or writing into these I/O registers. The only exception is when the board is used in DMA mode. Then the display memory looks to the CPU like a 1K byte block of RAM (4, 8, 12 or 16 bits wide for 1, 2, 3, or 4 RGB-GRAPH cards). The starting address of the 1K byte block can be positioned anywhere in the 20-bit address space.

## DISPLAY SYSTEM CONFIGURATIONS

The Matrox family of advanced color graphics boards; which include the RGB-GRAPH, RGB-ALPHA and VAF-512 offer the OEM system designer the unique capability to design a powerful optimal graphics system with equal or even superior performance to turn-key graphics system, at a lower cost. Futhermore, by using general purpose OEM boards (from Matrox, Intel, NEC, or other suppliers), the user can add CPUs (8 or 16 bit), memory, disk interfaces, etc. Software support, in the form of a graphics primitives library, which runs under CP/M DOS still further simplifies design of the custom graphics systems. Hardware upgrade capabilities enables adding extra display functions by simply plugging in additional boards (more bits/pixel, higher speed, frame grabbing, etc.).

## SINGLE BOARD DISPLAY SYSTEM

Using a single RGB-GRAPH board provides for a versatile graphics system that can be used in many display applications from B/W to color.

| RESOLUTION | BITS/ PIXEL | PART NUMBER | APPLICATION |
|---|---|---|---|
| 256 x 256 | 1 | RGB-G/16/1 | Non interlaced B/W or color systems |
| 256 x256 | 4 | RGB-G/16/4 | Grey scale or 16 color display system |
| 512 x 256 | 2 | RGB-G/16/4 | High res. B/W, one bit for graphics and one bit for alphanumerics |
| 512 x 512 | 1 | RGB-G/64/1 | B/W display systems |
| 512 x 512 | 4 | RGB-G/64/4 | Grey scale or 16 color display system |
| 1024 x 512 | 2 | RGB-G/64/4 | High res. B/W, one bit for graphics and one bit for alphanumerics |

Table 1: Examples of display systems using single RGB-GRAPH

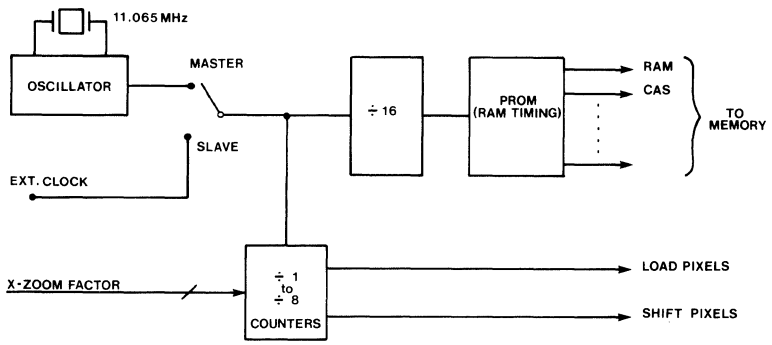



Figure 8. Timing and Control Unit

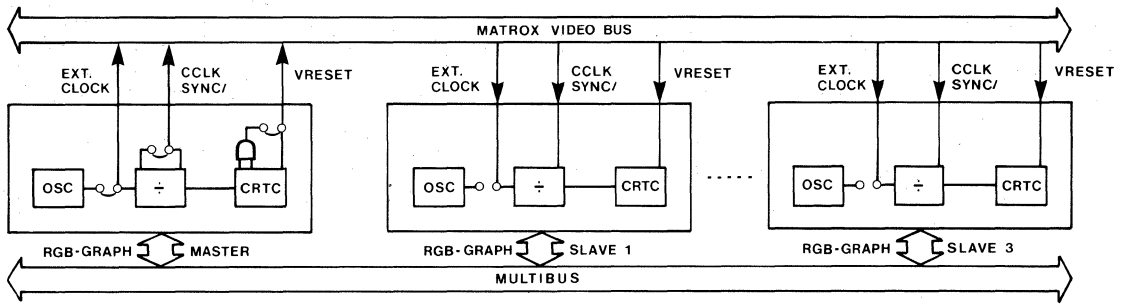



Figure 9. Multiple RGB-GRAPH System

## ADDING MORE BITS/PIXEL

Up to four RGB-GRAPH boards can be synchronized together via the video bus (single 50 pin ribbon cable) for up to 16 bits/pixel. Each RGB-GRAPH adds up to 4 bits/pixel.

## ADDING ALPHANUMERICS

Alphanumerics can be added to the graphics in three ways. The simplest way is to write alphanumerics, pixel by pixel, from a table stored in RAM or ROM. This offers flexibility in character size, color, position, and font but interferes with the graphics display. The second way is to use one of the bit planes on the RGB-GRAPH exclusively for alphanumerics and overlay it with the graphics planes. The use of a separate alphanumerics board (RGB-ALPHA) offers the highest speed. RGB-GRAPH and RGB-ALPHA are synchronized via the video bus connector. The alphanumeric format (character/line x lines) is user programmable. Video signals can be ORed (on the RGB-ALPHA) or mixed together via a color look-up table (on the VAF-512).

## VAF-512

The addition of a VAF-512 board enables the RGB-GRAPH system to digitize a real-time B/W or color video signal from a TV camera or VCR with 4 or 8 bits/pixel. Also, a high speed look-up table on the VAF-512 expands the number of displayable colors to over 16 million. The VAF-512 can also be used for video mixing, animation, etc. A high speed hardware vector generator executes high level graphics commands at 800ns/pixel. The VAF-512 is synchronized via the video bus and it works in 256 x 256, 512 x 256 and 512 x 512 resolution.

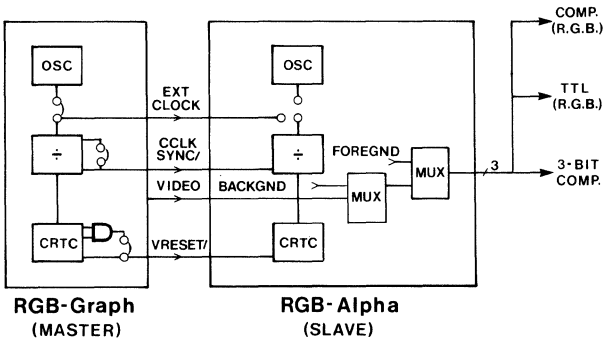



Figure 10. Alphanumerics Overlay

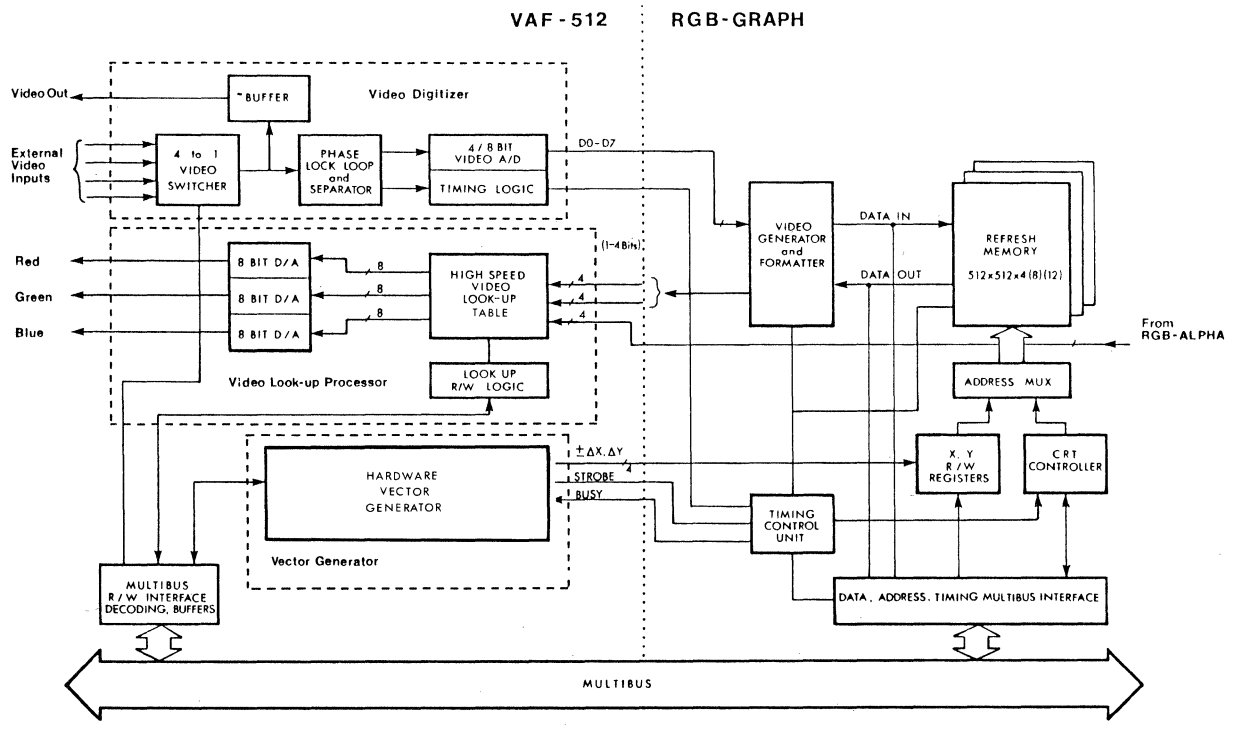



Figure 11. VAF-512 Video Processor

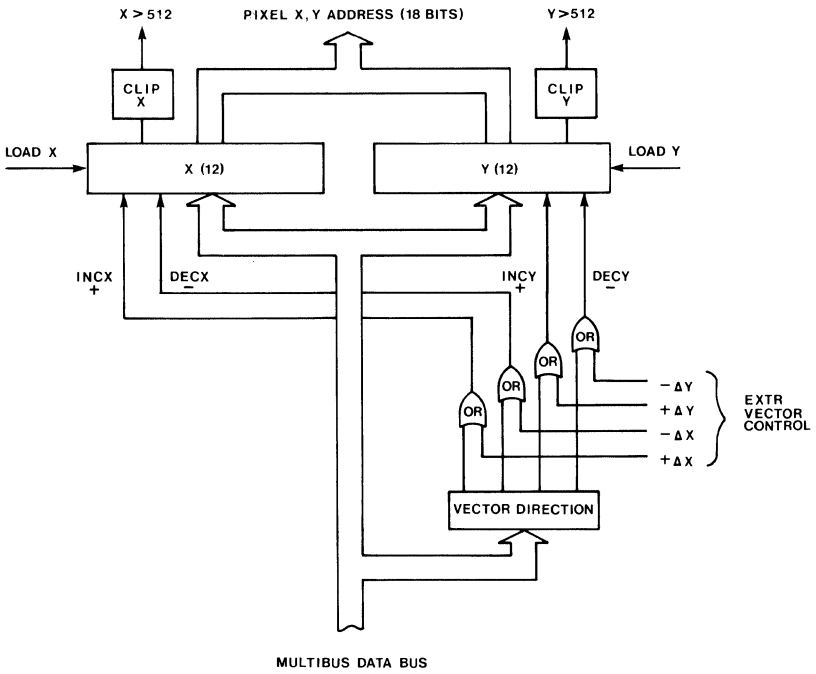



Figure 5. X,Y Registers

For high speed relative drawings, the vector plot feature can be used. By writing into the Vector Register the draw ing direction (4 bits), the X and Y Registers are automatically incremented/decremented (figure 6).

The vector plot can be interfaced with the hardware vector generator contained on the VAF-512 board. The VAF vector generator generates $\pm\triangle X$, $\pm\triangle Y$ increment/decrement pulses when drawing vectors, circles, etc. at the speed of 800ns/pixel. The vector plot function can also be used for drawing pictures without tying up the system bus in multiprocessor applications by connecting the $\pm\triangle X$, $\pm\triangle Y$ inputs to the I/O ports of the CPU board.

The X, Y Registers are also used in the DMA mode for autoincrementing the RAM address within the 1K byte DMA block.

The **Video Generator** performs three basic functions: conversion of digital data from the refresh RAM into the proper video signals to drive B/W and color monitors, conversion of digital video data from a frame grabber into a format required to write the data into the reresh RAM at video speeds, and the performance of various other video processing functions in hardware (zoom, scroll, overlay, clipping, video masking, doubling the horizontal resolution, etc.). The Video Generator is shown in figure 7.

Data is read from the display RAM as 4 consecutive pixels at one time for each plane (for refresh each plane looks like 512 rows x 128 strings/row x 4 1-bit pixels/string). This 4 pixel data is loaded into a shift register and then shifted out at the video clock speed (10MHz for 512 x 512 resolution) to produce a serial TTL signal for each plane (four in total).

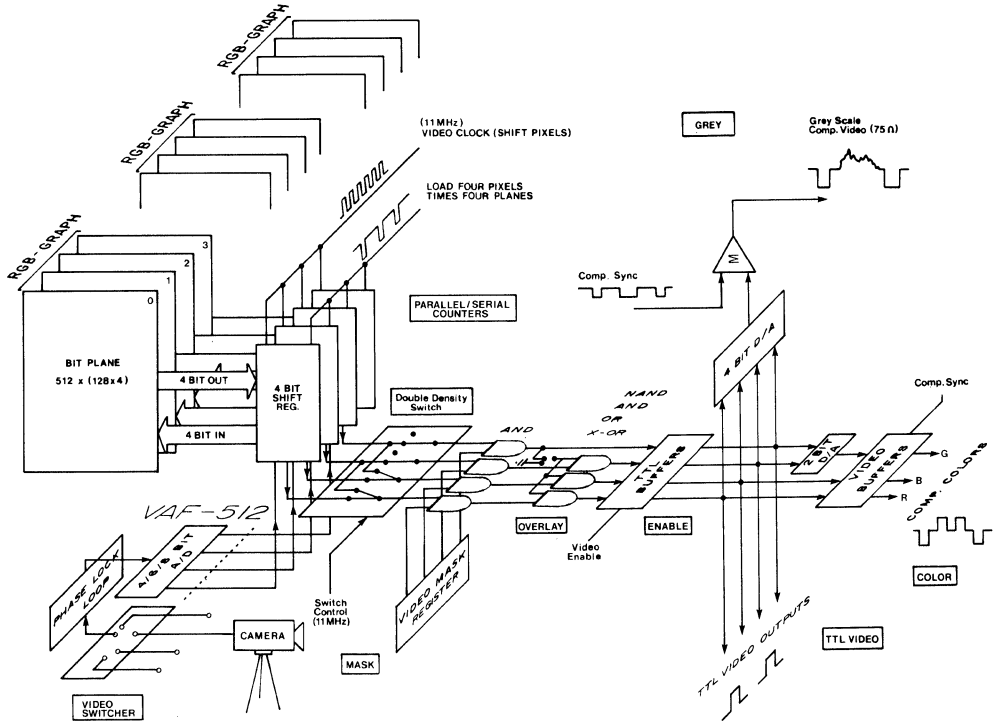



Figure 7. RGB-GRAPH Video Generator

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

CRTC Data, CRTC Address, CRTC Status, and Vector Register access time is fixed at 500ns.
Access time to all other locations (including DMA) varies from 50ns to 1.2 μs for boards using 64K parts (see ORDERING INFORMATION), and from 50ns to 2.4 μs for boards using 16K parts. Average access time for 64K boards is approximately 800ns, and for 16K boards is about 1600ns.

### DISPLAY PARAMETERS

| RESOLUTION | RAM TYPE |
|---|---|
| 256x 256 x 4 | 16K |
| 512x 256 x 2 | 16K |
| 512 x 512 x 4 | 64K |
| 1024 x 512 x 2 | 64K |

### VIDEO TIMING

For a display format of 512 horizontal dots x 512 vertical dots on a monitor with a 51.2μs active video time a 10.000 MHz crystal is used. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 51.2 μs | 51.2 μs |
| Horizontal Sync Frequency | 15.82 KHz | 15.82 KHz |
| Horizontal Sync Width | 4.80 μs | 4.80 μs |
| Vertical Sync Frequency | 62.2 Hz | 51.2 Hz |
| Vertical Sync Width | 189.6 μs | 189.6 μs |

### INPUT SIGNALS

Light-pen Enable
Lignt-pen Strobe

### OUTPUT SIGNALS

TTL Level Video: TTL level Red
TTL level Green0
TTL level Green1
TTL level Blue
Vertical Drive
Horizontal Drive

Analog Video: Red
Green (composite)
Blue
Grey Scale (composite)

### BUS INTERFACE

Address, data and control signals conform to Intel Multibus Specification No. 9800683
Command and Status Registers — Selectable on 16 byte I/O address boundaries 000 — FFF (0A0H)
Display Refresh Memory (DMA only) — Selectable on 1K byte memory address boundaries 0000-FFFFF (07C00H)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1 : 86 pin edge connector, 0.156" centers, | Multibus interface | COMPAR ESM-43-DSRI |
| J1 : 10 pin right angle header, | Analog video outputs | AMP 87922-1 |
| J2 : 10 pin right angle header, | TTL video outputs | AMP 87922-1 |
| J3 : 50 pin right angle header, | Matrox video bus | Molex 15-25-4505 |
| J4 : 10 pin right angle header, | Light pen interface | AMP 87922-1 |

## PHYSICAL

### SIZE

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15cm)
Depth — 0.50 in. (1.27cm)

### POWER REQUIREMENTS

64K — ±5V DC ±5% @ 2.25A
16K — ±5V DC ±5% @ 1.80A
+12V DC ±5% @ 128mA
−12V DC ±5% @ 30mA

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0%C to 55%C
Relative Humidity: 0° to 95° non-condensing

### ORDERING INFORMATION

RGB-G/XX /X
- XX — Type of RAM (16/64)
- X — Number of bits per pixel (1/4)

Example: RGB-G/64/4: 512 x 512 color graphics controller with four bit planes

Note: The RGB-GRAPH should be ordered in exact configurations. User field upgrades (different resolutions, more bits/pixel) are not recommended as these require straps and PROM.

Software Support:
GRAS-80: CP/M compatible graphics primitives library

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# VAF-512

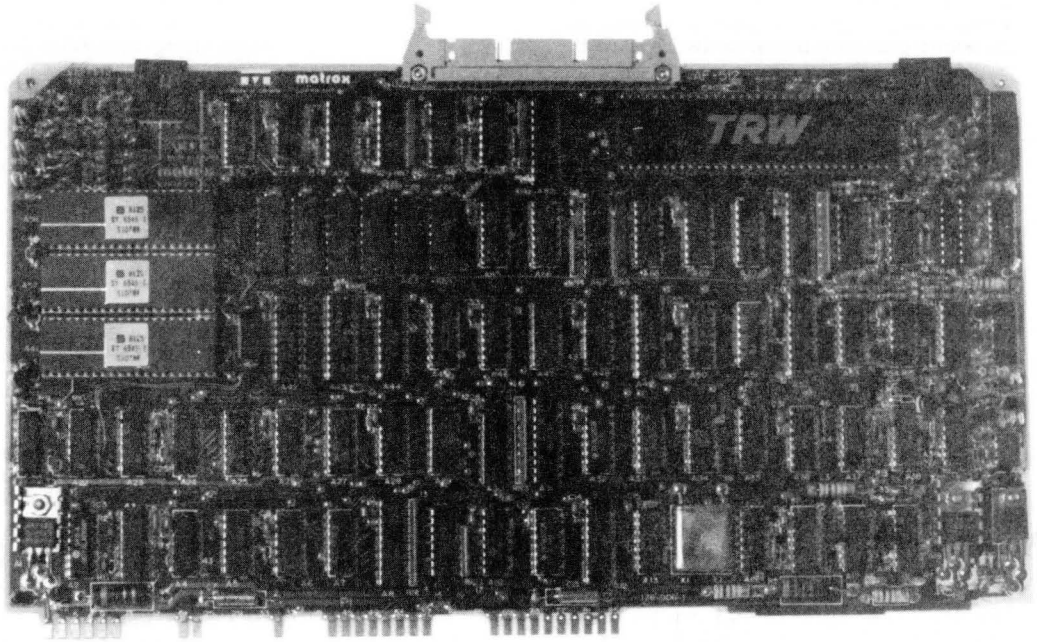
## RGB-GRAPH VIDEO INPUT/OUTPUT PROCESSOR FOR MULTIBUS

1

- **Real Time Video Frame Grabber**
  - **— 4 or 8 bit A/D**
  - **— 4 input video switch**
  - **— Programmable clamping and gain**
  - **— Internal/external, block/serrated sync**
  - **— Phase locked loop for Genlock**
- **Color Look-Up Table (RAM)**
  - **— 10 input lines/24 output lines**
  - **— Three 8 bit D/A converters (R, G, B)**
  - **— 16 million color palette**
  - **— Blink and overlay control**
- **Hardware Vector Generator**
  - **— High speed line drawing (800ns/pixel)**
  - **— Length, slope, and texture control**
- **Multibus* Compatible**
- **Works With RGB-GRAPH Board**
- **RGB-ALPHA Overlay Compatibility**
- **American/European Operation**

The VAF-512 is a video I/O processor board designed to extend the performance of the Matrox RGB-GRAPH video controller. The VAF-512 has three main subsections: a real time video digitizer (frame grabber), a color look-up table, and a high speed vector generator. The video A/D converter provides real time grey scale digitizing, of a camera, videodisk, or VCR signal (4 or 8 bits/pixel), into one or two RGB-GRAPH frame buffers. The color look-up table provides a palette of over 16 million output shades and colors. The look-up table can accommodate one or two RGB-GRAPH boards and an RGB-ALPHA. The on-board vector generator provides high speed line drawings (800ns/pixel). The length, slope, and texture of the displayed lines are all software controlled.

The VAF-512 plugs into any standard Multibus backplane and interfaces to the RGB-GRAPH/RGB-ALPHA via a single 50-pin ribbon cable. The board can be used with both 8 and 16 bit CPUs and will operate in either American or European standard systems.



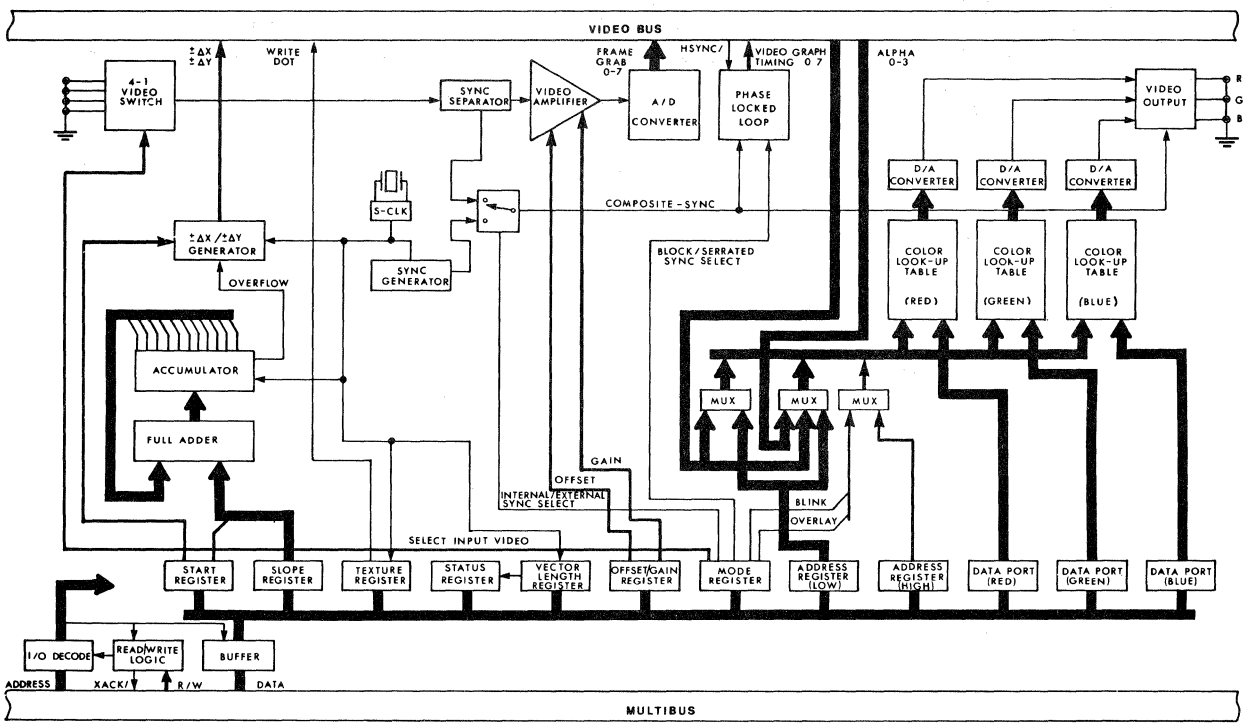



Figure 1. VAF-512 block diagram

## VAF-512 FEATURES

### FRAME GRABBER

**High Speed A/D Converter:** The VAF-512 contains an on-board 10 MHz A/D converter for real-time frame grabbing applications. Images can be digitized to either 4 or 8 bits/pixel.

**4 Input Video Switch:** Up to four different analog video inputs can be accepted by the VAF-512. Each video source can be individually selected for frame grabbing under software control.

**Color Frame Grabbing:** By connecting the R, G, B outputs from a color video camera to separate inputs on the video switcher, and then grabbing each channel separately, a color picture can be digitized.

**Software Controlled Gain and Offset:** The VAF-512 Frame Grabber enables the user to introduce a software programmable gain and/or offset to the input video signal. This feature enables the user to concentrate the digitizing operation on that part of the input signal which contains most of the video information — effectively increasing the contrast.

**Programmable Sync:** Under software control the VAF-512 can be programmed to lock to either block or serrated sync. Sync signals can be generated on-board, or stripped from the input video signal for broadcast and video mixing applications.

### VECTOR GENERATOR

**High Speed Line Drawings:** Vectors can be drawn to the graphics display, via the VAF-512 hardware Vector Generator, at speeds that are 20 to 40 times faster than conventional software vector generation techniques.

**Vector Texture Control:** The texture of the displayed vectors (dotted, dashed, solid, etc.) can be programmed by the user through an on-board 8 bit Texture Register. Up to 512 different texture patterns can be defined.

### COLOR LOOK-UP TABLE

**Programmable Colors:** The VAF-512 Color Look-Up Table allows the user to select the available display colors from over 16 million possible shades. Up to 16 colors can be displayed with systems using one RGB-GRAPH board, and 256 colors can be displayed using two RGB-GRAPH boards.

**Overlay:** Alphanumeric characters (from the RGB-ALPHA) can be overlayed on the graphics display through the Color Look-Up Table. When characters are to be overlayed on the display, the 4 bits from the RGB-ALPHA board will replace the four most significant graphics bits on the look-up table address lines.

**Blink:** The graphics display can be set to blink between any of the available display colors. The VAF-512 can also be programmed to blink only the overlayed alphanumeric characters. The blink frequency can be software selected for 1.8 Hz or 3.75 Hz.

**MULTIBUS INTERFACE** The VAF-512 looks to the user like 12 consecutive I/O locations. All communications between the host CPU and the VAF-512 (including read/write operations to the Color Look-Up Table) are accomplished via I/O read/write.

**ACCESS TIME:** Time from CMD/ to XACK/ for all registers is fixed at 200ns.

**VIDEO BUS:** A 50 pin connector provides all the video input and output lines required to interface the VAF-512 with up to two RGB-GRAPH boards and one RGB-ALPHA board.

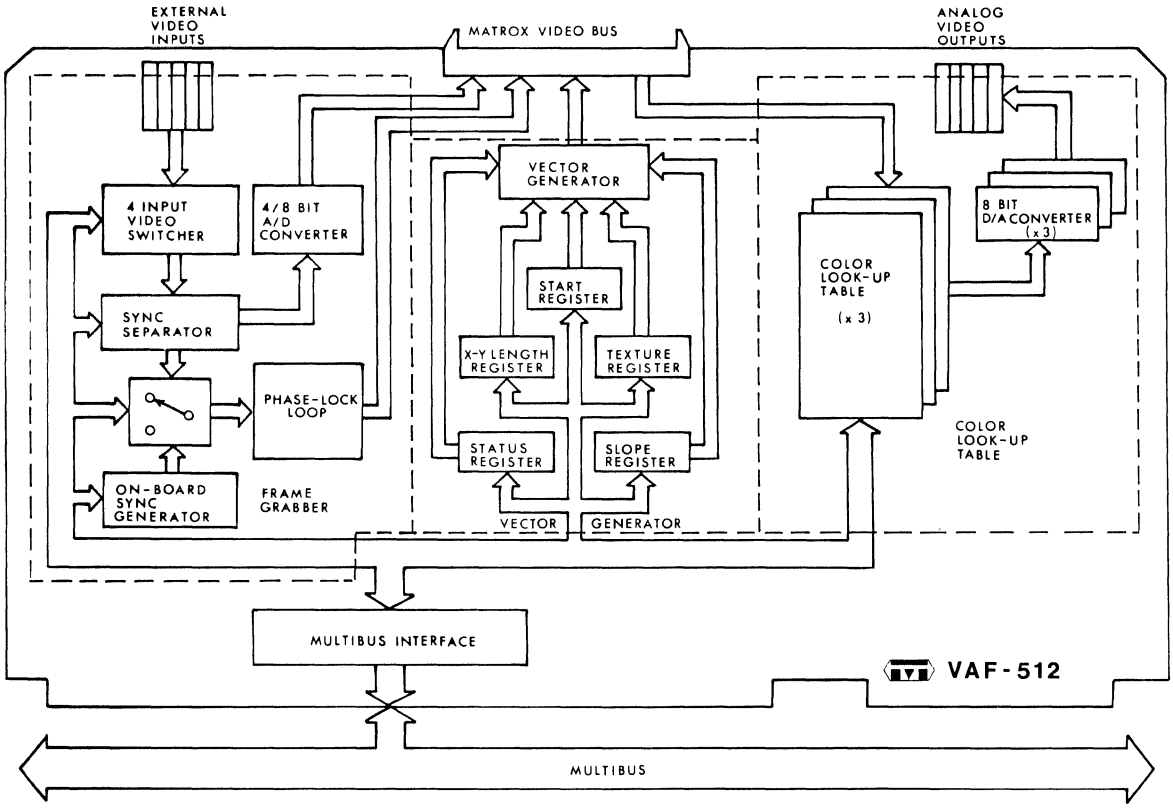



Figure 2. VAF-512 functional blocks

## FUNCTIONAL DESCRIPTION

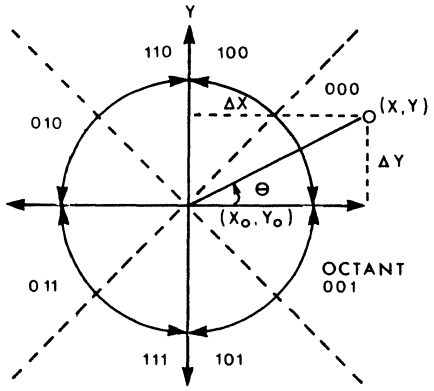
The VAF-512 has been designed to complement the operation of Matrox's RGB-GRAPH/RGB-ALPHA family of color video controllers. The VAF-512 comprises three independent operational sections (figure 2) contained on a single Multibus compatible PC board.

The on-board **Hardware Vector Generator** provides an efficient means of drawing vectors to the RGB-GRAPH display memory. Three parameters are required to specify a line draw operation; length, slope, and texture. The 10 bit Length Register stores the length of the larger of the two components ($\Delta X$, $\Delta Y$). This permits vectors of up to 1024 pixels to be drawn with a single software Write command. A 10 bit Slope Register stores, with single pixel precision, the $\tan\theta$ where $\theta$ is an angle between 0° and 45°. Three bits in the Start Register define the proper octant. The Vector Generator circuit calculates the $\Delta X$ and $\Delta Y$ addressing, as required by the RGB-GRAPH, on a pixel by pixel basis until the full vector has been drawn. A Busy Flag in the Status Register is used to indicate completion.

The texture of the displayed vector is stored in an 8 bit Texture Register. The contents of the Texture Register define an 8 bit repeating pattern of pixel information (figure 4). In this way solid, dotted, dashed, and hidden vectors can be drawn. Note that the Data Register on the RGB-GRAPH board is used to set the color of the vector.

The hardware Vector Generator operates with a drawing speed of 800ns/pixel. This represents an increase of about 20 to 40 times the conventional drawing speeds acheived by software vector generation.

The VAF-512 **Frame Grabber** enables the user to digitize a frame of video information (from an external video camera, VCR or videodisk), with either 4 or 8 bits per pixel, and store that frame in the RGB-GRAPH display memory (512 x 512 x 4 bits per GRAPH board). Using commands issued by the RGB-GRAPH, this frame grabbing operation can be continuous (RGB-GRAPH will display a continually updated or "live" picture) or one shot, effectively "freezing" the ac-




IF $|\Delta X| \geq |\Delta Y|$
THEN LENGTH = $|\Delta X|$
AND SLOPE = $\left|\frac{\Delta X}{\Delta Y}\right|$

IF $|\Delta X| < |\Delta Y|$
THEN LENGTH = $|\Delta Y|$
AND SLOPE = $\left|\frac{\Delta Y}{\Delta X}\right|$

Figure 3. Determining vector length and slope parameters

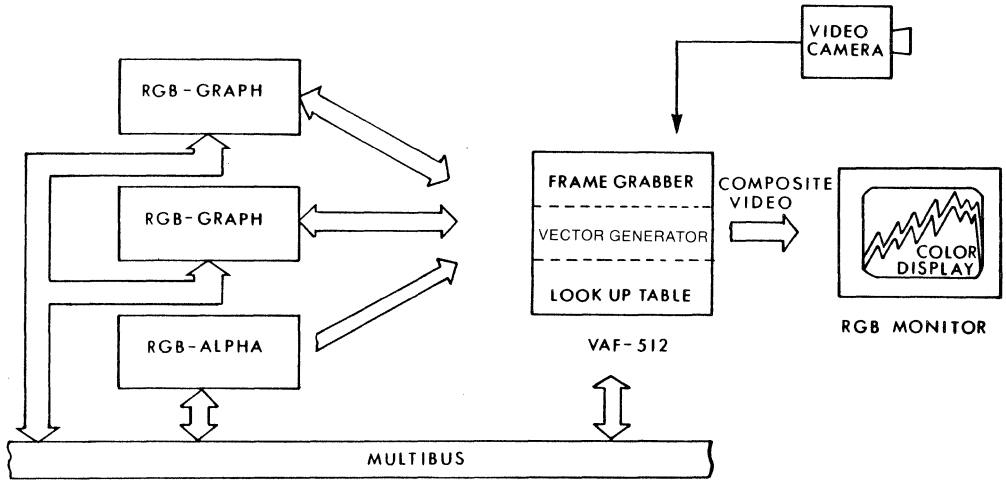



Figure 5. VAF-512 in system

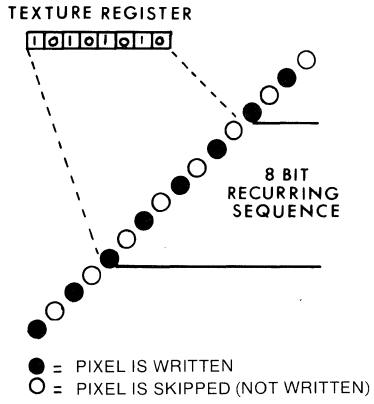



Figure 4. Defining the "Texture" pattern for the displayed vectors

tion. Up to four video cameras can be interfaced to the VAF-512 through an on-board four input video switcher which permits software selection between the four video sources.

Incorporated into the design of the frame grabber is a Phase-Lock Loop circuit (PLL). The PLL uses the sync signal stripped from the input video signal as a reference frequency to which it synchronizes the rest of the system (RGB-GRAPH/RGB-ALPHA). If required, an on-board sync generator (strappable for American EIA or European CCIR standard sync) can be software-selected to act as a master sync source for both the video display boards and the video source. The PLL can also be programmed to accept either block or serrated sync.

The VAF-512's frame grabber provides software control over the gain of the input signal. This feature, together with a software-variable voltage offset (clamping level) on the input, allows the user to take advantage of the full digitizing range of the A/D converter for a given input signal amplitude. This technique can be used to concentrate the operation of the A/D converter on that part of the input signal that contains the most video information, in effect increasing the contrast of the image. There are sixteen different levels of gain and sixteen different levels of offset.

The VAF-512 **Color Look-Up Table** is made up of three 1K x 8 RAM look-up tables (one for each primary color: red, green, and blue), each of which are divided into four 256 byte sections: Normal, Overlay, Blink, and Blink And Overlay. These Color Look-Up Tables provide the RGB-GRAPH

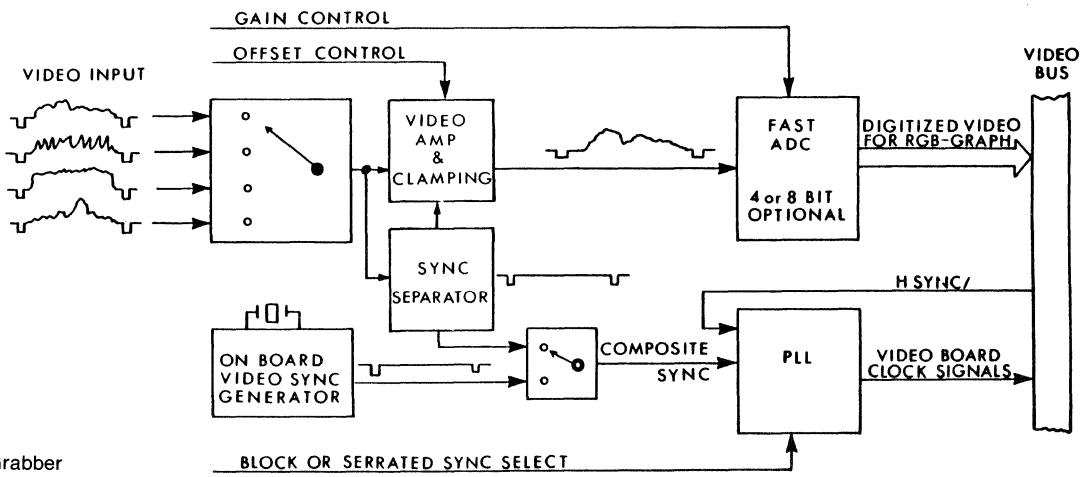



Figure 6. Frame Grabber

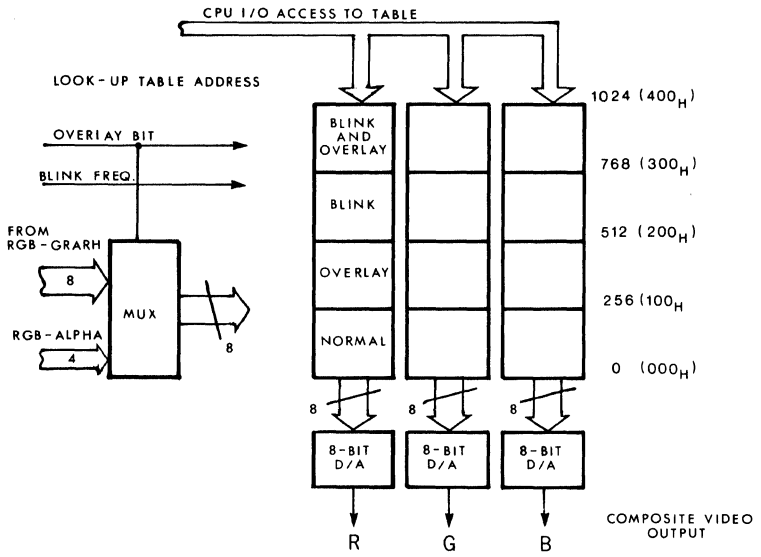



Figure 7. Color Look-Up Table

with a color palette of over 16 million colors. To display a desired color at a certain pixel location, the user simply loads that color's look-up table address into the RGB-GRAPH display memory location corresponding to the pixel position. The contents of the look-up table can be changed at any time. A single RGB-GRAPH board (4 bits) can address 16 different locations in the look-up table. Two RGB-GRAPH boards (8 bits) can address up to 256 locations in the look-up table. Additionally, the Color Look-Up Table is sectored into four 256 byte blocks (figure 5) in order to allow separate color mappings for overlayed alphanumerics and for blinking. The blink rate is software selectable to be either 1.8 Hz or 3.75 Hz.

When an RGB-ALPHA is interfaced to the VAF-512 the four bits from the alpha board replace 4 of the 8 graphic bits in addressing the Color Look-Up Table. When at least one of these bits is high (alphanumeric data is to be displayed) access to the look-up table is shifted to the Overlay section which contains its own color map. As a result, alphanumeric text from the RGB-ALPHA can be superimposed (overlayed) on the graphics background. The user can also program the VAF-512 to blink the alphanumeric characters between the colors defined in the Overlay and Overlay And Blink sections of the look-up table (similiar to blinking graphics pixels between the Normal and Blinking sections). This method of generating blinking characters is very flexible as it allows characters to blink to colors other than their background color.

## MATROX VIDEO BUS

The VAF-512 is interfaced to the RGB-GRAPH and RGB-ALPHA boards by way of a 50-pin Matrox Video Bus. Digitized video data as well as X and Y increment/decrement strobes are bussed from the VAF-512 to the RGB-GRAPH. The Video Bus also carries the 4 TTL video bits from each of the RGB-GRAPHs and the RGB-ALPHA boards for color look-up on the VAF-512.

## BUS INTERFACE

The VAF-512 plugs directly into the Multibus and works with both 8 and 16 bit processors using byte wide data transfers. The twelve Command and Status Registers are positioned on any 16 byte I/O address boundary between 0000H and FFFFH.

## PROGRAMMING

The VAF-512 is programmed via twelve on-board I/O registers. On power-up or reset all control registers must be loaded with the VAF-512's operational parameters (table 1).

| REGISTER | ADDRESS | DEFINITION |
|---|---|---|
| ADDRESS REGISTER LOW | BASE + 0 | Lower 8 bits of look-up table address |
| ADDRESS REGISTER HIGH | BASE + 1 | 2 most significant bits of look-up table address |
| GAIN/OFFSET REGISTER | BASE + 2 | Select gain/Select offset |
| MODE REGISTER | BASE + 3 | Select input video to frame grabber/Enable on-board sync generator/Select block sync/Enable overlay/Select blink frequency/Enable blink |
| VECTOR SLOPE REGISTER | BASE + 4 | Lower 8 bits of vector slope |
| X-Y LENGTH REGISTER | BASE + 5 | Lower 8 bits of vector length |
| TEXTURE REGISTER | BASE + 6 | Texture pattern |
| START REGISTER | BASE + 7 | 2 most significant bits of vector slope/Complement Texture Register/vector slope < 45/vector quadrant/2 most significant bits of vector length |
| RED DATA PORT | BASE + 8 | Read/write port to Red look-up table |
| BLUE DATA PORT | BASE + 9 | Read/write port to Blue look-up table |
| GREEN DATA PORT | BASE + A | Read/write port to Green look-up table |
| STATUS REGISTER | BASE + B | Vector generator status (BUSY) |

Table 1. Register Definitions

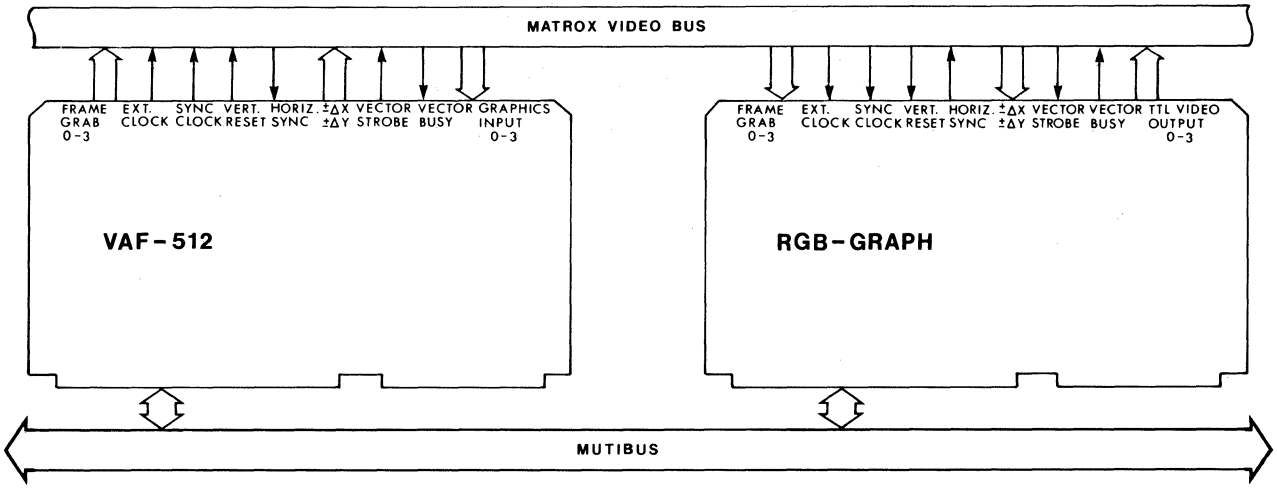



Figure 8. 512 x 512 x 4 video imaging system

## DISPLAY SYSTEM CONFIGURATIONS

The Matrox family of advanced color video boards, which include the VAF-512, RGB-GRAPH, and RGB-ALPHA, offer the OEM system designer a unique capability to design a powerful optimal graphics system with the equal or even superior performance of a turn-key graphics system — at a lower cost. Furthermore, by using general purpose OEM boards (from Matrox, Intel, NEC, or other suppliers), the user can add CPUs (8 or 16 bit), memory, disk interfaces, etc. to configure his system to his exact requirements. Software support, in the form of a graphics primitive library which runs under CP/M DOS, further simplifies design of custom video systems. Hardware upward capability enables adding extra display functions by simply plugging in additional boards (more bits/pixel, higher speed, alphanumeric overlay, etc).

### 4 BIT/PIXEL IMAGING SYSTEM

Combining the VAF-512 with a single RGB-GRAPH (figure 8) yields a video imaging system using 4 bits/pixel. Whole frames of video picture information with up to 16 color or grey levels can be digitized and stored in the display memory of the RGB-GRAPH.

### 8 BIT/PIXEL IMAGING SYSTEM

Adding another RGB-GRAPH graphics controller to the system (figure 9) doubles the number of bit planes to eight. This enables the system to store and display images with a resolution of 512 x 512 dots using up to 256 colors or grey levels.

An alphanumerics overlay can also be added to the graphics display by plugging in an RGB-ALPHA alphanumerics controller to the system.

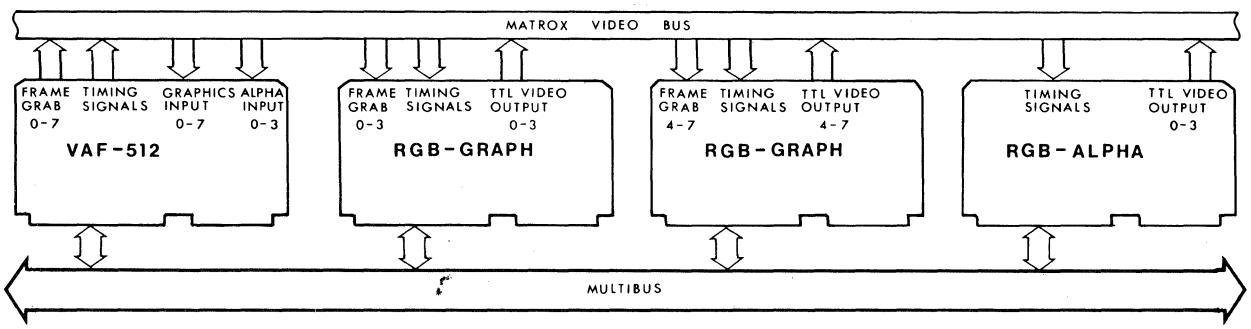



Figure 9. 512 x 512 x 8 video imaging system with alphanumerics overlay

# SPECIFICATIONS

## FUNCTIONAL

## OPERATIONAL PARAMETERS

### VECTOR GENERATOR

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Drawing Speed | 800ns/pixel (512 x 512 resolution) |
| Vector Texture | 512 texture patterns (software selectable) |

### FRAME GRABBER

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Spatial Resolution | 512 x 512 max. |
| Video Inputs | 4 analog video inputs (software switchable) |
| Sync | Internal/external, block/serrated (software selectable) |
| Bits/pixel | 4 or 8 bits |
| Offset | 16 increments form Black level to nominal mid-range (software selectable) |
| Gain | 16 increments from 0.7 to 1.9 of nominal (software selectable) |

### COLOR LOOK-UP TABLE

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Palette Size | $2^{24}$ = 16,777,216 colors |
| Addressable Colors | 16 colors (1 x RGB-GRAPH)/256 colors (2 x RGB-GRAPH) |
| Blink Rate | 1.8 Hz/3.75 Hz (software selectable) |

### INPUT SIGNALS

ANALOG INPUTS: Camera 0, Camera 1, Camera 2, Camera 3

TTL LEVEL INPUTS: 4/8 graphics bits, 4 overlays bits, HSYNC/, BUSY/

### OUTPUT SIGNALS

ANALOG OUTPUTS: Composite Video (RED), Composite Video (BLUE), Composite Video (GREEN)

TTL LEVEL OUTPUTS: 8 Video bits, System Clock, ± △X, ± △Y, V. Reset

### BUS INTERFACE

Address, data, and control signals conform to Intel Multibus Specification No. 9800683
Command and Status Register — Selectable on any 16 byte I/O address boundaries 0000 — FFFFH (0060H).

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 86 pin edge connector, 0.156" centers — Multibus Interface | COMAR ESM-43-DSRI |
| J1: 10 pin right angle header — Composite Video Ouptut | AMP 87922-1 |
| J2: 10 pin right angle header — Analog Video Input | AMP 87922-1 |
| J3: 50 pin right angle header — Matrox Video Bus | MOLEX 15-25-4505 |

### PHYSICAL

**SIZE**

WIDTH: 12.00 in. (30.48 cm)
HEIGHT: 6.75 in. (17.15 cm)
DEPTH: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+5V DC ±5% @ 3.2A
+12V DC ±5% @ 120mA
−12V DC ±5% @ 0.95A (VAF-512/8)
−12V DC ±5% @ 0.55A (VAF-512/4)

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 90% non-condensing

### ORDERING INFORMATION

VAF-512 / X — XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- X: Number of bits per pixel (4/8)

Example: VAF-512/8-AS: American standard board with an 8 bit/pixel A/D converter (frame grabber).

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# RGB-ALPHA

## PROGRAMMABLE COLOR ALPHANUMERIC DISPLAY CONTROLLER FOR MULTIBUS

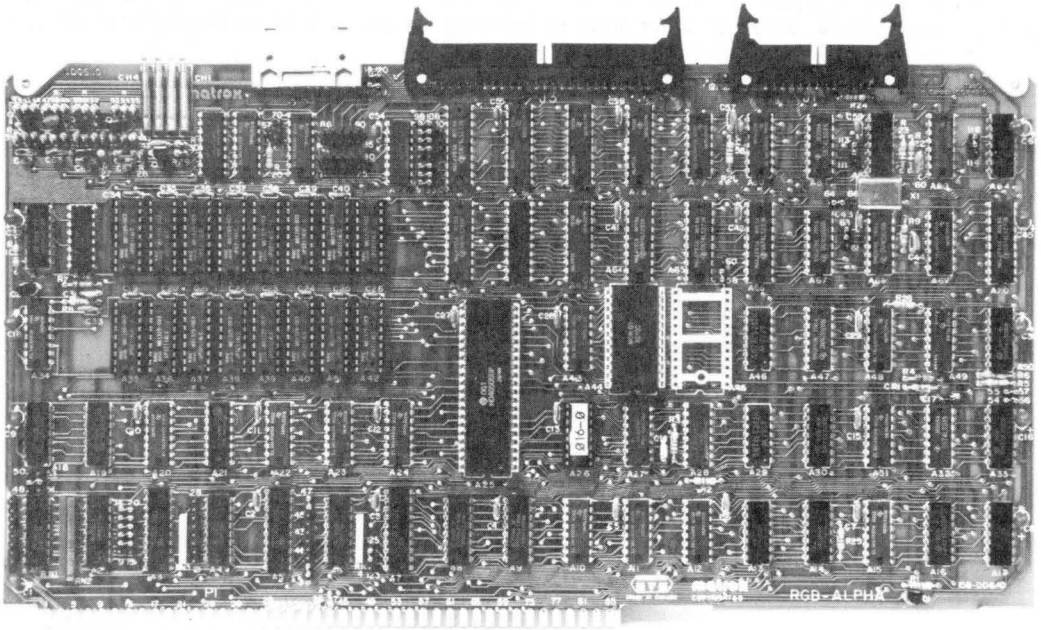
1

- **User Programmed Display Format**
- **Up to 4000 Characters**
- **8 Display Colors**
- **Blink**
- **Double Height Characters**
- **Underline**
- **Addressable Cursor**
- **Multibus* Compatible**
- **Keyboard Interface**
- **Light Pen Interface**
- **RAM and EPROM Character Generator**
- **Transparent Memory**
- **50 or 60 Hz Operation**
- **Drives any RGB Color Monitor**

The RGB-ALPHA is a Multibus* compatible, color video display controller card which allows the display (characters/line x lines/page) and character formats (5 x 7, 7 x 9 etc.) to be set by programmed I/O commands. Each character is displayed in 1 of 8 foreground colors on 1 of 8 background colors. Characters may be either single or double height and either normal, blinking at 2 Hz or underlined.

The character font provided with the RGB-ALPHA contains 128 - 5 x 7 dot upper/lower case alphanumeric characters and graphics symbols. By adding a second character generator ROM/RAM, 128 additional symbols may be defined. When using a RAM character generator, the character font may be rewritten at any time by the system processor.

The RGB-ALPHA works with all monochrome and color (RGB) video monitors in Europe (50 Hz) and America (60 Hz). Interfaces for a high-speed light pen and an 8-bit parallel keyboard are also provided.



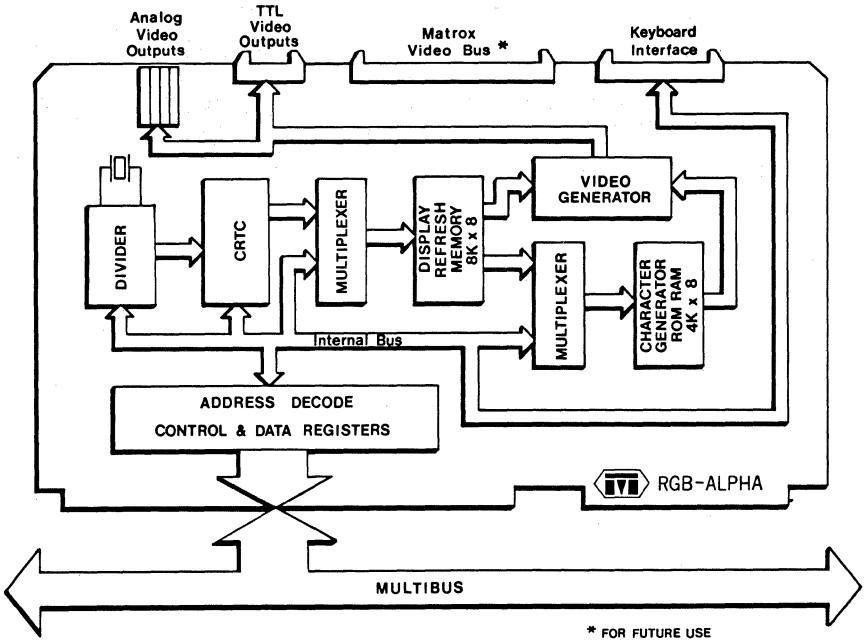



Figure 1. RGB-ALPHA block diagram

## FUNCTIONAL DESCRIPTION

The block diagram, Figure 1, shows the major functional components of the RGB-ALPHA.

## CRT CONTROLLER

In the design of the RGB-ALPHA, the 6845 CRT controller replaces many of the SSI/MSI components used in older designs and provides the RGB-ALPHA with features previously found only in the most expensive equipment. All display parameters are now user specified and displays can be configured to have virtually any combination of rows and columns up to a maximum of 4000 characters. In addition, the character cell size is variable and accomodates all commonly used character font sizes (5 x 7, 7 x 9, etc.).

## DISPLAY MEMORY

Each character position on the CRT screen corresponds to a pair of locations in the display refresh memory. The display refresh memory, 8K bytes in total, occupies 1K, 2K, 4K or 8K of system address space depending on the display size. The processor can read or write the display memory at full speed using all memory reference instructions ($t_a < 1052ns$). All accesses to the memory are "transparent". The processor can read or write the refresh memory at any time, and the display is free of "glitches".

When a character is to be displayed, its character Code and Attribute Code are written into the appropriate display memory locations. The display is "scrolled" up or down by rewriting the contents of the Display Start Address Register.

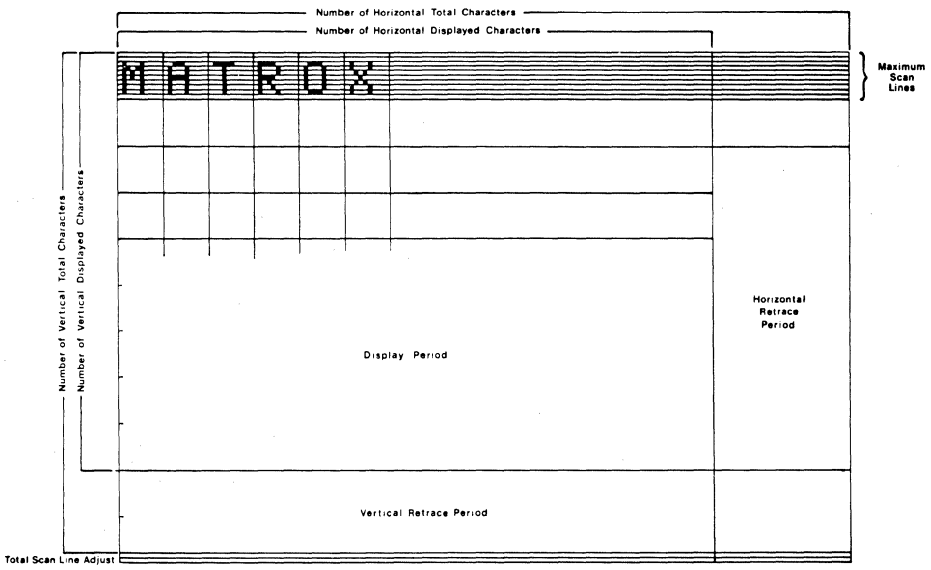



Figure 2. RGB-ALPHA display parameters

As supplied, the Character and Attribute Memories are mapped into 4K bytes of system address space and are enabled/disabled through programmed I/O commands. Two other operating modes are provided (Auto-Attribute Mode and Unified Memory Mode). When operating in the Auto-Attribute Mode, the Attribute Code is latched in the Attribute Register and is automatically written into Attribute Memory each time a Character Code is written into Character Memory. When operating in the Unified Memory Mode, all of the display refresh memory stores Character Codes. Only 1 attribute is permitted. All of the 8000 characters can be viewed by "scrolling" the display up or down.

**CHARACTER GENERATOR**
Two 24-pin DIP sockets accept up to 4K bytes of ROM/EPROM/RAM thereby permitting up to 256 different characters and symbols to be defined. When using a RAM character generator, the character font may be rewritten at any time by the processor. Read/write access to the character generator is enabled/disabled through programmed I/O commands.

As supplied, the RGB-ALPHA contains the Matrox MCH-01 character generator ROM (128 - 5 x 7 dot upper/lower case alphanumeric characters and graphic symbols). Other devices that may be used include TMS2516 (EPROM) and TMS4016 (RAM). Note that $t_a < 450$ns for displays having up to 80 characters/line and $t_a < 350$ns for displays having up to 132 characters/line.

1

**ATTRIBUTES**
Each character can be specified to be 1 of 8 foreground colors on 1 of 8 background colors. On an RGB monitor, the displayed colors are red, green, blue, cyan, magenta, yellow, black, and white. Characters may be either single or double height with character foreground and/or background normal or blinking at 2 Hz. Additionally, characters may be underlined or hidden (stored in display memory but not displayed).

**CURSOR**
An independently addressable cursor is provided. The Cursor Start and End Registers specify the scan lines in a character cell that are inverted to produce the cursor symbol. The position of the cursor on the screen is determined by the contents of the Cursor Register. The cursor blink rate is set to either 2 or 4 Hz.

**LIGHT PEN**
User-display interaction is possible through the use of a high-speed light pen. When the user points the pen at an illuminated spot on the CRT screen, the CRT loads the screen coordinates in to the Light Pen Register. The pen position may then be read by the processor. Note that the light pen can be used only with monitors having short persistence phosphors.

**KEYBOARD INTERFACE**
An 8-bit parallel keyboard interface is also provided. When a key is pressed, an interrupt is generated. The processor can read the keyboard data from the Keyboard Data Register.

**MATROX VIDEO BUS**
The RGB-ALPHA may be "slaved" to the RGB-GRAPH color graphic display controller card to provide a high-resolution graphics system with color alphanumeric overlay. All video and sync. signals required to "slave" the cards are bussed over the MATROX VIDEO BUS.

**BUS INTERFACE**
The RGB-ALPHA plugs directly into the Multibus* and works with both 8-bit and 16-bit processors using byte wide data transfers. The seven Command and Status Registers are positioned on any 8 byte I/O address boundary between 000H and FFFH. The Display Refresh Memory is positioned on any 4K memory address boundary between 00000H and FFFFFH.

**VIDEO GENERATOR**
All monochrome and RGB color video monitors work with the RGB-ALPHA. Red, Green, Blue TTL level and analog video, H. Drive, V. Drive, and composite B/W video signals are provided.

**GRAPHICS**
The RGB-ALPHA is ideal for producing character oriented graphics having a maximum resolution of 640H x 480V (interlaced) or 1024H x 240V (non-interlaced). An image is built up from graphic symbols written into the character generator RAM. Images are changed at high speed by rewritting the contents of the display memory and character generator.

**PROGRAMMING**
On power-up, all display control registers must be set, the display memory cleared and the character generator RAM, if used, loaded with the character font.

| REGISTER | ADDRESS | DESCRIPTION |
|---|---|---|
| CRTC ADDRESS | BASE + 0 | Select CRTC Register |
| CRTC DATA | BASE + 1 | CRTC Data |
| CONTROL 1 | BASE + 2 | Enable Video Ouptut/Select Character Cell Width/Select Dot Clock Frequency |
| CONTROL 2 | BASE + 3 | Enable Attributes/Enable Memory read/write |
| AUTO ATTRIBUTE | BASE + 4 | Character Attributes |
| NOT USED | BASE + 5 | — |
| KEYBOARD | BASE + 6 | Keyboard Data |
| FLAG | BASE + 7 | Keyboard Status |

Table 1. Register definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Display memory access time varies from access to access depending on when the access occurs with respect to the display refresh cycle: the worst case access time depends on the number of horizontal dots per charcter cell (see table). The best case access time is 315ns, and the average access time approaches 450ns as formats become less dense.

| HORIZONTAL DOTS/CELLS | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|
| Worst case time from MWTC/ or MRDC/ to XACK/ | 870ns | 1050ns | 1130ns | 1220ns | 960ns | 1050ns |

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTION |
|---|---|
| Resolution | 4000 characters max. |
| Horizontal Characters | 132 characters max. |
| Vertical Lines | 48 lines max. (American Standard), 52 lines max. (European Standard) |
| Character Cell Size | 6, 7, 8, 9, 10 or 11 horizontal dots (special 16 dot cell can be strap-selected) |

### VIDEO TIMING

For a display format of 80 characters by 24 lines with 5 x 7 dot characters within a 7 x 10 dot character cell an 11.667 MHz crystal is used. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 48 $\mu$s | 48 $\mu$s |
| Horizontal Sync Frequency | 15.723 KHz | 15.576 KHz |
| Horizontal Sync Width | 4.80 $\mu$s | 5.40 $\mu$s |
| Vertical Sync Frequency | 60.01 Hz | 49.92 Hz |
| Vertical Sync Width | 190.8 $\mu$s | 256.8 $\mu$s |

### INPUT SIGNALS

Light Pen: Light-pen Enable
Light-pen Strobe

Keyboard: Keyboard Data
Keyboard Strobe

### OUTPUT SIGNALS

TTL Level Video: TTL level Red
TTL level Green
TTL level Blue
Vertical Drive
Horizontal Drive

Analog Video: Red
Green (composite)
Blue
Grey Scale (composite)

### BUS INTERFACE

Address, data and control signals conform to Intel Multibus Specifications No. 9800683.
Command and Status Registers — Selectable on 8 byte I/O address boundaries 000 - FFF (098H).
Display Refresh Memory — Selectable on 4K byte memory address boundaries 00000 - FFFFF (07000H).
Keyboard Interrupt — Selectable for INTR0/ — INTR7/ (uncommitted).

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1: 86 pin edge connector, 0.156" centers | — Multibus Interface | COMPAR ESM-43-DSRI |
| J1: 10 pin right angle header | — Analog Video Outputs | AMP 87922-1 |
| J2: 10 pin right angle header | — TTL Video Outputs | AMP 87922-1 |
| J3: 50 pin right angle header | — Matrox Video Bus | Molex 15-25-4504 |
| J4: 26 pin right angle header | — Keyboard and Lightpen Interface | Molex 15-25-5103 |

## PHYSICAL

### SIZE

Width — 12.00 in. (30.48cm)
Height — 6.75 in. (17.15cm)
Depth — 0.50 in. ( 1.27cm)

### POWER REQUIREMENTS

+5V DC ±5% @2A

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

RGB-ALPHA : Color alphanumeric display controller for stand alone operation
RGB-ALPHA-SL : Color alphanumeric display controller for operation with RGB-GRAPH
X-TAL : 10.0000 MHz
X-TAL : 11.6666 MHz
} Optional crystals for special display format requirements

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# BW-ALPHA

## PROGRAMMABLE B/W ALPHANUMERIC DISPLAY CONTROLLER FOR MULTIBUS

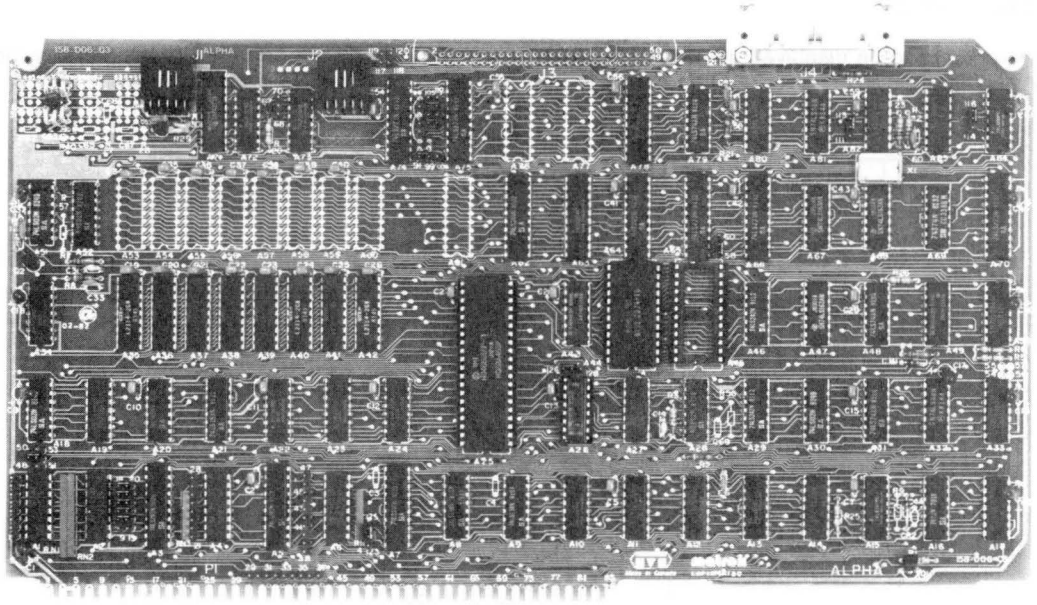
1

- User Programmed Display Format
- Up to 4000 Characters on screen
- Blink
- Inverse Video
- Underline
- Double Height Characters
- Addressable Cursor
- Multibus* Compatible
- Keyboard Interface
- Light Pen Interface
- RAM and EPROM Character Generators
- Transparent Memory
- 50 or 60 Hz Operation

The BW-ALPHA is a Multibus* compatible, video display controller card which allows the display (characters/line x lines/page) and character formats (5 x 7, 7 x 9, etc.) to be set by programmed I/O commands. Available attributes include: blink, inverse video, double height characters, underline, and foreground disable.

The character font provided with the BW-ALPHA contains 128 - 5 x 7 dot upper/lower case alphanumeric characters and graphics symbols. By adding a second character generator ROM/RAM, 128 additional symbols may be defined. When using a RAM character generator, the character font may be rewritten at any time by the system processor.

The BW-ALPHA works with all monochrome video monitors in Europe (50 Hz) and America (60 Hz). Interfaces for a high-speed light pen and an 8-bit parallel keyboard are also provided.



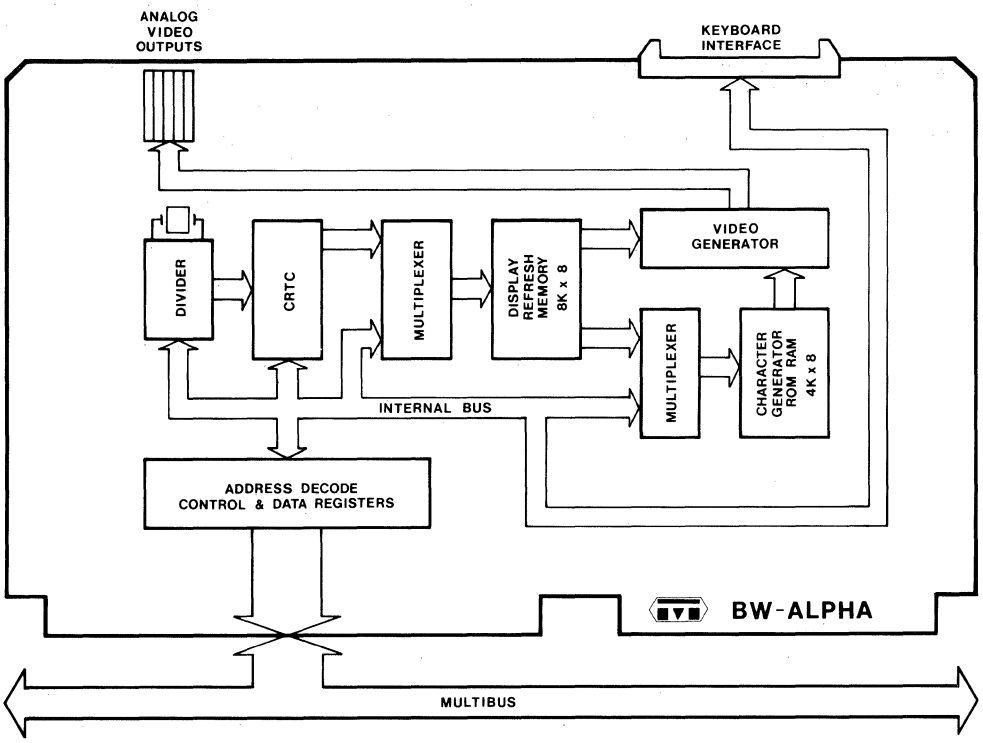



**Figure 1. BW-ALPHA block diagram**

## FUNCTIONAL DESCRIPTION

The block diagram, Figure 1, shows the major functional components of the BW-ALPHA.

## CRT CONTROLLER

In the design of the BW-ALPHA, the 6845 CRT controller replaces many of the SSI/MSI components used in older designs and provides the BW-ALPHA with features previously found only in the most expensive equipment. All display parameters are now user specified and displays can be configured to have virtually any combination of rows and columns up to a maximum of 4000 characters. In addition, the character cell size is variable and accommodates all commonly used character font sizes (5 x 7, 7 x 9, etc.).

## DISPLAY MEMORY

Each character position on the CRT screen corresponds to an 8-bit location in the display refresh memory. The display refresh memory, 4K bytes in total, occupies 1K, 2K, 4K of system address space depending on the display size. The processor can read or write the display memory at full speed using all memory reference instructions (ta<1052ns). All accesses to the memory are "transparent". The processor can read or write the refresh memory at any time, and the display is free of "glitches".

When a character is to be displayed, its Character Code is written into the appropriate display memory locations. The display is "scrolled" up or down by rewriting the contents of the Display Start Address Register.

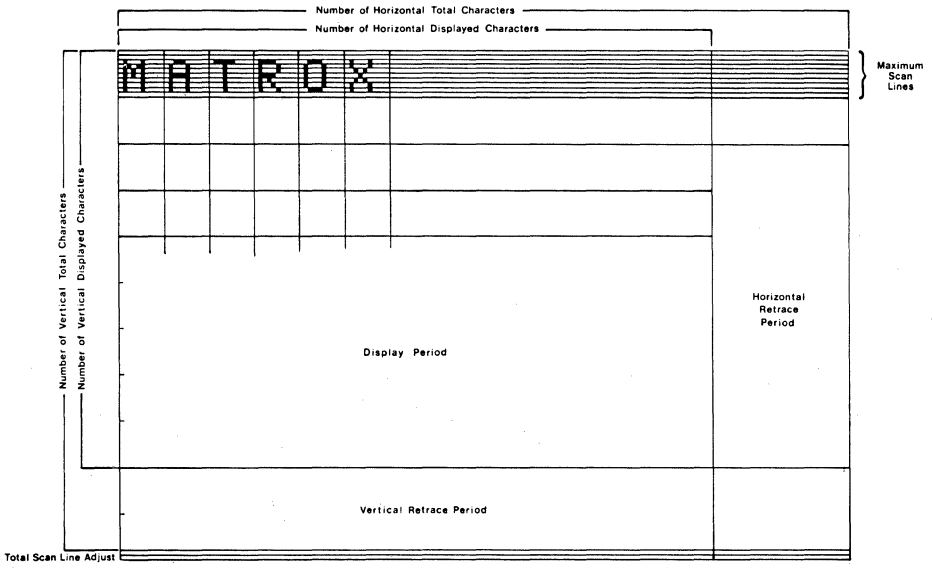



**Figure 2. BW-ALPHA display parameters**

**CHARACTER GENERATOR**
Two 24-pin DIP sockets accept up to 4K bytes of ROM/EPROM/RAM thereby permitting up to 256 different characters and symbols to be defined. When using a RAM character generator, the character font may be rewritten at any time by the processor. Read/write access to the character generator is enabled/disabled through programmed I/O commands.

As supplied, the BW-ALPHA contains the Matrox MCH-01 character generator ROM (128 - 5 x 7 dot upper/lower case alphanumeric characters and graphic symbols). Other devices that may be used include TMS2516 (EPROM) and TMS4016 (RAM). Note that $t_a < 450$ns for displays having up to 80 characters/line and $t_a < 350$ns for displays having up to 132 characters/line.

**ATTRIBUTES**
The BW-ALPHA provides five strap-selectable character attributes: inverted video, underline, extended height, blink, and foreground disable. As supplied, each character may be assigned one of these attributes which is enabled by the surplus bit in the 8-bit Character Code.

The MCH-01 character set can be reduced, by hardware straps, to produce a 64 character set comprised of the upper case alphanumeric characters only. With this reduced set one extra bit is released from the Character Code enabling the implementation of a second character attribute per character. This extra bit may be alternatively used to control the selection between the two character generators, effectively combining the two character generators as one double size unit capable of holding video information for 256 different characters.

**CURSOR**
An independently addressable cursor is provided. The Cursor Start and End Registers specify the scan lines in a character cell that are inverted to produce the cursor symbol. The position of the cursor on the screen is determined by the contents of the Cursor Register. The cursor blink rate is set to either 2 or 4 Hz.

**LIGHT PEN**
User-display interaction is possible through the use of a high-speed light pen. When the user points the pen at an illuminated spot on the CRT screen, the CRT loads the screen coordinates in to the Light Pen Register. The pen position may then be read by the processor. Note that the light pen can be used only with monitors having short persistence phosphors.

**KEYBOARD INTERFACE**
An 8-bit parallel keyboard interface is also provided. When a key is pressed, an interrupt is generated. The processor can read the keyboard data from the Keyboard Data Register.

**BUS INTERFACE**
The BW-ALPHA plugs directly into the Multibus* and works with both 8-bit and 16-bit processors using byte wide data transfers. The seven Command and Status Registers are positioned on any 8 byte I/O address boundary between 000H and FFFH. The Display Refresh Memory is positioned on any 4K memory address boundary between 00000H and FFFFFH.

**VIDEO GENERATOR**
All monochrome video monitors work with the BW-ALPHA. Composite B/W video signals are provided.

**GRAPHICS**
The BW-ALPHA is ideal for producing character oriented graphics having a maximum resolution of 640H x 480V (interlaced) or 1024H x 240V (non-interlaced). An image is built up from graphic symbols written into the character generator RAM. Images are changed at high speed by rewritting the contents of the display memory and character generator.

**PROGRAMMING**
On power-up, all display control registers must be set, the display memory cleared and the character generator RAM, if used, loaded with the character font.

| REGISTER | ADDRESS | DESCRIPTION |
|---|---|---|
| CRTC ADDRESS | BASE + 0 | Select CRTC Register |
| CRTC DATA | BASE + 1 | CRTC Data |
| CONTROL 1 | BASE + 2 | Enable video output/Select character cell width/select dot clock frequency |
| CONTROL 2 | BASE + 3 | Enable attributes/Enable memory read/write |
| NOT USED | BASE + 4 | — |
| NOT USED | BASE + 5 | — |
| KEYBOARD | BASE + 6 | Keyboard data |
| FLAG | BASE + 7 | Keyboard status |

**Table 1. Register definitions**

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Display memory access time varies depending on when the access occurs with respect to the display refresh cycle. The worst case access time depends on the number of horizontal dots per character cell (see table). The best case is 315 nsec., and the average access time approaches 450 nsec. as formats become less dense.

| HORIZONTAL DOTS/CELLS | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|
| Worst case time from MWTC/ or MRDC/ to XACK/ | 870ns | 1050ns | 1130ns | 1220ns | 960ns | 1050ns |

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTION |
|---|---|
| Resolution | 4000 characters max. |
| Horizontal Characters | 132 characters max. |
| Vertical Lines | 48 lines max. (American Standard), 52 lines max. (European Standard) |
| Character Cell Size | 6, 7, 8, 9, 10 or 11 horizontal dots (special 16 dot cell can be strap-selected) |

### VIDEO TIMING

For a display format of 80 characters by 24 lines with 5 x 7 dot characters within a 7 x 10 dot character cell an 11.667 MHz crystal is used. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 48 $\mu$s | 48 $\mu$s |
| Horizontal Sync Frequency | 15.723 KHz | 15.576 KHz |
| Horizontal Sync Width | 4.80 $\mu$s | 5.40 $\mu$s |
| Vertical Sync Frequency | 60.01 Hz | 49.92 Hz |
| Vertical Sync Width | 190.8 $\mu$s | 256.8 $\mu$s |

### INPUT SIGNALS

Light Pen: Light-pen enable
Light-pen strobe
Keyboard: Keyboard data
Keyboard strobe

### OUTPUT SIGNALS

Composite Analog Video

### BUS INTERFACE

Address, data and control signals conform to Intel Multibus Specification No. 9800683.
Command and Status Registers — Selectable on 8 byte I/O address boundaries 000-FFF (098H).
Display Refresh Memory — Selectable on 4K byte memory address boundaries 00000-FFFFF (07000H).
Keyboard Interrupt — Selectable for INTR0/ — INTR7/ (uncommitted).

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 86 pin edge connector, 0.156" centers, Multibus Interface | COMPAR ESM-43-DSRI |
| J1: 10 pin right angle header, composite video outputs | AMP 87922-1 |
| J4: 26 pin right angle header, Keyboard and lightpen interface | MOLEX 15-25-4264 |

## PHYSICAL

### SIZE

Width — 12.00 in. (30.48cm)
Height — 6.75 in. (17.15cm)
Depth — 0.50 in. ( 1.27cm)

### POWER REQUIREMENTS

+5V DC ±5% @2A

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

BW-ALPHA : B/W alphanumeric display controller for stand alone operation
BW-ALPHA-SL: B/W alphanumeric controller For slave lock operation with RGB-GRAPH

X-TAL : 10.0000 MHz
X-TAL : 11.6666 MHz
} Optional crystals for special display format requirements

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MSBC-QV3

## QUAD COLOR ALPHANUMERIC DISPLAY CONTROLLER FOR MULTIBUS

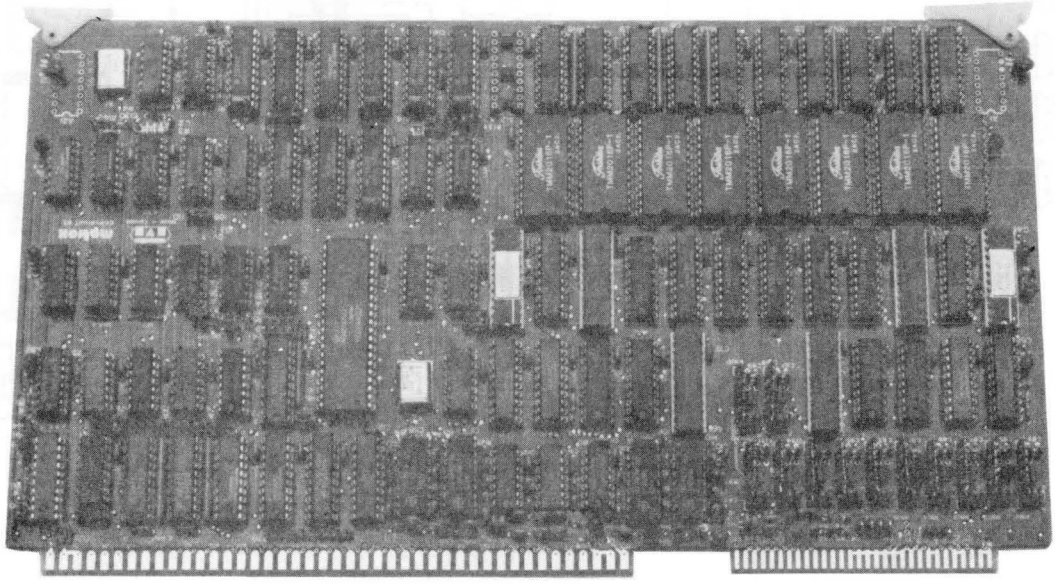


- **Four independent displays**
- **Programmable display format**
- **256 displayable colors**
- **Hardware scroll**
- **Underline and blink attributes**
- **128 ASCII character set**
- **Four DTMF keyboard interfaces**
- **Multibus compatible**
- **RS-330 video outputs**
- **Transparent memory**
- **20-bit address decoding**
- **American or European operation**

The Matrox MSBC-QV3 is a programmable color alphanumeric display controller which supports four independent displays. Display formats (characters per line and lines per page) are user definable to a maximum of 2000 characters per display. Powerful color manipulation capabilities are incorporated on-board which allows the user to independently select the color of the background, foreground, and underline components of each displayed character. Each of these components can also be programmed to blink to a different color.

The MSBC-QV3 features a Copy command which enables the user to copy the contents of one display memory into another display memory. Another on-board hardware feature allows the user to change his view (displayed image on his screen) from one display memory to another, without effecting the contents of either display memory.

The MSBC-QV3 generates RS-330 video signals capable of driving most standard RGB video display monitors. Sync signals generated by the MSBC-QV3 are user programmable to enable the board to operate in either American or European environments. Four separate DTMF keyboard interfaces are also supported on-board.



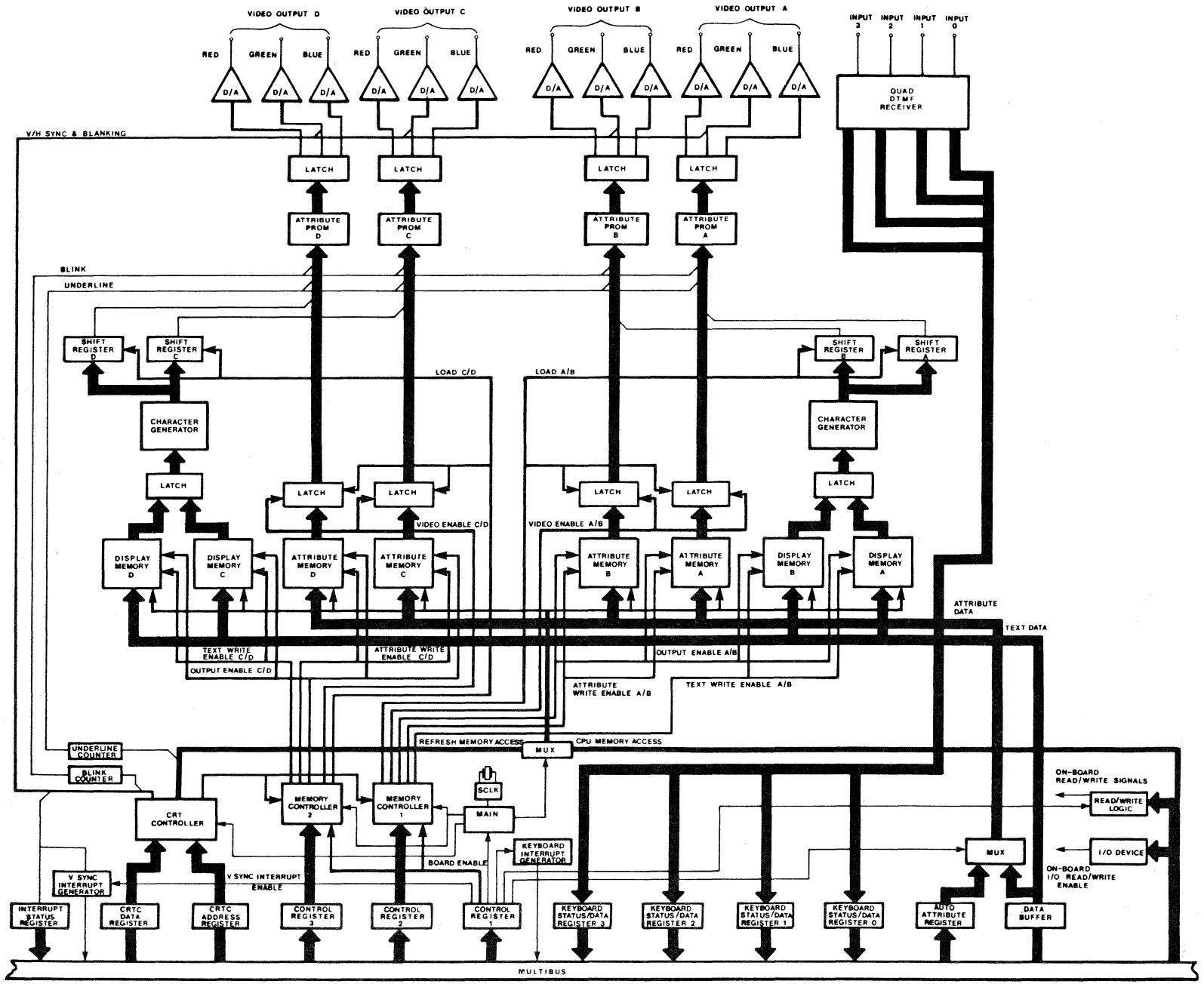



Figure 1. MSBC-QV3 block diagram

# MSBC-QV3 FEATURES



**Quad Displays:** The MSBC-QV3 generates four independent color alphanumeric displays on four separate CRT monitors.

**Programmable Formats:** The display format used by the MSBC-QV3 (i.e. characters/line and lines/page) is user programmable via software. Any format using up to 2000 characters can be accomodated. The standard display format is 80 characters on 24 (25) lines.

**Video Attributes:** On-board attribute memory stores 7 bits of attribute code per character. Video attributes include foreground and background color selection, underline, and blink. A color look-up PROM selects foreground, background, and underline colors from a pallette of 256 possible colors. The look-up table also defines to what color the foreground, background, and underline will blink. A total of 127 attribute color combinations are available for each character.

**Character Generator:** The MSBC-QV3 is supplied with 128 characters, including upper and lower case alphanumeric characters and 32 special graphics symbols.

**Copy:** The MSBC-QV3 allows the user to transfer data from one display memory to another display memory using a single I/O command. Copy operations are completely transparent to the host CPU and normal read/write operations to the display RAMs not involved in the COPY are not impeded.

**Change Display:** Users can select which display memory will be viewed on his particular CRT screen. For example, User A can select, using a single command, to view display memory B. Change Display operations do not effect the contents of either of the involved display memories.

**Keyboard Interface:** The MSBC-QV3 accepts tone-encoded DTMF data from four separate external keyboards. On-board receivers decode this information and provide 4-bit binary data which can be read by the system processor. The Matrox KB-16 keyboard can be used to generate the DTMF signals.

**Multibus Interface:** The MSBC-QV3 plugs directly into the Multibus. The board occupies a 4K byte block of system memory and is controlled via 11 I/O registers which reside on any 8 consecutive I/O locations.

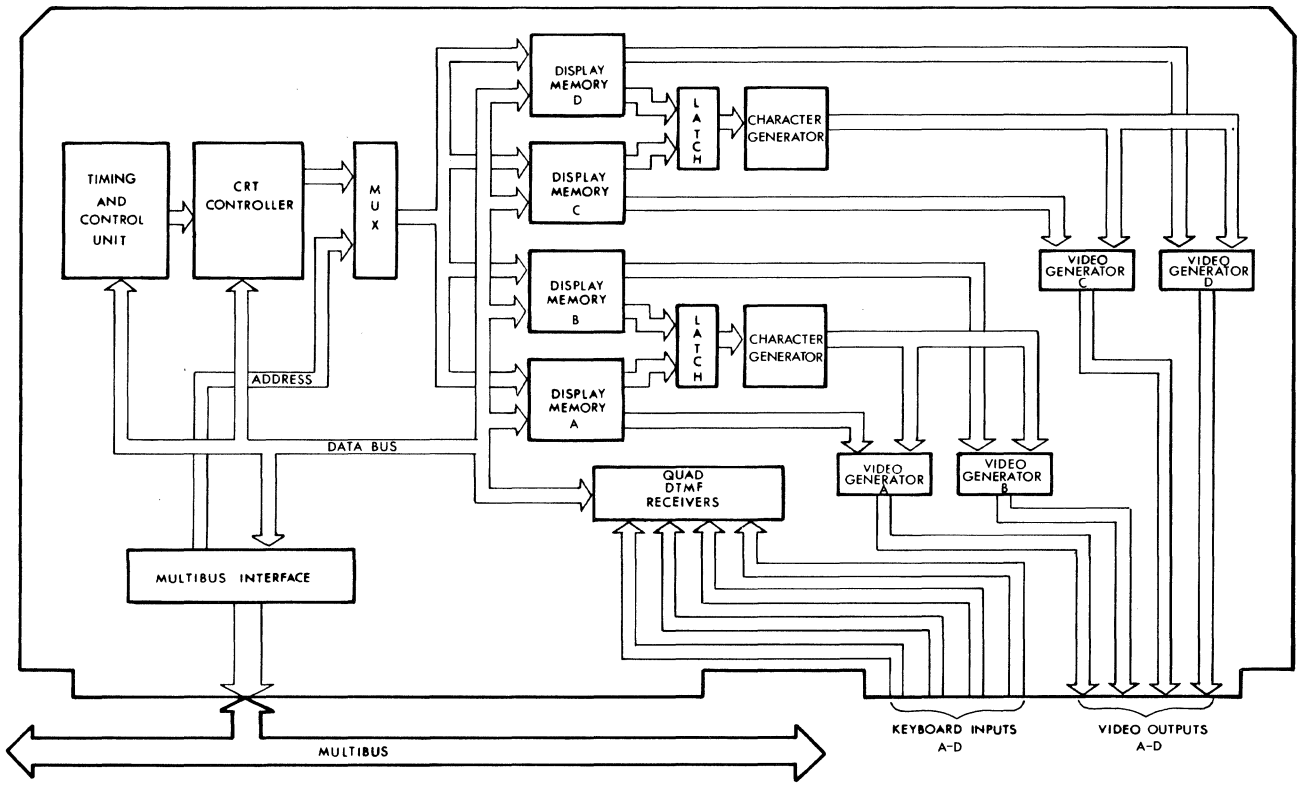



Figure 2. MSBC-QV3 functional blocks

## GENERAL DESCRIPTION

Contained on a single Multibus standard PCB (12.0" x 6.75"), the MSBC-QV3 is a sophisticated color alphanumerics display system capable of controlling up to four independent displays. Powerful on-board color manipulation techniques yield advanced character highlighting capabilities.

The MSBC-QV3 is made up of seven functional blocks: Display Memory, CRT Controller, Character Generators, Video Generators, Timing and Control Unit, Keyboard Interface, and Multibus Interface. These functional blocks are outlined in figure 2.

## CRT CONTROLLER

The MSBC-QV3 uses one single-chip CRT Controller to generate all of the required video timing signals for all four of the video displays. This VLSI IC provides the horizontal and vertical sync and blanking signals, and display refresh RAM addressing signals. The CRT Controller is software programmable, allowing the user to define parameters such as vertical refresh frequency, width and position of the horizontal and vertical sync pulses (important when using non-standard monitors), display resolution, etc. To the Multibus, the CRT Controller appears as an array of 18 registers which are indirectly accessed via a pair of I/O locations.

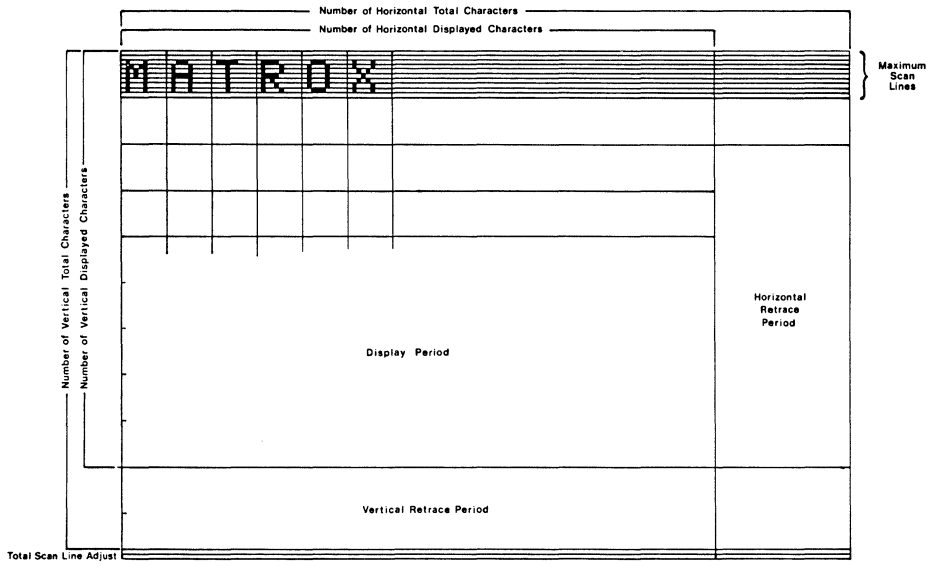



Figure 3. Display parameters

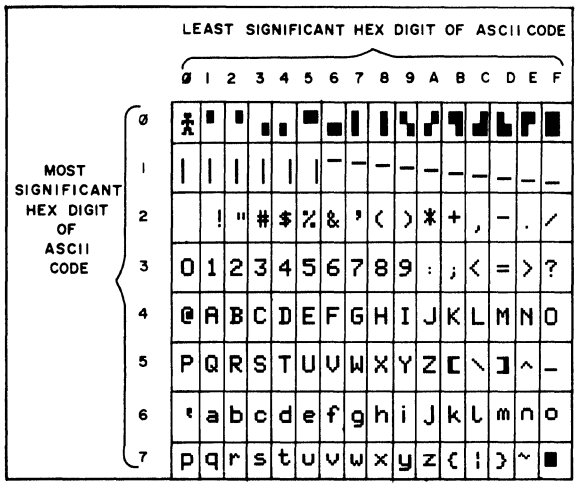



Figure 4. MSBC-QV3 character set

The CRT Controller allows the user to define the display parameters (horizontal characters/line, vertical lines/field, etc.) under software control. Due to memory access timing requirements, display formats are limited to a maximum of 80 characters per line on up to 25 lines per field. Note that all four displays must be programmed for the same display format.

## DISPLAY MEMORY

The MSBC-QV3 contains 16K bytes of on-board read/write display memory. This RAM memory is divided into four 4K byte blocks, each of which corresponds to a separate display. These 4K blocks are further divided into a 2K byte character text memory and a 2K byte attribute memory. The four MSBC-QV3 display memories are mapped into a single 4K byte block of system memory, which is strap-locatable on any 4K byte boundary in the 1M byte Multibus memory address space. The host CPU selects, via programmed I/O, which of the four displays is enabled for read/write access from the Multibus. Multibus access to the MSBC-QV3 can be disabled through software. This feature makes the MSBC-QV3 transparent to the host processor and enables multiple boards to occupy the same memory address space.

Each character position on the CRT screen corresponds to a unique 8-bit location in the 2K character text memory. When a character is to be displayed, its ASCII Character Code is written into the appropriate memory location. The desired Attribute Code, for that character, is then written to the corresponding location in the attribute memory.

The attribute memory can be accessed in one of two modes. Normally, the attribute memory appears as 2K bytes of RAM, where an attribute is located at an address 2048 bytes above the corresponding character byte. Optionally the attribute can be stored in an I/O latch (Auto-Attribute Register). Whenever a character is written to the character memory, the stored attribute is automatically copied into the appropriate attribute memory location. A single attribute latch is used for all four video channels. The Auto-Attribute Mode is enabled via programmed I/O.

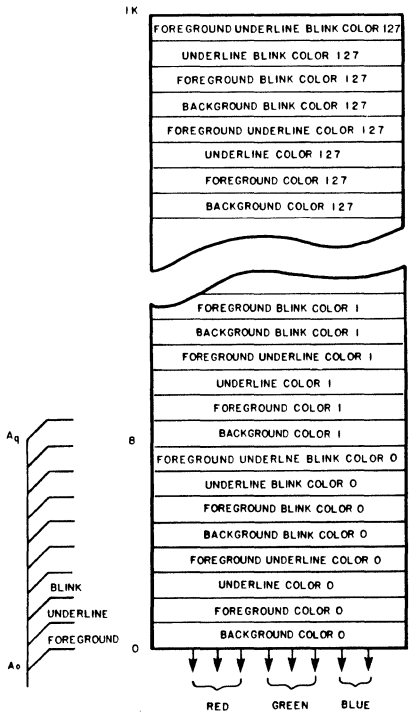
In addition to the CPU read/write, the display memory (character memory and attribute memory) is continually scanned by the CRTC every 16.66ms (in 60 Hz systems) to generate video signals. Memory access arbitration circuitry on the MSBC-QV3 efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display refresh is "transparent" to the user.

## CHARACTER GENERATOR

The MSBC-QV3 uses the Matrox MCH-01 character generator. This 24 pin DIP IC chip contains all the necessary video information required to generate a 128 character set. This character set consists of all the upper and lower case alphanumerics characters plus 32 special graphics symbols to permit the generation of limited graphics displays (eg. bar charts, trend displays, etc.). Alphanumeric characters are formed in a 5 x 7 dot matrix built up within a 7 x 10 dot character cell. The MSBC-QV3 can also support an optional 8 x 10 dot character cell.

## VIDEO GENERATOR

The MSBC-QV3 video generator processes the textual data from the text memory (via the character generator) adds color attributes and produces the output video signals which are RS-330 compatible. Each channel (display) of the MSBC-QV3 drives 8 levels of red, 8 levels of green, and 4 levels of blue, for a total of 256 possible displayable colors. Sync and blanking signals are composite on the green drive. Each video channel can also be enabled or disabled through programmed I/O.




Note: Attribute color combination 0 is reserved. All locations in this combination are set to black and are used, by the MSBC-QV3 for blanking.

Figure 6. Attribute PROM architecture

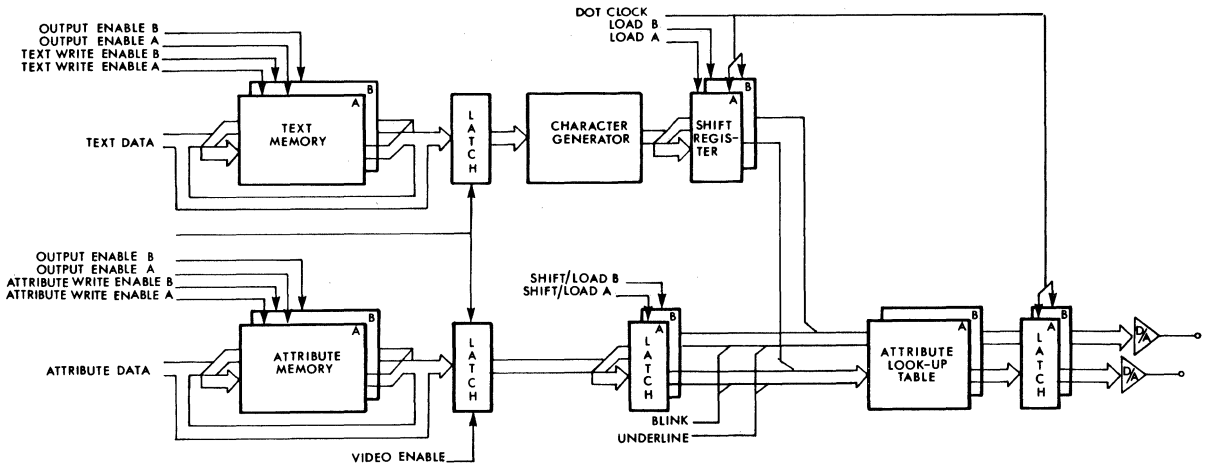



Figure 5. Video generator

**Attributes** — The MSBC-QV3 utilizes 1K byte look-up PROMS (one for each of the four display channels) for powerful color manipulation. Each look-up table is divided into 128 blocks (figure 6), each of which contains the color information for the background, foreground (character), underline, and underline over foreground. Each block also contains the color information to which each of these display components (i.e. foreground, background, underline, etc.) will blink. In this way each component can be set to blink to a separate color. The seven least significant bits from the attribute memory byte allow the color combination information for each character position to be individually selected from 127 available combinations.

**Copy** — The MSBC-QV3 features the capability to copy the contents of one display memory into another display memory with a single instruction. Internally, the MSBC-QV3 groups the four display channels into two groups of two channels each (A, B and C, D). Memory contents can be copied within each group with the direction of the copy operation being user defined.

The Copy operation is completely transparent to the user and does not effect or inhibit normal CPU accesses to the MSBC-QV3. Using signals generated internally (figure 5), the Copy command enables the output of the source memory while simultaneously write enabling the destination memory. In this way, while the CRT Controller reads the source memory to the screen (for CRT refresh), the destination memory is being written to, using this same data.

**Change Display** — Another feature of the MSBC-QV3 allows the user to select which display memory of the two channel group (i.e. A or B, C or D) is used to produce the display on his screen. Changing views from one display memory to another does not effect the display memory, but merely selects from which memory the screen refresh data will be taken.

## TIMING AND CONTROL UNIT

The MSBC-QV3's Timing and Control Unit synchronizes the operation of the various functional blocks on the board and generates most of the internal timing signals required by the board. This proprietary Matrox circuitry manages access to the display memory, between CPU read/write and display refresh, and times the display refresh so that each display is updated without interference from any of the other displays. The unique Matrox "transparent memory refresh" feature allows the CPU to read/write the display memory at any time, using all memory reference instructions, without causing snow on the screen.

## KEYBOARD INTERFACE

The MSBC-QV3 includes four keyboard interface channels. Each interface accepts tone-encoded (DTMF) data from an external keyboard and converts this signal into the 4-bit binary code representative of the depressed key (table 1). Keyboards can be located up to 500 feet from the MSBC-QV3.

Each keyboard interface includes an associated 8-bit I/O register which can be read by the CPU. The four least significant bits in these registers contain the keyboard data for the corresponding keyboard, while the four most significant bits specify which keyboard is requesting service. The MSBC-QV3 will generate an interrupt whenever data is available at any of the four keyboard channels.

## MULTIBUS INTERFACE

The MSBC-QV3 plugs directly into the Multibus backplane and conforms to the IEEE-796 (Multibus) bus specification. To the host processor, the MSBC-QV3 looks like a single 4K byte block of RAM located in system memory. This RAM memory can be located, by on-board hardware straps, on any 4K byte boundary in the available system memory space. The board also occupies 8 I/O locations which represent 11 control and

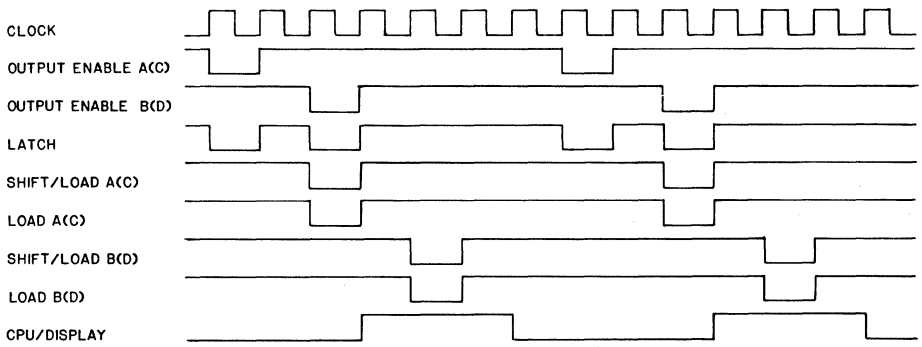



Figure 7. Video timing diagram

| KEYBOARD CHARACTER | KEYBOARD REGISTER DATA | | | |
|---|---|---|---|---|
| | BIT 4 | BIT 3 | BIT 2 | BIT 1 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| * | 1 | 0 | 1 | 1 |
| # | 1 | 1 | 0 | 0 |
| A | 1 | 1 | 0 | 1 |
| B | 1 | 1 | 1 | 0 |
| C | 1 | 1 | 1 | 1 |
| D | 0 | 0 | 0 | 0 |

Table 1. DTMF character codes

status registers. The MSBC-QV3 decodes 20 bits of memory address and 8 or 16 bits of I/O address.

A software disable feature enables multiple MSBC-QV3 boards to occupy the same space in system memory, each board only requiring separate I/O addressing. A special provision has also been incorporated onto the MSBC-QV3 to enable several boards, which occupy the same memory space, to be written to simultaneously.

## PROGRAMMING

On power-up and reset, the MSBC-QV3 automatically resets all on-board control and status registers. To program these boards the user loads these registers with the appropriate parameters (table 2). Two of these control registers, CRTC Data Register and CRTC Address Register are used to indirectly access a further 18 register, located in the CRT Controller.



| NAME | DIRECTION | ADDRESS | FUNCTION |
|---|---|---|---|
| Auto-Attribute | WRITE ONLY | BASE + 0 | Attribute data for auto-loading to attribute memory |
| Keyboard 0 | READ ONLY | BASE + 0 | Keyboard data 0/Keyboard status |
| Control 1 | WRITE ONLY | BASE + 1 | Select screen to read/Enable keyboard interrupt/Enable sync interrupt/Select 80 column mode/Enable Auto-Attribute mode/ Enable on-board memory |
| Keyboard 1 | READ ONLY | BASE + 1 | Keyboard data 1/Keyboard status |
| Control 2 | WRITE ONLY | BASE + 2 | Select display channel to write to (A/B)/Enable video (A/B)/Set Copy direction (A/B)/Execute Copy function (A/B)/Execute Change Display function (A/B)/Write Enable (A/B) |
| Keyboard 2 | READ ONLY | BASE + 2 | Keyboard data 2/Keyboard status |
| Control 3 | WRITE ONLY | BASE + 3 | Select display channel to write to (C/D)/Enable video (C/D)/Set Copy direction (C/D)/Execute Copy function (C/D)/Execute Change Display function (C/D)/Write Enable (C/D) |
| Keyboard 3 | READ ONLY | BASE + 3 | Keyboard data 3/Keyboard status |
| Interrupt Status | READ ONLY | BASE + 4 | Vertical sync interrupt flag/Vertical sync flag/Blanking Flag |
| CRTC Address | WRITE ONLY | BASE + 6 | Address to one of 16 internal CRTC registers |
| CRTC Data | WRITE ONLY | BASE + 7 | Data to internal CRTC register pointed to by CRTC Address Register |

Table 2. Register definitions

# SPECIFICATIONS

## FUNCTIONAL

### ACCESS TIME

Access time to all on-board I/O locations is fixed at 600ns.

The display memory access time varies from access to access depending on when the access is initiated with respect to the display refresh cycle. The worst case access time is 1.5μs.

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Resolution | 8000 characters total (2K character x 4 displays) |
| Horizontal Characters | 80 characters max. |
| Vertical Lines | 25 lines max. |
| Character Cell Size | 7 x 10 dots or 8 x 10 dots (strap-selectable) |

### VIDEO TIMING

For a display format of 80 characters x 24 lines using a 7 x 10 dot character cell, an 11.66 MHz crystal is used. The following table gives the video timing parameters required for this format for both American and European standard systems. Note that these parameters are programmable, through the CRT Controller, and must be defined by the user on power-up.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active video | 48μs | 48μs |
| Horizontal Sync Frequency | 15.723KHz | 15.576KHz |
| Horizontal Sync Width | 4.80μs | 5.40μs |
| Vertical Sync Frequency | 60.01Hz | 49.92Hz |
| Vertical Sync Width | 190.8μs | 256.8μs |

### INPUT SIGNALS

KEYBOARD — 4 channels of balanced power/signal lines
— keyboards may be located up to 500 ft.

### OUTPUT SIGNALS

VIDEO — Red, Green, and Blue video for each channel
— RS-330, 1.0Vp-p into 75 ohms
— Sync signals are composite on the Green video

### BUS INTERFACE

Address, data, and control signals conform to the IEEE-796 (Multibus) bus specification

Command and Status Registers — Selectable on any 8 byte I/O address boundary 0000H — FFFFH
Display Refresh Memory — Selectable on any 4K byte memory address boundary 00000H — FFFFFH

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1: 86 pin edge connector, 0.156" centers | — Multibus Interface | COMPAR ESM-43-DSRI |
| P2: 60 pin edge connector, 0.156" centers | — Video Interface<br>— Keyboard Interface | MOLEX 15-25-8601 |

## PHYSICAL

### SIZE

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5% @ 4.5A
+12V DC ±5% @ 150mA

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature — 0°C to 50°C
Relative Humidity — 0% to 95% non-condensing

### ORDERING INFORMATION

MSBC-QV3/11/X/55/54 — Quad color alphanumeric video display controller (7 x 10 cell)

X:
0 — No DTMF decoders
1 — Complete with 4 DTMF decoders

### SUPPORT PRODUCTS

XTAL: 12.8 MHz (must be ordered for 8 x 10 character cell)

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MSBC QV-2

## QUAD PROGRAMMABLE B/W ALPHANUMERIC CONTROLLER FOR MULTIBUS

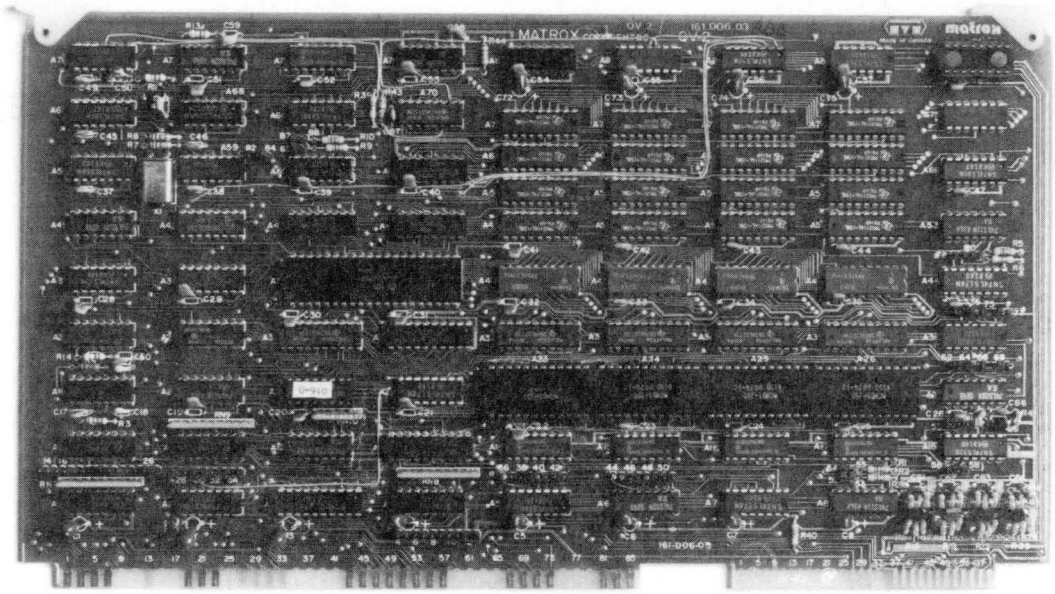
1

- Four independent displays
- User programmable display format
- Up to 132 characters per line
- Up to 52 lines per page
- Variable character cell sizes
- Hardware scroll
- Underline, blink and inverse video
- 128 ASCII character set
- Composite and TTL video outputs
- 8K byte memory-mapped display memory
- Multibus* compatible
- Single +5V supply
- American or European operation
- Transparent memory
- 20 bit address decoding

The MSBC-QV2 generates four separate video displays on four separate monitors. The number of character per line, number of lines, inter-character spacing, interline spacing, character height, etc. are all user programmable.

The on-board character generators provide 128 - 5 x 7 upper/lower case alphanumeric characters and graphic symbols. Each character can be displayed as normal (white on a black background), inverted (black on white), or blinking at 2 or 4 Hz.

Four separate composite and TTL video signals as well as TTL sync/drive outputs are available on-board. The MSBC-QV2 works with all monochrome video monitors in Europe (50 Hz) and America (60 Hz).



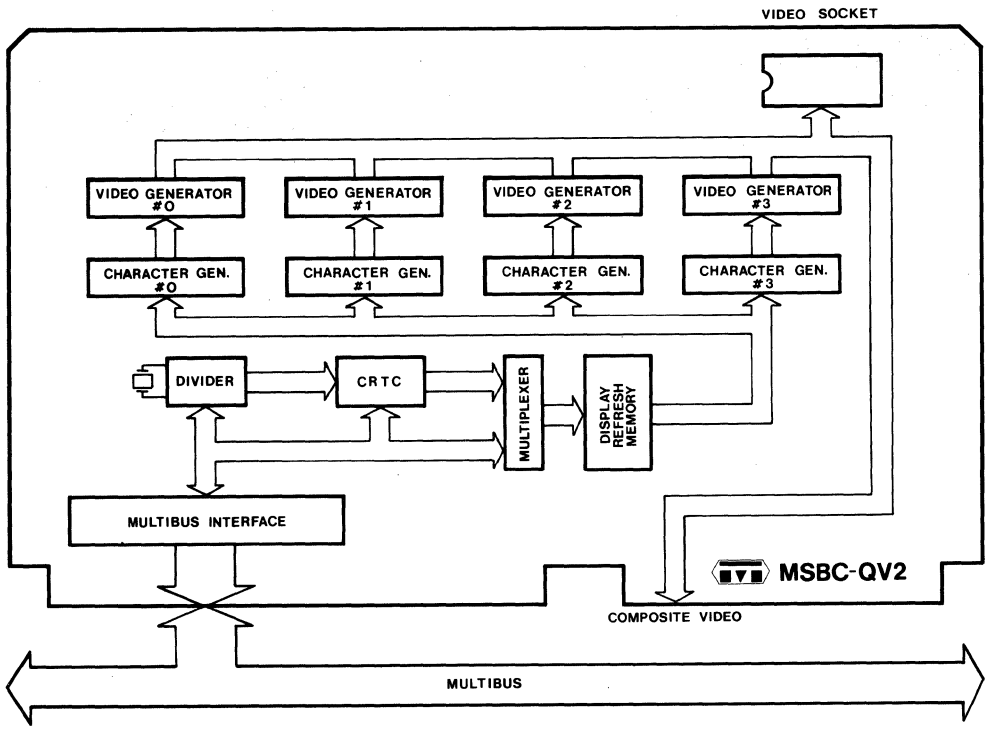



Figure 1. MSBC-QV2 block diagram

## FUNCTIONAL DESCRIPTION

The MSBC-QV2 is functionally divided into five major operational blocks: The CRT Controller, the Display Memory, the Character Generator, and the Multibus Interface. These five blocks are shown in figure 1.

## CRT CONTROLLER

The MSBC-QV2 uses one single chip CRT controller to generate all the required timing and control signals for all four displays. This VLSI IC replaces many of the SSI/MSI components used in earlier designs and provides the MSBC-QV2 with features that have previously been found only in the most expensive video display equipment.

The CRT controller allows the user to define the display parameters (horizontal characters per line, vertical lines per field, etc.) under software control. Virtually any display format can be programmed on the MSBC-QV2, limited only by the size of the display memory and the monitor specifications. For most standard CRT monitors, formats of up to 132 characters per line or up to 52 lines per field can be accommodated. In addition the character cell size is variable and accommodates all commonly used character font sizes (5 x 7, 7 x 9, etc.). Note that all four displays must use the same display format.

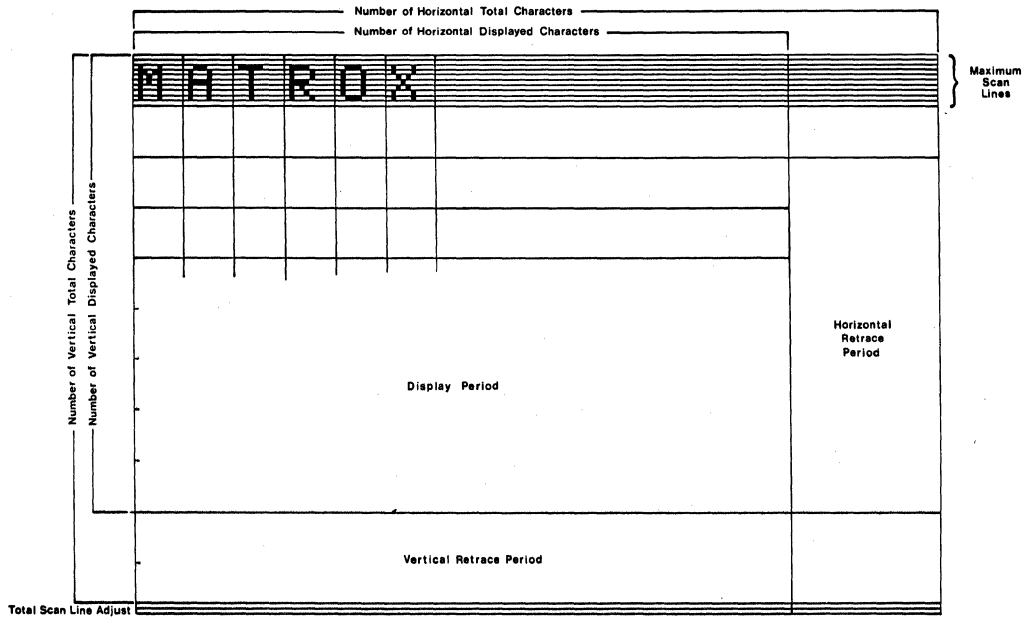



Figure 2. Display Parameters

**DISPLAY MEMORY**
The MSBC-QV2 contains a two port display memory that can be accessed by either the CRT controller, for display refresh, or by the CPU, for text manipulation. During display refresh the display memory is accessed as four 2K blocks of RAM that are addressed in parallel, by the CRT controller, for simultaneous updating of all four displays. When an external access occurs, the display memory appears as 8K bytes of contiguous RAM, strap-locatable to any 8K boundary in system address space. During CPU accesses the display memory is masked from the display to prevent streaking on the display. External accesses to the display memory can be disabled, through software, permitting more than one board to occupy the same space in the system memory.

Each character position on the CRT screen corresponds to a unique 8-bit location in the display refresh memory. When a character is to be displayed, its ASCII Character Code is written into the appropriate memory location. The processor can read/write the display memory at full speed using all memory reference instructions.

As supplied, the MSBC-QV2's display memory is arranged to generate four displays, each with a maximum resolution of 2048 characters. For larger displays the display memory can be arranged, via hardware straps, so as to produce two displays of 4096 characters per display.



**SCROLL**
The four displays can be simulanteously scrolled up or down to permit viewing of the entire display memory. Scrolling is acheived by rewriting the contents of the Display Start Address Register, contained within the CRT controller.

**CHARACTER GENERATOR**
As supplied, the MSBC-QV2 contains the MCH-01 character generator. This 24 pin DIP IC chip contains the necessary binary video information required to generate a 128 character set. This character set consists of all the upper/lower case alphanumeric characters plus special graphic characters to permit the generation of limited graphic displays. The alphanumeric characters are formed in a 5 x 7 dot matrix built up within a variable-sized character cell (the size of the character cell is software programmable through the CRT controller). The QV2 provides 4 different character heights so that proper character proportions can be maintained for both large and small formats. Normal, double, triple, and quadruple height characters can be programmed via the Control Register and these heights are halved in the interlace mode.

The MCH-01 character generator is pin-compatible with the 2516 EPROM. In this way the user can easily implement his own custom character font by simply replacing the MCH-01 with an EPROM loaded with the desired font.

**ATTRIBUTES**
Circuits for three different character attributes (blink, inverse video, and underline) are incorporated on-board the MSBC-QV2. These attributes are enabled/disabled by the surplus eighth bit in the ASCII Character Code. As supplied, one character attribute can be strap selected for each display. However the character generator can be hardware strapped to produce a reduced 64 character set, consisting of the upper case alphanumeric characters only. In this way an extra bit is released from the Character Code, thereby permitting the selection of an additional character attribute per display.

**BUS INTERFACE**
The MSBC-QV2 plugs directly into the Multibus and works with both 8-bit and 16-bit processors using byte wide data transfers. Although the QV2 occupies 8 I/O locations, only the four even locations are actually used. This is done to facilitate the use of 16-bit CPUs. The I/O registers can be strapped to reside at any 8 byte I/O address boundary between 000H and FFFH. The display refresh memory can be positioned on any 8K byte system memory address boundary between 00000H and FFFFFH.

**VIDEO GENERATOR**
There are four independent video generators on-board the MSBC-QV2. Both TTL level and composite analog video output signals are supported. Separate horizontal and vertical sync as well as composite sync signals are also provided. Note that the sync ports are bi-directional to enable the user to slave the QV2 to an external sync source.

**PROGRAMMING**
The MSBC-QV2 is programmed through 4 directly accessable I/O registers. Two of these registers (CRTC Address Register and CRTC Data Register) allow the user to access another 18 registers within the CRT controller, to specify the display format parameters. On power-up, all display control registers must be set and the display memory cleared. Register definitions for the four directly addressable I/O ports are given in Table 1.

| REGISTER | ADDRESS | DESCRIPTION |
|---|---|---|
| CRTC ADDRESS | BASE + 0 | Select CRTC register |
| CRTC DATA | BASE + 2 | CRTC data |
| CONTROL 1 | BASE + 4 | Enable memory/Select character cell width/Select dot clock frequency |
| CONTROL 2 | BASE + 6 | Enable Video 1/Enable Video 2/Enable Video 3/Enable Video 4/Select character height |

Table 2. Register Definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

The display memory access time varies from access to access depending on when the access is initiated with respect to the display refresh cycle. The best case access time is 225 nsec., while the worst case access time depends on the number of horizontal dots per character cell (see table)

| HORIZONTAL DOTS/CELLS | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|
| Worst case time from MRDC/ or MWTC/ to XACK/ | 678ns | 818ns | 888ns | 957ns | 748ns | 818ns |



### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Resolution | 8000 characters total (2K characters x 4 displays/4K characters x 2 displays) |
| Horizontal Characters | 132 characters max. |
| Vertical Lines | 48 lines max. (American Standard), 52 lines max. (European Standard) |
| Character Cell Size | 6, 7, 8, 9, 10 or 11 horizontal dots |

### VIDEO TIMING

For a display format of 80 characters by 25 lines with 5 x 7 dot characters within a 7 x 10 dot character cell a 14.381 MHz crystal was used. The following table gives the video timing in both American and European standards. Note that these timing parameters are programmable, through the CRT controller, and must therefore be defined by the user on power-up.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 39.11 $\mu$s | 39.11 $\mu$s |
| Horizontal Sync Frequency | 15.77 KHz | 15.77 KHz |
| Horizontal Sync Width | 4.87 $\mu$s | 5.85 $\mu$s |
| Vertical Sync Frequency | 59.96 Hz | 50.06 Hz |
| Vertical Sync Width | 190.23 $\mu$s | 190.23 $\mu$s |

### INPUT SIGNALS

4 x TTL Video
4 x Composite Video
4 x Horizontal/Vertical Sync

### BUS INTERFACE

Address, data and control signals conform to Intel Multibus Specification No. 9800693
Command and Status Registers — Selectable on any 8 byte I/O address boundary 000-FFFH (088H)
Display Refresh Memory — Selectable on any 8K memory address boundary 00000-FFFFFH (06000H)

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 86 pin edge connector, 0.156" centers — Multibus Interface | COMPAR ESM-43-DSRI |
| J1: 60 pin edge connector, 0.156" centers — Composite/TTL Video | MOLEX 15-25-8601 |
| V: 16 pin DIP socket — Video Expansion Socket | AUGAT 516-A6-37D |

### PHYSICAL

**SIZE**

Width — 12.00 in. (30.48cm)
Height — 6.75 in. (17.15cm)
Depth — 0.50 in. ( 1.27cm)

**POWER REQUIREMENTS**

5V DC ±5% @2A

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

MSBC-QV2 : Programmable format quad video controller

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MSBC-2480

## 24 x 80 ALPHANUMERIC DISPLAY CONTROLLER FOR MULTIBUS

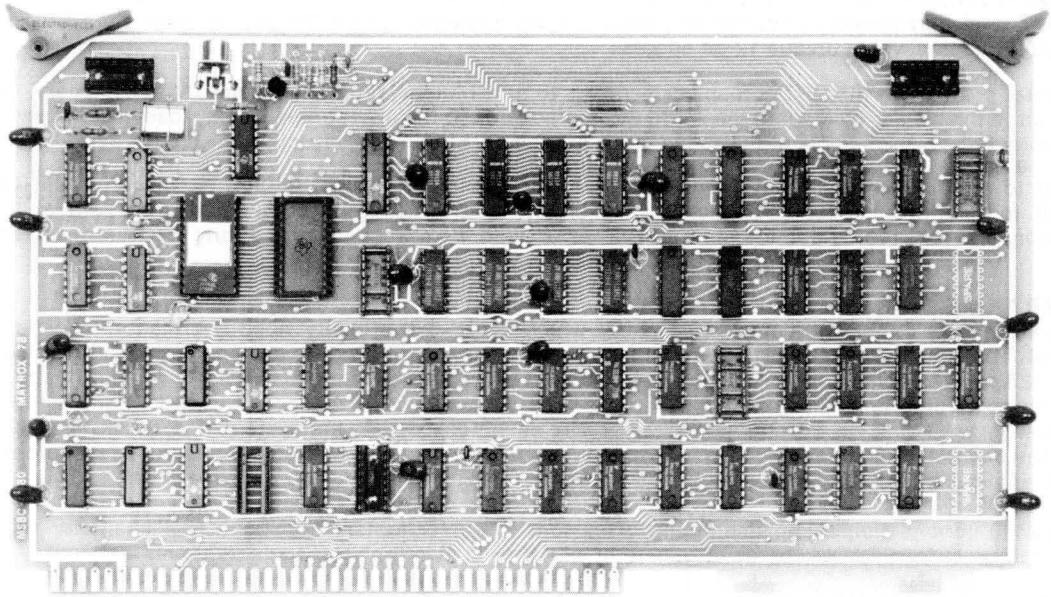
1

- **24 row x 80 column alphanumeric video display**
- **32 x 80 display memory**
- **Normal, inverse, blink attributes**
- **Hardware scroll**
- **EPROM ASCII character generator**
- **4K byte memory-mapped display**
- **Transparent memory access**
- **Multibus compatible**
- **Directly drives any monochrome monitor**
- **On-board ASCII keyboard interface**
- **Single +5V supply**
- **External/internal sync capability**
- **Decodes full 20 address lines**

The MSBC-2480 is a Multibus compatible alphanumeric display controller which is capable of generating displays of 24 lines of 80 charactres per line. Characters can be displayed as either white on a black background or black on a white background. Each character can also be set to blink under software control.

The character font provided with the MSBC-2480 contains 128 - 5 x 7 upper/lower case alphanumeric characters and graphic symbols. The character generator is user-programmable, allowing the user to implement his own custom character font.

The MSBC-2480 works with all standard monochrome video monitors in Europe (50 Hz) and America (60 Hz).



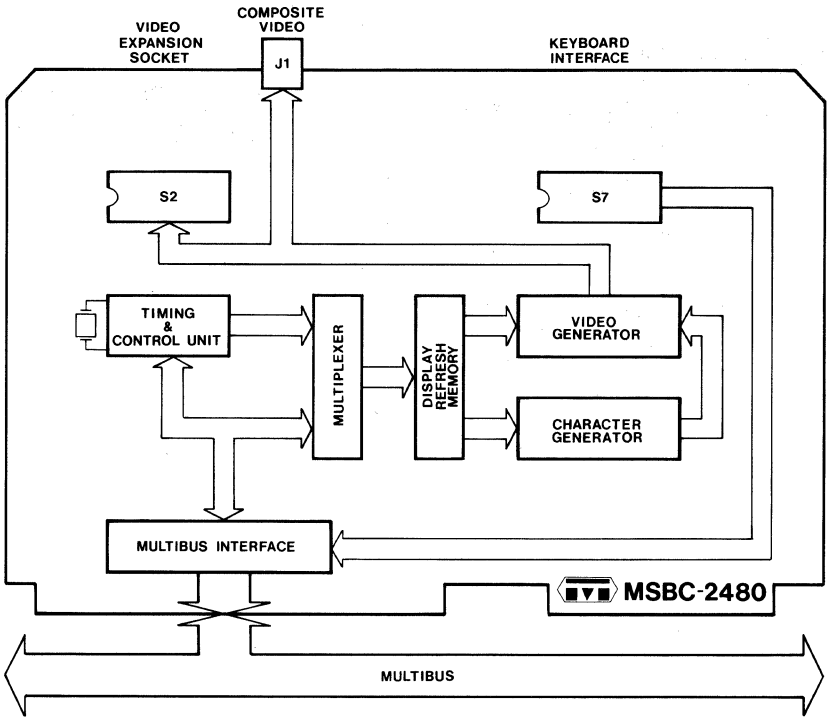



Figure 1. MSBC-2480 block diagram

## FUNCTIONAL DESCRIPTION

The MSBC-2480 is made up of five major operational blocks: Timing and Control Unit, Display Memory, Character Generator, Video Generator, and Multibus Interface. Communications between these blocks are shown in figure 1.

## TIMING AND CONTROL UNIT

All timing and control signals required to generate a video display with 24 lines of 80 characters per line are supported on-board the MSBC-2480. The Timing and Control Unit, consisting of the master oscillator (11 MHz) and various modulo counters, produces the horizontal and vertical sync signals needed by the monitor as well as all timing signals for display refresh memory (RAS, CAS).

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the MSBC-2480 can be synchronized to operate with other video boards as part of a complete video display system.

## DISPLAY MEMORY

The MSBC-2480 contains 2.5K bytes of on-board display refresh memory, to store up to 32 lines of 80 characters (2560 characters). The display memory occupies 4K bytes of system address space thereby permitting the CPU to identify each character location with a unique 12 bit address.

Each character position on the CRT screen corresponds to an 8 bit location in the display refresh memory. Characters are written on to the display by loading the ASCII Character Code to the appropriate display memory location. The CPU can read/write the display memory at full speed using all memory reference instructions.

All accesses to the display memory are controlled by a "Transparent Memory" control circuit within the Timing and Control Unit. In this way all accesses to the display memory (read, write, refresh) are efficiently arbitrated. The Transparent Memory control circuitry permits the CPU to read or write the refresh memory at any time and the display is free of glitches.

## CHARACTER GENERATOR

The MSBC-2480 contains an on-board 2716 EPROM which contains the binary video information to generate a 128 character set. The supplied character font consists of the full 96 upper/lower case alphanumeric character set with the addition of 32 special graphic characters. The alphanumeric characters are formed in a 5 x 7 dot matrix within a 6 x 10 dot character cell. The graphics characters utilize the entire character cell to allow for drawing continuous lines. For greater inter-character spacing the character cell size can be increased, with hardware straps, to 8 x 10 dots. Note that increasing the character cell size will cause gaps to appear between the graphics characters. Also, a different crystal is required for applications utilizing an 8 dot cell.

The MSBC-2480 permits simple implementation of custom character fonts. To install a new character set, the user need only reprogram the EPROM character generator with the video information to generate his own font.

## ATTRIBUTES

Each character is accessed by seven bits of the eight bit ASCII Character Code. This releases the most significant eighth bit for attribute selection. Characters displayed on the MSBC-2480 can be displayed either as normal (white on a black background), inverted (black on a white background), blinking, or both inverted and blinking. Character attributes are selected by on-board hardware straps and are enabled/disabled by the eighth bit of the character code.

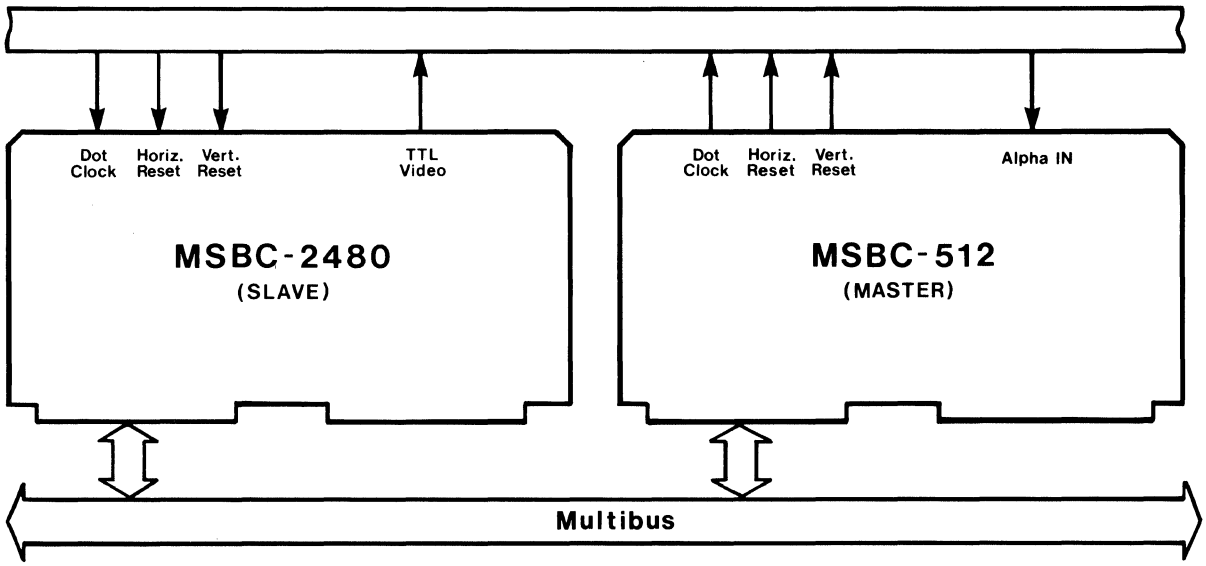



Figure 2. Combining MSBC-2480 with MSBC-512 for alpha/graph displays

The on-board character generator can be strapped to generate a reduced 64 character upper case only set. In this configuration an extra bit from the character code is released. These two surplus bits can be used to enable/disable any one of the four character attributes.

**SCROLL**
Although the MSBC-2480 can store up to 32 lines x 80 characters in the display memory, only 24 x 80 characters can be displayed at any one time. To enable the user to view the entire contents of the display memory a scroll feature has been incorporated into the design of the MSBC-2480. Through a Scroll Register, the user can specify which vertical line (0 to 31) will be displayed at the top of the screen.

**VIDEO GENERATOR**
The MSBC-2480 can directly drive any standard monochrome video monitor. Composite video signals as well as separate TTL level video, horizontal/vertical sync and blanking signals are supported on-board.

**KEYBOARD INTERFACE**
A keyboard can be interfaced to the MSBC-2480 through a 16 pin DIP socket, S7. The keyboard input port consists of eight input lines and one strobe line (positive pulse). Once the keyboard data strobe has been received, an interrupt is generated.

**BUS INTERFACE**
The MSBC-2480 plugs directly into the Multibus. The display refresh memory, which is memory mapped into the Multibus memory address space, can be strapped to reside at any 4K byte memory address boundary between 00000H and FFFFFH. The three internal registers (Scroll Register, Flag Register, and Keyboard Interface) are accessed through the unused locations of the occupied 4K byte address space.

**GRAPHICS**
The MSBC-2480 can be integrated, as an alphanumeric controller, within a complete alpha/graph video system. By configuring the MSBC-2480 to operate in the slave mode, the horizontal/vertical reset lines and the dot clock line are set to act as input ports. In this way the board can be synchronized to a master sync source. These lines can also be configured to operate as output ports to enable the user to configure his system to synchronize to the MSBC-2480. A typical application of combined alphanumerics/graphics is shown in figure 2, where the graphics board (MSBC-512) acts as the master sync source.

**PROGRAMMING**
The MSBC-2480 is programmed via three memory-mapped registers and 48 on-board hardware straps. Through the three registers the user can: select which vertical line will be displayed at the top of the screen (Scroll Register), accept data from an external keyboard (Keyboard Register), and read horizontal and vertical blanking (Flag Register). The board's operational status is determined by the hardware straps. Table 1 outlines the definitions of these straps.

| JUMPER NO. | DESCRIPTION | JUMPER NO. | DESCRIPTION |
|---|---|---|---|
| S1 | Select base address | W7 | Enable Transparent memory access mode |
| S3 | Select American/European operation | W8 | Enable "Slave" mode |
| S4 | Select Character Cell Size | W11 | Enable non-interlaced scan mode |
| S5 | Select character attribute | W12 | Enable interlaced scan mode |
| W1 | Enable "Master" mode | W14 | Enable European standard |
| W2 | Enable 8 x 10 character cell | W15 | Enable American standard |
| W3 | Enable 6 x 10 character cell | W16 | Disable Transparent memory access mode |
| W4 | Enable 6 x 10 character cell | W17 | Enable Transparent memory access mode |
| W5 | Enable 8 x 10 character cell | I0-7 | Select keyboard interrupt priority |
| W6 | Disable Transparent memory access mode | | |

Table 1. Jumper definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

With Transparent Memory Access: 800ns
Without Transparent Memory Access: 500ns

### DISPLAY PARAMETERS

| DESCRIPTION | DISPLAYED | STORED |
|---|---|---|
| Resolution | 1920 characters | 2560 characters |
| Horizontal Characters | 80 characters | 80 characters |
| Vertical Lines | 24 lines | 32 lines |
| Character Cell Size | 6 or 8 horizontal dots | |

### VIDEO TIMING

To generate a video display of 24 x 80 characters with a 6 dot cell, the MSBC-2480 uses an 11.06688 MHz crystal. The following table gives the video timing for both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 43.5 μs | 43.5 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 4.4 μs | 4.4 μs |
| Vertical Sync Frequency | 60.0 Hz | 50.2 Hz |
| Vertical Sync Width | 192.0 μs | 190.0 μs |

### IMPUT SIGNALS

Keyboard Data
Keyboard Strobe

### OUTPUT SIGNALS

TTL Level Video
Horizontal Drive
Vertical Drive
Composite Sync
Composite Video

### BUS INTERFACE

Address, data, and control signals conform to Intel Multibus Specification No. 9800683
Control Registers and Display Memory — Selectable on any 4K byte memory address boundary 00000H - FFFFFH (04000H)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1 : 86 pin edge connector, 0.156" centers | — Multibus Interface | COMPAR ESM-43-DSRI |
| S2 : 16 pin DIP socket | — Video Expansion Socket | AUGAT 516-A6-37D |
| S7 : 16 pin DIP socket | — Keyboard Interface | AUGAT 516-A6-37D |
| J1 : phono connector | — Composite Video | RCA 901 |

## PHYSICAL

### SIZE

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. ( 1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5% @ 0.9A

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

MSBC-2480 — XX — X

- 6 / 8 — Horizontal dots per character cell
- AS — American Standard (60 Hz)
- ES — European Standard (50 Hz)

Example: MSBC-2480-6-AS: 24 x 80 character display with 6 horizontal dots per character cell and a vertical refresh rate of 60 Hz.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MSBC-512

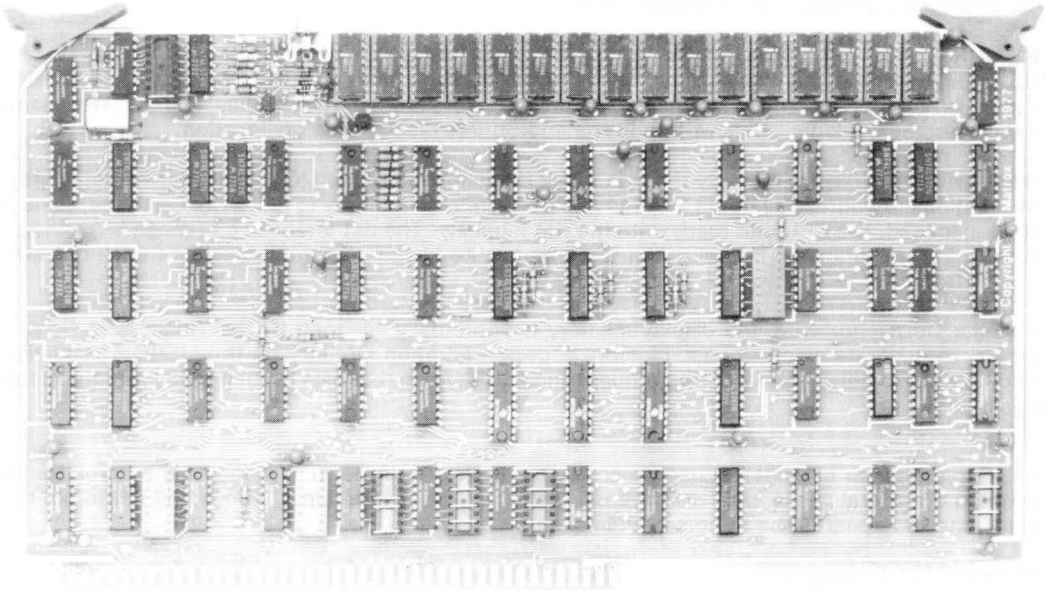
## 512 x 512 GRAPHICS DISPLAY CONTROLLER FOR MULTIBUS

1

- **Bit mapped 512 x 512 pixel display**
- **256 x 256, 512 x 256, 1024 x 256 formats also available**
- **Powerful X-Y virtual memory addressing**
- **Hardware scroll built-in**
- **Single instruction memory erase**
- **Color/grey-scale expansion**
- **Can be combined with MBSC-2480**
- **Transparent memory access**
- **Multibus* compatible**
- **Works with 8 and 16-bit CPUs**
- **Internal/external sync**
- **American/European operation**

The MSBC-512 is a member of Matrox's complete line of Multibus compatible graphics video boards. The MSBC-512 family of cards is designed to interface a mini or microcomputer to a CRT monitor and produce a B/W display of 512 x 512 points. The board also features built-in hardware scroll capabilities and a single instruction memory erase.

The MSBC-512 can also be combined with the MSBC-2480 to produce a complete alphanumerics/graphics video display system. Combining multiple MSBC-512 cards, the OEM system designer can construct a graphics display system with up to 24 bits/pixel (16 million different colors or grey levels).



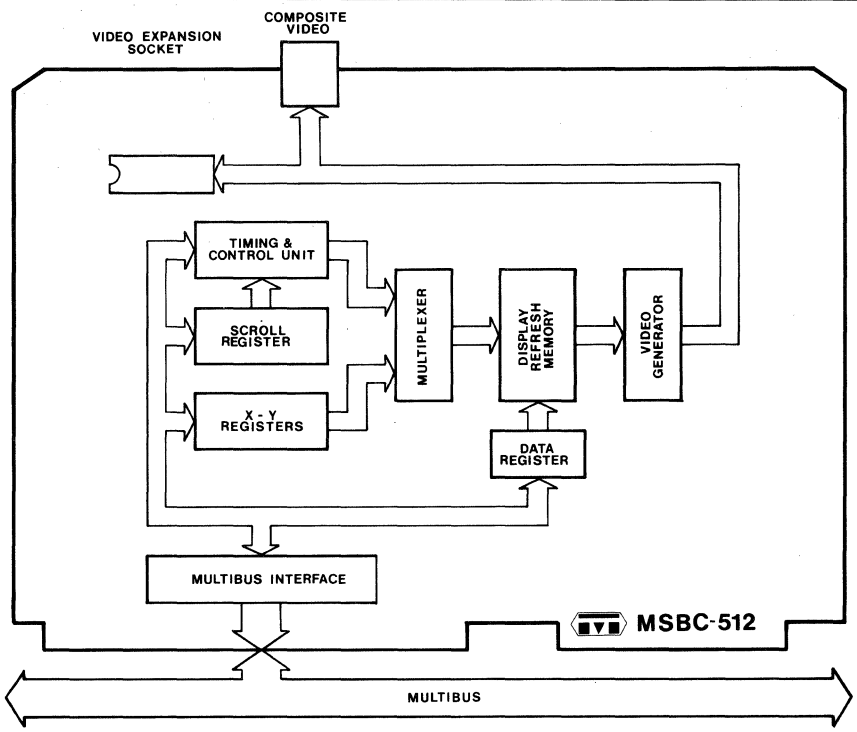



Figure 1. MSBC-512 Block Diagram

## FUNCTIONAL DESCRIPTION

The MSBC-512 consists of six main functional blocks (figure 1): Timing and Control Unit, Scroll Register, X-Y Registers, Display Memory, Video Generator, and Multibus Interface.

## TIMING AND CONTROL UNIT

All timing and control signals required by the video monitor (horizontal/vertical sync and blanking), display refresh memory (row/column addressing), and video generator (dot clock, load and shift) are generated by the Timing and Control Unit. The exact configurations of these signals are user-programmable, via hardware straps, to enable the MSBC-512 to generate displays with up to 512 horizontal dots by 512 vertical dots. The board can also be strapped to operate in either 50 Hz (European) or 60 Hz (American) systems.

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted through a bidirectional port, from an external sync source. In this way the MSBC-512 can be synchronized to operate with other video boards as part of a complete video display system.

## DISPLAY MEMORY

The MSBC-512 can be populated with 4, 8, or 16K RAMs for displays of 256 x 256, 512 x 256, 512 x 512, or 1024 x 256 dots. Each point on the CRT screen is identified by a unique address within the display memory. When a point is to be illuminated on the screen, a logic "1" is written to the appropriate display memory location.

The CPU reads/writes the display memory through a pair of memory-mapped I/O locations (X-Y Registers). This allows two memory locations to address all of the 262,144 bits of the refresh memory (512 x 512). Once the X and Y address of the dot has been loaded, the CPU can read/write the dot intensity. The dot intensity bit (image bit) can be assigned to any data bus bit. The resultant CRT display is a black and white image with the intensity of each dot being either on (logic "1") or off (logic "0").

In addition ot the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the MSBC-512 efficiently resolves any contention problems between read/write request and CRT refresh requests in such a way that the display is "transparent" to user.

## SCROLL

An on-board Scroll Register enables the user to scroll the display up or down. By loading the Scroll Register the user can specify which horizontal line is to be displayed at the top of the screen. Lines scrolled off the top of the display will "wrap-around" and re-appear at the bottom of the screen.

## SCREEN ERASE

The entire refresh memory on the MSBC-512 can be erased by a single OUTput instruction. Setting the memory erase enable bit when writing to the display memory will cause the entire memory to be set to that intensity (0 = black, 1 = white).

## VIDEO GENERATOR

The MSBC-512 works with all standard monochrome video monitors in American (60 Hz) and European (50 Hz) systems. TTL level video, horizontal sync, vertical sync, as well as composite video signals are supported on-board.

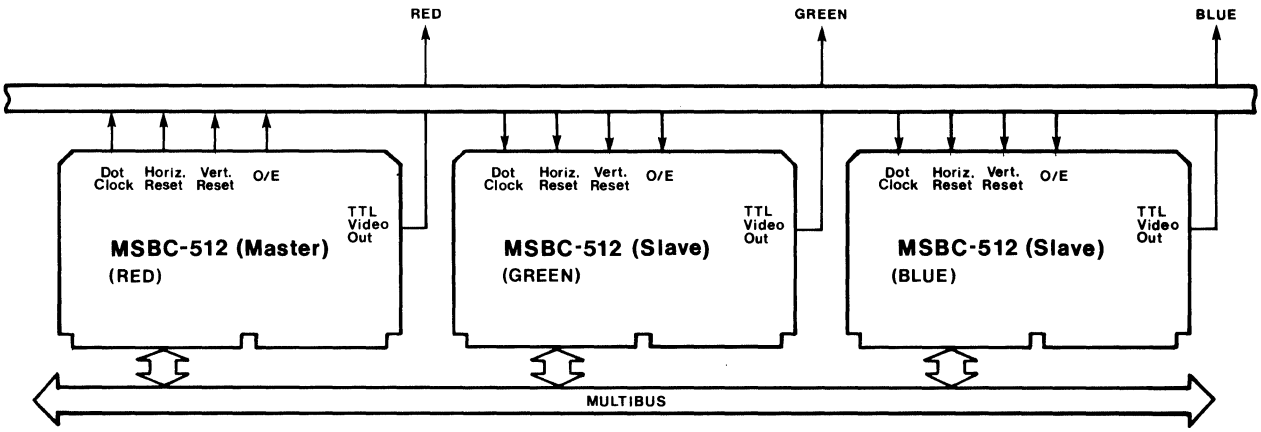



Figure 2. Stacking MSBC-512 cards for Color/Grey-scale displays

**BUS INTERFACE**

The MSBC-512 plugs directly into the Multibus and works with both 8-bit and 16-bit processors. All the Command and Statuts Registers as well as the Display Memory are accessed via memory mapped I/O. The MSBC-512 can be positioned on any 8 byte memory address boundary between 0000H and FFFFH.

**ALPHA-GRAPH DISPLAYS**

The MSBC-512 can be combined with the MSBC-2480 to generate alphanumeric/graphic displays. An on-board alphanumeric input port accepts the TTL level alphanumeric video information from the MSBC-2480 and combines it with the graphics video from the MSBC-512. The result is a powerful display combining both alphanumerics and graphics without the overhead involved in generating alphanumeric characters using graphic techniques.

**COLOR/GREY-SCALE EXPANSION**

Multiple MSBC-512 cards can be combined to provide for color/grey-scale displays. As previously outlined (DISPLAY MEMORY), the image bit on a given card can be assigned to any data bus bit. Thus the output of each card can be assigned a different weight or color. By assigning cards to different data bus bits and strapping all the cards with the same address, the intensity or color of a given dot can be loaded in a single instruction. A typical example of building up a color video system using the MSBC-512 is shown in figure 2.

**PROGRAMMING**

The MSBC-512 is programmed, for various display resolutions, by on-board hardware straps. These straps are organized into three 16 pin "programming sockets" to facilitate simple re-programming of the board. Table 1 defines the on-board jumpers used to configure the MSBC-512 for the various resolution options.

| SOCKET | JUMPER | DESCRIPTION |
|---|---|---|
| P | 1 | Vertical display = 240 lines (American standard) or 256 lines (European standard) |
| | 2 | Vertical reset = 262½ lines (American standard) |
| | 3 | Vertical reset = 312½ lines (European standard) |
| | 4 | Vertical sync = 244 lines (American standard) |
| | 5 | Vertical sync = 276 lines (European standard) |
| | 6 | Not used |
| | 7 | Enable 512 dot vertical resolution |
| | 8 | Not used |
| R | 1 | Enable 1024 dot horizontal resolution |
| | 2 | Set memory access mode for RAM type used |
| | 3 | Enable 1024 dot horizontal resolution |
| | 4 | Disable 1024 dot horizontal resolution |
| | 5 | Synchronize blanking for 512/1024 dot horizontal resolution |
| | 6 | Synchronize blanking for 256 dot horizontal resolution |
| | 7 | Dot clock = 5.53344 MHz (256 dot horizontal resolution) |
| | 8 | Dot clock = 11.06688 MHz (512/1024 dot horizontal resolution) |
| J | 1 | Enable 256 x 256 addressing |
| | 2 | Enable 512 x 256 addressing |
| | 3 | Enable interlaced addressing (512 x 512/1024 x 256) |
| | 4 | Enable 512 dot horizontal addressing |
| | 5 | Enable 1024 dot horizontal addressing |
| | 6 | Enable 512 dot vertical addressing |
| | 7 | Synchronize LOAD SCROLL signal to 60 Hz (American standard) |
| | 8 | Synchronize LOAD SCROLL signal to 50 Hz (European standard) |

Table 1. Jumper Configurations

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μs

### DISPLAY PARAMETERS

| RESOLUTION | RAM TYPE |
|---|---|
| 256 X 256 | 4K |
| 512 X 256 | 8K |
| 512 X 512 | 16K |
| 1024 X 256 | 16K |

### VIDEO TIMING

For a 256 x 256 or 512 x 256 display, the video output is non-interlaced. For a 512 x 512 or 256 x 1024 display, the video output is interlaced (two fields per frame). In order to avoid display flicker, a monitor with long persistence phosphors must be used.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46 μs | 46 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 5.67 μs | 5.67 μs |
| Vertical Sync Frequency | 60 Hz | 50.2 Hz |
| Vertical Sync Width | 190 μs | 190 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Sync
Vertical Sync
Composite Sync
Composite Video

### BUS INTERFACE

Address, data, and control signals conform to Multibus Specifications No. 9800683
Display Memory, Command and Status Registers — Selectable on any 8 byte memory address boundary 0000-FFFFH (5000H)
— or selectable on any 8 byte I/O address boundary

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1 : 86 pin edge connector, 0.156" centers | — Multibus Interface | COMPAR ESM-43-DSRI |
| J1 : phono connector | — Composite Video | RCA 901 |
| V : 16 pin DIP socket | — Video Expansion Socket | AUGAT 516-A6-37D |

## PHYSICAL

### SIZE

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. ( 1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5% @ 800mA
+12V DC ±5% @ 200mA

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0°C to 55°C
Relative Hymidity: 0% to 95% non-condensing

### ORDERING INFORMATION

MSBC — XXX/XXX — XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- XXX: Vertical resolution (256/512)
- XXX: Horizontal resolution (256/512/1024)

Example: MSBC-512/512 — AS: 512 x 512 dot display with a 60 Hz vertical frame refresh rate.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# NSBC-512

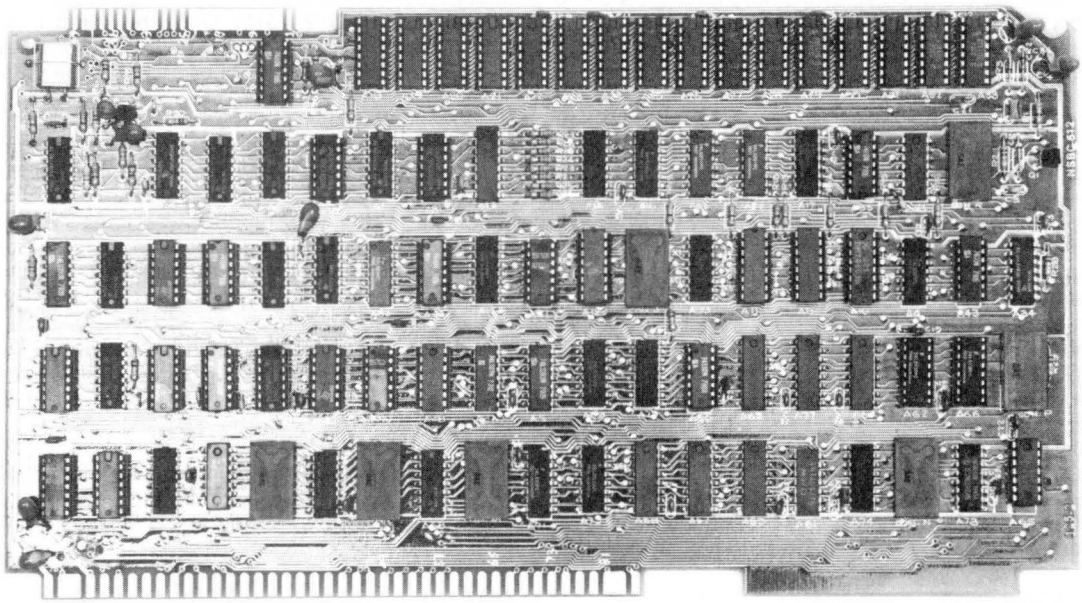
## VECTOR PLOT 512 x 512 GRAPHICS DISPLAY CONTROLLER FOR MULTIBUS

1

- **Bit mapped 512 x 512 dot display**
- **256 x 256, 512 x 256, 1024 x 256 formats available**
- **Powerful X-Y virtual memory addressing**
- **High speed vector plot**
- **Single instruction memory erase**
- **Color/grey-scale expansion**
- **Can be combined with MSBC-2480**
- **Transparent memory access**
- **Multibus* compatible**
- **Works with 8 and 16-bit CPUs**
- **Internal/external sync**
- **American/European operation**

The NSBC-512 is a member of Matrox's complete line of Multibus compatible graphics video boards. The NSBC-512 family of cards is designed to interface a mini or microcomputer to a CRT monitor and produce a B/W display of 512 x 512 points. The board also features a high speed vector plot capability and a single instruction memory erase.

The NSBC-512 can also be combined with the MSBC-2480 to produce a complete alphanumerics/graphics video display system. Combining multiple NSBC-512 cards, the OEM system designer can construct a graphics display system with up to 24 bits/pixel (16 million different colors or grey levels).



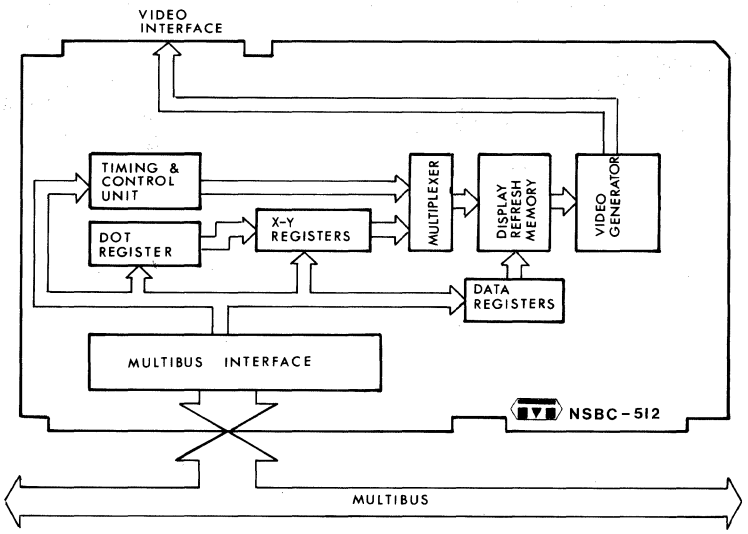



Figure 1. NSBC-512 Block Diagram

## FUNCTIONAL DESCRIPTION

The NSBC-512 consists of six main functional blocks (figure 1): Timing and Control Unit, Dot Register, X-Y Registers, Display Memory, Video Generator, and Multibus Interface.

## TIMING AND CONTROL UNIT

All timing and control signals required by the video monitor (horizontal/vertical sync and blanking), display refresh memory (row/column addressing), and video generator (dot clock, load and shift) are generated by the Timing and Control Unit. The exact configurations of these signals are user-programmable, via hardware straps, to enable the NSBC-512 to generate displays with up to 512 horizontal dots by 512 vertical dots. The board can also be strapped to operate in either 50 Hz (European) or 60 Hz (American) systems.

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the NSBC-512 can be synchronized to operate with other video boards as part of a complete video display system.

## DISPLAY MEMORY

The NSBC-512 contains a 32K byte on-board dynamic read/write display refresh memory capable of generating a display with up to 512 x 512 dots. Each point on the CRT screen is identified by a unique address within the display memory. When a point is to be illuminated on the screen, a logic "1" is written to the appropriate display memory location.

The CPU reads/writes the display memory through a pair of memory-mapped I/O locations (X-Y Registers). This allows two memory locations to address all of the 262,144 bits of the refresh memory (512 x 512). Once the X and Y address of the dot has been loaded, the CPU can read/write the dot intensity. The dot intensity bit (image bit) can be assigned to any data bus bit. The resultant CRT display is a black and white image with the intensity of each dot being either on (logic "1") or off (logic "0").

The NSBC-512 uses a 4096 x 4096 virtual address space. Within this space, the display memory can be accessed in either Wrap-Around mode or Clipping mode. When operating in the Wrap-Around mode the higher order address bits not allowed by the NSBC-512 will be ignored. The board will attempt to write to the specified location, but since it will not see the higher address bits it will actually write to a lower address. In this way the displayed image will appear to "wrap around" the screen. Alternatively, the NSBC-512 can be strapped to ignore addresses outside of the display area completely. In this way a "blind" working space is created in which Vector Plot software will continue to work, but will not de displayed.

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the NSBC-512 efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display is "transparent" to user.

The NSBC-512 can optionally be populated with either 4K or 8K memory for less dense display requirements. In this way displays of 256 x 256 or 512 x 256 dots can be configured without any wasted memory. Moreover the standard 512 x 512 memory configuration can be configured, via on-board hardware straps, to operate in a horizontal interlace mode whereby displays of 1024 x 256 dots can be generated.

## VECTOR PLOT

Lines and curves can be drawn at high speeds on the NSBC-512 with the vector plot feature. When drawing a line at high speed, the start point is written to the display by first specifying the X and Y coordinates and then writing the dot intensity to the Data Register. The next point on the line is written to the display by loading the Dot Register with the cursor step direction. The X and Y coordinates of the cursor will automatically be modified and the dot intensity will automatically be written to this location.

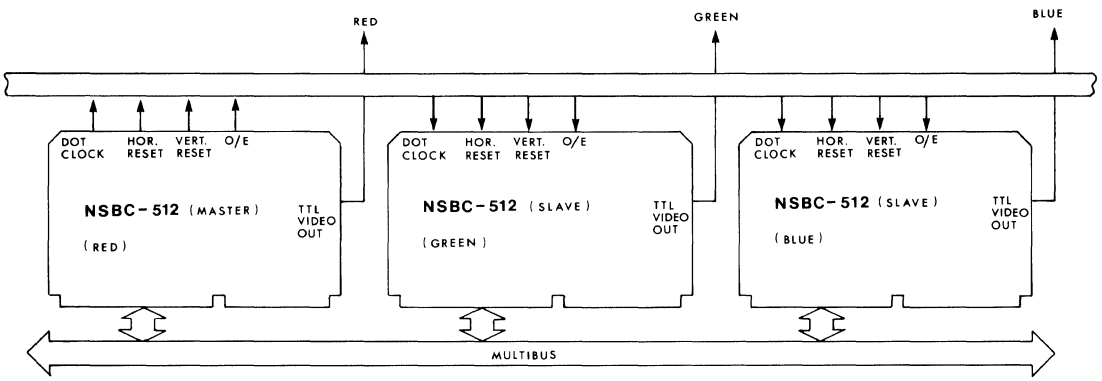



Figure 2. "Stacking" NSBC-512 cards for Color/Grey-scale displays

1

**SCREEN ERASE**
The entire refresh memory on the NSBC-512 can be erased by a single OUTput instruction. Setting the memory erase enable bit when writing to the display memory will cause the entire memory to be set to that intensity (0 = black, 1 = white).

**VIDEO GENERATOR**
The NSBC-512 works with all standard monocrome video monitors in American (60 Hz) and European (50 Hz) systems. TTL level video, horizontal sync, vertical sync, as well as composite video signals are supported on-board.

**BUS INTERFACE**
The NSBC-512 plugs directly into the Multibus and works with both 8-bit and 16-bit processors. All the Command and Status Registers as well as the Display Memory are accessed via memory mapped I/O. The NSBC-512 can be positioned on any 8 byte memory address boundary between 0000H and FFFFH.

**ALPHA/GRAPH DISPLAYS**
The NSBC-512 can be combined with the MSBC-2480 to generate alphanumeric/graphic displays. An on-board alphanumeric input port accepts the TTL level alphanumeric video information from the MSBC-2480 and combines it with the graphics video from the MSBC-512. The result is a powerful display combining both alphanumerics and graphics without the overhead involved in generating alphanumeric characters using graphic techniques.

**COLOR/GREY-SCALE EXPANSION**
Multiple NSBC-512 cards can be combined to provide for color/grey-scale displays. As previously outlined (DISPLAY MEMORY), the image bit on a given card can be assigned to any data bus bit. Thus the output of each card can be assigned a different weight or color. By assigning cards to different data bus bits and strapping all the cards with the same address, the intensity or color of a given dot can be loaded in a single instruction. A typical example of building up a color video system using the NSBC-512 is shown in figure 2.

**PROGRAMMING**
The NSBC-512 is programmed, for various display resolutions, by on-board hardware straps. These straps are organized into three 16 pin "programming sockets" to facilitate simple re-programming of the board.

| SOCKET | JUMPER | DESCRIPTION |
|---|---|---|
| P | 1 | Vertical display = 240 lines (American standard) or 256 lines (European standard) |
| | 2 | Vertical reset = 262½ lines (American standard) |
| | 3 | Vertical reset = 312½ lines (European standard) |
| | 4 | Vertical sync = 244 lines (American standard) |
| | 5 | Vertical sync = 276 lines (European standard) |
| | 6 | Not used |
| | 7 | Enable 512 dot vertical resolution |
| | 8 | Not used |
| R | 1 | Enable 1024 dot horizontal resolution |
| | 2 | Set memory access mode for RAM type used |
| | 3 | Enable 1024 dot horizontal resolution |
| | 4 | Disable 1024 dot horizontal resolution |
| | 5 | Synchronize blanking for 512/1024 dot horizontal resolution |
| | 6 | Synchronize blanking for 256 dot horizontal resolution |
| | 7 | Dot clock = 5.53344 MHz (256 dot horizontal resolution) |
| | 8 | Dot clock = 11.06688 MHz (512/1024 dot horizontal resolution) |
| J | 1 | Display memory addressing straps (exact configurations depend on resolution and type of RAM used) |
| | 2 | |
| | 3 | |
| | 4 | |
| | 5 | |
| | 6 | |
| | 7 | |
| | 8 | |

Table 1. Jumper Descriptions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μs

### DISPLAY PARAMETERS

| RESOLUTION | RAM TYPE |
|---|---|
| 256 X 256 | 4K |
| 512 X 512 | 8K |
| 512 X 512 | 16K |
| 1024 X 256 | 16K |

### VIDEO TIMING

For a 256 x 256 or 512 x 256 display, the video output is non-interlaced. For a 512 x 512 or 256 x 1024 display, the video output is interlaced (two fields per frame). In order to avoid display flicker, a monitor with long persistence phosphors must be used.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46 μs | 46 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 5.67 μs | 5.67 μs |
| Vertical Sync Frequency | 60 Hz | 50.2 Hz |
| Vertical Sync Width | 190 μs | 190 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Sync
Vertical Sync
Composite Sync
Composite Video

### BUS INTERFACE

Address, data, and control signals conform to Multibus Specifications No. 9800683
Display Memory, Command and Status Registers — Selectable on any 8 byte memory address boundary 0000-FFFFH (5000H)
— or selectable on any 8 byte I/O address boundary

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1 : 86 pin edge connector, 0.156" centers | — Multibus Interface | COMPAR ESM-43-DSRI |
| J1 : 50 pin edge connector, | — TTL/Composite Video | MOLEX 15-25-8501 |

### PHYSICAL

**SIZE**

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+5V DC ±5% @ 800mA
+12V DC ±5% @ 200mA

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

NSBC — XXX/XXX — XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- XXX: Vertical resolution (256/512)
- XXX: Horizontal resolution (256/512/1024)

Example: NSBC-512/512 — AS: 512 x 512 dot display with a 60 Hz vertical frame refresh rate.

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
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# RGB-256

## 256 x 256 COLOR GRAPHICS DISPLAY CONTROLLER FOR MULTIBUS

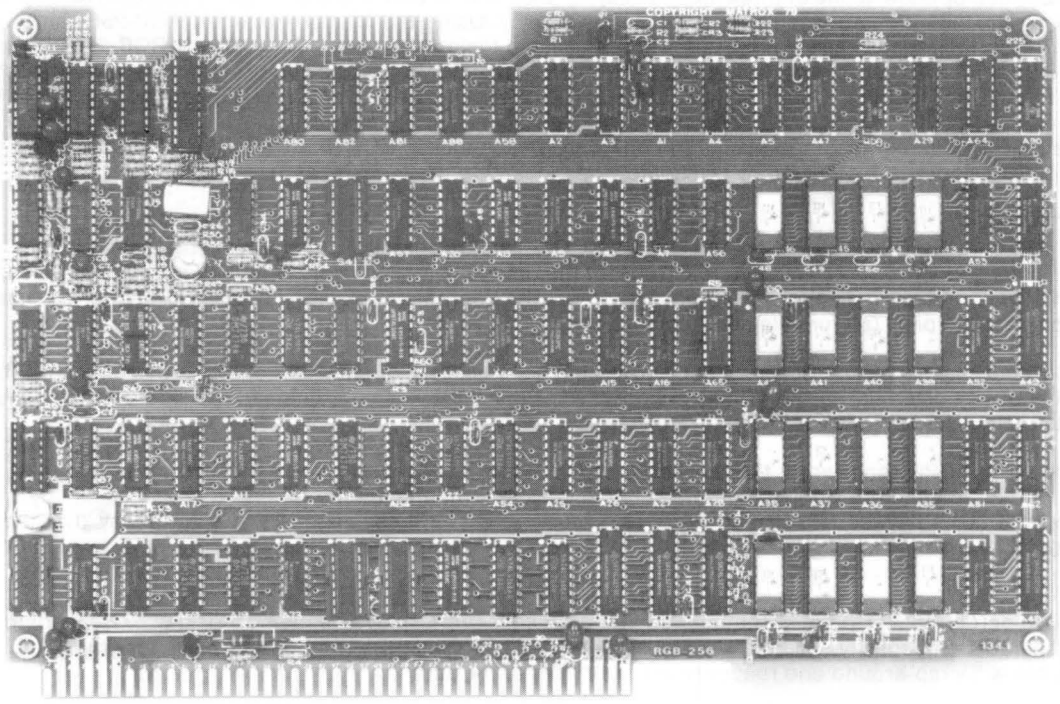
1

- **256 x 256 resolution**
- **4 bits/pixel expandable to 8 bits/pixel**
- **Built-in 8-bit D/A converter (grey scale)**
- **Built-in composite color encoder**
- **Single instruction erase**
- **Built-in phase lock loop (for genlock)**
- **Multibus* compatible**
- **Hardware scroll**
- **Internal/external sync**
- **American/European operation**

The RGB-256 is a powerful color graphics display controller built on a single Multibus* compatible card. Graphics images of up to 256 x 256 dots can be displayed in up to 16 colors or grey levels. The RGB-256 also includes such advanced features as hardware scroll, single instruction erase and digitize commands.

The RGB-256 can be combined with other Matrox video boards such as the MSBC-2480 (alphanumerics) and the FG-01 (frame grabber). The OEM sysem designer can therefore integrate the RGB-256 into a powerful tailor-made video display system.

The RGB-256 works with all standard video monitors in Europe (50 Hz) and America (60 Hz). An on-board phase lock loop can be synchronized to an external sync source to enable the RGB-256 to be used in broadcast applications.



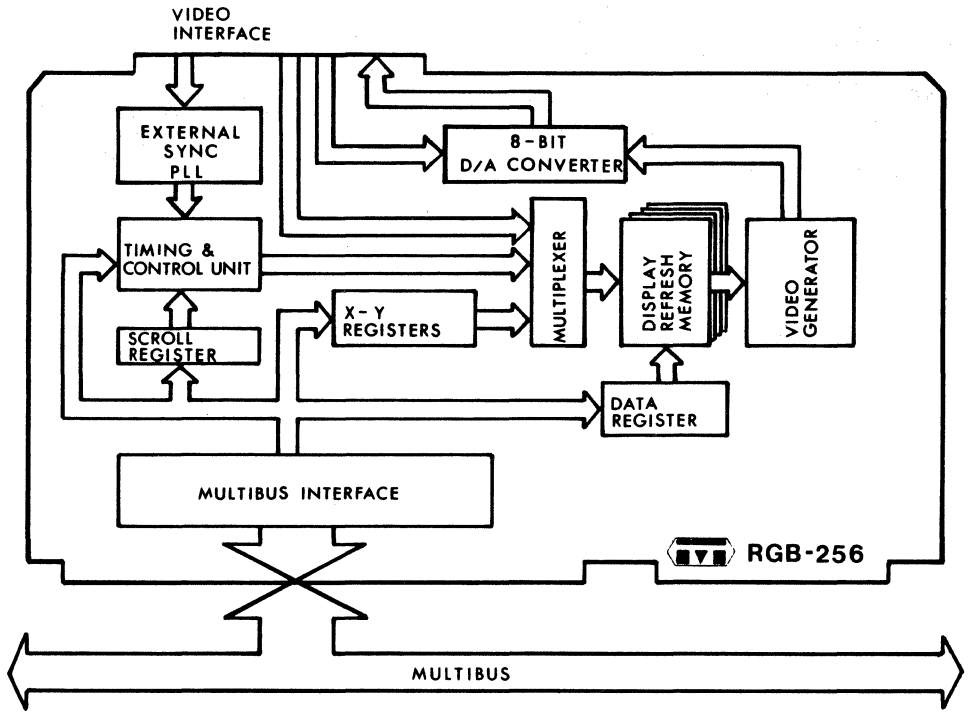



Figure 1. RGB-256 Block Diagram

**FUNCTIONAL DESCRIPTION**
The RGB-256 is a single board color graphics controller. It consists of five main operational blocks: Timing and Control Unit, X-Y Registers, Display Memory, Video Generator, and Multibus Interface. A block diagram of the RGB-256 is shown in figure 1.

**TIMING AND CONTROL UNIT**
The Timing and Control Unit consists of three major subsystems: Phase Lock Loop, Sync Generator, and Internal Reference. Through these three subsystems the RGB-256 is capable of generating all the necessary timing signals to produce a composite color or grey-scale video display. These timing signals include: horizontal/vertical sync and blanking, display refresh RAM addressing, as well as a color subcarrier.

The RGB-256 can operate in one of three modes: Master, External, or Slave. In the Master mode, the RGB-256 generates all the necessary video timing signals required for the display. Using the Master mode the RGB-256 can be used as a stand-alone controller or as a system master, where the video timing signals produced by the RGB-256 are used to synchronize one or more other boards into a complete video imaging system. The Slave mode is used to synchronize the RGB-256 to another RGB-256 system master. Slaved RGB-256 boards can be used to expand the number of bits/pixel.

Using the RGB-256 in external mode locks the on-board phase-locked loop to an external sync source. Fully NTSC or PAL compatible signals are provided by the board when locked to broadcast standard inputs.

**DISPLAY MEMORY**
The RGB-256 contains 32K bytes of on-board dynamic RAM which contains the binary picture information. The display memory is arranged as 256 x 256 x 4 bits, with each of the unique 65,536 memory locations representing a specific location on the CRT screen. To display a point on the screen, the appropriate memory location is loaded with four data bits which represent the pixel (picture element) color.

The RGB-256 uses a simple yet powerful X-Y addressing scheme. Two directly addressable registers store the X and Y coordinates of any given dot in the display memory. After the dot's X-Y coordinates have been defined, the CPU can read/write the pixel information to the Data Register.

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66 ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the RGB-256 efficiently resolves any contention problems between CPU read/write requests and CRT refresh requests in such a way that the display is "transparent" to the user.

**SCROLL**
An on-board scroll register permits the user to vertically shift the displayed image up or down. By loading the Scroll Register, the user can specify which horizontal line will be displayed at the top of the screen. Lines scrolled off the top of the display will wrap-around and reappear at the bottom of the screen.

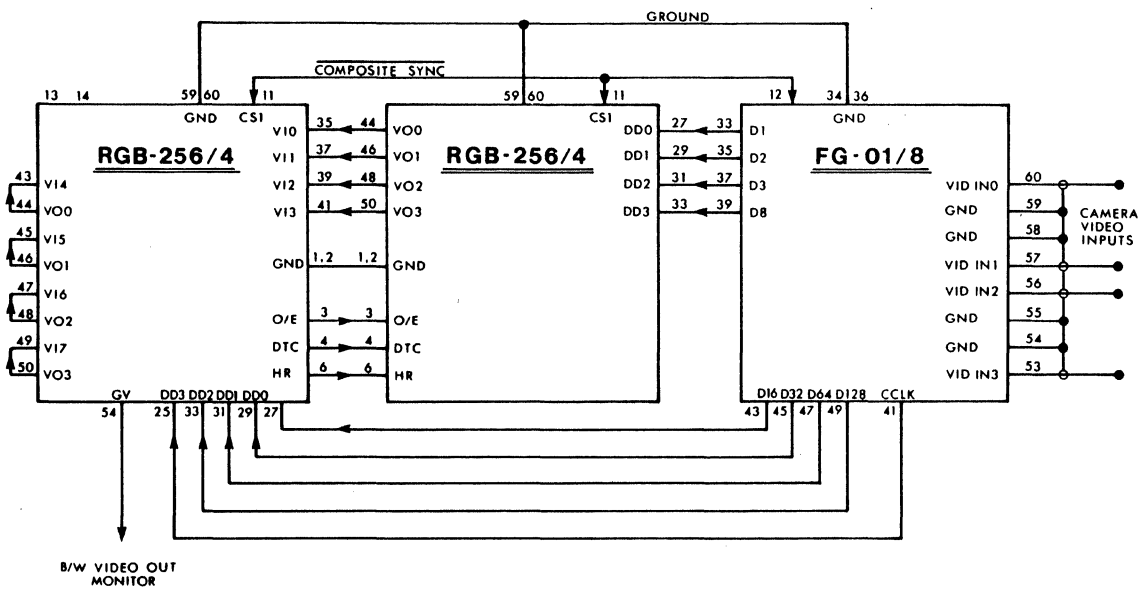



Figure 2. Combining RGB-256 and FG-01 — 256 x 256 x 8 bit imaging system

**ERASE/DIGITIZE COMMAND**
The RGB-256 has an erase/digitize command built into hardware. This command enables the user to preset the entire display refresh memory to a given value or to load one field of a digitized video signal obtained from an external frame grabber card. In the erase mode, the user can set the entire display memory to a specified value with a single INput instruction.

**VIDEO GENERATOR**
The RGB-256 includes a built-in color encoder which can provide up to 16 colors or grey levels. Most monochrome and composite color monitors will work with the RGB-256. Red, Green, Blue, and Mid-Green TTL level video, horizontal drive, vertical drive, as well as composite color and grey-scale video signals are provided.

**BUS INTERFACE**
The RGB-256 plugs directly into the Multibus and works most mini and microcomputers. The RGB-256 can be located on any 8 byte system I/O address boundary between 00H and FFH. Since the display refresh memory on the RGB-256 is directly accessed by two I/O ports (X-Y Registers), no system memory address space is required.

**SYSTEM CONFIGURATIONS**
The RGB-256 can be used as a stand alone controller or, by "stacking" cards, can be integrated into a complete video imaging system. As a stand alone controller the RGB-256 provides a 256 x 256 dot raster in 16 different colors or grey levels. Additionally the RGB-256 can be combined with other boards to provide more colors (multiple RGB-256 boards), digitized TV pictures (RGB-256 + FG-01) or a complete alphanumerics/graphics display system (RGB-256 + MSBC-2480). The RGB-256 can also be synchronized to an external sync source via the on-board phase lock loop. This feature enables the boards to generate NTSC/PAL compatible video signals for integration into a broadcasting environment.

**PROGRAMMING**
The RGB-256 is programmed via five I/O registers in combination with a series of on-board hardware straps. Address bits A2 and A3 are used to select between registers (Data Register, Scroll Register, X Register, and Y Register) which are located on even addresses relative to the RGB-256's base address (Table 1). A Flag Register is included on-board (accessed by reading location 2) to enable the host processor to monitor the board's status (Busy and Vertical Blank). Reading the X Register will initiate the Frame/Digitize command.

Much of the board's operational parameters are defined through on-board hardware straps, which have been organized into four 16-pin DIP sockets. With these jumpers, the user can program the on-board Sync Generator for American (60 Hz) or European (50 Hz) operation, in either Master, External, or Slave sync mode. Straps are also provided to set the RGB-256 video outputs for NTSC (American) or PAL (European) standard compatibility. The board's base address is determined by the on-board straps.

| Register | Relative Address | Description | |
|---|---|---|---|
| | | WRITE | READ |
| DATA | 0 | Write display memory | Read display memory |
| SCROLL | 2 | Set topmost displayed line | Read Flag Register |
| X | 4 | Set X coordinate | Initiate Erase/Digitize Command |
| Y | 6 | Set Y coordinate | Not used |

Table 1. Register definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μsec. max.

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Horizontal Resolution | 256 dots |
| Vertical Resolution | 256 dots (European standard), 240 dots (American standard) |

### VIDEO TIMING

The RGB-256 generates a 256 x 256 dot raster graphics display. The following table gives the video timing for both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46.1 μs | 46.5 μs |
| Horizontal Sync Frequency | 15.734 KHz | 15.638 KHz |
| Horizontal Sync Width | 5.8 μs | 5.8 μs |
| Vertical Sync Frequency | 60.05 Hz | 50.12 Hz |
| Vertical Sync Width | 190.66 μs | 191.83 μs |

### OUTPUT SIGNALS

TTL Level Video: Red
Green
Blue
Vertical Drive
Horizontal Drive

Composite Video: Composite Color
Composite Grey-Scale

### BUS INTERFACE

Address, data and control signals conform to Intel Multibus Specification No. 9800683
Command Status and Data Registers — Selectable on any 8 byte I/O address bondary 00H — FFH (80H)

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1 : 86 pin edge connector, 0.156" centers — Multibus Interface | COMPAR ESM-43-DSRI |
| J1 : 60 pin edge connector — Video Interface | MOLEX 15-25-8601 |

## PHYSICAL

**SIZE**

Width: 12.00 in. (30.48 cm)
Height: 8.00 in. (20.32 cm)*
Depth: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+5V DC ±5% @ 1A
+12V DC ±5% @ 400mA
−12V DC ±5% @ 250mA

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

*Note — The RGB-256 is slightly taller than the standard Multibus card size.

### ORDERING INFORMATION

RGB-256/X — XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- X: Number of bit planes (3/4)

Example: RGB-256/3-AS: 256 x 256 graphics display with 3 bit planes (8 possible colors or grey levels) using a vertical refresh rate of 60 Hz.

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

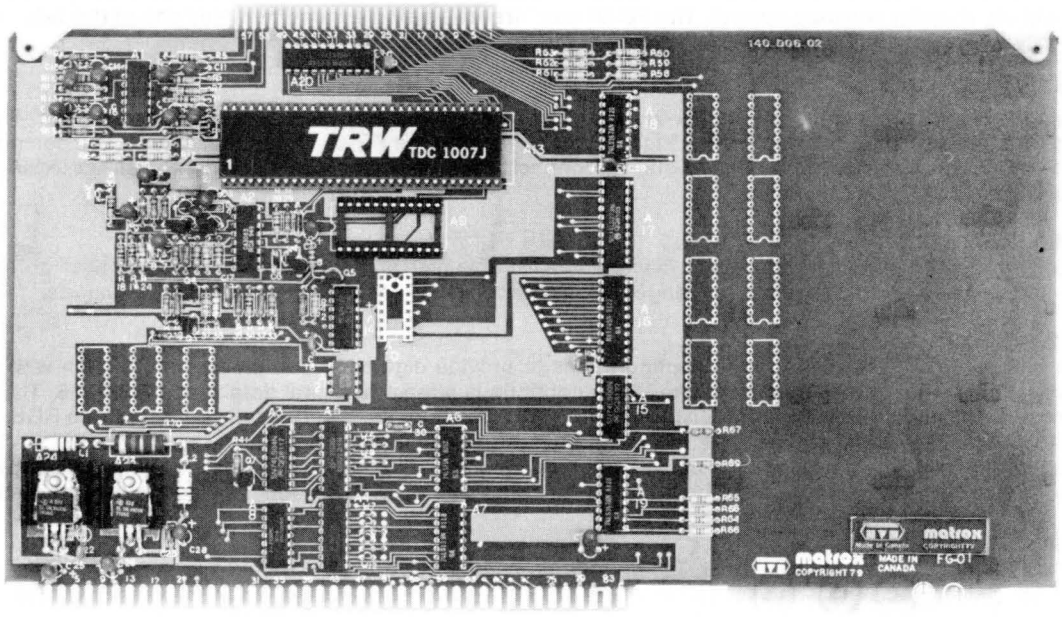
# FG-01

## HIGH SPEED VIDEO A/D CONVERTER FOR MULTIBUS

1

- 4, 6, or 8 bit A/D converter
- 4 video inputs
- Accommodates most video amplitudes
- Interfaces directly to RGB-256 to store TV picture
- Continuous or "Freeze" grab operation
- Multibus* compatible
- On-board sync separator circuit
- American/European operation

The FG-01 is a high speed analog to digital converter card that is intended to be used with the Matrox RGB-256 graphics display controller cards. The FG-01 permits the user to digitize a standard monochrome video signal ($1V_{p-p}$) and, on command, to write one digitized field of video information into the RGB-256 display refresh memory.



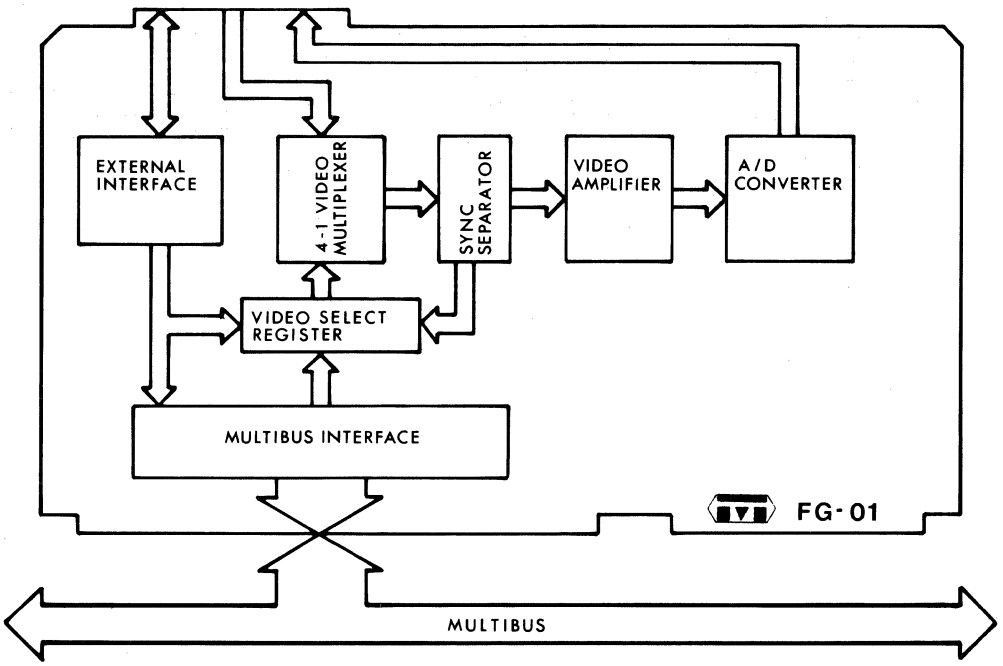



Figure 1. FG-01 block diagram

**FUNCTIONAL DESCRIPTION**
The FG-01 frame grabber card can be functionally divided into six operational blocks. These blocks (figure 1) are: Input Multiplexer, Sync Generator, Video Amplifier, A/D Converter, Multibus Interface, and External Interface.

The FG-01 has been designed to operate with the RGB-256 graphics controller. Through commands generated by the RGB-256 the FG-01 will digitize a frame of video information (from an external TV camera) and store it in the RGB-256 display memory. This frame grabbing operation can be continuous (the RGB-256 will display a continually updated or "live" picture) or one-shot, effectively "freezing" the action. Figure 2 illustrates the connections between the RGB-256 and the FG-01.

**INPUT MULTIPLEXER**
The FG-01 contains an on-board 4 to 1 input video multiplexer. In this way the user can interface up to four analog video inputs (composite video from four different TV cameras) to the 30 MHz A/D converter. Switching, between these four video inputs, is under software control. The FG-01 can "freeze" a single frame from any one of the video inputs or, by periodically accessing the board, can provide a continuous "grabbing" of consecutive fields.

**SYNC SEPARATOR**
Composite video signals, accepted by the FG-01, are stripped of the horizontal and vertical sync signals. These sync signals are then used by the FG-01 as control signals to synchronize the FG-01 to the TV camera. The composite sync signals are also made available on the video output connector to enable the user to synchronize the RGB-256 color graphics board to the TV camera as well.

**VIDEO AMPLIFIER**
The selected input video goes to a backporch clamp and a variable gain stage. An on-board gain control potentiometer allows the user to take advantage of the full range of the A/D converter for a given input signal amplitude.

**VIDEO A/D CONVERTER**
The FG-01 can be ordered in one of three configurations to provide digitized video picture information with 4, 6, or 8 bits per pixel. The on-board A/D converter provides a continuous stream of digital data to the RGB-256. The initiation of the storage of this data in the RGB-256 display memory is done, under software control, through the RGB-256 card. A/D conversion is initiated on the negative edge of the Convert Command generated by the RGB-256. On this same negative edge the data from the previous conversion is made valid. The digital outputs from the A/D converter are buffered before being passed out from the board. In this way the validity of the produced video information is assured.

**BUS INTERFACE**
The FG-01 plugs directly into the Multibus. To the Multibus computer the FG-01 looks like a single I/O addressable register (Video Select Register). The user can locate the FG-01 anywhere in the system I/O address map (00 to FFH).

**EXTERNAL INTERFACE**
An external interface is provided on-board the FG-01 to permit computers, external to the Multibus, to communicate with the FG-01. The external interface drives the 8 data lines, 8 address lines, and the IORC/ and IOWC/ lines of the Multibus to allow the host computer to access any device in the Multibus I/O address map. This allows the interfaced computer to fully access the RGB-256 or any other I/O mapped board on the Multibus system bus.

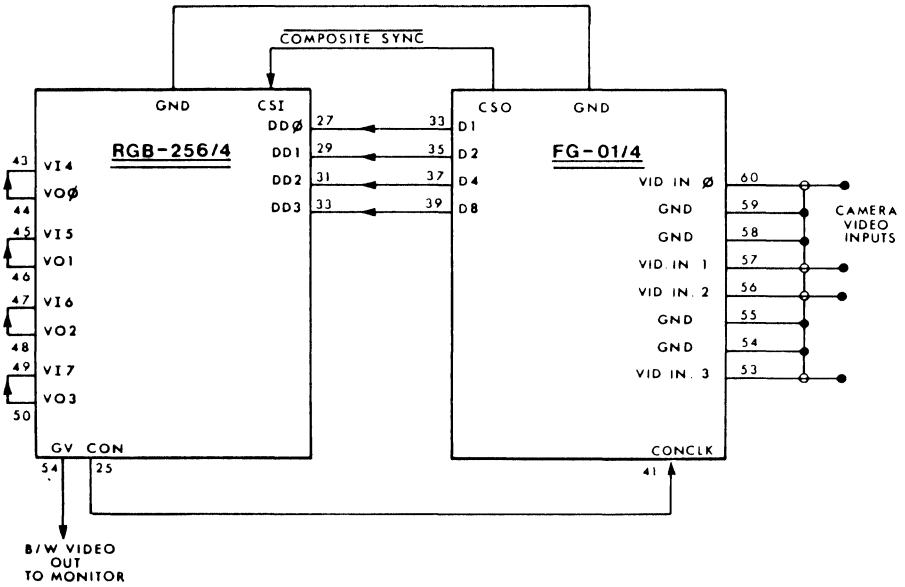



Figure 2. 256 x 256 x 4 bit imaging system

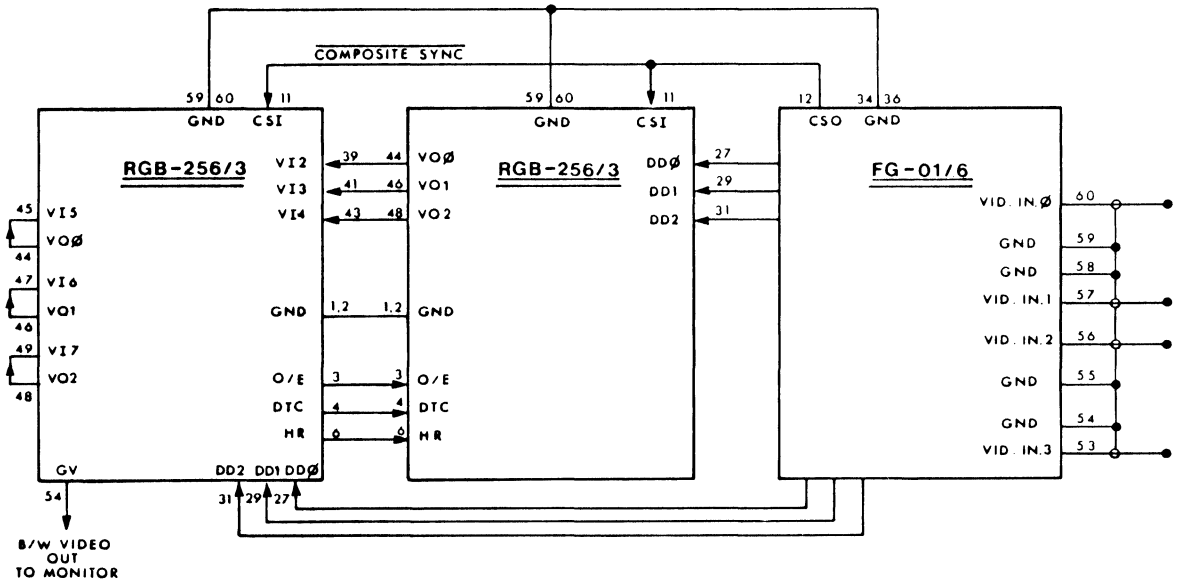



Figure 3. 256 x 256 x 6 bit imaging system

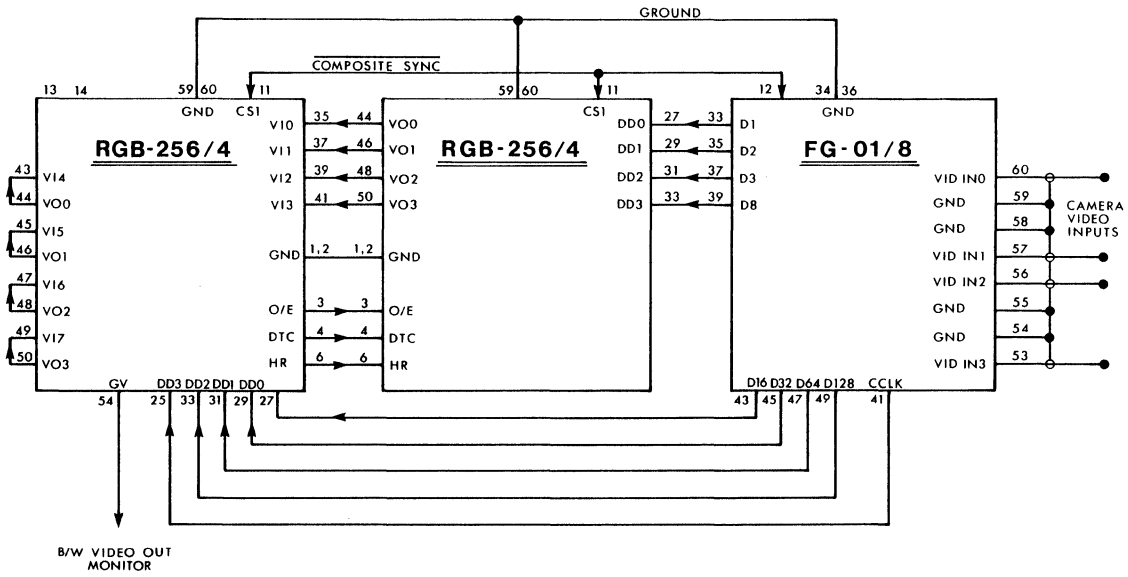



Figure 4. 256 x 256 x 8 bit imaging system

# SPECIFICATIONS

## FUNCTIONAL

### INPUT SIGNALS

Analog Video 0*
Analog Video 1
Analog Video 2
Analog Video 3
Convert Clock (TTL, 20 MHz max.)

*All analog video inputs are composite video (75Ω, 0.6V to 1.5$V_{p-p}$)

### OUTPUT SIGNALS

TTL Level Video (4, 6, or 8 bits)
TTL Level Composite Sync (negative going)

## BUS INTERFACE

Address, data and control signals conform to Intel Multibus Specification No. 9800683
Video Select Register — Strappable on any I/O address from 00 to FFH ($FO_H$)

## CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| J1 : 86 pin edge connector, 0.156" centers — Multibus Interface | COMPAR ESM-43-DSRI |
| J2 : 60 pin edge connector, — Analog Video IN | MOLEX 15-25-8601 |
| — Digital Video Out | |
| — External Interface | |

## PHYSICAL

### SIZE

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. ( 1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5% @ 300 mA
+12V DC ±5% @ 100 mA
−12V DC ±5% @ 200 mA (4 bits)
−12V DC ±5% @ 300 mA (6 bits)
−12V DC ±5% @ 500 mA (8 bits)

### ENVIRONMENTAL REQUIREMENTS

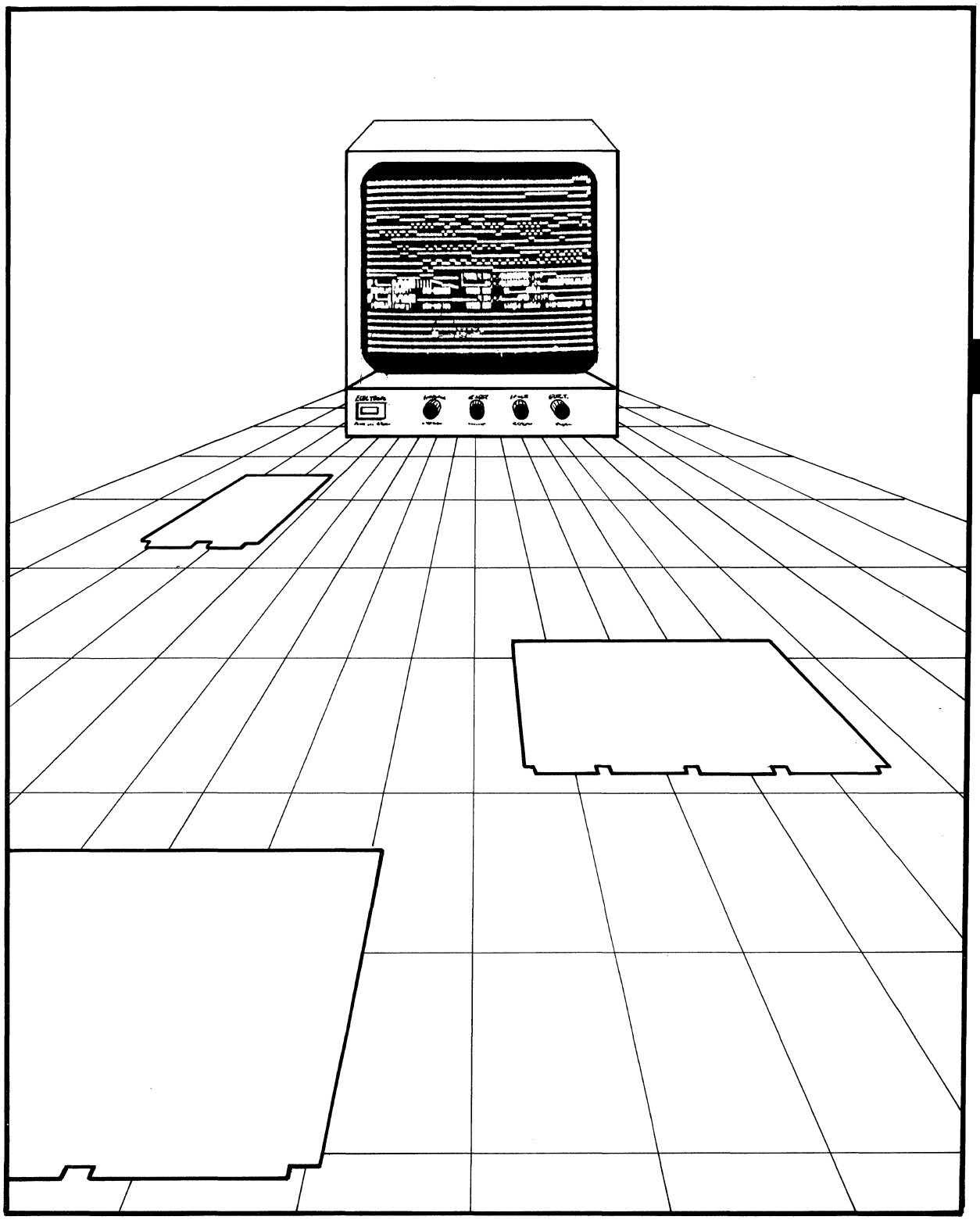
Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

## ORDERING INFORMATION

FG-01/X

X — Number of bits/pixel (4/6/8)

Example: FG-01/4: Frame grabber with a 4 bit/pixel A/D converter.



# Q-BUS (LSI-11) VIDEO BOARDS

## SECTION 2 Q-BUS (LSI-11) VIDEO BOARDS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# QRGB-GRAPH

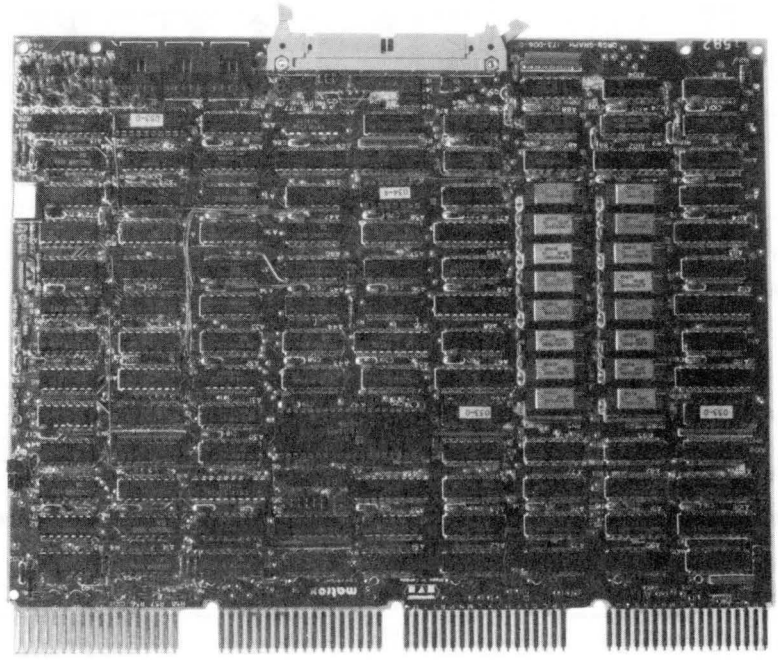
## VECTOR PLOT 512 x 512 COLOR GRAPHICS CONTROLLER FOR LSI-11 Q-BUS



- **512 x 512 pixel resolution standard**
- **4 bits/pixel expandable to 16 bits/pixel**
- **Writing speed of 800ns/pixel**
- **DMA access to video RAM**
- **Light pen interface built-in**
- **Vector plot**
- **Plug-in compatible with DEC LSI-11 Q-bus***
- **Hardware zoom, pan, scroll, and shift, clear, overlay, clipping, video enable**
- **Hardware blink**
- **Vectored interrupts**
- **Compatible with 16-bit and 18-bit addressing**
- **On-board ROM Color Look-up Table (256 shades)**
- **Add-on QRGB-ALPHA board provides color alphanumeric overlay**
- **Add-on QVAF-512 board adds:**
  - **— Real-time 512 x 512 frame grabber**
  - **— 16 million RAM color look-up table**
  - **— Hardware vector generator**

The QRGB-GRAPH is a member of Matrox's complete line of modular color video boards for the DEC LSI-11 Q-bus*. By using the latest state of the art LSI and VLSI technology, the QRGB-GRAPH provides an economical, self-contained solution for OEM color graphics applications requiring high resolution, top performance, and low cost. The board contains advanced video features such as hardware zoom, scroll, shift, pan, clipping, overlay, video masking, etc. which have previously been available only on the most expensive graphics systems at a much higher cost.

Furthermore, the QRGB-GRAPH can be combined with other Matrox color video boards such as the color alphanumerics QRGB-ALPHA and video I/O processor board, QVAF-512, (containing a real-time 512 x 512 frame grabber, color look-up table, and a hardware vector generator). The OEM system designer can now easily incorporate powerful tailor-made graphics into his system at a fraction of the cost of a turn-key system.



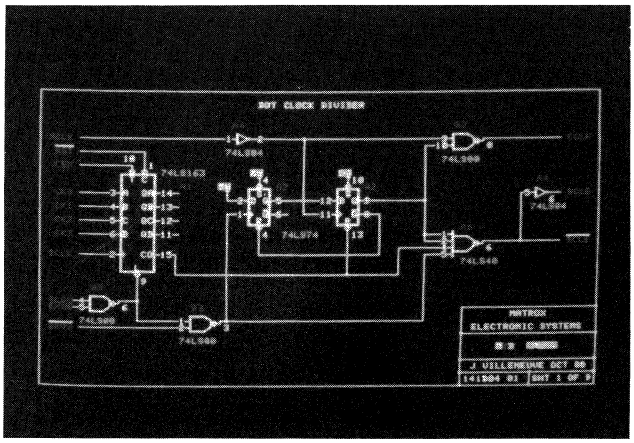


Figure 1. CAD/CAM application

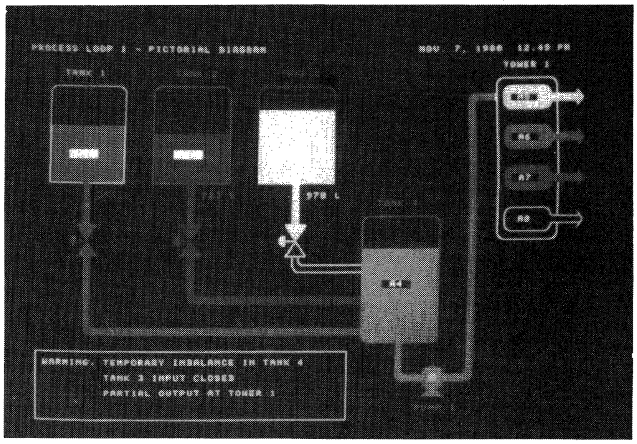


Figure 2. Process control application

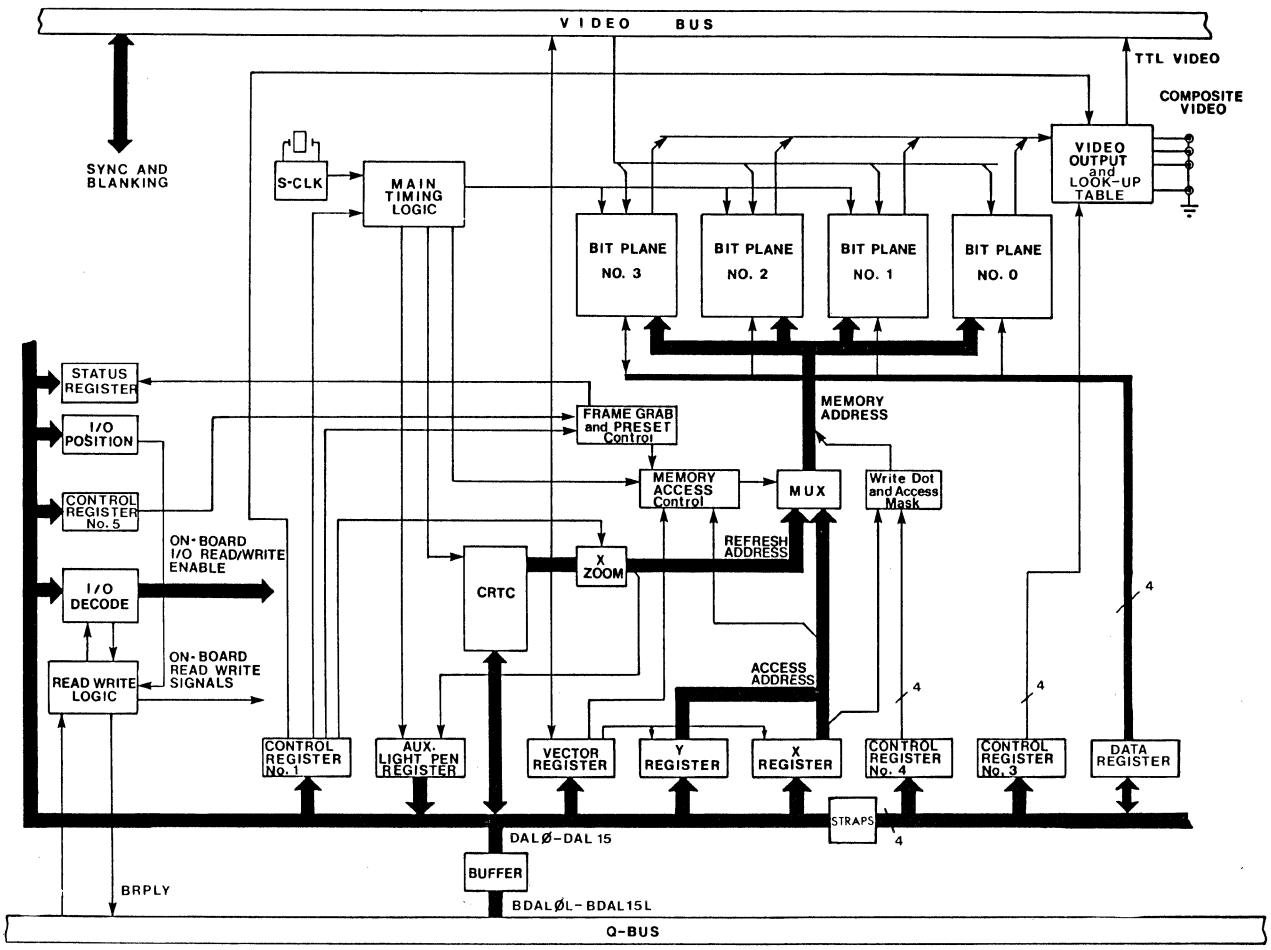



Figure 3. QRGB-GRAPH block diagram

## QRGB-GRAPH FEATURES

**Resolution:** 512 x 512 standard, 1024 x 512 optional

**Bits/Pixel:** 1-4 bits/pixel, expandable to 16 bits/pixel with additional QRGB-GRAPH boards.

**Zoom:** Independent X-zoom by 1, 2, 3, 4, 5, 6, 7, 8
Y-zoom by 1, 2, 4
Zoom works on any segment of the 512 x 512 display

**Scroll:** Up/down scroll (vertical) by multiple of 8 pixels

**Shift:** Left/right (horizontal) by single or multiple dots

**Pan:** Scroll and shift can be combined for full two dimensional pan inside the 512 x 512 area

**Clipping:** 4096 x 4096 addressable area with hardware clip to 512 x 512 for read/write and display

**Clear Display:** Memory hardware clear to zero (black). All pixels cleared in one frame (33 msec.)

**Preset Display:** Memory hardware preset to value (color) in data register. All pixels preset in one frame (33 msec.)

**Preset Mask:** Clear/Preset control of each bit plane by Plane Mask

**Color Look-Up Table:** An on-board color look-up table enables the user to select the 16 displayed colors from a palette of 256 shades. The ROM table consists of 32 separate 4 line in/8 line out software selectable partitions. The color look-up table also permits the implementation of various video effects, such as: overlay, and animation

**Blink:** The QRGB-GRAPH display can be set to blink to any of the 16 displayable colors.

**Video Mask:** The on-board color look-up table allows video on/off control of each bit plane through software

**Video Parameters:** All video parameters including horizontal and vertical syncs, blanking, frequency, and display format are user software programmable to drive any direct or composite B/W or color CRT monitor

**Video Outputs:** Direct TTL video (4), composite 75Ω R.G.B. color signals and 16-level grey scale signals are available

**Light Pen:** Detects true light pen position within one pixel accuracy. Interface built-in

**Vector Plot:** X-Y registers are auto-increment/decrement

**Display RAM:** Up to 128K byte on-board memory. CPU can read/write with 50ns (min.) and 1.2 μs (max.) access time/pixel. Memory looks like 262,144 x 4 RAM (single QRGB-GRAPH), 262,144 x 16 (four QRGB-GRAPHs)

**X, Y Pixel Address:** Each pixel can be addressed via X, Y registers (12 bits each). Data registers contains pixel color for read/write (I/O addressing)

**DMA Pixel Address:** 262,144 x 4 (8, 12, 16) display RAM can be accessed in 256 byte blocks (block base address in X, Y registers) in DMA mode for image dumping (each pixel is one memory address)

**Vectored Interrupt:** The QRGB-GRAPH can generate vectored interrupts when either a light pen strobe has been detected, or when a Display Preset command is completed. The interrupt vector, released by the QRGB-GRAPH, can be strapped to point to a service routine starting at any even word address in system memory.

**Q-bus Interface:** The QRGB-GRAPH looks to the user like 8 word wide I/O locations. All communications including pixel read/write, video functions, etc. are accomplished by I/O R/W (no DMA used). With DMA, 256 bytes of additional memory address space is used

**Access Time:** 500ns (max.) for any I/O port; 50ns (min.) — 1.2 μs (max.) for DMA

**Video Bus:** 50 pin connector provides video inputs and outputs for expanded performance using QRGB-ALPHA, QVAF-512 and additional QRGB-GRAPH boards

## ADDITIONAL ADD-ON FEATURES

### QRGB-ALPHA

**Alphanumerics:** Color alphanumeric displays can be added by the QRGB-ALPHA board (synchronized to the QRGB-GRAPH). Formats of up to 132 characters/line and up to 48 lines are user software programmable

### QRGB-GRAPH

**16 Bits/Pixel:** By connecting additional QRGB-GRAPH boards (max. 4) up to 16 bits/pixel can be obtained (each QRGB-GRAPH adds 4 bits/pixel)

### QVAF-512

**Color Look-up:** RAM video look-up table increases the number of displayable colors to $2^{24}$ = 16,772,216. CPU can read/write look-up table

**Frame Grabber:** Real-time frame grabber digitizes TV camera outputs with 4 or 8 bits/pixel resolution. Spatial resolution is 512 x 512 or 512 x 256. Single frame grab or continuous frame grab under software control

**Color Frame Grab:** By connecting R.G.B. outputs from a TV camera to the video switcher and grabbing each channel separately, a color picture can be digitized

**External Sync:** Built-in phase-lock loop synchronizes the QRGB-GRAPH to an external composite sync (serrated) for broadcast and mixing applications

**Video Switcher:** Four-input video switcher enables the user to digitize four separate TV camera inputs under software control

**Vector Generator:** On-board hardware vector generator with drawing speed of 800nsec/pixel. Vector length, slope, and texture are user defined.

## ACCESSORIES

**CRT Monitors:** Matrox supplies a full line of 9″ and 14″ monochrome monitors, as well as 12″, 14″, and 19″ high resolution (.3mm pitch) color monitors for interlaced and non-interlaced operations

**Light Pen:** High speed light pen (LP-600)

## SOFTWARE SUPPORT

**QUARTO:** The QUARTO software package includes a set of high level primitives (subroutines), similiar to those found in the CORE standard, and low level operations allowing access to all of the features on the QRGB-GRAPH card.

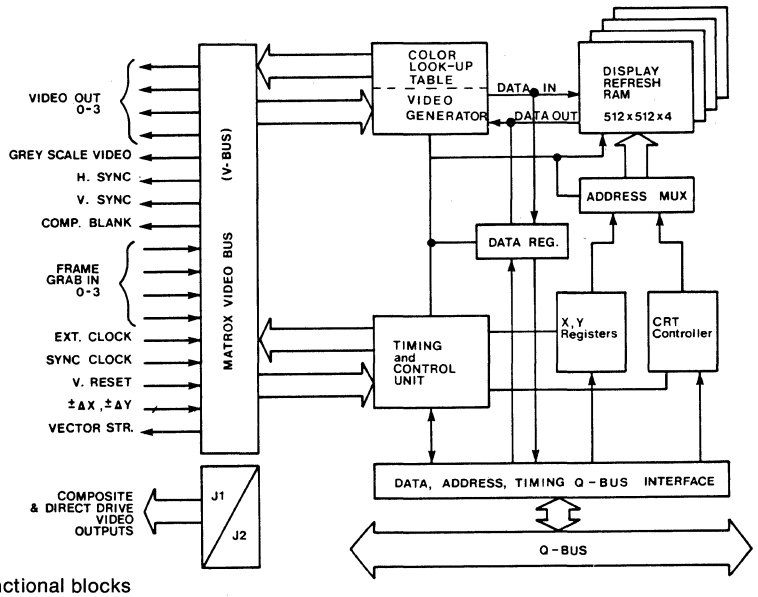



Figure 4. QRGB-GRAPH functional blocks

## FUNCTIONAL DESCRIPTION

The QRGB-GRAPH is a very complex digital graphics system on a single 10.45" x 8.43" PC board (figure 3). It consists of six main functional blocks (figure 4): CRT Controller, Video Generator, Color Look-Up Table, Display RAM, XY Registers, Timing and Control Unit, and Q-bus Interface.

The **CRT Controller (CRTC)** is a VLSI IC which provides all video timing signals including horizontal and vertical sync and blanking, display refresh RAM addresses, as well as various other timing and control signals such as cursor, light pen interface, etc. The CRT Controller is software programmable allowing the user to program parameters such as vertical refresh frequency, width and position of horizontal and vertical sync pulses (important when using non-standard CRT monitors), display resolution, etc. To the host CPU, the CRTC appears as an array of 18 registers which are indirectly addressed via two I/O ports.

The **Display Refresh Memory** is made up of 128K bytes of on-board dynamic RAM (for 512 x 512 x 4 resolution) which contains the binary picture information. Each pixel is identified by a unique address in the 262,144 address space (512 x 512). Each address contains 4 data bits which represent the pixel color. The memory is organized as four independent "planes", each containing one data bit (512 x 512 x 1). The display memory can be expanded to 16 planes through the combination of three additional QRGB-GRAPH boards.

The CPU can read/write the display RAM in one of two ways. In the XY mode the CPU loads the X and Y registers with the pixel address and then reads/writes the pixel color information through the Data Register. This mode is normally used when drawing graphics point by point. For high speed read/write operations the CPU can access the refresh memory in DMA mode. The display memory is accessed in 256 byte blocks with the starting address of the desired block loaded into the X and Y registers before executing DMA. This mode is usually used when transferring complete images from/to mass storage devices (floppy, Winchester, etc.) or for hard copies.

In addition to the CPU read/write, the display memory is continually scanned by the CRTC every 16.66ms (60 Hz) to generate video signals or, in the frame grabbing mode, to load digitized TV camera images into memory at speeds of over 100 Megabits/second. Memory access arbitration circuitry on the QRGB-GRAPH efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display refresh is "transparent" to the user.

The **X-Y Registers** are 12 bit up/down counter/latches with associated logic containing the address of the pixel being accessed by the graphics cursor (4096 x 4096 addressable area) as shown in figure 5. The CPU can load the X and Y Registers, through programmed I/O, with the pixel's absolute position. Two 8 bit ports are used for each Register. If the contents of either the X or Y Registers exceed the maximum resolution (i.e. X > 512, Y > 512) the Clip Circuit will prevent CPU read/write.

For high speed relative drawings, the vector plot feature can be used. By writing into the Vector Register the drawing direction (4 bits), the X and Y Registers are automatically incremented/decremented (figure 6).

The vector register can be interfaced with the hardware vector generator contained on the QVAF-512 board. The QVAF vector generator generates ± ΔX, ± ΔY increment/

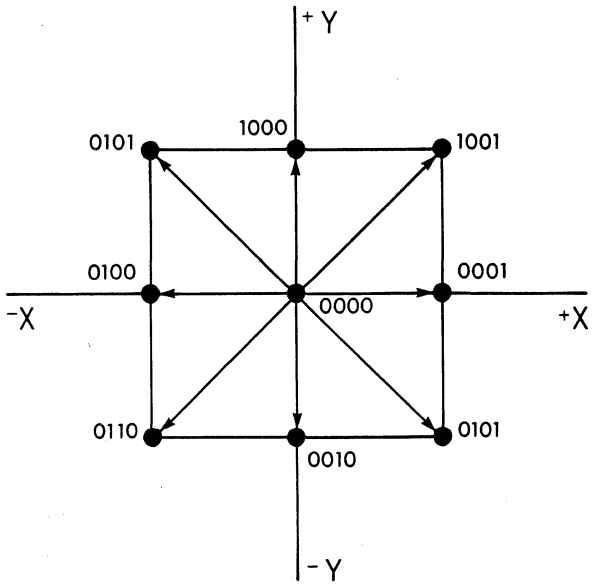



Figure 6. Vector step direction

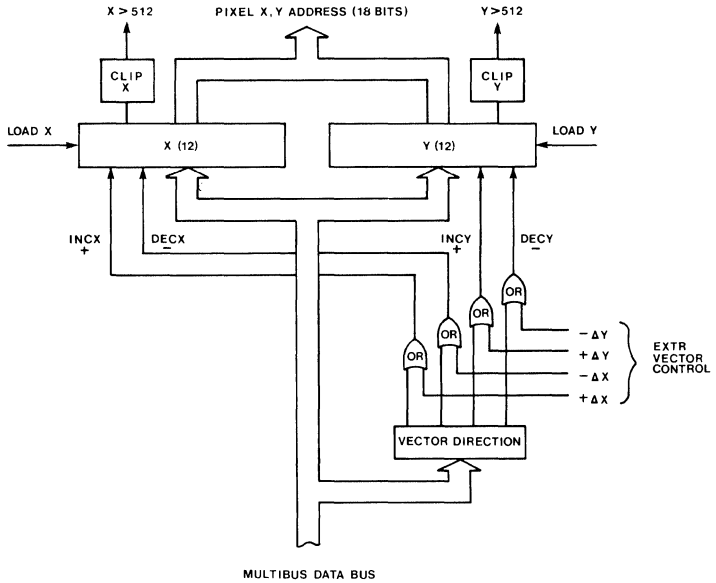



Figure 5. X-Y Registers

decrement pulses when drawing vectors, circles, etc. at the speed of 800ns/pixel. The vector plot function can also be used for drawing pictures without tying up the system bus in multiprocessor applications by connecting the ± △X, ± △Y inputs to the I/O ports of the CPU board.

The X, Y Registers are also used in the DMA mode for auto-incrementing the RAM address within the 256 byte DMA block.

The **Video Generator** performs three basic functions: conversion of digital data from the refresh RAM into the proper video signals to drive B/W and color monitors, conversion of digital video data from a frame grabber into a format required to write the data into the refresh RAM at video speeds, and the performance of various other video processing functions in hardware (zoom, scroll, clipping, etc.). The Video Generator (Video Input/Output Processor) is shown in figure 7.

Data is read from the display RAM as 4 consecutive pixels at one time for each plane (for refresh each plane looks like 512 rows x 128 strings/row x 4 1-bit pixels/string). This 4 pixel data is loaded into a shift register and then shifted out at the video clock speed (10 MHz for 512 x 512 resolution) to produce a serial TTL signal for each plane (four in total). These digital video signals are then used to address the on-board ROM Color Look-Up Table.

The **Color Look-Up Table** is contained in a 512 byte ROM, which is electrically divided into 32 16-byte blocks. Each block represents a separate 4 line in/8 line out (256 shade) color map, any of which can be selected by the user under software control (figure 8). Each "color map" is further divided into 16 locations, with each location being addressed by the four data bits from the QRGB-GRAPH display refresh memory (one bit from each memory plane). A blink bit can be ANDed with the most significant of these data bits to enable the user to blink the display between colors.

The major advantage of the on-board Color Look-Up Table is it's flexibility. By switching between color maps, the user can implement a wide range of video effects such as overlay and animation. The QRGB-GRAPH is supplied with a pre-programmed Color Look-Up Table in PROM, which is supported by the Matrox graphics software package QUARTO.

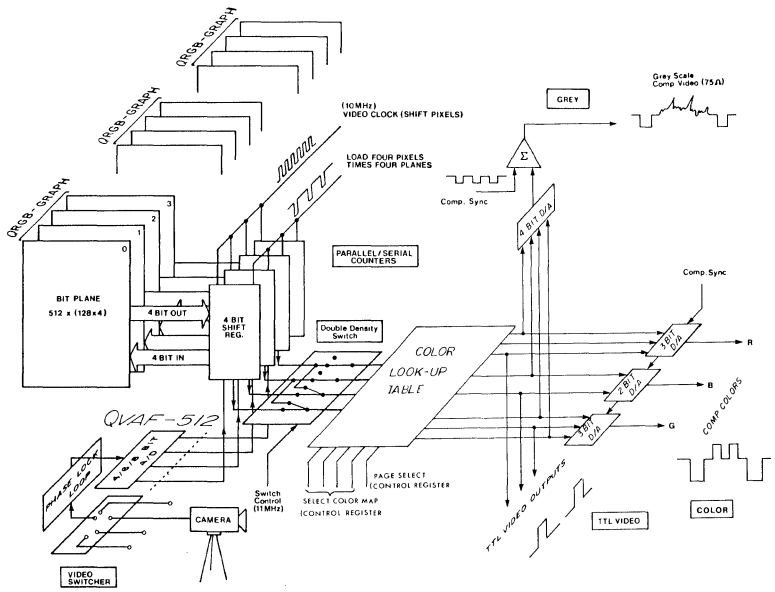



Figure 7. QRGB-GRAPH Video Generator

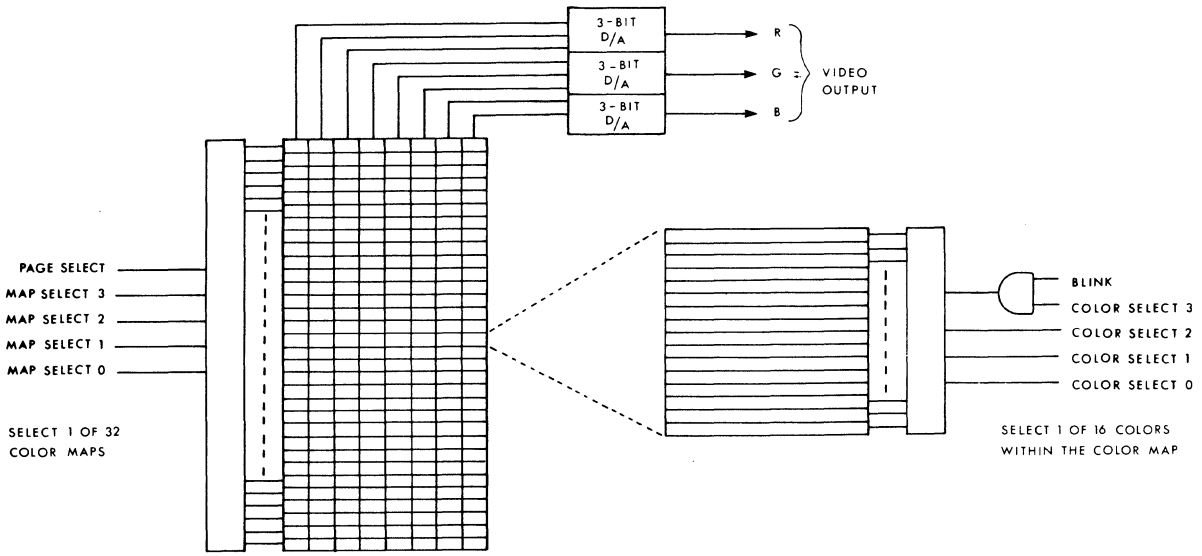



Figure 8. Color Look-Up Table

The Color Look-Up Table releases 8 bits of video data per pixel. This video information is fed to a series of D/A converters where a composite sync signal is combined with the outputs of the D/A converters to provide composite R, G, and B drives. Each color output is intensity controlled, with both red and green having 8 intensity levels (3 bits/pixel) and the blue output having 4 intensity levels (2 bits/pixel). Alternatively, four of the eight data bits (one red, one blue, and two green) can be fed to a 4-bit D/A converter which is combined with the composite sync signal for 16-level composite grey scale video signals (75Ω impedance) to drive monochrome monitors or hardcopy devices. R, G, B TTL signals are also provided for driving direct input CRT monitors and, via the Matrox video bus, for interfacing with video signals from a QRGB-ALPHA, an additional QRGB-GRAPH, or a QVAF-512 board.

While operating in the frame grabbing mode, the video signals from a TV camera via the QVAF-512 board are fed, through a phase lock loop (synchronizes the QRGB-GRAPH timing to that of the external sync), to an 8-bit 10 MHz A/D converter. The digitized video data is then serially input to a 4-bit shift register from where it is written to the display refresh memory. Note that this is exactly opposite to the generation of video signals during the read operation. Both the read and write video operations are synchronized so that the QRGB-GRAPH can operate in a continuous frame grabbing mode (write new pixel data after previous pixel is read).

Various hardware video functions are performed in different sections of the QRGB-GRAPH board rather than at one place. Video masking, overlay, and D/A conversion are performed in the Video Generator section. Vector plotting and clipping are done through the X, Y Registers, X-zoom, shift, screen clear, and selected plane clear are done in the Timing and Control Unit, and scroll, Y-zoom, user programmable video parameters and light pen interface are handled by the CRT Controller chip.

The **Timing and Control Unit** generates timing signals for the CRTC as well as all signals required by the display refresh memory (figure 9). It consists of the main oscillator (X-TAL = 10 MHz), variable modulo counters (divide by 1-8) which are controlled by the X-zoom factor to produce the appropriate load and shift signals for the display and a divide by 16 counter which, with a timing PROM, generates a series of timing signals for the memory refresh (RAS, CAS).

The **Q-bus* Interface** contains the logic required to interface the QRGB-GRAPH to the DEC LSI-11 Q-bus*. The QRGB-GRAPH looks like 8 consecutive 16-bit wide I/O locations strapped to any 16 address boundary. The CPU communicates with the QRGB-GRAPH by reading or writing into these I/O registers. The only exception is when the board is used in DMA mode. Then the display memory looks to the CPU like a 256 byte block of RAM (4, 8, 12, or 16 bits wide for 1, 2, 3, or 4 QRGB-GRAPH cards). The starting address of the 256 byte block can be positioned anywhere in the LSI-11 system I/O address space.

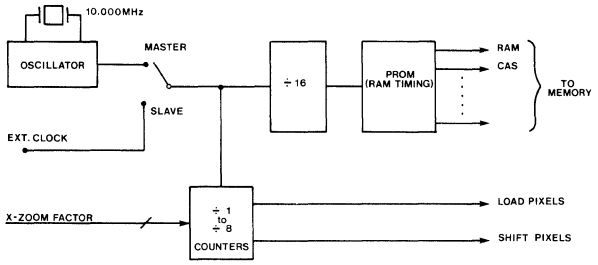



Figure 9. Timing and Control Unit

## DISPLAY SYSTEM CONFIGURATIONS

The Matrox family of advanced color graphics boards; which including the QRGB-GRAPH, QRGB-ALPHA and QVAF-512 offer the OEM system designer the unique capability to design a powerful optimal graphics system with equal or even superior performance to turn-key graphics systems, at a lower cost. Furthermore, by using general purpose OEM boards, the user can add CPUs, memory disk interface, etc. The software support package, which is supplied in the form of a graphics primitives library, further simplifies design of a custom graphics system. Hardware expansion capabilities allow extra display functions to be added by simply plugging in additional boards (more bits/pixel, higher speed, frame grabbing, etc.).

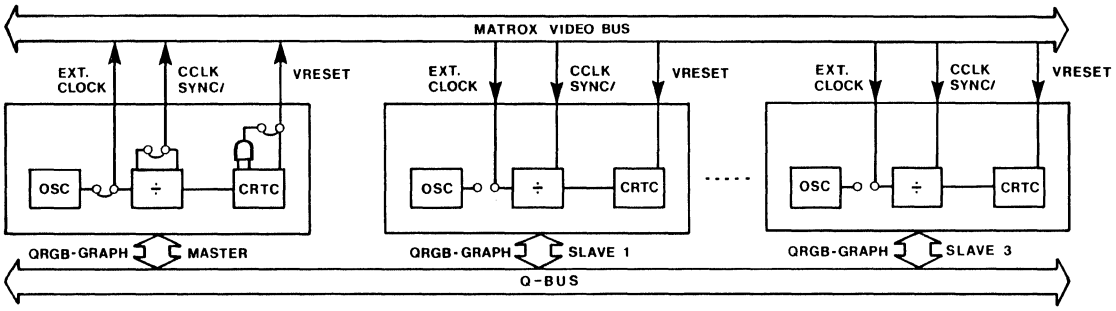



Figure 10. Multiple QRGB-GRAPH system

## SINGLE BOARD DISPLAY SYSTEM

Using a single QRGB-GRAPH board provides for a versatile graphics system that can be used in many display applications from B/W to color.

| RESOLUTION | BITS/ PIXEL | PART NUMBER | APPLICATION |
|---|---|---|---|
| 512 x 512 | 1 | QRGB-G/64/1 | B/W display systems |
| 512 x 512 | 4 | QRGB-G/64/4 | Grey scale or color display system |
| 1024 x 512 | 2 | QRGB-G/64/4 | High res. B/W, one bit for graphics and one bit for alphanumerics |

Table 1: Examples of display systems using single QRGB-GRAPH

## ADDING MORE BITS/PIXEL

Up to four QRGB-GRAPH boards can be synchronized together via the video bus (single 50 pin ribbon cable) for up to 16 bits/pixel. Each QRGB-GRAPH adds up to 4 bits/pixel.

## ADDING ALPHANUMERICS

Alphanumerics can be added to the graphics in three ways. The simplest way is to write alphanumerics, pixel by pixel, from a table stored in RAM or ROM. This offers flexibility in character size, color, position, and font but interferes with the graphics display. The second way is to use one of the bit planes on the QRGB-GRAPH exclusively for alphanumerics and overlay it with the graphics planes. The use of a separate alphanumerics and overlay it with the graphics planes. The use of a separate alphanumerics board (QRGB-ALPHA) offers the highest speed. QRGB-GRAPH and QRGB-ALPHA are synchronized via the video bus connector. The alphanumeric format (character/line x lines) is user programmable. Video signals can be ORed (on the QRGB-ALPHA) or mixed together via a color look-up table (via the QVAF-512).

## QVAF-512

The addition of a QVAF-512 board enables the QRGB-GRAPH system to digitize a real-time B/W or color video signal from a TV camera or VCR with 4 or 8 bits/pixel. Also, a high speed look-up table on the QVAF-512 expands the number of displayable colors to over 16 million. The QVAF-512 can also be used for video mixing, animation, etc. A high speed hardware vector generator executes high level graphics commands at 800ns/pixel. The QVAF-512 is synchronized via the video bus and it works in 256 x 256, 512 x 256 and 512 x 512 resolution.

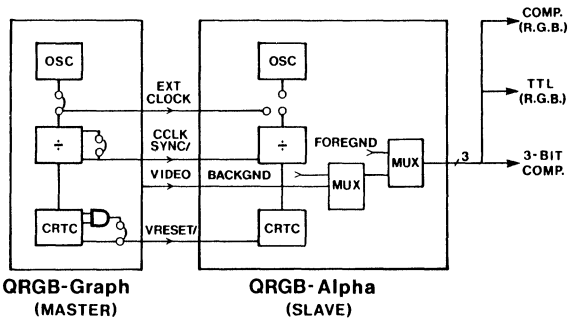



Figure 11. Alphanumerics overlay

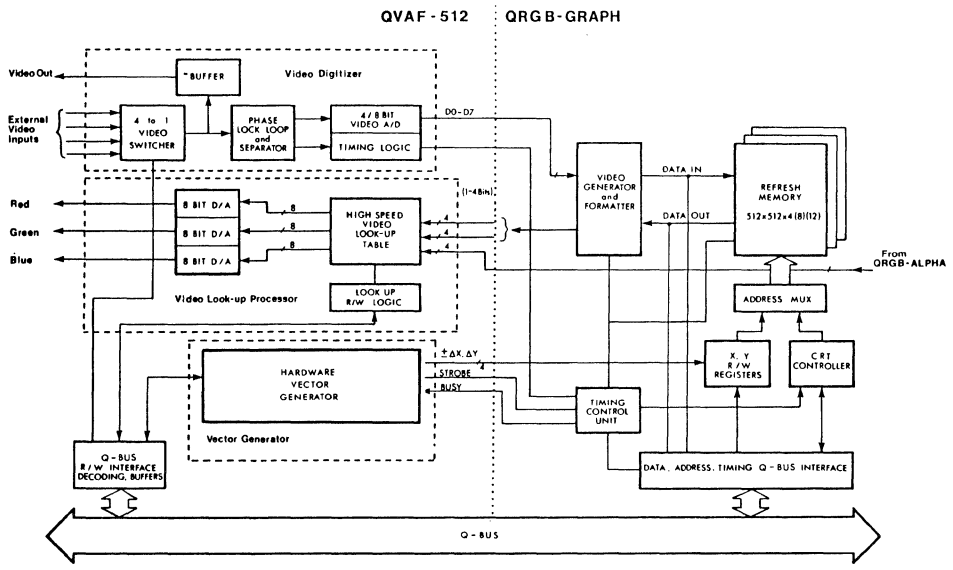



Figure 12. QVAF-512 Video Processor

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

CRTC Data, CRTC Address, CRTC Status, and Vector Register access time is fixed to 500ns.
Access time to all other locations (including DMA) varies from 50ns to 1.2 $\mu$s depending if an internal cycle is in progress at time of access.

### DISPLAY PARAMETERS

| RESOLUTION | RAM TYPE |
|---|---|
| 512 x 512 x 1 | 64K |
| 512 x 512 x 4 | 64K |
| 1024 x 512 x 2 | 64K |

2

### VIDEO TIMING

For a display format of 512 horizontal dots x 512 vertical dots on a monitor with a 51.2 $\mu$s active video time a 10.000 MHz crystal is used. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 51.2 $\mu$s | 51.2 $\mu$s |
| Horizontal Sync Frequency | 15.82 KHz | 15.82 KHz |
| Horizontal Sync Width | 4.80 $\mu$s | 4.80 $\mu$s |
| Vertical Sync Frequency | 62.2 Hz | 51.2 Hz |
| Vertical Sync Width | 189.6 $\mu$s | 189.6 $\mu$s |

### INPUT SIGNALS

Light-pen Enable
Light-pen Strobe

### OUTPUT SIGNAL

TTL Level Video: TTL level Red
TTL level Green0
TTL level Green 1
TTL level Blue
Vertical Drive
Horizontal Drive

Analog Video: Red
Green (composite)
Blue
Grey Scale (composite)

### BUS INTERFACE

Address, data and control signals conform to DEC LSI-11 Bus specifications.
Command and Status Registers — Selectable on 16 byte memory address boundaries 760 000$_8$ — 777 777$_8$ (164 400$_8$)
Display Refresh Memory (DMA only) — Selectable on 256 byte memory address boundaries 760 000$_8$ — 777 777$_8$ (164 000$_8$)
Interrupt Vector Address — Selectable on any even word address — (400$_8$)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| A: 36 pin edge connector, 0. 125" centers,<br>B: 36 pin edge connector, 0.125" centers,<br>C: 36 pin edge connector, 0.125" centers,<br>D: 36 pin edge connector, 0.125" centers, | LSI-11 Bus interface | DEC H8030 (2 required) |
| J1: 10 pin right angle header, Analog video outputs | | AMP 87922-1 |
| J2: 10 pin right angle header, TTL video outputs | | AMP 87922-1 |
| J3: 50 pin right angle header, Matrox video bus | | Molex 15-25-4505 |
| J4: 10 pin right angle header, Keyboard and lightpen interface | | AMP 87922-1 |

### PHYSICAL

#### SIZE

Width — 10.45 in. (26.54cm)
Height — 8.43 in. (21.41cm)
Depth — 0.50 in. (1.27cm)

#### POWER REQUIREMENTS

$\pm$5V DC $\pm$5% @2A

#### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

QRGB-G / 64 / X
└— Number of bits/pixel (1/4)

Example: QRGB-G/64/4: 512 x 512 color graphics controller with four bit planes

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# QVAF-512

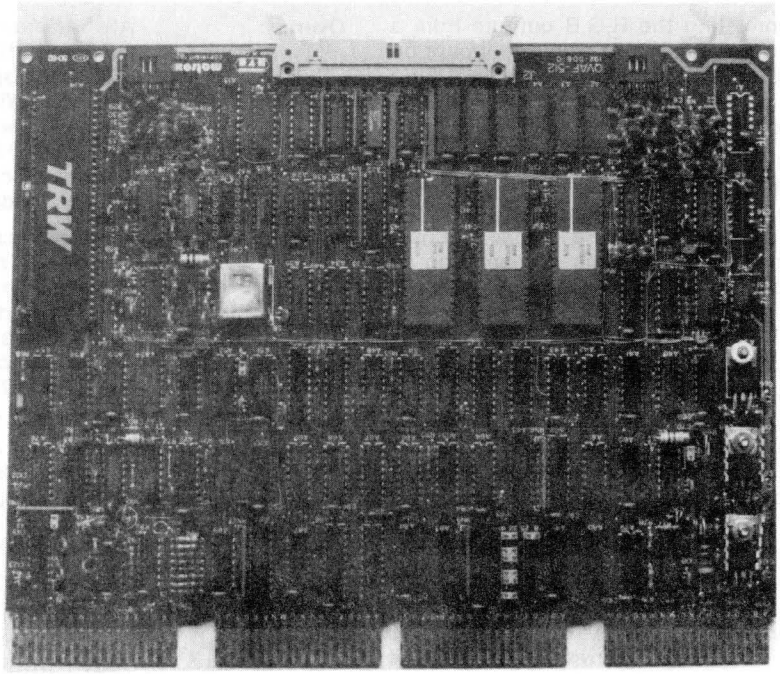
## QRGB-GRAPH VIDEO INPUT/OUTPUT PROCESSOR FOR LSI-11 Q-BUS



- **Real Time Video Frame Grabber**
  - **4 or 8 bit A/D**
  - **4 input video switch**
  - **Programmable clamping and gain**
  - **Internal/external, block/serrated sync**
  - **Phase locked loop for Genlock**
- **Color Look-Up Table (RAM)**
  - **10 input lines/24 output lines**
  - **Three 8 bit D/A converters (R,G,B)**
  - **16 million color palette**
  - **Blink and overlay control**
- **Hardware Vector Generator**
  - **High speed line drawing (800ns/pixel)**
  - **Length, slope, and texture control**
- **LSI-11 Q-Bus* Compatible**
- **Works With QRGB-GRAPH Board**
- **QRGB-ALPHA Overlay Compatibility**
- **American/European Operation**

The QVAF-512 is a video I/O processor board designed to extend the performance of the Matrox QRGB-GRAPH video controller. The QVAF-512 has three main subsections: a real time video digitizer (frame grabber), a color look-up table, and a high speed vector generator. The video A/D converter provides real time grey scale digitizing, of a camera, videodisk, or VCR signal (4 or 8 bits/pixel), into one or two QRGB-GRAPH frame buffers. The color look-up table provides a palette of over 16 million output shades and colors. The look-up table can accomodate one or two QRGB-GRAPH boards and a QRGB-ALPHA. The on-board vector generator provides high speed line drawings (800ns/pixel). The length, slope, and texture of the displayed lines are all software controlled.

The QVAF-512 plugs into any standard LSI-11 Q-bus backplane and interfaces to the QRGB-GRAPH/QRGB-ALPHA via a single 50-pin ribbon cable. The board will operate in either American or European standard systems.



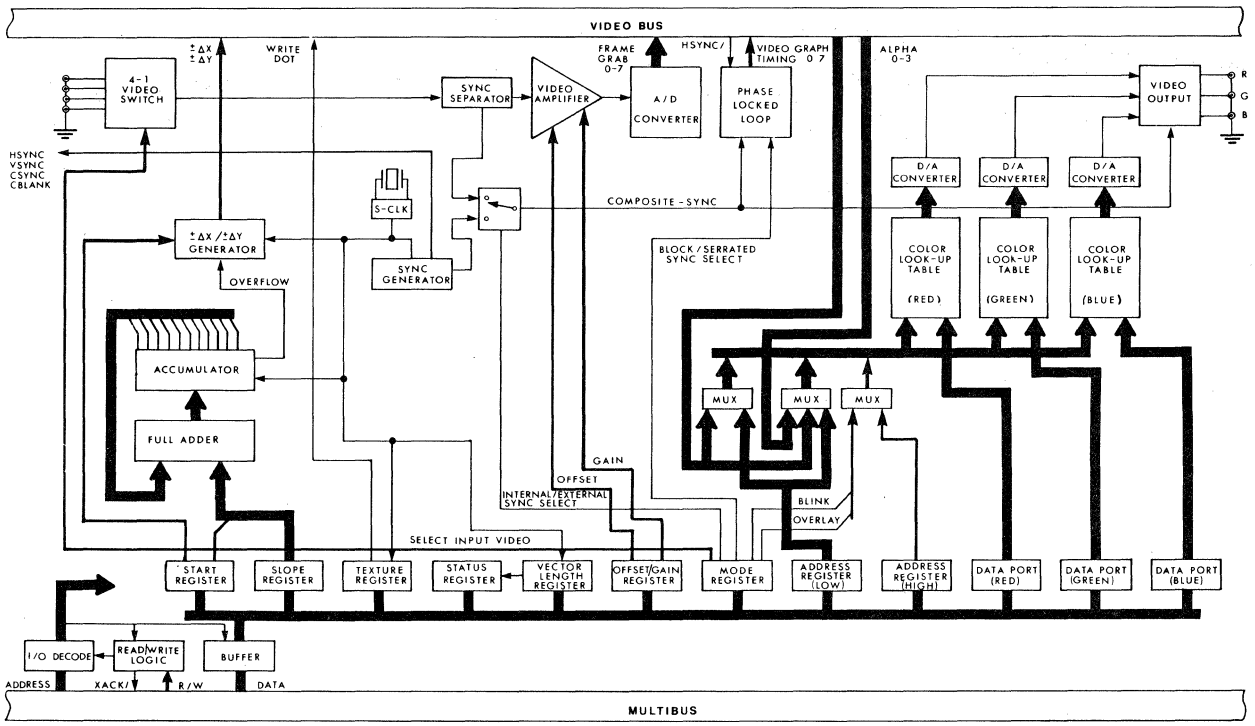



Figure 1. QVAF-512 block diagram

## QVAF-512 FEATURES

### FRAME GRABBER

**High Speed A/D Converter:** The QVAF-512 contains an on-board 10 MHz A/D converter for real-time frame grabbing applications. Images can be digitized to either 4 or 8 bits/pixel.

**4 Input Video Switch:** Up to four different analog video inputs can be accepted by the QVAF-512. Each video source can be individually selected for frame grabbing under software control.

**Color Frame Grabbing:** By connecting the R,G,B outputs from a color video camera to separate inputs on the video switcher, and then grabbing each channel separately, a color picture can be digitized.

**Software Controlled: Gain and Offset:** The QVAF-512 Frame Grabber enables the user to introduce a software programmable gain and/or offset to the input video signal. This feature enables the user to concentrate the digitizing operation on that part of the input signal which contains most of the video information — effectively increasing the contrast.

**Programmable Sync:** Under software control the QVAF-512 can be programmed to lock to either block or serrated sync. Sync signals can be generated on-board, or stripped from the input video signal for broadcast and video mixing applications.

### VECTOR GENERATOR

**High Speed Line Drawings:** Vectors can be drawn to the graphics display, via the QVAF-512 hardware Vector Generator, at speeds that are 20 to 40 times faster than conventional software vector generation techniques.

**Vector Texture Control:** The texture of the displayed vectors (dotted, dashed, solid, etc.) can be programmed by the user through an on-board 16 bit Texture Register. Up to 65,000 different texture patterns can be defined.

### COLOR LOOK-UP TABLE

**Programmable Colors:** The QVAF-512 Color Look-Up Table allows the user to select the available display colors from over 16 million possible shades. Up to 16 colors can be displayed with systems using one QRGB-GRAPH board, and 256 colors can be displayed using two QRGB-GRAPH boards.

**Overlay:** Alphanumeric characters (from the QRGB-ALPHA) can be overlayed on the graphics display through the Color Look-Up Table. When characters are to be overlayed on the display, the 4 bits from the QRGB-ALPHA board will replace the four most significant graphics bits on the look-up table address lines.

**Blink:** The graphics display can be set to blink between any of the available display colors. The QVAF-512 can also be programmed to blink only the overlayed alphanumeric characters. The blink frequency can be software selected for 1.8 Hz or 3.75 Hz.

**Q-Bus Interface:** The QVAF-512 looks to the user like 7 consecutive I/O locations. All communications between the host CPU and the QVAF-512 (including read/write operations to the Color Look-Up Table) are accomplished via I/O read/write.

**ACCESS TIME:** Time from CMD/to BRPLY/ for all registers is less than 50ns.

**VIDEO-BUS:** A 50 pin connector provides all the video input and output lines required to interface the QVAF-512 with up to two QRGB-GRAPH boards and one QRGB-ALPHA board.

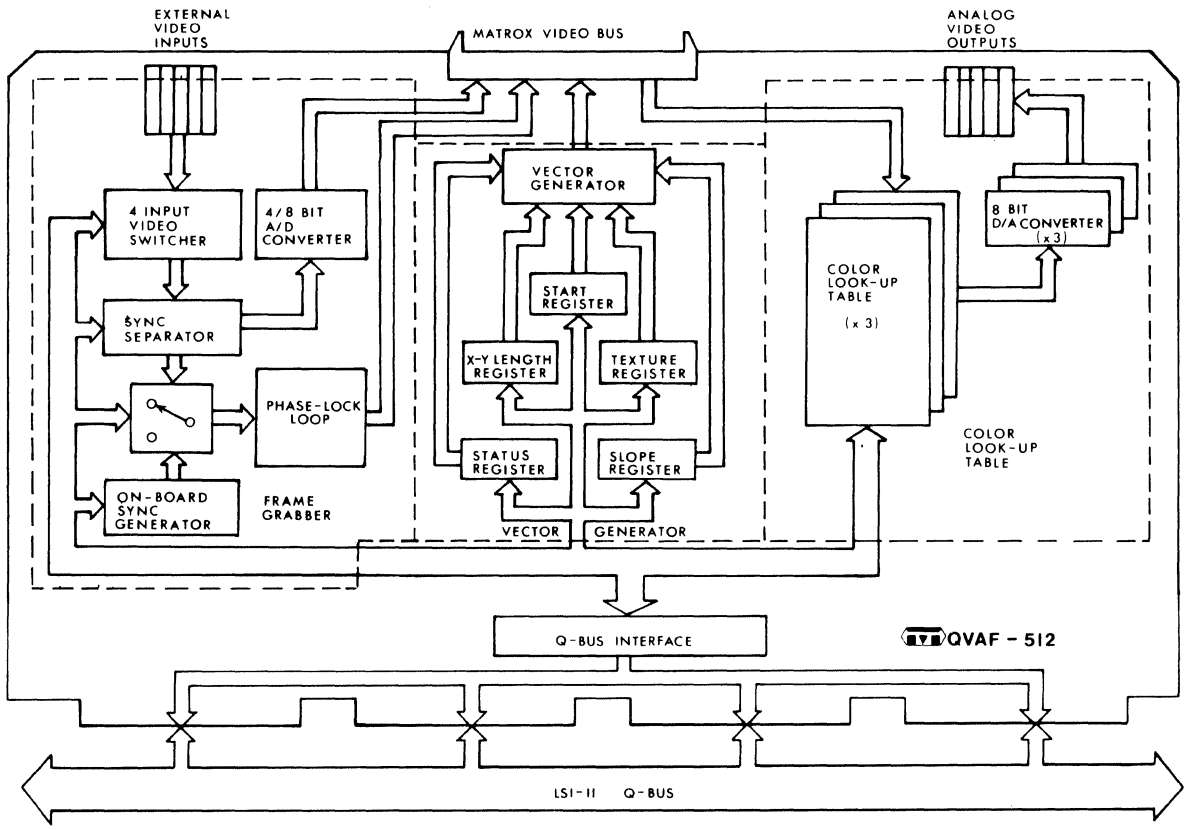



Figure 2. QVAF-512 functional blocks

## FUNCTIONAL DESCRIPTION

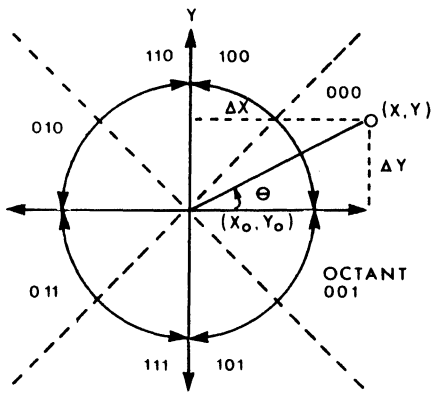
The QVAF-512 has been designed to complement the operation of Matrox's QRGB-GRAPH/QRGB-ALPHA family of color video controllers. The QVAF-512 comprises three independent operational sections (figure 2) contained on a single Q-bus compatible PC board.

The on-board **Hardware Vector Generator** provides an efficient means of drawing vectors to the QRGB-GRAPH display memory. Three parameters are required to specify a line draw operation; length, slope, and texture. The 10 bit Length Register stores the length of the larger of the two components ( $\Delta X$, $\Delta Y$). This permits vectors of up to 1024 pixels to be drawn with a single software Write command. A 10 bit Slope Register stores, with single pixel precision, the $\tan\theta$ where $\theta$ is an angle between 0° and 45°. Three bits in the Start Register define the proper octant. The Vector Generator circuit calculates the X and Y addressing, as required by the QRGB-GRAPH, on a pixel by pixel basis until the full vector has been drawn. A Busy Flag in the Status Register or a hardware interrupt can be used to indicate completion.

The texture of the displayed vector is stored in a 16 bit Texture Register. The contents of the Texture Register defines a 16 bit repeating pattern of pixel information (figure 4). In this way solid, dotted, dashed, and hidden vectors can be drawn. Note that the Data Register on the QRGB-GRAPH board is used to set the color of the vector.

The hardware Vector Generator operates with a drawing speed of 800ns/pixel. This represents an increase of about 20 to 40 times the conventional drawing speeds acheived by software vector generation.

The QVAF-512 **Frame Grabber** enables the user to digitize a frame of video information (from an external video camera, VCR or video disk), with either 4 or 8 bits per pixel, and store that frame in the QRGB-GRAPH display memory (512 x 512 x 4 bits per GRAPH board). Using commands issued by the QRGB-GRAPH, this frame grabbing operation can be continuous (QRGB-GRAPH will display a continually updated or "live" picture) or one shot, effectively "freezing"




IF $|\Delta X| \geq |\Delta Y|$
THEN LENGTH = $|\Delta X|$
AND SLOPE = $\left|\frac{\Delta X}{\Delta Y}\right|$

IF $|\Delta X| < |\Delta Y|$
THEN LENGTH = $|\Delta Y|$
AND SLOPE = $\left|\frac{\Delta Y}{\Delta X}\right|$

Figure 3. Determining vector length and slope parameters

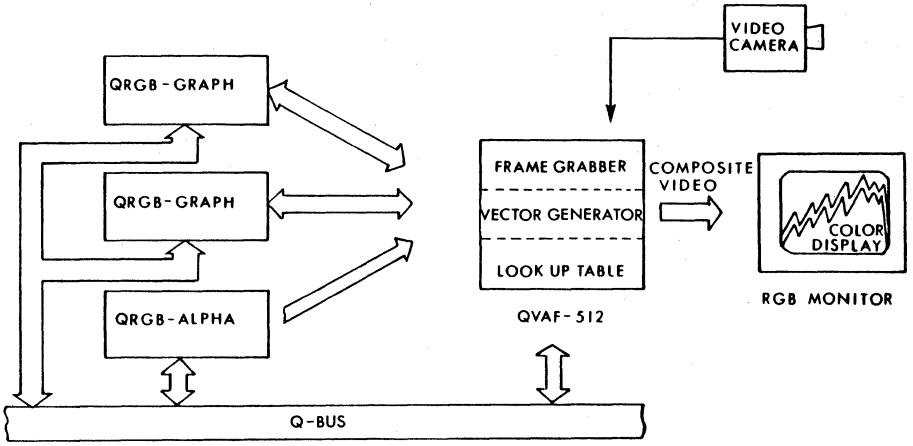



Figure 5. QVAF-512 in system

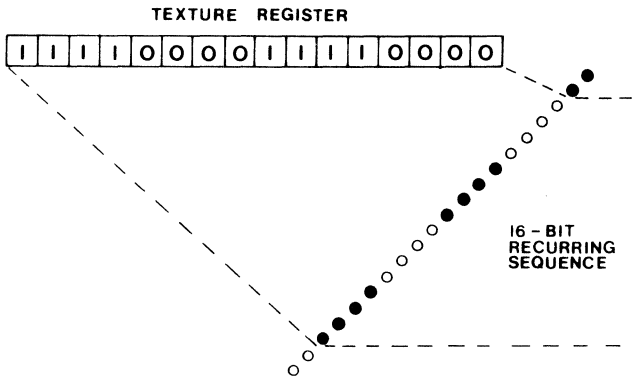



Figure 4. Defining the "Texture" pattern for the displayed vectors

the action. Up to four video cameras can be interfaced to the QVAF-512 through an on-board four input video switcher which permits software selection between the four video sources.

Incorporated into the design of the frame grabber is a Phase-Lock Loop circuit (PLL). The PLL uses the sync signal stripped from the input video signal as a reference frequency to which it synchronizes the rest of the system (QRGB-GRAPH/QRGB-ALPHA). If required, an on-board sync generator (strappable for American EIA or European CCIR standard sync) can be software-selected to act as a master sync source for both the video display boards and the video source. The PLL can also be programmed to accept either block or serrated sync.

The QVAF-512's frame grabber provides software control over the gain of the input signal. This feature, together with a software-variable voltage offset (clamping level) on the input, allows the user to take advantage of the full digitizing range of the A/D converter for a given input signal amplitude. This technique can be used to concentrate the operation of the A/D converter on that part of the input signal that contains the most video information, in effect increasing the contrast of the image. There are sixteen different levels of gain and sixteen different levels of offset.

The QVAF-512 **Color Look-Up Table** is made up of three 1K x 8 RAM look-up tables (one for each primary color: red, green,and blue), each of which are divided into four 256 byte sections: Normal, Overlay, Blink, and Blink And Overlay. These Color Look-Up Table provide the QRGB-GRAPH with a color palette of over 16 million colors. To display a

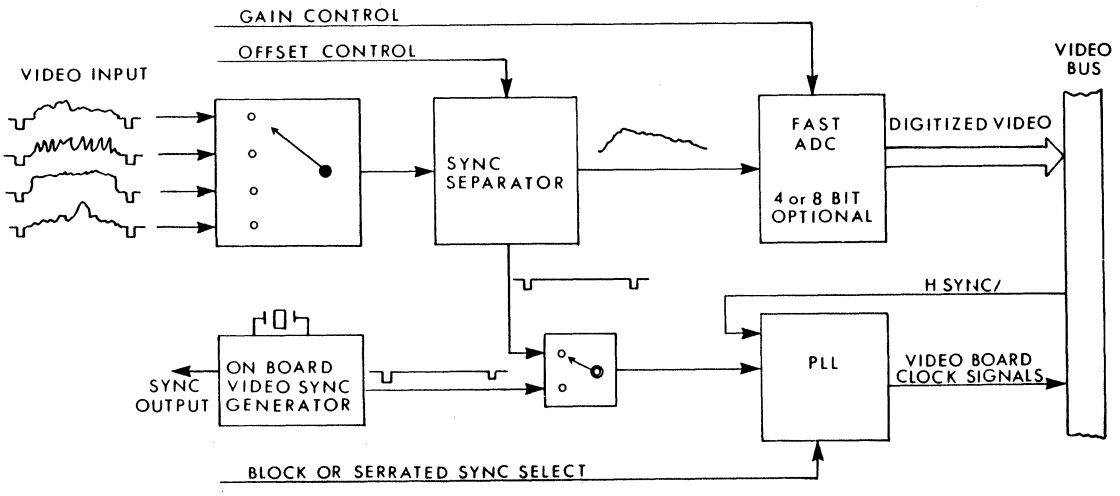



Figure 6. Frame Grabber

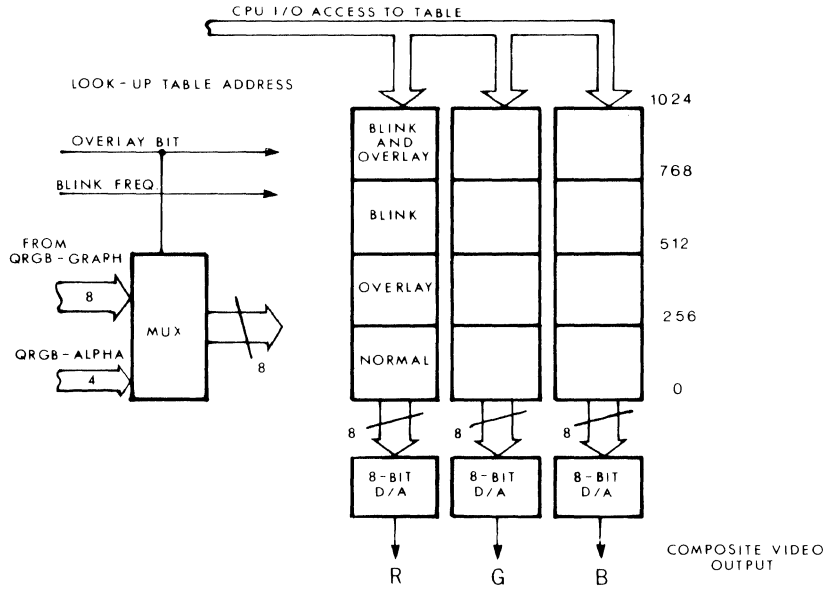



Figure 7. Color Look-Up Table

desired color at a certain pixel location, the user simply loads that color's look-up table address into the QRGB-GRAPH display memory location corresponding to the pixel position. The contents of the look-up table can be changed at any time. A single QRGB-GRAPH board (4 bits) can address 16 different locations in the look-up table. Two QRGB-GRAPH boards (8 bits) can address up to 256 locations in the look-up table. Additionally, the Color Look-Up Table is sectored into four 256 byte blocks (figure 5) in order to allow separate color mappings for overlayed alphanumerics and for blinking. The blink rate is software selectable to be either 1.8 Hz or 3.75 Hz.

When an QRGB-ALPHA is interfaced to the QVAF-512 the four bits from the alpha board replace 4 of the 8 graphic bits in addressing the Color Look-Up Table. When at least one of these bits is high (alphanumeric data is to be displayed) access to the look-up table is shifted to the Overlay section which contains its own color map. As a result, alphanumeric text from the QRGB-ALPHA can be superimposed (overlayed) on the graphics background. The user can also program the QVAF-512 to blink the alphanumeric characters between the colors defined in the Overlay and Overlay And Blink sections of the look-up table (similar to blinking graphics pixels between the Normal and Blinking sections). This method of generating blinking characters is very flexible as it allows characters to blink to colors other than their background color.

## MATROX VIDEO BUS

The QVAF-512 is interfaced to the QRGB-GRAPH and QRGB-ALPHA boards by way of a 50-pin Matrox Video Bus. Digitized video data as well as $\triangle X$ and $\triangle Y$ increment/decrement strobes are bussed from the QVAF-512 to the QRGB-GRAPH. The Video Bus also carries the 4 TTL video bits from each of the QRGB-GRAPHs and the QRGB-ALPHA boards for color look-up on the QVAF-512.

## BUS INTERFACE

The QVAF-512 plugs directly into the LSI-11 Q-Bus. The seven Command and Status Registers are positioned on any 8 word I/O address boundary between 760 000$_8$ and 777 777$_8$

## PROGRAMMING

The QVAF-512 is programmed via seven on-board I/O registers. On power-up or reset all control registers must be loaded with the QVAF-512's operational parameters (table 1).

| REGISTER | ADDRESS | DEFINITION |
|---|---|---|
| TEXTURE REGISTER | BASE + 0 | 16 bit vector texture pattern |
| VECTOR LENGTH REGISTER | BASE + 2 | 10 bit vector length |
| GAIN/OFFSET/MODE REGISTER | BASE + 4 | Select gain/Select offset/Select input video to frame grabber/Enable on-board sync generator/Select block sync/Enable overlay/Enable blink frequency/Enable blink |
| VECTOR REGISTER | BASE + 6 | 10 bit vector slope/Complement Texture Register/Vector slope < 45/vector quadrant |
| STATUS REGISTER | BASE + 10 | QVAF-512 status |
| ADDRESS REGISTER | BASE + 12 | 10 bit look-up table address/Select look-up table |
| DATA PORT | BASE + 14 | Read/write data to the selected look-up table |

Table 1. Register Definitions

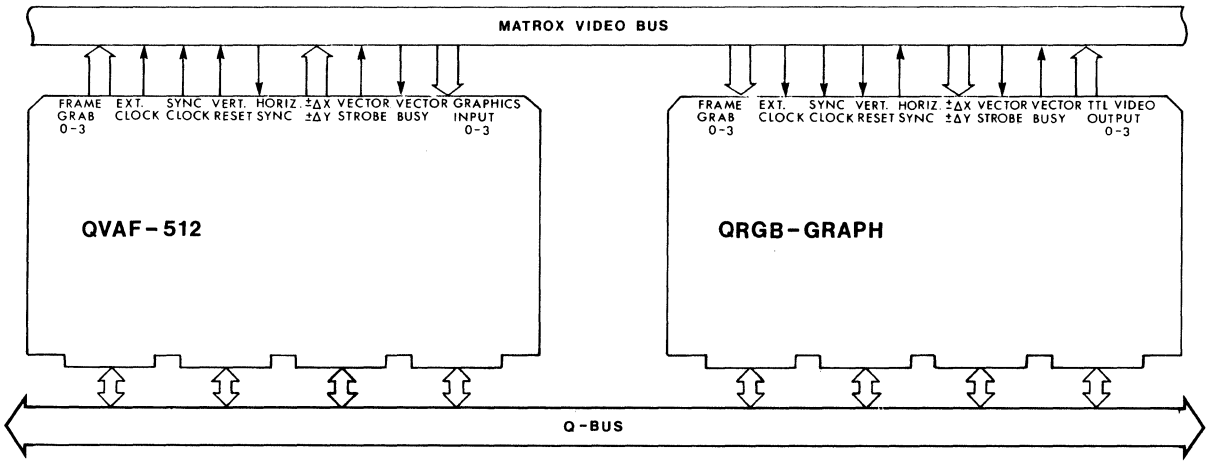



Figure 8. 512 x 512 x 4 video imaging system

## DISPLAY SYSTEM CONFIGURATIONS

The Matrox family of advanced color video boards, which include the QVAF-512, QRGB-GRAPH, and QRGB-ALPHA, offer the OEM system designer a unique capability to design a powerful optimal graphics system with the equal or even superior performance of a turn-key graphics system — at a lower cost. Furthermore, by using general purpose OEM boards, the user can add CPUs, memory disk interfaces, etc. to configure his system to his exact requirements. Software support, in the form of a graphics primitive library, further simplifies design of the custom video systems. Hardware upward capability enables adding extra display functions by simply plugging in additional boards (more bits/pixel, higher speed, alphanumeric overlay, etc).

### 4 BIT/PIXEL IMAGING SYSTEM

Combining the QVAF-512 with a single QRGB-GRAPH (figure 8) yields a video imaging system using 4 bits/pixel. Whole frames of video picture information with up to 16 color or grey levels can be digitized and stored in the display memory of the QRGB-GRAPH.

### 8 BIT/PIXEL Imaging system

Adding another QRGB-GRAPH graphics controller to the system (figure 9) doubles the number of bit planes to eight. This enables the system to store and display images with a resolution of 512 x 512 dots using up to 256 colors or grey levels.

An alphanumerics overlay can also be added to the graphics display by plugging in a QRGB-ALPHA alphanumerics controller to the system.

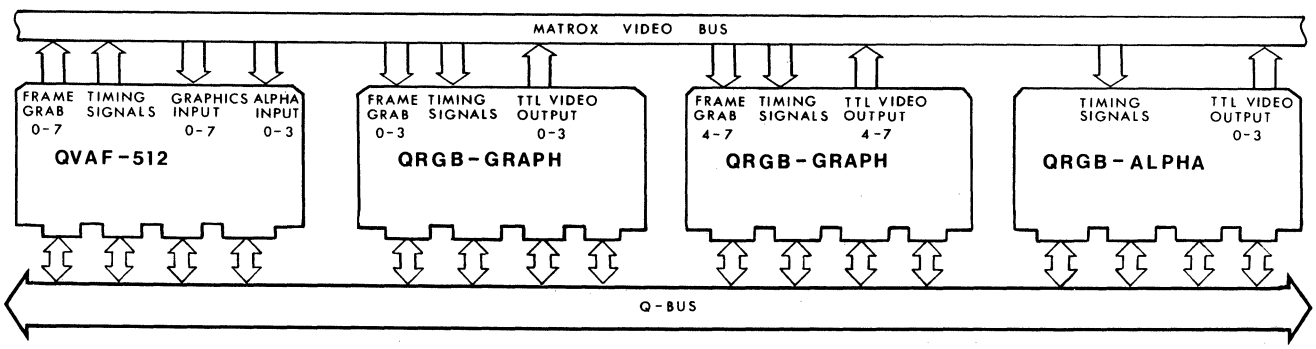



Figure 9. 512 x 512 x 8 video imaging system with alphanumerics overlay

# SPECIFICATIONS

## FUNCTIONAL

## OPERATIONAL PARAMETERS

## VECTOR GENERATOR

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Drawing Speed | 800ns/pixel (512 x 512 resolution) |
| Vector Texture | 65,000 texture patterns (software selectable) |

## FRAME GRABBER

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Spatial Resolution | 512 x 512 max. |
| Video Inputs | 4 analog video inputs (software switchable) |
| Sync | Internal/external, block/serrated (software selectable) |
| Bits/pixel | 4 or 8 bits |
| Offset | 16 increments from Black level to nominal mid-range (software selectable) |
| Gain | 16 increments from 0.7 to 1.9 of nominal (software selectable) |

## COLOR LOOK-UP TABLE

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Palette Size | $2^{24}$ = 16,777,216 colors |
| Addressable Colors | 16 colors (1 x QRGB-GRAPH)/256 colors (2 x QRGB-GRAPH) |
| Blink Rate | 1.8 Hz/3.75 Hz (software selectable) |

## INPUT SIGNALS

ANALOG INPUTS:
- Camera 0
- Camera 1
- Camera 2
- Camera 3

TTL LEVEL INPUTS:
- 4/8 graphics bits
- 4 overlay bits
- HSYNC/
- BUSY/

## OUTPUT SIGNALS

ANALOG OUTPUTS:
- Composite Video (RED)
- Composite Video (BLUE)
- Composite Video (GREEN)

TTL LEVEL OUTPUTS:
- 8 Video Bits
- System Clock
- ± △X, ± △Y
- V. Reset
- Composite Sync
- Horizontal Sync
- Vertical Sync
- Composite Blanking

## BUS INTERFACE

Address, data, and control signals conform to DEC LSI-11 Q-bus specifications.
Command and Status Registers — Selectable on any 8 word I/O address boundaries $760\ 000_8$ - $777\ 777_8$

## CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| A: 36 pin edge connector, 0.125" centers | LSI-11 Bus interface | DEC H8030 (2 required) |
| B: 36 pin edge connector, 0.125" centers | | |
| C: 36 pin edge connector, 0.125" centers | | |
| D: 36 pin edge connector, 0.125" centers | | |
| J1: 10 pin right angle header | — Composite Video Output | AMP 87922-1 |
| J2: 10 pin right angle header | — Analog Video Input<br>— Sync Output to Camera | AMP 87922-1 |
| J3: 50 pin right angle header | — Matrox Video Bus | MOLEX 15-25-4505 |

## PHYSICAL

### SIZE

WIDTH: 10.45 in. (26.54 cm)
HEIGHT: 8.43 in. (21.41 cm)
DEPTH: 0.50 in. ( 1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5% @ 3.2A
+12V DC ±5% @ 120mA
−12V DC ±5% @ 0.95A (QVAF-512/8)*
−12V DC ±5% @ 0.55A (QVAF-512/4)*

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 90% non-condensing

## ORDERING INFORMATION

QVAF-512/X-XX

- AS — American standard (60Hz)
- ES — European standard (50Hz)
- Number of bits per pixel (4/8)

Example: QVAF-512/8-AS: American standard board with a 8 bit/pixel A/D converter (frame grabber).

*The −12V power supply is not installed on all DEC systems.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# QRGB-ALPHA

## PROGRAMMABLE COLOR ALPHANUMERIC DISPLAY CONTROLLER FOR LSI-11 Q-BUS

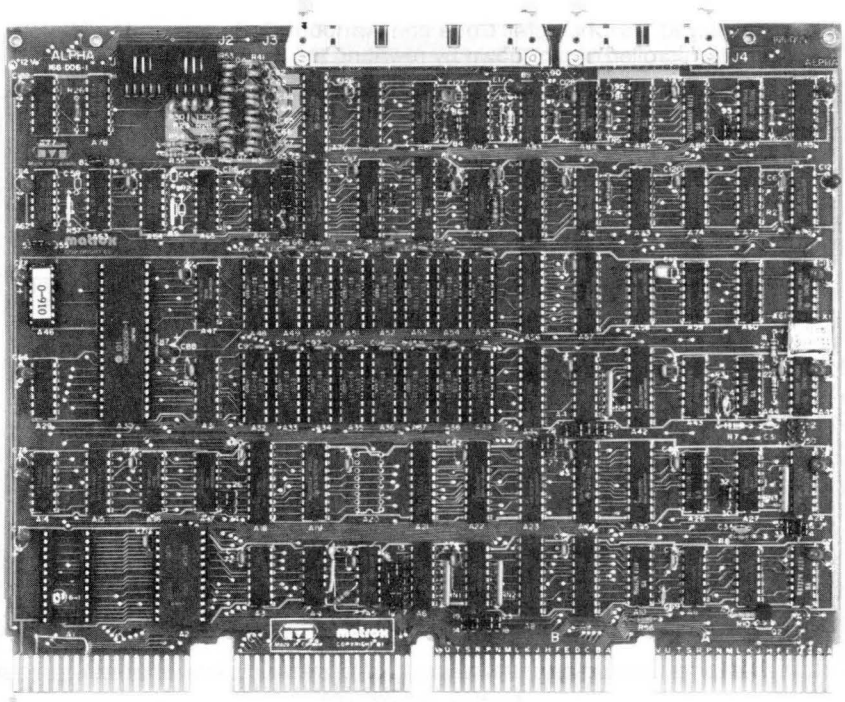


- **User Programmed Display Format**
- **Up to 4000 Characters**
- **8 Display Colors**
- **Blink**
- **Double Height Characters**
- **Underline**
- **Addressable Cursor**
- **LSI-11 Q-Bus* Compatible**
- **Keyboard Interface**
- **Light Pen Interface**
- **RAM and EPROM Character Generator**
- **Transparent Memory**
- **50 or 60 Hz Operation**
- **Drives any RGB Color Monitor**
- **Works with 16-bit and 18-bit addressing**

The QRGB-ALPHA is an LSI-11 compatible, color video display controller card which allows the display (characters/line x lines/page) and character formats (5 x 7, 7 x 9, etc.) to be set by programmed I/O commands. Each character is displayed in 1 of 8 foreground colors on 1 of 8 background colors. Characters may be either single or double height and either normal, blinking at 2 Hz or underlined.

The character font provided with the QRGB-ALPHA contains 128 — 5 x 7 dot upper/lower case alphanumeric characters and graphics symbols. By adding a second character generator ROM/RAM, 128 additional symbols may be defined. When using a RAM character generator, the character font may be rewritten at any time by the system processor.

The QRGB-ALPHA works with all monochrome and color (RGB) video monitors in Europe (50 Hz) and America (60 Hz). Interfaces for a high-speed light pen and an 8-bit parallel keyboard are also provided.



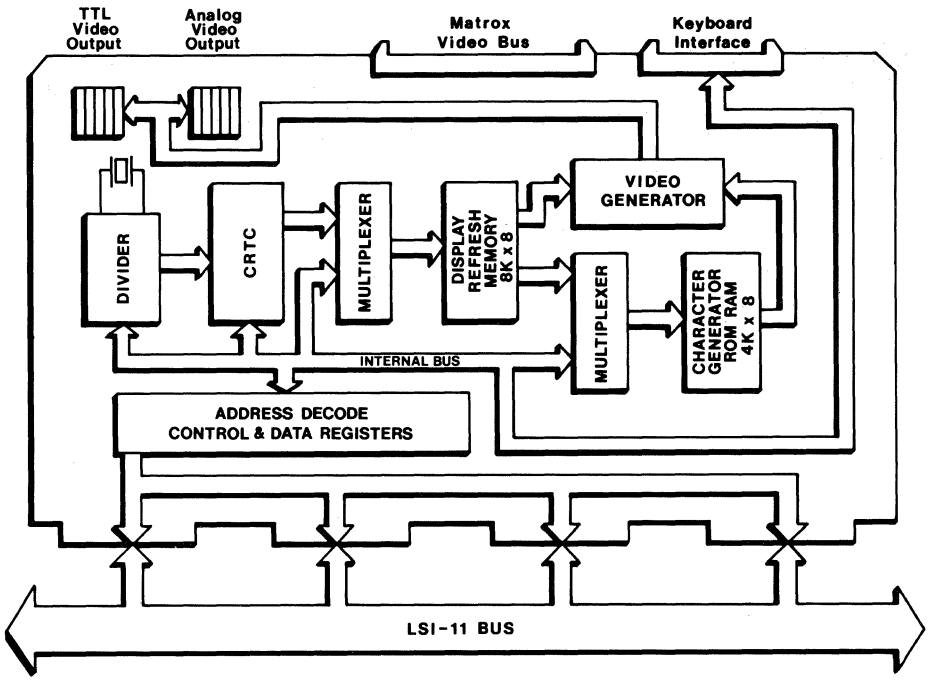



Figure 1. QRGB-ALPHA block diagram

## FUNCTIONAL DESCRIPTION

The block diagram, Figure 1, shows the major functional components of the QRGB-ALPHA.

## CRT CONTROLLER

In the design of the QRGB-ALPHA, the 6845 CRT controller replaces many of the SSI/MSI components used in older designs and provides the QRGB-ALPHA with features previously found only in the most expensive equipment. All display parameters are now user specified and displays can be configured to have virtually any combination of rows and columns up to a maximum of 4000 characters. In addition, the character cell size is variable and accommodates all commonly used character font sizes (5 x 7, 7 x 9, etc.).

## DISPLAY MEMORY

Each character position on the CRT screen corresponds to a pair of locations in the display refresh memory. The 8K byte display refresh memory can be fully memory mapped, or addressed through a 256 byte "window". In this way the QRGB-ALPHA can be memory-mapped without requiring a large overhead in system address space. The processor can read or write the display memory at full speed using all memory reference instructions ($T_a < 1052$ns). All accesses to the memory are "transparent". The processor can read or write the refresh memory at any time, and the display is free of "glitches".

When a character is to be displayed, its Character Code and Attribute Code are written into the appropriate display memory locations. The display is "scrolled" up or down by rewriting the contents of the Display Start Address Register.

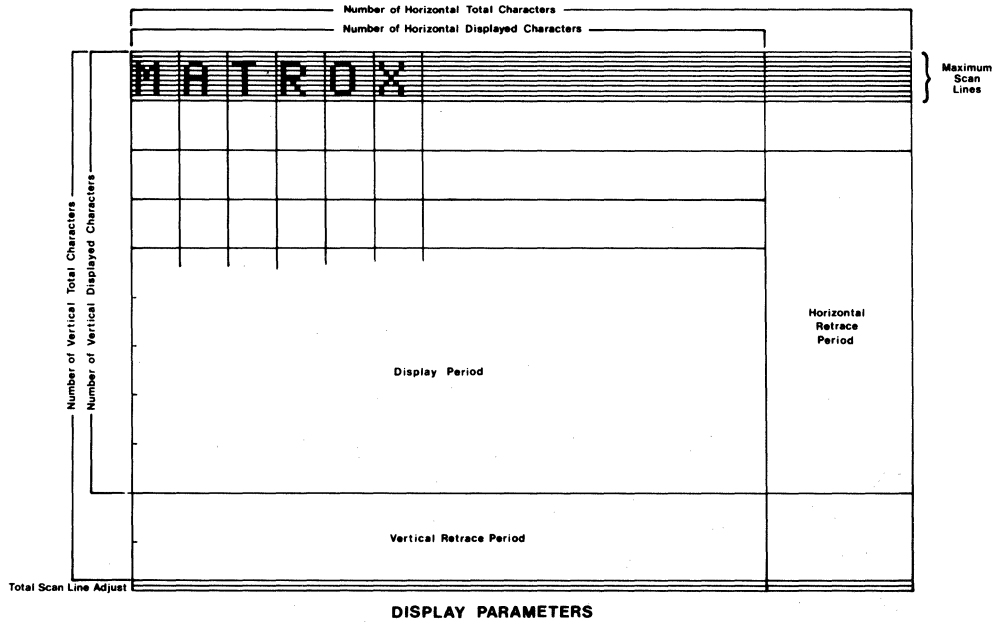



Figure 2. QRGB-ALPHA display parameters

As supplied, the Character and Attribute Memories are mapped into 256 bytes of system address space and are enabled/disabled through programmed I/O commands. The full display refresh memory, (8K bytes), is accessed by mapping the 256 byte system memory "window" into one of thirty-two, 256 byte, blocks. Block selection is determined by the Window Address Register. A Unified Memory Mode is also provided: when operating in the Unified Memory Mode all of the display refresh memory stores Characters Codes. Only 1 attribute is permitted. All of the 8000 characters can be viewed by "scrolling" the display up or down.

**CHARACTER GENERATOR**

Two 24-pin DIP sockets accept up to 4k bytes of ROM/EPROM/RAM thereby permitting up to 256 different characters and symbols to be defined. When using a RAM character generator, the character font may be rewritten at any time by the processor. Read/write access to the character generator is enabled/disabled through programmed I/O commands.

As supplied, the QRGB-ALPHA contains the Matrox MCH-01 character generator ROM (128 - 5 x 7 dot upper/lower case alphanumeric characters and graphic symbols). Other devices that may be used include TMS2516 (EPROM) and TMS4016 (RAM). Note that $t_a < 450$ns for displays having up to 80 characters/line and $t_a < 350$ns for displays having up to 132 characters/line.



**ATTRIBUTES**

Each character can be specified to be 1 of 8 foreground colors on 1 of 8 background colors. On an RGB monitor, the displayed colors are red, green, blue, cyan, magenta, yellow, black, and white. Characters may be either single or double height with character foreground and/or background normal or blinking at 2 Hz. Additionally, characters may be underlined or hidden (stored in display memory but not displayed).

**CURSOR**

An independently addressable cursor is provided. The Cursor Start and End Registers specify the scan lines in a character cell that are inverted to produce the cursor symbol. The position of the cursor on the screen is determined by the contents of the Cursor Register. The cursor blink rate is set to either 2 or 4 Hz.

**LIGHT PEN**

User-display interaction is possible through the use of a high-speed light pen. When the user points the pen at an illuminated spot on the CRT screen, the CRT loads the screen coordinates in to the Light Pen Register. The pen position may then be read by the processor. Note that the light pen can be used only with monitors having short persistence phosphors.

**KEYBOARD INTERFACE**

An 8-bit parallel keyboard interface is also provided. When a key is pressed, an interrupt flag is set in the Keyboard Status Register. The processor can read the keyboard data from the Keyboard Data Register.

**MATROX VIDEO BUS**

The QRGB-ALPHA may be "slaved" to the QRGB-GRAPH color graphic display controller card to provide a high-resolution graphics system with color alphanumeric overlay. All video and sync. signals required to "slave" the cards are bussed over the MATROX VIDEO BUS.

**BUS INTERFACE**

The QRGB-ALPHA plugs directly into the LSI-11 Q-bus and works with 16-bit processors using byte wide data transfers. The eight Command and Status Registers are positioned on any 8 byte I/O address boundary between 760 000$_8$ and 777 777$_8$. The Display Refresh Memory is positioned on any 256 byte memory address boundary between 000 000$_8$ and 777 777$_8$. Alternately, all 2K/4K/8K bytes of the display refresh memory can be mapped directly into system memory between 000 000$_8$ and 777 777$_8$.

**VIDEO GENERATOR**

All monochrome and RGB color video monitors work with the QRGB-ALPHA. Red, Green, Blue TTL level and analog video, H. Drive, V. Drive, and composite B/W video signals are provided.

**GRAPHICS**

The QRGB-ALPHA is ideal for producing character oriented graphics having a maximum resolution of 640H x 480V (interlaced) or 1024H x 240V (non-interlaced). An image is built up from graphic symbols written into the character generator RAM. Images are changed at high speed by rewritting the contents of the display memory and character generator.

**PROGRAMMING**

On power-up, all display control registers must be set, the display memory cleared and the character generator RAM, if used, loaded with the character font.

| ADDRESS | READ | | WRITE | |
|---|---|---|---|---|
| | UPPER BYTE | LOWER BYTE | UPPER BYTE | LOWER BYTE |
| BASE + O | — | CRTC Status | Window Address | CRTC Address |
| BASE + 2 | — | CRTC Data | Window Address | CRTC Data |
| BASE + 4 | — | Keyboard Data | Window Address | Control 1 |
| BASE + 6 | — | Keyboard Status | Window Address | Control 2 |

Table 1. Register definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Display memory access time varies from access to access depending on when the access occurs with respect to the display refresh cycle. The worst case access time depends on the number of horizontal dots per charcter cell (see table). The best case access time is 315ns, while the average access time approaches 450ns. as formats become less dense.

| HORIZONTAL DOTS/CELLS | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|
| Worst case time from BDINL or BDOUTL to BREPLYL | 870ns | 1050ns | 1130ns | 1220ns | 960ns | 1050ns |

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTION |
|---|---|
| Resolution | 4000 characters max. |
| Horizontal Characters | 132 characters max. |
| Vertical Lines | 48 lines max. (American Standard), 52 lines max. (European Standard) |
| Character Cell Size | 6, 7, 8, 9, 10 or 11 horizontal dots (special 16 dot cell can be strap-selected) |

2

### VIDEO TIMING

For a display format of 80 characters by 24 lines with 5 x 7 dot characters within a 7 x 10 dot character cell an 11.667 MHz crystal is used. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 48 $\mu$s | 48 $\mu$s |
| Horizontal Sync Frequency | 15.723 KHz | 15.576 KHz |
| Horizontal Sync Width | 4.80 $\mu$s | 5.40 $\mu$s |
| Vertical Sync Frequency | 60.01 Hz | 49.92 Hz |
| Vertical Sync Width | 190.8 $\mu$s | 256.8 $\mu$s |

### INPUT SIGNALS

Light Pen: Light-pen enable
Light-pen strobe

Keyboard: Keyboard data
Keyboard strobe

### OUTPUT SIGNALS

TTL Level Video: TTL level Red
TTL level Green
TTL level Blue
Vertical Drive
Horizontal Drive

Analog Video: Red
Green (composite)
Blue
Grey Scale (composite)

### BUS INTERFACE

Address, data and control signals conform to DEC LSI-11 Q-Bus specifications.
Command and Status Registers — Selectable on 8 byte I/O address boundaries 760 000 — 777 777 (766 400$_8$)
Display Refresh Memory — Selectable on 256 byte memory address boundaries 000 000 — 777 777 (766 000$_8$)
(Alternately selectable on any 8K memory address boundary)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| A: 36 pin edge connector, 0.125" centers, | LSI-11 Bus interface | DEC H8030 (2 required) |
| B: 36 pin edge connector, 0.125" centers, | | |
| C: 36 pin edge connector, 0.125" centers, | | |
| D: 36 pin edge connector, 0.125" centers, | | |
| J1: 10 pin right angle header, Analog video outputs | | AMP 87922-1 |
| J2: 10 pin right angle header, TTL video outputs | | AMP 87922-1 |
| J3: 50 pin right angle header, Matrox video bus | | Molex 15-25-4505 |
| J4: 26 pin right angle header, Keyboard and lightpen interface | | Molex 15-25-4264 |

## PHYSICAL

### SIZE

Width — 10.45 in. (26.54cm)
Height — 8.43 in. (21.41cm)
Depth — 0.50 in. ( 1.27cm)

### POWER REQUIREMENTS

+5V DC ±5% @2A

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

QRGB-ALPHA : Color alphanumeric display controller for stand alone operation
QRGB-ALPHA-SL : Color alphanumeric display controller for slave lock operation with QRGB-GRAPH

X-TAL : 10.000 MHz
X-TAL : 11.666 MHz
Optional crystals for special display format requirements

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# QBW-ALPHA

## PROGRAMMABLE B/W ALPHANUMERIC DISPLAY CONTROLLER FOR LSI-11 Q-BUS

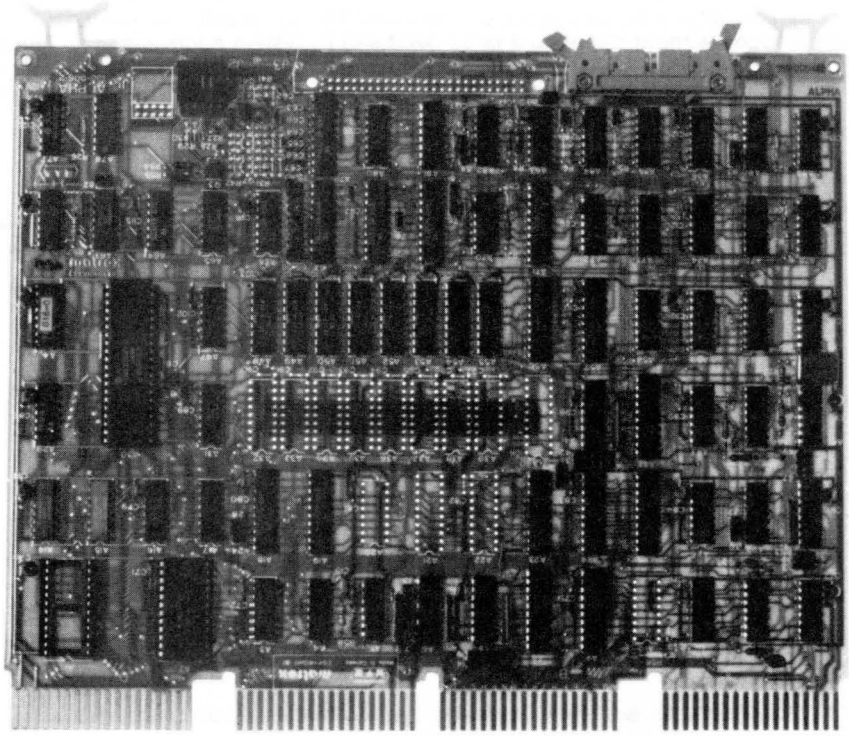


- **User Programmed Display Format**
- **Up to 4000 Characters on screen**
- **Blink**
- **Inverse Video**
- **Underline**
- **Double Height Characters**
- **Addressable cursor**
- **LSI-11 Q-bus* compatible**
- **Keyboard interface**
- **Light pen interface**
- **RAM and EPROM character generators**
- **Transparent memory**
- **50 or 60Hz operation**
- **Works with 16-bit and 18-bit addressing**

The QBW-ALPHA is a LSI-11 Q-bus* compatible, video display controller card which allows the display (characters/line x lines/page) and character formats (5 x 7, 7 x 9 etc.) to be set by programmed I/O commands. Available attributes include: blink, inverse video, double height characters, underline, and foreground disable.

The character font provided with the QBW-ALPHA contains 128 - 5 x 7 dot upper/lower case alphanumeric characters and graphics symbols. By adding a second character generator ROM/RAM, 128 additional symbols may be defined. When using a RAM character generator, the character font may be rewritten at any time by the system processor.

The QBW-ALPHA works with all monochrome video monitors in Europe (50 Hz) and America (60 Hz). Interface for a high-speed light pen and an 8-bit parallel keyboard are also provided.



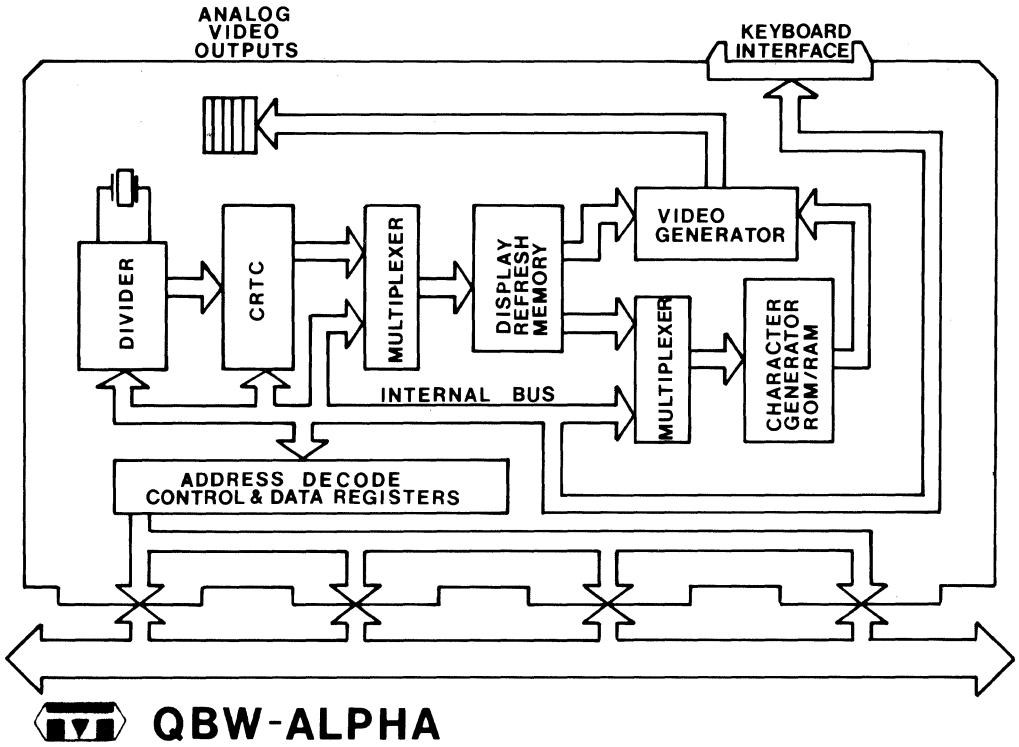



Figure 1. QBW-ALPHA block diagram

## FUNCTIONAL DESCRIPTION

The block diagram, Figure 1, shows the major functional components of the QBW-ALPHA.

## CRT CONTROLLER

In the design of the QBW-ALPHA, the 6845 CRT controller replaces many of the SSI/MSI components used in older designs and provides the QBW-ALPHA with features previously found only in the most expensive equipment. All display parameters are now user specified and displays can be configured to have virtually any combination of rows and columns up to a maximum of 4000 characters. In addition, the character cell size is variable and accomodates all commonly used character font sizes (5 x 7, 7 x 9, etc.).

## DISPLAY MEMORY

Each character position on the CRT screen corresponds to an 8-bit location in the display refresh memory. The 4K byte display refresh memory can be fully memory mapped, or addressed through a 256 byte "window". In this way the QBW-ALPHA can be memory mapped without requiring a large overhead in system address space. The processor can read or write the display memory at full speed using all memory reference instructions ($t_a < 1052ns$). All accesses to the memory are "transparent". The processor can read or write the refresh memory at any time, and the display is free of "glitches".

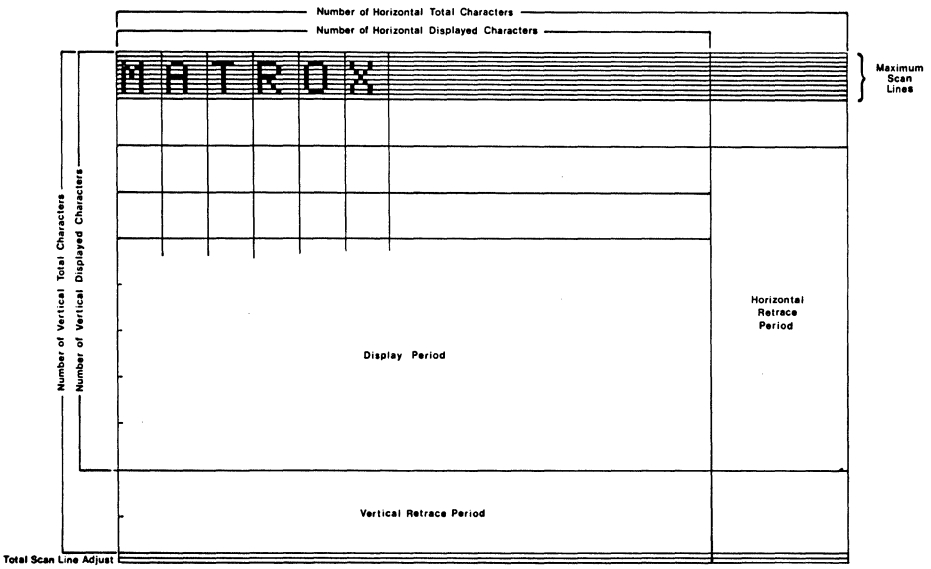



Figure 2. QBW-ALPHA display parameters

When a character is to be displayed, its Character Code is written into the appropriate display memory locations. The display is "scrolled" up or down by rewriting the contents of the Display Start Address Register.

As supplied the Character Memory is mapped into 256 bytes of system address space and is enabled/disabled through programmed I/O commands. The full display memory (4K bytes) is accessed by mapping the 256 byte system memory "window" into one of sixteen, 256 byte, blocks. Block selection is determined by the Window Address Register.

**CHARACTER GENERATOR**
Two 24-pin DIP sockets accept up to 4K bytes of ROM/EPROM/RAM thereby permitting up to 256 different characters and symbols to be defined. When using a RAM character generator, the character font may be rewritten at any time by the processor. Read/write access to the character generator is enabled/disabled through programmed I/O commands.

As supplied, the QBW-ALPHA contains the Matrox MCH-01 character generator ROM (128 - 5 x 7 dot upper/lower case alphanumeric characters and graphic symbols). Other devices that may be used include TMS2516 (EPROM) and TMS4016 (RAM). Note that $t_a < 450$ns for displays having up to 80 characters/line and $t_a < 350$ns for displays having up to 132 characters/line.



**ATTRIBUTES**
The QBW-ALPHA provides five strap-selectable character attributes: inverted video, underline, extended height, blink, and foreground disable. As supplied, each character may be assigned one of these attributes which is enabled by the surplus bit in the 8-bit Character Code.

The MCH-01 character set can be reduced, by hardware straps, to produce a 64 character set comprised of the upper case alphanumeric characters only. With this reduced set one extra bit is released from the Character Code enabling the implementation of a second character attribute per character. This extra bit may be alternatively used to control the selection between the two character generators, effectively combining the two character generators as one double size unit capable of holding video information for 256 different characters.

**CURSOR**
An independently addressable cursor is provided. The Cursor Start and End Registers specify the scan lines in a character cell that are inverted to produce the cursor symbol. The position of the cursor on the screen is determined by the contents of the Cursor Register. The cursor blink rate is set to either 2 or 4 Hz.

**LIGHT PEN**
User-display interaction is possible through the use of a high-speed light pen. When the user points the pen at an illuminated spot on the CRT screen, the CRT loads the screen coordinates in to the Light Pen Register. The pen position may then be read by the processor. Note that the light pen can be used only with monitors having short persistence phosphors.

**KEYBOARD INTERFACE**
An 8-bit parallel keyboard interface is also provided. When a key is pressed, an interrupt flag is set in the Keyboard Status Register. The processor can read the keyboard data from the Keyboard Data Register.

**BUS INTERFACE**
The QBW-ALPHA plugs directly into the Q-bus and works with 16-bit processors using byte or word data transfers. The seven Command and Status Registers are positioned on any 8 byte I/O address boundary between 760 000 and 777 777. The Display Refresh Memory is positioned on any 256 byte memory address boundary between 000 000 and 777 777.

**VIDEO GENERATOR**
All monochrome video monitors work with the QBW-ALPHA. Composite B/W video signals are provided.

**GRAPHICS**
QBW-ALPHA is ideal for producing character oriented graphics having a maximum resolution of 640H x 480V (interlaced) or 1024H x 240V (non-interlaced). An image is built up from graphic symbols written into the character generator RAM. Images are changed at high speed by rewritting the contents of the display memory and character generator.

**PROGRAMMING**
On power-up, all display control registers must be set, the display memory cleared and the character generator RAM, if used, loaded with the character font.

| ADDRESS | READ | | WRITE | |
|---|---|---|---|---|
| | UPPER BYTE | LOWER BYTE | UPPER BYTE | LOWER BYTE |
| BASE + 0 | — | CRTC Status | Window Address | CRTC Address |
| BASE + 2 | — | CRTC Data | Window Address | CRTC Data |
| BASE + 4 | — | Keyboard Data | Window Address | Control 1 |
| BASE + 6 | — | Keyboard Status | Window Address | Control 2 |

table 1. Register Definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Display memory access time varies depending on when the access occurs with respect to the display refresh cycle. The worst case access time depends on the number of horizontal dots per charcter cell (see table). The best case is 315 nsec., while the average access time approaches 450 nsec. as formats become less dense.

| HORIZONTAL DOTS/CELLS | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|
| Worst case time from MWTC/ or MRDC/ to XACK/ | 870ns | 1050ns | 1130ns | 1220ns | 960ns | 1050ns |

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTION |
|---|---|
| Resolution | 4000 characters max. |
| Horizontal Characters | 132 characters max. |
| Vertical Lines | 48 lines max. (American Standard), 52 lines max. (European Standard) |
| Character Cell Size | 6, 7, 8, 9, 10 or 11 horizontal dots (special 16 dot cell can be strap-selected) |

### VIDEO TIMING

For a display format of 80 characters by 24 lines with 5 x 7 dot characters within a 7 x 10 dot character cell an 11.667 MHz crystal is used. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 48$\mu$s | 48$\mu$s |
| Horizontal Sync Frequency | 15.723 KHz | 15.576 KHz |
| Horizontal Sync Width | 4.80$\mu$s | 5.40$\mu$s |
| Vertical Sync Frequency | 60.01 Hz | 49.92 Hz |
| Vertical Sync Width | 190.8 $\mu$s | 256.8$\mu$s |

### INPUT SIGNALS

Light Pen: Light-pen enable
Light-pen strobe
Keyboard: Keyboard date
Keyboard strobe

### OUTPUT SIGNAL

Composite Analog Video

### BUS INTERFACE

Address, data and control signals conform to DEC LSI-11 Q-bus specifications.
Command and Status Registers — Selectable on 8 byte memory address boundaries 760 000 — 777 777 (766 400$_8$)
Display Refresh Memory — Selectable on 256 byte memory address boundaries 000 000 — 777 777 (766 000$_8$)
(Alternately selectable on any 4K memory address boundary)

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| A: 36 pin edge connector, 0.125" centers } | |
| B: 36 pin edge connector, 0.125" centers } LSI-11 interface | DEC H8030 (2 required) |
| C: 36 pin edge connector, 0.125" centers } | |
| D: 36 pin edge connector, 0.125" centers } | |
| J1: 10 pin right angle header, composite video outputs | AMP 87922-1 |
| J4: 26 pin right angle header, Keyboard and lightpen interface | MOLEX 15-25-4264 |

### PHYSICAL

#### SIZE

Width — 10.45 in. (26.54cm)
Height — 8.43 in. (21.41cm)
Depth — 0.50 in. (1.27cm)

#### POWER REQUIREMENTS

+5V DC ±5% @2A

#### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0-95% non-condensing

### ORDERING INFORMATION

QBW-ALPHA : B/W alphanumeric display controller for stand alone operation
QBW-ALPHA-SL : B/W alphanumeric display controller for slave locked with QRGB-GRAPH

X-TAL : 10.0000 MHz } Optional crystals for special display format requirements
X-TAL : 11.6666 MHz }

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MLSI-2480

## 24 x 80 ALPHANUMERIC DISPLAY CONTROLLER FOR LSI-11 Q-BUS

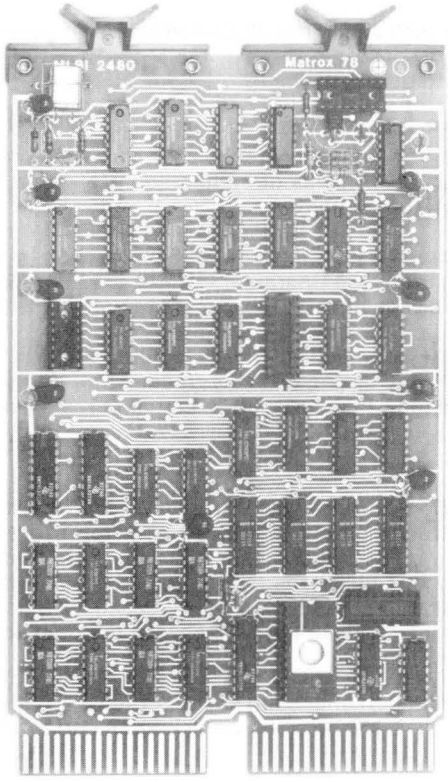


- **24 row x 80 column alphanumeric video display**
- **Normal, inverse, blink attributes**
- **4K byte memory mapped display**
- **LSI-11 Q-bus compatible**
- **Dual width board**
- **EPROM ASCII character generator**
- **Directly drives any monochrome monitor**
- **Single +5V supply**
- **External/internal sync capability**
- **American/European operation**
- **Decodes 16 address lines**

The MLSI-2480 is a LSI-11 Q-bus compatible alphanumeric display controller which is capable of generating displays of 24 lines of 80 characters per line. Characters can be displayed as either white on a black background or black on a white background. Each character can also be set to blink under software control.

The character font provided with the MLSI-2480 contains 128 - 5 x 7 upper/lower case alphanumeric characters and graphic symbols. The character generator is user-programmable, allowing the user to implement his own custom character font.

The MLSI-2480 works with all standard monochrome video monitors in Europe (50 Hz) and America (60 Hz).



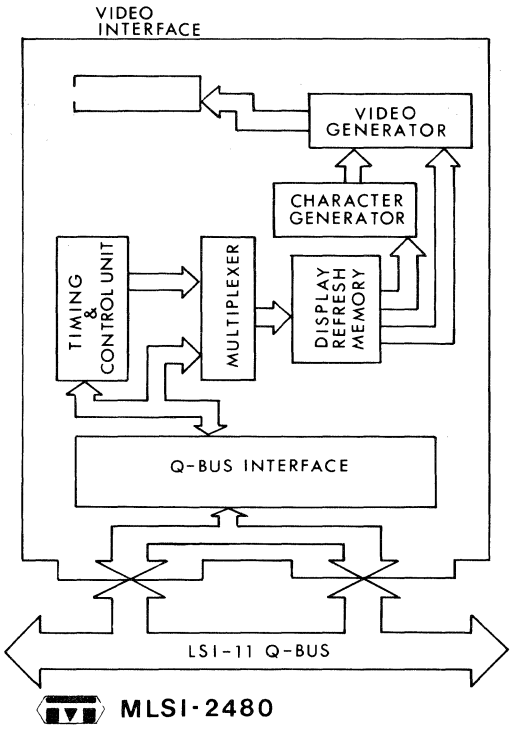



Figure 1. MLSI-2480 block diagram

**FUNCTIONAL DESCRIPTION**
The MLSI-2480 is made up of five major operational blocks: Timing and Control Unit, Display Memory, Character Generator, Video Generator, and Bus Interface. Communications between these blocks are shown in figure 1.

**TIMING AND CONTROL UNIT**
All timing and control signals required to generate a video display with 24 lines of 80 characters per line are supported on-board the MLSI-2480. The Timing and Control Unit, consisting of the master oscillator (11 MHz) and various modulo counters, produces the horizontal and vertical sync signals needed by the monitor as well as all timing signals for display refresh memory (RAS, CAS).

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the MLSI-2480 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The MLSI-2480 contains 2K bytes of on-board display refresh memory, to store up to 24 lines of 80 characters (1920 characters). The display memory occupies 4K bytes of system address space thereby permitting the CPU to identify each character location with a unique 12 bit address.

Each character position on the CRT screen corresponds to an 8 bit location in the display refresh memory. Characters are written on to the display by loading the ASCII Character Code to the appropriate display memory location. The CPU can read/write the display memory at full speed using all memory reference instructions.

All accesses to the display memory are controlled by a "Transparent Memory" control circuit within the Timing and Control Unit. In this way all accesses to the display memory (read, write, refresh) are efficiently arbitrated. The Transparent Memory control circuity permits the CPU to read or write the refresh memory at any time and the display is free of glitches.

**CHARACTER GENERATOR**
The MLSI-2480 contains an on-board 2716 EPROM which contains the binary video information to generate a 128 character set. The supplied character font consists of the full 96 upper/lower case alphanumeric character set with the addition of 32 special graphic characters. The alphanumeric characters are formed in a 5 x 7 dot matrix within a 6 x 10 dot character cell. The graphics characters utilize the entire character cell to allow for drawing continuous lines. For greater inter-character spacing the character cell size can be increased, with hardware straps, to 8 x 10 dots. Note that increasing the character cell size will cause gaps to appear between the graphics characters. Also, a different crystal is required for applications utilizing an 8 dot cell.

The MLSI-2480 permits simple implementation of custom character fonts. To install a new character set, the user need only reprogram the EPROM character generator with the video information to generate his own font.

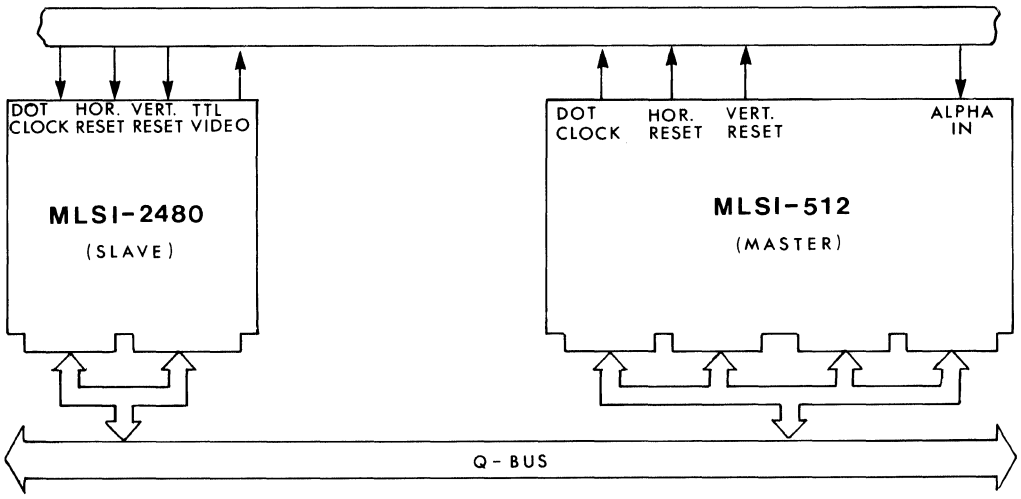



Figure 1. Combining MLSI-2480 with MLSI-512 for alpha/graph displays

**ATTRIBUTES**
Each character is accessed by seven bits of the eight bit ASCII Character Code. This releases the most significant eighth bit for attribute selection. Characters displayed on the MLSI-2480 can be displayed either as normal (white on a black background) or inverted (black on a white background). Character attributes are selected by on-board hardware straps and are enabled/disabled by the eighth bit of the character code.

**VIDEO GENERATOR**
The MLSI-2480 can directly drive any standard monochrome video monitor. Composite video signals as well as separate TTL level video, horizontal/vertical sync and blanking signals are supported on-board.

**BUS INTERFACE**
The MLSI-2480 plugs directly into the LSI-11 Q-bus. The display refresh memory, which is memory mapped into the LSI-11 Q-bus memory address space, can be strapped to reside at any 4K byte memory address boundary between 000 000$_8$ and 177 777$_8$.

**GRAPHICS**
The MLSI-2480 can be integrated, as an alphanumeric controller, within a complete alpha/graph video system. By configuring the MLSI-2480 to operate in the slave mode, the horizontal/vertical reset lines and the dot clock line are set to act as input ports. In this way the board can be synchronized to a master sync source. These lines can also be configurated to operate as output ports to enable the user to configure his system to synchronize to the MLSI-2480. A typical application of combined alphanumerics/graphics is shown in figure 2, where the graphics board (MLSI-512) acts as the master sync source.

**PROGRAMMING**
The MLSI-2480 operational status (American/European compatibility, Master/Slave operation, base address, etc) is programmed via on-board hardware straps. Table 1 outlines the definitions of these straps.

| JUMPER NO. | DESCRIPTION |
|---|---|
| S1 1-8 | Select base address |
| S3 1-10 | Select American/European TV standards |
| S4 1-2,6-9 | Select character cell size |
| S4 4-5 | Select character attribute |
| W1 | Enable "Master" mode |
| W2 | Enable 8 x 10 character cell |
| W3 | Enable 6 x 10 character cell |
| W4 | Disable transparent memory mode |
| W5 | Enable transparent memory mode |

Table 1. Jumper definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

With Transparent Memory Access: 800ns
Without Transparent Memory Access: 500ns

### DISPLAY PARAMETERS

| DESCRIPTION | DISPLAYED |
|---|---|
| Resolution | 1920 characters |
| Horizontal Characters | 80 characters |
| Vertical Lines | 24 lines |
| Character Cell Size | 6 or 8 horizontal dots |

2

### VIDEO TIMING

To generate a video display of 24 x 80 characters with a 6 dot cell, the MLSI-2480 uses an 11.06688 MHz crystal. The following table gives the video timing for both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 43.0 μs | 43.0 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 4.3 μs | 4.3 μs |
| Vertical Sync Frequency | 60.0 Hz | 50.2 Hz |
| Vertical Sync Width | 255.0 μs | 255.0 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Drive
Vertical Drive
Composite Sync
Composite Video

### BUS INTERFACE

Address, data and control signals conform to LSI Q-bus specifications.
Control Registers and Display Memory — Selectable on any 4K byte memory address boundary between 000 000$_8$ and 177 777$_8$ (160 000$_8$).

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| A : 36 pin edge connector<br>B : 36 pin edge connector | — Bus Interface | DEC H8030 |
| J1 : 16 pin DIP socket | — Video Interface | AUGAT 516-A6-37D |

### PHYSICAL

**SIZE**

Width: 5.25 in. (13.33 cm)
Height: 8.50 in. (21.59 cm)
Depth: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+5V DC ± 5% @ 0.9A

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

MLSI-2480 — XX—X
- X — Horizontal dots per character (6/8)
- XX — AS — American standard (60 Hz); ES — European standard (50 Hz)

Example: MLSI-2480-AS-6: 24 x 80 character display with 6 horizontal dots per character cell and a vertical refresh rate of 60 Hz

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MLSI-512

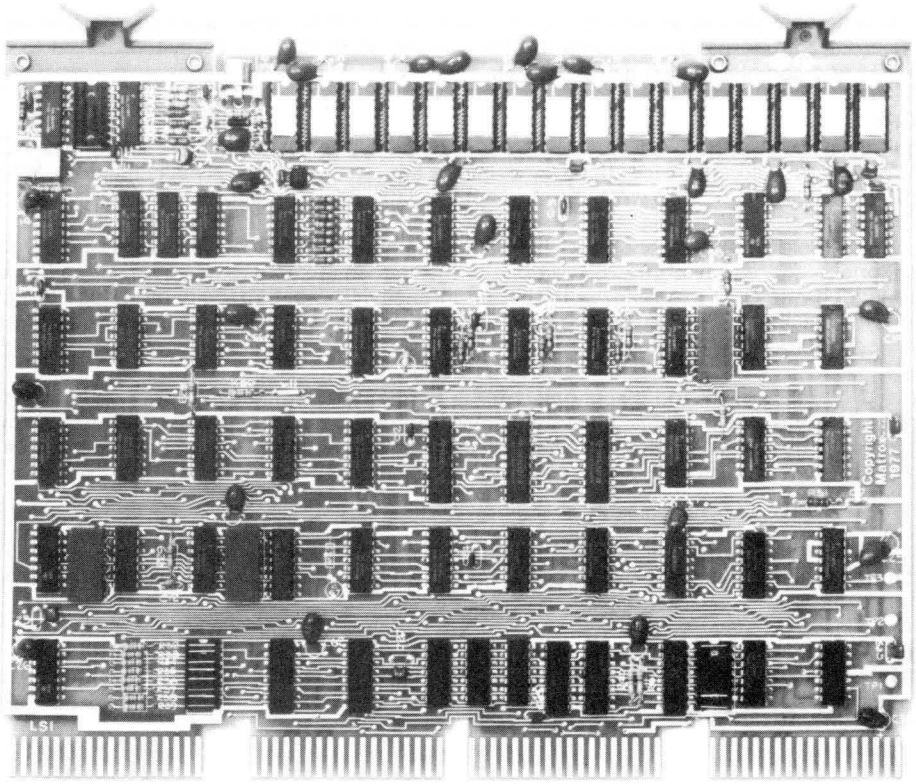
## 512 x 512 GRAPHICS DISPLAY CONTROLLER FOR LSI-11 Q-BUS



- **Bit mapped 512 x 512 pixel display**
- **256 x 256, 512 x 256, 1024 x 256 formats available**
- **Powerful X-Y virtual memory addressing**
- **Hardware scroll built-in**
- **Single instruction memory erase**
- **Color/grey-scale expansion**
- **Can be combined with MLSI-2480**
- **Transparent memory access**
- **LSI-11 Q-bus* compatible**
- **Internal/external sync**
- **American/European operation**

The MLSI-512 is a member of Matrox's complete line of LSI-11 Q-bus compatible graphics video boards. The MLSI-512 family of cards is designed to interface a mini or microcomputer to a CRT monitor and produce a B/W display of 512 x 512 points. The board also features built-in hardware scroll capabilities and a single instruction memory erase.

The MLSI-512 can also be combined with the MLSI-2480 to produce a complete alphanumerics/graphics video display system. Combining multiple MLSI-512 cards, the OEM system designer can construct a graphics display system with up to 24 bits/pixel (16 million different colors or grey levels).



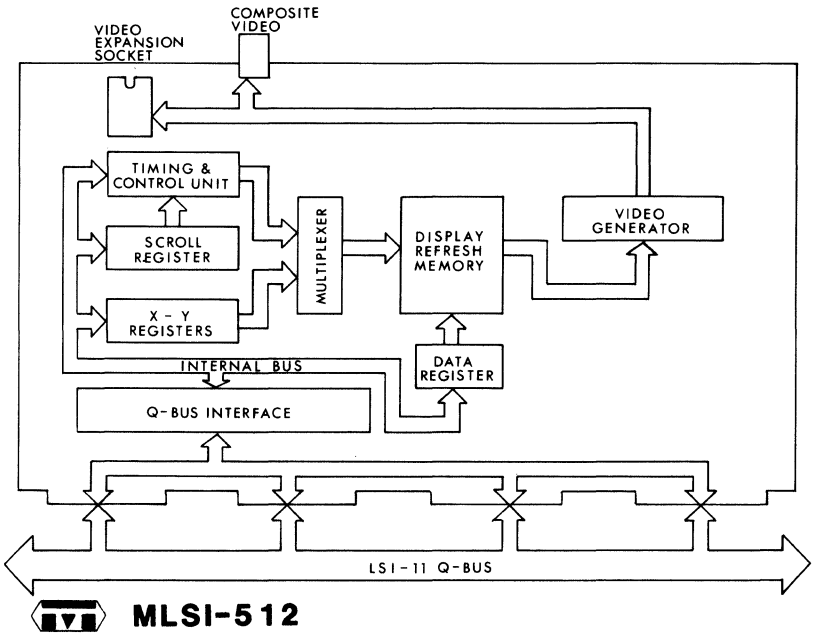



Figure 1. MLSI-512 block diagram

**FUNCTIONAL DESCRIPTION**
The MLSI-512 consists of six main functional blocks (figure 1): Timing and Control Unit, Scroll Register, X-Y Registers, Display Memory, Video Generator, and Bus Interface.

**TIMING AND CONTROL UNIT**
All timing and control signals required by the video monitor (horizontal/vertical sync and blanking), display refresh memory (row/column addressing), and video generator (dot clock, load and shift) are generated by the Timing and Control Unit. The exact configurations of these signals are user-programmable, via hardware straps, to enable the MLSI-512 to generate displays with up to 512 horizontal dots by 512 vertical dots. The board can also be strapped to operate in either 50 Hz (European) or 60 Hz (American) systems.

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the MLSI-512 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The MLSI-512 can be populated with 4, 8, or 16K RAMs for displays of 256 x 256, 512 x 256, 512 x 512, or 1024 x 256 dots. Each point on the CRT screen is identified by a unique address within the display memory. When a point is to be illuminated on the screen, a logic "1" is written to the appropriate display memory location.

The CPU reads/writes the display memory through a pair of memory-mapped I/O locations (X-Y Registers). This allows two memory locations to address all of the 262,144 bits of the refresh memory (512 x 512). Once the X and Y address of the dot has been loaded, the CPU can read/write the dot intensity. The dot intensity bit (image bit) can be assigned to any data bus bit. The resultant CRT display is a black and white image with the intensity of each dot being either on (logic "1") or off (logic "0").

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the MLSI-512 efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display is "transparent" to user.

**SCROLL**
An on-board Scroll Register enables the user to scroll the display up or down. By loading the Scroll Register the user can specify which horizontal line is to be displayed at the top of the screen. Lines scrolled off the top of the display will "wrap-around" and re-appear at the bottom of the screen.

**SCREEN ERASE**
The entire refresh memory on the MLSI-512 can be erased by a single OUTput instruction. Setting the memory erase enable bit when writing to the display memory will cause the entire memory to be set to that intensity (0 = black, 1 = white).

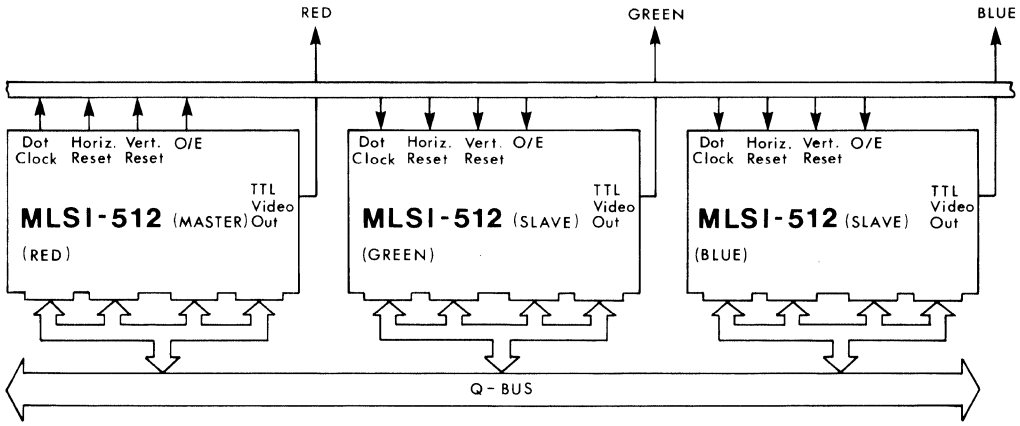



Figure 2. "Stacking" MLSI-512 cards for color/grey scale displays



**VIDEO GENERATOR**
The MLSI-512 works with all standard monochrome video monitors in American (60 Hz) and European (50 Hz) systems. TTL level video, horizontal sync, vertical sync, as well as composite video signals are supported on-board.

**BUS INTERFACE**
The MLSI-512 plugs directly into the LSI-11 Q-bus and works with both 8-bit and 16-bit processors. All the Command and Status Registers as well as the Display Memory are accessed via memory mapped I/O. The MLSI-512 can be positioned on any 8 byte memory address boundary between 160 000 and 177 7778.

**ALPHA/GRAPH DISPLAYS**
The MLSI-512 can be combined with the MLSI-2480 to generate alphanumeric/graphic displays. An on-board alphanumeric input port accepts the TTL level alphanumeric video information from the MLSI-2480 and combines it with the graphics video from the MLSI-512. The result is a powerful display combining both alphanumerics and graphics without the overhead involved in generating alphanumeric characters using graphic techniques.

**COLOR/GREY-SCALE EXPANSION**
Multiple MLSI-512 cards can be combined to provide for color/grey-scale displays. As previously outlined (DISPLAY MEMORY), the image bit on a given card can be assigned to any data bus bit. Thus the output of each card can be assigned a different weight or color. By assigning cards to different data bus bits and strapping all the cards with the same address, the intensity or color of a given dot can be loaded in a single instruction. A typical example of building up a color video system using the MLSI-512 is shown in figure 2.

**PROGRAMMING**
The MLSI-512 is programmed, for various display resolutions, by on-board hardware straps. These straps are organized into three 16 pin "programming sockets" to facilitate simple re-programming of the board. Table 1 defines the on-board jumpers used to configure the MLSI-512 for the various resolution options.

| SOCKET | JUMPER | DESCRIPTION |
|---|---|---|
| P | 1 | Vertical display = 240 lines (American standard) or 256 lines (European standard) |
| | 2 | Vertical reset = 262½ lines (American standard) |
| | 3 | Vertical reset = 312½ lines (European standard) |
| | 4 | Vertical sync = 244 lines (American standard) |
| | 5 | Vertical sync = 276 lines (European standard) |
| | 6 | Not used |
| | 7 | Enable 512 dot vertical resolution |
| | 8 | Not used |
| R | 1 | Enable 1024 dot horizontal resolution |
| | 2 | Set memory access mode for RAM type used |
| | 3 | Enable 1024 dot horizontal resolution |
| | 4 | Disable 1024 dot horizontal resolution |
| | 5 | Synchronize blanking for 512/1024 dot horizontal resolution |
| | 6 | Synchronize blanking for 256 dot horizontal resolution |
| | 7 | Dot clock = 5.53344 MHz (256 dot horizontal resolution) |
| | 8 | Dot clock = 11.06688 MHz (512/1024 dot horizontal resolution) |
| J | 1 | Enable 256 x 256 addressing |
| | 2 | Enable 512 x 256 addressing |
| | 3 | Enable interlaced addressing (512 x 512/1024 x 256) |
| | 4 | Enable 512 dot horizontal addressing |
| | 5 | Enable 1024 dot horizontal addressing |
| | 6 | Enable 512 dot vertical addressing |
| | 7 | Synchronize LOAD SCROLL signal to 60 Hz (American standard) |
| | 8 | Synchronize LOAD SCROLL signal to 50 Hz (European standard) |

Table 1. Jumper Configurations

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μs

### DISPLAY PARAMETERS

| RESOLUTION | RAM TYPE |
|---|---|
| 256 X 256 | 4K |
| 512 X 256 | 8K |
| 512 X 512 | 16K |
| 1024 X 256 | 16K |

### VIDEO TIMING

For a 256 x 256 or 512 x 256 display, the video output is non-interlaced. For a 512 x 512 or 1024 x 256 display, the video output is interlaced (two fields per frame). In order to avoid display flicker, a monitor with long persistence phosphors must be used.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46 μs | 46 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 5.67 μs | 5.67 μs |
| Vertical Sync Frequency | 60 Hz | 50.2 Hz |
| Vertical Sync Width | 190 μs | 190 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Sync
Vertical Sync
Composite Sync
Composite Video

### BUS INTERFACE

Address, data, and control signals conform to LSI-11 Q-bus Specifications
Display Memory, Command and Status Registers — Selectable on any 8 byte memory address boundary between 160 000$_8$ and 177 777$_8$ (160 000$_8$)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| A : 36 pin edge connector, 0.125" centers | Bus Interface | DEC H8030 (2 required) |
| B : 36 pin edge connector, 0.125" centers | | |
| C : 36 pin edge connector, 0.125" centers | | |
| D : 36 pin edge connector, 0.125" centers | | |
| J1 : phono connector | — Composite Video | RCA 901 |
| V : 16 pin DIP socket | — Video Expension Socket | AUGAT 516-A6-37D |

## PHYSICAL

### SIZE

Width: 10.50 in. (26.67 cm)
Height: 7.75 in. (19.69 cm)
Depth: 0.50 in. ( 1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5% @ 800mA
+12V DC ±5% @ 200mA

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

MLSI — XXX/XXX — XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- XXX: Vertical resolution (256/512)
- XXX: Horizontal resolution (256/512/1024)

Example: MLSI-512/512-AS: 512 x 512 pixel display with a vertical refresh rate of 60 Hz.

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# QRGB-256

## 256 x 256 COLOR GRAPHICS DISPLAY CONTROLLER FOR LSI-11 Q-BUS

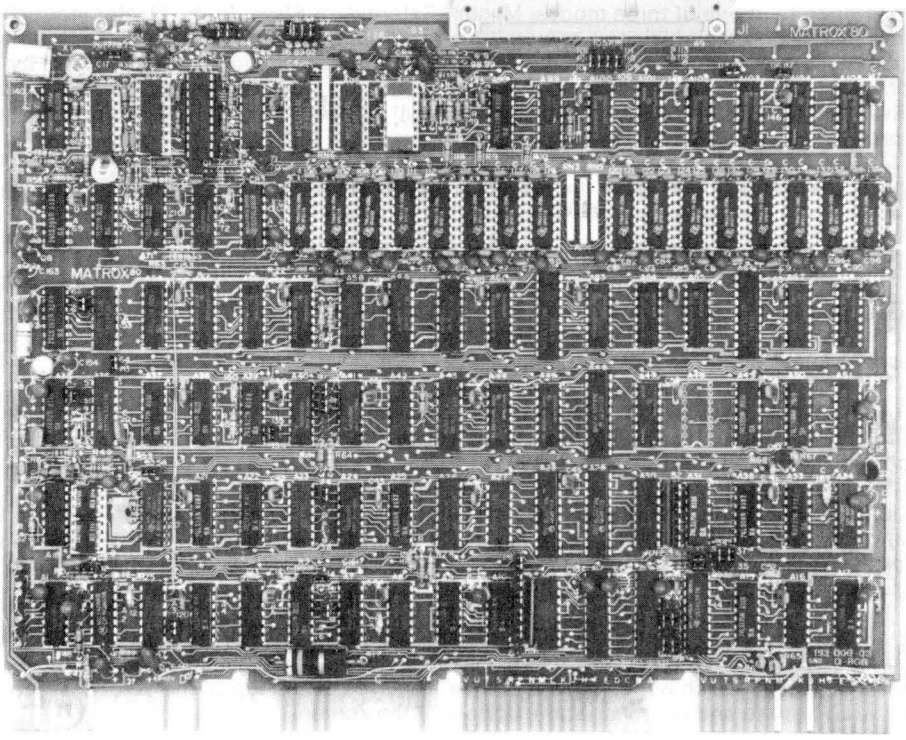


- **256 x 256 resolution**
- **4 bits/pixel expandable to 8 bits/pixel**
- **Built-in 8-bit D/A converter (grey scale)**
- **Built-in 8-bit composite color encoder**
- **Single instruction erase**
- **LSI-11 Q-bus* compatible**
- **Hardware scroll**
- **Internal/external sync**
- **American/European operation**
- **Built-in phase lock loop (for genlock)**

The QRGB-256 is a powerful color graphics display controller built on a single LSI-11 Q-bus* compatible card. Graphics images of up to 256 x 256 dots can be displayed in up to 16 colors or grey levels. The QRGB-256 also includes such advanced features as hardware scroll, single instruction erase and digitize commands.

The QRGB-256 can be combined with other Matrox video boards such as the MLSI-2480 (alphanumerics) and the QFG-01 (frame grabber). The OEM system designer can therefore integrate the QRGB-256 into a powerful tailor-made video display system.

The QRGB-256 works with all standard video monitors in Europe (50 Hz) and America (60 Hz). An on-board phase lock loop can be synchronized to an external sync source to enable the QRGB-256 to be used in broadcast applications.



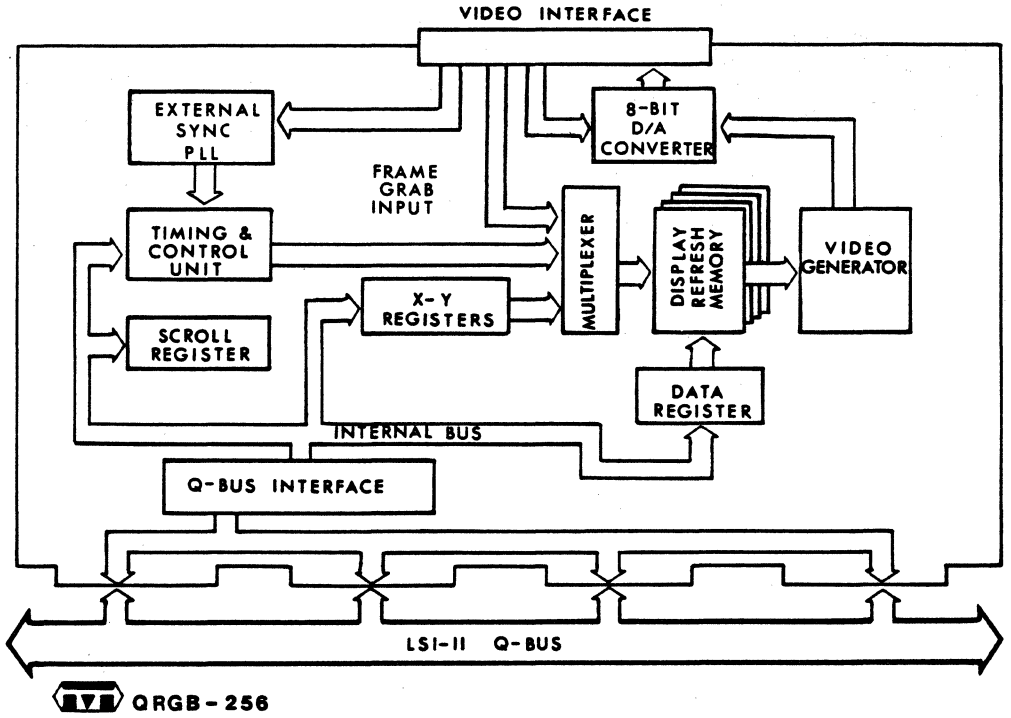



Figure 1. QRGB-256 block diagram

**FUNCTIONAL DESCRIPTION**

The QRGB-256 is a single board color graphics controller. It consists of five main operational blocks: Timing and Control Unit, X-Y Registers, Display Memory, Video Generator, and Q-bus Interface. A block diagram of the QRGB-256 is shown in figure 1.

**TIMING AND CONTROL UNIT**

The Timing and Control Unit consists of three major subsystems; Phase Lock Loop, Sync Generator, and Internal Reference. Through these three subsystems the QRGB-256 is capable of generating all the necessary timing signals to produce a composite color or grey-scale video display. These timing signals include: horizontal/vertical sync and blanking, display refresh RAM addressing, as well as a color subcarrier.

The QRGB-256 can operate in one of three modes: Master, External, or Slave. In the Master mode, the QRGB-256 generates all the necessary video timing signals required for the display. Using the Master mode the QRGB-256 can be used as a stand-alone controller or as a system master, where the video timing signals produced by the QRGB-256 are used to synchronize one or more other boards into a complete video imaging system. The Slave mode is used to synchronize the QRGB-256 to another QRGB-256 system master. Slaved QRGB-256 boards can be used to expand the number of bits/pixel.

Using the QRGB-256 in external mode locks the on-board phase-locked loop to an external sync source. NTSC or PAL compatible signals are provided by the board when locked to broadcast standard inputs.

**DISPLAY MEMORY**

The QRGB-256 contains 32K bytes of on-board dynamic RAM which contains the binary picture information. The display memory is arranged as 256 x 256 x 4 bits, with each of the unique 65,536 memory locations representing a specific location on the CRT screen. To display a point on the screen the appropriate memory location is loaded with four data bits which represent the pixel (picture element) color.

The QRGB-256 uses a simple yet powerful X-Y addressing scheme. Two directly addressable registers store the X and Y coordinates of any given dot in the display memory. After the dot's X-Y coordinates have been defined, the CPU can read/write the pixel information to the Data Register.

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66 ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the QRGB-256 efficiently resolves any contention problems between CPU read/write requests and CRT refresh requests in such a way that the display is "transparent" to the user.

**SCROLL**

An on-board scroll register permits the user to vertically shift the displayed image up or down. By loading the Scroll Register, the user can specify which horizontal line will be displayed at the top of the screen. Lines scrolled off the top of the display will wrap-around and reappear at the bottom of the screen.

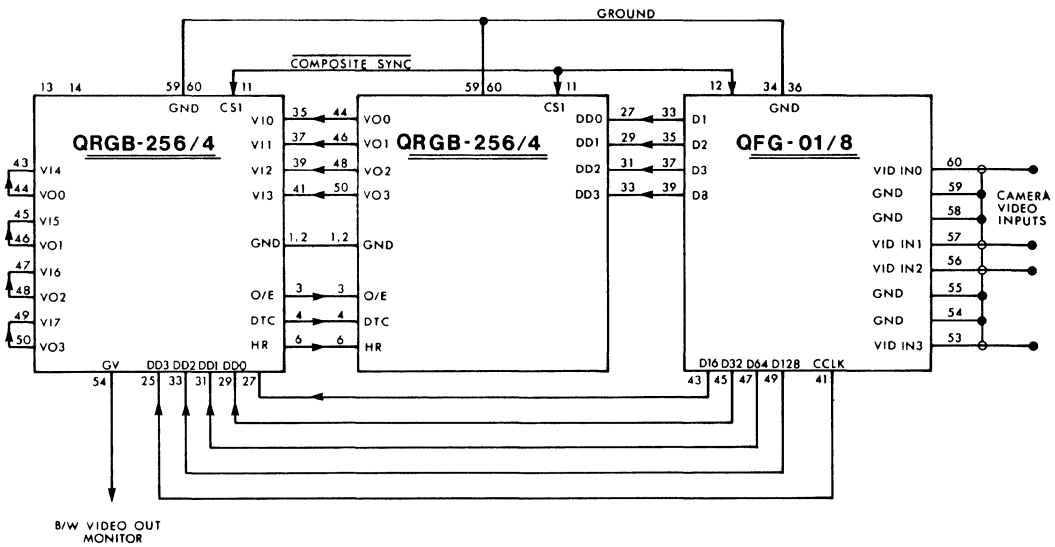



Figure 2. Combining QRGB-256 and QFG-01 — 256 x 256 x 8 bit imaging system

## ERASE/DIGITIZE COMMAND

The QRGB-256 has an erase/digitize command built into hardware. This command enables the user to preset the entire display refresh memory to a given value or to load one field of a digitized video signal obtained from an external frame grabber card. In the erase mode, the user can set the entire display memory to a specified value with a single INput instruction.

## VIDEO GENERATOR

The QRGB-256 includes a built-in color encoder which can provide up to 16 colors or grey levels. Most monochrome and composite color monitors will work with the QRGB-256. Red, Green, Blue, and Mid-Green TTL level video, horizontal drive, vertical drive, as well as composite color and grey-scale video signals are provided.

## BUS INTERFACE

The QRGB-256 plugs directly into the LSI-11 Q-Bus and works with both 8 and 16 bit processors. The QRGB-256 can be located on any 8 byte system I/O address boundary between 160 000 and 177 777.

## SYSTEM CONFIGURATIONS

The QRGB-256 can be used as a stand alone controller or, by "stacking" cards, can be integrated into a complete video imaging system. As a stand alone controller the QRGB-256 provides a 256 x 256 dot raster in 16 different colors or grey levels. Additionally the QRGB-256 can be combined with other boards to provide more colors (multiple QRGB-256 boards), digitized TV pictures (QRGB-256 + QFG-01) or a complete alphanumerics/graphics display system (QRGB-256 + MLSI-2480). The QRGB-256 can also be synchronized to an external sync source via the on-board phase lock loop. This feature enables the board to generate NTSC/PAL compatible video signals for integration into a broadcasting environment.

## PROGRAMMING

The QRGB-256 is programmed via five I/O registers in combination with a series of on-board hardware straps. Address bits A0 to A2 are used to select between registers (Data Register, Control Register, Scroll Register, X Register, and Y Register) which are located for either byte-wide or word-wide accesses (Table 1). A Flag Register is also included on-board (accessed by reading the Control Register) to enable the host processor to monitor the board's status (Busy, Vertical Blank). The Control Register is used to initialize the erase/digitize command on the QRGB-256 as well as provide a means of video control (video output enable/disable).

Much of the board's operational parameters are defined through on-board hardware straps. With these jumpers, the user can program the on-board Sync Generator for American (60 Hz) or European (50 Hz) operation, in either Master, External, or Slave sync mode. Straps are also provided to set the QRGB-256 video outputs for NTSC (American) or PAL (European) standard compatibility. The board's base address is determined by the on-board straps.

| RELATIVE LOCATION | 8-BIT SYSTEM | | 16-BIT SYSTEM | |
|---|---|---|---|---|
| | READ | WRITE | READ | WRITE |
| 0 | Data Register | Data Register | Flag/Data Registers | Control/Data Registers |
| 1 | Flag Register | Control Register | not used | — |
| 2 | not used | X Register | not used | X/Y Registers |
| 3 | not used | Y Register | not used | — |
| 4 | not used | Scroll Register | not used | Scroll Register |
| 5 | not used | not used | not used | — |
| 6 | not used | not used | not used | not used |
| 7 | not used | not used | not used | — |

Table 1. Register definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μsec. max.

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTIONS |
|---|---|
| Horizontal Resolution | 256 dots |
| Vertical Resolution | 256 dots (European standard), 240 dots (American standard) |

### VIDEO TIMING

The QRGB-256 generates a 256 x 256 dot raster graphics display. The following table gives the video timing for both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46 μs | 46.5 μs |
| Horizontal Sync Frequency | 15.735 KHz | 15.638 KHz |
| Horizontal Sync Width | 5.8 μs | 5.8 μs |
| Vertical Sync Frequency | 60 Hz | 50 Hz |
| Vertical Sync Width | 190 μs | 191 μs |

### OUTPUT SIGNALS

TTL Level Video: Red
Green
Blue
Vertical Drive
Horizontal Drive

Composite Video: Composite Color
Composite Grey-Scale

### BUS INTERFACE

Address, data, and control signals conform to DEC LSI-11 Q-bus specifications
Command Status and Data Registers — Selectable on any 8 byte memory-mapped I/O address boundary between 160 000$_8$ and 177 777$_8$ (170 000$_8$)

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| A : 36 pin edge connector<br>B : 36 pin edge connector<br>C : 36 pin edge connector<br>D : 36 pin edge connector — Bus Interface | DEC H8030 (2 required) |
| J1 : 50 pin right angle header — Video Interface | MOLEX 15-25-8601 |

### PHYSICAL

**SIZE**

Width: 10.48 in. (26.56 cm)
Height: 8.50 in. (21.59 cm)
Depth: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+5V DC ±5% @ 1A
+12V DC ±5% @ 400mA
−12V DC ±5% @ 250mA

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

QRGB-256/X — XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- X: Number of bit planes (3/4)

Example: QRGB-256/3-AS: 256 x 256 graphics display with 3 bits per pixel (8 possible colors or grey levels) and a vertical refresh rate of 60 Hz.

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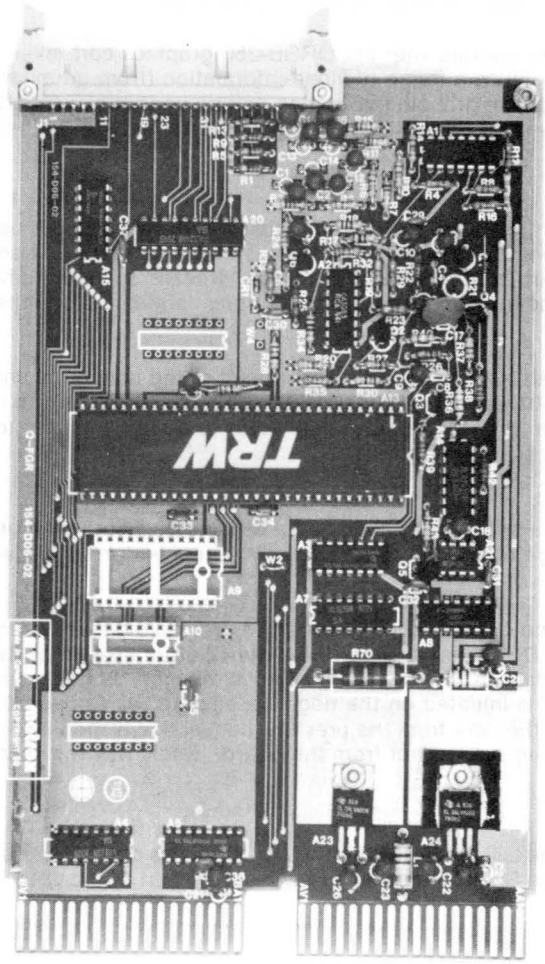
# QFG-01

## HIGH SPEED VIDEO A/D CONVERTER FOR LSI-11 Q-BUS



- **4,6, or 8 bit A/D converter**
- **4 video inputs**
- **Accomodates most video amplitudes**
- **Interfaces directly to QRGB-256 to store TV picture**
- **Continuous or "Freeze" grab operation**
- **LSI-11 Q-Bus* compatible**
- **On-board sync separator circuit**
- **American/European operation**

The QFG-01 is a high speed analog to digital converter card that is intended to be used with the Matrox QRGB-256 graphics display controller cards. The QFG-01 permits the user to digitize a standard monochrome video signal (1V p-p) and, on command, to write one digitized field of video information into the QRGB-256 display refresh memory.



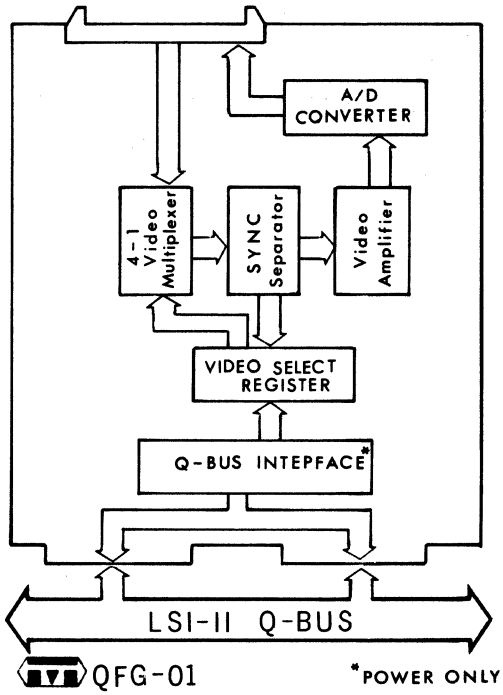



Figure 1. QFG-01 block diagram

**FUNCTIONAL DESCRIPTION**
The QFG-01 frame grabber card can be functionally divided into four operational blocks. These blocks (figure 1) are: Input Multiplexer, Sync Generator, Video Amplifier, and A/D Converter.

The QFG-01 has been designed to operate with the QRGB-256 graphics controller. Through commands generated by the QRGB-256, the QFG-01 will digitize a frame of video information (from an external TV camera) and store it in the QRGB-256 display memory. This frame grabbing operation can be continuous (the QRGB-256 will display a continually updated or "live" picture) or one-shot, effectively "freezing" the action. Figure 2 illustrates the connections between the QRGB-256 and the QFG-01.

**INPUT MULTIPLEXER**
The QFG-01 contains an on-board 4 to 1 input video multiplexer. In this way the user can interface up to four analog video inputs (composite video from four different TV cameras) to the 30 MHz A/D converter. Switching, between these four video inputs, is under software control. The QFG-01 can "freeze" a single frame from any one of the video inputs or, by continually accessing the board, can provide a continuous "grabbing" of consecutive fields.

**SYNC SEPARATOR**
Composite video signals, accepted by the QFG-01, are stripped of the horizontal and vertical sync signals. These sync signals are then used by the QFG-01 as control signals to synchronize the QFG-01 to the TV camera. The composite sync signals are also made available on the video output connector to enable the user to synchronize the QRGB-256 color graphics board to the TV camera as well.

**VIDEO AMPLIFIER**
The selected input video goes to a backporch clamp and a variable gain stage. An on-board gain control potentiometer allows the user to take advantage of the full range of the A/D converter for a given input signal amplitude.

**VIDEO A/D CONVERTER**
The QFG-01 can be ordered in one of three configurations to provide digitized video picture information with 4, 6, or 8 bits per pixel. The on-board A/D converter provides a continuous stream of digital data to the QRGB-256. The initiation of the storage of this data in the QRGB-256 display memory is done, under software control, through the QRGB-256 card. A/D conversion is initiated on the negative edge of the Convert Command generated by the QRGB-256. On this same negative edge the data from the previous conversion is made valid. The digital outputs from the A/D converter are buffered before being passed out from the board. In this way the validity of the produced video information is assured.

**BUS INTERFACE**
The QFG-01 plugs directly into the LSI-11 Q-Bus. To the LSI-11 Q-Bus computer the QFG-01 looks like a single register (Video Select Register). The Video Select Register is addressed as part of the QRGB-256 Control Register.

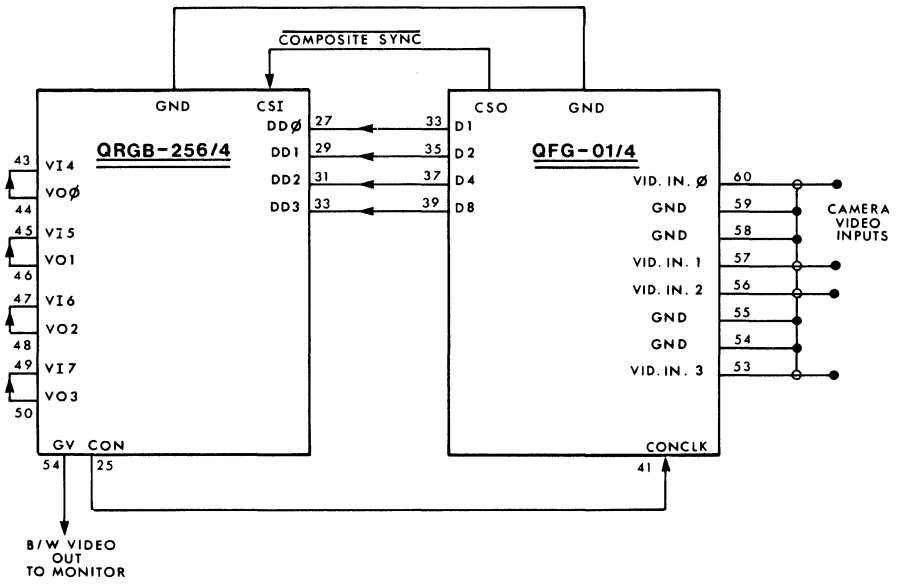



Figure 2. 256 x 256 x 4 bit imaging system

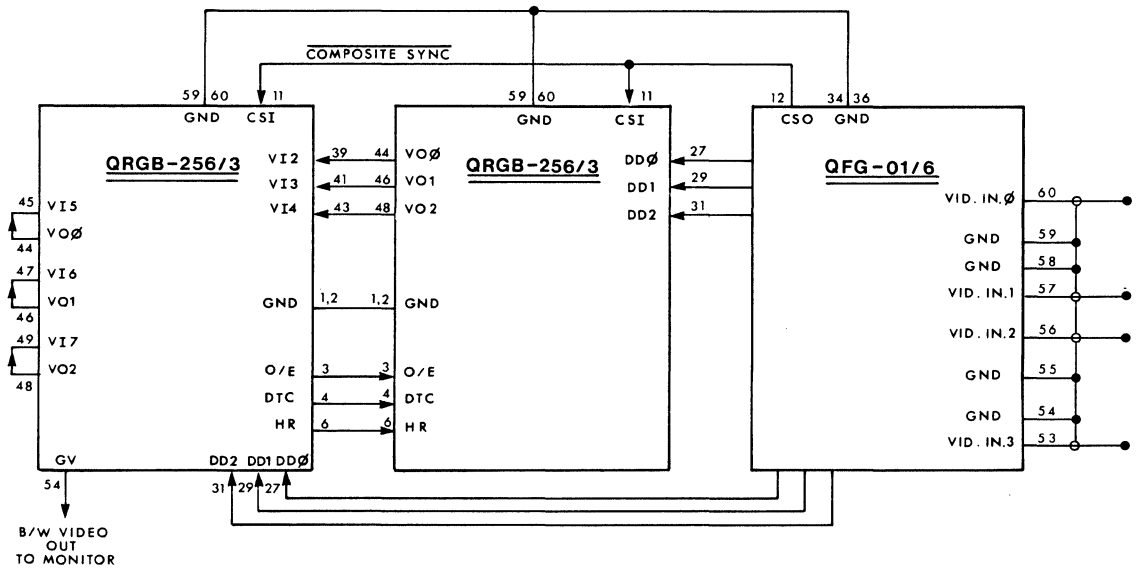



Figure 3. 256 x 256 x 6 bit imaging system

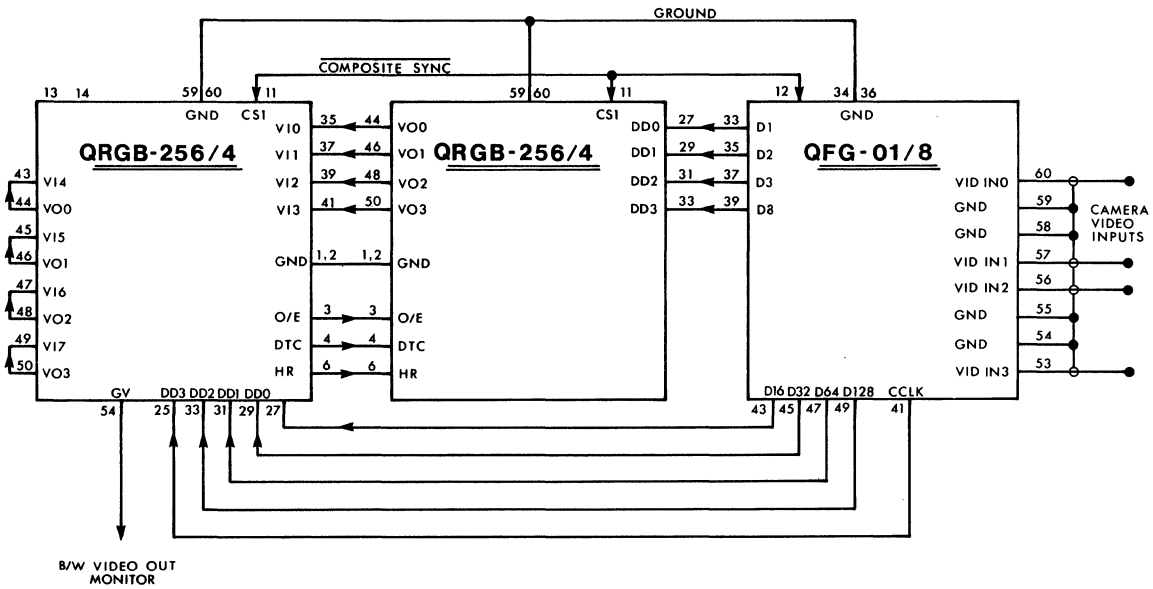



Figure 4. 256 x 256 x 8 bit imaging system.

# SPECIFICATIONS

## FUNCTIONAL

### INPUT SIGNALS

Analog Video 0*
Analog Video 1
Analog Video 2
Analog Video 3
Convert Clock (TTL, 20 MHz max.)

*All analog video inputs are composite video (75Ω, 0.6V to 1.5$V_{p-p}$)

### OUTPUT SIGNALS

TTL Level Video (4, 6 or 8 bits)
TTL Level Composite Sync (negative going)

## BUS INTERFACE

Address, data and control signals conform to DEC LSI-11 Q-Bus specifications
Video Select Register — Accessed via QRGB-256 Control Register

## CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| A : 36 pin edge connector<br>B : 36 pin edge connector | Bus Interface | DEC H8030 |
| P2 : 50 pin dual right angle header | — Analog Video In<br>— Digital Video Out | MOLEX 15-25-8601 |

## PHYSICAL

### SIZE

Width: 5.23 in. (13.28 cm)
Height: 8.50 in. (21.59 cm)
Depth: 0.50 in. ( 1.27 cm)

### POWER REQUIREMENTS

+ 5V DC ± 5% @ 300 mA
+12V DC ± 5% @ 100 mA
−12V DC ± 5% @ 200 mA (4 bits)
−12V DC ± 5% @ 300 mA (6 bits)
−12V DC ± 5% @ 500 mA (8 bits)

### ENVIRONMENTAL REQUIREMENTS

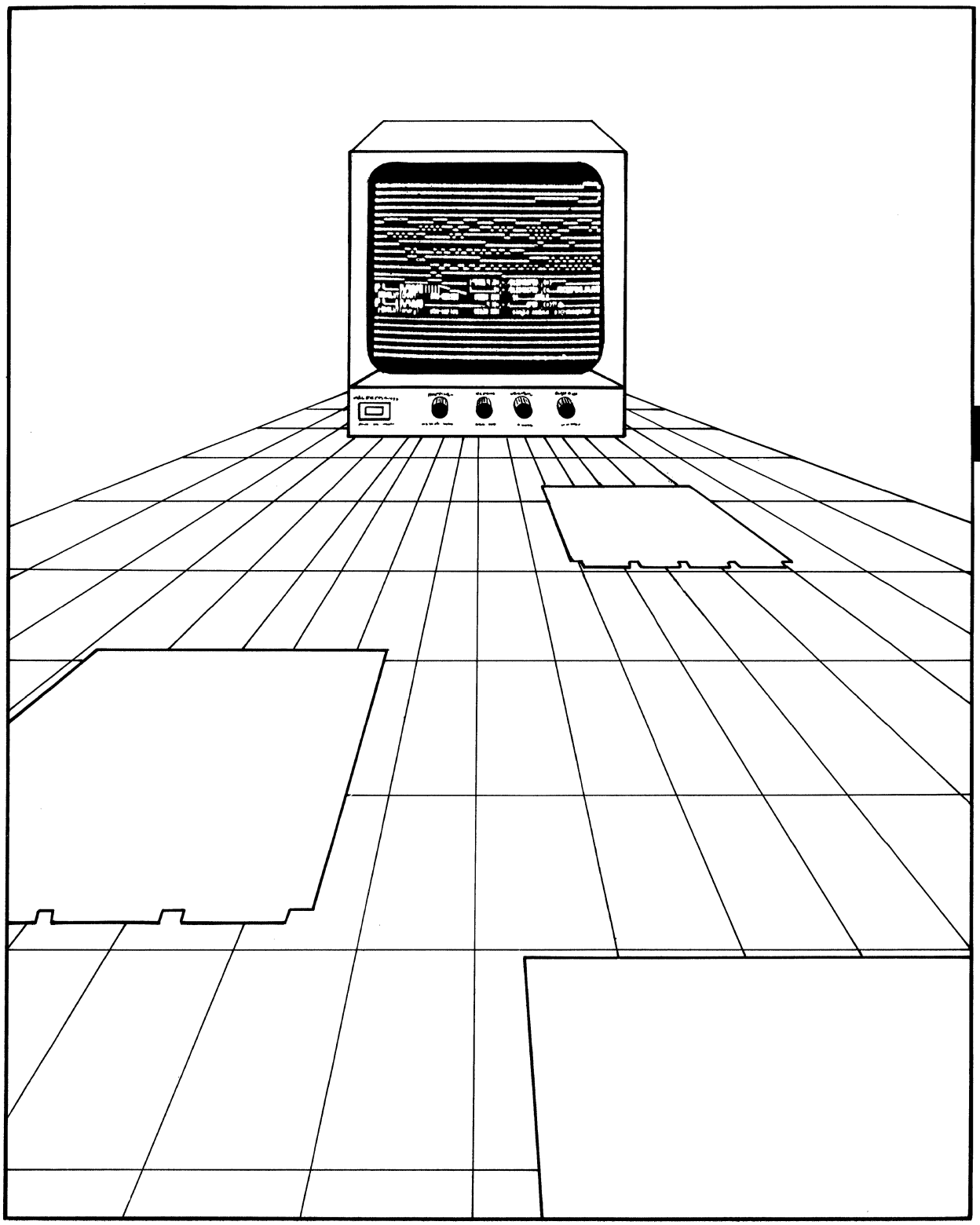
Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

## ORDERING INFORMATION

QFG-01 / X

X — Number of bits per pixel (4/6/8)

Example: QFG-01/8: Frame grabber with an eight bit A/D converter.



3

# UNI-BUS (PDP-11) VIDEO BOARDS

## SECTION 3 UNI-BUS (PDP-11) VIDEO BOARDS



**NOTE:** All Matrox Q-bus video boards can also be used with PDP-11 computers through the use of an interface card called a QNIVERTER. See Application Note #7 for details.

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MDC-2480

## 24 x 80 ALPHANUMERIC DISPLAY CONTROLLER FOR PDP-11 UNI-BUS

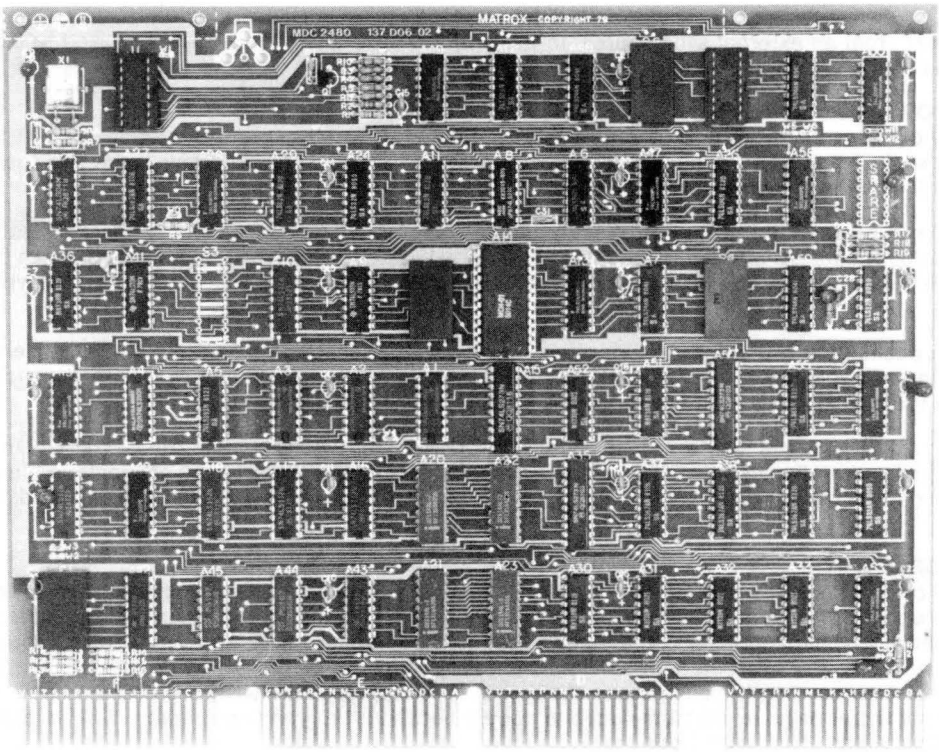


- **24 row x 80 column alphanumeric video display**
- **4K byte memory mapped display**
- **Normal, inverse, blink attributes**
- **EPROM ASCII character generator**
- **Transparent memory access**
- **PDP-11 UNI-bus compatible**
- **Directly drives any monochrome monitor**
- **Single +5V supply**
- **External/internal sync capability**
- **American/European operation**
- **Built-in keyboard interface**
- **Hardware scroll**

The MDC-2480 is a PDP-11 UNI-bus compatible alphanumeric display controller which is capable of generating displays of 24 lines of 80 characters per line. Characters can be displayed as either white on a black background or black on a white background. Each character can also be set to blink under software control.

The character font provided with the MDC-2480 contains 128 - 5 x 7 upper/lower case alphanumeric characters and graphic symbols. The character generator is user-programmable, allowing the user to implement his own custom character font.

The MDC-2480 works with all standard monochrome video monitors in Europe (50 Hz) and America (60 Hz).



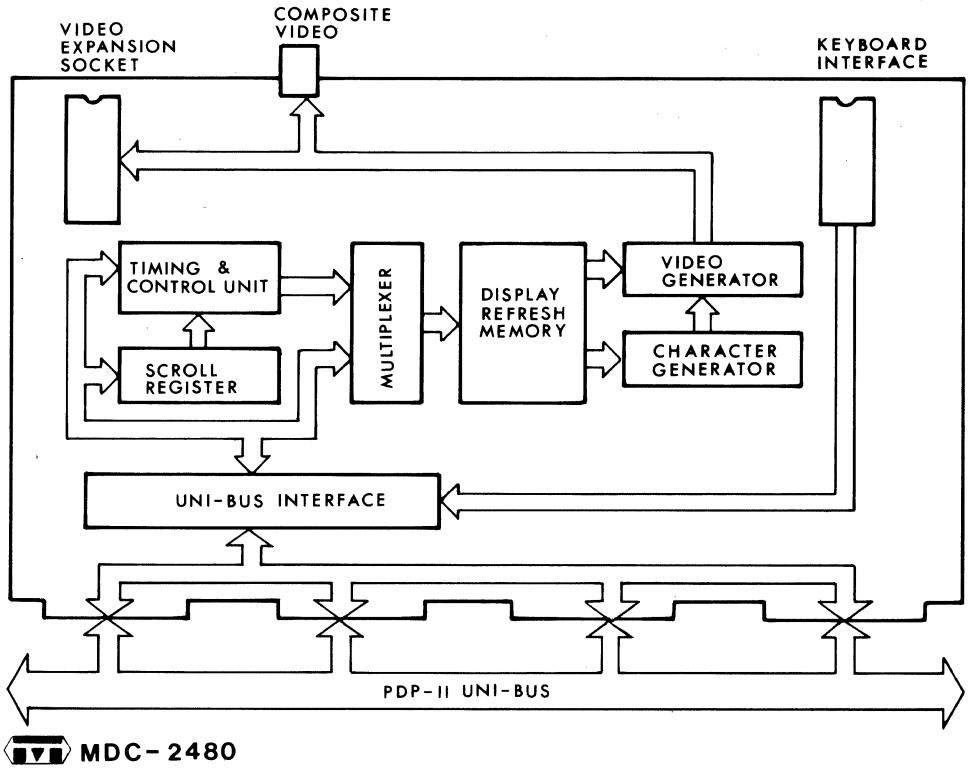



Figure 1. MDC-2480 block diagram

## FUNCTIONAL DESCRIPTION

The MDC-2480 is made up of five major operational blocks: Timing and Control Unit, Display Memory, Character Generator, Video Generator, and Bus Interface. Communications between these blocks are shown in figure 1.

## TIMING AND CONTROL UNIT

All timing and control signals required to generate a video display with 24 lines of 80 characters per line are supported on-board the MDC-2480. The Timing and Control Unit, consisting of the master oscillator (11 MHz) and various modulo counters, produces the horizontal and vertical sync signals needed by the monitor as well as all timing signals for display refresh memory (RAS, CAS).

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the MDC-2480 can be synchronized to operate with other video boards as part of a complete video display system.

## DISPLAY MEMORY

The MDC-2480 contains 2K bytes of on-board display refresh memory, to store up to 24 lines of 80 characters (1920 characters). The display memory occupies 4K bytes of system address space thereby permitting the CPU to identify each character location with a unique 12 bit address.

The MDC-2480 can be strapped so that the display memory is arranged as two independently accessable pages. In this way the MDC-2480 is capable of storing two displays of 24 x 40 characters, of which one display can be updated while the other is being displayed. An on-board Video Control Register allows the user to software select which page is to be displayed.

Each character position on the CRT screen corresponds to an 8 bit location in the Display refresh memory. Characters are written on to the display by loading the ASCII Character Code to the appropriate display memory location. The CPU can read/write the display memory at full speed using all memory reference instructions.

All accesses to the display memory are controlled by a "Transparent Memory" control circuit within the Timing and Control Unit. In this way all accesses to the display memory (read, write, refresh) are efficiently arbitrated. The Transparent Memory control circuitry permits the CPU to read or write the refresh memory at any time and the display is free of glitches.

## CHARACTER GENERATOR

The MDC-2480 contains an on-board 2716 EPROM which contains the binary video information to generate a 128 character set. The supplied character font consists of the full 96 upper/lower case alphanumeric character set with the addition of 32 special graphic characters. The alphanumeric characters are formed in a 5 x 7 dot matrix within a 6 x 10 dot character cell. The graphics characters utilize the entire character cell to allow for drawing continuous lines. For greater inter-character spacing the character cell size can be increased, with hardware straps, to 8 x 10 dots. Note that increasing the character cell size will cause gaps to appear between the graphics characters. Also, a different crystal is required for applications utilizing an 8 dot cell.

The MDC-2480 permits simple implementation of custom character fonts. To install a new character set, the user need only reprogram the EPROM character generator with the video information to generate his own font.

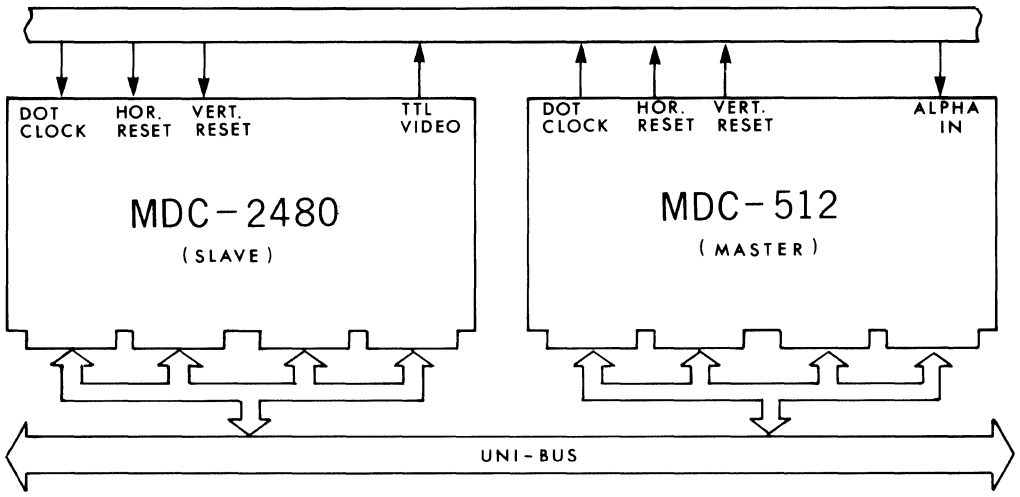



Figure 2. Combining MDC-2480 with MDC-512 for alpha/graph displays



**ATTRIBUTES**
Each character is accessed by seven bits of the eight bit ASCII Character Code. This releases the most significant eighth bit for attribute selection. Characters displayed on the MDC-2480 can be displayed either as normal (white on a black background) or inverted (black on a white background), and can be set as blinking or non-blinking. Character attributes are selected by on-board hardware straps and are enabled/disabled by the eighth bit of the character code.

The on-board character generator can be strapped to provide a reduced 64 character set which contains only the upper case alphanumeric characters. Using this character set the MDC-2480 uses only six of the eight data bits and therefore enables selection of two attributes per character.

**SCROLL**
The MDC-2480 allows the user to vertically rotate the display (scroll). Loading the on-board Scroll Register with any line number (0 to 23) will cause the display to vertically rotate until the specified line is displayed at the top of the screen.

**VIDEO GENERATOR**
The MDC-2480 can directly drive any standard monochrome video monitor. Composite video signals as well as separate TTL video, horizontal/vertical sync and blinking signals are supported on-board.

**KEYBOARD INTERFACE**
A keyboard can be interfaced to the MDC-2480 through a 16 pin DIP socket, S7. The keyboard input port consists of seven input lines and one strobe line (positive pulse). Once the keyboard data strobe has been received, the Keyboard Flag is set.

**BUS INTERFACE**
The MDC-2480 plugs directly into the PDP-11 UNI-bus. The display refresh memory, which is memory mapped into the PDP-11 UNI-bus memory address space, can be strapped to reside at any 4K byte memory address boundary between 000 000$_8$ and 777 777$_8$.

**GRAPHICS**
The MDC-2480 can be integrated, as an alphanumeric controller, within a complete alpha/graph video system. By configuring the MDC-2480 to operate in the slave mode, the horizontal/vertical reset lines and the dot clock line are set to act as input ports. In this way the board can be synchronized to a master sync source. These lines can also be configured to operate as output ports to enable the user to configure his system to synchronize to the MDC-2480. A typical application of combined alphanumerics/graphics is shown in figure 2, where the graphics board (MDC-512) acts as the master sync source.

**PROGRAMMING**
The MDC-2480 operational status (American/European compatibility, Master/Slave operation, base address, etc) is programmed via on-board hardware straps. Table 1 outlines the definitions of these straps.

| JUMPER NO. | DESCRIPTION | JUMPER NO. | DESCRIPTION |
|---|---|---|---|
| S1 1-6 | Select base address | S6 4-6 | Enable "Dual Page" mode |
| S3 1-10 | Select American/European TV standard | W2 | Enable "Dual Page" mode |
| S4 1-3,6-7 | Select character attribute | W3 | Enable "Dual Page" mode |
| S5 1-8 | Select character cell size | W4 | Enable "Dual Page" mode |
| S4 4-5 | Select character cell size | W0 | Enable "Master" mode |
| S6 7-8 | Select character set | W1 | Enable "Slave" mode |
| S8 8 | Select character set | W5 | Enable transparent memory mode |
| S6 1-2 | Select displayed page | W6 | Disable transparent memory mode |

Table 1. Jumper Definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

With Transparent Memory: 800ns
Without Transparent Memory: 500ns

### DISPLAY PARAMETERS

| DESCRIPTION | DISPLAY |
|---|---|
| Resolution | 1920 characters |
| Horizontal Characters | 80 characters |
| Vertical Lines | 24 lines |
| Character Cell Size | 6 or 8 horizontal dots |

### VIDEO TIMING

To generate a video display of 24 x 80 characters with a 6 dot wide character cell, the MDC-2480 uses an 11.06688 MHz crystal. The following tables gives the video timing for both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 43.0 μs | 43.0 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 4.3 μs | 4.3 μs |
| Vertical Sync Frequency | 60.0 Hz | 50.2 Hz |
| Vertical Sync Width | 255.0 μs | 255.0 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Drive
Vertical Drive
Composite Sync
Composite Video

### BUS INTERFACE

Address, data and control signals conform to PDP-11 UNI-bus specifications
Control Registers and Display Memory — Selectable on any 4K byte memory address boundary between 000 000$_8$ and 777 777$_8$ (760 000$_8$).

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| C : 36 pin edge connector<br>D : 36 pin edge connector<br>E : 36 pin edge connector<br>F : 36 pin edge connector | Bus Interface | DEC H8030 (2 required) |
| J1 : 16 pin DIP socket | — Video Interface | AUGAT 516-A6-37D |

### PHYSICAL

**SIZE**

Width: 5.25 in. (13.33 cm)
Height: 8.50 in. (21.59 cm)
Depth: 0.50 in. (1.27 cm)

**POWER REQUIREMENTS**

+ 5V ± 5% @ 0.9A

**ENVIRONMENTAL REQUIREMENTS**

Operating temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

MDC-2480 — XX- X
- X — Horizontal dots per character (6/8)
- XX — AS — American standard (60 Hz); ES — European standard (50 Hz)

Example: MDC-2480-AS-6: 24 x 80 character display using a six dot wide character cell. Vertical refresh rate is 60 Hz

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MDC-512

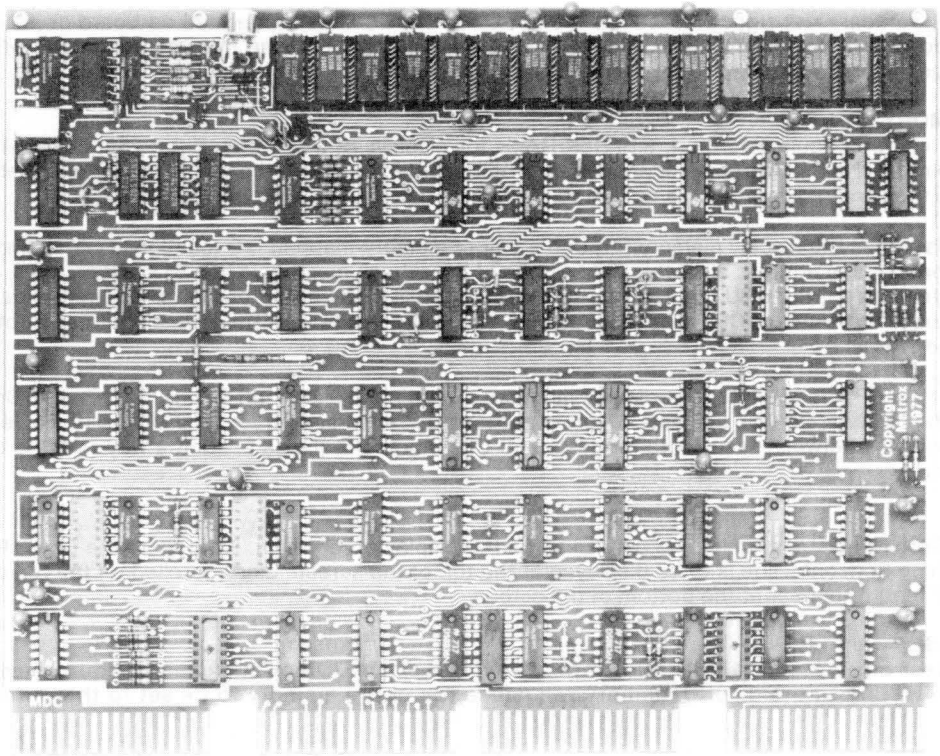
## 512 x 512 GRAPHICS DISPLAY CONTROLLER FOR PDP-11 UNI-BUS

- **Bit mapped 512 x 512 pixel display**
- **256 x 256, 512 x 256, 1024 x 256 formats available**
- **Powerful X-Y virtual memory addressing**
- **Hardware scroll built-in**
- **Single instruction memory erase**
- **Color/grey-scale expansion**
- **Can be combined with MDC-2480**
- **Transparent memory access**
- **PDP-11 UNI-bus* compatible**
- **Internal/external sync**
- **American/European operation**

3

The MDC-512 is a member of Matrox's complete line of PDP-11 UNI-bus compatible graphics video boards. The MDC-512 family of cards is designed to interface a mini or microcomputer to a CRT monitor and produce a B/W display of 512 x 512 points. The board also features built-in hardware scroll capabilities and a single instruction memory erase.

The MDC-512 can also be combined with the MDC-2480 to produce a complete alphanumerics/graphics video display system. Combining multiple MDC-512 cards, the OEM system designer can construct a graphics display system with up to 24 bits/pixel (16 million different colors or grey levels).






**MATROX products covered by Canadian and foreign patent and/or patent pending.**

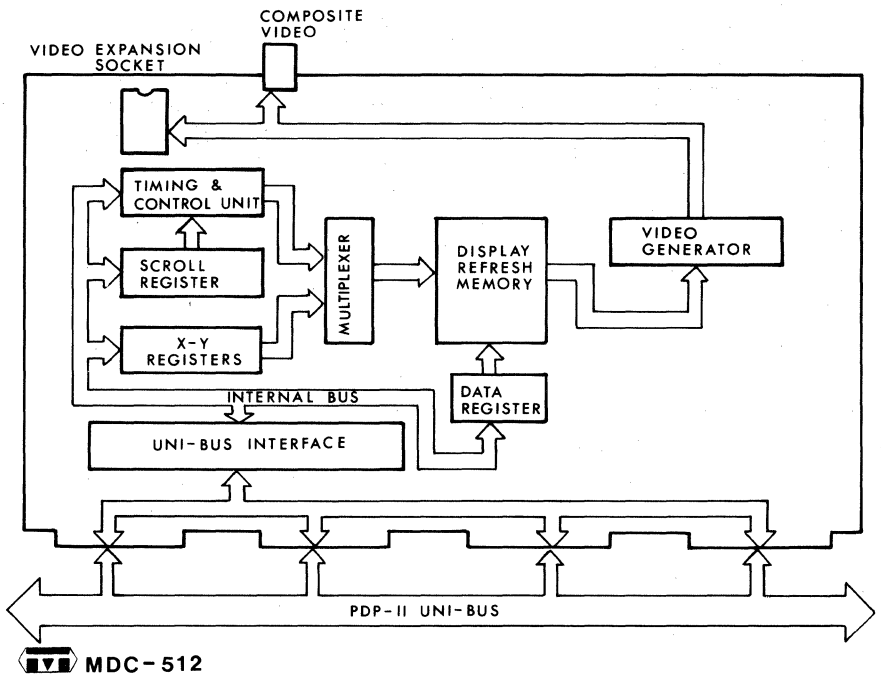



Figure 1. MDC-512 block diagram

## FUNCTIONAL DESCRIPTION

The MDC-512 consists of six main functional blocks (figure 1): Timing and Control Unit, Scroll Register, X-Y Registers, Display Memory, Video Generator, and Bus Interface.

## TIMING AND CONTROL UNIT

All timing and control signals required by the video monitor (horizontal/vertical sync and blanking), display refresh memory (row/column addressing), and video generator (dot clock, load and shift) are generated by the Timing and Control Unit. The exact configurations of these signals are user-programmable, via hardware straps, to enable the MDC-512 to generate displays with up to 512 horizontal dots by 512 vertical dots. The board can also be strapped to operate in either 50 Hz (European) or 60 Hz (American) systems.

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the MDC-512 can be synchronized to operate with other video boards as part of a complete video display system.

## DISPLAY MEMORY

The MDC-512 can be populated with 4, 8 or 16K RAMs for displays of 256 x 256, 512 x 256, 512 x 512, or 1024 x 256 dots. Each point on the CRT screen is identified by a unique address within the display memory. When a point is to be illuminated on the screen, a logic "1" is written to the appropriate display memory location.

The CPU reads/writes the display memory through a pair of memory-mapped I/O locations (X-Y Registers). This allows two memory locations to address all of the 262,144 bits of the refresh memory (512 x 512). Once the X and Y address of the dot has been loaded, the CPU can read/write the dot intensity. The dot intensity bit (image bit) can be assigned to any data bus bit. The resultant CRT display is a black and white image with the intensity of each dot being either on (logic "1") or off (logic "0").

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the MDC-512 efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display is "transparent" to user.

## SCROLL

An on-board Scroll Register enables the user to scroll the display up or down. By loading the Scroll Register the user can specify which horizontal line is to be displayed at the top of the screen. Lines scrolled off the top of the display will "wrap-around" and re-appear at the bottom of the screen.

## SCREEN ERASE

The entire refresh memory on the MDC-512 can be erased by a single OUTput instruction. Setting the memory erase enable bit when writing to the display memory will cause the entire memory to be set to that intensity (0 = black, 1 = white).

## VIDEO GENERATOR

The MDC-512 works with all standard monochrome video monitors in American (60 Hz) and European (50 Hz) systems. TTL level video, horizontal sync, vertical sync, as well as composite video signals are supported on-board.

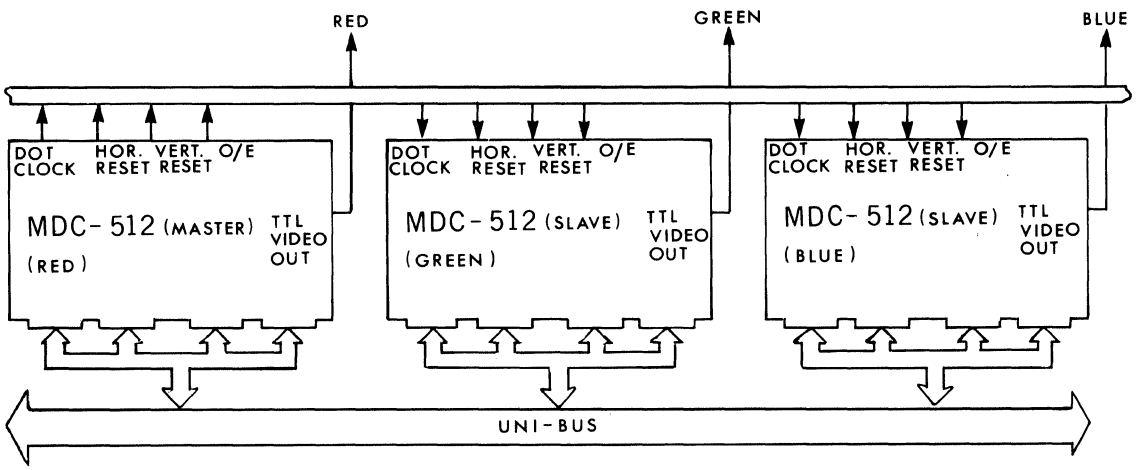



Figure 2. "Stacking" MDC-512 cards for color/grey scale displays



**BUS INTERFACE**

The MDC-512 plugs directly into the PDP-11 UNI-bus and works with both 8-bit and 16-bit processors. All the Command and Status Registers as well as the Display Memory are accessed via memory mapped I/O. The MDC-512 can be positioned on any 8 byte memory address boundary between 000 000 and 777 777$_8$.

**ALPHA/GRAPH DISPLAYS**

The MDC-512 can be combined with the MDC-2480 to generate alphanumeric/graphic displays. An on-board alphanumeric input port accepts the TTL level alphanumeric video information from the MDC-2480 and combines it with the graphics video from the MDC-512. The result is a powerful display combining both alphanumerics and graphics without the overhead involved in generating alphanumeric characters using graphic techniques.

**COLOR/GREY-SCALE EXPANSION**

Multiple MLSI-512 cards can be combined to provide for color/grey-scale displays. As previously outlined (DISPLAY MEMORY), the image bit on a given card can be assigned to any data bus bit. Thus the output of each card can be assigned a different weight or color. By assigning cards to different data bus bits and strapping all the cards with the same address, the intensity or color of a given dot can be loaded in a single instruction. A typical example of building up a color video system using the MLSI-512 is shown in figure 2.

**PROGRAMMING**

The MLSI-512 is programmed, for various display resolutions, by on-board hardware straps. These straps are organized into three 16 pin "programming sockets" to facilitate simple re-programming of the board. Table 1 defines the on-board jumpers used to configure the MLSI-512 for the various resolution options.

| SOCKET | JUMPER | DESCRIPTION |
|---|---|---|
| P | 1 | Vertical display = 240 lines (American standard) or 256 lines (European standard) |
| | 2 | Vertical reset = 262½ lines (American standard) |
| | 3 | Vertical reset = 312½ lines (European standard) |
| | 4 | Vertical sync = 244 lines (American standard) |
| | 5 | Vertical sync = 276 lines (European standard) |
| | 6 | Not used |
| | 7 | Enable 512 dot vertical resolution |
| | 8 | Not used |
| R | 1 | Enable 1024 dot horizontal resolution |
| | 2 | Set memory access for RAM type used |
| | 3 | Enable 1024 dot horizontal resolution |
| | 4 | Disable 1024 dot horizontal resolution |
| | 5 | Synchronize blanking for 512/1024 dot horizontal resolution |
| | 6 | Synchronize blanking for 256 dot horizontal resolution |
| | 7 | Dot clock = 5.53344 MHz (256 dot horizontal resolution) |
| | 8 | Dot clock = 11.06688 MHz (512/1024 dot horizontal resolution) |
| J | 1 | Enable 256 x 256 addressing |
| | 2 | Enable 512 x 256 addressing |
| | 3 | Enable interlaced addressing (512 x 512/1024 x 256) |
| | 4 | Enable 512 dot horizontal addressing |
| | 5 | Enable 1024 dot horizontal addressing |
| | 6 | Enable 512 dot vertical addressing |
| | 7 | Synchronize LOAD SCROLL signal to 60 Hz (American standard) |
| | 8 | Synchronize LOAD SCROLL signal to 50 Hz (European standard) |

Table 1. Jumper Configurations

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μs

### DISPLAY PARAMETERS

| RESOLUTION | RAM TYPE |
|---|---|
| 256 X 256 | 4K |
| 512 X 256 | 8K |
| 512 X 512 | 16K |
| 1024 X 256 | 16K |

### VIDEO TIMING

For a 256 x 256 or 512 x 256 display, the video output is non-interlaced. For a 512 x 512 or 1024 x 256 display, the video output is interlaced (two fields per frame). In order to avoid display flicker, a monitor with long persistence phosphors must be used.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46 μs | 46 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 5.67 μs | 5.67 μs |
| Vertical Sync Frequency | 60 Hz | 50.2 Hz |
| Vertical Sync Width | 190 μs | 190 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Sync
Vertical Sync
Composite Sync
Composite Video

### BUS INTERFACE

Address, data, and control signals conform to PDP-11 UNI-bus Specifications
Display Memory, Command and Status Registers — Selectable on any 8 byte memory address boundary between 000 000$_8$ and 777 777$_8$ (760 000$_8$)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| C : 36 pin edge connector, 0.125" centers<br>D : 36 pin edge connector, 0.125" centers<br>E : 36 pin edge connector, 0.125" centers<br>F : 36 pin edge connector, 0.125" centers | Bus Interface | DEC H8030 (2 required) |
| J1 : phono connector | — Composite Video | RCA 901 |
| V : 16 pin DIP socket | — Video Expansion Socket | AUGAT 516-A6-37D |

## PHYSICAL

### SIZE

Width: 10.50 in. (26.67 cm)
Height: 7.75 in. (19.69 cm)
Depth: 0.50 in. ( 1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5° @ 800mA
+12V DC ±5° @ 200mA

### ENVIRONMENTAL REQUIREMENTS

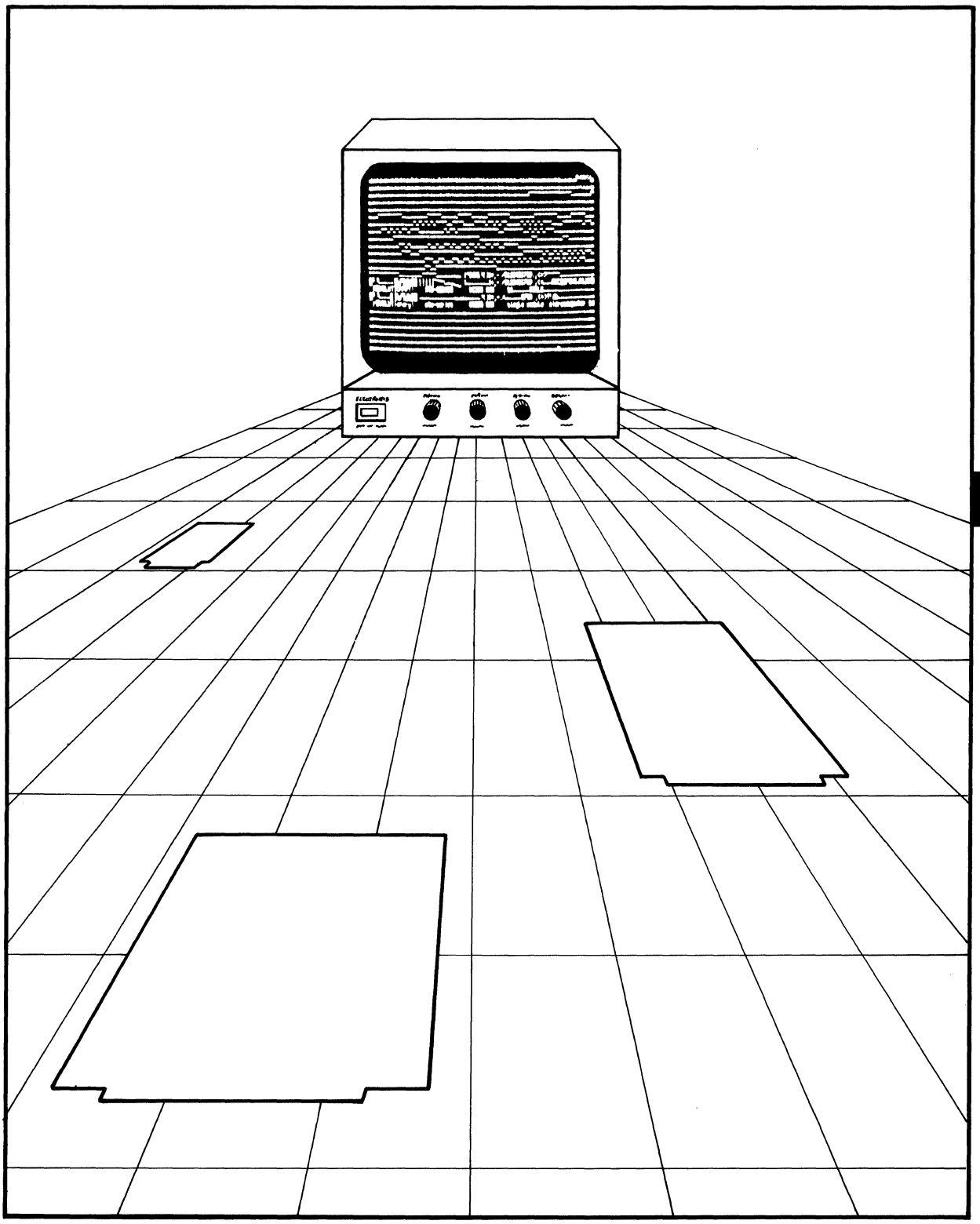
Operating Temperature: 0°C to 55°C
Relative Hymidity: 0% to 95% non-condensing

### ORDERING INFORMATION

MDC — XXX/XXX — XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- XXX (second): Vertical resolution (256/512)
- XXX (first): Horizontal resolution (256/512/1024)

Example: MDC-512/512-AS: 512 x 512 pixel display with a vertical refresh rate of 60 Hz.





# STD-BUS VIDEO BOARDS

## SECTION 4 STD-BUS VIDEO BOARDS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

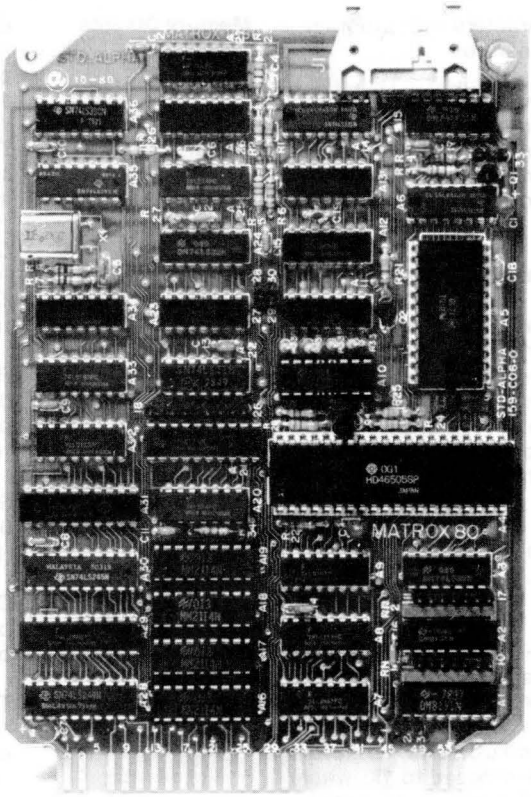
# STD-ALPHA

## VARIABLE FORMAT ALPHANUMERIC DISPLAY CONTROLLER FOR STD-BUS

- **Software programmable text format**
- **Up to 128 characters/row**
- **Up to 48 characters/column**
- **Up to 2048 characters/page**
- **Scroll**
- **Blink**
- **Inverse video**
- **Underline**
- **Programmable character height**
- **128 text/graphic symbols**
- **STD-bus compatible**
- **Single +5V power supply**
- **50/60 Hz operation**
- **Programmable cursor**
- **Light pen interface**

4

The STD-ALPHA is a very flexible alphanumeric video controller. The video display format (number of rows and columns of characters) is software programmable over a wide range. Also. the video sync information is software programmable for 50 Hz, 60 Hz or non-standard monitor requirements. The STD-ALPHA also features several powerful attributes including scroll, blink, inverse video, and underline.



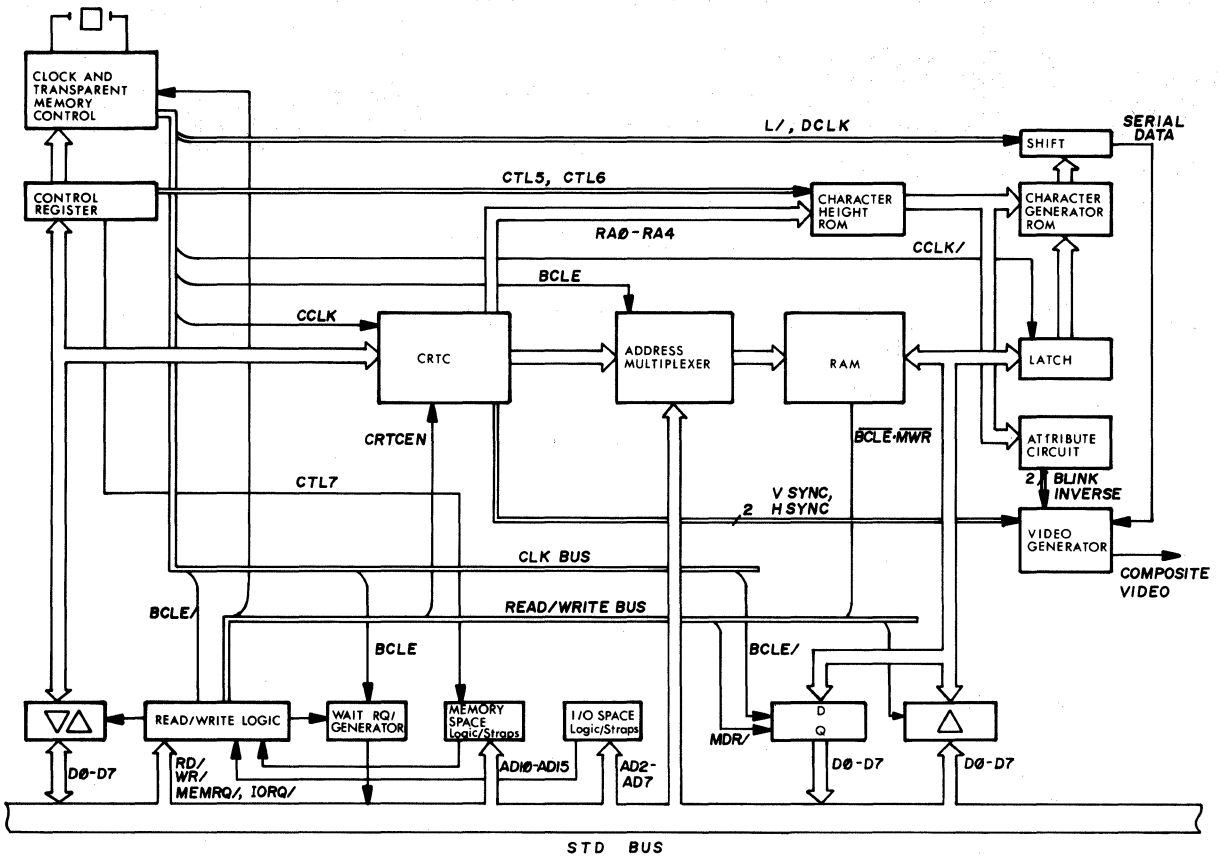



Figure 1. STD-ALPHA block diagram

## STD-ALPHA FEATURES

**Resolution** Up to 2048 characters with programmable display features

**Display Parameters** All video parameters including horizontal and vertical sync, blanking, and display formats are user software programmable to drive any direct or composite B/W monitor.

**Character Attributes** Inverse video, blink, and underline attributes are available on-board.

**Character Set** 128 upper/lower alphanumeric characters and graphics symbols are available through an on-board MCH-01 character generator. The character set can be reduced, with hardware straps, to produce a 64 lower case only alphanumeric character set.

**Character Height** Characters can be software selected to be 1, 2, 3, or 4 times normal height.

**Display Ram** 2K bytes of on-board memory, strap-selectable on any 2K byte boundary in system address space. CPU can read/write memory using all memory reference instructions. Display memory can be reduced to 1K, when used with small formats, to economize on RAM.

**Memory Disable** External access to the display memory can be software-disabled to permit multiple boards to occupy the same space in system memory.

**Scroll** The display "window" can be scrolled up or down with respect to information in the display memory.

**Cursor** Cursor is inverted video that can be full character, underline, or blink. The cursor position is software controlled.

**Light Pen** Built-in light pen interface. CPU can dynamically read the light pen position through an internal CRTC register.

**TV Standard** STD-ALPHA can operate in either 60 Hz (American standard) or 50 Hz (European standard).

**Video Outputs** Direct TTL level or 1Vpp, 75Ω composite video signals are available on-board.

**STD-Bus Interface** The STD-ALPHA is contained on a single 6.5" x 4.48" PC board which is plug-in compatible with the STD-bus. All address, data, and control signals are STD-bus compatible.

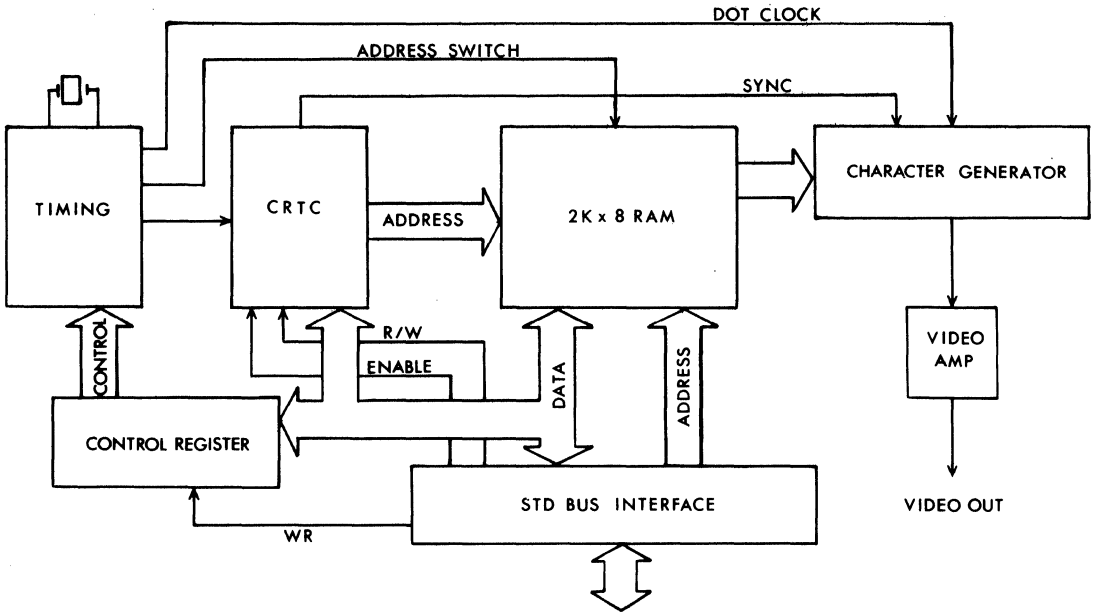



Figure 2. STD-ALPHA functional blocks

## FUNCTIONAL DESCRIPTION

The STD-ALPHA provides a versatile alphanumeric display system for the STD-bus based system designer. Contained on a single 6.5" x 4.48" printed circuit board is all the required circuitry for generating up to 2048 character displays. The STD-ALPHA can be regarded as six major functional blocks (figure 2); Display Memory, CRT Controller, Character Generator, Video Amplifier, Timing and Control Unit, and a Bus Interface.

The **Display Memory** on the STD-ALPHA is made up of 4 2114 static RAMs providing a 2K byte memory-mapped storage area. Addressable on any 2K byte boundary in system address space, the STD-ALPHA's display memory can be software disabled through programmed I/O command to enable the user to place multiple boards in the same address space. Also, when used with small display formats, the display memory can be reduced to 1K bytes to economize on address space. Access time varies from access to access depending on the display format and timing requirements used and on where the access is initiated with respect to the display refresh cycle. The average access time for formats using 128 characters/line is 343ns with 6 dots/cell and 500ns with 8 dots/cell. In less dense formats the average access time approaches 240ns.

Each character position on the CRT screen corresponds to a single location (8 bits) in the display refresh memory. When a character is to be displayed, its Character Code is written into the appropriate display memory locations. The processor can read or write the display memory at full speed using all memory reference instructions.

All display memory accesses (read, write, or refresh) are controlled via a Transparent Memory Control circuit. Through this circuit the RAM address lines are switched between the CRTC (display refresh) and the system bus (display memory read/write) by three 1 to 2 line multiplexers. By assuring that the system bus can not acquire memory access while the display is being refreshed (figure 3), the STD-ALPHA avoids any memory contention problems that would result in display streaking.

The **CRT Controller (CRTC)** is a VLSI IC which provides all the necessary signals (horizontal and vertical blanking and sync, display refresh RAM addresses, etc.) required to generate video displays. Through the CRTC, virtually all display format parameters are user selectable (figure 4). Display resolutions are only restricted by the intrinsic characteristics of the monitor used. For most monitors (active video

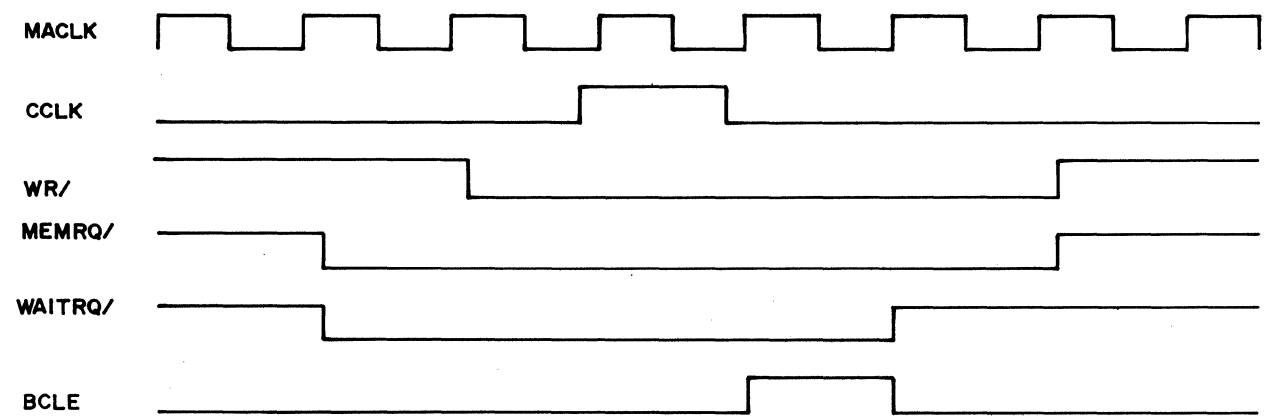



Figure 3: Transparent Memory Control Timing Diagram

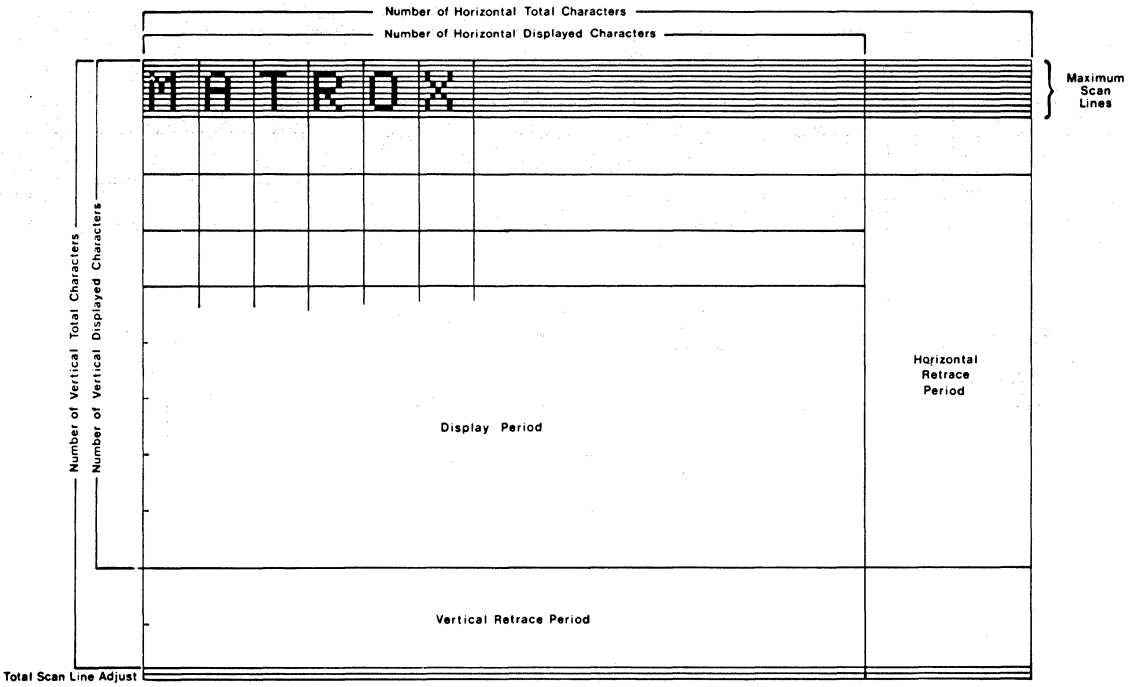



Figure 4: Display Format Parameters

time = 48μs) up to 128 characters per line can be formatted. Up to 48 character rows can be displayed on monitors using a 60 Hz Vertical Scan Rate (American standard) while a maximum of 52 lines can be programmed for monitors using a 50 Hz scan rate (European standard). Note that the number of characters formatted per display can not exceed 2048.

The CRT Controller can also be programmed to generate a displayable cursor, the position of which can be independently controlled by the CPU. The cursor is displayed on the CRT as inverse video (dark areas become light and light areas become dark) that can be full character, underline, or blink (blink rate = 2 or 4 Hz). The entire display can be "scrolled" up or down through programmed I/O command. In this way the user can move the display "window" to view the entire display memory. The CRTC also enables the STD-ALPHA to latch the position of an external light pen. Once latched, the light pen position can be read by the CPU.

The CRTC looks to the CPU as an array of 18 registers which are indirectly accessed through two I/O ports. Display format parameters (number of characters/line, number of lines, horizontal and vertical refresh frequency, etc.) are established by loading these internal CRTC registers.

The **Character Generator (MCH-01)** is a 2K x 8 ROM which can generate 128 characters, including ASCII upper and lower case and 32 graphics symbols (figure 5). The MCH-01 accepts the ASCII-coded Character Code (stored in display memory) as an address pointing to a 6 x 10 bit "character cell". Within this character cell the binary information required to generate the character is stored. The Character Generator can be strapped to supply a reduced set of 64 characters. The reduced character set does not include the lower case characters or the graphic symbols. Also the MCH-01 Character Generator is pin-compatible with the 2516 EPROM so that the user can easily implement his own custom character font.

A character height PROM is included in the character generation circuitry. This PROM addresses the individual character rows within the character cell and determines how many times each horizontal character segment is addressed per character. In this way the character height can be effectively expanded. The character height PROM, under software control, produces characters that are 1, 2, 3, or 4 times the normal character height. Moreover, when used in the interlaced mode, these character heights are halved, thereby providing a total of six possible character heights.

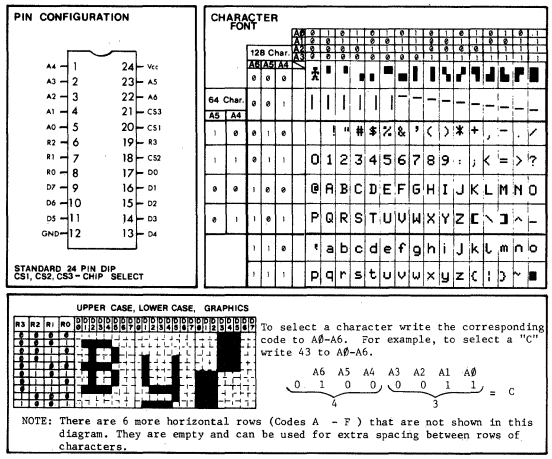



Figure 5: STD-ALPHA Character Set

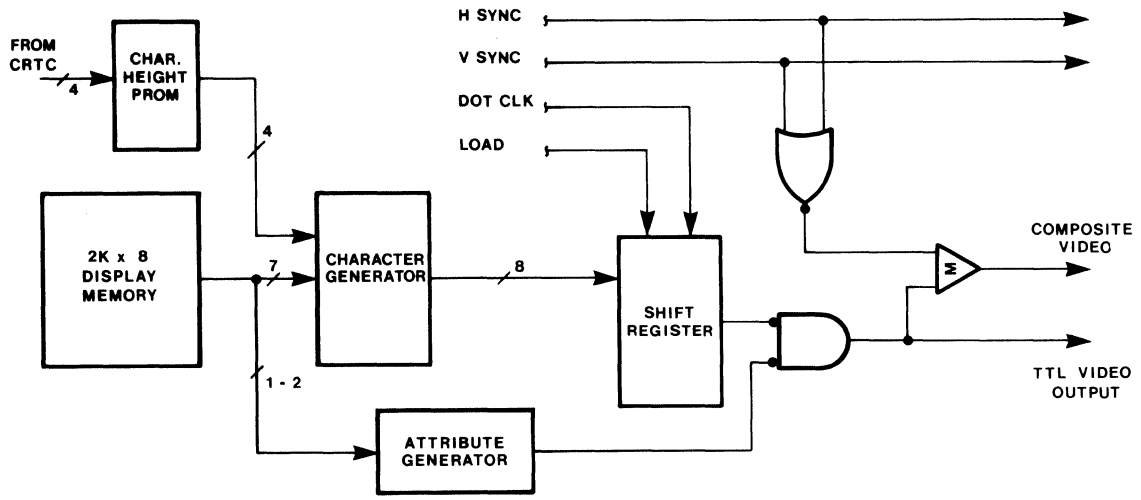



Figure 6: Video Amplifier and Attribute Generation Circuitry

The **Video Amplifier** (figure 6) on the STD-ALPHA accepts the video information as a serial data stream, through a shift register, from the character generator. This data is then synchronized with the vertical and horizontal sync signals and sent out as TTL level video outputs. Alternately the output video can be combined with the sync signals to produce a standard 1Vpp, 75Ω terminated composite video signal.

Character attributes can be added to each character as it passes through the video amplifier. The STD-ALPHA offers three on-board character attributes; blink, inverse video, and underline. When used with the full 128 character set any one of these attributes can be strap-selected. With the reduced 64 character set, up to two attributes per character may be selected. Character attributes are enabled by the unused bits in the Character Code (1 bit in the 128 character set and 2 bits in the reduced set).

The **Timing and Control Unit** generates the timing signals required by the CRTC (Character Clock) and the video amplifier (Dot Clock and Load) to generate the video displays. The Timing and Control Unit also generates the timing signals necessary for the display refresh memory (Memory Access Clock). This circuit (figure 7) consists of the master oscillator (16 MHz crystal), variable modulo counter (divide by 1-8) which is controlled by the programmed number of dots/cell to produce the Memory Access Clock (used to switch memory accesses between system bus and display refresh) and the appropriate load and shift signals for the display. The Timing and Control Unit also includes two divide by 16 counters which provide the Dot Clock and Character Clock signals.

The **STD-Bus Interface** contains the logic required to interface the STD-ALPHA with the STD-bus. The position of the STD-ALPHA's I/O ports and display memory within the system address space is determined by comparing bus addresses against a set of straps (I/O ports are addressable on any 4 byte address boundary in system address space and the display memory can be strapped to any 2K block of system memory space).

**Programming**

The STD-ALPHA is programmed through 3 I/O registers. Two of these registers (CRTC Address Register and CRTC Data Port) are used in turn to load 18 internal CRTC registers. By loading these registers the user can program the STD-ALPHA to generate displays using virtually any display format (Table 1).

| Parameter | Description |
|---|---|
| Horizontal Characters | Up to 128 |
| Vertical Lines | Up to 48<br>(52 with European standard) |
| Character Height | 1, 2, 3, 4 times normal |
| Character Cell Width | 6/8 dots |
| Vertical Refresh Rate | 50 Hz/60 Hz |
| Raster Scan | Interlaced/non-interlaced |

Table 1: Programmable Display Format Parameters

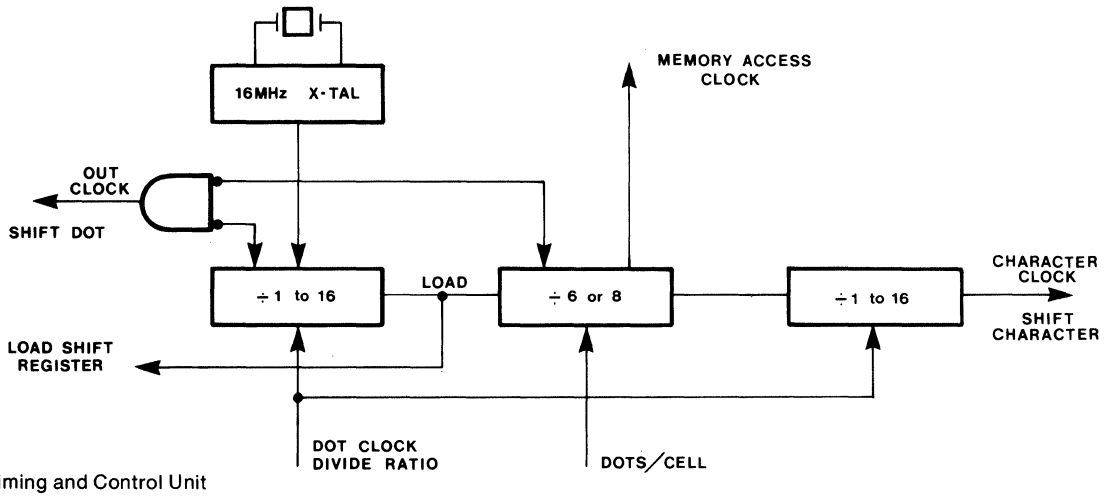



Figure 7: Timing and Control Unit

| Relative Location | Direction | Name | Function |
|---|---|---|---|
| 00H | WRITE ONLY | CRTC Address Register | Select CRTC register to be accessed. |
| 01H | READ WRITE | CRTC Data Port | CRTC register addressed by the CRTC Address Register |
| 02H | WRITE ONLY | Control Register | Selects Dot Clock Divider, Dots/cell, Character height, memory enabled/ disabled. |

Table 2: STD-ALPHA I/O registers

| Address 4 3 2 1 0 | Register Number | Register Name | Function |
|---|---|---|---|
| 0 0 0 0 0 | R0 | Horizontal Total | Total number of horizontal characters including retrace. |
| 0 0 0 0 1 | R1 | Horizontal Displayed | Number of characters displayed per line. |
| 0 0 0 1 0 | R2 | H. Sync Position | Horizontal sync position in units of horizontal character time. |
| 0 0 0 1 1 | R3 | Sync Width | Horizontal and vertical sync pulse widths in units of horizontal character time. |
| 0 0 1 0 0 | R4 | Vertical Total | Total number of vertical lines per frame including retrace. |
| 0 0 1 0 1 | R5 | Vertical Total Adjust | Optimum number from 0-31 to adjust total number of rasters per frame. |
| 0 0 1 1 0 | R6 | Vertical Displayed | Number of displayed character rows per frame. |
| 0 0 1 1 1 | R7 | V. Sync Position | Vertical sync position in units of horizontal character time. |
| 0 1 0 0 0 | R8 | Interlace/ Skew | Set up raster scan mode and skews of CUDISP, DISPTMG signals. |
| 0 1 0 0 1 | R9 | Max. Raster Address | Defines total number of rasters per character including spacing. |
| 0 1 0 1 0 | R10 | Cursor Start Address | Cursor start raster address and cursor display mode. |
| 0 1 0 1 1 | R11 | Cursor End Address | Cursor end raster address. |
| 0 1 1 0 0 | R12 | Start Address (HI) | Address of refresh memory to read out. |
| 0 1 1 0 1 | R13 | Start Address (LO) | |
| 0 1 1 1 0 | R14 | Cursor (HI) | Cursor display address. |
| 0 1 1 1 1 | R15 | Cursor (LO) | |
| 1 0 0 0 0 | R16 | Light Pen (HI) | Light Pen latch. |
| 1 0 0 0 1 | R17 | Light Pen (LO) | |

Table 3: CRTC Registers

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

The number of wait states required by the STD-ALPHA depends upon the type of access (read or write), the speed of the CPU, and where the RD and WR requests fall in relation to the board's internal timing. In the worst case three wait states are required for a memory write using a 4 MHz CPU.

Access to the STD-ALPHA I/O ports is fast enough that wait states, other than the one automatically inserted by the CPU, are not required and WAITRQ is never pulled low.

### DISPLAY PARAMETERS:

| PARAMETER | DESCRIPTION |
|---|---|
| Resolution | 2048 characters max. |
| Horizontal columns | 128 characters max. |
| Vertical rows | 48 lines max. (American), 52 lines (European) |
| Character cell size | 6/8 dots horizontal |
| Character height | 1,2,3,4 times normal |
| Vertical refresh rate | 50 Hz/60 Hz |

### VIDEO TIMING

The following table gives the video timing, for both American and European systems, of a display with 24 lines of 80 character using the standard 16 MHz crystal. Note that all these parameters are programmable and are determined by the user.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 40 μs | 30 μs |
| Horizontal Sync Frequency | 15.78 KHz | 15.68 KHz |
| Horizontal Sync Width | 5.25 μs | 5.62 μs |
| Vertical Sync Frequency | 59.97 Hz | 49.95 Hz |
| Vertical Sync Width | 191.12 μs | 191.25 μs |

| IMPUT SIGNALS | OUTPUT SIGNALS |
|---|---|
| Light Pen Enable | TTL Level Video |
| Light Pen Strobe | Horizontal Drive |
| | Vertical Drive |
| | Composite Video |

### BUS INTERFACE

Address, data, and control signals conform to Mostek-Prolog STD-bus specifications.
Command and Status Registers — Selectable on 4 byte I/O boundaries 00 - FF (FCH)
Display Refresh Memory — Selectable on 2K byte memory address boundaries 0000 — FFFF (B000H)

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1 : 56 pin edge connector — STD-bus Interface | ANSLEY 609-561 5M |
| J1 : 10 pin right angle header — Video Interface/Light Pen Interface | MOLEX 10-55-3103 |

## PHYSICAL

| SIZE | POWER REQUIREMENTS | ENVIRONMENTAL REQUIREMENTS |
|---|---|---|
| Width: 4.48 in. (11.38 cm)<br>Height: 6.50 in. (16.51 cm)<br>Depth: 0.50 in. ( 1.27 cm) | +5V DC ±5% @ 2A | Operating Temperature: 0°C to 55°C<br>Relative Humidity: 0% to 95% non-condensing |

### ORDERING INFORMATION

STD-ALPHA — XXX

- 015 — No underline
- 016 — Underline in row 12 (in character cell)
- 072 — Underline in row 10 (in character cell)

Example: STD-ALPHA-016: Programmable format alphanumeric display controller with an underline attribute supported in line 12 of the character cell.

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matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# STD-2480

## 24 x 80 ALPHANUMERIC DISPLAY CONTROLLER FOR STD-BUS

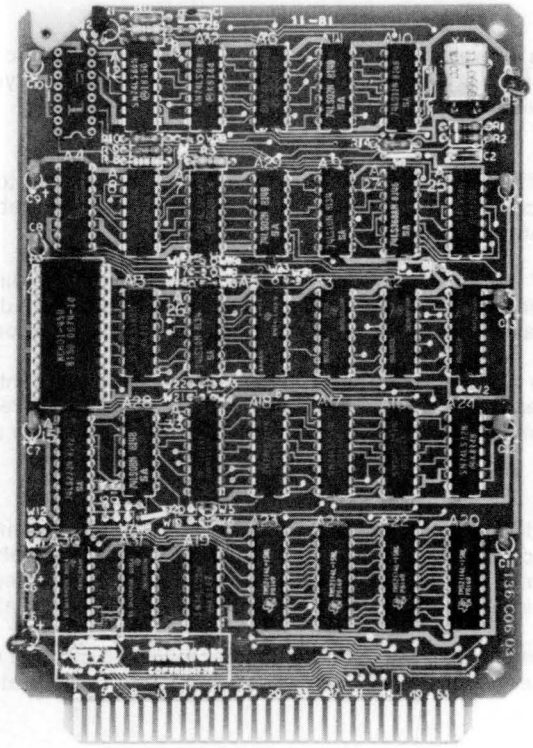
- **24 row x 80 column alphanumeric video display**
- **STD-bus compatible**
- **Inverse video**
- **Blink**
- **Directly drives any monochrome monitor**
- **Single +5V supply**
- **External/internal Sync capability**
- **American/European operation**

4

The STD-2480 is a STD-bus compatible alphanumeric display controller which is capable of generating displays of 24 lines of 80 characters per line. Characters can be displayed as either white on a black background or black on a white background. Each character can also be set to blink under software control.

The character font provided with the STD-2480 contains 128 - 5 x 7 upper/lower case alphanumeric characters and graphic symbols. A custom character generator can be user programmed for special font requirements.

The STD-2480 works with all standard monochrome video monitors in Europe (50 Hz) and America (60 Hz).



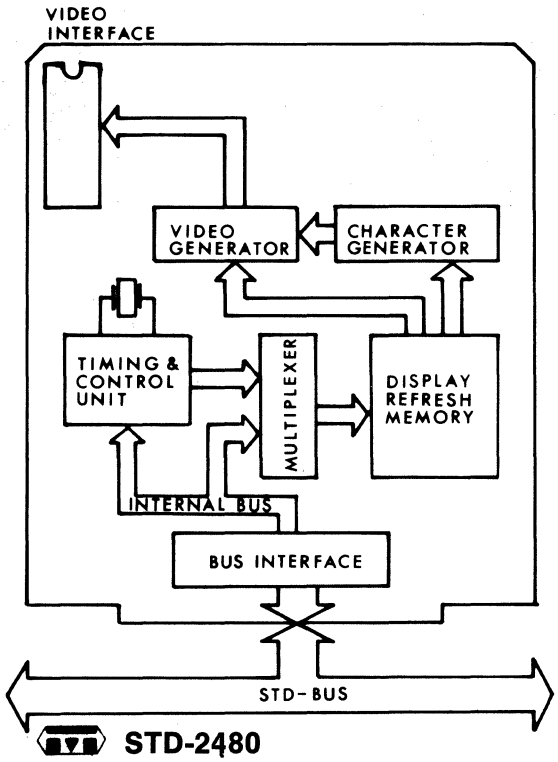



Figure 1. STD-2480 block diagram

**FUNCTIONAL DESCRIPTION**
The STD-2480 is made up of five major operational blocks: Timing and Control Unit, Display Memory, Character Generator, Video Generator, and Bus Interface. Communications between these blocks are shown in figure 1.

**TIMING AND CONTROL UNIT**
All timing and control signals required to generate a video display with 24 lines of 80 characters per line are supported on-board the STD-2480. The Timing and Control Unit, consisting of the master oscillator (11 MHz) and various modulo counters, produces the horizontal and vertical sync signals needed by the monitor as well as all timing signals for display refresh memory (RAS, CAS).

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted through a bidirectional port, from an external sync source. In this way the STD-2480 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The STD-2480 contains 2K bytes of on-board display refresh memory, to store up to 24 lines of 80 characters (1920 characters). The display memory occupies 4K bytes of system address space thereby permitting the CPU to identify each character location with a unique 12 bit address.

Each character position on the CRT screen corresponds to an 8 bit location in the display refresh memory. Characters are written on to the display by loading the ASCII Character Code to the appropriate display memory location. The CPU can read/write the display memory at full speed using all memory reference instructions.

All accesses to the display memory are controlled by a "Transparent Memory" control circuit within the Timing and Control Unit. In this way all accesses to the display memory (read, write, refresh) are efficiently arbitrated. The Transparent Memory control circuitry permits the CPU to read or write the refresh memory at any time and the display is free of glitches.

**CHARACTER GENERATOR**
The STD-2480 contains an on-board 2716 EPROM which contains the binary video information to generate a 128 character set. The supplied character font consists of the full 96 upper/lower case alphanumeric character set with the addition of 32 special graphic characters. The alphanumeric characters are formed in a 5 x 7 dot matrix within a 6 x 10 dot character cell. The graphics characters utilize the entire character cell to allow for drawing continuous lines.

The STD-2480 permits simple implementation of custom character fonts. To install a new character set, the user need only reprogram the EPROM character generator with the video information to generate his own font.

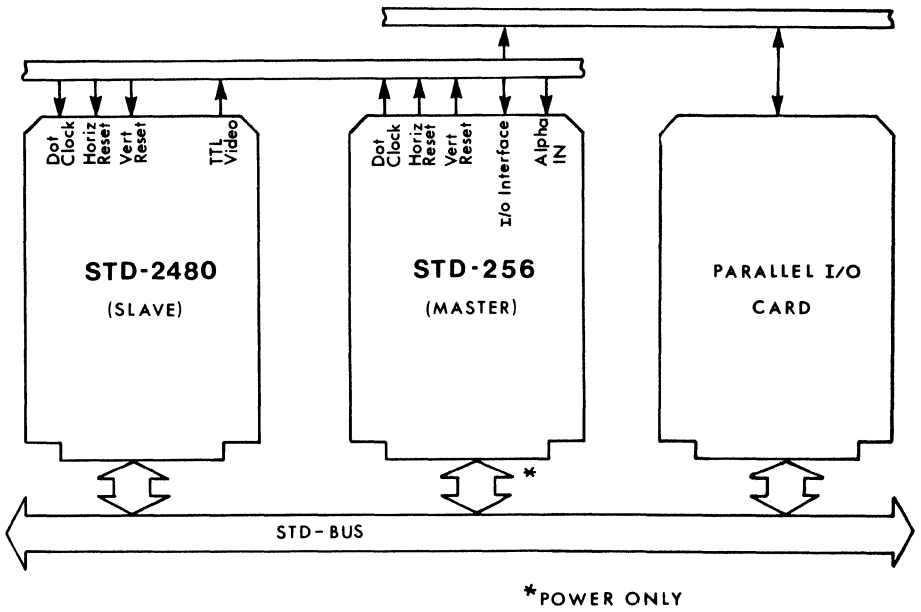



Figure 2. Combining STD-2480 and STD-256 cards for alpha/graph displays



**ATTRIBUTES**
Each character is accessed by seven bits of the eight bit ASCII Character Code. This releases the most significant eighth bit for attribute selection. Characters displayed on the STD-2480 can be displayed either as normal (white on a black background), inverted (black on a white background), blinking, or both inverted and blinking. Character attributes are selected by on-board hardware straps and are enabled/disabled by the eighth bit of the character code.

The on-board character generator can be strapped to generate a reduced 64 upper case only character set. In this configuration an extra bit from the character code is released. These two surplus bits can be used to independently enable/disable the two character attributes.

**VIDEO GENERATOR**
The STD-2480 can directly drive any standard monochrome video monitor. Composite video signals as well as separate TTL level video, horizontal/vertical sync and blanking signals are supported on-board.

**BUS INTERFACE**
The STD-2480 plugs directly into the STD-bus. The display refresh memory, which is memory mapped into the STD-bus memory address space, can be strapped to reside at any 4K byte memory address boundary between 0000H and FFFFH.

**GRAPHICS**
The STD-2480 can be integrated as an alphanumeric controller, within a complete alpha/graph video system. By configuring the STD-2480 to operate in the slave mode, the horizontal/vertical reset lines and the dot clock line are set to act as input ports. In this way the board can be synchronized to a master sync source. These lines can also be configured to operate as output ports to enable the user to configure his system to synchronize to the STD-2480. A typical application of combined alphanumerics/graphics is shown in figure 2, where the graphics board (STD-256) acts as the master sync source.

**PROGRAMMING**
The STD-2480 operational status (American/European compatibility, Master/Slave operation, base address, etc) is programmed via on-board hardware straps. Table 1 outlines the definitions of these straps.

| JUMPER NO. | DESCRIPTION |
|---|---|
| W 1,2 | Select Master/Slave mode |
| W 3,4,5,6,19,20,21,22 | Select base address |
| W 7,8,9,10,11,12 | Select character attributes |
| W 13,14,15,16,17,18,23,24,27,28 | Select American/European TV standard |
| W 25,26 | Enable/disable external sync to output video |

Table 1. Jumper definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

With Transparent Memory Access: 800ns
Without Transparent Memory Access: 500ns

### DISPLAY PARAMETERS

| DESCRIPTION | DISPLAYED |
|---|---|
| Resolution | 1920 characters |
| Horizontal Characters | 80 characters |
| Vertical Lines | 24 lines |
| Character Cell Size | 6 horizontal dots x 10 vertical dots |

### VIDEO TIMING

To generate a video display of 24 x 80 characters with a 6 dot wide character cell, the STD-2480 uses an 11.06688 MHz crystal. The following table gives the video timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 43.0 μs | 43.0 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 4.4 μs | 4.4 μs |
| Vertical Sync Frequency | 60.0 Hz | 50.2 Hz |
| Vertical Sync Width | 192.0 μs | 190.0 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Drive
Vertical Drive
Composite Sync
Composite Video

### BUS INTERFACE

Address, data and control signals conform to Pro-Log STD-bus specifications
Control Registers and Display Memory — Selectable on any 4K byte memory address boundary 0000H — FFFFH (4000H)

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1 : 56 pin edge connector — Bus Interface | ANSLEY 609-561 5M |
| J1 : 16 pin DIP socket — Video Interface | AUGAT 516-A6-37D |

### PHYSICAL

**SIZE**

Width: 4.50 in. (11.43 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+5V DC ±5% @ 0.8A

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

STD-2480 — XX

- AS — American standard (60 Hz)
- ES — European standard (50 Hz)

Example: STD-2480-AS: 24 x 80 character display with a vertical refresh rate of 60 Hz.

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

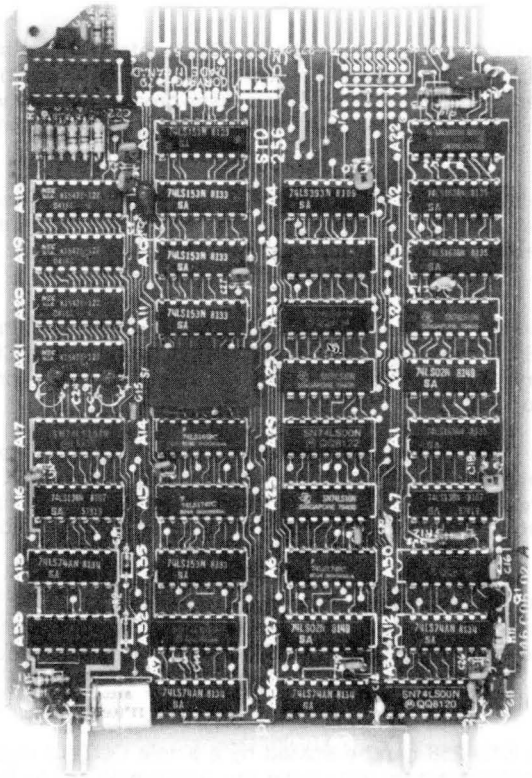
# STD-256

## 256 x 256 GRAPHICS DISPLAY CONTROLLER FOR STD-BUS

- **Displays 256 x 256 dot raster graphics**
- **Powerful X-Y addressing**
- **Single instruction memory erase**
- **Color/grey-scale expansion**
- **Can be combined with STD-2480**
- **STD-bus compatible**
- **Internal/external sync**
- **American/European operation**



The STD-256 is a complete graphics display controller on a single STD-bus plug-in board. It contains its own 65,536 bit refresh memory and TV sync and video generators. Each display dot (pixel) is addressable via X-Y Registers and can be either written to or read from. Three STD-256 cards can be combined to provide a full 256 x 256 x 8 color graphics display.



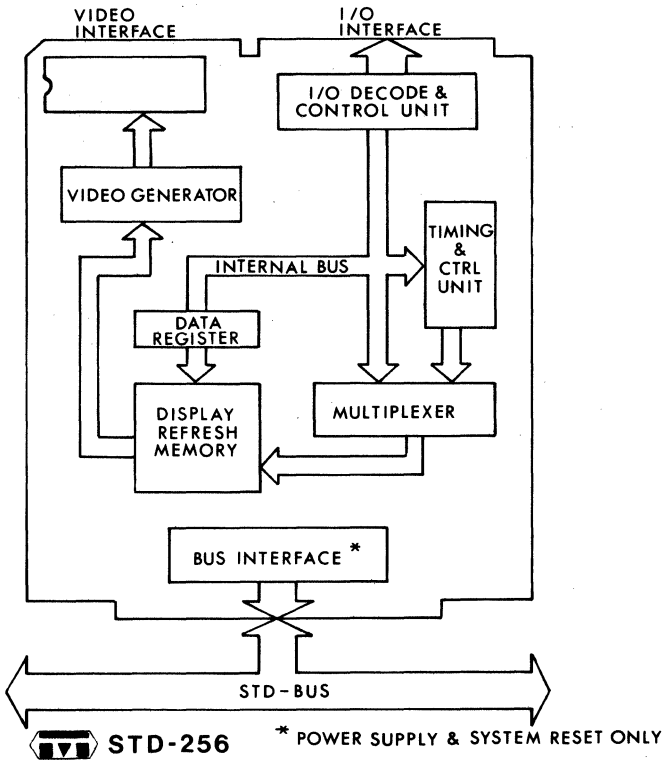



Figure 1. STD-256 block diagram

**FUNCTIONAL DESCRIPTION**
The STD-256 consists of five main functional blocks (figure 1): Timing and Control Unit, X-Y Registers, Display Memory, Video Generator, and Bus Interface.

**TIMING AND CONTROL UNIT**
All timing and control signals required by the video monitor (horizontal/vertical sync and blanking), display refresh memory (row/column addressing), and video generator (dot clock, load and shift) are generated by the Timing and Control Unit. The exact configurations of these signals are user-programmable, via hardware straps, to enable the STD-256 to generate displays with up to 256 horizontal dots by 256 vertical dots in either 50 Hz (European) or 60 Hz (American) systems.

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the STD-256 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The STD-256's display refresh memory is made up of 8K bytes of on-board dynamic RAM which contains the binary picture information for a 256 x 256 dot raster graphics display. Each point on the CRT screen is identified by a unique address within the display memory. When a point is to be illuminated on the screen, a logic "1" is written to the appropriate display memory location.

The CPU reads/writes the display memory through a pair of I/O locations (X-Y Registers). This allows two I/O locations to address all of the 65,536 bits of the refresh memory (256 x 256). Once the X and Y address of the dot has been loaded, the CPU can read/write the dot intensity. The dot intensity bit (image bit) can be assigned to any data bus bit. The resultant CRT display is a black and white image with the intensity of each dot being either on (logic "1") or off (logic "0").

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the STD-256 efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display is "transparent" to the user.

**SCREEN ERASE**
The entire refresh memory on the STD-256 can be erased by a single OUTput instruction. Setting the memory erase enable bit when writing to the display memory will cause the entire memory to be set to that intensity (0 = black, 1 = white).

**VIDEO GENERATOR**
The STD-256 works with all standard monochrome video monitors in American (60 Hz) and European (50 Hz) systems. TTL level video, horizontal sync, vertical sync, as well as composite video signals are supported on-board.

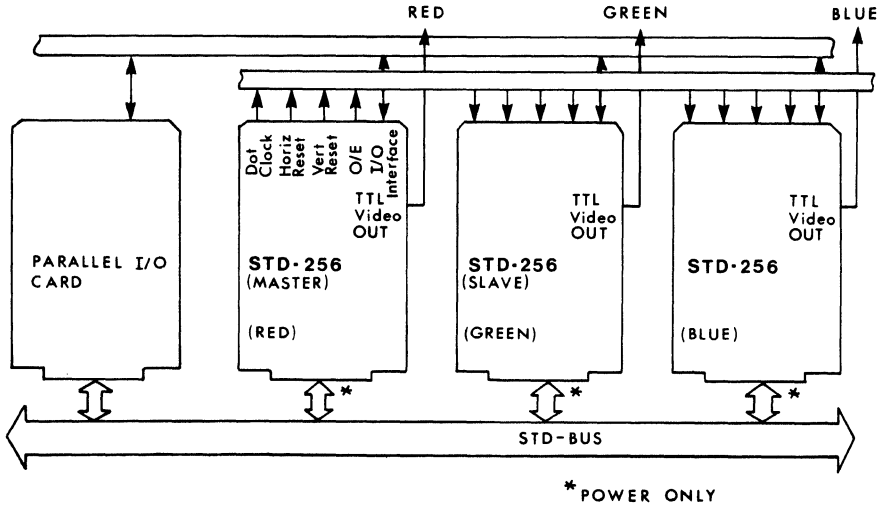



Figure 2. "Stacking" STD-256 cards for 8 level color/grey scale displays

**BUS INTERFACE**
The STD-256 plugs directly into the STD-bus. The card uses four eight bit ports for control, data, and X and Y addressing.

A parallel I/O card such as the Mostek MDX-PIO or the Prolog 7601 is required to provide data bus buffering for the STD-256. Up to six STD-256 cards can be supported by a single interface card.

**ALPHA/GRAPH DISPLAYS**
The STD-256 can be combined with the STD-2480 to generate alphanumeric/graphic displays. An on-board alphanumeric input port accepts the TTL level alphanumeric video information from the STD-2480 and combines it with the graphics video from the STD-256. The result is a powerful display combining both alphanumerics and graphics without the overhead involved in generating alphanumeric characters using graphic techniques.

**COLOR/GREY-SCALE EXPANSION**
Multiple STD-256 boards can be "stacked" to provide for sophisticated color or grey-scale applications that require more bits per pixel. Up to 24 STD-256 boards may be combined in this way to provide up to 24 bits/pixel (over 16 million colors).

**PROGRAMMING**
The STD-256 can be programmed for American/European standard operation via a series of on-board hardware straps. Additional straps are provided to program the board to operate in either master or slave mode and to set the boards base address.

| JUMPER | DEFINITION |
|---|---|
| W1 | Select master/slave operation |
| S1 1 | Enable video software control |
| 2 | Disable video software control |
| 3 | Select European/American operation |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | |
| P3 jumper matrix | Locate data input/output lines |

Table 1. Jumper definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μs

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTION |
|---|---|
| Horizontal Resolution | 256 dots max. |
| Vertical Resolution | 256 dots displayed max. (50 Hz), 240 dots displayed max. (60 Hz) |

### VIDEO TIMING

The STD-256 generates a display of 256 horizontal dots by 256 vertical dots using an 11.06688 MHz crystal. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 45.6 μs | 45.6 μs |
| Horizontal Sync Frequency | 15.7 KHz | 15.7 KHz |
| Horizontal Sync Width | 5.60 μs | 5.60 μs |
| Vertical Sync Frequency | 60.0 Hz | 50.0 Hz |
| Vertical Sync Width | 240.0 μs | 240.0 μs |

4

### OUTPUT SIGNALS

TTL Level Video
Horizontal Sync
Vertical Sync
Composite Sync
Composite Video

### BUS INTERFACE

Four 8-bit ports must be interfaced to the STD-bus via a Mostek or Prolog parallel I/O card. The STD-256 takes only power and reset directly from the bus.

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1 : 56 pin edge connector — STD-Bus Interface | ANSLEY 609-5615M |
| P3 : 56 pin edge connector — I/O Interface | ANSLEY 609-5615 |
| V : 16 pin DIP socket — Video Interface | AUGAT 516-A6-37D |

### PHYSICAL

**SIZE**

Width: 4.48 in. (11.38 cm)
Height: 6.50 in. (16.51 cm)
Depth: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+5V DC ±5% @ 400 mA
+12V DC ±5% @ 100 mA

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

STD-256 — XX

- AS — American standard (60 Hz)
- ES — European standard (50 Hz)

Example: STD-256-AS: 256 x 256 graphics display with a vertical refresh rate of 60 Hz.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# STD-800

## HIGH RESOLUTION COLOR GRAPHICS BOARD FOR STD-BUS

- **Display resolution up to 800 x 600 x 4**
- **16 colors selectable from a palette of 4096**
- **System expansion capabilities allow up to 12 bits/pixel (4096 simultaneously displayable colors)**
- **VLSI graphics processor (7220) draws vectors, arcs, circles, rectangles, and characters**
- **Split-screen, pan, and scroll**
- **Analog RGB video outputs**
- **Single +5V supply**
- **Supports DMA transfers**
- **Light pen support**
- **50/60 Hz interlaced or non-interlaced operation**



The Matrox STD-800 is a powerful color graphics display controller board for the STD-bus. Complex graphic images can be created on the STD-800 with resolutions ranging from 256 x 256 x 4 to 800 x 600 x 4.

The STD-800 recognizes an instruction set of 19 commands. These instructions enable the user to create displays with minimal host intervention or calculational overhead. Instructions include: defining video parameters, draw a line, draw an arc, draw a circle, draw a rectangle, draw a character, pan, and scroll. Area fills and pixel blink are also supported.

AVAILABLE
4th QUARTER
1983

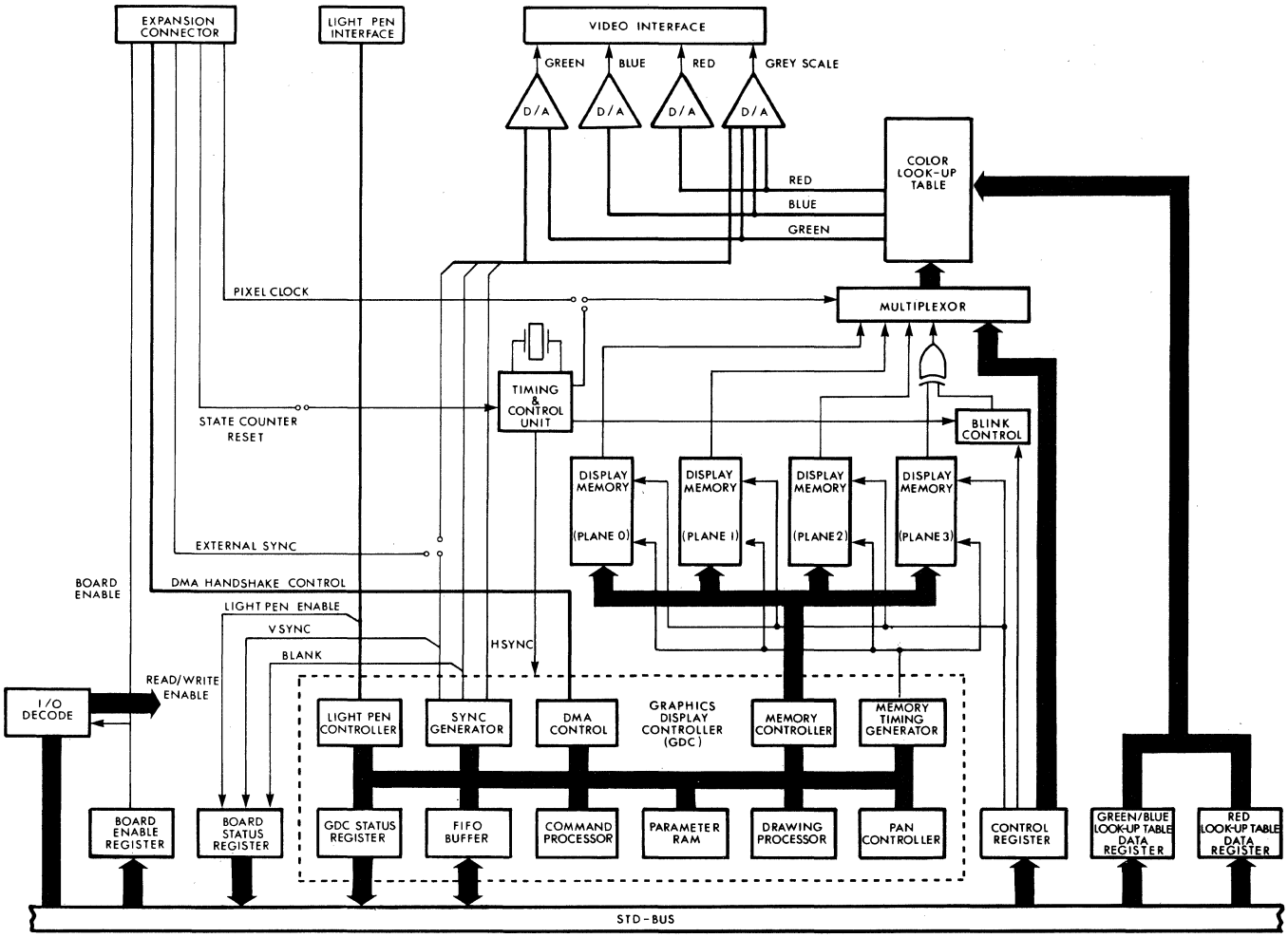



Figure 1. STD-800 block diagram

## STD-800 FEATURES

**Read/Write Area:** Read/write memory is 128K bytes (with 64K RAMs) expandable to 512K bytes (with 256K RAMs)

**Standard Resolution:** 512 x 512 interlaced or non-interlaced (512 x 480 with 60 Hz vertical refresh rate)

**User Selectable Resolutions:** 256 x 256 x 4 to 800 x 600 x 4 resolutions can be programmed by the user. Note that some resolutions will require crystal and/or RAM part changes.

**Bits/Pixel:** 4 bits/pixel (expandable to 12 bits/pixel)

**Blink:** Selected areas of the graphics display can be set to blink between any two predefined colors. The blink frequency is set at 1.8 Hz.

**Split Screen:** The display screen can be split horizontally into two independent image areas. The size of each area is software programmable.

**Pan:** Each image area can be horizontally panned, inside the read/write area, by multiples of 16 pixels.

**Scroll:** Smooth vertical scroll by one line resolution on either image area.

**Graphics Instructions:** The STD-800 understands 19 graphics instructions.

**Figure Generation:** Graphics primitives, such as lines, arcs, circles, and rectangles are drawn by the STD-800 using single instructions.

**Characters:** Any character can be defined by the user and then drawn by the STD-800 using a single instruction.

**Draw Speed:** 1.6 μsec./pixel/plane minimum; includes vectors, arcs, circles, rectangles, and character draws.

**DMA Data Transfers:** The STD-800 supports DMA handshaking for high speed image transfers.

**Video Parameters:** All video parameters including horizontal and vertical syncs, blanking, frequency, and display format are user software programmable.

**Light Pen:** On-board register latches deglitched light pen position. Interface built-in.

**Video Outputs:** R,G,B color signals $1V_{p\text{-}p}$ into 75Ω, sync can be either composite on green or supplied as a separate signal.

**STD-Bus Interface:** The STD-800 plugs directly into the STD-bus and looks to the host like five I/O registers.

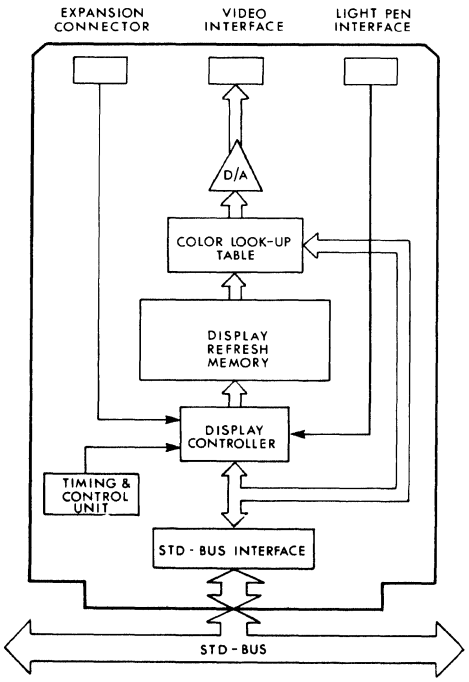



Figure 2. STD-800 functional blocks



## FUNCTIONAL DESCRIPTION

The STD-800 is a powerful, high resolution, graphics controller contained on a single STD-bus PC board (4.5" x 6.5"). The STD-800 contains four major subsections (figure 2): the Graphics Display Controller, the Display Refresh Memory, the Color Look-up Table, and the STD-bus Interface.

| CATEGORY | COMMAND | FUNCTION |
|---|---|---|
| Video Control | RESET | Reset the GDC to its idle state and specifies the display format. |
| | SYNC | Specifies the display format. |
| | VSYNC | Selects master or Slave video synchronization mode. |
| | CCHAR | Specifies the cursor and character row height. |
| Display Control | START | Starts the display scanning process. |
| | STOP | Blanks the display. |
| | CURS | Sets the position of the cursor in the display memory. |
| | PRAM | Defines the starting addresses and length of the display areas and specifies the eight bytes for the graphics character. |
| | PITCH | Specifies the width of the X dimension of the display memory. |
| Drawing Control | WDAT | Writes data words or bytes into the display memory. |
| | MASK | Sets the mask register contents. |
| | FIGS | Specifies the parameters of the drawing process. |
| | FIGD | Draws the figure as specified by FIGS. |
| | GCHRD | Draws the graphics character into the display memory. |
| Data Read | RDAT | Reads data words or bytes from the display memory. |
| | CURD | Reads the cursor position. |
| | LPRD | Reads the light pen address. |
| DMA Control | DMAR | Requests a DMA read transfer. |
| | DMAW | Requests a DMA write transfer. |

Table 1. STD-800 instruction set

## DISPLAY MEMORY

The STD-800 contains 16 64K bit RAM chips, on-board, for a total display read/write memory of 1,042,176 bits (128K bytes). This memory area is divided into 4 bit planes (allowing up to 16 simultaneously displayable colors or grey levels) and can be configured, by the user, into a three dimensional array of up to 512 horizontal x 512 vertical pixels x 4 bits/pixel. The resolution capabilities of the STD-800 can be increased by sacrificing bit planes. This feature enables the user to configure the on-board read/write memory for 800 x 655 x 2 bits/pixel. By using 256K x 1 RAMs, a 512K byte display refresh memory can be implemented and read/write arrays of up to 800 x 655 pixels can be configured, with 4 bits/pixel.

## DISPLAY CONTROLLER

An on-board VLSI display controller chip is the heart of the STD-800. All of the display maintenance requirements (horizontal/vertical syncs and blanking) and the display memory refresh functions are provided by the Display Controller and are completely transparent to the user. Much of the low level display memory addressing is off-loaded from the host processor, by the Display Controller, reducing software overhead and increasing system throughput.

The STD-800 Display Controller recognizes a 19 instruction set, which simplifies programming of the display. The instruction set is divided into five major categories (Video Control, Display Control, Drawing Control, Data Read, and DMA Control) and are shown in table 1.

**Display Organization** — The on-board Display Controller allows the user to configure the display memory for any display resolution format, so long as that format does not exceed the total available memory (128K bytes standard). The standard STD-800 can be configured for displays of 256 x 256, 512 x 256, 512 x 384, or 640 x 400 pixels with 4 bits per pixel, or 640 x 480 or 800 x 600 pixels using 2 bits/pixel. Optionally, using 256K RAMs, displays of up to 640 x 480 or 800 x 600 pixels by 4 bits/pixel can be programmed.

The Display Controller also generates all of the timing signals required by the CRT monitor (figure 3). These signals (horizontal sync, horizontal blanking, vertical sync, and vertical blanking) are user definable to allow the STD-800 to drive any analog RGB or monochrome video monitor. Sync frequencies

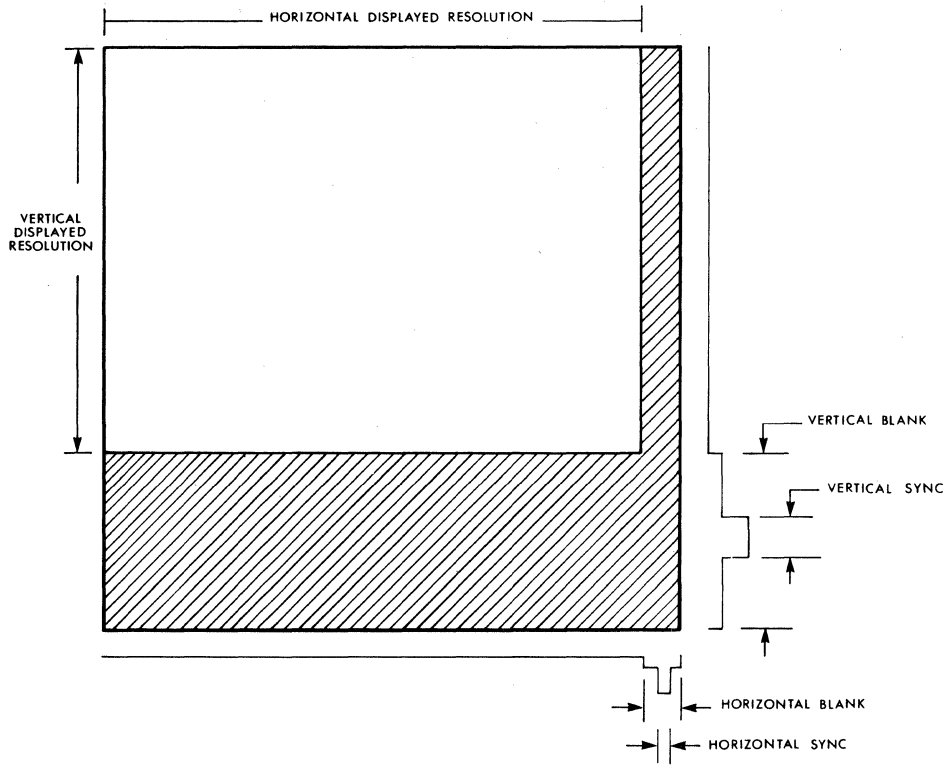



Figure 3. Display format parameters

can be defined to operate the system in either 50 Hz European or 60 Hz American Standard environments (interlaced or non-interlaced).

**Pan and Scroll** — The STD-800 allows the user to pan and/or scroll the generated graphics display. When using a small display format (i.e. 256 x 256 or 512 x 256) some of the available read/write display memory is not viewed on the screen. This "hidden" memory can be viewed by moving the CRT screen's "window" of the display memory either vertically or horizontally. Scrolling is accomplished on a line basis, for a "smooth" vertical image shift, while horizontal panning is done on 16-bit word boundaries.

**Split-Screen** — The CRT screen area can be divided into two, horizontally separate, independent display areas. The length of each area is independently user definable up to full screen. Note that the sum of the length of the two display areas can not exceed the total available screen area. Each display area can also be independently scrolled and/or panned.

**Figure Drawing** — The STD-800 features an ability to draw various graphics primitives with little or no assistance from the host CPU. Lines, arcs, circles, and rectangles can be constructed on the display by simply passing the figure's parameters to the STD-800. Calculation and generation of the addresses of the pixels, that make up the figure, are performed internally to the STD-800 and are transparent to the user. Rectangular area fills are also easily implemented using the STD-800.

The "texture" of the displayed figure (i.e. solid, dashed, or dotted) and the pattern of the area fill are also user programmable. The figure texture is defined by the user specified 16-bit texture pattern (figure 4) which represents those pixels, along the figure, which can be modified. A "1" in the texture pattern register will determine if the corresponding display memory bit is modified. The effect of writing to the display memory can produce one of four results, (replace, complement, set, or clear), selectable by the programmer. The Replace mode of writing to the display memory rewrites the contents of the memory with the contents of the texture register. Other writing modes available on the STD-800 allow the programmer to complement those bits in the display memory which correspond to 1s in the texture register, set the "modify-enabled" bits, or clear these bits. Likewise, the area fill pattern can be set by defining an 8 x 8 recurring matrix.

Characters can also be drawn to the graphics display, in any position and orientation, with a minimum of host CPU overhead. A character is drawn by first downloading an 8 x 8 pattern matrix, for that character, to the STD-800. Upon receipt of a character draw command, the GDC will then draw the character, pixel by pixel, to the display memory at the cursor position. Using this technique, any character (upper/lower case alphanumerics or special graphics symbol) can be drawn to the display.

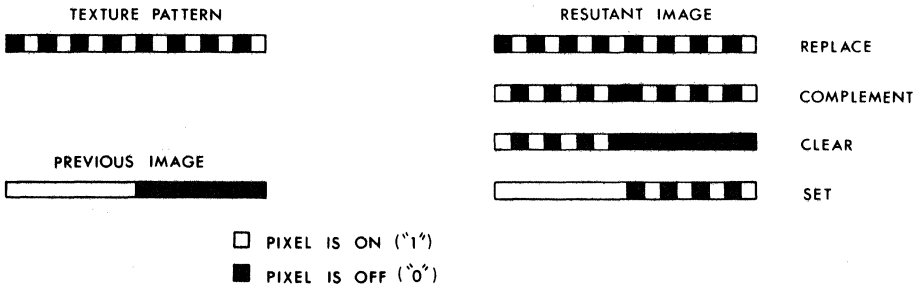



Figure 4. STD-800 "texture" pattern control

**DMA** — The STD-800 supports DMA data transfers to and from the display refresh memory. DMA Request and Acknowledge handshaking lines are provided, on a 10-pin Expansion connector, to permit direct communications between the STD-800 and an external DMA controller. This feature is useful in storing and/or loading entire images to/from disk.

### BLINK

Selected areas of the graphics image generated by the STD-800 can be set to blink, under software control, at a blink rate of 1.8 Hz. Setting the Blink Enable bit in the on-board Control Register causes any image data stored on bit plane 3 to toggle between two colors. The colors, from which and to which this data will blink, are defined by the user when the color look-up table is loaded.

### COLOR LOOK-UP TABLE

The STD-800 contains an on-board color look-up table which looks, to the user, like a 16 x 12 bit RAM. Through this look-up table, displays with up to 16 colors can be accomodated; with the displayed colors being user selected from a palette of 4096 colors. The color look-up table can be rewritten at any time.

The color look-up table allows the user to create a wide variety of video effects. Manipulation of the color look-up table allows the generation of such high performance effects as animation.

### TIMING AND CONTROL UNIT

The STD-800 contains an on-board 20 MHz clock which is the heart for the module's Timing and Control Unit. The Timing and Control Unit, using the 20 MHz crystal together with a pair of PALs* (Programmable Array Logic), supplies all of the individual functional blocks of the STD-800 with their required timing inputs and synchronizes their operation for maximum throughput. This proprietary Matrox circuit also enables the STD-800 to generate displays of up to 800 x 655 x 4 bits per pixel using an average drawing speed of 1.6 $\mu$sec./pixel. Optional 10.0, 11.66, and 13.33 MHz crystals are available, together with on-board strap-selectable divide by 2 and divide by 4 circuitry, to enable the STD-800 to accomodate video timing parameters for display formats ranging from 256 x 256 to 800 x 600 (see SPECIFICATIONS).

### VIDEO INTERFACE

The output video signals are supplied, via a 10-pin header on the module, as analog ($1V_{p\text{-}p}$) RGB signals (figure 5). Sync signals are provided either combined with the Green video output or as a separate composite signal.

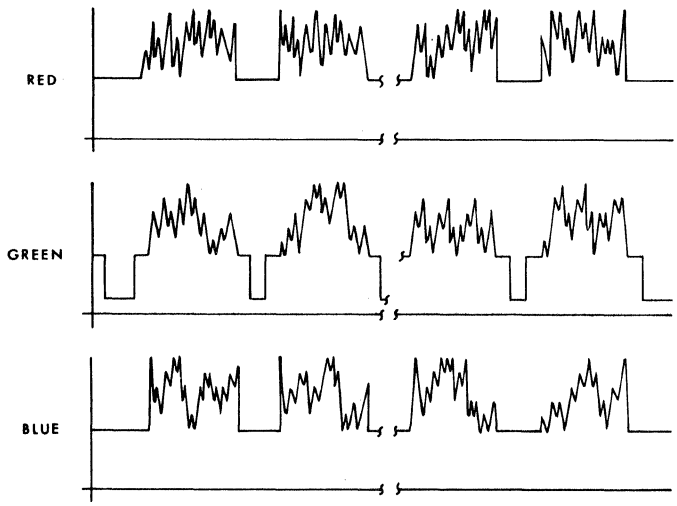



Figure 5. STD-800 video output signals

### LIGHT PEN INTERFACE

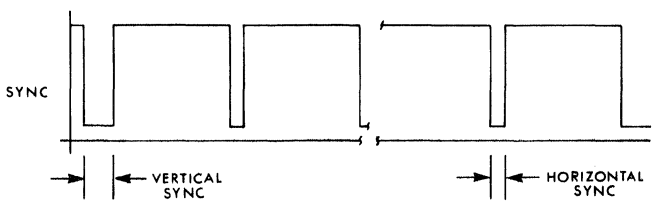
User interaction with the display is enabled through a light pen interface. The STD-800 latches the address of the word, pointed to by the light pen, and makes this information available to the host processor. An interrupt is generated on-board the STD-800 which can signal the host processor that light pen data is available. A "blue flood" feature is incorporated on the STD-800 to facilitate the use of a light pen. The light pen is interfaced to the STD-800 via a 10-pin right angle header.

### STD-BUS INTERFACE

The STD-800 interfaces directly to the STD-bus and meets all STD-bus specifications as laid out in the Mostek-Prolog STD-bus specification. To the host computer, the STD-800 looks like a group of six 8-bit registers which can be strapped to any 8-byte block of I/O address space. Reading locations 0 and 1, will read the Display Controller's Status and FIFO Read buffer respectively (table 2). Writing to these locations will transfer either a command byte (location 1) or a parameter byte (location 0) to the STD-800 FIFO. Writing to I/O port 2 (Control Register) sets various control parameters for the board, i.e. Blue Flood Enable and Blink Enable, and also loads the address for the next Color Look-Up Table write instruction. Reading this port allows the user to monitor the status of the Light Pen Enable signal and the Horizontal Blank. The remaining three registers are used to write the Color Look-Up Tables and enable read/write accesses to the board (Board Enable Register). The Board Enable Register allows strapping of up to three STD-800 boards within the same address space. By enabling or disabling access to the board, each board can be accessed individually or all three at the same time.

### PROGRAMMING

The STD-800 simplifies the programmer's task in generating a graphics display by performing much of the calculational overhead involved in producing a graphics image. All of the repetitive, low-level accesses to the display memory (pixel, addresses) are handled internally to the STD-800. The programmer, then, creates the graphics image as a combination of graphics primitives (lines, arcs, circles, etc). These primitives are invoked by passing the appropriate instruction to the STD-800 accompanied by the necessary parameters (eg. to draw a line the parameters required include the direction of the vector, the length of the vector, etc.). An on-board 16 byte FIFO instruction buffer allows the programmer to pipeline commands for greater system throughput.



| ADDRESS | READ | WRITE |
|---|---|---|
| Base + 0 | Read Status Register | Write Parameter into FIFO Buffer |
| Base + 1 | Read FIFO Command Buffer | Write Command into FIFO Buffer |
| Base + 2 | Read Board Status | Write Control Register |
| Base + 4 | Not Used | Write Color Look-Up Table (Green and Blue) |
| Base + 5 | Not Used | Write Color Look-Up Table (Red) |
| Base + 6 | Not Used | Board Enable Register |

Table 2. STD-800 register definitions.

## USER DEFINABLE RESOLUTIONS

The display format, used by the STD-800, is initialized by writing a Reset command (see table 1) to the board's FIFO command buffer, followed by eight bytes of video format parameter data. The desired format is expressed by defining the number of horizontally displayed dots (expressed as an integer number of 16-bit words), the number of vertically displayed lines, and the horizontal and vertical sync parameters (front and back porch widths, and sync signal widths). Also included as a Reset parameter is an 8-bit Mode of Operation descriptor which defines whether the resultant display will be interlaced or non-interlaced, and whether drawing will be restricted to retrace only or allowed to occur at any time. A Sync command is also recognized by the STD-800 and can be used, followed by the same parameter bytes as the Reset command, to dynamically change the display format without reinitializing the board. The Sync command can also be used alone (with no parameter bytes) to blank the screen for "all time" drawing (drawing can occur during active video as well as during retrace blanking). Note that "all time" drawing may result in streaking on the display.

Another command (PRAM), followed by up to 16 bytes of parameters, is used to define the starting address and length of the image areas on the display (up to two independent display image areas can be maintained by the STD-800). The PRAM parameters also define the 16-bit vector "texture" pattern and the 8 x 8 character (or area fill) pattern.

## SYSTEM EXPANSION

Two or three STD-800 boards can be synchronized together to provide 8 bits (two boards) or 12 bits (three boards) per pixel. In the case of a two board system, one board provides the drives for two guns; each with four colors from a palette of 4096. The second board provides the drives for the third gun with 16 colors from the 4096 palette. If three boards are used, each board drives drives one gun with 16 possible intensities per gun. The total number of displayable colors in such a system is 4096.

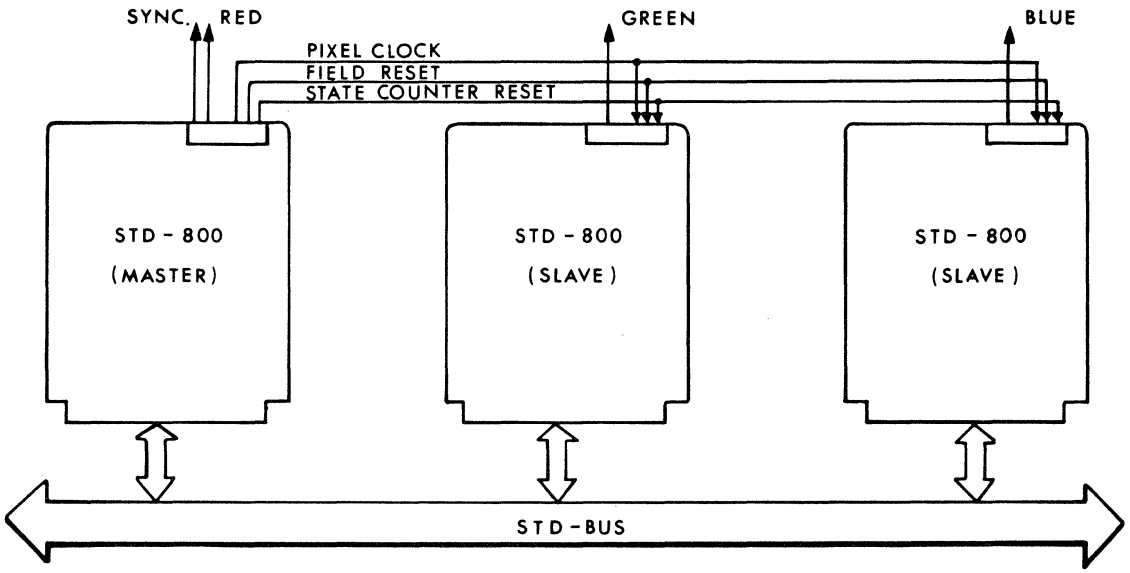



Figure 6. Combining STD-800 boards for 12 bits/pixel.

# SPECIFICATIONS

## FUNCTIONAL

### DISPLAY PARAMETERS

| ON-BOARD RAM | READ/WRITE AREA | RESOLUTION | BITS/PIXEL | CLOCK FREQUENCY | |
|---|---|---|---|---|---|
| | | | | INTERLACED | NON-INTERLACED |
| 128K | 512 x 512 | 256 x 256 | 4 | — | 5.8 MHz |
| 128K | 512 x 512 | 512 x 256 | 4 | — | 11.6 MHz |
| 128K | 512 x 512 | 512 x 384 | 4 | 10.0 MHz | 20.0 MHz |
| 128K | 512 x 512 | 512 x 480 | 4 | 10.0 MHz | 20.0 MHz |
| 128K | 640 x 400 | 640 x 400 | 4 | 13.3 MHz | 20.0 MHz |
| 128K | 800 x 655 | 640 x 480 | 2 | 13.3 MHz | — |
| 128K | 800 x 655 | 800 x 600 | 2 | 20.0 MHz | — |
| 512K | 1024 x 1024 | 640 x 480 | 4 | 13.3 MHz | — |
| 512K | 1024 x 1024 | 800 x 600 | 4 | 20.0 MHz | — |

Note 1: To obtain 640 x 480 x 4 or 800 x 600 x 4 display resolution, 256K RAM parts must be used.
Note 2: Divide by 2 and divide by 4 circuitry is included for obtaining the given clock frequencies using standard crystal oscillators.

4

### VIDEO TIMING

For a display format of 512 horizontal dots x 384 vertical lines, the following video parameters must be programmed. The table gives the parameters for both American and European systems using either Interlaced or Non-Interlaced Video formats.

| | AMERICAN | | EUROPEAN | |
|---|---|---|---|---|
| | INTERLACED | NON-INTERLACED | INTERLACED | NON-INTERLACED |
| Active Video | 51.2 μs | 25.6 μs | 51.2 μs | 25.6 μs |
| Horizontal Sync Frequency | 16.02 KHz | 28.4 KHz | 16.02 KHz | 28.4 KHz |
| Horizontal Sync Width | 6.4 μs | 3.2 μs | 6.4 μs | 3.2 μs |
| Vertical Sync Frequency | 30.01 Hz | 60.06 Hz | 25.04 Hz | 50.01 Hz |
| Vertical Sync Width | 249.6 μs | 105.6 μs | 249.6 μs | 105.6 μs |

### INPUT SIGNALS

Light Pen Enable
Light Pen Strobe

### OUTPUT SIGNALS

Analog Video: Red
Green (composite)
Blue
Composite Sync

Expansion: Pixel Clock
State Counter Reset
Frame Reset
Board 1 Enable
Board 2 Enable
Board 3 Enable
DMA Request
DMA Acknowledge

### BUS INTERFACE

Address, data, and control lines conform to the Mostek-Prolog STD-bus specification
Command and Status Registers — Selectable on any 8 byte I/O address boundary — 00 — FFH
— Detailed information on the STD-800 command set is available in the 7220 GDC manual.

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 56-pin edge connector — STD-bus Interface | Ansley 609-561-5M |
| J1: 10-pin header — Video Interface | AMP 89722-1 |
| J2: 10-pin header — Light Pen Interface | Molex 15-25-5103 #4700 |
| J3: 10-pin header — Expansion Connector | Molex 15-25-5103 #4700 |

## PHYSICAL

### SIZE

Width: 4.5 in. (11.38 cm)
Height: 6.5 in. (16.51 cm)
Depth: 0.5 in. ( 1.27 cm)

### POWER REQUIREMENTS

+5V DC ±5% @ 1.8A (STD-800/64)
+5V DC ±5% @ 2.5A (STD-800/256)

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0°C to 55°C
Relative Humidity: 0 — 95% non-condensing

## ORDERING INFORMATION

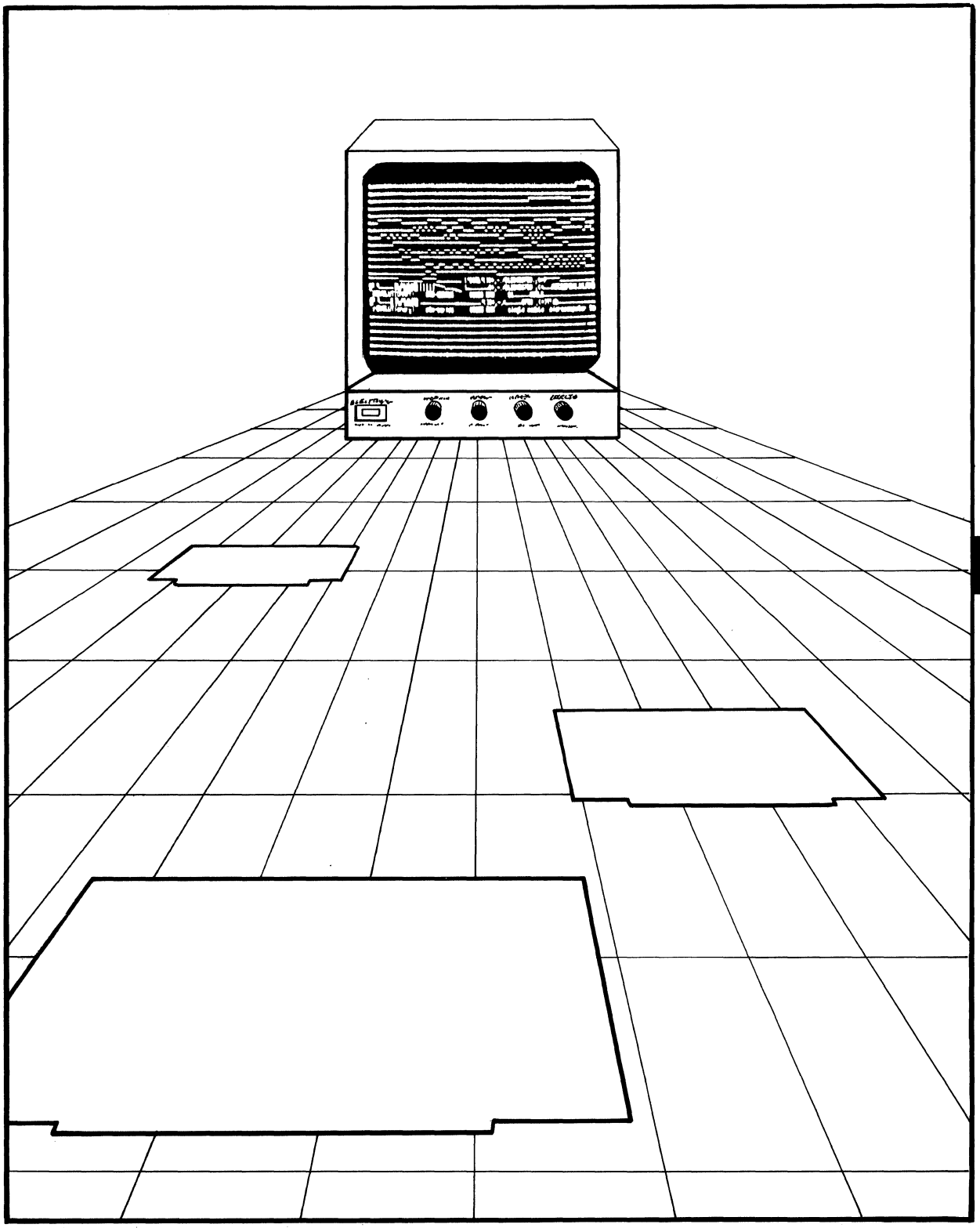
STD-800 / XXX — High resolution color graphics board (uses 20 MHz crystal)

- 64 — uses 64K RAMs
- 256 — uses 256K RAMs

## SUPPORT PRODUCTS

| | |
|---|---|
| XTAL | 10.000 MHz |
| XTAL | 11.666 MHz |
| XTAL | 13.333 MHz |

4



5

# S-100 BUS VIDEO BOARDS

## SECTION 5 S-100 BUS VIDEO BOARDS



5

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# ALTR-2480

## 24 x 80 ALPHANUMERIC DISPLAY CONTROLLER FOR S-100 BUS

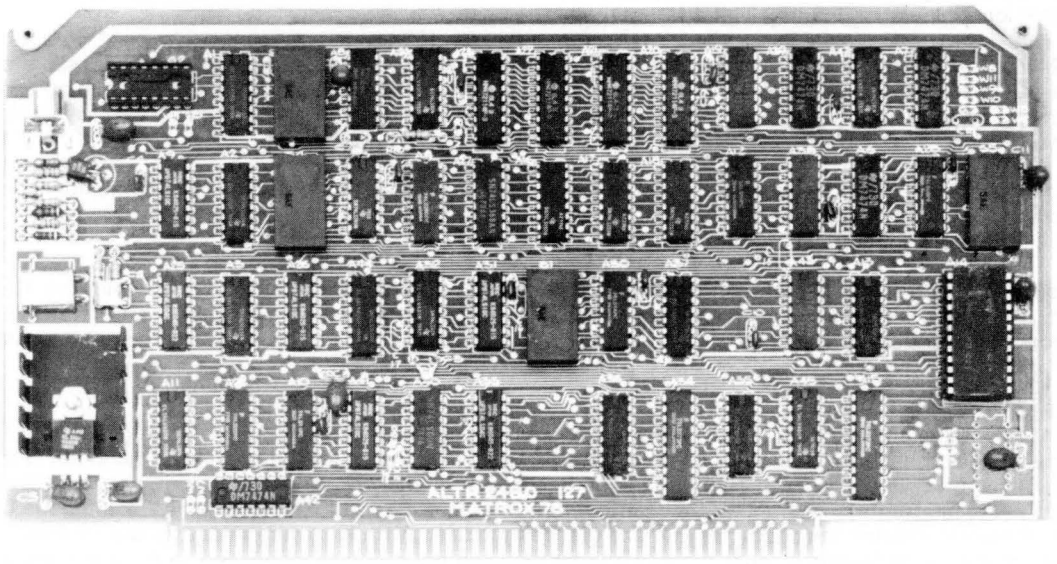
- **24 row x 80 column alphanumeric video display**
- **4K byte memory mapped display**
- **Normal, inverse, blink attributes**
- **EPROM ASCII character generator**
- **Transparent memory access**
- **S-100 bus compatible**
- **Directly drives any monochrome monitor**
- **Alpha/graph expansion**
- **External/internal sync capability**
- **American/European operation**

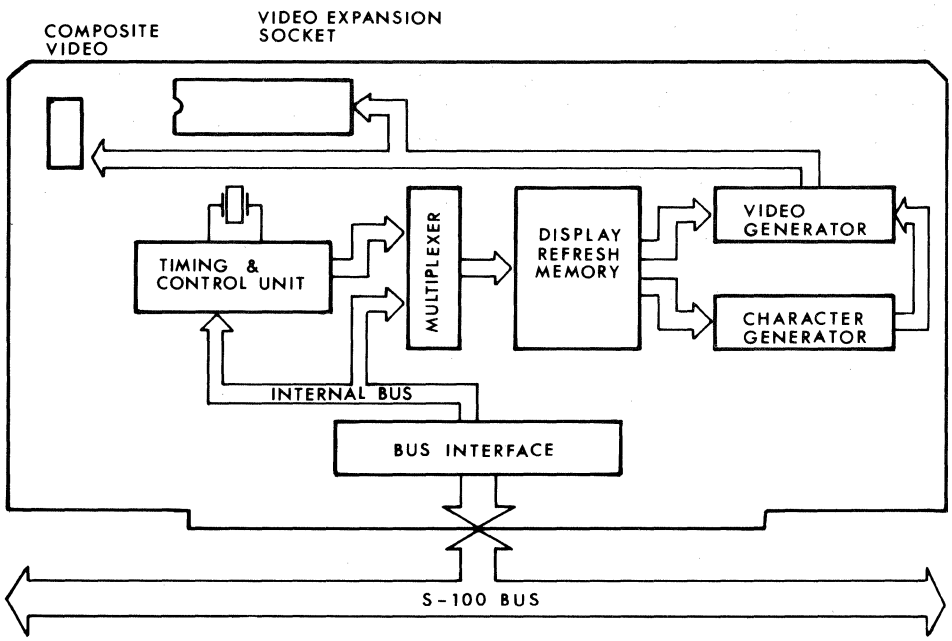
5

The ALTR-2480 is an S-100 bus compatible alphanumeric display controller which is capable of generating displays of 24 lines of 80 characters per line. Characters can be displayed as either white on a black background or black on a white background. Each character can also be set to blink under software control.

The character font provided with the ALTR-2480 contains 128 - 5 x 7 upper/lower case alphanumeric characters and graphic symbols. The character generator is user-programmable, allowing the user to implement his own custom character font.

The ALTR-2480 works with all standard monochrome video monitors in Europe (50 Hz) and America (60 Hz).






ALTR-2480

Figure 1. ALTR-2480 block diagram

**FUNCTIONAL DESCRIPTION**
The ALTR-2480 is made up of five major operational blocks: Timing and Control Unit, Display Memory, Character Generator, Video Generator, and Bus Interface. Communications between these blocks are shown in figure 1.

**TIMING AND CONTROL UNIT**
All timing and control signals required to generate a video display with 24 lines of 80 characters per line are supported on-board the ALTR-2480. The Timing and Control Unit, consisting of the master oscillator (11 MHz) and various modulo counters, produces the horizontal and vertical sync signals needed by the monitor as well as all timing signals for display refresh memory (RAS, CAS).

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the ALTR-2480 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The ALTR-2480 contains 2K bytes of on-board display refresh memory, to store up to 24 lines of 80 characters (1920 characters). The display memory occupies 4K bytes of system address space thereby permitting the CPU to identify each character location with a unique 12 bit address.

The ALTR-2480 can be strapped so that the display memory is arranged as two independently accessable pages. In this way the ALTR-2480 is capable of storing two displays of 24 x 40 characters, of which one display can be updated while the other is being displayed. An on-board Video Control Register allows the user to software select which page is to be displayed.

Each character position on the CRT screen corresponds to an 8 bit location in the display refresh memory. Characters are written on to the display by loading the ASCII Character Code to the appropriate display memory location. The CPU can read/write the display memory at full speed using all memory reference instructions.

All accesses to the display memory are controlled by a "Transparent Memory" control circuit within the Timing and Control Unit. In this way all accesses to the display memory (read, write, refresh) are efficiently arbitrated. The Transparent Memory control circuitry permits the CPU to read or write the refresh memory at any time and the display is free of glitches.

**CHARACTER GENERATOR**
The ALTR-2480 contains an on-board 2716 EPROM which contains the binary video information to generate a 128 character set. The supplied character font consists of the full 96 upper/lower case alphanumeric character set with the addition of 32 special graphic characters. The alphanumeric characters are formed in a 5 x 7 dot matrix within a 6 x 10 dot character cell. The graphics characters utilize the entire character cell to allow for drawing continuous lines. For greater inter-character spacing the character cell size can be increased, with hardware straps, to 8 x 10 dots. Note that increasing the character cell size will cause gaps to appear between the graphics characters. Also, a different crystal is required for operations using an 8 dot cell.

The ALTR-2480 permits simple implementation of custom character fonts. To install a new character set, the user need only reprogram the EPROM character generator with the video information to generate his own font.

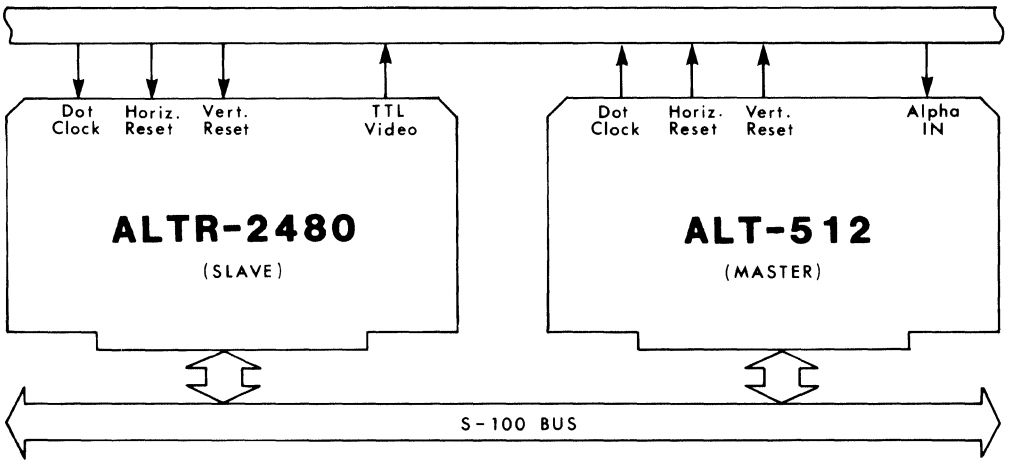



Figure 2. Combining ALTR-2480 with ALT-512 for alpha/graph displays

**ATTRIBUTES**
Each character is accessed by seven bits of the eight bit ASCII Character Code. This releases the most significant eighth bit for attribute selection. Characters displayed on the ALTR-2480 can be displayed either as normal (white on a black background), inverted (black on a white background), blinking, or both inverted and blinking. Character attributes are selected by on-board hardware straps and are enable/disabled by the eighth bit of the character code.

The on-board character generator can be strapped to generate a reduced 64 upper case only character set. In this configuration an extra bit from the character code is released. These two surplus bits can be used to enabled/disable any one of the four character attributes.

**VIDEO GENERATOR**
The ALTR-2480 can directly drive any standard monochrome video monitor. Composite video signals as well as separate TTL level video, horizontal/vertical sync and blinking signals are supported on-board.

**BUS INTERFACE**
The ALTR-2480 plugs directly into the S-100 bus. The display refresh memory, which is memory mapped into the S-100 memory address space, can be strapped to reside at any 4K byte memory address boundary between 0000H and FFFFH . The two internal registers (Video Control Register and Bank Select Register) are accessed through the unused location of the occupied 4K byte address space.

An on-board Bank Select Register allows up to eight ALTR-2480 boards to occupy the same address space in system memory. A single write instruction can select one of the resident ALTR-2480 boards for operation, making the other boards transparent to the user. The Bank Select Register is never inhibited by software and the display itself is not affected.

**GRAPHICS**
The ALTR-2480 can be integrated, as an alphanumeric controller, within a complete alpha/graph video system. By configuring the ALTR-2480 to operate in the slave mode, the horizontal/vertical reset lines and the dot clock line are set to act as input ports. In this way the board can be synchronized to a master sync source. These lines can also be configured to operate as output ports to enable the user to configure his system to synchronize to the ALTR-2480. A typical application of combined alphanumerics/graphics is shown in figure 2, where the graphics board (ALT-512) acts as the master sync source.

**PROGRAMMING**
The ALTR-2480 is programmed via two memory-mapped registers and 55 on-board hardware straps. Through the two registers the user can select which page is to be displayed (Video Control Register) when used in the 2 x 24 x 80 mode. The user can also select which ALTR-2480 board will be operational if more than one board occupies the same space in system address (Bank Select Register). The board's operational status is determined by the hardware straps. Table 1 outlines the definitions of these straps.

| JUMPER NO. | DESCRIPTION | JUMPER NO. | DESCRIPTION |
|---|---|---|---|
| S1 1-8 | Select base address | W4,6,8 | Enable 24 x 80 resolution |
| S3 1-8 | Select character cell size | W5,7,9 | Enable 2 x 24 x 40 resolution |
| S4 1-8 | Select American/European standard | W10,11 | Enable/disable Logic Video control |
| S5 1-2 | Select American/European standard | W12,13 | Select character attribute |
| S5 3-7 | Select character attribute | W15 | Enable 8080 CPU interface |
| W1,14 | Enable "Master" mode | W16 | Enable Z-80 CPU interface |
| W2 | Enable transparent memory mode | W17,18 | Enable/disable bank select option |
| W3 | Disable transparent memory mode | BS 0-7 | Select bank address |

Table 1. Jumper definitions.

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

With Transparent Memory Access: 800ns
Without Transparent Memory Access: 500ns

### DISPLAY PARAMETERS

| DESCRIPTION | DISPLAYED |
|---|---|
| Resolution | 1920 characters |
| Horizontal Characters | 80 characters |
| Vertical Lines | 24 lines |
| Character Cell Size | 6 or 8 horizontal dots |

### VIDEO TIMING

To generate a video display of 24 x 80 characters with a 6 dot wide character cell, the ALTR-2480 uses an 11.06688 MHz crystal. The following table gives the video timing for both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 42.0 μs | 43.0 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 4.3 μs | 4.3 μs |
| Vertical Sync Frequency | 60.0 Hz | 50.2 Hz |
| Vertical Sync Width | 255.0 μs | 255.0 μs |

5

### OUTPUT SIGNALS

TTL Level Video
Horizontal Drive
Vertical Drive
Composite Sync
Composite Video

### BUS INTERFACE

Address, data and control signals conform to S-100 Bus Specifications.

Control Registers and Display Memory — Selectable on any 4K byte memory address boundary 0000H — FFFFH (4000H)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1: 100 pin edge connector, O.156" centers | — Bus Interface | COMPAR ESA-50-DRSH |
| S2: 16 pin DIP socket | — Video Expansion Socket | AUGAT 516-A6-37D |
| J1: phono connector | — Composite Video | RCA 901 |

## PHYSICAL

### SIZE

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)

### POWER REQUIREMENTS

+8V DC ± 5% @ O.8A

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: O°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

ALTR-2480 — XX-X

- X — Horizontal dots per character (6/8)
- XX — AS — American standard (60 Hz); ES — European standard (50 Hz)

Example: ALTR-2480-AS-6: 24 x 80 display using a 6 dot wide character cell. Vertical refresh rate is 60 Hz.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

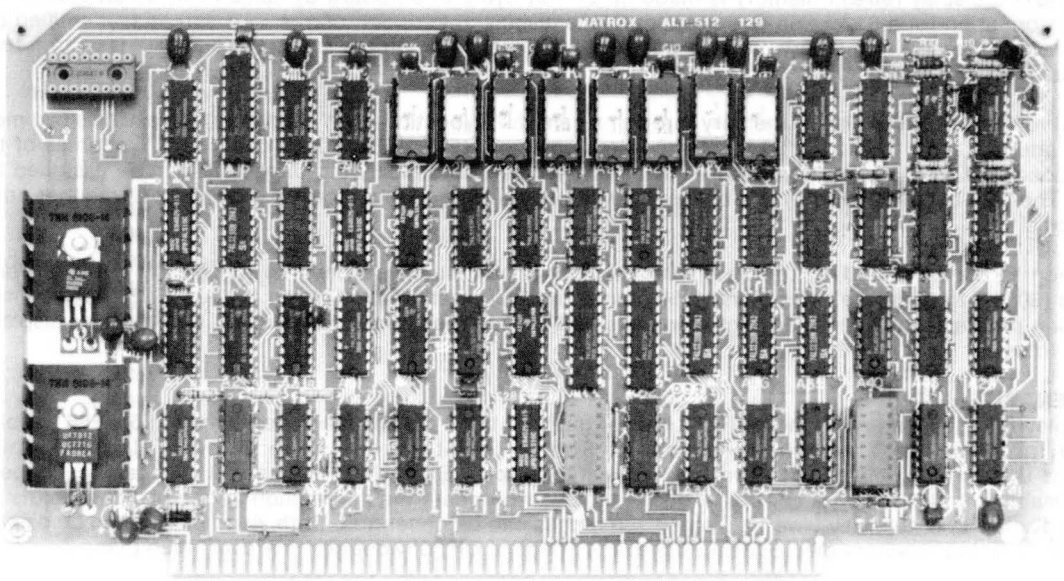
# ALT-512

## 512 x 256 GRAPHICS DISPLAY CONTROLLER FOR S-100 BUS

- **Displays 512 x 256 x 1 or 256 x 256 x 2**
- **Powerful X-Y virtual memory addressing**
- **Single instruction memory erase**
- **Grey-scale mode**
- **Color/grey-scale expansion**
- **Can be combined with ALTR-2480**
- **Transparent memory access**
- **S-100 bus compatible**
- **Internal/external sync**
- **American/European operation**

5

The ALT-512 is a complete graphics display controller on a single S-100 bus plus-in board. It contains its own 131,072 bit refresh memory, TV sync and video generators, and all the necessary I/O for the S-100 bus. Each display dot (pixel) is addresable via X-Y Registers and can be either written to or read from.



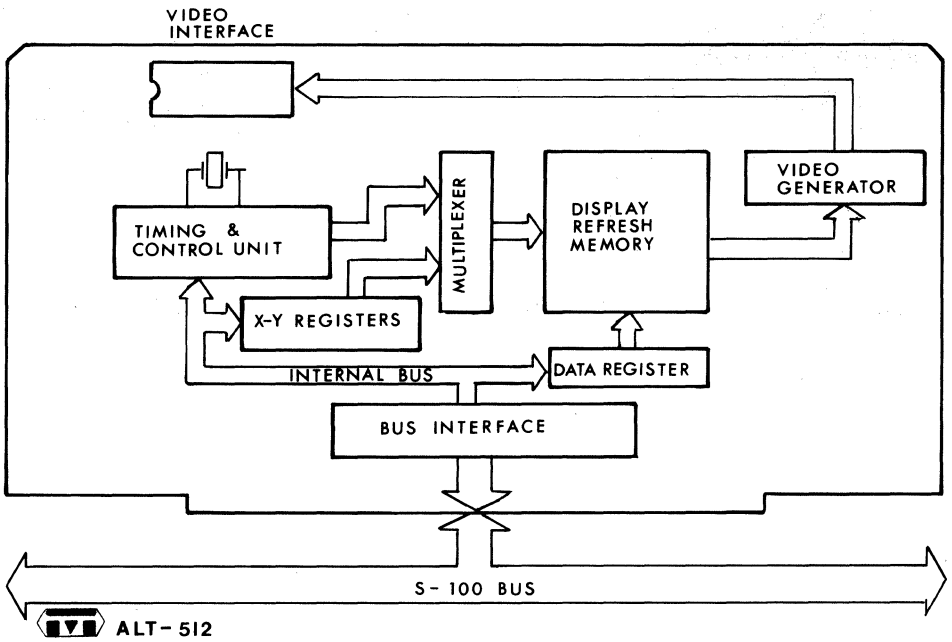



Figure 1. ALT-512 block diagram

5

**FUNCTIONAL DESCRIPTION**
The ALT-512 consists of five main functional blocks (figure 1): Timing and Control Unit, X-Y Registers, Display Memory, Video Generator, and Bus Interface.

**TIMING AND CONTROL UNIT**
All timing and control signals required by the video monitor (horizontal/vertical sync and blanking), display refresh memory (row/column addressing), and video generator (dot clock, load and shift) are generated by the Timing and Control Unit. The exact configurations of these signals are user-programmable, via hardware straps, to enable the ALT-512 to generate displays with up to 512 horizontal dots by 256 vertical dots in either 50 Hz (European) or 60 Hz (American) systems.

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the ALT-512 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The ALT-512's display refresh memory is made up of 16K bytes of on-board dynamic RAM which contains the binary picture information for a 512 x 256 dot raster graphics display. Each point on the CRT screen is identified by a unique address within the display memory. When a point is to be illuminated on the screen, a logic "1" is written to the appropriate display memory location.

The CPU reads/writes the display memory through a pair of I/O locations (X-Y Registers). This allows two memory locations to address all of the 131,072 bits of the refresh memory (512 x 256). Once the X and Y address of the dot has been loaded, the CPU can read/write the dot intensity. The dot intensity bit (image bit) can be assigned to any data bus bit. The resultant CRT display is a black and white image with the intensity of each dot being either on (logic "1") or off (logic "0").

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the ALT-512 efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display is "transparent" to user.

**VIDEO ENABLE**
The display refresh memory on the ALT-512 is arranged into two "pages", each containing 256 x 256 x 1 bits of binary picture information. Through an on-board Plane Register and Video Control Register the ALT-512 allows the user to manipulate the texture of the resultant display. Each video page or "plane" can be independently enabled/disabled, under software control, allowing the user to update the information in one plane while the other plane is being displayed. In this way "live" animated sequences can be generated. Both video planes can be displayed simultaneously, with the resultant display being the overlay (logical OR) of video plane A over video plane B.

**GREY-SCALE MODE**
The output video signal from each of the two video planes on the ALT-512 can be assigned a different weight or intensity. In this way the user can configure the ALT-512 to generate displays using up to 4 different grey-scale levels.

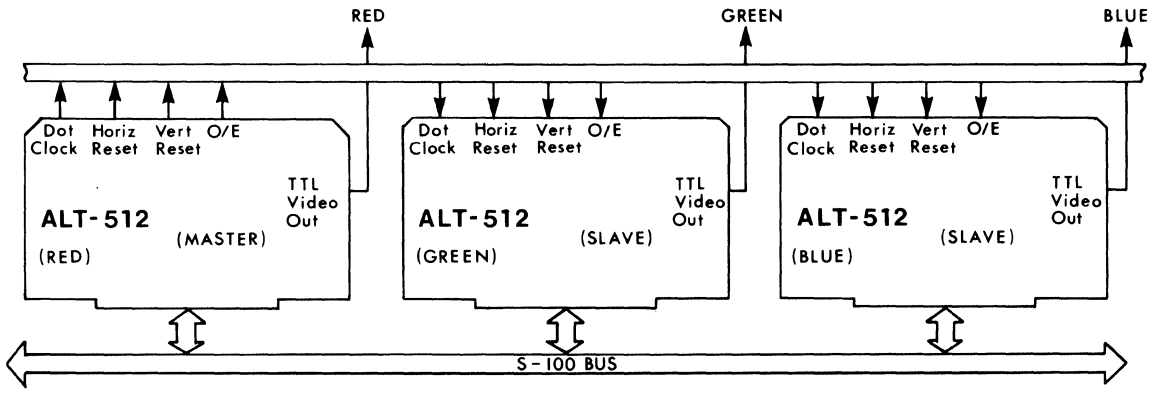



Figure 2. "Stacking ALT-512 cards for color/grey scale displays

**SCREEN ERASE**
The entire refresh memory on the ALT-512 can be erased by a single OUTput instruction. Setting the memory erase enable bit when writing to the display memory will cause the entire memory to be set to that intensity (0 = black, 1 = white).

**VIDEO GENERATOR**
The ALT-512 works with all standard monochrome video monitors in American (60 Hz) and European (50 Hz) systems. TTL level video, horizontal sync, vertical sync, as well as composite video signals are supported on-board.

**BUS INTERFACE**
The ALT-512 plugs directly into the S-100 bus and works with most 8-bit processors. All the Command and Status Registers as well as the Display Memory are accessed via I/O locations. The ALT-512 can be positioned on any 8 byte I/O address boundary between 00H and FFH.

**ALPHA/GRAPH DISPLAYS**
The ALT-512 can be combined with the ALTR-2480 to generate alphanumeric/graphic displays. An on-board alphanumeric input port accepts the TTL level alphanumeric video information from the ALTR-2480 and combined it with the graphics video from the ALT-512. The result is a powerful display combining both alphanumerics and graphics without the overhead involved in generating alphanumeric characters using graphic techniques.

**COLOR/GREY-SCALE EXPANSION**
Multiple ALT-512 boards can be "stacked" to provide for sophisticated color or grey-scale applications that require more bits per pixel. Up to 24 ALT-512 boards may be combined in this way to provide up to 24 bits/pixel (over 16 million colors).

**PROGRAMMING**
The ALT-512 can be programmed for American or European standard operation via a series of on-board hardware straps. Additional straps are provided to program the board to operate in either master or slave mode. These on-board straps are arranged into two 16 DIP sockets to facilitate simple field re-programming.

| SOCKET | DESCRIPTION |
|---|---|
| S1 1-6 | Select American/European operation |
| S1 8 | Enable Master mode |
| S2 1-8 | Select board base address |

Table 1. Jumper Definitions

# SPECIFICATIONS

**FUNCTIONAL**

**MEMORY ACCESS TIME**

Dot Write Time: 1.4$\mu$s

**DISPLAY PARAMETERS**

| DESCRIPTION | RESTRICTION |
|---|---|
| Horizontal Resolution | 512 dots max. |
| Vertical Resolution | 256 dots max. |

**VIDEO TIMING**

The ALT-512 generates a display of 512 horizontal dots x 256 vertical dots using an 11.06688 MHz crystal. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46 $\mu$s | 46 $\mu$s |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 5.67 $\mu$s | 5.67 $\mu$s |
| Vertical Sync Frequency | 60 Hz | 50.2 Hz |
| Vertical Sync Width | 190 $\mu$s | 190 $\mu$s |

5

**OUTPUT SIGNALS**

TTL Level Video
Horizontal Sync
Vertical Sync
Composite Sync
Composite Video

**BUS INTERFACE**

Address, data, and control signals conform to S-100 Bus Specifications.

Display Memory, Command and Status Registers — Selectable on any 8 byte I/O address boundary 00H — FFH (08H)

**CONNECTORS**

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 100 pin edge connector — Bus Interface | COMPAR ESA-50-DRSH |
| V: 16 pin DIP socket — Video Interface | AUGAT 516-A6-37D |

**PHYSICAL**

**SIZE**

Width: 10.00 in. (24.50 cm)
Height: 5.00 in. (12.70 cm)
Depth: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

+8V DC ±5% @ 100mA
−8V DC ±5% @ 600mA
−18V DC ±5% @ 10mA

**ENVIRONMENTAL REQUIREMENTS**

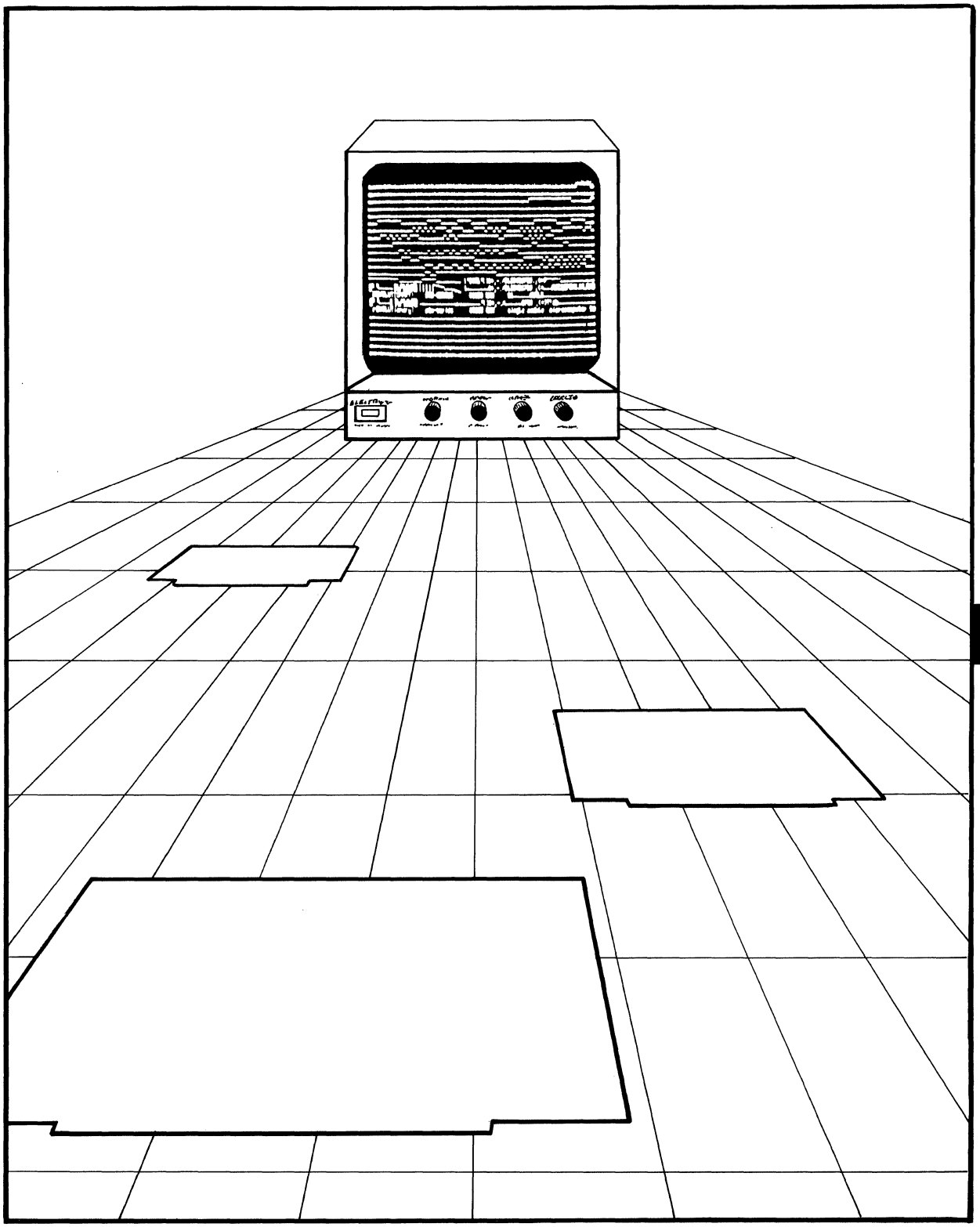
Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

**ORDERING INFORMATION**

ALT-512 — XX

- AS — American standard (60 Hz)
- ES — European standard (50 Hz)

Example: ALT-512-AS: 512 x 256 pixel display with a vertical refresh rate of 60 Hz.





# EXORCISER BUS VIDEO BOARDS

## SECTION 6 EXORCISER BUS VIDEO BOARDS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# EXO-2480

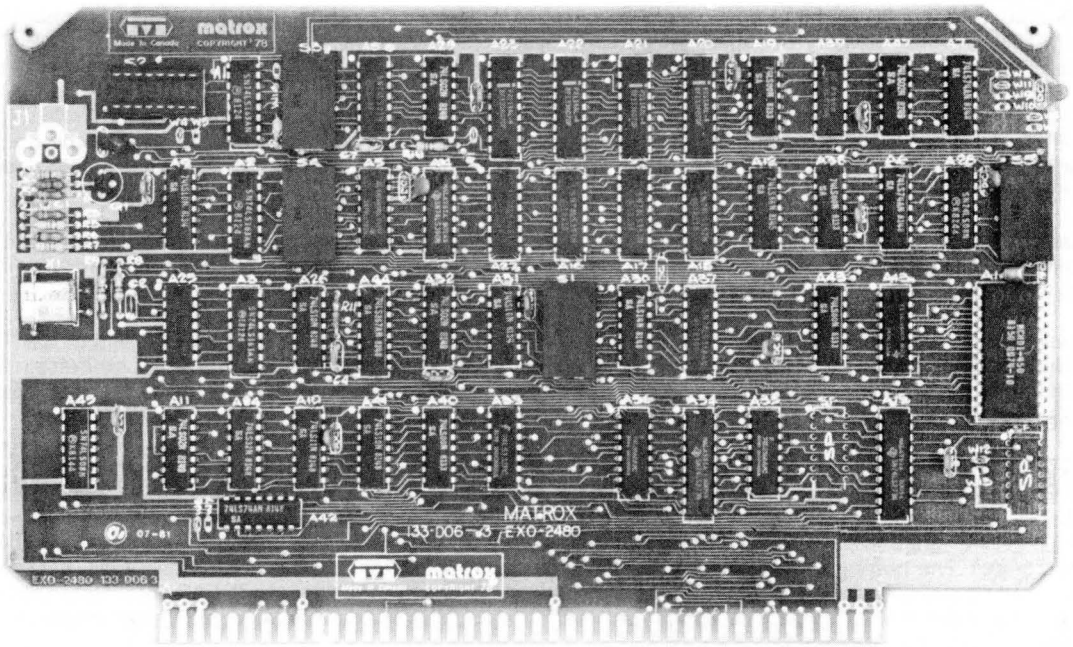
## 24 x 80 ALPHANUMERIC DISPLAY CONTROLLER FOR EXORCISER BUS

- **24 row x 80 column alphanumeric video display**
- **4K byte memory mapped display**
- **Normal, inverse, blink attributes**
- **EPROM ASCII character generator**
- **Transparent memory access**
- **Exorciser bus compatible**
- **Directly drives any monochrome monitor**
- **Alpha/graph expansion**
- **Single +5V supply**
- **External/internal sync capability**
- **American/European operation**

The EXO-2480 is an Exorciser* bus compatible alphanumeric display controller which is capable of generating displays of 24 lines of 80 characters per line. Characters can be displayed as either white on a black background or black on a white background. Each character can also be set to blink under software control.

The character font provided with the EXO-2480 contains 128 - 5 x 7 upper/lower case alphanumeric characters and graphic symbols. The character generator is user-programmable, allowing the user to implement his own custom character font.

The EXO-2480 works with all standard monochrome video monitors in Europe (50 Hz) and America (60 Hz).

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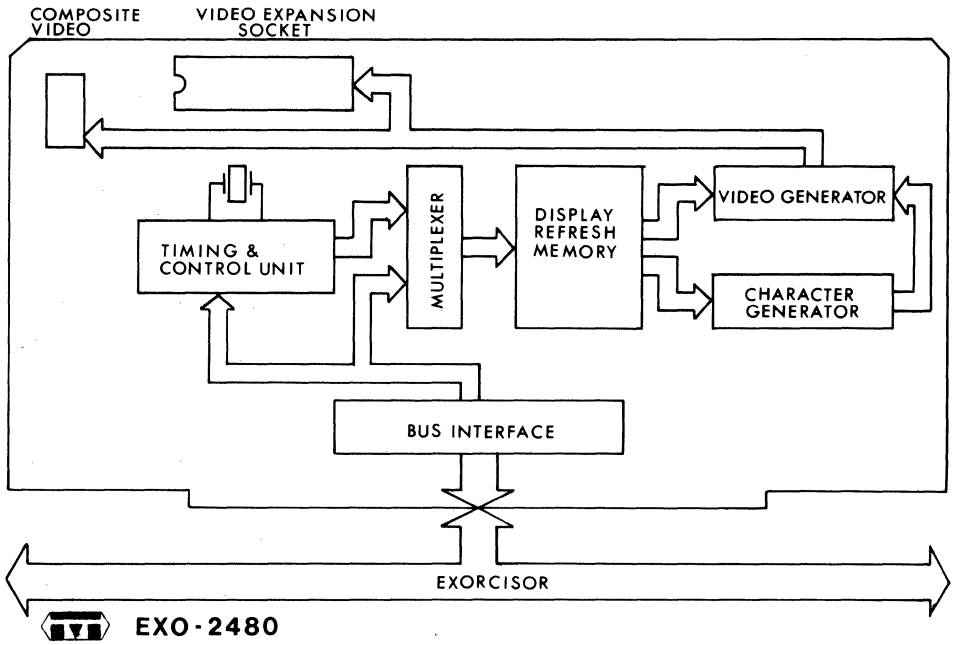



Figure 1. EXO-2480 block diagram

**FUNCTIONAL DESCRIPTION**
The EXO-2480 is made up of five major operational blocks: Timing and Control Unit, Display Memory, Character Generator, Video Generator, and Bus Interface. Communications between these blocks are shown in figure 1.

**TIMING AND CONTROL UNIT**
All timing and control signals required to generate a video display with 24 lines of 80 characters per line are supported on-board the EXO-2480. The Timing and Control Unit, consisting of the master oscillator (11 MHz) and various modulo counters, produces the horizontal and vertical sync signals needed by the monitor as well as all timing signals for display refresh memory (RAS, CAS).

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the EXO-2480 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The EXO-2480 contains 2K bytes of on-board display refresh memory, to store up to 24 lines of 80 characters (1920 characters). The display memory occupies 4K bytes of system address space thereby permitting the CPU to identify each character location with a unique 12 bit address.

The EXO-2480 can be strapped so that the display memory is arranged as two independently accessable pages. In this way the EXO-2480 is capable of storing two displays of 24 x 40 characters, of which one display can be updated while the other is being displayed. An on-board Video Control Register allows the user to software select which page is to be displayed.

Each character position of the CRT screen corresponds to an 8 bit location in the display refresh memory. Characters are written on to the display by loading the ASCII Character Code to the appropriate display memory location. The CPU can read/write the display memory at full speed using all memory reference instructions.

All accesses to the display memory are controlled by a "Transparent Memory" control circuit within the Timing and Control Unit. In this way all accesses to the display memory (read, write, refresh) are efficiently arbitrated. The Transparent Memory control circuitry permits the CPU to read or write the refresh memory at any time and the display is free of glitches.

**CHARACTER GENERATOR**
The EXO-2480 contains an on-board 2716 EPROM which contains the binary video information to generate a 128 character set. The supplied character font consists of the full 96 upper/lower case alphanumeric character set with the addition of 32 special graphic characters. The alphanumeric characters are formed in a 5 x 7 dot matrix within a 6 x 10 dot character cell. The graphics utilize the entire character cell to allow for drawing continuous lines. For greater inter-character spacing the character cell size can be increased, with hardware straps, to 8 x 10 dots. Note that increasing the character cell size will cause gaps to appear between the graphics characters. Also, a different crystal is required in applications utilizing an 8 dot cell.

The EXO-2480 permits simple implementation of custom character fonts. To install a new character set, the user need only reprogram the EPROM character generator with the video information to generate his own font.

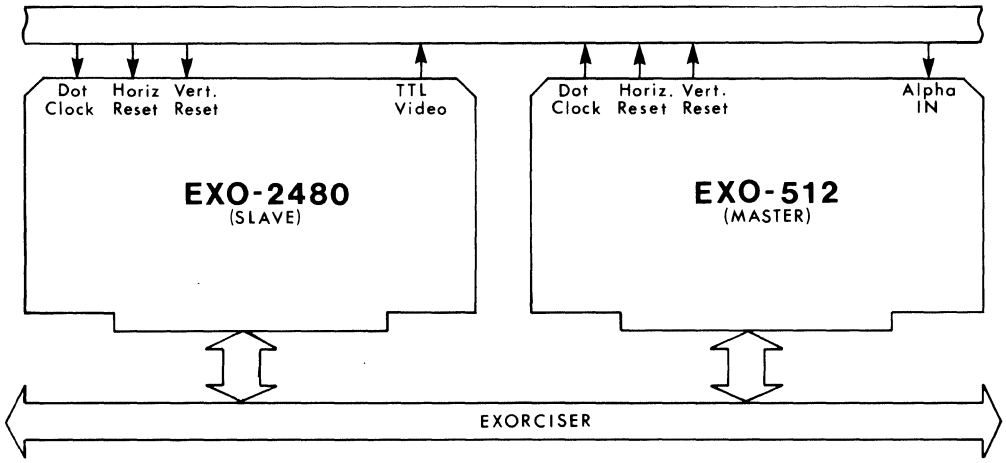



Figure 2. Combining EXO-2480 with EXO-512 for alpha/graph displays

**ATTRIBUTES**
Each character is accessed by seven bits of the eight bit ASCII Character Code. This releases the most significant eighth bit for attribute selection. Characters displayed on the EXO-2480 can be displayed either as normal (white on a black background), inverted (black on a white background), blinking, or both inverted and blinking. Character attributes are selected by on-board hardware straps and are enabled/disabled by the eight bit of the character code.

The on-board character generator can be strapped to generate a reduced 64 upper case only character set. In this configuration an extra bit from the character code is released. These two surplus bits can be used to enable/disable any one of the four character attributes.

**VIDEO GENERATOR**
The EXO-2480 can directly drive any standard monochrome video monitor. Composite video signals as well as separate TTL level video, horizontal/vertical sync and blanking signals are supported on-board.

**BUS INTERFACE**
The EXO-2480 plugs directly into the Exorciser bus. The display refresh memory, which is memory mapped into the system memory address space, can be strapped to reside at any 4K byte memory address boundary between 0000H and FFFFH.

**GRAPHICS**
The EXO-2480 can be integrated, as an alphanumeric controller, within a complete alpha/graph video system. By configuring the EXO-2480 to operate in the slave mode, the horizontal/vertical reset lines and the dot clock line are set to act as input ports. In this way the board can be synchronized to a master sync source. These lines can also be configured to operate as output ports to enable the user to configure his system to synchronize to the EXO-2480. A typical application of combined alphanumerics/graphics is shown in figure 2, where the graphics board (EXO-512) acts as the master sync source.

**PROGRAMMING**
Through an on-board I/O register the user can select which page is to be displayed (Video Control Register) when used in the 2 x 24 x 40 mode. This register is also used to allow software control of the video output of the board. Resetting the Logic Video Bit within the Video Control Register inhibits the video output of the EXO-2480. This feature is useful in applications combining alphanumerics and graphics. The board's operational status is determined by a series of on-board hardware straps. Table 1 outlines the definitions of these straps.

| JUMPER NO. | DESCRIPTION | JUMPER NO. | DESCRIPTION |
|---|---|---|---|
| S1 1-8 | Select base address | W6 | Enable 24 x 80 resolution |
| S3 1-8 | Select character cell size | W7 | Enable 2 x 24 x 40 resolution |
| S4 1-8 | } Select American/European standard | W8 | Enable 24 x 80 resolution |
| S5 1-2 | | W9 | Enable 2 x 24 x 40 resolution |
| S5 3-7 | Select character attribute | W10 | Enable logic video control |
| W1 | Enable "Master" mode | W11 | Disable logic video control |
| W2 | Disable transparent memory mode | W12 | Select character attribute |
| W3 | Enable transparent memory mode | W13 | Select character attribute |
| W4 | Enable 24 x 80 resolution | W14 | Enable "External sync" mode |
| W5 | Enable 2 x 24 x 40 resolution | | |

Table 1. Jumper definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

With Transparent Memory Access: 800ns
Without Transparent Memory Access: 500ns

### DISPLAY PARAMETERS

| DESCRIPTION | DISPLAYED |
|---|---|
| Resolution | 1920 characters |
| Horizontal Characters | 80 characters |
| Vertical Lines | 24 lines |
| Character Cell Size | 6 or 8 horizontal dots |

### VIDEO TIMING

To generate a video display of 24 x 80 characters with a 6 dot wide character cell, the EXO-2480 uses an 11.06688 MHz crystal. The following table gives the video timing for both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 43.0 $\mu$s | 43.0 $\mu$s |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 4.3 $\mu$s | 4.3 $\mu$s |
| Vertical Sync Frequency | 60.0 Hz | 50.2 Hz |
| Vertical Sync Width | 255.0 $\mu$s | 255.0 $\mu$s |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Drive
Vertical Drive
Composite Sync
Composite Video

### BUS INTERFACE

Address, data and control signals conform to Motorola Exorciser Bus Specifications.
Control Registers and Display Memory — Selectable on any 4K byte memory address boundary 0000H — FFFFH (4000H)

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 86 pin edge connector — Bus Interface | COMPAR ESM-43-DSRI |
| S2: 16 pin DIP socket — Video Expansion Socket | AUGAT 516-A6-37D |
| J1: phono connector — Composite Video | RCA 901 |

### PHYSICAL

**SIZE**

Width: 9.75 in. (30.01 cm)
Height: 5.97 in. (15.18 cm)
Depth: 0.50 in. (1.27 cm)

**POWER REQUIREMENTS**

+5V DC ±5% @ 0.8A

**ENVIRONMENTAL REQUIREMENTS**

Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 95% non-condensing

### ORDERING INFORMATION

EXO-2480 — XX — X

- X: Horizontal dots per character (6/8)
- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)

Example: EXO-2480-AS-6: 24 x 80 display using 6 dot wide character cell. Vertical refresh rate is 60 Hz.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

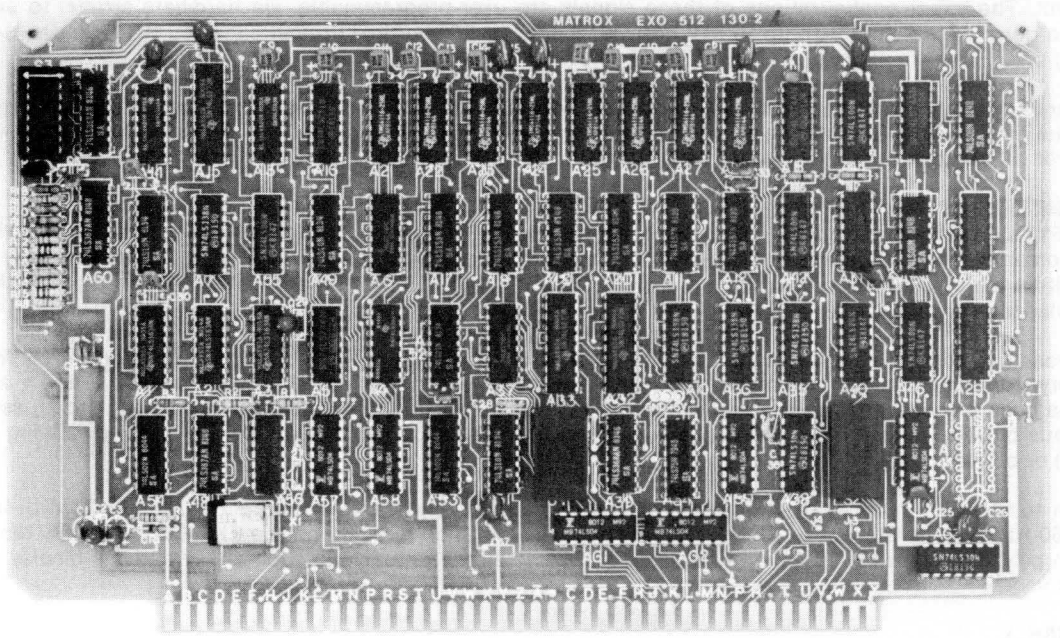
# EXO-512

## 512 x 256 GRAPHICS DISPLAY CONTROLLER FOR EXORCISER BUS

- **Displays 512 x 256 x 1 or 256 x 256 x 2**
- **Powerful X-Y virtual memory addressing**
- **Single instruction memory erase**
- **Grey-scale mode**
- **Color/grey-scale expansion**
- **Can be combined with EXO-2480**
- **Transparent memory access**
- **Exorciser bus compatible**
- **Internal/external sync**
- **American/European operation**

The EXO-512 is a complete graphics display controller on a single Exorciser bus plug-in board. It contains its own 131,072 bit refresh memory, TV sync and video generators, and all the necessary I/O for the Exorciser bus. Each display dot (pixel) is addressable via X-Y Registers and can be either written to or read from.





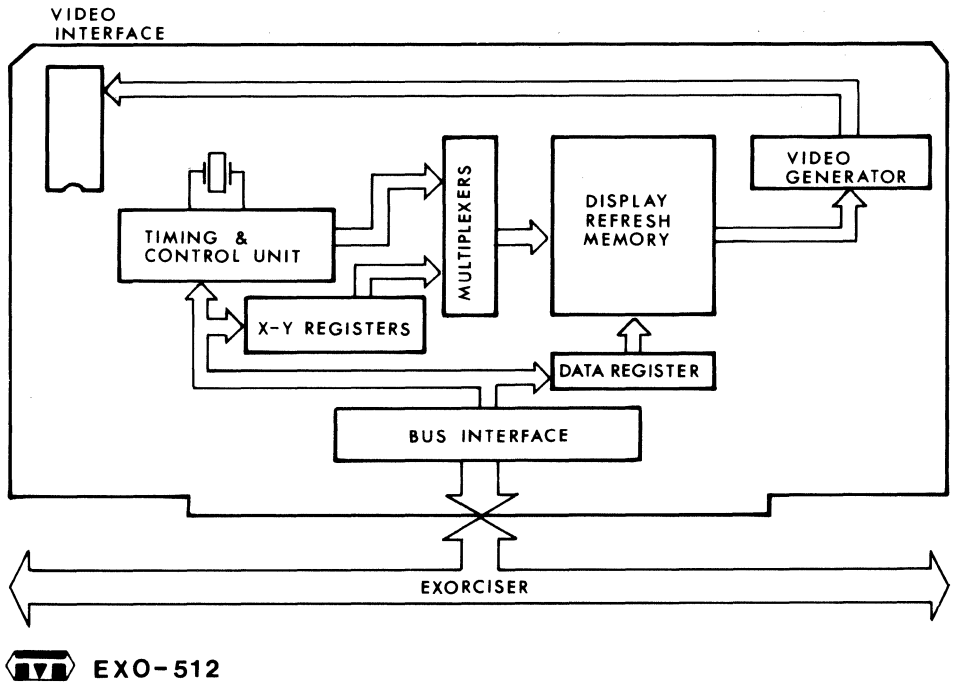



Figure 1. EXO-512 block diagram

6

**FUNCTIONAL DESCRIPTION**
The EXO-512 consists of five main functional blocks (figure 1): Timing and Control Unit, X-Y Registers, Display Memory, Video Generator, and Bus interface.

**TIMING AND CONTROL UNIT**
All timing and control signals required by the video monitor (horizontal/vertical sync and blanking), display refresh memory (row/column addressing), and video generator (dot clock, load and shift) are generated by the Timing and Control Unit. The exact configurations of these signals are user-programmable, via hardware straps, to enable the EXO-512 to generate displays with up to 512 horizontal dots by 256 vertical dots in either 50 Hz (European) or 60 Hz (American) systems.

The horizontal/vertical reset signals as well as the dot clock can be either generated on-board or accepted, through a bidirectional port, from an external sync source. In this way the EXO-512 can be synchronized to operate with other video boards as part of a complete video display system.

**DISPLAY MEMORY**
The EXO-512's display refresh memory is made up of 16K bytes of on-board dynamic RAM which contains the binary picture information for a 512 x 256 dot raster graphics display. Each point on the CRT screen is identified by a unique address within the display memory. When a point is to be illuminated on the screen, a logic "1" is written to the appropriate display memory location.

The CPU reads/writes the display memory through a pair of memory-mapped I/O locations (X-Y Registers). This allows two memory locations to address all of the 131,072 bits of the refresh memory (512 x 256). Once the X and Y address of the dot has been loaded, the CPU can read/write the dot intensity. The dot intensity bit (image bit) can be assigned to any data bus bit. The resultant CRT display is a black and white image with the intensity of each dot being either on (logic "1") or off (logic "0").

In addition to the CPU read/write, the display memory is continually scanned by the Timing and Control Unit every 16.66ms (60 Hz) to generate video signals. Memory access arbitration circuitry on the EXO-512 efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display is "transparent" to user.

**VIDEO ENABLE**
The display refresh memory on the EXO-512 is arranged into two "pages", each containing 256 x 256 x 1 bits of binary picture information. Through an on-board Plane Register and Video Control Register the EXO-512 allows the user to manipulate the texture of the resultant display. Each video page or "plane" can be independently enabled/disabled, under software control, allowing the user to update the information in one plane while the other plane is being displayed. In this way "live" animated sequences can be generated. Both video planes can be displayed simultaneously, with the resultant display being the overlay (logical OR) of video plane A over video plane B.

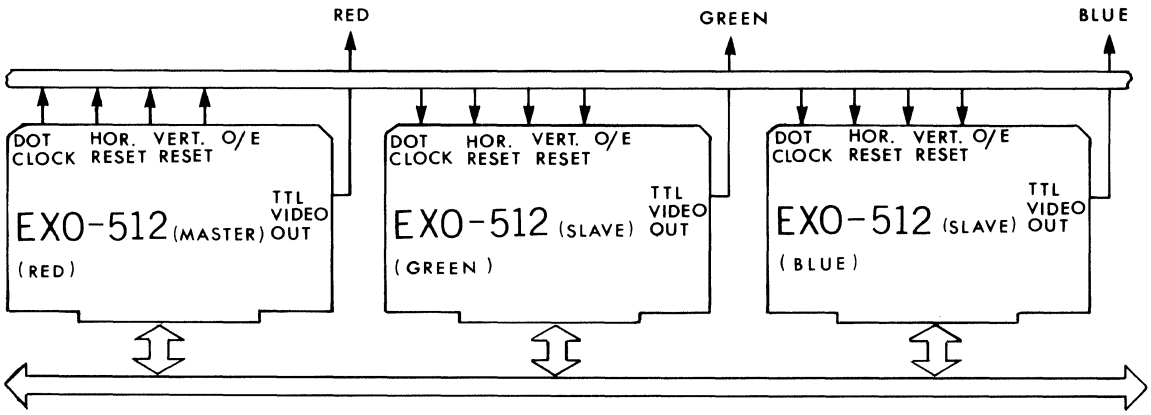



Figure 2. Stacking EXO-512 cards for color/grey scale displays

**GREY-SCALE MODE**
The output video signal from each of the two video planes on the EXO-512 can be assigned a different weight or intensity. In this way the user can configure the EXO-512 to generate displays using up to 4 different grey-scale levels.

**SCREEN ERASE**
The entire refresh memory on the EXO-512 can be erased by a single OUTput instruction. Setting the memory erase enable bit when writing to the display memory will cause the entire memory to be set to that intensity (0 = black; 1 = white).

**VIDEO GENERATOR**
The EXO-512 works with all standard monochrome video monitors in American (60 Hz) and European (50 Hz) systems. TTL level video, horizontal sync, vertical sync, as well as composite video signals are supported on-board.

**BUS INTERFACE**
The EXO-512 plugs directly into the Exorciser bus and works with most 8-bit processors. All the Command and Status Registers as well as the Display Memory are accessed via memory-mapped I/O locations. The EXO-512 can be positioned on any 8 byte memory address boundary between 0000H and FFFFH.

**ALPHA/GRAPH DISPLAYS**
The EXO-512 can be combined with the EXO-2480 to generate alphanumeric/graphic displays. An on-board alphanumeric input port accepts the TTL level alphanumeric video information from the EXO-2480 and combines it with the graphics video from the EXO-512. The result is a powerful display combining both alphanumerics and graphics without the overhead involved in generating alphanumeric characters using graphic techniques.

**COLOR/GREY-SCALE EXPANSION**
Multiple EXO-512 boards can be "stacked" to provide for sophisticated color or grey-scale applications that require more bits per pixel. Up to 24 EXO-512 boards may be combined in this way to provide up to 24 bits/pixel (over 16 million colors).

**PROGRAMMING**
The EXO-512 can be programmed for American or European standard operation via a series of on-board hardware straps. Additional straps are provided to program the board to operate in either master or slave mode. These on-board straps are arranged into two 16 DIP sockets to facilitate simple field re-programming.

| SOCKET | DESCRIPTION |
|---|---|
| S1 1-6 | Select American/European operation |
| S1 7 | Enable Master mode |
| S2 1-8 | Select board base address |

Table 1. Jumper Definitions

# SPECIFICATIONS

## FUNCTIONAL

### MEMORY ACCESS TIME

Dot Write Time: 1.4 μs

### DISPLAY PARAMETERS

| DESCRIPTION | RESTRICTION |
|---|---|
| Horizontal Resolution | 512 dots max. |
| Vertical Resolution | 256 dots max. |

### VIDEO TIMING

The EXO-512 generates a display of 512 horizontal dots x 256 vertical dots using an 11.06688 MHz crystal. The following table gives the timing in both American and European standards.

| SIGNAL | AMERICAN | EUROPEAN |
|---|---|---|
| Active Video | 46 μs | 46 μs |
| Horizontal Sync Frequency | 15.8 KHz | 15.8 KHz |
| Horizontal Sync Width | 5.67 μs | 5.67 μs |
| Vertical Sync Frequency | 60 Hz | 50.2 Hz |
| Vertical Sync Width | 190 μs | 190 μs |

### OUTPUT SIGNALS

TTL Level Video
Horizontal Sync
Vertical Sync
Composite Sync
Composite Video

### BUS INTERFACE

Address, data, and control signals conform to Motorola Exorciser Bus Specifications.
Display Memory, Command and Status Registers — Selectable on any 8 byte memory address boundary 0000-FFFFH (57F8H)

### CONNECTORS

| DESCRIPTION | | MATING CONNECTOR |
|---|---|---|
| P1 : 86 pin edge connector | — Bus Interface | COMPAR ESM-43-DSRI |
| V : 16 pin DIP socket | — Video Interface | AUGAT 516-A6-37D |

### PHYSICAL

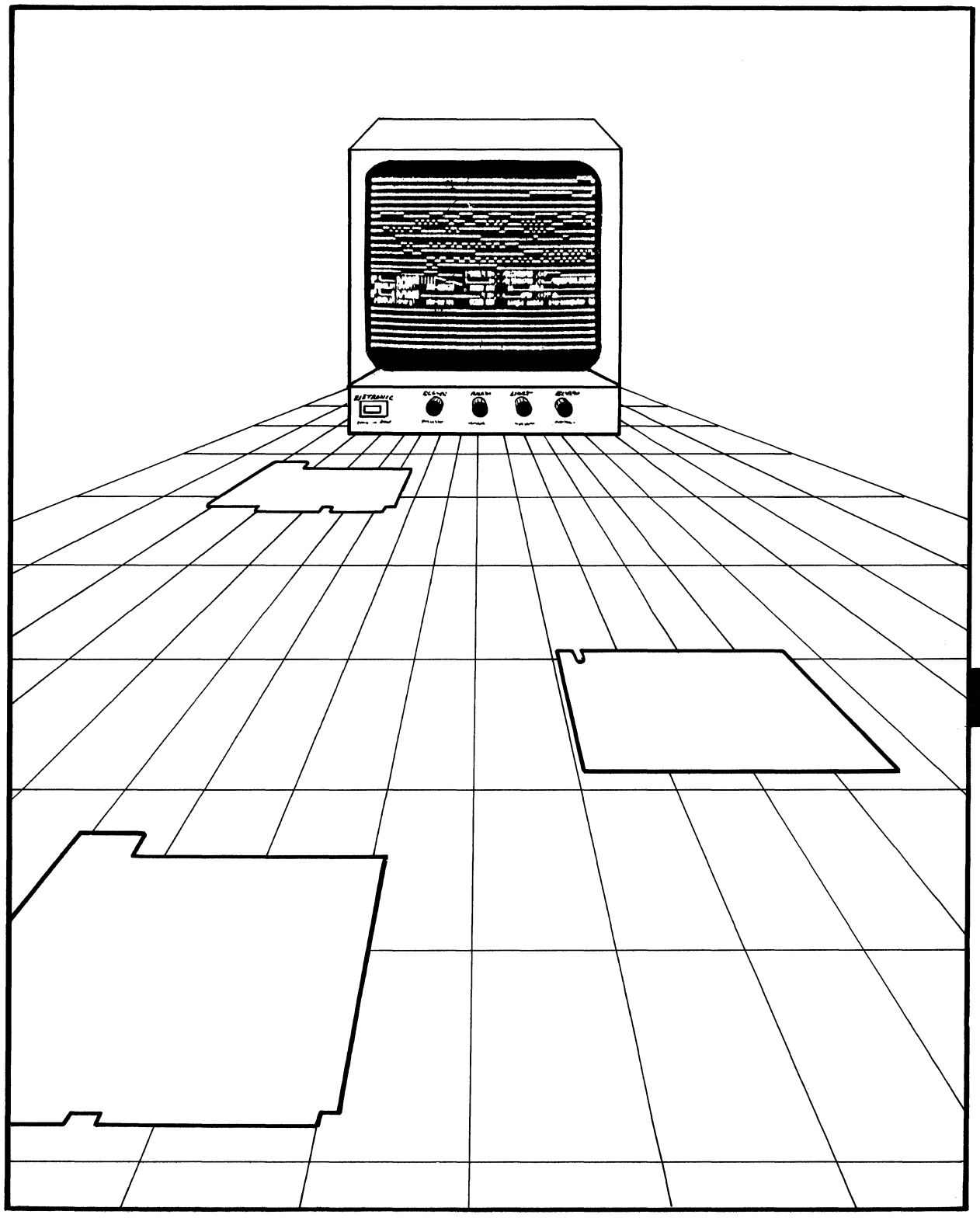
| SIZE | POWER REQUIREMENTS | ENVIRONMENTAL REQUIREMENTS |
|---|---|---|
| Width: 9.75 in. (24.76 cm) | +5V DC ±5% @ 600mA | Operating Temperature: 0°C to 55°C |
| Height: 5.97 in. (15.18 cm) | +12V DC ±5% @ 100mA | Relative Hymidity: 0% to 95% non-condensing |
| Depth: 0.50 in. ( 1.27 cm) | −12V DC ±5% @ 10mA | |

### ORDERING INFORMATION

EXO-512 — XX

- AS — American standard (60 Hz)
- ES — European standard (50 Hz)

Example: EXO-512-AS: 512 x 256 display with a vertical refresh rate of 60 Hz.



# SPECIAL PURPOSE VIDEO BOARDS

## SECTION 7 SPECIAL PURPOSE VIDEO BOARDS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# GT-600A

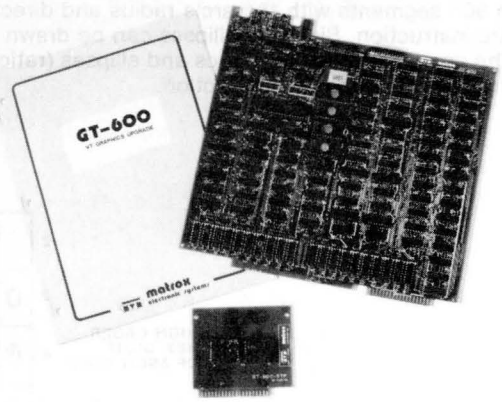
## GRAPHICS UPGRADE BOARD FOR VT-100 TERMINAL

- **Tektronix 4016 emulation**
- **PLOT-10 software compatibility**
- **Programmable resolution: 640 x 480, 1280 x 240, 640 x 240 x 2**
- **Pan, Zoom, and Scroll**
- **Printer interface (C.ITOH 8510A)**
- **VT-100, VT-103 compatible**
- **Vector generation for lines and circles**
- **Simple installation**
- **Low cost**

The Matrox GT-600 is a low cost/high performance plug in graphics board that upgrades the popular DEC VT-100 (VT-103) alphanumeric terminal to a graphics terminal. The on-board Z-80A CPU, resident firmware, and high speed vector generation make the GT-600/VT-100 combination an extremely powerful graphics terminal at a very low cost.

The powerful set of commands includes a subset emulation of the Tektronix 4010 series of graphic terminals. Existing Plot-10* based software is immediately transportable to the upgraded terminal without any change. In addition to executing all of the Tektronix 4010, 4014, 4016 commands, the GT-600 has many other enhancements. Included are generation of arcs and ellipses, a 96 ASCII character set with an inclined character baseline, software selection of pen size, pen aspect ratio, dashed line format, and high speed whole screen or selective area erase. Hardware functions include: pan (X direction) and scroll (Y direction) on a per pixel basis, independent X, Y zoom (from 1 to 8), and hardware erase.

Matrox's unique user defined resolution feature allows the software selection of four possible display configurations which are: 1280 x 240 x 1, 640 x 480 x 1, 640 x 240 x 2 (logical OR), and 64 x 240 x 2 (4 level grey scale). Automatic scaling from 1024 x 1024 input format can be selected for all configurations.



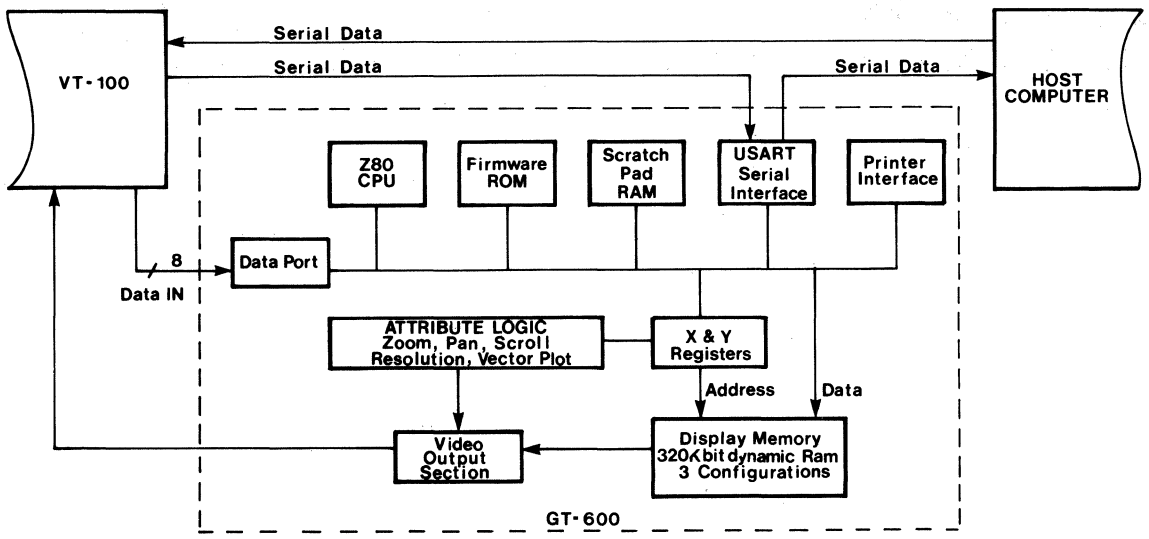



Figure 1. GT-600 block diagram

## FUNCTIONAL DESCRIPTION

The Matrox GT-600 is a plug-in graphics add-on board for the VT-100 and VT-103 alphanumeric terminals manufactured by Digital Equipment Corp. (DEC). When installed, it allows these terminals to emulate the Tektronix 401x (4010, 4014, 4016) series of graphic terminals and provides compatibility with the powerful PLOT-10 graphics package, also from Tektronix. In addition to its Tektronix compatible functions, the GT-600 provides a number of useful supplementary functions which can be exploited by the user.

## DISPLAY

The GT-600 features a unique user-definable resolution capability which allows the operator to select one of three available display configurations: 1280 x 240, 640 x 480, or 640 x 240 x 2. The third resolution option (640 x 240 x 2) is stored as two independent 640 x 240 bit planes. The two planes can be selected to be logically ORed together, (overlay), or used as intensity control bits to produce a 4 level grey scale image. The GT-600 also supports an automatic scaling feature which allows the user to run PLOT-10 software with any of the three format resolutions provided. When scaling is enabled, the GT-600 looks like the 1024 x 740 display used by the Tektronix 401x series terminals. Addresses and distance parameters sent by the host computer are automatically scaled to be compatible with the current display format resolution whether it be 1280 x 240, 640 x 480, or 640 x 240.

Every point on the display can be individually addressed and points can be drawn by simply defining the X and Y coordinates of the desired location (Point Plot Mode). Furthermore, strings of dots can be plotted on the GT-600 using relative address commands (Incremental Point Plot Mode). This mode enables the user to draw a line, up to 16 dots in length, from the present cursor position in any one of eight directions. Absolute vectors are drawn from the cursor position to a point whose X-Y coordinates are defined by the user. Line formats used to draw vectors are user selectable as solid, dashed, or dotted with the exact duty cycle defined in a special instruction.

The GT-600 allows the user to draw arcs and ellipses to the display using three simple commands. Arcs can be drawn in 90° segments with the arc's radius and direction (clockwise/counter-clockwise) information imbedded in the Draw Arc instruction. Similiarly ellipses can be drawn with a single instruction which includes the dimensions of the ellipse. The aspect ratio for both arcs and ellipses (ratio of the Y axis dimension over the X axis dimension) can be defined by the user in a separate instruction.

LOW ORDER HEX DIGIT OF ASCII CODE

| HIGH ORDER HEX DIGIT OF ASCII CODE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | | ! | " | # | $ | % | & | ' | ( | ) | * | + | , | - | . | / |
| 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| 4 | @ | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 5 | P | Q | R | S | T | U | V | W | X | Y | Z | [ | \ | ] | ^ | _ |
| 6 | ` | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| 7 | p | q | r | s | t | u | v | w | x | y | z | { | ! | } | ~ | ■ |

Figure 2. Alpha Mode character set

A crosshair graphics cursor is supported on board the GT-600 for efficient user-display interaction. The graphics cursor is positioned with the keyboard's cursor arrow keys which enable left, right, up, and down movement. Keeping any one of these keys depressed will cause the cursor to move continuously in the corresponding direction at an ever increasing rate.

**ALPHANUMERICS**
The GT-600's Alpha Mode allows for maximum flexibility in applying alphanumeric labels to the graphics display. The GT-600 supports a font of 96 upper/lower case alphanumeric characters (Figure 2) that are normally displayed light on a dark background. Up to 160 characters can be displayed per line on a maximum of 30 lines per page. Furthermore, the GT-600 supports two independent margins to allow two full pages of textual data to be displayed simultaneously (80 x 30 characters per page). The displayed characters are formed in a 5 x 7 "pen point" matrix within a 8 x 8 pen point character cell.

Several software commands are recognized by the GT-600 to set the alphanumeric display format. A variable baseline feature allows the user to display characters on a slope. The offset between characters can be up to 128 pen points up or down. Horizontal spacing between characters is also user selectable. Inserting a negative value for inter-character spacing allows the user to enter alphanumeric characters backwards (i.e. from right to left). The attitude of the displayed characters can be set to normal (rightside-up), upside-down, or oriented to the right or left.

**CONTROLS**
The GT-600 allows the user to set the size of the display "pen". Through this feature the operator can vary the width of the displayed lines: useful in creating bar graphs. By increasing the pen size, the user can also increase the size of the displayed alphanumeric characters.

A group of commands enable the user to manipulate the position of the display. Seperate commands are used to shift the display either vertically (scroll) or horizontally (pan) by an operator defined number of pixels. The GT-600 can also zoom in one any segment of the display (Zoom Window). This Zoom Window can be expanded by independent X and Y factors of 2 through 8.

**VIDEO INTERFACE**
The GT-600 can be used to drive an external monitor as well as the VT-100 display. Using sync signals generated within the VT terminal, the GT-600 provides a 1Vp-p composite video signal.

**PRINTER INTERFACE**
A parallel printer port is provided on the GT-600 to drive an external hard copy device. The standard GT-600 firmware supports a C.ITOH model 8510A Prowriter (drivers for other printers are available on special request).

**INSTALLATION**
The GT-600 is supplied with all the supplementary material required for installation. Once installed the GT-600 interfaces with the VT-terminal (VT-100 or VT-103) and the host computer as illustrated in figure 1. When the VT-terminal is operating in its normal manner, the GT-600 is transparent and has no effect on the system. However, once control has been given to the GT-600, serial data from the host computer is automatically forwarded to it via the 8-bit parallel port on the VT-terminal's Graphics Connector. The GT-600 sends data to the host computer through it's serial interface which is tied into the serial line coming from the VT-terminal. Serial data coming from the VT-terminal, however, passes through this interface on its way to the host computer without affecting the GT-600's operation.

**PROGRAMMING**
Upon initialization, all of the GT-600's attributes and special functions are configured to emulate the Tektronix 401X series graphics terminals. This emulator configuration, called the Tek Configuration, is special because it can not be changed until a modification enabling command is sent, and it can be returned to any time by sending a return command. If changes to attributes are attempted while in the Tek Configuration, the changed parameters will be stored but will not take effect until the modification enable command is received.

| | |
|---|---|
| FORMAT RESOLUTION | 1240 X 240 |
| SCALING | On |
| PEN ASPECT RATIO | Y/X = 1/1 |
| PEN SIZE | 1 |
| LINE FORMAT | Solid lines |
| HORIZONTAL IMAGE SHIFT | 0 |
| VERTICAL IMAGE SHIFT | 0 |
| ZOOM | Zoom by one |
| ELLIPSE & ARC ASPECT RATIO | Y/X = 1/1 |
| PEN COLOR | Bit plane 0 = light/bit plane 1 = dark |
| VIDEO DISABLE | Video 0 = enable/video 1 = disable |
| STATUS TERMINATION | CR |
| ALPHANUMERIC OFFSET | Vertical = 0/horizontal = 0 |
| ATTITUDE | Normal |

Table 1. Tek Configuration

A series of numbered wire-wrap pins are also included to implement various serial interface formats. The user can select to use either 7 or 8-bit data words and 1 or 2 stop bits. The user can also select either even, odd, or no parity.

# SPECIFICATIONS

## OPERATING MODES

### TRANSPARENT MODE

- In this mode the GT-600 becomes inactive and the VT-100 behaves exactly as it would without the add-on board

### ALPHA MODE

- Full ASCII character set
- User selectable character size: (8 x 8 to 255 x 255)
- Variable slope character baseline
- Inverse vidéo alpha cursor
- Selectable character shape (tall/thin, short/wide)

### POINT PLOT MODE

- Absolute addressing of points

### INCREMENTAL POINT PLOT MODE

- Relative addressing in any one of 8 directions
- "Long" form allows condensing of up to 16 moves in the same direction for compact representations of user defined fonts, etc.

### VECTOR MODE

- Absolute addressing of vectors
- User selectable line formats (solid, dashed, dotted)
- Can intermix commands for arcs and ellipses
- Variable line width (1 - 255)

## COMMAND SET

### DRAW

- Absolute vector
- Incremental vector
- Point plot
- Arc (size, quadrant)
- Ellipse (size)
- Text

### ALPHA CURSOR

- Move right space
- Backspace
- Linefeed
- Vertical tab
- Carriage return

### HARDCOPY

- Output to parallel port

### STATUS INQUIRY

- Graphic cursor position
- Current pen position
- Current alpha position

### SET ATTRIBUTES

- Pen size
- Pen color
- Pen aspect ratio
- Ellipse aspect ratio
- Dash line format
- Character baseline slope
- Character orientation

### GRAPHIC INPUT CROSSHAIR CURSOR

- Load start location
- Move crosshair cursor

### SET SPECIAL FUNCTIONS

- Pan
- Scroll
- Zoom
- Preset (clear) screen
- Video enable

### SELECT

- Resolution
- Scaling
- Tektronix emulator mode
- Point Plot Mode
- Incremental Point Plot Mode
- Vector Mode
- Crosshair Cursor Mode
- Graphics Input Mode
- Graphic Input Mode termination string

## VIDEO SPECIFICATIONS

### RESOLUTION

- 1280 x 240 x 1 bit
- 640 x 480 x 1 bit
- 640 x 240 x 2 bit (logical OR)
- 640 x 240 x 2 bit (grey scale)

### VIDEO OUTPUT

- RS-170 composite video (75 ohm)
- Separate output for external monitor

### HARDWARE FUNCTION GENERATOR

- Clear screen (16.6 ms)
- X, Y zoom (from 1 to 8)
- X, Y pan and scroll (single pixel and up)

## PHYSICAL SPECIFICATIONS

### POWER REQUIREMENTS

- +5V @ 2A
- +12V @ 500mA
- +12V @ 100mA

### ENVIRONMENTAL REQUIREMENTS

- Operating Temperature: 10° to 40° C
- Relative Humidity: 10 to 90% (non-condensing)

## ORDERING INFORMATION

The GT-600A is ordered as a complete kit and contains:

- one video and processor board that plugs into the VT terminal Graphics Board connector
- a serial interface card (4.5" x 1.275") that plugs into the terminal control board
- a backplane
- all mounting hardware
- technical manual

- the GT-600A is compatible with the VT-100, VT-103, VT-125, and VT-132.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

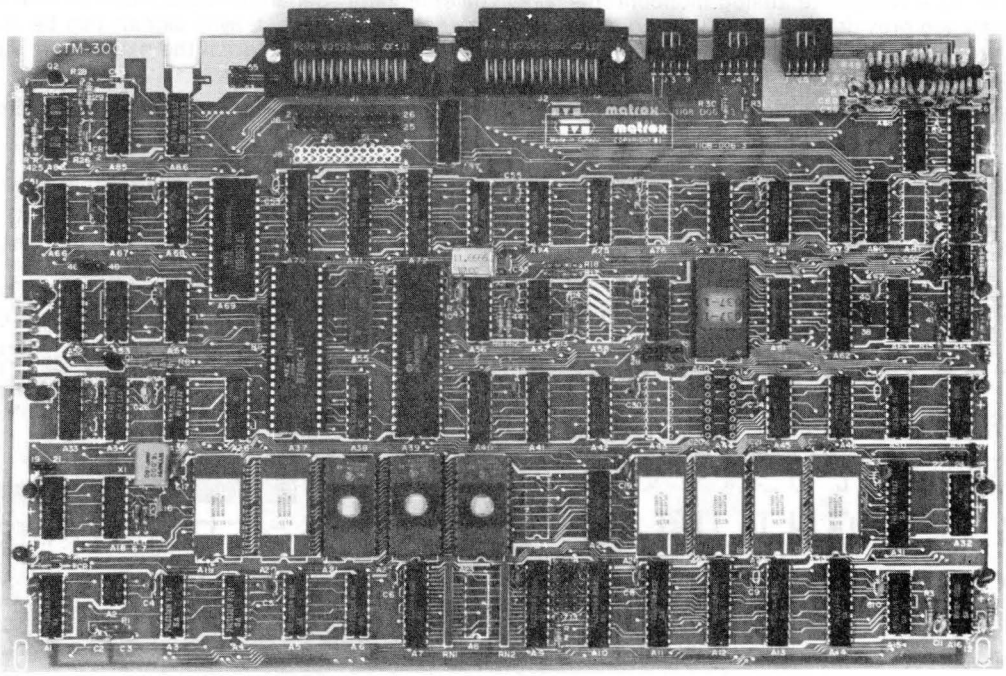
# CTM-300/BRD

## SINGLE BOARD INTELLIGENT COLOR ALPHANUMERIC TERMINAL

- **8-color alphanumeric display**
- **Programmable display format**
- **On-board Z-80A CPU**
- **256 different displayable characters**
- **ANSI standard firmware**
- **RS-232C input**
- **RGB color output (RS-170)**
- **Keyboard, printer, and light pen interfaces**
- **2K byte program download**
- **50/60 Hz operation**
- **19" rack-mount**
- **Blink, extended height, underline, and protected character attributes**

The Matrox CTM-300/BRD is an intelligent color alphanumeric terminal controller contained on a single PC board. When combined with an external keyboard and color CRT monitor, the CTM-300/BRD provides all of the features of an intelligent black and white terminal with the addition of color. The CTM-300/BRD supports 256 different displayable characters which include all of the alphanumeric characters and punctuation symbols for displaying text in one of six languages; English, French, Spanish, German, Greek, or Swedish. A set of graphic symbols are also supported by the CTM-300/BRD to enable the user to generate "character-oriented" graphic displays (business forms, process loop displays, bar charts, etc.).

The CTM-300/BRD firmware conforms to ANSI X3.64 and includes a comprehensive set of cursor, erase, and character attribute controls which facilitate text editing. The on-board firmware also configures the video output to produce a standard display format of 80 characters per line by 25 lines. A unique program download feature, together with a series of DIP switches, enable the user to adapt most of the CTM-300/BRD functions to conform to his specific requirements.



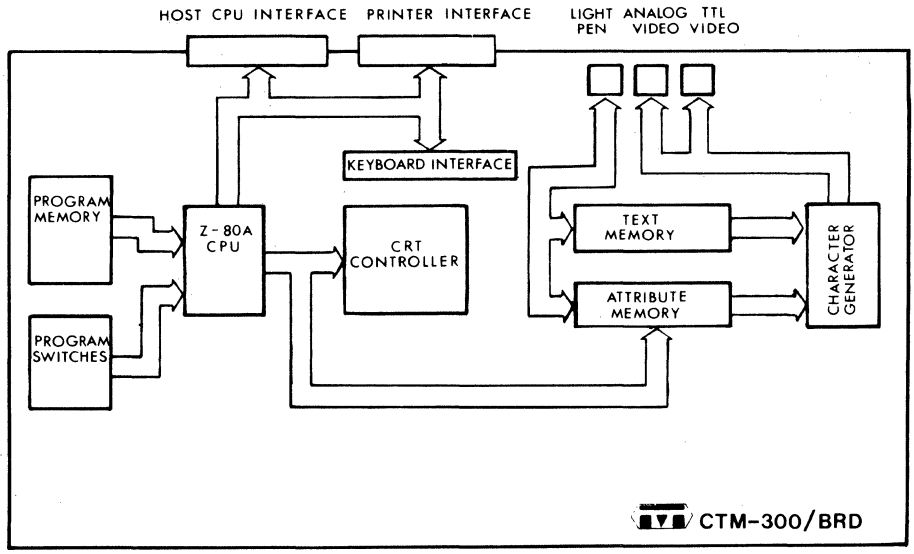



Figure 1. CTM-300/BRD Intelligent Color Terminal — Typical system configuration

## DISPLAY

The CTM-300/BRD generates a color alphanumeric display consisting of 25 horizontal lines with 80/132 characters (switch selectable) displayed per line. These parameters, however, can be redefined by the user to accomodate virtually any configuration of characters/line and lines/page up to maximum of 4000 characters per display. Characters can be assigned as blinking, underlined, or protected (protected characters can not be erased or edited while the erasure mode is not in effect). The blink or underline attribute can optionally be replaced (via a hardware strap) by an extended height attribute for displaying double height characters. Furthermore, each character can be assigned to be displayed in one of eight different foreground colors on one of eight different background colors. Color selection (foreground/background) is also user selectable via user function keys on the CTM-300/BRD.

7

As supplied, the CTM-300/BRD contains a font of 256 displayable characters. This character set (figure 2) consists of all the alphanumeric characters and punctuation symbols for displaying text in one of six different languages: English, French, Spanish, German, Greek, or Swedish. The CTM-300/BRD also includes a set of 32 "graphic characters" which can be used for generating character oriented graphics such as: business forms, process loop displays, bar charts, etc. Moreover, the user can redefine the character set for custom applications by simply replacing the supplied character generator with a 2532 EPROM loaded with his custom character font.

## MONITOR INTERFACE

Two video output connectors are available on the CTM-300/BRD to drive either a direct drive TTL color monitor, an analog RGB color monitor, or a composite analog monochrome (grey scale) monitor. Separate R,G,B video as well as horizontal and vertical sync signals are provided on the TTL video connector. The polarity of the TTL sync signals can be strapped for either positive or negative logic. On-board circuitry is also provided to allow the user to program the exact sync width and position, for use in non-standard monitors.

A separate 1Vp-p composite video signal is provided which permits monochrome displays with up to 8 different grey levels. Sync polarity on the composite signal is fixed to negative going.

## KEYBOARD INTERFACE

An on-board 8-bit parallel port latches data from an external keyboard in response to a negative going strobe from the keyboard. The resident Z-80A CPU, signaled via an interrupt generated by the keyboard strobe, can then read the keyboard buffer.

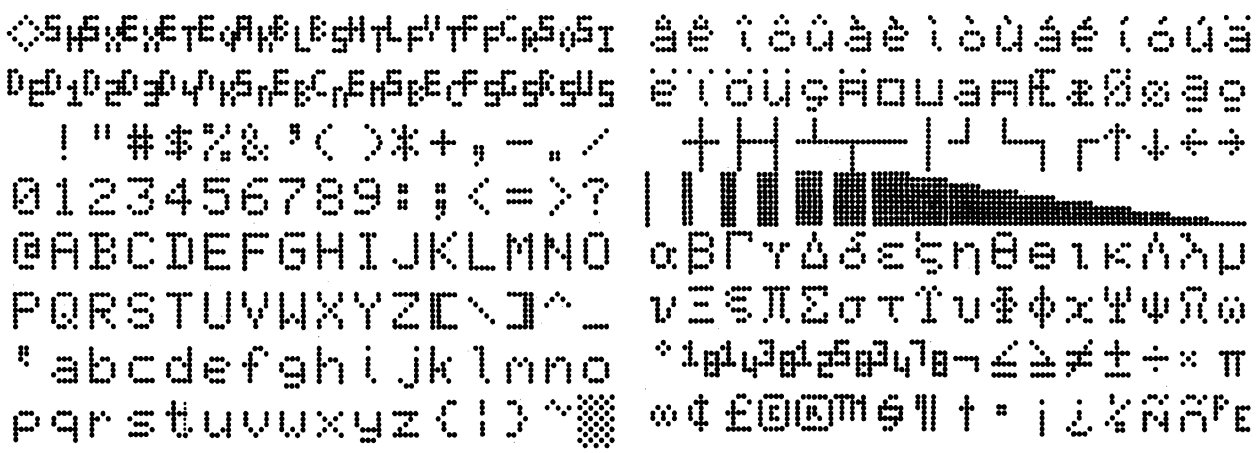


Figure 2. CTM-300/BRD Character set

## EDITING

The CTM-300/BRD includes a comprehensive set of cursor, erase, and character attribute controls which facilitate text editing. Cursor control commands enable the user to redefine the position of the cursor using either "relative" or "absolute" movement commands. Relative cursor movement commands include: Backward Field, Back Space, Cursor Down, and Cursor Up, which defines the cursor's position "relative" to its former position. Absolute cursor positioning places the cursor in a location whose X and Y coordinates are explicitly defined in the instruction. Other editing commands include: Insert/delete a character/line, erase a line/area/display, and protect a selected area. The CTM-300/BRD also includes a scroll feature which will cause the display to be scrolled up one line when a Carriage Return (CR) command is issued while the cursor is in the bottom-most line of the display.

The full usable command set of the CTM-300/R is shown below, and conforms to the ANSI standard X3.64. Moreover the CTM-300/R includes 2K bytes of user RAM into which the user can download custom functions. These user-defined functions are executed by a special Execute User Function command. The terminal firmware can be replaced with 20K bytes of user installed ROM/RAM loaded with the user's custom firmware.

## COMMAND SET

Self Test
Unlock Keyboard
Lock Keyboard
Start Protected Field
End Protected Field
Protect Selected Area
Protected Field
Insert Character
Insert Line
Delete Character
Delete Line
Clear Selected Area
Clear to End of Screen
Clear from Beginning of Screen to Cursor
Clear Screen
Clear Protected Only
Clear Unprotected Only
Clear to End of Line
Clear from Start of Line to Cursor
Clear Line
Clear Protected Fields on Line
Clear Unprotected Fields on Line
Auto Line Feed On/Off
Start of Selected Area
End of Selected Area
Read Back Selected Area
Define Scrolling Area
Set Tab
Clear Tab
Clear All Tabs
Back Tab
Tab
Cursor Left
Cursor Down
Cursor Up
Cursor Right
Cursor to Left of Line
Cursor Home
Set Cursor Position
Read Cursor Position
Set Line Number
Set Column Number
Set Color
Set Cursor On/Off
Read Light Pen
Connect to Printer
Set Alternate Character Set
Set Standard Character Set
Load Character Set Map
Load User Defined Function
Execute User Function
Load Screen Format
Beep

## COMPUTER INTERFACE

The CTM-300/BRD communicates with the host computer via an RS-232C serial interface, which can be configured by switches for several modes of operation. Input and output parity is selectable as even, odd, or no parity; and the user can choose one or two stop bits. Both full and half duplex operation are possible and the unit can be operated in an on-line or off-line mode. The user can also select the baud rate which can be from 110 baud to 19.2K baud.

## PRINTER INTERFACE

Any Centronics-compatible printer using positive logic can be connected to the CTM-300/BRD. In addition to the parallel ASCII inputs, the unit provides a strobe output and a Busy Input.

## LIGHT PEN INTERFACE

User-display interaction is possible through the use of a high speed light pen. When the user points the light pen at an illuminated spot on the CRT, the CTM-300/BRD loads the screen coordinates into an internal light pen register. The pen position may then be read by the processor. Note that the light pen can only be used with monitors having short persistence phosphors.

## PROGRAMMING

Functions that are not normally changed during actual operation are set by a series of switches located on the CTM-300/BRD mother board (table 1). 2K bytes of user RAM is also available for the user to define special functions. The CTM-300/BRD accepts data, from the host computer, in Intel Hex Format.

| SWITCH | NUMBER | DESCRIPTION |
|---|---|---|
| SW0 | 1 | Select baud rate (110 — 19.2K baud) |
| | 2 | |
| | 3 | |
| | 4 | Select number of bits per character (7/8) |
| | 5 | Select parity (on/off) |
| | 6 | Select parity (even/odd) |
| | 7 | Select number of stop bits (1/2) |
| | 8 | Select full/half duplex |
| SW1 | 1 | Select control mode (normal/monitor) |
| | 2 | Select terminal mode (local/on-line) |
| | 3 | Select cursor (steady/blinking) |
| | 4 | Select cursor (underline/block) |
| | 5 | Select number of characters per line (80/132) |
| | 6 | Select transmission protocol (XON-XOFF/RTS-CTS) |
| | 7 | Enable key click |
| | 8 | Select display mode (interlaced/non-interlaced) |

Table 1. Programming switches description

# SPECIFICATIONS

## DISPLAY PARAMETERS

| PARAMETER | RESTRICTION |
|---|---|
| Resolution | 4000 characters max. |
| Characters per Line | 80 standard, 132 max. |
| Lines per Page | 25 standard, 50 max. |
| Character Matrix Size | 5 x 7, 7 x 9 dots |
| Character Set | 256 upper/lower case alphanumeric and graphic characters |
| Languages | English, French, German, Greek, Spanish, Swedish |
| Foreground Colors | Red, green, blue, magenta, yellow, cyan, white, black |
| Background Colors | Red, green, blue, magenta, yellow, cyan, white, black |
| Cursor | Displayed/non-displayed, block/underline, blinking/steady |

## INTERFACES

| INTERFACE | DESCRIPTION | MATING CONNECTOR |
|---|---|---|
| Host Computer (J1) | RS-232C and 20mA current loop | DB-25 type connector (male) |
| Parallel Printer (J2) | Centronics compatible | DB-25 type connector (male) |
| Light Pen (J3) | 10 pin header | AMP 102184-3 |
| TTL Video (J4) | 10 pin header | AMP 102184-3 |
| Analog Video (J5) | 10 pin header | AMP 102184-3 |
| Keyboard Input (J6) | 26 pin header | 3M #3399 |
| Power Supply (J7) | 8 pin header | Molex 26-11-6074 |

## SIZE

| | |
|---|---|
| Height: | 7.75 in. (19.8 cm) |
| Width: | 12.0 in. (30.5 cm) |
| Depth: | 0.50 in. (1.27 cm) |

## POWER REQUIREMENTS

± 5V DC @ 1.6A
± 12V DC @ 50mA

## ENVIRONMENTAL REQUIREMENTS

| | |
|---|---|
| Operating Temperature: | 10° to 40° C |
| Relative Humidity: | 0 to 95% non-condensing |

## ORDERING INFORMATION

CTM-300/BRD-X — Single board intelligent color alphanumeric terminal

- A — American standard (60 Hz)
- E — European standard (50 Hz)

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MSBX-800

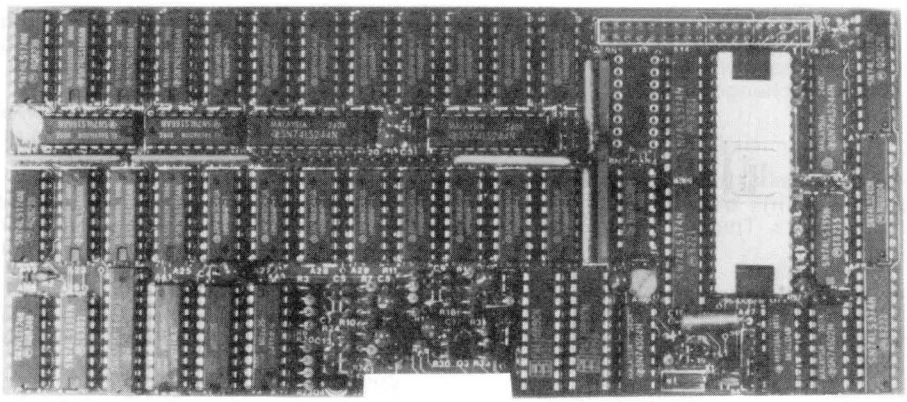
## HIGH RESOLUTION COLOR GRAPHICS iSBX MULTIMODULE*

- **Display resolution up to 800 x 600 x 4**
- **16 colors selectable from a palette of 4096**
- **50/60 Hz interlaced or non-interlaced operation**
- **VLSI graphics processor (7220) draws vectors, arcs, circles, rectangles, and characters**
- **Split-screen, pan, and scroll**
- **Analog RGB video outputs**
- **Double width iSBX Multimodule***
- **All mounting hardware supplied**
- **Single +5V supply**
- **Plugs into Matrox PBC-80 (Z-80A) or MBC-86/12 (8086) Multibus CPUs**
- **Light pen support**

The Matrox MSBX-800 is a powerful color graphics display controller contained on a double-width iSBX Multimodule. The MSBX-800 piggybacks onto any processor board using iSBX expansion connectors, including the Matrox MBC-86/12A and PBC-80. The host CPU transfers data directly to the MSBX-800 without having to access the Multibus, hence increasing system throughput. Complex graphic images can be created on the MSBX-800 with resolutions ranging from 256 x 256 x 4 to 800 x 600 x 4.

The MSBX-800 recognizes an instruction set of 17 commands. These instructions enable the user to create displays with minimal host intervention or calculational overhead. Instructions include: defining video parameters, draw a line, draw an arc, draw a circle, draw a rectangle, draw a character, pan, and scroll. Area fills and pixel blink are also supported.

The MSBX-800 provides extremely powerful graphics functionality at a very low cost. By adding this module to a CPU board, the user can create a low cost intelligent graphics terminal with his own specialized graphics firmware.



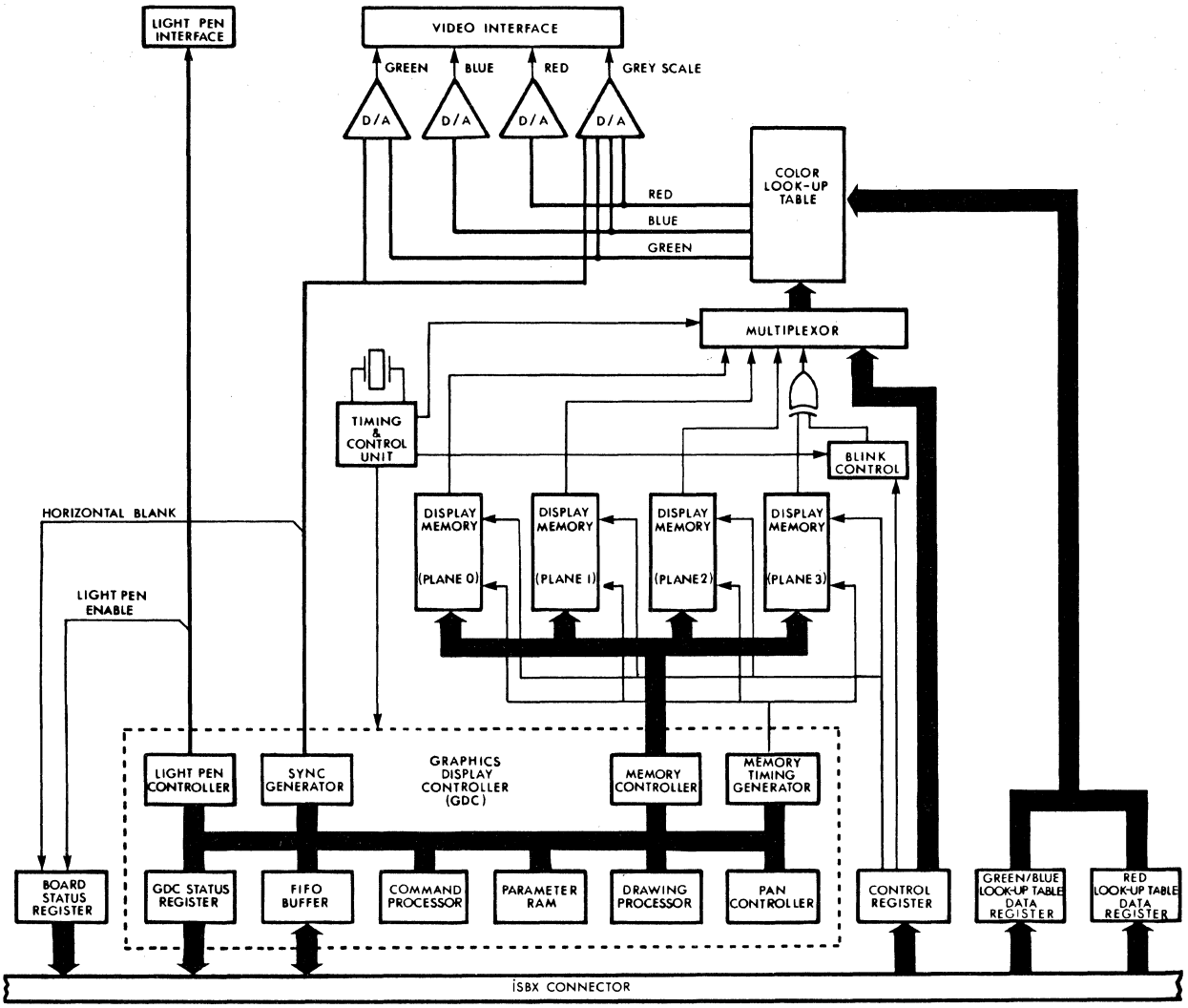



Figure 1. MSBX-800 block diagram

## MSBX-800 FEATURES

**Read/Write Area:** Read/write memory is 128K bytes (with 64K RAMs) expandable to 512K bytes (with 256K RAMs)

**Standard Resolution:** 512 x 512 interlaced or non-interlaced (512 x 480 with 60 Hz vertical refresh rate)

**User Selectable Resolutions:** 256 x 256 x 4 to 800 x 600 x 4 resolutions can be programmed by the user. Note that some resolutions will require crystal and/or RAM part changes.

**Bits/Pixel:** 4 bits/pixel

**Blink:** Selected areas of the graphics display can be set to blink between any two predefined colors. The blink frequency is set at 1.8 Hz.

**Split Screen:** The display screen can be split horizontally into two independent image areas. The size of each area is software programmable.

**Pan:** Each image area can be horizontally panned, inside the read/write area, by multiples of 16 pixels.

**Scroll:** Smooth vertical scroll by one line resolution on either image area.

**Graphics Instructions:** The MSBX-800 understands 17 graphics instructions.

**Figure Generation:** Graphics primitives, such as lines, arcs, circles, and rectangles are drawn by the MSBX-800 using single instructions.

**Characters:** Any character can be defined by the user and then drawn by the MSBX-800 using a single instruction.

**Draw Speed:** 1.6 μsec./pixel/plane minimum; includes vectors, arcs, circles, rectangles, and character draws.

**Video Parameters:** All video parameters including horizontal and vertical syncs, blanking, frequency, and display format are user software programmable.

**Light Pen:** On-board register latches deglitched light pen position. Interface built-in.

**Video Outputs:** R,G,B color signals $1V_{p-p}$ into 75Ω, sync can be either composite on green or supplied as a separate signal.

**iSBX Interface:** The MSBX-800 plugs directly into the iSBX bus and looks to the host like five local registers.

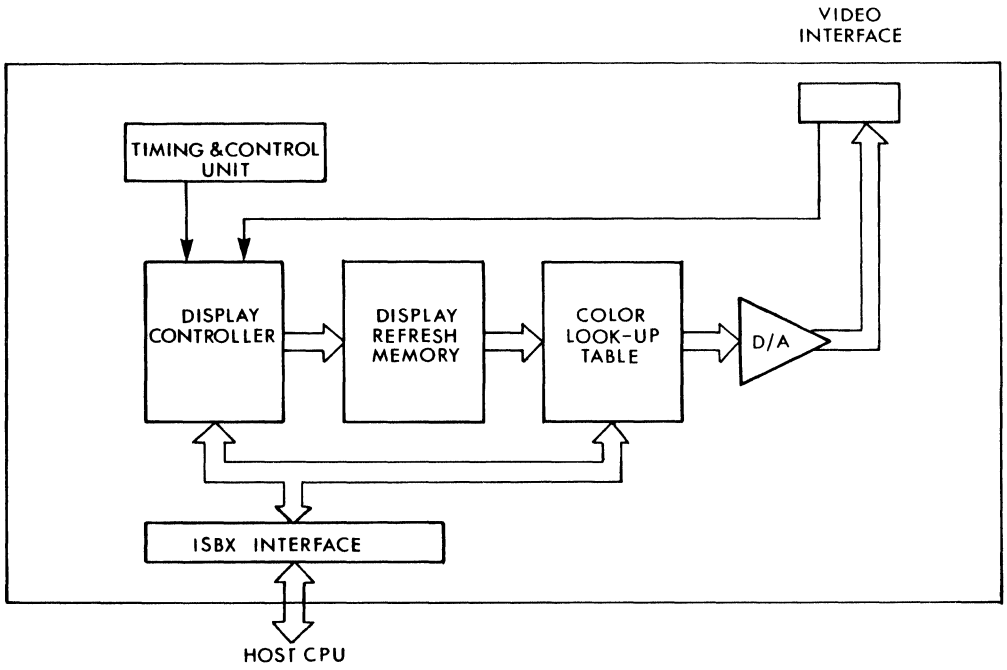



Figure 2. MSBX-800 functional blocks

## FUNCTIONAL DESCRIPTION

The MSBX-800 is a powerful, high resolution, graphics controller contained on a dual-width iSBX module. The MSBX-800 contains four major subsections (figure 2): the Graphics Display Controller, the Display Refresh Memory, the Color Look-up Table, and the iSBX Interface.

| CATEGORY | COMMAND | FUNCTION |
|---|---|---|
| Video Control | RESET | Reset the GDC to its idle state and specifies the display format. |
| | SYNC | Specifies the display format. |
| | VSYNC | Selects master or Slave video synchronization mode. |
| | CCHAR | Specifies the cursor and character row height. |
| Display Control | START | Starts the display scanning process. |
| | STOP | Blanks the display. |
| | CURS | Sets the position of the cursor in the display memory. |
| | PRAM | Defines the starting addresses and length of the display areas and specifies the eight bytes for the graphics character. |
| | PITCH | Specifies the width of the X dimension of the display memory. |
| Drawing Control | WDAT | Writes data words or bytes into the display memory. |
| | MASK | Sets the mask register contents. |
| | FIGS | Specifies the parameters of the drawing process. |
| | FIGD | Draws the figure as specified by FIGS. |
| | GCHRD | Draws the graphics character into the display memory,. |
| Data Read | RDAT | Reads data words or bytes from the display memory. |
| | CURD | Reads the cursor position. |
| | LPRD | Reads the light pen address. |

Table 1. MSBX-800 instruction set

## DISPLAY MEMORY

The MSBX-800 contains 16 64K bit RAM chips, on-board, for a total display read/write memory of 1,042,176 bits (128K bytes). This memory area is divided into 4 bit planes (allowing up to 16 simultaneously displayable colors or grey levels) and can be configured, by the user, into a three dimensional array of up to 512 horizontal x 512 vertical pixels x 4 bits/pixel. The resolution capabilities of the MSBX-800 can be increased by sacrificing bit planes. This feature enables the user to configure the on-board read/write memory for 800 x 655 x 2 bits/pixel. By using 256K x 1 RAMs, a 512K byte display refresh memory can be implemented and read/write arrays of up to 800 x 655 pixels can be configured, with 4 bits/pixel.

## DISPLAY CONTROLLER

An on-board VLSI display controller chip is the heart of the MSBX-800. All of the display maintenance requirements (horizontal/vertical syncs and blanking) and the display memory refresh functions are provided by the Display Controller and are completely transparent to the user. Much of the low level display memory addressing is off-loaded from the host processor, by the Display Controller, reducing software overhead and increasing system throughput.

The MSBX-800 Display Controller recognizes a 17 instruction set, which simplifies programming of the display. The instruction set is divided into four major categories (Video Control, Display Control, Drawing Control, Data Read) and are shown in table 1.

**Display Organization** — The on-board Display Controller allows the user to configure the display memory for any display resolution format, so long as that format does not exceed the total available memory (128K bytes standard). The standard MSBX-800 can be configured for displays of 256 x 256, 512 x 256, 512 x 384, or 640 x 400 pixels with 4 bits per pixel, or 640 x 480 or 800 x 600 pixels using 2 bits/pixel. Optionally, using 256K RAMs, displays of up to 640 x 480 or 800 x 600 pixels by 4 bits/pixel can be programmed.

The Display Controller also generates all of the timing signals required by the CRT monitor (figure 3). These signals (horizontal sync, horizontal blanking, vertical sync, and vertical blanking) are user definable to allow the MSBX-800 to drive any

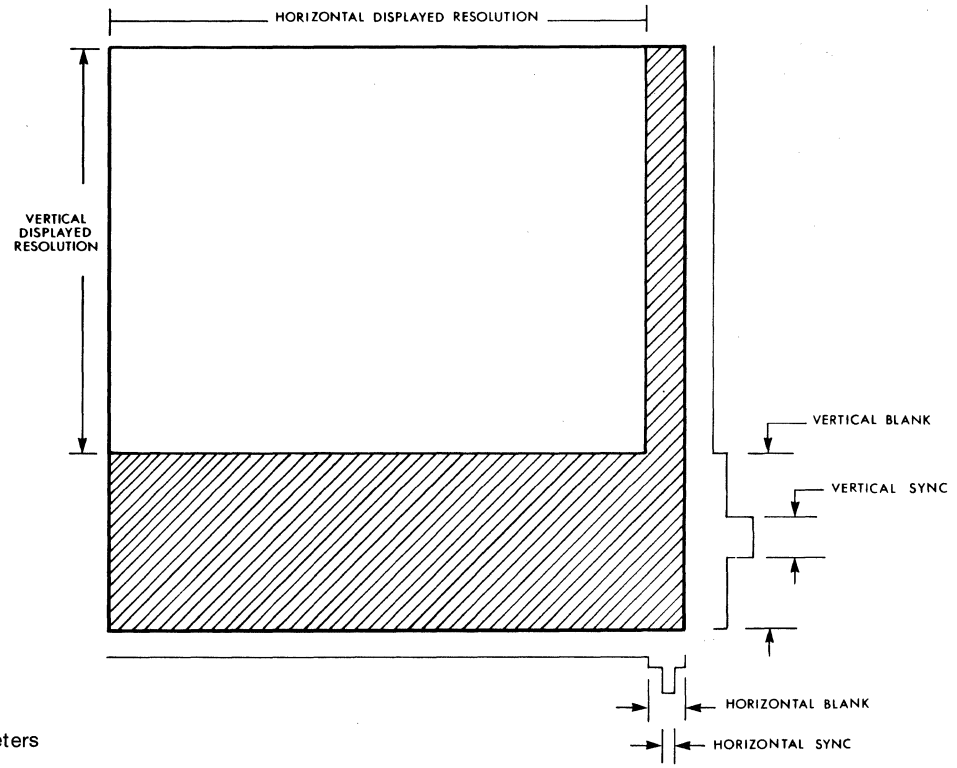



Figure 3. Display format parameters

analog RGB or monochrome video monitor. Sync frequencies can be defined to operate the system in either 50 Hz European or 60 Hz American Standard environments (interlaced or non-interlaced).

**Pan and Scroll** — The MSBX-800 allows the user to pan and/or scroll the generated graphics display. When using a small display format (i.e. 256 x 256 or 512 x 256) some of the available read/write display memory is not viewed on the screen. This "hidden" memory can be viewed by moving the CRT screen's "window" of the display memory either vertically or horizontally. Scrolling is accomplished on a line basis, for a "smooth" vertical image shift, while horizontal panning is done on 16-bit word boundaries.

**Split-Screen** — The CRT screen area can be divided into two, horizontally separate, independent display areas. The length of each area is independently user definable up to full screen. Note that the sum of the length of the two display areas can not exceed the total available screen area. Each display area can also be independently scrolled and/or panned.

**Figure Drawing** — The MSBX-800 features an ability to draw various graphics primitives with little or no assistance from the host CPU. Lines, arcs, circles, and rectangles can be constructed on the display by simply passing the figure's parameters to the MSBX-800. Calculation and generation of the addresses of the pixels, that make up the figure, are performed internally to the MSBX-800 and are transparent to the user. Area fills are also easily implemented using the MSBX-800.

The "texture" of the displayed figure (i.e. solid, dashed, or dotted) and the pattern of the area fill are also user programmable. The figure texture is defined by the user specified 16-bit texture pattern (figure 4) which represents those pixels, along the figure, which can be modified. A "1" in the texture pattern register will determine if the corresponding display memory bit is modified. The effect of writing to the display memory can produce one of four results, (replace, complement, set, or clear), selectable by the programmer. The Replace mode of writing to the display memory rewrites the contents of the memory with the contents of the texture register. Other writing modes available on the MSBX-800 allow the programmer to complement those bits in the display memory which correspond to 1s in the texture register, set the "modify-enabled" bits, or clear these bits. Likewise, the area fill pattern can be set by defining an 8 x 8 recurring matrix.

Characters can also be drawn to the graphics display, in any position and orientation, with a minimum of host CPU overhead. A character is drawn by first downloading an 8 x 8 pattern matrix, for that character, to the MSBX-800. Upon receipt of a character draw command, the GDC will then draw the character, pixel by pixel, to the display memory at the cursor position. Using this technique, any character (upper/lower case alphanumerics or special graphics symbol) can be drawn to the display.

## BLINK

Selected areas of the graphics image generated by the MSBX-800 can be set to blink, under software control, at a blink rate

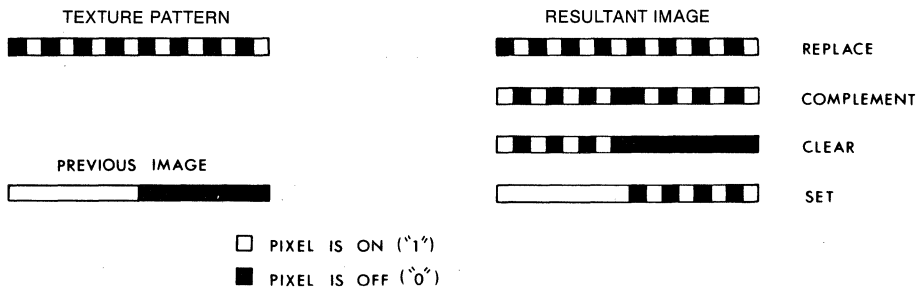



Figure 4. MSBX-800 "texture" pattern control

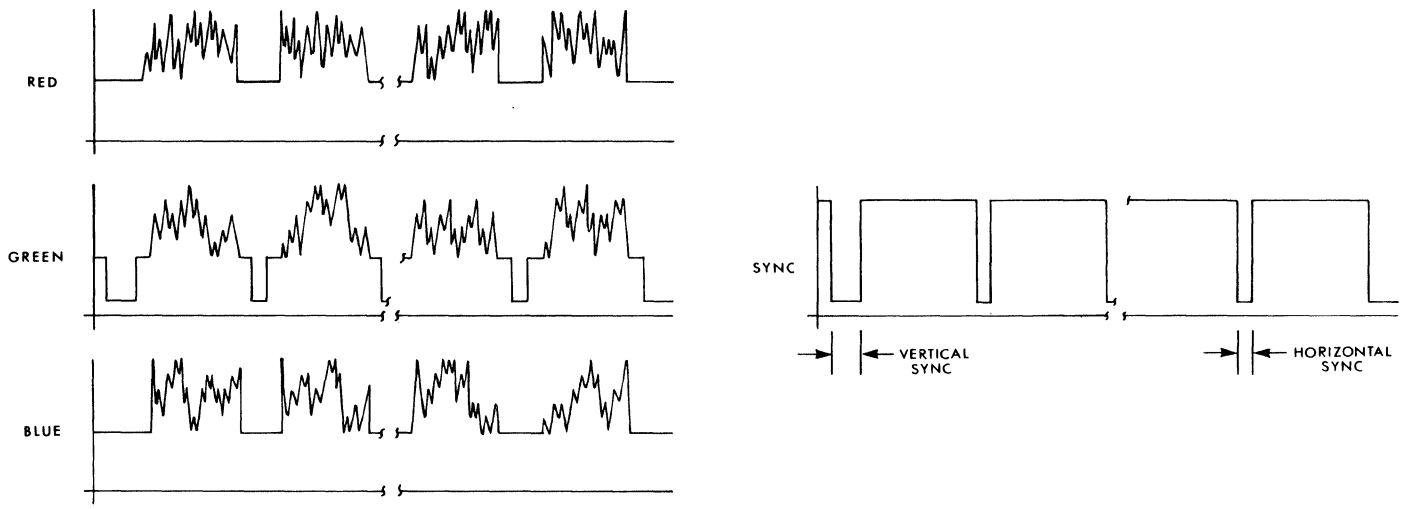



Figure 5. MSBX-800 video output signals

of 1.8 Hz. Setting the Blink Enable bit in the on-board Control Register causes any image data stored on bit plane 3 to toggle between two colors. The colors, from which and to which this data will blink, are defined by the user when the color look-up table is loaded.

### COLOR LOOK-UP TABLE

The MSBX-800 contains an on-board color look-up table which looks, to the user, like a 16 x 12 bit RAM. Through this look-up table, displays with up to 16 colors can be accommodated; with the displayed colors being user selected from a palette of 4096 colors. The color look-up table can be rewritten at any time.

The color look-up table allows the user to create a wide variety of video effects. Manipulation of the color look-up table allows the generation of such high performance effects as animation.

### TIMING AND CONTROL UNIT

The MSBX-800 contains an on-board 20 MHz clock which is the heart for the module's Timing and Control Unit. The Timing and Control Unit, using the 20 MHz crystal together with a pair of PALs* (Programmable Array Logic), supplies all of the individual functional blocks of the MSBX-800 with their required timing inputs and synchronizes their operation for maximum throughput. This proprietary Matrox circuit also enables the MSBX-800 to generate displays of up to 800 x 655 x 4 bits per pixel using an average drawing speed of 1.6 μsec./pixel/plane. Optional 10.0, 11.66, and 13.33 MHz crystals are available, together with on-board strap-selectable divide by 2 and divide by 4 circuitry, to enable the MSBX-800 to accommodate video timing parameters for display formats ranging from 256 x 256 to 800 x 600 (see SPECIFICATIONS).

### VIDEO INTERFACE

The output video signals are supplied, via a 12-pin header on the module, as analog ($1V_{p-p}$) RGB signals (figure 5). Sync and blanking signals are provided either combined with the Green video output or as a separate composite signal.

### LIGHT PEN INTERFACE

User interaction with the display is enabled through a light pen interface. The MSBX-800 latches the address of the word, pointed to by the light pen, and makes this information available to the host processor. An interrupt is generated on-board the MSBX-800 which can signal the host processor that light pen data is available. A "blue flood" feature is incorporated on the MSBX-800 to facilitate the use of a light pen. The light

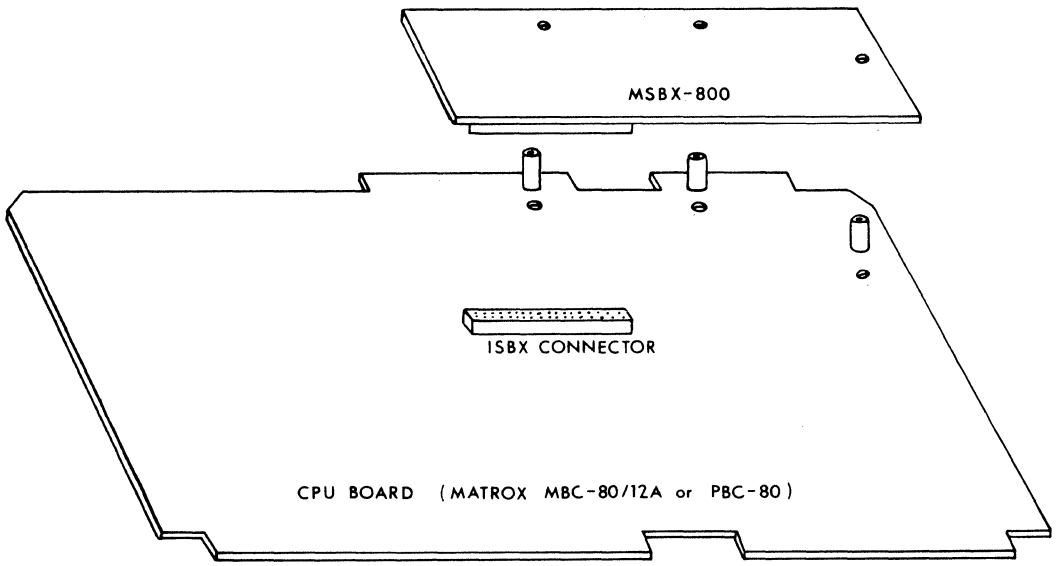



Figure 6. Mounting the MSBX-800

| LOCATION | READ | WRITE |
|---|---|---|
| 0 | Read Status Register | Write Parameter into FIFO Buffer |
| 1 | Read FIFO Command Buffer | Write Command into FIFO Buffer |
| 2 | Read Board Status | Write Control Register |
| 4 | Not Used | Write Color Look-Up Table (Green and Blue) |
| 6 | Not Used | Write Color Look-Up Table (Red) |

Table 2. MSBX-800 register definitions

pen is interfaced, to the MSBX-800, via the 12-pin video interface connector.

### iSBX INTERFACE

The MSBX-800 interfaces directly to the iSBX bus and meets all iSBX bus specifications as laid out in the Intel Specification No. 142686-001. To the host computer, the MSBX-800 looks like a group of five 8-bit registers which can be strapped anywhere in the host's I/O address space. Reading locations 0 and 1, will read the Display Controller's Status and FIFO Read buffer respectively (table 2). Writing to these locations will transfer either a command byte (location 1) or a parameter byte (location 0) to the MSBX-800 FIFO. Writing to I/O port 2 (Control Register) sets various control parameters for the board, i.e. Blue Flood Enable and Blink Enable, and also loads the address for the next Color Look-Up Table write instruction. Reading this port allows the user to monitor the status of the Light Pen Enable signal and the Horizontal Blank. The remaining two registers are used to write the Color Look-Up Table.

### MOUNTING

The MSBX-800 can be mounted on any microcomputer board which has on-board facilities for at least one double-width iSBX Multimodule. The module is secured to the host board by two threaded nylon spacers, which are supplied with the MSBX-800. Figure 6 shows how the MSBX-800 would mount on a typical iSBX-equipped Multibus CPU card (e.g. Matrox MBC-86/12A, Intel iSBC 86/30 (8086), Matrox PBC-80 (Z-80A), etc.).

### PROGRAMMING

The MSBX-800 simplifies the programmer's task in generating a graphics display by performing much of the calculational overhead involved in producing a graphics image. All of the repetitive, low-level accesses to the display memory (pixel addresses) are handled internally to the MSBX-800. The programmer, then, creates the graphics image as a combination of graphics primitives (lines, arcs, circles, etc). These primitives are invoked by passing the appropriate instruction to the MSBX-800 accompanied by the necessary parameters (eg. to draw a line the parameters required include the direction of the vector, the length of the vector, etc.). An on-board 16 byte FIFO instruction buffer allows the programmer to pipeline commands for greater system throughput.

### USER DEFINABLE RESOLUTIONS

The display format, used by the MSBX-800, is initialized by writing a Reset command (see table 1) to the board's FIFO command buffer, followed by eight bytes of video format parameter data. The desired format is expressed by defining the number of horizontally displayed dots (expressed as an integer number of 16-bit words), the number of vertically displayed lines, and the horizontal and vertical sync parameters (front and back porch widths, and sync signal widths). Also included as a Reset parameter is an 8-bit Mode of Operation descriptor which defines whether the resultant display will be interlaced or non-interlaced, and whether drawing will be restricted to retrace only or allowed to occur at any time. A Sync command is also recognized by the MSBX-800 and can

| PIN | MNEMONIC | DESCRIPTION | | PIN | MNEMONIC | DESCRIPTION |
|---|---|---|---|---|---|---|
| 1 | — | Not Used | | 2 | — | Not Used |
| 3 | GND | Signal Ground | | 4 | +5V | +5 Volts |
| 5 | RESET | Reset | | 6 | — | Not Used |
| 7 | MA2 | Address Line 2 | | 8 | MPST/ | Board Present Output |
| 9 | MA1 | Address Line 1 | | 10 | — | Not Used |
| 11 | MA0 | Address Line 0 | | 12 | MINTR1 | Interrupt Line 1 |
| 13 | IOWRT/ | I/O Write Command | | 14 | MINTR0 | Interrupt Line 0 |
| 15 | IORD/ | I/O Read Command | | 16 | — | Not Used |
| 17 | GND | Signal Ground | | 18 | +5V | +5 Volts |
| 19 | MD7 | Data Line 7 | | 20 | — | Not Used |
| 21 | MD6 | Data Line 6 | | 22 | MCS0/ | Chip Select |
| 23 | MD5 | Data Line 5 | | 24 | — | Not Used |
| 25 | MD4 | Data Line 4 | | 26 | — | Not Used |
| 27 | MD3 | Data Line 3 | | 28 | — | Not Used |
| 29 | MD2 | Data Line 2 | | 30 | — | Not Used |
| 31 | MD1 | Data Line 1 | | 32 | MDACK/ | Reserved |
| 33 | MD0 | Data Line 0 | | 34 | MDRQT | Reserved |
| 35 | GND | Signal Ground | | 36 | +5V | +5 Volts |

Table 3. MSBX-800 Address, data, and control lines

be used, followed by the same parameter bytes as the Reset command, to dynamically change the display format without reinitializing the board. The Sync command can also be used alone (with no parameter bytes) to blank the screen for "all time" drawing (drawing can occur during active video as well as during retrace blanking). Note that "all time" drawing may result in streaking on the display.

Another command (PRAM), followed by up to 16 bytes of parameters, is used to define the starting address and length of the image areas on the display (up to two independent display image areas can be maintained by the MSBX-800). The PRAM parameters also define the 16-bit vector "texture" pattern and the 8 x 8 character (or area fill) pattern.

## INTERFACING THE MSBX-800 TO OTHER COMPUTER SYSTEMS

Aside from mounting on a CPU board, equipped with a standard iSBX Multimodule connector, the MSBX-800 can also be easily interfaced to any computer via a parallel port which emulates the iSBX standard (figure 7). The small size of the MSBX-800 enables the board to be mounted either within the host computer chassis, in a separate box, or even within the CRT monitor housing. Table 3 outlines the address, data, and control lines required by the MSBX-800.

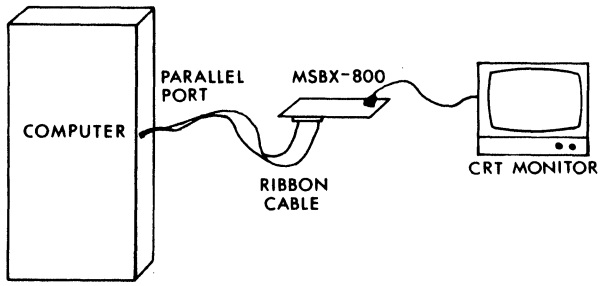



Figure 7. Interfacing the MSBX-800 via a parallel port

# SPECIFICATIONS

## FUNCTIONAL

### DISPLAY PARAMETERS

| ON-BOARD RAM | READ/WRITE AREA | RESOLUTION | BITS/PIXEL | CLOCK FREQUENCY | |
|---|---|---|---|---|---|
| | | | | INTERLACED | NON-INTERLACED |
| 128K | 512 x 512 | 256 x 256 | 4 | — | 5.8 MHz |
| 128K | 512 x 512 | 512 x 256 | 4 | — | 11.6 MHz |
| 128K | 512 x 512 | 512 x 384 | 4 | 10.0 MHz | 20.0 MHz |
| 128K | 512 x 512 | 512 x 480 | 4 | 10.0 MHz | 20.0 MHz |
| 128K | 640 x 400 | 640 x 400 | 4 | 13.3 MHz | 20.0 MHz |
| 128K | 800 x 655 | 640 x 480 | 2 | 13.3 MHz | — |
| 128K | 800 x 655 | 800 x 600 | 2 | 20.0 MHz | — |
| 512K | 1024 x 1024 | 640 x 480 | 4 | 13.3 MHz | — |
| 512K | 1024 x 1024 | 800 x 600 | 4 | 20.0 MHz | — |

Note 1: To obtain 640 x 480 x 4 or 800 x 600 x 4 display resolution, 256K RAM parts must be used.
Note 2: Divide by 2 and divide by 4 circuitry is included for obtaining the given clock frequencies using standard crystal oscillators.

### VIDEO TIMING

For a display format of 512 horizontal dots x 384 vertical lines, the following video parameters must be programmed. The table gives the parameters for both American and European systems using either Interlaced or Non-Interlaced Video formats.

| | AMERICAN | | EUROPEAN | |
|---|---|---|---|---|
| | INTERLACED | NON-INTERLACED | INTERLACED | NON-INTERLACED |
| Active Video | 51.2 μs | 25.6 μs | 51.2 μs | 25.6 μs |
| Horizontal Sync Frequency | 16.02 KHz | 28.4 KHz | 16.02 KHz | 28.4 KHz |
| Horizontal Sync Width | 6.4 μs | 3.2 μs | 6.4 μs | 3.2 μs |
| Vertical Sync Frequency | 30.01 Hz | 60.06 Hz | 25.04 Hz | 50.01 Hz |
| Vertical Sync Width | 249.6 μs | 105.6 μs | 249.6 μs | 105.6 μs |

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### INPUT SIGNALS

Light Pen Enable
Light Pen Strobe

### OUTPUT SIGNALS

Analog Video: Red
Green (composite)
Blue
Composite Sync

### BUS INTERFACE

Address, data, and control lines conform to the Intel iSBX bus Specification No. 142686-001
Command and Status Registers — Selectable on any 8 byte I/O address boundary — 000 — FFFH
— Detailed information on the MSBX-800 command set is available in the 7220 GDC manual.

### CONNECTORS

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 36-pin iSBX connector — iSBX-bus Interface | Intel iSBX Connector (female) |
| J1: 12-pin header — Video Interface | JS TERMINAL CORP. #H12P-SHF-AA |
| — Light Pen Interface | |

## PHYSICAL

### SIZE

Width: 7.5 in. (19.05 cm)
Height: 3.2 in. ( 9.24 cm)
Depth: 0.8 in. ( 2.05 cm)

### POWER REQUIREMENTS

+5V dc ±5% @ 1.8A (MSBX-800/64)
+5V dc ±5% @ 2.5A (MSBX-800/256)

### ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0°C to 55°C
Relative Humidity: 0 — 95% non-condensing

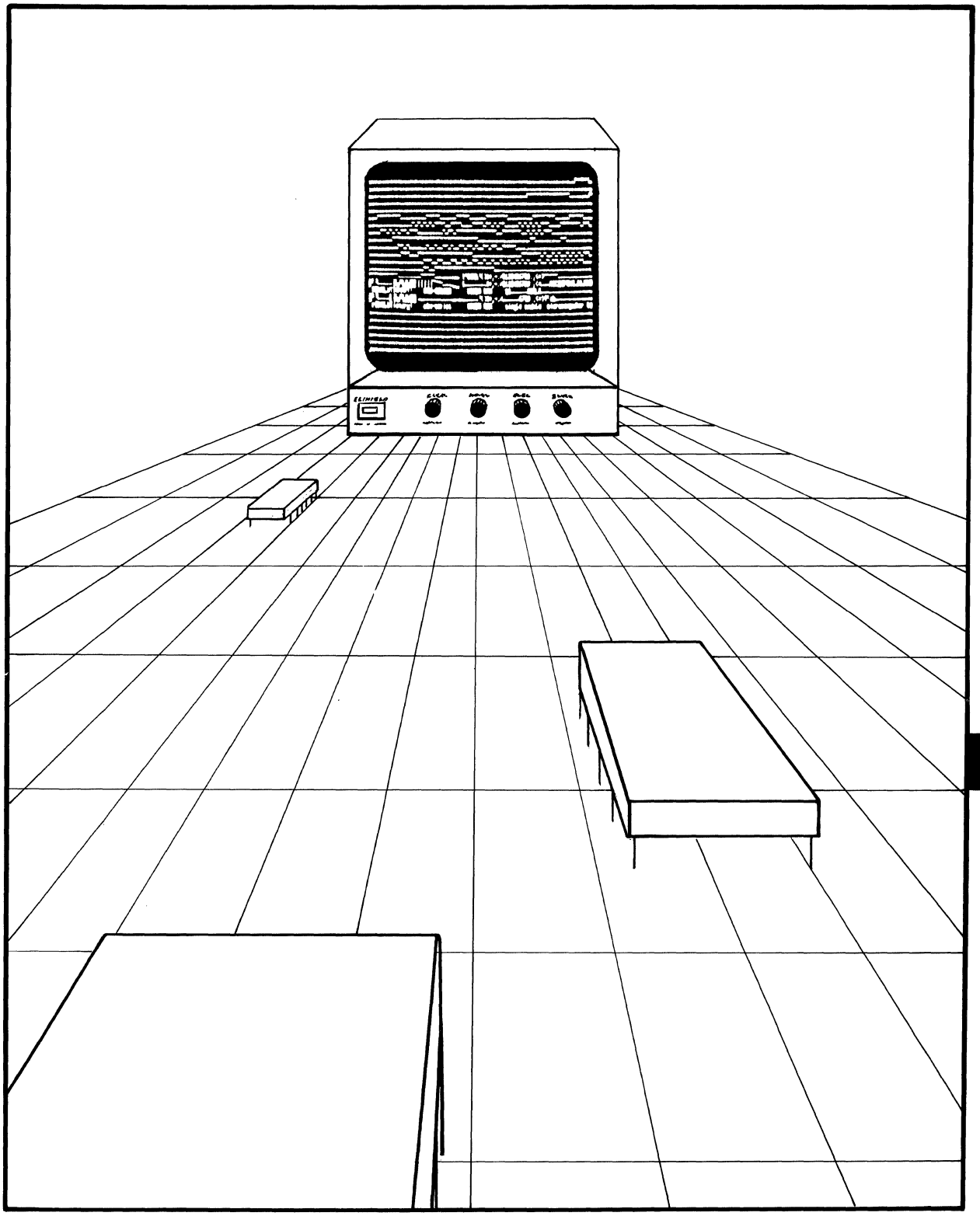
### ORDERING INFORMATION

MSBX-800 / XXX — High resolution iSBX Multimodule (uses 20 MHz crystal)

- 64 — uses 64K RAMs
- 256 — uses 256K RAMs

### SUPPORT PRODUCTS

| | |
|---|---|
| XTAL | 10.000 MHz |
| XTAL | 11.666 MHz |
| XTAL | 13.333 MHz |



8

# VIDEO CONTROLLER MODULES

## SECTION 8 VIDEO CONTROLLER MODULES

**matrox**
**electronic systems ltd.**
*5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA*
*TEL.: 514—735-1182* *TELEX: 05-825651*

# MTX-816

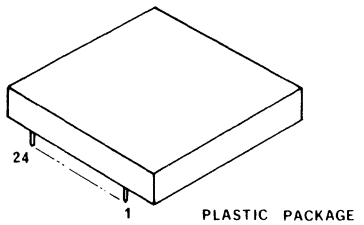
## MTX TV CRT CONTROLLER FAMILY

*HYBRID*
*(MOS, TTL)*
*8x16 ASCII Character*
*VIDEO RANDOM ACCESS MEMORY*

### 8x16 VIDEO RANDOM ACCESS MEMORY

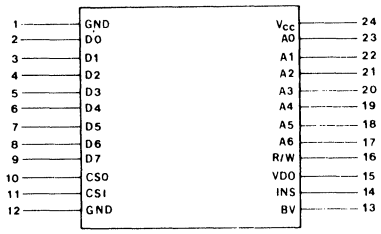
The MTX-816 is a TV CRT controller designed for use in systems that require display of alphanumeric data. On the input side the device is directly connected to bus organized systems and looks like a 128x8 RAM. The output is a video signal which directly drives a TV monitor to provide an 8x16 field of 128 ASCII characters.

- **organized as 128x8 RAM**
- **8x16 display field**
- **bidirectional data bus**
- **CMOS/TTL compatible**
- **access time <1 usec**
- **flicker free display**
- **single +5V power supply**
- **low power <800 mW**
- **ASCII font standard (5x7)**
- **standard video output**
- **drives up to 25 TV monitors**
- **electronic intensity control**



PLASTIC PACKAGE

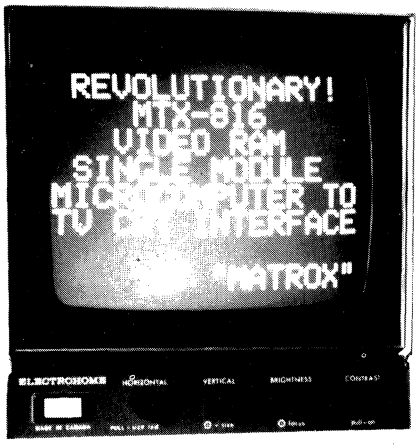
PIN ASSIGNMENT

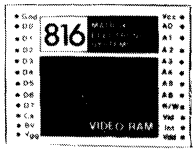



### ABSOLUTE MAXIMUM RATINGS

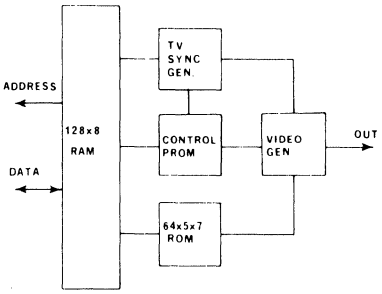
| | | | |
|---|---|---|---|
| Supply Voltage | Vcc | –0.3 to +7 | Vdc |
| Input Voltage | Vin | –0.3 to Vcc | Vdc |
| Operating Temp. | TA | 0 to 70 | °C |
| Storage Temp. | Tsta | –55 to 150 | °C |
| Lead Solder Temp. | TSD | +400 | °C |

TYPICAL APPLICATION




MTX-816 VIDEO RAM
BLOCK DIAGRAM



## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

### RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | Vdc |
| Temperature | $T_A$ | 0 | 25 | 70 | C |
| Power Dissipation | $P_D$ | 700 | 800 | 1200 | mW |
| Input High Voltage | $V_{IH}$ | 3.5 | — | Vcc | Vdc |
| Input Low Voltage | $V_{IL}$ | 0 | — | 0.8 | Vdc |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Input Current (An, R/W, CS) | $I_{IN}$ | — | — | 10 | pAdc |
| Input High Threshold | $V_{IHT}$ | 2.0 | — | — | Vdc |
| Input Low Threshold | $V_{ILT}$ | — | — | 0.8 | Vdc |
| Output High Voltage | $V_{OH}$ | 2.4 | — | — | Vdc |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | Vdc |
| Output Leakage (D0—D7) | $I_{LOH,L}$ | — | — | 10 | $\mu$Adc |
| Output Current (High) | $I_{OH}$ | — | — | –100 | $\mu$A |
| Output Current (Low) | $I_{OL}$ | — | — | 0.8 | mA |
| Supply Current (+5V) | $I_{CC}$ | — | 160 | 200 | mAdc |

### CAPACITANCE

| CHARACTERISTIC | SYMBOL | MAX. | UNIT |
|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 15 | pF |
| Output Capacitance | $C_{OUT}$ | 15 | pF |

All MTX-816 inputs are CMOS equivalent (CD4000 or MC14000 family or equivalent).

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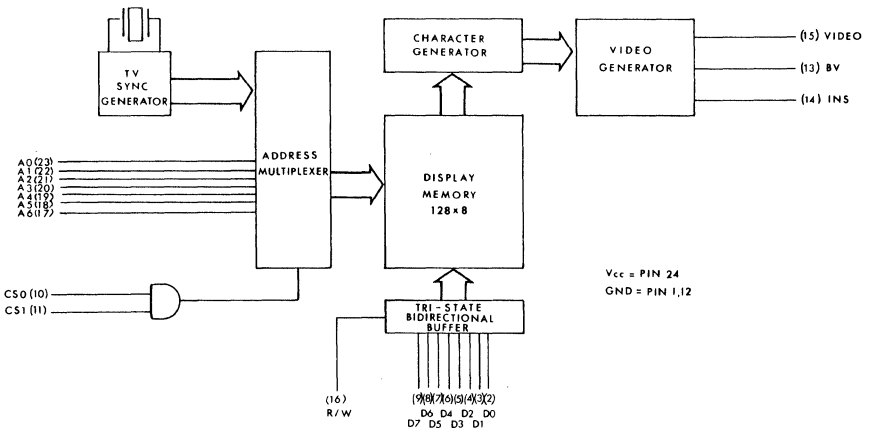
### FUNCTIONAL DESCRIPTION

The MTX-816 is a TV CRT controller module which generates a video signal that can directly drive any standard TV monitor. The display is 128 ASCII alphanumeric characters arranged in an 8x16 matrix. Characters are displayed white on a black background. Intensity control pin allows electronic control of the brightness of the whole field. It can also be used for blanking of the screen during a read/write operation or for flashing.

On the input side, the MTX-816 looks like an ordinary 128x8 RAM and can be directly connected to the address and data bus of any bus organized system.

The MTX-816 is particularly suitable for use in microcomputer systems due to low cost, small size, high speed, low power requirement, and no additional interface circuitry.



## AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

### RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | UNIT |
|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 0 | ns |
| Address Hold time | $t_{AH}$ | 0 | ns |

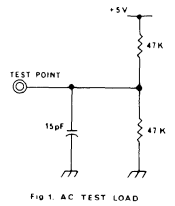
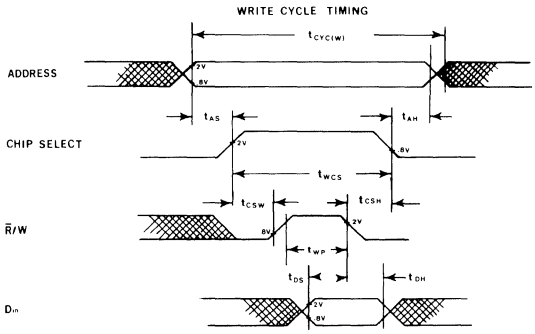


Fig 1. AC TEST LOAD

### WRITE CYCLE

(All timing with rise time/fall time = 20ns,)
(Load of Fig. 1)

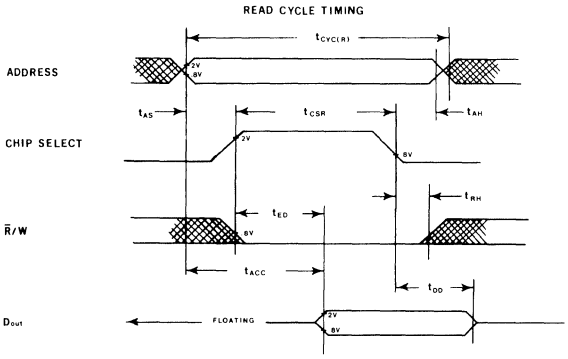
| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | $t_{CYC(W)}$ | 900 | — | ns |
| Write Chip Select Width | $t_{WCS}$ | 800 | — | ns |
| CS to Write Setup Time | $t_{CSW}$ | 400 | — | ns |
| Write Pulse Width | $t_{WP}$ | 400 | — | ns |
| Chip Select Hold Time | $t_{CSH}$ | 0 | — | ns |
| Data Setup Time | $t_{DS}$ | 350 | — | ns |
| Data Hold Time | $t_{DH}$ | 100 | — | ns |



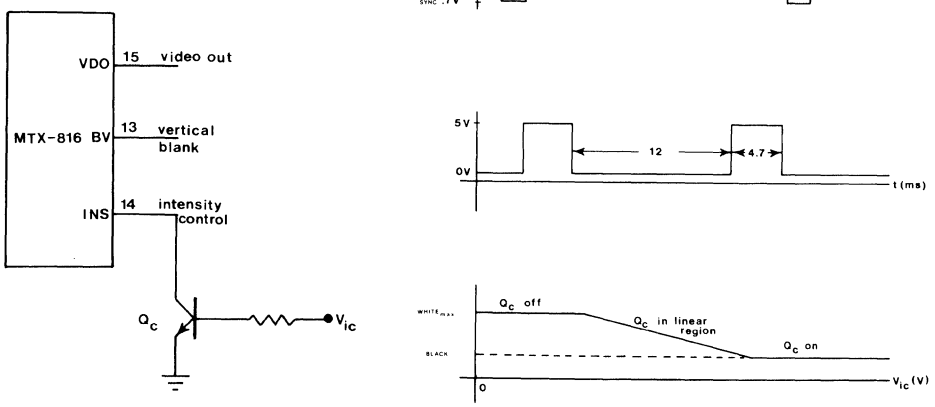

### READ CYCLE

(All timing with rise time/fall time = 20ns,)
(Load of Fig. 1)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | $t_{CYC(R)}$ | 975 | — | ns |
| Read Chip Select Width | $t_{CSR}$ | 975 | — | ns |
| Read Access Time | $t_{ACC}$ | — | 975 | ns |
| Output Enable Delay | $t_{ED}$ | — | 975 | ns |
| Output Disable Delay | $t_{DD}$ | 30 | 150 | ns |
| Read Hold Time | $t_{RH}$ | 150 | — | ns |




### VIDEO OUTPUTS




Sync. frequency
Horizontal: 15.840 kHz
Vertical: 60 Hz/50 Hz
Crystal controlled.
Output impedance: 75 ohms
Short circuit protection built in.

BV signal can be used as a flag to access VRAM during vertical retrace only. (no flicker during access).
BV drive current (max.)
.1 mA source
.25 mA sink.

Pin 14 open - white max.
Pin 14 ground - no video (black)
INS input allows electronic control of the brightness of the whole field.

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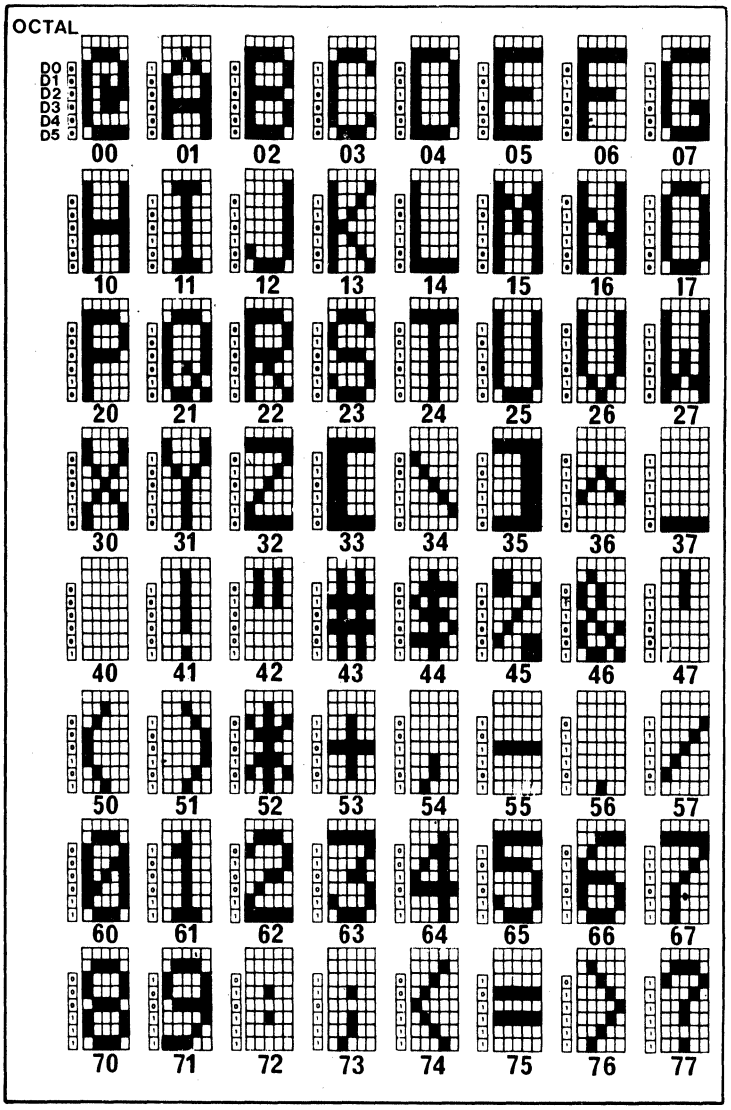
## ASCII CHARACTER FONT




## SCREEN DISPLAY ORGANISATION

| ROW | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | | | | | | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | |
| 3 | | | | | | | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | |
| 6 | | | | | | | | | | | | | | | | |
| 7 | | | | | | | | | | | | | | | | |

COLUMN

CHARACTER POSITION ADDRESS

| ROW | | | COLUMN | | | |
|---|---|---|---|---|---|---|
| A6 | A5 | A4 | A3 | A2 | A1 | A0 |

DATA

| X | X | ASCII CHARACTER | | | | | | X DON'T CARE |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

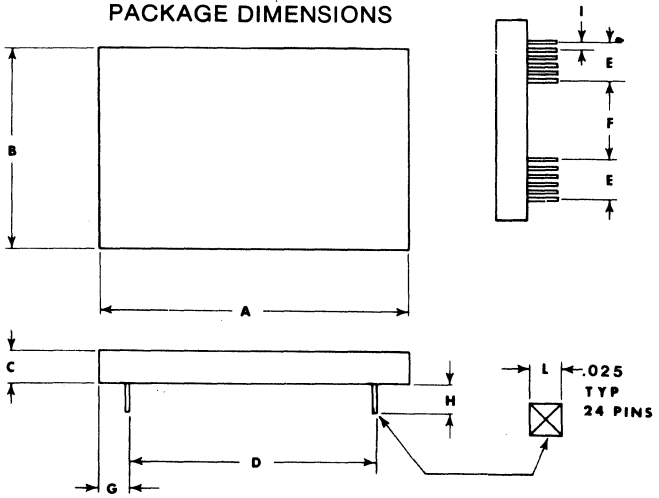
BITS D7 AND D6 NOT USED FOR VIDEO DISPLAY

## ORDERING INFORMATION

MTX-816–X X

AS—American standard (60 Hz)
ES—European standard (50 Hz)

## PACKAGE DIMENSIONS




MODULE CASE IS ISOLATED ALLOWING ETCH RUNS UNDERNEATH.

| DIM | CM | | INCHES | |
|---|---|---|---|---|
| | NOM. | TOL. | NOM. | TOL. |
| A | 11.191 | .02 | 4.406 | .01 |
| B | 8.331 | .02 | 3.280 | .01 |
| C | 1.549 | .02 | .610 | .01 |
| D | 9.957 | .02 | 3.920 | .01 |
| E | 1.270 | .02 | .500 | .01 |
| F | 2.540 | .02 | 1.000 | .01 |
| G | .587 | .02 | .235 | .01 |
| H | .432 | .02 | .170 | .01 |
| I | .254 | .007 | .100 | .003 |
| L | .063 | .002 | .025 | .001 |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

# MTX-1632

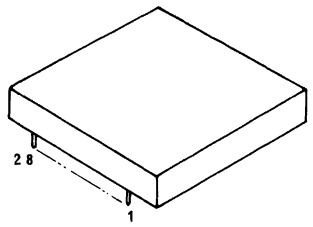
## MTX TV CRT CONTROLLER FAMILY

*HYBRID*
*(MOS, TTL)*
*16x32 ASCII Character*
*VIDEO RANDOM ACCESS MEMORY*

16x32 VIDEO RANDOM ACCESS MEMORY

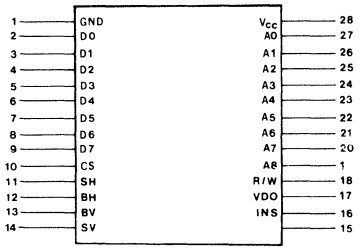
The MTX-1632 is a TV CRT controller designed for use in systems that require display of alphanumeric data. On the input side the device is directly connected to bus organized systems and looks like a 512x8 RAM. The output is a video signal which directly drives a TV monitor to provide a 16x32 field of 512 ASCII characters.

- **organized as 512x8 RAM**
- **16x32 display field**
- **bidirectional data bus**
- **TTL compatible**
- **access time < 550 ns**
- **flicker free display**
- **single + 5V power supply**
- **low power**
- **ASCII font standard (7x9)**
- **standard video output**
- **drives up to 25 TV monitors**
- **character blinking**
- **electronic intensity control**




PLASTIC PACKAGE

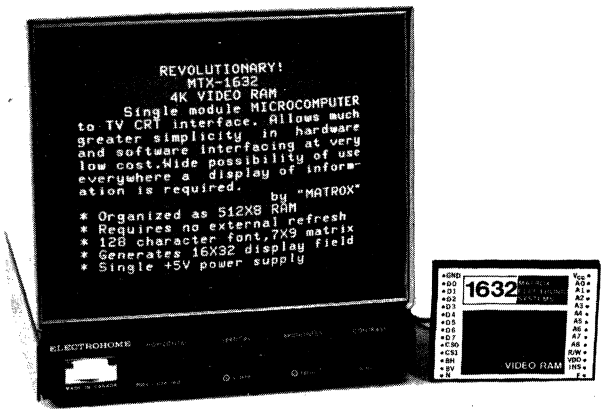
PIN ASSIGNMENT



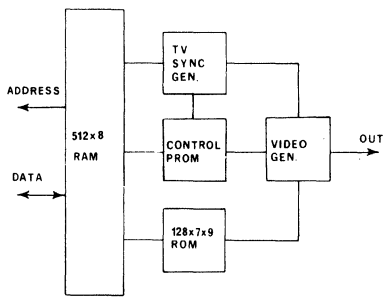

**ABSOLUTE MAXIMUM RATINGS**

| | | | |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to + 6 | Vdc |
| Input Voltage | Vin | -0.3 to Vcc | Vdc |
| Operating Temp. | $T_A$ | 0 to 70 | °C |
| Storage Temp. | $T_{sta}$ | -55 to 125 | °C |
| Lead Solder Temp | $T_{SD}$ | + 400 | °C |

TYPICAL APPLICATION




MTX-1632 VIDEO RAM
BLOCK DIAGRAM




8

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

### RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | Vdc |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ | Vdc |
| Input Low Voltage | $V_{IL}$ | O | | 0.7 | Vdc |

SH(pin 11) is horizontal sync.
Low = 5.8 $\mu$s,
High = 58.3 $\mu$s

SV(pin 14) is vertical sync.
Low = .256 ms
High = 16.41 ms

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Input Current (High) | $I_{IN}$ | | | 20 | $\mu$A |
| Input Current (Low) | $I_{IN}$ | — | — | -0.4 | mA |
| Output Current (High) | $I_{OH}$ | | — | -400 | $\mu$A |
| Output Current (Low) | $I_{OL}$ | — | — | 8 | mA |
| Output High Voltage | $V_{OH}$ | 2.4 | 3.4 | — | Vdc |
| Output Low Voltage | $V_{OL}$ | — | 0.3 | 0.5 | Vdc |
| Output Leakage (D0—D7) | $I_{LOH,L}$ | — | — | 20 | $\mu$A |
| Output Current (High) D0—D7 | $I_{OH}$ | — | — | -2.6 | mA |
| Output Current (Low) D0—D7 | $I_{OL}$ | — | — | 24 | mA |
| Supply Current (.5V) | $I_{CC}$ | — | 400 | 600 | mA |

### CAPACITANCE

| CHARACTERISTIC | SYMBOL | MAX. | UNIT |
|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 15 | pF |
| Output Capacitance | $C_{OUT}$ | 15 | pF |

Note: All MTX-1632 inputs are TTL equivalent (74LSxxx family or equivalent).

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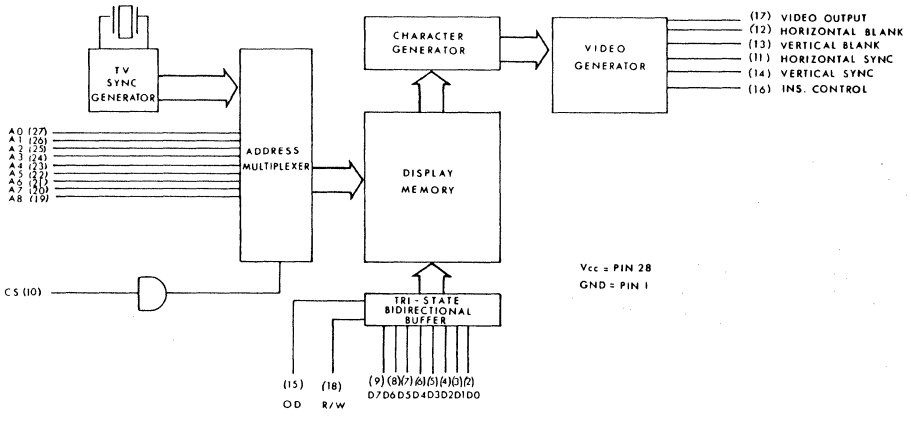
### FUNCTIONAL DESCRIPTION

The MTX-1632 is a TV CRT controller which generates a video signal that can directly drive any standard TV monitor. The display is 512 ASCII alphanumeric characters arranged in 16x32 matrix. Characters are displayed white on a black background. Intensity control pin allows electronic control of the brightness of the whole field. It can also be used for blanking of the screen during a read/write operation or for flashing.

On the input side, the MTX-1632 looks like an ordinary 512x8 RAM and can be directly connected to the address and data bus of any bus organized system.

The MTX-1632 is particularly suitable for use in microcomputer systems due to low cost, small size, high speed, low power requirement, and no additional interface circuitry.



## AC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted)

### RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | UNIT |
|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 0 | ns |
| Address Hold Time | $t_{AH}$ | 0 | ns |

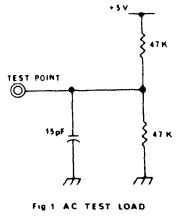
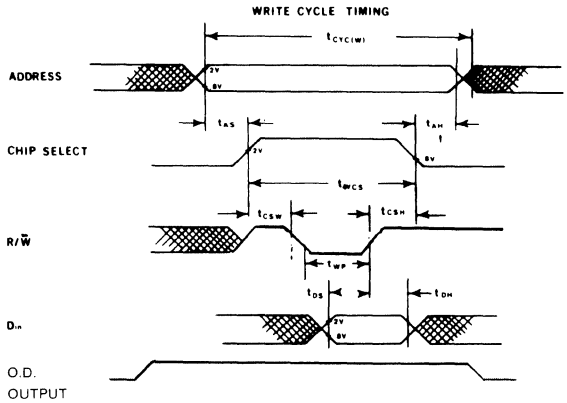


Fig 1 AC TEST LOAD

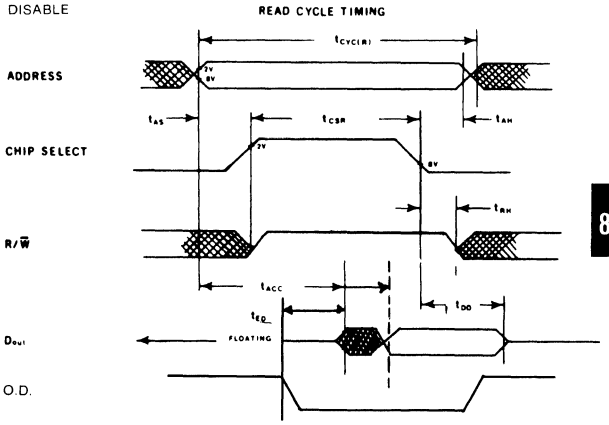
### WRITE CYCLE
(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | $t_{CYC(W)}$ | 565 | — | ns |
| Write Chip Select Width | $t_{WCS}$ | 565 | — | ns |
| CS to Write Setup Time | $t_{CSW}$ | 240 | — | ns |
| Write Pulse Width | $t_{WP}$ | 250 | — | ns |
| Chip Select Hold Time | $t_{CSH}$ | 75 | — | ns |
| Data Setup Time | $t_{DS}$ | 250 | — | ns |
| Data Hold Time | $t_{DH}$ | 40 | — | ns |

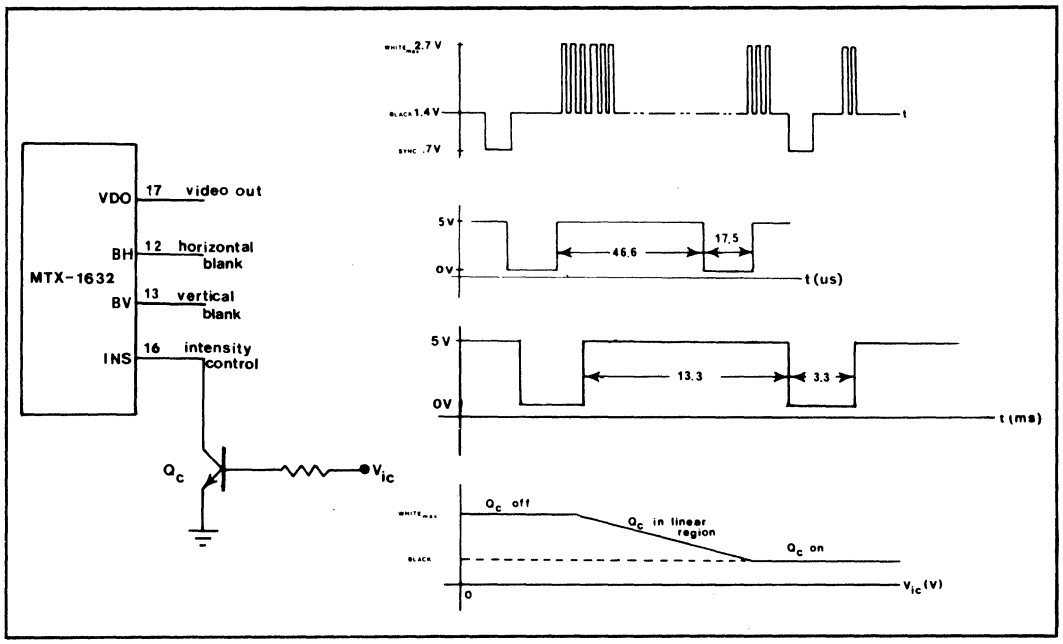



### READ CYCLE
(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | $t_{CYC(R)}$ | 550 | — | ns |
| Read Chip Select Width | $t_{CSR}$ | 550 | — | ns |
| Read Access Time | $t_{ACC}$ | — | 550 | ns |
| Output Enable Delay | $t_{ED}$ | — | 50 | ns |
| Output Disable Delay | $t_{DD}$ | | 50 | ns |
| Read Hold Time | $t_{RH}$ | 0 | — | ns |




**$\overline{\text{WRITE}}$ PULSE SWITCHES TRANCEIVERS FROM $\mu$P TO VRAM (WRITE)**
**$\overline{\text{O.D.}}$ PULSE SWITCHES TRANCEIVERS TO $\mu$P FROM VRAM (READ)**




Sync. frequency
Horizontal: 15.600 kHz
Vertical: 60 Hz/50 Hz
Crystal controlled.
Output impedance: 75 ohms
Short circuit protection built in.

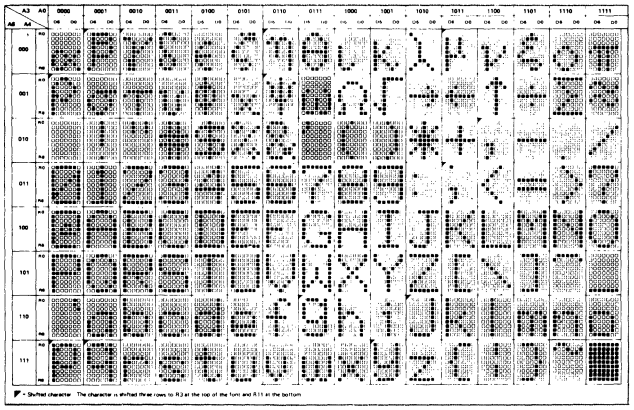
BH or BV signal can be used as a flag to access VRAM during horizontal or vertical retrace only.
(No flicker during access)

Pin 16 open - white max.
Pin 16 ground - no video (black)
INS input allows electronic control of the brightness of the whole field.

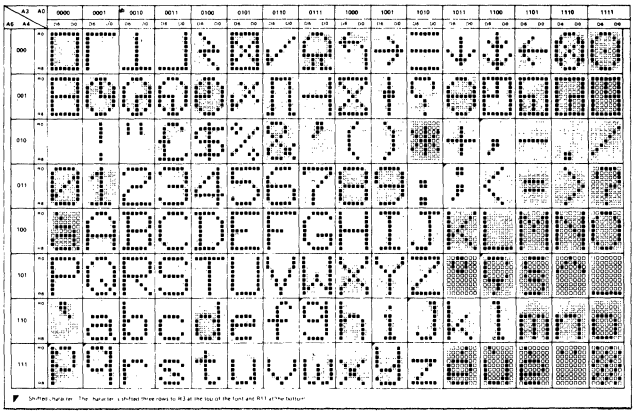
8

## ASCII CHARACTER FONT

MTX-1632 A

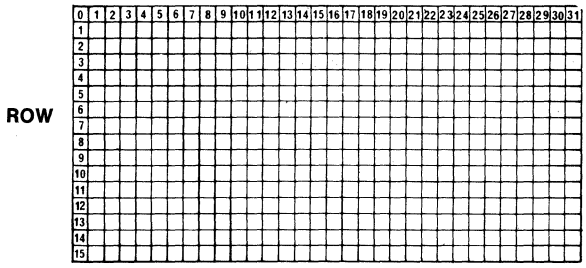


MTX-1632 B



Additional character fonts are available from stock.
Custom made font (128 characters in 7x9 matrix) available at extra cost.

## SCREEN DISPLAY ORGANIZATION




CHARACTER POSITION ADDRESS

ROW | COLUMN

| A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|

DATA

X | ASCII CHARACTER

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

D0-D6 ...character

D7 ...blink bit
0...normal
1...character
flashing at 1 Hz

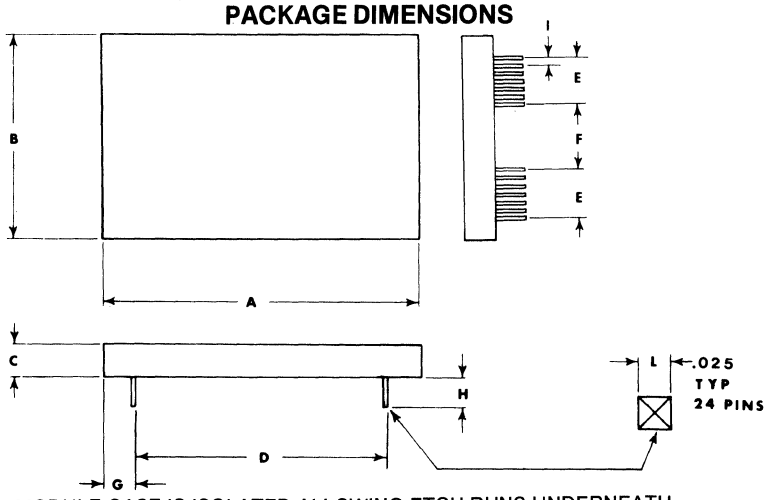
**ORDERING INFORMATION**

**MTX-1632—X X**

- A—American standard (60 Hz)
- E—European standard (50 Hz)

- A—Character set A (see ASCII CHARACTER FONT)
- B—Character set B (see ASCII CHARACTER FONT)
- G—German character set
- J—Japanese character set

## PACKAGE DIMENSIONS




| DIM | MM | | INCHES | |
|---|---|---|---|---|
| | NOM. | TOL. | NOM. | TOL. |
| A | 114.300 | .254 | 4.500 | .01 |
| B | 101.600 | .254 | 4.000 | .01 |
| C | 12.700 | .254 | .50 | .01 |
| D | 99.568 | .254 | 3.920 | .01 |
| E | 15.240 | .254 | .600 | .01 |
| F | 20.320 | .254 | .800 | .01 |
| G | 7.366 | .254 | .29 | .01 |
| H | 4.318 | .254 | .170 | .01 |
| I | 2.540 | .076 | .100 | .003 |
| L | .635 | .025 | .025 | .001 |

MODULE CASE IS ISOLATED ALLOWING ETCH RUNS UNDERNEATH.

**matrox**
**electronic systems ltd.**
*5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA*
*TEL.: 514-735-1182* *TELEX: 05-825651*

# MTX-1632SL

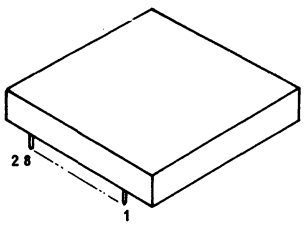
## MTX TV CRT CONTROLLER FAMILY

*HYBRID*
*(MOS, TTL)*
*16x32 ASCII Character*
*VIDEO RANDOM ACCESS MEMORY*

### EXTERNALLY SYNCHRONIZED 16x32 VIDEO RANDOM ACCESS MEMORY

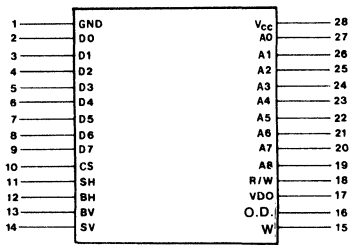
The MTX-1632SL is a TV CRT controller designed for use in systems that require display of alphanumeric data. On the input side the device is directly connected to bus organized systems and looks like a 512x8 RAM. The output is a video signal which directly drives a TV monitor to provide a 16x32 field of 512 ASCII characters. The device can be slave locked to an external source (TV sync. generator).

- **external synchronization**
- **organized as 512x8 RAM**
- **16x32 display field**
- **bidirectional data bus**
- **TTL compatible**
- **access time < 550 ns**
- **flicker free display**
- **broadcasting applications**
- **single + 5V power supply**
- **low power**
- **ASCII font standard (7x9)**
- **standard video output**
- **drives up to 25 TV monitors**
- **character blinking**




PLASTIC PACKAGE

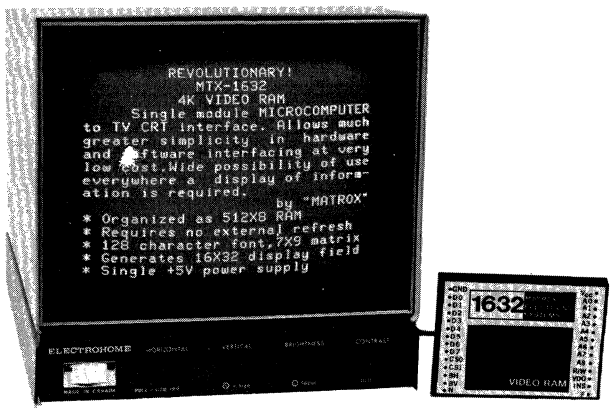
PIN ASSIGNMENT



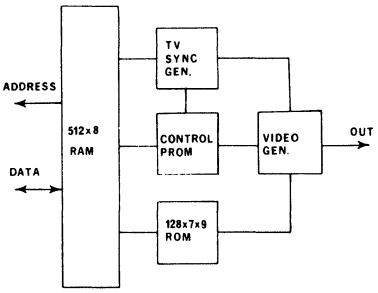

### ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to + 6 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to Vcc | Vdc |
| Operating Temp. | $T_A$ | 0 to 70 | °C |
| Storage Temp. | $T_{sta}$ | -55 to 125 | °C |
| Lead Solder Temp | $T_{SD}$ | + 400 | °C |

TYPICAL APPLICATION




MTX-1632 VIDEO RAM
BLOCK DIAGRAM

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FEBRUARY 1982

***MATROX products covered by Canadian and foreign patent and/or patent pending.**

DS-402-01

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

### RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | Vdc |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ | Vdc |
| Input Low Voltage | $V_{IL}$ | 0 | | 0.7 | Vdc |

SH (pin 11) is horizontal sync. input
positive TTL pulse
1 $\mu$s min. 8$\mu$s max.
f min. = 15 KHz, f max = 17 KHz

SV (pin 14) is vertical sync. input
positive TTL pulse
150 $\mu$s min. 1ms max.
f min. = 45 Hz, f max. = 65 Hz

W (pin 15) is video only output
TTL level, no sync. added

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Input Current (High) | $I_{IN}$ | | | 20 | $\mu$A |
| Input Current (Low) | $I_{IN}$ | — | — | -0.4 | mA |
| Output Current (High) | $I_{OH}$ | | — | -400 | $\mu$A |
| Output Current (Low) | $I_{OL}$ | — | — | 8 | mA |
| Output High Voltage | $V_{OH}$ | 2.4 | 3.4 | — | Vdc |
| Output Low Voltage | $V_{OL}$ | — | 0.3 | 0.5 | Vdc |
| Output Leakage (D0—D7) | $I_{LOH,L}$ | — | — | 20 | $\mu$A |
| Output Current (High) D0—D7 | $I_{OH}$ | — | — | -2.6 | mA |
| Output Current (Low) D0—D7 | $I_{OL}$ | — | — | 24 | mA |
| Supply Current (.5V) | $I_{CC}$ | — | 400 | 600 | mA |

### CAPACITANCE

| CHARACTERISTIC | SYMBOL | MAX. | UNIT |
|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 15 | pF |
| Output Capacitance | $C_{OUT}$ | 15 | pF |

Note: All MTX-1632SL inputs are TTL equivalent (74LSxxx family or equivalent).

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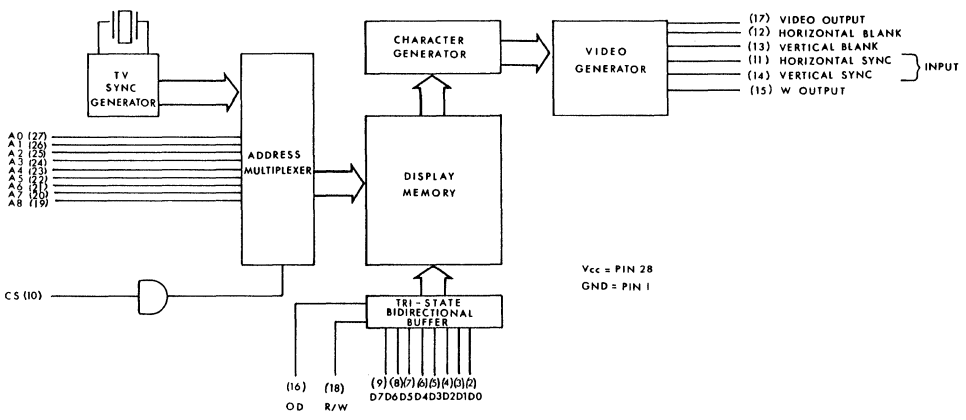
### FUNCTIONAL DESCRIPTION

The MTX-1632SL is a TV CRT controller module which generates a video signal that can directly drive any standard TV monitor. The display is 512 ASCII alphanumeric characters arranged in 16x32 matrix. Characters are displayed white on a black background. Intensity control pin allows electronic control of the brightness of the whole field. It can also be used for blanking of the screen during a read/write operation or for flashing.

The MTX-1632SL can be slave locked to an external sync. source. This feature allows the MTX-1632SL to be used in broadcasting (mixing with video from a TV camera, any standard TV system can be used as a sync. source). The device can be also used together with graphics VRAM MMD-256 to obtain full graphic/alphanumeric capability.

On the input side, the MTX-1632SL looks like an ordinary 512x8 RAM and can be directly connected to the address and data bus of any bus organized system.

The MTX-1632SL is particularly suitable for use in microcomputer systems due to low cost, small size, high speed, low power requirement, and no additional interface circuitry.



## AC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted)

### RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | UNIT |
|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 0 | ns |
| Address Hold Time | $t_{AH}$ | 0 | ns |

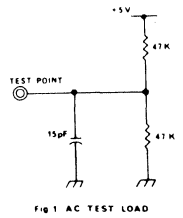
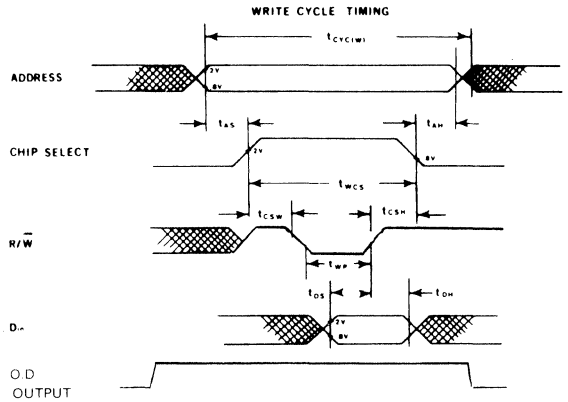


Fig 1 AC TEST LOAD

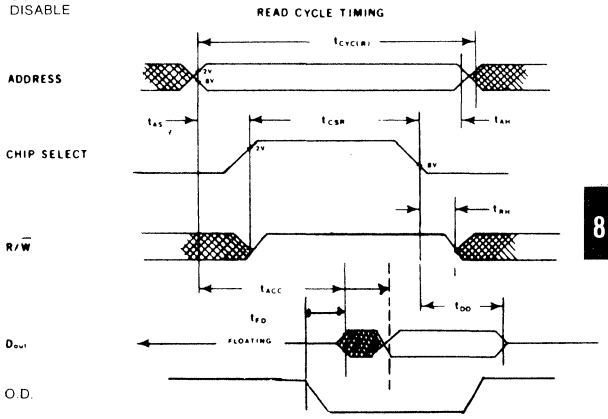
### WRITE CYCLE
(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | †CYC(W) | 565 | — | ns |
| Write Chip Select Width | †WCS | 565 | — | ns |
| CS to Write Setup Time | †CSW | 240 | — | ns |
| Write Pulse Width | †WP | 250 | — | ns |
| Chip Select Hold Time | †CSH | 75 | — | ns |
| Data Setup Time | †DS | 250 | — | ns |
| Data Hold Time | †DH | 40 | — | ns |

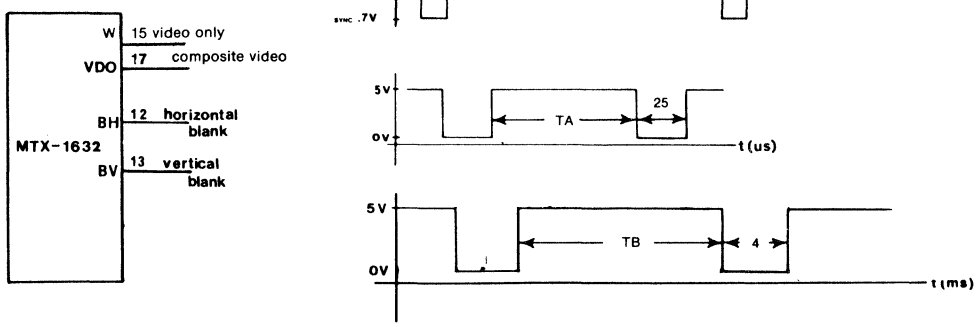



### READ CYCLE
(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | †CYC(R) | 550 | — | ns |
| Read Chip Select Width | †CSR | 550 | — | ns |
| Read Access Time | †ACC | — | 550 | ns |
| Output Enable Delay | †ED | — | 50 | ns |
| Output Disable Delay | †DD | | 50 | ns |
| Read Hold Time | †RH | 0 | — | ns |




**WRITE PULSE SWITCHES TRANCEIVERS FROM μP TO VRAM (WRITE)**
**O.D. PULSE SWITCHES TRANCEIVERS TO μP FROM VRAM (READ)**



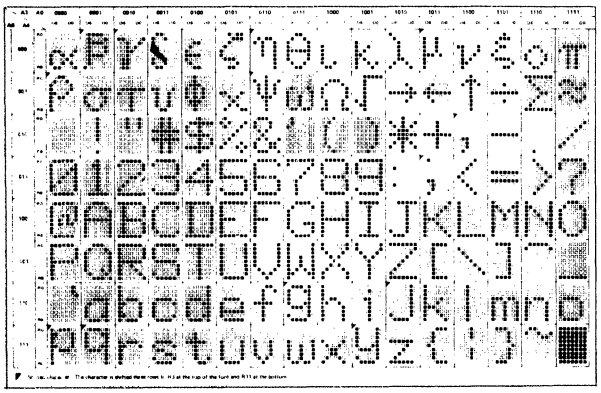

W is video only output. Can be used for mixing with other video signals. Composite video (VDO). Output impedance: 75 ohms. Short circuit protection built in.

BH or BV signal can be used as a flag to access VRAM during horizontal or vertical retrace only. (No flicker during access) TA, TB depend on external sync.

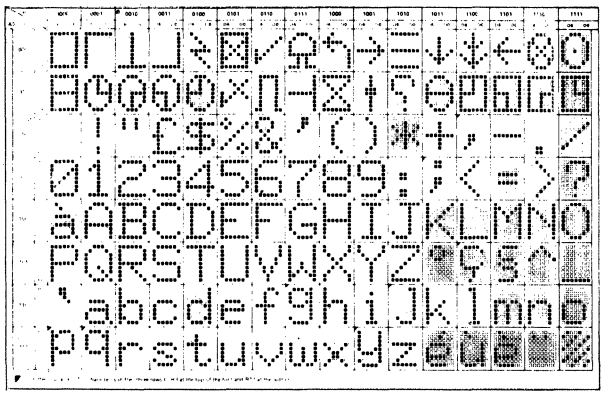
8

## ASCII CHARACTER FONT

MTX-1632 SL-A



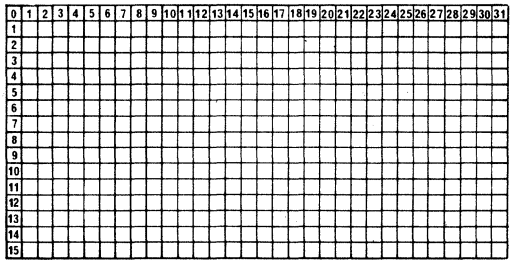
MTX-1632 SL-B



Additional character fonts are available from stock.
Custom made font (128 characters in 7x9 matrix) available at extra cost.

## SCREEN DISPLAY ORGANIZATION

ROW




COLUMN

CHARACTER POSITION ADDRESS
ROW | COLUMN

| A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|

DATA
X | ASCII CHARACTER

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

D0-D6 ...character
D7 ...blink bit
0...normal
1...character flashing at 1 Hz

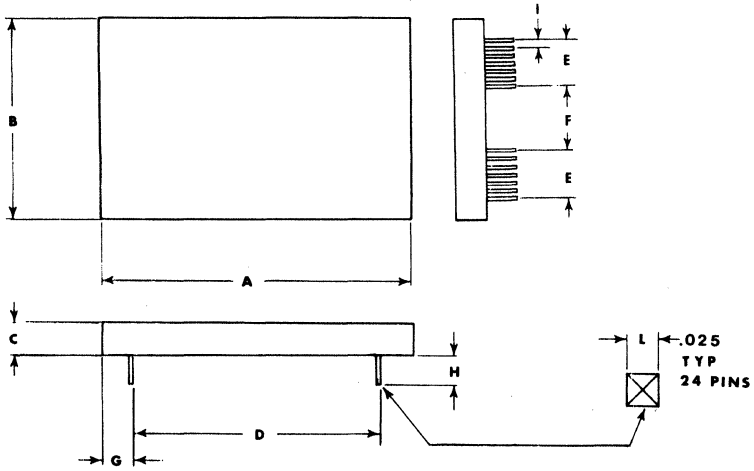
**ORDERING INFORMATION**

**MTX-1632SL—X X**

- A—American standard (60 Hz)
- E—European standard (50 Hz)

- A—Character set A (see ASCII CHARACTER FONT)
- B—Character set B (see ASCII CHARACTER FONT)
- G—German character set
- J—Japanese character set

## PACKAGE DIMENSIONS




| DIM | MM | | INCHES | |
|---|---|---|---|---|
| | NOM. | TOL. | NOM. | TOL. |
| A | 114.300 | .254 | 4.500 | .01 |
| B | 101.600 | .254 | 4.000 | .01 |
| C | 12.700 | .254 | .50 | .01 |
| D | 99.568 | .254 | 3.920 | .01 |
| E | 15.240 | .254 | .600 | .01 |
| F | 20.320 | .254 | .800 | .01 |
| G | 7.366 | .254 | .29 | .01 |
| H | 4.318 | .254 | .170 | .01 |
| I | 2.540 | .076 | .100 | .003 |
| L | .635 | .025 | .025 | .001 |

MODULE CASE IS ISOLATED ALLOWING ETCH RUNS UNDERNEATH.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

# PV-1

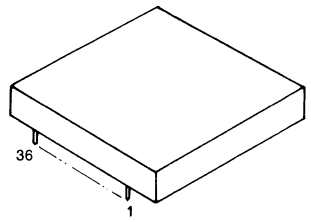
## MTX TV CRT CONTROLLER FAMILY

*HYBRID*
*(MOS, TTL)*
*PROGRAMMABLE*
*VIDEO RANDOM ACCESS MEMORY*

### PROGRAMMABLE VIDEO RANDOM ACCESS MEMORY

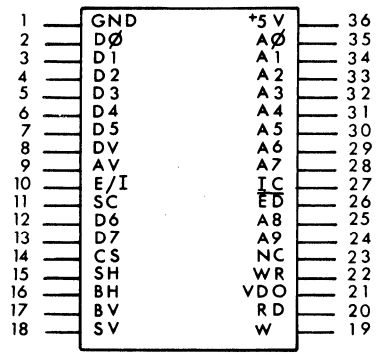
The PV-1 is a multiple format alphanumeric controller designed to satisfy the majority of users who have special display requirements. The module contains a programmable CRT controller with internal/external lock capability and all required circuitry to generate any screen format for up to 16 lines x 64 characters. On the input side the device is directly connected to any bus organized system and looks like a 1K x 8 RAM (500ns access). The output is a video signal which directly drives a TV monitor.

- **External/internal sync.**
- **Programmable display field**
- **8/16 columns**
- **8 to 64 rows**
- **Built-in 1K x 8 refresh RAM**
- **Access time 500ns**
- **Upper/lower case (7 x 9)**
- **Single +5V power supply**
- **American/European standard**
- **Standard video output**
- **Digital and analog video mixers built-in**
- **uP intensity control**
- **Character blink/inverse control**
- **Broadcast application**




**PLASTIC PACKAGE**

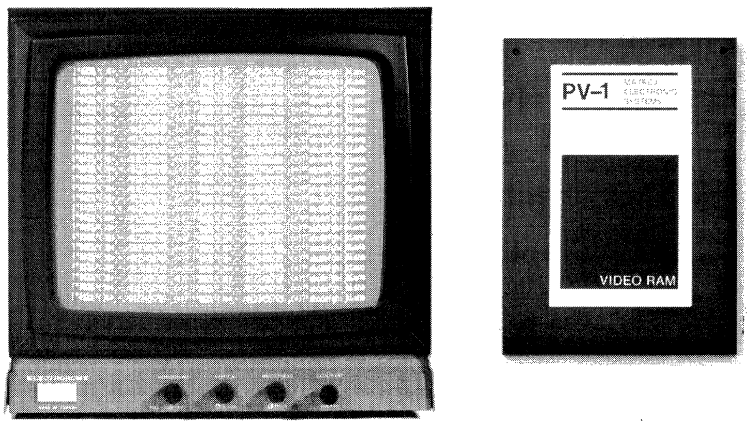
**PIN ASSIGNMENT**



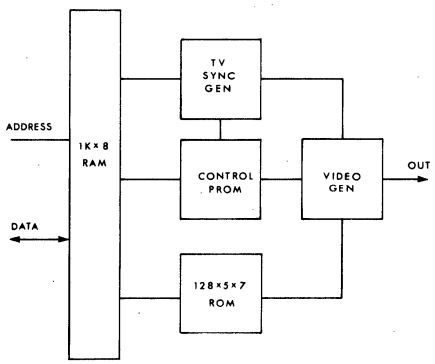

**ABSOLUTE MAXIMUM RATINGS**

| | | | |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +6 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to Vcc | Vdc |
| Operating Temp. | $T_A$ | 0 to 70 | °C |
| Storage Temp. | $T_{sta}$ | -55 to 125 | °C |
| Lead Solder Temp. | $T_{SD}$ | +400 | °C |

**TYPICAL APPLICATION**




**PV-1 VIDEO RAM BLOCK DIAGRAM**

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* MATROX products covered by Canadian and foreign patent and/or patent pending.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

### RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | Vdc |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ | Vdc |
| Input Low Voltage | $V_{IL}$ | 0 | | 0.7 | Vdc |

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Input Current (High) | $I_{in}$ | | | 20 | uA |
| Input Current (Low) | $I_{in}$ | — | — | -0.4 | mA |
| Output Current (High) | $I_{OH}$ | | — | -400 | uA |
| Output Current (Low) | $I_{OL}$ | — | — | 8 | mA |
| Output High Voltage | $V_{OH}$ | 2.4 | 3.4 | — | Vdc |
| Output Low Voltage | $V_{OL}$ | — | 0.3 | 0.5 | Vdc |
| Output Leakage (D0—D7) | $I_{LOH, L}$ | — | — | 20 | uAdc |
| Output Current (High) D0—D7 | $I_{OH}$ | — | — | -2.6 | mAdc |
| Output Current (Low) D0—D7 | $I_{OL}$ | — | — | 24 | mA |
| Supply Current (.5V) | $I_{CC}$ | — | 400 | 600 | mAdc |

E/I (pin 10) External/Internal sync mode control
External = high; Internal = low

SC (pin 11) Composite sync input/output
Direction controlled by E/I pin

SH (pin 15) Horizontal sync input/output

SV (pin 18) Vertical sync input/output

W (pin 19) TTL digital video only output

ED (pin 26) Video enable control
High will disable video portion of composite video, low enables video

DV (pin 8) Digital input to video mixer

AV (pin 9) Analog video input to video mixer

### CAPACITANCE

| CHARACTERISTIC | SYMBOL | MAX. | UNIT |
|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 15 | pF |
| Output Capacitance | $C_{OUT}$ | 15 | pF |

Note: All PV-1 inputs are TTL equivalent (74LSxxx family or equivalent).

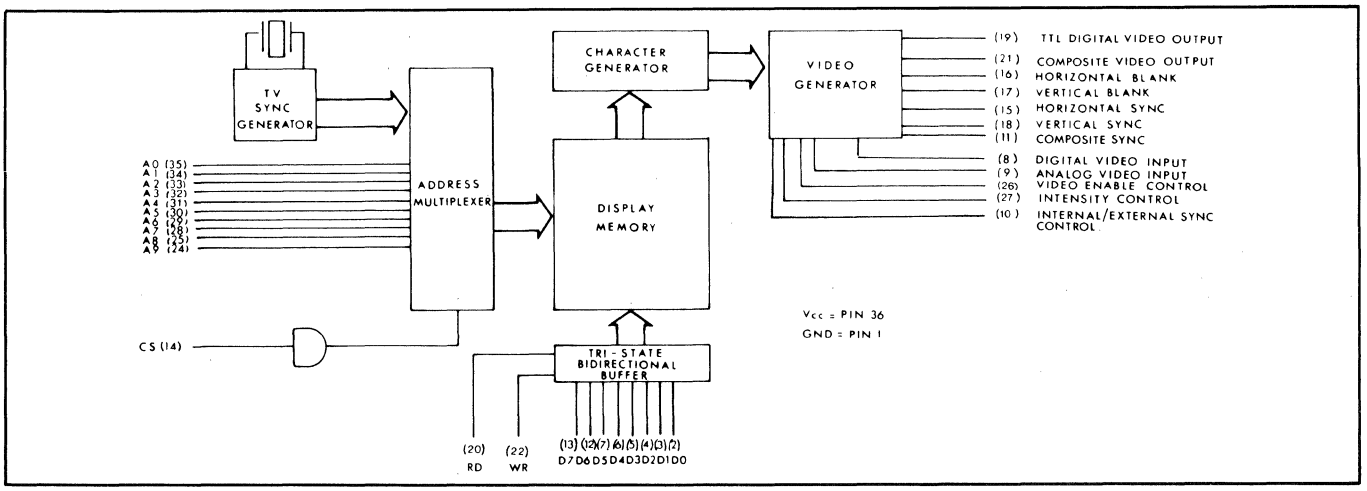
8

### FUNCTIONAL DESCRIPTION

The PV-1 is a programmable TV CRT controller which generates a video signal that can drive directly any standard TV monitor. By changing on-board straps any display format using 8 or 16 lines and 8 to 64 characters per line can be accommodated. Characters are displayed white on a black background. An intensity control pin allows electronic control of the brightness of the whole field. This pin can be used for blanking of the screen during a read/write operation or for flashing.

The PV-1 can be slave locked to an external sync. source. This feature allows the PV-1 to be used in broadcasting (mixing with video from a TV camera, any standard TV system can be used as the sync. source). The device can also be used together with a graphics VRAM (MMD-256) to obtain full alphanumeric/graphic capabilities.

The PV-1 is particularly suitable for use in microcomputer systems due to low cost, small size, high speed, low power requirement, and no additional interface circuitry.



## AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

### RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | UNIT |
|---|---|---|---|
| Address Setup Time | tAS | 0 | ns |
| Address Hold Time | tAH | 0 | ns |

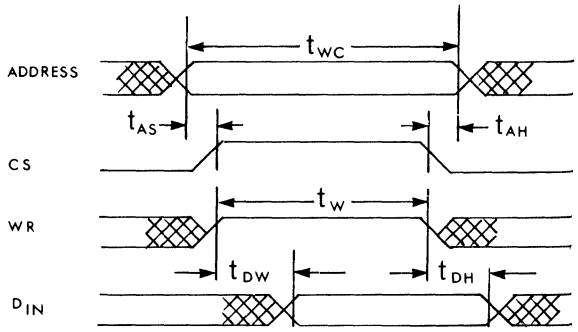
### WRITE CYCLE (All timing with rise time/fall time = 20ns)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | tWC | 500 | - | NS |
| Write Time | tW | 200 | - | NS |
| Data to Write Time Overlap | tDW | 200 | - | NS |
| Data Hold From Write Time | tDH | 0 | - | NS |

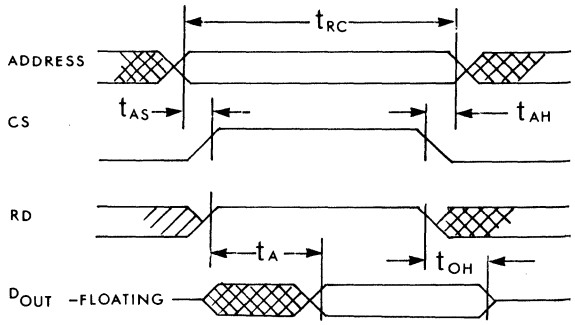
### READ CYCLE (All timing with rise time/fall time = 20ns)

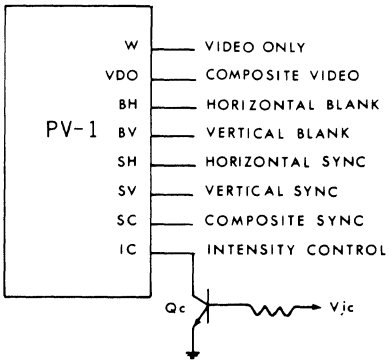
| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | tRC | 500 | - | NS |
| Access Time | tA | - | 500 | NS |
| Output Hold Time | tOH | - | 10 | NS |

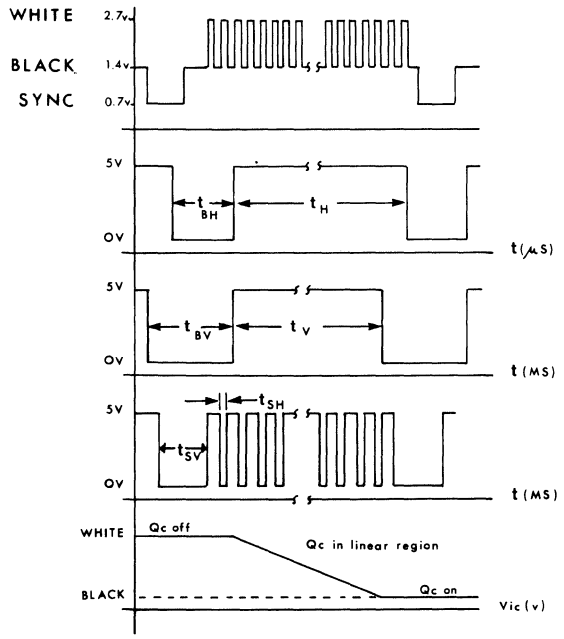
WRITE CYCLE TIMING




READ CYCLE TIMING




W is Digital Video only output. Can be used for mixing with other video signals. Composite video (VDO). Output impedence: 75 Short circuit protection built-in.

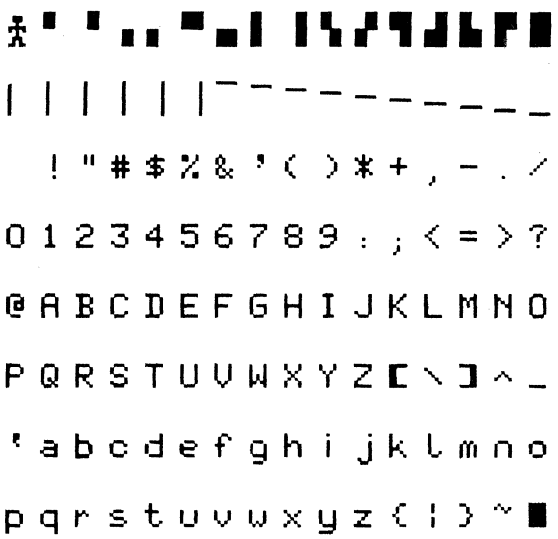
BH or BV signal can be used as a flag to access VRAM during horizontal or vertical blanking only. (No flicker during access)

SH, SV and SC output the horizontal sync., vertical sync. and composite sync. respectively. If PV-1 is used in the External sync. mode, these pins are used as inputs to lock the device to an external source.

IC allows electronic control of the brightness of the whole field.
Pin 27 open - white
Pin 27 ground - black

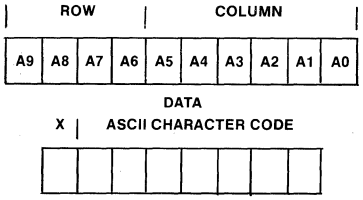
## CHARACTER FONT

MCH-01 (MATROX STANDARD 2716 EPROM)



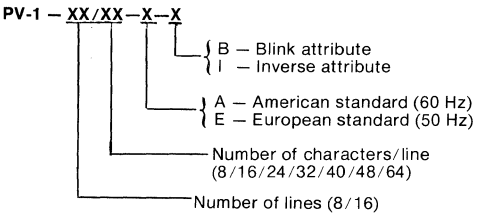
The Matrox character generator ROM includes upper and lower case alphanumerics (5 x 7 dot matrix) with below line extenders and special characters (6 x 10 dot matrix) for limited graphics applications. Should the user require special character fonts, the MCH-01 may be replaced by a user programmed EPROM (2716 Intel type).

**CHARACTER POSITION ADDRESS**



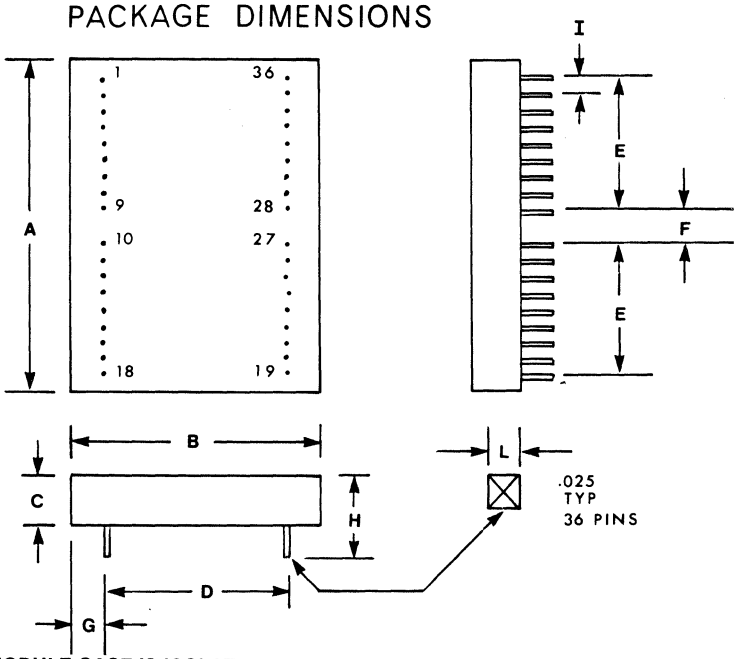

DO-D6 . . . character
D7 . . . attribute bit
0 . . . normal
1 . . . character inverse or flashing at 4 Hz

**ORDERING INFORMATION**




8

## PACKAGE DIMENSIONS




| DIM | MM | | INCHES | |
|---|---|---|---|---|
| | NOM. | TOL. | NOM. | TOL. |
| A | 114.300 | .254 | 6.000 | .01 |
| B | 101.600 | .254 | 4.500 | .01 |
| C | 12.700 | .254 | .50 | .01 |
| D | 99.568 | .254 | 3.920 | .01 |
| E | 20.32 | .254 | .800 | .01 |
| F | 10.16 | .254 | .400 | .01 |
| G | 7.366 | .254 | .29 | .01 |
| H | 4.318 | .254 | .170 | .01 |
| I | 2.540 | .076 | .100 | .003 |
| L | .635 | .025 | .025 | .001 |

**MODULE CASE IS ISOLATED ALLOWING ETCH RUNS UNDERNEATH.**

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

# MTX-2064

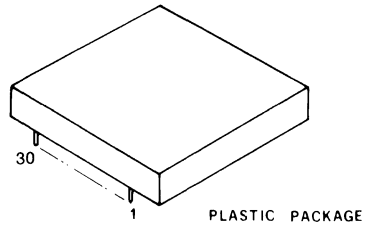
*HYBRID*
*(MOS, TTL)*
*24x80 ASCII Character*
*VIDEO RANDOM ACCESS MEMORY*

## MTX TV CRT CONTROLLER FAMILY

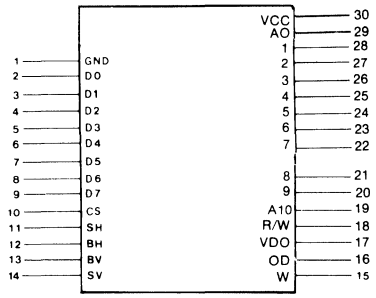
### 20x64 VIDEO RANDOM ACCESS MEMORY

The MTX-2064 is a TV CRT controller designed for use in systems that require display of alphanumeric data. On the input side the device is directly connected to bus organized systems and looks like a 1280X8 RAM. The output is a video signal which directly drives a TV monitor to provide a 20x64 field of 1280 ASCI characters.

- **organized as 1280x8 RAM**
- **20x64 display field**
- **bidirectional data bus**
- **TTL compatible**
- **access time 550 ns**
- **flicker free display**
- **single +5V power supply**
- **ASCII font standard**
- **standard video output**
- **drives up to 25 TV monitors**
- **character blinking**
- **upper/lower case/graphics**



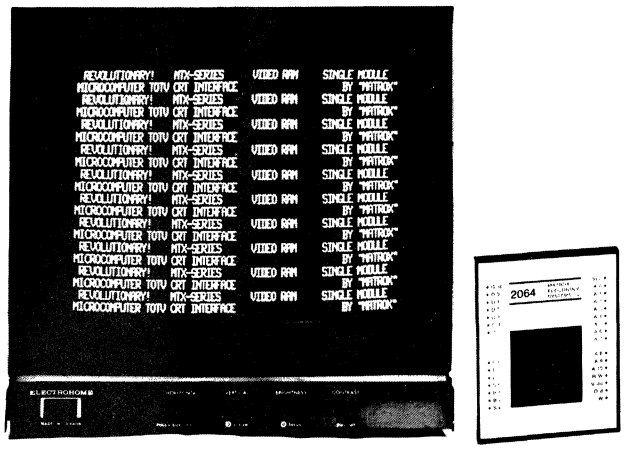

PIN ASSIGNMENT



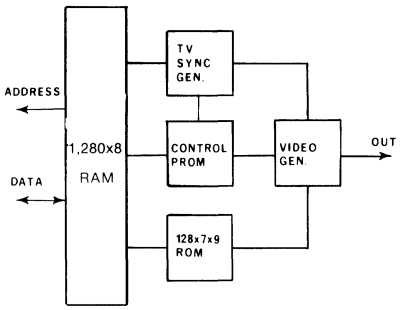

### ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Supply Voltage | Vcc | –0.3 to +6 | Vdc |
| Input Voltage | Vin | –0.3 to Vcc | Vdc |
| Operating Temp. | TA | 0 to 70 | °C |
| Storage Temp. | Tsta | –55 to 125 | °C |
| Lead Solder Temp. | TSD | +400 | °C |

TYPICAL APPLICATION



MTX-2064 VIDEO RAM
BLOCK DIAGRAM




8

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

### RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | Vdc |
| Input High Voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ | Vdc |
| Input Low Voltage | $V_{IL}$ | 0 | — | 0.7 | Vdc |

SH (pin 11) is horizontal sync.
Low = 5.8 μs,
High = 58.3 μs

SV (pin 14) is vertical sync.
Low = .256 ms,
HIgh = 16.41 ms

W (pin 15) TTL Video out

OD (pin 16) Output disable

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Input Current (High) | $I_{IN}$ | — | — | 20 | μA |
| Input Current (Low) | $I_{IN}$ | — | — | –0.4 | mA |
| Output Current (High) | $I_{OH}$ | — | — | –400 | μA |
| Output Current (Low) | $I_{OL}$ | — | — | 8 | mA |
| Output High Voltage | $V_{OH}$ | 2.4 | 3.4 | — | Vdc |
| Output Low Voltage | $V_{OL}$ | — | 0.3 | 0.5 | Vdc |
| Output Leakage (D0—D7) | $I_{LOH,L}$ | — | — | 20 | μA |
| Output Current (High) (D0—D7) | $I_{OH}$ | — | — | –2.6 | mA |
| Output Current (Low) (D0—D7) | $I_{OL}$ | — | — | 24 | mA |
| Supply Current (+5V) | $I_{CC}$ | — | 400 | 600 | mA |

### CAPACITANCE

| CHARACTERISTIC | SYMBOL | MAX. | UNIT |
|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 15 | pF |
| Output Capacitance | $C_{OUT}$ | 15 | pF |

Note: All MTX-2064 inputs are TTL equivalent (74LSxxx family or equivalent).

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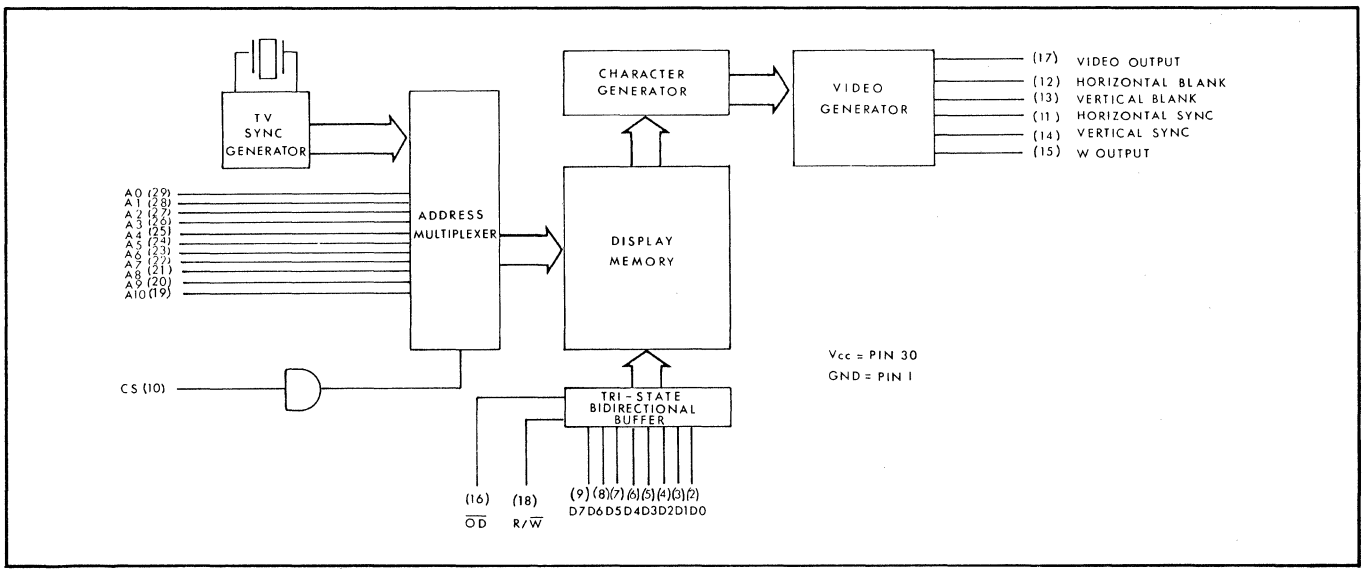
### FUNCTIONAL DESCRIPTION

The MTX-2064 is a TV CRT controller module which generates a video signal that can directly drive any standard TV monitor. The display is 1,280 ASCII alphanumeric characters arranged in an 20x64 matrix. Characters are displayed white on a black background.

On the input side, the MTX-2064 looks like an ordinary 1,280x8 RAM and can be directly connected to the address and data bus of any bus organized system.

The MTX-2064 is particularly suitable for use in microcomputer systems due to low cost, small size, high speed, low power requirement, and no additional interface circuitry.



## AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

### RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | UNIT |
|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 0 | ns |
| Address Hold time | $t_{AH}$ | 0 | ns |

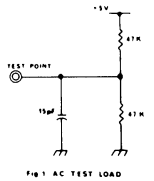
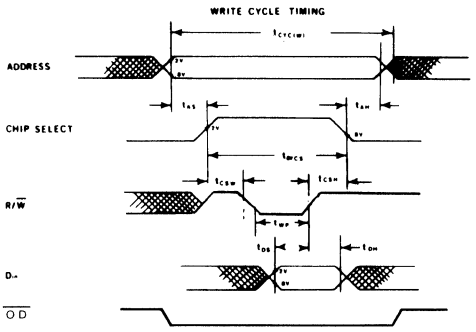


Fig. 1 AC TEST LOAD

### WRITE CYCLE

(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

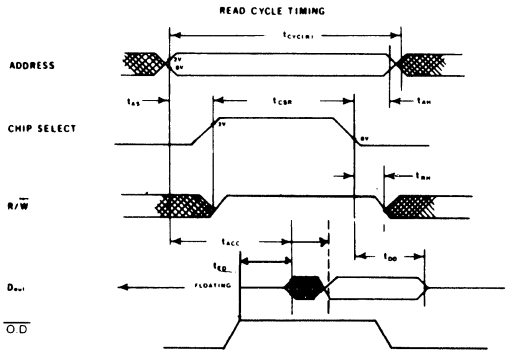
| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | $t_{CYC(W)}$ | 565 | — | ns |
| Write Chip Select Width | $t_{WCS}$ | 565 | — | ns |
| CS to Write Setup Time | $t_{CSW}$ | 240 | — | ns |
| Write Pulse Width | $t_{WP}$ | 250 | — | ns |
| Chip Select Hold Time | $t_{CSH}$ | 75 | — | ns |
| Data Setup Time | $t_{DS}$ | 250 | — | ns |
| Data Hold Time | $t_{DH}$ | 40 | — | ns |



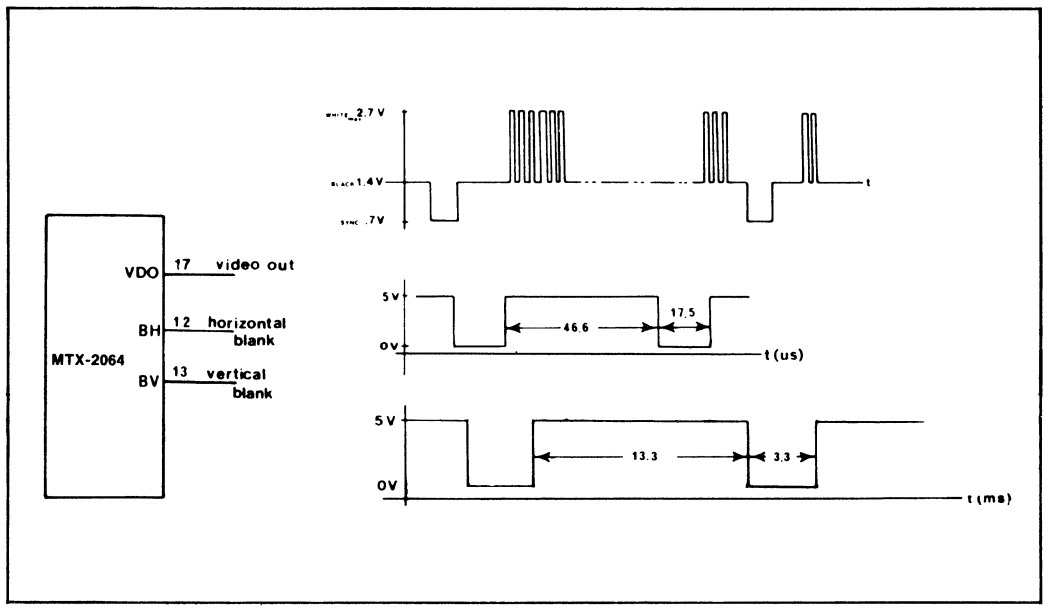

### READ CYCLE

(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | $t_{CYC(R)}$ | 550 | — | ns |
| Read Chip Select Width | $t_{CSR}$ | 550 | — | ns |
| Read Access Time | $t_{ACC}$ | — | 550 | ns |
| Output Enable Delay | $t_{ED}$ | — | 50 | ns |
| Output Disable Delay | $t_{DD}$ | — | 50 | ns |
| Read Hold Time | $t_{RH}$ | 0 | — | ns |




(OUTPUT DISABLE)



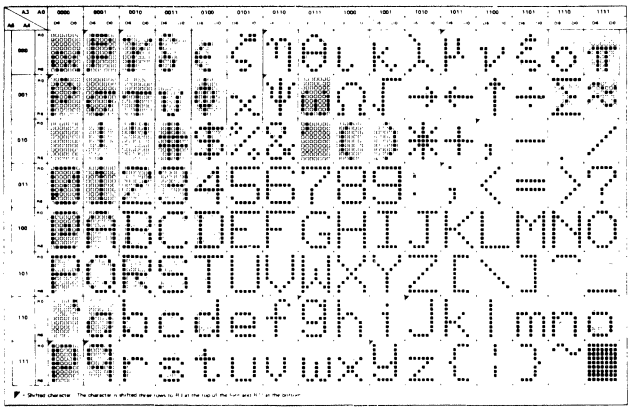

Sync. frequency
Horizontal: 15.600 kHz
Vertical: 60 Hz/50 Hz
Crystal controlled.
Output impedance: 75 ohms
Short circuit protection built in.

BH or BV signal can be used as a flag to access VRAM during horizontal or vertical retrace only.
(No flicker during access).

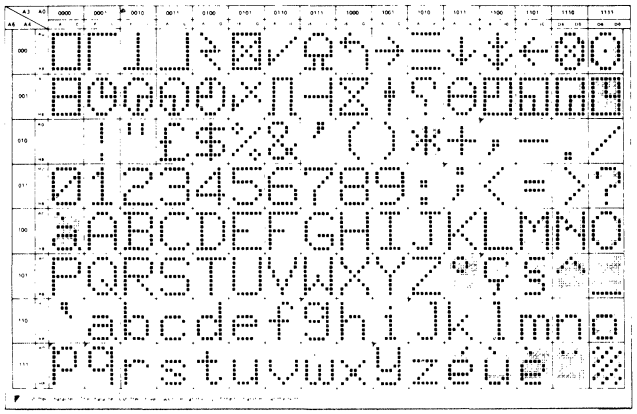
8

## ASCII CHARACTER FONT

### MTX-2064 A

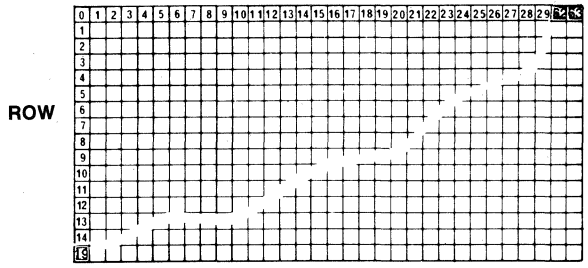


### MTX-2064 B



Additional character fonts are available from stock. Custom made font (128 characters in a 7x9 matrix) available at extra cost.

## SCREEN DISPLAY ORGANISATION




CHARACTER POSITION ADDRESS

ROW | COLUMN

| A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|

DATA

X | ASCII CHARACTER

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

D0-D6 ...character

D7 ...blink bit
0...normal
1...character flashing at 1 Hz

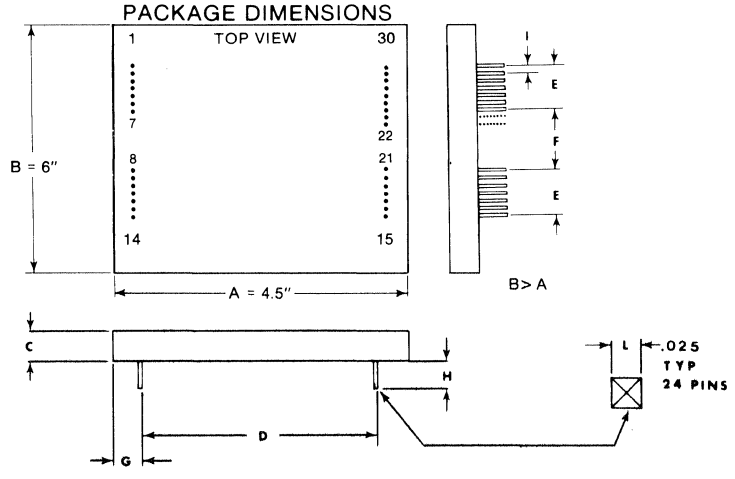
**ORDERING INFORMATION**

**MTX-2064–X X**

- A—American standard (60 Hz)
- E—European standard (50 Hz)

- A—Character set A (see ASCII CHARACTER FONT)
- B—Character set B (see ASCII CHARACTER FONT)
- G—German character set
- J—Japanese character set

PACKAGE DIMENSIONS




MODULE CASE IS ISOLATED ALLOWING ETCH RUNS UNDERNEATH.

| DIM | MM | | INCHES | |
|---|---|---|---|---|
| | NOM. | TOL. | NOM. | TOL. |
| A | 114.300 | .254 | 4.50 | .01 |
| B | 152.2 | .254 | 6.000 | .01 |
| C | 12.700 | .254 | .500 | .01 |
| D | 99.06 | .254 | 3.90 | .01 |
| E | 15.240 | .254 | .600 | .01 |
| F | 20.32 | .254 | .800 | .01 |
| G | 8.32 | .254 | .325 | .01 |
| H | 4.318 | .254 | .170 | .01 |
| I | 2.540 | .076 | .100 | .003 |
| L | .635 | .025 | .025 | .001 |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

# MMD-2480

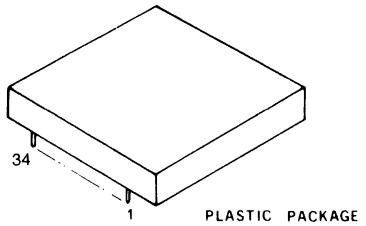
*HYBRID*
*(MOS, TTL)*
*24x80 ASCII Character*
*VIDEO RANDOM ACCESS MEMORY*

## MTX TV CRT CONTROLLER FAMILY

### 24x80 TV CRT CONTROLLER FAMILY

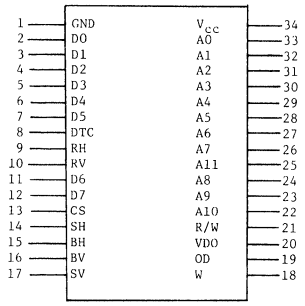
The MMD-2480 is a TV CRT controller designed for use in systems that require display of alphanumeric data. On the input side the device is directly connected to bus organized systems and looks like a 4Kx8 RAM. The output is a video signal which directly drives a TV monitor to provide a 24x80 field of 1920 ASCI characters.

- **24x80 display field**
- **organized as 4Kx8 RAM**
- **bidirectional data bus**
- **TTL compatible**
- **access time 500 ns**
- **flicker free display**
- **single + 5V power supply**
- **ASCII font standard**
- **standard video output**
- **drives up to 25 TV monitors**
- **character blinking**
- **upper/lower case/graphics**



PLASTIC PACKAGE

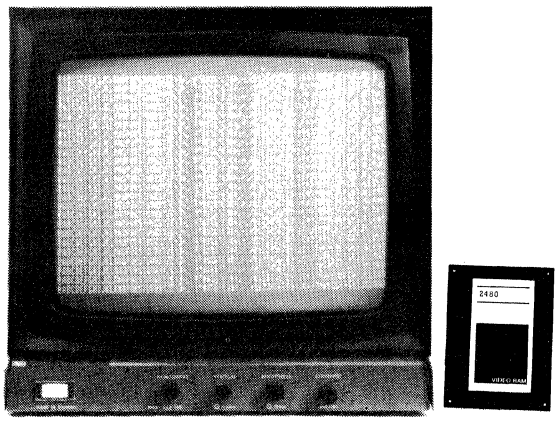
**PIN ASSIGNMENT**



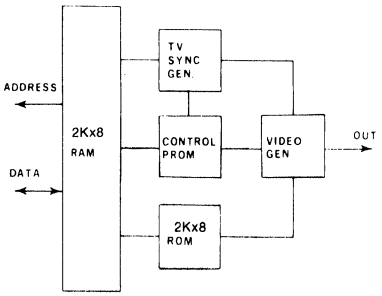

**ABSOLUTE MAXIMUM RATINGS**

| | | | |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to + 6 | Vdc |
| Input Voltage | Vin | -0.3 to Vcc | Vdc |
| Operating Temp. | $T_A$ | 0 to 70 | °C |
| Storage Temp. | $T_{sta}$ | -55 to 125 | °C |
| Lead Solder Temp. | $T_{SD}$ | + 400 | °C |

TYPICAL APPLICATION



MMD-2480 VIDEO RAM
BLOCK DIAGRAM




8

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

### RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 4.75 | 5.0 | 5.25 | Vdc |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ | Vdc |
| Input Low Voltage | $V_{IL}$ | 0 | | 0.7 | Vdc |

SH(pin 14) is horizontal sync.
High = 5.8 μs
Low = 58,3 μs

SV(pin 17) is vertical sync.
High = .256 ms
Low = 16.41 ms

W(pin 18) TTL Video out

$\overline{OD}$(pin 19) Output disable

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Input Current (High) | $I_{IN}$ | | | 20 | μA |
| Input Current (Low) | $I_{IN}$ | — | — | -0.4 | mA |
| Output Current (High) | $I_{OH}$ | | — | -400 | μA |
| Output Current (Low) | $I_{OL}$ | — | — | 8 | mA |
| Output High Voltage | $V_{OH}$ | 2.4 | 3.4 | — | Vdc |
| Output Low Voltage | $V_{OL}$ | — | 0.3 | 0.5 | Vdc |
| Output Leakage (D0—D7) | $I_{LOH,L}$ | — | — | 20 | μA |
| Output Current (High) D0—D7 | $I_{OH}$ | — | — | -2.6 | mA |
| Output Current (Low) D0—D7 | $I_{OL}$ | — | — | 24 | mA |
| Supply Current (.5V) | $I_{CC}$ | — | 400 | 900 | mA |

### CAPACITANCE

| CHARACTERISTIC | SYMBOL | MAX. | UNIT |
|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 15 | pF |
| Output Capacitance | $C_{OUT}$ | 15 | pF |

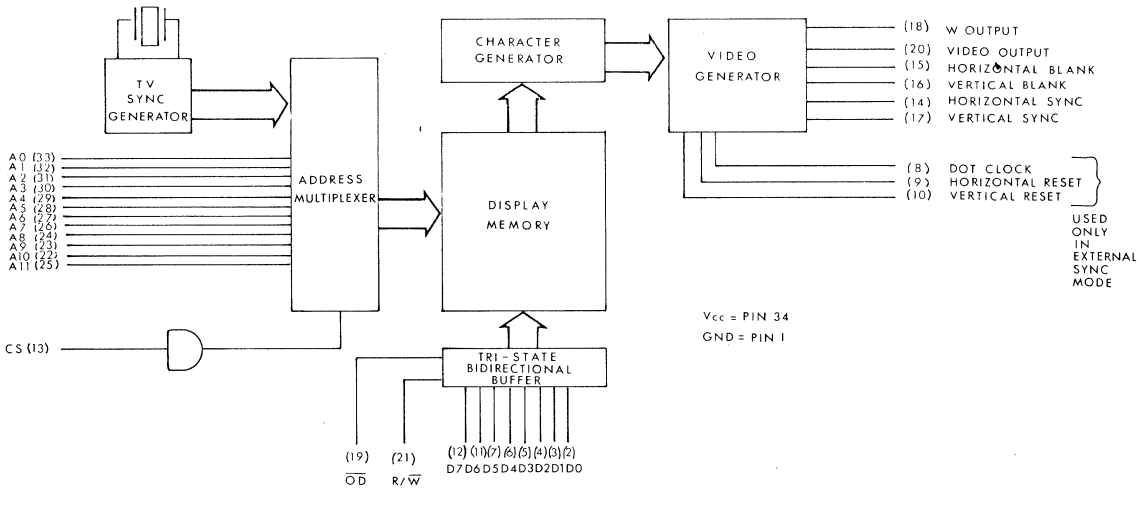
Note: All MMD-2480 inputs are TTL equivalent (74LSxxx family or equivalent).

8

### FUNCTIONAL DESCRIPTION

The MMD-2480 is a TV CRT controller module which generates a video signal that can directly drive any standard TV monitor. The display is 1920 ASCII alphanumeric characters arranged in a 24x80 matrix. Characters are displayed white on a black background. The character generator is a 2Kx8 EPROM (2716) programmed by Matrox. The user can program his own character generator by plugging in his 2716 EPROM (8x10 or 6x10 character cell).

On the input side, the MMD-2480 looks like an ordinary 4Kx8 RAM and can be directly connected to the address and data bus of any bus organized system. The MMD-2480 is particularly suitable for use in microcomputer systems due to low cost, small size, high speed, low power requirement, and no additional interface circuitry.



## AC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted)

### RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | UNIT |
|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 0 | ns |
| Address Hold Time | $t_{AH}$ | 0 | ns |

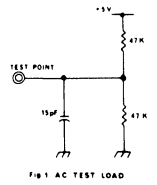


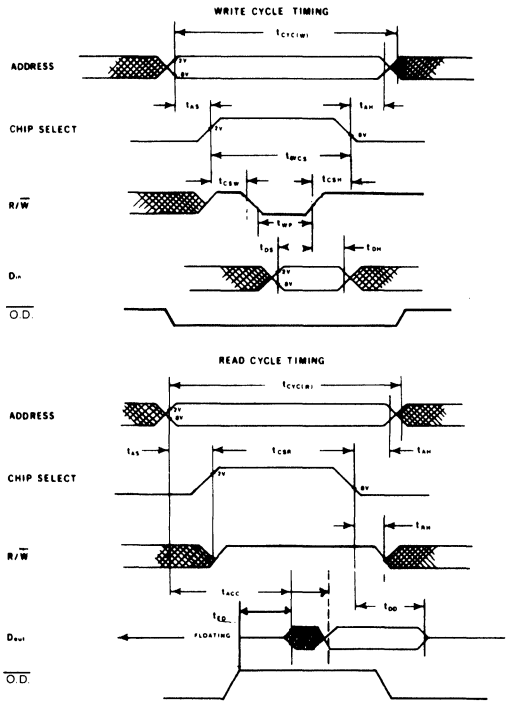
Fig. 1 AC TEST LOAD

### WRITE CYCLE
(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

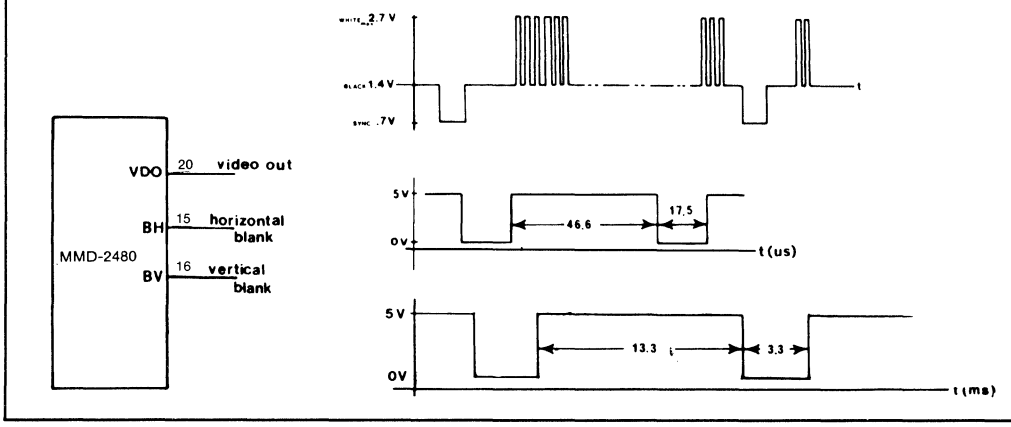
| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | $t_{CYC(W)}$ | 500 | — | ns |
| Write Chip Select Width | $t_{WCS}$ | 450 | — | ns |
| CS to Write Setup Time | $t_{CSW}$ | 200 | — | ns |
| Write Pulse Width | $t_{WP}$ | 200 | — | ns |
| Chip Select Hold Time | $t_{CSH}$ | 50 | — | ns |
| Data Setup Time | $t_{DS}$ | 200 | — | ns |
| Data Hold Time | $t_{DH}$ | 60 | — | ns |

### READ CYCLE
(All timing with rise time/fall time = 20ns)
(Load of Fig. 1)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | $t_{CYC(R)}$ | 500 | — | ns |
| Read Chip Select Width | $t_{CSR}$ | 500 | — | ns |
| Read Access Time | $t_{ACC}$ | — | 500 | ns |
| Output Enable Delay | $t_{ED}$ | — | 50 | ns |
| Output Disable Delay | $t_{DD}$ | | 50 | ns |
| Read Hold Time | $t_{RH}$ | 0 | — | ns |



(OUTPUT DISABLE)




Sync. frequency
Horizontal: 15.600 kHz
Vertical: 60 Hz/50 Hz
Crystal controlled
Output impedance: 75 ohms
Short circuit protection built in.
Non interlaced.

BH or BV signal can be used as a flag to access VRAM during horizontal or vertical retrace only.
(No flicker during access).

The MMD-2480 can be externally synchronised for special applications. To synchronise to external sync the PLL-01 module is required. Internal TV sync generator is forced in slave mode by cutting the jumper WI inside the module (module cover can be removed). Dot clock(8) and Reset Vert(10) are bidirectional signals; outputs when module is master, inputs when module is slave. All units are initially shipped in master mode.

For more data on external sync application consult PLL-01 data sheet.

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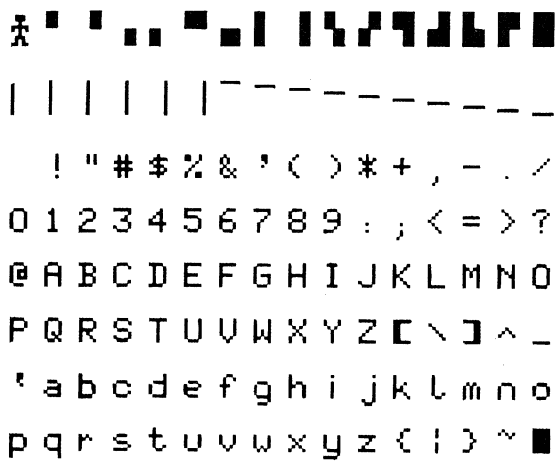
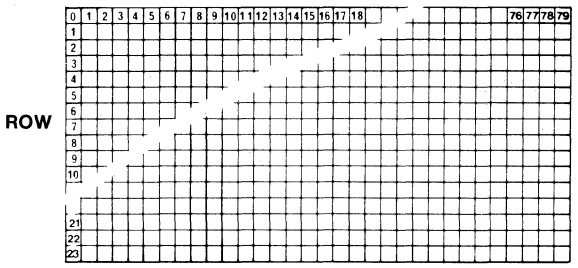
## ASCII CHARACTER FONT

MCH-01 (MATROX STANDARD 2716 EPROM)



A 2716 (2Kx8) EPROM is used as character generator. If the user wants other character sets, he can program his own EPROM and replace the one in the module.

## SCREEN DISPLAY ORGANISATION




COLUMN

**CHARACTER POSITION ADDRESS**

| ROW | | | | COLUMN | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**DATA**

X | **128 ASCII CHARACTER/GRAPHICS**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

X X | **64 ASCII CHARACTER**

**128 ASCII CHARACTERS**
D0-D6 = CHARACTER CODE
D7 = ATTRIBUTE BIT (INVERSE/BLINK)

**64 ASCII CHARACTERS**
D0-D5 = CHARACTER CODE
D6 = BLINK ATTRIBUTE
D7 = INVERSE ATTRIBUTE

## JUMPER OPTIONS

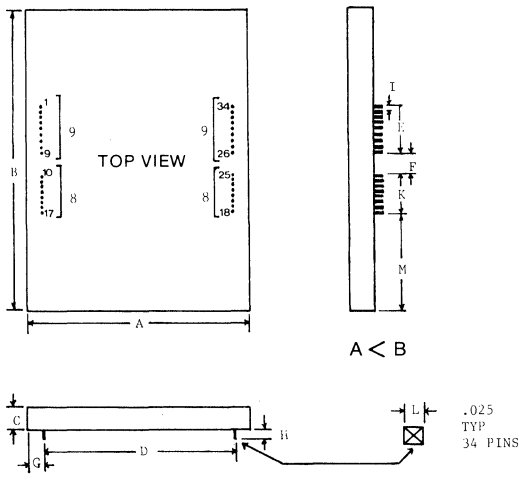
| JUMPER | | ATTRIBUTE |
|---|---|---|
| IN | OUT | |
| W1 | W2 | 64 Character Set |
| W2 | W1 | 128 Character Set |
| W1,W3 | W2 | Bit 6 = BLINK (64 Characters) |
| W4 | | Bit 7 = BLINK and INVERSE |
| W5 | W6 | 8 x 10 Character Cell |
| W6 | W5 | 6 x 10 Character Cell |
| W7 | | For External PLL |
| W8 | | MASTER Mode |
| | W8 | SLAVE Mode |

**ORDERING INFORMATION**

**MMD-2480-X X**

- AS—American standard (60 Hz)
- ES—European standard (50 Hz)

## PACKAGE DIMENSIONS







**MODULE CASE IS ISOLATED ALLOWING ETCH RUNS UNDERNEATH**

| DIM | MM | | INCHES | |
|---|---|---|---|---|
| | NOM. | TOL. | NOM. | TOL. |
| A | 114.300 | .254 | .500 | .01 |
| B | 152.2 | .254 | 6.000 | .01 |
| C | 12.700 | .254 | .500 | .01 |
| D | 99.06 | .254 | 3.90 | .01 |
| E | 20.32 | .254 | .800 | .01 |
| F | 12.7 | .254 | .500 | .01 |
| G | 7.366 | .254 | .29 | .01 |
| H | 4.318 | .254 | .170 | .01 |
| I | 2.540 | .076 | .100 | .003 |
| L | .635 | .025 | .025 | .001 |
| K | 17.78 | .259 | .700 | .01 |
| M | 50.70 | .254 | 2.00 | .01 |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

# MMD-256

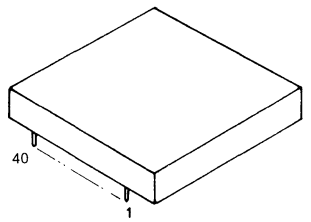
*HYBRID*
*(MOS, TTL)*
*256x256 DOT GRAPHICS*
*VIDEO RANDOM ACCESS MEMORY*

## MTX TV CRT CONTROLLER FAMILY

### 256 X 256 DOT GRAPHICS CRT CONTROLLER MODULE

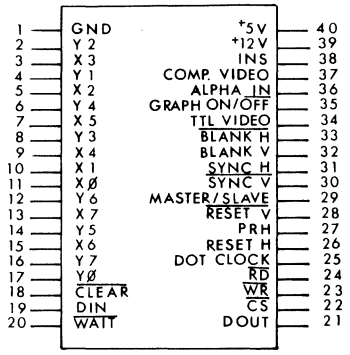
The MMD-256 is a TV CRT controller designed for use in systems that require the display of graphic data. On the input side, an XY matrix addressing scheme is used to access the 64K screen positions. The output is a video signal which directly drives a TV monitor to provide a 256 x 256 dot raster.

- **256 x 256 x 1 graphics**
- **Interfaces to any μP**
- **8K on-board RAM**
- **1.4 μs access time**
- **External clear**
- **Flicker free display**
- **External/internal sync**
- **Color/grey scale expansion**
- **Combines with alpha VRAMs**
- **Drives any TV monitor**
- **CPU on/off video control**
- **Low cost**




**PLASTIC PACKAGE**

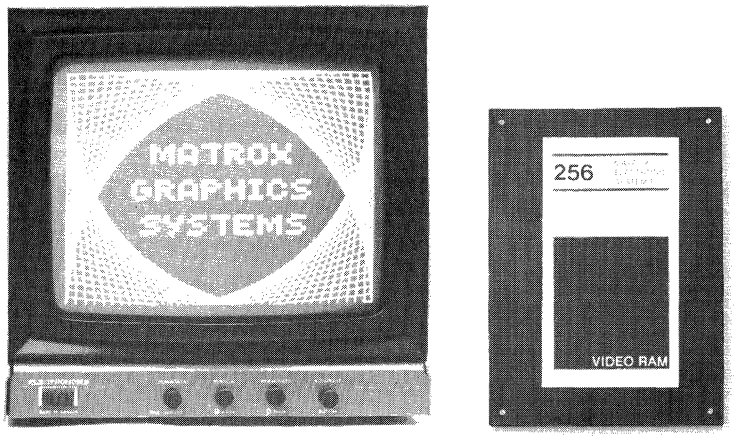
**PIN ASSIGNMENT**



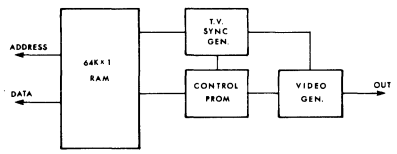

### ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +6V | Vdc |
| | $V_{DD}$ | −0.3 to +13V | Vdc |
| Input Voltage | $V_{in}$ | −0.3 to $V_{CC}$ | Vdc |
| Operating Temp. | $T_A$ | 0 to 70 | °C |
| Storage Temp. | $T_{sta}$ | −55 to 125 | °C |
| Lead Solder Temp. | $T_{SD}$ | +400 | °C |

### TYPICAL APPLICATION




### MMD-256 VIDEO RAM BLOCK DIAGRAM




8

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

### RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | Vdc |
| | $V_{DD}$ | 11.25 | 12.0 | 12.75 | Vdc |
| Input High Voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ | Vdc |
| Input Low Voltage | $V_{IL}$ | 0 | — | 0.7 | Vdc |

| | | | | | |
|---|---|---|---|---|---|
| Input Current (High) | Iin | — | — | 20 | μA |
| Input Current (Low) | Iin | — | — | –0.4 | mA |
| Input Current (High) | $I_{OH}$ | — | — | –400 | μA |
| Output Current (Low) | $I_{OL}$ | — | — | 8 | mA |
| Output High Voltage | $V_{OH}$ | 2.4 | 3.4 | — | Vdc |
| Output Low Voltage | $V_{OL}$ | — | 0.3 | 0.5 | Vdc |
| Output Leakage (Dout) | $I_{LOH,L}$ | — | — | 40 | μA |
| Output Current (High) | $I_{OH}$ | — | — | 2 | mA |
| Output Current (Low) | $I_{OL}$ | — | — | 12 | mA |
| Supply Current (+5V) | $I_{CC}$ | — | — | 400 | mA |
| Supply Current(+12V) | $I_{DD}$ | — | — | 100 | mA |

| | | |
|---|---|---|
| MASTER/SLAVE | (Pin 29) | Control signal used to configure the MMD-256 in either Master (Low) mode or Slave (High) mode. In Master mode Dot Clock, Hor. Reset, and Vert. Reset lines are output. In Slave mode Dot Clock, Hor. Reset and Vert. Reset are inputs. |
| PRH | (Pin 27) | Connected to Hor. Reset when PLL-01 is used to lock MMD-256 to external sync generator. |
| CLEAR | (Pin 18) | Clear input (active low) erases entire display memory. Minimum pulse width = 40ms. |
| INS | (Pin 38) | Intensity control input. Open = white. |
| GRAPH ON/OFF | (Pin 35) | On/off control of video output. Low = off. |
| ALPHA IN | (Pin 36) | TTL level video input from an alphanumeric VRAM or another MMD-256. Resulting video is logic OR. |

### CAPACITANCE

| CHARACTERISTIC | SYMBOL | MAX. | UNIT |
|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 15 | pF |
| Output Capacitance | $C_{OUT}$ | 15 | pF |

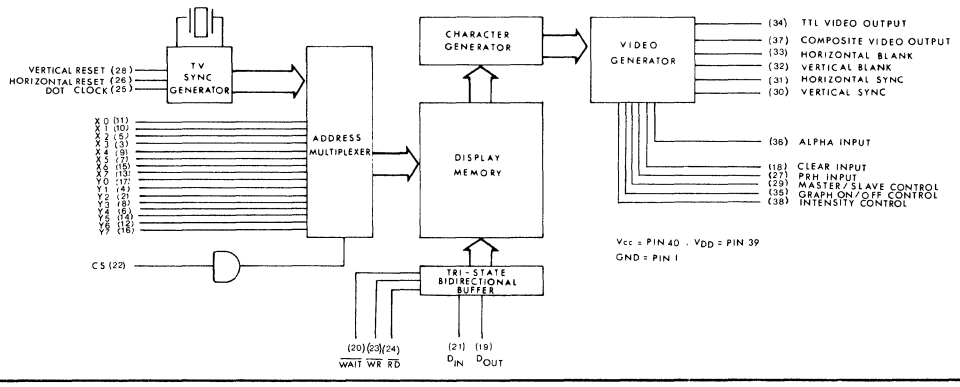
8

The MMD-256 is a complete 256 x 256 x 1 graphics CRT display controller in a small Matrox standard 4.5" x 6" x .5" self-enclosed module. The module contains an on-board TV sync generator, video generator, built-in refresh memory, and all the required electronics necessary to interface the MMD-256 to any 8 or 16 bit microprocessor. The composite video output from the MMD-256 module can directly drive any standard video monitor.

The MMD-256 features a CLEAR input pin which when pulled low will cause the entire display to be "cleared" to the value defined by DIN ("0" = black, "1" = white).

Multiple MMD-256 modules can be "stacked" together for various graphics effects. Increased resolution, more bits per pixel, color, or live animation are some examples of the enhancements of multiple module configurations. Also the MMD-256 can be combined with any of the Matrox alphanumeric VRAM modules to provide a combined alpha/graph display.

### BLOCK DIAGRAM

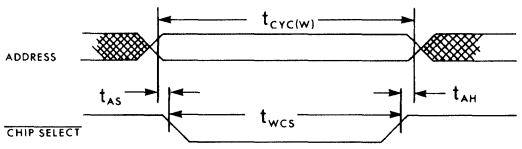


## AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

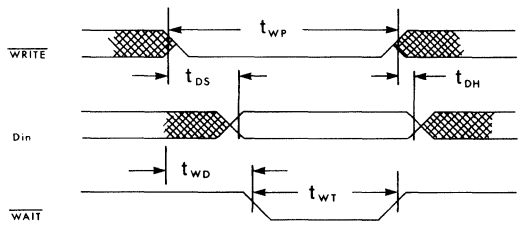
### RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | UNIT |
|---|---|---|---|
| Address Setup Time | tAS | 0 | ns |
| Address Hold time | tAH | 0 | ns |



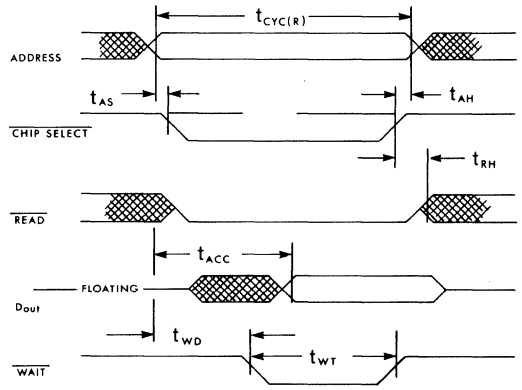

### WRITE CYCLE (All timing with rise time/fall time = 20ns)

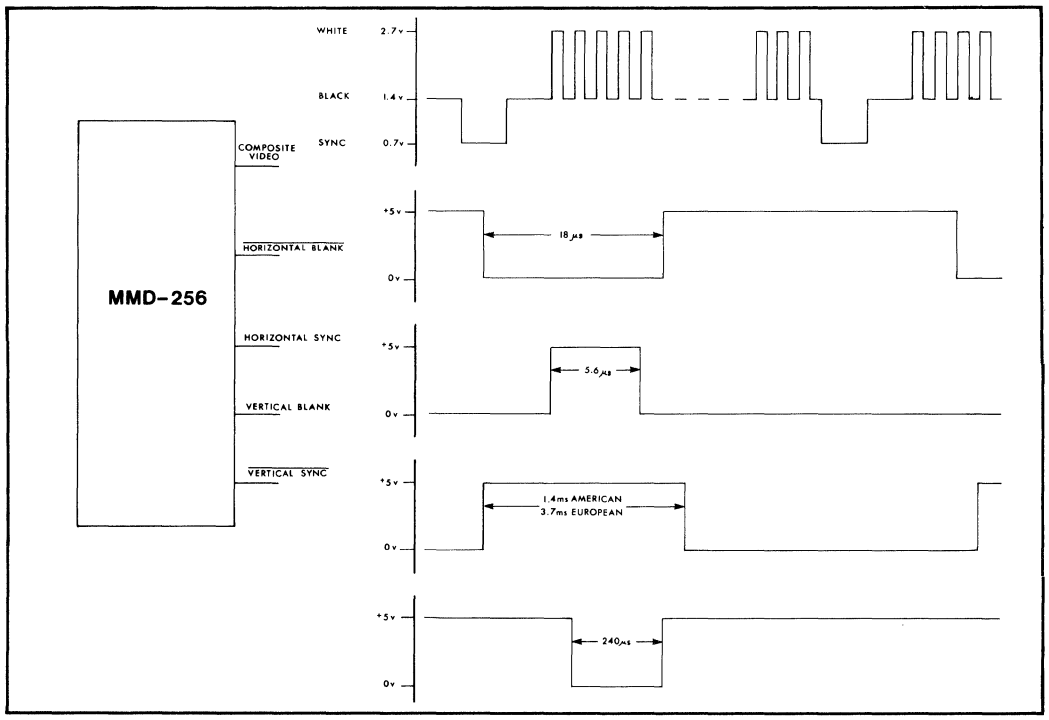
| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | tCYC(W) | 770 | — | ns |
| Write Chip Select Width | tWCS | 770 | — | ns |
| Write Pulse Width | tWP | 750 | — | ns |
| Data Set Up Time | tDS | 0 | — | ns |
| Data Hold Time | tDH | 0 | — | ns |
| Wait Pulse Width | tWT | 750 | 2150 | ns |
| Wait Pulse Delay | tWD | 20 | 50 | ns |




### READ CYCLE (All timing with rise time/fall time = 20ns)

| CHARACTERISTIC | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | tCYC(R) | 770 | — | ns |
| Read Chip Select Width | tCSR | 770 | — | ns |
| Read Access Time | tACC | 750 | — | ns |
| Read Hold Time | tRH | 0 | — | ns |
| Wait Pulse Width | tWT | 750 | 2150 | ns |
| Wait Pulse Delay | tWD | 20 | 50 | ns |



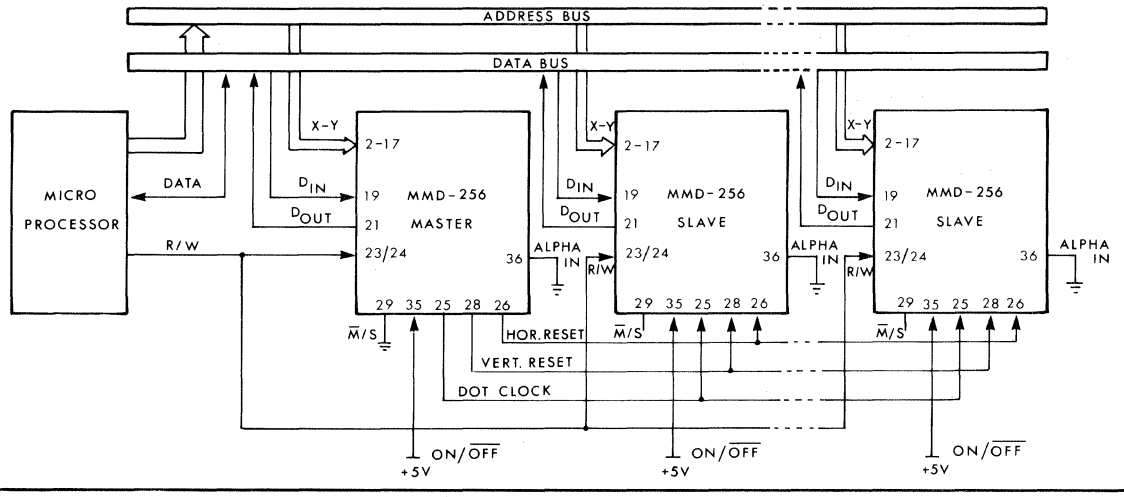

Sync. Frequency
Horizontal: 15.720 kHz
Vertical: 50/60 Hz (strap selectable)
Crystal controlled
Output impedence: 75 ohms
Short circuit protection built-in.

Horizontal or Vertical Blank signal can be used as a flag to access VRAM during horizontal or vertical retrace only. (no flicker during access)

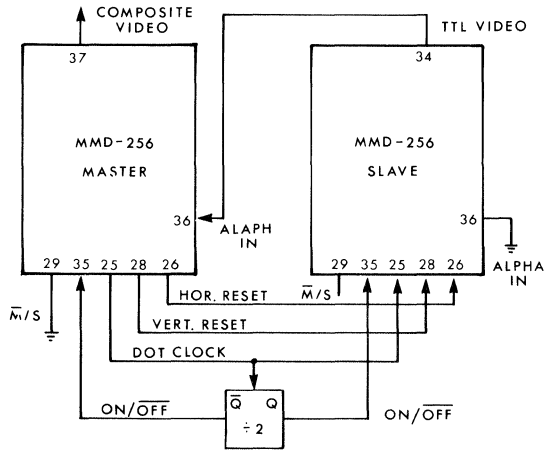
TTL Video output (pin 34) contains the video information without the sync signals. This output is useful for mixing with other video signals.

8

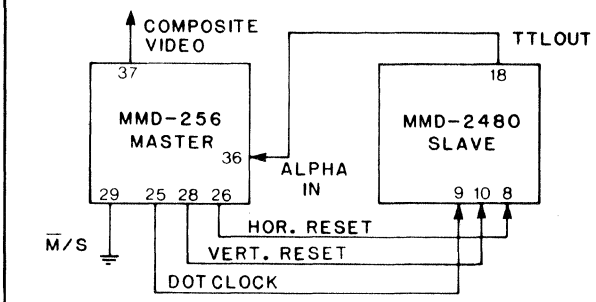
## 256 X 256 X 8 COLOR SYSTEM




## 512 x 256 RESOLUTION




## ALPHA/GRAPH DISPLAY

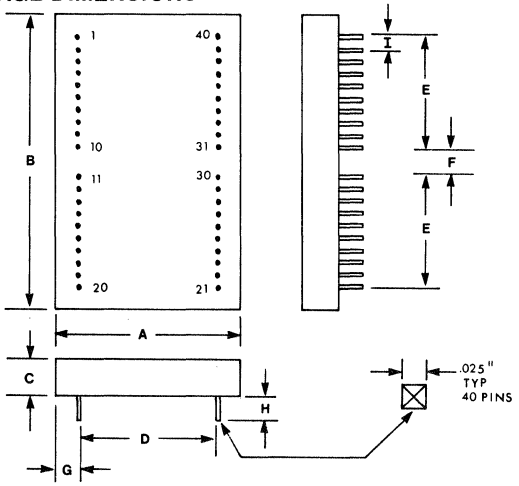



## ORDERING INFORMATION

**MMD-256D—XX**

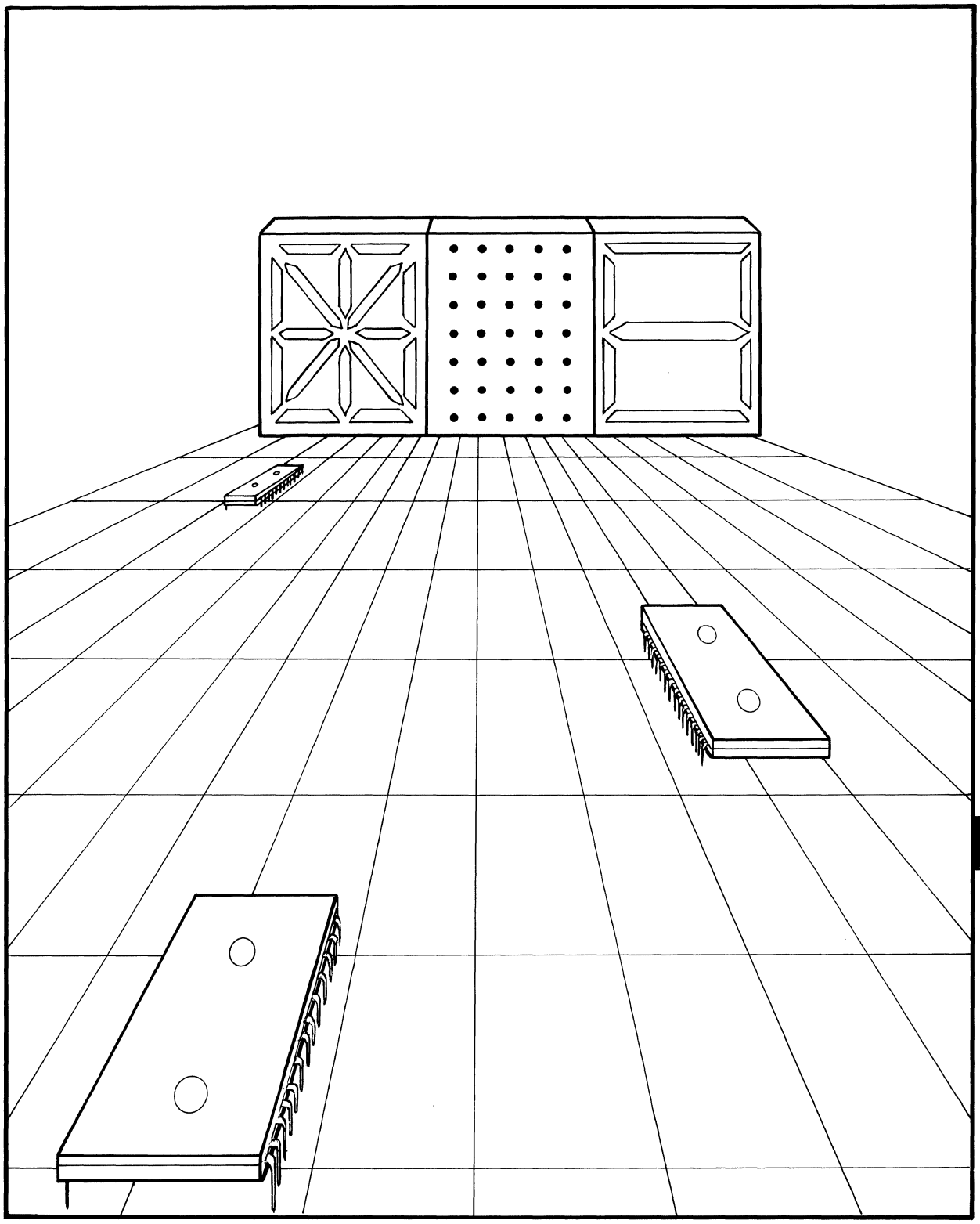
- AS—American standard (60 Hz)
- ES—European standard (50 Hz)

## PACKAGE DIMENSIONS




| DIM | MM | | INCHES | |
|---|---|---|---|---|
| | NOM. | TOL. | NOM. | TOL. |
| A | 114.300 | .254 | 4.500 | .01 |
| B | 152.200 | .254 | 6.000 | .01 |
| C | 12.700 | .254 | .50 | .01 |
| D | 99.060 | .254 | 3.900 | .01 |
| E | 22.830 | .254 | .900 | .01 |
| F | 5.070 | .254 | .200 | .01 |
| G | 7.366 | .254 | .29 | .01 |
| H | 4.318 | .254 | .170 | .01 |
| I | 2.540 | .076 | .100 | .003 |
| L | .635 | .025 | .025 | .001 |

**Module case is isolated, allowing etch runs underneath.**



# SINGLE CHIP LED DISPLAY CONTROLLERS

## SECTION 9 SINGLE CHIP LED DISPLAY CONTROLLERS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

# MTX-A1

*NMOS, Monolithic*
*single chip interface*
*32 ASCII character display*
*64 keys ASCII keyboard*

## MTX INTELLIGENT SINGLE CHIP DISPLAY INTERFACE FAMILY

### ALPHANUMERIC (DOT) DISPLAY/KEYBOARD CONTROLLER

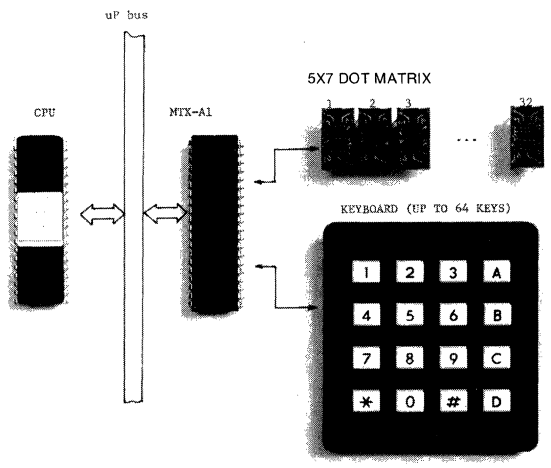
The MTX-A1 is a general purpose programmable three-way interface between a keyboard, an alphanumeric LED display, and a central processor. The single chip controller contains all the internal circuitry required to debounce and decode any keyboard with up to 64 keys. The display portion of the MTX-A1 provides all timing and refresh signals necessary to drive up to 32 popular 5x7 dot matrix LED displays. Many intelligent commands for display and keyboard manipulation are incorporated.

- **Single chip controller**
- **Drives up to 32 5x7 LEDs**
- **Built-in character generator**
- **Built-in 32x8 display memory**
- **No external refresh required**
- **Self-test built-in**
- **Scans up to 64 keys**
- **Interfaces to any $\mu$P**
- **Programmable display/ keyboard parameters**
- **Single +5V supply**
- **Low power (NMOS)**

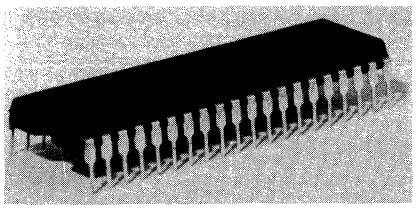
### ABSOLUTE MAXIMUM RATINGS

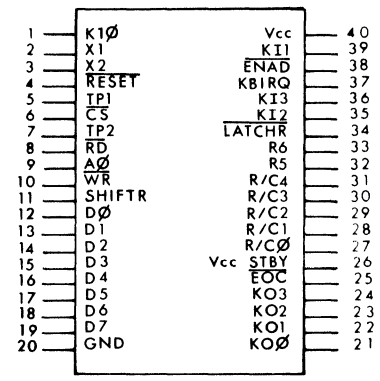
| | | | |
|---|---|---|---|
| Ambient Temperature Under Bias | Ta | 0 to 70 | °C |
| Storage Temperature | Tsta | –65 to +150 | °C |
| Voltage on Any Pin with Respect to Ground | Vpg | 0.5 to +7 | Vdc |
| Power Dissipation | Pd | 1.5 | W |

### TYPICAL APPLICATION

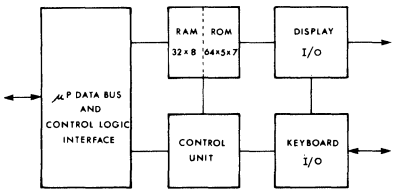



### 40-LEAD HERMETIC DUAL IN-LINE PACKAGE






### BLOCK DIAGRAM




9

## D.C. AND OPERATING CHARACTERISTICS

$T_A$ = 0°C TO 70°C, $V_{CC}$ = $V_{DD}$ = +5V ±5%, $V_{SS}$ = OV

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input Low Voltage (All Except X1, X2) | –0.5 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage (All Except X1, X2 RESET) | 2.0 | | $V_{CC}$ | V | |
| $V_{IH2}$ | Input High Voltage (X1, X2, RESET) | 3.0 | | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage ($D_0$-$D_7$) | | | 0.45 | V | $I_{OL}$ = 2.0 mA |
| $V_{OL2}$ | Output Low Voltage (All Other Outputs) | | | 0.45 | V | $I_{OL}$ = 1.6 mA |
| $V_{OH}$ | Output High Voltage ($D_0$-$D_7$) | 2.4 | | | V | $I_{OH}$ = 400 μA |
| $V_{OH2}$ | Output High Voltage (All Other Outputs) | 2.4 | | | V | $I_{OH}$ = 50 μA |
| $I_{IL}$ | Input Leakage Current ($T_0$, $T_1$, RD, WR, CS, $A_0$, EA) | | | ±10 | μA | $V_{SS} \leq V_{IN} \leq V_{CC}$ |
| $I_{OL}$ | Output Leakage Current ($D_0$-$D_7$, High Z State) | | | -10 | μA | $V_{SS}$ + 0.45 ≤ $V_{IN} \leq V_{CC}$ |
| $I_{DD}$ | $V_{DD}$ Supply Current (STBY) | | 10 | 25 | mA | $T_A$ = 25°C |
| $I_{DD} + I_{CC}$ | Total Supply Current | | 65 | 135 | mA | $T_A$ = 25°C |
| $I_{LI1}$ | Low Input Source Current R/C0, R6, K00-3, KI0-3 | | | 0.4 | mA | $V_{IL}$ = 0.8V |
| $I_{LI2}$ | Low Input Source Current RESET, | | | 0.2 | mA | $V_{IL}$ = 0.8V |

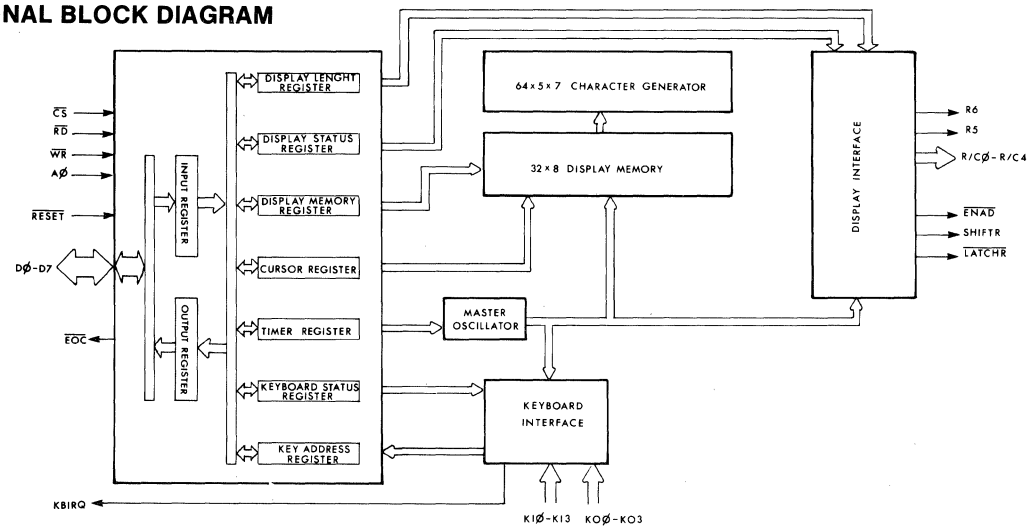
## FUNCTIONAL DESCRIPTION

The MTX-A1 recognizes a 22 command instruction set which enables the user to program the display and keyboard parameters by read/writing a set of on-chip command registers (see MTX-A1 FUNCTIONAL BLOCK DIAGRAM). The command registers allow the user to monitor the keyboard and display and control all internal operational parameters such as display length (1 to 32 characters), display attributes (display on/off, display blink on/off, cursor blink on/off, cursor index on/off, cursor index up/down), display refresh rate, and keyboard status (keyboard scan on/off, 16/64 key scan). Additionally the MTX-A1 instruction set enables the user to manipulate the display (Clear, rotate or shift display) as well as execute a self-test of the device whereby the MTX-A1 will display the first 32 characters in the ASCII alphabet in ascending order.

The on-chip display interface contains all the required circuitry to drive up to 32 5x7 dot matrix LEDs. A built-in character generator contains the binary information for a 64 character alphanumeric ASCII character set. In addition the user can program the MTX-A1 to display a blinking underline cursor (cursor position will blink between displayed character and an underline). The user can also disable the display through software.

The MTX-A1 can interface any standard 16 or 64 key keyboard. Key closure will be detected by either continuously testing D7 of the Keyboard Status Register or by a CPU interrupt, via the KBIRQ line. The MTX-A1 uses a lock-out scan method so that only one key closure will be detected at a time. Key scanning will not resume until the closed key is released.

## FUNCTIONAL BLOCK DIAGRAM

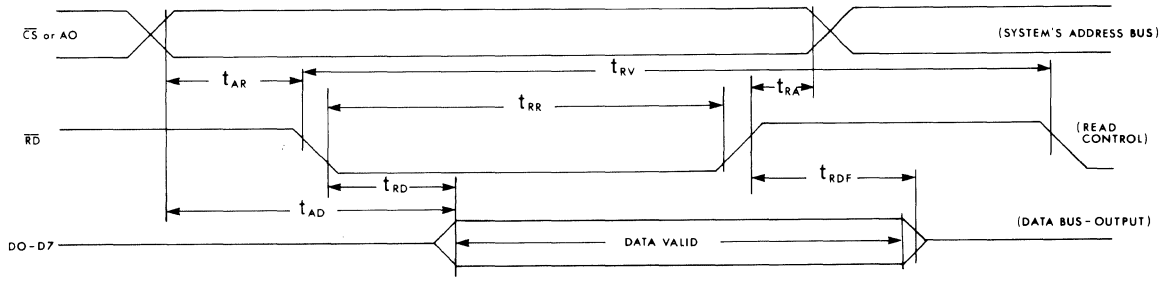


**A.C. CHARACTERISTICS** $T_A$ = 0°C TO 70°C, $V_{CC}$ = $V_{DD}$ = +5V ±5%, $V_{SS}$ = OV

**A.C. TEST CONDITIONS**

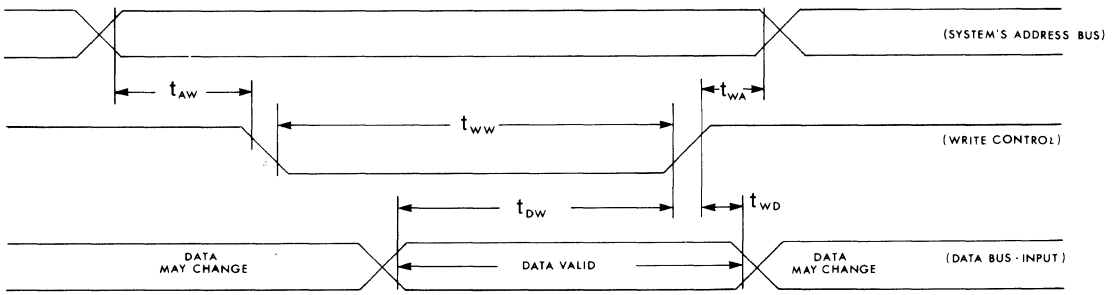
$D_7$-$D_0$ Outputs $R_L$ = 2.2k to $V_{SS}$
4.3k to $V_{CC}$
$C_L$ = 100 pF

## 1. READ OPERATION



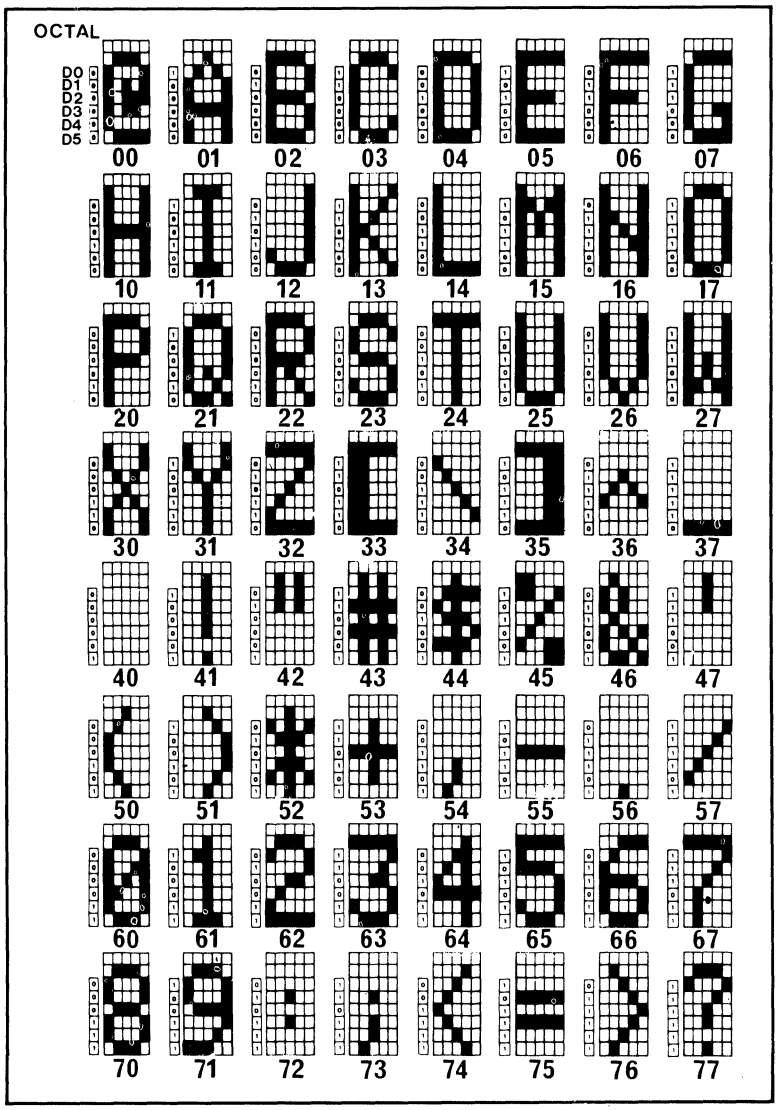

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{AR}$ | CS, $A_0$ Setup to RD | 0 | 100 | | ns | |
| $t_{RA}$ | CS, $A_0$ Hold After RD | 0 | 25 | | ns | |
| $t_{RR}$ | RD Pulse Width | 250 | 280 | 2 x $t_{CY}$ | ns | $t_{CY}$ = 2.5 μs |
| $t_{AD}$ | CS, $A_0$ to Data Out Delay | | 200 | 225 | ns | |
| $t_{RD}$ | RD to Data Out Delay | | 200 | 225 | ns | |
| $t_{RDF}$ | RD to Data Float Delay | 10 | | 100 | ns | CL = 15 pF |
| | | | 120 | | ns | CL = 100 pF |
| $t_{RV}$ | Recovery Time Between Reads And/Or Write | .300 | 1 | | μs | |
| $t_{CY}$ | Cycle Time | 2.5 | 2.5 | | μs | 6 MHz Crystal |

## 2. WRITE OPERATION




| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{AW}$ | CS, $A_0$ Setup to WR | 0 | 50 | | ns | |
| $t_{WA}$ | CS, $A_0$ Hold After WR | 0 | 40 | | ns | |
| $t_{WW}$ | WR Pulse Width | 250 | 280 | 2 x $t_{CY}$ | ns | $t_{CY}$ = 5 μs |
| $t_{DW}$ | Data Setup to WR | 150 | 220 | | ns | |
| $t_{WD}$ | Data Hold After WR | 0 | 0 | | ns | |

## ASCII CHARACTER FONT



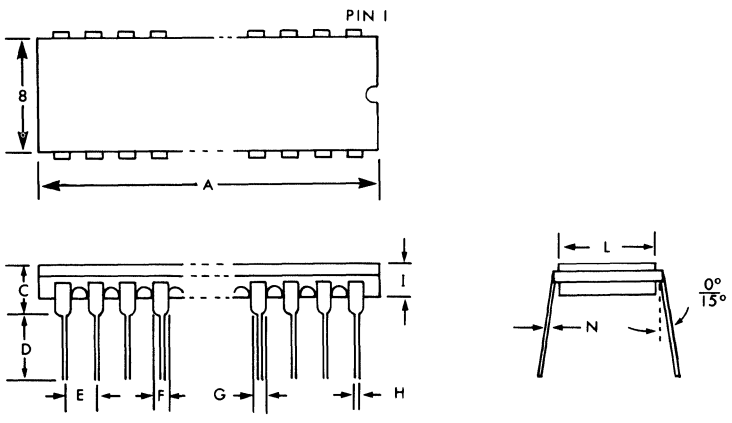

## MTX-A1 INSTRUCTION SET

| MNEMONIC | CODE D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|
| CLA | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Clear display memory |
| BLA | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Load blank to display memory |
| RTL | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Rotate display left |
| RTR | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Rotate display right |
| SHL | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | Shift display left |
| SHR | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | Shift display right |
| INC | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | Increment cursor |
| DEC | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | Decrement cursor |
| STT | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Execute self-test |
| GKA | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | Get key address |
| GDM | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Get display memory |
| GDL | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Get display length |
| GKS | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | Get keyboard status |
| GDS | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | Get display status |
| GTR | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Get timer register |
| GCA | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | Get cursor address |
| LCR | 1 | 0 | 0 | e | d | c | b | a | Load cursor and read display |
| LDL | 0 | 1 | 0 | e | d | c | b | a | Load display length |
| LKS | 1 | 0 | 1 | X | X | X | b | a | Load keyboard status |
| LDS | 1 | 1 | 0 | e | d | c | b | a | Load display status |
| LTR | 0 | 1 | 1 | e | d | c | b | a | Load timer register |
| LDM | 0 | 0 | f | e | d | c | b | a | Load display memory |

Note: The MTX-A1 is supplied with the ASCII character font as shown. However other character fonts (including Japanese Kata-Kana and general European) are available. Additionally custom designed character fonts can be supplied at extra cost. For more details consult the factory.

**ORDERING INFORMATION:**
**MTX-AI**

## PACKAGE DIMENSIONS




| DIM | MM MIN. | MM MAX. | INCHES MIN. | INCHES MAX. |
|---|---|---|---|---|
| A | 51.562 | 52.832 | 2.030 | 2,080 |
| B | 13.081 | 15.240 | 0.515 | 0.600 |
| C | — | 5.588 | — | 0.220 |
| D | 3.175 | — | 0.125 | — |
| E | 2.286 | 2.794 | 0.090 | 0.110 |
| F | 1.524 | — | 0.060 | — |
| G | 0.813 | — | 0.032 | — |
| H | 0.406 | 0.508 | 0.016 | 0.020 |
| I | 3.683 | 4.750 | 0.145 | 0.187 |
| L | — | 15.875 | — | 0.625 |
| M | 0.254 | — | 0.010 | — |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825651

# MTX-B1

*NMOS, Monolithic*
*single chip interface*
*32 ASCII character display*
*64 keys ASCII keyboard*

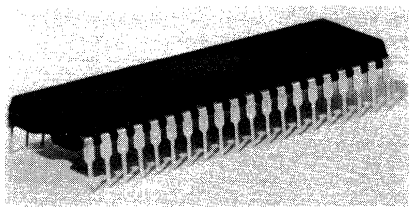
## MTX INTELLIGENT SINGLE CHIP DISPLAY INTERFACE FAMILY

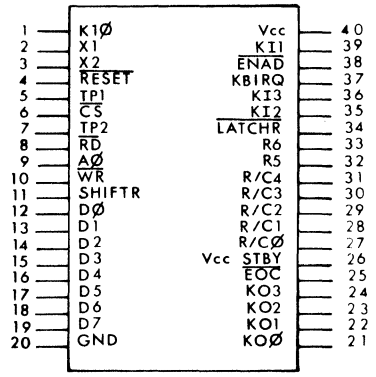
### ALPHANUMERIC (SEGMENT) DISPLAY/KEYBOARD CONTROLLER

The MTX-B1 is a general purpose programmable three-way interface between a keyboard, an alphanumeric LED display, and a central processor. The single chip controller contains all the internal circuitry required to debounce and decode any keyboard with up to 64 keys. The display portion of the MTX-B1 provides all timing and refresh signals necessary to drive up to 32 popular segment type displays. Many intelligent commands for display and keyboard manipulation are incorporated.

- **Single chip controller**
- **Drives up to 32 displays**
- **7 to 16 segment displays**
- **Built-in character generator**
- **Built-in 32x8 display memory**
- **Scans up to 64 keys**
- **Interfaces to any uP**
- **Self-test built-in**
- **Programmable display/ keyboard parameters**
- **Single +5V supply**
- **Low power (NMOS)**

### 40-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

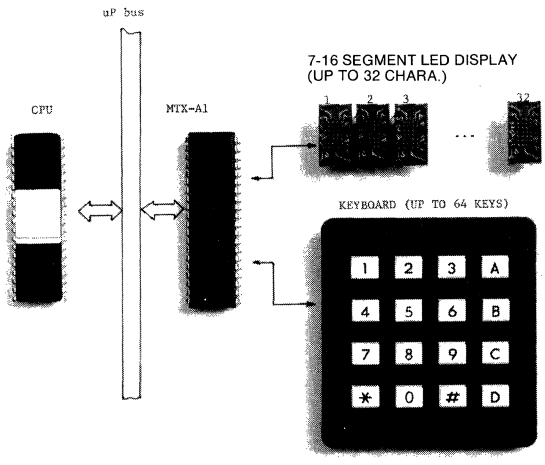




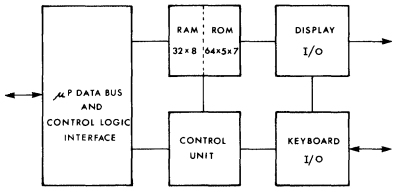

### ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Ambient Temperature Under Bias | Ta | 0 to 70 | °C |
| Storage Temperature | Tsta | –65 to +150 | °C |
| Voltage on Any Pin with Respect to Ground | Vpg | 0.5 to +7 | Vdc |
| Power Dissipation | Pd | 1.5 | W |

### TYPICAL APPLICATION




### BLOCK DIAGRAM

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## D.C. AND OPERATING CHARACTERISTICS

$T_A$ = 0°C TO 70°C, $V_{CC}$ = $V_{DD}$ = +5V ±5%, $V_{SS}$ = 0V

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input Low Voltage (All Except $X_1$, $X_2$) | –0.5 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage (All Except $X_1$, $X_2$ RESET) | 2.0 | | $V_{CC}$ | V | |
| $V_{IH2}$ | Input High Voltage ($X_1$, $X_2$, RESET) | 3.0 | | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage ($D_0$-$D_7$) | | | 0.45 | V | $I_{OL}$ = 2.0 mA |
| $V_{OL2}$ | Output Low Voltage (All Other Outputs) | | | 0.45 | V | $I_{OL}$ = 1.6 mA |
| $V_{OH}$ | Output High Voltage ($D_0$-$D_7$) | 2.4 | | | V | $I_{OH}$ = 400 μA |
| $V_{OH2}$ | Output High Voltage (All Other Outputs) | 2.4 | | | V | $I_{OH}$ = 50 μA |
| $I_{IL}$ | Input Leakage Current ($T_0$, $T_1$, RD, WR, CS, $A_0$, EA) | | | ±10 | μA | $V_{SS} \leq V_{IN} \leq V_{CC}$ |
| $I_{OL}$ | Output Leakage Current ($D_0$-$D_7$, High Z State) | | | -10 | μA | $V_{SS}$ + 0.45 ≤ $V_{IN} \leq V_{CC}$ |
| $I_{DD}$ | $V_{DD}$ Supply Current (STBY) | | 10 | 25 | mA | $T_A$ = 25°C |
| $I_{DD} + I_{CC}$ | Total Supply Current | | 65 | 135 | mA | $T_A$ = 25°C |
| $I_{LI1}$ | Low Input Source Current R/C0, R6, K0Ø-3, KIØ-3 | | | 0.4 | mA | $V_{IL}$ = 0.8V |
| $I_{LI2}$ | Low Input Source Current RESET, SS | | | 0.2 | mA | $V_{IL}$ = 0.8V |

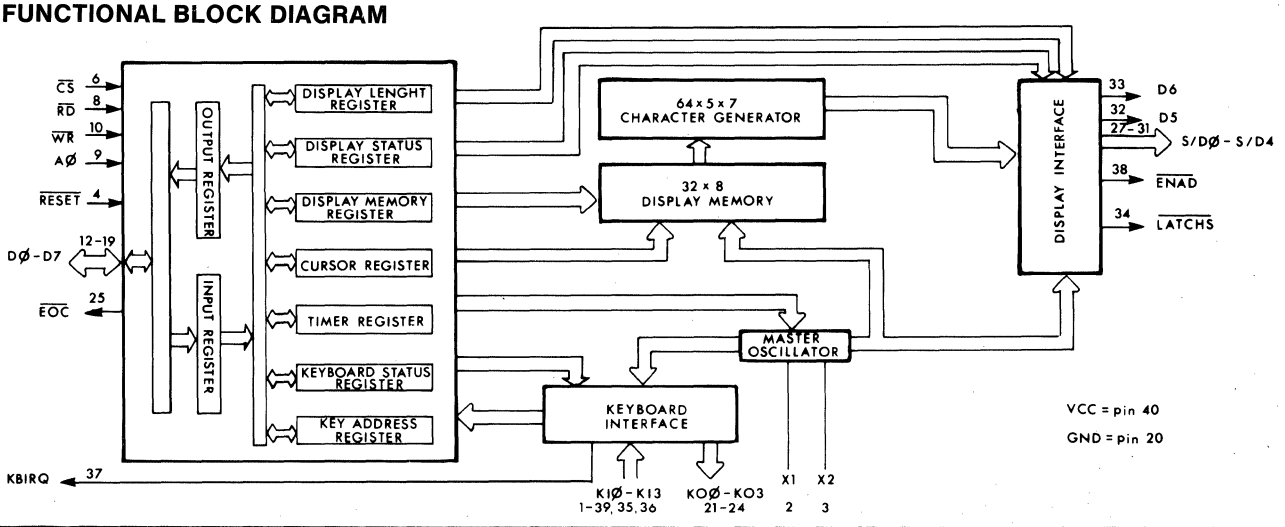
### FUNCTIONAL DESCRIPTION

The MTX-B1 recognizes a 22 command instruction set which enables the user to program the display and keyboard parameters by read/writing a set of on-chip command registers (see MTX-B1 FUNCTIONAL BLOCK DIAGRAM). The command registers allow the user to monitor the keyboard and display and control all internal operational parameters such as display length (1 to 32 characters), display attributes (display on/off, display blink on/off, cursor blink on/off, cursor index on/off, cursor index up/down), display refresh rate, and keyboard status (keyboard scan on/off, 16/64 key scan). Additionally the MTX-B1 instruction set enables the user to manipulate the display (Clear, rotate or shift display) as well as execute a self-test of the device whereby the MTX-B1 will display the first 32 characters in the ASCII alphabet in ascending order.

The on-chip display interface contains all the required circuitry to drive up to 32 segment type (from 7 to 16) displays. A built-in character generator contains the binary information for a 64 character alphanumeric ASCII character set. In addition the user can program the MTX-B1 to display a blinking underline cursor (cursor position will blink between displayed character and an underline). The user can also disable the display through software.

The MTX-B1 can interface any standard 16 or 64 key keyboard. Key closure will be detected by either continuously testing D7 of the Keyboard Status Register or by a CPU interrupt, via the KBIRQ line. The MTX-B1 uses a lock-out scan method so that only one key closure will be detected at a time. Key scanning will not resume until the closed key is released.

### FUNCTIONAL BLOCK DIAGRAM

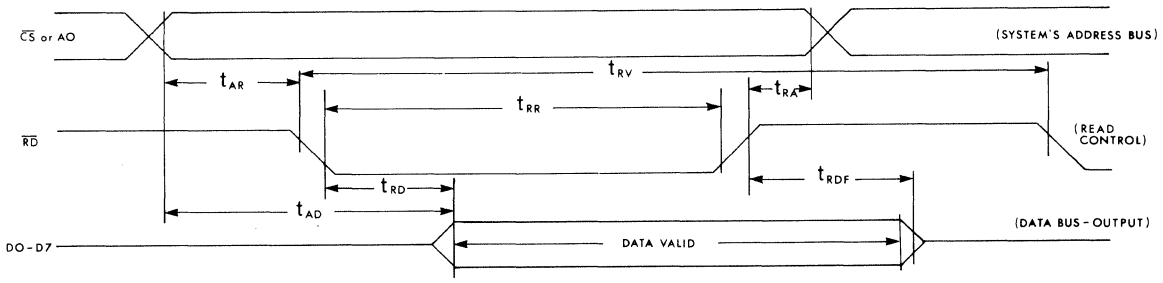


**A.C. CHARACTERISTICS** $T_A$ = 0°C TO 70°C, $V_{CC}$ = $V_{DD}$ = +5V ±5%, $V_{SS}$ = 0V

**A.C. TEST CONDITIONS**

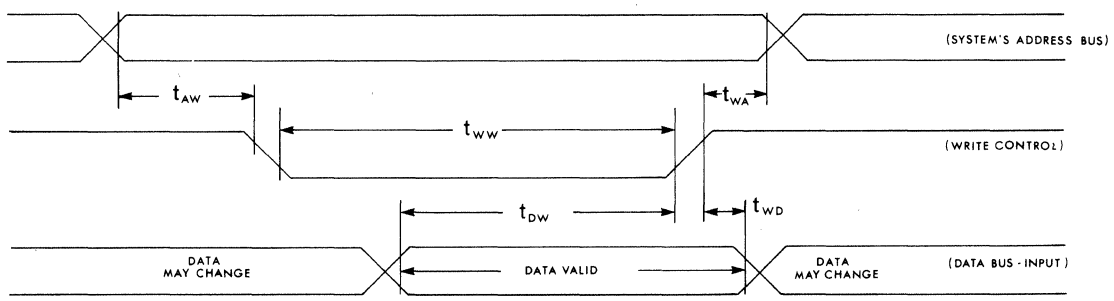
$D_7$-$D_0$ Outputs $R_L$ = 2.2k to $V_{SS}$
4.3k to $V_{CC}$
$C_L$ = 100 pF

## 1. READ OPERATION



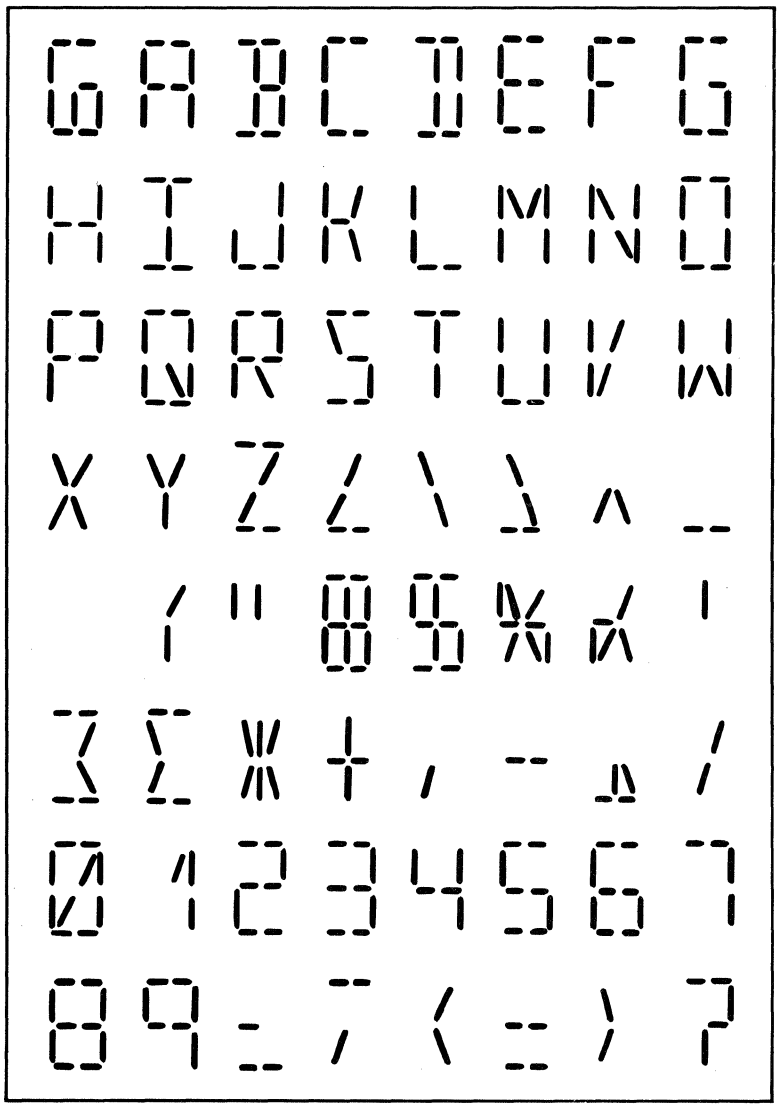

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| tAR | CS, A0 Setup to RD | 0 | 100 | | ns | |
| tRA | CS, A0 Hold After RD | 0 | 25 | | ns | |
| tRR | RD Pulse Width | 250 | 280 | 2 x tCY | ns | tCY = 2.5 μs |
| tAD | CS, A0 to Data Out Delay | | 200 | 225 | ns | |
| tRD | RD to Data Out Delay | | 200 | 225 | ns | |
| tRDF | RD to Data Float Delay | 10 | | 100 | ns | CL = 15 pF |
| | | | 120 | | ns | CL = 100 pF |
| tRV | Recovery Time Between Reads And/Or Write | .300 | 1 | | μs | |
| tCY | Cycle Time | 2.5 | 2.5 | | μs | 6 MHz Crystal |

## 2. WRITE OPERATION




| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| tAW | CS, A0 Setup to WR | 0 | 50 | | ns | |
| tWA | CS, A0 Hold After WR | 0 | 40 | | ns | |
| tWW | WR Pulse Width | 250 | 280 | 2 x tCY | ns | tCY = 5 μs |
| tDW | Data Setup to WR | 150 | 220 | | ns | |
| tWD | Data Hold After WR | 0 | 0 | | ns | |

## ASCII CHARACTER FONT



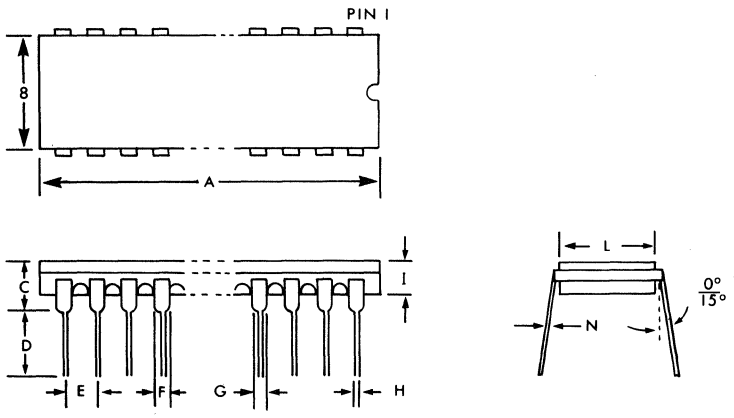
## MTX-B1 INSTRUCTION SET

| MNEMONIC | CODE | | | | | | | | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| CLA | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Clear display memory |
| BLA | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Load blank to display memory |
| RTL | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Rotate display left |
| RTR | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Rotate display right |
| SHL | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | Shift display left |
| SHR | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | Shift display right |
| INC | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | Increment cursor |
| DEC | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | Decrement cursor |
| STT | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Execute self-test |
| GKA | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | Get key address |
| GDM | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Get display memory |
| GDL | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Get display length |
| GKS | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | Get keyboard status |
| GDS | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | Get display status |
| GTR | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Get timer register |
| GCA | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | Get cursor address |
| LCR | 1 | 0 | 0 | e | d | c | b | a | Load cursor and read display |
| LDL | 0 | 1 | 0 | e | d | c | b | a | Load display length |
| LKS | 1 | 0 | 1 | X | X | X | b | a | Load keyboard status |
| LDS | 1 | 1 | 0 | e | d | c | b | a | Load display status |
| LTR | 0 | 1 | 1 | e | d | c | b | a | Load timer register |
| LDM | 0 | 0 | f | e | d | c | b | a | Load display memory |

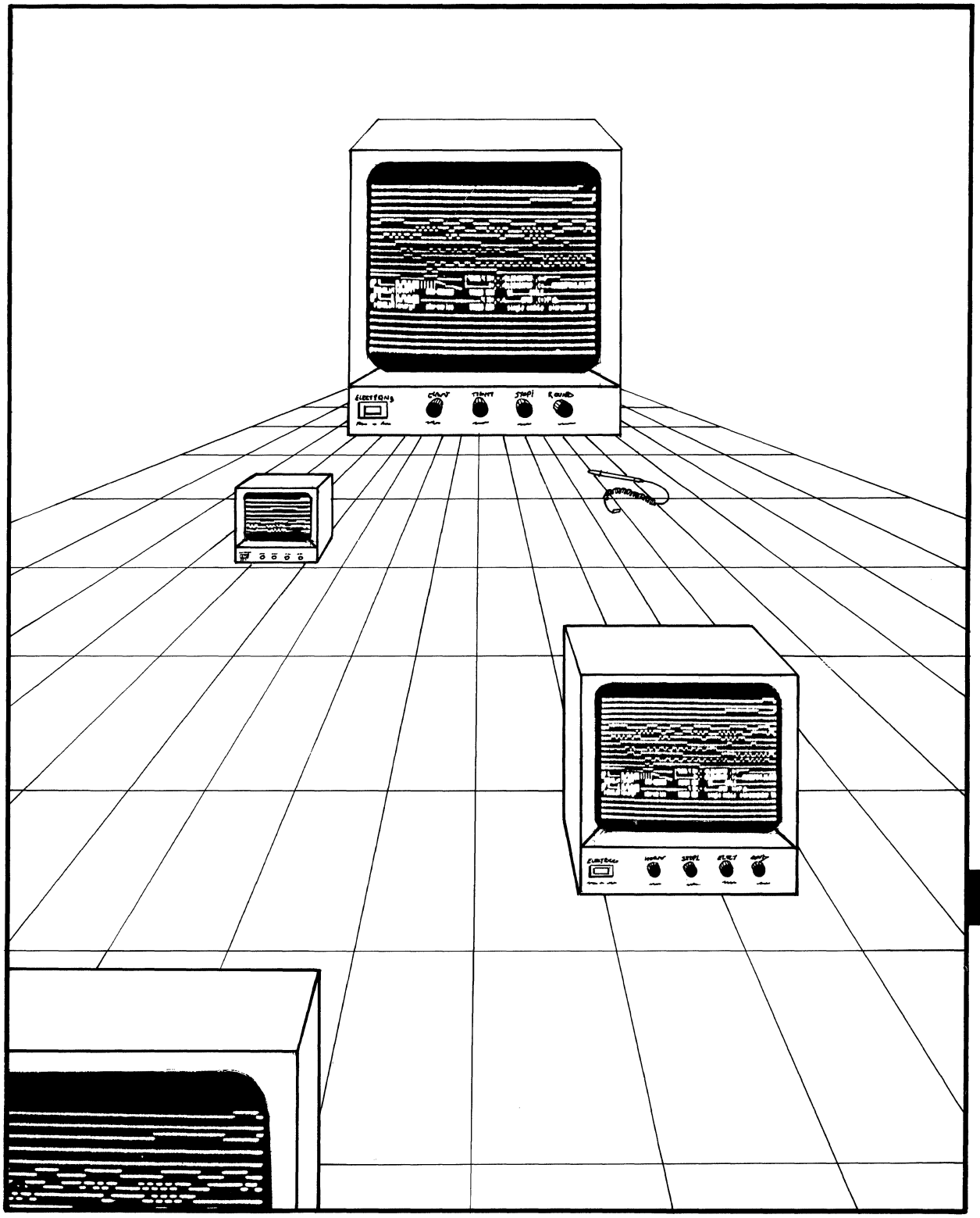
Note: The MTX-B1 is supplied with the ASCII character font as shown. However custom designed character fonts can be supplied at extra cost. For more details consult the factory.

**ORDERING INFORMATION:**
**MTX-B1**

## PACKAGE DIMENSIONS




| DIM | MM | | INCHES | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 51.562 | 52.832 | 2.030 | 2,080 |
| B | 13.081 | 15.240 | 0.515 | 0.600 |
| C | — | 5.588 | — | 0.220 |
| D | 3.175 | — | 0.125 | — |
| E | 2.286 | 2.794 | 0.090 | 0.110 |
| F | 1.524 | — | 0.060 | — |
| G | 0.813 | — | 0.032 | — |
| H | 0.406 | 0.508 | 0.016 | 0.020 |
| I | 3.683 | 4.750 | 0.145 | 0.187 |
| L | — | 15.875 | — | 0.625 |
| M | 0.254 | — | 0.010 | — |



# CRT MONITORS AND VIDEO ACCESSORIES

## SECTION 10 CRT MONITORS AND VIDEO ACCESSORIES

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MCM-2000L

## 19" HIGH-RESOLUTION (55 MHz) RGB COLOR MONITOR

- **55 MHz bandwidth**
- **19" screen size**
- **Designed for computer controlled color displays**
- **American or European operation**
- **Analog R,G,B video inputs**
- **Long persistence phosphors**
- **Interlaced/non-interlaced modes**
- **No flicker**
- **.31 mm dot triad pitch**

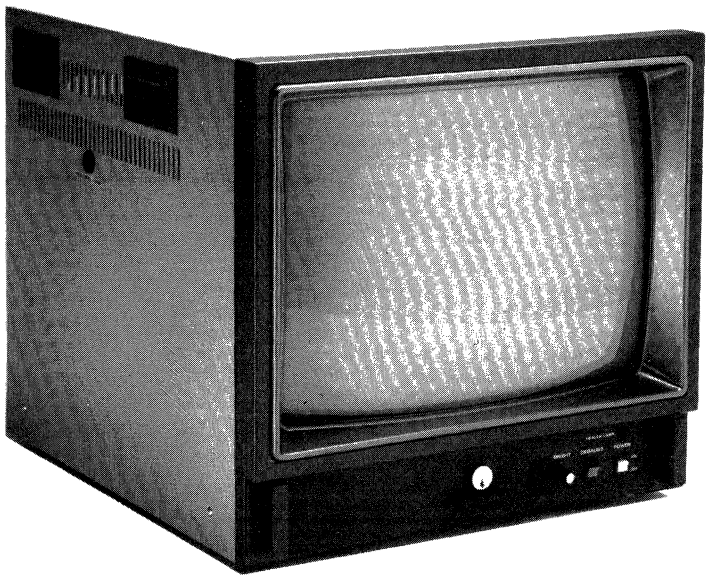
The Matrox MCM-2000L is a high quality color display monitor designed for high-resolution computer controlled color displays. This monitor is capable of displaying 1024 x 768 dots, non-interlaced at 55 Hz, or up to 1600 x 1200 dots interlaced at 30 Hz.

The MCM-2000L monitor uses a fine pitch shadow mask to provide high resolution color displays, and delta electron guns to maximize focus of individual dots to yield the highest resolution possible. Long persistence phosphors are used in the CRT to eliminate flicker in the display when the monitor is used in the interlaced mode.

Superior video signal regulation ensures the reliability of the displayed video information and raster size regulation circuitry maintains raster size within 1% of raster height. MCM-series monitors also offer internal circuitry protection through an anti-spark circuit which shunts dangerous voltage surges caused by arcing in the electron guns.

The MCM-series monitors operate using analog R,G,B video input signals which can be either non-composite or composite on green. The MCM-series monitors can operate at 60 Hz (American Standard) or 50 Hz (European Standard).





# SPECIFICATIONS

**ACTIVE DISPLAY AREA**

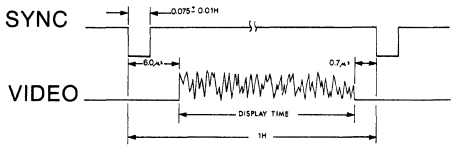
HEIGHT: 11.6 in. (29.5 cm)
WIDTH: 15.5 in. (39.4 cm)

**VIDEO BANDWIDTH**

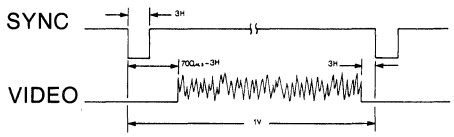
55 MHz

**TIMING DIAGRAM**

HORIZONTAL:




VERTICAL:




**SCANNING FREQUENCY**

HORIZONTAL RANGE: 37 KHz to 45 KHz
VERTICAL RANGE: 40 Hz to 70 Hz

**DOT TRIAD PITCH**

.31mm

**INPUT TERMINAL**

BNC connectors (high impedance or 75Ω — switch selectable)
All connectors are loop-through to permit daisy-chaining of monitors

**INPUT SIGNALS**

VIDEO SIGNALS: Analog, Positive white (composite sync on green drive)
HORIZONTAL SYNC.: TTL level, Negative
VERTICAL SYNC.: TTL level, Negative

**CONTROLS**

Power
Degauss
Brightness
Color/Monochrome
} (front mounted)

**MISCONVERGENCE**

STATIC: 0.50mm
DYNAMIC: 1.00mm

**AMBIENT TEMPERATURE**

0°C-40°C

**RELATIVE HUMIDITY**

95% (non-condensing)

**POWER SUPPLY**

100/115/120/220/240 Vac ± 10% 50/60 Hz (tap selectable)

**POWER CONSUMPTION**

200 W

**DIMENSIONS**

HEIGHT: 18.00 in. (45.2 cm)
WIDTH: 18.75 in. (47.6 cm)
DEPTH: 21.25 in. (53.9 cm)

**WEIGHT**

54 kg

**ORDERING INFORMATION**

MCM-2000L: 19" color display monitor
- No suffix — short persistance phosphor
- L — long persistance phosphor

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MCM-1000L

## 19" HIGH-RESOLUTION (40 MHz) RGB COLOR MONITOR

- **40 MHz bandwidth**
- **19" screen size**
- **Designed for computer controlled color displays**
- **American or European operation**
- **In-line electron guns**
- **Analog R,G,B video inputs**
- **Long persistence phosphors**
- **Interlaced/non-interlaced modes**
- **No flicker**
- **.31mm dot triad pitch**

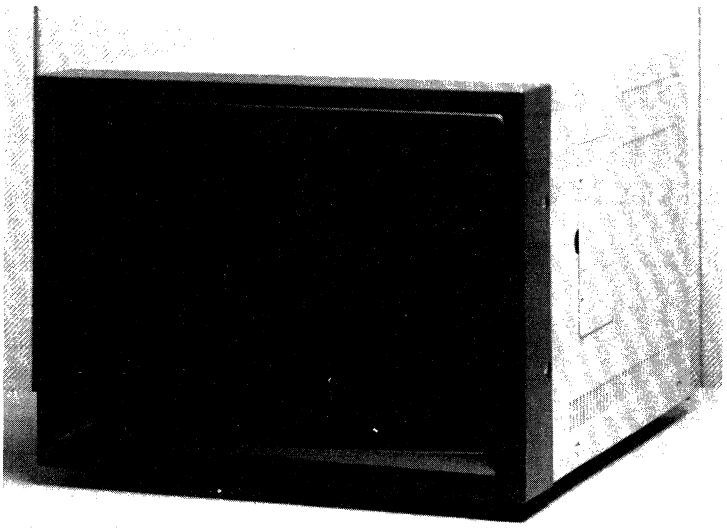
The Matrox MCM-1000L is a high quality color display monitor designed for high-resolution computer controlled color displays. This monitor is capable of displaying up to 768 x 576 dots non-interlaced at 60 Hz, or up to 1280 x 1024 dots interlaced at 30 Hz.

The MCM-1000L monitor uses a fine pitch shadow mask to provide high resolution color displays, and in-line electron guns to minimize color distortion due to convergence error. Long persistence phosphors are used in the CRT to eliminate flicker in the display when the monitor is used in the interlaced mode.

Superior video signal regulation ensures the reliability of the displayed video information and raster size regulation circuitry maintains raster size within 4mm. MCM-series monitors also offer internal circuitry protection through an anti-spark circuit which shunts dangerous voltage surges caused by arcing in the electron guns.

The MCM-series monitors operate using analog R,G,B, video input signals which can be either non-composite or composite in green. The MCM-1000L monitors accept video signals compatible with EIA-STD-RS-343, and can operate at 60 Hz (American Standard) or 50 Hz (European Standard).





# SPECIFICATIONS

**ACTIVE DISPLAY AREA**

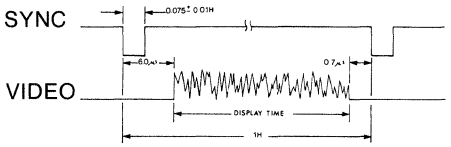
HEIGHT: 11.02 in. (27.0 cm)
WIDTH: 14.98 in. (35.0 cm)

**VIDEO BANDWIDTH**

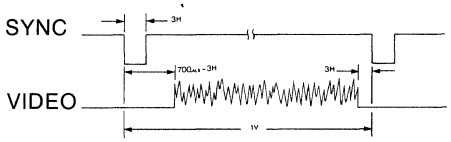
40 MHz

**TIMING DIAGRAM**

HORIZONTAL:




VERTICAL:




**SCANNING FREQUENCY**

HORIZONTAL RANGE: 28 KHz to 35 KHz
VERTICAL RANGE: 40 Hz to 60 Hz

**DOT TRIAD PITCH**

.31mm

**INPUT TERMINAL**

BNC connectors (high impedance or 75Ω — switch selectable)
All BNC connectors are loop-through to permit daisy-chaining of monitors

**INPUT SIGNALS**

VIDEO SIGNALS: Analog, Positive white (composite sync on green drive)
HORIZONTAL SYNC.: TTL level, Negative
VERTICAL SYNC.: TTL level, Negative

**CONTROLS**

Power
Degauss
Brightness
Gain
} (side mounted)

10

**MISCONVERGENCE**

STATIC: 0.75mm
DYNAMIC: 1.25mm

**AMBIENT TEMPERATURE**

0°C-40°C

**RELATIVE HUMIDITY**

95% (non-condensing)

**POWER SUPPLY**

100-120 Vac ±10% (50/60 Hz)
220-240 Vac ±10% (50/60 Hz)

**POWER CONSUMPTION**

200 W

**DIMENSIONS**

HEIGHT: 17.44 in. (38.5 cm)
WIDTH: 18.97 in. (48.2 cm)
DEPTH: 19.68 in. (45.0 cm)

**WEIGHT**

40 kg

**ORDERING INFORMATION**

MCM-1000L: 19" color display monitor
- No suffix — short persistance phosphor
- L — long persistance phosphor

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MCM-1014L

## 14" HIGH-RESOLUTION (40 MHz) RGB COLOR MONITOR

- **40 MHz bandwidth**
- **14" screen size**
- **Designed for computer controlled color displays**
- **American or European operation**
- **In-line electron guns**
- **Analog R,G,B video inputs**
- **EIA-STD-RS-343 video signal compatible**
- **Long persistence phosphors**
- **Interlaced/non-interlaced modes**
- **No flicker**
- **.31mm dot triad pitch**
- **Anti-glare shield**

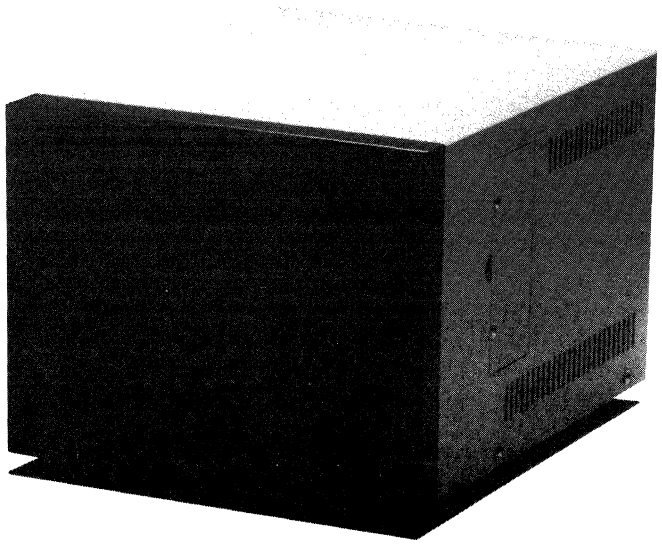
The Matrox MCM-1014L is a high quality color display monitor designed for high-resolution computer controlled color displays. This monitor is capable of displaying up to 768 x 576 dots non-interlaced at 60 Hz, or up to 1024 x 768 dots interlaced at 30 Hz.

The MCM-1014L monitor uses a fine pitch shadow mask to provide high resolution color displays, and in-line electron guns to minimize color distortion due to convergence error. Long persistence phosphors are used in the CRT to eliminate flicker in the display when used in the interlaced mode.

Superior video signal regulation ensures the reliability of the displayed video information and raster size regulation circuitry maintains raster size within 4mm. MCM-series monitors also offer internal circuitry protection through an anti-spark circuit which shunts dangerous voltage surges caused by arcing in the electron guns.

The MCM-series monitors operate using analog R,G,B video input signals which can be either non-composite or composite in green. The MCM-series monitors accept video signals compatible with EIA-STD-RS-343, and can operate at 60 Hz (American Standard) or 50 Hz (European Standard) in interlaced or non-interlaced mode.





# SPECIFICATIONS

**ACTIVE DISPLAY AREA**

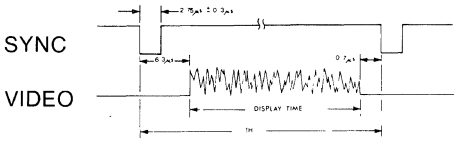
| | |
|---|---|
| HEIGHT: | 7.09 in. (18.0 cm) |
| WIDTH: | 9.84 in. (25.0 cm) |

**BANDWIDTH**

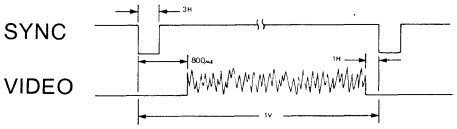
40 MHz

**TIMING DIAGRAM**

HORIZONTAL:




VERTICAL:




**SCANNING FREQUENCY**

| | |
|---|---|
| HORIZONTAL RANGE: | 28 KHz to 35 KHz |
| VERTICAL RANGE: | 50 Hz to 60 Hz |

**DOT TRIAD PITCH**

.31mm

**INPUT TERMINALS**

BNC connectors (high imdedance or 75 — switch selectable)
All connectors are loop-through to permit daisy-chaining of monitors

**INPUT SIGNALS**

| | |
|---|---|
| VIDEO SIGNALS: | Analog, Positive white (composite sync on green drive) |
| HORIZONTAL SYNC.: | TTL level, Negative |
| VERTICAL SYNC.: | TTL level, Negative |

**CONTROLS**

Power
Degauss
Gain
Brightness
} (side-mounted)

**MISCONVERGENCE**

| | |
|---|---|
| STATIC: | 0.50mm |
| DYNAMIC: | 0.80mm |

**AMBIENT TEMPERATURE**

0°C-40°C

**RELATIVE HUMIDITY**

95% (non-condensing)

**POWER SUPPLY**

100-120Vac ± 10% (50/60 Hz)
220-240Vac ± 10% (50/60 Hz)

**POWER CONSUMPTION**

160W

**DIMENSIONS**

| | |
|---|---|
| HEIGHT: | 10.86 in. (27.6 cm) |
| WIDTH: | 13.77 in. (35.0 cm) |
| DEPTH: | 17.80 in. (45.2 cm) |

**WEIGHT**

18kg

**ORDERING INFORMATION**

MCM-1014X: 14" high resolution color display monitor

X: No suffix — short persistance phosphors
L — long persistance phosphors

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MCM-19L

## 19" HIGH RESOLUTION (25 MHz) RGB COLOR MONITOR

- **Up to 6000 characters or 1140 x 810 dots**
- **19" screen size**
- **Designed for computer controlled color displays**
- **American or European operation**
- **In-line electron guns**
- **Analog R,G,B video inputs**
- **EIA-STD-RS-170 video signal compatible**
- **Long persistence phosphors**
- **Interlaced/non-interlaced modes**
- **No flicker**
- **.31mm dot triad pitch**

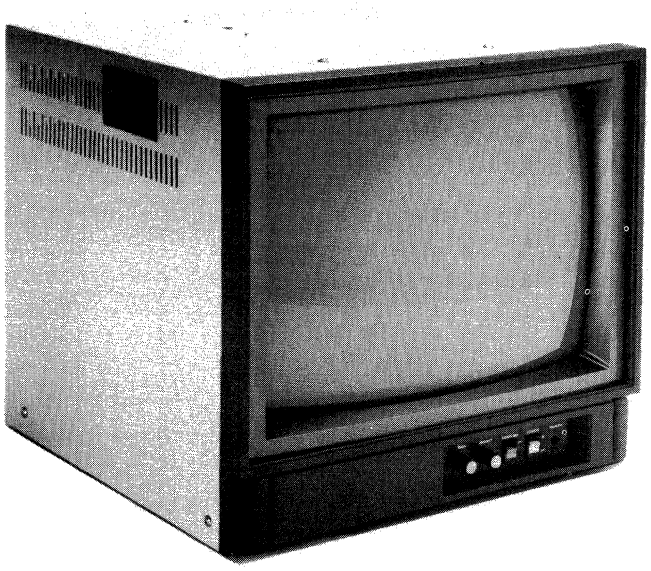
The Matrox MCM-19L is a high quality color display monitor designed for high-resolution computer controlled color displays. This monitor is capable of displaying up to 6000 characters or 1140 x 810 dots.

The MCM-19L monitor uses a fine pitch shadow mask to provide high resolution color displays, and in-line electron guns to minimize color distortion due to convergence error. Long persistence phosphors are used in the CRT to eliminate flicker in the display when used in the interlaced mode.

Superior video signal regulation ensures the reliability of the displayed video information and raster size regulation circuitry maintains raster size within 4mm. MCM-series monitors also offer internal circuitry protection through an anti-spark circuit which shunts dangerous voltage surges caused by arcing in the electron guns.

The MCM-series monitors operate using analog R,G,B video input signals which can be either non-composite or composite in green. The MCM-series monitors accept video signals compatible with EIA-STD-RS-170, and can operate at 60 Hz (American Standard) or 50 Hz (European Standard) in interlaced or non-interlaced mode.





# SPECIFICATIONS

**ACTIVE DISPLAY AREA**

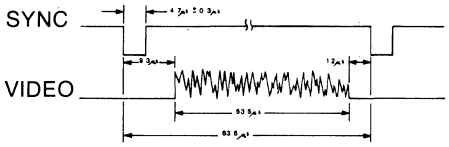
| | |
|---|---|
| HEIGHT: | 11.02 in. (28.0 cm) |
| WIDTH: | 14.98 in. (38.0 cm) |

**BANDWIDTH**

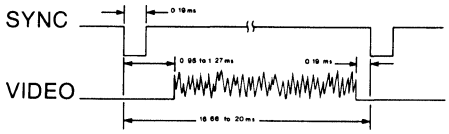
25 MHz

**TIMING DIAGRAM**

HORIZONTAL




VERTICAL:




**SCANNING FREQUENCY**

| | |
|---|---|
| HORIZONTAL RANGE: | 15.5 KHz to 19.0 KHz |
| VERTICAL RANGE: | 50 hz to 60 Hz |

**DOT TRIAD PITCH**

.31mm

**INPUT TERMINAL**

BNC connectors

**INPUT SIGNALS**

| | |
|---|---|
| VIDEO SIGNALS: | Analog, Positive white (composite sync on green drive) |
| HORIZONTAL SYNC.: | TTL level, Negative |
| VERTICAL SYNC.: | TTL level, Negative |

**MISCONVERGENCE**

| | |
|---|---|
| STATIC: | 0.75mm |
| DYNAMIC: | 1.25mm |

**AMBIENT TEMPERATURE**

0°C-40°C

**RELATIVE HUMIDITY**

95% (non-condensing)

**POWER SUPPLY**

100-120Vac ±10% (50/60 Hz)
200-240Vac ±10% (50/60 Hz)

**POWER CONSUMPTION**

240VA (140W)

**DIMENSIONS**

| | |
|---|---|
| HEIGHT: | 17.44 in. (44.3 cm) |
| WIDTH: | 18.97 in. (48.2 cm) |
| DEPTH: | 19.68 in. (50.0 cm) |

**WEIGHT**

27.5 kg

**ORDERING INFORMATION**

| | |
|---|---|
| MCM-19L: | 19" color display monitor |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MCM-14L

## 14" HIGH RESOLUTION (20 MHz) RGB COLOR MONITOR

- **Up to 4000 characters or 840 x 595 dots**
- **14" screen size**
- **Designed for computer controlled color displays**
- **American or European operation**
- **In-line electron guns**
- **Analog R,G,B video inputs**
- **EIA-STD-RS-170 video signal compatible**
- **Long persistence phosphors**
- **Interlaced/non-interlaced modes**
- **No flicker**
- **.31mm dot triad pitch**
- **Anti-glare shield**

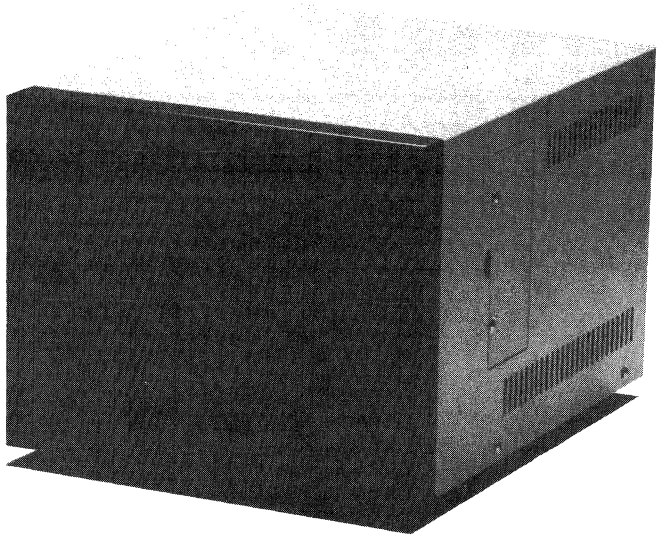
The Matrox MCM-14L is a high quality color display monitor designed for high-resolution computer controlled color displays. This monitor is capable of displaying up to 4000 characters or 840 x 595 dots.

The MCM-14L monitor uses a fine pitch shadow mask to provide high resolution color displays, and in-line electron guns to minimize color distortion due to convergence error. Long persistence phosphors are used in the CRT to eliminate flicker in the display when used in the interlaced mode.

Superior video signal regulation ensures the reliability of the displayed video information and raster size regulation circuitry maintains raster size within 4mm. MCM-series monitors also offer internal circuitry protection through an anti-spark circuit which shunts dangerous voltage surges caused by arcing in the electron guns.

The MCM-series monitors operate using analog R,G,B video input signals which can be either non-composite or composite in green. The MCM-series monitors accept video signals compatible with EIA-STD-RS-170, and can operate at 60Hz (American Standard) or 50Hz (European Standard) in interlaced or non-interlaced mode.





# SPECIFICATIONS

**ACTIVE DISPLAY AREA**

| | |
|---|---|
| HEIGHT: | 7.48 in. (19.0 cm) |
| WIDTH: | 10.4 in. (25.5 cm) |

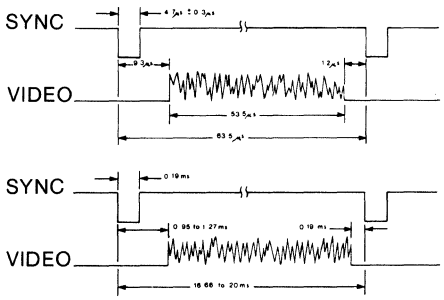
**BANDWIDTH**

20 MHz

**TIMING DIAGRAM**

HORIZONTAL:

VERTICAL:




**SCANNING FREQUENCY**

| | |
|---|---|
| HORIZONTAL RANGE: | 15.5 KHz to 19.0 KHz |
| VERTICAL RANGE: | 50 Hz to 60 Hz |

**DOT TRIAD PITCH**

.31mm

**INPUT TERMINALS**

BNC connectors

**INPUT SIGNALS**

| | |
|---|---|
| VIDEO SIGNALS: | Analog, Positive white (composite sync on green drive) |
| HORIZONTAL SYNC.: | TTL level, Negative |
| VERTICAL SYNC.: | TTL level, Negative |

**MISCONVERGENCE**

| | |
|---|---|
| STATIC: | 0.75mm |
| DYNAMIC: | 1.25mm |

10

**AMBIENT TEMPERATURE**

0°C-40°C

**RELATIVE HUMIDITY**

95% (non-condensing)

**POWER SUPPLY**

100-120Vac ± 10% (50/60 Hz)
220-240Vac ± 10% (50/60 Hz)

**POWER CONSUMPTION**

180VA (100W),

**DIMENSIONS**

| | |
|---|---|
| HEIGHT: | 10.86 in. (27.6 cm) |
| WIDTH: | 13.77 in. (35.0 cm) |
| DEPTH: | 17.80 in. (45.2 cm) |

**WEIGHT** 20kg

**ORDERING INFORMATION**

| | |
|---|---|
| MCM-14L: | 14" color display monitor |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MEC-12A

## 12" MEDIUM RESOLUTION RGB COLOR MONITOR

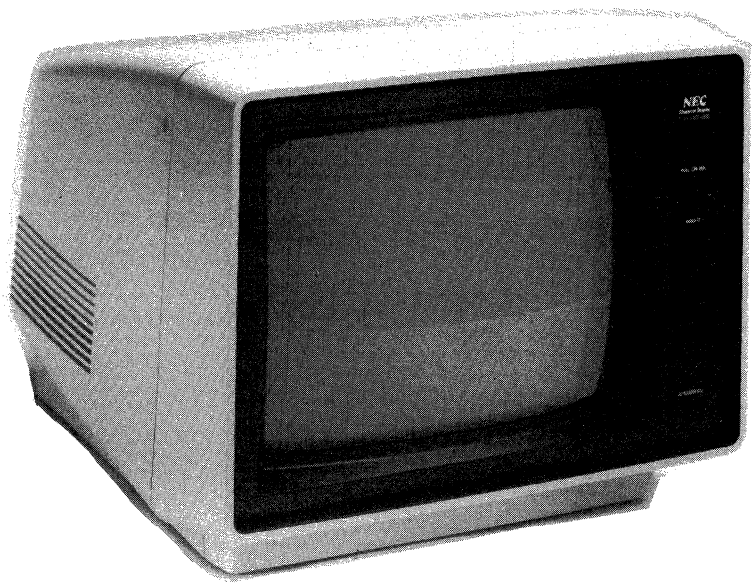
- **Up to 2000 characters or 690 x 280 dots**
- **Displays in 8 different colors**
- **Designed for computer controlled color displays**
- **Separate R,G,B and V,H sync. inputs**
- **Audio circuit (1.2W)**
- **In-line electron guns**
- **Short persistence phosphors**
- **TTL level video input**
- **Enhanced display stability**
- **Stable convergence**
- **.3mm dot triad pitch**

The Matrox MEC-12 is a high quality direct drive color display monitor designed for high resolution computer controlled color displays. The MEC-12's 12" screen can generate displays with up to 2000 characters (690 x 280 dots) in 8 colors.

The MEC-12 is equipped with a fine pitch shadow mask (.3mm dot triad pitch) for high resolution color displays, and in-line electron guns to minimize color distortion due to convergence error. The MEC-12's self convergence system controls convergence to within 0.6mm at the center of the screen and within 1.1mm around the perimeter. Short persistence phosphors are used in the MEC-12's CRT, to enable the use of a light pen.

Sharper, clearer pictures result from separate red, green, and blue TTL level video and vertical, horizontal sync. signals. Strict video signal regulation ensures the reliability of the displayed video information. The MEC-12's sophisticated circuit design ensures that variations in the power supply or environmental temperature can never affect display stability.





# SPECIFICATIONS

**ACTIVE DISPLAY AREA**

HEIGHT: 6.30 in. (16.0 cm)
WIDTH: 8.46 in. (21.5 cm)

**BANDWIDTH**

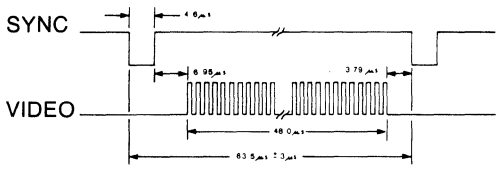
18 MHz

**DISPLAY COLORS**

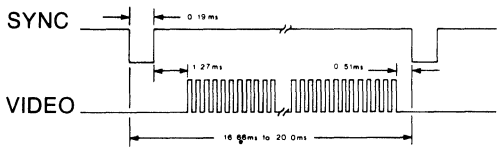
| INPUT | | | DISPLAY |
|---|---|---|---|
| R | G | B | COLOR |
| 0 | 0 | 0 | Black |
| 0 | 0 | 1 | Blue |
| 0 | 1 | 0 | Green |
| 0 | 1 | 1 | Cyan |
| 1 | 0 | 0 | Red |
| 1 | 0 | 1 | Magenta |
| 1 | 1 | 0 | Yellow |
| 1 | 1 | 1 | White |

**TIMING DIAGRAM**

HORIZONTAL:




VERTICAL:




**SCANNING FREQUENCY**

HORIZONTAL: 15.75 KHz
VERTICAL: 50 Hz to 60 Hz

**DOT TRIAD PITCH**

.3 mm

**INPUT TERMINAL**

8-pin connector (PC-8091(G) or equivalent)

**INPUT SIGNALS**

VIDEO SIGNALS: TTL level, Positive white
HORIZONTAL SYNC.: TTL level, Negative
VERTICAL SYNC.: TTL level, Negative

**MISCONVERGENCE**

DYNAMIC: 1.1mm
STATIC: 0.6mm

**AMBIENT TEMPERATURE** 0°C-40°C

**RELATIVE HUMIDITY** 95% (non-condensing)

**POWER SUPPLY** 100-120Vac ± 10% (60 Hz)

**POWER CONSUMPTION** 67W

**DIMENSIONS**

HEIGHT: 12.08 in. (30.7 cm)
WIDTH: 14.90 in. (37.8 cm)
DEPTH: 16.26 in. (41.3 cm)

**WEIGHT**

11.7 kg

**ORDERING INFORMATION**

MEC-12A: 12" color display monitor

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MCRT-9/14

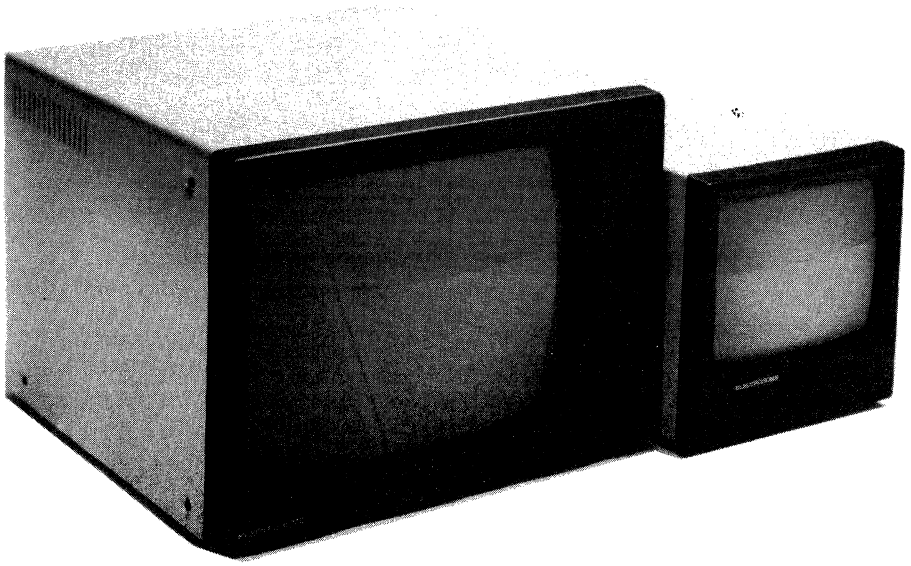
## 9" AND 14" MONOCHROME VIDEO MONITORS

- **18 MHz bandwidth**
- **Wide dynamic range**
- **Black level clamping**
- **Hum suppression**
- **Composite input video**
- **Enhanced display stability**
- **Internal/external sync**
- **American/European operation**
- **Attractive styling**
- **UL/CSA approved**

The MCRT series of video monitors are high quality monochrome display devices that are specifically designed for computer controlled display applications; including commercial, medical and industrial monitoring.

The MCRT series monitors operate using 1.0V p-p composite video input signals. The MCRT-9/G and 14/G versions are equipped with long persistence P39 phosphors enabling the monitors to operate in interlaced mode without flicker. Strict signal regulation ensures the reliability of the displayed video information.

Cabinets are constructed of Steltex textured steel and are finished in beige and brown. All units comply with CSA, UL, and DHEW regulations and standards.



# SPECIFICATIONS

**ACTIVE DISPLAY AREA**

| MONITOR | DISPLAY AREA | | | |
|---|---|---|---|---|
| | WIDTH | | HEIGHT | |
| | MM | IN | MM | IN |
| MCRT-9 | 181 | 7.12 | 135 | 5.31 |
| MCRT-14 | 290 | 11.42 | 215 | 8.46 |

**BANDWIDTH**

18 MHz

**SCANNING FREQUENCY**

HORIZONTAL RANGE: 15.75 KHz to 18.00 KHz
VERTICAL RANGE: 40 Hz to 65 Hz

**INPUT TERMINAL**

BNC connectors

**INPUT SIGNALS**

Composite video: 1.0V p-p nominal, negative sync

**AMBIENT TEMPERATURE**

0°-50°C

**RELATIVE HUMIDITY**

90% non-condensing

**POWER SUPPLY**

110/220/240 volts, 50/60 Hz

**POWER CONSUMPTION**

60W

**DIMENSIONS**

| MONITOR | WIDTH | | HEIGHT | | DEPTH | |
|---|---|---|---|---|---|---|
| | MM | IN | MM | IN | MM | IN |
| MCRT-9 | 222 | 8.74 | 220 | 8.66 | 352 | 13.85 |
| MCRT-14 | 400 | 15.74 | 251 | 9.88 | 451 | 17.75 |

**WEIGHT**

7.65kg (MCRT-9)
13.0kg (MCRT-14)

**ORDERING INFORMATION**

MCRT-XX/X

- No Suffix — P4 (white) phosphor
- G — P39 (green) long persistence phosphor
- 9 — 9" monochrome monitor
- 14 — 14" monochrome monitor

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TEL.: 514—735-1182 TELEX: 05-825651

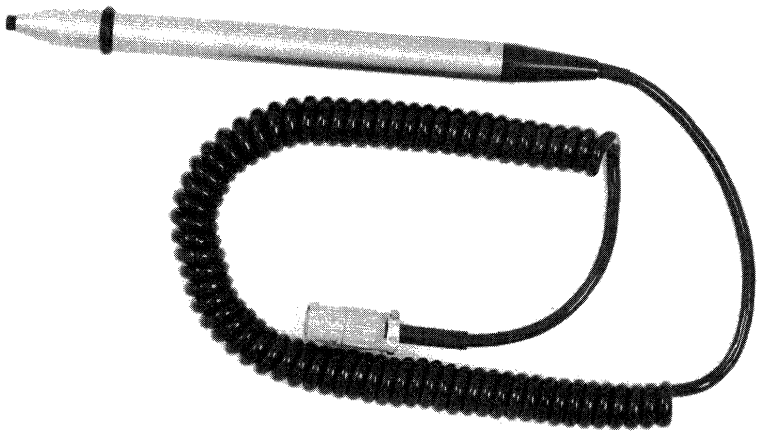
# LP-600

## HIGH SPEED LIGHT PEN

- **High sensitivity**
- **Sharply defined acceptance area**
- **Retractible cable with connector**
- **Light weight and small diameter for user comfort**
- **Push-tip or touch ring actuation**

The LP-600 is a high speed light pen that serves as an easy to use input device in interactive CRT display applications. The pen features high sensitivity, small barrel diameter for operator comfort, sharply defined acceptance area, push or touch actuation methods, and retractible cable with connector. The LP-600 is completely self-contained and requires only a single power supply voltage, +5V ±5%, 80 mA maximum.





# SPECIFICATIONS

**Functional**

**Luminous Sensitivity**
1 foot-lanbert

**Response Time**
300 nanosecond

**Spectral Response**
420-1100 nanometers

**Acceptance Area**
0.25 cm (0.10 in.) diameter

**Output-Light**
1 usec pulse, TTL compatible

**Output-Actuation**
Push Tip/Touch Ring — Level shift (TTL compatible) active high

**Background Tolerance**
Direct sunlight

**Cable**
Retractible, 120 cm (48 in.) extended, 35 cm (14 in.) retracted

**Mating Connector**
Viking TKR-07-100

**Power Requirements**
+5V ±5% @ 80mA

**Operating Temperature**
+10° — +50°C

**Dimensions**
Length: 6.00 in. (15.00 cm)
Diameter: 0.50 in. ( 1.25 cm)
Weight: 1.8 oz. (50 gr)

**Construction Material**
Pen Body: stainless steel
Pen Tip: polycarbonate

**Ordering Information**
LP-600

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# PLL-01

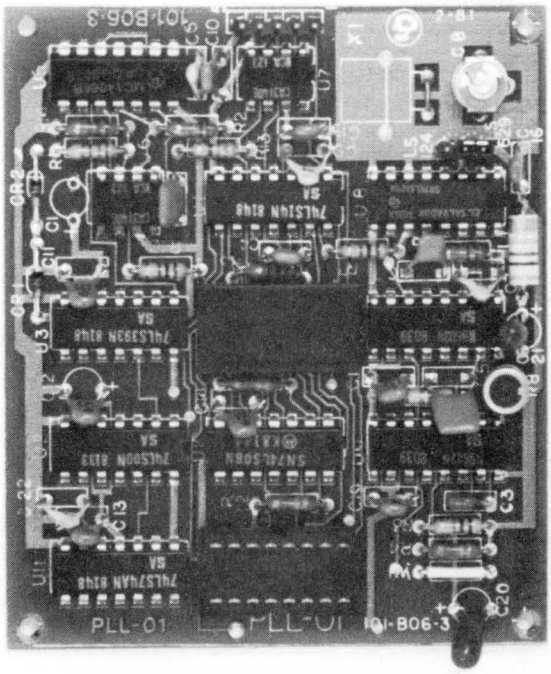
## EXTERNAL SYNC INTERFACE FOR VIDEO BOARDS

- **Synchronizes Matrox video controllers to an external sync source**
- **Composite sync or separate horizontal and vertical sync inputs**
- **Applications include closed circuit TV, broadcast, research, and industrial control**
- **Operates with 50/60 Hz sync**
- **Single +5V power supply**

The Matrox PLL-01 is a 3" x 3.5" module intended for use with the Matrox family of Video RAMs (VRAM) and video interface boards, in applications requiring external sync capabilities. This module allows the user to synchronize most Matrox video display products to a TV camera, studio master sync generator, etc. for applications requiring video mixing.

The PLL-01 requires only a single +5V power supply which can be obtained from the Matrox VRAM. The module interfaces directly to the VRAM. The PLL-01 can accept either composite or separate syncs. The user can also adjust the relative horizontal and vertical delay, to position the VRAM picture relative to the external syncs.

Typical applications exist in closed circuit TV, broadcast, research, and industrial control environments where alphanumeric and/or graphic data must be overlaid on a TV camera picture.

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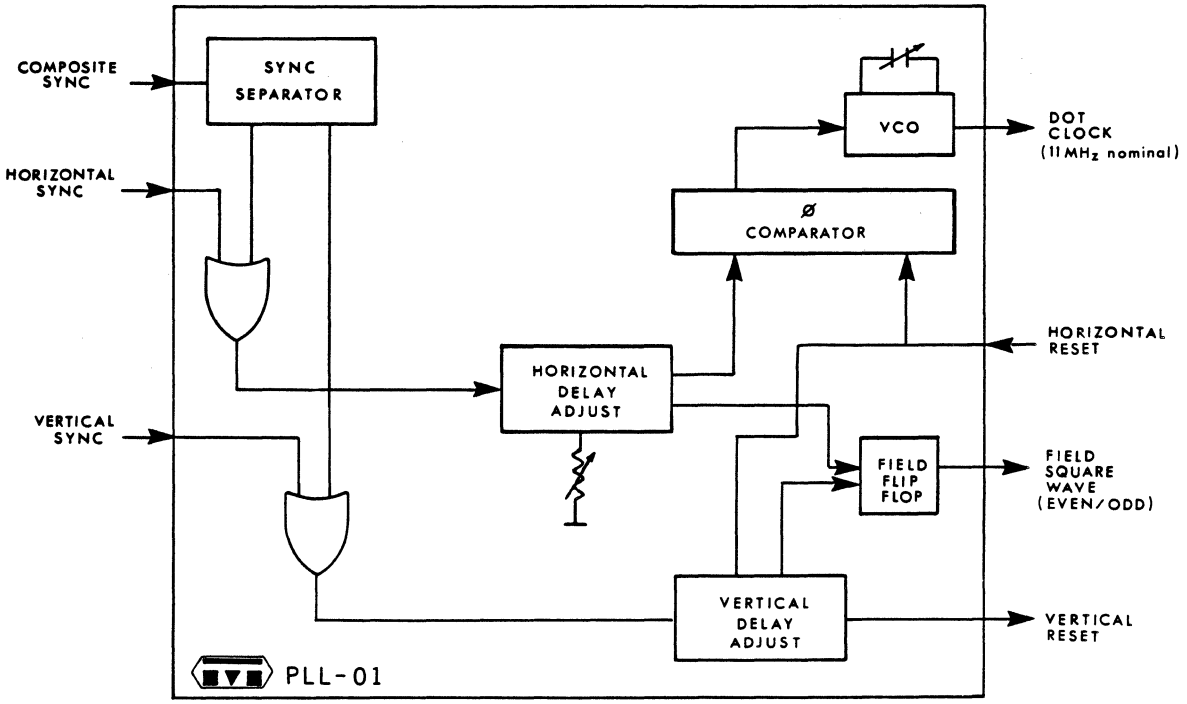


# SPECIFICATIONS

**Compatibility**

| | | |
|---|---|---|
| MSBC-512 | MLSI-512 | MDC-512 |
| NSBC-512 | MLSI-2480 | MDC-2480 |
| MSBC-2480 | EXO-512 | ALT-512 |
| STD-256 | EXO-2480 | ALTR-2480 |
| STD-2480 | MMD-2480 | MMD-256 |

**Input Signals**

Composite Sync
Horizontal Sync
Vertical Sync
Horizontal Reset

**Output Signals**

Dot Clock
Vertical Reset
Field Square Wave

**Connector**

16 pin DIP socket (AUGAT 516-16-37D)

**Dimensions**

Height: 3.0 in. (7.62 cm)
Width: 3.5 in. (8.89 cm)
Depth: 0.5 in. (1.27 cm)

**Power Requirements**

+5V ± 5%

**Environmental Requirements**

Operating Temperature: 0 - 55°C
Relative Humitidy: 0 - 95% (non-condensing)

**Ordering Information**

PLL-01

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# CABLES

## CABLES FOR MATROX VIDEO BOARDS

Matrox offers several standard cable assemblies for use with the graphics product line.

| PART NUMBER | DESCRIPTION |
|---|---|
| 15501-A01-00 | 2 header 50-pin ribbon cable for use with: BW-ALPHA/QBW-ALPHA, RGB-ALPHA/QRGB-ALPHA, RGB-GRAPH/QRGB-GRAPH, VAF-512/QVAF-512 } Video Bus |
| 15502-A01-00 | 3 header 50-pin ribbon cable for use with: BW-ALPHA/QBW-ALPHA, RGB-ALPHA/QRGB-ALPHA, RGB-GRAPH/QRGB-GRAPH, VAF-512/QVAF-512 } Video Bus |
| 15503-A01-00 | 4 header 50-pin ribbon cable for use with: BW-ALPHA/QBW-ALPHA, RGB-ALPHA/QRGB-ALPHA, RGB-GRAPH/QRGB-GRAPH, VAF-512/QVAF-512 } Video Bus |
| CABX/1 | Set of three 2 connector ribbon cables for use with the GXB-1000 (one VGM-1000 to one RMB-1000) |
| CABX/2 | Set of three 3 connector ribbon cables for use with the GXB-1000 (one VGM-1000 to two RMB-1000s) |
| CABX/3 | Set of three 4 connector ribbon cables for use with the GXB-1000 (one VGM-1000 to three RMB-1000s) |
| CABX/4 | Set of three 5 connector ribbon cables for use with the GXB-1000 (one VGM-1000 to four RMB-1000s) |
| 15004-A01-00 | 4 foot video output cable (RGB color/grey-scale) for use with:<br>BW-ALPHA/QBW-ALPHA GXB-1000<br>RGB-ALPHA/QRGB-ALPHA CTM-300/R<br>RGB-GRAPH/QRGB-GRAPH CTM-300/BRD<br>VAF-512/QVAF-512 CTM-300<br>10-pin AMP connector to four BNC connectors. |
| 15006-A01-00 | 6 foot BNC to BNC cable |
| KBL-4 | Video cable for CTM-300M terminal (with MEC-12 monitor)<br>10-pin connector (AMP 87922-1) to 8-pin connector (NEC PC-8091(G)) |
| KBL-4A | Video cable for CTM-300M terminal (with MEC-12A monitor)<br>10-pin connector (AMP 87922-1) to 8-pin connector (NEC PC-8091(G)) |

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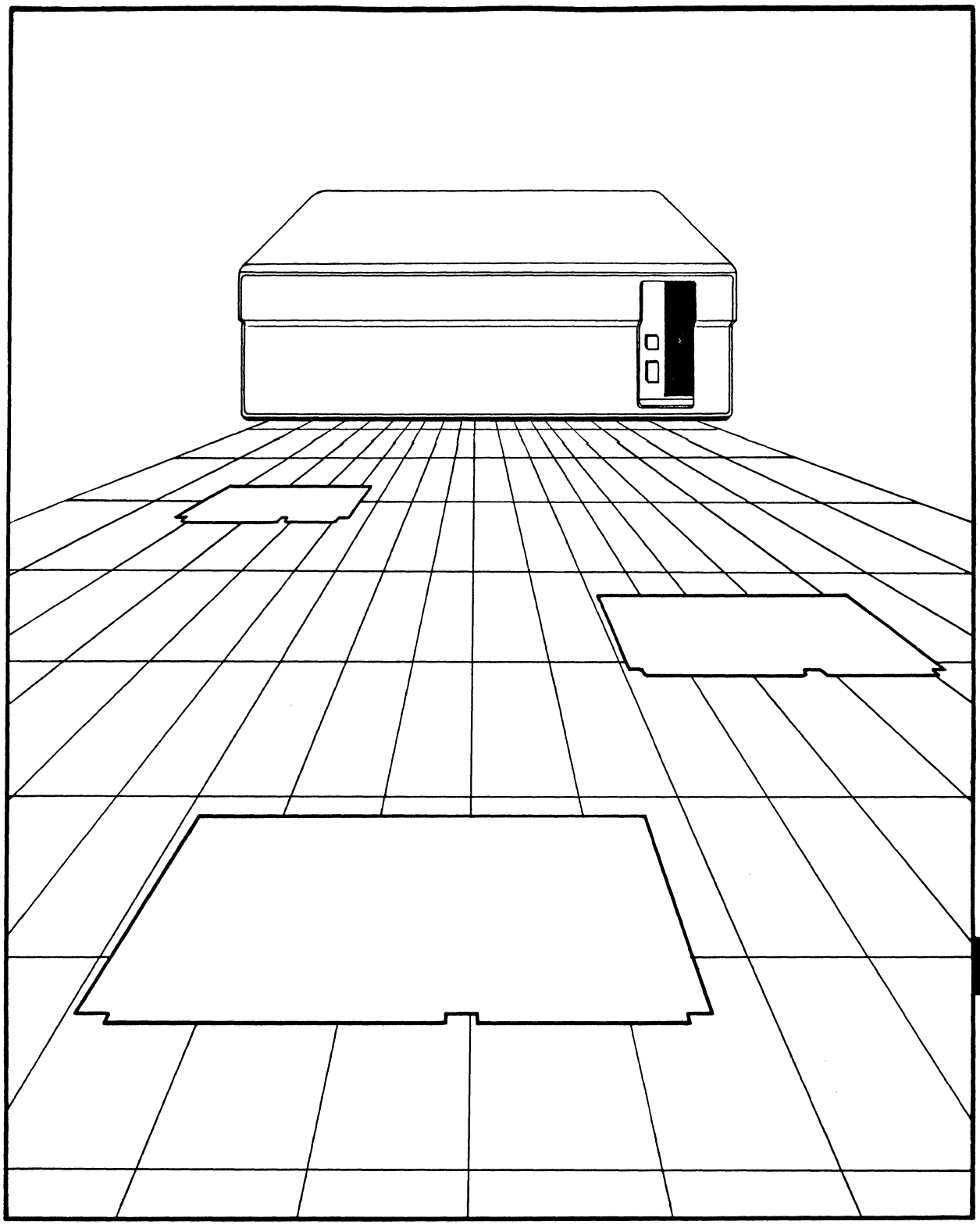


# MULTIBUS CPU BOARDS

## SECTION 11 MULTIBUS CPU BOARDS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

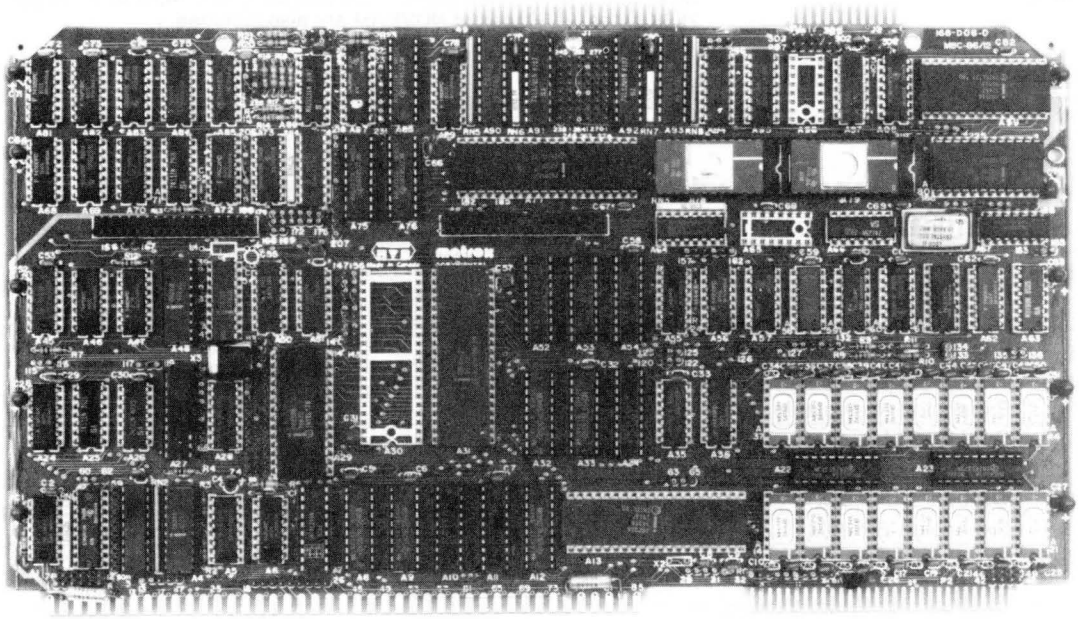
# MBC-86/12A

## HIGH PERFORMANCE 16-BIT MULTIBUS CPU BOARD

- **CPU — Powerful 16-bit 8086**
- **RAM — Up to 128K bytes dual ported**
- **EPROM — Up to 32K bytes**
- **PARALLEL I/O — 24 programmable lines**
- **SERIAL I/O — One RS-232C port**
- **8 MHz CPU available (standard 5 MHz)**
- **On board socket for 8087 NDP co-processor**
- **Direct replacement for iSBC-86/12A and iSBC-86/30**
- **Can emulate iSBC-86/12A and iSBC-86/30**
- **Multibus compatible**
- **1 Megabyte addressing range**
- **2 programmable hardware timers**
- **9 interrupt levels (externally expandable to 65 levels)**
- **2 iSBX connectors**

The MBC-86/12 is a member of the Matrox line of modular Multibus*-compatible single board computers. Featuring the 8086 16-bit CPU, the MBC-86/12 is software compatible with the Intel iSBC-86/12A and iSBC-86/30 CPU boards. The MBC-86/12 also offers several enhancements over the Intel boards: 128K byte on-board RAM, 8087 arithmetic coprocessor, optional 8 MHz version for faster cycle times, and two iSBX connectors for expansion.

The MBC-86/12 offers the system designer a base for a potentially powerful system. Programmable I/O interfaces provide the flexibility required to adapt the MBC-86/12 to virtually any combination of I/O peripherals. Moreover, the MBC-86/12 features master-slave capabilities for applications requiring multiprocessor configurations and/or high speed peripheral control.



# MBC-86/12A FEATURES:

**Fast Cycle Times**

The 8086 CPU is internally divided into an independent Execution Unit and Bus Interface Unit. This allows the CPU to maintain an instruction queue and thereby significantly reduce instruction cycle time.

**Powerful Instructions Set**

8086 operations include: multiplication and division of signed/unsigned binary numbers, move, scan, and compare, for strings of up to 64K bytes. Also the 8086 can perform non-destructive bit testing, byte translations, and software generated interrupts.

**Ram Priority**

On-board memory refresh is guaranteed through a RAM access priority scheme. The on-board CPU takes precedence over the Multibus* system bus for access to on-board RAM.

**Local Memory**

On-board RAM can be protected from system accesses in multiples of 8K bytes on 32K byte boards (multiples of 16K bytes on 128K byte boards).

**Catastrophic Interrupt**

A non-maskable interrupt line is available on-board to signal a catastrophic event (such as an impending power failure).

**Minimal Real Time Overhead on Interrupt**

A programmable interrupt controller generates an 8-bit pointer to a service routine on interrupt. Eight interrupt levels are supported.

**Hardware Generated Time Delays**

A 8253 Programmable Interval Timer can support up to three independent counter/timer functions. This feature eliminates the need to maintain timing loops in software thereby minimizing the system's software overhead.

**Flexible I/O Interfacing**

A programmable peripheral interface lends flexibility to the MBC-86/12's interfacing cababilities. This allows the MBC-86/12 to be "tailored" to suit most I/O requirements.

**Programmable Serial Interface**

Baud rate, synchronous/asynchronous operation, number of bits per character, etc. are all user-selectable.

**Power Failure Protection**

An auxiliary power bus is included to protect the contents of the on-board RAM during a power failure.

**Optional Coprocessor Expansion**

An optional 8087 coprocessor is available to further enhance the performance of the MBC-86/12.

**iSBX-BUS Expansion**

Two iSBX-Multimodule* connectors are included on-board for further expansion.

**CPU Upgrade**

The MBC-86/12 is also available in an 8 MHz version for increased throughput.

**CPU Expansion**

An optional piggy-back board increases on-board ROM to 128K bytes and RAM to 256K bytes. 256 bytes of NOVRAM are also included.

11

## Matrox's MBC-86/12A in comparison with Intel's iSBC-86/12A and iSBC-86/12

| FEATURE | MBC-86/12 | iSBC-86/12A | iSBC-86/30 |
|---|---|---|---|
| iSBC-86/12 Software Compatibility | YES | YES | YES |
| iSBC-86/30 Software Compatibility | YES | NO | YES |
| Clock Rate (MHz) | 5 or 8 | 5 | 5 or 8 |
| 8087 Coprocessor Socket | YES | NO | NO |
| Two iSBX Connectors | YES | NO | YES |
| Expansion Nonvolatile RAM | YES | NO | NO |
| Dual Port Memory Lock | YES | NO | YES |
| 24-bit Multibus Address Space | YES | NO | YES |
| On-board EPROM | 32KB | 16KB | 64KB |
| Expansion EPROM | 128KB | 32KB | 64KB |
| On-board RAM | 32KB/128KB | 32KB | 128KB |
| Expansion RAM | 256KB | 64KB | 256KB |
| Dual Port RAM for Multibus | 128KB | 64KB | 256KB |

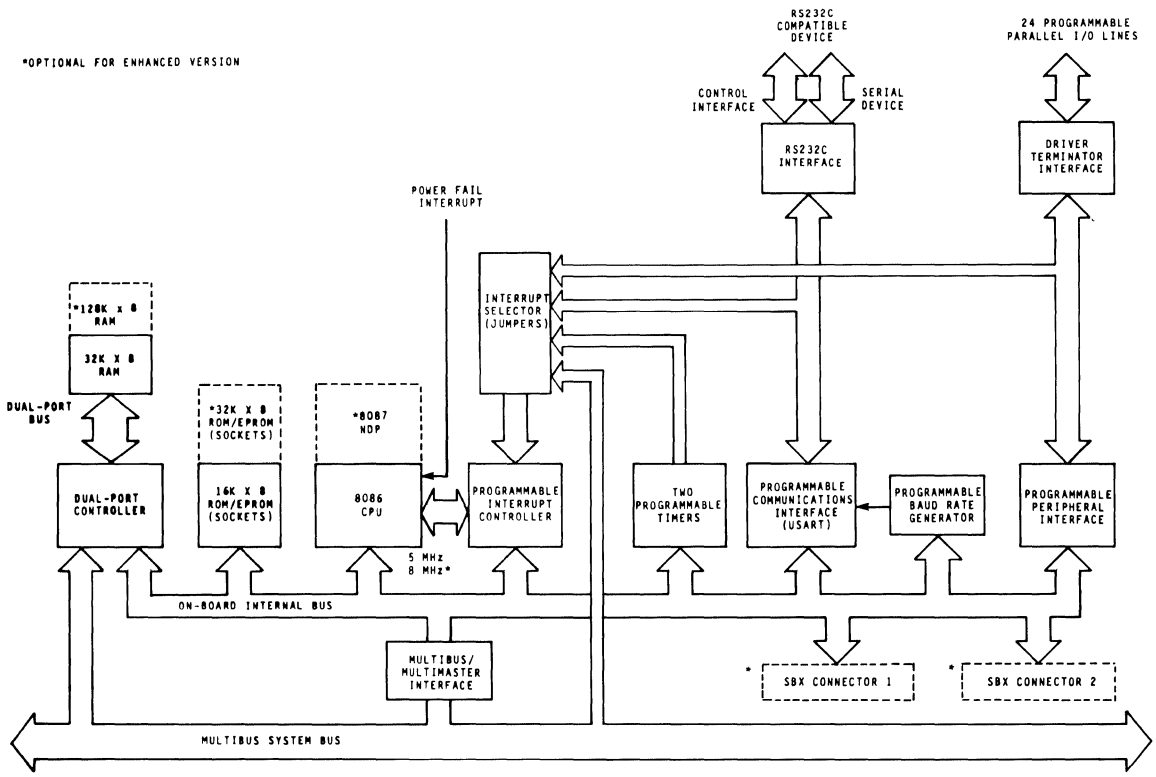



**Figure 1: MBC-86/12 Block Diagram**

The Matrox MBC-86/12 high power 16-bit CPU card is an enhanced version of Intel's iSBC 86/12A. The MBC-86/12 and the iSBC 86/12 are fully software compatible. The MBC-86/12 will run any Intel software without modifications.

The user can upgrade existing or new designs based on the iSBC 86/12 with a high speed 8 MHz CPU, more RAM (128K bytes), arithmetic processor (8087 NDP) and two iSBX connectors for Multimodules.

Other features include a programmable interrupt controller, programmable serial and parallel communications interfaces, programmable timers, up to 128K bytes on board RAM, and sockets for up to 32K bytes ROM/EPROM. Connecting a battery to the auxiliary connector allows saving of RAM contents in the event of a power failure.

For upgrading existing Multibus systems from 8 bits to 16 bits or for upgrading iSBC 86/12A systems the MBC-86/12 is ideal. All Multibus signals are supported and, with the auxiliary connector, battery power back-up may be implemented.

A full range of supporting products such as floppy disk controllers, 512K byte memory boards, CRT display interfaces and a system chassis are also available.

## CENTRAL PROCESSING UNIT

The core of the MBC-86/12 is an 8086 microprocessor chip. The 8086 is a third generation microprocessor which can accommodate 8 or 16-bit data transfers and is housed in a standard 40-pin dual in-line package operating from a single +5V power supply.

The 8086 CPU is substantially more powerful than earlier designs. Actual performance varies from application to application, but comparison to the industry standard 2MHz 8080A shows the 8086 to be seven to ten times more powerful. The high performance of the 8086 is realized by combining a 16-bit internal data path with a pipelined structure that allows instructions to be prefetched during spare bus cycles. Also contributing to performance is a compact instruction format that enables more instructions to be fetched in a given amount of time. Execution times of 1.2μs (800ns if instruction is in the queue) are provided with the 5MHz CPU, faster times are attainable with the 8MHz version (see specifications).

**Architecture** — The 8086 CPU is internally divided into two operational sections (figure 2): the Execution Unit (EU) and the Bus Interface Unit (BIU). The BIU maintains an instruction queue, which can store up to six instruction bytes, as well as performing all bus operations for the EU. Using the instruction queue, the BIU can keep the EU supplied with prefetched instructions without monopolizing the system bus. Both the BIU and the EU can operate independently of each other and are able to extensively overlap instruction fetch with execution. This technique significantly reduces the time required to execute instructions.

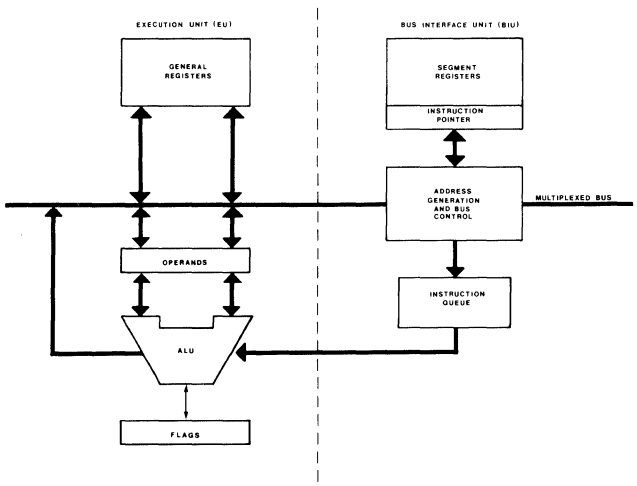



**Figure 2. Execution and Bus Interface Units (EU and BIU)**

**Instruction Set** — The instruction set of the 8086 is essentially a superset of the 8080A/8085A instruction set. Operations unique to the 8086 include: multiplication and division of signed and unsigned binary numbers as well as unpacked decimal numbers, move, scan and compare operations for strings of up to 64K bytes in length, non-destructive bit testing, byte translations from one code to another, software generated interrupts and instructions that can help coordinate the activities of multiprocessor systems. Instructions can be 8, 16, 24 or 32 bits long and may be aligned on byte or word boundaries.

## RAM CAPABILITIES

The MBC-86/12 is supplied with 32K bytes of on-board dynamic RAM in the basic version. Moreover enhanced versions are available which contain up to 128K bytes of dynamic read/write memory on-board. Off-board memory is expandable to 1M byte of any user specified combination of RAM, ROM or EPROM. Also contained on-board is a dual port controller which allows access to the on-board RAM from the MBC-86/12 CPU or from any other Multibus* master via the system bus. Data transfers to RAM from the system bus can be done, through the dual port controller, in either byte (8-bit) or word (16-bit) modes. All accesses to the on-board RAM by the MBC-86/12 are handled over a 16-bit data path. Priorities have been established whereby memory refresh is quaranteed by the on-board refresh logic and the on-board CPU has priority over Multibus* system bus requests for access to RAM. The dual port controller includes independent addressing logic for RAM accesses from the on-board CPU and from the Multibus* system bus. Straps are provided so that the system bus can position the base address of on-board RAM to any 8K byte boundary on any 128K byte segment of the 1M byte system address space. In addition to this, the MBC-86/12 has the capability to protect on-board memory from Multibus* system access. Any or all of the on-board memory can be protected in 8K byte segments (16K byte segments for 128K byte enhanced version). This feature allows multiprocessor systems to establish local memory for each processor and shared memory configurations where the total system memory size (including local on-board memory) can exceed 1M byte without addressing conflicts. Power for the on-board RAM and refresh circuitry may be optionally provided by an auxiliary power bus, and memory protect logic is included for RAM battery back-up requirements.

## EPROM/ROM CAPABILITIES

Sockets are included on the MBC-86/12 to accommodate up to 32K bytes of user-installed nonvolatile read-only memory. EPROM/ROM may be added in either 4K, 8K or 16K byte increments. Data is transfered to and from the on-board EPROM/ROM over a 16-bit data path.

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| Mode | Operation |
|---|---|
| Fully-nested | Interrupt request line priorities fixed at 0 as highest, 7 as lowest. |
| Auto-rotating | Equal priority. Each level, after receiving service, becomes the lowest priority level until the next interrupt occurs. |
| Specific priority | System software assigns lowest priority level. Priority of all other levels based on sequence numerically on this assignment. |
| Polled | System software examines priority-encoded system interrupt status via interrupt status register. |

**Table 1. Programmable Interrupt Modes**

| Function | Operation |
|---|---|
| Interrupt on terminal count | When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks. |
| Programmable one-shot | Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable. |
| Rate generator | Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period. |
| Square-wave rate generator | Output will remain high until one half the count has been completed, and then go low for the other half of the count. |
| Software triggered strobe | Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period. |
| Hardware triggered strobe | Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable. |
| Event counter | On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system. |

**Table 2. Programmable Timer Functions**

## PROGRAMMABLE INTERRUPT CONTROLLER

The MBC-86/12 recognizes nine vectored interrupt levels (expandable to 65 levels by cascading interrupt controllers via the Multibus* system bus). The highest level of these interrupts is the non-maskable interrupt (NMI) which is tied directly to the CPU and is usually used to signal a catastrophic event, such as a power failure. The other eight levels are managed through an 8259 Programmable Interrupt Controller. The Interrupt Controller initiates interrupts on a priority basis and can assign priorities to each level by one of four priority modes (Table 1). Priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment. The interrupt controller is programmed by the system's software as an I/O peripheral.

**Interrupt Sequence** — The Programmable Interrupt Controller can accept interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus or directly from peripheral equipment. When the interrupt controller receives an interrupt request it will evaluate the request according to the programmed priority mode and send an INT signal to the CPU, if appropriate. Upon acknowledgment of the interrupt request by the CPU (INTA), the interrupt controller releases an 8-bit pointer onto the data bus where it is read by the CPU. This pointer contains the code segment and offset at which the service routine for that interrupt is located. The CPU will then store it's status flags on the stack and execute an indirect CALL instruction through the vector location to the service routine. Each interrupt request input can be masked individually, via software, by storing a single byte in the Interrupt Mask Register in the interrupt controller. An Interrupt request can be recognized through either level-sensitive or edge-sensitive input circuitry.

## PROGRAMMABLE INTERVAL TIMER

The MBC-86/12 provides for accurate generation of time delays through an on-board 8253 Programmable Interval Timer. The 8253 is made up of three independent 16-bit counters, each with a count rate of up to 2MHz. By using the 8253 to generate time delays, the necessity of establishing timing loops in system software is eliminated. Therefore the software overhead is minimal. Using the Programmable Interval Timer, in conjunction with the 8259A Interrupt Controller, to generate an interrupt to the CPU on terminal count allows the user to maintain multiple delays by assignment of priority levels. Also non-delay type timer/counter functions can be implemented with the 8253. These non-delay functions include: Programmable Rate Generator, Event Counter, Binary Rate Multiplier, Real-Time Clock, Digital One-Shot and Complex Motor Controller. The outputs from the 8253 may be independently routed, through hardware straps, to the 8259A Interrupt Controller and to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, or may be routed as inputs to the 8255A. The gate/trigger inputs may be routed to I/O terminators or as outputs from the 8255A. Note that the third counter in the 8253 is used by the MBC-86/12 to provide the programmable baud rate generator for the board's RS-232C USART serial port.

**Programming** — Each counter in the 8253 is a 16-bit presettable down counter that can operate either in binary or binary-coded decimal (BCD). Each counter is initialized by loading an 8-bit control word into an internal register (control words specify the counter to be used, mode of operation, and whether the count is to be in binary or BCD), followed by the count value. Each counter is fully independent and can have separate modes of operation (Table 2), and count type (binary or BCD). Special features in the control words handle the loading of the count so that software overhead is minimized. Also special commands and logic are included so that the contents of each counter can be read "on the fly" without having to inhibit the clock input. The 8253 Programmable Interval Timer is seen by the CPU as an array of I/O ports in system memory and therefore can be programmed by the system software with simple I/O operations.

## PARALLEL I/O INTERFACE

The MBC-86/12 utilizes an 8255A Programmable Peripheral Interface (PPI) whose function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer board. Contained within the 8255A are three 8-bit ports (A, B and C) each of which may be assigned one of three basic modes of operation (Table 3). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs in conjunction with Port A and Port B. Operational modes for the 8255's I/O ports may be combined so that their functional description can be "tailored" to almost any I/O structure. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers. Hence the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers to provide the required sink current, polarity and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven or round cables.

**Programming** — The 8255A is programmed by the system software so that normally no external logic is required to interface peripheral devices or structures. During execution of the system program any of the operational modes may be selected using a single OUTput instruction. This allows a single 8255A to service a veriety of peripheral devices with a simple software maintenance routine. The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the definition of Ports A and B. Any of the eight bits of Port C can be set or reset using a single OUTput instruction. This feature reduces software requirements in control-based applications.

## SERIAL I/O INTERFACE

An 8251A Programmable Communications Interface is incorporated into the MBC-86/12. Used as a peripheral device by the CPU, the 8251A is programmed by system software to operate using virtually any serial data transmission technique presently in use. The 8251A Universal Asynchronous/Synchronous Receiver/Transmitter (USART) accepts data characters from the CPU in parallel format and then converts them into a continuous data stream for transmission. Simultaneously it can receive data as a serial stream and convert it to a suitable parallel format to be read by the CPU. The mode of operation (synchronous or asynchronous), data format, control character format, parity and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capabilities. Parity, overrun and framing error detection are all incorporated on-chip. The RS-232C interface on the MBC-86/12, in conjunction with the 8251A USART, provides a direct interface to RS-232C compatible peripherals (terminals, cassettes, asynchronous and synchronous modems, etc). The RS-232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS-232C round or flat cables.

| Port | Lines (qty) | Mode of Operation | | | | | |
|---|---|---|---|---|---|---|---|
| | | Unidirectional | | | | Bidirectional | Control |
| | | Input | | Output | | | |
| | | Latched | Latched & Strobed | Latched | Latched & Strobed | | |
| A | 8 | X | X | X | X | X | |
| B | 8 | X | X | X | X | | |
| C | 4 | X | | X | | | X1 |
| | 4 | X | | X | | | X1 |

**Note:**
1. Part of Port C must be used as a control port when either Port A or Port B is used as a latched and strobed input or a latched and strobed output port or if Port A is used as a bidirectional port.

**Table 3. Input/Output Port Modes of Operation**

## SYSTEM BUS INTERFACE

The MBC-86/12 interfaces directly to the industry standard Multibus*. All address, data, and control signals conform to the Intel Multibus Specification No. 9800683. A failsafe timer is included in the MBC-86/12's design which can be used to generate an interrupt if an addressed device does not respond within 6 msec.

**Multimaster Capabilities** — The MBC-86/12 is ideally suited for systems requiring additional processing capacity and the benefits of multiprocessing (several CPUs and/or controllers logically sharing system tasks through communications over the system bus). On-board control logic allows up to three bus masters to share the system bus in serial (daisy chain) priority fashion or up to 16 masters to share the Multibus* with the addition of an external priority network.

## HARDWARE EXPANSION

Matrox supports the MBC-86/12 with a variety of specialized IC chips. These chips can easily be integrated on board to provide added power and versatility.

**8 MHz CPU** — For special applications requiring very high speed execution times, the MBC-86/12 is available in 8 MHz version.

**128K byte RAM** — On-board random access memory can be expanded up to 128K bytes for applications requiring large amounts of local storage area. On-board RAM can be protected from system access in 16K byte segments to allow multiprocessor systems to establish protected local memory.

**iSBX-Bus expansion** — The MBC-86/12 contains two iSBX Multimodule* connectors which can accept any of the iSBX Multimodules (8087 Numeric Data Processing Module, 8089 Input/Output Processing Module, Fixed Point Math Module, Floating Point Math Module, etc.). In this way the MBC-86/12 can be easily upgraded to meet the specific requirements of most applications.

**Numeric Data Processor (NDP)** — The MBC-86/12 includes a socket to accept an 8087 Numeric Data Processor IC chip (NDP). The NDP option allows for easy implementation of floating point (32 and 64 bit), integer (16 bit, 32 bit and 64 bit) and BCD (up to 18 bits) arithmetic functions. Functions are 10-100 times faster, using the 8087 NDP, than the same functions executed in software (Table 4). Functions include: addition, subtraction, multiplication, division; TAN, ARCTAN, 2X — 1, SQRT, $Y \cdot \log_2(X+1)$ and $Y \cdot \log_2 X$. For evaluating functions such as: COS, SIN, $COS^{-1}$, log10 etc. the following constants are provided: PI, log102, loge2, log2e and log210. Numbers are stored internally in 80 bit registers allowing for precision with 64 bit real numbers and integers. The 8087's unique coprocessor interface to the CPU can yeild an additional performance increment beyond that of simple instruction speed. No overhead is incurred in setting up the device for a computation; the 8087 decodes its own instructions automatically in parallel with the CPU. Moreover, built-in coordination facilities allow the CPU to proceed with other instructions while the 8087 is simultaneously executing its numeric instructions. Programs can exploit this processor parallelism to increase total system throughput.

**ROM-86** ROM-86 is a piggyback EPROM expansion module that can be added to the MBC-86/12. ROM-86 expands onboard EPROM to 128K bytes and adds 256 bytes of NOVRAM.

| Instruction | Approximate Execution Time (μs) (5 MHz Clock) | |
|---|---|---|
| | 8087 | 8086 Emulation |
| Multiply (single precision) | 19 | 1,600 |
| Multiply (double precision) | 27 | 2,100 |
| Add | 17 | 1,600 |
| Divide (single precision) | 39 | 3,200 |
| Compare | 9 | 1,300 |
| Load (single precision) | 9 | 1,700 |
| Store (single precision) | 18 | 1,200 |
| Square root | 36 | 19,600 |
| Tangent | 90 | 13,000 |
| Exponentiation | 100 | 17,100 |

**Table 4. 8087 — 8086 Emulation Speed Comparison**

# SPECIFICATIONS

**WORD SIZE:**

INSTRUCTIONS: 8, 16, 24, or 32 bits
DATA: 8-bit (byte) or 16-bit (word)
CYCLE TIME:

| CLOCK | CYCLE TIME | |
|---|---|---|
| | INSTRUCTION IN QUEUE | INSTRUCTION NOT IN QUEUE |
| 5MHz | 400ns | 1.2μs |
| 8MHz | 250ns | 750ns |

**MEMORY CAPACITY:**

ON-BOARD ROM/EPROM: Up to 32K bytes — user installed in 4K, 8K, or 16K increments (expandable to 128K bytes).

ON-BOARD RAM: 32K, 128K bytes of dual port dynamic RAM (expandable to 256K bytes). (specify amount of RAM required when ordering — see ORDERING INSTRUCTIONS)

OFF-BOARD EXPANSION: Up to 1 Megabyte of user-specified combination of RAM, ROM, or EPROM

**MEMORY ADDRESSING:**

ON-BOARD ROM/EPROM:
FE000-FFFFF$_H$ (using 4732 ROMs or 2532 EPROMs)
FC000-FFFFF$_H$ (using 4764 ROMs or 2564 EPROMs)
F8000-FFFFF$_H$ (using 47128 ROMs or 25128 EPROMs)

ON-BOARD RAM:
CPU ACCESS:
00000-07FFF$_H$ (32K bytes)
00000-1FFFF$_H$ (128K bytes)

MULTIBUS ACCESS: Jumper-selectable on any 8K boundary within any 128K segment of the 1 Megabyte system address space
Accesses are selectable for 8K, 16K, 24K, 32K, or 64K bytes (or 16K increments for 128K option)
Jumpers and switches allow the board to act as a slave RAM for access by another bus master

**I/O CAPACITY:**

PARALLEL: 8255A Programmable Peripheral Interface — 24 lines with three software selectable operating modes

SERIAL: 8251A Programmable Communications Interface — EIA standard RS-232C
SYNCHRONOUS: 5-8 bit characters; internal or external character synchronization; automatic sync insertion

ASYNCHRONOUS: 5-8 bit characters; break character generation; 1, 1.5, or 2 stop bits; false start bit detection

BAUD RATES:

| FREQUENCY (KHz) (software selectable) | BAUD RATE (Hz) | | |
|---|---|---|---|
| | Synchronous | Asynchronous | |
| | | ÷16 | ÷64 |
| 153.6 | — | 9600 | 2400 |
| 76.8 | — | 4800 | 1200 |
| 38.4 | 38400 | 2400 | 600 |
| 19.2 | 19200 | 1200 | 300 |
| 9.6 | 9600 | 600 | 150 |
| 4.2 | 4800 | 300 | 75 |
| 2.4 | 2400 | 150 | — |
| 1.76 | 1760 | 110 | — |

**INTERRUPT CAPABILITIES:**

INTERRUPT LEVELS: 1 Non-Maskable Interrupt (NMI)
8 vectored interrupt levels (expandable to 64 levels by cascading interrupt controllers)

INTERRUPT PRIORITIES: 4 software selectable priority modes — Fully nested
— Auto-rotating
— Specific priority
— Polled

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**COUNTER/TIMERS:** 8253A Programmable Interval Timer

COUNTER/TIMERS: 1 16-bit timer for baud rate generation
2 16-bit timer/counters are available to the system designer

OPERATING MODES: 7 software selectable counter/timer functions — Interrupt on terminal count
— Programmable one-shot
— Rate generator
— Square wave rate generator
— Software triggered strobe
— Hardware triggered strobe
— Event counter

OUTPUT FREQUENCIES/ TIMING INTERVALS:

| FUNCTION | SINGLE TIMER/COUNTER | | DUAL TIMER/COUNTERS (Two timers cascaded) | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| Real Time Interrupt | 0.8138 μs | 853.3 ms | 1.628 μs | 15.534 hr |
| Programmable One-Shot | 0.8138 μs | 853.3 ms | 1.628 μs | 15.534 hr |
| Rate Generator | 1.1719 Hz | 1.2288 MHz | 0.0000179 Hz | 614.4 kHz |
| Square Wave Rate generator | 1.1719 Hz | 1.2288 MHz | 0.0000179 Hz | 614.4 kHz |
| Software Triggered Strobe | 0.8138 μs | 853.3 ms | 1.628 μs | 15.534 hr |
| Hardware Triggered Strobe | 0.8138 μs | 853.3 ms | 1.628 μs | 15.534 hr |
| Event Counter | — | 2.46 MHz | — | — |

**INTERFACES:**

MULTIBUS: All signals TTL compatible
PARALLEL I/O: All signals TTL compatible
SERIAL I/O: RS-232C compatible
INTERRUPT REQUESTS: All signals TTL compatible
TIMERS: All signals TTL compatible

**CONNECTORS:**

MULTIBUS: 86 pin edge connector, 0.156" centers
PARALLEL I/O: 50 pin edge connector, 0.1" centers
SERIAL I/O: 26 pin edge connector, 0.1" centers

**PHYSICAL CHARACTERISTICS:**

WIDTH: 12.00 in. (30.48 cm)
HEIGHT: 6.75 in. (17.15 cm)
DEPTH: 0.62 in. ( 1.57 cm)
WEIGHT: 19 oz. ( 539 gm)

**POWER REQUIREMENTS:**

+12V @ 25mA
−12V @ 90mA
+5V @ 5A
−5V @ 2mA (32K version only)

**ENVIRONMENTAL CHARACTERISTICS:**

OPERATING TEMPERATURE: 0°-55°C (32°-131°F)
RELATIVE HUMIDITY: Up to 95% (non-condensing)

**ORDERING INSTRUCTIONS:**

MBC-86/12A-XXX/X — Enhanced 16-bit CPU board
CPU speed: 5, 8MHz
On-board RAM: 32, 128K bytes

Example: MBC-86/12A-128/8 = 8MHz CPU with 128KB RAM

SUPPORT ICs and Modules

C8087-3: Numerical coprocessor chip (5MHz)
ROM-86: 128KB EPROM expansion module with 256 bytes NOVRAM
MSBX-423: iSBX board with two RS-232/423 interfaces
MSBX-422: iSBX board with RS-449/422 interface
MSBX-800: iSBX board for high resolution color graphics

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

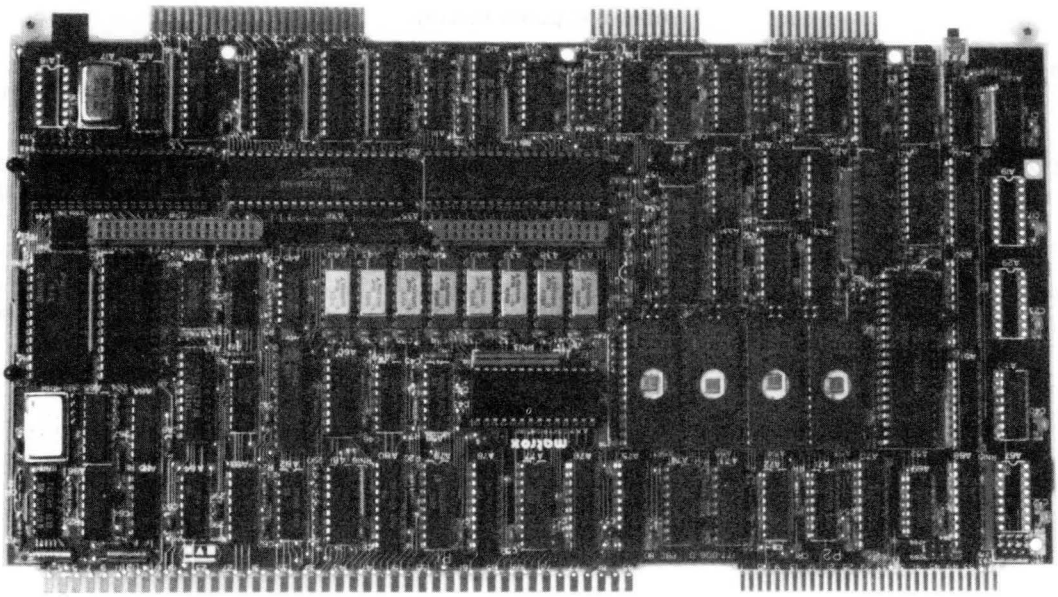
# PBC-80

## HIGH PERFORMANCE 8-BIT MULTIBUS CPU CARD

- **Z-80A Central Processing Unit (4MHz)**
- **On-board 64K byte dual-port RAM**
- **4 sockets for up to 128K bytes of ROM/EPROM**
- **On-board Memory Management Unit**
- **24 programmable I/O lines**
- **2 RS-232/423 serial ports**
- **5 programmable counter/timers**
- **256 bytes NOVRAM**
- **2 iSBX connectors**
- **Multibus compatible**
- **Multi-master bus arbitration**
- **1 Megabyte extended local addressing**
- **16 Megabyte Multibus addressing**

The PBC-80 is a member of the Matrox line of modular Multibus compatible single board computers. Using a 4MHz Z-80A CPU, the PBC-80 is a powerful 8-bit microcomputer with an advanced chip set for maximum flexibility in system configurations. On-board memory includes 64K bytes of dual-ported dynamic RAM, 256 bytes of non-volatile RAM (NOVRAM), as well as provisions for up to 128K bytes of user-installed ROM/EPROM or up to 8K bytes of static RAM.

Programmable I/O interfaces provide the flexibility required to adapt the PBC-80 to virtually any combination of I/O peripherals. The PBC-80 also features master-slave capabilities for applications requiring multiprocessors and for high speed peripheral control. Extended local addressing (1M byte) and full Multibus address decoding (16M bytes) provide full compatibility with all existing 8 and 16-bit Multibus CPUs and DMA controllers.



# PBC-80 FEATURES

**Powerful Central Processing Unit**

4MHz Z-80A CPU results in rapid instruction execution with consequent high data throughput. In addition, duplicate sets of both general-purpose and flag registers are provided to ease the design and operation of system software through single-context switching, background-foreground programming, and single level interrupt processing.

**Extensive Instruction Set**

The Z-80A instruction set contains 158 instructions including a subset emulation of the 8080A and 8085 instructions. Z-80A instructions include string, bit, byte, and word operations. Block search and block transfers together with indexed and relative addressing result in powerful data handling capabilities.

**Shared and Local Memory**

The PBC-80 contains 64K bytes of on-board dynamic RAM which is dual-ported to allow access from either the on-board Z-80A CPU or any other Multibus system master (Multibus can access on-board RAM through a 16K, 32K, or 64K address window). Furthermore, the Z-80A can establish a restricted local memory by protecting any or all of the on-board RAM in 2K, 4K, or 8K blocks (depending on the size of the Multibus address window).

**On-Board ROM/EPROM**

The PBC-80 supports four sockets for user-installed ROM/EPROM. These sockets can be populated with 2K, 4K, 8K, or 32K byte (when they become available) parts, for a total of 128K bytes of read-only memory. These sockets can optionally be populated with byte-wide static RAM (up to 8K bytes).

**Non-Volatile RAM**

The PBC-80 supports 256 bytes of non-volatile read/write memory (NOVRAM).

**Programmable Wait State Generator**

Provisions have been made on-board the PBC-80 to accomodate memory devices of differents makes, models, and speeds. 0 to 2 wait states can be programmed for each device.

**Memory Management Unit**

An on-board Memory Management Unit is used to map all of the on-board resources (RAM, ROM, NOVRAM, etc.). and the Multibus window, into the Z-80 memory map. The MMU also positions the 64K byte local addressing space within a 1M byte Multibus address space.

**Programmable Interrupt Structure**

On-board Am9519 Interrupt Controllers support 16 software maskable interrupt levels with a fixed or rotating priority schedule. Also, a separate, non-maskable interrupt line is available on-board to signal a catastrophic event (such as an impending power failure).

**Programmable Timer Functions**

Five independent 16-bit counter/timers can be programmed to operate in one of 17 count modes. This feature eliminates the need to maintain timing loops in software thereby minimizing the system's overhead.

**Dual RS-232/423 Serial Interfaces**

Two separate serial communications channels are supported on-board the PBC-80. These RS-232/423 compatible ports are capable of high speed digital data communications over distances of up to 4000 feet. The on-board serial channels can also interface to RS-232C compatible peripherals.

**Programmable Parallel Interface**

A programmable peripheral interface lends flexibility to the PBC-80's interfacing capabilities. This feature allows the PBC-80 to be "tailored" to suit most I/O requirements.

**iSBX-Bus Expansion**

Two iSBX-Multimodule connectors are included on-board to enhance the performance of the PBC-80.

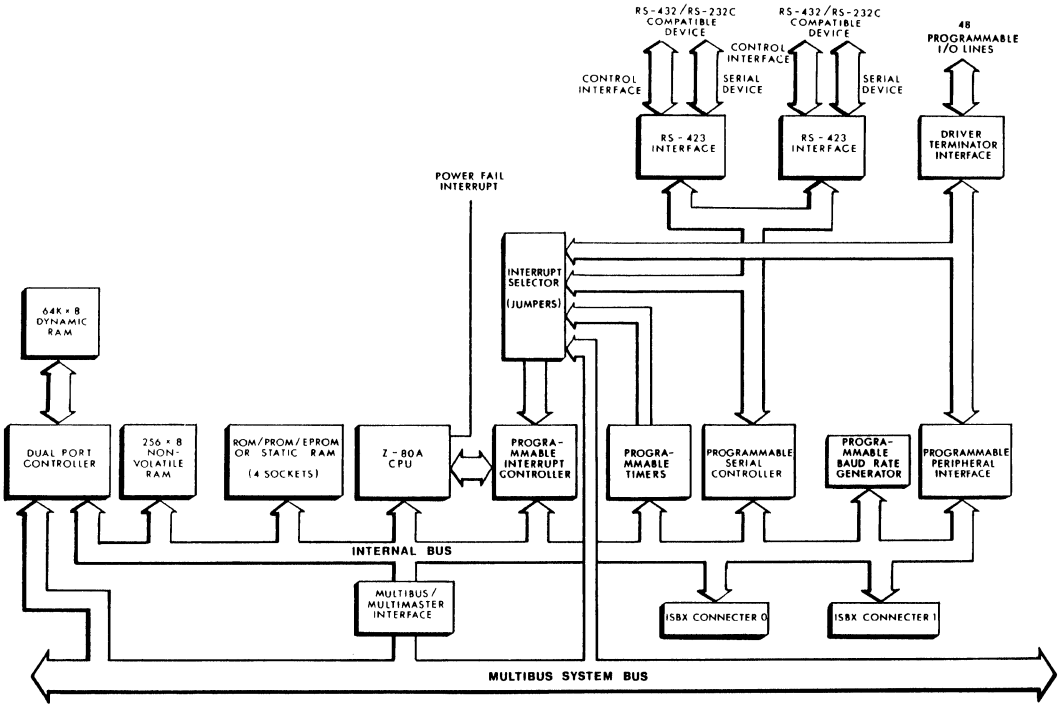



Figure 1. PBC-80 block diagram

## FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the PBC-80 single board computer. It has been designed, using a fast Z-80A CPU and state-of-the-art LSI peripheral chips, to provide high throughput in a real-time processing environment.

## CENTRAL PROCESSING UNIT (CPU)

**Architecture** — At the heart of the design of the PBC-80 is the 4 MHz Z-80A CPU, a powerful 8-bit processor on a single LSI chip, with a minimum instruction execution time of 1.00 $\mu$s. The Z-80A is essentially software compatible with the Intel 8080A or 8085A CPUs and can run programs written for these processors with little or no change required. In addition to the accumulator and flag register, the Z-80A contains six internal general purpose registers which can be addressed individually or in pairs. Used in pairs, these general purpose registers are ideal for 16-bit addressing or double precision arithmetic operations. The Z-80A also contains a duplicate set of these registers (accumulator, flag register, and general purpose registers) which can be activated by one of two unique instructions. This register duplication is useful to store the CPU's "environment" (contents of the register file) after receiving an interrupt. This technique eliminates the requirement for software routines that commit the "environmental" data to external memory during interrupts. The Z-80A contains a pair of 16-bit registers (IX and IY) which allow indexed memory addressing by summing the contents of either of these registers with a 16-bit "displacement field" contained within the executing instruction. The Z-80A also contains a 16-bit program counter. A memory stack, located within any portion of the PBC-80 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and any or all of the six general purpose registers. A 16-bit stack pointer controls the addressing of the stack. Completing the internal Z-80A register file are an 8-bit interrupt register and a 7-bit refresh

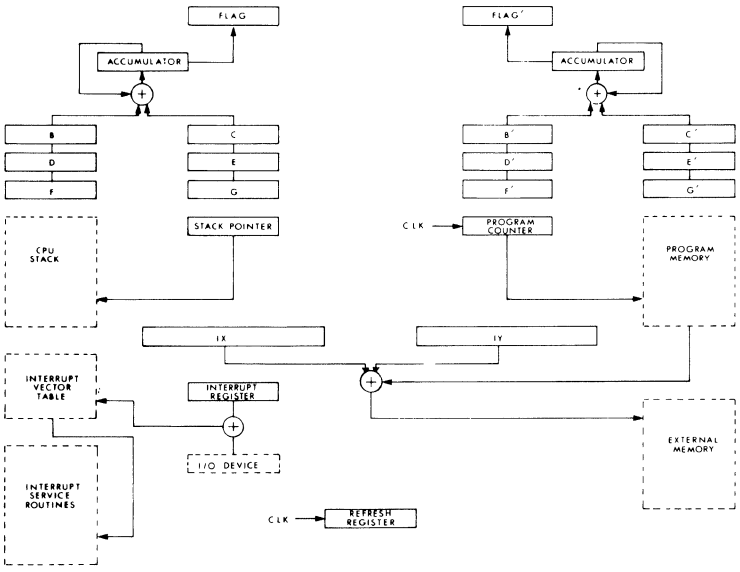



Figure 2. Z-80A internal registers

register. The interrupt register is loaded with an 8-bit pointer which when combined with an 8-bit offset (supplied by an interrupting device) will access a location in an external interrupt vector table. The refresh register assures the validity of system RAM by automatically providing refresh addressing for dynamic RAMs.

**Instruction Set** — The Z-80A instruction set is essentially a superset of the Intel 8080A or 8085A intruction set. The Z-80A instruction set, however, represents a significant increase in executable instructions over the 8080A and 8085A. Operations unique to the Z-80A include: indexed addressing capabilities on most instructions, rotate and shift operations on any of the general purpose registers or memory locations, digit rotation, non-destructive bit testing, and interrupt mode control. Instructions can be 8, 16, 24 or 32 bits long and are aligned on byte boundaries.

## RAM CAPABILITIES

The PBC-80 is supplied with 64K bytes of on-board dynamic read/write memory. All read and write operations to this on-board memory are performed at maximum processor speed. The on-board RAM memory is dual-ported and can be accessed by any other Multibus master. Hardware straps allow the Multibus to access on-board RAM through a 16K, 32K, or 64K byte window that can be located on any boundary of the same size within the 16M byte address space. Furthermore, the PBC-80 can inhibit bus accesses to RAM in 2K, 4K, or 8K blocks depending on whether a 16K, 32K, or 64K byte window (respectively) is selected. This feature allows multiprocessor systems to establish local memory for each processor and shared memory where the total system memory size can exceed 16M bytes without addressing conflicts.

## ROM/EPROM CAPABILITIES

Four sockets are available on-board the PBC-80 to accomodate up to 128K bytes of non-volatile read-only memory. Additionally these sockets may be populated with compatible byte wide static RAM for up to 8K bytes. The PBC-80 also contains 256 bytes of non-volatile random access memory (NOVRAM).

## MEMORY MANAGEMENT

The PBC-80 Memory Management Unit contains 32 software selectable memory address maps (stored in PROM) which map the 64K bytes of CPU address space into the first 1M byte of system address space. Each of the PROM memory address maps divides the CPU address space into 16 blocks of 4K bytes per block, and assigns each block a base address on any 4K byte boundary in system address. The Memory Management Unit also contains a corresponding device map for each of the 32 memory address maps. The device map further divides the 4K address blocks, defined in the address mapping, into 2K byte device blocks. Within each of these device blocks, then, the device map enables CPU access to one of seven available memory devices (figure 3). This feature allows efficient allocation of available memory resources as well as conserving system address space by placing all the memory devices at the same physical base address.

The PBC-80 Memory Management Unit is supplied with 32 independent memory address maps (and associated device maps). However, only the first eight maps are preprogrammed to allow the user to complete the remaining 24 maps according to his own specific environment. Upon initialization, Map 0 is selected which places EPROM 0 at location 00000H. This feature enables a Bootstrap-on-Reset capability.

## WAIT STATE GENERATOR

Provisions have been made on the PBC-80 to accomodate memory devices of different makes, types, and speeds. A variable number of wait states can be programmed for each of the four types of memory devices (dynamic RAM, ROM, static RAM, and NOVRAM) and for the two different command durations (instruction fetch cycle and normal memory request cycle).

The wait state structure is established by choosing one of four hardware-selectable PROM look-up tables. Each table contains separate wait state sequences for each of the different on-board memory devices. For custom wait state requirements, the user need only program another PROM look-up table.

## PROGRAMMABLE INTERRUPT CONTROLLER

The PBC-80 recognizes 17 independent interrupt sources. A non-maskable interrupt (NMI) is tied directly to the Z-80A CPU and is assigned to the highest priority level, and will therefore supercede any other interrupt request. This non-maskable interrupt is usually used to signal a catastrophic



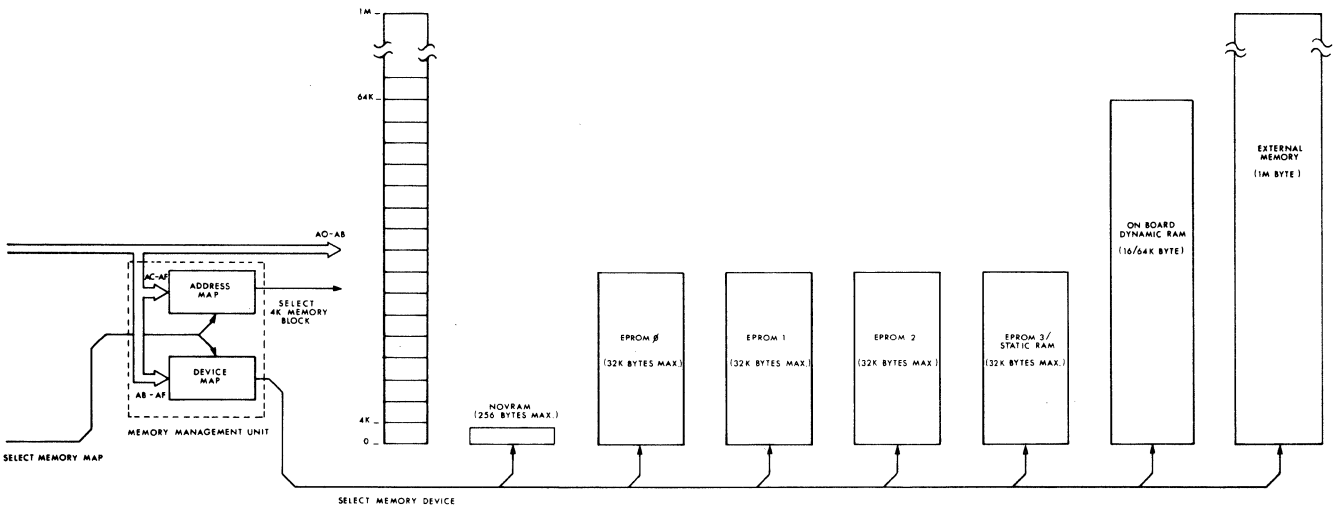



Figure 3. Memory Management Unit

| Port | Lines (qty) | Mode of Operation | | | | | |
|---|---|---|---|---|---|---|---|
| | | Unidirectional | | | | Bidirectional | Control |
| | | Input | | Output | | | |
| | | Latched | Latched & Strobed | Latched | Latched & Strobed | | |
| A | 8 | X | X | X | X | X | |
| B | 8 | X | X | X | X | | |
| C | 4 | X | | X | | | X1 |
| | 4 | X | | X | | | X1 |

**Note:**
1. Part of Port C must be used as a control port when either Port A or Port B is used as a latched and strobed input or a latched and strobed output port or if Port A is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

event, such as an impending power failure. The remaining 16 interrupt inputs are managed by two on-board Am9519 Universal Interrupt Controllers. These devices initiate interrupts on a priority basis and assign priorities to each interrupt line in either fixed or rotating priority modes. Using a fixed priority scheme assigns the highest interrupt priority to interrupt line 0 and the lowest priority to interrupt line 15. In the auto-rotating mode, each interrupt line, after receiving service, becomes the lowest priority level. Upon acknowledgement of an interrupt, the Am9519 releases a data byte which, when combined with the contents of the CPU's Interrupt Register, provides a vector to the required service routine.

**Interrupt Sequence** — The PBC-80 can accept interrupt requests from the programmable parallel and serial interfaces, the programmable timers, the system bus, or directly from peripheral equipment. A special non-maskable interrupt (power fail interrupt) can also be acknowledged directly by the CPU. When the on-board Interrupt Controller receives an interrupt request, it will evaluate the request according to the programmed priority mode and send an INT signal to the CPU, if appropriate. The Z-80A CPU then processes the request in one of three software selectable modes. In Mode 0, the CPU looks to the Interrupt Controller for the next executable instruction (normally a Restart instruction) which can be up to two bytes long. Interrupt Mode 1 causes the CPU to jump to a service routine (starting at location 0038H) in response to an interrupt request from the Interrupt Controller. Mode 2, similiar to Mode 1, causes the CPU to jump to a service routine stored in system memory. In Mode 2, however, the CPU expects an 8-bit offset, from the Interrupt Controller, which combines with the preprogrammed contents of the CPU's I register to form a pointer to a memory look-up table (containing the starting address for the service routine). This Interrupt Mode enables the PBC-80 to maintain a unique service routine for each of the interrupt sources. Each interrupt request input can be individually masked, through software, by storing a single byte in the Interrupt Mask Register in the Interrupt Controller.

A non-maskable interrupt line is connected directly to the Z-80A CPU and causes a restart to a service routine at location 0066H. The non-maskable interrupt input can be connected to the TIME OUT ACK/line and/or the Power Fail Interrupt (PFI/) line. The TIME OUT line goes low if an instruction takes longer than 6 msec to complete while the PFI/line warns of an impending power failure.

## SYSTEM TIMER CONTROLLER

The PBC-80 supports an on-board Am9513 System Timer Controller to enable the PBC-80 to service many types of counting, sequencing and timing applications without the necessity of maintaining cumbersome timing loops in software. The System Timing Controller is made up of five 16-bit counters, each of which can be independently configured for count mode, input source, and output polarity. Each counter can also be programmed for up or down counting in either binary or BCD. This programmable versatility together with the provisions for both hardware and software gating of each counter, enable the implementation of a wide variety of complex counter/timer functions. Any of the counters may also be internally cascaded to form an effective counter length of up to 80 bits.

Counter 1 and 2 of the Am9513 contain additional internal logic to enable them to operate as a Time-of Day clock or as alarm comparators. As a Time-of-Day clock, the Am9513 can hold a maximum count of 23 hours, 59 minutes, and 59.9 seconds. Input frequency scalars are available to allow real-time clocking using 50Hz, 60Hz, or 100Hz frequency inputs. Extra registers (Alarm Registers) are also included with Counters 1 and 2 so that when the value in the counter reaches the value in the Alarm Register, the Comparator output will become active.

**Programming** — Each counter in the Am9513 can be individually programmed by loading a Counter Mode control word which defines the mode of operation for that counter, the input source, and the polarity of the output. Another 16-bit control word further defines additional parameters such as: enabling Comparator or Time-of-Day operations for Counters 1 and 2, and selecting the input source and divider for the Frequency Output (Am9513 provides a frequency divider output that is completely independent of the counters).

The Am9513 maintains a powerful command set to simplify user interaction with the counters. ARM and DISARM instructions permit software gating of the count process. Data can be written to or read from any of the counters using LOAD and SAVE commands respectively (internal registers associated with each counter enable LOAD and SAVE intructions to be executed without interfering with the counting process). Additional commands are provided to: step an individual counter by one count, set or clear an output toggle, issue a software reset, set or clear special bits in the Master Mode Register, or load the Data Pointer Register.

## PARALLEL I/O INTERFACE

The PBC-80 utilizes an 8255A Programmable Peripheral Interface (PPI) chip whose function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer board. Contained within the 8255A are three 8-bit ports (A, B and C) each of which may be assigned one of three basic modes of operation (Table 1). Port C can be divided into two 4-bit ports under the mode

control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs in conjunction with Port A and Port B. Operational modes for the 8255A's I/O ports may be combined so that their functional description can be "tailored" to almost any I/O structure. The 24 programmable I/O lines from this PPI chip and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven or round cables.

**Programming** — The functional description of the 8255A is programmed by the system software so that normally no external logic is required to interface peripheral devices or structures. During execution of the system program any of the operational modes may be selected using a single OUTput instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine. The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the definition of Ports A and B. Any of the eight bits of Port C can be set or reset using a single OUTput instruction. This feature reduces software requirements in control-based applications.

## SERIAL I/O INTERFACE

An on-board μPD7201 Multi-Protocol Serial Controller provides the PBC-80 with two independent serial communications channels. This programmable controller allows user-definition of most communications protocol parameters to permit operations using most popular asynchronous and synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC. Double buffered transmitter data and quadruply buffered receiver data ensures data entegrity.

Drivers and receivers on all serial communications lines are RS-423 compatible. This EIA unbalanced, bipolar voltage specification permits the high speed transmission of digital information over distances of up to 4000 feet. The PBC-80's serial ports are also designed to interface to RS-232C, thereby greatly enhancing its operation.

## SYSTEM BUS INTERFACE

The PBC-80 interfaces directly to the industry standard Multibus. All address, data, and control signals conform to the IEEE-796 (Multibus) Specifications. A failsafe timer is included in the PBC-80's design which can be used to generate an interrupt if an addressed device does not respond within 6 msec.

**Multimaster Capabilities** — The PBC-80 is ideally suited for systems requiring additional processing capacity and the benefits of multiprocessing (several CPUs and/or controllers logically sharing system tasks through communications over the system bus). On-board control logic allows up to five bus masters to share the system bus in serial (daisy chain) priority fashion or up to 16 masters to share the Multibus with the addition of an external priority network. Also, with an on-board Multibus clock, different speed controllers can share resources on the same bus without interference from other controllers.

## HARDWARE EXPANSION

**iSBX-Bus Expansion** — The PBC-80 contains two iSBX Multimodule* connectors which can accept any of the iSBX Multimodules. In this way, the PBC-80 can be easily upgraded to meet the specific requirements of most applications.

Matrox manufactures a dual RS-232/423 piggy-back board (MSBX-423), which can be added to the PBC-80 to provide up to six on-board serial I/O ports.

**MON-80** — Matrox supports the PBC-80 with the MON-80 monitor program. Upon boot-up or reset MON-80 will first establish the baud rate needed to communicate with the terminal connected to the serial port. Then the monitor will set up the Programmable Communications Interface with the baud rate which it has calculated. The MON-80 monitor also recognizes a set of commands which allow the user to perform certain functions, such as: compare two memory blocks, display the contents of a memory block, find a match in a memory block, input data, output data, move a memory block, etc. MON-80 also contains a CP/M bootstrap loader which works with the Matrox FFD-1 floppy disk controller.

| COMMAND | FUNCTION |
|---|---|
| A | Assigns reader, punch, console, or list device options from the console. |
| B | Boot CP/M. |
| C | Compare the contents of memory with the reader input and display the differences. |
| D | Display the contents of any defined memory area in Hex and ASCII. |
| E | End of File statement generator. |
| F | Fill any defined area of memory with a constant. |
| G | Go to an address and execute with five breakpoints. |
| H | Hex math, gives the sum and difference of two Hex numbers. |
| I | Input data from a defined I/O port. |
| J | Justify Memory — a non-destructive test for hard memory failures. |
| L | Load a binary file. |
| M | Move a defined memory area to another starting address. |
| N | Write Nulls to the punch device. |
| O | Output data to a defined I/O port. |
| P | Put ASCII characters into memory from the keyboard. |
| R | Read Intel Hex formats. |
| S | Substitute and/or examine any value at any address (in Hex). |
| U | Unload a binary tape to the punch device. |
| V | Verify the contents of a defined memory block against that of another block and display the differences. |
| W | Write a checksummed hex file to the punch device. |
| X and X' | Examine and/or modify any or all registers including the special Z-80A registers. |
| Y | Search memory for a defined byte string and display all the addresses where they are found. |

Table 2. MON-80 monitor instructions

# SPECIFICATIONS

**WORD SIZE:**

| | |
|---|---|
| INSTRUCTIONS: | 8, 16, 24 or 32 bits |
| DATA: | 8-bit (byte) |

**CYCLE TIME:**

| | |
|---|---|
| CLOCK: | 4MHz |
| CYCLE TIME: | 1000ns min. |

**MEMORY CAPACITY:**

| | |
|---|---|
| ON-BOARD ROM/EPROM: | Up to 128K bytes — user installed in 2K, 4K, 8K, 16K, or 32K increments. |
| ON-BOARD RAM: | 64K bytes of dynamic RAM<br>256 bytes of non-volatile RAM<br>Up to 8K bytes of static RAM (user installed) |
| OFF-BOARD EXPANSION: | Up to 1M bytes of user-specified combination of RAM, ROM, or EPROM |

**MEMORY ADDRESSING:**

| | |
|---|---|
| LOCAL ACCESS: | The Memory Management Unit allows the local CPU to access all on-board resources (ROM, RAM, NOVRAM, I/O, etc.) within a 1M byte address range. Local access to the Multibus is restricted to the lower 1M byte of the 16M byte address space. |
| MULTIBUS ACCESS: | On-board RAM can be accessed from the Multibus via a 16K, 32K, or 64K byte window, within any section of the 16M byte address space. The memory window is locatable on any 16K byte boundary when using either a 16K or a 64K byte window. 32K byte memory windows can be located on any 32K byte boundary. |

**I/O CAPACITY:**

| | |
|---|---|
| PARALLEL: | 8255A Programmable Peripheral Interface — 24 lines with three software selectable operating modes<br>— Basic input/output<br>— Strobed input/output<br>— Bidirectional bus |
| SERIAL: | uPD7201 Multi-Protocol Serial Controller — 2 RS-232/423 channels |
| ASYNCHRONOUS: | — 5-8 bit characters<br>— 1, 1.5, or 2 stop bits<br>— Odd/even parity<br>— Break detection and generation<br>— Transmission speed x1, x16, x32, or x64 clock frequency<br>— Interrupt on parity overrun or framing errors |
| SYNCHRONOUS:<br>Monosync, Bisync, and External Sync | — Software selectable sync characters (8/16 bits)<br>— Automatic sync insertion<br>— CRC generation and checking |
| HDLC and SDLC | — Abort sequence generation and detection<br>— Automatic zero insertion and detection<br>— CRC generation and checking<br>— I-field residue handling |
| BAUD RATES: | — 110 to 19.2K baud (software selectable)<br>— Will support up to 302K baud with external clock |

**I/O ADDRESSING:**

The PBC-80 supports the standard 8 bit addressing mode (256 locations), as well as a pseudo 16 bit addressing mode (64K locations). On-board resources occupy 64 I/O locations.

**INTERRUPT CAPABILITIES:**

| | |
|---|---|
| INTERRUPT LEVELS: | 1 Non-Maskable Interrupt (NMI)<br>16 vectored interrupt levels |

**COUNTER/TIMERS:** Am9513 System Timer Controller

| | |
|---|---|
| COUNTER/TIMERS: | 5 16-bit timer/counters |
| OPERATING MODES: | 17 software selectable counter/timer functions |

- Software-Triggered Strobe
- Software-Triggered Strobe with Level Gating
- Hardware-Triggered Strobe
- Rate Generator
- Rate Generator with Level Gating
- Non-Retriggerable One-Shot
- Software-Triggered Delayed Pulse One-Shot
- Software-Triggered Delayed Pulse One-Shot with Hardware Gating
- Hardware Triggered Delayed Pulse Strobe
- Variable Duty Cycle Rate Generator
- Variable Duty Cycle Rate Generator with Level Gating
- Hardware-Triggered Delayed Pulse One-Shot
- Software-Triggered Strobe with Level Gating and Hardware Retriggering
- Software-Triggered Strobe with Edge Gating and Hardware Retriggering
- Retriggerable One-Shot
- Frequency-Shift Keying

**INTERFACES**

| | |
|---|---|
| MULTIBUS: | All signals TTL compatible |
| PARALLEL I/O: | All signals TTL compatible |
| SERIAL I/O: | RS-232/423 compatible |
| INTERRUPT REQUESTS: | All signals TTL compatible |
| TIMERS: | All signals TTL compatible |

**CONNECTORS:**

| | |
|---|---|
| MULTIBUS: | 86 pin edge connector, 0.156" centers |
| AUXILLARY: | 60 pin edge connector, 0.156" centers |
| PARALLEL I/O: | 50 pin edge connector, 0.1" centers |
| SERIAL I/O: | 2 x 26 pin edge connector, 0.1" centers |
| iSBX: | 2 x 36 pin iSBX Multimodule connectors |

**PHYSICAL CHARACTERISTICS:**

| | |
|---|---|
| WIDTH: | 12.00 in. (30.48 cm) |
| HEIGHT: | 6.75 in. (17.15 cm) |
| DEPTH: | 0.50 in. (1.27 cm) |

**POWER REQUIREMENTS:**

+5V ±5% @ 3A
−12V ±5% @ 25mA

**ENVIRONMENTAL CHARACTERISTICS:**

| | |
|---|---|
| OPERATING TEMPERATURE: | 0° — 55°C (32° — 131°F) |
| RELATIVE HUMIDITY: | Up to 95% (non-condensing) |

**ORDERING INFORMATION:**

| | |
|---|---|
| PBC-80 | 8-bit CPU board with 64K bytes of dynamic RAM and 256 bytes of NOVRAM |
| SUPPORT ICs: | |
| MON-86 | EPROM monitor with CP/M bootstrap. |

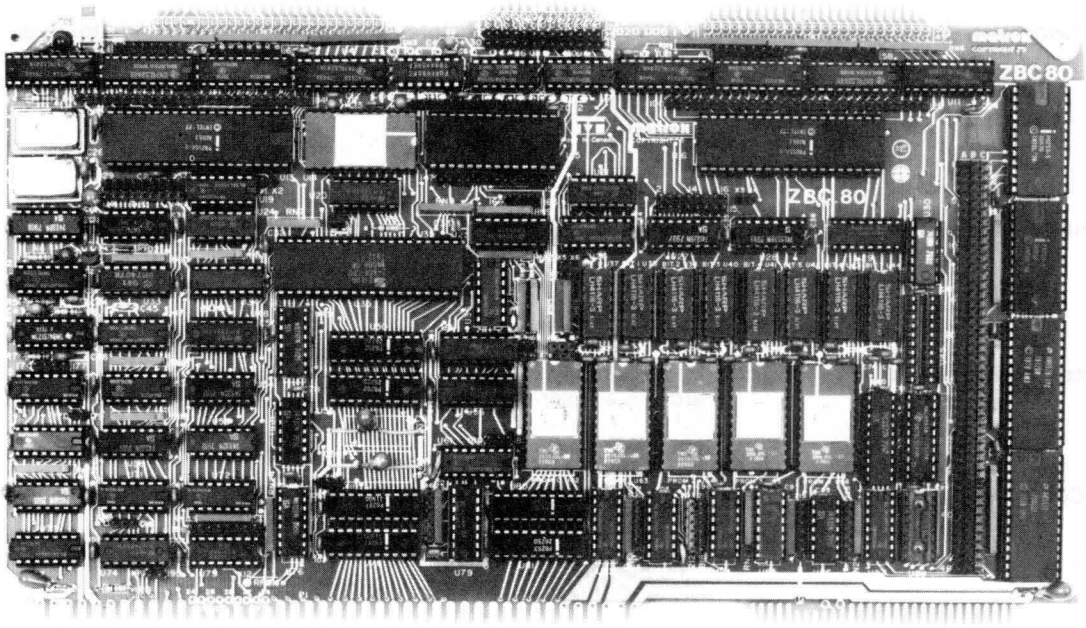
matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# ZBC-80

## HIGH PERFORMANCE 8-BIT MULTIBUS CPU CARD

- **Z-80A* CPU (4 MHz)**
- **Bootstrap-on-reset capability**
- **ZBC-80 runs CP/M 2.2* DOS**
- **5 sockets for up to 40K bytes of ROM/EPROM**
- **Programmable USART with RS-232C interface.**
- **48 programmable parallel I/O lines**
- **Large wire-wrap area and one spare socket**
- **Software enable/disable of on-board RAM/ROM**
- **Multibus* compatible**
- **Multimaster bus arbitration**
- **16K/64K bytes of on-board RAM**
- **Socket for Arithmetic/Floating Point Processor**
- **Up to 16 interrupt levels**

The Matrox ZBC-80 is a Z-80A* based single board computer that is compatible with the Multibus*. Software support in the form of CP/M*, the industry standard 8080/Z80 disk operating system, and a wide variety of high level language utilities such as FORTRAN, COBOL, PASCAL, and BASIC, are available from a number of sources. The card itself can contain a dedicated arithmetic processor, a 16-level programmable interrupt controller, bus arbitration logic for multiprocessor applications, 64K bytes of dynamic RAM and sockets for up to 40K bytes of ROM/EPROM. Also included are bootstrap-on-reset circuitry, six programmable parallel I/O ports, three programmable timers, and a serial communications controller. This advanced chip set maximizes processor speed and efficiency and at the same time provides the system designer with the greatest possible flexibility.



# ZBC-80 FEATURES

**Powerful Central Processing Unit**

4MHz Z-80A CPU results in rapid instruction execution with consequent high data throughput. In addition, duplicate sets of both general-purpose and flag registers are provided to ease the design and operation of system software through single-context switching, background-foreground programming, and single level interrupt processing.

**Extensive Instruction Set**

The Z-80A instruction set contains 158 instructions including a subset emulation of the 8080A and 8085 intructions. Z-80A instructions include string, bit, byte, and word operations. Block search and block transfers together with indexed and relative addressing result in powerful data handling capabilities.

**Bootstrap-On-Reset**

On-board Bootstrap circuitry allows software to roll the memory so that a PROM bootstrap or monitor program appears at location $0000_H$ on reset. This program can later be "rolled" out of the way to allow RAM to occupy the beginning of address space.

**Dynamic RAM Controller**

The ZBC-80 allows ROM and RAM to be positioned in overlapping address space. On-board memory automatically takes precedence over off-board memory in the same address space.

**Catastrophic Interrupt**

A non-maskable interrupt line is available to signal a catastrophic event (such as an impending power failure).

**Minimal Real Time Overhead on Interrupt**

A programmable interrupt controller generates an 8-bit pointer to a service routine on interrupt. 8 interrupt levels are supported with an additional 8 levels supported through an optional second interrupt controller.

**Hardware Generated Time Delays**

A 8253 Programmable Interval Timer can support up to three independent counter/timer functions. This feature eliminates the need to maintain timing loops in software thereby minimizing the system's software overhead. Up to two 8253 Interval Timers can be supported on-board the ZBC-80 (one 8253 is standard).

**Programmable Parallel Interface**

A programmable peripheral interface lends flexibility to the ZBC-80's interfacing capabilities. This feature allows the ZBC-80 to be "tailored" to suit most I/O requirements.

**Programmable Serial Interface**

Baud Rate, synchronous/asynchronous operation, number of bits/character, etc. are all user-selectable.

**Optional Coprocessor Expansion**

An optional Am9511 (Am9512) Arithmetic Coprocessor is available to further enhance the operation of the ZBC-80.

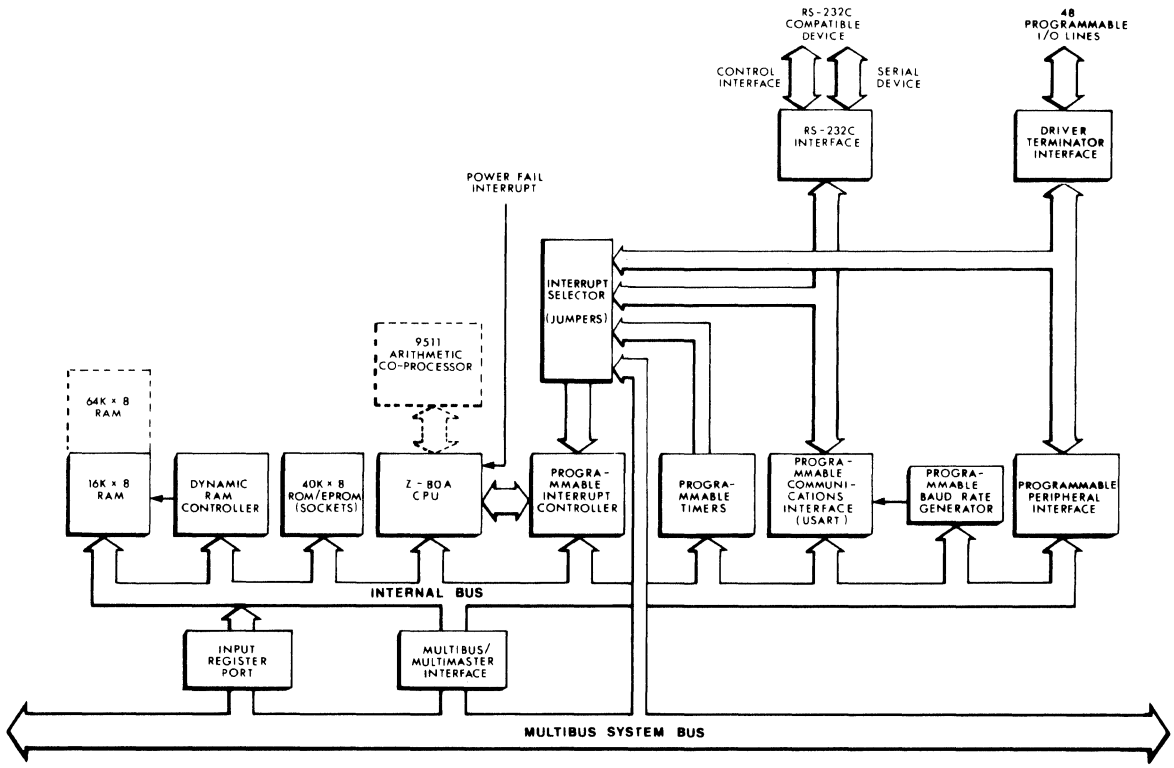



Figure 1. ZBC-80 block diagram

## FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the ZBC-80 single board computer. It has been designed, using a fast Z-80A CPU and state-of-the-art LSI peripheral chips, to provide high throughput in a real-time processing environment.

## CENTRAL PROCESSING UNIT (CPU)

**Architecture** — At the heart of the design of the ZBC-80 is the 4 MHz Z-80A CPU, a powerful 8-bit processor on a single LSI chip, with a minimum instruction execution time of 1.00 $\mu$s. The Z-80A is essentially software compatible with the Intel 8080A or 8085A CPUs and can run programs written for these processors with little or no change required. In addition to the accumulator and flag register, the Z-80A contains six internal general purpose registers which can be addressed individually or in pairs. Used in pairs, these general purpose registers are ideal for 16-bit addressing or double precision arithmetic operations. The Z-80A also contains a duplicate set of these registers (accumulator, flag register, and general purpose registers) which can be activated by one of two unique instructions. This register duplication is useful to store the CPU's "environment" (contents of the register file) after receiving an interrupt. This technique eliminates the requirement for software routines that commit the "environmental" data to external memory during interrupts. The Z-80A contains a pair of 16-bit registers (IX and IY) which allow indexed memory addressing by summing the contents of either of these registers with a 16-bit "displacement field" contained within the executing instruction. The Z-80A also contains a 16-bit program counter. A memory stack, located within any portion of the ZBC-80 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and any or all of the six

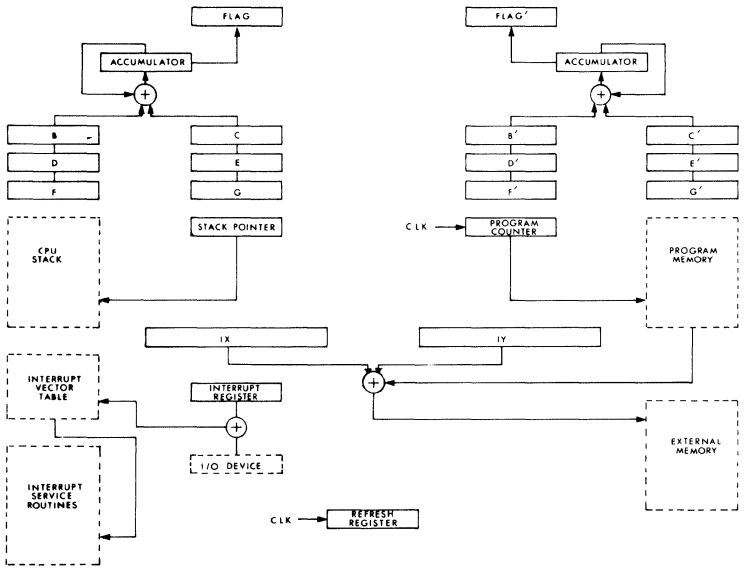



Figure 2. Z-80A internal registers

general purpose registers. A 16-bit stack pointer controls the addressing of the stack. Completing the internal Z-80A register file are an 8-bit interrupt register and a 7-bit refresh register. The interrupt register is loaded with an 8-bit pointer which when combined with an 8-bit offset (supplied by an interrupting device) will access a location in an external interrupt vector table. The refresh register assures the validity of system RAM by automatically providing refresh addressing for dynamic RAMs.

**Instruction Set** — The Z-80A instruction set is essentially a superset of the Intel 8080A or 8085A instruction set. The Z-80A instruction set, however, represents a significant increase in executable instructions over the 8080A and 8085A. Operations unique to the Z-80A include: indexed addressing capabilities on most instructions, rotate and shift operations on any of the general purpose registers or memory locations, digit rotation, non-destructive bit testing, and interrupt mode control. Instructions can be 8, 16, 24 or 32 bits long and are aligned on byte boundaries.

## MEMORY CAPACITY

**RAM** — The ZBC-80 is supplied with 16K bytes or 64K bytes of on-board dynamic read/write memory. All read and write operations to this on-board memory are performed at maximum processor speed. Straps are provided on-board to enable the user to position on-board RAM on any 16K byte boundary within the 64K byte system addressing range. Moreover, the CPU can disable access to the on-board RAM through software. For enhanced versions (64K RAM), memory can be disabled in 16K byte increments. This technique allows the user to make all (or part) of the on-board RAM "transparent" to the CPU. In this way the user can configure his system whereby the total system memory (including local on-board memory) exceeds 64K bytes without addressing conflicts. RAM refresh is assured by the CPU at the end of each instruction fetch.

**ROM/EPROM** — The ZBC-80 contains five sockets which can be populated with user installed 1K, 2K, 4K, or 8K byte ROM, PROM or EPROM chips, for a total of 40K bytes of non-volatile read only memory. Provisions have been made to accomodate ROMs of different makes, types, and speeds. The ZBC-80 also allows the user to configure the wait state structure to maximize throughput for any given ROM or PROM. The on-board wait state generator can be programmed (via hardware straps) to insert wait states during all ROM accesses, only during ROM accesses occuring during an instruction fetch cycle, or no wait states at all. On-board read only memory is strap-locatable anywhere within the available address space and can be software enabled/disabled.

**Dynamic RAM Controller** — The ZBC-80 allows the on-board RAM and ROM to overlap each other (in system memory space) when required. When an address where enabled ROM and RAM are both situated is accessed, an on-board Dynamic RAM Controller will allow the ROM to be read but will limit RAM access to writing. In order to read from the affected RAM the user must first disable the ROM in that address area. The Dynamic RAM Controller also generates multiplexed addressing and control strobes necessary to access RAM.

**Bootstrap Circuit** — The on-board Bootstrap Circuit, sometimes called a program loading circuit, allows the user, by using software, to shift the position of memory within address space. Upon reset, the Z-80A CPU always starts executing instructions at $0000_H$. Because of this any ROM bootstrap or monitor program must be located there, even though it might be desirable to have RAM in that address space. The ZBC-80 allows the user to have RAM at $0000_H$ and ROM at some higher address, because when the board is reset, a predetermined offset is added to the addresses, causing the CPU to see ROM at $0000_H$. After the ROM bootstrap program has been used to load a program into RAM, the Bootstrap Circuit can be disabled by software, and the CPU will see RAM at the start of memory.

## PROGRAMMABLE INTERRUPT CONTROLLER

The ZBC-80 recognizes 9 independent interrupt sources. A non-maskable interrupt (NMI) is tied directly to the Z-80A CPU and is assigned to the highest priority level, and will therefore supercede any other interrupt request. This non-maskable interrupt is usually used to signal a catastrophic event, such as an impending power failure. The remaining 8 interrupt inputs are managed by an on-board Am9519 Universal Interrupt Controller. This device initiates interrupts on a priority basis and assigns priorities to each interrupt line in either fixed or rotating priority modes. Using a fixed priority scheme assigns the highest interrupt priority to interrupt line 0 and the lowest priority to interrupt line 7. In the auto-rotating mode, each interrupt line, after receiving service, becomes the lowest priority level. Upon acknowledgement of an interrupt, the Am9519 releases a data byte which, when combined with the contents of the CPU's Interrupt Register, provides a vector to the required service routine. The ZBC-80 supports an extra socket for an optional second interrupt controller which increases the board's interrupt capabilities to a maximum of 17 levels.

**Interrupt Sequence** — The ZBC-80 can accept interrupt requests from the programmable parallel and serial interfaces, the programmable timers, the system bus, or directly from peripheral equipment. A special non-maskable interrupt (power fail interrupt) can also be acknowledged directly by the CPU. When the on-board Interrupt Controller receives an interrupt request, it will evaluate the request according to the programmed priority mode and send an INT signal to the CPU, if appropriate. The Z-80A CPU then processes the request in one of three software selectable modes. In Mode 0, the CPU looks to the Interrupt Controller for the next executable instruction (normally a Restart instruction) which can be up to two bytes long. Interrupt Mode 1 causes the CPU to jump to a service routine (starting at location $0038_H$) in response to an interrupt request from the Interrupt Controller. Mode 2, similiar to Mode 1, causes the CPU to jump to a service routine stored in System memory. In Mode 2, however, the CPU expects an 8-bit offset, from the Interrupt Controller, which combines with the preprogrammed contents of the CPU's I register to form a pointer to a memory look-up table (containing the starting address for the service routine). This Interrupt Mode enables the ZBC-80 to maintain a unique service routine for each of the interrupt sources. Each interrupt request input can be individually masked, through software, by storing a single byte in the Interrupt Mask Register in the Interrupt Controller.

A non-maskable interrupt line is connected directly to the Z-80A CPU and causes a restart to a service routine at location $0066_H$. The non-maskable interrupt input can be connected to the TIME OUT ACK/ line and/or the Power Fail Interrupt (PFI/) line. The TIME OUT line goes low if an instruction takes longer than 50$\mu$s to complete while the PFI/line warns of an impending power failure.

## PROGRAMMABLE INTERVAL TIMER

The ZBC-80 provides for accurate generation of time delays through an on-board 8253 Programmable Interval Timer. The 8253 is made up of three independent 16-bit counters, each with a count rate of up to 2MHz. By using the 8253 to generate time delays, the necessity of establishing timing loops in system software is eliminated. Therefore the software overhead is minimal. Using the Programmable Interval Timer, in conjunction with the 8259A

| Function | Operation |
|---|---|
| Interrupt on terminal count | When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks. |
| Programmable one-shot | Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable. |
| Rate generator | Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period. |
| Square-wave rate generator | Output will remain high until one half the count has been completed, and then go low for the other half of the count. |
| Software triggered strobe | Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period. |
| Hardware triggered strobe | Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable. |
| Event counter | On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system. |

Table 1. Programmable Timer Functions

Interrupt Controller, to generate an interrupt to the CPU on terminal count allows the user to maintain multiple delays by assignment of priority levels. Also non-delay type timer/counter functions can be implemented with the 8253. These non-delay functions include: Programmable Rate Generator, Event Counter, Binary Rate Multiplier, Real-Time Clock, Digital One-Shot and Complex Motor Controller. The outputs from the 8253 may be independently routed, through hardware straps, to the Am9519 Interrupt Controller and to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, or may be routed as inputs to the 8255A. The gate/trigger inputs may be routed to I/O terminators or as outputs from the 8255A. Note that the third counter in the 8253 is used by the ZBC-80 to provide the programmable baud rate generator for the board's RS232C USART serial port. The ZBC-80 has provisions to accept a second 8253 chip to provide for a total of six independent timers.

**Programming** — Each counter in the 8253 is a 16-bit presettable down counter that can operate either in binary or binary-coded decimal (BCD). Each counter is initialized by loading an 8-bit control word into an internal register (control words specify the counter to be used, mode of operation, and whether the count is to be in binary or BCD), followed by the count value. Each counter is fully independent and can have separate modes of operation (Table 1), and count type (binary or BCD). Special features in the control words handle the loading of the count so that software overhead is minimized. Also special commands and logic are included so that the contents of each counter can be read "on the fly" without having to inhibit the clock input. The 8253 Programmable Interval Timer is seen by the CPU as an array of I/O ports in system memory and therefore can be programmed by the system software with simple I/O operations.

## PARALLEL I/O INTERFACE

The ZBC-80 utilizes two 8255A Programmable Peripheral Interface (PPI) chips whose function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer board. Contained within the 8255A are three 8-bit ports (A, B and C) each of which may be assigned one of three basic modes of operation (Table 2). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs in conjunction with Port A and Port B. Operational modes for the 8255A's I/O ports may be combined so that their functional description can be "tailored" to almost any I/O structure. The 48 programmable I/O lines from these PPI chips and signal ground lines are brought out to a pair of 50-pin edge connectors that mates with flat, woven or round cables.

**Programming** — The functional description of the 8255A is programmed by the system software so that normally no external logic is required to interface peripheral devices or structures. During execution of the system program any of the operational modes may be selected using a single OUTput instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine. The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the definition of Ports A and B. Any of the eight bits of Port C can be set or reset using a single OUTput instruction. This feature reduces software requirements in control-based applications.

## SERIAL I/O INTERFACE

An 8251A Programmable Communications Interface is incorporated into the ZBC-80. Used as a peripheral device by the CPU, the 8251A is programmed by system software to

| Port | Lines (qty) | Mode of Operation | | | | | |
|---|---|---|---|---|---|---|---|
| | | Unidirectional | | | | Bidirectional | Control |
| | | Input | | Output | | | |
| | | Latched | Latched & Strobed | Latched | Latched & Strobed | | |
| A | 8 | X | X | X | X | X | |
| B | 8 | X | X | X | X | | |
| C | 4 | X | | X | | | X1 |
| | 4 | X | | X | | | X1 |

**Note:**
1. Part of Port C must be used as a control port when either Port A or Port B is used as a latched and strobed input or a latched and strobed output port or if Port A is used as a bidirectional port.

Table 2. Input/Output ports modes of operation

operate using virtually any serial data transmission technique presently in use. The 8251A Universal Asynchronous/Synchronous Receiver/Transmitter (USART) accepts data characters from the CPU in parallel format and then converts them into a continuous data stream for transmission. Simultaneously it can receive data as a serial stream and convert it to a suitable parallel format to be read by the CPU. The mode of operation (synchronous or asynchronous), data format, control character format, parity and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capabilities. Parity, overrun and framing error detection are all incorporated on-chip. The RS-232C interface on the ZBC-80, in conjunction with the 8251A USART, provides a direct interface to RS-232C compatible peripherals (terminals, cassettes, asynchronous and synchronous modems, etc). The RS-232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS-232C round or flat cables.

### INPUT REGISTER PORT

The ZBC-80 has an Input Register Port (IRP) which can be written into from the Multibus system bus and can be read by the on-board CPU. The IRP permits ZBC-80 boards operating in multi-master mode to exchange data without using common intermediate memory. A ZBC-80 sending data write to the IRP of the receiving board, which then reads the IRP internationally to complete the transfer. Reads and writes are automatically interlaced, allowing both the sender and the receiver to use the Z-80's repetitive I/O instructions for IRP access. This capability facilitates fast transfer of strings of data and, unlike standard DMA, it allows block transfers to be interrupted. The maximum transfer rate occurs when the IRP is used with bus override, and is 150K bytes/sec in bursts of 256 bytes.

### SYSTEM BUS INTERFACE

The ZBC-80 interfaces directly to the industry standard Multibus. All address, data, and control signals conform to the Intel Multibus Specification No. 9800683. A failsafe timer is included in the ZBC-80's design which can be used to generate an interrupt if an addressed device does not respond within 50 usec.

**Multimaster Capabilities** — The ZBC-80 is ideally suited for systems requiring additional processing capacity and the benefits of multiprocessing (several CPUs and/or controllers logically sharing system tasks through communications over the system bus). On-board control logic allows up to five bus masters to share the system bus in serial (daisy chain) priority fashion or up to 16 masters to share the Multibus with the addition of an external priority network. Also, with an on-board Multibus clock, different speed controllers can share resources on the same bus without interference from other controllers.

### HARDWARE EXPANSION

**MONTRAX** — Matrox supports the ZBC-80 with the MONTRAX monitor program. Upon boot-up or reset MONTRAX will first establish the baud rate needed to communicate with the terminal connected to the serial port. Then the monitor will set up the Programmable Communications Interface with the baud rate which it has calculated. The MONTRAX monitor also recognizes a set of commands which allow the user to perform certain functions, such as: compare two memory blocks, display the contents of a memory block, find a match in a memory block, input data, output data, move a memory block, etc. MONTRAX also contains a CP/M bootstrap loader which works with the Matrox FFD-1 floppy disk controller.

**Arithmetic Processors** — The ZBC-80 supports a socket for an optional math processor chip (Am9511 or Am9512). The Am9511 Arithmetic Processor provides for high performance fixed and floating point trigonometric and mathematical operations. Operations performed by the Am9511 include: 16 and 32-bit fixed point mathematics (add, subtract, multiply, and divide), 32-bit floating point mathematics, and floating point trigonometric functions (SQRT, SIN, COS, TAN, LOG, etc.). The Am9511 also includes a number of data manipulation commands such as: convert floating point to fixed point, change sign, copy operand, etc.

Alternatively the ZBC-80 can accept the AM9512 Floating Point Processor. This device, which performs only mathematical operations, trades the speed and number of functions provided by the AM9511 for greater precision. The Am9512 is capable of performing 32-bit fixed point and 32 or 64-bit floating point arithmetic operations.

| COMMAND | FUNCTION |
|---|---|
| A | Assigns reader, punch, console, or list device options from the console. |
| B | Boot CP/M. |
| C | Compare the contents of memory with the reader input and display the differences. |
| D | Display the contents of any defined memory area in Hex and ASCII. |
| E | End of File statement generator. |
| F | Fill any defined area of memory with a constant. |
| G | Go to an address and execute with five breakpoints. |
| H | Hex math, gives the sum and difference of two Hex numbers. |
| I | Input data from a defined I/O port. |
| J | Justify Memory — a non-destructive test for hard memory failures. |
| L | Load a binary file. |
| M | Move a defined memory area to another starting address. |
| N | Write Nulls to the punch device. |
| O | Output data to a defined I/O port. |
| P | Put ASCII characters into memory from the keyboard. |
| R | Read Intel Hex formats. |
| S | Substitute and/or examine any value at any address (in Hex). |
| U | Unload a binary tape to the punch device. |
| V | Verify the contents of a defined memory block against that of another block and display the differences. |
| W | Write a checksummed hex file to the punch device. |
| X and X' | Examine and/or modify any or all registers including the special Z-80A registers. |
| Y | Search memory for a defined byte string and display all the addresses where they are found. |

Table 3. MONTRAX monitor instructions

# SPECIFICATIONS

**WORD SIZE:**

INSTRUCTIONS: 8, 16, 24, or 32 bits
DATA: 8-bit (byte)

**CYCLE TIME:**

CLOCK: 4MHz
CYCLE TIME: 1000ns min.

**MEMORY CAPACITY:**

ON-BOARD ROM/EPROM: Up to 40K bytes — user installed in 1K, 2K, 4K, or 8K increments.
ON-BOARD RAM: 16K, 64K, bytes of dynamic RAM (specify amount of RAM required when ordering — see ORDERING INSTRUCTIONS)
OFF-BOARD EXPANSION: Up to 64K bytes of user-specified combination of RAM, ROM, or EPROM.

**MEMORY ADDRESSING:** Memory addressing on the ZBC-80 is user selectable by on-board hardware straps. The addresses shown here reflect the as-shipped values.

ON-BOARD ROM/EPROM:

$C000\text{-}C7FF_H$

ON-BOARD RAM:

$0000\text{-}3FFF_H$ (16K bytes)
$0000\text{-}FFFF_H$ (64K bytes)

**I/O CAPACITY:**

PARALLEL: 2 x 8255A Programmable Peripheral Interface — 48 lines with three software selectable operating modes

SERIAL: 8251A Programmable Communications Interface — EIA standard RS-232C

SYNCHRONOUS: 5-8 bit characters; internal or external character synchronization; automatic sync insertion

ASYNCHRONOUS: 5-8 bit characters; break character generation; 1, 1.5, or 2 stop bits; false start bit detection

BAUD RATES:

| FREQUENCY (KHz) (software selectable) | BAUD RATE (Hz) | | |
|---|---|---|---|
| | Synchronous | Asynchronous) | |
| | | ÷16 | ÷64 |
| 153.6 | — | 9600 | 2400 |
| 76.8 | — | 4800 | 1200 |
| 38.4 | 38400 | 2400 | 600 |
| 19.2 | 19200 | 1200 | 300 |
| 9.6 | 9600 | 600 | 150 |
| 4.8 | 4800 | 300 | 75 |
| 2.4 | 2400 | 150 | — |
| 1.76 | 1760 | 110 | — |

**INTERRUPT CAPABILITIES:**

INTERRUPT LEVELS: 1 Non-Maskable Interrupt (NMI)
8 vectored interrupt levels (expandable to 16 levels by cascading interrupt controllers)

**COUNTER/TIMERS:** 8253A Programmable Interval Timer

COUNTER/TIMERS: 1 16-bit timer for baud rate generation
2 16-bit timer/counters are available to the system designer (expandable to 5 timer/counters with optional second 8253A)

OPERTING MODES: 7 software selectable counter/timer functions — Interrupt on terminal count
— Programmable one-shot
— Rate generator
— Square wave rate generator
— Software triggered strobe
— Hardware triggered strobe
— Event counter

OUTPUT FREQUENCIES:

| FUNCTION | SINGLE TIMER/COUNTER | | DUAL TIMER/COUNTER (Two Timers Cascaded) | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| Real-time interrupt | 1.63 μs | 427.1 ms | 3.26 μs | 466.50 min. |
| Programmable one-shot | 1.63 μs | 427.1 ms | 3.26 μs | 466.50 min. |
| Rate generator | 2.342 Hz | 613.5 KHz | 0.000036 Hz | 306.8 KHz |
| Square-wave rate generator | 2.342 Hz | 613.5 KHz | 0.000036 Hz | 306.8 KHz |
| Software triggered strobe | 1.63 μs | 427.1 ms | 3.26 μs | 466.50 min. |
| Hardware triggered strobe | 1.63 μs | 427.1 ms | 3.26 μs | 466.50 min. |
| Event counter | — | 2.46 MHz | — | — |

**INTERFACES:**

| | |
|---|---|
| MULTIBUS: | All signals TTL compatible |
| PARALLEL I/O: | All signals TTL compatible |
| SERIAL I/O: | RS-232C compatible |
| INTERRUPT REQUESTS: | All signals TTL compatible |
| TIMERS: | All signals TTL compatible |

**CONNECTORS:**

| | |
|---|---|
| MULTIBUS: | 86 pin edge connector, 0.156" centers |
| PARALLEL I/O: | 2 x 50 pin edge connector, 0.1" centers |
| SERIAL I/O: | 26 pin edge connector, 0.1" centers |

**PHYSICAL CHARACTERISTICS:**

| | |
|---|---|
| WIDTH: | 12.00 in. (30.48 cm) |
| HEIGHT: | 6.75 in. (17.15 cm) |
| DEPTH: | 0.50 in. ( 1.27 cm) |

**POWER REQUIREMENTS:**

+5V ±5% @ 2.5A
−5V ±5% @ 2mA (16K version only)
+12V ±5% @ 75mA
−12V ±5% @ 10mA

**ENVIRONMENTAL CHARACTERISTICS:**

| | |
|---|---|
| OPERATING TEMPERATURE: | 0°-55°C (32°-131°F) |
| RELATIVE HUMIDITY: | Up to 95% (non-condensing) |

**ORDERING INSTRUCTIONS:**

ZBC-80/XX — 8-bit single board computer
- 16 — 16K bytes of on-board RAM
- 64 — 64K bytes of on-board RAM

ZBC-80C/XX — 8-bit single board computer with 9511 numerical coprocessor, additional Programmable Interrupt Controller, and an additional timer
- 16 — 16K bytes of on-board RAM
- 64 — 64K bytes of on-board RAM

SUPPORT ICs:

| | |
|---|---|
| 9511/9512 | Numerical coprocessor chip |
| MONTRAX | EPROM monitor |
| AM9519A-1 | Programmable Interrupt Controller |
| 8253-5 | Programmable Timer |

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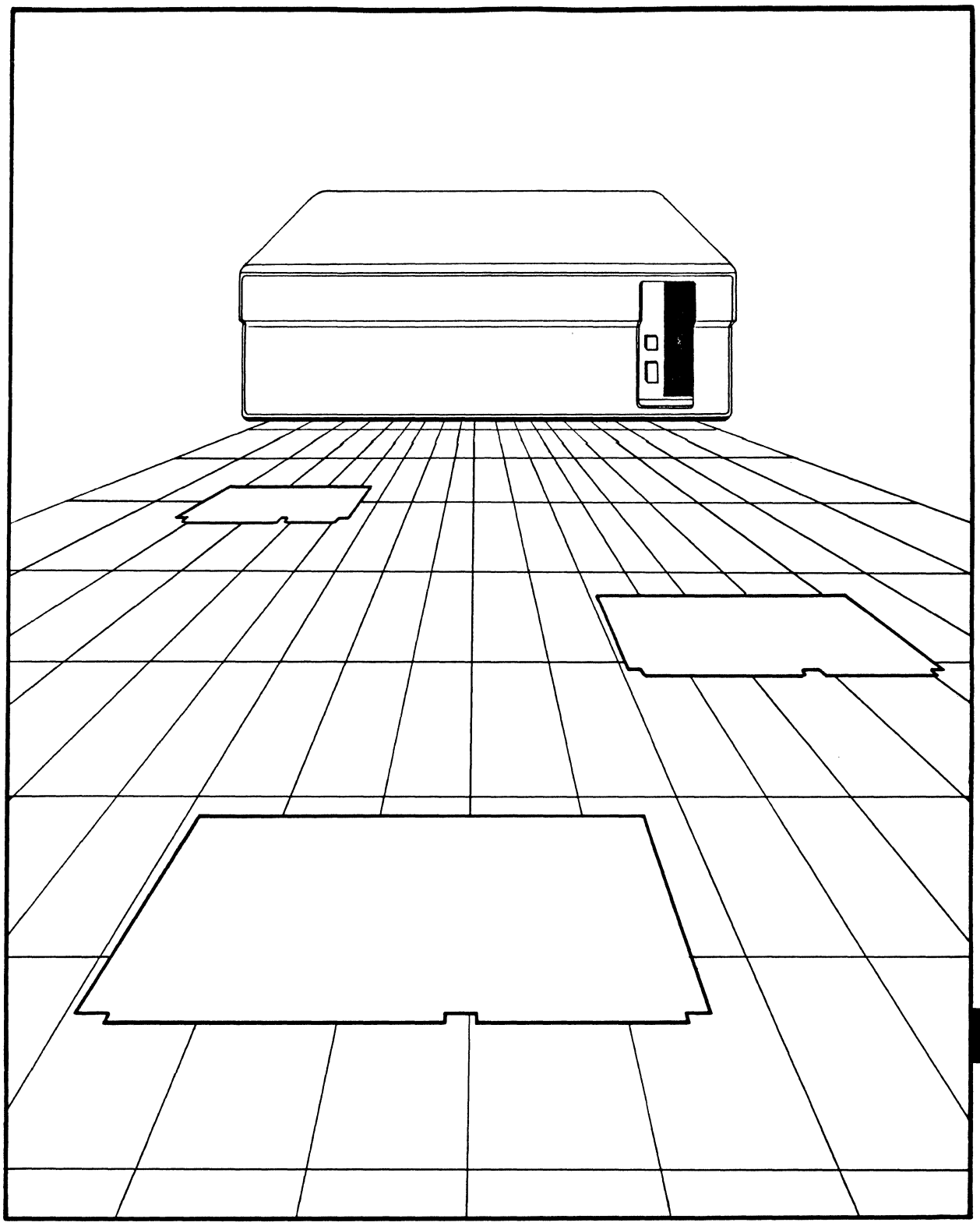


# MULTIBUS MEMORY, DISK CONTROLLER, COMMUNICATIONS AND ACCESSORY BOARDS

## SECTION 12 MULTIBUS MEMORY, DISK CONTROLLER, COMMUNICATIONS AND ACCESSORY BOARDS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MEGA-4

## 512K BYTE MULTIBUS MEMORY BOARD

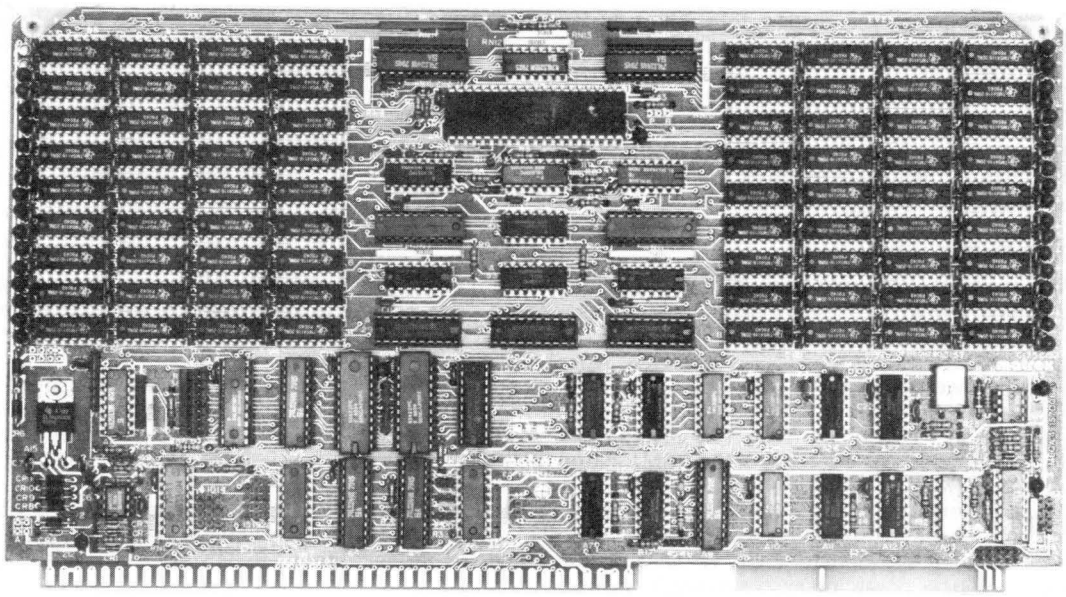
- **512K byte random access memory**
- **8-bit byte or 16-bit word transfers**
- **Multibus* compatible**
- **Full parity checking on each byte**
- **Memory management**
- **Parity error interrupt generator**
- **Transparent memory refresh**
- **24-bit address range**

The Matrox MEGA-4 is a Multibus* compatible memory board containing up to 512K bytes of read/write memory. It supports 8 or 16-bit data transfers making it compatible with both 8-bit and 16-bit CPUs. Memory refresh cycles are distributed and hence, transparent to the user.

Parity generating/checking circuitry provides for enhanced data transfer integrity in both byte and word mode. An interrupt signal is generated on parity error.

The on-board Memory Management Unit (MMU) enables mapping of the physical memory into the system memory address space. Each 8K byte memory block is assigned either read/write, read only, write only or read/write disable attributes. This mapping is changed at any time by rewriting the MMU register file.

In the event of power loss, the memory contents can be maintained by a single +12V battery supplying 1A of current through the back-up supply terminals.



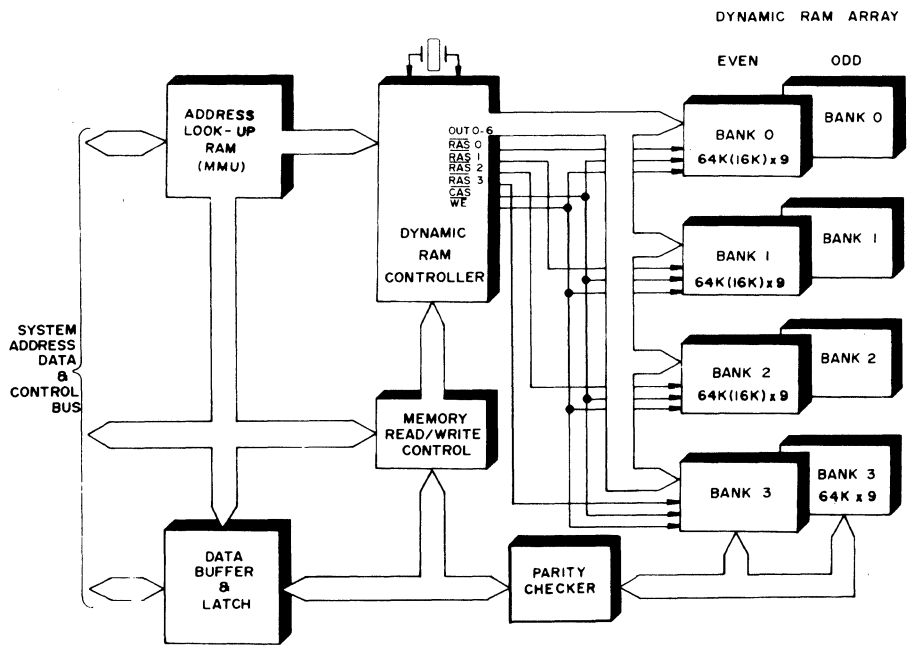



Figure 1. MEGA-4 Block Diagram

## FUNCTIONAL DESCRIPTION

### MEMORY

The MEGA-4 add-on memory board contains up to 512K bytes of read/write memory. High memory density and low power consumption/bit are assured through the use of 16k or 64k dynamic RAMs. Memory access time is 625ns max. while read/write cycle time is 725ns.

### MEMORY CONFIGURATIONS

| BYTE | WORD | NO. x RAM TYPE |
|---|---|---|
| 64K x 8 | 32K x 16 | 32 x 16K |
| 128K x 8 | 64K x 16 | 64 x 16K |
| 256K x 8 | 128K x 16 | 32 x 64K |
| 512K x 8 | 256K x 16 | 64 x 64K |

The MEGA-4's physical memory is divided, through on-board RAM look-up tables, into 8K byte blocks. Each is assigned to be read/write, read only, write only, or read/write disabled. The number of physical memory blocks on the MEGA-4 varies from 8 (64K x 8) to 64 (512K x 8).

### DYNAMIC RAM CONTROLLER

The heart of the MEGA-4 is the 8202 Dynamic RAM Controller. It performs all distributed memory refresh functions and resolves any conflicts between refresh cycle requests and read/write cycle requests. To the user the card appears as static RAM having a 625ns access time.

### MEMORY MANAGEMENT UNIT (MMU)

The Memory Management Unit maps each 8K byte block of on-board memory (physical block) into an 8K byte block of system address space (logical block). The MMU also enables the user to assign to each physical memory block read/write disable, read only, write only or read/write enable attributes.

The MMU consists of two fast bipolar RAM look-up tables containing 128 8-bit Memory Management Registers (MMR) each. The physical memory block number is specified by bits 0-5 of the MMR, while bits 6 and 7 specify the read/write attributes. Through I/O instructions, one of the two look-up tables is selected, making it possible for two complete mappings of the MEGA-4 memory to be made. The contents of the RAM look-up tables are rewritten at any time through programmed I/O transfers.

The Memory Management Unit makes the MEGA-4 ideal for multi-user systems. By initializing the RAM look-up table with a unique mapping, each user will have access to his own space in the MEGA-4's memory without disturbing space reserved for any other users. This feature is ideal for users with 8-bit CPUs which are normally limited to 64K bytes of memory, or for users of 16-bit CPUs with multi-user operating systems requiring virtual memory.

The MMU can map the MEGA-4 physical memory anywhere within the standard 1M byte Multibus* addressing range. MEGA-4 can also be strapped to any 1M byte boundary within the proposed IEEE 24-bit Multibus* addressing range.

The MMU can be disabled by on-board jumpers, allowing the MEGA-4 to operate as a conventional memory board.

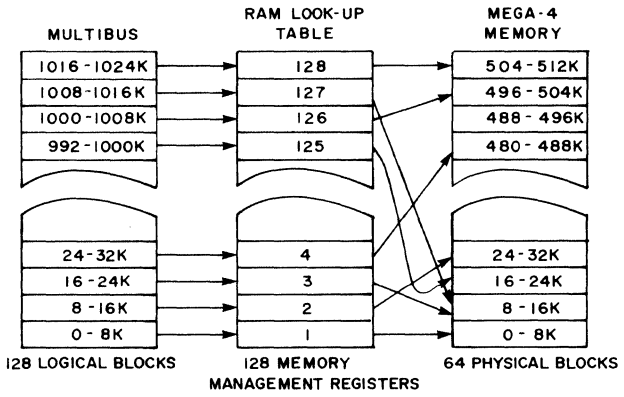



Figure 2. MMU Block Diagram

## PARITY GENERATOR/CHECKER

On-board parity generation and checking ensures validity of data transfers from the MEGA-4. Each byte is stored on the MEGA-4 as 9-bits (8 data bits and 1 parity bit). When writing to MEGA-4 memory, the parity generator inserts either a logic 1 or 0 to yield an odd number of logics 1s. During a read cycle, the parity checker will look for odd parity. If a parity error is encountered, the MEGA-4 generates an interrupt. The interrupt flag is reset when the CPU reads I/O port 0. When a word is addressed, parity error is the logical OR function of the byte parity error bits. The parity generator/checker is disabled by either on-board jumpers or by I/0 command.

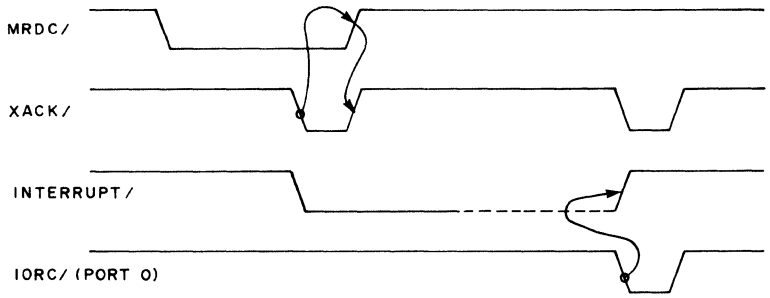
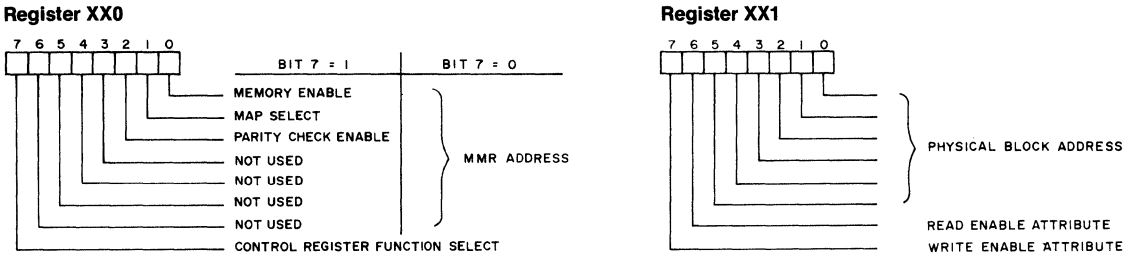



Figure 3. Parity Interrupt Timing Diagram

## PROGRAMMING INFORMATION

### SOFTWARE I/O

The MEGA-4 contains two control registers. When equal to zero, data bit 7 of register 0 selects the MMR Address Register (bit 0-6 specify the MMR number). If bit 7 is equal to one, the MEGA-4's Status Register (MEGA-4 enable/disable, look-up table selection, parity checking enable/disable) is selected. Reading register 0 resets the interrupt flags. The Memory Management Registers are loaded and their read/write attributes assigned via register 1.




### HARDWARE STRAPS

Jumpers on the MEGA-4 establish the address size (16 bit, 20 bit, or 24 bit), define the base address, and enable/disable the MMU and parity checker.

# SPECIFICATIONS

**WORD SIZE**

8/16-bits

**MEMORY SPEED**

| | ACCESS (ns max.) | CYCLE (ns max.) |
|---|---|---|
| READ | 625 | 725 |
| WRITE | — | 725 |

**MEMORY CONFIGURATIONS**

| BYTE | WORD | NO. x RAM TYPE |
|---|---|---|
| 64K x 8 | 32K x 16 | 32 x 16K |
| 128K x 8 | 64K x 16 | 64 x 16K |
| 256K x 8 | 128K x 16 | 32 x 64K |
| 512K x 8 | 256K x 16 | 64 x 64K |

**BUS INTERFACE**

Address, data and control signals conform to IEEE-796 bus specifications.

MMR and Status Registers: Positioned at any even address 0000-FFFD (0078H).

Read/Write Memory: Positioned at any 32K byte boundary (at any 8K byte boundary through MMU) 000000-FFFFFF (000800H).

Parity Error Interrupt: INTO/-INT7/ (uncommitted).

**CONNECTORS**

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 86 pin edge connector; 0.156" centers — Multibus interface | COMPAR ESM-43-DSRI |
| P2: 60 pin edge connector; 0.1" centers — Auxiliary connector | MOLEX 15-25-8601 |

**SIZE**

WIDTH: 12.00 in. (30.48 cm)
HEIGHT: 6.75 in. (17.15 cm)
DEPTH: 0.50 in. ( 1.27 cm)

**POWER REQUIREMENTS**

| SUPPLY | POWER CONSUMPTION | | |
|---|---|---|---|
| | NO BACK-UP CONNECTED | BACK-UP CONNECTED | BACK-UP ACTIVE |
| +5V ±10% | 1.5A | 1.0A | 0 |
| +12V ±10% | 100mA | 700mA | 0 |
| +12V back-up | 0 | 0 | 700mA |

**ENVIRONMENTAL REQUIREMENTS**

OPERATING TEMPERATURE: 0 — 55°C
RELATIVE HUMIDITY: 0 — 90% non-condensing

**ORDERING INFORMATION**

MEGA-4/XX

- 64 — MEGA-4 with 64KB memory
- 128 — MEGA-4 with 128KB memory
- 256 — MEGA-4 with 256KB memory
- 512 — MEGA-4 with 512KB memory

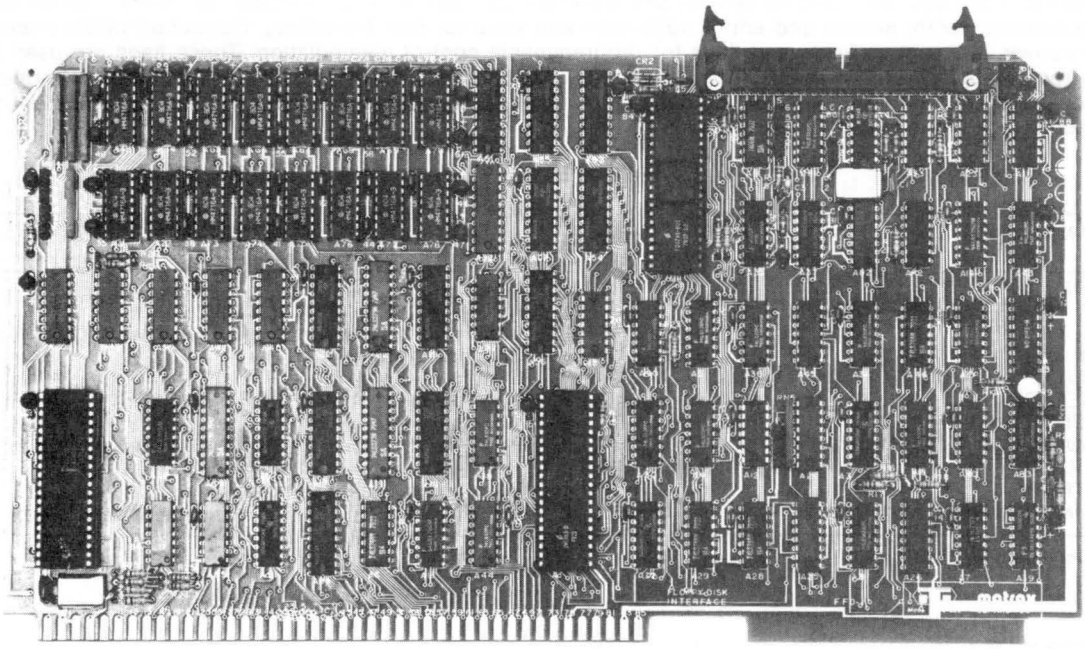
matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# FFD-1

## MULTIBUS FLOPPY DISK CONTROLLER BOARD

- **FD-1791 Floppy Disk Controller**
- **Controls up to four single/double sided drives**
- **IBM 3740 (FM) single-density**
- **IBM System 34 (MFM) double-density**
- **Commands include single/multiple sector R/W**
- **Runs under CP/M 2.2 DOS**
- **Multibus compatible**
- **Optional 32K bytes on-board two-port RAM**
- **DMA controller**
- **Works with most 5¼" or 8" disk drives**

The Matrox FFD-1 floppy disk controller/RAM card uses a state of the art ship set to provide for up to 5 megabytes of mass storage in Multibus-based systems using 5¼" or 8" floppy disk drives. The FFD-1 handles up to four single or double-sided drive units and is compatible with both the IBM 3740 (FM) single density and IBM System 34 (MFM) double density recording formats. In addition it may also be programmed for compatibility with sector lengths of 512 or 1024 bytes. The card may be ordered with 32K bytes of on-board dual-ported RAM that can be read from or written to by either the DMA controller or the bus master. The on-board DMA controller can transfer data between the disk controller and the on-board RAM or the disk controller and system memory. The FFD-1, when teamed up with any of the Matrox single board computers forms an extremely powerful floppy disk based computer system. CP/M 2.2 from Matrox is tailored to run on this card.



12

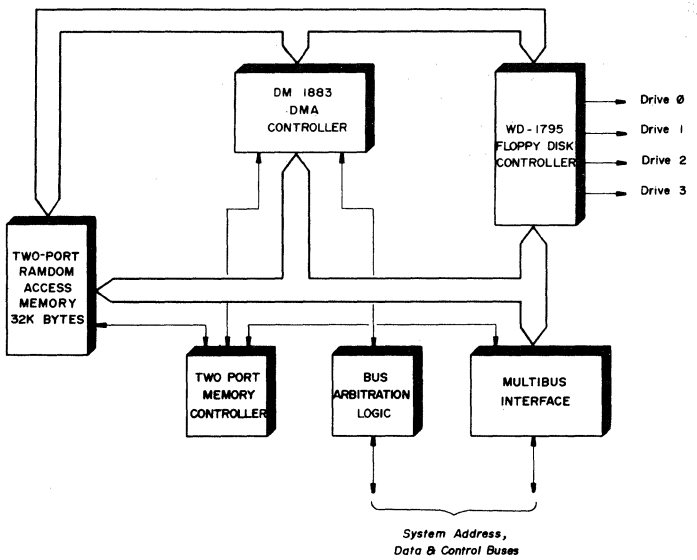



Figure 1. FFD-1 Block Diagram

## FLOPPY DISK CONTROLLER

At the heart of the FFD-1 design is the FD-1791-01 Programmable Floppy Disk Formatter/Controller chip. This 40-pin MOS LSI device provides all the control circuity required to interface virtually any standard 5¼" or 8" floppy diskette drives using either single or double density recording formats. Advanced features of the FD-1791-01 include read/write and format of address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. Because the Floppy Disk Controller is programmable, its performance is not compromised by its universal drive compatibility. The track-to-track access, head-load, and head-unload characteristics of the selected drive model are program specified.

The FD-1791-01 Floppy Disk Controller allows the user to configure his system to use most standard and non-standard recording formats. Sector lengths of 128, 256, 512, or 1024 bytes per sector are obtainable in either FM (single density) or MFM (double density) formats. The number of sectors per track (as far as the FD-1791-01 is concerned) is user selectable from 1 to 255 sectors per track. The number of tracks can also be programmed from 0 to 255 tracks. For !BM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For system 34 (MFM) compatibility, sector lengths are 256 bytes/sector with 26 sectors/track, or 1024 bytes/sector with 8 sectors/track.

The Floppy Disk Controller (FDC) chip recognizes 11 unique instructions (table 1), simplifying system software development. The FDC can read, write and verify both single and multiple sectors. Also included in the FD-1791-01 instruction set are automatic sector search and entire track read and write for disk formatting. Contained within these instructions, moreover, are various fields and flags for programmable control manipulation. These flags are used to select track-to-track stepping rate, single/multiple read/write, and interrupt conditions. Other functions performed by the instruction flags are: enable verification on destination track, update Track Register for each Head Step command, enable side select, and enable side compare.

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| COMMAND | BITS | | | | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| RESTORE | 0 | 0 | 0 | 0 | h | V | r | r | Move head to track 00 |
| SEEK | 0 | 0 | 0 | 1 | h | V | r | r | Move head to specified track |
| STEP | 0 | 0 | 1 | u | h | V | r | r | Step head in same direction as previous step command |
| STEP IN | 0 | 1 | 0 | u | h | V | r | r | Step head toward track 76 |
| STEP OUT | 0 | 1 | 1 | u | h | V | r | r | Step head toward track 00 |
| READ SECTOR | 1 | 0 | 0 | m | S | E | C | 0 | Read specified sector(s) |
| WRITE SECTOR | 1 | 0 | 1 | m | S | E | C | a | Write specified sector(s) |
| READ ADDRESS | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 | Read track number, side, sector number, and sector length |
| READ TRACK | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 | Read entire track starting at sector 0 |
| WRITE TRACK | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 | Write entire track starting at sector 0 |
| FORCE INTERRUPT | 1 | 1 | 0 | 1 | I | I | I | I | Terminate current command and generate interrupt |

Table 1. Command Summary

## ON-BOARD MEMORY

The FFD-1 can be supplied with an optional 32K bytes of on-board dynamic RAM. This on-board memory can be used as a supplement to system memory and can be positioned on any 32K byte boundary within the one megabyte Multibus system address space. It can be either byte or word oriented and may be enabled/disabled (in 4K byte increments) through programmed I/O.

Access to the on-board RAM memory is controlled by a dual port dynamic RAM controller. Memory access requests from the Multibus system are assigned highest priority, however if a memory request occurs while another cycle is in progress it will be delayed until the present request has been completed. The dynamic RAM controller also ensures that the on-board memory is refreshed in such a way as to be "transparent" to the rest of the system.

### DMA CONTROLLER

DMA transfers between the FFD-1 and the system memory (or between the Floppy Disk Controller and the on-board memory) can be made without CPU intervention by the on-board DMA controller. The FFD-1 employs a unique two mode DMA data transfer scheme for the highest possible data transfer rate.

In Mode 1, the FFD-1 card becomes the bus master and the DMA Controller transfers data between the disk controller and the system memory. Single or multiple sectors are transferred without CPU intervention. On completion of the task, an interrupt is generated or a flag bit is set in the DMAC status register. DMA transfers may be either transparent (the DMAC will release control of the bus after the transfer of each byte or burst), or the DMA Controller will retain control of the bus until the task is complete. The DMA Controller can address system memory anywhere within the one megabyte Multibus address space.

Mode 2 is similiar to Mode 1 except that the DMA Controller transfers data between the disk controller and the on-board RAM. This technique allows memory-disk transfers to be made while the system bus is left free for other uses.

### MULTIBUS INTERFACE

The Matrox FFD-1 plugs directly into the Multibus and works with both 8 and 16-bit processors. Bus arbitration logic enables the card to take control of the system bus and perform direct data transfers between disk and system memory.

### PROGRAMMING

The host processor programs, controls, and communicates with the FFD-1 by accessing 15 I/O locations. On power-up or reset, the FFD-1's command registers must be loaded with the correct operating parameters.

| REGISTER | ADDRESS | DESCRIPTION | |
|---|---|---|---|
| | | READ | WRITE |
| FDC STATUS/COMMAND | BASE + 0 | FDC status | FDC command |
| FDC TRACK | BASE + 1 | Current track number | Desired track number |
| FDC SECTOR | BASE + 2 | Current sector number | Desired sector number |
| FDC DATA | BASE + 3 | Data from disk | Data or track number for seek command |
| CONTROL and WAIT | BASE + 4 | Wait for-<br>— End of Command<br>— Data Request | FFD-1 controls |
| DRIVE SELECT and FLAG | BASE + 5 | Flags | Select drive |
| MEMORY BLOCK ENABLE | BASE + 6 | | Enable/disable 4K segments of on-board memory |
| DMAC CONTROL | BASE + 8 | DMAC controls | DMAC controls |
| DMAC STATUS | BASE + 9 | DMAC status | DMAC status |
| DMAC TRANSFER COUNT LOW | BASE + A | | Lower 8 bits of DMA transfer count |
| DNAC TRANSFER COUNT HIGH | BASE + B | | Higher 8 bits of DMA transfer count |
| DMAC MEMORY ADD LOW | BASE + C | | Lower 8 bits of DMA destination memory address |
| DMAC MEMORY ADD HIGH | BASE + D | | Higher 8 bits of DMA destination memory address |
| DMAC MEMORY ADD EXTENSION | BASE + E | | Bits 16-17 of DMA destination memory address (1 megabyte range) |
| DMAC INTERRUPT VECTOR | BASE + F | Interrupt vector address | Interrupt vector address |

Table 2. FFD-1 Register Definitions

# SPECIFICATIONS

**MEDIA**

Flexible 5¼" or 8" standard disk
One or two surfaces per disk

**COMPATIBLE DRIVES**

SHUGART SA800
SHUGART SA850 (double sided)
SIEMENS FFD-100-8
SIEMENS FFD-200-8 (double sided)
PERTEC FD-650 (double sided)
REMEX RFD 2000/2001
REMEX RFD 4000/4001 (double sided)

**DRIVE CHARACTERISTICS**

| | |
|---|---|
| TRANSFER RATE (K bytes/sec) | 250 (single density), 500 (double density) |
| DISK SPEED (RPM) | 360 |
| TRACK-TO-TRACK ACCESS | 3, 6, 10 or 15ms |
| HEAD SETTLING TIME | 182ms (max) |
| HEAD LOAD TIME | 15ms (min) |

**DISK FORMATS**

| | SINGLE DENSITY (FM) | | | | | | DOUBLE DENSITY (MFM) | |
|---|---|---|---|---|---|---|---|---|
| | IBM | | | NON-IBM | | | IBM | NON-IBM |
| BYTES/SECTOR | 128 | 256 | 512 | 128 | 512 | 1024 | 256 128 | 512 1024 |
| SECTORS/TRACK | 28 | 15 | 8 | 30 | 8 | 4 | 26 52 | 16 9 |
| TRACKS/DISKETTE | 77 | 77 | 77 | up to 255 | up to 255 | up to 255 | 77 | up to 255 |
| BYTES/DISKETTE | 256,256 | 295,980 | 315,392 | 295,680 | 315,392 | 315,392 | 512,512 | 700,000 |

**ON-BOARD RAM**

32K bytes of two-port dynamic RAM with on-board refresh circuitry (OPTIONAL)

| | ACCESS | CYCLE |
|---|---|---|
| READ | 425ns | 600ns |
| WRITE | — | 600ns |

**DMA CONTROLLER**

| | |
|---|---|
| DATA TRANSFERS | up to 65,536 bytes |
| TRANSFER RATE | 62K bytes/sec (max) |

**BUS INTERFACE**

Address, data, and control signals conform to Intel Multibus Specification No. 9800683.

Control, Status, and Data Registers — Strap selectable to any 16 I/O address boundary — 00-$FF_H$ ($B0_H$)
On-board dynamic RAM — Strap selectable on any 32K byte memory address boundary — 00000-FFFFFH (00000H)

**CONNECTORS**

| DESCRIPTION | MATING CONNECTOR |
|---|---|
| P1: 86 pin edge connector, 0.156" centers — Multibus interface | COMPAR ESM-43-DSRI |
| J2: 50 pin right angle header — Disk Drive interface | MOLEX 10-55-3505 |

**SIZE**

| | |
|---|---|
| WIDTH: | 12.00 in. (30.48 cm) |
| HEIGHT: | 6.75 in. (17.15 cm) |
| DEPTH: | 0.50 in. ( 1.27 cm) |

**POWER REQUIREMENTS**

+5V DC ±5% @ 2.5A
−12V DC ±5% @ 0.3A

**ENVIRONMENTAL REQUIREMENTS**

| | |
|---|---|
| OPERATING TEMPERATURE: | 0-50°C |
| RELATIVE HUMIDITY: | 0-90% non-condensing |

**ORDERING INFORMATION**

FFD-1/XX
- 00 — Floppy disk controller board
- 32 — Floppy disk controller with 32K bytes of on board dynamic RAM

**SUPPORT PRODUCTS**

| | |
|---|---|
| DF-28S | Dual 8" single sided disk drives (19" rack mount) |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
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# COM-1

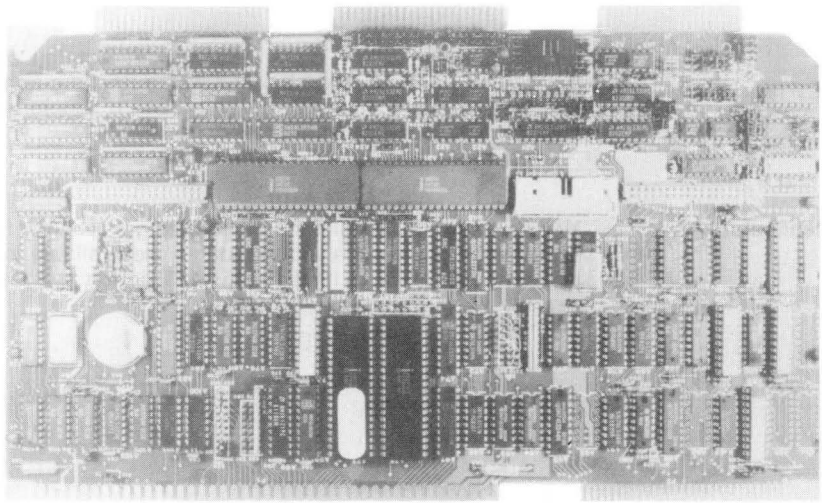
## HIGH SPEED MULTIBUS COMMUNICATIONS BOARD

- **9 I/O ports and 8 Multibus DMA channels**
- **16-bit parallel I/O port accommodates DMA transfers at up to 400K words/second**
- **Up to 8 serial I/O ports with data transfer rates up to 880K baud**
- **Local Area Network node interface**
- **1 Megabyte/second Multibus transfer rate**
- **VAX to Multibus DMA interface**
- **Real-time clock with battery back-up**
- **Two iSBX Multimodule sockets**
- **Multibus compatible (24-bit addressing)**

The COM-1 is a high performance communications board which enables any Multibus system to communicate with a wide range of computers and peripherals, at very high speeds, using DMA. The board has one on-board parallel port and up to eight serial I/O ports. Eight on-board Multibus DMA channels handle data transfers between any combination of Multibus RAM and I/O ports.

One bi-directional 16-bit parallel I/O port transfers data between a Multibus based system and a DEC VAX supermini, PDP-11, or LSI-11 computer at speeds of up to 400K words/second over distances of up to 50 feet. Three high speed serial lines (RS-232/RS-423) are standard and support transfer rates of up to 300K baud at 40 feet or up to 2.4K baud at 4000 feet. A fourth, multipurpose, serial port can be used in one of four modes: RS-449/422 (800K baud over 400 feet or 100K baud over 4000 feet max.), RS-449/423, RS-232/423 (300K baud over 40 feet or 2.4K baud over 4000 feet max.) or as a local area network node interface (MANET). MANET can support up to twelve nodes with data transfer rates of up to 880K baud. Two on-board iSBX connectors allow expansion to a total of 8 serial ports by using two Matrox MSBX-423 multimodules.

The COM-1's built-in flexibility and user programmability allows the OEM system designer to easily configure the board for a wide range of applications. Very high speed system communications performance is obtained with a minimum of design time and effort, at a low cost.



# COM-1 FEATURES

**Parallel Interface to VAX:**

The COM-1 can be directly interfaced to a VAX super minicomputer. The VAX communicates with the COM-1 as it would with any other DEC computer (Interprocessor Link) and can transfer data at transfer rates of 400K words/second over distances of up to 50 feet. The parallel DMA handshaking is compatible with DEC's DR-11W series interface cards. PDP-11 and LSI-11 computers can also be interfaced to the COM-1.

**Four Programmable Serial Channels:**

Four independent serial communications channels are supported on-board the COM-1. Each channel can be individually programmed to operate using most popular serial communications protocols, including asynchronous, character-oriented synchronous such as IBM Bisync, and bit-oriented synchronous such as HDLC and SDLC. Transmission rates can be individually defined, for each channel, up to 307.2K baud for channels 0-2 and up to 880K baud for channel 3.

**Distance and Cabling:**

A maximum data transfer rate/distance tradeoff enables the user to optimize the communications link. The parallel interface can run at 400K words/second at up to 50 feet. An RS-449 serial interface, with RS-422 drivers, supports data transfers of 880K baud over 400 feet or a maximum of 100K baud at 4000 feet. RS-232 serial interfaces, using RS-423 drivers, are capable of 300K baud at 40 feet or 2.4K baud at 4000 feet. Standard flat ribbon cables are used.

**LAN Node:**

An on-board multipurpose serial port can be used as a MANET Local Area Network node. Matrox's MANET supports up to 12 nodes at speeds up to 880K baud over distances up to 50 feet.

**8 DMA Channels:**

High speed data transfers can be made, via the COM-1, between Multibus memory and any one of eight peripheral devices, including memory to memory data transfers. Block transfers of up to 64K bytes can be supported. A user programmable DMA request matrix enables the user to select which 8, out of a possible 13, devices will transfer data through DMA. The other five devices transfer data by I/O port.

**Interrupt Matrix:**

The COM-1 can generate up to 13 different interrupts which are mapped, by the on-board user-programmable interrupt matrix, to up to 8 direct vector interrupt lines on the Multibus.

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**Real-Time Clock:**

An on-board real-time clock provides time-of-day calculation to within one tenth of one second precision and with automatic Leap Year adjustments. The real-time clock is backed-up by an on-board lithium battery to ensure the time count validity during power interruptions.

**Two iSBX Expansion Connectors:**

Two on-board iSBX Multimodule connectors allow for further system I/O expansion. Multimodule expansion modules are available from a number of sources including Matrox and Intel (MSBX-423 option increases the number of serial ports to 8).

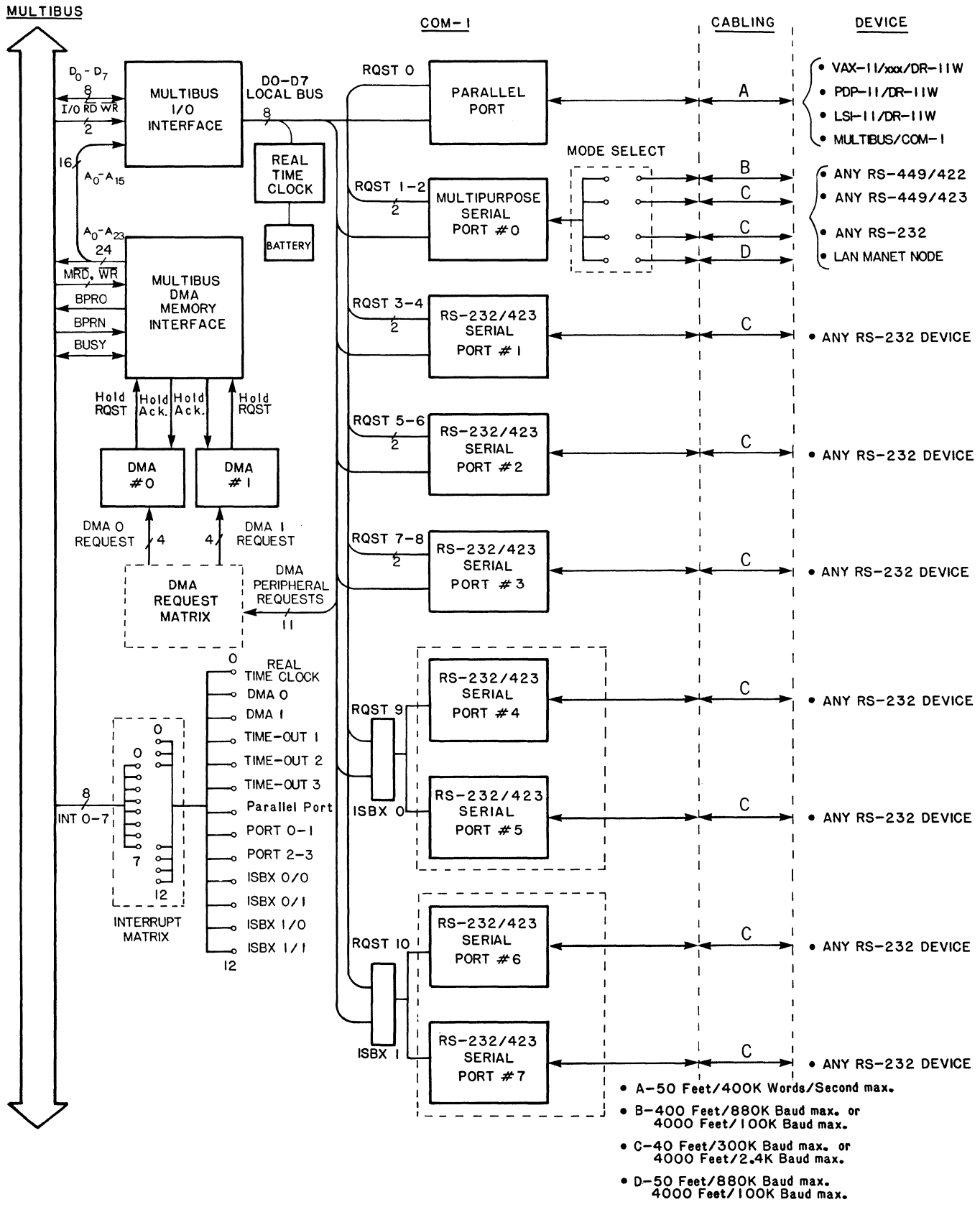



Figure 1. COM-1 system architecture

## FUNCTIONAL DESCRIPTION

The COM-1 has one parallel port (port 0) and four serial ports (ports 1-4). Optionally, by adding two Matrox MSBX-423 Multimodules, the number of serial ports can be expanded to eight. Each serial port has its own baud rate generator and can be programmed for a wide range of speeds, protocols, and formats.

Two DMA controllers accept 8 DMA data transfer requests from I/O ports. Since there can be more I/O requests than available DMA channels, the system designer can program which ports will transfer data using DMA and which will transfer data by programmed I/O, by straps on the DMA request matrix.

The COM-1 has an 8-level interrupt matrix which enables the user to program access to the Multibus for any combination of up to 13 internally generated interrupts. The rest of the interrupts can be polled and read by the host to determine which one caused the particular interrupt, through internal COM-1 I/O registers.

A real-time clock provides continuous time-of-day, accurate to within one-tenth of a second. On-board battery back-up can maintain the operation of the clock, in stand-by mode, for several years.

The user has access to all control and data registers on the COM-1 through the Multibus I/O space. COM-1 registers occupy 113 positions of a 128 addressing block from an 8-bit or 16-bit (strap-selectable) I/O addressing space.

## SERIAL PORTS (1-8)

Two LSI multi-protocol serial controllers handle the four serial lines on the COM-1. Each of the four channels can be programmed and operated independently and can support communications using either synchronous or asynchronous protocols. Data integrity, on each channel, is assured by double buffered transmitters and quadruple buffered receivers.

**Protocols** — Each of the four serial channels can be programmed to operate using any of the popular communications protocols. Character length can be defined as being 5, 6, 7, or 8 bits long. In asynchronous mode the user can further select the number of stop bits as being 1, 1½, or 2 bits. Transmission speeds in the asynchronous mode can be 1, 1/16, 1/32, or 1/64 the input clock frequency.

Both Character-Oriented and Bit-Oriented synchronous protocols are also suppored on the COM-1. When programmed for character-oriented protocols, the on-board serial controller allows the user to define the sync character. Sync characters can be either 8-bits (Monosync) or 16-bits (Bisync) long. Synchronization can alternately be established by monitoring the Sync input line (External). In bit-oriented (SDLC/HDLC) the COM-1 includes automatic zero insertion and deletion logic to differentiate between data and framing flags. The maximum data rate for all synchronous operations is 307.2K baud for channels 2 to 8. Channel 1 can be strapped to operate using the RS-449 serial interface standard, and as such can transmit data at up to 880K baud.

The COM-1 allows the user to program the Cyclic Redundancy Check (CRC) algorithm. Either the CRC-16 or the CRC-CCITT polynomial can be used. Internal logic allows the user to selectively exclude characters from the CRC calculations for both the transmitter and the receiver. This feature permits various portions of the message to be defined as non-character binary data ("transparent data").

**Programming** — The on-board serial controllers are programmed via a pair of I/O registers (Data Port and Control Port) for each channel. These registers are used, in turn, to indirectly access a further set of 8 Control registers and 3 Status registers which are internal to the serial controllers. These internal registers are independently maintained for each serial channel with the exception of one Control and one Status register, which are shared between two channels.

| FREQUENCY SELECT | OUTPUT FREQUENCY (KHz) | |
|---|---|---|
| | GENERATORS 0-2 | GENERATOR 3 |
| 0 0 0 0 | 0.800 | 275.000 |
| 0 0 0 1 | 1.200 | 293.333 |
| 0 0 1 0 | 1.759 | 314.286 |
| 0 0 1 1 | 2.152 | 338.462 |
| 0 1 0 0 | 2.400 | 366.667 |
| 0 1 0 1 | 4.800 | 400.000 |
| 0 1 1 0 | 9.600 | 440.000 |
| 0 1 1 1 | 19.200 | 488.888 |
| 1 0 0 0 | 28.744 | 550.000 |
| 1 0 0 1 | 31.917 | 628.571 |
| 1 0 1 0 | 38.400 | 733.333 |
| 1 0 1 1 | 57.826 | 880.000 |
| 1 1 0 0 | 76.800 | 1.100 MHz |
| 1 1 0 1 | 114.307 | 1.467 MHz |
| 1 1 1 0 | 153.600 | 2.200 MHz |
| 1 1 1 1 | 307.200 | — |
| Note: Frequency Select 1111 is invalid for channel 3 | | |

Table 1. Baud Rate generator output frequencies

The COM-1's serial controllers recognize a number of commands commonly used during the operation of the serial channels. These commands are executed by passing the appropriate command code to the Command Register of that channel. Commands include: Abort, Reset External/Status Interrupts, Channel Reset, Enable Interrupt on Next Character, Reset pending "Transmitter Becoming Empty" Interrupt, Error Reset, and End of Interrupt.

**Baud Rate Generators** — The on-board baud rate generators are independent; one for each serial channel. Each baud rate generator, in addition, provides two separate frequency outputs to allow the user to independently select the data rates for each receiver and transmitter. Each frequency output can be individually programmed to generate one of 16 different frequencies. Baud Rate Generators 2 — 8 can be programmed to produce output frequencies of from 800 Hz to 307.2 KHz. These clock frequencies are then divided, in the serial controller, by a user selectable divisor of from one to 64 to yield usable data rates ranging from 12.5 baud to 307.2K baud. Baud Rate Generator 3 can be programmed for clock frequencies of from 220 KHz to 1.76 MHz, or effective baud rates of from 3.43K baud to 880K baud.

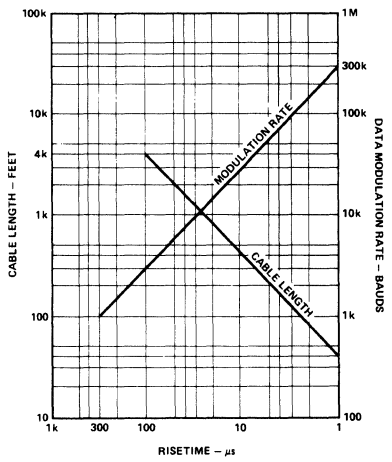



Figure 2. Data rate or cable length versus risetime for RS-423

The frequency outputs of each of the four baud rate generators is separately defined by loading an 8-bit register in each device. Using this data byte, the user can select one of 16 receiver frequencies (encoded in the lower four bits) and one of 16 transmitter frequencies (contained in the four most significant bits). Table 1 outlines the available frequencies for each baud rate generator.

**Drivers/Receivers** — The drivers and receivers for serial channels 2 — 8 conform to the EIA RS-232C serial interface standard and employ RS-423 (electrical characteristics for unbalanced digital interface circuits) standard line drivers and receivers. This configuration allows serial transmissions of up to 300K baud along interconnecting cables of 40 feet (cable length is dependent on the data rate and longer cables can be used with reduced data rates).

**Serial channel 1** can be hardware strapped to conform to either EIA RS-232C or RS-449 standards using RS-423 (unbalanced) or RS-422 (balanced) standard drivers and receivers. Using the RS-449 interface standard with RS-422 drivers results in a maximum throughput rate of 880K baud over a 400 foot cable. The RS-422 balanced electrical standard also provides improved noise immunity characteristics.

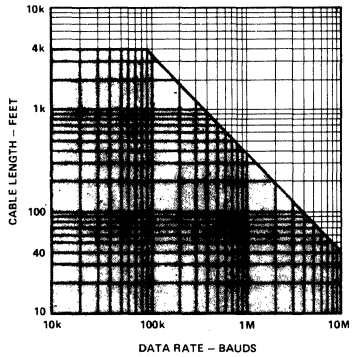



Figure 3. Data rate versus cable length for RS-422

## PARALLEL PORT (0)

The COM-1 contains an on-board 16-bit parallel interface, designed to allow direct communications between the Multibus and a DEC VAX super minicomputer, via a DR-11W interface module. To the DEC machine, the COM-1 resembles another DR-11W device. Communication with the COM-1 is the same as communication with any other DEC computer (VAX, PDP-11, LSI-11). Data transfers between the COM-1 and the DR-11W can be processed in a block mode, whereby a continuous block of data of up to 32K words can be transmitted in a single operation. In the block, or burst, mode, data can be transferred between the COM-1 and the DR-11W at up to 400K words/second.

Two COM-1's can be interconnected together, via this parallel interface, to form a high speed communications link between two Multibus systems.

## DMA MULTIBUS CHANNELS

The COM-1 can transfer data between the Multibus memory and any one of eight different peripherals via two on-board VLSI DMA controllers, at transfer rates of up to 880K bytes/second. DMA transfers can be made on continuous blocks of up to 64K bytes and can use one of three available transfer modes. In Single Transfer Mode, the DMA controller will release the system bus after every single byte transfer between memory and the peripheral device. Block Transfer Mode enables the DMA controller to continue making transfers, until a user defined word count expires. Finally, a Demand Transfer Mode is available to accommodate slower peripherals. Using the Demand Transfer Mode, the peripheral device holds its DMA request line active, and the DMA transfer continues, until it has exhausted its data capacity. After the device has had a chance to catch up, it re-asserts DREQ and the transfer process resumes. During the time between services, the intermediate address and word count values are stored and the host processor is allowed to regain control of the Multibus. Memory to memory DMA transfers are also supported via the COM-1.

Each of the on-board DMA controllers has two types of priority encoding schemes available as software selectable options. In the Fixed Priority Mode, each channel (each DMA controller supports four channels) is assigned a fixed priority whereby Channel 0 has the highest priority and Channel 3 represents the lowest priority. Optionally, the DMA controllers can be programmed to operate using a Rotating Priority scheme. This priority schedule assigns the last serviced channel as the lowest priority while the other channels are rotated accordingly. DMA Controller 1 always takes precedence over DMA Controller 0 in the priority heirarchy.

**Programming** — Each DMA controller is programmed via eight read/write I/O registers and four write-only registers (Command Register, Mode Register, Request Register, and Mask Register). Associated with each DMA channel (four channels/controller) is a 16-bit address register and a 16-bit word count register. These registers define the starting address, of the Multibus memory space to or from which the data transfer will take place, and the number of bytes to be transferred. Separate Address Extension Registers (for each DMA Request source) allow the DMA window to be positioned on any 64K byte boundary in the 16M byte Multibus memory address space.

The 8-bit Command Register and 8-bit Mode Register define the operational parameters of the DMA controller. Through the Command Register the user can: enable/disable the controller, enable/disable memory to memory transfers, and set



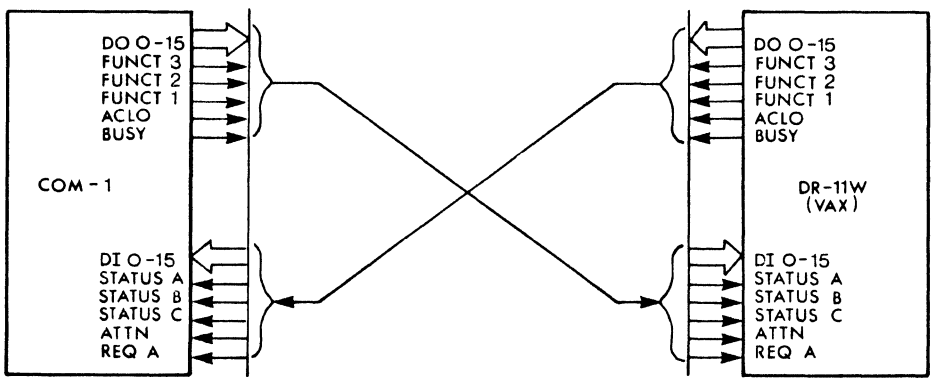



Figure 4. COM-1 to DR-11W interface cabling

the priority scheme. The Mode Register is used to define the type of DMA transfer each channel will respond with when a DMA request is sensed. The Mode Register is also used to enable an Autoinitialization feature of the DMA controller. The Autoinitialize feature resets the address and word count registers to their original values after a DMA transfer has been completed. The three-bit write-only Request Register can be used to request a DMA transfer through software, while the three-bit Mask Register can disable DMA requests from any of the four DMA channels. The DMA request enable/disable status for all four channels can be set in a single instruction through a separate four-bit Mask Register.

### REAL-TIME CLOCK

An on-board real-time clock provides continuous time of day measurement, accurate to within one-tenth of a second. Internal counters are available to yield the elapsed time in tenth of seconds, seconds, minutes, hours, days, and months since the initialization of the clock. Internal logic is also incorporated to compensate for the effects of Leap Year, once every four years.

The real-time clock can be programmed to generate an interrupt at 60 second, 5.0 second, or 0.5 second intervals. Interrupts can also be programmed to operate either as a one-shot interrupt (single interrupt at the completion of the selected timing period) or in continuous mode which allows for automatically repeated timer interrupts.

**Programming** — The on-board real-time clock is programmed via 16 4-bit I/O registers. Nine of these registers are used to load the initial time data into the clock (minutes, hours, days, and months). An additional write-only register is used to program the current year, in relation to Leap Year (i.e. Leap Year, Leap Year + 1, Leap Year + 2, Leap Year + 3). In reading the time-of-day from the clock, three read only registers combine with the nine registers previously mentioned to provide a time count precision to within one-tenth of one second. A Start/Stop Register permits precise starting of the clock, once the initial values have been loaded.

**Battery Back-Up** — An on-board 3V Lithium battery ensures the continued time-of-day integrity through any power interruptions. Relying strictly on the Lithium battery for power, the real-time clock could maintain operation for well over a year. Under normal operations, with the battery in stand-by mode, the battery will last for several years.

### INTERRUPTS

The COM-1 supports 13 different interrupt sources, up to 8 of which can be hardware strapped to the eight available Multibus interrupt lines. Two on-board I/O registers also latch the status of each of the 13 interrupt sources and can be read by the host processor as an optional method of determining which interrupt source is requesting service. This method of interrupt servicing allows all 13 interrupt sources to be supported and also minimizes the number of Multibus interrupt lines required by the board. The interrupt sources recognized by the COM-1 include:

- 4 interrupt lines from iSBX connector 0
- 2 interrupt lines from the serial controllers
- 2 interrupt lines from the DMA controllers
- 1 interrupt line from the parallel port
- 1 interrupt line from the real-time clock
- 3 interrupt lines indicating time-outs during iSBX, DR-11W, or memory accesses

### MULTIBUS INTERFACE

The COM-1 plugs directly into the Multibus and conforms to the IEEE-796 bus specification. All COM-1 registers are I/O mapped and occupy 113 positions of a 128 addressing block from an 8-bit or 16-bit (strap selectable) I/O addressing space. Table 2 outlines this I/O register mapping. DMA transfers are performed using 8-bit data bytes. Memory addressing can be extended from 16 bits to 24 bits during DMA transfers, via an on-board address extension RAM table, although the source or destination address cannot cross 64K byte boundaries. The COM-1 can also provide a 10 MHz bus clock to the Multibus.

A software controlled Bus Override feature allows the COM-1 to retain control of the bus, during DMA transfers, until the transfer is complete. The COM-1 can also be strapped to release the bus to any other module, when requested by the CBREQ line.

### EXPANSION

The COM-1 supports two on-board iSBX Multimodule connectors to facilitate I/O communications expansion. Matrox offers a pair of Multimodule compatible serial interface controllers (MSBX-422 and MSBX-423) which can be plugged into these connectors. With two MSBX-423 modules installed, the COM-1 supports 8 serial lines. The two expansion sockets can also accept any other Multimodule, from any other manufacturer (Intel, Zendex, etc.) which conforms to the Intel iSBX-bus specification no. 142686-001.

### TYPICAL APPLICATIONS

The COM-1 is a versatile communications board which can be used in a wide range of systems. The COM-1 greatly reduces OEM system design time and effort and provides very high speed performance at a low cost. Typical applications include computer to computer communications, Local Area network communications, serial interfaces to peripheral devices. Multibus 8-channel DMA controller board, high speed data multiplexer/demultiplexer applications, etc. Multiple COM-1 boards can be used in the same Multibus chassis to increase the number of interface lines and DMA channels. The built-in flexibility and user-programmability allows the OEM system designer to easily adapt the board to these or any other applications requiring high speed communications.

### VAX-11/XXX TO MULTIBUS INTERFACE

The COM-1 will interface DEC VAX-11/730, 750, 780, or 790 series computers with any Multibus system. The bidirectional 16-bit port enables a sustained data transfer rate of over 400,000 words/second at up to 50 feet. The DEC DR-11W parallel interface in the Unibus VAX chassis is connected directly to the COM-1, in the Multibus chassis, by a dual 40-pin ribbon cabling and a Matrox supplied cable adaptor.

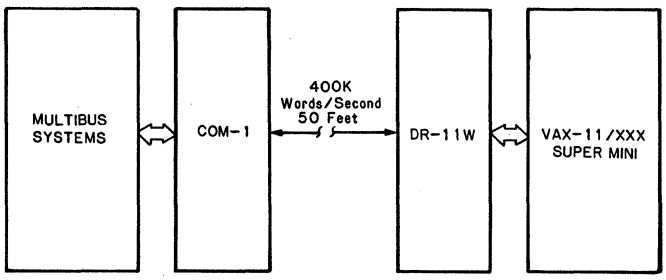



Figure 5. VAX to Multibus Interface

### PDP-11 TO MULTIBUS INTERFACE

The COM-1 will interface DEC PDP-11 series computers with any Multibus system. The bidirectional 16-bit port enables a sustained data transfer rate of over 400,000 words/second at up to 50 feet. The DEC DR-11W parallel interface in the Unibus chassis is connected directly to the COM-1, in the Multibus chassis, by a dual 40-pin ribbon cabling and a Matrox supplied cable adaptor.

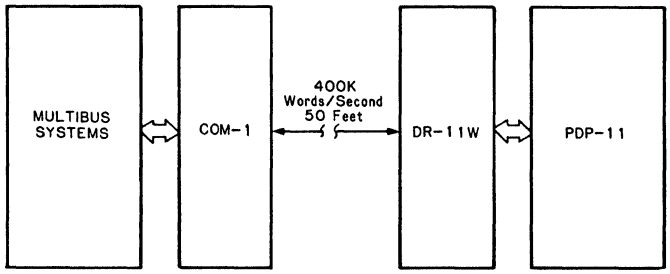



Figure 6. PDP-11 to Multibus Interface

## LSI-11 (Q-BUS) TO MULTIBUS INTERFACE

The COM-1 will interface DEC LSI-11 series computers with any Multibus system. The bidirectional 16-bit port enables a sustained data transfer rate of over 400,000 words/second at up to 50 feet. The DEC DR-11W parallel interface in the Q-bus chassis is connected directly to the COM-1, in the Multibus chassis, by a dual 40-pin ribbon cabling and a Matrox supplied cable adaptor.

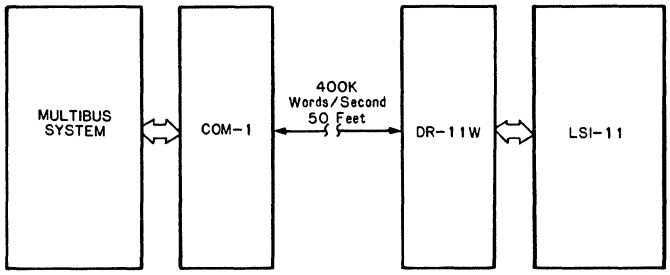



Figure 7. LSI-11 to Multibus Interface

## MULTIBUS TO MULTIBUS INTERFACE

Two Multibus systems can be interfaced with a COM-1 board in each system. Up to 800K byte/second transfer rates can be sustained from one Multibus RAM to the other Multibus RAM, using the 16-bit bidirectional port. If the serial RS-449/422 I/O port is used, 800K baud data rates over distances of 400 feet can be sustained.

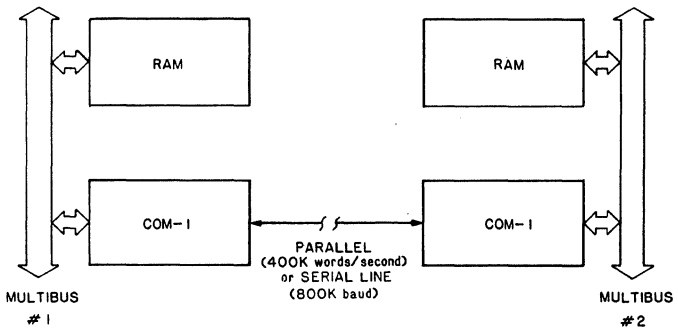



Figure 8. Multibus to Multibus Interface

## MULTIPLE SERIAL LINE INTERFACES

The COM-1 can be used as a four, or eight, serial line interface board to any RS-232, RS-423, or RS-422 peripheral device. A wide range of protocols, speeds, and formats are supported. The I/O data can be transferred to/from Multibus RAM at very high speed without any CPU support using the 8 on-board DMA channels, capable of sustaining a combined 1 Megabyte/second transfer rate on the Multibus. Alternatively, any serial port can be interfaced to the CPU by using I/O port transfers under CPU control. Up to 880K baud (RS-449/422) transfer rates per channel can be supported.

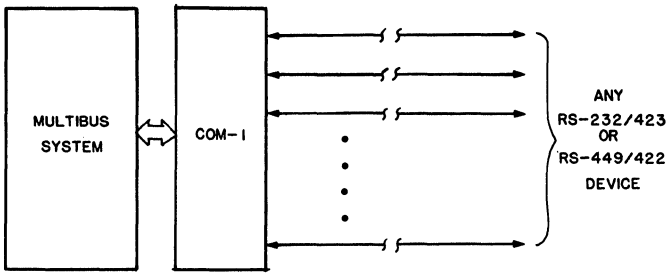



Figure 9. Multiple Serial Interface lines for Multibus systems

## MULTIBUS DMA CONTROLLER BOARD

The COM-1 can also be used as an 8 channel DMA controller board for any Multibus system. Memory to memory, I/O to memory, and memory to I/O DMA transfers are available for each channel under software control. Sustained combined Multibus DMA throughput is 1 Megabyte/second. Two iSBX connectors are also supported by the on-board DMA controllers, enabling the user to transfer data between any Multimodule (floppy or Winchester controller, laser printer, etc.) and Multibus RAM at up to 1 Megabytes/second.

## MANET — LOCAL AREA NETWORK

Multiple Multibus systems can be connected in a Matrox MANET Local Area Network by using the multipurpose serial port available on the COM-1 board. Transfer speeds of up to 880K baud using a network length of 50 feet, or 100K baud over a length of 4000 feet, are supported. A single cable with multiple twisted wires (5) is used as the transmission media. The MANET is software compatible with the Ethernet protocol at levels 2 and up.

For media access, the MANET uses the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) method which is similar to Ethernet. In order to transmit, any station wishing to transmit listens first. If the cable is busy (i.e. some other station is transmitting) the station waits until the line is clear before transmitting. (This is known as Carrier Sense and is implemented by the COM-1 hardware). When the cable is free

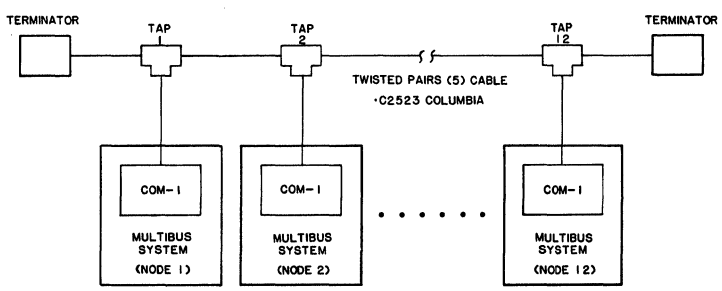



Figure 10. MANET LAN with 12 Multibus system nodes

(no other station is transmitting) a station can start transmitting. The transmitting station always listens while transmitting (local looping) in order to detect if any other station is also transmitting, causing a "collision". In that case the transmitting stations will continue transmitting for a fixed time to ensure that all transmitting stations detect the collision. This is known as a "Jam". After the jam, the stations stop transmitting and wait for a random period of time before retrying. The MANET is a multiple access network with no central controller, since all stations have equal priority access.

The above protocol is executed by the user's CPU, with a MANET driver routine, and the COM-1 hardware. The MANET driver routine is available from Matrox for 8088, 8086, or 80286 CPUs, under the CP/M-86 DOS, and is equivalent to Ethernet level 1. The user can also write his own protocol to drive the COM-1 hardware for optimum performance without using the MANET driver.

### HIGH SPEED DATA MULTIPLEXER/DEMULTIPLEXER

The COM-1 can be used as a multiple slow speed lines to single high speed line concentrator. For example, up to 8 RS-232 ports can be used locally at slow speed. The data from these seven or eight ports is then concentrated (packed) and transmitted to the remote host or other system using a single high speed line available on the COM-1. Either Parallel Port 0 (400,000 words/second) or Serial Port 1 (RS-449/422 at 880K baud) can be used. (Note that if Serial Port 1 is used, only seven serial lines are available as input data lines). This approach can significantly offload the host CPU and cut the number of interconnections to the host, from 8 to one. (The total sum of the sustained data rates on the multiple lines can not exceed the maximum data transfer rate of the single line; 400K words for the parallel port or 880K baud for the serial port).

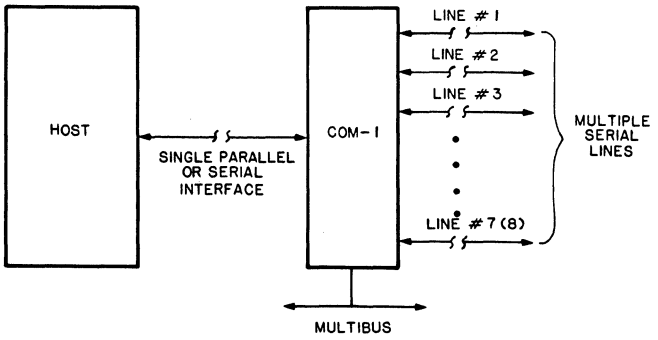



Figure 11. Multiple Serial Lines to Single Parallel (or serial) Line Data Multiplexer/Demultiplexer

| COM-1 I/O REGISTER | ADDRESS | TYPE | DESCRIPTION |
|---|---|---|---|
| Not Used | 00 to 06 | — | These locations are not used by the COM-1 |
| Memory to Memory Extension Register | 07 | WRITE ONLY | 8-bit destination memory address extension for data transfers between two blocks of memory |
| DREQ4 Extension Register | 08 | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 4 |
| DREQ5 Extension Register | 09 | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 5 |
| DREQ6 Extension Register | 0A | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 6 |
| DREQ7 Extension Register | 0B | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 7 |
| DREQ0 Extension Register | 0C | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 0 |
| DREQ1 Extension Register | 0D | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 1 |
| DREQ2 Extension Register | 0E | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 2 |
| DREQ3 Extension Register | 0F | WRITE ONLY | 8-bit source/destination memory address extension for data transfer between memory and DMA device 3 |
| Real-Time Clock Registers | 10 to 1F | READ/WRITE | Control, Status, and Data registers used to program the on-board real-time clock or read the time-of-day |
| DMA Controller 0 Registers | 20 to 2F | READ/WRITE | Command and Status registers used to program DMA Controller 0 |
| DMA Controller 1 Registers | 30 to 3F | READ/WRITE | Command and Status registers used to program DMA Controller 1 |
| Serial Controller 0 Registers | 40 to 43 | READ/WRITE | Command and Status registers used to program Serial Controller 0 (serial channels 0 and 1) |
| Serial Controller 1 Registers | 44 to 47 | READ/WRITE | Command and Status registers used to program Serial Controller 1 (serial channels 2 and 3) |
| Baud Rate Select Register 0 | 48 | WRITE ONLY | 8-bit register used to select the receiver and transmitter clock frequencies for serial channel 0 |
| Baud Rate Select Register 1 | 49 | WRITE ONLY | 8-bit register used to select the receiver and transmitter clock frequencies for serial channel 1 |
| Baud Rate Select Register 2 | 4A | WRITE ONLY | 8-bit register used to select the receiver and transmitter clock frequencies for serial channel 2 |
| Baud Rate Select Register 3 | 4B | WRITE ONLY | 8-bit register used to select the receiver and transmitter clock frequencies for serial channel 3 |
| DR-11W Control Register | 4C | WRITE ONLY | 6-bit register used to pass control information to the DR-11W (VAX) |
| Clear Time-Out Flags | 4D | WRITE ONLY | Reset interrupt lines 4-6 (iSBX time-out, memory time-out, and DR-11W time-out respectively) |
| COM-1 Control Register | 4E | WRITE ONLY | Set/reset interrupt enable and bus override enable |
| DR-11W Interrupt Clear | 4F | WRITE ONLY | Clear interrupt register of parallel interface |
| iSBX Module 0 Registers | 50 to 5F | READ/WRITE | 16 8-bit I/O registers for iSBX module 0 |
| iSBX Module 2 Registers | 60 to 6F | READ/WRITE | 16 8-bit I/O registers for iSBX module 1 |
| Interrupt Status Register 0 | 70 | READ ONLY | 6-bit register containing the status of interrupt lines 0-3 and the two iSBX present lines |
| Interrupt Status Register 1 | 71 | READ ONLY | 8-bit register containing the status of interrupt lines 4-11 |
| DR-11W Status Register | 72 | READ ONLY | 4-bit register containing DR-11W (VAX) status information |
| Clear Interrupt Flag 0 | 73 | READ ONLY | Reset interrupt line 0 (from iSBX connector 0) |
| Clear Interrupt Flag 1 | 74 | READ ONLY | Reset interrupt line 1 (from iSBX connector 0) |
| Clear Interrupt Flag 2 | 75 | READ ONLY | Reset interrupt line 2 (from iSBX connector 1) |
| Clear Interrupt Flag 3 | 76 | READ ONLY | Reset interrupt line 3 (from iSBX connector 1) |
| Clear Interrupt Flag 4 | 77 | READ ONLY | Reset interrupt lines 10 and 11 (from the DMA controllers) |
| Note: Interrupt lines 7 (real-time clock), 8 and 9 (serial controllers) are reset by writing to registers internal to the respective devices. | | | |

Table 2. COM-1 I/O mapping

# SPECIFICATIONS

## SERIAL INTERFACE

**Interface specifications**

| | |
|---|---|
| Channel 1-3: | RS-232C |
| Channel 0: | RS-232C, RS-449, or MANET (strap selectable) |

**LINE DRIVERS/RECEIVERS**

| | |
|---|---|
| Channel 1-3: | RS-423 |
| Channel 0: | RS-423, RS-422, or MANET (strap selectable) |

**Asynchronous Operation**

| | |
|---|---|
| Character Length: | 5, 6, 7 or 8 bits |
| Stop Bits: | 1, 1½, or 2 bits |
| Parity: | Even, odd, or disabled |
| Transmission Speed: | 1, 1/16, 1/32, 1/64 clock frequency |

Break Generation and Detection
Interrupt on Parity Overrun, or Framing Error (vectored or non-vectored)

**Synchronous Operation**

MONOSYNC, BISYNC, AND EXTERNAL SYNC OPERATION

| | |
|---|---|
| Sync Characters: | 8 or 16 bits |
| CRC Generation and Checking: | CRC-16 or CRC-CCITT |

Automatic Sync Insertion

HDLC AND SDLC OPERATION
Abort Sequence Generation and Detection
Automatic Zero Insertion and Detection
CRC Generation and Checking
I-Field Residue Handling

**Baud Rates**

| | |
|---|---|
| Channel 0-2: | 50 baud to 307.2K baud |
| Channel 3: | 50 baud to 880K baud |

## PARALLEL INTERFACE

| | |
|---|---|
| Word Size: | 16-bits |
| Transfer Rate: | 400K words/second max. |

## DMA CONTROLLER

| | |
|---|---|
| Word Size: | 8-bits |
| Block Size: | 65,536 words max. |
| No. of DMA Channels: | 8 |
| Priority Schedule: | Fixed or Rotating (software selectable) |

## REAL-TIME CLOCK

| | |
|---|---|
| Count Capability: | 0.1 seconds to 1 year |
| Interrupt Intervals: | 0.5, 5.0, or 60 seconds — one-shot or continuous |
| Battery Back-Up | |
| Duration: | 1 year |
| Part No.: | CR2032 |

## INTERRUPTS

Sources:

| | |
|---|---|
| Serial controllers | (2) |
| iSBX connectors | (4) |
| Real-time clock | (1) |
| DMA controllers | (2) |
| Time-outs | (3) |
| Parallel Interface | (1) |

Addressing: 8 of the 13 available interrupt sources can be strapped to the 8 Multibus Interrupt lines. Alternatively the 13 sources can be ORed to drive a single interrupt line and the CPU can interrogate a pair of on-board registers to determine which of the 13 interrupt sources is requesting service.

**ADDRESSING**

| | |
|---|---|
| DMA: | Data can be transferred to or from a block of system memory located an any 64K byte boundary in the 16M byte Multibus memory address space; 000000 — FFFFFFH |
| I/O Registers: | Command, and Status Registers occupy 113 locations of any 128 block of system I/O space; 0000 — FFFFH |

**INTERFACES**

| | |
|---|---|
| Multibus: | All signals TTL compatible |
| Serial I/O | |
| Channel 0-2: | RS-232C compatible |
| Channel 3: | RS-232C or RS-449 compatible |
| Parallel I/O: | All signals TTL compatible |
| Interrupt Requests: | All signals TTL compatible |

**CONNECTORS**

| | |
|---|---|
| Multibus: | 86-pin edge connector, 0.156" centers |
| Serial I/O | |
| Channel 0-1: | 50-pin edge connector, 0.1" centers |
| Channel 2: | 26-pin header |
| Channel 3: | 40-pin edge connector, 0.1" centers |
| Parallel I/O:* | 50-pin edge connector, 0.1" centers |

**Note:** The COM-1 is supplied with a separate cable adaptor to convert the 50-pin parallel interface, on the COM-1, to a dual 40-pin format like that on the DR-11W.

**PHYSICAL CHARACTERISTICS**

| | |
|---|---|
| Width: | 12.00 in. (30.48 cm) |
| Height: | 6.75 in. (17.15 cm) |
| Depth: | 0.62 in. ( 1.57 cm) |

**POWER REQUIREMENTS**

+5V @ 4.0A
+12V @ 220mA
−12V @ 220mA

**ENVIRONMENTAL CHARACTERISTICS**

| | |
|---|---|
| Operating Temperature: | 0° to 55°C (32° — 131°F) |
| Relative Humidity: | Up to 95% (non-condensing) |

**OPERATING INFORMATION**

COM-1/1/X: High-speed communications board

- 0 — No serial ports
- 1 — Includes 4 serial ports (3 x RS-232/423, 1 x MANET)
- 2 — Includes 4 serial ports (3 x RS-232/423, 1 x RS-422)

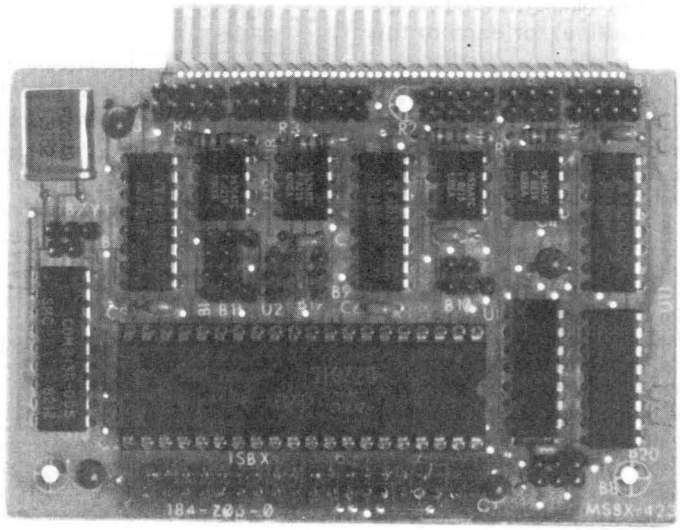
matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MSBX-423

## DUAL RS-232/423 SERIAL INTERFACE iSBX MODULE

- **Two independent serial communications ports**
- **Synchronous and Asynchronous operations**
- **Transmission Rates up to 307K baud**
- **iSBX bus compatible**
- **Programmable communications protocol**
- **RS-423/RS-232C compatible**
- **Modem control signals**
- **Interrupt on parity, overrun, or framing error**
- **Compatible with Matrox MBC-86/12, PBC-80 CPU cards**

The MSBX-423 module provides the user with two independent serial communications ports on a 3.70" x 2.85" board, which interfaces to a single width iSBX connector. An on-board Multi-Protocol Serial Controller allows user-definition of most communications protocol parameters, permiting operation in most popular asynchronous protocols, character-oriented synchronous protocols such as IBM Bisync, and bit-oriented synchronous protocols such as HDLC and IBM SDLC. Each channel can be programmed for data transmission rates up to 307K baud. Double-buffered transmitters and quadruple-buffered receivers ensures data validity.

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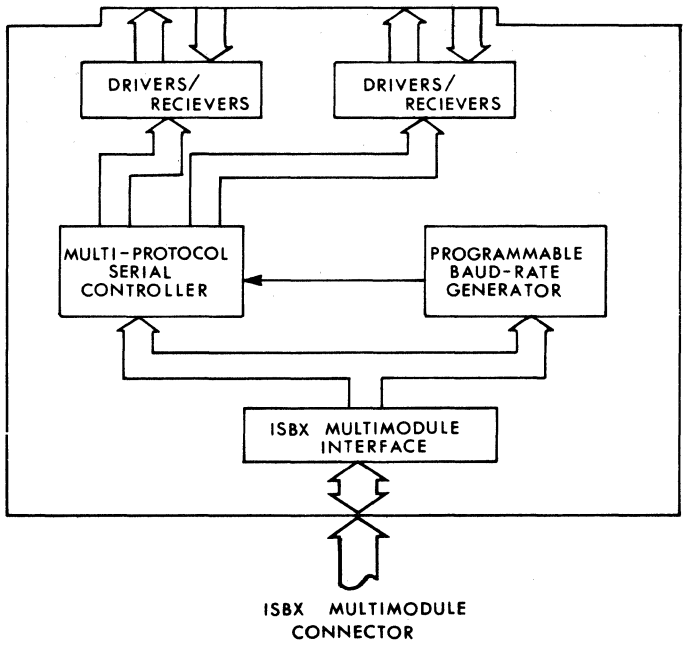


Figure 1. MSBX-423 block diagram

## MULTI-PROTOCOL SERIAL CONTROLLER

At the heart of the MSBX-423 is a Multi-Protocol Serial Controller. This VLSI IC supports two serial channels and permits communications using synchronous or asynchronous protocols. Each channel may be programmed and operated independently. Data integrity on the MSBX-423 is assured by double-buffered transmitters and quadruple-buffered receivers. Modem control signals are also supported for each channel.

Internal interrupt control logic prioritizes interrupt requests generated on the MSBX-423. These interrupts can originate from any one of three sources: Receiver Interrupts (Interrupt on First Character, Interrupt on All Characters, Parity, Overrun, or Framing Error, etc.), Transmitter Interrupt (Transmitter Buffer Empty), or External Status Interrupt (DCD, CTS, or Sync input transition, Break, Abort, etc.) The MSBX-423 can be programmed to release an 8-bit vector (pointer to an external service routine) for each of the interrupt requests.

**Protocols** — The MSBX-423 can be programmed to operate using virtually any serial communications protocol. Character length can be defined as being 5, 6, 7, or 8 bits long. In asynchronous mode the user can further select the number of stop bits as 1, 1½, or 2 bits. Transmission speeds in the asynchronous mode can be 1, 1/16, 1/32, or 1/64 the input clock frequency.

Both Character-Oriented and Bit-Oriented synchronous protocols are also supported on the MSBX-423. When programmed for character-oriented protocols, the on-board Serial Controller allows the user to define the sync character. Sync characters can be either 8-bit (Monosync) or 16-bits (Bisync) long. Synchronization can alternately be established by monitoring the Sync input line (External). In bit-oriented protocols (SDLC/HDLC) the MSBX-423 includes automatic zero insertion and deletion logic to differentiate between data and framing flags. The maximum data rate for all synchronous operations is 307.2K baud.

The MSBX-423 allows the user to program the Cyclic Redundancy Check (CRC) algorythm. Either the CRC-16 or the CRC-CCITT polynomial can be used. Internal logic allows the user to selectively exclude characters from the CRC calculations for both the transmitter and the receiver. This feature permits various portions of the message to be defined as non-character binary data ("transparent data").

**Programming** — The on-board Serial Controller is programmed via two I/O registers (Data Port and Command Port) for each channel. The registers are used, in turn, to access a set of registers internal to the Serial Controller (table 1). The internal registers are duplicated and independently maintained for each of the two serial channels with the exception of Control Register 2 and Status Register 2.

**CONTROL REGISTERS**

| CONTROL REGISTER | FUNCTION |
|---|---|
| 0 | Frequently used commands and Register Pointer Control |
| 1 | Interrupt Control |
| 2 | Processor/Bus Interface Control |
| 3 | Receiver Control |
| 4 | Mode Control |
| 5 | Transmitter Control |
| 6 | Sync/Address Character |
| 7 | Sync Character |

**STATUS REGISTERS**

| STATUS REGISTER | FUNCTION |
|---|---|
| 0 | Buffer and "External/Status" Status |
| 1 | Received Character Error and Special Condition Status |
| 2 (Channel B Only) | Interrupt Vector |

Table 1. Serial Controller internal registers

Control Register 2A is used to program the Controller's interface control circuitry, while Control Register 2B is used to define the Interrupt Vector response byte (if used). The Interrupt Vector can be read from Status Register 2B only.

The MSBX-423 recognizes a number of commands commonly used during the operation of the board. These commands are executed by passing the appropriate command code to Control Register 1. Commands include: Abort, Reset External/Status Interrupts, Channel Reset, Enable Interrupt on Next Character, Reset Pending "Transmitter Buffer Empty" Interrupt, Error Reset, and End of Interrupt.

### BAUD RATE GENERATOR

The on-board Baud Rate generator can be programmed, via system software, to provide one of 16 available frequencies at each of the two outputs. These output frequencies can then be routed, independently, to either the receiver or transmitter of either serial channel. In this way data transmission rates can be established such that:

a) Both channels have independent baud rates, but on each channel the transmitting and receiving rates are equal.

b) On each channel the transmitting and receiving rates are independent, but the two channels have the same frequencies.

**Programming** — The output frequencies from the Baud Rate Generator are defined by selecting one of 16 input frequency dividers for each output. Both dividers are selected simultaneously, by loading a single byte to the Baud Rate Generator Register. The four lower bits of this data byte are used to define the frequency divider for output 1 while the four most significant bits are used to select the divider for output 2. Dividers are available to provide output frequencies of up to 307.2 KHz (table 2).

| DIVIDER SELECT | DIVIDER | OUTPUT* FREQUENCY (KHz) |
|---|---|---|
| 0000 | 6144 | 0.800000 |
| 0001 | 4096 | 1.200000 |
| 0010 | 2793 | 1.758983 |
| 0011 | 2284 | 2.152000 |
| 0100 | 2048 | 2.400000 |
| 0101 | 1024 | 4.800000 |
| 0110 | 512 | 9.600000 |
| 0111 | 256 | 19.200000 |
| 1000 | 171 | 28.743859 |
| 1001 | 154 | 31.916883 |
| 1010 | 128 | 38.400000 |
| 1011 | 85 | 57.825882 |
| 1100 | 64 | 76.800000 |
| 1101 | 43 | 114.306976 |
| 1110 | 32 | 153.600000 |
| 1111 | 16 | 307.200000 |
| *Input Reference Frequency = 4.9152 MHz | | |

Table 2. Programmable data rates

### DRIVERS/RECEIVERS

The drivers and receivers on all communications lines are RS-423 compatible. This EIA unbalanced, bipolar voltage specification permits the communication of digital information over distances of up to 4000 feet and at data rates of up to 300 kilobaud. The MSBX-423 is also designed to interface with RS-232C thereby greatly enhancing its operational capabilities.

### BUS INTERFACE

The MSBX-423 plugs directly into any single width iSBX connector. Many companies now support CPU cards with the on-board facilities to accept modules such as the MSBX-423. Matrox supports two such CPU cards: the PBC-80 (8-bit Z-80A) and the MBC-86/12 (16-bit 8086).

### MOUNTING

The MSBX-423 is a "piggy back" card designed to be mounted directly onto host CPU cards that have provided provisions for iSBX modules. There are many CPU cards on the market today that meet this requirement, including the PBC-80 and MBC-86/12 from Matrox. The MSBX-423 is held in place on the host card by the iSBX connector and one nylon spacer (figure 2).

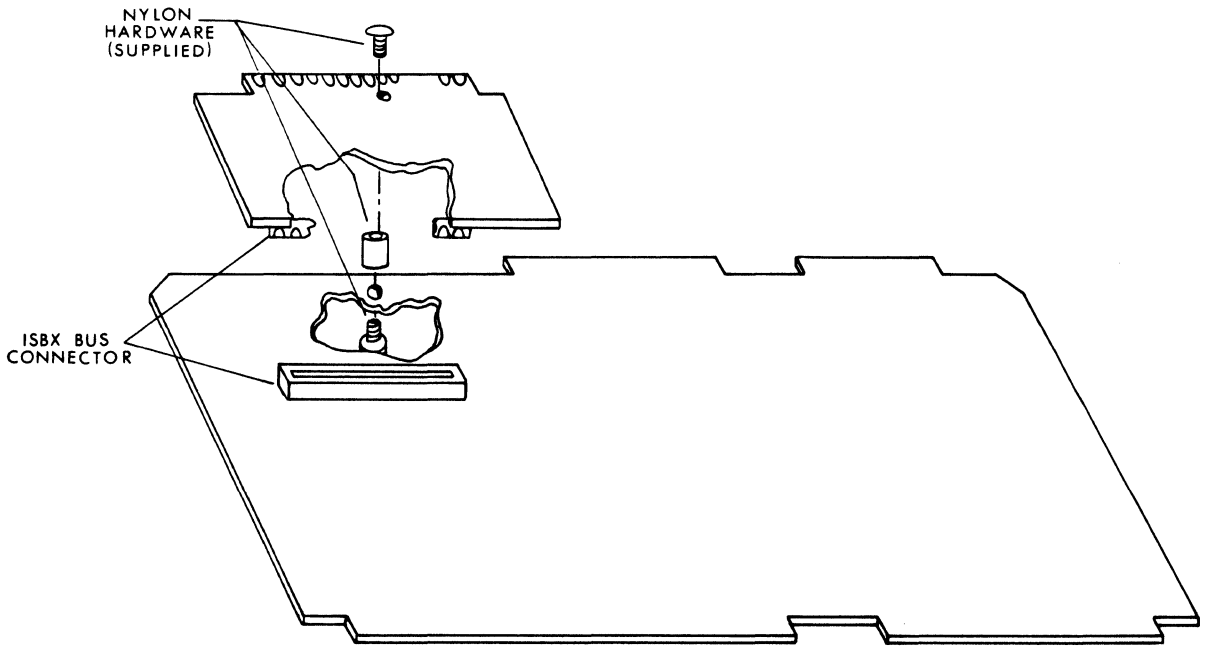


Figure 2. Mounting the MSBX-423

# SPECIFICATIONS

## ASYNCHRONOUS OPERATION

| | |
|---|---|
| Character Length: | 5, 6, 7, or 8 bits |
| Stop Bits: | 1, 1½, or 2 bits |
| Parity: | Even, odd, or disabled |
| Transmission Speed: | x1, x16, x32, x64 clock frequency |

Break Generation and Detection
Interrupt on Parity, Overrun, or Framing Error (vector or non-vector)

## SYNCHRONOUS OPERATION

MONOSYNC, BISYNC, AND EXTERNAL SYNC OPERATION

Sync Characters: 8 or 16 bits
CRC Generation and Checking (CRC-16 or CRC-CCITT)
Automatic Sync Insertion

HDLC AND SDLC OPERATION

Abort Sequence Generation and Detection
Automatic Zero Insertion and Detection
CRC Generation and Checking
I-Field Residue Handling

## BAUD RATES

| FREQUENCY (KHz) (software selectable) | BAUD RATE (Hz) | | | |
|---|---|---|---|---|
| | SYNCHRONOUS | ASYNCHRONOUS | | |
| | | ÷16 | ÷32 | ÷64 |
| 0.800000 | 800.00 | 50.00 | 25.00 | 12.50 |
| 1.200000 | 1200.00 | 75.00 | 37.50 | 18.75 |
| 1.758983 | 1758.98 | 109.93 | 54.96 | 27.48 |
| 2.152000 | 2152.00 | 134.50 | 67.25 | 33.62 |
| 2.400000 | 2400.00 | 150.00 | 75.00 | 37.50 |
| 4.800000 | 4800.00 | 300.00 | 150.00 | 75.00 |
| 9.600000 | 9600.00 | 600.00 | 300.00 | 150.00 |
| 19.200000 | 19200.00 | 1200.00 | 600.00 | 300.00 |
| 28.743859 | 28743.86 | 1796.49 | 898.24 | 449.12 |
| 31.916883 | 31916.88 | 1994.81 | 997.40 | 498.70 |
| 38.400000 | 38400.00 | 2400.00 | 1200.00 | 600.00 |
| 57.825882 | 57825.88 | 3614.11 | 1807.05 | 903.52 |
| 76.800000 | 76800.00 | 4800.00 | 2400.00 | 1200.00 |
| 114.306976 | 114306.97 | 7144.19 | 3572.09 | 1786.04 |
| 153.600000 | 153600.00 | 9600.00 | 4800.00 | 2400.00 |
| 307.200000 | 307200.00 | 19200.00 | 9600.00 | 4800.00 |

## INTERFACES

| | |
|---|---|
| iSBX bus: | All signals compatible with Intel iSBX bus Specification No. 142686-001 |
| Serial I/O: | RS-423/RS-232C compatible |

## CONNECTORS

| | |
|---|---|
| iSBX bus: | iSBX bus connector |
| Serial I/O: | 50 pin edge connector, O.1'' centers |

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## PHYSICAL CHARACTERISTICS

| | |
|---|---|
| Width: | 3.70 in. (9.39 cm) |
| Height: | 2.85 in. (7.24 cm) |
| Depth: | 0.50 in. (1.27 cm) |

## ENVIRONMENTAL CHARACTERISTICS

| | |
|---|---|
| Operating Temperature: | 0° to 55°C (32° to 131°F) |
| Relative Humidity: | Up to 95% (non-condensing) |

## ORDERING INFORMATION

| | |
|---|---|
| MSBX-423 | Dual serial interface card |

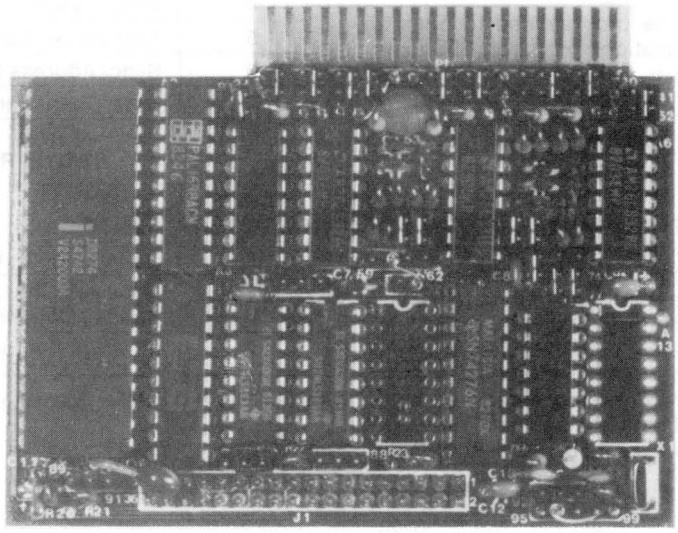
matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# MSBX-422

## RS-449/422 SERIAL INTERFACE iSBX MODULE

- **High speed serial communications port**
- **Synchronous and Asynchronous operations**
- **Transmission Rates up to 307K baud**
- **iSBX bus compatible**
- **Programmable communications protocol**
- **RS-422/RS-449 compatible**
- **Modem control signals**
- **Interrupt on parity, overrun, or framing error**
- **Compatible with Matrox MBC-86/12, PBC-80 CPU cards**

The MSBX-422 module provides the user with a high speed RS-449 serial communications port on a 3.70 x 2.85" board, which interfaces to a single width iSBX connector. An on-board Multi-Protocol Serial Controller allows user-definition of most communications protocol parameters, permiting operation in most popular asynchronous protocols, character-oriented synchronous protocols such as IBM Bisync, and bit-oriented synchronous protocols such as HDLC and IBM SDLC. Double-buffered transmitters and quadruple-buffered receivers ensures data validity.



12

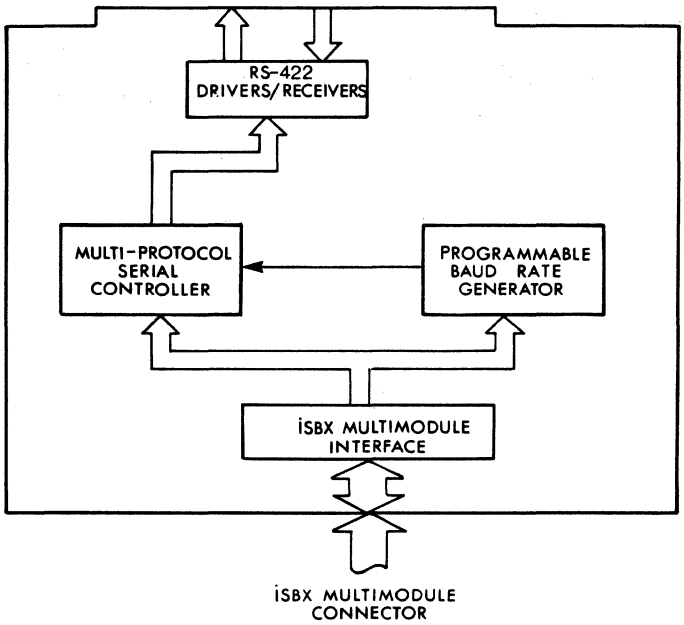



Figure 1. MSBX-422 block diagram

## MULTI-PROTOCOL SERIAL CONTROLLER

At the heart of the MSBX-422 is a Multi-Protocol Serial Controller which permits communications using synchronous or asynchronous protocols. Data integrity on the MSBX-422 is assured by double-buffered transmitters and quadruple-buffered receivers. Modem control signals are also supported.

Internal interrupt control logic prioritizes interrupt requests generated on the MSBX-422. These interrupts can originate from any one of three sources: Receiver Interrupts (interrupt on First Character, Interrupt on All Characters, Parity, Overrun, or Framing Error, etc.), Transmitter Interrupt (Transmitter Buffer Empty), or External Status Interrupt (DCD, CTS, or Sync input transition, Break, Abort, etc.). The MSBX-422 can be programmed to release an 8-bit vector (pointer to an external service routine) for each of the interrupt requests.

**Protocols** — The MSBX-422 can be programmed to operate using virtually any serial communications protocol. Character length can be defined as being 5, 6, 7, or 8 bits long. In asynchronous mode the user can further select the number of stop bits as 1, 1-1/2, or 2 bits. Transmission speeds in the asynchronous mode can be 1, 1/16, 1/32, or 1/64 the input clock frequency.

Both Character-Oriented and Bit-Oriented synchronous protocols are also supported on the MSBX-422. When programmed for character-oriented protocols, the on-board Serial Controller allows the user to define the sync character. Sync characters can be either 8-bits (Monosync) or 16-bits (Bisync) long. Synchronization can alternately be established by monitoring the Sync input line (External). In bit-oriented protocols (SDLC/HDLC) the MSBX-422 includes automatic zero insertion and deletion logic to differentiate between data and framing flags. The maximum data rate for all synchronous operations is 307.2K baud.

The MSBX-422 allows the user to program the Cyclic Redundancy Check (CRC) algorythm. Either the CRC-16 or the CRC-CCITT polynomial can be used. Internal logic allows the user to selectively exclude characters from the CRC calculations for both the transmitter and the receiver. This feature permits various portions of the message to be defined as non-character binary data ("transparent data").

**Programming** — The on-board Serial Controller is programmed via two I/O registers (Data Port and Command Port). These registers are used, in turn, to access a set of Control and Status registers internal to the Serial Controller (table 1).

| | CONTROL REGISTERS |
|---|---|
| **CONTROL REGISTER** | **FUNCTION** |
| 0 | Frequently used commands and Register Pointer Control |
| 1 | Interrupt Control |
| 2A | Processor/Bus Interface Control |
| 2B | Load Interrupt Vector |
| 3 | Receiver Control |
| 4 | Mode Control |
| 5 | Transmitter Control |
| 6 | Sync/Address Character |
| 7 | Sync Character |

**STATUS REGISTERS**

| STATUS REGISTER | FUNCTION |
|---|---|
| 0 | Buffer and "External/Status" Status |
| 1 | Received Character Error and Special Condition Status |
| 2 | Interrupt Vector |

Table 1. Serial Controller internal registers

The MSBX-422 recognizes a number of commands commonly used during the operation of the board. These commands are executed by passing the appropriate command code to Control Register 1. Commands include: Abort, Reset External/Status Interrupts, Channel Reset, Enable Interrupt on Next Character, Reset Pending "Transmitter Buffer Empty" Interrupt, Error Reset, and End of Interrupt.

### BAUD RATE GENERATOR

The on-board Baud Rate Generator provides two separate output frequencies to allow the user to independently select the data rates for the receiver and the transmitter. Each of the frequency outputs can be individually programmed, via the system software, to generate one of 16 different output frequencies. Frequencies of from 800 Hz to 307.2 KHz are available, from the Baud Rate Generator, which are then divided in the Serial Controller by a user selectable divisor of from 1 to 64 to yield a usable data rate ranging from 12.5 baud to 307.2K baud.

**Programming** — The output frequencies from the Baud Rate Generator are defined by selecting one of 16 input frequency dividers for each output. Both dividers are selected simultaneously, by loading a single byte to the Baud Rate Generator Register. The four lower bits of this data byte are used to define the frequency divider for output 1 (receiver) while the four most significant bits are used to select the divider for output 2 (transmitter). Dividers are available to provide output frequencies of up to 307.2 KHz (table 2).

### DRIVERS/RECEIVERS

The drivers and receivers on all communications lines are RS-422 compatible. This EIA balanced, bipolar voltage specification permits the communication of digital information over distances of up to 4000 feet and at data rates of up to 10 megabaud. The MSBX-422 is designed to interface with external peripherals using the RS-449 interface standard.

| DIVIDER SELECT | DIVIDER | OUTPUT* FREQUENCY (KHz) |
|---|---|---|
| 0000 | 6144 | 0.800000 |
| 0001 | 4096 | 1.200000 |
| 0010 | 2793 | 1.758983 |
| 0011 | 2284 | 2.152000 |
| 0100 | 2048 | 2.400000 |
| 0101 | 1024 | 4.800000 |
| 0110 | 512 | 9.600000 |
| 0111 | 256 | 19.200000 |
| 1000 | 171 | 28.743859 |
| 1001 | 154 | 31.916883 |
| 1010 | 128 | 38.400000 |
| 1011 | 85 | 57.825882 |
| 1100 | 64 | 76.800000 |
| 1101 | 43 | 114.306976 |
| 1110 | 32 | 153.600000 |
| 1111 | 16 | 307.200000 |
| *Input Reference Frequency = 4.9152 MHz | | |

Table 2. Programmable data rates

### BUS INTERFACE

The MSBX-422 plugs directly into any single width iSBX connector. Many companies now support CPU cards with the on-board facilities to accept modules such as the MSBX-422. Matrox supports two such CPU cards: the PBC-80 (8-bit Z-80A) and the MBC-86/12 (16-bit 8086).

### MOUNTING

The MSBX-422 is a "piggy back" card designed to be mounted directly onto host CPU cards that have provided provisions for iSBX modules. There are many CPU cards on the market today that meet this requirement, including the PBC-80 and MBC-86/12 from Matrox. The MSBX-422 is held in place on the host card by the iSBX connector and one nylon spacer (figure 2).

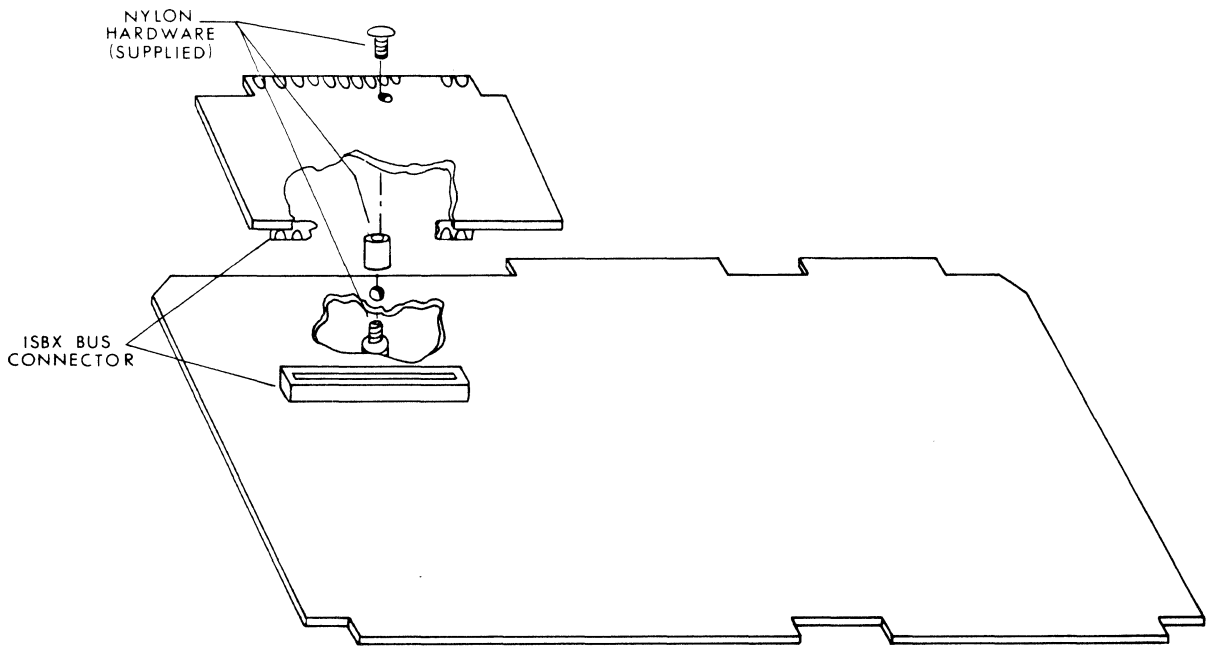



Figure 2. Mounting the MSBX-422

# SPECIFICATIONS

## ASYNCHRONOUS OPERATION

| | |
|---|---|
| Character Length: | 5, 6, 7, or 8 bits |
| Stop Bits: | 1, 1½, or 2 bits |
| Parity: | Even, odd, or disabled |
| Transmission Speed: | x1, x16, x32, x64 clock frequency |

Break Generation and Detection
Interrupt on Parity, Overrun, or Framing Error (vector or non-vector)

## SYNCHRONOUS OPERATION

MONOSYNC, BISYNC, AND EXTERNAL SYNC OPERATION

Sync Characters: 8 or 16 bits
CRC Generation and Checking (CRC-16 or CRC-CCITT)
Automatic Sync Insertion

HDLC AND SDLC OPERATION

Abort Sequence Generation and Detection
Automatic Zero Insertion and Detection
CRC Generation and Checking
I-Field Residue Handling

## BAUD RATES

| FREQUENCY (KHz) (software selectable) | BAUD RATE | | | |
|---|---|---|---|---|
| | SYNCHRONOUS | ASYNCHRONOUS | | |
| | | ÷16 | ÷32 | ÷64 |
| 0.800000 | 800.00 | 50.00 | 25.00 | 12.50 |
| 1.200000 | 1200.00 | 75.00 | 37.50 | 18.75 |
| 1.758983 | 1758.98 | 109.93 | 54.96 | 27.48 |
| 2.152000 | 2152.00 | 134.50 | 67.25 | 33.62 |
| 2.400000 | 2400.00 | 150.00 | 75.00 | 37.50 |
| 4.800000 | 4800.00 | 300.00 | 150.00 | 75.00 |
| 9.600000 | 9600.00 | 600.00 | 300.00 | 150.00 |
| 19.200000 | 19200.00 | 1200.00 | 600.00 | 300.00 |
| 28.743859 | 28743.86 | 1796.49 | 898.24 | 449.12 |
| 31.916883 | 31916.88 | 1994.81 | 997.40 | 498.70 |
| 38.400000 | 38400.00 | 2400.00 | 1200.00 | 600.00 |
| 57.825882 | 57825.88 | 3614.11 | 1807.05 | 903.52 |
| 76.800000 | 76800.00 | 4800.00 | 2400.00 | 1200.00 |
| 114.306976 | 114306.97 | 7144.19 | 3572.09 | 1786.04 |
| 153.600000 | 153600.00 | 9600.00 | 4800.00 | 2400.00 |
| 307.200000 | 307200.00 | 19200.00 | 9600.00 | 4800.00 |

## INTERFACES

| | |
|---|---|
| iSBX bus: | All signals compatible with Intel iSBX bus Specification No. 142686-001 |
| Serial I/O: | RS-422/RS-449 compatible |

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## CONNECTORS

| | |
|---|---|
| iSBX bus: | iSBX bus connector |
| Serial I/O: | 50 pin edge connector, 0.1" centers |

## PHYSICAL CHARACTERISTICS

| | |
|---|---|
| Width: | 3.70 in. (9.39 cm) |
| Height: | 2.85 in. (7.24 cm) |
| Depth: | 0.50 in. (1.27 cm) |

## ENVIRONMENTAL CHARACTERISTICS

| | |
|---|---|
| Operating Temperature: | 0° to 55°C (32° to 131°F) |
| Relative Humidity: | Up to 95% (non-condensing) |

## ORDERING INFORMATION

| | |
|---|---|
| MSBX-422 | Serial interface card |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

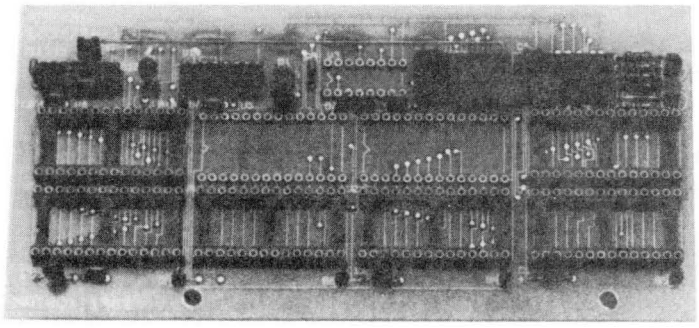
# ROM-86

## EPROM EXPANSION CARD FOR MATROX CPU BOARDS

- **Up to 512K bytes of EPROM**
- **256 bytes of on-board NOVRAM**
- **Provides eight 28-pin sockets**
- **Accomodates 8K, 16K, or 32K byte-wide EPROM parts**
- **Compatible with MBC-86/12**
- **Small size (6.3" x 3.2")**
- **Additional chip selects for double socketing**

The ROM-86 card plugs into the existing EPROM sockets of the MBC-86/12 CPU board and is mounted on two spacers. It has eight 28-pin sockets which can be configured for 8K x 8, 16K x 8, or 32K x 8 EPROMs. This gives a total of 64K, 128K, or 256K bytes of storage. Note that different sized EPROMs may not be mixed on the same card. Extra chip selects are available to allow for a second set of "piggy-back" EPROMs. This allows a total of 128K, 256K, or 512K bytes.

The ROM-86 card also has two 256 x 4 NOVRAMs for a total of 256 bytes of non-volatile static RAM. The NOVRAM is addressed as an array of I/O registers which can be written to and read from. The data is transfered to non-volatile storage by an I/O strobe and is recalled on power up or reset. The NOVRAM is very useful in graphics terminal applications having user-definable set up parameters.



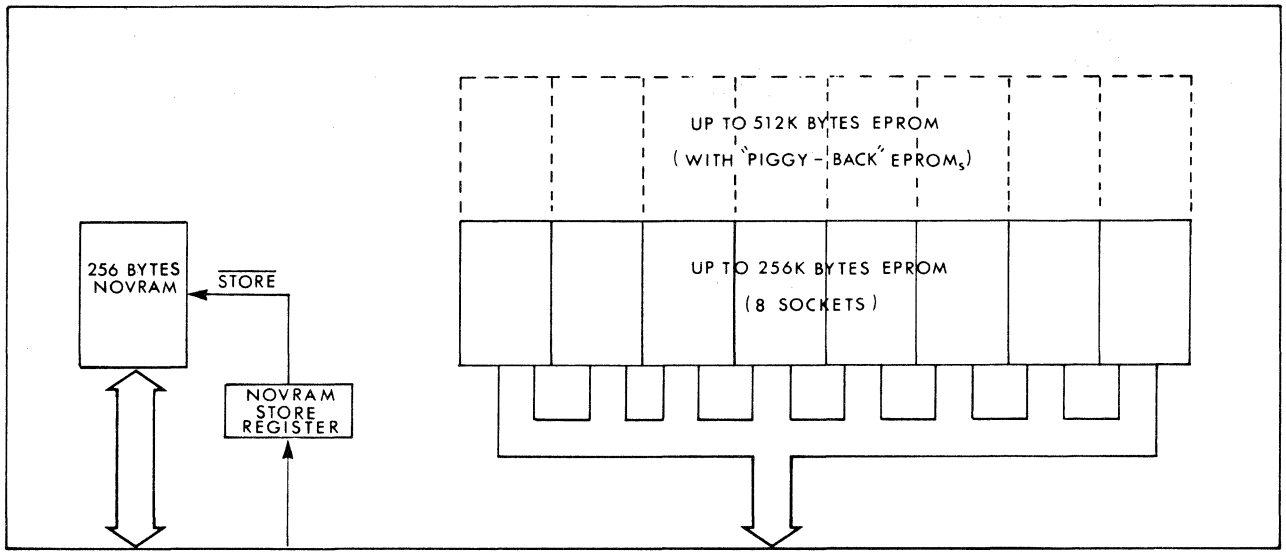



Figure 1. ROM-86 block diagram

## FUNCTIONAL DESCRIPTION

The ROM-86 is an EPROM extension board designed for the Matrox MBC-86/12 CPU board and provides up 512K bytes of non-volatile memory. With the expanded ROM capabilities provided by ROM-86, large applications programs and even sophisticated operating systems can be implemented without external storage, and without tying up the Multibus.

The ROM-86 card also contains 256 bytes of non-volatile RAM. The NOVRAM allows the user to store several key "set-up" parameters which can be modified, but which are still maintained in a power-off state.

## EPROM

ROM-86 contains 8 sockets for user installed EPROM memory. Each socket can be populated with 8K x 8, 16K x 8, or 32K x 8 (2764, 27E4, 27256) EPROMs to yield up to 256K bytes of read-only memory. This memory is electrically organized as an array of 16-bit (2 byte) words for a total of 128K words. Furthermore, extra chip select lines are provided which enable the user to "piggy-back" the memory chips and further expand EPROM capacity to a maximum of 512K bytes (256K words).

**Addressing** — MBC-86/12 allocates the top of its memory space for read-only memory (figure 2). Hardware straps, on the ROM-86 board, are provided to establish the amount of address space required as being 64K, 128K, 256K, or 512K bytes depending on the type of EPROMs being used. EPROM memory on the ROM-86 interfaces directly into the MBC-86/12 address and data bus and can only be accessed by the 8086 CPU resident on the MBC-86/12 board

## NOVRAM

ROM-86 also contains 256 bytes of non-volatile RAM (NOVRAM). This memory can be functionally viewed as two distinct memory devices (figure 3); a 256 byte static RAM array and a 256 byte Electrically Erasable PROM ($E^2$PROM) array. The static RAM behaves like a normal static read/write memory device and data transfers to and from this array require no special handling. The user communicates with the static RAM array using standard read and write commands.

The $E^2$PROM array in NOVRAM can save the contents of the static RAM array and protect this data against a "power-down" condition. A Store command copies the contents of the static RAM array to the $E^2$PROM. Note that when a Store command is executed, the contents of the

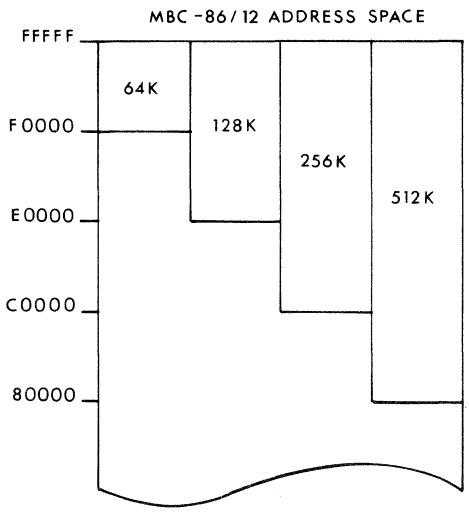



Figure 2. ROM address allocation

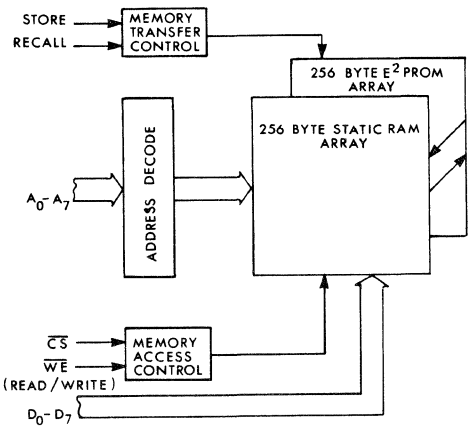



Figure 3. NOVRAM functional diagram

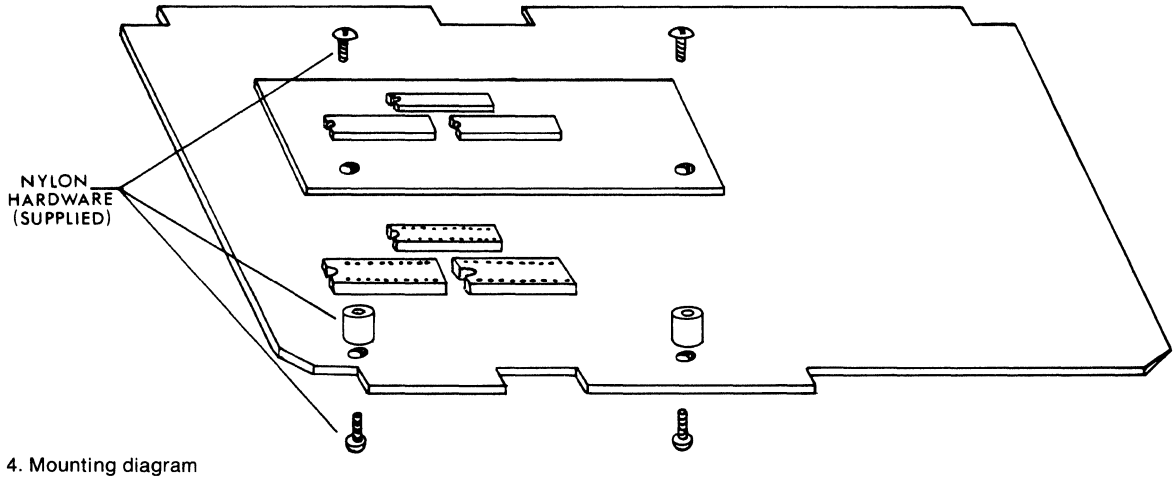



Figure 4. Mounting diagram

static RAM will "overwrite" the contents of the E²PROM and any data previously stored in E²PROM will be lost. On power-up, the contents of the E²PROM array will automatically be transferred to the static RAM and hence become available to the user. On-board straps are also available to enable the ROM-86 NOVRAM to "recall" the contents of E²PROM memory every time a Reset is executed by the MBC-86/12.

**Addressing** — The MBC-86/12 accesses the ROM-86 NOVRAM as an array of I/O locations which are positioned on I/O addresses 200H to 3FEH. Another I/O port, located at 0E0H, is used as a control register for storing data from the static RAM array to the E²PROM array. Any write access to this Control Register will initialize a Store command.

**MOUNTING**

ROM-86 is plugged directly into the MBC-86/12 and connects to the CPU card via the two empty ROM sockets and an interface socket (figure 4). The ROM-86 is then secured to the host board using two threaded nylon spacers (supplied with ROM-86). Note that the MBC-86/12 (when mounted with a ROM-86) should be installed in the topmost slot of the Multibus chassis. This is recommended since the top slot usually provides the extra room required by the piggy-back ROM board. If a lower slot is used, the slot immediately above it must be left vacant so as not to interfere with the ROM-86.

The ROM-86 card is located directly over one of the two iSBX connectors on the MBC-86/12. Full access to the second iSBX connector is still possible, as is access to the 8086 socket (for in-circuit emulator cables).

# SPECIFICATIONS

**WORD SIZE**

EPROM: 16 bits
NOVRAM: 8 bits

**MEMORY CAPACITY**

EPROM:

| | ON-BOARD MEMORY (bytes) | |
|---|---|---|
| TYPE | NORMAL | PIGGY-BACK |
| 8K x 8 | 64K | 128K |
| 16K x 8 | 128K | 256K |
| 32K x 8 | 256K | 512K |

NOVRAM: 256 bytes

**MEMORY ADDRESSING**

EPROM:

| MEMORY SIZE | ADDRESS (hex) |
|---|---|
| 64K | F0000 — FFFFF |
| 128K | E0000 — FFFFF |
| 256K | C0000 — FFFFF |
| 512K | B0000 — FFFFF |

NOVRAM: 200H — 3FEH (NOVRAM is I/O mapped)
0E0H (NOVRAM Store Register)

**PHYSICAL CHARACTERISTICS**

Width: 6.30 in. (16.00 cm)
Height: 3.20 in. ( 8.13 cm)
Depth: 0.50 in. ( 1.27 cm)

**ENVIRONMENTAL CHARACTERISTICS**

Operating Temperature: 0° to 55°C (32° to 131°F)
Relative Humidity: Up to 95% (non-condensing)

**ORDERING INFORMATION**

ROM-86-XX

{ NV — Includes 256 bytes of NOVRAM
{ No Suffix — ROM-86 without NOVRAM

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# PTB-2

## MULTIBUS WIREWRAP PROTOTYPE BOARD

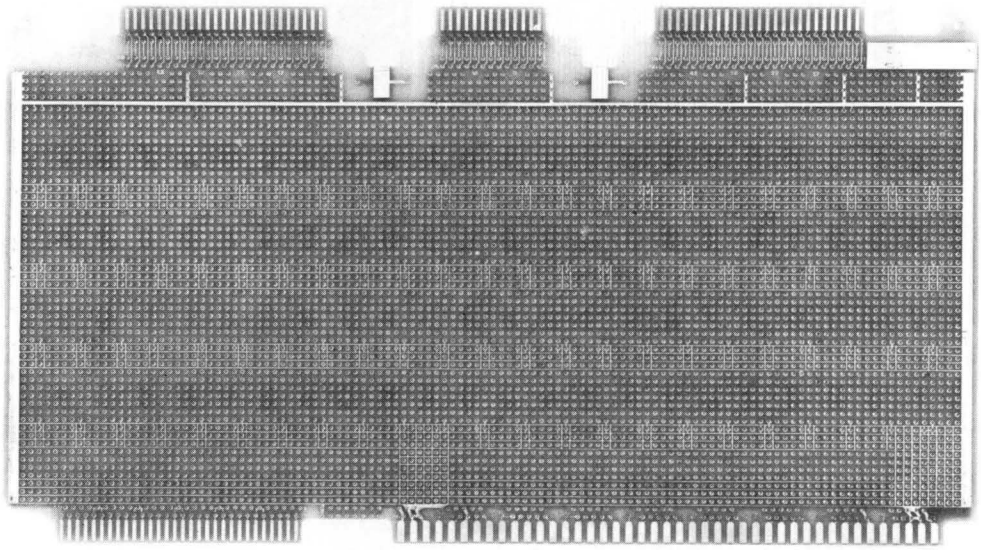
- **Holds over 120 ICs**
- **Uncommitted power supply buses**
- **Gold-plated edge connectors**
- **Plated-through holes (0.1 inch centers)**
- **Two 50 pin and one 26 pin user definable board edge connectors**
- **Multibus compatible connectors**
- **Cutouts for two BNC edgemount connectors**

The Matrox PTB-2 is a high quality wire-wrap or solder prototype board which allows the user to build his own cards. The board will hold over 120 ICs and its uncommited power supply buses allow the user maximum flexibility in IC type and placement. All PCB edge contacts are gold plated to ensure a long and trouble free life.

The top-side edge connectors are designed to provide a simple means of interfacing to serial port, parallel port, and analog I/O devices.

**ORDERING INFORMATION**

PTB-2: Wirewrap prototype board



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# BEX-1

## MULTIBUS EXTENDER BOARD

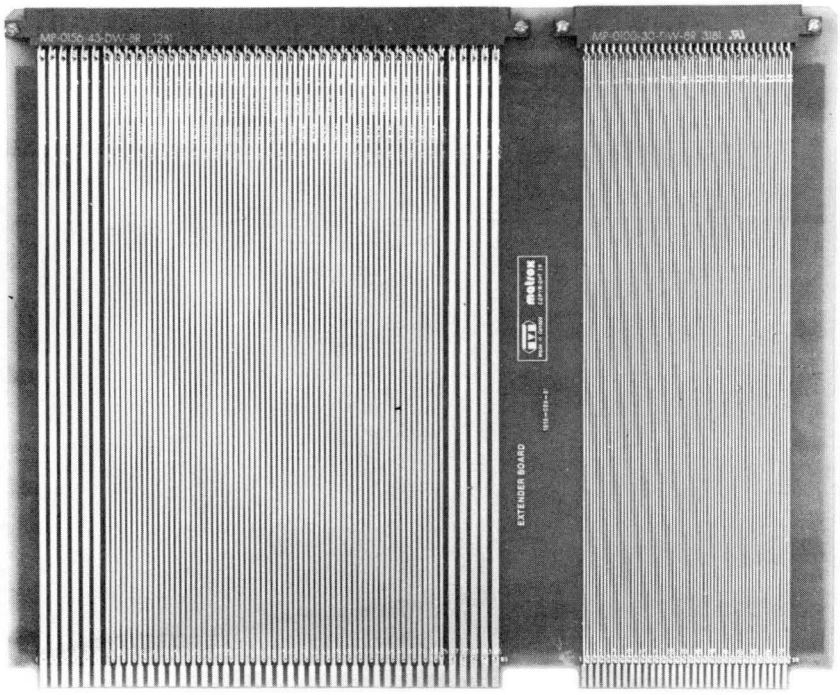
- **Numbered pins for easy identification**
- **8" card height enabling easy access to all pins**
- **Gold-plated edge connectors**
- **Multibus compatible connectors**

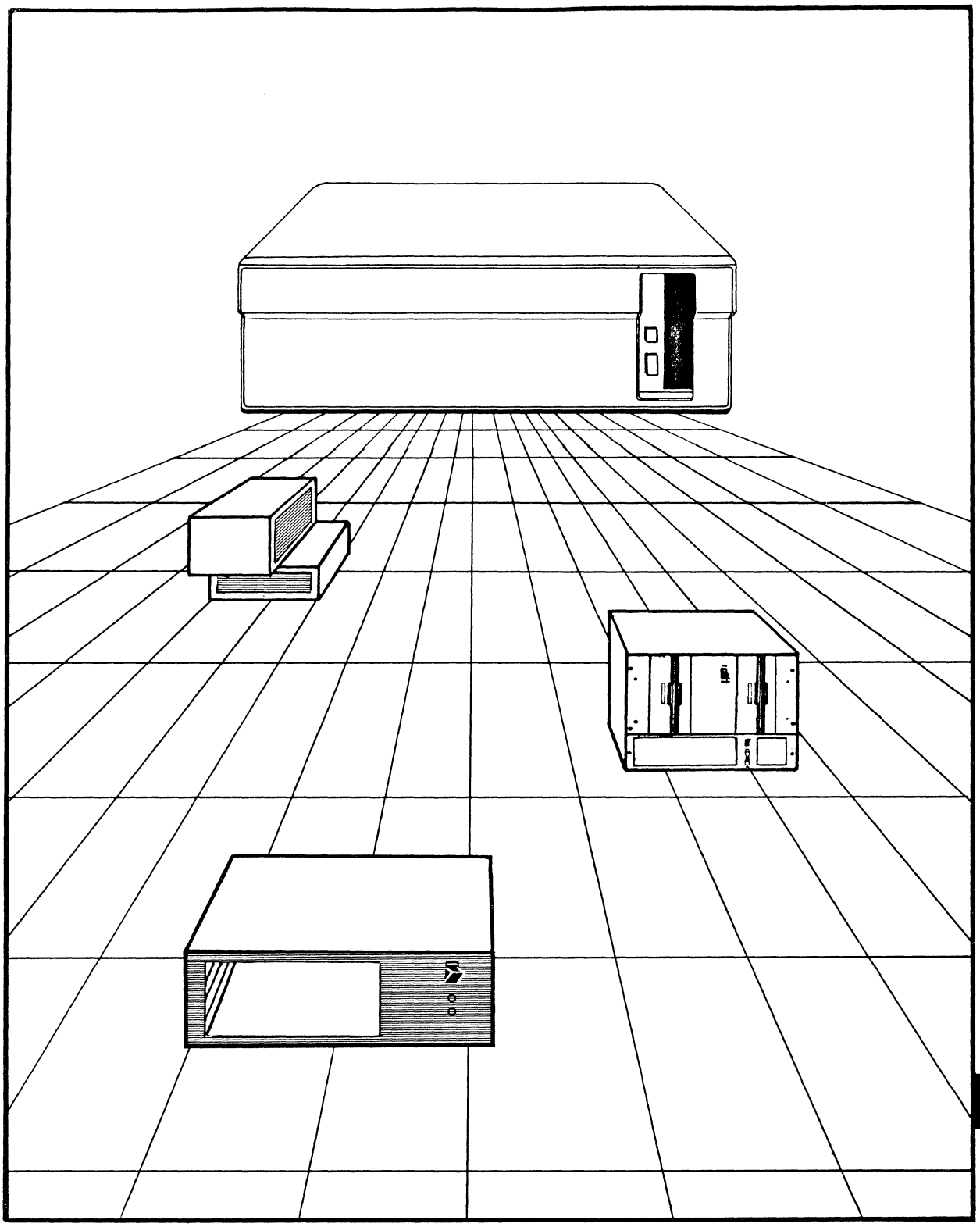
The BEX-1 extender card is used for experimenting on or trouble-shooting defective boards within the users computer system. The card has both a standard Multibus (P1) and an auxiliary (P2) connector to maintain flexibility. All pins are numbered for easy identification. To minimize cross-coupling and signal degradation, all signal lines are contained on one side of the PCB while the other side serves as a ground plane.

The BEX-1 is 8" high, enabling easy access to all pins including those on the connectors. This facilitates connection of voltmeters, logic probes, or oscilloscopes. All PCB edge contacts are gold plated to ensure a long and trouble free life.

**ORDERING INFORMATION**

BEX-1: Extender board





# CARDCAGES, DISKDRIVES AND KEYBOARDS

## SECTION 13 CARDCAGES, DISKDRIVES AND KEYBOARDS

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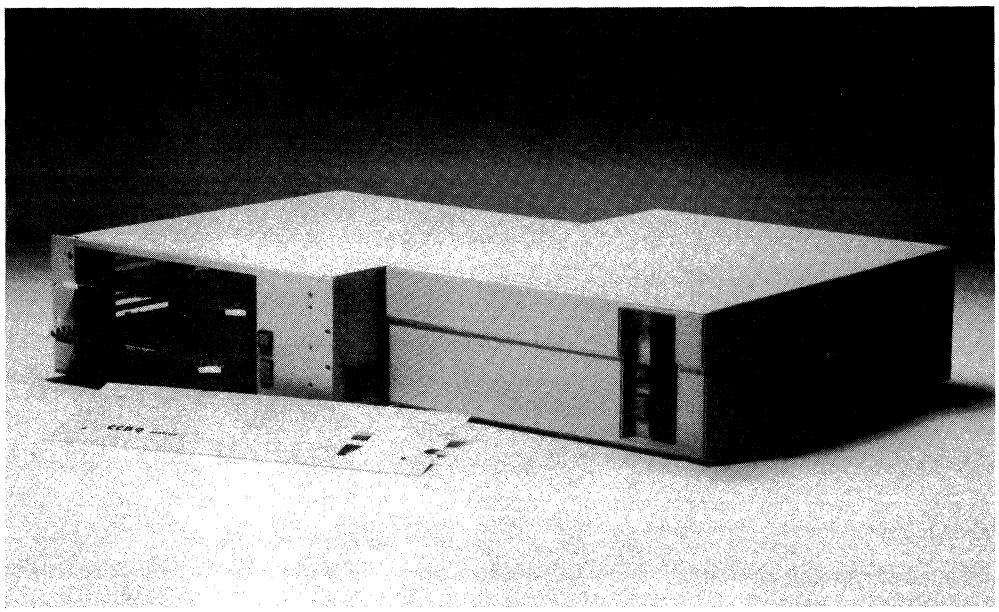
# CCB-9

## 9-SLOT MULTIBUS SYSTEM CHASSIS

- **9-slot Multibus cardcage and backplane**
- **Front loading**
- **Desktop or rackmount construction**
- **Winchester and floppy disk drive options**
- **Built-in switching power supply, 20, 40, or 60 amps**
- **Automatic power-failure detection**
- **Battery back-up with trickle charger**
- **Large custom connector panel on back**
- **Quiet force-air cooling**
- **Accomodates 50/60 Hz operation**
- **UL, CSA approved**

The Matrox CCB-9 is a 9-slot microcomputer cardcage, with a built-in Multibus backplane, designed for use in applications requiring both smart appearance and solid construction. The CCB-9 conforms to the IEEE-796 bus specifications and can accomodate any Multibus-standard card including Matrox's own wide range of Multibus compatible microcomputer boards (CPU cards, memory boards, communications controllers, graphic display controllers, etc.). Frontal access to the cardcage promotes simple board insertion and maintenance.

The CCB-9 provides many powerful features including a priority arbitrator, which resolves bus request contentions between bus masters on the Multibus, and battery back-up, for emergency back-up power during power failures. Local mass storage is available through optional 20M byte Winchester disk and 1M byte 5¼" floppy disk drives. A large connector panel on the back of the CCB-9 can be used to customize connector configurations to suit the user's specific requirements. The built-in power supplies are available for 50 Hz or 60 Hz operations and can be ordered to deliver 20, 40, or 60 amps.



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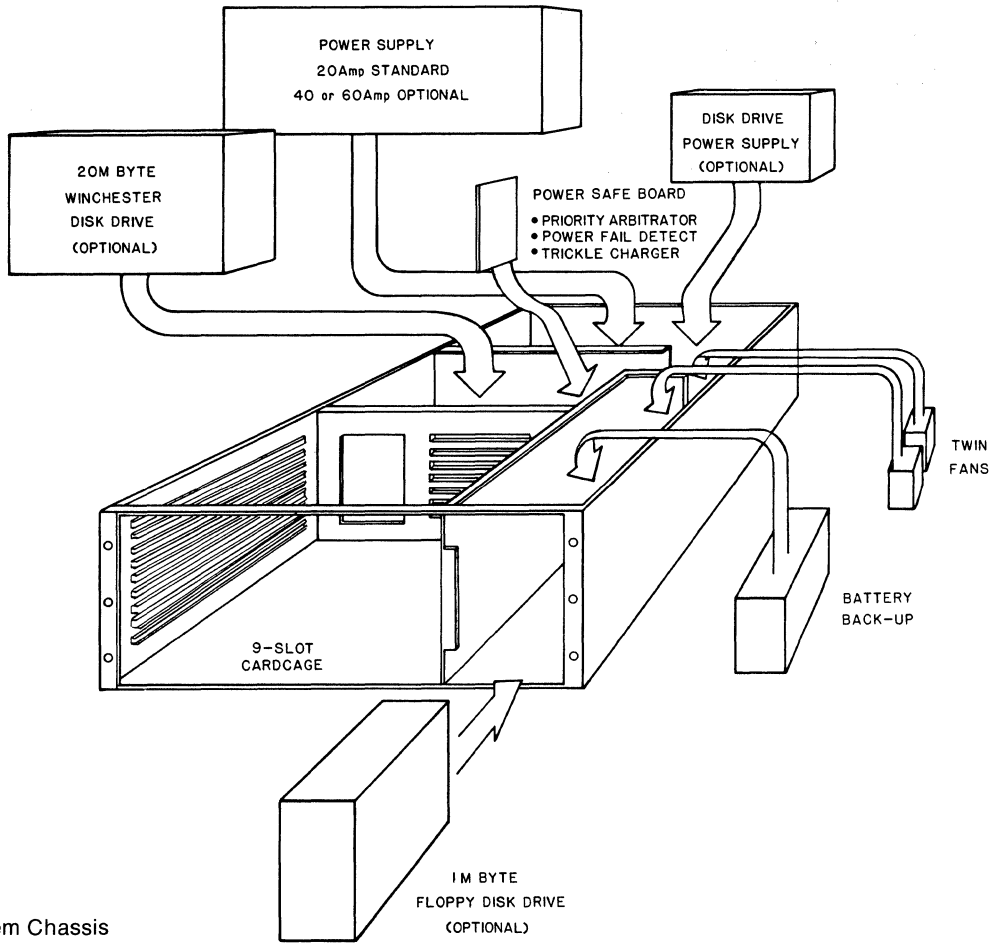


Figure 1. CCB-9 System Chassis

## FUNCTIONAL DESCRIPTION

The CCB-9 is a 9-slot system chassis based on the industry standard Multibus. Standard features of the CCB-9 include: bus request priority arbitration, power-fail detect, battery back-up, either 50 Hz (European) or 60 Hz (American) operation, and frontal loading of the Multibus cardcage. Frontal loading permits easy access to the cardcage for convenient insertion or removal of cards. The CCB-9 can be ordered as either a 19" EIA-standard rackmount or attractive desktop unit.

Optional add-ons to the CCB-9 include 21M bytes of mass memory storage and either a 40 or 60 amp switching power supply.

## POWER SAFE BOARD

A small (3" x 6") PC board contains the required circuitry for implementing the Multibus parallel priority arbitration and battery back-up. The Priority Arbitrator resolves any Multibus contentions by assigning a fixed parallel priority scheme to the Multibus backplane. Under the supplied priority schedule, card slot #1 is assigned the highest priority level and as such bus requests issued by a card residing in slot #1 will take precedence over any other bus request. The remaining priority levels are assigned to the remaining card slots in descending order (i.e. card slot #2 has priority level #2, card slot #3 has priority level #3, . . ., card slot #9 has priority level #9). The priority schedule can be changed, by the user, via a set of hardware straps. Serial priority is also supported, by the CCB-9, directly on the Multibus backplane.

A power-fail detect and battery back-up feature is also included with the CCB-9. The power-fail detect circuitry monitors the input AC line and detects a power failure if the input voltage drops below the low level voltage (105V in American systems and 210V for European systems) for more than 11 msec. On power-fail detection, the CCB-9 issues a NMI/ (non-maskable interrupt) to the Multibus and then brings the reset line (INIT/) low and holds it low until power is restored. A 5 msec. delay is implemented between NMI/ and INIT/ to allow the system CPU(s) to execute power-fail service routines. Also, on issuing INIT/, the CCB-9 activates the battery back-up supply which provides emergency power to certain system devices such as RAM memory. The duration of the back-up power is fixed at 20 minutes, however this can be varied by changing the value of the associated RC time constant on the CCB-9 Power-Safe Board.

When AC power is restored, the INIT/ line will remain low for a period of 1 second to allow for settling of any oscillations in the power supply. During normal operations the back-up battery power is restored and maintained by a trickle charger contained on the CCB-9 Power-Safe Board.

## MASS MEMORY STORAGE

A 5¼" Winchester and a 5¼" Floppy disk drive can be added to the CCB-9, as an option, to provide 21M bytes of local mass memory storage. The Winchester drive provides a maximum of 19.14M bytes (unformatted) on three double sided/double density platters. The minifloppy drive yields up to 1.0M bytes using a double sided/double density diskette.

## POWER SUPPLIES

The CCB-9 uses two independent power supplies; a switching supply which delivers +5V @ 20A and a linear supply for ±12V @ 3.4A. For systems requiring greater current ratings, the +5V switching supply can optionally be replaced by a 40 or 60 amp version. Also, when ordered with the local disk option, the CCB-9 is equipped with a separate +12V/5A supply for the drive motors.

# SPECIFICATIONS

**CAPACITY**

| | |
|---|---|
| Number of Cards: | 9 cards maximum per CCB-9 |
| Inter-Card Spacing: | 0.6" spacing (center to center) |
| Card Size: | Accepts any standard Multibus compatible cards (12" x 6.5") |

**BUS**

All address, data, and control lines supported on the CCB-9 backplane conform to the IEEE-796 (Multibus) specification.

The CCB-9 supports bus contention arbitration using either a serial or parallel priority structure. As supplied slot #1 is assigned the highest priority and slot #9 is assigned the lowest priority. The priority schedule can be changed via hardware straps.

**BATTERY BACK-UP**

A 6V, 2.6A.H. battery supplies back-up power to the system in case of power interruptions. The back-up power must be wired into the system by the user.

Power fail detection circuitry is provided which activates the battery back-up when the line power drops below 105V (210V in European systems) for more than 11 msec.

A trickle charger is included to maintain the battery during normal operation (battery on stand-by).

**DISK STORAGE**

| | | 5¼ FLOPPY DISK | | WINCHESTER |
|---|---|---|---|---|
| | | SINGLE DENSITY | DOUBLE DENSITY | |
| **CAPACITY** | Unformatted | | | |
| | per disk | 500K bytes | 1.0M bytes | 19.14M bytes |
| | per surface | 250K bytes | 500K bytes | 3.19M bytes |
| | per track | 3125 bytes | 6250 bytes | 10416 bytes |
| | Formatted | | | |
| | per disk | 409.6K bytes | 819.2K bytes | 15.0M bytes |
| | per surface | 204.8K bytes | 409.6K bytes | 2.5M bytes |
| | per track | 2560 bytes | 5120 bytes | 8.2K bytes |
| | sectors/track | 10 | 10 | 32 |
| **TRANSFER RATE** | | 125K bits/sec. | 250K bits/sec. | 5.0M bits/sec. |
| **LATENCY** | | 100 msec. | 100 msec. | 8.33 msec. |
| **ACCESS TIME** | | | | |
| | track-track | 3 msec. | 3 msec. | 2 msec. |
| | average | 94 msec. | 94 msec. | 72 msec. |
| **SETTLING TIME** | | 15 msec. | 15 msec. | 13 msec. |

**CONTROLS**

Power Switch, Reset Switch } front-mounted

**CONNECTORS**

Cut-Outs For:

16 BNC connectors
10 DB-25 connectors
2 40-pin connectors
1 50-pin connector
1 6-pin plug
1 5-pin plug

Supplied:

3 BNC connectors
1 DB-25 connectors

## COOLING

Twin "Whisper" fans (100 CFM)

## SIZE

| | RACKMOUNT | DESKTOP |
|---|---|---|
| Height | 6.969 in. (17.7 cm) | 7.0 in. (17.78 cm) |
| Width | 19.0 in. (48.26 cm) | 19.0 in. (48.26 cm) |
| Depth | 22.2 in. (56.2 cm) | 23.2 in. (58.42 cm) |

## ELECTRICAL CHARACTERISTICS

| | PS-20 | PS-40 | PS-60 |
|---|---|---|---|
| AC Input | 90-130V @ 47-63 Hz | 90-130V @ 47-63 Hz | 90-132 @ 47-63 Hz |
| | 180-260V @ 47-63 Hz | 180-260V @ 47-63 Hz | 180-264V @ 47-63 Hz |
| DC Output | +5V @ 20A | +5V @ 40A | +5V @ 60A |
| | ±12V @ 3.4A | ±12V @ 3.4A | ±12V @ 3.4A |
| | +12V @ 5A (optional supply for disk drives) | | |

## ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0° — 40°C
Relative Humidity: 0 — 90% (non-condensing)

## ORDERING INFORMATION

CCB-9-X-XX-XX XX — 9-slot Multibus cardcage

- XX: AS — 60 Hz 120V (American Standard) operation; ES — 50 Hz 230V (European Standard) operation
- XX: ND — No disk drives; 20 — 20M byte Winchester and 1M bytes Floppy disk drives
- X: 20 — 5V @ 20A power supply; 40 — 5V @ 40A power supply; 60 — 5V @ 60A power supply
- X: R — Rackmont; D — Desktop

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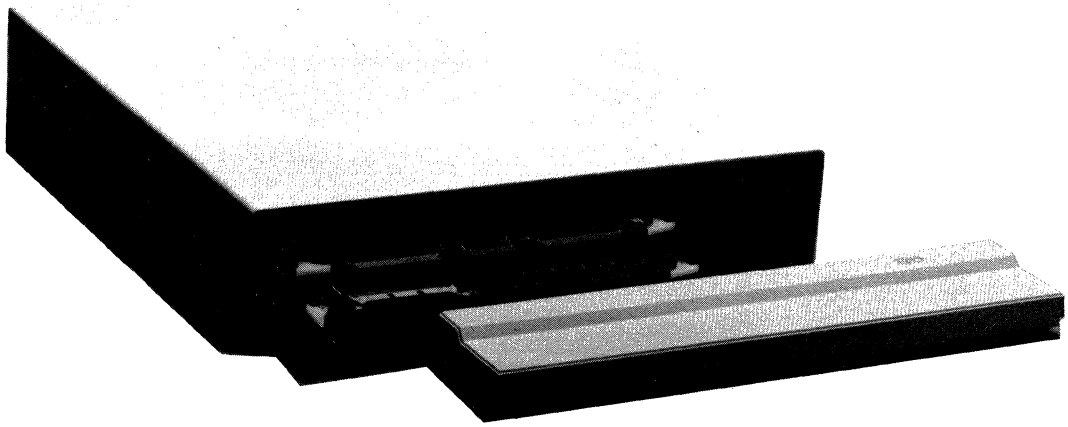
# CCB-4

## MULTIBUS DESKTOP SYSTEM CHASSIS

- **4-slot Multibus backplane**
- **Top slot is double height to accomodate iSBX Multimodules**
- **Front loading of boards**
- **Built-in switching power supply, 20A or 28A**
- **Smart appearance for office or lab**
- **Designed to serve as a base for a 19" CRT monitor**
- **UL and CSA approved**
- **Large custom connector panel on back**
- **Quiet forced-air cooling**
- **Accomodates any mains voltage**

The Matrox CCB-4 is a microcomputer chassis designed for use in applications requiring both smart appearance and solid construction. It supports all Multibus compatible cards, including Matrox's own wide range of Multibus compatible CPU boards and graphic controller boards. The CCB-4 has been designed to mate and coordinate with the Matrox KB-100 low profile keyboard. The low profile cabinet provides an excellent base for a CRT monitor, making the CCB-4 ideal for OEM graphics and alphanumerics terminal systems.



# SPECIFICATIONS

**CAPACITY**

| | |
|---|---|
| Number of Cards: | 4 cards max. per CCB-4 |
| Inter-card Spacing: | 0.6″ spacing; top card slot has 1.2″ spacing to accomodate multimodules |
| Card Size: | Accepts any standard Multibus compatible card (12″ x 6.5″) |

**BUS**

All address, data, and control lines supported on the CCB-4 backplane conform to IEEE-796 (Multibus) specifications

**CONTROLS**

Rear-mounted Power switch
Side-mounted Reset switch

**CONNECTORS**

| | |
|---|---|
| CUT-OUTS FOR: | 6 BNC connectors<br>6 DB-25 serial connectors |
| SUPPLIED: | 1 6-pin Berg serial keyboard plug (side mounted)<br>3 BNC connectors<br>1 DB-25 connector<br>1 3″ x 3.5″ blank connector plate for custom connectors |

**COOLING**

"Whisper Fan" forced-air cooled

**SIZE**

| | |
|---|---|
| Height: | 3.9 in. (10 cm) |
| Width: | 19.0 in. (48 cm) |
| Depth: | 20.0 in. (51 cm) |

**ELECTRICAL CHARACTERISTICS**

| | PS-20 | PS-28 |
|---|---|---|
| AC Input: | 90-130V 47/63 Hz<br>180-250V 47/63 Hz<br>225W (2.0A at 110VAC) | 90-132V 47/63 Hz<br>184-264V 47/63 Hz<br>340W (3.8A at 90VAC) |
| DC Output: | +5V @ 20A (switching supply)<br>±12V @ .5A (linear supply)<br>—5V @ .05A (linear supply) | +5V @ 28A (switching supply)<br>±12V @ .5A (linear supply)<br>—5V @ .05A (linear supply) |

**ENVIRONMENTAL CHARACTERISTICS**

| | |
|---|---|
| Operating Temperature: | 0-55°C |
| Relative Humidity: | 0-95% (non-condensing) |

**ORDERING INFORMATION**

CCB-4/PS-XX-XX

- XX: AS — American standard (60 Hz); ES — European standard (50 Hz)
- XX: 20 — 20A/5V power supply; 28 — 28A/5V power supply

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# CCB-7

## MULTIBUS SYSTEM CHASSIS/POWER SUPPLY

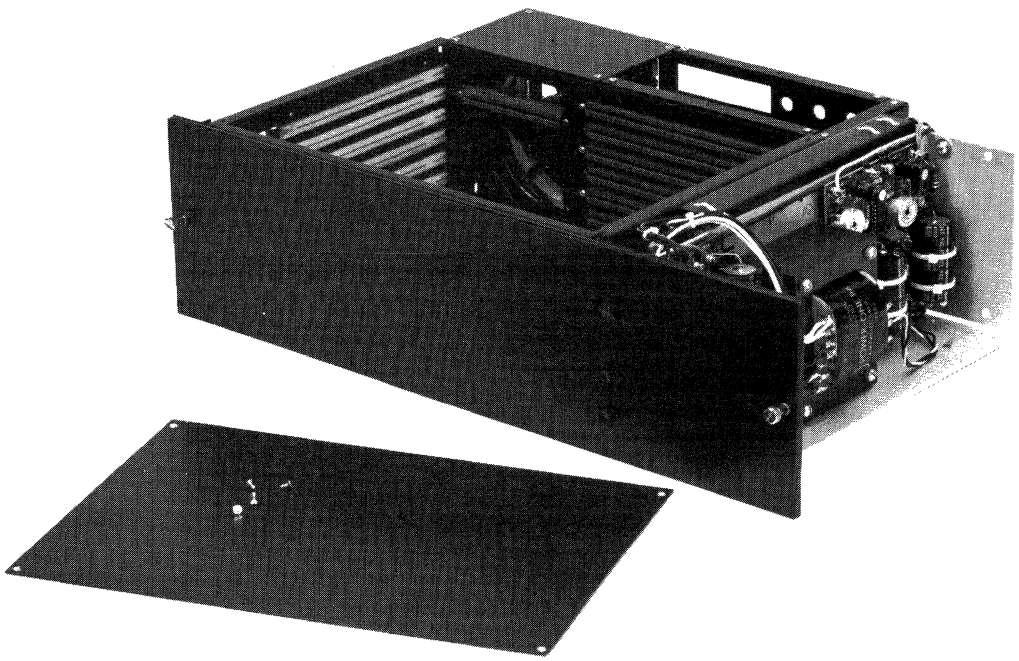
- **7-slot cardcage**
- **Expandable to 21 slots (3 x CCB-7)**
- **Multibus* backplane**
- **Only 5.25" high, EIA standard**
- **Forced air cooled**
- **Choice of three power supplies**
- **Easy frontal access to all boards**
- **User defined front panel**
- **American/European power supply standards**

The Matrox CCB-7 is a modular 7-slot cardcage with a built-in Multibus* backplane. Up to three cardcages may be stacked for systems requiring up to 21 slots. The CCB-7 is constructed adhering to EIA standard rack mount dimensions (5.25" x 19"), and it may be placed in any 19" EIA enclosure.

An increased depth allows the CCB-7 to accept cards larger than the Multibus standard size (6.75" x 12") boards. Extended size cards (up to 8.5") may be placed within the cardcage allowing for greater flexibility and performance.

The CCB-7 may be ordered with one of three available power supplies mounted within the cage. The PS-6 is a +5V/6A and ±12V/1.5A power supply whereas the PS12 features +5V/12A and ±12V/3A. For systems requiring extra power; the PS20 switching power supply supplies +5V/25A and ±12V/4A.

The CCB-7 is supplied with all connectors and card guides completely assembled.



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# SPECIFICATIONS

## CAPACITY

| | |
|---|---|
| Number of Cards: | 7 cards max. per CCB-7 (expandable to 14 or 21 by stacking cardcages) |
| Inter-card Spacing: | 0.6" spacing |
| Card Size: | Accepts any standard 12" wide Multibus compatible card (CCB-7 will accept oversize cards to a max. of 8.5" deep) |

## BUS

All address, data, and control lines supported on the CCB-7 backplane conform to Intel Multibus Specification No. 9800683.

## CONNECTORS

1 RS-232 connector (supplied standard)
2 RS-232 connectors
2 7-contact Hex connectors } (user-installed)
10 BNC connectors

## COOLING

Forced-air cooled (75 CPM capacity fan)

## SIZE

EIA standard rack mount dimensions:

| | SHORT VERSION (with PS6) | LONG VERSION (with PS12/PS20) |
|---|---|---|
| Height: | 5.25 in. (13.33 cm) | 5.25 in. (13.33 cm) |
| Width: | 19.0 in. (48.26 cm) | 19.0 in. (48.26 cm) |
| Depth: | 11.0 in. (27.94 cm) | 16.0 in. (40.64 cm) |

## WEIGHT

| | |
|---|---|
| With PS20 Supply: | 31 lbs. |
| With PS6/PS12 Supply: | 45 lbs. |

## ELECTRICAL CHARACTERISTICS

AC Input: 115/230V 47-440 Hz

DC Output:

| PS6 POWER SUPPLY | PS12 POWER SUPPLY | PS20 POWER SUPPLY |
|---|---|---|
| +5V @ 6A | +5V @ 12A | +5V @ 25A |
| −12V @ 1.5A | −12V @ 3.4A | −12V @ 4A |
| +12V @ 1.5A | +12V @ 3.4A | +12V @ 4A |

## ORDERING INFORMATION

CCB-7-XXXX-X

- A — American operation (115V 50/60 Hz)
- E — European operation (220V 50/60 Hz)

- NPS — Cardcage only, long version
- PS6 — Cardcage with PS-6 power supply
- PS12 — Cardcage with PS-12 power supply
- PS20 — Cardcage with PS-20 power supply

## SUPPORT PRODUCTS

| | |
|---|---|
| SYS-1 : | 19" rack mount cabinet for CCB-7-PS6 |
| SYS-2 : | 19" rack mount cabinet for CCB-7 (all models except PS6) |

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# KB-100

## LOW PROFILE GRAPHICS KEYBOARD

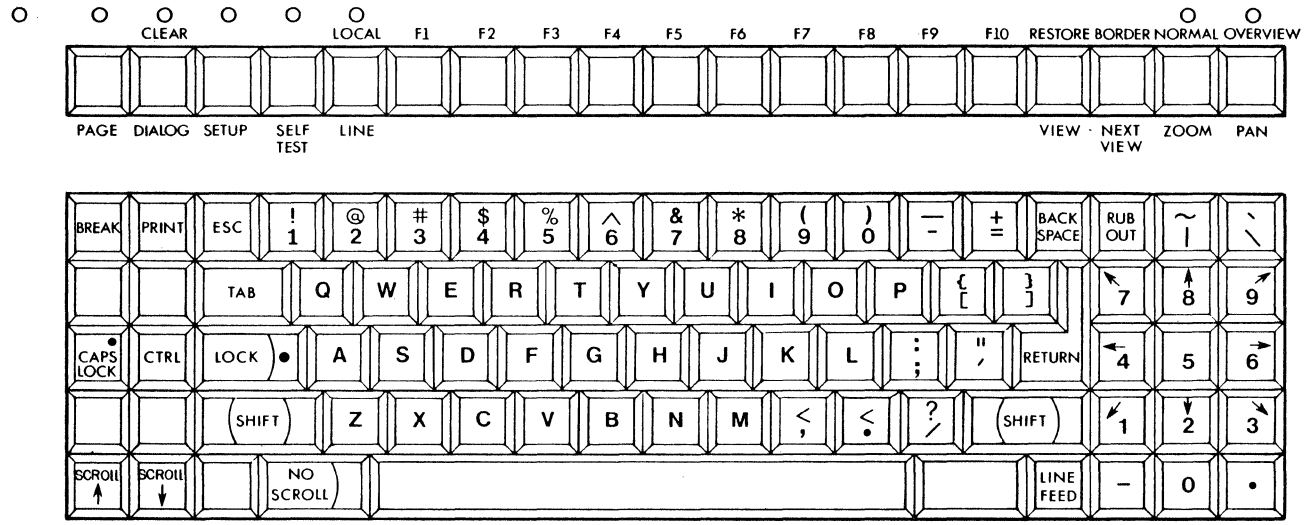
- **101 Keys**
- **Illuminated Shift Lock and Caps Lock keys**
- **18 user functions keys**
- **Numeric keypad**
- **Sculptured typing area**
- **RS-423 serial interface**
- **Detachable coiled cord**
- **8 programmable LED indicator lamps**
- **Audible bell**
- **Works with CCB-4 desktop chassis**
- **N-key rollover**
- **Stylish appearance**
- **UL, CSA approved**

The KB-100 is a serial keyboard designed to be used as an operator interface to graphics and alphanumerics terminals. The KB-100's "silent typing" feature, together with its attractive styling, make the keyboard ideal for office environments. A sculptured typing area promotes operator comfort, thus increasing data entry efficiency. N-key rollover circuitry is built into the keyboard, eliminating the possibility of missing a character during high-speed typing.

The KB-100 features an auxillary keypad which can be used for high speed numeric data entry, graphics cursor control, or other special graphics functions. Also included are 18 user definable function keys which enable the user to customize his terminal functions.

# SPECIFICATIONS

## KEYBOARD LAYOUT




## CONNECTIONS

| PIN | FUNCTION |
|---|---|
| 1 | Ground |
| 2 | +5V |
| 3 | −12V |
| 4 | RxD (Keyboard output) |
| 5 | TxC |
| 6 | TxD |

## MATING CONNECTOR

Berg #66011-002

## BAUD RATE

1200/2400/4800/9600 baud (switch selectable)

## POWER REQUIREMENTS

| | |
|---|---|
| +5V DC | 500mA |
| −12V DC | 15mA |

## DIMENSIONS

| | |
|---|---|
| WIDTH: | 19.0 in. (48.2 cm) |
| HEIGHT: | 3.9 in. ( 9.9 cm) |
| DEPTH: | 10.0 in. (25.4 cm) |

## ORDERING INFORMATION

| | |
|---|---|
| KB-100 | Serial keyboard with 8 LED indicator lamps and sonalert |

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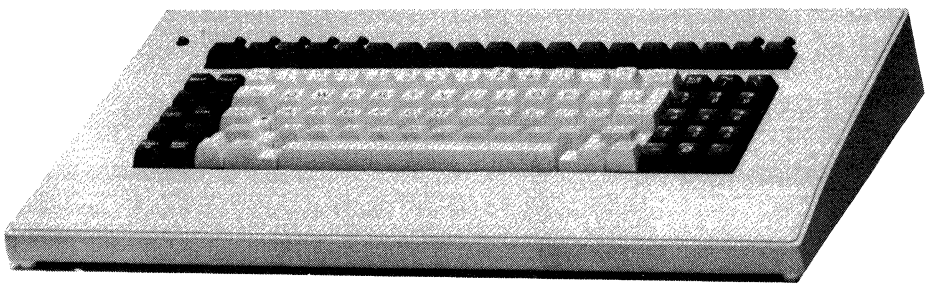
# KB-300

## PARALLEL OUTPUT SYSTEM KEYBOARD

- **101 keys**
- **Illuminated Shift Lock and Caps Lock keys**
- **18 user function keys**
- **Numeric keypad**
- **Sculptured typing area**
- **Parallel interface**
- **Works with CTM-300/R**
- **N-Key rollover**
- **Stylish appearance**
- **UL, CSA approved**

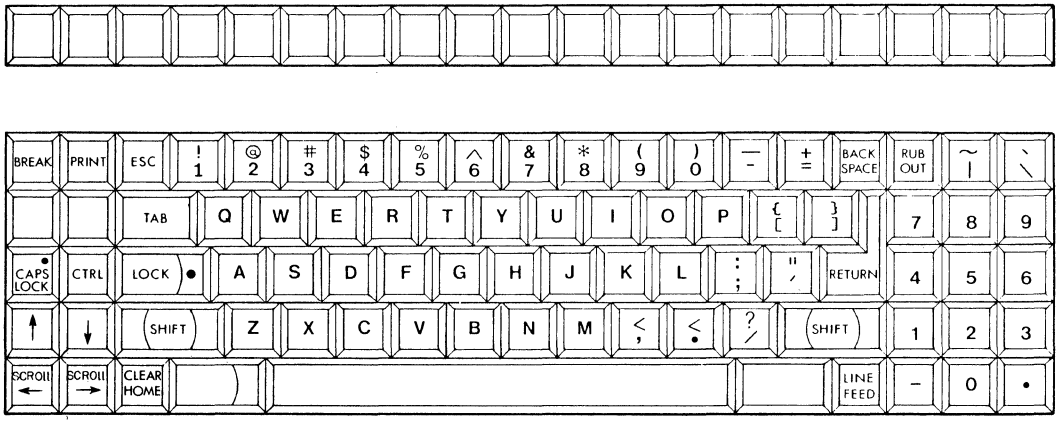
The KB-300 is a parallel keyboard designed to be used as an operator interface to graphics and alphanumerics terminals. The KB-300's "silent typing" feature, together with its attractive styling, make the keyboard ideal for office environments. A sculptured typing area promotes operator comfort, thus increasing data entry efficiency. N-key rollover circuitry is built into the keyboard eliminating the possibility of missing a character during high speed typing.

The KB-300 features a separate numeric keypad, and a row of 18 user-definable function keys.



# SPECIFICATIONS

## KEYBOARD LAYOUT




## CONNECTIONS

| PIN | FUNCTION | | PIN | FUNCTION |
|---|---|---|---|---|
| 1 | Ground | | 14 | Data Bit 6 |
| 2 | Data Bit 0 | | 15 | Ground |
| 3 | Ground | | 16 | Strobe |
| 4 | Data Bit 1 | | 17 | Ground |
| 5 | Ground | | 18 | Strobe/ |
| 6 | Data Bit 2 | | 19 | Ground |
| 7 | Ground | | 20 | Data Bit 7 |
| 8 | Data Bit 3 | | 21 | Not Used |
| 9 | Ground | | 22 | +5V |
| 10 | Data Bit 4 | | 23 | Ground |
| 11 | Ground | | 24 | +5V |
| 12 | Data Bit 5 | | 25 | Ground |
| 13 | Ground | | 26 | Not Used |

## MATING CONNECTOR

26-pin connector (Molex 15-25-4264 or equivalent)

## POWER REQUIREMENTS

+5V @ 160mA

## DIMENSIONS

Width: 19.0 in. (48.2 cm)
Height: 2.4 in. ( 6.0 cm)
Depth: 10.0 in. (25.4 cm)

## ORDERING INFORMATION

KB-300 Parallel keyboard

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

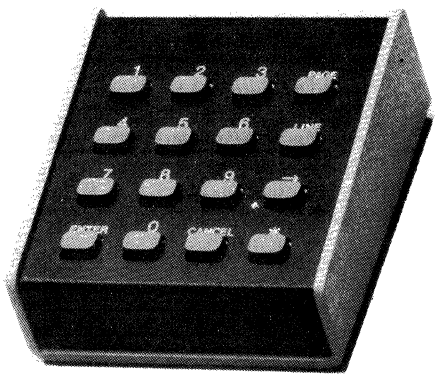
# KB-16

## DTMF KEYBOARD

- **16 keys**
- **Rugged metal case**
- **Low power requirements**
- **Attractive styling**
- **DTMF encoded output**
- **Double key lockout protection**
- **Compatible with Matrox MSBC-QV3**

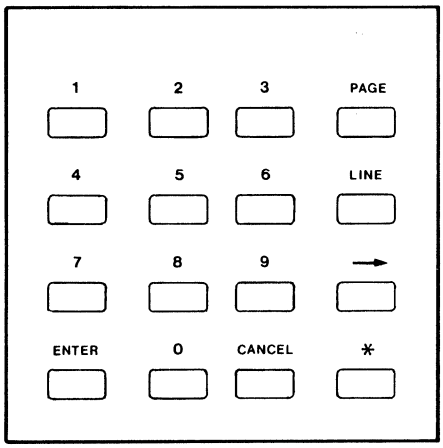
The KB-16 is a DTMF (Dual Tone Multi Frequency) keyboard designed to be used as a remote operator interface for graphics and computer systems. The KB-16 can be located several hundred feet away from the computer system.

The KB-16 is housed in a small attractive case, which fits well into an office environment. The keyboard can be interfaced to the Matrox MSBC-QV3 Multibus quad display controller which supports DTMF decoders for up to four keyboards.



# SPECIFICATIONS

## KEYBOARD LAYOUT




## CONNECTIONS

| PIN | FUNCTION |
|---|---|
| 1 | Vcc (Modulated) |
| 2 | GND |
| 3 | Shield |

## MATING CONNECTOR

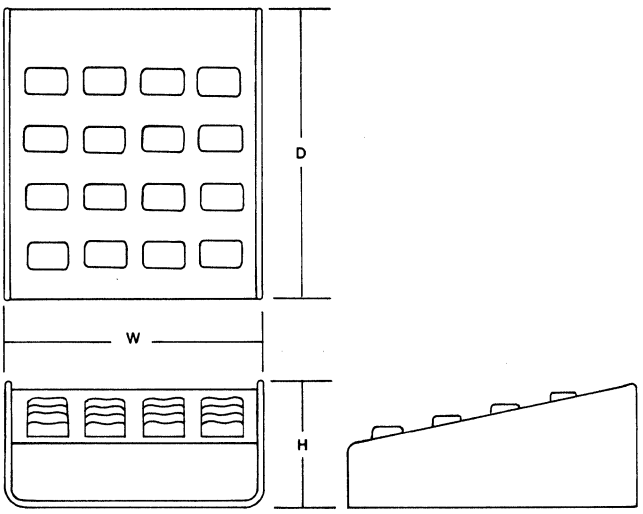
SMR-03V-B

## POWER REQUIREMENTS

+ 5V @ 5mA

## DIMENSIONS

| | |
|---|---|
| WIDTH: | 3.78 in. ( 9.6 cm) |
| HEIGHT: | 1.70 in. ( 4.3 cm) |
| DEPTH: | 4.09 in. (10.4 cm) |




## ORDERING INFORMATION

| | |
|---|---|
| KB-16 | DTMF Keyboard |

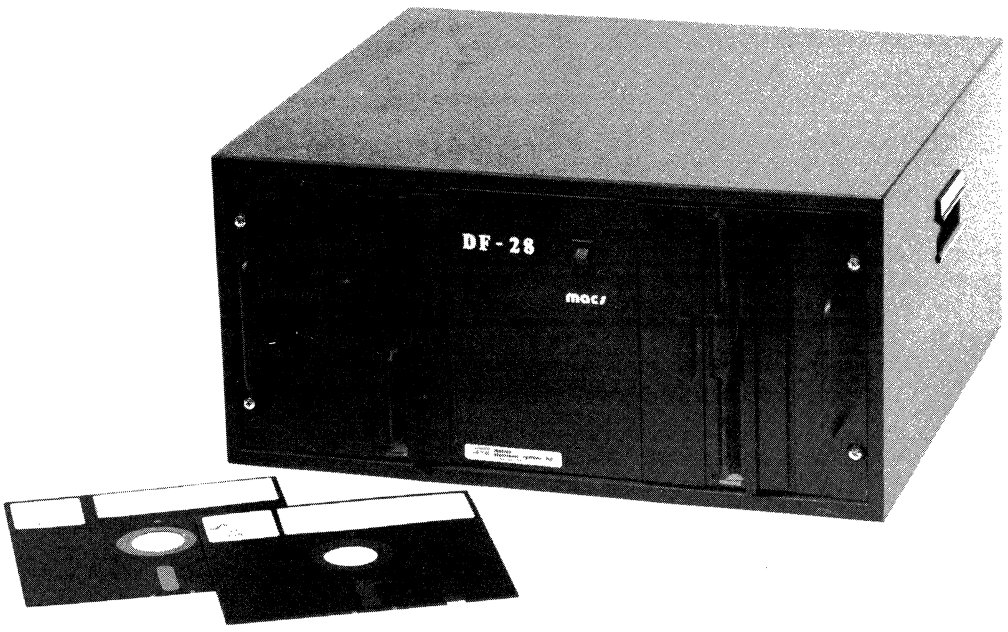
matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# DF-28

## DUAL 8" FLOPPY DISK DRIVES

- **Dual 8" drive system**
- **Shugart SA-800 or equivalent**
- **Single/double density**
- **Power supply included 50/60 Hz, 115/220V**
- **Standard EIA 19" mounting**
- **Modular, available with/without enclosure**
- **Works with FFD-1 controller**

The DF-28 is a dual 8" floppy drive unit with power supply. The drives are compatible with the Matrox FFD-1 floppy disk controller card. The modular system is supplied with chassis only to facilitate easy mounting in a 19" rack, or it can be supplied as a stand-alone desk top unit. A single 50 pin ribbon cable connects both drives to the FFD-1. The DF-28 is available in either American or European power supply versions.



# SPECIFICATIONS

| | SINGLE DENSITY | DOUBLE DENSITY |
|---|---|---|
| **CAPACITY** | | |
| Unformatted | | |
| per disk: | 3.2 megabits | 6.4 megabits |
| per track: | 41.7 kilobits | 83.4 kilobits. |
| IBM Format | | |
| per disk: | 2.0 megabits | 4.4 megabits |
| per track: | 26.6 kilobits | 45.2 kilobits |
| **TRANSFER RATE** | 250 kilobits/sec. | 500 kilobits/sec. |
| **LATENCY** (AVERAGE) | 83 ms | 83 ms |
| **ACCESS TIME** | | |
| Track to Track: | 8 ms | 8 ms |
| Average: | 260 ms | 260 ms |
| Settling Time: | 8 ms | 8 ms |
| **HEAD LOAD TIME** | 35 ms | 35 ms |
| **ROTATIONAL SPEED** | 360 rpm | 360 rpm |
| **RECORDING DENSITY** (inside track) | 3200 bpi | .6400 bpi |
| **FLUX DENSITY** | 6400 fci | 6400 fci |
| **TRACK DENSITY** | 48 tpi | 48 tpi |
| **ENCODING METHOD** | FM | MFM/$M_2$FM |

**SIZE**

| | |
|---|---|
| Width: | 19.0 in. (48.26 cm) |
| Height: | 9.7 in. (24.64 cm) |
| Depth: | 16.0 in. (40.64 cm) |

**POWER REQUIREMENTS**

| | |
|---|---|
| American: | 115V/60 Hz, 150W |
| European: | 220V/50 Hz, 150W |

**ENVIRONMENTAL REQUIREMENTS**

| | |
|---|---|
| Ambient Temperature: | 40° to 115°F (4.4° to 46.1°C) |
| Relative Humidity: | 20% to 80% |

**ORDERING INFORMATION**

DF-28-S-X

- A — American operation (115V 60 Hz)
- E — European operation (220V 50 Hz)

**SUPPORT PRODUCTS**

| | |
|---|---|
| SYS-4 : | 19" rack mount cabinet |
| RKM-1 : | Rack mount slide kit |

matrox
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TEL.: 514—735-1182 TELEX: 05-825651

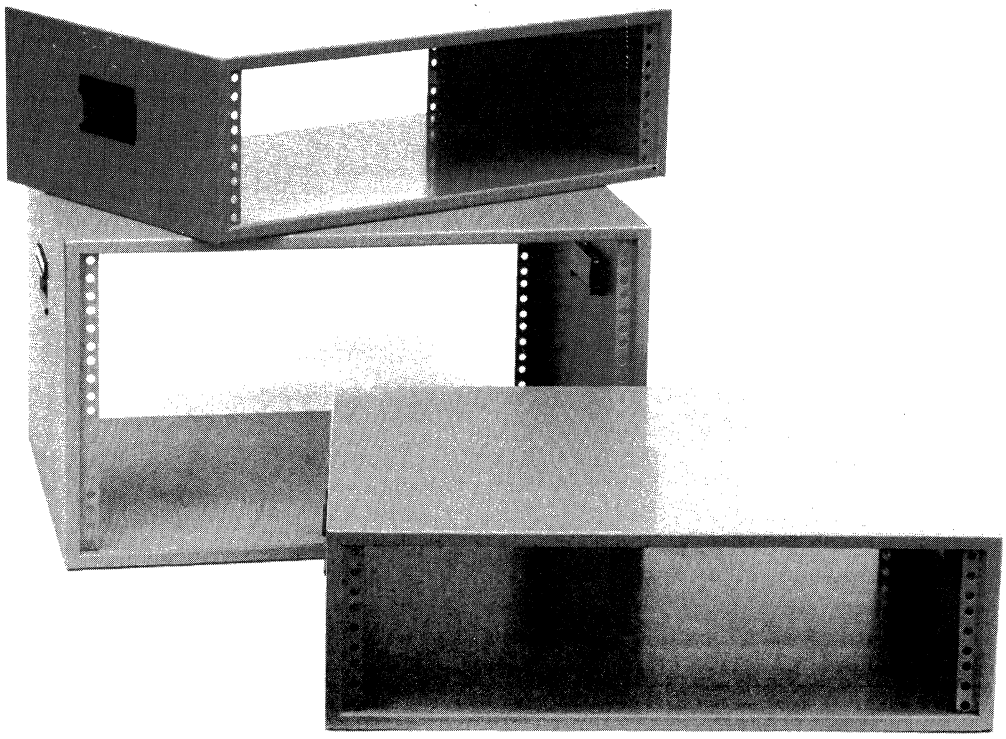
# SYS-CAB

## SYSTEM CABINETS

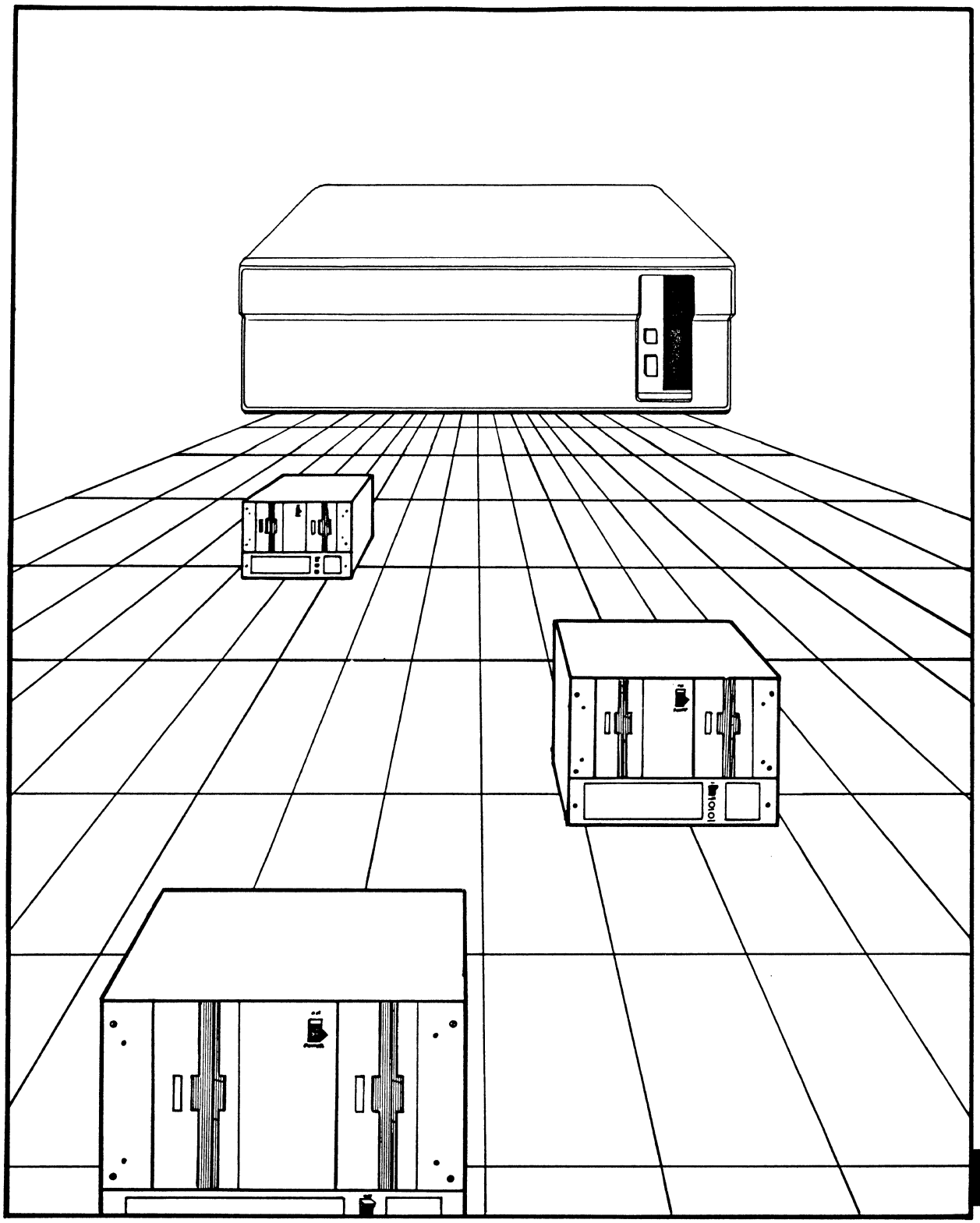
Matrox offers standard desk top enclosures for the microcomputer system designer. These modular cabinets are constructed from 18 gauge CR steel adhering to an EIA standard rack width of 19". They feature recessed side lifting grips and a flat raised bottom with rubber feet. The cabinets are painted a textured semi-gloss blue (Gulf) and all mounting hardware is included.

**ORDERING INFORMATION**

| NO. | DESCRIPTION | SIZE (IN.) | | |
|---|---|---|---|---|
| | | W | H | D |
| SYS-1 | Houses one CCB7/PS-6 cardcage | 19 | 6.25 | 13 |
| SYS-2 | Houses one CCB7/PS-12; PS-20 cardcage | 19 | 6.25 | 17 |
| SYS-3 | Houses two CCB7/PS-12; PS-20 cardcages | 19 | 11.5 | 17 |
| SYS-4 | Houses dual 8" floppy disk drives and power supply | 19 | 9.7 | 17 |
| SYS-5 | Houses one CCB7/PS-12 cardcage and dual 8" floppy disk drives with power supply | 19 | 15 | 17 |



13



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# OEM COMPUTER SYSTEMS

## SECTION 14 OEM COMPUTER SYSTEMS

matrox
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5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

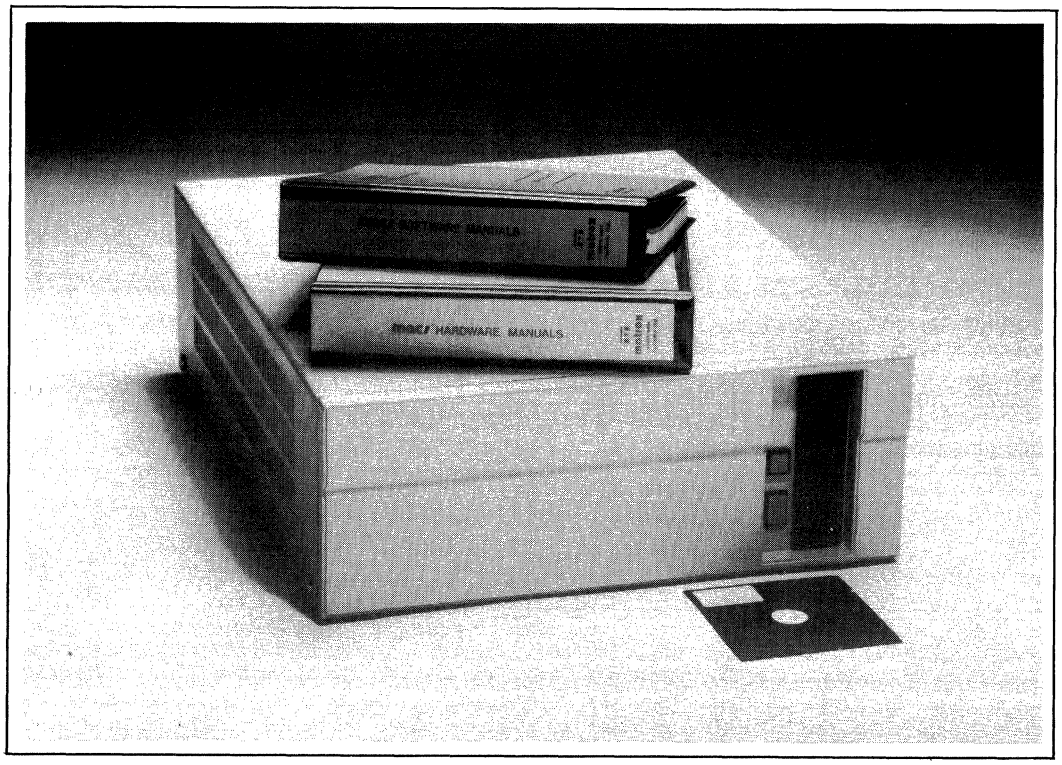
# MACS-86

## 8086 BASED MULTIBUS OEM COMPUTER SYSTEM WITH CP/M-86 DOS

- **8086 10 MHz CPU board**
- **640K bytes system RAM**
- **1MB floppy disk**
- **20MB Winchester disk**
- **9-slot card cage with power supply**
- **Desktop or rackmount chassis**
- **Equivalent to Intel system 86/330**
- **CP/M-86 or Concurrent CP/M-86 operating system**
- **Multibus architecture**
- **RS-232C terminal interface**
- **Parallel interface for printer**
- **115/230 volt, 50/60 Hz operation**
- **2 hour battery back-up for RAM**
- **Automatic power failure recovery**

The MACS-86 is a versatile OEM microcomputer system based on the industry standard 8086 CPU and CP/M-86 operating system. The system contains 640K bytes of dynamic RAM memory, a 1M byte 5¼" floppy disk drive, and a 20M byte hard disk drive. The complete electronics are contained on three Multibus boards, leaving six slots available for user expansion.

Interfaces are included for a video terminal and a line printer.




14

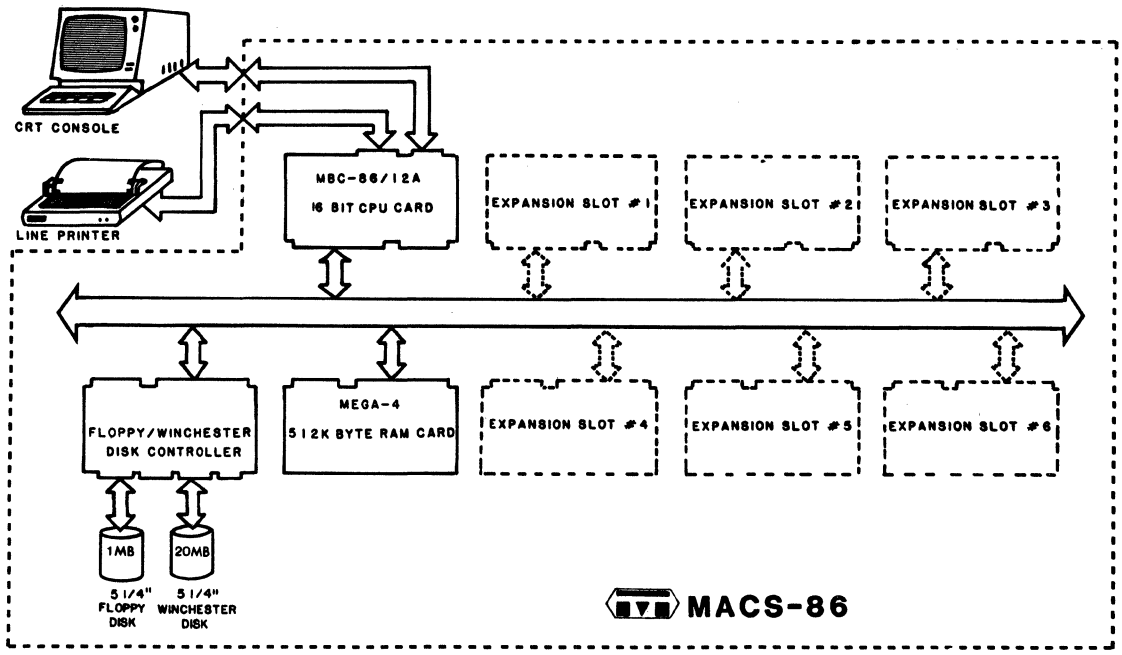



Figure 1. MACS-86 block diagram

## FUNCTIONAL DESCRIPTION

The MACS-86 is a powerful 16-bit OEM microcomputer system, based on the 10 MHz 8086 CPU, which runs under the industry standard CP/M-86 operating system. Housed within the system cabinet (rackmount or attractive desktop versions are available) are the CPU board, a combined Winchester/Floppy disk controller, and a 512K byte RAM memory board (figure 1). Also included in the MACS-86 are a 1M byte floppy disk drive and a 19M byte Winchester drive.

## CENTRAL PROCESSING UNIT

At the heart of the MACS-86 microcomputer system is the Matrox MBC-86/12A CPU board. Based on the industry standard 8 MHz 8086 16-bit central processing unit, the MBC-86/12A supplies the MACS-86 with high speed, high performance processing capabilities. Standard on-board features of the MBC-86/12A include an 8-level programmable interrupt controller, two programmable counter/timers, RAM, ROM, parallel and serial interfaces, two iSBX connectors for I/O expansion, and an 8087 coprocessor socket.

**On-Board Memory** — The MBC-86/12A contains 128K bytes of on-board dynamic RAM memory which is dual ported to permit read/write accesses from either the on-board 8086 or an external processor via the Multibus. The MBC-86/12A's on-board processor has priority over Multibus requests for access to the on-board RAM and can also "protect" any or all of this memory, from Multibus access, in 16K byte segments.

## SYSTEM MEMORY

Besides the 128K bytes of RAM on the MBC-86/12A CPU board, the MACS-86 contains a memory board (MEGA-4) which provides an additional 512K bytes of read/write system memory. The MEGA-4 features an on-board Memory Management Unit (MMU) which divides the 512K bytes of MEGA-4 memory into 8K byte blocks, and maps each of these blocks into an 8K byte block of system address space (figure 2). The Memory Management Unit also enables the user to define each 8K byte block of memory as read/write protected, read only, write only, or read/write. The user can change the memory mapping or read/write definition for any or all of the 8K byte memory blocks by simply writing to a pair of I/O registers.

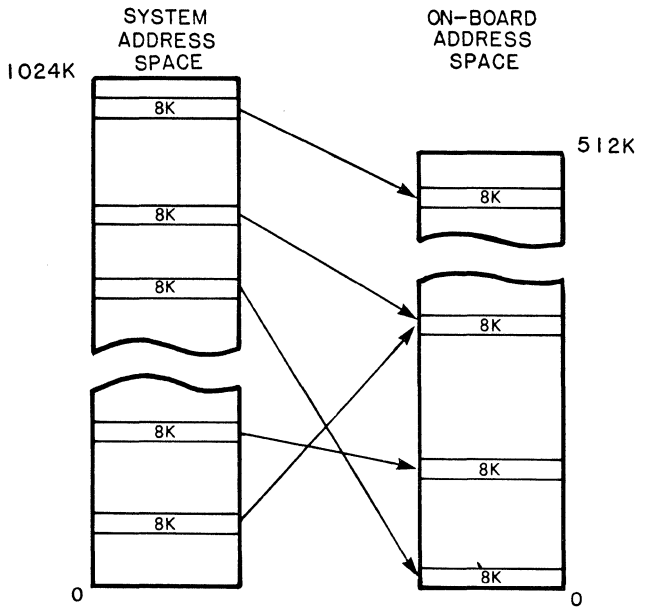



Figure 2. Memory Management Unit

The MEGA-4 has on-board parity generation and checking, which ensures the validity of data transfers from the memory board. On parity error (the MEGA-4 uses an odd parity scheme), an interrupt is issued.

## BATTERY BACK-UP

The contents of the MACS-86 system RAM memory (MEGA-4 and MBC-86/12A) are protected against power interruptions by a 6V, 2.6 A.H. back-up battery. If the input AC line voltage drops below a low level voltage level (105V for American systems and 210V for European systems) for more than 11 msec., the Power Fail Detect circuitry informs the 8086 CPU of an impending power failure and activates the back-up supply. The back-up battery power is maintained, during normal operations, by an integral trickle charger.

**Power Fail Recovery** — The MACS-86 has an automatic power-fail recovery feature usually found only in mainframe and supermini computers. When an advanced power fail detect interrupt occurs, the CPU saves all internal register contents and activates a back-up supply for RAM. When line power is restored, the CPU will reinitialize all registers and continue at the point of power interruption.

### DISK CONTROLLER

A mass storage controller board is supplied with the MACS-86 to provide high speed DMA transfers between the system bus and the integral mass storage devices. A pipelined hardware architechture permits high data throughput and an on-board dual-ported 4K byte RAM buffer allows a full track of data to be read in one disk rotation. A proprietary error correction chip is incorporated on the disk controller board which can generate both Winchester ECC and CRC codes for the floppy disk. When disk data is read, this error correction chip will detect error bursts of up to 22 bits in length and will correct up to 11 bits. If "hard errors" are detected on a disk track (attempts to re-read data fails to produce correct data), an alternate track address is written on the bad track's ID sector header. This alternate track address acts as a pointer to an alternative track during all subsequent disk operations. The controller automatically seeks an alternate track whenever a bad track is encountered. The disk controller is capable of controlling two 5¼" Winchester drives (ST506 or equivalent) and two 5¼" floppy disk drives (SA460 or equivalent).

### DISK DRIVES

The MACS-86 incorporates a 5¼" floppy disk drive and a 5¼" Winchester disk drive providing a total of 20M bytes of formatted mass memory storage. The Winchester drive supplies 19.14M bytes of mass storage on three double sided/double density platters. The drive has an average access time of 72 msec. and a transfer rate of 5.0M bits/second. The floppy disk drive is a 1.0M byte double sided/double density unit which has an average access time of 94 msec. and a data transfer rate of 250K bits/second. This drive can be used for both data storage and system back-up.

### CONSOLE INTERFACE

The MACS-86, as supplied, supports a serial interface for a standard ASCII CRT console device. This port is wired as a data set modem and supports TxD, RxD, CTS, DTR, and DSR lines compatible with the EIA-RS-232C serial interface specification. The console interface is implemented using a programmable communications controller on the MBC-86/12A board, which is initialized by a ROM monitor program (see MON-86/12). The serial interface is accessed via a standard DB-25 connector located on the back panel of the system chassis.

### PRINTER INTERFACE

The parallel port on the MBC-86/12A CPU board is initialized, by the CP/M-86 operating system, as an interface to any Centronics compatible printer. A negative going software strobe is used to transfer data to the printer when the BUSY line is low. A edge connector and wiring harness connect printer data from the MBC-86/12A to a DB-25 connector on the back panel of the system chassis.

### SOFTWARE

The MACS-86 is supplied with a comprehensive software package which includes the industry standard CP/M-86 Operating System, a ROM-based monitor program for the MBC-86/12A CPU board (MON-86/12), and diagnostics routines for system debugging (TESTMACS-86).

**CP/M-86** — The powerful CP/M-86 Operating System, supplied with the MACS-86, contains all of the facilities of the popular CP/M 8-bit Operating System with additional features to account for increased processor address space of up to one megabyte of main memory. CP/M-86 also takes advantage of the static relocation capabilities inherent in the 8086 processor. Concurrent CP/M-86 is also available as an option with the MACS-86 system.

The MACS-86 CP/M-86 Operating System is supported by a number of utility programs such as ED, PIP, STAT, FORMAT, and SUBMIT which operate in the same way as the equivalent routines under CP/M. Also, ASM-86 allows assembly language programming and development for the 8086 and DDT-86 provides debugging of 8086 machine code.

**MON-86/12** — The MBC-86/12A CPU board contains an on-board ROM-based monitor program. On reset, the MON-86/12 monitor is used to determine and match the baud rate of the console device, to establish serial communications. Succeeding this, MON-86/12 will then either boot CP/M-86 (if a formatted disk is present in drive A) or display the prompt character "." on the console device and wait for a command to be typed. MON-86/12 supports an 18 instruction command set which permits the user to perform such functions as: Compare two memory blocks, Display the contents of a memory block, Find a match in a memory block, Execute a program, Examine and modify registers, and Input or output data from/to an I/O port. MON-86/12 also provides the power fail recovery service routines.

**TESTMACS-86** — TESTMACS-86 is a diagnostics program designed to isolate problems in the MACS-86. It allows the user to test the disk subsystems, the system RAM, the printer port interface, and the console interface. If a problem is encountered by the disk or memory tests, an error message will be displayed. TESTMACS-86 also keeps two sets of tables for recording errors. The user can display these tables at any time.

### BUS COMPATIBILITY

The Matrox MACS-86 implements the industry standard Multibus (IEEE-796). The Multibus enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. MACS-86 supports two modes of priority arbitration; serial and parallel. As supplied, the MACS-86 uses parallel priority arbitration with a fixed priority scheme which assigns the top card slot as priority level #1, slot #2 as priority level #2, slot #3 as priority level #3, ... , and slot #9 as priority level #9. The priority schedule can be changed by the user via a set of hardware straps.

### SYSTEM EXPANSION

The MACS-86 system chassis (CCB-9) contains 9 slots of which only three are used in the basic system configuration. The other six slots are available for adding on additional boards for increased versatility. Matrox supports a full line of alphanumeric and graphic video boards that can be incorporated into the MACS-86 to add computer generated display capabilities. Additional system memory can be added to the MACS-86 by plugging in more Matrox MEGA-4 memory boards for up to 2M bytes of RAM.

The I/O capabilities of the CPU board can be expanded via the two iSBX Multimodule sockets. Matrox supports a number of Multimodules including a dual RS-232C/RS-423 serial interface module (MSBX-423), an RS-232C/RS-422 serial interface (MSBX-422), and a high resolution color graphics CRT controller module (MSBX-800), which fit in these sockets. A numerical coprocessor (8087) can be plugged into the MBC-86/12A CPU's coprocessor socket to add floating point capabilities.

A large variety of CP/M-86 software packages are current available. High level languages include; FORTRAN, COBOL, BASIC, PASCAL, and C. Moreover, numerous applications packages are available from a variety of sources. Matrox supports a number of software packages designed to work with the Matrox video boards.

# SPECIFICATIONS

**HOST PROCESSOR (MBC-86/12A)**

| | | | |
|---|---|---|---|
| CPU | 8086, 10 MHz | CYCLE TIME | 250ns (min.) |
| WORD SIZE — instructions | 8, 16, 24, 32 bits | ON-BOARD MEMORY — RAM | 128K bytes |
| — data | 8, 16 bits | — ROM | 4K bytes (MON-86/12 monitor) |
| — address | 20 bits | | sockets for up to 32K bytes |

**MEMORY BOARD (MEGA-4)**

| | |
|---|---|
| WORD SIZE | 8, 16 bits |
| CYCLE TIME | 725ns |
| ON-BOARD MEMORY | 512K bytes |

**DISK CONTROLLER (DSD-5215)**

DISK FORMAT

| | FLOPPY DISK | | | WINCHESTER | | | |
|---|---|---|---|---|---|---|---|
| bytes/sector | 256 | 512 | 1024 | 128 | 256 | 512 | 1024 |
| sectors/track | 16 | 8 | 4 | 54 | 31 | 17 | 9 |

**DISK STORAGE**

| | FLOPPY DISK | WINCHESTER |
|---|---|---|
| CAPACITY Unformatted | | |
| per disk | 1.0M bytes | 20.0M bytes |
| per surface | 500K bytes | 5.0M bytes |
| per track | 6250 bytes | 10416 bytes |
| Formatted | | |
| per disk | 655.4K bytes | 17.7M bytes |
| per surface | 327.7K bytes | 4.4M bytes |
| per track | 4096 bytes | 9.2K bytes |

**SOFTWARE**

| | | | | | |
|---|---|---|---|---|---|
| MON-86/12 | — media | ROM | TESTMACS-86 — media | | double density diskette |
| | — function | MBC-86/12A monitor | | — function | system diagnostics program |
| CP/M-86 | — media | double density diskette | | | |
| | — function | disk operating system | | | |

**BUS COMPATIBILITY**

All control, address, and data lines conform to Multibus (IEEE-796) specifications.

**ADDRESSING**

| | MEMORY | I/O |
|---|---|---|
| MBC-86/12A RAM | 00000H — 1FFFFH | 00C0H — OOFFH |
| MEGA-4 RAM | 20000H — 9FFFFH | 0078H — 0079H |
| MON-86/12 ROM | FF000H — FFFFFH | 00B0H |

**SIZE**

| | | | |
|---|---|---|---|
| Width: | 19.0 in. (48.26 cm) | Depth: | 23.2 in. (58.42 cm) |
| Height: | 7.0 in. (17.78 cm) | Weight: | 60.0 lb. (27.27 kg) |

**POWER REQUIREMENTS**

115V/60 Hz @ 120W
220V/50 Hz @ 120W

**POWER SUPPLIES AVAILABLE FOR EXPANSION**

| SUPPLY | CURRENT DRAWN BY MACS-86 | CURRENT AVAILABLE FOR EXPANSION |
|---|---|---|
| +5V | 10.7A | 29.3A |
| +12V | 825mA | 2.57A |
| −12V | 90mA | 3.31A |

**ENVIRONMENTAL REQUIREMENTS**

| | |
|---|---|
| Operating Temperature: | 0°C — 50°C (dual fans included) |
| Relative Humidity: | 95% non-condensing |

**ORDERING INFORMATION**

MACS-86/X/XX — 16-bit OEM microcomputer (specify CP/M-86 or Concurrent CP/M-86 operating system)

- X: AS — American standard (60 Hz); ES — European standard (50 Hz)
- X: R — Rackmount chassis; D — Desktop chassis

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

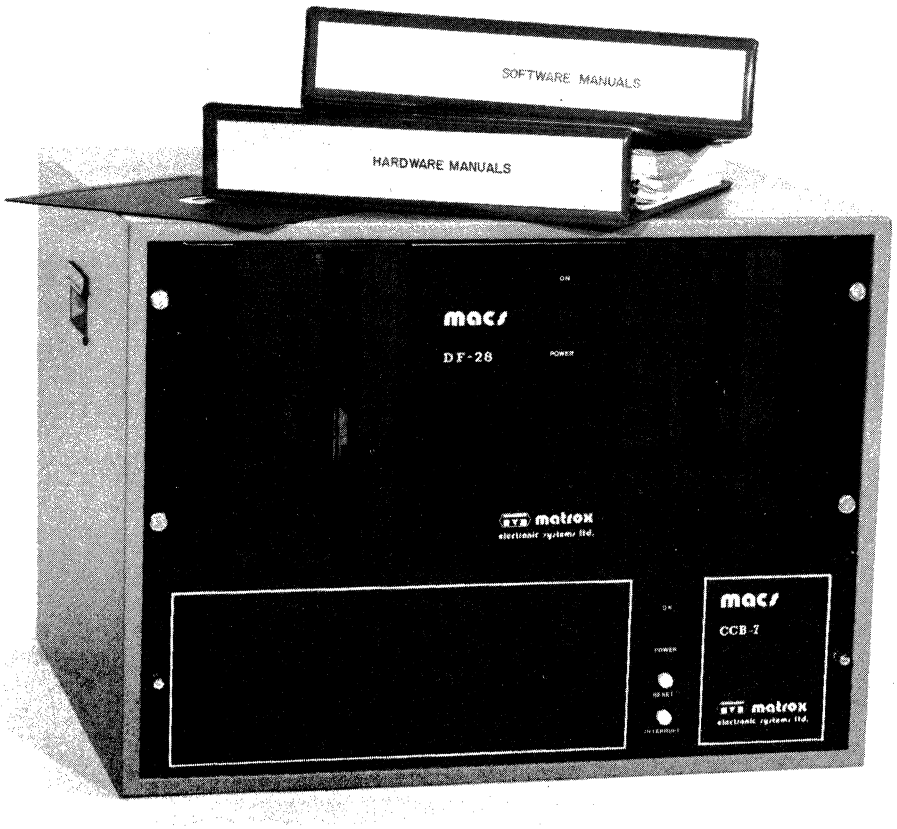
# MACS-10

## Z-80 BASED MULTIBUS COMPUTER SYSTEM

- **Z-80 based CPU board**
- **64K RAM**
- **Floppy disk controller**
- **Dual 8" floppy disk drives**
- **7 slot card cage with power supply**
- **CP/M 2.2 operating system**
- **Multibus architechture**
- **RS-232C terminal interface**
- **Parallel interface for printer**
- **115/230 volt, 50/60 Hz operation**

The MACS-10 is a powerful OEM computer system based on the Z-80 (4MHz) CPU. The hardware runs under the CP/M 2.2 disk operating system software. All hardware is contained on two Multibus cards (ZBC-80 and FFD-1). Five card slots are available for system expansion. The system contains 64K bytes of RAM as well as sockets for up to 40K bytes of ROM/EPROM. A 2K monitor program, dual 8" floppy disk drives with controller, and interfaces for a video terminal and line printer are also included.

Applications for the MACS-10 system range from software development systems to OEM computers as part of larger systems where modularity, low cost, and high performance are called for. Applications software, compatible with the industry standard CP/M operating system, is available from a wide range of vendors.

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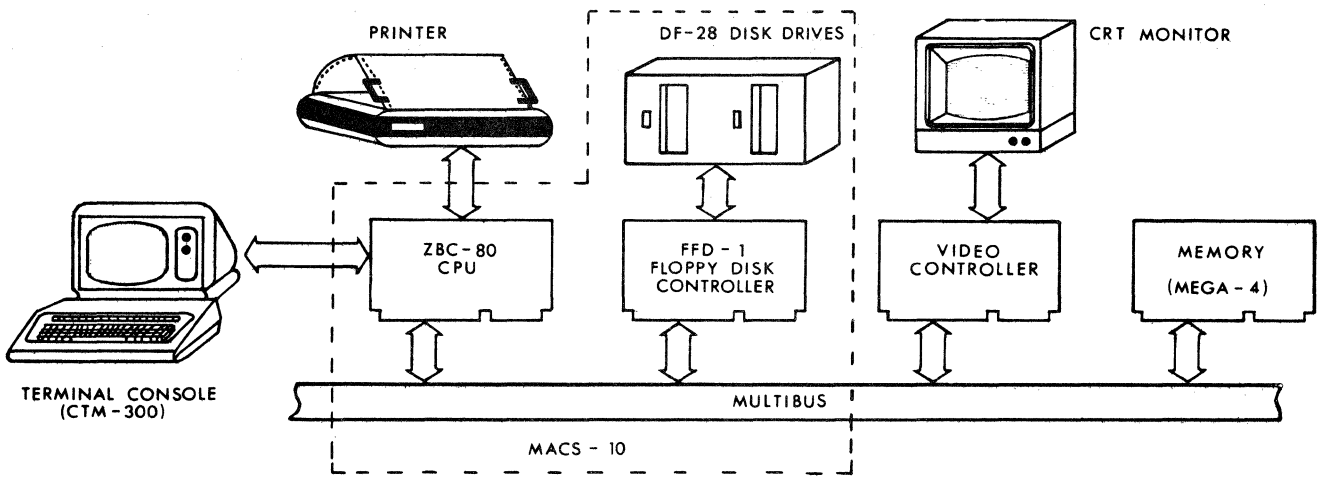


Figure 1. MACS-10 block diagram

## CENTRAL PROCESSING UNIT

The MACS-10 is based on the Matrox ZBC-80 single board computer which utilizes a 4MHz Z-80A CPU. The ZBC-80 card contains an advanced chip set to provide a high throughput in a real-time processing environment. Using the ZBC-80, the MACS-10 boasts such features as user programmable interrupts, timers, and I/O interfaces. In addition an optional dedicated arithmetic co-processor chip can be plugged in to the ZBC-80 to provide efficient high-speed number crunching without tying up the resources of the master CPU.

The ZBC-80 contains 64K of on-board dynamic RAM. This on-board RAM does not require the insertion of wait states and thereby increases system throughput by as much as 20%. A 2K byte ROM monitor (MONTRAX), with CP/M bootstrap loader, is also supplied on-board the ZBC-80 and 4 sockets are provided for additional ROM/EPROM.

## DISK CONTROLLER

A Floppy Disk Controller card (FFD-1) is supplied with the MACS-10 to provide a means of communication between the disk drives and the system bus. The FFD-1 utilizes a state of the art chip set which puts virtually all operational parameters under user software control. Recording formats can be programmed for IBM 3740 (FM) single density and IBM System 34 (MFM) double density. Non-standard sector lengths of 512 and 1024 bytes can also be used. A powerful command set is supported by the FFD-1 which includes single/multiple sector read and write.

## DISK DRIVES

The MACS-10 incorporates the Matrox DF-28 which contains two 8" floppy disk drives. Each drive can be assigned to operate using either single or double density recording formats. The DF-28 provides the MACS-10 with up to 3.2 Megabytes (double sided/double density) of mass storage with a data transfer rate of 500 Kilobits per second. Furthermore, using the FFD-1, the MACS-10 is capable of supporting a second set of dual disk drives for up to 6.4 Megabytes of on-line storage.

## CONSOLE INTERFACE

When shipped, the ZBC-80 is wired as a data set Modem that supports (among others) the TxD, RxD, CTS, DTR, and DSR lines of an RS-232C serial interface. The serial interface is implemented using a programmable communications interface (on the ZBC-80) that is initialized by the MONTRAX monitor and is accessed via a standard RS-232 connector on the back of the system chassis.

## PRINTER INTERFACE

Two of the six ports of the ZBC-80's programmable peripheral interface are initialized by the BIOS to be a port to any Centronics compatible printer. A negative going software strobe is used to transfer data to the printer when the BUSY line is low. An edge connector and wiring harness connect printer data from the ZBC-80 to a miniature "D" connector on the back of the system chassis.

## READER/PUNCH INTERFACE

The operating system software, CP/M 2.2, contains software to control a reader/punch. The user just must install some straps and make signal interconnections to complete the interface, if a reader/punch is to be used.

## SOFTWARE

The MACS-10 is supplied with a comprehensive set of software, including the ZBC-80 monitor program (MONTRAX) and the CP/M 2.2 disk operating system. A system test program, TESTMACS, is also included.

MONTRAX is supplied as firmware on the ZBC-80 and it comes up when the system is reset. On reset MONTRAX will first attempt to determine and match the baud rate of the console device, to establish serial communications. Succeeding this, MONTRAX will then either boot CP/M (if there is a disk present in drive 0) or display the prompt character "." and wait for a command to be typed. MONTRAX supports a 22 instruction command set which permit the user to perform such functions as: Display contents of defined memory area, Fill defined memory area with a constant, Hex math, and Input data from a defined I/O port.

The MACS-10 computer is designed to run under the CP/M 2.2 disk operating system. CP/M is comprised of four sections or operational units; BIOS, BDOS, CCP, and TPA. Through these units CP/M provides a machine level interface with the floppy disk controller, the console, and the line printer. CP/M also provides a disk management system which can find and manipulate information stored on disk. The CCP section of CP/M together with the Transient Program Area (TPA) permit the user to enter and implement commands from the console device.

TESTMACS is a disgnostics program designed to isolate problems in the MACS-10. It allows the user to test the disk system, the RAM, the printer interface, and the console interface. If a problem is encountered by the disk or memory tests, an error messge will be displayed. TESTMACS also keeps two sets of tables for recording errors. The user can display these tables at any time.

## BUS COMPATIBILITY

The Matrox MACS-10 implements the industry standard Multibus. Multibus enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by the independently derived bus clock signal. Figure 2 shows how the MACS-10 memory and I/O maps are organized.

## SYSTEM EXPANSION

The MACS-10 system chassis (CCB-7) contains 7 slots of which only two are used in the basic system configuration. The other five slots are available for adding on additional boards for increased versatility. Matrox supports a full line of alphanumeric and graphic video boards that can be incorporated into the MACS-10 to add computer generated display capabilities. Matrox also offers a 512K byte memory board (MEGA-4) which can be plugged into the MACS-10 system chassis for increased system memory.

A large variety of CP/M compatible software packages are currently available. High level languages include; FORTRAN-80, COBOL-80, BASIC-80, and PASCAL/MT. Moreover numerous applications packages and video graphics packages are available from Matrox and any other software manufacturers.

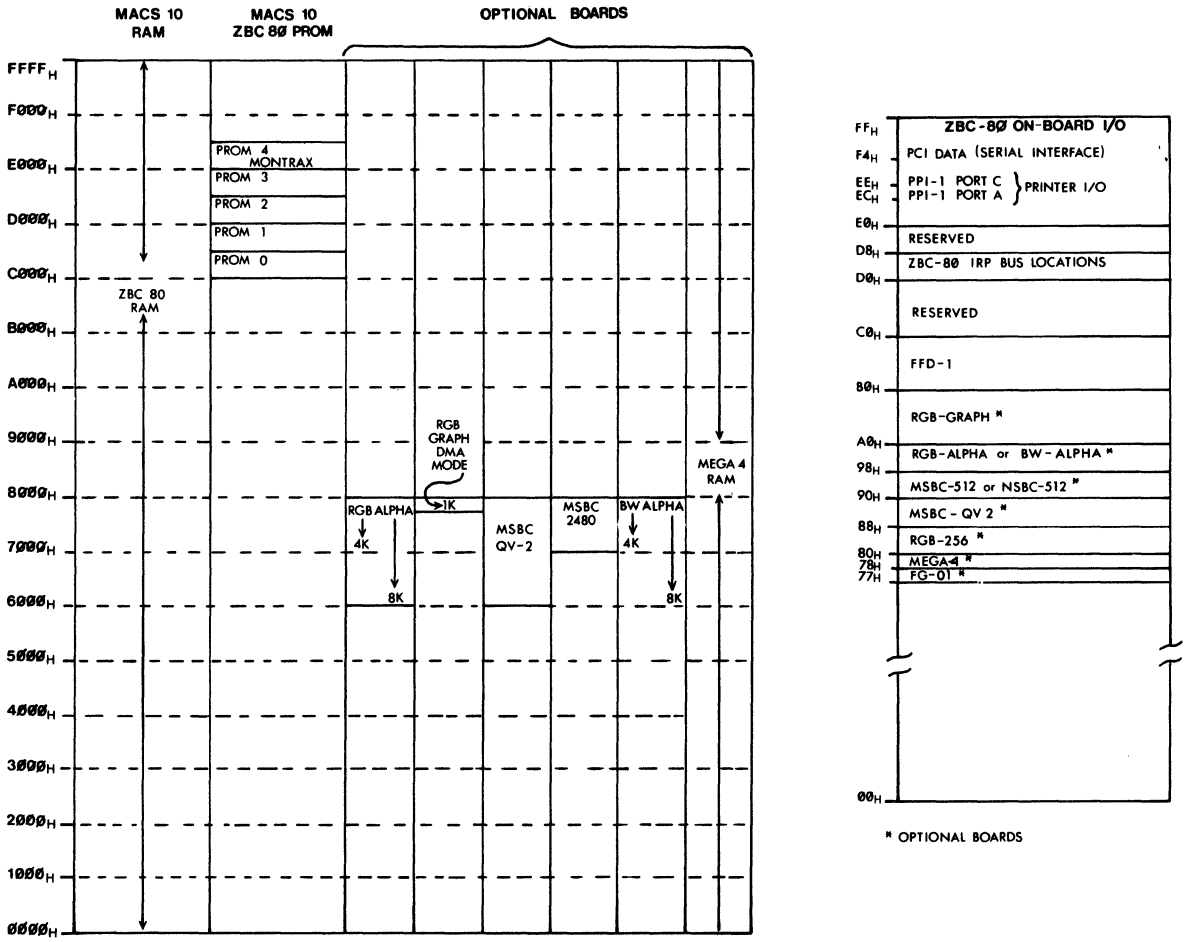


Figure 2. MACS-10 memory and I/O space distribution

# SPECIFICATIONS

**HOST PROCESSOR (ZBC-80)**

| | |
|---|---|
| CPU | Z-80A |
| WORD SIZE — instructions | 8, 16, 4, 32 bits |
| — data | 8 bits |
| — address | 16 bits |
| CYCLE TIME | 1000 ns (min.) |
| ON-BOARD MEMORY — RAM | 64K bytes |
| — ROM | 2K bytes (MONTRAX monitor) |
| | sockets for up to 40K bytes |

**DISK CONTROLLER (FFD-1)**

DISK FORMAT

| | SINGLE DENSITY (FM) | | | | | | DOUBLE DENSITY (MFM) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | IBM | | | NON-IBM | | | IBM | | NON-IBM | |
| bytes/sector | 128 | 256 | 512 | 128 | 512 | 1024 | 256 | 128 | 512 | 1024 |
| sectors/track | 28 | 15 | 8 | 30 | 8 | 4 | 26 | 52 | 16 | 9 |
| tracks/diskette | 77 | | | up to 225 | | | 77 | | up to 225 | |

**DISK SYSTEM (DF-28)**

| | SINGLE DENSITY | DOUBLE DENSITY |
|---|---|---|
| **CAPACITY** | | |
| Unformatted | 3.2 megabits/disk | 6.4 megabits/disk |
| | 41.7 kilobits/track | 83.4 kilobits/track |
| IBM format | 2.0 megabits/disk | 5.6 megabits/disk |
| | 26.6 kilobits/track | 73.7 kilobits/track |
| **TRANSFER RATE** | 250 kilobits/sec. | 500 kilobits/sec. |
| **ACCESS TIME** | | |
| Track to track: | 8 ms | 8 ms |
| Settling time: | 8 ms | 8 ms |
| Average: | 260 ms | 260 ms |

**SOFTWARE**

| | |
|---|---|
| MONTRAX — media | ROM |
| — function | ZBC-80 monitor |
| CP/M 2.2 — media | double density diskette |
| — function | disk operating system |
| TESTMACS — media | double density diskette |
| — function | system diagnostics program |

**BUS COMPATIBILITY**

All control, address and data lines conform to Inter Multibus specification no. 9800683

**SIZE**

| | |
|---|---|
| Width: | 20.00 in. (50.8 cm) |
| Height: | 15.00 in. (38.1 cm) |
| Depth: | 18.00 in. (45.7 cm) |
| Weight: | 90.00 lb. (40.5 kg) |

**POWER REQUIREMENTS**

115/230V AC 50/60 Hz

**ENVIRONMENTAL REQUIREMENTS**

| | |
|---|---|
| Operating Temperature: | 0°C — 50°C dual fans included |
| Relative Humidity: | 95% non-condensing |

**ORDERING INFORMATION**

MACS-10/S/XX

- AS — American standard (60 Hz)
- ES — European standard (50 Hz)

OEM computer

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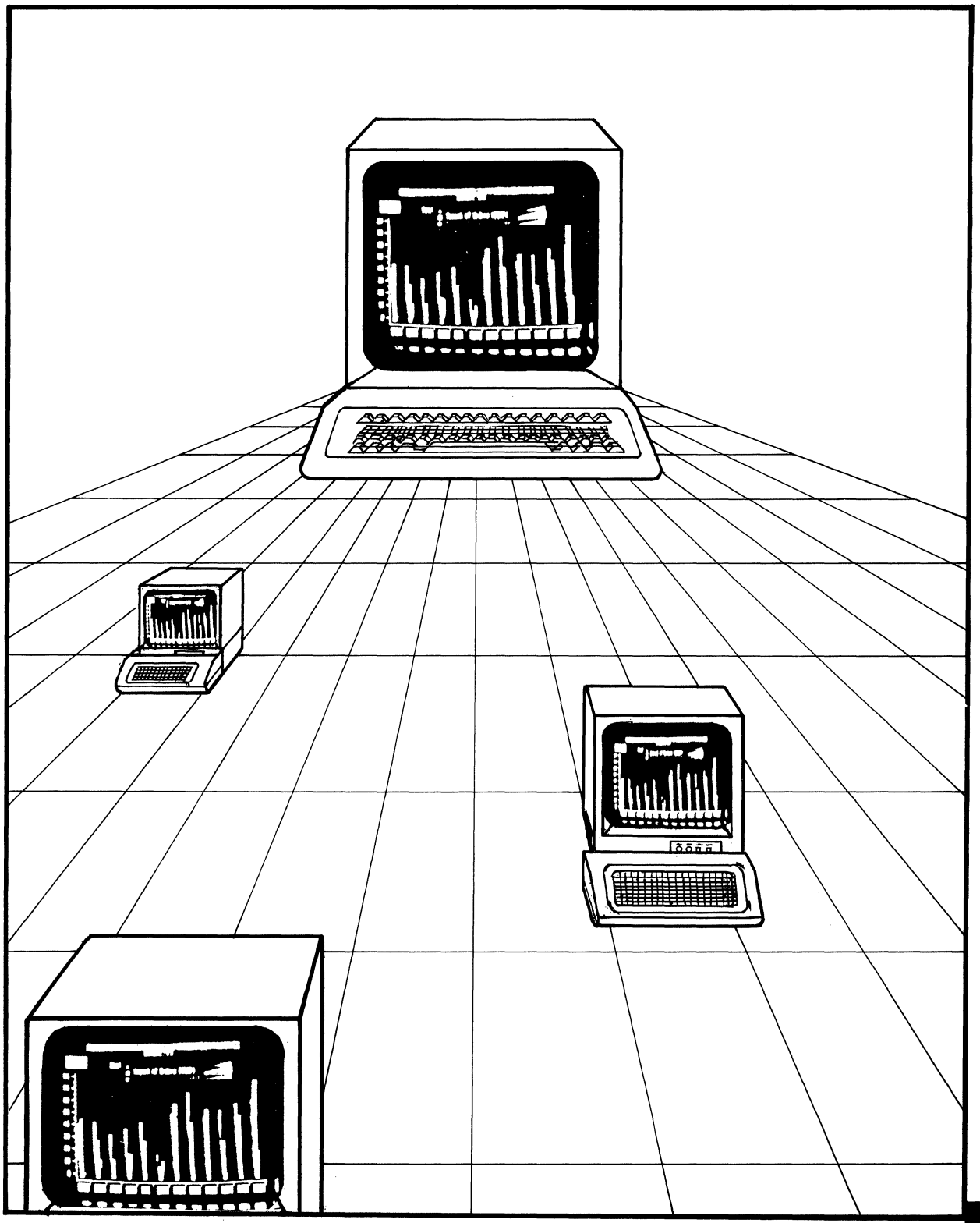

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# GRAPHICS TERMINALS

## SECTION 15 GRAPHICS TERMINALS

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

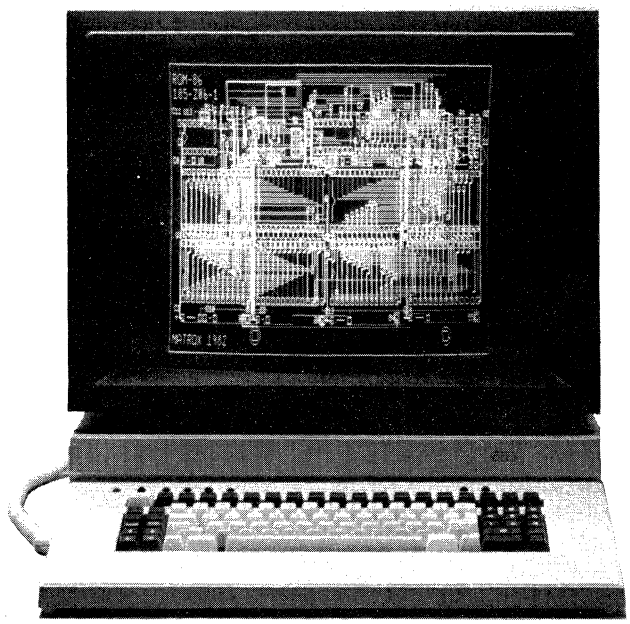
# GXT-1000

## HIGH RESOLUTION INTERACTIVE COLOR GRAPHICS TERMINAL

- **Display resolution of up to 1280 x 1024**
- **80286 main CPU plus 6 additional pipelined processors including 8086, 8088, and Z-80A**
- **20,000 vectors/second max. system throughput**
- **Up to 16 video memory planes**
- **Look-up table provides 256 display colors/surface**
- **19" flicker free color CRT**
- **Detachable low profile keyboard**
- **Local picture storage (up to 20M bytes)**
- **Local segment storage (up to 1M bytes)**
- **Full 2D transformations standard**
- **3D with hidden surface removal and shading optional**
- **Multiple viewports and dialog areas**
- **EASY ROAM real time pan function and smooth zoom in 64K x 64K space**
- **Data tablet, mouse, printer, and color plotter interfaces built-in**
- **Host communications via RS-232 (19.2K baud), optional RS-422 (300K baud), or parallel DMA (400K words/sec)**

The GXT-1000 is a high performance/low cost interactive color graphics terminal for use in single or multiuser CAD/CAM systems with micromainframe, supermini, or mainframe hosts. The GXT-1000 provides near real-time interactive response. It accepts picture data from the user's host computer via a serial or parallel communications line, and displays the image on a flicker free high resolution 19" color screen. The GXT-1000 provides a viewable resolution of up to 1280 x 1024 points, and each point can be displayed in one of 256 different colors.

The GXT-1000 provides exceptional local functionality including; 64K x 64K x 64K virtual display coordinates, multiple viewports, multiple surfaces, full 2D and 3D transformations, optional 3D hidden surface removal and shading, local picture segment storage, and graphics input device control. The benefits of local intelligence are simpler and shorter host graphics programs, and faster program execution. Multiple users can be accommodated without degrading the overall system performance.



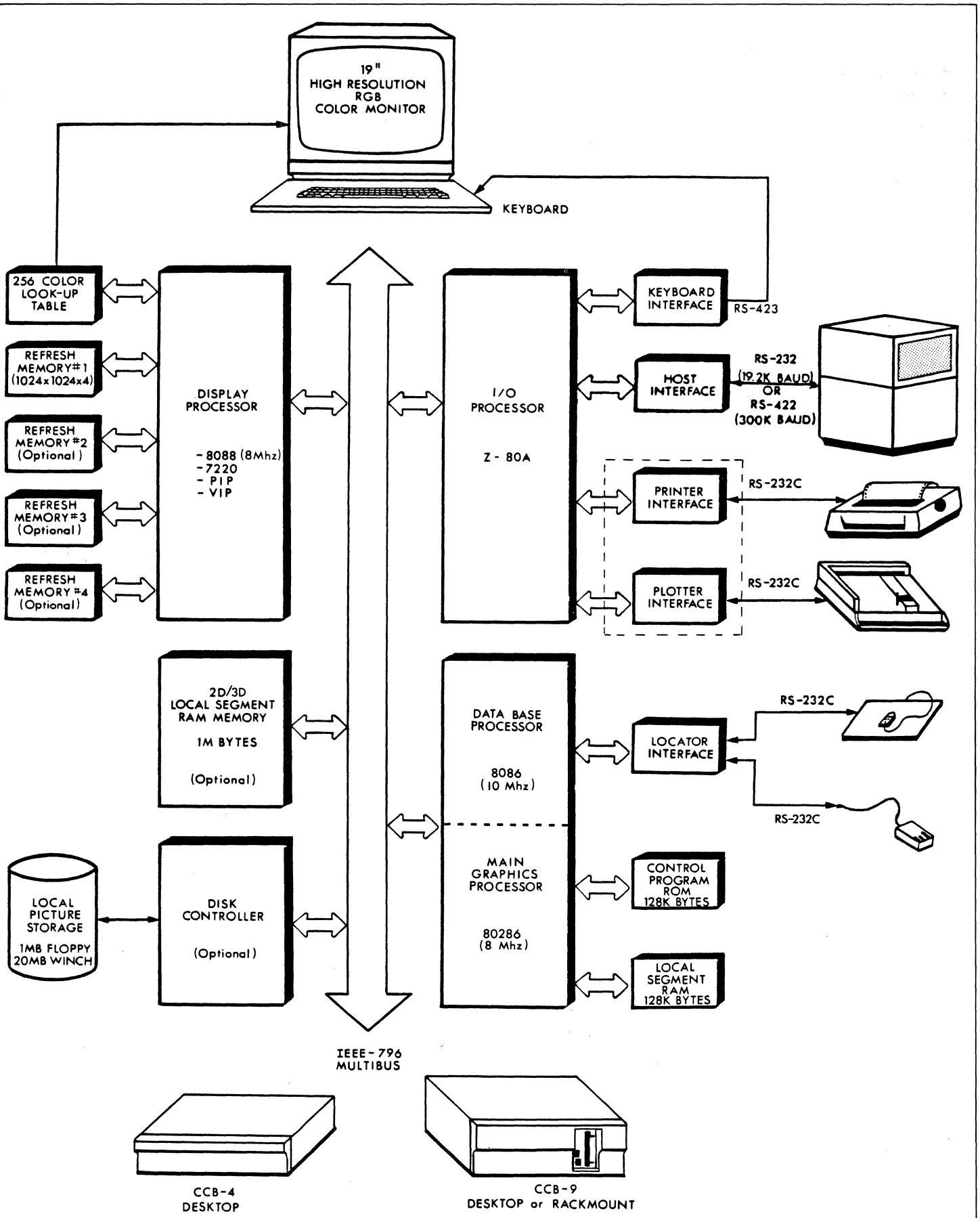



Figure 1. GXT-1000 block diagram

# GXT-FEATURES

## HIGH RESOLUTION

**Resolution:** The GXT-1000 can be supplied with one of three standard resolutions; 1280 x 1024, 1024 x 768, or 640 x 480. Interlaced or non-interlaced operation can be specified.

**Bits/Pixel:** 4 bits/pixel (16 colors) are standard. Extra bit planes can be optionally added to the terminal, in multiples of four, to a maximum of 16 bits/pixel (four 4-bit surfaces).

**Color Look-Up Table:** Each 4-bit surface has its own look-up table. Up to 16 colors, from a 256 color palette, can be selected for each surface under user control.

**High Resolution Color Monitor:** The GXT-1000 can be supplied with any of three high resolution RGB color monitors, depending on the resolution and refresh rate requirements.

## HIGH SPEED

**80286 Graphics Engine:** The GXT-1000 uses a high speed 8 MHz 80286 CPU as the main graphics engine.

**Multiprocessor Architecture:** In addition to the 80286, the GXT-1000 uses 6 pipelined slave processors (including a 10 MHz 8086, 8 MHz 8088, and a 4 MHz Z-80A) for maximum system throughput. Each processor is optimized to perform a unique task such as I/O or data base management. The pipelining and parallel processing capabilities associated with a multiprocessor system allows much higher throughput than would be achievable with a single processor system.

**Drawing Speed:** Maximum drawing speed of 20,000 vectors/second includes transformation, clipping, and drawing.

**Fast Area Fills:** The GXT-1000 can generate filled areas at a rate of up to 5000 filled rectangles/second.

## HIGH PERFORMANCE

**Read/Write Area:** The GXT-1000 supports a virtual addressing area of 64K x 64K for 2D applications and 64K x 64K x 64K for 3D applications. The virtual coordinate space can be reduced to 4K x 4K, under software control, if required.

**Local Picture Storage:** A Winchester hard disk drive and a 5¼" Floppy disk drive provide up to 21M bytes of mass memory for local picture storage.

**Local Segment Storage:** The GXT-1000 terminal can support up to 1M bytes of RAM memory for local segment storage. Up to 2000 segments can be retained in the terminal RAM.

**2D Transformations:** All 2D transformations (scaling, clipping, zooming, etc.) are done locally, within the GXT-1000 terminal.

**3D Transformations:** The GXT-1000 can optionally support local 3D transformations, including hidden surface removal and surface shading.

**Viewports and Dialog Areas:** The display screen can support up to 64 independent viewports and up to 4 dialog areas. The size and position of each viewport and dialog area can be set by the user.

**EASY ROAM:** The displayed image can be panned over the entire 64K x 64K data base in near real time

## LOCAL I/O SUPPORT

**Host Communications:** The GXT-1000 supports an RS-232C serial port (programmable up to 19.2K baud) as the standard communications line with host. Optionally the host interface can be replaced by an RS-449/422 serial line (up to 300K baud) or a high speed parallel DMA port (400K words/second).

**Serial Keyboard:** The detachable 101-key low-profile keyboard connects to the GXT-1000 via an RS-232C serial port.

**Data Tablet Interface:** An RS-232C serial port is supported to interface a data tablet. A software driver is also included, which is configured to support a Summagraphics BIT PAD ONE data tablet. A +5V power connector is also provided for the tablet.

**Mouse Interface:** The data tablet interface can also be used to interface an optical mouse. Drivers are provided which support the Summagraphics Summamouse.

**Printer Interface:** An RS-232C serial port is provided to interface a line printer. The software driver is configured to support a C.ITOH MI550-R printer.

**Plotter Interface:** An RS-232C serial port is provided to interface a color plotter. The software driver is configured to support a Bausch & Lomb DMP-29.

## OEM OPTIONS

**System Chassis:** The GXT-1000 system chassis is available in either a 4-slot or 9-slot version. The 4-slot cardcage is intended for desktop systems while the 9-slot cardcage is available as either a desktop or rackmount unit.

**Modular Hardware:** For OEM applications the GXT-1000 hardware is available, unbundled, as a Multibus board set. The system cabinet, keyboard, and monitor are also available as separate items.

**Host Software:** Matrox supports a host software package (QUARTO/GXT) to run on Digital Equipment's VAX and LSI-11 minicomputers. The QUARTO/GXT package is compatible with the GKS graphics standard.

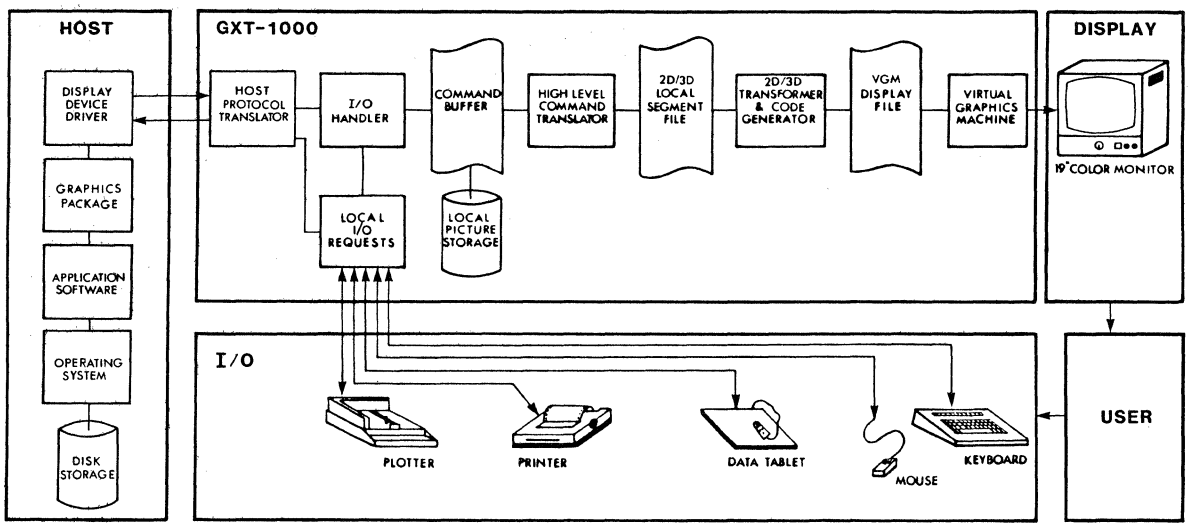



Figure 2. GXT-1000 software organization in a typical CAD/CAM system

## FUNCTIONAL DESCRIPTION

The GXT-1000 is a highly intelligent graphics terminal. The unit provides a high resolution color display of graphic and alphanumeric data on a flicker free 19" display. The terminal provides, to the user, the ability to display and manipulate a 2D, 2½D or full 3D object data base defined in 64K x 64K x 64K virtual coordinates. Up to 16 planes of memory are available to store video data for applications such as printed circuit board designs, VLSI designs, and mechanical or architectural CAD/CAM.

The GXT-1000 employs the latest advances in VLSI technology. A multiprocessor design consisting of 7 pipelined general purpose 16 bit processors and special purpose graphics processors has been used to provide extremely fast command execution. The most powerful 16-bit CPU on the market, the 80286 (8 MHz), is used as the main graphics processor, and additional support is provided by an 8086 (10 MHz), an 8088 (8 MHz), and four additional processors. The result is a terminal that outperforms older raster and vector devices on several key benchmarks, and at a significantly lower cost.

The GXT-1000 receives picture files containing high level graphics commands, from the user's "host" computer. The enhanced Tektronix 4113 type commands allow the user to create multiple viewports on the screen, to pan the display throughout the virtual coordinate space, to rotate pictures or picture segments, to zoom in for detail, to zoom out for overall views, etc.

The GXT-1000 incorporates a very powerful feature; local picture segments. Local segment storage allows the operator or the user's host computer to manipulate the displayed image (rotate, pan, zoom, etc.) without modifying or retransmitting the picture file. Local segments permit much faster display view updates than would otherwise be possible. Also, host-terminal communications are greatly reduced, leaving the host computer free for non-graphics tasks. Local picture and segment memory can be expanded with additional RAM or disk options, providing up to 22M bytes of local storage.

The GXT-1000 is an interactive terminal. The operator can use the keyboard, a data tablet, or a mouse to create or modify a picture file. The modified file can then be transferred to the host. Local interactive support greatly reduces the operator-display feedback cycle. Views are updated quickly and without tying up valuable host CPU time and resources.

**High Resolution Color Display** — The GXT-1000 provides a dot addressable display format of up to 1280 x 1024 pixels (picture elements). The display raster is refreshed at a rate of up to 60 frames per second (60 Hz), thereby providing a totally flicker free picture. This image is displayed on a 19" high resolution color CRT.

Four video refresh memory planes are standard on the GXT-1000. The data stored in memory (4 bits/pixel) indexes a user loadable color look-up table which generates 16 colors from a palette of 256 different shades. Additional video refresh memory boards can be added (optional) to provide up to 16 memory planes, with up to 256 simultaneously displayable colors.

**Surfaces/Subsurfaces** — A single refresh memory board is treated as a four plane "surface". Each surface has its own color look-up table. The video outputs of multiple surfaces can be enabled or disabled, combined in a priority manner, or logically "ORed" together. This flexibility allows the user to define a straightforward 16 plane overlay or a double buffer type format, when multiple surfaces are used.

The surface concept, used on the GXT-1000, has been extended down to the plane level. The user can define up to 4 subsurfaces per surface, with each subsurface consisting of one to four planes. All high level commands work on surfaces and subsurfaces rather than bits/pixel and look-up table entries, thereby greatly simplifying the conceptual model.

## INTERACTIVE 2D AND 3D APPLICATIONS

The host generates pictures in the GXT-1000 viewport in two ways. In **Non-Retained Segments** mode the picture is drawn primitive by primitive as received from the serial port or the DMA channel. Data base processing and viewing transformations are all done by the host. The terminal is used for display only (equivalent to the Tektronix 4014 terminal). This mode is usually used for the data base generation and host segment modifications.

In **Retained Segments** mode, the host transfers only the viewing parameters. The GXT-1000 will then transform, clip, and draw pictures from the local terminal's data base. (The viewing parameters can also be generated locally by the operator without host assistance by using local GXT-1000 I/O devices such as keyboard, data tablet, and mouse).

A **Local Picture Segment** is a group of graphics primitives that describes a portion of a bigger picture. These segments are retained in the terminal's local memory as graphics subroutines to be redrawn and manipulated at any time without host intervention. The GXT-1000 supports both 2D and 3D segments and viewing modes.

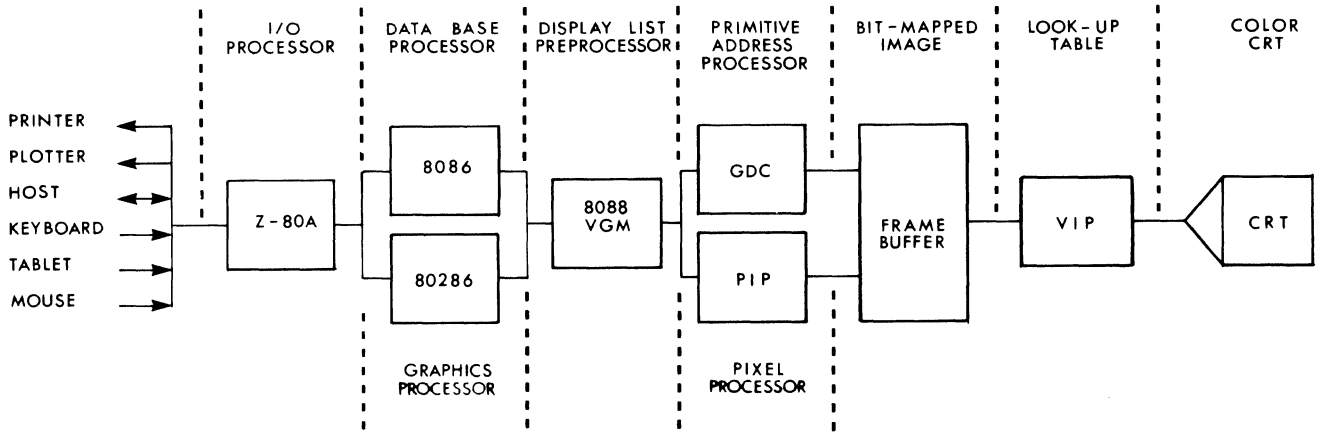



Figure 3. GXT-1000 multiprocessor pipeline organization

For 2D and 2½D applications, the segments are specified in virtual 64K x 64K space with priority levels from 0 to 64K. (A priority level is equivalent to a constant "Z" coordinate for every 2D primitive in the segment). The 2D primitives include markers (points), vectors, filled and outlined polygons, circles, alpha and graph text, etc.

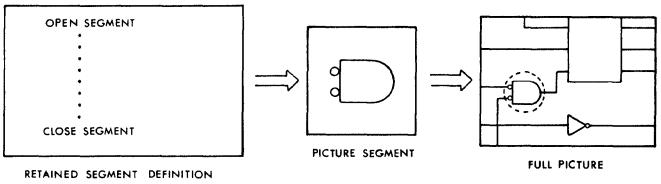



Figure 4. Retained picture segments

For 3D applications, the segments are specified in a 64K x 64K x 64K virtual space. A 3D surface segment is a series of shaded colored 3D planar polygons describing 3D surfaces and bodies in space.

### 2D DISPLAY MODE

2D and 2½D is the standard mode of operation for the GXT-1000. Local 2D segments can be rotated, scaled, translated (moved around the screen) by simple short commands from the host or from the local keyboard.

The GXT-1000 works with viewports and windows. The CRT screen is divided into multiple rectangular viewports (from 1 to 64). Viewports can be specified as rectangles of any size and position on the screen, up to the maximum CRT raster size (1280 x 1024). Multiple viewports enable the user to simultaneously display several views of the same object or of several different objects. Each viewport, has associated with it a 2D window and viewing transformation.

The window is a virtual 2D rectangle in 64K x 64K space which defines what portion of the 2D virtual space will be displayed in the viewport. The position and size of the 2D windows (up to 64K x 64K) are specified by the host or locally by the user.

The 2D viewing transformation maps the 2D world picture enclosed in the window to the corresponding 2D viewport on the screen. All primitives in the segment are transformed, clipped, and drawn locally by the GXT-1000 at the speed of 20,000 vectors per second.

High speed 2D smooth zoom and pan can be performed locally or via the host. A graphics keypad is used to pan the display locally with a rectangular cursor and to set the dimensions of the magnified image.

With this magnification capability, the user can view and work with plots of the same complexity as those developed on the highest resolution storage tube displays. This permits local examination of extremely fine detail without waiting for rescaled data to be transmitted from the host.

**EASY ROAM** — A proprietary Matrox pan circuit allows the user to perform a two-dimensional pan over the entire 64K x 64K 2D data base in near real-time at any zoom factor. When the EASY ROAM mode is selected, the terminal automatically uses a combination of hardware and software windows to simulate full smooth hardware pan over a virtual 64K x 64K (4 Gigapixels) video frame buffer is near real-time.

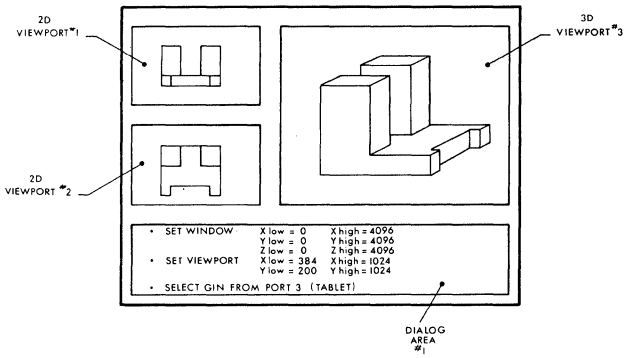



Figure 5. Windows, viewports, and dialog areas

### 3D DISPLAY MODE

In the 3D mode, (option TC-286/3D is required), segments can be defined as either 2D or 3D. The viewports are specified and positioned in the same way as for the 2D mode. Each viewport has associated with it a 2D or 3D window and corresponding viewing transformation. The GXT-1000 supports a mix of 2D and 3D segments and windows on viewports, enabling the user to view 3D objects, their 2D projections and other 2D segments (such as text, overlays, etc.) at the same time.

3D segments are used to specify objects in 64K x 64K x 64K virtual space. The position, size, and orientation of the 3D window (actually a pyramid) and its 3D viewing transformation are transmitted by the host, or generated locally. The viewing transformation maps the 3D world scene enclosed within the 3D window into the corresponding 2D viewport on the screen. 3D segments are transformed, clipped, scaled, and drawn on the screen locally by the GXT-1000. Full 3D transformations including perspective projection, near/far plane clipping, and wireframe or hidden surface removal with shading are supported.

When 2D segments are used in the 3D mode they are considered to be 2D in a plane, Z = constant, specified by the segment's priority. The 2D segments will be transformed by a separate 2D transformation and drawn in the same, or separate, viewport together with 3D segments at a speed of up to 20,000 2D vectors per second.

3D segments are defined as a series of 3D colored planar polygons describing 3D surfaces and bodies in 64K x 64K x 64K space. Each polygon is specified as a series of co-planar vertices in a 3D plane and has one of 256 possible colors. (Half-tone dither is used to obtain shading with 4 bits/pixel).

The GXT-1000 obtains hidden surface removal at interactive speeds by implementing an exclusive Matrox "F" algorithm in hardware and software. Instead of building a picture pixel by pixel from top to bottom with full resolution, as in classical hidden surface algorithms which are very slow, the GXT-1000 generates a picture in one or more passes with increased resolution after each pass.

Each pass generates a true 3D full size picture with the hidden surfaces properly removed. The first pass, F0, generates a 3D wireframe outline of the scene with or without the object's backsurfaces removed (user selected). This pass is very fast and draws at speeds of 4,000 3D vectors per second. Additional F passes are required to color and shade visible surfaces and remove object by object hidden surfaces. The number of required passes depends on the CRT viewport dimensions. Viewports smaller than 256 x 256 pixels require only one pass, viewports between 256 x 256 and 512 x 512 pixels require four passes, and viewports bigger than 512 x 512 pixels require a minimum of sixteen passes.

The effect on the screen is a gradual fill-up of the visible surfaces after each pass. (This method is similar to the familiar generation of waveforms by cummulative addition of Fourier sinewaves with frequencies increasing with each addition).

A typical 3D picture, containing 5000 polygons, requires between 2 — 20 seconds per pass. The unique feature of the "F" algorithm is the ability of the user to stop the picture update after any number of passes, since additional passes mainly improve apparent resolution of the displayed picture and have little or no effect on the geometric properties of the scene.

The GXT-1000 uses a shading model with a single diffused illumination source for both ambient light and specular diffuse reflection. Each polygon is assigned eight possible uniform intensities after transformation. Pixel color intensity is a function of the angle between the incident light and the polygon normal. The light source can be at any angle relative to the viewing pyramid Z-axis.

**Dialog Areas** — The user can specify up to four independent dialog areas of any size, anywhere on the screen. Two keys are provided for scrolling the current dialog area. Dialog areas are primarily used for displaying host-terminal communications. Other applications for dialog areas include the display of host background task status, menus, and user prompts. The context (pen color, size, cursor position, etc.) for each dialog area is stored independently. This allows instant access to all dialog areas.

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## INPUT/OUTPUT

The GXT-1000 I/O processor communicates with several I/O devices. The primary communications link is with the user's host computer. This is a bidirectional link which allows the host to transmit picture files to the GXT-1000, and to receive commands and data from the terminal. Complete hardware and software I/O interfaces are also provided for communications between the terminal and the keyboard, a data tablet, and a mouse. Optional interfaces are available for a printer, and a low cost color plotter.

**Host Interface** — The GXT-1000 communicates with the host computer via an RS-232/423 serial line. Transmission speeds of up to 19.2K baud can be selected by the user. X-ON/X-OFF protocol is provided. The GXT-1000 accepts graphics commands using Tektronix 4113 serial line protocol. An optional RS-422 interface is available for transmission rates of up to 300K baud. Using this interface, a typical object file of 5000 vectors can be downloaded to local disk memory in less than one second. If extremely high speed communications are required, a parallel DMA option, compatible with a DEC DR-11W, can provide transfer rates of up to 400K words per second.

**Keyboard Interface** — The keyboard is used for normal operator interaction (editing picture files, calling programs from the host, etc.). Several special graphics functions including cursor manipulation, pan and zoom, and paging, are controllable by the operator from the keyboard. The keyboard displays system status to the operator via 10 LED indicators and an audible tone.

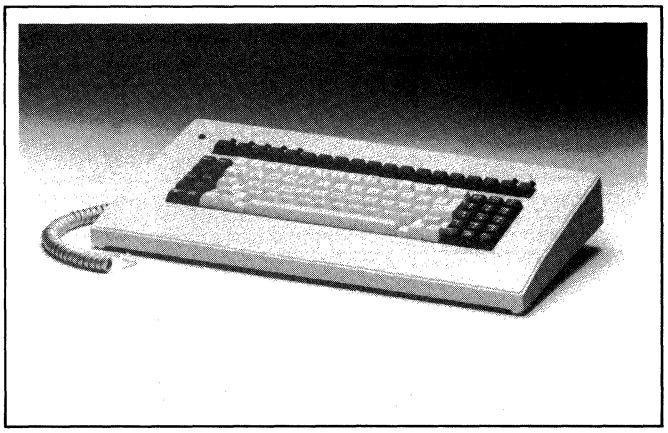


Figure 6. KB-100 serial keyboard

**Data Tablet Interface** — The GXT-1000 has been configured to operate with a Summagraphics Bit Pad 1, using either a stylus or a four button cursor. The GXT-1000 software supports point and segment identification, inking, rubber banding, tracking, etc. An RS-232C port is used to communicate with the tablet. A power take-off is also provided.

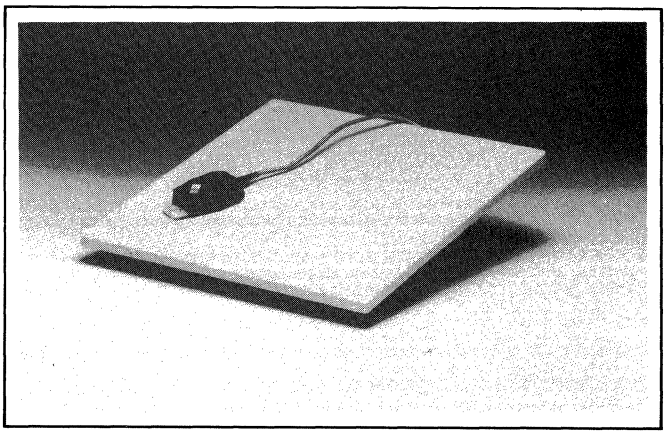


Figure 7. BIT PAD ONE data tablet

**Mouse Interface** — The user may elect to use a mouse rather than a data tablet for I/O. The GXT-1000 will also accept data from a Summagraphics optical mouse via the tablet port.

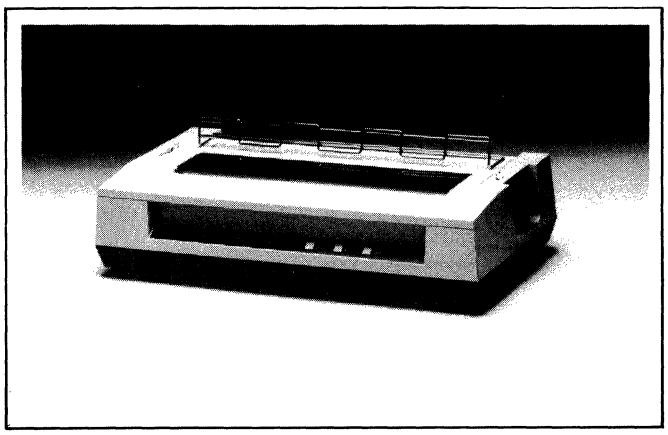


Figure 8. C.ITOH MI550-R line printer

**Printer/Plotter Interface** — A optional dual RS-232C port controller can be added to the terminal if a local printer and/or plotter is required. The terminal software supports a C.ITOH MI550-R line printer for dialog area print-outs, and a Bausch & Lomb (Houston Instruments) DMP-29 eight-pen flatbed color plotter.

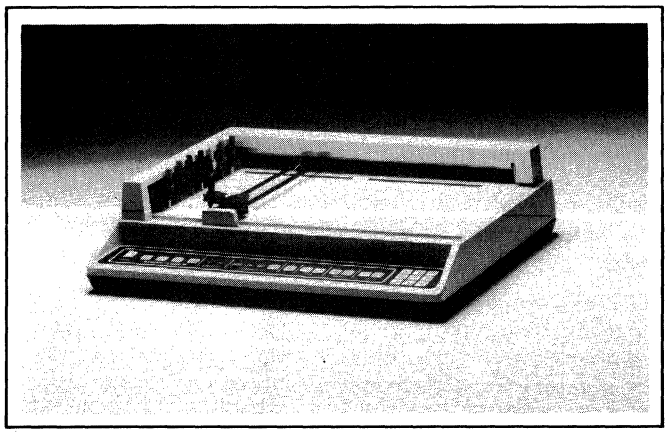


Figure 9. Bausch & Lomb DMP-29 color plotter

## HOST SOFTWARE SUPPORT

The GXT-1000 is designed to function with CORE and GKS software packages running on a wide range of host processors. In the host, a device dependent software module known as a "device driver" is responsible for handling communications with a graphics terminal. The device driver is usually optimized to take advantage of the features found in a specific terminal. Similarly there is a "host driver" software module, called a protocol translator, resident in the GXT-1000, which can be optimized to communicate with different hosts. The GXT-1000 can easily be integrated into existing CAD/CAM systems by modifying either the host device driver or the GXT-1000 protocol translator module. Any existing or new terminal protocol can be emulated, thus allowing the user to replace older terminals by the state-of-the-art GXT-1000. Matrox provides sufficient documentation to allow the user to write the front-end host device driver. Alternatively, Matrox can write a custom GXT-1000 Host Protocol Translator module to emulate any existing or new graphics terminal. Matrox also supports the GXT-1000 with a host software package, written in Fortran, for use under the VMS operating system on DEC VAX-series super-minicomputers.

## SYSTEM HARDWARE

The GXT-1000 consists of three physically separate components: a self-contained RGB color monitor, a detachable keyboard, and a system chassis containing the electronics. These three pieces fit together to provide a complete graphics terminal.

The actual electronics are implemented on standard Multibus cards. These cards partition the terminal circuitry into three separate functional blocks: I/O processor, graphics processor, and display processor. Two different chassis are available to house the display electronics. A 4-slot low profile cardcage can be used for systems requiring one option card. If more option cards are required, or if local disk memory is required, a 9-slot cardcage must be used.

**Color Monitor** — Three different monitors can be used with the GXT-1000. The MCM-1000L low profile 19" unit pictured on the front page is the standard display provided with the GXT-1000. This monitor uses long persistence phosphors to minimize flicker if the system is run in the interlaced video mode. The MCM-1000L uses in-line electron guns to maximize convergence over the entire display area. The MCM-1014L is a low profile 14" monitor similar in performance to the MCM-1000L.

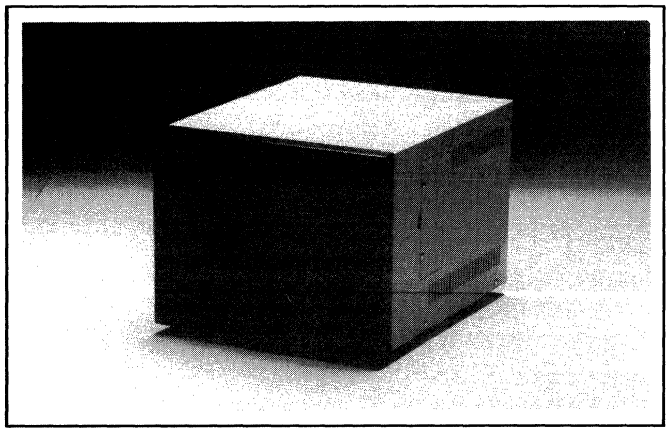


Figure 10. MCM-1014L color monitor

In order to display a 1024 x 768 image at a refresh rate of 50/60 Hz, it is necessary to use a higher bandwidth monitor. The MCM-2000L employs high speed deflection circuitry and an extremely fine pitch shadow mask to accommodate the required video performance.

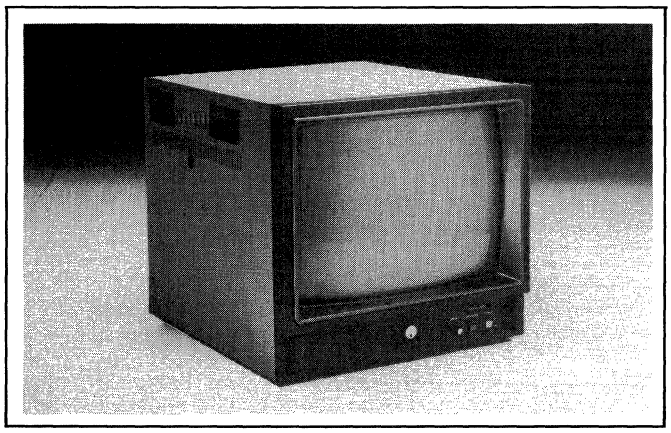


Figure 11. MCM-2000L color monitor

**Keyboard** — The GXT-1000 keyboard is a detachable low profile serial output device. It connects to the display controller via a single coiled cord. System status is displayed, on the

keyboard, by 10 LEDs. A "bell" is used to provide an audible tone.

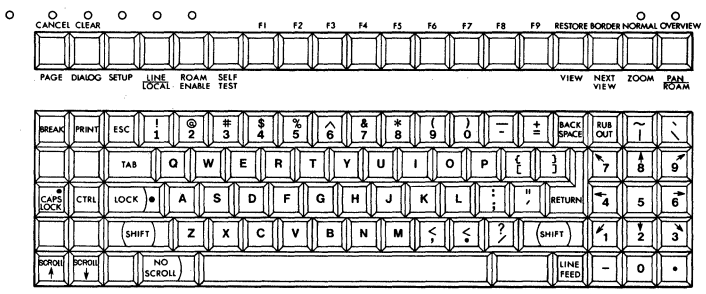



Figure 12. KB-100 keyboard layout

**System Chassis** — The GXT-1000 display electronics are housed in a Multibus chassis. Two different chassis are available. The CCB-4 is an attractive 4-slot low profile desktop box which has been designed to sit underneath the 19" CRT monitor. The CCB-4 is ideal for systems requiring only one option card. A larger chassis, the CCB-9, supports 9 Multibus slots. This attractive case is available in either desktop or rack-mount versions to suit terminal or workstation requirements. The CCB-9 is required if local disks are used for picture segment storage.

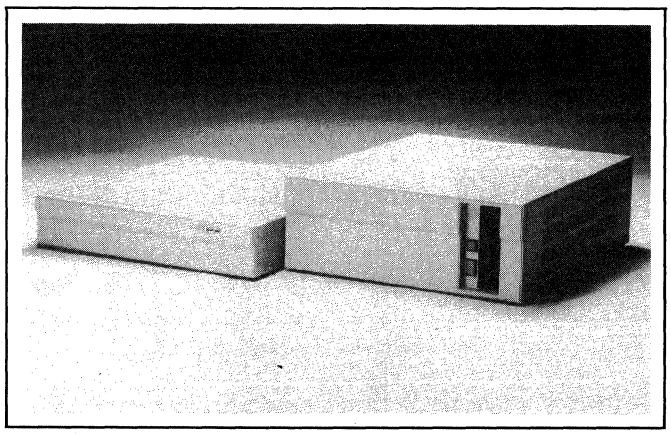


Figure 13. CCB-4/CCB-9 system chassis

**Display Processor** — The display processor is a Matrox GXB-1000. The display processor interfaces with the main graphics processor via a display file (using transformed screen addresses) stored in common RAM on the Multibus. The GXB-1000, which contains four dedicated graphics CPUs, executes a powerful instruction set which provides for surface and sub-surface visibility and priority; vector, arc, circle, and character drawing; cursor and marker generation; tracking, inking, and rubber banding; look-up tables; raster ops; and area fills. The GXB-1000 also includes the image buffer. The buffer memory, which can be up to 2M bytes in size, is partitioned into 1024 x 1024 x 4 bit sections, each occupying a separate Multibus board.

**Graphics Processor** — The main graphics processor is an 8 MHz, high performance, 80286 CPU tightly coupled with a 10 MHz 8086 data base processor. The graphics processor card contains 128K bytes of EPROM and 128K bytes of RAM. The processor board uses a concurrent real-time operating system with multitask scheduling. These tasks include dynamic memory management, high level graphics command interpretation, 2D and 3D transformation, clipping, scaling, windows and viewports, and tablet and mouse support. A picture data base, specified in 2D virtual coordinates, can be traversed, transformed, and drawn at a maximum rate of 20,000 vectors/second, and at an average rate of 5000 vectors/second, depending on the picture complexity, number of segments, and vector length. The GXT-1000 can sustain a continuous speed of over 5000 vectors per second from host to CRT screen.

**I/O Processor** — A separate Z-80A based processor card is used to handle all communications between the terminal and the host, as well as I/O to local peripherals. A serial RS-232C/423 communications port is used to communicate with the user's host. A second serial port is used as a keyboard interface. The I/O processor card also supports two iSBX expansion connectors which can be used to accommodate several communications options. An optional dual RS-232 module can be added for supporting a local printer and local color plotter; and an optional RS-422 module can be added for supporting high speed host communications.

**DMA Controller** — An optional high speed DMA controller board is used to provide a 16-bit parallel communications path from the GXT-1000 to the host (400K words/second). The COM-1 controller provides full compatibility with DEC's DR-11W series of interface cards.

# SPECIFICATIONS

## GENERAL

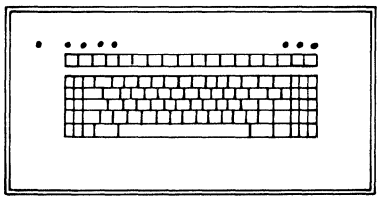
| PARAMETER \ FORMAT | | 1 | 2 | 3 |
|---|---|---|---|---|
| Graphics Resolution | | 640 x 480 | 1024 x 768 | 1280 x 1024 |
| Read/Write Area | | 1K x 1K | 1K x 1K | 1.4K x 1.4K |
| Refresh Rate | | 50/60 Hz | 25/30 Hz or 50/60 Hz | 25/30 Hz |
| Dialog Area Alphanumerics | | 80 x 30 | 128 x 48 | 80 x 32 |
| Virtual Address Range | | 64K x 64K x 64K | 64K x 64K x 64K | 64K x 64K x 64K |
| Color Palette Size/Surface | | 256 | 256 | 256 |
| Bits/Pixel | Standard | 4 | 4 | 4 |
| | Optional | 8, 12, 16 | 8, 12, 16 | 8 |
| Screen Size | | 14″ or 19″ diagonal | 14″ or 19″ diagonal | 19″ diagonal |
| Segment Storage | Standard RAM | 128K bytes | 128K bytes | 128K bytes |
| | Optional RAM Board(s) | 512K bytes/1M byte | 512K bytes/1M byte | 512K bytes/1M byte |
| Picture Storage | Optional 5¼″ Disks | 1MB Floppy 20MB Winchester | 1MB Floppy 20MB Winchester | 1MB Floppy 20MB Winchester |
| Vector Drawing Speed | | 20000 vectors/sec max. | 20000 vectors/sec max. | 20000 vectors/sec max. |

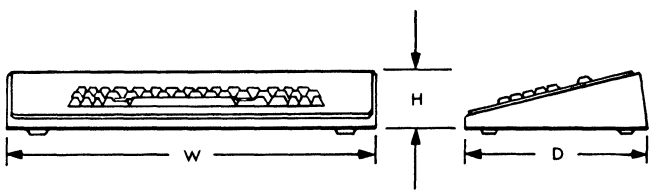
## ENVIRONMENTAL

| PARAMETER | DESCRIPTION | RESTRICTION |
|---|---|---|
| Operating Temperature | Operating | 10 — 40°C |
| | Non-operating | –40 — 65°C |
| Relative Humidity | Operating | 10 — 90% |
| | Non-operating | 0 — 95% non-condensing |
| Power Requirements | American Standard | 115V, 60 Hz AC @ 200W |
| | European Standard | 230V, 50 Hz AC @ 200W |

## KEYBOARD

| PARAMETER | DESCRIPTION |
|---|---|
| Keyboard Layout | Standard Qwerty typewriter layout with sculptured key design |
| Auxillary Keypad | Functions as numeric pad, cursor control pad (GIN mode), and graphics function controller (pan, zoom) |
| Graphics Functions Keys | ZOOM, PAN, and VIEW keys control the display window |
| Special Function Keys | Break, print, escape, control, page, print, set-up, self test, dialog, line/local, rub out, line feed |
| User Function Keys | 10 programmable user function keys |
| LEDs | 10 system status LED indicators |
| Audio Output | Audible tone |
| Weight | 8 lbs (3.6kg) |
| Dimensions | 2.0″ (H) x 19.0″ (W) x 10.0″ (D) (5.1 cm x 48.3 cm x 25.4 cm) |

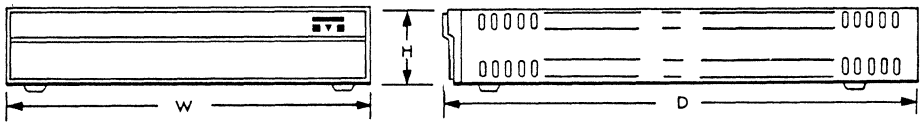




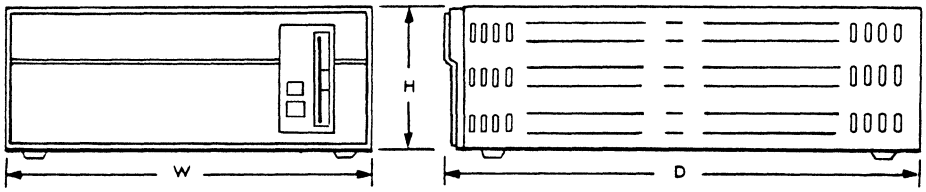
## ENCLOSURE/DISPLAY ELECTRONICS

| PARAMETER | CCB-4 | CCB-9 |
|---|---|---|
| Weight | 25 lbs. (11.2kg) | 50 lbs. (22.5kg) |
| Dimensions | 3.9" (H) x 19.0" (W) x 20.0" (D)<br>(9.9 cm x 48.2 cm x 50.8 cm) | 7.0" (H) x 19.0" (W) x 20.0" (D)<br>(17.8 cm x 48.2 cm x 50.8 cm) |

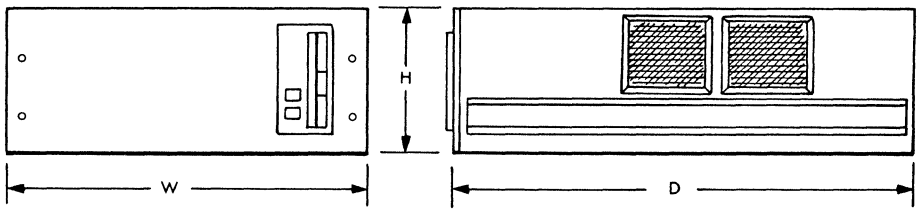
CCB-4




CCB-9



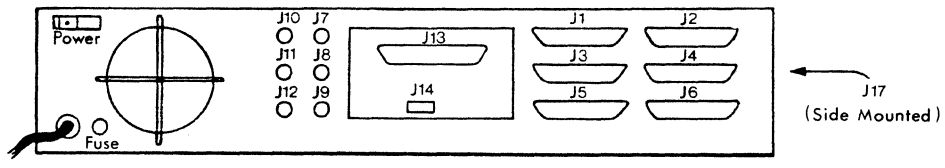

CCB-9/R



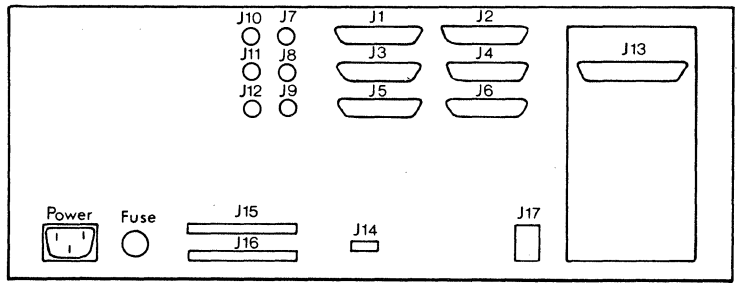

## INPUT/OUTPUT

| INTERFACE | NO. | DESCRIPTION | MATING CONNECTOR | COMMENTS |
|---|---|---|---|---|
| Not Used | J1 | — | DB-25 (male) | |
| Not Used | J2 | — | DB-25 (male) | |
| Serial Host Computer (standard) | J3 | RS-232/423 | DB-25 (male) | |
| Data Tablet/Mouse | J4 | RS-232 | DB-25 (male) | Summagraphics Bit Pad 1 |
| Printer | J5 | RS-232/423 | DB-25 (male) | C.ITOH MI-1550R |
| Plotter | J6 | RS-232/423 | DB-25 (male) | Bausch & Lomb DMP-29 |
| Monitor (red) | J7 | Analog video | BNC | MCM-1000L, MCM-1014L, or MCM-2000L |
| Monitor (green) | J8 | Analog video | BNC | |
| Monitor (blue) | J9 | Analog video | BNC | |
| Serial Host Computer (optional) | J13 | RS-422 | DB-37 (male) | |
| Tablet Power Jack | J14 | +5V | SM SMP-05V-B | |
| Parallel Host Computer (optional) | J15 | 16-bit input | ANSLEY 609-4031 | DEC VAX Superminicomputer |
| | J16 | 16-bit output | ANSLEY 609-4031 | (DR-11W) |
| Keyboard | J17 | RS-423 | Berg 66011-002 | KB-100 |

CCB-4




CCB-9

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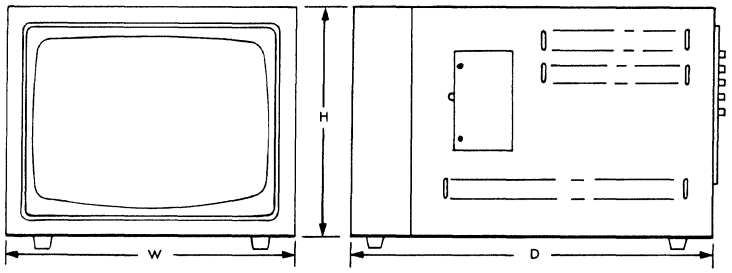
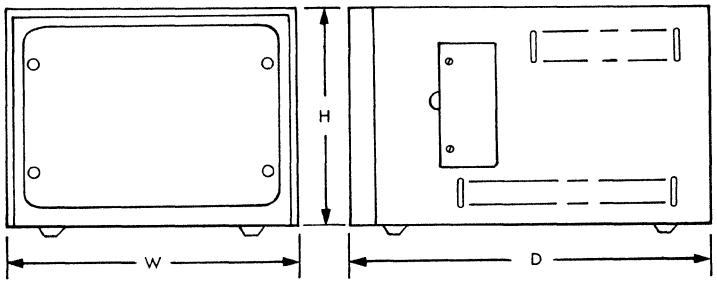
**MONITOR**

| PARAMETER | | MCM-1000L | MCM-1014L | MCM-2000L |
|---|---|---|---|---|
| Screen Size | | 19 in. diagonal | 14 in. diagonal | 19 in. diagonal |
| Gun Type | | In-line electron guns | In-line electron guns | Delta guns |
| Shadow Mask | | .31mm resolution | .31mm resolution | .31mm resolution |
| Controls | | Brightness, gain, and degauss controls | Brightness, gain, and degauss controls | Brightness controls and degaussing controls |
| Weight | | 88.0 lbs (40kg) | 39.6 lbs (18kg) | 120.1 lbs (54.6kg) |
| Dimensions | Height | 15.1 in. (38.5 cm) | 10.9 in. (27.6 cm) | 18.0 in. (45.7 cm) |
| | Width | 19.0 in. (48.2 cm) | 13.8 in. (35.0 cm) | 18.7 in. (47.6 cm) |
| | Depth | 20.0 in. (50.8 cm) | 17.8 in. (45.2 cm) | 21.2 in. (53.9 cm) |

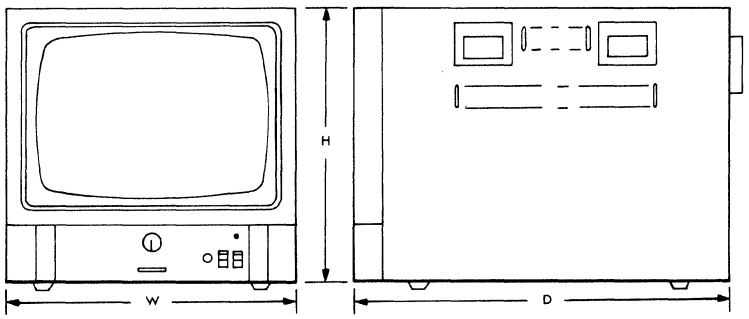
MCM-1000L




MCM-1014L




MCM-2000L

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## ORDERING INFORMATION

The GXT-1000 configuration data has been set up to allow for a great deal of ordering flexibility to suit different user applications and requirements. The main GXT-1000 part number identifies the main electronics cabinet configuration, and several option numbers are used to specify which monitor is to be supplied, and what additional boards will be added to the basic system. Note that the CCB-4 (4-slot chassis) can accommodate only one option card.

The basic system consists of a display electronics cabinet containing the I/O processor; Graphics processor; RS-232C interfaces for a tablet/mouse, a host processor, and a keyboard; and a Display processor (VGM-1000) with one 1K x 1K x 4 bit refresh memory board (RMB-1000). The keyboard is also included with the basic system. Note that the monitor is ordered as a separate item (see OPTIONS).

GXT-1000/XX/XX — 1K x 1K graphics terminal

- AS — 60 Hz American standard operation
- ES — 50 Hz European standard operation
- 4 — 4-slot chassis
- 9 — 9-slot chassis
- 9R — 9-slot rackmount chassis

GXT-1000D/XX/XX — 1K x 1K graphics terminal with local disks for picture storage

- AS — 60 Hz American standard operation
- ES — 50 Hz European standard operation
- 9 — 9-slot chassis
- 9R — 9-slot rackmount chassis

## RESOLUTION/REFRESH RATE AVAILABILITY

| RESOLUTION / REFRESH | 640 x 480 | 1024 x 768 | 1280 x 1024 |
|---|---|---|---|
| 25 Hz | — | X | X |
| 30 Hz | — | X | X |
| 50 Hz | X | X | — |
| 60 Hz | X | X | — |

Note 1: Since the 1280 x 1024 format exceeds the 1K x 1K memory stored on a single RMB, two RMB boards are required for each four bit surface.

Note 2: For refresh rates or resolutions not covered by the above table (i.e. 1600 x 1200) please consult the factory.

## OPTIONS

### Video Memory

| | |
|---|---|
| GXRMB-01 | Adds a second refresh memory board (RMB-1000) for more video planes, or a larger read/write area. |
| GXRMB-02 | Adds two additional refresh memory boards. |
| GXRMB-03 | Adds three additional refresh memory boards. |

### Segment Memory

| | |
|---|---|
| MEGA-4/512T | Adds an additional 512K bytes of local segment storage RAM. |

### Communications

| | |
|---|---|
| MSBX-423T | Adds a dual RS-232C serial port controller for interfacing to a printer and color plotter. |
| MSBX-422T | Adds an RS-422 serial port controller for high speed host communications. |
| COM-1/1/0T | Adds a parallel DMA controller compatible with a DEC DR-11W. |

### Monitors

| | |
|---|---|
| MCM-1000L | Adds a high resolution 19" RGB color monitor (supports all resolutions except 1024 x 768 @ 50/60 Hz). |
| MCM-1014L | Adds a high resolution 14" RGB color monitor (supports all resolutions except 1024 x 768 @ 50/60 Hz). |
| MCM-2000L | Adds a high bandwidth high resolution 19" RGB color monitor (supports 1024 x 768 @ 50/60 Hz). |

### Software

| | |
|---|---|
| TC-286/3D | Adds 3D graphics firmware and hardware with hidden surface elimination and shading. |
| QUARTO/GXT | Host software package for GXT-1000. FORTRAN subroutine library for use with VAX and LSI minicomputers. |

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# CTM-300

## INTELLIGENT COLOR ALPHANUMERIC TERMINAL

- **Intelligent color alphanumeric terminal**
- **25 x 80/132 character displays standard**
- **8 foreground/8 background colors**
- **101 key sculptured keyboard with numeric keypad**
- **18 user defined function keys**
- **2K user RAM for program download**
- **256 upper/lower case alphanumerics and graphics characters**
- **Blink, extended height, underline and protected character attributes**
- **Printer and light pen interfaces built in**

The CTM-300 Color Alphanumeric Terminal is a standard serially interfaced (RS-232C) ASCII terminal with an eight color CRT display. It is a high performance terminal with all the functions of an intelligent Black and White terminal plus color. A popular display format of 80 characters per line by 25 lines is standard, however any format, with up to 132 characters/line and 50 lines, can be programmed by the user.

In addition to the terminal firmware, which conforms to ANSI X3.64 (VT-100 compatible), the unique Matrox program download enables the user to customize terminal functions. The host computer can download a program into the CTM-300's 2K user RAM memory for execution by the CTM-300's CPU (Z-80A). This feature, together with 18 user definable keys, enables the user to adapt the CTM-300 to a variety of applications.

A high resolution (.3mm dot pitch) 12" color monitor offers superior color clarity and resolution. The detachable keyboard (containing all the terminal electronics) and the CRT display stand allow the operator the flexibility and freedom to operate the terminal efficiently. Standard options include: light pen interface, printer interface, American/European standard for power and video, and a 256 character font including upper/lower case alphanumeric characters, graphic characters, European characters, and more. Serial interface speeds of up to 19.2K baud are set by the user.

15

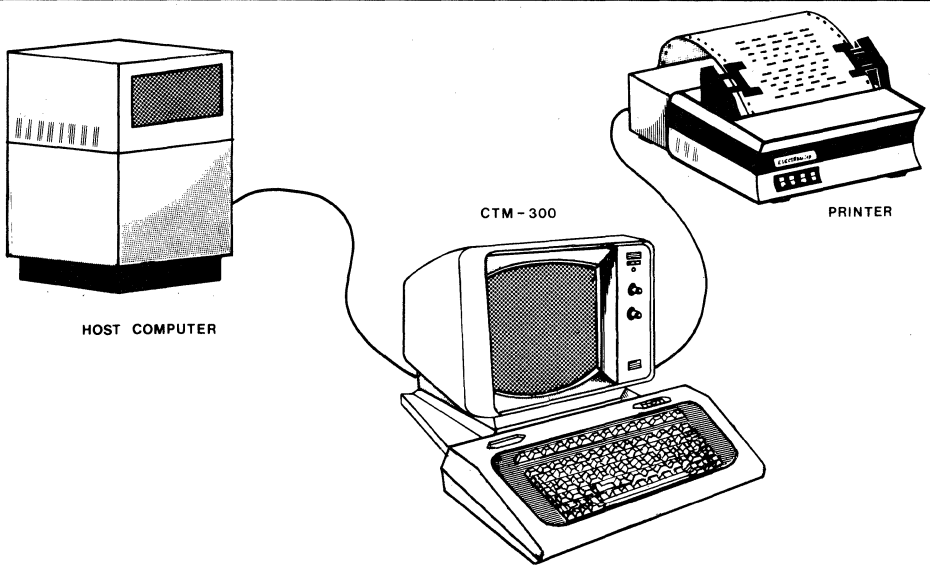



Figure 1. CTM-300 Intelligent Color Terminal — Typical system configuration

**DISPLAY**

The CTM-300 generates a color alphanumeric display consisting of 25 horizontal lines with 80/132 characters (switch selectable) displayed per line. These parameters, however, can be redefined by the user to accomodate virtually any configuration of characters/line and lines/page up to maximum of 4000 characters per display. Characters can be assigned as blinking, underlined, or protected (protected characters can not be erased or edited while the erasure mode is not in effect). The blink or underline attribute can optionally be replaced (via a hardware strap) by an extended height attribute for displaying double height characters. Furthermore, each character can be assigned to be displayed in one of eight different foreground colors on one of eight different background colors. Color selection (foreground/background) is also user selectable via user function keys on the CTM-300.

As supplied, the CTM-300 contains a font of 256 displayable characters. This character set (figure 2) consists of all the alphanumeric characters and punctuation symbols for displaying text in one of six different languages: English, French, Spanish, German, Greek, or Swedish. The CTM-300 also includes a set of 32 "graphic characters" which can be used for generating character oriented graphics such as: business forms, process loop displays, bar charts, etc. Moreover, the user can redefine the character set for custom applications by simply replacing the supplied character generator with a 2532 EPROM loaded with his custom character font.

The CTM-300 is normally equipped with a 12" color monitor which uses a fine pitch shadow mask for high resolution color displays, and in-line electron guns to minimize color distortion due to convergence error. The CTM-300, however, contains all its electronic hardware circuitry in the keyboard module and therefore allows the user to replace the monitor with virtually any other available monitor. This feature allows the user the flexibility to configure the CTM-300 to suit his own environment (i.e. screen size, interlaced/non-interlaced displays, etc.).

**KEYBOARD**

The main component of the CTM-300 is the keyboard module which contains all the electronics for the terminal. The keyboard contains 101 keys in a standard typewriter layout with a numeric keypad and cursor controls. Special Control Keys include: Break, Print, Insert, Delete, and Caps Lock. A further 18 user defined function keys can be used to adapt the CTM-300 to a variety of applications. As supplied, these keys are defined as color selection keys and character set mapping keys.

The CTM-300 keyboard features a sculptured keyboard layout. This ergonomic design promotes operator comfort and therefore improves data entry efficiency.

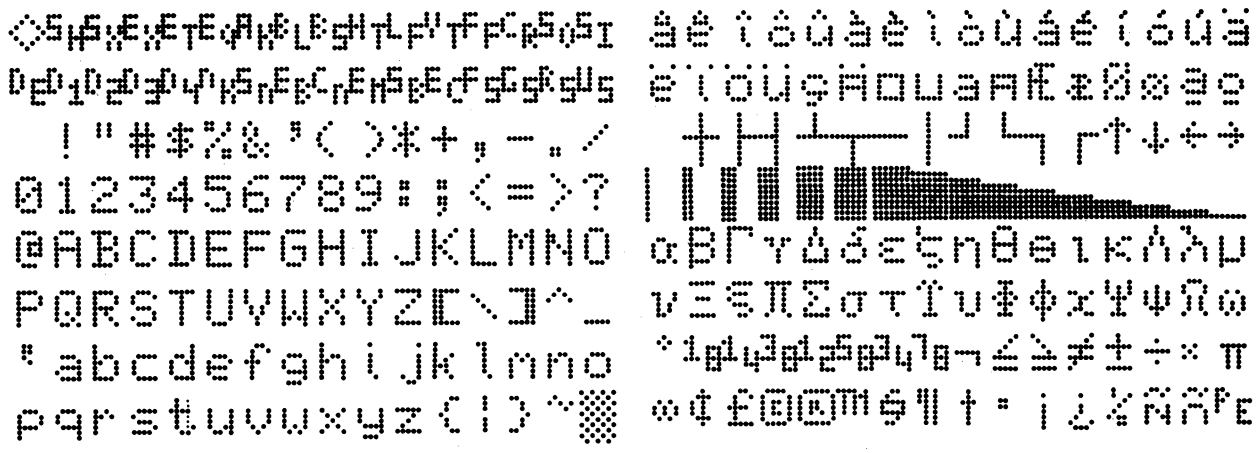


Figure 2. CTM-300 Character set

## EDITING

The CTM-300 includes a comprehensive set of cursor, erase, and character attribute controls which facilitate text editing. Cursor control commands enable the user to redefine the position of the cursor using either "relative" or "absolute" movement commands. Relative cursor movement commands include: Backward Field, Back Space, Cursor Down, and Cursor Up, which defines the cursor's position "relative" to its former position. Absolute cursor positioning places the cursor in a location whose X and Y coordinates are explicitly defined in the instruction. Other editing commands include: Insert/delete a character/line, erase a line/area/display, and protect a selected area. The CTM-300 also includes a scroll feature which will cause the display to be scrolled up one line when a Carriage Return (CR) command is issued while the cursor is in the bottom-most line of the display.

The full usable command set of the CTM-300/R is shown below, and conforms to the ANSI standard X3.64. Moreover the CTM-300/R includes 2K bytes of user RAM into which the user can download custom functions. These user-defined functions are executed by a special Execute User Function command. The terminal firmware can be replaced with 20K bytes of user installed ROM/RAM loaded with the user's custom firmware.

## COMMAND SET

Self Test
Unlock Keyboard
Lock Keyboard
Start Protected Field
End Protected Field
Protect Selected Area
Protect Field
Insert Character
Insert Line
Delete Character
Delete Line
Clear Selected Area
Clear to End of Screen
Clear from Beginning of Screen to Cursor
Clear Screen
Clear Protected Only
Clear Unprotected Only
Clear to End of Line
Clear from Start of Line to Cursor
Clear Line
Clear Protected Fields on Line
Clear Unprotected Fields on Line
Auto Line Feed On/Off
Start of Selected Area
End of Selected Area
Read Back Selected Area
Define Scrolling Area
Set Tab
Clear Tab
Clear All Tabs
Back Tab
Tab
Cursor Left
Cursor Down
Cursor Up
Cursor Right
Cursor to Left of Line
Cursor Home
Set Cursor Position
Read Cursor Position
Set Line Number
Set Column Number
Set Color
Set Cursor On/Off
Read Light Pen
Connect to Printer
Set Alternate Character Set
Set Standard Character Set
Load Character Set'Map
Load User Defined Function
Execute User Function
Load Screen Format
Beep

## COMPUTER INTERFACE

The CTM-300 communicates with the host computer via an RS-232C serial interface, which can be configured by switches for several modes of operation. Input and output parity is selectable as even, odd, or no parity; and the user can choose one or two stop bits. Both full and half duplex operation are possible and the unit can be operated in an on-line or off-line mode. The user can also select the baud rate which can be from 110 baud to 19.2K baud.

## PRINTER INTERFACE

Any Centronics-compatible printer using positive logic can be connected to the CTM-300. In addition to the parallel ASCII inputs, the unit provides a strobe output and a Busy Input.

## LIGHT PEN INTERFACE

User-display interaction is possible through the use of a high speed light pen. When the user points the light pen at an illuminated spot on the CRT, the CTM-300 loads the screen coordinates into an internal light pen register. The pen position may then be read by the processor. Note that the light pen can only be used with monitors having short persistence phosphors.

## PROGRAMMING

Functions that are not normally changed during actual operation are set by a series of switches located on the CTM-300 mother board (table 1). 2K bytes of user RAM is also available for the user to define special functions. The CTM-300 accepts data, from the host computer, in Intel Hex Format.

| SWITCH | NUMBER | DESCRIPTION |
|---|---|---|
| SW0 | 1 | Selected baud rate (110 — 19.2K baud) |
| | 2 | |
| | 3 | |
| | 4 | Select number of bits per character (7/8) |
| | 5 | Select parity (on/off) |
| | 6 | Select parity (even/odd) |
| | 7 | Select number of stop bits (1/2) |
| | 8 | Select full/half duplex |
| SW1 | 1 | Select control mode (normal/monitor) |
| | 2 | Select terminal mode (local/on-line) |
| | 3 | Select cursor (steady/blinking) |
| | 4 | Select cursor (underline/block) |
| | 5 | Select number of characters per line (80/132) |
| | 6 | Select transmission protocol (XON-XOFF/RTS-CTS) |
| | 7 | Enable key click |
| | 8 | Select display mode (interlaced/non-interlaced) |

Table 1. Programming switches description

# SPECIFICATIONS

**DISPLAY**

| PARAMETER | RESTRICTION |
|---|---|
| Resolution | 4000 characters |
| Characters per Line | 80 standard, 132 max. |
| Lines per Page | 25 standard, 50 max. |
| Character Matrix Size | 5 x 7, 7 x 9 dots |
| Character Set | 256 upper/lower case alphanumeric and graphic characters |
| Languages | English, French, Spanish, German, Greek, Swedish |
| Foreground Colors | Red, green, blue, magenta, yellow, white, cyan, black |
| Background Colors | Red, green, blue, magenta, yellow, white, cyan, black |
| Cursor | Displayed/non-displayed, block/underline |

**KEYBOARD**

| PARAMETER | DESCRIPTION |
|---|---|
| Total Keys | 101 keys |
| Keyboard Layout | Standard typewriter layout with sculptured key design |
| Numeric Keypad | 0 — 9 with minus sign and decimal point |
| Cursor Controls | Up, down, left, right |
| Special Function Keys | Break, print, escape, control, insert, delete, clear home, rub out, line feed |
| User Function Keys | 18 programmable user function keys — originally set as color selection keys |

**MONITOR***

| PARAMETER | DESCRIPTION |
|---|---|
| Screen Size | 12 in. diagonal |
| Gun Type | In-line electron guns |
| Shadow Mask | .3mm high resolution shadow mask |
| Controls | Front mounted brightness and volume controls |
| Audio Outputs | Audible key click and beep |

**INTERFACES**

| INTERFACE | DESCRIPTION | MATING CONNECTOR |
|---|---|---|
| Host Computer (J1) | RS-232C and 20mA current loop | DB-25 type connector (male) |
| Parallel Printer (J2) | Centronics compatible | DB-25 type connector (male) |
| Light Pen (J3) | 10 pin header | AMP 102184-3 |
| TTL Video (J4) | 10 pin header | AMP 102184-3 |
| Analog Video (J5) | 10 pin header | AMP 102184-3 |

**MECHANICAL**

| PART | DESCRIPTION | SIZE |
|---|---|---|
| Monitor | Height | 36.3 cm (14.3 in) |
| | Width | 43.5 cm (17.5 in) |
| | Depth | 42.0 cm (16.4 in) |
| | Weight | 12.3 kg (27.0 lb) |
| Keyboard | Height | 8.5 cm ( 3.4 in) |
| | Width | 50.4 cm (19.7 in) |
| | Depth | 24.0 cm ( 9.5 in) |
| | Weight | 5.2 kg (11.5 lb) |

**OPERATING**

| PARAMETER | DESCRIPTION |
|---|---|
| Operating Temperature | 10 — 40°C |
| Relative Humidity | 10 — 90% |
| Power Requirements | 115V, 60 Hz AC @ 50W (American Standard)<br>230V, 50 Hz AC @ 50W (European Standard) |

**ORDERING INFORMATION**

The CTM-300 terminal consists of a 12" color monitor (MEC-12), keyboard with electronics (CTM-300), monitor base (CBS-300), and interconnecting cable assembly (KBL-4).

CTM-300X-X

- AS — American standard (60 Hz)
- ES — European standard (50 Hz)
- M — Complete Color CRT Terminal
- No Suffix — Color Tubeless Terminal (no monitor)

**SUPPORT PRODUCTS**

LP-600 High Speed Light Pen



*Monitor can be replaced by the user

VT-100 Digital Equipment Corp. TM

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

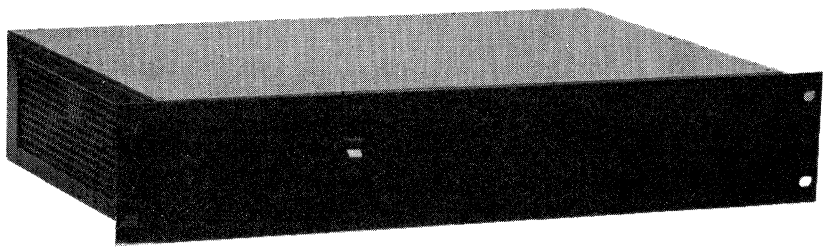
# CTM-300/R

## RACK-MOUNT INTELLIGENT COLOR ALPHANUMERIC TERMINAL

- **8-color alphanumeric display**
- **Programmable display format**
- **On-board Z-80A CPU**
- **256 different displayable characters**
- **ANSI standard firmware**
- **RS-232C input**
- **RGB color output (RS-170)**
- **Keyboard, printer, and light pen interfaces**
- **2K byte program download**
- **50/60 Hz operation**
- **19" rack-mount**
- **Blink, extended height, underline, and protected character attributes**

The Matrox CTM-300/R is an intelligent color alphanumeric terminal controller. The electronics are contained on a single PC board which is mounted in a 19" steel enclosure, complete with a self-contained power supply. When interfaced to an external keyboard and color CRT monitor, the CTM-300/R provides all of the features of an intelligent black and white terminal with the addition of color. The CTM-300/R supports 256 different displayable characters which include all of the alphanumeric characters and punctuation symbols for displaying text in one of six languages; English, French, Spanish, German, Greek, or Swedish. A set of graphic symbols are also supported by the CTM-300/R to enable the user to generate "character-oriented" graphic displays (business forms, process loop displays, bar charts, etc.).

The CTM-300/R firmware conforms to ANSI X3.64 and includes a comprehensive set of cursor, erase, and character attribute controls which facilitate text editing. The on-board firmware also configures the video output to produce a standard display format of 80 characters per line by 25 lines. A unique program download feature, together with a series of DIP switches, enables the user to adapt most of the CTM-300/R functions to conform to his specific requirements.



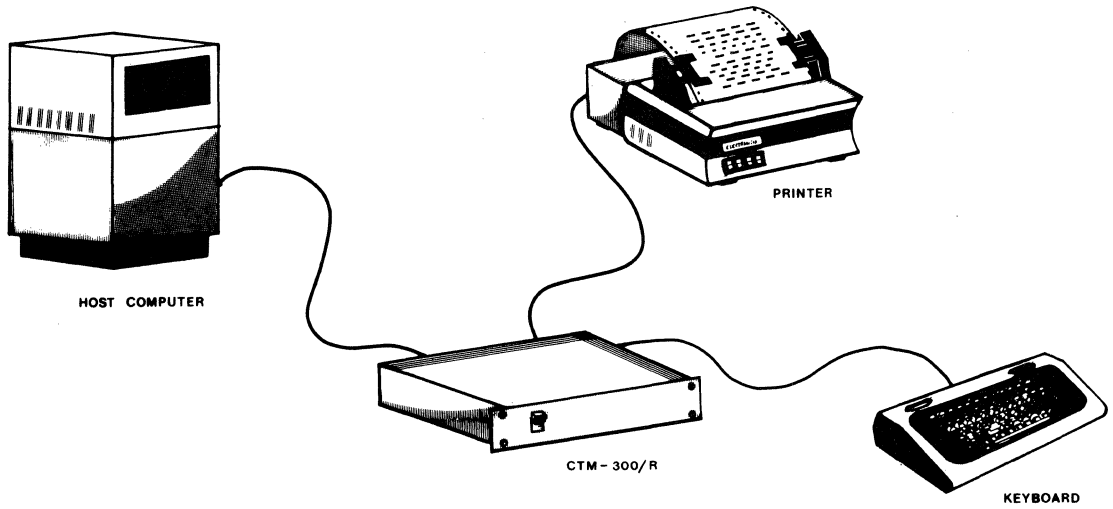



Figure 1. CTM-300/R Intelligent Color Terminal — Typical system configuration

## DISPLAY

The CTM-300/R generates a color alphanumeric display consisting of 25 horizontal lines with 80/132 characters (switch selectable) displayed per line. These parameters, however, can be redefined by the user to accomodate virtually any configuration of characters/line and lines/page up to maximum of 4000 characters per display. Characters can be assigned as blinking, underlined, or protected (protected characters can not be erased or edited while the erasure mode is not in effect). The blink or underline attribute can optionally be replaced (via a hardware strap) by an extended height attribute for displaying double height characters. Furthermore, each character can be assigned to be displayed in one of eight different foreground colors on one of eight different background colors. Color selection (foreground/background) is also user selectable via user function keys on the CTM-300/R.

As supplied, the CTM-300/R contains a font of 256 displayable characters. This character set (figure 2) consists of all the alphanumeric characters and punctuation symbols for displaying text in one of six different languages: English, French, Spanish, German, Greek, or Swedish. The CTM-300/R also includes a set of 32 "graphic characters" which can be used for generating character oriented graphics such as: business forms, process loop displays, bar charts, etc. Moreover, the user can redefine the character set for custom applications by simply replacing the supplied character generator with a 2532 EPROM loaded with his custom character font.

## MONITOR INTERFACE

Two video output connectors are available on the CTM-300/R to drive either a direct drive TTL color monitor, an analog RGB color monitor, or a composite analog monochrome (grey scale) monitor. Separate R,G,B video as well as horizontal and vertical sync signals are provided on the TTL video connector. The polarity of the TTL sync signals can be strapped for either positive or negative logic. On-board circuitry is also provided to allow the user to program the exact sync width and position, for use in non-standard monitors.

A separate 1Vp-p composite video signal is provided which permits monochrome displays with up to 8 different grey levels. Sync polarity on the composite signal is fixed to negative going.

## KEYBOARD INTERFACE

An on-board 8-bit parallel port latches data from an external keyboard in response to a negative going strobe from the keyboard. The resident Z-80A CPU, signaled via an interrupt generated by the keyboard strobe, can then read the keyboard buffer. The keyboard interfaces to the CTM-300/R via a DB-25 connector on the back of the rack-mount box.

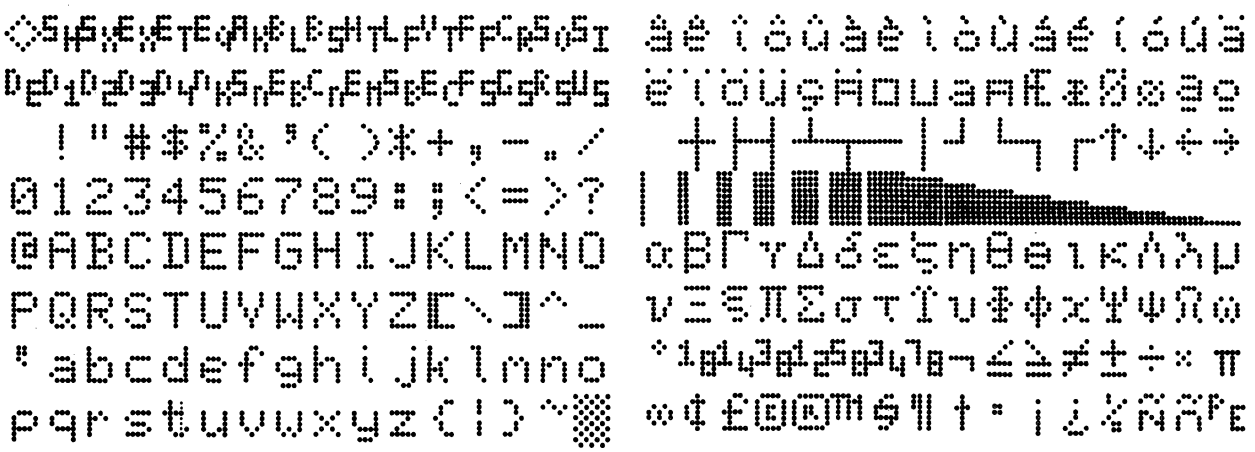


Figure 2. CTM-300/R Character set

## EDITING

The CTM-300/R includes a comprehensive set of cursor, erase, and character attribute controls which facilitate text editing. Cursor control commands enable the user to redefine the position of the cursor using either "relative" or "absolute" movement commands. Relative cursor movement commands include: Backward Field, Back Space, Cursor Down, and Cursor Up, which defines the cursor's position "relative" to its former position. Absolute cursor positioning places the cursor in a location whose X and Y coordinates are explicitly defined in the instruction. Other editing commands include: Insert/delete a character/line, erase a line/area/display, and protect a selected area. The CTM-300/R also includes a scroll feature which will cause the display to be scrolled up one line when a Carriage Return (CR) command is issued while the cursor is in the bottom-most line of the display.

The full usable command set of the CTM-300/R is shown below, and conforms to the ANSI standard X3.64. Moreover the CTM-300/R includes 2K bytes of user RAM into which the user can download custom functions. These user-defined functions are executed by a special Execute User Function command. The terminal firmware can be replaced with 20K bytes of user installed ROM/RAM loaded with the user's custom firmware.

## COMMAND SET

Self Test
Unlock Keyboard
Lock Keyboard
Start Protected Field
End Protected Field
Protect Selected Area
Protect Field
Insert Character
Insert Line
Delete Character
Delete Line
Clear Selected Area
Clear to End of Screen
Clear from Beginning of Screen to Cursor
Clear Screen
Clear Protected Only
Clear Unprotected Only
Clear to End of Line
Clear from Start of Line to Cursor
Clear Line
Clear Protected Fields on Line
Clear Unprotected Fields on Line
Auto Line Feed On/Off
Start of Selected Area
End of Selected Area
Read Back Selected Area
Define Scrolling Area
Set Tab
Clear Tab
Clear All Tabs
Back Tab
Tab
Cursor Left
Cursor Down
Cursor Up
Cursor Right
Cursor to Left of Line
Cursor Home
Set Cursor Position
Read Cursor Position
Set Line Number
Set Column Number
Set Color
Set Cursor On/Off
Read Light Pen
Connect to Printer
Set Alternate Character Set
Set Standard Character Set
Load Character Set Map
Load User Defined Function
Execute User Function
Load Screen Format
Beep

## COMPUTER INTERFACE

The CTM-300/R communicates with the host computer via an RS-232C serial interface, which can be configured by switches for several modes of operation. Input and output parity is selectable as even, odd, or no parity; and the user can choose one or two stop bits. Both full and half duplex operation are possible and the unit can be operated in an on-line or off-line mode. The user can also select the baud rate which can be from 110 baud to 19.2K baud.

## PRINTER INTERFACE

Any Centronics-compatible printer using positive logic can be connected to the CTM-300/R. In addition to the parallel ASCII inputs, the unit provides a strobe output and a Busy Input.

## LIGHT PEN INTERFACE

User-display interaction is possible through the use of a high speed light pen. When the user points the light pen at an illuminated spot on the CRT, the CTM-300/R loads the screen coordinates into an internal light pen register. The pen position may then be read by the processor. Note that the light pen can only be used with monitors having short persistence phosphors.

## PROGRAMMING

Functions that are not normally changed during actual operation are set by a series of switches located on the CTM-300/R mother board (table 1). 2K bytes of user RAM is also available for the user to define special functions. The CTM-300/R accepts data, from the host computer, in Intel Hex Format.

| SWITCH | NUMBER | DESCRIPTION |
|---|---|---|
| SW0 | 1 | Select baud rate (110 — 19.2K baud) |
| | 2 | |
| | 3 | |
| | 4 | Select number of bits per character (7/8) |
| | 5 | Select parity (on/off) |
| | 6 | Select parity (even/odd) |
| | 7 | Select number of stop bits (1/2) |
| | 8 | Select full/half duplex |
| SW1 | 1 | Select control mode (normal/monitor) |
| | 2 | Select terminal mode (local/on-line) |
| | 3 | Select cursor (steady/blinking) |
| | 4 | Select cursor (underline/block) |
| | 5 | Select number of characters per line (80/132) |
| | 6 | Select transmission protocol (XON-XOFF/RTS-CTS) |
| | 7 | Enable key click |
| | 8 | Seleot display mode (interlaced/non-interlaced) |

Table 1. Programming switches description

# SPECIFICATIONS

## DISPLAY PARAMETERS

| PARAMETER | RESTRICTION |
|---|---|
| Resolution | 4000 characters max. |
| Characters per Line | 80 standard, 132 max. |
| Lines per Page | 25 standard, 50 max. |
| Character Matrix Size | 5 x 7, 7 x 9 dots |
| Character Set | 256 upper/lower case alphanumeric and graphic characters |
| Languages | English, French, German, Greek, Spanish, Swedish |
| Foreground Colors | Red, green, blue, magenta, yellow, cyan, white, black |
| Background Colors | Red, green, blue, magenta, yellow, cyan, white, black |
| Cursor | Displayed/non-displayed, block/underline, blinking/steady |

## INTERFACES

| INTERFACE | DESCRIPTION | MATING CONNECTOR |
|---|---|---|
| Host Computer (J1) | RS-232C and 20mA current loop | DB-25 type connector (male) |
| Parallel Printer (J2) | Centronics compatible | DB-25 type connector (male) |
| Light Pen (J3) | 10 pin header | AMP 102184-3 |
| TTL Video (J4) | 10 pin header | AMP 102184-3 |
| Analog Video (J5) | 10 pin header | AMP 102184-3 |
| Keyboard Input (J6) | 8-bit parallel port | DB-25 type connector (male) |

## SIZE

## POWER REQUIREMENTS

American standard: 115V, 60 Hz AC @ 50W
European standard: 230V, 50 Hz AC @ 50W

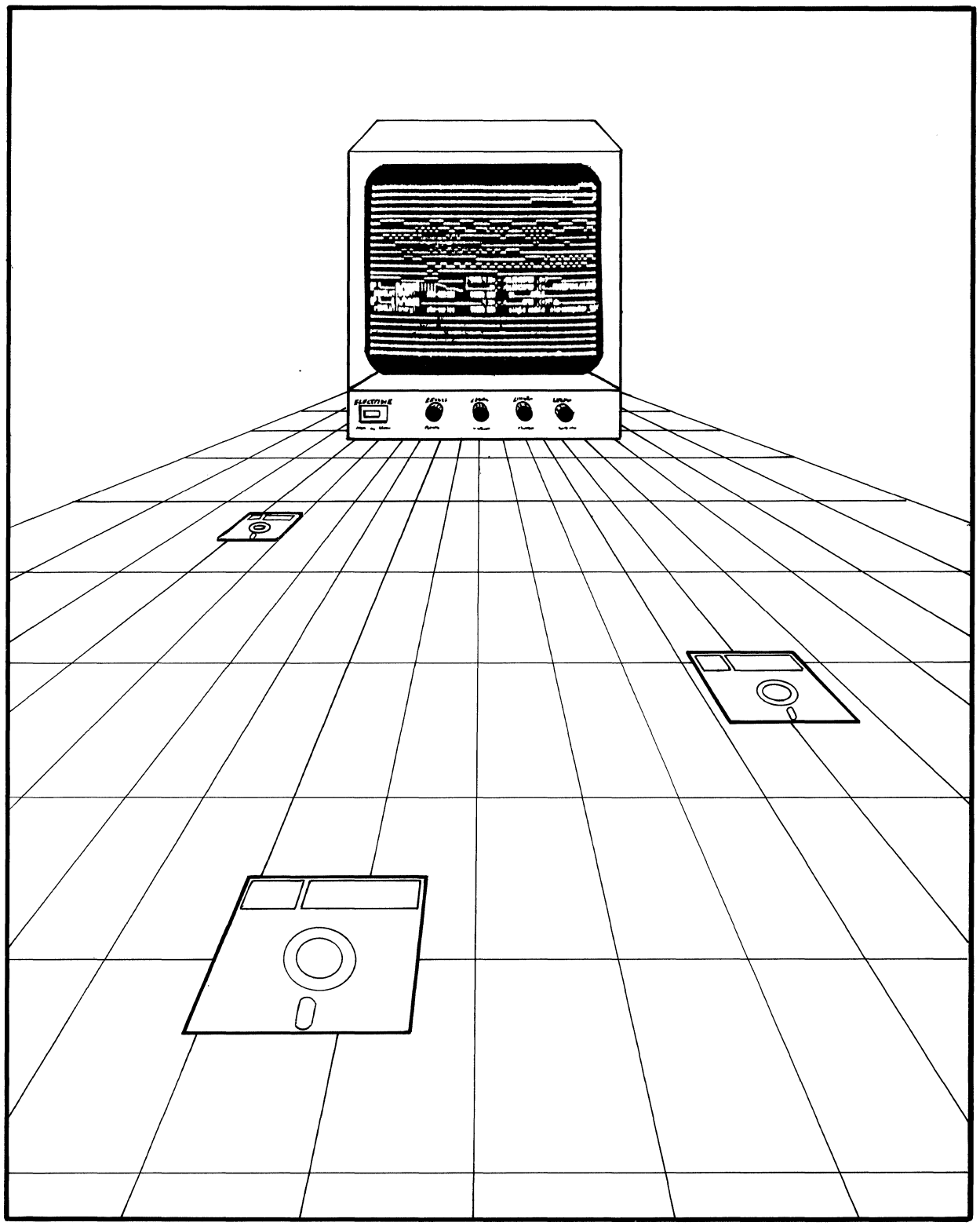
## ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 10° to 40° C
Relative Humidity: 0 to 95% non-condensing

## ORDERING INFORMATION

CTM-300/R-X — 19" rack-mount intelligent color alphanumeric terminal

- A — American standard (60 Hz)
- E — European standard (50 Hz)



# GRAPHICS SOFTWARE

## SECTION 16 GRAPHICS SOFTWARE

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

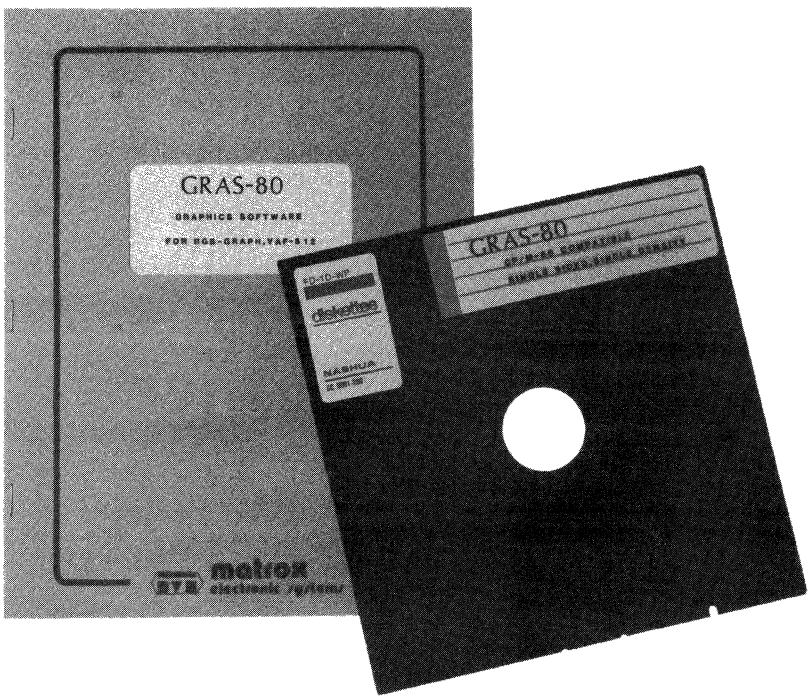
# GRAS-80

## GRAPHICS SOFTWARE PACKAGE FOR RGB-GRAPH AND VAF-512

- **Software support for the RGB-GRAPH/ VAF-512**
- **49 independent subroutines**
- **Draws lines, circles, ellipses, and characters**
- **Light pen and data tablet support routines**
- **Special functions include: pan, scroll, and zoom**
- **Advanced character manipulation including inclined character baseline**
- **Supplied on 8" CP/M compatible diskette**

GRAS-80 is a software package which provides extensive high level graphics facilities to the "C" or MACRO-80 programmer using a Z-80 based CP/M microcomputer system with a Matrox RGB-GRAPH graphics controller.

Subroutines are provided for line drawing, point drawing, arc and ellipse drawing, initializing, panning, zooming, scrolling, and character generation.

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## FUNCTIONAL DESCRIPTION

The GRAS-80 package is a collection of subroutines stored in relocatable library form. Designed to run on a Matrox ZBC-80 CPU in a MACS-10 microcomputer system, it can also be made to work with any Z-80 based CPU board. GRAS-80 version 1.0 can support 1 or 2 RGB-GRAPH boards and one VAF-512 board.

The GRAS-80 routines are provided as a Microsoft compatible library on an 8" CP/M compatible floppy diskette. The GRAS-80 package is mainly written in "C" language, although some sections have been implemented in assembler for increased efficiency. These routines are called, by the user's program, using either the Microsoft Assembler (M80) and Linker (L80) or Whitesmith's "C".

## UTILITY ROUTINES

A set of general purpose Utility Routines are included in GRAS-80 which perform various "house-keeping" functions such as initializing the RGB-GRAPH boards and accessing registers. An initialization routine, Init(), sets the RGB-GRAPH's internal registers to their default values on power-up and/or reset (table 1). Other utility routines enable the user to redefine any or all of these default values and re-initialize using these new values.

| PARAMETER | DESCRIPTION | DEFAULT VALUE |
|---|---|---|
| PAN | Starting column number at left side of display | COLUMN 0 |
| SCROLL | Starting row number at top of display | ROW 0 |
| ZOOM | X and Y zoom factors | X = 1, Y = 1 |
| ASPECT RATIO | Y to X ratio for arcs and ellipses | 1:1 |
| RESOLUTION | X and Y resolution | 512 x 512 |
| ADDRESS | RGB-GRAPH base I/O address | A0H |
| COLOR | Pen color | Red |
| WRITE ENABLE | Enables writing to selected bit planes | All planes enabled |
| BACKGROUND | Background color | Black |
| VIDEO ENABLE | Enables video outputs of selected bit planes | All planes enabled |
| LINE FORMAT | Line texture (solid, dashed, dotted) duty cycle | Solid |
| PEN SIZE | Set size of graphics pen | 1 |
| PEN ASPECT RATIO | Y to X ratio for graphics pen | 1:1 |
| BASE DIRECTION | Base direction for future chain moves | Left to right |
| TEXT ENABLE | Enables alpha mode and select bit plane for text | Alpha mode disabled |
| ALPHA PEN SIZE | Set pen size for alpha mode | 1 |
| ALPHA PEN ASPECT RATIO | Y to X ratio for alpha pen | 1:1 |
| CHARACTER SPACING | Sets horizontal and vertical offsets between characters | Vertical offset = 0, Horizontal offset = 0 |

Table 1. GRAS-80 default values

## BASIC OUTPUT ROUTINES

The Basic Output Routines include 11 independent subroutines that are used for display manipulation. These routines allow the user to draw vectors to the display by simply passing the desired X-Y coordinates, of the vector's endpoint, to the called routine. Short relative vectors (up to 16 pixels in length) can be drawn, point by point, using the Chain() routine. The Chain() routine expects a pointer as its input argument which points to a character buffer that contains a series of chain commands. Each chain command defines a number of chain moves in relative directions (table 2). The Basic Output Routines also permit drawing of arcs and alpha characters to the display by passing the Y size and quadrant code (draws arcs) or an index into the ASCII character table (draw characters). The balance of the Basic Output Routines deal with the user's view of the display. Routines are available to allow the user to pan, scroll, or zoom, the display as well as setting the display resolution and the aspect ratio used for drawing arcs. An Erase routine is also included to preset or clear the visible part of the screen to the background color.

| CHAIN COMMAND | DESCRIPTION |
|---|---|
| CODE = 0 | Chain move in base direction |
| CODE = 1 | Chain move in base direction + 45 degrees |
| CODE = 2 | Chain move in base direction + 90 degrees |
| CODE = 3 | Chain move in base direction + 135 degrees |
| CODE = 4 | Chain move in base direction + 180 degrees |
| CODE = 5 | Chain move in base direction + 225 degrees |
| CODE = 6 | Chain move in base direction + 270 degrees |
| CODE = 7 | Chain move in base direction + 315 degrees |
| CODE = 8 | Turn on WRITE ENABLE flag (subsequent chain moves will be displayed) |
| CODE = 9 | Turn off WRITE ENABLE flag (subsequent chain moves will not be displayed) |
| CODE = 10 | Set number of chain moves encoded per chain command code (1 to 16) |
| CODE = 11 | End of file (terminates chain command) |
| CODE = 12 | Plot point without doing a chain move |
| CODE = 13 | Reserved |
| CODE = 14 | Reserved |
| CODE = 15 | No operation |

Table 1. Chain command code description

**OUTPUT ATTRIBUTE ROUTINES**

The Output Attribute Routines consist of eight independent subroutines that are used to specify parameters controlling the appearance of the display such as line width and line format. These routines allow the user to set the graphics "pen" size and aspect ratio to obtain a pen of virtually any size and shape, from 1 pixel horizontally x 1 pixel vertically to 512 pixels horizontally x 512 vertically. The line format (i.e. solid, dashed, dotted, etc.) is also set in a separate routine, with the exact duty cycle being passed as an argument to the routine. The Output Attribute Routines also sets the displayed colors of both the background video and the graphics pen. Both background and pen color can be independently set to: black, red, blue, magenta, green, yellow, cyan, or white.

**COMPOUND OUTPUT ROUTINES**

The Compound Output Routines are similiar in function to the Basic Output Routines, except that all functions are performed relative to the present cursor position. For example, a line can be drawn by passing X and Y values from the present cursor position (starting endpoint) to the destination endpoint. The Compound Output Routines also enable the user to draw an ellipse to the display by simply passing the ellipse's radius (along the Y axis) as an input argument to the called routine. Two types of chain routines are included in the Compound Output Routines. Tchain() can be used as an alternative to the Chain() routine found in the Basic Output Routines. Cstring() makes succesive calls to Chara() to write to the display the ASCII characters in the buffer pointed to by the pointer passed to the routine.

**ALPHA MODE ROUTINES**

The Alpha Mode Routines provide more advanced character manipulation including writing complete strings, a block cursor that can be positioned, auto line feed, wrap around, sloped baselines for the alpha characters, and a separate size and aspect ratio for characters only. All the special character functions are enabled or disabled by calling the routine Entext(). These routines are useful for terminal emulation.

**INPUT ROUTINES**

GRAS-80 supports a number of graphic input devices (light pen, data tablet, or joystick) through a library of six subroutines. Using these routines, the user can select which device (if more than one input device is used in the system) is active as well as enable a graphics crosshair cursor to be displayed at the XY coordinates obtained from the active input device. The user can also specify, through a separate routine, whether an input XY coordinate will cause a line to be drawn from the last input position to the new position, or whether the cursor will just be moved without otherwise effecting the display.

**VAF-512 ROUTINES**

VAF-512 support routines contained in GRAS-80 enable the user to read or write the entire color look-up tables on the VAF-512 board. The user can also read/write any one of the look-up tables (red, green, or blue) selectively. The VAF-512 library also contains a routine to "grab" a frame of video information, from a TV camera, and load it into the RGB-GRAPH display memory.

**SUMMARY OF GRAS-80 ROUTINES**

**UTILITY ROUTINES**

| NAME | FUNCTION |
|---|---|
| Init | Initializes RGB-GRAPH boards at as-shipped address and sets internal variables for GRAS-80 |
| Pinit | Initializes RGB-GRAPH boards at any base address and sets internal variables for GRAS-80, also sets resolution |
| Setport | Tells GRAS-80 the RGB-GRAPH I/O base address |
| Setreg | Writes data to selected I/O location |
| Setcrtc | Writes data to selected CRTC register |
| Getreg | Reads data from selected I/O location |

**BASIC OUTPUT ROUTINES**

| NAME | FUNCTION |
|---|---|
| Moveto | Absolute pen move with no vector draw |
| Lineto | Absolute pen move with vector draw |
| Chara | Writes a standard character at the current pen position |
| Apan | Absolute horizontal display shift |
| Ascrl | Absolute vertical display shift |
| Zoom | Expands part of the display |
| Chain | Draws a sequence of short relative vectors |
| Arc | Draws 90° of an arc |
| Setaspect | Set the ratio of the Y to X extent fo subsequent arcs and ellipses |
| Setres | Changes the display resolution |
| Erase | Erases the screen and presets it to the current background color |

**OUTPUT ATTRIBUTE ROUTINES**

| NAME | FUNCTION |
|---|---|
| Setcolour | Sets pen color |
| Setwen | Enables writing to selected bit planes |
| Setback | Sets background color to be used after the next Erase |
| Viden | Enables selected video outputs |
| Setdash | Sets line texture as solid or dashed and sets dash duty cycle |
| Setsize | Sets pen size |
| Setpar | Sets pen shape |
| Setdir | Sets base direction for future chains (including characters) |

### COMPOUND OUTPUT ROUTINES

| NAME | FUNCTION |
|---|---|
| Moverel | Moves pen relative to current pen position without drawing vector |
| Linerel | Moves pen relative to current pen position, drawing a vector |
| Rpan | Relative horizontal display shift |
| Rscrl | Relative vertical display shift |
| Ellipse | Draws an ellipse |
| Tchain | Translates ASCII characters to a form that can be used by the Chain command |
| Cstring | Display a string of characters that have previously been put in a buffer |

### ALPHA MODE ROUTINES

| NAME | FUNCTION |
|---|---|
| Entext | Enables or disables alpha mode and selects bit plane for text |
| Setaxy | Assigns values to alpha cursor position variables used by Entext |
| Acmove | When in Alpha mode, moves cursor without writing character |
| Setasize | Sets pen size for alpha mode |
| Setapar | Sets pen shape for alpha mode |
| Setoffs | Sets horizontal and vertical offsets between characters in a string |

### INPUT ROUTINES

| NAME | FUNCTION |
|---|---|
| Activate | Activates the specified input device (light pen, data tablet, or joystick) |
| Deactivate | Deactivates the specified input device |
| Encur | Enables crosshair cursor on specified display memory bit plane(s) |
| Getcoor | Gets one coordinate from the currently activated input device and places it in an external buffer |
| Inkmode | Sets up parameters for input "inking". If mode = 1, the input will cause a line to be drawn from the last input position to the new position, otherwise it will just move the cursor |
| Ink | Starts the input routine |

### VAF-512 ROUTINES

| NAME | FUNCTION |
|---|---|
| Loadcolourmap | Loads all the VAF-512 color look-up tables from an external buffer |
| Readcolourmap | Reads all the VAF-512 color look-up tables to an external buffer |
| Loadc | Loads the specified VAF-512 color look-up table (red, green, or blue) from an external buffer |
| Readc | Reads the specified VAF-512 color look-up table (red, green, or blue) to an external buffer |
| Framegrab | Grabs a frame of video information from a TV camera and places it in the display memory |

### ORDERING INFORMATION

GRAS-80-X/X-X — Graphics software package on an 8" floppy diskette

- A — American operation
- E — European operation

- V — For RGB-GRAPH/VAF-512 display systems
- S — For RGB-GRAPH stand alone systems

- O — Output routines only
- I — Input and output routines

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matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# QUARTO

## GRAPHICS SOFTWARE PACKAGE FOR QRGB-GRAPH

- **Software support package for QRGB-GRAPH**
- **Page-oriented graphics**
- **Supports scaling and windows**
- **Line, point, and character draw and erase commands**
- **Seed area fill**
- **RT-11, RSX-11, TSX, UNIX, and XENIX drivers available**
- **Special functions include: pan, scroll, zoom, and overlay**
- **Advanced character manipulation including inclined character baseline and character rotation**
- **Supplied on an 8" floppy diskette**

QUARTO is a software system for producing line drawings, plotting diagrams and graphs, and for other tasks in which the computer graphics device is used in the manner of a sketchpad and a set of colored pencils. QUARTO provides an extensive set of subroutines for writing graphic plots onto color or monochrome pages of a display, for making the written pages visible, or for hiding them.

QUARTO is designed to be used with a Matrox QRGB-GRAPH graphics display controller card, driven by a PDP-11/LSI-11 (Q-bus or Uni-bus) computer, and either a color or monochrome display monitor.

QUARTO is available for use with RT-11, RSX-11, TSX, TSX-PLUS, UNIX, XENIX, and other operating systems.


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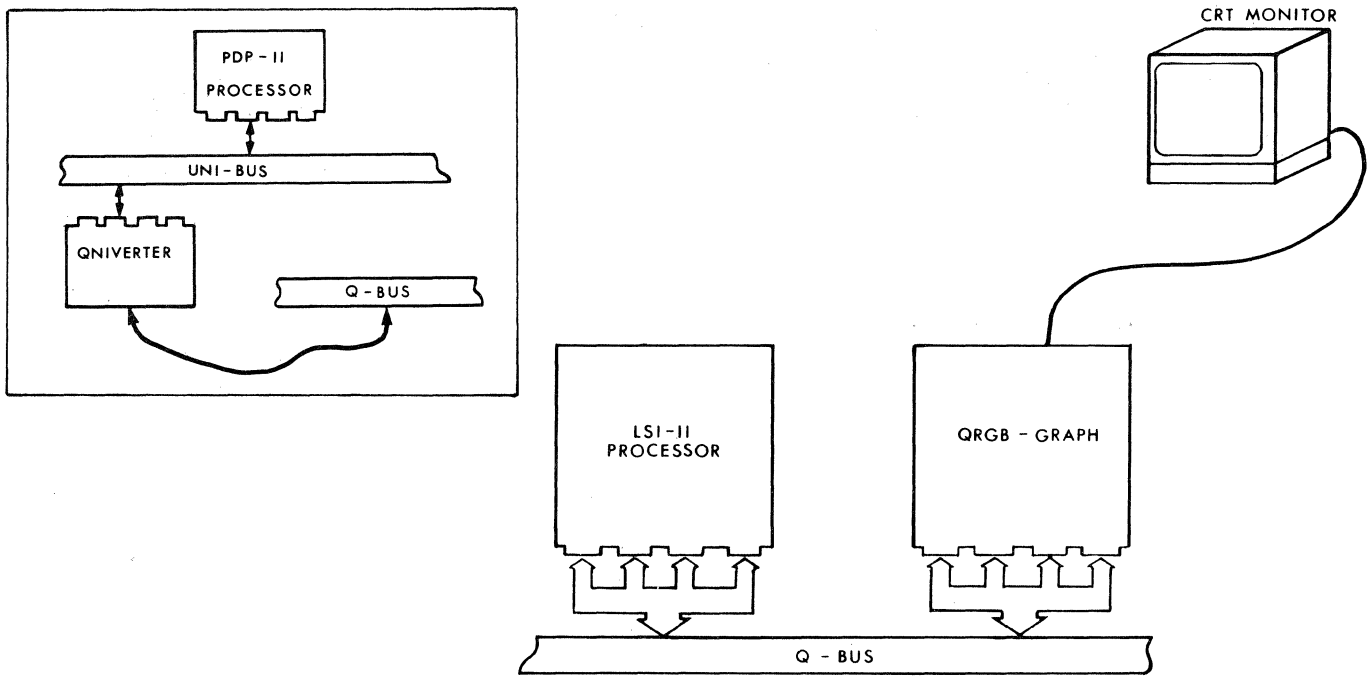


Figure 1. QUARTO — Typical application

## FUNCTIONAL DESCRIPTION

The QUARTO software package is a library of subroutines supplied on an 8" floppy diskette. The QUARTO routines enable the user to create and manipulate graphic video displays, with up to 512 x 512 dot resolution, on a color or monochrome CRT monitor.

QUARTO is designed to be used with a Matrox QRGB-GRAPH graphics CRT display controller board driven by a PDP-11/LSI-11 (Q-bus or Uni-bus) processor, and is available for use with RT-11, RSX-11, TSX, TSX-PLUS, UNIX, XENIX, and other operating systems. QUARTO subroutines are furnished as threaded code and make use of the appropriate operating system library. These routines can generally be called from Fortran, Pascal, C, or assembler-language programs provided the standard system library is available. In addition to the subroutine library, a device driver may be required by certain operating systems. Where needed, the standard QUARTO release package includes such a driver.

The QUARTO software package employs a "paged graphics" technique, whereby the four display planes of the QRGB-GRAPH are grouped together to form one or more "pages" (analogous to sheets of drawing paper), each of which can be written on, erased, cleared, displayed, or otherwise manipulated individually. The four display planes of the QRGB-GRAPH can be configured, by QUARTO, to form eight different combinations of pages (Virtual Machines).

| MACHINE | NUMBER OF PAGES | DESCRIPTION |
|---|---|---|
| 1111 | 4 | Four monochrome pages (one plane each) |
| 2110 | 3 | One four-color page (two planes) and two monochrome pages (one plane each) |
| 2111 | 3 | Same as Machine 2110 except using different colors (different plane-page configuration) |
| 2112 | 3 | Same as Machine 2111 except using different colors (different plane-page configuration) |
| 220 | 2 | Two four-color pages (two planes each) |
| 221 | 2 | Same as Machine 220 except using different colors (different plane-page configuration) |
| 222 | 2 | Same as Machine 221 except using different colors (different plane-page configuration) |
| 31 | 2 | One eight-color page (three planes) and one monochrome plane (one plane) |

Table 1. Virtual Machines supported by QUARTO

## PAGED GRAPHICS

The Paged Graphics routines in QUARTO are used to define and manipulate the working, or "environmental", parameters of the display on a page level. Page control routines allow the user to individually enable the video output from each page, enable/disable writing to each page, or clear a specified page to a specified color. The enable/disable video routine allows several pages to be overlayed on the screen together. Displays may also be combined in many complicated ways by merging the contents of two pages into a single page. In the merging process both pages to be merged are read, pixel by pixel, and rewritten in accordance with whatever logical function the user has chosen to specify. Full or partial images can also be transferred, through QUARTO, between the display and disk.

An initialization routine (QRINIT) loads a set of default parameters for QUARTO (table 2). QRINIT defines such parameters as: currently active Virtual Machine, currently active page, and graphics pen color. Other routines in the Paged Graphics library allow the user to dynamically update these parameters. Routines are included to set the display resolution in terms of virtual coordinates (i.e. X and Y coordinates are expressed in the range of 0 to 1.0) for each page, and to map this virtual window onto a defined portion of the screen. This feature allows the programmer to display several windows on the page simultaneously (figure 2).

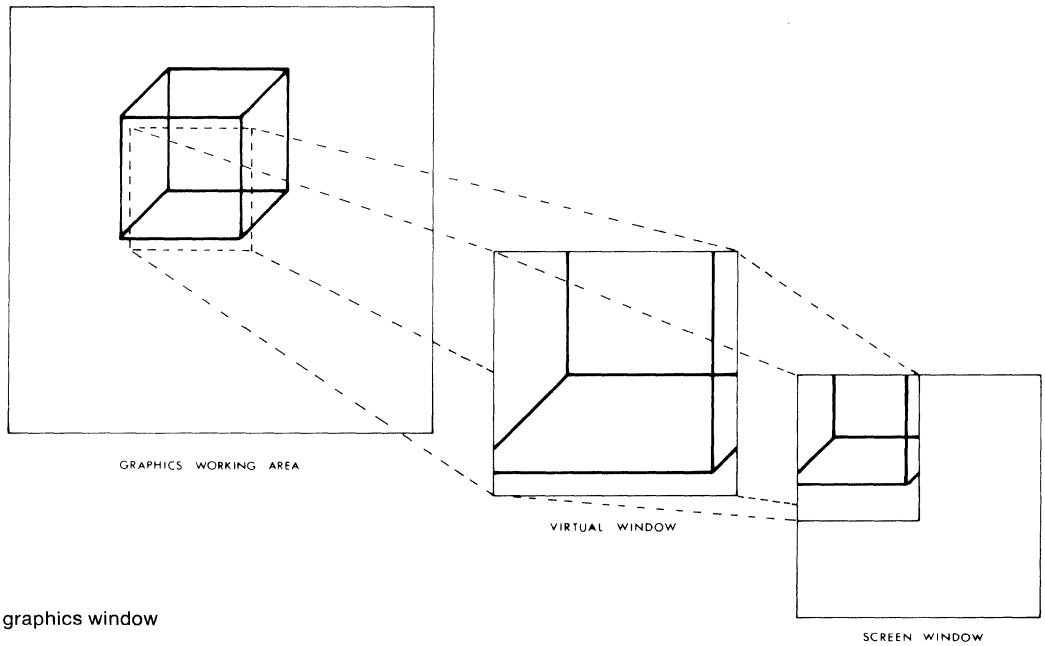


Figure 2. Virtual graphics window

| PARAMETER | DESCRIPTION | DEFAULT VALUE |
|---|---|---|
| PAN | Starting column number at left side of display | Column 0 |
| SCROLL | Starting row number at top of display | Row 0 |
| ZOOM | X and Y zoom factors | X = 1, Y = 1 |
| RESOLUTION | X and Y resolution | 512 x 512 |
| PAGE | Activates page to display | Page 0 active |
| COLOR | Sets pen color | Red |
| VIRTUAL WINDOW | Sets resolution of virtual window | 1.0 x 1.0 |
| SCREEN WINDOW | Sets resolution of screen window | 512 x 512 |
| MACHINE | Select Virtual Machine | 31 |
| POSITION | Set X and Y coordinates of graphics pen | X = 0, Y = 0 |

Table 2. QUARTO default parameters

A separate routine is available to enable the programmer to introduce horizontal and vertical offsets, when drawing characters, to simulate a sloped character baseline.

### VIRTUAL LINE GRAPHICS

Virtual Line Graphics routines are used to actually construct the images on the currently active page. Lines, points, and characters can be written to the display using routines found in the Virtual Line Graphics library. Characters that can be drawn to the display include all of the upper and lower case alphanumeric characters as well as any user-defined characters. Strings of characters can be drawn to the currently active page using powerful character manipulation routines. Characters can be increased in size up to 42 times their normal height and can be rotated, in multiples of 90°, to a maximum of 360°.

Writing to the display is done in one of five modes. In mode 0, the graphics pen is moved along its perscribed route without writing. Mode +1 enables writing in a specified color, regardless of the previous or background color. A Masked Complemented Writing mode (—1) causes each point on the pen route to be written in a color obtained by complementing those bits of the existing color which correspond to zero bits in the specified pen color (eg. a cyan pen (110), writing on a yellow background (011), yields a green (010) line). Modes +2 and —2 refer to Additive Relative Writing and Subtractive Relative Writing respectively. In these modes, the new point color is determined by either adding or subtracting the pen color from the previous point color. An area fill routine (QRVNFL) is also incorporated in QUARTO which allows the use to "color" a defined area of the display. QRVNFL can also be used to copy filled areas between pages.

### PIXEL ADDRESSED GRAPHICS

The Pixel Addressed Graphics subroutines in QUARTO deal with the pixel addresses as integer pixel numbers and may be regarded as being the low-level access to the actual hardware. For applications requiring maximum memory use, graphics at the pixel level can be very advantageous. Where it is desirable to embed these routines in PROM firmware, a separate "embedded code licence" is available.

### DEBUGGING FACILITY

To aid in debugging programs incorporating QUARTO, many of the subroutines supply debugging information to the programmer in the form of error messages displayed at the system console. These error messages are presented in the form of a four character code, of which the first two characters define the error type and the last two characters identify the subroutine.

Parallel versions of subroutines are provided wherever the error reporting facilities have a significant effect on either execution time or code length (routines of the form QDxxxx incorporate debug error reporting). QRxxxx versions of the routines (no error reporting facilities) should be used in the final production program since these routines generally run faster.

# SUMMARY OF QUARTO ROUTINES

## PAGED GRAPHICS ROUTINES

| NAME | FUNCTION |
|---|---|
| QRCPOS<br>QDCPOS | Specify character pen beginning and ending position |
| QRINIT | Initialize all hardware and software parameters |
| QRMERG<br>QDMERG | Merge two pages |
| QRPAGE<br>QDPAGE | Write enable selected page (only one page can be write enabled at one time) |
| QRPCLR<br>QDPCLR | Clear specified page to specified color |
| QRPVEN<br>QDPVEN | Enable/disable video from specified page |
| QRECN<br>QDECN | Select current virtual machine for page graphics |
| QRSAVE<br>QDSAVE | Store specified portion of current picture on disk |
| QRSERS | Disable video from all pages |
| QRSTAT | Display current graphics system status |
| QRSWIN<br>QDSWIN | Define screen window to be used on specified page |
| QRVWIN<br>QDVWIN | Define virtual window to be used on specified page |
| QRWRIT<br>QDWRIT | Restore saved picture from disk to display buffer |

## VIRTUAL LINE GRAPHICS ROUTINES

| NAME | FUNCTION |
|---|---|
| QRCCHR<br>QDCCHR | Draw an array of ASCII characters |
| QRVCHR<br>QDVCHR | Draw an ASCII character |
| QRVLIN<br>QDVLIN | Draw a line in virtual space |
| QRVNFL<br>QDVNFL | Fill an area |
| QRVPNT<br>QDVPNT | Draw a point at the specified virtual coordinates |
| QRVSCH<br>QDVSCH | Draw a user-defined character |
| QRVVCH<br>QDVVCH | Draw a string of user-defined characters |

## PIXEL ADDRESSED GRAPHICS ROUTINES

| NAME | FUNCTION |
|---|---|
| QRACLR<br>QDACLR | Clear specified planes and set to specified color |
| QRHCLP<br>QDHCLP | Enable/disable hardware clipping |
| QRHPAN<br>QDHPAN | Pan display to specified X coordinate |
| QRHSCR<br>QDHSCR | Scroll display to specified Y coordinate |
| QRHZOM<br>QDHZOM | Zoom display by specified zoom factor |
| QRRPDX<br>QDRPDX | Read pixel color from specified location |
| QRSCHV<br>QDSCHV | Draw a user-defined dot matrix character |
| QRSPCH<br>QDSPCH | Draw a dot matrix character |
| QRWPXL<br>QDWPXL | Write a pixel to the specified location in the specified color |
| QRWREN<br>QDWREN | Write enable the specified plane (one plane is enabled per call but any number of planes can be write enabled at any one given time) |
| QRWVCT<br>QDWVCT | Draw a line of pixels |

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## ORDERING INFORMATION

QUARTO — Graphics software package on an 8" floppy diskette. When the QUARTO package is ordered, the user must complete a licensing agreement, and a configuration form.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# PLOT-512

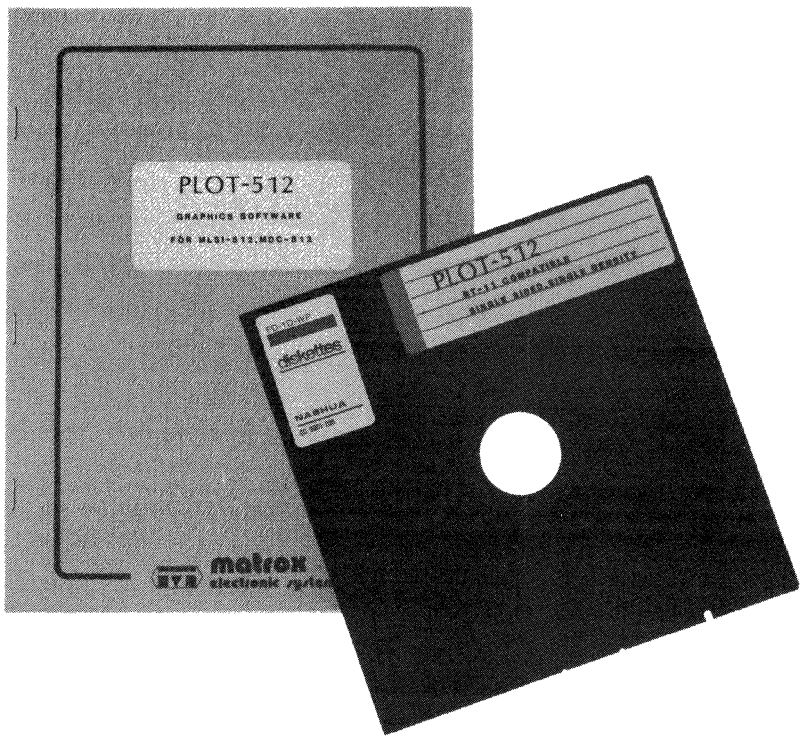
## GRAPHICS SOFTWARE PACKAGE FOR MLSI-512 AND MDC-512

- **Graphics subroutine library**
- **Compatible with MLSI/MDC-512**
- **Line, point, and character draw and erase commands**
- **Compatible with RT-11 operating system**
- **Supplied on 8" diskette**

PLOT-512 is a software package which provides extensive high-level graphics facilities to the RT-11 Fortran or Macro-11 programmer using a PDP-11 or LSI-11 computer equipped with a Matrox MLSI-512 or MDC-512 graphics controller.

The combination of PLOT-512 and a Matrox display controller can be used to add a fast and powerful graphics terminal to any existing PDP-11 or LSI-11 system. Alternatively, a very inexpensive, highly intelligent graphics terminal for general use can be configured around an LSI-11 processor.

PLOT-512 is specifically directed to line graphics; displays consisting of lines, points, and alphanumeric characters. Graphics, curves, and diagrams can be produced quickly so that PLOT-512 is particularly well suited to computer-aided design applications.

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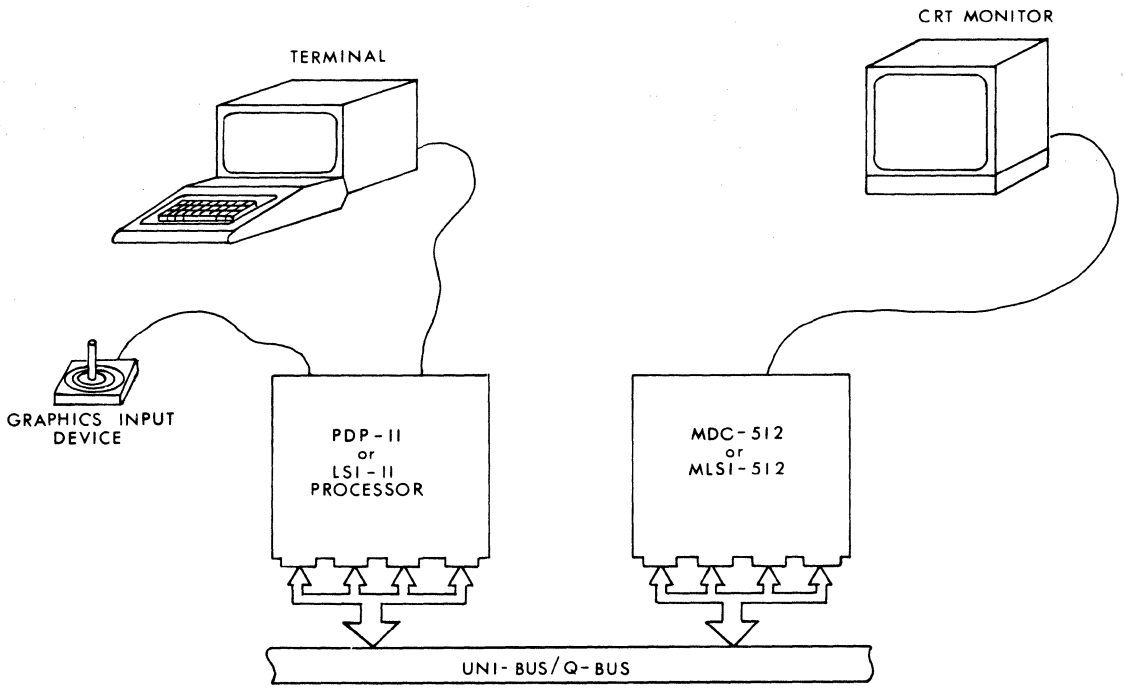



Figure 1. PLOT-512 — Typical application

PLOT-512 is a collection of subroutines stored in relocatable library form. Designed to run in either PDP-11 or LSI-11 computer systems, equipped with a Matrox MDC-512 or MLSI-512 graphics controller board, PLOT-512 supports display formats of up to 512 x 512 dots.

PLOT-512 is line graphics oriented as are the Tektronix, Calcomp, and several other software packages. Although PLOT-512 is not intended to be totally compatible with the Calcomp or Tektronix packages (full compatibility would very likely rob the user of the many powerful features that only raster graphics can provide), PLOT-512 does include a number of subroutines analogous to similarly named and similarly called routines in PLOT-10. Thus conversion of already existing PLOT-10 software should not be difficult, and in many instances should prove unnecessary.

PLOT-512 is provided on a standard 8" diskette in RT-11 format. The PLOT-512 routines are called, by the user's program, using either Macro-11 or Fortran.

## INITIALIZATION

The INITT routine of PLOT-512 initializes all the graphics indexing, sets up buffers, and sets up default values prior to program execution. Another function of the INITT routine clears the entire screen to the default background color.

| NAME | FUNCTION | DEFAULT VALUE |
|---|---|---|
| Pen Color | Color of the graphics pen | Black |
| Background | Color of the background screen | White |
| Controller Address | Base address of the graphics controller board | 175 000$_8$ |
| I/O Address | Address of the parallel interface | 174 000$_8$ |
| Virtual Window Size | Width and height of the virtual window | 512 x 512 |
| Screen Window Size | Width and height of the screen window | 512 x 512 |
| Pixel Size | Width and height of one displayed dot | 2 x 2 |
| TV Standard | Vertical frame refresh rate | 60 Hz American standard |

Table 1. PLOT-512 default values

## DIRECT GRAPHICS

Using the Direct Graphics subroutines, plotting operations are specified using absolute screen locations. To these routines, the plotting range of the program, like the display screen, is seen as an array of 512 x 512 pixels. Direct Graphics routines are generally most useful in writing further, more sophisticated and specialized display routines.

The Direct Graphics routines are made up of four routines; PLOT, PNTABS, MOVABS, and DRWABS. Through these routines the user can draw lines in the current pen color, the complement of the current pen color, or alternating between the current color and its complement (i.e. dotted line). Note that by drawing over a line in the complement pen color, the user can selectively "erase" any line of the display. Routines are also available to enable the user to move the drawing "pen" to a defined location on the screen and display a point (a point is drawn by PLOT-512 as two pixels wide by two pixels high), or to simply move the pen to a new screen coordinate without effecting the display.

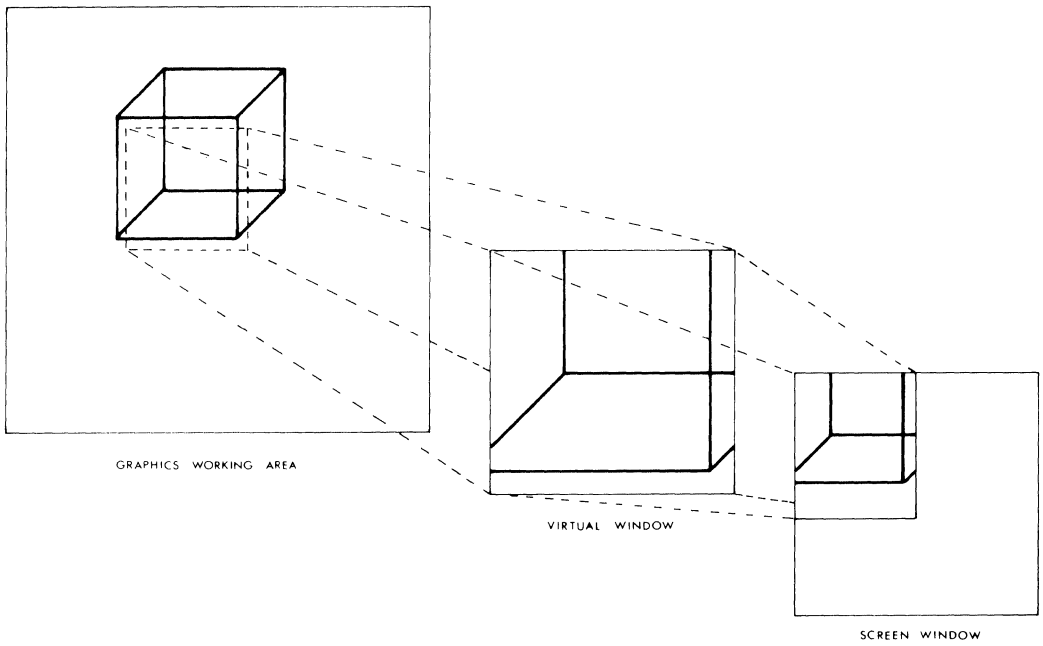



Figure 2. Virtual graphics window

### VIRTUAL GRAPHICS

The Virtual Graphics capabilities of PLOT-512 enable the user to establish a plotting range (within which the program will function normally) which can be larger than the active area of the display screen. A "virtual window" (up to 512 x 512 pixels in size) is then defined within this working area, to represent the portion of the working area that is to be displayed on the screen.

The Virtual Graphics routines include two subroutines, VWINDO and SWINDO, used to define that area of the work space that is to be displayed. VWINDO identifies the size and location of the virtual window. Another routine SWINDO, redefines the screen window such that the user can specify that only a certain portion of the screen is to be employed. The virtual coordinate space, defined by VWINDO, is mapped into the partial screen, defined by SWINDO, and clipping is applied at the edges of the screen window. This feature can be used to plot several displays on the same screen at the same time (eg. several views of an object can be displayed simultaneously).

The basic line drawing routines of the Virtual Graphics portion of PLOT-512; DRAWC, POINTA, MOVEA, and DRAWA, translate directly from the Direct Graphic routines; PLOT, PNTABS, MOVABS, and DRWABS. In the Virtual Graphics routines, however, X and Y coordinates are referred to with respect to their position in the overall working area. A separate routine is maintained to convert these virtual coordinates into actual screen locations.

### ALPHANUMERIC OUTPUT

Alphanumeric characters may be intermixed with the graphics drawings on the display, through the use of the Alphanumeric Output routines. The full upper-case ASCII character set can be generated by PLOT-512 with each character being formed within a 5 x 7 dot matrix. To display a character, the user simply passes the character's ASCII Character Code and X-Y coordinates to the subroutine CHARR. A second routine, ANMODE, is included in PLOT-512 in order to achieve a measure of compatibility with the Tektronix PLOT-10 software package. ANMODE performs no other function in PLOT-512.

### STAND-ALONE ROUTINES

Several basic PLOT-512 routines operate at the pixel level and do not depend on support from the RT-11 operating system. These routines permit the user to extend PLOT-512 and to create custom packages including specialized subroutines. In applications where the memory space is at a premium, there may be advantages to programming directly in these relatively low-level routines. The Stand-Alone routines are accessable to programs operating in a stand-alone environment as well as those intended to be fully supported by the RT-11 system library at run-time.

The Stand-Alone library includes 11 subroutines. An ERASE routine enables the user to clear the entire screen to the current background color. Line drawing routines permit the user to move the pen without drawing a line, draw a point, draw a line, clear a line (draw a line in its complementary color), or draw a dotted line. Further routines are included in the Stand-Alone routines which can draw a box (horizontal width and vertical height of the box are passed as arguments to the routine) or alphanumeric characters to the display.

### GRAPHIC AND ALPHANUMERIC INPUT

Graphics input can be accepted by PLOT-512, through a joystick, track ball, or data tablet, by means of a standard 16-bit parallel interface. The X and Y screen coordinates of the graphics input device are communicated to the PDP/LSI-11 computer as two bytes of a 16-bit word. The graphics cursor (cursor is displayed as a cross hair pattern) is software generated by PLOT-512 in less than one frame period, so that cursor movements appear smooth and continuous.

Provisions have been made in PLOT-512 for formatless input of limited amounts of alphanumeric information through the subroutines INSTRG and TTACC. These routines enable the user to read a line of up to 80 character terminated by a carriage return, from the console terminal.

# SUMMARY OF PLOT-512 ROUTINES

## DIRECT GRAPHICS ROUTINES

| NAME | FUNCTION |
|---|---|
| PLOT | Absolute pen move with vector draw in accordance to line color code, N.<br>N = 1: draw line in complement pen color<br>2: draw line in pen color<br>3: move pen without drawing line<br>4: draw dotted line |
| PNTABS | Absolute pen move with point draw at new pen position |
| MOVABS | Absolute pen move with no vector draw |
| DRWABS | Absolute pen move with vector draw |

## VIRTUAL GRAPHICS ROUTINES

| NAME | FUNCTION |
|---|---|
| VWINDO | Identifies the size and location of the virtual window |
| SWINDO | Defines portion of the screen used for display |
| DRAWC | Virtual pen move with vector draw in accordance to line color code, N.<br>N = 1: draw line in complement pen color<br>2: draw line in pen color<br>3: move pen without drawing line<br>4: draw dotted line |
| POINTA | Virtual pen move with point draw at new pen position |
| MOVEA | Virtual pen move with no vector draw |
| DRAWA | Virtual pen move with vector draw |
| SCRCDT | Performs conversions between virtual and absolute screen coordinates |
| PIXLW | Define pixel size |

## ALPHANUMERIC OUTPUT ROUTINES

| NAME | FUNCTION |
|---|---|
| CHARR | Write a character at the specified pen position |
| ANMODE | No real function. Used only for partial compatability with Tektronix PLOT-10 software |

## STAND-ALONE ROUTINES

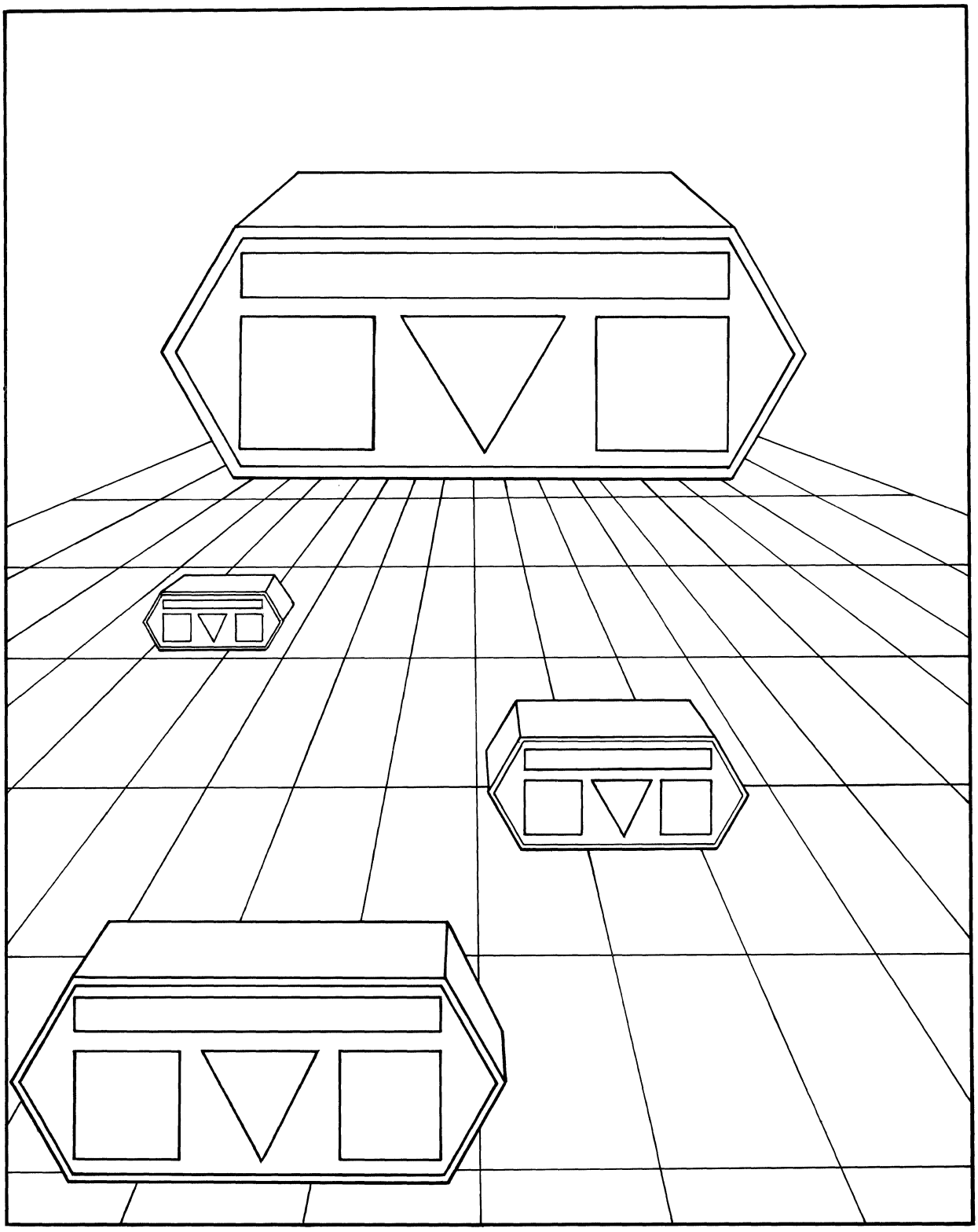
| NAME | FUNCTION |
|---|---|
| ERASE | Clear screen to current background color |
| PENCOL | Complement current pen color |
| BAKCOL | Complement current background color |
| MOVPT | Absolute pen move with no vector draw |
| MPOINT | Absolute pen move with point draw at new pen position |
| LINE | Absolute pen move with vector draw |
| CLINE | Absolute pen move with vector draw using complement of current pen color |
| DLINE | Absolute pen move with vector draw using a dotted line format |
| XLINE | Absolute pen move with vector draw in accordance the line color code, N.<br>N = 1: draw line in complement pen color<br>2: draw line in pen color<br>3: draw dotted line |
| BOX | Draw a box at the current pen position |
| MATCHR | Draw a character at the specified pen position |

## ALPHA/GRAPH INPUT ROUTINES

| NAME | FUNCTION |
|---|---|
| VCURSR | Displays graphics crosshair cursor and accepts input from keyboard |
| DCURSR | Displays graphics crosshair cursor and accepts input from keyboard |
| MATCSR | Displays graphics crosshair cursor and accepts input from keyboard (Does not require support from RT-11 operating system) |
| INSTRG | Accepts a line of alphanumeric data. This data is classified (alpha, numeric, or general) and converted to a standard format |
| TTACC | Reads the console terminal buffer |

## ORDERING INFORMATION

PLOT-512: Complete graphics package on an 8″ floppy diskette.



# APPLICATION NOTES

## APPENDIX A APPLICATION NOTES

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# APPLICATION NOTE #1

# PROGRAMMING CRTC BASED VIDEO CONTROLLER BOARDS



## 1.0 INTRODUCTION

This application note is intended as a programming aid for users of the Matrox RGB-ALPHA and RGB-GRAPH video boards. The information provided here supplements that found in the RGB-ALPHA and RGB-GRAPH Hardware Reference Manuals and provides the basis for understanding how various video display formats may be generated using these cards.

The fundamentals of raster-scan video are explained in Section 2, and the key terms of raster-scan are defined.

The SY6545 CRTC is discussed in detail in Section 3. The function of each internal register is explained with respect to its role in generating the video display.

The remaining sections provide specific examples of programming single and multiple board systems. The general rules for initializing non-standard board/format are also covered.

## 2.0 RASTER SCAN VIDEO

Raster Scan video systems typically use a Cathode Ray Tube (CRT) as the display device. The inside of the display surface of the CRT is coated with phosphor, which, when bombarded with electrons, emits light. The type of phosphor used determines both the color of the light and the duration of the emission (persistence).

In raster systems, the electron beam(s) is cyclically swept across the face of the CRT, from left to right, top to bottom. The cycle time and the persistence of the phosphor must be matched so that the image traced by the raster appears stable. Figure 1 shows the raster scan principle.

At the end of each hozirontal line, a sync pulse is generated to reset the electron beam to the left side of the display. This is the horizontal sync pulse. In order to prevent the retrace from affecting the display, the electron beam is shut off or "blanked" during this interval. This is the horizontal blanking period.

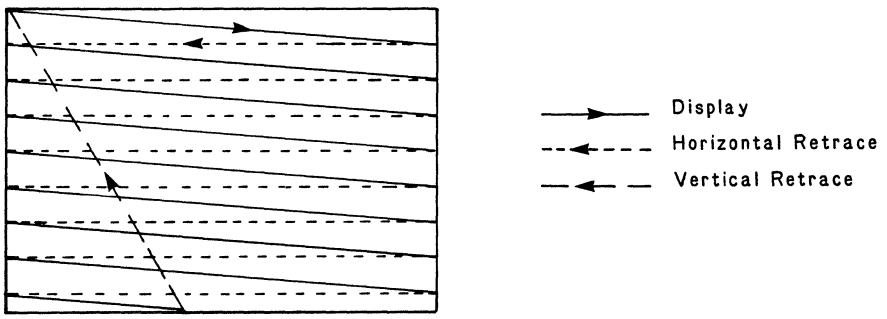



Figure 1. Raster Scan Principle

A

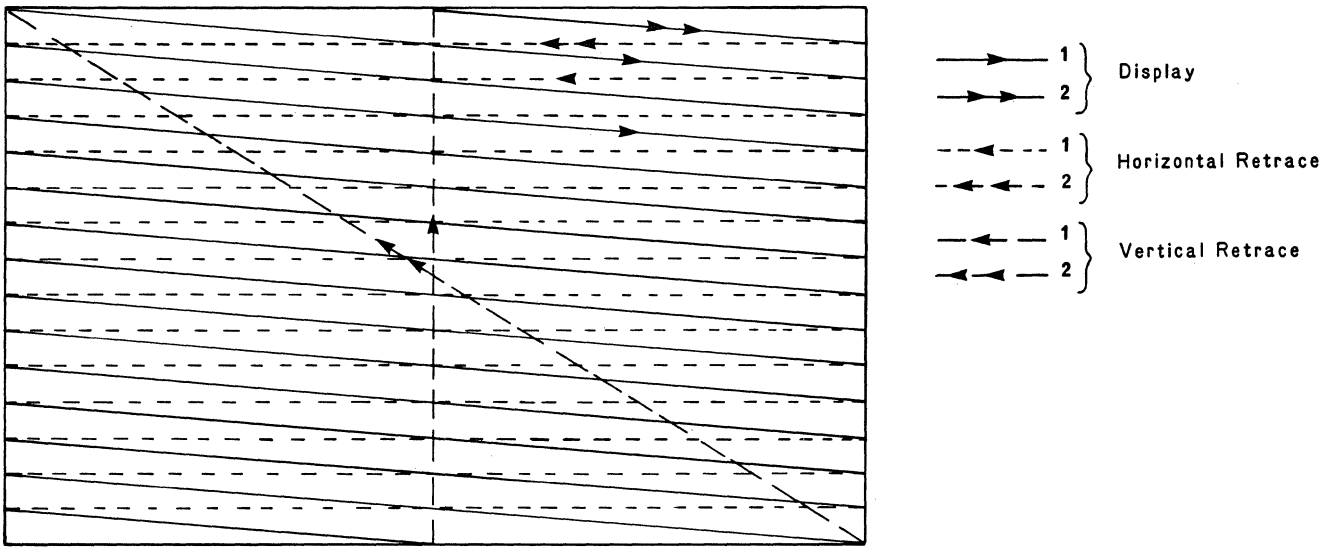



Figure 2. Interlaced Video

Lines of video are generated in this fashion until the electron beam reaches the bottom of the display. A vertical sync pulse is supplied to reposition the beam to the top of the screen and a vertical blanking period is used to "blank" the video during the vertical retrace period.

That portion of the raster that includes one full sweep of the screen from top to bottom is called a "field" of video. The generation of a full image on the screen is called a "frame".

Two conventions exist for generating complete rasters: a non-interlaced raster is one in which the frame rate is equal to the field rate (i.e. one field per frame); an interlaced raster is one in which the frame rate is half of the field rate (i.e. two fields per frame). In an interlaced raster system, two consecutive fields (odd and even) are vertically offset such that the lines of the odd field fill in between the lines of the even field. See figure 2.

**STANDARDS**

Raster timing standards exist and are used by most, but not all, equipment manufacturers. Note that the standards are different for U.S. Broadcast, European Broadcast and U.S. closed circuit.

| VIDEO PARAMETER | | U.S. BROADCAST | EUROPEAN BROADCAST | U.S. CLOSED CIRCUIT |
|---|---|---|---|---|
| LINES/FRAME | Non-Interlaced | 262½ | 312½ | 262½ |
| | Interlaced | 525 | 625 | 525 |
| FRAME RATE | Non-Interlaced | 60Hz | 50Hz | 60Hz |
| | Interlaced | 30Hz | 25Hz | 30Hz |
| VERTICAL FIELD PERIOD (TOTAL) | | 16,667us | 20,000us | 16,667us |
| VERTICAL DISPLAY PERIOD (VISIBLE) | | 15,834us | 18,800us | 15,417us |
| VERTICAL BLANK PERIOD (BLANKED) | | 883us | 1,200us | 1,250us |
| VERTICAL SYNC PULSE WIDTH | | 190.5us | 192.0us | 150.0us |
| HORIZONTAL LINE RATE | | 15.75KHz | 15.625KHz | 15.75KHz |
| HORIZONTAL LINE PERIOD (TOTAL) | | 63.5us | 64.0us | 63.5us |
| HORIZONTAL DISPLAY PERIOD (VISIBLE) | | 52.1us | 51.2us | 53.5us |
| HORIZONTAL BLANK PERIOD (BLANKED) | | 11.4us | 12.8us | 10.0us |
| VERTICAL SYNC POSITION* | | 642.1us | 1,008us | 972.0us |
| HORIZONTAL SYNC POSITION** | | 9.4us | 11.5us | 9.5us |
| HORIZONTAL SYNC PULSE WIDTH | | 5.1us | 5.8us | 4.8us |

*With respect to the end of the vertical blank period
**With respect to the end of the horizontal blank period

**3. THE CRT CONTROLLER**

The CRT controller is an integrated circuit which is responsible for controlling the raster timing parameters as produced by the RGB-ALPHA and RGB-GRAPH video boards. The CRTC contains eighteen read/write registers which must be initialized by the user according to his display format requirements and monitor drive requirements.

In order to display digital data on the CRT, the CRT controller must sector the display into a finite number of display segments. This segmentation takes place at two levels as shown in Figure 3. The screen is divided into coarse units called cells and the cells in turn are segmented into finer units called pixels (picture elements).

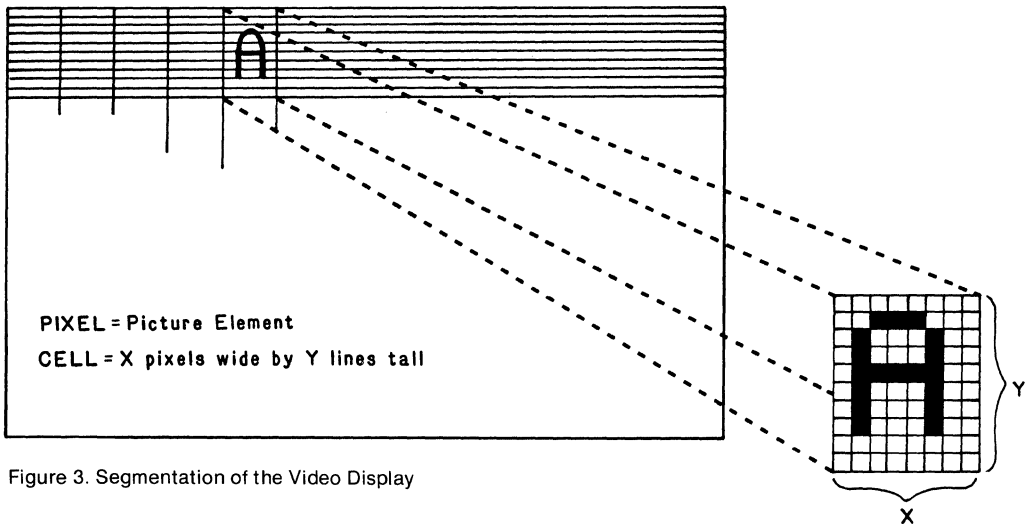



Figure 3. Segmentation of the Video Display

The CRTC has an internal register structure as shown in Figure 4.

The Address register is used to select one of the 18 internal registers and the data register is then used to read or write data to the selected register.

Registers (R0 through R9) are used to set up the raster timing parameters. Refer to figure 5 while reading the text. In order to properly program the CRTC, it is necessary to establish the cell size (X, Y) since many of the internal registers use those cells as a base measure.

Note: There are some slight differences between Hitachi and Synertek parts. Be sure which part is used on your board.

**R0 — Horizontal Total** — This register identifies the number of cells (both visible and blanked) in each horizontal line of video. Since cell numbering starts at 0, the actual value loaded is Ht-1.

**R1 — Horizontal Displayed** — This register stores the number of displayed cells; Hd.

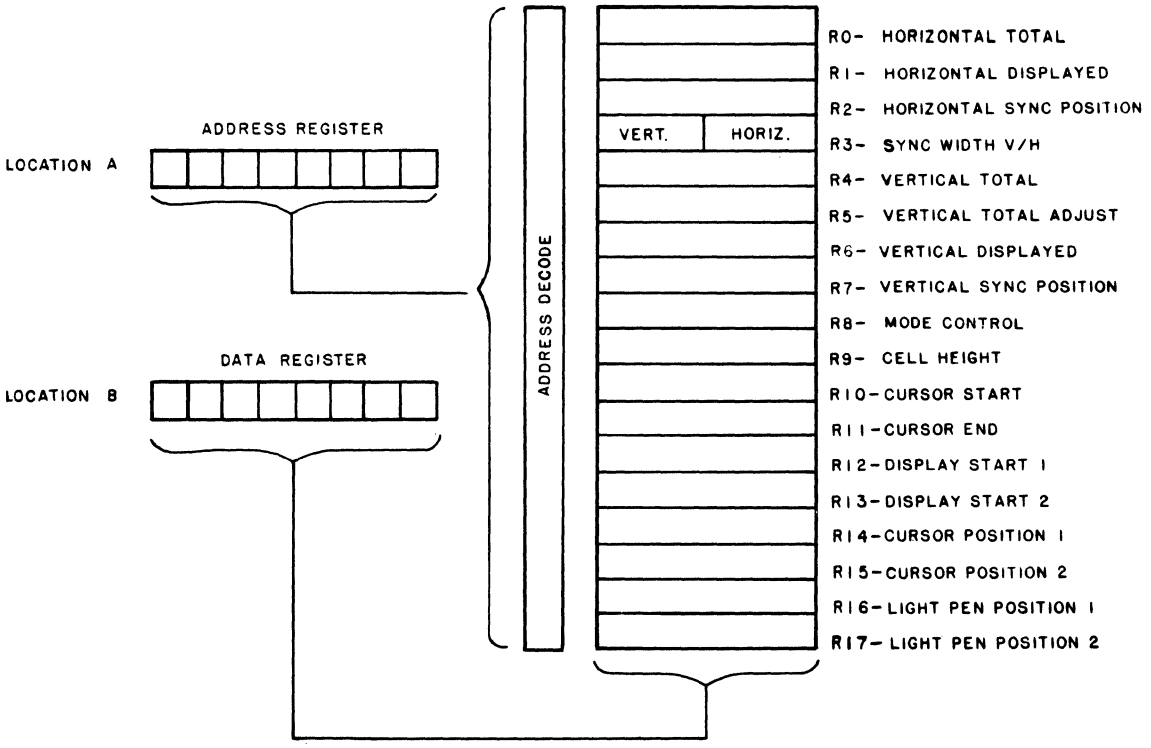



Figure 4. Internal CRTC Register Structure

A

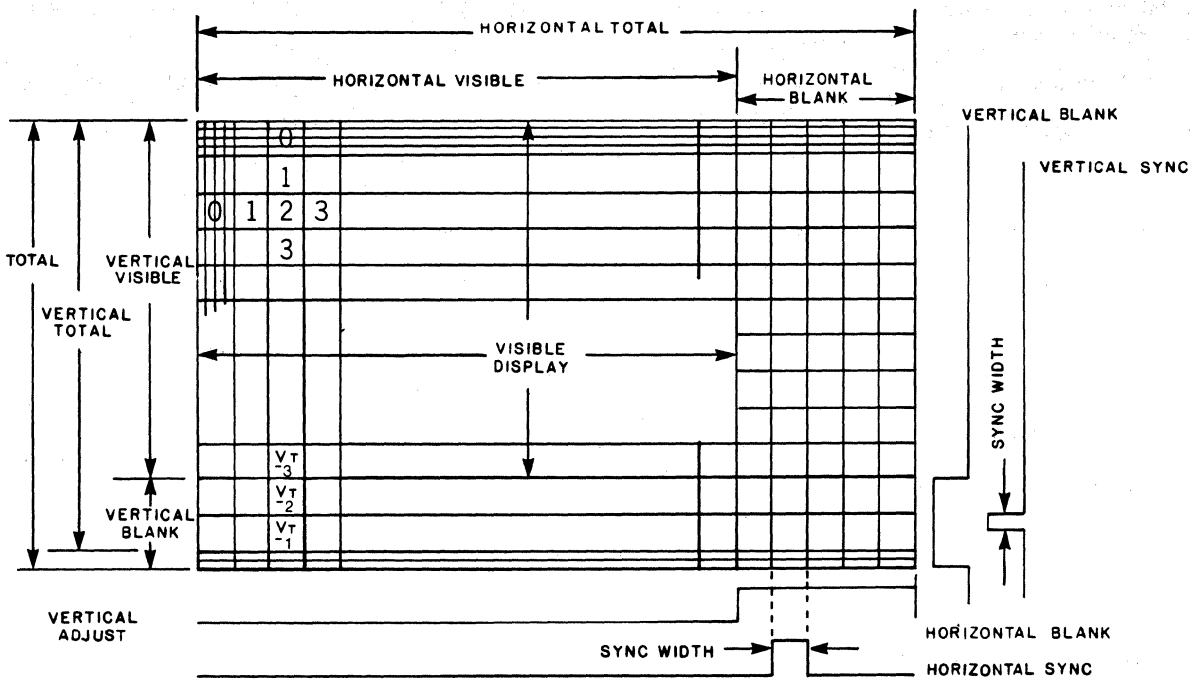



Figure 5. Raster Timing Requirements

**R2 — Horizontal Sync Position** — The horizontal sync position corresponds to the cell number loaded in this register (start position).

**R3 — Sync Width V/H** — The first four bits of this register store the vertical sync width in lines; the second four bits store the horizontal sync width in cells.

**R4 — Vertical Total** — The CRTC uses two registers to identify the total number of lines in the raster. The vertical total register stores the number of complete cells (Vt-1) and any remaining lines (partial cells) are stored in the Vertical Adjust register.

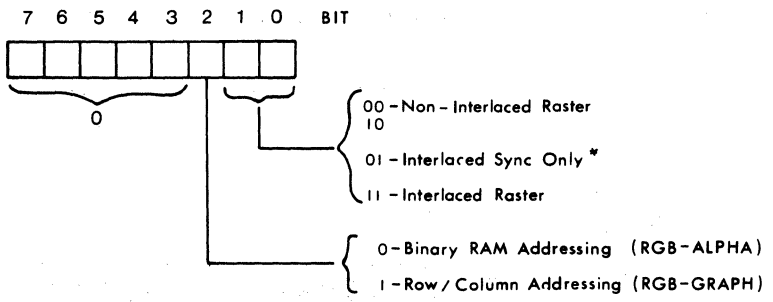
**R5 — Vertical Total Adjust** — If the total vertical lines does not correspond to an integral number of cells, the remaining lines are identified with the Vertical Adjust register. (The adjust lines are added to each field.)

**Note:** In all modes an extra ½ line per field is automatically added to the display by the CRTC.

**R6 — Vertical Displayed** — This register stores the number of vertical cells displayed — Vd.

**R7 — Vertical Sync Position** — This register stores the vertical cell position which contains the vertical sync pulse.

**R8 — Mode Control** — Each bit of this control register performs a different function. For Matrox applications, the upper five bits are always zero and only the lower three bits are relevant.




*Interlaced sync only mode has the same timing as interlaced mode, only the same data is repeated in both the odd and even fields. This mode can be used instead of non-interlaced if a long persistance monitor is used. (Refer to CRTC data sheets for a detailed explanation.

Figure 6. Mode Control Register

**R9 — Cell Height** — This register contains the number of lines per cell (height). Because the cell rows are numbered from zero, the actual value programmed is "# rows — 1".

The other CRTC registers are not relevant to raster timing. Their description can be found in the CRTC data sheets.

**PROGRAMMING DISCREPANCIES**

**Hitachi**

In interlaced mode, the following differences and restrictions apply:

a) H total must be even

b) Cell height must be even (R9 is programmed with # rows — 2)

**Synertek**

In interlaced mode, the following differences and restrictions apply:

**Interlaced Sync & Video** (Row/Column Addressing)

a) Horizontal total must be even

b) Vertical adjust $\longrightarrow$ R5 = R9
R5 = R9 + 1

**Interlaced Sync & Video** (Binary Addressing)

a) Horizontal total must be even

b) Vertical adjust $\longrightarrow$ R5 = R9
R5 = R9 + 1
$R5 = \frac{(R9 + 1)}{2}$
$R5 + 1 = \frac{(R9 + 1)}{2}$

c) Vertical total $\longrightarrow \frac{(\text{Vertical Total} - 1)}{2}$

d) Vertical displayed $\longrightarrow \frac{\text{Vertical Displayed}}{2}$

e) Vertical sync position $\longrightarrow \frac{\text{Vertical Position}}{2}$

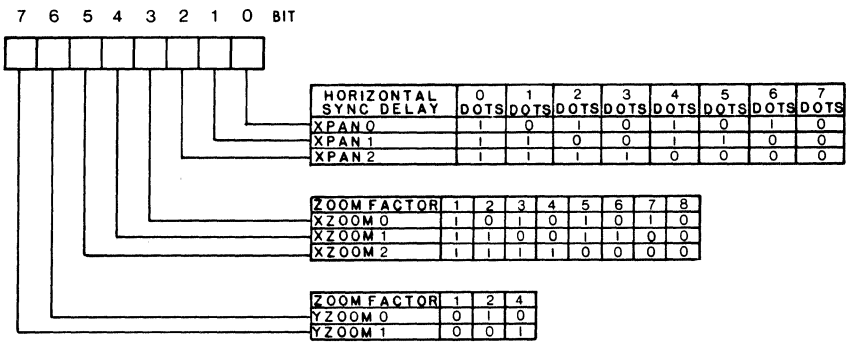
**4.0 RGB-ALPHA**

The RGB-ALPHA is a cell addressable alphanumeric/graphic video controller. The user can format the CRTC to produce virtually any row/column combination as long as the total number of displayed cells is less than 4096; (8192 in unified mode).

The standard character set is implemented in a 5 x 7 dot matrix format with lower case descenders. The recommended minimum cell size is seven (7) pixels wide by ten (10) lines high, but smaller or larger cells can be defined to suit different applications.

In addition to the CRTC, the RGB-ALPHA has two control registers that must be initialized in order to operate the board:

**CONTROL REGISTER 1**

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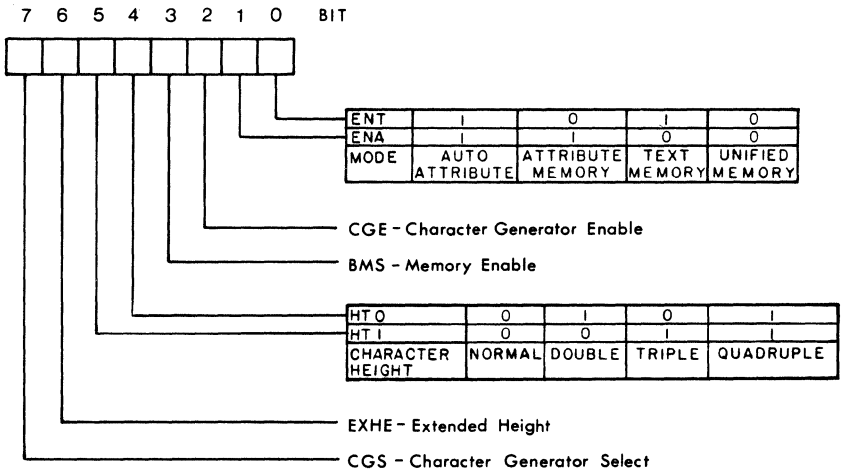
BIT 0 VE: When this bit is zero, all outputs are disabled. When this bit is one, all video outputs are enabled.

BIT 1-3 DT0, DT1, DT2: These bits set the number of dots per cell horizontally. See table above.

BIT 4-7 CK0 — CK3: These bits program the dot clock frequency as a fraction of the crystal clock. See table above.

$$\text{DOT CLOCK FREQUENCY} = \frac{\text{XTAL FREQUENCY}}{\text{DOT CLOCK DIVIDER}}$$

**CONTROL REGISTER 2**




In order to accommodate all possible formats, it may be necessary to change the crystal (XTAL) used in the RGB-ALPHA boards:

Standard: 11.6666 MHz

Optional: 16.0000 MHz
13.3333 MHz
10.0000 MHz

**PROGRAM EXAMPLE**

The needed display format is 24 rows x 80 columns of characters, non-interlaced, in a 7 x 10 pixel cell. A standard (262½)/(525) line, 60 Hz monitor is to be used. The RGB-ALPHA board has a Hitachi CRTC.

**Step 1**

Calculate ideal crystal frequency:

$$\text{XTAL frequency} = \frac{\text{\# of displayed pixels per line}}{\text{visible display time}}$$

$$= \frac{80 \text{ columns} \times 7 \text{ pixels/cell}}{53.5 \text{ usec}}$$

$$= 10.47 \text{ MHz}$$

To ensure monitor compatibility, choose the closest XTAL frequency to 10.47 MHz that is equal to or greater than that value, i.e. 11.6666 MHz.

$$\text{Dot clock divider} = \frac{11.6666}{11.6666} = 1$$

**Step 2**

Calculate the control register and CRTC register parameters (all values in hex):

CTRL 1 1 1 1 1 1 0 0 1 = [F9]

CTRL 2 0 0 0 0 1 0 1 1 = [0B]

CRTC 0 Horizontal Total = Horizontal Total Time x Dot Clock Frequency / Cell Width

$$= \frac{63.5 \text{ usec.} \times 11.6666 \text{ MHz}}{7} = 106$$

$106_{10}$ = 6A

$(H_{TOT} - 1)$ = [69]

CRTC 1 Horizontal Displayed = $80_{10}$ = [50]

CTRC 2 Horizontal Sync Position = 9.5 usec. from end of line (standard)

$$H_{pos} = \frac{(63.5 - 9.5) \times 11.6666 \text{ MHz}}{7} = 90$$

= [5A]

CRTC 3 Sync Width (V/H)

$$V_{SYNC} \text{ (ideal)} = 150 \text{ usec.} = \frac{150}{63.5} = 3 \text{ lines}$$

$$H_{SYNC} \text{ (ideal)} = 4.8 \text{ usec.} = \frac{4.8 \times 11.6666}{7} = 8 \text{ cells}$$

V/H Sync = [38]

CRTC 4 Vertical Total = $\frac{262\frac{1}{2}}{\text{cell height}} = \frac{262\frac{1}{2}}{10} = 26$

$(V_{TOT} - 1)$ = $5_{10}$ = [19]

CRTC 5 Vertical Adjust = $262\frac{1}{2} - (26 \times 10) = 2\frac{1}{2} = 2$

= [02]

CRTC 6 Vertical Displayed = $24_{10}$ = [18]

CRTC 7 Vertical Sync Position = 972 usec. from end of the frame (ideal)

$$V_{pos} = \frac{16{,}667 - 972}{16{,}667} \times 26$$

= 24.5

= $24_{10}$ = [18]

CRTC 8 Mode Control = Non-Interlaced = [00]

CRTC 9 Cell Height = (10 lines — 1) = [09]

**PROGRAM SUMMARY**

| ADDRESS (as shipped) | DATA | ADDRESS (as shipped) | DATA |
|---|---|---|---|
| 9A | F9 | 99 | 19 |
| 9B | 0B | 98 | 05 |
| 98 | 00 | 99 | 02 |
| 99 | 69 | 98 | 06 |
| 98 | 01 | 99 | 18 |
| 99 | 50 | 98 | 07 |
| 98 | 02 | 99 | 18 |
| 99 | 5A | 98 | 08 |
| 98 | 03 | 99 | 00 |
| 99 | 38 | 98 | 09 |
| 98 | 04 | 99 | 09 |

A

**Step 3**
Some formats are not compatible with standard monitor timing. Most monitors will accommodate a variation of about ±5% on the horizontal sync frequency. The vertical refresh rate should be kept very close to the power line frequency to avoid beat frequency interference on the screen. Some monitors will accept a wide variation in vertical sync frequency without distortion.

If your monitor will not accommodate the desired format, the displayed format must be restricted.

For example, in a 525 line/60 Hz North American system, it is impossible to accommodate 512 displayed lines out of 525 total. Typically the displayed number of lines must be limited to 480, if standard sync signals are used.

## 5.0 RGB-GRAPH

The RGB-GRAPH is a pixel addressable graphics video controller. The board can be strapped to provide four different base formats:

512V X 1024H
512V X 512H
256V X 512H
256V X 256H

Within each format, the actual display can be altered using a Zoom control. The Zoom factors available are:

x1, x2, x4 — Vertical
x1, x2, x3, x4, x5, x6, x7, x8 — Horizontal

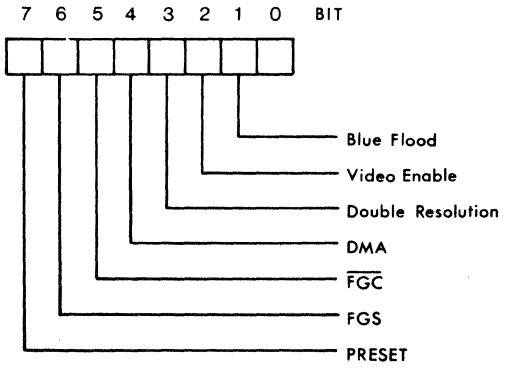
The RGB-GRAPH is designed to operate with a cell size of 8 pixels wide by 8 lines high and must be programmed this way.

The CRTC on the graph board (Synertek) is used to control the sync signals and the zooming operation.

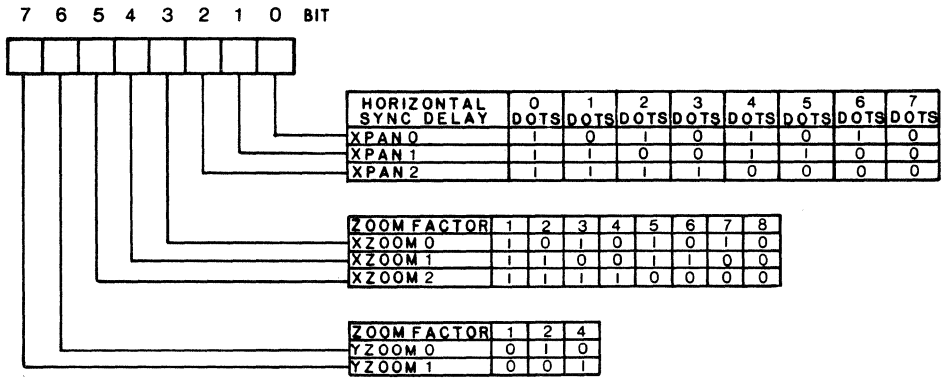
The standard RGB-GRAPH board uses a 10.0000 MHz crystal. For higher frequency XTALs, contact the factory.

In addition to the CRTC, the RGB-GRAPH has four control registers which must be initialized:

**CONTROL REGISTER 1**




**CONTROL REGISTER 2**



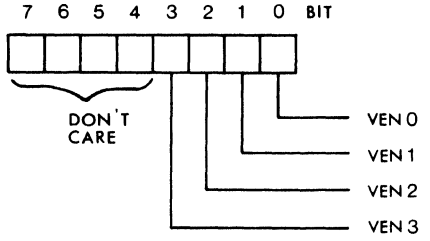

| HORIZONTAL SYNC DELAY | 0 DOTS | 1 DOTS | 2 DOTS | 3 DOTS | 4 DOTS | 5 DOTS | 6 DOTS | 7 DOTS |
|---|---|---|---|---|---|---|---|---|
| XPAN 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| XPAN 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| XPAN 2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

| ZOOM FACTOR | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| XZOOM 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| XZOOM 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| XZOOM 2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

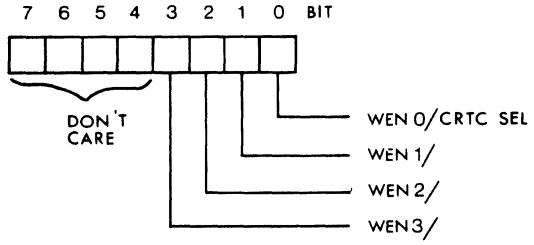
| ZOOM FACTOR | 1 | 2 | 4 |
|---|---|---|---|
| YZOOM 0 | 0 | 1 | 0 |
| YZOOM 1 | 0 | 0 | 1 |

A

**CONTROL REGISTER 3**




**CONTROL REGISTER 4**




**PROGRAM EXAMPLE**

The needed display format is 512 x 512 pixels, interlaced, on a standard European (312½)/(625) line, 50 Hz monitor. The RGB-GRAPH uses a Synertek CRTC.

**Step 1**

CTRL 1 0 0 1 0 0 0 0 0 = [20]

CTRL 2 0 0 1 1 1 1 1 1 = [3F]

CTRL 3 0 0 0 0 1 1 1 1 = [0F]

CTRL 4 0 0 0 0 0 0 0 0 = [00]

CRTC 0 Horizontal Total $= \frac{\text{Horizontal Total Time x Dot Clock Frequency}}{\text{Cell Width}}$

$= \frac{64 \times 10.000}{8} = 80$

$80_{10}$ = 50

(HTOT — 1) = [4F]

CRTC 1 Horizontal Displayed $= \frac{512}{8} = 64$

$64_{10}$ = [40]

CRTC 2 Horizontal Sync Position = 11.5 usec. from the end of the line (standard)

$= \frac{(64 - 11.5) \times 10.000}{8} = 66$

$66_{10}$ = [42]

CRTC 3 Sync Width (V/H)

Vertical Sync (ideal) = 192 usec. $= \frac{192}{64} = 3$ lines

Horizontal Sync (ideal) = 5.8 usec. $= \frac{5.8 \times 10.000}{8} = 7$ cells

V/H Sync = [37]

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CRTC 4 Vertical Total = $\frac{625}{8}$ = 78

$(V_{TOT} - 1)$ = $77_{10}$ = [4D]

CRTC 5 Vertical Adjust = (625 — 1) — (78 x 8) = 0

= [00]

Note: The CRTC adds one line in the interlaced mode.

CRTC 6 Vertical Displayed = $\frac{512}{8}$ = 64

= [40]

CRTC 7 Vertical Sync Position = 1008 usec. from end of frame (ideal)

= $\frac{20000 - 1200}{20000}$ x 78

= [48]

CRTC 8 Mode Control = Interlaced = [07]

CRTC 9 Cell Height = 8 — 1 = [07]

**PROGRAM SUMMARY**

| ADDRESS (as shipped) | DATA |
|---|---|
| A6 | 20 |
| A6 | 20 |
| A7 | 3F |
| A8 | 0F |
| AA | 00 |
| AC | 00 |
| AE | 4F |
| AC | 01 |
| AE | 40 |
| AC | 02 |
| AE | 42 |
| AC | 03 |
| AE | 37 |
| AC | 04 |
| AE | 4D |
| AC | 05 |
| AE | 00 |
| AC | 06 |
| AE | 40 |
| AC | 07 |
| AE | 48 |
| AC | 08 |
| AE | 07 |
| AC | 09 |
| AE | 07 |

**Step 2**

Some formats are not compatible with standard monitor timing. Most monitors will accommodate a variation of about ±5% on the horizontal sync frequency. The vertical refresh rate should be kept very close to the power line frequency to avoid beat frequency interference on the screen. Some monitors will accept a wide variation in vertical sync frequency without distortion.

If your monitor will not accommodate the desired format, the displayed format must be restricted.

For example, in a 525 line/60 Hz North American system, it is impossible to accommodate 512 displayed lines out of 525 total. Typically the displayed number of lines must be limited to 480, if standard sync signals are used.

**6.0 VAF-512**

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The VAF-512 is a graphics support board. This board is designed to increase the performance of the RGB-GRAPH board(s), (and the RGB-ALPHA board).

The board consists of four principle circuits: a frame grabber, a hardware vector generator, a color look-up table, and three 8-bit D/A converters.

**The frame grabber:** digitizes monochrome video information from a camera or a similar source and loads it into the display memory of one or two RGB-GRAPH boards. Once the digitized frame is in the RGB-GRAPH display memory, it can then be manipulated through software by the user.

**The hardware vector generator:** allows straight lines (vectors) to be drawn in virtually any direction with less software overhead than would be required if each pixel in the line was plotted independantly.

**The color look-up table** allows a palette of 256 colors to be chosen by software from a bank of 16 million colors. Programmable via software, the look-up table may be used to create animation without modifying the information stored in the RGB-GRAPH card(s).

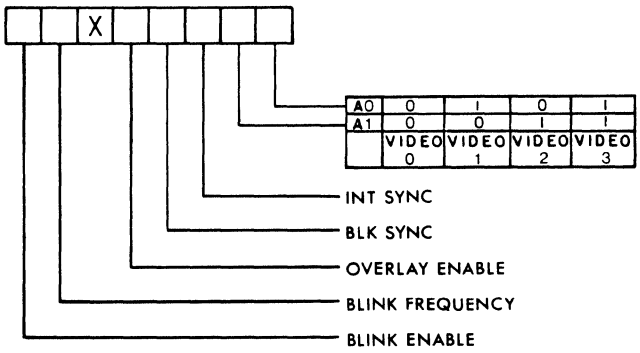
The VAF-512 is designed to operate with up to two RGB-GRAPH boards and one RGB-ALPHA board.

Data is passed between the VAF-512 and the video controller cards on a well organized video bus that is implemented with a single 50 line ribbon cable.

The VAF-512 board uses a 2.5830 MHz crystal for the American Standard, and a 2.5625 MHz crystal for the European Standard.

The VAF-512 does not have a CRTC, and only the "Mode Register" has to be initialized for proper operation. It is also advisable to initialize the Color Look-up Table for ease of picture identification, although it will not hamper system operation.

**MODE REGISTER**




BITS 0 AND 1: A0 AND A1. The user uses these two bits to enable one of the four video inputs to the Frame Grabber.

BIT 2: INT SYNC. When a one is written to this bit, the Frame Grabber's PLL will use the on-board sync source. When a zero is written to this bit, the Frame Grabber's PLL will lock onto the sync in the video signal that the user supplies at the selected video input.

BIT 3: BLK SYNC. When a one is written to this bit, the Frame Grabber's PLL is programmed to lock onto block sync. provided at the selected video input. When a zero is written to this bit, the Frame Grabber's PLL is programmed to lock onto serrated sync. (CCIR/EIA) provided by the on-board sync generator or by external source via the selected video input.

BIT 4: OVERLAYEN: When a one is written to this bit, TTL video signals input via J2-38 through J2-41 are OR'D and gated onto look-up table address line A8. When a zero is written to this bit, A8 is pulled low.

BIT 6: BLINK FREQ: When a one is written to this bit, the blink frequency is programmed to be 3.75 Hz. When a zero is written to this bit, the blink frequency is programmed to be 1.8 Hz.

BIT 7: BLINKEN: When a 1 is written to this bit, the blink frequency is gated onto look-up table address line A9. When a zero is written to the bit A9 is pulled low.

The VAF-512 will not operate without at least one properly initialized RGB-GRAPH connected to the video-bus. The reason being that the VAF-512 requires the horizontal sync pulses generated by the RGB-GRAPH to lock its phase locked loop.

### 7.0 RGB-ALPHA/RGB-GRAPH COMBINATION

For applications requiring extensive graphics and alphanumerics, an RGB-ALPHA and an RGB-GRAPH can be combined to produce an overlayed image. The RGB-ALPHA will provide the foreground color information for the characters and the RGB-GRAPH will provide the background color information. Variations of the above can be accomplished through straps on the RGB-ALPHA and software commands. A description is given in the Hardware Configuration section. For further information, please contact the factory. The method used to synchronize the two boards is such that several programming restrictions must be observed in setting up the raster format.

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The recommended method of putting together a two board system is to start off with two, one board systems. Try operating and programming each of the two boards in a stand-alone master mode. When you have become comfortable with the two cards on their own, then and only then should the two board system be constructed. Use a 10.0 MHz crystal on the RGB-ALPHA board during the preliminary testing to get a proper feeling for the resulting display, since the ALPHA card will be slaved to the 10.0 MHz crystal on the GRAPH card in a two board system also, **the RGB-ALPHA SLAVE must use a Synertek CRTC instead of the Hitachi part.**

### HARDWARE MODIFICATIONS

All RGB-ALPHA boards, level 3 and higher, and all RGB-GRAPH boards level 4 and higher can be mated without any hardware modifications.

Production Modification Bulletins (PMB's) have, in some cases, been implemented on lower level boards to provide full compatibility. Determine the modification level of your boards and consult the chart below:

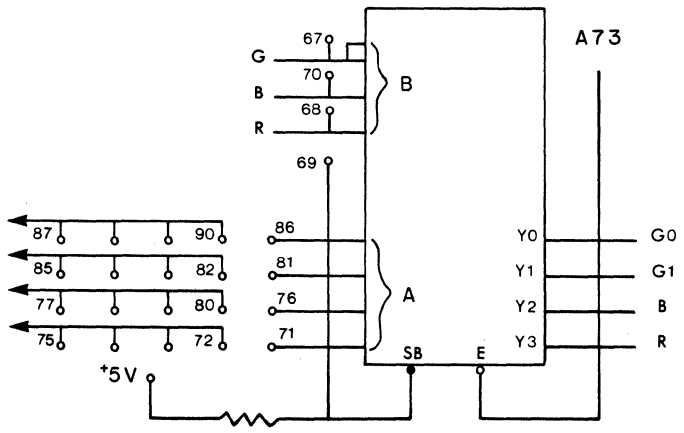
| RGB-ALPHA | | | RGB-GRAPH | | |
|---|---|---|---|---|---|
| **REVISION LEVEL** | **PMB LEVEL** | **INSTRUCTIONS** | **REVISION LEVEL** | **PMB LEVEL** | **INSTRUCTIONS** |
| 1 | | CONSULT FACTORY | 1 | | CONSULT FACTORY |
| 1 | A | " " | 1 | A | " " |
| 1 | AB | " " | 1 | AB | " " |
| 1 | ABC | " " | 1 | | " " |
| 2 | | CONSULT FACTORY | 2 | | CONSULT FACTORY |
| 2 | A | " " | 2 | A | " " |
| 2 | AB | " " | 2 | AB | " " |
| 2 | ABC | " " | 2 | ABC | " " |
| 2 | ABCD | " " | | | |
| 2 | ABCDE | OK | | | |
| | | | 3 | | CONSULT FACTORY |
| 3 & UP | | OK | 3 | A | " " |
| | | | 3 | AB | " " |
| | | | 3 | ABC | " " |
| | | | 4 & UP | | OK |

### HARDWARE CONFIGURATION

1. Disconnect jumper 113-112 on the RGB-ALPHA (this disables the internal clock).
   Connect jumper 111-112 on the RGB-ALPHA (this enables the external clock).

**Note:** in a combined ALPHA/GRAPH configuration, the ALPHA board receives a 10 MHz clock signal from the GRAPH board. Higher XTAL frequencies can not be selected.

2. The graphics input to the RGB-ALPHA must be strapped to select the RGB-GRAPH signal as the background color. All straps are on the RGB-ALPHA board.




To select the "A" input on the A73 multiplexor circuit, pin 69 must be driven low (0 volts). This is accomplished by jumpering pin 69 to ground, or by jumpering pin 69 to one of pins 67, 70 or 68.

In the latter case, one of the RGB-ALPHA background color attribute bits is used to select or deselect the graphics background for each alphanumeric character cell.

| SOURCE | | WIRE WRAP PINS | EXAMPLE STRAPS | WIRE WRAP PINS | DESTINATION |
|---|---|---|---|---|---|
| RGB-GRAPH #1 | J3 PIN 12 | 87 | | 71 | RED |
| | J3 PIN 13 | 88 | | | |
| | J3 PIN 14 | 89 | | | |
| | J3 PIN 15 | 90 | | | |
| RGB-GRAPH #2 | J3 PIN 16 | 85 | | 76 | BLUE |
| | J3 PIN 17 | 84 | | | |
| | J3 PIN 18 | 83 | | | |
| | J3 PIN 19 | 82 | | | |
| RGB-GRAPH #3 | J3 PIN 20 | 77 | | 81 | GREEN 1 |
| | J3 PIN 21 | 78 | | | |
| | J3 PIN 22 | 79 | | | |
| | J3 PIN 23 | 80 | | | |
| RGB-GRAPH #4 | J3 PIN 24 | 75 | | 86 | GREEN 0 |
| | J3 PIN 25 | 74 | | | |
| | J3 PIN 26 | 73 | | | |
| | J3 PIN 27 | 72 | | | |

3. On the RGB-GRAPH board:

a) pins 101-100 must be strapped in order to enable a proper external character clock sync signal

b) pins 107-106 must be strapped in order to enable a proper vertical reset pulse.

c) the video output signals must be strapped to the appropriate J3 lines in order to match the input strapping on the ALPHA board.

| TTL VIDEO | PIN | AS-SHIPPED STRAPS | PIN | J3 PIN |
|---|---|---|---|---|
| 0 | 123 | | 112 | 12 |
| | | | 117 | 16 |
| | | | 122 | 20 |
| | | | 127 | 24 |
| 1 | 118 | | 111 | 13 |
| | | | 116 | 17 |
| | | | 121 | 21 |
| | | | 126 | 25 |
| 2 | 113 | | 110 | 14 |
| | | | 115 | 18 |
| | | | 120 | 22 |
| | | | 125 | 26 |
| 3 | 108 | | 109 | 15 |
| | | | 114 | 19 |
| | | | 119 | 23 |
| | | | 124 | 27 |

**Note:** when using level three and higher ALPHA boards, strap the graphics output to pins 109, 110, 111 and 112.

4. Couple the RGB-GRAPH board to the RGB-ALPHA board using a 50 pin ribbon cable from J3 to J3. The J3 headers are 3M connectors, part no. 3433-1202. The mating connector part number is 3425-7000.

The graphics and alphanumerics video is mixed on the RGB-ALPHA, and the video output for both cards is taken from the RGB-ALPHA. The video socket on all current boards is a 10 pin AMP connector. The mating connector consists of a shell and ten terminals, the part numbers are as follows:

| | | |
|---|---|---|
| Shell | AMP 87922-1 | (1) |
| Terminal | AMP 87667-2 | (10) |

5. On level 4 and higher GRAPH boards, connect post 162 to 163.

## PROGRAMMING CONSIDERATIONS

When the RGB-GRAPH is used with the RGB-ALPHA, the ALPHA board is programmed to drive the monitor, but the GRAPH board is programmed somewhat differently in order to synchronize its output with that of the ALPHA.

### Restrictions

1) Horizontal Total (pixels) must be the same on both the ALPHA and the GRAPH.

2) Vertical Total (lines) must be the same on both the ALPHA and the GRAPH.

3) Horizontal Displayed on ALPHA must be greater than or equal to that on GRAPH.

4) In non-interlaced mode, the vertical adjust on the graph board must be even (i.e. = 0, 2, 4 or 6).

### Differences (RGB-GRAPH) Programming

The RGB-GRAPH is programmed to generate a reset pulse for the CRT controllers once every frame. This pulse is positioned three cells from the end of the last line of video. The width and position of the reset pulse is determined by the horizontal and vertical sync information programmed into the GRAPH board.

| | |
|---|---|
| Horizontal sync | Position $\longrightarrow (H_{TOT} - 4)$ |
| | Width $\longrightarrow$ 1 cell |
| Vertical sync | Position $\longrightarrow V_{TOT}$ (for $V_{adj} > 2$) |
| | $V_{TOT} - 1$ (for $V_{adj} < 2$) |
| | Position $\longrightarrow (V_{adj} + 8) - 1$ |
| | Width $\longrightarrow V_{adj} - 1$ (for $V_{adj} > 2$) |
| | $(V_{adj} + 8) - 1$ (for $V_{adj} < 2$) non-interlaced |
| | $(V_{adj} + 4) - 1$ (for $V_{adj} < 2$) interlaced |

## PROGRAM EXAMPLE

The required display is 512 x 512 graphics with 25 rows x 80 columns alphanumerics (preferably using a 7 x 10 cell) on a standard North American monitor, 525 lines/60 Hz.

### Step 1

Are the formats reasonable?

a) **Vertical** — It will be difficult to display 512 lines vertically in a 525 line/60 Hz system. By increasing the horizontal sync frequency (less than 5%), some "extra" lines can be added but probably not enough for 512 visible. Considering that the desired alphanumeric format is 25 rows of characters, ten lines high, a total of 250 lines are required for alphanumerics. The entire system must be run interlaced in order to accommodate the graphics, but if the ALPHA is programmed for interlaced video and sync, the characters will occupy only the top half of the screen (250/525). It is more practical therefore to run the ALPHA board in interlaced sync only mode. In this mode, the number of lines doubles to 500 which is very close to the graphics requirement. A standard monitor should be capable of accommodating 500 displayed lines.

b) **Horizontal** — The graphics requirement is for 512 pixels displayed. The alphanumeric requirement is for 80 x 7 = 560 pixels. With a 10 MHz clock, 560 pixels translate into a displayed time of 56 usec. This is greater than the standard requirements (53.5 usec) and quite impractical, thus we must reduce the standard timing in order to display more horizontal pixels. If the cell width is dropped to 6 x 10 and the number of columns is expanded to 85, the horizontal requirement becomes 85 x 6 = 510 pixels. This is slightly less than the 512 required by the graphics video, but very close.

c) **The Modified Format**

GRAPHICS — 504V x 512H

ALPHA — 25 x 85, 6 x 10 pixel cell

**Step 2**

Calculate the horizontal total (in cells) for both boards, the vertical total (in cells) for both boards and the vertical adjust requirements. Modify them if required.

**Horizontal:**

Displayed Pixels = 64 x 8 = 512⟶51.2 usec.

Blanked time required is 10.0 usec.

Therefore the number of blanked pixels = 10 MHz x 10 usec. = 100

100 is not divisible by 8, so choose the next highest value (even):

$$14 \times 8 = 112$$

Therefore total pixels = 512 + 112 = 624

Is 624 evenly divisible by 8 for the graph board? Yes $\rightarrow \frac{624}{8} = 78$

If it were not evenly divisible, one would choose the next highest value which is divisible.

$$\text{Horizontal Video Time} = \frac{624}{10\ \text{MHz}} = 62.4\ \text{usec.}$$

$$\text{Horizontal Frequency} = \frac{1}{62.4\ \text{usec}} = 16.026\ \text{KHz}$$

Verify that 16.026 is within the ± 5% tolerance of the video standard.

Video Standard = 15.75 KHz
Standard + 5% = 16.538 KHz
Standard — 5% = 14.963 KHz

**Vertical:**

$$\text{Number of raster lines at 60 Hz} = \frac{16.026\ \text{KHz} \times 2}{60} = 534$$

Required vertical blanking/field is 1250 usec.⟶20 lines

Therefore the number of displayed lines = 534 — (2 x 20) = 494

If the monitor to be used is very critical about the vertical sync frequency, it would be necessary to modify either the horizontal or vertical display requirements, as not all the desired 500 lines can be displayed simultaneously.

Number of raster lines = 500 + (2 x 20) = 540

$$\text{Vertical Sync Frequency} = \frac{2}{540 \times 62.4\ \text{usec}} = 59.4\ \text{Hz}$$

$$\text{Vertical Total (GRAPH)} = \frac{540}{8} = 67 + 4\ \text{(remainder)}$$

$$\text{Therefore the vertical adjust (GRAPH)} = \frac{4}{2} = 2$$

$$\text{Vertical Total (ALPHA)} = \frac{540}{10} = 54 + 0\ \text{remainder (27 for interlaced sync only)}$$

$$\text{Therefore vertical adjust (ALPHA)} = \frac{0}{2} = 0$$

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**Step 3:**

Calculate the Control and CRTC register parameters for the RGB-ALPHA (Interlaced Sync Only):

CTRL 1 1 1 1 1 1 0 1 1 = [FB]

CTRL 2 0 0 0 0 1 0 1 1 = [0B]

CRTC 0 Horizontal Total = 104

HTOT — 1 = 103

= [67]

CRTC 1 Horizontal Display = 85

= [55]

CRTC 2 Horizontal Sync Position = $\frac{(62.4 \text{ usec.} - 9.5 \text{ usec.}) \times 10 \text{ MHz}}{6} = 88.166$

= 88

= [58]

CRTC 3 Sync Width (V/H)

Vertical Sync Width = $\frac{150}{62.4} = 2.4$ 3 lines

Horizontal Sync Width = $\frac{4.8 \times 10}{6} = 8$ cells

V/H Sync Width = [38]

CRTC 4 Vertical Total = $\frac{540}{10 \times 2} = 27$

VTOT — 1 = 26

= [1A]

CRTC 5 Vertical Adjust = 0

= [00]

CRTC 6 Vertical displayed = $\frac{50}{2} = 25$

= [19]

CRTC 7 Vertical Sync Position = $\frac{16{,}667 - 972}{16{,}667} \times 27 = 25.425$

= 25

= [19]

CRTC 8 Control Mode = Interlace Sync Only = [01]

CRTC 9 Cell Height = 10 lines — 1 = [09]

**Step 4;**

Calculate the Control and CRTC register parameters for the RGB-GRAPH (Interlaced Sync and Video):

CTRL 1 0 0 1 0 0 0 0 0 = [20]

CTRL 1 0 0 1 0 0 0 0 0 = [20]

CTRL 2 0 0 1 1 1 1 1 1 = [3F]

CTRL 3 0 0 0 0 1 1 1 1 = [0F]

CTRL 4 0 0 0 0 0 0 0 0 = [00]

CRTC 0 Horizontal Total = $\frac{624}{8}$ = 78

$H_{TOT}$ −1 = 77

= [4D]

CRTC 1 Horizontal Displayed = $\frac{512}{8}$ = 64

= [40]

CRTC 2 Horizontal Sync Position = $H_{TOT}$ − 4 = CRTC 0 − 3

= [4A]

CRTC 3 Sync Width (V/H)

Vertical Sync Width = $V_{adj}$ − 1 = 2 −1 = 1

Horizontal Sync Width = 1

V/H Sync Width = [11]

CRTC 4 Vertical Total = $\frac{540 - 4}{8}$ = 67

$V_{TOT}$ − 1 = 66

= [42]

CRTC 5 Vertical Adjust = 2

= [02]

CRTC 6 Vertical Displayed = 500

$\frac{500}{8}$ = 62.5

Therefore use 62 (496 lines)

= [3E]

CRTC 7 Vertical Sync Position = 67

= [43]

CRTC 8 Mode Control = Interlaced Sync and Video = [07]

CRTC 9 Cell Height = 8 lines − 1 = [07]

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**PROGRAM SUMMARY**

| RGB-ALPHA | | RGB-GRAPH (S) | |
|---|---|---|---|
| **ADDRESS (as shipped)** | **DATA** | **ADDRESS (as shipped)** | **DATA** |
| 9A | FB | A6 | 20 } Done |
| 9B | 0B | A6 | 20 } Twice |
| 98 | 00 | A7 | 3F |
| 99 | 67 | A8 | FF |
| 98 | 01 | AA | 00 |
| 99 | 55 | AC | 00 |
| 98 | 02 | AE | 4D |
| 99 | 58 | AC | 01 |
| 98 | 03 | AE | 40 |
| 99 | 38 | AC | 02 |
| 98 | 04 | AE | 4A |
| 99 | 1A | AC | 03 |
| 98 | 05 | AE | 11 |
| 99 | 00 | AC | 04 |
| 98 | 06 | AE | 42 |
| 99 | 19 | AC | 05 |
| 98 | 07 | AE | 02 |
| 99 | 19 | AC | 06 |
| 98 | 08 | AE | 3E |
| 99 | 01 | AC | 07 |
| 98 | 09 | AE | 43 |
| 99 | 09 | AC | 08 |
| | | AE | 07 |
| | | AC | 09 |
| | | AE | 07 |

## 8.0 RGB-GRAPH/VAF-512 COMBINATION

For applications requiring graphics with color look-up capability, hardware vector generator, and up to 8 bits per pixel, multiple RGB-GRAPH boards and a VAF-512 can be combined to produce an overlayed image.

The method used to synchronize the two boards is such that several programming restrictions must be observed in setting up the raster format.

### HARDWARE MODIFICATIONS

All RGB-GRAPH boards, level 4 and higher can be mated without any hardware modifications.

Production modification bulletins (PMB's) have, in some cases, been implemented on lower level boards to provide full compatibility. Determine the modification level of your boards and consult the factory.

**on the RGB-GRAPH (Pseudo-Master):**

1. Disconnect jumper 97-98 on the graph to disable the internal clock since the VAF-512 board provides the external clock on Pin 2 of J3 connector.
2. Pin 100-101 must be strapped in order to enable a proper external character clock SYNC signal.
3. Pin 106-107 must be out, because the vertical reset pulse is provided by the real master (ie. VAF-512 board) on Pin 6 of J3 connector.
4. Pin 136-137 must be strapped so that the VAF-512 will receive the HSYNC/ from the RGB-GRAPH, to lock its phased locked-loop.
5. Pin 156-155 must be strapped to enable the XYCLK signal to provide the X, Y DEC, INC controls.
6. Pin 73-72 must be strapped to enable the read access from all registers.
7. For the Pseudo Master RGB-GRAPH, the data lines DAT0 — DAT3 are used so the following connections must be done:

   (Red) MD0 Pin 20 — Pin 16 DAT0
   (Blue) MD1 Pin 29 — Pin 15 DAT1
   (Green) MD2 Pin 18 — Pin 14 DAT2
   (Overlay) MD3 Pin 17 — Pin 13 DAT3

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The nibble selected must be completely within the low byte.

Data port in low byte — 32-33IN, 28-29IN.

8. Bits 0-3 of control registers 3 and 4 (A97 and A81) must be strapped to the same Multibus data lines used by bits 0-3 of the data port.

   For low byte access, connect pin 159-160.

| REGISTER BIT | PIN | AS-SHIPPED STRAPS | PIN | BUS DATA BIT |
|---|---|---|---|---|
| VEN 0 and WEN 0 | 96 | | 80 | DAT 0 |
| | | | 91 | DAT 4 |
| | | | 78 | DAT 8 |
| | | | 94 | DAT 12 |
| VEN 1 and WEN 1 | 86 | | 81 | DAT 1 |
| | | | 79 | DAT 5 |
| | | | 90 | DAT 9 |
| | | | 93 | DAT 13 |
| VEN 2 and WEN 2 | 85 | | 92 | DAT 2 |
| | | | 87 | DAT 6 |
| | | | 83 | DAT 10 |
| | | | 89 | DAT 14 |
| VEN 3 and WEN 3 | 95 | | 82 | DAT 3 |
| | | | 77 | DAT 7 |
| | | | 84 | DAT 11 |
| | | | 88 | DAT 15 |
| *For high byte access 159-158 IN, 159-160 OUT, 159-161 OUT<br>For low byte access strap 159-160 IN, 159-158 OUT, 159-161 OUT<br>For word access strap 159-161 IN, 159-158 OUT, 159-160 OUT | | | | |

9. For the Frame Grab, each of the RGB-GRAPH's bit planes can be strapped to any of the 8 data lines on the video bus (J3). For the Pseudo Master, do the following:

   BIT PLANE 0 Pin 151 to Pin 141
   1 Pin 150 to Pin 143
   2 Pin 149 to Pin 142
   3 Pin 148 to Pin 144

10. The RGB-GRAPH's 4 TTL video signals can be strapped to any one of the 16 lines on the video bus.

| TTL VIDEO | PIN | AS-SHIPPED STRAPS | PIN | J3 PIN |
|---|---|---|---|---|
| 0 | 123 | | 112 | 12 |
| | | | 117 | 16 |
| | | | 122 | 20 |
| | | | 127 | 24 |
| 1 | 118 | | 111 | 13 |
| | | | 116 | 17 |
| | | | 121 | 21 |
| | | | 126 | 25 |
| 2 | 113 | | 110 | 14 |
| | | | 115 | 18 |
| | | | 120 | 22 |
| | | | 125 | 26 |
| 3 | 108 | | 109 | 15 |
| | | | 114 | 19 |
| | | | 119 | 23 |
| | | | 124 | 27 |

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11. Bit Plane Control Straps

    The 4th output channel can be disconnected from the green and grey scale drivers and can be connected to overlay the other 3 video channels. The straps are as follows:

    OVERLAY 103-104IN, 102-105IN
    NO OVERLAY 102-103IN, 104-105IN

    Pin 162-163 must be left open if no RGB-ALPHA board is in the set-up.

**on the RGB-GRAPH (Slave):**

1. Disconnect jumper 97-98 on the graph to disable the internal clock, since the VAF-512 board provides the external clock on Pin 2 of J3 connector.

2. Pin 100-101 must be out, because the proper external character clock SYNC/ signal is provided by the RGB-GRAPH Pseudo Master on Pin 4 of J3 connector.

3. Pin 106-107 must be out, because the vertical reset pulse is provided by the real master (i.e. VAF-512 board) on Pin 6 of J3 connector.

4. Pin 136-137 must be out, because the Pseudo Master graph provides the HSYNC/.

5. Pin 156-157 must be strapped.

6. Pin 71-72 must be strapped to disable the read access from all registers except the data register.

7. For the RGB-GRAPH Slave, we use the data lines DAT4-DAT7, so the following connections must be done.

    (Red) MD0 Pin 20 to Pin 12
    (Blue) MD1 Pin 19 to Pin 11
    (Green) MD2 Pin 18 to Pin 10
    (Overlay) MD3 Pin 17 to Pin 9

    The nibble selected must be completely within the low byte.

    Data port in low byte 32-33IN, 28-29IN

8. Bits 0-3 of control registers 3 and 4 (A81 and A97) must be strapped to the same Multibus data lines used by bits 0-3 of the data port.

    For low byte access, pin 159-160 is connected.

| REGISTER BIT | PIN | AS-SHIPPED STRAPS | PIN | BUS DATA BIT |
|---|---|---|---|---|
| VEN 0 and WEN 0 | 96 | | 80 | DAT 0 |
| | | | 91 | DAT 4 |
| | | | 78 | DAT 8 |
| | | | 94 | DAT 12 |
| VEN 1 and WEN 1 | 86 | | 81 | DAT 1 |
| | | | 79 | DAT 5 |
| | | | 90 | DAT 9 |
| | | | 93 | DAT 13 |
| VEN 2 and WEN 2 | 85 | | 92 | DAT 2 |
| | | | 87 | DAT 6 |
| | | | 83 | DAT 10 |
| | | | 89 | DAT 14 |
| VEN 3 and WEN 3 | 95 | | 82 | DAT 3 |
| | | | 77 | DAT 7 |
| | | | 84 | DAT 11 |
| | | | 88 | DAT 15 |
| *For high byte access 159-158 IN, 159-160 OUT, 159-161 OUT<br>For low byte access strap 159-160 IN, 159-158 OUT, 159-161 OUT<br>For word access strap 159-161 IN, 159-158 OUT, 159-160 OUT | | | | |

9. For the Frame Grab, each of the RGB-GRAPH's bit planes can be strapped to any of the 8 data lines on the video bus (J3). For the RGB-GRAPH Slave the following pins are strapped:

   BIT PLANE 0 Pin 151 to 145
   1 Pin 150 to 146
   2 Pin 149 to 140
   3 Pin 148 to 147

10. The RGB-GRAPH's 4 TTL video signals can be strapped to any one of the 16 lines on the video bus.

| TTL VIDEO | PIN | AS-SHIPPED STRAPS | PIN | J3 PIN |
|---|---|---|---|---|
| 0 | 123 | | 112 | 12 |
| | | | 117 | 16 |
| | | | 122 | 20 |
| | | | 127 | 24 |
| 1 | 118 | | 111 | 13 |
| | | | 116 | 17 |
| | | | 121 | 21 |
| | | | 126 | 25 |
| 2 | 113 | | 110 | 14 |
| | | | 115 | 18 |
| | | | 120 | 22 |
| | | | 125 | 26 |
| 3 | 108 | | 109 | 15 |
| | | | 114 | 19 |
| | | | 119 | 23 |
| | | | 124 | 27 |

11. Pin 162-163 must be out.

12. Couple the boards using a 50 pin ribbon cable to all J3 connectors. The J3 headers are 3M connectors, part no. 3433-1202. The mating connector part number is 3425-7000.

## PROGRAMMING CONSIDERATIONS

### Restrictions

1. In non-interlaced mode, the vertical adjust on the Graph board must be even (i.e. = 0, 2, 4 or 6).

### Differences (RGB-GRAPH) Programming

The RGB-GRAPH is programmed to generate a reset pulse for the CRT controllers once every frame. This pulse is positioned three cells from the end of the last line of video. The width and position of the reset pulse is determined by the horizontal and vertical sync information programmed into the GRAPH board.

Horizontal sync Position $\longrightarrow$ ($H_{TOT}$ − 4)
Width $\longrightarrow$ 1 cell

Vertical sync Position $\longrightarrow$ $V_{TOT}$ (for $V_{adj} > 2$)
$V_{TOT}$ − 1 (for $V_{adj} < 2$)

Width $\longrightarrow$ $V_{adj}$ − 1 (for $V_{adj} > 2$)
($V_{adj}$ + 8) − 1 (for $V_{adj} < 2$) non-interlaced
($V_{adj}$ + 4) − 1 (for $V_{adj} < 2$) interlaced

## PROGRAM EXAMPLE:

The required display format is 512 x 512 graphics on a standard N. American monitor, 525 lines/60 Hz.

**NOTE:** The VAF-512 can only work with a cell of 8 pixels horizontally.

**Step 1**

Are the formats reasonable?

a) Vertical: It will be difficult to display 512 lines vertically in a 525 line/60 Hz system. By increasing the horizontal sync frequency (less than 5%), some "extra" lines can be added but not enough for 512 visible.

A standard monitor should be capable of accommodating 500 displayed lines.

b) Horizontal: The graphics requirement is for 512 pixels displayed.

c) Modified Format:

Graphics — 504 V x 512 H

**Step 2**

Calculate the horizontal total (in cells) for both boards, the vertical total (in cells) for both boards and the vertical adjust requirements. Modify them if required.

**Horizontal:**

Displayed Pixels = 64 x 8 = 512⟶51.2 usec.

Blanked time required is 10.0 usec.

Therefore the number of blanked pixels = 10 MHz x 10 usec. = 100

100 is not divisible by 8, so choose the next highest value (even):

$$14 \times 8 = 112$$

Therefore total pixels = 512 + 112 = 624

Is 624 evenly divisible by 8 for the graph board? Yes $\rightarrow \frac{624}{8} = 78$

If it were not evenly divisible, one would choose the next highest value which is divisible.

$$\text{Horizontal Video Time} = \frac{624}{10\ \text{MHz}} = 62.4\ \text{usec.}$$

$$\text{Horizontal Frequency} = \frac{1}{62.4\ \text{usec}} = 16.026\ \text{KHz}$$

Verify that 16.026 is within the ± 5% tolerance of the video standard.

Video Standard = 15.75 KHz
Standard + 5% = 16.538 KHz
Standard — 5% = 14.963 KHz

**Vertical:**

$$\text{Number of raster lines at 60 Hz} = \frac{16.026\ \text{KHz}}{60} \times 2 = 534$$

Required vertical blanking/field is 1250 usec.⟶20 lines

Therefore the number of displayed lines = 534 — (2 x 20) = 494

If the monitor to be used is very critical about the vertical sync frequency, it would be necessary to modify either the horizontal or vertical display requirements, as not all the desired 500 lines can be displayed simultaneously.

Number of raster lines = 500 + (2 x 20) = 540

$$\text{Vertical Sync Frequency} = \frac{2}{540 \times 62.4\ \text{usec}} = 59.4\ \text{Hz}$$

$$\text{Vertical Total} = \frac{540}{8} = 67 + 4\ \text{(remainder)}$$

$$\text{Therefore the vertical adjust} = \frac{4}{2} = 2$$

A

**Step 3;**

Calculate the Control and CRTC register parameters for the RGB-GRAPH (Interlaced Sync and Video):

CTRL 1 0 0 1 0 0 0 0 0 = [20]

CTRL 1 0 0 1 0 0 0 0 0 = [20]

CTRL 2 0 0 1 1 1 1 1 1 = [3F]

CTRL 3 0 0 0 0 1 1 1 1 = [FF]

CTRL 4 0 0 0 0 0 0 0 0 = [00]

CRTC 0 Horizontal Total = $\frac{624}{8}$ = 78

HTOT — 1 = 77

= [4D]

CRTC 1 Horizontal Displayed = $\frac{512}{8}$ = 64

= [40]

CRTC 2 Horizontal Sync Position = HTOT — 4 = CRTC 0 — 3

= [4A]

CRTC 3 Sync Width (V/H)

Vertical Sync Width = $V_{adj}$ — 1 = 2 —1 = 1

Horizontal Sync Width = 1

V/H Sync Width = [11]

CRTC 4 Vertical Total = $\frac{540 - 4}{8}$ = 67

VTOT — 1 = 66

= [42]

CRTC 5 Vertical Adjust = 2

= [02]

CRTC 6 Vertical Displayed = 500

$\frac{500}{8}$ = 62.5

Therefore use 62 (496 lines)

= [3E]

CRTC 7 Vertical Sync Position = 67

= [43]

CRTC 8 Mode Control = Interlaced Sync and Video = [07]

CRTC 9 Cell Height = 8 lines — 1 = [07]

A

**PROGRAM SUMMARY**

**RGB-GRAPH**

| ADDRESS (as shipped) | DATA |
|---|---|
| A6 | 20 |
| A6 | 20 |
| A7 | 3F |
| A8 | FF |
| AA | 00 |
| AC | 00 |
| AE | 4D |
| AC | 01 |
| AE | 40 |
| AC | 02 |
| AE | 4A |
| AC | 03 |
| AE | 11 |
| AC | 04 |
| AE | 42 |
| AC | 05 |
| AE | 02 |
| AC | 06 |
| AE | 3E |
| AC | 07 |
| AE | 43 |
| AC | 08 |
| AE | 07 |
| AC | 09 |
| AE | 07 |

**VAF-512**

| ADDRESS (as shipped) | DATA |
|---|---|
| 63 (Mode Register) | 04 |

## 9.0 RGB-ALPHA/RGB-GRAPH/VAF-512 COMBINATION

For applications requiring extensive graphics and alphanumerics, an RGB-ALPHA, RGB-GRAPH and a VAF-512 can be combined to produce an overlayed image.

The RGB-ALPHA will provide the foreground color information for the characters and the RGB-GRAPH will provide the background color information. The VAF-512 allows the RGB-ALPHA alphanumeric characters to be overlayed on the graphics display, and allows portions of the display to blink back and forth from one color to another. Also **the RGB-ALPHA SLAVE must have a SYNERTEK CRTC instead of the HITACHI part that is the standard part on the RGB-ALPHA.**

The method used to synchronize the two boards is such that several programming restrictions must be observed in setting up the raster format.

**HARDWARE MODIFICATIONS**

All RGB-ALPHA boards, level 3 and higher, and all RGB-GRAPH boards level 4 and higher can be mated without any hardware modifications.

Production Modification Bulletins (PMB's) have, in some cases, been implemented on lower level boards to provide full compatibility. Determine the modification level of your boards and consult the chart below:

| RGB-ALPHA | | | RGB-GRAPH | | |
|---|---|---|---|---|---|
| REVISION LEVEL | PMB LEVEL | INSTRUCTIONS | REVISION LEVEL | PMB LEVEL | INSTRUCTIONS |
| 1 | | CONSULT FACTORY | 1 | | CONSULT FACTORY |
| 1 | A | " " | 1 | A | " " |
| 1 | AB | " " | 1 | AB | " " |
| 1 | ABC | " " | 1 | | " " |
| 2 | | CONSULT FACTORY | 2 | | CONSULT FACTORY |
| 2 | A | " " | 2 | A | " " |
| 2 | AB | " " | 2 | AB | " " |
| 2 | ABC | " " | 2 | ABC | " " |
| 2 | ABCD | " " | | | |
| 2 | ABCDE | OK | | | |
| | | | 3 | | CONSULT FACTORY |
| 3 & UP | | OK | 3 | A | " " |
| | | | 3 | AB | " " |
| | | | 3 | ABC | " " |
| | | | 4 & UP | | OK |

**on the RGB-ALPHA**

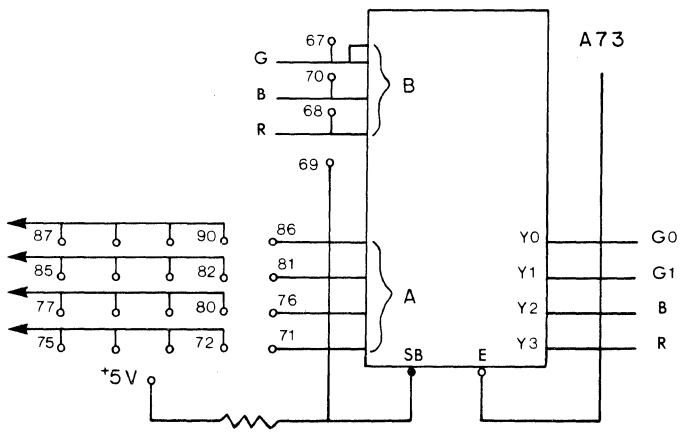
1. Disconnect jumper 113-112 on the RGB-ALPHA to disable the internal clock, connect jumper 111-112 on the RGB-ALPHA to enable the external clock which is provided by the VAF-512 board.

2. An external field SYNC is provided by the VAF-512 board on Pin 6 of J3 connector to reset the RGB-ALPHA CRTC.

3. The external character clock SYNC signal and the CRTC reset/signal, which are provided by the RGB-GRAPH pseudo master are NANDed and put through a frequency divider in the RGB-ALPHA.

4. The alpha board receives a 10 MHz clock signal from the graph board. Higher XTAL frequencies cannot be selected.

5. The graphics input to the RGB-ALPHA must be strapped to select the RGB-GRAPH signal as background color. All straps are on the alpha board.




NOTE: On the RGB-ALPHA, level 3 and higher, these jumpers do not exist. The graphics input (#1) is tied directly to the "A" port on the multiplexor. To select the "A" input on the A73 multiplexor circuit, Pin 69 must be driven low (0 volts). This is accomplished by jumpering Pin 69 to ground, or by jumpering Pin 69 to one of the pins, 67, 70 or 68.

In the latter case, one of the RGB-ALPHA background color attribute bits is used to select or deselect the graphics background for each alphanumeric character cell.

| SOURCE | | WIRE WRAP PINS | EXAMPLE STRAPS | WIRE WRAP PINS | DESTINATION |
|---|---|---|---|---|---|
| RGB-GRAPH #1 | J3 PIN 12 | 87 | | 71 | RED |
| | J3 PIN 13 | 88 | | | |
| | J3 PIN 14 | 89 | | | |
| | J3 PIN 15 | 90 | | | |
| RGB-GRAPH #2 | J3 PIN 16 | 85 | | 76 | BLUE |
| | J3 PIN 17 | 84 | | | |
| | J3 PIN 18 | 83 | | | |
| | J3 PIN 19 | 82 | | | |
| RGB-GRAPH #3 | J3 PIN 20 | 77 | | 81 | GREEN 1 |
| | J3 PIN 21 | 78 | | | |
| | J3 PIN 22 | 79 | | | |
| | J3 PIN 23 | 80 | | | |
| RGB-GRAPH #4 | J3 PIN 24 | 75 | | 86 | GREEN 0 |
| | J3 PIN 25 | 74 | | | |
| | J3 PIN 26 | 73 | | | |
| | J3 PIN 27 | 72 | | | |

**on the RGB-GRAPH (Pseudo-Master):**

1. Disconnect jumper 97-98 on the graph to disable the internal clock since the VAF-512 board provides the external clock on Pin 2 of J3 connector.

2. Pin 100-101 must be strapped in order to enable a proper external character clock SYNC signal.

3. Pin 106-107 must be out, because the vertical reset pulse is provided by the real master (ie. VAF-512 board) on Pin 6 of J3 connector.

4. Pin 136-137 must be strapped so that the VAF-512 will receive the HSYNC/ from the RGB-GRAPH, to lock its phased locked-loop.

5. Pin 156-155 must be strapped to enable the XYCLK signal to provide the X, Y DEC, INC controls.

6. Pin 73-72 must be strapped to enable the read access from all registers.

7. For the Pseudo Master RGB-GRAPH, the data lines DAT0 — DAT3 are used so the following connections must be done:

   (Red) MD0 Pin 20 — Pin 16 DAT0
   (Blue) MD1 Pin 29 — Pin 15 DAT1
   (Green) MD2 Pin 18 — Pin 14 DAT2
   (Overlay) MD3 Pin 17 — Pin 13 DAT3

   The nibble selected must be completely within the low byte.

   Data port in low byte — 32-33IN, 28-29IN.

8. Bits 0-3 of control registers 3 and 4 (A97 and A81) must be strapped to the same Multibus data lines used by bits 0-3 of the data port.

   For low byte access, connect pin 159-160.

   Pin 162-163 must be left open if no RGB-ALPHA board is in the set-up.

| REGISTER BIT | PIN | AS-SHIPPED STRAPS | PIN | BUS DATA BIT |
|---|---|---|---|---|
| VEN 0 and WEN 0 | 96 | | 80 | DAT 0 |
| | | | 91 | DAT 4 |
| | | | 78 | DAT 8 |
| | | | 94 | DAT 12 |
| VEN 1 and WEN 1 | 86 | | 81 | DAT 1 |
| | | | 79 | DAT 5 |
| | | | 90 | DAT 9 |
| | | | 93 | DAT 13 |
| VEN 2 and WEN 2 | 85 | | 92 | DAT 2 |
| | | | 87 | DAT 6 |
| | | | 83 | DAT 10 |
| | | | 89 | DAT 14 |
| VEN 3 and WEN 3 | 95 | | 82 | DAT 3 |
| | | | 77 | DAT 7 |
| | | | 84 | DAT 11 |
| | | | 88 | DAT 15 |
| *For high byte access 159-158 IN, 159-160 OUT, 159-161 OUT<br>For low byte access strap 159-160 IN, 159-158 OUT, 159-161 OUT<br>For word access strap 159-161 IN, 159-158 OUT, 159-160 OUT | | | | |

9. For the Frame Grab, each of the RGB-GRAPH's bit planes can be strapped to any of the 8 data lines on the video bus (J3). For the Pseudo Master, do the following:

   BIT PLANE 0 Pin 151 to Pin 141
   1 Pin 150 to Pin 143
   2 Pin 149 to Pin 142
   3 Pin 148 to Pin 144

10. The RGB-GRAPH's 4 TTL video signals can be strapped to any one of the 16 lines on the video bus.

| TTL VIDEO | PIN | AS-SHIPPED STRAPS | PIN | J3 PIN |
|---|---|---|---|---|
| 0 | 123 | | 112 | 12 |
| | | | 117 | 16 |
| | | | 122 | 20 |
| | | | 127 | 24 |
| 1 | 118 | | 111 | 13 |
| | | | 116 | 17 |
| | | | 121 | 21 |
| | | | 126 | 25 |
| 2 | 113 | | 110 | 14 |
| | | | 115 | 18 |
| | | | 120 | 22 |
| | | | 125 | 26 |
| 3 | 108 | | 109 | 15 |
| | | | 114 | 19 |
| | | | 119 | 23 |
| | | | 124 | 27 |

11. Bit Plane Control Straps

    The 4th output channel can be disconnected from the green and grey scale drivers and can be connected to overlay the other 3 video channels. The straps are as follows:

    OVERLAY 103-104IN, 102-105IN
    NO OVERLAY 102-103IN, 104-105IN

    Pin 162-163 must be connected to provide a CRTC RESET/ for the alpha board.

**on the RGB-GRAPH (Slave):**

1. Disconnect jumper 97-98 on the graph to disable the internal clock, since the VAF-512 board provides the external clock on Pin 2 of J3 connector.

2. Pin 100-101 must be out, because the proper external character clock SYNC/ signal is provided by the RGB-GRAPH Pseudo Master on Pin 4 of J3 connector.

3. Pin 106-107 must be out, because the vertical reset pulse is provided by the real master (i.e. VAF-512 board) on Pin 6 of J3 connector.

4. Pin 136-137 must be out, because the Pseudo Master graph provides the HSYNC/.

5. Pin 156-157 must be strapped.

6. Pin 71-72 must be strapped to disable the read access from all registers except the data register.

7. For the RGB-GRAPH Slave, we use the data lines DAT4-DAT7, so the following connections must be done.

   (Red) MD0 Pin 20 to Pin 12
   (Blue) MD1 Pin 19 to Pin 11
   (Green) MD2 Pin 18 to Pin 10
   (Overlay) MD3 Pin 17 to Pin 9

   The nibble selected must be completely within the low byte.

   Data port in low byte 32-33IN, 28-29IN

8. Bits 0-3 of control registers 3 and 4 (A81 and A97) must be strapped to the same Multibus data lines used by bits 0-3 of the data port.

   For low byte access, pin 159-160 is connected.

| REGISTER BIT | PIN | AS-SHIPPED STRAPS | PIN | BUS DATA BIT |
|---|---|---|---|---|
| VEN 0 and WEN 0 | 96 | | 80 | DAT 0 |
| | | | 91 | DAT 4 |
| | | | 78 | DAT 8 |
| | | | 94 | DAT 12 |
| VEN 1 and WEN 1 | 86 | | 81 | DAT 1 |
| | | | 79 | DAT 5 |
| | | | 90 | DAT 9 |
| | | | 93 | DAT 13 |
| VEN 2 and WEN 2 | 85 | | 92 | DAT 2 |
| | | | 87 | DAT 6 |
| | | | 83 | DAT 10 |
| | | | 89 | DAT 14 |
| VEN 3 and WEN 3 | 95 | | 82 | DAT 3 |
| | | | 77 | DAT 7 |
| | | | 84 | DAT 11 |
| | | | 88 | DAT 15 |
| *For high byte access 159-158 IN, 159-160 OUT, 159-161 OUT<br>For low byte access strap 159-160 IN, 159-158 OUT, 159-161 OUT<br>For word access strap 159-161 IN, 159-158 OUT, 159-160 OUT | | | | |

9. For the Frame Grab, each of the RGB-GRAPH's bit planes can be strapped to any of the 8 data lines on the video bus (J3). For the RGB-GRAPH Slave the following pins are strapped:

   BIT PLANE 0 Pin 151 to 145
   1 Pin 150 to 146
   2 Pin 149 to 140
   3 Pin 148 to 147

10. The RGB-GRAPH's 4 TTL video signals can be strapped to any one of the 16 lines on the video bus.

| TTL VIDEO | PIN | AS-SHIPPED STRAPS | PIN | J3 PIN |
|---|---|---|---|---|
| 0 | 123 | | 112 | 12 |
| | | | 117 | 16 |
| | | | 122 | 20 |
| | | | 127 | 24 |
| 1 | 118 | | 111 | 13 |
| | | | 116 | 17 |
| | | | 121 | 21 |
| | | | 126 | 25 |
| 2 | 113 | | 110 | 14 |
| | | | 115 | 18 |
| | | | 120 | 22 |
| | | | 125 | 26 |
| 3 | 108 | | 109 | 15 |
| | | | 114 | 19 |
| | | | 119 | 23 |
| | | | 124 | 27 |

11. Pin 162-163 must be out.

12. Couple the boards using a 50 pin ribbon cable to all J3 connectors. The J3 headers are 3M connectors, part no. 3433-1202. The mating connector part number is 3425-7000.

**PROGRAMMING CONSIDERATIONS**

**Restrictions**

1) Horizontal Total (pixels) must be the same on both the ALPHA and the GRAPH.

2) Vertical Total (lines) must be the same on both the ALPHA and the GRAPH.

3) Horizontal Displayed on ALPHA must be greater than or equal to that on GRAPH.

4) In non-interlaced mode, the vertical adjust on the graph board must be even (i.e. = 0, 2, 4 or 6).

**Differences (RGB-GRAPH) Programming**

The RGB-GRAPH is programmed to generate a reset pulse for the CRT controllers once every frame. This pulse is positioned three cells from the end of the last line of video. The width and position of the reset pulse is determined by the horizontal and vertical sync information programmed into the GRAPH board.

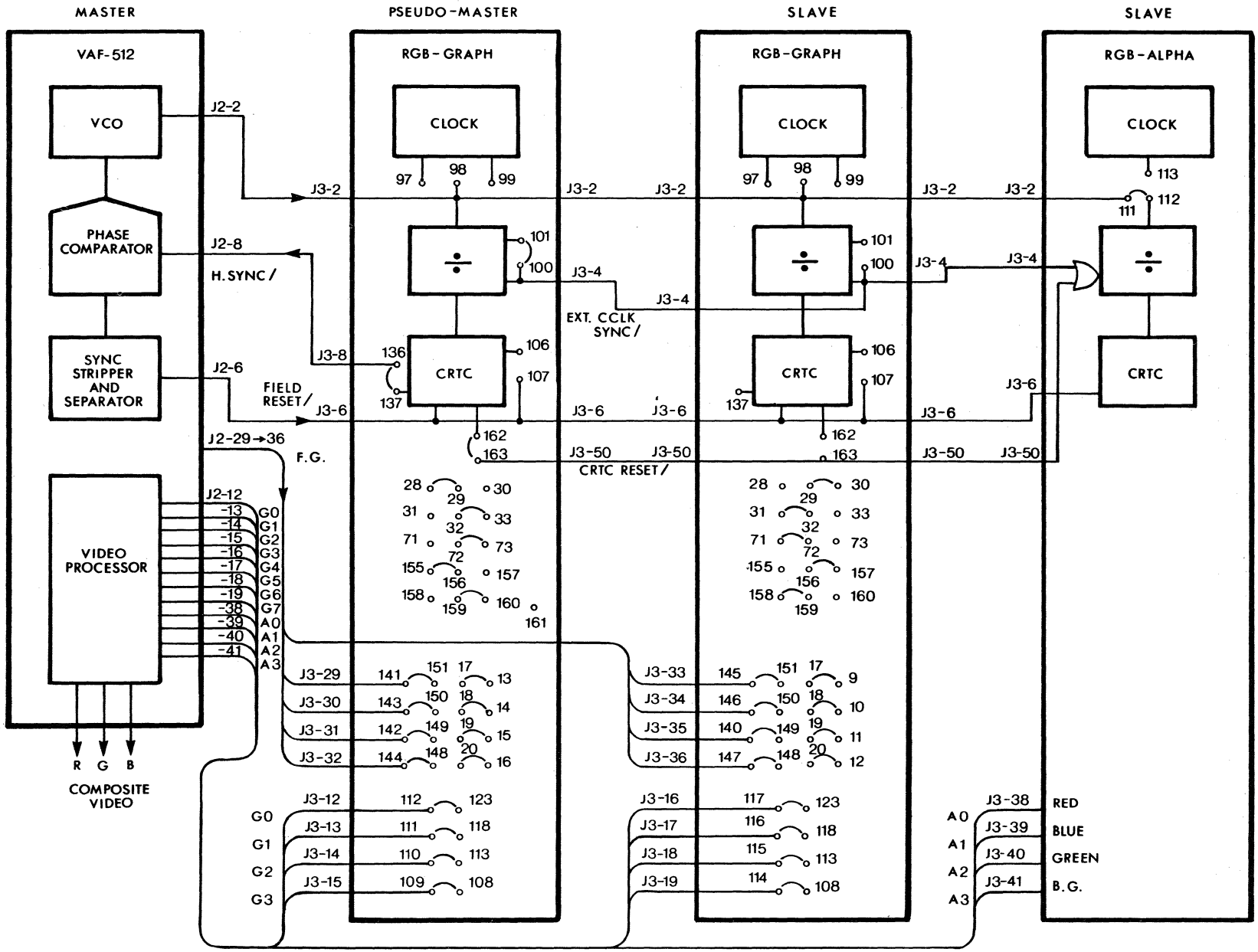
Horizontal sync
Position $\longrightarrow (H_{TOT} - 4)$
Width $\longrightarrow$ 1 cell

Vertical sync
Position $\longrightarrow V_{TOT}$ (for $V_{adj} > 2$)
$V_{TOT} - 1$ (for $V_{adj} < 2$)

Width $\longrightarrow V_{adj} - 1$ (for $V_{adj} > 2$)
$(V_{adj} + 8) - 1$ (for $V_{adj} < 2$) non-interlaced
$(V_{adj} + 4) - 1$ (for $V_{adj} < 2$) interlaced

A

# VAF-512/RGB-GRAPH/RGB-GRAPH/RGB-ALPHA



**PROGRAM EXAMPLE:**

The required display format is 512 x 512 graphics and 25 rows x 70 columns alphanumerics, using a 8 x 10 cell, on a standard N. American monitor, 525 lines/60 Hz.

NOTE: The VAF-512 can only work with a cell of 8 pixels horizontally.

**Step 1**

Are the formats reasonable?

a) **Vertical** — It will be difficult to display 512 lines vertically in a 525 line/60 Hz system. By increasing the horizontal sync frequency (less than 5%), some "extra" lines can be added but probably not enough for 512 visible. Considering that the desired alphanumeric format is 25 rows of characters, ten lines high, a total of 250 lines are required for alphanumerics. The entire system must be run interlaced in order to accommodate the graphics, but if the ALPHA is programmed for interlaced video and sync, the characters will occupy only the top half of the screen (250/525). It is more practical therefore to run the ALPHA board in interlaced sync only mode. In this mode, the number of lines doubles to 500 which is very close to the graphics requirement. A standard monitor should be capable of accommodating 500 displayed lines.

b) **Horizontal:** The graphics requirement is for 512 pixels displayed. The alphanumeric requirement is for 70 x 8 = 560 pixels, but with a 10 MHz clock, 560 pixels translate into a displayed time of 56 micro-seconds. This is greater than the standard requirements (53.5 micro seconds) and quite impractical, thus we must reduce the standard timing in order to display more horizontal pixels. Sice we cannot change the cell width, we have to reduce the number of columns to 64, the horizontal requirement becomes 8 x 64 = 512 pixels; exactly the same as the graph.

c) Modified Format:

Graphics — 504 V x 512 H
Alpha — 25 x 64, 8 x 10 pixel cell

**Step 2**

Calculate the horizontal total (in cells) for both boards, the vertical total (in cells) for both boards and the vertical adjust requirements. Modify them if required.

**Horizontal:**

Displayed Pixels = 64 x 8 = 512 → 51.2 usec.

Blanked time required is 10.0 usec.

Therefore the number of blanked pixels = 10 MHz x 10 usec. = 100

100 is not divisible by 8, so choose the next highest value (even):

$$14 \times 8 = 112$$

Therefore total pixels = 512 + 112 = 624

Is 624 evenly divisible by 8 for the graph board? Yes $\quad \frac{624}{8} = 78$

If it were not evenly divisible, one would choose the next highest value which is divisible.

$$\text{Horizontal Video Time} = \frac{624}{10\ \text{MHz}} = 62.4\ \text{usec.}$$

$$\text{Horizontal Frequency} = \frac{1}{62.4\ \text{usec}} = 16.026\ \text{KHz}$$

Verify that 16.026 is within the ±5% tolerance of the video standard.

Video Standard = 15.75 KHz
Standard + 5% = 16.538 KHz
Standard — 5% = 14.963 KHz

A

**Vertical:**

Number of raster lines at 60 Hz $= \frac{16.026\ \text{KHz}}{60} \times 2 = 534$

Required vertical blanking/field is 1250 usec.⟶20 lines

Therefore the number of displayed lines $= 534 - (2 \times 20) = 494$

If the monitor to be used is very critical about the vertical sync frequency, it would be necessary to modify either the horizontal or vertical display requirements, as not all the desired 500 lines can be displayed simultaneously.

Number of raster lines $= 500 + (2 \times 20) = 540$

Vertical Sync Frequency $= \frac{2}{540 \times 62.4\ \text{usec}} = 59.4\ \text{Hz}$

Vertical Total $= \frac{540}{8} = 67 + 4\ \text{(remainder)}$

Therefore the vertical adjust $= \frac{4}{2} = 2$

Vertical Total (ALPHA) $= \frac{540}{10} = 54 + 0$ remainder (27 for interlaced sync only)

Therefore vertical adjust (ALPHA) $= \frac{0}{2} = 0$

**Step 3:**

Calculate the Control and CRTC register parameters for the RGB-ALPHA (Interlaced Sync Only):

CTRL 1 1 1 1 1 0 1 1 1 = [F7]

CTRL 2 0 0 0 0 1 0 1 1 = [0B]

CRTC 0 Horizontal Total $= \frac{624}{8} = 78$

$H_{TOT} - 1 = 77_{10}$

$= [4E]$

CRTC 1 Horizontal Display $= 64_{10}$
$= [40]$

CRTC 2 Horizontal Sync Position $= \frac{(62.4\ \text{usec.} - 9.5\ \text{usec.}) \times 10\ \text{MHz}}{8} = 66.125$

$= 66_{10}$

$= [42]$

CRTC 3 Sync Width (V/H)

Vertical Sync Width $= \frac{150}{62.4} = 2.4$ 3 lines

Horizontal Sync Width $= \frac{4.8 \times 10}{8} = 6$ cells

V/H Sync Width = [36]

CRTC 4 Vertical Total = $\frac{540}{10 \times 2}$ = 27

$V_{TOT} - 1$ = 26

= [1A]

CRTC 5 Vertical Adjust = 0

= [00]

CRTC 6 Vertical displayed = $\frac{50}{2}$ = 25

= [19]

CRTC 7 Vertical Sync Position = $\frac{16{,}667 - 972 \times 27}{16{,}667}$ = 25.425

= $25_{10}$

= [19]

CRTC 8 Control Mode = Interlace Sync Only = [01]

CRTC 9 Cell Height = 10 lines — 1 = [09]

**Step 4:**

Calculate the Control and CRTC register parameters for the RGB-GRAPH (Interlaced Sync and Video):

CTRL 1 0 0 1 0 0 0 0 0 = [20]

CTRL 1 0 0 1 0 0 0 0 0 = [20]

CTRL 2 0 0 1 1 1 1 1 1 = [3F]

CTRL 3 1 1 1 1 1 1 1 1 = [FF]

CTRL 4 0 0 0 0 0 0 0 0 = [00]

CRTC 0 Horizontal Total = $\frac{624}{8}$ = 78

$H_{TOT} - 1$ = 77

= [4D]

CRTC 1 Horizontal Displayed = $\frac{512}{8}$ = 64

= [40]

CRTC 2 Horizontal Sync Position = $H_{TOT} - 4$ = CRTC 0 — 3

= [4A]

CRTC 3 Sync Width (V/H)

Vertical Sync Width = $V_{adj} - 1$ = 2 —1 = 1

Horizontal Sync Width = 1

V/H Sync Width = [11]

A

CRTC 4 Vertical Total = $\frac{540 - 4}{8}$ = 67

$V_{TOT} - 1$ = 66

= [42]

CRTC 5 Vertical Adjust = 2

= [02]

CRTC 6 Vertical Displayed = 500

$\frac{500}{8}$ = 62.5

Therefore use 62 (496 lines)

= [3E]

CRTC 7 Vertical Sync Position = 67

= [43]

CRTC 8 Mode Control = Interlaced Sync and Viedo = [07]

CRTC 9 Cell Height = 8 lines − 1 = [07]

**PROGRAM SUMMARY**

| RGB-ALPHA | | RGB-GRAPH (S) | |
|---|---|---|---|
| **ADDRESS (as shipped)** | **DATA** | **ADDRESS (as shipped)** | **DATA** |
| 9A | F7 | A6 | 20 } Done |
| 9B | 0B | A6 | 20 } Twice |
| 98 | 00 | A7 | 3F |
| 99 | 4E | A8 | FF |
| 98 | 01 | AA | 00 |
| 99 | 40 | AC | 00 |
| 98 | 02 | AE | 4D |
| 99 | 42 | AC | 01 |
| 98 | 03 | AE | 40 |
| 99 | 36 | AC | 02 |
| 98 | 04 | AE | 4A |
| 99 | 1A | AC | 03 |
| 98 | 05 | AE | 11 |
| 99 | 00 | AC | 04 |
| 98 | 06 | AE | 42 |
| 99 | 19 | AC | 05 |
| 98 | 07 | AE | 02 |
| 99 | 19 | AC | 06 |
| 98 | 08 | AE | 3E |
| 99 | 01 | AC | 07 |
| 98 | 09 | AE | 43 |
| 99 | 09 | AC | 08 |
| | | AE | 07 |
| | | AC | 09 |
| | | AE | 07 |

Note: Both RGB-GRAPH boards will be programmed simultaneously, as the registers for both boards have the same addresses.

**VAF-512**

| ADDRESS (as shipped) | DATA |
|---|---|
| 63 (is using an RGB-ALPHA) | 14 (Mode Register) |
| 63 (if no RGB-ALPHA is used) | 04 |

**Floppy Disk Controller (register disable)**

| ADDRESS (as shipped) | DATA |
|---|---|
| B6 | 80 |

This is to disable 7000 — 7FFF of the memory bank, because it is used by the RGB-ALPHA.

A

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# APPLICATION NOTE #2

# ENHANCED CHARACTER GRAPHICS ON THE RGB-ALPHA

## INTRODUCTION:

Character graphics are generated by the same cards that generate the alphanumeric characters, therefore the graphics resolution is equal to the alphanumerics capability of those cards. An alphanumeric card configured for a display format of 24 lines by 80 characters with an 8 x 10 character cell can display only 24 Vertical x 80 Horizontal Graphic Characters in an 8 x 10 cell.

This Application Note discusses the doubling of the horizontal resolution of the graphic characters. Therefore, the same card discussed above becomes capable of displaying 24 Vertical x 160 Horizontal Graphic Characters.

## ARCHITECTURE

Most of the programmable alphanumeric display cards manufactured by MATROX are capable of character graphics. The character generator on those cards can be replaced by a TI 2516 EPROM, thus allowing users to design, burn and install their own custom character generators. By designing their own character generators, users can adapt the display card more towards their own needs of character graphics or even special alphanumerics.

Some of the MATROX boards accept two 2516 EPROM's, one for the standard display set and the second for the alternate set. The selection between one or the other can be done through the use of one of the attribute bits of the display. Such cards allow the user to install a standard character generator in one socket, and a special graphics set in the second socket. One of those cards is the RGB-ALPHA.

By installing Bytewide Ram memory chips in place of one or both of the character generators on the RGB-ALPHA, the character generators can be down-loaded onto the card from the system microcomputer. This allows users to change the character font of both the graphic and the alphanumeric characters to meet the need for the different display requirements. In process control, as an example, different fonts can be used for normal condition displays as compared to displays of emergency situations.

## OVERVIEW

The RGB-ALPHA has programmable formats, i.e.: the display formats can be changed by software commands (certain formats also require that the crystal be changed for an acceptable display on the screen). As with the display formats, the character cell can also be controlled through software.

To double the horizontal resolution, two alternatives are available. The first is to use a format of double the characters that are needed for alphanumerics. The second is to use half of the number of dots per cell, while doubling the number of cells per alphanumeric character. Investigating the first alternative, we find the following: It was already mentioned above that in character graphics the number of alphanumeric characters is the same as the number of graphic characters. Therefore, this is not a usable alternative since it requires modifying the original specification of the alphanumeric display. Furthermore, by using the example mentioned, we find that 160 (number of characters) x 8 (horizontal pixels per cell) = 1280 pixels to be displayed per horizontal line. To accomodate 1280 pixels horizontally, not only a high resolution and wide bandwidth monitor is required, but also a very fast alphanumeric video controller.

The second alternative functions as follows: If the number of pixels per cell is divided by 2 for the graphics display, then we effectively have 160 graphic characters horizontally, each in a 4 x 10 cell (see figure 1). If at the same time, an alphanumeric character generator is devised that requires two adjacent cells to form a full alphanumeric character, then the alphanumerics will remain 80 characters in an 8 x 10 cell (see figure 2).

Each character generator normally used on the MATROX alphanumeric cards holds 128 characters in an 8 x 10 cell. In the case discussed above, since two cells are used per alphanumeric character, then all 64 upper and lower case characters fit in one character generator.

## HARDWARE MODIFICATIONS

In order to accomplish the above, the standard RGB-ALPHA has to be modified as follows:—

1. The crystal frequency is to be increased to 13.3333 MHz from 11.6666 MHz to allow displaying the full required screen.

A

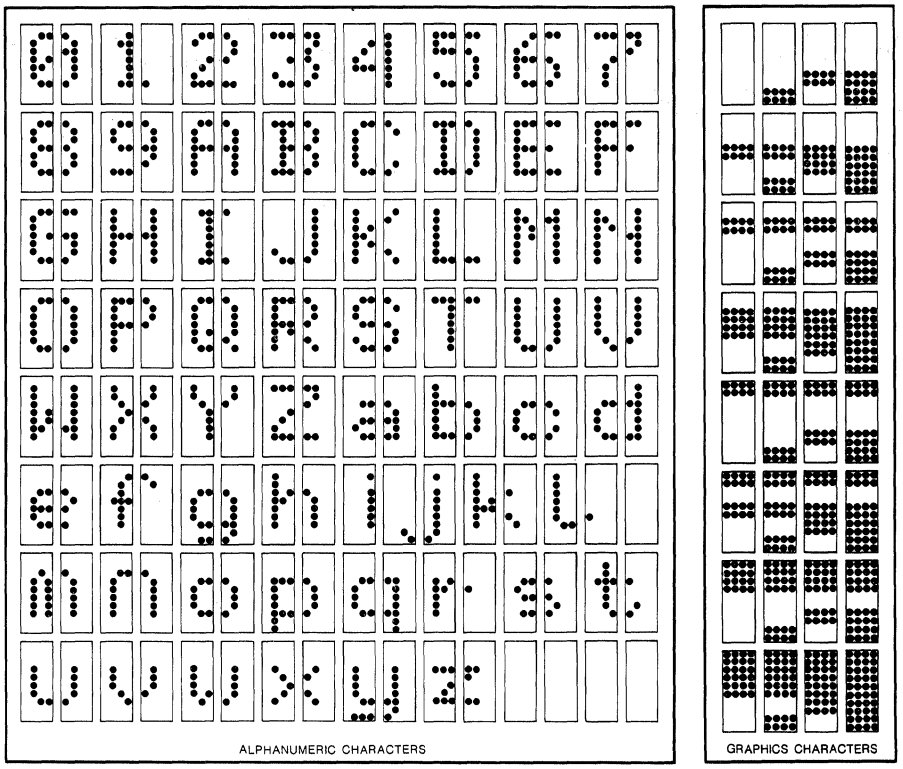



Figure 1. 4 x 10 dot character set

2. The RAM chips are changed to 100 nsec. access time (Intel P2114AL-1) instead of the standard 150 nsec. access time.

3. The character generators are changed to bipolar ROM's with average access time of 70 nsec. (Raytheon R29681DC or Harris HM-76161) instead of 2516's with access time of 350nsec.

4. Exchange pins 19 and 21 of the character generator, i.e.: the trace arriving at pin 19 of the character generator is disconnected and connected instead to pin 21 of the same chip, at the same time the trace going to pin 21 of the character generator is disconnected and connected to pin 19 instead.

5. Disconnect A81 pin 2 from A68 pin 13 and reconnect A81 pin 2 to A68 pin 14.

6. Disconnect wire-wrap pin 98 from 105 and strap pin 98 to pin 59. This will allow the use of D3 of the attributes byte to select one of the two character generators. The attribute register bit assignment (attribute byte) becomes as follows:

| | | |
|---|---|---|
| bit 0 | Foreground Green | 1 = on, 0 = off |
| bit 1 | Foreground Blue | 1 = on, 0 = off |
| bit 2 | Foreground Red | 1 = on, 0 = off |
| bit 3 | Character Generator Select | 1 = character set<br>0 = graph set |
| bit 4 | Background Green | 1 = on, 0 = off |
| bit 5 | Background Blue | 1 = on, 0 = off |
| bit 6 | Background Red | 1 = on, 0 = off |
| bit 7 | Background Blink | 1 = on, 0 = off |

**CONCLUSION:**

By modifying the RGB-ALPHA to run a 4 x 10 character cell, and installing two specially designed character generators, the charcter graphics capability of this card can be enhanced. Using a smaller character cell for the graphics allows the user to display finer graphics lines without sacrificing any of the requirements of the system.

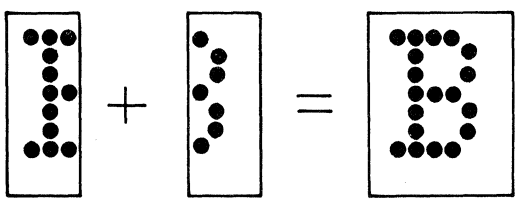


Figure 2. Combining two consecutive 4 x 10 dot cells to form an 8 x 10 dot character

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# APPLICATION NOTE #3

# USING RAM CHARACTER GENERATORS ON THE RGB-ALPHA

## INTRODUCTION

The RGB-ALPHA is a color alphanumeric video board that has software programmable formats. It also has two sockets that can accomodate a 2516 EPROM each, with each EPROM holding the code for 128 characters in an 8 x 16 cell, for a total of 256 characters.

The EPROM chips can be replaced by byte-wide RAM chips, which can be programmed through the bus. Thus the user can download his characters or modify them at any time.

This application note supplies the information needed to design a character generator, and the way these RAM character generators can be downloaded from the bus under program control.

## CHARACTER GENERATOR ARCHITECTURE

The character generator is loaded into a 2716 which is an EPROM of 2K x 8 bits. The characters are formed in a cell of 8 x 16 pixels with each half (i.e. 8 x 8 pixels) loaded into 1K of the EPROM. Every bit is equivalent to one pixel on the screen. A bit that is reset to zero is an OFF pixel, while a bit set to one is an ON pixel, as shown in figure 1.

Each byte on the EPROM holds the 8 bits for each row of a character, and 8 consecutive bytes hold 8 rows of a character. The byte at address 0 holds the 8 pixels of row 0 of character 0, while address 1 holds the 8 pixels for row 1 of character 0, and so on. Address 8 holds the 8 pixels of row 0 of character 1, ....., and address 1023 holds the 8 pixels of row 7 of the 127th character. Address 1024 holds the 8 pixels of row 8 of character 0, address 1025 holds the 8 pixels of row 9 of character 0, and so on. Address 1031 holds the 8 pixels of row 7 of character 1, ....., and address 2047 hold the 8 pixels of row 15 of character 127.

In cases where the cell that is used is an 8 x 8 cell per character, rather than the standard 8 x 16 cell, each character generator can be made to hold 256 characters by using each half of the character generator for a different character and by configuring the straps for the character generator as shown in table 5.12 in section 5 or the RGB-ALPHA manual.

If the character cell is less than 8 pixels horizontally, then the character generator should be programmed for such a cell. If not, the character will be cut off on its left side by the difference between the programmed cell and what the

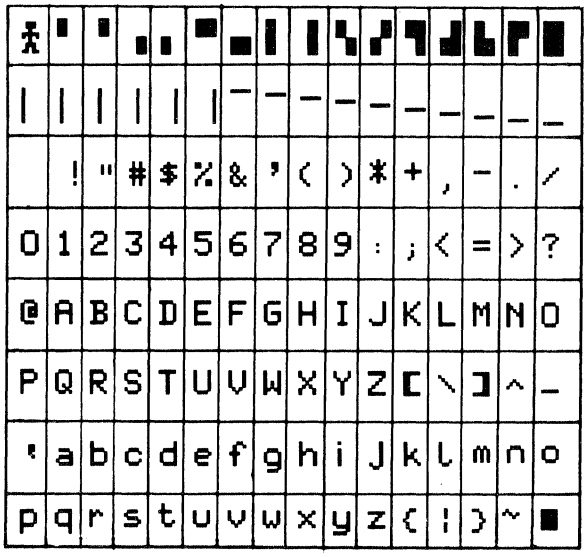

Figure 1. MCH-01 character generator for the RGB-ALPHA

RGB-ALPHA is programmed to display. Also, the character should always have at least one pixel less both vertically and horizontally than the actual display cell to allow for one blank pixel between characters (i.e. a cell of 8 x 10 should have a maximum character size of 7 x 9).

**OVERVIEW**

As mentioned earlier, each RGB-ALPHA board has two sockets for two character generators that are usually loaded with 2716 EPROM chips or their equivalent byte-wide RAM chips (4016 or MK4802P-1). The RGB-ALPHA has provisions to access these two RAM character generators, as RAM, off the bus through I/O control.

Normally the RGB-ALPHA acts like 4K bytes of RAM on the Multibus (in the Auto-Attribute mode) or 8K bytes of RAM in the Unified Memory mode. Memory access is completely controlled by bit 3 of Control Register 2 which, in turn, is controlled by I/O commands. Thus the memory space can be shared between any boards having a different I/O address.

When the RAM character generators are connected to the bus, they act like 4K bytes of RAM with address 0 of character generator 0 equal to the memory base address of the board. Address 1 is equal to the base address plus 1, and so on. Address 0 of character generator 1 is equal to the memory base address plus 2048.

**CONCLUSION:**

Using an RGB-ALPHA, the user can design different character generators and can load them in his system memory. These character generators can then be called as needed and loaded, under software control, into the RAM character generators on the board to allow changes of fonts or alphagraphic characters as for process control applications.

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5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# APPLICATION NOTE #4

## GENERATING MULTIPLE MONOCHROME GRAPHIC DISPLAYS WITH ONE RGB-GRAPH

### INTRODUCTION

The RGB-GRAPH is a dot addressable video graphics board that has software programmable formats. It is available in two memory sizes, and for two buses, the Multibus and the LSI-11 bus (Q-bus). For the Multibus, the RGB-G/16/4 has a maximum format of 256 x 256 x 4, while the RGB-G/64/4 has a maximum format of 512 x 512 x 4. For the Q-bus, only the QRGB-G/64/4 is available with a maximum resolution of 512 x 512 x 4.

This application note discusses the hardware modifications required to generate either two 2 bit outputs, or four 1 bit graphic displays from one RGB-GRAPH/xx/4 board.

### ARCHITECTURE

The memory of the RGB-GRAPH boards mentioned above is divided into 4 independent bit planes. Each bit plane stores one bit for each pixel of the display, for a total of 4 bits per pixel. Four bits per pixel allow for the display of 16 gray levels on a monochrome monitor, or 16 colors on a color monitor. Each RGB-GRAPH board supplies four TTL level outputs of video, one output per plane, and 4 analog outputs, one output per primary color and one for gray scale.

The gray scale output is a 4 bit Digital to Analog (D/A) converter which combines the 4 bit planes into one composite gray scale signal for monochrome displays. The color outputs consist of two 1 bit D/A converters that supply the Red and Blue analog outputs, and a 2 bit D/A converter that supplies the Green output.

### OVERVIEW

Each memory plane is independent from the other planes in so far as memory read, write, preset and output circuits. It can be wire-wrapped to any one of the Data bits on the bus. It can, also, be preset to one or zero independent of the other planes, and they are all clocked to the output in parallel, interconnecting only at the D/A converters. The memory planes share the zoom, pan, scroll, memory refresh and output control circuitry.

Therefore, the RGB-GRAPH outputs can be easily reconfigured to two independent 512 x 512 x 2 displays, or four 512 x 512 x 1 displays. All of that by changing the already existing four D/A converters into four 1 bit D/A converters (Fig. 1a), or into two 2 bit D/A converters (Fig. 1b). A four bit D/A is shown in figure 1c.

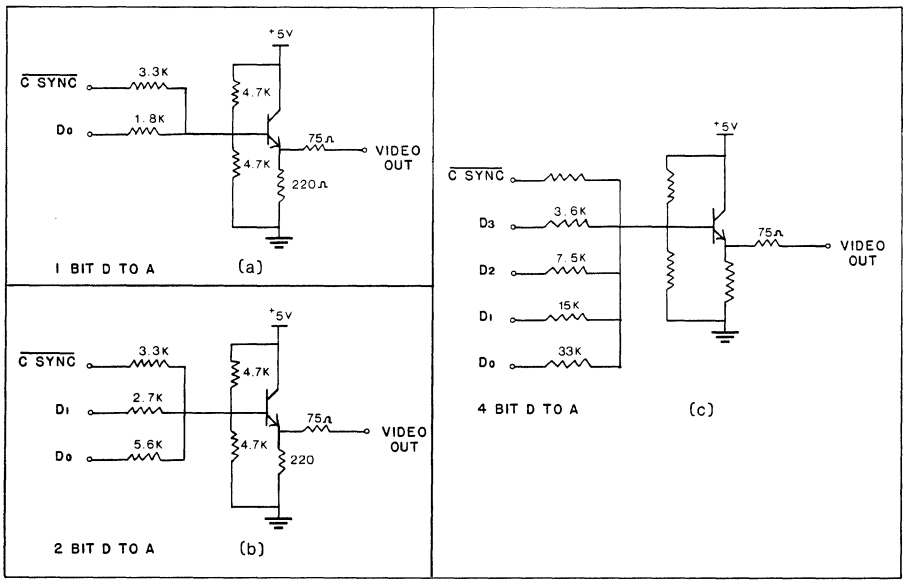


Figure 1. RGB-GRAPH D/A converters: a) 1 bit/pixel, b) 2 bits/pixel, c) 4 bits/pixel

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## HARDWARE MODIFICATIONS

A) Modifying the RGB-GRAPH for two 2 bit outputs (Fig. 2):

1 — Remove Q5, Q6, R37, R38, R39, and R40 from the board.
2 — Insert in the position of R38 a 27 K resistor, and in the position of R39 a 5.6 K resistor.

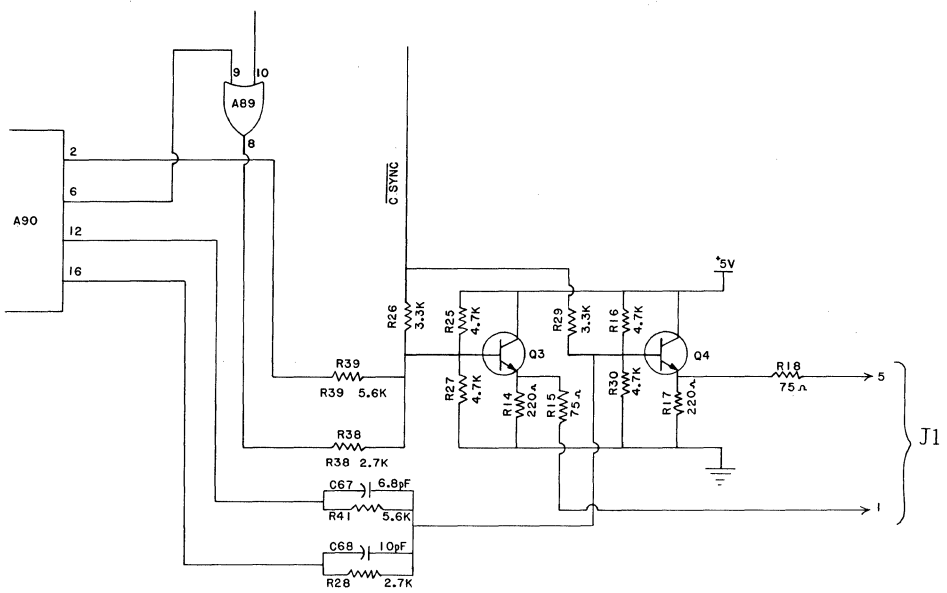


Figure 2. Modifying the RGB-GRAPH for two 2 bit DACs

With the above modifications completed, J1 pin 1 becomes the first 2 bit output, while J1 pin 5 becomes the second 2 bit output. Memory data bits 0 and 1 are the LSB and MSB, respectively, of the first output, while bits 2 and 3 are the LSB and MSB, respectively, of the second output.

B) Modifying the RGB-GRAPH for four 1 bit outputs (Fig. 3):

1 — Remove R28, R37, R38, R39, R40 and R41.
2 — Insert in the positions of R28 and R37 1.8 K resistors.

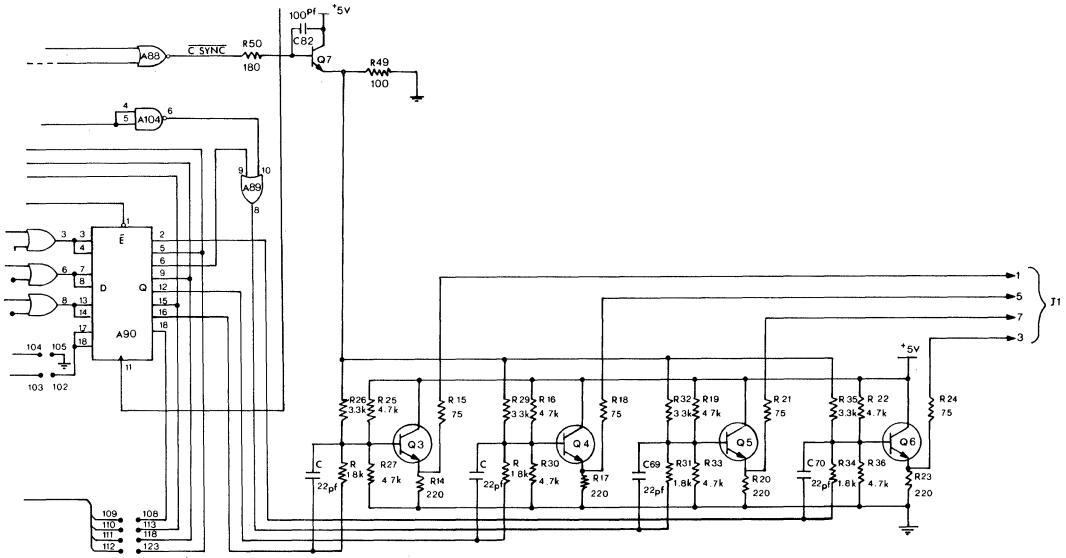


Figure 3. Modifying the RGB-GRAPH for four 1 bit DACs

With the above modifications completed, then each of the pins 1, 3, 5 and 7 of J1 becomes a composite black and white video output.

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## CONCLUSION

By simple modifications on the standard RGB/QRGB-GRAPH/xx/4 board, each board can generate either two 2 bits, or four 1 bit independent displays. Thus one board becomes capable of multiple monochrome graphic displays saving space and hardware for systems designers.

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5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# APPLICATION NOTE #5

## SEGMENTING THE RGB-GRAPH MEMORY FOR FASTER ACCESS

### INTRODUCTION

The RGB-GRAPH is a dot addressable video graphics controller board, that in its color version has four bits per pixel, i.e.: four independent memory planes. When the four bits of color information are written into the memory, only one bit is loaded into each memory plane.

This application note discusses the hardware modifications required to allow the user to write four bits directly on each plane, instead of one bit at a time.

### ARCHITECTURE

The memory of the color RGB-GRAPH is divided into four independent memory planes, and each memory plane normally ties to one data bit on the Data Bus. The interconnection of the memory planes to the Data Bus is done through wire-wrap posts, data buffers, multiplexers, and control logic. The wire-wrap posts allow the user to tie each memory plane to any one of the 16 data bits on the Data Bus. The data buffers isolate the Data Bus from the card, while the multiplexers do the selection between memory refresh data and input or output data. The control logic usually enables only one bit at a time on each memory plane to be written into or read from.

The memory planes on the standard RGB-GRAPH are divided as follows: Plane 0 is RED, Plane 1 is BLUE, Plane 2 is LIGHT GREEN, and Plane 3 is DARK GREEN. Therefore, by writting one bit in each plane simultenously, any color out of the 16 possible is assigned to that pixel.

### OVERVIEW

To allow the user to write four consecutive bits on each plane, at a time, the multiplexer circuitry and the control logic have to be changed, so as to enable four bits of memory on each plane with only one plane enabled at a time.

The control logic consists of two bipolar prom chips A44 and A67, MATROX part number: 033-00. These two prom chips decode X0 and X1 of the X Register into 4 enable signals, one for each memory plane. The data multiplexers are A16, A20, A82 and A86. These multiplexers arbitrate between the data from the Data Register and the Refresh Data that is supplied to the memory chips during the refresh cycle. (see sheet 3 of 5 of the RGB-GRAPH schematic diagrams).

The required modification to the control logic is simply changing the program of the two prom chips, so that 4 enable signals are supplied as before, except this time to only one memory plane at a time. X0 and X1 of the X Register will now decode into which plane the four bits are going to be written into, as follows:

| X0 | X1 | PLANE |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

On the standard RGB-GRAPH, each one of the four data buffers connects to only one bit out of the four input data bits, thus only one bit can be written in each plane at a time. To allow the user to write four consecutive bits in each plane, in one operation, all four input data bits have to be connected to each one of the four data buffers.

A

## HARDWARE MODIFICATIONS

1 — Cut the traces connecting between pins 3, 6, 11, and 14 of A16, A20, A82, and A86.

2 — Cut the traces connecting to pins 6 and 11 of A16. Reconnect the two traces together and connect them, also, to pin 11 of A16.

3 — Cut the trace connecting to pins 11 and 14 of A20, and connect it only to pin 14 of A20.

4 — Cut the trace connecting to pin 6 of A82, also cut the trace connecting to pins 11 and 14 of A82. Reconnect the two traces together and connect them, also, to pin 3 of A82.

5 — Cut the trace connecting to pins 11 and 14 of A86, and connect it to pin 6 instead.

6 — Connect pins 3 of A16, A20, A82, and A86 together.

7 — Connect pins 6 of A16, A20, A82, and A86 together.

8 — Connect pins 11 of A16, A20, A82, and A86 together.

9 — Connect pins 14 of A16, A20, A82, and A86 together.

10 — Remove the two prom chips 033-00 (A44 & 67) from the board and replace them with prom chips part number 0120-00.

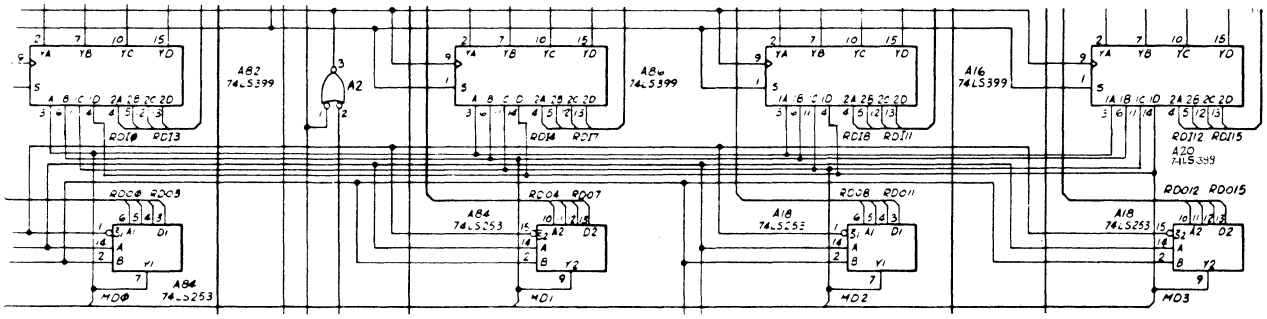

Figure 1. Modified RGB-GRAPH for segmented memory

## CONCLUSION

By modifying the RGB-GRAPH to allow the user to write four bits at a time into each memory plane, the user can do high speed B/W animations by high speed writting into one plane while displaying another. It could also be useful in applications where one RGB-GRAPH is used for four independent graphic displays or special alphanumerics like Japanese or Chinese alphanumeric terminals.

(See Application Note #4 for information on how to reconfigure the output D/A converters for four independent B/W displays).

## NOTE

The hardware changes described in this Application Note will only modify the method of writing into the RGB-GRAPH memory. All other functions like memory read, video enables and plane memory enables remain the same as on a regular RGB-GRAPH. An RGB-GRAPH modified as above will not function with a VAF-512 Frame Grabber board.

A

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# APPLICATION NOTE #6

# BASICS OF RASTER SCAN VIDEO DISPLAYS

## INTRODUCTION

All the video boards manufactured by Matrox, whether they are for alphanumeric or graphic displays, are designed for raster scan type video monitors.

This application note explains the terms, rules & regulations of raster scan displays.

## BASICS of RASTER SCAN DISPLAYS

Raster Scan video systems typically use a Cathode Ray Tube (CRT) as the display device. The inside of the display surface of the CRT is coated with phosphor, which, when bombarded with electrons, emits light. The type of phosphor used determines both the color of the light and the duration of the emission (persistence).

In raster systems, the electron beam(s) is cyclically swept across the face of the CRT, from left to right, top to bottom. Each pixel is lit once for every full sweep of the electron beam, therefore the cycle time and the persistance of the phosphor must be matched so that the image traced by the raster appears stable. If the persistance of the screen is not long enough to keep the pixel illuminated between sweeps of the electron beam, then the pixel will flicker on and off.

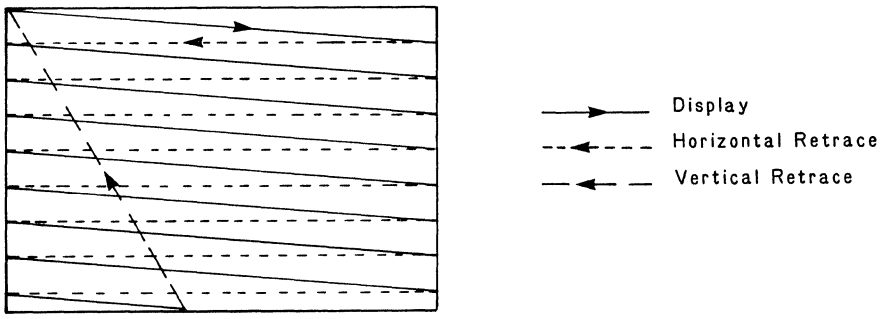


Figure 1. Raster scan principle (non-interlaced video)

At the end of each horizontal line, a sync pulse is generated to reset the electron beam to the left side of the display. This is the horizontal sync pulse. During the horizontal sync pulse the electron beam returns (retraces) to the left of the screen, to start the next line, diagonally across the screen. In order to prevent the retrace from affecting the display, the electron beam is shut off or "blanked" during this interval. This is the horizontal blanking period.

Lines of video are generated in this fashion until the electron beam reaches the bottom of the display. A vertical sync pulse is supplied to reposition the beam to the top of the screen and a vertical blanking period is used to "blank" the video during the vertical retrace period.

That portion of the raster that includes one full sweep of the screen from top to bottom is called a "field" of video. The generation of a full image on the screen is called a "frame".

Two conventions exist for generating complete rasters: a non-interlaced raster is one in which the frame rate is equal to the field rate (i.e. one field per frame); an interlaced raster is one in which the frame rate is half of the field rate (i.e. two fields per frame). In an interlaced raster system, two consecutive fields (odd and even) are vertically offset such that the lines of the odd field fill in between the lines of the even field. In non-interlaced display systems each pixel on the screen is refreshed once every 1/60th of a second. That requires a shorter persistance phosphor, but the monitor bandwidth will be higher since the screen image has to be updated 60 times per second. On the other hand, interlaced display systems refresh each pixel once every 1/30th of a second, since each frame consists of two fields. By dropping the display update rate, the monitor bandwidth is halved, but the screen phosphor must have a longer persistance, since the time between updates is doubled. See figure 2.

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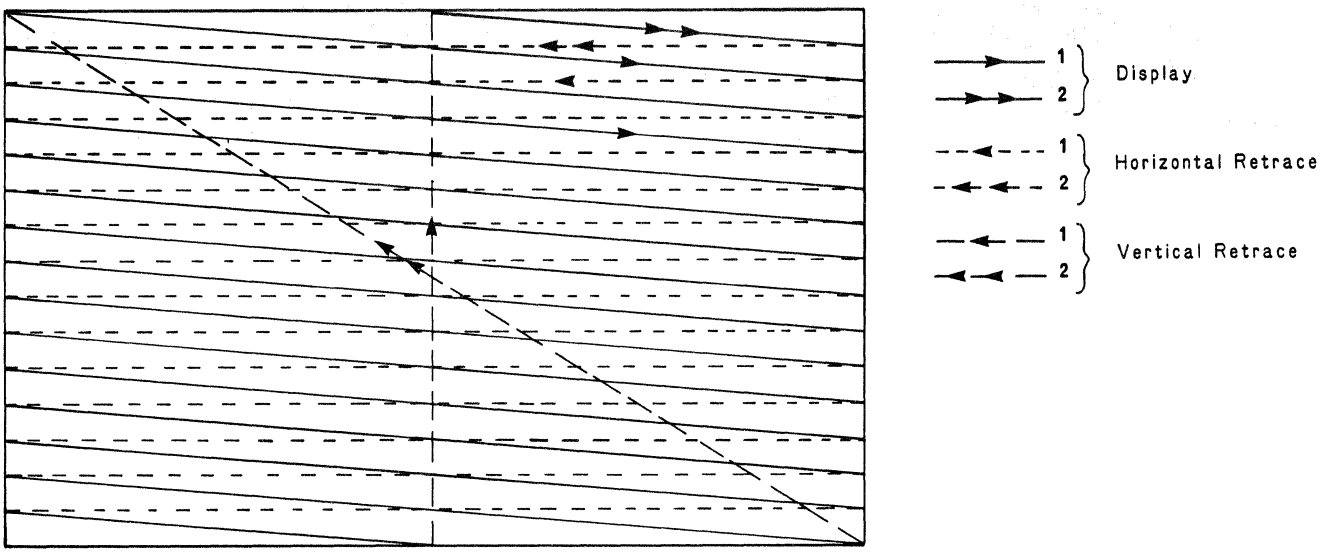



Figure 2. Interlaced video

The image itself is generated by modulating the electron current arriving at the display surface of the CRT, as the beam is sweeping across the screen during the display part. Therefore, a signal has to be supplied to the monitor for every pixel (picture element or dot) to be displayed on the screen. This signal includes the information for the intensity of the pixel at every displayed location on the screen.

**COLOR RASTER SCAN DISPLAY GENERATION**

The generation of color displays is accomplished by mixing the three primary colors: Red, Green, and Blue (hence the term "RGB" was coined by the industry for color displays). Color mixing is accomplished by essentially combining three monitors in one package. RGB monitors have a display surface coated with three types of phosphor, each emitting one of the primary colors, and three electron guns, each bombarding one of the primary color phosphors.

All three electron guns scan the display screen at the same time driven by the same timing generation circuitry. Each gun must be presented with its own modulating signal to decide the intensity of each primary color at that pixel location.

The generation of hues other than the primary colors is accomplished by illuminating more than one primary color phosphor, simultanuously at the same pixel location. The small size of the illuminated area has an additive effect to the color perceived by the human eye, so that an unlimited multitude of colors besides the three primary ones can be generated on certain monitors.

**RASTER SCAN VIDEO SIGNALS**

The video signals, supplied to the monitors for display, must include the video information plus the required synchronization pulses (H and V sync) to keep the scanning circuitry of the monitor locked to the video signal. Video information can be presented to the monitor in logic form (TTL levels) or analog form, depending on the monitor used. Monochrome TTL input monitors can only display two distinct colors: Black and White (the pixel can either be off or on). The number of different colors generated on a TTL color monitor is limited to eight due to the on-off nature of the TTL signal (i.e.: three guns, each with two active states = $2_3$ = 8). Analog monitors on the other hand can generate an almost unlimited number of colors because of the virtually infinite range between "full-off" to "full-on" inherent in analog signals. The number of displayed colors in such a monitor is limited only by the quality of the generated video signal (usually expressed in bits/pixel).

The principal standards, governing both standard television broadcast and local graphic and alphanumeric display generation, were established by the Electronic Industries Association (EIA). Those standards apply to both monochrome and color displays.

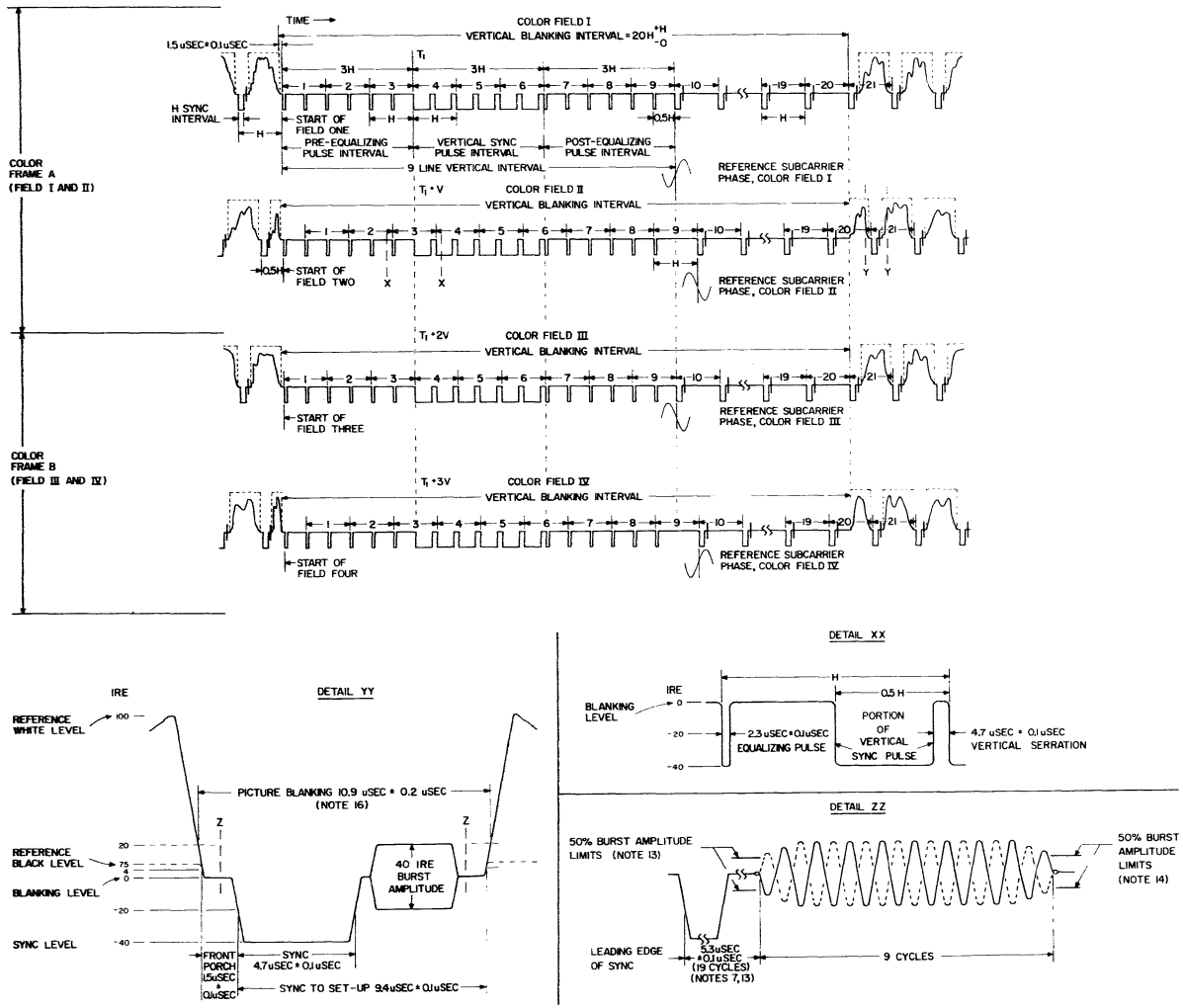
The following is a description of the standards and accepted norms governing video signals.

**1-EIA RS-170A TENTATIVE STANDARD**

This standard calls for a composite video signal in which the display signal and the synchronization pulses are combined together and supplied to the monitor as one signal. The composite video signal shall not exceed 2Vp-p in an open circuit, while the short circuit current shall not exceed 2mA. The load impedance of the source shall have a value of 75 Ohm ± 5%, while the internal impedance of the source shall be 75 Ohm ± 10%.

The RS-170A standard also specifies that the display signal, as measured across a standard load impedance of the source, shall be 1.0 ± 0.05Vp-p, and the synchronizing signal shall be 40 ± 5% of the display signal. Refer to figure 3.

This standard shall be used for display resolutions with a minimum of 350 scan lines in the vertical direction and 400 pixels in the horizontal direction, both measurements to be made near the centre of the display. The display shall have an aspect ratio, which is the ratio of the frame width to the frame height, of 4:3.




NOTES

1. SPECIFICATIONS APPLY TO STUDIO FACILITIES. COMMON CARRIER, STUDIO TO TRANSMITTER AND TRANSMITTER CHARACTERISTICS ARE NOT INCLUDED.
2. ALL TOLERANCES AND LIMITS SHOWN IN THIS DRAWING PERMISSIBLE ONLY FOR LONG TIME VARIATIONS.
3. THE BURST FREQUENCY SHALL BE 3.579545 MHz ± 10 Hz.
4. THE HORIZONTAL SCANNING FREQUENCY SHALL BE 2/455 TIMES THE BURST FREQUENCY [ONE SCAN PERIOD (H) = 63.556 uSEC].
5. THE VERTICAL SCANNING FREQUENCY SHALL BE 2/525 TIMES THE HORIZONTAL SCANNING FREQUENCY [ONE SCAN PERIOD (V) = 16,683 uSEC].
6. START OF COLOR FIELDS I AND III IS DEFINED BY A WHOLE LINE BETWEEN THE FIRST EQUALIZING PULSE AND THE PRECEDING H SYNC PULSE. START OF COLOR FIELDS II AND IV IS DEFINED BY A HALF LINE BETWEEN THE FIRST EQUALIZING PULSE AND THE PRECEDING H SYNC PULSE. COLOR FIELD I: THAT FIELD WITH POSITIVE GOING ZERO-CROSSINGS OF REFERENCE SUBCARRIER MOST NEARLY COINCIDENT WITH THE 50% AMPLITUDE POINT OF THE LEADING EDGES OF EVEN NUMBERED HORIZONTAL SYNC PULSES. REFERENCE SUBCARRIER IS A CONTINUOUS SIGNAL WITH THE SAME INSTANTANEOUS PHASE AS BURST.
7. THE ZERO-CROSSINGS OF REFERENCE SUBCARRIER SHALL BE NOMINALLY COINCIDENT WITH THE 50% POINT OF THE LEADING EDGES OF ALL HORIZONTAL SYNC PULSES. FOR THOSE CASES WHERE THE RELATIONSHIP BETWEEN SYNC AND SUBCARRIER IS CRITICAL FOR PROGRAM INTEGRATION, THE TOLERANCE ON THIS COINCIDENCE IS ± 40° OF REFERENCE SUBCARRIER.
8. ALL RISE TIMES AND FALL TIMES UNLESS OTHERWISE SPECIFIED ARE TO BE 0.14 uSEC ± 0.02 uSEC MEASURED FROM 10% TO 90% AMPLITUDE POINTS. ALL PULSE WIDTHS ARE MEASURED AT 50% AMPLITUDE POINTS, UNLESS OTHERWISE SPECIFIED.
9. TOLERANCE ON SYNC LEVEL, REFERENCE BLACK LEVEL (SET-UP) AND PEAK TO PEAK BURST AMPLITUDE SHALL BE ± 2 IRE UNITS.
10. THE INTERVAL BEGINNING WITH LINE 17 AND EXTENDING THROUGH LINE 20 OF EACH FIELD MAY BE USED FOR TEST, CUE AND CONTROL SIGNALS.
11. EXTRANEOUS SYNCHRONOUS SIGNALS DURING BLANKING INTERVALS, INCLUDING RESIDUAL SUBCARRIER, SHALL NOT EXCEED 1 IRE UNIT. EXTRANEOUS NON-SYNCHRONOUS SIGNALS DURING BLANKING INTERVALS SHALL NOT EXCEED 0.5 IRE UNIT. ALL SPECIAL PURPOSE SIGNALS (VITS, VIR, ETC.) WHEN ADDED TO THE VERTICAL BLANKING INTERVAL ARE EXCEPTED. OVERSHOOT ON ALL PULSES DURING SYNC AND BLANKING, VERTICAL AND HORIZONTAL, SHALL NOT EXCEED 2 IRE UNITS.
12. BURST ENVELOPE RISE TIME IS 0.3 uSEC ± 0.2 uSEC - 0.1 uSEC MEASURED BETWEEN THE 10% AND 90% AMPLITUDE POINTS. BURST IS NOT PRESENT DURING THE NINE LINE VERTICAL INTERVAL.
13. THE START OF BURST IS DEFINED BY THE ZERO-CROSSING (POSITIVE OR NEGATIVE SLOPE) THAT PRECEDES THE FIRST HALF CYCLE OF SUBCARRIER THAT IS 50% OR GREATER OF THE BURST AMPLITUDE. ITS POSITION IS NOMINALLY 19 CYCLES OF SUBCARRIER FROM THE 50% AMPLITUDE POINT OF LEADING EDGE OF SYNC. (SEE DETAIL ZZ)
14. THE END OF BURST IS DEFINED BY THE ZERO-CROSSING (POSITIVE OR NEGATIVE SLOPE) THAT FOLLOWS THE LAST HALF CYCLE OF SUBCARRIER THAT IS 50% OR GREATER OF THE BURST AMPLITUDE.
15. MONOCHROME SIGNALS SHALL BE IN ACCORDANCE WITH THIS DRAWING EXCEPT THAT BURST IS OMITTED, AND FIELDS III AND IV ARE IDENTICAL TO FIELDS I AND II RESPECTIVELY.
16. OCCASIONALLY, MEASUREMENT OF PICTURE BLANKING AT 20 IRE UNITS IS NOT POSSIBLE BECAUSE OF SCENE CONTENT AS VERIFIED ON A PICTURE MONITOR.

COLOR TELEVISION STUDIO
PICTURE LINE AMPLIFIER OUTPUT
RS 170 A
EIA TENTATIVE STANDARD

DRAWN: JWPG

NOVEMBER 8, 1977

Figure 3. RS-170A tentative video standard

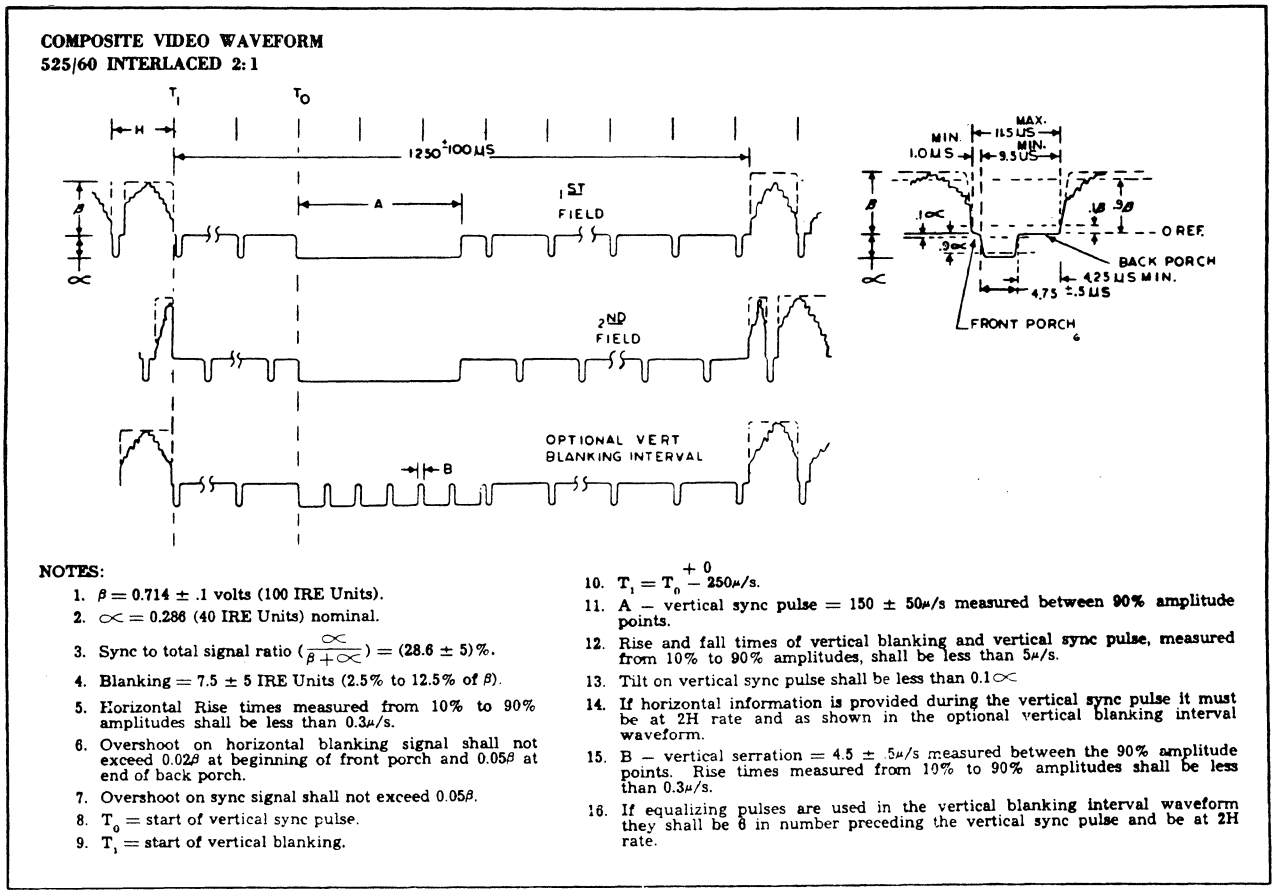



Figure 4. RS-330 video standard

### 2-EIA RS-330 STANDARD

This standard calls for the same requirements as RS-170A except for the following: The display signal shall be 0.714 ± 0.1V, while the synchronization part of the video signal shall be 0.286 ± 0.05V.

This standard shall be used for display resolutions of at least 350 lines vertically and 600 pixels horizontally. Refer to figure 4.

### 3-EIA RS-343 STANDARD

This standard has the same specifications as RS-170A except for the following: The display signal shall be 0.714 ± 0.1V, while the synchronizing signal shall be 0.286 ± 0.05V. This standard shall apply to display resolution in the range of 675 to 1023 pixels horizontally with a field rate of 60 Hz, interlaced 2:1.

The frame aspect ratio shall be 4:3 or 1:1. Refer to figure 5.

### 4-TTL LEVEL

There is no standard governing this kind of an output. Since the video input is a logic level, than the video signal and the synchronization pulses can not be mixed. The norm in the industry is a positive going video signal, while the vertical sync and the horizontal sync outputs can be either positive or negative going pulses.

The synchronization TTL outputs of the Matrox boards can be wire-wrapped for positive or negative going pulses. The outputs themselves are driven by Bipolar 74SLxxx series drivers, therefore normal Fan Out considerations for that series should be taken into account in cases where more that one TTL monitor is attached to the same output.

### NOTE:

In cases where a number of analog monitors are to be driven by the analog output of one Matrox board, the monitors selected should have an impedance selection switch, plus loop-through connectors. The switch allows the user to put the monitor on the line with the standard 75 Ohm impedance or with high impedance, while the loop-through connectors duplicate the input BNC connectors for multiple monitor connections.

Let us consider a case where there is three monitors to be driven by the same signal, see figure 6. The video signal is connected to monitor #1 which is put in the high impedance state. The signal is connected from the secondary connectors of monitor #1 to the input of monitor #2, which is also in the high impedance state. The signal is fed from the secondary connectors of monitor #2 to the input of monitor #3. Since monitor #3 is the last monitor to be driven

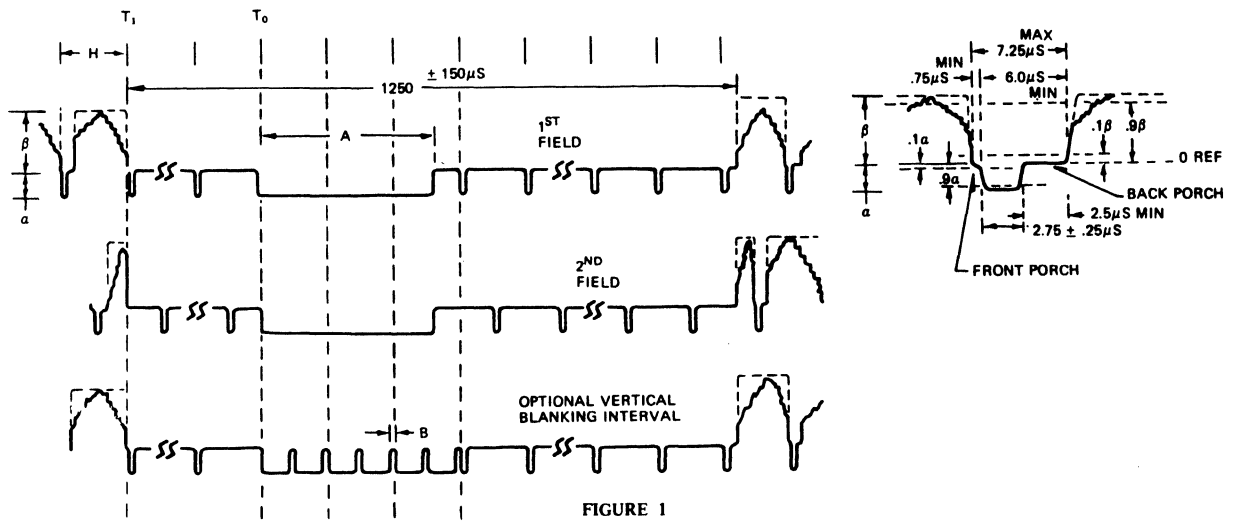



FIGURE 1

COMPOSITE VIDEO WAVEFORM HIGH RESOLUTION MONOCHROME TELEVISION CAMERA

NOTES:

1. $\beta$ = 0.714 ± 0.1 volts (100 IRE Units).
2. $\alpha$ = 0.286 (40 IRE Units) nominal.
3. Sync to total signal ratio $(\frac{\alpha}{\beta + \alpha})$ = 28.6 ± 5%.
4. Blanking = 7.5 ± 5 IRE Units (2.5% to 12.5% of $\beta$).
5. Horizontal Rise Times measured from 10% to 90% amplitudes shall be less than 0.1 μ/s.
6. Overshoot on horizontal blanking signal shall not exceed 0.02$\beta$ at beginning of front porch and 0.05$\beta$ at end of back porch.
7. Overshoot on sync signal shall not exceed 0.05$\beta$.
8. $T_0$ = start of vertical sync pulse.
9. $T_1$ = start of vertical blanking.
10. $T_1 = T_0 + 0 - 250$ μ/s
11. A - vertical sync pulse = 125 ± 50 μ/s measured between 90% amplitude points.
12. Rise and fall times of vertical blanking and vertical sync pulse, measured from 10% to 90% amplitudes, shall be less than 5 μ/s.
13. Tilt on vertical sync pulse shall be less than 0.1α.
14. If horizontal information is provided during the vertical sync pulse it must be at 2H frequency and as shown in the optional vertical blanking interval waveform.
15. B - vertical serration = 2 ± .5 μ/s measured between the 90% amplitude points. Rise time measured from 10% to 90% amplitudes shall be less than 0.1 μ/s.
16. If equalizing pulses are used in the vertical blanking interval waveforms they shall be 6 in number preceding and following the vertifcal sync pulse, be at 2H frequency and 1/2 the width of H sync pulse.
17. It is recommended that for proper interlace the time duration between the leading edge of vertical sync and the leading edge of horizontal sync be a multiple of H/2.

Figure 5. RS-343 video standard

by the same signal, then it should have an impedance of 75 Ohm so that the line is terminated according to the standards. Normally there is no restriction as to the number of monitors that are driven by the same signal, as long as all the monitors between the source and the last monitor are set for high impedance, and only the last one is set for 75 Ohm. Under no circumstance should the monitors be connected in parallel to the source.

## VIDEO MONITORS

The two most important factors in selecting a monitor are the video bandwidth and the screen persistance.

The video bandwidth of the monitor has to be equal to or better than the actual video signal that it is supposed to display. The following is a table that lists the required bandwidth of the monitor to be used with Matrox boards with the different resolutions.

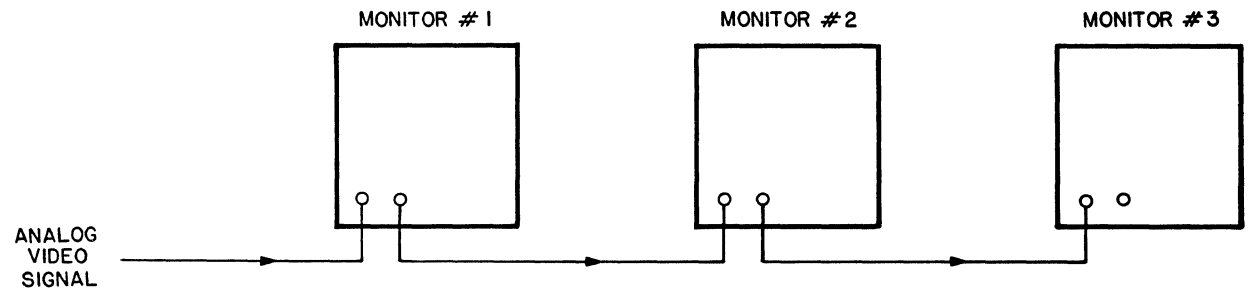



Figure 6. Driving several Monitors with a single video signal

| Display Resolution | Field Rate | Bandwidth [MHz] |
|---|---|---|
| 1600 x 1200 | interlaced 30 Hz | 85-90 |
| 1600 x 1200 | interlaced 25 Hz | 70-75 |
| 1280 x 1024 | interlaced 30 Hz | 65-70 |
| 1216 x 862 | interlaced 35 Hz | 65-70 |
| 1024 x 768 | non-interlaced 60 Hz | 70-75 |
| 1024 x 768 | non-interlaced 50 Hz | 65-70 |
| 1024 x 768 | interlaced 30 Hz | 45-50 |
| 640 x 480 | non-interlaced 60 Hz | 35-40 |
| 512 x 512 | interlaced 30 Hz | 15-20 |
| 256 x 256 | non-interlaced 60 Hz | 10-15 |

The screen persistance is totally dependant on the type of display and its resolution. The problem arises from the fact that each pixel is re-illuminated (refreshed) once every 1/60th of a second, and if the screen phosphor does not remain illuminated (persist) between refresh, then the display will flicker.

A medium or long persistance phosphor is recommended for all graphics applications that use interlaced displays, except for high speed animation. For non-interlaced displays a short or medium persistance phosphor would be satisfactory. As a comparison, phosphor types P39 and P40 which are long persistance phosphors take as long as 150msec. to decay, while the medium persistance phosphors like P1 and P42 decay in 24 and 10msec. respectively. Short persistance phosphors like P4, P7 and P31 decay in microseconds. The above decay times are the length of time it requires the light intensity of the phosphor to drop to 90% from 100%.

**CABLES and CONNECTORS**

All the latest video boards from Matrox use a 10 pin AMP connector for the video outputs. The part number for the housing of the equivalent cable connector is 87922-1 and the part number of the pins is 87667-2. These pins can be either crimped or soldered to the wires.

The majority of color monitors on the market today use 75 Ohm BNC jacks, while there might still be some monitors using 75 Ohm UHF jacks. Since UHF to BNC adaptors are readily available, then it is more convenient to use BNC plugs to connect to the monitors. The part number for the BNC plug is Amphenol 554-82/262. The interconnecting 75 Ohm cable for the BNC plug is RG-179 A/U for distances of up to 15 feet. For distances of up to 500 feet RG-59 A/U is required.

Flat ribbon cable is sufficient for interconnecting the TTL signals to the monitor, if the distance is 15 feet or less. For longer distances shielded cables and line drivers are required.

**NOTE:**

Signal attenuation and gross mismatches of impedances due to bad cables and connections can cause dim displays, double pictures, noisy and torn images, or bad colors.

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# APPLICATION NOTE #7

## USING MATROX Q-BUS CARDS WITH UNIBUS SYSTEMS

Matrox manufactures the QRGB-ALPHA, QRGB-GRAPH, and QVAF-512 video cards, which plug into the DEC Q-bus (LSI-11). These video cards can also be interfaced to Unibus (PDP11) systems via a Unibus to Q-bus converter.

A dual purpose bus converter, the "QNIVERTER" is available from:

Able Computer
1732 Reynolds Avenue
Irvine, CA 92714
Tel: (714) 979-7030
TWX: 910-595-1729 ACT IRIN

The QNIVERTER is a quad width card which performs one of two user selected functions:

— permits an LSI-11, LSI-11/2, LSI-11/23, or PDP-11/03 computer system to access Unibus compatible cards.

— permits a PDP-11 (Unibus) computer system to access Q-bus compatible cards.

The QNIVERTER card installs into a quad slot of a Q-bus backpane and connects to that bus through the A and B connectors on the card. Two Unibus connectors, on the top of the QNIVERTER card, provide connection to a standard Unibus cable, through which the QNIVERTER connects to the Unibus backplane.

The QNIVERTER is software transparent to the host computer, supports a four level interrupt structure, and functions with memory parity and full 256K byte addressing.

The QNIVERTER can not be used to interface a PDP-11 computer system to an LSI-11 computer system or vice-versa, since it can not function as a bus arbitrator between two computers.

To use the Matrox Q-bus video boards with a Unibus computer, the computer owner needs the following items:

1. A standard Unibus cable
2. A quad LSI-11 cardcage with power supply (DEC BA11-N or equivalent)
3. A QNIVERTER bus converter card

The QNIVERTER card plugs into the first slot of the LSI-11 cardcage, the slot the CPU usually occupies. A standard Unibus cable is plugged, on one side, into the two Unibus connectors on top of the QNIVERTER and on the other side, into the last slot of the Unibus backplane of the Unibus computer. The Matrox Q-bus video cards plug into the LSI-11 cardcage, anywhere after the QNIVERTER, and assume lower priority than the Unibus cards.

The above set-up is useful for any Q-bus card, thus Q-bus memories and controllers can be added to the new cardcage.

Further technical information about the QNIVERTER, its installation, and use is available from Able Computer Technology.





MAY 1983

AP-E07-01

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electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

# APPLICATION NOTE #8

# CALCULATING USER-DEFINED VIDEO FORMATS FOR THE GXB-1000

## INTRODUCTION

The GXB-1000 is an advanced high resolution graphics controller which may be configured for different display formats. There are eight different pre-programmed formats available, however, it is possible to program the GXB with other video formats. The purpose of this application note is to explain how to compute the parameters required for custom video formats.

## ARCHITECTURE

The GXB-1000 is a multiboard set designed for the INTEL MULTIBUS. The VGM board, which is the video controller, contains an 8088 microprocessor, a NEC 7220 graphics controller, and the firmware required to perform various functions. Some of these functions are circle drawing, filled polygons, text areas, and input function (i.e. bit pad) support. The RMB board contains 512 KBYtes of video RAM, connected to the VGM via a special high-speed video bus, called a META bus. Up to four RMB boards may be used with a single VGM.

When running in the graphics mode, the GXB fetches op-codes from memory to perform various functions. One of these functions, labelled LOAD VIDEO FORMAT, allows the user to load custom video formats. Sixteen bytes of data are required to completely define a new video format.

## OVERVIEW

For the purposes of the following discussion, frequency will be measured in Hertz and periods measured in seconds.

In order to determine the required parameters, it is first necessary to compute the dot clock period as follows:

$$\text{Dot Clock (DC)} = \frac{1}{\text{crystal frequency}}$$

$$\text{Dot Clock Word (DCW)} = \text{DC} \times 32$$

The DCW value will be required later.

The next step is to compute the horizontal frequency and determine if it resides within your monitor's horizontal bandwith specification. The number chosen for the horizontal displayed pixels must be *evenly* divisible by 32. Satisfying this requirement, the horizontal frequency is computed as follows:

Horizontal PERiod (HPER) = horizontal displayed pixels x DC + HSYNC + HFPORCH + HBPORCH

where: HSYNC is the horizontal sync width time.

HFPORCH is the horizontal front porch width time.

HBPORCH is the horizontal back porch width time.

and

$$\text{Horizontal Frequency} = \frac{1}{\text{HPER}}$$

If the horizontal frequency is too high there are two options. The number of displayed pixels may be decreased, or the crystal frequency may be divided by two. This division is achieved by removing jumper 105-106 on the VGM board, and installing jumpers 104-105, and 106-107. If, however, the horizontal frequency is too low, then the number of displayed pixels may be increased. Additionally, the HSYNC/HFPORCH/HBPORCH values may be "padded" to obtain the required value.

A

The vertical refresh rate must now be determined. Needless to say this value must fall within your monitor's vertical bandwidth specifications. The calculations are as follows:

Vertical PERiod (VPER) = HPER x ((flag x vertical displayed lines) + VSYNC + VFPORCH + VBPORCH)

where: VSYNC is the number of horizontal lines required for the vertical sync pulse.

VFPORCH is the number of horizontal lines required for the vertical front porch.

VBPORCH is the number of horizontal lines required for the vertical back porch.

flag = 0.5 for interlaced video
1.0 for non-interlaced video

In some cases the above three values are given in time. In this case VPER is computed as follows:

$$VPER = (HPER \times flag \times \text{vertical displayed lines}) + vsync(t) + vfporch(t) + vbporch(t)$$

with:

$$VSYNC = \frac{vsync(t)}{HPER}$$

$$VFPORCH = \frac{vfporch(t)}{HPER}$$

$$VBPORCH = \frac{vbporch(t)}{HPER}$$

It should be noted that VSYNC, VFPORCH, and VBPORCH must be integer quantities.

The vertical frequency is determined by the following equation:

$$\text{Vertical Frequency} = \frac{1}{VPER}$$

Once parameters have been determined that satisfy your monitor's bandwidth requirements, it is necessary to create a "display file" so that the GXB can implement the new display format. Note that parameters which contain two bytes are stored with the LSB first and the MSB second.

| DISPLAY FILE LOCATION | DATA |
|---|---|
| byte 1 | Op-code to LOAD VIDEO FORMAT. C1 hex. |
| bytes 2 & 3 | Number of horizontal displayed pixels. |
| bytes 4 & 5 | Number of vertical displayed pixels. |
| bytes 6 & 7 | Horizontal dimension of the GXB's memory. This value must not be less than the number of horizontal displayed pixels and must be a multiple of 64. |
| bytes 8 & 9 | Vertical dimension of the GXB's memory. This value must not be less than the number of vertical displayed pixels. |
| byte 10 | 1B hex selects interlaced video.<br>12 hex selects non-interlaced video. |
| byte 11 | This is where the DCW becomes important. The value here is the number of active display words per line minus 2, computed as follows: (the result must be even).<br>$\frac{\text{horizontal displayed pixels}}{32} - 2$ |

byte 12

The lower 5 bits contain the horizontal sync width, measured in Display Word Periods (DWP), minus one. This value is obtained as follows:

$$\frac{\text{HSYNC} - 1}{\text{DCW}}$$

The upper 3 bits of this byte (least significant), and the lower two bits of byte 13 (most significant), contain the vertical sync width, measured in horizontal scan periods. This is the VSYNC parameter.

byte 13

The lower two bits are as mentioned above. The upper 6 bits measure, in DWP, the horizontal front porch minus one.

$$\frac{\text{HFPORCH} - 1}{\text{DCW}}$$

byte 14

The lower six bits represent the horizontal back porch width (in DWP) minus one.

$$\frac{\text{HBPORCH} - 1}{\text{DCW}}$$

The two upper bits must be zero.

byte 15

The lower six bits specifies the vertical front porch, in horizontal lines. This is the VFPORCH parameter. The upper two bits must be zero.

byte 16

This byte contains the least significant 8 bits of a 10 bit number, while the 2 lower bits of byte 17 contain the most significant bits of this 10 bit number. Its value is computed as follows:

vertical displayed lines x flag.

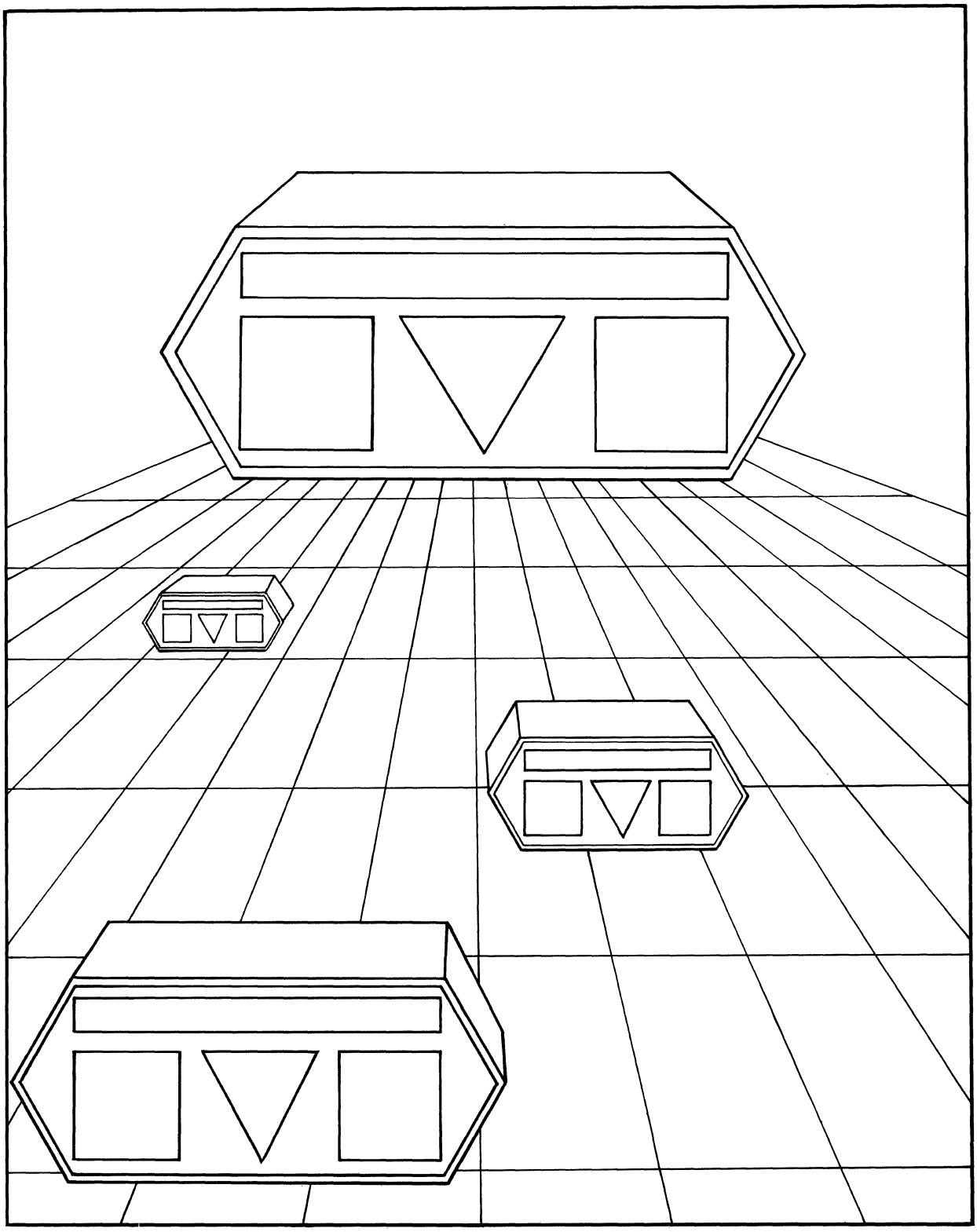
This value will either be the same or one-half the value entered in bytes 3 and 4.

byte 17

The lower two bits are mentioned above. The upper 6 bits contain the vertical back porch width, measured in horizontal lines. This is the VBPORCH value.

**CONCLUSION**

Due to the wide variety of video monitors available, it is not possible to have a pre-programmed video format for every individual monitor. Thus, applications such as CAD/CAM and CAE will benefit by allowing the user to implement non-standard screen formats with a minimal amount of effort.



# ORDERING INFORMATION

## APPENDIX B ORDERING INFORMATION

## ORDERING INFORMATION

Orders can be placed directly with Matrox, or through our local distributors and representatives. Orders will be accepted by telephone, mail, or telex.

Detailed product ordering information is provided on the last page of the product data sheet. It is important that the proper product configuration be defined on the order, to ensure prompt delivery.

## PRICE

Price information, including quantity discounts, is published in the "Matrox OEM Price List". All prices are subject to change, and should be verified at the time an order is placed.

## TERMS

Terms are net 30 to firms approved by Matrox's credit department. New customers are required to provide three trade references and a bank reference in order to secure credit.

## DELIVERY

Delivery on all standard products can vary from stock to eight weeks. Consult the factory for specific delivery times when ordering. All US orders are shipped F.O.B. our warehouse facility at Mooers, NY. All Canadian and Overseas orders are shipped F.O.B. our plant in Montreal.

Orders can be shipped via UPS, UPS Blue Label, Airborne, or Purolator Sky courier. Shipping charges are prepaid and invoiced by Matrox.

## WARRANTY

All products manufactured by Matrox are warranted against defects in material and workmanship for a period of six (6) months from date of shipment from Matrox. Color monitors are warranted against defects for a period of ninety (90) days from the date of shipment from Matrox. Matrox will repair or replace products which prove to be defective during the warranty period provided that they are returned to Matrox Electronic Systems Ltd. at the point of original shipment. No other warranty is expressed or implied. Matrox is not responsible for consequential damages.

Matrox shall not be liable under this warranty for: (i) the goods that the buyer alleges are defective and have been repaired or altered by someone other than Matrox designated personnel or authorized representative, unless such repair or alteration was effected pursuant to prior written approval of Matrox Electronic Systems, or (ii) where the buyer fails to notify Matrox Electronic Systems of any alleged defects within the period of warranty, or (iii) where the buyer fails to return defective items to Matrox Electronic Systems, freight prepaid, or (iv) where equipment has been altered or damaged in such a way which Matrox Electronic Systems reasonably determines to personally effect the performance or reliability, or where the equipment has been subject to misuse, neglect, or accident.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING, BUT NOT LIMITED TO ANY WARRANTY FOR FITNESS OF PURPOSE MERCHANTABILITY, OR FREEDOM FROM INFRINGEMENT OR THE LIKE, AND ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATIONS, OR SAMPLE. MATROX ELECTRONIC SYSTEMS NEITHER ASSUMES OR AUTHORIZES ANY PERSON TO ASSUME FOR IT ANY OTHER LIABILITY.

## RETURNS

No returned goods, for service or otherwise, will be accepted without prior authorization from Matrox Electronic Systems. All returned units must have a Returned Merchandise Authorization (RMA) number issued by Matrox. Units must be returned to the original shipping point and the packaging must indicate the RMA number on the outside.

Goods returned for warranty servicing must be shipped prepaid. They will be returned at no charge for freight. All other returns will be shipped back collect or prepaid.

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MATROX ELECTRONIC SYSTEMS LTD.
5800 Andover Avenue
T.M.R., Quebec H4T 1H4
Canada
Tel: (514) 735-1182
Tlx: 05-825651

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627 Cherokee Street
Marietta, GA 33060
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MATROX ELECTRONIC SYSTEMS LTD.
5800 Andover Avenue
T.M.R., Quebec H4T 1H4
Canada
Tel: (514) 735-1182
Tlx: 05-825651

**IDAHO**

P.A.R. ASSOCIATES
10515 East 40th Avenue
No. 103
Denver, CO 80239
Tel: (303) 371-4140
Twx: 910-932-0180

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Suite 201
Earth City, MO 63045
Tel: (314) 291-0001
Twx: 910-762-0685

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1375 Remington Road
Suite M
Schaumburg, IL 60195
Tel: (312) 885-1131
Twx: 910-291-0370

**INDIANA**

MICRO-TEX INC.
1375 Remington Road
Suite M
Schaumburg, IL 60195
Tel: (312) 885-1131
Twx: 910-291-0370

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TECHNICAL REPRESENTATIVES INC.
2510 White Eagle Trail SE
Cedar Rapids, IA 52403
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360 North Rock Road
Suite 4
Wichita, KS 67206
Tel: (316) 681-0242

**KENTUCKY**

MATROX ELECTRONIC SYSTEMS LTD.
5800 Andover Avenue
T.M.R., Quebec H4T 1H4
Canada
Tel: (514) 735-1182

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KLM GARNER
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Pen-Tech Building, Suite C
3709 Alliance Drive
Greensboro, NC 27407
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**NORTH DAKOTA**

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5300 West 73rd Street
Minneapolis, MN 55435
Tel: (612) 831-5060

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T.M.R., Quebec H4T 1H4
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Tel: (514) 735-1182
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1006 Hampshire Lane
Richardson, TX 75080
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Huntingdon Valley, PA 19006
Tel: (215) 947-5641
Twx: 510-665-5303

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3709 Alliance Drive
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Suite 212
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Twx: 910-443-2319

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BURGIN-KREH ASSOCIATES
7000 Security Boulevard
Suite 330
Baltimore, MD 21207
Tel: (301) 265-8500
Twx: 710-862-1450

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5800 Andover Avenue
T.M.R., Quebec H4T 1H4
Canada
Tel: (514) 735-1182
Tlx: 05-825651

**WISCONSIN**

JEN-RAY SYSTEMS
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Minneapolis, MN 55435
Tel: (612) 831-5060

MICRO-TEX INC.
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Suite 3B
Waukesha, WI 53186
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Tlx: 76159 MATROX

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Switzerland
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Suite 212
Bellevue, WA 98005
Tel: (206) 453-8881
Twx: 910-443-2319

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Mississauga, Ontario
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Suite 540
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6600 Trans-Canada Highway
Suite 540
Pointe Claire, Quebec
H9R 4S2
Tel: (514) 694-5343
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T.M.R., Quebec
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TRACAN ELECTRONICS CORP.
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**ONTARIO**

TRACAN ELECTRONICS CORP.
1200 Aerowood Drive
Suite 46
Mississauga, Ontario
L4W 2S7
Tel: (416) 625-7752
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K1Z 7L7
Tel: (613) 722-7667

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electronic systems ltd.

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T.M.R., (Montreal) Quebec
Canada H4T 1H4
Telex: 05-825651
Tel.: (514) 735-1182