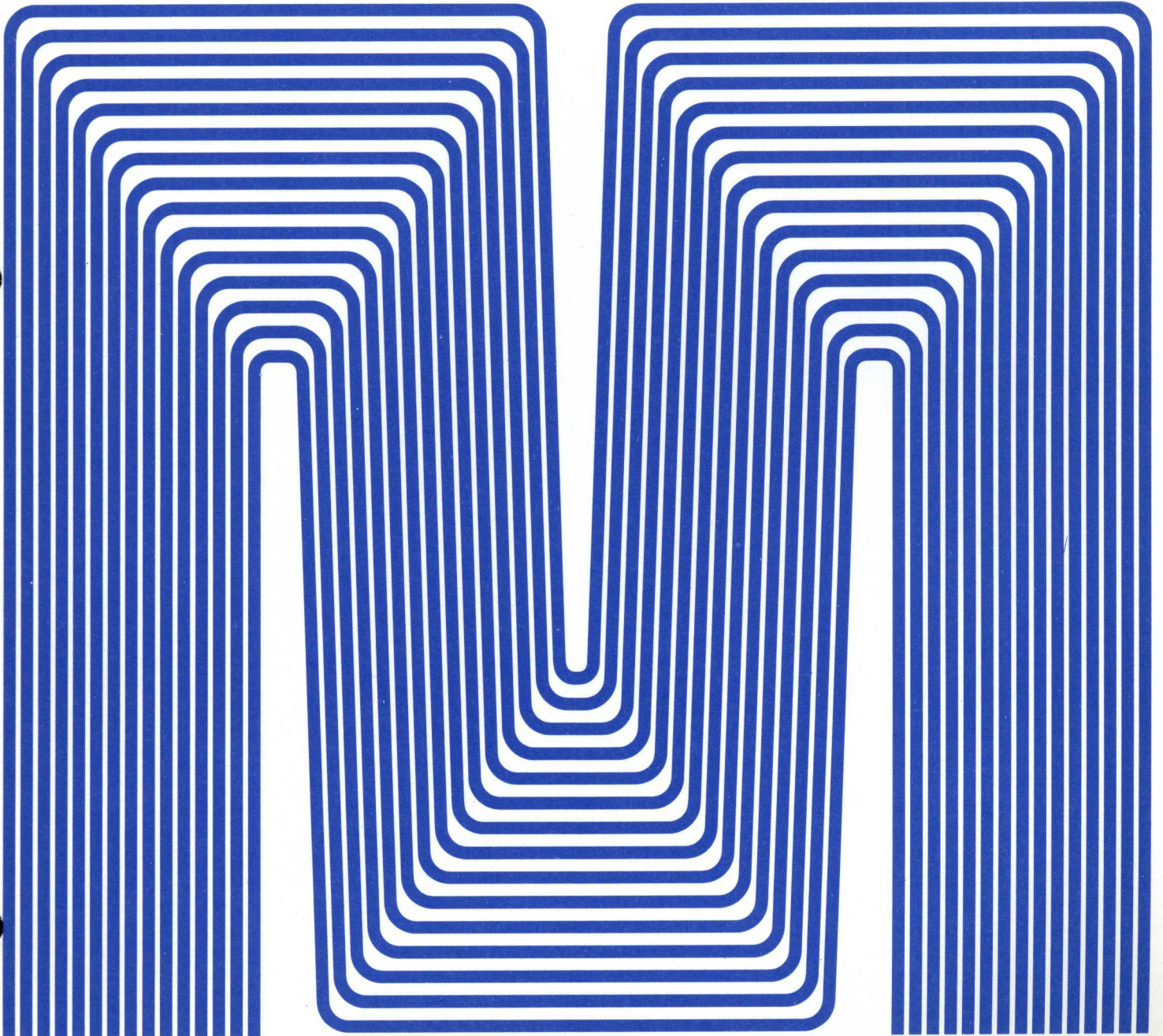


MicroSystems Inc.

APR 21 1970

Micro 810 Computer

M810 Firmware  
Program Manual



# **MICRO 810 COMPUTER M810 FIRMWARE PROGRAM MANUAL**

69-1-0810-005

August, 1969

Micro Systems Inc  
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Santa Ana, California 92705

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## FILE ASSIGNMENTS

0	C	CONDITION CODES
1	I	INSTRUCTION
2	XL	INDEX REGISTER
3	XU	
4	AL	ACCUMULATOR
5	AU	
6	BL	EXTENDED ACCUMULATOR
7	BU	
8	OL	OPERAND ADDRESS
9	OU	
10	PL	PROGRAM COUNTER
11	PU	
12	S1	TEMPORARY, ALWAYS SUBROUTINE RETURN
13	S2	TEMPORARY
14	S3	TEMPORARY
15	OV/W	OVERFLOW AND WORD LENGTH

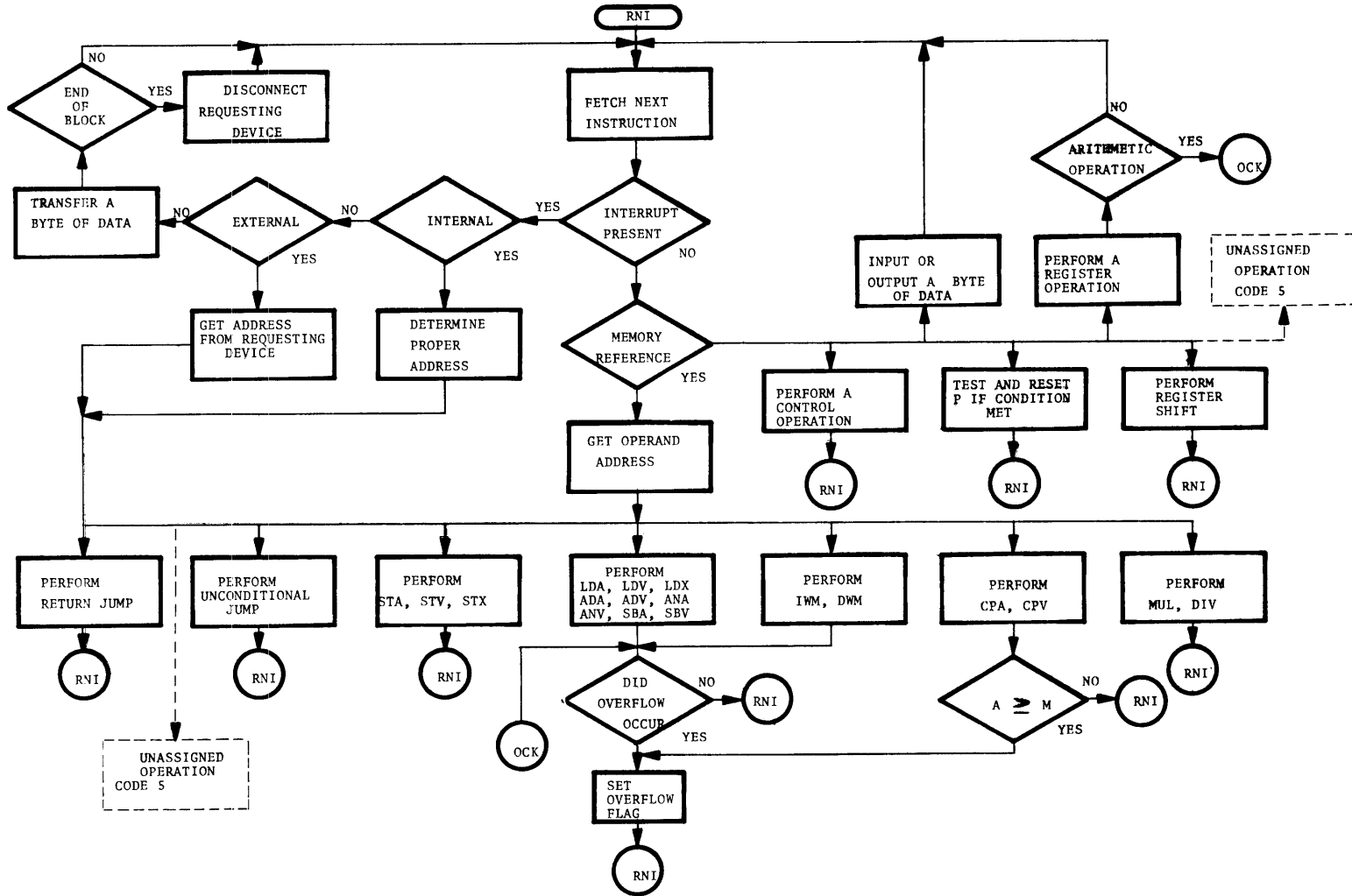


FIGURE 1. 810 SYSTEM FLOWCHARTS

READ NEXT INSTRUCTION

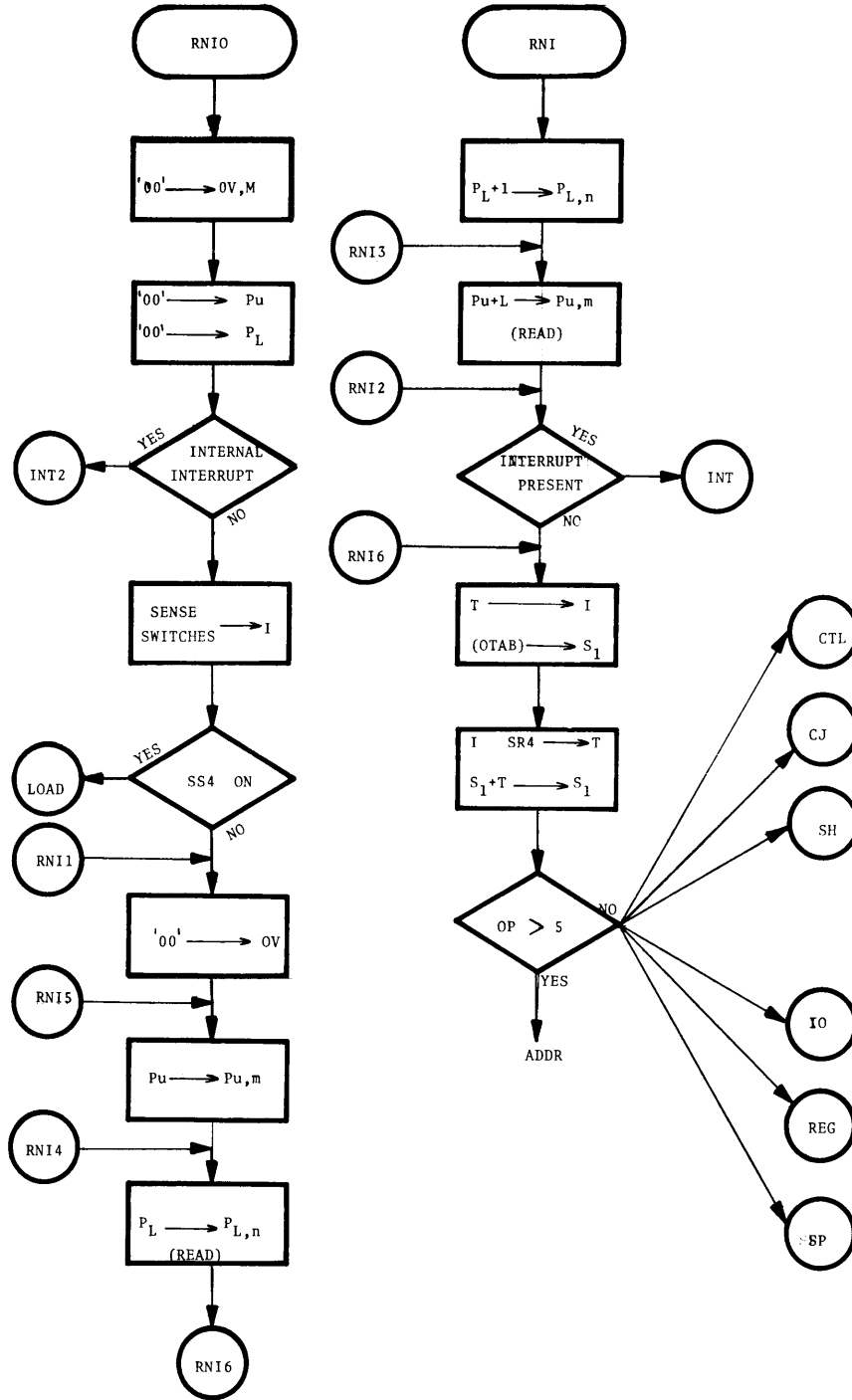


FIGURE 2. READ NEXT INSTRUCTION

OPERAND ADDRESSING

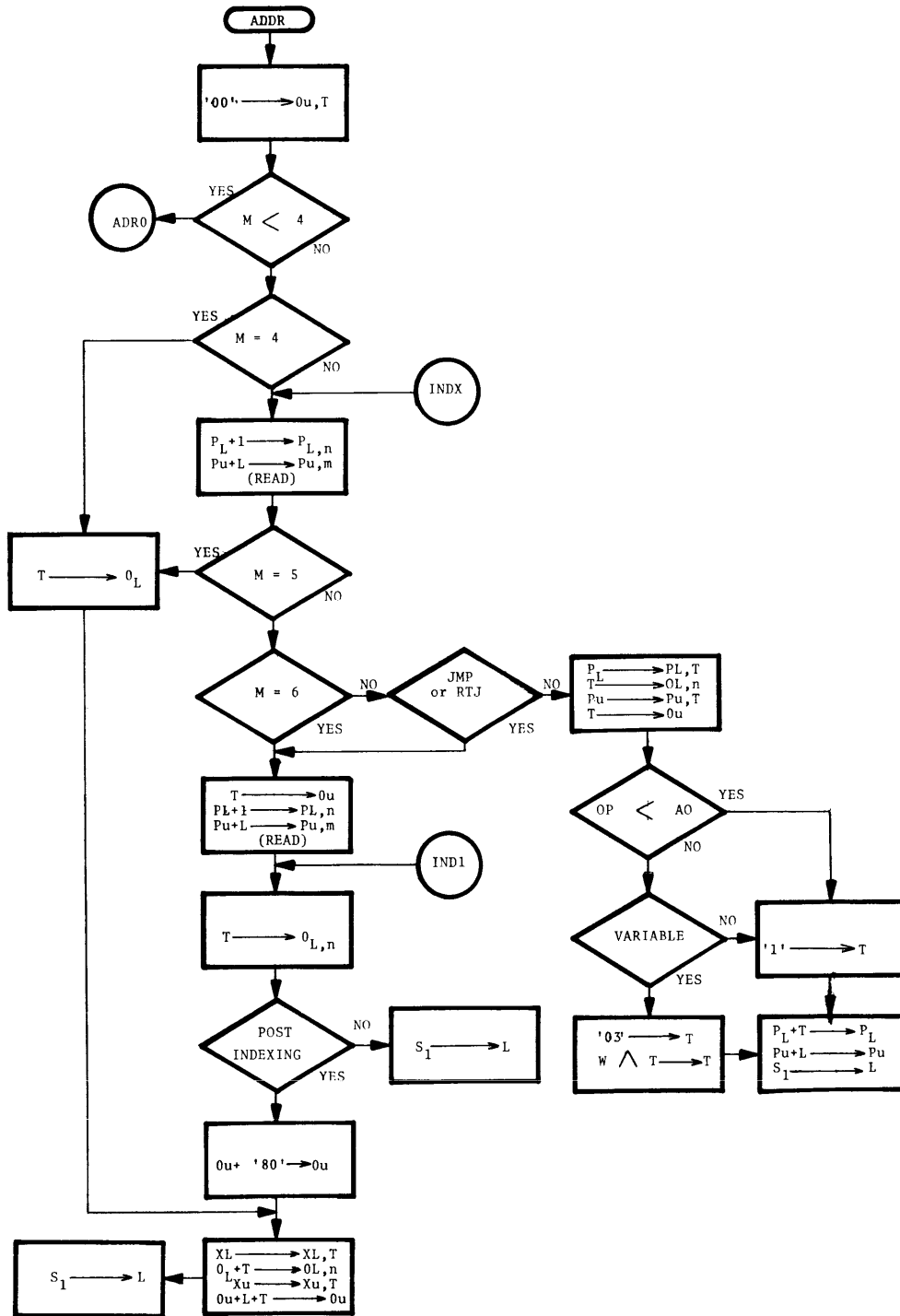


FIGURE 3. OPERAND ADDRESSING

OPERAND ADDRESSING

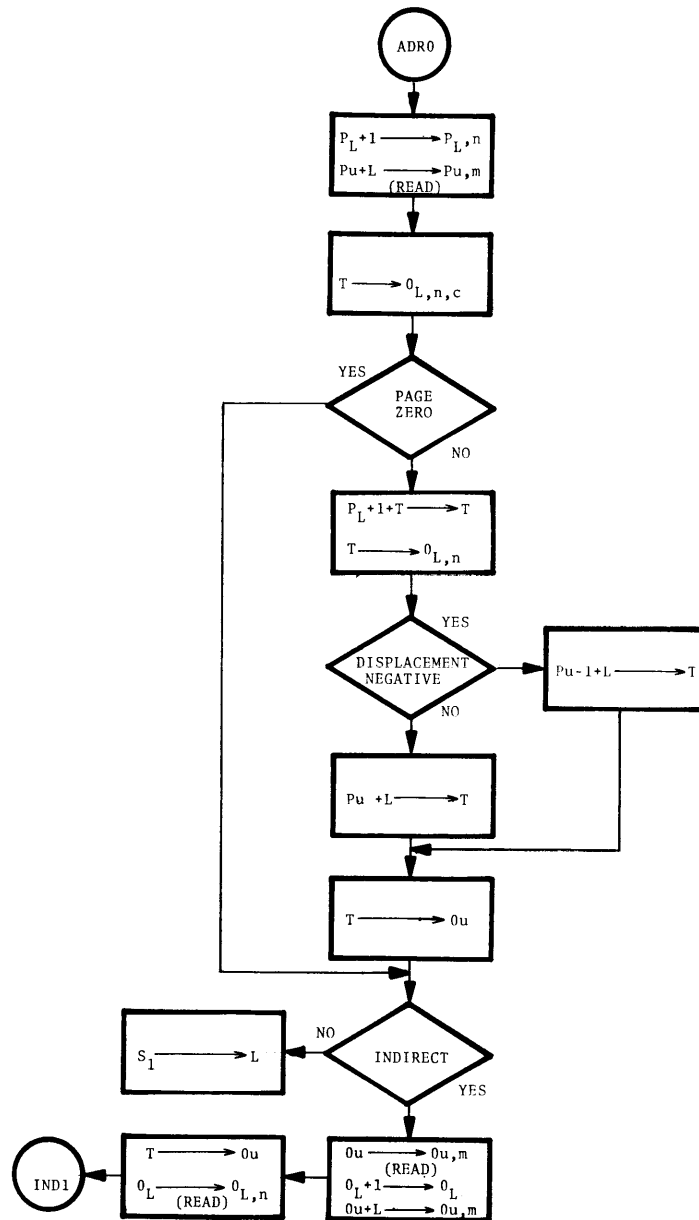
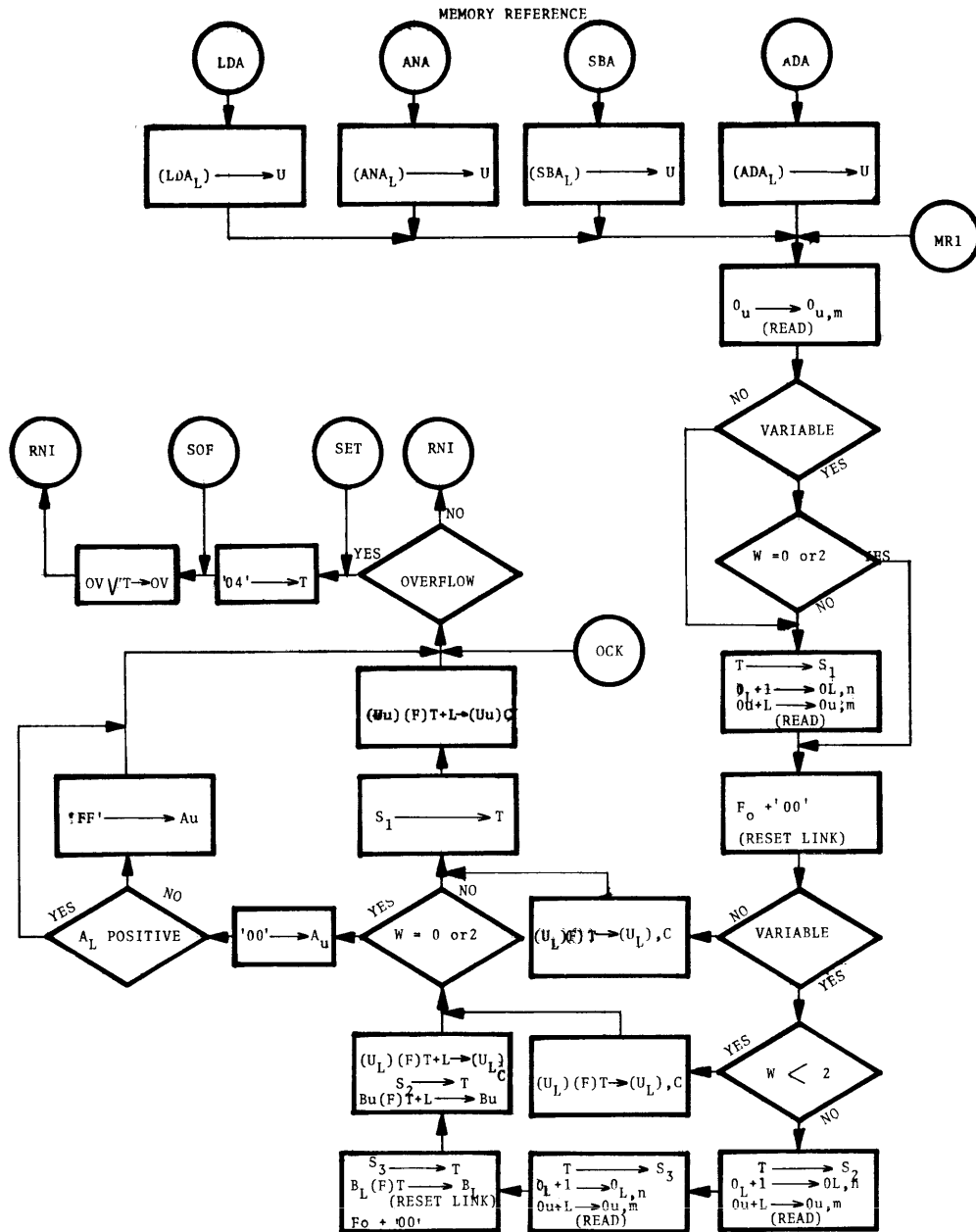


FIGURE 3. OPERAND ADDRESSING (CONTINUED)





	FIXED	W = 0	W = 1	W = 2	W = 3
A <sub>u</sub>	S1	Sign Extend	S1	Sign Extend	S1
A <sub>L</sub>	T	T	T	S2	S2
B <sub>u</sub>				S3	S3
B <sub>L</sub>				T	T

FIGURE 4. MEMORY REFERENCE

MEMORY REFERENCE

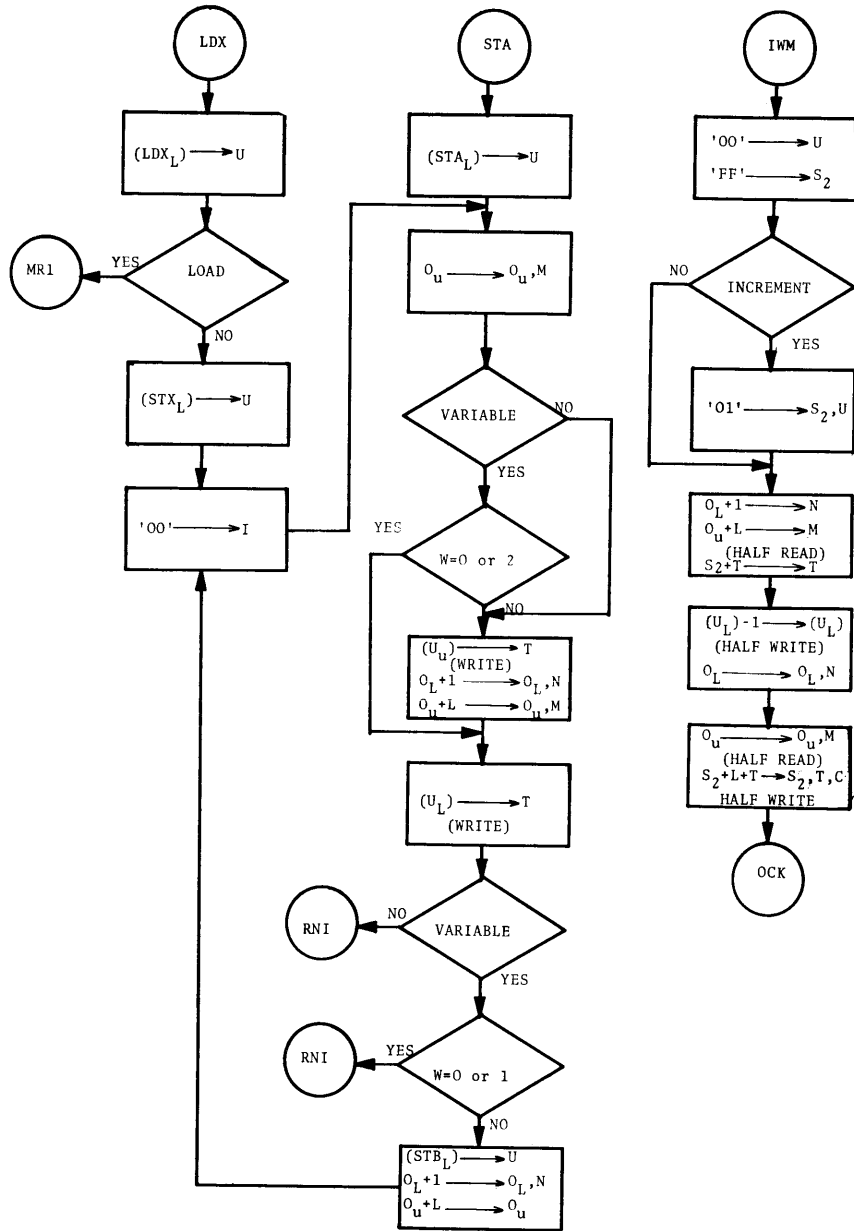


FIGURE 4. MEMORY REFERENCE (CONTINUED)

JUMP AND RETURN JUMP

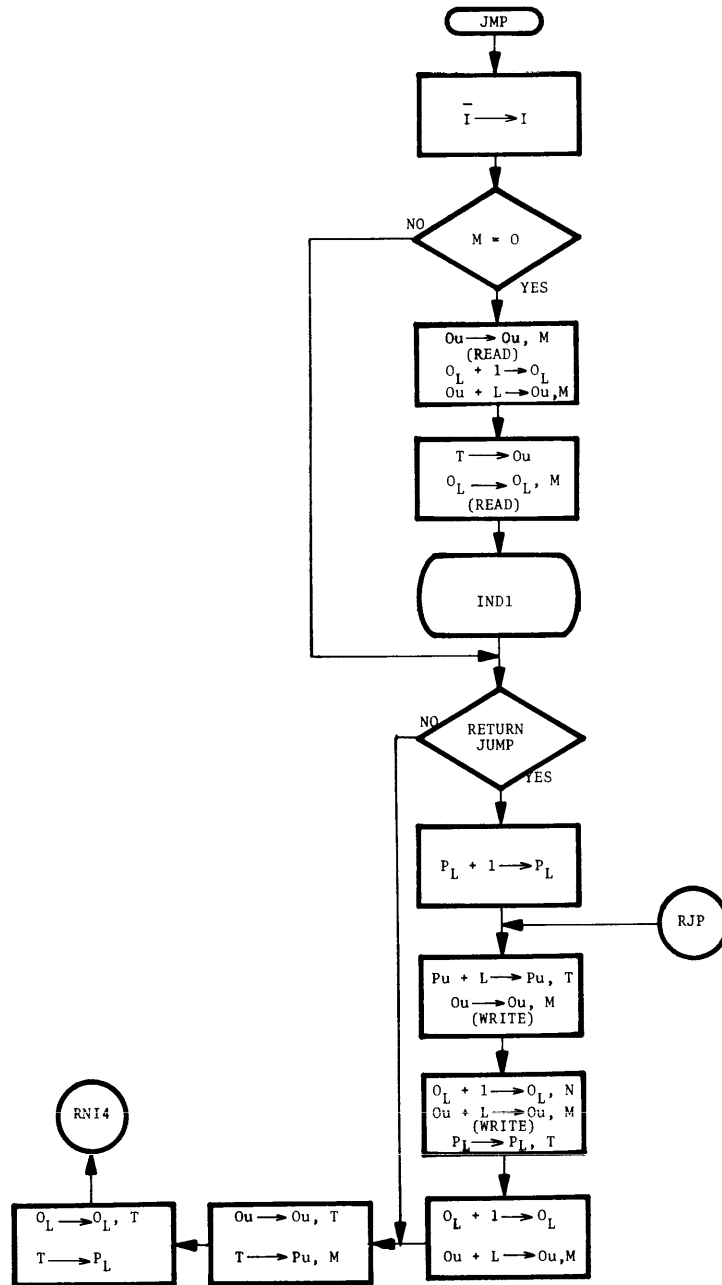


FIGURE 5. JUMP AND RETURN JUMP

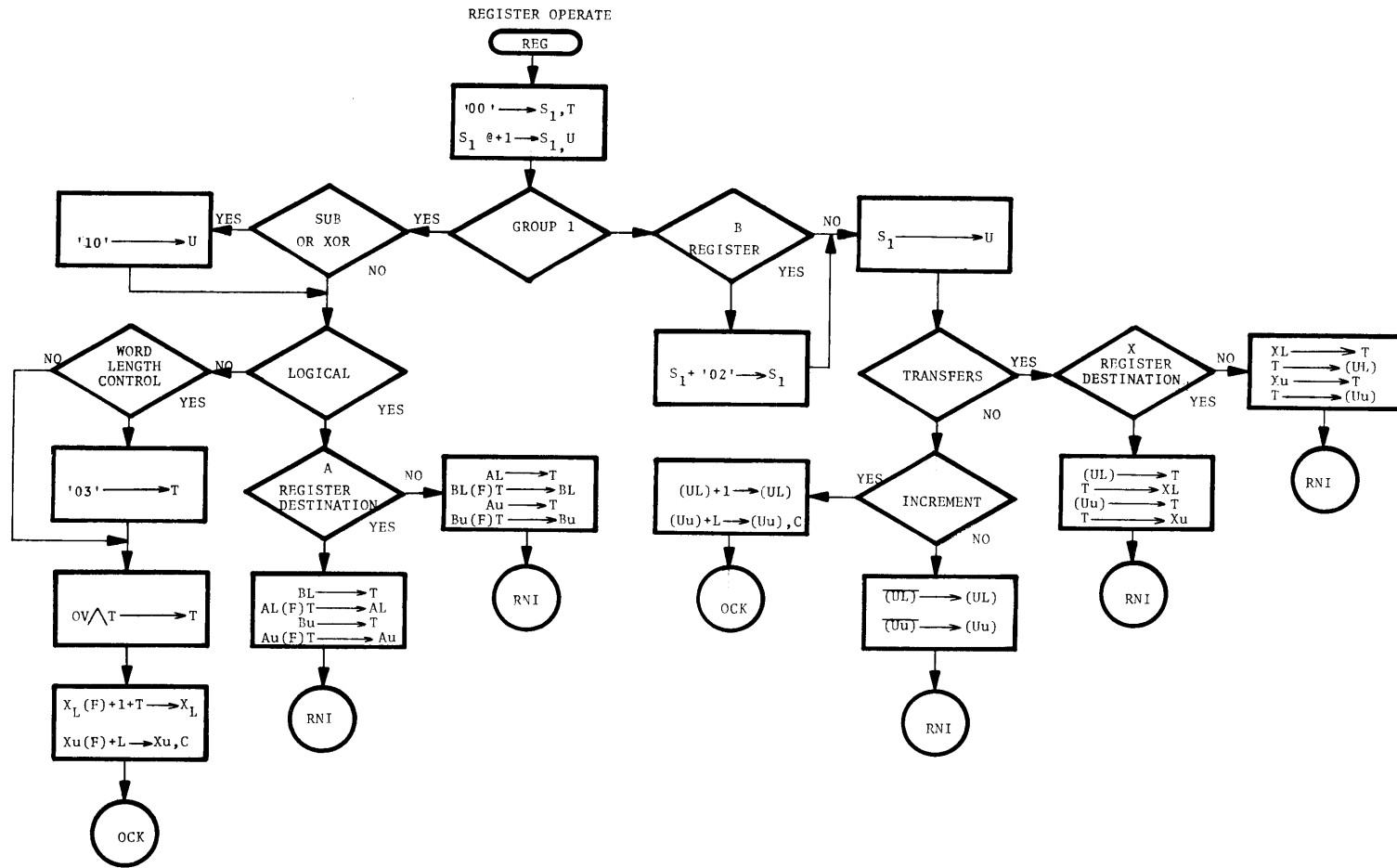


FIGURE 6. REGISTER OPERATE

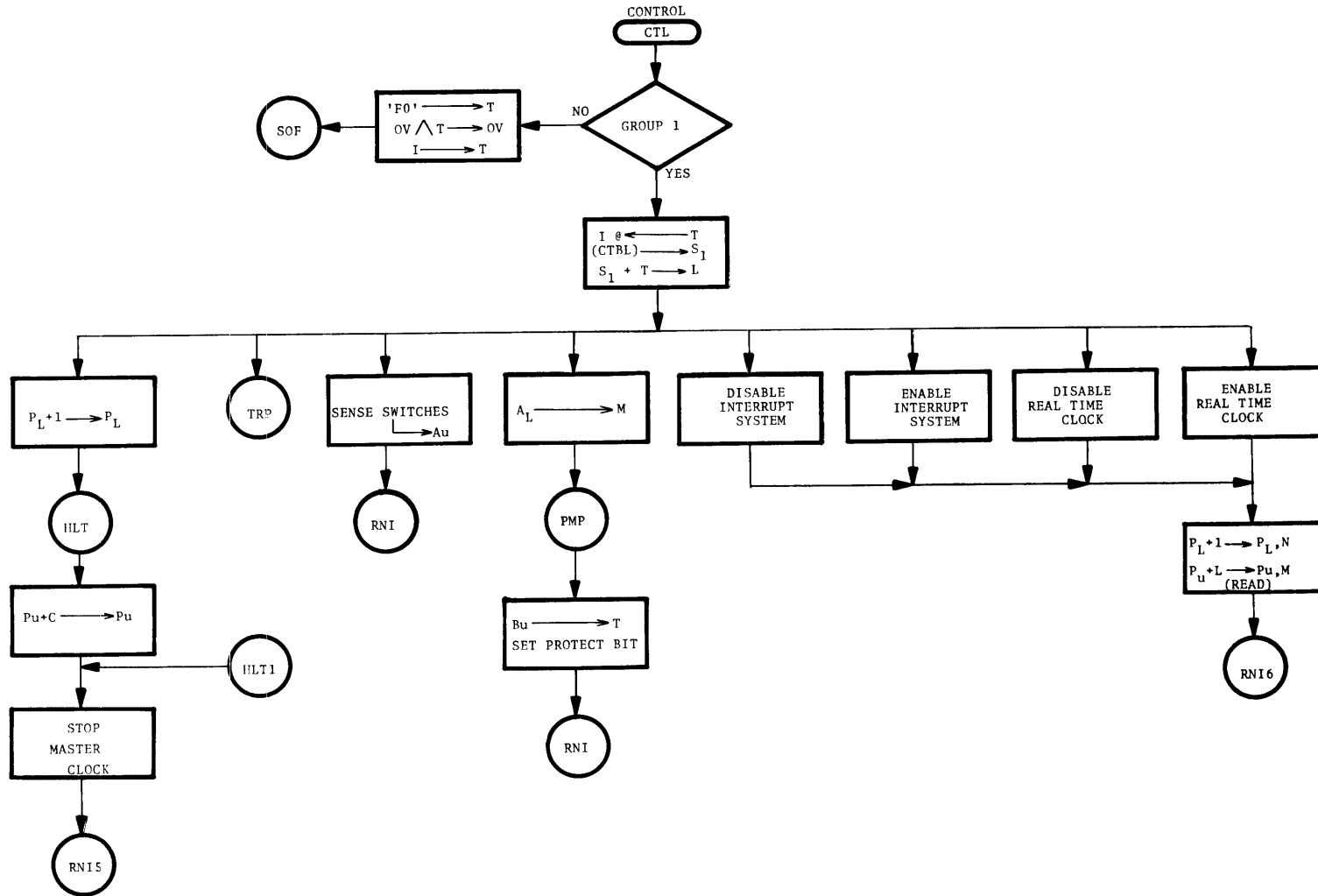


FIGURE 7. CONTROL

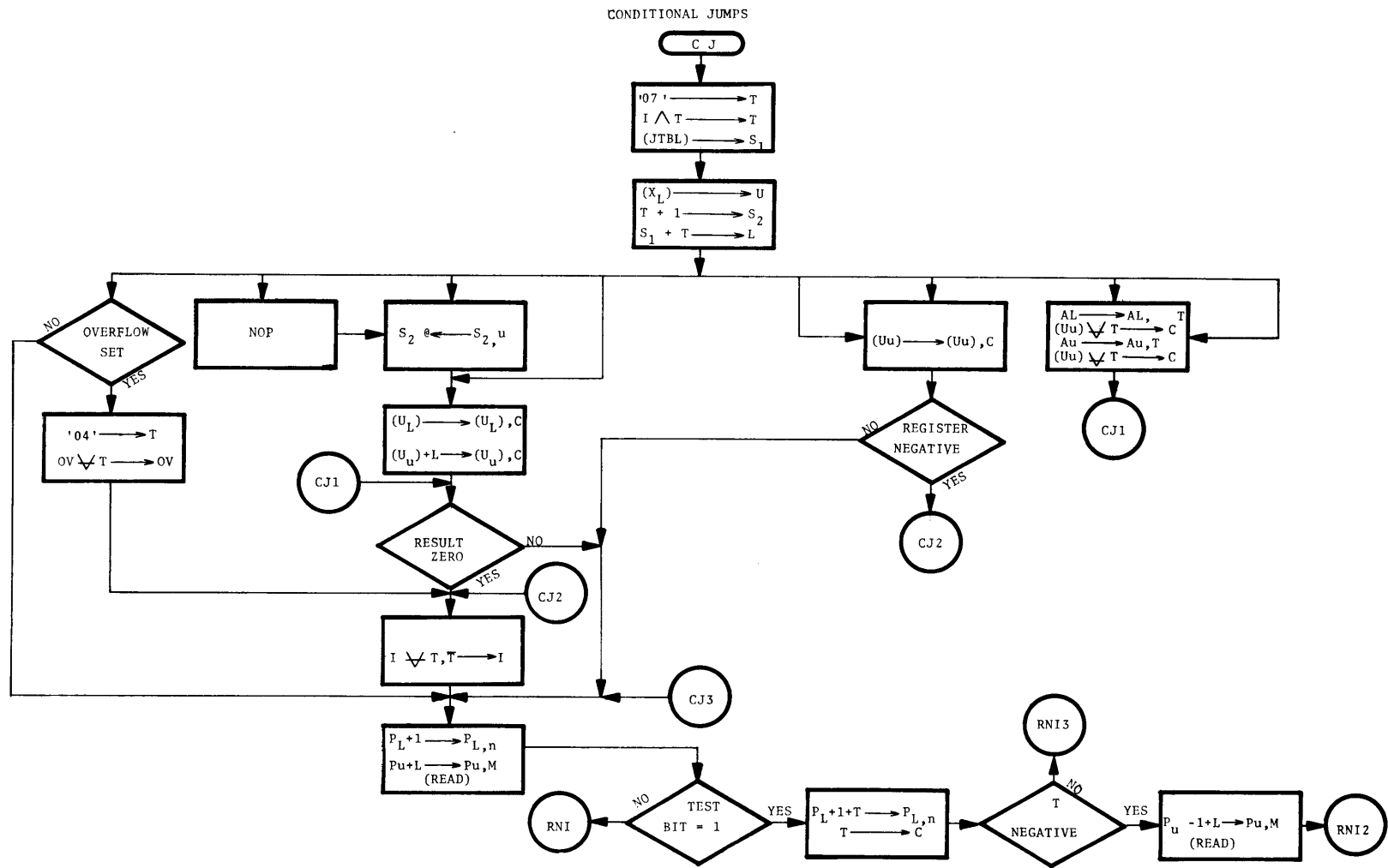


FIGURE 8. CONDITIONAL JUMPS

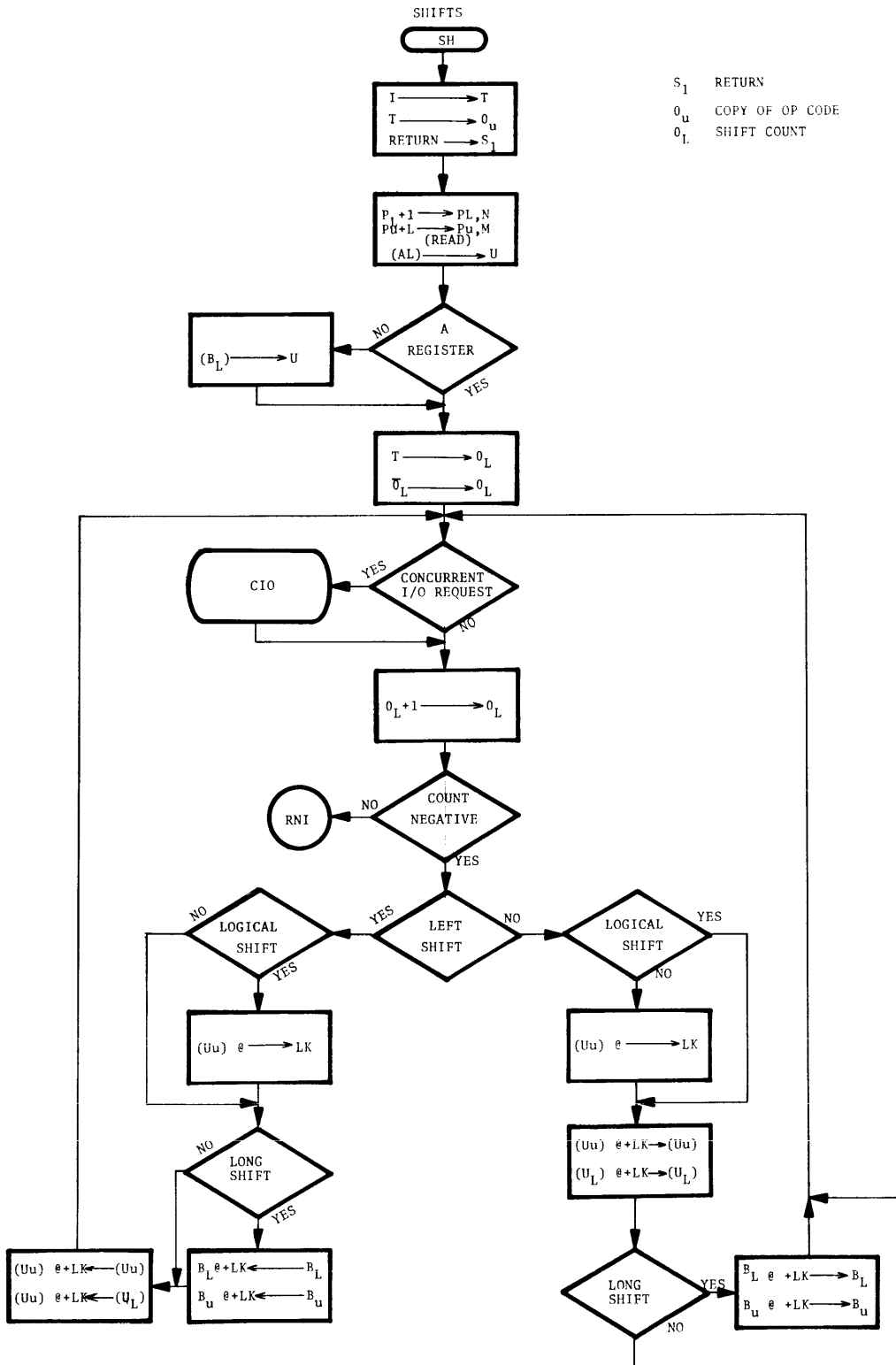


FIGURE 9. SHIFTS

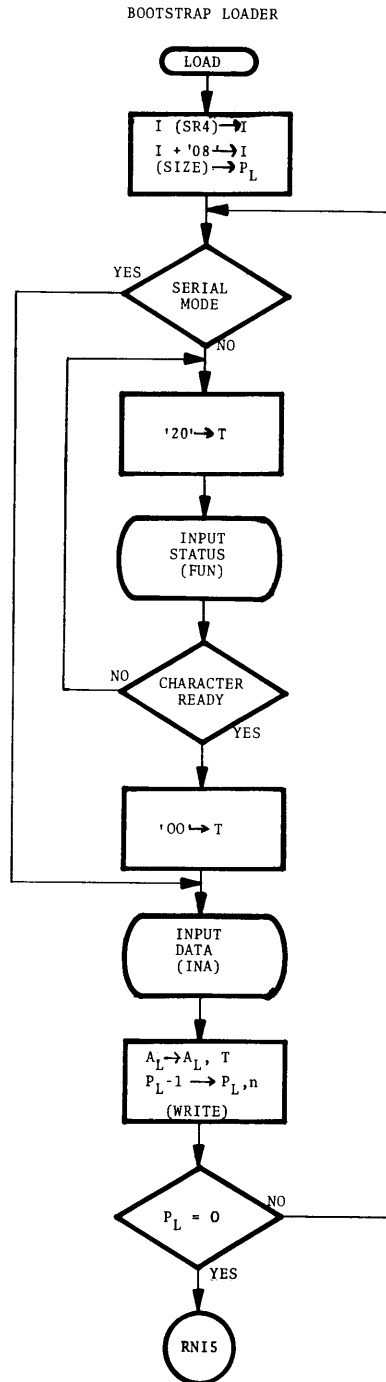


FIGURE 10. BOOTSTRAP LOADER



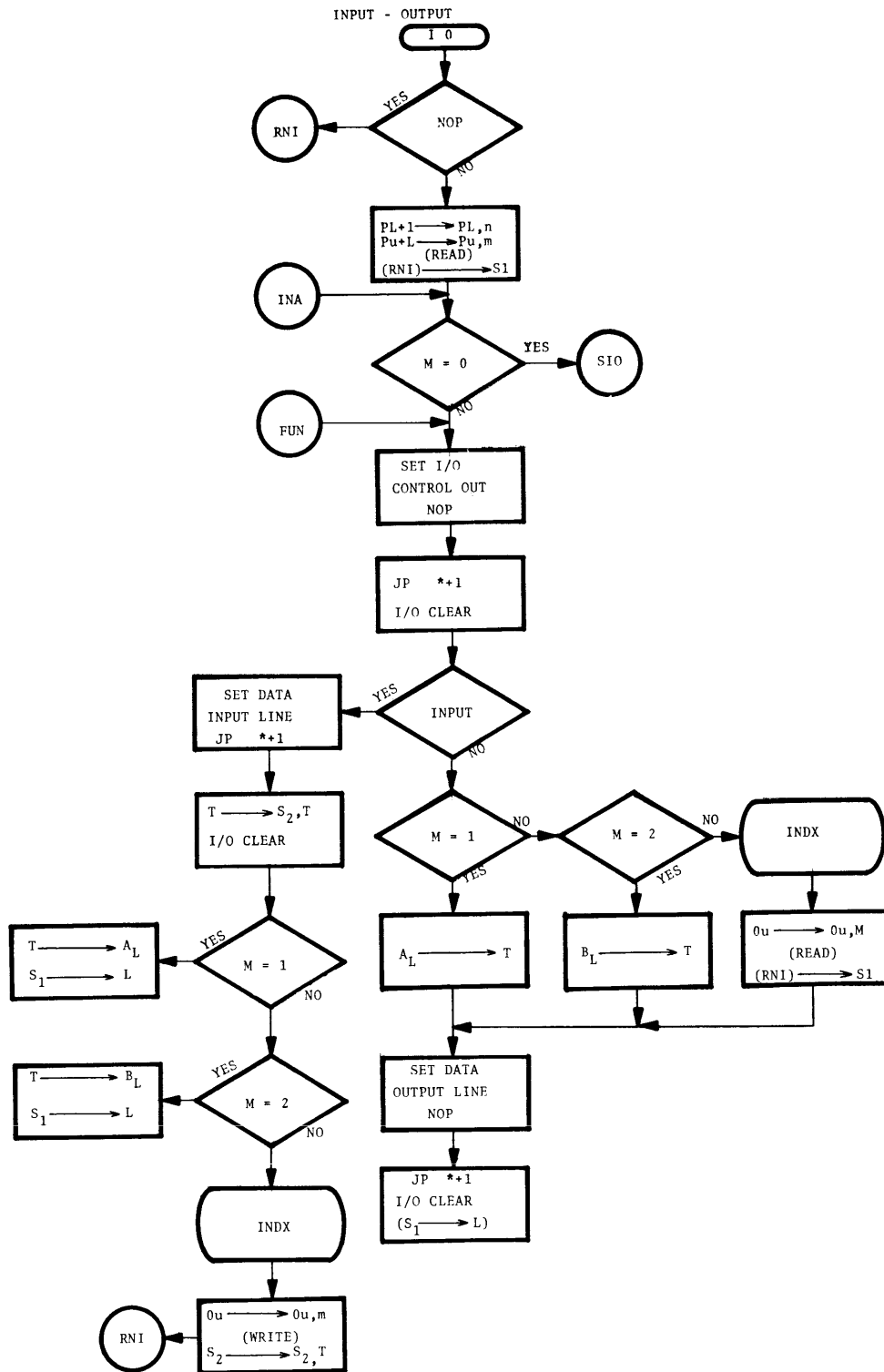


FIGURE 11. INPUT - OUTPUT

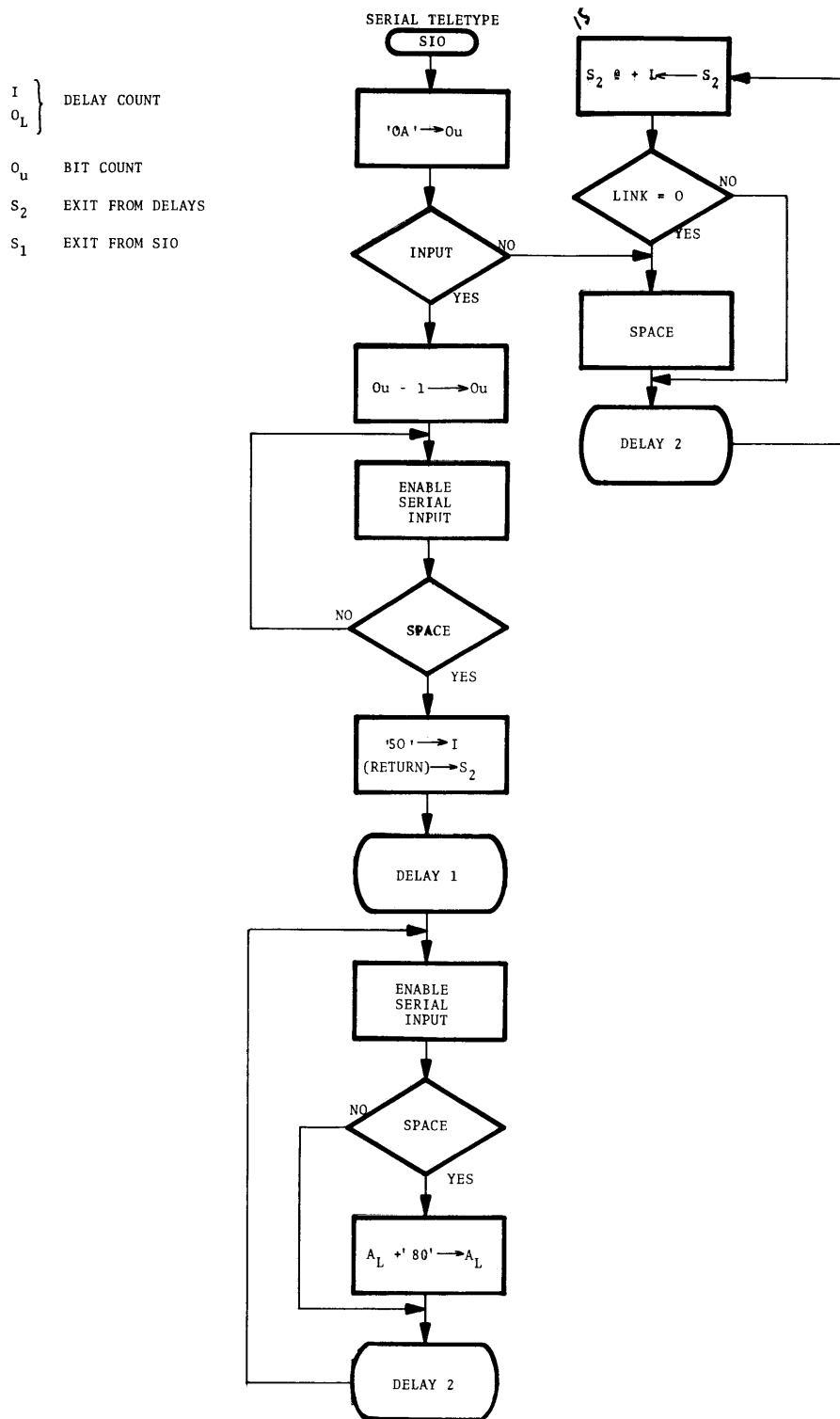


FIGURE 12. SERIAL TELETYPE

SERIAL TELETYPE DELAYS

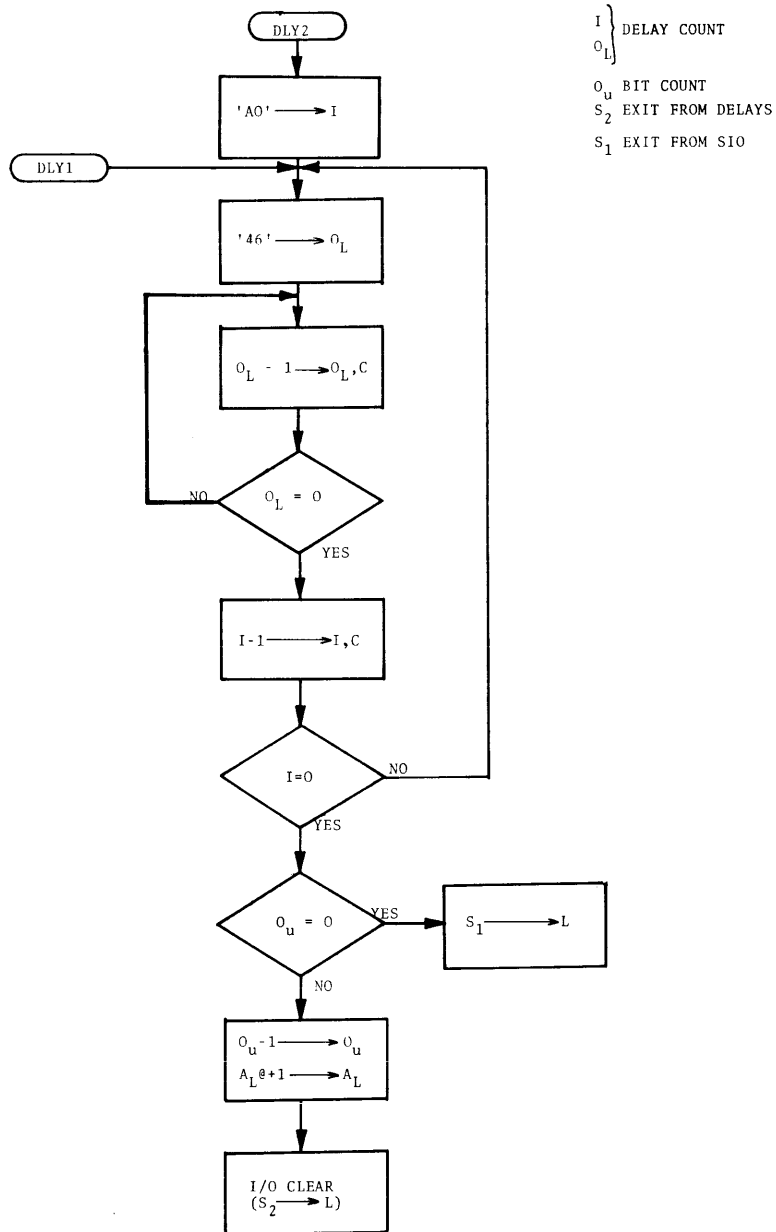


FIGURE 13. SERIAL TELETYPE DELAYS



CONCURRENT INPUT/OUTPUT

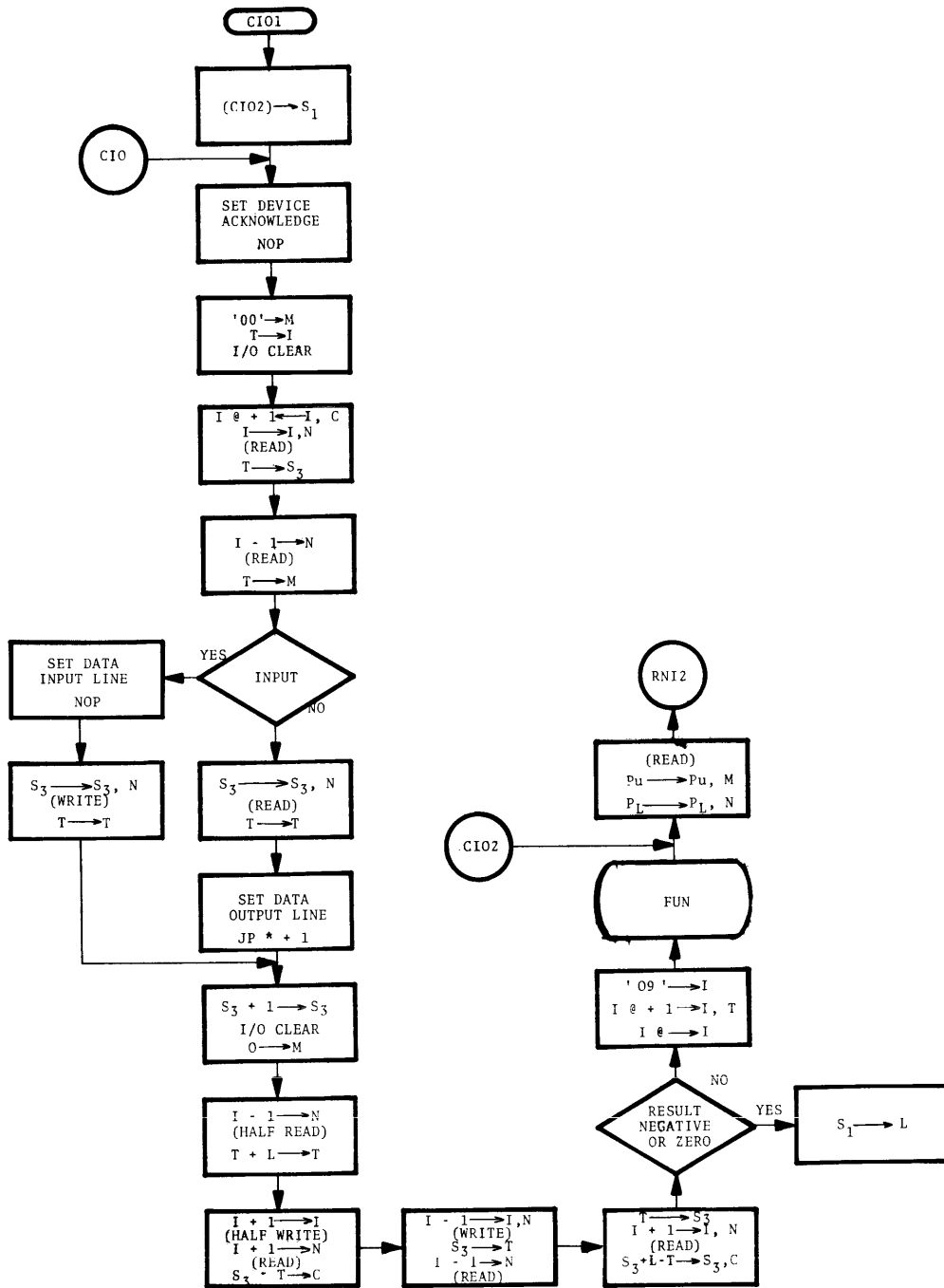
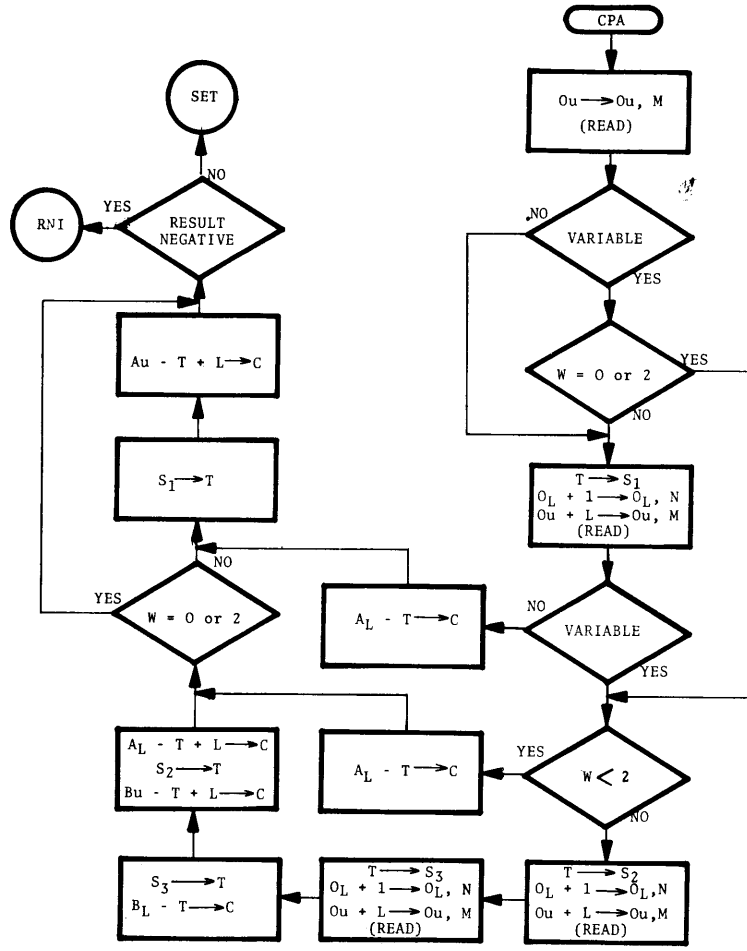


FIGURE 15. CONCURRENT INPUT/OUTPUT

COMPARE



	FIXED	W=0	W=1	W=2	W=3
Au	S <sub>1</sub>		S <sub>1</sub>		S <sub>1</sub>
A <sub>L</sub>	T	T	T	S <sub>2</sub>	S <sub>2</sub>
Bu				S <sub>3</sub>	S <sub>3</sub>
B <sub>L</sub>				T	T

FIGURE 16. COMPARE

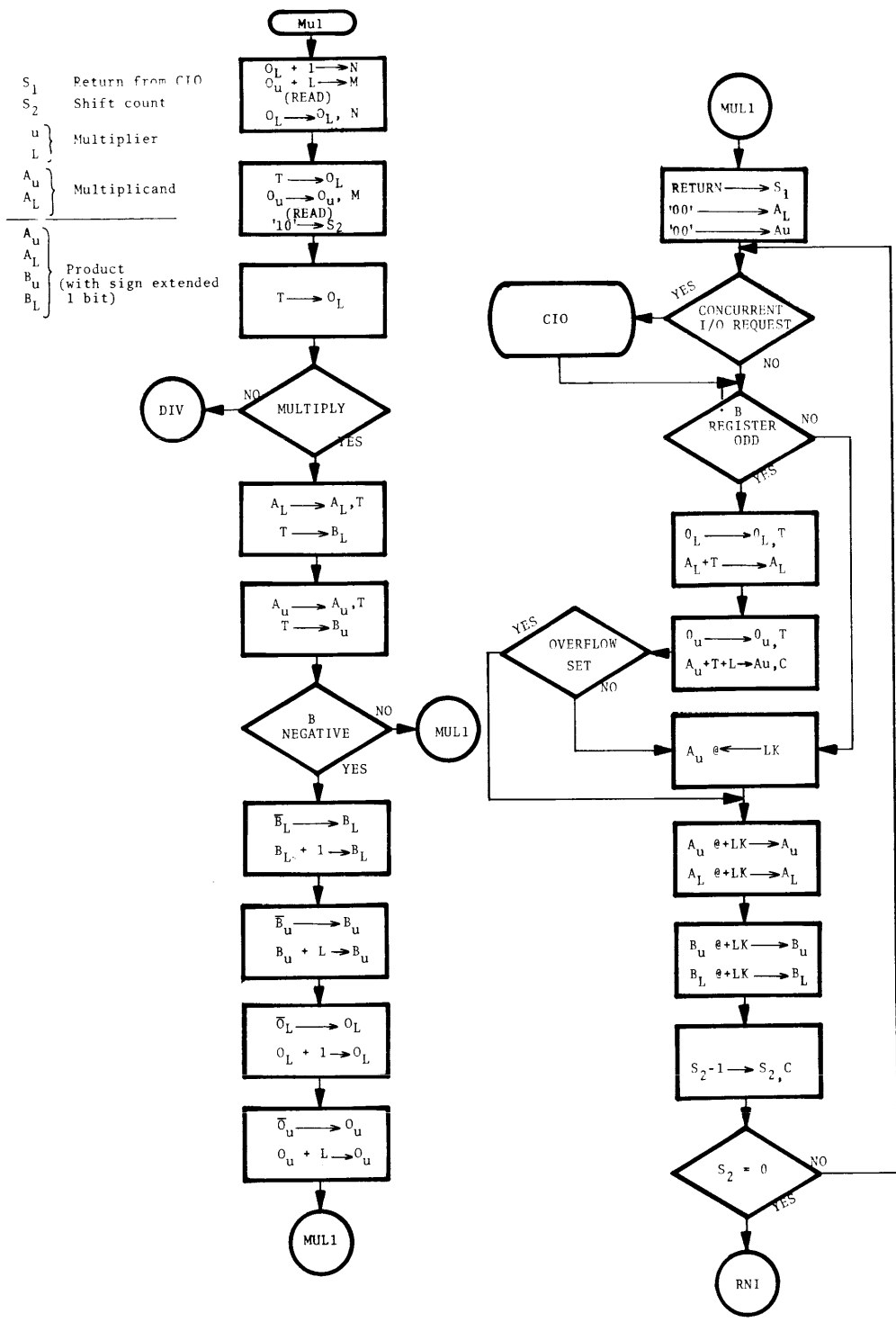
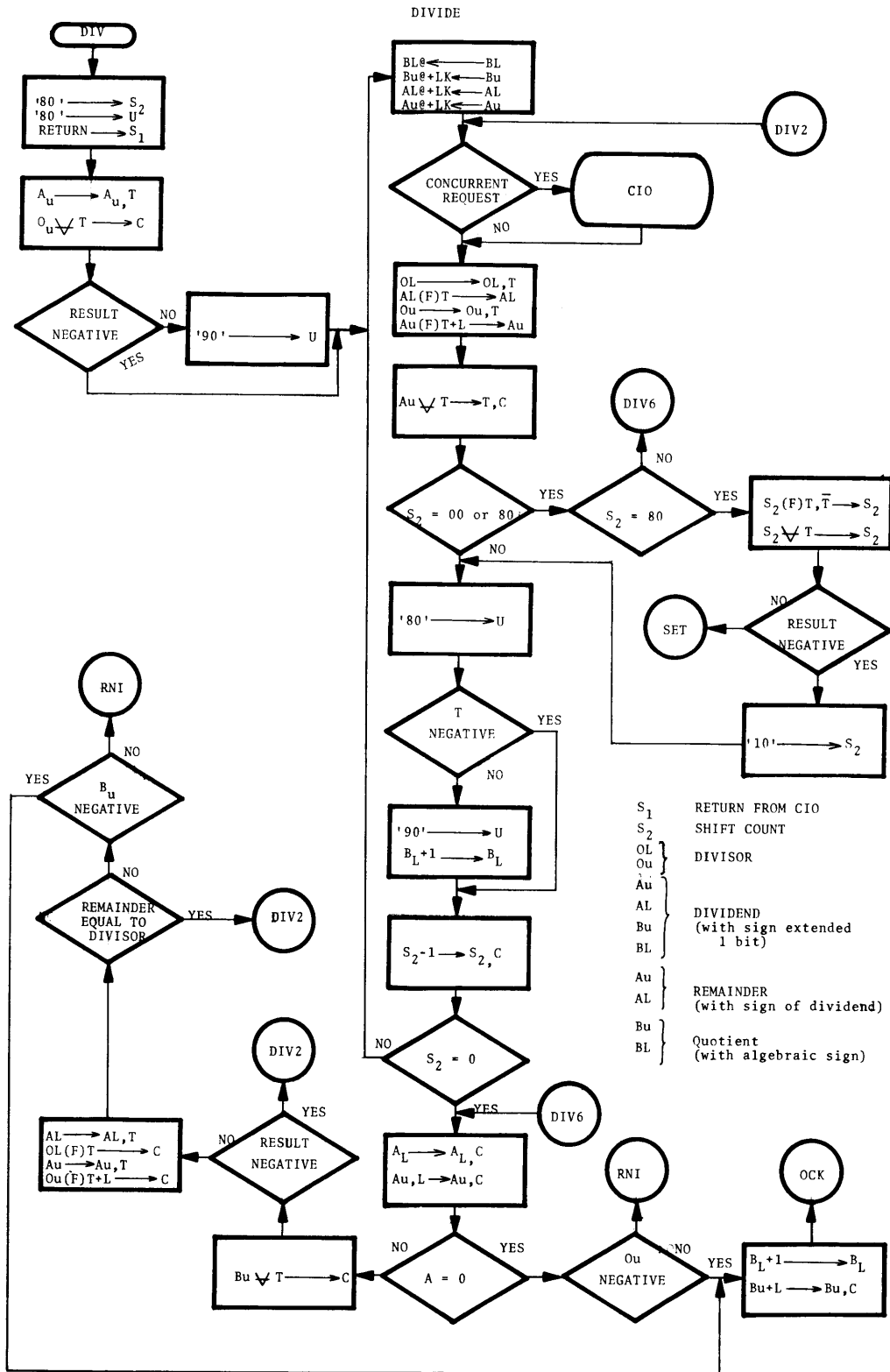


FIGURE 17. MULTIPLY



$S_1$  RETURN FROM CIO  
 $S_2$  SHIFT COUNT  
 $OL$   
 $Ou$  } DIVISOR  
 $Au$   
 $AL$  } DIVIDEND  
 $Bu$  (with sign extended  
 $BL$  1 bit)  
 $Au$  } REMAINDER  
 $AL$  (with sign of dividend)  
 $Bu$  }  
 $BL$  Quotient  
(with algebraic sign)

FIGURE 18. DIVIDE





# APPENDIX

## MICRO 810 SYSTEM LISTINGS

IDENT M810

```

*
*
* MICRO 810 SYSTEM
*
* FILE ALLOCATION
0000 F0 EQU 0 CONDITION FLAGS
0001 I EQU 1 INSTRUCTION REGISTER
0002 XL EQU 2 INDEX REGISTER
0003 XU EQU 3
0004 AL EQU 4 ACCUMULATOR
0005 AU EQU 5
0006 BL EQU 6 EXTENDED ACCUMULATOR
0007 BU EQU 7
0008 OL EQU 8 OPERAND ADDRESS
0009 OU EQU 9
000A PL EQU 10 PROGRAM COUNTER
000B PU EQU 11
000C S1 EQU 12 TEMPORARY STORAGE
000D S2 EQU 13
000E S3 EQU 14
000F OV EQU 15 OVERFLOW AND WORD LENGTH
0001 F1 EQU 1 USED WITH EXECUTE FOR ODD FILE
0000 SIZE EQU 0 SIZE OF BASIC LOADER
*
* ORG 0 BOARD 1
*
* READ NEXT INSTRUCTION
000 BF02 RNI0 CM OV CLEAR OV/W AND M
001 2B00 LF PU,X'00' CLEAR P
002 2A00 LF PL,X'00'
003 4010 TZ F0,X'10' INTERNAL INTERRUPT
004 15F8 JP INT2 YES
005 7110 K I,1 ENTER SENSE SWITCHES
006 4180 TZ I,X'80' SWITCH 4 ON
007 1574 JP LOAD YES, LOAD BOOT STRAP
008 2F00 RNI1 LF OV,X'00' CLEAR OV/W
009 CB02 RNI5 MM PU
00A AA03 RNI4 RN PL GET OP CODE
00B 1410 JP RNI6 IGNORE INTERRUPTS
00C 8A43 RNI IN PL UPDATE P
00D AB82 RNI3 RM PU,L
00E 4098 RNI2 TZ F0,X'98' TEST FOR INTERRUPTS
00F 15D3 JP INT SERVICE REQUEST
010 B120 RNI6 C I,T SAVE OP CODE
011 2C10 LF S1,OTAB+16 BASE ADDRESS OF TABLE
012 7129 KT* I,2 SHIFT RIGHT 4
013 8C20 A S1,T
014 61A0 CP I,X'A0' MEMORY REFERENCE
015 CC05 MK S1 NO
* YES, GET OPERAND ADDRESS
*
* OPERAND ADDRESSING
016 B901 ADDR CT OU CLEAR OU AND T
017 4104 TZ I,X'04' M < 4
018 142E JP ADR4 NO
019 8A43 IN PL GET ADDRESS BYTE
01A AB82 RM PU,L
01B B833 CN OL,T,C SET CONDITION CODE
01C 5101 TN I,X'01' PAGE ZERO

```

01D	1424		JP	ADR2	YES
01E	8A69		AT*	PL,I,T	ADD RELATIVE VALUE
01F	8823		CN	OL,T	
020	4002		TZ	F0,X'02'	DISPLACEMENT NEGATIVE
021	142C		JP	ADR3	YES
022	8B89		AT*	PU,L	ADD CARRY
023	B920	ADR1	C	OU,T	
024	5102	ADR2	TN	I,X'02'	INDIRECT
025	CC05		MK	S1	NO, EXIT
026	A902		RM	OU	GET ADDRESS AT
027	8840		I	OL	INDIRECT LOCATION
028	8982		AM	OU,L	
029	B920		C	OU,T	GET UPPER ADDR
02A	A803		RN	OL	
02B	1439		JP	IND1	GET LOWER ADDR
02C	9B89	ADR3	ST*	PU,L	BORROW FROM UPPER
02D	1423		JP	ADR1	
02E	5103	ADR4	TN	I,X'03'	M = 4
02F	1442		JP	ADR7	YES
030	8A43	INDX	IN	PL	
031	AB82		RM	PU,L	
032	5102		TN	I,X'02'	M = 5
033	1442		JP	ADR7	YES
034	4101		TZ	I,X'01'	M = 6
035	1444		JP	LIT	NO
036	B920	ADR5	C	OU,T	GET UPPER ADDR
037	8A43		IN	PL	
038	AB82		RM	PU,L	
039	B823	IND1	CN	OL,T	
03A	5980		TN	OU,X'80'	POST INDEXING
03B	CC05		MK	S1	NO, EXIT
03C	3980		AF	OU,X'80'	REMOVE BIT
03D	C201	ADR6	MT	XL	ADD X TO ADDR
03E	8823		AN	OL,T	
03F	C301		MT	XU	
040	89A0		A	OU,L,T	
041	CC05		MK	S1	EXIT
042	B820	ADR7	C	OL,T	GET BIAS
043	143D		JP	ADR6	
044	6190	LIT	CP	I,X'90'	JMP,RTJ,IBM, OR ORM
045	1436		JP	ADR5	YES
046	CA01		MT	PL	SET ADDR = P
047	B823		CN	OL,T	
048	CB01		MT	PU	
049	B920		C	OU,T	
04A	6160		CP	I,X'60'	FIXED LENGTH
04B	1453		JP	ADR9	YES
04C	5108		TN	I,X'08'	VARIABLE
04D	1453		JP	ADR9	YES
04E	1103		LT	X'03'	SET MASK
04F	EF29		NT*	OV,T	REMOVE W
050	8A20	ADR8	A	PL,T	ADJUST P
051	8B80		A	PU,L	
052	CC05		MK	S1	EXIT
053	1101	ADR9	LT	X'01'	1 TO 1
054	1450		JP	ADR8	
			*		
			* MEMORY REFERENCE		
055	16B4	LDA	LU	X'B4'	SET FOR LOAD
056	145C		JP	MR1	

057	16E4	ANA	LU	X'E4'	SET FOR AND
058	145C		JP	MR1	
059	1694	SBA	LU	X'94'	SET FOR SUBTRACT
05A	145C		JP	MR1	
05B	1684	ADA	LU	X'84'	SET FOR ADD
05C	A902	MR1	RM	OU	
05D	5108		TN	I,X'08'	VARIABLE
05E	1461		JP	MR2	NO
05F	5F01		TN	OV,X'01'	W=0 OR 1
060	1464		JP	MR3	YES
061	BC20	MR2	C	S1,T	GET AN OPERAND
062	8843		IN	OL	
063	A982		RM	OU,L	
064	8000	MR3	A	F0	RESET LINK
065	5108		TN	I,X'08'	VARIABLE
066	1480		JP	MR8	NO
067	5F02		TN	OV,X'02'	W < 2
068	147E		JP	MR7	YES
069	BD20		C	S2,T	GET AN OPERAND
06A	8843		IN	OL	
06B	A982		RM	OU,L	
06C	BE20		C	S3,T	GET AN OPERAND
06D	8843		IN	OL	
06E	A982		RM	OU,L	
06F	8000		A	F0	RESET LINK
070	0620		E	BL,2	OPERATE ON BL
071	CE01		MT	S3	
072	07A0		E	BU,10	OPERATE ON BU
073	CD01		MT	S2	
074	00B0		E	F0,11	OPERATE ON AL
075	5F01	MR4	TN	OV,X'01'	W= 0 OR 2
076	1482		JP	MR9	YES
077	CC01	MR5	MT	S1	
078	0180		E	F1,11	OPERATE ON AU OR XU
079	5001	OCK	TN	F0,X'01'	OVERFLOW SET
07A	140C		JP	RNI	NO
07B	1104	SET	LT	X'04'	SET MASK
07C	CF20	SOF	O	OV,T	SET BIT IN OV
07D	140C		JP	RNI	
07E	0030	MR7	E	F0,3	OPERATE ON AL
07F	1475		JP	MR4	
080	0020	MR8	E	F0,2	OPERATE ON AL OR XL
081	1477		JP	MR5	
082	2500	MR9	LF	AU,X'00'	CLEAR AU
083	4480		TZ	AL,X'80'	OPERAND POSITIVE
084	C560		U	AU,T,F	FF TO AU
085	1479		JP	OCK	
086	16B2	LDX	LU	X'B2'	LOAD X
087	5108		TN	I,X'08'	STORE
088	145C		JP	MR1	NO
089	16A2		LU	X'A2'	STORE X
08A	2100	ST4	LF	I,X'00'	CLEAR I
08B	148D		JP	ST1	
08C	16A4	ST1A	LU	X'A4'	STORE A
08D	C902	ST1	MM	OU	
08E	5108		TN	I,X'08'	VARIABLE
08F	1492		JP	ST2	NO
090	5F01		TN	OV,X'01'	W= 0 OR 2
091	1495		JP	ST3	YES
092	0111	ST2	ET	F1,1	STORE UPPER

093	8843		IN	OL	
094	8982		AM	OU,L	
095	0011	ST3	ET	F0,1	STORE LOWER
096	5108		TN	I,X'08'	VARIABLE
097	140C		JP	RNI	NO
098	5F02		TN	OV,X'02'	W= 0 OR 1
099	140C		JP	RNI	YES
09A	16A6		LU	X'A6'	STORE B
09B	8843		IN	OL	
09C	8980		A	OU,L	
09D	148A		JP	ST4	GO STORE B
09E	1600	IWM	LU	X'00'	CLEAR U
09F	CD60		O	S2,T,F	SET FOR DECREMENT
0A0	5108		TN	I,X'08'	
0A1	BD46		CU	S2,I	SET FOR INCREMENT
0A2	884B		IN*	OL	
0A3	A9AA		RM*	OU,L,H	HALF READ
0A4	8D29		AT*	S2,T	+1 OR -1
0A5	AC77		WS	S1,D,H	WRITE AND DECR S2 IF AN INCR
0A6	C803		MN	OL	
0A7	A922		RM	OU,H	HALF READ
0A8	8DB1		AT	S2,L,T,C	
0A9	A030		W	F0,H	HALF WRITE
0AA	1479		JP	OCK	CHECK FOR OVERFLOW

\*  
\* JUMP AND RETURN JUMP

0AB	D160	JMP	X	I,T,F	COMPLEMENT
0AC	4107		TZ	I,X'07'	M=0
0AD	14B5		JP	JM1	NO
0AE	A902		RM	OU	YES, INDIRLCT
0AF	8840		I	OL	
0B0	8982		AM	OU,L	
0B1	B920		C	OU,T	GET HIGH BYTE
0B2	A803		RN	OL	START MEMORY
0B3	2C18		LF	S1, PTR3	INDIRECT RETURN
0B4	1439		JP	IND1	CHECK FOR POST INDEXING
0B5	4108	JM1	TZ	I,X'08'	RETURN JUMP
0B6	14BF		JP	JM2	NO
0B7	8A40		I	PL	ADJUST P
0B8	8B81	RJP	AT	PU,L	
0B9	A912		WM	OU	STORE PU
0BA	8843		IN	OL	
0BB	A992		WM	OU,L	STORE PL
0BC	CA01		MT	PL	
0BD	8840		I	OL	ADJUST FOR NEW P
0BE	8982		AM	OU,L	
0BF	C901	JM2	MT	OU	SET NEW P
0C0	BB22		CM	PU,T	
0C1	C801		MT	OL	
0C2	BA20		C	PL,T	
0C3	140A		JP	RNI4	

\*  
\* REGISTER OPERATE

0C4	BC01	REG	CT	S1	CLEAR T AND S2
0C5	FC66		HU	S1,I,R	ADD COMMAND TO U
0C6	4108		TZ	I,X'08'	GROUP1
0C7	14DE		JP	REG3	NO
0C8	4101		TZ	I,X'01'	SUB OR XOR
0C9	1610		LU	X'10'	YES
0CA	4104		TZ	I,X'04'	INDEX CONTROL

0CB	14D8		JP	REG2	YES
0CC	4102		TZ	1,X'02'	A REG DESTINATION
0CD	14D3		JP	REG1	NO
0CE	C601		MT	BL	B OR A TO A, AND
0CF	C427		OS	AL,T	
0D0	C701		MT	RU	B XOR A TO A
0D1	C527		OS	AU,T	
0D2	140C		JP	RNI	
0D3	C401	REG1	MT	AL	A OR B TO B, AND
0D4	C627		OS	BL,T	
0D5	C501		MT	AU	A XOR B TO B
0D6	C727		OS	BU,T	
0D7	140C		JP	RNI	
0D8	4102	REG2	TZ	1,X'02'	WORD LENGTH CONTROL
0D9	1103		LT	X'03'	YES, SET MASK
0DA	EF29		NT*	OV,T	
0DB	8267		AS	XL,I,T	
0DC	8397		AS	XU,L,C	
0DD	1479		JP	OCK	CHECK FOR OVERFLOW
0DE	4101	REG3	TZ	1,X'01'	B REG USED
0DF	3C02		AF	S1,X'02'	YES
0E0	CC06		MU	S1	
0E1	4104		TZ	1,X'04'	TRANSFERS
0E2	14EB		JP	REG5	YES
0E3	4102		TZ	1,X'02'	COMPLEMENT
0E4	14E8		JP	REG4	YES
0E5	0440		E	AL,4	ADD 1
0E6	0590		E	AU,9	ADD CARRY
0E7	1479		JP	OCK	CHECK FOR OVERFLOW
0E8	D467	REG4	XS	AL,T,F	1'S COMPLEMENT
0E9	D567		XS	AU,T,F	
0EA	140C		JP	RNI	
0EB	4102	REG5	TZ	1,X'02'	X REG SOURCE
0EC	14F2		JP	REG6	YES
0ED	0401		ET	AL	A OR B TO T
0EE	B220		C	XL,T	I TO X
0EF	0501		ET	AU	
0F0	B320		C	XU,T	
0F1	140C		JP	RNI	
0F2	C201	REG6	MT	XL	X TO T
0F3	B427		CS	AL,T	T TO A OR B
0F4	C301		MT	XU	
0F5	B527		CS	AU,T	
0F6	140C		JP	RNI	

\*

\* RIGHT SHIFTS

0F7	4908	SR	TZ	0U,X'08'	LOGICAL
0F8	F10F		HS*	F1	NO, SET LINK
0F9	F1A7		HS	F1,L,R	RIGHT 1
0FA	F0A7		HS	F0,L,R	RIGHT 1
0FB	5902		TN	0U,X'02'	LONG SHIFT
0FC	1564		JP	SH1	
0FD	F7A0		H	RU,L,R	RIGHT 1
0FE	F6A0		H	BL,L,R	RIGHT 1
0FF	1564		JP	SH1	

\*

URG 256 BOARD 2

\*

\* OP CODE JUMP TABLE

100	1510	OTAB	JP	CTL	CONTROL
-----	------	------	----	-----	---------

101	1531	JP	CJ	CONDITIONAL JUMPS
102	155A	JP	SH	SHIFTS
103	1586	JP	IO	INPUT/OUTPUT
104	14C4	JP	REG	REGISTER OPERATE
105	1C00	JP	SP.	
106	14AB	JP	JMP	JUMP AND RETURN JUMP
107	149E	JP	IWM	INCREMENT AND DECREMENT MEMORY
108	1486	JP	LDX	LOAD AND STORE X
109	1C01	JP	MUL.	
10A	145B	JP	ADA	ADD
10B	1459	JP	SBA	SUBTRACT
10C	1C02	JP	CPA.	
10D	1457	JP	ANA	AND
10E	1455	JP	LDA	LOAD A
10F	148C	JP	STA	STORE A

\*  
\* CONTROL

110	4108	CTL	TZ	I,X'08'	
111	152D		JP	GP2	OVERFLOW AND WORD LENGTH
112	F109		HT*	I	
113	2C15		LF	S1,CTRL	
114	8C25		AK	S1,T	TABLE JUMP
115	8A40	CTRL	I	PL	HALT
116	152A		JP	HLT	
117	15E4		JP	TRP	TRAP
118	14B5	PIR3	JP	JM1	INDIRECT FROM ADDR TO JUMP
119	7510		K	AU,1	ENTER SENSE SWITCHES
11A	140C		JP	RNI	
11B	C402		MM	AL	PROTECT MEMORY PAGE
11C	1527		JP	PMP	
11D	1704		LS	X'04'	DISABLE INTERRUPT SYSTEM
11E	1524		JP	FC1	
11F	1708		LS	X'08'	ENABLE INTERRUPT SYSTEM
120	1524		JP	EC1	
121	1710		LS	X'10'	DISABLE REAL TIME CLOCK
122	1524		JP	EC1	
123	1720		LS	X'20'	ENABLE REAL TIME CLOCK
124	8A43	EC1	IN	PL	
125	AB82		RM	PU,L	
126	1410		JP	RNI6	BY PASS INTERRUPT CHECK
127	C701	PMP	MT	BU	
128	1740		LS	X'40'	SET PROTECT STATUS
129	140C		JP	RNI	
12A	8B80	HLT	A	PU,L	ADJUST P
12B	1780	HLT1	LS	X'80'	STOP CLOCK
12C	1409		JP	RNI5	
12D	11F0	GP2	LT	X'F0'	SET MASK
12E	EF20		N	OV,T	REMOVE STATUS
12F	C101		MT	I	
130	147C		JP	SOF	GO SET NEW STATUS

\*  
\* CONDITIONAL JUMPS

131	1107	CJ	LT	X'07'	MASK FOR CONDITION
132	E129		NT*	I,I	REMOVE OP CODE
133	2C4E		LF	S1,JTBL	BASE TABLE ADDRESS
134	1602		LU	X'02'	SET FOR X
135	BD60		C	S2,I,T	
136	8C25		AK	S1,T	DO A TABLE JUMP
137	5F04	J0	IN	OV,X'04'	OVERFLOW TEST
138	1540		JP	CJ3	NO

139	1104		LT	X'04'	
13A	DF20		X	OV,T	RESET OVERFLOW
13B	153F		JP	CJ2	
13C	C017	J3	MS	F0,C	TEST LOW BYTE
13D	C197		MS	F1,L,C	TEST HIGH BYTE
13E	4004	CJ1	IZ	F0,X'04'	RESULT ZERO
13F	D160	CJ2	X	I,T,F	YES, FLIP TEST BIT
140	8A43	CJ3	IN	PL	GET DISPLACEMENT
141	AB82		RM	PU,L	
142	5108		TN	I,X'08'	CONDITION MET
143	140C		JP	RNI	NO
144	8A63		AN	PL,I,T	ADD DISPLACEMENT
145	B030		C	F0,T,C	LOOK AT T
146	5002		TN	F0,X'02'	T NEGATIVE
147	140D		JP	RNI3	NO
148	AB42		RM	PU,D	ADJUST PAGE
149	140E		JP	RNI2	
14A	C117	J5	MS	F1,C	LOOK AT AU OR XU
14B	4002		IZ	F0,X'02'	NEGATIVE
14C	153F		JP	CJ2	YES
14D	1540		JP	CJ3	NO
* * CONDITIONAL JUMP TABLE					
14E	1537	JTBL	JP	J0	OVERFLOW
14F	1000		L	X'00'	NOP
150	FD06		HU	S2	SET FOR A OR B
151	153C		JP	J3	
152	1604		LU	X'04'	SET FOR A
153	154A		JP	J5	
154	1606		LU	X'06'	SET FOR B
155	C401	J7	MT	AL	
156	D03F		XS*	F0,T,C	COMPARE LOWER
157	C501		MT	AU	
158	D1BF		XS*	F1,L,T,C	COMPARE UPPER
159	153E		JP	CJ1	TEST RESULT
* * SHIFTS					
15A	C101	SH	MT	I	SAVE OP CODE
15B	B920		C	OU,T	
15C	2C66		LF	S1,SH2	SET ADDR FOR CONCURRENT I/O
15D	8A43		IN	PL	GET SHIFT COUNT
15E	AB82		RM	PU,L	
15F	1604		LU	X'04'	SET FOR A
160	4901		TZ	OU,X'01'	
161	1606		LU	X'06'	SET FOR B
162	B820		C	OL,T	
163	D860		X	OL,T,F	
164	4008	SH1	IZ	F0,X'08'	CONCURRENT I/O REQUEST
165	1C14		JP	C10	YES
166	8840	SH2	I	OL	ADD 1 TO COUNT
167	5880		TN	OL,X'80'	COUNT NEGATIVE
168	140C		JP	RNI	NO
169	4904		TZ	OU,X'04'	LEFT SHIFT
16A	14F7		JP	SR	NO
16B	5908		TN	OU,X'08'	LOGICAL
16C	F10F		HS*	F1	YES, SET LINK
16D	5902		TN	OU,X'02'	LONG SHIFT
16E	1571		JP	SL1	NO
16F	F680		H	BL,L	LEFT 1
170	F780		H	BU,L	LEFT 1



171	F087	SL1	HS	F0,L	LEFT 1
172	F187		HS	F1,L	LEFT 1
173	1564		JP	SH1	
* * BOOTSTRAP LOADER					
174	7120	LOAD	K	I,2	SHIFT RIGHT
175	3108		AF	I,X'08'	REMOVE BITS
176	2A00		LF	PL,SIZE	SET LOADER SIZE
177	5101	LOD1	TN	I,X'01'	SERIAL MODE
178	157F		JP	LOD3	YES
179	1120	LOD5	LT	X'20'	SET FOR STATUS IN
17A	2C7C		LF	S1,LOD2	SET RETURN
17B	158D		JP	FUN	GET STATUS
17C	5402	LOD2	TN	AL,X'02'	CHARACTER READY
17D	1579		JP	LOD5	NO
17E	1100		LT	X'00'	SET FOR DATA IN
17F	2C81	LOD3	LF	S1,LOD4	SET RETURN
180	158B		JP	INA	GET DATA
181	C401	LOD4	MT	AL	SET DATA IN T
182	AA53		WN	PL,D	STORE BYTE
183	4AFF		TZ	PL,X'FF'	DONE LOADING
184	1577		JP	LOD1	NO
185	1409		JP	RNI5	YES
* * INPUT-OUTPUT					
186	4104	I0	TZ	I,X'04'	NOP
187	140C		JP	RNI	YES
188	8A43		IN	PL	GET DEVICE ADDRESS
189	AB82		RM	PU,L	
18A	2CA3		LF	S1,I0K5	RETURN TO RNI
18B	5103	INA	TN	I,X'03'	SERIAL MODE
18C	15B4		JP	SIO	YES
18D	7090	FUN	K	F0,9	CONTROL OUT
18E	1000		L	X'00'	NOP
18F	1590		JP	I01	
190	7080	I01	K	F0,8	CLEAR
191	4108		TZ	I,X'08'	INPUT
192	15A4		JP	OUI	NO
193	70E0		K	F0,14	DATA IN
194	1595		JP	I02	
195	BD21	I02	CT	S2,T	GET DATA
196	7080		K	F0,8	CLEAR
197	5102		TN	I,X'02'	M = 1
198	15A0		JP	I04	YES
199	5101		TN	I,X'01'	M = 2
19A	15A2		JP	I05	
19B	2C9D		LF	S1,I03	
19C	1430		JP	INDX	GET STORE ADDRESS
19D	A912	I03	WM	OU	
19E	CD01		MT	S2	STORE BYTE
19F	140C		JP	RNI	
1A0	B420	I04	C	AL,T	PUT IN A
1A1	CC05	I04A	MK	S1	
1A2	B620	I05	C	BL,T	PUT IN B
1A3	140C	I0K5	JP	RNI	
1A4	5102	OUT	TN	I,X'02'	M = 1
1A5	15AD		JP	I07	YES
1A6	5101		TN	I,X'01'	M = 2
1A7	15B2		JP	I010	YES
1A8	2CAA		LF	S1,I06	

1A9	1430		JP	INDX	GET OUTPUT ADDRESS
1AA	A902	I06	RM	OU	
1AB	2C9F		LF	S1,I04-1	SET RETURN
1AC	15AE		JP	I08	
1AD	C401	I07	MT	AL	A TO T
1AE	70A0	I08	K	F0,10	OUTPUT
1AF	1000		L	X'00'	NOP
1B0	15B1		JP	I09	
1B1	7C85	I09	KK	S1,8	CLEAR AND EXIT
1B2	C601	I010	MT	BL	B TO T
1B3	15AE		JP	I08	

\*  
\* SERIAL TELETYPE

1B4	290A	S10	LF	OU,X'0A'	SET BIT COUNT
1B5	4108		TZ	I,X'08'	INPUT
1B6	15C4		JP	SOUT	NO
1B7	9940		D	OU	ADJUST BIT COUNT
1B8	1701	S101	LS	X'01'	ENABLE SERIAL TTY
1B9	5040		TN	F0,X'40'	START BIT
1BA	15B8		JP	S101	NO
1BB	2148		LF	I,X'48'	SET DELAY COUNT (220 NS)
1BC	2DBE		LF	S2,S101	SET DELAY RETURN
1BD	15C7		JP	DLY1	
1BE	1701	S101	LS	X'01'	ENABLE SERIAL TTY
1BF	4040		TZ	F0,X'40'	SPACE
1C0	3480		AF	AL,X'80'	YES, REMOVE BIT
1C1	15C6		JP	DLY2	GO, DELAY
1C2	FD80	S100	H	S2,L	GET LINK BIT
1C3	5D01		TN	S2,X'01'	CURRENT BIT, A ZERO
1C4	7080	SOUT	K	F0,11	YES, SPACE
1C5	2DC2		LF	S2,S100	SET DELAY RETURN
1C6	2190	DLY2	LF	I,X'90'	SET DELAY COUNT (220 NS)
1C7	2846	DLY1	LF	OL,X'46'	
1C8	9850	DL1	D	OL,C	REDUCE LOW COUNTER
1C9	5004		TN	F0,X'04'	COUNTER ZERO
1CA	15C8		JP	DL1	NO
1CB	9150		D	I,C	REDUCE UPPER COUNTER
1CC	5004		TN	F0,X'04'	COUNTER ZERO
1CD	15C7		JP	DLY1	NO
1CE	590F		TN	OU,X'0E'	BIT COUNTER ZERO
1CF	CC05		MK	S1	YES, EXIT
1D0	9940		D	OU	
1D1	F460		H	AL,I,R	SHIFT LOW BIT TO LINK
1D2	7D85		KK	S2,8	CLEAR AND EXIT (MARK)

\*  
\* INTERRUPTS

1D3	4F80	INT	TZ	OV,X'80'	POWER FAIL IN PROGRESS
1D4	1410		JP	RN16	YES
1D5	4010		TZ	F0,X'10'	INTERNAL
1D6	15E3		JP	INT0	YES
1D7	4008		TZ	F0,X'08'	CONCURRENT I/O
1D8	1C13		JP	CI01	YES
1D9	70D0	EXT	K	F0,13	ACKNOWLEDGE
1DA	2800		LF	OL,X'00'	CLEAR OL
1DB	1201		LM	X'01'	SET FOR PAGE 1
1DC	BC20		C	S1,T	GET ADDRESS
1DD	7080		K	F0,8	CLEAR
1DE	AC03	INT1	RN	S1	
1DF	B920		C	OU,T	GET UPPER ADDRESS
1E0	ACC3		RN	S1,I	

1E1	8823		AN	OL,T	GET LOWER ADDRESS AND RESET LINK
1E2	1488		JP	RJP	DO A RETURN JUMP
1E3	7140	INT0	K	I,4	GET INTERNAL STATUS
1E4	B802	TRP	CM	OL	CLEAR OL AND M
1E5	4101	INT3	TZ	I,X'01'	CONSOLE INTERRUPT OR TRAP
1E6	2C80		LF	S1,X'80'	YES
1E7	4102		TZ	I,X'02'	SPARE
1E8	2C82		LF	S1,X'82'	YES
1E9	4104		TZ	I,X'04'	REAL TIME CLOCK
1EA	2C00		LF	S1,X'00'	YES
1EB	4108		TZ	I,X'08'	MEMORY PROTECT
1EC	2C88		LF	S1,X'88'	YES
1ED	4110		TZ	I,X'10'	MEMORY PARITY
1EE	2C8A		LF	S1,X'8A'	YES
1EF	4120		TZ	I,X'20'	MEMORY BOUNDARY
1F0	2C8C		LF	S1,X'8C'	YES
1F1	4180		TZ	I,X'80'	POWER FAIL
1F2	1C03		JP	PWRF	YES
1F3	4140		TZ	I,X'40'	CONSOLE HALT
1F4	152B		JP	HLT1	YES
1F5	4C80		TZ	S1,X'80'	REAL TIME CLOCK
1F6	15DE		JP	INT1	NO
1F7	1C06		JP	INT4	
1F8	7140	INT2	K	I,4	GET INTERNAL STATUS
1F9	5180		TN	I,X'80'	POWER RESTART
1FA	15E4		JP	TRP	NO
1FB	1C10		JP	INT5	

\*  
\* INDIRECT POINTERS

1FC	1C38	PTR4	JP	C102	INDIRECT FROM C10 OR I0 TO C102
1FD	1C7E	PTR1	JP	MUL3	INDIRECT FROM C10 TO MULTIPLY
1FE	1C9B	PTR2	JP	DIV3	INDIRECT FROM C10 TO DIVIDE

\*  
ORG 512 BOARD 3

\* SECONDARY OP CODE TABLE

200	1780	SP.	LS	X'80'	SPECIAL (ERROR HALT)
201	1C62	MUL.	JP	MUL	MULTIPLY/DIVIDE
202	1C40	CPA.	JP	CPA	COMPARE

\* INTERRUPT OPTIONS (PWFL/RESTART AND RTC)

203	3F80	PWRF	AF	OV,X'80'	SET FLAG FOR POWER FAIL
204	2C8E		LF	S1,X'8E'	
205	15DE		JP	INT1	
206	2C84	INT4	LF	S1,X'84'	SET COUNTER ADDRESS
207	ACE3		RN	S1,I,H	GET LOWER HALF
208	8879		AT*	OL,I,T,C	ADD 1 AND SET COND CODE
209	A030		W	F0,H	PUT BACK
20A	AC6B		RN*	S1,D,H	GET UPPER HALF
20B	B0B1		CT	F0,L,T,C	ADD CARRY AND SET COND CODE
20C	ACF0		W	S1,I,H	PUT BACK
20D	4004		TZ	F0,X'04'	COUNTER ZERO
20E	15DE		JP	INT1	YES, GO TO SERVICE ROUTINE
20F	1C38		JP	C102	NO
210	2800	INT5	LF	OL,X'00'	CLEAR OL
211	2C90		LF	S1,X'90'	SET ADDRESS
212	15DE		JP	INT1	

\* CONCURRENT INPUT-OUTPUT

213	2CFC	CJ01	LF	S1,PTR4	INDIRECT RETURN
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214	70D0	C10	K	F0,13	ACKNOWLEDGE REQUEST
215	1000		L	X'00'	NOP
216	1200		LM	X'00'	SET FOR PAGE ZERO
217	B120		C	I,T	GET ADDRESS
218	7080		K	F0,8	CLEAR
219	F150		H	I,I,C	ADJUST AND REMOVE I/O FLAG
21A	A103		RN	I	
21B	BE20		C	S3,T	GET CURRENT LOWER
21C	A14B		RN*	I,D	
21D	B022		CM	F0,T	GET CURRENT UPPER
21E	5001		TN	F0,X'01'	INPUT
21F	1C3B		JP	C104	YES
220	AE03		RN	S3	
221	B020		C	F0,T	WAIT FOR DATA
222	70A0		K	F0,10	OUTPUT
223	1C24		JP	C103	DELAY
224	8E40	C103	I	S3	ADJUST CURRENT LOWER
225	7080		K	F0,8	CLEAR
226	1200		LM	X'00'	SET FOR PAGE ZERO
227	A16B		RN*	I,D,H	GET CURRENT UPPER
228	B0A1		CT	F0,L,T	ADJUST
229	A1F0		W	I,I,H	PUT BACK
22A	A1CB		RN*	I,I	GET ENDING LOWER
22B	9E38		S*	S3,T,C	COMPARE LOW BYTES
22C	A153		WN	I,D	STORE CURRENT LOWER
22D	CE01		MT	S3	
22E	A14B		RN*	I,D	GET CURRENT UPPER
22F	BE20		C	S3,T	
230	A1C3		RN	I,I	GET ENDING UPPER
231	9EB0		S	S3,L,T,C	COMPARE HIGH BYTES
232	4006		TZ	F0,X'06'	RESULT < 0
233	15A1		JP	I04A	GET TO SECOND PAGE TO EXIT
234	F120		H	I,R	ADJUST DEVICE ADDRESS
235	F161		HT	I,I,R	PUT IN FUNCTION CODE
236	2109		LF	I,X'09'	OUTPUT FROM A COMMAND
237	158D		JP	FUN	DISCONNECT DEVICE
238	CA03	C102	MN	PL	GET CURRENT INSTRUCTION
239	AB02		RM	PU	
23A	140E		JP	RNI2	
23B	70E0	C104	K	F0,14	INPUT
23C	1000		L	X'00'	NOP
23D	AE13		WN	S3	STORE INPUT DATE
23E	B021		CT	F0,T	GET INPUT BYTE
23F	1C24		JP	C103	
*					
* COMPARE					
240	A902	CPA	RM	OU	GET AN OPERAND
241	5108		TN	I,X'08'	VARIABLE
242	1C45		JP	CP1	NO
243	5F01		TN	OV,X'01'	W= 0 OR 1
244	1C4A		JP	CP2	YES
245	BC20	CP1	C	S1,T	
246	8843		IN	OL	
247	A982		RM	OU,L	GET AN OPERAND
248	5108		TN	I,X'08'	
249	1C60		JP	CP7	
24A	5F02	CP2	TN	OV,X'02'	W < 2
24B	1C5E		JP	CP6	YES
24C	B020		C	S2,T	
24D	8843		IN	OL	

24E	A982		RM	OU,L	GET AN OPERAND
24F	BE20		C	S3,T	
250	8843		IN	OL	
251	A982		RM	OU,L	GET AN OPERAND
252	9638		S*	BL,T,C	COMPARE WITH BL
253	CL01		MT	S3	
254	97H8		S*	BU,L,T,C	COMPARE WITH BU
255	CD01		MT	S2	
256	9488		S*	AL,L,T,C	COMPARE WITH AL
257	5F01	CP3	TN	OV,X'01'	W= 0 OR 2
258	1C5B		JP	CP5	YES
259	CC01	CP4	MT	S1	
25A	95B8		S*	AU,L,T,C	COMPARE WITH AU
25B	4002	CP5	TZ	FO,X'02'	RESULT NEGATIVE
25C	140C		JP	RN1	YES
25D	147B		JP	SET	NO, SET OVERFLOW
25E	9438	CP6	S*	AL,T,C	COMPARE WITH AL
25F	1C57		JP	CP3	
260	9438	CP7	S*	AL,T,C	COMPARE WITH AL
261	1C59		JP	CP4	
* * MULTIPLY					
262	884B	MUL	IN*	OL	
263	A98A		RM*	OU,L	GET MULTIPLIER OR DIVISOR
264	C803		MN	OL	
265	B820		C	OL,T	
266	A902		RM	OU	
267	2D10		LF	S2,X'10'	SET SHIFT COUNT
268	B920		C	OU,T	
269	4108		TZ	I,X'08'	MULTIPLY
26A	1C8E		JP	DIV	NO
26B	C401		MT	AL	MOVE A TO B
26C	B620		C	BL,T	
26D	C501		MT	AU	
26E	B720		C	BU,T	
26F	5580		TN	AU,X'80'	A NEGATIVE
270	1C79		JP	MUL1	NO
271	D660		X	BL,T,F	2'S COMPLEMENT
272	8640		I	BL	
273	D760		X	BU,T,F	MULTIPLIER AND
274	8780		A	BU,L	
275	D860		X	OL,T,F	MULTIPLICAND
276	8840		I	OL	
277	D960		X	OU,T,F	
278	8980		A	OU,L	
279	2CFD	MUL1	LF	S1, PTR1	INDIRECT RETURN
27A	2400		LF	AL,X'00'	CLEAR A
27B	2500		LF	AU,X'00'	
27C	4008	MUL2	TZ	FO,X'08'	CONCURRENT REQUEST
27D	1C14		JP	C10	YES
27E	5601	MUL3	TN	BL,X'01'	B REGISTER ODD
27F	1C85		JP	MUL4	NO
280	C801		MT	OL	
281	8420		A	AL,T	ADD PARTIAL PRODUCT
282	C901		MT	OU	
283	85B0		A	AU,L,T,C	
284	5001		TN	FO,X'01'	OVERFLOW SET
285	F508	MUL4	H*	AU	SET LINK WITH SIGN
286	F5A0		H	AU,L,R	SHIFT PRODUCT RIGHT 1
287	F4A0		H	AL,L,R	WITH SIGN EXTENDED

288	F7A0		H	BU,L,R	
289	F6A0		H	RL,L,R	
28A	9D50		D	S2,C	REDUCE SHIFT COUNT
28B	5004		TN	F0,X'04'	COUNTER ZERO
28C	1C7C		JP	MUL2	NO
28D	140C		JP	RNI	YES
*					
* DIVIDE					
28E	2D80	DIV	LF	S2,X'80'	FIRST TIME FLAG
28F	1680		LU	X'80'	SET FOR ADD
290	2CFE		LF	S1,PTR2	INDIRECT RETURN
291	C501		MT	AU	
292	D938		X*	OU,T,C	TEST SIGNS
293	5002		TN	F0,X'02'	SIGNS ALIKE
294	1690		LU	X'90'	YES, SET FOR SUB
295	F600	DIV1	H	BL	SHIFT LEFT 1
296	F780		H	BU,L	
297	F480		H	AL,L	
298	F580		H	AU,L	
299	4008	DIV2	TZ	F0,X'08'	CONCURRENT REQUEST
29A	1C14		JP	C10	YES
29B	C801	DIV3	MT	OL	PERFORM ARITHMETIC
29C	0420		E	AL,2	
29D	C901		MT	OU	
29E	05A0		E	AU,10	
29F	D539		XT*	AU,T,C	COMPARE SIGNS
2A0	5D0F		TN	S2,X'0F'	FIRST OR LAST TIME THROUGH
2A1	1C8F		JP	DIV9	YES
2A2	1680	DIV4	LU	X'80'	SET FOR ADD
2A3	4002		TZ	F0,X'02'	SIGNS ALIKE
2A4	1CA7		JP	DIV5	NO
2A5	1690		LU	X'90'	SET FOR SUB
2A6	8640		I	BL	DEVELOP A QUOTIENT BIT
2A7	9D50	DIV5	D	S2,C	REDUCE SHIFT COUNT
2A8	5004		TN	F0,X'04'	SHIFT COUNT ZERO
2A9	1C95		JP	DIV1	NO
2AA	C410	DIV6	M	AL,C	LOOK AT REMAINDER
2AB	C590		M	AU,L,C	
2AC	4004		TZ	F0,X'04'	REMAINDER ZERO
2AD	1C8A		JP	DIV7	YES
2AE	D738		X*	BU,T,C	COMPARE QUOTIENT SIGN
2AF	4002		TZ	F0,X'02'	REMAINDER SIGN CORRECT
2B0	1C99		JP	DIV2	NO, DO A CORRECTION CYCLE
2B1	C401		MT	AL	REMAINDER EQUAL TO DIVISOR
2B2	0838		E*	OL,3	
2B3	C501		MT	AU	
2B4	09B8		E*	OU,11	
2B5	4004		TZ	F0,X'04'	ARE THEY EQUAL
2B6	1C99		JP	DIV2	YES, DO A CORRECTION CYCLE
2B7	4780		TZ	BU,X'80'	QUOTIENT NEGATIVE
2B8	1C8C		JP	DIV8	YES, INCREMENT QUOTIENT
2B9	140C		JP	RNI	NO
2BA	5980	DIV7	TN	OU,X'80'	DIVISOR NEGATIVE
2BB	140C		JP	RNI	NO
2BC	8640	DIV8	I	BL	YES, INCREMENT QUOTIENT
2BD	8790		A	BU,L,C	
2BE	1479		JP	OCK	CHECK FOR OVERFLOW
2BF	5D80	DIV9	TN	S2,X'80'	FIRST TIME THROUGH
2C0	1CAA		JP	DIV6	NO
2C1	CD67		OS	S2,T,F	SET OR REMOVE FLAG BIT

2C2	DD20	X	S2,T	COMPARE WITH REMAINDER SIGN
2C3	5D80	TN	S2,X'80'	WAS A QUOTIENT BIT DEVELOPED
2C4	147B	JP	SET	YES, SET OVERFLOW AND EXIT
2C5	2D10	LF	S2,X'10'	SET SHIFT COUNT
2C6	1CA2	JP	DIV4	

```

*          THIS ROUTINE FOR USE FROM FRONT PANEL ONLY
*
*
*          SPECIAL ROS TO PERMIT READING AND WRITING
*          MEMORY EASILY FROM THE FRONT PANEL
*
*          SENSE SWITCH 4 OFF-  READ FROM MEMORY
*          SENSE SWITCH 4 ON-   WRITE INTO MEMORY
*
*          ENTRY POINT OF THIS ROUTINE IS 2F0
*
*          MEMORY ADDRESS-1 IS PLACED INTO FILES 8 AND 9
*          LOW ORDER 8 BITS OF ADDRESS ARE PLACED INTO FILE 8
*          HIGH ORDER 7 BITS OF ADDRESS ARE PLACED INTO FILE 9
*
*          AFTER A READ, THE LOCATION MAY BE MODIFIED
*          BEFORE EXAMINING THE NEXT LOCATION
*
*
*          ORG   X'2EF'
2EF   1780      LS   X'80'          WAIT FOR OPERATOR
2F0   7010      ESS  K   F0,1       EXAMINE SENSE SWITCHES
2F1   8843      IN   OL           SET MEMORY ADDRESS
2F2   8982      AM   OU,L
2F3   4002      IZ   F0,X'02'     SWITCH 4 ON
2F4   1CFC      JP   WRI          YES, GO STORE
2F5   A000      R    F0           READ
2F6   1780      LS   X'80'       WAIT FOR OPERATOR
2F7   B020      C    F0,T        DISPLAY MEMORY DATA
2F8   7010      K    F0,1       EXAMINE SWITCHES AGAIN
2F9   5002      IN   F0,X'02'   MODIFY CURRENT LOCATION
2FA   1CF1      JP   ESS+1      NO
2FB   1000      L    X'00'      NOP, RINH MAY NOT PRECEED NEXT COMMAI
2FC   7070      WRI  K   F0,7    ENABLE FRONT PANEL
2FD   11FF      LT   X'FF'      ENTER LOW ORDER 8 COMMAND SWITCHES
2FE   A010      W    F0         WRITE
2FF   1CEF      JP   ESS-1     GO CHECK SWITCHES
          END

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