Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PROJECT GRIND MEETING OF JUNE 26, 1953 (Third Day)

To: AN/FSQ-7 Planning Group

From: A. P. Kromer, R. P. Mayer

Date: June 29, 1953

Abstract: The magnetic drums were discussed at this meeting. There will be 6 fields per physical drum, and probably five physical drums per computer.

Members Present:

M.M. Astrahan	IBM		K.E. McVicar	MIT
W.L. Batchelor	IBM		J.A. O'Brien	MIT
R.L. Best	MIT		K.H. Olsen	MIT
J.M. Coombs	IBM		E.S. Rich	MIT
D.J. Crawford	IBM		H.K. Rising	MIT
N.P. Edwards	IBM		H.D. Ross	IBM
R.R. Everett	MIT		N.H. Taylor	MIT
E.H. Goldman	IBM		D. Thompson	IBM
J.F. Jacobs	MIT		R.L. Walquist	MIT
R.P. Mayer	MIT			

It was agreed that there should be 6 fields per physical drum, with 32 data tracks per field plus 2 status tracks per field (except in some cases), with probably 2 heads per track except for the auxiliary memory fields.

There will be 62 spots per circumferential inch, 20 tracks per axial inch (0.050 inch spacing), and the tracks will be 0.020 inches wide. There will be 204 tracks per physical drum (including timing), and space for 408 heads. There will be 2,048 spots per revolution, using an "open" timing track (not quite filling the circumference).

A study of the use of drum fields must be made before deciding on the number of fields and spares required. It has been suggested that 5 physical drums may be desirable, providing eight spare fields.

The drum must work with spot spacing of 12 to 8 microseconds simply by changing speed of rotation (i.e. pulley).

Write circuits will probably use a 5:1 transformer. The base-line shift in the transformer appears to cause no trouble, but an investigation must be made of the minimum write current possible before a change in reading is noticed. The write circuits must be protected against any combination of power failures.

It has not been decided whether the drum background ("0") should be saturated or not. Saturation seems preferable at the moment. The recording medium will be plated on the drum.

For reading, an investigation should be made of the various kinds of differentiating systems as well as the straight amplitude system now proposed.

Field switching must also be investigated. For reading, the field-switch recovery time need not be faster than 100 microseconds. Read switches under study include cathode follower (at the head) and low or hi-level diode (before or after a pre-amp stage). Write switches to be studied include saturable core transformers.

Each register, of any field that the computer can write on, will contain a parity bit. This bit will be generated and checked in the M. Buf. Check circuits might also be provided in the output drum circuits.

The radar input drum was discussed in some detail, and the following decisions were made.

There will be 16 radar input lines per field (XD-1 will have two such fields). The 32 bits of a field will be used as follows: 4 bits for radar identification, 8 bits each for R and θ (these 20 bits arriving from the SDV counters), 6 bits for read time (these 6 bits originating near the drum and being written any time an R, θ is written), leaving 6 bits for future expansion.

Drum capacity is provided for maintaining high probability of storage of at least one full scan's worth of data.

Two status bits per 32-bit word will be used, and they are placed on the radar status track and the computer status track (titles are not official), depending on which element writes in the track. A "zero" in either track means the related pocket is "empty". These status tracks are explained in the following two paragraphs. "SDV equipment" means equipment more closely related to the SDV system than to the computer, and vice versa (titles are not official).

The SDV equipment reads the computer status track half a pocket before writing. If it is a "zero", the Radar Input Buffer Register (RIB Reg), and a "1" status in the radar status track, are written at writing time unless the RIB Reg is empty. If the RIB Reg is empty, or if a "1" status is read, the computer status is copied into the radar status track and no other writing is done. At read time, if the RIB Reg is empty or about to be emptied (because a "0" is read) then a "drum demand" pulse senses the SDV counters (see Project Grind, first day) and reads one of them to the RIB Reg, the new number arriving after the drum write time has emptied the RIB Reg.

The computer equipment reads the radar status track and related pocket half a pocket before writing. If the status is a "1" the word from the pocket is transferred into the main memory and a "0" is written in the computer status track at "write" time, unless the computer identification request doesn't match the pocket ID digits or unless this field is not selected and running. If the identification does not match, or if the field is not selected, or if a "0" status is read, the radar status is copied into the computer status track. A counter counts timing marks, and disconnects the system when one drum revolution has been completed (unless a previous disconnect has occurred).

Perhaps the computer (via the output system) should be able to inject SDV signals into any SDV line for checking purposes.

The possibility of eliminating the RIB Reg should be investigated. (In the "Building A planned installation" the drum may be 200 feet from the SDV counters).

A drum buffer register (between the drum and IO Reg) will not be included unless it seems necessary (the parity check scheme mentioned above might require it).

The manual input drum (cards, tape, switches, special phone lines) will be just like the radar input drum unless there are very good reasons for not doing so.

Signed A. P. Kromer
A. P. Kromer

R. P. Mayer
R. P. Mayer

APK/RPM:jrt