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SUBJECT: DIGITAL-DATA RECEIVER AND GAP FILLER INPUT RECEIVER

To: Those Listed

From: E. B. Glover

Date: April 1, 1955

Approved: R. L. Best
R. L. Best

Abstract: A phone-line output in the form of a modulated wave composed of three different types of information is amplified, detected, and separated into channels. The output from each channel is in the form of a 0.25-μsec pulse for each information bit in that particular channel. Eight test points in the circuit show all important phases of operation. Seven marginal check lines provide a method of checking circuit deterioration.

I. Purpose

The digital-data receiver (DDR) and gap filler input receiver (GFIR) are essentially demodulators. They take a modulated wave from a phone line made up of three different types of information, separate it according to type, and convert it into pulses.

II. Circuit Operation

The DDR and GFIR are identical in design with one exception; the bit rate of the GFIR is 1600 bits per second, whereas the DDR has a bit rate of 1300 bits per second. In the timing circuit of both units is a high-Q filter tuned to the frequency of the basic bit rate. Consequently, in the high-Q filter of the DDR is a capacitor (C24, Fig. 12) not present in the GFIR, which changes the band-pass from 1600 cps to 1300 cps. This capacitor is located physically on the back panel.

A. In General

The DDR can be divided into four basic parts (Fig. 1). The input signal, a modulated wave from a phone line, is made up of synchronization, data, and timing signals superimposed on a 1950-cps carrier. (A 2000-cps carrier is used for the GFIR.) The input synchronization signal ranges in amplitude from 0.1 to 0.22 volt. Amplitudes of the other two signals relative to the synchronization signal are shown in Fig. 2. The output of the signal-detector (SD) is a demodulated signal with a synchronization amplitude of approximately 30 volts. This output

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is at a d-c level proportional to the percentage of unmodulated carrier present in the input wave. Relative amplitudes of the other signals are shown in Fig. 3.

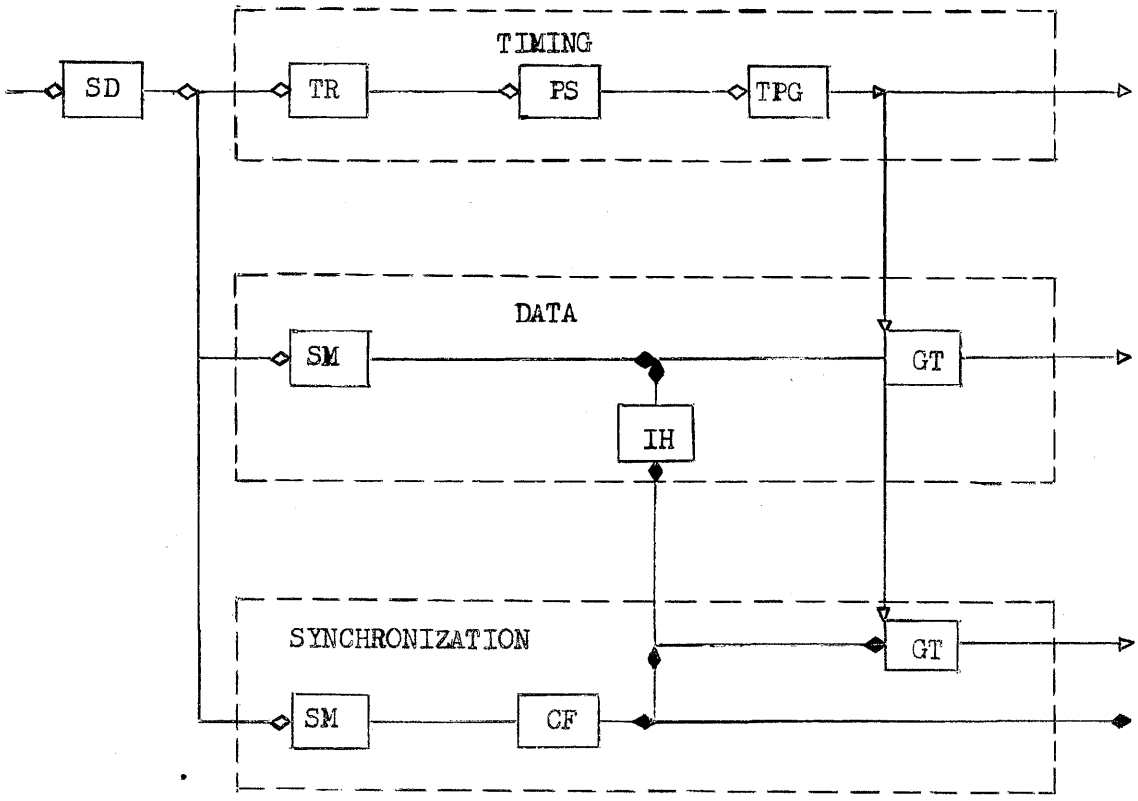

Fig. 1

Block Diagram

The output of the signal detector feeds three parallel circuits, of which the first is the timing circuit. In this circuit the timing portion of the demodulated wave is isolated by frequency discrimination, amplified, and converted into pulses. The output of this circuit is, therefore, in the form of positive 0.25-μsec pulses of about 30 volts amplitude (across 100 ohms), one for each bit of timing (i.e., 1300 pulses per second for the DDR, and 1600 pulses per second for the GFIR).

The second circuit fed by the signal-detector is the data circuit. Here the data portions of the signal are selected by amplitude discrimination. The output of this circuit is a positive 0.25-μsec pulse of about 30 volts for each bit of data.

The third of the parallel circuits is the synchronization circuit. As in the data circuit, the synchronization signals are isolated by amplitude discrimination; the output is in the form of a positive 0.25-μsec pulse of approximately 30 volts amplitude for each signal. This circuit has an additional output in the form a positive gate (of approximately 40 volts swing) clamped at the base to -30 volts.

B. In Detail

(See circuit schematic, Fig. 12, and the block diagram, Fig. 1.)

1. Signal detector

a. The modulated wave enters the signal detector through a line matching transformer, T1.

b. The transformer output goes through a low-pass filter which has a drop of 3db at 3200 cps and removes high frequency pickup. (The signal at this point is shown in Fig. 2.)

c. The output of the filter is fed to the two-stage automatic gain controlled (AGC) amplifier V1 and V2.

d. The amplified signal goes to the triode amplifier V3A and is coupled through transformer T2 to the full wave rectifier V4.

e. The output of the rectifier is passed to a cathode-follower, V3B, with a low-pass filter as its load. This filter has a drop of 3db at 1000 cps and, therefore, removes the carrier from the signal. The signal at this point (test point 3) is the output signal of the signal detector (Fig. 3).

f. The output signal is fed through a differentiator (condenser C14 and resistor R21) to an amplifier, V5A.

g. From the amplifier the signal feeds a peak detector, V5B. The bias of the peak detector is set by the resistors R22 and R23 to a value that allows only the highest pulse, synchronization, to pass through.

h. These peaks are smoothed by the filter consisting of condensers C16, C17, and C49 and resistors R24 and R25.

i. This smoothed d-c voltage, the AGC voltage, is negative with respect to the -150 volt line and is fed back to the grids of amplifiers V1 and V2, giving them a negative bias proportional to the synchronization amplitude at the output of the amplifier detector.

j. When the DDR is first turned on, there is no AGC voltage present. Lack of this voltage means that the gain of the amplifier detector is at its maximum. Consequently, if the input signal is large enough, the excessive amplification can cause the detected signal to have a constant amplitude (synchronization, data, and timing all the same size). When this signal is fed through the differentiator (capacitor C14 and resistor R21) only one pulse is passed to the AGC peak detector V5B. Since this pulse is not enough to appreciably affect the gain of the amplifiers, no other pulses are passed; thus, the AGC circuit is blocked and the amplifier gain remains constant. Resistors R12, R13, and R14 were added to prevent this blocking. The signal that feeds the rectifier V4 developes a negative bias (with respect to the

-150 volt line) across resistor R12. This bias is passed through resistors R13 and R14 to the AGC line and gradually brings the gain of the amplifier down until the AGC circuits start to function.

Fig. 13 plots the variation of the synchronization amplitude at test point 3 against the synchronization amplitude at test point 1. The curve demonstrates the effectiveness of the AGC voltage. Within the limits of the input signal (1.0 to 2.2 volts at test point 1) the amplitude at test point 3 does not vary more than ±1.5 volts.

Note that a restriction on the input signal of the signal-detector forbids a data signal to occur in the timing boxes immediately before and after the synchronization signal. The former restriction is necessary because the signal-detector output is differentiated before entering the AGC circuits. If a data signal were present immediately prior to the synchronization signal, a decrease in synchronization amplitude would result after the differentiation. This, of course, might produce an AGC voltage dependent on data signals as well as synchronization signals. The latter restriction is due to a slight overshoot in the signal-detector output which occurs immediately after the synchronization signal. Amplitude of a data signal (immediately following the synchronization signal) might be so decreased by the overshoot as to be undetected.

2. Timing

a. Timing Recovery Circuit (TR)

(1) The output of the signal-detector, differentiated to minimize the effect of synchronization and data signals, goes to the first amplifier (V6A) of the timing recovery circuit.

(2) The amplified signal, full-wave rectified by diodes CR5, CR6, CR7, and CR8 to double its frequency, is passed through transformer T3 to the high-Q filter (capacitors C22, C23, and C24 and inductor L4). Capacitor C22 is adjustable for fine tuning.

b. Phase Shifter (PS)

The output from the filter is fed through a cathode follower (V6B) to the phase shifting network (switch S1, transformer T4, and an RC network, R35 and C27). The switch gives a phase shift of 180°; the RC network connected to the center tap of the transformer gives a variable phase shift of approximately 167°.

c. Timing Pulse Generator (TPG)

(1) Over driven amplifiers V7A, V7B, and V8A convert the sine wave to a fast rise time square wave. The amplifiers are coupled together by RC networks designed to aid in decreasing the rise time.

(2) The signal from V8A is differentiated and goes to the puller tube V8B.

(3) The puller tube triggers the blocking oscillator V9, producing the output of the timing circuit described in Sec. II A.

3. Data and Synchronization

The output of the signal detector also goes to the data and synchronization circuits. The data circuit consists of a Schmitt slicer circuit (SM), V10A and V10B; an inhibitor (IH), V11A; and a standard gate tube, (GT) V12. The plate of V10A is connected through its plate resistor to a variable voltage divider made up of resistors R46, R47, and R48. The divider sets the grid bias of the normally conducting tube V10B and thus sets the tripping level of the slicer. A positive signal on the grid of V10A with enough amplitude to trip the slicer causes V10B to cut off. V10B stays off until the signal on the grid of V10A drops below the tripping level. Under normal signal conditions, the output of the slicer taken at the plate of V10B is a positive gate with a width of roughly 500 to 600 μsec. This gate is fed to the suppressor grid of the gate tube V12. The control grid of this tube is connected to the output of the timing circuit. If the timing pulse on the control grid occurs while the gate is on the suppressor grid, the gate tube will have an output pulse of 0.25 μsec width. The phase shifter in the timing circuit allows the timing pulse to be shifted with respect to the slicer gate, thereby, insuring their proper phase relationship. Since the circuit feeding the suppressor grid of the gate tube (V12) has a relatively high impedance, capacitor C32 has been added to supply the suppressor-grid current that is drawn when the timing pulse occurs. This action keeps the suppressor grid voltage from dropping during the pulse.

The synchronization circuit consists of a Schmitt slicer (SM), V13A and V13B; a cathode-follower (CF), V11B; and a standard gate tube (GT), V14. This slicer is the same as the slicer in the data circuit. Its output feeds the cathode-follower V11B. The output of the cathode-follower is the gate output of the synchronization circuit mentioned in Sec. II A. The cathode-follower also feeds two other circuits, the inhibitor V11A and the gate tube V14. Operation of the gate tube is the same as that of the gate tube in the data circuit. Operation of the inhibitor requires further explanation.

The potentiometer in the data slicer is set so that the tripping level is low enough for the slicer to trip on any data pulse that occurs (data pulses are one-half the amplitude of synchronization pulses). If the slicer is set in this manner, it will give an output for synchronization pulses as well as data pulses. To prevent this, the inhibitor tube V11A is included in the data circuit. The grid of this tube, normally biased below cut off by the voltage divider, resistors R70 and R71, is connected to the output of the cathode-follower in the synchronization circuit. When a synchronization pulse occurs, there is a positive gate output from both synchronization and data slicers. However, the synchronization output causes V11A to conduct which pulls

the plate of V10B back down and prevents the data output gate from occurring while the synchronization output is up. It will be noted that the data gate is not totally inhibited since the synchronization gate is not as wide as the data gate. This smaller width is, of course, due to the effect of the higher tripping level of the synchronization slicer and the relatively slow rise time of the input signal. (See Fig. 8.)

III. Test Points

The eight test points in the DDR and GFIR are to check on operation at strategic points in the circuit (see the circuit schematic, Fig. 12). Test point 1 (Fig. 2) is located at the input of the AGC amplifier in the signal detector. This point shows the input signal to the DDR stepped up by T1 and with high-frequency pickup removed. Test point 3 (Fig. 3), at the output of the signal detector, shows the demodulated signal. Test point 2 (Fig. 4), in the timing circuit at the output of the phase shifting network, shows the 1300-cps sine wave (1600 cps in the GFIR) generated from the input timing signal. Test point 2 is used while the tuning capacitor C22 of the high-Q filter is being adjusted, since a signal here will peak when the filter is tuned to the proper frequency.

To show the phase relationship between the timing circuit output and the outputs of the signal detector, the data slicer, and the synchronization slicer, test points 4, 6, and 8 combine the signals of the above pairs. Test point 4 (Fig. 6) combines the output of the signal detector with the input of the puller tube V8B. Test points 6 and 8 (Figs. 8 and 10) combine the output of the data slicer and the synchronization slicer, respectively, with the input of the puller tube V8B. Note that the input of the puller tube has a positive transient in phase with the timing circuit output. Although this positive pulse is clipped by grid conduction of V8B and does not show as well as the negative pulse at the test points, it is the correct pulse to use when setting the phase potentiometer. Test point 6 (Fig. 8) is advantageously used when phase potentiometer R35 is being set, since the phase relationship of the timing pulse, the data gate, and the inhibited synchronization gate can all be seen at once. Test point 5 (Fig. 7) combines the output signal of the signal detector with the signal at the plate of the normally-off tube (V10A) of the data slicer. This point is useful when the tripping level of the slicer is being set by potentiometer R47, since it shows exactly what amplitude of the input wave is tripping the slicer. Test point 7 (Fig. 9) shows the same relationship with the synchronization slicer as does test point 5 with the data slicer.

IV. Marginal Checking

Seven marginal check lines provide a method of detecting circuit deterioration. Curves illustrating the effectiveness of these lines are described below.

Fig. 14 plots marginal-check voltage +90 no. 1 against test point 3 and the AGC voltage. As the marginal-check voltage is lowered there is a very gradual decrease in over-all signal at test point 3. During this gradual decrease, the AGC voltage decreases linearly. When the marginal-check voltage reaches -110 volts (a 200 volt excursion), the AGC voltage reaches its limit, causing a sharp decrease in over-all signal at test point 3. Fig. 15 plots marginal-check voltage +90 no. 2 against the plate-supply voltages of tubes V3A, V3B, and V5A. As this marginal-check voltage is lowered, a gradual decrease in signal is observed at test point 3. As the voltage is further decreased, any data signals that are present start getting through the peak detector; a sharp decrease in signal amplitude results at test point 3. Failure, defined as this point of sharp decrease, occurs normally at a marginal-check voltage of about -30 volts (a 120 volt excursion). Figs. 16 through 21 plot the plate-supply voltage of each tube in the timing circuit against marginal-check voltage #250 no. 1. Failure in these curves is defined as the point where the blocking oscillator first fails to produce all timing pulses (normally when marginal-check voltage #250 no. 1 has a value of +95 volts). Fig. 22 plots the plate-supply voltage of tube V9, the blocking oscillator, against marginal-check voltage +90 no. 3. In this case, the marginal-check voltage has both upper and lower limits. Failure in the lower direction is defined as the point where the blocking oscillator first fails to produce all timing pulses (normally when marginal-check voltage #90 no. 3 has a value of #40 volts). Failure in the upper direction is defined as the point where the blocking oscillator goes into oscillation (normally at #185 volts). Fig. 23 plots the gate amplitude output of tubes V11A and V11B against marginal-check voltage +150. As the marginal-check voltage is lowered there is a gradual decrease in amplitude of synchronization gate output and of the inhibitor gate. This marginal-check voltage can normally be lowered to +70 volts with no appreciable effect on the outputs. No curve is given for marginal check #250 no. 2 since there are only a few points of interest of this voltage and each requires some explanation. The failure point depends entirely on the setting of the potentiometer R47 or R50. With the potentiometer set at the most difficult tripping level (counterclock wise) marginal-check #250 no. 2 can be lowered to roughly +175 volts before synchronization is picked up. (This is with a normal synchronization signal of about 30.5 volts at test point 3.) It can be lowered to +92 volts before data is picked up. Under normal conditions with potentiometers in both slicers set correctly for a normal signal input the marginal-check voltage can be lowered to about +200 volts before failure occurs. Here, failure for the synchronization slicer is defined as the point where the slicer trips on data pulses as well as synchronization pulses. In the case of the data slicer, failure is defined as the point where data pulses are inhibited as well as synchronization pulses. This failure point is, of course, the same for both slicers. No curve is given for the marginal-check #90 no. 4 since this marginal-check voltage is for both gate circuits. (General information on these circuits is found in the MRD report on gate tubes.) In this particular circuit, with normal signals, marginal-check #90 can be lowered to +25 volts before failure occurs. The marginal-check voltage can be raised to about +150 volts before failure occurs. Failure is defined for either direction as an output pulse falling below 20 volts.

Another curve should be mentioned although it is not a marginal-check curve. Fig. 24 shows the variation of the d-c level at the plate of the data slicer against the -150 end of the inhibitor grid bias divider. Two curves are presented; one with the data slicer "on" and the inhibitor tube biased "off", the other with both the data slicer and the inhibitor tube "on". These curves effectively illustrate the wide margins of the inhibitor tube. The upper curve is taken with a constant signal on the data slicer and with no signal on the inhibitor tube. The d-c level at the output of the data slicer should, therefore, be +10 volts under normal operating conditions. As the supply for the inhibitor grid bias divider approaches zero, the inhibitor tube finally conducts even though no signal is present. This constitutes a failure of the circuit. The lower curve (Fig. 24) is obtained with a constant signal on both the data slicer and the inhibitor tube. In this case the d-c level at the plate of the data slicer should be below -20 volts. As the supply for the inhibitor grid bias divider is lowered the inhibitor tube reaches a state of nonconduction, even though there is a signal present at its grid. This condition constitutes a failure in the opposite direction. The normal operating voltage of the inhibitor grid bias divider is an effective compromise between these two failures.

Signed: E. B. Glover
E. B. Glover

EBG/er

Attached:

Fig. 2, 3, & 4 - A-62277
Fig. 5, 6, 7, & 8 - A-62278
Fig. 9, 10, 11 - A-62279
Fig. 12 - D-75002-2
Fig. 13 & 14 - B-61832
Fig. 15 - B-61831
Fig. 16 & 17 - B-61828
Fig. 18 & 19 - B-61829
Fig. 20 & 21 - B-61830
Fig. 22 & 23 - B-61847
Fig. 24 - A-61859

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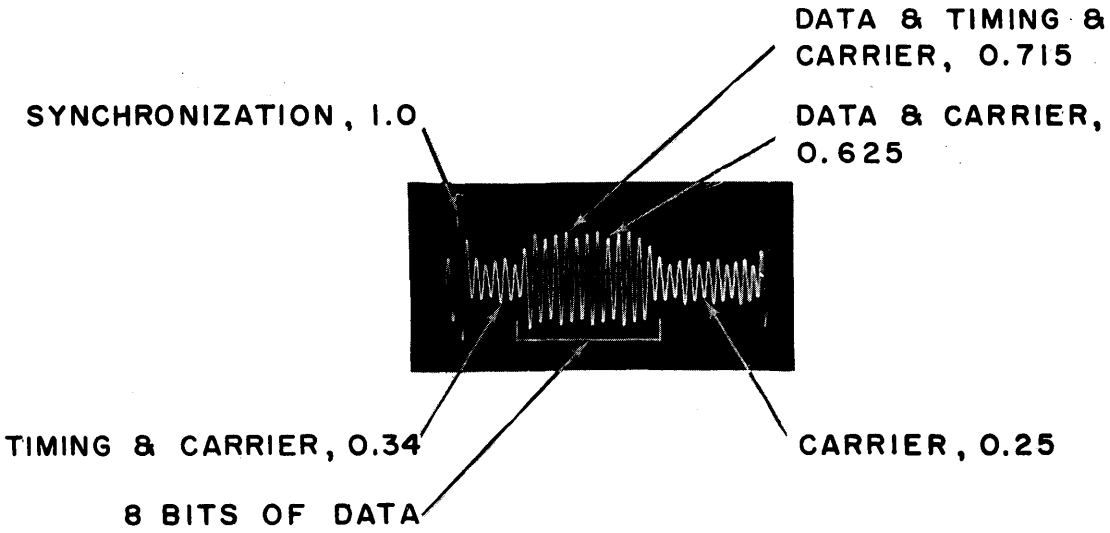


FIG. 2
TEST POINT 1

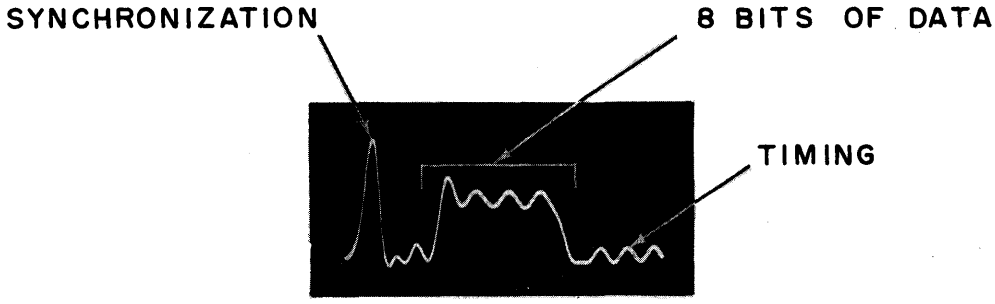


FIG. 3
TEST POINT 3

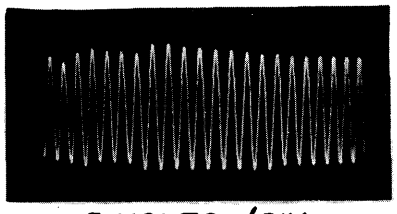
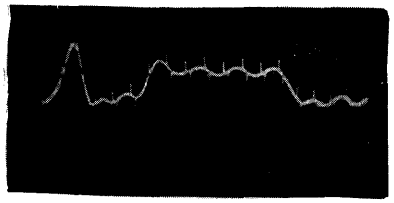


FIG. 4
TEST POINT 2

A-62277

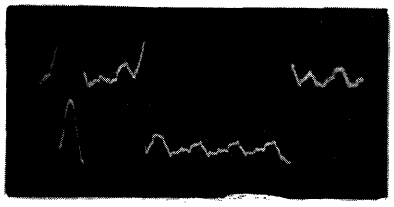
(OUTPUT TERMINATED WITH 100 Ω)
8 VOLTS / DIV.
0.1 μ SEC. / DIV.

FIG. 5
TIMING OUTPUT



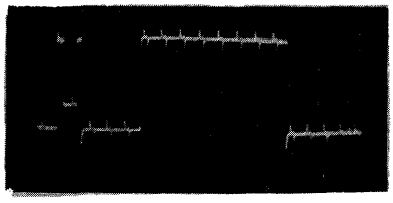
1.5 VOLTS / DIV.

FIG. 6
TEST POINT 4



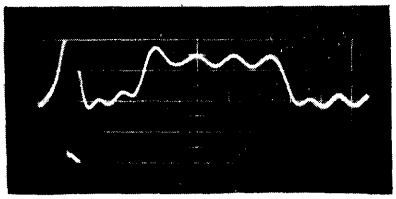
0.5 VOLTS / DIV.

FIG. 7
TEST POINT 5



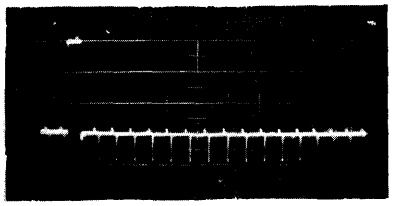
1.1 VOLTS / DIV.

FIG. 8
TEST POINT 6



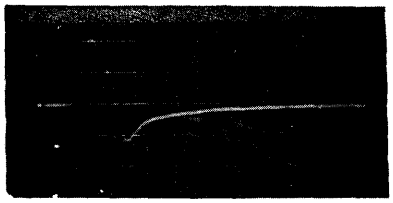
0.6 VOLTS / DIV.

FIG. 9
TEST POINT 7



2 VOLTS / DIV.

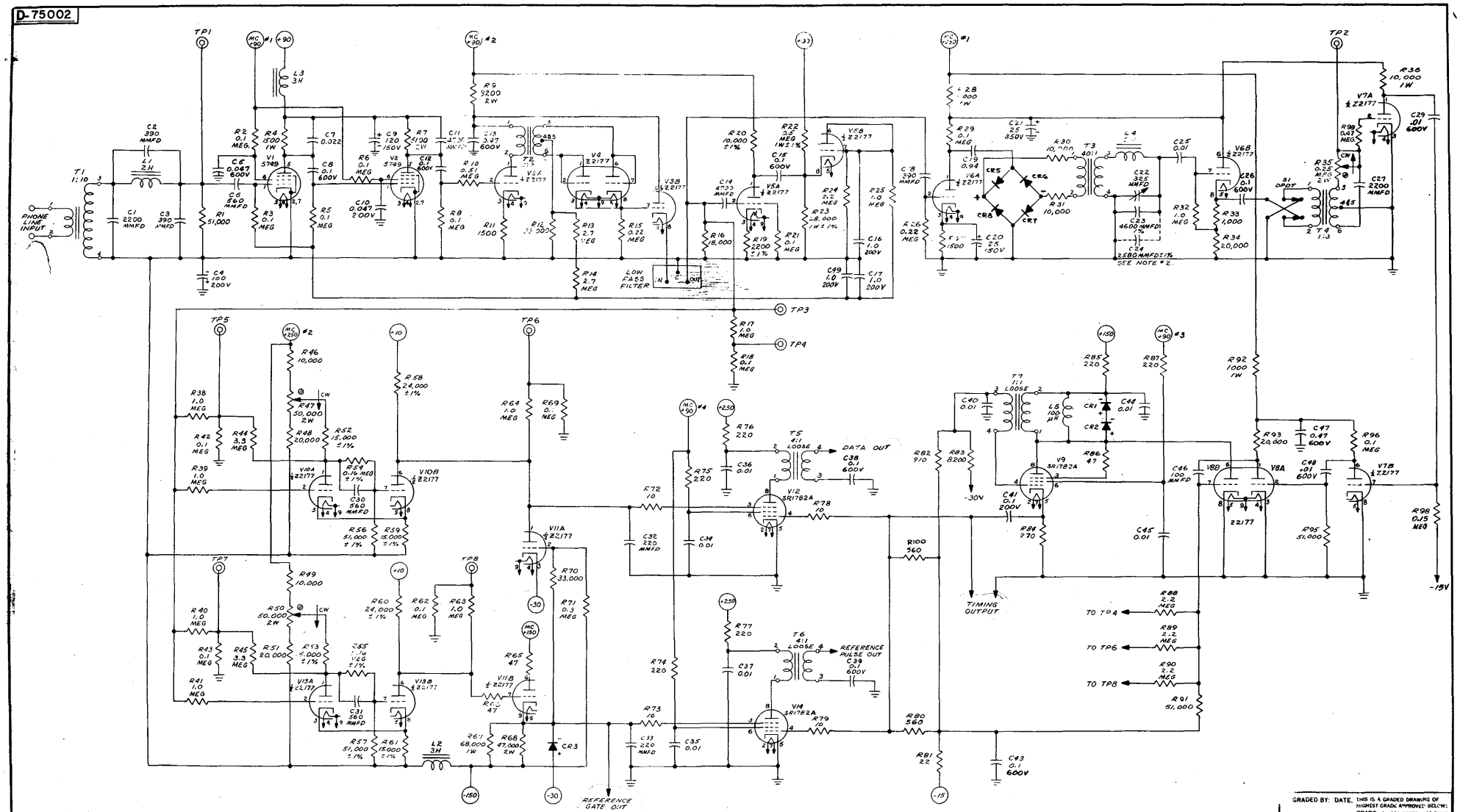
FIG. 10
TEST POINT 8



(OUTPUT TERMINATED WITH 100 Ω)
16 VOLTS / DIV.

FIG. 11
GATE TUBE OUTPUT

D-75002



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTORS ARE IN OHMS, ½ WATT ± 5%.
   - B. CAPACITORS ARE IN MICROFARADS.
   - C. ALL DIODES ARE TYPE Y.
2. 2580 MMFD ON BACK PANEL OF DIGITAL DATA RECEIVER ONLY.

FIG. 12

GRADED BY: DATE. THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. L. C. PROJECT NO.

CIRCUIT SCHEMATIC, GAP FILLER INPUT RECEIVER AND DIGITAL DATA RECEIVER AN/FSQ-7, XD-1

SCALE: — DR. JR 9-7-54
DWN. 9/13/54 CK. 9/17/54 APPD. 9/17/54

D-75002

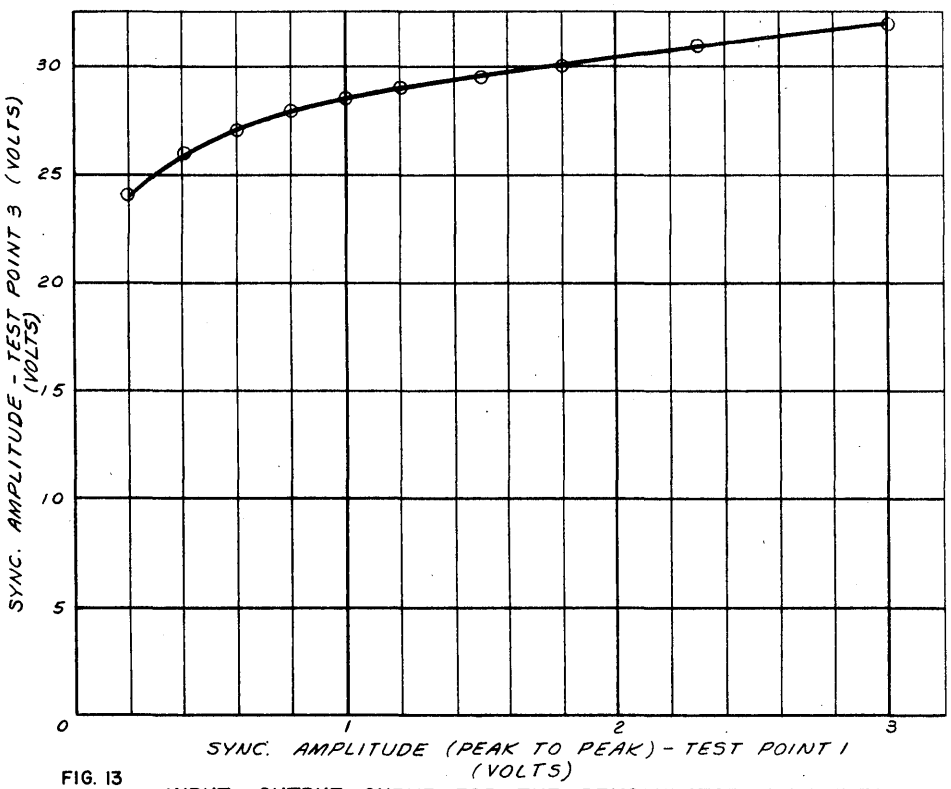


FIG. 13 INPUT - OUTPUT CURVE FOR THE DEMODULATOR AMPLIFIER

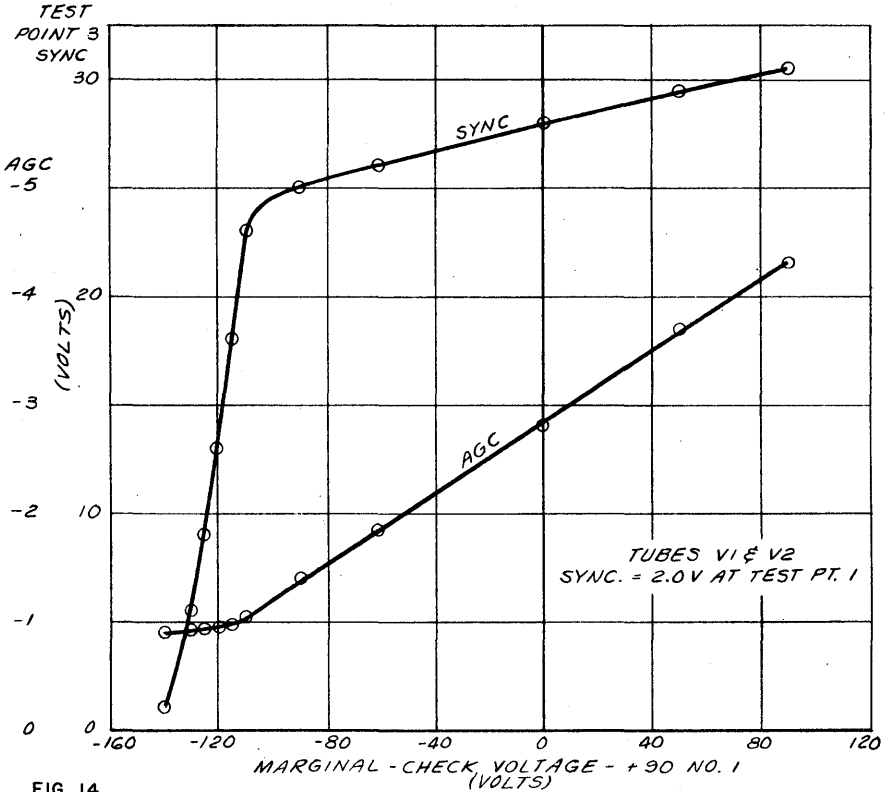
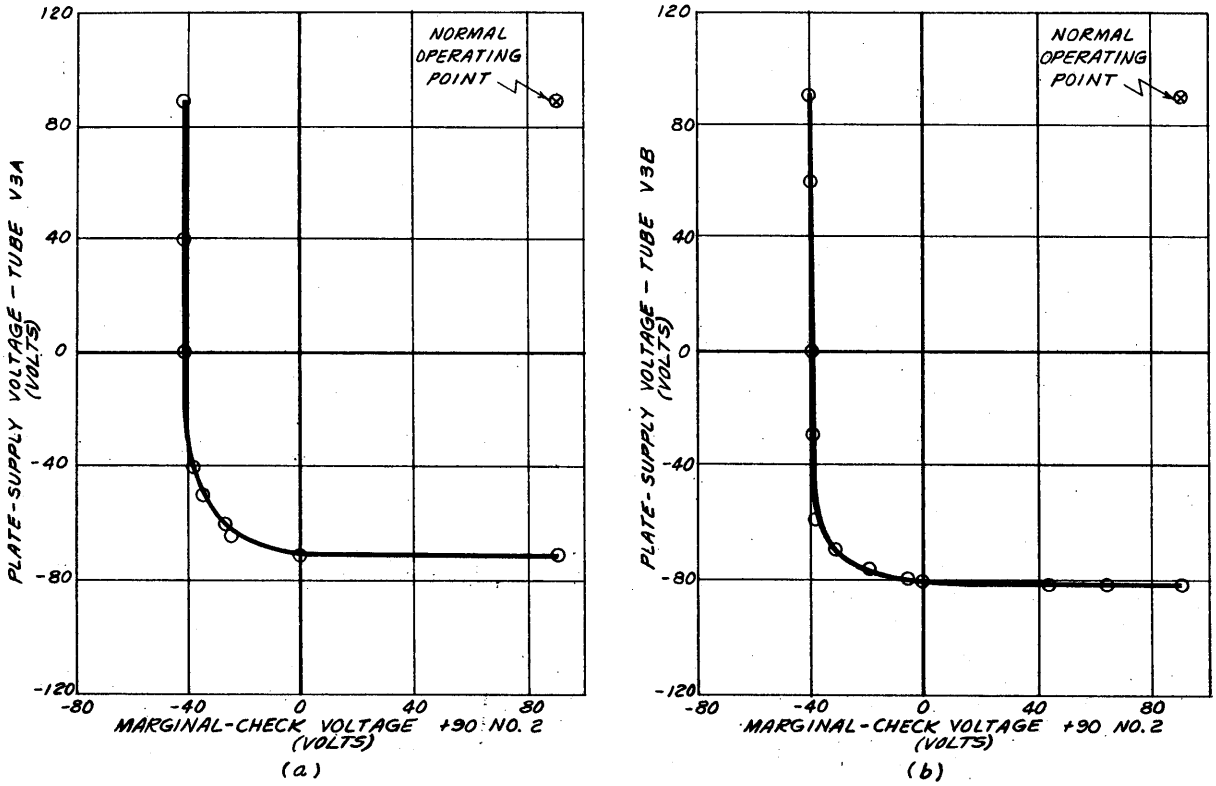


FIG. 14 VARIATION OF AGC AND SYNCHRONIZATION VOLTAGES AGAINST A MARGINAL - CHECK VOLTAGE

B-61832



B-61831

FIG. 15

VARIATION OF PLATE-SUPPLY VOLTAGE AGAINST A MARGINAL-CHECK VOLTAGE

TUBES V3A, V3B & V5A

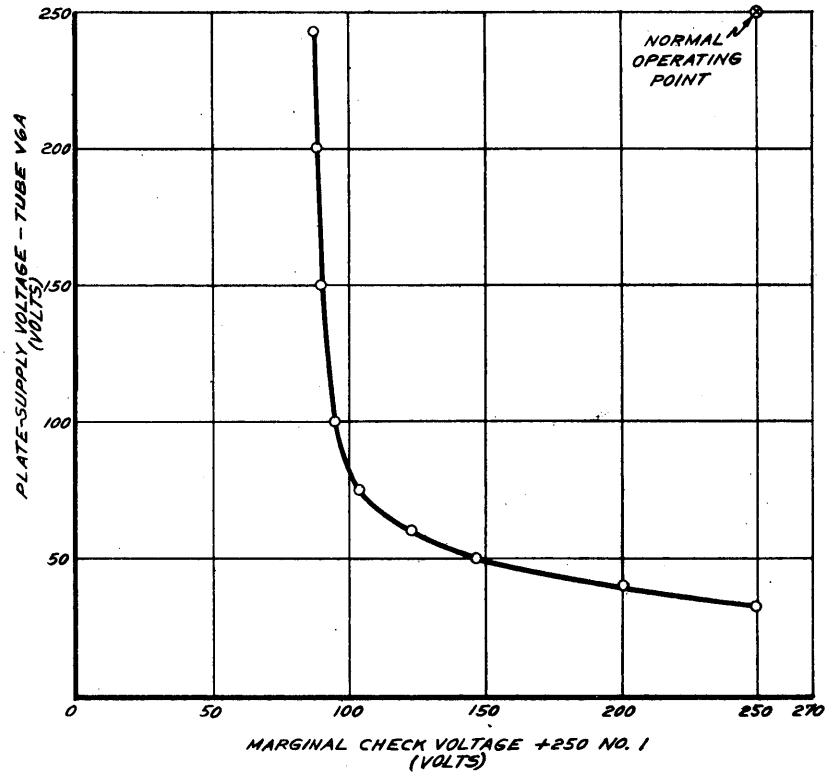


FIG. 16

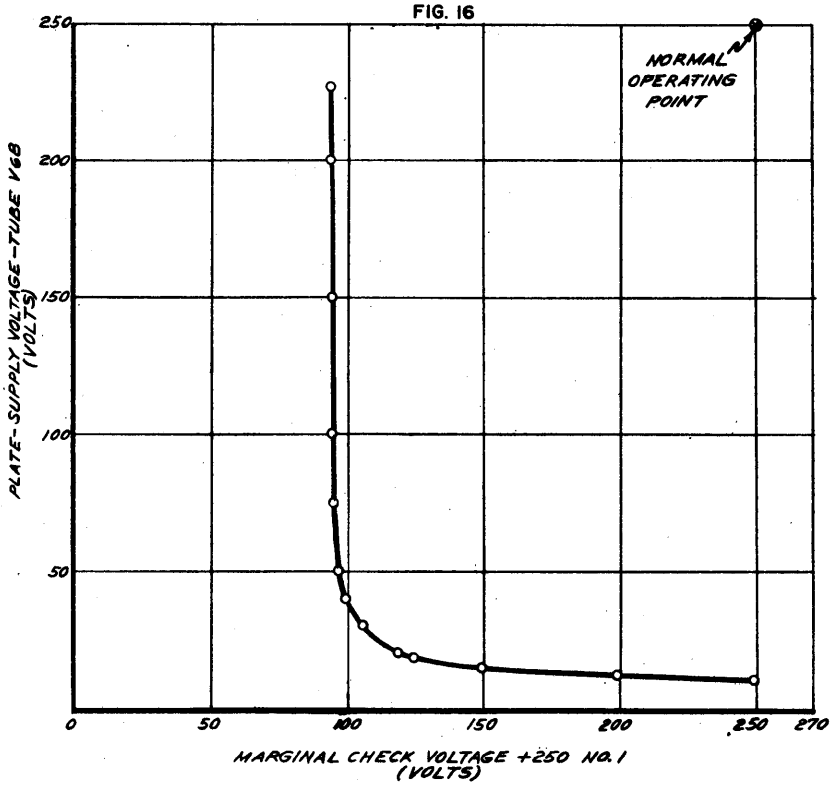


FIG. 17

VARIATION OF PLATE-SUPPLY VOLTAGE AGAINST A MARGINAL-CHECK VOLTAGE

TUBES V6A & V6B

B-61828

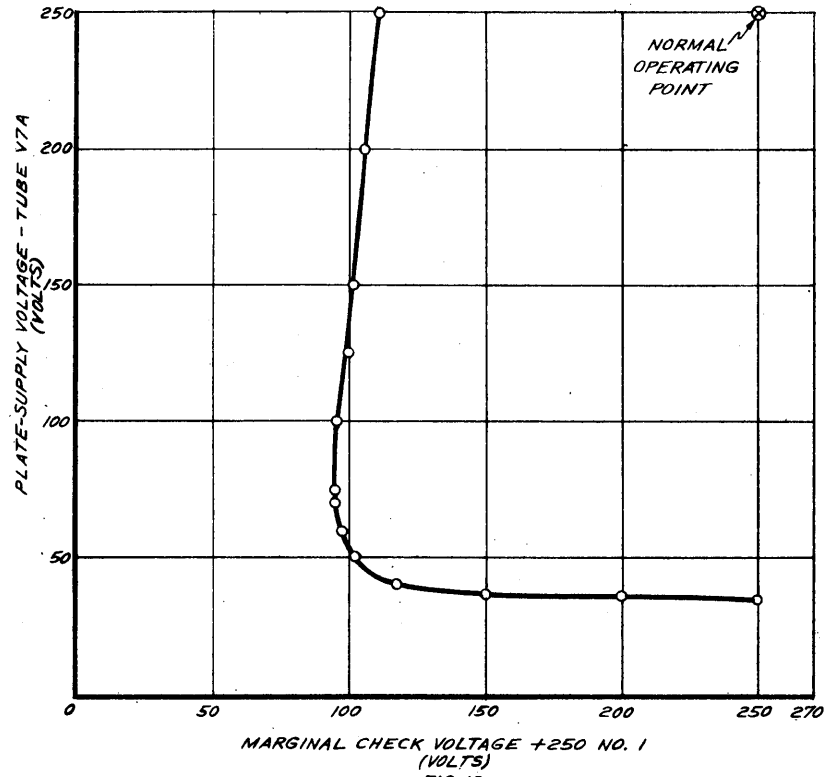


FIG. 18

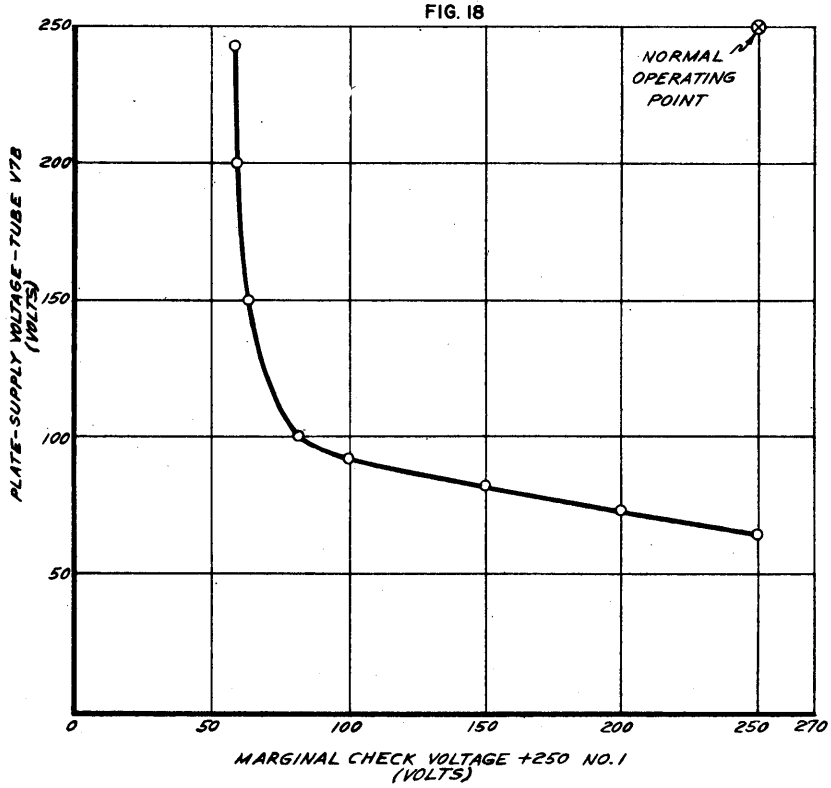


FIG. 19

VARIATION OF PLATE-SUPPLY VOLTAGE AGAINST A MARGINAL-CHECK VOLTAGE

TUBES V7A & V7B

B-61829

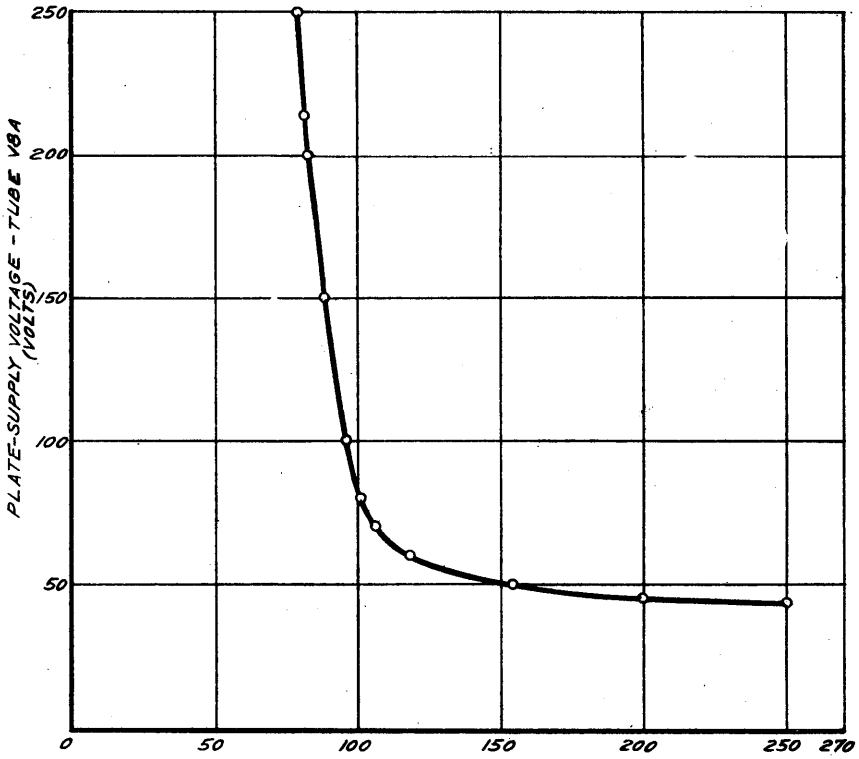


FIG. 20

VARIATION OF PLATE-SUPPLY VOLTAGE AGAINST A MARGINAL-CHECK VOLTAGE- TUBE V8A

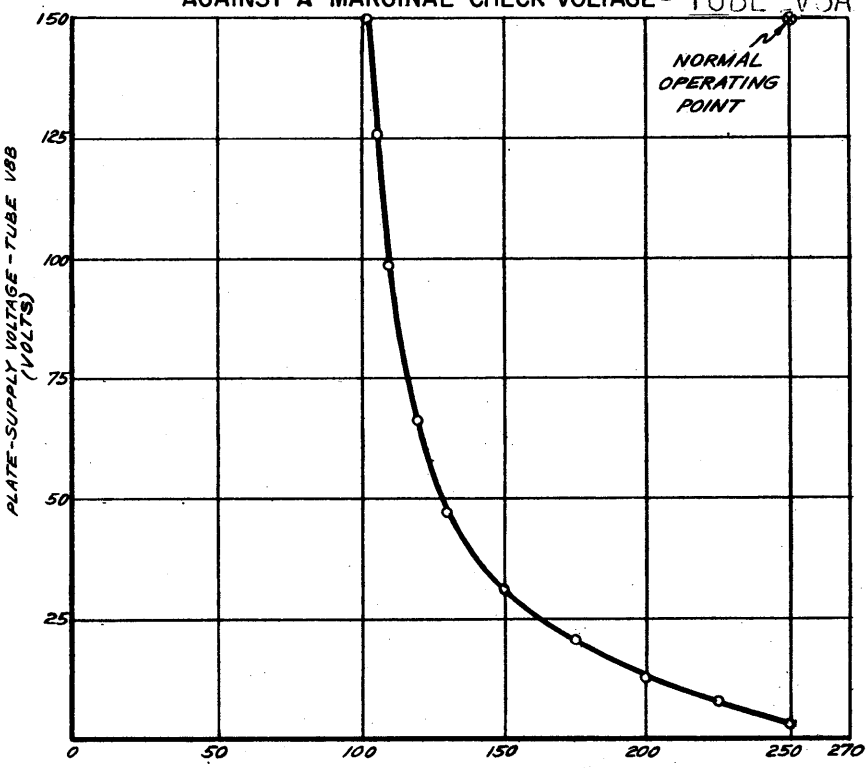


FIG. 21

VARIATION OF PLATE VOLTAGE AGAINST A MARGINAL-CHECK VOLTAGE TUBE V8B

B-61830

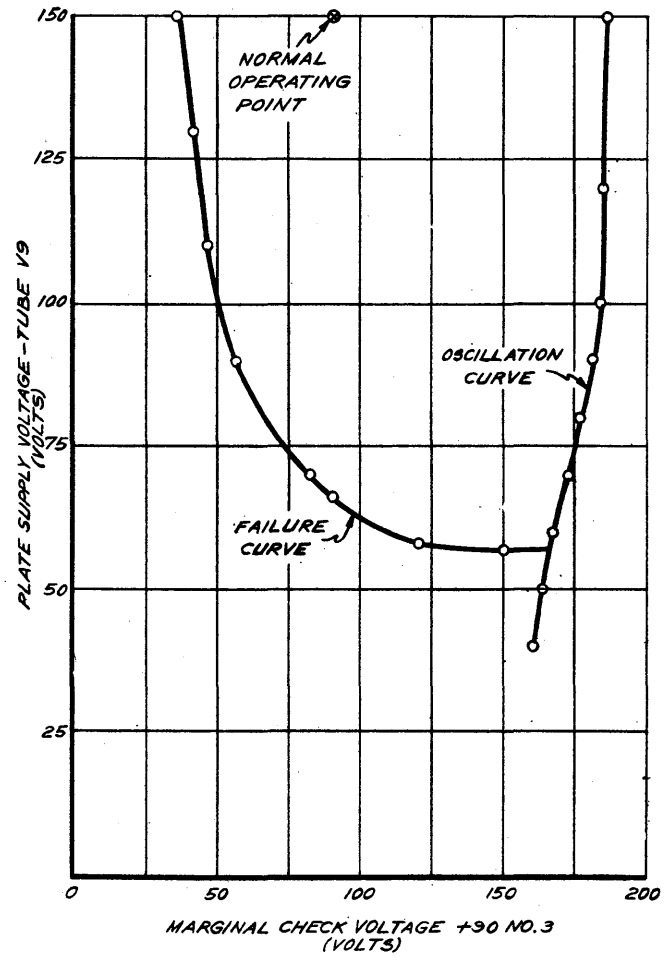


FIG. 22

VARIATION OF PLATE-SUPPLY VOLTAGE AGAINST A MARGINAL CHECK VOLTAGE

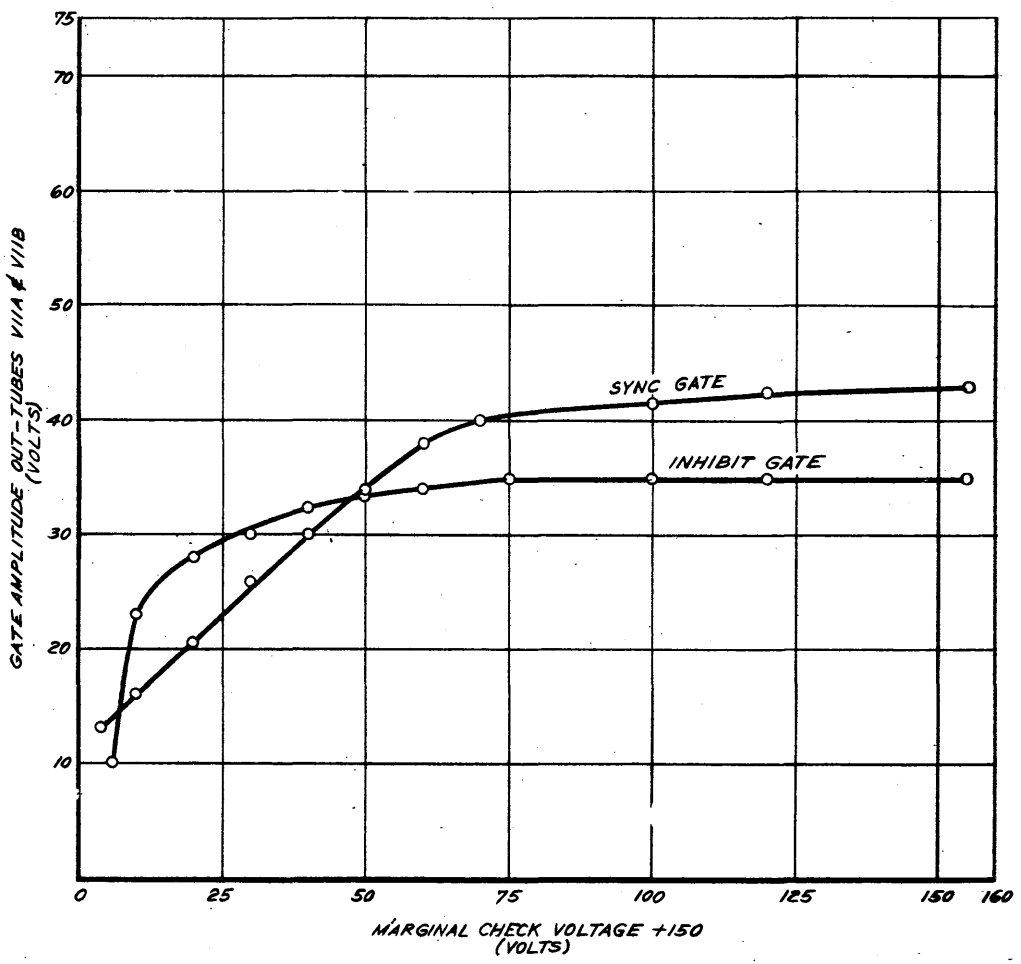


FIG. 23

VARIATION OF OUTPUT GATE AMPLITUDE AGAINST A MARGINAL-CHECK VOLTAGE

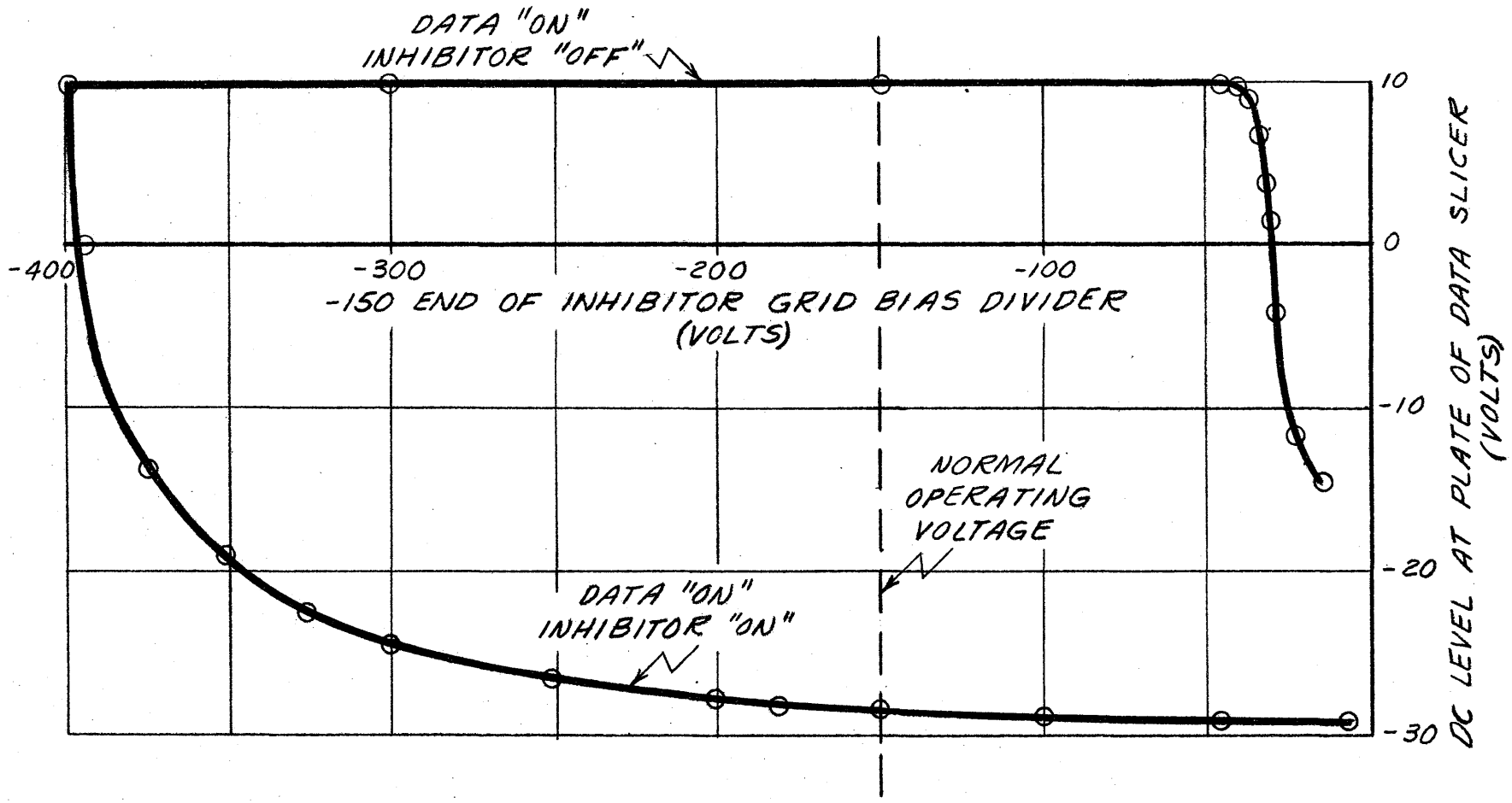


FIG. 24

VARIATION IN THE "DATA" DC LEVEL OUTPUT AGAINST EFFECTIVE GRID BIAS OF INHIBITOR (DATA "ON" — INHIBITOR "ON" AND "OFF")