

A DIGITAL ELECTRONIC CORRELATOR

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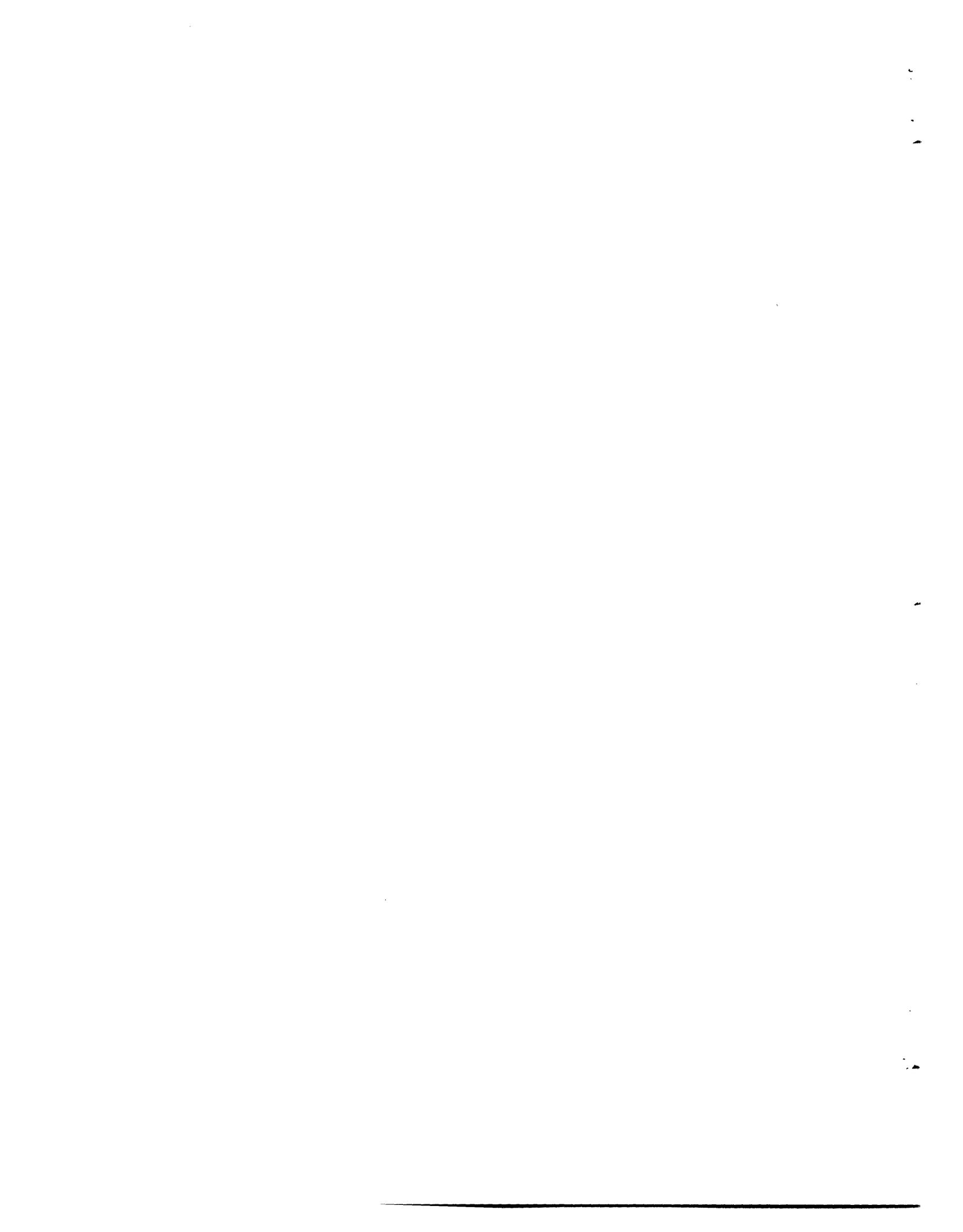
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A DIGITAL ELECTRONIC CORRELATOR

Henry E. Singleton

Abstract

The relation between correlation functions and the general theory of communication is presented; this relation leads to a technique for electronic computation of correlation functions and to the design of a machine for carrying out the computation. Because of the requirements of great accuracy and long storage the machine makes use of binary digital techniques for storage, multiplication and integration. Descriptions of the more unusual circuits in the machine are given, and complete circuit diagrams are included. A number of experimental results obtained by the machine are presented.



A DIGITAL ELECTRONIC CORRELATOR

The application of statistical methods to communication problems is still only a few years old, but already the power of the statistical approach is becoming generally appreciated (1-5). An adequate body of statistical data is not yet available, however, and this lack prevents the full strength of the statistical technique from being brought to bear on a large number of communication problems. The branch of statistical theory which is applicable here, and which, indeed, must be considerably extended if it is to be of greatest use, is the theory of random processes. The theory of random processes enters because communication equipment must operate for an ensemble of possible signals, none of which can be specified in advance; they are characterized by a set of probability distribution functions. The fundamental statistical parameters which are required for the solution of general communication problems are accordingly the set of functions which characterize the ensemble, namely, the probability distributions

$$P_n(y_1, t_1; y_2, t_2; \dots; y_n, t_n), \quad n = 1, 2, \dots$$

where $P_n dy_1 dy_2 \dots dy_n$ is the probability that a member of the ensemble will have values in the ranges $(y_1, y_1 + dy_1)$, $(y_2, y_2 + dy_2)$, \dots , $(y_n, y_n + dy_n)$ at times t_1, t_2, \dots, t_n . Since P_i can be found from P_j for $j > i$, it follows that the P_n describes the process in successively greater detail as n increases (6). In applications of the theory it is usual to assume that the probability distributions are invariant under a shift of the origin of time, i. e. that the process is stationary.

Although a knowledge of all the probability distributions P_n is required in order to treat more general communication problems, many problems can be handled through the use of the second probability distribution $P_2(y_1, t_1; y_2, t_2)$. Since for stationary ensembles the distribution P_2 depends not on the absolute values of t_1 and t_2 but on the difference $t_2 - t_1$, it is convenient to abbreviate $P_2(y_1, t_1; y_2, t_2)$ as $P(y_1, y_2; \tau)$ where $\tau = t_2 - t_1$. The experimental evaluation of $P(y_1, y_2; \tau)$ for even a single stationary ensemble is a lengthy task (7) because it requires the evaluation of P for each point in the three-dimensional space y_1, y_2, τ . It is therefore fortunate and of considerable engineering interest that a certain class of communication problems* can be treated in terms of the moment of the distribution P :

$$M(\tau) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} y_1 y_2 P(y_1, y_2; \tau) dy_1 dy_2 \quad (1)$$

The three-dimensional probability distribution undergoes a smoothing due to the process

*Notably the design of optimum linear systems, Refs. 1 and 2.

of integration, and the result is a one-dimensional rather than a three-dimensional function. Furthermore, the moment $M(\tau)$, which may be regarded as the average value of the product $y_1 y_2$ (for a specified τ), can be evaluated without recourse to the probability distribution P . In fact, if $f(t)$ is a member of the ensemble, the average of products of pairs of values of $f(t)$ which are separated by time τ is the correlation function

$$\phi(\tau) = \lim_{T \rightarrow \infty} \frac{1}{2T} \int_{-T}^T f(t) f(t + \tau) dt \quad (2)$$

For a stationary process it follows from the ergodic theorem that $M(\tau) = \phi(\tau)$.

Theory of Computation

Since, according to the results above only one member $f(t)$ of the ensemble is required to compute $\phi(\tau)$, a convenient approximate method of evaluating $\phi(\tau)$ experimentally is to average a large number of products of pairs of samples of $f(t)$:

$$\phi(\tau) = \frac{1}{N} \sum_{1}^N a_n b_n(\tau) \quad (3)$$

where N is a large number and a_n and b_n are samples of $f(t)$ which are separated by the interval τ .

Physically, the above discussion means that the computation may proceed as follows: A sample a_1 of the input time series is obtained and stored; after a time τ has elapsed, a sample b_1 is taken and stored; the two samples a_1 and b_1 are multiplied together; the product is stored, and the samples a_1 and b_1 are discarded. The sampling and multiplying process is carried out repetitively, and each time a product is obtained it is added to the cumulative sum of the products previously obtained. After N such products have been obtained, the sum is recorded and the device which stores the products is reset to zero. The sum recorded represents the value of $\phi(\tau)$ for the value of τ under consideration. Proceeding in this way, as many points on the correlation function as desired may be obtained. The procedure just described is used in the present machine. Although an average might be obtained in a shorter period of time by delaying the entire wave form, such a procedure would require the use of more complex equipment.

General Design Specifications

An earlier experimental correlator (8) at the Research Laboratory of Electronics demonstrated the feasibility of high-speed electronic computation of correlation functions. Results on this earlier correlator pointed out the need for great accuracy in the computing circuits and in the specification of the delay τ , as well as a need for a very large range of possible values of τ . Although the preliminary machine served an exceedingly useful purpose, it was limited in the range of delay available, and hence was unable to handle many of the problems susceptible to treatment by correlation functions. The

present research was initiated in order to provide the laboratory with a highly flexible, general-purpose correlator; one which would meet the requirements of the numerous applications which had been proposed, and would take advantage, in its design, of experience gained on the first correlator. The following general design specifications for the present machine were evolved:

1. Wideband input circuits (d-c to 12 Mc/sec).
2. Wide range of delays (0 sec to 0.1 sec).
3. Minimum increments in τ to be less than 0.1 μ sec.
4. Value of τ to be known to within 0.01 μ sec.
5. Machine to be completely automatic.
6. Accuracy and long-term stability to be as great as possible.

The requirement for great accuracy and stability, and especially for very long storage, strongly indicated the use of digital techniques. The binary system is therefore used for storing, multiplying and integrating. By this means, possible sources of error are limited to the sampling circuits and to the circuits for translating the samples into binary numbers. Errors from these sources are first minimized by careful selection and design of the circuits used. Remaining errors are further reduced by a special feedback drift-compensating circuit. Descriptions of the circuit techniques used are given below, and together with the general description of the machine, form the body of the report.

General Description

A functional block diagram of the correlator is shown in Fig. 1. This is a straightforward translation of Eq. 3 into functional components. To avoid using a separate number generator for each of the two channels, a selector gate is used to route the A and B boxcars (or samples) successively to a single number generator. If the inputs $f_1(t)$ and $f_2(t)$ are different, their crosscorrelation is obtained. If an autocorrelation function is required, the two inputs are connected together. The boxcar generators are so called because their outputs consist of wide flat-topped pulses developed from the original narrow samples. Typical wave forms at the numbered points on Fig. 1 are shown in Fig. 2. The value of τ is controlled by fixing the time interval between pulses 3 and 4. Operation of the computer is as follows. Boxcars 5 and 6 are obtained from signals 1 and 2 at the time of occurrence of timing pulses 3 and 4. The selector gate normally passes the larger of the two boxcars to the number generator, except during occurrence of gate 7 when boxcar 5 is passed, and during occurrence of gate 9 when boxcar 6 is passed. Gates 7 and 9 are also fed to the number generator, and during their occurrence the output of the selector gate is coded into binary form. The purpose of delaying pulse 4 to produce pulse 8 is to insure that gates 7 and 9 do not overlap for small or zero values of τ . Thus the number generator has time to code the first boxcar, gate the resulting binary digits into storage in the number register, and reset itself

before it receives the signal (gate 9) to code the second boxcar. After the A and B numbers are stored in the number register, they are multiplied together in the multiplier and added to the previously accumulated products in the integrator. When a predetermined number of products (of the order 10^5) have been accumulated, a number-stop gating pulse of approximately four seconds duration goes out on the number stop line from the timing equipment to the number generator, and stops the gating of the A numbers into storage. By this means the A number section of the register remains reset to zero. The output of the multiplier therefore becomes zero also, and the number accumulated in the integrator is recorded. This is the value of $\phi(\tau)$ for the particular value of τ being used. The integrator is then reset to zero, and the value of τ is changed in the timing equipment by changing the separation of the A and B timing pulses. The operations of recording $\phi(\tau)$, resetting the integrator, and changing τ are completed in about two seconds. When the number-stop gating pulse ends, the machine begins the computation of ϕ for the new value of τ .

Circuit Features

We now proceed to a somewhat more detailed discussion of those parts of the machine which are especially important in meeting the design specifications listed above.

Timing Equipment. Fig. 3 is a block diagram of the portion of the timing equipment which is used in obtaining the A and B timing pulses. These timing pulses must be accurately spaced, since it is their separation which defines τ . A one-megacycle crystal oscillator is used as a reference. The output of the oscillator drives a pulse generator which in turn feeds a cascade of bistable multivibrators. A square wave is taken from one of the latter stages in the cascade to govern the repetition rate at which A and B timing pulses are produced, and therefore the rate at which multiplications are carried out. This rate may be as great as approximately 1000 per second for small values of τ , but must be decreased as the value of τ increases. Normally the rate is set low enough to include the maximum value of τ used in any one correlation function, and is not changed throughout the computation. By means of the pulse generator, a pulse obtained from one edge of the square wave triggers the phantastrons, and the phantastrons trigger gate pulse generators whose outputs are set to have a duration equal to the steps in τ which are to be used. The gate pulse generators turn on the gates during the occurrence of one of a train of pulses obtained from an earlier stage in the divider cascade. This latter pulse train has a repetition period equal to the desired steps in τ . Numbered wave forms are shown in Fig. 4. The steps in τ which are available by this method range from $1 \mu\text{sec}$ to $2^{10} \mu\text{sec}$. Smaller steps in τ are obtainable by making use of the trailing edges of the phantastron outputs directly. By this means, increments in τ as low as $0.02 \mu\text{sec}$ can be obtained. The phantastron plate-catching voltage is under control of a stepping relay which produces 110 different voltages in succession. A particular value of τ corresponds to each position of the stepping relay, and the relay changes after each

value of $\phi(\tau)$ is recorded. The maximum range of τ is 110×2^{10} μ sec or about 0.1 sec.

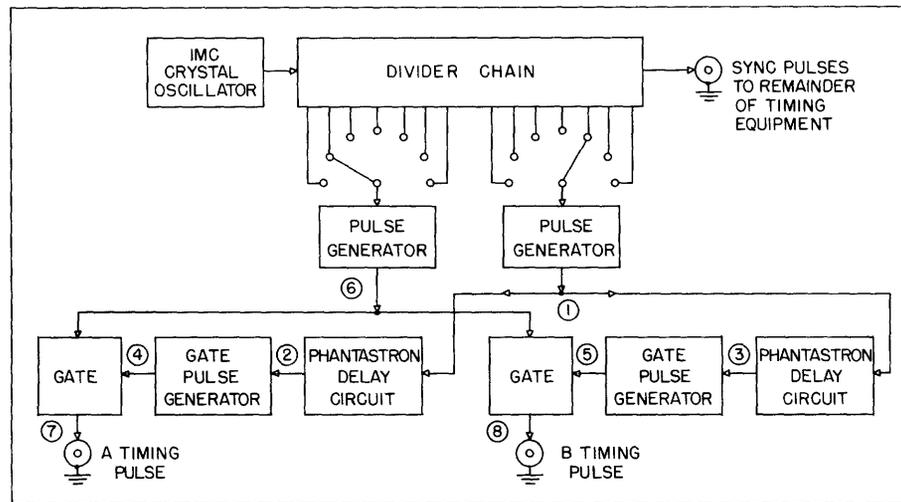


Fig. 3 Block diagram of timing equipment.

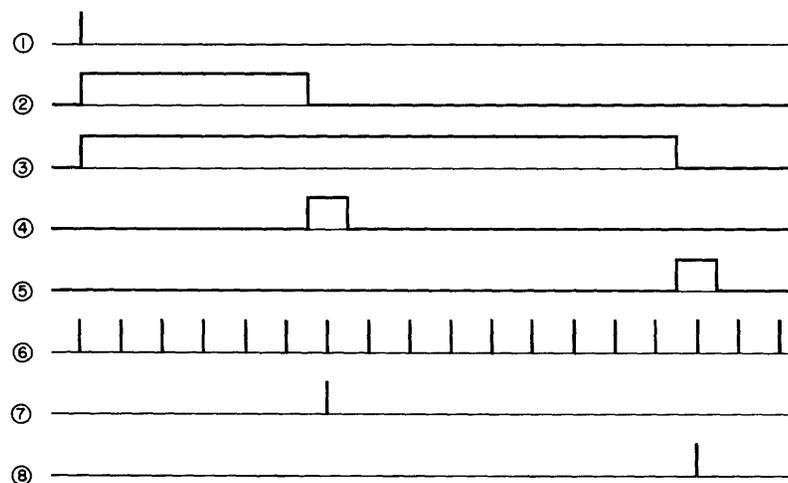


Fig. 4 Wave forms at numbered points of Fig. 3.

Sampling and Coding Circuits. In order to produce a binary digital representation of the amplitude of the input signal at the time of sampling, the corresponding boxcar is first converted to a pulse having a duration proportional to the boxcar amplitude. The duration-modulated pulse is then used to gate a train of timing pips to a binary counter. The counter is reset to zero prior to the occurrence of each duration-modulated pulse so that the condition of the counter at the end of the duration-modulated pulse is a binary representation of the boxcar amplitude (10). It is evident that the only important errors produced by the correlator must lie in these circuits; that is, in the boxcar generator and in the duration-modulated pulse generator. The duration-modulated pulse is obtained by intersecting the boxcar with a saw-tooth wave form, and marking the instant of

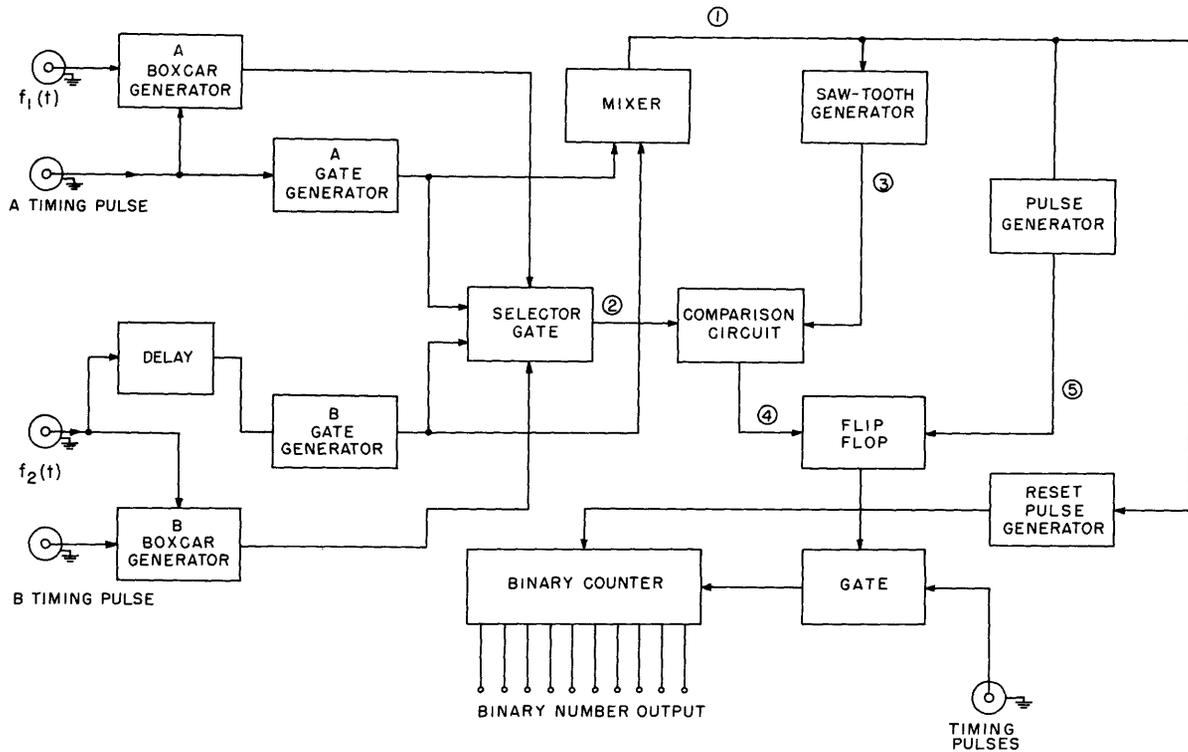


Fig. 5 Block diagram of number generator and associated circuits.

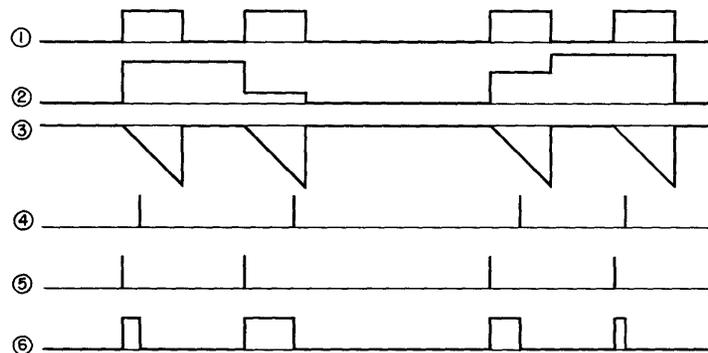


Fig. 6 Wave forms at numbered points of Fig. 5.

equality of the two voltages. Thus the critical portions of the duration-modulated pulse generator are the saw-tooth wave form generator and the comparison circuit used to indicate equality between the saw-tooth and the boxcar. The boxcar generators, saw-tooth generator, and comparison circuit are discussed next. A block diagram showing the interconnection of these circuits is given in Fig. 5. The operation indicated by the diagram can be followed with the aid of Fig. 6, which shows wave forms for numbered points on the diagram.

Boxcar Generator. A block diagram of one of the boxcar generators is shown in

Fig. 7. There are two of these circuits, one for each channel. The input timing pulse is reshaped for uniformity in a blocking pulse generator, which produces a very sharp sampling pulse a little less than $0.1 \mu\text{sec}$ in duration. The sampling pulse is applied to

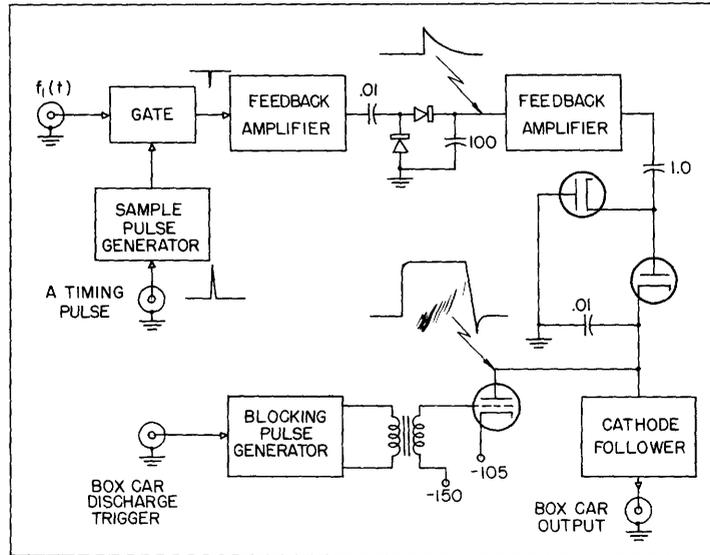


Fig. 7 Block diagram of boxcar generator.

the suppressor grid of a 6AS6 gate tube normally biased below plate current cut-off, and the input time series is applied to the control grid. The need for a very narrow sampling pulse and a wide, flat-topped output pulse imposes conflicting requirements on the boxcar generator. The wide output pulse is obtained by storing charge on a condenser. In some cases use is not made of the stored sample until about $600 \mu\text{sec}$ have passed. To prevent appreciable decay of the charge during this interval a large condenser ($0.01 \mu\text{f}$) is used. If we assume a leakage resistance of 40 megohms, for example, the discharge time constant is 400 millisecc, and this is satisfactory. Assuming a charging resistance of 500 ohms, which is the order of magnitude that can be easily obtained, the time constant is $5 \mu\text{sec}$, and a $0.1\text{-}\mu\text{sec}$ pulse is not wide enough. The conflicting requirements are met by widening the original $0.1\text{-}\mu\text{sec}$ sample in successive stages, as shown in Fig. 7.

Saw-Tooth Generator. A schematic diagram of the saw-tooth generator is shown in Fig. 8. This is a Miller feedback circuit using three stages of gain, and gives extremely good linearity. Generation of the saw-tooth takes place during the presence of a gating pulse on the normally cut-off suppressor of the first stage of the amplifier. Temperature drift affecting the saw-tooth slope is compensated by returning the resistor of the RC combination which determines the slope to a variable voltage under control of the first or principal digit in the B channel of the output of the number generator. The output of the number generator ranges from 0 to 1023. If the first digit is one, the output

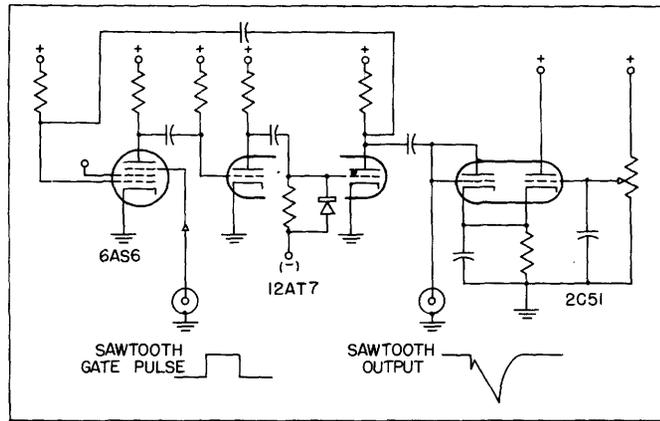


Fig. 8 Saw-tooth generator

is equal to or greater than 512. If the first digit is zero, the output is less than 512. The voltage applied to the slope control resistor is proportional to the relative frequency of occurrence of one in the first digit; and is of the proper polarity to decrease the size of the number if the relative frequency is greater than 50 percent, and to increase the size of the number if the relative frequency is less than 50 percent. Use of this drift compensation circuit has reduced errors due to long-term drifts in the correlator to negligible importance.

Comparison Circuit. A schematic diagram of the comparison circuit is shown in Fig. 9. The saw-tooth is applied to the grid of V1 and the boxcar to the grid of V2.

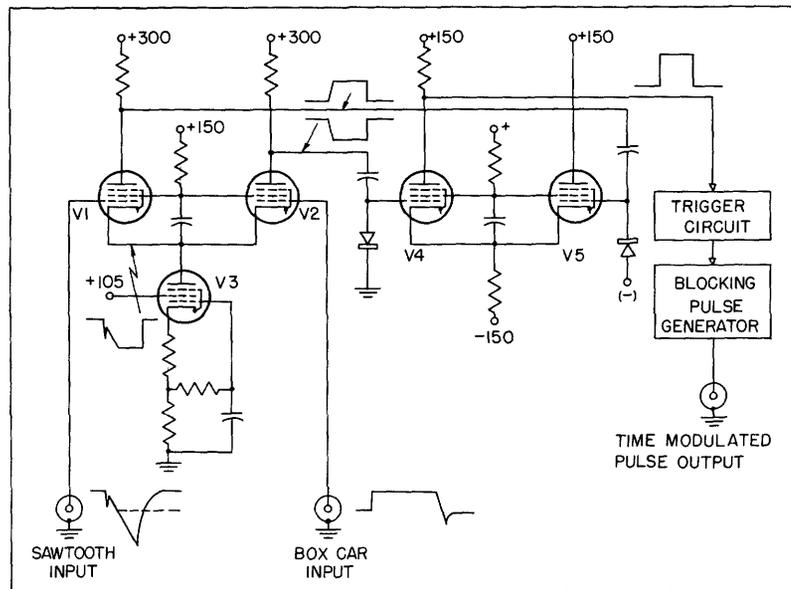


Fig. 9 Comparison circuit.

As the saw-tooth passes through a narrow range of voltage in the neighborhood of the boxcar voltage, the plate current of V1 shifts to V2. No triggering is involved, since no

regeneration is present. Because of the pentode V3 in the common cathode circuit of V1 and V2, the plate current of V2 after the shift is equal to the plate current of V1 before the shift. This causes the voltage swings across the plate resistor of V1 and V2 to be equal, and allows the use of fixed grid biases in V4 and V5. The grids of V4 and V5 are driven in push-pull. A narrow slice is taken near the midpoint of the grid swing, and appears in amplified form at the plate of V4. The resulting essentially rectangular wave form is applied to a regenerative amplifier, or trigger circuit, which derives a sharp pulse from the leading edge of the rectangle. This sharp pulse is used to reset a flip-flop (not shown on Fig. 9, see Fig. 5) previously triggered by the leading edge of the saw-tooth gate. The wave form at the plate of the flip-flop is the required duration-modulated pulse. It is used, as has been indicated, to gate the timing pulse generator which drives the binary counter in the number generator.

High-Speed Counter. Very little need be said about the binary counter in the number generator. Since 10 digits are used, a maximum of 1023 pulses may be counted. In order not to take too long in the counting, a 5-Mc repetition rate is used for the pulses to be counted, thus requiring at most 200 μ sec. The first stage of the counter is shown in Fig. 10. The circuit was tested for several weeks at 10 Mc/sec before being incorporated into the equipment. The essential feature of the circuit, which allows it to

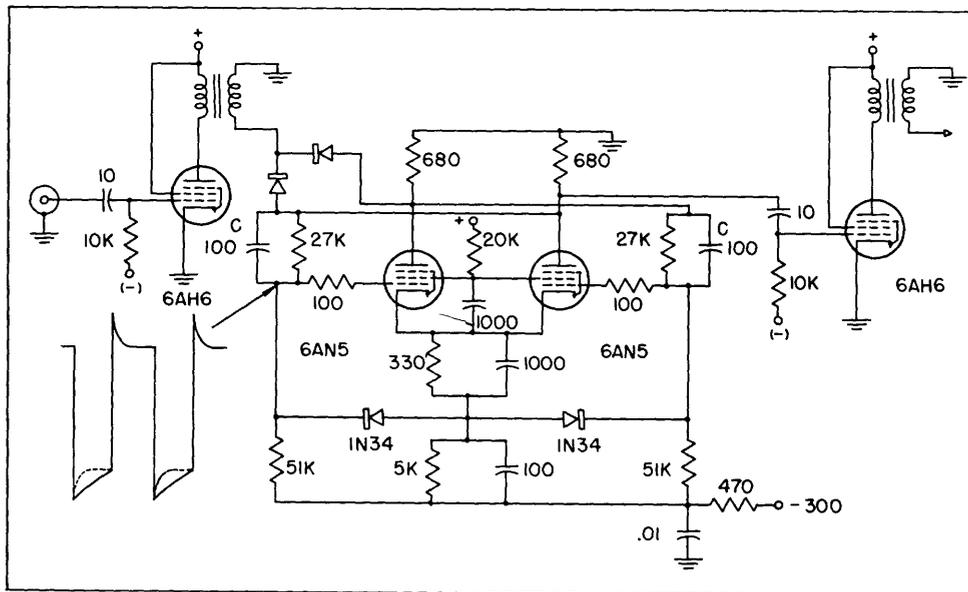


Fig. 10 High-speed counter

operate at unusually high speed, is that crystal diodes from the grids to a tap on the cathode resistor are used to discharge the coupling capacitors C through the low input impedance of the opposite tube. This permits the use of large coupling capacitors (100 μ f in this case) and still permits them to discharge quickly after each triggering to a voltage from which the flip-flop can again be triggered.

Register and Multiplier. After each of the numbers for the two input channels is generated, it is gated into storage in the number register (see Fig. 11). The register consists of two sets of ten flip-flops each (one set for each of the two numbers to be

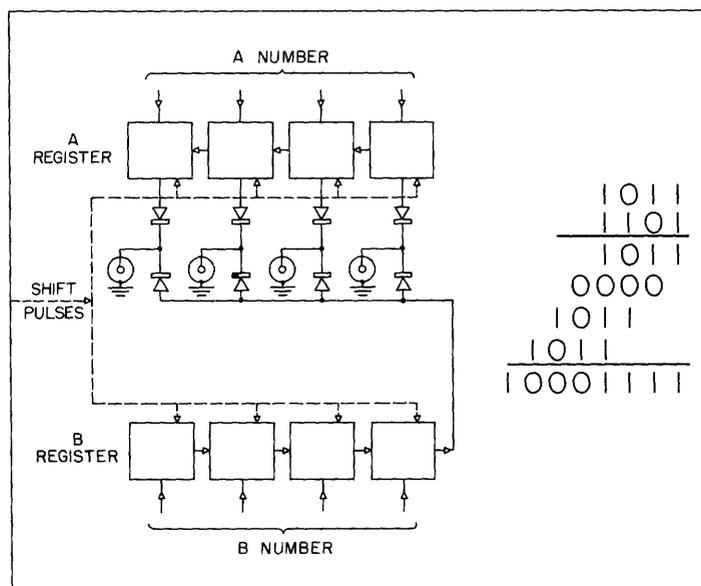


Fig. 11 Block diagram of part of number register.

multiplied) and includes means for shifting the A numbers to the left and the B numbers to the right. Although ten digits are stored in each register, for simplicity only four stages of each are shown in Fig. 11. Assuming that a number is in one of the registers, the shifting is accomplished by resetting all of the flip-flops to zero. Associated with each flip-flop is a monostable delay multivibrator. Any flip-flop in state one has its state changed by the reset, and produces a pulse which triggers its associated delay multivibrator. The trailing edge of the delay multivibrator is used to set the next flip-flop to one. Thus each symbol of the stored numbers is moved one stage to the left (in the upper register) or right (in the lower register). This process continues, as shift pulses are applied, until only zeros are present in the register. The shift pulses are then stopped.

In Fig. 11 is also shown an example of binary multiplication. The multiplication is carried out in a manner analogous to decimal multiplication, as follows: 1. Each digit of the upper number is multiplied by the digit occupying column four of the lower number, and the result is written in the highest empty spaces directly under the upper number. 2. The upper number is shifted one space to the left and the lower number, one space to the right. 3. Steps 1 and 2 are repeated until all digits have been used. 4. The partial products obtained with each step 1 are summed to give the complete product.

In the machine the process is exactly similar. The value of each partial product is present between shift pulses in the state of the coincidence circuits shown in Fig. 11. In

fact, the first partial product is present as soon as both numbers are stored. This partial product is read off into the accumulator, or integrator, by means of a sequence of pulses which examine the state of the coincidence circuits in succession, and send, or fail to send, trigger pulses to the appropriate stages in the integrator. As soon as all the coincidence circuits have been read, a shift pulse is sent to the register, and the reading process is repeated. This sequence of operations continues until only zeros remain in the register. The two ten-digit binary numbers are multiplied together in 250 μ sec, once they are both present in the register.

Integrator and Recorder. As has been indicated, the integrator comprises a cascade of scale-of-two circuits, or flip-flops. A multiple-pen Esterline-Angus Recorder is connected to the last ten stages of the integrator and the condition of these stages is read into the recorder at the end of each integration period. The integrator is then reset before beginning a calculation with the next value of τ . A switch is provided for skipping one or more of the intermediate stages in the integrator so that the ten stages recorded may always represent the most significant part of the result. At the same time that the digits are recorded they are decoded in a voltage adding circuit, and the result is recorded on a General Electric Recording Microammeter. The decoded recording is useful in test runs for immediate observation of results, but is not as accurate as the digit recording.

Sample Results

Fig. 12 shows the correlation function of a sine wave as evaluated and plotted by the machine. The steps in τ are 4 μ sec.

Fig. 13 shows the correlation function of a limited wave produced by passing wide-band (3 Mc/sec) noise through an RC integrator (5 μ sec time constant) and then limiting the output of the integrator to produce a rectangular wave.

Fig. 14 shows the correlation function of a rectangular wave with independent random zero crossings*.

Fig. 15 shows the convolution integral

$$\int_0^{\infty} e^{-|\tau-\sigma|/T_2} e^{-\sigma/T_1} d\sigma$$

obtained by taking the crosscorrelation of the output and input of an RC circuit ($T_1 = 50 \mu$ sec time constant). The input to the circuit was obtained by passing wide-band (3 Mc/sec) noise through an RC ($T_2 = 5 \mu$ sec time constant) integrator (10).

*Obtained from equipment designed by C. A. Stutt.

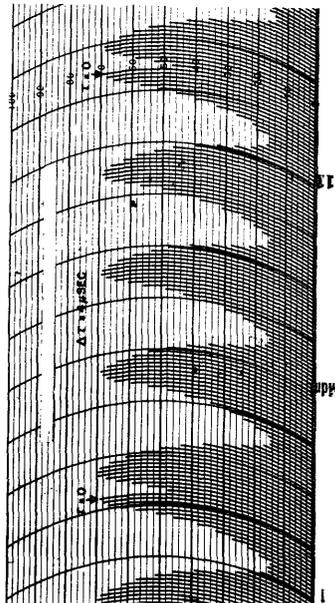


Fig. 12 Autocorrelation of sinusoid.

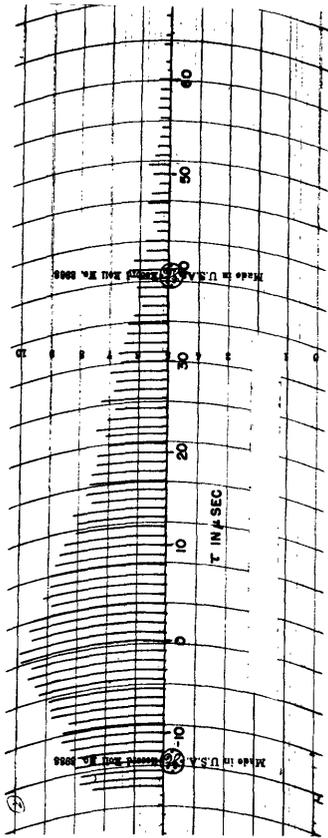


Fig. 14 Autocorrelation of random square wave.

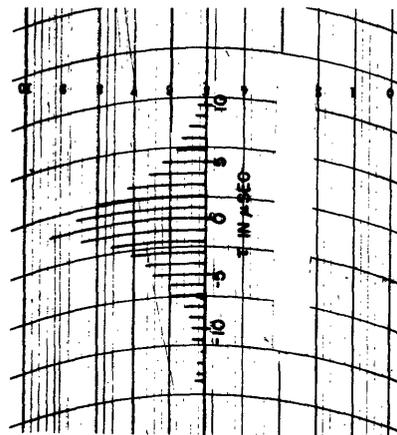


Fig. 13 Autocorrelation of clipped noise.

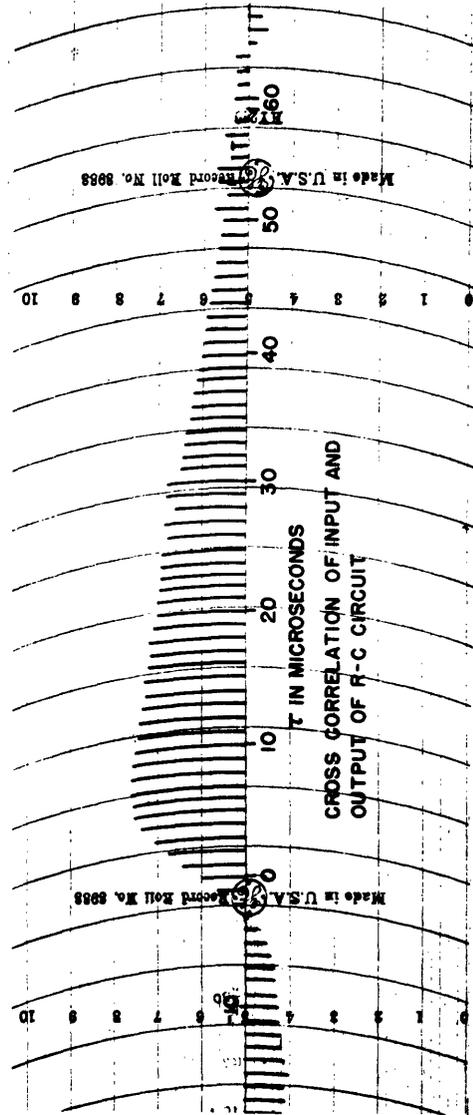


Fig. 15 Convolution of exponentials.

Detailed Functional Diagrams

A detailed functional block diagram of the complete correlator is shown in Fig. 16 and Fig. 17. Fig. 16 includes all the computing circuits of the machine and Fig. 17 includes all the timing circuits. These functional schematics are easily followed on the basis of the preceding discussion of individual circuits.

Schematic Diagrams

Complete schematic diagrams of all circuits are given in Figs. 18 through 31. It is believed that these detailed schematics may be useful as reference material to future designers of similar equipment.

Photograph

A photograph of the correlator is shown in Fig. 32.

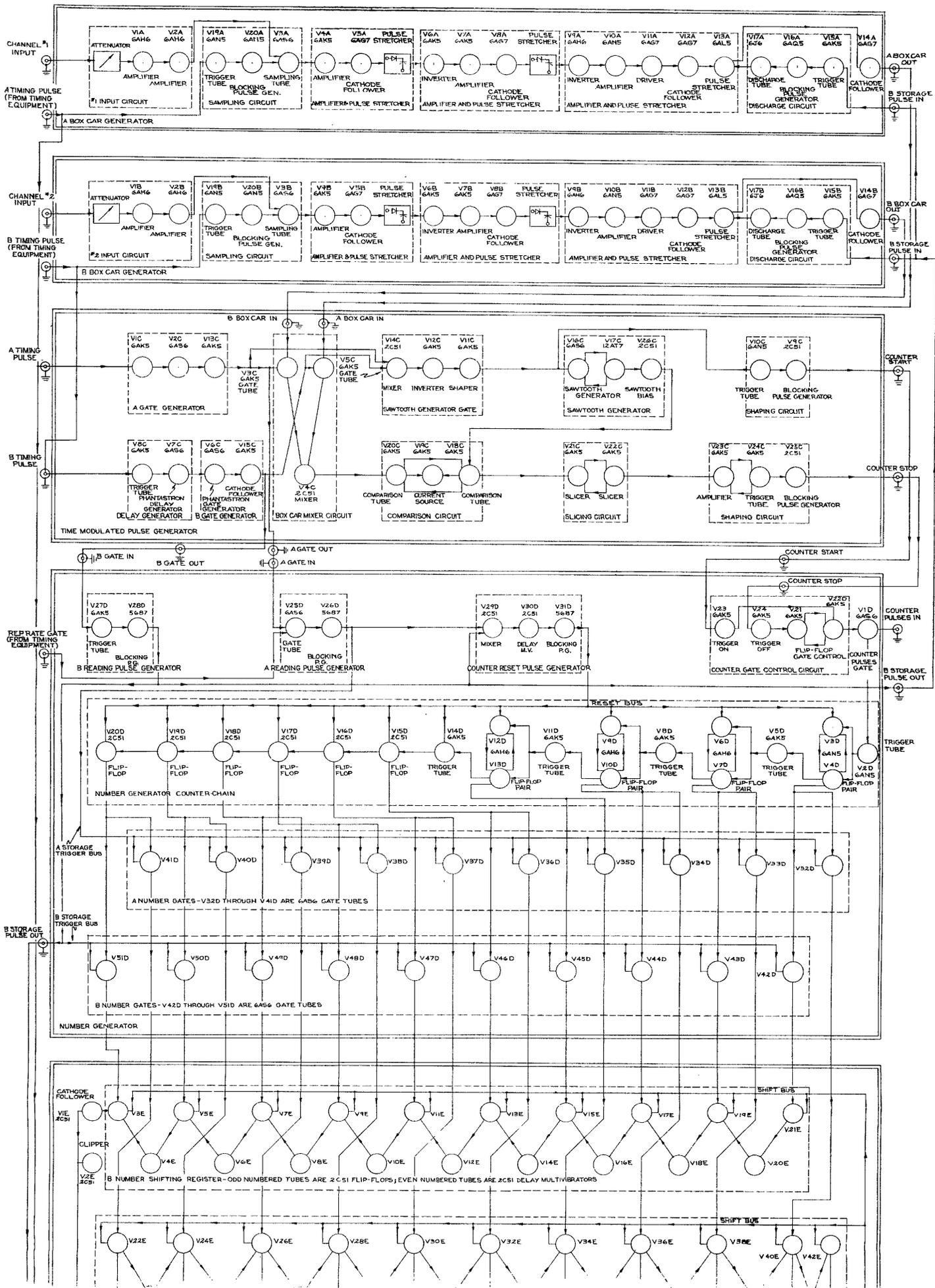
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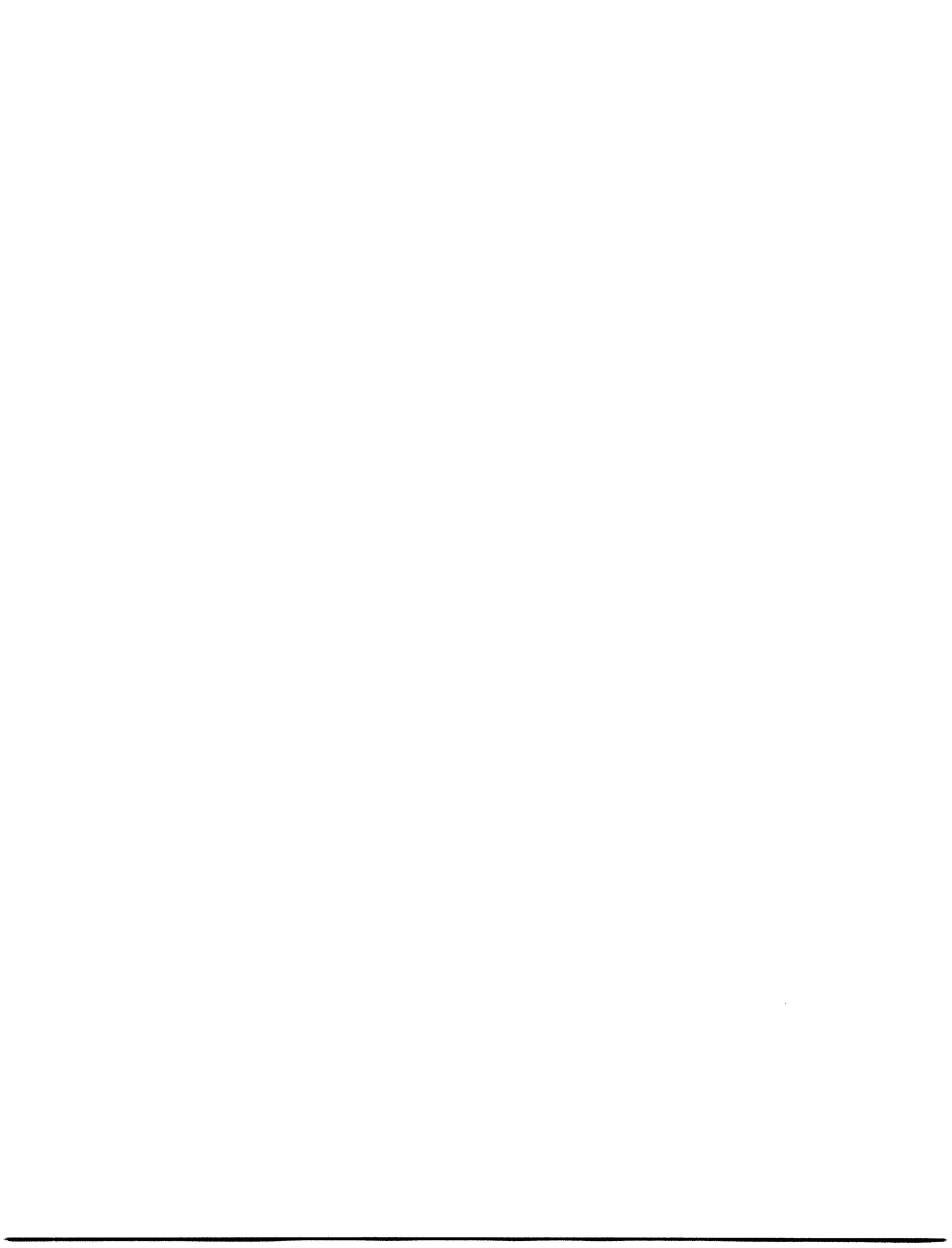
The writer wishes to express his appreciation to Professors J. B. Wiesner and Y. W. Lee for the supervision of this project, to Professors R. M. Fano and W. B. Davenport, Jr. for helpful suggestions, and to T. P. Cheatham, L. G. Kraft, A. J. Lephakis and C. A. Stutt for their generous assistance on numerous problems connected with the design and testing of the machine.

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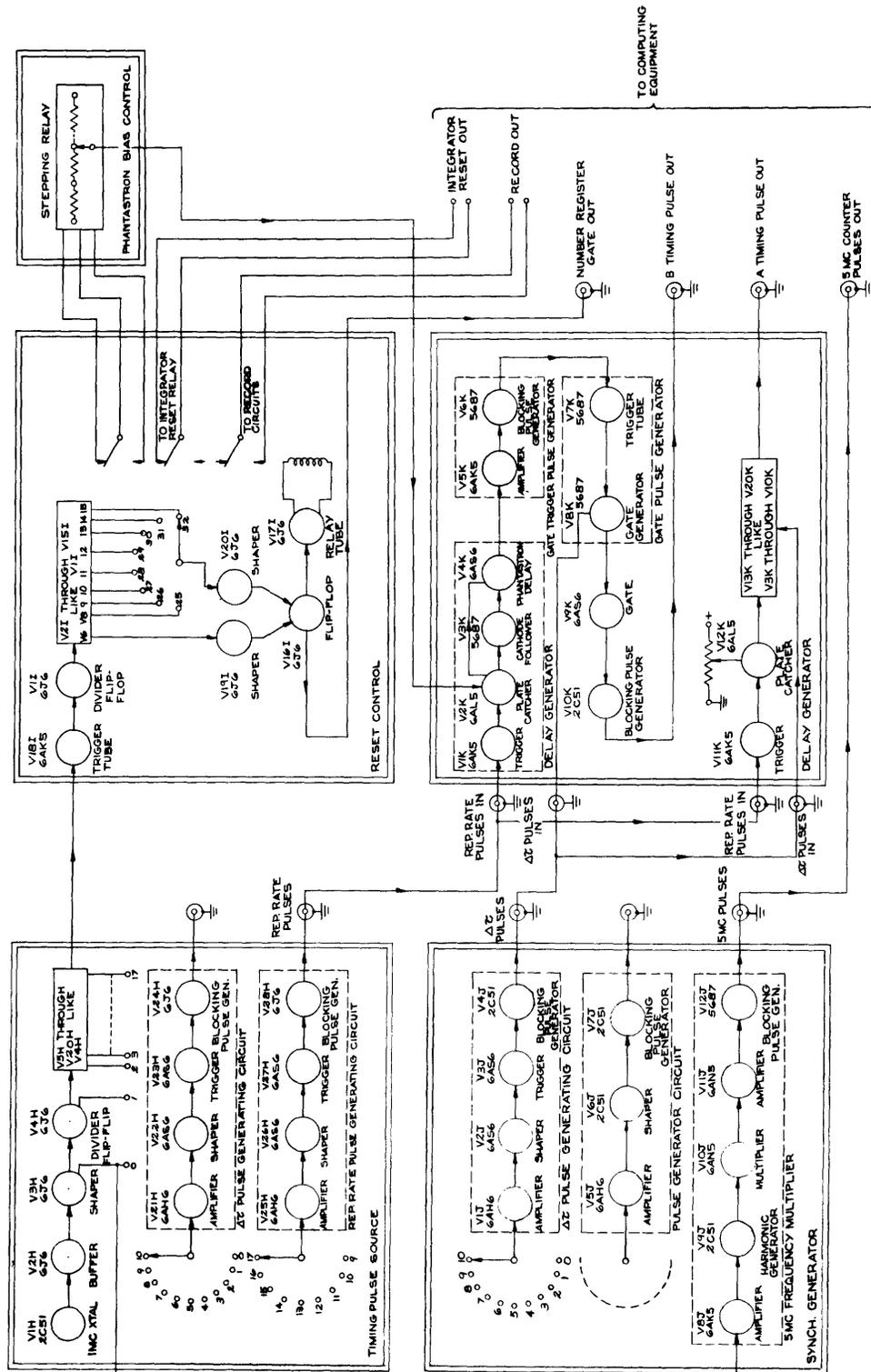


Fig. 17 Timing circuits.

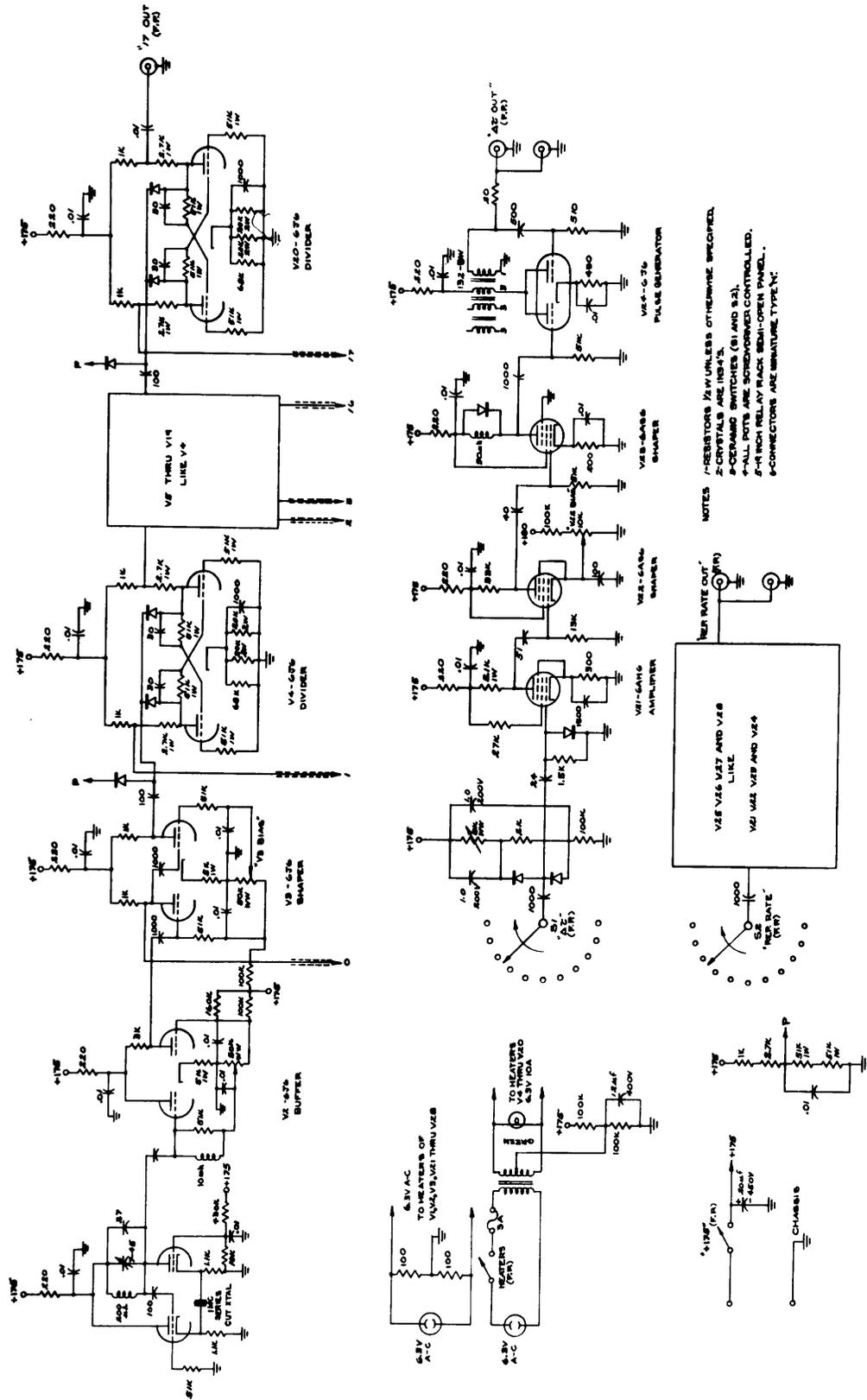
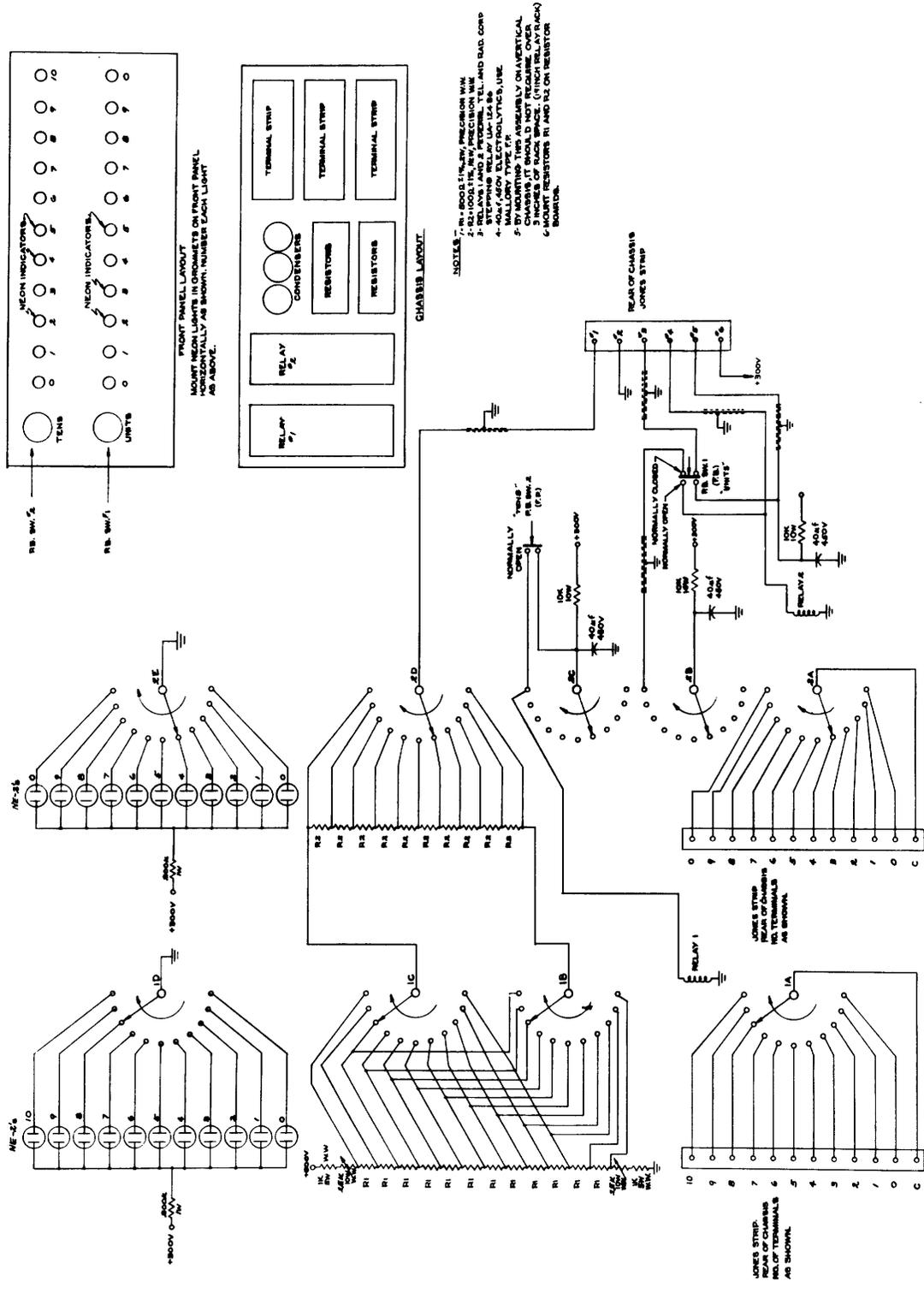


Fig. 18 Timing pulse source.



- NOTES:
- 1- 800 Ω 1/4 W, PRECISION WM
 - 2- 100 Ω 1/4 W, PRECISION WM
 - 3- 100 Ω 1/4 W, PRECISION WM
 - 4- 40 μF 450V ELECTROLYTIC, UIC
 - 5- 40 μF 450V ELECTROLYTIC, UIC
 - 6- 40 μF 450V ELECTROLYTIC, UIC
 - 7- 40 μF 450V ELECTROLYTIC, UIC
 - 8- 40 μF 450V ELECTROLYTIC, UIC
 - 9- 40 μF 450V ELECTROLYTIC, UIC
 - 10- 40 μF 450V ELECTROLYTIC, UIC

Fig. 22 Phantastron bias control.

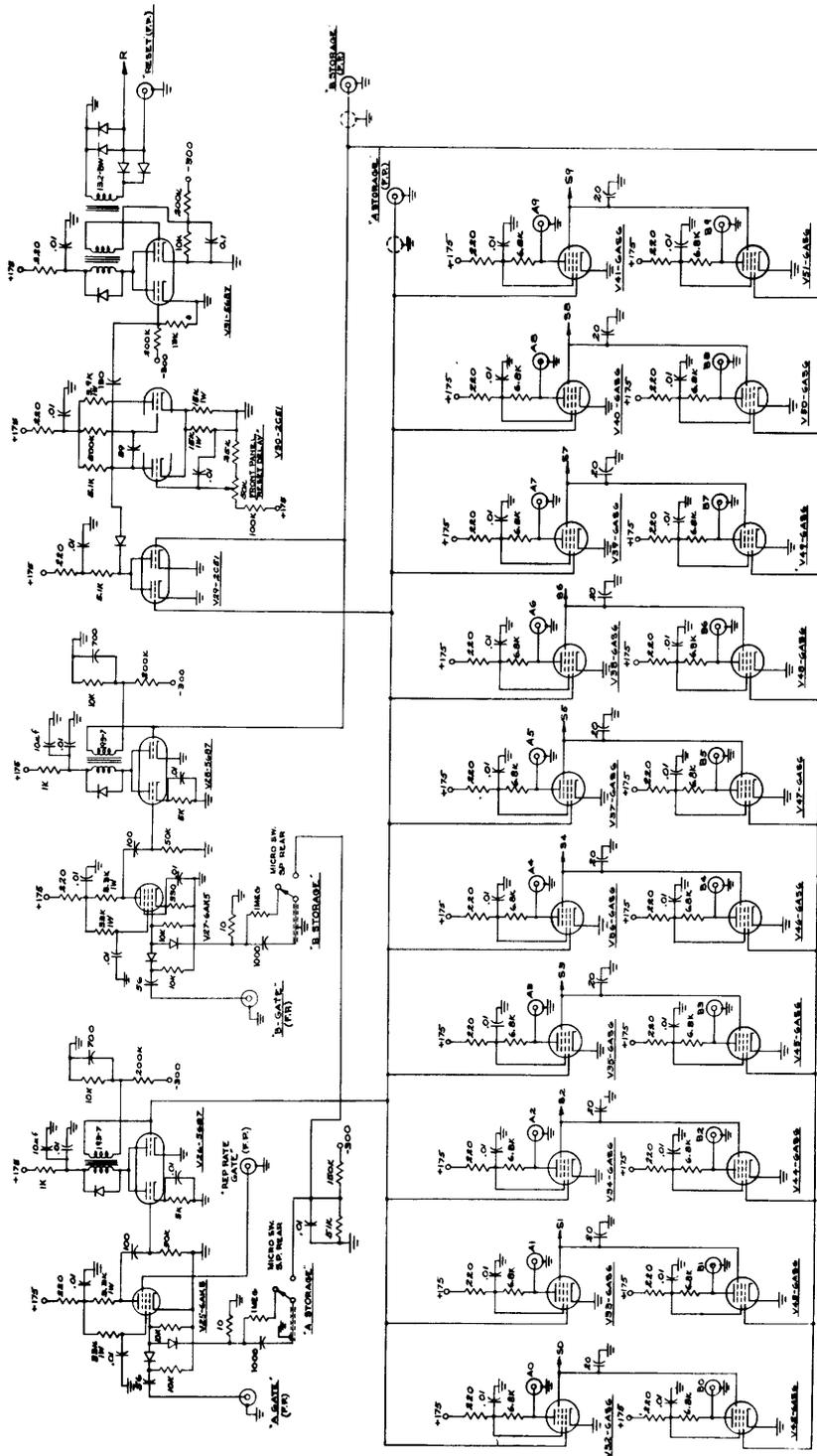


Fig. 26 Number gates.

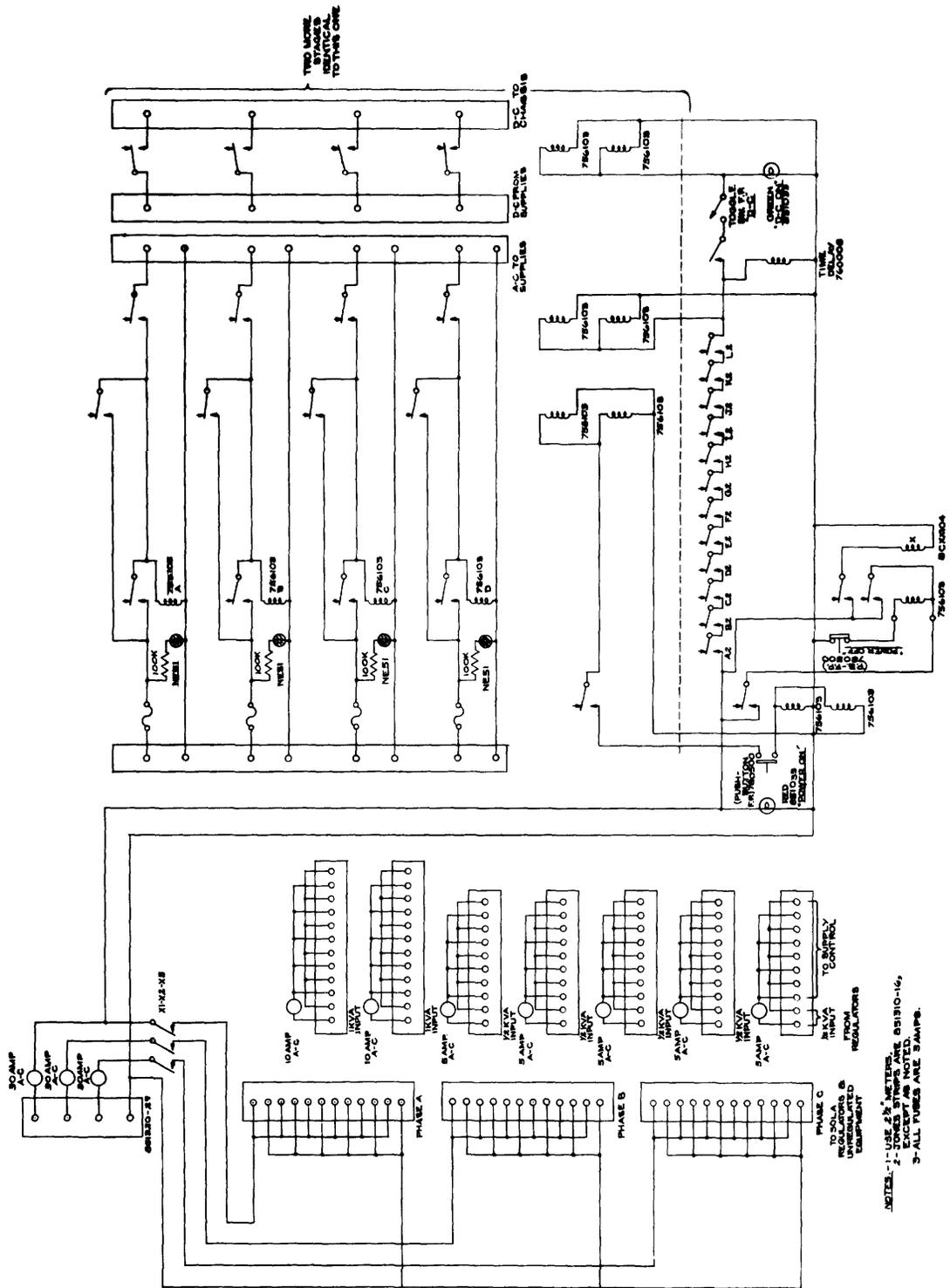


Fig. 31 Power control panel.

NOTES: 1- USE 2.5 METERS.
 2- JONES STRIPS ARE 81310-16.
 3- ALL USES ARE STAMPS.

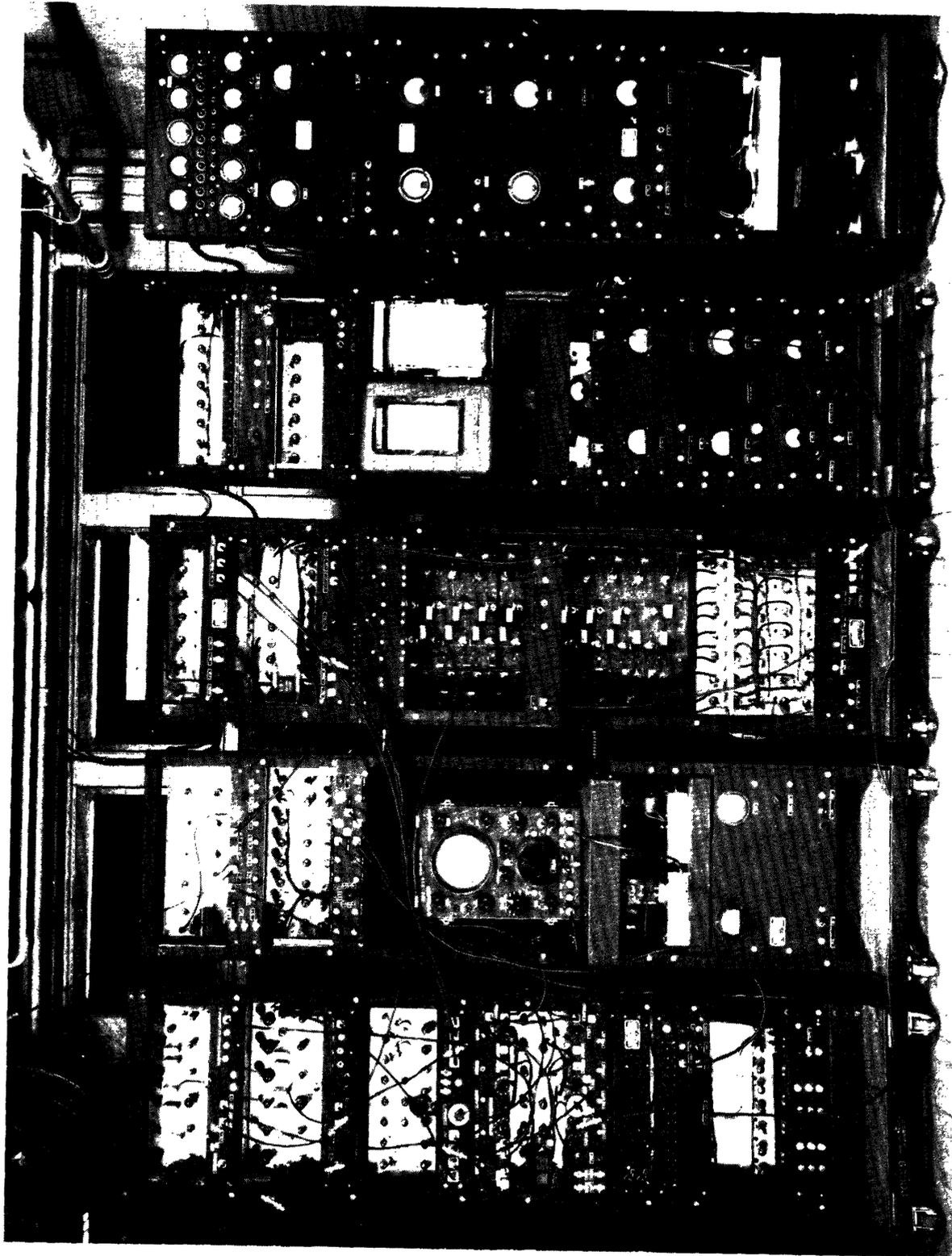


Fig. 32 Digital electronic correlator.