Division 6 - Lincoln Laboratory Massachusetts Institute of Technology Cambridge 39, Massachusetts

SUBJECT: TEST RESULTS ON THE DCL MEMORY PLANE

To: F.E. Vinal

From: E. A. Guditz

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Abstract: The DCL plane (C25) is compared with a standard MTC plane which has General Ceramics cores. Except for requiring slightly higher driving currents for maximum output, the DCL plane compares favorably with the MTC planes and could, in fact, operate as a substitute MTC plane without seriously impairing the system's margins.

Plane C25, herin referred to as the DCL plane, contains cores made at this laboratory by Group 63. These cores are designated DCL-1-180. The object of this test was to find the optimum driving current for the plane and the worst ONE-ZERO ratio. Data was taken showing the relationship of Sensing Amplifier Gate Tube bias to Strobe Time for four values of driving current and four different patterns.

Patterns of all ONES and all ZEROS were used to find optimum driving current. Data was taken at 1.0a., 0.9a., 0.8a., and 0.7a. The attached graphs SA-48528-G through SA-48531-G show the comparison of the DCL plane (C25-dotted line) with the MTC plane (C21-solid line) under these conditions. Note that the MTC plane has its maximum ONE-ZERO ratio in the 0.8a. to 0.9a. region while the DCL plane has an increasing ONE-ZERO ratio right up to the maximum available driving current of 1.0a. Also, the ONE-ZERO ratio of the DCL plane at this maximum available current is approximately equal to the best ONE-ZERO ratio available from the MTC plane. It should be noted that at the best operating current for the MTC plane the DCL plane has a very good ONE-ZERO ratio and is quite capable of operating in conjunction with MTC planes.

Graphs SA-48532-G through SA-48535-G show the operating margins for the two complementary patterns of complemented pairs-checkerboard for driving current values of 0.8a. and 1.0a. Again it can be seen that the margins are still increasing at the maximum available driving current of 1.0a. In these graphs a comparison is made not with the MTC plane but with and without the Post-Write Disturb current. It is interesting to note that the Post-Write Disturb current is most beneficial for the pattern with zeros in the corners (Graphs SA-48534-G and SA-48535-G). The reason for this is not understood. Observation of Sensing Winding output voltage showed that the spread in outputs is very small and is as good or better than that observed from the MTC planes.

It is felt that a memory made of planes using these cores and operated at its optimum currents would have operating margins at least equal to those of the present $6\mu \ge 6\mu$ memory.

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EAG: jb

Group 63 Staff (Group 62) Magnetic Memory Section Staff (Group 62) W. Wittenberg (IEM)

Graphs

SA-48528-G SA-48529-G SA-48530-G SA-48531-G SA-48532-G SA-48533-G SA-48534-G SA-48535-G



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SA-48529-E





SA-48531-C-



SA-48533-6



SA-48533-G





SA-48535-G