

Report R-211

A MAGNETIC MATRIX SWITCH
AND
ITS INCORPORATION INTO A COINCIDENT-CURRENT MEMORY

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FOREWORD

The random-access memory is an important element of a high-speed digital computer. This memory must be capable of operating at high speeds with long-time reliability, and should be compact and of low cost. The coincident-current magnetic memory has been proposed as a possible device which has these qualifications. It was one of the original purposes of this thesis research to prove experimentally the feasibility of a coincident-current memory of useful size. Since the distribution of the thesis report is limited and since the information it contains is of interest to the computer field, it is being issued as a Digital Computer Laboratory R-series report.

Although one of the features of this type of memory is the straightforward method by which the storage units are selected, there remains the switching problem associated with the selection and driving of its coordinate lines. Early in the research, the magnetic-matrix switch was developed as a solution to this problem, and the thesis was broadened to include the proving of the practicability of using such a switch for selecting and driving the coordinate wires of a large coincident-current memory array.

The author is grateful to Mr. Robert Everett who supervised the thesis work, and to the staff members, technicians, draftsmen, and secretaries of the M. I. T. Digital Computer Laboratory for their invaluable aid during the research and preparation of the thesis report.

ABSTRACT

A MAGNETIC MATRIX SWITCH AND ITS INCORPORATION INTO A
COINCIDENT-CURRENT MEMORY

by KENNETH H. OLSEN

Submitted to the Department of Electrical Engineering on May 16, 1952 in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

A multi-position switch, capable of handling pulses shorter than one microsecond, can be made from magnetic cores. Windings on the magnetic cores, when matrix-connected, control selection of the switch output. These windings can be excited with either direct current or pulses. This switch is capable of transmitting power efficiently, and the magnetic cores from which it is made are inexpensive and rugged, and promise reliability and long life.

Two such switches pulse the 16 coordinate rows and the 16 coordinate columns of a coincident-current magnetic-core memory. The complete cycle-time of the memory, including the switch set-up time, reading of information, and re-writing of information, is less than 4 microseconds.

Design of the magnetic-matrix switch is facilitated by an equivalent-circuit technique.

Thesis Supervisor: Robert R. Everett,
Associate Director of the Digital
Computer Laboratory

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CHAPTER I INTRODUCTION

The magnetic-matrix switch is a multiposition selection switch. It can distribute energy to any one of a number of positions in the same sense that a mechanical rotary switch can distribute energy to many positions. The selection in this magnetic switch is, however, electrically controlled in that the selected position is determined by the presence of current at certain inputs to the switch.

The Saturable-Core Transformer as a Simple Switch

The basic building block of the magnetic-matrix switch is the saturable-core transformer. Although much of the effort devoted to the study of this transformer has been concerned with its use in magnetic amplifiers, there are many applications for this device as a switch. Before its use in the magnetic matrix switch is presented, the operation of the saturable transformer will be considered.

The circuit schematic in figure I-1 shows a simplified saturable-core transformer. With zero current in the control winding (that is, with the control circuit open) this device acts as a simple transformer. It operates about the zero-current point on the flux-current curve where every change in the primary current (shown as the vertical sine wave) produces a significant change in flux and thus a voltage across the secondary. However, when the control circuit is closed, as in figure I-2, and a biasing current flows in the control winding, the operating point is displaced to the flat portion of the

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F-1467
SN-369

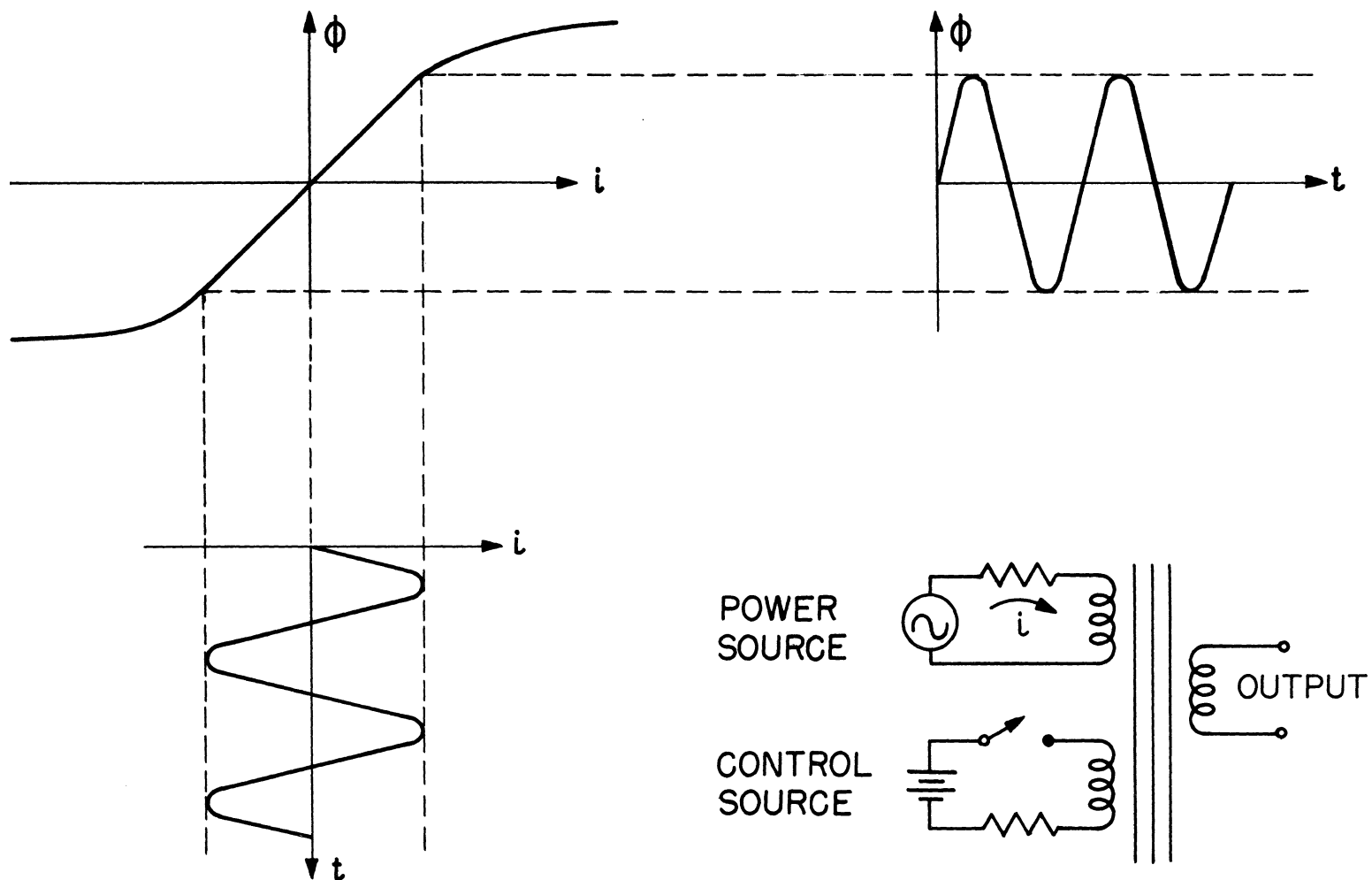


FIG. I-1

SATURABLE TRANSFORMER (UNSATURATED)

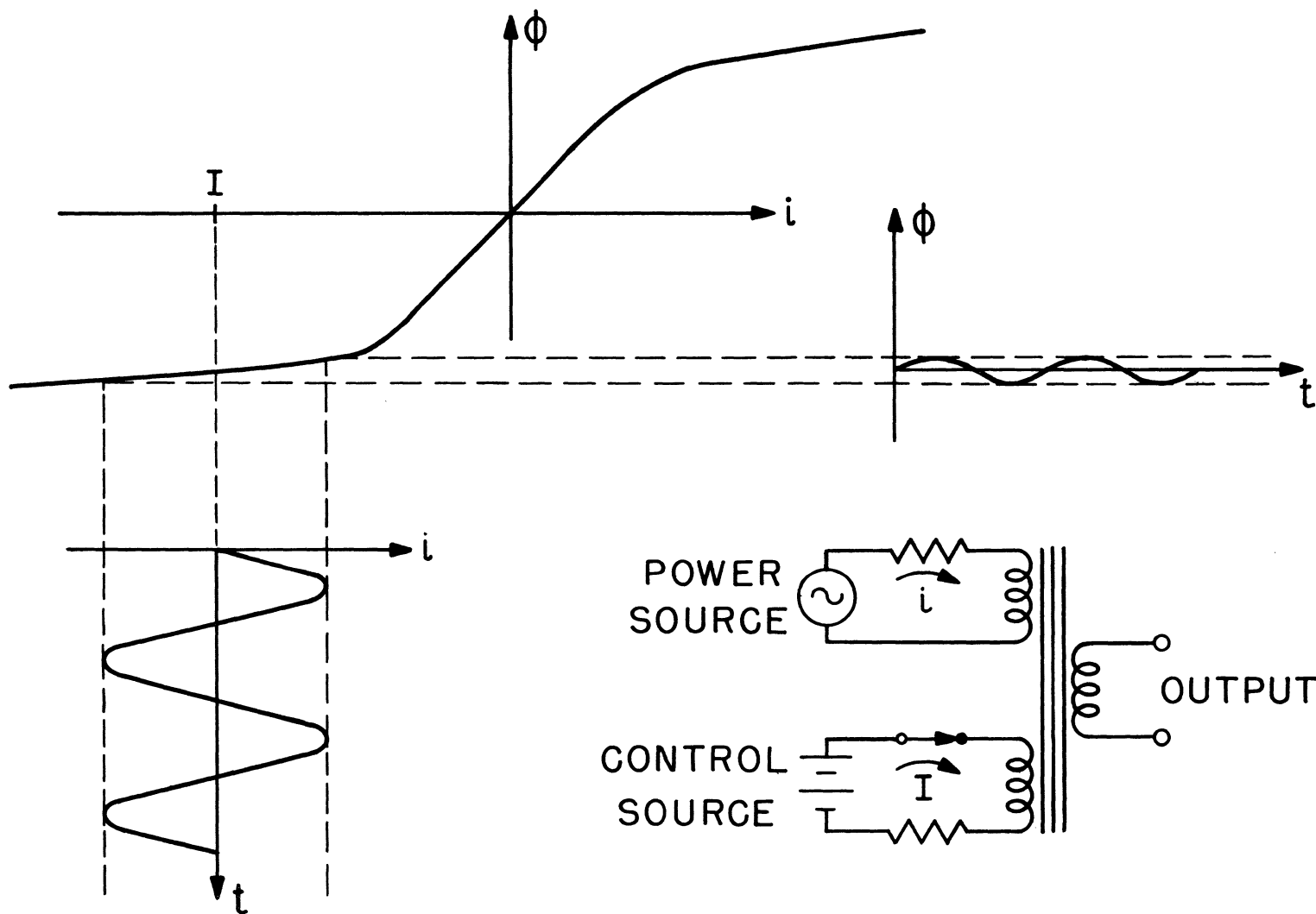


FIG. I-2

SATURABLE TRANSFORMER (SATURATED)

flux-current curve where there is little change in flux for changes in primary current.

Operating under these conditions of zero or full current in the control winding, makes the transformer, in effect, a simple single-pole, single-throw switch. This switch has three very useful characteristics. First, it has the impedance-matching characteristics of a transformer. Second, it is in effect a power amplifier, since a little energy in the control winding can control a large amount of energy in the output. Third, an unlimited number of control windings can be put on the core. Current in any one of the windings saturates the core; current in more than one only saturates it further.

Application of the Transformer in the Magnetic-Matrix Switch

The magnetic-matrix switch is a multi-position switch consisting of a number of these saturable-core transformers - one for each output of the switch. Figure I-3 shows a four-position switch. It consists of four of the transformers just discussed. All their primaries are connected in series to a common driving source and their secondaries are the outputs of the matrix switch. The control windings are connected in a binary scheme to double-throw mechanical switches in such a way that, for each combination of switch positions, one and only one of the cores is not saturated or cut off. The secondary of this core is the selected output of the switch.

For example, if all the mechanical switches were in the ONE position, as they are in the figure, every core, except number three,

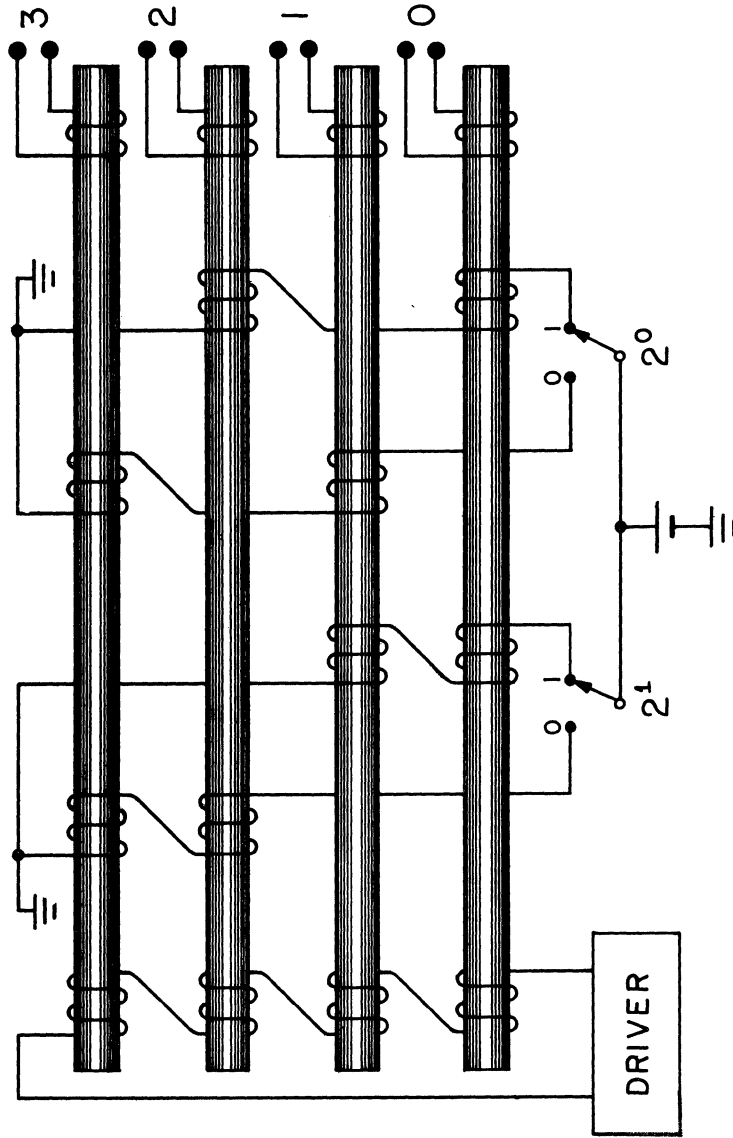


FIG 1-3

4-POSITION MAGNETIC - MATRIX SWITCH

would have current in at least one of its control windings. Since number three is the only core free to act as a transformer, it alone passes on the signal from its primary to its secondary. Likewise, any core could be selected by setting up its equivalent binary number in the mechanical switches. The setting ONE ZERO selects terminal two, for example.

It should be noted that n of these mechanical switches can control the selecting in a 2^n position magnetic-matrix switch: three mechanical switches can control an 8-position matrix switch; four, a 16-position switch; and five, a 32-position switch. Mechanical switches are shown here for clarity. In electronic circuits, flip-flops would be used in place of mechanical switches.

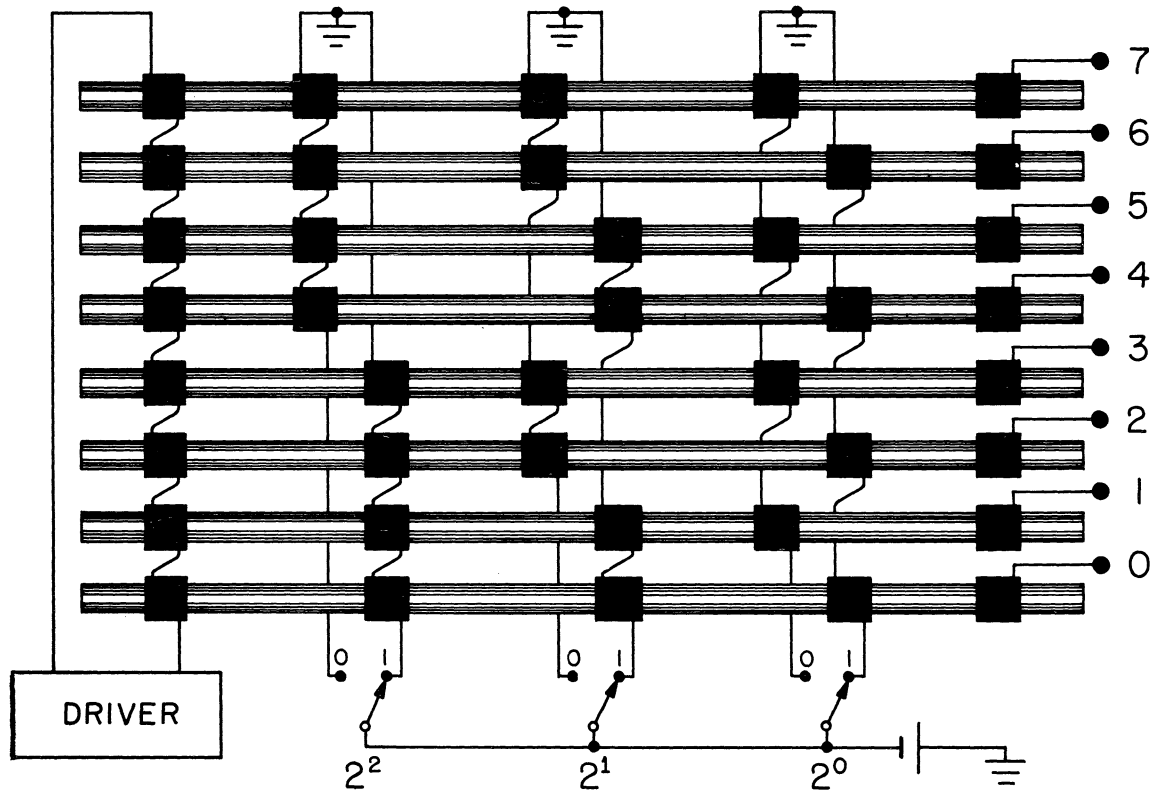
Eight-Position Switch

Figure I-4 is an eight-position switch. Here the binary scheme in the control windings can be seen more clearly. A binary number set up in the mechanical switches selects the equivalent numbered output. For example, ONE, ZERO, ONE selects terminal five.

An Alternate Switch

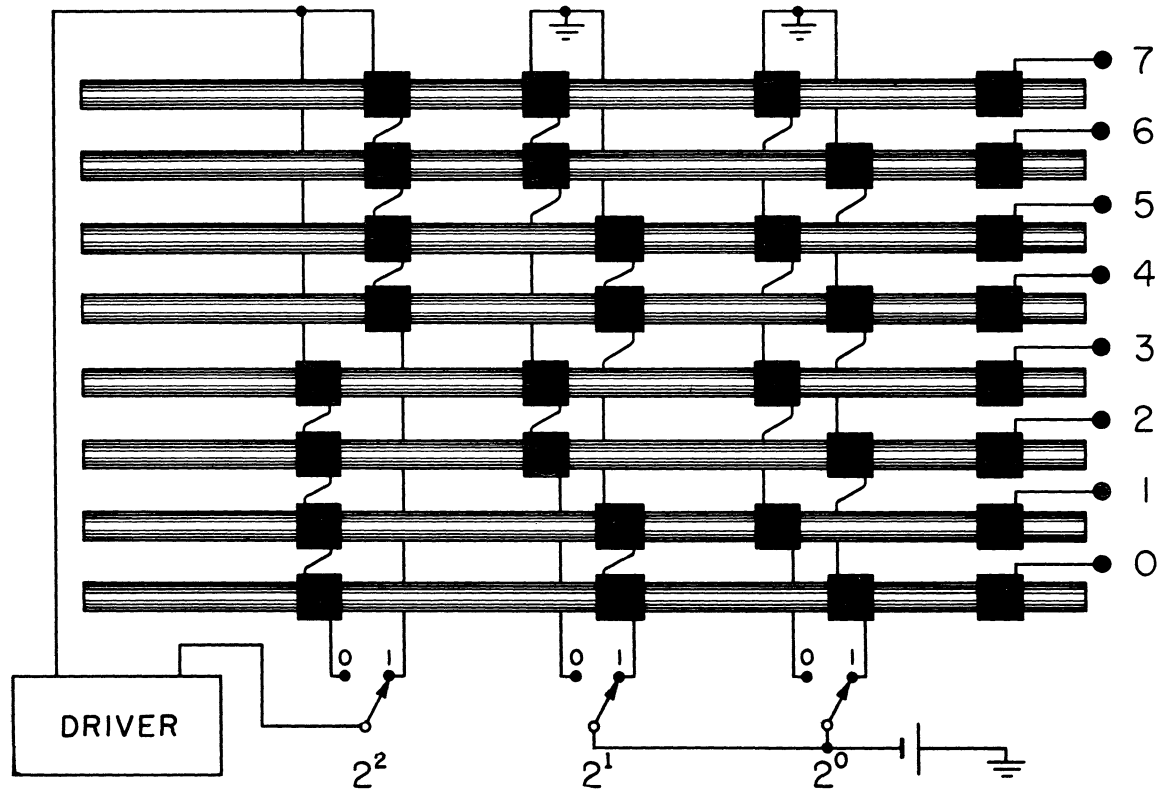
The switch can take a number of configurations. One which should be mentioned eliminates the need for a separate driving winding or primary on each core. This is done by using one of the sets of control windings for the combined operations of selecting and driving. Figure I-5 is an eight-position switch using this alternate scheme.

B-50910
T-1470
SN-372



8-POSITION MAGNETIC-MATRIX SWITCH

FIG I-4



8-POSITION MAGNETIC-MATRIX SWITCH
(ALTERNATE)

FIG I - 5

The driving windings have been removed and the position and sense of the first set of control windings reversed. Now the other control windings will saturate all but two cores, and this first set will select between the two and drive only the selected one. It can be seen that the setting ZERO, ONE, ONE still selects terminal number 3. The extra winding is eliminated at the expense of having to switch current from the driving source.

Demonstration Model

Figure I-6 is a photograph of an eight-position demonstration model of the magnetic-matrix switch. The eight cores are Deltamax ribbon wound in plastic cases. Their primaries are driven from a 5000-cycle sine-wave source. The control windings are selected by the toggle switches and are driven from two dry cells. A lampbulb at each secondary glows when its associated core is selected.

The toggle switches and the outputs are labeled so that the switch is a binary-to-octal decoder. A binary number set up in the toggle switches will select the corresponding octal number in the output.

On this model, the open-circuit voltage of the non-selected outputs is better than 40 db below that of the selected output. This excellent selected-to-nonselected ratio is due to the very low permeability of Deltamax when it is saturated.

In this model, and in the discussion up to this point, matrix switches driven by sine waves were used to demonstrate the principle of

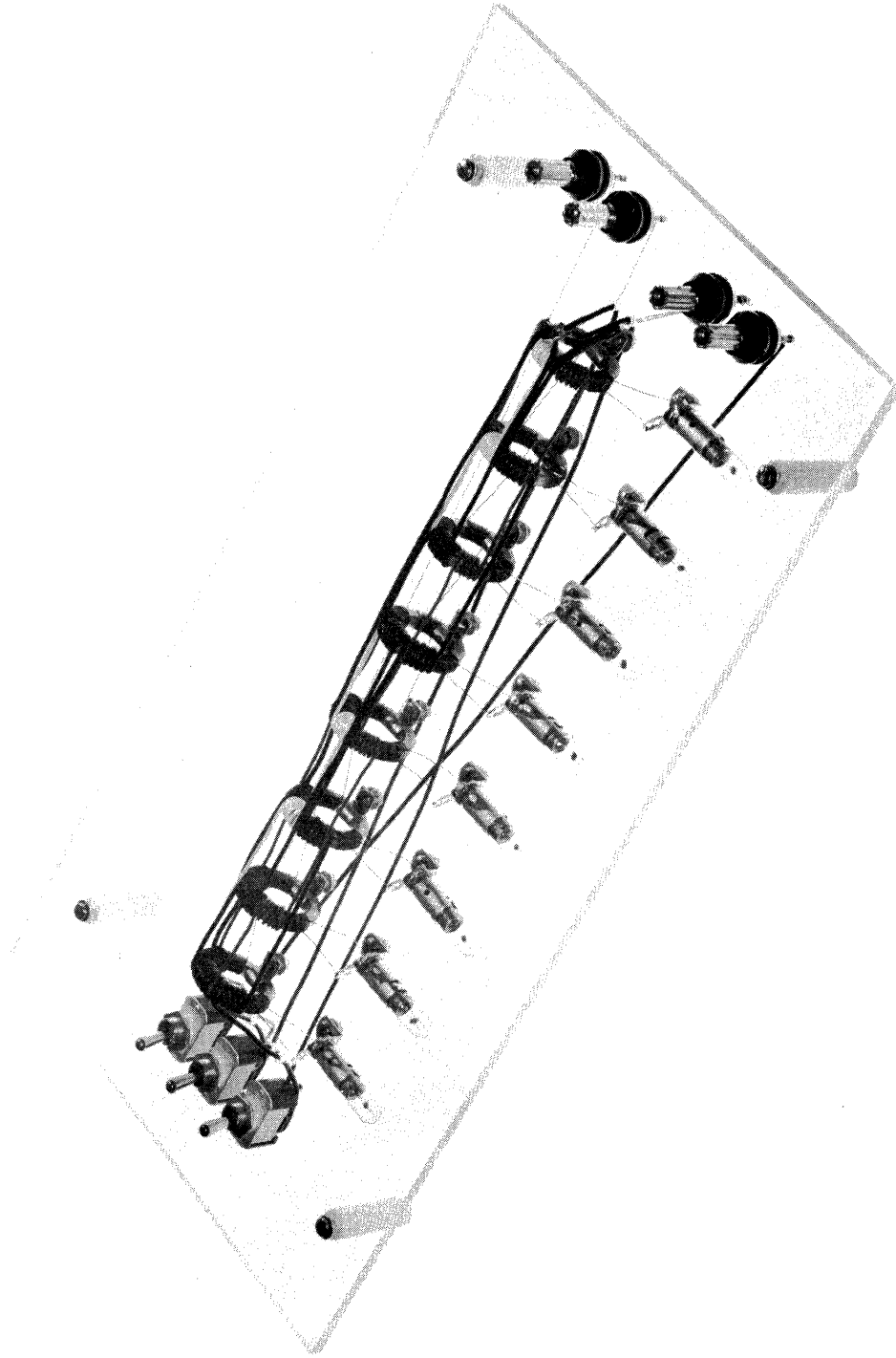


FIG. I-6
DEMONSTRATION MODEL OF MATRIX SWITCH

operation. There are many uses for the magnetic-matrix switch when driven from a sine-wave source. In those applications where the mechanical motion of a relay limits its speed or reliability, this switch might be used. For example, it could be used to decode paper tape and drive an electric typewriter directly.

Application to Pulse Circuits

The magnetic-matrix switch is particularly adaptable for use in pulse circuits. In this use, it is desirable that there be no output from the switch when the current in the control windings is changed. This makes desirable a core with a flux-current characteristic different from that in figure I-1. In the latter, there is a large change in flux, and so an output as current is changed in the control windings. Curve B of figure I-7 shows the general shape of the flux-current curve desired. One can see that the current, as I , is varied negatively from zero to saturation, there is little change in flux.

Figure I-7 illustrates the pulsed operation of an unsaturated saturable-core transformer. Curve A is the current applied to the primary. At first there is no change in flux as the current increases, until the knee of curve B is reached. Then flux increases with current until the core saturates. The flux stays at the saturation level as the current continues to increase and remains there even after the current is removed, as shown in the plot of flux in curve C. When the pulse of current of opposite polarity is applied, the operation is

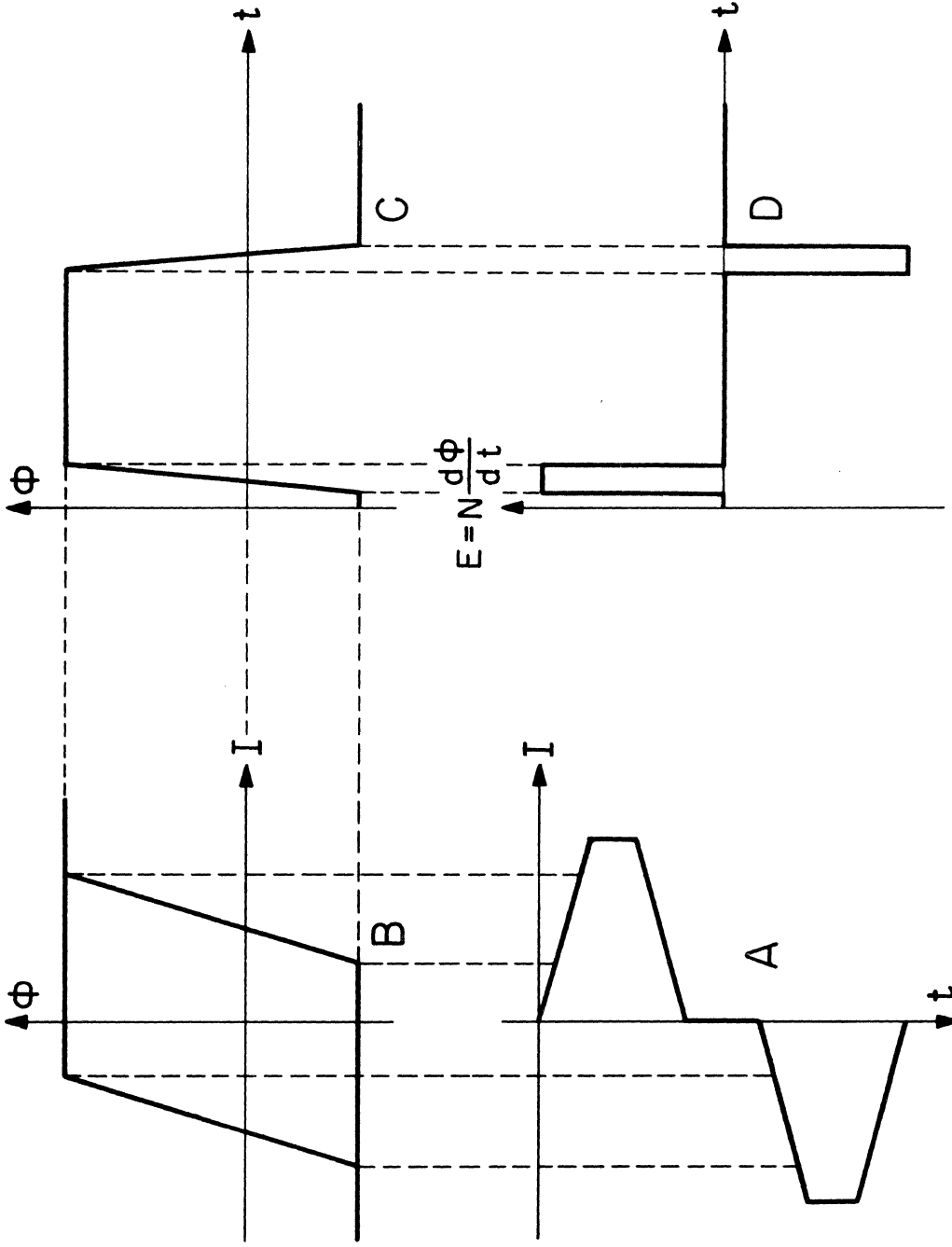


FIG. I-7

PULSED SATURABLE TRANSFORMER

reversed and the flux is returned to its original direction. The voltage across the windings is in proportion to the derivative of flux with respect to time. A flux curve like that of C will produce the voltage shown in D across a winding of N turns.

It should be noted that, after a single unidirectional pulse, a core with this characteristic will have its residual flux reversed and it will have to be returned to its original condition before it can be pulsed again in the same direction.

Materials Presently Available

The flux-current curve just discussed was idealized but a number of core materials are now available with this general type of flux-current characteristic that can be operated at pulse speeds. The new rectangular-loop ferrites are of particular interest for pulse circuits because of the ease with which they can be made to change direction of flux in less than one microsecond. The switch and memory discussed in this report are made with cores of this ferrite material. The metallic cores, such as Deltamax and Mo-Permalloy, have somewhat more rectangular loops, but eddy-current losses become significant when they are switched rapidly.

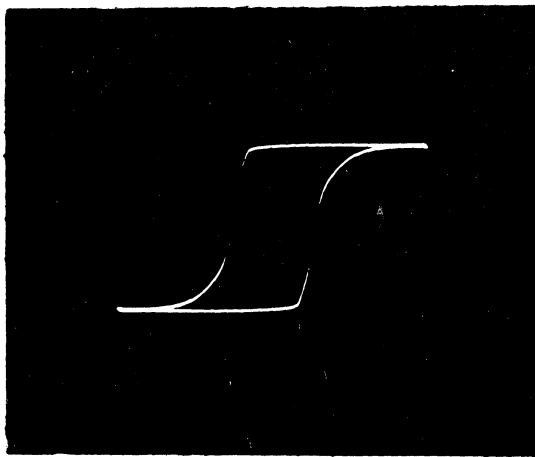
The cores are usually in the form of toroids or rings to keep the flux path short and to eliminate airgaps. Whereas the ferrites are a ceramic, molded and fired as a solid ring; metallic cores are usually in the form of thin ribbon wound on plastic or porcelain bobbins. Both the ferrites and the metallic cores are available in a large variety of sizes down to diameters less than that of a pencil.

CHAPTER II MATRIX SWITCH DESIGN CONSIDERATIONS

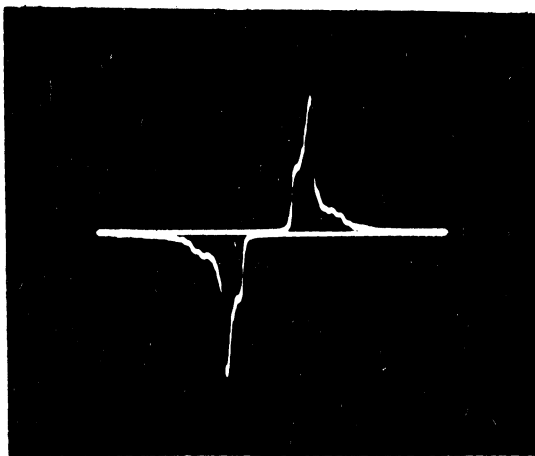
This research is concerned with the design of a switch to drive a coincident-current memory. However, many of the design considerations will be valid for other applications of the switch. In driving the memory, the switch is required to distribute rectangular pulses of current of about one and one-half amperes in amplitude and less than one microsecond in length. Only ferrite core materials have been considered because loss in the metallic cores is high when they are switched at these speeds.

Flux-Current Characteristics

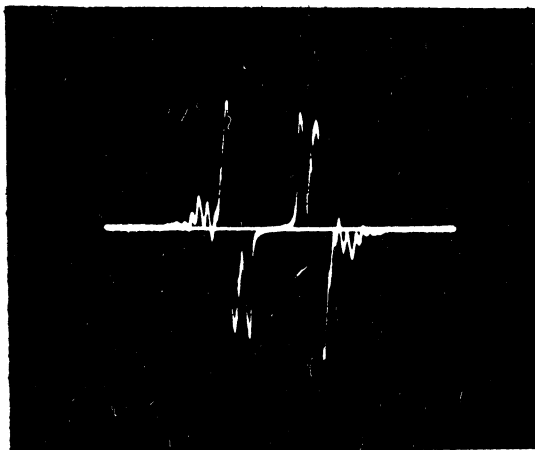
Three representations of the flux-current characteristic of a core that can be readily obtained experimentally are illustrated in figure II-1. The first and most common is the hysteresis loop where flux is plotted versus current. This configuration can be obtained by plotting on the X axis of an oscilloscope a varying current that is applied to a primary winding on the sample being tested. The voltage across a secondary winding is integrated and plotted on the Y axis of the scope. For small samples, a very-high-gain amplifier is needed in this scheme and the requirements on the amplifier are very stringent because any phase shift or hum pickup distorts the plot seriously. It is particularly difficult to keep the closing of the loop at the correct place (distance 4 in figure II-3.)



ϕ vs. I



$\frac{d\phi}{dt}$ vs. I



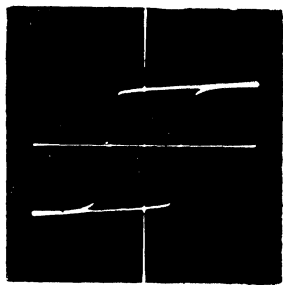
$\frac{d^2\phi}{dt^2}$ vs. I

FIG. II-1
FLUX-CURRENT CURVES, FERRAMIC III18 (259)

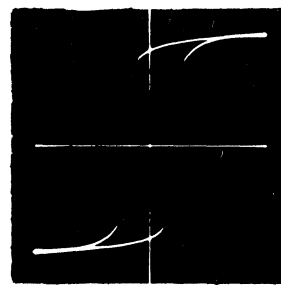
The second flux-current characteristic representation is a plot of $\frac{d\phi}{dt}$ versus I . Here the output of the secondary is plotted directly versus the current in the primary. The high-gain amplifier of the previous scheme is not needed because the signal is not attenuated by an integrator. In this presentation, it is possible to observe characteristics not readily observed in the ϕ versus I plot. For example, in figure II-1 it can be seen from the $\frac{d\phi}{dt}$ versus I plot that the steep part of the ϕ - I characteristic consists of three distinct slopes, but this is difficult to observe in ϕ - I plot. This second scheme necessitates a current source that changes linearly with time so that the amplitude scale of $\frac{d\phi}{dt}$ will be uniform. The source of current used in the plots in figure II-1 was the 60-cycle power line and so the scale of $\frac{d\phi}{dt}$ is not uniform.

The third scheme plots $\frac{d^2\phi}{dt^2}$ versus current. The output of the sample is differentiated and plotted versus current. In this plot, all the important inflexions in the ϕ - I curve are very clearly presented. This scheme has the disadvantages of the previous two schemes in that a high-gain amplifier is again necessary to make up for the loss in signal through the differentiator and a linear current source should be used to make the vertical scale uniform.

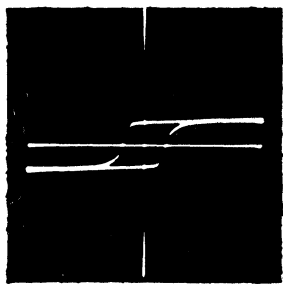
In this research, the ϕ versus I plot was used because it did not need a linear current generator, but the sample could be driven from the 60-cycle power line. Figure II-2 shows the flux-current plot of several ferrite materials available at the time of



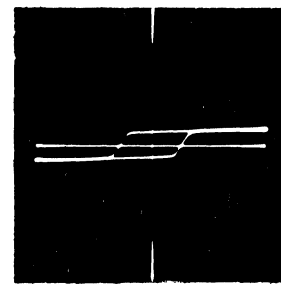
MF 1118 (262)



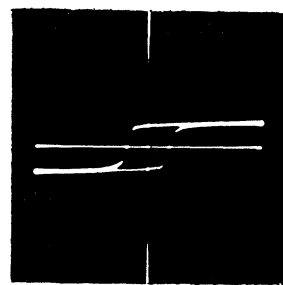
MF 1131 (262)



MF 1118 (259)



MF 1112 (259)



MF 1124 (259)

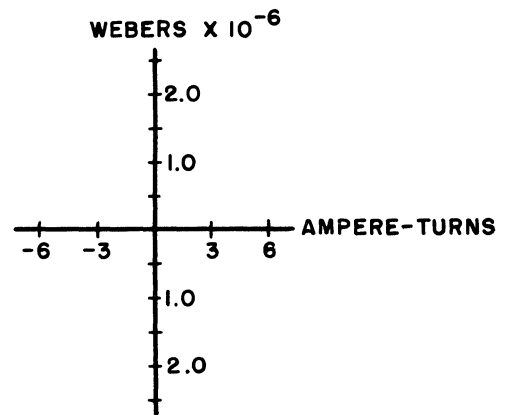


FIG. II-2
FLUX-CURRENT CURVES OF SEVERAL FERRITES

this report. The numbers in parentheses are the die numbers. Cores from die 262 are approximately an eighth of an inch thick with an O.D. and I.D. of roughly one-fourth and one-eighth of an inch respectively; the dimensions of cores from die 259 are approximately half those from the 262 die. The shrinkage during firing varies with the material used, and so cores from the same die may have different dimensions. The apparatus used to obtain these plots is described in Appendix II. The flux-current curves were taken at low frequency so that they could be assumed to be approximately the static characteristics. Curves taken at high frequency are difficult to interpret and are often ambiguous.

Desirable Flux-Current Characteristics

Several characteristics that are desirable in a switch core are illustrated in figure II-3. One of the most important characteristics is that the slope between points 1 and 2 be negligible so that there will be little change in flux when current in the primary or control windings moves the operating point of the core between points 1 and 2.

Low coercive force, distance 3 in figure II-3, is desirable to keep down the number of ampere-turns needed to drive the core and to keep down the energy dissipated in the core. The energy dissipated in one quasi-static traversal of the flux-current loop is equal to the area of the loop, and so is roughly proportional to the coercive force.

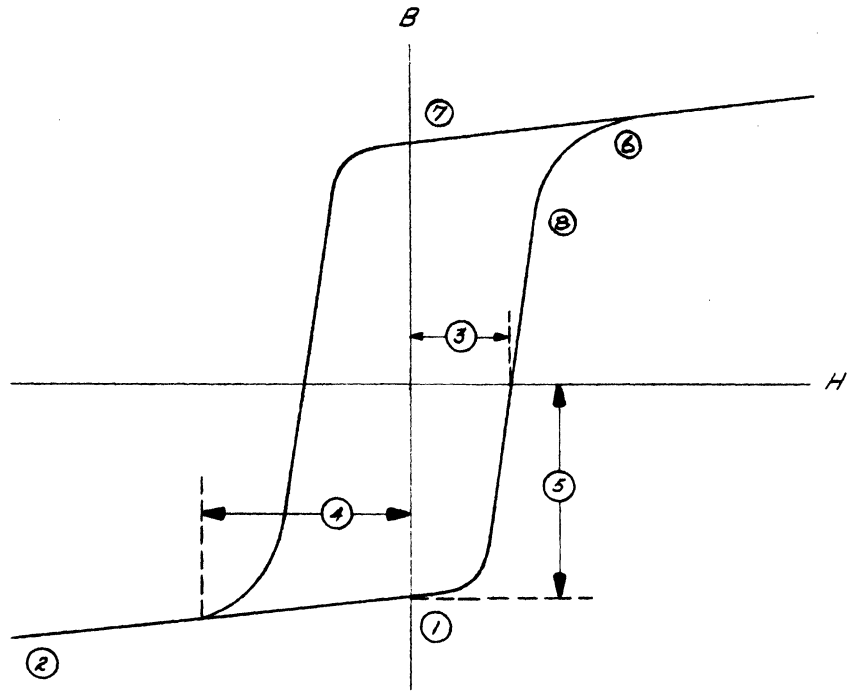


FIG II-3
 A "RECTANGULAR" HYSTERESIS LOOP

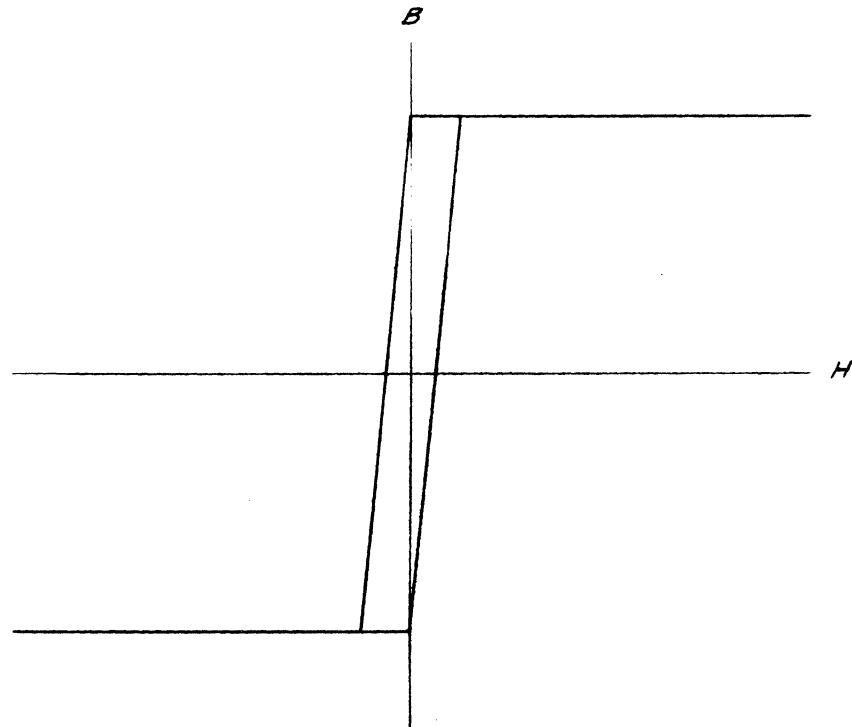


FIG II-4
 AN "IDEAL" SWITCH CORE HYSTERESIS LOOP

Distance 4 in figure II-3 is the current necessary to bring the core from point 7 to point 1. It is usually necessary to have a core start from the same residual point, e.g., point 1, whether it just traversed the loop or whether it came from saturation (point 2). It is desirable to keep this current low so that large tubes are not needed to drive the core.

High residual flux (distance 5) is in general desirable because greater voltage is obtained per turn in the secondary.

Much of the effort spent on rectangular-loop ferrites has been toward developing cores for use in the coincident-current memory where it is necessary that the flux-current curve be flat from point 2 to beyond point 1, and that it then sharply rise to point 6. The ideal switch core is somewhat different as illustrated in figure II-4. Here flux rises immediately after point 1. The MF 1131 core shown in figure II-2 is one of the first to be produced for the switch. The others were made for the memory.

Compensating for Non-Rectangular Loops

Some of the non-rectangular ferrite materials have the desirable characteristics of low coercive force and high permeability. Some experimenting has been done with cores of these materials as saturable transformers, using additional cores to compensate for the non-rectangularity.

Figure II-6 is a schematic of the compensating scheme used. Core B is the saturable transformer used as the switch element, while cores A and C are the compensating elements that cancel the unwanted output produced in B when it is supposed to be cut off. The

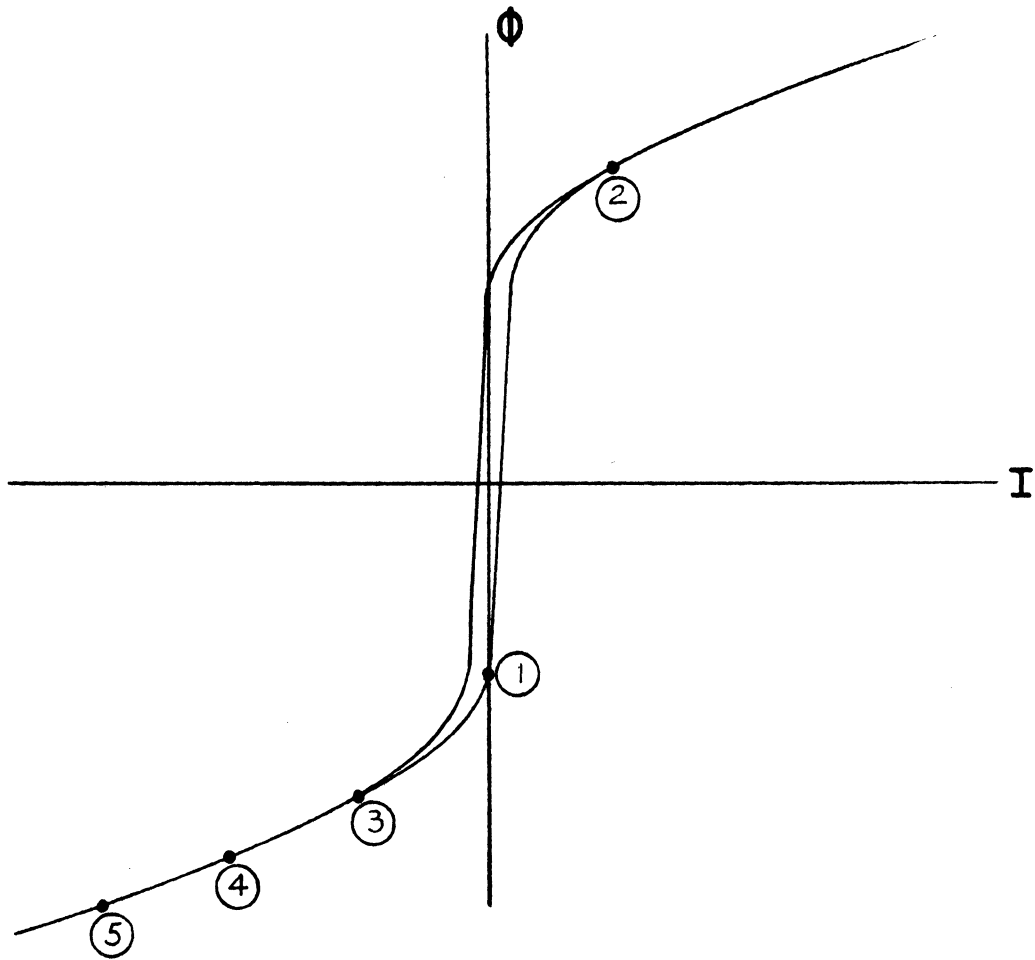


FIG II-5

NON-RECTANGULAR FLUX-CURRENT LOOP

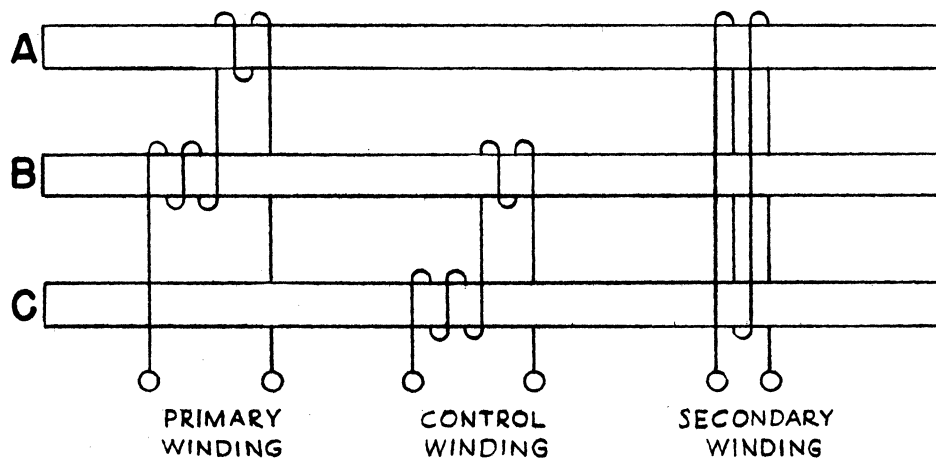


FIG II-6

COMPENSATED SATURABLE TRANSFORMER

three cores have identical flux-current characteristics, as in figure II-5. When core B is biased to point 4 of this figure, it is desired that there be no change in flux when the primary is driven. However, when it is driven, the core moves to point 3 and there is a change in flux. But core A which has been at point 1 is driven also, and it moves to point 3 and produces an opposite change in flux which subtracts from that in core B. Core A also subtracts from core B when core B is not to be cut off and is driven from point 1 to point 2, but the fraction subtracted in this case is small.

An unwanted change in flux is also produced as current in its control winding is changed and core B moves along points 1, 3, 4, and 5. Core C also moves along with B and subtracts an identical change in flux from the output of B.

Although this scheme has made it possible to use non-rectangular material in the switch, it has been rejected because of its complexity. In high-speed circuits, it is important to keep the inductance and capacities of the windings low, but this is very difficult to do with the extra cores and windings.

Unsymmetrical Flux-Current Loops

The switch cores usually start on the saturation ϕ -I loop because they are saturated while being cut-off. However, they are not necessarily driven to saturation in the other direction. For example, the core in figure II-3 may start at point 1, but instead of going all the way to point 6, it might stop in region 8 when the

current is removed. When the core is driven in the other direction, it will traverse a completely different path.

When the rise in current is limited by the external circuitry, this situation can be simulated by superimposing a d-c component on the alternating current being used to plot a Φ -I characteristic. Figure II-7 and figure II-8 are families of Φ -I loops biased with direct current. It can be seen in these plots that the slope of the upper flat portion of the curve is less when the core is driven all the way to saturation than when it is not. One effect of this slope, observed when the core is pulsed, is that the negative over-shoot after the pulse is in proportion to the slope.

Core Geometry and Material

The flux-current characteristic of a core is a function of the geometry of the core and the magnetic characteristics of the material from which it is made. At the present time, it is difficult to design a ferrite core by using the characteristics of a material as observed in another core because the characteristics of ferrite material seem to be dependent upon the geometry of the die in which the cores are formed. Design is further complicated by the fact that the characteristics of the material are not uniform across a section of a core. However, the general characteristics of a core and certain limitations in these characteristics can be found by consideration of the effect of geometry on a core using an idealized, uniform material characteristic. It is possible to show a simple relationship between the geometry and material characteristics on the most

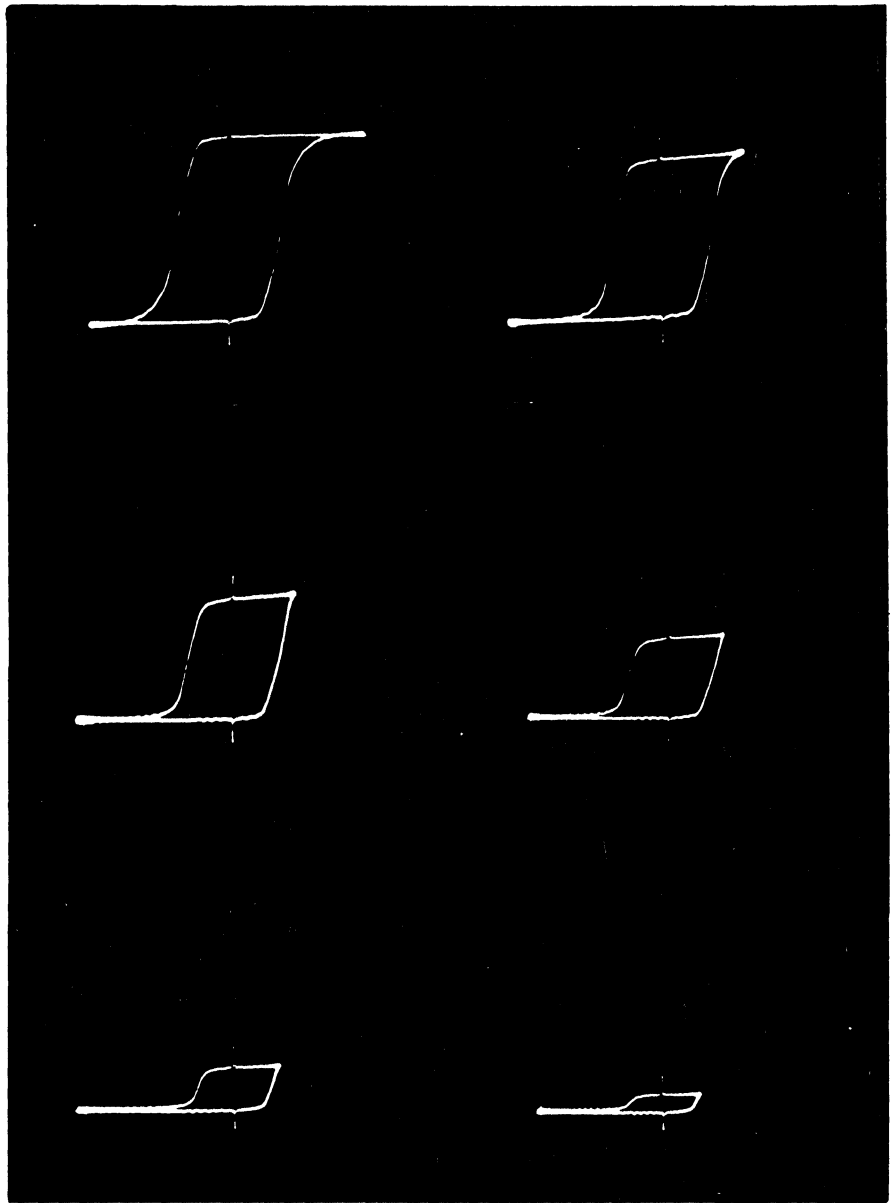


FIG. II-7
FLUX-CURRENT CURVES OF MF1118(259)
WITH D.C. SUPERIMPOSED

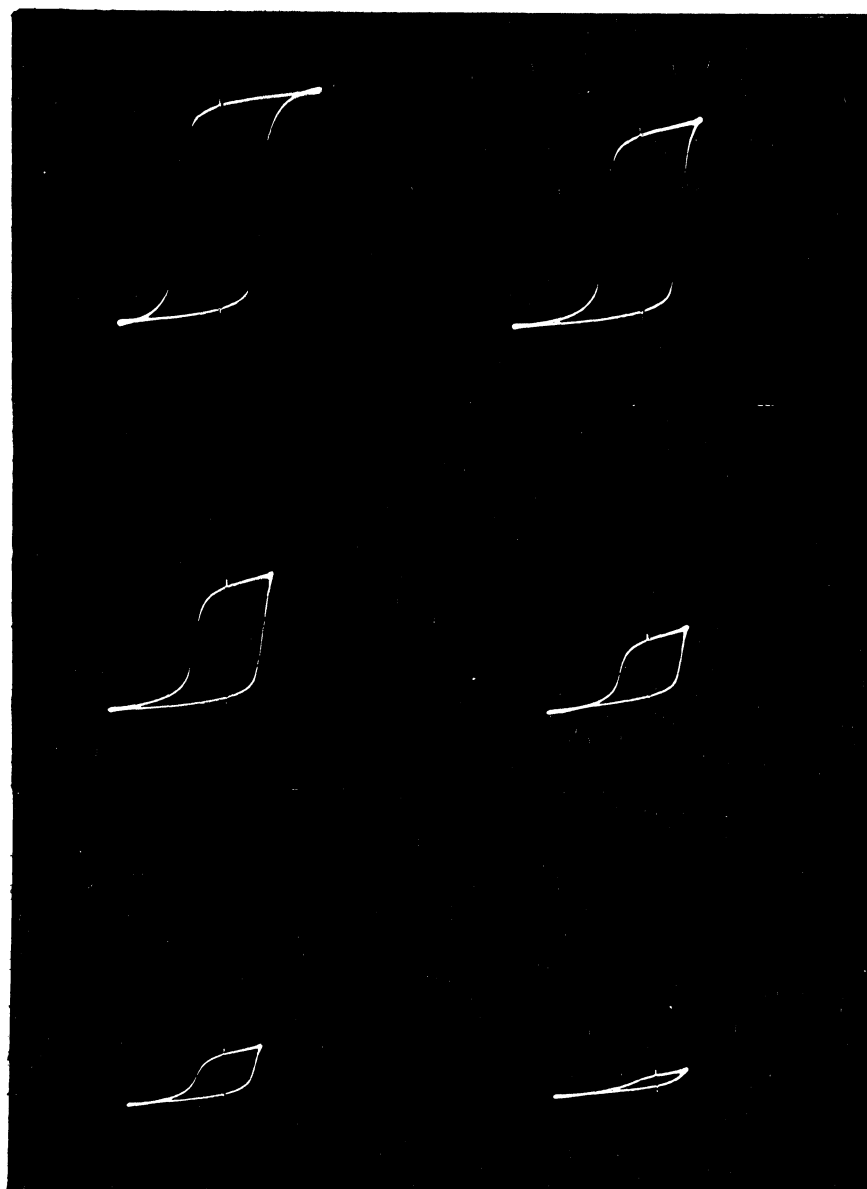
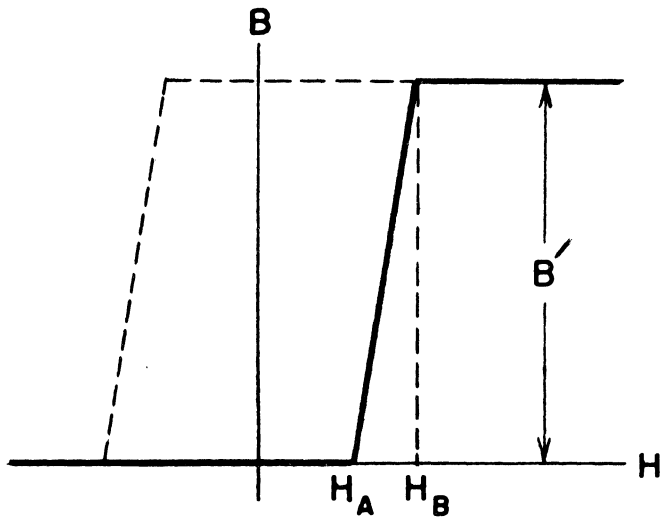
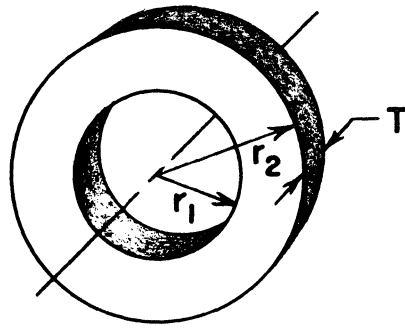


FIG. II-8
FLUX-CURRENT CURVES OF MF1131(262)
WITH D.C. SUPERIMPOSED

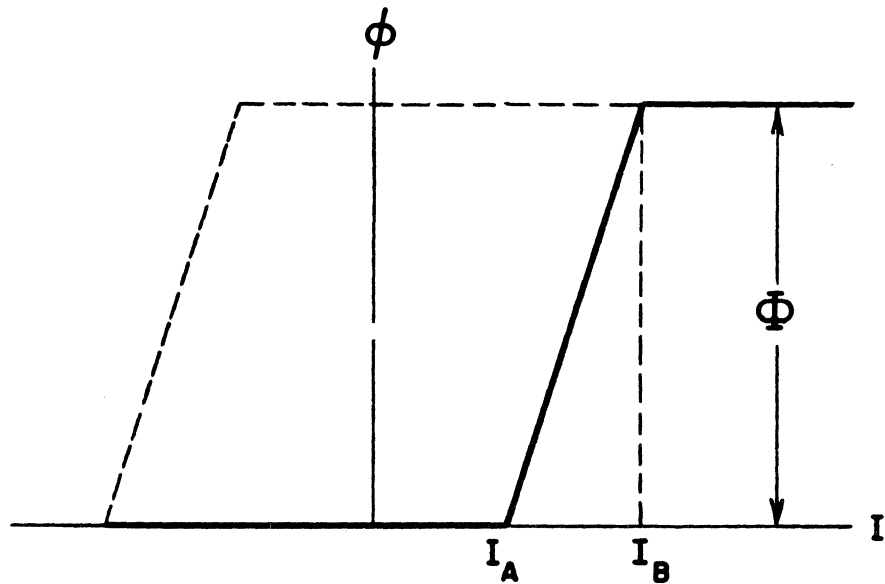
pertinent points of the flux-current characteristic of a core.

The magnetic characteristics of a material are given in the form of B-H curves where B, the flux density, is plotted versus H, the magnetic intensity. In a toroidal core of high permeability, the H within the core may be considered symmetrical about the center of the core even if the windings do not pass through the center. When this assumption is made, H at any point in the core is equal to the ampere-turns of the winding divided by the circumference of the core at that point. When H is determined at all points in the core, B can be found from the B-H curve. To find the total flux in the core, the B is integrated across the cross-sectional area of the core. In general, this is a difficult procedure because the B-H curve is multivalued, but in the matrix switch, we are usually interested in only the saturation B-H curve.

If we consider the toroid in figure II-9, which is made of material with the idealized B-H characteristic shown, several pertinent facts about the saturation flux-current curve are readily observed. The lower saturation values of B and flux have been arbitrarily defined as being zero in the curves shown here. If the B of all the material in the toroid is initially at zero, the flux is also at zero. As current is increased from zero, flux first starts to change when H at the inside radius r_1 , of the core reaches the value H_A . This fixes the value of I_A to $\frac{2\pi r_1 H_A}{N_1}$ where N_1 is the number of turns on the winding. The last change of flux occurs when H_B at the outside radius, r_2 , reaches the value H_B . This fixes I_B to $\frac{2\pi r_2 H_B}{N_1}$. All the



SIMPLIFIED B-H CHARACTERISTIC



SIMPLIFIED ϕ I CHARACTERISTIC

FIG. II-9

B-H & ϕ -I CHARACTERISTICS

material will have changed in flux density, a quantity B'_L . The total change in flux is B' times the cross-sectional area of the core.

An Equivalent Circuit of a Saturable-Core Transformer

An equivalent circuit will be presented that has been found useful in approximating the design of a switch and giving direction to the "cut and try" development. In its present form, the equivalent circuit does not take into account the eddy-current losses or other time-dependent losses within the core, but in the ferrites these are not large at the speeds used in this work. Leakage inductance and stray capacitances are also assumed to be negligible.

When the flux-current characteristic of a core can be approximated by the simplified curve of figure II-10, the equivalent circuit of the core, during the change of flux as I_1 is increased from zero, is simply an inductance, $L_m = \frac{\Phi N_1}{I_B - I_A}$, shunted by a current source of magnitude I_A . Before current reaches I_A and after it reaches I_B , the equivalent is a simple short circuit.

The equivalent of a vacuum tube that drives the core can usually be assumed to be a current source equal to the direct current of the tube shunted by a resistor equal to its plate resistance. The equivalent circuit of a tube and core is shown at the top of figure II-11. This can be simplified to the simple series L-R circuit shown in this figure where $E_o' = \frac{I_o - I_A}{R_1}$. When a step

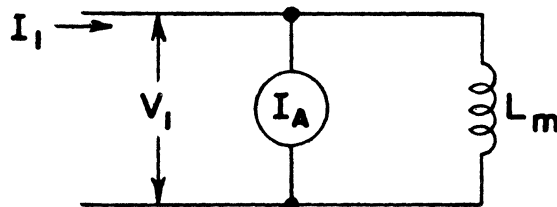
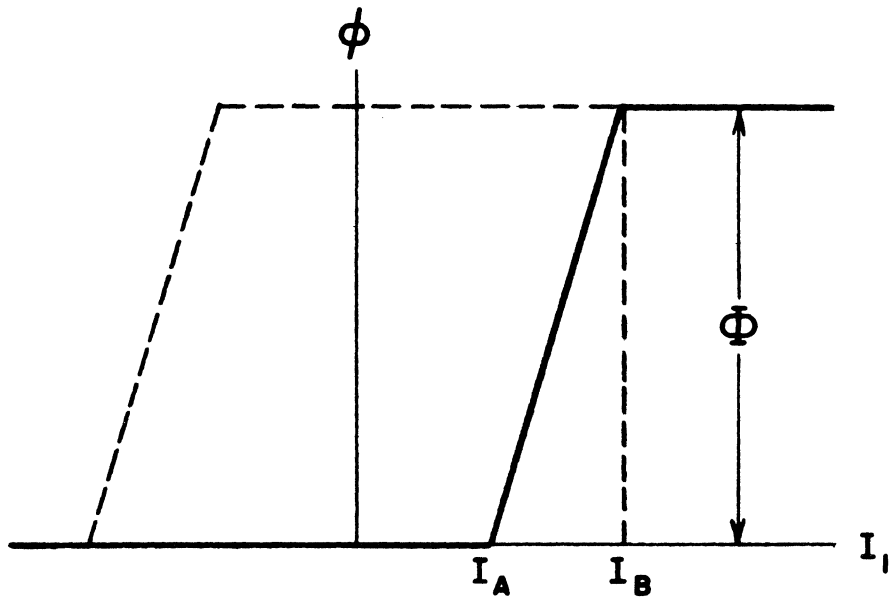
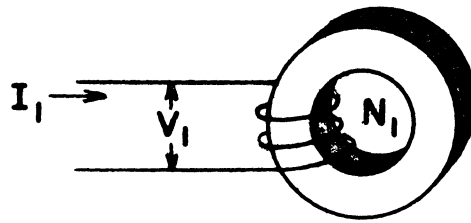
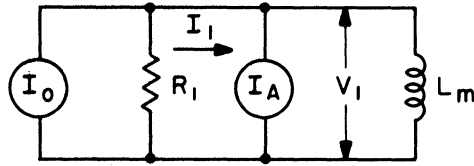
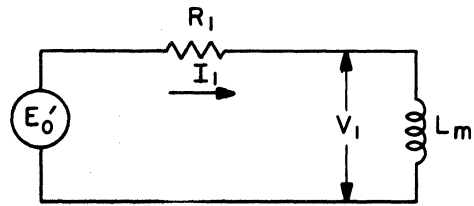


FIG. II - 10

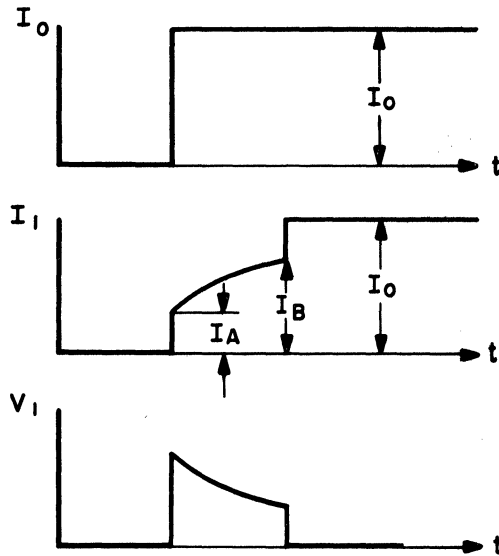
EQUIVALENT CIRCUIT OF CORE



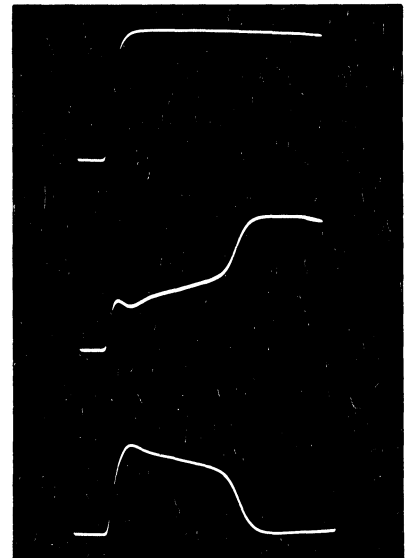
EQUIVALENT OF CORE AND VACUUM TUBE DRIVER



SIMPLIFIED EQUIVALENT



RESPONSE OF EQUIVALENT



RESPONSE OF AN ACTUAL CORE

FIG. II - II

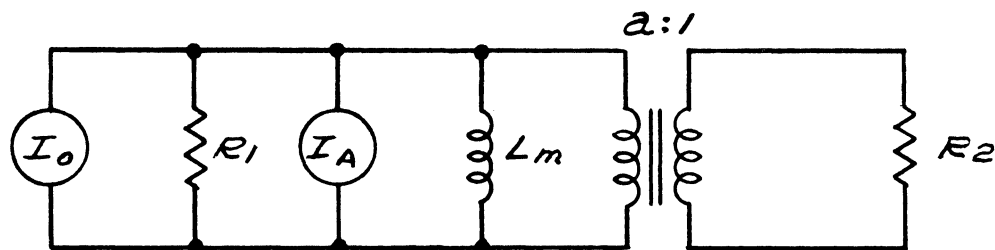
RESPONSE OF A CORE TO A STEP OF CURRENT

of current is applied, the core at first acts as a short circuit and the current in the core immediately rises to I_A . Then this equivalent circuit becomes valid and further current rise is limited to an exponential increase by the back voltage of the core. But when I_B is reached, the core again becomes a short circuit and the current increases immediately to I_0 as shown in the plots of figure II-11.

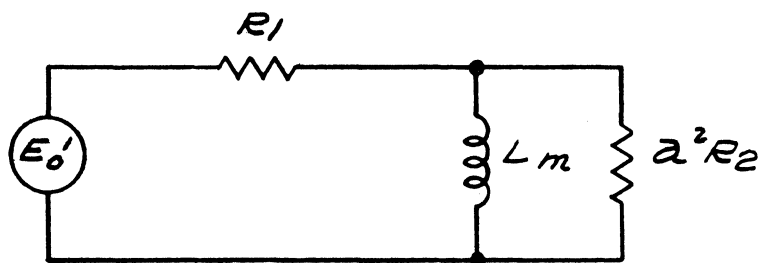
If the core has a secondary loaded by a resistor, an idealized equivalent circuit is the inductance, L_m , and current source, I_A , shunted by an ideal transformer with the same turns ratio and followed by the resistor. As shown in figure II-12, this equivalent can be simplified by taking out the transformer and multiplying the value of the resistor in the secondary by the turns ratio squared. The current source I_A can be removed as before and included in E_0' . This can be further simplified to the third circuit of figure II-12 by Thevenin's theorem. The resulting circuit has the same response as that of figure II-11.

This equivalent can be expanded to the case where there is inductance in series with the resistor in the secondary (see figure II-13). When this is simplified, a two-loop network results that is not difficult to solve¹, but its solution is not easily interpreted in terms of the transformer parameters. Because L_m will usually

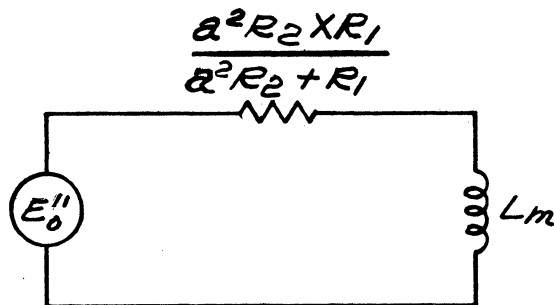
1 Superscripts refer to similarly numbered entries in the Bibliography.



EQUIVALENT CIRCUIT

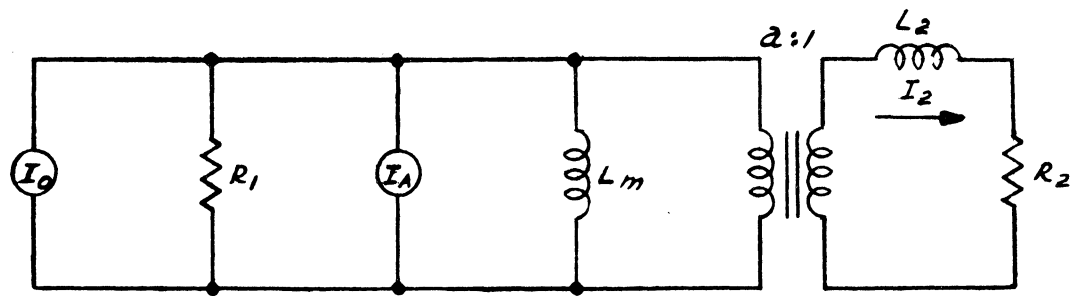


SIMPLIFIED EQUIVALENT

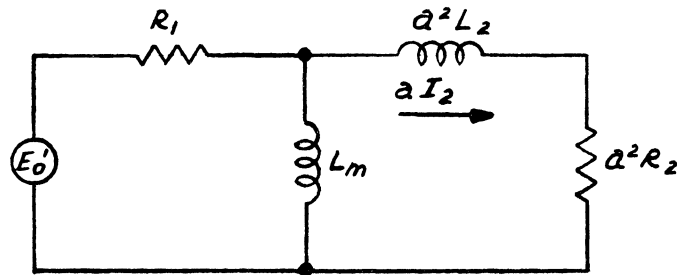


FURTHER SIMPLIFIED EQUIVALENT

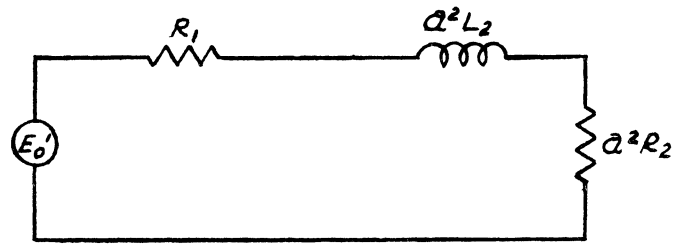
FIG. II-12
EQUIVALENT OF CORE
WITH RESISTOR ACROSS SECONDARY



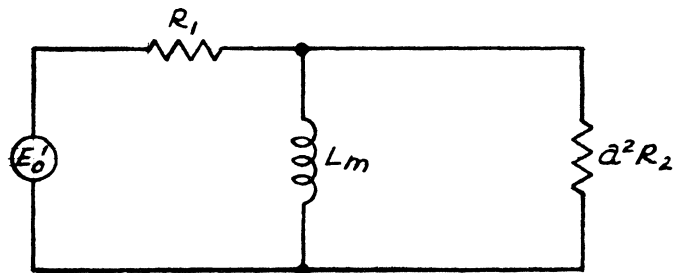
EQUIVALENT CIRCUIT



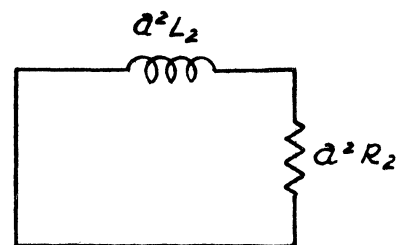
SIMPLIFIED EQUIVALENT



CASE I



CASE II



CASE III

FIG. II-13

EQUIVALENT OF CORE WITH RESISTOR
AND INDUCTANCE ACROSS SECONDARY

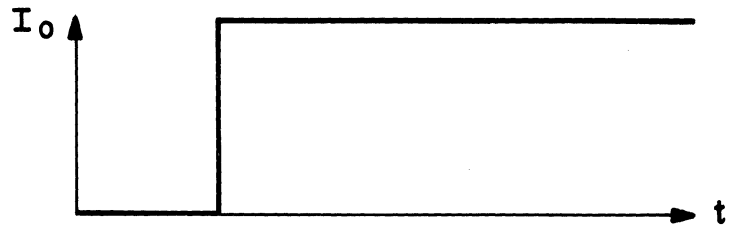
be greater than a^2L_2 , the response to this circuit can be divided into two cases each involving only a simple L-R circuit. When a step of current is first applied, L_m can be considered negligible as in Case I of figure II-13. The current I_2 will rise with an exponential time constant equal to $\frac{a^2L_2}{R_1+a^2R_2}$. After this rise of current is well underway, a^2L_2 can be considered negligible, and case II will be valid. Here I_2 will decrease with an exponential time constant of $\frac{L_m(R_1+a^2R_2)}{R_1 \times a^2R_2}$ until the core saturates, at which time L_m will be a short circuit.

When L_m becomes a short circuit, a third case becomes valid. The current flowing at the time of saturation will decay with a third time constant equal to a^2L_2/a^2R_2 . I_2 for the complete circuit will be a combination of the responses of the three cases as illustrated in figure II-14.

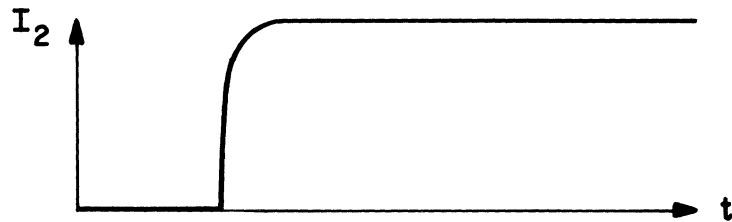
"Transmission-Line Effect"

When several windings are connected in series as in the matrix switch, the inductance of the windings and their capacity to ground are, in effect, a lumped-parameter transmission line. If care is not taken in the design of the switch, the delay that a step of current will suffer in progressing the length of the switch may be significant. For example, if sixteen windings, each with an inductance of only 10 microhenries and a capacity of only 10 micromicrofarads, are placed in series, there will be a delay of 0.16 microsecond in the windings.

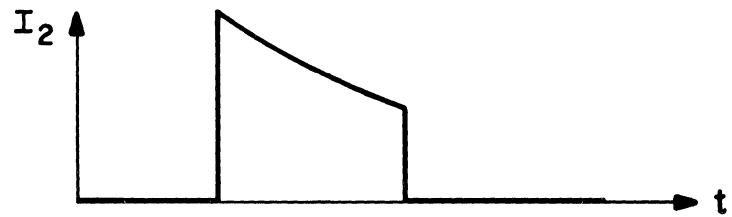
This effect can cause several difficulties in applying the matrix switch to a problem. In some applications, such as where



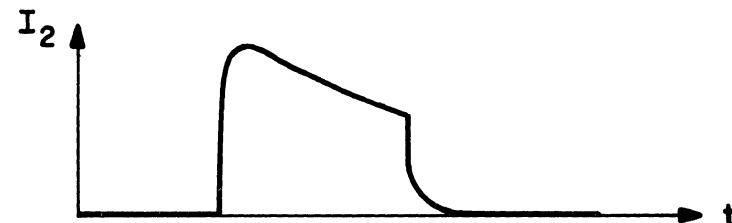
CURRENT STEP APPLIED



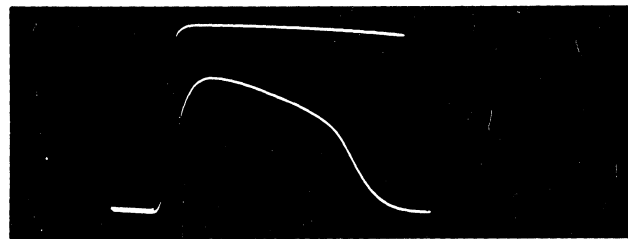
RESPONSE TO CASE I



RESPONSE TO CASE II



RESPONSE OF COMPLETE CIRCUIT



RESPONSE OF AN ACTUAL CIRCUIT

FIG. II-14

RESPONSE OF CIRCUIT OF FIG. II-13

the switch is to drive a coincident-current magnetic memory, the delay between the outputs of different positions of the switch cannot be tolerated. The reflections produced in the transmission line, may also cause spurious effects within the switch. A third factor to be considered is the loading that the transmission line puts on the control windings of the selected transformer in a switch. The control windings are effectively secondaries which drive transmission lines while the transformer is being switched.

CHAPTER III A BRIEF DESCRIPTION OF THE COINCIDENT-CURRENT MEMORY

The application of the magnetic matrix switch to be considered in this research and the application for which the switch was developed is the driving of a coincident-current memory. The general aspects of the memory have been presented in the literature 2, 3, 4, 5, 6 and , and so will not be discussed in detail here.

The memory is made up of many tiny rectangular-loop ferromagnetic cores -- one for each binary digit. Figure III-1 is a photograph of the flux-current loop of an actual memory core. This loop, which is one of the minor hysteresis loops of the core, is shown superimposed on the saturation loop in the corner of this photograph. If the residual flux in the core is in one direction, for example, the lower position on this curve, it is defined as holding a ONE. If it is in the other direction, it is defined as holding a ZERO. To sense or "read" a core it is driven to the ZERO position by a positive current pulse. If the core held a ONE, the change in flux develops a voltage in a sensing winding. If it were already in the ZERO position, no voltage will be developed in the sensing winding.

The selection scheme depends upon the fact that a current I_m will change the direction of flux but a current of $I_m/2$ will not. Figure III-2 shows how these cores are wired into an array. To select a core in the array, half the current is supplied from the row and half from the column that passes through the core. These add in the

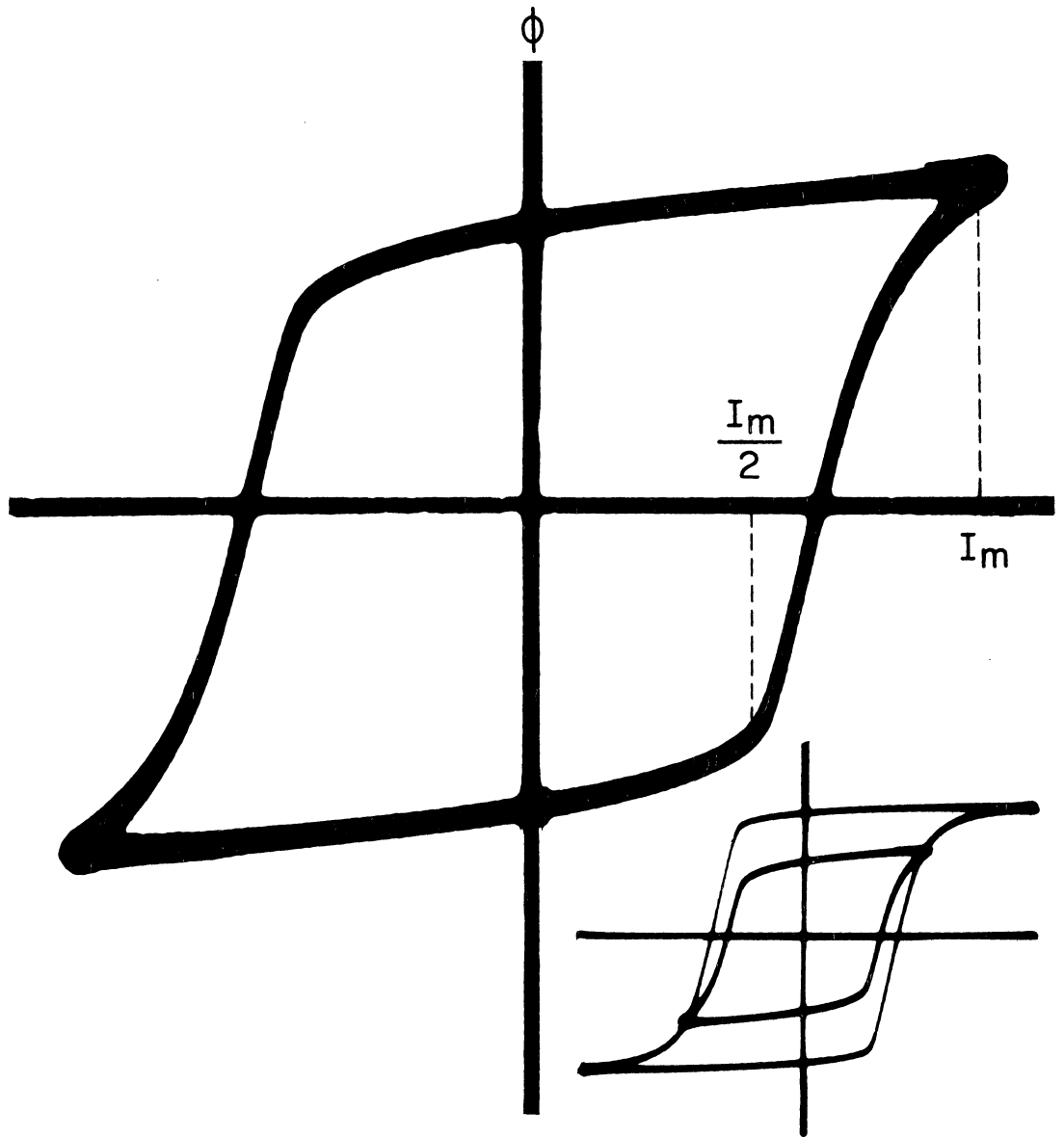


FIG. III-1

ϕ -I LOOP FERRAMIC III8 (259)

A-51527

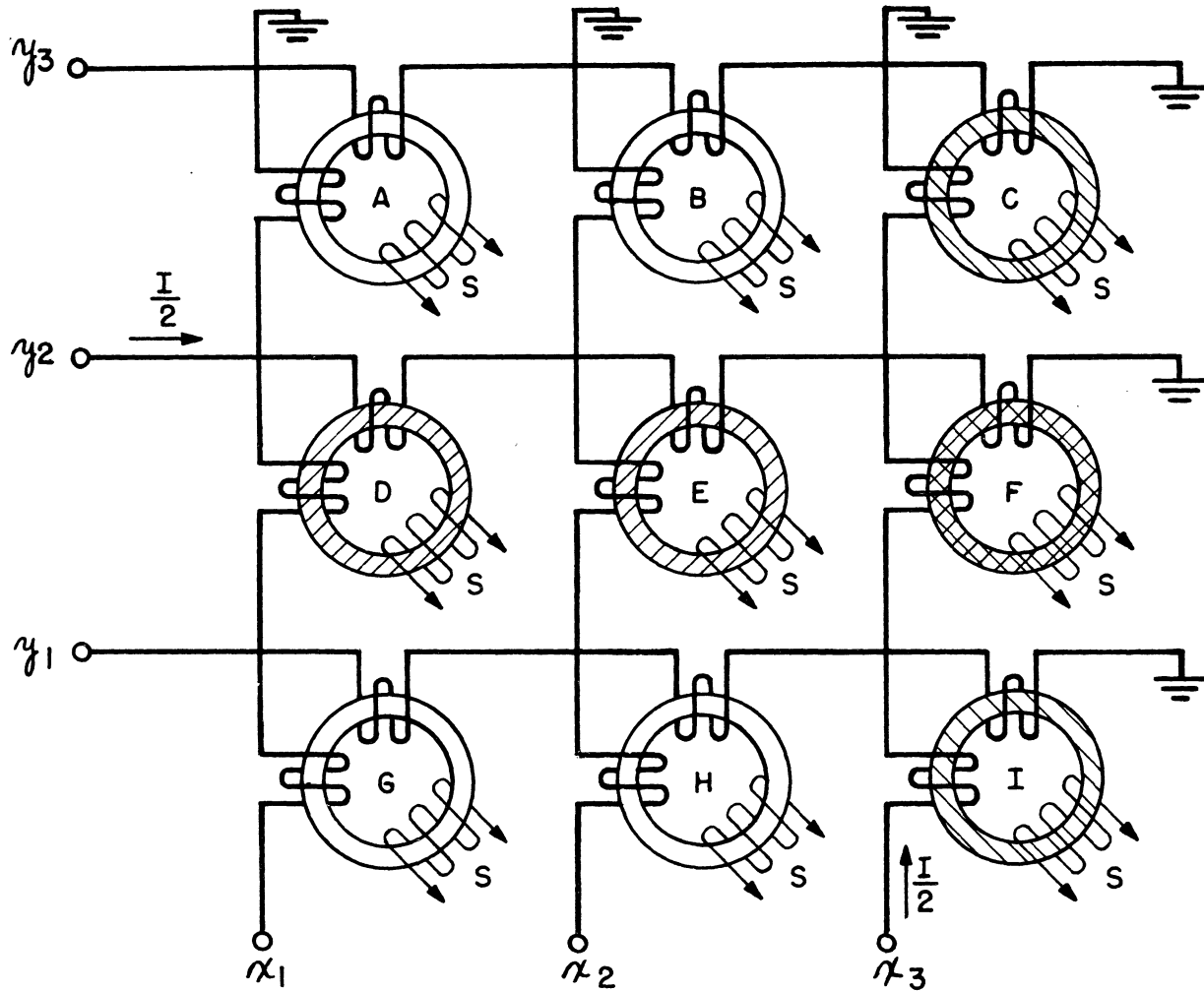


FIG. III-2

A TWO-DIMENSIONAL ARRAY OF CORES

selected core and switch the direction of flux, but the current from one coordinate alone is not enough to change the flux in the non-selected cores. For example, to select core "F", $I_m / 2$ is supplied by line Y_2 and $I_m / 2$ by line X_3 . The magnetomotive force due to each of these adds at core "F" and the core switches flux direction. Cores "C", "D", "E", and "I" see only a current of $I_m / 2$ which is not enough to switch the core.

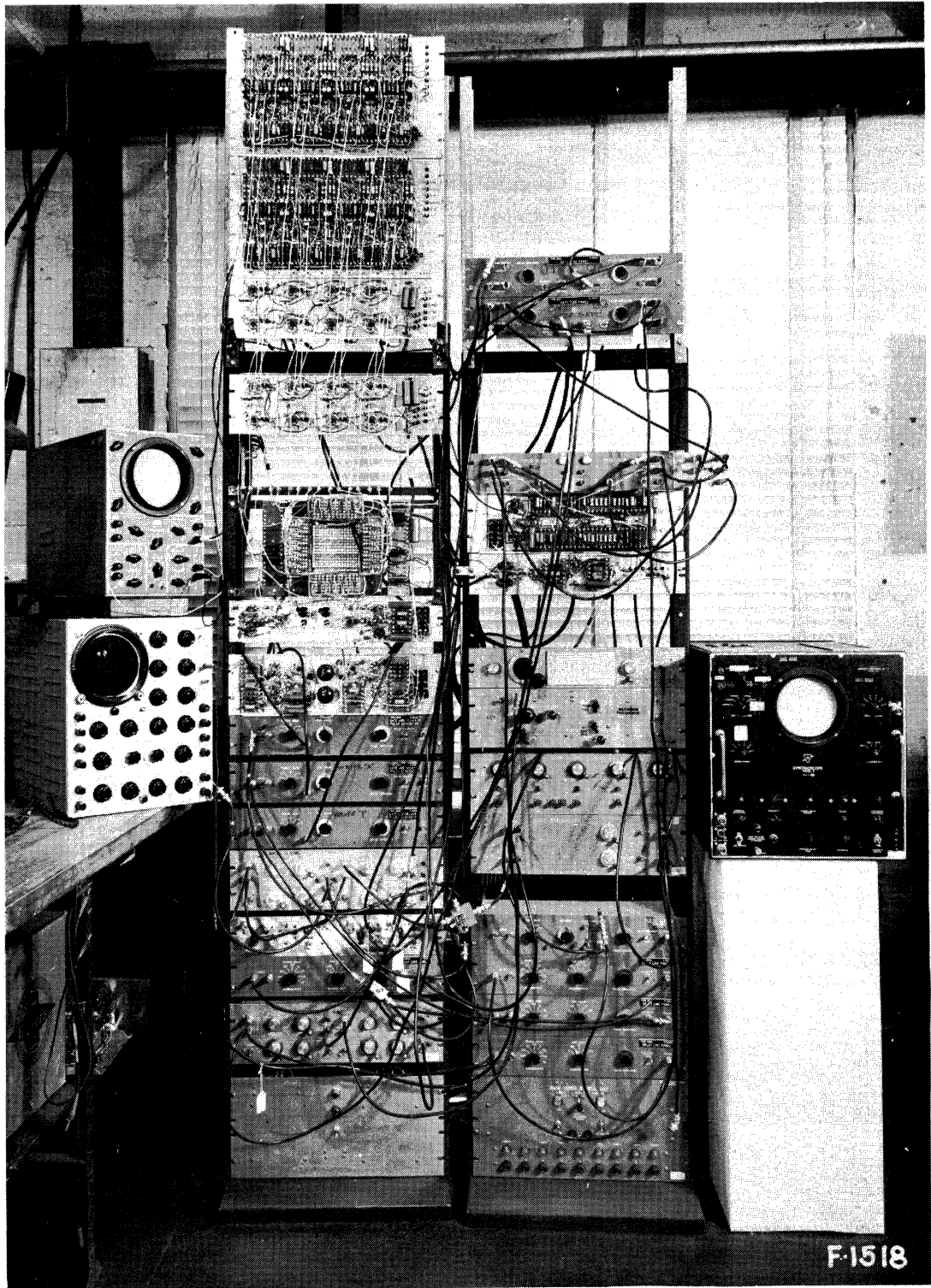
One of the features of this memory is the straightforward method by which the memory units are selected. There remains, however, a switching problem involving the selection of one line along each coordinate and driving current first in one direction to read and then in the other to write. This can be done with a crystal-matrix switch followed by hard tubes, but the large numbers of heavy tubes necessary make this rather awkward and expensive. To drive a two-dimensional array, one would need two crystal-matrix switches, one for each coordinate, plus two hard tubes for each switch output. For a 16 x 16 array, this would mean 128 crystal diodes and 64 hard tubes. The magnetic matrix switch is a more straightforward solution to this problem in that it eliminates the need for the large numbers of crystals and hard tubes.

CHAPTER IV AN EXPERIMENTAL MEMORY AND SWITCH

In the course of this research, two memory arrays with their associated selecting and logical-testing apparatus were assembled. On the basis of the experience gained in the design and operation of the first array, a second array was assembled which eliminated several of the weaknesses inherent in the original design. In this report only the second array and its test system will be discussed in detail, while the first array will be mentioned only in indicating the reasons for certain design decisions. Photographs of both arrays are included, with figure IV-1 and IV-2 being those of the first array, and figures IV-3 and IV-4 those of the second array.

Construction of the Memory

Each of the windings on the memory cores consists of only a single turn (i.e., one wire passing through a core). The coordinate lines of the memory from a grid of wires, as can be seen in the close-up views of the two arrays. The sensing winding is run through the array diagonally to make the outputs from alternate cores in opposite directions so that spurious signals from the cores will tend to cancel. In some systems, it is desirable to have a Z-axis winding, common to the whole array, which can be used to write "ZERO's" into the memory or can be used in one of several redundant selection schemes.



A-51515

F-1518

FIG. IV-1
CERAMIC MEMORY ARRAY I

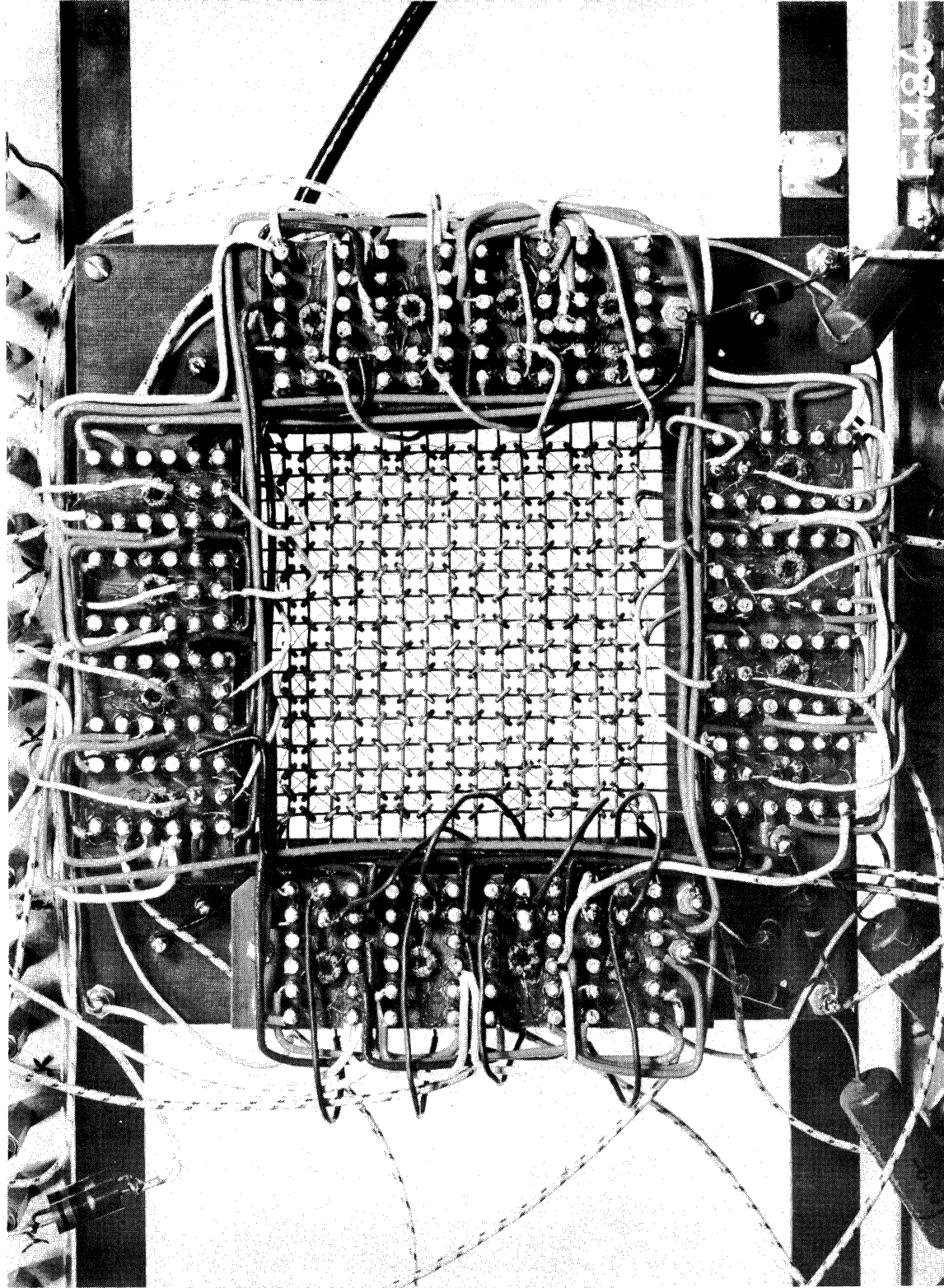
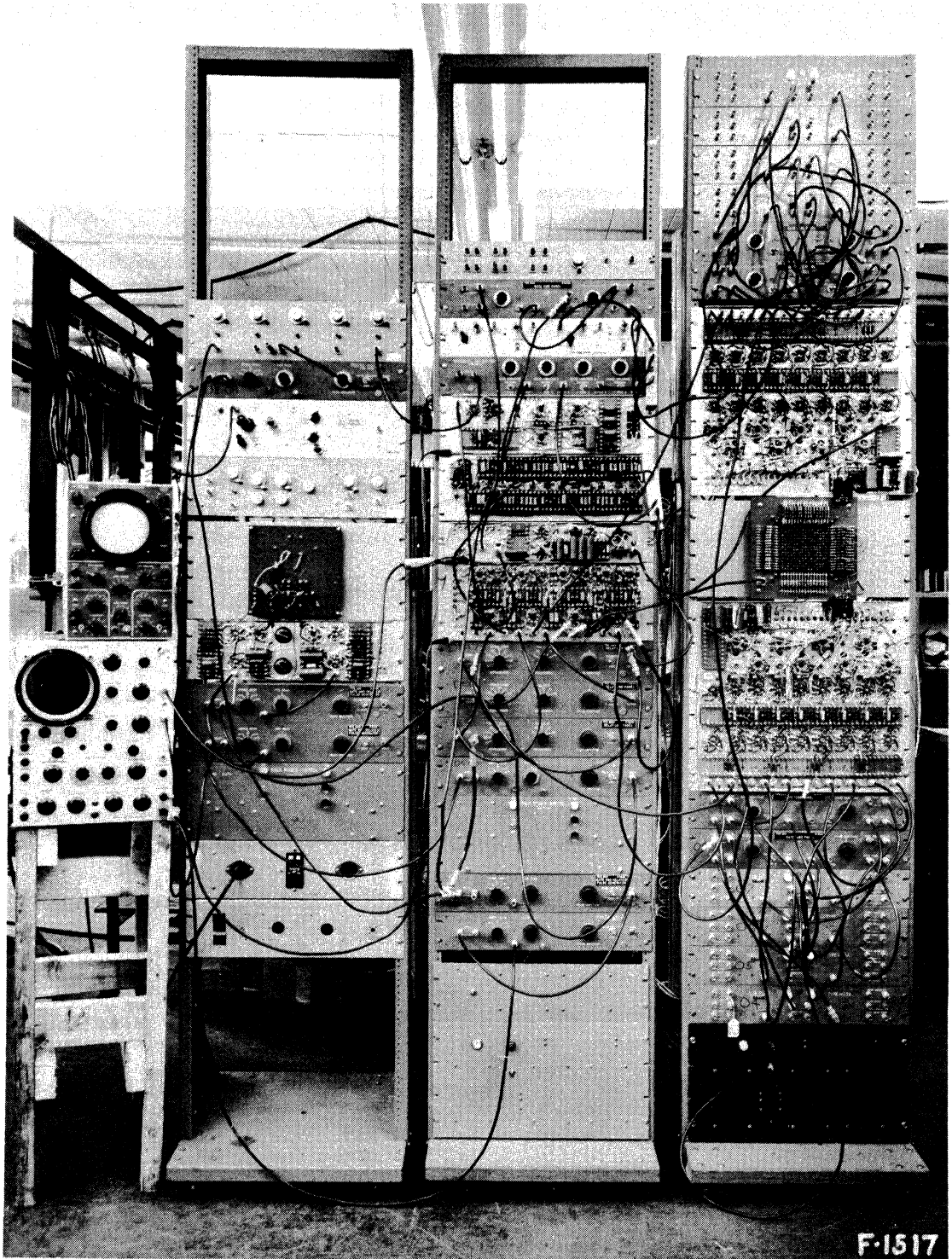


FIG. IV - 2
CLOSE-UP OF CERAMIC MEMORY I



A-51516

F-1517

FIG. IV-3
CERAMIC MEMORY ARRAY II



A-51529

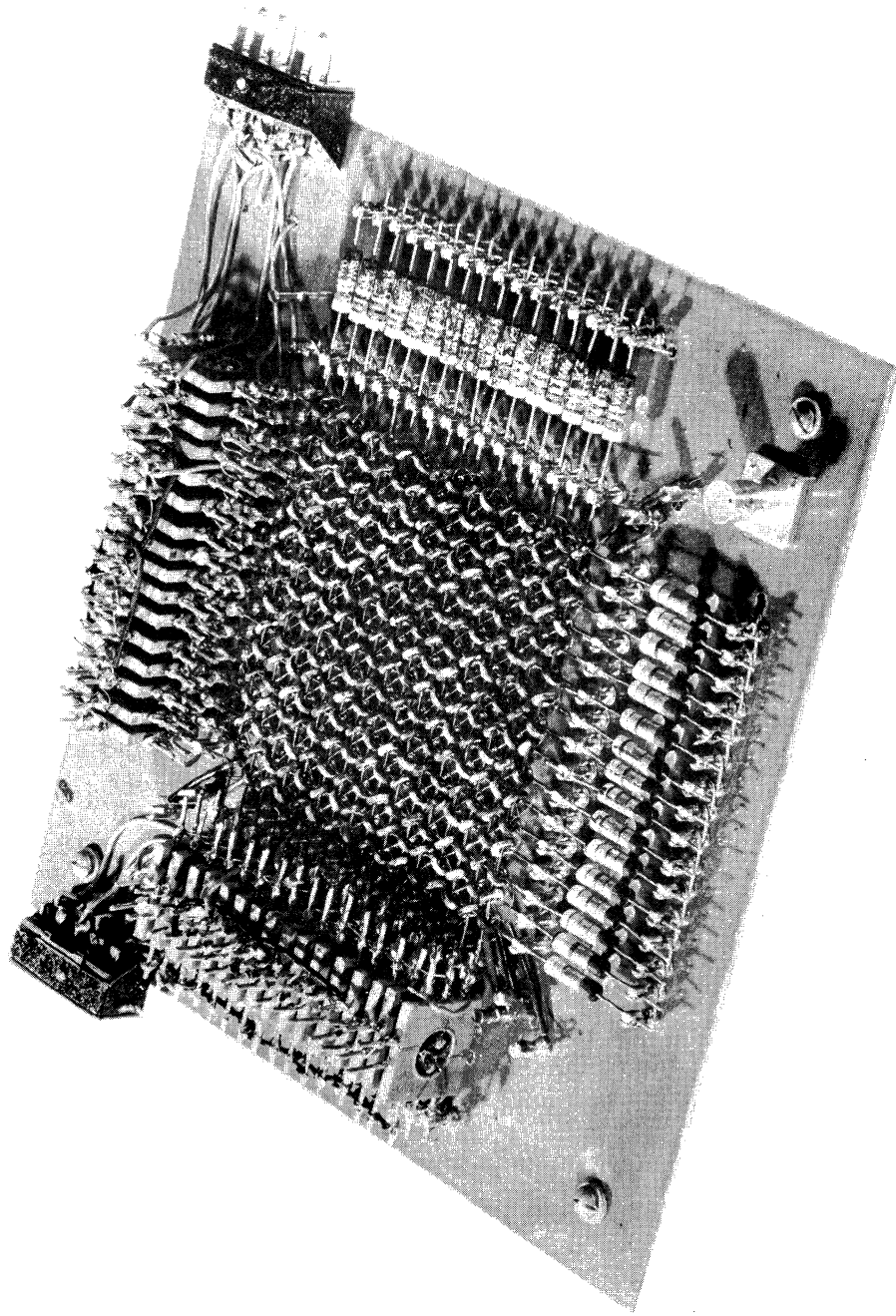


FIG. IV - 4
CLOSEUP OF CERAMIC ARRAY II

Figure IV-5 is a schematic representation of a memory array without the Z-axis winding. One end of all the coordinate lines is grounded so that they will help shield the sensing winding from external fields. There is no direct return between the terminals of each switch transformer, but current goes down the one selected coordinate line of the memory and returns through all the others. There is less inductance in this multiple return than in a single return and construction of the memory is simplified.

The memory with the Z-axis winding shown in figure IV-6 is much the same, but the direction of the current in alternate lines is reversed so that the Z winding can be made continuous. The switch terminals here are on opposite sides of the memory to show that the current directions are reversed, but it is not necessary to arrange the memory in this way. The sensing winding becomes more complicated in this scheme, but the length of the winding is not much greater than in the first scheme. Figures IV-7 and IV-8 are photographs of arrays corresponding to figures IV-5 and IV-6.

Design and Construction of the Switch

In designing the switch, the equivalent circuit of figure II-13 was considered to represent one of the saturable transformers. The inductance of the memory, which is approximately 0.4 microhenries, is represented by L_2 and the terminating resistor is represented by R . The secondary current is fixed by the characteristics

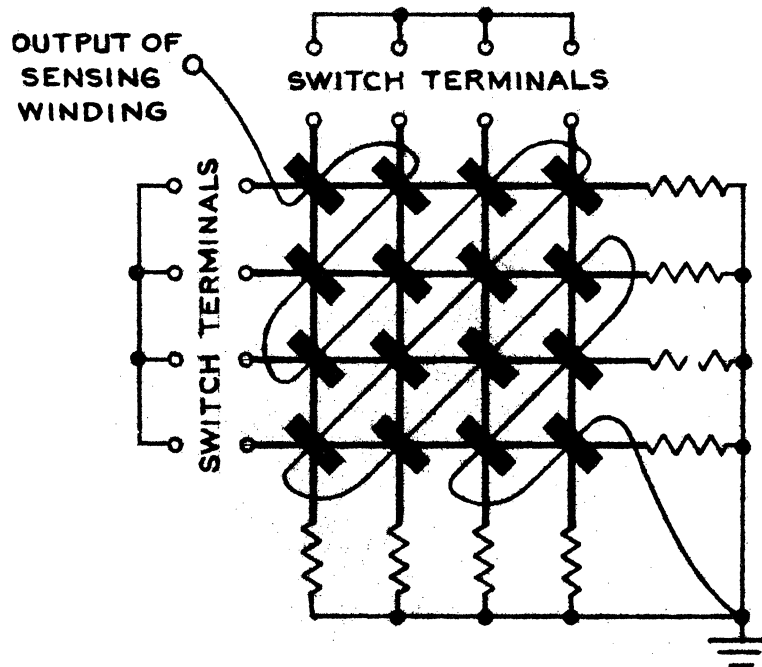


FIG IV-5

A MEMORY ARRAY WITHOUT Z AXIS WINDING

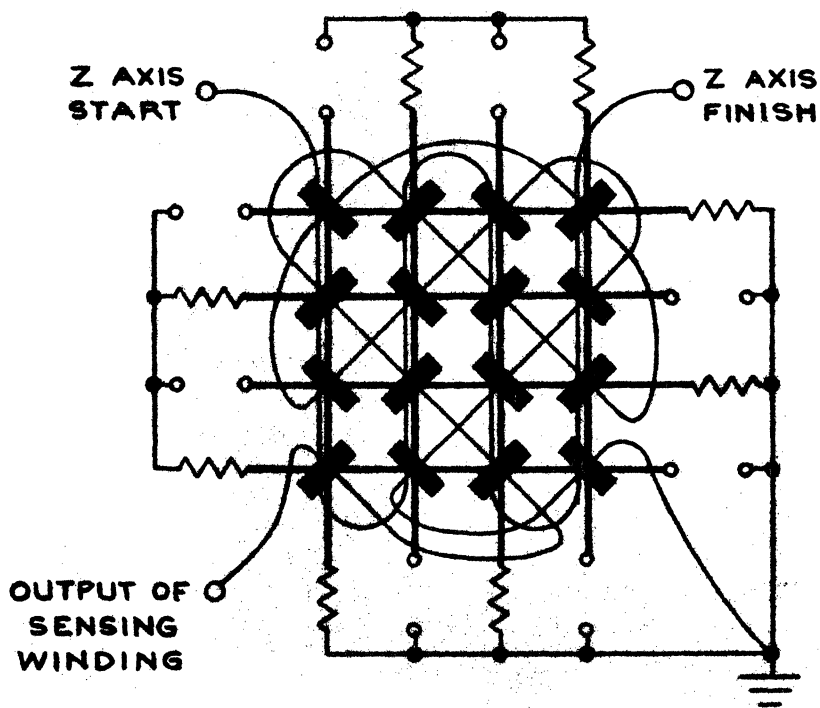


FIG IV-6

A MEMORY ARRAY WITH Z AXIS WINDING

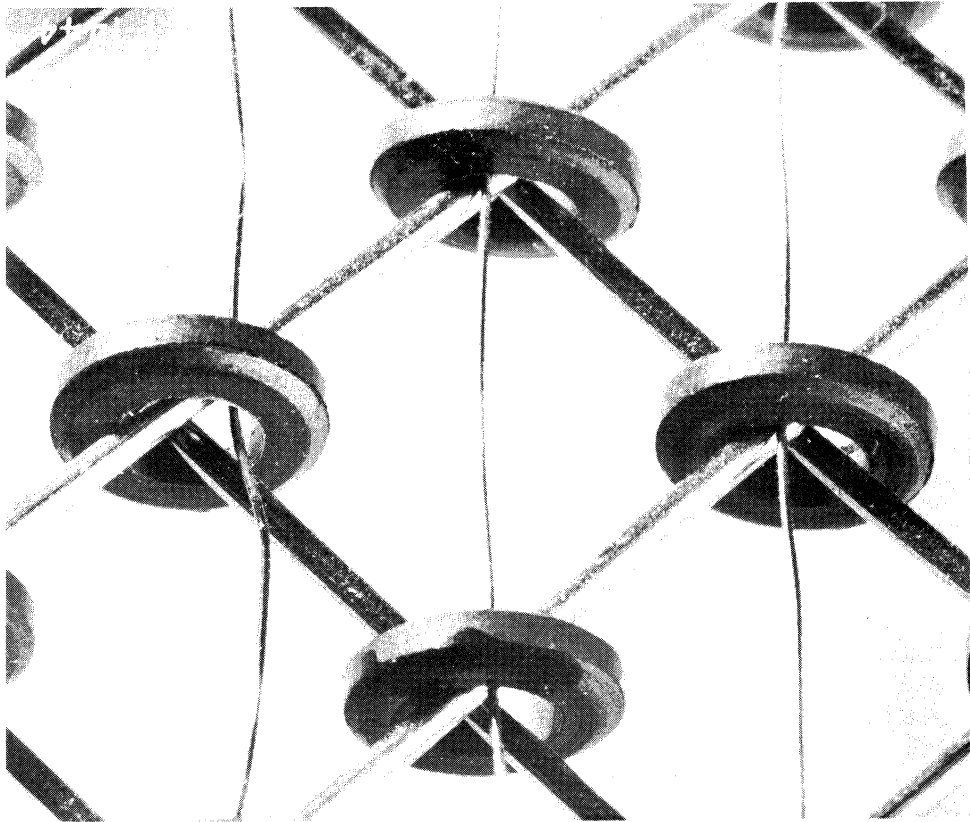


FIG. IV-7
MEMORY WITHOUT Z WINDING

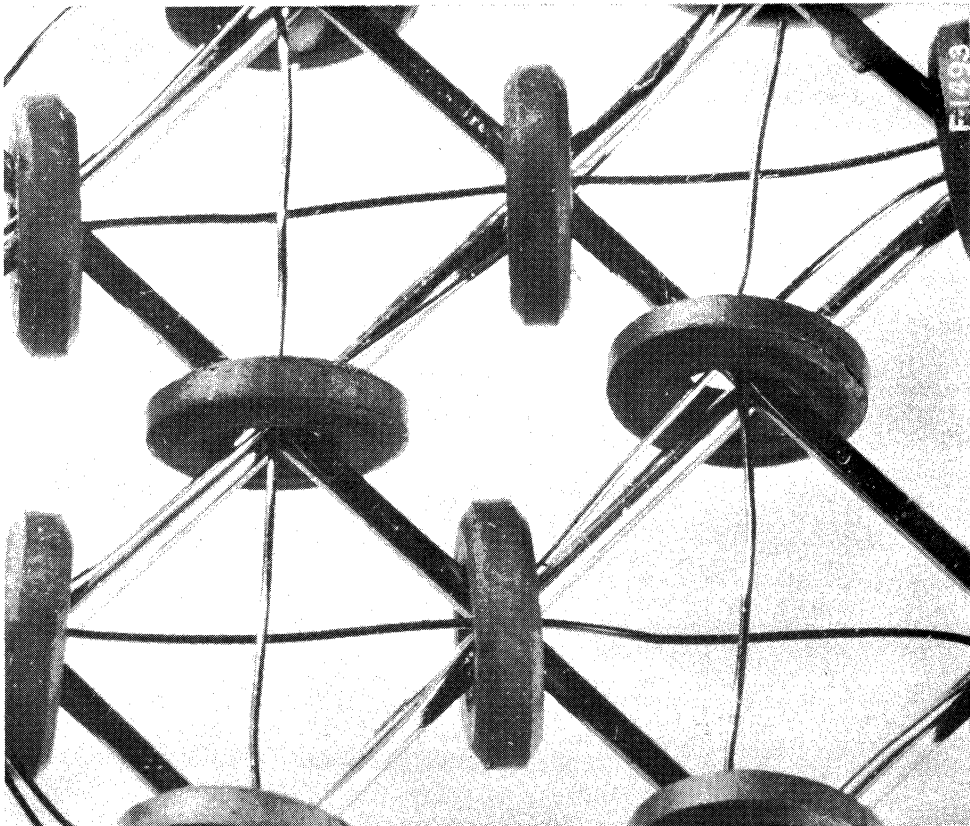


FIG. IV-8
MEMORY WITH Z WINDING

A-51465
F-1493
F-1444

of the cores used in the memory. It was found, by testing individual memory cores, that a rectangular pulse 1.5 amperes in amplitude and at least 0.7 microseconds in length gave the best ONE-to-ZERO signal ratio. The amplitude of the current source was fixed at about 400 milliamperes because this is the most that can be obtained conveniently from receiving type vacuum tubes. R_p , the plate resistance of the driver tube, is about 3000-ohms for a 6CD6.

MF 1131 (262) cores were used because, of those available at this time, they have the most nearly ideal Φ -I loop for the switch application. This can be seen from the plots in figure II-2. Because the output pulse should be rectangular, L_m was made large by putting many turns on the primary. 20 turns of number 36 enameled wire was found to be the most that could be put conveniently on a core and the winding still be kept uniform. The "transmission line effect" was kept to a minimum by bunching the windings so that the interwinding capacity is low. The number of secondary turns and the value of the terminating resistor were picked so that most of the flux of the core is switched during a one microsecond pulse. The terminating resistor was adjusted experimentally when the switches were connected to the memory.

The mechanical design of the switch presents a significant problem. As can be seen in figure IV-2, the mounting of the saturable-core transformers is difficult because of the large number of windings to be terminated at each transformer. Figure IV-9 is a cross-section of

A-51528

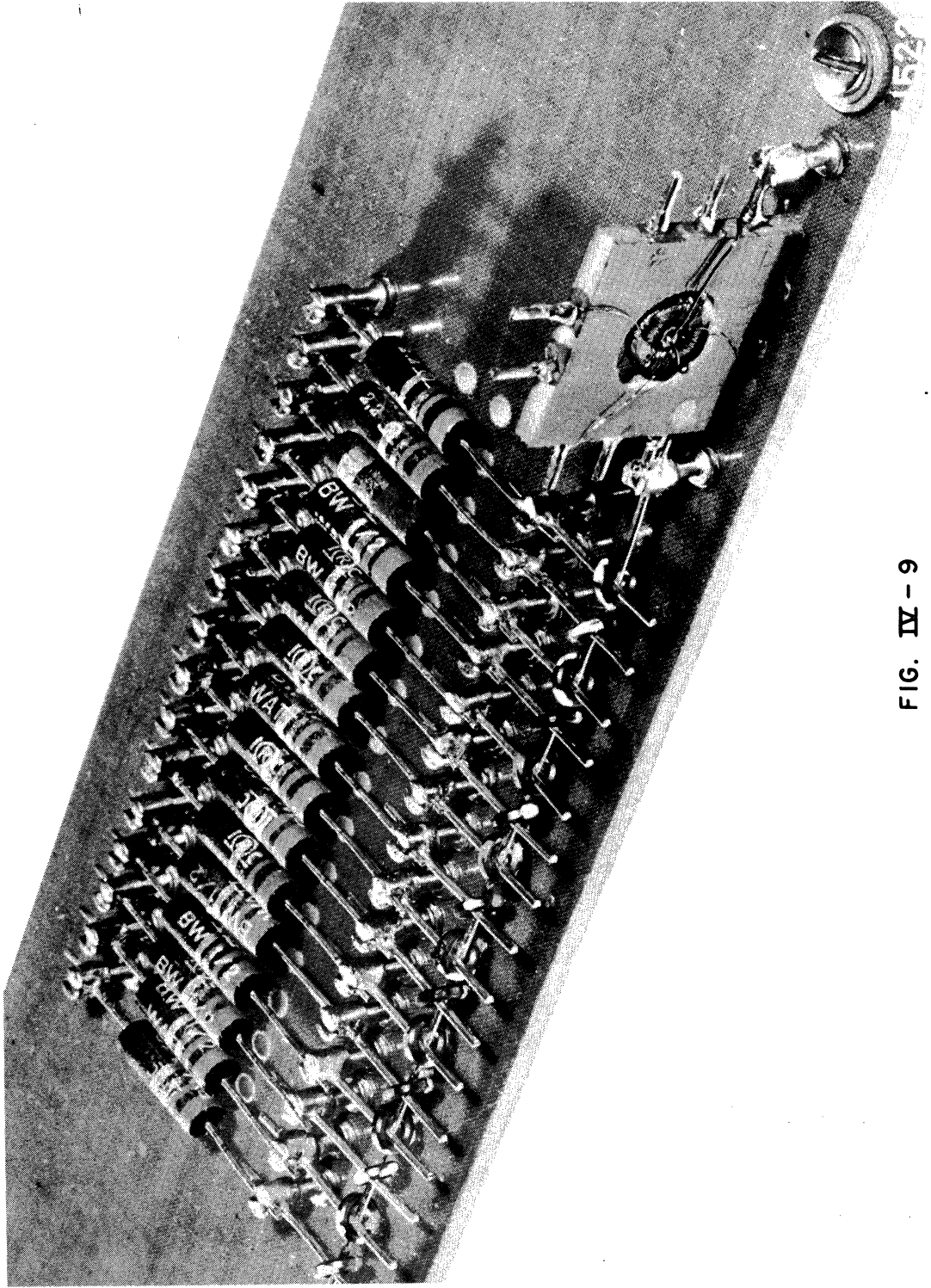


FIG. IV - 9
CROSS SECTION OF CERAMIC ARRAY II

the second memory showing the details of the final transformer mounting. Each core is mounted in a one-inch square of phenolic that has ten terminals on it. The leads from each control winding come out on one side of the square, and the secondary leads come out to the terminals on which the transformer is mounted. With this scheme, it is possible to mount or to change transformers quickly.

Writing a "ZERO" in the Memory

When the memory is driven directly from vacuum tubes, a "ZERO" can be written by simply skipping the write operation, for the core is left in the "ZERO" position after reading. When the matrix switches are used to drive the memory, the write operation cannot be skipped because it is necessary to return the switches to their original condition before they can be used to read again.

Two schemes have been used to clear switches without writing a "ONE" into the memory. In the first scheme, one switch is cleared before the other so that the currents do not add at the selected core. In the second scheme, an "inhibiting" current equal to the output of one switch but of opposite polarity is applied to a "Z" axis winding which passes through every core in the array. This current is not enough to disturb the cores in the array but when the switches are cleared, it subtracts from the switch current, and the selected memory core is not disturbed. The time for a write operation is significantly shorter in this latter scheme.

Figure IV-10 is a block diagram of a scheme for clearing the switches alternately when a "ZERO" is to be left in the memory after reading. This is part of a memory test system where the content of a core is read out, temporarily held in a buffer storage flip-flop, and then written back into the same core.

The switch driver tubes, which are shown along the top of the diagram, are connected to flip-flops so that they drive the switch as long as the flip-flops are in the "ONE" position. Because the width of the driver gates is very critical, delay lines are used to control the length of time that the flip-flops are in the "ONE" position.

The initiating pulse first resets the buffer storage flip-flop FF05 and starts the read operation by setting FF01 and FF02 in the "ONE" position. If a "ONE" is read out of the selected core, FF05 is set in the "ONE" position by a pulse from the sensing winding. If the core held a "ZERO", there is no pulse and FF05 remains in the "ZERO" position.

The read operation is terminated by the pulse out of delay line DE01 and the pulse out of DE04 starts the write operation. If FF05 holds a "ONE", GT02 passes a pulse and sets both FF03 and FF04 in the "ONE" position so that both the X and the Y switches are driven at the same time. If, however, FF05 held a "ZERO", GT01 passes the pulse and the start of the write Y operation is delayed by DE05 until after the write X operation is

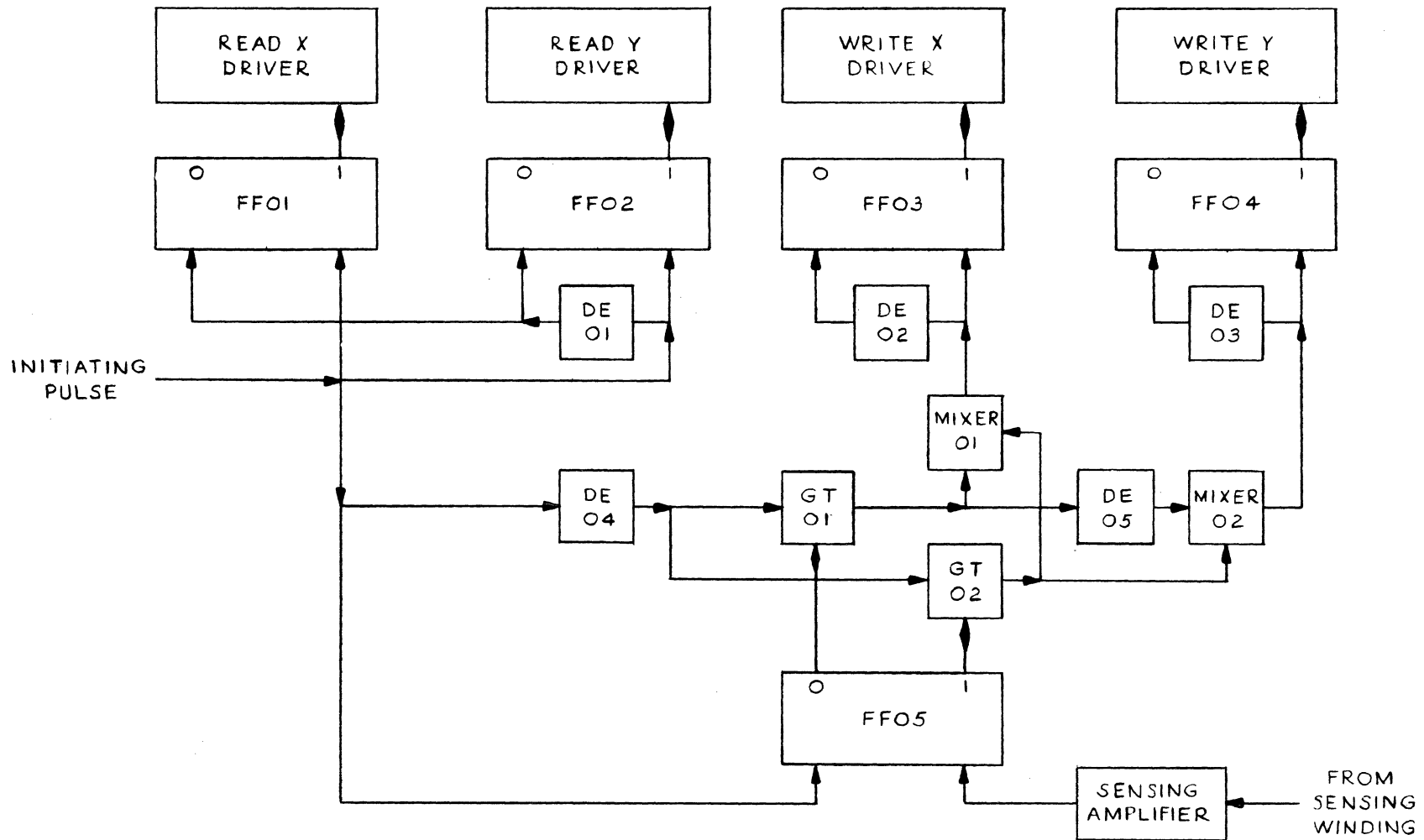


FIG IV-10

SCHEME FOR WRITING "ZERO" WITHOUT A "Z" WINDING

finished. Mixer O1 could be eliminated by connecting the input of FF03 directly to the output of DE04, but the slight delay a pulse suffers going through a gate tube circuit would make the Y driver start later than the X when a "ONE" is being written.

Scheme for Writing "ZERO" Using a "Z" Winding (Figure IV-11)

The initiating pulse sets the buffer storage flip-flop FF04 in the "ZERO" position and sets FF01 in the "ONE" position which starts the read operation. If the selected core holds a "ONE", the sensing winding will pick up a pulse which, when amplified, will set the buffer storage flip-flop FF04 in the "ONE" position. If the memory holds a "ZERO", no pulse is produced and the buffer storage stays in the "ZERO" position. After the delay DE02, the gate tube on the "ZERO" side of FF04 is sensed. If the flip-flop holds a "ZERO", the pulse passes the gate and sets FF03 which starts the gate that puts current in the Z axis and keeps a "ONE" from being written into the memory.

The pulse from DE02 also enters DE03 which compensates for the delay in the pulse to the Z axis suffers in the gate so that the write drivers will not start before the Z driver.

Design of Switch Drivers

In the first memory system, the control windings of the switch were driven from a set of heavy triodes whose grids were tied directly to the outputs of the selecting flip-flops. This scheme

A-51229

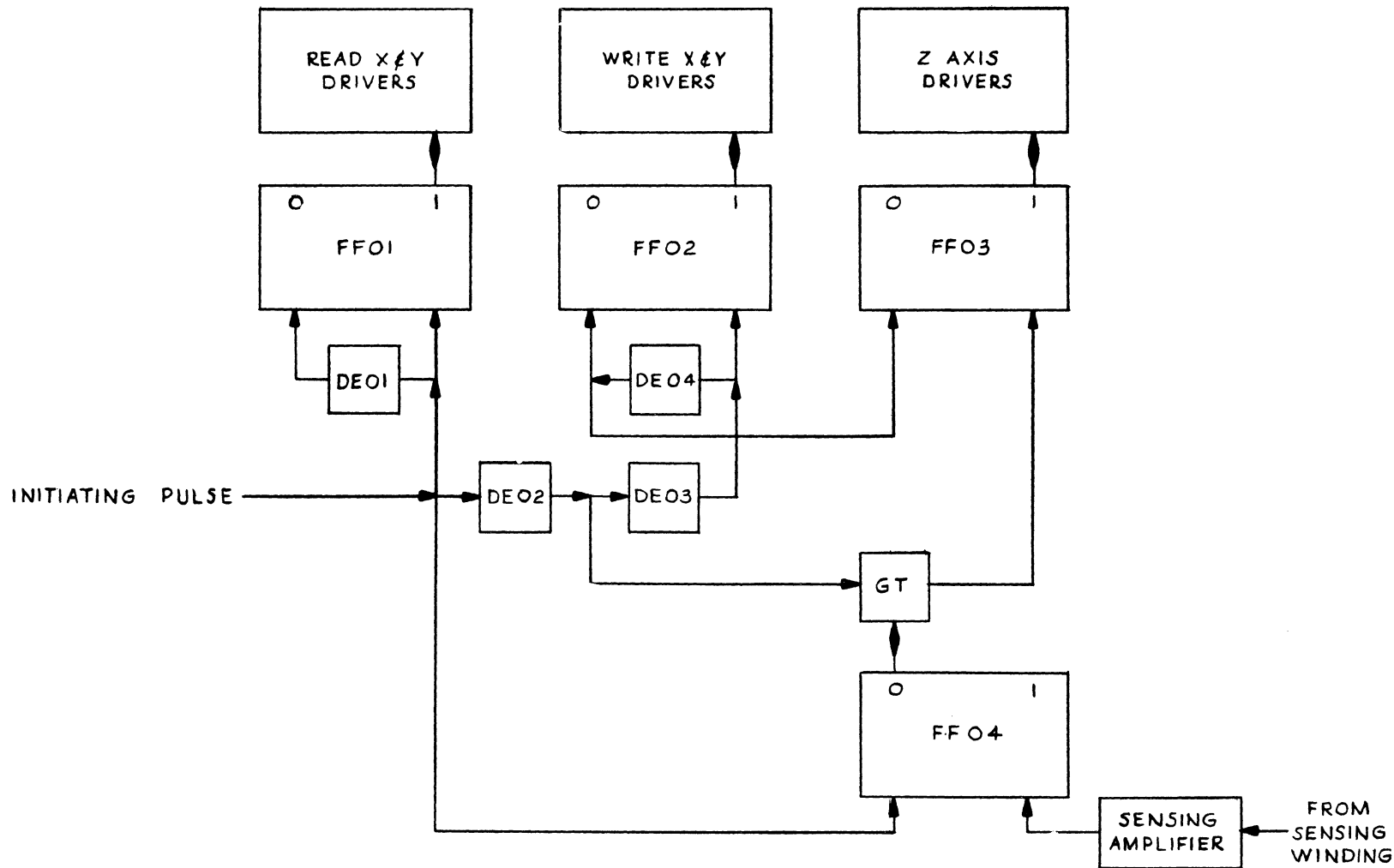


FIG IV-II
SCHEME FOR WRITING "ZERO" USING A "Z" WINDING

had two disadvantages: the triodes were continuously drawing several amperes from the power supply, and they were difficult to keep cut-off during the positive back-voltage pulse from the switch.

The final drivers use pentodes to drive the windings so that variations in plate voltage will not affect the cut-off voltage. Gate tubes are included in the circuit so that the drivers are not drawing current continuously, but only during the switching operation.

Figure IV-12 is the circuit schematic of the drivers used in the final system. Grid 3 of the gate tube V1 is controlled by one of the selection flip-flops. Grid 1 is normally negative but is brought to ground level during the switching operation. If both control grids of F1 are positive, the plate is driven negative and cuts off the normallyconducting triode V2. When V2 is conducting, its plate is at about -50 volts and it keeps the driver tube V3 cut off, but when V2 is cut off, its plate goes to ground and V3 conducts and drives the switch. Figure IV-13 shows some waveforms illustrating the operation of the driver.

Block Diagram of Selection Scheme

In the first memory system, the control windings were used only to saturate the transformers in the switch that were to be cut off. Besides the control winding, each transformer had two primary windings — one to drive in each direction. The second memory used the control windings for both driving and selection as in the

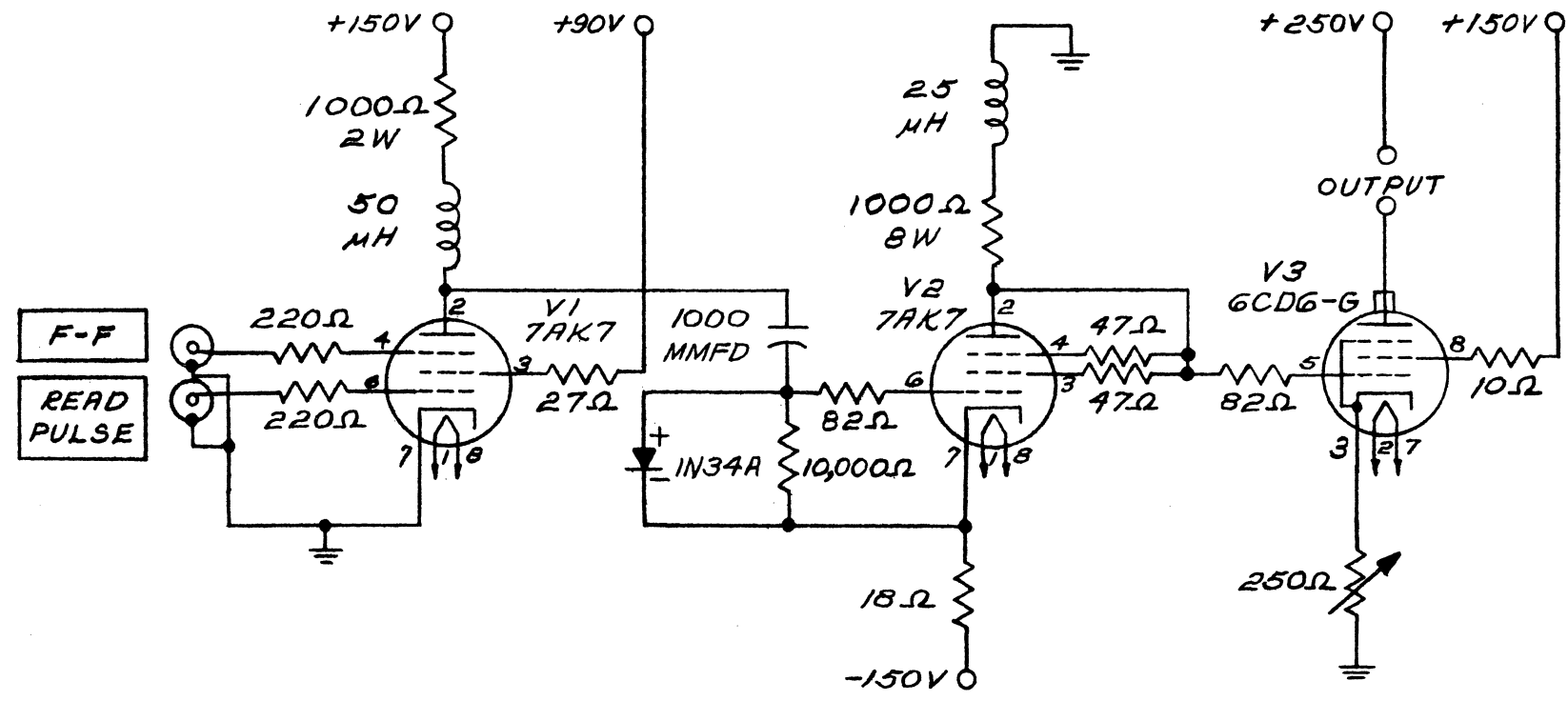


FIG IV-12
CIRCUIT SCHEMATIC, GATED DRIVER

GRID 1 OF V_1

GRID 3 OF V_1

GRID 1 OF V_2

GRID 1 OF V_3

PLATE OF V_3 WITH 100Ω LOAD

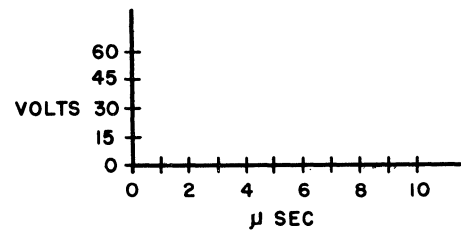
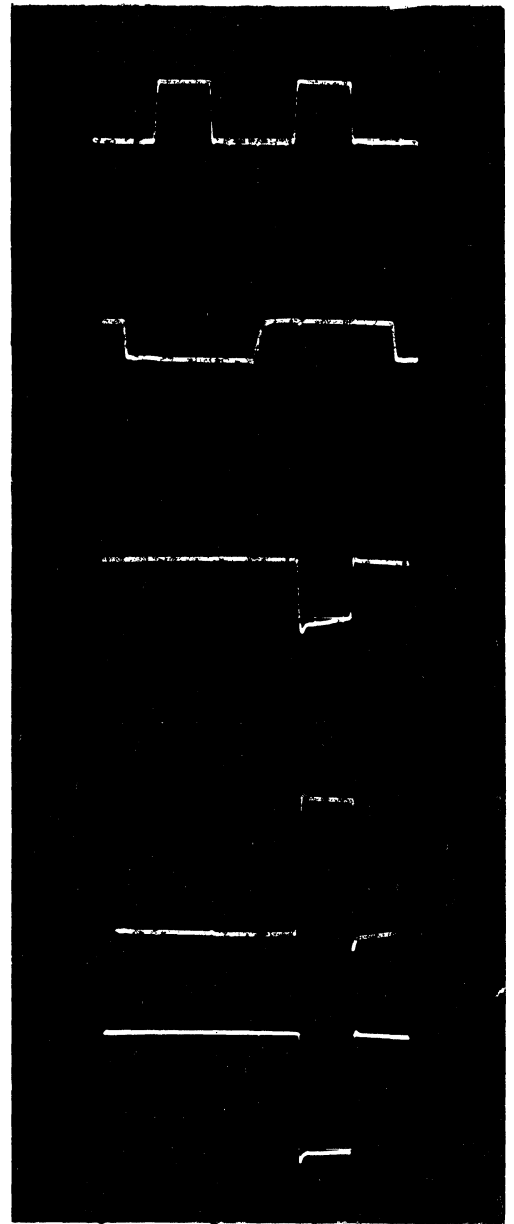


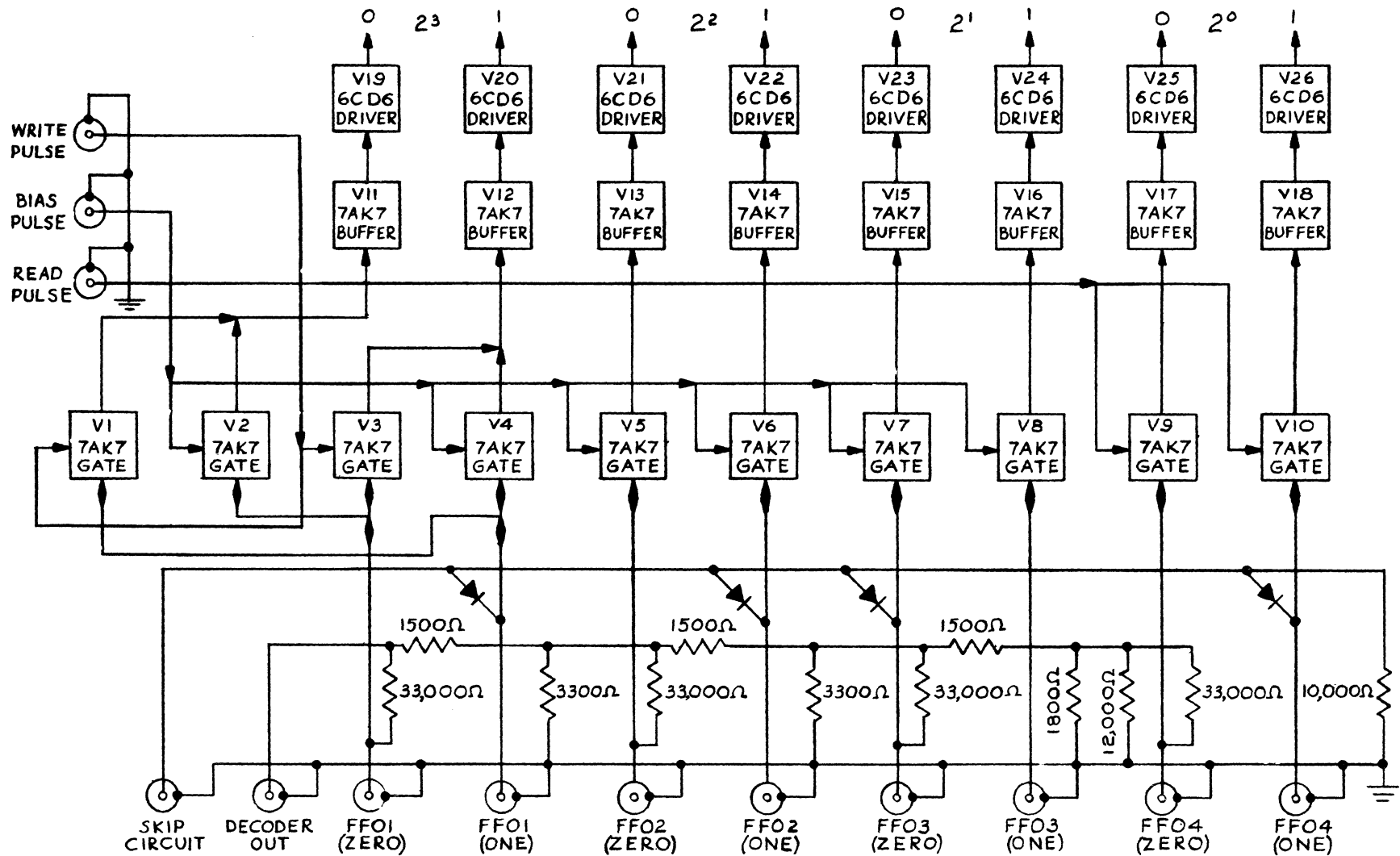
FIG. IV-13
WAVEFORMS OF GATED DRIVER

alternate switch discussed in Chapter I and illustrated in Figure I-5. This elimination of two windings on each transformer significantly simplified the construction of the switch.

A block diagram of the driving circuits for one of the sixteen-position switches is shown in figure IV-14. It consists of eight of the three-tube driver circuits discussed in the previous section — one for each input to the switch. At the start of a switch operation, the binary number corresponding to the position of the switch to be selected is set up in the selection flip-flops whose inputs are along the bottom of the diagram. They select the appropriate four drivers and hold the others inoperative. After the flip-flops are set, the "bias pulse" input is driven positive. In each of the last three digits, the drivers that are not held inoperative by the selection flip-flops are made to conduct. The currents from these drivers are used to saturate all but two cores in the switch. Then the "read pulse" input is driven positive which starts one of the two drivers of digit 2^0 . This driver puts current into the switch in the opposite direction and drives one of the two transformers which were not saturated by the bias drivers. After the read operation is complete, the read pulse and the bias pulse are both terminated.

The transformer that was just used to read is the only one that must be driven in the write direction because all the others have flux already in that direction. This transformer can be driven

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BLOCK SCHEMATIC GATED DRIVER PANEL
FIG IV-14

in the write direction by simply driving current into the whole switch. In this block diagram only half the switch is driven because it is so simple to determine which half of the switch this transformer will be in. It will be in series with the driver of digit 2³ that was not activated during the read operation. Gate tubes V1 and V3 are connected so that when the write pulse is applied to their grids 1, that driver is activated which had previously not been activated by V2 or V4 during the read operation.

These drivers were built on one panel which also contains a display decoder and a skip circuit to be discussed in the later sections.

Sensing Amplifiers

Figure IV-15 is the schematic of the circuit used to amplify the output of the sensing winding, which is between a half and one volt. The step-up transformers at the input are arranged with crystal diodes in a full-wave rectifying circuit so that regardless of the polarity of the pulses in, positive pulses are applied to the grid of V1. The tubes V1 and V2 amplify the pulse but their bias is adjustable so that they can differentiate against low level pulses such as those that are produced when a "ZERO" is read out of the memory.

Memory Display

Equipment has been incorporated into the testing scheme

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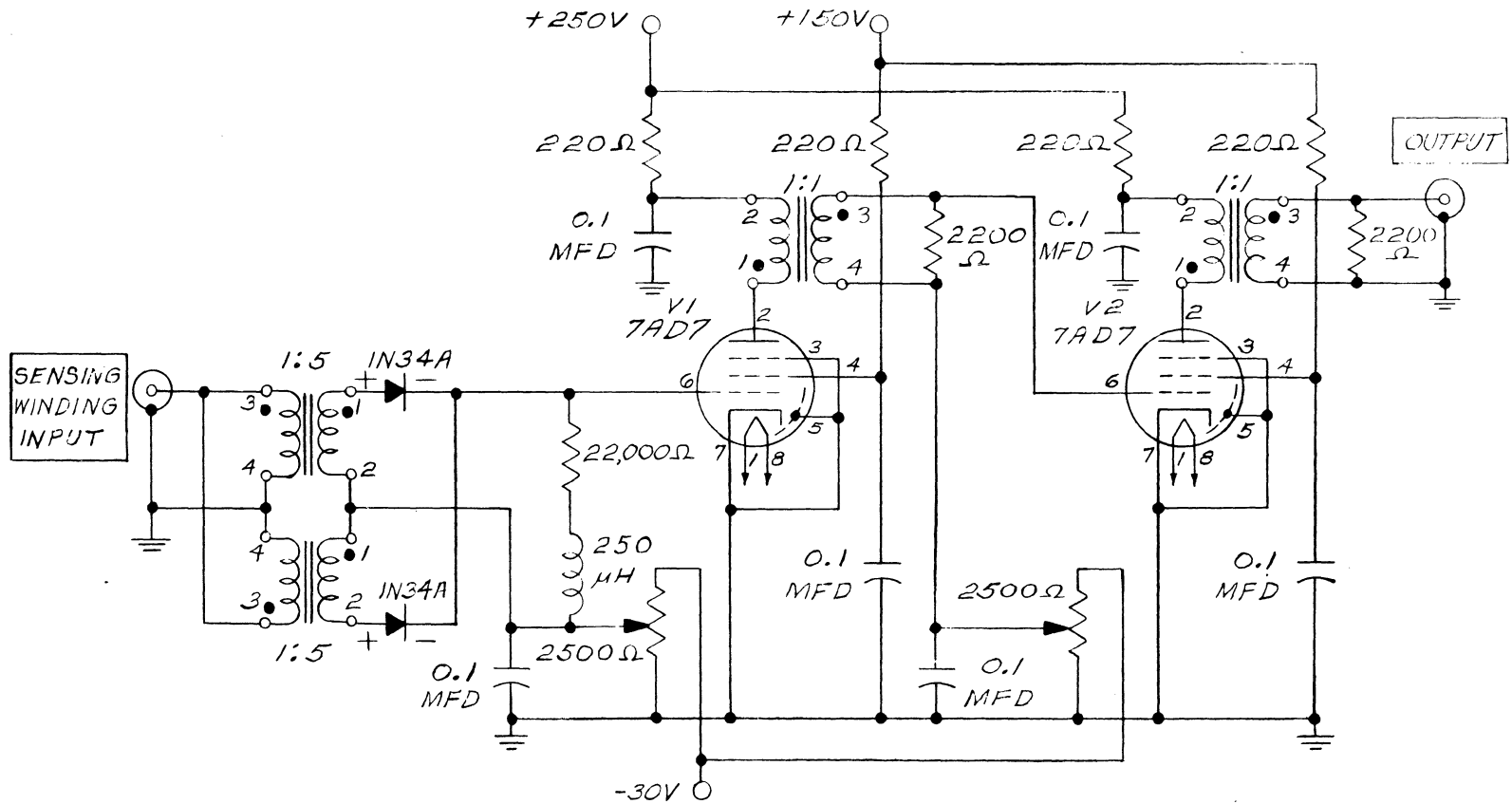


FIG IV-15

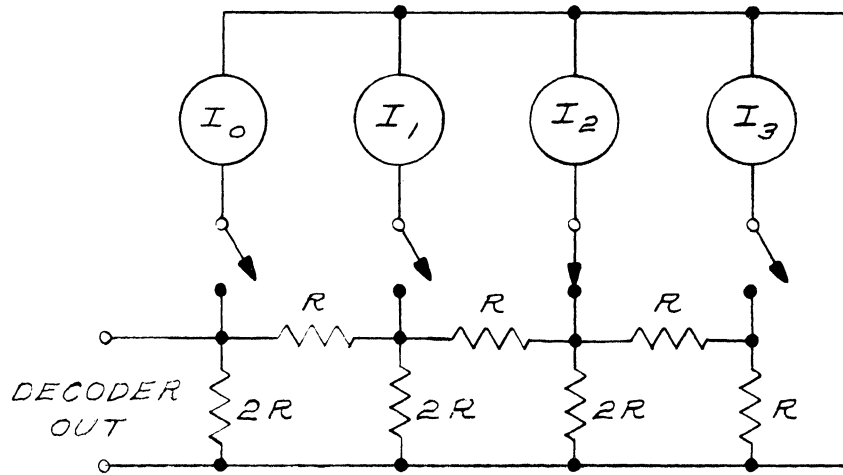
CIRCUIT SCHEMATIC, SENSING AMPLIFIER

to display all the "ONE's" in the memory as spots on an oscilloscope physically positioned as corresponding cores on the array. It is not only convenient to have the contents of the memory visible during testing but this makes possible very interesting displays.

In the scheme used to test the memory, the selecting flip-flops are arranged to count so that each core in the array is selected in sequence. During the time a core is selected, its content is read out, and if it is a "ONE", it is displayed on the scope. Just before the next core is selected, the original content of the core is written back in. During the period between the read and rewrite operations, the content of the core is held in a buffer-storage flip-flop. This flip-flop not only holds the information to be written back in the selected core but also unblanks the scope when a "ONE" has been read out of a core. Binary-to-analog decoders, one for each coordinate, produce deflection voltages proportional to the binary numbers set up in the selecting flip-flops and so displace the spots according to the position of the cores in the memory array.

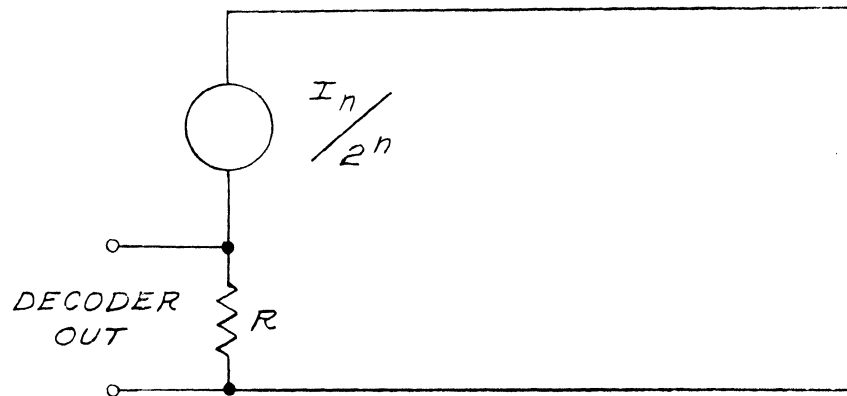
Display Decoders

Figure VI-16 shows a four-digit ladder-type binary-to-analog voltage decoder. A current source for each digit in the decoder feeds one node of the ladder. When a digit is "ZERO", no current flows from the source in that digit, but when a digit holds "ONE", the source feeds a fixed current to the ladder.



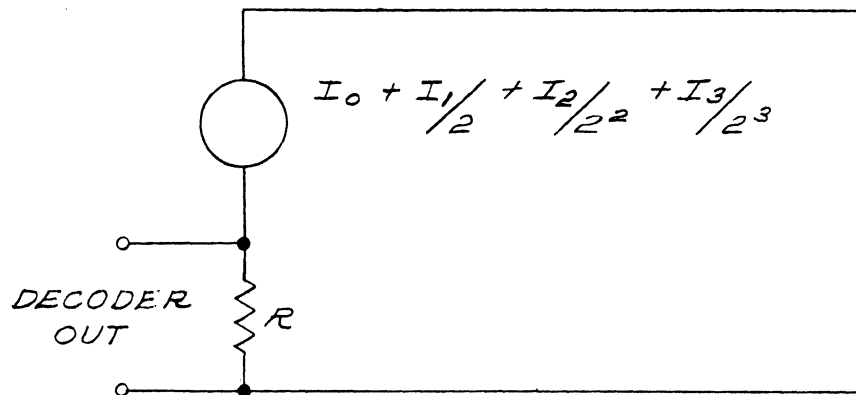
FOUR DIGIT BINARY TO ANALOG DECODER

FIG IV-16



EQUIVALENT OF DECODER WITH ONLY SOURCE I_n ON

FIG IV-17



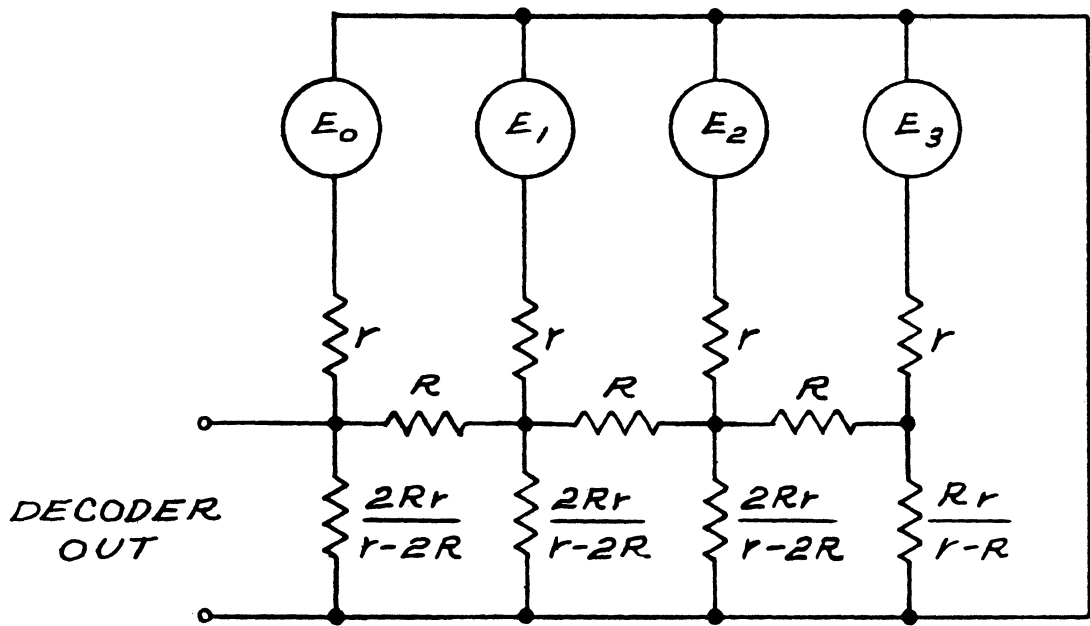
EQUIVALENT OF DECODER WITH ALL SOURCES ON

FIG IV-18

The voltage at the output terminal is proportional to the binary number set up in the current sources. (The most significant digit is nearest the output.) This can be seen by making a Thevenin equivalent circuit of the decoder with only one source on. The equivalent circuit will be found to be that of figure IV-7, regardless of which source is on. By superposition, the equivalent with all sources is that of figure IV-18. The contribution of each current source to the output voltage is weighted according to the significance of its digit.

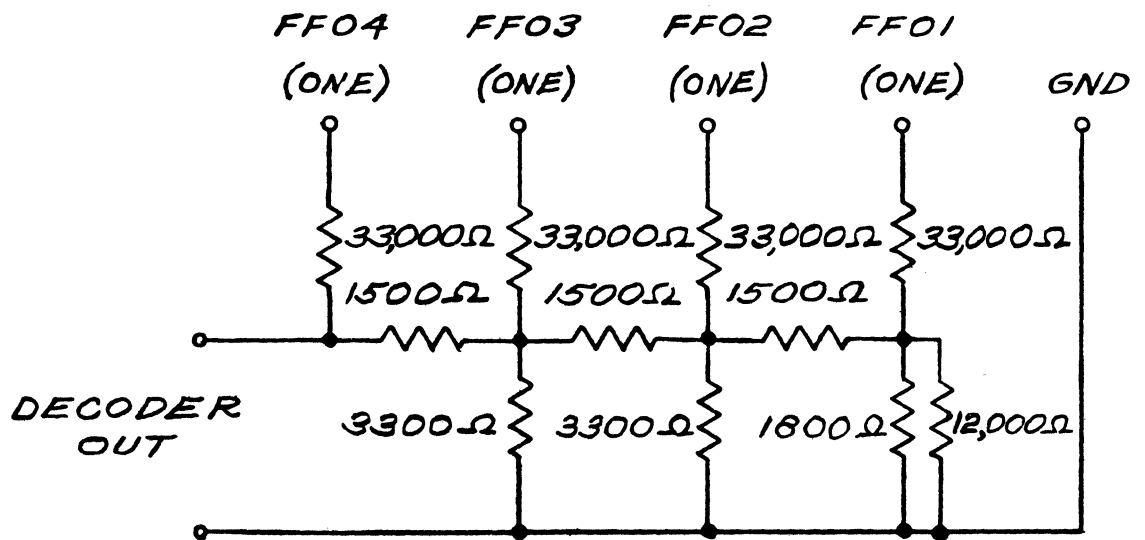
The decoders used in this apparatus are driven directly from flip-flops whose impedance is low and therefore must be taken into account. If we assume the output of a flip-flop is a voltage source with a series resistance, as in figure IV-19, a circuit equivalent to Figure IV-16 can be had by increasing the shunt resistors in the ladder so that the parallel resistance of source impedance and the new shunt resistance equal the original shunt resistance used with ideal current sources. The relationships between resistances are shown in Figure IV-19.

The circuit actually used in the memory system is shown in figure IV-20. The precision of the decoder is in proportion to the precision of the resistors used except in the case of the shunt resistor across the output, which can be any value. In this decoder the resistor was left out altogether because slightly greater voltage is obtained without it.



DECODER USING FINITE IMPEDANCE SOURCES

FIG IV-19



DECODER USED IN DRIVER PANEL

FIG IV-20

"Light Gun"

A "light gun" is used with the scope display to write arbitrary patterns of "ONE's" and "ZERO's" into the memory. These patterns are used to test the memory and to demonstrate its operation. The "light gun" is a tiny photocell connected through an amplifier to a gas tube pulse generator as in the schematic of figure IV-21. When light strikes the photocell, the current produced is amplified and applied to the pulse generator and a pulse is produced at the output. The pulse generator is held inoperative except when the trigger switch is pushed so that spurious light will not produce pulses.

To write a pattern into the memory, all "ONE's" are first read in by holding the buffer storage flip-flop in the "ONE" position as all the cores in the memory are read and rewritten. The system is then put back to normal operation where each core is selected in order, its contents read, displayed, and rewritten. The light gun is then aimed at each spot in the display that is to be changed to "ZERO". When the gun is aimed at a spot, a pulse is produced as the scope is intensified indicating that a "ONE" has been read out of the core corresponding to that spot. This pulse sets the buffer storage flip-flop to the "ZERO" position so that a "ZERO" will be read back into the core. From then on a "ZERO" will be read out of that core and rewritten during each cycle and the spot will not be intensified. Figure

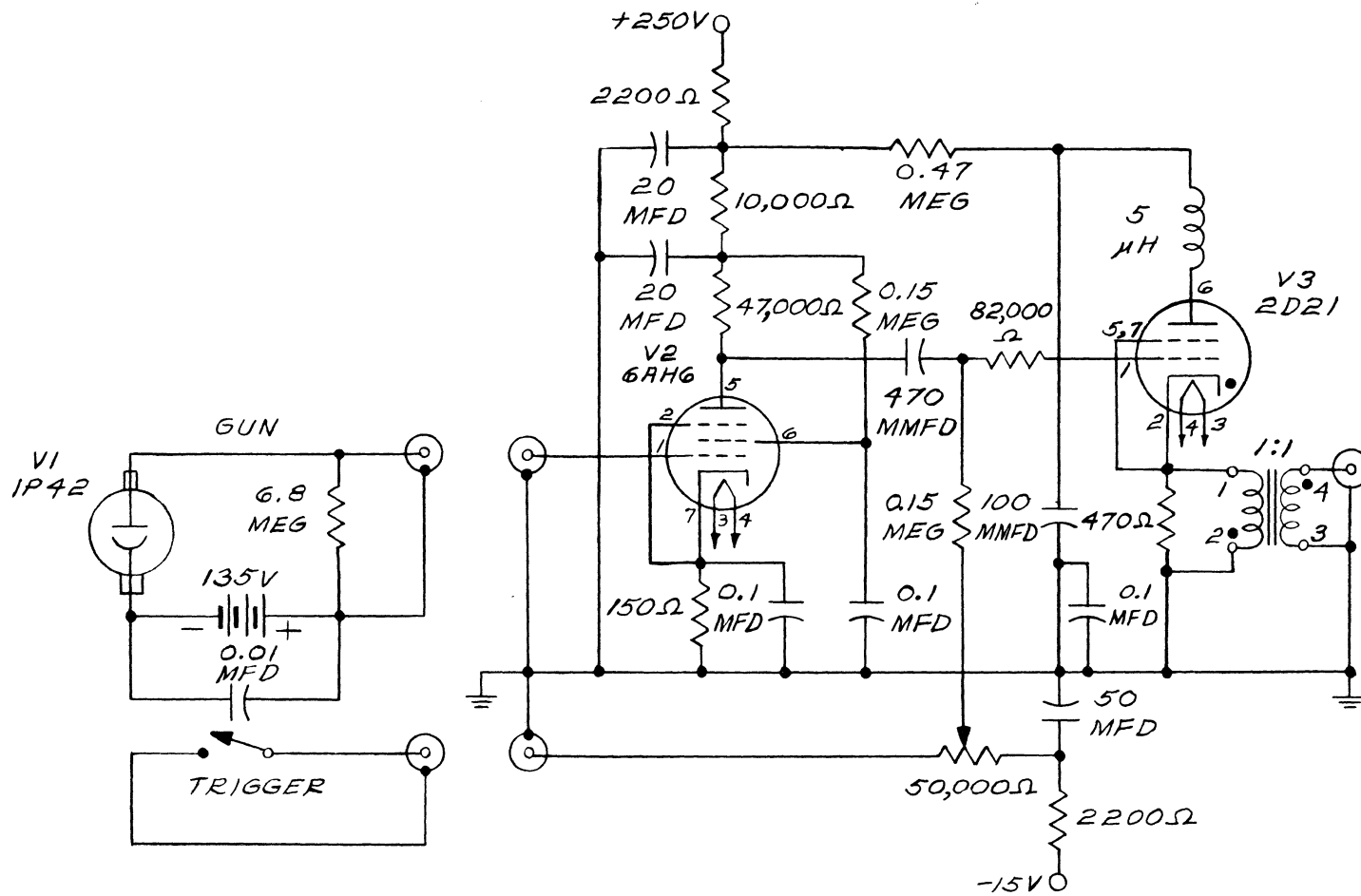


FIG IV-21,
CIRCUIT SCHEMATIC,
LIGHT GUN PULSE GENERATOR

IV-22 is a photograph of the light gun being used to write a pattern into the memory.

Complete Block Diagram of Memory System

Figure IV-23 is the block diagram of the final memory system. Each read-write operation is initiated by a pulse from the multivibrator pulse generator in the lower left-hand corner. This normally goes through the adjustable delay DE09 to start the sweep on the synchroscope. The start of the operation is delayed by DE01 so that all of the operation can be seen on the scope. The coder is a pulse amplifier that has four individually adjustable outputs. The first output transfers the contents of FF14 into FF09 through the gates GT12 and GT13 and after DE10 it sets FF14 in the "ZERO" position. Switch S2 connects directly to the output of the coder or to a push-button pulse generator that is synchronized by an output of the coder. From S2 the pulse goes through mixer O2 to the first of the selection Flip-Flops, FF01 to FF08. These flip-flops with their associated gate tubes are arranged so that they could the pulses from mixer O2. With each count, a new core is selected in the memory, and after 256 pulses every core in the array has been selected.

In each gated driver panel there is a skip circuit which consists of a crystal diode tied to one of the outputs of each selection flip-flop as in figure IV-14. When a predetermined number is set up in the selecting flip-flops controlling a driver

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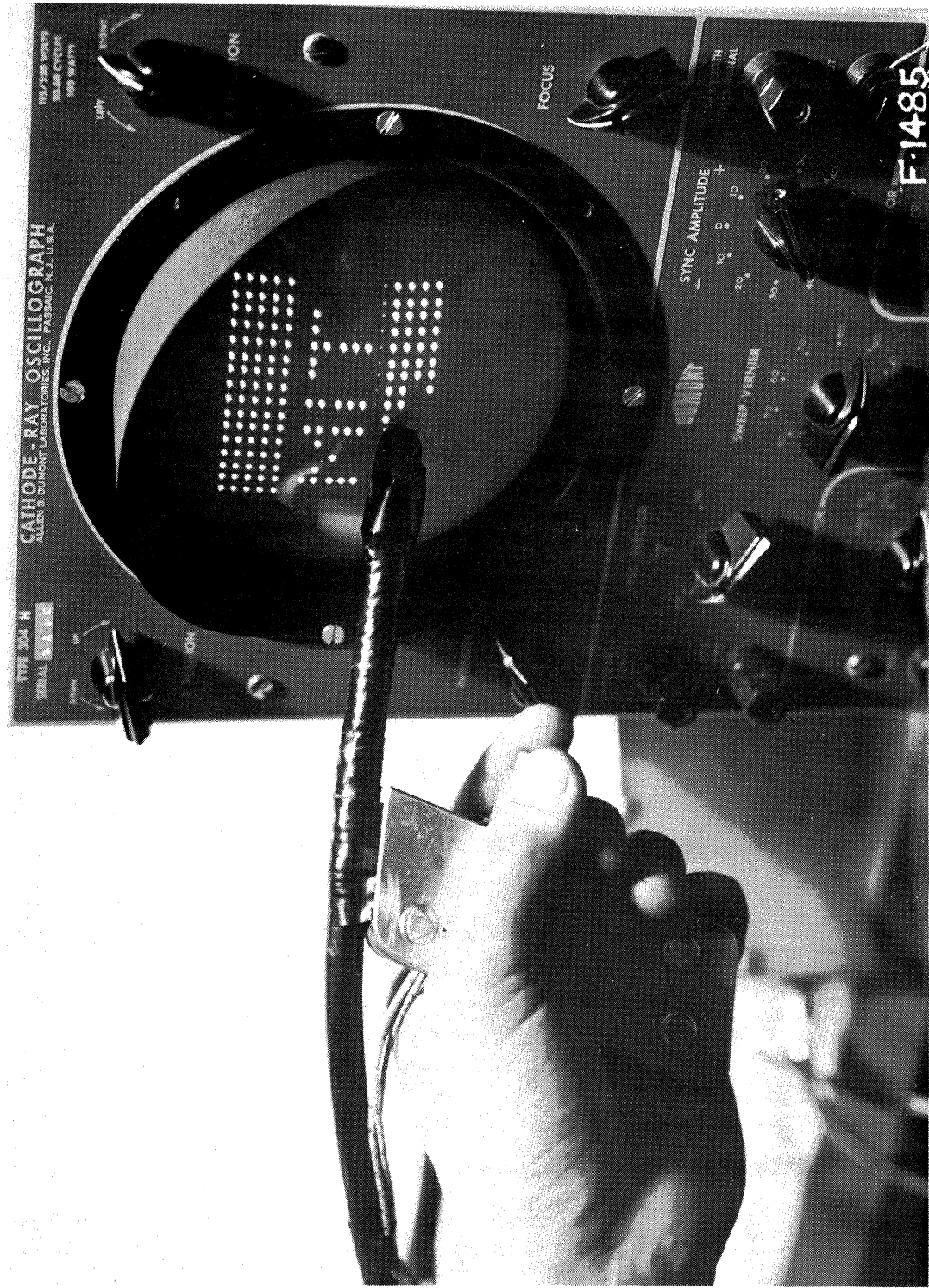


FIG. IV-22
LIGHT GUN AND DISPLAY

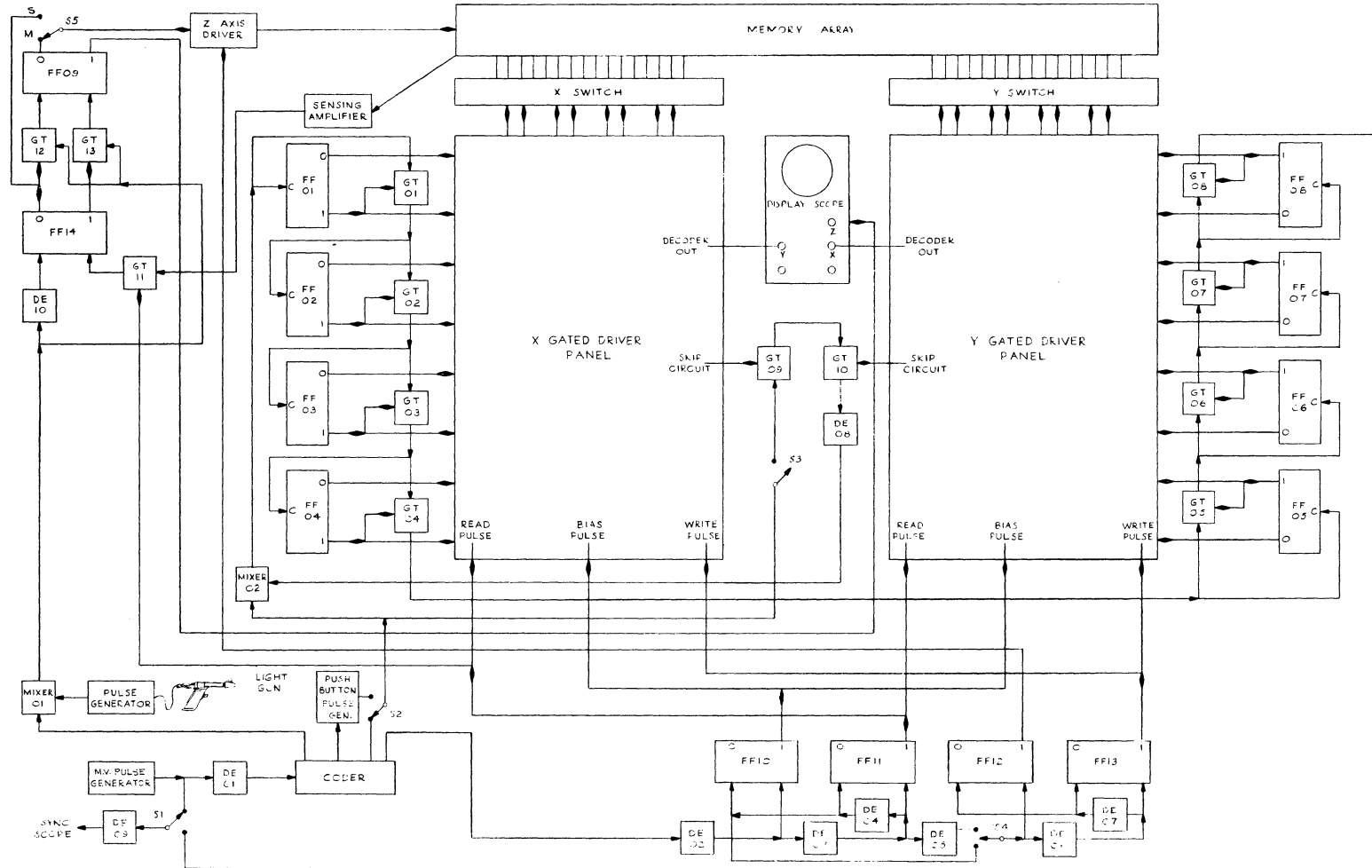


FIG. 1V. -23

BLOCK DIAGRAM CERAMIC MEMORY ARRAY II

panel, the output of the skip circuit rises to ground. In this block diagram the skip circuits are connected to the gate tubes GT09 and GT10 so that when the predetermined numbers are set up in the flip-flops, these gates can pass pulses. If switch S3 is closed and if this number is in the flip-flops, the pulse from the coder will not only go to the FF01 to be counted, but will also go through GT09 and GT10 and after a short delay in DE03, it will again go to FF01 to be counted. In this way, one core in the memory can be skipped during the cycle to see if it will hold its information while the rest of the memory is operated on.

An output of the coder also goes through DE02 to start the read operation. The first step is to set FF10 in the "ONE" position which starts the bias pulse to the driver panels and so sets up current in the control windings of the switches. After DE03, FF04 is set and the read pulse sent to the driver panels. If a "ONE" is read out of the memory, a pulse is picked up in the sensing winding which is amplified and applied to grid 1 of Gate Tube, GT11. Grid 3 is held positive by FF11 only during the read operation so that noise picked up in the winding any other time will not get by this gate. FF14 was originally set in the "ZERO" position and it stays there if the selected core contains a "ZERO", but if the core contains a "ONE", it is set to "ONE" by the output of GT11.

The read operation is terminated by the pulse from DE04.

The write operation can be started immediately or it can be delayed by DE05 as decided by the position of switch S4. First FF12 is set which drives the Z axis driver and then FF13 is set and the switches are driven in the write direction. The Z axis driver is a gated driver like those on the driver panels. If a "ZERO" is to be left in the memory, the grid 3 of the gate tube in the driver is positive so that current is driven through the Z winding during the write operation. When switch S5 is in the S position, the number that was just read out of the core, which is held in FF14, will be written back in. In this mode of operation, a pattern of "ONE's" and "ZERO's" will stay stationary in the memory. With S5 in the M position, the content of the previous core, which is now held in FF09, is written in to the selected core. In this mode of operation, the pattern is advanced one core during each cycle and when the pattern is displayed, it can be seen to move across the array.

Testing Schemes

Three schemes have been found to be very useful in testing the memory system. In the first scheme, "ONE" is read into a single memory core, and "ZERO" into all the others. The system is then put into the mode of operation in which one by one the contents of each core is read and temporarily stored to be written into the next succeeding core. The "ONE" then progresses continuously through the whole memory. The second scheme

is like the first except that all "ONE's" and a single "ZERO" are written in the memory. This "ZERO" then cycles through the whole array. The third scheme can be used in conjunction with the previous schemes or it can be used with a stationary pattern. A "ZERO" or a "ONE" is written into a certain core and the selection system is then fixed so that this core is skipped during each major cycle. After many cycles, this core is selected again to see if it still contains the number that was placed there originally.

CHAPTER V RESULTS AND CONCLUSIONS

The purpose of this thesis research was to demonstrate experimentally the feasibility of using magnetic-matrix switches to drive a coincident-current memory. It is believed that this purpose has been accomplished by the construction and operation of a 256 core memory driven by two 16 position switches. Although careful adjustments and exhaustive tests have not been made as yet, the memory has held arbitrary patterns of "ONE's" and "ZERO's" for many operations.

The access time of this experimental memory is much less than that of most other random access memories. In three microseconds, a core is selected, its contents read out, and a number written back in. The timing cycle is divided as follows: 0.75 microseconds to set the selecting flip-flops and saturate the desired portions of the switch, 1.1 microseconds to read, and 1.2 microseconds to write back into the memory. The contents of a core are received 1.6 microseconds after the start of the operation.

Research on this experimental model is continuing and improvements in access time and reliability are expected. However, much research remains to be done before a memory and switch are ready for use in a computer. The development of better cores will be an important part of this work. The memory cores should have lower coercive force and more nearly rectangular ϕ -I curves.

Much of this improvement will have to come from the development of better materials, but one of these two characteristics can be improved by changes in the geometry of the core. A high ratio of inside to outside diameter will improve rectangularity, but because the minimum wall thickness is fixed by the fragility of the material, this ratio is obtained by increasing the diameter and thus the coercive force. The coercive force can be made low at the expense of rectangularity by making the inside diameter of the core very small and making the outside diameter any convenient size. When the core wall is thick, flux is changed only in the material close to the inside radius and so the diameter ratio is not important.

Future development of matrix switches must be aimed in two directions. First toward greater simplicity, because the switches as built in this experimental unit with their many windings of fine wire, do not have the simplicity and thus the reliability that is desired in a large scale computer. Second, switches must be developed that can drive large portions of a complete memory.

Signed


Kenneth H. Olsen

Approved


Jay W. Forrester

APPENDIX I SOME OTHER USES OF THE MATRIX SWITCH

In driving the coincident-current magnetic memory, the matrix switch was used as a multiposition selection switch. Each binary number in the input uniquely selected one output. The switch can also be used to convert the binary input into some arbitrary function. Function tables have been made with crystal-diodes, but those made with magnetic cores would have the following advantages:

- (1) A small number of cores can often do the job of many crystals.
- (2) The output of each switch position can be mixed by simply wiring the windings in series. Mixing is often difficult and slow with crystals.
- (3) The impedance of a core switch can be made low so that short pulses can be switched. The impedance of crystals is fixed within a narrow range.
- (4) Only the selected core in a magnetic matrix switch passes power, but in a crystal switch, all outputs but the selected one draw current.

Two simple examples of how function tables could be made with magnetic cores are discussed below.

Binomial-Binary to Cyclical-Binary Decoders

The ordinary binary code in which arithmetic operations are usually done is called a binomial-binary code. There are several other binary codes some of which have advantages in that errors picked

up in transmission or storage are less significant than in the binomial code. Figure VI-1 is a table comparing four digits of the binomial code to one of the other binary codes. This is one of the cyclical codes where only one digit is changed at each count.

Since arithmetic operations and some binary-analog conversions are difficult in any code other than the binomial code, it is often desirable to use a converter or a decoder to change from one code to another. One way of doing this is to reproduce the conversion table, such as that in Figure VI-1, in a matrix switch as has been done in Figure VI-2, where the original code is set up in the control windings and the new code is set up in the secondaries. Only the first three digits of the table were reproduced in this switch. The driving winding has been omitted for clarity. Just as the number in the original code selects one row in the conversion table, the number in the control windings will select one core in the switch. When this core is pulsed, it will produce pulses at the output corresponding to the output columns of the conversion table.

This decoder becomes unwieldy for large numbers because of the many cores needed. Study of the conversion table of Figure VI-1 will reveal that any digit, 2^n , in the cyclical code is dependent only upon digits 2^n and 2^{n+1} in the binomial code. There are only four possible combinations of the digits 2^n and 2^{n+1} and each of these combinations uniquely determines the integer in the 2^n digit of the cyclical code. These conditions can easily be built into a four-position matrix switch as in Figure VI-3, so that the two digits of the

DECIMAL	BINOMIAL BINARY	CYCLICAL BINARY
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

FIG VI-1
A CYCLICAL BINARY CODE

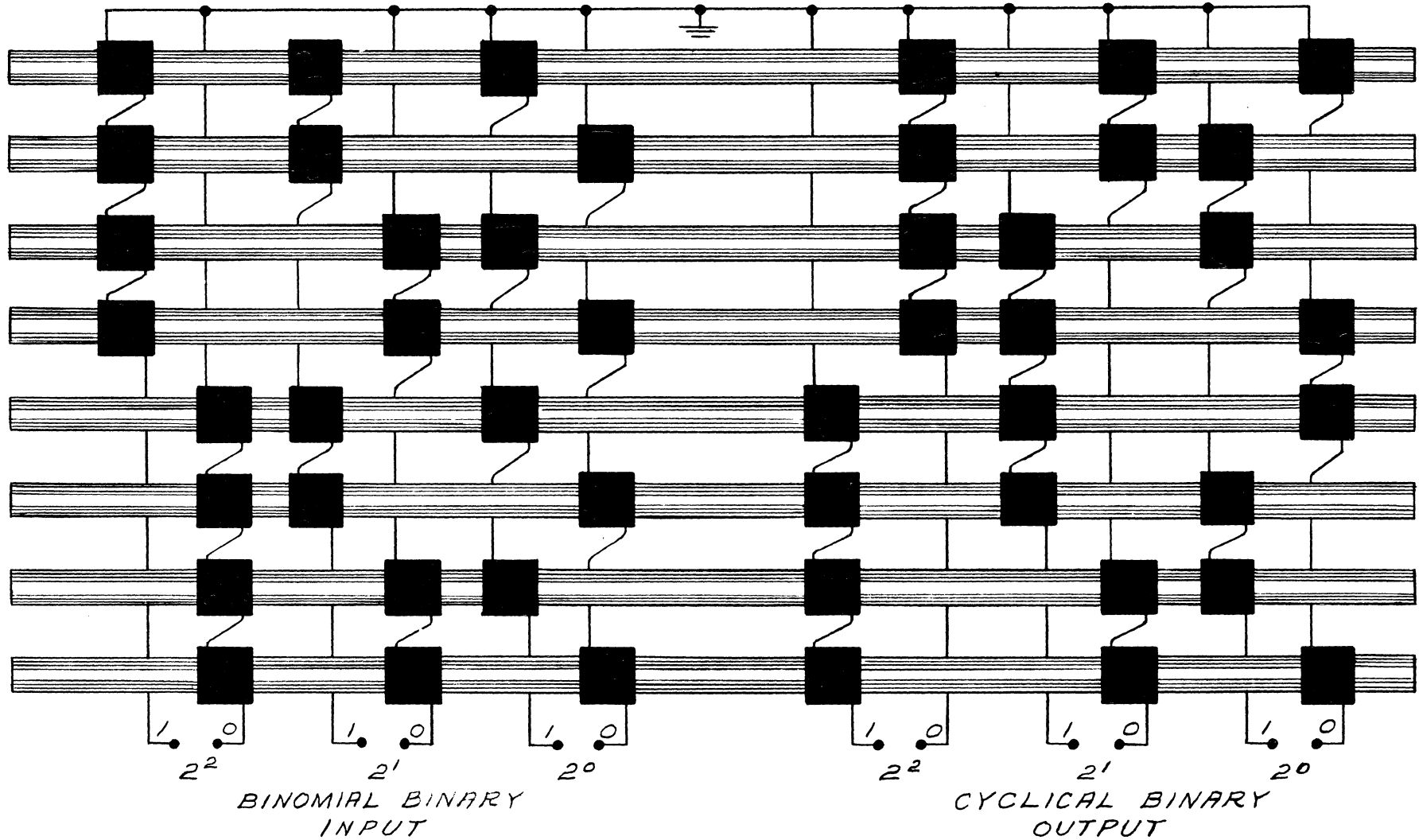


FIG VI-2
 BINOMIAL BINARY TO CYCLICAL BINARY DECODER

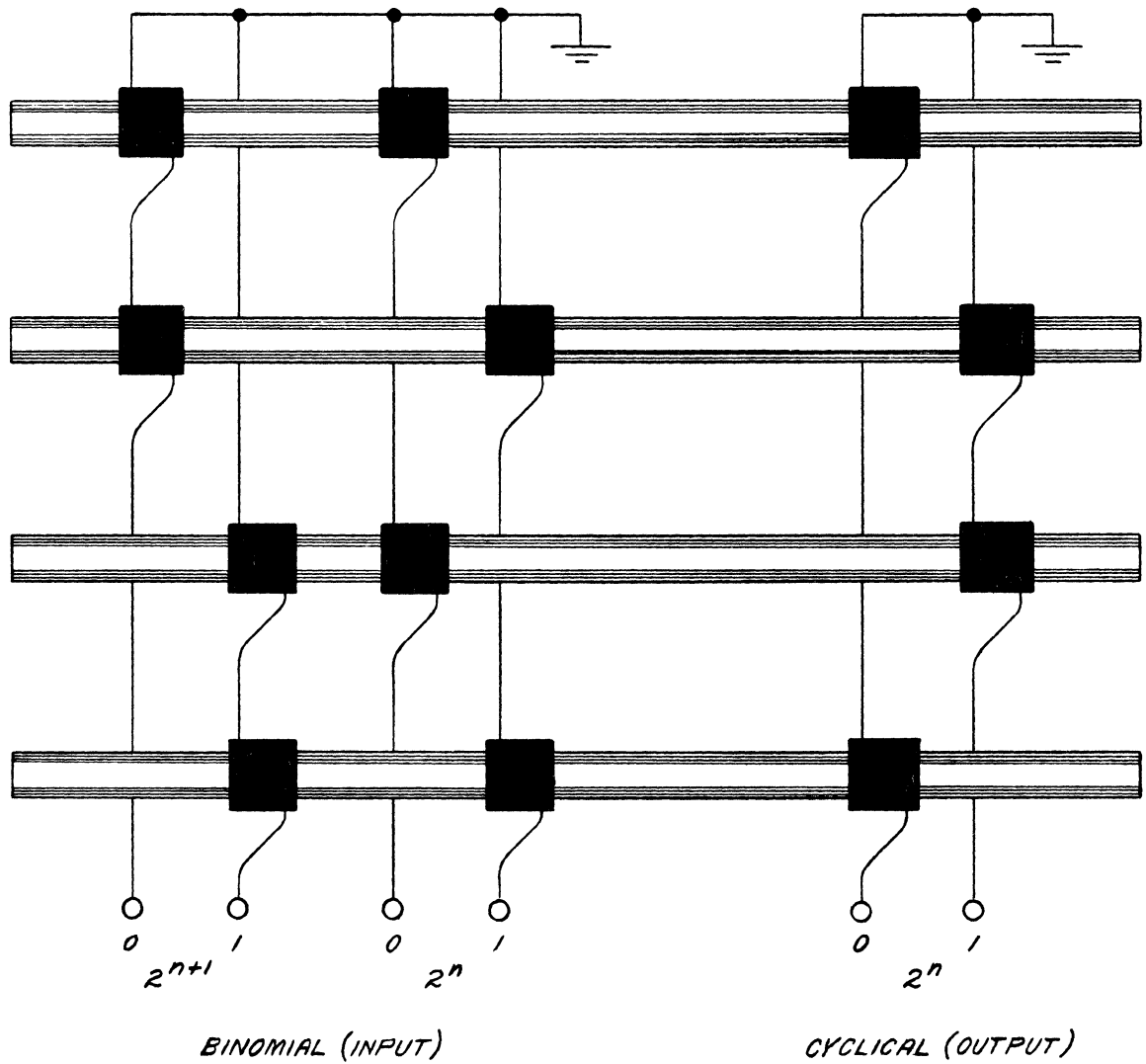


FIG VI - 3

BINOMIAL TO CYCLICAL DECODER

binomial code select one core. When this core is pulsed, it supplies the correct cyclical integer to the output. By using one of the latter type of decoders per digit, one can greatly reduce the number of cores required for converting multi-digit numbers.

A Matrix-Switch Adder

The magnetic matrix switch also lends itself nicely to arithmetic tables. Figure VI-4 shows a single-digit binary addition table where A and B are the two numbers of this digit to be added and C is the carry from the previous digit column. The answer is in the sum column and the carry for the next digit is in the last column. The three inputs, A, B, and C, define one row of the table and each row has the appropriate sum and carry.

In Figure VI-5, the table is reproduced in a magnetic-matrix switch. The three inputs, A, B, and C, select one of the eight cores each of which has two secondaries to give the appropriate sum and carry output pulses.

If the sense and position of the C windings are reversed as in the alternate switch of figure I-5, these windings drive the switch; and it is possible to use the carry output of one digit to drive the next digit. If a complete register of these switches is assembled as in Figure VI-6, we need only hold an input to the A and B terminals on each switch as we pulse the C-ZERO input of the rightmost digit. The switch in the first digit will produce the appropriate output at the sum terminals and the output of the carry termi-

$$A + B + C = \text{SUM} + \text{CARRY}$$

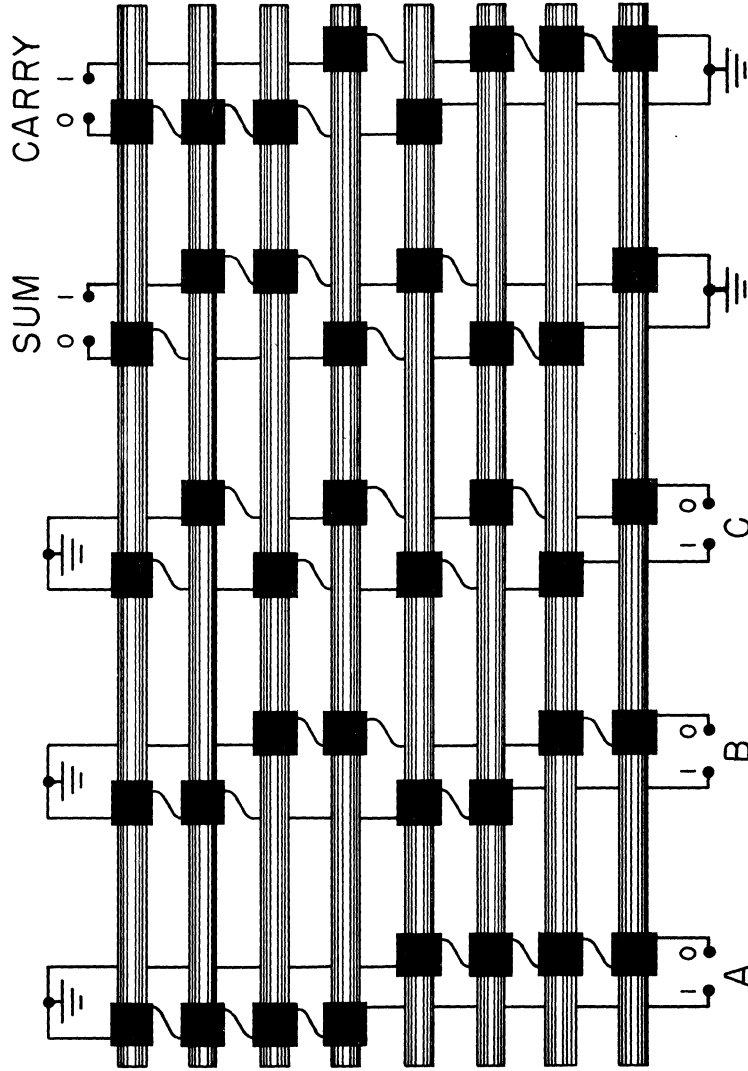
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FIG. VI-4

A SINGLE-DIGIT ADDITION TABLE

A-50900
F-1465
SN-367

B-50919
F-1472
SN-374



SINGLE DIGIT ADDER

FIG. VI-5

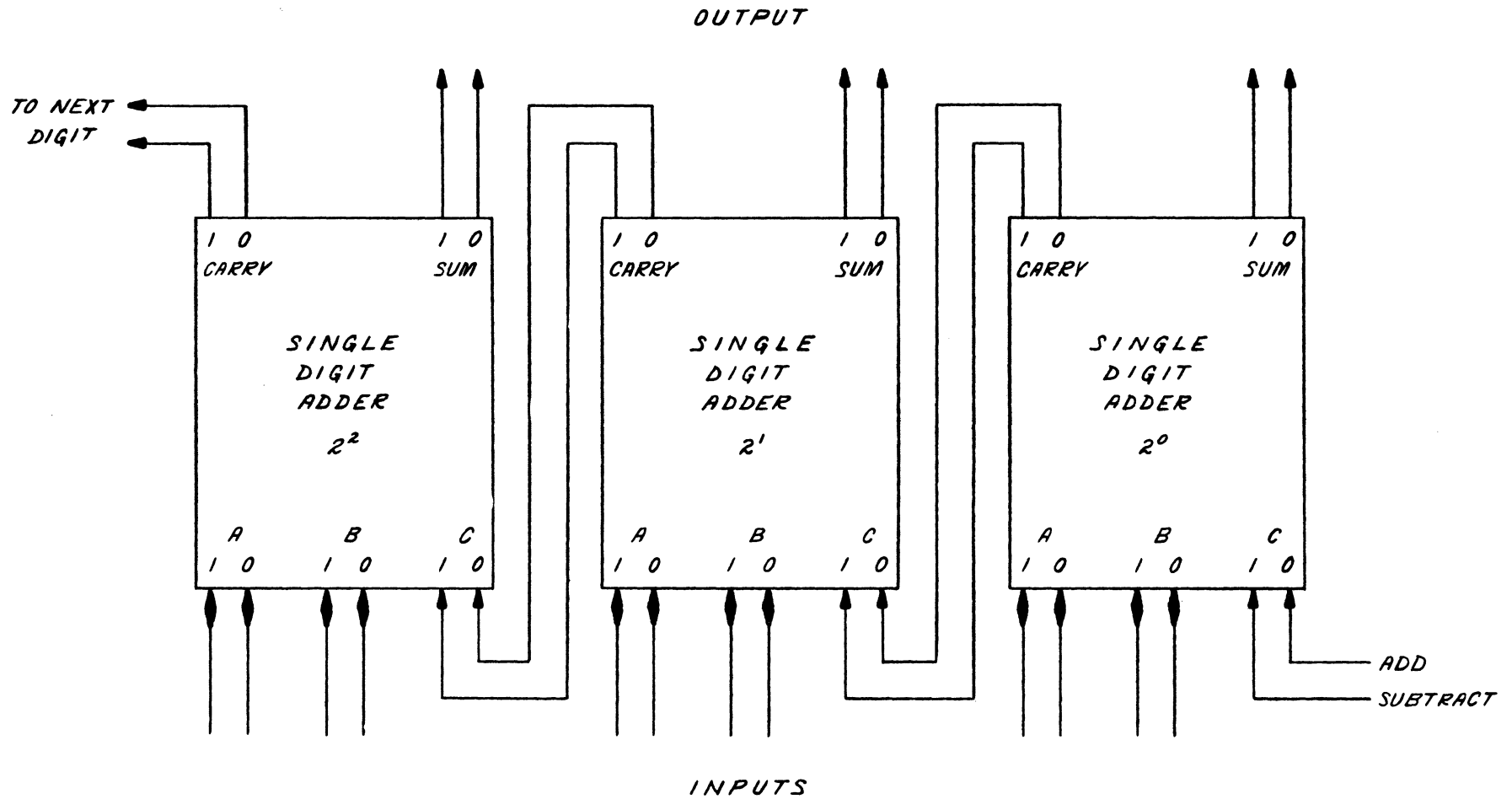


FIG. VI-6
COMPLETE ADDER I

nals will drive the appropriate C input of the next digit. The carry will progress down the adder reading out the sum as it goes.

If the C-ONE input to the first digit is pulsed, instead of the C-ZERO, a 1 is automatically added to the answer. This makes possible a very simple way of using the "10's complement" method of subtracting. To subtract B from A we need only put the complement of B into the adder and pulse the C-ONE input of its first digit and the difference is read out at the sum terminals.

When the adder is used in this form, it is necessary to hold the two numbers to be added at the switch terminals during the addition operation. It is often more useful to be able to put the numbers in and get the sum out in sequence. For example, one might want to take A out of storage and into the adder, and then do the same with B, and then put the sum of A and B back in storage.

This can be done with this switch adder by putting gated amplifiers between the digits of the adder as in Figure VI-7 and reversing the windings of the A and B inputs as was already done with the C windings. First A is read in and it switches the four cores which it has eliminated from being the answer core. Then B is read in and it switches the two cores which it eliminates from being the answer core. The amplifiers, held inoperative during read-in to keep spurious carries from going on to the next digits, are now made operative and the appropriate C input of the first digit is pulsed. This causes one of the two remaining cores in each digit column to be switched. The carry propagates along the line of digits and the sum is read out.

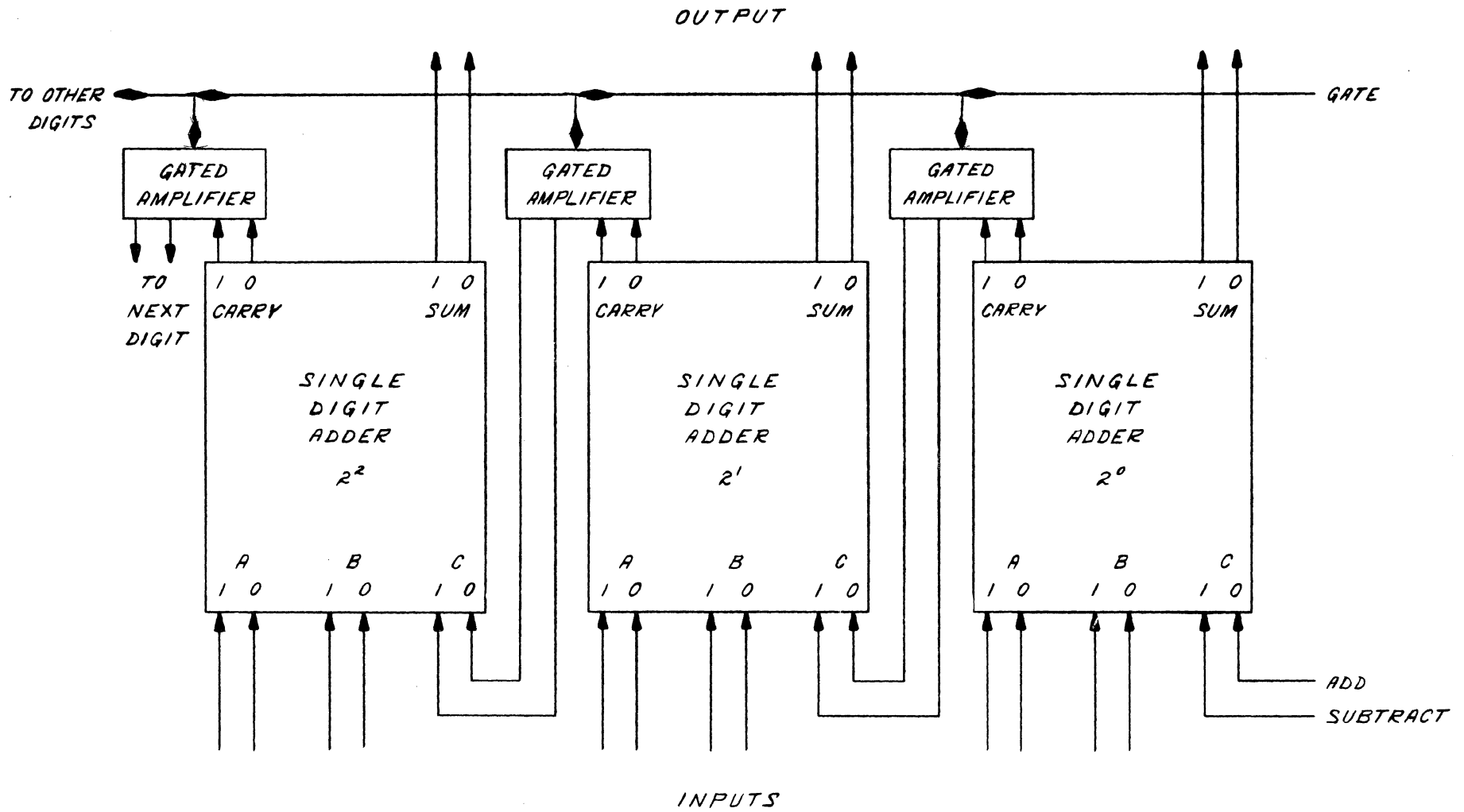


FIG VI-7
COMPLETE ADDER II

APPENDIX II FLUX-CURRENT LOOP PLOTTER

A flux-current loop plotter was constructed to facilitate this research. This unit plots on the X coordinate of an oscilloscope a voltage proportional to the alternating current which is applied to the primary winding of the core under test. The secondary voltage is integrated by a simple R-C integrator, then amplified, and applied to the Y axis. The resulting plot on the oscilloscope is the familiar flux-current loop. Figure VII-1 is a block schematic, and Figure VII-2 is a photograph of the complete unit.

The 60-cycle power line acts as a source of current which can be controlled by a variable autotransformer. A second transformer isolates the unit from the line and steps up the current. Deflection voltage for the current axis of the oscilloscope is developed across a resistor in series with the current source. An ammeter is placed in series with the current source so that one can calibrate the current axis.

The sample cores are mounted on plugs in order to facilitate rapid testing. When the secondary winding consists of a single turn, it is followed by a step-up transformer. However, when a number of turns are used in the secondary, the transformer is not needed. The signal from the secondary is integrated, amplified, and applied to the Y axis of the scope.

Since the signal amplitude is greatly attenuated in the integrator, the loss in amplitude must be compensated by an amplifier. The signal is integrated before amplification because it is easier to

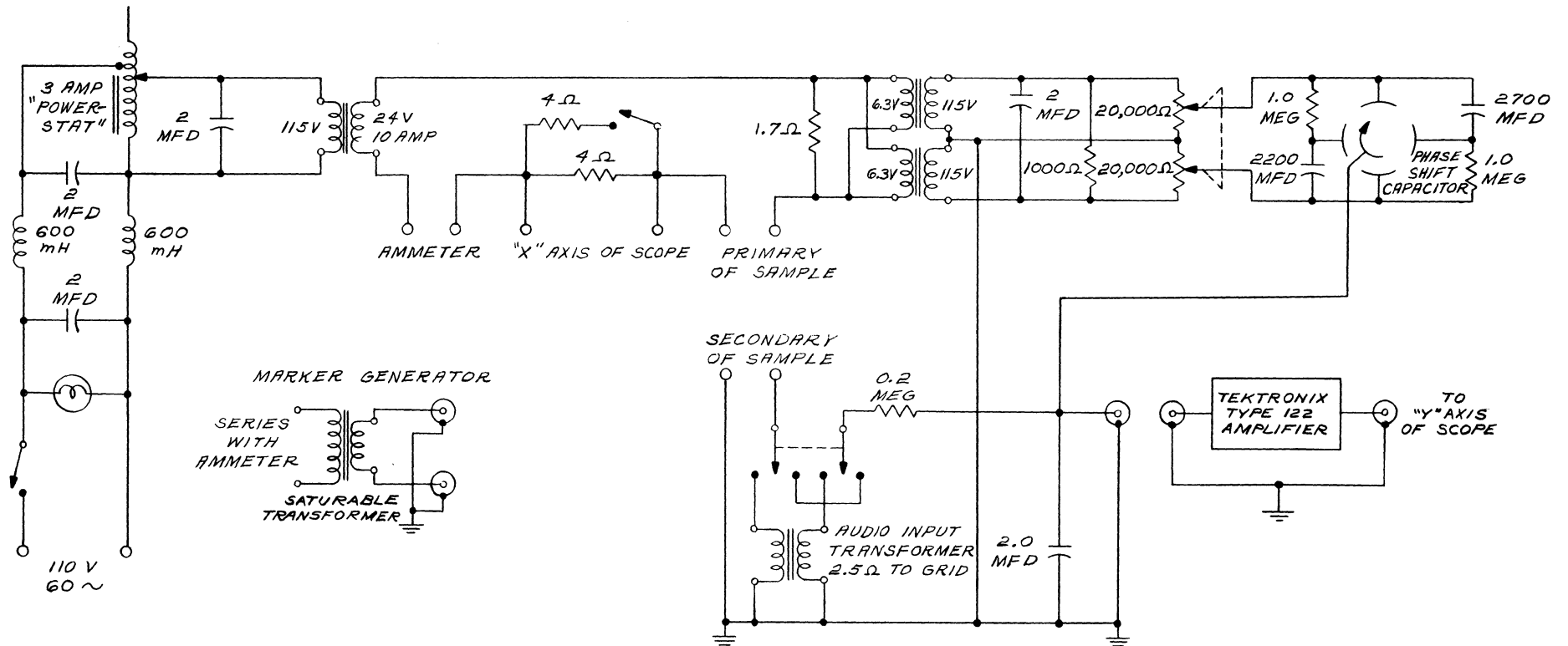


FIG. VII - 1

CIRCUIT SCHEMATIC, FLUX-CURRENT PLOTTER

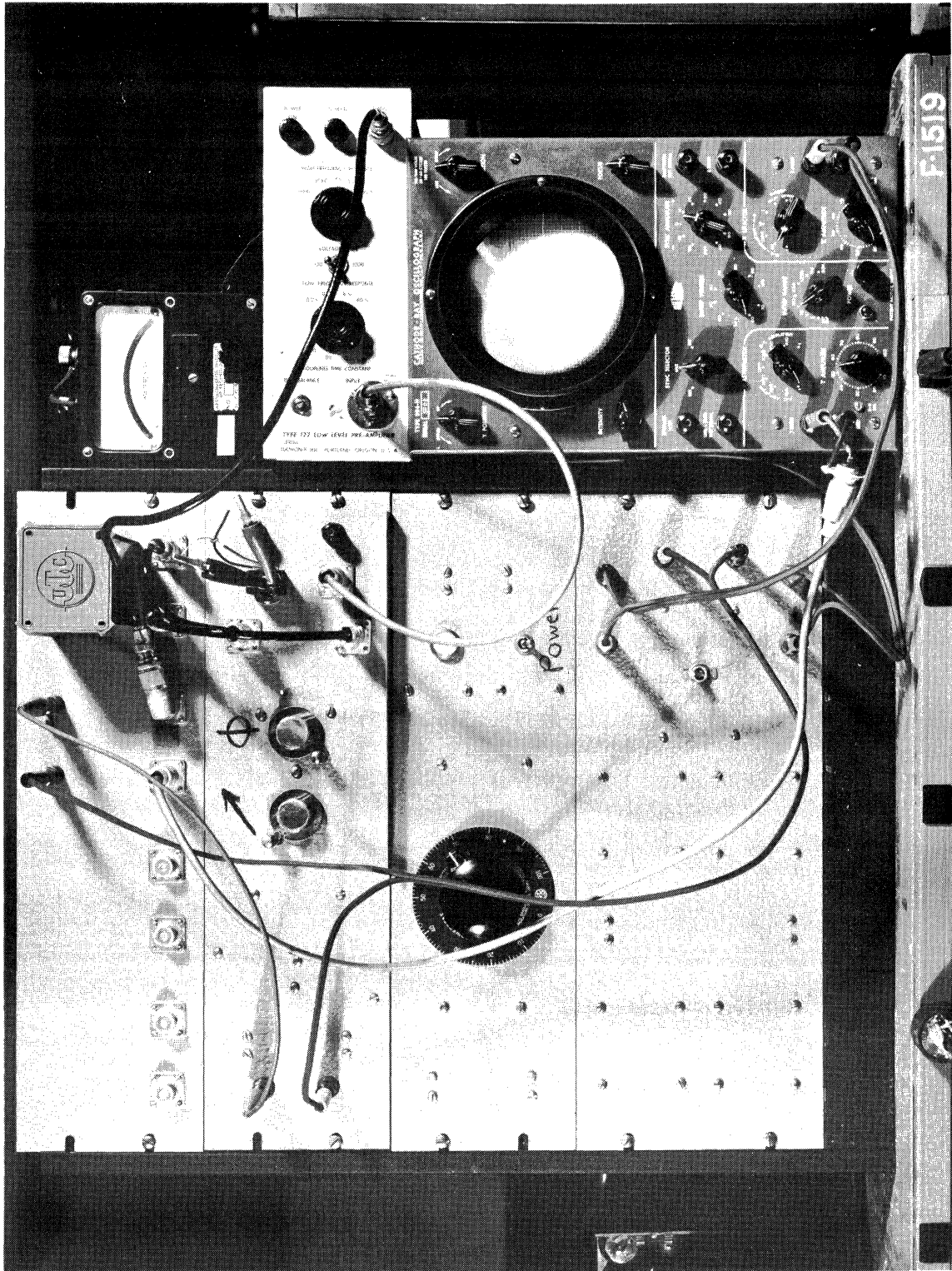


FIG VII-2
FLUX-CURRENT LOOP PLOTTER

obtain the necessary gain at low signal levels. The frequency-response characteristics of the amplifier are also less critical because there are significantly fewer high-frequency components in the integrated signal. A commercial battery-operated low level amplifier (Tektronix type 122) with a gain of 1000 is used.

When a spurious 60-cycle signal, such as that due to hum pickup in the input transformer, is introduced into the output signal of the core, the forward and return traces of the loop beyond saturation are separated as in Figure VII-3 or Figure VII-4. This spurious signal may be cancelled, by the addition of a corrective component, to yield the result shown in Figure VI-5. Phase shift in the 60-cycle component of the signal can also be compensated by this corrective component.

The corrective component is obtained from two step-up transformers in series with the current source, and hence is roughly proportional to the current applied to the primary of the sample. A 20,000-ohm dual potentiometer adjusts the amplitude of the corrective component and a phase-shifting capacitor adjusts its phase. The corrective component is applied directly to the integrator.

A small saturable transformer has been included in the plotter to produce markers on the plot that indicate zero-current points. The primary of the transformer is put in series with the ammeter so that it produces a pulse of voltage as the current in the primary of the sample goes through zero. The secondary of the saturable transformer is in series with the output of the amplifier and

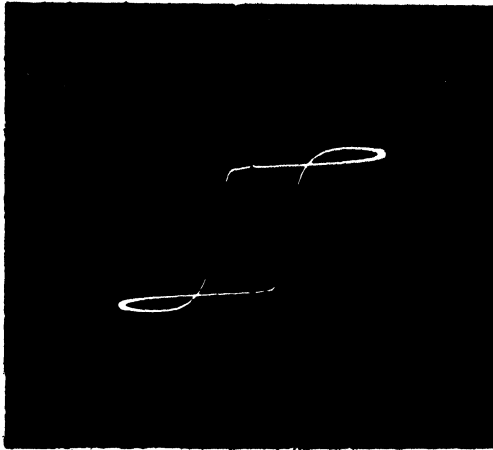


FIG. VII-3
LOOP NOT COMPENSATED



FIG. VII-4
LOOP NOT COMPENSATED

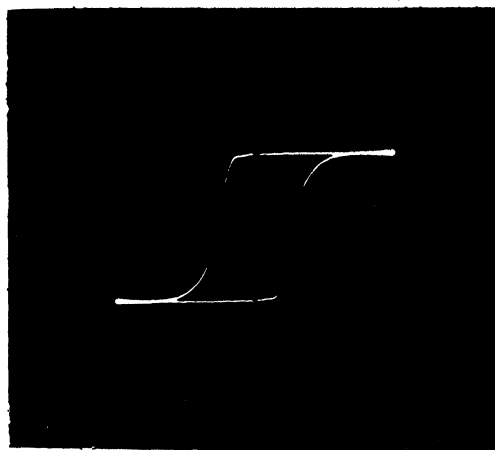


FIG. VII-5
COMPENSATED LOOP

the input of the scope. These markers are particularly useful in determining the zero-current points of biased loops such as those in Figures II-7 and II-8.

This unit is simple to operate and results can be obtained quickly. When the step-up transformer is used between the core and the integrator, large plots can be obtained from even the smallest ferrite samples with only a single secondary turn.

APPENDIX III MAGNETIC MATRIX SWITCH II

Another multi-position matrix core switch, quite different from the one discussed in this report, is possible using significantly fewer cores. This switch does not have the general applicability of the switch previously discussed because current is switched to all but the selected output instead of to only the selected. The use of this switch is further limited by the fact that the outputs are not equal in amplitude. There are, however, a number of applications for this switch — one of these being the case in which the switch is to cut off all but one vacuum tube.

Figure VIII-1 is a diagram of this switch. All the cores are driven from a common source, but one core in each digit is saturated by a control winding and so does not pass the driving signal on to its secondaries. The secondaries are arranged in a binary scheme in such a way that when a binary number is set up in the mechanical switches there is no voltage at the output terminal corresponding to the number in the mechanical switches. All the secondaries in series with this output are on saturated cores.

An alternate to this switch is shown in Figure VIII-2. Here, instead of driving all the cores and saturating specific ones, only the desired cores are driven. It is, therefore, not necessary that the cores be saturable.

The originally proposed matrix switch requires 2^n cores for a 2^n position switch. The switch discussed here requires only $2n$ cores

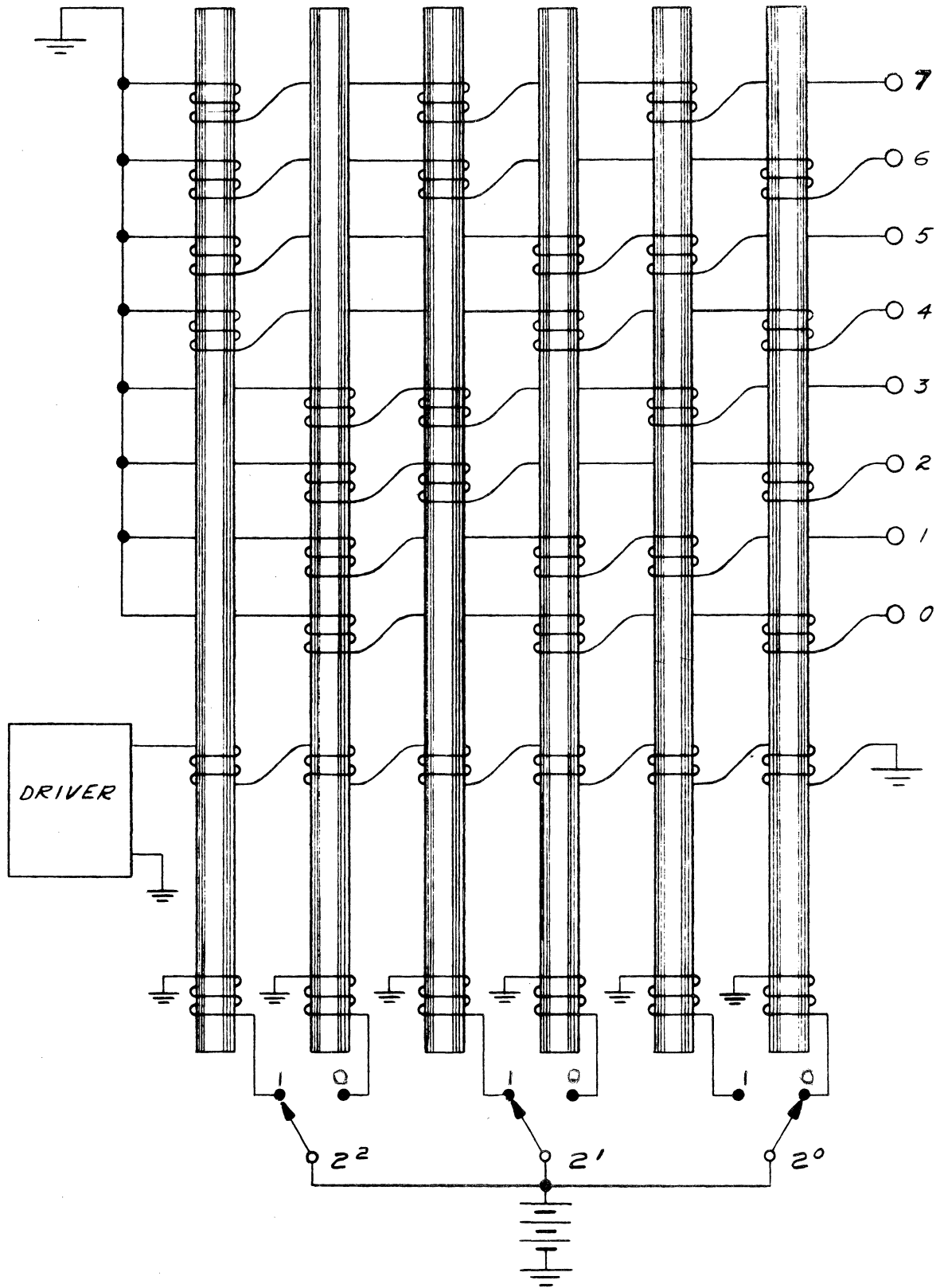


FIG VIII-1
 MAGNETIC MATRIX SWITCH II

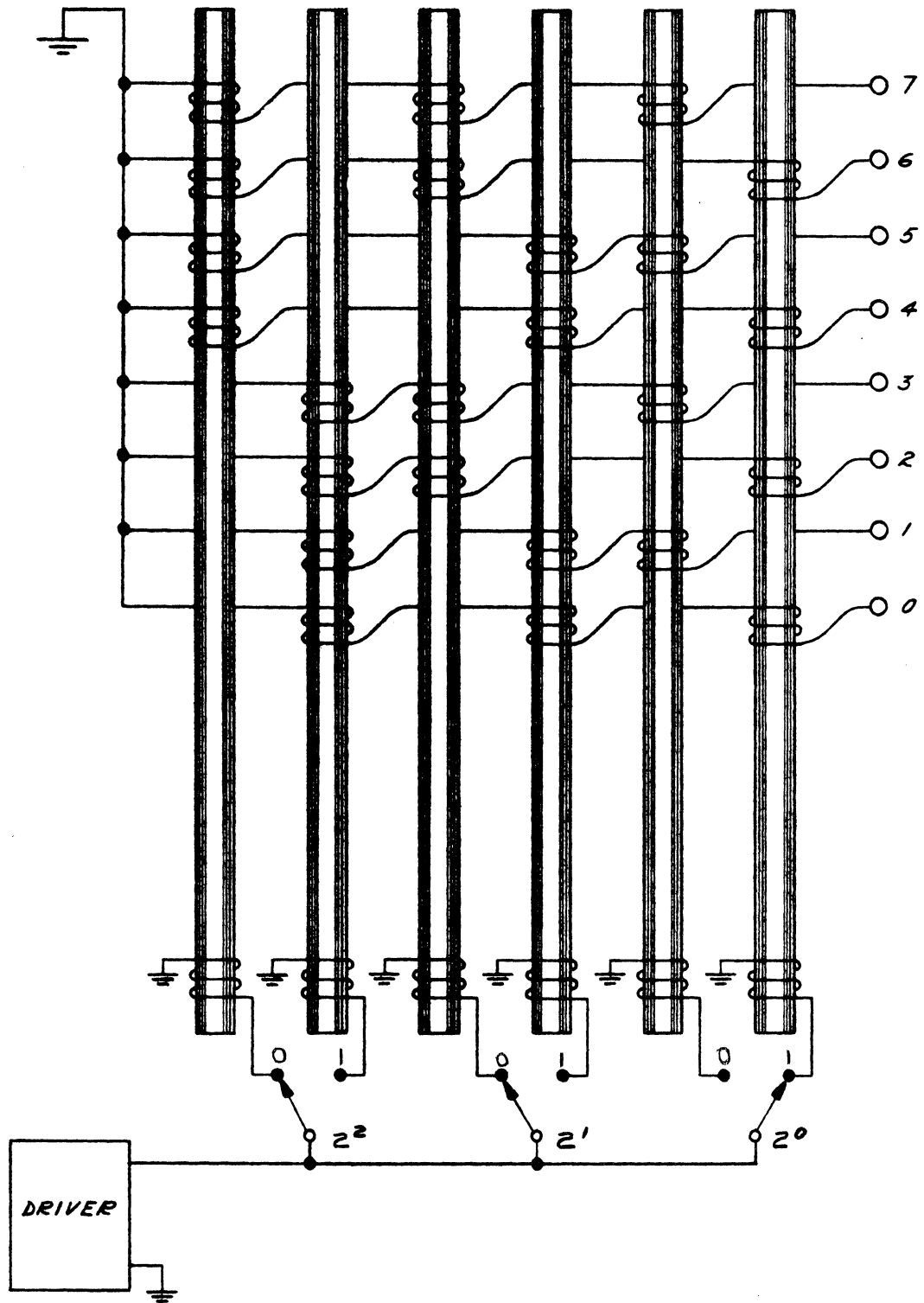


FIG VIII-2

MAGNETIC MATRIX SWITCH II
(ALTERNATE)

for the same number of positions. The latter switch also has the advantage that the control current flows through only one winding. The large number of control windings in series in the original switch is one of the factors limiting its speed of operation.

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