Report R-220

ANALYSIS AND DESIGN OF A DIGITAL-TO-ANALOG DECODER

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FOREWORD

Because it treats a subject of widespread current interest, this thesis report, which has had only limited distribution, is being published as a Digital Computer Laboratory R-series report. Digital computers are finding rapidly increasing applications to the control of physical systems of many kinds. The input to such systems must be in analog form such as an electrical voltage or a shaft position. The unmodified output of the digital computer is a set of numerical digits. Before this digital information can be fed into the control system, it must be translated into analog form. One device for this conversion is the digital-to-analog decoder described in this report.

Signed Robert L. Walquist
Robert L. Walquist

Approved .....
Jay W. Forrester

ABSTRACT

"Analysis and Design of a Digital-to-Analog Decoder"

by

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The purpose of this thesis is to study the general problems associated with the various types of digital-analog conversion equipment and, by means of this study, to design a high-accuracy digital-to-analog decoder without sacrificing speed of response.

In choosing a particular form of conversion device for use in a system, the following characteristics must be considered:

1. The general applicability of the input to or output from the conversion device;
2. The accuracy of the conversion;
3. The sensitivity of the conversion;
4. The freedom from drift of the conversion device;
5. The time taken for a single conversion;
6. The amount of equipment necessary for single and multiple conversion channels.

The internal operation of the conversion device may be characterized by only two of these quantities:

1. The number of quantizing levels (the static conversion accuracy);
2. The conversion time.

Comparison of these two characteristics of digital-analog conversion devices to the characteristics of analog systems indicated that quantization error is similar to noise, while conversion time is similar to bandwidth.

The problem of conversion is one of comparison or matching of the input and output signals of the conversion device. The three fundamental ways in which this comparison may be accomplished are:

1. Serial matching of each quantizing increment;

2. Serial matching of each binary digit;

3. Parallel matching of all digits (simultaneous comparison).

These three methods of comparison are completely analogous to the three ways in which digital information may be transmitted.

Study of the various conversion methods indicates that a binary-weighted decoder which uses equal-valued current sources connected to a binary-weighted ladder network is one of the best solutions to the digital-to-analog decoder problem. Experimental design and testing of 2 stages of a proposed 10 stage decoder of this type gave the following results:

1. With only $1\frac{1}{2}$ twin-triodes used for each stage, accurate current sources were built, each of thich includes a storage medium (an unsymmetrical flip-flop) for holding digital information.

2. A maximum output voltage of 100 volts, without the use of amplifiers, may be obtained from the decoder with an accuracy of 0.1 percent (10 binary digits). Recalibration need be carried out no oftener than every few days.

3. The time taken by the decoder to set up this accuracy of output voltage, with only a small load applied, is less than 1.5 microsecond.

4. Repeated operation of the decoder may be obtained at frequencies up to 125 kilocycles.

Transmission of the output voltage of a decoder becomes an important problem whenever many paralleled devices are to receive this voltage. Special transmission schemes, such as three-conductor transmission lines, may be used to retain the rapid response and accuracy of the decoder output voltage but only at the expense of increased complexity of equipment and greater power loss.

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ANALYSIS AND DESIGN

OF A

DIGITAL-TO-ANALOG

DECODER

1.0 INTRODUCTION

A digital-to-analog decoder is a device which converts or changes a quantity represented by a set of numerical digits into an analog quantity such as an electrical voltage or shaft position. The digital-to-analog decoder is one of two general classifications of digital-analog conversion equipment, the other classification being the inverse or encoding equipment. Digital-analog conversion may be thought of as an extension of the field of analog-analog conversion which deals with the problem of changing a quantity, such as light intensity, into an analogous quantity, such as a shaft position. A fundamental difference, however, is introduced because of the fact that the digital representation of a quantity, by its very nature, can only assume discrete values. That is, if the quantity to be represented digitally falls between two numerical values, it must be represented by one or the other of these two values and not by some intermediate value. Analog quantities, on the other hand, may assume an infinite number of values inside of the finite range through which they vary. It thus becomes the problem of the digital-analog conversion equipment to interconnect an analog system which has the possibility of conveying an infinite amount of information to a digital system which can convey only a limited amount of information, this amount being directly dependent upon the range of numbers handled by the digital system.

1.1 Uses of Digital-Analog Conversion Devices

Devices which convert one analog quantity into another analog quantity have been widely used where one form of analog information

is more easily measured and controlled than others. One might well ask: why the need of converting between analog and digital information? The following three examples should help to answer this question.

1.11 Digital Computer Control Systems

Before the advent of high-speed digital computers into the fields of electronic control and simulation, analog computers were used for performing complex and varied operations upon the information being handled by such control and simulation systems. Since these systems operate on analog information, as do the analog computers, the need for conversion equipment is only that of converting one analog quantity into another. However, analog computers are limited in their accuracy, cannot deal with complex problems involving several independent variables, and are restricted to performing a given set of operations upon the information received by them. In order to overcome these limitations and especially to allow the computer to make decisions as to what it will do with the information it receives, digital computers have been introduced into these fields.

With the introduction of digital computers into control and simulation systems, a new problem arises. Digital computers perform operations upon discrete values of input information (as represented by a sequence of numbers), whereas the control or simulation system external to the computer uses continuous information such as voltages or shaft positions. In order, therefore, for the digital computer to be connected into these systems, it is necessary to

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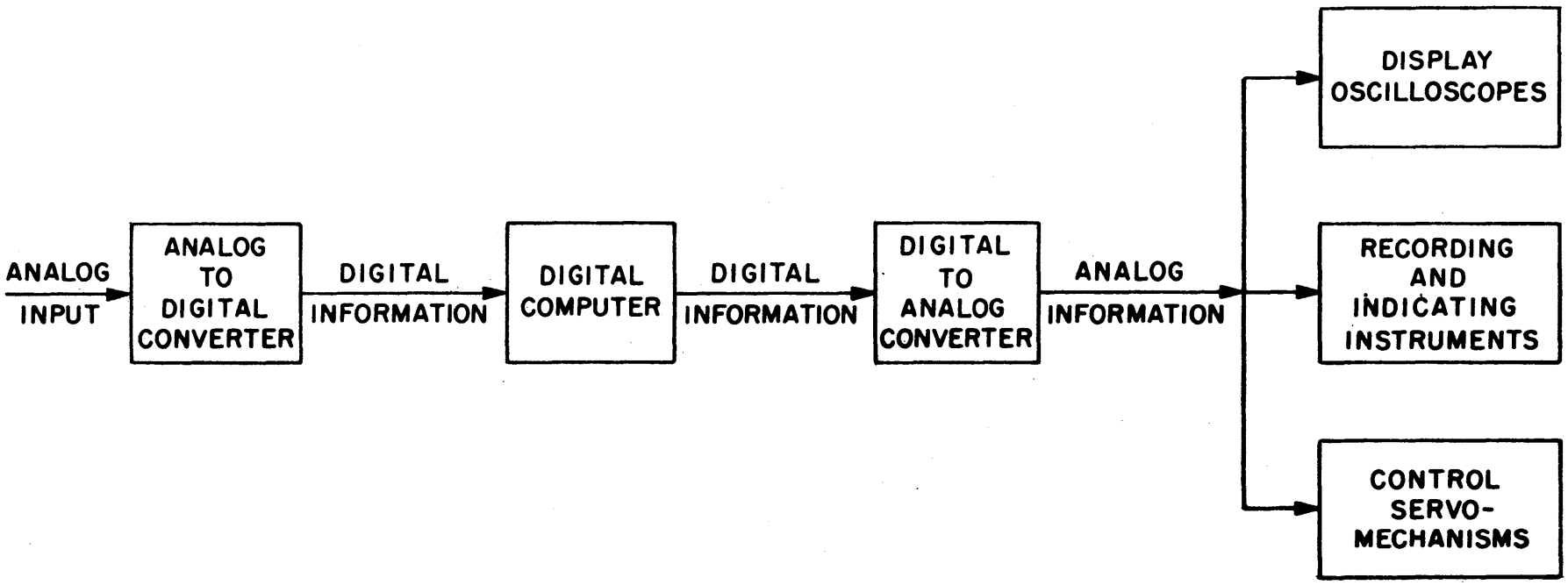

FIG. 1

USES OF DIGITAL-ANALOG CONVERSION DEVICES

(1) DIGITAL COMPUTER CONTROL SYSTEMS

introduce devices which will convert continuous analog information into digital information and vice versa. The replacing of analog equipment by a digital computer thus requires not only a knowledge of the computer characteristics but also a knowledge of the digital-analog conversion devices through which the computer is connected to the rest of the system.

A control or simulation system utilizing a digital computer is shown in Figure 1. Analog information is received by a conversion device which changes this analog information into a form of digital information usable by the digital computer. The digital computer then processes this information, yielding the digital results of this processing at its output. These digital results are then changed into analog information by a second conversion device, the output of which is connected to the desired analog equipment.

1.12 Telemetering and Servomechanism Control Systems

In some telemetering problems, the accuracy of the quantity being telemetered is often of great importance. Noise, occurring during the transmission of the information as a continuously variable quantity, reduces the accuracy obtainable at the receiving device to a value which may be considerably less than the accuracy of the transmitted information. However, it is possible to convert the continuous information into discrete or digital information at the transmitting end and send this digital information in the form of

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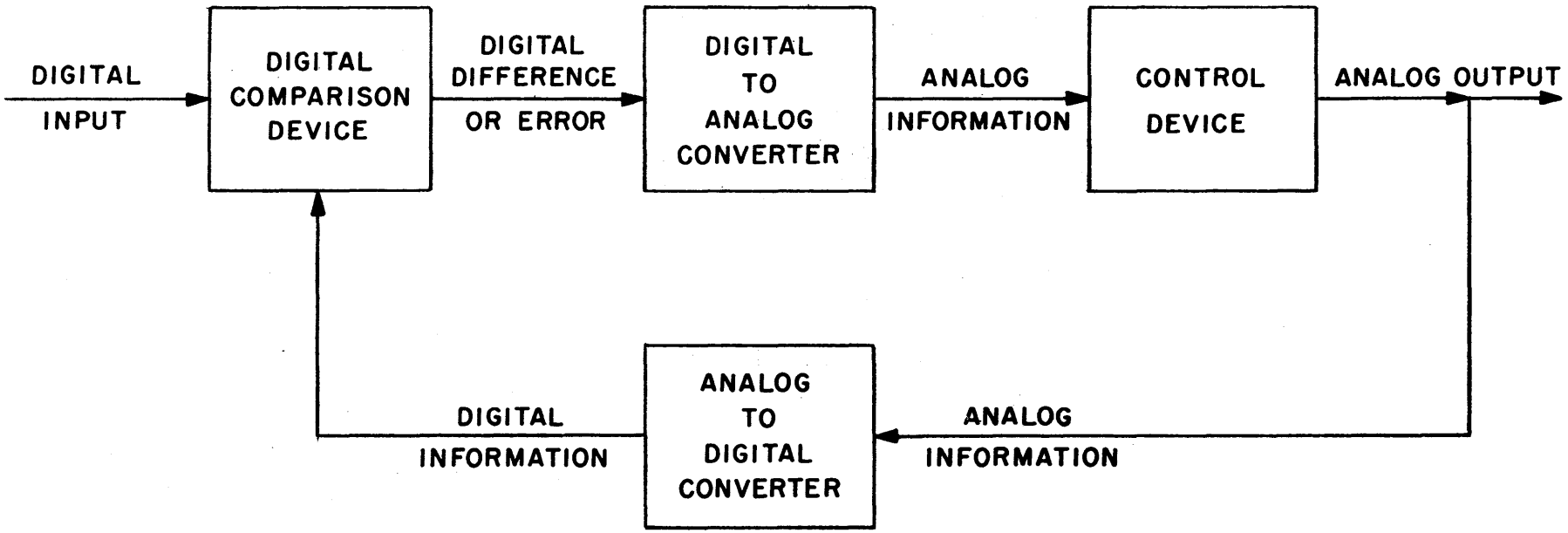


FIG. 2

USES OF DIGITAL-ANALOG CONVERSION DEVICES

(2) SERVOMECHANISM CONTROL SYSTEMS

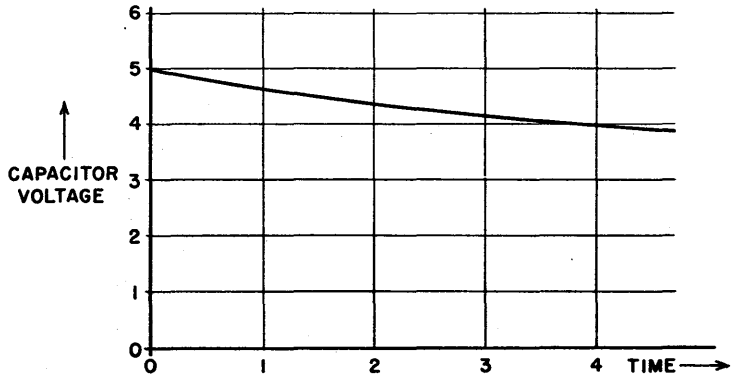
time sequences of pulses, multiplexed frequencies, pulse positionings, or by some other method. Such transmission schemes can reduce transmission noise to a relatively insignificant level.

A receiving device for handling telemetered digital information might appear in the form shown in Figure 2. Here a servomechanism or control device is operated by comparing the input digital information with digital information proportional to the analog output of the device. Comparison might be made of digital quantities rather than analog quantities in order to achieve a higher degree of accuracy.

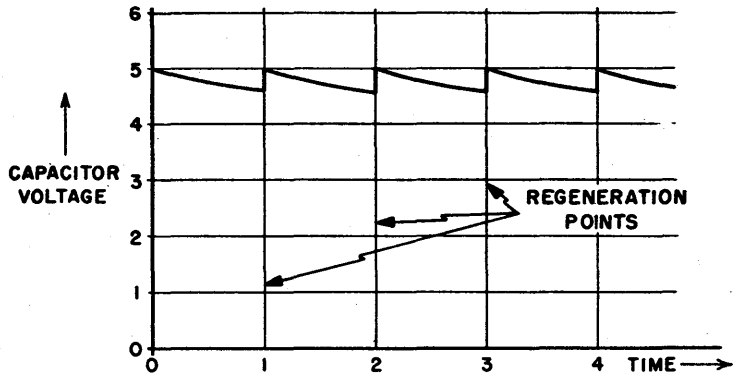
1.13 Information Storage

In systems where it is desirable to store information for some arbitrary length of time, storage of continuous-valued quantities becomes quite difficult due to drift or decay of the stored quantity. An example of the decay of a voltage stored on a capacitor is shown in Figure 3-A. Due to leakage resistances both in the capacitor and the associated circuitry, the capacitor voltage will decay in an exponential manner. Such a method of storage is adequate only if the discharge time constant of the circuitry is considerably greater than the time interval over which the voltage is to be stored.

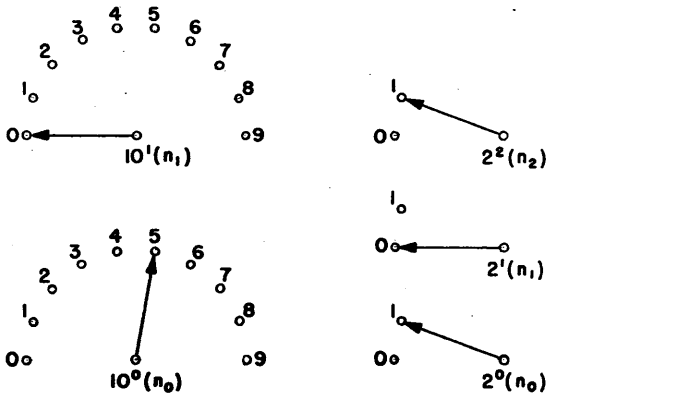
The same capacitor can be made to store information indefinitely if, in some manner, the decaying voltage can be returned to its original level after it has drifted from this value. However, in order to do this, it is necessary to quantize the original voltage (change it from a continuous quantity to a discrete quantity) so



(A) INFORMATION STORED AS A CONTINUOS ANALOG QUANTITY



(B) INFORMATION STORED AS A DISCRETE OR QUANTIZED ANALOG QUANTITY



$I = k[n_0 \times 10^0 + n_1 \times 10^1 + \cdots] = k[5+0\times10] = 5k$

BASE 10 NUMBER SYSTEM

$I = k[n_0 \times 2^0 + n_1 \times 2^1 + n_2 \times 2^2 + \cdots] = k[1+0\times2+1\times4] = 5k$

BASE 2 NUMBER SYSTEM

(C) INFORMATION STORED AS A DIGITAL QUANTITY

FIG. 3
USES OF DIGITAL-ANALOG CONVERSION DEVICES

(3) STORAGE OF INFORMATION

that any drift can be recognized and corrected. Such a scheme is shown in Figure 3-B where the magnitude of the decayed voltage is sensed and is increased (as indicated by the regeneration points) until it equals the next larger quantizing unit.

The information may also be stored as a digital quantity as shown in Figure 3-C. Here, the storage medium is assumed to be drift free, such as a rotary switch, so that regeneration is not necessary and the information may be stored indefinitely. Two different methods of storing this digital information are given: one of these requires the use of a group of storage units, each having 10 discrete and stable storage positions; the other requires the use of a larger group of storage units but with each having only 2 discrete and stable positions.

1.2 The Analysis of Conversion Devices as Presented in This Paper

The examples given in the previous section show three of the various ways in which digital-analog conversion devices may be employed. In each of these usages it becomes important to know the characteristics of the conversion device, including a knowledge of the analog and digital input-output information. The various sections of this paper attempt an analysis of the field of digital-analog conversion equipment, with emphasis placed upon the problem of designing a binary-weighted decoder.

Section 2 of this paper discusses in a general way the various characteristics of conversion devices including the analog input to or output from the conversion device. This discussion is

presented from an engineering point of view, stressing the requirements which are important when one is designing conversion equipment. It also gives a common background upon which a rough comparison can be made between different types of conversion devices.

Section 3 analyzes the three basic methods by which digital-analog conversion equipment may operate in order to match or compare the input and output signals. It is also pointed out that these three methods are identical to the three ways in which digital information may be transmitted. The number of quantizing levels (static conversion accuracy) and the conversion time are shown to be the important parameters for discussing the internal operation of the conversion device. It is pointed out that these quantities are comparable to the signal-to-noise ratio and bandwidth of analog systems. Two brief examples are given in order to show the extreme cases which may arise when a digital-analog conversion device is to be matched to the remainder of a system.

With the information presented in Sections 2 and 3 as a foundation upon which to build, and for the reasons given therein, Section 4 approaches the problem of designing a suitable decoder by the use of parallel-channel, binary-weighting methods as distinguished from incremental methods. Two methods of binary weighting are analyzed: the use of voltage sources as the weighting elements, and the use of current sources as the weighting elements. The engineering difficulties encountered with each of these methods are discussed and an evaluation is made of their relative merits.

Section 5 discusses the final design and testing of 2 stages of a proposed 10 stage binary-weighted decoder. For reasons given in Section 4, current sources incorporating a "holding" or storage medium are used for each decoder channel (each binary digit). The results achieved with this decoder are evaluated in terms of the principles stressed in Section 2, with special emphasis being placed on accuracy, drift, speed of response, and ease of calibration.

Section 6 discusses briefly some of the engineering problems which would be encountered if a binary-weighted decoder is used as an encoding device to change analog voltages into an equivalent binary number. The problem associated with the accurate and rapid transmission of the output voltage of a decoder is also considered along with some of the possible means for solving the problem. The section ends by summarizing the material covered in this report, pointing out some of the limitations, and suggesting possible directions for further study.

2.0 IMPORTANT ENGINEERING REQUIREMENTS OF DIGITAL-ANALOG CONVERSION EQUIPMENT

The problem of developing a method of comparison for any type of equipment is a difficult one, since the factor which ultimately determines a selection is the cost. If several pieces of equipment will all adequately do a specified task, then that piece of equipment which is the least expensive is chosen. However, the principal difficulty here is in the meaning of adequate. Different applications must meet different requirements; and even for the same application, what seems adequate for one user may not be adequate for another. Unless the exact usage to which a piece of equipment is to be put is known beforehand, cost is an inadequate means of comparison. For this reason, this chapter discusses several of the important design considerations for digital-analog encoding and decoding devices.

The design of any system that is to either code or decode digital information must consider the following:

1. The general applicability of the input to or output from the conversion devices;
2. The accuracy of the conversion;
3. The sensitivity of the conversion;
4. The freedom from drift of the conversion device;
5. The time taken for a single conversion;
6. The amount of equipment necessary for single and multiple conversion channels.

The following sections of this chapter consider each of these items briefly. Wherever possible, reference is made to the achievements and limitations of already existing conversion equipment.

2.1 The Input and Output of the Conversion Device

Since a digital-analog conversion device must deal with both analog and digital representations of information, it is important to determine which of the many possible forms these representations should take. Analog information may assume a multiplicity of forms, including such things as position, velocity, pressure, voltage, current, etc. Digital information may likewise be expressed in several ways, two of which were shown in Figure 3. Two of the most useful forms (one digital and one analog) are discussed below.

2.11 Digital Information Represented as a Binary Number

The almost universal way to represent digital information is by means of a decimal number (base 10 system) which uses the digit values 0 through 9. The position of a digit in the number determines the power of 10 by which that digit is to be multiplied. As an example, consider the number 54; the decimal representation of this number is:

$$N_{10} = n_1 \times 10^1 + n_0 \times 10^0 = 5 \times 10^1 + 4 \times 10^0 = 54$$

However, it is possible to use other forms of representing digital information by adopting a new number base. Consider, for example, the

use of a binary (base 2) form of number representation. Here, instead of the 10 distinct digital values of the decimal system, we have only 2 distinct values -- 0 and 1. The same decimal number 54 would be written in the binary system as follows:

$$N_2 = n_5 \times 2^5 + n_4 \times 2^4 + n_3 \times 2^3 + n_2 \times 2^2 + n_1 \times 2^1 + n_0 \times 2^0$$

$$N_2 = 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 110110$$

Two conclusions can be drawn from the above comparisons:

1. The smaller the number base, the larger the number of digits needed to specify a given number;
2. The smaller the number base, the fewer the number of values each digit must assume.

This latter consideration is a very important one when high speed and high reliability are desired. Since electronic equipment is almost always used in high speed devices, and since this equipment works most reliably in an off-on (0-1) fashion, it is customary to use the base 2 system for the representation of digital information in conversion equipment.

2.12 Analog Information Represented as a Voltage Amplitude

Considering only the general applicability of the input to or output from a conversion device, the advantage of using voltage as the analog parameter is immediately apparent. Electrical transducers which convert pressure, strain, temperature, light intensity,

color, sound intensity, pitch, pH (hydrogen ion) content, and an almost endless variety of other quantities into analog voltages are quite common. Also, a voltage output can be used for deflecting an oscilloscope beam, for operating a recording galvanometer or visual indicating instrument, or, in conjunction with a servo-mechanism, for positioning a shaft.

Several schemes have already been devised and tested for changing a set of binary digits into an analog voltage. [1,4,5,6,12, 17, 20, 24].* Similar work has been done on the converse problem of changing an analog voltage into a set of binary digits. [6, 12, 18, 19, 21, 24]. Besides the use of voltage as the analog parameter, systems have been considered and designed wherein a shaft position is used as an indication of the analog parameter. [20, 22, 23, 24] One of the disadvantages of this latter technique is the difficulty of obtaining the analog input quantities in the form of shaft positions (unless they already occur as such) without first having to convert to an analog voltage. A system which eliminates the intermediate step of conversion from an analog voltage to a shaft position and then to a set of binary digits should be more advantageous, since the introduction of each conversion step in the process introduces another source of error and the possibility of an increased complexity of the conversion equipment.

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* Superscripts refer to items in the Bibliography.

2.13 "Holding" of the Analog Output of a Decoder

An important consideration in any digital-to-analog conversion is the "holding" or "non-holding" property of the output. If the output of the conversion device is "holding" from one digital input to another, a steady value of output is obtained for each digital conversion and this value of output is maintained constant, regardless of the time elapsed before the next digital input.

In systems where the digital input to the conversion device is uniformly spaced in time, and adjacent pieces of digital information are sufficiently close together, the consideration of a "holding" or "non-holding" output is not as important, since the average value of the output quantity can be directly related to the digital input. Even here, however, the "non-holding" character of the output will be important if the digital input changes rapidly, for an averaging device is effectively a low pass filter and must necessarily have a time delay over which it averages a reading.

The problem is even more acute when the digital input to the conversion device is randomly spaced in time. Either the conversion device must maintain constant the magnitude of the analog output, or else the analog receiving device must be able to store information. In either case, storage of some form must be utilized. Since most analog devices do not have the requisite storage medium, it is desirable to place this burden upon the conversion device.

2.2 Accuracy of Conversion

A second important consideration in the design of a conversion device is the accuracy of the conversion. Methods have been suggested for obtaining a high degree of accuracy in both the analog-to-digital conversion[22] and in the digital-to-analog conversion[17]. Such methods rely on the use of a fine and coarse analog evaluating device. As outlined, these methods give a theoretical accuracy of 0.01 percent or better, but the difficulties of building and stabilizing such devices have not been thoroughly studied. Methods which have actually been tried, and which do not use a coarse and fine level of evaluation of the analog quantity, more generally have accuracies of around 1 or 2 percent.[5, 12, 17] However, transducers, output meters, and recorders have an accuracy of about this same order of magnitude -- generally around 1/2 to 1 percent. (Bridge balancing schemes will give a much higher sensitivity to parameter changes, but the reference level of the variable parameter usually has an accuracy of only 1/2 to 1 percent.) Thus, an accuracy of conversion of around 1 to 2 percent rather than the accuracy of the analog device would be the limiting factor. It is desirable to have the overall accuracy of conversion approach the accuracy of the transducers or output devices, rather than have the accuracy limited by the conversion device.

2.3 Sensitivity of Conversion

Besides the accuracy, the sensitivity of the conversion device is important -- by sensitivity is meant the ability of the conversion device to reproduce small changes in the digital or analog input quantity. It is quite often desirable to have a sensitivity which is considerably greater than the accuracy of the conversion device. Sensitivities as high as 1 part in 1,000 have been obtained[20], but a more usual figure is somewhere around 1 part in 200 or 300.[6, 12, 17, 23]

High sensitivity may be obtained from an analog voltage to digital conversion device by utilizing two input channels from each transducer. One input channel is used to establish the reference level of the input quantity, while the other input channel is connected in a sensitive bridge circuit such that the input to the conversion device gives only the deviation of the parameter from a fixed reference level. This second input channel could then give a very high sensitivity; but such a scheme would not increase the overall accuracy of the conversion since this accuracy would be set by the input channel establishing the reference level. Since the input channel establishing the reference level must yield a coarse bridge adjustment and since the sensitivity of the bridge should not vary with the reference level, difficulties would be encountered in such a system if the reference level is forced to vary over wide limits.

2.4 Freedom from Drift

The drift of most of the high-sensitivity systems so far developed has not been checked closely enough to determine to what extent this drift will affect the results. If a conversion system has to be frequently adjusted and recalibrated due to such things as zero drift, sensitivity to power supply voltage fluctuations, and aging components, the usefulness of the device is critically handicapped. Ideally, the system should not have to be checked after it is once installed; however, such stability of operation is generally not forthcoming, especially where high accuracy is desired.

This need for calibration, especially in the more accurate systems, often requires an increased system complexity in order that a simple checking and recalibrating scheme may be incorporated. This checking feature has often been neglected in the past, with the result that the utility of the devices has been seriously handicapped.

2.5 Conversion Time

For a computer operating with analog inputs and outputs, the time of conversion of these quantities becomes another important parameter in determining the utility of the conversion device. Analog-to-digital conversion times as short as 10 microseconds have been obtained in a Pulse Code Modulation system by the use of a special beam deflection coding tube.[12, 18, 19] The receiving end of

the system converts a time sequence of pulses to analog voltages in the same length of time.[1] Digital-to-analog conversion times of around 3 microseconds have been obtained with the system used at Project Whirlwind for deflecting the electron beams in the electrostatic storage tubes.[5] Conversion times, however, generally run around 150 to 250 microseconds.[17, 20]

The higher the rate at which the computer can sample the several analog inputs and adjust the several analog outputs, the more versatile the computer will be. Certainly the coding and decoding times will determine the total number of analog signal inputs and outputs that can be obtained during a given time interval. This in turn limits the product of the number of channels of information and the sampling rate per channel. High conversion speed is an important quantity when designing any conversion device; however, as will be pointed out in the next section, accuracy of conversion and conversion time are interrelated and may require that a compromise be made in the one or the other.

2.6 Amount of Equipment Needed

If a system is to be practicable, both the amount of equipment necessary for a single conversion channel and the additive equipment necessary for handling several conversion channels must be considered. Quite often, the additive equipment per added channel can be reduced by increasing the amount of equipment needed for a single conversion channel. Such matters must be evaluated in terms

of the probable number of conversion channels to be used, with the idea in mind of reducing the net amount of equipment and thus the net cost.

One additional factor must be considered when multiple conversion channels are used -- this is the difficulty of switching analog quantities which are amplitude sensitive. Several schemes have been devised for getting around this difficulty. The amplitude sensitive analog quantity often is used to phase modulate[20] or frequency modulate[22] an alternating voltage waveform. The switching is then done on this modulated voltage, the switching device being insensitive to phase and frequency variations. Other methods involve the utilization of time positioned pulses to represent the analog magnitude, all switching operations being done on these pulses.[17, 20]

The methods mentioned above have one inherent disadvantage -- they must perform an additional conversion with the possibility of introducing additional errors. Up to the present, a satisfactory solution to this problem has not been obtained.

2.7 Brief Historical Summary of Digital-Analog Conversion Equipment

With the various engineering requirements for digital-analog conversion equipment firmly in mind, it is worthwhile to compare several of the devices which have been designed in this field. The following tables list the basic principles of operation, and a few other important

Developed by	Type of Input	Principle of Operation	Accuracy	Time of Conversion in microseconds	Amount of Equipment Duplicated for Multiple Inputs*
Goodall Ref. 6	Voltage Magnitude	An amount of charge is removed from capacitor corresponding to largest binary digit contained in analog input. Process is continued for all smaller binary digits. Time-positioned pulses occur as the output.	1/32	10	all
Bell Laboratories Ref. 12,18,19	Voltage Magnitude	Vertical position of electron beam in "coding tube" is determined by the magnitude of analog input. Horizontal deflection of electron beam gives time-positioned pulse output corresponding to magnitude of analog input.	1/128	10	almost all
Stabler Ref. 23	Shaft Position	Number in binary counter is changed each time shaft is moved. Counter is reversible in operation and direction of shaft rotation is sensed by means of photo cells.	1/180	Continuous Conversion of Position.	all
Sisson Ref. 20	Shaft Position	Shaft position is converted to phase-modulated signal; phase-modulated signal is converted to pulse-position modulated signal; latter signal is converted to binary number by means of binary counter.	1/360	250	approx. 1/5
Smith Ref. 21	Voltage Magnitude	Output of binary weighted voltage generator is compared with analog input voltage, and resulting error signal is used to set the voltage generator. Comparison is continued until error is less than the smallest unit of the voltage generator.	1/32	100	approx. 1/5

* It is assumed here that analog voltages cannot be switched without introducing error, and hence voltage switching is not considered when evaluating the amount of duplication necessary.

2.71 Table of Previous Coders

Developed by	Principle of Operation	Is Output "Holding" in Nature?	Accuracy	Time of Conversion in microseconds	Amount of Equipment Duplicated for Multiple Outputs*
Goodall Ref. 6	Time-positioned input pulses discharge a capacitor in binary weighted time sequence. Output is proportional to decrease of voltage across capacitor.	NO	1/32	10	almost all
Shannon-Rack Ref. 1, 12	Time-positioned input pulses cause equal current pulses to flow in a capacitor circuit. Binary weighting is accomplished by allowing capacitor to discharge to 1/2 its value between input pulses. Output is proportional to voltage across capacitor.	NO	1/128	10	all
Sard Ref. 17	Binary number is converted into a pair of time-positioned pulses by means of binary counter. Time between pulses is integrated to obtain output voltage.	NO	Approx. 1/50	Approx. 150	1/3
Susskind Ref. 20	Same principle as used by Sard above, except that time-positioned pulses are held in delay and regeneration network.	YES	Approx. 1/200	Approx. 150	1/2
Ely Ref. 4,5	Binary weighted current sources are summed in load resistance which converts sum of currents into analog voltage. This voltage is amplified to obtain usable output.	YES	1/32	3	all

* It is assumed here that analog voltages cannot be switched wihtout introducing error, and hence voltage switching is not considered when evaluating the amount of duplication necessary.

2.72 Table of Previous Decoders

quantities, for 5 decoding and 5 coding devices. The Bibliography in the Appendices of this report gives a fairly complete listing of the references dealing with these devices for those who desire a more detailed study.

Several conclusions as to the desirability of a particular conversion method may be drawn from the information presented in these tables. However, the tables do not indicate if a particular method has been exploited up to its theoretical limits. It appears as if certain of the devices could be improved in accuracy without sacrificing other factors such as time of conversion. It might be, however, that some of the methods have already been pushed to the extreme with respect to these factors. In order to obtain a better insight into the problem, the following section is devoted to an analysis of digital-analog conversion devices from the point of view of accuracy and conversion time.

3.0 ANALYSIS OF DIGITAL-ANALOG CONVERSION DEVICES

As was pointed out in Section 2, there are several important quantities to consider in connection with conversion devices. When the conversion device is viewed only from the outside and one is interested in the relationship between input and output, this is certainly true. However, if one is to describe the internal operation of the conversion device, it is sufficient to consider only the following:

1. The number of quantizing levels (the static conversion accuracy)
2. The conversion time.

As was explained in Section 1, one of the inherent characteristics of any conversion device which involves digital quantities is quantization. Quantization is introduced because of the finite range of numbers which can be handled by the digital portion of the conversion device. The second item given above, the conversion time, is introduced because there is always a certain delay between the time when an input signal is applied to the conversion device and the time when the correct output signal has been established. In analog or continuous data systems, this is generally characterized by a phase lag or time delay; in digital-analog conversion devices it is more useful to speak of this as the conversion time.

Since the above two quantities determine how fast and how accurately the components of the conversion device must operate, it is possible to derive relationships between the conversion time, the quantization accuracy, and the operating frequency for the various conversion devices. The following section gives examples of several forms of digital-analog conversion devices and shows that certain conversion methods are more restrictive in their accuracy-conversion-time relationships than others.

3.1 The Problem of Conversion is One of Comparison or Matching

The problem which any conversion device must solve is: given an input signal, determine and produce the corresponding output signal. In order to accomplish this, it is necessary for the conversion device to compare and match its output signal with the input signal. Since some of the conversion devices are forced to make more than a single comparison during this conversion process, the number of comparisons necessary will, to a large extent, influence the operating speed of the various components of the conversion device.

There are three fundamental ways in which the requisite comparison process can be carried out in the digital-analog conversion device; these are:

1. Serial matching of each quantizing increment;
2. Serial matching of each binary digit;
3. Parallel matching of all digits (simultaneous comparison).

It should be emphasized that this classification of conversion methods is not restricted to either encoding or decoding devices alone, but is equally applicable to both. The following sections briefly discuss and exemplify each of these methods.

3.11 Serial Matching of Each Quantizing Increment

The method of increment matching is accomplished by making a comparison between the input and output signals of the conversion device. If the two do not agree, the output signal is changed by one quantizing unit. A new comparison is then made, and the process is continued until an agreement is established. There are two fundamental ways in which this method of increment matching may be accomplished:

1. The last tested value of the output is stored, and a new output is established by changing the preceding output a sufficient number of quantizing increments so that it agrees with the new value of the input;
2. The output is cleared to zero, and a new output is established by comparing the input and output at each quantizing level until the correct output level is reached.

The first method given above corresponds to the operation of the continuous coding device which was given in the table in Section 2.71 for the continuous conversion of a shaft position into a binary number.[23] This conversion device remembers the last position of

the shaft and changes its binary number output only if the shaft moves to a new position. Such an operating method requires, of course, that the conversion device realize in which direction the shaft has turned in order that it can correctly change the output quantity. With this type of operation, there is an obvious relationship between the frequency at which comparisons must be made (the frequency of operation of the equipment in the conversion device) and the conversion time:

$$f_c = \frac{1}{\tau} \qquad (3\text{-}1)$$

where f_c is the frequency of making comparisons, and τ is the conversion time.

The second method given above has been used in the following form as an encoding device:[22,24] An integrating circuit generates a voltage amplitude which is proportional to the time interval being measured (counted) by a binary counter; a continuous amplitude comparison is made between this generated voltage and the voltage which is to be converted; when the output voltage of the integrator is equal in magnitude to the analog input voltage, the counter is stopped and now contains the binary number representation of the input voltage. Figure 4-a shows this form of incremental encoding.

This same conversion scheme is also used to convert binary numbers to analog voltages.[17,20] The number is put into a counter, and as the integrator linearly increases the output voltage of the conversion device, pulses are sent to the counter, each pulse

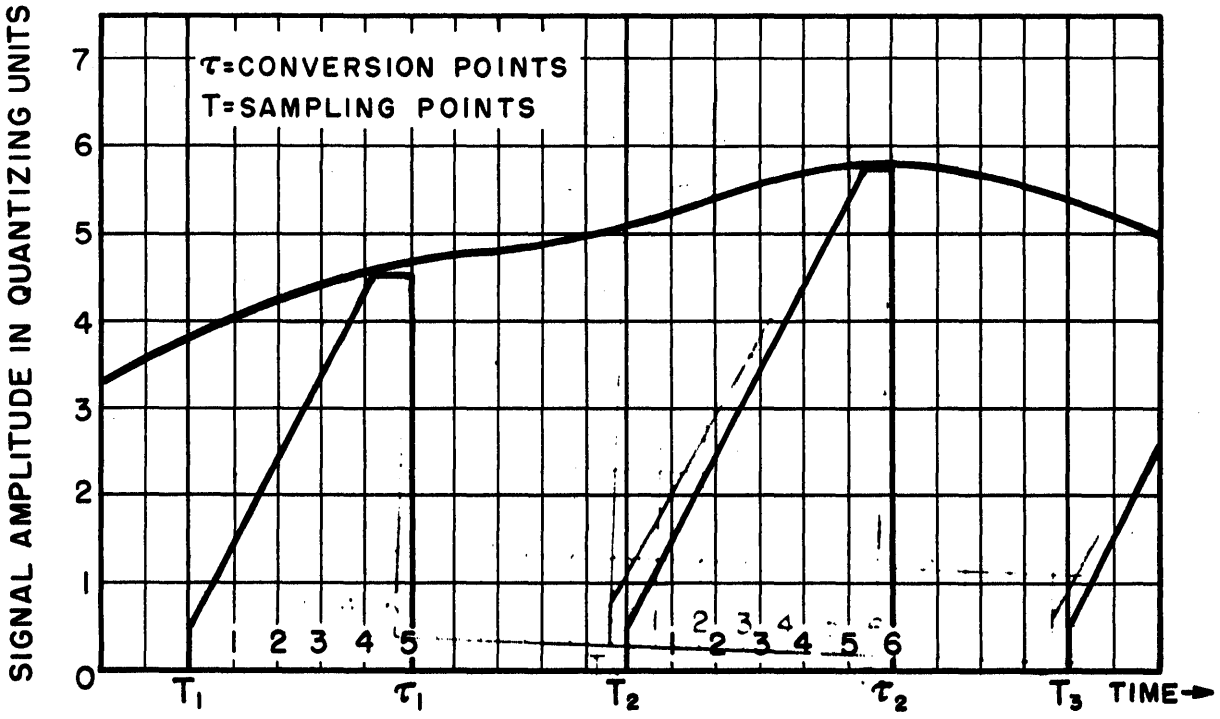
subtracting one unit from the counter. When the contents of the counter equals zero, the integrator is stopped and the amplitude of the output voltage is linearly related to the input number.

In both of the methods just presented, a comparison is made between the input and output of the conversion device for each quantizing level. It is immediately obvious, therefore, that the frequency of comparison for the conversion device will depend upon the number of quantizing levels. In terms of the notation used for the continuous conversion device, we have:

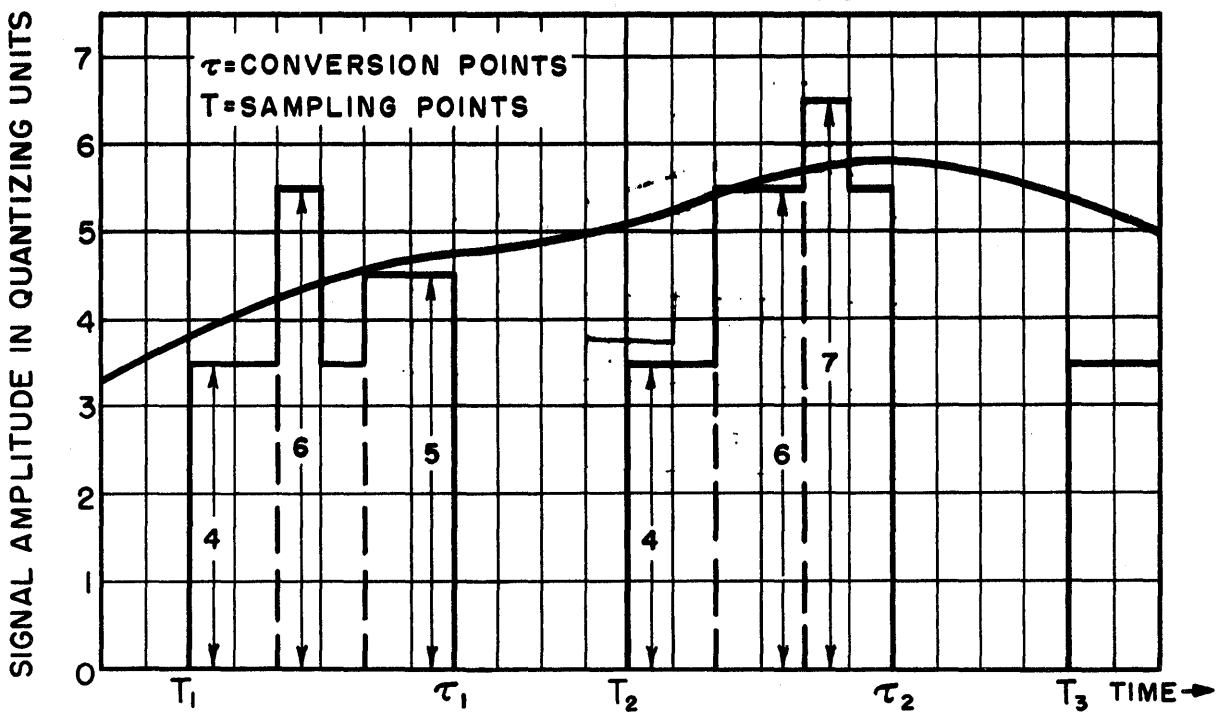
$$f_{c(max)} = \frac{1}{\tau} \times N \qquad (3\text{-}2)$$

Equation 3-2 shows that we have paid rather dearly for the privilege of each time initiating the comparison from a zero reference level. The only benefits which have resulted are:

1. The conversion device no longer has to store or remember the last value of the output;
2. The conversion equipment need not sense the direction of change of the input signal, since the zero reference is generally made equal to the minimum (or maximum) value of the input signal.



(a) INCREMENTAL ENCODING



(b) BINARY-WEIGHTED ENCODING

FIG. 4

EXAMPLES OF SAMPLING CONVERSION DEVICES

A-45288

3.12 Serial Matching of Each Binary Digit

Instead of making a comparison of each quantizing increment as was done in Section 3.11 above, it is possible to make these comparisons on a digital basis. One possible way of doing this for encoding is shown in Figure 4-b.[21] In this method, a comparison voltage is generated by the conversion device, the amplitude of which is proportional to the largest binary digit of the output number. This magnitude is then compared with the input voltage amplitude:

(a) If the comparison voltage amplitude is less than the input voltage, the conversion device leaves this binary digit in the one (1) position, which at the same time leaves the corresponding comparison voltage set up;

(b) If this voltage magnitude is greater than the input voltage, the binary digit is cleared to the zero (0) position, at the same time reducing the comparison voltage by an equivalent amount (if no other binary digit is in the 1 position, the comparison voltage is reduced to zero).

This process is continued for each smaller binary digit until every digit has been checked. At the end of the conversion process, the comparison voltage is equal in magnitude (within one quantization unit) to the input voltage, and the conversion device now has the correct binary number representation of the input signal.

There are several other conversion devices which operate in this same manner. One of these is the Bell Laboratories' Coding Tube which is used for converting a voltage amplitude into a binary number.[12, 18, 19] Here, each binary digit is checked as the deflected electron beam is swept horizontally across the tube. Another example would be the Shannon-Rack decoder which receives its digital information serially, and thus sets up each digit in time sequence.[1, 12]

All of the above-mentioned devices follow the same general rule for establishing a relationship between the input and output signals of the conversion device: a comparison is made for each binary digit. As a result, the following relationship must hold:

$$f_{c(max)} = \frac{1}{\tau} \times \log_2 N \qquad (3\text{-}3)$$

where $f_{c(max)}$ is the maximum frequency of making comparisons, τ is the conversion time, and $\log_2 N$ equals the number of binary digits in the digital part of the conversion device.

3.13 Parallel Matching of All Digits (Simultaneous Comparison)

Two methods have already been given by which a conversion between the digital and analog realms can be carried out. Both of these methods have operated with only a single comparison channel, requiring the comparisons to be made in a serial fashion. It is

possible, however, to parallel the conversion equipment so that all comparisons can be made simultaneously. There are two fundamental ways of doing this:

1. Parallel all of the quantizing increments and interrogate the number of increments corresponding to the input signal;
2. Parallel the binary digits and interrogate the digits such that a correspondence is obtained with the input signal.

Obviously, it is the second method which would be used, since the first method requires N information-carrying channels, while the second method requires only $\log_2 N$ information-carrying channels. An example of the latter method is included in the table of decoders in Section 2.72 where an output voltage is established by simultaneously setting up all digits of a binary number.[5] For this device we again arrive at a relationship of:

$$f_c = \frac{1}{\tau} \qquad (3\text{-}4)$$

It is worthwhile to compare the conversion method which led to equation 3-4 with the method which led to equation 3-1, since they yield identical equations, and remembering that the methods are equally applicable to both coders and decoders. The continuous conversion device established the relationship of equation 3-1 by keeping in constant communication with the input signal. By this constant communication, the last value of the input signal was always available;

Thus, a change in this value could be sensed and the output signal correspondingly corrected. The parallel conversion method which led to equation 3-4, however, did not need to remember the last value of the input in order to establish a new value of the output. Each time a conversion is made, the total value of the input is sent to the conversion equipment over parallel channels. This latter method allows the output of the conversion device to be kept independent of the input signal fluctuations at all times except when an actual conversion is taking place; but more will be said of this later.

3.2 Comparison of Digital-Analog Conversion Devices to Analog Systems

The preceding section has established relationships between the number of quantizing levels, the conversion time, and the frequency of comparison for the various conversion devices. However, no restrictions have as yet been placed upon the number of quantizing units or upon the length of time allowable for the conversion process. The specification of these values can be accomplished only if one has a knowledge of the overall system in which the conversion device is to be used.

In order to consider the effect which the conversion device will have upon the external system and thus to determine such factors as the requisite number of quantizing units and the conversion time,

it is very helpful to have a single method of evaluation for the entire system. Since the digital-analog conversion equipment interconnects the digital and analog fields, it is possible to consider the entire system from either of these two points of view. However, because the analysis and synthesis of analog devices has been carried the further, it appears logical to choose this field. The following sections first discuss the important characteristics used to describe analog devices and then compare these characteristics and the ones established above for digital-analog conversion devices.

3.21 Methods for Comparing Analog Devices

Analog equipment, especially electrical equipment, has been rather thoroughly analyzed and several methods of evaluating the various pieces of analog equipment have been developed. An electrical signal can be described in terms of its frequency components, the phase and magnitude of these components, and some sort of description of the noise, such as the mean square signal-to-noise amplitude ratio or power density spectrum. If one wishes to perform some sort of complex operation on the electrical signal, it is possible to apply the methods of filter theory and network synthesis in order to determine how well one can perform this operation. The determination of how well the operation is performed may take several forms, but probably the one most used is that of the mean square error between the desired result and the obtained result.

In analog conversion devices, generally the only desired form of operation on the input signal is that of converting it from one analog variable into another. In this case, the dynamic and steady-state accuracy and the time delay with which the conversion is achieved are the important quantities. Various analog conversion devices may thus be compared by means of the mean square error criteria, where the desired output of the conversion device is an exact replica of the input except for the form of the analog variable, i.e., related directly by means of a scale factor. If a constant time lag between the input to and the output from the conversion device is not important, then the mean square error may be evaluated by assuming the desired output of the conversion device to be delayed with respect to the input signal by a fixed time delay.

In order to obtain a value for the mean square error, it is necessary to be able to describe completely the input signal to the conversion device. Even though this description can be made and the mean square error determined, this particular error criteria may not always be the best one to use. It is possible, however, to obtain a crude and relative evaluation without using this criteria and hence without requiring a complete description of the input signal. The properties of the conversion device (which itself may be thought of as being similar to an amplifier for which the

desired output is a scale factored replica of the input) can be described in much the same fashion as one describes an amplifier -- the bandwidth, the linearity or accuracy, and the noise level of the device. All three of these can produce a distortion of the input signal. When several frequency components are present in the input signal, bandwidth distortion attenuates and phase shifts some of these frequencies with respect to the others. When a single frequency component is applied to the input, linearity distortion (an amplitude-sensitive distortion) will introduce new frequency components. Noise level is usually independent of the input signal, being dependent upon the equipment in the system.

With this section as a background, it is possible to relate the conversion time and the size of the quantizing units of the digital-analog conversion device to certain of the parameters used to describe analog systems.

3.22 Quantization Error Compared to Noise

In the terms of numerical analysis, quantization error is equivalent to a round-off error. This round-off error is produced because of the limited number capacity of the digital part of the conversion system. In this respect it is similar to noise, since any variation of the input signal within a single quantization unit does not change the output signal. If one were then to express the output of a quantizing device in terms of the input signal and a quantizing error, the result would be:

$$g(t) = f(t) - E\left[Q,\ f(t)\right] \qquad (3\text{-}5)$$

where $0 \leq E\left[Q, f(t)\right] \leq Q$ is the instantaneous deviation of the output signal, and Q is the magnitude of a quantization interval. Quantization can thus be looked upon as an additional noise or corruption of the input signal, the frequencies of this noise being dependent upon and higher than the frequencies of the input signal to the quantizing device. With quantization similar to noise, the maximum amplitude of which is equal to one quantizing unit, the necessity of keeping the quantizing units small for high accuracy systems is immediately obvious.

3.23 Conversion Time Compared to Bandwidth

The conversion time has been defined as the interval between the time when an input signal is applied to be converted and the time when the output has been established to within the desired accuracy. The frequency of conversion (the reciprocal of the conversion time) thus roughly corresponds to the bandwidth of an analog system. This is readily seen by noting that as the frequency of the input signal to the conversion device increases, the accuracy of the output decreases, if the conversion frequency is maintained constant. The conversion frequency itself is related to the time constants of the conversion device in much the same way that the bandwidth of an analog system is related to the various system time constants.

3.3 Matching the Conversion Device to the External System

With quantization and conversion time related to accuracy and bandwidth, it is now possible to see what relationships must exist between the conversion device and the rest of the system.

If a signal with a certain noise level is applied to the input of a conversion device, it is obviously desirable that the conversion device introduce little additional error into this signal. In order to accomplish this, it is necessary that the size of the quantization unit and the amplitude of the noise signal should be of similar magnitude. However, an additional factor which has not been considered so far is the interrelationship between the quantizing unit, the conversion time, and the characteristics of the input signal. The examples which follow should help in this respect.

One possible signal which we might specify as an input to a digital-analog conversion device is a signal for which the peak amplitude and maximum frequency are all that are specified. Inside of these boundary values, it is possible for the signal to vary in any and all fashions. If the output from the conversion device is at all times to be accurate to within one quantization unit, it is necessary to establish a new value of the output each time the input signal changes from one quantization level to another. The rate at which the input changes levels is dependent upon the slope of the input waveform and the size of the quantization units of the conversion device. The relationship which results is:

$$\frac{dE}{dt} \times \tau \cong Q \qquad (3\text{-}6)$$

where $\frac{dE}{dt}$ is the slope of the input waveform during the conversion, τ is the conversion time, and Q is the size of a single quantization unit.

The above relationship is a very pessimistic one, since it requires in the extreme that the maximum conversion frequency equal the product of the number of quantizing levels times the angular frequency of the highest frequency component of the input signal. The reason for this result is that so little was assumed to be known about the input signal to the conversion device. It might also be noted that this same relationship occurs if a simple R-C filter is used to pass such a signal, where conversion frequency is related to the filter's upper half-power frequency, and the number of quantizing levels is inversely related to the desired instantaneous accuracy of the signal at the output of the filter.

Instead of the almost completely arbitrary input signal given in the last example, let us assume a signal having a constant slope (a ramp input). If we make the slope of this ramp equal to the slope used in equation 3-6, the apparent result is that γ must be the same as before in order to have the converted signal accurate to within one quantization unit. This is certainly true, <u>if</u> we proceed with the conversion as previously; but we must also recognize that a total of two readings will completely specify the ramp input signal. In this case, then, we may introduce a device which will sample the ramp at a particular point and then hold this sample for as long as is necessary to complete the conversion. By repeating this process a second value is obtained, and if the times at which the samples are obtained are known, the ramp can be completely specified.

It must be realized from these two examples that there is no unique way in which one can specify a relationship between the conversion time, the size of the quantizing units, and the characteristics of the input signal. The process of sampling and holding the input signal, as was done in the second example, need not introduce large errors if enough is known about the characteristics of this input signal.[10] However, this knowledge of the input signal required that one know ahead of time the system in which the conversion device is to be used, and also that some suitable criteria for evaluation, such as mean square error, can be applied. If this is not the case, the two examples given, plus the fact that it is desirable to have the quantizing error and the signal noise-level of about the same magnitude, allow one to bracket the necessary requirements.

3.4 Conclusions and Evaluation of the Various Conversion Methods

This section is not intended as an exhaustive discussion of all the possible types of equipment and the associated problems which one might run into in the field of digital-analog conversion devices. However, it has been possible to obtain some idea of the problems associated with conversion equipment. Certain relationships have been derived which are useful in comparing the various conversion methods and which allow a relative evaluation of such devices. The following paragraphs summarize the conclusions which can be drawn from the discussion in this section.

Quantization may be considered as a noise introduced into the input signal by the conversion device; it may also be considered

as a round-off error, if one wishes to describe it in the terms of numerical analysis. Conversion frequency is directly related to the bandwidth of an analog system: as the bandwidth of an analog system is increased in order to pass higher frequency signals, the conversion frequency of a conversion device should also be increased, if an increase in error is to be avoided.

Exact relationships cannot be obtained between the input signal to a conversion device and the conversion time unless the input signal is completely described and suitable evaluation criteria are known. However, if this evaluation can be made, it is possible, by means of sampling and holding of the input function over the conversion interval, to increase the conversion time over the limiting value obtained in equation 3-6. The type of system to which the output of the conversion device is connected is also important, since this system can help to eliminate the corruption introduced by the sampling process.[10]

Three fundamental techniques have been presented in this section for the conversion between digital and analog quantities. Each of these conversion methods has a direct correspondence to the three basic methods of transmitting digital information:

1. Transmission in series of all the increments which correspond to the present value of the signal;

2. Transmission in series of each binary digit which corresponds to the present value of the signal;
3. Transmission in parallel of all the digital information corresponding to the present value of the signal.

Speed of conversion is achieved in the third method given above at the sacrifice of increasing the number of conversion channels. However, the method also allows a time multiplexing of the conversion equipment thus allowing for the handling of several conversion channels. Because of this speed and the possibility of multiplexing, the parallel-channel, binary-weighted conversion scheme appears to be one of the best available.

It should be noted that the parallel-channel, binary-weighted decoder discussed in Section 3.13 is also used as a part of the binary-weighted encoder discussed in Section 3.12. This decoder is that part of the circuitry which receives the pulses from a controlling device and produces the comparison voltage. As the derived relationships have pointed out, this decoder is one of the most critical parts of the conversion equipment as regards operating speed and accuracy. Since the parallel-channel, binary-weighted decoder is also a critical part of the most favorable form of encoding device, it appears advantageous to study this type of decoder in fairly close detail. With this in mind, the following section analyzes several possible designs for such decoders.

4.0 SOLUTION OF THE DECODER PROBLEM BY BINARY-WEIGHTING METHODS

Three fundamental ways of performing digital-analog conversion have been given in Section 3. Each of the methods has some form of limitation which keeps it from being the ideal device for which one might wish. However, of the three basic methods studied, that of binary-weighting parallel channels appears, for the reasons previously given, to be the most profitable approach. This section compares some of the methods which may be used for binary-weighting and attempts to evaluate them with regard to their physical realizability.

4.1 Basic Binary-Weighted Decoder Circuit

Probably the most fundamental approach to the problem of binary-weighting is that shown in Figure 5.[4] The relationship between E_2, E_1, and N, the binary number input, is readily obtained as follows:

$$E_2 = E_1 \frac{\frac{R_0}{k}}{R_{eq} + \frac{R_0}{k}} \tag{4-1}$$

where R_{eq} is the equivalent resistance of the R_0, R_1, R_2,...R_n network corresponding to N.

If the resistances are chosen such that $R_x = \frac{R_0}{2^x}$, then,

$$\frac{1}{R_{eq}} = \sum_{x=0}^{n} K \frac{2^x}{R_0} \tag{4-2}$$

where K is either 0 or 1, depending upon whether this particular

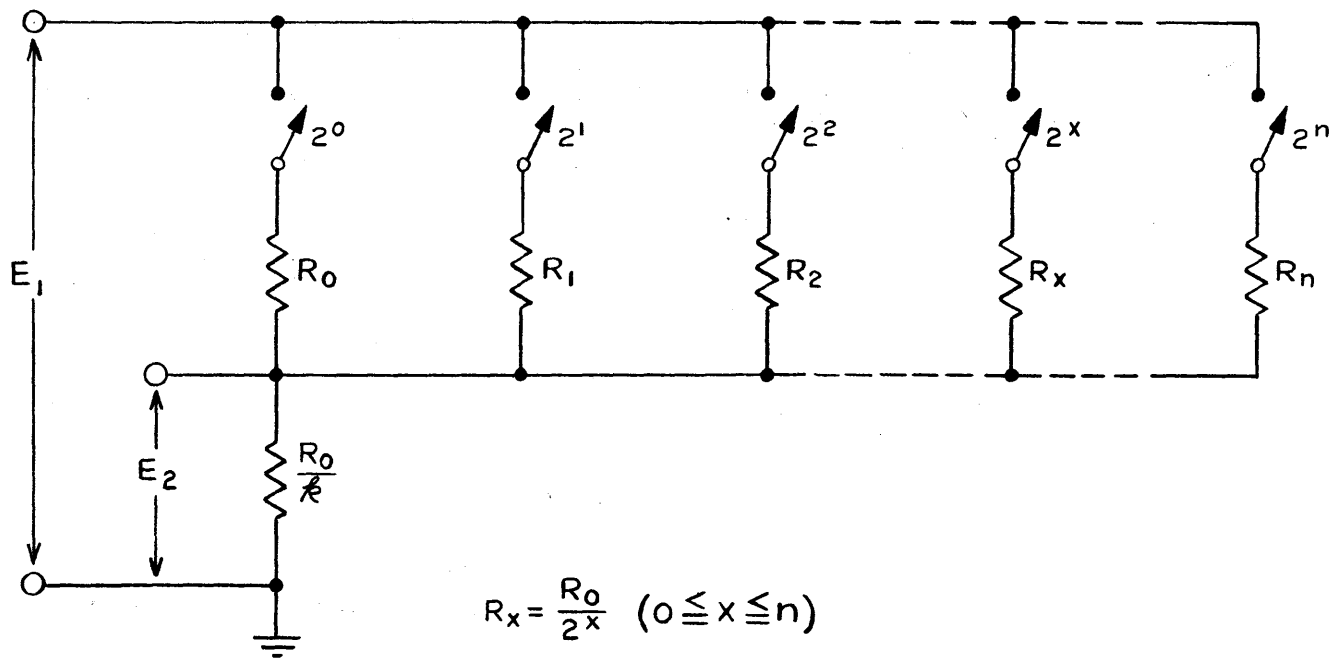


FIG. 5

BASIC BINARY-WEIGHTED DECODER CIRCUIT
USING VOLTAGE SOURCES

binary digit is present in N or not. Since the summation over all the binary digits must equal N, we obtain:

$$\frac{1}{R_{eq}} = \frac{1}{R_0} \sum_{x=0}^{n} K2^x = \frac{N}{R_0} \tag{4-3}$$

and thus, $$E_2 = E_1 \frac{1}{1 + \frac{kR_{eq}}{R_0}} = E_1 \frac{1}{1 + \frac{k}{N}} = E_1 \frac{N}{N + k} \tag{4-4}$$

4.11 Accuracy Limitations of This Decoder

The desired relation for this conversion device would be $E_2 = C_1 N$ where C_1 is a constant relating the output voltage to the input binary number. The amount by which the derived formula deviates from this value depends upon the deviation of the denominator from the constant k. This deviation in turn depends upon the ratio of k to N, and reaches a maximum value for maximum N. If the expression for E_2 is written in a slightly different form, the deviation becomes evident:

$$E_2 = \frac{E_1 N}{k} \cdot \frac{1}{1 + \frac{N}{k}} \tag{4-5}$$

For $N < k$, the term in parentheses may be expanded in a power series, giving:

$$E_2 = \frac{E_1 N}{k} \left[1 - \frac{N}{k} + \left(\frac{N}{k}\right)^2 - \left(\frac{N}{k}\right)^3 \ldots\right] \tag{4-6}$$

It is immediately apparent that for a high accuracy system the maximum value of N must be considerably less than k. Two obvious conclusions which can be drawn are:

1. The values of the resistance used in a high accuracy decoder circuit extend over a very large range;

2. The maximum output voltage E_2 is very small, because of the necessarily large value of k. The need for large resistance values also introduces considerable difficulty when a fast rise time of the output voltage is desired.

An important feature to note is that the non-linearity introduced above is equivalent to saturation effects in other types of equipment. The non-linearity increases with the magnitude of the input signal, in this case the binary number. Although the absolute accuracy obtainable by the decoder circuit is limited by this non-linearity, the sensitivity of the conversion is not. If N is increased by 1 unit, the output voltage increases by a factor equal to the slope of the N versus E_2 curve at that point. Drift in E_1 and R_0/k will only change the proportionality factor and hence the slope of the curve relating N and E_2; however drift in any one of the R_x's poses an entirely different problem.

4.12 An Accuracy Problem Common to All Numerically-Weighted Conversion Devices

Suppose that N, the number to be converted, changes from the value $N = 2^0 + 2^1 + 2^2 + 2^3 + 2^4 + 2^5 = 63$ to the value $N = 2^6 = 64$. If then, $R_5 = \frac{R_0}{2^5} = \frac{R_0}{32}$ decreases to $R_5 = \frac{R_0}{31}$, the output voltage, E_2 will remain constant as N changes from 63 to 64. In fact, it is easily seen that for drift occurring in several of the R_x's, it is

possible for the output voltage to decrease as N increases. If such a result occurs, the sensitivity of the decoder is reduced by a factor directly proportional to the error in slope at that point; similarly, the smaller digits comprising N become meaningless.

This problem of drift in the individual digit columns of the decoder is not restricted to this particular decoding scheme, but is common to any of the weighting schemes. A generalized relationship may be stated as follows: In any numerically-weighted conversion device, the accuracy of each of the numerical conversion channels must be greater than the sensitivity desired for the overall conversion, regardless of the overall conversion accuracy desired. It is this relationship which introduces all the difficult accuracy problems into numerically-weighted conversion devices.

4.13 Possible Ways of Improving This Decoder Circuit

The problems of non-linearity, large range of resistance values, and low output voltage are the three major limitations of this decoder circuit. It is possible to improve the linearity by building the circuit such that the output is obtained as a "push-pull" output from two decoder networks. The output voltage is then given by:

$$E_0 = \frac{E_1 k(2N-N_{max})}{(N+k)(N_{max}-N+k)} = \frac{E_1(2N-N_{max})}{k\left[1 + \frac{N_{max}}{k} - (\frac{N}{k})^2 + N\frac{N_{max}}{k^2}\right]} \qquad (4\text{-}7)$$

The degree of improvement is apparent when it is remembered that $k >> N_{max} \geq N$. The problem of the large range of resistance values for the R_x's can be overcome by introducing a ladder network in place of the single resistance $\frac{R_0}{k}$. However, even with these improvements, the problem is not completely solved since the output voltage is still quite low (for a reasonable value of E_1) and the linearity problem still remains important as N_{max} is increased in order to obtain higher decoding accuracies.

Two alternatives present themselves which might solve the problem. First the reason for keeping k large is so that the decoding digits all feed into a small load resistance and hence the interaction between these digits is kept to a minimum. This is the same as requiring a constant current from each decoder digit, the magnitude of this current being proportional to the magnitude of that particular decoder digit. Weighted constant current sources thus might be used in place of the resistance network. An alternative procedure also might solve the problem. In the equation $E_2 = \frac{E_1 N}{N+k}$, the variation in the denominator is what produces the non-linearity. If a way was available whereby the denominator could be maintained constant, then a linear decoder would result. The following sections analyze and evaluate these two alternative ways of producing a linear output voltage.

4.2 An Improved Voltage Source Decoding Circuit

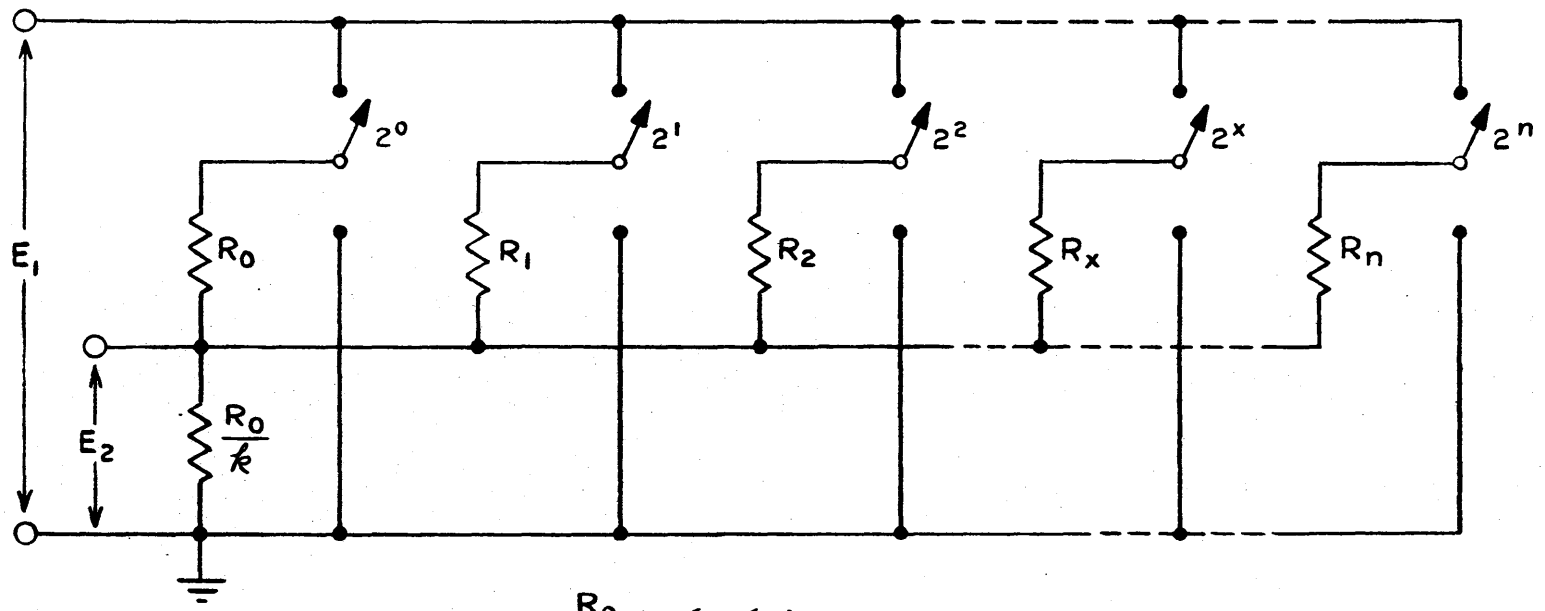
This section demonstrates how the output voltage from a set of binary-weighted voltage sources may be maintained linear, even when the magnitude of the output voltage approaches the magnitude of the input voltage.

The formula relating E_2 to E_1 for the circuit of Figure 5 was given above as: $E_2 = \frac{E_1 N}{N+k}$

Rewriting this, we obtain: $$E_2 = E_1 \frac{\frac{N}{R_0}}{\frac{N}{R_0} + \frac{k}{R_0}} \qquad (4\text{-}8)$$

The values $\frac{N}{R_0}$ and $\frac{k}{R_0}$ are respectively the reciprocal of the equivalent resistance corresponding to the input number and the reciprocal of the load or output resistance. Since $\frac{N}{R_0}$ increases as N increases, the denominator in the above expression could be maintained constant if $\frac{R_0}{k}$ (i.e., the load resistance) varied directly with N. Figure 6 shows a way in which this result can be obtained. The circuit functions in the same way as before except that when a particular binary digit column is missing from the input number N, the resistance corresponding to this digit column is placed in parallel with R_0/k.

In Section 4.1 it was shown that R_{eq} (the equivalent resistance of the R_0, R_1, R_2,.....R_n network corresponding to N) $= \frac{R_0}{N}$. The minimum value of the network resistance, R_t, corresponding to N_{max} the largest binary number that could be



$$R_x = \frac{R_0}{2^x} \; (0 \leqq x \leqq n)$$

$$E_2 = \frac{E_1 N}{N_{max} + k}$$

$N \leqq 2^{n+1} - 1$ = BINARY NUMBER INPUT

$N_{max} = 2^{n+1} - 1$

FIG. 6

IMPROVED BINARY-WEIGHTED DECODER CIRCUIT USING VOLTAGE SOURCES

converted, is: $R_t = \frac{R_0}{N_{max}}$ (this is obtained for all the R_x's in parallel). Since all of the R_x's are utilized in the circuit, those which do not go to make up R_{eq} must appear in parallel with $\frac{R_0}{k}$. If this latter resistance is designated R_n', its value may be found from the equation:

$$\frac{1}{R_t} = \frac{1}{R_{eq}} + \frac{1}{R_n'}, \quad \text{or} \quad \frac{1}{R_n'} = \frac{1}{R_t} - \frac{1}{R_{eq}} = \frac{N_{max}}{R_0} - \frac{N}{R_0} \tag{4-9}$$

$$\text{and therefore,} \quad R_n' = \frac{R_0}{N_{max} - N}. \tag{4-10}$$

The load resistance, R_L, across which E_2 is obtained, will be the parallel combination of $\frac{R_0}{k}$ and R_n', which gives:

$$\frac{1}{R_L} = \frac{k}{R_0} + \frac{N_{max} - N}{R_0} \quad \text{or,} \quad R_L = \frac{R_0}{N_{max} - N + k}. \tag{4-11}$$

The output voltage E_2 is then given by:

$$E_2 = \frac{E_1 R_L}{R_{eq} + R_L} = E_1 \frac{\frac{R_0}{N_{max} - N + k}}{\frac{R_0}{N} + \frac{R_0}{N_{max} - N + k}} \quad \text{or,} \quad E_2 = \frac{E_1 N}{N_{max} + k}. \tag{4-12}$$

The formula arrived at for E_2 is linear with respect to N, and what is even more important, the ratio of N to k is in no way restricted. In fact, it is possible to let k equal zero; under such conditions, the maximum value of E_2 (corresponding to $N = N_{max}$) would be equal to E_1. Theoretically, then, this circuit can yield

an output voltage linearly related to the input number N, and whose amplitude may approach that of the supply voltage. However, as in all theoretically perfect systems, engineering problems always present themselves. The major problem in this decoder is that of switching the binary-weighted decoder channels. The following section analyzes and evaluates one of the many ways in which this switching might be accomplished.

4.21 A Possible Voltage Source Switching Circuit

The switching problem posed by the decoder circuit of Figure 6 is rather critical since it requires that the switch operate so as to bring the voltage on one end of the decoder resistances to either one of two stable voltage positions, with current flowing through the decoder resistances in each of these two positions. The problem of switching is relatively simple if cam- or relay-operated mechanical switches are used, but this of necessity yields a slow speed device. For high speed switching, requiring the use of vacuum tubes, probably one of the easiest ways of producing the requisite switching action is by means of clamping circuits. A voltage source switching circuit employing clamping diodes is shown in Figure 7. For V1 conducting, with the grid-cathode voltage near zero, the plate of V1 is at approximately ground potential, while with VI cut off, its plate potential rises to approximately E_1. The switching action would be ideal if the clamping diodes had infinite back resistance and zero forward

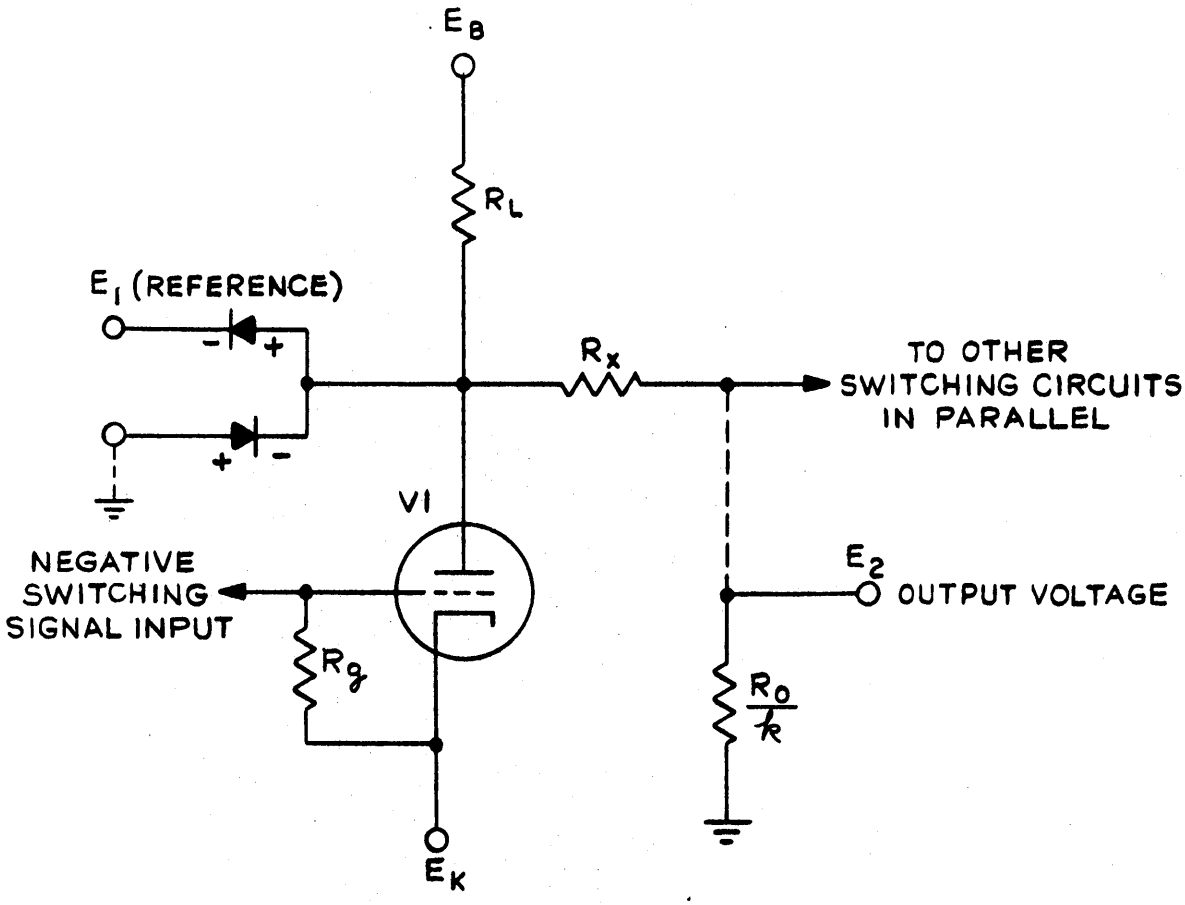


FIG. 7

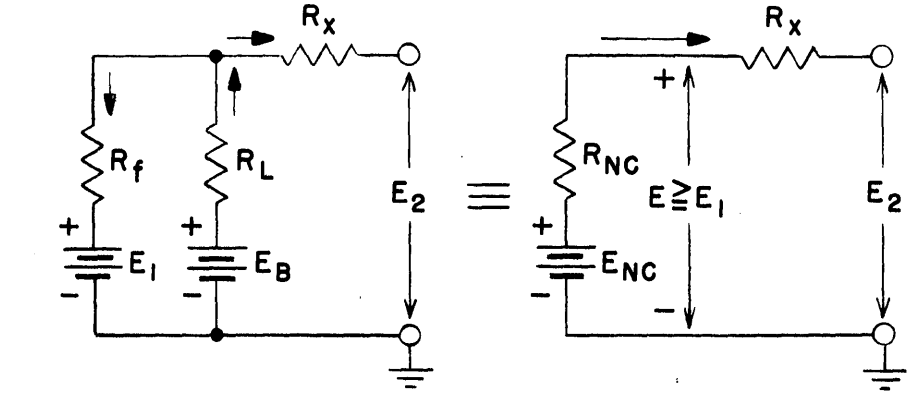
VOLTAGE SOURCE SWITCHING CIRCUIT

A-45258

resistance and the other circuit parameters were adjusted so that current would be flowing in a forward direction through either one or the other of the diodes regardless of the value of the output voltage. It is immediately apparent that the clamping diodes and E_1 are the most important elements in the circuit for determining the output voltage accuracy.

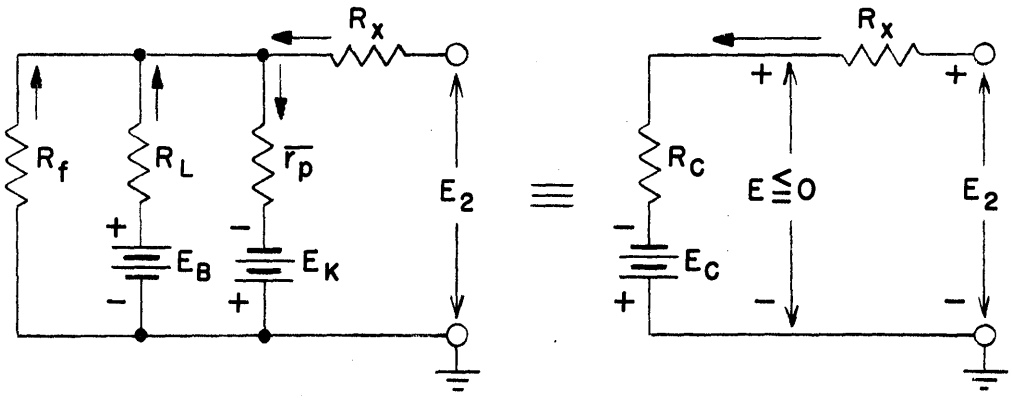
4.22 Analysis of the Switching Circuit of Figure 7

The equivalent circuits corresponding to the two operating positions of the switching circuit described above are shown in Figure 8. These equivalent circuits and the formulas given are readily derived by the use of elementary circuit analysis. The equivalent circuit for V1 non-conducting shows that the switching circuit reduces to a voltage source E_{NC} having a value somewhat greater then E_1, the reference voltage, and a resistance, R_{NC}, having a value somewhat less than R_f. The effect of R_{NC} not being zero can readily be allowed for by reducing the calculated value for R_X by an amount equal to R_{NC}. The fact that E_{NC} is greater than E_1 is also unimportant, since if the value of E_{NC} is the same for all decoder digits, it merely means that the circuit operates with a slightly larger effective reference voltage. Because the voltage E_{NC} minus the drop across R_{NC} must always be greater then E_1, the reference voltage, in order for the diode clamping action to be effective, it is not possible to completely eliminate the effect of fluctuations



$$E_{NC} = \frac{E_1 R_L + E_B R_f}{R_L + R_f} = E_1 + \frac{E_B - E_1}{1 + \frac{R_L}{R_f}} \qquad R_{NC} = \frac{R_L R_f}{R_L + R_f} = \frac{R_f}{1 + \frac{R_f}{R_L}}$$

(a) VI NON-CONDUCTING



$$E_C = \frac{(E_K R_L - E_B \overline{r_p}) R_f}{\overline{r_p} R_L + \overline{r_p} R_f + R_L R_f} = \frac{E_K R_L - E_B \overline{r_p}}{R_L + \overline{r_p}(1 + \frac{R_L}{R_f})}$$

$$R_C = \frac{R_L R_f \overline{r_p}}{\overline{r_p} R_L + \overline{r_p} R_f + R_L R_f} = \frac{R_f}{1 + R_f(\frac{R_L + \overline{r_p}}{R_L \overline{r_p}})}$$

(b) VI CONDUCTING WITH GRID-CATHODE VOLTAGE $\cong 0$

$\overline{r_p}$ = STATIC PLATE RESISTANCE OF VI (MAY ALSO INCLUDE EXTERNAL RESISTANCES)

R_f = FORWARD RESISTANCE OF DIODES

R_b = BACK RESISTANCE OF DIODES; ASSUMED LARGE ENOUGH TO BE NEGLECTED IN COMPARISON WITH R_L AND $\overline{r_p}$

FIG. 8
EQUIVALENT CIRCUITS FOR VOLTAGE SOURCE SWITCHING CIRCUIT

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in E_B. However, variations in E_B will normally be unimportant since they will be attenuated by $1 + \frac{R_L}{R_f}$, and this factor should be large.

The equivalent circuit for V1 conducting shows that the switching circuit reduces to a voltage source, E_C, having a value which must be greater than zero in magnitude, and a resistance, R_C, having a value somewhat less than R_f and also somewhat less than R_{NC}. The slight difference between R_C and R_{NC} is unimportant in a practical circuit, since R_X would normally be very much larger than R_f. The voltage E_C, however, poses a different problem. By using methods of superposition, it can be shown that the voltage E_C produces an output voltage at E_2 having the opposite polarity to that of the desired output and whose magnitude is related to the binary input number N by the same equation as was derived for Figure 5, with E_C replacing E_1 in this equation. If the voltage E_C is small enough, then the output will be negligibly affected. This same result can be achieved by letting $k \rightarrow 0$; this gives an infinite load resistance. A third alternative is to return the grounded side of the lower diode in Figure 7 to a potential slightly positive with respect to ground and so force E to be zero and still allow forward conduction through the diode.

Further difficulties that are encountered in this switching circuit are as follows:

1. Diode forward resistance must be small compared to R_x, and stable in value. Diode back resistance is unimportant so long as it remains large compared to R_L.
2. Back voltage across diodes is equal to E_1, which may be relatively large.
3. The reference source E_1 must remain at a constant value, even for varying magnitudes of currents flowing into this reference source.
4. The power dissipation in R_L can become very large for V1 conducting.
5. V1 must be capable of carrying currents in the tens of milliamperes in order that the circuit function properly and that the rise time of the output voltage be kept small.
6. A "holding" or storage device must be used in conjunction with each switching circuit.
7. Since each R_x is different, the design of each switching circuit should be somewhat different, as the operating current requirements will differ. This, in turn, makes the problem of periodic alignment very difficult, since a single checking scheme might not be usable for all switching circuits.
8. Additional difficulty might be introduced by fluctuations in either E_K or E_B. However, for $R_L \gg R_f$, and $\overline{r_p}$ of the

same order of magnitude as R_L, the effect of these fluctuations can be reduced to a relatively insignificant level.

Notice that no mention has been made as to the necessity of an extreme resistance range for R_x if one were to use this decoder for very accurate decoding. Suppose one desired to decode numbers from 0 to 1,023; i.e., $2^{n+1} = 1024$. The formula associated with Figure 6 requires a decoder resistance range from R_0 to $\frac{R_0}{512}$. However, it is possible to circumvent this difficulty by separating the decoder output into two sections: these two output sections are then reconnected through a resistance attenuation network. Such a procedure will reduce the resistance range of 512 which was given above to a range of 16. The resistance values in the attenuation network connecting the two halves of the decoder can be adjusted to any level, since they turn out to be dependent upon the parameter k (as defined in Figure 6), and this parameter may assume any reasonable value.

4.23 Summary of the Method of Using Binary-weighted Voltage Sources

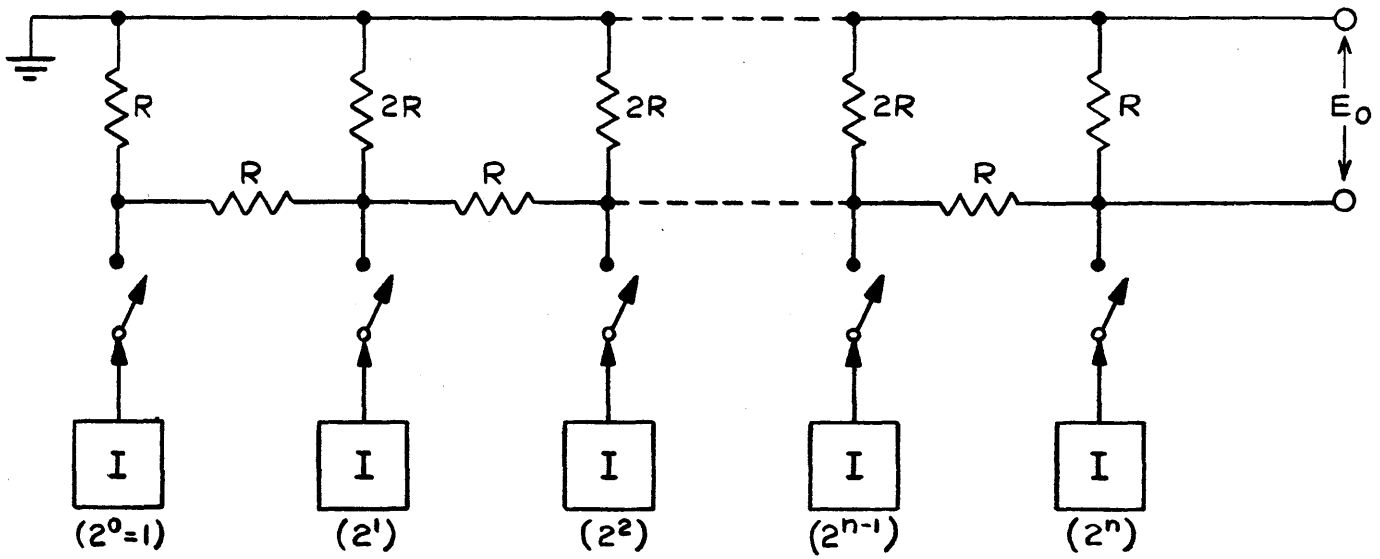
The method which has been described above shows promise of being a relatively worthwhile means of accomplishing weighted conversion. Several inherent engineering difficulties have been presented, such as the possible non-uniformity in the design of the switching circuits for the various decoder channels. Aside

from the need for closely regulating the reference voltage E_1, the greatest problem is associated with the clamping diodes. However, for the most part, these engineering difficulties probably can be overcome and a successful decoder built. But before any such conclusions are drawn, it would be well to analyze and evaluate the alternative method for weighted decoding which was mentioned earlier -- that of using binary-weighted constant current elements. This procedure is discussed in the following section.

4.3 A Binary-Weighted Decoding Circuit Using Constant Current Sources

This section briefly considers the ways in which current sources can be used in a binary-weighted conversion device, along with the design of a suitable current source for solving the problem. The additional problem of switching these current sources and the necessity of incorporating a "holding" or storage device in order to maintain the current sources in either one of their two stable positions are also considered.

As was mentioned in Section 4.1, one possible solution to the problem of a weighted decoder can be obtained by using current sources in place of the weighting resistances appearing in Figure 5. One of the major problems in such a scheme lies in the need of designing a set of different-valued current sources to produce the requisite binary weighting. Instead of weighting the decoder digits by using differently valued current sources, it is possible to do the binary weighting by means of a resistance ladder network to which a set of equal-valued current sources is connected; such a scheme is shown in Figure 9. Each current source sees at its output terminal an equivalent resistance of $\frac{2}{3}$ R. The network is so designed that the voltage attenuation per section is $\frac{1}{2}$, this attenuation producing the necessary binary weighting. As shown on Figure 9, the output voltage is given by: $E_0 = (\frac{2}{3} IR) \frac{N}{2^n}$, where N is the binary number input. Linearity of the output voltage is dependent both upon the correct values of the resistances in the ladder network and upon the constancy and equality of the current sources. (4-13)



$$E_o = \left(\frac{2}{3} I R\right) \frac{N}{2^n} = \frac{IR}{3} \cdot \frac{N}{2^{n-1}}$$

$n+1$ = NUMBER OF CURRENT SOURCES

$N \leq 2^{n+1} - 1$ = BINARY NUMBER INPUT

FIG. 9

BINARY-WEIGHTED DECODER CIRCUIT USING EQUAL-VALUED CURRENT SOURCES

It is worthwhile to study the exact effect of the resistance ladder network upon the linearity of the output voltage E_0. The first question which naturally arises is: What is the effect of a load resistance placed across the output terminals? This question is readily answered when one realizes that the combination of ladder network and current sources can be replaced by an equivalent voltage source, whose value depends upon the binary number N, and a series resistance, whose value remains constant at $\frac{2}{3}$ R. A constant load resistance placed across the output terminals will thus only attenuate the magnitude of the output voltage, but will in no way affect the linearity or binary weighting of the decoder.

A second question which one might ask is: What if all the resistances in the ladder network are not either R or 2R, but some of them differ appreciably from their correct value? The answer to this problem lies in the fact that the ladder network is linear; if the ladder network does not give the correct binary weighting, then the current sources may be adjusted so that the overall result is a binary weighting at the output terminals. The only difficulty with such a scheme is that each current source may have to be adjusted to a different value, and the normal ease with which this decoder circuit can be adjusted and checked is lost; but more will be said of this later.

Besides the problems associated with the resistance network, several difficulties arise in conjunction with the current sources. These must be drift-free, capable of being switched on and off, and must be insensitive to voltage changes

in the ladder network which are produced by neighboring current sources. The problem of a suitable current source is discussed in the following section.

4.31 Analysis of a Constant-Current Source

The problem of designing a constant-current source is generally that of converting a reference voltage into a current which can be maintained to within a specified accuracy for a given range of voltage variation on the output terminal of the current source. In order to obtain a better idea of the possible magnitude of this voltage variation, it is worthwhile to analyze the voltage variations occurring throughout the ladder network. Equation 4-13 gives as the maximum output voltage of the ladder network:

$$E_{0(max)} = \frac{2}{3} IR \frac{N_{max}}{2^n} = \frac{2}{3} IR \frac{(2^{n+1} - 1}{2^n} \cong \frac{4}{3} IR \text{ (for } 2^n >> 1). \qquad (4\text{-}14)$$

If only one digit is in the "on" position, the voltage across the ladder network at that current source is $\frac{2}{3}$ IR. Therefore, the voltage variation on the outputs of the current sources at the ends of the ladder network approaches $\frac{1}{2} E_{0(max)}$. By superposition, it can be shown that the maximum voltage at the center of the ladder network approaches 2IR for $2^n >> 1$. Thus, the current sources in the ladder network must be able to absorb voltage fluctuations varying from $\frac{1}{2} E_{0(max)}$ at the ends of the network to a value approaching $E_{0(max)}$ at the middle of the network (the total voltage

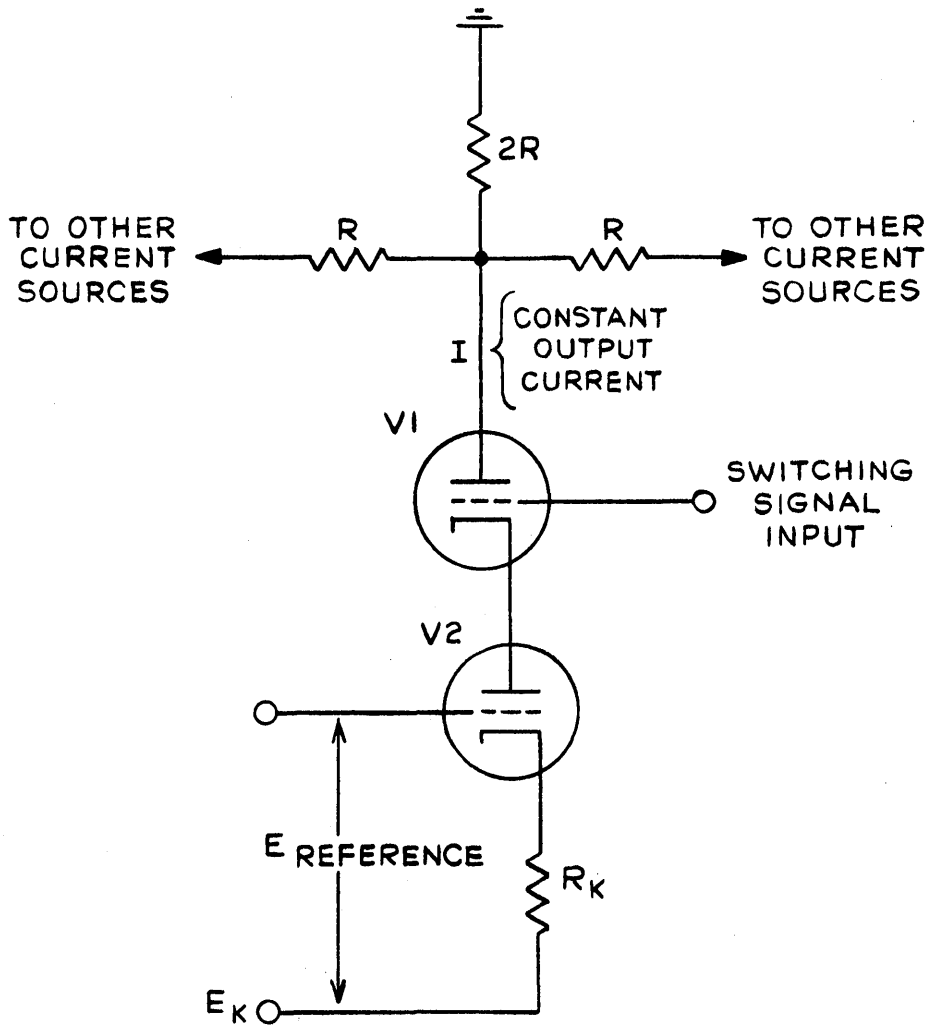


FIG. 10

CASCADED CATHODE-FOLLOWER USED AS A CONSTANT-CURRENT SOURCE

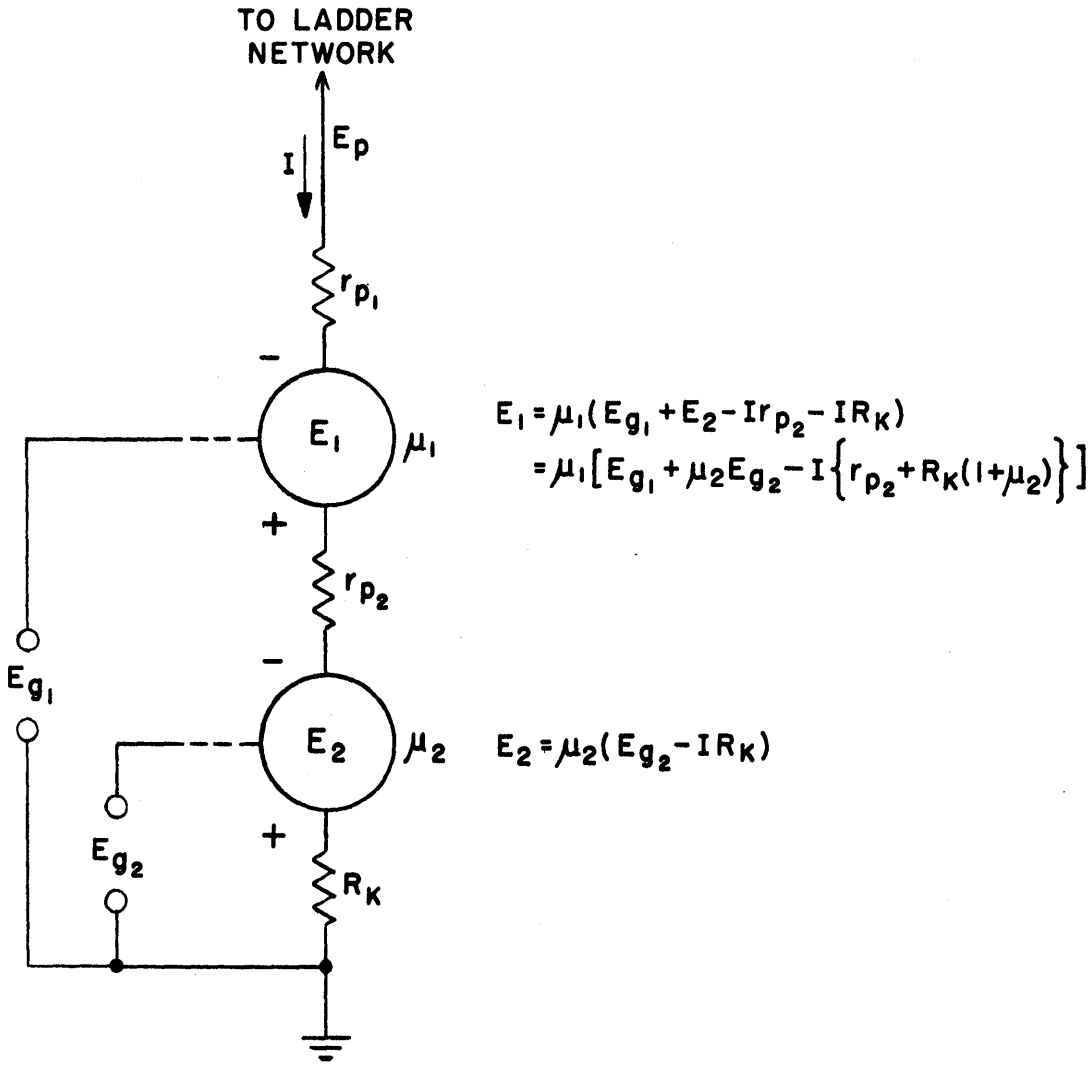
A-45255

drop across the ladder network varies from 0 to $E_{0(max)}$ and $\frac{3}{2} E_{0(max)}$ in these respective locations). Therefore, for large output voltages, the current sources must be designed so as to allow for a voltage deviation equal to the maximum output voltage and still maintain a constant current. A possible circuit for achieving such a constant current is shown in Figure 10. The output circuit has been separated from the current regulating part of the circuit by the introduction of two vacuum tubes, the gain of these tubes allowing the output current to be relatively unaffected by large deviations in output voltage.

The equivalent circuit corresponding to the cascaded cathode-follower of Figure 10 is shown in Figure 11. The derivation of the equation for "I" follows directly from elementary circuit analysis and this derivation has been outlined on the diagram. The resulting equation is:

$$I = \frac{E_p \frac{1}{(\mu_1 + 1)(\mu_2 + 1)} + E_{g_1} \frac{\mu_1}{(\mu_1 + 1)(\mu_2 + 1)} + E_{g_2} \frac{\mu_2}{\mu_2 + 1}}{\frac{r_{p_1}}{(\mu_1 + 1)(\mu_2 + 1)} + \frac{r_{p_2}}{\mu_2 + 1} + R_k} \qquad (4\text{-}15)$$

This can be simplified by letting $\mu_1 = \mu_2 \gg 1$.



$$I = \frac{E_p + E_1 + E_2}{r_{p_1} + r_{p_2} + R_K} = \frac{E_p \frac{1}{(\mu_1+1)(\mu_2+1)} + E_{g_1} \frac{\mu_1}{(\mu_1+1)(\mu_2+1)} + E_{g_2} \frac{\mu_2}{\mu_2+1}}{\frac{r_{p_1}}{(\mu_1+1)(\mu_2+1)} + \frac{r_{p_2}}{\mu_2+1} + R_K}$$

FIG. 11

EQUIVALENT CIRCUIT FOR CASCADED CATHODE-FOLLOWER

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We then obtain:

$$I = \frac{E_p \left(\frac{1}{\mu}\right)^2 + E_{g_1} \left(\frac{1}{\mu}\right) + E_{g_2}}{r_{p_1}\left(\frac{1}{\mu}\right)^2 + r_{p_2}\left(\frac{1}{\mu}\right) + R_k} \qquad (4\text{-}16)$$

This equation has been written in a form which readily allows an evaluation of the effect of the various circuit voltages and resistances on the output current. The output current is primarily determined by the ratio $\frac{E_{g_2}}{R_k}$; this requires that these two parameters be maintained at least as accuracte as the desired accuracy of the output current. The effect of variations in E_p is reduced by a factor of $\left(\frac{1}{\mu}\right)^2$ so that for $\mu = 50$, a deviation in E_p of 250 volts will have the same effect on the output current as a 0.1 volt deviation in E_{g_2}; a similar relationship holds for r_{p_1}. Since the vacuum tubes are operating at constant current, the μ of the tubes is almost independent of their plate voltage; variations in μ are therefore reduced to a minimum.[25] Also, vacuum tube V_1, which must accommodate the greatest change in its operating conditions, is located in the most insensitive part of the circuit; this allows a relatively large variation in the r_p of this tube without affecting the accuracy of the output current.

Two questions immediately arise concerning this form of current source:

1. Why not use a single pentode in place of the two triodes;
2. How does one switch the current source on and off?

The answer to the first question becomes obvious once one considers the operation of a pentode: the pentode, connected as a cathode follower, maintains a relatively constant cathode current, but the plate current is directly affected by changes in the screen-grid current and/or voltage. Since the output network must be in the plate circuit, satisfactory operation with a pentode would require maintaining both the screen and cathode currents constant. Also, since triode constant-current devices have a much greater stability with respect to tube drift than have pentode constant-current devices, they are almost always used where high accuracy and relatively drift-free operation is desired.[25]

Switching of the constant current source shown in Figure 10 poses somewhat of a problem. As shown in the diagram, the switching signal might be applied to the grid of V_1. However, to reduce the output current to zero, it is necessary to drive the grid of V_1 to a potential more negative than the grid of V_2.

Although such a procedure could be adopted, there are several disadvantages to it:

1. The amplitude of the switching signal must be of the order of 100 volts in order to cut the current source off.
2. A relatively large voltage will appear between the plate and cathode of V_1 for the current source in the "off" position.
3. Grid current, of nearly the same magnitude as the output current, will be drawn by V_2; this may excessively load the voltage reference source and at the same time damage the grid of V_2.

By careful selection of circuit elements, the above difficulties might be reduced to a less significant level; however, it is desirable to examine possible ways of circumventing these difficulties. The following section discusses a few of the methods which might be used. The problem of including a storage medium in the circuit in order to maintain the output current is also considered.

4.32 Ways of Improving the Switching of the Cascaded Cathode-Follower

The primary difficulty in switching the cascaded cathode-follower of Figure 10 is that a potential change on the grid of V_1 is accompanied by a potential change on the cathode of V_1; thus as one attempts to drive the grid beyond cutoff, the cathode voltage also decreases, requiring a very large grid swing before the tube

current is reduced nearly to zero. The most obvious solution to the difficulty is to restrict the change in the cathode voltage of V_1. Several methods are available for accomplishing this. One possibility is to connect a diode to the cathode of V_1, this diode being in a non-conducting state when V_1 is conducting. As the grid voltage on V_1 is decreased, the cathode voltage of V_1 would drop until the diode began to conduct, at which point the cathode voltage would stabilize. A relatively small switching signal could then switch off the current source. Another possibility is to use a switching triode in place of the diode. The grid voltage on V_1 would then be maintained constant and the grid voltage of the switching tube would be varied in order to produce the requisite switching action.

This latter procedure also suggests a third alternative which is shown in Figure 12. Here, a "push-pull" output voltage is obtained by applying switching signals of opposite polarity to the grids of V_1 and V_3, only one of the two tubes conducting in either of the two steady-state positions. One of the greatest advantages of this circuit is that the voltage across V_2 and R_k remains constant except for the very short interval of time when the circuit is being switched from one stable position to the other. The switching portion of the circuit is separated from and at an effectively higher signal level than the current reference portion, thus allowing for some deviations in the grid voltages

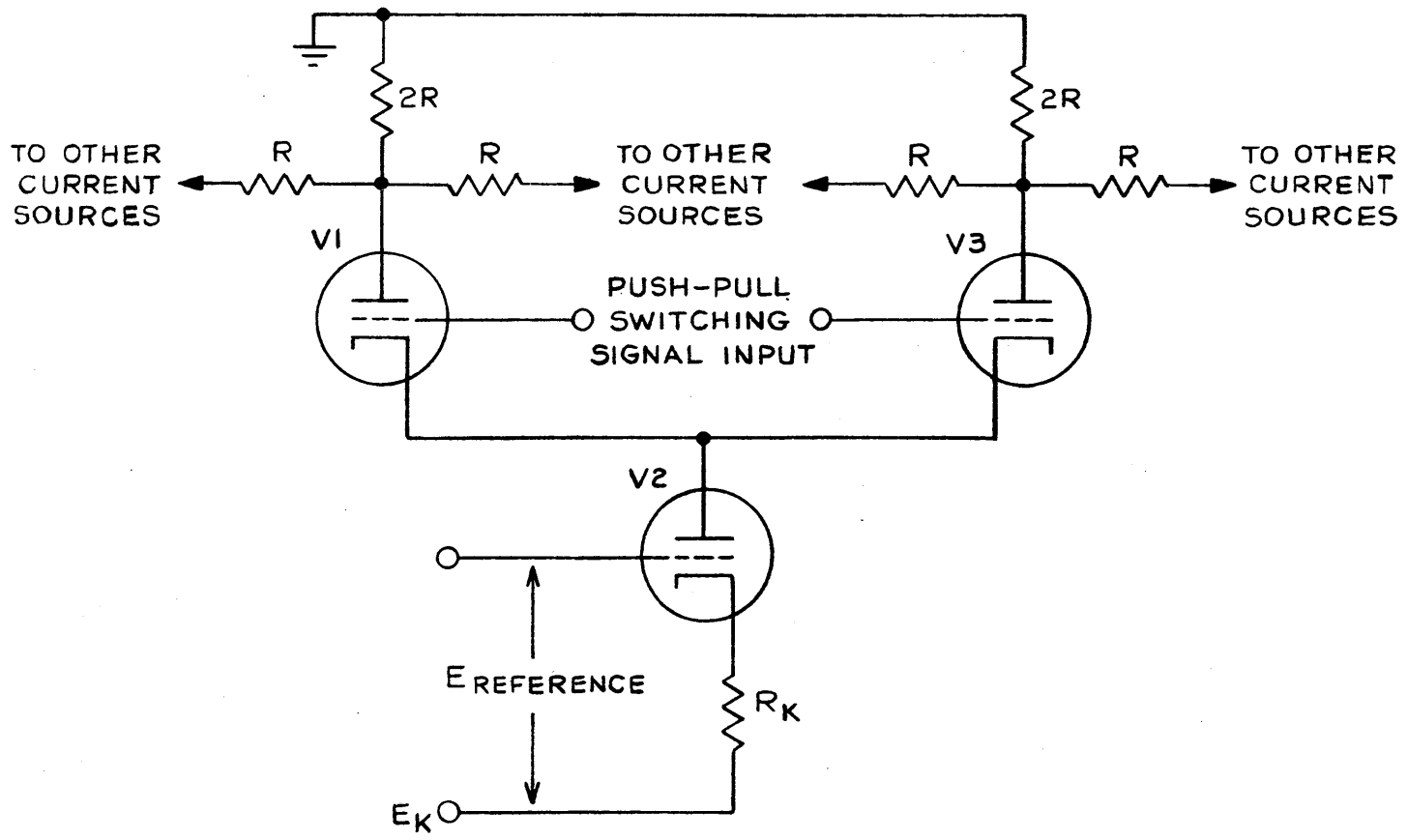
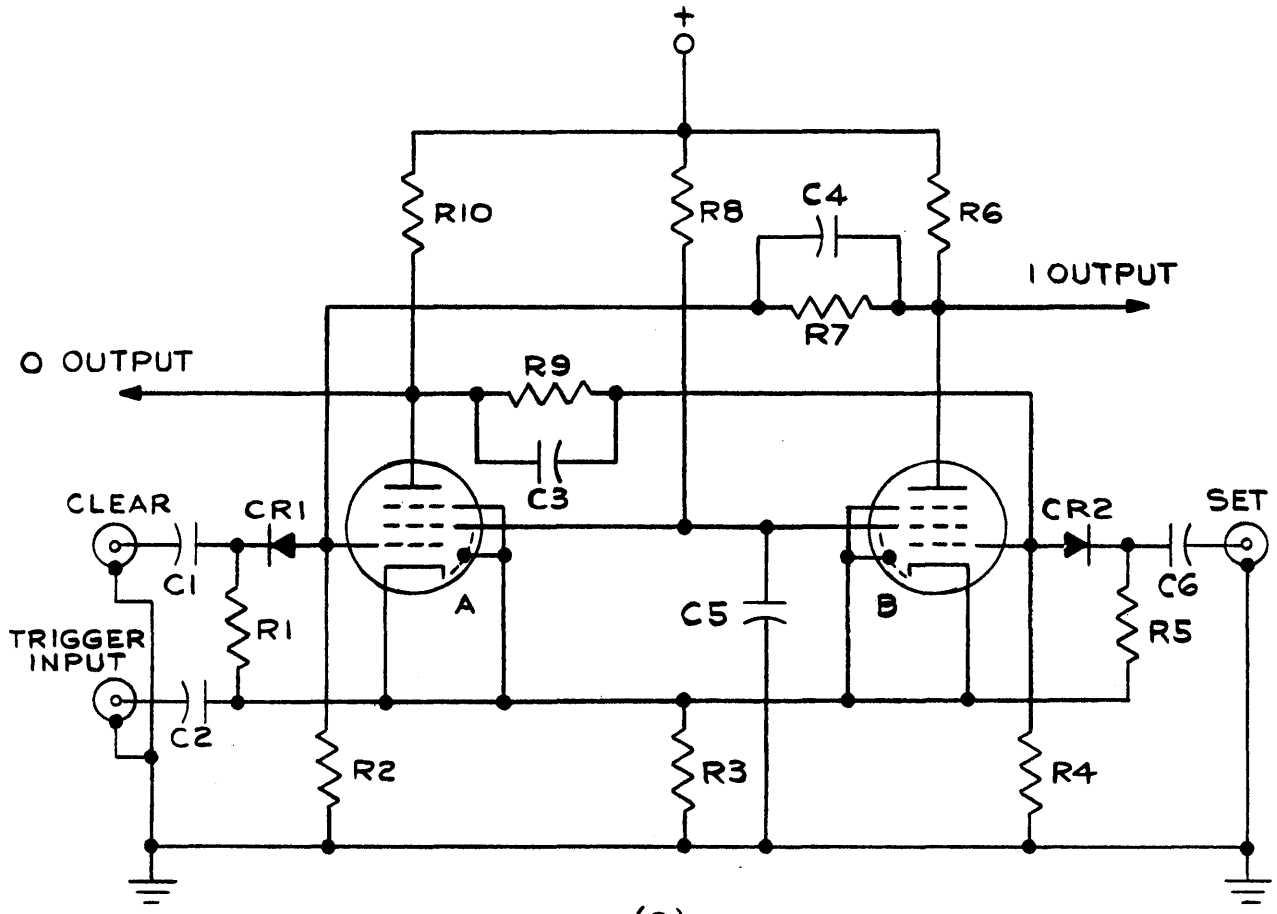


FIG. 12

CONSTANT-CURRENT SOURCE WITH PUSH-PULL OUTPUT AND IMPROVED SWITCHING

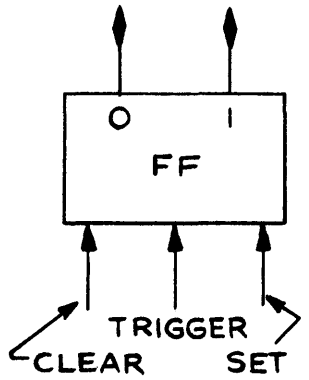
of V_1 and V_3 without destroying the accuracy of the output current. The reference source applied to the grid of V_2 may be a low power, high accuracy source, with the previous problem of current loading of this source being eliminated.

One limitation, however, which occurs in the current source of Figure 12 and in all the other methods so far discussed is the need of applying a switching signal to the circuit for as long as an output current is desired. This requires that some sort of "holding" or storage device must be used in conjunction with each current source. The usual way of doing this electronically is by means of a flip-flop such as the one shown in Figure 13. This device operates so that it is always in one of two stable positions (when it is not being switched), the switching from one position to the other being accomplished by means of short pulses applied to the indicated parts of the flip-flop circuit. The action of the flip-flop will not be covered here, but may be found in several of the references given in the Bibliography: 8, 13, 14. It is sufficient to note that the plate and grid voltage changes of V_1 and V_3 in Figure 12 vary in an identical manner with those of the flip-flop circuit of Figure 13. If the requisite feedback is introduced into the circuit of Figure 12 between the plate of one tube and the grid of the other, the circuit would function quite well as a flip-flop.



(a)

FLIP-FLOP CIRCUIT DIAGRAM



(b)

BLOCK DIAGRAM REPRESENTATION OF FLIP-FLOP

FIG. 13

FLIP-FLOP CIRCUIT DIAGRAM

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However, the interconnection of the output circuit of one tube to the grid of the other tube introduces two major problems:

1. How does one keep voltage variations in the ladder network from changing the state of the flip-flop;
2. What is the effect of the loading of the interconnecting network on the accuracy of the output current?

Both of these problems are important, but the first is by far the most critical. As was pointed out in Section 4.31 above, the magnitude of the voltage fluctuation on the output of a current source can reach a value nearly equal to the magnitude of the maximum output voltage obtainable from the decoder. This holding scheme would thus be useless if a large output voltage is desired. If, however, the push-pull output is unnecessary and only a single output from each conversion channel is desired, it is possible to eliminate the above-mentioned difficulties by the method shown in Figure 14.

The circuit of Figure 14 is comprised basically of two parts:

1. The cathode follower and reference voltage section for yielding a constant current;

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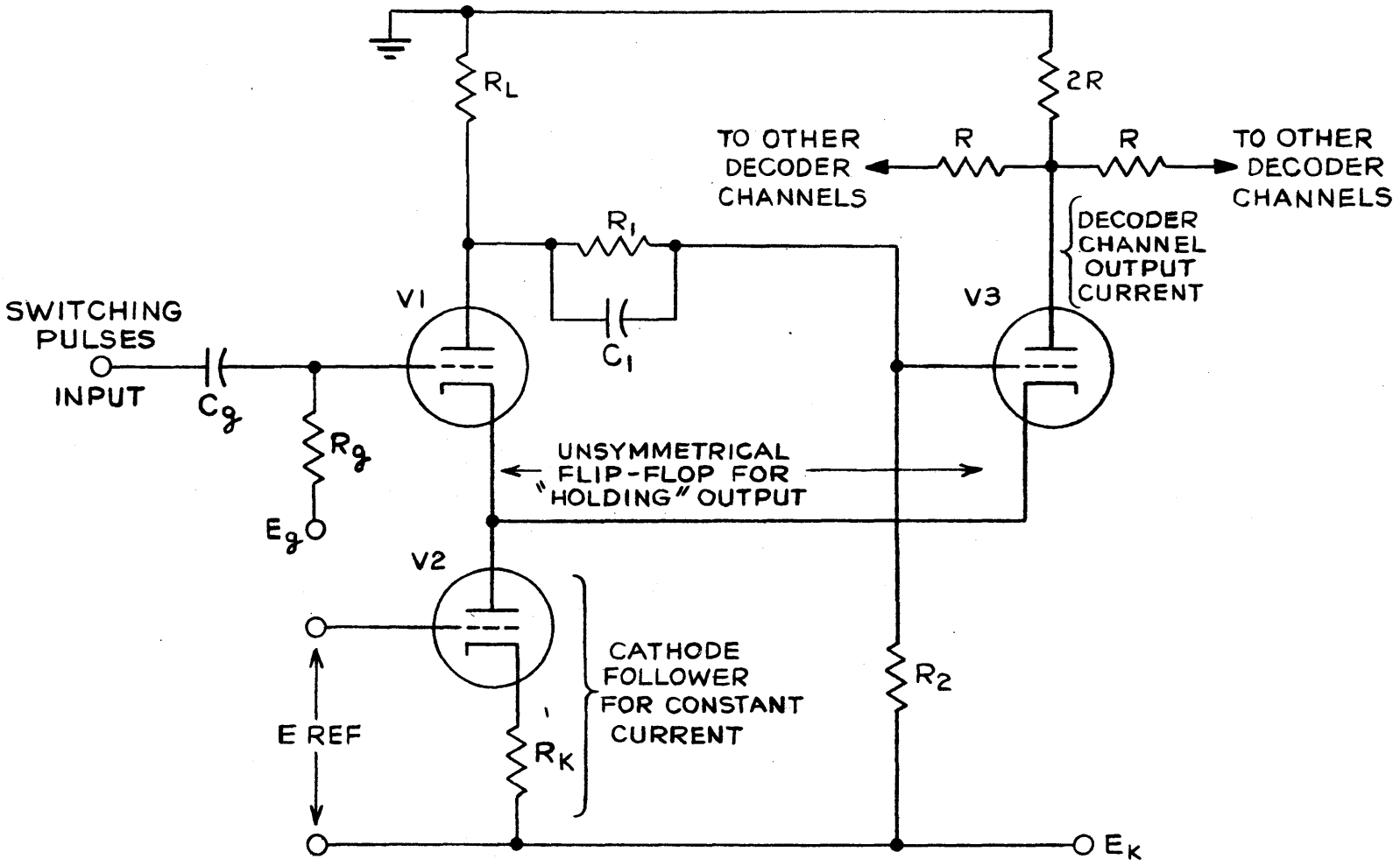

FIG. 14

CONSTANT CURRENT SOURCE INCORPORATING A FLIP-FLOP AS THE "HOLDING" OR STORAGE MEDIUM

2. The unsymmetrical flip-flop for switching the output current "on" and "off," and for remembering and maintaining the last desired position of the switch.

The unsymmetrical flip-flop was so named because, contrary to usual flip-flop design, feedback is introduced by means of a single plate-grid interconnection network, instead of the usual pair of identical networks. The following section discusses in some detail the operation of the flip-flop section of this current source.

4.33 Analysis of the Unsymmetrical Flip-Flop Used As a Storage Medium

As has been mentioned previously, flip-flops are introduced into the decoder circuit in order to remember and maintain the output voltage at the last desired value. Although the flip-flops can be kept separate from the constant current sources in the decoder, it is possible to combine these two functions to some extent, and thus achieve a net reduction in the amount of equipment. The constant current source of Figure 14 is an attempt to achieve such a result.

The action of the unsymmetrical flip-flop of Figure 14 differs in several respects from the action of the usual flip-flop;[8,14]

1. Feedback is introduced by means of only one of the usual two plate-grid coupling circuits;

2. The grid of V_1 is maintained at the same value E_g regardless of the "position" of the flip-flop;
3. As a result of (1) and (2), the cathode voltage of V_1 and V_2 must assume either one or the other of two static levels depending upon the "position" of the flip-flop (the cathode voltage of the usual flip-flop circuit has only one static value);
4. The grid swing of V_3 must be approximately double that of the usual flip-flop in order to allow for the change in cathode voltage mentioned in (3) above.

4.331 Switching the Current Source "On"

The operation of the flip-flop may be analyzed by first assuming V_1 is conducting and V_3 is cut off. The grid of V_1 is at the potential E_g, while the cathodes of both V_1 and V_3 are slightly positive with respect to E_g. In order then for V_3 to be cut off, its grid voltage must be maintained several volts negative with respect to E_g. Now, consider a negative switching pulse applied to the grid of V_1. This pulse will make the grid of V_1 negative with respect to E_g, trying to drive V_1 towards cut-off. At the same time, however, the cathodes of V_1 and V_3 will follow the grid voltage change on V_1 and will themselves be driven negative with respect to E_g. Since the cathode follower is attempting to maintain a constant current, the plate voltage of V_1

and hence the grid voltage of V_3, will remain at almost the same value as before the switching pulse was applied. As the input switching pulse and therefore the cathode voltage becomes more negative, a point is reached at which V_3 begins to conduct.

With the initiation of conduction in V_3, the cathode voltage for both V_1 and V_3 will start to stabilize, since a further decrease in cathode voltage can only attempt to increase the current flow into the cathode follower. Therefore, any further decrease in the grid voltage of V_1 will begin to decrease the current through R_L and hence increase the plate voltage of V_1. By means of the coupling network between the plate of V_1 and the grid of V_3, the grid voltage of V_3 also begins to increase. Because of this increase in grid voltage, the cathode voltage of both tubes now starts to rise, completing the regenerative feedback loop.

For the flip-flop to remain in this new stable condition, the cathode voltage, which had been driven negative with respect to E_g by the negative switching pulse, must rise sufficiently above E_g to assure that V_1 will remain nonconducting after the switching pulse is removed. This also requires that the time interval during which the grid of V_1 is driven negative be long enough to allow the cathode voltage nearly to complete its positive change. In order to switch the flip-flop to its new stable position we see

that, because the grid potential of V_1 did not change, the cathode voltage of both tubes had to assume a new value; and because of this change in cathode voltage, the change in grid voltage of V_3 had to be about twice that of a balanced flip-flop circuit.

4.332 Switching the Current Source "Off"

The switching action of the circuit of Figure 14 with V_3 connecting and V_1 cut off may now be studied. The grid of V_1 is at the potential E_g, while the cathodes of both V_1 and V_3 are maintained far enough above E_g to assure that the grid-cathode voltage of V_1 is below cutoff. If a positive pulse is applied to the grid of V_1, the grid-cathode voltage will begin to rise towards cutoff. As the amplitude of the pulse increases, tube V_1 will start to conduct. With the initiation of conduction in V_1, the plate voltage of V_1 and hence the grid voltage of V_3 will start to decrease. Since the voltage gain between the grid of V_1 and the grid of V_3 is much greater than unity, and since the cathode follower is maintaining a constant current, this decrease in the grid voltage of V_3 will be accompanied by a decrease in the cathode potential of V_1 and V_3. This cathode voltage decrease will only tend to drive V_1 further into conduction and V_3 towards cutoff. The cathode voltage will continue to drop until it reaches a potential which is one or two volts positive with respect to the grid voltage on V_1, at which value

it will tend to stabilize. During this process, the cathode voltage has decreased much less rapidly than the grid voltage of V_3. The end result is that V_3 will be driven beyond cutoff, and V_1 will be in its fully conducting state. Note that the positive switching pulse is assumed to be still on the grid of V_1, holding the grid voltage of V_1 and the cathode voltage of V_1 and V_3 above their static values.

Any further increase in the switching pulse will not affect the circuit, since it will merely drive V_3 further into the cutoff region. A decrease in the switching pulse amplitude will allow the grid and cathode voltages of V_1 to decrease to their static operating values, and the flip-flop will remain in this new position. The time interval during which the positive switching pulse is applied is much less critical than for the case of the negative switching pulse discussed previously. The reason for this is that the cathode voltage of V_1 and V_3 does not have to change in order to cutoff V_3, this being accomplished by the plate-grid coupling circuit between V_1 and V_3.

Although the above analysis has assumed that all switching pulses are applied to the grid of V_1, this is not necessarily the only point at which these pulses might be applied. In fact, the requirement of having both positive and negative switching pulses at the same terminal poses several engineering difficulties. It is possible, however, to apply only the negative switching pulses

to the grid of V_1, and to apply the positive pulses at some other part of the circuit. A positive pulse applied to the grid of V_1 could be replaced by a positive pulse applied to the cathodes of V_1 and V_3, or by a negative pulse applied either to the grid of V_3 or the plate of V_1. The choice of location for the switching pulses is primarily dictated by the need of keeping the pulse input circuits from interfering with each other and from affecting the constant output current of the decoder channel.

4.4 Evaluation of Binary-Weighted Decoding Methods Using Voltage or Current Sources

The reasons for attempting a binary-weighting in conversion devices, including the advantages and disadvantages such a method presents, have been discussed in preceding sections. In this section, an analysis has been made of two basic methods of designing such a binary-weighted decoder. The first method utilized a set of voltage sources whose internal impedances were adjusted so as to give a binary weighting to these sources. The second method utilized a set of equal-valued current sources, the requisite binary weighting being achieved by connecting these current sources into a binary-weighted resistance ladder network. As a result of the analysis of these two methods, two discrete systems were evolved for achieving the common result of a binary-weighted decoder.

Although either of the two methods discussed in this section is satisfactory from a theoretical standpoint, the engineering problems involved seem to dictate the choice of current sources. There are several reasons for making this choice, some of which are the following:

1. The use of voltage sources requires that diodes be used for clamping the reference voltages. It was noticed that drift in diode characteristics would critically affect the accuracy available.
2. The reference voltage circuit in the current source method is not loaded down by a power drain as it is in the voltage source method.
3. The current sources can all be identical, therefore requiring only a single design problem and allowing for easier alignment and checking.
4. The critical parts of the current source circuit which determine the accuracy of the output current are separated from the switching part of the circuit; this is not the case in the voltage source circuit.
5. The current through the cathode follower of the current source circuit (see Figure 13) is maintained constant regardless of whether the current source is in an "on" or "off" position. This removes a considerable part of the problem of drift in R_k,

since its power dissipation is maintained constant. In the voltage source circuit, the power dissipation in the R_x's (see Figure 7) varies depending upon whether the voltage source is in an "on" or "off" position.

It should be noted that the above statements do not give conclusive evidence as to the use of current instead of voltage sources in a decoder circuit. For example, the fact that the current sources introduce a storage medium without the use of additional components is really no advantage, since by increasing to three the number of triodes associated with a voltage source (the same number as in each current source), it too could have a storage medium. However, the balance of favorability appears to lie in the use of current sources. For this reason, experimental tests were made on a decoder which utilized current sources connected to a binary-weighted resistance attenuation network. These tests and their results are discussed in the next section.

5.0 EXPERIMENTAL STUDY OF A BINARY-WEIGHTED CURRENT-SOURCE DECODER

The preceding sections of this report have discussed the engineering problems associated with conversion equipment and have set the background for an experimental study of conversion devices. It was pointed out that the accuracy and conversion time are the basic parameters needed to describe the internal operation of digital-analog conversion equipment, and that these parameters are related to similar characteristics of analog devices. The study of various types of conversion equipment indicated that one of the better ways of accomplishing this conversion is by the use of parallel-channel, binary-weighted methods. Several ways were then discussed as to how this binary weighting might be accomplished, and the conclusion was reached that binary-weighted current sources appear to be the most satisfactory solution to the problem. A method was then described showing how a "holding" or storage medium could be incorporated into the current source circuit without increasing the total number of vacuum tubes. It remains for this present section to discuss the experimental study of this decoding method, along with the final decoder design and the experimental results.

5.1 Voltage Reference Element and Power Supply for Experimental Decoder

In all of the decoding schemes studied in Section 4, it is necessary to supply each decoder channel with several sources of power. For the constant current source decoding scheme of Figure 14, three different supply voltages are indicated — E_g, E_{ref}, and E_k. As was pointed out in the discussion of this circuit, the most important voltage for determining the accuracy of the output current is E_{ref}. However, the other voltages will

also affect the circuit and must be controlled to some extent if external voltage fluctuations are not to affect the operation of the decoder. The design of a power supply regulator which provides the requisite voltages and the selection of a suitable voltage reference element are briefly discussed in this section.

5.11 Possible Voltage Reference Elements

In order to obtain a high-accuracy output current from the current source of Figure 14, and hence to obtain a high-accuracy decoder, it is necessary to have a good voltage reference element for supplying E_{ref}. Five possible methods for obtaining such a reference voltage are briefly discussed below.

5.111 Standard Cells as Reference Elements

One of the most accurate voltage reference elements which can be obtained is the standard cell. This reference element can be obtained with accuracies in the range of 1 part in 10,000 to 1 part in 100,000 but with the restriction that no current may be drawn from the cell. Besides this current restriction, the output voltage of these cells is only slightly greater than 1 volt, so that in order to use them in high-voltage regulators they must be used as a part of an electronic voltage regulator. Although accuracies of better than 1 part in 1,000 have been obtained in this way,[7] the requirements are rather severe when one desires to regulate voltages of greater than 100 or 200 volts. Also, since the standard cell is affected by sudden temperature changes and to some extent by jarring, their use is somewhat restricted.

5.112 Dry Cells (Batteries) as Reference Elements

A very common form of voltage reference device is the common dry cell. Although dry cells are more commonly used for supplying power to electronic circuits without too much regard to their voltage regulating ability, they are fairly good reference elements if a negligible amount of current is drawn from them. The output voltage from one of these cells should not drift by more than 0.1 to 0.2 per cent in a month's time if the cell has not been subjected to large current drains previous to this time. One very useful aspect in connection with these dry cells is the fact that they can be obtained with a much greater terminal voltage than the standard cells, and hence they are easier to use for regulating large voltages.

5.113 Standard Voltage Regulator (V-R) Tubes

One of the most generally used voltage sources for vacuum tube circuits is the V-R tube. This is a special form of gas discharge tube which regulates over an operating current range of from 5 to 30 ma. The major difficulty with these devices is that they can not be relied upon to yield an accuracy of more than about 1 per cent, even with a constant current through them. The reason for this is that they have a rather high noise level caused by their changing discharge domains during their operation.[7]

5.114 The 5651 Voltage-Reference Tube

A second type of glow-discharge voltage-reference tube is the 5651. This is a special type of V-R tube designed to reduce the relatively high noise level normally associated with this type of tube. Section B of the Appendix gives a list of the characteristics for this tube, showing that it can be expected to yield an accuracy of about 0.1 per cent if the

current through the tube is maintained constant. This tube has an operating voltage of around 90 volts so that higher reference levels can easily be obtained by cascading the tubes.

5.115 The New Corona Discharge Tubes

A new voltage-reference tube has been developed which should prove of great value in the regulation of high-voltage circuits. A discussion of many of the characteristics of these tubes is given in Reference 9 in the Bibliography, but it is useful to note the more important characteristics at this point. These tubes were especially designed to regulate voltages in the 1000 volt range, while the allowable currents which they may handle are of the order of 100 μamps. The regulation of these tubes is very good, since in one type a current change from 100 μamps to 200 μamps produces an output voltage deviation of 0.28 per cent. Tubes have been designed for regulating from around 700 volts to over 2000 volts. The primary difficulty with these tubes is that their voltage stability is very dependent upon the ambient operating temperature, the voltage changing by about 0.03 per cent for each Centigrade degree change.

5.12 Power Supply Regulator Design

The preceding section has discussed several of the various types of equipment which may be used to provide a reference voltage in order to maintain an accurate decoding device. Of the various methods suggested, that consisting of the use of a 5651 voltage regulator tube appears to be the most promising, since this device is not too sensitive to temperature changes or deterioration, and also has a fairly good accuracy. The relatively low current capacity of the tube is unimportant, since in the decoder

circuit mentioned in Section 4 it was shown that the high-accuracy voltage reference source did not have to allow for current drains.

The actual regulator which was built to operate in conjunction with the decoder circuit of Figure 14 is shown in Figure 30 (Appendix A). This regulator provides three regulated voltages, whereas it was mentioned in Section 4.31 that for accurate current sources, it is only necessary to maintain a single high-accuracy reference voltage. There are several reasons for regulating the other voltages of the circuit, the primary one being to isolate the decoder circuitry from the fluctuations which might appear on the power supply lines. Another very important consideration which must be met is the need of keeping the voltage on the grid of the triggering tube of the flip-flop at a constant value. Any drift of this voltage will require an increased magnitude of triggering pulse from one of the two input circuits and a decreased magnitude from the other. In fact, if this voltage drifted too far from its optimum value, it would force the flip-flop to remain in one of its two stable positions regardless of the input pulses to the circuit. For this reason, and for the other reason of isolation, the regulator was designed so as to isolate the current sources from all external circuits except the laboratory -150 and -15 volt supplies and the filament supply which is derived from the regulated a-c power lines.

The actual design of the power supply regulator is not at all unusual except for the possible novelty of cascading two electronic regulators. This was done in order to allow a separate regulation of all the voltages as mentioned previously. A complete description of the power supply regulator is unimportant to this study, so only its more important characteristics are listed below:

1. The power supply regulator uses a 900 volt floating power supply from which is derived all of the regulated voltages. This supply is capable of furnishing about 200 ma of current and has a choke-input type filter.
2. An 0A2 is used as the reference element for the less critical voltages (-370 and -800). (It was found during the course of the drift tests that a more accurate reference element should have been used in place of the 0A2.)
3. The -800 volts is regulated by means of a 6AS7 which is capable of handling around 200 ma. Regulation is achieved by means of a 3-stage degenerative feedback amplifier having a total gain of about 20,000.
4. The -370 volts, the voltage which adjusts the operating position of the flip-flop circuit, is regulated by means of a 6L6 regulator tube. This regulator tube derives its input voltage from the regulated output of the 6AS7 circuit and is operated by means of a degenerative feedback amplifier having a total gain of around 300. The primary reason for introducing an additional regulator circuit is for ease in adjusting the circuit voltages and not for any particular need of an increased regulation.
5. The -550 volts, the high-accuracy voltage to the grid of the cathode follower, is obtained by cascading three 5651 voltage-reference tubes. The supply for these reference tubes is obtained from the regulated output of the -370 volts circuit;

the requisite series resistance is a precision wire-wound resistor so as to reduce to a minimum the effects of varying currents on the operation of the voltage-reference tubes.

6. All three of these supply voltages (-800, -550, and -370) were designed to be adjusted so that the optimum operating conditions could be achieved for the decoder circuit.
7. Filament isolation transformers are included in the regulator so that the various current source tubes may be operated with the d-c level of their filaments within 10 or 20 volts of their cathode voltages.

5.2 Final Binary-Weighted Decoder Design

With the basic form of the decoder circuit already evaluated in Section 4, and a set of regulated voltages available with which to operate the circuit, it only remains to decide upon such final details of the decoder design as: the tube type to be used, the method of switching, the choice of resistances for the ladder network, and a few other incidentals. This section discusses each of these briefly and arrives at the decoder circuitry of Figure 28 in Appendix A as the final design.

5.21 The Choice of Tube Type for the Decoder

In the selection of a suitable tube type to be used in the decoder circuit of Figure 14, several factors such as the gain, current capacity, tube capacitances, and sharpness of cutoff must be considered. The most important characteristic, as far as the regulation of the output current is concerned, is a high gain. As was shown in Section 4.31, the effect of voltage variations in the various parts of the current-source circuit are

decreased in proportion to the value of this gain. A desirable characteristic is thus to have as high a gain as possible without sacrificing the other requirements. The high plate current requirement is specified in order that the time constants associated with the output circuits can be kept low (i.e., low values of load resistance) and still obtain a sufficiently large magnitude of output voltage. Low tube capacitances and sharp cutoff are desirable because of the use of the tubes in a form of flip-flop circuit; the speed of switching the flip-flop and the ease with which this switching can be accomplished are highly dependent upon these two parameters.

Two additional quantities which must be considered in the tube selection are the voltage drop across the tube and need for stable operating characteristics; this latter is an obvious one for any high-accuracy device. The desirability of long life is one which arises in any equipment design and is not novel to this particular circuit.

It should be obvious that all of these requirements can not be obtained at the same time, but that there must be some sacrifice in at least some of them if commercially available tubes are to be used. Compromising on such things as reliability, constancy of characteristics, and the other parameters, the final result was the selection of the 12AT7 tube for the decoder circuit. Appendix B contains a complete set of the operating characteristics for this tube.

5.22 Method Adopted for Switching the Current Sources

It was mentioned in Section 4.33 that there are several possible points at which switching signals can be injected into the decoder circuit of Figure 14. The desirability of keeping these input circuits from

interacting with each other suggested their separation. The location of these inputs is also dependent upon not allowing them to interfere with the accuracy of the output current from the current source. For these reasons, it was decided to connect the switching inputs to the grid and plate of V_1 in the circuit of Figure 14; these connections are shown in Figure 28 in Appendix B. All input pulses are negative pulses, so that it is possible to use crystal diodes in order to keep positive pulses from affecting the flip-flop. The input clear channel connecting to the plate of the 12AT7 in Figure 28 is made inoperative by the action of the crystal CR-1 whenever the left hand section of this tube is conducting.

The input set channel is connected directly to the grid of the switching tube of the flip-flop by means of a crystal diode and a capacitor. The capacitor is introduced into the circuit in order that the input pulses may occur at ground potential, while the grid may have a bias of -370 volts. The lower side of R_{17} is returned to ground, whereas it could just as easily be returned to a slightly negative potential to insure that small negative input pulses would not disturb the operation of the flip-flop. The crystal diode, CR-2, fulfills the same purpose as CR-1, that of eliminating positive input pulses into the circuit. This is necessary since, as was mentioned in conjunction with the discussion of Figure 18, it is otherwise possible to switch the flip-flop by applying both positive and negative pulses to the same input terminal.

5.23 Choice of Ladder Network and Cathode-Follower Resistors

The choice of resistors to be used in the cathode-follower and ladder network circuits poses somewhat of a problem, since these resistors

determine, as was pointed out in Section 4, the accuracy with which the decoder output voltage is established. Actually, the cathode resistor is less critical than the ladder network resistors, since the circuitry is such that the current and hence the power dissipation of this resistor are maintained constant to better than 1/2%. This means that once the circuit has been turned on and allowed to warm up, there will be little temperature change in this resistor and hence its temperature coefficient need not be exceptionally low. Thus the primary requirement on the cathode resistor is that it remain drift free; note, however, that it may have a large inductance without affecting the operation of the circuit.

The resistors used in the ladder network pose an entirely different problem. Here, a relatively large voltage swing must be accommodated without the resistors changing their values by any significant amount (0.1 per cent in the decoder being considered). As was mentioned in Section 4.31, the voltage at the center of a long binary-weighted ladder network can reach a value of 1 1/2 times the output voltage from the ladder network. This means that the power dissipation in the resistors will vary from zero for no output voltage to a relatively large value for full output voltage, and thus requires that both the voltage and temperature coefficients of the resistors used in the ladder network be as small as possible. Also, it is desirable, in order to achieve a fast rise time for the output voltage, that the inductance of these resistors be kept as small as possible.

A resistor which has a low inductance and a fairly low temperature coefficient is given in Appendix B. The effect of various values of power rating for the ladder network resistors is discussed under the static testing of the decoder.

5.24 The Checking Circuit

The desirability of including a simple checking and calibrating circuit into the decoder design has also been discussed previously. It was indicated that a simple checking circuit would greatly facilitate the alignment of the decoder and aid in the maintenance of a high-accuracy device. Such a checking circuit is shown in Figure 28 along with the decoder circuitry. The reference element used is the 5651 voltage-reference tube which was discussed above and whose characteristics are included in Appendix B. The output of the reference circuit is adjustable over a small range and is connected to a terminal. A voltmeter may be connected between this terminal and the terminal attached to a standard resistance also incorporated into the checking circuit. The voltage developed across this standard resistance is proportional to the current through it, this current coming from any one of the decoder channels.

The magnitude of the current in each current source is adjustable by means of the variable cathode resistance R_{29} as shown in Figure 28. The output current from any decoder channel is sent to the checking circuit by means of a three-position switch, the positions of this switch being the following:

1. The "ON" position is the normal switch position and allows the output current of the current source to go directly into the appropriate place in the ladder network.
2. The "OFF" position disconnects the output lead of the current source, forcing this current source into the "clear" position. At the same time, if all of the current sources are in the

"OFF" position, all of the resistances of the ladder network are isolated from each other; this facilitates the checking and balancing of these resistances by means of a sensitive Wheatstone bridge circuit.

3. The "CHECK" position directs the output current of a particular current source into the checking circuit, so that this source can be appropriately set in case it has begun to drift. This position of the switch also sends a transient pulse to the flip-flop, by means of the resistance capacitance network, R_{30} and C_{10}, thereby forcing the current source into the "set" position and hence sending the output current to the checking circuit.

5.25 Other Details of the Final Decoder Design

Besides the various items covered above, certain other details of the decoder design are important. Among these are: the inclusion of indicator lights; the coupling network from the plate of the switching tube of the flip-flop to the grid of the current output tube of the flip-flop; the various current and voltage values throughout the circuit. Each of these items is discussed briefly below.

In order to be able to monitor the operation of the current sources when making static operating tests, it was felt desirable to include neon indicating lights in the flip-flop circuit. Normally, these indicator lights would be operated with one of them in parallel with each of the plate load resistances of the flip-flop. However, since a high current accuracy is desired from one of the plate terminals, it was decided to connect both

of the indicating lights to the same plate terminal as shown in Figure 28. These indicating lights have a somewhat detrimental effect upon the operation of the current sources as will be pointed out later.

The value of the coupling capacitance, C_{11}, was determined experimentally, and set at the minimum value required in order to allow the flip-flop to be switched by means of the 0.1 μsec input pulses. The value of 47 μμfd was used since it was a stock capacitance value; however, it was experimentally determined that capacitances of around 25 μμfd would not provide the requisite switching. The time constant for the coupling circuit, with values for C_{11} and the various resistances as given by Figure 28, is approximately 3.5 μsec. This rather large value had considerable effect upon the speed with which the circuit could be switched, but more will be said of this later. R_{31} and R_{34} could have been halved in their resistance values (and doubled in their power dissipation ratings), but this was not felt to be necessary since the operating speeds obtained with the circuit as it stands were fairly satisfactory.

The various voltages occurring in the circuit of Figures 14 and 28 are as follows (nomenclature the same as in Figure 14):

Output plate current = 10 ma

	Tube 1 conducting; Tube 3 cutoff	Tube 1 cutoff; Tube 3 conducting
E_{gk}-1	- 0.27 volts	- 17.2 volts
-2	- 0.37 volts	- 0.6 volts
-3	- 18 volts	- 2.6 volts

	Tube 1 conducting; Tube 3 cutoff	Tube 1 cutoff; Tube 3 conducting
E_g-1	-370 volts	-370 volts
-2	-540 volts	-540 volts
-3	-387.7 volts	-355.4 volts

These values of voltage show that the cathode voltage of the flip-flop part of the current source circuit changes by about 17 volts between the two stable positions, while the grid voltage of Tube 3 has to change by about 32 volts. Reference to Figure 28 in the Appendix would indicate that the change in plate voltage of Tube 1 should be around 56 volts for the magnitude of load resistance and plate current given. The reduction in the expected plate voltage swing of around 8 volts is caused by the loading effect of the neon indicator lamps. Note that the voltage to the grid of Tube 1 has been adjusted so that both tubes of the flip-flop will be driven into the cutoff region by approximately the same amount.

5.3 Static Testing of Experimental Decoder

In order to be able to determine the accuracy with which the decoder is able to maintain its output current, several static accuracy tests were made by allowing certain parameters in the circuit to vary, and also by determining the effect of drift over a long time interval. This section discusses the various tests made and evaluates the corresponding results.

5.31 Effect of Power Supply and Filament Voltage Fluctuations

It was pointed out in Section 4 that one of the reasons for using a cascaded cathode-follower circuit as a current source is that such a circuit is relatively insensitive to fluctuations in all of the supply

voltages except the reference voltage. Figure 11 in this same section showed the equivalent circuit for the cascaded cathode-follower and gave the equation which relates the output current to the various parameters of the circuit. From this diagram and the corresponding equation for the output current it can be seen that the larger the magnitude of the reference voltage, the larger may be the voltage variations in other parts of the circuit without interfering with the accuracy of the output current. For this reason, the reference voltage element consisted of three 5651's in series. It also was felt that such a series arrangement would yield an overall accuracy which would be better than that indicated by the sum of the individual accuracies of the three tubes. The reason for this is that the errors in all tubes would not be expected to occur simultaneously, but rather in a more or less random fashion. This then allows such a circuit to have a percentage accuracy which is higher than that indicated by the accuracy of an individual reference tube. With three of these tubes in series, the resulting reference voltage is around 260 volts, allowing a deviation in the reference circuit of 0.26 volts for a 0.1 percent accuracy.

As was mentioned previously, any variations in the -370 volt supply do not affect the accuracy of the output current, but rather upset the switching action of the flip-flop. The -800 volt supply, however, presents another problem. In Figure 11, variations in E_p (effectively the -800 volt supply in the actual decoding circuit) are divided by approximately the square of the gain of the 12AT7 tubes. The characteristics of these tubes are given in Appendix B; from these characteristics, the gain of a 12AT7 for a plate current of 10 ma is approximately 55. Using this figure, variations in E_p are reduced in their effect on the output current by a factor of about 3,000.

Theoretically then, E_p could be changed by approximately 800 volts before the output current changed by 0.1 percent. Actually, however, variations in the -800 volt supply had a considerably greater effect on the output curremt than this figure allows. A rapid glance at Figure 14, which shows the current source combined with the flip-flop action, will explain the reason for this. As is shown here, any variations in the value of E_k (the -800 volt supply) are reflected onto the grid of the output tube of the current source. The magnitude of this variation can be obtained in terms of the resistances in Figure 14, and is:

$$dE_g = E_k \frac{R_2}{R_L+R_1+R_2} \qquad (5\text{-}1)$$

In terms of the resistance values given in Figure 28, which shows the final design of this decoder, this relationship becomes:

$$dE_g = 0.68\ E_k \qquad (5\text{-}2)$$

As Figure 11 indicates, changes of the voltage on the grid of this output tube are reduced by the gain of the cathode follower tube in their effect on the output current. This means that for an output current deviation of 0.1 percent, the voltage on this grid can vary by about 14 volts, which in turn allows a deviation in the -800 volt supply of about 21 volts. Experimental tests showed that this was approximately the case, and as a result necessitated the rather involved regulator design. In connection with one of the drift tests, the effect of changes in this -800 volt supply will be pointed out.

The only other voltages supplied to this decoder circuit are the filament voltages and the -150 volt laboratory bench supply. From the way in which the -150 volt supply is connected into the circuit, it can be seen that it will have the same effect upon the accuracy of the output current as did the -800 volt supply discussed in the above paragraphs. As for the effect of the filament voltage variations, although such effects were not checked directly on this decoder circuit, such effects were checked for a type 7F8 twin-triode (which has similar characteristics to the 12AT7) operating as a cascaded cathode-follower. For this tube operating at a plate current of 5 ma it was found that the output current deviated by less than 0.05 percent for a filament voltage deviation of $\pm$10 percent, this corresponding to a line voltage change of about $\pm$10 volts. Although it is to be expected that the error in the output current will increase as the magnitude of this current is increased, due to forcing the cathodes of the tubes to operate nearer their region of temperature-limited current flow, the error introduced should not be more than doubled for a plate current of 10 ma. Since the line voltage supplied to the circuitry was regulated to an accuracy of about 1 percent, no difficulty is expected to have arisen from this source.

5.32 Effect of Grid Current on Output Current Accuracy

Although in most circuits, the effects of grid current upon the circuit performance can be neglected, in the present circuitry, this is by no means true. Consider, for example, a grid current flowing in the cathode-follower triode (V_2) of Figure 14 in Section 4. Since the total current through R_k is maintained constant in this circuit, an increase in the grid current of V_2 will decrease the plate current of this tube by an equal

amount, correspondingly decreasing the output current of V_3. It is not the magnitude of the grid current which is important, but rather the change in this current which has the detrimental effect on the output current accuracy. For this reason, it is necessary to keep these current fluctuations to a minimum. For an output current of 10 ma, a change in grid current of 10 μamps will produce a deviation in the output current of 0.1 percent. Of course, the easiest way to remedy this situation is to make sure that the various tubes in the circuit never operate under conditions where the grid current exceeds 10 μamps. However, such operation on the 12AT7, and on similar triodes, requires that the grid-cathode voltage of the triode never becomes more positive than about -1 volt. This, in itself, requires that the triodes must operate with a fairly large plate voltage drop across them.

Besides the lower, or cathode-follower triode, the output tube V_3 of the current source must likewise maintain a grid current constancy of at least 10 μamps. However, when the current source is in the "off" position, if tube V_1 is conducting, a relatively large grid current may be drawn. This grid current is actually beneficial to the operation of the circuit, since it helps to maintain the "off" position of the current source more stable.

5.33 Output Current for Current Source "Off"

It is possible for the current sources to maintain a small value of output current even when the current sources are in the "off" position, since it is impossible for the triodes to act as perfect switches. If, however, this output current is below 10 μamps, it will not introduce an output voltage error of greater than 0.1 percent. The first question which

naturally arises is: what would be the difficulty in allowing a relatively large current flow in the "off" position? The answer to this question is that as far as the output current accuracy is concerned, there would be no problem in allowing this to occur, as long as this current is maintained accurate to better than 0.1 percent. However, there are other things to consider in conjunction with this circuit, such as the effect of plate current flow on the operation of the flip-flop. Plate current flow in the cutoff tube of a flip-flop is very detrimental to stable operation, since slight changes in this current can produce enough of a transient to allow the flip-flop to switch to the opposite stable position.

5.34 Effect of Ladder Network Voltage on Output Current

As was mentioned in Section 5.31 above, the cascaded cathode-follower circuit allows a relatively large deviation in the output voltage without producing a noticeable error in the output current. For the circuitry as given in Figure 28, it was stated that a change in the output voltage was reduced by a factor of 3,000 in its effect on the reference voltage and hence on the output current of the circuit. With the magnitude of reference voltage such as it is in this circuit, it was also stated that theoretically a change of 800 volts in the output voltage would introduce a 0.1 percent error in the output current. In order to check the validity of this, a test was run on the decoder shown in Figure 28, with the following results:

Output Current Deviation vs Decoder Network Voltage

Decoder Network Voltage	Output Current Deviation in percent (%)	
	Stage 1	Stage 2
0	0	0
100	0.01	0.01
160	0.02	0.03
180	0.03	----
190	0.05	0.05
200	0.10	0.09

The above table would tend to disprove the previously stated result that a deviation of 800 volts could be allowed in the ladder network voltage without affecting the accuracy of the output current by more than 0.1 percent, since the table would indicate that this voltage should be nearer to 200 volts. The reason for this is quite simple. As was mentioned in Section 5.32, grid current flow in the various tubes would cause a loss of accuracy. This is exactly what occurred in the present situation. As the voltage was increased across the ladder network (this was actually accomplished by changing the resistance of the ladder network), a corresponding decrease in voltage had to occur across the total current source circuitry. Most of this voltage change occurs across the output tube of the current source; so that with a change of 200 volts on the ladder network, the voltage on this tube changed by nearly the same amount. The net result is that as the voltage of the ladder network is made larger, the grid-cathode voltage of the output tube becomes more and more positive; grid current thus begins to flow, reducing the magnitude of the output current. That this actually occurred was proven by checking the grid current under these conditions, and also by noting that a voltage drop of greater than 200 volts on the ladder network began to cause increasingly larger errors in the magnitude of the output current.

5.35 Drift Tests of Experimental Decoder

In order to determine the changes which might occur in the output current of the current sources, and hence the corresponding changes in the output voltage of the ladder network, several drift tests were made. The block diagram of the circuitry used for these drift tests is shown in Figure

15. As this circuit shows, the output of the two digit experimental decoder is referenced against a voltage reference source. The major part of the output voltage of the decoder network is removed in this way and only the small changes in this output voltage appear at the output of the resistance attenuation network. The main purpose of this network is to introduce a simple means of adjusting the scale of the output equipment, so that the decimal scale of the recording instrument corresponds to the actual percentage deviation in the output voltage of the decoder. The self-balancing galvanometer which is shown in the circuit is merely a fancy d-c amplifier where the drift problem has been overcome by means of a comparison circuit which includes a sensitive galvanometer.

The following sections briefly discuss three of the basic drift tests which were made on the output voltage of this decoder:

1. Relative drift between two decoder channels;
2. Warmup drift of decoder output voltage;
3. Extended drift test of decoder output voltage.

5.351 Relative Drift Between Two Decoder Channels

The most important item in the decoder circuit which determines the sensitivity of the conversion is the accuracy with which each decoder channel's output current can be maintained. For this reason, a test was made of the relative drift of the output voltage of the two decoder channels. In order to accomplish this, it was necessary to modify the arrangement of the equipment such that it was slightly different from that shown in Figure 15, the change consisting of replacing the reference voltage source by one of the decoder channels. A relative drift test should be almost completely

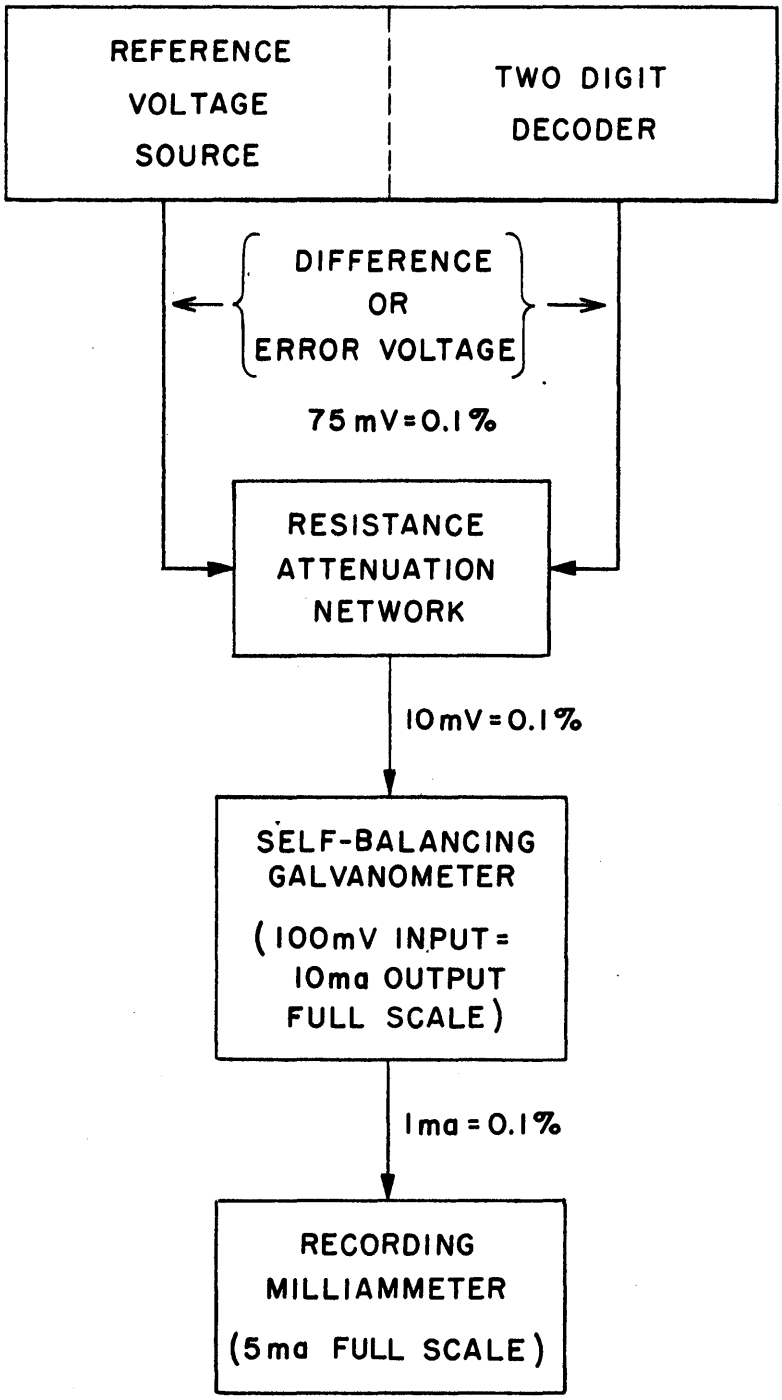

FIG. 15

BLOCK DIAGRAM FOR STATIC TESTING OF TWO DIGIT DECODER

A-45262

insensitive to voltage variations in the reference voltage since this same reference source is common for both decoder channels; therefore, any fluctuations external to the decoder circuitry itself and the voltage measuring network should have no effect on this test.

The experimental results of this relative drift test for a period of 24 hours are shown in Figure 16. As shown on the graph, the total drift for this 24 hour period is 0.08 percent. It is felt that this value is somewhat on the pessimistic side, since the various components in the circuit were not fully aged before the test was carried out. However, it is felt that the curve of Figure 16 provides sufficient information to be able to state that the sensitivity of a completed decoder could be kept to within 0.1 percent for at least a period of 24 hours. Note that if the relative drift is only measured over the 16 hour period extending from 6 hours to 22 hours, the total drift is reduced to about 0.025 percent.

5.352 Warmup Drift of Decoder Output Voltage

The preceding test was able to establish the sensitivity with which the experimental decoder circuit would be expected to operate, but it did not consider the effect of a change in the absolute magnitude of the output voltage. This change in what may be considered the d-c reference level of the output voltage is effected primarily by two quantities: the change in the various regulated voltages supplied to the current sources, and drift occurring in the output circuit ladder network. The drift in the ladder network is primarily due to the initial heating of the network resistors. As these resistors develop a temperature rise due to the sudden application of an output voltage, they will change their resistance values.

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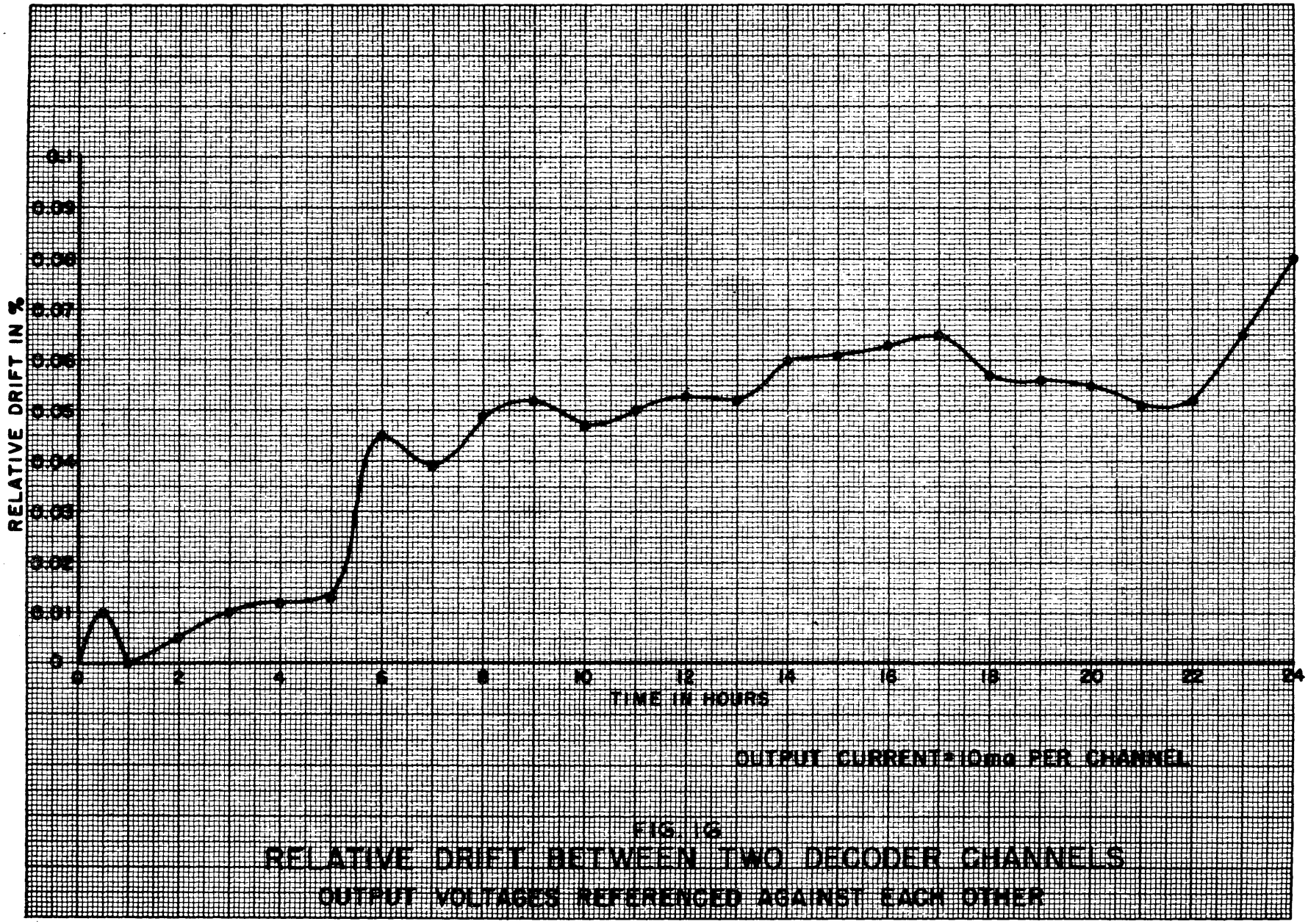

FIG. 16

RELATIVE DRIFT BETWEEN TWO DECODER CHANNELS
OUTPUT VOLTAGES REFERENCED AGAINST EACH OTHER

This change in turn is dependent upon the temperature change in the resistors and their corresponding temperature coefficients.

Figure 17 gives a graph of the warmup drift of the decoder output voltage for the 10 minutes interval immediately after the current sources are turned on. As shown on the figure, two different resistance networks were tested; each of these networks had the same resistance value, but the power dissipation ratings were different. This figure indicates that even though both of the resistance networks were operating at considerably less than their normal rating, the drift in one case exceeded 0.1 percent. In order to keep the drift of these resistances below 0.1 percent, it appears that they should be operated at considerably below their power dissipation rating.

As shown on Figure 17, three tests were made for each of the resistance networks. The importance of these three tests is that they show that the output current of the decoder channels each time returned to very nearly the same value, even though the circuit remained in the "off" position for a considerable length of time between trials. This repeatability indicates that the current sources should come to well within 0.1 percent of the same value on repeated trials. Although several more trials should have been taken to confirm this, it is felt that the results shown are indicative of what could be expected.

5.353 Extended Drift Test of Decoder Output Voltage

In order to determine the long time drift of this decoder circuit and hence to obtain an indication of the frequency of calibration and the corresponding accuracy expected, information as to the output voltage drift

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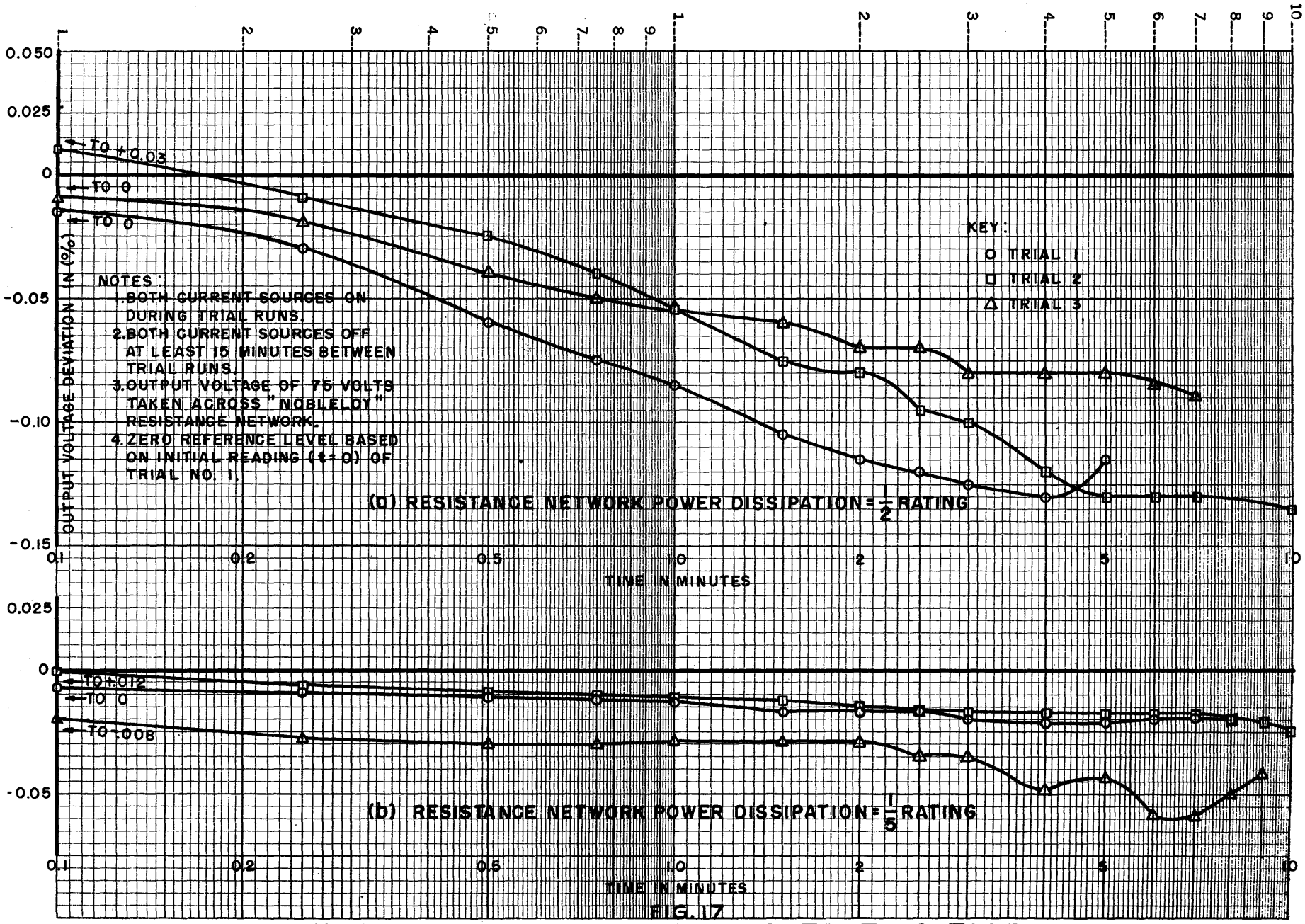
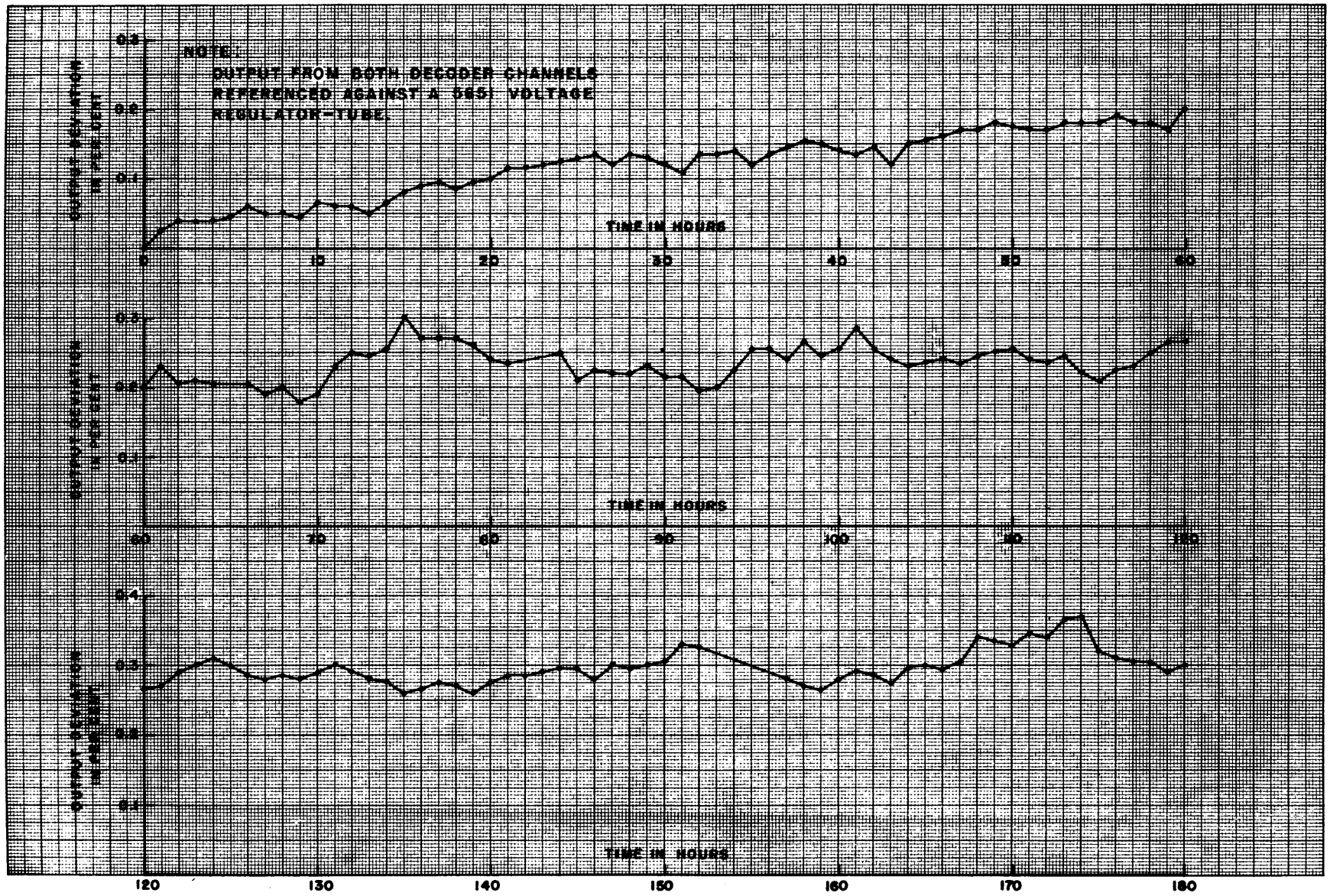


FIG. 17

WARMUP DRIFT OF DECODER OUTPUT VOLTAGE

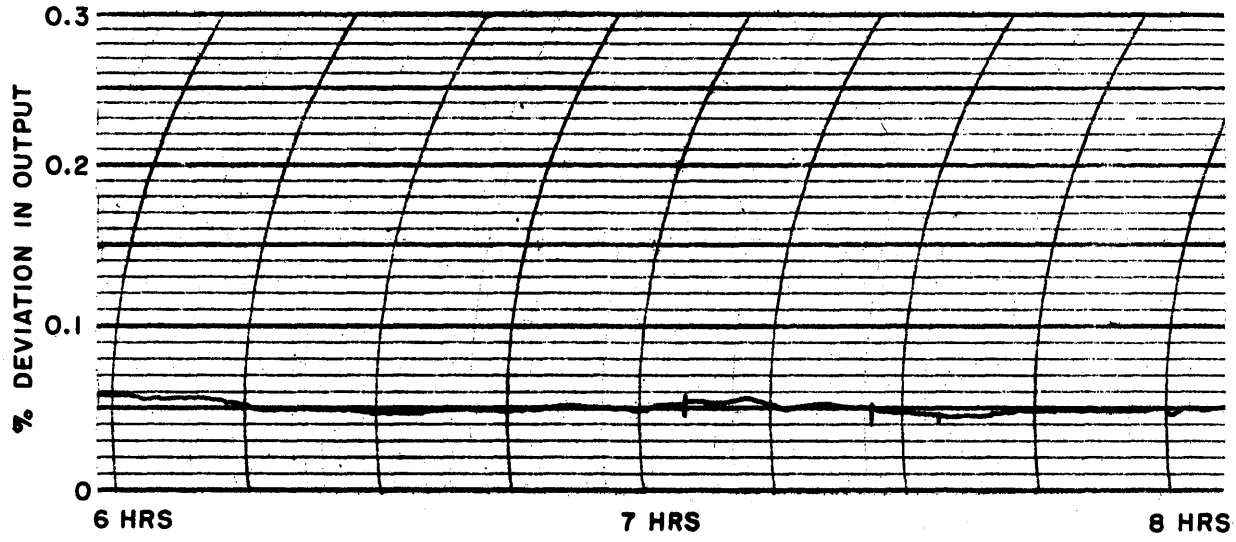
was taken over a period in excess of 7 days. The resulting graph is shown on Figure 18, with the output resistance network being the same as the one tested in Figure 17-b. As shown by the graph, there is an almost continual increase in the error over this period of time, the output voltage of the decoder actually decreasing as a function of time. Two rather long periods of operation occurred for which the total drift did not exceed 0.1 percent: one of these occurred for the 40 hour period extending from 20 to 60 hours; the other occurred for the 50 hour period extending from 120 hours to 170 hours. Two samples of the actual recording obtained for this test are shown in Figure 19. The percent deviation and the time scales have been superimposed and parts of the tape have been cut away in order that it could be shown full scale. The two samples of the chart show two somewhat extreme cases of the amount of deviation occurring in the recording other than the rather consistent drift mentioned above.

Although this extended drift test was quite satisfactory, both the random noise fluctuations and the rather steady decrease in the output voltage of the decoder were larger than one would expect. The principal reason for this total drift of 0.4 percent in a period of 180 hours was found to be due to a faulty operation of the voltage regulator circuit discussed in Section 5.12 above. As has already been mentioned, if the -800 volt supply changes by approximately 20 volts, the output current from the decoder channel would change by approximately 0.1 percent. It was also mentioned that a change of 10 μamps in the grid current of the output tube of the current source would also change the output current by 0.1 percent. Both of these events were found to have occurred during the



STATIC DRIFT TEST OF DECODER OUTPUT VOLTAGE

FIG. 18



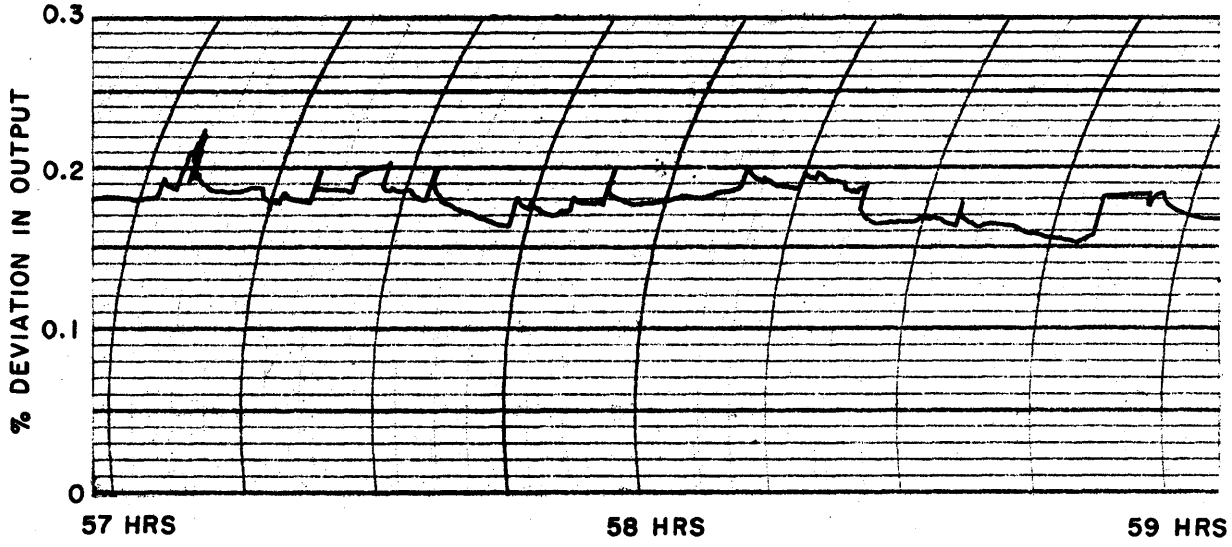


FIG. 19
SAMPLES OF RECORDING TAPE SHOWING
DECODER OUTPUT VOLTAGE

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course of this test, the reason apparently being a change in the operating characteristics of the OA2 used as a reference element for the -800 and -370 supplies. The voltage across this tube apparently decreased, introducing also a decrease in the -800 and -370 volt outputs. The change in the -800 volt supply reflected itself directly onto the grid of the output tube, producing a proportional change in this grid voltage and also a corresponding change in the output current. The change in the -370 volt supply also affected the circuit, but in a more subtle fashion. The decrease in magnitude which occurred in this voltage tended to move the grid of the "off" tube of the flip-flop towards the conduction region. From the rather erratic behavior of the output voltage during the later stages of the drift test, it is felt that this tube actually began to conduct slightly; a plate current of 10 μamps in this tube is sufficient to change the output current by approximately 0.1 percent.

It is felt that the above-mentioned effects account for a large part of the total drift observed during the 180 hour period of this test. Measurement of the -800 volt supply showed that it had drifted more than 25 volts during the test. The difficulty could of course be overcome in any finished decoder design by using a 5651 in place of the OA2 for reference, along with some redesigning of the regulator circuit. It is possible that if this had been done, the resulting curve for the extended drift test would have shown a total deviation of less than 0.2 percent for the total 180 hour period.

5.4 Dynamic Testing of Experimental Decoder

The preceding sections have discussed the final design of the experimental decoder and the associated power supply regulator and voltage reference source. Also the various static tests which were made on this decoder have been discussed and their results evaluated. However, additional tests need to be discussed which indicate the speed of response of the decoder and whether any interaction occurs when decoder channels are being switched simultaneously. The experimental test setup for these dynamic tests was basically that shown in Figure 20, although for certain of the tests minor modifications were made in this setup. The various pieces of equipment, other than the decoder panel itself, are self-explanatory. All of this additional equipment, except for the Synchroscope which is merely an oscilloscope used for measuring high frequency phenomena, is briefly described in Reference 15 of the Bibliography. Of the several dynamic tests made on the decoder, only the more important ones are discussed in this section.

5.41 Input Switching Pulse Discrimination

It was mentioned in Section 4.33 that the flip-flop part of this decoder circuit will respond to both positive and negative input pulses unless special precautions are taken to prevent such things from occurring. Since the desired pulses are both negative and occur over separate input circuits, it is necessary to eliminate any positive pulses which might appear along these input lines. If this is not done, these positive pulses may switch the circuit to the incorrect position; that is, a positive pulse on the "set" input would change the flip-flop to the

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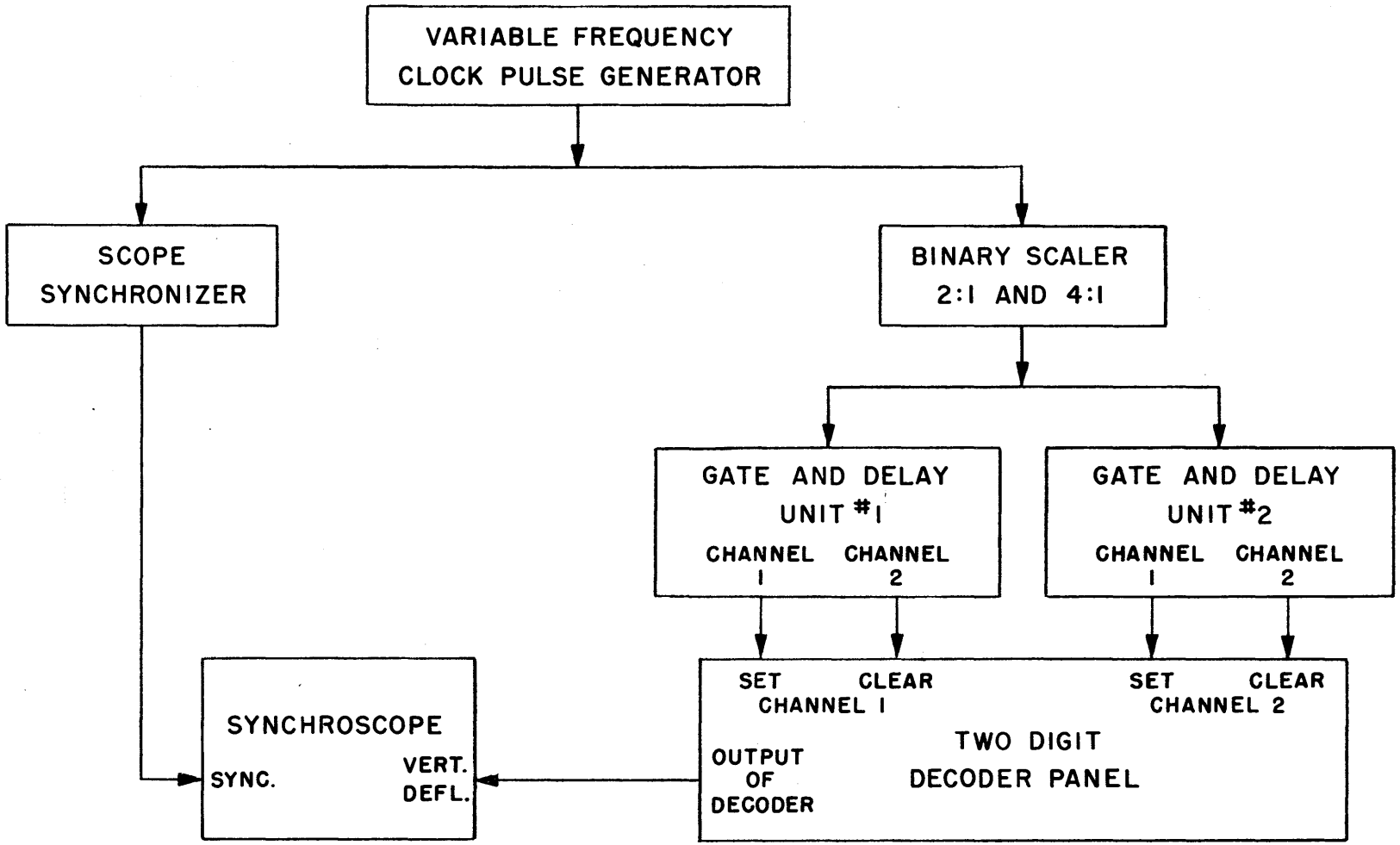

FIG. 20

BLOCK DIAGRAM FOR DYNAMIC TESTING
OF TWO DIGIT DECODER

"clear" position unless special methods are introduced into the circuit to eliminate these pulses before they reach the critical parts of the flip-flop circuit. For this reason, the crystal diodes have been introduced into the input switching circuits shown in Figure 28.

The effect of the crystal diodes in discriminating between positive and negative input pulses is shown in Figure 21. Figure 21-a shows the input pulses which were applied to both the "set" and "clear" input channels. Figure 21-b shows that the positive pulse appearing on the "set" input is completely eliminated before it reaches the grid of the switching tube, except for the negative overshoot which occurred along with this pulse. Figure 21-c shows the effect of the same pair of input pulses applied to the "clear" input channel. Here the negative input pulse has been lengthened and the positive input pulse almost completely eliminated. The reason for the lengthening of the input pulse is that the flip-flop was actually being driven so as to switch it part way to the "clear" position. In order to keep this from occurring and still to allow the circuit to be on the verge of switching, the amplitude of the negative input pulse shown in Figure 21-a was considerably reduced.

With a slightly increased negative input pulse, the flip-flop switched to the "clear" position as shown in Figure 21-d. In this "clear" position, a relatively large back voltage appears across the crystal diode associated with this input circuit. This back voltage is larger than the magnitude of the input pulses, so that neither the positive nor the negative "clear" pulses appear on the plate of the switching tube. In other words, with the flip-flop in the "clear" position it is effectively isolated from any disturbances which may appear on the input "clear" channel.

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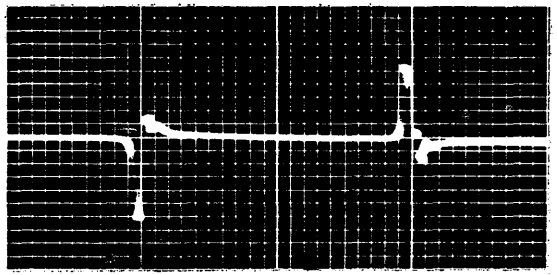
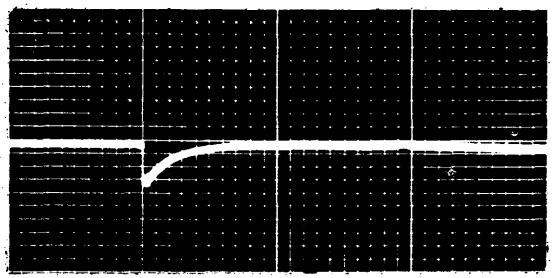
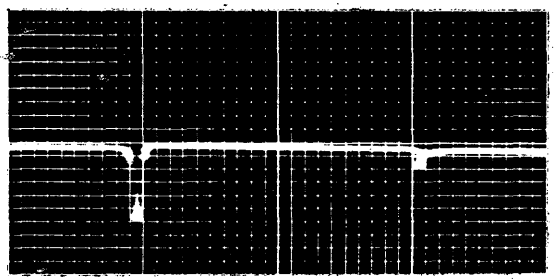


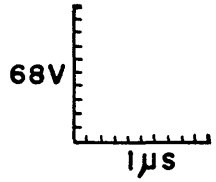
(a) POSITIVE AND NEGATIVE SET AND CLEAR PULSES APPLIED TO DECODER INPUTS



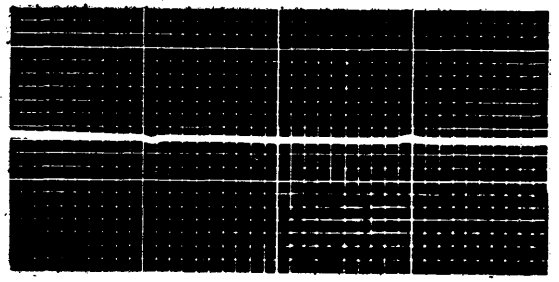
(c) CLEAR PULSES APPEARING ON PLATE (FLIP-FLOP IN SET POSITION)



(b) SET PULSES APPEARING ON GRID



REPETITION RATE = 4KC



(d) CLEAR PULSES APPEARING ON PLATE (FLIP-FLOP IN CLEAR POSITION)

FIG. 21

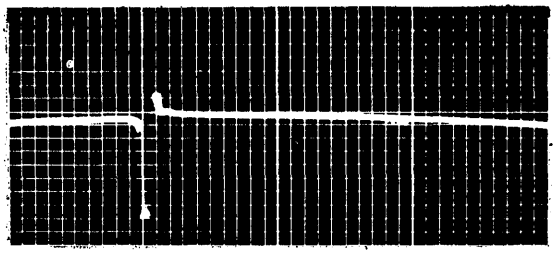
DECODER RESPONSE TO POSITIVE AND NEGATIVE INPUT PULSES

5.42 Single Decoder Channel Response

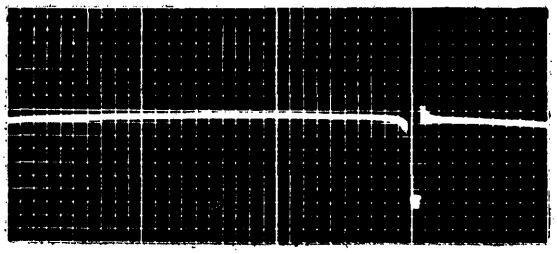
It has been shown that by introducing crystal diodes into the input channel circuitry it is possible to achieve the necessary pulse discrimination in order that the current sources will respond correctly to input signals. Even with the correct input pulses, however, the current sources may fail to respond to these pulses, or they may respond but take a considerable length of time in producing the correct output voltage across the ladder network. Also, the speed at which the current sources can be switched has not been evaluated as yet, nor the requisite amplitude of the input switching pulses. The following paragraphs discuss several of the important characteristics of the response of a single decoder channel to the pulses applied to its inputs.

5.421 Output Circuit Time Constant

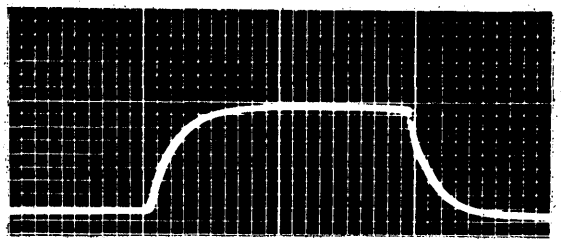
As was pointed out in Sections 2 and 3, one of the most important quantities which it is necessary to know in connection with a decoder is its speed of response. The easiest way of obtaining this speed of response is by determining the time constant for the buildup of the output voltage of the decoder; then, by knowing the accuracy desired, the total time delay necessary for obtaining this accuracy can be obtained. Figure 22 shows the output voltage waveform across the ladder network due to a single current source responding to the input pulses shown. The time constant of the output circuit of this decoder channel can thus be obtained from Figure 22-c by remembering that for an R-C circuit a step change applied to the input will reach 63.3 percent of completion in a time interval equal to one time constant. Applying this to the output waveform of Figure 22-c



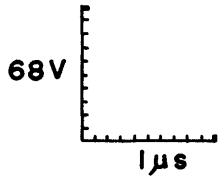
(a) INPUT CLEAR PULSE



(b) INPUT SET PULSE



(c) OUTPUT WAVEFORM



REPETITION RATE = 4 KC

FIG. 22

INPUT SET AND CLEAR PULSES AND OUTPUT WAVEFORM FOR SINGLE DECODER CHANNEL

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we obtain a time constant of approximately 0.2 microseconds. This value of time constant is produced by the shunt capacitance occurring in the output ladder network and the added capacitance of the circuitry used to measure this waveform (the Synchroscope and associated connecting wiring). Since the resistance presented to any one of the current sources is 5,000 ohms, the total distributed shunt capacitance turns out to be about 40 μμf. For an output voltage accuracy of 0.1 percent, it is necessary to allow a time delay of 6.9 time constants for the buildup of the output voltage; this would indicate that each current source is capable of setting up the required output in a total time interval of less than 1.5 microseconds.

5.422 Current Source Waveforms and Time Delays

The preceding paragraph has arrived at the result that the output voltage of the decoder circuit can attain the desired accuracy of 0.1 percent in a time interval of 1.5 microseconds. This is certainly true, if the operation of the flip-flop part of the circuit is such that the magnitude of the output current reaches an accuracy of 0.1 percent in a somewhat shorter interval of time. In order to determine if this occurred, several tests were made of the variations in the cathode and plate circuit waveforms of the flip-flop; the results of some of these tests are shown in Figure 23. All of the waveforms shown were photographed with the flip-flop circuit on the verge of changing from one stable position to the other in order to see at what points on the various waveforms the transition from one stable position to the other occurred.

Figure 23-a shows the cathode voltage waveform of the flip-flop. The initial negative dip of this voltage was discussed in Section 4.33 and

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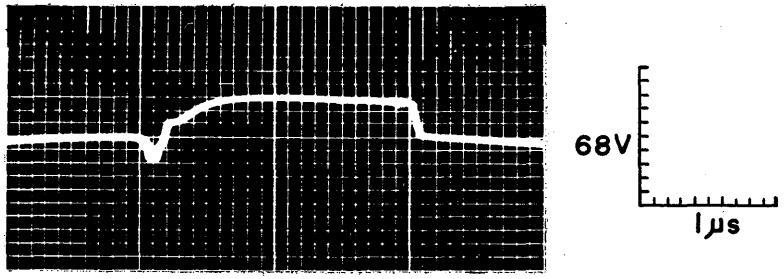
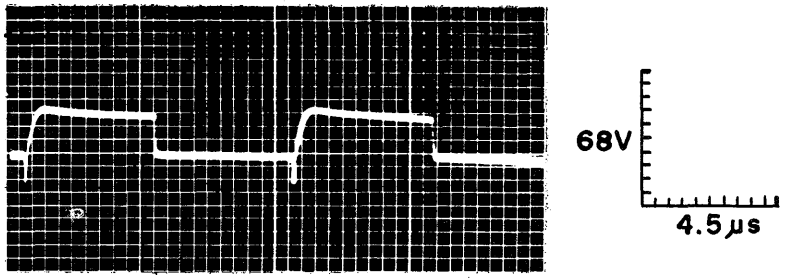
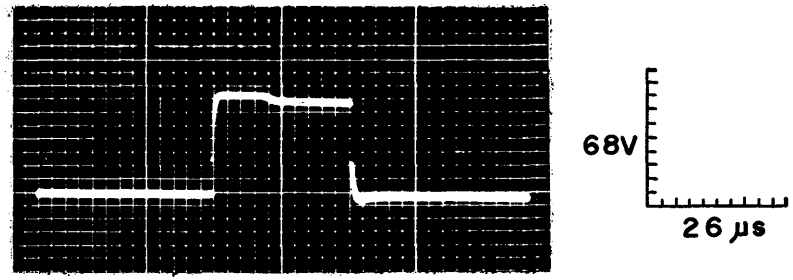


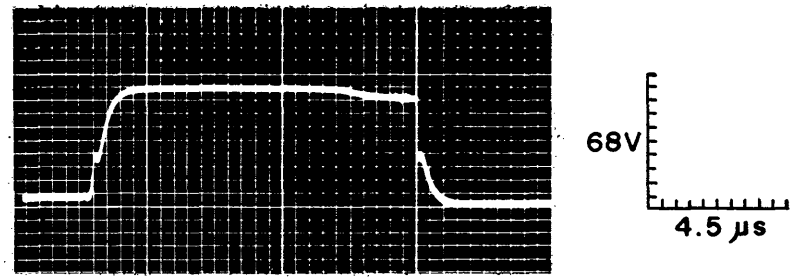
(a) CATHODE VOLTAGE WAVEFORM
REPETITION RATE = 4 KC



(b) CATHODE VOLTAGE WAVEFORM
REPETITION RATE = 100 KC



(c) PLATE VOLTAGE WAVEFORM
REPETITION RATE = 4 KC



(d) PLATE VOLTAGE WAVEFORM
REPETITION RATE = 50KC

FIG. 23
CATHODE AND PLATE CIRCUIT WAVEFORMS OF FLIP-FLOP

need not be repeated here. The figure shows that the transition point for the flip-flop changing from one state to the other occurs for a cathode voltage about 6 volts above its previous level; the time taken for the cathode voltage to reach this point can also be determined from the figure. Figure 23-b shows this cathode voltage at a much higher repetition rate and with a very noticeable decay associated with the more positive sections of the cathode voltage which correspond to the "set" position of the current source. This decay of the cathode voltage must also introduce a change in the magnitude of the output current; however, since the magnitude of the decay is about 5 volts, the output current changes only by about 0.04 percent. The reason for this decay in the cathode voltage is due to the charging of the coupling capacitor of the flip-flop (C_1 of Figure 14, C_{11} of Figure 28). If this coupling capacitor had been adjusted correctly, the voltage changes applied to the grid of the output tube would have divided correctly between this coupling capacitance and the shunt capacitance associated with the tube, and hence the cathode voltage would not have shown this decay.

Figures 23-c and 23-d show the plate waveform for the switching tube of the flip-flop circuit. The most obvious defect in these waveforms is the failure of the more positive part of the waveform to remain constant. The decrease of about 5 volts in this waveform can be explained, however, by the loading effect of the neon indicator lights which occur in the current source circuitry (see Figure 28). The delay in this decrease of the plate voltage is produced by the neon indicator lamps requiring a relatively long ionization time compared to the switching time of the

flip-flop circuit; as indicated by the waveforms, this time lies somewhere between 5 and 10 microseconds. The effect of this 5 volt decrease is to introduce a change in the output current of the decoder channel of about 0.025 percent.

5.423 Maximum Repetition Frequencies for Switching Current Source

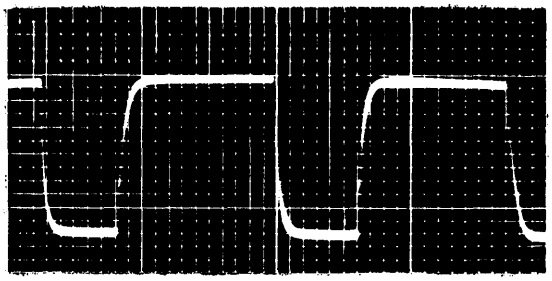
The tests so far discussed have considered the effects of the various parts of the flip-flop circuitry on the accuracy and speed of response of the output voltage of the decoder circuit, but as yet no discussion has been given of the maximum speed with which the current sources can repeatedly be "set" and "cleared". Tests were made to determine what this maximum speed might be and it was found that the current sources could be operated at a 400 kilocycle rate; this allows 2.5 microseconds to "clear" the current source and then to "set" it and obtain the correct magnitude of output voltage. Although this high rate was obtained, it was found that the input pulses to the current source had to have a very large value in order to obtain the requisite switching, the pulses being some 60 to 70 volts in magnitude. As was mentioned in Section 4.33, one of the reasons for needing large amplitude pulses is so that the requisite pulse width may be obtained for switching the flip-flop. Since the pulses used were 0.1 microsecond pulses, it was very difficult to obtain good switching at the higher switching frequencies. However, for the lower switching frequencies of around 100 kilocycles, pulse amplitudes of about 30 volts were sufficient.

5.43 Interaction Tests of Two Current-Source Decoder Channels

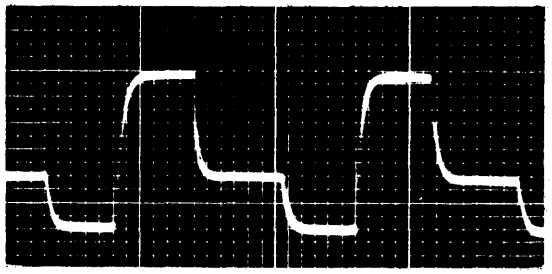
The dynamic tests which have been discussed up to this point have been concerned with the operation of a single decoder channel, and have not considered the possible effect which separate decoder channels may have upon each other. There is a possibility of interaction since the outputs of the separate decoder channels are all interconnected by means of the output ladder network. Therefore, tests were made to see if the buildup of an output voltage produced by one current source would interfere with the switching operation of a second current source. A few of the results of this testing are shown in Figure 24. The three photographs presented indicate that regardless of whether the separate decoder channels are "cleared" and/or "set" at the same time or individually, there is no apparent interaction.

5.5 Summary and Conclusions of Decoder Testing

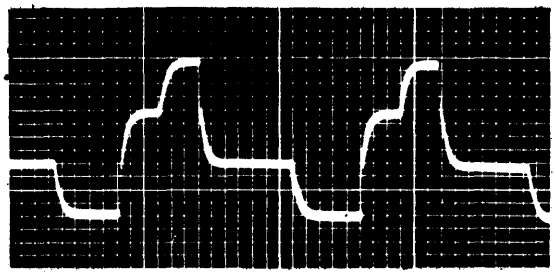
Section 5 has presented the final design of the experimental decoder and the associated voltage regulation and reference source equipment. Several tests which were performed on this experimental decoder were discussed and the results evaluated. From these tests it appears that the speed of the decoder is sufficient such that it may be operated at repetition frequencies exceeding 100 kilocycles. However, in order to use smaller amplitude switching pulses, it would be desirable to use wider pulses than the 0.1 microsecond ones which were available. The output voltage of the decoder was found to come to within 0.1 percent of its final value in less than 1.5 microseconds, so that paralleling of a large number of current sources should not introduce an excessive operating time.



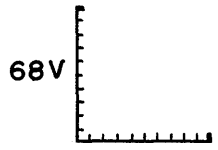
(a) COINCIDENT CLEARING
AND SETTING OF DECODER CHANNELS



(b) COINCIDENT CLEARING
AND INDEPENDENT SETTING OF DECODER CHANNELS



(c) INDEPENDENT CLEARING
AND SETTING OF DECODER CHANNELS



REPETITION RATE = 125 KC

FIG. 24
OUTPUT WAVEFORMS FOR TWO
DECODER CHANNELS

A-45267
F-1328

Drift and accuracy tests were also made in order to determine what accuracy might be expected from such a device. These tests indicated that a 10 binary digit decoder (static conversion accuracy of 0.1 percent) could be expected to maintain the desired sensitivity and accuracy over several days without the need of calibration during this time. The simple calibrating circuit which was included in the decoder proved to be invaluable in making initial alignments and these subsequent calibrations. With the decoding circuit tested, it was found that output voltages of 100 volts could be obtained with little difficulty, this voltage being more than sufficient to operate the usual types of output equipment.

As a result of the testing carried out on this decoder, several modifications or changes have suggested themselves. One of these was mentioned in conjunction with the power supply regulator. Drift which occurred in this regulator is believed to have greatly affected the results of some of the static drift tests which were taken. The primary cause of this drift was traced to the 0A2 voltage regulator tube producing changes in the -800 and -370 volt supply circuits. It is felt that a different voltage regulator circuit should be used with a 5651 voltage-reference tube used in place of the 0A2.

Several other changes have been suggested by the various tests. It was suggested that the neon indicator lamps should be eliminated if possible since they add to the complexity of the circuit and also affect the switching operation and accuracy of the circuit. The resistance coupling circuit connecting the plate of the switching tube of the flip-flop to the grid of the output tube of the flip-flop should be decreased in

value so that a smaller time constant for the coupling capacitor can be obtained. This capacitor, in turn, should be more closely adjusted to its optimum value than was done. Finally, in order to more closely match the several current sources which would be used in a high accuracy decoder, 1 percent resistors should be used throughout instead of the 5 percent ones used in the experimental decoder.

6.0 ADDITIONAL PROBLEMS IN THE USE OF BINARY-WEIGHTED DECODERS

The preceding section discussed the final design and testing of a binary-weighted decoder. The results obtained would indicate that this method of decoding can be used in systems which require both a fast operating speed (short conversion time) and a high degree of accuracy (large binary number capacity). However, certain engineering problems associated with the system use of these decoders as yet have not been considered.

An important use of binary-weighted decoders occurs in one of the encoding schemes discussed in Section 3; associated with this use are several additional circuitry problems besides those mentioned in Sections 4 and 5. Also in many applications it is not possible to place the decoder equipment and the device which utilizes the decoder output voltage in the same location; the problem of accurately and rapidly transmitting the decoder output voltage becomes very important in this case.

The following sections briefly discuss the above two situations along with some of the possible solutions. Following this, a general summary is included which briefly reviews the principal results of this report. Finally, several suggestions are made for possible further study in the field of digital-analog conversion equipment.

6.1 Use of a Binary-Weighted Decoder for Encoding

In Section 3.1 of this report, several methods were discussed for converting from analog quantities to digital representations of these quantities. One of the most favorable of these methods consists in using a binary-weighted decoder in a type of step-comparison conversion device. In this device a serial comparison is made between an internally generated

voltage, which is proportional to each binary digit, and the analog input voltage. Since one of the most critical parts of such an encoding device is a binary-weighted decoder, it is worthwhile to consider what additional problems would be encountered in such a system.

Figure 25 gives a block diagram of a possible form of such a step-comparison conversion device. This diagram shows that an encoder of this type consists of three main parts:

1. The d-c generator which develops a comparison voltage proportional to the binary number presented to it.
2. The amplitude comparator which compares the magnitude of the internally generated voltage against the analog input voltage.
3. The pulse distributor which controls the operation of the d-c generator and establishes the correct binary number output.

The d-c generator and the associated flip-flops for storing digital information have already been thoroughly discussed in Sections 4 and 5. The operation and the associated problems of the amplitude comparator and the pulse distributor are discussed briefly in the following paragraphs.

6.11 The Pulse Distributor

It was mentioned in Section 3.12 that the step-comparison conversion method must make a series of comparisons between the internally generated voltage and the analog input voltage, the number of comparisons equaling the number of digits corresponding to the binary number capacity of the conversion device. Since these comparisons may not be carried out simultaneously, it is necessary to progress serially from the largest

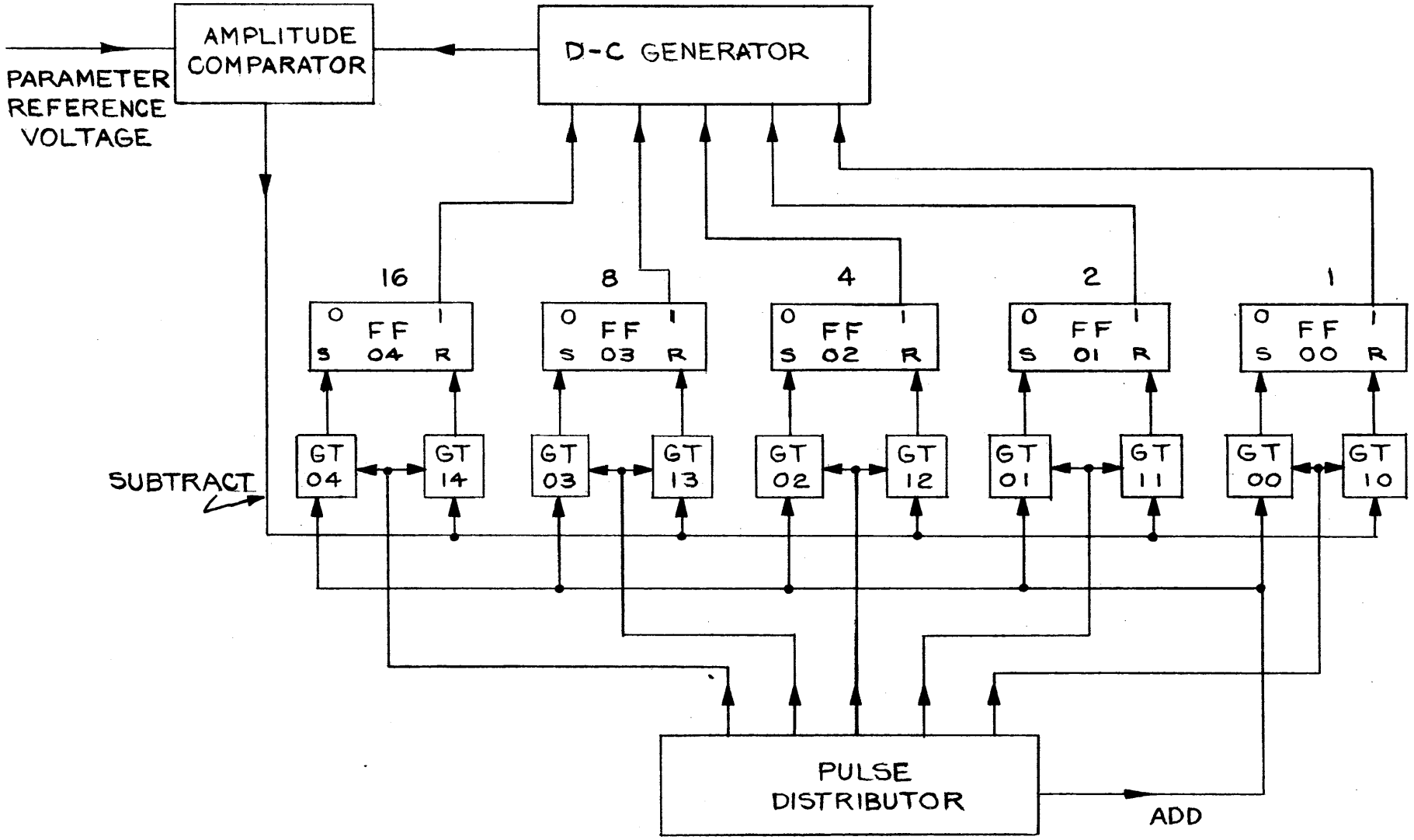


FIG. 25

D-C STEP-COMPARISON CONVERSION METHOD

binary digit down through the smallest; it is this job which the pulse distributor must fulfill. The operation of the pulse distributor may thus be summarized as follows:

1. Upon the receipt of some form of information which tells it to carry out a conversion, the pulse distributor must first clear all of the flip-flops associated with the d-c generator; that is, the decoder section of this conversion device must be cleared.
2. The pulse distributor then sends a broad pulse or gate to the two gate tubes associated with the largest binary digit of the conversion device (this is the 16's digit in Figure 25); this pulse opens both of the corresponding gate tubes so that they will pass any information (pulses) which is being carried by the "add" or "subtract" lines.
3. Immediately following the initiation of this broad pulse, and the corresponding opening of the gate tubes, the pulse distributor sends out a single pulse over the "add" line; this pulse sets the flip-flop corresponding to the largest binary digit of the conversion device.
4. The pulse distributor then waits to see if a "subtract" pulse will be sent out by the amplitude comparator; this subtract pulse resets the flip-flop if the internally generated voltage is greater in magnitude than the analog input voltage.

5. After waiting a sufficient length of time to insure the receipt of a "subtract" pulse, if one is to be sent, the pulse distributor moves on to the next lower-valued binary digit and repeats steps 2 through 4; this process is continued until each binary digit has been compared against the analog input voltage.
6. Following the last comparison, the pulse distributor ceases operation, at the same time leaving the digital representation of the analog input voltage set in the various decoder flip-flops; other circuitry would then remove this number and use it in the desired fashion.

The above description should indicate that the pulse distributor is really a very simple device consisting primarily of a counter and a few delay circuits. Its operation is not at all critical except for the necessity of allowing sufficient time for the return of a "subtract" pulse, following each "add" pulse. However, as was pointed out in Section 3.3, this time interval should be kept as short as possible in order to achieve a high conversion speed and hence more easily match the conversion device to the external system. The factors which determine this minimum time between comparisons are: the time for the decoder to set up the comparison voltage and the time it takes for the amplitude comparator to complete a comparison and send out the "subtract" pulse. An idea of what this minimum time is may be obtained by remembering that the experimental decoder discussed in Section 5 was able to set up an output voltage to an accuracy of about 0.1 percent in less than 1.5 μsec. Allowing for an additional 1 μsec

for the amplitude comparator to complete its comparison, the minimum time delay between comparisons is thus around 2.5 μsec. This time for a single comparison, along with a conversion accuracy of 0.1 percent (i.e., 10 binary digits), will give a total conversion time of approximately 25 μsec. The pulse repetition frequencies for the pulse distributor and the decoder flip-flops are also determined by these values; the pulse distributor must operate at a maximum frequency of 400 Kcps, while the various decoder flip-flops are "set" at a maximum frequency of 40 Kcps.

The results obtained above for the various operating frequencies indicate that the pulse distributor is not a critical part of the conversion device since its operating speed is limited by components external to itself. Also, the pulse distributor does not have to meet the rather rigid accuracy requirements which are placed on the operation of the d-c generator and the amplitude comparator. The design of the pulse distributor for this type of conversion device should therefore pose no difficult problems.

6.12 The Amplitude Comparator

Outside of the d-c generator, the amplitude comparator is the most critical part of the encoding system shown in Figure 25. It is the job of this device to detect any small differences between the two voltages applied to it. Furthermore, it must be able to determine which of the two voltages is the larger so that it only generates an output signal for the correct input conditions. In high sensitivity systems the operating conditions for the comparator become rather severe. For example, if the d-c generator can set up 1,024 different voltage levels (this corresponds to 10 binary digits), the comparator must be sensitive enough so that it can

detect a difference corresponding to a single decoder increment between the analog input voltage and the internally generated comparison voltage. The amplitude comparator must also be able to maintain this same sensitivity regardless of whether it is working at the 1st or the 1,001st increment level. Therefore, a relatively large voltage magnitude for each increment will simplify the comparison for any single input voltage level; however, it will also require a comparator which is capable of handling input signals that change over more than 1,000 of these large-valued increments.

Although amplitude comparison schemes are quite common (the literature contains several such circuits with comparison sensitivities of better than 0.1 volt[2,3,7,25]), the operation required in the step-comparison method is more severe than that which is normally encountered. Usually the amplitude comparators are operated in conjunction with an internal voltage generator which yields a uniformly changing comparison voltage. The step-comparison method, on the other hand, introduces sudden large changes in this comparison voltage. This in turn places the additional burden on the comparator of rejecting these large jumps; at the same time, it must be able to respond to a change in the internally generated voltage of only a single increment. Such factors would have to be studied before one could obtain a satisfactory step-comparison conversion device.

6.13 Multiple Input Channels

It was mentioned in Section 2 that the amount of equipment which one must use in making a conversion is very important. It was also suggested that it is sometimes possible to use a centralized piece of conversion

equipment in connection with several input channels. The conversion method of Figure 25 lends itself rather well to such a scheme. If multiple inputs are to be used with this device, a separate amplitude comparator may be supplied to each of these inputs, the output of the d-c generator connecting directly to each of the comparators. The selection of the desired input channel and the exclusion of all others during a particular conversion is readily obtained by gating the output signals from the comparators. If only the desired "subtract" signal is allowed to reach the decoder section of the conversion device, the conversion will be carried out to correspond to the commands from only this particular comparator. One advantage of this type of input channel selection is immediately obvious -- only error signals are switched or gated.

A possible difficulty which might occur when one uses multiple input channels, is the problem of rapidly and accurately transmitting the output voltage of the d-c generator to all the amplitude comparators. The following section discusses several of the ways in which such a voltage transmission can be carried out.

6.2 Transmission of the Decoder Output Voltage

In several of the systems which require the use of a digital-to-analog decoder, the output voltage of this decoder must be transmitted to some remote location. An example of such a required transmission was presented in Section 6.1 in conjunction with the use of multiple input channels to a conversion device. In fact it may be stated that, in any system requiring the multiple reception of the output voltage of a decoder, a transmission problem will occur.

In order to transmit a signal from one location to another it is necessary to have some form of transmission line. The form which this transmission line will take depends to a great extent upon the desired accuracy and the time allowed for the transmission. If the transmission is to take place over fairly long distances, stray pickup becomes a difficult problem; as a result, it is usually necessary to shield the information carrying part of the line from such pickup. However, the very act of shielding will have an adverse effect upon the time it takes to establish the voltage level at the receiving end of the transmission line.

The major problem in using transmission lines to carry the output voltage of a decoder circuit is that useful sizes of transmission lines have characteristic impedances of around 100 to 300 ohms. In order to keep from having reflections along the line, and hence to be able to set up an accurate voltage at the far end of the transmission line in as short a time as possible, it is necessary that the line be terminated in a resistance having a value equal to this characteristic impedance. If a decoder is connected directly to this transmission line, it must develop its output voltage across a relatively small resistance; this in turn will result in a relatively small output voltage. It is possible, however, to remedy this situation by the use of d-c amplifiers or cathode-followers. The following paragraphs discuss three possible ways in which this high-speed transmission can be carried out.

6.21 Use of D-C Amplifiers at the Output of the Transmission Line

The primary objection presented above was that the characteristic impedance of the transmission lines is so low that a sufficiently large

output voltage can not be obtained unless a large time delay is allowed for charging the transmission line. One of the most direct ways of overcoming this problem is to connect the output of the decoder directly to the transmission line; at the receiving end of the transmission line, one then installs a d-c amplifier which amplifies the resulting small voltage until it reaches a usable level. The main difficulty in such a transmission scheme is in maintaining the amplifier at the receiving end of the transmission line linear and free from drift. Special precautions also might have to be taken in order to keep the transmission line from picking up small noise signals.

As an example of the difficulties which may be encountered, it might be helpful to consider how one would use this scheme to transmit the output voltage of the decoder discussed in Section 5. It was pointed out in that section that the output voltage of such a decoder could achieve an accuracy of 0.1 percent in 1.5 μsec, at the same time reaching a peak amplitude of about 100 volts. For this decoder connected directly to a transmission line terminated in its characteristic impedance of about 200 ohms, the same accuracy could be achieved but at a much reduced output voltage amplitude (see Section 4.3). The decoder discussed in Section 5, for the specified tube currents of 10 ma, would thus yield a peak magnitude of output voltage of about 4 volts. The d-c amplifier at the receiving end of the transmission line must then be able to amplify this 4 volt input to the original level of 100 volts without introducing any appreciable error. It is also readily seen that the noise pickup along the transmission line must be kept below 4 mv if for an accuracy of 0.1 percent the small decoder digits are to be significant.

These problems of the noise pickup by the transmission line and the linearity of the d-c amplifier are the important determining factors in using this scheme. The noise pickup is actually the more serious problem, since it affects both the sensitivity and accuracy of the decoder output voltage; whereas, any non-linearity in the d-c amplifier introduces a decrease in accuracy but does not affect the sensitivity. If this decreased accuracy can be tolerated, the amplifier design is not critical.

6.22 Use of Cathode-Followers at the Output of the Decoder

The transmission system discussed above considered the use of d-c amplifiers at the receiving end of the transmission line to increase the output voltage to a higher and more usable level. However, one of the primary difficulties of the scheme is the noise pickup along the transmission line due to the low signal voltage level. Instead of using the amplifier at the receiving end of the transmission line, it is possible to feed the output voltage of the decoder directly to the grid of a cathode-follower; the output of the cathode-follower in turn feeds the transmission line. In this case, the output voltage of the decoder is not reduced in magnitude since it is not loaded down by the transmission line. Thus for a decoder output voltage of 100 volts, the cathode-follower circuit will give very nearly 100 volts at the receiving end of the transmission line.

If the transmission line is terminated in a resistance equal to its characteristic impedance, the cathode-follower must provide a very large charging current so that the line voltage will reach its peak value in a short interval of time. For the transmission line considered above, which had a characteristic impedance of 200 ohms, the cathode-follower must

be able to supply a maximum current of at least 500 ma in order to produce a peak output voltage of 100 volts. With a peak voltage of 100 volts, and a decoder accuracy of 0.1 percent, the noise level may now approach 100 mv; this is an improvement by a factor of about 25 over the d-c amplifier transmission scheme.

The linearity problems associated with the amplifier discussed in the previous example are also important for the cathode-follower. Although the operation of the cathode-follower is such that the drift problem is considerably reduced, with an input voltage swing of around 100 volts the linearity problem for the cathode-follower might prove to be every bit as important as for the d-c amplifier.

6.23 Use of a Three-Conductor Transmission Line

The cathode-follower was introduced into the output circuit of the decoder in order to charge the transmission line in a minimum amount of time and still allow a large value of output voltage. It was found, however, that the cathode-follower may also introduce non-linearity into the transmitted voltage, thus decreasing the accuracy of the output voltage to a value which may be considerably less than the sensitivity with which this voltage can be set up. In order to improve this accuracy, it would be helpful if the line-charging operation of the cathode-follower could be separated from the signal carrying part of the transmission line. A possible method for accomplishing this is shown in Figure 26. In this figure a three-conductor transmission line is used for carrying the output voltage of the decoder to the remote locations: the inner conductor of this line carries the output voltage of the decoder, while the output of the cathode-

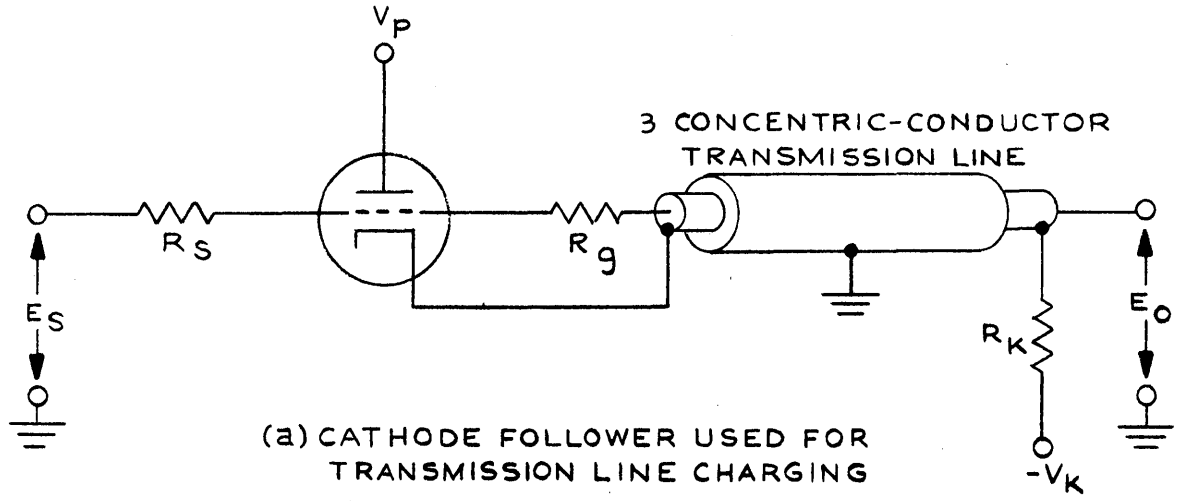
follower is connected to the middle conductor. The cathode-follower is thus used only to charge the transmission line. As a result, any drift in the cathode-follower and its associated circuitry will merely change the time it takes for the output voltage to reach its final accuracy; this drift will not interfere with the accuracy or precision of the output voltage.

Appendix C of this report derives the relationships which hold for the buildup of the output voltage of the transmission line; the approximations used in arriving at the equivalent circuits shown in Figure 26-b are also discussed in this appendix. The derivation shows that, if R_g has a value of zero, the cathode-follower has the effect of reducing the time constant of the circuit presented to E_s by the factor:

$$A = 1 + \frac{\mu R_{eq}}{r_p} \qquad (6\text{-}1)$$

where R_{eq} is the parallel combination of R_k and r_p. The time it takes for the output voltage to reach the desired accuracy is thus directly dependent upon the value of μ for the cathode-follower. In this respect, the cathode-follower may actually be driven by an amplifier, the gain of this amplifier corresponding to μ in equation 6-1. With a sufficiently large gain, and also a large current-handling capacity for the cathode-follower circuit, it is possible to set up the output voltage of the transmission line in a relatively short time.

One additional parameter which should be considered in connection with the cathode-follower is the effect of R_g upon the operation of the



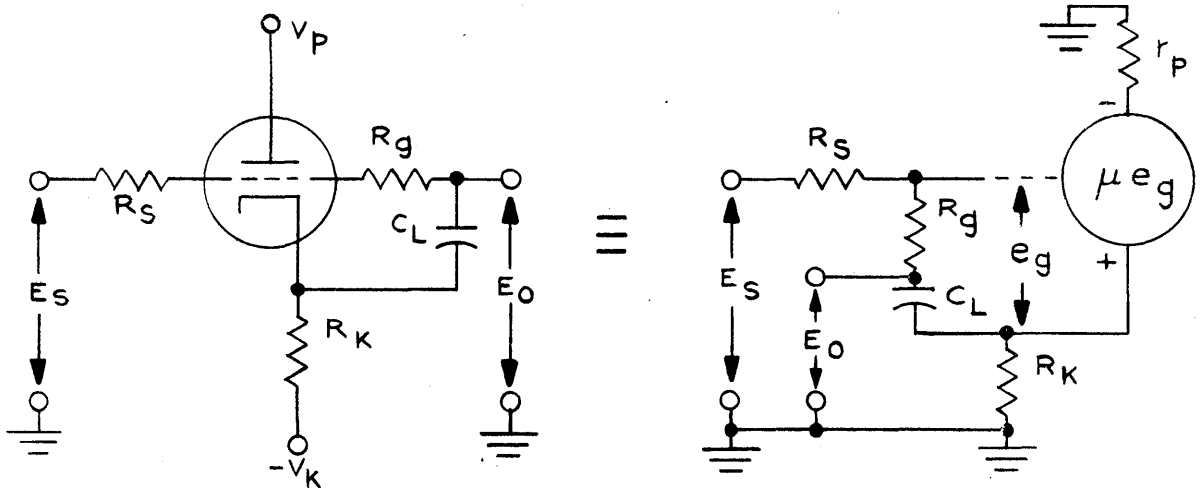
(a) CATHODE FOLLOWER USED FOR TRANSMISSION LINE CHARGING

R_K = CHARACTERISTIC IMPEDANCE OF OUTER SECTION OF TRANSMISSION LINE.

$R_S + R_g >>$ CHARACTERISTIC IMPEDANCE OF INNER SECTION OF TRANSMISSION LINE.

C_L = TOTAL CAPACITANCE OF INNER SECTION OF TRANSMISSION LINE.

ASSUME VACUUM TUBE CAPACITANCES ARE SMALL ENOUGH TO BE NEGLECTED.



(b) EQUIVALENT CIRCUITS

FIG. 26

A METHOD FOR THE RAPID TRANSMISSION OF AN ACCURATE VOLTAGE MAGNITUDE

A-45278

circuit. Appendix C shows that the inclusion of this resistance can actually help to decrease the total time it takes for the output voltage to reach a given accuracy. The results given in the appendix point out, however, that for R_g to be beneficial, it is necessary that A have a value which is greater than the reciprocal of the desired per unit accuracy of the output voltage. In other words, for an output voltage accuracy of 0.1 percent, the value of A must exceed 1,000. For high-accuracy systems then, R_g will normally have a detrimental effect due to the failure of A to attain this requisite large value.

6.24 Conclusions Regarding the Various Transmission Schemes

The preceding paragraphs have presented three possible methods for the transmission of the output voltage of a decoder. All of the methods were introduced, first of all, in order to produce a usable magnitude of output voltage at the receiving end of a transmission line. It was shown that one way of obtaining this output voltage is by using a d-c amplifier at the receiving end which increases the voltage level above that supplied by the decoder and transmission line combination. However, such a scheme is highly susceptible to noise pickup by the transmission line, whereas the accuracy is affected by any drift or non-linearity in the amplifier.

In order to decrease the effect of noise pickup, a transmission method was suggested which uses a cathode-follower at the sending end of the transmission line instead of a d-c amplifier at the receiving end. This method can considerably reduce the problem of noise pickup by the transmission line, but at the sacrifice of a considerable waste of power. It was pointed out, however, that the cathode-follower does not completely remove the problem of non-linearity and drift.

In order to keep the accuracy of the output voltage from the transmission line equal to the accuracy at the output of the decoder, a third transmission scheme was suggested which uses a three-conductor transmission line. In this method, both the noise and the accuracy problems have been greatly improved upon, but at the expense of requiring a special and more complicated form of transmission line.

The choice of any of these transmission schemes will depend upon the accuracy and speed of response which are desired at the receiving end of the transmission line. With each improvement, each of the methods also introduces a further complexity in equipment. In many applications this increased complexity might completely offset the particular advantages which that method offers over the others.

6.3 General Summary

This thesis report has included both a general and a specific discussion of the problems associated with the field of digital-analog conversion equipment. In order to demonstrate how such conversion equipment might be used, and for what reasons, three examples of its use were given. These examples included digital computer control systems, telemetering and servomechanism control systems, and information storage.

A study was then made of the important engineering requirements of digital-analog conversion equipment. The requirements specifically studied were:

1. The general applicability of the input to or output from the conversion device;
2. The accuracy of the conversion;

3. The sensitivity of the conversion;
4. The freedom from drift of the conversion device;
5. The time taken for a single conversion;
6. The amount of equipment necessary for single and multiple conversion channels.

In the discussion of these engineering requirements, examples were given of what had been achieved by previous conversion systems. Two tables were also given which gave a comparison of the various decoding and encoding schemes, along with a comparison of their abilities and limitations.

It was then pointed out that the number of quantizing levels and the conversion time would completely specify the internal operation of digital-analog conversion devices. In this respect, the problem of conversion was shown to be one of comparison or matching of the input and output signals. Three fundamental ways of carrying out this comparison or matching process were given:

1. Serial matching of each quantizing increment;
2. Serial matching of each binary digit;
3. Parallel matching of all digits (simultaneous comparison).

These three types of matching process were shown to be similar to the three ways in which digital information may be transmitted:

1. Transmission in series of all the increments which correspond to the present value of the signal;
2. Transmission in series of each binary digit which corresponds to the present value of the signal;

3. Transmission in parallel of all the digital information corresponding to the present value of the signal.

The characteristics of digital-analog conversion devices were then compared to those of analog systems, where quantization error is similar to noise and conversion time may be compared to the bandwidth of an analog system. In order to match the digital-analog conversion device to the external system, it was pointed out that knowledge must be had of the characteristics of the input signal to the conversion device and also the characteristics of the system following the conversion device. Two examples were given which indicated the extremes which the conversion device might take. In connection with one of these examples, the benefit of clamping the input signal to the conversion device was also demonstrated.

This analysis of digital-analog conversion devices indicated that binary-weighting schemes are one of the better methods for accomplishing both decoding and encoding. Since the binary-weighted decoder occurs as one of the most critical parts of a step-comparison type of encoder, a study of this type of decoder would also encounter a large number of the problems associated with binary-weighted encoders. As a result, an analysis was made of two types of binary-weighted decoding:

1. The use of binary-weighted voltage sources;
2. The use of equal-valued current sources connected to a binary-weighted ladder network.

Study of these two methods indicated that the current source method is superior to the voltage source method. Further study of the current source method showed that it would be possible to include a "holding"

or storage medium with each current source without increasing the number of vacuum tubes needed in such a decoder circuit. Tests were then made on an experimental two digit current source decoder. The result of these tests indicated that such a decoder could be expected to yield an accuracy of 0.1 percent (10 binary digits) without the need of recalibration more often than every few days. The response time of the decoder was found to be around 1.5 microseconds for the accuracy given, while continuous operation at frequencies up to 125 kilocycles was obtained. A method for the inclusion of a simple checking and recalibrating circuit was demonstrated in order to simplify the initial alignment and subsequent recalibration of the decoder.

Two final problems associated with the use of such a decoder were then considered:

1. Use of a binary-weighted decoder for encoding;
2. Transmission of the decoder output voltages.

In connection with the first problem, it was indicated that one of the primary necessities, in addition to an accurate decoder, is an amplitude comparator which will have the requisite sensitivity over a large operating range. It was pointed out that this method of encoding is very useful when multiple input channels are to be considered, since the only duplication necessary is in the amplitude comparators and the gating circuits for the error signals.

Three methods were given for solving the problem of accurately and rapidly transmitting the decoder output voltage:

1. Use of a d-c amplifier at the output of the transmission line;

2. Use of a cathode-follower at the output of the decoder;
3. Use of a three-conductor transmission line and a cathode-follower for charging this line.

These three methods were then evaluated; it was pointed out that the better transmission methods involved a greater complexity of equipment and a large power loss. The choice of a particular method appears to depend upon how much one wishes to pay for accuracy and speed of response.

6.4 Suggestions for Further Study

During the course of this report several of the problems associated with digital-analog conversion have been only touched upon. There were also several instances when it would have been desirable to have carried out experimental work on some of the various suggestions for conversion equipment and the uses of this conversion equipment. The analysis of conversion equipment and the comparison of this conversion equipment to analog systems was only briefly touched. Effort might profitably be directed towards obtaining a simple criterion for the selection of a particular type of conversion equipment. Several of the conversion methods which were presented might also be analyzed more carefully to determine at exactly what points their limitations lie. The use of voltage sources for binary-weighted decoders might be further studied and experimental results obtained for this method. An experimental study of the step-comparison encoding device would be very valuable in helping to determine just what accuracies and response times can be achieved, along with the specifications which must be placed upon the amplitude comparator. Finally, the various methods for transmitting the output voltage of a high speed conversion device might be studied experimentally in order to determine how well each of them would operate in any actual system.

APPENDIX A

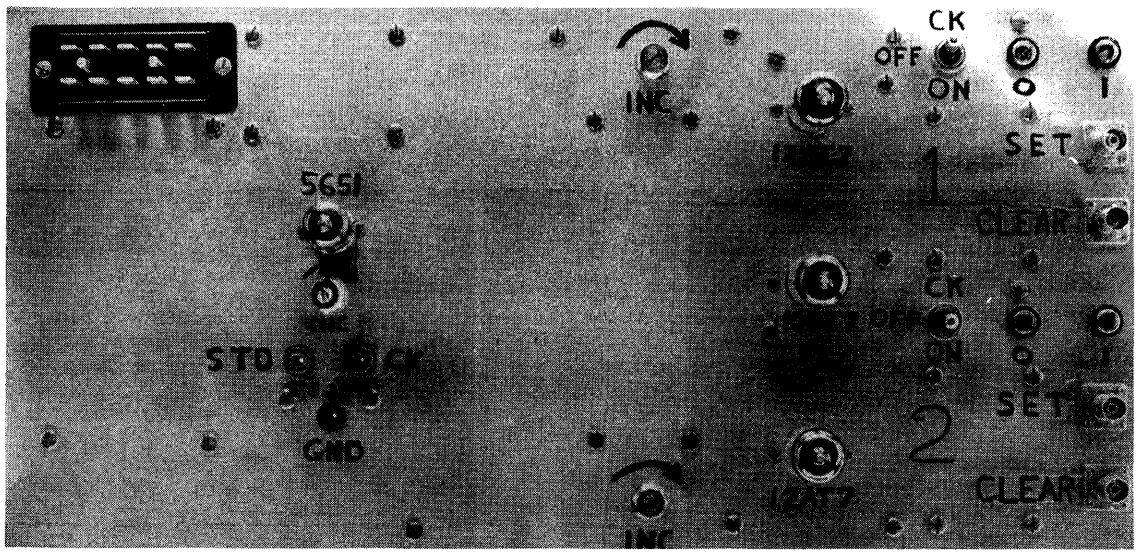
PHOTOGRAPHS AND CIRCUIT DIAGRAMS

OF

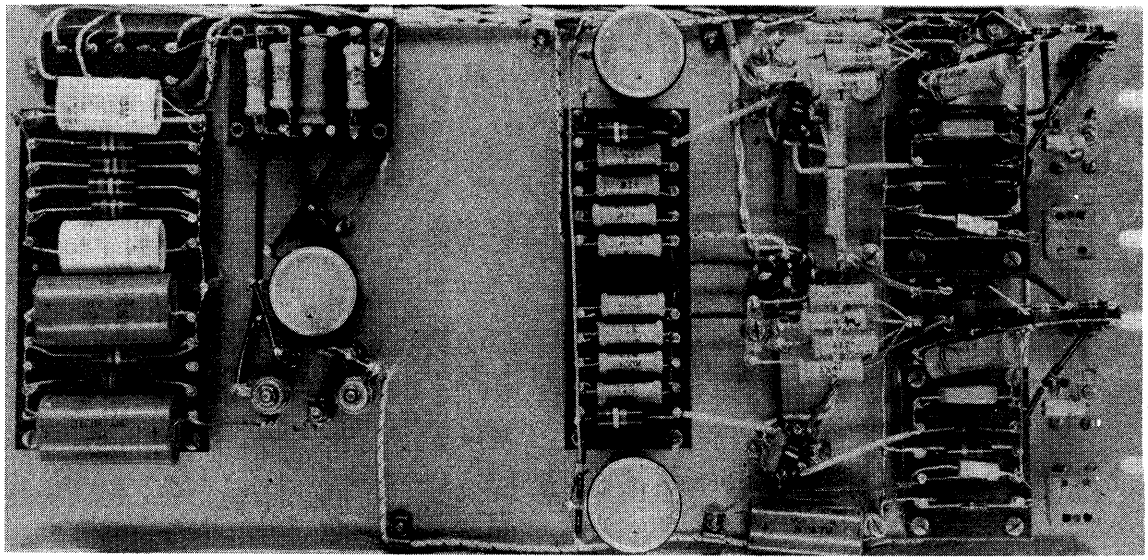
EXPERIMENTAL TWO-DIGIT DECODER

AND

ASSOCIATED POWER-SUPPLY REGULATOR



FRONT VIEW



REAR VIEW

FIG. 27

EXPERIMENTAL TWO-DIGIT DECODER

A-45287
F-1339

B-45270

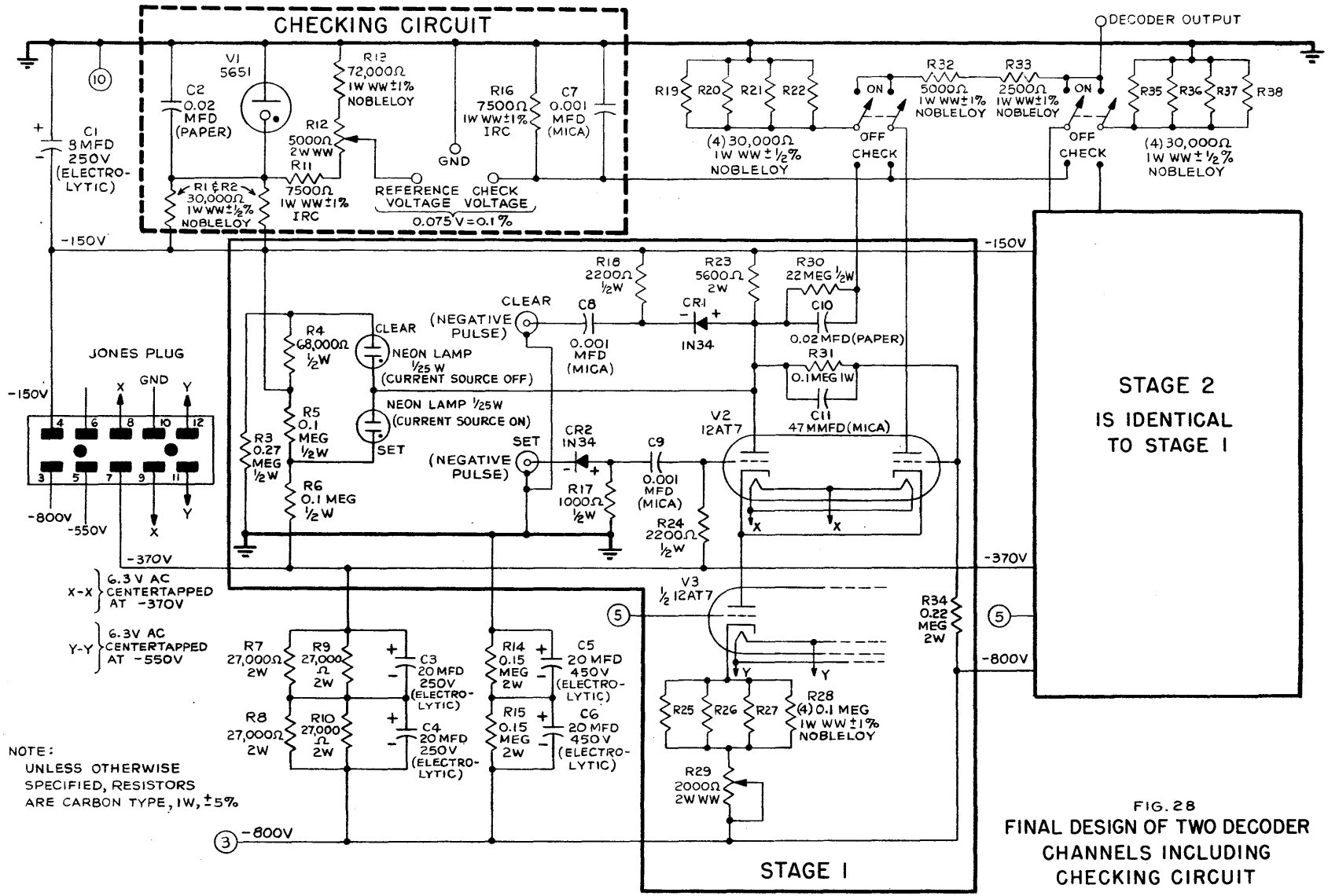
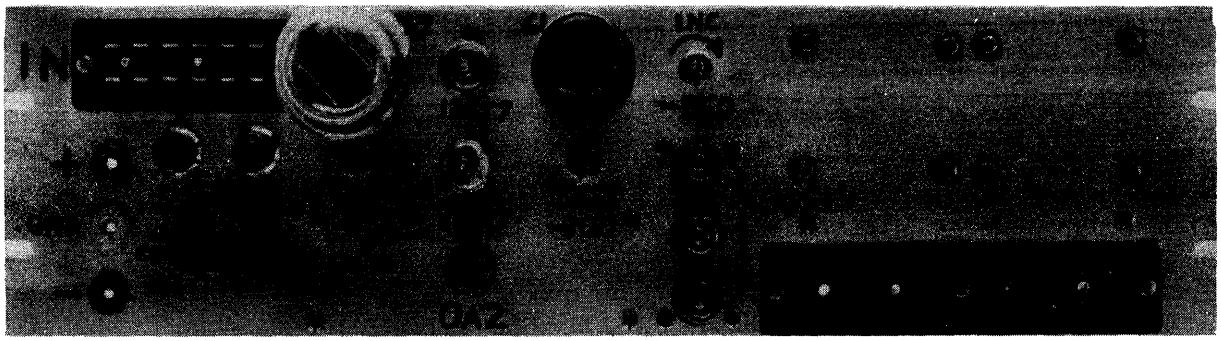
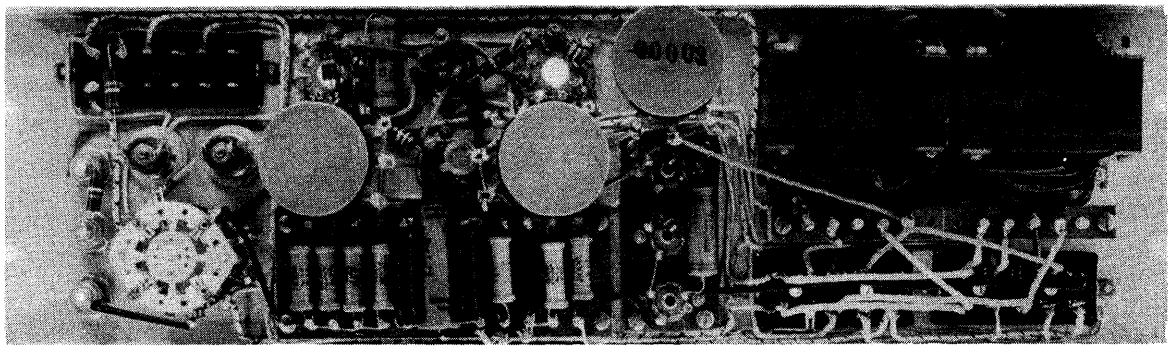


FIG. 28
FINAL DESIGN OF TWO DECODER CHANNELS INCLUDING CHECKING CIRCUIT



FRONT VIEW



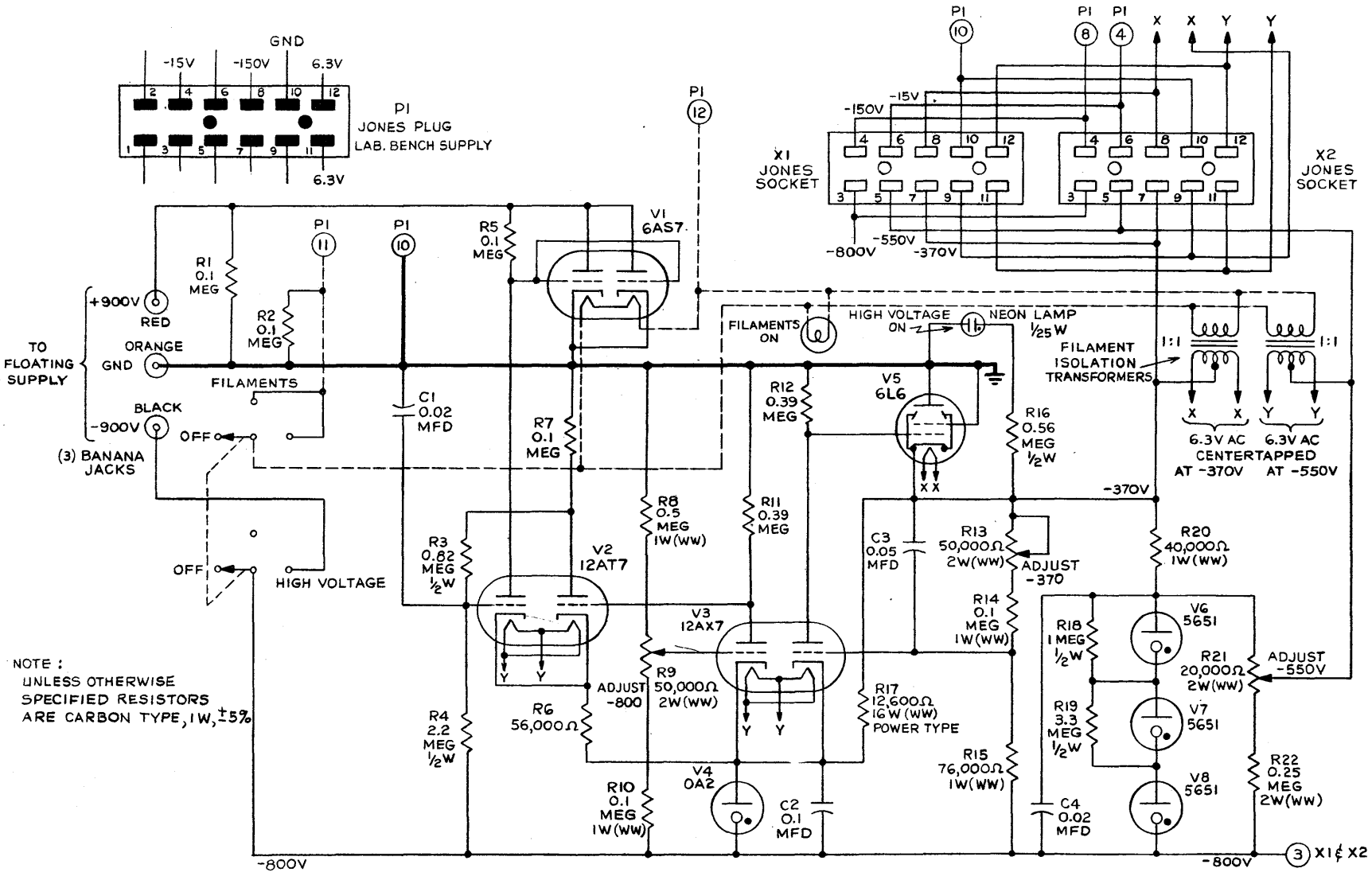
REAR VIEW

A-45286
F 1340

FIG. 29

POWER SUPPLY REGULATOR FOR DECODER

B-45264



NOTE :
UNLESS OTHERWISE
SPECIFIED RESISTORS
ARE CARBON TYPE, 1W, ±5%

FIG. 30
POWER SUPPLY REGULATOR
FOR DECODER

APPENDIX B

CHARACTERISTICS OF
DECODER VACUUM TUBES AND
"NOBLELOY" RESISTORS

5651

VOLTAGE-REFERENCE TUBE°

Miniature Glow-Discharge Type

Maximum Ratings (Absolute Values):

DC Operating Current (Continuous)	3.5 Max.	ma
Ambient Temperature Range	-55 to +90	°C

Characteristics and Operation Range Values:

	Min.	AV.	Max.	
DC Starting Voltage	---	107	115*	volts
DC Operating Voltage	82	87	92	volts
DC Operating Current	1.5	---	3.5	ma
Regulation (1.5 ma to 3.5 ma)	---	---	3	volts
Stability**	---	---	0.1	volt

Circuit Values:

Shunt Capacitor	---	---	0.02 ...	µf
Series Resistor	See NOTE Below			

° Data obtained from reference No. 16.

* A supply voltage of not less than this value should be provided to insure "starting" throughout tube life.

** Defined as the maximum voltage fluctuation at any current level within the operating current range.

NOTE: A series resistor must always be used with the 5651. The resistance value must be chosen so that (1) the maximum current rating of 3.5 ma is not exceeded at the highest anode-supply voltage employed, and (2) the minimum current rating of 1.5 ma is always exceeded when the anode-supply voltage is at its lowest value.

12AT7

HIGH-MU TWIN TRIODE°

9-Pin Miniature, Grounded Grid Type

ELECTRICAL DATA

Heater, for Unipotential Cathodes:

Heater Arrangement	Series	Parallel	
Voltage	12.6	6.3	ac/dc volts
Current	0.15	0.3	..... amp.

Direct Interelectrode Capacitances (Approx.)*:

	Unit No. 1	Unit No. 2	
Grounded-Cathode Operation:			
Grid to Plate	1.45	1.45	μμf
Grid to Cathode	2.5	2.5	μμf
Plate to Cathode	0.45	0.35	μμf
Heater to Cathode	2.5	2.5	μμf
Grounded-Grid Operation:			
Plate to Cathode	0.15	0.15	μμf
Grid & Heater to Cathode	5	5	μμf
Grid & Heater to Plate	1.6	1.5	μμf
Grid to Grid	0.005 max.		μμf
Plate to Plate	0.4 max.		μμf

° Data obtained from reference No. 16.

* with no external shield.

12AT7

(continued)

Maximum Ratings, Design-Center Values:
Values are for each unit

Plate Voltage	300	max.	volts
Plate Dissipation	2.5	max.	watts
Peak Heater-Cathode Voltage:			
Heater negative with respect to cathode	90	max.	volts
Heater positive with respect to cathode	90	max.	volts

Characteristics:

Plate Voltage	100	180	250	volts
Grid Voltage	-1	-1	-2	volts
Amplification Factor	54	62	55	
Transconductance	4000	6600	5500	µmhos
Grid Voltage (Approx.) for plate current of 10 µamp.	-6	-8	-12	volts
Plate Current	3.7	11	10	ma

CHARACTERISTICS OF "NOBLELOY" PRECISION RESISTORS

Voltage Characteristics:

Voltage coefficient does not exceed 1/10 of 1%.

Normal Load Life Characteristics:

The permanent change in resistance will not be more than 1.0% when the resistor is subjected to a normal life test of 1000 hours.

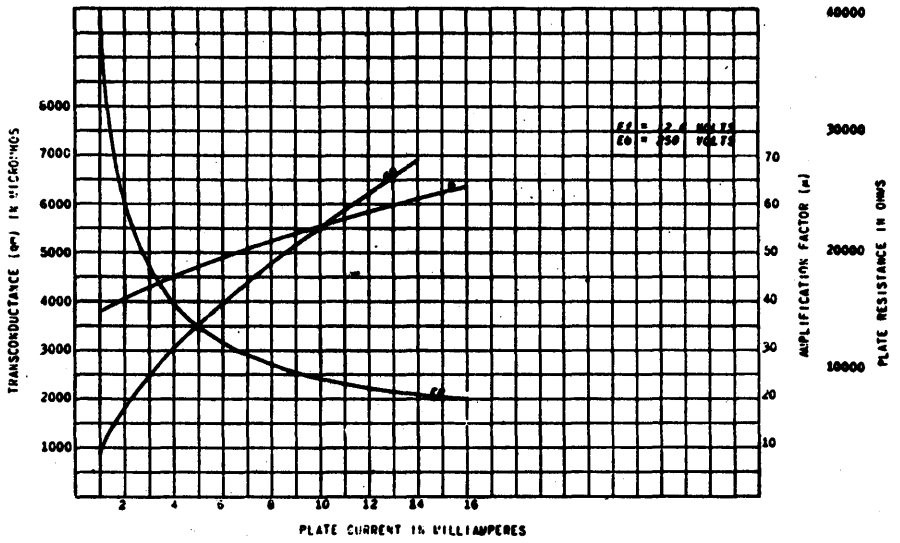
Noise Characteristics:

When tested for noise according to standard R.M.A. procedure, the inherent noise level will not exceed 1/4 microvolt per volt, irrespective of the resistance value.

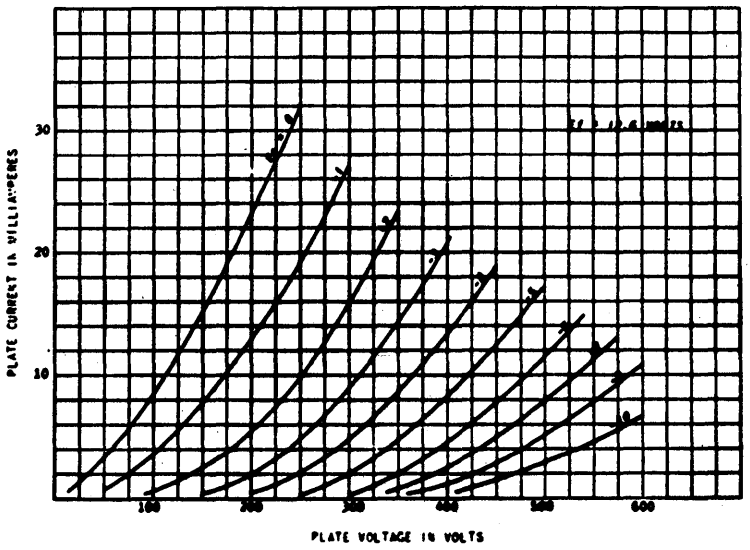
Tolerances and Temperature Coefficients:

Tolerances of 1% and 5% are available, for which the temperature coefficient will not exceed 0.0005 (0.05% per degree Centigrade) negative. Ultra-precision "Nobleloy" resistors with tolerances of 0.5% are available, for which the temperature coefficient is 0.02% per degree Centigrade, positive.

AVERAGE CHARACTERISTICS



AVERAGE PLATE CHARACTERISTICS



12AT7

FIG. 31

A-40481

APPENDIX C

Derivation of Equations for Cathode Follower Charging of Three Concentric-Conductor Transmission Line

Section 6.2 of this report describes a method for the rapid transmission of an accurate voltage magnitude by means of a cathode follower and a three concentric-conductor transmission line (see Figure 26). The following assumptions are made as to the manner in which the transmission line functions:[13]

1. The cathode follower resistance R_K is equal to the characteristic impedance of the outer section of the transmission line. This outer section thus appears to the remainder of the circuit as a constant resistance R_K.
2. The sum of the grid circuit resistances is so much greater than the characteristic impedance of the inner section of the transmission line that this section may be approximated by replacing it with a capacitance C_L, where C_L equals the total capacitance of the inner section of the transmission line.

With these assumptions, it is possible to arrive at the equivalent circuits of Figure 26-b. It is possible to further simplify the circuit by combining the R_K and r_p resistances, yielding the following:

$$R_{eq} = \frac{r_p R_K}{r_p + R_K} \tag{1}$$

$$E_{eq} = \frac{\mu e_g R_K}{r_p + R_K} = \frac{\mu e_g R_{eq}}{r_p} \tag{2}$$

Assuming that the output circuit at E_o has an infinite impedance, the following relationship holds between E_s and I_s:

$$E_s = I_s(R_s + R_g + R_{eq}) + \frac{1}{C_L} \int I_s dt + E_{eq} \tag{3}$$

Replacing E_{eq} by the relationship of equation (2), and substituting the equivalent value for e_g into equation (2), we obtain:

$$E_s = I_s(R_s + R_g + R_{eq}) + \frac{1}{C_L} \int I_s dt + \frac{\mu R_{eq}}{r_p} \left[I_s R_g + \frac{1}{C_L} \int I_s dt \right] \tag{4}$$

If we now combine the terms in I_s and $\int I_s dt$, there results:

$$E_s = I_s(R_s + R_g + R_{eq} + \frac{\mu R_{eq} R_g}{r_p}) + \frac{1}{C_L} (1 + \frac{\mu R_{eq}}{r_p}) \int I_s dt \tag{5}$$

It is possible to simplify the above expression by making the following substitutions and assumptions:

1. $R_s \gg R_{eq}$ (this is the normal condition) (6)
2. $A = 1 + \frac{\mu R_{eq}}{r_p}$ (7)
3. $R_{tot} = R_s + AR_g$ (8)
4. $C_{tot} = \frac{C_L}{A}$ (9)

Equation (5) then becomes:

$$E_s = I_s R_{tot} + \frac{1}{C_{tot}} \int I_s dt \qquad (10)$$

Equation (10) is merely a simple series RC circuit, whose current is given by:

$$I_s = \frac{E_s}{R_{tot}} \varepsilon^{-\frac{t}{R_{tot}C_{tot}}} \qquad (11)$$

It is well to stop at this point and consider what effect the introduction of a cathode follower has had upon the circuit operation. If R_g has a value of zero (i.e., a short circuit), the only effect of the cathode follower is to decrease the effective capacitance of the transmission line, and hence to decrease the time constant of the circuit which is seen by the source E_s. However, if R_g is made very large with respect to R_s, the time constant of the circuit is not changed since R_{tot} increases by the same proportion that C_{tot} decreases. Therefore, the only result is a greatly decreased initial value for I_s.

Knowing the value of I_s, we can obtain E_o by means of the following equation:

$$E_o = E_s - I_s(R_s + R_g) = E_s \left[1 - \frac{R_s + R_g}{R_{tot}} \varepsilon^{-\frac{t}{R_{tot}C_{tot}}}\right] \qquad (12)$$

In order to more readily determine the effect of R_g on the buildup of the output voltage E_o, it is desirable to make the additional substitutions:

5. $T = R_s C_L$ (13)

6. $K = \frac{R_g}{R_s}$ (14)

Equation 12 may then be written in the more useful form:

$$E_c = E_s \left(1 - \frac{1 + K}{1 + AK} \varepsilon^{-\frac{A}{T(1+AK)}t}\right) \tag{15}$$

where the quantities T, A, and K have been defined above. If we allow R_g, and hence K, to be zero, we obtain the following:

$$E_c = E_s \left(1 - \varepsilon^{-\frac{A}{T}t}\right) \tag{16}$$

Since the exponential terms in equations 15 and 16 are the ones which introduce the error in E_c, it is obvious that for R_g to have a <u>beneficial</u> effect we must have:

$$\varepsilon^{-\frac{A}{T}t} \geq \frac{1+K}{1+AK} \varepsilon^{-\frac{A}{T(1+AK)}t} \tag{17}$$

for a given value of t.

This leads to the result that:

$$\frac{1+K}{1+AK} \leq \varepsilon^{-\left(1 - \frac{1}{1+AK}\right)\frac{A}{T}t} \tag{18}$$

Writing this in a more useful form, we obtain:

$$\frac{1+K}{1+AK} \leq \left[\varepsilon^{-\frac{A}{T}t}\right]^{\frac{AK}{1+AK}} \tag{19}$$

The expression in brackets is merely the per unit error between E_c and E_s at a particular time t, for the case of $R_g = 0$. By taking the base-ten logarithm of both sides of equation 19, and by making the following substitution:

$$\%\ E_{pu} = \varepsilon^{-\frac{A}{T}t} \tag{20}$$

we finally obtain:

$$\log \frac{1}{E_{pu}} \leq \left(1 + \frac{1}{AK}\right) \log \frac{1+AK}{1+K} \qquad (21)$$

This equation thus requires that $K = \frac{R_g}{R_s}$ take on certain values, depending upon the values of E_{pu} and A, in order that R_g will function such as to shorten the time it takes for $\dot{E}_o$ to reach a given accuracy. The values for which R_g just begins to have a beneficial effect upon the response time of the circuit are obtained when the equality sign holds for equation 21. The following tabulation is given for this case.

Tabulation of Equation 21 for Various Values of E_{pu}, A, and K

AK	$E_{pu} = \frac{1}{10}$		$E_{pu} = \frac{1}{100}$		$E_{pu} = \frac{1}{1000}$	
	K	A	K	A	K	A
10	0.36	27.8	----	----	----	----
100	9.6	10.4	0.057	1,750	----	----
1,000	99.3	10.1	9.05	111	0.008	125,000
10,000	999	10	99.1	101	9.01	1,110
100,000	9,999	10	999	100	99	1,010

APPENDIX D

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