SUPPORT CIRCUITS, FASTER 8080A’S ADDED

Less than one year ago we entered the 8080A marketplace with our INS8080A — a pin-for-pin, function-for-function replacement for you-know-who’s MPU. But that was only the start. Since then we’ve added two more versions of that microprocessor, as well as a complete family of support circuits.

The new versions of our original 2-μs cycle time INS8080A are the INS8080A-1, which has a 1.3-μs cycle time, and the INS8080A-2, with a 1.5-μs cycle time.

In addition to the faster 8080A’s, we now offer ten types of interface circuits to support 8080A system design.

- DP 8212 is a 8-bit I/O port that you can use to implement all major peripheral and MPU I/O system functions.
- INS8255 is a programmable peripheral I/O interface that features direct bit set/reset capability.
- DP8301 is a microprocessor interface latch element (MILE) with on-chip status flags for ‘handshake’ control and interrupt generation. It drives TTL, NMOS, PMOS, and CMOS circuitry.
- DP8224 is a crystal-controlled clock generator and driver, which also provides a status strobe and oscillator outputs for external circuits.
- DP8228/8238 are system controller and bus driver circuits that generate all needed read/write control signals, provide drive and isolation for the 8080A’s bidirectional data bus, and a user-selected single-level interrupt vector.
- DP8304 is an 8-bit bidirectional bus transceiver with high active outputs to both ports, a Tri-State chip enable control, and transmit/receive control.
- INS8251 is a universal communications interface (USART) for data communication in 8080A and other bus-structured systems.
- DP8216/8226 are I/O buffer drivers (4-bit parallel transceivers) suited to both 8080A and general MPU applications.

Line-By-Line Resident Assembler For “SC/MP” MPU Enhances Development System

National is now offering a line-by-line resident assembler firmware kit, designed for use with its SC/MP LCDS (Low Cost Development System). Known as SUPAK, the $300 assembler is contained in eight PROM/ROM devices that can be plugged into a blank ROM/PROM card (ISP-8B/004B) which is available from National. The entire assembled card is then inserted into the LCDS/teletype system.

SUPAK is the only firmware kit of its kind. It greatly enhances the flexibility and capability of the SC/MP LCDS, making it both the most inexpensive and effective SC/MP development tool. SUPAK is a 4K byte package that consists of three programs: a line-by-line assembler, a paper tape line editor and a PROM tape punch program.

The line-by-line assembler accepts a program in limited assembly language from a keyboard or paper reader, and then assembles it directly into RAM.

The paper tape line editor, which allows insertion, deletion or replacement of lines of program source code, punches either leader or trailer.

The PROM tape punch program punches the contents of a specified memory range, in BPNF or complemented binary format, onto paper tape. This tape could be used to program memories using a standard, commercially available PROM programmer such as the DATA I/O.

SUPAK requires the LCDS firmware, but will run on either a SC/MP or a SC/MP II (n-channel) LCDS. It comes as a set of eight MM5204/MM5214 ROM IC’s, designated ISP-8F/111.
NEW LIBRARY PROGRAM

SC/MP Program SL0047A-PLOT
(from Jermy MicroComputer Center, Kent, England)
Program Listing — see page 3
Source paper tape — $5.00 each

A sample plot of a SINE wave drawn on a Teletype by the PLOT routine is shown below.

GRAPH PLOTTING FROM RAM A JERMYN UTILITY PROGRAM

Programming Tidbit

When using the PACE or IMP-16 you may use a version of the following assembly instruction to load an ASCII character into one of the Accumulators

LI 0, '9'/256

an ASCII instruction will result in object code that will result in an ASCII 9 or X'39 to be loaded left justified in AC0 when executed.

SM/PL TIMER PROGRAM

(by Bob Edwards
LECO Corporation
(616) 983-5531)

This is a SM/PL program that works with a 1200 baud CRT. This program prints the time from 0 to 99 hrs 59 mins and 59 secs. It was developed using an IMP-16P with 16K and the IMP-16 Disc system.

SM/PL-A High Level Language For IMP-16

A few words on the SM/PL Compiler for IMP-16 . . .

• SM/PL (Smart or Simple Programming Language) is a high level language compiler for the IMP-16 only.
• To compile a SM/PL program and accommodate the compiler 16K of R/W memory is necessary.
• It is not a supported product and is only available through the Microprocessor Users Group at a cost of $100.00.
• The $100.00 price tag includes the source listing, SM/PL Programming Manual and the object (machine language) tape.
• Ordering SM/PL is done by sending a check or Purchase Order to Compute/208, National Semiconductor, 2900 Semiconductor Dr, Santa Clara, Ca. 95051 (see the library order form on page 15).
• The August 1976 issue of the COMPUTE (Vol. 2 #8) newsletter contains a description of the language features.
THIS PROGRAM FETCHES DATA STORED IN RAM AND DISPLAYS THE CONTENT IN GRAPHICAL FORM ON THE TELETYPE CONSOLE.

AFTER LOADING SET THE TARGET PROGRAM COUNT TO HEX 0001 (INITIALIZE) AND THEN RUN.

THIS PROGRAM WILL RUN WITHIN AN L.C.D.S.

DATA FOR PLOTTING IS FETCHED FROM LOCATION MDATA UPWARDS AND LOOPS AROUND AT LOCATION DATEND.

0001 P1 = 1
0002 P2 = 2
0003 P3 = 3
007D VECTOR = X'07FD'
0107 COUNT = X'0107'
0000 ZERO = X'0000'
0004 EOT = X'004'
004C STACK = X'04C'
7AEC PUTC = X'7AEC'
000D CR = X'00D'
000A LF = X'00A'
0008 BS = X'008'

FFFF MINONE = -1
FFFF6 MINTEN = -10
FFFFF MINUS = -15
0020 SP = X'20'
0007 BEL = X'07'
003F RSTCYL = X'03F'

0000 X'0000'
0001 C4FC BEGIN LDI (LAST)
0003 32 XPAL P2
0004 C407 LDI (LAST)
0006 36 XPAH P2
0007 C4FD LDI (VECTOR)
0009 31 XPAL P1
000A C407 LDI (VECTOR)
000C 35 XPAH P1
000D C402 LDI (MDATA)
000F 30 ST P1(F1)
0011 C42F LDI (MDATA)
0013 C900 ST P1(F1)
0015 C454 LDI (MIMAX)
0017 31 XPAH P1
0018 C401 LDI (MIMAX)
001A 35 XPAH P1
001B C400 JS P3.Print
001D 27C4
001F D333
0021 3F
0022 C400 LDI (MCRFL)
0024 31 XPAL P1
0025 C401 LDI (MCRFL)
0027 35 XPAH P1
0028 C400 JS P3.Print
002A 37C4
002C D333
002E 3F
002F C4FF CLEAR: LDI (LINCT)
0031 31 XPAL P1
0032 C407 LDI (INCT)
0034 35 XPAH P1
0035 C400 LDI ZERO
0037 C900 ST P1(F1)
0039 C400 LDI (MCRUSR)
003B 31 XPAH P1
003C C400 LDI (IMAXV)
003E 35 XPAH P1
003F 9033 JMP PRJNCY
0041 C4EC NOSAX: XNZ CLEAR
0043 C401 LDI (MIMAX)
0045 35 XPAH P1
0046 C491 LDI (MIMAX)
0048 31 XPAH P1
0049 9029 JMP PRJNCY
004B C407 OVER: LDI (LOVER)
004D 31 XPAH P1
004E C401 LDI (HMOVE)
0050 35 XPAH P1
0051 9006 JMP PRJRE
0053 C403 POINT: LDI (HPOINT)
0055 31 XPAH P1
0056 C401 LDI (HPOINT)
0058 35 XPAH P1
0059 C400 PIRET: JS P3.Print
005B 37C4
005D D333
005F 3F
0060 C4FF RETURN: LDI (HRETURN)
0062 35 XPAH P1
0063 C4FF LDI (LTECT)
0065 31 XPAL P1
0066 9000 ILD P1(F1)
0068 C900 ST P1(F1)
006A 9045 JP MINTEN
006C 9042 JP (MIMAX)
006E 35 XPAH P1
0070 35 XPAH P1
0071 C424 LDI (MIMAX)

97 0073 31 XPAL P1
98 0074 C400 PRICYC: JS P3.Print
99 0076 27C4
0078 D333
007A 3F
100 007D 31 XPAL P1
101 007E C407 LDI (HVECTOR)
102 0080 35 XPAH P1
103 0081 C501 LD @P1(F1)
104 0083 01 XAE
105 0084 C100 LD (P1)
106 0086 31 XPAL P1
107 0087 40 LDE
108 0088 35 XPAH P1
109 0089 40 LDE
110 008A 9042 XRI (DATEND)
111 008B 904F NZU FETCH
112 008E 31 XPAL P1
113 008F 01 XAE
114 0090 40 LDE
115 0091 31 XPAL P1
116 0092 40 LDE
117 0093 904F NZU FETCH
118 0095 C402 LDI (MDATA)
120 0099 35 XPAH P1
121 009A C42F LDI (HDATA)
122 009C 31 XPAL P1
123 009D C501 FETCH: LD @P1(F1): DATA FETCH
124 009F C6FF ST @P1(F2): AND TEST
125 00A1 C4FD LDI (HVECTOR): ROUTINE
126 00A3 31 XPAL P1
127 00A4 01 XAE
128 00A5 C407 LDI (HVECTOR)
129 00A7 35 XPAH P1
130 00A8 C501 ST @P1(F1)
131 00AA 01 XAE
132 00AB C900 ST (P1)
133 00AD C601 LD @P1(F2)
134 00AF 9042 JZ POINT
135 00B1 01 XAE
136 00B2 06 FSA
137 00B3 9D3F ANI RSTCYL
138 00B5 07 CAS
139 00B6 40 LDE
140 00B7 80F8 ADI MINS
141 00B9 9940 JMP
142 00BB C4FE SPACE: LDI (MSPACE)
143 00BD 31 XPAL P1
144 00BE C400 LDI (HMSPACE)
145 00C0 35 XPAH P1
146 00C1 C400 JS P3.Print
147 00C2 37C4
148 00C5 D333
149 00C7 3F
14C9 C401 LDI (MCRFL)
150 00C9 3D3F ANI RSTCYL
151 00C9 07 CAS
152 00CC 40 LDE
153 00CD 01 XAE; DATA TO EXT
154 00D2 90E7 JMP SPACE
155
156 00D4 01 PRINT: XAE MESSAGE PRINT
157 00D5 C6FF ST @P2(F2): ROUTINE INDEXED
158 00D7 06 CAS
159 00D8 C6E8 ST @P2(F2)
160 00DA 37 XPAH P3
161 00DB C6E8 ST @P2(F2)
162 00DD 35 XPAH P3
163 00DE C6E8 ST @P2(F2)
164 00E0 C501 OBTAIN: LD @P1(F1)
165 00E2 01 XAE
166 00E3 C404 LDI EOT
167 00E5 60 XRE
168 00E6 9099 JZ EXIT
169 00E7 9081 XAE
170 00EA C47A LDI (HPRINT): TO OUTPUT
171 00EC 37 XPAH P3 CHARACTER
172 00ED 40 LDE
173 00EE 3F XPPC P3
174 00F0 904F JMP OBTAIN
175 00F1 C601 EXIT: LD @P2(F2)
176 00F3 33 XPAH P3
177 00F4 C601 LD @P2(F1)
178 00F6 37 XPAH P3
179 00F7 C601 LD @P1(F1)
180 00F9 07 XAE
181 00FA C501 LD @P2(F1)
182 00FB C501 LD @P1(F1)
183 00FC 01 XAE
184 00FD 3F XPPC P3
185 00FE 20 MSPACE: BYTE SP.EOT
186 00F0 04 BYTE
187 0100 0A NCRLF: BYTE LCR.EOT
188 0101 0D
189 0102 04 MAP: ASCII 'N' FOR OPTIONS
189 0104 0A BYTE LCR.EOT
190 0105 0D
190 0107 22 MOVE ASCII '-----------'
A new booklet describing electronic components designed for use in citizen's band radio manufacture is now available from National.

The products described in the booklet include synthesizer systems, 5-pin audio amplifiers, microprocessor controlled tuning systems, linear IC's, light emitting diodes (LED's), clock modules, RF output discretes, and regulators.

Titled National Semiconductor Personal Communications: CB Radio, the booklet is available without charge from National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051.

How To Build
A Digital Thermometer

Analog electronic thermometers have been available for some time, but they are generally difficult to read and, besides, are relatively fragile. Digital thermometers, on the other hand, are both easy to read and rugged.

Besides a +5 V input, the ADD2500 draws 18 mA from a negative supply. This comes from the dc/dc converter (at −15 V) as a regulated current via the 2N5457 FET, the LED, and the 2N3904. The negative supply of the ADD2500 is internally Zener regulated; it, together with the two diodes and the resistor string between ground and $I_{EE}$, establish a low-drift offset voltage for the LM134's sense resistor.

The finished thermometer requires only a single, unregulated +12 V supply, and operates from −29°C to +60°C (−20°F to +140°F).

The digital thermometer described here uses an ADD2500 2½-digit DPM chip for A/D conversion and display decoding. The LM134 programmable current source operates here as the temperature sensor, and the LM555 timer as a dc/dc converter. The DS8866 and the npn transistors drive the NSB3882 display.

The LM134 makes an excellent temperature sensor; it has a constant temperature coefficient of +0.30%/°C (0.167%/°F); and its noise immunity and current programmability make it ideal for remote sensing use. Output-current flow through a sense resistor scales the LM134's output voltage—in this case, to 10 mV/°F, which is one count of the DPM or 1°F displayed.
Tough mathematical tasks are child's play for Number Cruncher

New special-purpose microprocessor combines best features of general-purpose and calculator chips

by Alan J. Weissberger and Ted Toal, National Semiconductor Corp., Santa Clara, Calif.
Reprinted from Electronics, February 17, 1977; Copyright © McGraw-Hill, Inc., 1977

There is one hurdle that the general-purpose microprocessor clears awkwardly: complex mathematical computations. For such applications, designers have had to spend considerable time learning to use efficiently the chosen device's instruction set and unique input/output transfer characteristics. Then they have had to sweat out the development of complex software to perform the desired mathematical operations or algorithms.

A few, hardy designers have put up with these chores in order to gain the benefits of large-scale-integrated technology, but even they would prefer a special-purpose microprocessor designed specifically for complex calculations. A new microprocessor, the 57109 or Number Crunching Unit, does this.

The NCU, presently being built with p-channel metal-oxide-semiconductor technology, can serve in machine process controllers, navigation systems, and measurement and test equipment. It can also extend a mini- or microcomputer's processing power when connected as a peripheral device on the host processor's bus.

In such processing applications, software development time can drop significantly with the NCU. Its instruction set is like those of scientific calculators, which means that the Number Cruncher already has most of the required calculation software. Trigonometric, logarithmic, and exponential functions, for example, are performed directly.

Data formats at the input or the output may be in floating-point or scientific notation. Digit lengths may range up to an eight-digit mantissa, with one or two digits for the exponent.

The 57109 combines the best features of calculator

---

1. Digit handler. Major functional blocks of the Number Cruncher are the control-logic and arithmetic units and the program-storage ROM, which holds about 1,500 8-bit microinstruction words. The device handles 4-bit binary-coded-decimal digits directly. They enter the control-logic block through the 1, 4, lines, and the results go out through the digit-data-out block. The digit-address-counter block sequences each digit during input/output operations. Programmed instructions, 6 bits long, enter through the 1, 6 lines and are converted to sequences of microinstructions.

---

At Weissberger is now with Signetics Corp., Sunnyvale, Calif.
chips and general-purpose microprocessors (Table 1). For example, its I/O functions are more flexible than those of the calculator, which is limited to inputs from a keyboard and outputs to a display. But it is more directly useful for calculations than microprocessors. The NCU can accept a sequence of binary-coded-decimal digits with a single input instruction, an asynchronous digit input, or single-bit inputs for control purposes. In contrast, microprocessors work only on data bytes.

Unlike calculators, the Number Cruncher is controlled by a program stored in an external read-only memory and can perform conditional and unconditional program branches. As in processors, a HOLD input allows handling asynchronous instructions and single stepping, while test and branch instructions facilitate decision-making within programs.

The NCU's major functional blocks (Fig. 1) are the control-logic and arithmetic units and the program-storage ROM, which holds about 1,500 8-bit microinstruction words. Programmed instructions, 6 bits long, enter through the I₁₄ lines and are converted to sequences of microinstructions. Binary-coded-decimal 4-bit data words enter the control-logic block through the I₁₄ lines.

Output data passes through the digit-data-out block, while the digit-address-counter block sequences each digit during I/O operations. Logic levels are compatible with low-power logic families, and the device has on-chip generation of input/output strobes and timing signals.

Examples of the 6-bit operation codes are given in Table 2. (If 8-bit instruction memories are used, external hardware can use the additional 2 bits for device addresses.) Instruction executions vary in time from 1 to 500 milliseconds, although most require 5 to 10 ms. Although these speeds may seem rather slow, they compare favorably with similar functions implemented as subroutines in low-cost microprocessors.

Conditional-test-and-skip/branch instructions permit decision making within the user's program. The conditional-test instructions operate on the results of computations or from an external jump-condition sense input on line I₄. The two flag outputs (F₁ and F₂) may be used to activate external devices. A four-register stack (X, Y, Z, T) holds operands and temporary results, and a

![Table 1](image)

**Table 1. Comparison of Large Scale Integrated**

**PROCESSING CHIPS**

<table>
<thead>
<tr>
<th>Function</th>
<th>Calculator</th>
<th>Number Cruncher</th>
<th>Microprocessor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input/output</td>
<td>keyboard and display</td>
<td>multidigit,</td>
<td>data bytes,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>asynchronous,</td>
<td>single bit</td>
</tr>
<tr>
<td>Data format</td>
<td>floating point or scientific notation</td>
<td>floating-point</td>
<td>binary</td>
</tr>
<tr>
<td></td>
<td></td>
<td>scientific</td>
<td>notation</td>
</tr>
<tr>
<td>Data length</td>
<td>fixed</td>
<td>variable (1 to 8</td>
<td>fixed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>digits for mantissa)</td>
<td></td>
</tr>
<tr>
<td>Program</td>
<td>key sequence</td>
<td>external ROM/program</td>
<td>external ROM,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>counter, microprocessor,</td>
<td>internal PC</td>
</tr>
<tr>
<td>Speed (math or I/O operations)</td>
<td>14 - 400 ms</td>
<td>0.5 - 400 ms</td>
<td>0.5 - 500 ms</td>
</tr>
<tr>
<td>Minimum number of chips for CPU and RAM</td>
<td>1 - 3</td>
<td>(external PC)</td>
<td>2 - 6</td>
</tr>
</tbody>
</table>

![Table 2](image)

**Table 2. NCU Instruction Classes**

<table>
<thead>
<tr>
<th>Digit entry:</th>
<th>0 - 9</th>
<th>Each digit is entered into the X register mantissa or exponent if in enter-exponent mode.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EE</td>
<td>Fixes decimal point of mantissa or number being entered.</td>
</tr>
<tr>
<td></td>
<td>CS</td>
<td>Set enter exponent mode.</td>
</tr>
<tr>
<td></td>
<td>PI</td>
<td>Change sign of mantissa or exponent.</td>
</tr>
<tr>
<td></td>
<td>EN</td>
<td>Number entry terminated and stack is pushed.</td>
</tr>
<tr>
<td>Move:</td>
<td>Roll</td>
<td>Roll stack. X = T + Z = Y = X</td>
</tr>
<tr>
<td></td>
<td>POP</td>
<td>Pop stack. X = Y + Z = T = 0</td>
</tr>
<tr>
<td></td>
<td>XEV</td>
<td>Exchange X with Y. X = Y</td>
</tr>
<tr>
<td></td>
<td>XEM</td>
<td>Exchange X with memory. X = X</td>
</tr>
<tr>
<td></td>
<td>MS</td>
<td>Memory store. X = M</td>
</tr>
<tr>
<td></td>
<td>MR</td>
<td>Memory recall. X = M</td>
</tr>
<tr>
<td>Math:</td>
<td>X + Y</td>
<td>Result in X, stack popped.</td>
</tr>
<tr>
<td></td>
<td>X - Y</td>
<td>Y = Z + T = 0</td>
</tr>
<tr>
<td></td>
<td>X = Y</td>
<td>Result in memory.</td>
</tr>
<tr>
<td></td>
<td>M + X</td>
<td>Result in X, previous X lost, stack unchanged.</td>
</tr>
<tr>
<td></td>
<td>M - X</td>
<td>Result in X, previous X lost, stack unchanged.</td>
</tr>
<tr>
<td></td>
<td>1/X</td>
<td>Convert X from radians to degrees or vice versa. Previous X lost, stack unchanged.</td>
</tr>
<tr>
<td>Branch:</td>
<td>JMP</td>
<td>Unconditional jump. On call branch instructions, second word of instruction is the branch address, which is loaded into an external program counter by a load pulse from the NCU.</td>
</tr>
<tr>
<td></td>
<td>TJC</td>
<td>Test external jump condition, branch if true.</td>
</tr>
<tr>
<td>Input/output:</td>
<td>IN</td>
<td>Multidigit synchronous input from RAM or peripheral into X register.</td>
</tr>
<tr>
<td></td>
<td>OUT</td>
<td>Multidigit synchronous output to RAM or peripheral from X register.</td>
</tr>
<tr>
<td></td>
<td>AIN</td>
<td>Single digit asynchronous input. Wait for asynchronous data ready (AISR) to go low, then read data and pulse acknowledge flag F₂.</td>
</tr>
<tr>
<td>Mode control:</td>
<td>SMDC</td>
<td>Set mantissa digit count from one to eight digits.</td>
</tr>
</tbody>
</table>

**Floating-Point Notation**

1. 3 < N < 10 (one to eight mantissa digits)

2. 2. Two formats. The NCU can operate on data in floating-point or scientific notation formats with one to eight mantissa digits, depending on the setting of the digit count. It takes only one instruction to input or output a string of digits.
3. Stand-alone. The Number Cruncher can be used by itself in many control applications. Here a programmable ROM stores instructions, controlled by an external program counter, and a 256-by-4-bit RAM extends the internal memory. Multiplexers enter data or instructions.

memory register can store constants or temporary results or can serve as a loop counter for data transfer or program control. Additional data storage may be provided by external 256-word-by-4-bit random-access memories.

The two data formats are shown in Fig. 2. No reformatting is necessary when data is extracted from the 57109 or reentered from an external RAM. An asynchronous digit-input (AIN) instruction will accept a single digit when a data-ready signal indicates valid data.

Error detection is facilitated by an error flag, set by an arithmetic or output error. The TERR instruction tests the flag or can clear the external program counter, resulting in a hardware jump to memory location 0, the error recovery location. In either case, an ECLR instruction must be executed to clear the error flag.

The basic setup

The basic Number Cruncher system in Fig. 3 includes a programmable ROM for instructions, an external program counter, and a RAM for memory expansion. To fetch an instruction from the PROM, the NCU raises its ready line after it has executed the previous instruction. This signal is used as a clock to advance the program counter.

The PROM then accepts the new 8-bit address supplied by the PC, executes a read cycle, and supplies the instruction to the NCU. To facilitate entry of asynchronous instructions, the 57109 does not lower RDY and begin execution until its HOLD input is low.

When the incoming instruction is a test and skip, the chip activates RDY to advance the PC and obtain the next word on the PROM output lines. This word is actually a branch address.

If the branch condition is true, the NCU’s branch signal gates this address back to the program counter by parallel-loading it on the leading edge of the next RDY signal. When the PC is loaded, the PROM outputs will be the contents of the instruction at the branch address.

If the branch condition is not true, RDY is raised to step the PC so that it will point to the next sequential instruction at the time of the next instruction fetch.

The instruction-select signal (ISEL) selects which type of input will be used: instructions or data. The 2:1 multiplexers supply the Number Cruncher with data signals or instructions on the six input lines. This multiplexing saves pins so that the NCU can fit into a 28-pin package.

For a data-input instruction (IN), the Number Cruncher again raises RDY to advance the PC to the next instruction word, which contains a 4-bit high-order RAM address. The NCU supplies a 4-bit low-order digit address to the RAM from the digit-address DA lines and reads the RAM digit data on its input lines, having set ISEL low to select data instead of instructions. On a single IN instruction, 3 to 12 digits are input.

The OUT instruction procedure is similar to that for IN,
4. Partners. The NCU can extend processing power of a general-purpose microprocessor by taking instructions and data from the processor's bus and executing the instructions at its own pace. Flow chart shows software for microprocessor control of interface.

except that digit-output data is supplied on the data-output DO lines and the read/write line is pulsed to write each digit into the RAM. After putting out 3 to 12 digits, the 57109 enters a fetch cycle to obtain the next instruction.

Extending a processor

Software overhead can be staggering for microprocessor applications requiring mathematical functions or BCD operations. Sophisticated subroutines must be written for multiply, divide, square root, log, exponential, and trigonometric functions. The data must be scaled to fix the decimal-point position and to assure there will be no register overflow as a result of an operation. Further conversion is necessary if the result is to be given in floating-point or scientific notation.

However, the Number Cruncher provides a microprocessor with a convenient peripheral unit for performing these specialized calculations. The microprocessor controls the NCU simply by supplying it with valid instructions, directly or through a buffer memory. Overlapping execution in the two devices gives much greater throughput than when the microprocessor performs the calculations itself.

A straightforward processor-NCU interface can be built with a pair of latches (Fig. 4); one for instructions and input data, the other for output data. The processor suspends the NCU's operation through the latter's HOLD signal. When the microprocessor is ready, it loads the instruction latch with a 6-bit instruction code and sets HOLD low.

The Number Cruncher executes the 6-bit code. The microprocessor senses succeeding RDY signals from the 57109 (as an interrupt or jump-condition input) and then loads the latch with the next instruction. It supplies input data to the Number Cruncher on a digit-by-digit basis in the same manner as it does 6-bit instructions.

When the NCU has data to send back, it uses a 4-bit latch. The microprocessor reads and stores this data as it is loaded into the latch.

Using a FIFO

In another method for extending a microprocessor system with the Number Cruncher, a first-in, first-out buffer memory is a dynamic instruction store (Fig. 5). The microprocessor loads the FIFO, and the NCU draws instructions from it. Another FIFO is used for output data from the 57109. Since these memories are totally asynchronous, with separate input and output controls, the processor and the Number Cruncher can run at full speed in parallel for maximum system throughput.

This setup is useful in applications where the sequence of instructions executed by the NCU may change. Since the FIFO is a dynamic memory, it permits easy alteration of the sequence. Because instructions are stored only until the 57109 removes them, it is possible to load a very large sequence in a very small space.

When the microprocessor has a job for the NCU, it...
loads a linear sequence of instructions (no branches) into the instruction FIFO, which was initially cleared. Once loading has been completed, the processor is free to process data or control devices. The FIFO can be used as the storage medium for many different instruction sequences with only minimum microprocessor software required for loading.

The FIFO stacks the instruction words in the same order as they are entered and makes them available at the output in the same sequence. The processor treats instructions to the 57109 as output data, as if they were to be written into a RAM or loaded into a register. But it selects the FIFO as an I/O device by putting that memory's address on its address bus. Next it puts the NCU instruction data on the data bus followed by a write strobe, which the FIFO uses as an input data clock.

This sequence is repeated each time a word is loaded into the FIFO. Before transmitting each instruction word, the processor checks the FIFO's status-indicator flag. If the FIFO is full, the microprocessor waits until it is ready before resuming data transfer.

While the processor is loading data into the FIFO, the NCU is fetching instructions from the FIFO output ports at its own speed, executing them one by one. An output-indicator flag signals the 57109 when the ports are ready (FIFO not empty) or not ready (FIFO empty). When the processor has loaded the first instruction word, the FIFO is ready and may be interrogated. The Number Cruncher's ready line is used as a FIFO output clock to extract data and gate it onto its instruction input lines.

The last instruction executed empties the FIFO, which forces its output indicator to not ready. This flag is the hold input for the NCU and an interrupt input for the microprocessor, which senses that the Number Cruncher has completed its instructions.

The 57109 continues to execute instructions until it has completed its specialized calculations. It sends its results to the output FIFO using an OUT instruction. If output data is present in the FIFO, the processor senses this via an interrupt or jump condition. It obtains the results if needed or sends them on to an output device.

**Control by a ROM**

To transfer instructions where only a few sequences are necessary, a ROM can be programmed to contain the sequence of instructions for the NCU. This setup is similar to the stand-alone system in Fig. 3. It permits conditional test instructions not possible with the FIFO interface.

An AIN instruction suspends the Number Cruncher until the microprocessor requests a calculation. At that time the processor sets the asynchronous data ready (ADR) to 0 and supplies a 4-bit starting address code. The NCU decodes the starting address, branches to that address in the ROM, and executes the calculation routine there. As in the FIFO setup, an interrupt notifies the microprocessor when the 57109 has completed its task.

In this setup, the microprocessor does not have to load

---

5. **FIFO interface.** A microprocessor can control the Number Cruncher through first-in first-out memories. The microprocessor enters data and instructions into the instruction FIFO, and the Number Cruncher extracts them asynchronously.
a buffer memory to provide the NCU with instructions, but merely switches it on by supplying a single input (ADR). The result is very high system throughput and parallel processing.

In the analog data-acquisition system in Fig. 6, the PROM program controls the Number Cruncher. It makes the NCU measure analog variables, perform some digital transformation on them, compare the results to certain specified limits, and send out control information on the DO lines.

**Acquiring analog data**

An eight-input analog multiplexer selects the desired analog input channel based on a 3-bit address supplied by the NCU on DO1. This address is latched by the multiplexer and will not change during the conversion time of the three-BCD digit analog-to-digital converter via Flag 1. After starting the conversion via Flag 1, the NCU’s AIN instruction waits for the end-of-convert signal before reading one of the three digits through the 3:1 digital multiplexer. The second and third AIN instructions read the second and third BCD digits with the results stored internally.

The PROM program updates the analog address and tests to see if all analog channels have been interrogated. If so, the program will output the digitized data to the RAM or will process the data as required. If not all analog channels have been interrogated, the PROM program scans the next one.

This system uses internal NCU storage for simultaneous calculations on four three-digit numbers. Additional storage is provided by the 256-by-4 RAM so that the 57109 can operate on an array of data. Addressing the data in the RAM is facilitated by the IN and OUT instructions. The first instruction word is either IN or OUT, and the second supplies a 5-bit address to select one of 32 numbers in the RAM. This address is stable on the instruction input lines (16-1) and is valid throughout the data transfer cycle.

The Number Cruncher generates a 4-bit address (DAi) to select a digit each time it is ready to input or output 4-bit data. For an OUT instruction, digit data is output on DOi and clocked into the RAM by the R/W strobe. For an IN instruction, the high level on R/W causes the RAM to go into a read cycle and supply digit data to the NCU through the quad 2:1 multiplexers.
Dear Georgia:

I recently noticed that you are providing a list of microprocessor consultants for your readers in each issue of COMPUTE Newsletter. Please consider our corporation as a possible addition to that list.

Texas Microsystems, Inc. is a Houston, Texas based consulting firm started several years ago. In November of 1976, I left National to open the West Coast Office of TMI. TMI has the capability to provide complete microcomputer system design and development, including hardware and software design. We can handle the client's entire needs from evaluation and specification to system prototype and debug. Our experience ranges from IMP-16, PACE and SC/MP systems, to systems involving the 8080A, 8085 and 8048, as well as other microprocessors.

Before November 1976, I spent three years as a microprocessor systems design engineer with National, working on such projects, as the PACE/16-P interface card, PACE application cards, PACE LCDS and custom SCMP microcomputer systems. I am currently a member of COMPUTE.

Thanks for considering Texas Microsystems, Inc.

Sincerely,

TExAS MIcROSYSYSTEMS, INC.

GARY A. MILLER
Regional Director
West Coast Office
1530 The Alameda
Suite 200
San Jose, CA 95126
(408) 292-4004

Dear Mr. Marszalek:

Since I wrote you last week about the problems with the SC/MP Cassette system, I discovered a potential problem with the software in the SC/MP keyboard kit SKMPKB. It contains a re-executable subroutine KYBD at location X'0185 which can be used by other software for display and keyboard input. It should be pointed out to users of this subroutine that the Carry/Link (CY/L) flag must be reset (cleared, CCL instruction) prior to calling KYBD. If CY/L is set, the number returned in the E register will be incorrect for keyboard keys 8 thru F.

Is it possible to obtain a corrected copy of the SC/MP Keyboard Kit Schematic Diagram (Drawing NS10634) which is in the Keyboard Kit User's Manual? The one in my manual contains a large number of errors.

The SC/MP Cassette continues to work well — zero errors after many 1k byte reads and writes.

Sincerely,

Ronald G. Parsons
9001 Laurel Grove Drive
Austin, Texas 78758

Drawing NS10634 is replaced by NS10686 (shown on page 13 this issue) in revision 8 of SC/MP Keyboard Kit User's Manual.

My SC/MP based microcomputer is up and running. I built it for under $100 with 1K of RAM (2102's) yet!

On page 5-3 of the technical description I read of a user group and imagine you have information to share about using this CPU chip.

Please add me to the club. My particular interest is circuits showing how to expand my unit to TV, keyboard and cassette.

Any help at all is OK and let me know how I can aid you too.

Sincerely,

Bob Weir
318 N. 7th
Canon City, CO 81212

Dear Georgia:

I have built a Homebrew SC/MP, with 1K of 1702A, 1K of 2102LI, ASCII Keyboard, and selectric printing unit. I've implemented the hold and continue control lines and have a full front-panel LED display of addresses, data (read or write), and all flags and status indicators. I need some programming hints on subroutine linkage, etc.

Thanks,

Olin R. Boyer
P.O. Box 3000
Tulsa, OK 74102

See the SC/MP Programming and Assembler Manual Chap. 6 for some programming details. Also the SC/MP Applications Handbook has many programming examples.
SC/MP KEYBOARD KIT REPAIR POLICY

Kits may be returned to the Microcomputer Service Center for repair on a consignment basis only! *NO DEBIT MEMO'S*. The customer should return the kit, not the distributor. The following information *MUST* be supplied or kit will be returned.

1) Name of customer contact
2) Telephone number of contact
3) Data purchased
4) Purchased from
5) Symptom of problem

Upon receipt of the unit in the service center the technician will determine if the kit will be repaired under warranty or if the customer is responsible for its repair.

If the customer is found to be responsible, a charge of $35.00 per hour plus parts will be charged. A purchase order or check for the amount of the repairs must be sent to the service center prior to the return of the repaired kit.

Kits must be returned to:

NATIONAL SEMICONDUCTOR CORP.
2921 COPPER RD.
SANTA CLARA, CA. 95051
ATTN: MICROCOMPUTER SERVICE CENTER

The following spare parts are also available from the service center. A check payable to National Semiconductor must accompany all orders.

P/N482305235 — 001 KEYBOARD KIT ROM @ $25.00
P/N980305232 — 001 KEYBOARD & CABLE @ $35.00

**NCSS Expands Its Service**

National CSS has extended its telephone access and service through the world-wide TELEX network. This enables customers to access any of our host machines by dialing the NCSS TELEX rotor, 965806. International users may also access TWX by dialing 710-474-3540.

Line charges to the customer will be from the originating country to Stamford, Conn. All TELEX users should type (LTRS) NCSS after the connect light illuminates. Any problem during login should be reported to NCSS at (203) 327-9100 extension 381.

NATIONAL CSS, INC.
542 Westport Avenue
Norwalk, Connecticut 06851
(203) 853-7200
UNDERGROUND BUYING GUIDE
TELLS ELECTRONIC HOBBYISTS WHERE TO GET IT

A new directory has just been published that helps amateurs, CBers, experimenters and computer hobbyists locate equipment, parts, supplies and services.

Over 600 sources of standard and hard-to-find gear are listed in the handy guide. Many of the 600 sources are mail order firms and discounters. All are firms that do business with electronic hobbyists.

The Underground Buying Guide is available direct mail from PMS Publishing, 12625 Lido Way, Saratoga, CA. 95070. The price is $5.95 plus 55¢ postage and handling. Californians add 39¢ sales tax.

For further information contact:
Dennis A. King
PMS Publishing
12625 Lido Way
Saratoga, CA. 95070
(408) 996-0471

MICROPROCESSOR USER’S GROUP

The following programs are available from the COMPUTE User Group Library. Copies can be ordered from COMPUTE/208, National Semiconductor, 2900 Semiconductor Drive, Santa Clara, Ca. 95051.

These programs are versions of assemblers, interpreters or compilers available for IMP, PACE, and SC/MP. Included in this list is also a listing of modifications for the NOVA assembler that will allow it to produce PACE object code and a PACE assembler written in FORTRAN with modified assembly mnemonics.

Note: As part of the User Library, these programs are not supported as National products.

<table>
<thead>
<tr>
<th>Program Number</th>
<th>Program Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL0034A</td>
<td>NOVA</td>
<td>Instructions and listing for conversion of DATA GENERAL’s Nova Assembler to a PACE cross assembler. Limited copies available.</td>
</tr>
<tr>
<td>SL0040A</td>
<td>8080X IMP-16</td>
<td>8080 Cross Assembler for IMP-16. Object Module and source listing only available $15.00. Uses assembly directives similar to other National assemblers. Requires the following definitions: B=0, C=1, D=2, E=3, H=4, L=5, A=7, memory=6, PSW=6, Stack Pointer=7.</td>
</tr>
<tr>
<td>SL0042A</td>
<td>IMP-16</td>
<td>SM/PL is a high level programming language compiler for the IMP-16. See Compute Vol. 2, #8 for language features. It requires 16K of R/W memory and can be used with the IMP-16 disc system. Cost is $100.00 for the manual, object module paper tape and source listing.</td>
</tr>
<tr>
<td>SL0043A</td>
<td>SC/MP</td>
<td>NIBL is a version of Tiny Basic for SC/MP. It requires 4K of memory for the interpreter and an additional 2-4K for the NIBL source program. Cost is $15.00 for the paper tape load module and source listing. Both p- and n-channel versions are available.</td>
</tr>
<tr>
<td>SL046A</td>
<td>SC/MP-Basic PACE X-Assembler</td>
<td>Cross-assembler written in BASIC for PDP-8E with disc operating system. Listing only available. Contributed by R. Gitzel, University of Alberta, Edmonton, Canada.</td>
</tr>
</tbody>
</table>

COMPUTE Newsletter • Vol. 3 No. 6
<table>
<thead>
<tr>
<th>PROGRAM NUMBER</th>
<th>NAME</th>
<th>NUMBER OF PROGRAM LISTINGS</th>
<th>SOURCE PAPER TAPES</th>
<th>QUANTITY</th>
<th>UNIT COST</th>
<th>TOTAL COST</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL001A</td>
<td>BINBCD</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL002A</td>
<td>BCD</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL003A</td>
<td>MD</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL004A</td>
<td>PTBIN</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL005A</td>
<td>BINASC</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL006A</td>
<td>BINGRAY</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL007A</td>
<td>BCDBIN</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL008A</td>
<td>PNMULT</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL010A</td>
<td>MEMORY DUMP</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL011A</td>
<td>GALPAT</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL012A</td>
<td>RAMDUMP</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL013A</td>
<td>TAPE TITLER</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL014A</td>
<td>GRAY CODE</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL016A</td>
<td>PRPTPLT</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL017A</td>
<td>TSTPLT</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL019A</td>
<td>MESGH</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL020A</td>
<td>CHARST</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL021A</td>
<td>CONTAP</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL022A</td>
<td>DISC RLM-PROMSFT-B</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL023A</td>
<td>DISC RLM-PROMSFT-C</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL024A</td>
<td>TABTAP</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL025A</td>
<td>SORT</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL030A</td>
<td>TITLER</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL031A</td>
<td>DORIG</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL033A</td>
<td>TAPE</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL040A</td>
<td>8080-X</td>
<td></td>
<td></td>
<td></td>
<td>$15.00</td>
<td></td>
</tr>
<tr>
<td>SL042A</td>
<td>SM/PL</td>
<td></td>
<td></td>
<td></td>
<td>$100.00</td>
<td></td>
</tr>
<tr>
<td>SL044A</td>
<td>DECIM8</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL015A</td>
<td>PACRAM</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL018A</td>
<td>CALCULATOR</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL022A</td>
<td>NUMPRG</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL025A</td>
<td>PALM</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL026A</td>
<td>TATBAP</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL029A</td>
<td>BINBCD</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL032A</td>
<td>DIVIDE</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL033A</td>
<td>DELSEM</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL035A</td>
<td>PRNTLM</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL036A</td>
<td>BASCII</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL037A</td>
<td>JITTER</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL027B</td>
<td>SC/MP MATH</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL039A</td>
<td>TAP/E/O</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL041A</td>
<td>SCSORT</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL043A</td>
<td>NIBL</td>
<td></td>
<td></td>
<td></td>
<td>$15.00</td>
<td></td>
</tr>
<tr>
<td>SL047A</td>
<td>PLOT</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL028A</td>
<td>SC/MP-X</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL034A</td>
<td>PAC-RX</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL045A</td>
<td>PAC-X</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
<tr>
<td>SL046A</td>
<td>SC/MP-X</td>
<td></td>
<td></td>
<td></td>
<td>$5.00</td>
<td></td>
</tr>
</tbody>
</table>

*Price includes the manual, program listing, and paper tape load module.

†Available from the Melbourne Training Centre in Australia for DLR 100.00 for SM/PL and DLR 15.00 for NIBL.

Please make sure the programs you select are for the microprocessor you have.

Notes: 1. There is no charge for program listings, but the number of listings per order is limited to three (3). 2. NA indicates not available.

NAME ______________________ Fill out the form completely, make your check payable to COMPUTE, and mail to:

TITLE ______________________ UNITED STATES  GERMANY  AUSTRALIA

COMPANY _____________________ COMPUTE/208 National Semiconductor GmBH NS Electronics Pty Ltd.

ADDRESS _____________________ 2900 Semiconductor Drive 808 Fuerstenfeldbruck 808 Fuerstenfeldbruck 2500 Semiconductor Drive

CITY _________________________ Santa Clara, CA 95051 808 Fuerstenfeldbruck Industristrasse 10 808 Fuerstenfeldbruck

ADDRESS _____________________ 2500 Semiconductor Drive 808 Fuerstenfeldbruck Industristrasse 10 808 Fuerstenfeldbruck

CITY _________________________ Bayswater, Victoria 3153 32096 32096

TOTAL $ _______
CALL FOR PAPERS

IECI 78 CONFERENCE
"INDUSTRIAL APPLICATIONS OF MICROPROCESSORS"

SHERATON HOTEL • Philadelphia, Pennsylvania • MARCH 20–22, 1978

Papers on the Following Subjects are Invited:

- Industrial Uses of Microprocessors
- Microprocessor System Hardware Architecture
- Microprocessor Software and Standardization
- Microprocessor in Thyristor Controls
- Computerized Data Acquisition Systems
- Programmable Controllers
- MSI and LSI in Process Control
- Automotive Diagnosis and Operation
- Vehicle Control
- Automatic Inspection
- "Intelligent" Test Instrumentation
- Transducers
- Textile Manufacturing
- Food Processing
- Petroleum Refining
- Geophysics
- Metal Fabrication
- Power Generation
- Education
- The State-of-the-Art in Microprocessor Standards

PAPER REQUIREMENTS

Ten copies of the paper in summary form no longer than 600 words and an abstract of no more than 60 words, describing work not generally published or previously presented. The copies should be mailed by August 25, 1977 to:

H. W. MERGLER
Leonard Case Professor of Electrical Engineering
CASE WESTERN RESERVE UNIVERSITY
CLEVELAND, OHIO 44106
216/368-4574

The paper summary will be used for paper selection and session assignment and thus should clearly define the salient concepts and NOVEL features of the work described.

Notification of acceptance and format required for publication in the IECI '77 Proceedings will be sent to you by September 25, 1977. Final manuscripts of papers accepted for publication in the IECI proceedings must be received by November 25, 1977.

UNITED STATES
COMPUTE/208
National Semiconductor
2900 Semiconductor Dr.
Santa Clara, CA 95051
Tel: (408) 247-7924
TWX: 910-338-0537

GERMANY
National Semiconductor Corp. GmbH
808 Fuerstenfeldbruck
Industriestrasse 10
Tel: 08141/1371
Telex: 05-27649

AUSTRALIA
NS Electronics Pty Ltd.
Cnr. Stud Road & Mtn. Highway
Bayswater, Victoria 3153
Tel: 03-729-6333
Telex: 32096