8-inch

JA-751A

DOUBLE-SIDED FLOPPY DISK DRIVE

SPECIFICATION

MATSUSHITA COMMUNICATION INDUSTRIAL CO., LTD.

DATA EQUIPMENT & CONTROL SYSTEMS DEPT.

SYNELEC
DATENSYSTEME GmbH

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DRIVE JUMBERS JA-751A

DSI - DS4 Drive Select Jumbers

	B	C	Head Load
	O	O	Permanent Head Load
B	O	I	Head Load
C	I	O	Drive Select
	I	I	Head Load + Drive Select

	MO	MIC	MEC	Motor On
	O	O	O	None
MO	O	O	I	Permanent
MIC/	O	I	O	From Processor (Drive Select)
MEC	I	O	I	Motor On from Motor on Signal

IU/D4 In use LED from In use/From Head Load

RR Radial Ready (installed = with Drive Select)

RI Radial Index (installed = with Drive Select)

ADJ For Adjustment of PLL (normally out)

VS/VA Select PLL mode

RC Disconnects raw data out

Note : I = installed
O = out

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GEGENÜBERSTELLUNG SA 860 - JA-751A

	SA 860	JA-751A
Note 1	Motor On = 165 ms	Motor On = 1 s
	Motor On = PIN 18 (HL)	Motor On = PIN 4
	No Head Load	HL = PIN 18
	True Ready = PIN 8	No True Ready
Note 2	Sector = PIN 24	No Sector Output
	Only FM Data Separator	Full PLL
		PIN 24 = VFO SYNC
	No Post Comp.	Automatic post comp.track 60
	Standard edge Connector	Pin + Socket Connector
	Five Pin DC-Stecker	4 PIN Minifloppy DC
Note 3	Buffered Seek	No Buffered Seek

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Gegenüberstellung SA 860 - JA 751A

Note 1

The SA 860 has replaced head select with motor on. This allows the SA 860 to replace the SA 850 in theory. In practice the SA 860 should be handled using the true ready signal and compatibility to the SA 850 disappears.

The JA-751A uses an extra signal for motor on and the normal ready signal. Because motor on is an option the drive can be seen as a true replacement for the SA 850. By clever use of the motor on signal a customer can reduce media wear and at the same time achieve the same access times as the SA 850.

Note 2

The SA 860 can seperate FM data but not MFM data. The data seperator on the SA 860 us really only useful with hand sectored diskettes. This option is seldom used. The JA-751A cannot handle hard sectored diskettes.

The JA-751A has a on board data seperator which can handle MFM and FM this, together with the post comp facility, allows a customer to discard most of the extra support IC's in a normal LSI FDC.

The post comp on the JA-751A is at present not a jumper option but permanent. Our test indicate that with normal Pre comp values the drives still work at margin code 6. This means that post comp should have no negative influences.

Note 3

The SA 860 has buffered seek while the JA-751A has only 3 ms seek. This is a luxury option of the SA 860 which is difficult to implement with small operating systems and LSI controllers. This is probably not used by any of our customers. This is not an industry standard option.

Note 4

The JA-751A uses different connectors to the SA 860. The DC connector on the SA 860 is expensive and difficult to obtain. The DC connector on the JA-751A is the standard mini floppy connector. The SA 860 is an industry standard. The SA 860 uses an edge connector for the signal cable the JA-751A uses a pin and socket connector. The pin and socket connector is a cheaper and more reliable system. There is a tendency in the market to move to this type of connector. The only problem we should see is in evaluation units.

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Gegenüberstellung SA 860 - JA-751A

Summary

The SA 860 includes several innovations which make it an outstanding product, however most people simply want a slim line replacement for the SA 850.

The JA-751A fits this description better. The added option of a PLL on the JA-751A can prove a big money saver to systems houses.

München, den 01.03.1984

Du/mm

Table of Contents

1. Features

The JA-751 double-sided floppy disk drive has Media compatibility with IBM 3740 and SA 851.

In order to provide the high performance solution for OEM data storage application, this product is reduced weight, less deeper and half height sizing.

The information can be written and read in the single density and double density recording method, and the POST COMPENSATION function for compensating the wave forms when at double density recording and the VFO circuit incorporated in this product greatly improve the reliability of the data in the double density recording.

The JA-751 with the built-in VFO circuit may be used as it is even when a VFO is provided in the customer's control side.

The use in the recording method in the IBM format with the NEC's PD used as the FDD controller is assumed to be the standard. It can be also connected when designing with the Western Digital's FDC LSI FD-1791 or Fujitsu's MB8866 for the controller. In this case, refer to Section 3.2.11.

1.1 Composition

Each block of this product is developed based on the know-how of the conventional ones with improvement on the necessary parts for the special use for the thin type, as follows:

(1) Head Block

Uses the head and the head support system which give satisfactory results in both quality and performance among those used in the conventional products.

The carriage part is improved for the thin type.

(2) Head Positioning Part

Follows the metal band method which has been conventionally highly evaluated on the performance and the reliability.

(3) Media Driving Part

Designed to use the DC direct drive motor so that the entire driving system can fit to the thin type.

(4) Circuit System

VFO circuit is incorporated therein, and the conventional circuits are large scale integrated so as to improve the packaging density.

(5) Rating

Only two kinds of supply voltage: +24V and +5V DC are permitted to lower the power consumption.

Conforms to the domestic electricity treatment laws, and also allows the approval of UL (U.S.A.) and CSA (Canada).

2. Specifications

Item	Specification		Single Density	Double Density	Unit
Storage Capacity	Unformatted	Per Disk	6.4	12.8	M bits
		Per Track	41.7	83.4	K bits
	IBM Format	Per Disk	4.0	8.0	M bits
		Per Track	26.6	53.2	K bits
Transfer Rate			250	500	K bits/Sec
Access Time	Average Access Time within Track		83	83	mSec
	Seak Time from Track to Track		3	3	mSec
	Average Latency		91	91	mSec
	Settling Time		15 <Note 1>	15 <Note>	mSec
	Direction Change Time		15	15	mSec
	Head Load Time		50	50	mSec
	Motor Start Time		1	1	Sec
Recording Density	Maximum Recording Density (Innermost Track)		3.408	6.816	BPI
	Track Density		48	48	TPI
	Number of Tracks (Cylinders)		154(77)	154(77)	
	Number of Heads		2	2	
	Number of Indexes		1	1	

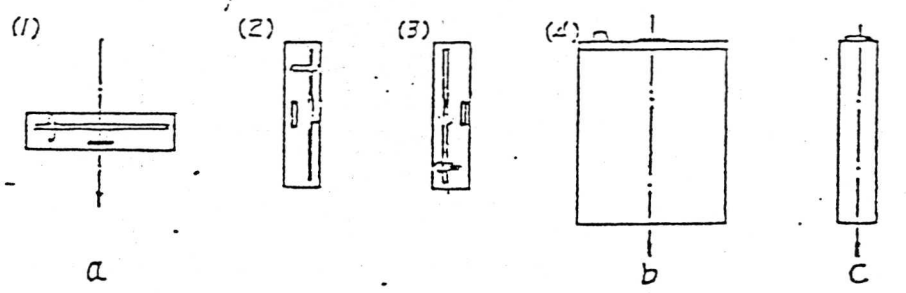
<Note 1> In the case of upto 50% of the average output; 25 mSec for upto 90%.

Item	Specification		Single Density	Double Density	Unit
Encording Method			FM	MFM	
Media Requirements			IBM Diskette 2 or its equivalent	IBM Diskette 2D or its equivalent	
Operating Environment Requirements	Ambient Temperature		5 ∿ 46		°C
	Relative Humidity(without dew condensation)		20 ∿ 60		RH
	Maximum Wet Bulb		25.6		°C
	Temperature Change		10		°C/H
	Vibration (except the resonance point)		0.3(5 ∿ 100Hz) or less		G
	Impact		5 or less (within 20mS)		G
Storing Environment Requirements	Ambient Temperature		-20 ∿ 60		°C
	Relative Humidity(without des condensation)		20 ∿ 90		RH
	Maximum Wet Bulb		29 or less		°C
	Temperature Change		Within 20		°C/H
	Vibration (except the resonance point)	Non-operating	1.0 or less (5 100Hz)		G
		When packed	1.5 or less (5 50Hz)		G
	Impact	Non-operating	15 or less		G
		When packed	25 or less		G

Item	Specification		Single Density	Double Density	Unit
Supply Power	DC 24 V	Voltage	±10 %		V
		Maximum Ripple	100		mVp-p
		Current	Except in rushing 1.0 In rushing 1.6		A
	DC 5 V	Voltage	± 5 %		V
		Maximum Ripple	50		mVp-p
		Current	Except in rushing 1.3 (Max)		A
Mechanical Dimensions	Width Height Depth		57 217 308		mm
Weight			3.0 or less		Kg
Reliability	MTBF	Under heavy usage	5.000		POH
		Under typical usage	10.000		POH
	P M (Preventive Maintenance)	Under heavy usage	5.000		POH
		Under typical usage	8.000		POH
	MTTR		30		second
	Component Life		15.000		POH
	Error Rate	Soft Error Rate	10^{-9}		Times/bits
		Hard Error Rate	10^{-12}		Times/bits
		Seek Error Rate	10^{-6}		Times/bits

Item	Specification		Single Density	Double Density	Unit
Reliability	Media Life	Single track wear	3.5×10^6		Passes
		Tap-tap wear	10^5		Times
		Seek wear	10^7		Seeks
		Insertions	3×10^4		Times
		Unload-wear	5×10^7		Passes
Safety	Incombustibility		Satisfies UL specifications		
<Note 1> Mounting	Mounting angel of ±3° in three directions : horizontal, vertical, and perpendicular				

<Note 1> See figures below.



2.1 IBM Compatibility

This device is provided with the characteristics specifications as described below to assure the media compatibility between the IBM FDD and our FDD JK-880, JK-885 and JK-888 series.

2.2 Characteristics Specifications

2.2.1 Output Resolution

When the output voltage of the read amplifier after write/read (recording method = MFM) is measured. Average minimum read back amplitude peak to peak should be as below.

This measurement is taken differentially at the test points TP1 and TP2.

Side	Track	Output Voltage (ali "1")	Resolution
Side $\overset{\Phi}{1}$	76	160 mVpp minimum	45 % minimum

The reference media should be determined.

The resulution shall be determined as:

$$\text{Resolution} = \frac{V1}{V0} \times 100\%$$

, wherein V1 is the average of the output voltages (P-P) at TP1 and TP2 after writing/reading 2F (data pattern of (00000000 = $(00)_{16}$ or 11111111 = $(FF)_{16}$), and V0 is the average of output voltages (P-P) at TP1

and TP2 after writing/reading 1F (data pattern of 10101010 = $(AA)_{16}$ or 01010101 = $(55)_{16}$).

2.2.2 Time Margin

(1) FM Encoding

When a random pattern or the repeated pattern of 11100101 = $(E5)_{16}$ is written/read, the time margin satisfies the specification:

$TM \geqq 0.15T$

, wherein T = Interval between clocks (4 μsec.)

(2) MFM Encoding

When a random pattern or the pattern of 11011101 = $(DD)_{16}$ is written/read, the time margin satisfies the specification:

$TM \geqq 0.15T$

, wherein T = Bit cell interval (2 μsec.)

(3) Interchangeability Time Margin

1) FM Encoding

$TM \geqq 0.13T$ T = 1 clock --- (4 μsec.)

2) MFM Encoding

$TM \geqq 0.13T$ T = 1 Bit cell interval (2 μsec.)

2.2.3 Positioning Information

Side	R_N
Side 0	$R_N = 51.5366 \div \frac{76-N}{48} \times 25.4 \pm 0.05$
Side 1	$R_N = 49.4208 \div \frac{76-N}{48} \times 25.4 \pm 0.05$

(mm)

Rn : Radius from the spindle center to the track center

N : Track Number (0 to 76)

Measured Track : N = 38

Measuring Altitude : See Figure 2 on Page 4.

2.2.4 Burst Timing between Index and Head

Burst timing between Index Sensor and Head is within ±400 μs.

2.2.5 Azimuth

Within 12 min. for either Head side 0 or side 1.

2.2.6 Off-track Time Margine (at MFM Encoding)

When the data pattern of 10101010 = $(AA)_{16}$ is written off-tracked by ±250 μm from Tr03 and Tr73, and then the data pattern of 11011101 = $(DD)_{16}$ is written/read on Tr03 and Tr73, the off-track time margin is 150 ns or more at 150 μm for either side 0 or side 1.

3. Interface Specification

3.1 Signal Interface and Pin Assignments

The interface signals and pin assignment are as listed in the table below, connector seen from back of drive. (JAE's PS-50PE-D4LT1-L1)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	LOW CURRENT
3	〃	4	MOTOR ON/OFF
5	〃	6	MFM
7	〃	8	VFO D (Optional)
9	〃	10	TWO SIDED
11	〃	12	DISK CHANGE
13	〃	14	SIDE SELECT
15	〃	16	IN USE
17	〃	18	HEAD LOAD
19	〃	20	INDEX
21	〃	22	READY
23	〃	24	VFO SYNC
25	〃	26	DRIVE SELECT 1
27	〃	28	〃 2
29	〃	30	〃 3
31	〃	32	〃 4
33	〃	34	DIRECTION SELECT
35	〃	36	STEP
37	〃	38	WRITE DATA
39	〃	40	WRITE GATE
41	〃	42	TRACK ϕϕ
43	〃	44	WRITE PROTECT
45	〃	46	RAW DATA
47	〃	48	RD DATA
49	〃	50	WINDOW

Table 2 Interface Signal List

3.2 Input Lines

Electric Specifications

Low = Logic 0 = (Vin) + 0.0V ∿ +0.4V @Iin = 40mA(Max)

High = Logic 1 = (Vin) + 2.5V ∿ +5.25V @Iin = 0mA(Open)

Input Impedance = 150Ω

Recommended circuit is shown in Figure 1.

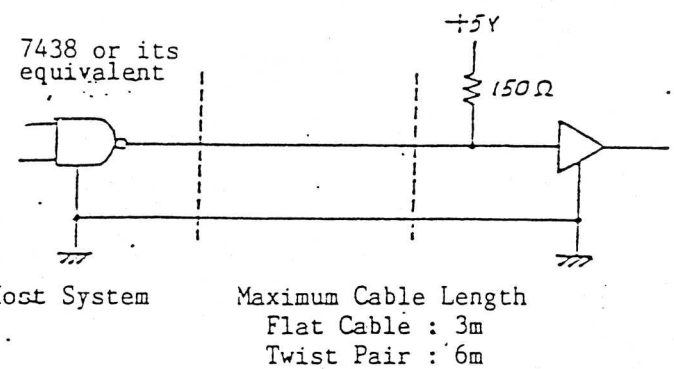


Figure 1 Input Interface

Input line termination

(1) The terminator consists of two DIP resister pack and packaged in the two IC sockets located near the symbol connector J1 on PCB.

(2) In the case of the digi-chain connection, to install these packs should be removed from all drives except one on the interface.

3.2.1 Drive Select 1 ∿ 4

Setting the drive select signal to the "Low" level enables the multiplexed I/$\bar{O}$ lines. Concretely speaking, the drive with this line active allow the gate of the output line to open.

Shorting plug DS1 to DS4 are used to select which drive select line will activate.

3.2.2 Head Load

When this signal goes to the "Low" level while the drive is ready, the R/W head will load against the diskette. Also, when in the HEAD LOAD state, the IN USE LED lights up and the door is locked. Writing/reading may be possible 50 ms after turning this signal to the "Low" level.

Conditions for the head load state can be selected by the user by inserting the shorting plugs.

	Shorting Plug	Pattern Cut	
−HL	C = O	B = ×	
(−HL) × (−DS)	C = O	B = O	(When shipped from the factory)
−DS	C = ×	B = O	

(B means the tracing)

3.2.3 DIRECTION SELECT

This signal defines the moving direction of the R/W head, at the time when the step line is pulsed.

When this signal is "High", the R/W head moves in accordance with the step signal away from the center of disk.

On the other hand, when this signal is "Low", the step signal causes the R/W head to move to the "IN" (toward the center).

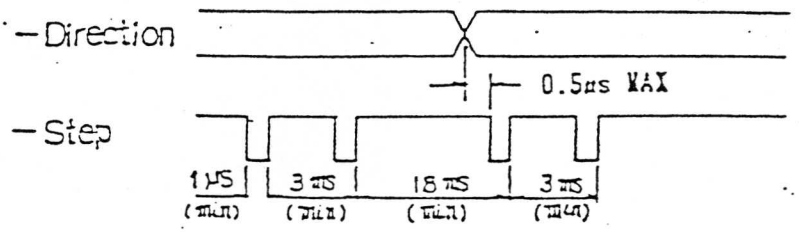
3.2.4 STEP

This interface signal is the control signal which causes the R/W head to move in the direction defined by the direction select signal. The head moves with this signal transition from "Low" to "High", or the trailing edge of the signal pulse. Any change in the direction select line must be made at least 0.5μS before the rising edge of the step pulse.

See Figure 2 for these timings.

Track-to-track access time is minimum 3 mS, however, when the direction select line is changed, it becomes minimum 18 mS including the settling time.

(1) Direction and Step



(2) Step and Track ØØ

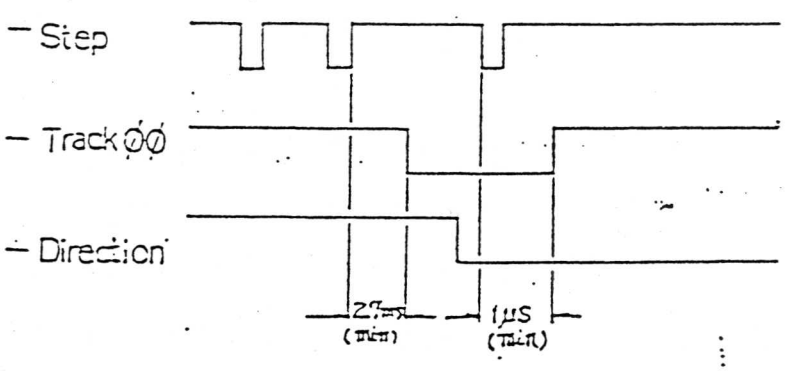
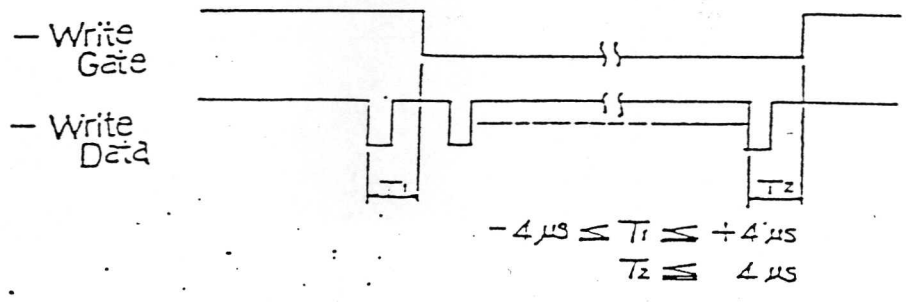


Figure 2

3.2.5 WRITE GATE

When this signal is "Low", data can be written in the media. When it is "High" on the contrary, the data can be sent out of the drive.

(1) Write Gate and Write Data



(2) Write Gate and Drive Select

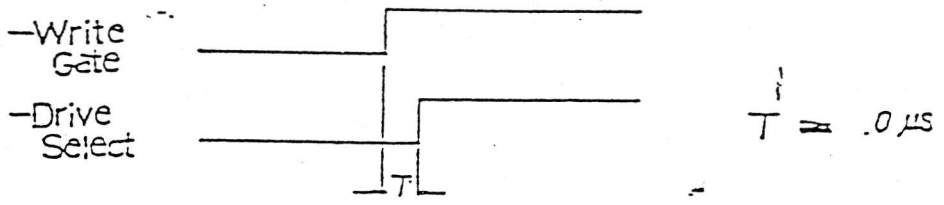


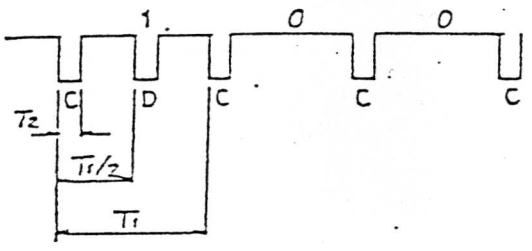
Figure 3

3.2.6 WRITE DATA

This signal is used for transfer of data to be written on the disk. Each transition from "High" to "Low" level will cause the current through the R/W head to be reversed. This line works when the write gate is "Low". Figure 4 shows the write data timing.

Do not perform the write precompensation to the Write Data.

(1) Write Data Timing in FM Encoding

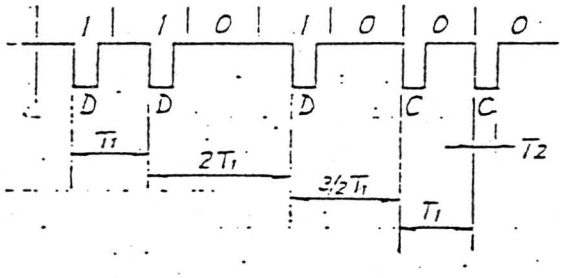


Frequency Accuracy T1
4.00μs±10ns

Pulse Width T2
150 ∿ 1100 ns

Rising, Falling
50 ns or less

(2) Write Date Timing in MFM Encoding



Frequency Accuracy T1
2.00μs±10ns

Pulse Width T2
150 ∿ 600 ns

Rising, Falling
50 ns or less

Figure 4

3.2.7 SIDE SELECT

This signal defines which side of a two-sided media is used for reading or writing. When this signal is "High", the R/W head on the Ø side of the media. When switching from the side Ø to the side 1, or vice versa, it takes 100 S before starting the read or write operation. When using the single-sided media, set this signal to the "High" level. If the side 1 is selected while a single-sided medium is inserted, the ready signal is released.

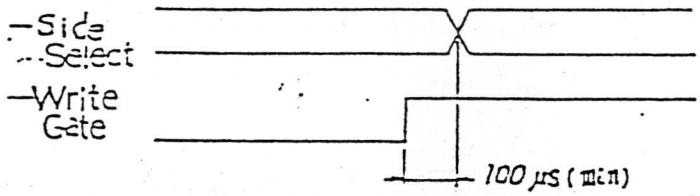


Figure 5

3.2.8 Write Current Switch (LOW CURRENT)

This signal is used as the current switch signal only in writing. The signal level is "High" when writing on TRKØØ to 43, and "Low" when writing on TRK44 to 76. Post Compensation in reading is automatically performed within the drive.

3.2.9 IN USE

For use as the signal that allows the IN USE LED to turn on in the ready state while the head is loaded. Even when the head is not loaded, this signal is used if the IN USE LED is desired to light up.

3.2.10 MFM MODE

This interface signal designates the recording mode of the VFO circuit. When this signal is "Low", it works in MFM, and when "High", in FM recording mode.

3.2.11 VFO SYNC

This interface signal designates the operating mode of the VFO circuit. "Low" level of this signal allows the read operation, while "High" level prohibits it.

Figure 6 shows the timing when using in IBM format. This timing is for the NEC's FDC μPD765.

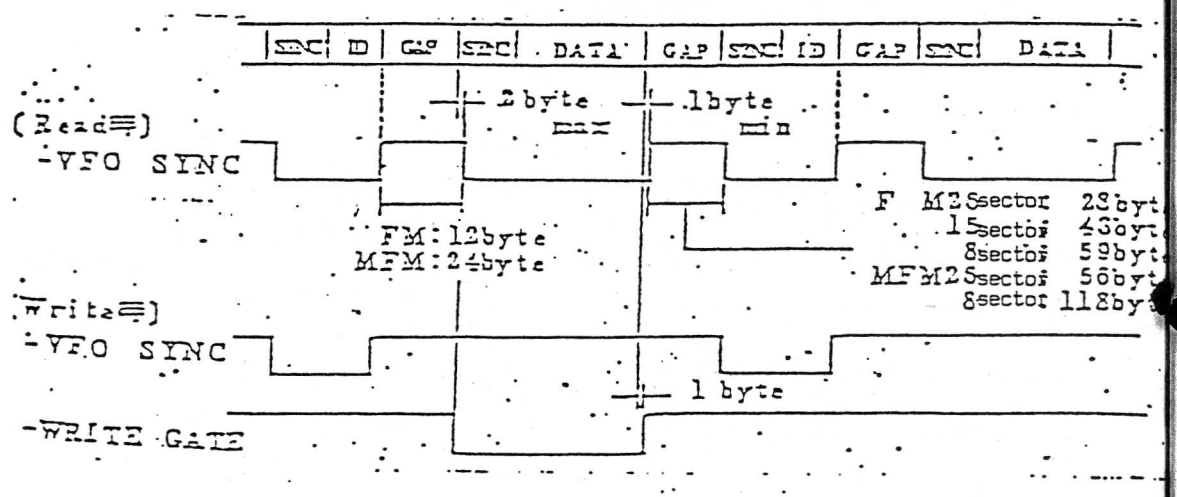


Figure 6

When designing to use Western Digital's FDC LSI FD1791 or Fujitsu's MB8866 as the controller, following requirements should be satisfied:

(1) Input RG signal instead of VFO SYNC signal.

Timing of -RG signal is illustrated below.

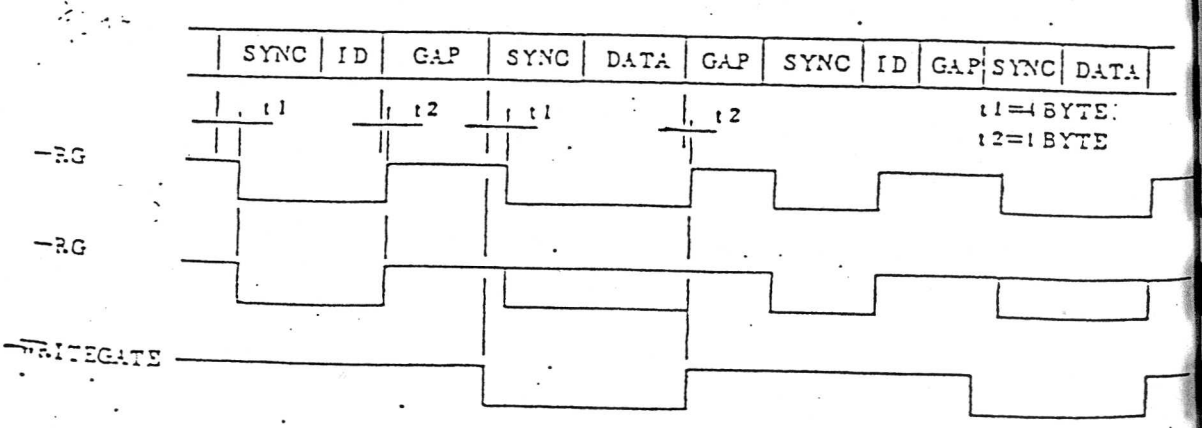


Figure 7 RG Timing

(2) Open the shorting plug (trace) "VS" on the P board to short "DA".

(3) Install the shorting plug (trace) "VD" on the P board, and input "-VFO D" signal from the pin No. 8 of the I/C interface.

The -VFO D signal is the input signal controlled by the -RD DATA signal and WINDOW signal. Add the circuit diagram shown in Figure 8.

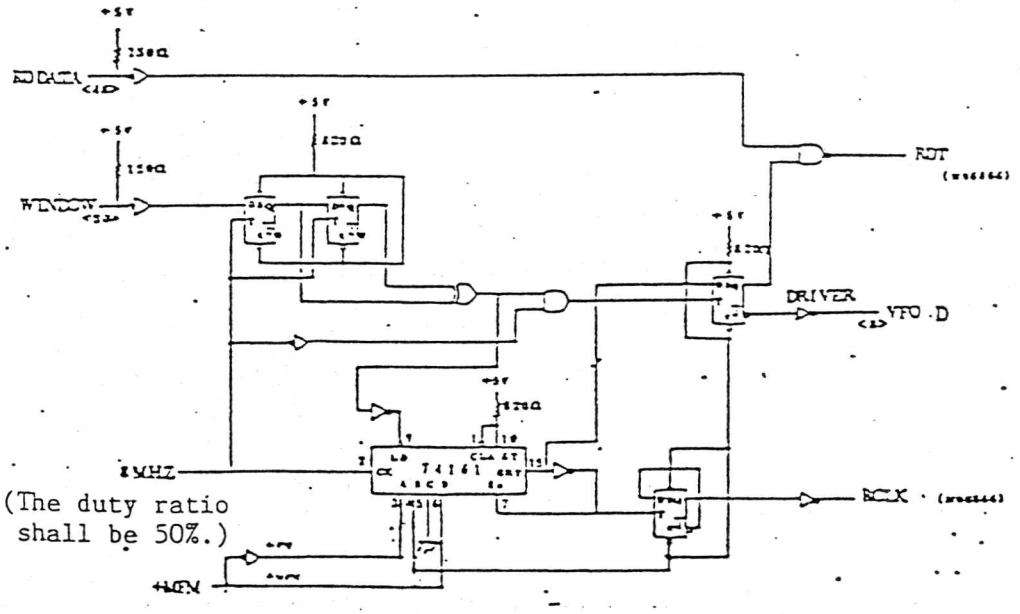


Figure 8

3.3 Output Line

When the control signal is "Low", it is driven by the open collector capable of the sinking current of maximum 40 mA, and the output level at this time is maximum 0.4V. When the control output signal is "High", the drive transistor is "OFF", and the collector Cut-Off current is maximum 250 μA.

Following illustrates the recommended conneciton of the I/C interfaces.

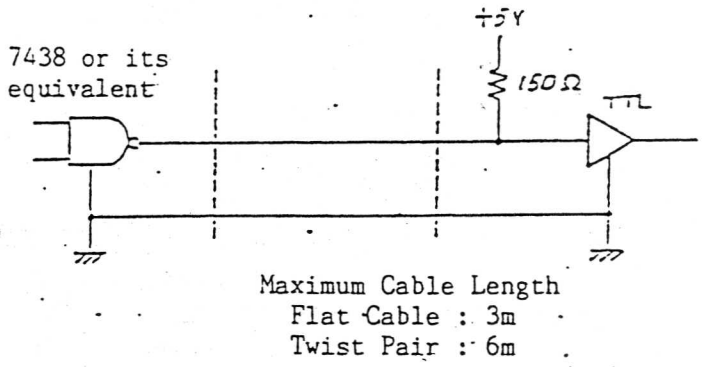


Figure 9

3.3.1 INDEX

This signal is sent out of the drive on every rotation of disk (166.7 mS) to indicate the start of each track. This signal is normally "High", and the "Low" level pulse is generated once every rotation for about 2.3 mS. In order to detect the index on the host system correctly, neglect the index signal on the instance of Drive Select.

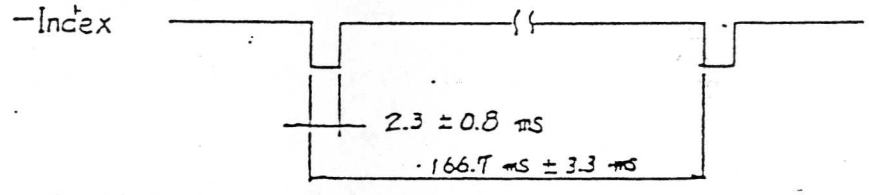


Figure 10 Index Signal

3.3.2 READY

This interface signal goes to the "Low" level when the following three conditions are all satisfied:

(1) All the power is turned on.

(2) The disk rotation reaches 70% or more of the normal working speed, and after it turned twice.

(3) Diskette are correctly installed.

When any one of the drive ready conditions above is not satisfied, this signal goes to the "High" level.

3.3.3 WRITE PROTECT

This interface signal is issued from the drive to inform the user of the installation of a write-protected diskette.

When write-protected, the signal is "Low", and when not protected, it is "High".

The write protect notch is provided in ISO and JIS.

3.3.4 TRACK ØØ

This signal is "Low" only when the R/W head is on the outer most track ØØ and the current flows through the

phases 1 of stepper motor. It is at the "High" level when the R/W head is not on the track ØØ.

3.3.5 RAW DATA

Timing of the raw data differs between FM and MFM. Timing of the bit position is shown in Figure 11. Trace RC should be shorted when this signal is output through pin 46 of connector J_1. Then the trace RC is cut, it is not output.

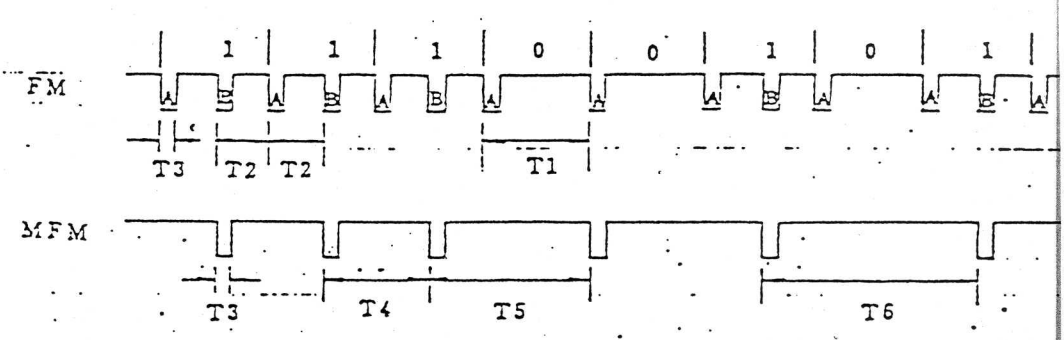


Figure 11 Read Data

A bit : Rising edge of the pulse is within ±400 ns from the reference position thereof.

B bit : Rising edge of the pulse is within ±200 ns from the reference position thereof.

T1 = 4.00 μS TYP	T4 = 2.00 μS TYP
T2 = 2.00 μS TYP	T5 = 3.00 μS TYP
T3 = 200 ns ± 50 ns	T6 = 4.00 μS TYP

Time is required after the Write Gate goes to the High level before Read can be performed correctly.

This is called the Read Recovery Time, and requires at least 100 μS.

3.3.6 RD DATA

This signal is the read data stabilized by the VFO circuit, and consists of clock and data bit.

3.3.7 WINDOW

This signal is created by the VFO circuit for use in dividing the clock and data bit in the RD data signal. Timing of this signal with the RD data signal is given in the following figure:

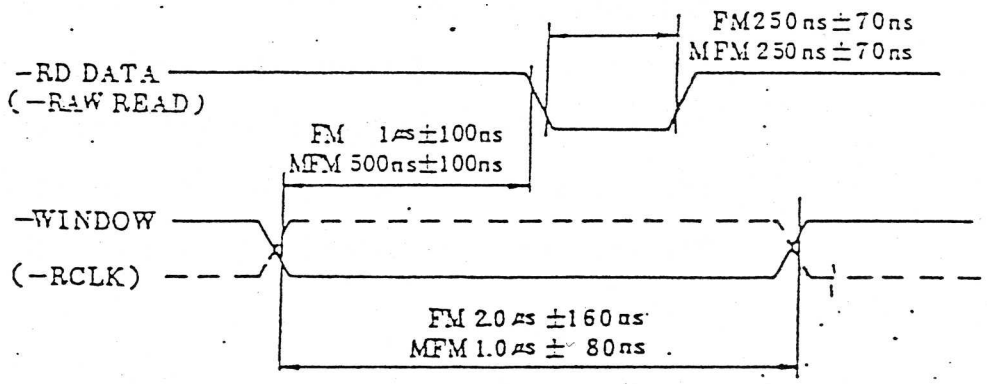


Figure 12 Relation between RD DATA and WINDOW

3.3.8 TWO SIDED

This signal will indicate "LOW" when the two-sided media are installed in the drive, and indicate "HIGH" when the single-sided media are installed.

3.3.9 DISK CHANGE

This signal is at the "Low" level when Drive Select is activated if while deselected the drive has gone from a Ready to a Not Ready condition.

This signal is reset by the transition of Drive Select Signal from "Low" to "High" if the drive has gone Ready.

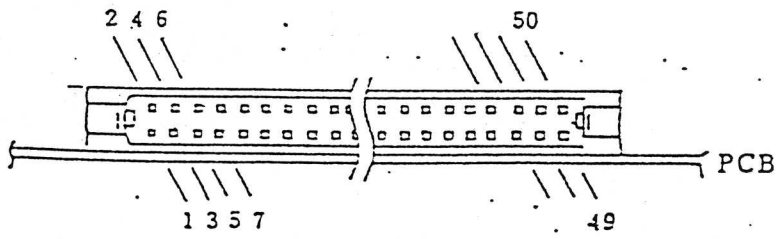
4. Connector

There are two types of connector, J_1 and J_5, between the JA-751 and the host system. The connector J_1 is used for the interface signal, and J_5 for the DC power for the circuits (motor driving power).

4.1 J_1/P_1 Connector

The interface signal connector J_1 is located on the bottom on the PCB part side surface. The used connector is JAE's PS-50PE-D4LT1-L1. Recommended connector P_1 on the cable side is also the JAE's PS-50SEO-D4P1-1C.

Pin Nos. of the connector J_1 are as illustrated below.



Connector J 1
(observed from the front pin side)

Figure 13 Connector J 1

4.2 J_5/P_5 Connector

The connector J_5 for the DC power is fixed on the soldered surface side of PCB. J_5 used AMP's connect P/N 172 94-1 provided with 4 pins. The connector P_5 on the other side uses the pins of the socket 170121-1 of 1-4804240.

Pin arrangement viewing from the rear side is shown below.

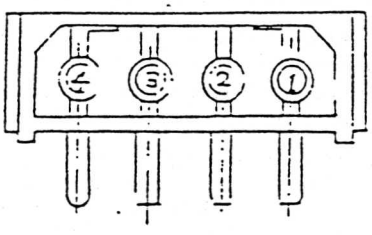


Figure 14

Pin No.	1	2	3	4
Type	+24V	+24V RETURN	GND	+5V

5. Type of Shorting plugs and Setting Thereof

There are shorting plugs as listed below on the JA-751 PCB. Inserting these shorting plugs causes the signals in this list to be sent or received.

Short Pin Name	Description
DS1	Inserted when selecting as the drive 1 (inserted in the standard shipping).
DS2	Inserted when selecting as the drive 2.
DS3	Inserted when selecting as the drive 3.
DS4	Inserted when selecting as the drive 4.
DS △3 SI	When DS is inserted and the drive has been selected, the current is applied to the stepping motor. When SI is inserted, the current is applied to the stepping motor only in seeking or head load. When DS and SI are drawn out, the stepping motor is kept turned on.
C	By inserting the shorting plug, conditions for the head load state can be selected by the customer. (See Page 12.)
VS VD	Using upd765 makes it shorted, and using MB8866 makes it open while DA is shorted. Using upd765 makes it open, and using MB8866 makes it shorted.

(When making the standard shipping, it is inserted to VS.)

Shorting plug

AMP Co., Ltd. : P/N141767-1
Yamaichi Electric Company : KS-20707B

6. Supply Power and Motor Actuating Time

6.1 Type and Power-on Procedure

Types and ratings of the DC supply power are as shown in Section 2 (on Page). The power-on procedure is not specifically designated, except that the write gate signal must be turned off before turning on and off the power.

6.2 Motor Actuating Time and DC Supply Power

It takes one sec. after starting the motor to reaching the fixed speed. Therefore, it is necessary to turn on the -5 V supply power within one sec. after turning on the +24 V supply power.

6.3 Installation of Media

It is recommended to install and clamp the media after the motor rotates so as to extend the life of the media.

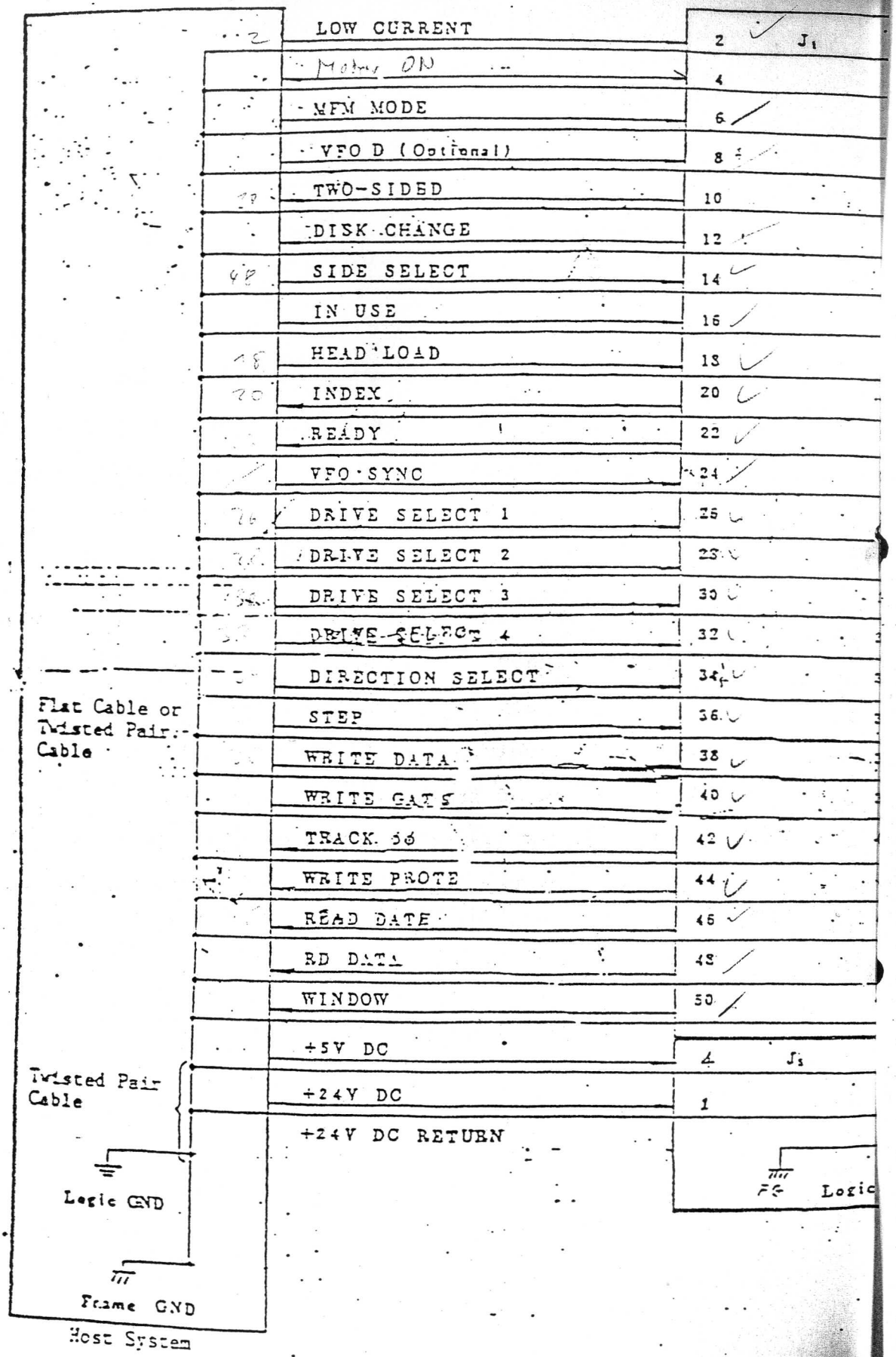
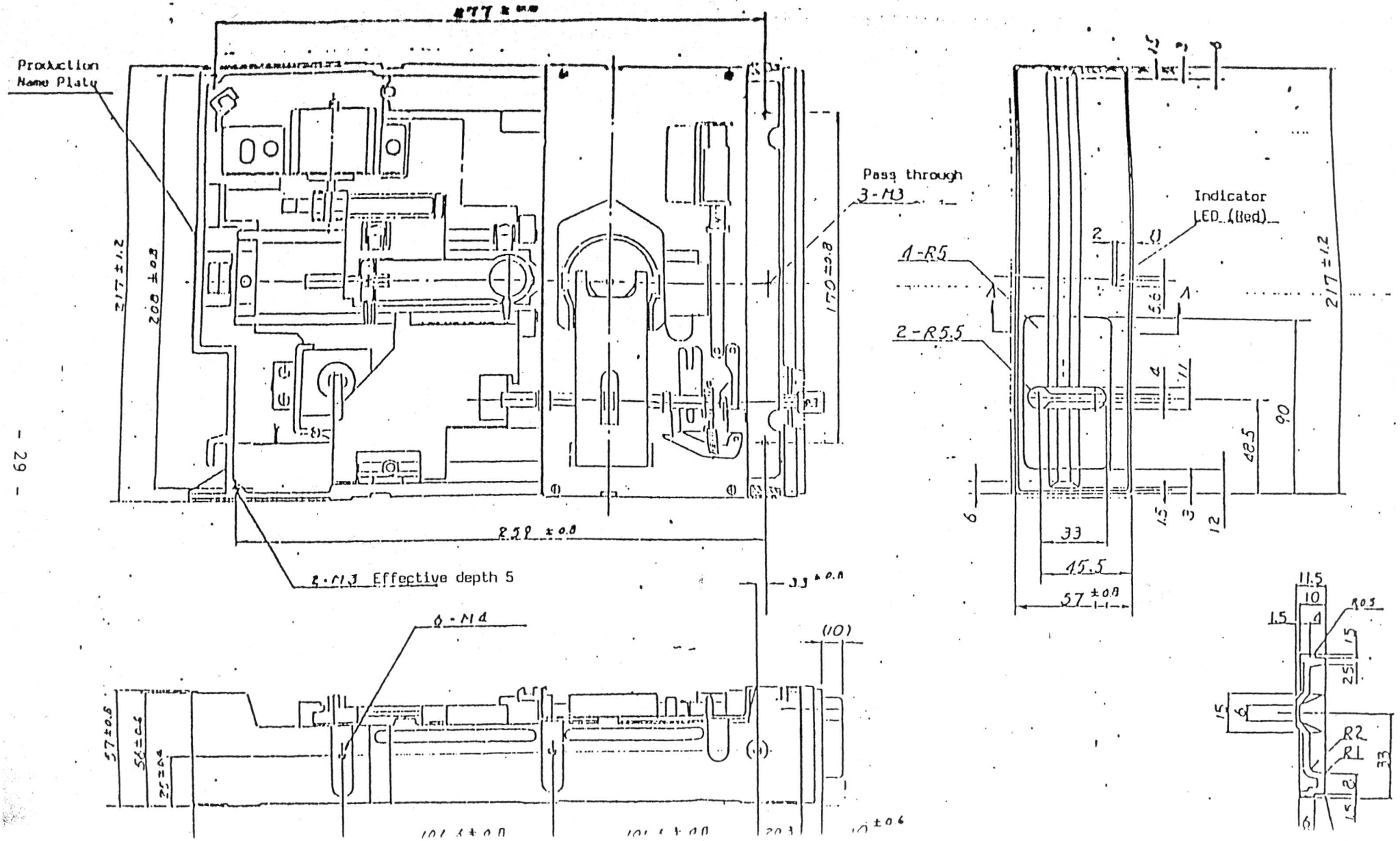


Table 6 Interface Connection


Protection
Name Plate
Pass through
3-M3
Indicator
LED (Red)
1-R5
2-R5.5
2-M3 Effective depth 5
ϕ-M4
217 ±1.2
208 ±0.3
170 ±0.8
259 ±0.8
33 ±0.8
57 ±0.8
33
15.5
11.5
R0.5
R2
R1