MICROFORMATTER ADDENDUM

FOREWORD

This addendum is designed to be used in conjunction with Pertec Peripherals Corporation (PPC™) tape drive models T6000, T7000, T8000, T9000, and T1000 having microformatter capabilities.

The document describes the theory of operation, interface specifications, installation and interface connections. Also described is the Power Supply II PCBA.

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SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides the physical description, functional description and specifications for the NRZI, PE, and Dual (PE/NRZI) Microformatters manufactured by Pertec Peripherals Corporation (PPC™), Chatsworth, California.

1.2 PURPOSE OF EQUIPMENT

The microformatter, in conjunction with a companion PPC tape drive, enables the generation and decoding of ANSI and IBM compatible, 9-track, NRZI (800 cpi) and PE (1600 cpi) tapes. All timing and control necessary for the recording and reproduction of NRZI or PE data are provided by the microformatter.

Model numbers for microformatted systems are given in Table 1-1. The system is comprised of a PPC tape drive and an internally mounted microformatter.

1.3 PHYSICAL DESCRIPTION

The Microformatter PCBA is mounted within the tape drive as illustrated in Section II of the companion Operating and Service Manual. An additional 5-volt regulator is added to the drive to supply voltage to the Microformatter PCBA. The interface signals from the customer's controller are connected to the Microformatter PCBA via edge connectors.

Table 1-1
Microformatted Systems

PPC Model No.	Data Format Drive			Data Format Formatter			Drive Tape Speeds Available							
	PE	NRZI	PE/ NRZI	PE	PE/ NRZI	NRZI	12.5	18.75	25	37.5	45	75	112.5	125
FT6840-9F		X			X		X	X	X	X	X			
FT6640-9F	X			X			X	X	X	X	X			
FT6840-9DF		X				X	X	X	X	X	X			
FT6640-9DF	X					X	X	X	X	X	X			
FT6640-98DF			X			X	X	X	X	X	X			
FT7840-9F		X			X		X	X	X					
FT7640-9F	X			X			X	X	X					
FT7640-9DF	X					X	X	X	X					
FT8840A-9F		X			X		X	X	X	X	X			
FT8640A-9F	X			X			X	X	X	X	X			
FT8840A-9DF		X				X	X	X	X	X	X			
FT8640A-9DF	X					X	X	X	X	X	X			
FT8640A-98DF			X			X	X	X	X	X	X			
FT9840-9F		X			X					X	X	X		
FT9640-9F	X			X						X	X	X		
FT9840-9DF		X				X				X	X	X		
FT9640-9DF	X					X				X	X	X		
FT9640-98DF			X			X				X	X	X		
FT1640-98DF			X			X						X	X	X

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1.4 FUNCTIONAL DESCRIPTION

All logic and functions associated with the reading and writing of 9-channel NRZI or PE ANSI and IBM compatible tape are contained in the microformatter.

For NRZI operation, all logic for the generation of the initial gap, Inter-Block Gaps (IBGs), and file mark gaps is provided, in addition to the logic necessary to record data on tape. The logic for complete data recovery (including buffering, error and file mark detection) is also provided.

The NRZI functions of the microformatter include the following:

(1) Compatibility with drives having either single- or dual-stack heads.

(2) Provision for fixed and variable length erase commands.

(3) Facility for the generation of special commands for editing previously recorded tapes.

(4) Facility for internal or external parity.

For PE operation, all logic for the generation of the preamble, postamble, PE data, and file mark is provided, in addition to the logic necessary to record data on tape. The logic for complete data recovery (including data decoding, buffering, error and file mark detection, and error correction) is also provided.

The PE functions of the microformatter include the following:

(1) All timing necessary for the generation of IBM compatible IBGs and for correct head positioning between records.

(2) Compatibility with drives having either single- or dual-stack heads.

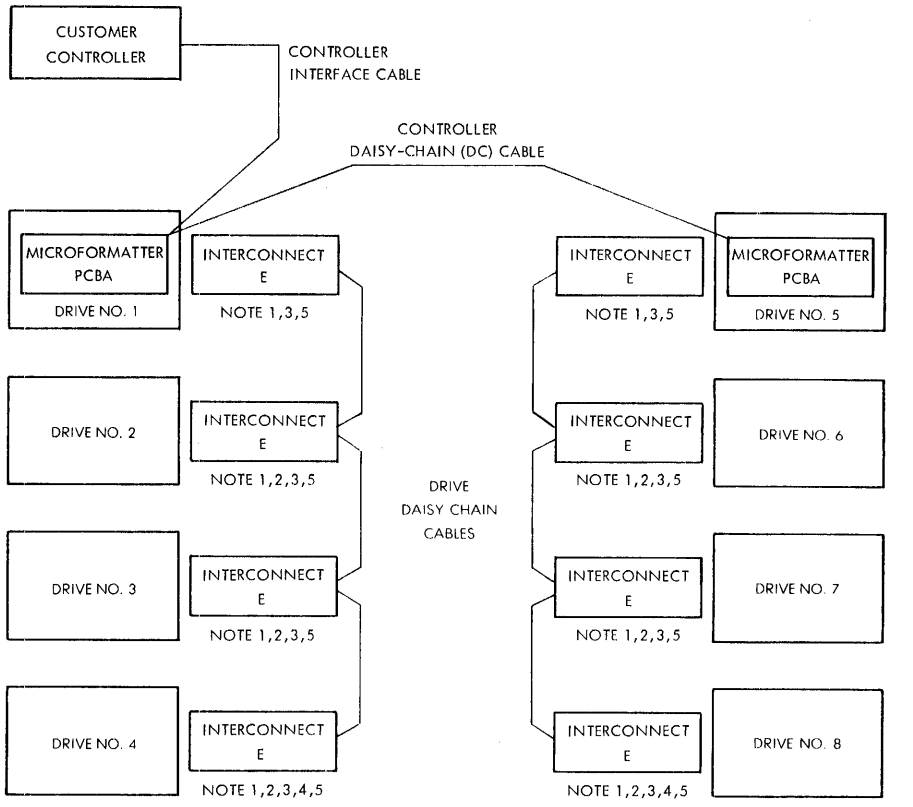
(3) Automatic recording of a PE identification burst prior to recording the first record on a tape.

(4) Automatic testing for the PE identification burst when reading the first record on a tape.

(5) Provision for fixed and variable length erase commands.

(6) Facility for the generation of special commands for editing previously recorded tapes.

Two microformatters may be daisy-chained to a controller and up to four drives may be daisy-chained to a microformatter. Figure 1-1 illustrates a system configuration of eight drives, two of which are microformatted drives.



NOTES:

1. THESE INTERCONNECT E PCBAS ARE DC PCBAS WHEN USED WITH T7000 DRIVES ONLY.
2. THESE INTERCONNECT E PCBAS ARE MTA II WHEN USED WITH T6000, T8000 AND T9000 DRIVES THAT DO NOT HAVE MICROFORMATTER CAPABILITY.
3. THESE INTERCONNECT E PCBAS ARE NOT REQUIRED WHEN USED WITH T1000 DRIVES.
4. TERMINATORS ARE REQUIRED ON THE LAST DC PCBA ON A DAISY CHAIN.
5. THE UNIT SELECT SWITCH IS LOCATED ON THE DC II PCBA OR THE INTERCONNECT PCBA.
6. DISCONNECT P5 FROM J5 ON THE INTERCONNECT E PCBA ON ALL SLAVE FT6000, FT8000, AND FT9000 DRIVES ON A DAISY CHAIN.

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Figure 1-1. Typical System Configuration

MICROFORMATTER PCBA

CONTROLLER

P5 46 ITAD1, 48 IFAD, 18 IFEN
P4 46 ITAD0
P5 40 ISPEED
P6 2, P1 1 IPSEN

PART OF U112
3 4
ADDRESS SELECT

ISLT1, ISLT2, ISLT3, ISLT0, ISPD
P2 33 31 28, P1 9, P3 22
DRIVE

CONTROLLER
P5 28 IRDY, 44 IONL, 30 IRWD, 32 IFPT, 4 ILDP, 22 IEOT, 26 INRZ
P4 14 ISGL

PART OF U112
5 NRZI
PART OF U112
6 SINGLE

P1 19 IRDY, 6 IONL, 5 IRWD, 4 IFPT, 3 ILDP, 2 IEOT
P3 25 INRZ, 23 ISGL
DRIVE

CONTROLLER
P4 16 ILOL, 20 IRWC, 38 IEDIT, 34 IWRT, 44 IRTH 1, 36 IRTH 2, 18 IREV, 40 IERASE, 42 IWFM, 8 IGO

P1 17 ILOL, 10 IRWC, 15 IOVW, 8 ISWS
P2 30 IRTH1, 29 IRTH2
DRIVE

CONTR
CONTR

INTERFACE LOGIC

SPEED

CLOCK GENERATOR
1 2 3 4 5 6 7 8
U187 (FREQ SELECT)

WCLK
NWCLK

EDIT, WRT, NRZ, WFM
LDP, ERASE, EOT, GOI
SFC, SRC, SGL, NRST
WARS
REV1, WD, WSTR, FBY
DBY

REV1, LDCRC, DBY, LDCRC
WCN0, WCN1, WCN2, LDWRTDATA
RGATENZ1, RGATENZ2, RENDNZ, FMKNZ

REV1, WCLK, NWCLK, RGATENZ1, RGATENZ2
NRZI READ CONTROL
CCG, RDS, RDNZP-7, NCLRNZDATA, RSTRNZ, HERNZ, FMKNZ, RENDNZ

NWCLK
WCLK

CONTROLLER
P4 4 ILWD

MASTER CONTROL

RGATEP2, IDGATE, RGATEP1
FMKPE, RENDPE

COPY, NCOPY, DGATE/0, DGATE/2, ENV/0, ENV/2
TRACKING OSCILLATOR
R3
FREQUENCY ADJUSTMENT
SHRCLK, NRCLK2, SHLCLK, NSHRCLK, NRCLK1, ECLK

P6 1 GROUND
3 +5V

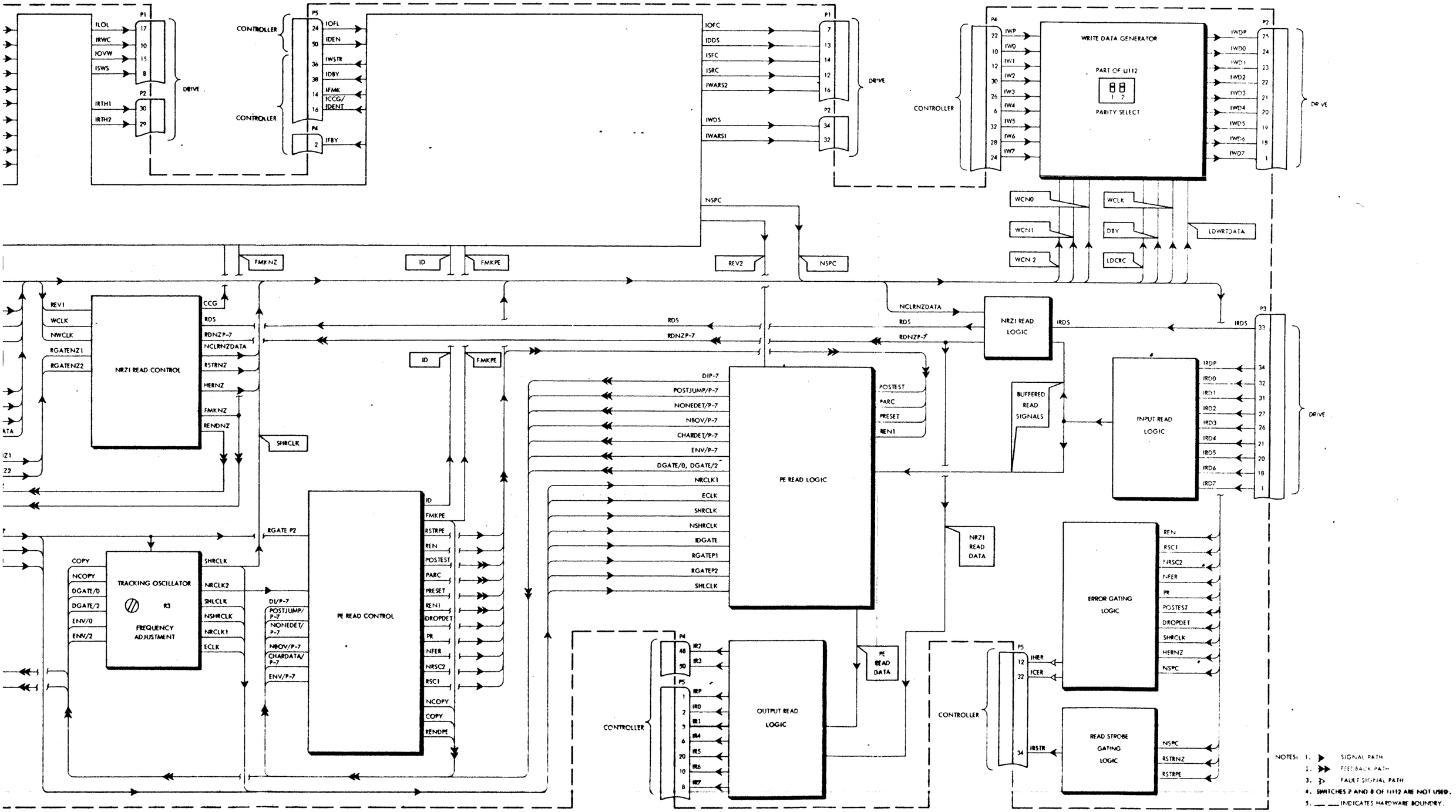

Figure 4-1. Dual Microformatter Block Diagram

SECTION II
INSTALLATION AND INTERFACE CONNECTION

2.1 INTRODUCTION

This section contains a summary of the physical interface connections for the microformatter. Also given are the configuration requirements of master and slave drives when used in a daisy-chain configuration.

2.2 INTERFACE ELECTRICAL SPECIFICATIONS

Levels: True = Low = 0v to +0.4v dc
False = High = +3v dc

Pulses: Levels as above. Minimum pulsewidth is 1 microsecond.

The interface circuits are designed so that an open circuit results in a high signal. Figure 2-1 shows the configuration of the drivers and receivers between the controller and microformatter.

2.3 POWER SPECIFICATIONS

The power consumption of the Microformatter PCBA and the +5 volt regulator is 60 watts (maximum). This consumption is in addition to the drive power requirements listed in Section I of the companion drive manual.

2.4 INTERFACE CONNECTIONS

Two 50-lead flat cables (3M 3365-50 or equivalent) are required for the microformatter to controller interface. This interface is given in Table 2-1. These two cables connect directly to P4 and P5 on the Microformatter PCBA. The two 50-lead flat cables are not supplied by PPC. Two edge connectors are required and will be supplied by PPC upon request at no charge. Edge connector part numbers are: PPC P/N 503-0147; 3M P/N 3415.

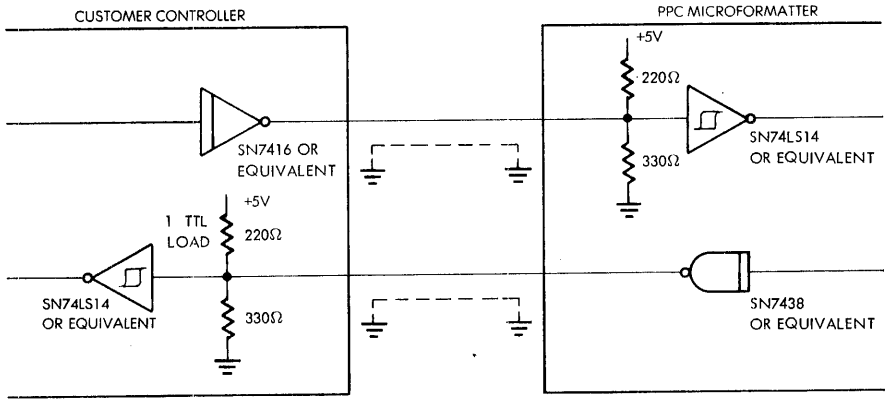

Figure 2-1. Driver/Receiver Interface Configuration

To connect the interface, the following must be considered.

(1) When connecting a controller to a single microformatter, the length of cable should be limited to 12.2 m (40 feet).

(2) When two microformatters are connected in a daisy-chain configuration to a controller, the *total* cable length should be limited to 12.2 m (40 feet). There should be no more than 1.5 m (5 feet) of cable between the two microformatters, although this distance may be increased to 6.1 m (20 feet) if a 220/330 ohm DIP terminator for each microformatter to controller interface signal is installed within 305 mm (12 inches) of the last microformatter in the daisy-chain.

Table 2-1

Controller/Microformatter Interface Lines

Microformatter P4/P5		Signal (Controller to Microformatter)	Microformatter P4/P5		Signal (Microformatter to Controller)
Live Pin	Return Pin		Live Pin	Return Pin	
P5-48	P5-47	FORMATTER ADDRESS (IFAD)	P4-2	P4-1	FORMATTER BUSY (IFBY)
P4-46	P4-45	TRANSPORT ADDRESS (ITAD0)	P5-38	P5-37	DATA BUSY (IDBY)
P5-46	P5-45	TRANSPORT ADDRESS (ITAD1)	P5-16	P5-15	CHECK CHARACTER GATE (ICCG)*
P4-8	P4-7	INITIATE COMMAND (IGO)	P5-16	P5-15	IDENTIFICATION (IDENT)*
P4-18	P4-17	REVERSE/FORWARD (IREV)	P5-12	P5-11	HARD ERROR (IHER)
P4-34	P4-33	WRITE/READ (IWRT)	P5-14	P5-13	FILE MARK (IFMK)
P4-42	P4-41	WRITE FILE MARK (IWFM)	P5-28	P5-27	READY (IRDY)
P4-38	P4-37	EDIT (IEDIT)**	P5-44	P5-43	ON-LINE (IONL)
P4-40	P4-39	ERASE (IERASE)	P5-30	P5-29	REWINDING (IRWD)
P4-44	P4-43	READ THRESHOLD 1 (IRTH1)	P5-32	P5-31	FILE PROTECT (IFPT)
P4-36	P4-35	READ THRESHOLD 2 (IRTH2)	P5-4	P5-5	LOAD POINT (ILDP)
P5-50	P5-49	DENSITY SELECT (IDEN)	P5-22	P5-21	END OF TAPE (IEOT)
P4-20	P4-19	REWIND (IREW)	P5-26	P5-25	NRZI (INRZ)
P5-24	P5-23	OFF-LINE (IOFL)	P4-14	P4-13	SINGLE (ISGL)
P4-4	P4-3	LAST WORD (ILWD)	P5-40	P5-39	SPEED (ISPEED)
P5-18	P5-17	FORMATTER ENABLE (IFEN)	P5-36	P5-35	WRITE STROBE (IWSTR)
P4-22	P4-21	WRITE DATA PARITY (IWP)	P5-34	P5-33	READ STROBE (IRSTR)
P4-10	P4-9	WRITE DATA 0 (IW0)	P5-1	P5-5	READ DATA PARITY (IRP)
P4-12	P4-11	WRITE DATA 1 (IW1)	P5-2	P5-5	READ DATA 0 (IR0)
P4-30	P4-21	WRITE DATA 2 (IW2)	P5-3	P5-5	READ DATA 1 (IR1)
P4-26	P4-25	WRITE DATA 3 (IW3)	P4-48	P4-47	READ DATA 2 (IR2)
P4-6	P4-5	WRITE DATA 4 (IW4)	P4-50	P4-49	READ DATA 3 (IR3)
P4-32	P4-31	WRITE DATA 5 (IW5)	P5-6	P5-5	READ DATA 4 (IR4)
P4-28	P4-27	WRITE DATA 6 (IW6)	P5-20	P5-19	READ DATA 5 (IR5)
P4-24	P4-23	WRITE DATA 7 (IW7)	P5-10	P5-9	READ DATA 6 (IR6)
P4-16	P4-15	LOAD ON LINE (ILOL)	P5-8	P5-7	READ DATA 7 (IR7)
			P5-42	P5-41	CORRECTED ERROR (ICER)

*ICCG and IDENT line shared by NRZI and PE.

**Not applicable to FT1000.

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2.5 DAISY-CHAIN CONNECTIONS

Three 34-lead flat cables (3M 3365-34 or equivalent) are required for the drive daisy-chain interface.

When one, two, or three slave drives are daisy-chained to a master drive, the interconnecting cables may be 12.2 m (40 feet) maximum length. These three cables connect to J11, J12, and J13 of the Cable Adapter (DC) PCBAs when used with the FT7000 series drives. These cables connect to the Interconnect E PCBA when used with FT6000, FT8000, and FT9000 series drives. When used with the FT1000 model, the cables connect to the Interconnect D or D1 PCBA.

To ensure proper operation, terminators are required on the last Cable Adapter PCBA (FT7000) or Interconnect E PCBA (FT6000, FT8000, and FT9000) in a daisy chain. In addition, connector P5 must be disconnected from J5 on the Interconnect E PCBA on all slave drives.

The Cable Adapter (DC) PCBAs are shown in Figure 2-2 and the Interconnect E PCBA is shown in Figure 2-3. When using the microformatter with an FT1000 model, refer to Figure 2-4 and the companion Operating and Service Manual for the description of the Interconnect D or D1 PCBA. The daisy-chain interface is described in Table 2-2.

2.5.1 T7000 DAISY-CHAIN

When connecting the Cable Adapter (DC) PCBAs to a T7000, Cable Adapter I (DC) connects to J101 of the Tape Control PCBA, Cable Adapter II (DC) connects to J102 of the Data PCBA, and Cable Adapter III (DC) connects to J103 of the Data PCBA. Refer to Paragraph 2.5.4 for configurations and to Table 2-3 for details of the cable assembly used for these connections.

The three flat cables referred to in Paragraph 2.5 connect to:

(1) P1 of the Microformatter PCBA and J11 of Cable Adapter II (DC) PCBA.

(2) P2 of the Microformatter PCBA and J12 of Cable Adapter II (DC) PCBA.

(3) P3 of the Microformatter PCBA and J13 of Cable Adapter III (DC) PCBA.

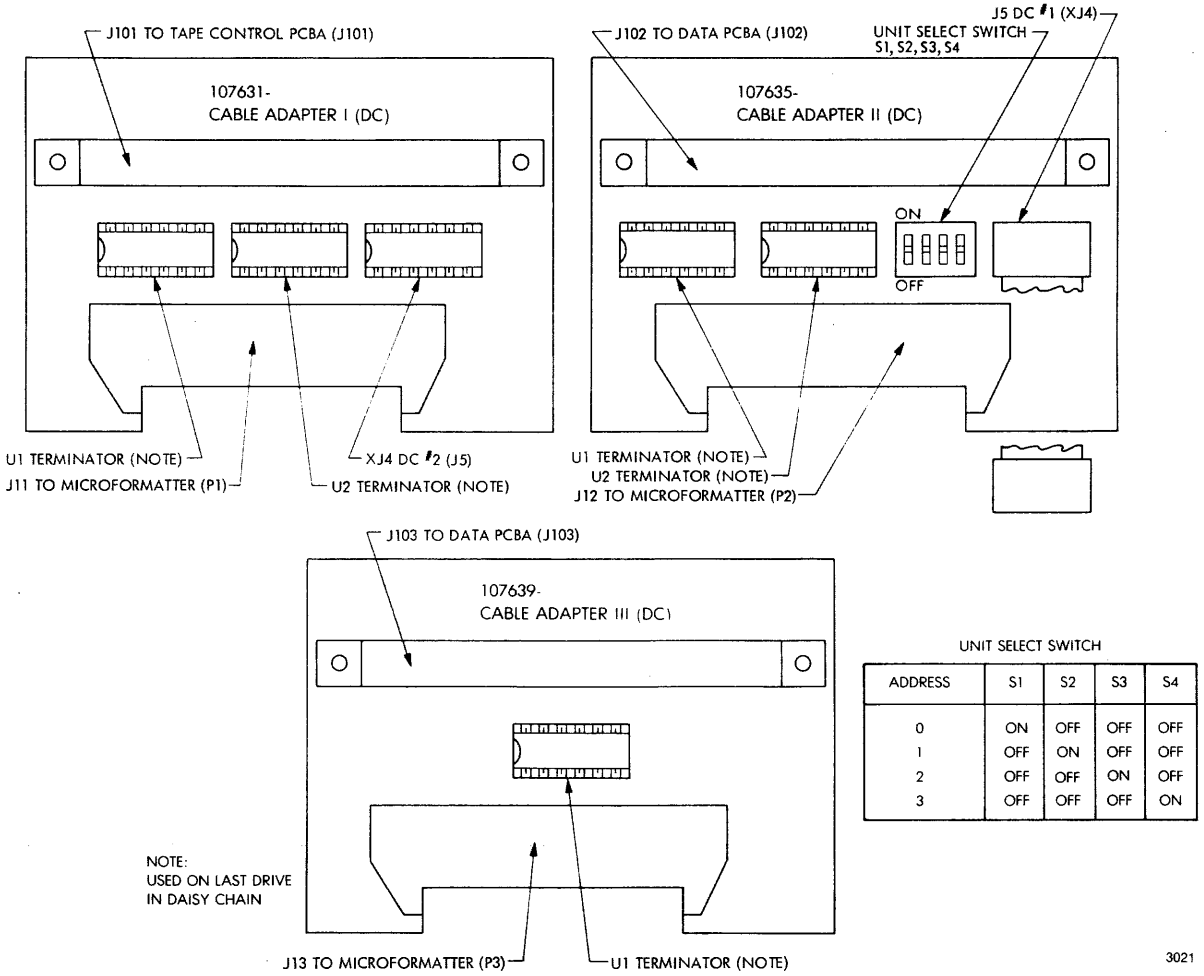
2.5.2 T6000, T8000 OR T9000 DAISY-CHAIN

When connecting the Interconnect E PCBA to a T6000, T8000, or T9000, J101 of the Interconnect E PCBA connects to J101 of the Tape Control PCBA, J102 and J103 of the Interconnect E PCBA connects to J102 and J103 of the Data PCBA, and J1, J2, and J3 of the Interconnect E PCBA connect to P1, P2, and P3 of the Microformatter PCBA. Refer to Paragraph 2.5.4 for configurations.

One end of the three flat cables referred to in Paragraph 2.5 connect to J11, J12, and J13 of the Interconnect E PCBA, the other ends connect to the remaining drives in the daisy-chain. Refer to Table 2-4 for details of the cable assembly used for these connections.

2.5.3 T1000 DAISY-CHAIN

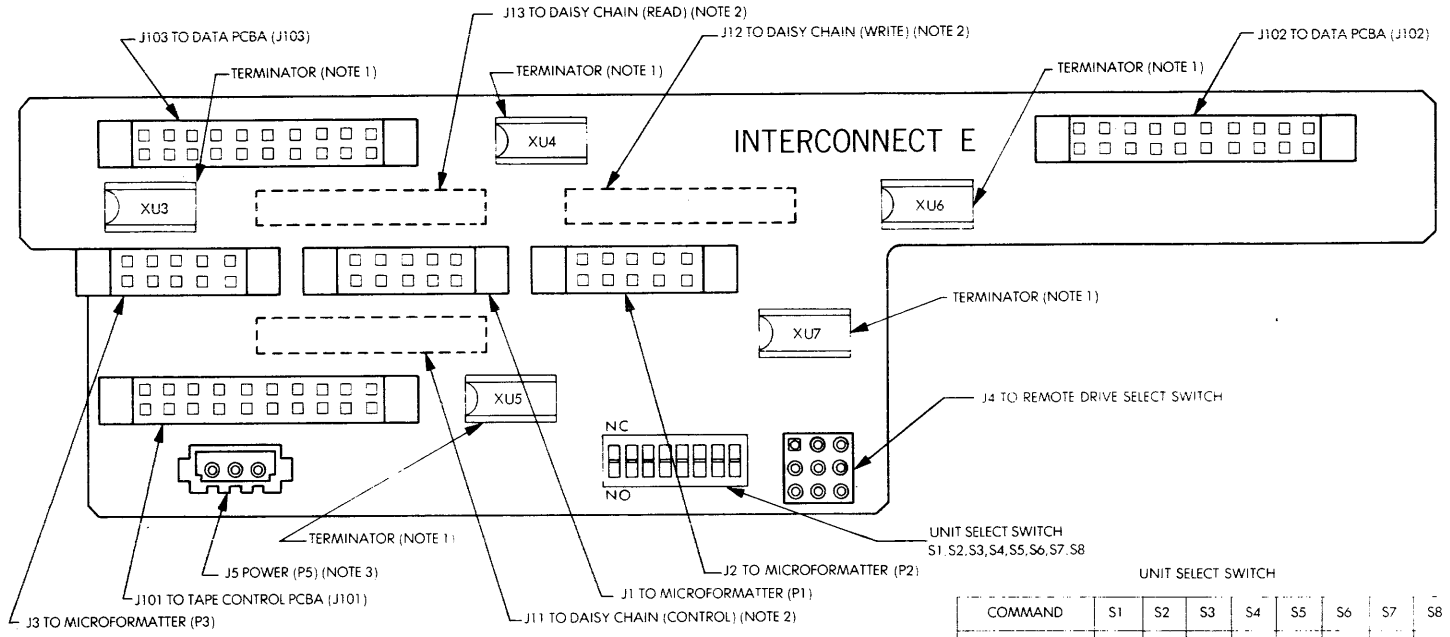
When daisy chaining T1000 Drives, connectors J201, J202, and J203 of the Interconnect D or D1 PCBA are used. Refer to Table 2-4 for details of the cable assembly used for these connections.



UNIT SELECT SWITCH

ADDRESS	S1	S2	S3	S4
0	ON	OFF	OFF	OFF
1	OFF	ON	OFF	OFF
2	OFF	OFF	ON	OFF
3	OFF	OFF	OFF	ON

Figure 2-2. Cable Adapter (DC) PCBAs



NOTES:
1. USED ON LAST DRIVE IN DAISY CHAIN.
2. PHANTOM LINES INDICATE BACK OF BOARD.
3. DISCONNECT P5 FROM J5 ON ALL SLAVE DRIVES.

UNIT SELECT SWITCH

COMMAND	S1	S2	S3	S4	S5	S6	S7	S8
DRIVE 0	NC	NO	NO	NO	NO			
DRIVE 1	NO	NC	NO	NO	NO			
DRIVE 2	NO	NO	NC	NO	NO			
DRIVE 3	NO	NO	NO		NO			
REMOTE SELECT								
NRZI						NC		
PE						NO		
SINGLE HEAD							NC	
DUAL HEAD							NO	
LOW SPEED								NC
HIGH SPEED								NO

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Figure 2-3. Interconnect E PCBA

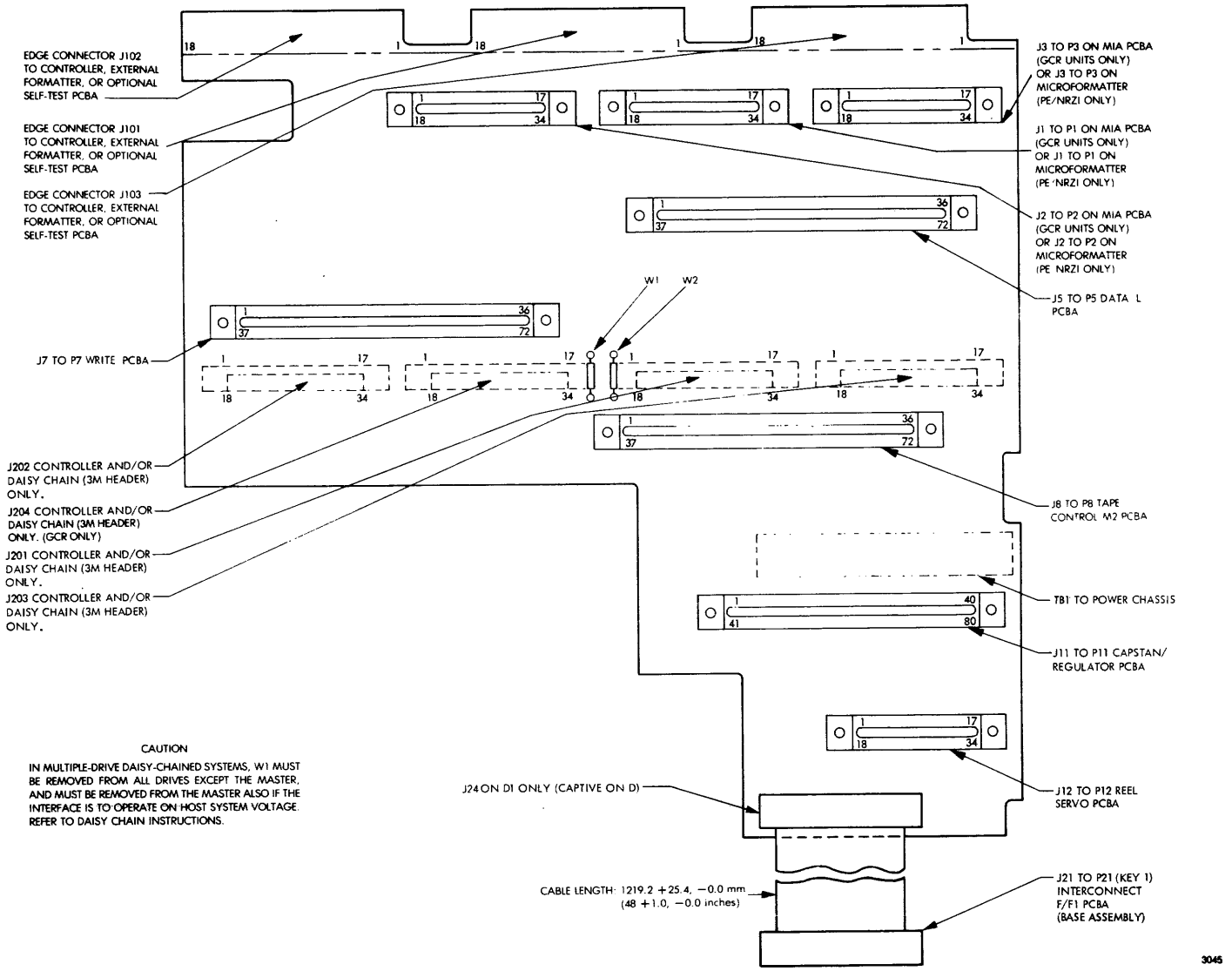

Figure 2-4. Interconnect D1 PCBA

Table 2-2(A)

Control Signals, Drive/Cable Adapter I, Interconnect D or D1, or Interconnect E

Drive J101		Cable Adapter (DCI) J11 or Interconnect E, J11 or FT1000, J201		Signal
Live	Return	Live	Return	
1	2	17	—	LOAD ON LINE (ILOL)
A	8	16	—	WRITE AMPLIFIER RESET #2 (IWARS2)
B	2	15	33	OVERWRITE (IOVW)
C	3	14	32	SYNCHRONOUS FORWARD COMMAND (ISFC)
D	4	13	31	DATA DENSITY SELECT (IDDS)
E	5	12	30	SYNCHRONOUS REVERSE COMMAND (ISRC)
F	6	11	29	DATA DENSITY INDICATOR (IDDI)
H	7	10	28	REWIND COMMAND (IRWC)
K	9	8	26	SET WRITE STATUS (ISWS)
L	10	7	25	OFF-LINE COMMAND (IOFC)/REWIND UNLOAD (IRWU)*
M	11	6	24	ON-LINE (IONL)
N	12	5	23	REWIND (IRWD)
P	13	4	22	FILE PROTECT (IFPT)
R	14	3	21	LOAD POINT (ILDP)
T	16	19	20	READY (IRDY)
U	17	2	34	END OF TAPE (IEOT)
J	8	9	27	SELECT 0 (ISLT0)**
—	—	1	—	POWER SUPPLY ENABLE (IPSEN)

*REWIND UNLOAD applies to FT9000 and FT1000.
**Provided through Select Switch.

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2.5.4 OTHER CONFIGURATIONS

To daisy-chain a Model FT7000 to T7000 models, both the master and slave drives require the Cable Adapter (DC) PCBA, Figure 2-2. In order to daisy-chain a model FT7000 to T6000 and/or T8000 models, the master drive requires the Cable Adapter (DC) PCBAs and the slave drives require an MTA II. Refer to PPC Operating and Service Manual No. 103920 for details of the MTA II.

NOTE

When T7000 drives are daisy-chained, the Cable Adapter (DC) PCBAs must be used.

When daisy-chaining a model FT6000, FT8000, or FT9000 to either T6000, T8000, or T9000 models, the master drive requires an Interconnect E PCBA (see Figure 2-3) and the slave drives require an MTA II.

To daisy-chain the model FT1000 to T1000 models, no adapters are required. When daisy-chaining a model FT1000 to T6000, T8000, or T9000 models, the slave drives require an MTA II.

Units having different tape speeds may be daisy-chained only if the tape speeds are related by a factor of two. For example, a 25 ips machine can be daisy-chained only with another 25 ips unit or a 12.5 ips unit. In any case, the microformatter must be set for the higher of the two speeds.

Table 2-2(B)

Write Signals, Drive/Cable Adapter II, Interconnect D or D1, or Interconnect E

Drive J102		Cable Adapter (DCII) J12 or Interconnect E, J12 or FT1000, J202		Signal
Live	Return	Live	Return	
A	1	34	2	WRITE DATA STROBE (IWDS)
C	3	32	4	WRITE AMPLIFIER RESET (IWARS)
F	6	29	7	READ THRESHOLD 2 (IRTH2)*
L	10	25	11	WRITE DATA PARITY (IWDP)
M	11	24	12	WRITE DATA 0 (IWD0)
N	12	23	13	WRITE DATA 1 (IWD1)
P	13	22	14	WRITE DATA 2 (IWD2)
R	14	21	15	WRITE DATA 3 (IWD3)
S	15	20	16	WRITE DATA 4 (IWD4)
T	16	19	17	WRITE DATA 5 (IWD5)
U	17	18	—	WRITE DATA 6 (IWD6)
V	18	1	—	WRITE DATA 7 (IWD7)
—	—	33	2	SELECT 1 (ISLT1)**
—	—	31	5	SELECT 2 (ISLT2)**
—	—	28	8	SELECT 3 (ISLT3)**
—	—	26	10	TACHOMETER (ITACH)***

*Not applicable to FT7000.
**Provided through Select Switch.
***Applicable to FT9000 and FT1000 only.

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Table 2-2(C)

Read Signals, Drive/Cable Adapter III, Interconnect D or D1, or Interconnect E

Drive J103		Cable Adapter (DCIII) J13 or Interconnect E, J13 or FT1000, J203		Signal
Live	Return	Live	Return	
1	A	34	2	READ DATA PARITY (IRDP)
2	B	33	3	READ DATA STROBE (IRDS)[1]
3	C	32	4	READ DATA 0 (IRD0)
4	D	31	5	READ DATA 1 (IRD1)
8	J	27	7	READ DATA 2 (IRD2)
9	K	26	8	READ DATA 3 (IRD3)
10	L	25	9	NRZI (INRZ)[2]
12	N	23	6	SINGLE (ISGL)[2,3]
13	P	22	14	SPEED (ISPD)[2]
14	R	21	15	READ DATA 4 (IRD4)
15	S	20	16	READ DATA 5 (IRD5)
17	U	18	—	READ DATA 6 (IRD6)
18	V	1	—	READ DATA 7 (IRD7)

NOTES:

1. Relevant to NRZI operation only.
2. Not applicable to FT7000.
3. Not applicable to FT1000.
4. The following pins provide +5v from the microformatter to the dc assemblies.

J11*	J13*	J201/J204**	J203**
18	11, 28 12, 29 13, 30	18	11, 28 12, 29 13, 30

*FT6000, FT7000, FT8000, and FT9000
**FT1000 only.

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Table 2-3

FT7000 Daisy Chain Cable Assemblies

Max. No. of Units	Cable Lengths mm (inches)				Part No.(s) Required
	A*	B**	C**	D**	
1	0.25 (10) 0.43 (17) 0.70 (27.5)				107647-01 107647-02 107647-03
2	0.25 (10) 0.43 (17) 0.70 (27.5)	1.52 (60) 1.52 (60) 1.52 (60)			107647-04***
4	0.25 (10) 0.43 (17) 0.70 (27.5)	1.52 (60) 1.52 (60) 1.52 (60)	3.04 (120) 3.04 (120) 3.04 (120)	1.52 (60) 1.52 (60) 1.52 (60)	107647-04***

*Microformatter to DC PCBAs in first unit.

**DC PCBAs to DC PCBAs.

***Includes the three required cables.

Table 2-4

FT6000/FT8000/FT9000/FT1000
Daisy Chain Cable Assemblies

Max. No. of Units	Cable Lengths m (feet)				Cable Part No.
	A*	B**	C**	D**	
2	1.52 (5)				103936-01
2	3.04 (10)				103936-02
4		1.52 (5)	3.04 (10)	1.52 (5)	103936-03
4		3.04 (10)	3.04 (10)	3.04 (10)	103936-04

SECTION III
OPERATION

3.1 INTRODUCTION

This section contains the basic microformatter operation and a detailed definition of the microformatter to controller interface lines.

3.2 BASIC OPERATION

The microformatter is capable of executing the commands necessary to enable the modes of operation described in the following paragraphs. All commands, with the exception of Rewind, Off Line and Load On Line, are executed by sampling the logic states of the interface lines as given in Table 3-1. Rewind, Off Line, and Load On Line commands are executed directly from the interface without combination.

Refer to Table 3-1 in conjunction with the following command descriptions.

3.2.1 READ FORWARD

The Read Forward command causes tape on the selected unit to be accelerated to the normal drive operating speed. The microformatter reads the first record of data encountered and then decelerates the tape to a stop. The microformatter generates the delays necessary for proper positioning of the drive read head in the Inter-Block Gap (IBG). It is possible to read the next record on tape by supplying a new Read Forward command to the microformatter prior to the completion of the tape deceleration, thereby improving the access time to the next record by as much as one ramp time. This is referred to as *on the fly* operation.

Table 3-1
Microformatter Commands

Command	IREV	IWRT	IWFM	IEDIT*	IERASE
Read Forward	F	F	F	F	F
Read Reverse (Normal)	T	F	F	F	F
Read Reverse (Edit)*	T	F	F	T	F
Write	F	T	F	F	F
Edit*	F	T	F	T	F
Write File Mark	F	T	T	F	F
Erase (Variable Length)	F	T	F	F	T
Erase (Fixed Length)	F	T	T	F	T
Space Forward	F	F	F	F	T
Space Reverse	T	F	F	F	T
File Mark Search Forward	F	F	T	F	F
File Mark Search Reverse	T	F	T	F	F
File Mark Search Forward (Ignore data)	F	F	T	F	T
File Mark Search Reverse (Ignore data)	T	F	T	F	T

NOTES:
1. T = True, F = False
2. *Not applicable to FT1000

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3.2.2 READ REVERSE

The Read Reverse command is similar to a Read Forward command except that tape motion is in the reverse direction. Records may also be read in reverse *on the fly*. During any reverse operation, the microformatter always resets to the quiescent state when the BOT signal is present. A Read Reverse command may be modified to position the head further back in the gap after reading a record. This change in position of the head is to facilitate the editing of a record, and is done by the microformatter in response to an Edit command. Details of the Edit command are contained in Paragraph 3.2.4.

3.2.3 WRITE

When executing a Write command, the microformatter accelerates tape and, after the appropriate pre-record delay time, begins to transfer data from the controller to the drive. The process continues until a LAST WORD (ILWD) is received from the controller. The tape will continue to move forward until the record has been read by the read head, then the tape will be decelerated to a stop with the write head properly located in the center of the IBG. Consecutive records may be written *on the fly*.

3.2.4 EDIT

Edit operations are similar to Write operations except that the write current is switched off slowly at the end of an edit sequence to minimize the possibility of recording a *glitch* on tape. For proper head positioning, Edit commands should be preceded by a Read Reverse (Edit) command.

3.2.5 WRITE FILE MARK

The Write File Mark command causes a file mark to be written on tape; Paragraphs 3.4.6 and 3.5.5 provide details of the Write File Mark command for PE Format and NRZI Format, respectively.

3.2.6 ERASE (VARIABLE LENGTH)

The Erase (Variable Length) command causes tape to be moved in the forward direction with erase current on. An ILWD signal from the controller terminates the erase operation. It should be noted that in the PE mode, the ID burst will not be erased when an Erase command is given from BOT.

3.2.7 ERASE (FIXED LENGTH)

The Erase (Fixed Length) command causes a 102 mm (4 inch) length of tape to be erased. This command is always executed while moving tape in the forward direction.

3.2.8 SPACE FORWARD

The Space Forward command is similar to a Read Forward command except that no READ STROBE (IRSTR) signals are supplied to the controller. Although error checking is not performed, a test is made to determine if the record spaced over was a File Mark.

3.2.9 SPACE REVERSE

The Space Reverse command is similar to a Read Reverse command except that no READ STROBE (IRSTR) signals are supplied to the controller. Although error checking is not performed, a test is made to determine if the record spaced over was a File Mark.

3.2.10 FILE MARK SEARCH FORWARD

A File Mark Search Forward command causes the drive to execute a series of Read Forward commands while in the *on the fly* mode of operation. This series is terminated by the recognition of either a File Mark character or the EOT tab. Tape is stopped following the reading of a File Mark in a manner similar to terminating a normal Read operation. If the EOT tab is encountered during a File Mark Search operation, the operation will terminate and tape will be stopped at the end of the record currently being processed. The File Mark Search Forward command may be combined with a Space Forward command, thereby preventing IRSTR, ICER and IHER signals from being presented at the Microformatter to Controller Interface.

3.2.11 FILE MARK SEARCH REVERSE

The File Mark Search Reverse command causes the drive to execute a series of Read Reverse commands while in the *on the fly* mode of operation. This series is terminated by the recognition of either a File Mark character or the EOT tab. The tape is stopped after reading a File Mark in a manner similar to terminating a normal Read operation. If the EOT tab is encountered during a File Mark Search operation, the operation is terminated and tape will be stopped at the end of the record currently being processed. The File Mark Search Reverse command may be combined with a Space Reverse command, thereby preventing IRSTR, ICER and IHER signals from being presented at the Microformatter to Controller Interface.

3.2.12 REWIND

The Rewind command causes the unit to rewind to BOT. In systems where more than one unit is daisy-chained, it is possible to rewind several drives while transferring data to or from another unit in the chain.

3.2.13 OFF-LINE

The Off-Line command places the drive under local control. Only the selected unit is placed off-line in daisy-chained systems. In some tape drives (e.g., T9000 series), this command causes the tape unit to perform a Rewind/Unload operation.

3.2.14 LOAD-ON-LINE

The Load-On-Line command enables a remote load sequence.

3.3 GAP GENERATION

3.3.1 INTER-BLOCK GAP GENERATION

The microformatter provides timing to generate the necessary 15.2 mm (0.6-inch) gap between data blocks. Longer gaps can be generated by using the Erase command.

3.3.2 INITIAL GAP

When writing in the NRZI format, the first data record is written approximately 89 mm (3.5 inches) down tape from the trailing edge of the BOT tab. In the PE format, the gap follows the ID burst.

3.3.3 FILE MARK GAP

A File Mark will be preceded by a gap of approximately 102 mm (4 inches) of tape and followed by a normal IBG.

3.4 PHASE ENCODED FORMAT

The following features apply only to PE and dual format drives. These models write tapes in accordance with ANSI Specification No. X3.39-1973 for 1600 cpi 9-track recording.

3.4.1 DATA

Phase Encoded (PE) data are characterized as follows.

(1) A 0 bit corresponds to a transition in the middle of the bit cell away from the erase direction of magnetization. When writing, this corresponds to a high-to-low transition at the microformatter output to the drive.

(2) A 1 bit corresponds to a transition in the middle of the bit cell toward the erase direction of magnetization. When writing, this corresponds to a low-to-high transition at the microformatter output to the drive.

(3) In the case of successive 0 bits or successive 1 bits, an additional transition is required at the cell boundary. This transition is referred to as the *phase transition* and is in the opposite direction from that of the *data transition.*

3.4.2 PREAMBLE

The preamble is a burst of forty 0 bits and a 1 bit in all nine tracks at the beginning of each record. When reading, the microformatter tracking circuit uses this burst to synchronize the decoding circuits. The detection of the 1 bit indicates the beginning of the data field.

3.4.3 DATA FIELD

The data field is written with data and phase transitions as defined in Paragraph 3.4.1. The length of the data field may be a minimum of 18 characters and a maximum of 2,048 characters, in accordance with the ANSI specification. The microformatter is capable of writing and reading records of a minimum of three characters. There is no hardware limitation to the maximum number of data characters that may be included in a single data record.

3.4.4 POSTAMBLE

The postamble is comprised of a single 1 bit and a burst of forty 0 bits at the end of the record. The postamble provides a means of synchronization when reading tape in the reverse direction. The microformatter interprets a 1 bit and two consecutive 0 bits in all tracks as being a valid postamble.

3.4.5 PARITY

When writing, the data in the parity data track are generated by the microformatter in such a way as to provide odd parity for all characters in the data field. An external parity generator may also be used.

3.4.6 FILE MARK

When a Write File Mark command is executed, the microformatter generates the file mark gap and then generates a File Mark consisting of 256 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6, and 7. Channels 1, 3, and 4, are dc-erased.

When reading, the microformatter will recognize a File Mark if there are at least 64 flux reversals in Channels 2, 6, and 7 with Channels 1, 3, and 4 dc-erased. Channels P, 0, and 5 are ignored for this test.

3.4.7 IDENTIFICATION BURST

When performing a Write command from BOT, the microformatter writes an ANSI and IBM compatible identification (ID) burst consisting of a sequence of 1600 frpi flux reversals in Channel P, with all other tracks dc-erased. To write this ID Burst properly, a Write command from BOT should not be preceded by any Reverse command except Rewind.

In the Read mode, the microformatter samples the output of Channel P as the BOT tab traverses the read head. If an ID burst is detected, the IDENT interface line is pulsed.

3.4.8 DROPOUT AND ERROR CORRECTION

A dropout is detected by the microformatter for a particular track if no data are present on that track for more than one and one-fourth bit cell times. This test is made after approximately twenty 0 bits of the preamble have been read in each track. If only one of the nine tracks has a dropout detected in the microformatter, the microformatter will correct this track by using the odd parity nature of the data in conjunction with the single track dropout indication.

If a dropout of more than one track is indicated by the microformatter, data are invalid and the command is immediately terminated. Tape motion is not stopped until the end of the record is found.

3.4.9 DESKEW OF READ DATA

As data are read from tape, the data transitions corresponding to bits of a specific character may arrive at the microformatter at different times, due to the skewed relationship of the nine data tracks. Data may be skewed as much as 2.9 characters and still be deskewed properly to be presented at the controller interface.

3.4.10 ERROR DETECTION

If the data read back from the tape shows even parity for a particular data character with no track dropout indication, an error indication is provided during the transfer of that specific character to the controller. The command is not aborted. The microformatter continues execution of the current command, provided that none of the following errors occur. If one of these errors is detected, the command is aborted and the microformatter will search for the IBG.

(1) A 1 bit is detected in either the preamble or postamble.

(2) An overflow condition is detected in the deskew buffer, indicating excessive tape skew, i.e., greater than 2.9 characters.

(3) One or more channels fails to detect the 1 bit at the end of the preamble.

(4) A false postamble is detected in the middle of the record.

(5) A dropout indication is generated for two or more channels.

3.4.11 TRACKING OSCILLATOR

When reading PE data, a tracking oscillator is used to decode data. This oscillator follows the long-term and short-term speed variation of the data being read. The characteristics of the oscillator are such that any PE tape that complies with the ANSI specification may be read by any PPC Microformatter/Drive PE tape system.

3.4.12 RECORD RECOGNITION

When a Read command is given to the microformatter, tape is ramped up to nominal speed and the microformatter searches for the preamble of a data record. Channels 2, 0, 4, and 5 inclusive are monitored. A valid preamble is declared if data are present on Channels 2, 0, 4, or 5 inclusive continuously for 10 character times.

If data are present on Channels 2, 0, 4, or 5 continuously for a time period less than 10 character times, the microformatter will assume that the few data pulses received were due to erroneous flux transitions occurring prior to the actual data record, and the microformatter will continue to search for the data record.

Once a valid record has been recognized at 10 character times into the preamble, any loss of data (as determined from Channels 2, 0, 4, and 5) results in the microformatter stopping tape motion. This is due to either the loss of data in these four channels or the valid end of the data record. The data loss must be continuous for greater than 22 character times for tape motion to stop.

3.5 NRZI FORMAT

The following NRZI Format description applies to all NRZI and dual format models. The data format described is consistent with ANSI Specification X3.22-1973 for 9-track, 800 cpi NRZI recording.

3.5.1 DATA

NRZI data are characterized as follows.

(1) A 1 bit corresponds to a flux transition in the center of the bit cell on tape. This corresponds to a logic true (1) on the WRITE DATA interface line to the drive during a Write operation.

(2) A 0 bit corresponds to a lack of any flux transition on tape or a logic false (0) on the WRITE DATA interface line to the drive during a Write operation.

3.5.2 DATA RECORD

A record of NRZI data may contain between 18 and 2048 ASCII characters. This is in accordance with the ANSI specification for 800 cpi 9-track recording. The microformatter is capable of writing and reading records of a minimum of three characters. There is no hardware limitation to the maximum number of data characters that may be included in a record. Channel P on tape is written to provide odd parity for all data characters. Nominal spacing between characters is 31.75 micrometers (1250 microinches).

3.5.3 CYCLIC REDUNDANCY CHECK CHARACTER

The Cyclic Redundancy Check Character (CRCC) is written on tape after a four character delay from the last data character. The CRCC is generated in accordance with the ANSI specification for 800 cpi NRZI magnetic tape recording.

3.5.4 LONGITUDINAL REDUNDANCY CHECK CHARACTER

The Longitudinal Redundancy Check Character (LRCC) is written on tape after a four character delay from the CRCC. The data in this character is such that the total number of 1 bits in a track (including the CRCC and LRCC) is even. The LRCC will never be an all-0s character. The LRCC is generated by the reset of the write register in the tape drive. The LRCC also serves to set the tape magnetization in the proper direction for IBG.

3.5.5 FILE MARK

When executing a Write File Mark command, the microformatter generates a one-character record. This single data character consists of a 1 bit in Channels 3, 6, and 7 and a 0 bit in all other channels. The CRCC contains all 0s. The LRCC is equivalent to the single data character.

The microformatter tests for the presence of the file mark pattern during every Read operation. When this is detected, the IFMK interface line to the controller is pulsed and the file mark characters are transmitted to the controller.

3.5.6 ERROR DETECTION

In the NRZI format, all deskewing functions during a Read operation are performed in the tape drive. The microformatter receives a nine-bit word from the drive and relays this word to the customer's controller. A HARD ERROR (IHER) is generated by the microformatter if any of the following read errors occur.

(1) A data character is read from tape containing even parity.

(2) A CRCC is read from tape containing even parity and the record contains an even number of data characters.

(3) A CRCC is read from tape containing odd parity and the record contains an odd number of data characters.

(4) Longitudinal parity on any track is odd.

(5) A track dropout occurs in such a way as to cause more than two check characters, i.e., CRCC and LRCC, to be detected when the microformatter interprets the dropout as an end-of-record condition.

It should be noted that all of the foregoing errors except (5) are checked during both Read Forward and Read Reverse operations. The error described in (5) is checked only during Read Forward operations.

3.6 CONTROLLER-TO-MICROFORMATTER INTERFACE

3.6.1 FORMATTER ADDRESS (IFAD)

This is a level which selects one of the two possible microformatters attached to the controller to microformatter interface.

False = Address 0

True = Address 1

The microformatter's address is predetermined by a switch on the Microformatter PCBA.

When selected, a microformatter is connected to the controller and all controller to microformatter interface lines are activated. Unless otherwise noted, the description of all other controller to microformatter lines will assume that the microformatter is selected.

3.6.2 TRANSPORT ADDRESS (ITAD0, ITAD1)

The levels on these two lines select one of the four units which may be daisy-chained to the microformatter. These lines are decoded by the microformatter and transmitted to the microformatter to drive interface as follows.

ITAD0	ITAD1	Address
False	False	ISLT0
False	True	ISLT1
True	False	ISLT2
True	True	ISLT3

3.6.3 INITIATE COMMAND (IGO)

This pulse initiates the commands given in Table 3-1. On the trailing edge of IGO, the command lines described in Paragraphs 3.5.4—3.6.8 are copied into the microformatter and the FORMATTER BUSY signal (IFBY) is set low. IFBY is described in Paragraph 3.7.1.

3.6.4 REVERSE/FORWARD (IREV)

This signal specifies forward or reverse tape motion.

True = Reverse

False = Forward

3.6.5 WRITE/READ (IWRT)

This signal specifies the operation mode of the system.

True = Write

False = Read

3.6.6 WRITE FILE MARK (IWFM)

This pulse causes a Write File Mark to be written on the tape, if IWRT is also low during this time.

3.6.7 EDIT (IEDIT)

The EDIT signal is employed in two ways:

(1) Read reverse. Modifies the read reverse stop delay to optimize head positioning when editing tapes.

(2) Write. The drive write current is turned off gradually at the end of the record, thus preventing an adjacent data record from being erased.

3.6.8 ERASE (IERASE)

When the IERASE and IWRT signals are low, the microformatter is conditioned to perform a dummy Write command. The microformatter goes through all the functions of a normal Write operation except that no data are recorded. A length of tape is erased equivalent to the length of the dummy record as defined by LAST WORD (ILWD) Paragraph 3.6.14.

Alternatively, if the IERASE, IWRT, and IWFM signals are low, the microformatter is conditioned to perform a dummy Write File Mark operation. A fixed length of tape of approximately 102 mm (4 inches) is erased.

The IERASE signal is also used to inhibit READ STROBE (IRST) during a space operation (Space Forward or Space Reverse) (NSPC) or File Mark Search operation.

3.6.9 READ THRESHOLD LEVEL 2 (ITHR2)

This signal is used on units having a low read threshold capability and is normally made true only when it is required to recover low amplitude data.

True = Low Threshold

False = Normal Threshold

3.6.10 DENSITY SELECT (IDEN)

The IDEN signal is used only when dual format microformatters are used in conjunction with drives equipped with PE or NRZI format selection capability. The state of this line is loaded into the microformatter with each INITIATE COMMAND (IGO).

True = 800 cpi (NRZI)

False = 1600 cpi (PE)

3.6.11 REWIND (IREW)

IREW is a pulse which causes the selected drive to rewind to Load Point, providing the unit is Ready and On-Line. The pulse is routed directly to the drive and does not cause the microformatter to become busy.

3.6.12 OFF-LINE (IOFL)

This pulse causes the selected drive to be placed in the Off-Line mode of operation. IOFL is routed directly to the drive and does not cause the microformatter to become busy.

3.6.13 LAST WORD (ILWD)

During the execution of a Write command or an Erase (Variable Length) command, this pulse is used to indicate that the next character to be strobed into the microformatter is the last character of the record. The line will be set low by the controller at the time the last data character is set on the interface lines.

3.6.14 FORMATTER ENABLE (IFEN)

This is a level which, when high, causes the microformatter to reset to the quiescent state. The signal is not gated by IFAD, hence, if two microformatters are connected to the interface, both will be simultaneously reset.

This line may be used to disable the microformatter if the controller power is lost, or, to clear the microformatter logic.

3.6.15 WRITE DATA LINES (IW0—7)

These eight lines transmit write data from the controller to the microformatter. The eight data bits appearing on WRITE DATA LINES (IW0—7) are written onto the corresponding channels on tape. IW7 corresponds to the least significant bit of the character.

The first character of the data record should be available on these lines within one character period after IDBY goes true and should remain true until the trailing edge of the first IWSTR pulse issued by the microformatter. The next character of information must then be set up in less than half a character period. Subsequent characters will be processed in this way until ILWD is set low, indicating that the last character is being transferred. Table 3-2 identifies these lines with regard to interface identification, ANSI Track Number and binary weight.

3.6.16 WRITE DATA PARITY (IWP)

This line is used only when the external parity generation option is used. This option requires the customer to generate odd parity on the eight data lines (IW0—7) and apply this parity bit to IWP. Setup timing requirements for this line are consistent with requirements for IW0—7. This line is ANSI track number 4.

Table 3-2
Write Data Line Identification

Interface Line	ANSI Track Number	Binary Weight
W0	7	2^7
W1	6	2^6
W2	5	2^5
W3	3	2^4
W4	9	2^3
W5	1	2^2
W6	8	2^1
W7	2	2^0

3.6.17 LOAD-ON-LINE COMMAND (ILOL) (Optional)

The ILOL pulse, when low (1 second minimum width), can be given at any time after ac power is applied to the drive. Tape is tensioned after the first ILOL pulse. When a second ILOL pulse (1 microsecond minimum duration) is given, the drive goes into an On-Line mode. The two pulses must be separated by at least 1 microsecond.

3.7 MICROFORMATTER-TO-CONTROLLER INTERFACE

3.7.1 FORMATTER BUSY (IFBY)

When a command is issued to the microformatter, FORMATTER BUSY (IFBY) goes low at the trailing edge of IGO and remains low until tape motion ceases after execution of the command. This signal may be used by the controller to inhibit further commands.

3.7.2 DATA BUSY (IDBY)

The IDBY signal goes low when the drive has reached operating speed, traversed the IBG, and the microformatter is about to write data on the tape or read data from the tape. IDBY remains low until the data transfer is finished and the appropriate post-record delay completed. IDBY goes high at the same time that the capstan starts to decelerate the tape. A new command may be given when IDBY goes high for an *on the fly* operation. *On the fly* commands must be of the same Read/Write mode and the same tape direction.

3.7.3 CHECK CHARACTER GATE (ICCG) — IDENTIFICATION (IDENT)

This interface line is shared by NRZI and PE Formats. In the NRZI format, the signal is ICCG and is set low by the microformatter when the read information currently being transmitted to the controller is either a CRCC or an LRCC. The signal is high when data characters are being transmitted. Data and check information can be distinguished by gating READ STROBE (IRSTR) with ICCG or its inverse.

In the PE format, the signal on this line is IDENT. The line is pulsed when an ID burst is read from the tape.

3.7.4 HARD ERROR (IHER)

The IHER signal is set low if a read error is detected by the microformatter. Read errors are defined in Paragraphs 3.4.10 and 3.5.6 for PE format and NRZI Format respectively.

All error information is reported to the controller before DATA BUSY (IDBY) goes high.

3.7.5 CORRECTED ERROR (ICER)

The CORRECTED ERROR signal (ICER) is used only in the PE mode. It is set low by a single track dropout during a Read or Read-After-Write operation. ICER in a Read-After-Write operation indicates that the record should be rewritten.

3.7.6 FILE MARK (IFMK)

This is a pulse which indicates that the microformatter read logic has detected a File Mark. This may be during execution of any Read Forward or Read Reverse operation, or during a Write File Mark operation for a read-after-write drive.

3.7.7 DRIVE STATUS AND CONFIGURATION LINES

Status: IRDY, IONL, IRWD, IFPT, ILDP, IEOT
Configuration: INRZ, ISPEED

These lines are used to indicate the status and configuration of the selected drive and are defined exactly the same as in the drive-to-microformatter interface description, except that they have also been gated with the FORMATTER ADDRESS LINE (IFAD). Refer to companion Operating and Service Manual (Section III) for these definitions.

3.7.8 WRITE STROBE (IWSTR)

The IWSTR line is pulsed for each data character to be written on tape. The pulsewidth of IWSTR is approximately 25 percent of a character time. IWSTR samples the WRITE DATA lines (IWP, IW0—7) from the controller and copies this information, character by character, into the microformatter write logic.

The first character must be available before the first IWSTR is issued, and succeeding characters must be set up within half a character period ofter the trailing edge of each IWSTR pulse.

This line is also active during Erase (Variable Length) commands; however, the data being copied into the microformatter will not be written on tape.

For a Write File Mark or Erase (Fixed Length) command, the required pattern is generated internally by the microformatter and IWSTR is not used.

3.7.9 READ STROBE (IRSTR)

The READ STROBE line (IRSTR) is pulsed for each character of read information (data, CRCC, and LRCC) to be transmitted to the controller. IRSTR is used to sample the READ DATA lines (IRP, IR0—7).

The transmission of check characters (CRCC and LRCC) is flagged by the CHECK CHARACTER GATE line (ICCG) as described in Paragraph 3.7.3 and in the event of an all 0s character, an IRSTR pulse is provided.

Note that although the average time between adjacent IRSTR pulses is 1/BV where

B = packing density

V = tape velocity

this time may vary considerably due to the combined effects of bit crowding and skew. The minimum time between adjacent pulses in one-half character period.

3.7.10 READ DATA LINES (IRP, IR0—7)

These nine lines transmit read data from the microformatter to the controller. Each character read from the tape is available by sampling IRP, IR0—7 in parallel by IRSTR.

Data remains set on IRP, IR0—7 for a full character period. The corresponding IRSTR pulse is placed centrally during the time that data are available.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

A microformatted drive system (FT) consists of one or more tape drives, a Microformatter PCBA, and a Power Supply II PCBA. This section provides a block diagram description and the theory of operation of the microformatter. Also presented are methods of fault isolation and maintenance procedures.

NOTE

An FT1000 system does not require the Power Supply II PCBA.

Figure 4-1* is a block diagram of a Dual Microformatter and should be referred to in conjunction with the following paragraphs. It is important to note that the functional discussion of the block diagram is addressed to dual operation of the microformatter and individual NRZI and PE operations are discussed as subsets of the dual operation.

4.2 BASIC CONFIGURATION AND OPERATION

The microformatter may be configured as NRZI only, PE only, or Dual (both NRZI and PE).

Referring to Figure 4-1, it can be seen that the NRZI section contains the Clock Generator, Interface Logic, Master Control, NRZI Read Control, NRZI Read Logic, Error Gating Logic, Read Strobe Gating Logic, Input Read Logic, Output Read Logic and Write Data Generator.

Similarly, it can be seen that the PE section contains the Clock Generator, Interface Logic, Master Control, PE Read Control, Tracking Oscillator, PE Read Logic, Error Gating Logic, Read Strobe Gating Logic, Input Read Logic, Output Read Logic and Write Data Generator.

The microformatter must be selected to operate. Selection is according to the FORMATTER ADDRESS line (IFAD) and the settings of U112-S3 and S4 (refer to Table 4-1).

The microformatter logic must be conditioned according to the type of drive, i.e., PE, NRZI, or Dual. The drive must be selected by the switch settings on the Cable Adapter PCBA (DC) (FT7000 series), Interconnect E PCBA (FT6000, FT8000, and FT9000 series), or the Select Switch on the FT1000 series.

Additionally, if the drives are daisy-chained, U112-S5 and S6 must be set. Table 4-2 describes the method of format selection.

The drive status lines are received by the Interface Logic and coupled to the Master Control. The Interface Logic transmits these signals to the controller.

The SPEED signal is coupled through the Interface Logic and into the Clock Generator.

The Clock Generator controls all the timing within the microformatter for both NRZI and PE operation. The clock frequency is dependent on the tape speed and is programmed by the setting of U187 (Frequency Select). When SPEED is high, the output of the Clock Generator (WCLK and NWCLK) is divided by two. These clocks are applied to the Master Control, the Write Data Generator, and the NRZI Read Control.

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*Foldout drawing, see end of section.

Table 4-1

Formatter Address (U112)

Formatter Address	S3	S4
0	Down	Up
1	Up	Down

Table 4-2

Format Select (U112)

Switch	Format	Model FT7000	Models FT6000, FT8000, FT9000, FT1000
Format S5	PE	Up	Up
	NRZI	Down	Up
	Dual	Up	Up
Head S6	Dual	Up	Up

The Master Control receives signals from the Interface Logic via status and command lines and conditions the microprogram on Read Only Memory (ROM) chips. The Master Control provides the required control for both NRZI and PE Write and Read Logic. The Write signal (WRT) input to the Control logic determines whether the microprogram selects a Write operation or a Read operation.

When the Master Control receives a GO1 signal from the Interface Logic, the status and command lines set the Master Control. Formatter Busy (FBY) is set at this time. Data Busy (DBY) is set when the microformatter is processing data (write or read).

When WRT is high, the Master Control microprogram selects a Write operation. The coding of the Write Commands (WCN0, WCN1, WCN2) determines the type of data to be written. Also, Load Write Data (LDWRTDATA), Load Cyclic Redundancy Character (LDCRC) are provided to the Write Data Generator. Write Strobe (WSTR) is provided to the Interface Logic.

When WRT is low, the Master Control microprogram selects a Read operation. The state of the REVERSE command (IREV) determines if the Read operation is to be executed in a forward or reverse direction.

When in the PE mode, the LAST WORD (ILWD) sets a jump condition and a postamble is written.

4.3 WRITE OPERATION

The Write Data Generator receives and buffers Write signals (IWP, IW0—7) from the controller and transmits them to the drive (IWDP, IWD0—7). The WRITE PARITY signal (IWP) may be selected either internally or externally by setting U112-S1 and S2 (refer to Table 4-3).

Table 4-3
Parity Select (U112)

PARITY	S1	S2
Internal	Up	Down
External	Down	Up

4.3.1 NRZI WRITE OPERATION

Figure 4-2 is a timing diagram for a NRZI Write operation and should be referred to in conjunction with Figure 4-1. The Write Data Generator is enabled when DBY is high. The Write Data Generator transfers data when LDWRTDATA is high. WCN0, WCN1, WCN2 determine the type of data to be written.

After one character time, the first byte of data is coupled to the drive data lines. At the end of the character period, the WRITE DATA STROBE (IWDS) line is pulsed which transfers the byte of data to the selected tape unit. The drive encodes the data into NRZI form and writes it on the tape.

The data are also transferred into a CRC register and the register generates the CRCC, which is written on the tape after the end of the record.

At the end of the character period, a WRITE STROBE (IWSTR) pulse informs the controller that processing of this character is complete and that a new byte is required. The controller must set the new byte on IWP, IW0—7 within one-half character period after the trailing edge of IWSTR.

Subsequent characters are processed in this manner until the controller sets LAST WORD (ILWD) low, indicating that the last bit is being transmitted. Following the IWSTR pulse, the Write Data Generator starts a termination sequence and causes the CRCC and/or LRCC to be written on the tape.

The contents of the CRC register are coupled to the drive during the fourth character period after the last data bit is written. An additional IWDS pulse causes the information to be written on the tape. Four character periods later, the WRITE AMPLIFIER RESET (IWARS) line is pulsed, which resets the drive write register and causes the LRCC to be written on the tape.

After the LRCC is written, a post-record delay is entered. The post-record delay is initiated when the microformatter Read Logic completes a read-after-write check on the data. An internal signal, End NRZI (RENDNZ), indicates the end of the Read-After-Write operation.

The Erase (Variable Length) command is a dummy Write File Mark (WFM) command. A fixed length of tape is erased (approximately 102 mm [4 inches]).

The NRZI format requires that the first record appearing on tape be placed approximately 127 mm (5 inches) past the BOT marker. To accomplish this, the microformatter generates an extra long pre-record delay when a Write command is issued at BOT.

A File Mark consists of a single character record having 1 bits in Channels 3, 6, and 7 for both the data character and the LRCC. The CRCC contains all 0s. This record is separated from the previous record by approximately 102 mm (4 inches) and by a normal IBG of 15.2 mm (0.6 inch) from the following record.

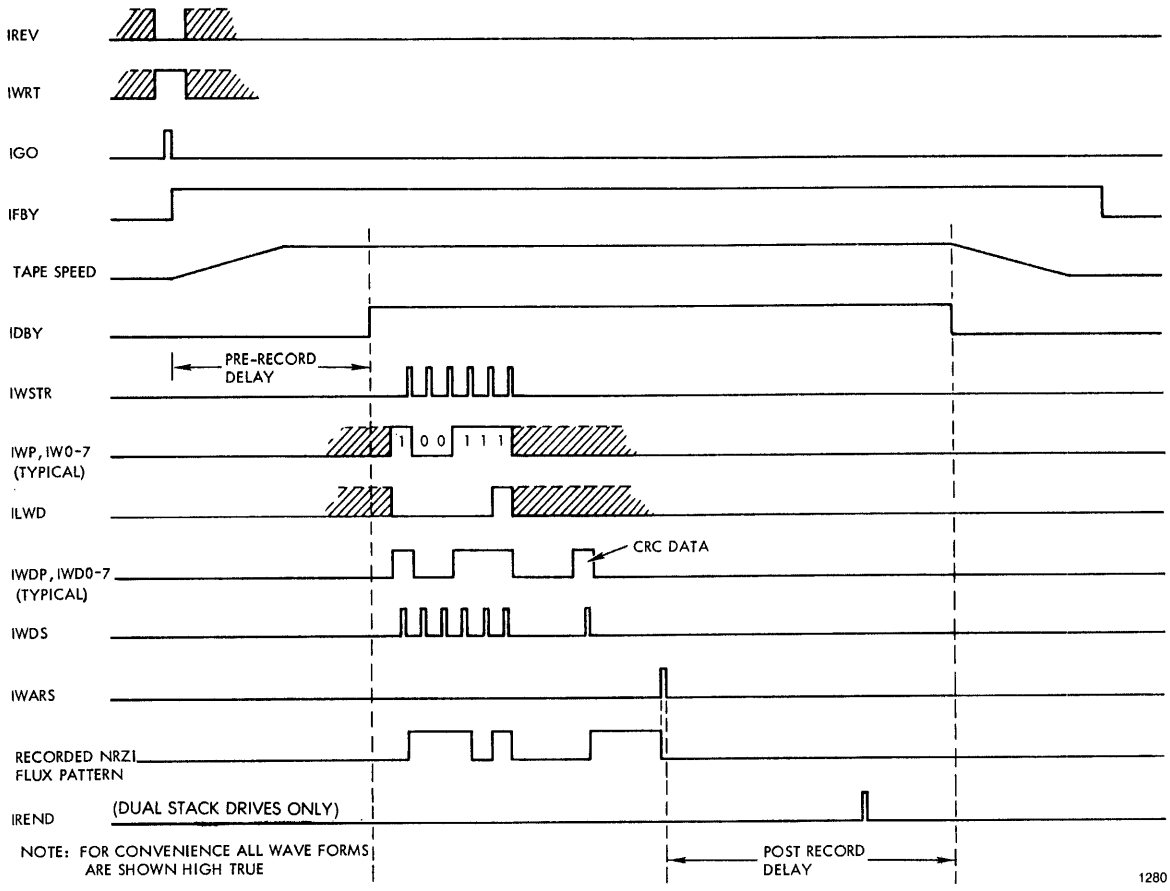


Figure 4-2. 9-Channel NRZI Write Operation

4.3.2 PE WRITE OPERATION

Figure 4-3 is a timing diagram of a PE Write operation. The Write Data Generator is enabled when DBY is high, and transfers data when LDWRTDATA is high. WCN0, WCN1, WCN2 determine the type of data to be written.

When DBY goes high, the microformatter generates a preamble data pattern consisting of forty 0 bits followed by a 1 bit. This pattern is phase encoded and written on the nine data channels on the tape.

During the time period in which the last preamble 1 bit is being recorded, an IWSTR pulse is sent to the controller. On the trailing edge of IWSTR, the data appearing on IWP, IW0—7 is transferred to the microformatter, encoded, and then written on the tape immediately following the preamble 1 bit.

The controller uses the trailing edge of the IWSTR pulse to set the next byte of data on IWP, IW0—7. The microformatter requires the first bit be set on the data lines before the first IWSTR is sent and the subsequent bits are set within one-half of a character period after the trailing edge of IWSTR.

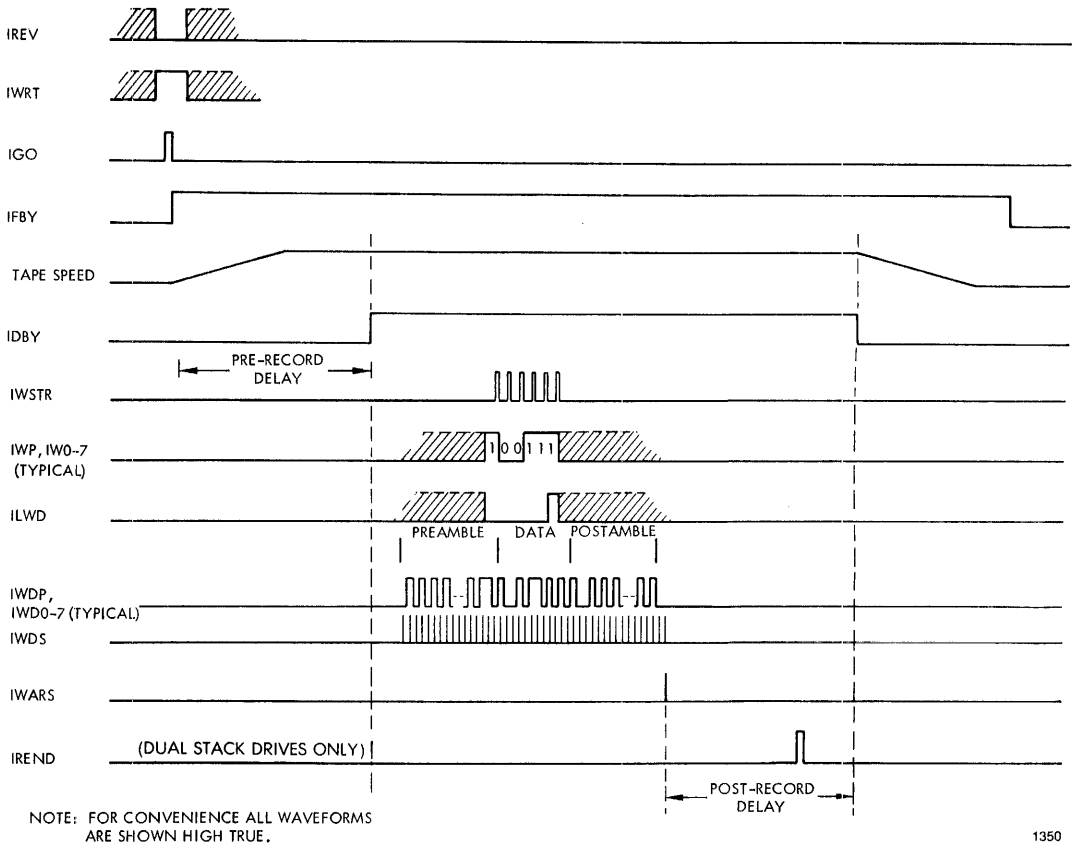


Figure 4-3. 9-Channel PE Write Operation

The controller sets ILWD low when the last data byte is set on IWP, IW0—7. When the following IWSTR pulse occurs, the microformatter samples ILWD and then enters a postamble sequence immediately following the writing of the last data byte.

The postamble pattern is a mirror image of the preamble and consists of a 1 bit followed by forty 0 bits. The postamble is phase encoded and written simultaneously on the nine tape tracks.

Shortly after the last postamble bit is recorded, a WRITE AMPLIFIER RESET (IWARS) pulse is issued by the microformatter. In some models, the IWARS pulse is used to control write current turn-off at the end of an Edit operation.

The post-record delay is initiated after the drive read electronics have completed a read-after-write check on the data just recorded. An internal signal, RENDPE, is used to indicate the end of the Read-After-Write operation.

The 1600 cpi PE format requires identification by a burst of alternate 1s and 0s at the BOT marker. It also requires the first record be written approximately 127 mm (5 inches) after the marker.

When writing from BOT, the microformatter generates an extra long pre-record delay. In a suitable time interval during the delay, the PE identification burst, consisting of a pattern of alternate 1s and 0s (1 0 1 0 1 0 1 0), is written in the Parity Channel. All other channels are erased.

After completion of the pre-record delay, the tape is positioned approximately 127 mm (5 inches) past the BOT marker and the first record is written.

A File Mark record consists of 256 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6, and 7. Channels 1, 3, and 4 are dc-erased. The File Mark is separated from the preceding record by approximately 102 mm (4 inches) and from the following record by a nominal IBG of 15.2 mm (0.6 inch).

The microformatter generates a long pre-record delay equivalent to a 95 mm (3.75-inch) IBG. The Write logic then generates and encodes 128 preamble 0 bits and records this on Channels P, 0, 2, 5, 6, and 7. This pattern is equivalent to 256 flux reversals at 3200 frpi.

At the completion of the Write File Mark operation, the command is terminated the same as other Write operations.

The Erase (Variable Length) is a dummy Write command used to erase any length of tape. This operation is useful in applications which require the ability to erase individual records on a previously recorded tape.

When executing the Erase (Variable Length) command, the microformatter performs all operations of a normal Write command except that the dummy data being transmitted from the controller to the microformatter is not recorded. Therefore, a length of tape equivalent to the dummy record is erased. The ILWD signal determines the record length, in the manner previously described.

The Erase (Fixed Length) command is a dummy Write File Mark command. When enabled, a fixed length of tape (approximately 102 mm [4 inches]) is erased.

4.4 READ OPERATION

Referring to Figure 4-1, it can be seen that there are two Read Logic sections of the microformatter, NRZI Read Logic and PE Read Logic. The NRZI section consists of the NRZI Read Control and the NRZI Read Logic. The PE section consists of the Tracking Oscillator, PE Read Control, and the PE Read Logic.

The Input Read Logic, Output Read Logic, Error Gating Logic and Read Strobe Gating Logic are common to both NRZI and PE Read operations. A Read operation is enabled by GO1.

Incoming Read data are routed through the Input Read Logic, buffered and supplied to either the NRZI Read Logic or the PE Read Logic.

Outgoing Read data are routed through the Output Read Logic from either the NRZI Read Logic or the PE Read Logic. The data are buffered and transmitted to the controller.

The Error Gating Logic and the Read Strobe Gating Logic are discussed within the NRZI and PE Read operations (Paragraphs 4.4.1 and 4.4.2).

4.4.1 NRZI READ OPERATION

The NRZI Read operation is enabled when the NRZ signal is high and WRT signal is low to the Master Control from the Interface Logic. The microprogram in the Master Control sets the NRZI Read Gate signal (RGATENZ1 and RGATENZ2) high. Refer to Figure 4-4.

The microformatter reads data either in the forward or reverse direction, depending on the state of REV1.

The Read data are received and buffered by the Input Read Logic and coupled to the NRZI Read Logic.

The RGATENZ inputs and the Read Strobe (RDS) input to the NRZI Read Control enables the NRZI Read Strobe (RSTRNZ) and forces Not Clear NRZI Data (NCLRNZDATA) high. The NCLRNZDATA signal enables the NRZI Read Logic. The Buffered Read signals and the Read Data Strobe (IRDS) from the drive provide RDS and the nine channels of Read Data (RDNZP—7), which are coupled to the Output Read Logic and the NRZI Read Control. The Output Read Logic buffers and transmits the data to the controller.

The RDNZP—7 signals fed back to the NRZI Read Control provide the following information.

(1) File Mark detection and the File Mark character (FNKNZ) are supplied to the Interface Logic and to the Master Control.

(2) LRCC and CRCC detection (CCG) is supplied to the Interface Logic.

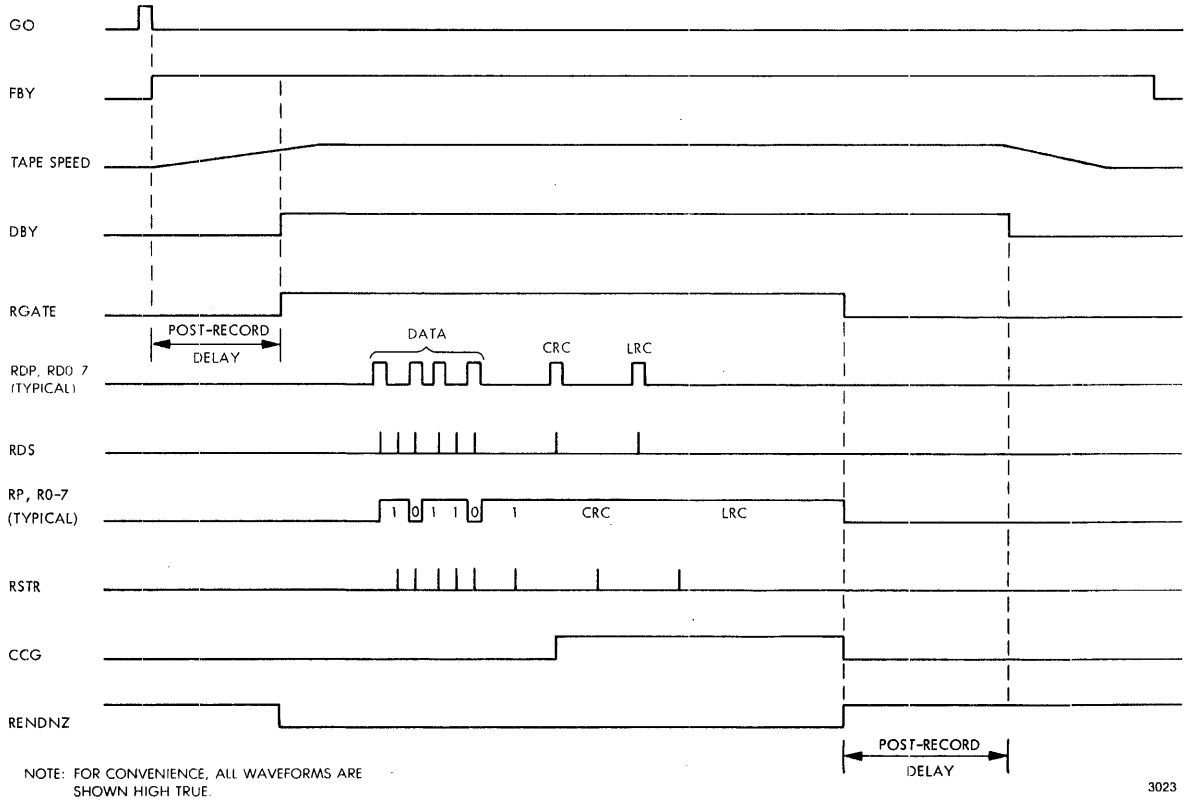


Figure 4-4. NRZI Read Operation

(3) Error information (HERNZ) is supplied to the Error Gating Logic.

(4) End of data (RENDNZ) is supplied to the Master Control.

The HERNZ signal is supplied to the Error Gating Logic, buffered, and transmitted to the controller as HARD ERROR (IHER).

RENDNZ is fed back to the Master Control and disables the RGATENZ signals. The low RGATENZ signals disable RSTR and sets NCLRNZDATA low. NCLRNZDATA clears the NRZI Read Logic and the Read operation is complete.

If a Space Forward or Reverse (NSPC) is commanded, the Error Gating Logic and the Read Strobe Gating Logic are disabled.

4.4.2 PE READ OPERATION

The Tracking Oscillator, the PE Read Control, and the PE Read Logic form a phase-lock-loop (PLL) oscillator.

The PE Read operation is enabled when the NRZ and WRT signals are low to the Master Control. The microprogram in the Master Control sets the PE Read Gate signals (RGATEPE1 and RGATEPE2) and the Identification Gate (IDGATE) high. Refer to Figure 4-5.

The microformatter reads data either in the forward or reverse direction, depending on the state of REV2.

The READ DATA (IRDP, IRD0—7) are received and buffered by the Input Read Logic and coupled to the PE Read Logic.

The free running Tracking Oscillator provides all the clocks immediately except the Shift Right clocks (SHRCLK and NSHRCLK).

Plug-in R-C networks are used to determine the basic frequency of the oscillator. This basic frequency is dependent on the drive speed. Potentiometer R3 is provided for fine frequency adjust.

The clocks, SHRCLK and NSHRCLK, and signals, RGATE and IDGATE, are provided to the PE Read Logic. PE information is recognized and the feedback signals are generated. The feedback signals are:

(1) Delay Gate signals (DGATE/0 and DGATE/2) are supplied to the Tracking Oscillator to phase lock the oscillator.

(2) Envelope signals (ENV/P—7, ENV/0 and ENV/2) are supplied to the Tracking Oscillator to phase lock the oscillator. The ENV/P—7 signals are also supplied to the PE Read Control to generate the Drop signal (DROPDET), File Mark PE (FMKPE), and ID pulse (ID).

(3) Data In (D1/P—7) and Ones Detector (NONEDET/P—7) are supplied to the PE Read Control and provide control signals Postamble Test (POSTEST), Parity Correcting (PARC), Read Enable (REN1), Preset (PRESET), and Read Strobe (RSTRPE). The error status signals, Parity (PR), Formatter Error (NFER), and the Read Counter signals (RSC1 and NRSC2) are also provided to the Error Gating Logic.

(4) Character Detector signals (CHARDET/P—7) are supplied to the PE Read Control to trigger End of Data (RENDPE).

RSTRPE is supplied to the Read Strobe Gating Logic and is buffered and transmitted to the controller as READ STROBE (IRSTR).

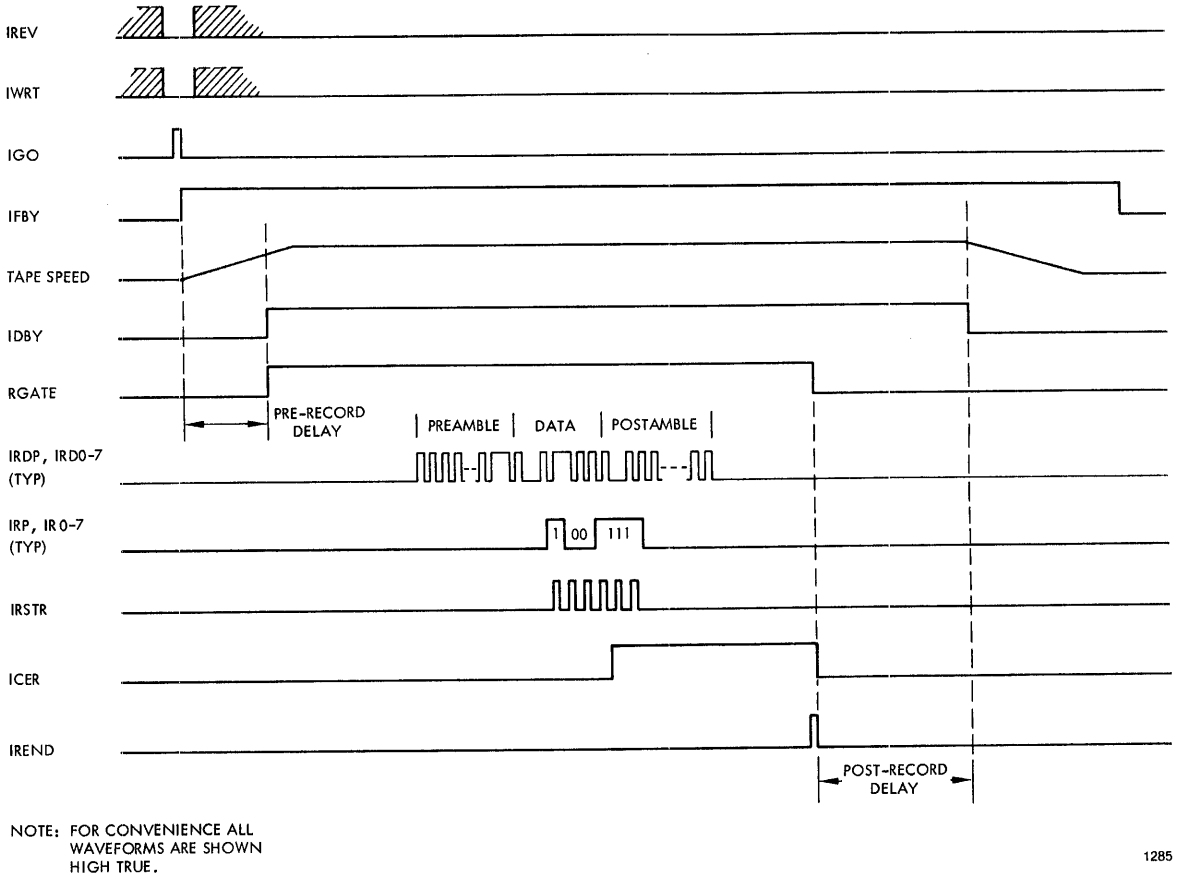


Figure 4-5. PE Read Operation Illustrating Error Correction for Last Two Data Bytes

The clocks and error signals are supplied to the Error Gating Logic. All error signals provide a HARD ERROR (IHER) indication except a single channel dropout (DROPDET1). DROPDET1 is a CORRECTED ERROR (ICER). RENDPE is fed back to the Master Control and disables the RGATEPE signals (low). The Read operation is complete.

If a Space Forward or Reverse (NSPC) is commanded, the Error Gating Logic and the Read Strobe Gating Logic are disabled.

4.5 FUNCTIONAL DESCRIPTION

The following paragraphs describe the major functional blocks of the microformatter. These blocks are shown in Figure 4-1 and should be referred to in conjunction with the following discussion.

4.5.1 INTERFACE LOGIC

The Interface Logic receives, buffers, and transmits status signals between the drive and controller. It also provides status signals to the microformatter circuits. U112-S3 and U112-S4 select either Microformatter Address 1 or 0. U112-5 (NRZI) is used for Format definition and U112-6 (SGL) is used for Head Type definition. Refer to Table 4-2.

4.5.2 CLOCK GENERATOR

The Clock Generator provides two programmed clock pulses, WCLK and NWCLK. U187 is set to provide the proper clock frequency, dependent on the drive speed. Refer to Table 4-4 for drive and switch settings.

The frequency of the clock pulses is eight times the PE data rate and sixteen times the NRZI data rate.

The SPEED signal causes the output frequency to be divided by two. This signal is used on dual speed systems only.

4.5.3 MASTER CONTROL

The Master Control stores the microprogram, contains the address counter, and provides the output buffer logic and the jump and output instructions. The Master Control also provides the Write Control logic signals (WCN0, WCN1 and WCN2) and the Write Load signal (LDWRTDATA).

Also provided by the Master Control logic are the PE Read Enable logic signals (RGATEP1, RGATEP2) or the NRZI Read Enable logic signals (RGATENZ1, RGATENZ2).

4.5.4 NRZI READ CONTROL

The NRZI Read Control provides control for decoding 9-track NRZI read data. This function is enabled by Reverse Command 1 (REV1) and allows the microformatter to decode read signals in both the forward and reverse directions.

Table 4-4

Master Oscillator Frequency Select (U187)

Drive (ips)	Frequency (kHz)	Switch Setting							
		1	2	3	4	5	6	7	8
12.5	160	U	U	U	D	D	U	D	U
18.75	240	U	U	U	D	D	D	U	U
22.5	288	Low Speed Only*							
25	320	D	D	U	D	U	D	U	U
37.5	480	U	U	D	D	D	U	U	U
45	576	D	D	D	U	D	U	U	U
75	960	D	U	D	D	U	U	U	U
112.5	1440	U	U	U	D	U	U	U	U
125	1600	D	D	D	U	U	U	U	U

U = Up
D = Down

*This frequency is selected by setting the switch to the 45 ips positions and SPEED is high.

4.5.5 TRACKING OSCILLATOR

The Tracking Oscillator provides selected clock frequencies determined by the drive speed. The frequency is nominal until locked to the data rate by the Data Gate (DGATE) and the Envelope (ENV) signals. Deskew is controlled by the feedback signals, NCOPY and COPY. Refer to Table 4-5 for drive speed and frequency of the Tracking Oscillator. The frequency is selected by plug-in R-C networks and is adjusted by potentiometer R3 (Frequency Adjust).

4.5.6 PE READ CONTROL

The PE Read Control provides control for decoding PE read data. It also provides feedback signals to deskew the PE read data.

4.5.7 INPUT READ LOGIC

The Input Read Logic receives and buffers read signals from the drive.

4.5.8 PE READ LOGIC

The PE Read Logic buffers and decodes PE read data from the drive. This function is enabled by Reverse Command 2 (REV2) and allows the microformatter to decode read signals in both the forward and reverse directions. It also provides feedback signals to lock the Tracking Oscillator to the incoming data.

4.5.9 NRZI READ LOGIC

The NRZI Read Logic buffers and decodes 9-track NRZI read data from the drive. The circuits are enabled via the interface signal, READ DATA STROBE (IRDS) and an internal signal, Not Clear NRZI Data (NCLRNZDATA).

4.5.10 OUTPUT READ LOGIC

The Output Read Logic buffers and transmits read signals to the controller.

Table 4-5

Tracking Oscillator Frequency

Tape Speed (ips)	Config. Plug 107609 Version No.	Maximum Frequency Limit (kHz)	Minimum Frequency Limit (kHz)	Exact Frequency Value (kHz)
12.5	-01	465	455	460
18.75	-02	697	683	690
22.5	-03	836	820	828
25	-04	929	911	920
37.5	-05	1394	1366	1380
45	-06	1672	1639	1656
75	-07	2788	2732	2760
112.5	-08	4181	4100	4140
125	-09	4700	4500	4600

4.5.11 WRITE DATA GENERATOR

The Write Data Generator receives and buffers write signals from the controller, processes the signals, and transmits the write signals to the drive. Depending on the states of the write control signals, PE or NRZI data are written. These signals also determine when the CRCC is written.

U112-S1 selects external parity and U112-S2 selects internal parity.

4.5.12 ERROR GATING

Error Gating provides error signals to the controller. The error signals are HARD ERROR (IHER) or CORRECTED ERROR (ICER). NSPC disables Error Gating during a space command.

4.5.13 READ STROBE GATING

The Read Strobe Gating provides either a NRZI or PE read strobe to the controller. NSPC disables Read Strobe Gating during a space command.

4.6 MICROFORMATTER MAINTENANCE AND ADJUSTMENT

The following paragraphs provide a method of fault isolation between the microformatter and the drive. Electrical adjustment procedures for the microformatter are also given.

4.6.1 MICROFORMATTER—DRIVE(S) FAULT ISOLATION

The recommended level of fault isolation is to the Microformatter PCBA and to the drive components. Two methods of fault isolation, in order of preference, are:

(1) Use Wilson Laboratories Inc. Hand Exerciser, TFX500, and the operating instructions for the exerciser; refer to Section VI of the applicable operating and service manual for the drive.

— OR —

(2) Use the procedure defined in Paragraph 4.6.1.1.

4.6.1.1 Fault Isolation

It is recommended that an all 1s tape for NRZI drive configurations, or an all 0s tape for PE drive configurations be generated. Also, a test tape to check errors and file marks should be available.

(1) Check the interface commands between the microformatter and the drive(s) using an oscilloscope. Refer to the fault isolation flow chart given in Figure 4-6.

(2) Using the previously generated test tapes, monitor (with an oscilloscope) the read interface lines between the microformatter and drive(s).

(3) Remove the all 1s or all 0s tape from the drive.

(4) Load a work tape, which is known to be good, onto the drive. Write an all 1s or an all 0s tape. Monitor the write interface lines between the microformatter and the drive(s).

When the fault is isolated to the microformatter or the drive, either replace the Microformatter PCBA or refer to Section VI of the applicable operating and service manual to fault isolate within the drive.

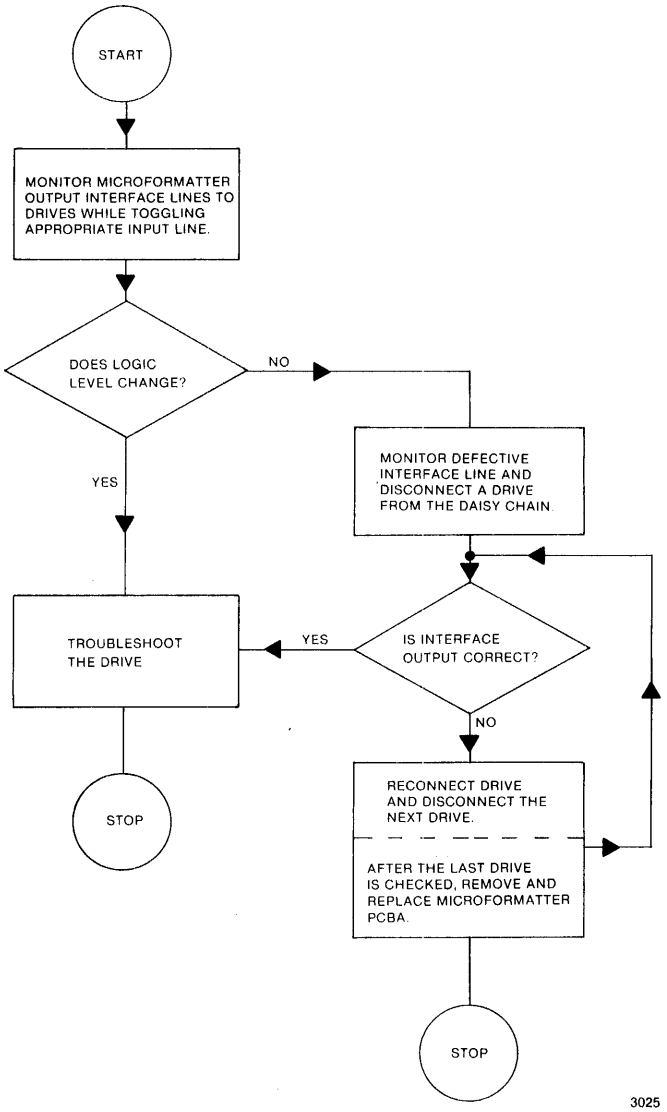


Figure 4-6. Fault Isolation Flow Chart

4.6.2 MICROFORMATTER ADJUSTMENTS

Electrical adjustments to the Microformatter PCBA are made as follows.

(1) Connect a DVM between TP1 and TP2 on the Microformatter PCBA.

(2) Acceptable Limits:

- + 5.0v (maximum)
- + 4.9v (minimum)

(3) If the reading observed in step (2) is outside the acceptable limits, adjust R6 on Power Supply II PCBA for + 4.95v.

NOTE

FT1000 systems only. This procedure may be performed by adjusting R179 on the Capstan/Regulator PCBA. However, some versions of the Capstan/Regulator PCBA have no provision for adjustment of the + 5v.

(4) Set switch U112 as defined in Table 4-1, 4-2, or 4-3.

(5) Set switch U187 as defined in Table 4-4.

(6) Connect a frequency counter between TP3 and TP4 on the Microformatter PCBA.

(7) Monitor the output of the frequency counter. The frequency of the Tracking Oscillator should fall within the maximum and minimum frequency limits given in Table 4-5 for the drive tape speed.

(8) If the observed frequency falls outside the maximum and minimum frequency range, adjust R3 on the Microformatter PCBA for the exact Tracking Oscillator frequency given in Table 4-5.

4.7 POWER SUPPLY II PCBA

The Power Supply II PCBA is used in conjunction with the Microformatter PCBA on PPC Drive Models FT6000, FT7000, FT8000, and FT9000. 48v dc versions of the drive use a different version of the PCBA. The primary difference is that a dc input voltage is provided on the 48v units, eliminating the need for the rectifier. Refer to Schematic No. 107614 and Assembly No. 107615 for discussion of the power supply functions.

(1) Rectifier.

(2) + 5v Regulator.

(3) Overcurrent Protection.

(4) Overvoltage Protection.

(5) Power Supply Enable

4.7.1 RECTIFIER (NOT USED ON 48V DC VERSIONS)

Rectifier CR1 is a full wave rectifier. The output of the rectifier is filtered, fused, and supplied to the regulator.

4.7.2 + 5V REGULATOR

The + 5v Regulator consists of U1, R5, R6, R7 and Q1. The regulator provides base drive to the series pass transistor, Q1. The voltage divider (R5, R6 and R7) determines the voltage output. R6 is adjusted to provide + 4.95v at TP1 on the Microformatter PCBA. The regulator also has a current foldback circuit.

4.7.3 OVERCURRENT PROTECTION

The overcurrent protection is provided by a voltage divider (R2, R3 and R4). R3 is the current sense resistor. If the current increases across R3, the signal is fed back to U1 causing U1 to decrease its output. A short at the output causes U1 to shut off and remain shut off until the short is removed.

4.7.4 OVERVOLTAGE PROTECTION

The overvoltage protection is provided by Q2, VR1 and SCR1. If the output voltage exceeds + 5.7 volts, VR1 conducts. This causes Q2 to conduct and fire SCR1. When SCR1 fires, a direct short (crowbar) occurs causing fuse F1 to open.

4.7.5 POWER SUPPLY ENABLE (PSEN)

The POWER SUPPLY ENABLE signal (IPSEN) is used to reset all microformatter logic to the quiescent state. This is done while the + 5v supply is being established after power is applied and while the supply is decaying after power is turned off. This ensures that the logic is in a defined state after power on and that no spurious signals are sent to the drive logic.

When power is applied, the regulated output builds up to + 5v causing C6 to charge through R14 and R15. When the voltage on C6 reaches 2.5v, the voltage on the base of Q5 will be greater than the voltage on the base of Q3. Q4 and Q5 will then turn on causing the output PSEN to go to + 4v approximately 50 milliseconds after power is applied. A loss of dc power is detected by Q3 when the voltage on C7 drops below + 3v.

4.8 POWER SUPPLY II ELECTRICAL ADJUSTMENTS

The following paragraphs provide a method of fault isolation to a stage in the power supply.

4.8.1 POWER SUPPLY II

Figure 4-7 is a functional block diagram of the power supply. Table 4-6 lists measurement points and voltage readings for a normally operating power supply. All readings assume that the output voltage of the power supply as measured between pins 3 and 1 of Power Supply J2 is:

- + 5.36v (maximum)
- + 5.14v (minimum)

In the event that the voltage read between J2 pins 3 and 1 falls outside the acceptable limits, perform the adjustment given in Paragraph 4.8.2.

4.8.2 POWER SUPPLY II ALIGNMENT

Electrical adjustments to the power supply are made as follows.

(1) Connect a DVM between TP1 and TP2 on the Microformatter PCBA.

(2) Acceptable Limits:
   - + 5.0v (maximum)
   - + 4.9v (minimum)

(3) If the reading observed in step (2) is out of tolerance, adjust R6 on Power Supply II PCBA until a voltage reading of + 4.95v is obtained between TP1 and TP2 on the Microformatter PCBA.

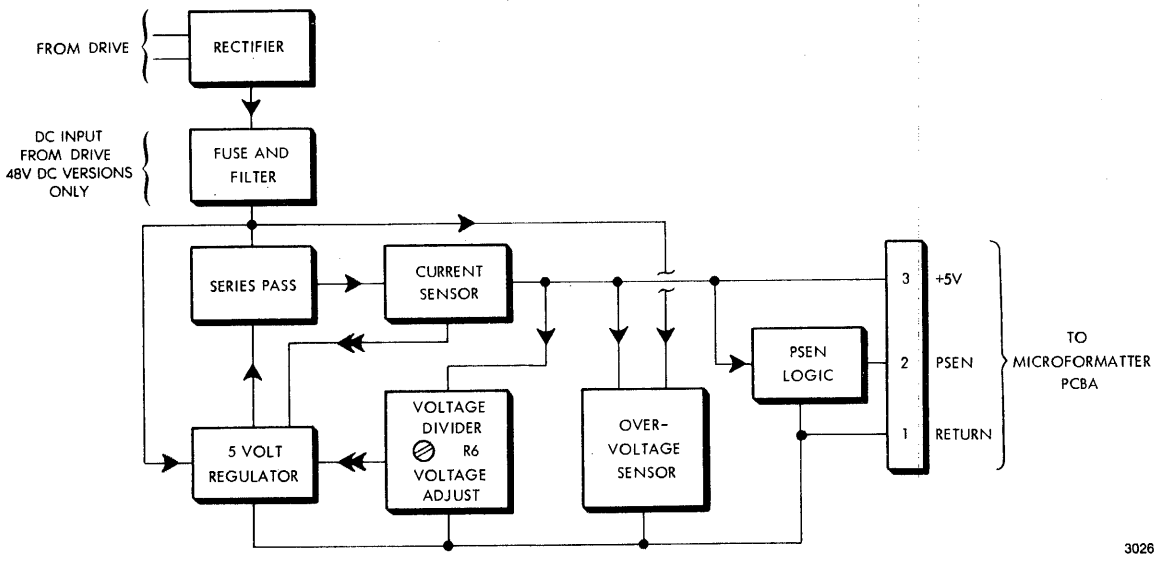


Figure 4-7. Power Supply Functional Block Diagram

Table 4-6
Nominal Power Supply Voltage Readings

Measurement Point	Voltage Reading
Across rectifier input	10.4v ac
Q1E/GND	+ 10.5
Q1B/GND	+ 9.0
Q1C/GND	+ 6.0
JCT R3-R5/GND	+ 5.25
JCT R6-R7/GND	+ 1.8
VR1 Cathode/GND	+ 5.2
Q2B/GND	+ 5.2
Q2C/GND	0v

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8YZ PRE PROD RELEASE				
B	ECN 971				
C	ECN 9893A				
	ERN 9-UX PROD RELEASE				
D	ECN 9940				
E	ECN 10745				
F	ECN 10874				
G	ECN 11134				
H	ECN 12519C				
J	ECN 12900				
K	ECN 12966				
K1	ECN 14769				
L	ECN 15360				
M	ECN 17026				
N	ECN 17617		E.T.		
N1	ECN 18380				
P	ECN 19017				

[1] TABLE I

PART NO.	REFERENCE DESIGNATION
100-1025	R1
100-0205	R2
120-0001	U130, 94, 173, 214
120-0008	U186
132-2752	C4, 5, 7, 8, 11, 12, 14, 17, 18, 20, 21, 22, 25, 26, 29, 30, C32 THRU 47, 50, 51
135-1002	C31
402-1115	U108
564-0009	U112, 187
700-7404	U134, 251
700-7406	U91, 111, 151, 190, 210
700-7453	U69, 109, 169, 233, 267
700-7450	U92, 113, 132, 258
710-4051	U228, 260, 000, 270, 280
710-4101	U209, 250
710-4163	U270, 304, 248, 249, 250, 165
710-4174	U34, 41, 49, 101, 149, 161, 172, 188, 192, 204, 209, U212, 229, 273, 274, 284
710-4175	U152, 272
710-4200	U195
710-7400	U182, 207, 232, 252, 254, 286
710-7402	U266, 98
710-7404	U50, 222
710-7408	U263
710-7410	U227
710-7411	U130, 135, 154
710-7414	U9, 93, 114, 130, 159, 174, 190, 213
710-7432	U245
710-7474	U189
710-7476	U208
710-7486	U150, 189, 234
107651-07	U170, 171
107654-08	U191
107654-09	U211
107652-10	U231

[3] TABLE III

PART NO.	REFERENCE DESIGNATION
100-1025	R9
100-1535	R7
100-2225	R6
100-4815	R4
107-4220	R8
107-4810	R5
124-1021	R3
130-4715	C48
132-2752	C1, 2, 3, 6, 9, 10, 13, 15, 16, 19, 23, 24, 27, 28,
139-4990	C49
200-4025	Q1, 2, 3
200-4025	Q4
700-4040	U223
700-7400	U262
700-7404	U244
710-4153	U7, 27, 47, 67, 87, 107, 128, 147, 167
710-4161	U242, 243
710-4163	U8, 13, 14, 28, 34, 48, 68, 88, 108, 129, 148, 168, 288, U221, 241
710-4164	U264
710-4174	U6, 26, 46, 66, 86, 106, 127, 146, 166
710-4200	U51, 202
710-7400	U265
710-7402	U71, 287
710-7404	U247
710-7408	U225
710-7410	U226, 285
710-7411	U4, 24, 44, 64, 84, 104, 125, 144, 164, 208, 224, 246
710-7427	U1, 61, 122
710-7450	U70, 72
710-7452	U11, 205
710-7476	U30, 52, 53, 54, 73, 74
710-7486	U29, 89
710-7495	U2, 22, 42, 62, 82, 102, 123, 142, 162
710-7496	U3, 23, 43, 63, 83, 103, 124, 143, 163
108650-01	U216
107651-01	U5, 25, 45, 65, 85, 105, 126, 140, 165
108651-02	U21, 81, 141

[2] TABLE II

ASSEMBLY 107605 VERSION NO.	VERSION CHARACTER-ISTIC	W1, 3 (100-0005)	W2, 4 (100-0005)	U11, 13, 14, 30, U31, U51 THRU 54, U70 THRU 74 — USAGE [3]	C1, 2, 3, 6, 9, 10, 13, 15, 16, 19, 23, 24, 27, 28, 48, 49; R3 THRU 9; Q1 THRU 4; U1 THRU 8, 21 THRU 29, 42 THRU 48, 61 THRU 68, U81 THRU 89, 102 THRU 108, 122 THRU 129, U141 THRU 148, 162 THRU 168, 181, 202, 203, 205, U206, 221, 223 THRU 226, 241 THRU 244, 246, 247, U262, 264, 265, 285, 287 — USAGE [3]	U12 (107649-XX)	U33	U289 (107649-XX)	U291 [15]	U292 [15]	U293 [15]	U294 [15]
-01	PE AND NRZI	OMIT	OMIT	USE	USE	-02	103983-03	-01	USE	USE	USE	USE
-02	PE ONLY	OMIT	USE	OMIT	USE	OMIT	OMIT	-01	USE	USE	USE	USE
-03	NRZI ONLY	USE	OMIT	USE	OMIT	-02	103983-03	OMIT	USE	USE	USE	USE
-04	PE/NRZ	OMIT	OMIT	USE	USE	-04	109380-01	-03	USE	USE	USE	USE

TABLE VII
[13] OPTION CONFIGURATIONS

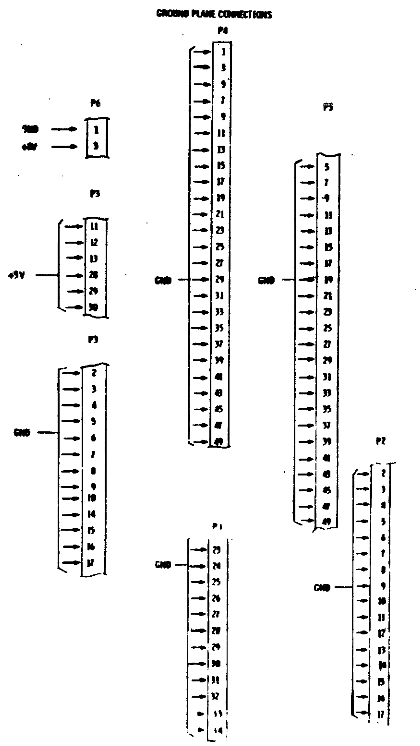
FUNCTION		U112 SWITCHES OPEN	U112-SWITCHES CLOSED
PARITY	INTERNAL	S1	S2
	EXTERNAL	S2	S1
FMTR ADDRESS	ZERO	S4	S3
	ONE	S3	S4
FORMAT	PE - NOT DAISY CHAIN		S5
	ALL OTHERS	S5	
HEAD	SINGLE - NOT DAISY CHAIN		S6
	ALL OTHERS	S6	

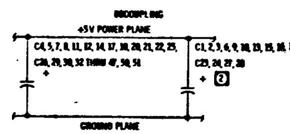
TABLE VI
[12] SPEED CONFIGURATIONS

SPEED (IPS)	U187-SWITCHES OPEN	U187-SWITCHES CLOSED	FOR PE INSTALL 107609-XX IN U282 [11]
12.5	S1, S2, S3, S6, S8	S4, S5, S7	-01
18.75	S1, S3, S7, S8	S2, S4, S5, S6	-02
25	S3, S5, S7, S8	S1, S2, S4, S6	-04
37.5	S1, S2, S6, S7, S8	S3, S4, S5	-05
45	S4, S6, S7, S8	S1, S2, S3, S5	-06
75	S2, S5, S6, S7, S8	S1, S3, S4	-07
112.5	S1, S2, S3, S5, S6, S7, S8	S4	-08
125	S4, S5, S6, S7, S8	S1, S2, S3	-09

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	DELETED
C51		
R9		
Q4		
U294	10	
W4		

GROUND PLANE CONNECTIONS





[5] TABLE IV

TYPE	REFERENCE DESIGNATION
7433	U169B, U169C, U169D, U231A, U231C, U231D
74LS00	U207A, U252C, U286C
74LS02	U71B, U266C
74LS08	U263D
74LS10	U226B
74LS11	U130A, U130B, U154A, U154D, U246A, U246B
74LS14	U194D
7406	U91B, U111C, U190A, U210A, U210B
74LS86	U234C, U234D
120-0008	U186B, C, D, E, F
74LS32	U264B

[9] TABLE V

TYPE	FUNCTIONAL DESCRIPTION
74LS95	4-BIT SHIFT REGISTER
74LS96	5-BIT SHIFT REGISTER
74LS151	8-TO-1 DATA SELECTOR
74LS153	DUAL 4-TO-1 DATA SELECTOR
74LS161	4 BIT CNTR/SYNCHRONOUS CLR
74LS163	4 BIT CNTR/SYNCHRONOUS CLEAR
74LS164	8-BIT SHIFT REGISTER
74LS174	6-BIT D TYPE FLIP FLOP
74LS280	9-BIT PARITY GENERATOR

[15] SEE TABLE XIII FOR VALID COMBINATIONS OF PROM & PLA PART NUMBERS, VERSION NUMBERS AND REVISION LEVELS FOR EACH ASSEMBLY VERSION AND REVISION LEVEL.

[14] "T" OR "C" SUFFIX ON MNEMONIC IS FOR REFERENCE ONLY.

[13] SEE TABLE VII FOR OPTION CONFIGURATIONS.

[12] SEE TABLE VI FOR SPEED CONFIGURATIONS.

[11] PLUG ASSY 107609-XX IS SPECIFIED AT TOP ASSEMBLY.

[10] ~~REFERENCE DESIGNATIONS NOT USED:~~ U15, 16, 17, 18, 19, 20, 32, 35, 36, 37, 38, 39, 40, 55, 56, 57, 58, U59, 60, 75, 76, 77, 78, 79, 80, 95, 96, 97, 98, 99, 100, 115, 116, 117, 118, 119, 120, 121, 131, 135, 136, 137, U138, 139, 140, 155, 156, 157, 158, 159, 160, 175, 176, 177, 178, 179, 180, 195, 196, 197, 198, 199, 200, 215, U216, 217, 218, 219, 200, 235, 236, 237, 238, 239, 240, 255, 256, 257, 258, 259, 260, 261, 271, 275, 276, 277, U278, 279, 280, 281.

[9] FOR I. C. FUNCTIONAL DESCRIPTION, SEE TABLE V.

8. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING WITH THE ASSOCIATED LOGIC TERM MNEMONIC. THE [illegible]

7. CAPACITOR VALUES ARE 2.7 MICROFARADS, 80%, 35V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

[5] FOR SPARE LOGIC ELEMENTS SEE TABLE IV.

4. ON 14 PIN I. C.'s PIN 7 IS GND AND PIN 14 IS +5V, ON 16 PIN I.C.'s PIN 8 IS GND AND PIN 16 IS +5V.

[3] FOR PART NUMBER, SEE TABLE III.

[2] FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY NO. 107605
SPECIFICATION NO.
PROGRAM LISTING: -01, -02, -03 VERSIONS: 107600
-04 VERSION: 110070
REFERENCE DRAWINGS

PERTEC PERIPHERAL EQUIPMENT

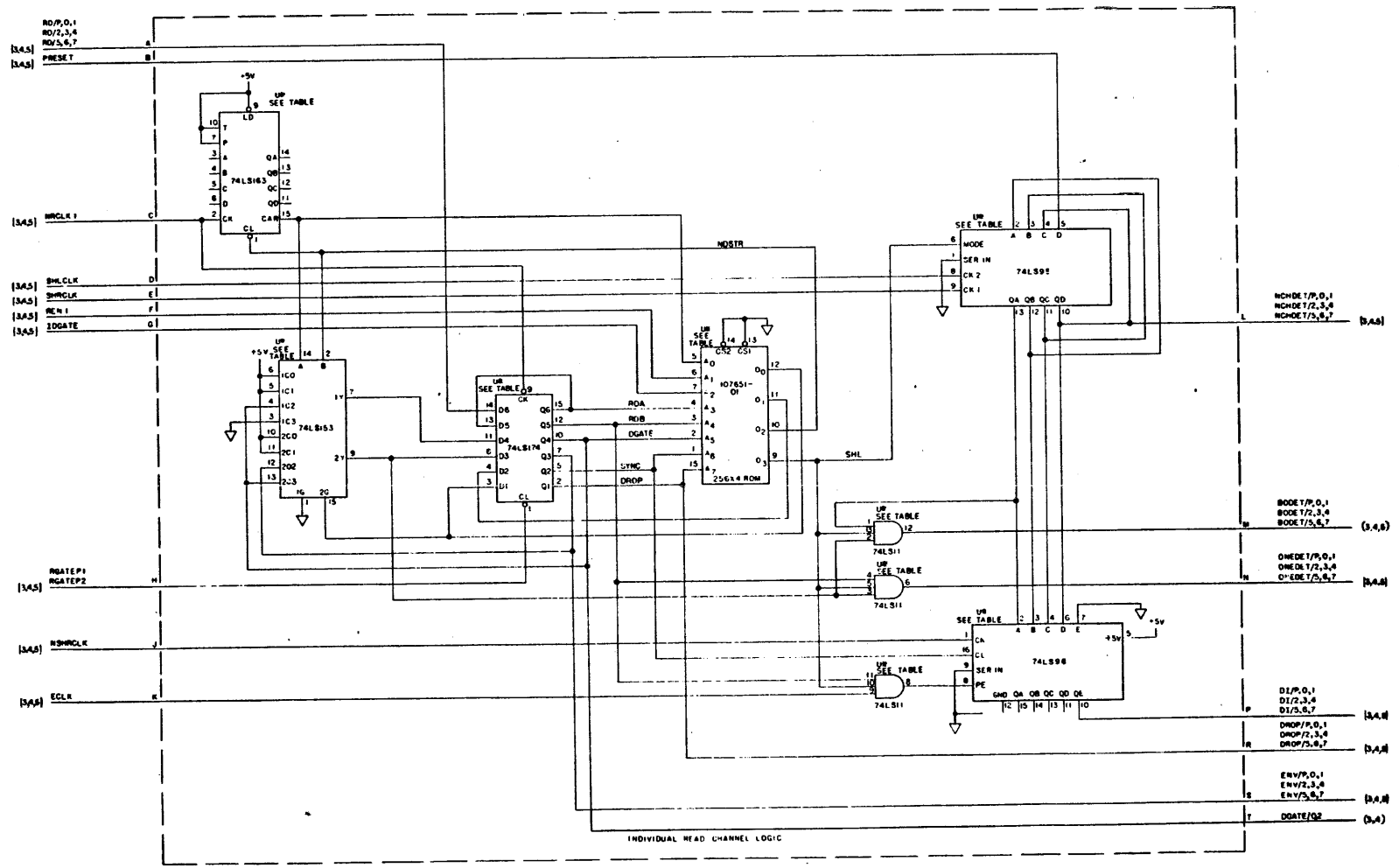
TITLE SCHEMATIC, MICROFORMATTER BOARD

SIZE E DRAWING NO. 107604 REV P

107605 | APPLICATION

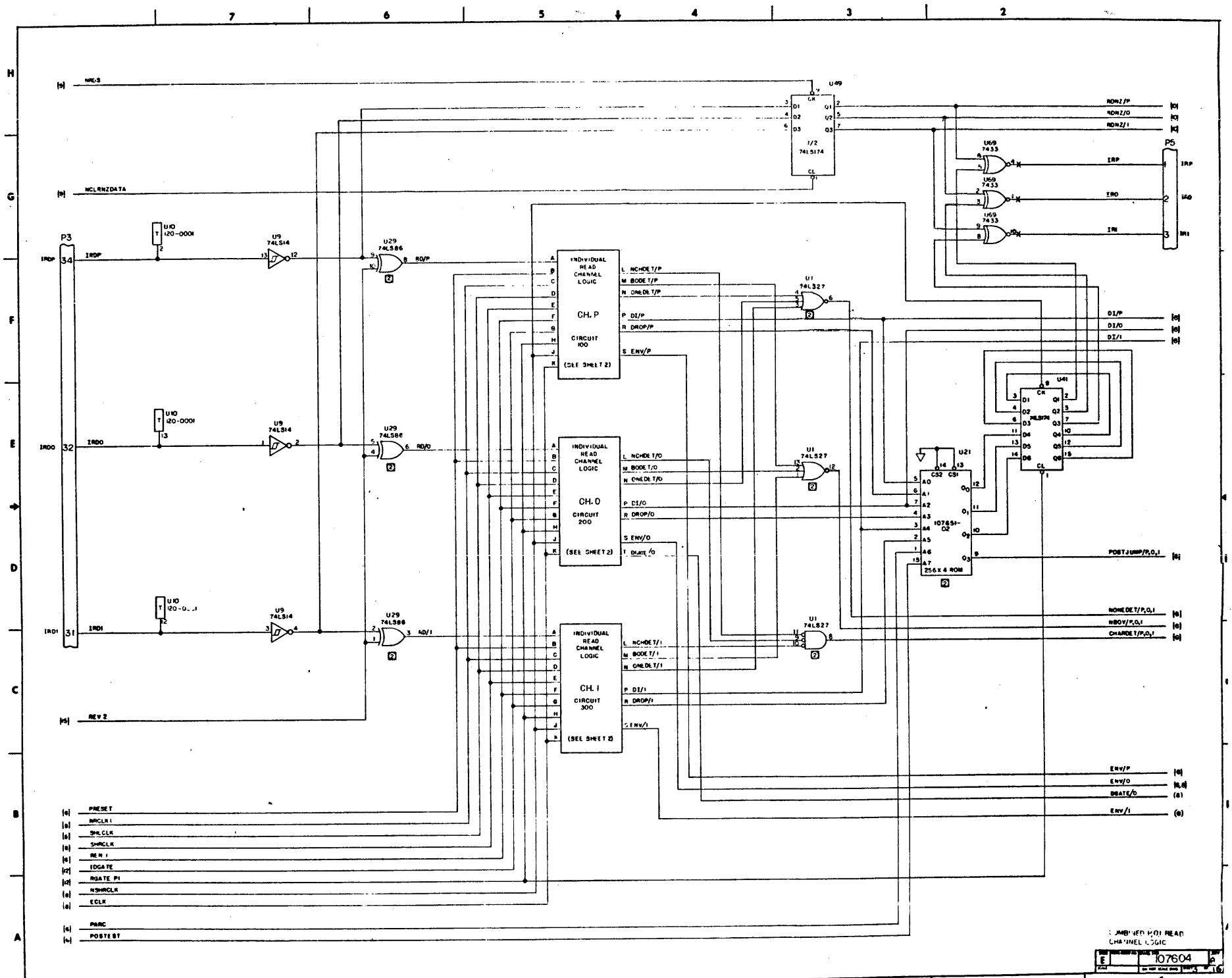
SHEET 1 OF 16

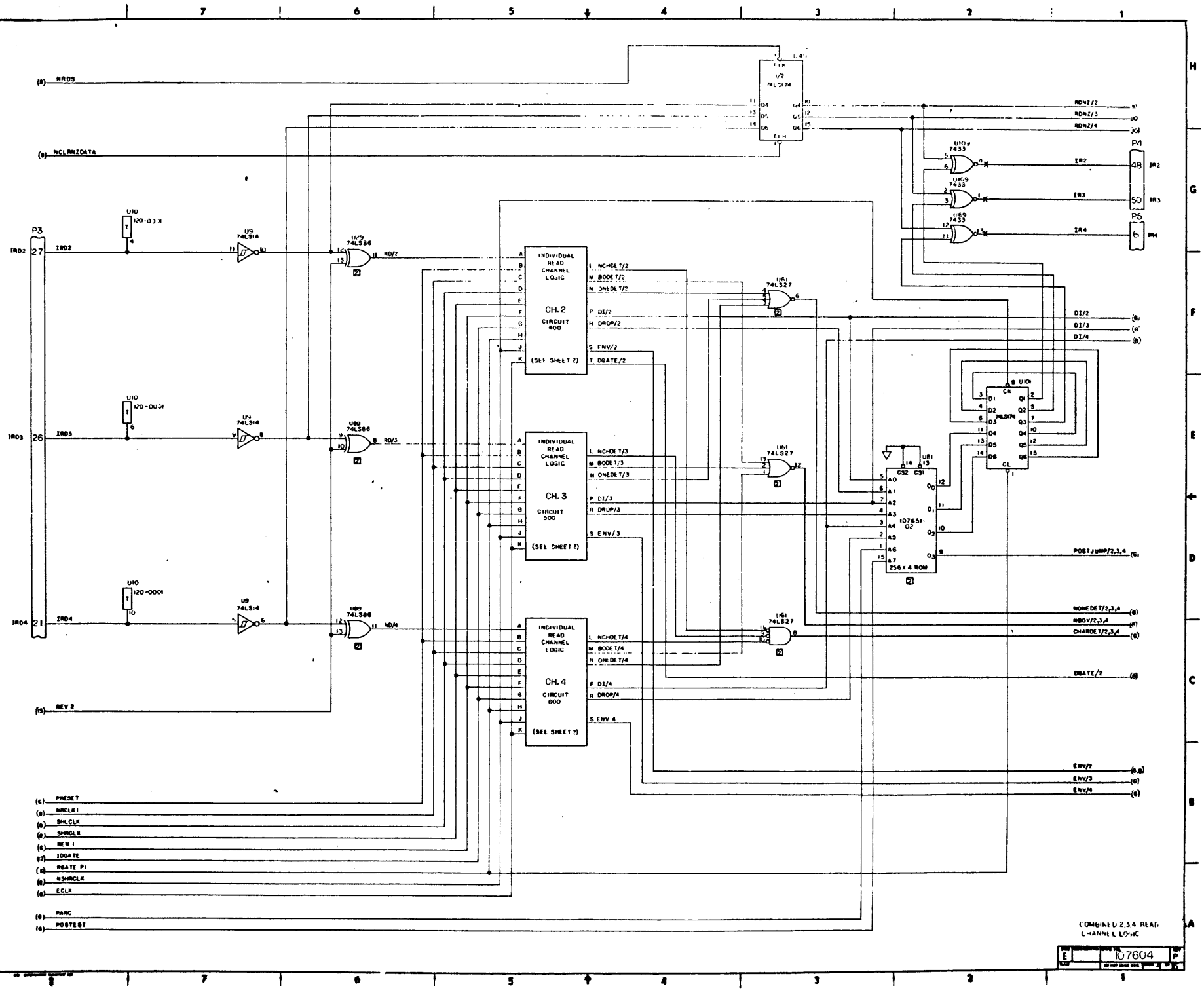
REF DESIGNATION TABLE [2]									
		INDIVIDUAL READ CHANNEL							
IC TYPE		P	0	1	2	3	4	5	6	7
	74LS95	U2	U22	U42	U62	U82	U102	U123	U142	U162
	74LS96	U3	U23	U43	U63	U83	U103	U124	U143	U163
	74LS11	U4	U24	U44	U64	U84	U104	U125	U144	U164
	107651-01	U5	U25	U45	U65	U85	U105	U126	U145	U165
	74LS174	U6	U26	U46	U66	U86	U106	U127	U146	U166
	74LS153	U7	U27	U47	U67	U87	U107	U128	U147	U167
	74LS163	U8	U28	U48	U68	U88	U108	U129	U148	U168

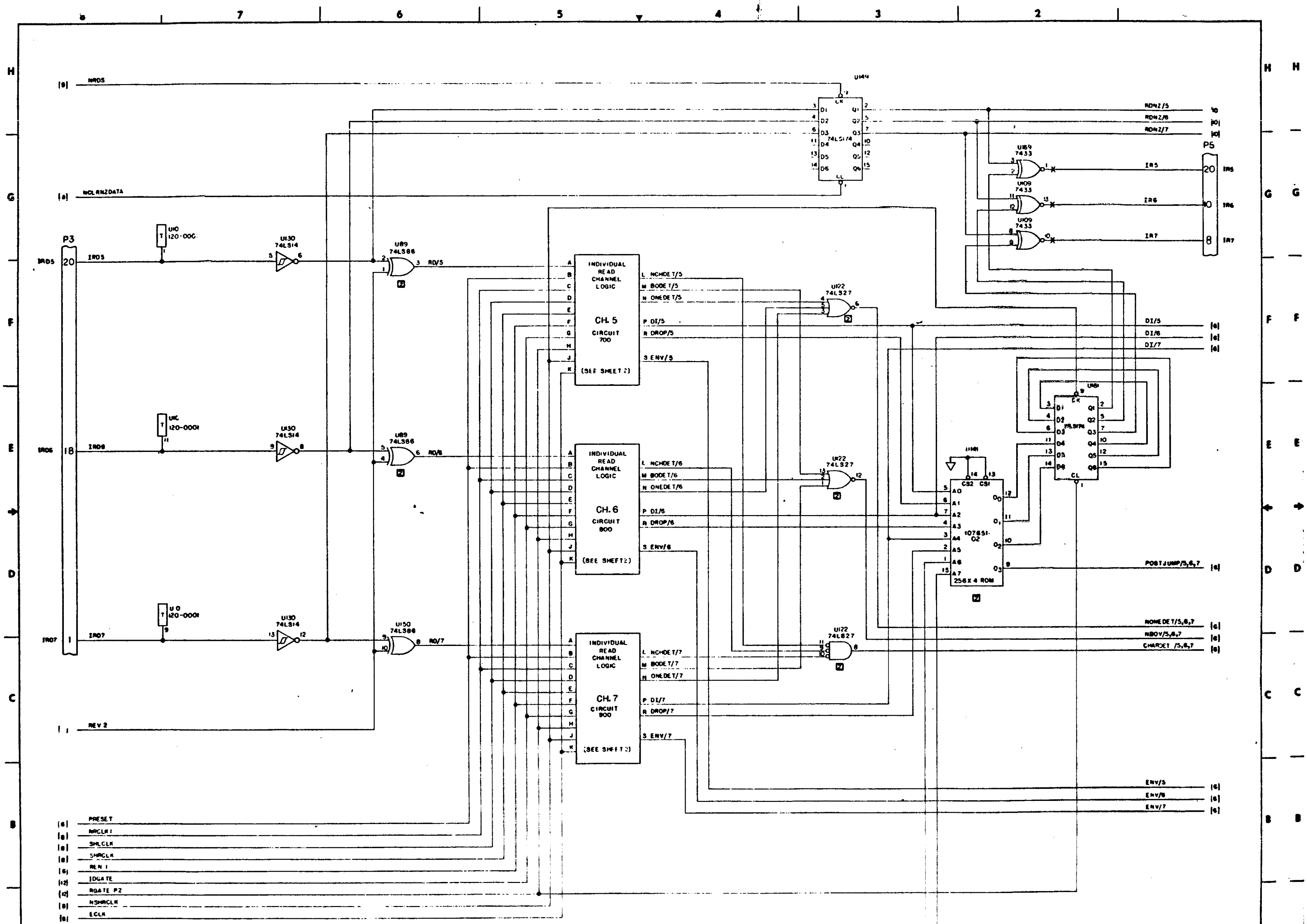


INDIVIDUAL READ CHANNEL LOGIC

SIZE	DWG NO	REV
E	107604	P


NRDS
NCLRNZDATA
P3
IRDP
IRDO
IRDI
REV 2
U10 120-0001
U9 74LS14
U29 74LS86
RD/P
RD/O
RD/I
INDIVIDUAL READ CHANNEL LOGIC
CH. P CIRCUIT 100
CH. 0 CIRCUIT 200
CH. 1 CIRCUIT 300
(SEE SHEET 2)
L NCHDET/P
M BDDET/P
N ONEDET/P
P DI/P
R DROP/P
S ENV/P
L NCHDET/O
M BDDET/O
N ONEDET/O
P DI/O
R DROP/O
S ENV/O
T DGATE/O
L NCHDET/1
M BDDET/1
N ONEDET/1
P DI/1
R DROP/1
S ENV/1
U49
1/2 74LS174
U69 7433
RDNZ/P
RDNZ/O
RDNZ/1
IRP
IRO
IR1
P5
U1 74LS27
DI/P
DI/O
DI/1
U41
74LS374
U21
CS2 CS1
A0 A1 A2 A3 A4 A5 A6 A7
O0 O1 O2 O3
1074S1-02
256 X 4 ROM
POSTJUMP/P,O,I
NONEDET/P,O,I
NBDY/P,O,I
CHARDET/P,O,I
ENV/P
ENV/O
BGATE/O
ENV/1
PRESET
NRCLR1
SHLCLK
SHRCLK
REN 1
IDGATE
RGATE P1
NSHRCLR
ECLR
PARC
POSTEST
COMBINED PDT READ CHANNEL LOGIC
107604

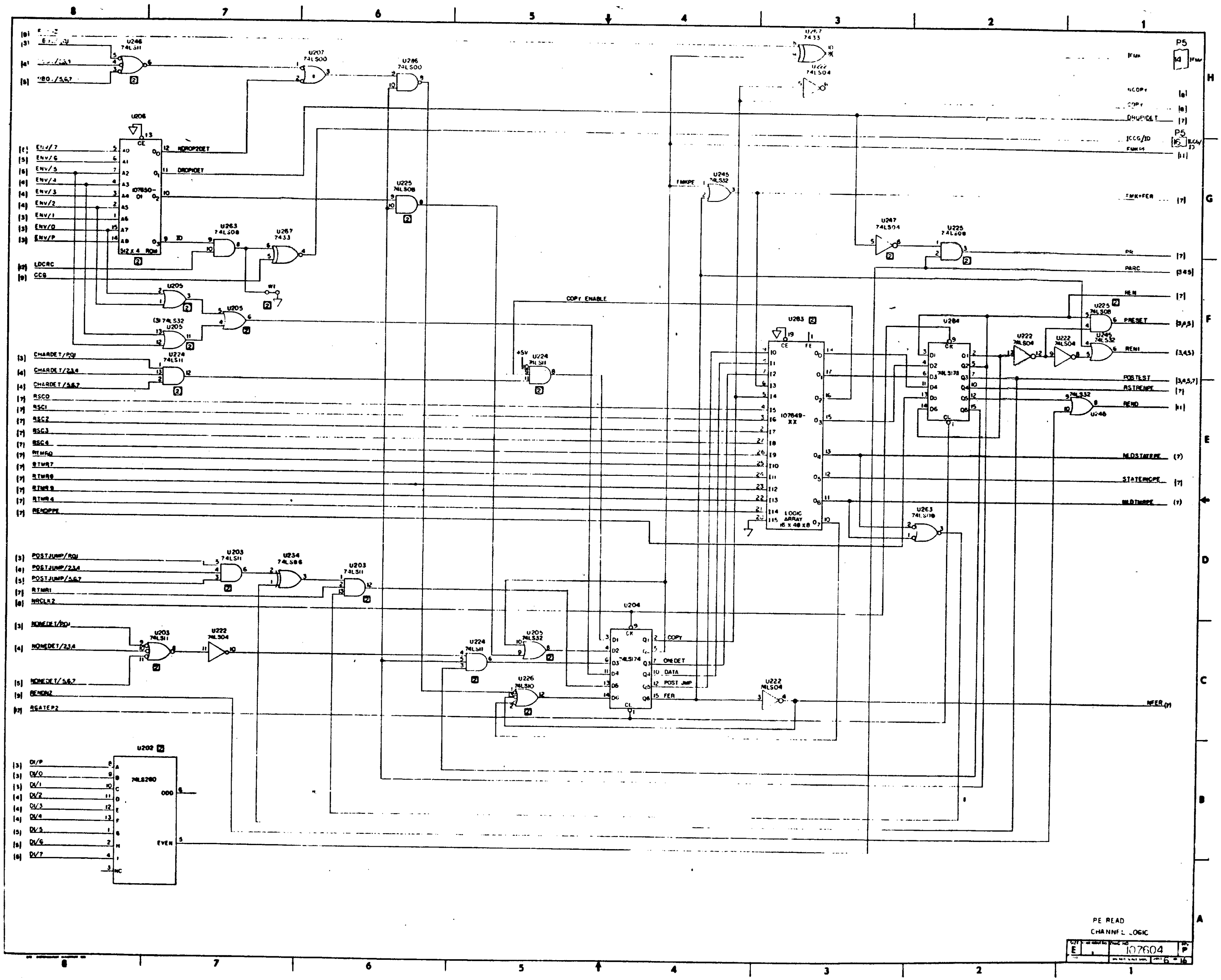

NRD9
NCLRNZDATA
P3
IRD2
IRD3
IRD4
REV 2
U10
120-0001
U9
74LS14
U89
74LS86
RD/2
RD/3
RD/4
INDIVIDUAL READ CHANNEL LOGIC
CH. 2 CIRCUIT 400
CH. 3 CIRCUIT 500
CH. 4 CIRCUIT 600
(SEE SHEET 2)
L NCHDET/2
M BODET/2
N ONEDET/2
P DI/2
R DROP/2
S ENV/2
T DGATE/2
L NCHDET/3
M BODET/3
N ONEDET/3
P DI/3
R DROP/3
S ENV/3
L NCHDET/4
M BODET/4
N ONEDET/4
P DI/4
R DROP/4
S ENV 4
U151
74LS27
U81
CS2 CS1
107651-02
256 X 4 ROM
U101
74LS174
RDN2/2
RDN2/3
RDN2/4
U109
7433
IR2
IR3
IR4
P4
P5
48
50
6
DI/2
DI/3
DI/4
POSTJUMP/2,3,4
NONEDET/2,3,4
NBOV/2,3,4
CHARDET/2,3,4
DGATE/2
ENV/2
ENV/3
ENV/4
PRESET
NRCLR1
BHLCLK
SHRCLK
REN 1
IDGATE
RGATE P1
NSHRCLK
ECLK
PARC
POSTEST
COMBINED 2,3,4 READ CHANNEL LOGIC
107604



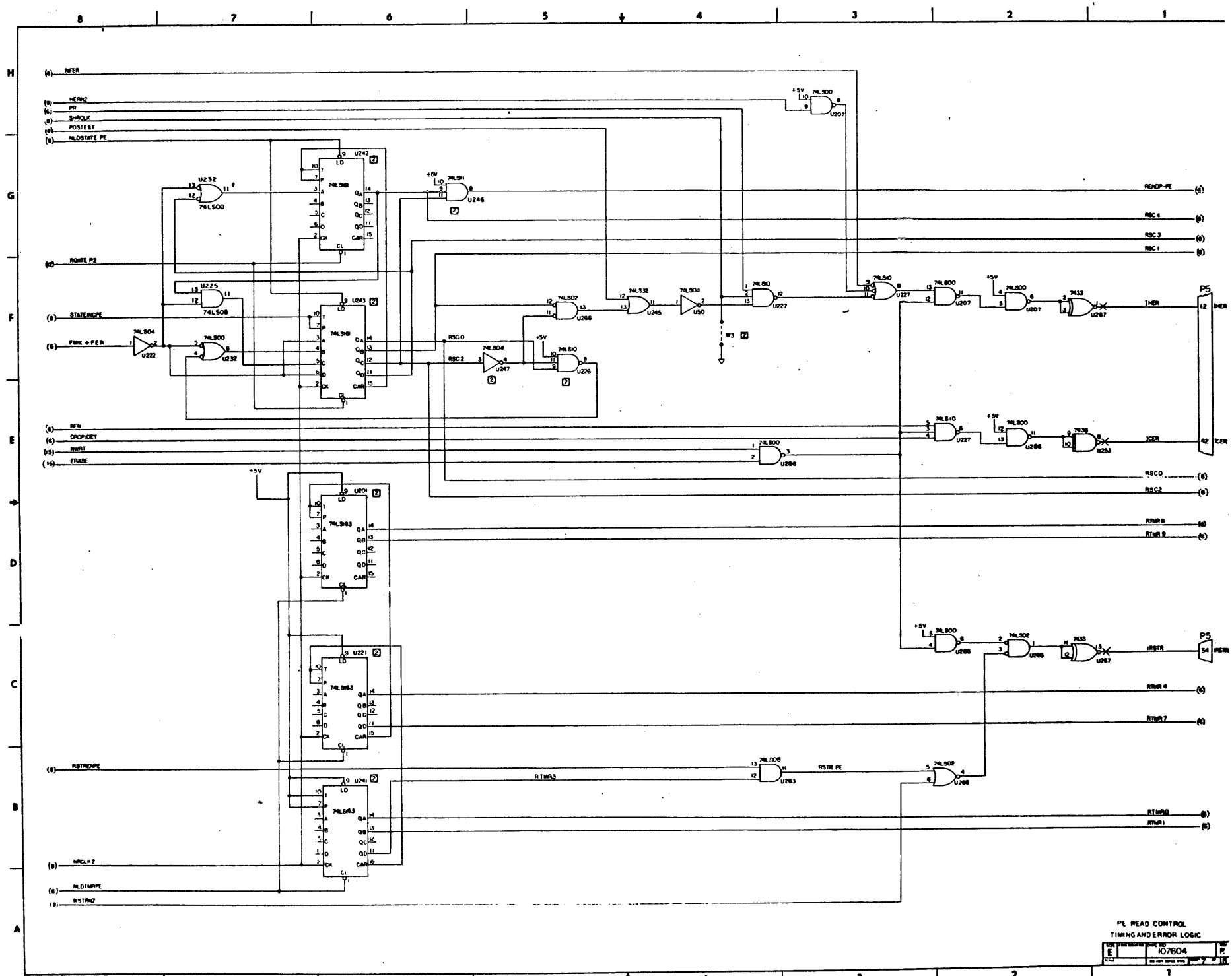
COMBINED 5,6,7 READ
CHANNEL LOGIC

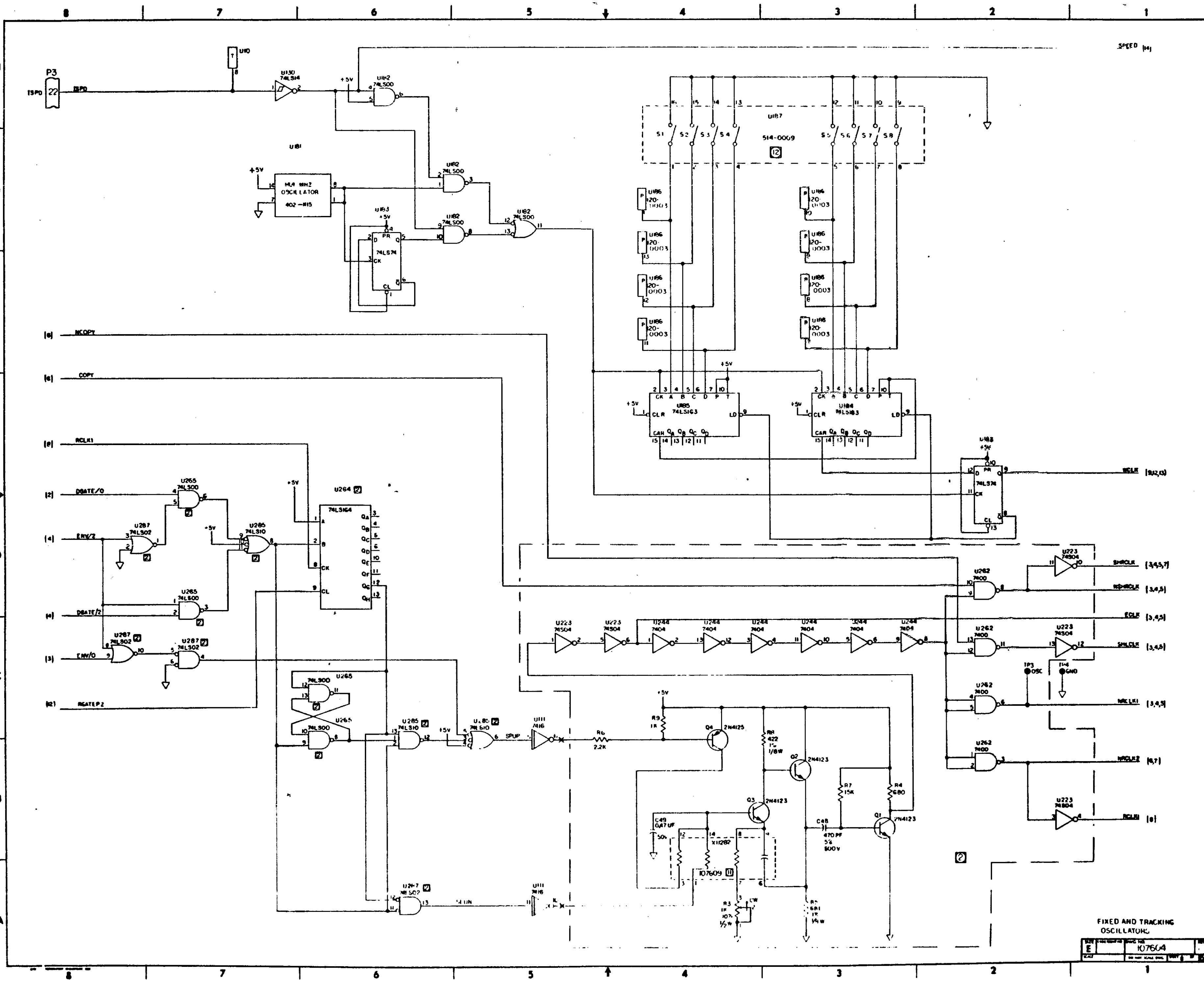
SIZE	DWG NO	REV
E	107604	P

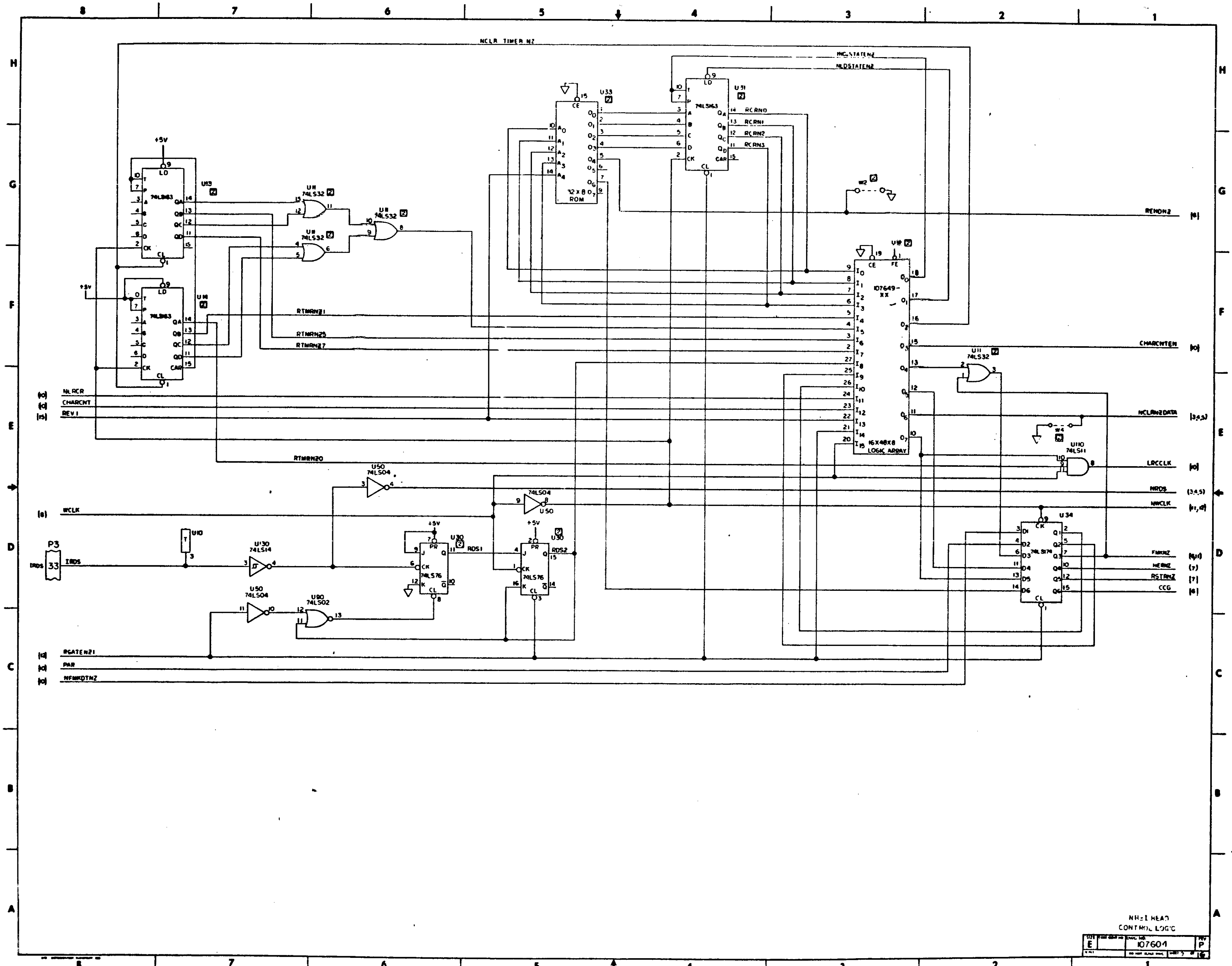
SHEET 5 OF 6

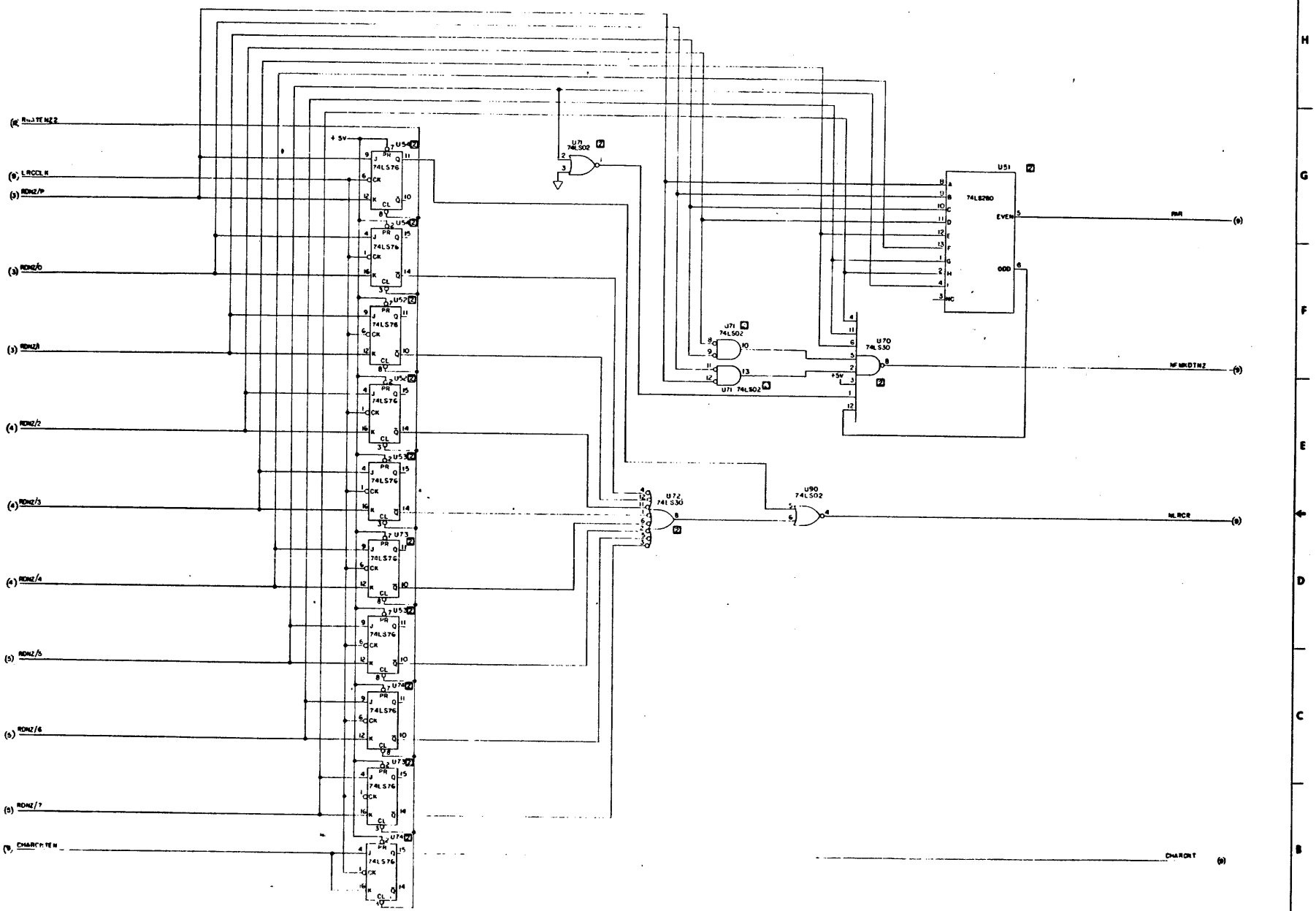


U246 74LS11
U207 74LS00
U286 74LS00
U206
107850-01
512 x 4 ROM
NDROP2DET
DROPDET
U225 74LS08
U263 74LS08
U267 7433
LDCRC
CCG
U205
U205 74LS32
U224 74LS11
CHARDET/PQ1
CHARDET/234
CHARDET/567
RSC0
RSC1
RSC2
RSC3
RSC4
RTMR0
RTMR7
RTMR8
RTMR9
RTMR4
RENOPPE
COPY ENABLE
U245 74LS32
FMKPE
U247 74LS04
U283
107849-XX
LOGIC ARRAY 16 x 48 x 8
U284
74LS173
U222 74LS04
U246 74LS32
U248
PR
PARC
FEN
PRESET
RENI
POSTEST
RSTRENPE
REND
NLDSTATEPE
STATENOPE
NLDTMRPE
FMK+FER
ICCG/ID
NCOPY
COPY
DRUPIDET
POSTJUMP/PQ1
POSTJUMP/234
POSTJUMP/567
RTMR1
NRCLK2
U203 74LS11
U234 74LS86
U204
74LS174
COPY
ONEDET
DATA
POST JMP
FER
NFER
NONEDET/PQ1
NONEDET/234
NONEDET/567
RENDN2
RGATEP2
U226 74LS10
U202
74LS280
ODD
EVEN
DI/P
DI/0
DI/1
DI/2
DI/3
DI/4
DI/5
DI/6
DI/7
P5
PE READ
CHANNEL LOGIC
107604


PE READ CONTROL
TIMING AND ERROR LOGIC
E
107604
P


P3
TSPD
U130
74LS14
U142
74LS00
+5V
SPEED
U187
514-0009
S1
S2
S3
S4
S5
S6
S7
S8
U181
+5V
OSCILLATOR
U182
74LS00
U163
74LS74
U186
NCOPY
COPY
U185
74LS163
U184
74LS163
RCLK1
U183
74LS74
WCLK
DGATE/0
ENV/2
U265
74LS00
U287
74LS02
U285
74LS10
U264
74LS164
DGATE/2
ENV/0
RGATEP2
U223
74S04
U244
7404
U262
7400
SHRCLK
RSHRCLK
ECLK
SHLCLK
TP3
OSC
GND
NRCLK1
NRCLK2
RCLKI
SPUP
U111
7416
R6
2.2K
R9
1K
Q4
2N4125
Q2
2N4123
Q3
2N4123
Q1
2N4123
R7
15K
R4
680
C49
0.47 UF
C48
470 PF
500V
107609
R3
1K
CW
FIXED AND TRACKING
OSCILLATORS
E
107604

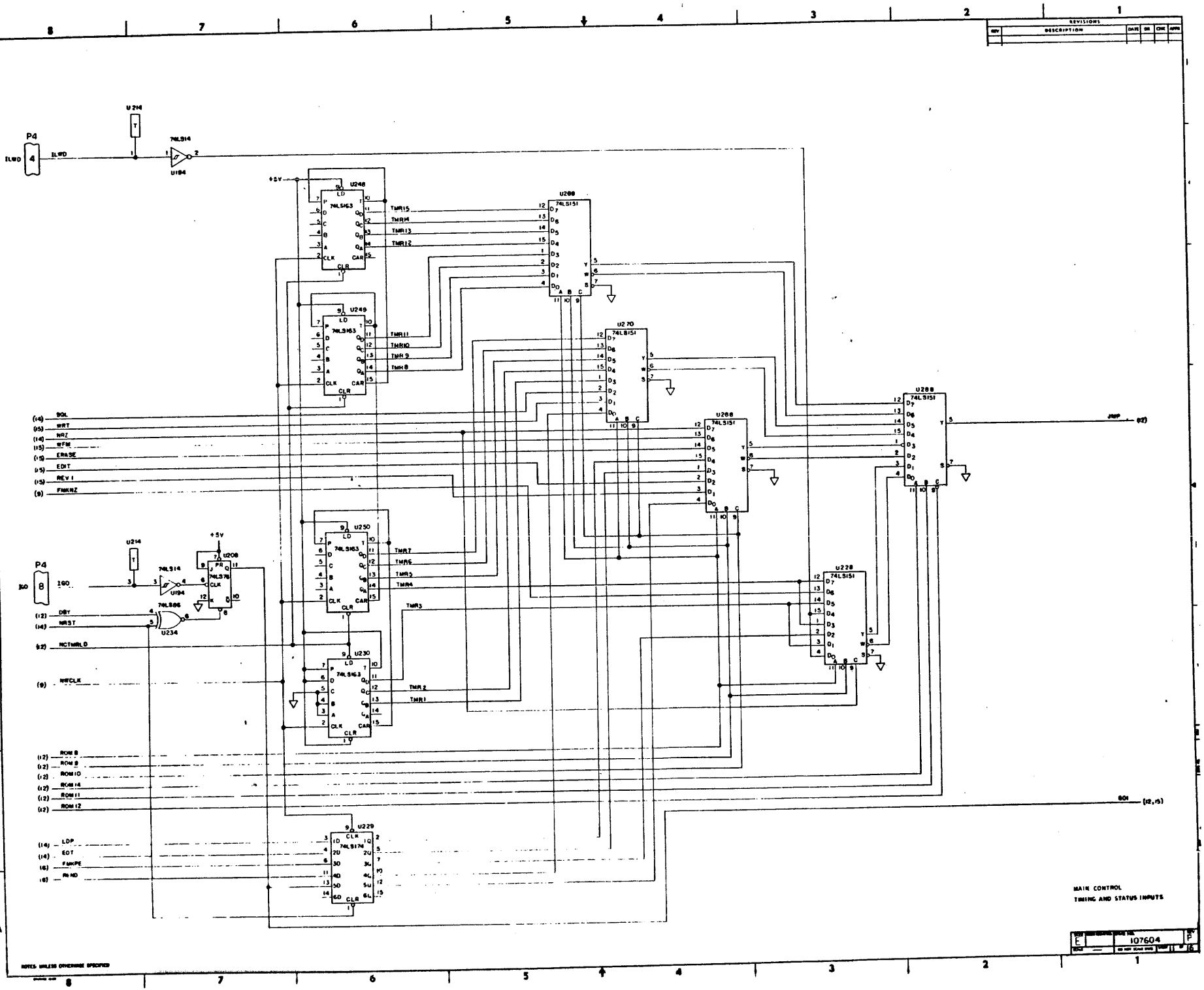

NCLR TIMER NZ
INCSTATENZ
NLDSTATENZ
U33
32 X 8 ROM
U51
74LS163
RCRN0
RCRN1
RCRN2
RCRN3
U13
74LS163
U14
74LS163
U11
74LS32
U8
74LS32
RTMRN21
RTMRN25
RTMRN27
RTMRN20
W2
RENDN2
U19
107649-XX
16X48X8 LOGIC ARRAY
CHARCNTEN
NCLRN2DATA
W4
U110
74LS11
LRCCLK
NRDS
NWCLK
NLRCR
CHARCNT
REV1
WCLK
P3
IRDS
U10
U130
74LS14
U50
74LS04
U90
74LS02
U30
74LS76
RDS1
RDS2
U34
74LS174
FMRNZ
MERNZ
RSTRNZ
CCG
RGATENZ1
PAR
NFMKDTNZ
+5V
NH=1 HEAD
CONTROL LOGIC
E
107604
P

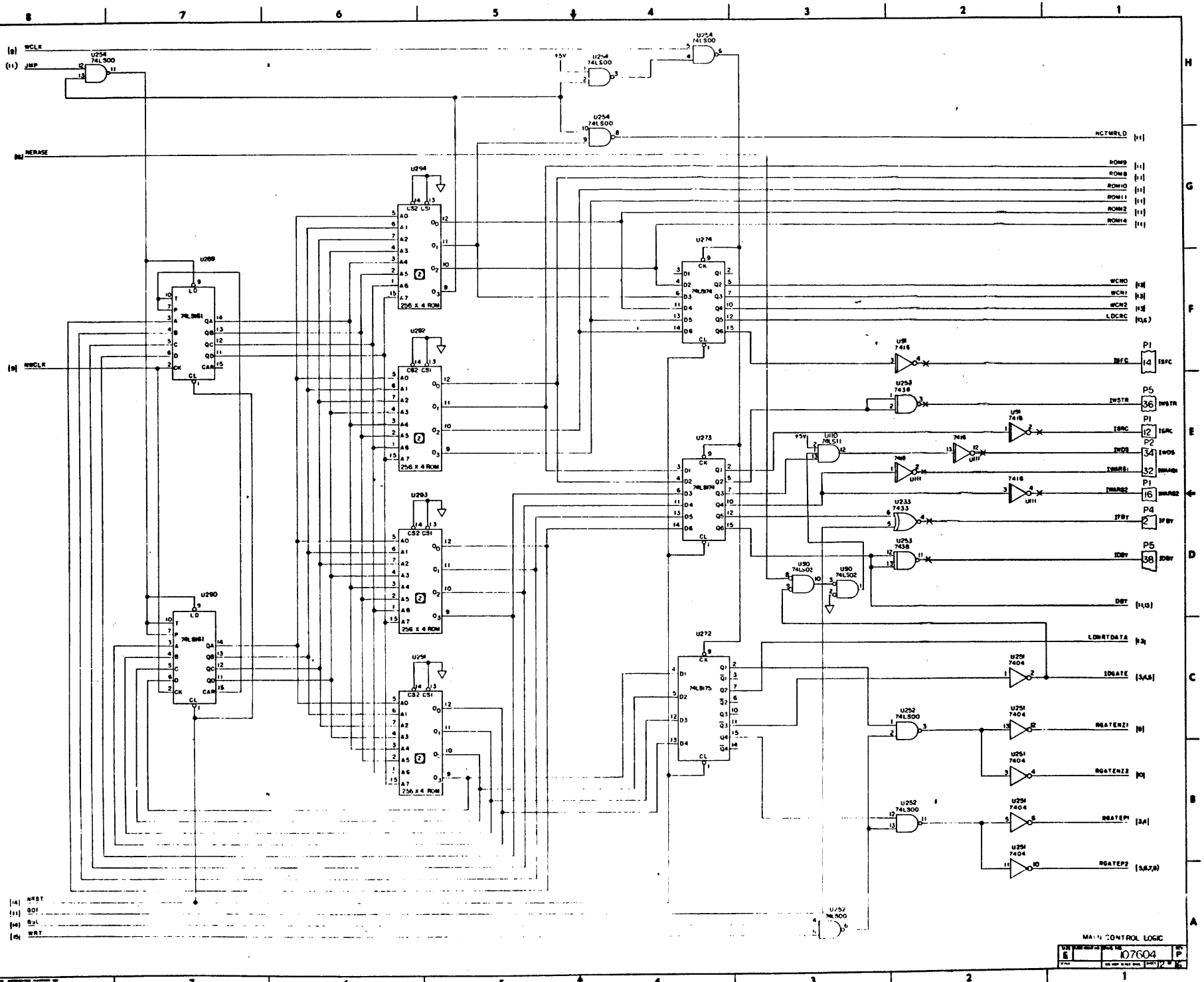


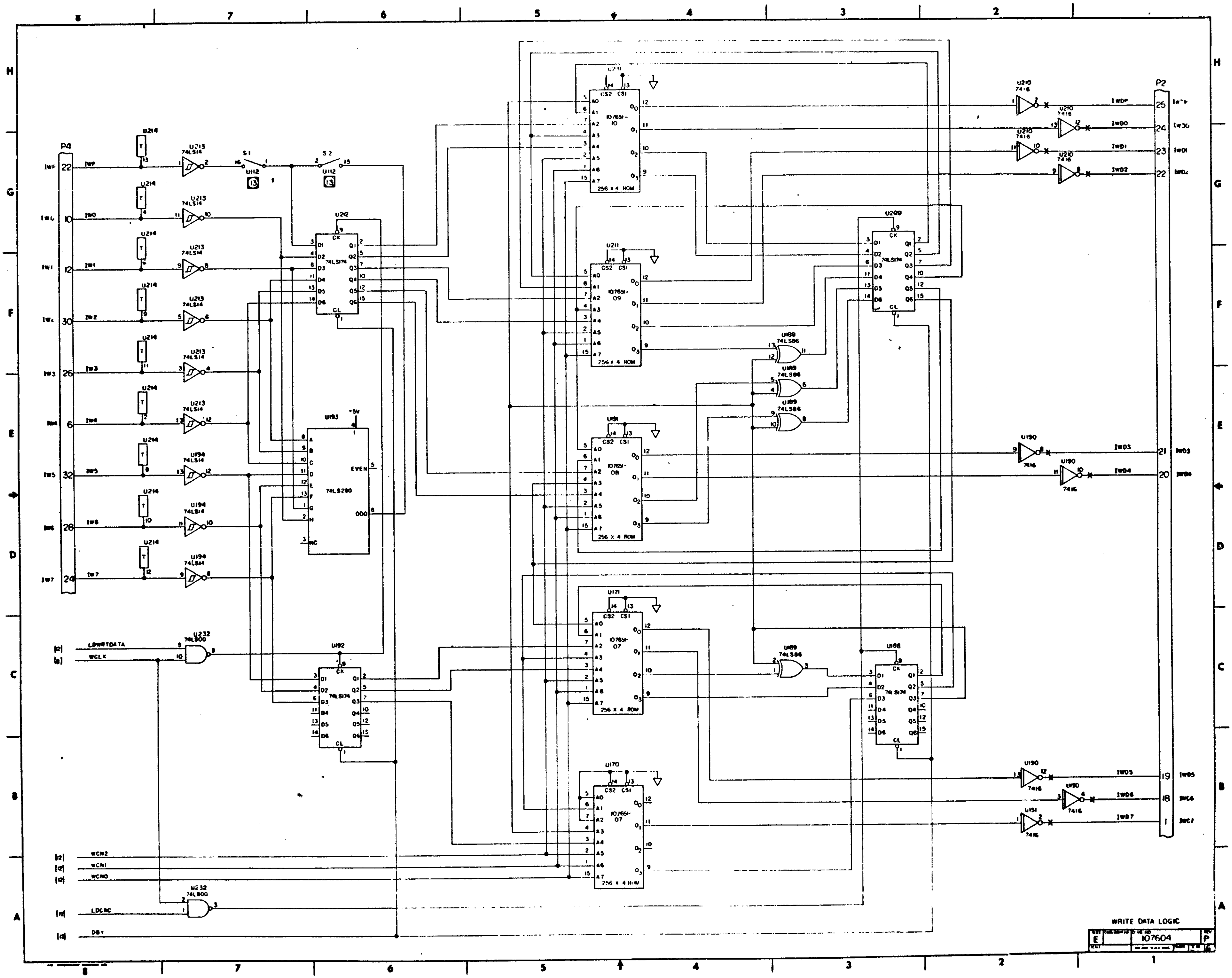
NRZI EPROM CHECK LOGIC

SIZE	DWG NO	REV
E	107604	P

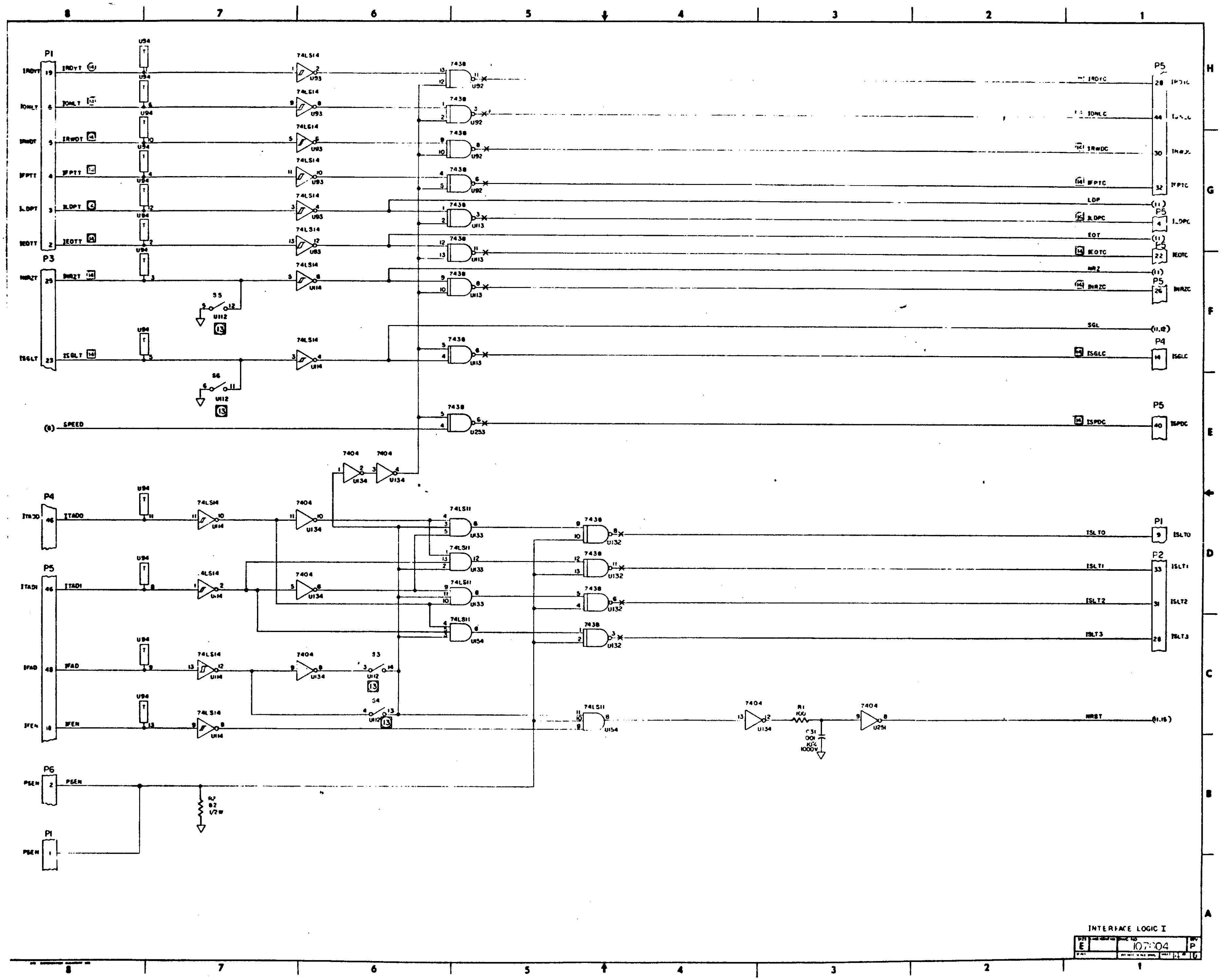
SCALE: NONE SHEET 10 OF 16


REVISIONS
DESCRIPTION
MAIN CONTROL
TIMING AND STATUS INPUTS
107604
NOTES: UNLESS OTHERWISE SPECIFIED


MAIN CONTROL LOGIC
E
107604
P



P4
P2
U214
U213
74LS14
U194
S1
S2
U112
U212
74LS174
U193
74LS280
EVEN
ODD
U232
74LS00
LDWRTDATA
WCLK
U192
U211
U210
7416
U209
10765I-10
10765I-09
10765I-08
10765I-07
256 X 4 ROM
U189
74LS86
U191
U190
U171
U170
U188
U151
IWP
IW0
IW1
IW2
IW3
IW4
IW5
IW6
IW7
IWDP
IWD0
IWD1
IWD2
IWD3
IWD4
IWD5
IWD6
IWD7
WCN2
WCN1
WCN0
LDCRC
DBY
+5V
WRITE DATA LOGIC
107604


P1
P3
P4
P5
P6
P2
U94
74LS14
7438
7404
74LS11
SPEED
PSEN
LDP
EOT
NRZ
SGL
NRST
ISLT0
ISLT1
ISLT2
ISLT3
R1
100
C31
.001
10%
1000V
R7
82
1/2W
INTERFACE LOGIC I
E
P

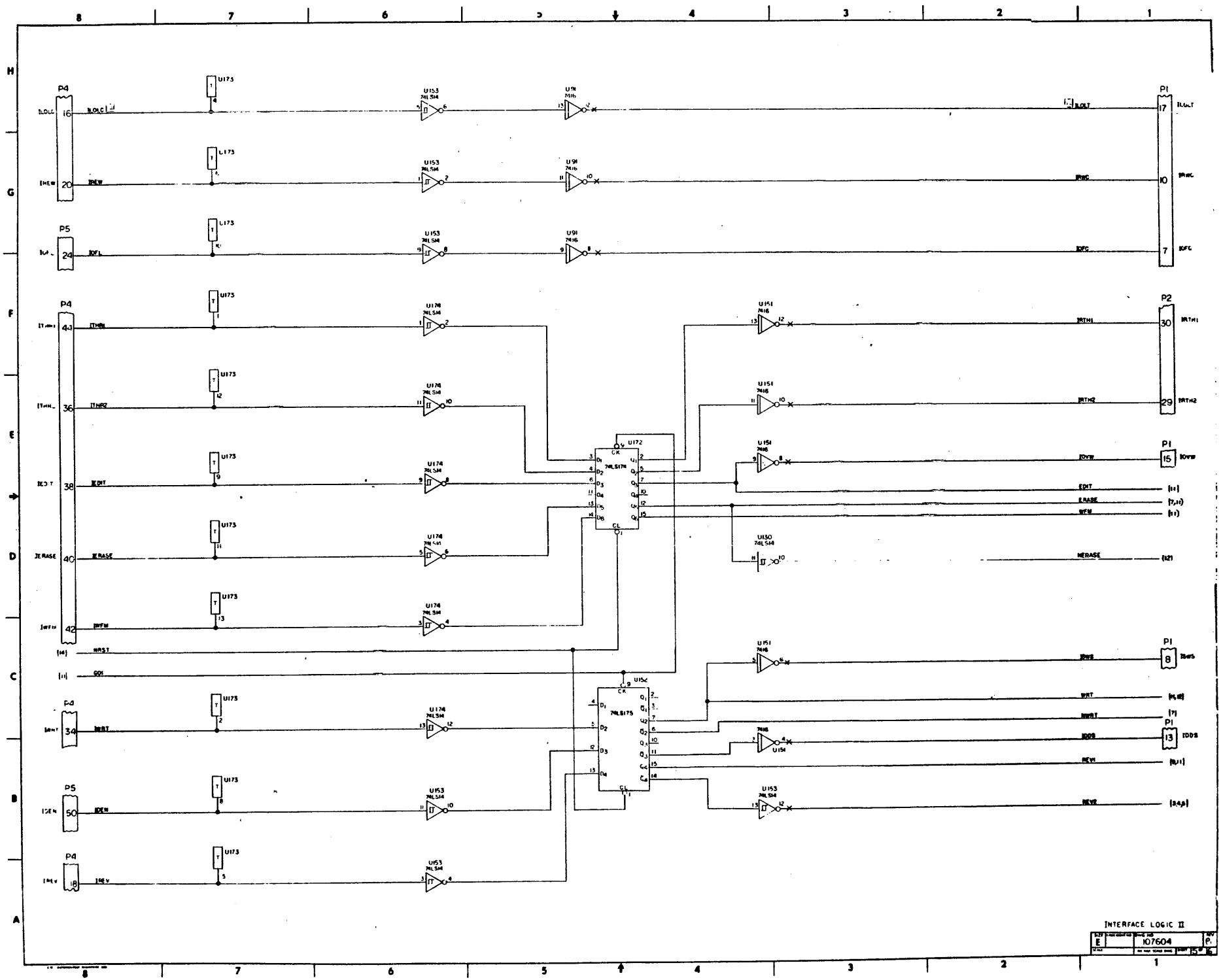
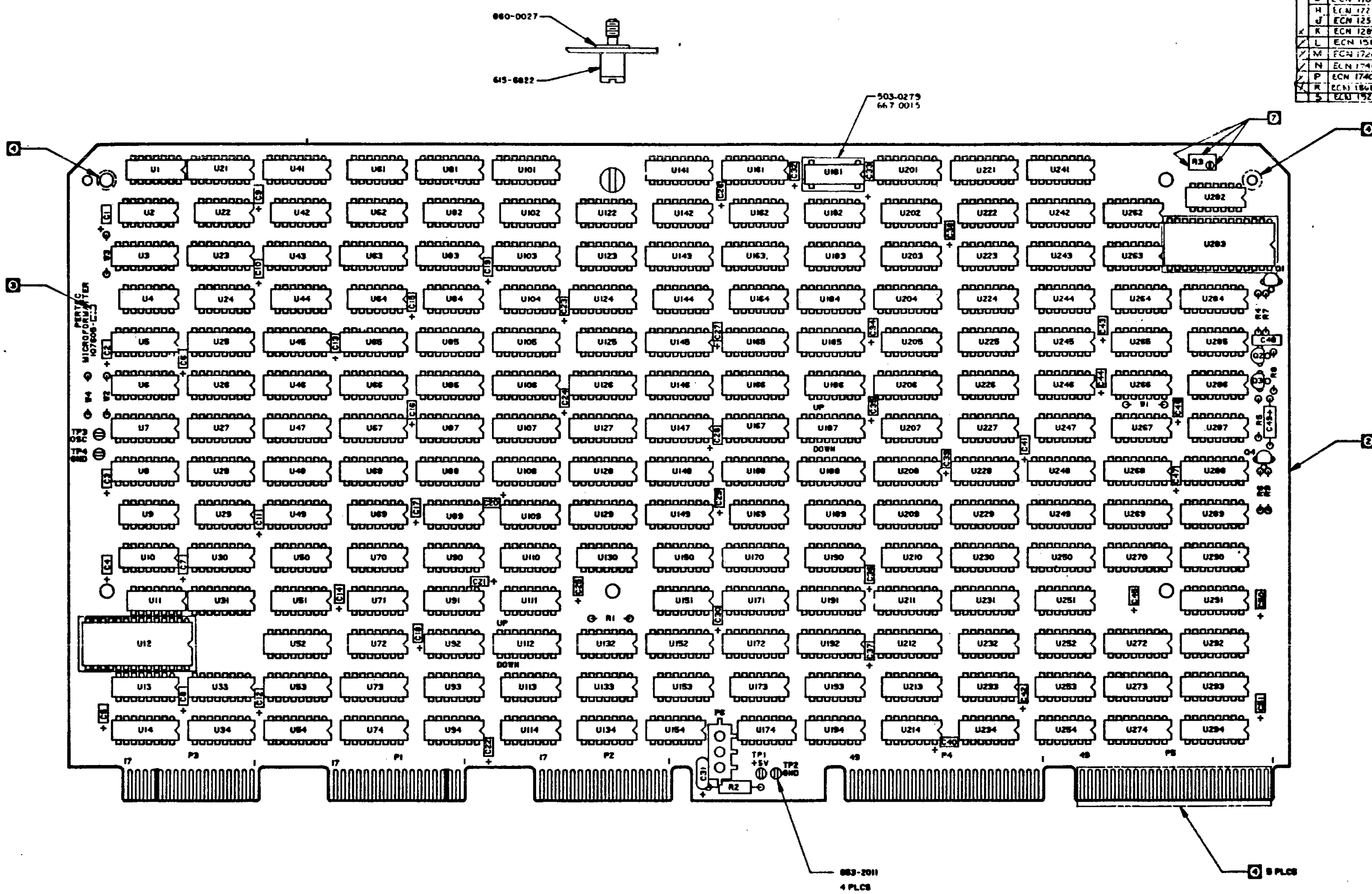

INTERFACE LOGIC II
E
107604

TABLE VIII (15)

MICROFORMATTER PROGRAMMABLE DEVICE CONFIGURATION TABLE

107605 VERSION	PROGRAMMABLE DEVICE REFERENCE DESIGNATION	ASSEMBLY REVISION LEVEL																		
		A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V
-01	U33	103983-03A	←																→	103983-03A
	U283	107649-01A	←																→	107649-01A
	U12	107649-02A	107649-02A	107649-02A/B	107649-02B	←													→	107649-02B
	U206	107650-01A	←																→	107650-01A
	U5,25,45,65,85,105,126,145,165	107651-01A	←																→	107651-01A
	U21,81,141	107651-02A	←																→	107651-02A
	U291	107651-03A	←				→	107651-03A	107651-03B	←	←	107651-03B	109361-01A	←					→	109361-01A
	U293	107651-04A	←				→	107651-04A	107651-04B	← ←	107651-04B	107651-04C	109362-01A	←					→	109362-01A
	U292	107651-05A/B	107651-05B	←			→	107651-05B	107651-05C	107651-05C	107651-05C/D	107651-05E	109363-01A	←				→	109363-01A	109363-02A
	U294	107651-06A	←				→	107651-06A	107651-06B	← ←	107651-06B	107651-06C	109364-01A	←				→	109364-01A	109364-02A
	U170	107651-07A	←																→	107651-07A
	U171	107651-07A	←																→	107651-07A
	U191	107651-08A	←																→	107651-08A
	U211	107651-09A	←																→	107651-09A
-01	U231	107651-10A	←																→	107651-10A
-02	U33	NOT USED	←																→	NOT USED
	U283	107649-01A	←																→	107649-01A
	U12	NOT USED	←																→	NOT USED
	U206	107650-01A	←																→	107650-01A
	U5,25,45,65,85,105,126,145,165	107651-01A	←																→	107651-01A
	U21,81,141	107651-02A	←																→	107651-02A
	U291	107651-03A	←				→	107651-03A	107651-03B	←	←	107651-03B	109361-01A	←					→	109361-01A
	U293	107651-04A	←				→	107651-04A	107651-04B	← ←	107651-04B	107651-04C	109362-01A	←					→	109362-01A
	U292	107651-05A/B	107651-05B	←			→	107651-05B	107651-05C	107651-05C	107651-05C/D	107651-05E	109363-01A	←				→	109363-01A	109363-02A
	U294	107651-06A	←				→	107651-06A	107651-06B	← ←	107651-06B	107651-06C	109364-01A	←				→	109364-01A	109364-02A
	U170	107651-07A	←																→	107651-07A
	U171	107651-07A	←																→	107651-07A
	U191	107651-08A	←																→	107651-08A
	U211	107651-09A	←				→												→	107651-09A
-02	U231	107651-10A	←																→	107651-10A
-03	U33	103983-03A	←															→	103983-03A	
	U283	NOT USED	←															→	NOT USED	
	U12	107649-02A	107649-02A	107649-02A/B	107649-02B	←												→	107649-02B	
	U206	NOT USED	←															→	NOT USED	
	U5,25,45,65,85,105,126,145,165	NOT USED	←															→	NOT USED	
	U21,81,141	NOT USED	←															→	NOT USED	
	U291	107651-03A	←					←	107651-03A	107651-03B	←	←	107651-03B	109361-01A	←			→	109361-01A	
	U293	107651-04A	←					←	107651-04A	107651-04B	← ←	107651-04B	107651-04C	109362-01A	←			→	109362-01A	
	U292	107651-05A/B	107651-05B	←				←	107651-05B	107651-05C	107651-05C	107651-05C/D	107651-05E	109363-01A	←			→	109363-01A	109363-02A
	U294	107651-06A	←					←	107651-06A	107651-06B	← ←	107651-06B	107651-06C	109364-01A	←			→	109364-01A	109364-02A
	U170	107651-07A	←																→	107651-07A
	U171	107651-07A	←																→	107651-07A
	U191	107651-08A	←																→	107651-08A
	U211	107691 09A	←																→	107651-09A
-03	U231	107651-10A	←																→	107651-10A
-04	U33	103983-04A	←					←	103983-04A	109380-01A	←				→	109380-01A				
	U283	107649-03A	←												→	107649-03A				
	U12	107649-04A	←												→	107649-04A				
	U206	107650-01A	←												→	107650-01A				
	U5,25,45,65,85,105,126,145,165	107651-01A	←												→	107651-01A				
	U21,81,141	107651-02A	←												→	107651-02A				
	U291	107651-03B	107651-03B	107651-11A	← ←	107651-11A	109371-01A	←							→	109371-01A				
	U293	107651-04B	107651-04B	107651-12A	107651-12A	107651-12B	109372-01A	←							→	109372-01A				
	U292	107651-05C	107651-05C	107651-13A	107651-13A	107651-13B	109373-01A	←							109373-01A	109373-02A				
	U294	107651-06B	107651-14B	107651-14A	107651-14A	107651-14B	109374-01A	←							→	109374-01A	109374-02A			
	U170	107651-07A	←												→	107651-07A				
	U171	107651-07A	←												→	107651-07A				
	U191	107651-08A	←												→	107651-08A				
	U211	107651-09A	←												→	107651-09A				
-04	U231	107651-10A	←												→	107651-10A				

	REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK	APPR
	A. ERN 8-YZ PRE-PROD RELEASE; B. ECN 9780 C. ECN 9868A & ERN 8-8Z PROD RELEASE D. ECN 10240				
E	ECN 10874 REPLOT				
F	ECN 11134				
G	ECN 11836				
H	ECN 12251				
J	ECN 12519C				
K	ECN 12894		MP		
L	ECN 15868		IS		
M	ECN 17264				
N	ECN 17403				
P	ECN 17406				
R	ECN 18682		AS		
S	ECN 19202				



SCHEMATIC: 107604
SPECIFICATION:
REF DWGS:

PART NO. 107605- REV

7. APPLY A BEAD OF ADHESIVE PART NO. 667-0034 ALONG THREE (3) EDGES AT BASE OF COMPONENT.
6. REMOVED
5. REMOVED
4. MASK AREAS SHOWN DURING FLOW SOLDER OPERATION.
3. MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN.
2. THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 107606-01 REV H AND SUBSEQUENT.
1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON
FT7000	
APPLICATION	

DR. CADDS — SIGNATURES / DATE

FINISH — SEE L/M

PERTEC
a division of Pertec Computer Corporation

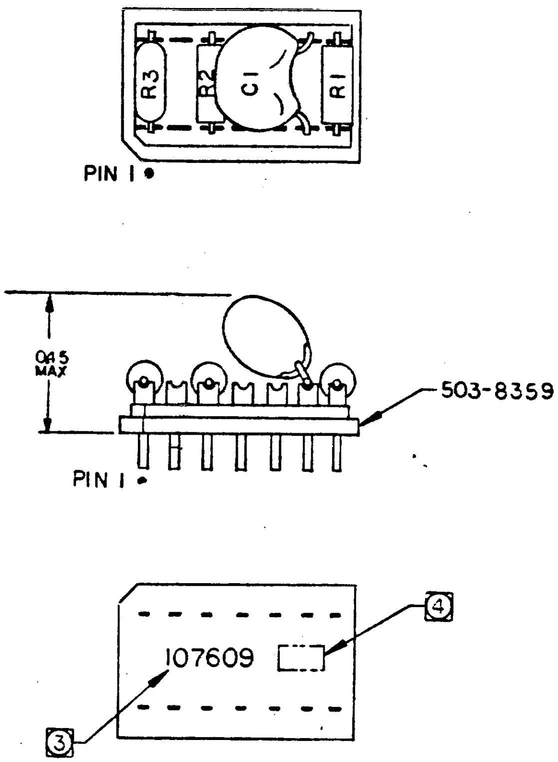
TITLE: PCBA MICROFORMATTER

SIZE: E | CODE IDENT NO: 32097 | DWG NO: 107605 | REV: S

SCALE: 2/1 | SHEET 1 OF 1

CADDS

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 8-WU PROD RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
B	ECN 9707	[illegible]	[illegible]	[illegible]	[illegible]



ASSY VERSION NO.	TAPE SPEED (IPS)	2 C1 VALUE (PF)	2 C1 PART NO.	1 R1 VALUE (OHM)	1 R1 PART NO.	1 R2 VALUE (OHM)	1 R2 PART NO.	1 R3 VALUE (OHM)	1 R3 PART NO.
-01	12.5	750	130-7515	2370	107-2371	3480	107-3481	1620	107-1621
-02	18.75	750	130-7515	1210	107-1211	1780	107-1781	825	107-8250
-03	22.5	470	130-4715	1960	107-1961	1960	107-1961	909	107-9090
-04	25	470	130-4715	1620	107-1621	1470	107-1471	681	107-6810
-05	37.5	330	130-3315	1470	107-1471	1000	107-1001	464	107-4640
-06	45	330	130-3315	1100	107-1101	750	107-7500	348	107-3480
-07	75	220	130-2215	750	107-7500	348	107-3480	162	107-1620
-08	112.5	100	130-1015	1470	107-1471	316	107-3160	147	107-1470
-09	125	100	130-1015	1100	107-1101	261	107-2610	121	107-1210

4. MARK VERSION NO. & REV LEVEL AS SHOWN.
3. MARK ASSEMBLY NO. AS SHOWN.
2. CAPACITORS ARE ±5%, 500 WDC.
1. RESISTORS ARE ±1%, 1/8W.

NOTES: UNLESS OTHERWISE SPECIFIED

TOP BILL FT8000A
NEXT ASSY | 1ST USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX .010

FINISH:
MATL:

SIGNATURES	DATE
DR T. Wilson	[illegible]
CHK [illegible]	1/5/76
DES	
ENGR	
PROJ. ENGR [illegible]	[illegible]

PERTEC
PERIPHERAL EQUIPMENT DIVISION

TITLE
PLUG ASSY, MICROFORMATTER TRACKING OSCILLATOR

SIZE C | CODE IDENT NO. | DWG NO. 107609 | REV B
SCALE 4-1 | DO NOT SCALE DWG | SHEET 1 OF 1

REV. B
DWG. NO. 107609

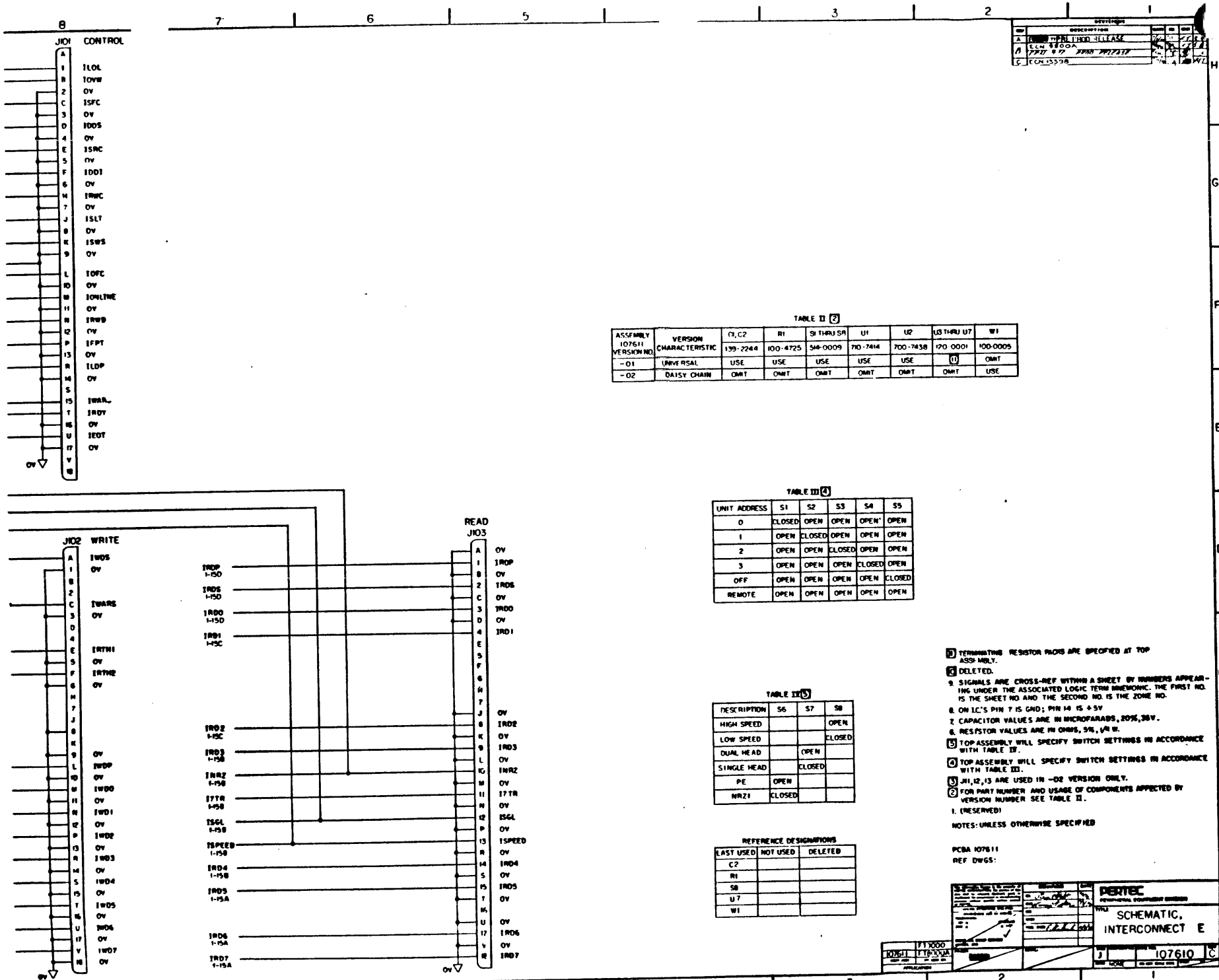


TABLE II [2]

ASSEMBLY 107611 VERSION NO.	VERSION CHARACTERISTIC	C1, C2	R1	S1 THRU S8	U1	U2	U3 THRU U7	W1
		139-2244	100-4725	548-0009	710-7414	700-7438	120-0001	100-0005
-01	UNIVERSAL	USE	USE	USE	USE	USE	[1]	OMIT
-02	DAISY CHAIN	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	USE

TABLE III [4]

UNIT ADDRESS	S1	S2	S3	S4	S5
0	CLOSED	OPEN	OPEN	OPEN	OPEN
1	OPEN	CLOSED	OPEN	OPEN	OPEN
2	OPEN	OPEN	CLOSED	OPEN	OPEN
3	OPEN	OPEN	OPEN	CLOSED	OPEN
OFF	OPEN	OPEN	OPEN	OPEN	CLOSED
REMOTE	OPEN	OPEN	OPEN	OPEN	OPEN

TABLE IV [5]

DESCRIPTION	S6	S7	S8
HIGH SPEED			OPEN
LOW SPEED			CLOSED
DUAL HEAD		OPEN	
SINGLE HEAD		CLOSED	
PE	OPEN		
NRZI	CLOSED		

REFERENCE DESIGNATIONS

LAST USED	NOT USED	DELETED
C2		
R1		
S8		
U7		
W1		

[3] TERMINATING RESISTOR PACKS ARE SPECIFIED AT TOP ASSEMBLY.

[4] DELETED.

9. SIGNALS ARE CROSS-REF WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO AND THE SECOND NO. IS THE ZONE NO.

8. ON IC'S PIN 7 IS GND; PIN 14 IS +5V

7. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 30V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 W.

[5] TOP ASSEMBLY WILL SPECIFY SWITCH SETTINGS IN ACCORDANCE WITH TABLE IV.

[4] TOP ASSEMBLY WILL SPECIFY SWITCH SETTINGS IN ACCORDANCE WITH TABLE III.

[3] J11, J12, J13 ARE USED IN -02 VERSION ONLY.

[2] FOR PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER SEE TABLE II.

1. (RESERVED)

NOTES: UNLESS OTHERWISE SPECIFIED

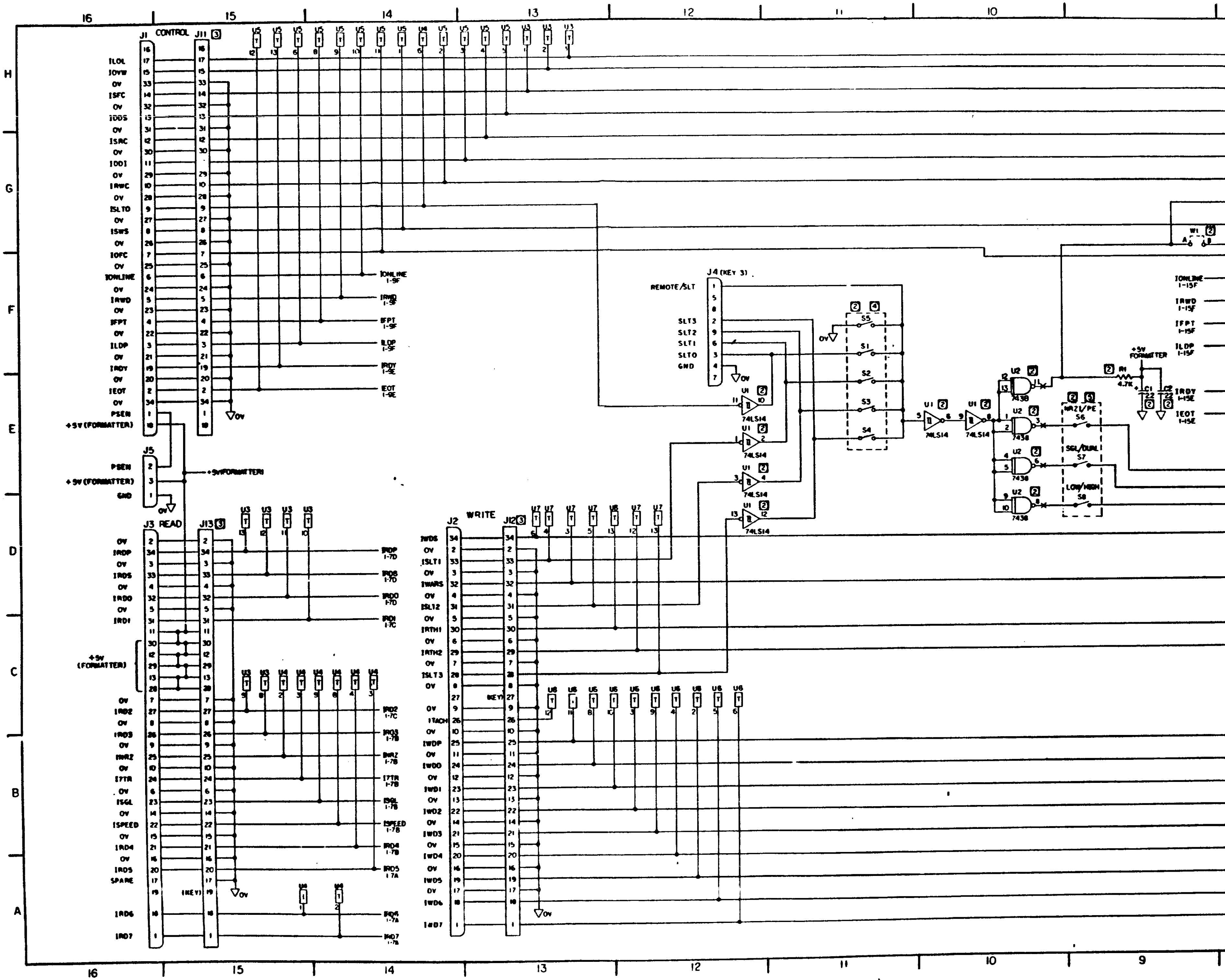
PCBA 107611

REF DWGS:

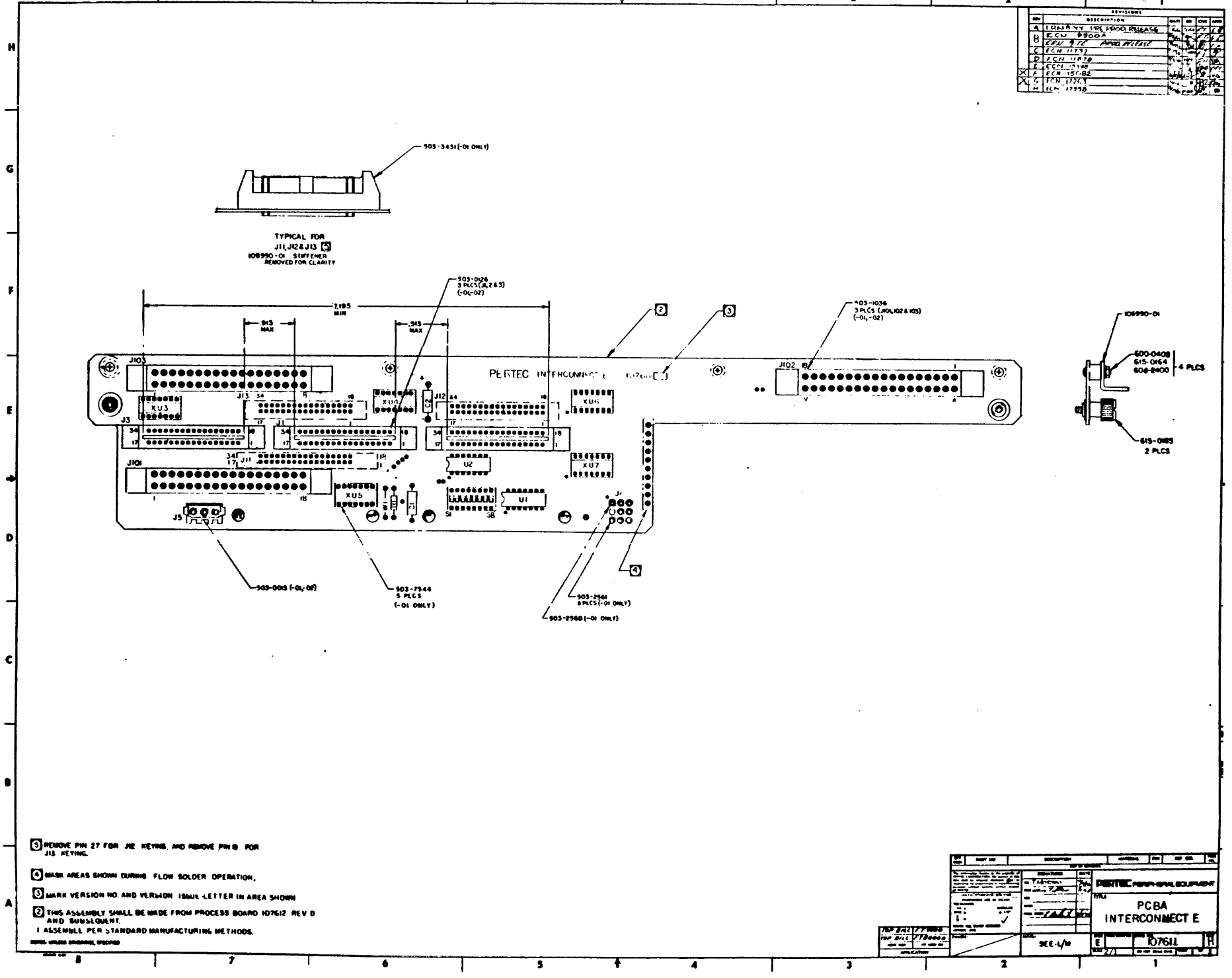
PERTEC

SCHEMATIC, INTERCONNECT E

107610 C



J1 CONTROL
J11
ILOL
IOVW
ISFC
IODS
ISRC
IODI
IRWC
ISLTO
ISWS
IOFC
IONLINE
IRWD
IFPT
ILDP
IRDY
IEOT
PSEN
+5V (FORMATTER)
J5
GND
+5V(FORMATTER)
IONLINE 1-9F
IRWD 1-9F
IFPT 1-9F
ILDP 1-9F
IRDY 1-9E
IEOT 1-9E
J3 READ
J13
IRDP
IRDS
IRD0
IRD1
IRD2
IRD3
INRZ
I7TR
ISGL
ISPEED
IRD4
IRD5
SPARE
IRD6
IRD7
(KEY)
J2 WRITE
J12
IWDS
ISLT1
IWARS
ISL12
IRTH1
IRTH2
ISLT3
ITACH
IWDP
IWD0
IWD1
IWD2
IWD3
IWD4
IWD5
IWD6
IWD7
KEY
J4 (KEY 3)
REMOTE/SLT
SLT3
SLT2
SLT1
SLT0
GND
S5
S1
S2
S3
S4
74LS14
7438
NRZI/PE
S6
SGL/DUAL
S7
LOW/HIGH
S8
R1
4.7K
C1
C2
+5V FORMATTER
W1
IONLINE 1-15F
IRWD 1-15F
IFPT 1-15F
ILDP 1-15F
IRDY 1-15E
IEOT 1-15E



[5] REMOVE PIN 27 FOR J12 KEYING, AND REMOVE PIN 8 FOR J13 KEYING.

[4] MASK AREAS SHOWN DURING FLOW SOLDER OPERATION.

[3] MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN

[2] THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 107612 REV D AND SUBSEQUENT.

1 ASSEMBLE PER STANDARD MANUFACTURING METHODS.

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
INTERCONNECT E

SIZE E | 107611 | REV H

SHEET 2/1

SEE-L/M

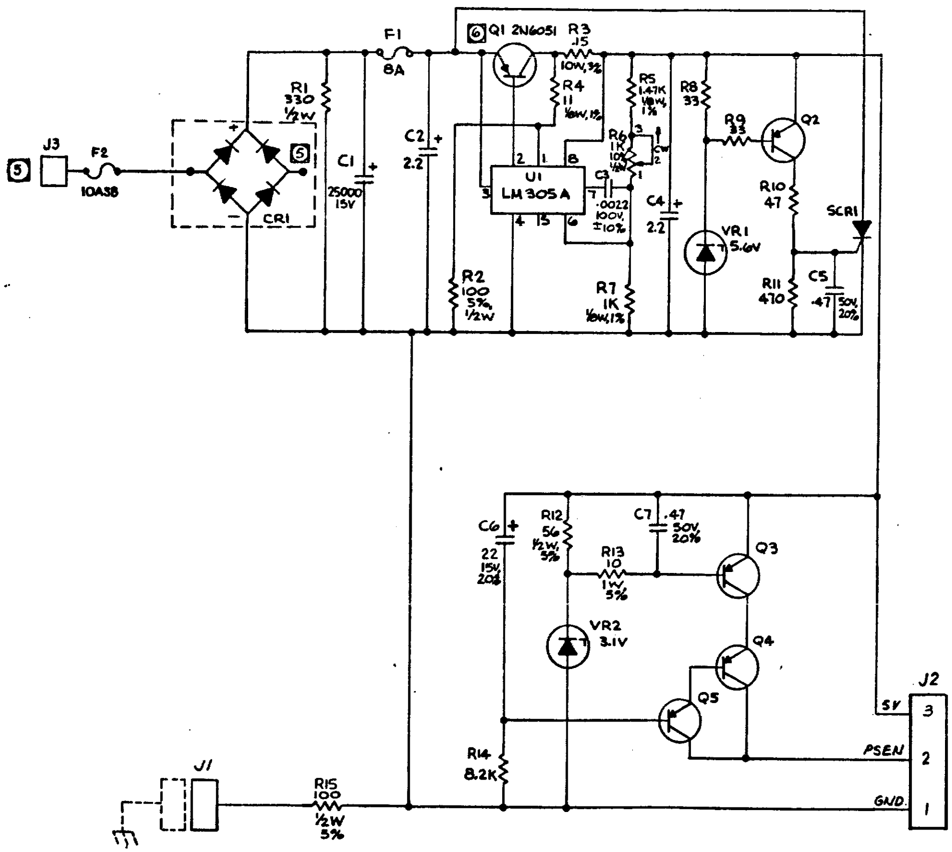


TABLE I

PART NO.	REF DES
101-3315	R1
101-1015	R2,15
118-0013	R3
107-0110	R4
107-1471	R5
124-1021	R6
107-1001	R7
100-3305	R8, 9
100-4705	R10
100-4715	R11
101-5605	R12
102-1005	R13
100-8225	R14
134-2591	C1
139-2244	C2, 4
131-2220	C3
135-4742	C5, 7
139-2262	C6
200-6051	Q1
200-4402	Q2, 3, 4, 5
330-0565	VR1
330-0395	VR2
201-0126	SCR1
400-0305	U1
320-2510	CR1
663-8080	F1
663-3700	F2

REVISIONS

	REV	DESCRIPTION	DATE	DR	CHK	APPR
	1	PROTOTYPE	[illegible]	TM		
	2	REVERSE PINS 1&3 ON J3				
	A	ERN 8-TN PROD RELEASE	[illegible]	SK	[illegible]	F.D.
	B	ECN 9965	5/26/77	EL	[illegible]	F.D.
X	C	ECN 14861	[illegible]	L.S.	[illegible]	[illegible]
	D	ECN 15869	[illegible]	PAD	[illegible]	KG

6 COMPONENT IS MOUNTED ON HEATSINK.

5 TRANSFORMER OUTPUT LEADS ARE CONNECTED TO FAST-ON TERMINALS ON THE BRIDGE RECTIFIER (CR1) & CONNECTOR (J3).

4. PNP TRANSISTORS ARE 2N4402.

3. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.

2. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

1 FOR PART NUMBER SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY NUMBER- 107615

REFERENCE DRAWINGS-

QTY. REQD.	PART NO.	DESCRIPTION	MATERIAL	REF. DES.	ITEM NO.

LIST OF MATERIAL

NEXT ASSY	USED ON
107615	T-FMTR

APPLICATION

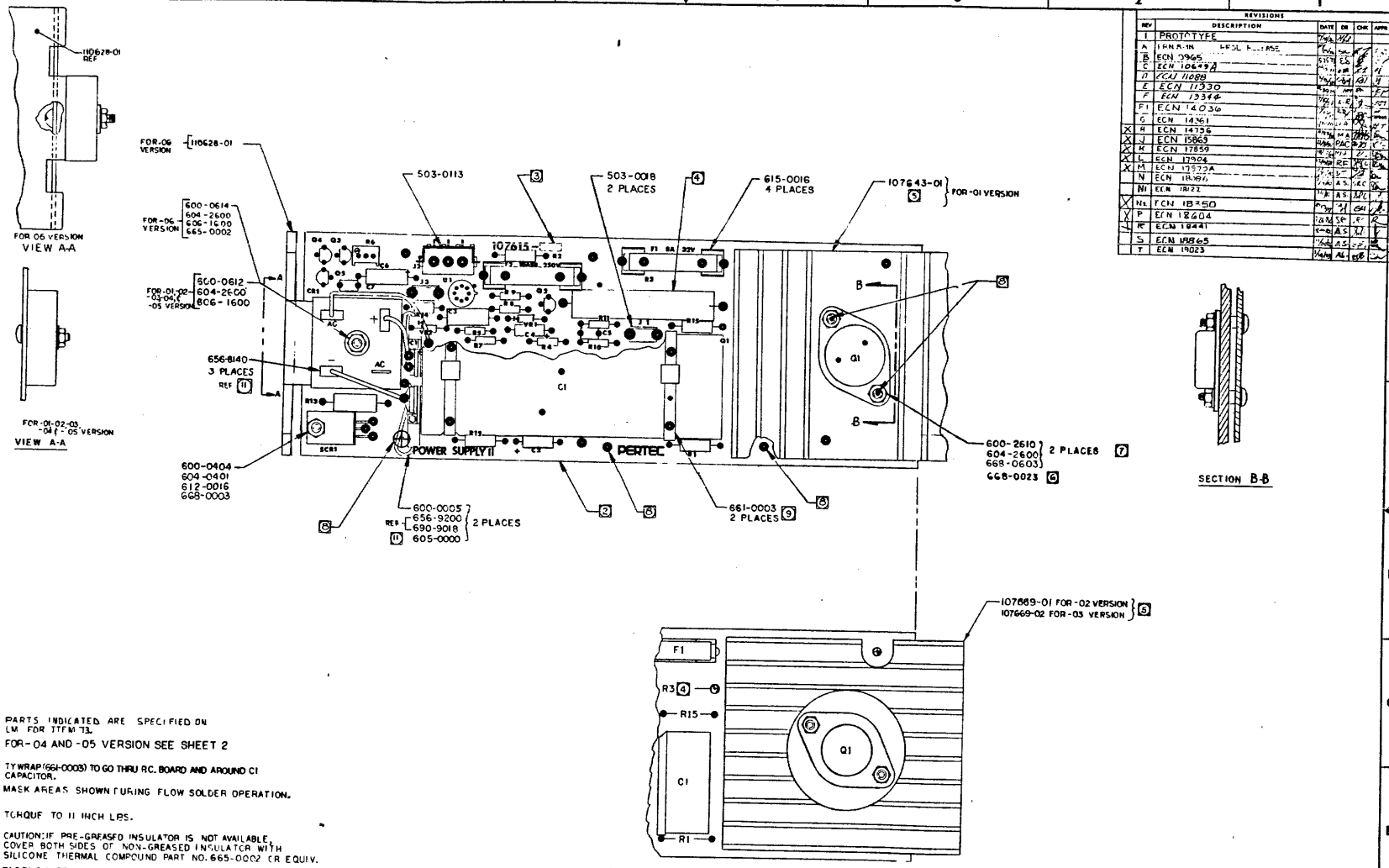
PERTEC PERIPHERAL EQUIPMENT

TITLE: SCHEMATIC, POWER SUPPLY II

DRAWN: T. HORTON

SIZE: D | CODE IDENT NO. 32097 | DWG NO. 107614 | REV D

SCALE: NONE



REV	DESCRIPTION	DATE	DR	CHK	APPR
	I PROTOTYPE				
	A TRANS-IN FROM RELEASE				
	B ECN 3965				
	C ECN 10649A				
	D ECN 11088				
	E ECN 11330				
	F ECN 13346				
	F1 ECN 14036				
	G ECN 14361				
X	H ECN 14756				
X	J ECN 15869				
X	K ECN 17859				
X	L ECN 17904				
X	M ECN 17979A				
	N ECN 18087				
	N1 ECN 18122				
X	N2 ECN 18350				
X	P ECN 18404				
	R ECN 18441				
	S ECN 18865				
	T ECN 19023				

[11] PARTS INDICATED ARE SPECIFIED ON LM FOR ITEM 73.

[6] FOR-04 AND -05 VERSION SEE SHEET 2

[9] TYWRAP (668-0003) TO GO THRU PC BOARD AND AROUND C1 CAPACITOR.

[6] MASK AREAS SHOWN DURING FLOW SOLDER OPERATION.

[*] TORQUE TO 11 INCH LBS.

[5] CAUTION: IF PRE-GREASED INSULATOR IS NOT AVAILABLE, COVER BOTH SIDES OF NON-GREASED INSULATOR WITH SILICONE THERMAL COMPOUND PART NO. 665-0002 OR EQUIV.

[5] BEFORE INSTALLATION OF COMPONENTS-REMOVE ALL DIRT PARTICLES AND METAL FROM MOUNTING SURFACES.

[4] MAINTAIN MINIMUM AIR GAP OF .10 BETWEEN COMPONENT BODY AND BOARD.

[3] MARK VENDOR NO. AND VERSION ISSUE LETTER IN AREA SHOWN.

[2] THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 107616-01 REV F & SUBSEQUENT.

[1] ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTE: UNLESS OTHERWISE SPECIFIED

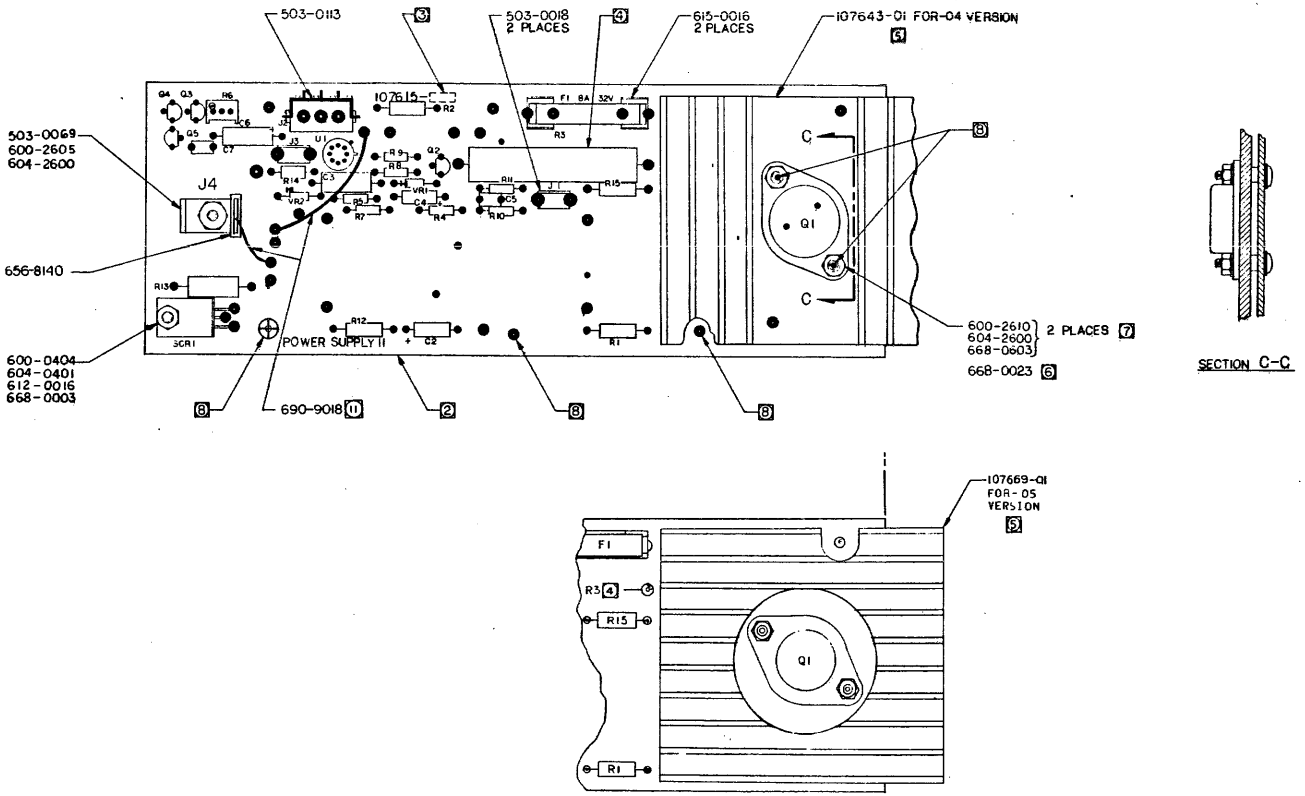
PERTEC PERIPHERAL EQUIPMENT

TITLE PCBA POWER SUPPLY II

SEE L/M

SIZE F | 107615 | REV T

SCALE 2/1


503-0113
3
503-0018
2 PLACES
4
615-0016
2 PLACES
107643-01 FOR-04 VERSION
5
503-0069
600-2605
604-2600
656-8140
600-0404
604-0401
612-0016
668-0003
J4
POWER SUPPLY II
690-9018 11
2
8
600-2610
604-2600
668-0603
2 PLACES 7
668-0023 6
C
Q1
SECTION C-C
107669-01
FOR-05
VERSION
9
F1
R3 4
R15
R1