MA 703510-A

PM-MFV11A
Multifunction
Board Manual

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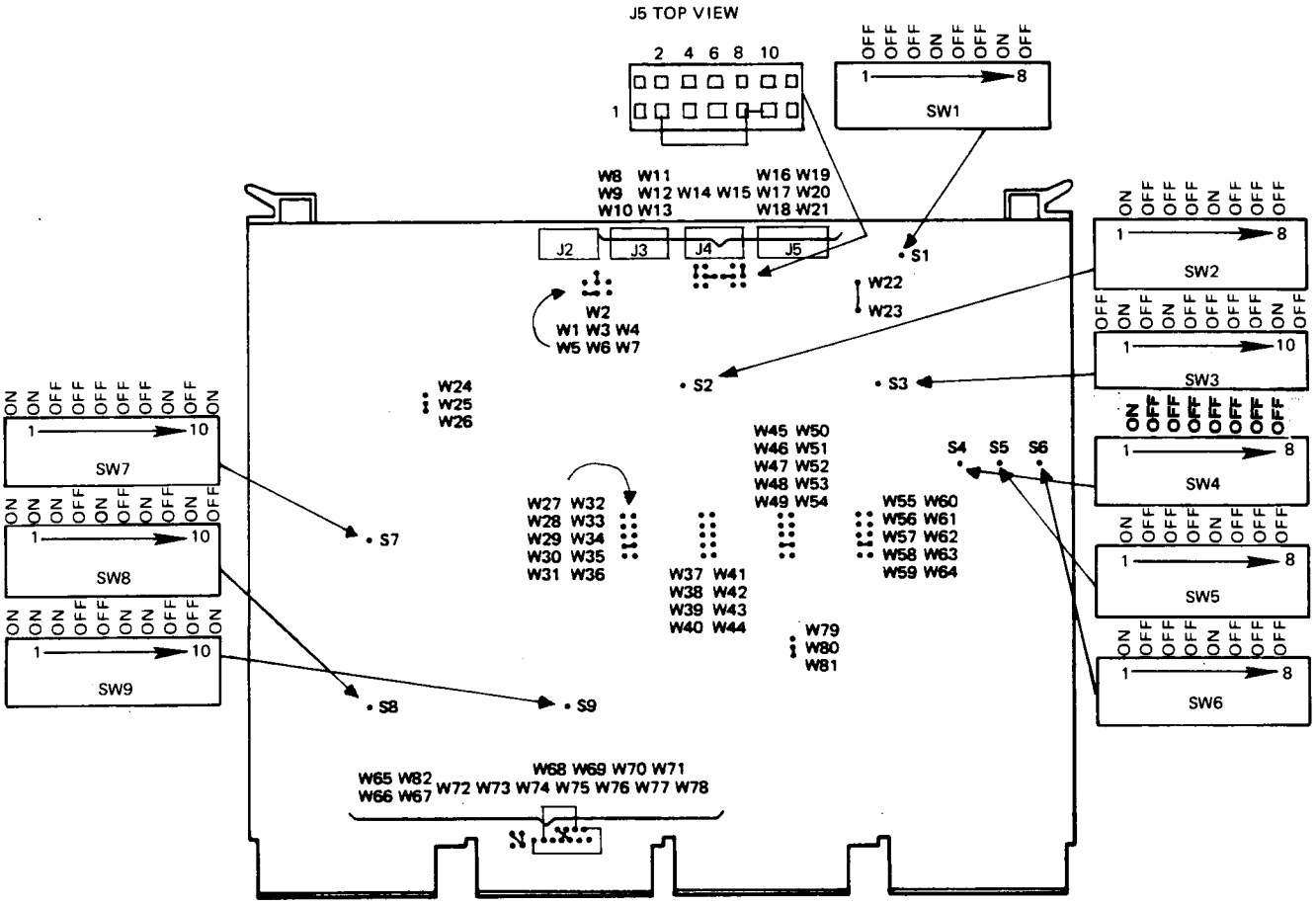
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PM-MFV11A (Q-BUS MULTI-OPTION) BOARD 703510A
SPO USER COMM. SUBSYSTEM PROCESSOR CHASSIS
TTD USER COMM. SUBSYSTEM PROCESSOR CHASSIS
(SU #1, SLOT #9, C-F)



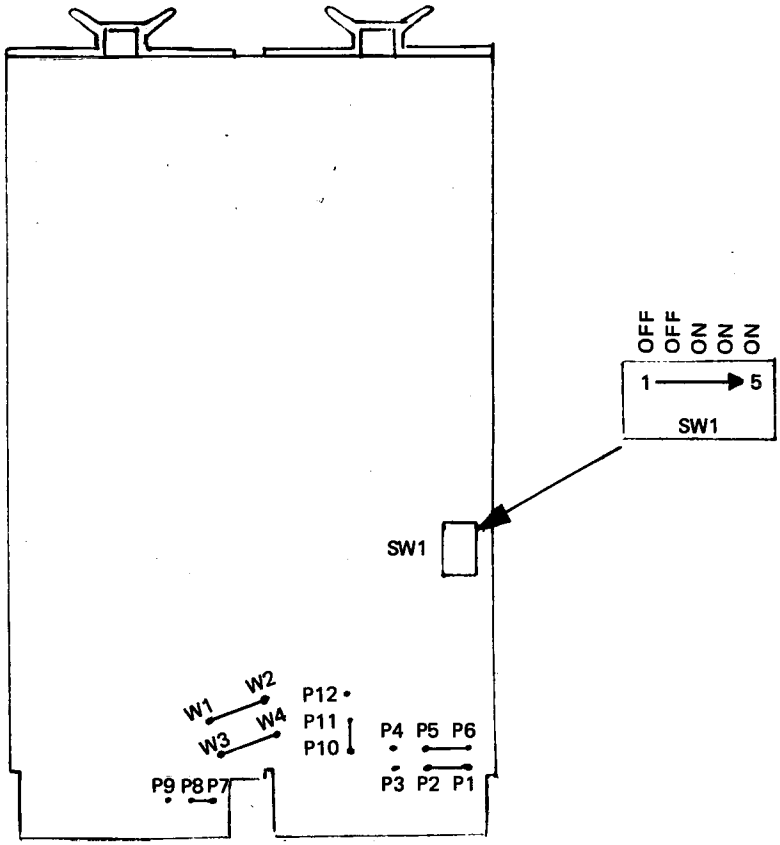
S = SWITCH
W = JUMPER

JUMPERS INSTALLED AS SHOWN

W2 - W3	W22 - W23	W67 - W82	J5.1 - J5.7
W5 - W6	W25 - W26	W68 - W76	J5.7 - J5.9
W8 - W9	W30 - W35	W69 - W75	
W12 - W14	W48 - W53	W70 - W73	
W15 - W17	W58 - W63	W71 - W72	
W19 - W20	W65 - W67	W80 - W81	

SWITCH POSITIONS AND REQUIRED JUMPERS

4TH DEC MEMORY BOARD M8044DB
SPO USER COMM. SUBSYSTEM PROCESSOR CHASSIS
(SU #1, SLOT #3, A-B)
TTD USER COMM. SUBSYSTEM PROCESSOR CHASSIS
(SU #1, SLOT #4, C-D)



JUMPERS	WIRE WRAP PINS JUMPERS TO
W1 - W2	P1 - P2
W3 - W4	P5 - P6
TWO SMALL JUMPERS AT THE BOTTOM OF THE BOARD WHICH ARE COVERED BY A PLASTIC RING	P10 - P11
	P7 - P8

STARTING ADDRESS = 96 KW
192 K BYTE
(OCTAL 600000 BYTE)

general information 1

1.1 INTRODUCTION

This manual provides the necessary information to install and operate the PM-MFV11A multi-function board manufactured by Plessey Peripheral Systems, Irvine, California 92714.

The information is arranged into four sections as follows:

Section 1 - GENERAL INFORMATION. This section contains a brief, general description of the PM-MFV11A and the specifications for the module.

Section 2 - INSTALLATION AND OPERATION. This section explains the procedures for equipment installation.

Section 3 - FUNCTIONAL DESCRIPTION. This section contains a detailed, functional description of the PM-MFV11A, including address selection and interfacing for this unit.

Section 4 - THEORY OF OPERATION. This section contains a circuit logic description of the PM-MFV11A.

DRAWING PACKAGE. A separate drawing package, MD 703510, is available. This document contains logic diagrams, schematics, and assemblies required for a complete understanding of the multi-function board.

1.2 GENERAL DESCRIPTION

The PM-MFV11A is a multi-function board designed for use with Plessey's LSI based microcomputer systems. It provides four Electronic Industry Association (EIA) RS232 ports which may be used for console device interface, serial printer, modem, and spare terminals, front panel control circuits, a 1024 word bootstrap Read Only Memory (ROM) program, self-test diagnostic, and a Line Time Clock (LTC) circuit. It can be used on the LSI-11 bus*.

*Trademark of Digital Equipment Corporation

1.3 FEATURES, PM-MFV11A MULTI-FUNCTION BOARD

- Fully Q-bus compatible
- User definable ports with user selection of:

  baud rate
  parity, data, and stop bits
  operation as console or non-console device
  full modem (RS-232) support
  serial line printer support

- Front panel circuitry for:

  BOOT, HALT/ENABLE, LTC ON/OFF switches
  RUN and DCON lights

- Bootstrap operation from on-board ROMs
- LTC control circuitry
- Central Processing Unit (CPU), memory, RX11, RK11, and console port diagnostics from on-board ROMs
- 12 Light-emitting diodes (LED) which indicate system and board status
- 120Ω Q-bus termination

1.4 SPECIFICATIONS

1.4.1 PHYSICAL SPECIFICATIONS

The PM-MFV11A is contained on a quad-wide multi-layer printed circuit board.

- Width: 10.4 inches (26.4cm)
- Height: 8.9 inches (22.6cm)

1.4.2 POWER REQUIREMENTS

- +5VDC @ 4A
- +12VDC @ 0.38A

1.4.3 ENVIRONMENTAL SPECIFICATIONS

Temperature

Operating:	0° C to 50° C
Non-operating:	-40° C to 85° C

Relative humidity: 10 to 90% non-condensing

installation and operation 2

2.1 UNPACKING AND INSPECTION

The PM-MFV11A is shipped in a special carton designed to minimize shock and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment. Remove all packing materials, and visually inspect the PM-MFV11A for physical damage.

2.2 INSTALLATION (FACTORY STANDARD CONFIGURATION)

Refer to Figure 2-1 for switch and jumper locations.

The factory standard configuration is as follows:

- Port 1 console, address 177560-66, vector 60-64
- Port 2 1st spare DLV-11, address 176500-06, vector 300-04
- Port 3 2nd spare DLV-11, address 176510-16, vector 310-14
- Port 4 3rd spare DLV-11, address 176520-24, vector 320-24
- Bootstrap address 173000
- Line Time Clock (LTC) external (power supply) source, front panel control (manual), address 177546, vector 100
- Baud rate 9600 for all ports
- 8-data bits, 1-stop bit, no parity for all ports
- Console port framing error (i.e., BREAK character) asserts BHALTL

See Table 2-1 for switch settings and Table 2-2 for jumpers.

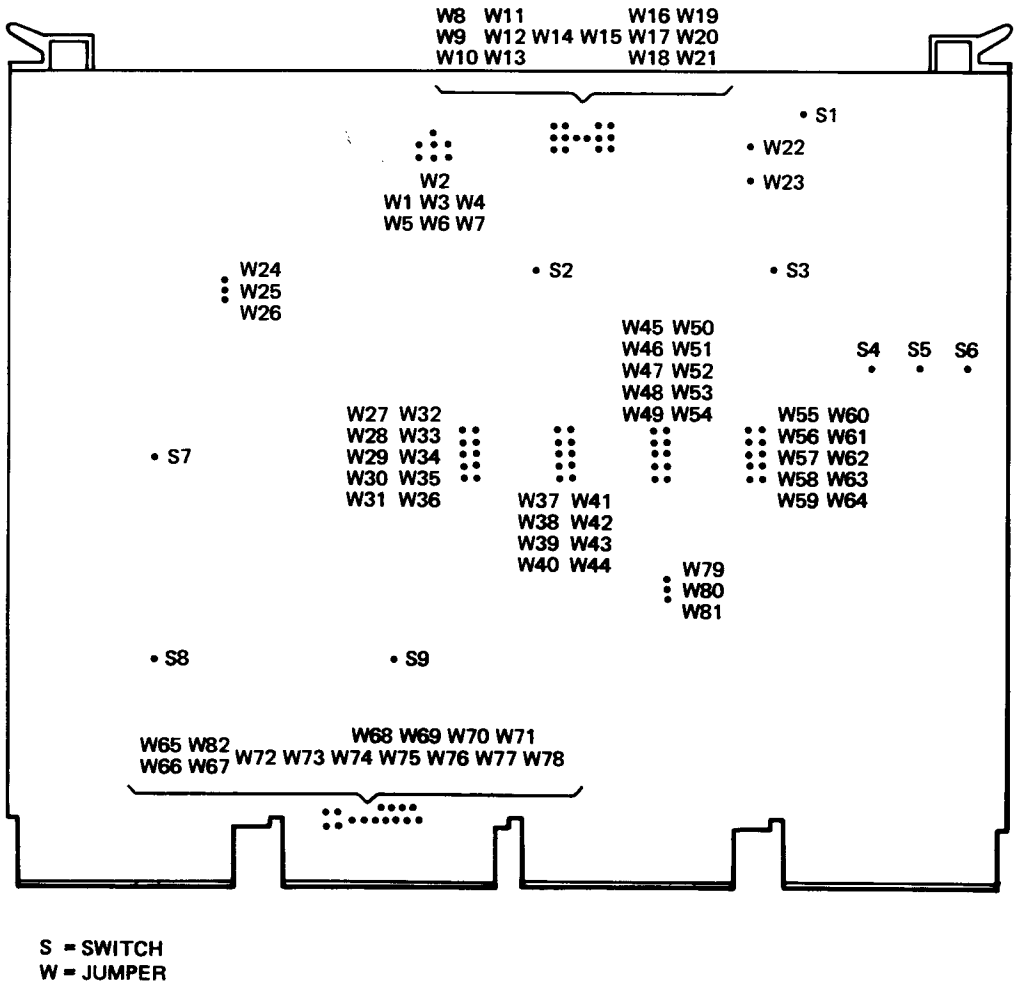


Figure 2-1. Switch and Jumper Locations

TABLE 2-1. FACTORY STANDARD SWITCH SETTINGS

SW# Pos	1	2	3	4	5	6	7	8	9
1	OFF	ON	OFF	ON	ON	ON	ON	ON	ON
2	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON
3	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
4	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
5	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF
6	OFF	OFF	OFF*	OFF	OFF	OFF	OFF	OFF	ON
7	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
8	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
9	---	---	ON	---	---	---	OFF	ON	OFF
10	---	---	OFF	---	---	---	ON	OFF	ON

--- = no switch position

Note

*K1 & L1 are wired together on all connectors on the MICRO-II backplane effectively shorting around this switch position.

TABLE 2-2. FACTORY STANDARD JUMPERS

W82-W67-W65	W2 -W3
W76-W78	W5 -W6
W75-W69	W8 -W9
W73-W70	W12-W14
W72-W71	W15-W17
W80-W81	W19-W20
W25-W26	W35-W30
W63-W58	W53-W48

2.3 PORT CONFIGURATION

The PM-MFV11A contains four serial data interfaces (ports) with seven possible addresses. These ports are independently configurable for address, vector, and data word characteristics. The four ports can be used in any way that the user desires. However, if a console is desired, it should be placed in Port #1. If a modem or line printer are required, they must be placed in Port #2 and #3, respectively. Port #4 can be used for any asynchronous serial line device. Refer to Tables 2-3 thru 2-6 for set-up information.

TABLE 2-3. CHANNEL ADDRESSES, DEVICES, AND PORTS

Devices				Channels				
Addr	Device	Std Vec	W/W Post	Port	W/W Post	Conn	UART	Use
177560	console	(60)	W76	1	W68	J2	U65	console
177514	LP	(200)*	W78	2	W69	J1	U66	modem
175610	modem	(300)	W77	3	W70	J3	U67	line printer
176500	ch A	(300)	W75	4	W71	J4	U68	asynchronous serial line device
176510	ch B	(310)	W73					
176520	ch C	(320)	W72					
176530	ch D	(330)	W74					

*SW7-10 must be OFF or the vector will be 204.

Note

The seven addresses may be mapped into the four ports in any way; however, if remote DLV (modem) or line printer operation is desired, their addresses must be mapped into channels 2 and 3, respectively.

TABLE 2-4. VECTORS, PORTS, AND BITS

Port	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	(Bit 2)	Norm
1	S9-1	S9-2	S9-3	S9-4	S9-5	S9-6	RQDISABLE 4	(60)
2	S9-7	S9-8	S9-9	S9-10	S8-1	S8-2	RQDISABLE 6	(300)
3	S8-3	S8-4	S8-8	S8-5	S8-7	S8-6	RQDISABLE 2	(310)
4	S8-9	S8-10	S7-4	S7-1	S7-3	S7-2	RQDISABLE 0	(320)

for 60 ON ON ON off off ON

Note

A switch in the "ON" position is a logical "0".

TABLE 2-5. BAUD RATE SELECTION

(The XMTR and RCVR for Port 1 are tied together and controlled by SW 1-4 only)

Pos:	4 8	3 7	2 6	1 5	(RCVR) (XMTR)
Baud Rate					
50	ON	ON	ON	ON	
75	ON	ON	ON	OFF	
110	ON	ON	OFF	ON	
134.5	ON	ON	OFF	OFF	
150	ON	OFF	ON	ON	
300	ON	OFF	ON	OFF	
600	ON	OFF	OFF	ON	
1,200	ON	OFF	OFF	OFF	
1,800	OFF	ON	ON	ON	
2,000	OFF	ON	ON	OFF	
2,400	OFF	ON	OFF	ON	
3,600	OFF	ON	OFF	OFF	
4,800	OFF	OFF	ON	ON	
7,200	OFF	OFF	ON	OFF	
9,600	OFF	OFF	OFF	ON	
19,200	OFF	OFF	OFF	OFF	

Note

Since the receiver is not independent from the transmitter on Port 1, only SW4 positions 1-4 are used to set that port's baud rate.

TABLE 2-6. SETTINGS FOR EACH PORT

Universal Asynchronous Receiver Transmitter (UART) Configuration

(The indicated jumper is installed)

Feature	Port 1 (LA120)	Port 2	Port 3 (VT-100)	Port 4
stop bits:				
1	W35-W30	N/A*	W53-W48	W63-W58
2	(out)	N/A*	(out)	(out)
data bits:				
5	W34-W29 W33-W28	W43-W39 W42-W38	W52-W47 W51-W46	W62-W57 W61-W56
6	W34-W29	W43-W39	W52-W47	W62-W57
7	W33-W28	W42-W38	W51-W46	W61-W56
8	(out)	(out)	(out)	(out)
parity:				
yes	W36-W31	W44-W40	W54-W49	W64-W59
no	(out)	(out)	(out)	(out)
odd	W32-W27	W41-W37	W50-W45	W60-W55
even	(out)	(out)	(out)	(out)

*The number of stop bits for Port 2 is controlled by internal logic:
110 Baud = 2 stop bits
All other baud rates are set for one stop bit.

2.4 BAUD RATE SELECTION

Baud rate settings for the four ports are implemented as follows:

Switch	Port	
SW2	Port 2	
SW4	Port 1	(receiver and transmitter NOT independent)
SW5	Port 3	
SW6	Port 4	

2.5 DATA WORD CHARACTERISTICS

The settings for number of stop bits, data bits, and parity selection for each port are shown in Table 2-6.

2.6 LINE TIME CLOCK (LTC)

The PM-MFV11A contains a clock register at bus address 177546. The clock interrupts the processor, using the BEVENTL line on the LSI bus (vector = 100). The clock may be controlled by it's bus register, the front panel LTC switch, or both. You may select either the external source for the clock (derived from the AC power line) or an internal 60Hz source (derived from a crystal). See Table 2-7 for switch settings.

TABLE 2-7. LINE TIME CLOCK

Function	S1-4	S1-5	S1-7	S1-8	S3-9
EXT/MANUAL (factory setting)	ON	OFF	ON	OFF	ON
EXT/PROG	ON	OFF	OFF	ON	OFF
INT/MANUAL	OFF	ON	ON	OFF	ON
INT/PROG	OFF	ON	OFF	ON	OFF
EXT/PM*	ON	OFF	OFF	ON	ON
INT/PM	OFF	ON	OFF	ON	ON

*PM = Programmable/Manual

2.7 READ ONLY MEMORY (ROM)

The PM-MFV11A contains 1024 words of ROM in four pages of 256 words, each residing at bus address 173000-173776. The ROM contains both the basic system diagnostics and the bootstrap routine.

2.7.1 DIAGNOSTICS

The PM-MFV11A contains a set of 12 diagnostic light-emitting diodes (LEDs) which, in conjunction with the firmware diagnostics, facilitate fault diagnostics to the module level.

Table 2-8 lists the signals and conditions each LED monitors. The LEDs are mounted on the top edge of the board, enabling easy viewing during system operation.

TABLE 2-8. DIAGNOSTICS LEDS

LED	Signal	Condition
CR13	+5VDC	(ON)
12	BDCOK	(ON)
11	BPOK	(ON)
10	+12VDC	(ON)
9	BREF	(OFF)
8	DAI 03	(ON) [self-test indicator]
7	DAI 02	(ON) [self-test indicator]
6	DAI 01	(ON) [self-test indicator]
5	DAI 00	(ON) [self-test indicator]
4	BEVENT	(ON if clock is ON)
3	SERIAL IN	(ON if Port 1 is receiving)
CR 2	SERIAL OUT	(ON if Port 1 is transmitting)

OPERATION:

When the BOOT switch is depressed on the front panel, the ROM program executes test 1-9, then enters the bootstrap monitor.

WARNING

Test 9 requires that the console device have a maintenance bit for a 'wrap' test. The Plessey and DEC DLV11-J and DEC DLV11 do not have this bit so the diagnostic will fail if they are used as the console device. This condition can be remedied by pressing the BREAK key on the console and typing 173766G in response to the console-ODT prompt character. (Use 773766G if you have an LSI-11/23 CPU).

Table 2-9 gives a test listing and description of the diagnostics and their resulting failure pattern displayed in the LEDs.

TABLE 2-9. SELF-TEST DIAGNOSTICS

The self-test diagnostics (enabled by depressing the boot switch) will not print an error message; however, the LEDs (CR5,6,7,8) will display the test number then halt:

CR8	CR7	CR6	CR5	test ID	Test Description
0	0	0	1	test 1	LED and R/W register test
0	0	1	0	test 2	single operand instr test
0	0	1	1	test 3	double operand instr test
0	1	0	0	test 4	jump test with mode 1, 2, & 3
0	1	0	1	test 5	single operand, byte test
0	1	1	0	test 6	dbl oper instr with modes 2 & 4
0	1	1	1	test 7	dbl oper, modes, byte test
1	0	0	0	test 8	JSR instr with modes 1 & 6
1	0	0	1	test 9	port 1 (console) test
1	0	1	0	XMTEST	28K memory test
1	0	1	1	XFTEST	dual density floppy disc test } N/A
1	1	0	0	XRTEST	RK11/RK05 test

Note

The results of XFTEST & XRTEST can be verified by dumping block 0 with the RT-11 program DUMP.
XMTEST results can be verified by using console ODT to examine the registers:

R0 = MEMORY ADDRESS
R1 = BAD DATA
R2 = GOOD DATA
R5 = HIGHEST MEMORY ADDRESS

2.7.2 MONITOR

The PM-MFV11A PROM contains a monitor program which allows the user to run additional tests or bootstrap from a device.

Additional tests:

XM - Memory test writes and verifies a pattern in low 28K of memory
Type: XM [CR] ([CR] denotes carriage return). There should be a CR at the beginning of the test and a line-feed and prompt character at the end of the test with several seconds between.

XF - Dual density floppy disc test (writes and verifies a pattern in block 0)
Type: XF [CR] The following message will be printed:

```
INSTALL SCRATCH, FORMATTED DISC ON DRIVE
ANY EXISTING DATA WILL BE LOST
DOUBLE DENSITY (Y or N) ? =
```

Enter a single character corresponding to the media density (No CR). The diagnostic will write and verify a test pattern in block 0. If the test passes, the only print-out will be the prompt character. If the test fails, the program will halt with the test number displayed in the diagnostic lights (1011).

XR - RK11/RK05 test (writes and verifies a pattern in block 0).
Install a 'scratch, formatted' pack in the RK05.
Type: XR [CR] The following message will be printed:

```
ALL DISC DATA WILL BE LOST
READY?
```

Type: Y (No CR)
The test works the same as the XF test except the failure indication is 1100 in the disagnostic lights.

Note

The results of XFTEST and XRTEST can be verified by dumping block 0 with the RT-11 program DUMP.
XMTEST results can be verified by using console ODT to examine the registers:

R0 = MEMORY ADDRESS
R1 = BAD DATA
R2 = GOOD DATA
R5 = HIGHEST MEMORY ADDRESS

2.7.3 BOOTSTRAP MONITOR

The bootstrap monitor will type a carriage return, line-feed (CRLF), and prompt character (*) on the console teletype (TTY) device (CSR 177560). The monitor then waits for an operator response in the following formats (square brackets indicate optional parameters):

DD[N][:XXXXXX] (CR)

When DD represents the two character test ID or device identifier specified below, N represents the device unit number (if no unit number is specified, 0 is used as a default), and XXXXXX represents the command register address to be used. If none is specified, the defaults below are used.

Table 2-10 lists the devices which the PM-MFV11A is capable of bootstrapping.

TABLE 2-10. PM-MFV11A CAPABILITY OF BOOTSTRAPPING DEVICES

Device	Dev.ID	Default CSR	Description
RK11	DK	177404	2.5/5.0 MB Cartridge Disc
RK06	DM	177440	14 MB Cartridge Disc
RP11	DP	176714	20/40/80 MB Disc-Removable
RL11	DL	174400	Cartridge Disc Top-Loader
RX01	DX	177170	Floppy Disc (RX11)
RX02	DY	177170	Dual Density Floppy Disc (RX211)
TM11	MT	172522	9 Trk 800 BPI Mag Tape
TU58	DD	176500	TU58 DECTAPE-II

2.8 SWITCHES AND JUMPERS

The PM-MFV11A contains 70 switches and 82 wire-wrap posts to allow maximum flexability of configuration.

2.8.1 SWITCHES

The PM-MFV11A has nine switch assemblies (dip-switches) with eight to ten switches on each pack. The switches and their positions are defined as follows:

Note

[MU/X] = Mutually exclusive with switch position X.

SWITCH 1:

pos		
1	(not used)	
2	enable program ctrl of modem (Port 2) RCVR baud rate	
3	(not used)	
4	enable external LTC source	[MU/5]
5	enable internal LTC source	[MU/4]
6	allow to receive DATA-SET-RDY from line printer (Port 3)	
7	manual LTC ctrl	[MU/8]
8	programmable LTC ctrl	[MU/7]

SWITCH 2:

pos	Port #2 (modem)
1-4	RCVR baud rate
5-8	XMTR baud rate

SWITCH 3:

pos		
1	modem XMTR uses RCVR clock	[MU/2]
2	modem XMTR uses own clock	[MU/1]
3	modem XMTR & RCVR use same clock	
4	modem XMTR uses internal clock	
5	modem XMTR clock available to outside world	
6	modem RCVR uses internal clock	
7	program ctrl of DATA-XMIT-RDY	
8	program ctrl of RDY-TO-SEND	
9	manual LTC ctrl	
10	program ctrl of modem port	

SWITCH 4:

pos	Port #1 (console)
1-4	RCVR XMTR baud rate
5	DAO 04
6	DAO 05
7	DAO 06
8	DAO 07

SWITCH 5:

pos	Port #3 (line printer)
1-4	RCVR baud rate
5-8	XMTR baud rate

SWITCH 6:

pos	Port #4 (user)
1-4	RCVR baud rate
5-8	XMTR baud rate

SWITCH 7:

pos	
1	port #4 vector bit 5
2	port #4 vector bit 3
3	port #4 vector bit 4
4	port #4 vector bit 6
5	enable modem RQST-TO-SEND
6	enable modem FORCE-BUSY
7	enable modem (Port 2) interrupt on level 5
8	address selection of page and GP reg (ON--Factory setting)
9	address selection of page and GP reg (OFF--Factory setting)
10	disable LP vector (sets vector of XX4 instead of XX0 - Port 3)

SWITCH 8:

pos	
1	port #2 vector bit 4
2	port #2 vector bit 3
3	port #3 vector bit 8
4	port #3 vector bit 7
5	port #3 vector bit 5
6	port #3 vector bit 3
7	port #3 vector bit 4
8	port #3 vector bit 6
9	port #4 vector bit 8
10	port #4 vector bit 7

SWITCH 9:

pos	
1	port #1 (console) vector bit 8
2	port #1 (console) vector bit 7
3	port #1 (console) vector bit 6
4	port #1 (console) vector bit 5
5	port #1 (console) vector bit 4
6	port #1 (console) vector bit 3
7	port #2 vector bit 8
8	port #2 vector bit 7
9	port #2 vector bit 6
10	port #2 vector bit 5

2.8.2 JUMPERS

The PM-MFV11A has 82 wire-wrap posts arranged in 11 functional groups as shown in Table 2-11.

TABLE 2-11. WIRE-WRAP POSTS IN FUNCTIONAL GROUPS

Wire-Wrap Posts	Functional Groups
W1-W7	port #1 cable driver
W8-W21	port #3 & #4 cable drivers
W22-W23	control panel HALT
W24-W26	port #1 framing error
W27-W36	port #1 UART characteristics
W37-W44	port #2 UART characteristics
W45-W54	port #3 UART characteristics
W55-W64	port #4 UART characteristics
W65,W67,W82	ROM address
W68-W78	port mapping
W79-W81	UART reset

Note

The factory setting for these jumpers are given in Section 2.2.

2.9 CONNECTOR SIGNAL DESIGNATIONS

2.9.1 LSI-11 BUS PIN ASSIGNMENTS

The PM-MFV11A operates on the LSI-11 bus. Bussed signals and their pin assignments are shown in Table 2-12.

2.9.2 FRONT PANEL CONNECTOR PIN ASSIGNMENTS

Connector J5 provides control signals to the front panel. The available signals and their pin assignments are shown in Table 2-13. Connector pin number assignments are shown in Figure 2-2.

TABLE 2-12. PM-MFV11A LSI-11 BUS CONNECTIONS

Side 2		Side 1
Connector A		
+5V	A	BIRQ5L
	B	BIRQ6L
GND	C	BAD16
+12V	D	BAD17
BDOUTL	E	
BRPLYL	F	LTC
BDINL	H	SRUNL
BSYNCL	J	GND
BNTBTL	K	
B1RQ4L	L	
B1NACKL	M	GND
BILKOUTL	N	BDMRL
BBS7L	P	BHALTL
BDMGIL	R	BREFL
BDMGOL	S	
B1NI1L	T	GND
BDALDDL	U	
BDAL01L	V	

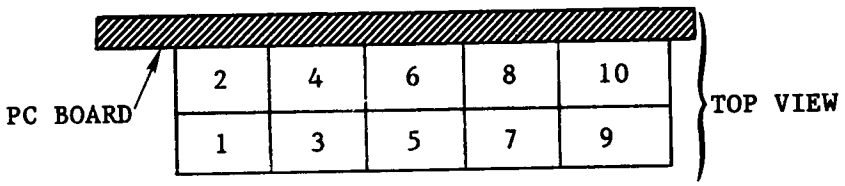
Side 2		Side 1
Connector C		
+5V	A	
	B	
GND	C	
+12V	D	
	E	
	F	LTC
	H	SRUNL
	J	GND
	K	
	L	
BINACKL	M	GND
BINACKOUTL	N	
	P	
BDMG1L	R	
BDMGOL	S	
	T	GND
	U	
	V	

Connector B		
+5V	A	BDCOKH
	B	BPOKL
GND	C	
	D	
BDAL02L	E	
BDAL03L	F	
BDALQ4L	H	EX TCLK
BDAL05L	J	GND
BDAL06L	K	EX RCLK
BDAL07L	L	EX RCLK
BDAL08L	M	GNDD
BDAL09L	N	BSACKL
BDAL10L	P	BIRQ7L
BDAL11L	R	BEVENTL
BDAL12L	S	
BDAL13L	T	GND
BDAL14L	U	
BDAL15L	V	+5V

Connector D		
+5V	A	
	B	
GND	C	
	D	
	E	
	F	
	H	
	J	GND
	K	
	L	
	M	GND
	N	
	P	
	R	
	S	
	T	GND
	U	
	V	+5V

TABLE 2-13. FRONT PANEL CONNECTIONS

Pin	Signal
J5-1	HALT
-2	ENABLE
-3	UNUSED
-4	BOOT
-5	UNUSED
-6	RUN LIGHT
-7	GND
-8	DC ON
-9	LTC OFF
J5-10	LTC ON



Note

The 10-pin connectors are assigned as follows:

J2 - Port #1
J3 - Port #3
J4 - Port #4
J5 - Front panel

Figure 2-2. 10-Pin Connector

2.9.3 PORT #2 INTERFACE CONNECTIONS

Connector J1 provides EIA - RS232C serial interface signals to an external device. Available signals and their pin assignments are shown in Table 2-14. The connector pin number arrangement is shown in Figure 2-3.

TABLE 2-14. SERIAL INTERFACE CONNECTIONS

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A	GND	M	RDATA	Y		KK	
B	GND	N		Z		LL	
C	FORCE BUSY	P		AA		MM	
D		R		BB	CARRIER	NN	
E	TTLSI2	S		CC	REC CLK	PP	
F	XMT DATA 2+	T	CLEAR TO SEND	DD	DATA TERM RDY	RR	
H		U	CLK OUT	EE	RDR EN 2	SS	TTL SO2
J	RCVD DATA	V	REQ TO SEND	FF	SEC XDATA	TT	
K		W		HH	CLK ENL	UU	GND
L		X	RING INDICATOR	JJ	SEC RCVD DATA	VV	GND

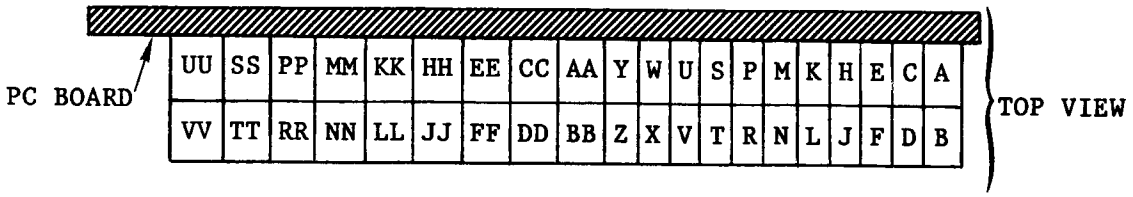


Figure 2-3. Port #2 Interface Connector

2.9.4 PORT #1 INTERFACE CONNECTIONS

Connector J2 provides serial interface signals for Port #1. Available signals and their pin assignments are shown in Table 2-15. The connector pin number arrangement is shown in Figure 2-4.

TABLE 2-15. PORT #1 INTERFACE CONNECTIONS

Pin	Signal
J2-1	T/R CLK
-2	GND
-3	XMT DATA 1+
-4	XMT DATA 1-
-5	
-6	
-7	RCV DATA 1-
-8	RCV DATA 1+
-9	GND
J2-10	+12F

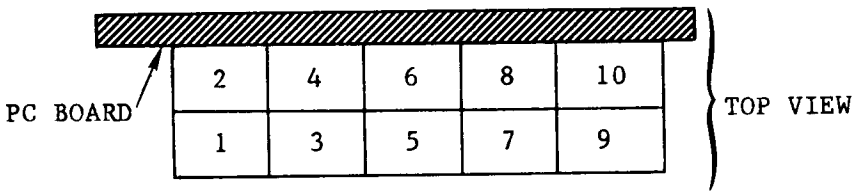


Figure 2-4. Port #1, #3, #4 Interface Connections

2.9.5 PORT #3 INTERFACE CONNECTIONS

Connector J3 provides serial interface signals for Port #3. Included is a hand-shaking signal for a serial printer (DATA SET READY). Available signals and their pin assignments are shown in Table 2-16. The connector pin number arrangement is shown in Figure 2-4.

TABLE 2-16. PORT #3 INTERFACE CONNECTIONS

Pin	Signal
J3-1	TCLK 3
-2	GND
-3	XMT DATA 3+
-4	XMT DATA 3-
-5	DATA SET RDY
-6	
-7	RCVD DATA 3-
-8	RCVD DATA 3+
-9	GND
J3-10	+12F

2.9.6 PORT #4 INTERFACE CONNECTIONS

Connector J4 provides serial interface signals for port #4. Available signals and their pin assignments are shown in Table 2-17. The connector pin number arrangement is shown in Figure 2-4.

TABLE 2-17. PORT #4 INTERFACE CONNECTIONS

Pin	Signal
J4-1	TCLK 4
-2	GND
-3	XMT DATA 4+
-4	XMT DATA 4-
-5	
-6	
-7	RCVD DATA 4-
-8	RCVD DATA 4+
-9	GND
J4-10	+12F

TABLE 3-2. PROM STORAGE ARRANGED IN TWO OPTIONS

Option 1

Bit 8		
	Page 2 256 Words	page 3 256 Words
	Page 0 256 Words	Page 1 256 Words
Addr	173000	Addr 165000

Option 2

Page 3 256 Words	Page	Bits 8	Bits 9
Page 2 256 Words	0	0	0
Page 1 256 Words	1	1	0
	2	0	1
Page 0 256 Words	3	1	1
Addr 173000	Addr 177520		

3.2 PAGE SELECT AND GENERAL PURPOSE REGISTERS

The PM-MFV11A also has two registers to facilitate self-test diagnostics. The first of these registers is located at address 177520 and is called the Display and Page Selection register as shown in Table 3-3. The purpose of this register is to control a set of four LEDs to be used for fault diagnosis, to provide configuration information to the processor via four switches on board the MFV11A, and to select the banks of PROM used to store bootstrap and self-test programs.

The second register located at 177522 (optional address available but not specified) is a 16-bit Read/Write register which can be used as a general purpose register, but it is specifically used for diagnostic tests before memory is known to be good.

TABLE 3-3. DISPLAY AND PAGE SELECTION REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	ø
NOT USED						PAGE SEL	PAGE SEL	SW 3	SW 2	SW 1	SW 0	CR8 DISPL	CR7 DISPL	CR6 DISPL	CR5 DISPL

BIT	CODE	DESCRIPTION
8-9	PAGE SEL	Page Select Bits: When set, transfers appropriate ROM page (256 Words) to starting address 173000 or 165000 depending upon configuration. Bits are Read/Write and accessible by Write byte to high byte only. Cleared By INIT.
4-7	0,1,2,3	Configuration Bits: Connect directly to switches on the MFV11A. Intended to be used to define configuration for diagnostic purposes. Read only cannot be cleared.
0-3	CR 5,6,7,8	Display Bits: Connect directly to LED's on MFV11A. LED's are lit when bits are cleared and extinguished when bits are asserted. Read/Write cleared by INIT.

3.3 LINE TIME CLOCK (LTC) REGISTER

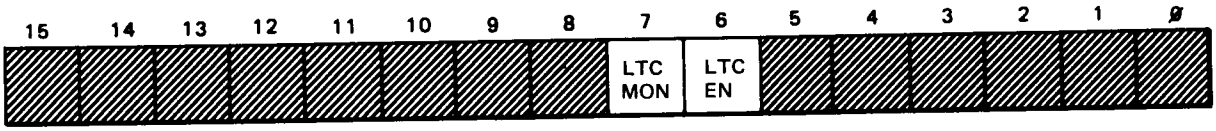
The MFV11A has a LTC control register. The LTC can be driven from the LTC signal emanating from the power supply or optionally via a 60Hz signal generated on the MFV11A itself.

The LTC function can be controlled in three ways:

- Manually via the LTC switch on the front panel
- By program control, ignoring the front panel switch
- By the AND of the switch and the programmable register

The control register for the LTC function is located at address 177546. Its format is in Table 3-4.

TABLE 3-4. LTC CONTROL STATUS REGISTER



BIT	CODE	DESCRIPTION
15-8		Unused.
7	LTC MON	LTC Monitor: Read only. Set by the positive going edge of the LTC input from the bus. This bit can be cleared from software but not set.
6	LTC EN	LTC Enable: Read/Write. When set, enables LTC interrupts to occur on the BEVNT L line. Cleared by INIT.
5-0		Unused.

3.4 PORT REGISTERS

The MFV11A has four ports; each port has a set of four registers. There are seven possible address sets available through switch settings, and the four ports can be mapped in to the set of seven in any way. The standard address configuration is presented in Table 3-5.

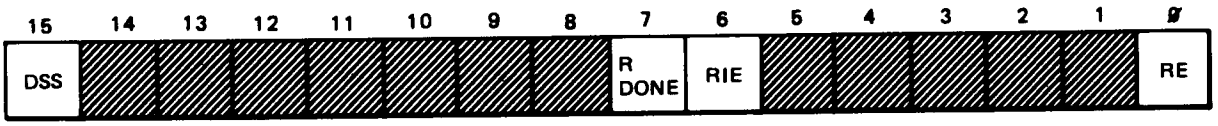
Each of the ports has an individually settable vector. All channels have a fixed bus priority of four except port 2 (DLV11-E) which can be set by switches to five. Channels 1, 3, 4 use a 10-pin connector whose pinout is the same as found on the PM-DLV11J.

All ports have the same register configuration as port 1 (unless port 2 is configured as a DLV11-E). A description of the registers for port #1 are presented in Tables 3-6, 3-7, 3-8, and 3-9.

TABLE 3-5. STANDARD ADDRESS CONFIGURATION

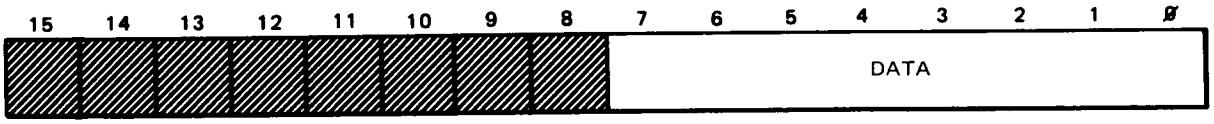
Port	Function	Address	Assignment
1	Receiver CSR	177560	Console
1	Receiver Buffer	177562	Console
1	Transmitter CSR	177564	Console
1	Transmitter Buffer	177566	Console
2	Receiver CSR	176500	
2	Receiver Buffer	176502	DLV11 #1
2	Transmitter CSR	176504	
2	Transmitter Buffer	176506	
3	Receiver CSR	176510	
3	Receiver Buffer	176512	DLV11 #2
3	Transmitter CSR	176514	
3	Transmitter Buffer	176516	
4	Receiver CSR	176520	
4	Receiver Buffer	176522	DLV11 #3
4	Transmitter CSR	176524	
4	Transmitter Buffer	176526	

TABLE 3-6. RECEIVER CONTROL STATUS REGISTER (RCSR)



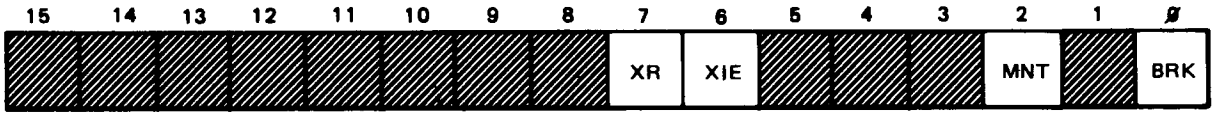
BIT	CODE	DESCRIPTION
15-8		Unused.
7	R DONE	Receiver Done: Read only. Set when the UART has received a character from the external device and is ready to send it to the processor.
6	RIE	Receiver Interrupt Enable: Read/Write. When set, allows R DONE to initiate an interrupt sequence. Cleared by INIT.
5-1		Unused.
0	RE	Reader Enable: Write only. Used with current loop option only. When set, advances paper tape to starting position. Cleared automatically in the middle of the first START bit received.

TABLE 3-7. RECEIVER BUFFER REGISTER (RBUF)



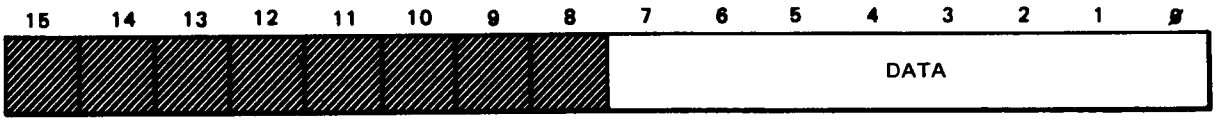
BIT	CODE	DESCRIPTION
15-8		Unused.
7-0	DATA	Received Data: Read only. Bits 0-7 contain the eight bit data word received from the external device for transmission to the processor.

TABLE 3-8. TRANSMITTER CONTROL STATUS REGISTER (XCSR)



BIT	CODE	DESCRIPTION
15-8		Unused.
7	XR	Transmitter Ready: Read only. Set when transmitter has completed the transfer of a character and is ready to accept another.
6	XIE	Transmitter Interrupt Enable: Read/Write. When set, allows Transmitter Ready to initiate an interrupt sequence.
5-3		Unused.
2	MNT	Maintenance: Read/Write. For diagnostic purposes only. When set, SERIAL OUT and SERIAL IN transfers to the external device are inhibited. The serial data output is routed to the serial data input. Cleared by INIT.
1		Unused.
0	BRK	Break: Read/Write. When set, a continuous space level is transmitted. Transmitter Ready (bit 7) and Transmitter Interrupt Enable (bit 6) are still operable, allowing software timing of Break. Cleared by INIT.

TABLE 3-9. TRANSMITTER BUFFFER REGISTER (XBUF)



BIT	CODE	DESCRIPTION
15-8		Unused.
7-0	DATA	Transmitter Data: Write only. Bits 0-7 contain 5 to 8 bits of right-justified data. Loaded under program control for serial transmission.

3.5 ASYNCHRONOUS TRANSMISSION FORMAT

In asynchronous transmission, for proper data recovery by the receiver, stop, start, and parity bits are added to the data in the format shown in Figure 3-1.



Figure 3-1. Asynchronous Data Format

The START bit is detected by the UART as a mark-to-space transition, causing it to begin loading the character into its storage register.

The DATA can be five to eight characters long. It is shifted by the UART so the least significant bit is in the lowest bit position in the register (right-justified).

The PARITY can be configured for odd, even, or no parity. If the device is configured for no parity, the stop bits follow immediately after the DATA bits.

The STOP bits can be configured for either one or two bits. When the first STOP bit is received, the UART shifts the data (in parallel) to a parallel holding register. All START, STOP, and PARITY bits are removed from the data. The receiver asserts Receiver Done (RCSR bit 7), and the data bits become valid.

3.6 PORT #2 AS DLV11-E

When port #2 is configured as a DLV11-E, the additional bits are valid as shown in Tables 3-10 and 3-11.

TABLE 3-10. DLV11-E RECEIVER CONTROL STATUS REGISTER (RCSR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA SET INT	RING	CLR TO SEND	CAR DET	RCVR ACT	SEC REC	NOT USED	NOT USED	RCVR INT	RCVR INT ENB	DSRT INT ENB	NOT USED	SEC XMIT	REQ TO SEND	DTR	READ-ER EN-ABLE

Note

Bits 0, 6, 7 are the same as port 1 RCVR CSR.

BIT	CODE	DESCRIPTION
15	DATA SET INT	Data Set Interrupt: This bit inititates an Interrupt sequence provided the DSET INT ENB (bit 5) is also set. This bit is set whenever CAR-DET (bit 12) CLR-TO-SEND (bit 13) or SEC-REC (bit 10) changes state. It is also set when RING changes from 0 to 1. Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is a Read once bit.
14	RING	Ring: When set, indicates that a ringing signal is being received from the data set. Note that the ringing signal is not a level but an EIA control with duty cycle of three seconds OFF. Read only.
13	CLR TO SEND	Clear to Send: State of this bit is dependant on the state of the clear-to-send signal from the data set. When set, this bit indicates an ON condition; when cleared indicates an OFF condition. Read only.

BIT	CODE	DESCRIPTION
12	CAR DET	Carrier Detect: This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition. Read only.
11	RCVR ACT	Receive Active: This bit, when set, indicates that the DLV11-E receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and is cleared by the leading edge of R DONE H (bit 7). Read only cleared by INIT or DONE H.
10	SEC REC	Secondary or Supervisory Received Data: This bit provides a receive capability for the reverse channel of a remote station. A space (+6V) is read as a 1. The transmit capability is provided via bit 3.
8-9		Not Used.
7	RCVR DONE	Receiver Done: This bit is set when an entire character has been received and is ready for transfer to the processor. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set.
6	RCVR INT ENB	Receiver Interrupt Enable: When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets.
5	DSRT INT ENB	Data Set Interrupt Enable: When set, allows on interrupt sequence to start when DATA SET INT (bit 15) sets. Read/Write cleared by INIT.

Note

When clearing an interrupt enable bit, first set the appropriate processor status bit. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.

BIT	CODE	DESCRIPTION
4		Not Used.
3	SEC XMIT	Secondary or Supervisory Transmitted Data: Provides transmit capability to reverse channel of a remote station. When set, transmits a space (+11.5V). Read/Write cleared by INIT.
2	REQ TO SEND	Request To Send: A control lead to the data set which is required for transmission. A switch ties Request-to-Send to Force Busy in the data set. Read/Write, cleared by INIT.
1	DTR	Data Terminal Ready: A control lead for the data set communication channel. When set, permits connection to the channel. When clear, disconnects the interface from the channel. Read/Write must be cleared by program control. Not cleared by INIT.

TABLE 3-11. DLV11-E TRANSMITTER CONTROL STATUS REGISTER (XCSR)

15	14	13	12	11	10 9 8 7 6 5 4 3 2 1 Ø
PBR SEL 3	PBR SEL 2	PBR SEL 1	PBR SEL 0	PBR SEL END	SEE NOTE

Note

Bits 10 thru 0 are the same as for port 1

BIT	CODE	DESCRIPTION
15-12	PBR SEL	Programmable Baud Rate Select. When set, these bits choose a baud rate from 50 - 19.2K baud. Write only.
11	PBR ENB	Programmable Buad Rate Enable. This bit must be set in order to select a new baud rate as indicated in setting bits 12-15. Write only.

When Port 2 is configured as a DLV11-E, the transmitter and receiver data buffers remain the same as Port 1.

3.7 BUS TERMINATION

The PM-MFV11 supplies 120 ohm bus termination for the LSI-11 bus. Provision has been made for future expansion by including termination for BIRQ5, BIRQ6, BAD 16, and BAD 17.

theory of operation 4

4.1 INTRODUCTION

Figure 4-1 shows a simplified block diagram of the PM-MFV11A.

4.2 ADDRESS SELECTION LOGIC

Address information from the LSI-11 bus is decoded by the two Programmable Read-Only Memories (PROMs), hardwired logic, and a switch. If the correct address from ROM, line-time clock (LTC), general purpose (G/P) register, page/display register, or properly implemented port is present, the appropriate select (SEL) line is driven, and Bus Reply (BRPLY) is asserted to the bus.

The bus data/address lines BDAL00-BDAL15 are buffered and inverted by bus transceivers U112-U115. Bus control lines are buffered and inverted by bus receivers U116-U118.

Address lines DAI00-DAI12 and BBS7 are latched into U63 and U64 at the leading edge of SYNC. The latched address lines LA00-LA12 and BS7 are available for decoding elsewhere on the board as shown in Figure 4-2.

4.2.1 ROM, PAGE, and G/P REGISTER SELECTION

Latched address lines LA01-LA12 and BS7 are decoded by ROM (U79), SW7-8, wire-wrap posts W65, W67, W82, gates U74 and U108 to select the Bootstrap ROM, Page/Display, and G/P registers.

The Bootstrap ROM has 1024 words broken into four 256 word "pages". Only one page is resident at a time and responds to addresses 173000-173776. Page selection is accomplished by writing only to the high byte of the Page/Display register (177520). Bits 8 and 9 of the Page register are loaded into latch U110 and select the upper or lower half of the four ROMs (U93-U96) and the first (U93, U95) or second (U94, U96) group in conjunction with the ROM enable signal from U79. Refer to subsection 3.1.2, Option 2 for page selection. When power is first applied to the system (or the front panel BOOT switch is depressed), the page register (U110) is cleared to ensure that page 0 of the ROM is enabled. Thereafter, the Bootstrap program takes care of selecting the necessary page for proper program operation. The block diagram for ROM and Page register selection is shown in Figure 4-3.

The display section of the Page/Display register is the four least significant bits of the low byte. Latch U81 holds DAI00-DAI03. The outputs are used to drive LEDs CR5-CR8. A "0" bit turns the LEDs ON. A "1" bit turns the respective LED OFF. Refer to subsection 3.2 for bit assignments. The output from U81 is passed on to U99 to enable these bits to be read by the software.

The G/P register consists of U97 and U92, It is a 16-bit Read/Write (R/W) register which appears to the software as a memory location on the bus. It is used by the internal diagnostic until the processor general registers are known to be good.

4.2.2 DEVICE REGISTER SELECTION

Device register addresses are decoded by ROM U90. The ROM is capable of responding to eight addresses:

Address	Device	Group
177546	Clock	Fixed
177560	Console	Selectable
175610	Modem	Selectable
176500	DLV11	Selectable
176510	DLV11	Selectable
176520	DLV11	Selectable
176530	DLV11	Selectable
177514	LP	Selectable

Seven of the eight addresses are selectable for the four ports by wire-wrap posts. The individual buffer and control/status register addresses are further decoded by U50. LA02-LA12 and BS7 are decoded. If one of the eight address groups is present, the appropriate output line from U90 is driven. If the Clock is selected, the signal is passed on to the reply logic, and the Clock register (U39 and U75) is enabled for a read or write operation. If any of the other devices is selected, the signal is passed on to U109 via wire-wrap posts. If no jumper is installed, there will not be a reply from the PM-MFV11A. For jumpers that are installed, U109 passes the signal on to the reply logic and encodes the port select signals (SEL 0 and SEL 1). The block diagram for the device register address is shown in Figure 4-4.

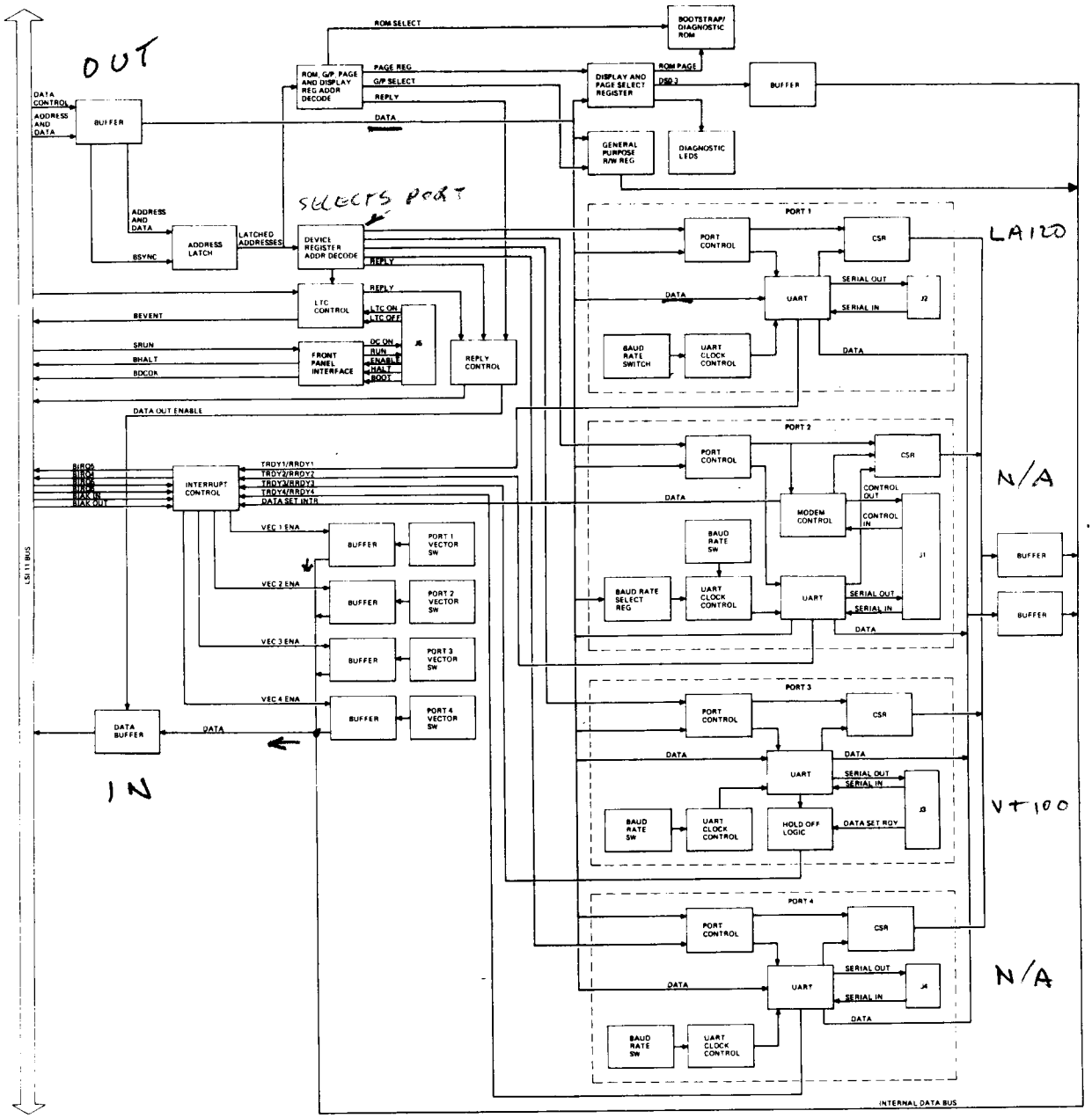


Figure 4-1. Simplified PM-MFV11A Block Diagram

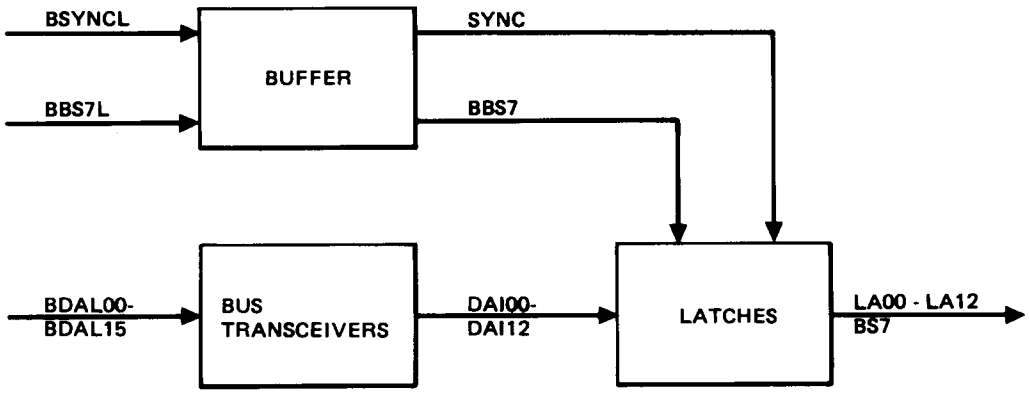


Figure 4-2. Available Latched Address Lines

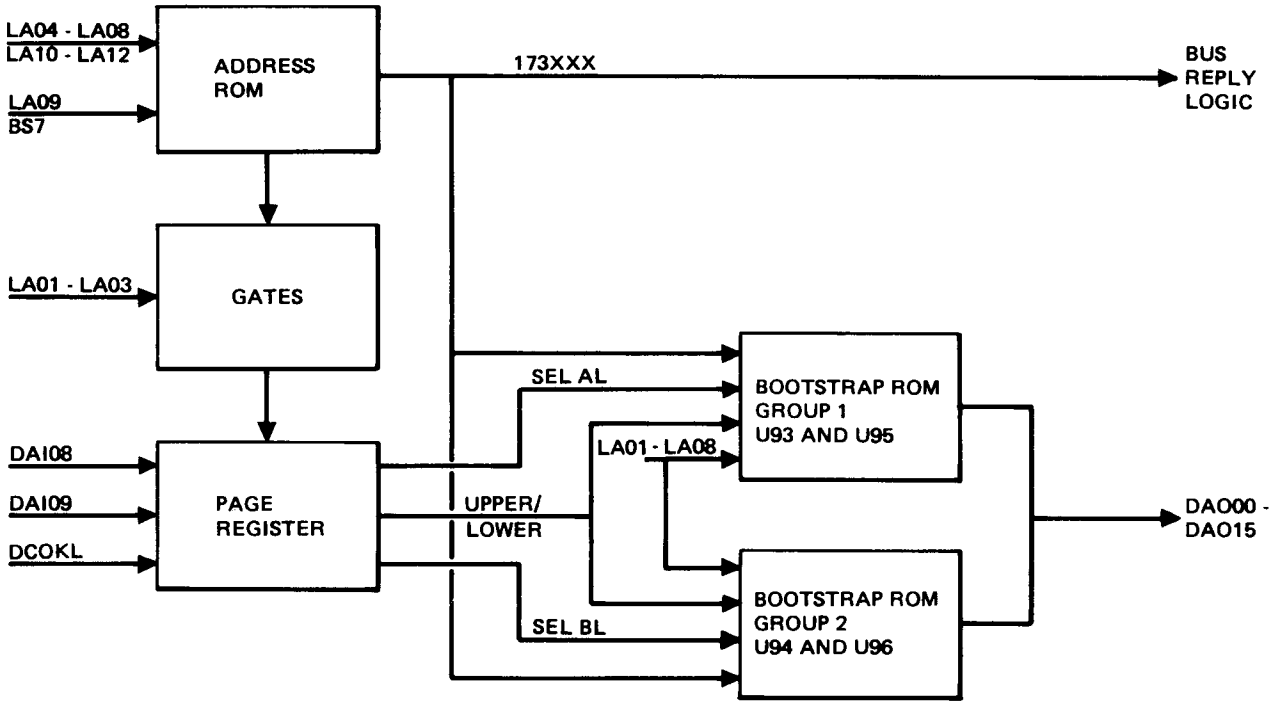


Figure 4-3. ROM, Page Register Selection Block Diagram

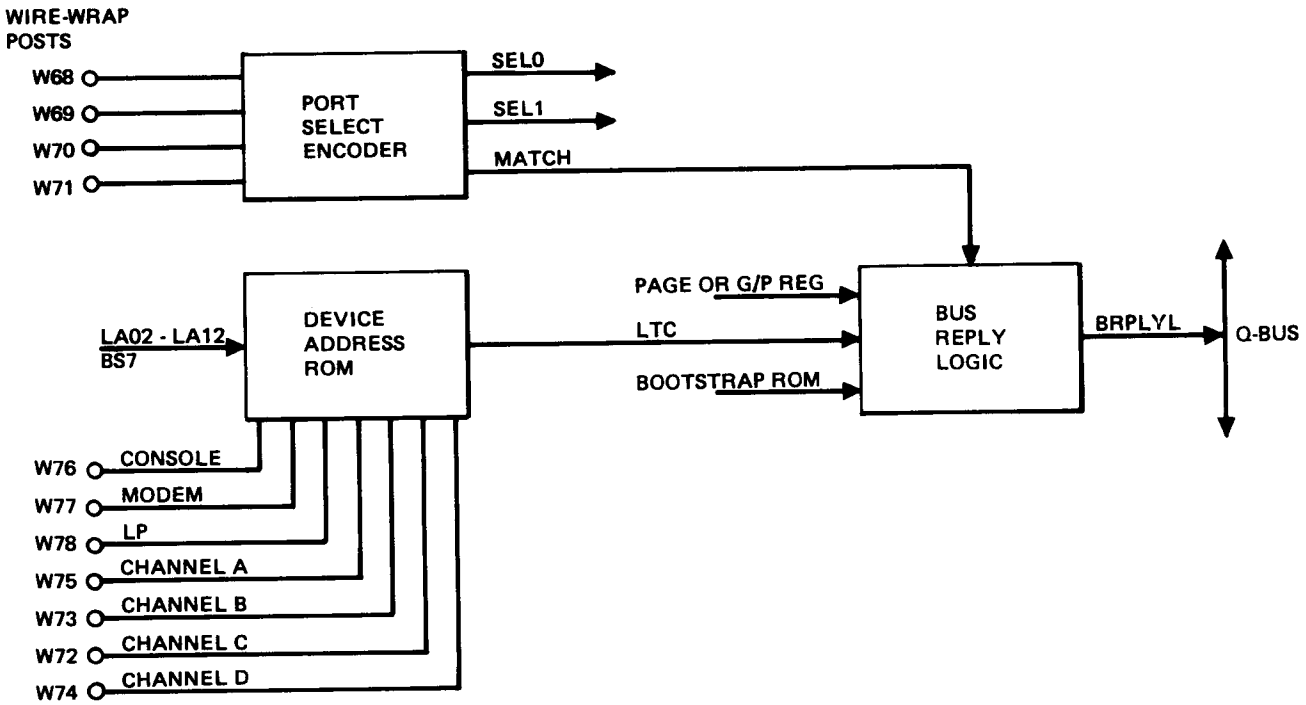


Figure 4-4. Device Register, Address Block Diagram

4.2.3 BUS REPLY LOGIC

Whenever a bus device responds to an address sequence, the CPU SYNC signal is acknowledged by BRPLYL from the addressed device. This function is performed on the PM-MFV11A by gates U74, U102, and U107. A small delay is provided by U109 before the reply latch, U106, is set. The reply latch is cleared at the end of the sequence by the negation of one of the data transfer signals, DIN or DOUT.

4.3 LINE TIME CLOCK (LTC) INTERFACE

The LTC logic uses either the LTC signal from the power supply or an internal crystal-controlled 60Hz clock. The selection of the clock source is done by SW1-4 and SW1-5. The power supply clock, LTC is picked up from the bus on pin CF1 and filtered by R11 and C2 before being passed to SW1-4. The internal clock (60Hz) is received from U21 and applied to SW1-5. The selected clock, LTC OUT, is passed to bus-buffer U101 and flip-flop U73. The LTC Control and Status Register (CSR) functions are provided by U73 and U39. Bit 7 of the CSR is the clock monitor bit. Bit 7 is read-only and is set by LTC OUT or INITL. The output of U73 is gated by U19. When a read operation is performed, bit 6 and bit 7 are gated onto the internal data bus as DA006 and DA007. Bit 6 of the CSR is the interrupt enable bit. Bit 6 is a read/write bit stored in U39. The output of U39 is gated to the internal data bus by U13. The output is also passed to SW1-8 for selection as a clock control signal when programmable clock control is desired.

Selection of clock control is handled by SW1-7, SW1-8, and SW3-9. U100 buffers the control signals and applies them to U101 as an enable. One section of U101 drives LED CR4 to indicate that the clock is interrupting the CPU. Another section of U101 gates the clock signal to the BEVENTL line to interrupt the CPU. A block diagram for the LTC interface is shown in Figure 4-5.

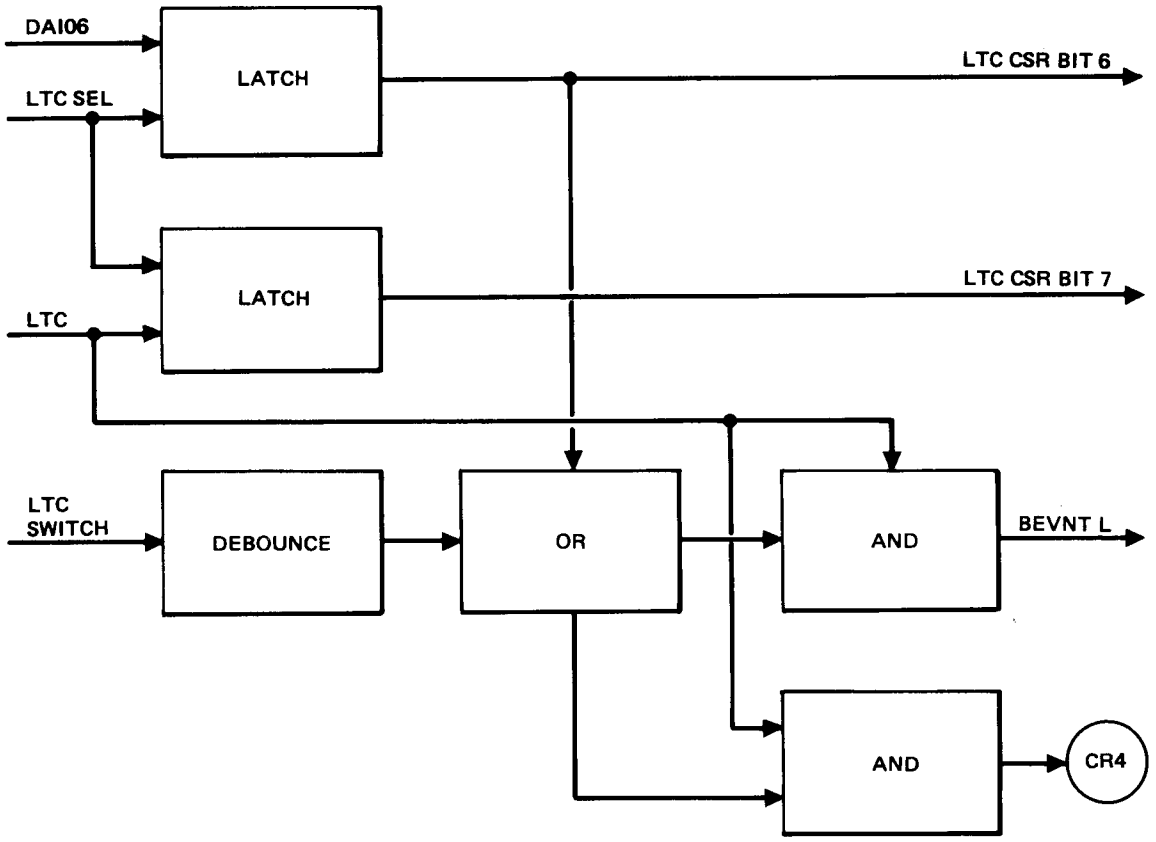


Figure 4-5. LTC Block Diagram

4.4 FRONT PANEL INTERFACE

The PM-MFV11A contains logic to handle the front panel LTC, Boot, Enable/halt switches, and DCON and RUN lights. The LTC switch is debounced by U20 and passed by SW3-9 to U100 for manual control of the Line Time Clock.

The BOOT switch is debounced by U20 and passed to U9 which generates a fixed pulse. The pulse is buffered by U27 and drives the BDCOKH line to simulate a power-fail condition to the CPU. The reaction of the CPU to this signal is dependant on its jumpers and is typically strapped to jump to location 173000 and begin program execution. The PM-MFV11A Bootstrap ROM starts at this location.

The Enable/Halt switch is debounced by another section of U20, buffered by U27, and drives the BHALTL line to the CPU. The SRUNL signal is buffered by U100 and drives retriggerable one-shot U33. When the CPU is executing program code, the output of U33 drives the RUN light on the front panel through U101 to indicate program operation.

The DCON light is driven by +5VDC, current limited by R7, and indicates that DC power is available. The block diagram for the front panel interface is shown in Figure 4-6.

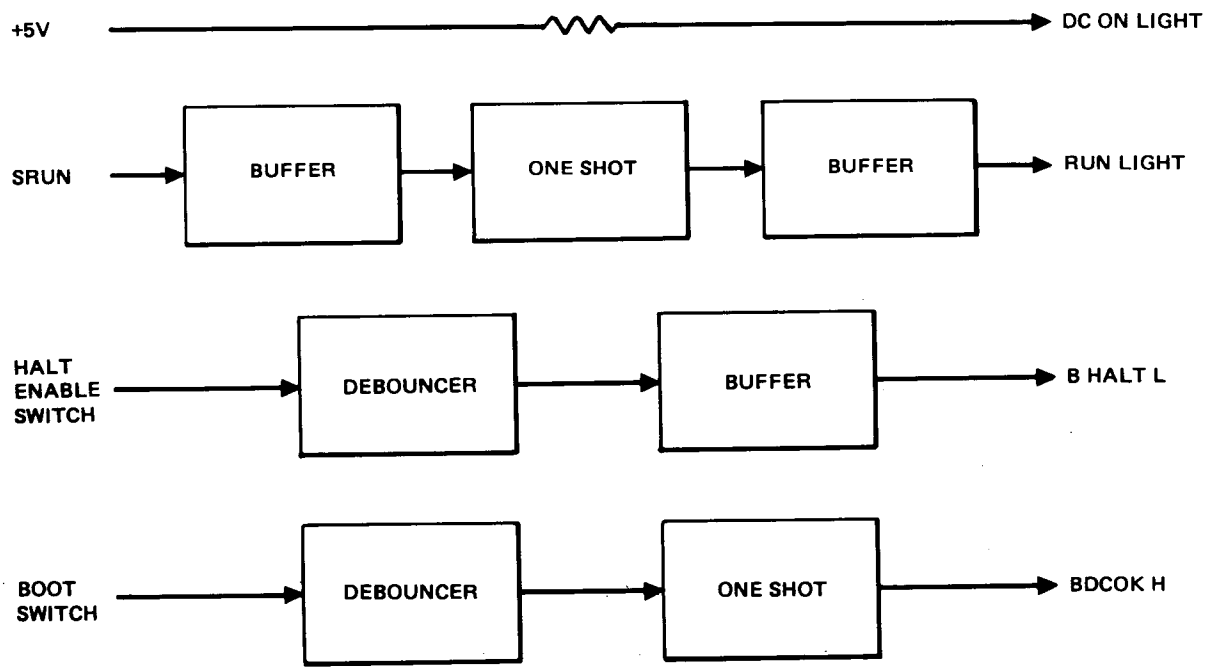


Figure 4-6. Front Panel Interface

4.5 PORT 1, 3, AND 4

Ports 1, 3, and 4 function in a similar manner with the few exceptions noted in subsections 4.5.1 and 4.5.2.

4.5.1 BAUD RATE SELECTION

The PM-MFV11A contains a 5.0688MHz crystal clock. This clock feeds baud rate dividers U33, U69, U70, and U71. The dividers have independent outputs for the receivers and transmitters; however, the clock for the port 1 receiver and transmitter is tied together. The "unused" clock from U69 is further divided by U56 and U21 to generate the 60Hz clock for the LTC circuit. The divide-by-4 clock output of U69 is divided again by U80 to drive the charge pump which creates -12VDC (used by various intergrated circuits).

The baud rate divider is presented in Figure 4-7.

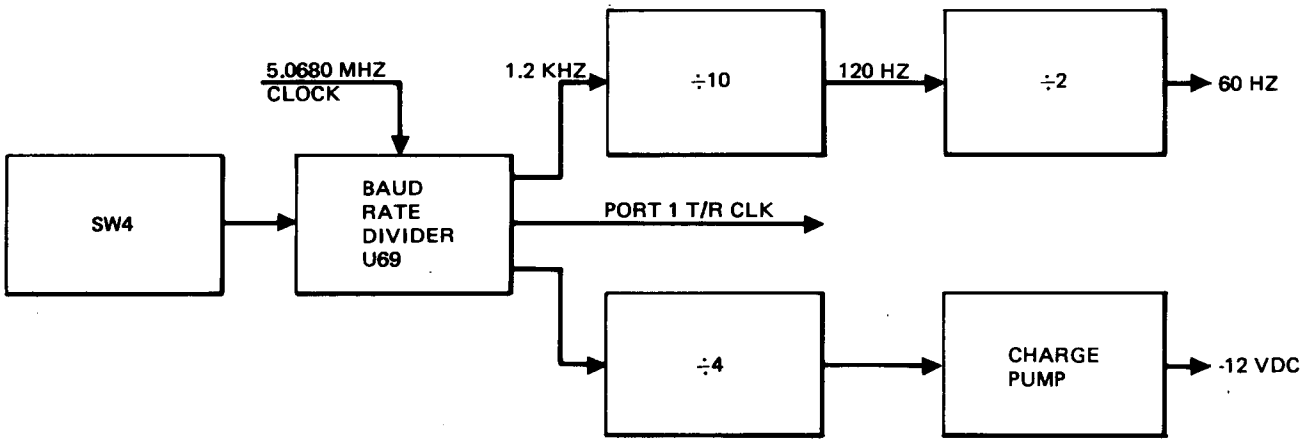


Figure 4-7. Port 1 Baud Rate Divider

Port 3 and 4 have independent switch selection of their baud rates. In each case, the transmitter clock is available at the I/O connector for the port.

Note

Since the baud rate dividers are loaded by DCOKL, the BOOT switch (front panel) must be operated if the baud switches are changed with power applied.

4.5.2 UNIVERSAL ASYNCHRONOUS RECEIVER - TRANSMITTERS

Each port has its own UART with its own configuration jumpers for selection of word length, parity, and stop bits (refer to subsections 2.5 and 3.4).

The UARTs may be jumpered to clear on power-up or on a RESET instruction.

When the Port 1 receiver detects a framing error (i.e., BREAK key), it can be configured to re-boot the system or cause the CPU to halt.

Port 3 has additional logic for use with a serial line printer. The Port 3 I/O connector (J3) passes the DATA SET RDY signal to U14 which buffers it and sends it via SW1-6 to U37 (HOLDL). When HOLDL is low, U39 is inhibited from clocking high, and the transmit-ready signal (TRDY3) is not passed to the Port 3 transmitter CSR. Opening SW1-6 will allow the Port 3 transmitter-ready bit to function normally (i.e., go "ready" when the transmitter has finished sending a character).

4.6 PORT 2

When configured as a spare DLV-11, Port 2 functions similar to the other three ports. However, when Port 2 is configured for remote DLV operation (modem control), many additional bits in the CSRs are enabled.

The normal CSR functions (refer to Section 3) are handled by U34-U36 and U50-U54.

4.6.1 BAUD RATE SELECTION

The baud rate divider for Port 2 is U33. The transmitter baud rate is selected in the same fashion as Ports 1, 3, and 4. The receiver baud rate is selected by multiplexer U32 from either the baud rate switches or from bits 12-15 of the transmitter CSR if SW1-2 is closed. SW3-1, 2, 3, 4, 5, and 6 allow versatile routing of the clocks between receiver, transmitter, bus, and I/O connector. (To enable read/write control of the "entended" CSR bits, S3-10 must be closed).

4.6.2 DATA SET CONTROL

Request-to-Send, Sec XMIT, Data Term RDY, and Data Set Interrupt Enable bits are stored in latches U55 and U21. Leaving SW3-8 open will force Request-to-Send high. Leaving SW3-7 open will force Data-Term-Rdy high. These signals are passed to cable drivers U6 and U7 (except Data Set Interrupt Enable) where they are converted to Electronic Industry Association (EIA) voltage levels before going to the I/O connector J1.

4.6.3 DATA SET STATUS

Ring, Clear-to-Send, Carrier-Detect, and Sec Rcvd Data are converted to TTL logic levels by U4 and U5, then sent to buffer register U62 where they become part of the receiver CSR. They are also used by U103 and U85 to compare their current state with their previous state to cause a Data Set Interrupt if their state has changed.

RCVR ACTIVE is created by the Port 2 RCVR clock and counter U18 when Port 2 is receiving serial data. It is cleared by the Port 2 RCVR-DONE bit.

4.7 INTERRUPT CIRCUIT

The interrupts for all four ports are handled the same way with the exception of Port 2 being able (by closing SW7-7) to interrupt on level 5 as well as level 4.

The interrupt enable bits are stored in U34 and allow U43, 45, 46, or 48 to set when a receiver or transmitter is done or a data-set-change occurs. U76 detects the interrupt request and drives the request line on the bus through buffer U105. U76 also encodes the interrupting circuit according to its internal priority.

When the interrupt acknowledge signal is received from the CPU, U8, 26, 41, and 72 check for a higher priority device interrupting before responding. If a higher priority device is requesting service, U73 steers the acknowledge signal back to the bus through U72 and buffer U105 to the next interface. If no higher priority bus request is being made, U73 channels the acknowledge signal to U41 which enables the vector. U77 is also loaded by the data-input cycle of the bus and freezes the internal interrupt code while U78 clears the latch causing the interrupt, and U84 selects the vector to be placed on the bus. U41 also causes U106 to set, and BRPLYL is driven low on the bus. The interrupt cycle is completed when BDINL and BIAKOL is removed by the CPU.

SW7, SW8, and SW9 are used to set the individual vectors for each port. U86-U89 gate the vectors onto the internal data bus.

The block diagram for the interrupt circuit is shown in Figure 4-8.

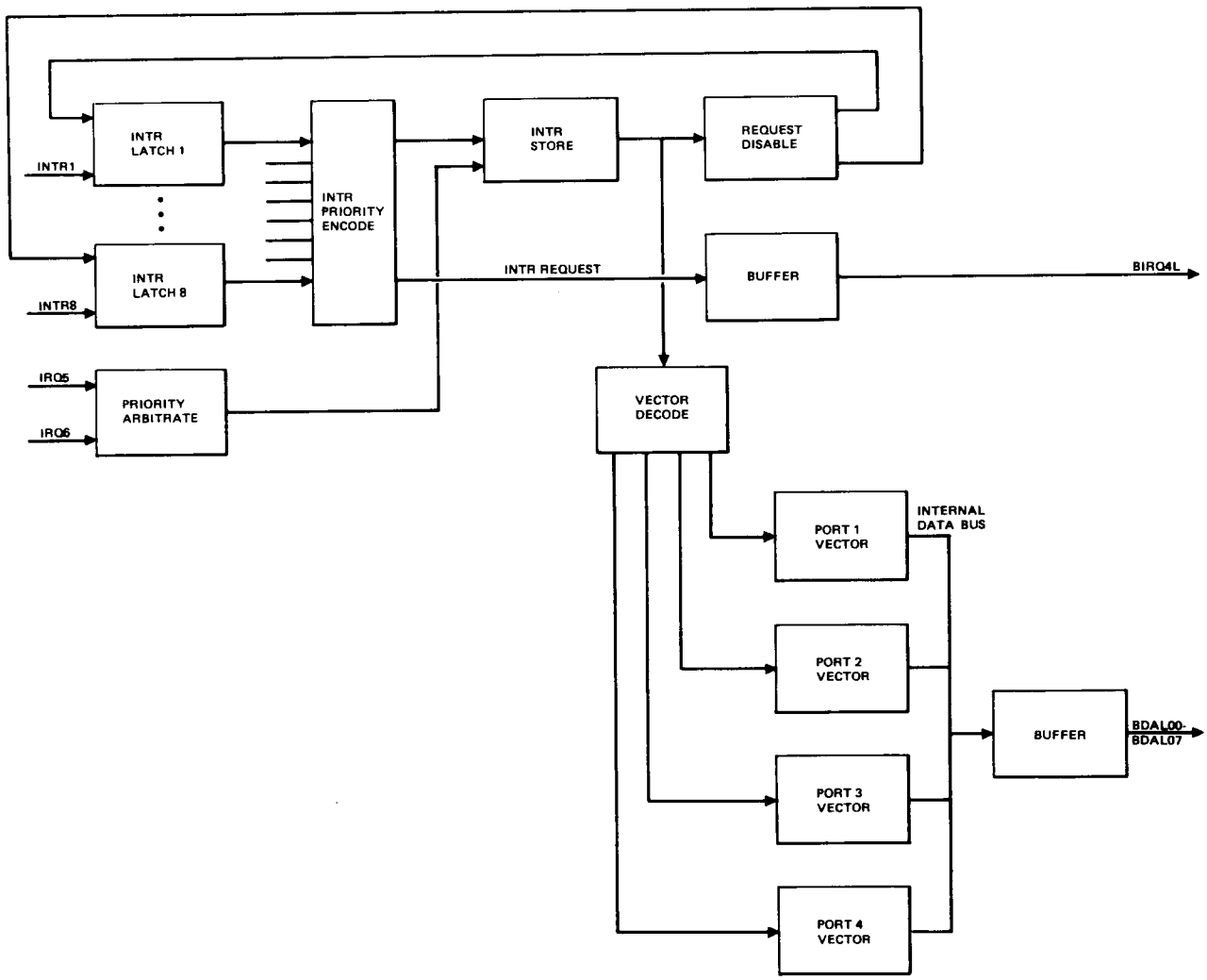


Figure 4-8. Interrupt Logic Block Diagram