Section 4

Theory of Operation

4.1 INTRODUCTION

The PM-TC11A is made up of three boards. The first, Board #1, Format Control Board, has the system clock, the delay counter and main sequencer, and error detection logic on it. Additionally, some PE functions (PE lock, ID burst and postamble detection) are included on this board. They are only utilized on the PM-TC11B version when in PE mode.

Board #2, Unibus Control, has all Unibus interface and bus control logic on it. Also included are all Unibus registers, the data multiplexers, start sequence and tape motion control logic. The tape drive control cable plugs into Board #2, and all control signals are interfaced to the drive by this board.

Board #3, NRZI Control, contains the data and tape format control logic. Error checking is also done on this board. All write and read data interface to the drive via the write data and read data cables plugged into this board.

The PM-TC11B version requires Board #4, PE Control. This board contains the VCO, transition detector, and deskew logic required to read PE data from tape. While Board #4 is necessary to have a dual density controller, all PE logic is not limited to this board. Only read logic is on Board #4. The controller will not function in PE, however, without this board.

Figure 1-1 is a simplified block diagram of the PM-TC11 Magnetic Tape Controller. This shows the basic blocks required to interface to a magnetic tape drive. The following discussion will attempt to define the function of the blocks in this diagram. Reference will also be made to portions of the schematics included in the standard Print Set provided with each controller.

It is assumed the reader is familiar with the DEC PDP-11 computer and Unibus theory of operation. A detailed description can be found in the *"PDP-11 Peripherals Handbook"* by Digital Equipment Corporation, 1975 edition. It is also assumed that the reader understands basic digital logic and is familiar with magnetic tape recording and formats.

4.2 UNIBUS INTERFACE

Schematics SD703290, Sheet 3, shows the logic for Unibus control signals MSYN, SSYN, CØ, and C1. The interface for BBSY and INIT can also be seen there.

The Unibus places a register address on lines AØØ through A17, asserts MSYN, and waits for SSYN. When MSYN is asserted, the controller compares the address lines AØ4 through A17 for a six-word range switched by SW2. When a comparison is found, U95 flip-flop is asserted and generates SSYN to the Unibus. If the Unibus is reading a MT (magnetic tape) register (DATI), both CØ and C1 will be negated. This will generate a selected signal (SELØOUT through SEL5OUT) by decoding ADØ1 through ADØ3 when an address comparison is made of ADØ4 through AD17 and MSYN.

The Unibus writes (DATO or DATOB) to a MT register in much the same way. C1 will be true; CØ will be negated for DATO (true for a DATOB). Address lines are decoded at MSYN time and SSYN is generated. SELØLIN through SEL5LIN and SELØHIN through SEL5HIN are decoded from the output of U108-2, ADØ1 through ADØ3, C1 and ADØØ. A select line is generated for each byte in the register (high byte or low).

Interrupts and DMA Transfers are also controlled by Board #2. DMA Transfers are accomplished under NPR control. Schematic SD703290, Sheet 10, shows the logic used for NPR Transfers. NPR Flip-Flop (U26) generates a request (NPR) when NPRENBL is true or at the end of State One (S1END) during a write operation. The NPR is answered by a grant (NPG) from the Unibus. The Grant Flip-Flop would propagate the NPG to the next device if the tape controller had not issued the NPR. If the NPR was issued by this controller, U38 Grant Flip-Flop will get set by NPG and capture the grant signal. U89 SACK Flip-Flop will get set and issue SACK to the Unibus. The BBSY Flip-Flop waits for the negation of BBSY and SSYN from the Unibus, then gets set when NPG is negated, thus declaring mastership of the bus by generating BBSY. Since NXM and SSYN are both negated at this time, the BBSY Flip-Flop will cause MSYN to be generated through U108 Flip-Flop. MSYNT and the SSYN generated SPLS, then generates XFR to the data control circuitry to read or write a data word on the data lines DØØ through D15.

Interrupt control is shown on Sheet 11 of SD703290. The logic is similar to the NPR logic. BR Flip-Flop U26 generates a request which may be strapped to any single request line BR4 through BR7. A corresponding grant line (BGIN4 through BGIN7) is jumpered through to Grant Flip-Flop U5. The remaining three grant lines are jumpered through to BGT4 through BGT5 to be passed on to the next device. Grant Flip-Flop U5 captures the grant if the request originated from this controller. If the request was not made from this controller, the grant will be

passed on via the corresponding BGT line (BGT4 through BGT7). The grant then generates a SACKI via SACK Flip-Flop U3. BAVAL is the same signal used in DMA to enable the BBSY Flip-Flop there. It is true when SSYN and BBSY are negated. BAVAL then allows BBSY Flip-Flop U3 to be set when the grant goes false. BBSY then negates SACKI, generates INTR, and places the vector on the DØØ through DØ7 lines. Sheet 8 of SD703290 shows how the vector is placed on the data lines. BMSTRI is generated by BBSY Flip-Flop U3. This places the vector configured by SW1 (normal location 224, switches V2, V4, V7 open, all others closed) on DBOØØ through DBOØ7 and eventually on the Unibus data lines.

The Unibus data lines interface is shown on Sheet 4 of SD703290. The top two transceiver IC's (U113 and U126) are enabled by BMSTRI for an interrupt operation to place the vector on the data lines.

DBOØØ through DBO15 are the data MUX output. The data MUX is made up of 12 multiplexer IC's on Sheets 8 and 9 of SD703290. Data for each of the six MT registers is read through the data MUX to the Unibus data bits when a register select output line is true (SELØOUT through SEL5OUT), or the controller is NPR Master during a read. Unibus data lines drive through the receivers at all times and become DBIØØ through DBI15. Unibus address lines interface with the controller through transceivers shown on SD703290, Sheets 2 and 3. Address lines are received as AØØ through A17 and become ADØØ through AD17. Controller address output lines ADOØØ through ADO17 are driven to the Unibus address lines when the controller is NPR Master.

4.3 MAGNETIC TAPE CONTROLLER REGISTERS

MTS, Tape Status register, is an accumulation of status conditions from throughout the controller gated through the data mux by SELØOUT select line. The MTS register is read only and will not respond to select in lines. Bit definitions are explained in Section 4.9 and more generally in Section 3.1.

MTC, Tape Command register, is shown on Sheet 5 of SD703290. Register bits are read through the data mux by SEL1OUT.

The command register is loaded by SEL1LIN and SEL1HIN. U79 is the register for the command and interrupt enable bits. U116 decodes the three command bits to form a function.

U41 is the register for Select, Density and Even Parity bits. Select is decoded at U28.

MTCMA, Current Memory Address register, is on SD703290, Sheets 2 and 3. Counters U85, U86, U97 and U98 make up the register and are loaded by SEL3LIN and SEL3HIN from the data lines

DBIØØ through DBI15. Counter U7 is used for extended address bits AD016 and AD017 and is loaded by SEL1LIN from DBI04 and DBI05. The counters increment from the least significant bit (AØØ) to the most significant bit (AD17) at INCMTCMA time by XCLK2.

MTBRC, Byte or Record Counter, is shown on Sheet 4 of SD703290. Counters U87, U99, U98 and U100 form the 16-bit register and are loaded by SEL2LIN and SEL2HIN from DBIØØ through DBI15. The Byte/Record Counter increments from the least significant bit (BRCØØ) to the most significant bit (BRC15) at INCMTBRC time by XCLK2. When all counters have been incremented to all ones, an overflow occurs into U44 and generates the term LAST BYTE. On the next XCLK term OVERFLOW is set. These two terms are used to signal the sequencing logic that the last operation (byte transfer or record search) has occurred.

MTD, Data Register, is shown on Sheet 6 of SD703290. The four quad type D flip-flops, U58, U59, U71 and U72 are the data registers. They are loaded by STB1 through STB4. During a register read STB1 through STB4 are generated by SEL4HIN and SEL4LIN. During DMA transfers STB1 through STB4 are generated by Format Control Logic. The data loaded into the MTD register comes from the Assemble MUX (also on Sheet 6). The Assemble MUX assembles a word from the FIFO data buffer (and ultimately from tape). The output of the FIFO is only 8 bits so the Assemble MUX places this byte in either the high or low byte of the MTD to assemble a 16-bit word for transfer. When using the seven-track core dump mode, the Assemble MUX also functions to assemble the 16-bit MTD word from four, four-bit tape characters. The Assemble MUX is made up of multiplexers U84, U96, U83 and U109 on Sheet 6 and U122 on Sheet 7 of SD703290. During a READ operation, the FIFO output data (FODØ through FOD7) is presented to the input of the multiplexers. All FIFO output data is presented in parallel to both the high and low byte of the Assemble MUX. STB1 through STB4 are then used to determine where the tape character is loaded in the MTD. The Assemble MUX is loaded at any time other than a READ by DBIØØ through DBI16 from the data line receivers.

MTRD, TU10 register, is not actually a register. When reading the MTRD register, the select line SEL5OUT gates the output of the LRC register and specific status bits on to the data lines through the Data Mux. A write to the MTRD will set flip-flops within the controller for the following functions:

- BTG - SEL5HIN and DBI13 true sets U90 (Sheet 4 of SD703290) to generate a BTE error status.
- EDIT - SEL5HIN and DBIØ9 true will set U67-1 (Sheet 7 of SD703290) to EDIT a tape.

- IBM - $\overline{\text{SEL5HIN}}$ and DBI10 true will set U67-2 to generate tapes in IBM compatible format.

- LCPS - $\overline{\text{SEL5HIN}}$ and DBI14 true will set U67-3 to place the LRC character read from tape in the MTD register at the end of a read operation. If DBI14 is false, the CRC character is stored in the MTD at the end of a read.

- Core Dump - $\overline{\text{SEL5HIN}}$ and DBI11 true will set U67-4 and force the signal PACK true when in seven-track mode. This will cause U122 of the Assemble MUX to align the tape characters in the MTD during a read.

$\overline{\text{SEL5LIN}}$ will have no affect in the controller since the low byte of the MTRD is read only.

4.4 SYSTEM CLOCK

The controller architecture utilizes synchronous logic and requires a system clock. Functions are synchronized to three basic times: X Clock (XCLK), Clock (CLK), and Speed Clock (SPCLK). The basic clock can be seen on Sheet 2 of SD701700. Two solid state oscillators are used to generate the basic frequency. This frequency is then switched to generate two different XCLK periods for defined function of the controller. The basic frequencies are 7.2MHz and 5.0MHz. The 7.2MHz is the basic frequency for most functions. The exception is where 5.0MHz is used during State 6 of any write or State 3, 4 or 5 of a 556 BPI (seven-track) operation. Switching is accomplished at the trailing edge of a clock (7.2MHz or 5.0MHz) by anding the output of selector flip-flops U16 with the desired clock at U15 to generate XCLK. This signal is then inverted and both polarities are distributed throughout the controller. Figure 4-1 shows the timing relationship of the system clocks.

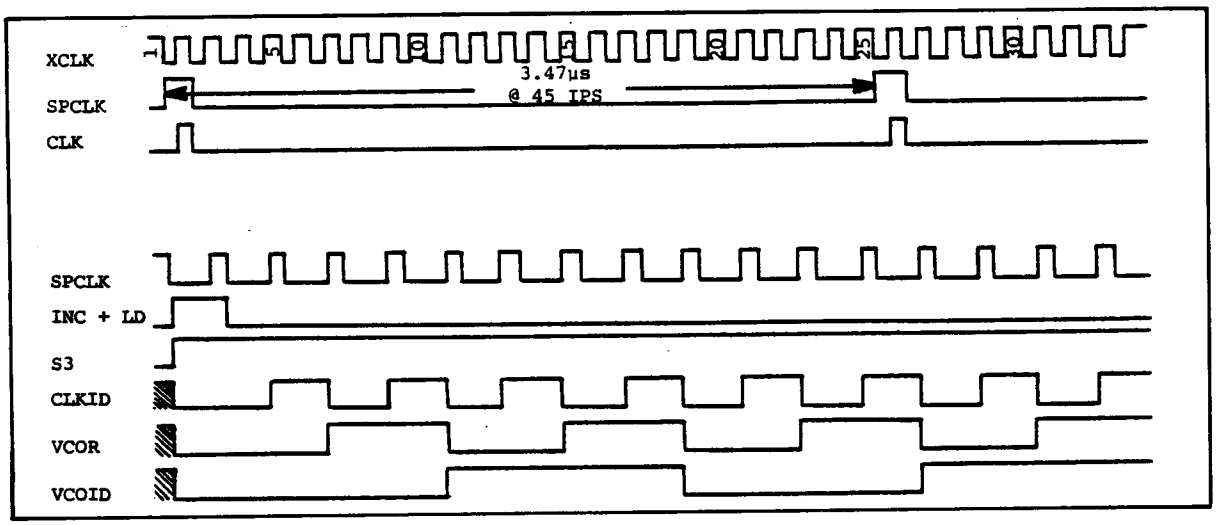


FIGURE 4-1: TIMING DIAGRAM BASIC SYSTEM TIMING @ 45 IPS

Speed clock (SPCLK) is derived from a count of the basic frequency (XCLK) dependent on the speed (ips) of the drive selected. Two speeds (primary and secondary) must be selected by switches SW1 and SW2 (Sheet 3 of SD701700). The term SPDSEL comes from the control adapter on each drive and is switch selectable at the adapter for either primary or secondary drive speed. When a selected drive is on-line, the term SPDSEL will be true for secondary speed or false for primary speed. Switch 1 or 2 are thereby enabled and place a constant on the inputs to counters U5 and U12 that will be loaded when U12 overflows the previous count. The new constant will count XCLK's and generate a SPCLK with each overflow of U12. This overflow loads the constant again and regenerates the count. The term SPCLK is one XCLK wide and goes true on the trailing edge of XCLK. SPCLK is used throughout the controller to generate a drive speed dependent timing signal.

Clock (CLK) is a third system clock which is true only when XCLK is true at SPCLK time. This is accomplished (Sheet 2 of SD701700) by the and function (U45) of XCLK and SPCLK. Clock is also used throughout the controller to synchronize functions.

When CLK and XCLK (or $\overline{\text{CLK}}$ and $\overline{\text{XCLK}}$) are brought to a board and buffered, they receive the board number in the name, i.e., $\overline{\text{XCLK}}$ on Board #2, after buffering, would be $\overline{\text{XCLK2}}$.

4.5 COMMAND DECODE AND START SEQUENCE

Function bits (DBIØ1 through DBIØ3) of the command word are stored in U79 (Sheet 5 of SD703290) and decoded by U116 decoder to create the various signals indicating a particular operation, i.e., read, write end of file (WEOF), etc. The GO Bit (DBIØØ) is also loaded at SEL1LIN time. This starts a chain of events that sequence through U104 and eventually start the main sequencer. The start sequence will issue a forward or reverse (SFC or SRC) command and start tape motion.

Figure 4-2 is a simplified schematic diagram of the Start Sequence Logic. The simplified schematic is necessary to understand the operation since the actual logic is spread out on Boards #1 and #2. The timing diagram of Figure 4-3 will aid in following through the sequence of events starting with DBIØØ setting the GO F/F true. Three $\overline{\text{XCLK}}$ periods later GO DLY will be clocked true. If the selected drive is ready or the requested function was a rewind operation, GO DLY will set GO strobe one (GS1) flip-flop. GS2 resets GO flip-flop and sets DO IT flip-flop on the next $\overline{\text{XCLK}}$.

DO IT waits at the start sequence flip-flop for the next $\overline{\text{CLK}}$ to set STARTSEQ when the Main Sequencer is at State Ø. Tape motion command TAPEMTN is set true the next $\overline{\text{CLK}}$ period time after STARTSEQ comes true.

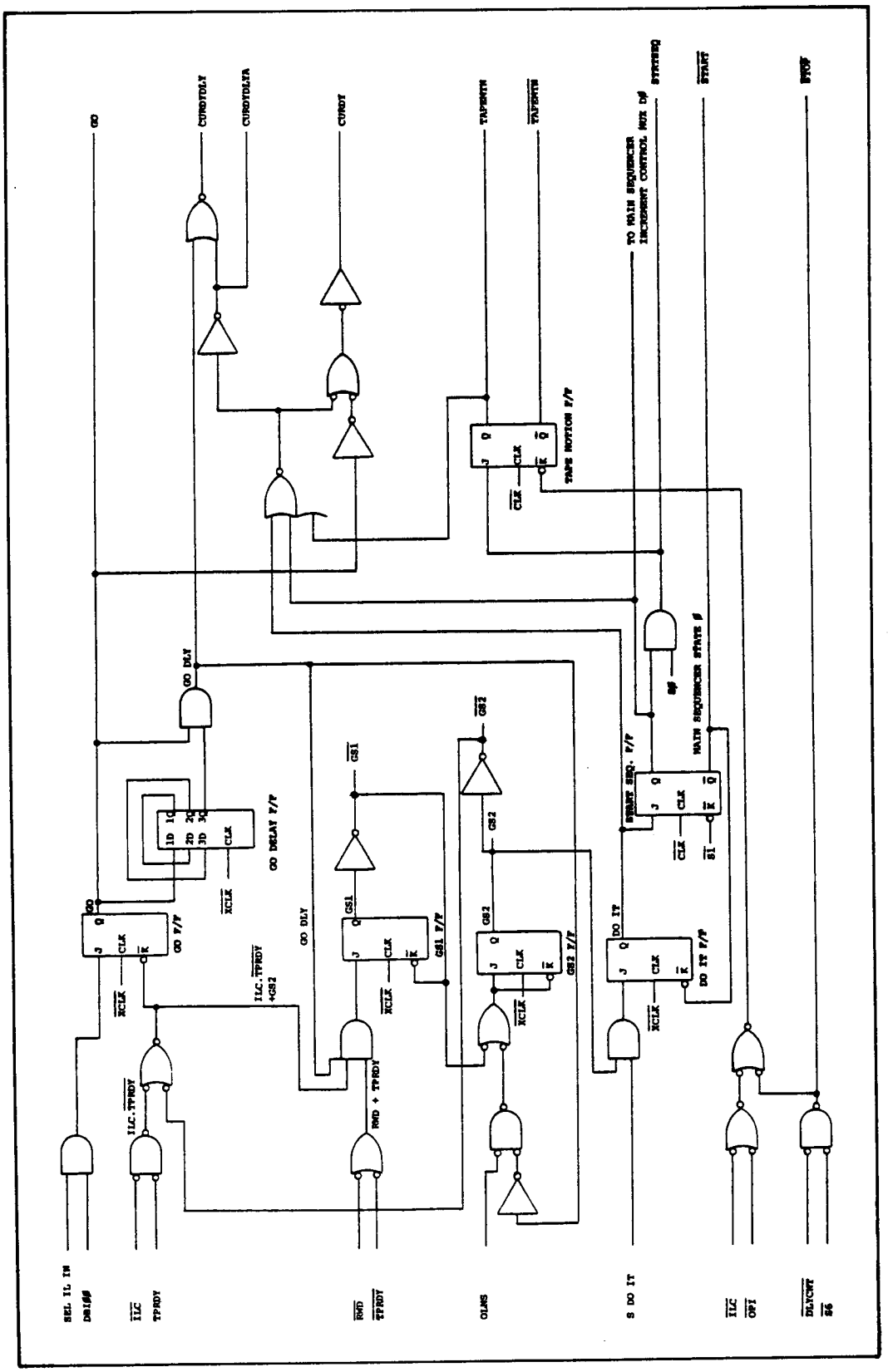


FIGURE 4-2: SIMPLIFIED SCHEMATIC START SEQUENCE

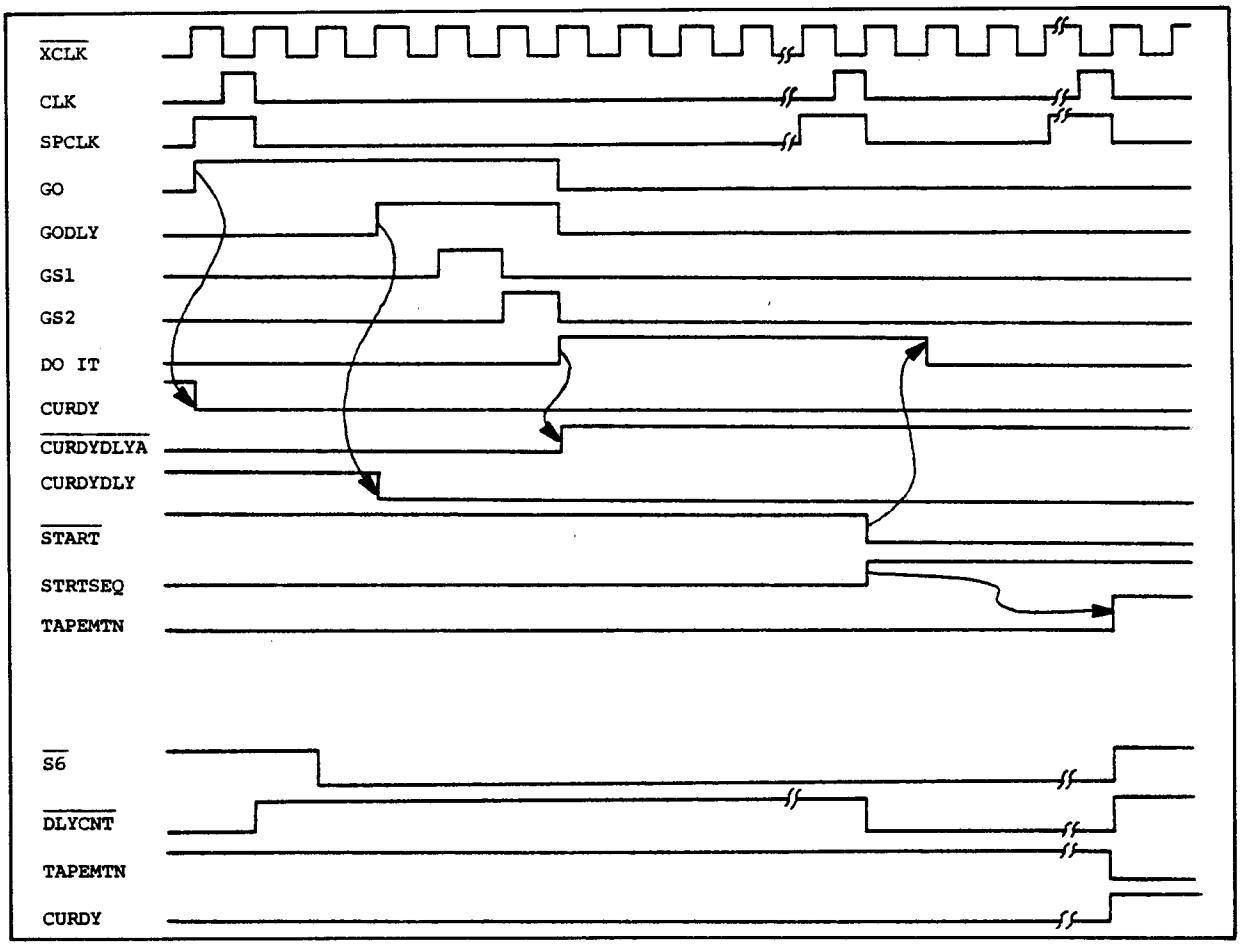


FIGURE 4-3: TIMING DIAGRAM START SEQUENCE

Three signals are used to show the controller is no longer ready. They are timed to go low at different times. CURDY goes low first, when GO goes true. CURDYDLY waits for GO DLY to go low. Finally, CURDYDLYA goes low when DO IT is true.

4.6 MAIN SEQUENCER

The Main Sequencer controls the order and timing of operations to complete a command.

Main Sequences block diagram, Figure 4-4, shows the relationship of major components in the Main Sequencer. There are eight states to the sequence and, with two exceptions, the states proceed in sequential order. External events (i.e., Write from BOT in State Ø) cause the sequence control to increment the sequencer after waiting for a predetermined delay entered into the delay counter. All logical functions are synchronized to CLK clock signal.

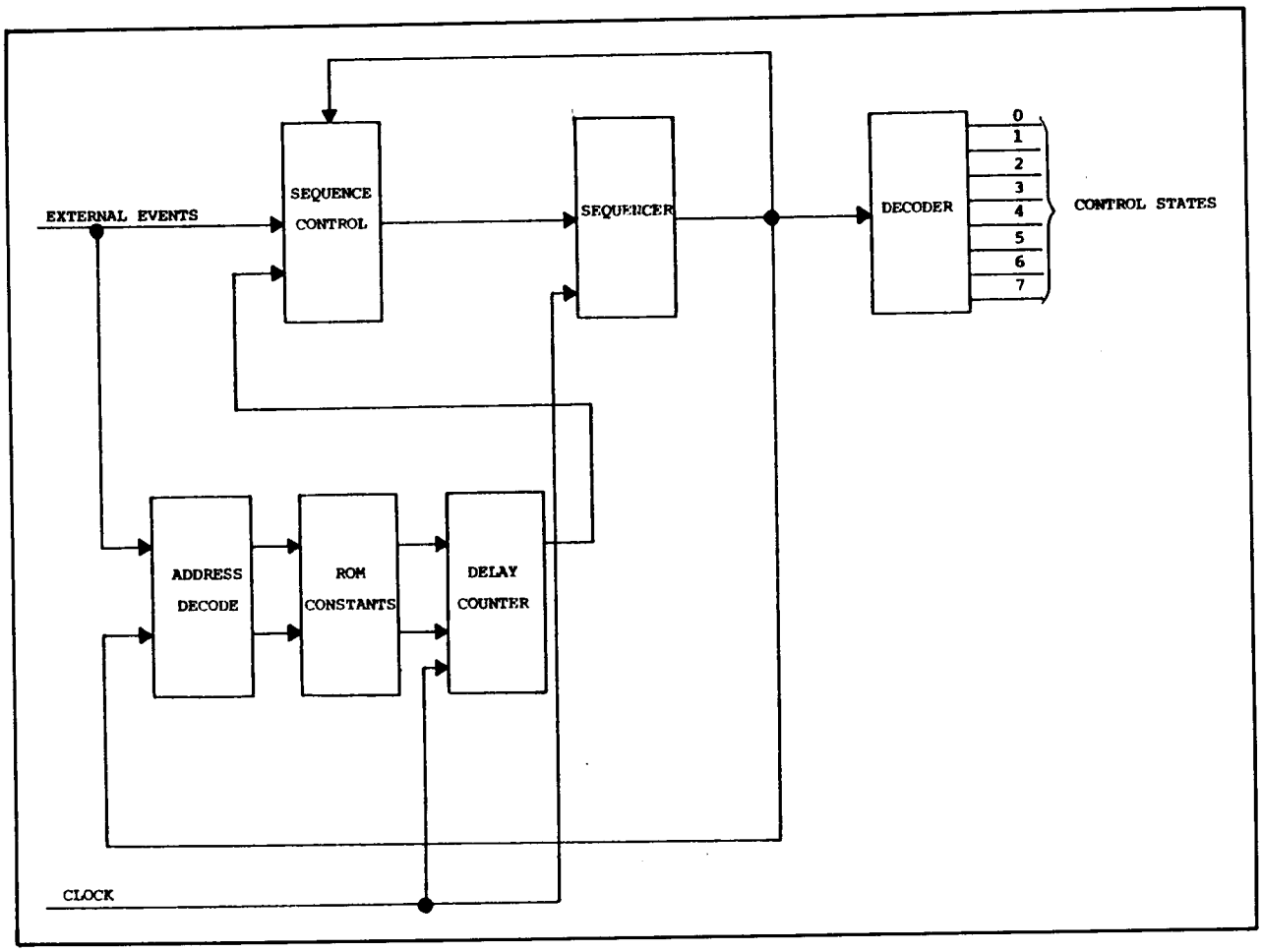


FIGURE 4-4: MAIN SEQUENCER BLOCK DIAGRAM

Figure 4-5 is a simplified schematic of the Delay Counter. The Delay Counter is made up of four cascaded counters, U42, U51, U83 and U81. A constant is side loaded into the counters from ROM's U52 and U82, and then counted down until an overflow occurs out of U81. The overflow becomes DLYCNT. The term LPDLY (load point delay) keeps the counter from incrementing when at load point. ROM address is a function of BCD output of the Main Sequencer and a decode of external events. Appendix A shows the ROM values and actual delay equivalent for all cases.

Figure 4-6 is a simplified schematic of the Main Sequencer. Components of the Sequencer are U74 Sequencer, Increment Control Mux U75, Side Load Control U73, and Decoder U64. U64 decodes the BCD output of sequencer counter U74 into eight individual states. U74 counts to eight states under the control of Side Load Control U73 or Increment Control U75. Sequencing is synchronized at CLK time. U74 is initialized to State Ø by an INIT signal, from the Unibus, completion of sequencing, or a catastrophic error condition. The Sequencer remains in State Ø waiting for a command from the processor. When a command is received and DO IT is set in the Start Sequence, Increment Control Mux U75 allows the Sequencer U74 to remain in a given state until an external input comes true and has timed out with the delay counter. Exceptions to this are for State 2 and State 5. When the Sequencer reaches State 2 during an operation other than any form of write, the Side Load Control U73 takes over and side loads a four into U74, thereby passing the Sequencer to State 4. State 3 is skipped entirely. From this it can be seen that State 3 is used only for write operations. The second condition requiring a side load is during a space operation when in State 5. If the Byte/Record Count has not yet reached zero, the space is not yet complete. U73 then side loads U74 with a four and forces the sequencer back into State 4. It can now be seen that during a space operation the Sequencer toggles between States 4 and 5 once for each record until the byte/record counter reaches zero and the last record has been found.

During normal operation when the Sequencer has reached State 7, and the delay counter has timed out U74 becomes reset to State Ø, and again waits for the next command.

Appendix A shows the flow of each state and ROM address and constants associated with each command.

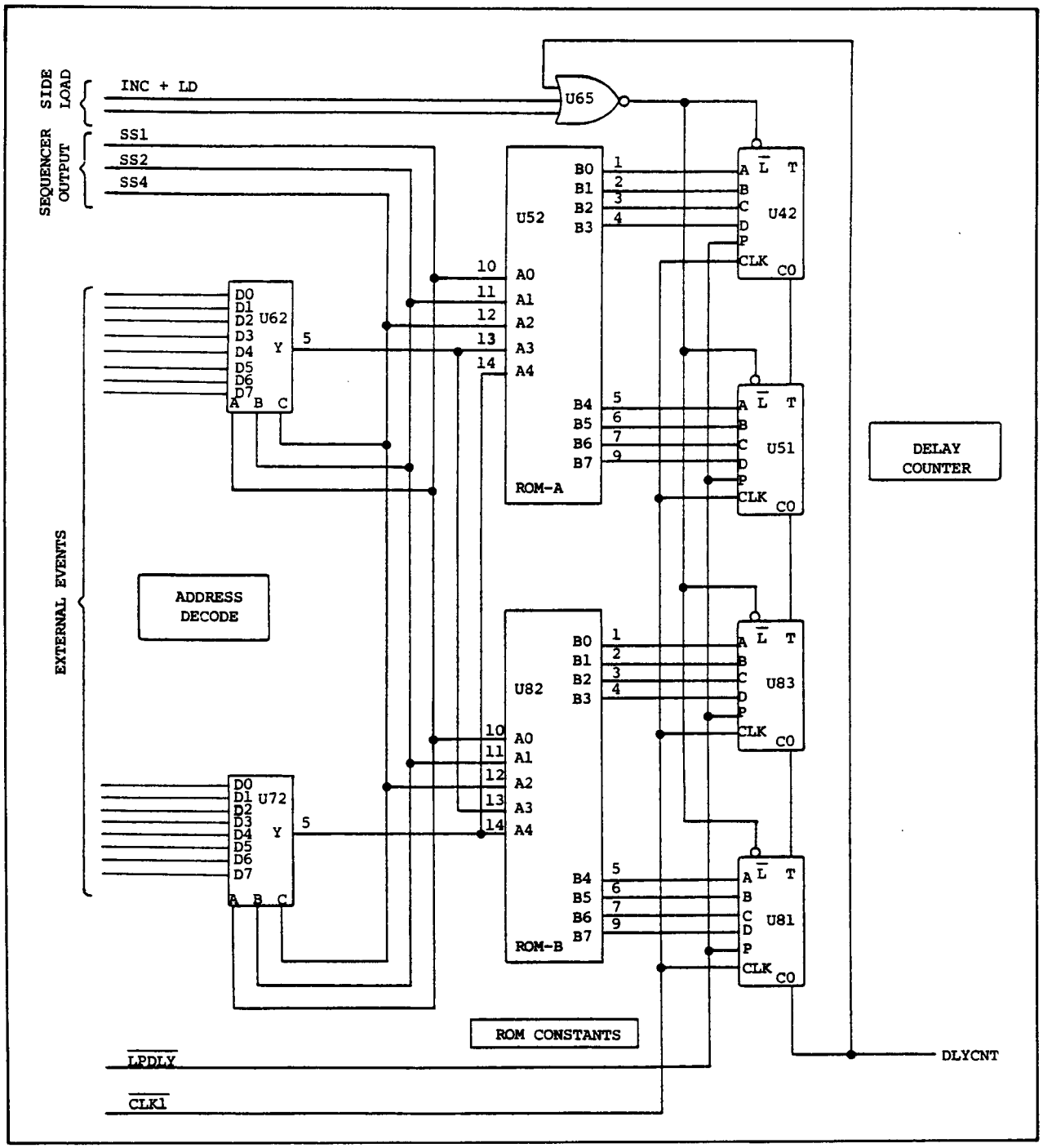


FIGURE 4-5: SIMPLIFIED SCHEMATIC DELAY COUNTER

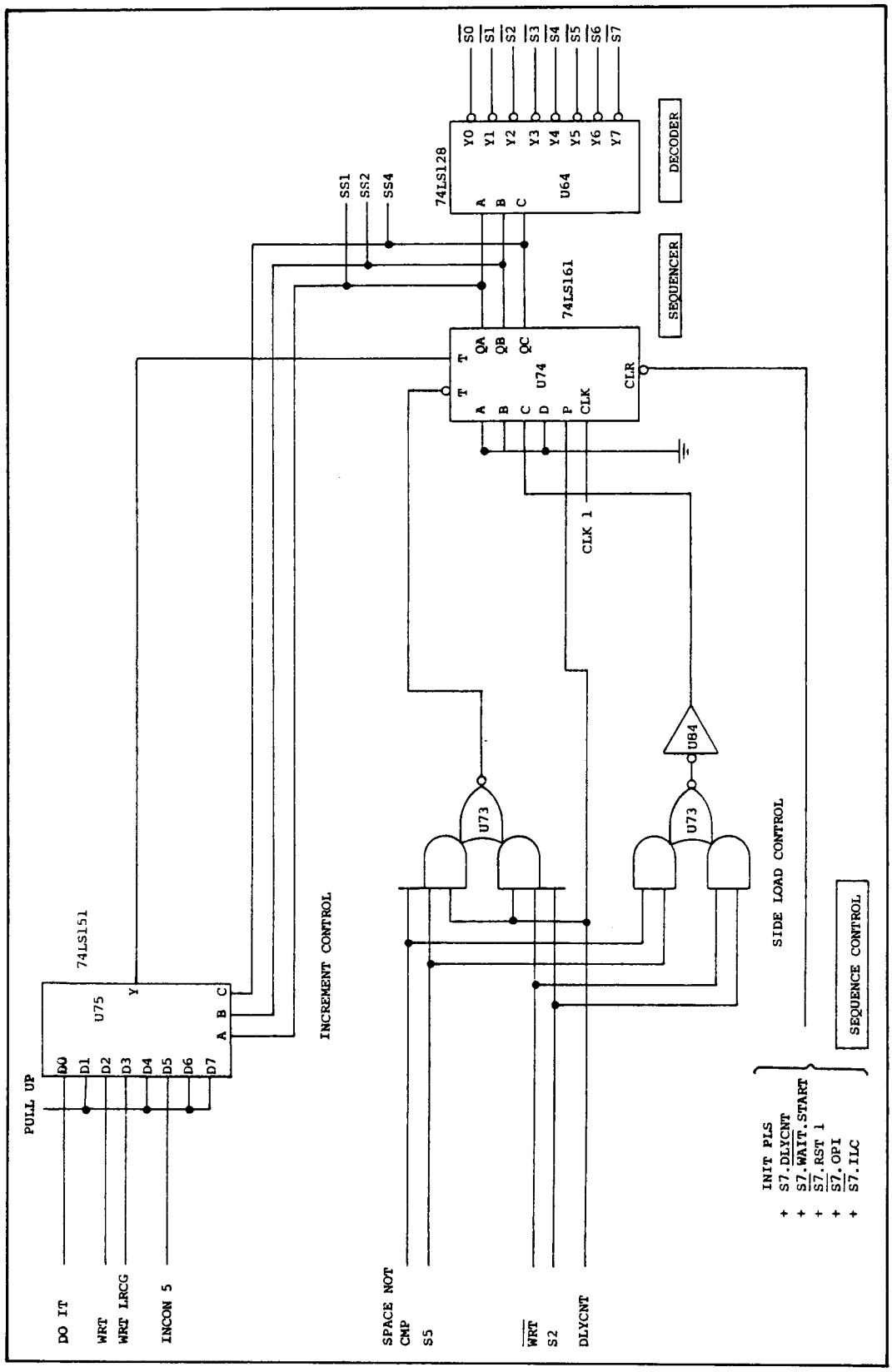


FIGURE 4-6: SIMPLIFIED SCHEMATIC MAIN SEQUENCER

4.7 MOTION CONTROL

An on-line tape drive will move tape under the following conditions:

- The drive is selected by SLT Ø through 5.
- One of the following motion control commands are issued:
  - SRC - Synchronous reverse
  - SFC - Synchronous forward
  - RWC - Rewind command

Absence of a SFC or SRC will cause the tape drive to halt.

SFC and SRC are a combination of the command $\overline{\text{SPRVS}}$, and the signal TAPEMTN from the Start Sequence Logic.

RWC is issued directly by a decode of the command to a $\overline{\text{RWD}}$ at go state 2 (GS2) time.

4.8 DATA TRANSFER

The PM-TC11 is capable of reading data from tape into a location on the Unibus and writing data on tape from a Unibus location. All data transfer is accomplished via Unibus NPR transfer method. Data is held in a buffer (FIFO) within the controller to prevent differences in timing (processor or tape drive) from affecting reliable operation. A description of FIFO operation is included in the data sheet in Appendix C.

Refer to the Write Data Path of Figure 4-7 detailed block diagram. A write command brings one word of data from a Unibus location under NPR Control (DATI). Sixteen bits of data enter through the bus receivers and go through the Assemble Mux to the MTD registers. The 16 bits are then presented to the Disassemble Mux and are formed into a tape character there under control of the Assemble/Disassemble control logic. The 8-bit tape character is then processed by the FIFO input mux and presented to the FIFO input. The FIFO input data is sampled and used to generate a CRC character which is presented to the FIFO input mux for entry at CRC time.

Parity is generated from the FIFO input data, FIDØ through FID7, and is presented to the FIFO through the flag input. This, along with FIFO input data FIDØ through FID7, is entered into the FIFO by the FIFO control circuitry. When the Main Sequencer is in State 3, the FIFO control circuitry takes the character from the FIFO and transmits it to the tape drive. After a word is transferred from the Unibus, the MTBRC and MTCMA registers are incremented. When an entire computer word (16 bits) have been entered into the FIFO, and the MTBRC is not at zero, and the FIFO is not full, another NPR transfer is

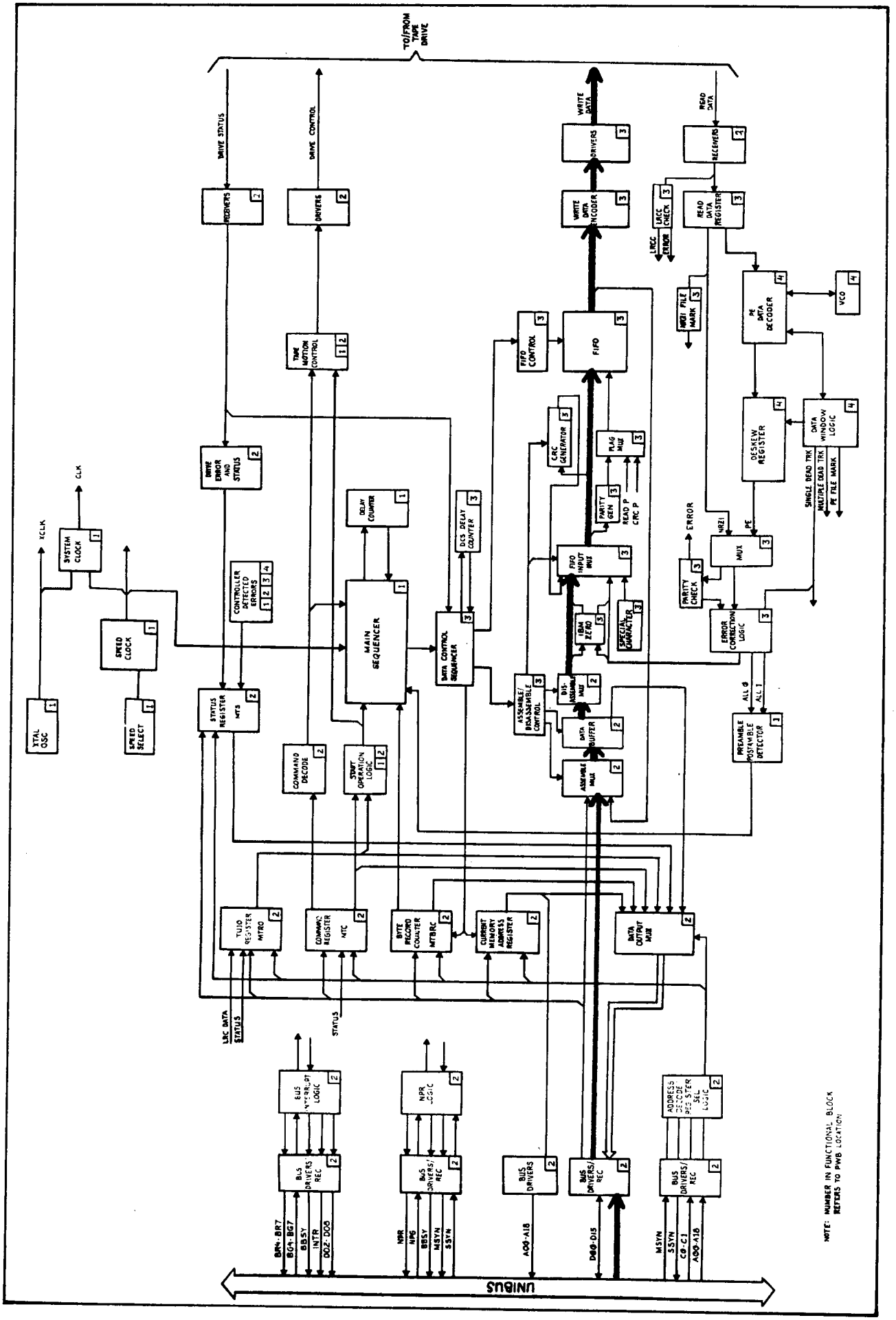


FIGURE 4-7: WRITE DATA PATH

initiated. This cycle continues until the MTBRC is incremented to zero and an overflow occurs.

A sub-state sequencer, the Data Control Sequencer, controls the data format on the tape by controlling the MUXES and FIFO control. The data control sequencer has eleven states and does not proceed in sequential order. The completion of one state and an external event will cause the next state to set. The table on Schematic Sheet 11 of SD701720 shows the function of each state.

Data is formatted on tape by filling the FIFO with everything to be written on tape, then taking it out one character at a time until the entire record is written. In the case of a nine-track NRZI record data will be loaded, then three null characters, the CRC character and three more null characters. An LRC flag is then loaded into the FIFO. When writing from the FIFO, the data, mux characters, CRC, and null characters are brought out and transmitted to the tape drive. When the LRC flag appears, a reset (WARS) is issued to the tape drive. The drive then generates an LRC on tape. The LRC does not come from the controller. When writing PE, a preamble of forty zeroes and one all ones character is loaded, then data, followed by one all ones character, and again forty zeroes.

When writing a PE tape character, the write data encoder provides the mid-bit cell transition to create a PE data bit.

Refer to the Read Data Path of Figure 4-8 detailed block diagram. A read command causes a record of data to be read from tape into the Unibus.

Two distinct paths are taken for read data; one for NRZI data and another for PE data. NRZI data is usable just as it comes from the tape drive, but PE data must be synchronized to define a bit cell time and detect data. Also, each bit must be deskewed to form a tape character. A preamble must also be detected. This preamble facilitates data synchronization.

Both NRZI and PE data are read into the controller through the receivers and read data register at Main Sequencer State 4. Data is also being sampled by the LRC check logic to make the longitudinal check of a NRZI record. This is accomplished by toggling a J-K flip-flop for each ones bit every time a character is read in. Since the tape drive does the same thing during a write, the LRC character on tape for that record will be the compliment of the final state of all J-K flip-flops. When read back out, the LRC character will toggle the checker's flip-flops for that final time and all should be in the zero state. When this happens, an LRC MATCH is made and the record is OK. If a bit was dropped or a number of bits were dropped, the final state of the J-K flip-flops will not be all zeroes and LRCMATCH will not be made. An LRC error will be generated.

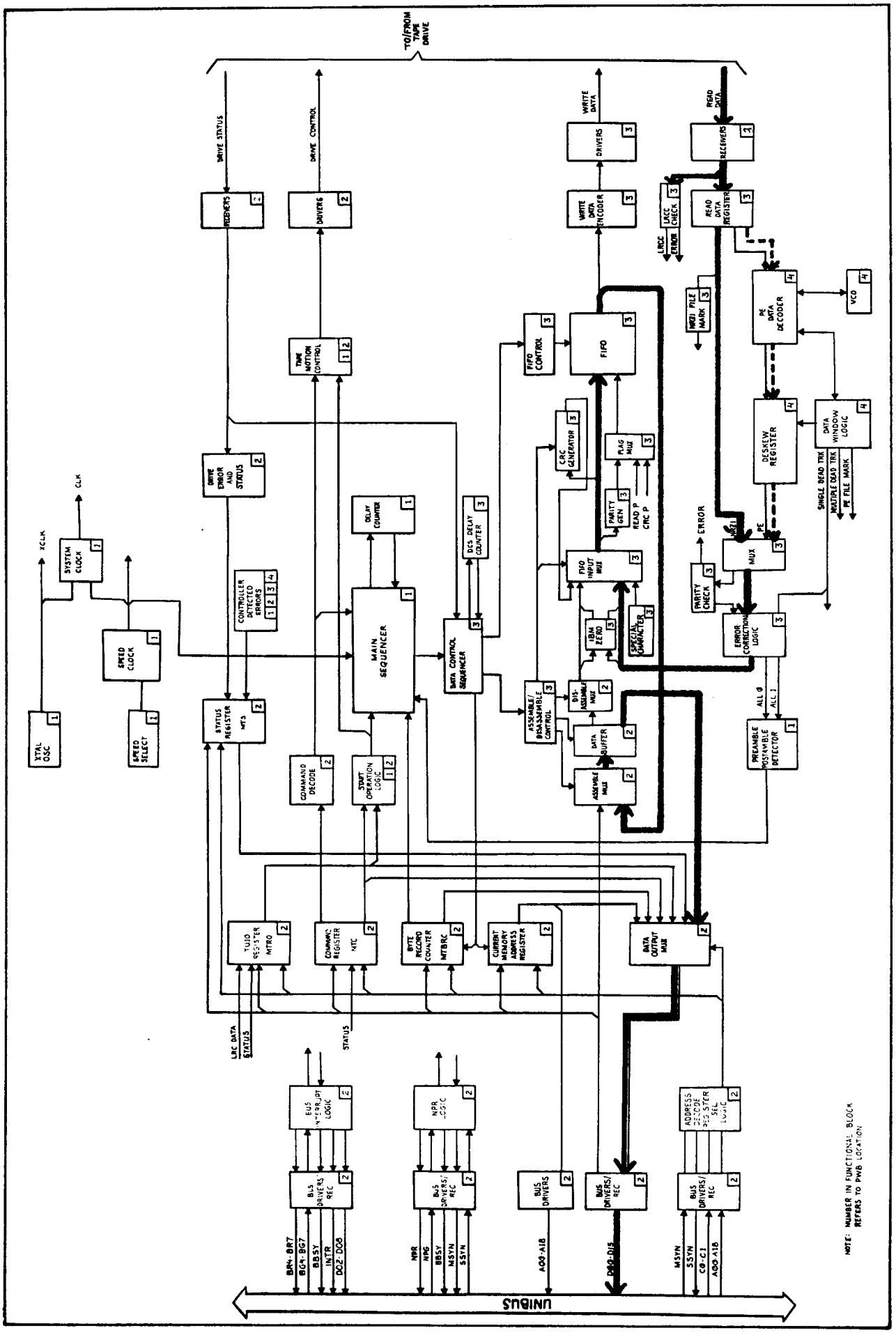


FIGURE 4-8: READ DATA PATH (NRZI DATA) ——— (PE DATA) — — — —

Data is then read through the data mux and into the error correction logic. A parity check is made of data coming out of the data mux and an error is set if improper parity is found. The data mux accepts data directly from the read data register only if reading NRZI data. If reading PE data, the data mux receives the data from the deskew registers on Board #4.

As mentioned earlier, reading PE data is considerably different than NRZI. The PE control Board #4 takes care of most of the differences for reading the PE data and presents this data in usable form to the data mux in Board #3.

PE data is read during Main Sequencer State 4. The delay counter is held in a load condition until a record is detected. When tape begins to move, all tracks are dead. The first data transition seen causes a channel active condition. Since there are no read strobes (RDSTB) associated with PE data, one must be generated. In PE this comes from the VCO (voltage controlled oscillator). The VCO is controlled initially by VCOR which comes from the system clock. When a channel becomes active, VCO becomes controlled by Track 1 or Track 2 clocking signal. If both tracks are dead, control again goes to VCOR. The forty zeroes in the preamble are used to synchronize data and define a bit cell. When CHANACT has been true for 16-bit cells, the term LOCK comes true and defines the bit cell time. If a transition does not occur within one bit cell time, a track is declared dead. Data transitions occurring within a bit cell window are used to clock the data bit into the skew register after the first ones bit has been detected. The skew registers can deskew up to four bits of data for a tape character. An explanation of the skew register operation is available from the data sheet included in Appendix B. Data from the skew registers are brought to the Data MUX. Parity is checked after the data mux. When during a PE read, if one track is dead, parity will be used in the error correction logic to correct for that dead track.

After the error correction logic, all data is treated the same (NRZI and PE). The FIFO Input MUX directs the data into the FIFO under control of the FIFO Control Circuitry. When a character is in the FIFO, it is then taken out by FIFO control circuitry and brought to the assemble mux where a complete word (16 bits) is assembled and placed in the MTD. When a word has been assembled, an NPR request is generated and the word is then transferred from MTD to the Unibus via the Data Output MUX.

The end of a record is determined by a read timeout. This is defined as no read strobe for two-and-a-half bit cells. When this occurs, DLYCNT is issued and the main sequencer goes to State 5.

In NRZI the CRC character will be read three bit cell times after the end of data. The CRC generator is continuously sampling data going into the FIFO. When the CRC character is read, the resultant generated CRC should be zero. If it is not, a CRC error is reported.

In PE the record is considered ended when an all ones character followed by thirty-eight all zeroes characters are read. This is determined by the PE Postamble Detection Logic. CRC and LRC are not read or detected in PE.

4.8.1 File Marks

A File Mark is a unique character (record) placed on tape and used by the computer program to detect an end of a file on tape. A file may be an arbitrary number of records defined by the system program. A number of File Marks may also be used by an individual program as flags for a specific purpose unique to that program.

A different File Mark is defined for PE and NRZI. For NRZI a File Mark is a record with one character (a 23_8 for nine-track, a 17_8 for seven-track) followed by and LRC (which will be equal to the tape character).

A PE tape record is recognized by the controller as being a File Mark if tracks 2, 6 and 7 are active, tracks 1, 3 and 4 are dead, and tracks 0, 5 and parity are either active or dead.

A PE File Mark is written on tape by writing forty zeroes with tracks 1, 3 and 4 dead.

4.9 ERRORS

Errors are reported to the processor by setting the error bit (Bit 15) in the command register (MTC) and setting a bit in the status register (MTS) unique to the error. In this manner the error bit acts as a flag and the program can then examine the status register to determine the cause.

The status register is read onto the data lines through the data mux on Board #2 (703290) by $\overline{\text{SELOOUT}}$ signal. The DEC TM11 controller is intended to be used with an 800 BPI (NRZI only) tape drive. Therefore, to extend the use of the predefined registers to 1600 BPI (PE) and still be compatible, it was necessary to define some bits as multipurpose.

Parity error is one such multipurpose bit. It is used in both PE and NRZI to signify a character parity error. It is also used in PE to indicate multiple (more than one) dead tracks. Logic for this can be seen on Sheet 8 of SD701700.

When reading a PE record, if a Skew Register becomes full and another bit is entered into it, a skew error is declared. This condition will cause the error bit to be set in MTC but no bits will be set in the status register (MTS).

4.10 TAPE DRIVE INTERFACE

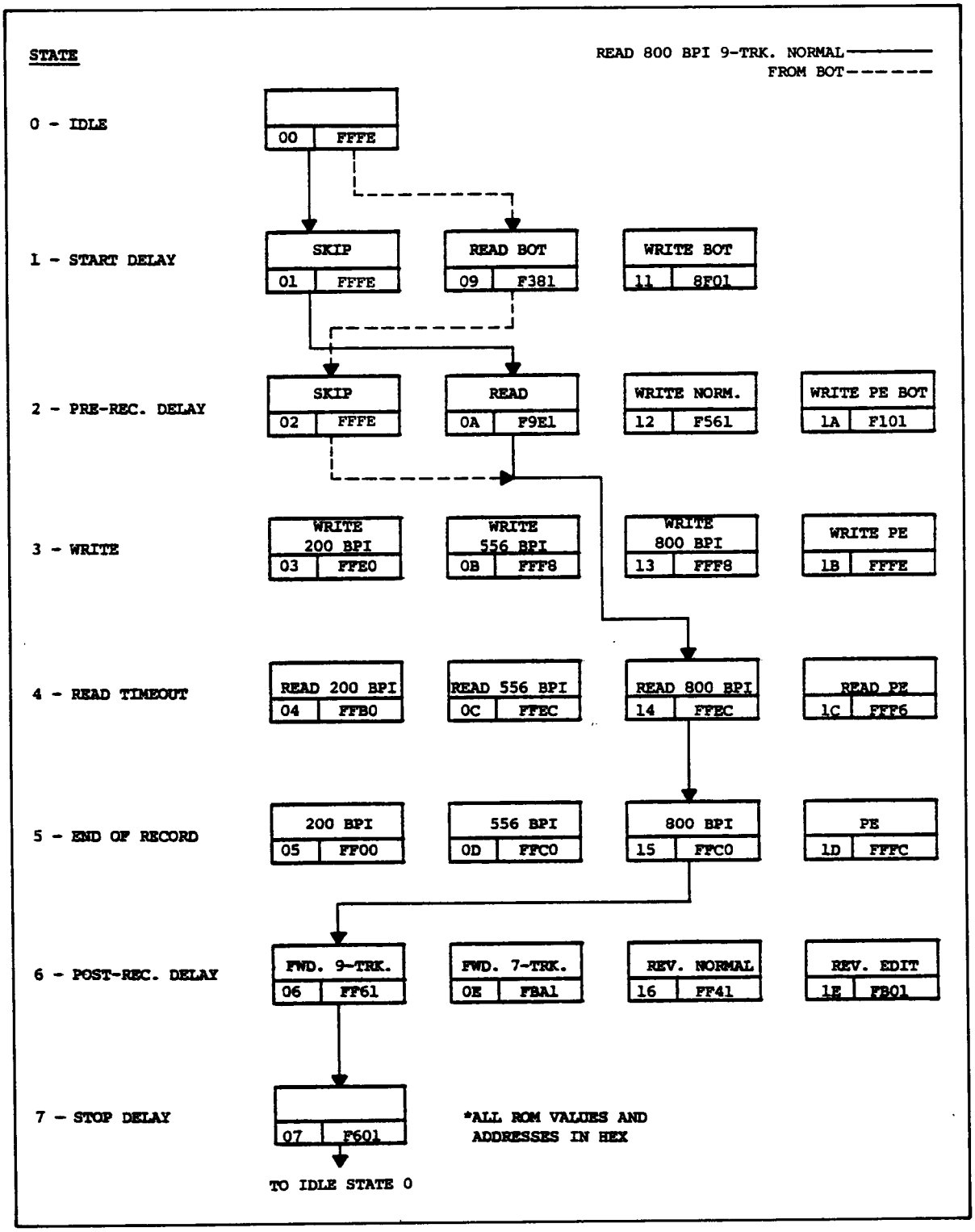
Drivers and receivers are TTL level devices. All drivers are open collector type from the controller and should be terminated on the last tape drive only by 220/330Ω pull up/ pull down terminator resistors. All receivers are pulled up to +5 volts through 220Ω and down to ground by 330Ω at the controller.

Appendix A

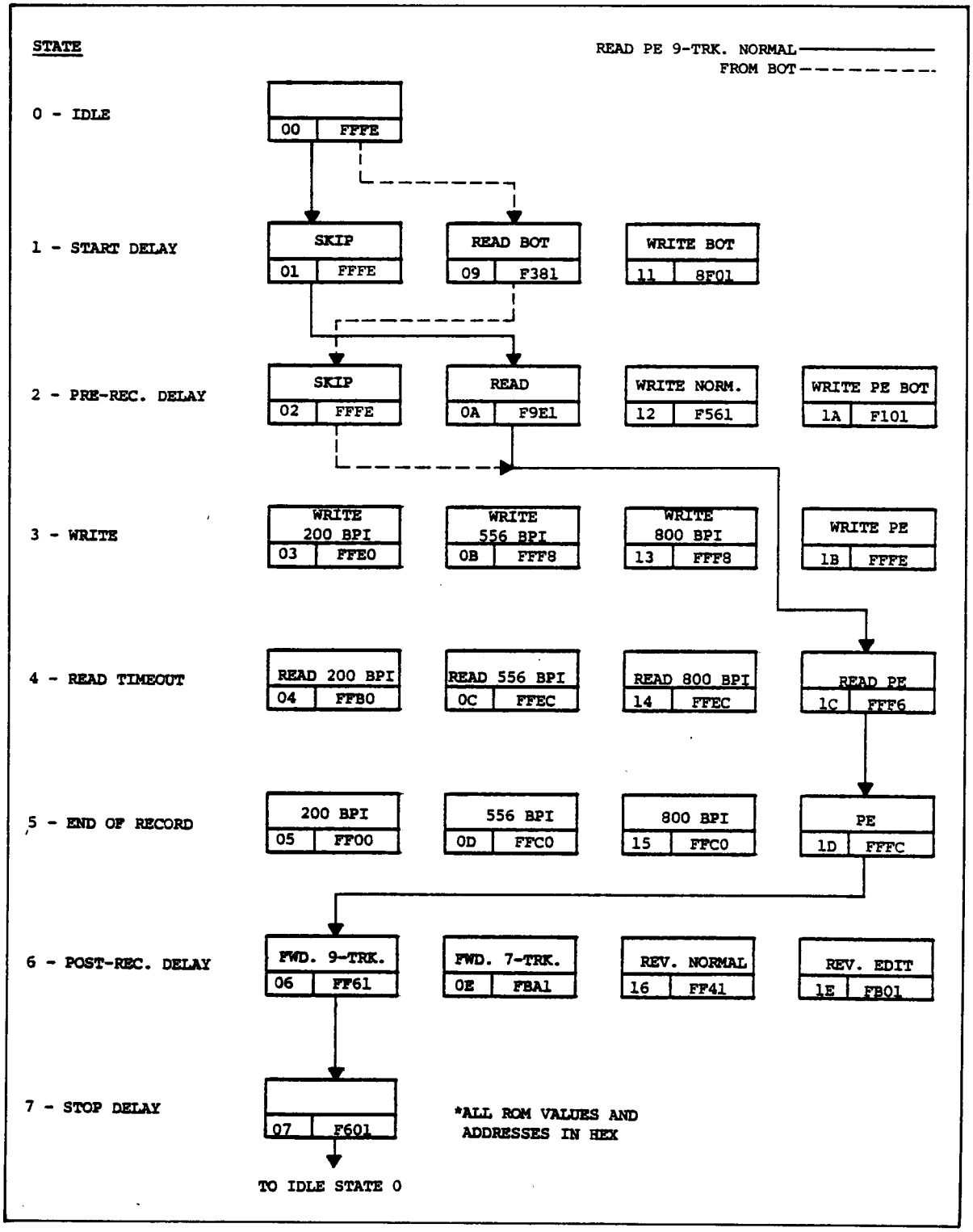
ROM Constants

MAIN SEQUENCER STATE	DENSITY BPI	DELAY PERIOD AT TAPE SPEED						ROM ADD. (HEX)	ROM VALUE (HEX)	CONSTANT VALUE (DEC)	*5MHz CLOCK FUNCTION
		12.50ips	25.00ips	37.50ips	45.00ips	75.00ips	125.00ips				
0	All	12.50µs	6.25µs	4.17µs	3.47µs	2.08µs	1.25µs	00	FFFE	2	
1	All	12.50µs	6.25µs	4.17µs	3.47µs	2.08µs	1.25µs	01	FFFE	2	Skip
	All	39.99ms	19.99ms	13.34ms	11.10ms	6.65ms	4.00ms	09	F381	3199	Start Delay - Read from BOT
	All	361.59ms	180.79ms	120.63ms	100.38ms	60.17ms	36.16ms	11	8F01	28927	Start Delay - Write from BOT
2	All	12.50µs	6.25µs	4.17µs	3.47µs	2.08µs	1.25µs	02	FFFE	2	Skip
	All	19.59ms	9.79ms	6.53ms	5.44ms	3.26ms	2.00ms	0A	F9E1	1567	Start Delay - Read Normal
	All	33.99ms	16.99ms	11.34ms	9.43ms	5.66ms	3.40ms	12	F561	2719	Start Delay - Write Normal
	1600	47.99ms	23.99ms	16.00ms	13.30ms	7.99ms	4.80ms	1A	F101	3839	Start Delay - Write PE from BOT
3	200	400.00µs	200.00µs	133.44µs	111.04µs	66.56µs	40.00µs	03	FFE0	32	Write
	556	144.00µs	72.00µs	48.00µs	40.00µs	24.00µs	14.40µs	0B	FFF8	8	Write*
	800	100.00µs	50.00µs	33.36µs	27.76µs	16.64µs	10.00µs	13	FFF8	8	Write
	1600	12.50µs	6.25µs	4.17µs	3.47µs	2.08µs	1.25µs	1B	FFFE	2	Write
4	200	1.00ms	500.00µs	333.60µs	277.60µs	166.40µs	100.00µs	04	FFB0	80	Read Timeout
	556	360.00µs	180.00µs	120.00µs	100.00µs	60.00µs	36.00µs	0C	FFEC	20	Read Timeout*
	800	250.00µs	125.00µs	83.40µs	69.40µs	41.60µs	25.00µs	14	FFEC	20	Read Timeout
	1600	25.00µs	12.50µs	8.34µs	6.94µs	4.16µs	2.50µs	1C	FFF6	10	Read Timeout
5	200	3.20ms	1.60ms	1.07ms	888.30µs	532.50µs	320.00µs	05	FF00	256	End of Record
	556	1.15ms	576.00µs	384.00µs	320.00µs	192.00µs	115.20µs	0D	FFC0	64	End of Record*
	800	800.00µs	400.00µs	266.90µs	222.00µs	133.10µs	80.00µs	15	FFC0	64	End of Record
	1600	50.00µs	25.00µs	16.68µs	13.88µs	8.32µs	5.00µs	1D	FFFC	4	End of Record
6		1.99ms	99.37µs	663.00µs	551.00µs	330.70µs	198.80µs	06	FF61	159	Read
		2.86ms	1.43ms	954.00µs	795.00µs	477.00µs	286.20µs				Write* Post Delay Forward 9-track
		13.99ms	6.99ms	4.67ms	3.88ms	2.33ms	1.40ms	0E	FBA1	1119	Read
		20.14ms	10.07ms	6.70ms	5.60ms	3.36ms	2.00ms				Write* Post Delay Forward 7-track
		2.39ms	1.19ms	796.50µs	662.80µs	397.30µs	238.80µs	16	FF41	191	Read
		3.44ms	1.72ms	1.15ms	955.00µs	573.00µs	343.80µs				Write* Post Delay Reverse Normal
		15.99ms	7.99ms	5.34ms	4.44ms	2.66ms	1.60ms	1E	FB01	1279	Read
		23.02ms	11.51ms	7.67ms	6.40ms	3.84ms	2.30ms				Write* Post Delay Reverse Edit
7	All	31.99ms	15.99ms	10.67ms	8.88ms	5.33ms	3.20ms	07	F601	2559	Stop Delay
OSCILLATOR'S BASIC											
7.2MHz OSC 139µs		12.50µs	6.25µs	4.17µs	3.47µs	2.08µs	1.25µs	} SPEED CLOCK (SPCLK) PERIOD			
5.0MHz OSC 200µs		18.00µs	9.00µs	6.00µs	5.00µs	3.00µs	1.80µs				

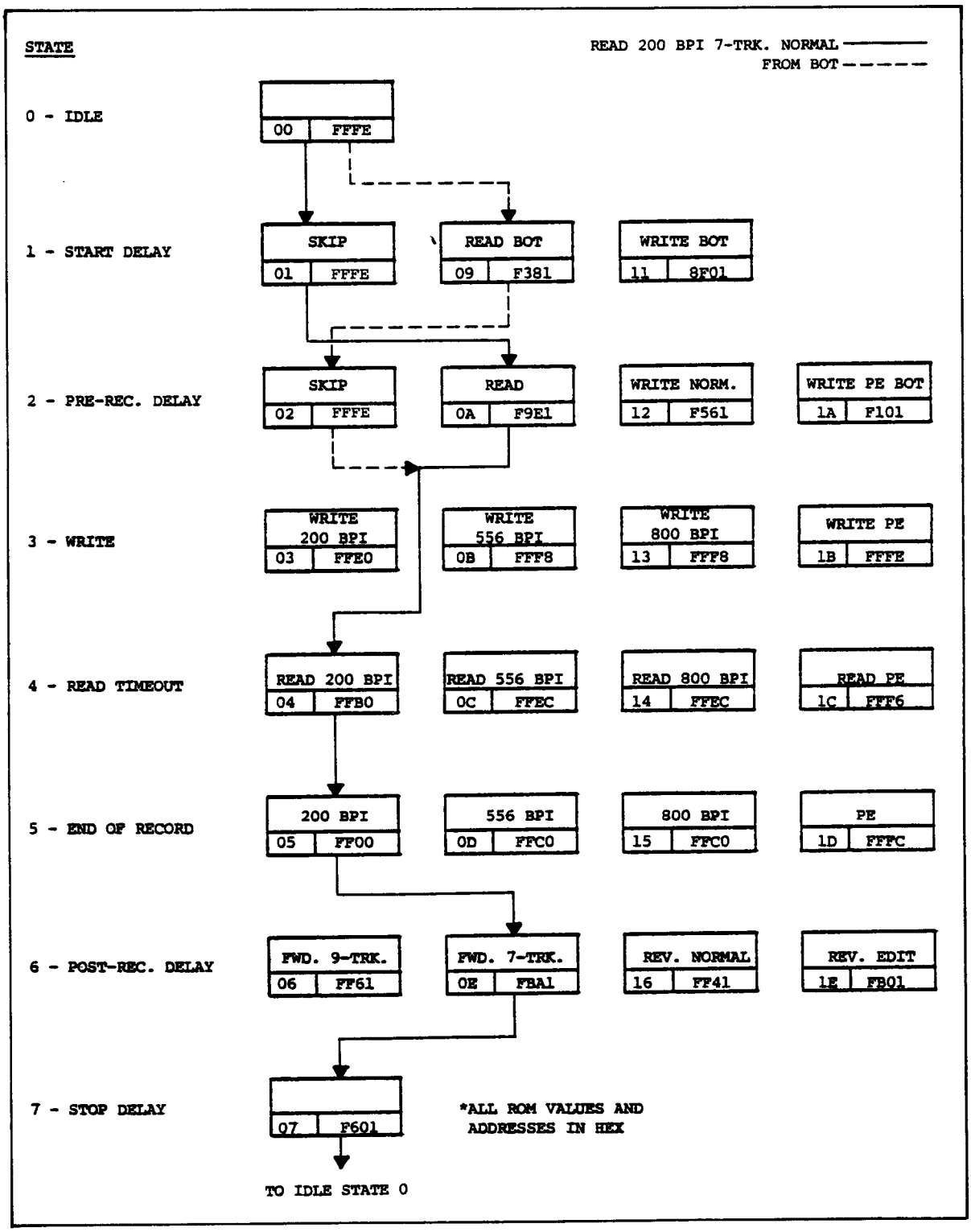
ROM CONSTANTS



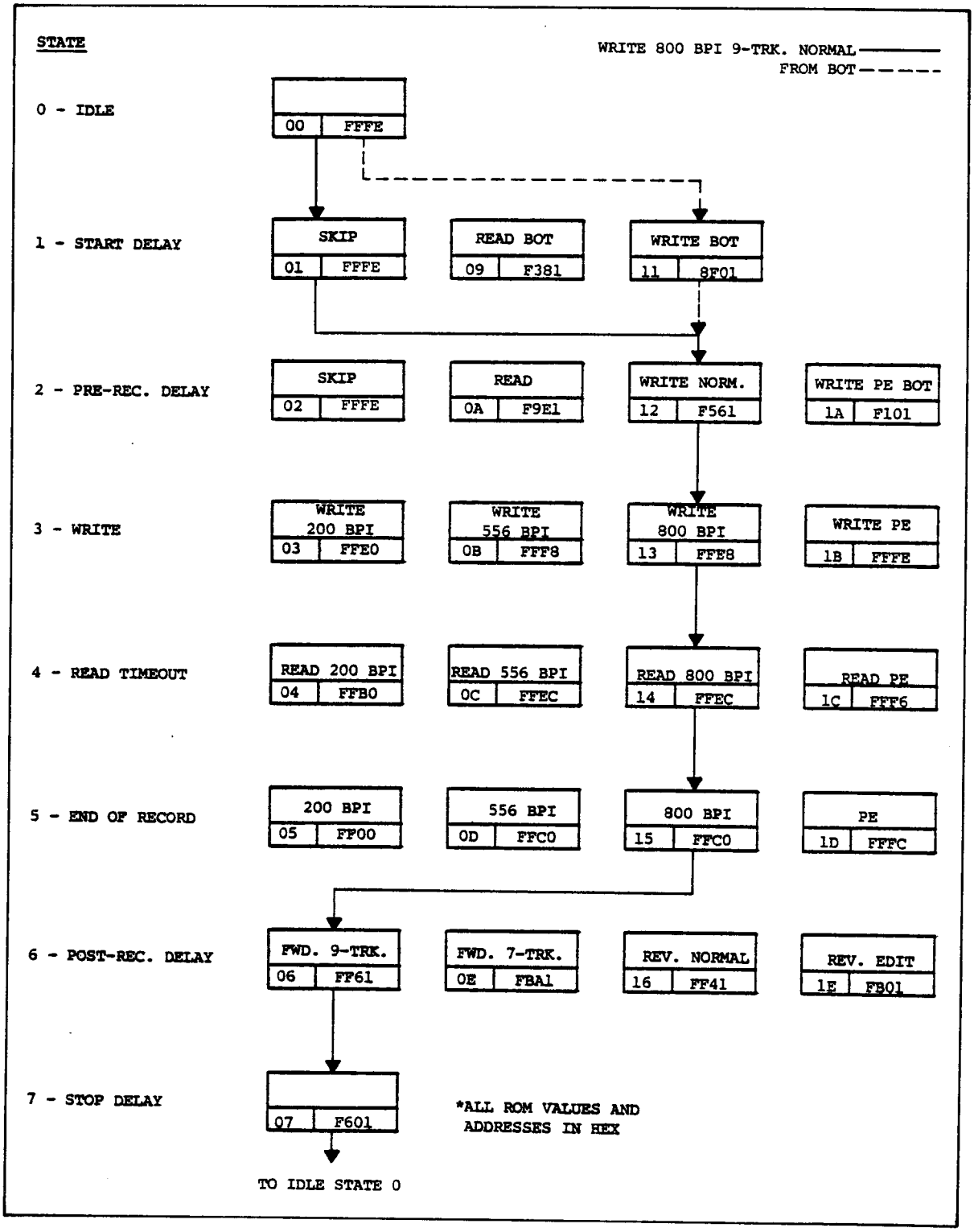
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



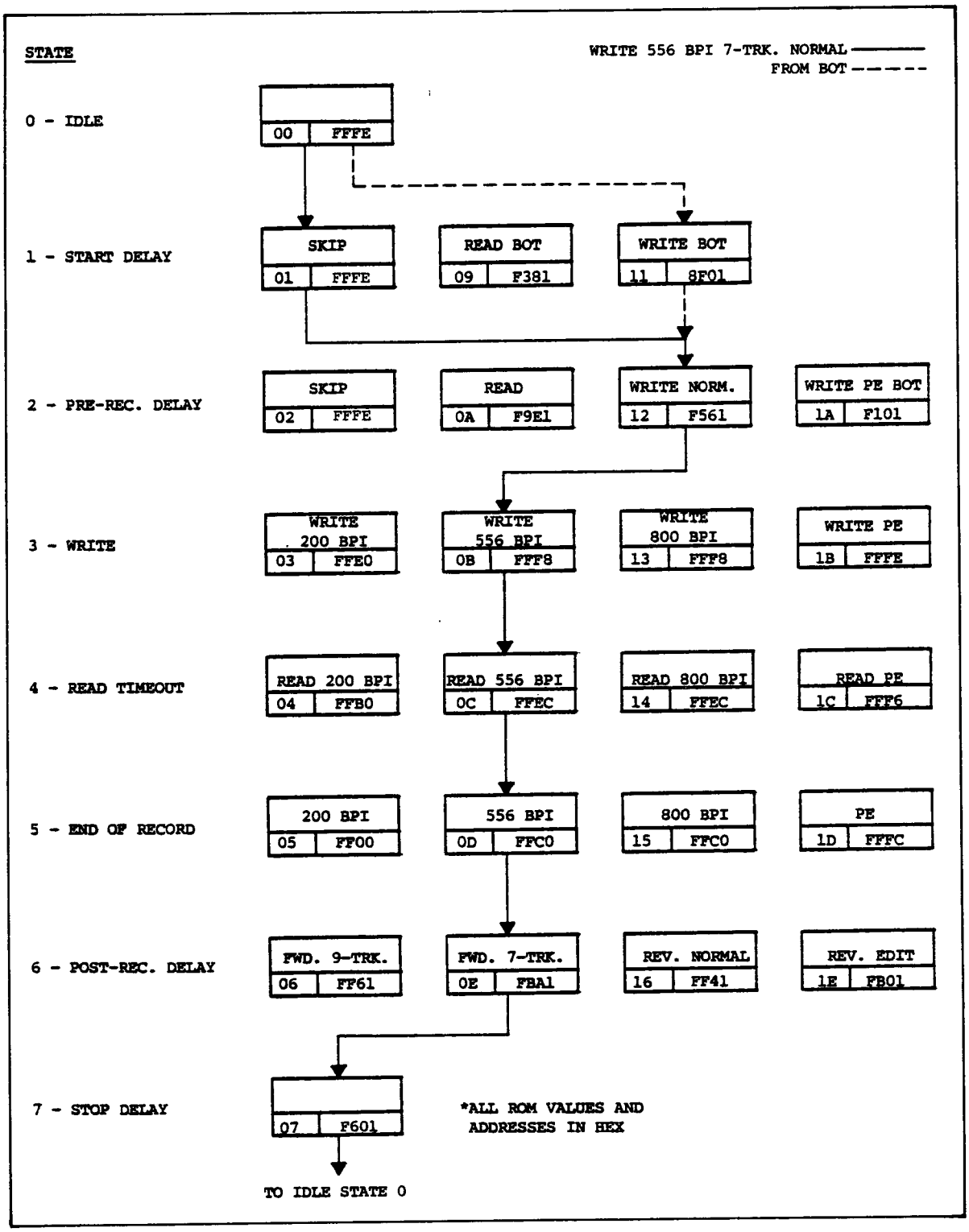
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



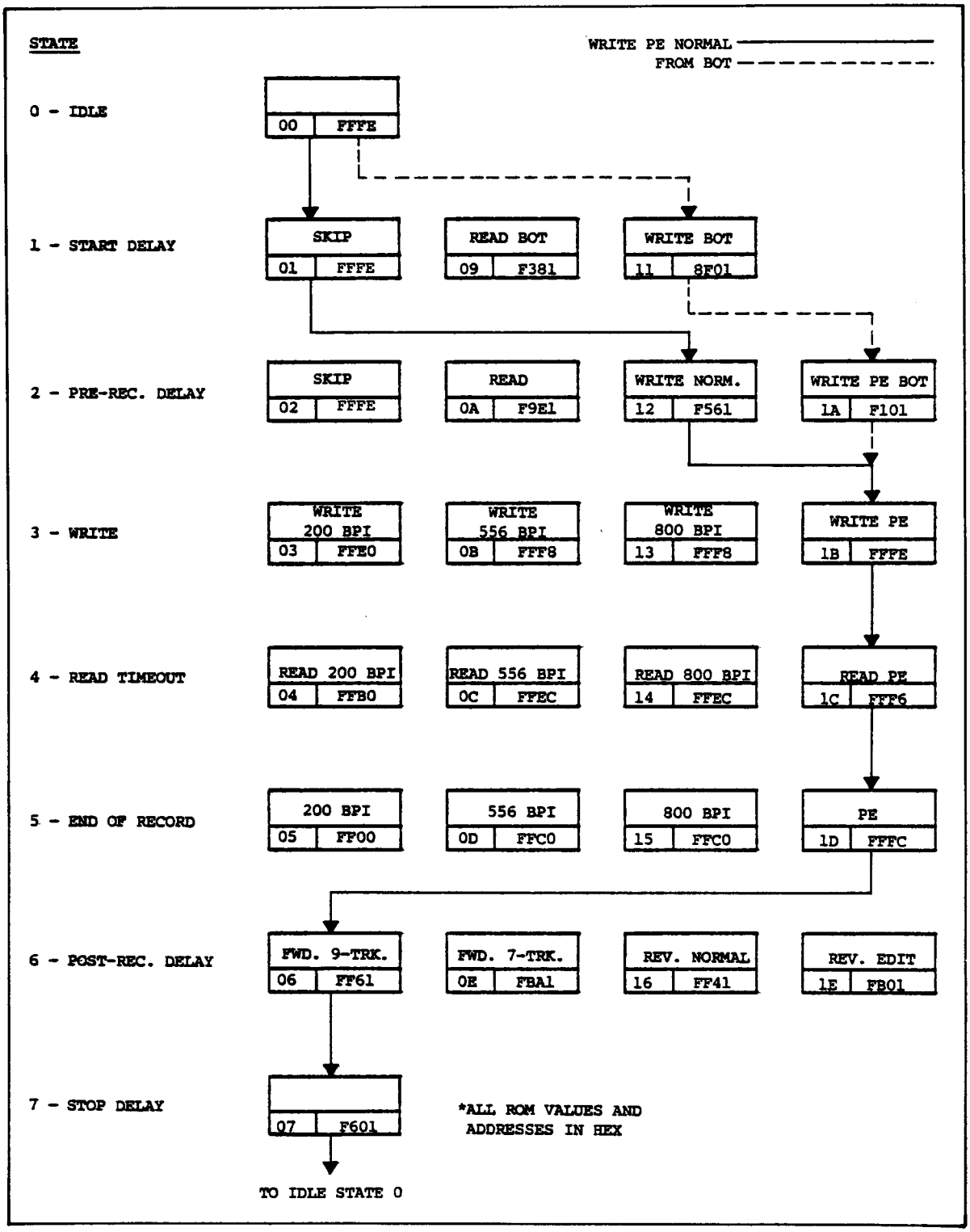
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



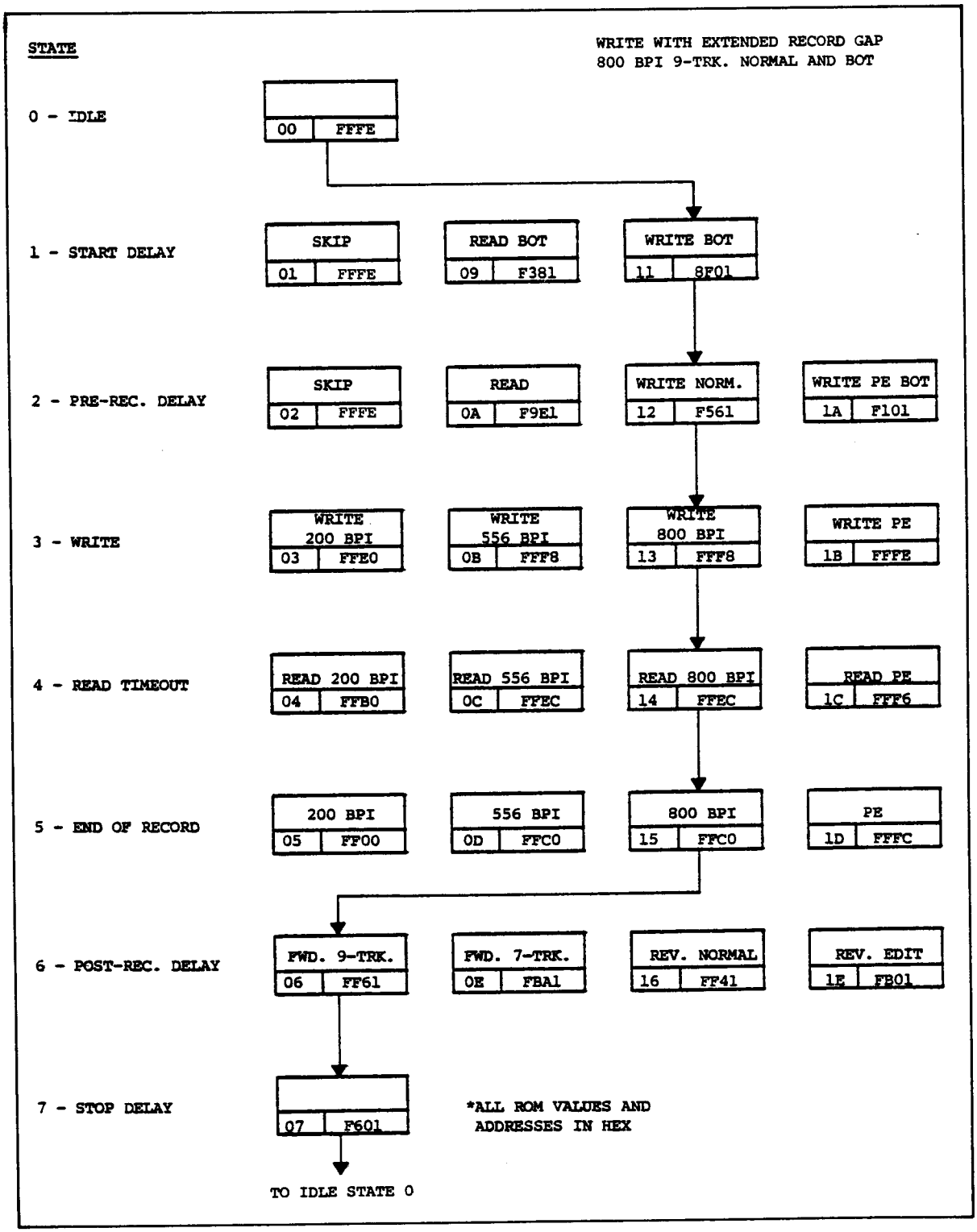
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



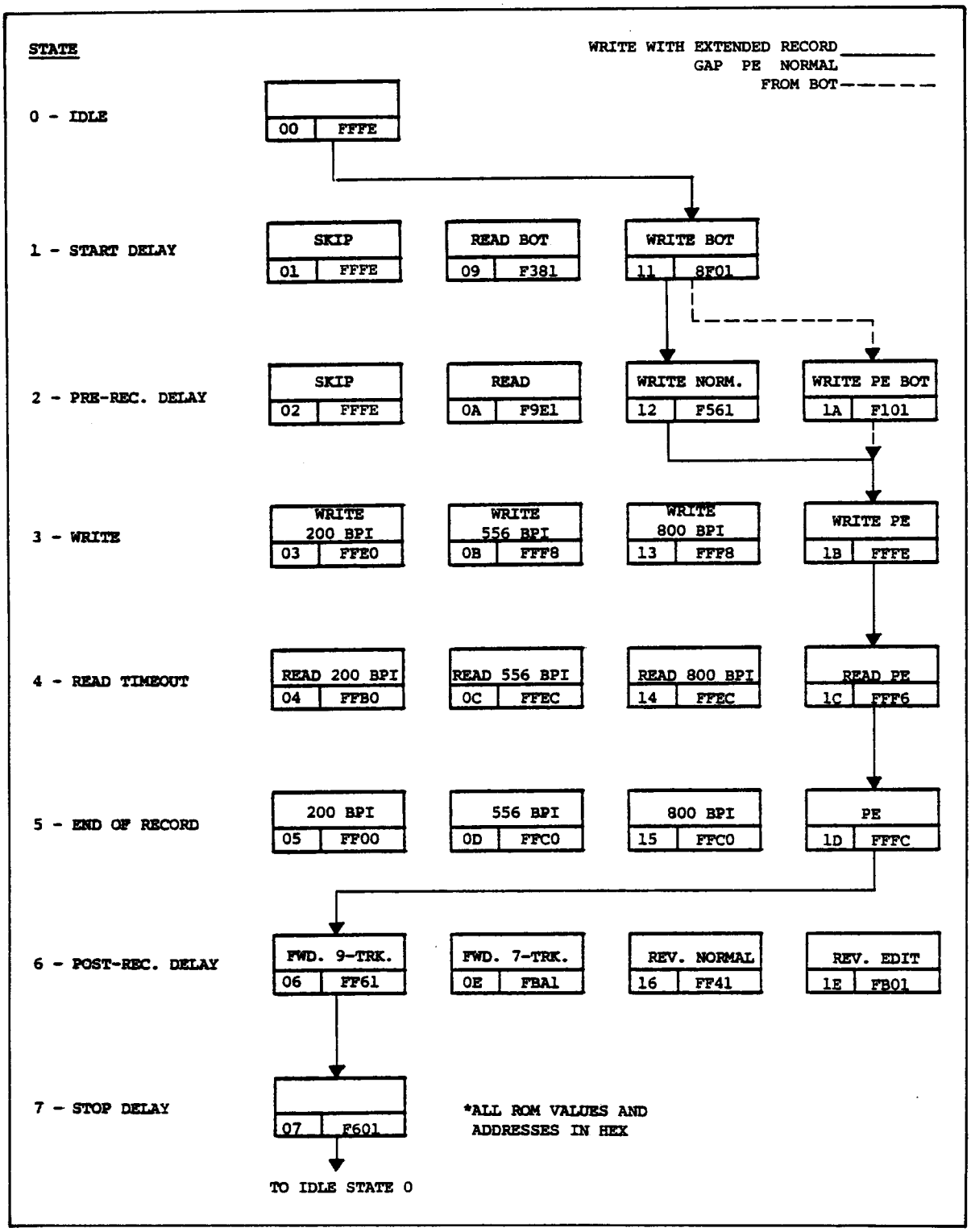
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



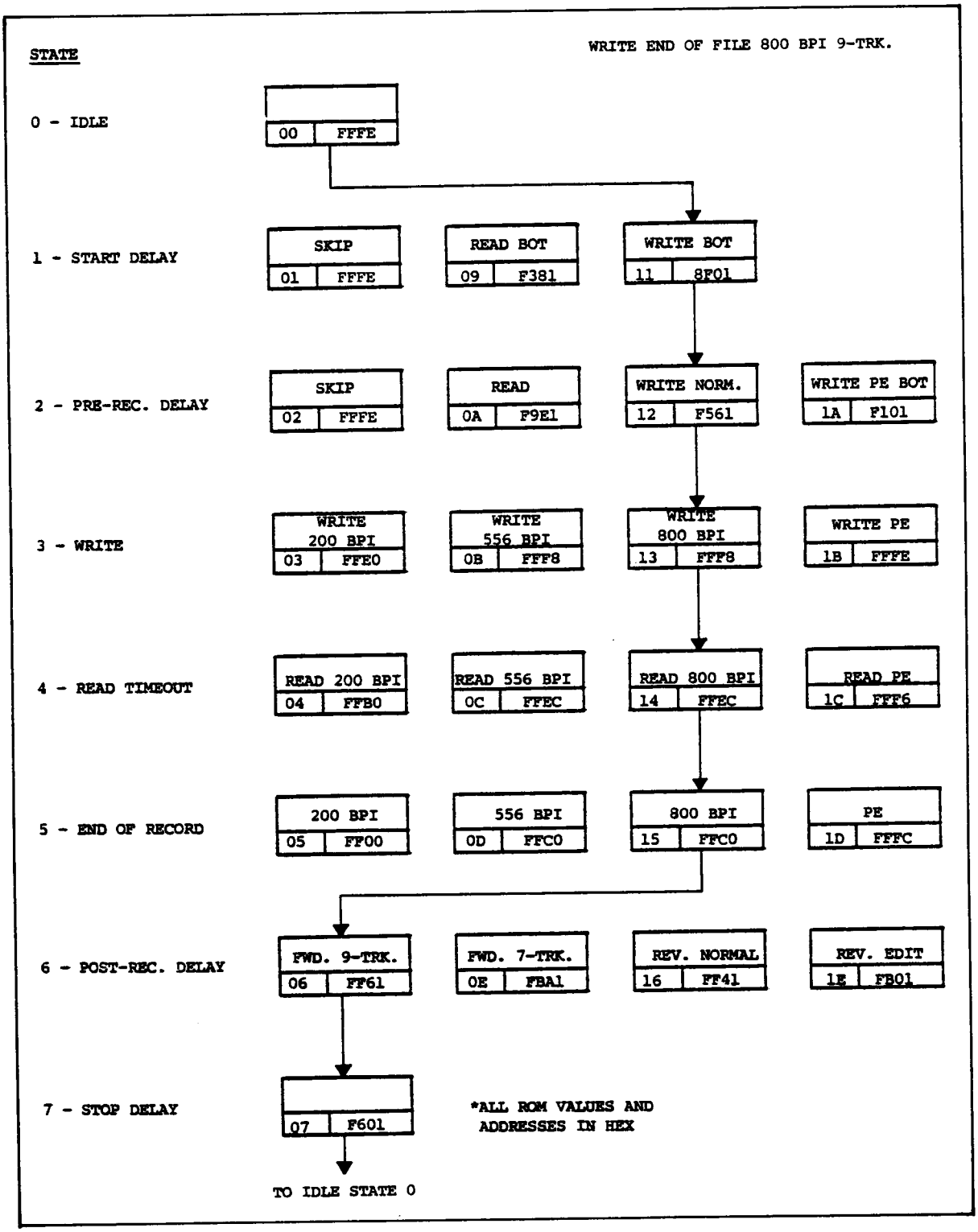
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



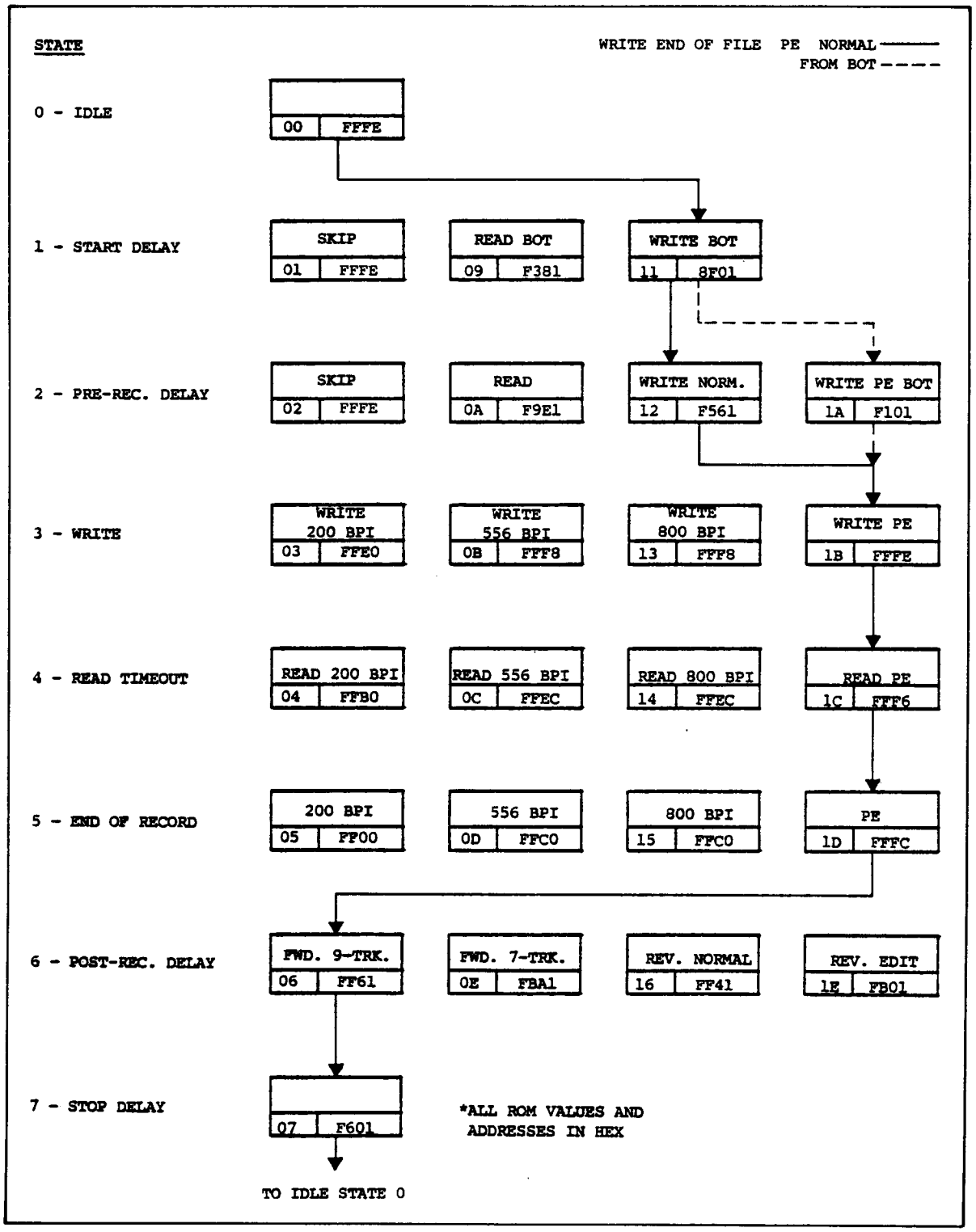
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



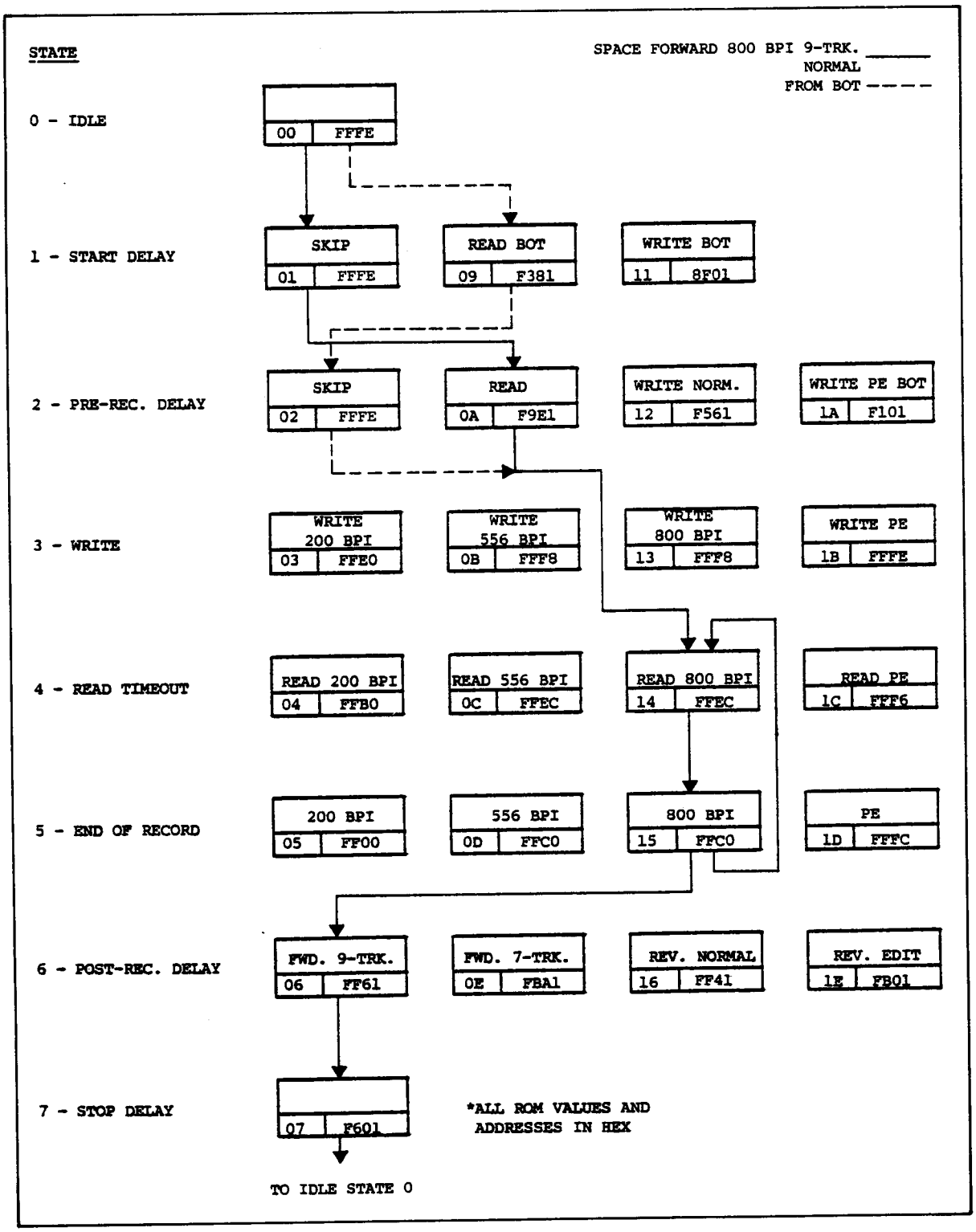
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



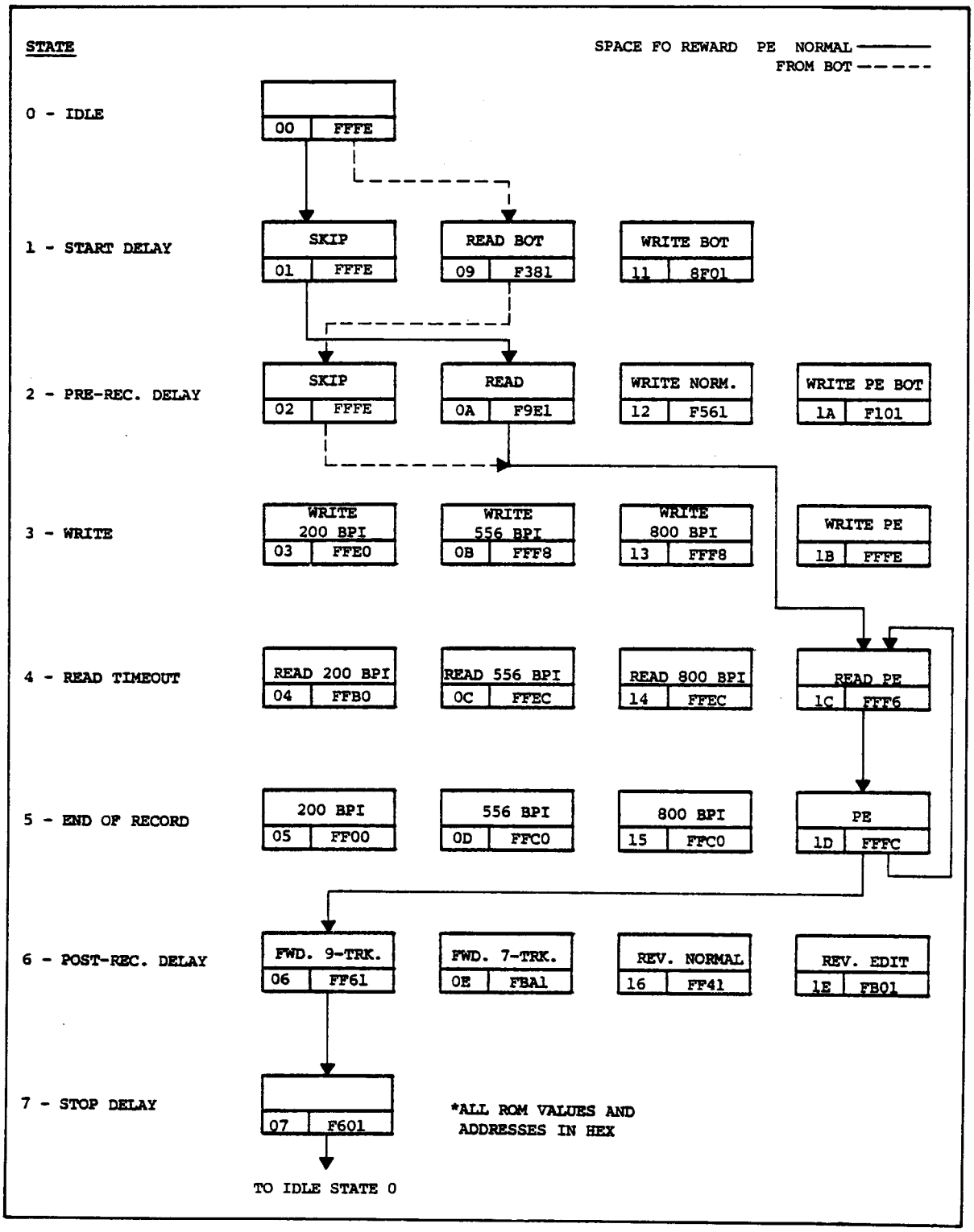
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



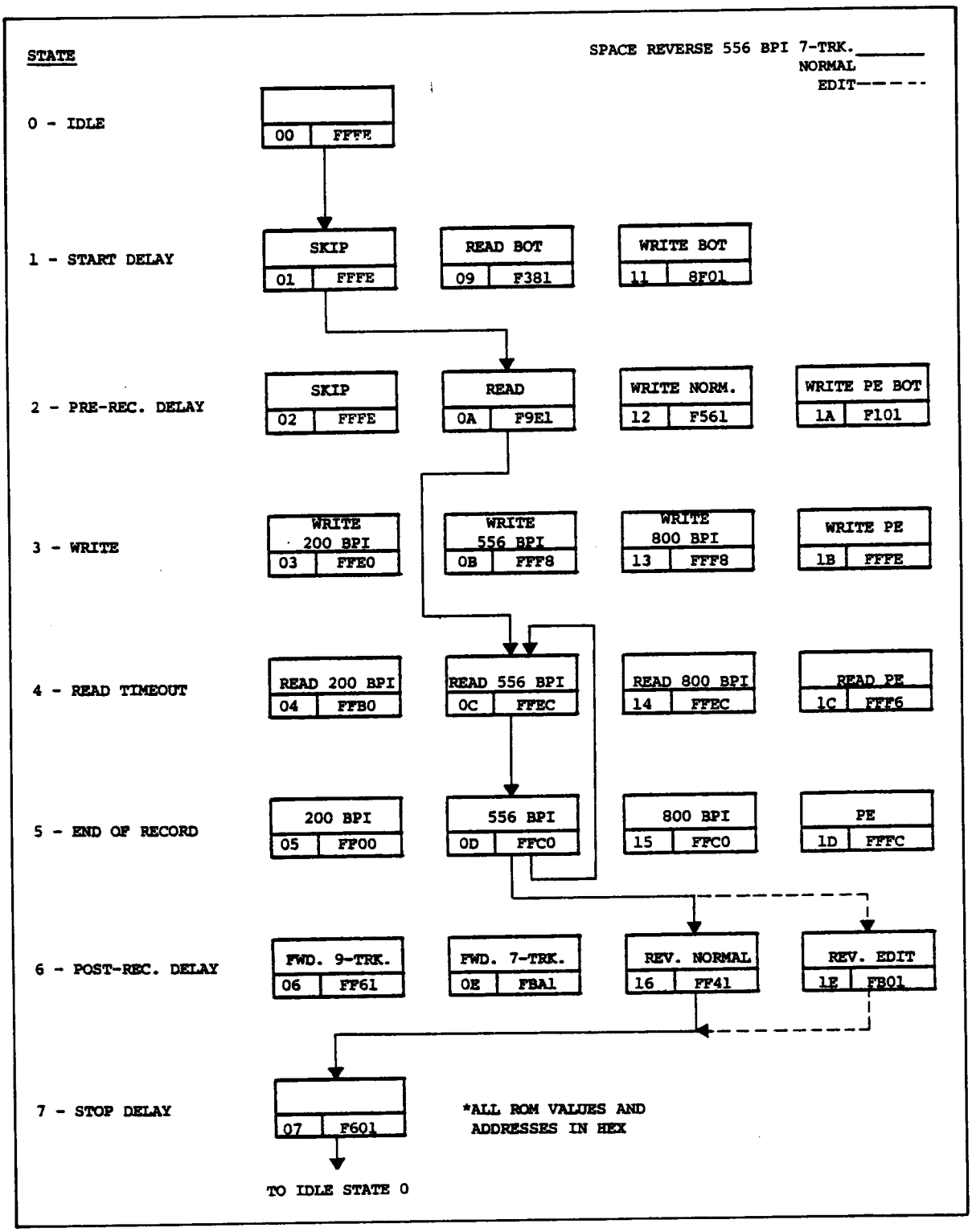
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



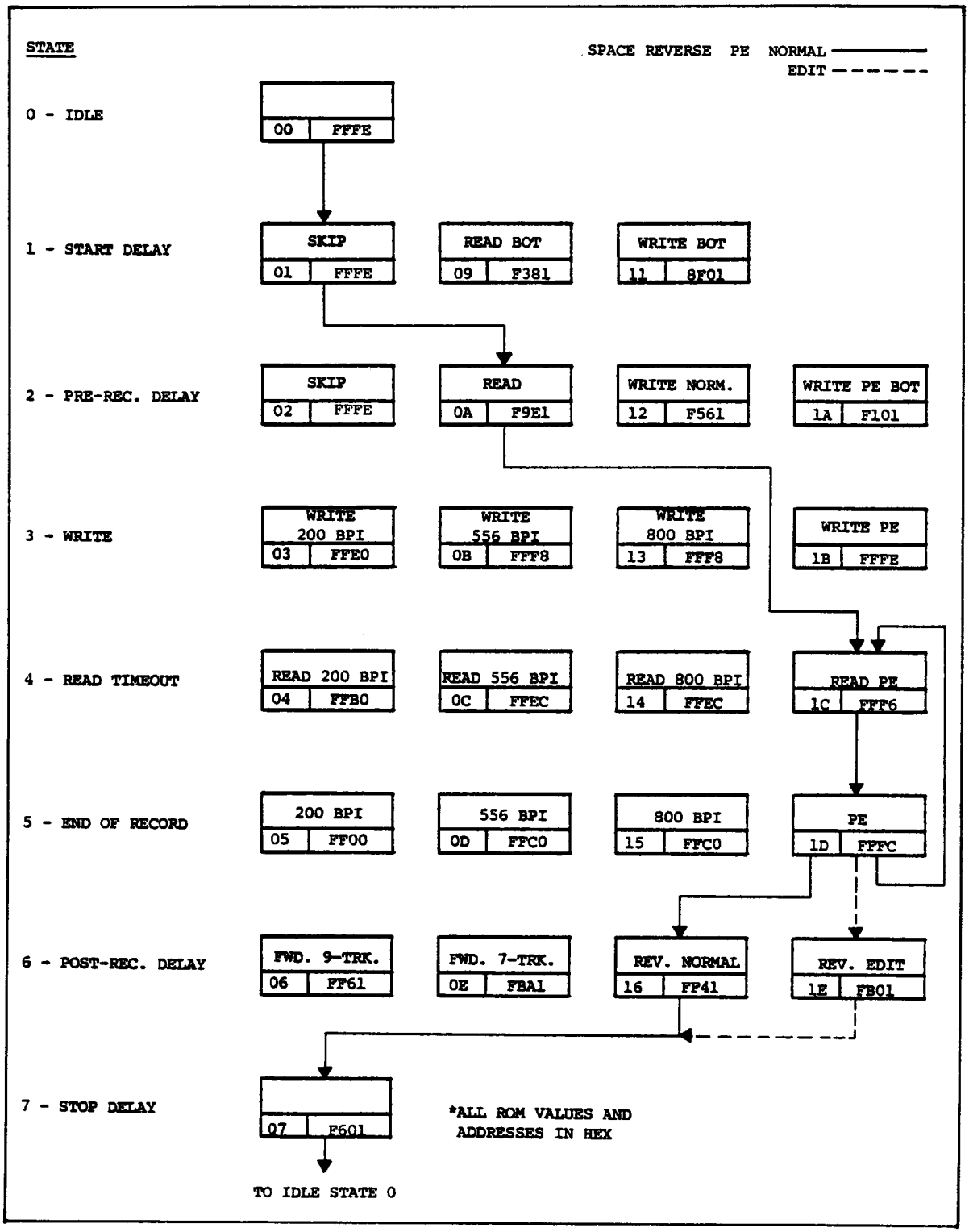
MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



MAIN SEQUENCER AND ROM MAP WITH CONSTANTS



MAIN SEQUENCER AND ROM MAP WITH CONSTANTS

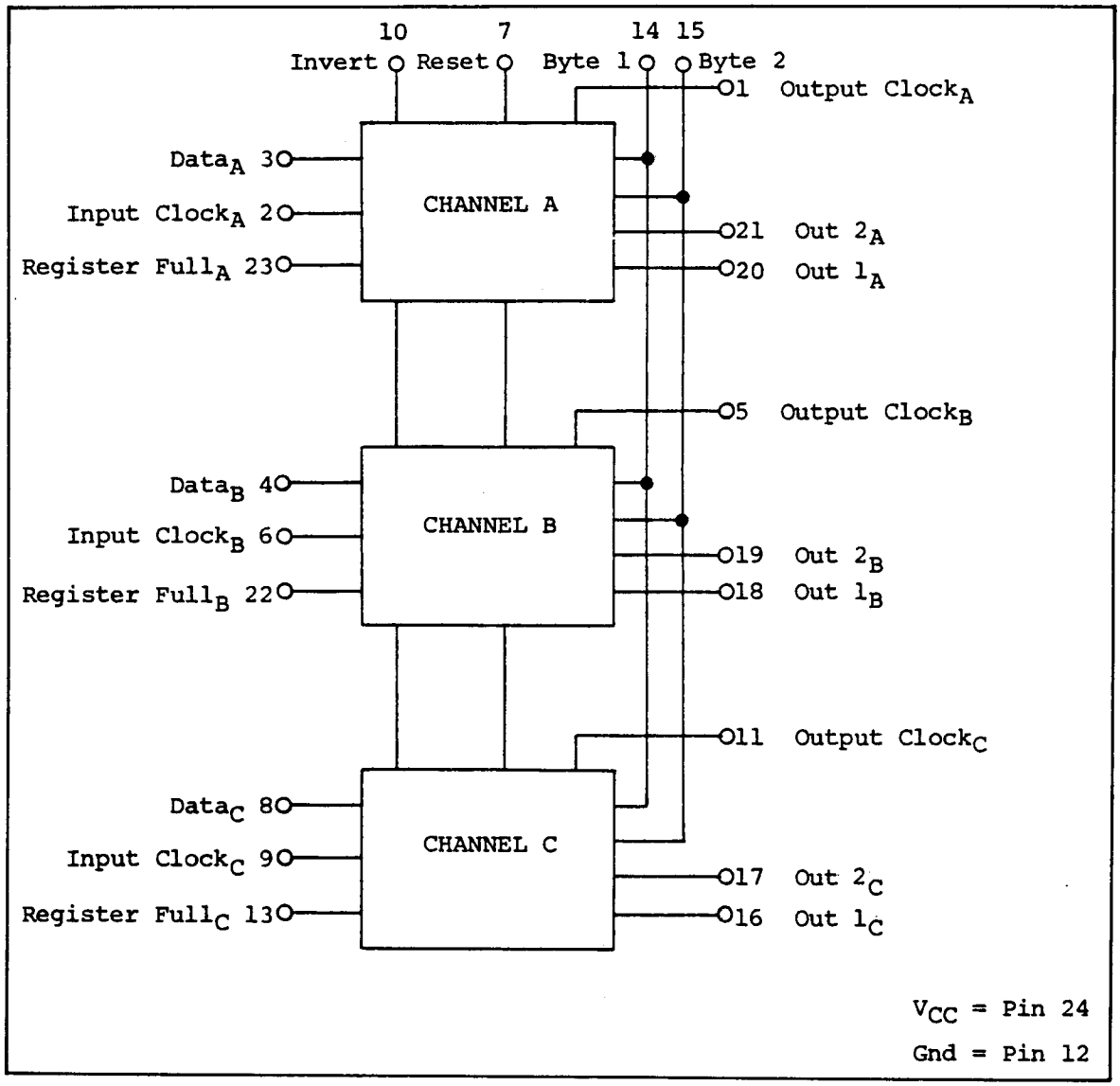
Appendix B

MC8520

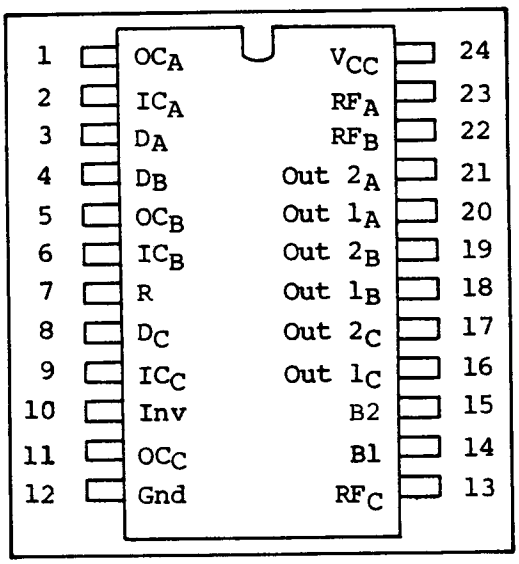
The Deskew/Queue Register

MC8520 - THE DESKEW/QUEUE REGISTER

The MC8520 integrated circuit (Deskew/Queue Register or Deskew Register) is used in magnetic tape transport controllers using Phase Encoded (PE) data format for data handling functions. The primary purpose of the Deskew function is the realignment of data, during the read operation, on a number of different recording channels.



MC8520 INTEGRATED CIRCUIT BLOCK DIAGRAM



MC8520 PIN ASSIGNMENTS

FEATURES AND SPECIFICATIONS

- Independent Input and Output Clocking
- Four Bits per Channel of Skew Data Storage
- Status Indication on Last Two Data Bytes
- +5.0VDC Operation
- Data Rate = 3.0MHz Typical
- Total Power Dissipation = 975mW Typical
- Compatible with TTL Maximum Fan-Out = 1 TTL Load

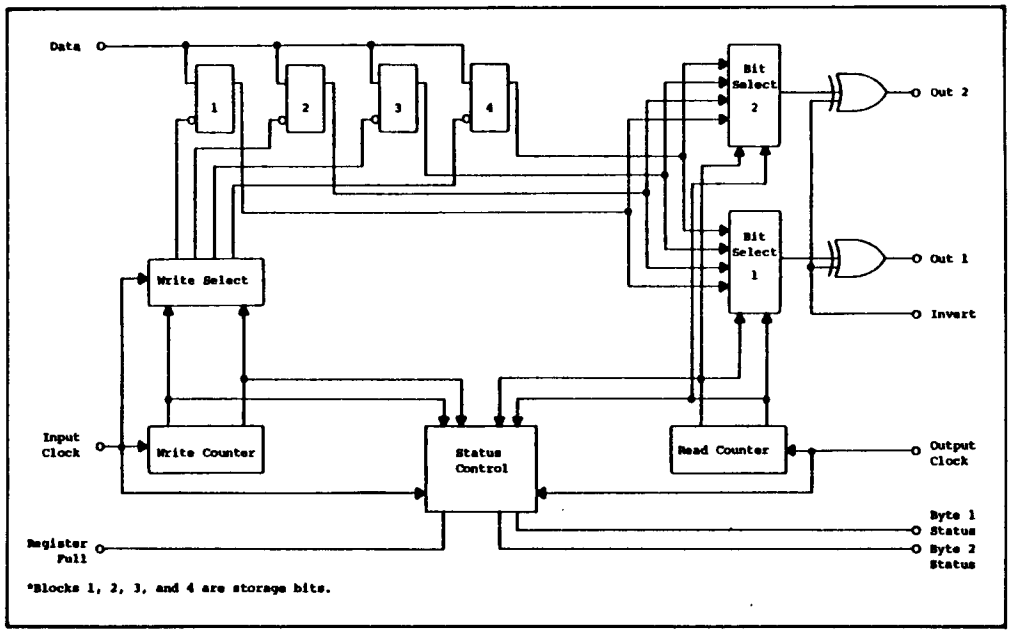
OPERATING CHARACTERISTICS

The primary function of a Deskew Register is the realignment of data occurring on a number of different channels. A recovery (input) system clock accompanies each channel. Each of these clocks occur at the same frequency but may differ somewhat in phase from the other channel clocks. Only when all bits of the input data have arrived should a data byte be read out of the register. A large amount of buffer storage is not required as the output clock is approximately the same frequency as the input clock.

The MC8520 employs a FIFO with dual addressing. Setting time is minimal and clock interaction does not effect storage function. The input and output clockings are non-destructive and independent.

DESKEW REGISTER

The use of the Deskew Register requires a status signal (byte 1, ready or data ready) and a Register Full signal indicating when all storage locations are full.



DESKEW REGISTER FUNCTIONAL BLOCK DIAGRAM

Appendix C

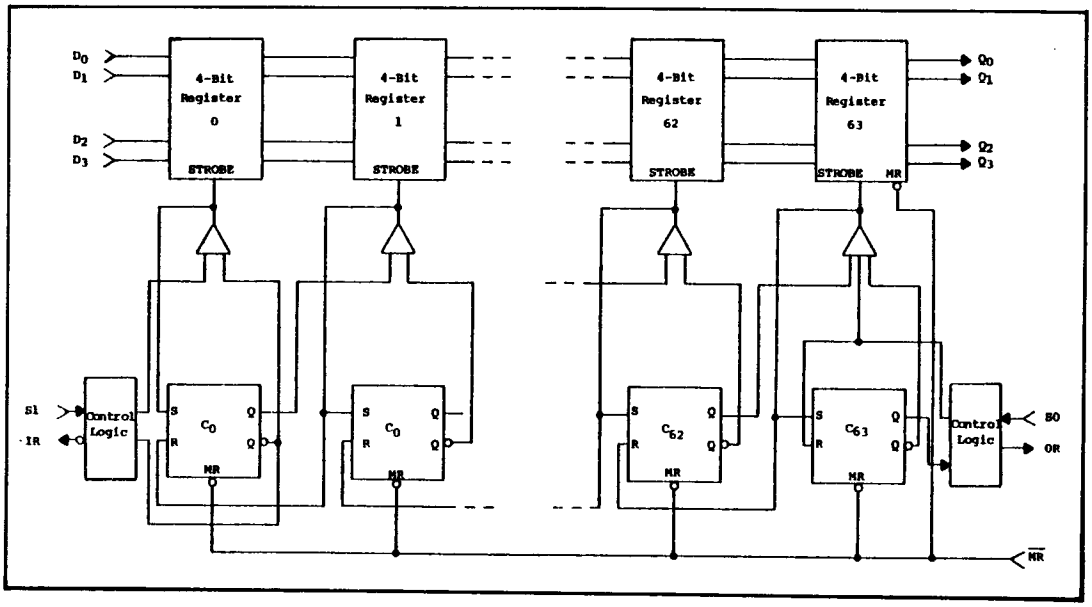
AM2841

A 64 x 4 First-In First-Out Memory

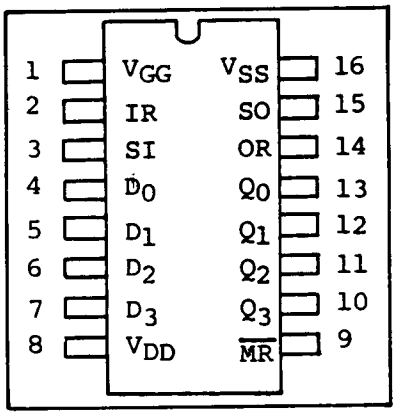
AM2841 - A 64 x 4 FIRST-IN FIRST-OUT MEMORY

The AM2841 integrated circuit is an asynchronous first-in first-out (FIFO) memory stack organized as 64 four-bit words. A four-bit parallel word D_0 - D_3 is accepted by this device under control of the shift-in input. When data is entered into the FIFO, it instantly ripples through the device to the outputs Q_0 - Q_3. Stored words line up at the output end in the order in which they are written, and before any words are read from the memory, a total of up to 64 words may be entered. Upon a read command on the shift out input, the next to the last word stored moves to the output, and all data shifts one place down the stack. The input ready and output ready signals act as memory full and memory empty flags, respectively. They also provide the necessary pulses for interconnecting FIFO's to obtain deeper stacks. Rows of FIFO's may be placed side by side for parallel expansion to wider words.

The Read and Write operations are completely independent; therefore, this device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates.



AM2841 LOGIC BLOCK DIAGRAM



AM2841 PIN ASSIGNMENTS

FEATURES

- Asynchronous Buffer for up to 64 Four-Bit Words
- Easily Expandable to Larger Buffers
- Guaranteed Data Rate of 1MHz

SWITCHING CHARACTERISTICS

For switching characteristics over operating range (unless otherwise noted), refer to table on following page.

TIMING

Until the master reset is strobed or a new data word falls through to the output, the last word read will remain on the outputs. When memory is empty, the OR will remain LOW indicating data at the output is not valid.

When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.

While the memory is empty and a word is written into the input, if SO is HIGH, that word will then fall through the memory to the output. OR will go HIGH for one internal cycle and then will return to LOW. The stored word will remain on the outputs. When

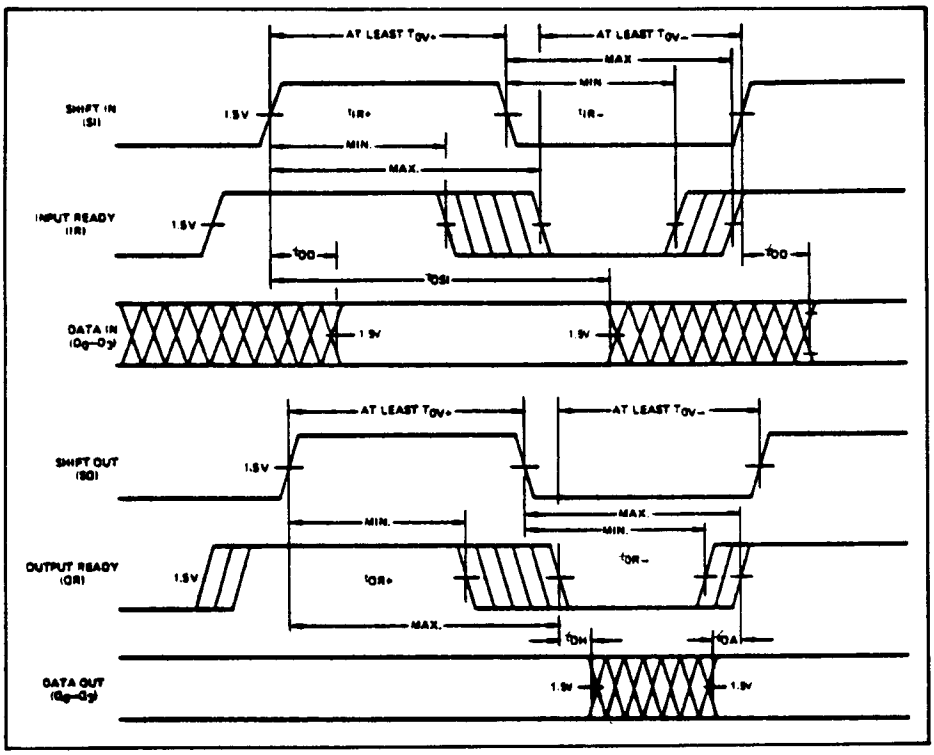
PARAMETERS	DEFINITION	TEST CONDITIONS	AM2841		
			MIN.	TYP.	MAX.
f_{max}	Maximum S1 or S0 Frequency		1.0		
t_{IR+}	Delay, S1 HIGH or IR LOW		80		400
t_{IR-}	Delay, S1 LOW to IR HIGH		100		550
t_{OV+}	Minimum Time S1 and IR both HIGH				80
t_{OV-}	Minimum Time S1 and IR both LOW				80
t_{DSI}	Data Release Time				200
t_{DD}	Data Set-up Time		0		
t_{OR+}	Delay, SO HIGH to OR LOW		70	200	450
t_{OR-}	Delay, SO LOW to OR HIGH		70	200	550
t_{PT}	Ripple through Time	FIFO Empty		8	16
t_{DH}	Delay, OR LOW to Data Out	S0 = LOW	75		
t_{MRW}	Minimum Reset Pulse Width				400
t_{DA}	Delay, Data Out to OR HIGH	S0 = HIGH	0	20	
CI	Input Capacitance (Except $\overline{MR}$)				7
C_{MR}	Input Capacitance $\overline{MR}$				7

NOTE: Switching times over the entire temperature range are such that two devices at approximately the same ambient temperature can drive each other.

SWITCHING CHARACTERISTICS

more words are written into the FIFO, they will line up behind the first word and not appear on the outputs until SO goes LOW.

The control register and outputs are cleared when the master reset is brought to LOW; IR goes HIGH and OR goes LOW. When the master reset goes HIGH, if S1 is HIGH, the data on the inputs will be written into the memory. Also, IR will return to LOW until S1 is brought LOW. If S1 is LOW when the master reset is ended, IR will go HIGH. Data on the inputs will not enter the memory until S1 goes HIGH.



TIMING DIAGRAM

FIFO OPERATION

The FIFO consists internally of 64 four-bit data registers and one 64-bit control register. A "1" in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register, versus an "0", which indicates the corresponding data register does not contain valid data. The control register directs the data's movement through the data registers. Whenever the nth bit of the control register contains a "1" and the (n + 1)th bit contains a "0", then a strobe is generated causing the (n + 1)th data register to read the contents of the nth data register, simultaneously setting the (n + 1)th control register bit and clearing the nth control register bit, so that the control flag moves with the data. In this way, as long as there are empty locations ahead of the data registers, data moves down the data register stack toward the output. When the data reaches a register n with a "1" in the (n + 1)th control register bit, or the end of the register, the fall through operation stops.

By applying a LOW-to-HIGH transition on the shift in input (SI), data is, initially, loaded from the four data inputs D_0 - D_3; simultaneously a "1" is placed in the first control register bit. The first control register bit is returned, buffered, to the input ready (IR) output. The IR pin goes LOW indicating data has been

entered into the first data register, and the input is now unable to accept more data. Assuming at least the second location is empty, when S1 goes LOW again, the fall through process begins. The IR goes HIGH when data in the first register is copied into the second, and the first control register bit is cleared indicating that the inputs are available for another data word. The data falling through the register stacks up at the output end.

At the output, the last control register is buffered and brought out as Output Ready (OR). When OR is HIGH, there is a "1" in the last control register bit; therefore, the four data outputs Q_0 - Q_3 contain valid data. The input signal shift out (S0) is used to shift the data out of the FIFO. The OR goes LOW when a LOW-to-HIGH transition on S0 clears the last register bit, thus indicating that data on the outputs may no longer be valid. When S0 goes LOW, the "0" now present at the last control register bit allows the data in the next-to-the-last register to move into the last register and on to the outputs. The "0" in the register then changes places with each word, in the register, consecutively toward the input.

When all data is being read out of the memory, as the last word is read and S0 goes HIGH, OR will go LOW. When S0 next goes LOW, there is no data to move to the next location, so OR will remain LOW until more data arrives in the output. When the memory is full, data written into the first location will not shift into the second when S1 goes LOW, and IR will remain LOW instead of returning to a HIGH state.

To reset all control register bits, an overriding master reset ($\overline{MR}$) is used. The $\overline{MR}$ will also remove the data from the output.