PM-TC11

Magnetic Tape Controller

Manual

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Section 1

General Information

1.1 INTRODUCTION

This manual provides the information needed to install and operate the PM-TC11 magnetic tape controller manufactured by Plessey Peripheral Systems, Irvine, California.

The material is arranged in four sections as follows:

Section 1 - GENERAL INFORMATION. This section contains a brief general description and the specifications of the PM-TC11.

Section 2 - INSTALLATION AND TESTING. This section describes the requirements and procedures for equipment installation and testing. Switch positions, cabling and diagnostics are included.

Section 3 - PROGRAMMING. This section contains a detailed description of the registers and provides programming information.

Section 4 - THEORY OF OPERATION. This section describes the tape controller logic.

Appendix - This section contains additional information such as specialized integrated circuits and ROM constants.

DRAWINGS. A separate drawing package, MD 701893, contains the parts lists, assembly drawings and schematics necessary for a complete understanding of the PM-TC11.

1.2 GENERAL DESCRIPTION

The PM-TC11 magnetic tape controller provides control and formatting for 9-track phase encoded (PE), as well as 7 and 9-track non-return to zero (NRZI) tape operations. The controller with attached tape drives is designed for the DEC PDP-11 series of computers and functions as a software compatible, direct replacement for DEC's TM11/TU10 tape system.*

*DEC and PDP-11 are registered trademarks of Digital Equipment Corporation.

A simplified block diagram of the PM-TC11 is shown in Figure 1-1.

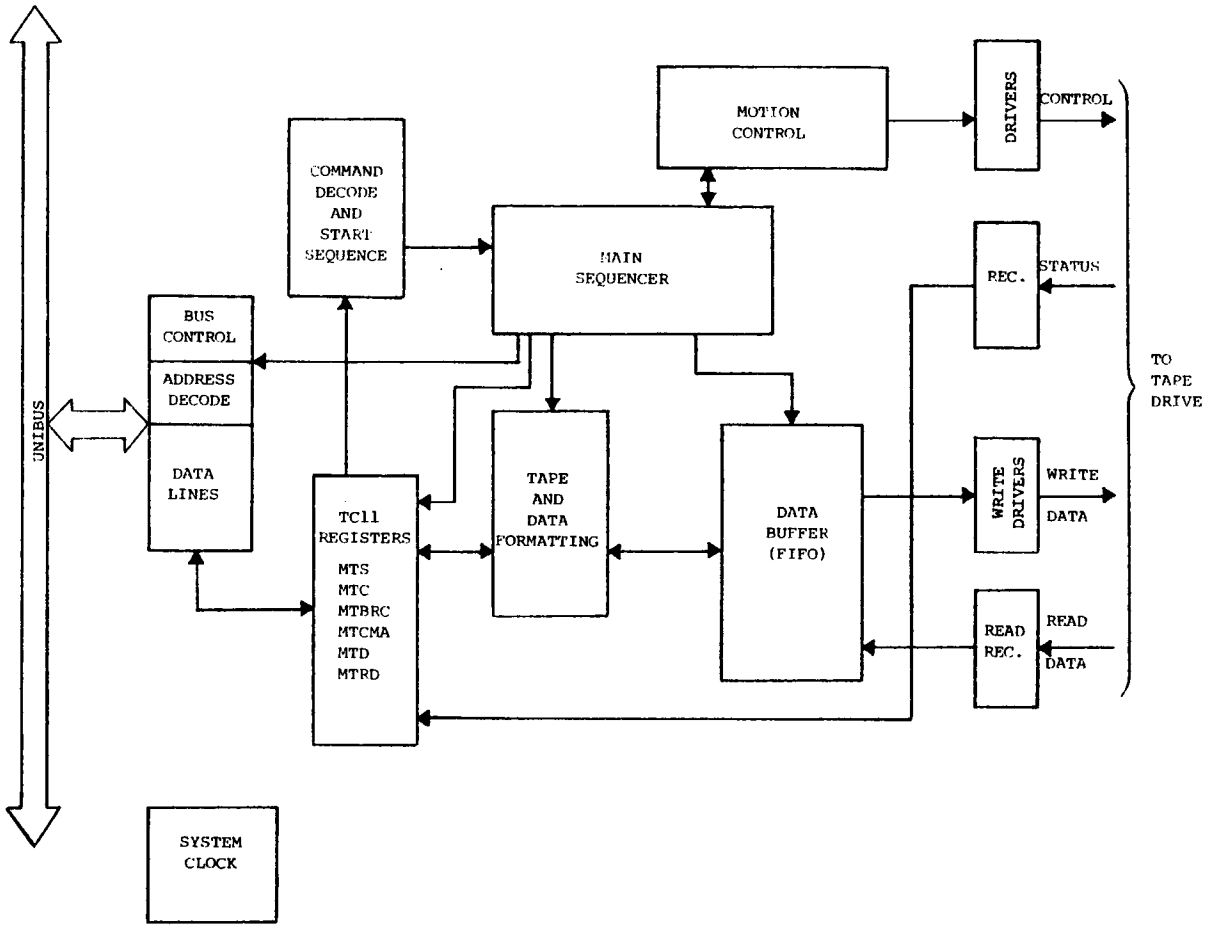


FIGURE 1-1: SIMPLIFIED BLOCK DIAGRAM

1.2.1 Tape Controller (PM-TC11)

The PM-TC11 tape controller consists of a maximum of four cards which occupy one DEC system unit. The controller will read/write DEC or IBM compatible tapes in 9-track PE (1600 bpi), 9-track NRZI (800 bpi) and 7-track NRZI (800/556/200 bpi) formats at industry standard tape drive speeds from 12.5 to 125 ips.† A maximum of four tape drives per controller with any mix of 7 or 9-track NRZI, PE or dual density is allowed. A controller will accommodate a maximum of two drive speeds.

All reading and writing of tape is performed in the forward direction. However, tape positioning is done in both the forward and reverse direction. Tape motion control, inter-record gap control, together with the generation and detection of check characters and file marks, allows operation with industry compatible magnetic tapes.

For 7-track units a program selectable 4 x 4 packing mode allows the dumping of main memory to magnetic tape.

1.2.2 Unibus* Register Usage

Unibus register usage is compatible with DEC TM11/TU10 register definitions. The controller provides for register read/write, interrupt control and NPR data transfers. All data transfers, except for odd bytes at the beginning or end of a record, are done on a word (16-bit) basis. A 32-word buffer internal to the controller compensates for time variations between NPR transfer and tape drive data transfers, and thereby, allows greater flexibility in the assignment of computer priorities.

1.2.3 Additional Features

Additional features are edit mode, IBM mode and non-stop consecutive operations. The edit mode allows user update of selected records on a previously recorded magnetic tape. IBM mode of operation modifies the byte sequence to allow reading or writing of IBM compatible tapes. Non-stop consecutive read or write operations to the same tape unit provide throughput improvements by eliminating the unnecessary stopping of tape between records.

†IBM is a registered trademark of International Business Machines, Inc.
*Unibus is a registered trademark of Digital Equipment Corporation.

1.3 SPECIFICATIONS

1.3.1 Tape Format

- Standards: ANSI
- Number of Tracks: 7 or 9
- Recording Method:

7-track	NRZI
9-track	NRZI (Non-return to zero) or PE (Phase encoded)

- Recording Density:

7-track NRZI	200/556/800 bits/inch (bpi) programmable selectable
9-track NRZI	800 bpi
9-track PE	1600 bpi

- Tape Character Bits/Computer Word:

7-track core dump	4, 4, 4, 4
7-track	6, 6
9-track NRZI	8, 8
9-track PE	8, 8

- Tape Speeds: 12.5, 25, 37.5, 45, 75, 125 inches/second (ips)
- Maximum Number of Tape Speeds per Controller: 2

1.3.2 Unibus Specifications

- Standard Register Address:

Status (MTS)	772520
Command (MTC)	772522
Byte Record Counter (MTBRC)	772524
Current Memory Address (MTCMA)	772526
Data Buffer (MTD)	772530
TU10 Read Lines (MTRD)	772532

Base address may be modified by switch settings.

- Data Transfer Path: Direct Memory Access (DMA) with tape controller as bus master

- DMA Format: Word transfer (16 bits) except for odd byte at beginning or end of record

- Standard Interrupt Vector Address: 224

Vector may be modified by switch setting.

- Standard Priority Level: BR5

Other levels available as a jumper option.

- Unibus Load: One Unibus DC load defined by Digital Equipment Corporation

1.3.3 Physical Specifications

- Number of Cards:

  NRZI: 2 hex, 1 quad
  PE: 3 NRZI cards plus 1 additional PE quad card

- Mounting: Controller includes one system unit backplane capable of accommodating all four controller cards plus Unibus and/or terminator cards. The backplane will mount in standard computer or expansion chassis.

- Number of Cables: 3 cables to first drive. Additional drives connected in daisy-chain fashion from first drive.

- Maximum Drives/Controller: 4

- Tape Drive Interface: Pertec/Kennedy compatible

- Weight (approximate): 4 pounds
- Shipping Weight: 10 pounds

1.3.4 Electrical Specifications (Controller)

- Power Requirements (estimated): Power obtained from DEC CPU or expansion box power supply.

  +5V:5.5A
  -15V:75mA

1.3.5 Environmental Specifications (Controller)

- Operating Temperature: 0°C to +55°C
- Storage Temperature: -10°C to +70°C
- Humidity: 10 to 90% without condensation
- Altitude: The controller will operate at altitudes equal to or greater than the tape drive capability.

Section 2

Installation and Testing

2.1 UNPACKING AND INSPECTION

The PM-TC11 is shipped in a special packing carton designed to keep the components from vibrating and to give the controller maximum protection during shipment. The packing carton should be retained in case the PM-TC11 requires reshipment.

Remove any packing materials, unpack the controller and check all parts to ensure complete delivery. Table 2-1 identifies the PM-TC assemblies.

701893 PM-TS11 Magnetic Tape System	
• 701894-XXX	PM-TC11 Magnetic Tape Controller
701700	Board #1 - Format Control
703290	Board #2 - Unibus Control
701720	Board #3 - NRZI Control
701690	Board #4 - PE Control
701895	System Unit
701620-100	Assembly Backpanel Board
700492-100	Frame Assembly
701895	Wire List
701528-XXX	Adapter Assembly PE Tape Speed
700144-101	Unibus Cable
701894	Installation Manual
800068-100	Basic Logic Diagnostic Program
800069-100	Data Reliability Diagnostic Program
800070-100	Function Select Diagnostic Program
• 701376-100	DC Power Cable
• 701377-100	DC Power Cable
• 701378-100	DC Power Cable
• 701383-100	DC Power Cable
• 701892-XXX	Drive Signal Cable Kit
701891-100	Control Cable
701855	Control Cable Adapter
703015	Control Cable Adapter, Right Angle
701891-102	Read Cable
701865	Read Cable Adapter
703155	Read Cable Adapter, Right Angle
701891-104	Write Cable
701875	Write Cable Adapter
703145	Write Cable Adapter, Right Angle

7025-01-006-1609
7025-01-000-1611
7025-01-008-1610
7025-01-000-1608

TABLE 2-1: PM-TS11 TAPE SUBSYSTEM DRAWING ASSEMBLIES

2.1.1 Controller

After removal of the controller from the shipping container, visually inspect the boards and cable assemblies for any physical damage. Inspect the controller backpanel for any bent or damaged pins.

2.1.2 Drive

After removal of the tape drive from the shipping container, use Kennedy Company Operation and Maintenance Manual packaged with each drive for visual inspection and installation of each drive.

2.2 INSTALLATION

2.2.1 Controller

A. Install the PM-TC11 controller backplane (P/N 701895-100) into the CPU mainframe or expansion box. Connect the DC power cable to the quick disconnect spade lugs as shown in Figure 2-1. Connect other end of DC power cable to the nearest power connector in the chassis.

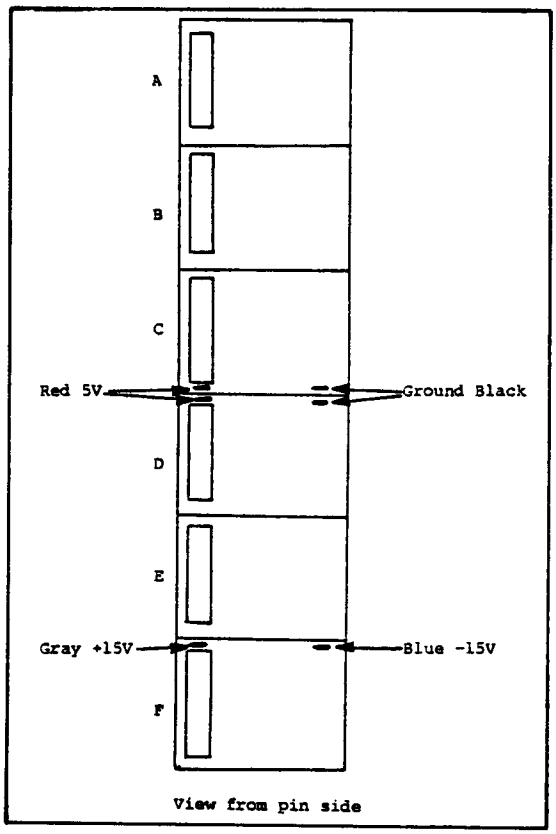


FIGURE 2-1: DC POWER CONNECTION

B. Install the Unibus IN cable into slots A1 and B1 of the backplane.

C. Install the Unibus OUT cable into slots A4 and B4 of the backplane. If the PM-TC11 controller is the last device on the bus, install the appropriate bus terminator into slots A4 and B4.

NOTE: When installing the controller in DEC PDP-11/34 systems, use a minimum of two feet of Unibus cables at the input and output of the controller.

D. On Board #1 (FORMAT CONTROL P/N 701700), set the primary and secondary drive speeds as shown in Table 2-2.

SWITCH 1 (SW1): PRIMARY DRIVE SPEED
SWITCH 2 (SW2): SECONDARY DRIVE SPEED

SWITCH POSITION	DRIVE SPEED					
	12.5	25	37.5	45	75	125
1	X		X			
2					X	
3		X	X		X	
4	X	X	X	X	X	X
5	X		X	X		
6		X				
7	X					
8						

NOTE: Ensure that primary and secondary drive speed definitions correspond with switch settings on Control Adapter Boards (P/N 701855-100 or 703015-100) on each tape drive. See Section 2.3.2, Step 4.

TABLE 2-2: TAPE SPEED SELECTION SWITCH (X = CLOSED; DEPRESSED ON CLOSED SIDE OF SWITCH)

E. On Board #2 (P/N 703290, Unibus Control), register address and interrupt vector should be selected on switches 1 and 2.

Register Address: A range of register addresses can be selected from word location 760000 to location 777760. Standard address is 772520. An open switch corresponds to a logical one, and a closed switch corresponds to a logical zero.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	9	8	7	6	5	4	3	2	1	X	X	X	X

Example Address 772520
(Switch 2 position)

Position 1 - Open
Position 2 - Closed
Position 3 - Open
Position 4 - Closed
Position 5 - Open
Position 6 - Closed
Position 7 - Open
Position 8 - Closed
Position 9 - Open

Vector Address: The standard vector address is location 000224. An alternate interrupt vector address can be selected by switch 1 from a range of locations from 000004 to location 000374. An open switch corresponds to logical one, and a closed switch corresponds to a logical zero.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	8	7	6	5	4	3	X	X

Example Location 000224
(Switch 1 position)

Position 3 - Open
Position 4 - Closed
Position 5 - Open
Position 6 - Closed
Position 7 - Closed
Position 8 - Open

F. If controller being installed is dual density, insure that the Component Adapter Assembly (P/N 701528-XXX) corresponds to the PE (1600 bpi) tape drive speed. Component Adapter Assembly is mounted in location TB1 on Board #4 (PE CONTROL P/N 701690). Table 2-3 shows adapter drive speed selections.

VERSION NUMBER	TAPE DRIVE SPEED (IPS)
-100	12.5
-101	25
-102	37.5
-103	45
-104	75
-105	125

TABLE 2-3: PE COMPONENT ADAPTER SELECTION

G. Install boards into backplane as shown in Figure 2-2.

	A	B	C	D	E	F
1	UNIBUS IN		BOARD #1 FORMAT CONTROL (P/N 701700)			
2	BOARD #2 UNIBUS CONTROL (P/N 703290)					
3	BOARD #3 NRZI CONTROL (P/N 701720)					
4	UNIBUS OUT/TERMINATOR		BOARD #4 PE CONTROL (P/N 701690)			

FIGURE 2-2: MODULE SLOT ASSIGNMENT

If tape controller is NRZI only (200, 556 or 800 bpi), install boards 1, 2 and 3. If controller is dual density NRZI and PE (1600 bpi), install boards 1, 2, 3 and 4.

2.2.2 Tape Drive

A. Remove the Data Terminator Module (Kennedy P/N 890-3860-XXX) and the Control Terminator Module (Kennedy P/N 890-3841-XXX) from each tape transport.

B. On the Multiple Tape Adapter (MTA) Board (Kennedy, type 4147), verify jumper positions according to Table 2-4.

JUMPER	POSITION
St1	OUT
St2	OUT
St3	OUT
St4	OUT
St5	IN
St6	OUT
St7	IN
St8	IN
St9	IN
St10	IN

TABLE 2-4: MULTIPLE TAPE ADAPTER JUMPER POSITIONS

C. On Kennedy Models 9100 and 9300 use the following cable adapters:

		All Others:	
703015-100	Control	701855-100	Control
703155-100	Read	701865-100	Read
703145-100	Write	701875-100	Write

D. On each Control Cable Adapter (P/N 701855 or 703015) Board perform the following:

1. Set Switch 1 (SW1) to reflect correct system configuration. See Table 2-5 for switch settings.

SW1	MEANING	
	ON = CLOSED	OFF = OPEN
1	Kennedy	Cipher, Pertec
2	7 Track - 800/556 BPI 9 Track - Dual Density	7 Track - 556/200 BPI 9 Track - Single Density
3	Secondary Speed	Primary Speed
4	ON - All Others	Pertec - 9 Track NRZI Only
5	Pertec - 9 Track NRZI Only	OFF - All Others
6	9 Track	7 Track
7	---	OFF
8	Cipher, Pertec	Kennedy

TABLE 2-5: CONTROL CABLE ADAPTER SWITCH SETTING

2. If system configuration specifies daisy chaining drives, remove terminator RU1 on all Control Cable Adapter Boards except on the last drive.

3. Install Control Cable Adapter Board (P/N 701855 or 703015) on J1 of Multi-Tape Adapter Board at the rear of each tape drive. Insure P101 and J1 pins match.

E. Install the Read Cable Adapter Board (P/N 701865 or 703155) on J3 of Multi-Tape Adapter Board at the rear of each tape drive. Insure P103 and J3 pins match.

F. Write Cable Adapter Board (P/N 701875 or 703145). If system configuration specifies daisy chaining drives, remove terminator RU1 on all Write Cable Adapter Boards except on the last drive.

Install Write Cable Adapter Board on J2 of the Multi-Tape Adapter Board at the rear of each tape drive. Insure P102 and J2 pins match.

2.2.3 Controller/Drive Cable Installation

NOTE: All signal cables should connect so that Pin 1 on the cable connector mates with Pin 1 on the PWB. See Figure 2-2.

A. Single Drive System (See Figure 2-2.)

1. Control Cable (P/N 701891-100). Install Control Cable such that cable connector P1-A connects with J1-A on board #2 (P/N 701710) in slot #2 and cable connector P1-B connects to J1-B on the Control Cable Adapter Board (P/N 701855 or 703015) at the rear of the tape transport.

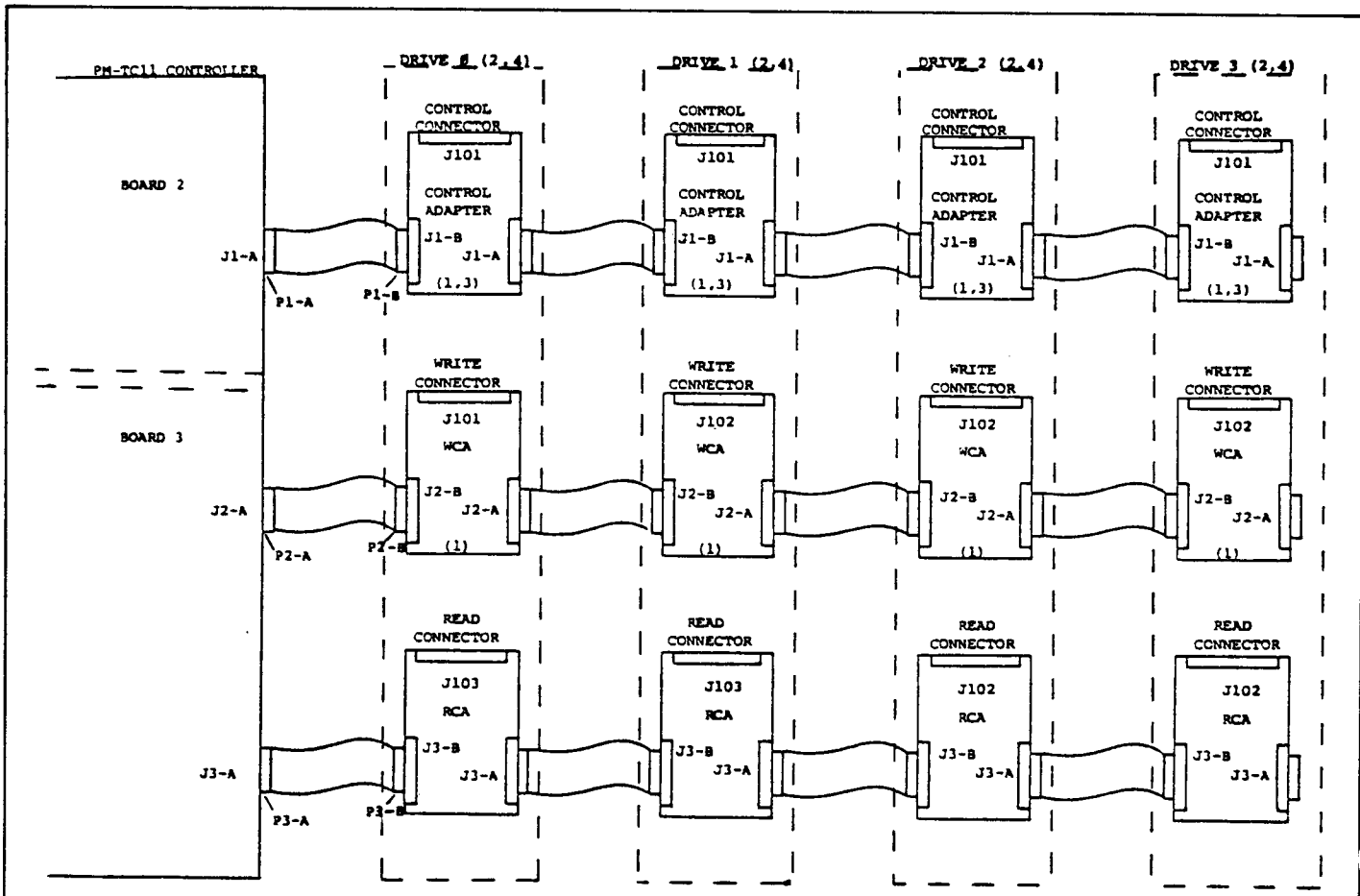
2. Read Cable (P/N 701891-102). Install Read Cable such that cable connector P3-A connects to J3-A on Board #3 (P/N 701720) in slot #3 and cable connector P3-B connects to J3-B on the Read Cable Adapter Board (P/N 701865 or 703155) at the rear of the tape transport.

3. Write Cable (P/N 701891-104). Install Write Cable such that cable connector P2-A connects to J2-A on Board #3 (P/N 701720) in slot #3 and cable connector P3-B connects to J3-B on the Write Cable Adapter Board (P/N 701875 or 703145) at the rear of the tape transport.

B. Connect remaining drives as follows:

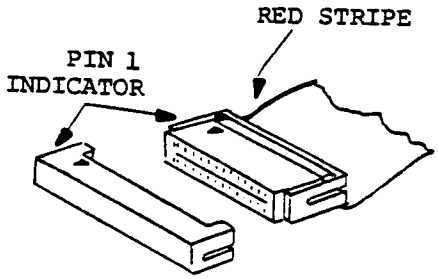
1. Control Cable (P/N 701891-100). Install control cables such that cable connector P1-A connects to J1-A on the Control Cable Adapter Board on the preceding drive in the daisy chain and cable connector P1-B connects to J1-B on the Control Cable Adapter Board on the following drive in the daisy chain.

2. Read Cable (P/N 701891-102). Install read cables such that cable connector P3-A connects to J3-A on the Read Cable Adapter Board on the preceding drive in the daisy chain and cable connector in the daisy chain and cable connector P3-B connects to J3-B on the Read Cable Adapter Board on the following drive in the daisy chain.



() NOTES:

1. Terminator to be used in Adapter Board for last drive only.
2. Drives may be configured in any numerical sequence desired.
3. For drives above Unit 3 (SEL 3) a special jumper configuration may be required. Consult Control Adapter Schematic.
4. Remove all internal terminators in drive.



CABLE CONNECTORS

FIGURE 2-3: MAGNETIC TAPE DRIVES INTERCONNECTION DIAGRAM

3. Write Cable (P/N 701891-104). Install write cable such that cable connector P2-A connects to J2-A on the Write Cable Adapter Board on the preceding drive in the daisy chain and cable connector P2-B connects to J2-B on the Write Cable Adapter Board on the following drive in the daisy chain.

2.3 TESTING

2.3.1 Preliminary Tests

A. Refering to Kennedy Company Operation and Maintenance Manual, power up and mount a scratch tape on all tape drives.

B. Power up controller and verify following voltages at PM-TC11 backpanel.

+5VDC $\pm$ 200mV
-15VDC $\pm$ 500mV

2.3.2 Diagnostic Tests

A. PMTDA Plessey Basic Logic Test (P/N 800068). Run manual intervention on each drive for a minimum of 1 pass. Run automatic test (all tests, excluding manual intervention) on each drive for a minimum of 5 passes. All passes should be error free.*

B. PMTDB Plessey Reliability Diagnostic (P/N 800069). Run test on all drives for a minimum of 3 passes. All passes should be error free.*

*If tape system is a Dual Density NRZI/PE (800/1600 bpi) system, all tests should be completed in both modes.

NOTE: Marginal magnetic tapes may result in some recoverable errors; however, unrecoverable read errors are not acceptable. If errors are experienced, a thorough check of tapes and heads should be made before attempting further troubleshooting. Replace any tapes which show signs of wear or being creased. If head or tape path appears dirty, they should be cleaned.

After correcting for a bad or questionable tape or cleaning the heads, a second try should be made with all tests.

Section 3

Programming

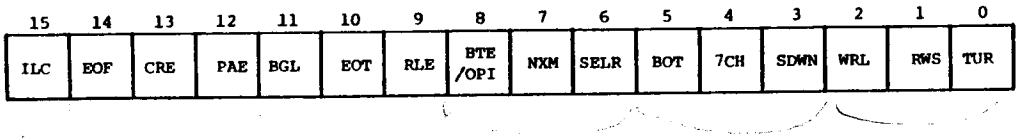
3.1 FUNCTIONAL DESCRIPTION

Registers and their mnemonic codes and standard bus address are listed:

• MTS	Status Register	772520
• MTC	Command Register	772522
• MTBRC	Byte Record Counter	772524
• MTCMA	Current Memory Address Register	772526
• MTD	Data Buffer Register	772530
• MTRD	Read Lines	772532

Register functions and bit assignments are described below.

3.1.1 Status Register (MTS) 772520



BIT	CODE	FUNCTION
15	ILC	(Illegal Command). This bit indicates an illegal command. It is set by the following illegal conditions:

- Any DATO or DATOB transfer to the command register during tape operation. CU RDY in the MTC register indicates a tape operation in progress.
- Any write, write-end-of-file, or write-with-extended-inter-record gap (Functions 2, 3, and 6 in the MTC) operation to a file-protected tape unit. WRL in the MTS indicates a file-protected tape unit.
- Any command to a tape unit that is not on-line. SELR in the MTS indicates a tape unit which is on-line.
- Any time a tape unit goes off-line during any operation except off-line.

BIT	CODE	FUNCTION

The ILC in MTS and ERR in MTC are set simultaneously. This is a read-only bit which is cleared by INIT, PWR CLR or the initiation of a tape operation.

14 EOF (End of File). This bit indicates that the tape has reached the end of the file. The EOF bit is set on the following operations.

- A NRZI read or space-forward operation and the EOF character is read.
- A NRZI space-reverse operation and the LRC character following the EOF character is read.
- A PE read, space-forward or space-reverse operation and the PE file mark is detected.
- During a write EOF operation.

The ERR in the MTC is set when the LRC character following an EOF character (NRZI) or the end of record (PE) is detected. This is a read-only bit which is cleared by INIT, PWR CLR or the initiation of a tape operation. The EOF character is read into the memory during a NRZI read operation.

13 CRE (Cyclic Redundancy Error). This bit indicates a cyclic redundancy error has been detected during a NRZI read operation. This check compares the CRC character written on a 9-track NRZI tape during a write or write-with-extended-IRG operation with the CRC character generated in the controller during a read operation. If the two CRC characters are not the same the CRE bit is set. The ERR bit in the MTC is set when the LRC character is detected.

This is a read-only bit which is cleared by INIT, PWR CLR or the initiation of a tape operation.

12 PAE (Parity Error). In NRZI operation this bit indicates the detection of:

- Vertical parity error on any character other than the CRCC or LRCC character. Odd or even parity is defined by the even parity bit (PEVN in the MTC). Detection of a vertical parity error does not affect the transfer of data.

BIT	CODE	FUNCTION

- Longitudinal parity error. This error is defined as an odd number of ones in any channel in the record.

(Parity Error). In PE operation, this bit indicates the detection of:

- Vertical parity error, other than the preamble and postamble all ones or all zeros characters. This check is disabled for single track errors on read operation. Vertical parity errors do not affect the transfer of data.
- Multiple dead track errors except in the preamble and postamble areas of a record. Multiple dead track errors do not affect the transfer of data.
- Postamble format error. A check is made for 33 consecutive all zero characters following the postamble all ones character. An error condition will be indicated if a character other than all zeros character is detected, or if all tracks go dead prior to detecting the 33 consecutive all zero characters.

The PAE bit is set when the parity error is detected, and the ERR bit in the MTC is set at the end of the record. This is a read-only bit which is cleared by INIT, PWR CLR or the initiation of a tape operation.

11 BGL (Bus Grant Late). This error occurs if Unibus NPR data transfers do not occur in sufficient time to insure valid data transfer through the controller data buffer (FIFO). During write or write-with-extended-IRG, this error will occur if a write strobe is issued to the drive when the data buffer is empty. During read this error occurs when a data character is read from the tape and the data buffer is full. A check is also performed to insure all data is transferred via NPR requests prior to completing a read operation.

The BGL in the MTS and ERR in the MTC are set simultaneously. This is a read-only bit which is cleared by INIT, PWR CLR or the initiation of a tape operation.

BIT	CODE	FUNCTION
10	EOT	(End of Tape). The EOT bit is set as soon as the EOT marker is detected when the tape is moving in the forward direction. It is cleared by the trailing edge of the EOT marker when the tape is moving in the reverse direction. The EOT is an error condition when the tape is moving in the forward direction and ERR in the MTC is set when the end of the record is detected. This is a read-only bit.
9	RLE	(Record Length Error). This bit is tested only during read operations and occurs when the byte counter attempts to increment beyond zero. When a RLE occurs, data transfer into memory and the incrementing of the MTCMA and MTBRC registers stop. The controller continues to read the entire record and sets ERR in the MTC when the end of record is detected. The CU RDY in the MTC remains cleared until the end of record is detected, at which time CU RDY is set. Read-Only
8	BTE/OPI	(Bad Tape/Operation Incomplete Error). A bad tape error occurs when a tape character is detected during the gap shutdown or settle down period of a data transfer operation. Operation Incomplete Error occurs if valid data is not detected on tape for a period of 7 seconds after an operation has been initiated. ERR in the MTC is set simultaneously with BTE/OPI. See bit 13 of the MTRD register for diagnostic simulation of this error bit. This is a read-only bit which is cleared by INIT, PWR CLR or the initiation of a tape operation.
7	NXM	(Non-Existent Memory). This error occurs when the controller is bus master during NPR transfer and does not receive a SSYN response within 10μs after asserting MSYN. NXM in MTS and ERR in MTC are set simultaneously. This is a read-only bit which is cleared by INIT, PWR CLR or the initiation of a tape operation.

BIT	CODE	FUNCTION
6	SELR	(Select Remote). This bit is set when the tape unit has been properly selected. The SELR bit is zero if the tape unit addressed does not exist, if the selected tape unit is off-line, or if the tape unit power is off. This is a read-only bit.
5	BOT	(Beginning of Tape). This bit is set when the BOT marker is detected and cleared whenever the BOT marker is not being detected. The BOT bit does not set the ERR in MTC. This is a read-only bit.
4	7CH	(7 Channel). This bit is set to indicate a 7 channel tape unit and is cleared to indicate a 9 channel unit. This is a read-only bit.
3	SDWN	(Settle Down). This bit is set whenever the tape unit has completed an operation (other than rewind) and the tape is slowing down. When the tape unit stops, SDWN is cleared and tape unit ready (TUR) is set. The tape controller will accept and execute any new command during the SDWN period except if the new command is directed to the same tape unit which issued SDWN and the direction implied in the new command is opposite to the present direction. This is a read-only bit.
2	WRL	(Write Lock). This bit is controlled by the presence or absence of a write protect ring on the selected tape unit. Absence of the write ring sets WRL and prevents the controller from writing on the tape. Presence of the write ring clears WRL and enables the writing of information on tape. This is a read-only bit.
1	RWS	(Rewind Status). This bit is set at the start of a rewind operation and is cleared as soon as the BOT marker is detected while the tape is moving in the forward direction. This is a read-only bit.
0	TUR	(Tape Unit Ready). This bit is set when the tape unit is selected, the tape is loaded and stopped, and the SELR bit is set. This indicates the tape unit is ready to receive a new command. The bit is cleared when the selected tape is being used. This is a read-only bit.

3.1.2 Command Register (MTC) 772522

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	DEN 8	DEN 5	PWR CLR	PEVN	SEL 2	SEL 1	SEL 0	CU RDY	INT ENB	XADR 17	XADR 16	FCTN 2	FCTN 1	FCTN 0	GO

BIT	CODE	FUNCTION
15	ERR	(Error). This bit indicates an error condition and is a function of bits 7-15 in the status register. In PE mode this bit will be set when a SKEW error occurs. SKEW error does not set any other status bit. It is cleared by INIT, PWR CLR or by the next GO command. This is a read-only bit.
14-13	DEN 8 DEN 5	(Density). These bits select the bit packing density of the tape as illustrated below.

(X indicates "Don't Care" condition.)

BIT 14 (DEN 8)	BIT 13 (DEN 5)	DENSITY (BPI)	NO. OF TRACKS
0	0	200 NRZI	7
0	1	556 NRZI	7
1	0	800 NRZI	7
1	1	800 NRZI CORE DUMP	7
1	X	800 NRZI	9
0	X	1600 PE	9

The 7-track core dump mode can also be selected by CPE/CORE DUMP in the MTRD register. These are read/write bits which are cleared by INIT, PWR CLR or by loading zeros.

12	PWR CRL	(Power Clear). When a 1 is loaded into this bit position, it clears the controller logic and all tape units without clearing any other device in the system. The PWR CRL bit is always read back by the processor as 0.
11	PEVN	(Parity Even). This bit is set if even vertical parity is to be used for a NRZI read or write operation. The bit is cleared if odd vertical parity is to be used. PE read or write operations utilize odd vertical parity only.

BIT	CODE	FUNCTION
		Vertical parity is checked for all tape motion operations except space forward, space reverse, and rewind. This is a read/write bit which is cleared by INIT, PWR CLR or by loading a 0.
10-8	SEL	(Unit Select). These three bits represent the octal code of the tape unit being selected. All operations defined in the MTC and all status conditions defined in the MTS pertain to the selected tape unit. This is a read/write bit which is cleared by INIT, PWR CLR or by loading zeros.
7	CU RDY	(Control Unit Ready). This bit, when set, indicates the controller is ready to receive a new command. It is cleared at the start of a tape operation and is set at the completion of a tape operation, by INIT, PWR CLR, or when an error condition exists. This is a read-only bit.
6	INT ENB	(Interrupt Enable). When set this bit allows an interrupt to occur whenever CU RDY changes from 0 to 1 or whenever a tape unit that was set into rewind has arrived at BOT. In addition, an interrupt occurs on an instruction that sets INT ENB and does not set the GO bit. This is a read/write bit which is cleared by INIT, PWR CLR or by loading a zero.
5-4	XADR	(Extended Address Bits). These bits represent bus address bits A17 and A16 and are used with the MTCMA register to specify an 18-bit address. These bits function with the MTCMA register and are incremented by a carry out from MTCMA. These are read/write bits which are cleared by INIT, PWR CLR or by loading a zero.
3-1	FCTN	(Function Bits). These bits specify a command to be performed by the selected tape unit. These functions are described on next page. Function bits are read/write and are cleared by INIT, PWR CLR or by loading a zero. Table 1 describes each controller function.

OCTAL NUMBER	FUNCTION BITS 03	02	01	FUNCTION
0	0	0	0	Off-line
1	0	0	1	Read
2	0	1	0	Write
3	0	1	1	Write End of File
4	1	0	0	Space Forward
5	1	0	1	Space Reverse
6	1	1	0	Write with Extended IRG
7	1	1	1	Rewind

0 GO — This bit is loaded with a 1 from the bus to initiate the function selected. When set, this bit clears CU RDY. GO is cleared when the command is sent to the tape unit. The time required to clear may vary when issued to a rewinding drive.

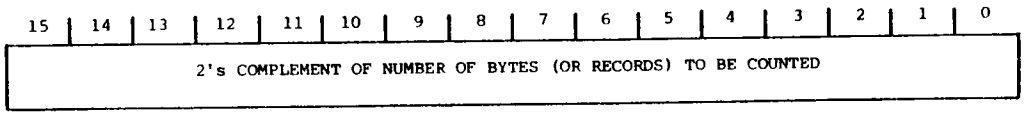
NO.	FUNCTION	DESCRIPTION
0	Off-Line	This function is used to return control to the tape transport so that tape can be rewound, reels changed, etc., without using processor time. This function places the selected tape unit in the off-line mode (SELR cleared) and causes it to begin a rewind operation. The controller cannot write on or read from the magnetic tape when the off-line function is used.
1	Read	This function permits reading from the magnetic tape. During the read operation, the data portion of the record is loaded into the controller data buffer for transfer to the memory. The LRC, CRC, preamble and postamble characters are read but are not transferred into memory. The read function advances the tape forward one record.
2	Write	This function allows writing on the magnetic tape. During the write operation, data from the bus is loaded into the controller data buffer register. The controller then transfers the data to the tape transport write heads. In NRZI mode the controller generates the necessary CRCC and the tape unit generates the LRCC. In PE mode the controller generates the required preamble and postamble characters. The write function advances the tape forward one record.
3	Write EOF	This function writes an end-of-file (EOF) mark on the tape. When selected, this function erases a 5-inch segment of tape prior to writing the first character. The PE tape mark and the NRZI EOF character and its associated LRCC are considered one record.

TABLE 3-1: CONTROLLER FUNCTIONS (CONTINUED)

NO.	FUNCTION	DESCRIPTION
4	Space Forward	This function is used to skip over a number of records to find a specific record on the tape. When selected, the space forward function causes the tape transport to advance forward a specified number of records. The number of records is determined by the value in the byte record counter. This value is loaded into the byte record counter by the program. Space forward is used for tape positioning only and, therefore, does not affect information stored on the tape or in memory.
5	Space Reverse	This function is identical to the space forward function except the tape moves in the reverse direction.
6	Write-with-Extended-IRG	This function is identical to the write function except that a 5-inch segment of tape is erased before writing the first character.
7	Rewind	This function is used for rewinding the tape on the supply reel so that the tape can either be unloaded from the transport or operation can start at the beginning of the tape. When this function is used, the tape moves in the reverse direction, at a much higher speed than for other functions, until the beginning-of-tape (BOT) marker is detected. Rewind is used for tape positioning only and has no effect on information stored on tape or in memory.

TABLE 3-1: CONTROLLER FUNCTIONS

3.1.3 Byte Record Counter (MTBRC) 772524



The byte record counter contains the 2's complement of the number of bytes or records to be transferred. The desired value is loaded by the program on a processor DATO. The MTBRC is cleared by INIT, PWR CLR or by loading zeros.

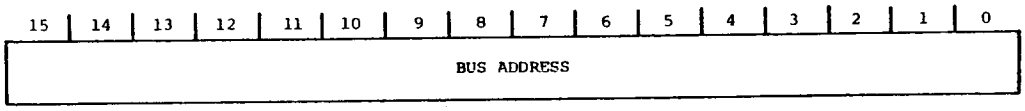
This is a 16-bit binary counter used to count bytes in a read or write operation and records in space forward or reverse operations. When used in a write or write-with-extended-IRG operation, this register is set by the program to the 2's complement of the number of bytes to be written on the tape. After the last byte of the record has been strobed from memory the register becomes 0.

In NRZI (non-return to zero method of recording) the controller then writes the CRC character and instructs the tape unit to write the LRC character. In PE (phase encoded) operation, the controller writes the postamble ones and zeros characters.

When used in a read operation, this register is set to a number equal to or greater than the 2's complement of the number of words to be loaded into memory. A record length error occurs whenever a read pulse is generated after the register is at 0. Neither the CRC or LRC character in NRZI mode or the preamble or postamble characters in PE mode are loaded into memory.

When used in a space forward or space reverse operation, the byte record counter register is loaded with the 2's complement of the number of records to be spaced. The counter is incremented by 1 at the end of record time, regardless of tape direction.

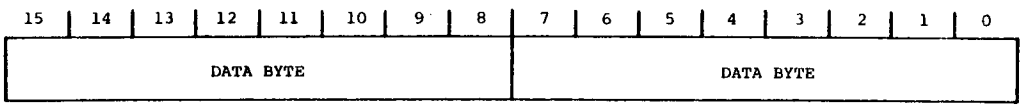
3.1.4 Current Memory Address Register (MTCMA) 772526



The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write-with-extended-IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation or from which the first byte is read in a write or write-with-extended-IRG operation. If the initial or final memory address is not on a word boundary (bit 00 is a 1) that NPR operation will transfer one byte of data. NPR transfers, when the memory address falls on word boundaries (bit 00 is a 0), will be on a word basis (2 bytes). The MTCMA is incremented by 1 for each byte of data transferred. Therefore, at any instance of time it points to the next higher address than the one which had most recently been accessed. In the error condition non-existent memory (NXM), the MTCMA contains the word address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI. All bits can be set or cleared on a processor DATO. INIT or PWR CLR clears all bits in the MTCMA.

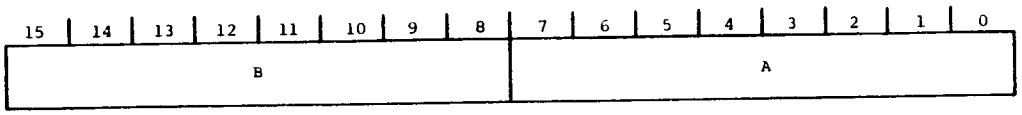
3.1.5 Data Buffer Register (MTD) 772530



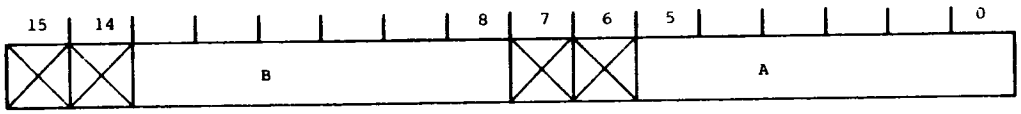
The data buffer is a 16-bit register which is used during read, write, or write-with-extended-IRG operations. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. As the tape characters are read from the tape they are assembled into a 16-bit word prior to transfer into memory. During a write or write-with-extended-IRG operation, the data buffer is a temporary storage register for words read from memory is disassembled into 2 tape characters during normal operation or into 4 tape characters in NRZI 7-track core dump mode. Figure 1 shows the relationship between tape characters and memory words for read, write, and write-with-extended-IRG operations.

In a NRZI read operation the LRC character enters the data buffer when character select (CHAR SEL) in the read lines register (MTRD) is a 1 and is inhibited from doing so when CHAR SEL is a 0. Thus, after reading a 9 channel tape, the data buffer contains the LRCC when CHAR SEL is a 1 and the CRCC when CHAR SEL is a 0. After reading a 7 channel tape,

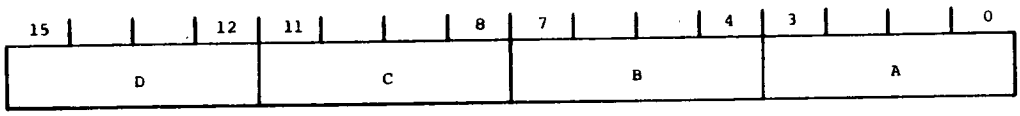
the data buffer contains the LRCC when CHAR SEL is a 1 and zero when CHAR SEL is a 0. After reading a NRZI EOF character the data buffer contains all 0's when CHAR SEL is a 0 and the LRCC when CHAR SEL is a 1.



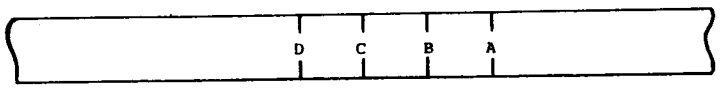
9-TRACK NRZI OR PE



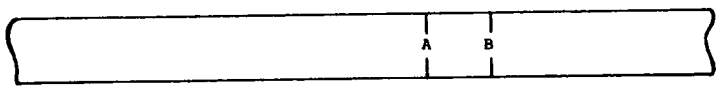
7-TRACK NRZI (BITS 6, 7, 14, 15 NOT USED)



7-TRACK CORE DUMP MODE



TAPE MOTION →
TAPE CHARACTERS - DEC MODE

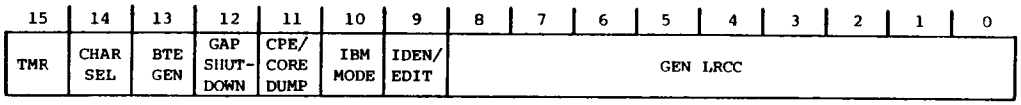


TAPE MOTION →
TAPE CHARACTERS - IBM MODE (9-TRACK)

FIGURE 3-1: RELATIONSHIP BETWEEN TAPE CHARACTERS AND MEMORY WORD

The MTD is available to the processor on a DATI and all bits can be set or cleared on a processor DATO. INIT or PWR CLR clears all bits of the MTD.

3.1.6 TU10 Read Lines (MTRD) 772532



BIT	CODE	FUNCTION
15	TMR	(Timer). The timer is a 10KHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of tape operations. This is a read-only bit.
14	CHAR SEL	(Character Select). This bit is used to select the last character of a record that is to be loaded into the data buffer. Selection is as follows:

BIT 14	7 CHANNEL NRZI	9 CHANNEL NRZI
1	LRCC	LRCC
0	Last Data Character	CRCC

This is a read/write bit which is cleared by INIT or PWR CLR.

13	BTE GEN	(Bad Tape Generator). This bit is used during diagnostics to check the bad tape error logic. When loaded with a one, CU RDY is set, causing a premature gap shutdown while characters are still being read. This, in turn, causes a bad tape error indication.

This is a write-only bit which is cleared by INIT, PWR CLR or the completion of a tape operation.

12	GAP SD	(Gap Shutdown). When set, this bit indicates the tape controller is in a gap shutdown period. This is a read-only bit.

BIT	CODE	FUNCTION
11	CPE/CORE DUMP	(Correctable Parity Error Status/Core Dump Mode Control). This is a dual purpose bit which provides status or is used as a control bit. As correctable parity error status, this bit indicates the controller detected a single dead time during a PE read operation. Data is corrected by modifying the bit corresponding to the dead track to insure proper byte parity. The data transferred into memory is the corrected data. Correctable parity error status is read-only and is cleared by INIT, PWR CLR or by the initiation of a tape operation. As core dump mode control, this bit will force the core dump mode in 7-track read, write, and write-with-extended-IRG operations. See DEN 8 and DEN 5 bits in MTC for alternate selection. This is a write-only bit which is cleared by INIT, PWR CLR or by writing a zero.
10	IBM MODE	This bit controls the assembling and disassembling of the 16-bit data word transferred to or from the processor on a read, write, or write-with-extended-IRG operation. When cleared, the even byte (bits 15-08) correspond to the second character on tape. This is the normal DEC mode of operations. See Figure 1. When this bit is set, the order of bytes is reversed. The odd byte (bits 15-08) corresponds to the first character, and the even byte (bits 07-00) corresponds to the second character on tape. This is the IBM mode of operation. This is a read/write bit which is cleared by INIT, PWR CLR or by writing a zero.
9	IDEN/EDIT	(Identity Status/Edit Mode Control). This is a dual purpose bit which provides status or control.

BIT	CODE	FUNCTION
		As identity status bit, this bit indicates that the controller has detected the PE identification burst. The ID burst is located at the BOT and is used to identify the tape as a PE tape. Identify status is a read-only bit and is cleared by INIT, PWR CLR or the initiation of a tape operation. As edit mode control bit, this bit allows the controller to operate in edit mode. In this mode of operation the processor can selectively replace any record of a previously recorded tape with an updated record. Edit mode control is a write-only bit which is cleared by INIT, PWR CLR or by writing a zero.
8-0	GEN LRCC	(Generated LRC Character). As NRZI read data is received from the tape unit, the controller generates a LRC character. This generated LRC character, which includes the parity channel plus 8 data channels, is available to the processor as bits 08 through 00. After the LRC character from tape is read, the generated LRC character should be all zeros. When a LRC error is detected, one or more of the bits 08-00 remains as a 1, indicating the channel or channels in error. These are read-only bits which are cleared by INIT, PWR CLR or the initiation of a tape operation.